HEWLETT hp PACKARD

2770A/2771A
DISC MEMORY

UPDATING SUPPLEMENT FOR INSTALLATION MANUAL

11 SEPT. 1970

MANUAL IDENTIFICATION

Manual Serial No. Prefix: NA

Manual Printed: Jan. 1970

Manual Part Number: 02770-90046

SUPPLEMENT DESCRIPTION

The purpose of this supplement is to adapt the manual to instruments containing production improvements made subsequent to the printing of the manual and to correct manual errors. Enter the new information (or the Change Number, if more convenient) into the appropriate places in the manual, identified at left.

INSTRUMENT CHANGES

Serial No. Prefix	Change
ALL	ALL

ASSEMBLY CHANGES

Ref Des	Description	HP Part No.	Rev	Changes

Change 1 dated 11 September 1970.

US-1

11000 Wolfe Road, Cupertino, California 95014, Tel. (408) 257-7000, TWX 910-338-0221
Europe: 1217 Meyrin-Geneva, Switzerland • Cable "HEWPACKSA" Tel. (022) 41.54.00

Printed in U.S.A.

CHANGE	DESCRIPTION
1	Change all HP 2770A and 2771A Disc Memory references to include the HP 2766A Magnetic Disc Memory, except as follows:

a. Page 2-1, paragraph 2-2. Change the last sentence to read:

This information should be used in conjunction with the inspection and handling information in section 2 of the appropriate Disc Memory Operating and Service Manual, part number 02770-9001 (2770A/2771A) or 02766-90003 (2766A).

b. Page 2-1, paragraph 2-10. Change the second sentence to read:

Refer to section 2 (paragraph 2.2.2 for 2770A/2771A, paragraph 2.3 for 2766A) of the Disc Memory Operating and Service Manual for an itemized inspection procedure.

c. Page 2-3, paragraph 2-13, step "l". Change the first sentence to read:

Connect the interconnecting cables as explained in section 2 (paragraph 2.5 for 2770A/2771A, paragraph 2.4 for 2766A) of the Disc Memory Operating and Service Manual.

BOB BOND - 40
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HEWLETT hp PACKARD

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HEWLETT hp PACKARD

DISC MEMORY

model
2770A/-01/-02/-03
2771A/-01/-02/-03

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CUPERTINO DIV

MANUAL SUPPLEMENT DEC 1969

MANUAL IDENTIFICATION

Manual	Part No.
2770A	02770-9001
2770A-01	02770-90043
2770A-02	02770-90044
2770A-03	02770-90045
2771A	02771-9001
2771A-01	02771-90002
2771A-02	02771-90003
2771A-03	02771-90004

SUPPLEMENT DESCRIPTION

The purpose of this supplement is to correct manual errors (Errata) and to adapt the manual to instruments containing production improvements made subsequent to the printing of the manual. Enter the new information (or the Change Number, if more convenient) into the appropriate places in the manual, identified at left.

CHANGE	DESCRIPTION
1	2770A/-01/-02/-03 units: On drawing 13770/13870, change item 14 part no. to 13989 for units with serial number of 17 or higher.
2	2771A/-01/-02/-03 units: On drawing 13770/13870, change item 14 part no. to 13989 for units with serial number of 27 or higher.
3	All units: a. On drawing 13775, Page 15, Remove -12V dc monitor callout from pin 18; insert callout in pin 33 column. Change +5V dc monitor callout from pin 30 to pin 31. Change +18V dc monitor callout from pin 25 to pin 24. Pin 12 "To" column: change A6-8 to A6-15. b. On drawing 13779, Page 3, move F & H register waveforms to show transitions on leading edge of C2. c. On drawing 13779, Page 4, remove word "trailing" and insert word "leading" in Note 2 (Documentation change only.) d. On drawing 11601, add a line from base of Q12 terminating in a pin block labeled 16. (Documentation change only.)

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Printed in U.S.A.

CHANGE	DESCRIPTION
	e. On drawing 11819, change 'R' callout to '$\overline{R}$'. Change $\overline{R}$ callout to R. (Documentation change only.)
	f. On drawing 13774, change Write Amp P/L from 11601 to 11306, schematic to 11326, Pictorial to 11336. Field units to be retrofitted.
4	Options 02 and 03 (50 Hz operation): Add pin 24 under polarization column for Decode Matrix board. Add note to indicate use of Clock Generator board no. 11874. (Documentation change only.)
5	2770A, 2770A-01, 2771A, and 2771A-01 (60 Hz operation): Add pin 24 under polarization column for Decode Matrix board. Add note to indicate use of Clock Generator board no. 11791. (Documentation change only.)
6	On drawing 11807, delete R11, R13, R14, R17, C4, C6, and C9.
7	On drawing 11726/11727, delete R11, R13, R14, R17, C4, C6, and C9. Add a jumper wire in place of C9.
8	On drawings 11811 and 11812/11813, delete R23, R25, R26, R30, C12, C14, and C17.

HEWLETT hp PACKARD

2770A/-01/-02/-03
2771A/-01/-02/-03
DISC MEMORY

UPDATING SUPPLEMENT FOR OPERATING AND SERVICE MANUAL

27 APR 1970

MANUAL IDENTIFICATION

Manual Serial No. Prefix: N/A

Manual Printed: SEPT 1969

Manual Part Number:
02770-9001 (2770A/-01, 2771A/-01)
02770-90043 (2770A-02/-03, 2771A-02/-03)

SUPPLEMENT DESCRIPTION

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INSTRUMENT CHANGES

Serial No. Prefix	Change

ASSEMBLY CHANGES

Ref Des	Description	HP Part No.	Rev	Changes

Changes 1 through 8 dated December, 1969.

Change 9 dated April 27, 1970.

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4	Options 02 and 03 (50 Hz operation): Add pin 24 under polarization column for Decode Matrix board. Add note to indicate use of Clock Generator board no. 11874. (Documentation change only.)
5	2770A, 2770A-01, 2771A, and 2771A-01 (60 Hz operation): Add pin 24 under polarization column for Decode Matrix board. Add note to indicate use of Clock Generator board no. 11791. (Documentation change only.)
6	On drawing 11807, delete R11, R13, R14, R17, C4, C6, and C9.

CHANGE	DESCRIPTION
7	On drawing 11726/11727, delete R11, R13, R14, R17, C4, C6, and C9. Add a jumper wire in place of C9.
8	On drawings 11811 and 11812/11813, delete R23, R25, R26, R30, C12, C14, and C17.
9	Incorporate attached pages into manual; all pages replace manual pages bearing the same page number or drawing number except as noted on the drawings. Note that in several cases two drawings with the same number are provided; this is to provide coverage of more than one version of a particular model. Model effectivity has been indicated, in each of these cases, by listing the appropriate serial numbers on the drawings.

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TABLE OF CONTENTS (Cont)

LIST OF ILLUSTRATIONS

The electronics assembly provides the interface between the disc device and the controller. The electronics assembly accepts integrated circuit logic levels for control, write data, and address selection. Outputs consist of read data and timing signals at logic levels.

1.3 SPECIFICATIONS

Specifications for the memory unit are contained in Table 1-1.

TABLE 1-1. SPECIFICATIONS

FUNCTIONAL REQUIREMENTS	The memory system will perform the following basic operations: a. Decode track address to select proper head(s). b. Receive and transmit data in NRZ bit serial format at a nominal rate of 3 MHz. c. Store data on the medium via the selected head(s). d. Provide clock and origin signals to controller. e. Provide sector timing signals to allow sector addressing. f. Display memory system status information.
PERFORMANCE REQUIREMENTS	
Capacity	
Addressable track capacity:	97,920 Data Bits
Addressable track organization:	90 Sectors: 64 words/sector; 17 bits/word
Total capacity:	Model 7301 - 6,406,144 Data Bits Model 7302 - 12,812,288 Data Bits
Heads	
Data storage:	Model 7301 - 256 plus 4 spares Model 7302 - 512 plus 4 spares
Clock:	1 plus 1 spare
Timing:	1 plus 1 spare

TABLE 1-1. SPECIFICATIONS (Cont)

FUNCTIONAL REQUIREMENTS (Cont)	
Processing Speeds:	
Rotational speed:	3450 RPM nominal
Data transfer rate from disc:	1.5 MHz nominal (2 track parallel)
Data transfer rate to controller:	3.0 MHz nominal (serial)
Average access time:	17.4 msec
Head select time:	20 μsec
Write to read stabilization time:	20 μsec
Date Error Rates (recoverable):	1 in 10^{10} bits
Noise immunity:	The disc memory shall be capable of operation in the presence of noise pulses of ± 5 volts peak amplitude not exceeding ± 100 ma peak current applied between the AC and DC common busses. Under this stress the disc memory should exhibit a mean error-free transfer of 1.0×10^8 bits. This level shall not affect writing in any way.
POWER REQUIREMENTS	
AC Power	
Voltage:	115 volts $\pm 10\%$
Phase:	Single - 3 wire
Frequency:	60 Hz $\pm 3\%$

TABLE 1-1. SPECIFICATIONS (Cont)

POWER REQUIREMENTS (Cont)

AC Power (Cont)

Run current:	Model 7301 - 0.5a Model 7302 - 0.6a
Start current:	Model 7301 - 1.8a Model 7302 - 2.0a

DC Power

Voltage	Max. Current	Regulation
+18 ±5%	2a	1%
-12 ±5%	1a	1%
+ 5 ±5%	2a	1%

Grounding	The AC and DC common busses shall be isolated.
Power Failure	No recorded data shall be affected by loss in any sequence, of AC or DC power in other than the write mode. In the write mode, only the track being written may be affected.

ENVIRONMENTAL REQUIREMENTS

Temperature

Operating:	0° to +50°C
Non-operating:	-40°C to +75°C

Altitude

Operating:	15,000 ft. (16.8 in.Hg.)
Non-operating:	25,000 ft. (10.8 in.Hg.)

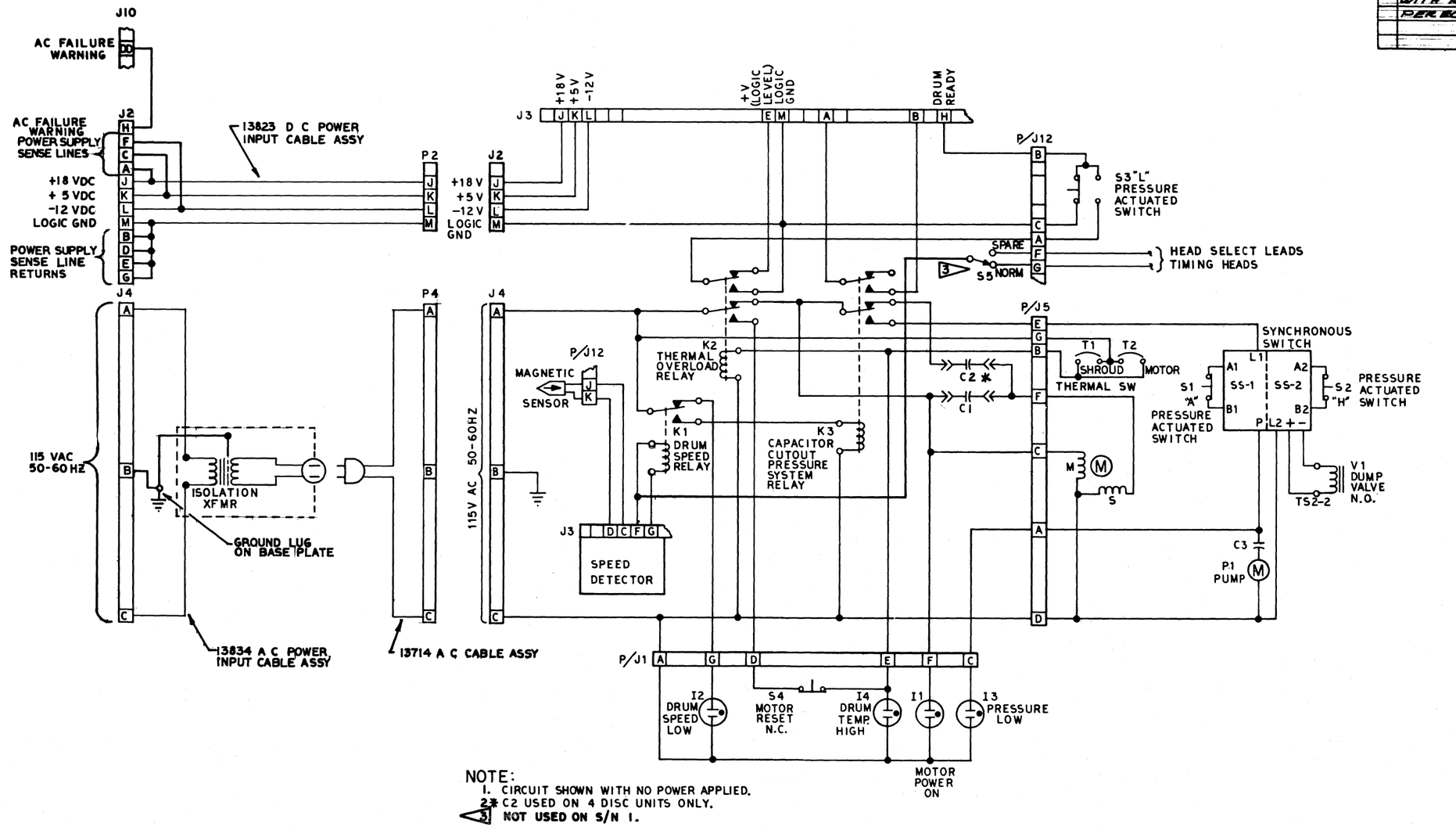
TABLE 1-1. SPECIFICATIONS (Cont)

INTERFACE REQUIREMENTS (Cont)	
Circuits:	All output signal lines from the memory system are driven by TTL gates capable of sinking 16 milliamps to ground in the output low state. Outputs are on twisted-pair lines with the return wire grounded near the driver. For reliable transmission, the return line must be tied to logic ground at the receiver. The signal line should be terminated with approximately 130 ohms to 2.5 volts. It is recommended that each output signal from the disc unit be received by using one edge of clock as a strobe for clocking into the receiving flip-flop so that noise on the line other than at strobe time be eliminated. All memory input lines will be received with TTL logic devices and will be terminated with approximately 130 ohms to +2.5 volts.
Logic levels:	
With lines properly terminated all interface signals shall have the following characteristics (signals are the logical inverse):	
Logic "one" or TRUE:	+5.1 volts maximum +2.4 volts minimum
Logic "zero" or FALSE:	+0.4 volts maximum 0.0 volts minimum

TABLE 1-1. SPECIFICATIONS (Cont)

INTERFACE REQUIREMENTS (Cont)	
Interface signal connectors:	All interface signal lines between the controller and the memory system are connected via one Winchester type MRAC-50-S (50 pin) connector. A mating connector is also provided.
AC Power:	The AC power required by the disc motor is supplied via a Bendix PTO 2A-12-3P connector. A mating connector is also provided.
DC Power:	The DC power required by the disc electronics is supplied via a Bendix PTO 2A-14-12P connector. A mating connector is also provided.

REV	ALTERATION	BY	DATE
A	ADDED WIRE FROM J2-H TO J10-DD Jackson 12-17-8		
B	INTERCHG'D C1 & C2 PER ECR 1073 Eade 4-5-67		
C	REVISED WIRING TO AGREE WITH RELAY BOARDS PER ECR 1228 GPR 11-26-69		



NOTE:
1. CIRCUIT SHOWN WITH NO POWER APPLIED.
2. * C2 USED ON 4 DISC UNITS ONLY.
3. NOT USED ON S/N 1.

FIGURE 3-5. SYSTEM CONTROL WIRING
Model 7302, Serial No. 14 and above
Model 7301, Serial No. 10 and above

		SYSTEM CONTROL WIRING	DIGITAL DEVELOPMENT CORPORATION
			1 / 13832

Drum speed relay K1 is controlled by the speed detector which, in turn, responds to pulses from the disc speed magnetic sensor. As the drive motor causes the disc speed to increase, the rate of the magnetic sensor pulses to the speed detector increases proportionately, and when the disc speed reaches 3300 rpm, the speed detector energizes relay K1. The disc speed relay remains energized as long as the disc speed is maintained above 3100 rpm. When relay K1 energizes, the DRUM SPEED LOW lamp I2 goes off and the AC power at relay K1 contacts is switched to relay K3.

The energized capacitor cutout/pressure system relay K3 removes AC power from the motor-start capacitor C1, permitting the motor to operate on the AC power applied from the normally-closed contacts of thermal overload relay K2 to the main power winding. The MOTOR POWER ON lamp I2 remains on. The energized contacts of relay K3 route the AC power to the synchronous switch to control the pump motor P1 and dump valve V1 operation.

On receipt of AC power at pins L1 and L2, the synchronous switch SS-1 section starts pump P1, and the SS-2 section energizes the dump valve V1 solenoid. The synchronous switch SS-1 and SS-2 sections contain SCR switch circuits used for eliminating voltage transients inherent in any circuits that require switching combined with inductive loads. The AC output of SS-1 to pump P1 is controlled by the "A" pressure-actuated S1, and the SS-2 AC output to the dump valve is controlled by the "H" pressure-actuated switch S2, as explained in the following paragraphs. Initially, the synchronous switch applies AC power to pump P1 and parallel PRESSURE LOW lamp I3. Pump P1 starts supplying pressure to the head actuating system and lamp I3 lights and remains on. At the same time, energized dump valve V1 closes and allows the head pneumatic system pressure to build up to operating level. The dump valve, closed when energized, opens to allow a controlled discharge of pressure whenever system shutdown occurs or AC power is inadvertently removed.

When the pump brings the actuating system up to the required average pressure of 1-5/8 psi, the "A" pressure-actuated switch S1 opens, causing the synchronous switch to interrupt AC power to pump P1. The pump then stops and PRESSURE LOW lamp I3 goes off.

If the system pressure exceeds 1-3/4 psi at any time, the "H" pressure-actuated switch S2 opens, causing the synchronous switch to remove power from dump valve V1. The deenergized dump valve releases the gas until pressure returns to normal.

If the pressure drops below 1-5/8 psi, the pump will be turned on by action of the "A" switch S1 and pressure will be restored. When this occurs, the PRESSURE LOW lamp will come on for a few seconds, but the operation of the unit will not be interrupted.

When the head actuation pressure is above 1.5 psi, indicating the heads are actuated properly, the "L" (low) pressure-actuated switch S3 closes to provide a status signal from pin J3-E to pin J3-H. When switch S3 is closed to the normal state, the signal indicates to the control logic that the drum is at operating speed, the head pressure system is activated, and the system is ready for operation. If the "L" switch is opened by a reduction in pressure below 1.5 psi, an abnormal state status indication is switched to pin J3-H and sent to the controller.

The drive motor is protected from thermal overload by parallel thermostats T1 and T2. If the shroud temperature reaches 150°F or if the motor housing temperature reaches 270°F, the respective thermostat, T1 or T2 closes, applying AC power from P4-A through the completed thermostat switch patch to thermal overload relay K2 and the DRUM TEMP HIGH lamp I4. Relay K2 energizes and lamp I4 remains on as long as the overload condition exists. When relay K2 is energized, AC power is removed from the drive motor, the synchronous switch, the dump valve, and the pump. Opening of the AC power circuit deenergizes the solenoid dump valve, causing the head actuation pressure to reduce to zero, and automatically retracting the read and write heads. Drum speed relay K1 is deenergized when the disc speed slows below 3100 rpm, because of the deenergized drive motor. When relay K1 deenergizes, the SPEED LOW lamp I2 goes on again.

When the actuated thermostat, T1 or T2, cools, its contacts will automatically reopen, removing the AC power applied from the thermostats to thermal overload relay K2. However, relay K2 remains energized because of the holding AC voltage applied from the normally-open contacts of K2 through MOTOR RESET switch S4. To restart operation, MOTOR RESET switch S4 must be pressed to remove the holding voltage from relay K2, permitting the relay to become deenergized and the DRUM TEMP HIGH lamp to go off. The AC voltage will then be reapplied to the drive motor, dump valve, and pump.

signals into NRZ signals is accomplished by a read flip-flop which is clocked with a clock pulse derived from the clock track.

3.3.2.1 READ/WRITE CLOCK GENERATION. From the clock read amplifier, the clock is coupled to the input of two identical clock generator circuits which shape the symmetrical clock into pulses of predetermined width. The clock generator one-shot multivibrator will trigger on either the positive or negative-going edge of the clock depending on which input is used. (See Figure 3-7.)

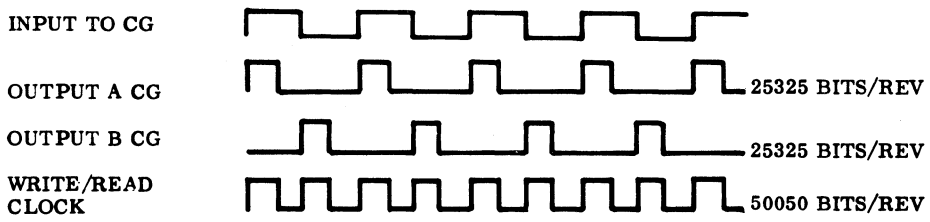


Figure 3-7. Clock Generation Timing

Clock generator circuit A, Figure 3-8, is wired to trigger on the positive-going edge of the clock. Thus two clocks, designated C_1 and C_2, are formed which are respectively 180° out of phase.

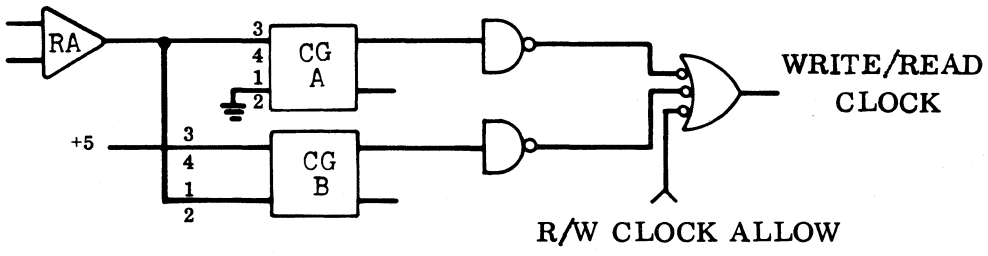


Figure 3-8. Clock Generator Circuits A and B

The outputs of the clock generators are inverted, ORed and gated by a read/write clock allow signal in a 3-input NAND gate. Clock generators C_1 and C_2 thus form the 3 MHz R/W clock of 50,650 bits/disc revolution.

3.3.2.2 ORIGIN PULSE ($\overline{TOP}$) AND SECTOR CLOCKS ($\overline{SC}$) GENERATION. The origin pulse and sector clocks are recorded on the same timing track and share a common timing preamplifier. The timing is written in a logical code of "1's" and "0's" and is decoded into NRZ timing with a decode flip-flop located in the electronic card rack. The NRZ multiplexed timing signal is then separated in an origin pulse and sector clocks by shift registers and logic gating circuits.

The $\overline{TOP}$ pulse is six-clock periods wide, with respect to the read/write clock, and is logically true every other disc revolution.

There are 45 sectors per disc revolution, plus one guard band. Each sector is 1124 clock (3 MHz) bits in length. There are two sector clocks per sector, each sector clock being logically true for one-clock period. The first sector clock (SCa) is logically true 68 bits before the second sector clock (SCb), except for sector one. SCa is true 62 bits prior to SCb for sector one. The guard band is 70-clock periods in duration and follows the leading edge of the index pulse (an internal memory signal) every disc revolution.

Digital Development Corporation Drawing Number 13779, which is included in Section 6, shows the above timing relationship in detail.

3.3.3 WRITE LOGIC

Data to be written into the disc memory is presented to the disc file as a 3 MHz NRZ signal. The disc system is designed to write this data at a 1.5 MHz rate. It is therefore necessary to divide the incoming data into two parts. Data is gated with the read/write clock allow (RWA) and sent to two flip-flops as shown in Figure 3-9. One flip-flop is clocked with $\overline{C_1}$ and the other is clocked with $\overline{C_2}$. One flip-flop output will consist of the odd-numbered bits, the other output will consist of the even-numbered bits. Data is to be clocked into the write amplifiers at clock C_1 time, Figure 3-10,

so it is necessary to resync the odd-numbered bits again with another sample flip-flop. This circuit is clocked with clock $\overline{C2}$. The timing relationships are shown in greater detail on Digital Development Corporation Drawing Number 13779, provided in Section 6.

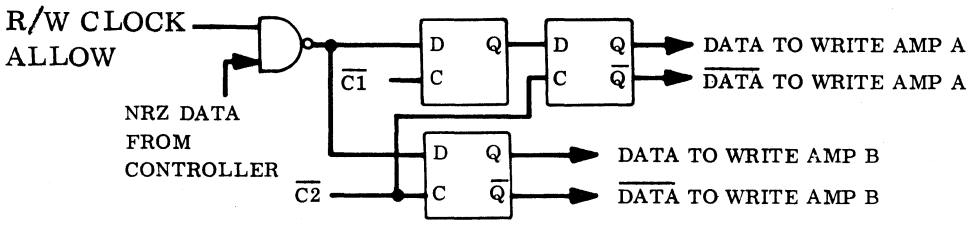


Figure 3-9. Separation of NRZ Data from Controller into Two Data Lines

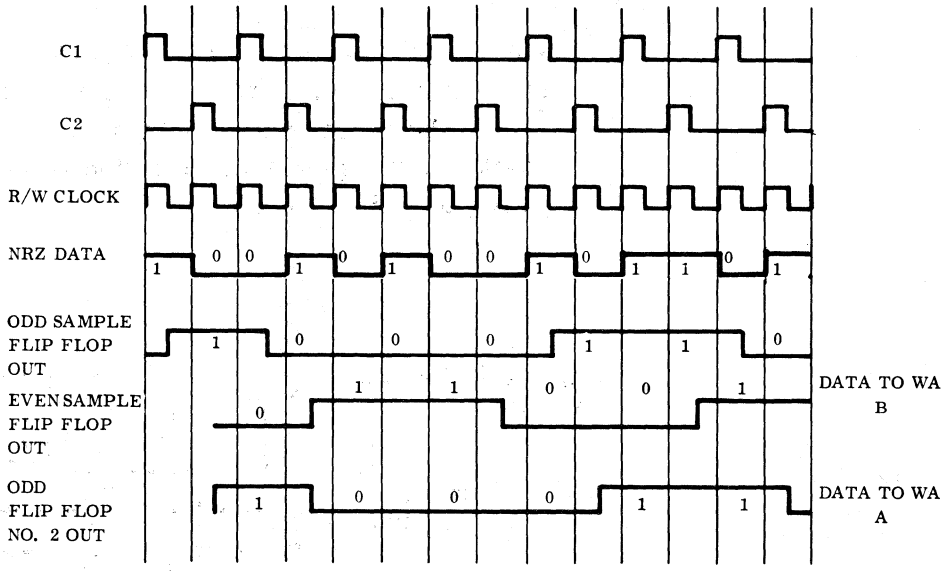


Figure 3-10. Timing For Data Separation

3.3.4 WRITE AMPLIFIER OPERATION

The function of the write amplifier is to convert the NRZ data into phase modulated data, and to control a pair of write current drivers. Conversion of NRZ data into phase modulated data is accomplished by a special flip-flop located on the write amplifier card. Data and $\overline{\text{data}}$ are applied to the write flip-flop through dc control gates which resynchronize data and $\overline{\text{data}}$ with clock C1. The output of these gates are conducted to the bases of the write flip-flop switching transistors. If data and clock C1 are TRUE, the write flip-flop will set. If $\overline{\text{data}}$ and clock C1 are TRUE, the write flip-flop will be reset. In addition to the dc control gate outputs which set or reset the write flip-flop, another gate is added. This gate is common to both bases of the write flip-flop switching transistors. Clock $\overline{\text{C2}}$ is connected to this gate. Remember that clock C2 is 180° displaced from clock C1. Consider now that the flip-flop is setting and resetting depending on the condition of (data and C1) and ($\overline{\text{data}}$ and C1). The flip-flop will be set or reset with the positive-going edge of C1. **If $\overline{\text{C2}}$ is input to the bases of the write flip-flop switching transistors, then at each C2 time the flip-flop will toggle to the opposite state.**

The phase modulated data and $\overline{\text{data}}$ are coupled to a pair of write enable gates, G_1 and G_2, Figure 3-11, which allow passage only if the write enable signal is present. This signal must be high (true) to enable the write amplifier. If the write enable signal is low, then write enable gates G1 and G2 will be inhibited.

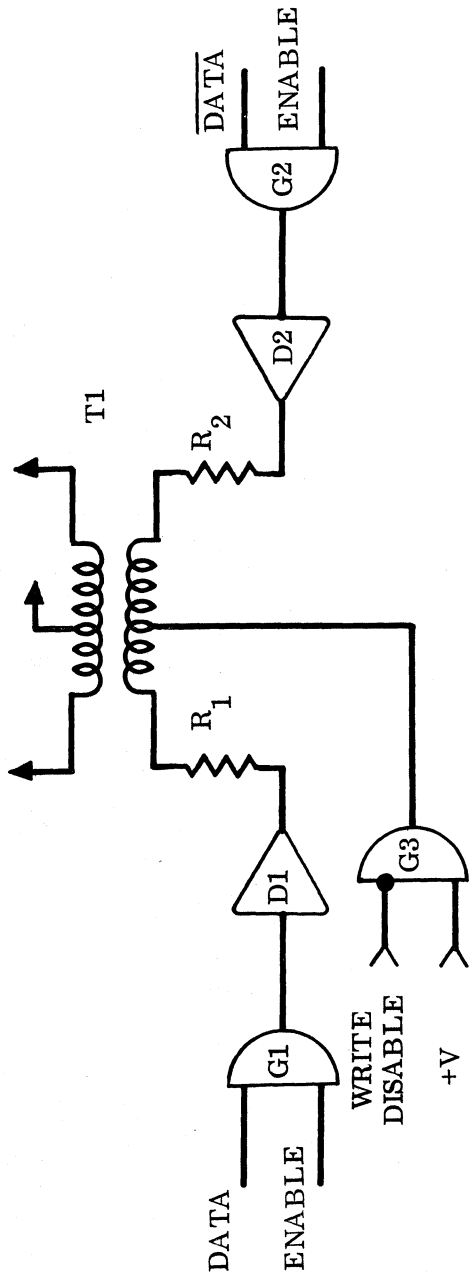


Figure 3-11. Write Enable/Disable Gates

Current drivers D1 and D2, Figure 3-12, are NPN transistors with emitters at ground potential and collectors connected to current-determining resistors R1 and R2. The R1 and R2 values are set to allow 125-ma of write current to flow through each half of write transformer T1. Because phase modulated data and data are 180° out of phase with each other only one current driver is "on" at any one time. Collector potential Vcc is supplied to the center tap of transformer T1 via disabling gate G3. Disabling gate, G3 is a PNP transistor switch with emitter connected to +V and collector connected directly to the center tap of transformer T1. The base of this transistor must be grounded to enable this switch. If the input to this switch goes to +18V at anytime, write current will cease to flow.

Write amplifiers A and B deliver write current to all read/write heads in the memory system. Only one head can be written into at one time by each write amplifier. Current distribution is accomplished by forming a matrix of "X" and "Y" lines. This matrix will be discussed in detail in another section. For now, consider that the memory consists of one read/write head. The "X" lines will be connected through the "X" amplifier; the "Y" line will be returned to ground through one "Y" amplifier.

The write amplifier, Figure 3-13, has been enabled and is delivering phase modulated current to the write transformer in push-pull fashion. Diodes D1 and D2 are turned off until the "X" amplifier receives an enable signal at the bases of Q1 and Q2. Current will not flow until Q3, in the "Y" amplifier, is turned on to supply a ground return at the center-tapped read/write head. The "X" amplifier and "Y" amplifier are enabled at the same time by the decoding of the track address lines.

At the write transformer, consider point "A" positive with respect to point "B". Current will flow through D1 and D3, the emitter collector junction of biased-on transistor Q3, through D5 and D7, through the left half of the read/write head, completing its path through transistor Q3 to ground. A similar current path through the right half of the head is used for the opposite polarity signal out of the write amplifier. Waveforms of normal and abnormal write current are provided in Figure 3-14.

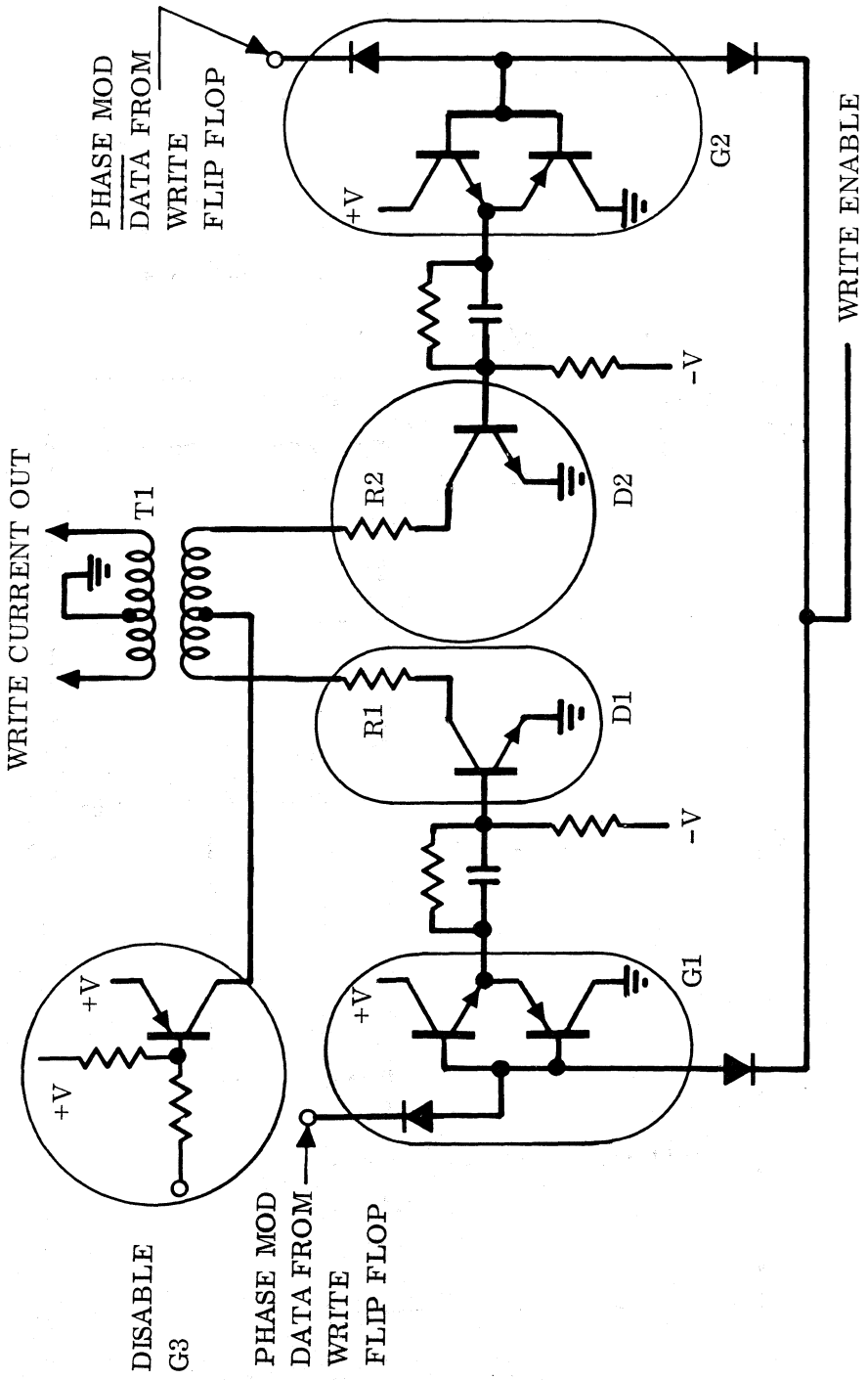


Figure 3-12. Write Head Current Drivers

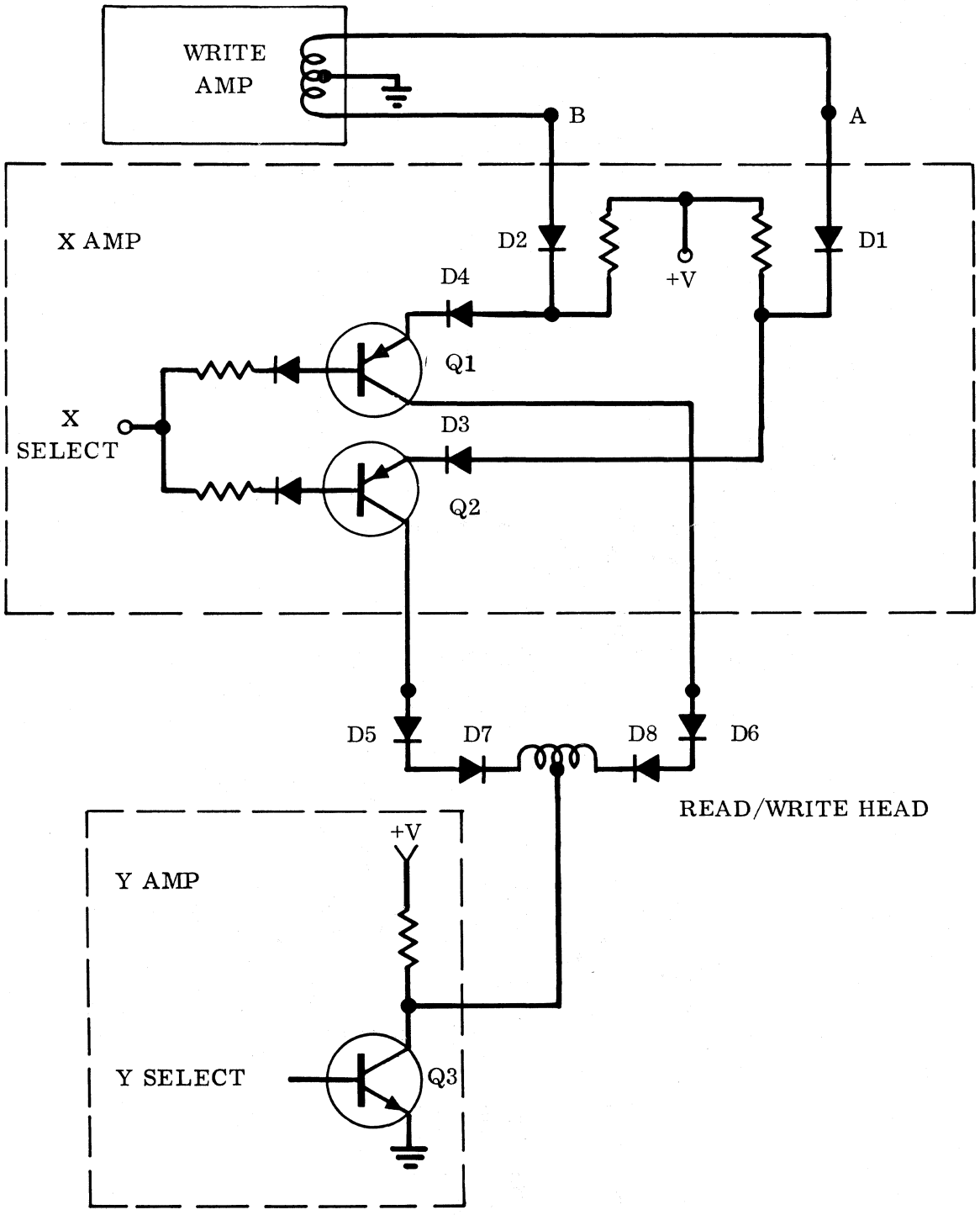


Figure 3-13. Write Amplifier Push-Pull Operation

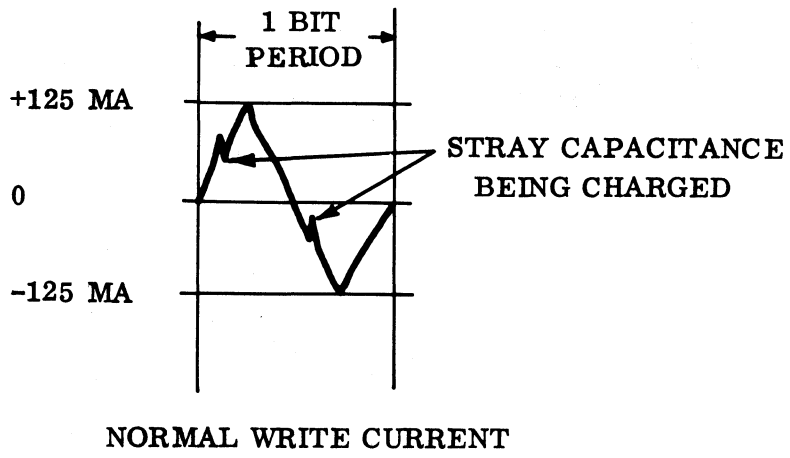


Figure 3-14. Write Current Waveforms

3.3.5 ADDRESSING AND HEADPLATE ORGANIZATION

There are up to four rotating discs located within the disc housing. Each of the flat sides on the discs is used for data storage. Each flat side has a capacity of 64 recording tracks, and is serviced by one headplate assembly containing the 64 read/write heads. This section describes the electrical organization of the headplates and their associated addressing circuitry.

3.3.5.1 HEADPLATE AND MATRIX ORGANIZATION. Electrically, the 64 read/write heads of each headplate, Figure 3-15 and 3-16, are separated into 4 "X" lines, each containing 16 read/write heads. Each "X" line is serviced by one "X" amplifier. Each of the 16 read/write heads is a center-tapped coil. The center tap of each head in the "X" line is made common with one head in each of the remaining three "X" lines. A functional schematic diagram of the headplate organization, Digital Development Corporation Drawing Number 14011, is provided as Figure 3-17.

Matched pairs of isolation diodes are in series with each of the read/write heads. These diodes reduce noise as well as prevent cross-coupling into an unselected head. All electrical connection and input points are made on a terminal board mounted on the back of each headplate. This terminal board also contains the isolation diodes. Total matrix size of each headplate is 4 "X" and 16 "Y" lines. (See Figure 3-17.) As there is a total of 8 headplates, the second 4 headplates use the same 16 "X" amplifiers that service the first 4 headplates. Separation is accomplished with 16 different "Y" lines. Total matrix size is 16 "X" lines (selected two at a time) and 32 "Y" lines. The "X" amplifiers are located on the back of the lower 4 headplates with jumper wires routed to the upper 4 headplates. The 32 "Y" lines are routed through a connector on the baseplate from the outputs of 32 "Y" amplifiers located on the "Y" decode matrix board. The "X" select lines to the "X" amplifiers are routed through a connector on the baseplate from the 16 decode drivers outputs. Track selection is accomplished by enabling a particular "X" amplifier and "Y" amplifier.

3.3.5.2 ADDRESSING. As previously discussed, data from the controller is divided into two sections, A and B. This data is transmitted to separate write amplifiers and written simultaneously on different recording tracks. Because one addressable track, with respect to the controller, is two disc revolutions in duration, it is necessary to switch to two new tracks at the end of the first revolution of the disc. Switching is accomplished within the disc system by switching track address flip-flop TA at index time. Therefore, the address sent by the controller remain the same during both revolutions of the disc.

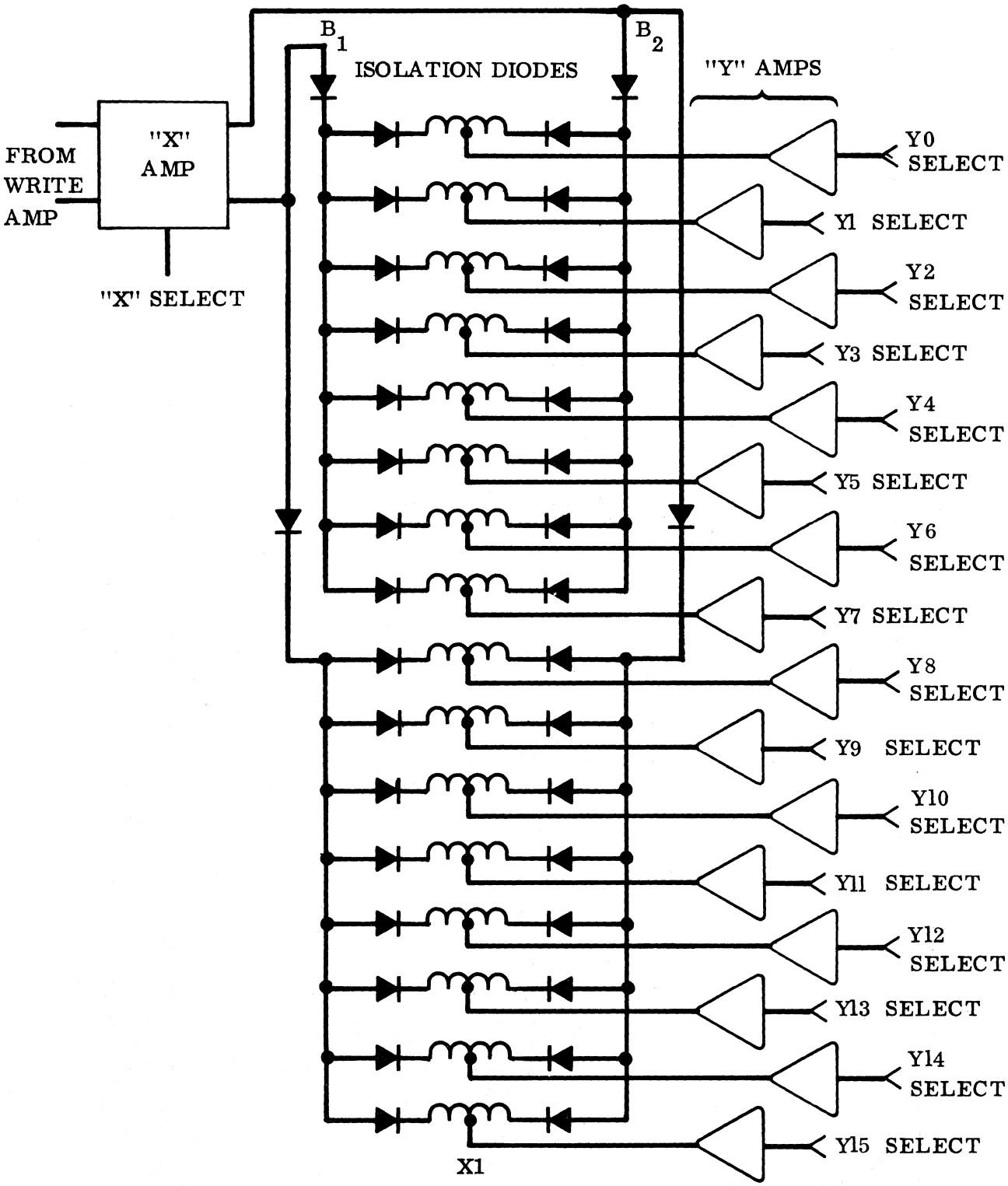


Figure 3-15. 16 R/W Heads with Common X Amp (1/4 Headplate)

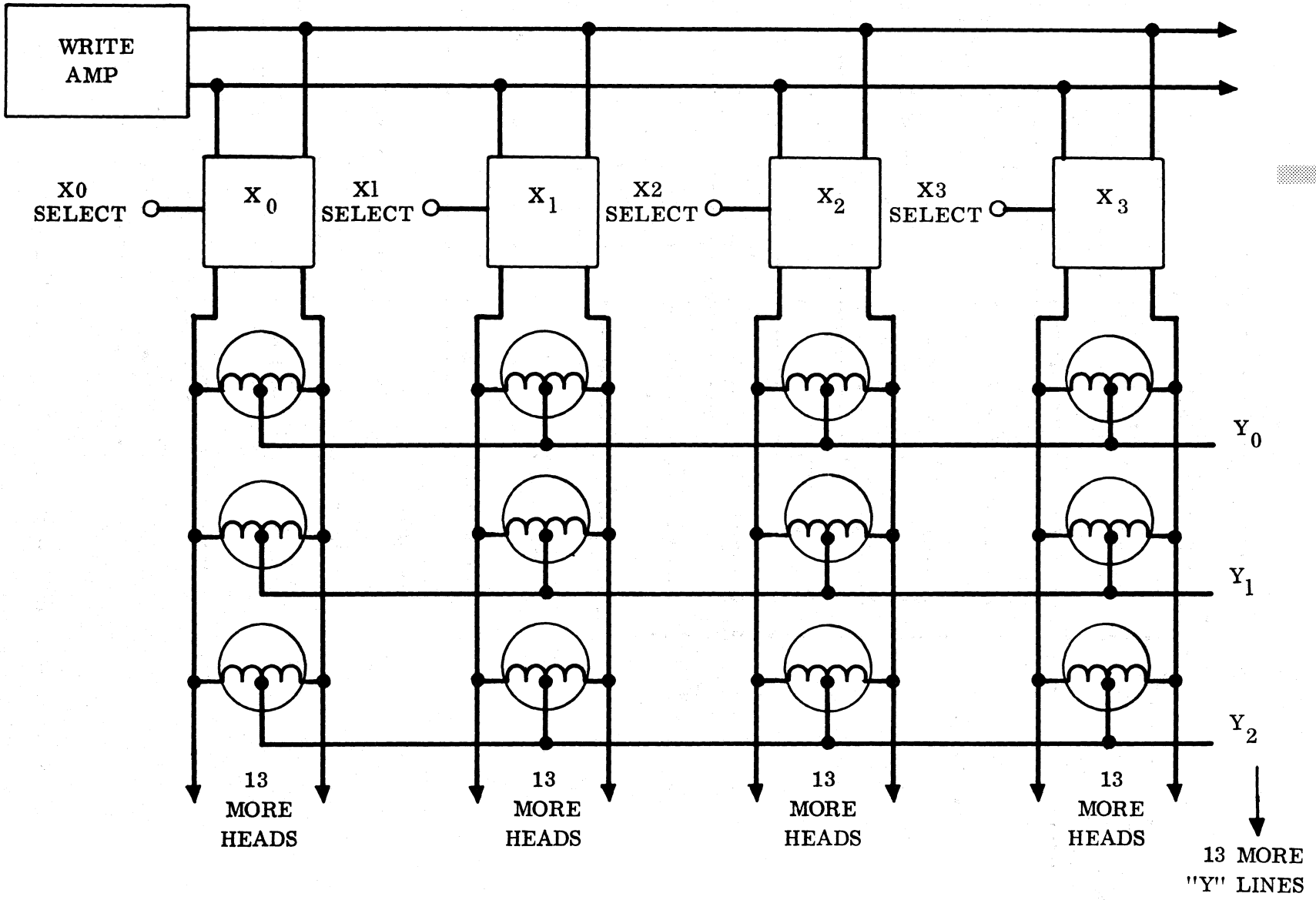


Figure 3-16. Block Diagram of Typical Headplate

TABLE 3-2. "Y" LINE ADDRESS LOCATION

Location (disc surface)	Headplate "Y" Line Input	Octal Address
L1, U1, L2, U2	A1	0N0 * $\overline{TA}$
	A2	0N0 TA
L1, U1, L2, U2	A3	0N1 $\overline{TA}$
	A4	0N1 TA
L1, U1, L2, U2	A5	0N2 $\overline{TA}$
	A6	0N2 TA
L1, U1, L2, U2	A7	0N3 $\overline{TA}$
	A8	0N3 TA
L1, U1, L2, U2	A9	0N4 $\overline{TA}$
	A10	0N4 TA
L1, U1, L2, U2	A11	0N5 $\overline{TA}$
	A12	0N5 TA
L1, U1, L2, U2	A13	0N6 $\overline{TA}$
	A14	0N6 TA
L1, U1, L2, U2	A15	0N7 $\overline{TA}$
	A16	0N7 TA
L3, U3, L4, U4	A1	1N0 $\overline{TA}$
	A2	1N0 TA
L3, U3, L4, U4	A3	1N1 $\overline{TA}$
	A4	1N1 TA
L3, U3, L4. U4	A5	1N2 $\overline{TA}$
	A6	1N2 TA
L3, U3, L4, U4	A7	1N3 $\overline{TA}$
	A8	1N3 TA

* $0 \leq N \leq 7$

TABLE 3-2. "Y" LINE ADDRESS LOCATION (Cont)

Location (disc surface)	Headplate "Y" Line Input	Octal Address	
L3, U3, L4, U4	A9	1N4	$\overline{TA}$
	A10	1N4	TA
L3, U3, L4, U4	A11	1N5	$\overline{TA}$
	A12	1N5	TA
L3, U3, L4, U4	A13	1N6	$\overline{TA}$
	A14	1N6	TA
L3, U3, L4, U4	A15	1N7	$\overline{TA}$
	A16	1N7	TA

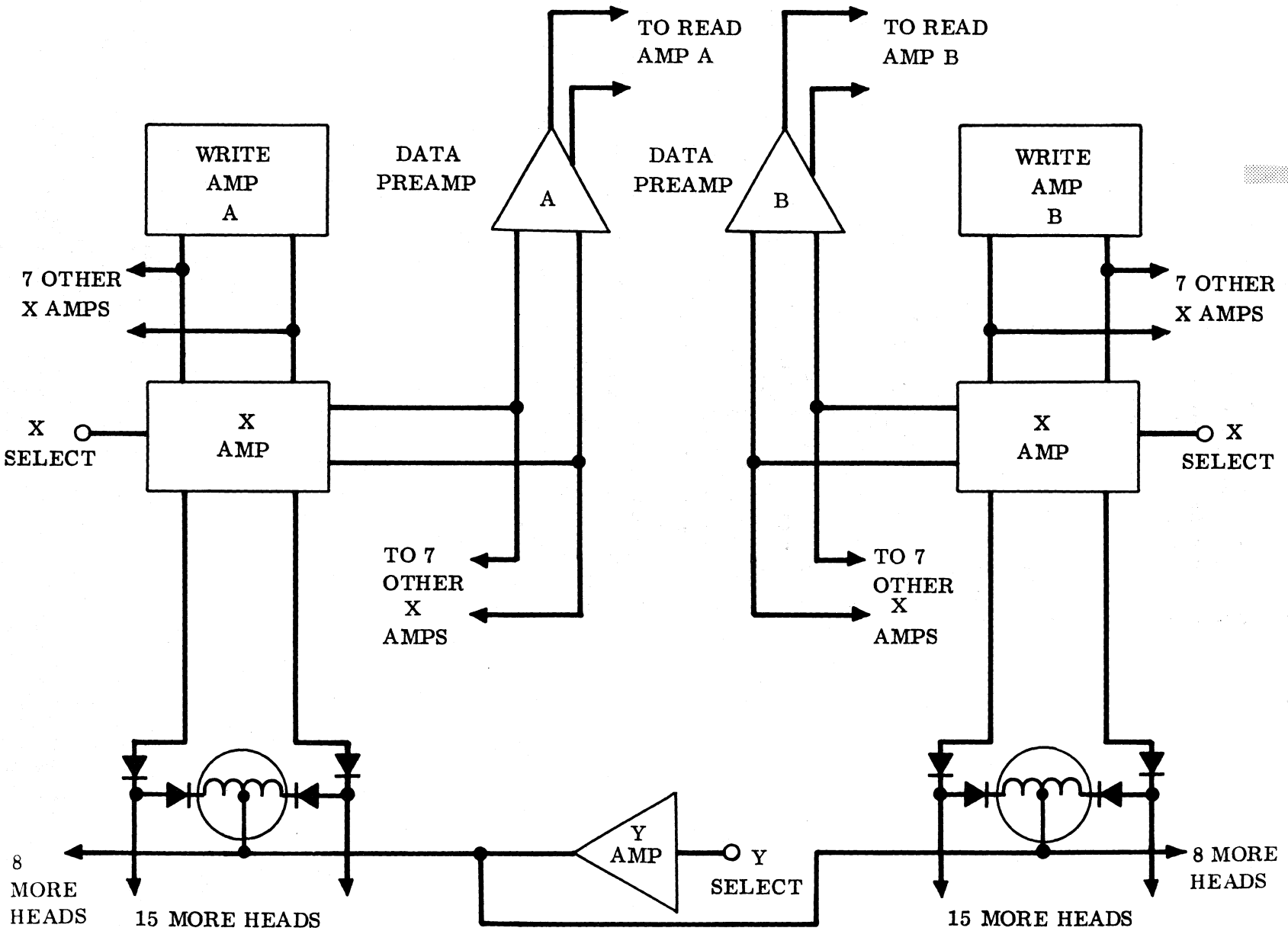


Figure 3-20. Read/Write/Select Block Diagram

diodes in series with each read/write head. The function of the "Y" amplifiers in the read mode is to provide a return path for the bias current. Head selection in the read mode is the same as in the write mode.

3.3.6.1 READING WITH A TYPICAL READ/WRITE HEAD. (Refer to Figure 3-21.) Assume that "X" amplifier X_0 and "Y" amplifier Y_0 are selected. DC current flows from V through resistor R1, diode D13, the emitter-collector of transistor Q2, diodes D2 and D4, half of the read/write head, and through Q1 to ground. DC current also flows from V through resistor R2, diode D11, transistor Q1, diodes D1 and D3, half of the read/write head, and through Q1 to ground.

Read buss diodes D12 and D14 are forward biased by current flowing from V through resistors R2 and R1, transistors Q1 and Q2, read buss diodes D12 and D14, and through Q2 and Q1 to -4V DC. The low-level AC readback signals are coupled to the input of the data preamplifiers. The linear data preamplifier outputs are coupled to the read amplifiers where they are further amplified into logic levels. The read amplifiers are saturable comparators that provide a positive voltage or ground level output, depending on the relative polarity of the input signal. DC feedback is used to ensure signal symmetry.

The readback signals are then decoded into NRZ data with D flip-flops that are gated with the data strobe clock. (See Figure 3-23.) The data strobe clock is delayed so that it will examine the second half of each bit. The flip-flop will set if the data is high at strobe time and reset if the data is low at strobe time.

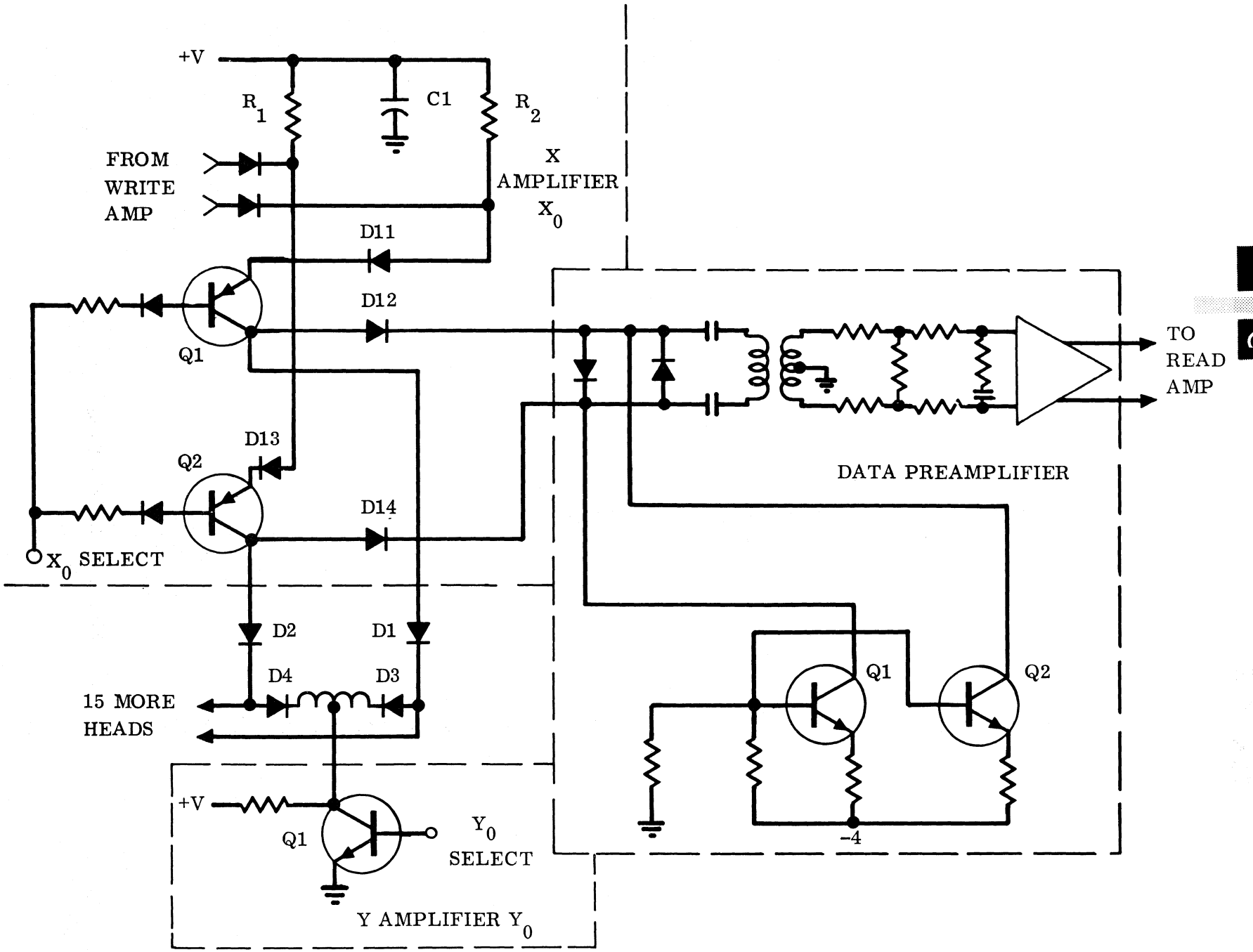


Figure 3-21. Read/Write/Select Schematic

Figure 3-22. Not Used

clock $\overline{C2}$ and $\overline{C1}$ respectively. The outputs of the data latches become true with their respective clocks and the two outputs are combined through an OR gate. The OR gate output is inverted and processed to the controller. The OR gate in inhibited from operation during the write mode by an inhibit signal.

D D C

3.4 SYSTEM / CONTROLLER INTERFACE

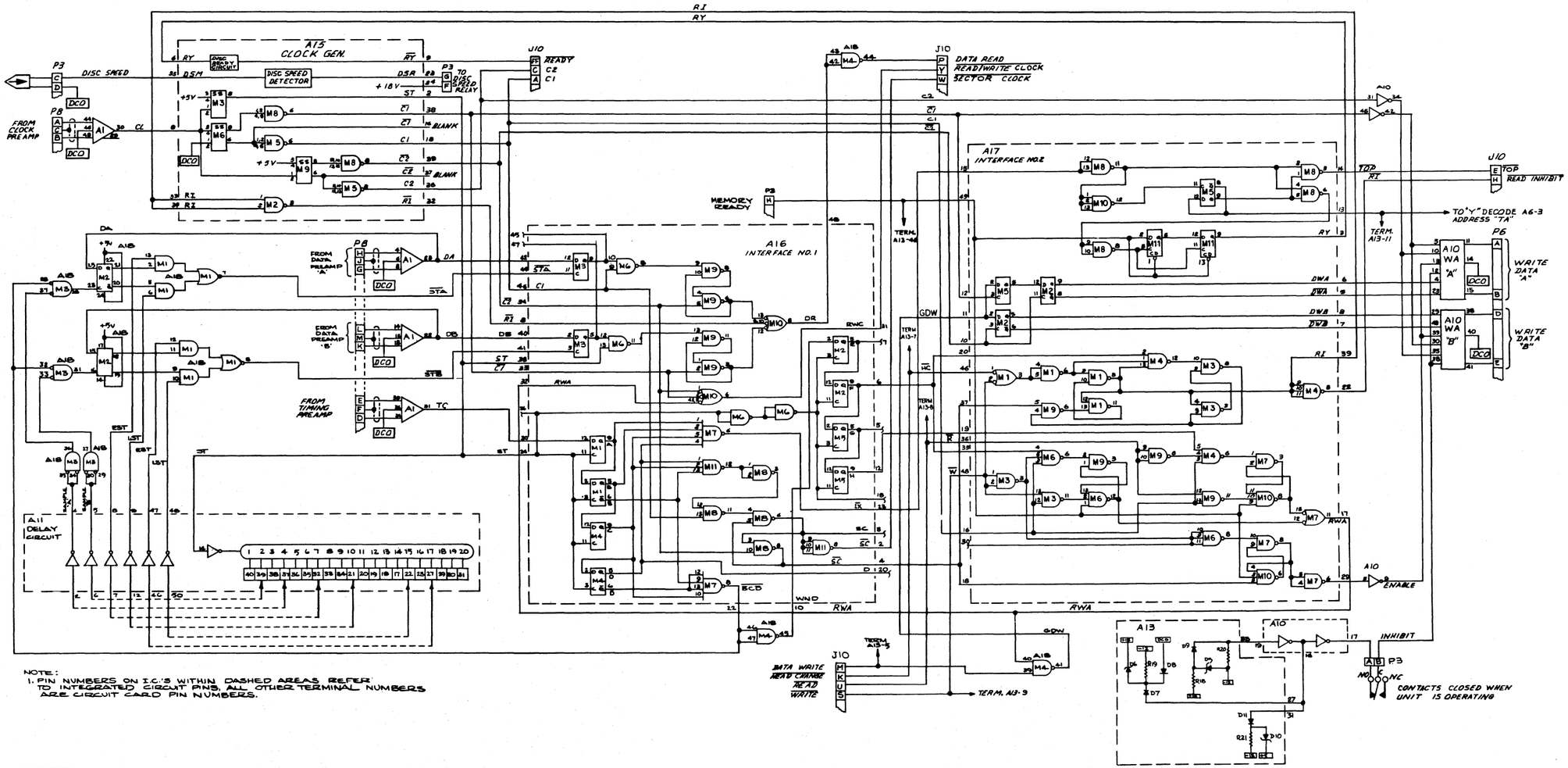
3.4.1 FUNCTIONAL BLOCK DIAGRAM

A functional block diagram of the system is provided in Figure 3-24, consisting of two sheets. Data control logic is shown on sheet 1. Address decoding logic is shown on sheet 2. Sheet 1 of the drawing depicts elements of the eight circuit cards (A1, A10, A11, A13, A15, A16, A17, A18). Card A1 contains the four read amplifiers; one each for clock, timing code, channel A data, and channel B data. Card A10 has the write amplifiers (for both data channels A and B), and also several inverters. Card A11 is the delay line card. Card A13 is the terminator card that has line termination resistors and voltage monitoring diodes. The function of card A15 is to generate the three clocks (C1, C2, and ST) and to supply a current sink for the disc-speed relay.

Card A16 is the Interface No. 1 card. As shown on the block diagram, the lower portion of card A16 has flip-flop shift registers and gates used for generating the sector and index timing signals from the coded information recorded on the timing track. The upper portion contains channel A and B read flip-flops and the gates required to serialize the two data streams of 1.5 MHz data into a single 3 MHz stream.

Card A17 is the Interface No. 2 card. The upper portion generates the signals ($\overline{\text{TOP}}$ and TA) required to simulate an 1800-rpm disc speed and also generates the delayed ready signal (RY). The three flip-flops shown in the center of the A17 logic, separate alternate data bits in the 3 MHz data write into two parallel 1.5 MHz data streams. The read inhibit logic and the logic that causes the flow of read/write clocks to begin at the correct times is below these flip-flops. At the very bottom, there is the write enable logic that causes writing to continue for a short time after the write command is removed. Card A18 contains the circuitry necessary for selecting the correct data strobe for each of the two data channels.

Sheet 2 of the functional block diagram shows the "Y" and "X" decode logic that generates the "X" and "Y" select signals that control the matrix of read/write heads. The inputs consist of the address lines (T0 through T6) from the controller and a signal (TA) generated in the memory that selects different halves of the memory during alternate disc revolutions.



NOTE:
1. PIN NUMBERS ON I.C.'S WITHIN DASHED AREAS REFER TO INTEGRATED CIRCUIT PINS. ALL OTHER TERMINAL NUMBERS ARE CIRCUIT CARD PIN NUMBERS.

NOTE:

1. Pin numbers on I.C.'s within dashed areas refer to integrated circuit pins. All other terminal numbers are circuit card pin numbers.

FIGURE 3-24. FUNCTIONAL BLOCK DIAGRAM (SHEET 1 OF 2)

FUNCTIONAL BLOCK DIAGRAM
DIGITAL EQUIPMENT CORPORATION

DWG. NO. 13777/13882

REV	ALTERATION	BY	DATE
A	SEE SH. 1 Jackson 2-4-9	ERA	2/7/69
	DECODE OUTPUT INVERTER SYMBOL	ERA	2/9/69
	WAS AMPLIFIER PER ECR 738	NVL	2/17/69
B	SEE SHT 1	ERA	3/10/69
C	SEE SHT 1	PC	9/2/69

C.N 9 2-17-69

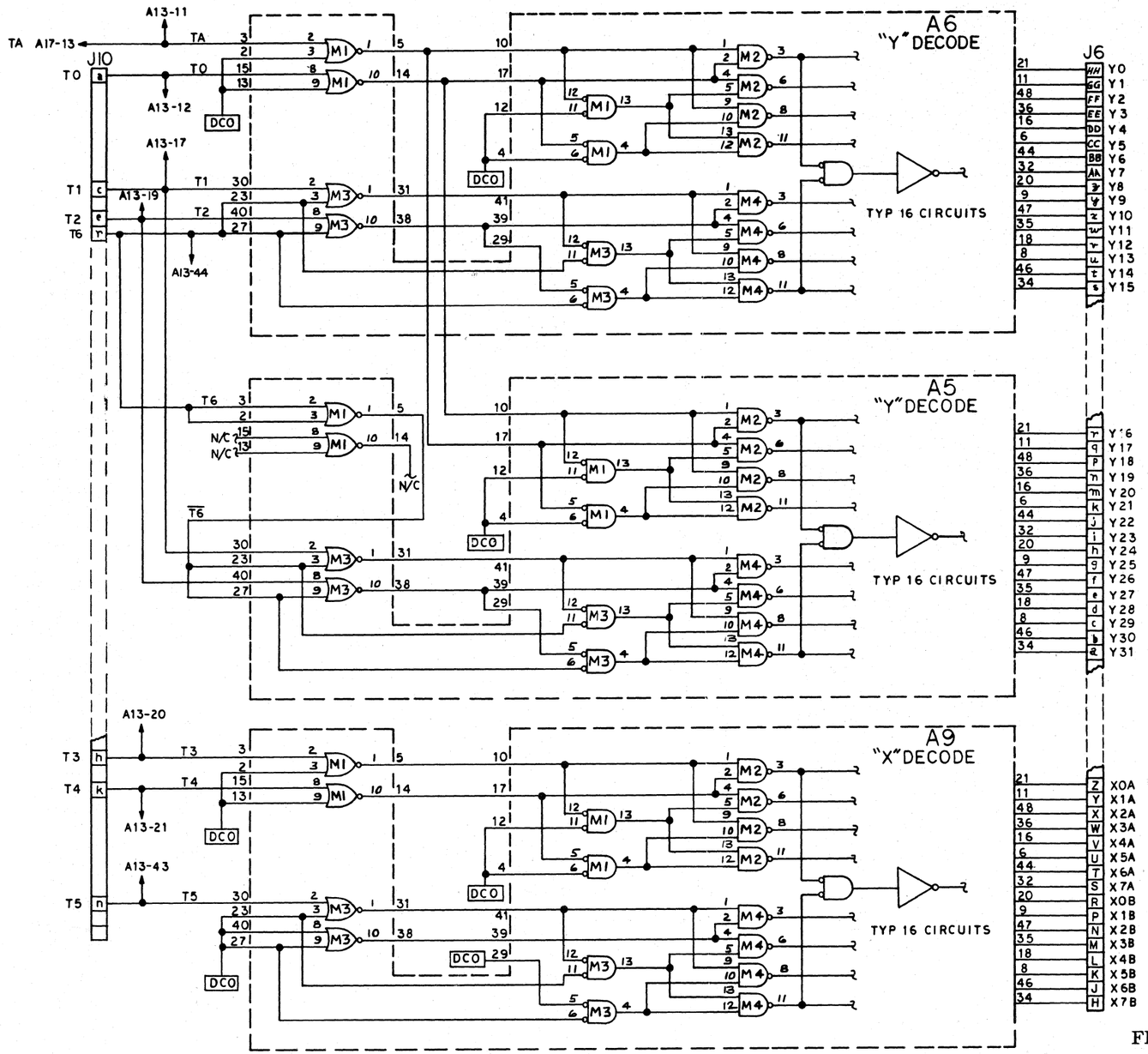


FIGURE 3-24. FUNCTIONAL BLOCK DIAGRAM (SHEET 2 OF 2)

NOTE:

1. This Functional Block Diagram applies to both Part No. 13770 and Part No. 13870, except "Y" Decode Card A5 is used only on Part No. 13770 units.

MATERIAL	TOLERANCE EXCEPT AS NOTED: X.XX± .03, X.XXX± .010, DEG± 0°15'	NEXT ASSY	SCALE
MACHINED SURFACES		DRAWN Gary Clarke 12/9/68	TITLE FUNCTIONAL BLOCK DIAGRAM
FINISH	HEAT TREAT	CHECKED Ernie 12/9/68	DIGITAL DEVELOPMENT CORPORATION
		APPROVED E.H.B. 12-20-68	DWG NO 2
		ENGR W. Schmidt 12/20/68	

2 FUNCTIONAL BLOCK DIAG.

D D C

SECTION 4
CIRCUIT BOARD SPECIFICATIONS

4.1 INTRODUCTION

Descriptions and specifications of the individual circuit boards installed in the Magnetic Memory System are included in this section as an aid to maintenance. The functional description of the circuit boards containing the integrated circuit logic modules (DIP) is contained in Section 3, Paragraph 3.4. The circuit board descriptions are arranged in numerical order. The respective schematics, assembly drawings, and parts lists for the circuit boards are provided in Section 5. The following list of circuit boards and respective part numbers is provided for reference purposes:

PART NUMBER	CIRCUIT BOARD
11306	Write Amplifier
11640	Delay Circuit
11661	Decode Driver
11791/11874	Clock Generator and Speed Detector
11803	Read Amplifier
11807	Linear Data Preamplifier
11811	Linear Timing Preamplifier
11815	Line Terminator
11818	"X" Amplifier

WRITE AMPLIFIER 11306

This module contains two write amplifiers, one buffer amplifier, and three inverter circuits. The write amplifier consists of three separate circuit functions: (1) Set/reset diode-gated flip-flop designed to form phase-modulated write data from NRZ computer data, its complement, and a two-phase clock; (2) a push-pull current switch, controlled by the flip-flop and used to drive write currents through magnetic read/write heads; (3) a high-current transistor switch designed to remove the source voltage from the write driver to inhibit writing when commanded. The buffer amplifier may be used to drive the disable input in the high-current transistor switch or for other functions that require a non-inverting amplifier. If write protect switches are used as part of the design and a protected track is selected, the write voltage is removed from the write driver. The three inverter circuits have no special function and are used wherever inverter or buffer amplifiers are required.

SPECIFICATIONS

WRITE AMPLIFIER SECTION:

Maximum Operating Frequency: 2.0 MHz

Input Signals:

Data:	TRUE = +3V min. FALSE = +1V max.
	Input current = -10ma @ 0V
	Open circuit voltage = +3V nom.
C1 Input:	TRUE = +3V min. FALSE = +1V max.
	Input current = -10ma @ 0V, for each of two inputs required
	Open circuit voltage = +3V nom.
C2' Toggle Input:	Triggers on falling edge of pulse
	Minimum Pulse Width = 50 ns
	Minimum Amplitude = 6V
Enable Input:	TRUE = +6V min. FALSE = +1V max.
	Open circuit voltage: 7V nom. Input current: -14ma @ 0V

D D C

WRITE AMPLIFIER
11306 (Cont)

SPECIFICATIONS
(Cont)

Disable Input:	TRUE = +18V or open FALSE = +1V max.
	Input current = -10ma @ 0V
Output Signals:	Push-pull
	Output to head = 150ma max.
Rise/Fall Time:	100 ns min., into 10 μH nominal head load
Propagation Delay:	75 ns max.

INVERTER SECTION:

Input Signals:	TRUE = +3V min. FALSE = +1V max.
Output Signals:	TRUE = 7.5V ±0.5V @ 8ma FALSE = 0.5V max. @ -65ma
Input Current:	-10ma @ 0V
Rise/Fall Time:	15 ns typical
Propagation Delay:	25 ns nominal

BUFFER SECTION:

Input Signals:	TRUE = +3V min. FALSE = +1V max.
Output Signals:	OFF = +18V, no load ON = +1V @ 100ma
Input Current:	-10ma @ 0V
Rise/Fall Time:	25 ns typical, dependent on load
Propagation Delay:	50 ns

D D C

WRITE AMPLIFIER 11306 (Cont)

SPECIFICATIONS (Cont)

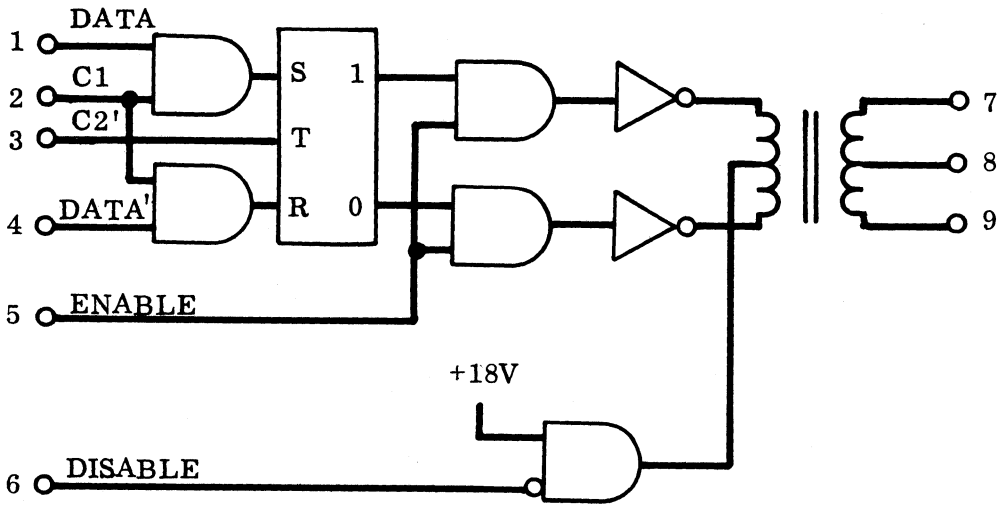
MODULE POWER REQUIREMENTS: +18V @ 500ma
-12V @ 25ma

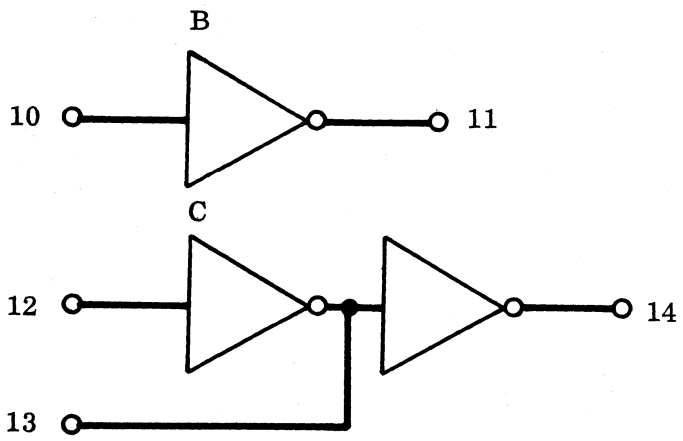
CONNECTIONS:

Circuit Ref. Point	Circuit Pin Numbers A	B	C
1	4	29	-
2	3	30	-
3	10	35	-
4	23	49	-
5	13	39	-
6	12	38	-
7	15	41	-
8	14	40	-
9	11	36	-
10	5	31	45
11	9	34	42
12	19		-
13	16		-
14	17		-

D D
C

WRITE AMPLIFIER
11306 (Cont)





NOTE: Ref. 13 (pin 16) provides access directly to base of second inverter for special control applications.

WRITE AMPLIFIER FUNCTIONAL SCHEMATIC

DELAY CIRCUIT
11640

This module contains one delay line driver circuit, one delay line, eight tap amplifier circuits, and one inverter circuit. The delay circuit is used to derive the read strobe clock from one phase of the two-phase write clock. The delay line has a total delay of 250 ns and is tapped every 12.5 ns. Each tap amplifier may be connected to any tap of the delay line. The inverter has no special function and is used wherever an inverter or buffer is required.

SPECIFICATIONS

DELAY LINE DRIVER CIRCUIT:

Maximum Operating Frequency: 5 MHz

Input Signals: TRUE = +3V min.
FALSE = +1V max.

Input Current: -8ma max. @ 0V

Minimum Pulse Width: 50 ns

Output Drive Capacity: Delay line with tap amplifiers

TAP AMPLIFIER:

Maximum Operating Frequency: 5 MHz

Input Signals: Delay line tap output

Output Signals: 4.3V ±0.5V @ 8ma
+0.5V max. @ -65ma

Rise/Fall Time: 15 ns max.

Driver/Amplifier Propagation Delay: Delay line setting +50 ns nominal

INVERTER CIRCUIT:

Input Signals: TRUE = +3V min.
FALSE = +1V max.

Output Signals: 4.3V ±0.5V @ 8ma
+0.5V max. @ -65ma

D D C

SECTION 5
MAINTENANCE

5.1 INTRODUCTION

This section includes preventive maintenance instructions, corrective maintenance, troubleshooting, and component replacement procedures.

> **CAUTION**
>
> DO NOT run the disc system with the cover removed. Serious damage may result by allowing unit to operate in a contaminated environment.

5.2 PREVENTIVE MAINTENANCE

Preventive maintenance for the Magnetic Memory System consists of checking the environmental gas system pressure gauges at regular intervals and replacing the sustaining helium gas bottle as required.

5.2.1 HELIUM BOTTLE REPLACEMENT

Under ordinary conditions, the helium bottle which supplies the sealed enclosure should last approximately six months. The helium bottle should be replaced before reaching a level of 300 psi, while a small amount of pressure remains in the system. New bottle pressure is approximately 2100 to 2200 psi. Use highest-grade, oil-free helium with a purity of at least 99.995% (Liquid Carbonic Specification L-114 Atomic Grade, or equivalent). It is not necessary to purge the system when replacing the helium bottle unless the cover has been opened. To replace the helium bottle while system is in operation, proceed as follows:

> **CAUTION**
>
> In the following steps, take care not to disturb the setting of the two stage regulator (Figure 3-2) except as indicated.

1. Shut off main valve on helium bottle (turn fully clockwise).

2. Disconnect either end of tube between low pressure gauge and enclosure inlet fitting (Figure 3-2).

3. Unfasten encircling clamp that supports helium bottle and pull bottle away from unit.

4. Disconnect depleted bottle from regulator and connect full bottle.

5. Clamp helium bottle into place and reconnect tube.

6. Open main valve on helium bottle (turn fully counterclockwise).

D D C

CAUTION

Do not attempt to set regulator while system is hot. Thermal expansions will cause an improper setting which may result in damage to the unit.

7. Monitor high pressure gauge (Figure 3-2) for 10 minutes. If pressure is dropping, omit steps 8 and 9 and go to step 10.

8. If high pressure is stable, write down reading of low pressure gauge, then manually actuate pressure relief valve located on baseplate until low pressure gauge indicates 0.

9. Release pressure relief valve and monitor low pressure gauge for 10 minutes. If pressure does not return to reading in step 8, readjust regulator (step 10).

10. If helium flow is correct, omit steps 10 through 15 and go to step 16. If helium flow is too fast (high pressure dropping) or too slow (internal pressure cannot be recovered within 10 minutes), shut off regulator by loosening locknut and turning T-handle two or more full turns counterclockwise. Manually actuate pressure relief valve until low pressure gauge indicates 0.

11. Remove power from unit and allow to cool down for at least three hours.

12. When the unit is at room temperature, slowly turn T-handle valve on regulator clockwise until pressure gauge needle just moves off 0 psi pin stop. This prevents excessive pressure from entering the cover.

13. Adjust regulator slowly until gauge indicates between 1/4 and 1/2 psi. If gauge indicates more than 1/2 psi, reverse T-handle slightly and discharge some of the gas within the cover by manually actuating pressure relief valve. Repeat the adjust-discharge sequence until gauge indicates between 1/4 and 1/2 psi.

14. Tighten locknut of T-handle valve.

15. Monitor low pressure gauge for ten minutes and verify that pressure remains less than 1/2 psi. If necessary, loosen locknut and repeat steps 12 through 14 until pressure remains less than 1/2 psi.

16. Monitor the high pressure gauge each week and maintain a log of helium usage.

5.2.2 SYSTEM PURGING

The sealed enclosure must be purged each time the cover is opened. Purging is accomplished by allowing gas to flow through the system until contaminated helium is expelled from under the cover. A K-size cylinder of gas can be used for this purpose, but a small container (type B medical cylinder) may be more convenient. It is recommended that an extra regulator be used for

purging to eliminate resetting the system regulator. To purge the sealed enclosure, proceed as follows:

> **CAUTION**
>
> The unit must be shut off and allowed to cool down at least three hours prior to purging.

1. When the unit is at room temperature, replace cover and install the 12 cap screws. Torque each cap screw in 5-inch-pound steps until all screws are at 18-inch-pounds. This torquing procedure is necessary to obtain a proper seal.

2. Install purging bottle per helium bottle replacement procedure.

> **CAUTION**
>
> Do not exceed 3 psi when purging, or damage to the unit may result.

3. Open valve of purging bottle and adjust regulator to approximately 2-1/2 psi. The relief valve in baseplate assembly will open at 2 psi. If a type B medical cylinder is used for purging, it will be necessary to use entire contents for purging. If a K-size bottle of helium is used, a reduction of 200 psi in the bottle will indicate that a sufficient purge has been completed.

4. After purging, shut off regulator by loosening locknut and turning T-handle two full turns counterclockwise. Replace purging bottle with sustaining bottle per helium bottle replacement procedure.

5.3 CORRECTIVE MAINTENANCE

5.3.1 PRESSURE SWITCH ASSEMBLY ADJUSTMENTS

The pressure switch assembly contains an expanding bellows that comes in contact with three microswitches. Two of these switches exercise control over the actuation pressure. The "L" switch provides an indication that actuation pressure is less than 1.5 psi, indicating the system is in a "ready" condition. The "A" switch stops pump action when pressure reaches 1-5/8 psi, and the "H" switch opens the dump valve when pressure exceeds 1-3/4 psi. These pressure switch settings can be adjusted manually as follows:

5.3.1.1 INITIAL SETUP ADJUSTMENTS.

1. Shut off power and remove cover.

2. Wrap 1-1/2 turns of teflon plumbers tape (one-mil thick) around threads of 0-3 psi Marshaltown pressure gauge and install pressure gauge in manifold block.

3. Open valve on manifold block.

4. Carefully disconnect pressure line from manifold block to the manifold, taking care not to stress or bend manifold inlet. Place teflon plumbers tape over exposed end of manifold inlet to prevent particules from entering pressure system.

5. Install stop plug over dump valve outlet. (Make sure the stop plug is removed from the dump valve after adjustments are complete.)

6. Assemble a helium bottle, regulator, and an extended purging line with appropriate swagelok fittings that will mate with regulator and swagelok fittings on manifold block.

7. Connect purging line to the open outlet on manifold block.

8. Rotate T-handle on regulator counterclockwise at least two full turns. The regulator must be off to ensure that a sudden rush of gas will not rupture diaphragm on pressure switch assembly.

5.3.1.2 LOW PRESSURE SWITCH SETTING

1. Disconnect connector P12 on baseplate.

2. Connect an ohmmeter between pins A and B of JT2.

CAUTION

Do not exceed 2 psi at any time during the switch setting procedure.

3. Rotate regulator slowly clockwise until a pressure of 1-1/2 psi is indicated on the Marshaltown 0-3 psi gauge installed on the manifold block.

4. Note that contact closure between pins A and B, as obser on ohmmeter, occurs at 1-1/2 psi. If it does not, adjust slotted s (identified "L") on pressure switch assembly to obtain proper contact closure. Clockwise rotation will cause switch to close at a lower pressure. Counterclockwise rotation will cause the switch to close at a higher pressure.

D D
C

SECTION 6

ENGINEERING DRAWINGS AND PARTS LISTS

6.1 INTRODUCTION

This section provides applicable engineering drawings and parts lists for reference during routine maintenance operations or troubleshooting of the Model 7301 (Part No. 13870) or Model 7302 (Part No. 13770) Magnetic Memory System.

Representative engineering drawings for the Magnetic Memory System are provided in this section. Appropriate notes have been added to the drawings to define any differences between Part No. 13770 and Part No. 13870 systems. Drawing or part numbers which are unique to a particular system are listed in Table 6-1.

TABLE 6-1. DIFFERENCE DATA

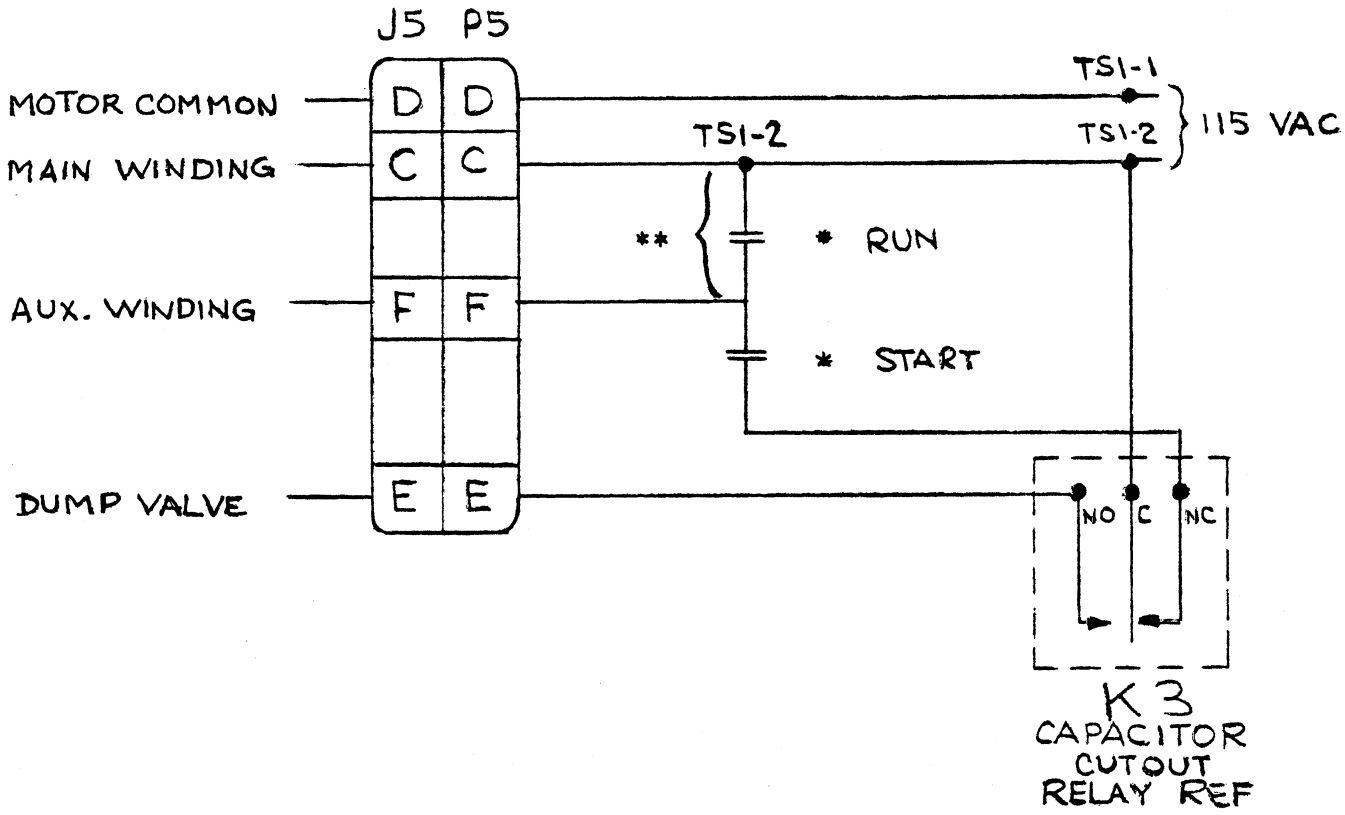
Drawing Title	Applicable Drawing No. Part No. 13770	Part No. 13870
Memory System Installation Assembly	13770	13870
Functional Block Diagram	13777	13882
Relay Mounting Board Assembly	13833	13884

D D
C

6.2 INDEX

The following reference drawings and parts lists are provided in this section in the order listed.

Drawing No.	Title
13834	Drum Wiring and X-Y Harness List (9 sheets)
13775	Card Rack Wire List (27 sheets)
13770/13870	Memory System Installation Assembly (3 sheets)
13777/13882	Functional Block Diagram (2 sheets)
13779	Timing Diagram (4 sheets)
13774	Card Location Diagram
14011	Headplate Organization
13833/13884	Relay Mounting Board Assembly (2 sheets)
11795	Parts List, Interface No. 1
11796/11797	Interface No. 1, Pictorial/Schematic
11799	Parts List, Interface No. 2
11800/11801	Interface No. 2, Pictorial/Schematic
11791	Parts List, Clock Generator (60 Hz)
11874	Parts List, Clock Generator (50 Hz)
11792/11793	Clock Generator, Pictorial/Schematic
11803	Parts List, Read Amplifier
11804/11805	Read Amplifier, Pictorial/Schematic
11306	Parts List, Write Amplifier (2 sheets)
11326/11336	Write Amplifier, Pictorial/Schematic
11661	Parts List, Decode Driver (2 sheets)
11662/11663	Decode Driver, Pictorial/Schematic



NOTES:

1) * See MDL for Capacitor Values,
2) Use 16 Ga. white Teflon, Stranded wire.
3) ** Omit this Capacitor on 1 & 2 Disc Units.

DIGITAL EQUIPMENT CORPORATION	DRUM WIRING	CONNECTION OF MOTOR CAPACITORS	
		1	13834
		Page 9	

Page	Rev	Page	Rev
1	H	21	
2	H	22	
3	G	23	
4		24	B
5		25	B
6		26	D
7	D	27	F
8	E		
9			
10			
11	B		
12	B		
13	B		
14			
15	H		
16			
17	G		
18	G		
19	B		
20	F		

Rev.	ALTERATION	By	Date
A	Revisions made to Page 1, 7, 8, 13, 15, 17, 18 and 24. E.B.	Eade	11/9/68
B	**Updated logic changes and corrected errors**	DVA	11/9/68
		Eade	12/9/68
		DVA	12/16
C	Page 27, Pin DD added connection from J2-H, AC Failure Warning		
	Per ECR #766	Eade	1/9/69
		DVA	1/7/69
D	Deleted wire P8-N to A5-24	Eade	1/15/69
	PER ECR 740	DVA	1/16/69
E	**Pin 23 Function should be T6 input is (T6)' (page 8)**		1/21/69
	PER ECR #800	Eade	1/21/69
		DVA	1/27/69
F	**Chg'd. sheets 15, 18, 20 & 27 per ECR 819** Jackson 2-4 9	Eade	2/5/69
			2/11/69

DRAWN Eade	11/23/68	RACK WIRE LIST	DIGITAL EQUIPMENT CORPORATION
TRACED Eade	12/5/68		
DESIGNED DVA	10/25/68		SIZE 1 · DWG NO. 13775 · REV H
APPROVED			

REV	ALTERATION	BY	DATE
G	Changed sheets 3, 17 and 18 per ECR 1409 PC 5/3/9	DVL	5/3/69
H	**Page 15 changed function column on lines 18, 30, 25 and 12 Per ECR 1311 PC 5-29-69 Incorporated ECN 719**	Eade DVL	6/2/69 6/3/69

DRAWN CEDASON	DATE 5-3-9	REVISION SHEET	DIGITAL DDC DEVELOPMENT CORPORATION
CHECKED		RACK WIRE LIST	
APPROVED			
APPROVED			

SHT NO	DWG NO	REV
1	13775	H

Form No. 026

NOTES:

1. See DDC 13775 Sheet 1, pages 24 through 27, for Connector Wiring.

2. Socket to socket wiring to be No. 24 ga. Kynar solid wire.

3. Install DDC #12888-13 Power Bus between Pins 24 and 28 of Connectors A1 thru A13.

4. Install DDC #14023-4 Power Bus on Pin 26 of Connectors A15 thru A18.

Terminal	From	To	Function
1			D C Common
2			
3			
4	P8-H (B)		Read Data "A" Input
5			
6	P8-J (S)	*	Shield
7			
8	P8-G (W)		Read Data "A" Input
9			
10			
11			
12			
13			
14	P8-L (B)		Read Data "B" Input
15			
16	P8-M (S)	*	Shield
17			
18	P8-K (W)		Read Data "B" Input
19			
20			
21			
22	A16-40 ***		Data "B" Output
23	A16-42 ***		Data "A" Output
24	** Sleeve		+18 VDC
25			
26	A13-32		+5 VDC
27			
28	** Sleeve		-12 VDC
29			Clock Data Output
30	A15-8 ***		Clock Data Output
31	A16-30 ***		Timing Data Output
32			
33			
34	P8-D (W)		Timing Read Input
35			
36	P8-F (S)	*	Shield
37			
38	P8-E (B)		Timing Read Input
39			
40			
41			
42			
43			
44	P8-A (W)		Clock Read Input
45			
46	P8-C (S)	*	Shield
47			
48	P8-B (B)		Clock Read Input
49			
50			
51			D C Common

* Shielded twisted pair 24 ga.

** INSULATE ENTIRE PIN TO BUS BAR WITH SHRINK TUBING

*** B & W Twisted Pair, Black to DC Common

***Route outside pin area

Location: A1
Card Type:
Read Ampl.

DIGITAL D/B/C DEVELOPMENT CORPORATION

TITLE: WIRE LIST - CARD RACK

SHT NO: 1 | DWG NO: 13775 | REV: G

FORM NO C64

Terminal	From	To	Function
1			
2			
3			
4			
5			
6			
7			
8			
9			
10			
11			
12			
13			
14			
15			
16			
17			
18			
19			
20			
21			
22			
23			
24			
25			
26			
27			
28			
29			
30			
31			
32			
33			
34			
35			
36			
37			
38			
39			
40			
41			
42			
43			
44			
45			
46			
47			
48			
49			
50			
51			

Location: A12
Card Type:
No card required

DIGITAL DDC DEVELOPMENT CORPORATION

TITLE: WIRE LIST - CARD RACK

SHT. NO: 1 | DWG. NO: 13775 | REV:

Terminal	From	To	Function
1			D C Common
2			
3			
4			
5	J10-M *	A18-39	Data Write
6			
7	J10-K *	A17-46	Head Change
8	J10-U *	A17-36	Read
9	J10-S *	A17-48	Write
10			
11	A17-13	A6-3	TA Address
12	J10-a *	A6-15	T0 Address
13			
14			
15			
16			
17	J10-c *	A6-30	T1 Address
18			-12 VDC Monitor
19	J10-e *	A6-40	T2 Address
20	J10-h *	A9-3	T3 Address
21	J10-k *	A9-15	T4 Address
22			
23			
24	A11-24	A15-24	+18 VDC
25			
26			
27		A10-16	+ V Mon
28			-12V
29			
30			
31			+5VDC Monitor
32		A1-26	+5 VDC
33		A10-19	-12 VDC Monitor
34			
35			
36			
37			
38			
39			
40	A17-49		Memory Ready Terminator
41			
42			
43	J10-n *	A9-30	T5 Address
44	J10-r *	A5-2	T6 Address
45			
46			
47			
48			
49	A15-26 P3-E		+5v Source for Ready
50			
51			D C Common

* Twisted pair 24 ga. Black to DC0

Location: A13
Card Type: Line Terminator

DIGITAL DEVELOPMENT CORPORATION

TITLE: WIRE LIST - CARD RACK

SHT NO: 1 | DWG NO: 13775 | REV: H

Terminal	From	To	Function
1			
2			
3			
4			
5			
6			
7			
8			
9			
10			
11			
12			
13			
14			
15			
16			
17			
18			
19			
20			
21			
22			
23			
24			
25			
26			
27			
28			
29			
30			
31			
32			
33			
34			
35			
36			
37			
38			
39			
40			
41			
42			
43			
44			
45			
46			
47			
48			
49			
50			
51			

Location: A14
Card Type:
No card required

DIGITAL D/D DEVELOPMENT CORPORATION

TITLE
WIRE LIST - CARD RACK

SHT. NO	DWG. NO.	REV
1	13775	

Terminal	From	To	Function
1			D C Common
2	A16-24	A11-14	Early Strobe
3			
4			
5			
6	A17-3		Ready
7			
8	A1-30 *		Clock
9	J10-FF *		(Ready)'
10			
11			
12			
13			
14			
15			
16			(C2)' (not used)
17			
18	A16-46		C1
19			
20			
21			Disc Sp. Ready Test Point
22			
23		P3-G (B) } *	Disc Speed Ready
24	A13-24	P3-F (W) }	+18V
25			
26	Insulate with sleeve	A13-48	+5 VDC
27			
28			
29			
30			
31			
32	A16-8		(Read Inhibit)'
33	A17-39		Read Inhibit
34			
35	P3-C *		Disc Speed Mark
36	J10-C *	A10-31	C2
37			(C2)'
38	A16-33	A10-45	(C1)'
39	A16-34		(C2)'
40			
41			
42			
43			
44			
45			
46			
47			
48			
49			
50			
51			D C Common

* Twisted pair 24 ga. B & W
Black wire to DC0 except where specified

Location: A15
Card Type:
Clock Generator

DIGITAL D/C DEVELOPMENT CORPORATION

TITLE: WIRE LIST - CARD RACK

SHT NO: 1 | DWG NO: 13775 | REV: G

Terminal	From	To	Function
1			D C Common
2	J10-W *		(Sector Clock)'
3			
4	A17-37		(Sector Clock)'
5			Shift Reg. "G"
6	A17-20		Shift Reg. "F"
7			Shift Reg. "E"
8		A15-32	(Read Inhibit)'
9			
10	A18-45		Window
11			
12	A17-19		Shift Register "H"
13			
14			
15			
16			
17			
18			
19			
20			
21			
22	A18-47		(Window)
23	A17-15		(Index)'
24		A15-2	Early Strobe
25			
26		A18-26	+5 VDC
27			
28			
29			
30		A1-31 *	Timing Read Amp Output
31	J10-Y *		(Read/Write Clock)'
32	A17-17		R W A
33	A17-12	A15-38	(C1)'
34	A17-10	A15-39	(C2)'
35			
36			
37			
38			Early Strobe
39			
40	A18-15	A1-22 *	Data "B"
41	A18-8		Strobe "B"
42	A18-25	A1-23 *	Data "A"
43			
44	A18-7		Strobe "A"
45			
46	A17-16	A15-18	C1
47			
48		A18-42	Data Read
49			
50			
51			D C Common

* Twisted Pair 24 ga B & W
Blk Wire to DC0.
Route outside pin area

Location: A16
Card Type:
Interface #1

DIGITAL DEC DEVELOPMENT CORPORATION

TITLE: WIRE LIST - CARD RACK

SHT NO: 1 | DWG NO: 13775 | REV: 5

Terminal	From	To	Function
1			D C Common
2			
3		A15-6	Ready
4			
5		A10-23	(Data Write)' A
6		A10-4	Data Write A
7		A10-49	(Data Write)' B
8		A10-29	Data Write B
9			
10		A16-34	(C2)'
11	A18-41		Gated Data Write
12		A16-33	(C1)'
13		A13-11	Track Address
14	J10-E *		(Origin Pulse)'
15		A16-23	(Index)'
16	J10-A *	A17-16	C1
17	A18-40	A16-32	Read/Write Clock Allow
18			
19		A16-12	Shift Reg. "H"
20		A16-6	Shift Rec. "F"
21			
22	J10-H *		(Read Inhibit)'
23			
24			
25			
26	P3-K Blu 16 ga.		+5 VDC
27			
28			
29		A10-5	Write Enable
30			
31			
32			
33			
34			
35			
36	A13-8		(Read)'
37		A16-4	(Sector Clock)'
38			
39		A15-33	Read Inhibit
40			
41			
42			
43			
44			
45			
46	A13-7		(Head Change)'
47			
48	A13-9		(Write)'
49	P3-H **	A13-40	Memory Ready
50			
51			D C Common

* B & W Twisted Pair, Black to DCO

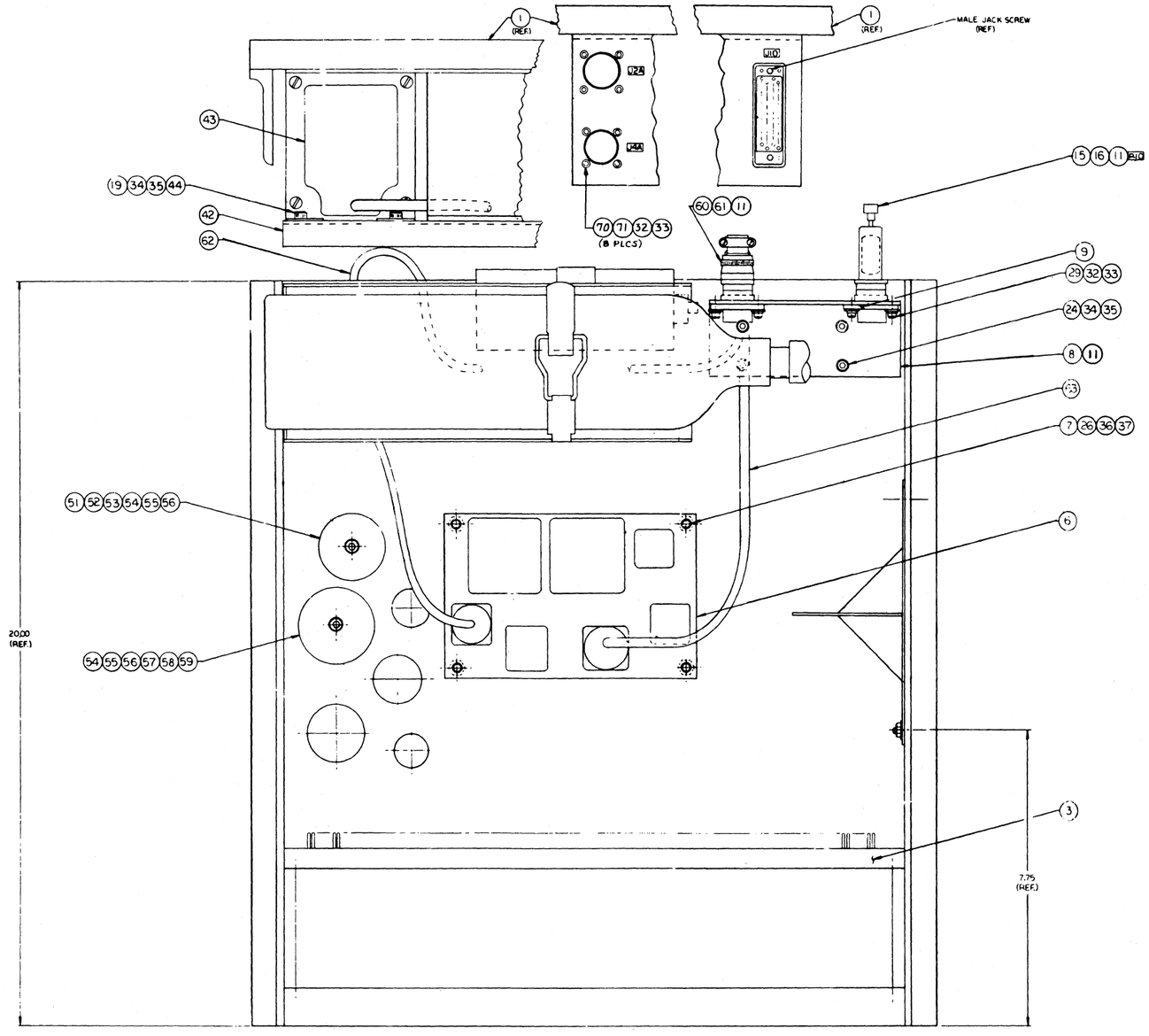
** 24 Ga White

Location: A17
Card Type:
Interface #2

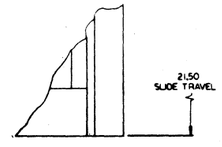
DIGITAL DEVELOPMENT CORPORATION

TITLE: WIRE LIST - CARD RACK

SHT. NO: 1 | DWG. NO: 13775 | REV: B



VIEW **A-A**
ROTATED 180°
ITEMS 18 AND 19
HAVE BEEN OMITTED

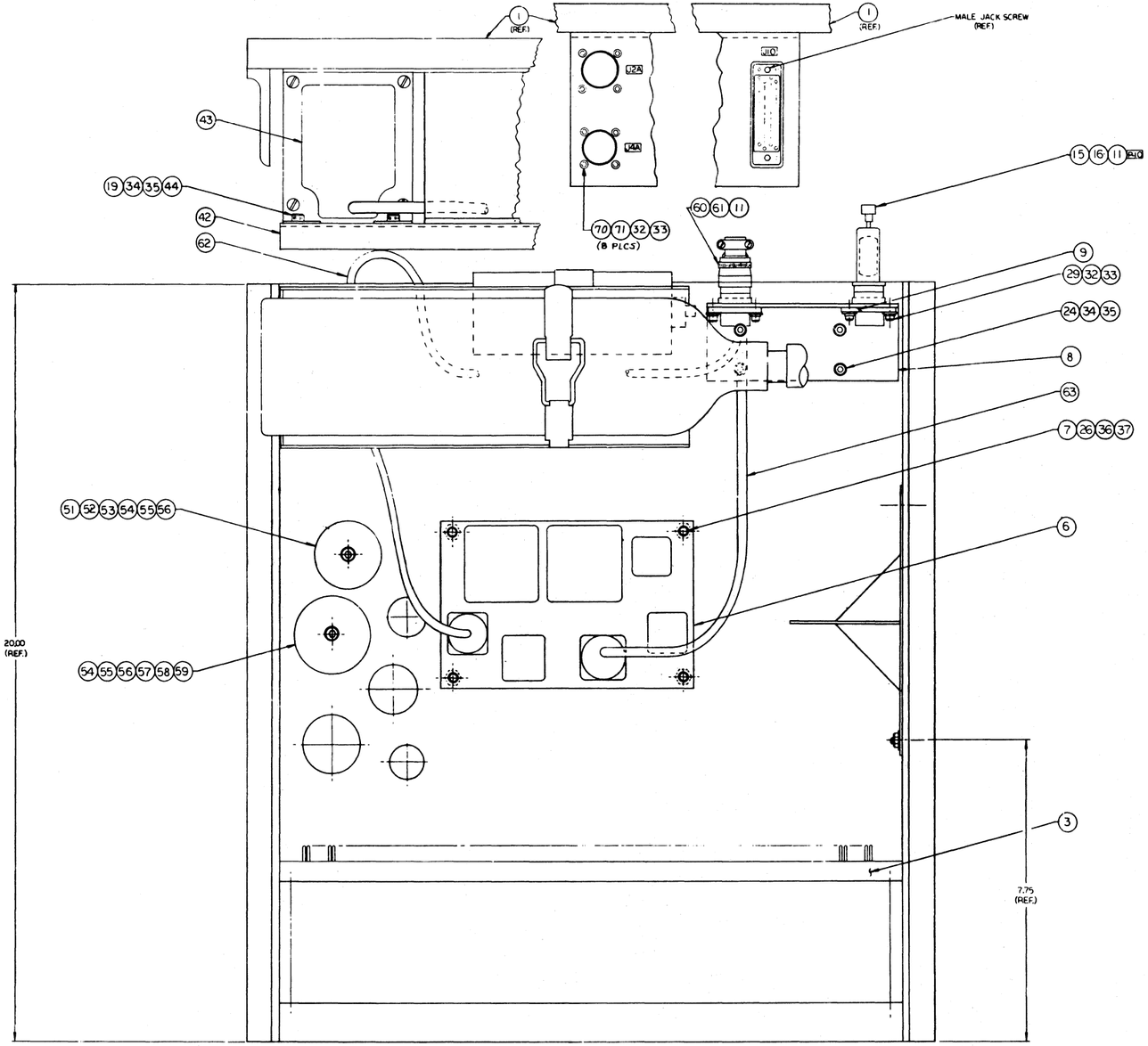


Model 7302, Serial No. 16 and below.
Model 7301, Serial No. 26 and below.

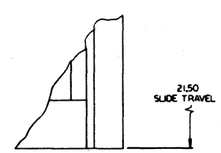
MEMORY SYSTEM

MEMORY SYSTEM INSTALLATION ASSEMBLY

DWG. NO. 13770/13870



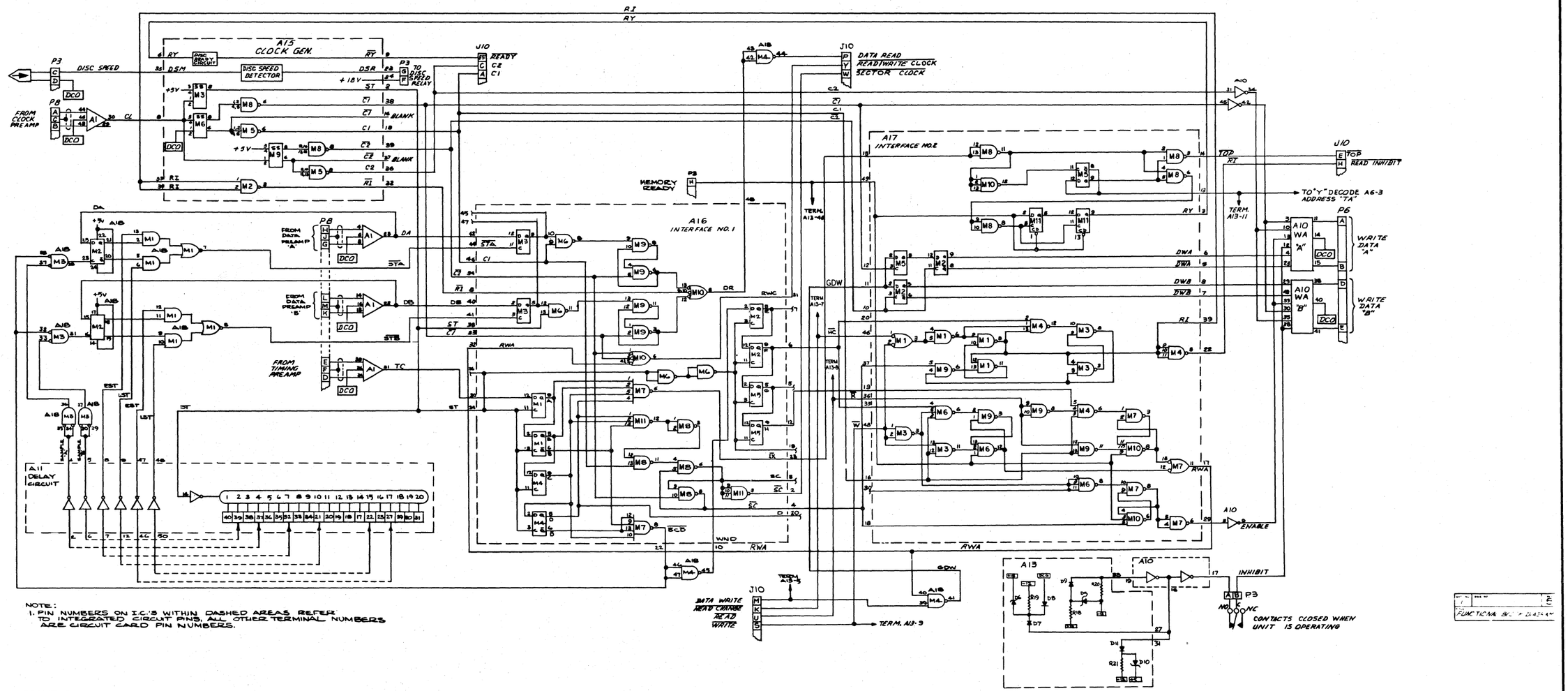
VIEW **A-A**
ROTATED 180°
ITEMS 18 AND 19 HAVE BEEN OMITTED



Model 7302, Serial No. 17 and above.
Model 7301, Serial No. 27 and above.

MEMORY SYSTEM
MEMORY SYSTEM INSTALLATION ASSEMBLY

DWG. NO. 13770/13870



NOTE:

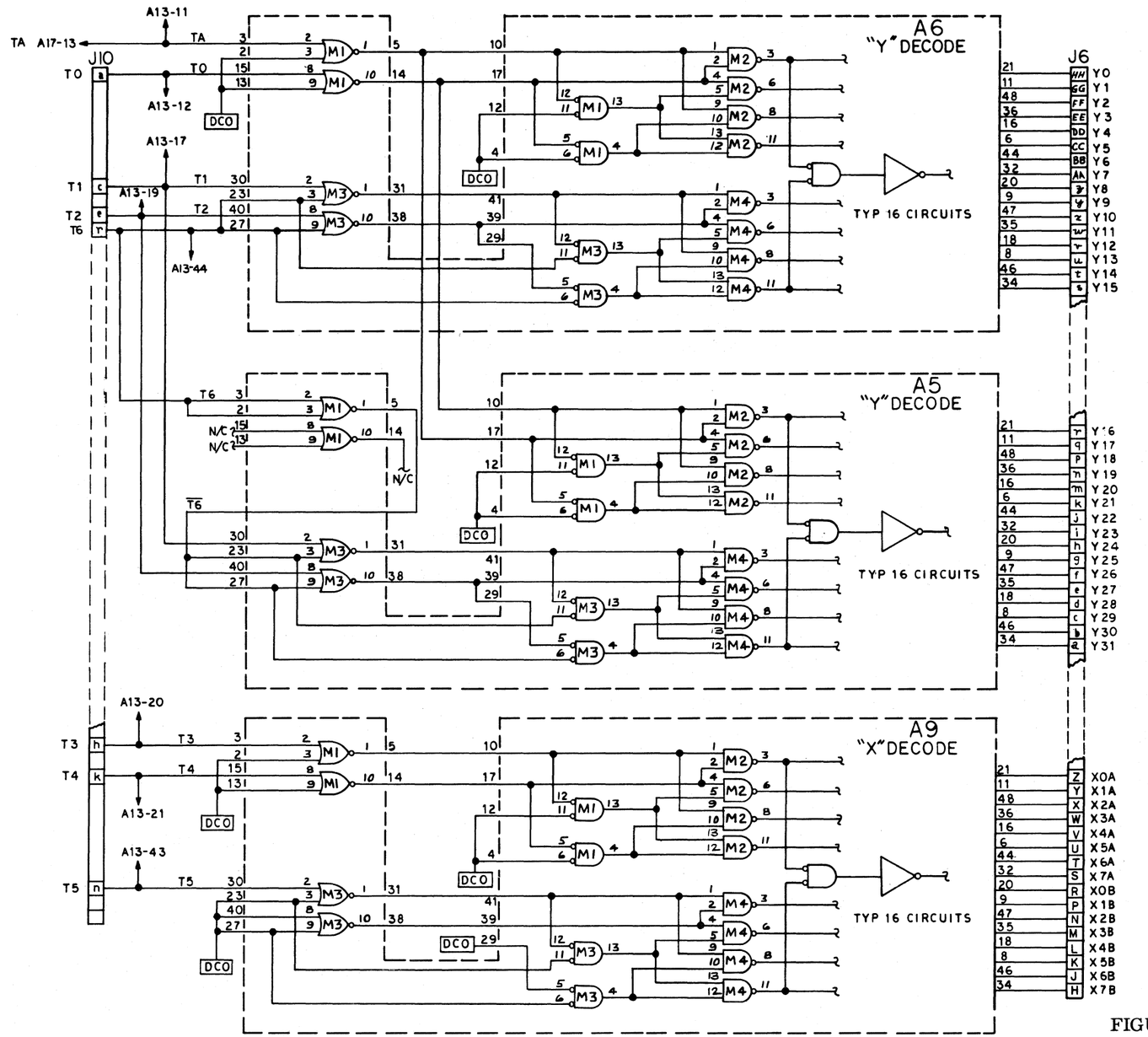
1. Pin numbers on I. C. 's within dashed areas refer to integrated circuit pins. All other terminal numbers are circuit card pin numbers.

FIGURE 3-24. FUNCTIONAL BLOCK DIAGRAM (SHEET 1 OF 2)

DWG. NO. 13777/13882

REV	ALTERATION	BY	DATE
A	SEE SH. 1 Jacks 2-9-9	EVG	2/9/68
	DECODE OUTPUT INVERTER SYMBOL	EVG	2/9/68
	NAS AMPLIFIER PER ECR 738	EVG	2/11/68
B	SEE SHT 1	EVG	3/6/68
C	SEE SHT 1	PC	9/2/69

CM 2-17-69



FUNCTIONAL BLOCK DIAG. 2

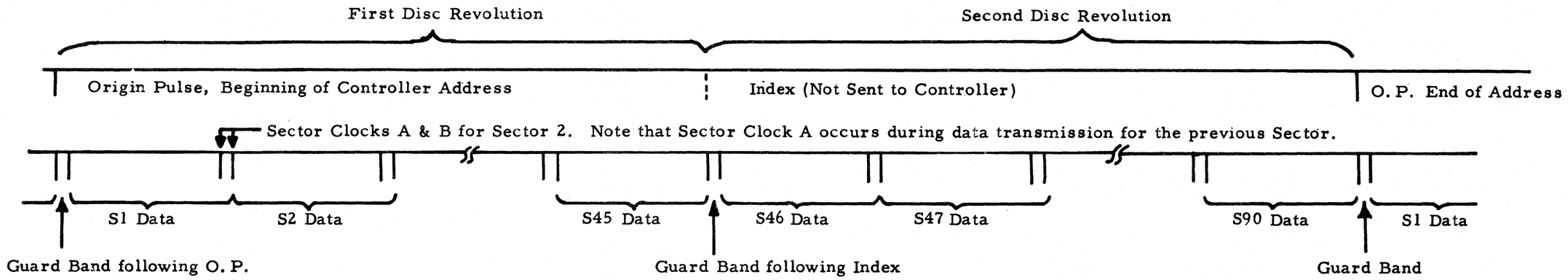
FIGURE 3-24. FUNCTIONAL BLOCK DIAGRAM (SHEET 2 OF 2)

NOTE:

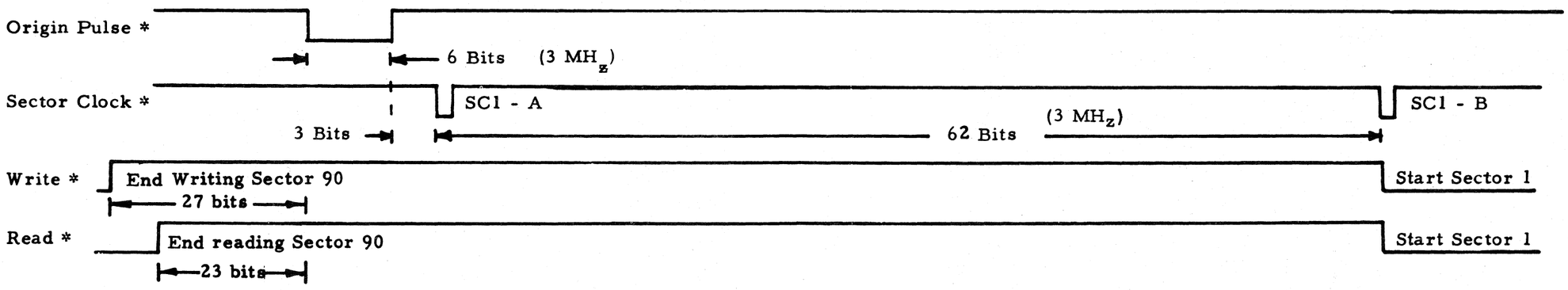
1. This Functional Block Diagram applies to both Part No. 13770 and Part No. 13870, except "Y" Decode Card A5 is used only on Part No. 13770 units.

FUNCTIONAL BLOCK DIAGRAM — DIGITAL EQUIPMENT CORPORATION

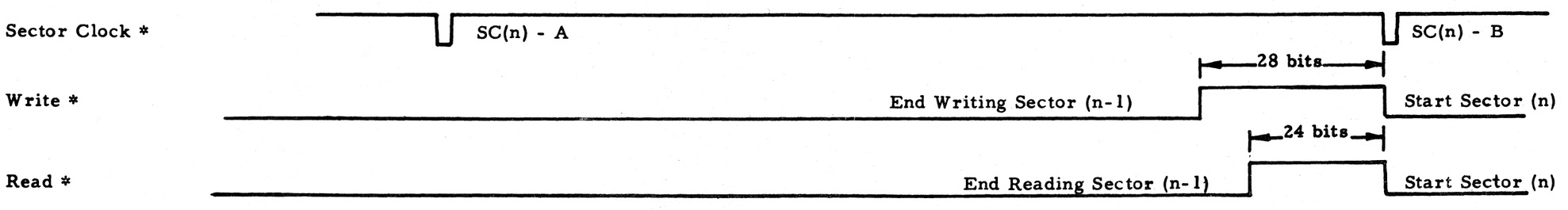
DWG. NO. 13777/13882



TIMING RELATIONSHIPS AT ORIGIN PULSE TIME (Timing at Index is similar)



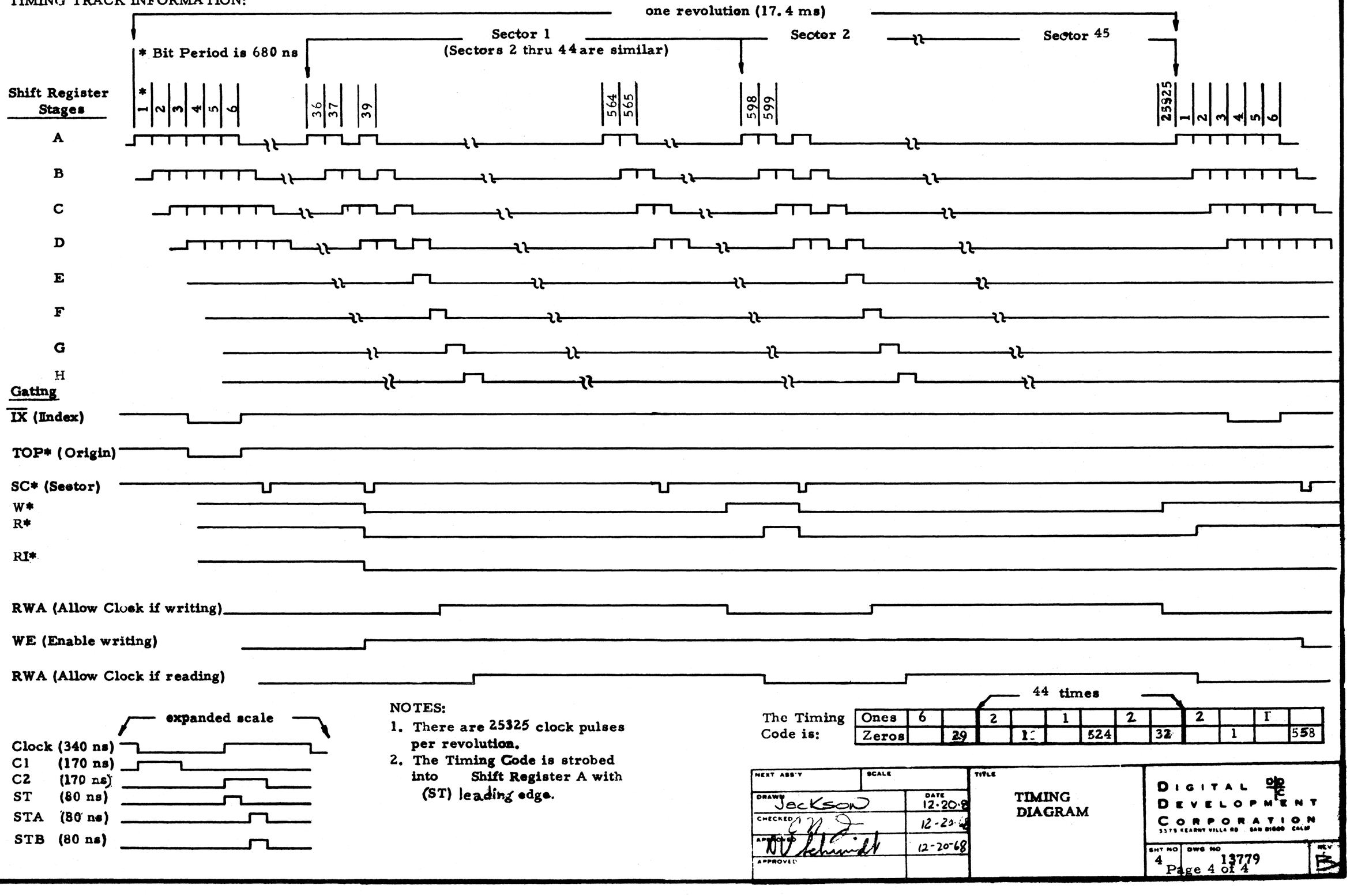
TIMING RELATIONSHIPS AT SECTORS NOT AT O. P. OR INDEX.



DRAWN Jackson	DATE 12·20·8	TITLE TIMING DIAGRAM	DIGITAL DEVELOPMENT CORPORATION 5575 KEARNY VILLA RD SAN DIEGO CALIF
CHECKED			SHT NO 1 · DWG NO 13779 · REV A
APPROVED	12/20/68		
APPROVED			

FORM 007

TIMING TRACK INFORMATION:



NOTES:

1. There are 25325 clock pulses per revolution.
2. The Timing Code is strobed into Shift Register A with (ST) leading edge.

The Timing Code is:

			44 times											
Ones	6		2		1		2		2		I			
Zeros		29		1[illegible]		524		32		1		558		

NEXT ASS'Y	SCALE	TITLE	DIGITAL DEC DEVELOPMENT CORPORATION 3575 KEARNY VILLA RD SAN DIEGO CALIF
DRAWN Jackson	DATE 12-20-8	TIMING DIAGRAM	
CHECKED	12-20-68		SHT NO 4 DWG NO 13779 REV B
APPROVED W Schmidt	12-20-68		
APPROVED			

A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
(not used)	(not used)	(not used)	I.C. Mounting Board 11844	Interface #2 11799	Interface #1 11795	Clock Generator 2	(not used)	Line Terminator 11815	(not used)	Delay Circuit 11640	Write Amplifier 11306	Decode Driver 11661	(Not Used)	(Not Used)	Decode Driver 11661	Decode Driver 11661 1	(not used)	(not used)	(not used)	Read Ampl. 11803

NOTE - CARD INSERTION SIDE SHOWN

REV	ALTERATION	BY	DATE
A	SLOT 7 & 8 WAS 'X'	10/16/68 EB	
	AMPLIFIER 11303	Ede	10/16/68
B	ADDED 11844 I.C.MTG	Ede	11/7/68
	BOARD SLOT A18	AVL	11/20/68
C	ADDED FLAG NOTE 1	Ede	1/21/69
	PER ECR 773	DVL	1/22/69
D	Added polarization to Decode Driver board per ECR 1310 PC 5-23	Ede DVL	6/2/69 6/3/69
E	Added Note 2 Per ECR1196	PC Ede DVL	6/16/69 6/20/69
F	CHANGED WRITE AMP TO 11306 PER ECR 1276 7-PC-9	Ede DVL	7/9/69 7/10/69

CIRCUIT CARD	POLARIZATION
Read Amplifier	Pin 20
Interface Board #2	Pin 40
Interface Board #1	Pin 42
Clock Generator	Pin 32
Line Terminator	Pin 30
Delay Circuit	Pin 12
Decode Matrix	Pin 24
Write Amplifier	Pin 22
X Amplifier	Pin 16
Decode Driver	Pin 14

NOTES:

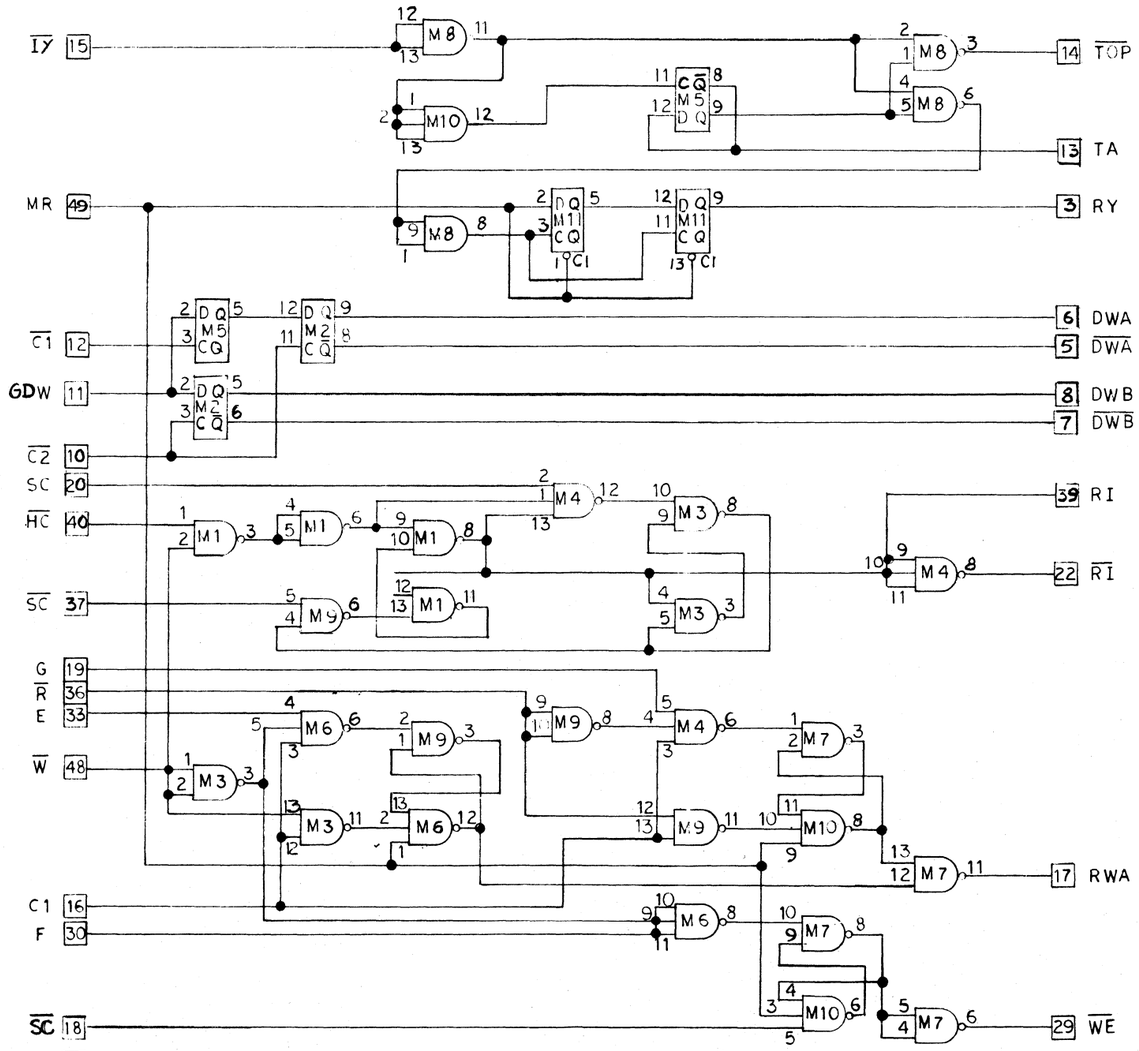
1. Not Used on units of 256 track or smaller capacity.
2. Use 11791 Clock Generator for 60 Hz operation.
   Use 11874 Clock Generator for 50 Hz operation.

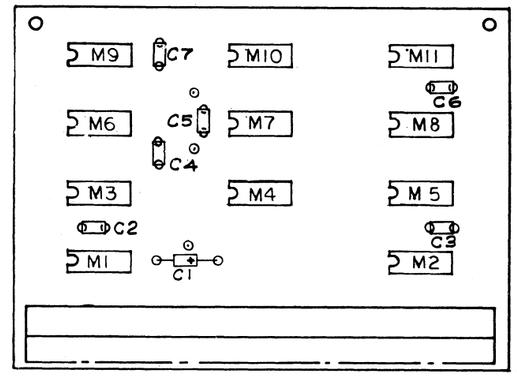
DRAWN Ede	10/3/68	TITLE CARD LOCATIONS
CHECKED E. H. B.	10-4-68	
APPROVED E. H. B.	10-4-68	
APPROVED [signature]	10/24/68	

DIGITAL DEVELOPMENT CORPORATION
1575 KEARNY VILLA RD SAN DIEGO CALIF

SHT NO	DWG NO	REV
1	13774	F

REV	ALTERATION	BY	DATE
A	[illegible]	[illegible]	[illegible]





NOTE -
UNUSED PINS 1, 4, 10 & 13 ON F/F'S M2, M5 & M11 ARE TIED TO +5V

SHT. NO	DWG NO	REV
1		A

TITLE: INTERFACE NO.2

MATERIAL	TOLERANCE EXCEPT AS NOTED	NEXT ASS'Y	SCALE	TITLE
	X.XX± .03		NONE	Pictorial/Schematic Interface No. 2
MACHINED SURFACES	X.XXX± .010	DRAWN [illegible]	DATE [illegible]	
	DEG± 0°15'	CHECKED [illegible]	[illegible]	
FINISH	HEAT TREAT	APPROVED [illegible]	[illegible]	
		APPROVED [illegible]	[illegible]	

DIGITAL DEVELOPMENT CORPORATION

SHT. NO 1 | REV A

DWG. NO. 11800/11801

ITEM	DESCRIPTION	MANUFACTURER	PART NUMBER	QTY
M1,3,4,6,7,9	Integrated Circuit, Monostable Multivibrator	Fairchild	U1A960159X	6
M2	Integrated Circuit Quad-Two Input Gate	DDC	S150	
		or Signetics	N7400A	1
M5,8	Integrated Circuit, Dual-Four Input Buffer	Signetics	N7440A	
		or T.I.	SN7440N	2
Q1	Transistor S201	DDC	S201	1
Q2	Transistor 2N356		2N3565	1
Q3	Transistor S204 or 2N3641	DDC	S204 or 2N3641	1
D2,3,5	Diode S101	DDC	S101	3
D4	Zener Diode 3.6v. 1/2 watt		IN5227	1
C1, 15	Capacitor 390 pf ± 5%	Elmenco	DM-10-391J	2
C2	Capacitor .12μf ± 10% 50v.	Paktron	MPC600-.120-50-K	1
C3	Capacitor .033μf ± 5% 50v.	Paktron	PCR700-.033-50-J	1
C4,5	Capacitor 1μf ± 10% 35v.		CS13BF105K	2
C6-10,14	Capacitor .01μf ± 10%, 100v.		CK06BX103K	6
C11-13	Capacitor 22μf ± 5%	Elmenco	DM-10-220J	3
R10	Resistor 24K ± 5% 1/4 watt		RC07GF243J	1
R1-3,5,6,14	Resistor 510Ω ± 5% 1/4 watt		RC07GF511J	6
R8	Resistor * ± 5% 1/4 watt	RC07GF	RC07GF * J	1
R9	Resistor 866K ± 1% 1/4 watt		RN60D8663F	1
R11	Resistor 39K ± 5% 1/4 watt		RC07GF393J	1
R12	Resistor 22M ± 5% 1/4 watt		RC07GF226J	1
R13	Resistor 330Ω ± 5% 1/4 watt		RC07GF331J	1
R15	Resistor 750Ω ± 5% 1/2 watt		RC20GF751J	1
R16	Resistor 5.1K ± 5% 1/4 watt		RC07GF512J	1
R17, 18	Resitor 10K ± 5% 1/4 watt		RC07GF113J	2
	Connector 51 Pin	Elco	00-7022-051-000-001	1
	* Value to be selected during test.	Model 7302, Serial No. 20 and below		
		Model 7301, Serial No. 38 and below		

VOLTAGES

Pin 26 + 5v.

DETAIL NUMBERS

CIRCUIT CARD 11794

SCHEMATIC 11792

PICTORIAL 11793

		DATE
DRAWN	Eade	12/30/68
CHECKED	EHB	12/30/68
APPROVED	DVS	12/30/68
APPROVED		

TITLE

CLOCK GENERATOR
60 Cycle

DIGITAL DEVELOPMENT CORPORATION

SHT. NO. 1

DRAWING NO. 11791

ITEM	DESCRIPTION	MANUFACTURER	PART NUMBER	QUANTITY
M1, 3, 4, 6, 7, 9	Integrated Circuit, Monostable Multivibrator	Fairchild	U1A960159X	6
M2	Integrated Circuit, Quad-Two Input Nand Gate	DDC	S150	1
		or Signetics	N7400A	
M5, 8	Integrated Circuit, Dual-Four Input Buffer	Signetics	N7440A	2
		or T. I.	SN7440N	
Q1	Transistor S201	DDC	S201	1
Q2	Transistor S204 or 2N3641	DDC	S204	1
		or	2N3641	
D2, 3, 5	Diode S101	DDC	S101	3
D4, 8	Zener Diode 3.6v. ± 5% 1/2 watt		1N5227A	2
D6, 7	Diode S121	DDC	S121	2
D9	Zener Diode 5.1v. ±5% 1/2 watt		1N5231A	1
C1	Capacitor 390 pf ± 5%	Elmenco	DM-10-391J	1
C2, 3	Capacitor .68 µf ± 5%, 100v.	Elpac	Z1R684J	2
		or IMB	XP2B684J	
C4, 5	Capacitor 1 µf ± 10%, 35v.		CS13BF105K	2
C6-10, 14, 15,	Capacitor .01 µf ± 10%, 100v.		CK06BX103K	7
C11-13	Capacitor 22 pf ± 5%	Elmenco	DM-10-220J	3
			Model 7302, Serial No. 21 and above	
			Model 7301, Serial No. 39 and above	

VOLTAGES	DETAIL DRAWINGS		DRAWN	DATE
Pin 26 + 5v.	CIRCUIT CARD	11794	EHB	4.28 9
	SCHEMATIC	11792	CHECKED CERASOLI	4.28 9
	PICTORIAL	11793	APPROVED E. H. B	6-24-69
			APPROVED	

TITLE

CLOCK GENERATOR
and
60 Hz Speed Detector
(160 ns clock)

DIGITAL DEVELOPMENT CORPORATION

SHT. NO.	DRAWING NO.
1/2	11791 I

ITEM	DESCRIPTION	MANUFACTURER	PART NUMBER	QUANTITY
R10	Resistor 33.2K ± 1%, 1/8 watt		RN55D3322F	1
R1-3, 5, 14	Resistor 510 ohms ± 5%, 1/4 watt		RC07GF511J	5
R8	Resistor ***±5%, 1/4 watt		RC07GF***J	1
R8 trim	Resistor **± 5%, 1/4 watt		RC07GF**J	1
R11	Resistor 39K ± 5% 1/4 watt		RC07GF393J	1
R12	Resistor 510 K ± 5% 1/4 watt		RC07GF514J	1
R13	Resistor 330 ohms ± 5% 1/4 watt		RC07GF331J	1
R15	Resistor 750 ohms ± 5%, 1/2 watt		RC20GF751J	1
R16	Resistor 5.1K ± 5%, 1/4 watt		RC07GF512J	1
R17, 18	Resistor 11K ± 5%, 1/4 watt		RC07GF113J	2
R19, 6	Resistor 750 ohms ± 5%, 1/4 watt		RC07GF751J	2
R20, 21, 22, 23	Resistor 27 ohms ± 5%, 1/2 watt		RC20GF270J	4
R24	Resistor 22 ohms ± 5%, 1/2 watt		RC20GF220J	1
	Connector 51 Pin	Elco	00-7022-051-000-001	1
	Model 7302, Serial No. 21 and above Model 7301, Serial No. 39 and above			

* Value may be changed if necessary to achieve proper test results.

** Value to be selected during test. 5.1K max.

*** Value to be selected during test. 15K max.

VOLTAGES

Pin 26 + 5v

DETAIL DRAWINGS

CIRCUIT CARD	11794
SCHEMATIC	11792
PICTORIAL	11793

		DATE
DRAWN	EHB	4-28-9
CHECKED	CERASOLI	4.28.9
APPROVED	E.H.B.	6-24-69
APPROVED		

TITLE

CLOCK GENERATOR
and
60 Hz Speed Detector
(160 ns clock)

DIGITAL DEVELOPMENT CORPORATION

SHT NO 2/2

DRAWING NO. 11791 I

ITEM	DESCRIPTION	MANUFACTURER	PART NUMBER	QUANTITY
M1, 3, 4, 6, 7, 9	Integrated Circuit, Monostable Multivibrator	Fairchild	U1A960159X	6
M2	Integrated Circuit, Quad-Two Input Nand Gate	DDC or Signetics	S150 N7400A	1
M5, 8	Integrated Circuit, Dual-Four Input Buffer	Signetics or T.I.	N7440A SN7440N	2
Q1	Transistor S201	DDC	S201	1
Q2	Transistor S204 or 2N3641	DDC	S204 or 2N3641	1
D2, 3, 5	Diode S101	DDC	S101	3
D4, 8	Zener Diode 3.6v. ± 5% 1/2 watt		1N5227A	2
D6, 7	Diode S121	DDC	S121	2
D9	Zener Diode 5.1v. ±5% 1/2 watt		1N5231A	1
C1	Capacitor 390 pf ± 5%	Elmenco	DM-10-391J	1
C2, 3	Capacitor .68 µf ± 5%, 100v.	Elpac or IMB	Z1R684J XP2B684J	2
C4, 5	Capacitor 1 µf ± 10%, 35v.		CS13BF105K	2
C6-10, 14, 15	Capacitor .01 µf ± 10%, 100v.		CK06BX103K	7
C11-13	Capacitor 22 pf ± 5%	Elmenco	DM-10-220J	3
			Model 7302, Serial No. 28 and above	
			Model 7301, Serial No. 79 and above	

VOLTAGES	DETAIL DRAWINGS		DRAWN	DATE
Pin 26 + 5v.	CIRCUIT CARD	11794	EHB	4.28 9
	SCHEMATIC	11792	CHECKED CERASOLI	4.28 9
	PICTORIAL	11793	APPROVED E. H. B.	6-24-69
			APPROVED	

TITLE

CLOCK GENERATOR and 50 Hz Speed Detector (160 ns clock)

DIGITAL DEVELOPMENT CORPORATION

SHT. NO. 1/2 | DRAWING NO. 11874 D

ITEM	DESCRIPTION	MANUFACTURER	PART NUMBER	QUANTITY
R10	Resistor* 39.2K ± 1%, 1/8 watt		RN55D3922F	1
R1-3, 5, 14	Resistor 510 ohms ± 5%, 1/4 watt		RC07GF511J	5
R8	Resistor ***±5%, 1/4 watt		RC07GF***J	1
R8 trim	Resistor **± 5%, 1/4 watt		RC07GF**J	1
R11	Resistor 39K ± 5% 1/4 watt		RC07GF393J	1
R12	Resistor 510K ± 5% 1/4 watt		RC07GF514J	1
R13	Resistor 330 ohms ± 5% 1/4 watt		RC07GF331J	1
R15	Resistor 750 ohms ± 5%, 1/2 watt		RC20GF751J	1
R16	Resistor 5.1K ± 5%, 1/4 watt		RC07GF512J	1
R17, 18	Resistor 11K ± 5%, 1/4 watt		RC07GF113J	2
R19, 6	Resistor 750 ohms ± 5%, 1/4 watt		RC07GF751J	2
R20, 21, 22, 23	Resistor 27 ohms ± 5%, 1/2 watt		RC20GF270J	4
R24	Resistor 22 ohms ± 5%, 1/2 watt		RC20GF220J	1
	Connector 51 Pin	Elco	00-7022-051-000-001	1
		Model 7302, Serial No. 28 and above		
		Model 7301, Serial No. 79 and above		

* Value may be changed if necessary to achieve proper test results.

** Value to be selected during test. 5.1K max.

*** Value to be selected during test. 15K max.

VOLTAGES: Pin 26 + 5v

DETAIL DRAWINGS

CIRCUIT CARD	11794
SCHEMATIC	11792
PICTORIAL	11793

		DATE
DRAWN	EHB	4.28.9
CHECKED	CERASOLI	4.28.9
APPROVED	E.H.B.	6-24-69
APPROVED		

TITLE: CLOCK GENERATOR and 50 Hz Speed Detector (160 ns clock)

DIGITAL DEVELOPMENT CORPORATION

SHT. NO. 2/2

DRAWING NO. 11874 D

ITEM	DESCRIPTION	MANUFACTURER	PART NUMBER	QUANTITY
M1,3,4,6,7,9	Integrated Circuit, Monostable Multivibrator	Fairchild	U1A960159X	6
M2	Integrated Circuit Quad-Two Input Gate	DDC	S150	
		or Signetics	N7400A	1
M5,8	Integrated Circuit, Dual-Four Input Buffer	Signetics	N7440A	
		or T.I.	SN7440N	2
Q1	Transistor S201	DDC	S201	1
Q2	Transistor 2N356		2N3565	1
Q3	Transistor S204 or 2N3641	DDC	S204 or 2N3641	1
D2,3,5	Diode S101	DDC	S101	3
D4	Zener Diode 3.6v. 1/2 watt		IN5227	1
C1, 15	Capacitor 390 pf ± 5%	Elmenco	DM-10-391J	2
C2	Capacitor .12μf ± 10% 50v.	Paktron	MPC600-120-50-K	1
C3	Capacitor .033μf ± 5% 50v.	Paktron	PCR700-.033-50-J	1
C4,5	Capacitor 1μf ± 10% 35v.		S13BF105K	2
C6-10,14	Capacitor .01μf ± 10%, 100v.		CK06BX103K	6
C11-13	Capacitor 22μf ± 5%	Elmenco	DM-10-220J	3
R10	Resistor 24K ± 5% 1/4 watt		RC07GF243J	1
R1-3,5,6,14	Resistor 510Ω ± 5% 1/4 watt		RC07GF511J	6
R8	Resistor * ± 5% 1/4 watt	RC07GF	RC07GF*J	1
R9	Resistor * ± 5% 1/4 watt		RC07GF*J	1
R11	Resistor 39K ± 5% 1/4 watt		RC07GF393J	1
R12	Resistor 22M ± 5% 1/4 watt		RC07GF226J	1
R13	Resistor 330Ω ± 5% 1/4 watt		RC07GF331J	1
R15	Resistor 750Ω ± 5% 1/2 watt		RC20GF751J	1
R16	Resistor 5.1K ± 5% 1/4 watt		RC07GF512J	1
R17, 18	Resitor 11K ± 5% 1/4 watt		RC07GF113J	2
	Connector 51 Pin	Elco	00-7022-051-000-001	1
	* Value to be selected during test. R8 must be between 5.1K & 39K. R9 must be between 820K and 1.2M.			

VOLTAGES	DETAIL DRAWINGS		DRAWN	DATE
Pin 26 + 5v.	CIRCUIT CARD	11794	Cerasoli	4-7-69
	SCHEMATIC	11792	CHECKED E.A.B.	4-9-69
	PICTORIAL	11793	APPROVED W.V. Schmidt	4/9/69
			APPROVED	

TITLE: CLOCK GENERATOR AND 50 Hz Speed Detector

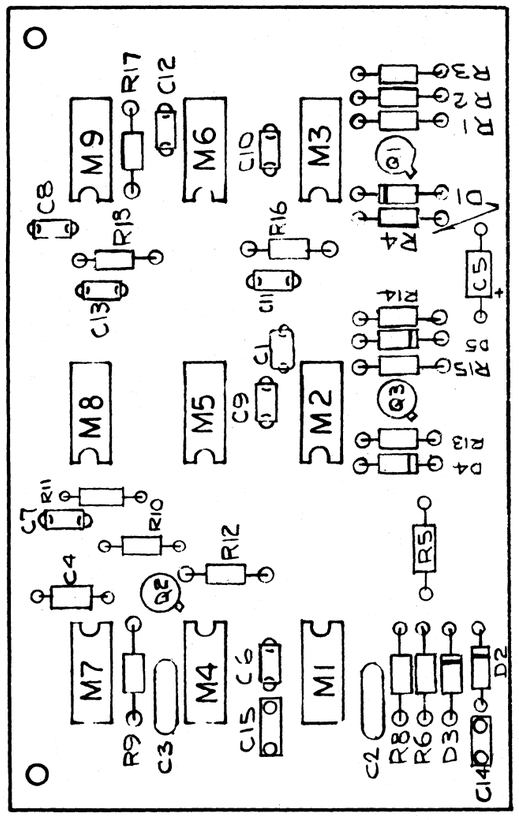
DIGITAL DEVELOPMENT CORPORATION

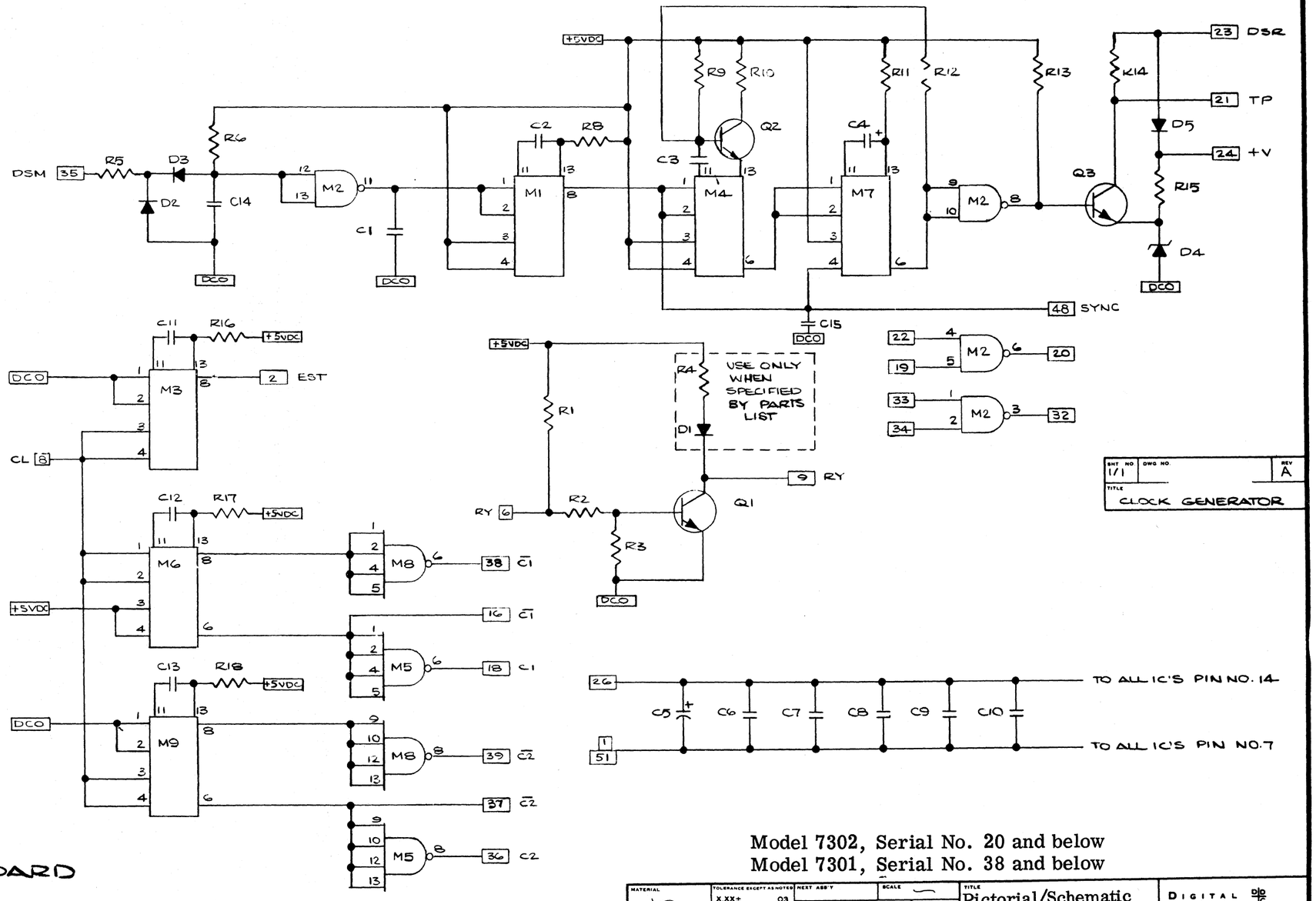
SHT. NO. 1 | DRAWING NO. 11874

Model 7302, Serial No. 27 and below
Model 7301, Serial No. 78 and below

FORM 006

REV	ALTERATION	BY	DATE
A	REVISED PER. ECR 729		1/6/69





1. C4 MOUNTED NEGATIVE TO BOARD

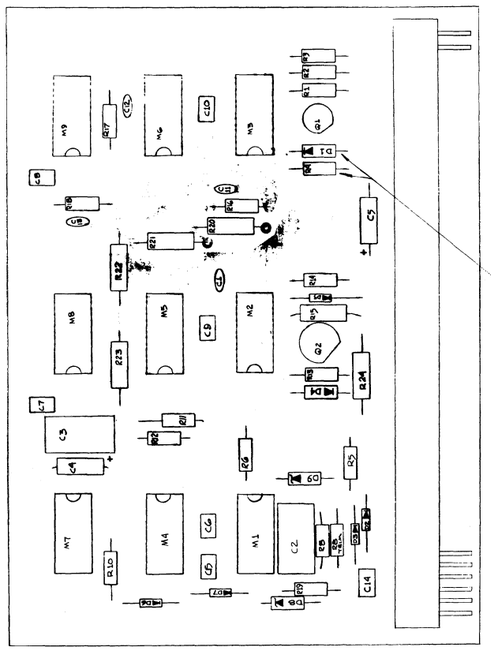
NOTES:

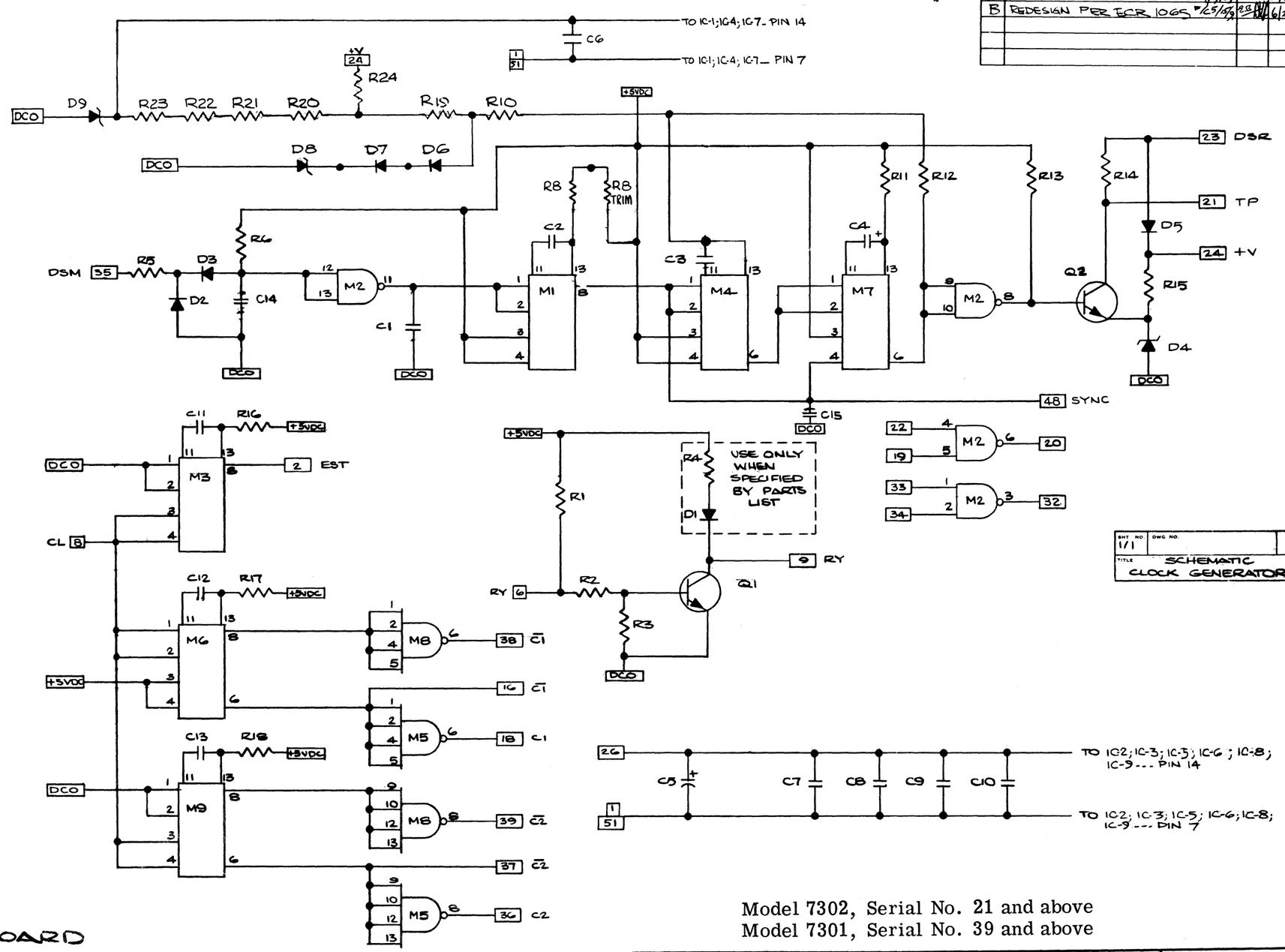
Model 7302, Serial No. 20 and below
Model 7301, Serial No. 38 and below

MATERIAL	TOLERANCE EXCEPT AS NOTED	NEXT ASS'Y	SCALE	TITLE	DIGITAL DEVELOPMENT CORPORATION
	X.XX± .03	DRAWN Jackson	DATE 12-2-68	Pictorial/Schematic Clock Generator	5570 KEARNY VILLA RD. SAN DIEGO, CALIF.
MACHINED SURFACES	X.XXX± .010	CHECKED E.H.B.	12-20-68		SHT. NO. 1/1 DWG NO. REV. A
	DEG± 0°15'	APPROVED	12/30/68		
FINISH	HEAT TREAT	APPROVED			

DWG. NO. 11792/11793

REV	ALTERATION	BY	DATE
A	REVISED PER. ECR 729		1/8/69
B	REDESIGN PER ECR 1065		6/24/69





SHT NO 1/1 | DWG NO. | REV B

TITLE: SCHEMATIC CLOCK GENERATOR

1. C4 MOUNTED NEGATIVE TO BOARD

NOTES:

Model 7302, Serial No. 21 and above
Model 7301, Serial No. 39 and above

MATERIAL ~	TOLERANCE EXCEPT AS NOTED: X.XX± .03; X.XXX± .010; DEG± 0°15'	NEXT ASS'Y	SCALE ~	TITLE: Pictorial/Schematic Clock Generator
MACHINED SURFACES ~	HEAT TREAT ~	DRAWN Jackson	DATE 12.20.68	DIGITAL DEVELOPMENT CORPORATION 3235 KEARNY VILLA RD SAN DIEGO CALIF
FINISH ~		CHECKED E.H.B.	12.20.68	SHT NO 1/1 DWG NO. REV
		APPROVED W. Schmidt	12/20/68	
		APPROVED		

DWG. NO. 11792/11793

ITEM	DESCRIPTION	MANUFACTURER	PART NUMBER	QUANTITY
R1-5,16-20,25,26	Resistor 390 Ohms ± 5% 1/4 W		RC07GF391J	26
R6,7,21,22	Resistor 5.1K Ohms ± 5% 1/4 W		RC07GF512J	8
R8	Resistor 510 Ohms ± 5% 1/4 W		RC07GF511J	1
R9, 27	Resistor 2.4K Ohms ± 5% 1/4 W		RC07GF242J	4
R10,11	Resistor 4.7K Ohms ± 5% 1/4 W		RC07GF472J	2
R12	Resistor 1.2K Ohms ± 5% 1/4 W		RC07GF122J	1
R13	Resistor 1.0K Ohms ± 5% 1/4 W		RC07GF102J	1
R14	Resistor 180 Ohms ± 5% 1/4 W		RC07GF181J	1
R15	Resistor 330 Ohms ± 5% 1/4 W		RC07GF331J	1
R23,24	Resistor 100 Ohms ± 5% 1/2 W		RC20GF101J	2
T1,2	Transformer	Technitrol	1ZKHA	4
D1-11	Diode S101	DDC	S101	15
D12	Zener Diode 12 volt ± 5% 1 W	Motorola	1N4742A	1
D13	Zener Diode 6 volt ± 5% 1/2 W	Motorola	1N5233B	1
Q1,2	Transistor S201	DDC	S201	2
Z1,2	Integrated Circuit, Hex Inverter	Signetics or Fairchild	N8H90A or U6A901659X	2
A1,2	Integrated Circuit, Diff. Comparator	Motorola or Fairchild	MC1710C or U5B771039X	4
C1,2,6,7	Capacitor .0027 uf ± 5%	Paktron	PCR-330-0027-50-J	8
C3,4,5,8,9	Capacitor .047 uf -20, +80% 16V	Sprague	HY 435	9
C10,13,16	Capacitor 1 uf ± 10% 35V		CS13BF105K	3
C11,12,14,15,17,18	Capacitor .01 uf -20,+80% 100V	Erie	805-000-X5V0 103Z	6
C19,20	Capacitor 390pf ±5%	Elmenco	DM10-391J	2
	Washer, Teflon (.10 o.d. x .046 i.d. x .015 thk.)		Qty: As required	
	Connector 51 pin	Elco	00-7022-051-000-001	1

VOLTAGES
+18 V, Pin 24
+ 5 V, Pin 26
-12 V, Pin 28

DETAIL DRAWINGS
CIRCUIT CARD 11806
SCHEMATIC 11804
PICTORIAL 11805

	DRAWN	DATE
	EHB	10-22-68
CHECKED	Eade	10/22/68
APPROVED	EHB	10-23-68
APPROVED	NV Hewitt	10/23/68

TITLE
READ AMPLIFIER

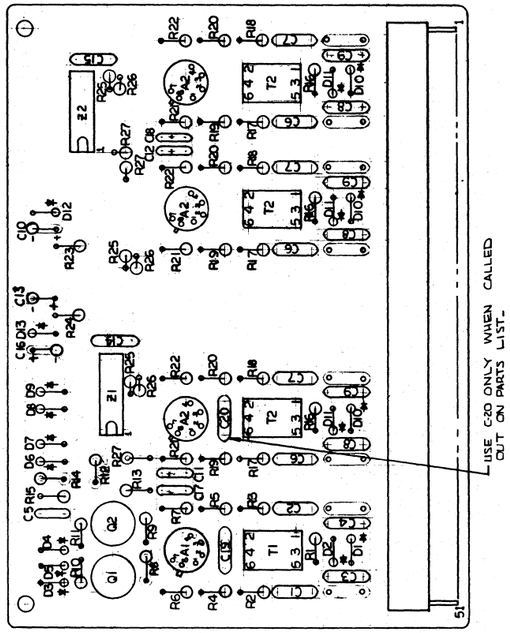
DIGITAL DEVELOPMENT CORPORATION

SHT. NO. 1

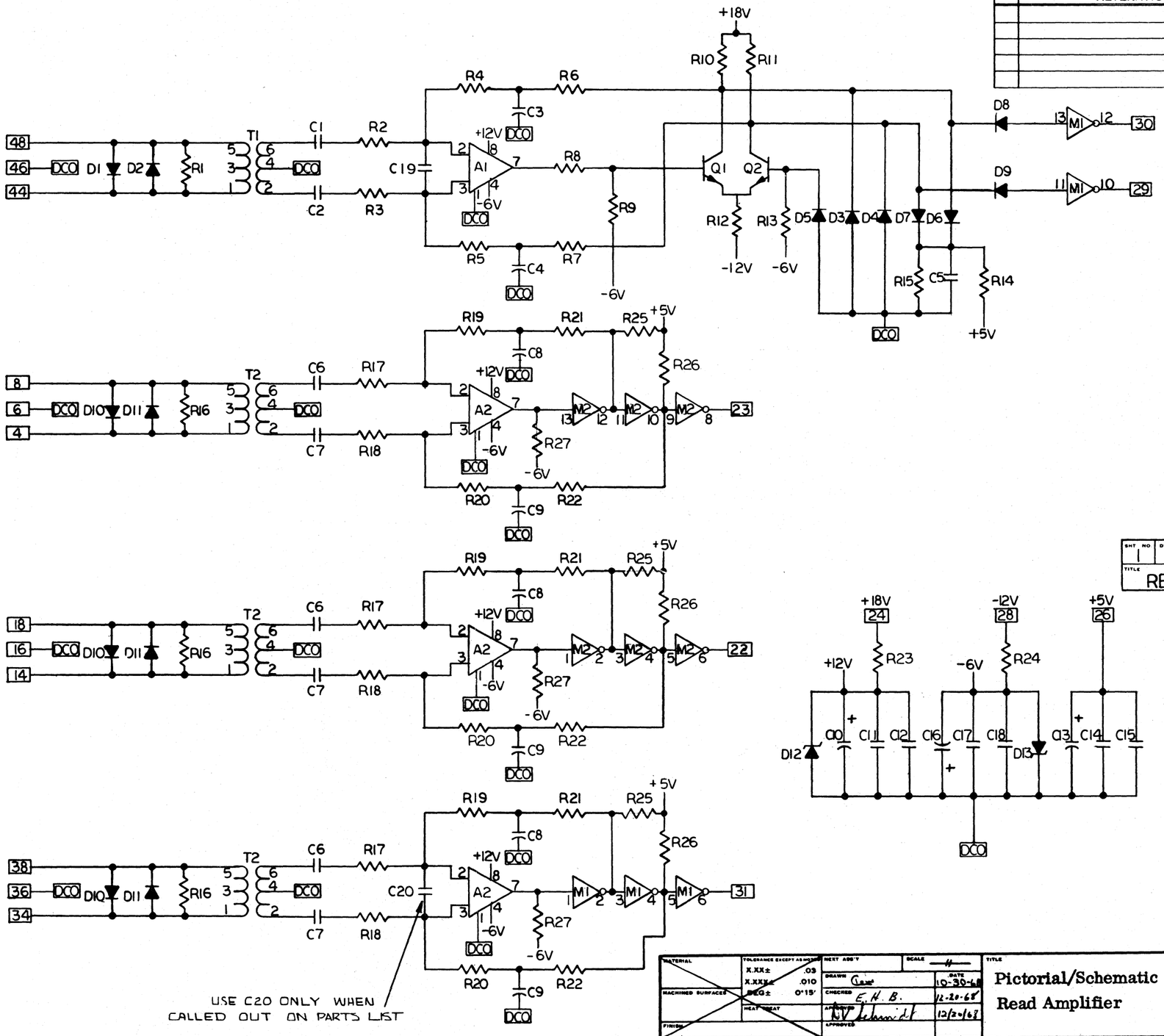
DRAWING NO. 11803 C

FORM 005

REV	ALTERATION	BY	DATE



USE C20 ONLY WHEN CALLED OUT ON PARTS LIST.



READ AMPLIFIER

MATERIAL	TOLERANCE EXCEPT AS NOTED	NEXT ASS'Y	SCALE
	X.XX± .03		
MACHINED SURFACES	X.XXX± .010	DRAWN C.Lam	DATE 10-30-68
	ANG± 0°15'	CHECKED E.H.B.	12-20-68
FINISH	HEAT TREAT	APPROVED N.V. Schmidt	12/20/68

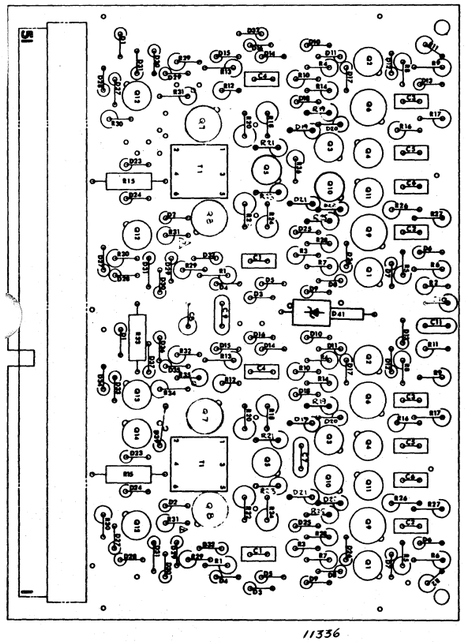
Pictorial/Schematic
Read Amplifier

DIGITAL DEVELOPMENT CORPORATION
3375 SCALDY VILLA RD., SAN DIEGO, CALIF.

SHT. NO. 1 | DWG NO 11804/11805 | REV

DWG. NO. 11804/11805

REV	ALTERATION	BY	DATE
A	ADDED R37 & R38	NVW	4-21-65
B	INCORP ECN 329	NVW	8-30-65
C	ADDED CONNECTION OF PIN 16	[illegible]	2-16-70
	PER ECR 1694 R.P. 11/1/69	[illegible]	3/11/70



11336

CIRCUIT B A

ΦB' INPUT 35 10

DATA INPUT 29 4

ΦA INPUT 30 3

(DATA)' INPUT 49 23

DISABLE INPUT 38 12

ENABLE INPUT 39 13

INVERTER INPUT 45 31 5 — C B A CIRCUIT

INVERTER OUTPUT 9 34 42 — A B C CIRCUIT

ΦA INPUT 19 — CIRCUIT A

ΦA OUTPUT 17 — CIRCUIT A

OUTPUT — CIRCUIT A B: 15 41, 14 40, 11 36

T1

24 +V, 28 -V, 1 51 DCO

SHT NO	DWG NO	REV
1	11326	C

TITLE: WRITE AMPLIFIER

MATERIAL	TOLERANCE EXCEPT AS NOTED	NEXT ASS'Y	SCALE NONE	TITLE
~	X.XX± .03			WRITE AMPLIFIER
	X.XXX± .010	DRAWN W. L. DEUEL	DATE 10 SEPT. 64	
MACHINED SURFACES	DEG± 0°15'	CHECKED		
~	HEAT TREAT ~	APPROVED [illegible]	12 [illegible] 64	
FINISH ~		APPROVED		

DIGITAL DEC DEVELOPMENT CORPORATION
1961 EDDS AVENUE • LA JOLLA, CALIFORNIA

SHT NO	DWG NO	REV
1	*11326	C

FORM NO [illegible]

*REPLACES DWG. NO. 11601/11602

ITEM	DESCRIPTION	MANUFACTURER	PART NUMBER	QUANTITY
C8, 10	Capacitor 1 µf ±20% 35 V		CS13AF010M	2
C2, 3	Capacitor 51 pf ±5% 500 V	Elmenco	DM-10-510J	4
C1, 4	Capacitor 150 pf ±5% 500 V	Elmenco	DM-10-151J	4
C5, 6	Capacitor 390 pf ±5% 500 V	Elmenco	DM-10-391J	4
C9, 11	Capacitor .01 µf +80%-20% 100 V	Erie	805X5V103Z	2
C7	Capacitor .1 µf +80-20% 12V	Erie	5655-000 Y5FO 104M	1
D1-4, 6-13, 15, 18,				
25-37,	Diode S101	DDC	S101	63
D23, 24	Diode 1N483		1N483	4
D5, 14	Diode, Zener 1N4370A		1N4370A	4
D41	Diode, Zener 1N3016A		1N3016A	1
D39	Diode	Hughes	HMN9502	1
D19-22	Diode S121	DDC	S121	4
	Connector 51 Pin	Elco	00-7022-051-000-001	1
Q1, 2, 3, 10, 12, 13,				
14	Transistor 2N708		2N708	13
Q4, 11	Transistor 2N3250		2N3250	4
Q6-9	Transistor 2N2537		2N2537	8
Q5	Transistor 2N3135		2N3135	2
	Transimount	Circuit Structures Lab	#88000	12

VOLTAGES

+18 V D.C.

-12 V D.C.

DETAIL DRAWINGS

CIRCUIT CARD #11316

SCHEMATIC #11326

PICTORIAL #11336

DRAWN H. L. W. DATE 9-9-64

CHECKED E. I. M. 9-21-64

APPROVED R. R. C. 9-21-64

APPROVED

TITLE

WRITE AMPLIFIER

DIGITAL DEVELOPMENT CORPORATION

SHT NO 1/2

DRAWING NO *11306 F

*REPLACES DWG. NO. 11600

FORM 006

ITEM	DESCRIPTION				MANUFACTURER	PART NUMBER	QUANTITY
R16, 26	Resistor	430 ohm	±5%	1/2 watt		RC20GF431J	4
R4, 7, 14, 28, 31							
35	Resistor	1300 ohm	±5%	1/2 watt		RC20GF132J	12
R3, 10	Resistor	1500 ohm	±5%	1/2 watt		RC20GF152J	4
R1, 13, 34	Resistor	1800 ohm	±5%	1/2 watt		RC20GF182J	5
R5, 8, 12, 15, 36	Resistor	2K	±5%	1/2 watt		RC20GF202J	9
R29, 32	Resistor	2200 ohm	±5%	1/2 watt		RC20GF222J	4
R17, 27	Resistor	3300 ohm	±5%	1/2 watt		RC20GF332J	4
R30, 33	Resistor	4700 ohm	±5%	1/2 watt		RC20GF472J	4
R2, 11	Resistor	5100 ohm	±5%	1/2 watt		RC20GF512J	4
R6, 9	Resistor	24K	±5%	1/2 watt		RC20GF243J	4
R18, 20, 22, 24,	Resistor	250 ohm		2 watt either/or	Sprague	240E2515	8
					Ward Leonard	TYPE 2X	
R21, 23	Resistor	3K	±5%	1/2 watt		RC20GF302J	4
R19, 25	Resistor	5.1 ohm	±5%	1/2 watt		RC20GF5R1J	4
T1	Transformer				Technitrol	1ZPHA	2
	Washer, Teflon (.10 O.D. x .046 I.D. x .015 thk)						166

VOLTAGES

+18 V D.C.

-12 V D.C.

DETAIL DRAWINGS

CIRCUIT CARD #11316

SCHEMATIC #11326

PICTORIAL #11336

		DATE
DRAWN	H. L. W.	9-9-64
CHECKED	E. I. M.	9-21-64
APPROVED	R. R. C.	9-21-64
APPROVED		

TITLE

WRITE AMPLIFIER

DIGITAL DEVELOPMENT CORPORATION

7341 EADS AVENUE • LA JOLLA, CALIFORNIA

SHT. NO. 2

DRAWING NO. *11306 F

*REPLACES DWG. NO. 11600

FORM 006

ITEM	DESCRIPTION		MANUFACTURER	PART NUMBER	QUANTITY
C1, C3	Capacitor, Tantalum	1 ufd 35 V		CS13BF010M	2
C2, 4, 5, 6, 7, 8	Capacitor, Disc Ceramic	.01 ufd	ERIE	805X5V103Z	6
R1	Resistor	82 ohms, 5W ±3%	DALE	Type GL-6	1
R2	Resistor	1.2K		RC20GF122J	16
I.C.1, I.C.3 &					
I.C.5-8	Integrated Circuit - Quad 2 input Nor Gate		DDC	S152	6
I.C.2, I.C.4	Integrated Circuit - Quad 2 input Nand Gate		DDC	S170	2
D1	Diode, Zener	5.1V, 1 W, ±5%	Motorola	IN4733A	1
Q1	Transistor			2N3641	16
	Connector	51 Pin	Elco	00-7022-051-000-001	1
	Washer, Teflon .10 O.D. x .046 I.D. x .015 thk				16
	Transimount		Ckt. Structures Lab. 88000		16

VOLTAGES

+18V

DETAIL DRAWINGS

CIRCUIT CARD	11660
SCHEMATIC	11662
PICTORIAL	11663

DRAWN	Eade	DATE 3/20/68
CHECKED	Eade	3/20/68
APPROVED	E. H. BUTLER	3-20-68
APPROVED		

TITLE

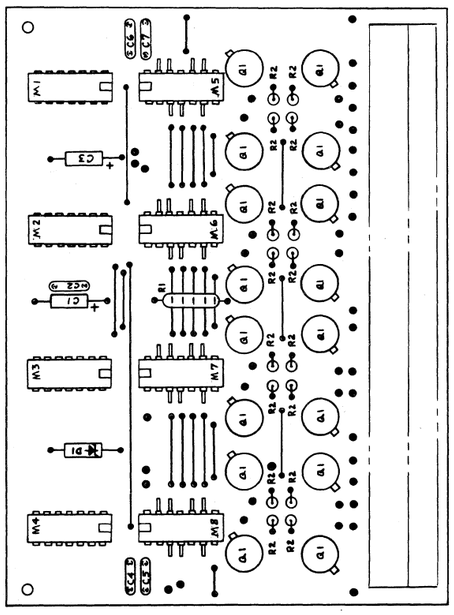
DECODE DRIVER

DIGITAL DEVELOPMENT CORPORATION
7241 EADS AVENUE • LA JOLLA, CALIFORNIA

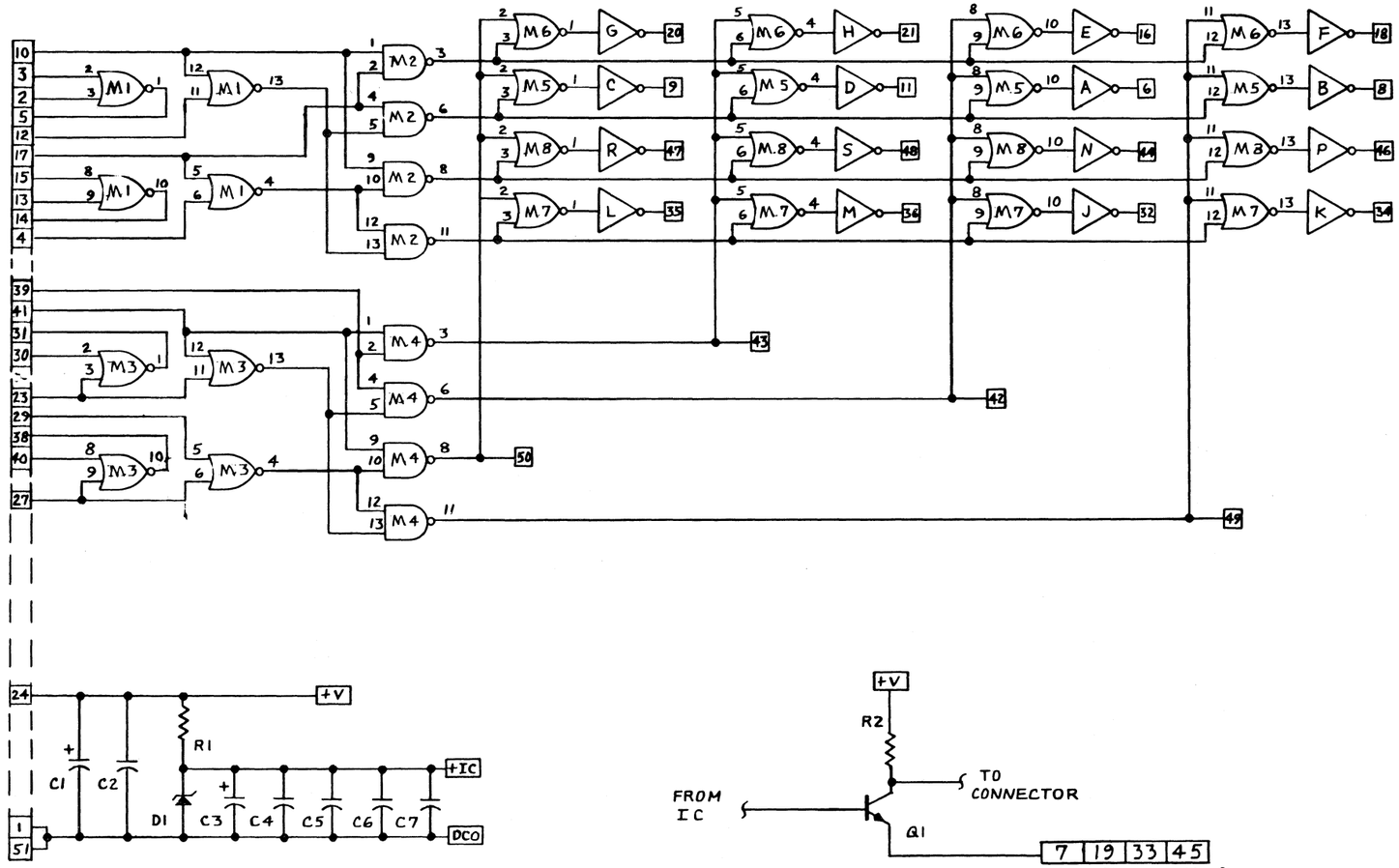
DRY. NO.	DRAWING NO.
1	11661

FORM 0.0.0

REV	ALTERATION	BY	DATE
	SEE REVISION SHT		



NOTES—
1. ALL JUMPERS TO BE INSULATED WITH TEFLON TUBING.
2. ● INDICATES THRU BOARD JUMPERS TO BE INSTALLED IF CKT. BOARD IS NOT MADE WITH PLATED THRU HOLES.



INVERTER
TYP. 16 PLC'S.

7	19	33	45
A	E	J	N
B	F	K	P
C	G	L	R
D	H	M	S

} CKTS

SHT NO	DWG NO	REV
1		

TITLE: DECODE DRIVER

MATERIAL	TOLERANCE EXCEPT AS NOTED	NEXT ASS'Y	SCALE	TITLE
	X.XX± .03			Pictorial/Schematic
	X.XXX± .010	DRAWN Eado	DATE 10/24/67	Decode Driver
MACHINED SURFACES	DEG± 0°15'	CHECKED		
	HEAT TREAT	APPROVED E.H. BUTLER	3-20-68	
FINISH		APPROVED		

DIGITAL DEVELOPMENT CORPORATION
5575 KEARNY VILLA RD., SAN DIEGO, CALIF.

SHT NO	DWG NO	REV
1		

DWG. NO. 11662/11663

ITEM	DESCRIPTION	MANUFACTURER	PART NUMBER	QUANTITY
R1, 11	Resistor, 2.4 K ohm, ±5%, 1/2 watt		RC20GF242J	2
R2, 12	Resistor, 5.1 K ohm, ±5%, 1/2 watt		RC20GF512J	2
R3, 10, 13	Resistor, 1.3 K ohm, ±5%, 1/2 watt		RC20GF132J	10
R4	Resistor, 1.8 K ohm, ±5%, 1/2 watt		RC20GF182J	1
R5, 6	Resistor, 100 ohm, ±5%, 1/2 watt		RC20GF101J	2
R7	Resistor, 240 ohm, ±5%, 1/2 watt		RC20GF241J	1
R8	Resistor, 1 K ohm, ±5%, 1/2 watt		RC20GF102J	8
R9	Resistor, 4.3 K ohm, ±5%, 1/2 watt		RC20GF432J	8
R14	Resistor, 750 ohm, ±5%, 1/2 watt		RC20GF751J	1
D6	Diode	DDC	S121	1
D1-5, 8-14	Diode	DDC	S101 or IN914	19
D7	Diode, Zener, 4.3 volt ±5%		IN4731A	1
D15	Diode, Zener, 3.6 volt ±5%		IN4729A	1
Q1, 2, 5, 6,	Transistor	DDC	S201 or 2N4275	11
Q3, 4	Transistor		2N3250	9
C1-3	Capacitor, 1 mfd, ±20%, 35 volt		CS13AF010M	3
DL1	Delay Line, 250 ohm, 12.5 n sec per tap	PCA	DL250L-.25T-2750	1
	Connector, 51 Pin	Elco	00-7022-051-000-001	1
	Washer, Teflon (.10 O.D. x .046 I.D. x .015 thk)			60

VOLTAGES

+18 VDC
-12 VDC

DETAIL DRAWINGS

CIRCUIT CARD	11550
SCHEMATIC	11645
PICTORIAL	11650

DRAWN	C.J.C.	7-21-67
CHECKED	E.H.B.	7-21-67
APPROVED		7-21-67

TITLE: DELAY CIRCUIT

DIGITAL DEVELOPMENT CORPORATION

SIZE	DWG. NO.
1	11640

ITEM	DESCRIPTION	MANUFACTURER	PART NUMBER	QUANTITY
R1, R3, R7	Resistor 2K 1/2 W 5%		RC20GF202J	3
R2	Resistor 4.7K 1/2 W 5%		RC20GF472J	1
R4, R5	Resistor 220 Ohms 7 W	Sprague	244E 2215	2
R6	Resistor 5K 5 W	Sprague	243E5025	1
R8	Resistor 600 Ohms 7 W	Sprague	244E 6015	1
D1 Thru D12	Diode 600v PIV 1A		IN4385	12
D13	Diode 4-layer, 8-12v		S120	1
Q3	Silicon Controlled Rectifier		S205	1
Q1, Q2	Silicon Controlled Rectifier		S208	2
	Transistor Pad	Milton Ross	10197	3
	Terminal	Cambion	1245-2	9

VOLTAGES

DETAIL DRAWINGS

CIRCUIT CARD 11696

SCHEMATIC 11697

PICTORIAL 11698

DRAWN Eade DATE 3/28/68

CHECKED Eade 3/28/68

APPROVED E. H. BUTLER 3-29-68

APPROVED

TITLE

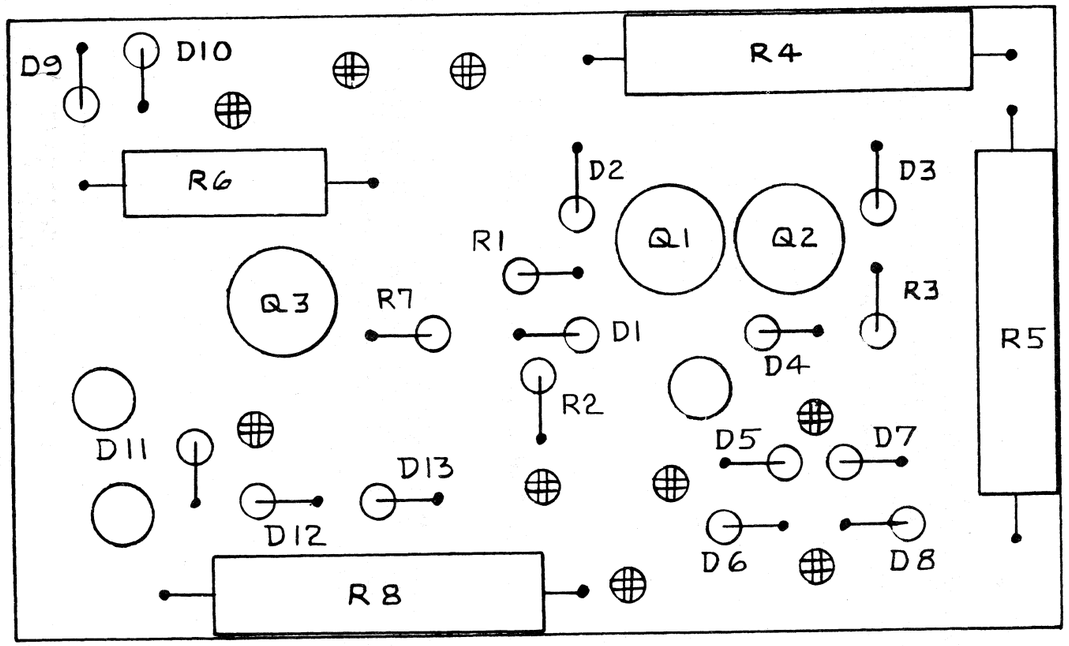
SYNCHRONOUS SWITCH

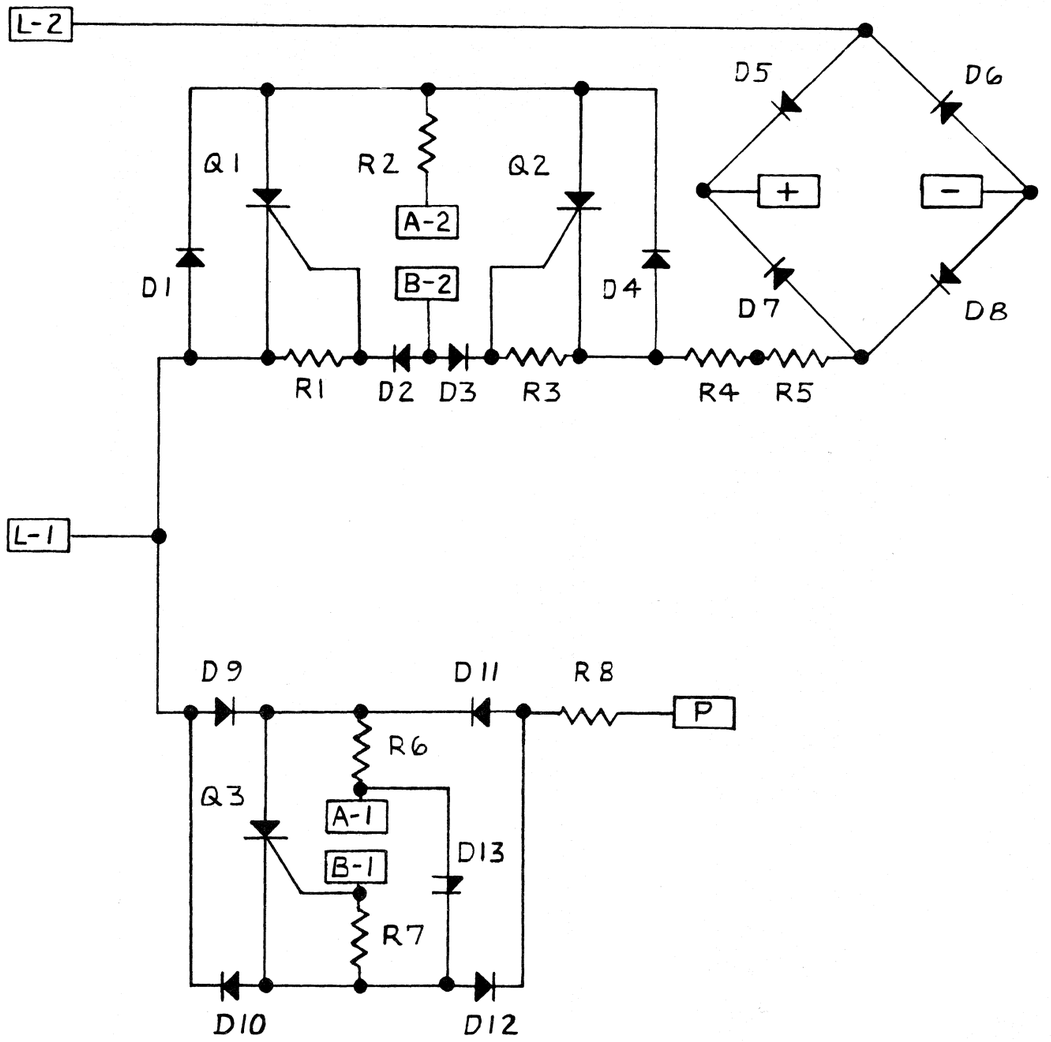
DIGITAL DEVELOPMENT CORPORATION

7941 EADS AVENUE • LA JOLLA CALIFORNIA

SHT. NO. 1

DRAWING NO. 11695 B





1. ALL DIODES CATHODE TO BOARD.

NOTES ~.

DRAWN Eade	DATE 3-8-68	TITLE SYNCHRONOUS SWITCH PICTORIAL / SCHEMATIC	DIGITAL DEVELOPMENT CORPORATION
			SHT NO 1 / DWG NO 11697/11698 / REV

ITEM	DESCRIPTION	MANUFACTURER	PART NUMBER	QUANTITY
R1, R2	Resistor 1.5K ±5% 1/2 watt		RC20GF152J	2
R3-R10	Resistor 1K ±5% 1/2 watt		RC20GF102J	8
C1	Capacitor .01uf +80%-20% 100V	Erie	805-000-X5V0 103Z	1
C1-D26	Diode	DDC	S121 Matched	26
Q1-Q8	Transistor	Fairchild	EN3502	8
	Terminal	Lerco	#5020B	6
			Model 7302, Serial No. 39 and below	
			Model 7301, Serial No. 66 and below	

VOLTAGES

DETAIL DRAWINGS

CIRCUIT CARD	11821
SCHEMATIC	11819
PICTORIAL	11820

		DATE
DRAWN	E.H.B	10-25-68
CHECKED	E.H.B.	10-25-68
APPROVED	DV Schmidt	10/25/68
APPROVED		

TITLE

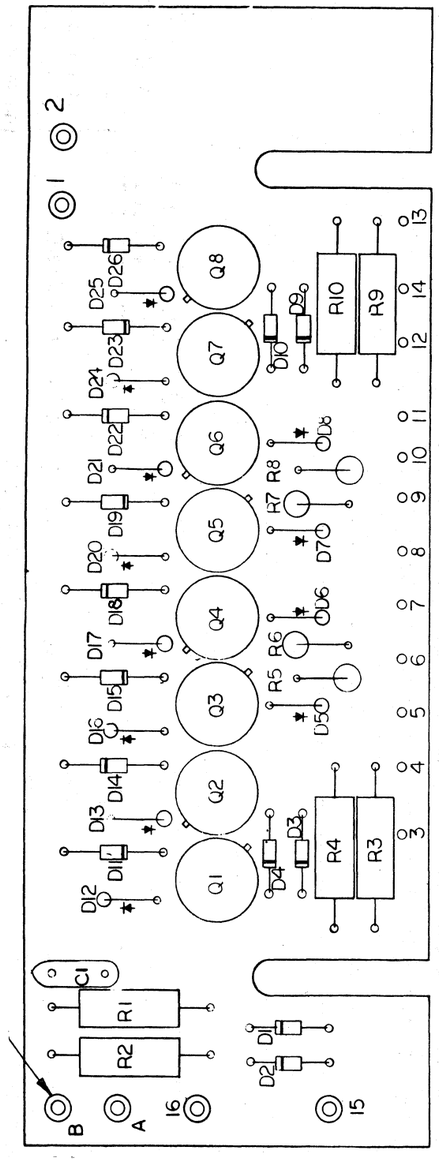
"X" AMPLIFIER

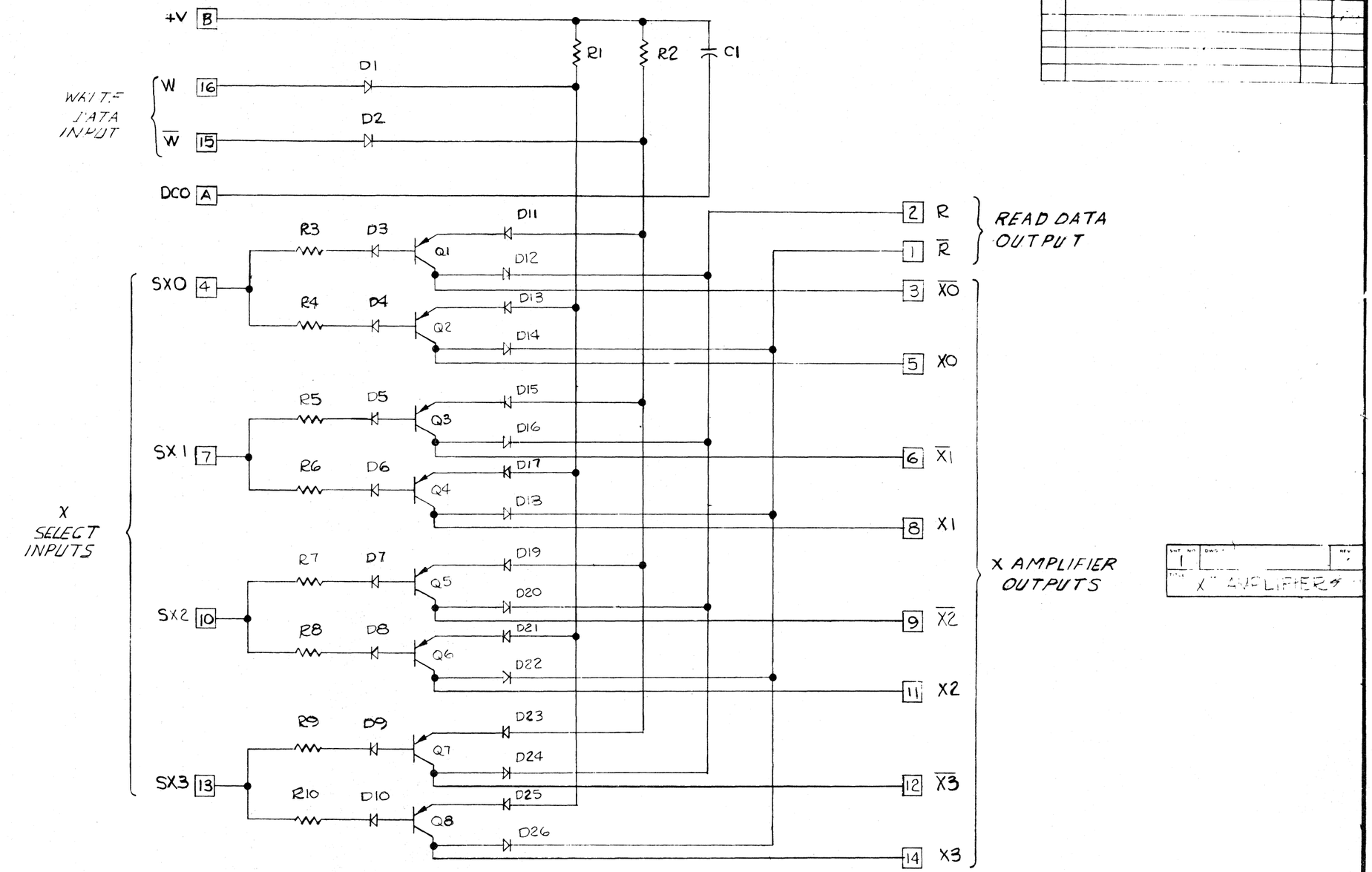
DIGITAL DEVELOPMENT CORPORATION

SHT. NO.	DRAWING NO.	
1	11818	A

FORM 005

REV	ALTERATION	BY	DATE





SHT. NO. 1 | DWG. | REV.

"X" AMPLIFIER

Model 7302, Serial No. 39 and below
Model 7301, Serial No. 66 and below

MATERIAL	TOLERANCE EXCEPT AS NOTED: X.XX± .03; X.XXX± .010; DEG± 0°15'	NEXT ASS'Y	SCALE NONE
MACHINED SURFACES	HEAT TREAT	DRAWN Jones 12-19-68	CHECKED J.H.E. 12-19-68
FINISH		APPROVED W. Schmidt 12/20/68	

TITLE: Pictorial/Schematic "X" Amplifier

DIGITAL DEVELOPMENT CORPORATION, 5515 KEARNY MESA RD. SAN DIEGO, CALIF.

SHT. NO. 1 | DWG. | REV.

DWG. NO. 11819/11820

ITEM	DESCRIPTION	MANUFACTURER	PART NUMBER	QUANTITY
R1, R2	Resistor 1.5K ±5% 1/2 watt		RC20GF152J	2
R3-R10	Resistor 1K ±5% 1/2 watt		RC20GF102J	8
R11-R18	Resistor 1.5K±5% 1/8 watt		RC05GF152J	8
C1	Capacitor .01uf +80%-20% 100V	Erie	805-000-X5V0 103Z	1
C1-D26	Diode	DDC	S121 Matched	26
Q1-Q8	Transistor	Fairchild	EN3502	8
	Terminal	Lerco	#5020B	6
	Terminal	Cambion	#2089-2	12
		Model 7302, Serial No. 40 and above		
		Model 7301, Serial No. 67 and above		

VOLTAGES

DETAIL DRAWINGS

CIRCUIT CARD	11821
SCHEMATIC	11819
PICTORIAL	11820

		DATE
DRAWN	E. N. B.	10-25-68
CHECKED	E. N. B.	10-25-68
APPROVED	D V Schmidt	10/25/68
APPROVED		

TITLE

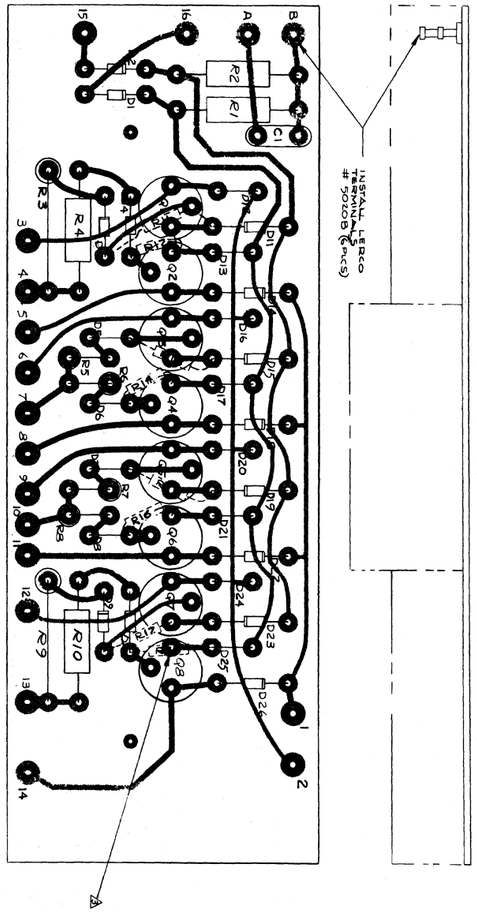
"X" AMPLIFIER

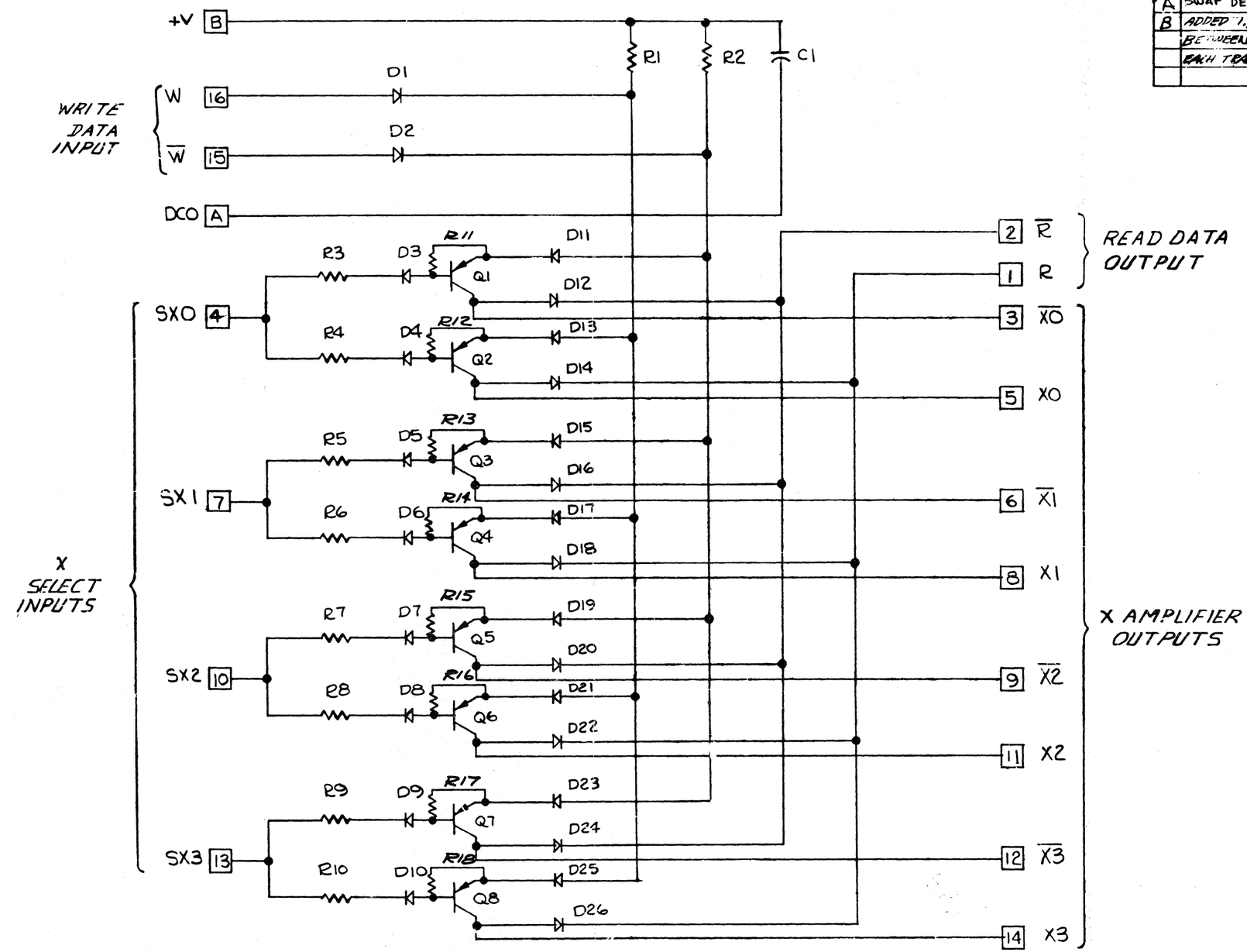
DIGITAL DEVELOPMENT CORPORATION

SHT. NO.	DRAWING NO.	
1	11818	D

FORM 006

REV	ALTERATION	BY	DATE
A	SWAP DESIG. R&R - ECR 1153		
B	ADDED 1.5K, ½ WATT 5% RESISTOR		
	BETWEEN THE BASE AND EMITTER OF		
	EACH TRANSISTOR - PER ECR 1262		
	RP 12-22-69		





SHT NO	DWG NO	REV
1	11819	B

TITLE "X" AMPLIFIER

Model 7302, Serial No. 40 and above
Model 7301, Serial No. 67 and above

MATERIAL	TOLERANCE EXCEPT AS NOTED: X.XX± .03; X.XXX± .010; DEG± 0°15'	NEXT ASS'Y	SCALE NONE
MACHINED SURFACES	HEAT TREAT	DRAWN Jones	DATE 12-19-68
FINISH		CHECKED J.H.C.	12-19-68
		APPROVED D.V. Schmidt	12/20/68

TITLE SCHEMATIC "X" AMPLIFIER

DIGITAL DEVELOPMENT CORPORATION 5575 KEARNY VILLA RD. SAN DIEGO CALIF.

SHT NO	DWG NO	REV
1	11819	B