HEWLETT-PACKARD

HP 7957A AND HP 7958A DISC DRIVES

HARDWARE SUPPORT MANUAL

CERTIFICATION

Products, materials, parts, and services furnished on this order have been provided in accordance with all applicable Hewlett-Packard specifications. Actual inspection and test data pertaining to this order is on file and available for examination.

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HP 7957A AND 7958A DISC DRIVES HARDWARE SUPPORT MANUAL

Manual part number: 07957-90903
Microfiche part no. 07957-90803

Printed: SEPTEMBER 1987 Edition 2
Printed in U.S.A. E0987

MODELS COVERED

This manual covers the following models: HP 7957A and HP 7958A.

OPTIONS COVERED

In addition to the standard model, this manual covers the following options: 015, 550.

HEWLETT-PACKARD
P.O. Box 39, Boise, Idaho 83707-0039

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The Federal Communications Commission has specified that the following notice be brought to the attention of the users of this product.

FEDERAL COMMUNICATIONS COMMISSION
RADIO FREQUENCY INTERFERENCE
STATEMENT

Warning: This equipment generates and uses radio frequency energy and if not installed and used properly, that is, in strict accordance with the manufacturer's instructions, may cause interference to radio and television reception. It has been type tested and found to comply with the limits for a Class B computing device in accordance with the specifications in Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference in a residential installation. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures: re-orient the receiving antenna; relocate the computer with respect to the receiver; move the computer away from the receiver; plug the computer into a different branch circuit. If necessary, the user should consult the dealer or authorized field service representative for additional suggestions. The user may find the following booklet prepared by the Federal Communications Commission helpful: "How to Identify and Resolve Radio-TV Interference Problems". This booklet is available from the U.S. Government Printing Office, Washington, DC 20402. Stock No. 004-000-00345-4.

Safety Considerations

GENERAL - This product and related documentation must be reviewed for familiarization with safety markings and instructions before operation.

SAFETY SYMBOLS

Instruction manual symbol: the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect the product against damage.

Indicates hazardous voltages.

Indicates earth (ground) terminal.

WARNING

The WARNING sign denotes a hazard. It calls attention to a procedure or practice that, if not correctly performed or adhered to, could result in personal injury. Do not proceed beyond a WARNING sign until the indicated conditions are fully understood and met.

CAUTION

The CAUTION sign denotes a hazard. It calls attention to an operating procedure or practice that, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a CAUTION sign until the indicated conditions are fully understood and met.

SAFETY EARTH GROUND - This is a safety class I product and is provided with a protective earthing terminal. An uninterruptible safety earth ground must be provided from the main power source to the product input wiring terminals, power cord, or supplied power cord set. Whenever it is likely that the protection has been impaired, the product must be made inoperative and be secured against any unintended operation.

BEFORE APPLYING POWER - Verify that the product is configured to match the available main power source according to the input power configuration instructions provided in this manual.

If this product is to be operated with an autotransformer make sure that the common terminal is connected to the earth terminal of the main power source.

SERVICING

WARNING

Any servicing, adjustment, maintenance, or repair of this product must be performed only by service-trained personnel.

Adjustments described in this manual may be performed with power supplied to the product while protective covers are removed. Energy available at many points may, if contacted, result in personal injury.

Capacitors inside this product may still be charged after the product has been disconnected from the main power source.

To avoid a fire hazard, fuses with the proper current rating and of the specified type (normal blow, time delay, etc.) must be used for replacement. To install or remove a fuse, first disconnect the power cord from the device. Then, using a small flat-bladed screw driver, turn the fuseholder cap counterclockwise until the cap releases. Install either end of a properly rated fuse into the cap. Next, insert the fuse and fuseholder cap into the fuseholder by pressing the cap inward and then turning it clockwise until it locks in place.

Printing History

New editions are complete revisions of the manual. Update packages, which are issued between editions, contain additional and replacement pages to be merged into the manual by the customer. The dates on the title page change only when a new edition or a new update is published. No information is incorporated into a reprinting unless it appears as a prior update; the edition does not change when an update is incorporated.

A software code may be printed before the date; this indicates the version level of the software product at the time the manual or update was issued. Many product updates and fixes do not require manual changes and, conversely, manual corrections may be done without accompanying product changes. Therefore, do not expect a one-to-one correspondence between product updates and manual updates.

Edition 1 ..... DECEMBER 1986
Edition 2 ..... SEPTEMBER 1987

Herstellerbescheinigung

Hiermit wird bescheinigt, daß das Gerät/System HP 7957A/HP 7958A in Übereinstimmung mit den Bestimmungen von Postverfügung 1046/84 funkentstört ist.

Der Deutschen Bundespost wurde das Inverkehrbringen dieses Gerätes/Systems angezeigt und die Berechtigung zur Überprüfung der Serie auf Einhaltung der Bestimmungen eingeräumt.

Manufacturer's Declaration

This is to certify that the product(s) HP 7957A/HP 7958A is in accordance with the Radio Interference Requirements of Directive FTZ 1046/1984. The German Bundespost was notified that this equipment was put into circulation; the right to check the series for compliance with the requirements was granted.

Additional Information for Test and Measurement Equipment

If Test and Measurement Equipment is operated with unscreened cables and/or used for measurements on open setups, the user has to assure that under operating conditions the Radio Interference Limits are still met at the border of his premises.

Contents

Contents (continued)

Contents (continued)

Figures and Tables

Figure or Table **Page**

General Information 1

1-1. INTRODUCTION

The Hewlett-Packard 7957A and HP 7958A Disc Drives are random access, data storage devices designed for use with small and medium sized computer systems. The formatted storage capacities of the HP 7957A and HP 7958A are 81 megabytes and 130 megabytes, respectively. In this manual, unless otherwise specified, "disc drive" refers to the HP 7957A and HP 7958A.

The disc drive employs three (HP 7957A) or five (HP 7958A) nonremovable 130-millimetre (5.12-inch) discs for storage media. Each disc surface employs one movable head to service its data tracks. The bottom surface of the lowest disc in the stack contains continuous prerecorded servo data which is used to ensure the precise positioning of the read/write heads.

Head positioning is performed by a rotary actuator and a closed-loop servo positioning system. Mechanical and contamination protection for the discs, heads, and the rotary actuator is provided by a sealed head-disc module. The head-disc module includes a self-contained air filtration system which supplies clean air and temperature equalization throughout the module.

Also included in the disc drive are a Hewlett-Packard Interface Bus (HP-IB) controller and a power supply.

The disc drive contains internal self-test diagnostics and a fault-finding system which exercise key functions of the disc drive. Self test is performed automatically at power on and can also be initiated by the host. Go/no-go test results are indicated by a green/red indicator on the front panel. If a failure occurs, information on the cause of the failure can be determined by viewing the status of the green/red indicators.

The disc drive is packaged in a stand-alone desktop cabinet. Accessories available include a desk-height stand-alone cabinet designed to hold the disc drive and other desktop stack modules. A kit for rack mounting the disc drive in a standard EIA equipment rack is also available.

This manual provides all the service information needed to maintain the disc drive. Details of the control functions provided by the host computer are described in the installation documentation provided with the computer.

1-2. SCOPE OF MANUAL

The manual is divided into six chapters as follows:

a. Chapter 1 contains a general description of the disc drive.

b. Chapter 2 provides information about the ESDI Interface between the controller PCA and the head disc assembly (HDA). It also contains information on CS/80 Command Set implementation, Request Status Summary and Utility Command summary.

c. Chapter 3 describes the operating principles of the disc drive.

d. Chapter 4 contains servicing information for the disc drive, including instructions on how to use the diagnostics tools.

e. Chapter 5 supplies step-by-step removal and replacement procedures for all field-replaceable assemblies and parts in the disc drive.

f. Chapter 6 lists and illustrates all of the field-replaceable assemblies and parts in the disc drive.

Appendix A provides a listing and copy of all the service notes applicable to the HP 7957A and HP 7958A Disc Drives.

1-3. OPTIONS

Option 015 is the power option. The only requirement is for the switch in the power module to be placed in the proper position. Option 550 is the deletion of the Model 10833B HP-IB Cable from the order.

1-4. RELATED MANUALS

For operating and installation instructions, refer to the *HP 7957A and HP 7958A Disc Drive Owners Manual*, part no. 07957-90901, and the *Site Environmental Requirements for Disc/Tape Drives Manual*, part no. 5955-3456. For instruction set information, refer to the *CS/80 Instruction Set Programming Manual*, part no. 5955-3442. For additional service information, refer to the *CS/80 External Exerciser Reference Manual*, part no. 5955-3462. The CE Handbook for the HP 7957A and HP 7958A Disc Drive is part no. 07957-90905.

1-5. CHARACTERISTICS

Characteristics of the disc drive, including physical dimensions and power requirements, are listed in Table 1-1, Disc Drive Characteristics. Detailed specifications for the disc drive, including environmental requirements, are listed in the *Site Environmental Requirements for Disc/Tape Drives Manual*, part no. 5955-3456. This publication is supplied with the disc drive.

Table 1-1. Disc Drive Characteristics

SAFETY

Meets all applicable safety standards of IEC 380 and IEC 435.

UL Listed UL 114 and UL 478.

CSA certified to CSA C22.2 No. 143 and No. 154.

POWER REQUIREMENTS

Specified Source (selected by rear panel VOLTAGE SELECTOR switch)

Voltage (true RMS): 115V range; 100V, 115V, 120V, single phase, (inclusive tolerance range is 90V to 132V)

230V range; 220V, 240V, single phase, (inclusive tolerance range is 180V to 264V)

Frequency: 47.5 to 66 Hz

Typical Current (true RMS): 115V range; 0.87A
230V range; 0.48A

Typical Power: 115V range; 65W
230V range; 65W

SIZE/WEIGHT

Height: 132 mm (5.2 in.)

Width: 325 mm (12.8 in.)

Depth: 285 mm (11.2 in.)

Net Weight: 9.9 kg (21.8 lb)

Shipping Weight: 14.0 kg (31.0 lb)

Interface Information 2

2-1. INTRODUCTION

This chapter describes the implementation of the Enhanced Small Device Interface (ESDI) on the disc drive mechanisms. Also included at the end of this section is information on the CS/80 Command Set implementation, request status summary and utility command summary. Included is the ESDI information specific to these products, as well as a discussion of operating features designed to improve system performance. The information in this chapter is intended to give the user an insight into how the product operates within the ESDI environment.

The disc drives conform fully to the specifications defined in the following industry-standard document: *Enhanced Small Device Interface Specification (REV F).* It is assumed that the reader is thoroughly familiar with the general operation of ESDI as defined in the specification. When used in conjunction with the ESDI specification, this chapter provides the additional information necessary to successfully communicate with the drive over ESDI.

NOTE

To maintain consistency with standard ESDI terminology, the term "drive" is used to refer to the disc mechanism in this chapter.

2-2. SUPPORTED ESDI FEATURES

The disc drives support the following standard ESDI features:

- Serial Mode Operation
- 10 Megabit Per Second Transfer Rate
- Configuration Reporting
- Drive Hard Sectoring
- Daisy Chain Configuration (up to 7 drives)
- Power-On Sequencing
- Track Offsets
- Internal Self-Test Diagnostics
- Media Defect List

2-3. DRIVE INTERFACE CHARACTERISTICS

The drive complies with the physical interface characteristics defined in the ESDI specification. Refer to the specification for cabling requirements and connector pin assignments. The physical location of the two interface, one power and one ground connectors are shown in figure 6-1. (For clarity, the power connector pin assignments are also shown.)

The drive electrical interface circuits conform to the specified electrical requirements. The drive uses the 220/330-ohm termination option to terminate all control signals originating at the controller.

2-4. INTERFACE SIGNALS

The serial-mode use of all data and control signal lines is defined in the ESDI specification. The following paragraphs include additional product-specific considerations regarding the use of each signal line. Tables 2-1, 2-2 and 2-3 provide response bit information.

- **DRIVE SELECT LINES.** The drive responds to selection by asserting its DRIVE SELECTED line within 250 nanoseconds (see figure 2-1). When selecting a drive, the controller must ensure that all drive select lines change within less than 100 nanoseconds. This precludes any undesired drive selection during transition of the drive select lines.

Table 2-1. General Configuration Response Bits

BIT POSITION	DRIVE FEATURE	BIT VALUE*
15	Tape Drive	0
14	Format Speed Tolerance Gap Required	0
13	Track Offset Option Implemented	1
12	Data Strobe Offset Option Implemented	1
11	Rotational Speed Tolerance > 0.5%	0
10	Transfer Rate > 10 MHz	0
9	Transfer Rate > 5 MHz <= 10 MHz	1
8	Transfer Rate <= 5 MHz	0
7	Removable Cartridge Drive	0
6	Fixed Media Drive	1
5	Spindle Motor Control Option Implemented	1
4	Head Switch Time > 15 usec	0
3	RLL Encoded (not MFM)	1
2	Controller Soft Sectored (Address Mark)	0
1	Drive Hard Sectored (Sector Pulses)	1
0	Controller Hard Sectored (Byte Clock)	0

* 1 indicates that drive implements specified feature.

If the controller attempts a write with an invalid head selected, the drive responds by setting ATTENTION and Invalid Or Unimplemented Command status bit. If the controller attempts to read with an invalid head, the read will be executed with the last valid head selected.

- **HEAD SELECT LINES.** When selecting a head, the controller must ensure that all head select lines change within less than 100 nanoseconds. This avoids an inadvertent head selection during transition of the head select lines. Valid head select values for each drive are shown in table 2-4.

- **WRITE GATE.** The WRITE GATE timing used during formatting and normal writing is shown in figures 2-2 and 2-3, respectively.

  The following timing restrictions apply to the WRITE GATE signal:

  - When the drive performs a head switch operation, the controller must not activate WRITE GATE until COMMAND COMPLETE is activated, indicating completion of the head switch.

  - When performing a write following a read, WRITE GATE must not be activated for a minimum of 500 nanoseconds after READ GATE is deactivated.

Table 2-2. Specific Configuration Response Bits

CMD MODIFIER BITS				CONFIGURATION DATA REQUESTED	DRIVE RESPONSE	
11	10	9	8		HEX	DEC
0	0	0	1	Number of cylinders, fixed	05DD	1501
0	0	1	0	Number of cylinders, removable	0000	0
0	0	1	1	Number of heads Bits 15-8: Removable drive heads Bits 2-0: Fixed heads	 00 *	 0 *
0	1	0	0	Minimum unformatted bytes per track	5780	22400
0	1	0	1	Unformatted bytes per sector	015E	350
0	1	1	0	Sectors per track	0040	64
0	1	1	1	Minimum bytes in ISG field (not including intersector speed tolerance): Bits 15-8: ISG bytes after INDEX Bits 2-0: Bytes per ISG	 0C 2E	 12 46
1	0	0	0	Minimum bytes per PLO Sync field	000E	13
1	0	0	1	Number of words of vendor-unique status available	0001	1

*HP 7957A - 06/6; HP 7958A - 09/9
(includes servo head)

- When formatting the disc media, the controller must activate WRITE GATE a minimum of 2.5 microseconds before the beginning of the Address PLO Sync field (see figure 2-2). Once activated, WRITE GATE may remain active for the entire track. If deactivated, WRITE GATE must remain inactive for at least 200 nanoseconds.

- After writing the address field or data field, two additional bytes of dummy data must be written. This is due to encoding delays, which cause an 8-bit delay between the time the data is transmitted to the drive and when it is actually written on the media. This dummy data is written in the Address Pad or Data Pad field as appropriate.

- The drive must not be deselected while WRITE GATE is activated.

Table 2-3. Standard Status Response Bits (1 of 2)

BIT POSITION	DESCRIPTION
15	**Reserved.** This bit is always zero.
14	**Removable Media Not Present.** The drive does not use removable media, therefore this bit is always zero.
13	**Write Protected, Removable Media.** The drive does not use removable media, therefore this bit is always zero.
12	**Write Protected, Fixed Media.** The drive does not include a write protect feature, therefore this bit is always zero.
11	**Reserved.** This bit is always zero.
10	**Reserved.** This bit is always zero.
9	**Spindle Motor Stopped.** This bit indicates the spindle motor is not up to speed. If this bit is set, the controller should send a Control command specifying a Start Spindle Motor operation. A change of state on this bit due to the successful execution of a Start Spindle Motor or Stop Spindle Motor operation does not cause ATTENTION to go active.
8	**Power-On Reset Conditions Exist.** This bit notifies the controller that the drive operating parameters have been set to their default values. This bit is set following a power-on sequence or when an internal drive fault condition occurs that causes an internal power-on reset operation to occur (e.g., a momentary loss of dc power). The controller may have to reconfigure drive operating conditions. The controller should also check the Spindle Motor Stopped status bit (bit 9) and perform a motor-on sequence if necessary.
7	**Command Data Parity Fault.** This bit indicates that the drive detected a parity error on the serial command data received from the controller. The drive will not attempt execution of the command if a parity error is detected.
6	**Interface Fault.** This bit indicates that the drive has detected an interface protocol timeout. An Interface Fault occurs when the controller fails to respond to an edge of the TRANSFER REQ/TRANSFER ACK handshake protocol within 13 milliseconds (see figure 2-5).
5	**Invalid Or Unimplemented Command.** This bit indicates that the drive has received an invalid or reserved command, command modifier, or command parameter. The drive will also set this bit if the controller sends a valid command that the drive is currently unable to execute (e.g., a Seek command while the spindle motor is stopped).
4	**Seek Fault.** This bit indicates that a catastrophic seek failure occurred. This bit will be set only after the drive has made every attempt to successfully complete the seek. The controller may elect to retry the seek operation, however such retries will most likely be unsuccessful.

Table 2-3. Standard Status Response Bits (2 of 2)

3	**Write Gate With Track Offset.** This bit indicates that the controller activated WRITE GATE while the drive was configured for a nonzero track offset. The controller should restore the track offset to zero, and then retry the write operation.
2	**Vendor-Unique Status Available.** This bit indicates that vendor-unique status is valid and available to the controller. This information is intended for use by service-trained personnel. The controller should not initiate any action based on the content of the vendor-unique status.
1	**Write Fault.** This bit indicates that a write fault has occurred. This fault can be caused by a variety of conditions; however, regardless of the cause, the controller should retry the write operation a minimum of five times. For simplification, the controller may elect to use the same recovery routine recommended for the preceding Write Gate With Track Offset fault. A Write Fault can be caused by one of the following conditions: • The controller activated WRITE GATE while the head was physically off track center. • The controller activated WRITE GATE while the spindle motor was off speed. • The controller activated WRITE GATE while COMMAND COMPLETE was inactive. The controller must wait for the drive to activate COMMAND COMPLETE before retrying the write operation. • The controller attempted a write with an illegal head selected. • The controller attempted a write while the spindle was out of write speed tolerance. • The controller attempted a write while the spindle was not spinning. • The controller attempted a write while ATTENTION was set. • The drive's R/W preamp chip indicated a Write Unsafe condition.

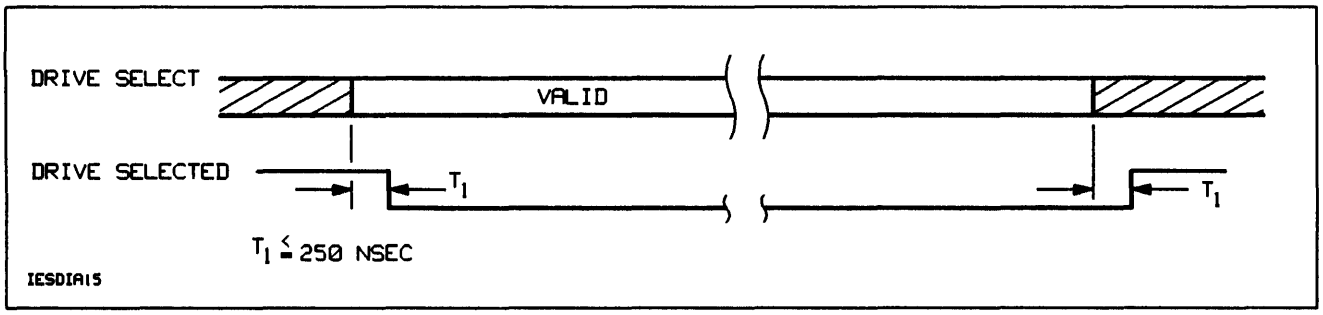


Figure 2-1. Drive Selection/Deselection Timing

Table 2-4. Valid Head Select Values

HEAD SELECT LINES				HEAD SELECTED	
2^3	2^2	2^1	2^0	HP 7957A	HP 7958A
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	2	2
0	0	1	1	3	3
0	1	0	0	4	4
0	1	0	1	5	5
0	1	1	0	Inv	6
0	1	1	1	Inv	7
1	0	0	0	Inv	Inv
1	0	0	1	Inv	Inv
1	0	1	0	Inv	Inv
1	0	1	1	Inv	Inv
1	1	X	X	Inv	Inv

- **READ GATE.** The READ GATE timing is shown in figure 2-4.

  The following timing restrictions apply to the READ GATE signal:

  - When the drive performs a head switch operation, the controller should not activate READ GATE until COMMAND COMPLETE is activated, indicating completion of the head switch.

  - When performing a read following a write, READ GATE should not be activated for at least 500 nanoseconds after WRITE GATE is deactivated.

  - READ GATE must be deactivated when passing over a Write Splice. READ GATE must be deactivated a minimum of 100 nanoseconds (one bit time) before the Write Splice, and must remain deactivated for a minimum of 100 nanoseconds following the Write Splice (see figure 2-2).

  - READ GATE must be activated at least 14 bytes before the Sync Pattern byte.

- **DRIVE SELECTED.** The drive activates this signal within 250 nanoseconds after its drive selection address is valid (see figure 2-1). This signal is deactivated within 250 nanoseconds of being deselected by the controller.

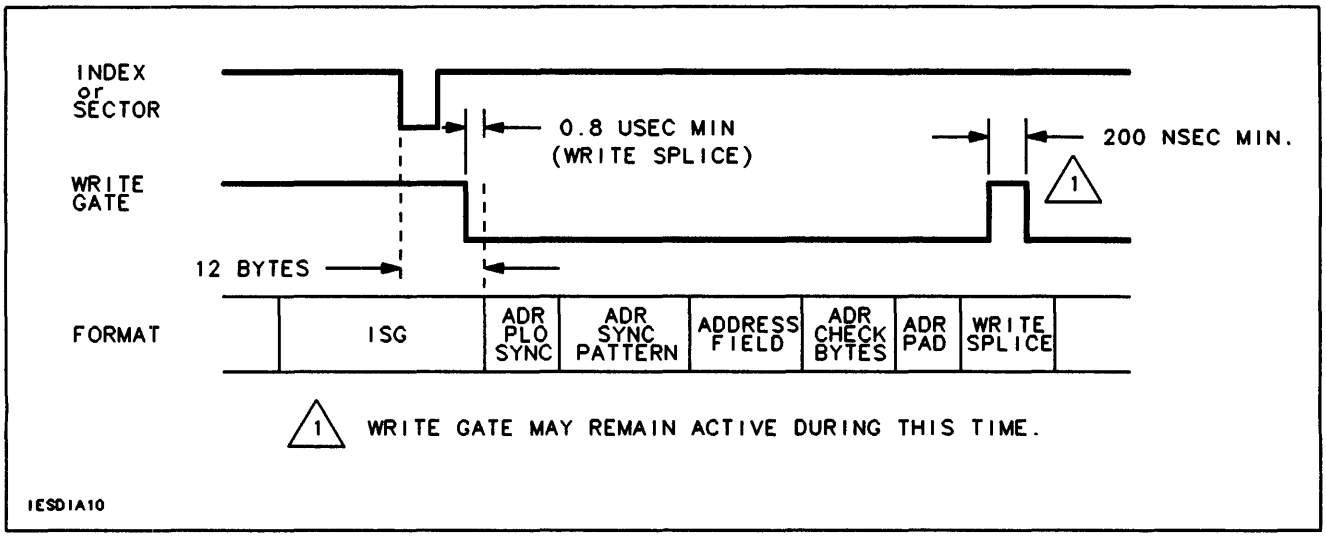


Figure 2-2. Write Gate Timing During Format

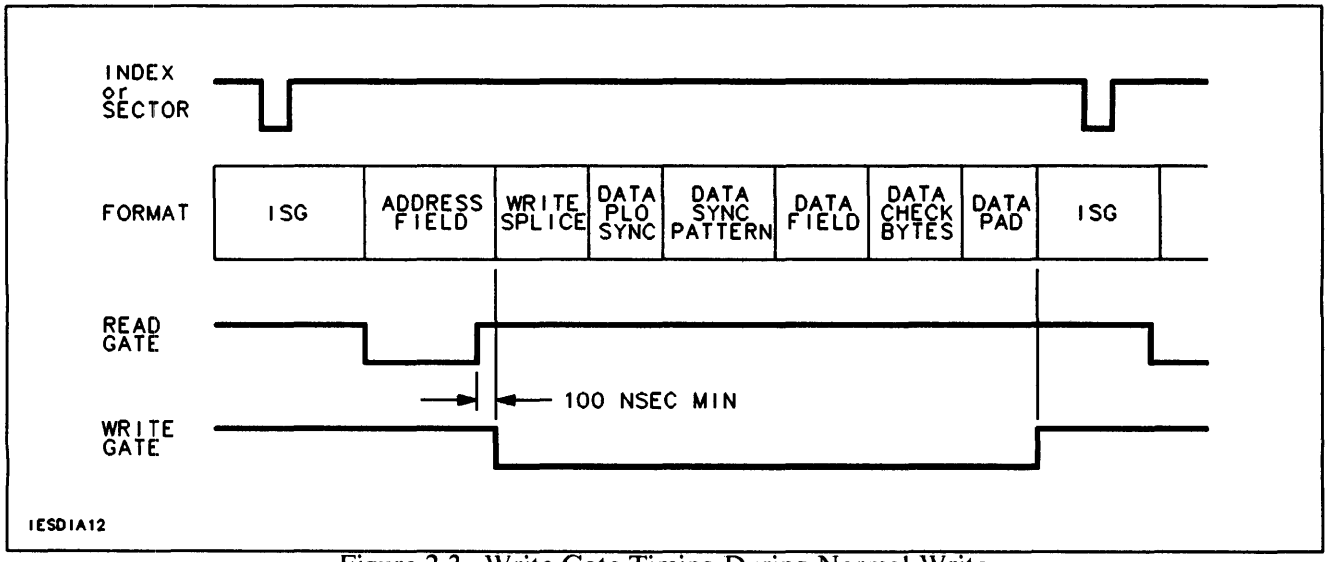


Figure 2-3. Write Gate Timing During Normal Write

- **READY.** This signal is used as defined in the ESDI specification.

- **COMMAND DATA.** The following commands are supported by the drive (refer to table 2-5):
  - Seek
  - Recalibrate
  - Request Status
  - Request Configuration
  - Select Head Group
  - Control (Reset Interface, Stop Spindle Motor, Start Spindle Motor)
  - Track Offset
  - Initiate Diagnostics

  All other commands and reserved command codes are treated as illegal commands.

- **TRANSFER REQUEST.** The TRANSFER REQUEST handshake timing is shown in figure 2-5.

- **ADDRESS MARK ENABLE.** This signal is not used. The drive will ignore any activity on this line.

- **TRANSFER ACKNOWLEDGE.** The TRANSFER ACKNOWLEDGE handshake timing is shown in figure 2-5.

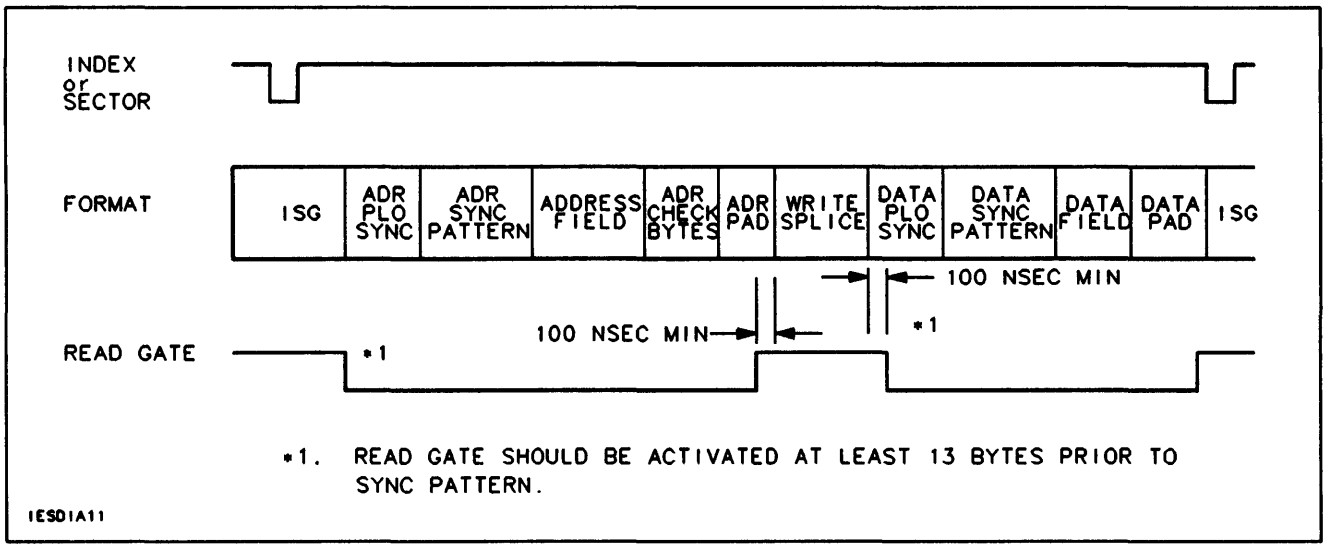


Figure 2-4. Read Gate Timing

- **ATTENTION.** There are no product-specific details for this signal.

- **INDEX.** The INDEX timing (relative to SECTOR) is shown in figure 2-6.

- **SECTOR.** The SECTOR timing (relative to INDEX) is shown in figure 2-6.

- **COMMAND COMPLETE.** There are no product-specific details for this signal.

- **DATA TRANSFER SIGNALS.** All four data transfer signals (NRZ WRITE DATA, WRITE CLOCK, NRZ READ DATA, READ CLOCK) conform to the timing requirements defined in the specification. There are no product-specific timing requirements associated with any of these signals.

- **TRACK OFFSET.** This command causes the disc drive to perform a track offset (±80 microinches) as specified by the command modifier bits. See figure 2-7 for track offset definition.

2-5. DRIVE OPERATING FEATURES

The following paragraphs explain specific operating features of the drive. The controller can exploit the full performance of the drive by utilizing these features.

2-6. DRIVE/HEAD SELECTION SEQUENCE

Before performing a data transfer with a drive, the controller may have to initiate up to three separate operations: drive selection, a seek to the desired track, and head selection. To optimize drive performance, these operations should be performed in the following order:

NOTE

Figure 2-8 illustrates the following sequence. The timing references (T0) used in the discussion refer to this figure. The drives used in the example have arbitrarily been assigned addresses of 1 and 2.

1) Deselect drive 1 (T0). The drive retains the selected head value in effect when the deselection occurs. This step is necessary only in multi-drive environments.

2) Set the head select lines to the value of the head currently selected on drive 2 (T1) with regards to 1, 2, or 3. The disc drive leaves Drive 1 selected all the time because there is no Drive 2 option.

3) Initiate a seek to the desired track (T3). The drive will deactivate COMMAND COMPLETE and begin the seek operation.

Table 2-5. CS/80 Command Implementation

COMMAND	IMPLEMENTED
Transparent Commands	
Universal Device Clear	yes
Amigo Clear	yes
Channel Independent Clear	yes
Selected Device Clear	yes
Cancel	yes
Loopback	yes
HP-IB Parity Checking	yes
Identify	yes
Real Time Commands	
Locate and Read	yes
Cold Load Read	yes
Locate and Write	yes
Write File Mark (tapes only)	no
Complementary Commands	
Set Unit (unit 0 and 15)	yes
Set Volume (volume zero only)	yes
Set Address (1 and 3 vector)	yes
Set Block Displacement	no
Set Length	yes
Set Burst	yes
Set RPS (Rotational Position Sensing)	no op
Set Retry Time	no op
Set Status Mask	yes
No Op	yes
Set Release	no op
Set Options	no
Set Return Addressing Mode	yes
General Purpose Commands	
Spare Block	yes
Describe	yes
Locate and Verify	yes
Release	no op
Release Denied	no op
Copy Data	no
Initialize Media	yes
Diagnostic Commands	
Request Status	yes
(refer to Table 2-7. Request Status Summary)	
Initiate Utility (refer to table 2-7)	
No execution message	yes
Device will receive execution message	no
Device will send execution message	yes

yes = Implemented as defined by CS/80
no = Will return illegal opcode if received
no op = Command ignored but parameters are checked. If the parameters are incorrect, then illegal parameter/bounds is returned.

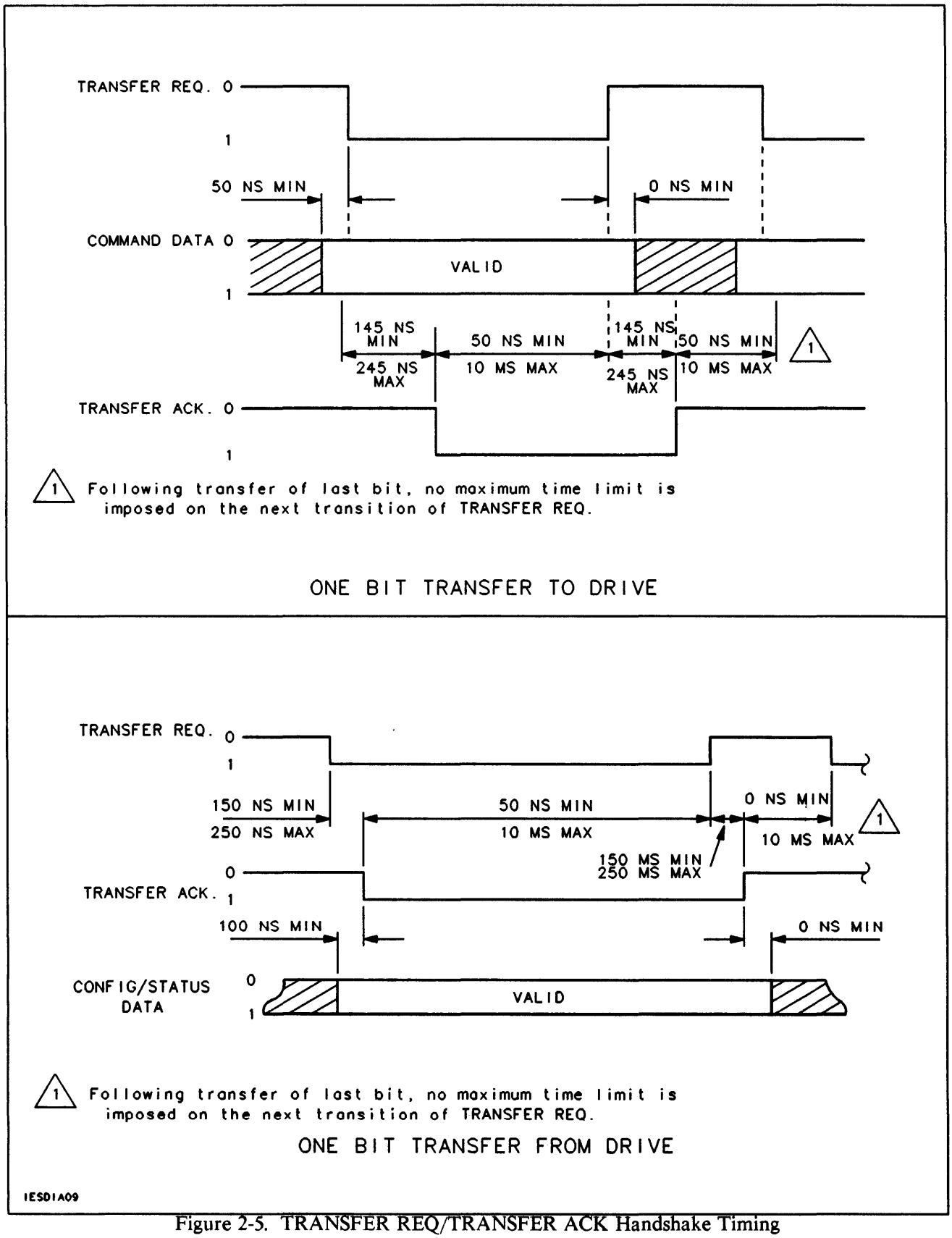


Figure 2-5. TRANSFER REQ/TRANSFER ACK Handshake Timing

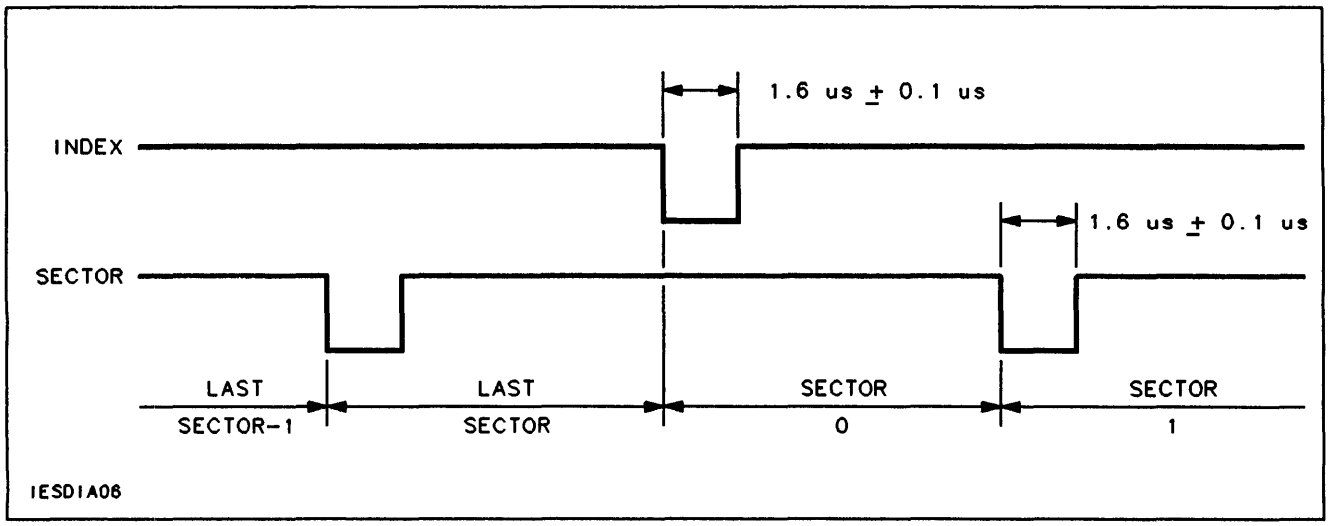


Figure 2-6. Index/Sector Timing

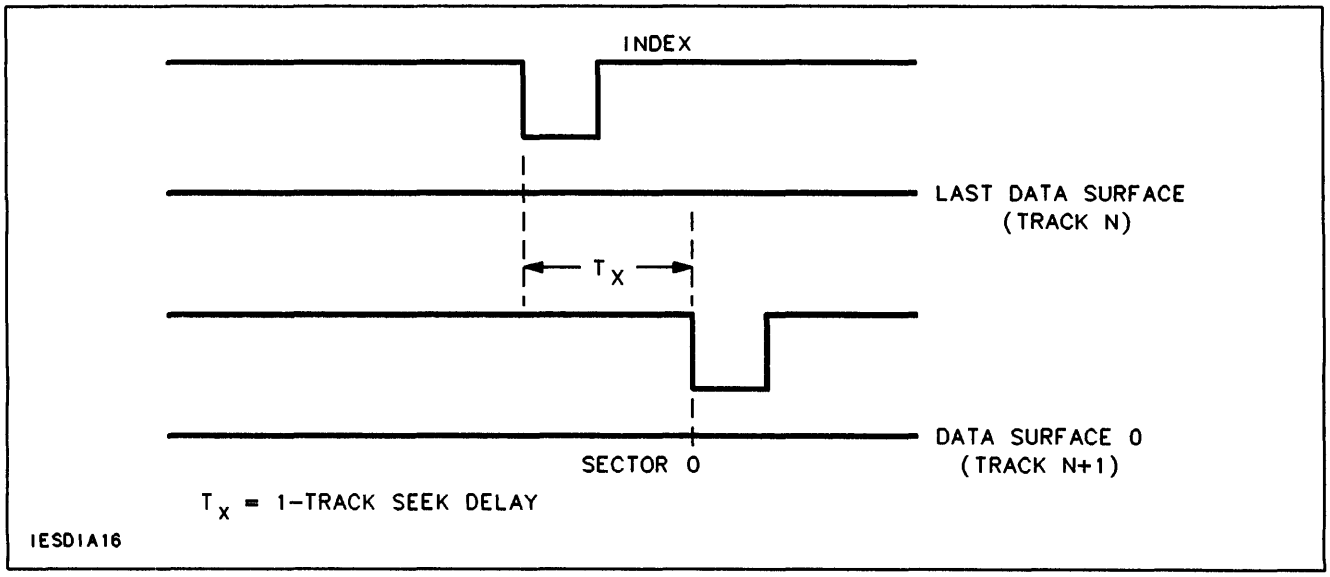


Figure 2-7. Track-To-Track Sector Offset

4) Before the seek completes (COMMAND COMPLETE activated), select the new head (T4). By changing the head select lines during the seek, the head switch operation is performed as part of the seek. If the seek operation completes before the controller changes the head select lines, the head select will be performed as a separate operation, resulting in an additional delay as the new head seeks to the target track.

5) When the newly selected head has arrived at the target track, the drive asserts COMMAND COMPLETE (T5). This sequence assumes that all three operations are necessary; however, it also applies to simpler situations. For example, if the controller wants to access a different track and data surface on the currently selected drive, only steps 3 and 4 would be required. The important element to recognize in this sequence is that when both a head switch and seek are required, the controller should always initiate the seek and then follow it immediately with the head switch. This avoids the additional delay incurred if the head switch is performed before or after the seek.

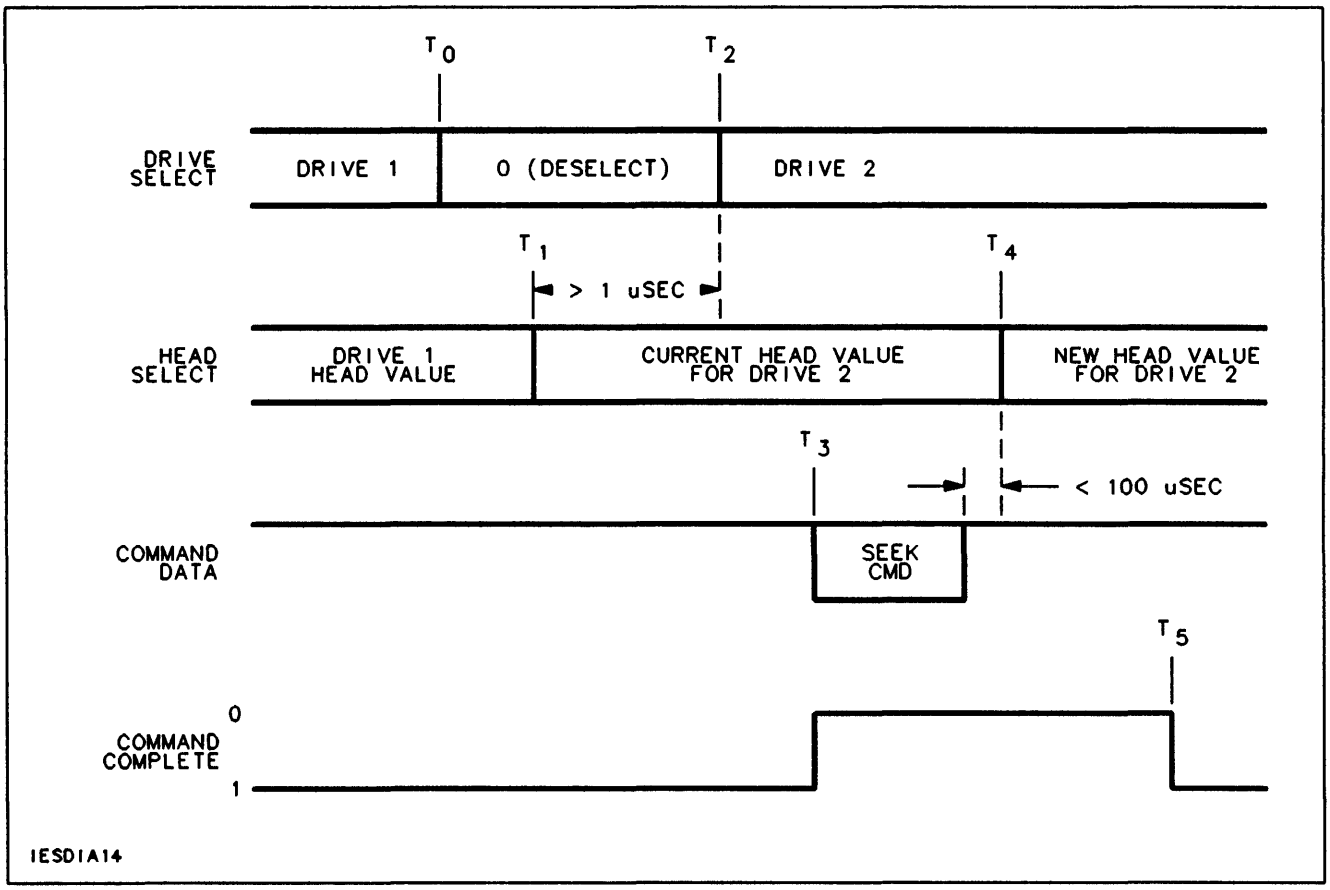


Figure 2-8. Recommended Drive/Head Selection Sequence

2-7. MEDIA FORMAT

The following paragraphs address the physical format of the disc media.

2-8. SECTOR FORMAT. The drive employs "hard sectoring" with the beginning of each sector defined by the occurrence of the SECTOR signal. The beginning of each track (sector 0) is defined by the INDEX pulse. Each sector is a minimum of 315 bytes long. Of 315 bytes, a minimum of 16 bytes are used for the intersector gap. The remaining 299 bytes of the sector are available for use by the controller. Although sector format is user-dependent, it is recommended that the format used conform to the fixed-sector format example contained in the ESDI specification.

2-9. SECTOR OFFSET. The sector offset also improves the performance of data transfers that include successive cylinders. When the end of a cylinder is reached, the drive must perform a 1-track seek to the next cylinder to continue the transfer (see figure 2-9). When switching from the last head of one cylinder to the first head (0) of the next cylinder, the track-to-track sector offset provides the delay necessary to avoid a rotational latency (see figure 2-7).

2-10. CS/80 COMMAND SET IMPLEMENTATION

Table 2-5 provides a listing of the CS/80 commands and their implementation on these disc drives. Table 2-6 provides a summary of the REQUEST STATUS Command and table 2-7 provides a summary of the Utility Commands.

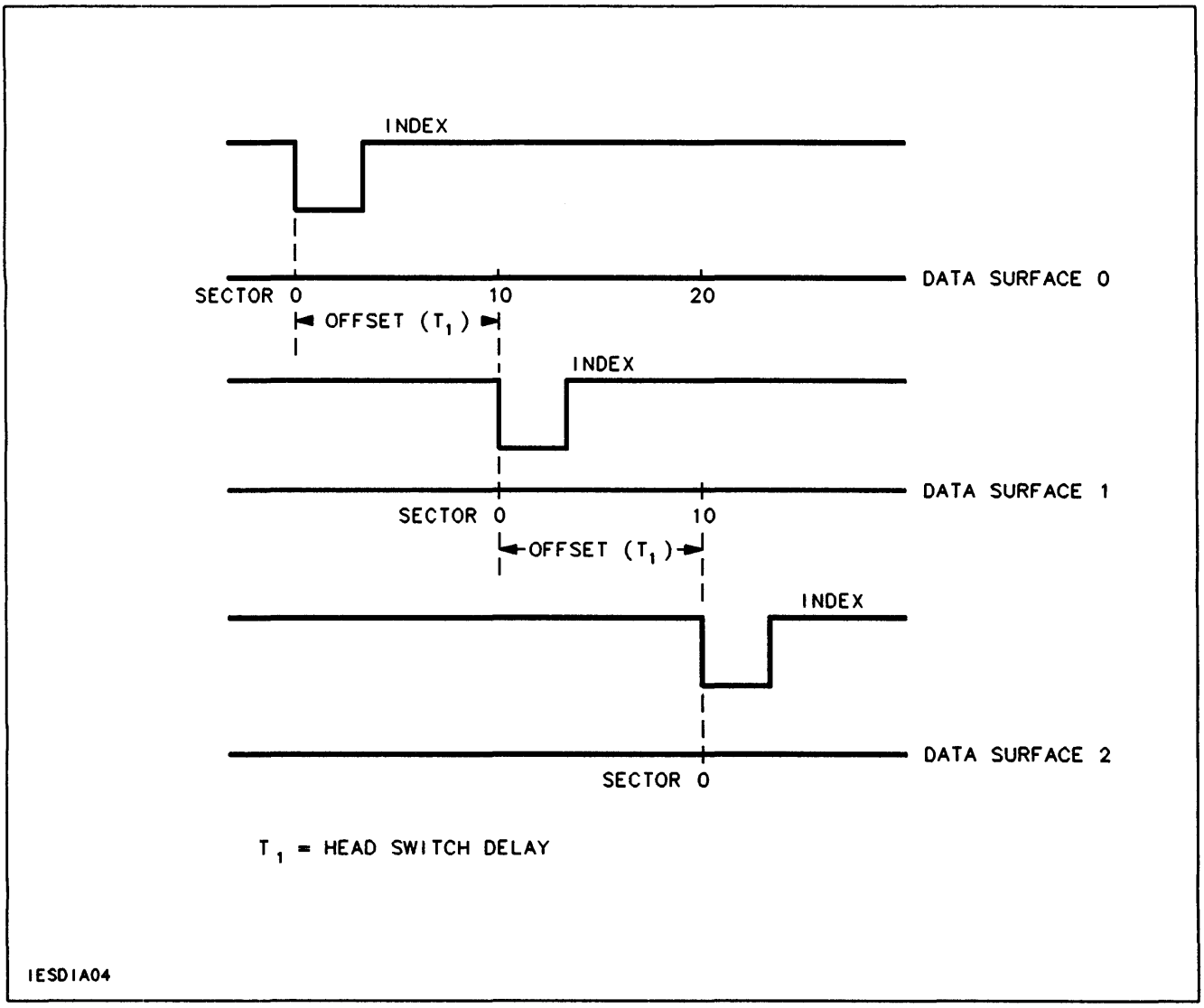


Figure 2-9. Sector Offset

Table 2-6. Request Status Summary

COMMAND	IMPLEMENTED
Reject Errors	
Channel Parity Error	yes
Illegal Opcode	yes
Module addressing (only volume 0 and unit 1 or 15 are supported)	yes
Address Bounds	yes
Parameter Bounds	yes
Illegal Parameter	yes
Message Sequence	yes
Message Length	yes
Fault Errors	
Cross-Unit (copy data not supported)	no
Controller Fault	yes
Unit Fault (set whenever a problem is detected in disc mechanism)	yes
Diagnostic Result (set when a failure occurs during a disc diagnostic)	yes
Operator Request (release never required)	no
Diagnostic Request (release never required)	no
Internal Maintenance (release never required)	no
Power Fail	yes
Retransmit	no
Access Errors	
Illegal Parallel Operation (only support 1 unit)	no
Uninitialized Media (formatted at factory)	no
No Spares Available	yes
Not Ready	no
Write Protect	no
No Data Found	no
Unrecoverable Data Overflow	yes
Unrecoverable Data	yes
End of File (only for tapes)	no
End of Volume	yes
Information Errors	
Operator Request (release never requested)	no
Diagnostic Request (release never requested)	no
Internal Maintenance (release never requested)	no
Media Wear	yes
Latency Induced	yes
Auto Sparing Invoked	yes
Recoverable Data Overflow	no
Marginal Data	yes
Recoverable	no
Maintenance Track Overflow	no

yes = bit will be set by the controller in response to an error as described by the CS80 manual
no = under no condition will this bit be set

Table 2-7. Utility Command Summary

No Execution Message

Clear Logs (run time/fault, error rate test)
Pattern Error Rate Test
Random Error Rate Test
Read Only Error Rate Test
Read Only Random Error Rate Test
Preset

Send Execution Message

Read Fault Log
Read Run Time Log
Read Error Rate Test Log
Measure Seek Time
Read Spare Table
Locate and Read Full Sector
Servo Test
Pattern Error Rate Test
Random Error Rate Test
Read Only Error Rate Test
Read Only Random Error Rate Test
Read ROM Revision number
Read Defect List

Receive Execution Message

No commands are implemented for this option.

Theory Of Operation 3

3-1. INTRODUCTION

The HP 7957 and HP 7958 Disc Drives are random access, mass storage devices intended for use with small and medium size computers. The formatted capacities of the HP 7957 and HP 7958 are 81 megabytes and 130 megabytes, respectively. In this chapter "disc drives" refers to both the HP 7957 and HP 7958, unless otherwise specified. The disc drive has three functional areas divided into three assemblies (see figure 3-5). The three assemblies are: the CS80/ESDI Controller [CEC] PCA-A2, the Disc Drive Assembly [HDA] PCA-A1, and the Power Supply PCA-A3.

The CEC (PCA-A2) provides CS/80 interface to the host and Enhanced Small Device Interface (ESDI) to the HDA. The CEC converts CS/80 commands to ESDI commands and vice versa. It also provides for error logging to the maintenance track. The CEC also initiates retries and error correction. It manages data transfers between the host and HDA and passes and executes host commands.

NOTE

The CEC also provides for error logging via an Electrical Erasable PROM (EEPROM). Instead of logging errors on the maintenance track these disc drives log errors (run time and faults) to the EEPROM.

The HDA (PCA-A1) contains a sealed disc drive assembly which contains a sealed head-media module, a preamp PCA, a motor control PCA and a device electronics PCA. The HDA provides the means of storing data, converting NRZ code to Run Length Limited (2,7 RLL) code, write fault detection, motor control and braking.

The head-disc module in the HDA is sealed and uses three (HP 7957A) and five (HP 7958A) 130-millimetre (5.12-inch) diameter nonremovable discs. One read/write head is used for each disc surface. The bottom surface of the lowest disc in the stack contains continuous prerecorded servo data which is used to ensure the precise positioning of the read/write heads.

The power supply (PCA-A3) provides regulated +5V and +12V to the CEC and HDA.

Two LED's (red and green) on the front panel provide information on the disc drive status (see figure 4-6).

3-2. CS80/ESDI CONTROLLER [CEC] PCA-A2

The three major functional areas of the CEC (see figure 3-5) are the HP-IB Interface IC, the Disc Data Controller (DDC) IC and the microprocessor (μP) IC. There are two major buses in the CEC; the Direct Memory Access (DMA) bus and the μP Bus.

The DMA bus is divided into two buses; upper DMA bus and the lower DMA bus. This is to allow both 8-bit and 16-bit transfers. The HP-IB Interface IC is an 8-bit device and the DDC is a 16-bit device.

The EOI detect block looks for the byte tagged EOI and sends a signal to the DMA Bus Arbiter. The DMA Bus Arbiter, which controls all access to the DMA bus, inhibits any further transfer of information from the HP-IB Interface IC and the buffers.

Buffer 0 and Buffer 1 are 8k by 8 RAM's. Information is passed between the HP-IB Interface IC and the buffers 8-bits at a time.

All odd bytes are transfer to Buffer 1 and all even bytes are transferred to Buffer 0. Transceiver 1, between the DMA bus and Buffer 1, is controlled by the DMA Bus Arbiter, and is turned off for all even byte transfers. Information passed between the buffers and DDC is 16-bits at a time and both buffers are active at this time.

The DDC provides the ESDI Interface to the HDA. It has an internal programmable error correction code (ECC) circuit. It also provides serialization/deserialization of all data and performs all internal control and timing.

The ESDI PAL circuit is a programmable logic array that provides the proper delay to the read gate to prevent the read gate from being asserted over a write splice when writing headers (sparing operation) or when formatting.

The microprocessor (μP) controls the disc drive operations by using the firmware contained in the 32k by 8 ROM. The μP uses the 2k x 8 RAM for holding variables and stacks. Access to the ROM and RAM is on the μP Bus.

The Control Bit Register and Status Bit Register are accessed by the μP via the μP Bus. The output of these two registers process the signals across the ESDI interface between the CEC and HDA. The output of the Control Bit Register logs fault and run time information in four contiguous sectors on physical cylinder 0. The fault log has capacity for logging 46 errors. The run log has capacity for logging 50 errors.

NOTE

The output of the Control Bit Register logs fault and run time information into the X2024 EEPROM. The EEPROM is used in place of a maintenance track. The EEPROM holds the last 50 detected fault and run time errors.

The index pulse is fed to the green LED counter which is a divide-by-4 counter. The output of the LED counter drives the front panel green and red LED's.

3-3. TRANSFERS

There are three types of transfers on the CEC. Two transfers, local and remote are on the DMA bus and the third transfer, μP transfer, is when the μP accesses the DMA bus. The transfers are handled on a priority basis with the local transfer having the first priority and the remote transfer having the last priority.

The local transfer is for transfer of information between the DDC and the buffers. The μP transfer is for transfer of information between the μP and DMA bus. The remote transfer is for transfer of information from the HP-IB Interface IC and the buffers. Paragraphs 3-43, 3-44 and 3-45 provide the sequence of events for each transfer. See figure 3-6 when using the transfer sequence paragraphs.

3-4. DISC FORMAT

The plated metal discs in the HDA PCA-A1 provides five data surfaces (HP 7957A) or eight data surfaces (HP 7958A) each with one read/write head. One surface contains prerecorded servo data and is accessed by the servo head.

Each surface is divided into 1024 concentric circles called tracks (see figure 3-1). From the outside diameter these are: one self-test track, one guard track, 1013 data tracks, six spare tracks, one guard track, one self-test track, and a landing zone.

The two self-test tracks are used to test reading and writing. The 1013 data tracks are used for reading and writing data. This provides the user with 1013 cylinder addresses. The six spare tracks are used for sparing out tracks containing hard errors.

Each data track is organized into smaller sequential numbered blocks of data called sectors. Each track has 63 sectors plus one spare sector (see table 3-1). Figure 3-2 shows the sector format, based on 63 data sectors, each having 256 bytes of data information. The beginning of each sector is identified by an address area which contains the physical sector address plus cylinder and head information.

Each address area contains sync bytes to ensure read and write operations happen in the proper time sequence. Each section is separated by a minimum 16-byte intersector gap.

The 5th byte of the address field is the Flag Status byte. This byte is used by the controller for sector and track sparing information. Table 3-4 shows the values of the Flag Status byte for various conditions.

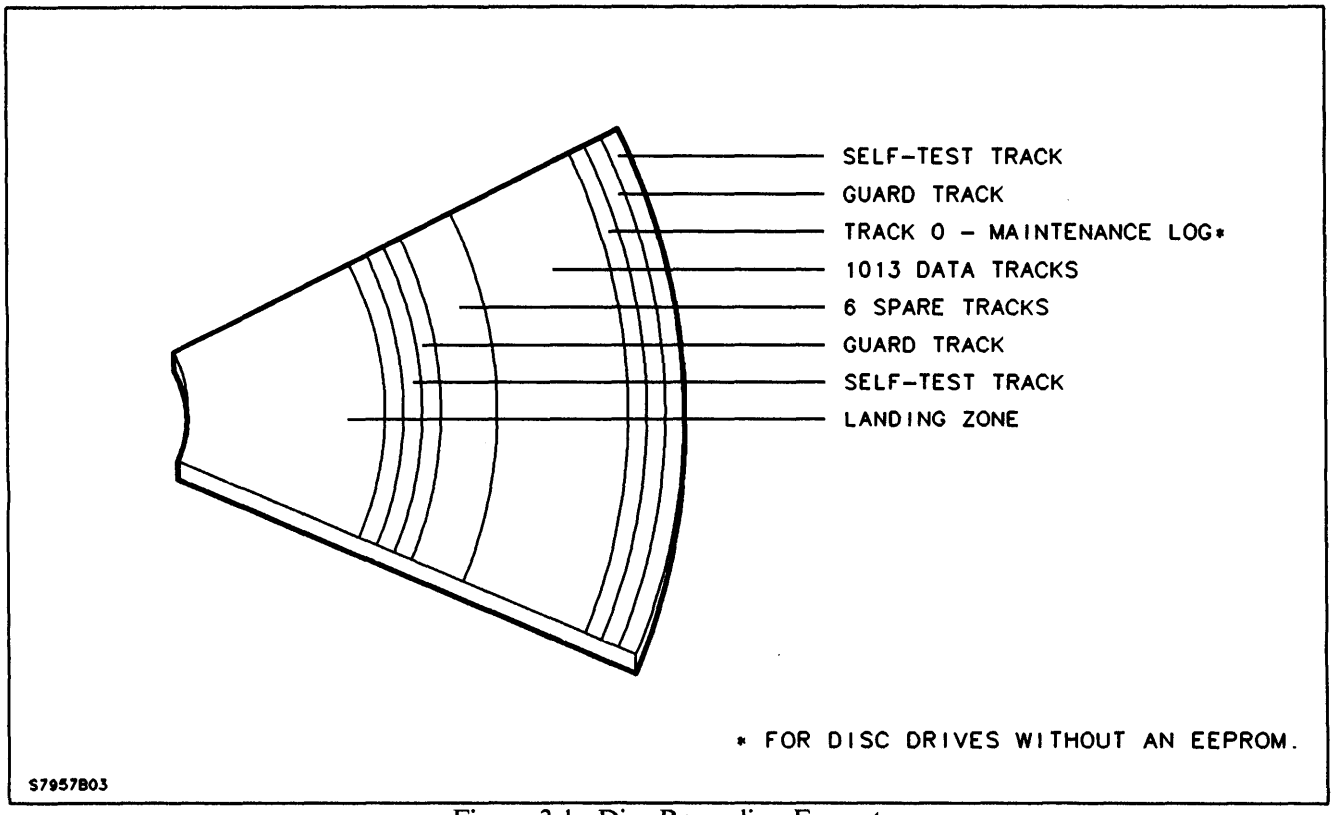
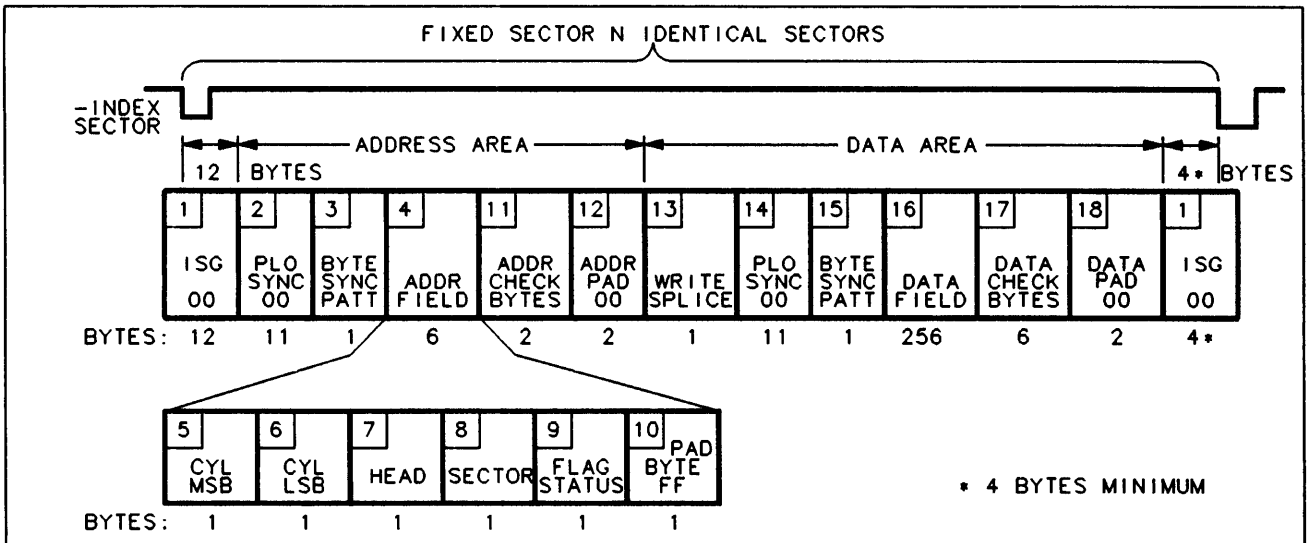


Figure 3-1. Disc Recording Format

Table 3-1. Disc Drive Capacity

	Data Bytes Per	Sectors Per	Tracks Per	Heads Per
Sector	256			
Track	16,128	63		
Head	16,337,664	63,819	1013	
HP 7957A	81,688,320	319,095	5,065	5
HP 7958A	130,701,312	510,552	8,104	8
There is one spare sector per track and six spare tracks per head.				



1	Intersector Gap	– bytes used for sector separation
2	PLO Sync	– 11 bytes for phase-and frequency-synchronization with data bits recorded on media
3	Byte Sync Pattern	– 1 byte indicates beginning of address field information
4	Address Field	– 6 bytes
5	Cylinder MSB	– 1 byte cylinder most significant bit
6	Cylinder LSB	– 1 byte cylinder least significant bit
7	Head	– 1 byte for head address
8	Sector	– 1 byte for sector address
9	Flag Status	– 1 byte for status byte
10	Pad Byte	– Loaded With FF
11	Address Check Bytes	– 2 bytes for verifying address field when address field is read
12	Address Pad	– 2 bytes for field address check codes for file integrity
13	Write Splice	– 1 byte allows internal circuits sufficent time to ensure data recovery. Controller sends 00 at this time
14	PLO Sync Bytes	– 11 bytes required when reading to allow circuits to become phase and frequency synchronized with data bits on media. Controller sends 00 at this time.
15	Byte Sync Pattern	– 1 byte to establish byte synchronization and indicates beginning of data field
16	Data Field	– 256 bytes of data
17	Data Check Bytes	– 6 bytes for error correction code (ECC) information
18	Data Pad Bytes	– 2 bytes to ensure proper recording and recovery of lost bits of data check bytes. Controller sends 00 at this time.

S7957A02

Figure 3-2. Sector Format

3-5. SPARING

There are two sparing sequences available. One is sector sparing and the other is track sparing. Each track contains 63 data sectors plus one spare sector. The second sector spare operation on a track generates a track spare operation. Each data head has six available spare tracks. There is no cross head sparing allowed.

If 1 or 0 spares are available after a sparing operation, the "media wear" bit (bit 51) in the CS/80 status word will be set. If a track sparing operation is attempted with no available spares, the "No Spare Available" bit (bit 34) is set.

3-6. SEQUENCE

The sparing sequence is as follows:

- The host issues a Spare Block command.
- The drive seeks to track with defective sector.
- The drive reads a sector header and looks at the Flag Status Byte (refer to table 3-4) to determine if sector sparing has occurred.
- If sector sparing is available, then sector sparing is attempted.
- If sector sparing is unavailable, then track sparing is attempted.

3-7. SECTOR SPARING

A sector sparing operation is as follows:

- The disc drive performs write then read error rate test (WTR ERT) seven times on the spare sector using the random pattern table.
- If the WTR ERT fails the track is spared.
- If the WTR ERT, passes the track data is read (to Buffer 0 and Buffer 1) except for the bad sector.
- Unrecoverable errors on any other sector will cause the sparing operation to terminate and an unrecoverable error will be reported.
- The disc drive then writes the bad sector header with the defective sector number 255 (FF) and subsequent sectors are numbered sequentially starting with the sector being spared. Data is written to the track.
- The defective sector's data field is filled with zeros.

3-8. TRACK SPARING

- The disc drive looks up the next available spare track in RAM.
- It seeks to the spare track.
- If the seek fails, the spare track is flagged as bad in the spare track table. The sparing operation is terminated and a Unit Fault is reported in the CS/80 status.
- If the disc drive seeks to the correct track, a WTR ERT is initiated seven times on sectors 0 through 62 using the pattern table.
- If WTR ERT fails, a sector sparing operation is initiated.
- The WTR ERT is initiated again (seven times).
- If WTR ERT fails again, the disc drive looks up the next spare track in the spare table and repeats the previous five steps.
- If the second spare track fails, the sparing operation is terminated and a Unit Fault is issued in the CS/80 status.
- If the WTR ERT passes, data is read (to Buffer 0 and Buffer 1) from the defective track.
- If any errors, other than the defective sector, are detected the sparing operation fails and an unrecoverable error is reported.

- A new header and the data is written to the spare track.
- Sector headers contain the logical address of the defective track and the sector spare bits will show that no sparing has been done.
- The defective track is formatted with its physical track number. (Physical addresses have the most significant bit (msb) of the cylinder address set to 1 to differentiate them from the logical addresses (refer to table 3-4).
- The spare track table is updated.

3-9. ERRORS

3-10. ERROR DEFINITION

Recoverable errors are errors that are corrected on the first retry. Marginal errors are errors that are corrected after the first retry or by the error correction code (ECC). If an error is greater than 12 bits and/or there are two bad locations in a sector; ECC cannot correct this and the sector is considered unrecoverable.

3-11. ERROR LOGS

The information in the logs is defined as follows:

ERT LOG -
Correctable (recoverable and marginal) errors
Uncorrectable errors

RUN TIME LOG -
Correctable (marginal) errors
Uncorrectable errors

3-12. ERROR DETECTION AND CORRECTION

Error detection is implemented during run time and during diagnostics. Error correction is implemented only when errors are detected during run time and the error is not correctable during retries. The run time error detection and correction sequence is described as follows:

- An error is detected on read by the ECC circuits inside the DDC.
- Retries are initiated.
- On each retry, data is read and checked by the ECC circuits.
- The first retry is done on track center.
- The retry is then done one time with a +80 microinch offset; then one time with a -80 microinch offset.
- If the data is unreadable during each retry the disc drive loops back with one retry on track, one retry with +80 microinch offset, one retry with -80 microinch offset for a total of 36 retries.
- If a correct read cannot be accomplished with the retries (a total of 36 retries for 800 ms), ECC is invoked to correct up to 12 bits.
- If the error is greater than 12 bits and/or there are two bad locations in a sector, ECC cannot correct this and the sector is considered unrecoverable.

During WRT ERT testing a pattern is written to the track and then read back. If an error is detected the retries are initiated as follows:

- The disc drive makes 12 retries on track center.
- If the data is not read correct with the first 12 retries 12 more retries are made with a +80 microinch offset.
- If the data is not read correct with the first two sets of retries then 12 more retries are initiated with a -80 microinch offset.

If the data is not read correctly with the retries (36 retries for 800 ms) an error is recorded in the log.

3-13. DISC DRIVE PCA-A1

The Disc Drive PCA-A1 consists of a mechanical assembly and three printed circuit boards (see figures 3-3 and 3-4).

3-14. DRIVE MECHANICS

The mechanical portion of the disc drive consists of a die-cast frame and a Head/Disc Assembly [HDA]. The HDA is suspended within the frame on shock isolators/absorbers. This method of construction protects the HDA from mechanical shock and stresses associated with mounting the drive in a system enclosure.

The HDA consists of a die-cast base, sealed to form a clean area that contains virtually all the drive's mechanical components. Air is circulated through the clean area by disc-rotation induced flow. The circulating air is passed through a filter. For pressure equalization, the clean area "breathes" to the outside via another filter.

Inside the clean area are three or five magnetic discs (depending on the model); the servo head and from five or eight recording heads (again, depending on the model); and the rotary voice-coil positioner. The surface of the disc that is nearest the die-cast base is used for servo track information. The discs are driven by a direct-coupled brushless DC motor which mounts on the outside

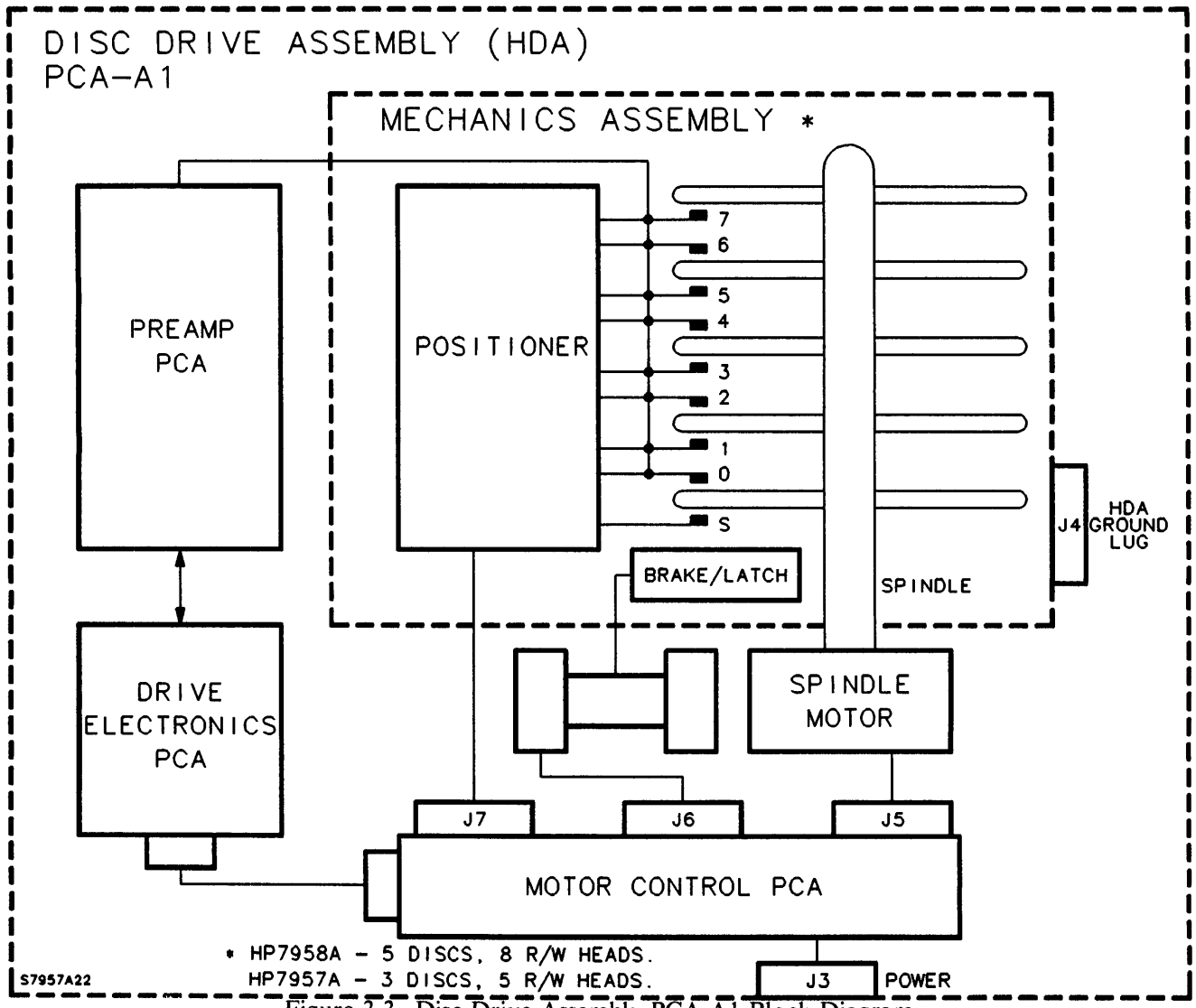


Figure 3-3. Disc Drive Assembly PCA-A1 Block Diagram

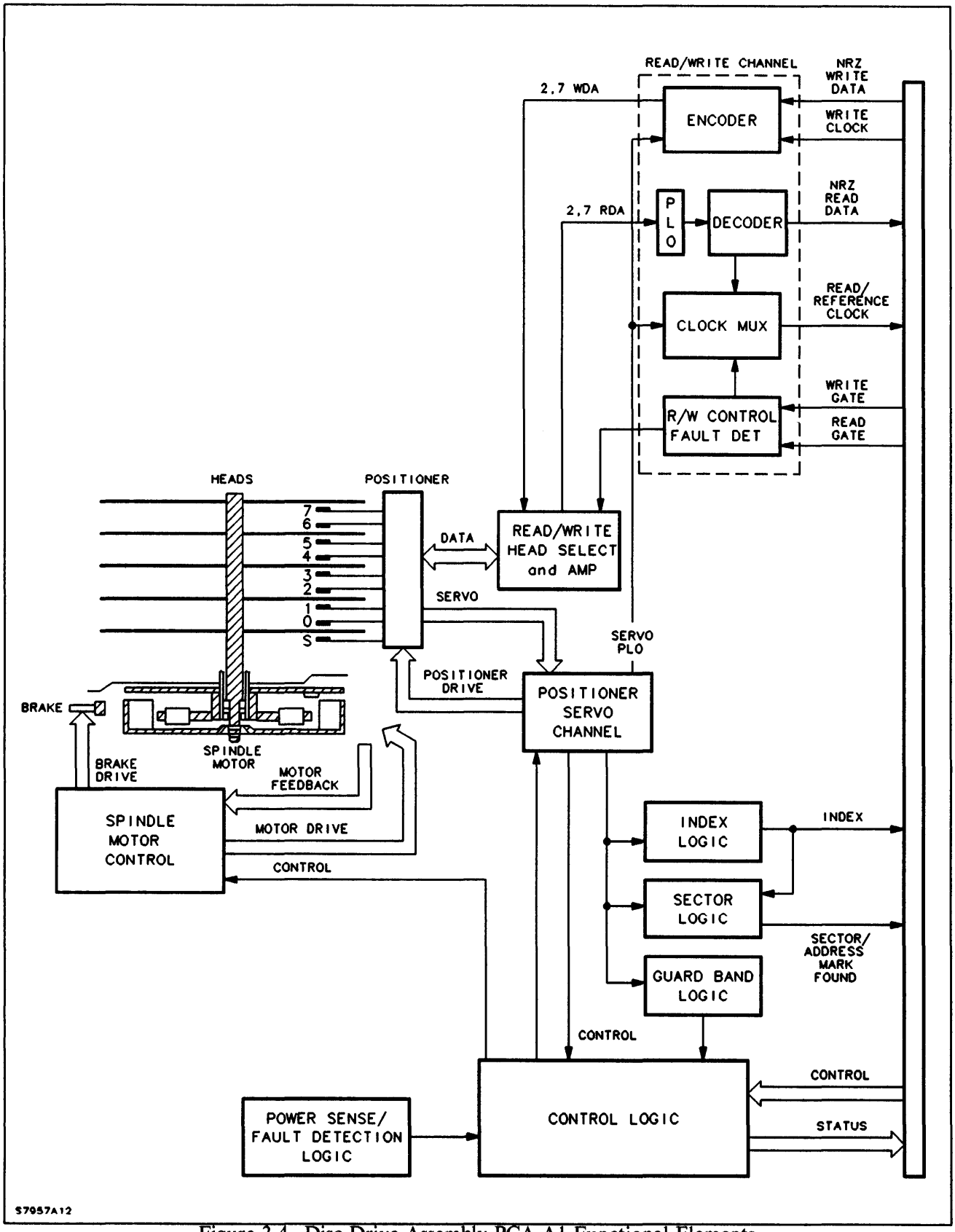


Figure 3-4. Disc Drive Assembly PCA-A1 Functional Elements

of the base, along with the brake mechanism. Switching information for the electronic commutator is supplied by three Hall-effect sensors positioned within the motor assembly.

3-15. PREAMPLIFIER BOARD

Electrical connection to the heads and the positioner is made via flexible circuits which pass through a port in the HDA casting. The port is sealed with a gasket to maintain the integrity of the clean area. The flexible circuits then connect to the Preamplifier board mounted on the HDA casting. The Preamplifier board contains the The servo signal preamplifier IC and the read/write preamplifier IC. The read/write preamplifer IC contains the read signal preamplifier circuits, head select circuits and write current drivers.

- Head selection (for up to eight data heads).
- Read signal preamplification.
- Servo signal preamplification.
- Write fault detection.

3-16. MOTOR CONTROL BOARD

The electronic components associated with the DC Motor and with the servo power amplifier circuit for the positioner are mounted on the Motor Control board. The board provides the following functions:

- Spindle motor commutation, current limiting, and control.
- Positioner signal power amplification.
- Brake solenoid control.
- DC power filtering and reference voltage generator.

3-17. DEVICE ELECTRONICS BOARD

The remaining electronic components are mounted on the Device Electronics board, which provides the overall control functions for the drive. The board contains microprocessor-based control logic and interface drivers and receivers. The board provides the following functions:

- Power-up and power-down sequencing.
- Spindle speed control to ±0.5 percent accuracy.
- Servo signal amplification, AGC, and demodulation.
- Closed loop positioner servo.
- Velocity profile generation.
- Read channel signal processing.
- Fault detection.
- Index, Guardband, and Track 0 decoding.
- Write data encoding.
- Data separation and read data decoding.
- Index and sector pulse generation.

3-18. READ/WRITE FUNCTIONAL DESCRIPTION

3-19. WRITE CHANNEL

When the drive is selected and in the write mode, data to be written is received over the drive interface via balanced, differential data lines NRZ WRITE DATA± with timing provided by the Write Clock signal. Write data is transmitted from the controller to the drive as a serial binary data stream with a clock signal. Data is encoded (from NRZ data to 2,7 RLL data), and then applied to the Read/Write Head Select circuit. A flip-flop, internal to the control circuit, is clocked by the data pulses. Each time the flip-flop changes state, the write drivers in the control circuit switch the head

current thereby recording magnetic dipoles on the disc.

The microprocessor-generated inner zone signal is asserted when the positioner is within the inner range of tracks (i.e., track numbers greater than 511). This signal selects the lower of two values of write current. The lower value of write current is selected because the recorded linear bit density on the inner tracks is higher than on the outer tracks. The lower value of write current improves resolution.

3-20. READ CHANNEL

When the drive is selected and the interface Read Gate signal is true, low-level read signals from the selected data head are amplified. Since read data is represented by the time position of the read signal's peak and since the peak is difficult to sense directly, the read signal is differentiated to produce a signal that changes state at the peak. As a result, each peak corresponds to a "zero crossing." Next, the differentiated signal is filtered to remove high-frequency noise and minimize distortion. Then the signal is digitized and applied to a pulse-former circuit, which generates the Read Data signal. The read data is decoded (from 2,7 RLL data to NRZ data) and passed to the controller via balanced, differential data lines NRZ Read Data± with its associated read clocks transmitted via the Read/Reference Clock±.

3-21. READ/REFERENCE CLOCK MULTIPLEXER

When Read Gate is not asserted, Read/Reference Clock signal is switched to Reference Clock, which is Servo PLO divided by 2.

When Read Gate is asserted, the read data separator PLO is synchronized to the preamble data, and the Read/Reference Clock signal is switched to the Read Clock.

3-22. READ/WRITE HEAD SELECT. The Read/Write Head Select circuit controls up to eight data heads. Functions included in the circuit are:

- Head selection matrix
- Read/write switching logic
- Read preamplifier
- Write drivers
- Write Unsafe detection logic

The head address is determined by three interface head Select lines ($HS2^3$ is not used in this disc drive). The address is decoded by the Read/Write Head Select circuit (refer to table 3-2).

Table 3-2. Head Selection

$HS2^3$	$HS2^2$	$HS2^1$	$HS2^0$	HP7957A	HP 7958A
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	2	2
0	0	1	1	3	3
0	1	0	0	4	4
0	1	0	1	-	5
0	1	1	0	-	6
0	1	1	1	-	7

The write enable signal is tied to the read/write head select circuit. When Write Enable is asserted, the circuit operates in the write mode. When Write Enable is inactive, the circuit operates in the read mode.

- In the write mode, the write current source in the read/write head select circuit is enabled. Encoded write data is passed into the circuit as a stream of digital pulses. The write drivers, under control of the write data input, switch current between the two head windings.

- In the read mode, encoded read data from the selected head is amplified and is then passed to the read channel on the device electronics board.

If a circuit malfunction causes the loss of write transitions or if a head shorts or opens, the Write Unsafe Detector in the read/write head selection circuit asserts the Unsafe signal, which is applied to the read/write control logic on the device electronics board. The drive alerts the controller by asserting the interface Attention signal and sending status information via the appropriate Standard Status bits and Vendor Unique Status Response bits. All writing is inhibited.

3-23. POWER SUPPLY ASSEMBLY PCA-A3

Power Supply Assembly PCA-A3 develops dc operating voltages from the ac line voltage and distributes these voltages throughout the disc drive. The power supply assembly also generates a power-on reset signal.

Power Supply Assembly PCA-A3 is a self-contained switch-mode power supply mounted on a printed-circuit assembly (see figure 4-4). Located in the assembly are all of the ac line voltage components including the line cord connector, line fuse, line voltage selector switch, line on/off switch, and line filter. Output voltages are +5 Vdc, +12 Vdc, and -12 Vdc. (The -12 Vdc output is not used in the HP 7957A and HP 7958A Disc Drives.) The power supply output voltages and power-on reset signal can be measured at test points at the front of PCA-A3 (see figure 3-6). The output voltages are not adjustable. The power supply voltages are connected to CEC PCA-A2 and Disc Drive Assembly PCA-A1 via cable assembly W1.

The following paragraphs provide a more detailed description of the Power Supply Assembly PCA-A3 circuitry, as shown in figure 3-6. Refer to table 3-3 for a description of the mnemonics used in figure 3-6, and to figure 4-4 for detailed voltage and signal distribution information.

3-24. AC INPUT CIRCUITS

The ac line voltage is connected to Power Supply Assembly PCA-A3 through a printed-circuit assembly (PCA) mounted ~AC LINE connector. A PCA-mounted ac line on/off switch controls both sides of the ac line into the power supply. The switch is operated by a LINE~ pushbutton projecting through an opening on the front panel of the disc drive. There is a fuse in the line side of the ac input following the power switch. The fuse value is the same (3A, 250V) for both 115-Vac and 230-Vac inputs. A line filter following the fuse reduces the level of line transients entering the power supply and the amount of switching noise leaving the power supply.

Also associated with the input circuitry is a VOLTAGE SELECTOR switch which selects line voltages of 115 Vac or 230 Vac. When the switch is in the 115 Vac position, a surge voltage protection device protects the power supply from damage if it is inadvertently connected to 230 Vac.

3-25. SWITCH-MODE SUPPLY

The switch-mode supply consists basically of an ac-dc converter and a flyback-mode dc-dc converter. The ac-dc converter rectifies and filters the ac line voltage. This filtered dc operating voltage is supplied to the dc-dc converter. Included in the ac-dc converter are two thermistors that limit the initial power-on surge current to approximately 25 amperes peak at 115 Vac and 230 Vac. The dc-dc converter chops the dc input into time-varying voltages, transforms them to lower levels and filters the outputs to supply the desired dc voltages of +5, +12, and -12 Vdc.

3-26. POWER-ON RESET

The power-on reset circuit is activated by the +5V output from Power Supply Assembly PCA-A3 and produces Power Valid signal PVAL. At power on, PVAL remains low for at least 100 milliseconds after the +5V output reaches 4.75V or higher. Signal PVAL then goes to a high level. Signal PVAL will also go low for at least 500 microseconds prior to the +5V going below 4.75V. Signal PVAL can be monitored at a test point on the front of power supply PCA-A3 (see figure 4-4). PVAL is connected to CEC PCA-A2.

3-27. SUMMARY OF WRITE DATA OPERATION

Data is transferred from the host to the HP-IB Interface IC over the HP-IB bus.

The data is transferred by DMA from the HP-IB Interface IC to the buffers. This is referred to as a remote DMA transfer.

The data is transferred by DMA from the buffer to the DDC. This is referred to as a local DMA transfer.

The data is serialized in the DDC and transferred to the Disc Drive Assembly [HDA] PCA-A1. The DDC generates the ECC (or Cycle Redundancy Check [CRC]) bytes as it transfers the data to the Disc Drive Assembly [HDA] PCA-A1.

3-28. SUMMARY OF READ DATA OPERATION

Data is transferred from the Disc Drive Assembly [HDA] PCA-A1 to the DDC and deserialized in the DDC. The DDC generates the ECC (or CRC) bytes at the same time that the data is transferred into the DDC.

The data is transferred by DMA from the DDC to the buffers. This is referred to as a local DMA transfer.

The data is transferred by DMA from the buffers to the HP-IB Interface IC. This is referred to as a remote DMA transfer.

The data is transferred from the HP-IB Interface IC to the host over the HP-IB bus.

3-29. CEC FUNCTIONAL THEORY

The CS80/ESDI Controller (CEC) PCA-A2 controls the data transfer between the HP-IB host computer implementing the CS/80 instruction set and the Disc Drive Assembly [HDA] PCA-A1 implementing the ESDI interface standard. Data which is transferred between the HDA PCA-A1 and the host passes through the CEC where it is buffered and changed to the correct format required by its destination. The format of the data which is transferred between the HDA and the CEC is serial NRZ. Data transferred between the host and CEC is over the HP-IB interface. The CEC performs the following tasks.

- Receives high level disc control commands (such as locate and read and locate and write) from the host computer, and performs the low level tasks necessary to execute these commands.
- Ensures that only error free data is passed back to the host by performing retries and error correction.
- Provides high level status reports to the host.
- Logs error and fault information.
- Performs self test at power on.

3-30. BUS STRUCTURE

The CEC is made up of two buses, the microprocessor bus and the DMA bus (see figure 3-6). The DMA bus is used to transfer data between the host and the HDA. These transfers are controlled by DMA circuitry in the DDC. The data buffers consist of 16 kbytes of static RAM divided into two buffers (Buffer 0 and Buffer 1).

The DDC controls data transfers between the HDA and the CEC. The HP-IB Interface IC controls data transfers between the host and CEC.

The microprocessor bus is made up of the microprocessor, ROM, RAM, Control Bit Register and Status Bit Register. The microprocessor bus lines are isolated from the DMA bus lines by Transceiver 2. Transceiver 2 allows the microprocessor to access the devices on the DMA bus when required. It also isolates the two buses so a data transfer can be taking place at the same time the microprocessor is performing other tasks on the microprocessor bus.

The DMA bus handles the transfer of data between the host computer and the HDA. Data which is to be written to the HDA is transferred to the HP-IB Interface IC, to the buffers, and then from the buffers to the DDC. The DDC then transfers data serially to the HDA. When reading data from the HDA, the data follows the same path but in the opposite direction.

The DMA line consists of two halves; an upper (most significant) bus and a lower (least significant bus. The buffers connected to the bus consist of two 8k bytes by 8 static RAMs. Buffer 0 is connected directly to the lower DMA bus. Buffer 1 is isolated by Transceiver and is on of the upper DMA bus.

Data transfers between the DDC and buffers are 16 bits wide. Both buffers are accessed at the same time. This is referred to as a local DMA transfer. Transceiver 2 (on the microprocessor bus) is disabled during local DMA transfers.

Data transfers between the buffers and the HP-IB Interface IC are 8 bits wide. During transfers, only one buffer is accessed. When Buffer 1 is accessed, Transceiver 1 is enabled and when Buffer 0 is accessed Transceiver 1 is disabled.

The microprocessor can also access devices on the DMA bus. Transceiver 2 is enabled during these transfers. When the microprocessor accesses the HP-IB Interface IC, DDC or Buffer 0, Transceiver 1 is disabled. When the microprocessor accesses Buffer 1, Transceiver 1 is enabled. Transfers to and from the microprocessor are 1-byte long.

3-31. MICROPROCESSOR DATA BUS

The following devices reside on the microprocessor data bus:

- Microprocessor
- 32k by 8 ROM for program memory
- 2k by 8 static RAM for microprocessor
- Control Bit Register
- Status Bit Register
- Transceiver 2 for DMA bus interface

The microprocessor is an 8-bit microprocessor. Two quadrature clocks (E and Q) are generated externally and input to the microprocessor. The microprocessor clock generator and stretcher generates these two clocks. Normally, the frequency of E and Q is 3 MHz.

Outputs from the microprocessor provides 8-control bits to the Control Bit Register for head select, EEPROM control, and READ GATE delay. The microprocessor controls these bits by simply writing the appropriate byte to the Control Bit Register. The Control Bit Register passes ESDI commands to the HDA.

The transmission of ESDI commands and the reception of ESDI status are controlled by the microprocessor. The COMMAND DATA and TRANSFER REQUEST lines are control bits which are toggled by the firmware. The STATUS and TRANSFER ACKNOWLEDGE lines are status input bits which are read by the firmware. Other ESDI control lines which are output from the CEC (e.g., select drive, head select, etc.) are also control bits which are controlled directly by the firmware. Other ESDI control lines which are input to the CEC (e.g., COMMAND COMPLETE, ATTENTION, etc.) are also status input bits which are read by the firmware.

The Status Bit Register provides status information (i.e., configuration/status, attention, transfer acknowledge, ready, sector and index) received from the HDA.

Transceiver 2 provides an interface between the microprocessor bus and the DMA bus. When the microprocessor accesses a device on the DMA bus, and the DMA Bus Arbiter grants access, Transceiver 2 is enabled. Otherwise, it is disabled. This permits the microprocessor to access devices on the microprocessor bus at the same time that a DMA transfer is taking place on the DMA bus.

3-32. CONTROL, CLOCK GENERATOR AND STRETCHER CIRCUIT

The Control, Clock Generator and Stretcher circuitry performs the following functions:

- Microprocessor E and Q clock generation.
- Microprocessor clock stretching. The clock stretching suspends operation of the microprocessor until the Bus Arbiter grants access to the lower DMA bus.
- Performs microprocessor transfer request/acknowledge handshaking with DMA Bus Arbiter.
- Generates DMA bus read and write strobes (NDMARD [Not DMA Read] and NDMAWR [Not DMA Write]) during a microprocessor access to the DMA bus
- Generates enable signals for Transceiver 2 and microprocessor address buffers. These devices allow the microprocessor address and data buses to be either isolated from or connected to the DMA address and data buses.

A state machine in this circuit is used to control the microprocessor clock generation and stretching, as well as to generate the microprocessor transfer request (NUREQ) to the DMA Bus Arbiter. When the microprocessor is not accessing a device which needs to have the clock stretched, the state machine simply divides the input clock by 4 to generate the two quadrature clocks E and Q for the microprocessor. The input clock is normally 12 MHz, resulting in a 3-MHz E and Q clock.

Clock stretching is performed whenever a device on the DMA bus is accessed by the microprocessor. The state machine looks for any of the DMA bus chip selects to be asserted at a point in time when they are guaranteed to be valid. If one of them is asserted, then the state machine goes to a state where E is held high, Q is held low, and NUREQ is asserted low. The state machine remains in this state until an internal STPSTR (stop stretch) is asserted high. This signifies that the microprocessor transfer has completed. The state machine exits this state (E goes low, NUREQ goes high) and the clock stretching stops.

When the DMA Bus Arbiter grants access to the microprocessor UEN (Microprocessor Enable) goes high. ACSEN (Address Chip Select Enable) goes high on the first clock cycle after UEN goes high. ACSEN performs the following functions when it goes high:

- Causes NBUF2E (Not Transceiver 2 Enable).
- Causes the appropriate DMA bus device's chip select to be asserted (except DDC). This is controlled by the DMA PAL.
- Enables NDMARD and NDMAWR in the Control, Clock Generator and Stretcher circuit.

RWEN (Read/Write Enable) is asserted 2 clock periods after ACSEN is asserted. This causes the appropriate strobe line (NDMARD or NDMAWR) to be asserted low. STPSTR is asserted 4 clock periods after RWEN is asserted. This is what terminates the clock stretch and allows the transfer to complete. When the arbiter resets UEN back low, ACSEN, RWEN, an STPSTR are all reset back low, ready for the next microprocessor access to the DMA bus.

3-33. DISC DATA CONTROLLER (DDC) IC

The DDC's function is to control data transfers between the HDA and HP-IB Interface IC. It also performs ECC generation/checking and error correction. The DDC has on-board DMA circuitry for controlling both local and remote DMA transfers.

The DDC receives high level commands from the microprocessor and then controls the execution of these commands. When a command is complete or an error occurs, the DDC notifies the microprocessor by updating the internal status register and

generates an interrupt, if enabled by the microprocessor.

The DDC does not send ESDI commands to the HDA or receive ESDI status from the HDA. It only controls the transfer of read/write data. All ESDI commands are sent by the microprocessor.

The following is a list of the primary commands that the DDC executes:

- Read Data (reads data from HDA and transfers it to the buffers via local DMA).
- Write Data (reads data from the buffers via local DMA and transfers it to HDA).
- Remote DMA transfer (between the buffers and HP-IB Interface IC).
- Error Correction.
- Format

For a read data operation, the microprocessor sets up the DDC for the number of sectors to be read, the starting sector number, the starting buffer address where the data will be stored, and the size (in bytes) of each local DMA burst transfer. Once the microprocessor initiates the operation, the DDC searches for the beginning sector. Once it is found, the DDC begins reading in the serial data from the HDA. The DDC computes the ECC bytes as the data is read in, and compares it to the ECC bytes stored on the disc. If the DDC detects an error, the operation is aborted. After the data is deserialized, it is transferred to the DDC's internal 32-byte buffer. When the buffer is filled to the local DMA burst size, the DDC requests a local DMA transfer by asserting LREQ (Local Transfer Request).

The DDC begins the local DMA burst transfer after the DMA Bus Arbiter acknowledges the local transfer by asserting LACK (Local Transfer Acknowledge). The DDC then proceeds to write the data out to the buffers. Each transfer to the buffers is 16 bits wide and takes 4 DCLK cycles (333 ns). The DDC performs the following steps for each 16 bit word transferred.

- Outputs buffer address onto DMA data bus.
- Outputs data onto DMA data bus and generates NDMAWR to strobe data into buffers.
- Increments buffer address counter by 2 for next transfer.

This process of filling and emptying the buffer is repeated until the entire transfer is complete. For a write data operation, the microprocessor sets up the DDC for the number of sectors to be written, the starting sector number, the starting buffer address where the data will be transferred from, and the size (in bytes) of each local DMA burst transfer. Once the microprocessor initiates the operation, the DDC performs local burst transfers to fill the internal 32-byte buffer. As in a read data operation, the DDC must wait for an acknowledge from the DMA Bus Arbiter before it can begin a local burst transfer. Each transfer from the buffer is 16 bits wide and takes 4 DCLK cycles (333 ns). The DDC performs the following steps for each 16-bit word transferred:

- Outputs buffer address onto DMA data bus.
- Generates NDMARD to read data from buffers. The DDC strobes the data in on the rising or trailing edge of NDMARD.
- Increments buffer address counter by 2 for next transfer.

The DDC then searches for the beginning sector. Once it is found, the DDC begins serializing the data in the buffer, and transferring it to the HDA. The DDC generates the ECC bytes as it transfers the data to the HDA and appends them to the end of each sector. When the buffer has been depleted by the local burst size, the DDC initiates another local burst transfer by asserting LREQ. This process of filling and emptying the buffer is repeated until the entire transfer is complete.

3-34. REMOTE DMA TRANSFER

For a remote DMA transfer operation, the microprocessor sets up the DDC for the number of bytes to be transferred, the starting buffer address where the data will be written to or read from, and the direction of the transfer. Once the microprocessor initiates the operation, the DDC asserts the remote

transfer request line RREQ. When the DMA Bus Arbiter acknowledges the transfer by asserting RACK, the DDC performs the following steps to complete each 1-byte transfer:

- Outputs buffer address onto DMA data bus.
- Generates NDMAWR strobe if data is being transferred from the HP-IB Interface IC to the buffers.
- Increments buffer address counter by 1 for next transfer.

The DDC will continue this process until all of the bytes specified have been transferred. The microprocessor may set up the DDC to have both a remote and local transfer operation active at the same time. In this situation, the local and remote DMA transfers are interleaved.

3-35. ESDI PAL

The purpose of the ESDI PAL Circuit is to delay the leading edges of READ GATE, WRITE GATE, and ADDRESS MARK ENABLE going to the HDA. Explanations for each case are given below. In each case, an enable signal is generated which is gated with the appropriate DDC signal. Two state machines are implemented in the ESDI PAL. One of the state machines is used to delay READ GATE during the post-index ISG control, and the other is used to generate the three enable signals for READ GATE, WRITE GATE, and ADDRESS MARK ENABLE (RGEN, WGEN, and AMEN respectively).

The ESDI PAL powers up in an asserted low state. The firmware does not change this state until the READ/REFERENCE CLOCK from the HDA is running. This is required for the state machines in the ESDI PAL to reset. During a read or compare header operation, the DDC asserts READ GATE within a couple of READ CLOCK cycles after the INDEX or SECTOR pulse. When a header is written, or at the beginning of a format operation, WRITE GATE has a similar delay from INDEX or SECTOR. Thus, READ GATE could be asserted over a write splice.

The ESDI PAL counter delays the leading edge of READ GATE until the head is over the header PLO sync field in order to avoid this problem. When the ESDI PAL detects an INDEX or SECTOR pulse, counting is enabled by setting (CNT) high. The ESDI PAL asserts RGEN high.

The microprocessor must set up this READ GATE delay at power-on initialization. It does this by writing a 7-bit value into the the counter. Once the 7-bit word has been set up, the microprocessor strobes it into the counter by reading address 3000H. The value of the 7-bit word should be:

```
count = 125 - (post-index ISG)
where the post-index ISG is in bits
```

This insures that READ GATE will be asserted 0.5 to 3.5 bits into the address PLO sync field.

The READ GATE delay circuitry also delays the leading edge of READ GATE by 3-bit times during a data field read. This is to compensate for the delay of WRITE GATE during a data field write. This insures that READ GATE is not asserted over the write splice.

3-36. WRITE GATE AND ADDRESS MARK ENABLE DELAY CIRCUIT. The ESDI specification requires that WRITE CLOCK be active for 2.5 cycles prior to the assertion of WRITE GATE, and that ADDRESS MARK ENABLE be asserted a minimum of 100 ns after the assertion of WRITE GATE. Since the DDC does not meet these requirements by itself, additional hardware was added to delay WRITE CLOCK and ADDRESS MARK ENABLE by the required amounts.

3-37. ERROR CORRECTION

The DDC has the capability to perform 16-bit CRC, or 48-bit ECC generation and checking on the address and data fields. The DDC allows for the microprocessor to program the desired ECC polynomial, polynomial preset, and correction span. An error correction cycle is performed internal to the DDC, however it must be initiated by the microprocessor. When the correction cycle is complete, the DDC contains information for the microprocessor to compute the buffer address of the first byte in the data field that contains the error. The microprocessor then completes the

correction process by XOR'ing the syndrome bytes (in the DDC) with the bytes in the data field that contain the error.

3-38. FORMAT

There are three different ways that the DDC can format a track:

- Internal sequential - the DDC increments the sector number for each physically adjacent sector.
- Buffer table - The information for each header is stored in the buffers and transferred into the DDC at the appropriate time by local DMA.
- Interlock - The microprocessor updates the format parameter bytes in the DDC after each sector is formatted.

The firmware causes the DDC to format an entire track or, during a sparing operation, any number of sectors on a track.

3-39. HP-IB INTERFACE IC

The HP-IB Interface IC is used as the HP-IB interface chip. It implements all of the IEEE STD 488 interface functions. The controller functions are not used in this application. The HP-IB Interface IC has eight internal 10-bit registers which allow the microprocessor to initiate and monitor the HP-IB transfers. In addition, it has an 8-byte in-bound buffer and an 8-byte out-bound buffer for data buffering.

Data transfers to and from the HP-IB Interface IC on the microprocessor side are synchronous, even though the HP-IB Interface IC was designed for asynchronous transfers. This is necessary because the microprocessor has a synchronous bus. DMA transfers are also synchronous. Synchronous transfers are accomplished by asserting NIOGO for the correct period of time. During a remote DMA transfer from the buffers 0 and 1 to the HP-IB Interface IC, NIOGO is delayed so that the data is valid on the DMA bus before NIOGO is asserted. In this case, NDDRD (Not Delay Read) is used to generate the NIOGO (Not I/O Go) signal in the DMA PAL.

The HP-IB Interface IC is operated in the 8-bit mode since the microprocessor is an 8-bit device. Remote DMA transfers are also 8 bits wide, however if the transfer is from the HP-IB Interface IC to Buffers 0 and 1, then the ninth and tenth bits (D0 and D1) are latched. Both D0 and D1 are latched by DQCLK which is equivalent to NIOGO when the transfer direction is from the HP-IB Interface IC to the buffers. When transferring in the other direction, DQCLK remains high. When an incoming byte is tagged with EOI or is a secondary address, then D1 is high. NREMGO (Not Remote Transfer Go) will be set high at the end of that byte transfer and cause the DMA Bus Arbiter to inhibit any more remote DMA transfers. The microprocessor can reset NREMGO back low by toggling the remote DMA direction bit (NREMRD) low. This reenables the remote DMA transfer. NREMGO is a status bit which can be read by the microprocessor.

The state of NREN (Not Remote Transfer Enable) selects the HP-IB Interface IC address lines. When a remote transfer is active, NREN is low and the address is fixed at 2, which is the address of the HP-IB Interface IC buffer (inbound and out-bound). When a remote transfer is not active, NREN is high and the DMA bus address lines are selected. When NREN is high, the DDC read/write line (NR/W) is selected. When NREN is low, the control bit NREMRD is selected. The microprocessor sets NREMRD low when the remote DMA transfer is from Buffers 0 and 1 to HP-IB Interface IC, and sets it high when the transfer is in the opposite direction.

3-40. BUFFERS

One 8k by 8 RAM (Buffer 1) resides on the upper (or most significant) half of the DMA bus, and another 8k by 8 RAM (Buffer 0) resides on the lower (or least significant) half. The addressing and chip selects are arranged so that during remote DMA and microprocessor transfers, Buffer 0 is accessed if the address is even, and Buffer 1 is accessed if the address is odd.

3-41. DMA BUS ARBITER

The DMA Bus Arbiter is a sequential state machine that receives requests from various sources for access to the DMA bus and grants access on a priority basis. The three different types of transfers which can take place on the DMA bus are listed below in the order of highest to lowest priority:

- Local DMA (between the HDA and the buffer)
- Microprocessor (between the microprocessor and any device on the DMA bus)
- Remote DMA (between the HP-IB Interface IC and the buffers)

When no transfers are taking place, the DMA Bus Arbiter is in the idle state and is continuously monitoring the input requests. A detailed description of how the DMA Bus Arbiter handles each type of transfer is given below.

3-42. LOCAL DMA TRANSFERS. A local transfer request is generated by the DDC. It does this by asserting the LREQ signal high. If the DMA Bus Arbiter is in the idle state, then it grants access by asserting LACK (local acknowledge) high. Once the DDC receives LACK, it takes control of the DMA bus and completes the local burst transfer. The DMA Bus Arbiter continues to assert LACK and grant access for local transfers as long as LREQ is asserted. When LREQ is deasserted, the DMA Bus Arbiter deasserts LACK and returns to the idle state. The DMA Bus Arbiter asserts NLEN low during the local transfer period to signify that a local transfer is taking place. NLEN is input to the DMA PAL and is used to generate the chip selects for Buffers 0 and 1.

3-43. MICROPROCESSOR TRANSFERS. Microprocessor transfer requests are generated by asserting NUREQ low. If the DMA Bus Arbiter is in the idle state and the local transfer request (LREQ) is not asserted, then the DMA Bus Arbiter grants access for the microprocessor transfer by asserting UEN high. Once the microprocessor has completed its transfer, which is limited to 1 byte, NUREQ is set high. The DMA Bus Arbiter then deasserts UEN low and returns to the idle state.

3-44. REMOTE DMA TRANSFERS. Remote transfer requests come from two sources, the DDC and the HP-IB Interface IC. The DDC asserts RREQ high and the HP-IB Interface IC asserts NHPIBR (Not HP-IB Read) low to make a request. Both requests and NREMGO must be asserted in order for a remote request to be recognized by the DMA Bus Arbiter. Before the transfer can be acknowledged, the DMA Bus Arbiter must also be in the idle state and both the local and microprocessor requests deasserted. The DMA Bus Arbiter will then grant access by asserting RACK (remote acknowledge) high. Once the DDC receives RACK, it takes control of the DMA bus and completes the remote transfer, which is limited to 1 byte. The DMA Bus Arbiter inserts wait states in the remote transfer. This is required because of the slow speed at which HP-IB Interface IC transfers can be made. The RACK signal is also connected to the EXT-STAT input of the DDC, which causes wait states to be inserted. Three wait states (or 3 DCLK cycles) are inserted into each remote byte transfer. Each remote byte transfer takes one microsecond. Once the byte transfer is complete, the DMA Bus Arbiter returns to the idle state. NREN is asserted low by the arbiter during the remote transfer to signify that a remote transfer is in process. NREN is input to the DMA PAL and is used to generate various control signals used in the transfer.

3-45. EEPROM (When Used)

The EEPROM has a capacity of 512 bytes. All information (address, operation command, data, etc.) is transmitted over the serial data line EEDATA. This is a bidirectional data line. All data is clocked into or out of the EEPROM by the EECLK signal. EEDATA and EECLK are controlled in microprocessor firmware. The microprocessor performs the serialization and deserialization of the data.

Acknowledge cycles are included in all transfers to or from the EEPROM. The transmitting device, either the EEPROM or microprocessor, will release the EEDATA line after transmitting 8 bits. During the ninth clock cycle, the receiver will pull the EEDATA line low to acknowledge that it received the 8 bits of data. This acknowledge cycle is repeated for each 8-bit block of data transferred.

Due to the serial nature and acknowledge cycles of the EEPROM, it is extremely unlikely that inadvertent writes could take place during power cycling. However, for added protection, NRESET is connected to the microprocessor circuits that are used to generate EEDATA. This insures that EEDATA will be held high. Since the device address is 0, the EEPROM can never be addressed during power up or power down. If power is turned off during the middle of a write operation, then the address which is currently being written to may end up with bad data, however no other address locations should be corrupted.

3-46. LED CONTROL

The LED CONTROL circuit sets the condition of the two front panel LEDs. When the disc drive is in an active state the green LED blinks once every 68 ms. If the disc drive fails self test the green LED is turned off and the red LED (FAULT) is turned on. If the disc drive goes into a fault state the green LED is turned off and the red LED is turned on. If the disc drive is operational but in an idle state the red LED is off and the green LED turned on continuously.

Table 3-3. Mnemonic Table

Mnemonic	Definition	Source	Description
ACSEN	Address Chip Select Enable	Microprocessor Control, Clock Generation and Stretcher	Used to enable appropriate address and chip select functions during a microprocessor transaction
DCLK	D CLOCK	Microprocessor Control, Clock Generation and Stretcher	Used to drive DMA Bus Arbiter
DQCLK	DQ Clock	DMA PAL	Clock signal from DMA PAL for remote
EECLK*	EEPROM Clock	Control Bit Register	Used to clock information into and from EEPROM
EEDATA*	EEPROM Data	Status Bit Register/Control Bit Register	Line use to transfer information in and out of EEPROM
LREQ	Local Request	DDC	Activated by DDC to initiate a local transfer
NBUF2E	Not Buffer 2 Enable	DMA PAL	Activated by DMA PAL to turn on Transceiver 2 for microprocessor transactions
NDDRD	Not Delay Read	DMA Bus Arbiter Circuit	Used to generate delayed NIOGO signal
NDMARD	Not DMA Read	DDC/Control, Clock Generation and Stretcher circuit	This signal is activated to provide a Read from the DMA Buffers
NDMAWR	Not DMA Write	DDC/Control, Clock Generation and Stretcher circuit	This signal is activated to provide a Write to the DMA buffers

**For disc drives with an EEPROM only.*

Table 3-3. Mnemonic Table (continued)

Mnemonic	Definition	Source	Description
NHPIBR	HP-IB Remote Transfer Request	HP-IB Interface IC	Signal to DMA Bus Arbiter requesting a remote transfer
NIOGO	Not I/O GO	DMA PAL	Signal used to strobe information into and out of the HP-IB Interface IC. Read/Write strobe.
NLEN	Not Local Enable	DMA Bus Arbiter	This signal signifies that a local transfer is taking place. Enables buffer chip-select signals.
NREMGO	Not REMOTE GO	EOI Detect Circuit	This signal is activated for a Remote transfer. Terminates with a byte tagged with EOI.
NREMRD	Not Remote Direction	Control Bit Register	Input to HP-IB Interface circuits to set direction of remote transfer
NREN	Not Remote Enable	DMA Bus Arbiter	This signal drives the DMA PAL for remote transfers
NR/W	Not Read/Write	Microprocessor	Read/Write from microprocessor. Enabled by NREN signal.
NUREQ	Not Microprocessor Request	Control, Clock Generator Stretcher circuit	Signal line to DMA Bus Arbiter for microprocessor access to DMA Bus
PVAL	Power Valid	Power Supply	Indicates that power supply outputs are up to their proper value
RACK	Remote Acknowledge	DMA Bus Arbiter	Control signal enabling DDC for a remote transfer

Table 3-3. Mnemonic Table (continued)

Mnemonic	Definition	Source	Description
RREQ	Remote Request	DDC	Control signal to DMA Bus Arbiter requesting a remote transfer
RWEN	Read/Write Enable	Control, Clock Generation and Stretcher circuit	Signal to enable microprocessor to DMA bus
STPSTR	Stop Stretch	Control, Clock Generation and Stretcher	Signal used to Terminal Clock Stretch
UEN	Microprocessor Enable	DMA Bus Arbiter	Enable microprocessor for access to DMA bus

Service Information 4

4-1. Introduction

WARNING

The disc drive does not contain operator serviceable parts. To prevent electrical shock, refer all service activities to service-trained personnel.

CAUTION

- The field-replaceable assemblies (FRA's) in the disc drive are electrostatic-sensitive devices. Take appropriate precautions when removing the FRA's from the disc drive. Use of an anti-static pad and wrist strap is required. (These components are contained in anti-static work station, part no. 9300-0749.) Immediately after removal, store the FRA's in anti-static, conductive plastic bags.
- The disc drive is delicate and should be handled with care. Also, the disc drive is heavier (10.9 kilograms/24.0 pounds) than its size would indicate.
- Do not turn the LINE~ switch off when the system is transferring data on the Hewlett-Packard Interface Bus (HP-IB). This can be identified by a flashing green front panel LED.
- Do not cycle the LINE~ switch on and off unnecessarily.
- Do not connect or disconnect the HP-IB cable(s) from the disc drive when the system is transferring data on the HP-IB.

NOTE

- For HP 7957A and HP 7958A Disc Drives with a CEC Controller PCA-A2 date coded B-2633 and version MR1.1 firmware (07957-10151) with an EEPROM installed, all error and fault logging is done to the EEPROM.
- For HP 7957A and HP 7958A Disc Drives with a CEC Controller PCA-A2 date coded B-2633 and version MR1.2 firmware (07957-10161) installed, all error and fault logging is placed on track 0 of the disc drive.
- For HP 7957A and HP 7958A Disc Drives with a CEC Controller PCA-A2 date coded B-2707 or later, all error and fault logging is placed on track 0 of the disc drive.

4-2. Service Tools

The following tools and materials are required to service the disc drive:

- Torx* T10 Driver
- Torx* T15 Driver
- Torx* T25 Driver
- Nut Driver, 9/32"
- Pozi Driver, No. 1
- Anti-Static Workstation, part no. 9300-0794

4-3. PCA Locations

The locations of the three field replaceable assemblies (FRA's) identified by the self-test diagnostics are shown in Figure 4-1, Field Replaceable Assembly (FRA) Locations. Refer to chapter V for removal and replacement instructions and to chapter VI for identification and ordering information.

4-4. Cable Connectors

Figures 4-2 through 4-5 show the locations of the cable connectors on the three FRA's in the disc drive and the cables coupled to these connectors. Figure 6-1, Disc Drive, Exploded View, shows how the cables are connected between the FRA's. An overall cabling diagram of the disc drive is provided in Figure 4-5, Cabling Diagram.

4-5. Signal Distribution

Cable connections between the FRA's in the disc drive are shown in figure 4-5. The distribution of signals via these cables is shown in Figure 4-7, Signal Distribution. The mnemonics appearing in figure 4-5 are defined in Table 3-2, Mnemonics Table.

4-6. Power Distribution

Details of ac input wiring and dc power distribution are shown in Figure 3-5, Disc Drive, Functional Block Diagram, and in Figure 4-5, Cabling Diagram.

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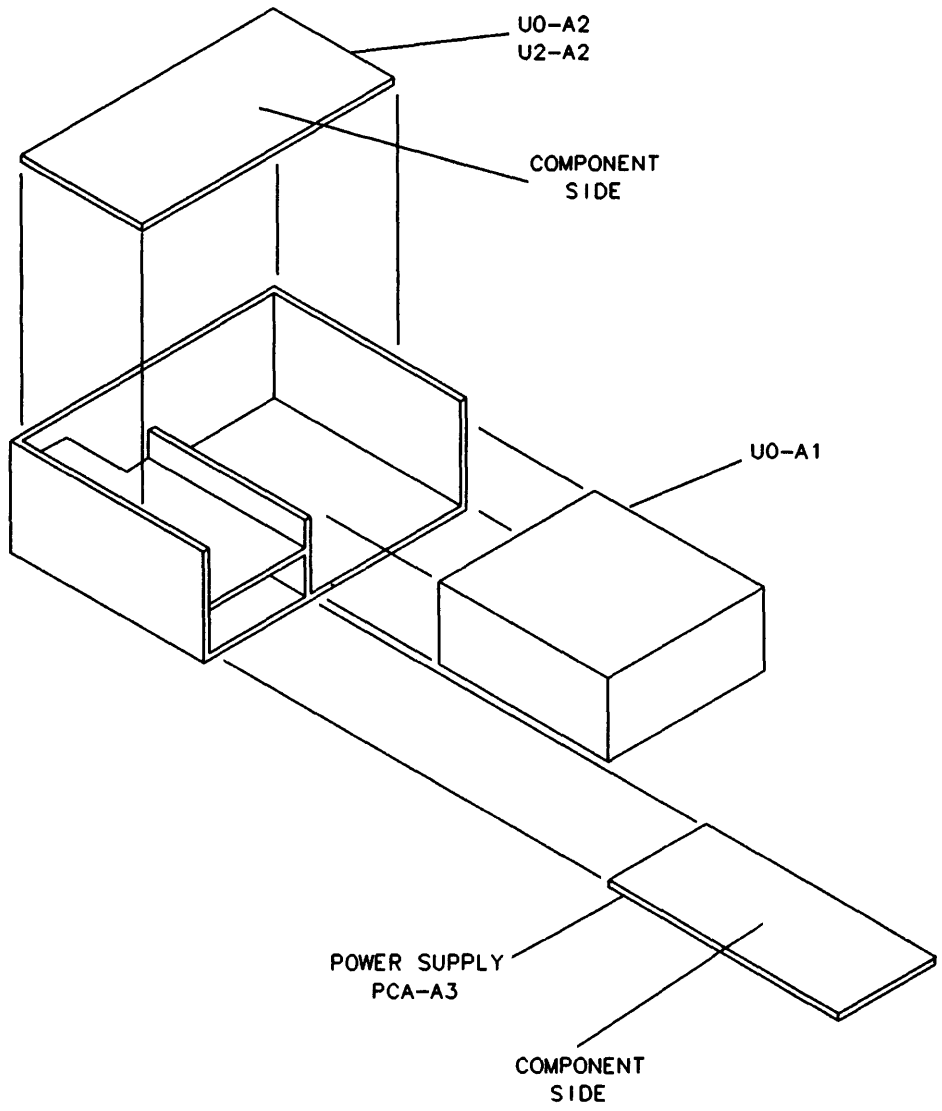
*TORX is a registered trademark of the Camcar Division of Textron, Inc.



U (unit)	A (field replaceable assembly)
0-DISC DRIVE	1-DISC DRIVE PCA-A1 2-CS80/ESDI CONTROLLER (CEC) PCA-A2
2-CONTROLLER	2-CEC PCA-A2

S7957B06

Figure 4-1. Field Replaceable Assembly (FRA) Location

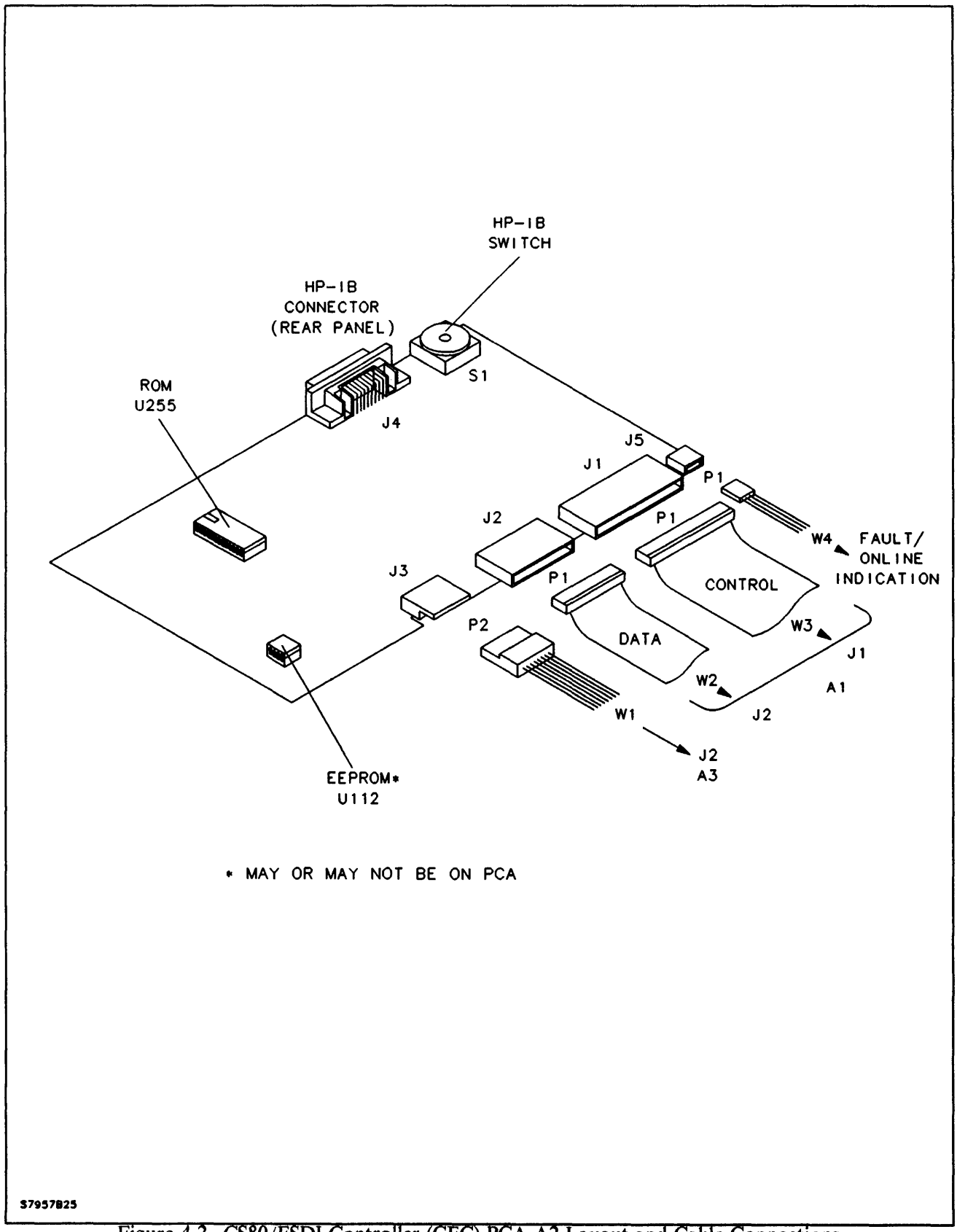
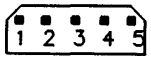
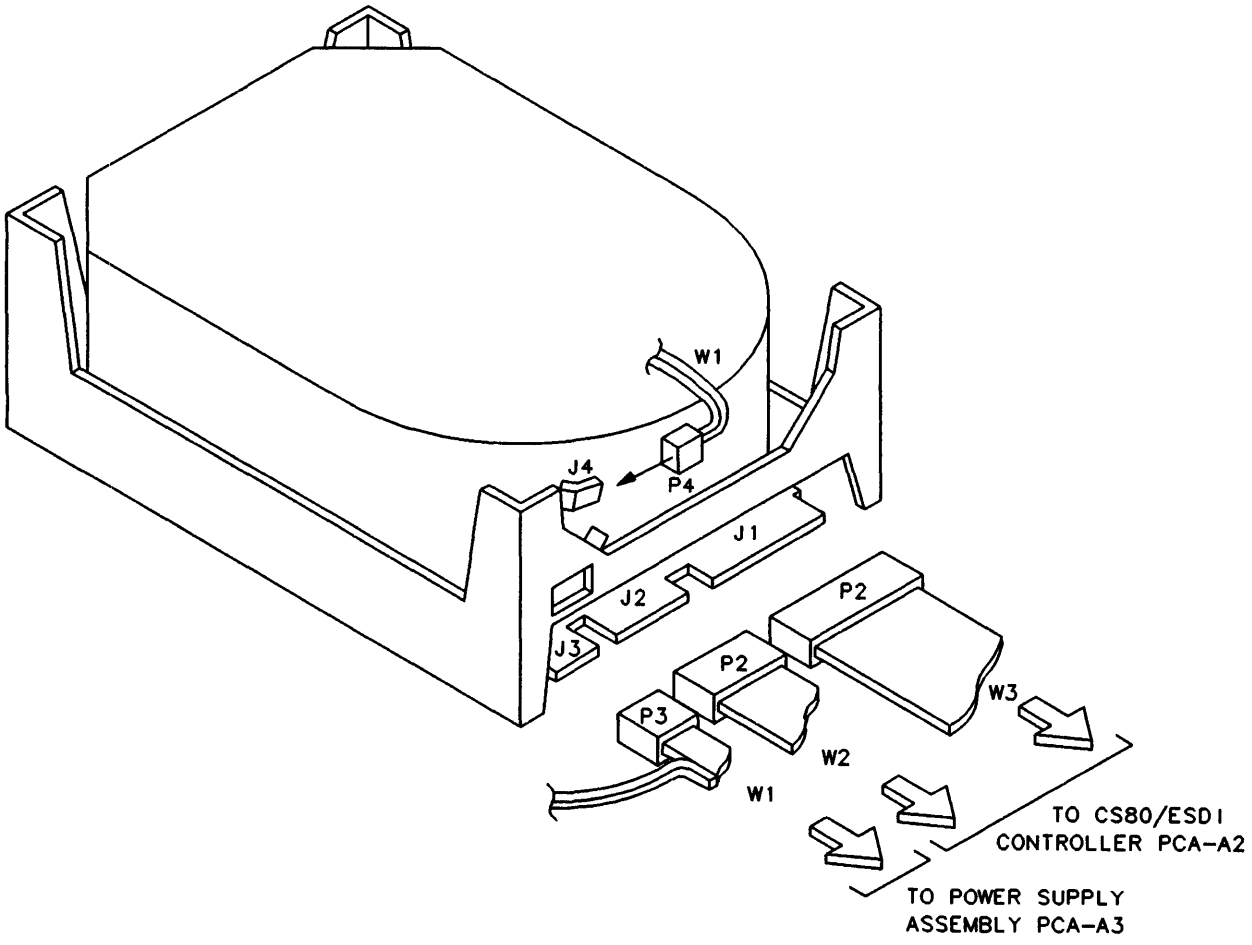


Figure 4-2. CS80/ESDI Controller (CEC) PCA-A2 Layout and Cable Connections

1. J1 PINS ARE NUMBERED 1 THRU 20. EVEN-NUMBERED PINS ARE ON SOLDER SIDE OF PCA. THERE IS A KEYSEAT BETWEEN PINS 4 AND 6.

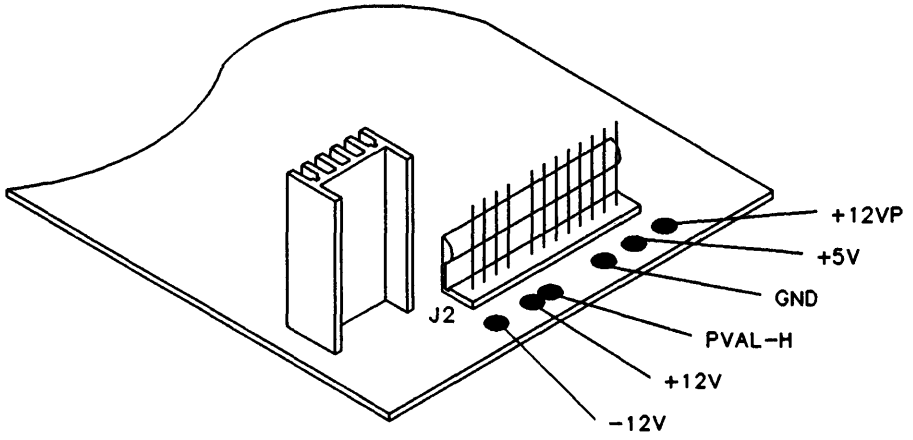
2. J2 PINS ARE NUMBERED 1 THRU 34. EVEN-NUMBERED PINS ARE ON SOLDER SIDE OF PCA. THERE IS A KEYSEAT BETWEEN PINS 4 AND 6.

3. J3 IS NUMBERED AS SHOWN 



S7957A26

Figure 4-3. Disc Drive Assembly PCA-A1, Layout and Cable Connections



TEST POINT	VOLTAGE RANGE
-12V	-11.4 TO -12.6V
+12V	+11.64 TO +12.36V
PVAL-H	≥ +2.4V (TYPICALLY 4.0V)
+5V	+4.85 TO 5.15V
+12VP	11.0 TO 13.0V

NOTE:
1. -12V IS NOT USED IN THE HP 7957 AND HP 7958.
2. USE RET (GND) TEST POINT FOR VOLTMETER RETURN.
3. THE OUTPUT VOLTAGES ARE NOT ADJUSTABLE.
4. MAXIMUM RIPPLE:
   5V SUPPLY: <50 mV P-P
   12V SUPPLIES: <100 mV P-P

S7957A07

Figure 4-4. Power Supply (PCA-A3) Test Points and Voltages

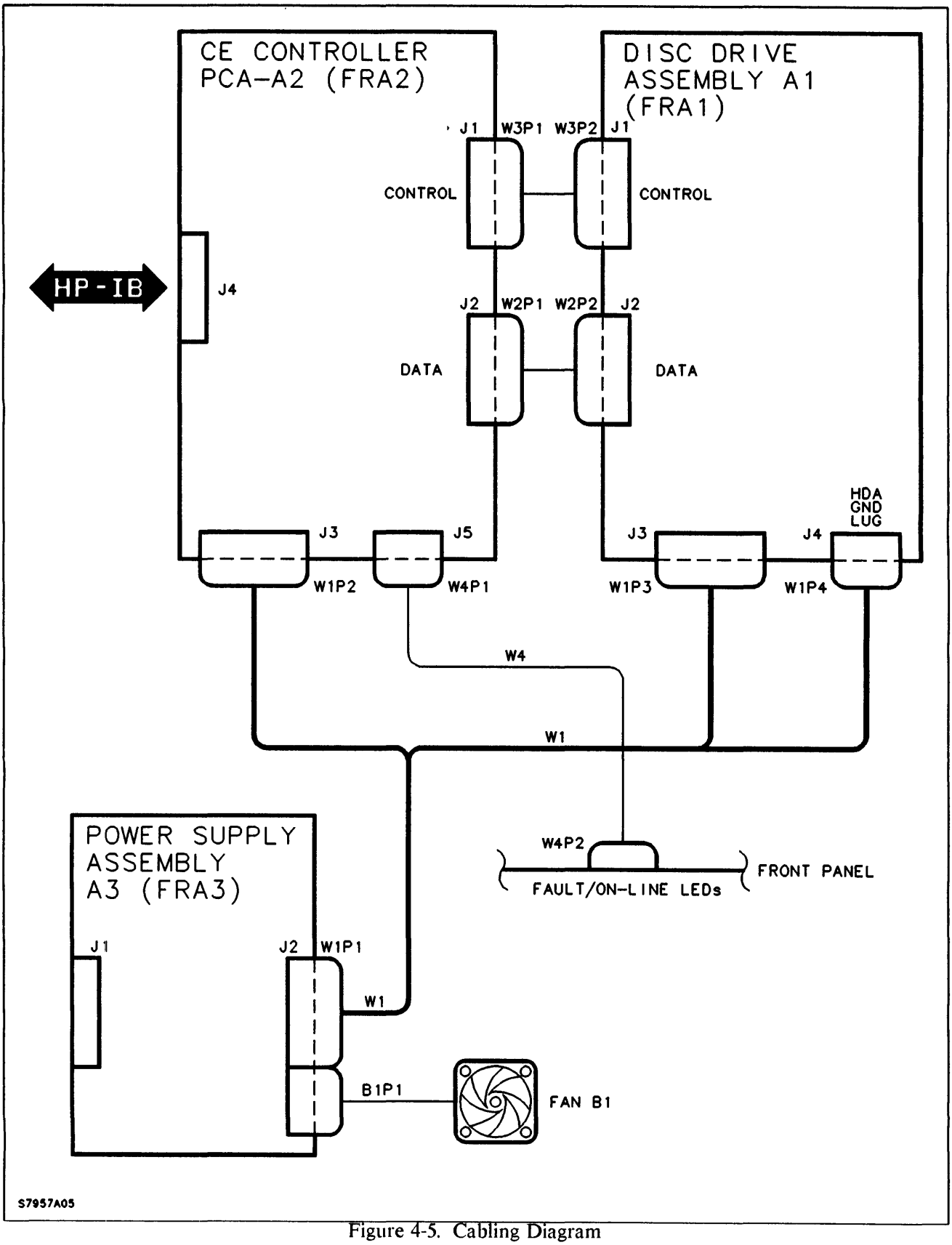


Figure 4-5. Cabling Diagram

4-7. Signal Notation

In the disc drive logic circuits, a digital signal is applied to its destination in one of two states: active or inactive. The signal is active when its voltage level (high or low) makes the action occur for which the signal was designed. This action is usually identified by a signal mnemonic. Refer to Table 3-2, Mnemonics Table. A mnemonic with an "N" prefix indicates a logic signal with an active low voltage level. Signal mnemonics without an "N" prefix usually indicate analog, data bus, control bus signals or an active high signal.

4-8. Block Diagram

A functional block diagram of the disc drive is provided in chapter 3 of this manual (see figure 3-5). Figure 3-6 is a detailed functional block diagram of the CEC and the power supply.

4-9. Test Points

A number of test points are provided in power supply PCA-A3 for troubleshooting and test purposes.

The location of these test points is shown in Figure 4-4, Power Supply (PCA-A3) Test Points and Voltages. Also provided are specifications for the voltages monitored at the test points. The output voltages are not adjustable. It should be noted that access to the test points requires the removal of the front panel assembly from the disc drive. Refer to chapter V for removal details.

4-10. CS/80 Implementation Information

The following information provides details on how various CS/80 commands are implemented in these disc drives. Table 2-5 provides information on what CS/80 commands are implemented.

4-11. Initialize Media Command

The following format options are available when using the Initialize Media Command:

Format Option A - This option will write zeros over the logical tracks. Spare tracks and the spare table are not affected. This option does not write over the headers. This option is completed in a short period of time.

Format Option P - This option will deallocate the field (secondary) spares and writes zeros over the logical tracks. This option takes approximately 5 minutes to complete.

Format Option R - This option reformats all tracks on the disc, but maintains sparing. The headers from the disc are read into the CEC buffers. These headers are used to reformat the tracks. All tracks are reformatted. Sector and track sparing are maintained. This option takes approximately 10 minutes to complete.

4-12. Initiate Diagnostics Command (DIAG)

The following options are available when using this command:

0 = initiates self test
1 = initiates random seek test
2 = initiates outside diameter to inside diameter seek test
3 = initiates incremental seek test
4 = initiates butterfly seek test
5 = initiates EEPROM test (for disc drives with EEPROM only)

4-13. CS/80 Describe Command Response

In response to a CS/80 DESCRIBE command the disc CEC will respond with the following information:

```
CONTROLLER DESCRIPTION FIELD
INSTALLED UNIT <1 bit for each unit>:
****1000 0000 0000 0001****
MAXIMUM TRANSFER RATE: 1000 K-BYTES/SEC
CONTROLLER TYPE:  0
<INTEGRATED SINGLE-UNIT CONTROLLER>
```

UNIT 0 DESCRIPTION FIELD	7957A	7958A
GENERIC DEVICE TYPE: 0		
<FIXED DISC>		
HP PRODUCT NUMBER	079570	079580
NUMBER OF BYTES PER BLOCK	256	256
NUMBER OF BLOCKS THAT CAN BE BUFFERED	64	64
RECOMMENDED BURST SIZE	0	0
BLOCK TIME (microseconds)	265	265
CONTINUOUS AVE TRANS RATE <KBYTES/SEC>	900	900
OPTIMAL RETRY TIME (tens of millisec>	80	80
ACCESS TIME PARAMETER	500	500
MAXIMUM INTERLEAVE FACTOR	1	1

```
FIXED VOLUME BYTE <one bit per vol>:
****0000 0001****
REMOVABLE VOLUME BYTE <one bit per vol>:
****0000 0000****
```

```
------------------------------------------------------------------------
  VOLUME 0 DESCRIBE FIELD
------------------------------------------------------------------------
MAXIMUM CYLINDER ADDRESS ..............................  1012      1012
MAXIMUM HEAD ADDRESS ..................................     4         7
MAXIMUM SECTOR ADDRESS ................................    62        62
MAXIMUM SINGLE-VEC ADDRESS ............................ 319094    510551
CURRENT INTERLEAVE FACTOR .............................     1         1
```

4-14. Self-Test Controls

The disc drive self-test controls include a red/green FAULT/ON LINE indicator on the front panel (see Figure 4-6, Self-Test Display). Information regarding the use of these controls and indicators is provided in the following paragraphs.

4-15. Fault/On Line Indicator

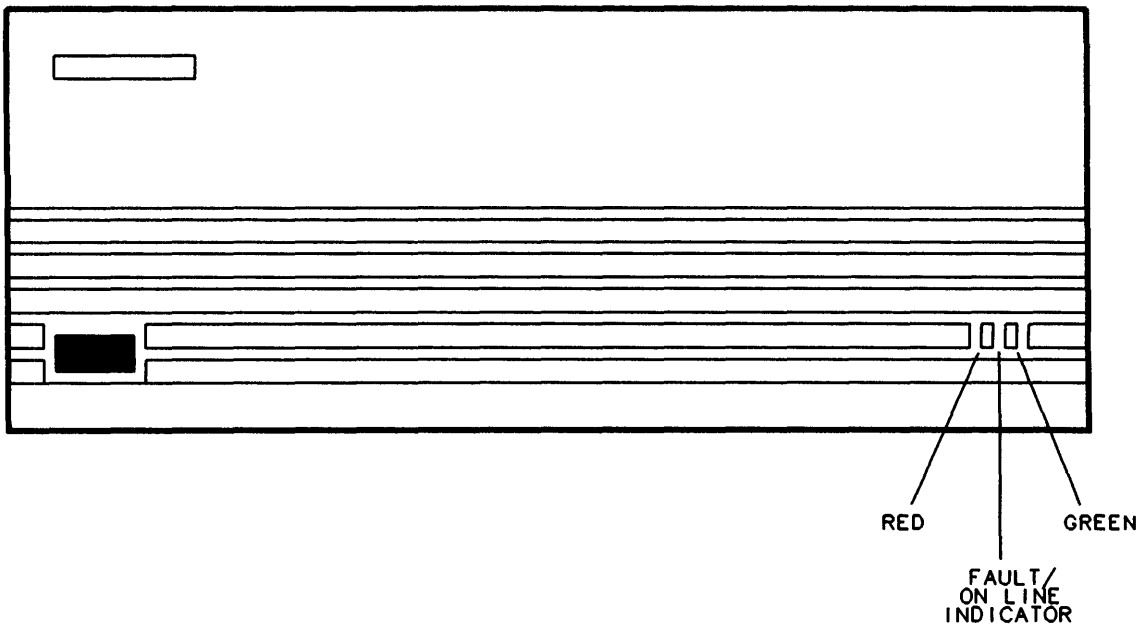
The FAULT/ON LINE indicator is a red/green display which signals the operating status of the disc drive. When line voltage is applied to the disc drive, the FAULT (red) and ON LINE (green) portions of the display will illuminate for 5 seconds while the CEC PCA-A2 runs Self Test and the Disc Drive Assembly PCA-A1 spins up. Next, the green portion will flash during the time that the disc drive is executing its internal self-test routines. Self Test takes between six and twelve seconds to complete. If the disc drive passes self test, the display will change to a solid green. If the disc drive fails self test, the display will change to a solid red with a flashing green indicating that the self-test failure has occurred, but that the self-test routines are still accomplishing some "housekeeping" tasks. When these tasks are complete, the green indicator will extinguish, indicating that the disc drive is ready to accept host commands such as diagnostics. The green indicator will flash again when the disc drive attempts to respond to these commands. A solid red and green display indicates that the CEC PCA-A2 has failed self test.

After a successful self test, a solid green display indicates that the disc drive is idle and a flashing green display indicates that the disc drive is active.

4-16. Internal Diagnostics

The disc drive internal diagnostics includes self-test routines and run time error and fault reporting circuits. The self-test routines, activated at power on, consist of a series of subtests which check the overall operation of the disc drives.

When the disc drive is powered on, the red and green LED's will both be on for about 5 seconds while the CEC PCA-A2 tests its memory. If the memory self test fails, both LED's will remain on and the disc drive will not attempt to come on line. If the memory self test passes then the red LED is turned off and the green LED flashes, as the self-test sequence establishes communications with the Disc Drive Assembly PCA-A1 to attempt seeks and read/write tests. If the



FAULT/ON LINE INDICATOR

RED	GREEN	
ON	ON	ON FOR 5 SECONDS AT POWER ON WHILE CONTROLLER RUNS SELF TEST AND DISC MECHANISM SPINS UP. IF EITHER CONTROLLER SELF TEST OR MECHANISM SPIN UP FAILS THEN BOTH LED's REMAIN ON.
OFF	FLASHING	EXECUTING SELF TEST OR DISC DRIVE ACTIVE.
ON	OFF	DISC DRIVE HAS FAILED MECHANISM SELF TEST THE DISC DRIVE MAY STILL BE ACCESSED BY THE HOST CPU TO RUN DIAGNOSTICS.
OFF	ON	DISC DRIVE IS IN A READY STATE
OFF	FLASHING	DISC DRIVE IS ACTIVE (i.e., PROCESSING A COMMAND)

W7957A04

Figure 4-6. Self-Test Display

Disc Drive PCA-A1 is unable to spin up there will be no index pulse to flash the green LED. A misleading front panel indication will occur for approximately 1 minute until the self test times out and fails.

This portion of the self test, tests the Disc Drive PCA-A1 and normally requires 10 to 15 seconds to complete. If this portion passes the disc drive comes on line and the red LED will be off and the green LED will be on indicating a drive ready state.

If the Disc Drive Assembly PCA-A1 fails self test the red LED will light and the green LED will be off. The disc drive will come on line and the diagnostic result bit will be set. It is strongly recommended that the host not attempt to access data on the disc drive or issue commands to the disc drive if the power-on self test has failed.

Note: Faults which occur during run time do not affect the red or green LED.

After power-on and completion of self test, circuits monitor the operation of the disc drive and log run time errors and faults on the maintenance track. Details of these two diagnostics tools are provided in the following paragraphs. Refer to table 4-1 for a summary of supported utilities.

4-17. Self Test

Self test consists of the following subtests:

- Microprocessor Self Test
- RAM Self Test
- ROM Checksum Test
- HP-IB Interface IC Loopback Test
- Buffer Self Test
- Hardware/Firmware Initialization
- Select A Drive
- Command Complete
- ESDI Status Check
- Reset Attention
- Check for Drive Ready
- Request Configuration
- Mechanism Self Test

Table 4-1. Supported Utilities

CS/80 NO EXECUTION MESSAGE (no information is returned to host)

Clear Logs
Preset

CS/80 SEND EXECUTION MESSAGE (drive returns information to host)

Read Fault Log
Read Run Time Error Log
Read Error (ERT) Log
Measure Seek Time
Read Spare Table
Locate and Read Full Sector
Servo Test
Pattern Error Rate Test (ERT)*
Random Pattern Error Rate Test (ERT)*
Read Only Error Rate Test (ERT)*
Random Read Only Error Rate Test (ERT)*
Read ROM Revision Number

*These utilities provide both a NO EXECUTION MESSAGE and a SEND EXECUTION MESSAGE depending upon the bits set in the "Initiate Utility" command. Refer to paragraph 4-30.

- Read Write ECC Test
- Build Spare Tables
- Seek With Verify Position
- Copy EEPROM Logs to Self Test Cylinder (for disc drives with EEPROM only)
- Finish HP-IB Interface IC Initialization

These self-test routines are stored in the ROM on the CEC PCA-A2. The host can determine the details of self-test failures at the Select A Drive Subtest point by using the CS/80 Request Status Command.

4-18. Self-Test Subtests

4-19. Microprocessor Self Test

Note: Hardware forces the LED's ON when a power-on reset condition occurs.

Limitations: This self test is by no means intended to be a thorough test of the operation of the microprocessor or even a sufficient subset of the microprocessor's operation.

Process: The X and D registers are loaded with C355hex (H). The Y and U registers are loaded with 3CAAH. The registers are compared against the loaded values and a mismatch in any register causes the firmware to loop forever at the point where the error was detected. The purpose of the infinite loop is to assure that the CEC PCA-A2 will not attempt to come on line.

Fault Reporting: The only means of communicating a failure to the user is through the two LED's. Both the red and green LED's will remain on indefinitely.

Note: Without monitoring the address of the firmware loop this fault will be indistinguishable from RAM Self Test failure, ROM Checksum Failure, or a Buffer Self Test failure.

4-20. RAM Self Test

Limitations: This is a 2k RAM which the microprocessor uses for its stack and for variables. Each byte is tested for stuck at one and stuck at zero.

Process: A 3-byte pattern (00H, A5H, C3H) is written to the RAM. The RAM is read to make certain each byte contains the correct value. The RAM is rewritten with another 3-byte pattern (FFH, 5AH, 3CH) such that each byte is written with the complement of the value it received on the first write pass. The RAM is read and each byte is compared against the value it should contain.

If a failure occurs, the firmware enters an infinite loop. The disc drive is not allowed to come on line.

Fault Reporting: The only means of communicating a failure to the user is through the two LED's. Both the red and green LED's will remain on indefinitely.

Note: Without monitoring the address of the firmware loop this fault will be indistinguishable from a Microprocessor Self Test Failure, ROM Checksum Failure, or a Buffer Self Test failure.

4-21. ROM Checksum Test

A checksum is calculated and compared to the ROM's checksum.

Process: If a failure occurs, the firmware enters an infinite loop. The drive is not allowed to come on line.

Fault Reporting: The only means of communicating a failure to the user is through the two LED's. Both the red and green LED's will remain on indefinitely.

Note: Without monitoring the address of the firmware loop this fault will be indistinguishable from a Microprocessor Self Test Failure, RAM Self Test Failure, or a Buffer Self Test Failure.

4-22. HP-IB Interface IC Loopback Test

Limitations: Data patterns are written to the internal Outbound FIFO and are read back through the Inbound FIFO. A check is made to see that the last byte is tagged with EOI as it should be. This test does not attempt to check functionality of most of the interrupts. It cannot verify the ability of the circuit to control lines over the HP-IB interface.

Process: If this test fails the firmware will loop indefinitely. The disc drive will not come on line.

Fault Reporting: The only means of communicating a failure to the user is through the two front panel LED's. Both the read and green LED's will remain on indefinitely.

Note: Without monitoring the address of the firmware loop this fault will be indistinguishable from a Microprocessor Self Test Failure, a RAM Self Test Failure, or a Buffer RAM Self Test Failure.

This test is not available through the diagnostics command option 0. It only occurs as part of the power-on sequence.

4-23. Buffer Test

Limitations: These are the two buffers (0 and 1) which the DMA uses to buffer data transfers between the host and the Disc Drive Assembly PCA-A1. It is also used to receive commands from the host and to return reports and execution messages to the host.

Each byte is tested for stuck at one and stuck at zero.

Process: A 3-byte pattern (00H, A5H, C3H) is written to the buffers. The buffer is read to make certain each byte contains the correct value. The buffer is rewritten with another three byte pattern (FFH, 5AH, 3CH) such that each byte is written with the complement of the value it received on the first write pass. The buffer is read and each byte is compared against the value it should contain.

If a failure occurs, the firmware enters an infinite loop. The drive is not allowed to come on line.

The self test which is done as a result of an initiate Diagnostic command also does a walking one and a walking zero test on each byte of the buffer.

Fault Reporting: The only means of communicating a failure to the user is through the two LED's. Both the red and green LED's will remain on indefinitely.

Note: Without monitoring the address of the firmware loop this fault will be indistinguishable from a Microprocessor Self Test Failure, ROM Checksum Failure, or a RAM Self Test Failure.

4-24. Hardware/Software Initialization

Process: The Disc CEC PCA-A2 IC is initialized and placed in a benign state. The HP-IB interface IC is initialized to a harmless state, but its initialization is not complete at this point. Certain status and global variables are initialized to their power-on values. The spare table is cleared and the error rate test table is initialized. The seek variables are initialized.

Fault Reporting: No self test is associated with this step in the power-on process so no faults are detected.

The preceding portion of self test normally takes about 2-3 seconds to execute.

4-25. Select A Drive

Limitations: This CEC PCA-A2 was designed to support only a single Disc Drive Assembly PCA-A1. Therefore, the Disc Drive Assembly PCA-A1 will always be selected by the firmware.

Process: The ESDI drive select line for Disc Drive Assembly PCA-A1 is asserted. Up to 60 seconds is allowed for the Disc Drive Assembly PCA-A1 to assert the

drive selected line in response. If the drive selected line is not asserted within the timeout period the mechanism self test will terminate and the disc drive will not attempt to come on line. The disc drive is not allowed to come on line because the "drive not selected" condition may be the result of a disconnected ESDI Data Cable (W2). If this is the case the READ CLOCK to the DDC IC which would make DMA transfers to the host impossible.

Fault Reporting: In this case both LED's are on solid. In the second case, the disc drive comes on line and reports self-test fault #69 in P7 and P3. The diagnostic result bit will be set. P1 contains the code for the first suspect FRA. It will be 1 (Disc Drive Assembly PCA-A1). P2 contains the code for the second suspect FRA. a two (2) indicates the CEC PCA-A2. The ribbon cables between the CEC PCA-A2 and the Disc Drive Assembly PCA-A1 are also suspect but no FRA number exists for this component.

Note: Disc Drive Assembly PCA-A1 must be de-selected and re-selected as part of the initialization. If the disc drive fails to respond with "drive selected" then the "Can't Select Drive" diagnostic fault is generated. The remainder of the self test and initialization is skipped and the disc drive comes on line to report the fault.

Once the power-on sequence completes Select A Drive the disc drive will always come on line and report the nature of subsequent self-test failures using the CS/80 status bytes P1, P2, P3, P7, P8, and P9. This does not mean that subsequent self-test failures are less critical or that the disc drive is operable. On the contrary, it is strongly advisable for the host not to issue commands to the Disc Drive Assembly PCA-A1 after any self-test failure. If the diagnostic result bit is set during the power on self test, any operation initiated by the host can have unpredictable results.

The only reason that the disc drive is allowed to come on line is to report the nature of the self-test failure to the operator.

At this point in the power-on process the red LED will be turned off. The green LED will blink if an index pulse is available from the Disc Drive Assembly PCA-A1.

4-26. Command Complete

Process: The CEC PCA-A2 will wait up to 60 seconds for the Disc Drive Assembly PCA-A1 to assert the ESDI command complete line. If the command complete line is not asserted within the timeout period a fault will be generated. The remainder of the self test and initialization is skipped and the disc drive comes on line to report the fault.

Fault Reporting: The disc drive comes on line and reports self-test fault #70 in P7 and P3. The diagnostic result bit will be set. P1 contains the code for the first suspect FRA. A one (1) indicates Disc Drive Assembly PCA-A1. P2 contains the code for the second suspect FRA. A two (2) indicates CEC PCA-A2. The ribbon cables between the CEC PCA-A2 and the Disc Drive Assembly PCA-A1 are also suspect but no FRA number exists for this component.

Note: At this point it is strongly advisable for the host not to attempt any further operations with the disc drive. If the host attempts to run utilities or diagnostics, unpredictable results will occur. For example, diagnostics may return a status of pass without having done anything. This result comes from the fact that configuration was not executed.

4-27. ESDI Status Check

Process: This is the first time that the CEC PCA-A2 attempts to send a command over the ESDI serial communication line. More than one type of fault can arise.

An ESDI request status command is sent to the Disc Drive Assembly PCA-A1. The Disc Drive Assembly PCA-A1 should respond with a 16-bit general status word. If the status is successfully received from the Disc Drive Assembly PCA-A1 the vendor unique status bit is checked. If the vendor unique status bit is set, the vendor unique status is requested from the Disc Drive Assembly PCA-A1, a fault is generated, and the fault number, ESDI status and least significant byte of the vendor unique status are returned to the host. Information from the 16-bit word is compressed into the ESDI status word.

If the vendor unique status available bit is not set then several of the other status bits are checked. If any of these bits are set, a fault is generated. The fault and ESDI status will be returned to the host.

```
Compressed ESDI status bits:
                    7 = SMS-spindle motor stopped
                    6 = PON-power-on conditions exist/
                      start spindle motor command may
                      be required
                    5 = CDP- command data parity fault
                    4 = IF-interface fault
                    3 = IC-invalid or unimplemented command
                    2 = SF-seek fault
                    1 = WG-write gate with track offset fault
                    0 = 1-write fault
```

Note: Bit 6 is expected to be set during a fault condition.

Note: Retry commands are transparent to the self-test procedure. If the ESDI communication fails but a retry is successful, the self test will pass and none of the bits listed above should be set.

Fault Reporting: If the vendor unique status bit is set, fault #76 will be placed in P3. The first suspect (P1) is the Disc Drive Assembly PCA-A1. The second suspect (P2) is set to zero which implies that the guilty party is known with sufficient confidence that no second suspect is necessary.

```
P7 = fault 76
P8 = compressed ESDI statues
P9 = least significant byte of vendor unique status
```

If one of the ESDI status bits is set indicating that the Disc Drive Assembly PCA-A1 is in an unexpected state then:

```
P1 = Disc Drive Assembly PCA-A1
P2 = zero
P3 = fault 71
P7 = fault 71
P8 = compressed ESDI status
P9 = least significant byte of vendor unique status
```

4-28. Reset Attention

Process: The ESDI reset attention command is sent to the Disc Drive Assembly PCA-A1. This command deasserts the attention line and clears the status. A fault occurs if an ESDI communication timeout occurs and the retries are exhausted or if the attention line is still asserted after the reset attention command is sent.

Fault Reporting: The disc drive comes on line and reports self-test fault #75 in P3. The diagnostic result bit will be set. P1 contains the code for the first suspect FRA. A one (1) indicates Disc Drive Assembly PCA-A1. P2 contains the code for the second suspect FRA. A two (2) indicates CEC PCA-A2. The ribbon cables between the CEC PCA-A2 and the Disc Drive Assembly PCA-A1 are also suspect but no FRA number exists for this component.

P7 will contain either fault #75 if the attention line was not reset or a fault number describing the ESDI communication problem if that condition occurred. P8 and P9 will contain the status associated with the fault number stored in P7.

Note: At this point it is strongly advisable for the host not to attempt any further operations with the disc drive. If the host attempts to run utilities or diagnostics, unpredictable results will occur. For example, diagnostics may return a status of pass without having done anything. This result comes from the fact that configuration was not executed.

4-29. Check for Drive Ready

Process: The firmware will read the ESDI drive ready line. If drive ready is not asserted a fault is generated.

Fault Reporting: The disc drive comes on line and reports self-test fault #72 in P3 and P7. The diagnostic result bit will be set. P1 contains the code for the first suspect FRA. A one (1) indicates Disc Drive Assembly PCA-A1. P2 contains the code for the second suspect FRA. A two (2) indicates CEC PCA-A2. The ribbon cables between the CEC PCA-A2 and the Disc Drive Assembly PCA-A1 are also suspect but no FRA number exists for this component.

P8 and P9 will contain the compressed ESDI status and vendor unique status respectively.

Note: At this point it is strongly advisable for the host not to attempt any further operations with the disc drive. If the host attempts to run utilities or diagnostics, unpredictable results will occur. For example, diagnostics may return a status of pass without having done anything. This result comes from the fact that configuration was not executed.

4-30. Request Configuration

Process: The ESDI request configuration command is used to determine capacity and feature characteristics of the Disc Drive Assembly PCA-A1. The information which the Disc Drive Assembly PCA-A1 returns is not bounds checked, but is assumed to be correct. The only faults which can result from this step in the initialization process are ESDI communication faults.

Note: The configuration process issues a set number of unformatted bytes per sector command. This command overrides the 63 sector configuration set by internal jumpers. The Disc Drive Assembly PCA-A1 is now configured for 325 bytes per sector which results in 64 sectors per track.

Fault Reporting: The disc drive comes on line and reports self-test fault #73 in P3. The diagnostic result bit will be set. P1 contains the code for the first suspect FRA. A one (1) indicates Disc Drive Assembly PCA-A1. P2 contains the code for the second suspect FRA. A two (2) indicates CEC PCA-A2.

P7 will contain the fault number describing the ESDI communication problem. P8 and P9 will contain the status associated with the fault number stored in P7.

Note: At this point it is strongly advisable for the host not to attempt any further operations with the disc drive. If the host attempts to run utilities or diagnostics, unpredictable results will occur. For example, diagnostics may return a status of pass without having done anything. This result comes from the fact that configuration was not executed.

4-31. Disc Drive Assembly PCA-A1 Self Test

Limitations: The Disc Drive Assembly PCA-A1 self test is not intended to be exhaustive or to verify the product specifications. It does attempt to determine if minimal read, write and seek capabilities exist. **Process:** The Disc Drive Assembly PCA-A1 self test is broken down into four major subtests.

1) seeks without position verify

2) Read, Write and ECC tests

3) Build Spare Tables

4) seeks on all heads with position verify after each seek

4-32. Seek Test Without Position Verify

Process: Logical seeks are performed with head 0 selected. The target tracks are 0, 1, 2, 4, 8 . . . max logical, 0, max logical, max logical - 1, max logical -2, max logical -4, max logical -8 . . . 0. Faults occur if the Disc Drive Assembly PCA-A1 reports a seek fault or ESDI communication problems arise. No attempt is made to read a header to verify that a seek actually occurred.

Fault Reporting:

```
P1 = 1 (Disc Drive Assembly PCA-A1)
P2 = 2 (CEC PCA-A2)
P3 = 77 Disc Drive Assembly PCA-A1 self test failed
P7 = fault #
P8 = status associated with fault # in P7
P9 = status associated with fault # in P7
```

4-33. Read Write ECC Test

Limitations: A sector may be found which can be read and written 10 times without an error yet still contain a slight media defect. The defect could cause some inconsistency in the ECC test results.

Process: There are two phases to the Read/Write ECC test. The first consists of finding a sector which can be written and read 10 times without a data error. This sector is then assumed to be free of major media defects and so it is used for the second phase which is the ECC portion of the test.

The test begins with a physical seek to the outside-diameter (OD) self-test cylinder which is at physical cylinder 0. Starting on head 0, up to 5 sectors are tried in an attempt to find one which can be read and written 10 times without an error. If five sectors are tried unsuccessfully self-test fault #67 is generated to indicated that the Read/Write retry count was exhausted. If any other fault is detected during the read/write test it will be reported. As soon as a fault occurs testing stops.

When a sector is found that can be read and written without an error the ECC test is performed. This consists of writing an uncorrectable data error on the sector. The sector is read and an uncorrectable error must be detected. A correctable error is written and it must be read back as a correctable error. The corrected data is checked to make certain that the errors were accurately corrected. The final step is to rewrite the sector with no error. An ECC test failure results in fault #68.

The tests outlined in the preceding two paragraphs are repeated for each head at the OD self-test cylinder and again for each head on the inside diameter (ID) self-test cylinder.

Each time a sector is read as part of the read/write test the data is compared against that which was written. Any mismatch which was not detected by the ECC is flagged as a fault #66. Fault #66 is a self-test data compare error. The data is read into various locations in the buffer space in an attempt to guarantee the integrity of the buffer RAM addressing and the DMA.

Fault Reporting: The three most likely faults to be generated are:

```
66 self-test data compare error
67 self-test read/write retry count exhausted
68 ECC test failed
```

The errors would be reported in P3 and P7.

```
For Faults 66 and 68: P1 = 2 (CEC PCA-A2)
                      P2 = 0 (no second suspect)
For Fault 67:         P1 = 1 (Disc Drive Assembly PCA-A1)
                      P2 = 2 (CEC PCA-A2)
```

4-34. Build Spare Tables

Since the spare table is not stored on a maintenance track, it must be built at power on. A seek is done on each head and the sector header is read. If the flag byte indicates that there is a spare track in use, then the header cylinder value is entered in the table for the head being accessed. If the spare table cannot be built (due to data errors or faults) then no spares will be in the spare table. However, if an attempt is made to access a spared out track, a Unit Fault will be reported.

4-35. Copy EEPROM Logs to Self Test Cylinder (for drives with EEPROM only)

Process: This procedure will not generate a self-test fault. It is intended as a debug aid for manufacturing. The entire 512 byte EEPROM is copied to maximum logical sector -1 and maximum logical sector of each head on the OD self-test cylinder. It is hoped that one of these redundant copies will be readable when the Disc Drive Assembly PCA-A1 is returned to the factory.

Faults can be generated during the process of copying the EEPROM to the self-test cylinder but the diagnostic result bit should not be set.

4-36. Finish HP-IB Interface IC Initialization

Process: No self-test faults can be generated by this step. The HP-IB Interface IC initialization is completed. The green light is turned on solid (blink is set to off). The interrupts are enabled.

4-37. Request Status

If an Initiate Diagnostic command (DIAG) is issued to the disc drive and an execution message returns a QSTAT of 1, this means that a self-test error has occurred. A Request Status command (REQSTAT) should be issued to obtain the reason for the previous QSTAT of 1. When the Request Status command is executed, a 20-byte field is returned. This field is defined in the *CS/80 Instruction Set Programming Manual*, part no. 5955-3442. When self test is executed and it fails, the Diagnostic Result Bit (bit 24) will be set in the Fault Error Field (sometimes referred to as the Error Fault Field) of the 20 bytes

returned from the Request Status command. When bit 24 is set, P1, P2, P3, P7, and P8 contain specific self-test results, as detailed below:

- P1 - Identifies the most suspect FRA:
  1 = PCA1 (Disc Drive Assembly A1)
  2 = PCA2 (CEC PCA-A2)

- P2 - Identifies the next most suspect FRA:
  Same code as P1

- P3 - Failed disc drive (unit 0) self-test subtest.
  Refer to table 4-2

- P7 - Failed disc drive error condition.
  Refer to table 4-2

- P8 - Details of failed disc drive error condition.
  Refer to table 4-2

4-38. Request Status Example

The following example shows how to interpret P1, P2, P3, P7 and P8 returned for a Request Status command following a self-test failure.

P1 = 1
P2 = 2
P3 = 4E (hex)
P7 = 4E
P8 = 0000 0100

P1 indicates that the most suspect FRA is PCA-A1 (Disc Drive Assembly [HDA]). P2 indicates that the next most suspect FRA is PCA-A2 (CS80/ESDI Controller [CEC]). P3 indicates that the failed self-test subtest is 4E (hex) which is defined in table 4-2 as "One of the 4 seek diagnostic tests failed". P7 contains the fault code 4E and P8 contains the ESDI status with bit 2 set indicating a seek fault.

Note: P7 may contain a fault code other than 4E if more detailed information on the cause of the failure is available.

NOTE

The OFFSET and REPORT bytes are don't care bytes for these products.

4-39. Utilities

Utilities are firmware routines which perform error rate tests, access error logs, access fault logs and access the spare table. The utilities may be initiated through the CS/80 command "Initiate Utility". The utilities are classified by the method through which they are invoked. Table 4-1 includes all the supported utilities. This product does not support utilities which receive execution messages.

The format for the "Initiate Utility" command is:

<INITIATES Utility> <Micro Code> <up to 8 parameter bytes>

Initiate utility = 001100XX
Where XX: 00 = no execution message
01 = not supported on 7957A/7958A
10 = device will send execution message text

4-40. Run Time and Fault Logs (Media Based)

The Run Time (RT) Error Log and Fault Log contain data error information and fault information, respectively. The Run Time Error Log and Fault Log are stored in four contiguous sectors on physical cylinder 0. The Fault Log has a capacity for recording 46 faults and are written over in a FIFO fashion. The Run Time Error Log has a capacity for recording 50 faults and are written over in a FIFO fashion. The ERT log is RAM based and contains information on data errors which occur during error rate testing.

During a run time operation, marginal and nonrecoverable data errors are immediately logged to the Run Time Error Log. The CEC PCA-A2 will not be able to respond to commands for a period of 100 ms while the error information is being stored in the Run Time Error Log. The disc drive does not request release to store the error information. The Read Run Time Error Log utility extracts the run time error information from the maintenance track and returns it to the host.

Faults which occur during utilities/diagnostics and run time activities are, with a few exceptions (see fault ranges), stored in the maintenance track Fault Log. The CEC PCA-A2 will not respond to commands for 100 ms while a fault is being logged. Release is not requested to log a fault. Each fault creates a unique log entry. (An occurrence count of faults is not stored.) The Read Fault Log utility extracts the fault information from the Fault Log and returns it to the host. Error codes are listed in table 4-2. Codes are divided in functional groups for ease of use. Each group of faults identifies which parameter byte(s) is affected by the fault.

4-41. Run Time and Fault Logs (EEPROM Based)

The Run Time (RT) Error Log and Fault Log contain data error information and fault information, respectively. The Run Time Error Log and Fault Log are stored in an EEPROM on the CEC PCA-A2. The size of the EEPROM limits the total number of entries for both logs to 50. The ERT log is RAM based and contains information on data errors which occur during error rate testing.

NOTE

Maintenance tracks are not used to store fault or error information.

During a run time operation, marginal and nonrecoverable data errors are immediately logged to the Run Time Error Log. The CEC PCA-A2 will not be able to respond to commands for a period of 100 ms while the error information is being stored in the Run Time Error Log. The disc drive does not request release to store the error information. The Read Run Time Error Log utility extracts the run time error information from the EEPROM and returns it to the host.

Faults which occur during utilities/diagnostics and run time activities are, with a few exceptions (see fault ranges), stored in the EEPROM Fault Log. The CEC PCA-A2 will not respond to commands for 100 ms while a fault is being logged. Release is not requested to log a fault. Each fault creates a unique log entry. (An occurrence count of faults is not stored.) The Read Fault Log utility extracts the fault information from the Fault Log and returns it to the host. Error codes are listed in table 4-2. Codes are divided in functional groups for ease of use. Each group of faults identifies which parameter byte(s) is affected by the fault.

4-42. EEPROM

The EEPROM is used as a circular buffer where the oldest information is overwritten once the buffer is full. Since the process of overwriting old fault/error information is anticipated, a fault is not generated when it occurs. There will be a total of 50 entries in the EEPROM. Faults and run time errors are interspersed in the EEPROM. They are distinguishable by the fault code value.

ERROR 20H . . . 3FH
FAULT 1 . . . 1FH, 40H . . . FFH

Note: A fault may be generated when reading from or writing to the EEPROM log. A location in the EEPROM is reserved as a pointer for the circular buffer. If this pointer does not contain a legal EEPROM address a 'corrupted EEPROM' fault is generated. This fault is reported to the host and the EEPROM logs will automatically be cleared in an attempt to restore the logs to a usable state. There are three causes for this fault condition:

(1) The CEC PCA-A2 was shipped from the factory without first initializing the pointer.
(2) The CEC PCA-A2 lost power while updating the pointer.
(3) A hardware problem exists which renders the EEPROM unusable.

The EEPROM structure is as follows:

Bytes 0-2 = Pointer
Bytes 2-7 = Number of sectors read
Bytes 8-507 = Log entries

Run time data errors take the following format in the EEPROM:

Current physical cylinder	2 bytes
Current physical head	1 byte
Current logical cylinder	2 bytes
Current logical head	1 byte
Logical sector	1 byte
Fault Code (most recent error)	1 byte
Error Byte	1 byte
Occurrence Count	1 byte

Faults take the following format in the EEPROM:

Current logical cylinder	2 bytes
Current logical head	1 byte
Target logical cylinder	2 bytes
Target logical head	1 byte
Logical sector	1 byte
Fault Code	1 byte
Status byte	1 byte
Status byte	1 byte

Note: Run time errors and faults take on a slightly different format in the execution message of a read fault log or read run time log utility command. Refer to paragraphs 4-53 and 4-54.

Faults are distinguished from data errors by the fault code number. Errors are in the range 20H through 3FH. Fault code numbers may have any other number except 0 which is reserved.

4-43. Fault Status Bytes

The contents of the two status bytes which are associated with a Fault entry depends on Fault code of that entry. The range of all possible Fault codes (00H . . . FFH) has been divided into subranges for the purpose of defining appropriate contents for the status bytes (refer to table 4-2 for a listing of error codes).

```
 1-1FH   Faults not logged on maintenance track
         Faults not logged in EEPROM
20-3FH   Data errors NO fault log entry
40-4FH   Status1 = compressed ESDI status,
                 Status 2 = vendor unique status
50-5FH   Status1 = 0, Status2 = 0
60-6FH   Status1 = compressed ESDI status,
                 Status2 = vendor unique status
70-8FH   Status1 = Disc Controller IC Status reg,
                 Status2 = Disc Controller IC error reg
90-AFH   Status1 = compressed ESDI status,
                 Status2 = vendor unique status
B0-DFH   Status1 = 0, Status2 = 0
E0-FFH   Status1 = compressed ESDI status,
                 Status2 = vendor unique status
```

Compressed ESDI status:

```
bit 0 = write fault
bit 1 = write gate with track offset
bit 2 = seek fault
bit 3 = invalid or unimplemented command
bit 4 = interface fault
bit 5 = command data parity fault
bit 6 = power on conditions exist
bit 7 = spindle motor stopped
```

Disc Controller IC Status Register:

```
bit 0 = header fault
bit 1 = next disc command
bit 2 = header match completed
bit 3 = local request
bit 4 = remote command busy
bit 5 = local command busy
bit 6 = correction cycle active
bit 7 = error detected
```

Disc Controller IC Error Register:

```
bit 0 = header failed although sector matched
bit 1 = data field error
bit 2 = sector not found
bit 3 = sector overrun
bit 4 = no data sync
bit 5 = FIFO data lost
bit 6 = correction failed
bit 7 = late interlock
```

Vendor Unique status:

Only the least significant byte of the first word of vendor unique status is saved. This information is not available to the field.

4-44. Physical Address Reporting

Faults will normally be reported with a logical address as is shown in paragraph 4-53. If the seek preceding the occurrence of the fault was a physical seek then the current logical cylinder and target logical cylinder will be replaced by a current physical cylinder and a target physical cylinder. The exercisers and test systems are informed of the switch by setting the most significant bit of the cylinder address.

4-45. Run Time Sectors Read Count (Media and EEPROM Based)

The CEC PCA-A2 maintains an estimate of the number of sectors read during run time (i.e., not utility or diagnostic) commands. An estimate of the number of sectors read per head is returned to the host in the header of the read run time log execution message.

The 'estimate' is given to the count for several reasons. The count is not kept on an individual head basis as is the case for the ERT sectors read count. The run time sectors read count is a total for all heads, which is divided by the total number of heads, to give an estimate of the number of sectors read by an individual head.

The count is also compromised by the fact that it is initially kept in RAM. The count is only moved to a more permanent location (maintenance track or EEPROM) when a run time marginal/unrecoverable data error occurs or the utility command PRESET is issued. Therefore, if power is lost before the RAM based count is added to the EEPROM based count, an inaccuracy equal to the RAM based count occurs.

Note: Reading the run time error log also updates the EEPROM count with the total of the RAM based count and the EEPROM count.

4-46. Error Rate Test (ERT) Log

The RAM based ERT table will store data error information on a maximum of 50 locations.

The log is allocated in the following way:

```
        sectors read head 0      5 bytes
        sectors read head 1      5 bytes
                  .                .
                  .                .
                  .                .
        sectors read head N*     5 bytes
                               -----------
                                 80 bytes

*N = 4 for HP 7957A (total bytes = 25 bytes)
*N = 7 for HP 7958A (total bytes = 40 bytes)

entry:physical cylinder        2 bytes
      physical head            1 byte
      physical sector          1 byte  (equal logical sector)
      logical cylinder         2 bytes
      logical head             1 byte
      logical sector           1 byte
      error byte               1 byte
      occurrence count         1 byte
                             ----------
                               10 bytes

              50 entries ===> 500 bytes
```

If the error rate tests are initiated via CS/80 using the 'send execution message' option, errors are reported immediately to the host and are not logged to the ERT log.

Both 'send execution' and 'no execution' ERT utilities keep a count of the sectors successfully read by individual heads. The sectors read count is read by the host through the read ERT log command.

4-47. Error Byte Description

The error byte is used by error rate test utilities and by the run time log to report the location of a data error and its severity to the host.

```
error byte format:
        bit 7 = byte sync (no data sync or sector overrun)
        bit 6 = error in header field
        bit 5 = error in data field
        bit 4 = unrecoverable data error
                (all retries exhausted)
        bit 3 = ECC marginal data error
        bit 2 = retry marginal data error
                (more than 1 retry required)
        bit 1 = recoverable on the first retry
        bit 0 = FIFO data lost or track offset invoked

bits 5-7 describe the location
bits 1-4 describe the severity
```

Bit 0 of the error byte serves two functions.

(1) If bit 0 and bit 1 are set simultaneously, a FIFO data loss has occurred during a write operation. This is a condition from which the write firmware can recover. It is reported because a high frequency of occurrence can affect drive performance. None of the location bits will be set.

(2) The second function is reported when bit 0 is set along with bit 2, bit 3, or bit 4. This implies that the head had to be moved off track center to successfully read data. The error location and severity are accurate.

Note: The recoverable bit (bit 1) will not be set when bit 0 signifies track offset used for data recovery. This is because the first retry is always performed on track center. The two definitions for bit 0 are reported in a unique way so that there should be no confusion as to which meaning to assign to bit 0 if ERT's are run in send execution message mode.

(Confusion can occur when error bytes are "ORed" together in an ERT log entry.)

If a data error occurs more than once at the same location (i.e., same physical cylinder, physical head, and logical sector) on the disc, the error byte is 'OR'ed to give a cumulative report, and the occurrence count is incremented.

4-48. CS/80 No Execution Message Utilities

4-49. Clear Logs

```
MICRO OPCODE : OCDH (205)
PARAMETERS   : 0 = clear all logs (run time/Fault
                   log and ERT log)
               1 = clear ERT log only
               2 = clear EEPROM logs (fault, run time
                   data error)
```

Clearing the ERT log clears all ERT entries. Clearing the fault logs clears all log entries.

4-50. Preset

```
MICRO OPCODE : OCEH  (206)
PARAMETERS   : none
```

This command adds the RAM based run time sectors read count to the EEPROM based sectors read count and stores the total on the maintenance track or in the EEPROM. The RAM based count is cleared.

If this utility is used before scheduled system shutdowns, a more accurate sectors read count will be maintained.

4-51. Faults/Errors During Error Rate Testing

Faults: If a fault is encountered, the ERT is halted and the state of the machine is saved. QSTAT is set and the status will indicate the fault. The host may continue the test by sending the ERT command sequence with the loop count set to zero.

A fault is generated during error rate testing if the ERT log overflows. The host is allowed to read the ERT log, send the clear ERT log command and then continue the error rate test by sending the ERT command sequence with the loop count set to zero.

Errors: If a data error occurs, it will be logged in the ERT log and the test will continue at the next block. QSTAT will be "pass" if only data errors occur.

If no errors have occurred since the last restart of the test, then one byte (containing a zero) tagged with EOI will be returned to the host upon completion of the test.

4-52. CS/80 Send Message Utilities

4-53. Read Fault Log

```
MICRO OPCODE : 0C7H  (199)
PARAMETERS   : none
```

The utility searches through the maintenance track or the EEPROM for any faults which have occurred. These faults are returned to the host in chronological order.

Note: Performing an error rate test does not clear the fault log, so unless the log is specifically cleared before beginning a test, the faults which are returned may have occurred during previous tests or run time activities.

```
Format:

header:
        # of entries          1 byte

(Max. number of entries:  50)
entry:
        Current logical cylinder  2 bytes
        Current logical head      1 byte
        Logical sector            1 byte

        Target logical cylinder   2 bytes
        Target logical head       1 byte
        Logical sector            1 byte

        Fault code                1 byte
        Status                    1 byte
        Status                    1 byte
```

Refer to paragraph 4-43 for a description of the contents of the status bytes. Refer to paragraph 4-44 for a description of physical address reporting for faults.

4-54. Read Run Time Error Log

```
MICRO OPCODE : 0C5H  (197)
PARAMETERS   : head #  (1 byte)
```

The utility searches through the maintenance track or the EEPROM looking for any data errors. The number of data error entries on the selected head and a report on the location of these errors are returned to the host.

Note: Since an entry contains an occurrence count, the total number of errors may exceed the number of entries.

```
header:
         # of entries on the selected head   1 byte
         estimate sectors read by this head  5 bytes
         not used  = 0                       2 bytes
         # of entries on the selected head   1 byte

entry: (selected head only)
         Current physical cylinder           2 bytes
         Current physical head               1 byte
         not used = 0                        1 byte
         Current logical cylinder            2 bytes
         Current logical head                1 byte
         Logical sector                      1 byte
         'Error byte'                        1 byte
         occurrence count                    1 byte
```

The error byte gives information about the location in the sector where the error occurred and the severity of the error (i.e., recoverable, nonrecoverable).

```
error byte format:
    bit 7 = byte sync (no data sync or sector overrun)
    bit 6 = error in header field
    bit 5 = error in data field
    bit 4 = unrecoverable data error
            (all retries exhausted)
    bit 3 = ECC marginal data error
    bit 2 = retry marginal data error
            (more than 1 retry required)
    bit 1 = recoverable on the first retry
    bit 0 = FIFO data lost or track offset invoked
```

4-55. Read Error (ERT) Log

```
MICRO OPCODE : 0C6H  (198)
PARAMETERS   : head #    (1 byte)
```

This utility returns the data error information stored in the RAM based ERT log to the host. Only those data errors which occurred on the specified head are sent to the host.

```
format:

header:
         # of entries on the selected head   1 byte
         # of sectors read by this head      5 bytes
         not used  = 0                       2 bytes
         # of entries on the selected head   1 byte
```

```
entry: (selected head only)
         current phys cyl                    2 bytes
         current phys head                   1 byte
         current phys sector                 1 byte
                  (logical sector)
         current log cyl                     2 bytes
         current log head                    1 byte
         current log sector                  1 byte
         'Error byte'                        1 byte
         occurrence count                    1 byte
```

The error byte gives information about the location in the sector where the error occurred and the severity of the error (i.e., recoverable, nonrecoverable).

```
error byte format:
    bit 7 = Byte sync (no data sync or sector overrun)
    bit 6 = error in header field
    bit 5 = error in data field
    bit 4 = unrecoverable data error
            (all retries exhausted)
    bit 3 = ECC marginal data error
    bit 2 = retry marginal data error
            (more than 1 retry required)
    bit 1 = recoverable on the first retry
    bit 0 = FIFO data lost or track offset invoked
```

If a data error occurs more than once at the same location (i.e., same physical cylinder, physical head, and logical sector) on the disc, the error byte is 'OR'ed to give a cumulative report, and the occurrence count is incremented.

4-56. Measure Seek Time

```
MICRO OPCODE : 0F7H  (247)
PARAMETERS   :   physical cyl  (2 bytes)
                 physical head (1 byte)
```

This utility measures the time required to seek from the present location to the physical track specified by the input parameters. The output consists of 2 bytes which is the seek time in milliseconds. If the seek fails, the fault will be logged in status, QSTAT will equal 1, and the time returned will be zero.

4-57. Read Spare Table

```
MICRO OPCODE : 0C4H  (196)
PARAMETERS   :   Table = 1 (spare table)
```

The spare table is the only accessible table in this controller. Since the spare table is not stored on maintenance tracks, it must be built on power up. This is done by going to the spare track area and seeing which have been allocated. Reading the spare table only reports spared tracks. Sector spares are not reported.

```
     HEADER
Head #                              1 byte
# of field track spares             2 bytes (MSB first)
# of spare tracks used              1 byte
# of logical spared tracks          1 byte

     ENTRY
Cylinder High                       1 byte
Cylinder low                        1 byte
Scalar #                            1 byte
```

The 'head #' is the head address. There will be one header for each head in the drive.

The '# of field track spares' is the number of spare tracks on this head which have been allocated during field sparing operations.

The '# of spare tracks used' is the total number of spare tracks on this head that have been allocated by factory and field sparing operations.

The '# of logical spared tracks' is the number of tracks on this head which have been determined to be defective and were spared. The number of logical spared tracks will be equal to the number of entries.

The 'scalar #' indicates which of the spare tracks on a surface were used when the defective track was spared. For example, if there are 6 (0 through 5) spare tracks per surface, and the second spare track was used by this entry, then the scalar # would be 1.

4-58. Locate And Read Full Sector

```
MICRO OPCODE : OCOH  (192)
PARAMETERS   :   physical cylinder     (2 bytes)
                 physical head         (1 byte)
                 physical sector       (1 byte)
                 (logical sector)
```

The utility will read a physical sector and return the 256 data bytes from that sector and the 6 ECC bytes. The total execution message will be 262 bytes long. Faults will show up in the status, but data errors are neither detected nor reported.

Headers are not read by the read full sector command.

4-59. Servo Test

```
MICRO OPCODE : OBFH  (191)
PARAMETERS   : Loop count
```

This utility will perform seeks to the following tracks: 0, 1, 2, 4, 8, 16, 32, . . . n, 0, n, n-1, n-2, n-4, n-8, n-16, n-32, . . . 0 (n = max log track). This sequence of seeks is repeated once for each head.

A seek failure or a timeout will be reflected in the status as well as the first byte of the execution message. A seek error will only be reflected in the first byte of the execution message. A seek error results if the header is readable, and it shows the head is not on target track.

Servo test can be canceled or cleared for early termination.

The test will halt and return the execution message as soon as the first failure occurs.

```
execution message:
   byte 1:  0 = pass                QSTAT 0
            1 = seek failure        QSTAT 1
                (timeout, header read failed)
            2 = seek error          QSTAT 0
                 (target versus actual different)

   byte 2, 3:  Number of seeks completed in the last loop.
```

4-60. Pattern Error Rate Test (ERT) (Log Option)

```
MICRO OPCODE : 0C8H  (200)
PARAMETERS   : LOOP    (0-255) 255 implies infinite loop
             : OFFSET  (XXXXXXXX)
             : REPORT  (XXXXXXXX)
             : TEST AREA       0 = SECTOR
                               1 = TRACK
                               2 = CYLINDER
                               3 = SURFACE
                               4 = VOLUME (the whole disc)
             : PATTERN SELECT  0 = change pattern with
                                   each loop
                               1 = 39CE7H
                               2 = C30H
                               3 = 30E61CC3987H
                               4 = B8F32E3CCH
                               5 = CCH
                               6 = DB6H
                               7 = 33F94CFE5H
                               8 = random data
```

No Message Option: This utility stores the addresses of data errors in the ERT Log.

Send Message Option: This utility will report data errors to the host immediately after they occur. The errors are not stored in the ERT log.

The sector count is updated for each head.

The first loop of the test begins at the target address which should be determined by the complementary command 'Set Address'. If the target address is in the middle of the test area, the first pass will consist of writing from the target address to the end of the test area. The first read operation will also be from the

target address to the end of the test area. The second loop and each loop thereafter will be from the start of the test area to the end of the test area.

Each loop consists of writing and reading the test area. If the loop count is set to 255, the test will continue indefinitely until a CANCEL or CLEAR command is sent from the host.

If a fault occurs, the test will halt; QSTAT is set; status will indicate the fault.

If a data error occurs, the execution message has the following format:

```
 (no header is sent)
entry:
       current phys cyl              2 bytes
       current phys head             1 byte
       current logical sector        1 byte
       current logical cyl           2 bytes
       current logical head          1 byte
       current logical sector        1 byte
       error byte                    1 byte
       loop count when error occurred 1 byte

error byte format:
   bit 7 = byte sync (no data sync or sector overrun)
   bit 6 = error in header field
   bit 5 = error in data field
   bit 4 = unrecoverable data error
           (all retries exhausted)
   bit 3 = ECC marginal data error
   bit 2 = retry marginal data error
           (more than 1 retry required)
   bit 1 = recoverable on the first retry
   bit 0 = FIFO data lost or track offset invoked
```

The state of the test is saved when an error or fault occurs. After reporting the error/fault, the test may be continued by re-sending the ERT command sequence with the loop count set to zero.

At the end of the test (loop count exhausted), one byte (containing a zero) tagged with EOI will be sent to the host.

4-61. Random Pattern Error Rate Test (Log Option)

```
MICRO OPCODE : OCBH  (203)
PARAMETERS   : LOOP    (0-255) 255 implies infinite loop
             : OFFSET  (XXXXXXXX)
             : REPORT  (XXXXXXXX)
             : PATTERN SELECT  0 = change pattern with
                                   each loop
                               1 = 39CE7H
                               2 = C30H
                               3 = 30E61CC3987H
```

```
                                    4 = B8F32E3CCH
                                    5 = CCH
                                    6 = DB6H
                                    7 = 33F94CFE5H
                                    8 = random data
```

The Random Pattern ERT functions exactly like the nonrandom Pattern ERT with the exception that the test area is randomly generated. This is done by generating a random starting address and then generating a random transfer length between 1 sector and 64 sectors. It is assumed that random error rate test is allowed to read and write anywhere in the logical data space of the disc. If the randomly generated transfer length would go beyond the disc boundaries the length is truncated to fit within the disc volume.

The sector count is updated for each head.

Refer to paragraph 4-59 for details on execution message.

4-62. Read Only Error Rate Test (Log Option)

```
MICRO OPCODE : 0C9H  (201)
PARAMETERS   : LOOP    (0-255) 255 implies infinite loop
             : OFFSET  (XXXXXXXX)
             : REPORT  (XXXXXXXX)
             : TEST AREA       0 = SECTOR
                               1 = TRACK
                               2 = CYLINDER
                               3 = SURFACE
                               4 = VOLUME (the whole disc)
```

No message option: This utility will store the addresses of data errors in the ERT Log and fault descriptions.

Send message option: This utility will report data errors to the host as soon as they occur.

The sector count is updated for each head and is available by reading the ERT log. As the name implies, this test does not write data on the disc. Therefore, data written previous to calling this utility will not be destroyed.

The first loop of the test begins at the target address which should be determined by the complementary command 'Set Address'. If the target address is in the middle of the test area, the first pass will consist of reading from the target address to the end of the test area. Each loop thereafter will begin at the start of the test area.

If a fault occurs, the test will halt; QSTAT is set; status will indicate the fault.

If a data error occurs, the execution message has the following format:

```
 (no header is sent)
entry:
       current phys cyl              2 bytes
       current phys head             1 byte
       current phys sector           1 byte
        (current logical sector)
                                     (equals 0)
       current logical cyl           2 bytes
       current logical head          1 byte
       current logical sector        1 byte
       error byte                    1 byte
       loop count when error occurred 1 byte
error byte format:
    bit 7 = byte sync (no data sync or sector overrun)
    bit 6 = error in header field
    bit 5 = error in data field

    bit 4 = unrecoverable data error
            (all retries exhausted)
    bit 3 = ECC marginal data error
    bit 2 = retry marginal data error
            (more than 1 retry required)
    bit 1 = recoverable on the first retry
    bit 0 = FIFO data lost or track offset invoked
```

The state of the test is saved when an error or fault occurs. After reporting the error/fault, the test may be continued by re-sending the ERT command sequence with the loop count set to zero.

At the end of the test (loop count exhausted), one byte (containing a zero) tagged with EOI will be sent to the host.

4-63. Random Read Only Error Rate Test (Log Option)

```
MICRO OPCODE : 0CCH  (204)
PARAMETERS   : LOOP    (0-255) 255 implies infinite loop
```

This routine functions like the Read Only Error Rate test. The one exception is that the TEST AREA is generated randomly. This is done by generating a random starting address and then generating a random length between 1 sector and 64 sectors. If the random length exceeds the length between the starting address and the end of the disc volume, the length will be truncated to stop at the volume boundary.

Refer to paragraph 4-62 for details on the execution message.

4-64. Read Revision Numbers

```
MICRO OPCODE : 0C3H (195)
PARAMETERS    : none
```

This utility will read the firmware ROM revision numbers and return them in an execution message. The first byte specifies the number of revision number bytes that will follow.

```
byte #
   0     number of bytes to follow
         (equals 1 since there is only one ROM)
   1     revision # for ROM
```

The format for the revision byte is for the most significant nibble to contain the main revision number, and for the least significant nibble to contain a secondary revision number.

4-65. Troubleshooting

When troubleshooting the disc drive, the first thing to do is to determine if the fault is repeatable or intermittent. A repeatable fault usually causes the same self-test fail result to be presented each time self test is performed. An intermittent fault, on the other hand, occurs at random intervals, and may not always cause a self-test failure.

In the case of a repeatable fault, self test will identify the failing FRA with a 95 percent certainty. In the event that more than one FRA is lsited as the possible cause of the failure, replace the FRA's one at a time, in the order given in the self-test display.

NOTE

Cable faults (an open cable conductor, loose cable connector, etc.) may present a multiple FRA failure message. The FRA's listed will be the FRA's at either end of the defective cable. All cabling should therefore be checked before replacing any FRA's.

Cables W1 and W3 are sufficiently long to allow PCA-A1 (disc drive assembly A1) to be connected into the circuit adjacent to the disc drive cabinet. This allows a substitute PCA-A1 to be connected into the circuit without removing PCA-A1 from the cabinet.

Attempt to isolate the fault to a specific FRA by running self test following the replacement of each FRA.

Table 4-2. Error Codes (1 of 6)

Miscellaneous errors. These errors are caused by externally initiated operations. These errors do not cause a fault log entry to be generated. Only error 1C-1FH will affect P7.

Oct	Dec	Hex	Description
010	01	01	End Of Volume
020	02	02	Channel Parity Error
050	05	05	Illegal Opcode
070	07	07	Address Bounds
100	08	08	Parameter Bounds
110	09	09	Illegal Parameter
120	10	0A	Message Sequence
130	11	0B	EEPROM diagnostic failed. (EEPROM only)
140	12	0C	Message Length
200	16	10	No spares available on this head.
210	17	11	Media wear - one or fewer spare tracks left on this head after this sparing operation.
220	18	12	Power on initialization.
270	23	17	FIFO Data Loss on Read successful retries.
300	24	18	FIFO Data Loss on Write successful retries.

NOTE

THE FOLLOWING ERRORS WILL AFFECT P7:

360	30	1E	Corrupted EEPROM log. (EEPROM only)
370	31	1F	No acknowledge or R/W retries exhausted. (EEPROM only)

Data errors (media related data bit errors). A run log entry will be generated. In the Request Status parameter bytes, P7 will contain the error code.

400	32	20	Data field - marginal data error - on a read operation.
410	33	21	Data field - marginal data error - correction operation was used to recover the data.
420	34	22	Data field - uncorrectable data error on read.
430	35	23	Marginal Header Failed Although Sector Matched error on a read operation.
440	36	24	Unrecoverable Header Failed Although Sector Matched error on a read operation.
450	37	25	Marginal Sector Not Found error on a read operation.
460	38	26	Unrecoverable Sector Not Found error on a read operation.
470	39	27	Marginal No Data Sync error on a read operation.
500	40	28	Unrecoverable No Data Sync error on a read operation.
510	41	29	Marginal Sector Overrun error on a read operation.
520	42	2A	Unrecoverable Sector Overrun error on a read operation.
570	47	2F	Unrecoverable data error on write operation (header not readable).
630	51	33	Marginal Header Failed Although Sector Matched error on a write operation.
640	52	34	Unrecoverable Header Failed Although Sector Matched error on a write operation.

Table 4-2. Error Codes (2 of 6)

Oct	Dec	Hex	Description
650	53	35	Marginal Sector Not Found error on a write operation.
660	54	36	Unrecoverable Sector Not Found error on a write operation.
670	55	37	Marginal No Data Sync error on a write operation.
700	56	38	Unrecoverable No Data Sync error on a write operation.
710	57	39	Marginal Sector Overrun error on a write operation.
720	58	3A	Unrecoverable Sector Overrun error on a write operation.

Self test errors. A fault log entry will be generated. In the Request Status parameter bytes, P7 will contain the fault code, P8 will contain the ESDI status, P9 will contain the least significent byte (LSByte) of Vendor Unique Status.

1010	65	41	Buffer RAM test failed.
1020	66	42	Self test data compare failed.
1030	67	43	Self test R/W retry count exhausted.
1040	68	44	ECC test failed.
1050	69	45	Drive selected line not asserted during power on.
1060	70	46	Timeout 30 seconds waiting for Command Complete during power on.
1070	71	47	Illegal ESDI status during power on.
1100	72	48	Drive Ready not asserted after Command Complete during power on.
1110	73	49	Auto configuration failed; probably ESDI communication problem (no configuration parameters checked).
1130	75	4B	Reset attention failed during power on.
1140	76	4C	Vendor unique status available.
1150	77	4D	Mechanism self test has failed.
1160	78	4E	One of the four seek diagnostic tests failed (ATN, ESDI comm, verify failed twice).

Controller Faults. A fault log entry will be generated. In the Request Status parameter bytes, P7 will contain the fault code.

1220	82	52	FIFO data loss retry on a read operation failed.
1230	83	53	FIFO Data Loss Retry on a write operation failed.
1240	84	54	Offset recovery position unknown.
1250	85	55	Seek recovery position unknown.

COMPRESSED ESDI STATUS

```
0 = write fault
1 = write gate with track offset fault
2 = seek fault
3 = invalid/unimplemented command fault
4 = interface fault
5 = command data parity fault
6 = PON conditions exist/start spindle motor command may be required
7 = spindle motor stopped
```

Table 4-2. Error Codes (3 of 6)

Controller faults with Disc Data Controller (DDC) IC status. A fault log entry will be generated and the fault log entry will include the Disc Data Controller (DDC) IC status. In the Request Status parameter bytes, P7 will contain the fault code, P8 will contain the Disc Data Controller (DDC) IC Status register, and P9 will contain the Disc Data Controller (DDC) IC Error register.

Oct	Dec	Hex	Description
1400	96	60	Disc Data Controller (DDC) IC timed out when trying to read sector headers (0-63).
1410	97	61	Error detected during read full sector.
1420	98	62	Disc Data Controller (DDC) IC indicates a fatal fault on a read operation.
1430	99	63	Disc Data Controller (DDC) IC indicates a fatal fault on a write operation.
1440	100	64	Retries exhausted during Format Track.
1450	101	65	Retries exhausted during verify initialize. No header was readable on track.
1460	102	66	Retries exhausted during Read Header.
1470	103	67	This should not directly cause a bit in status to be set. It is used by Wait For INT or ATN (a low level routine) to call Save drive info and get the right information stored away.
1500	104	68	Disc Data Controller (DDC) IC timeout when trying to read any header for sparing.
1510	105	69	Disc Data Controller (DDC) IC timeout when formatting a spare track to deallocate it.
1520	106	6A	Disc Data Controller (DDC) IC timeout while formatting a track to flag a sector defective.
1530	107	6B	Disc Data Controller (DDC) IC timeout while formatting the spare track before the data is written.
1540	108	6C	Retries exhausted during format track; last problem was Disc Data Controller (DDC) IC timeout.
1550	109	6D	Retries exhausted during Read Header operation; last problem was Disc Data Controller (DDC) IC timeout.
1560	110	6E	Retries exhausted when verifying initialize; last problem was Disc Data Controller (DDC) IC timeout.

Unit fault with Disc Data Controller (DDC) IC status. A fault log entry will be generated and the fault log entry will include the Disc Data Controller (DDC) IC status. In the Request Status parameter bytes, P7 will contain the fault code, P8 will contain the Disc Data Controller (DDC) IC status, P9 will contain the Disc Data Controller (DDC) IC error register.

1610	113	71	Error Detected (ED) bit set in Disc Data Controller (DDC) IC during read defect list.
1620	114	72	Failed due to Disc Data Controller (DDC) IC error while formatting a track to flag a sector defective.
1630	115	73	Failed due to Disc Data Controller (DDC) IC error while formatting the spare track for track sparing.
1640	116	74	Failed due to an Disc Data Controller (DDC) IC error while formatting a spare track to deallocate it.
2010	129	81	FIFO data loss occurred on a read operation.
2020	130	82	FIFO data loss occurred on a write operation.

Table 4-2. Error Codes (4 of 6)

Oct	Dec	Hex	Description
2030	131	83	Header failed although sector number matched error (missed seek if head error bit not set in Disc Data Controller (DDC) IC status register). (EEPROM only)
2040	132	84	Data field error occurred. (EEPROM only)
2050	133	85	No data sync, Sector overrun, Sector not found. (EEPROM only)
2060	134	86	Correction failed error erroneously set.
2070	135	87	Late interlock error erroneously set.
2080	136	88	Illegal DDC status detected in utilities.
Unit fault with Compressed ESDI status. A log entry will be generated and the fault entry will include the compressed ESDI status. In the Request Status parameter bytes, P7 will contain the fault code, P8 will contain the compressed ESDI status, P9 will contain the LSByte of Vendor Unique Status.			
2210	145	91	ESDI status indicates a fatal fault on a read operation.
2220	146	92	ESDI status indicates a fatal fault on a write operation.
2230	147	93	Retry of Write Fault (Offtrack on write) was unsuccessful.
2240	148	94	Retry of Write with Offset (aggressive seek on write) failed.
2250	149	95	Drive set attention during read headers (verify position).
2260	150	96	Local write expected an offtrack write error but received another ESDI error instead.
2270	151	97	ATN set during read full sector.
2300	152	98	ATN set during read defect list.
2310	153	99	ESDI command utility failed.
2320	154	9A	Retries exhausted during format track. Track probably did not get formatted.
2330	155	9B	Retries exhausted during verify initalize. No header readable on a track.
2340	156	9C	Retries exhausted during read headers operation.
2350	157	9D	Used by low level routine (wait for INT or ATN). Should not directly affect status. Used when calling save-drive-information to save the right information.
2360	158	9E	Logs unreadable due to unrecoverables on all copies.
2370	159	9F	Logs unreadable due to no valid copies.
2400	160	A0	Failed due to ATN being set by the drive while formatting a track to flag a sector defective.
2410	161	A1	Failed due to ATN being set by the drive while formatting the spare track before the data is written on it.
2420	162	A2	Failed due to ATN being set by the drive while reading any header for sparing.
2430	163	A3	Failed due to ATN being set by the drive while formatting a track to deallocate a spare.
2470	167	A7	HDA did too many internal recalibrations in a utility.
2500	168	A8	ATN set to many times during a write (write fault).
2510	169	A9	A fatal fault was detected (probably on a seek).
2520	170	AA	Local read saw ATN set (fatal so no retries).
2530	171	AB	A check of the HDA saw it was deasserted.

Table 4-2. Error Codes (5 of 6)

Unit Faults. A log entry will be generated and the extra byte in the fault entry will be zero. In the Request Status parameter bytes, P7 will contain the fault code. P8 through P10 will be zeroes.

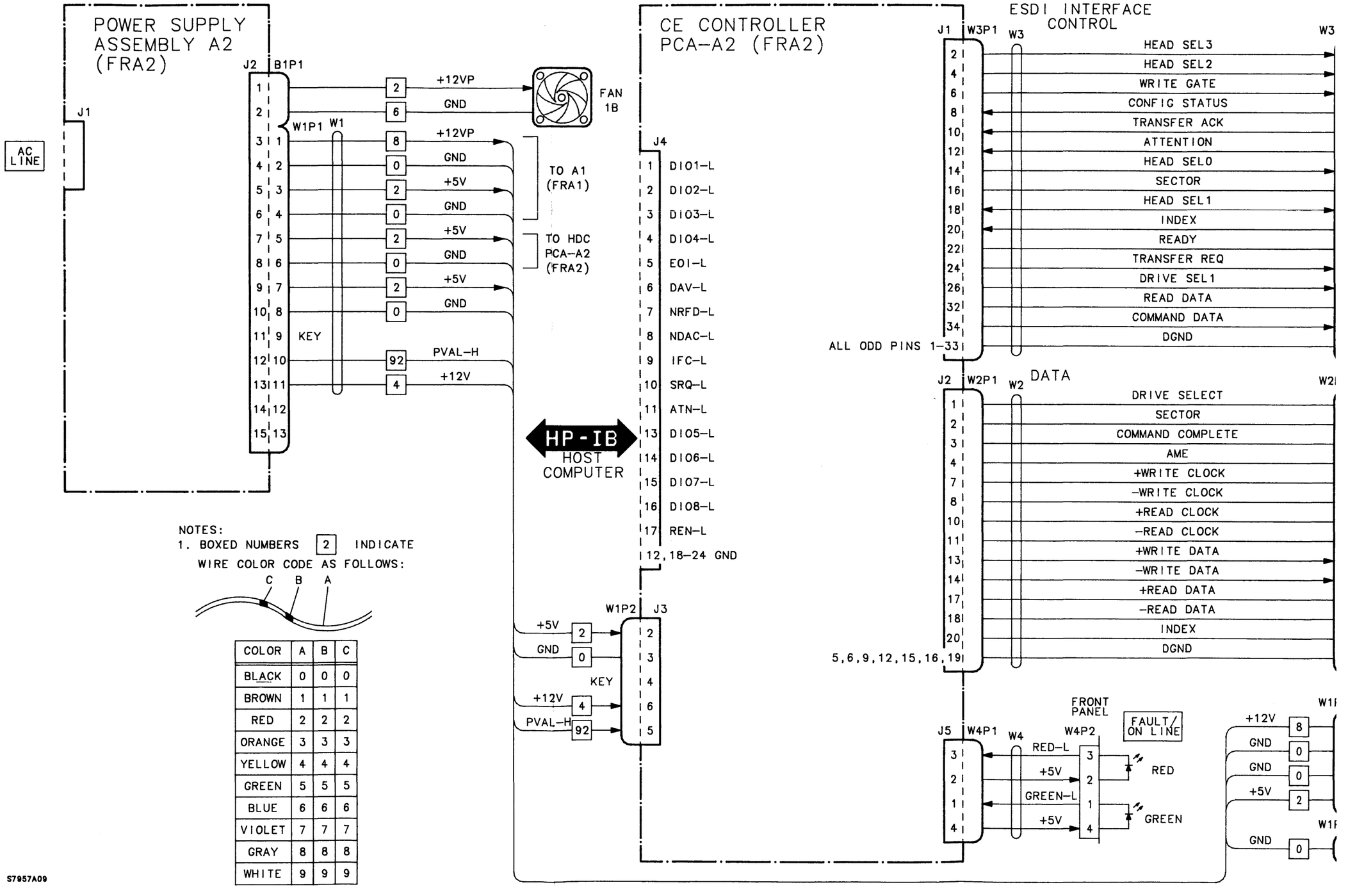
Oct	Dec	Hex	Description
2600	176	B0	Logical seek timeout.
2610	177	B1	Physical seek timeout.
2620	178	B2	Defective track reached when doing a logical seek (field spare deallocation).
2630	179	B3	When seeking back to defective track to flag it defective, header is not logical cylinder or head.
2640	180	B4	Headers bad when flagging a sector defective.
2650	181	B5	Defective sector header not found when sector sparing.
2660	182	B6	Headers on spare track bad after they tested good (when writing logical headers).
2700	184	B8	Cannot read any headers for sparing. (EEPROM only)
2710	185	B9	Header unrecoverable during write of data for sparing. (EEPROM only)
2720	186	BA	Header failed although sector matched without Header Fault - seek retried successfully - but retry of read not successful.
2730	187	BB	Header failed although sector matched without Header Fault - seek retried successfully - but retry of write not successful.
2740	188	BC	Reseek in local operation failed.
2760	190	BE	No Disc Data Controller (DDC) IC interrupt while reading the defect list.
2770	191	BF	No Disc Data Controller (DDC) IC interrupt while reading full sector.
3000	192	C0	ERT log overflow
3010	193	C1	Cannot read disc logs during power up.
3030	195	C3	Verify position failed after initialize media - cylinder and head in header did not match as expected.
3050	197	C5	The Disc Data Controller (DDC) IC timed out during an ECC correction cycle.
3060	198	C6	Bad parity on EEPROM data read. (EEPROM only)
3070	199	C7	All headers bad on a track during format option 2.
3100	200	C8	Headers unreadable during verify position (servo test).
3110	201	C9	Header does not match logical target address (seek diagnostic).
3120	202	CA	Hardware fault other than Disc Data Controller (DDC) IC fault. (EEPROM only)
3130	203	CB	Disc Data Controller (DDC) IC communication time out.
3140	204	CC	Unrecoverable data error occurred.
3150	205	CD	Two spare tracks in a row were bad when sparing attempted (includes section spares).
3200	208	D0	Transfer acknowledged set timed out after transfer request was set (took longer than 10 milliseconds).
3210	209	D1	Transfer acknowledged reset timed out after transfer request was reset (took longer than 10 milliseconds).
3220	210	D2	Command timed out (Command Complete was not asserted a specified time after the command was sent).
3230	211	D3	Command retried out (number of times a command was retried exceeded the retry count).
3250	213	D5	Request ESDI status command failed.

Table 4-2. Error Codes (6 of 6)

Oct	Dec	Hex	Description
3260	214	D6	Reset Attention command failed.
3270	215	D7	HDA timed out while controller waited for command complete before sending a command.
3300	216	D8	Timeout on auto recalibrate during a read or write.
3340	220	DC	Command Complete signal drop out on a read operation.
3350	221	DD	Command Complete signal drop out on read retry.
3360	222	DE	Command Complete signal drop out on write.
3370	223	DF	Command Complete signal drop out on a write retry.

Unit fault that is logged only. A log entry will be generated and the fault log entry will contain the Compressed ESDI status. No bits will be set in the Request Status bytes.

3400	224	E0	ESDI attention line set.
3410	225	E1	ESDI command retried.
3420	226	E2	Bad parity detected on read data.
3430	227	E3	Header failed although sector matched on read operation without a Header Fault - Seek retried OK - Read retried OK.
3440	228	E4	Header failed although sector matched for write operation.
3450	229	E5	Retry of a Write Fault (Offtrack) successful.
3460	230	E6	Retry of a Write with Offset (Aggressive seek on write) successful.
3560	238	EE	Retries required during Format Track.
3570	239	EF	Retries required during Read Headers. Recovery was successful.
3600	240	F0	Seek error header does not match target (servo test).
3610	241	F1	Timed out waiting for operation complete INT during Disc Data Controller (DDC) IC reset.
3630	243	F3	The Reserved Interrupt Vector was taken.
3640	244	F4	The SWI3 Interrupt Vector was taken.
3650	245	F5	The SWI2 Interrupt Vector was taken.
3660	246	F6	The SWI1 Interrupt Vector was taken.
3670	247	F7	The NMI Interrupt Vector was taken.
3700	248	F8	Seek missed target track during a read retry.
3710	249	F9	Seek missed target track during a write retry.
3720	250	FA	Write fault during write in utilities (retried).
3730	251	FB	HDA auto recal detetected in utilities.



NOTES:
1. BOXED NUMBERS [2] INDICATE WIRE COLOR CODE AS FOLLOWS:

COLOR	A	B	C
BLACK	0	0	0
BROWN	1	1	1
RED	2	2	2
ORANGE	3	3	3
YELLOW	4	4	4
GREEN	5	5	5
BLUE	6	6	6
VIOLET	7	7	7
GRAY	8	8	8
WHITE	9	9	9

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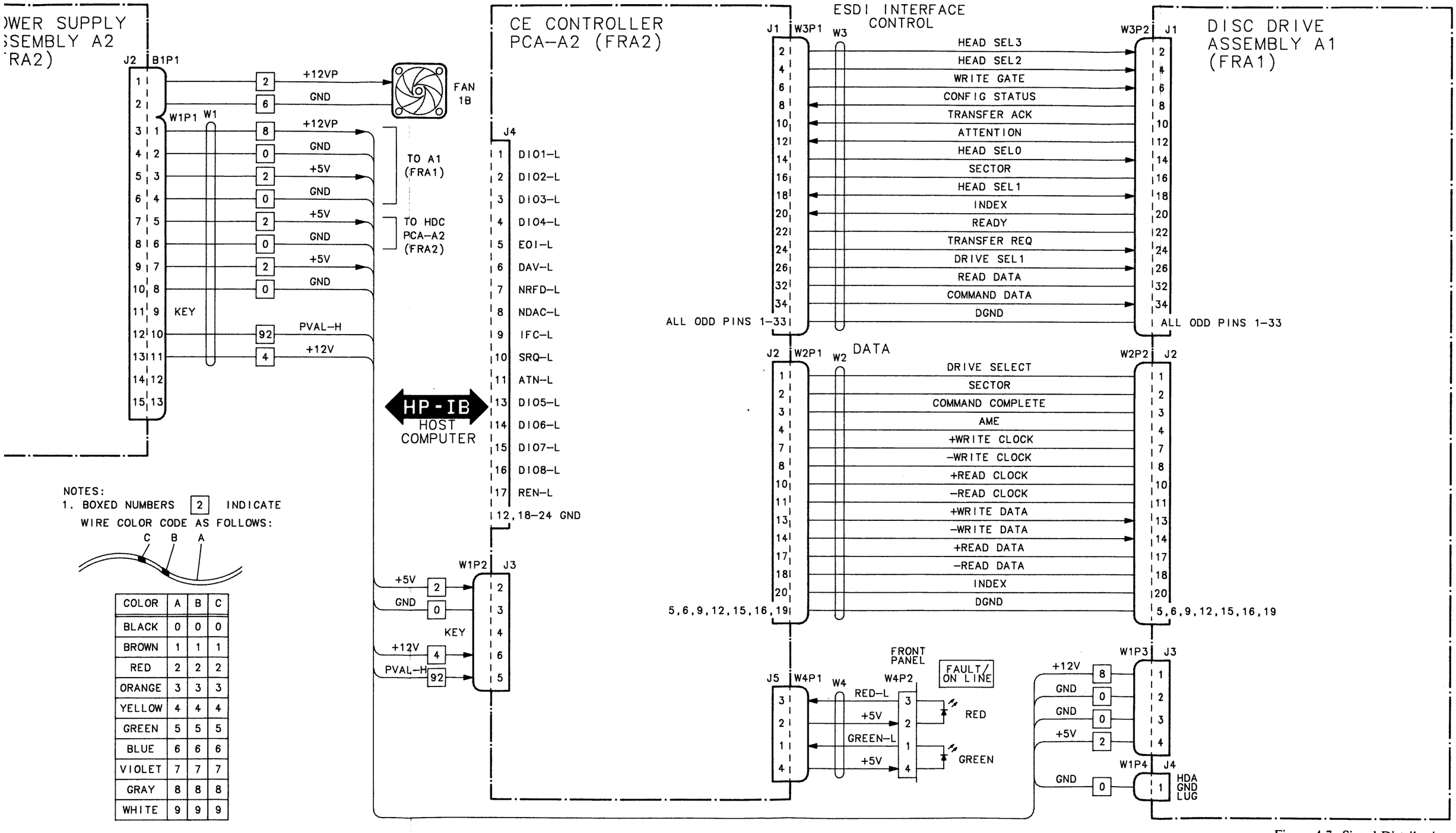

NOTES:
1. BOXED NUMBERS [2] INDICATE WIRE COLOR CODE AS FOLLOWS:

COLOR	A	B	C
BLACK	0	0	0
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ORANGE	3	3	3
YELLOW	4	4	4
GREEN	5	5	5
BLUE	6	6	6
VIOLET	7	7	7
GRAY	8	8	8
WHITE	9	9	9

Figure 4-7. Signal Distribution

Removal and Replacement 5

CAUTION

Failure to tighten the screws properly may result in the disc drive not meeting the RFI specifications.

5-1. INTRODUCTION

WARNING

The disc drive does not contain operator serviceable parts. To prevent electrical shock, refer all service activities to service-trained personnel.

CAUTION

- The field-replaceable assemblies (FRA's) in the disc drive are electrostatic-sensitive devices. Take appropriate precautions when removing the FRA's from the disc drive. Use of an anti-static pad and wrist strap is required. (These components are contained in the anti-static work station, part no. 9300-0749.) Immediately after removal, store the FRA's in anti-static, conductive plastic bags.

- The disc drive is delicate and should be handled with care. Also, the disc drive is heavier (10.9 kilograms/24.0 pounds) than its size would indicate.

- Do not turn the LINE~ switch on or off when the system is transferring data on the Hewlett-Packard Interface Bus (HP-IB).

- Do not cycle the LINE~ switch on and off unnecessarily.

- Do not connect or disconnect the HP-IB cable assembly(s) from the disc drive when the system is transferring data on the HP-IB.

This chapter provides removal and replacement procedures for field-replaceable assemblies (FRA's) and parts in the disc drive. Procedures are given in the order in which disassembly normally occurs. Each part or assembly which must be removed before access can be gained to another assembly or part is presented first, followed by the next assembly which can be removed. This disassembly order is shown in figure 5-1. The locations of the FRA's are shown in figure 4-1. Figures 4-2 through 4-5 identify the connectors on the FRA's and their mating cable assembly connectors. Figure 4-5 provides an overall cabling diagram of the disc drive. References are also made to Figure 6-1, Disc Drive, Exploded View, to assist in identifying and locating parts.

NOTE

TORX* hardware is used in the disc drive. This hardware requires the use of special drivers. In this manual, any reference to this type of hardware will be accompanied by the required driver size (for example, "T15").

*TORX is a registered trademark of the Camcar Division of Textron, Inc.

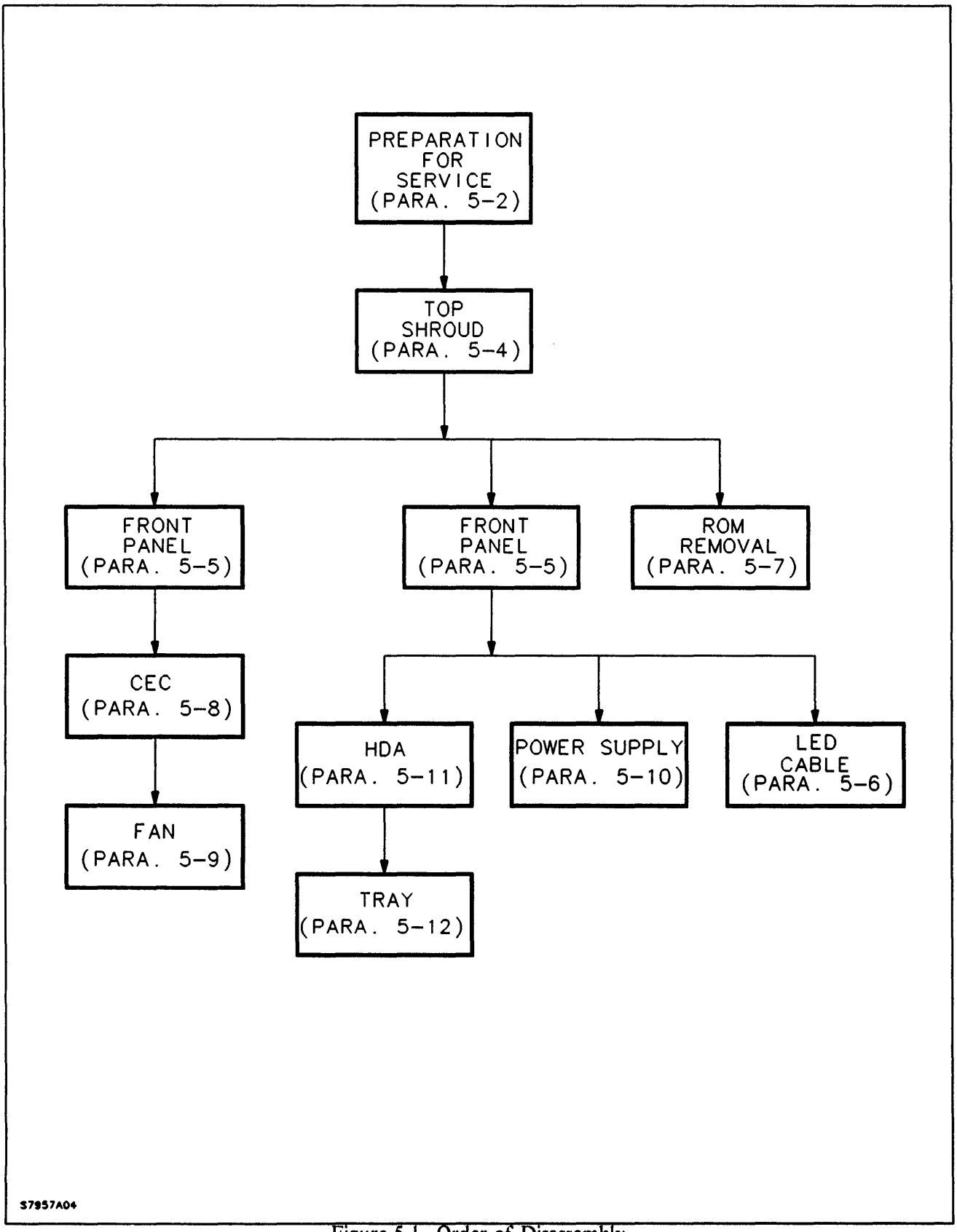


Figure 5-1. Order of Disassembly

5-2. PREPARATION FOR SERVICE

Before starting any removal or replacement procedure, prepare the disc drive for service as follows:

a. Set the disc drive LINE~ switch to the 0 (out) position and disconnect the power cord from the ~AC LINE connector.

b. Disconnect the HP-IB cable assembly from the disc drive HP-IB connector.

c. Place the disc drive on the anti-static pad and connect the wrist strap to the pad. When the top shroud is removed (paragraph 5-4), ground the frame of the disc drive to the pad.

CAUTION

Ensure that the anti-static wrist strap is attached to the wrist before removing or replacing any components in the disc drive.

5-3. REMOVAL AND REPLACEMENT

Removal and replacement instructions for field-replaceable assemblies (FRA's) and parts in the disc drive are provided in the following paragraphs. Unless otherwise specified, replacement is a reversal of the removal instructions.

5-4. TOP SHROUD

To remove the top shroud (1, figure 6-1), proceed as follows:

a. Perform the preparation for service procedure outlined in paragraph 5-2.

b. Ensure that the power cord is disconnected from the ~AC LINE connector on the rear panel of the disc drive.

c. Remove the three T10 screws (2, figure 6-1) which secure the top shroud to the disc drive.

d. Raise the rear of the top shroud upward slightly and then move it backward and away from the disc drive.

e. Ground the frame of the disc drive to the anti-static pad.

Reinstallation is a reversal of the removal procedure.

5-5. FRONT PANEL

To remove the front panel (3, figure 6-1) from the disc drive, proceed as follows:

a. Perform the preparation for service procedure outlined in paragraph 5-2.

b. Ensure that the power cord is disconnected from the ~AC LINE connector on the rear panel of the disc drive.

c. Remove the top shroud (refer to paragraph 5-4).

d. Remove the four T10 screws (7) which secure the front shield (4), with front panel (3) and LED cable assembly W4 (5), to the disc drive. Move the front panel forward away from the disc drive.

e. Disconnect connector P1 on LED cable assembly W4 (5) from connector J5 on PCA-A2 (9) and remove the front panel (3) from the disc drive.

f. If it is necessary to remove the front panel shield (4) from the front panel (3), proceed as follows:

1) Remove the four T25 screws (8) which secure the front panel shield (4) to the front panel (3).

2) Remove W4 LED cable assembly (5) from the forks which secure it to the front panel shield (4).

3) Remove the front panel shield (4) from the front panel (3).

Torque Specifications: For item (7) screw torque to 14 in./lbs with T-10 bit.

Reinstallation is a reversal of the removal procedure. Ensure that the cable assembly connector disconnected in step e is properly seated in its mating connector. Check also that the LINE~ switch operates freely before tightening the four T10 screws (7) removed in step d.

5-6. LED CABLE REMOVAL

a. Perform the preparation for service outlined in paragraph 5-2.

b. Ensure that the power cord is disconnected from the ~AC LINE connector on the rear panel of the disc drive.

c. Remove the top shroud (refer to paragraph 5-4) and the front panel (refer to paragraph 5-7).

d. Remove the four T25 screws (8) that hold the front panel shield (4) to the front panel (3).

e. Lift the front panel shield (4) from the front panel (3) and remove the LED cable (5) from the front panel.

5-7. ROM REMOVAL

To remove the ROM (9, figure 6-1), proceed as follows:

a. Perform the preparation for service procedure outlined in paragraph 5-2. Pay particular attention to the instructions given for use of the anti-static pad and wrist strap.

b. Ensure that the power cord is disconnected from the ~AC LINE connector on the rear panel of the disc drive.

c. Remove the top shroud (refer to paragraph 5-4).

d. Remove the ROM (10) from the 28-pin socket on PCA-A2 (9). See figure 4-6 for the location of U2. Place the ROM on a piece of anti-static foam.

Reinstallation is a reversal of the removal procedure. ROM is labeled U2. Ensure that the EPROM is installed in its matching 28-pin socket on PCA-A2 (9), with the index notch on the ROM facing toward the edge of PCA-A2 (see figure 4-5).

5-8. CS80/ESDI CONTROLLER (CEC) PCA-A2

To remove PCA-A2 (9, figure 6-1) from the disc drive, proceed as follows:

a. Perform the preparation for service procedure outlined in paragraph 5-2.

b. Ensure that the power cord is disconnected from the ~AC LINE connector on the rear panel of the disc drive.

c. Remove the top shroud (refer to paragraph 5-4).

CAUTION

Item 12 in step d is made of a conductive zinc-plated material. Do not substitute this part (HP Part No. 0380-1918) with any other part. Failure to use the correct part will mean that this disc drive will most likely not meet the RFI specifications.

d. Remove the two 6-32 hex standoffs (12) and lock washers (13) which secure the HP-IB connector on PCA-A2 (9) to the rear panel of the disc drive.

e. Disconnect connector P2 on power cable assembly W1 (14) from connector J3 on PCA-A2 (9).

f. Disconnect connectors W2P1 (16) and W3P1 (15) on the ribbon cable assemblies from connectors J2 and J1, respectively, on PCA-A2 (9).

g. Disconnect connector P1 on LED cable assembly W4 (5) from connector J5 on PCA-A2.

h. Slide PCA-A2 (9) forward and out of the disc drive.

Reinstallation is a reversal of the removal procedure. Ensure also that the cable assembly connectors disconnected in steps e and f are firmly seated in their mating connectors.

5-9. FAN

To remove the fan (17, figure 6-1) from the disc drive, proceed as follows:

a. Perform the preparation for service procedure outlined in paragraph 5-2.

b. Ensure that the power cord is disconnected from the ~AC LINE connector on the rear panel of the disc drive.

c. Remove the top shroud (refer to paragraph 5-4), PCA-A2 (refer to paragraph 5-6), and the front panel (refer to paragraph 5-7).

d. Remove the standoffs on the Controller PCA-A2 (refer to paragraph 5-8) and slide the PCA forward to gain access to the fan.

e. Remove the four T20 screws (19) and grille (18) which secure the fan (17) to the rear panel.

f. Disconnect the fan (17) power cable connector B1P1 from connector J2 on PCA-A3 (21).

g. Disengage the fan cable assembly from the two cable clamps (20) and remove the fan from the disc drive.

Reinstallation is a reversal of the removal procedure. Ensure that the fan is positioned with its power cable assembly in line with the cable clamps (20). Ensure also that the cable assembly connector disconnected in step e is firmly seated in its mating connector. Before returning the disc drive to service, check that the fan is operating correctly.

5-10. POWER SUPPLY ASSEMBLY PCA-A3

To remove PCA-A3 (21) from the disc drive, proceed as follows:

a. Perform the preparation for service procedure outlined in paragraph 5-2.

b. Ensure that the power cord is disconnected from the ~AC LINE connector on the rear panel of the disc drive.

c. Remove the top shroud (refer to paragraph 5-4) and the front panel (refer to paragraph 5-7).

d. Disconnect connector P1 on power cable assembly W1 (14) from connector J2 on PCA-A3 (21).

e. Disconnect the fan (17) cable assembly connector B1P1 from connector J2 on PCA-A3 (21).

f. Remove the T10 screw (22) and spacer (23) which secure PCA-A3 (21) to the mainframe assembly (35).

g. Remove the two T15 screws (24) which secure PCA-A3 (21) to the mainframe assembly (35).

h. Slide PCA-A3 (21) forward and out of the disc drive.

WARNING

Items 24 (screw) and 27 (power supply shield) must be installed before power is applied to the disc drive.

NOTE

If items 22 (screw) and 23 (spacer) are not reinstalled the disc drive may not pass RFI specifications.

Torque Specification: For item (22) screw torque to 10 in./lbs with T-10 bit and make sure the screw is seated. Replace item (22) each time it is removed from the disc drive.

Reinstallation is a reversal of the removal procedure. Check that the cable assembly connectors disconnected in steps d and e are properly seated in their mating connector. Ensure that the T10 screw (22) and spacer (23) removed in step f are properly installed. Ensure also that the two T15 screws (24) removed in step g are properly replaced. This attaching hardware is required to

properly ground the power supply to the mainframe assembly of the disc drive.

5-11. DISC DRIVE ASSEMBLY (HDA) PCA-A1

CAUTION

The defective Disc Drive Assembly (HDA) PCA-A1 being returned to the factory must be packaged and shipped in Hewlett-Packard shipping material or the warranty will be void.

To remove PCA-A1 (31, figure 6-1) from the disc drive, proceed as follows.

NOTE

Before removing PCA-A1,, refer to paragraph 4-64. This describes how to use a substitute PCA-A1 to verify the operation of PCA-A1 without removing it from the disc drive.

a. Perform the preparation for service procedure outlined in paragraph 5-2.

b. Ensure that the power cord is disconnected from the ~AC LINE connector on the rear panel of the disc drive.

c. Remove the top shroud (refer to paragraph 5-4) and the front panel (refer to paragraph 5-7).

d. Disconnect W2P2 (16) and W3P2 (15) ribbon cable assemblies from connecting J1 and J2, respectively, on PCA-A1 (31).

e. Disconnect connectors P3 and P4 on power cable assembly W1 (14) from connectors J3 and J4, respectively, on PCA-A1 (31).

f. Remove the four T15 screws (33) which secure PCA-A1 (31) to the mainframe assembly (35).

h. Carefully withdraw PCA-A1 (31) from the mainframe assembly (35).

Torque Specification: For item (33) screw torque to 15 in./lbs with T-15 bit.

Reinstallation is a reversal of the removal process. Ensure that the cable assembly connectors disconnected in steps d and e are firmly seated in their mating connectors.

5-12. TRAY REMOVAL AND REPLACEMENT

If it becomes necessary to replace the tray (32, figure 6-1) proceed as follows:

a. Perform the preparation for service procedure outlined in paragraph 5-2.

b. Ensure that the power cord is disconnected from the ~AC LINE connector on the rear panel of the disc drive.

c. Remove the top shroud (refer to paragraph 5-4) and the front panel (refer to paragraph 5-7).

d. Remove the Disc Drive Assembly (refer to paragraph 5-11).

e. Remove the four T15 screws (34) that hold the tray (32) to the disc drive assembly PCA-A1(31).

Torque Specification: for item (34) screw torque to 10 in./lbs with T-15 bit.

Reassembly is a reversal of the removal procedure.

Replaceable Parts 6

6-1. INTRODUCTION

This chapter provides listings of all field-replaceable parts and an illustrated parts breakdown for th disc drive. Replaceable parts ordering information for the disc drive is also provided in this section.

Replaceable parts for the disc drive are listed in order of disassembly in table 6-1 and illustrated in figure 6-1. In each listing, attaching parts are listed immediately after the item they attach. Items in the DESCRIPTION column are indented to indicate their relationship to the next higher assembly. In addition, the symbol "- - - X - - - " follows the last attaching part for the item. Identification of the items and the labels is as follows:

Major Assembly

*Replaceable Assembly

*Attaching Part for Replacement Assembly

**Subassembly or component Part

**Attaching Part for Subassembly or Replacement Part

The replaceable parts listings provide the following information for each part:

a. FIGURE AND INDEX NO. The figure and index number which indicates where the replaceable part is illustrated.

b. HP PART NO. The Hewlett-Packard number for the replaceable part.

c. DESCRIPTION. The description of the replaceable part.

Refer to table 6-2 for an explanation of the abbreviations used in the DESCRIPTION column.

d. MFG. CODE. The 5-digit code that denotes a typical manufacturer of a part. Refer to table 6-3 for a listing of manufacturers that corresponds to the codes.

e. MFG. PART NO. The manufacturer's part number for each replaceable part.

f. UNITS PER ASSEMBLY. The total quantity of each part used in the major assembly.

g. The MFG CODE and MFG PART NO. for common hardware are listed as 00000 and OBD (order by description), respectively, because these items can be purchased locally.

NOTE

TORX* hardware is used in the disc drive. This hardware requires the use of special drivers. In this manual, any reference to this type of hardware will be accompanied by the required driver size (for example, "T15").

6-2. ORDERING INFORMATION

To order replaceable parts for the disc drive, address the order to your local Hewlett-Packard Sales and Support Office. Headquarters Offices are listed at the back of this manual. Specify the following information for each order:

a. Model and full serial number.

b. Hewlett-Packard part number.

c. Complete description of each part as provided in the replaceable parts listing.

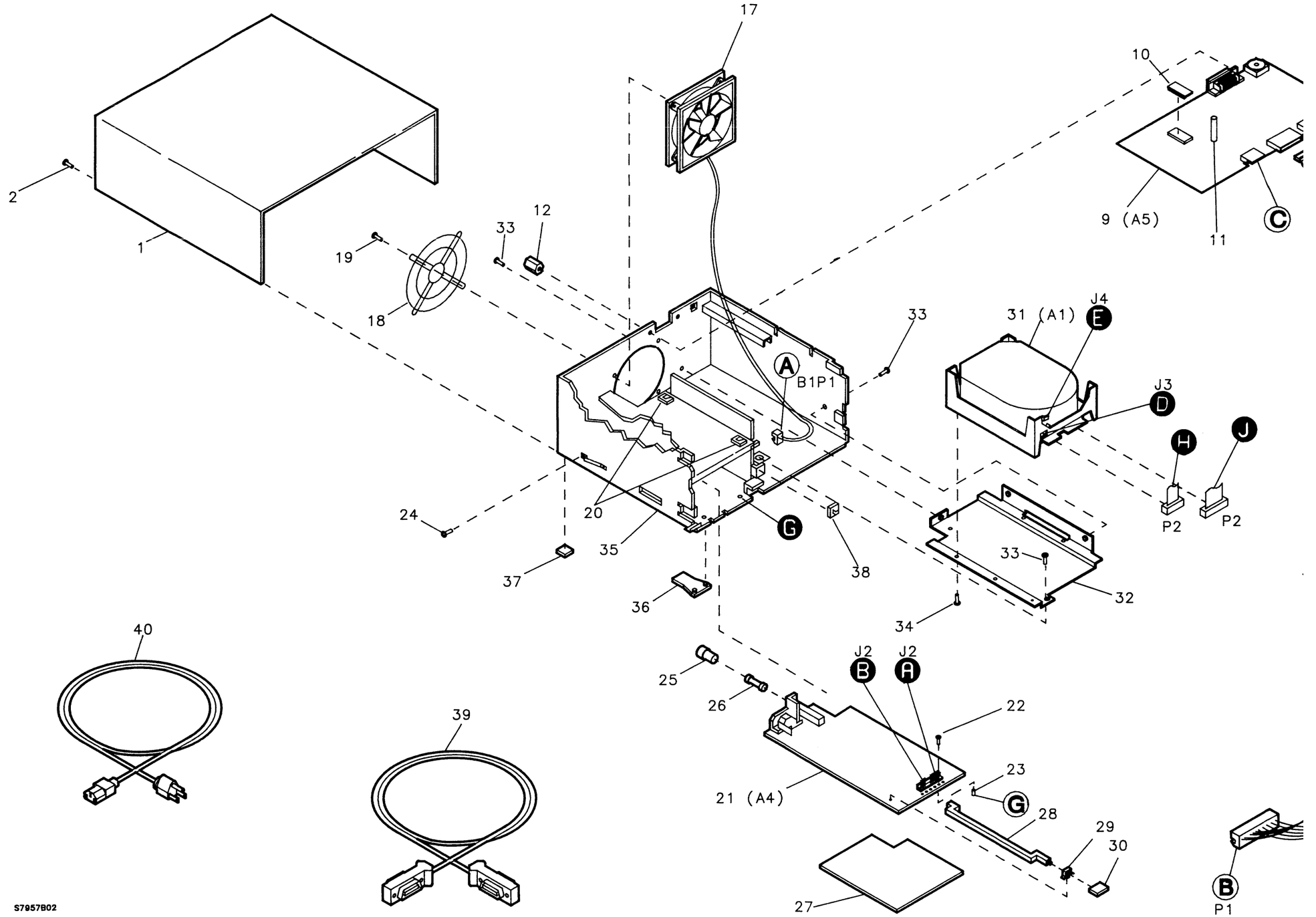
*TORX is a registered trademark of the Camcar Division of Textron, Inc.

Table 6-1. Disc Drive Replaceable Parts

FIG.& INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
6-1-	7957A	DISC DRIVE	28480	7957A	REF
	7958A	DISC DRIVE	28480	7958A	REF
1	07957-60015	* TOP SHROUD ASSEMBLY	28480	07957-60015	1
		(Attaching Parts)			
2	0515-0374	* SCREW,pnh,T10,M3.0 X 0.50, 10 mm long w/scw	00000	OBD	3
		- - - X - - -			
3	07957-60016	* FRONT PANEL ASSEMBLY, 7957A	28480	07957-60016	1
	07958-60016	* FRONT PANEL ASSEMBLY, 7958A	28480	07958-60016	1
		Index items 4, 5, and 6 are shipped with index item 3			
		(Attaching Parts)			
4	5001-3344	* FRONT PANEL SHIELD	28480	5001-3344	1
5	07941-60003	* LED Cable Assembly (W4)	28480	07941-60003	1
6	1400-0510	* CLAMP, cable	02768	8511-28-00-99	1
7	0515-0374	* SCREW,pnh,T10,M3.0 X 0.50, 10 mm long w/scw	00000	OBD	4
8	0624-0590	* SCREW, tapping, pnh, T25, 8-16, 0.312	00000	OBD	4
		- - - X - - -			
9	07957-60001	* HP-IB/ESDI CONTROLLER PCA ASSEMBLY	28480	07957-60001	1
		Item 10 will be shipped with exchange assembly 07957-69001			
		(Attaching Parts)			
10	07957-10161	* ESDI/HP-IB PROM KIT	28480	07957-10161	1
11	0380-1656	* SPACER, SNAP-IN, 0.625 in. long, 0.280 in. OD, Nylon	00000	OBD	1
12	0380-1918	* STANDOFF, hex, 6-32, 0.255 in. long	28480	0380-1918	2
13		Not Assigned			
		- - - X - - -			
14	07957-60008	* ESDI POWER CORD ASSEMBLY (W1)	28480	07957-60008	1
15	07957-60005	* ESDI CONTROL CABLE ASSEMBLY (W3)	28480	07957-60005	1
16	07957-60006	* ESDI DATA CABLE ASSEMBLY (W2)	28480	07957-60006	1
		- - - X - - -			
17	07941-60019	* FAN	28480	07941-60019	1
		(Attaching Parts)			
18	07941-00026	* GRILLE, fan	28480	07941-00026	1
19	0624-0661	* SCREW, tapping, pnh, T20, 10-14, 0.625 in. long	00000	OBD	4
20	1400-0510	* CLAMP, cable	02768	8511-28-00-99	2
		- - - X - - -			
21	09133-67120	* POWER SUPPLY ASSEMBLY	28480	09133-67120	1
		(Attaching Parts)			
22	0515-0665	* SCREW, machine, pnh, T10, M3.0 by 0.5, 14 mm long, w/scw	00000	OBD	1
23	5021-1534	* SPACER	28480	5021-1534	1
24	0515-0433	* SCREW, machine, pnh, T15, M4.0 by 0.7, 8 mm long, w/scw	00000	OBD	2
25	2110-0565	** CAP, fuse	28480	2110-0565	1

Table 6-1. Disc Drive Replaceable Parts (continued)

FIG.& INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
26	2110-0003	** FUSE, 3A, 250V, nontime delay	75915	2A250V3.0A	1
27	09144-45404	** SHIELD, power supply	28480	09144-45404	1
28	09133-40202	** SHAFT, switch	28480	09133-40202	1
29	0380-1655	** HOLDER, shaft	28480	0380-1655	1
30	5041-1203	** CAP	28480	5041-1203	1
		- - - X - - -			
31	07957-60021	* DISC DRIVE ASSEMBLY, 7957 (A1/FRA1)	28480	07957-60021	1
	07958-60021	* DISC DRIVE ASSEMBLY, 7958 (A1/FRA1)	28480	07958-60021	REF
		(Attaching Parts)			
32	5001-3341	* DISC TRAY	28480	5001-3341	1
33	0515-0433	* SCREW, machine, pnh, T15, M4.0 by 0.7, 8 mm long, w/scw	00000	OBD	4
34	2360-0464	* SCREW, pnh, T15, 0.375 in. long, 6-32 w/scw	00000	OBD	4
		- - - X - - -			
35	5061-3145	* MAINFRAME ASSEMBLY	28480	5061-3145	1
		(Attaching Parts)			
36	09121-48303	* FOOT, front	28480	09121-48303	1
37	0403-0427	* FOOT, rear	94959	SJ-5008	2
38	8160-0280	* CONTACT, finger	28480	8160-0280	1
		- - - X - - -			
39	8120-3445	* HP-IB CABLE ASSEMBLY, 1m, (Model 10833A)	28480	8120-3445	1
40	8120-0698	* POWER CORD ASSEMBLY, NEMA5A/CEE	28480	8120-0698	REF
	8120-1351	* POWER CORD ASSEMBLY, BS 1363/CEE	28480	8120-1351	REF
	8120-1369	* POWER CORD ASSEMBLY, ASC 112/CEE	28480	8120-1369	REF
	8120-1378	* POWER CORD ASSEMBLY, NEMA5A/CEE	28480	8120-1378	REF
	8120-1689	* POWER CORD ASSEMBLY, GMBH/CEE	28480	8120-1689	REF
	8120-1860	* POWER CORD ASSEMBLY, CEE/CEE	28480	8120-1860	REF
	8120-2104	* POWER CORD ASSEMBLY, SEV/CEE	28480	8120-2104	REF
	8120-2956	* POWER CORD ASSEMBLY, MDPP/CEE	28480	8120-2956	REF
	8120-4211	* POWER CORD ASSEMBLY, SABS/CEE	28480	8120-4211	REF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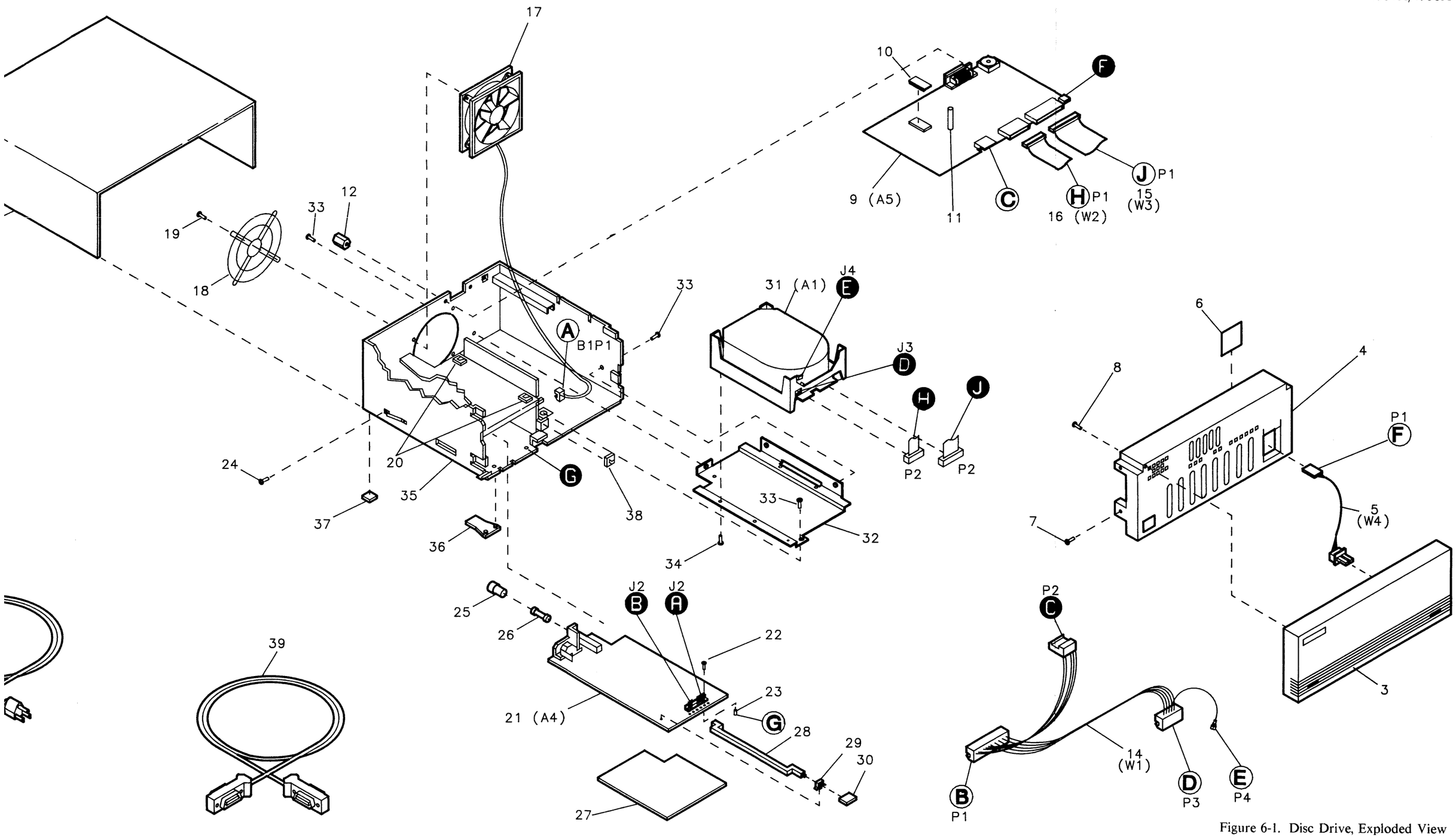

Figure 6-1. Disc Drive, Exploded View

Table 6-2. Abbreviations

A	= ampere(s)	incand	= incandescent	qty	= quantity
ac	= alternating current	incl	= include(s)		
		intl	= internal	rdh	= round head
AR	= as required	I/O	= input/output	rect	= rectifier
assy	= assembly			ref	= reference
		k	= kilo (10^3), kilohm	rf	= radio frequency
brkt	= bracket			rfi	= radio frequency interference
		kg	= kilogram		
c	= centi (10^{-2})			rh	= right hand
C	= Celsius, centigrade	lb	= pound	rpm	= revolutions per minute
		LED	= light-emitting diode		
cer	= ceramic			rwv	= reverse working voltage
cm	= centimetre	lh	= left hand		
comp	= composition				
conn	= connector	M	= mega (10^6), megohm	sb	= slow blow
				SCR	= semiconductor-controlled rectifier
d	= deci (10^{-1})	m	= milli (10^{-3})		
dc	= direct current	mach	= machine		
deg	= degree(s)	mb	= medium blow	scw	= square cone washer
dia	= diameter	met oxd	= metal oxide		
dpdt	= double-pole, double-throw	mfr	= manufacturer	Se	= selenium
		misc	= miscellaneous	Si	= silicon
dpst	= double-pole, single throw	mm	= millimetre	slftpg	= self-tapping
		mtg	= mounting	spdt	= single-pole, double throw
		My	= Mylar		
elctlt	= electrolytic			spst	= single pole, single throw
encap	= encapsulated	n	= nano (10^{-9})		
ext	= external	n.c.	= normally closed	sst	= stainless steel
		no.	= number	stl	= steel
F	= Fahrenheit, farad	NSR	= not separately replaceable	sw	= switch
				T	= TORX(R) screw
fb	= fast blow	ntd	= no time delay	Ta	= tantalum
fh	= flat head			tgl	= toggle
fig.	= figure	OBD	= order by description	thd	= thread
filh	= fillister head			Ti	= titanium
flm	= film	OD	= outside diameter	tol	= tolerance
fw	= full wave				
fxd	= fixed	ovh	= oval head		
		oxd	= oxide	U (μ)	= micro (10^{-6})
G	= giga (10^9)				
Ge	= germanium	p	= pico (10^{-12})	V	= volt(s)
		PCA	= printed-circuit assembly	var	= variable
H	= Henry, Henries			Vdcw	= direct current working volts
hd	= head	phh	= phillips head		
hex	= hexagon, hexagonal	pnh	= pan head		
		P/O	= part of	W	= watt(s)
hlcl	= helical	pot	= potentiometer	w/	= with
Hz	= Hertz	pozi	= Pozidriv	WIV	= inverse working volts
ID	= inside diameter			ww	= wire-wound
in.	= inch, inches				

TORX(R) is a registered trademark of the Camcar Division of Textron, Inc. (abbrev-8/83)

Table 6-3. Code List of Manufacturers

CODE NO.	MANUFACTURER	ADDRESS
02768	Illinois Tool Works, Inc	Chicago, IL
28480	Hewlett-Packard Co.	Palo Alto, CA
75915	Tracor Littelfuse Inc.	Des Plaines, IL
94959	3M Co., Adhesives, Coating, Sealers Division	St. Paul, Mn

HEADQUARTERS OFFICES

If there is no sales office in your area,
contact one of these headquarters offices.

FAR EAST
Hewlett-Packard Asia Headquarters
26 Harbor Rd.
Wanchai, Hong Kong
Tel: 5-833-0833
Telex: 66678 HEWPA HX
Cable: HEWPACK HONG KONG

CANADA
Hewlett-Packard (Canada) Ltd.
6877 Goreway Drive
Mississauga, Ontario L4V 1M8
Tel: (416) 678-9430
Telex: 610-492-4246

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Hewlett-Packard S.A.
150 Route du Nant-d'Avril
CH-1217 Meyrin 2, Switzerland
Tel: (011)-41 22 838-111
Telex: 27835 hpse
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(Offices in the World Trade Center)

JAPAN
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Suginami-Ku, Tokyo 168
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Hewlett-Packard Co.
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Tel: (301) 258-2000

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7957A AND 7958A DISC DRIVES HARDWARE SUPPORT MANUAL

07957-90903 SEPTEMBER 1987

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Manual Part Number: 07957-90903
Printed in U.S.A., SEPTEMBER 1987
Edition 2
E0987

HEWLETT PACKARD