HP 27110A

HP-IB INTERFACE
(HP-IB)

Technical Reference Manual

Card Assembly: 27110-60001
Date Code: D-2321

HEWLETT PACKARD

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PRINTING HISTORY

The Printing History below identifies the Edition of this Manual and any Updates that are included. Periodically, update packages are distributed which contain replacement pages to be merged into the manual, including an updated copy of this Printing History page. Also, the update may contain write-in instructions.

Each reprinting of this manual will incorporate all past updates; however, no new information will be added. Thus, the reprinted copy will be identical in content to prior printings of the same edition with its user-inserted update information. New editions of this manual *will* contain new information, as *well* as updates.

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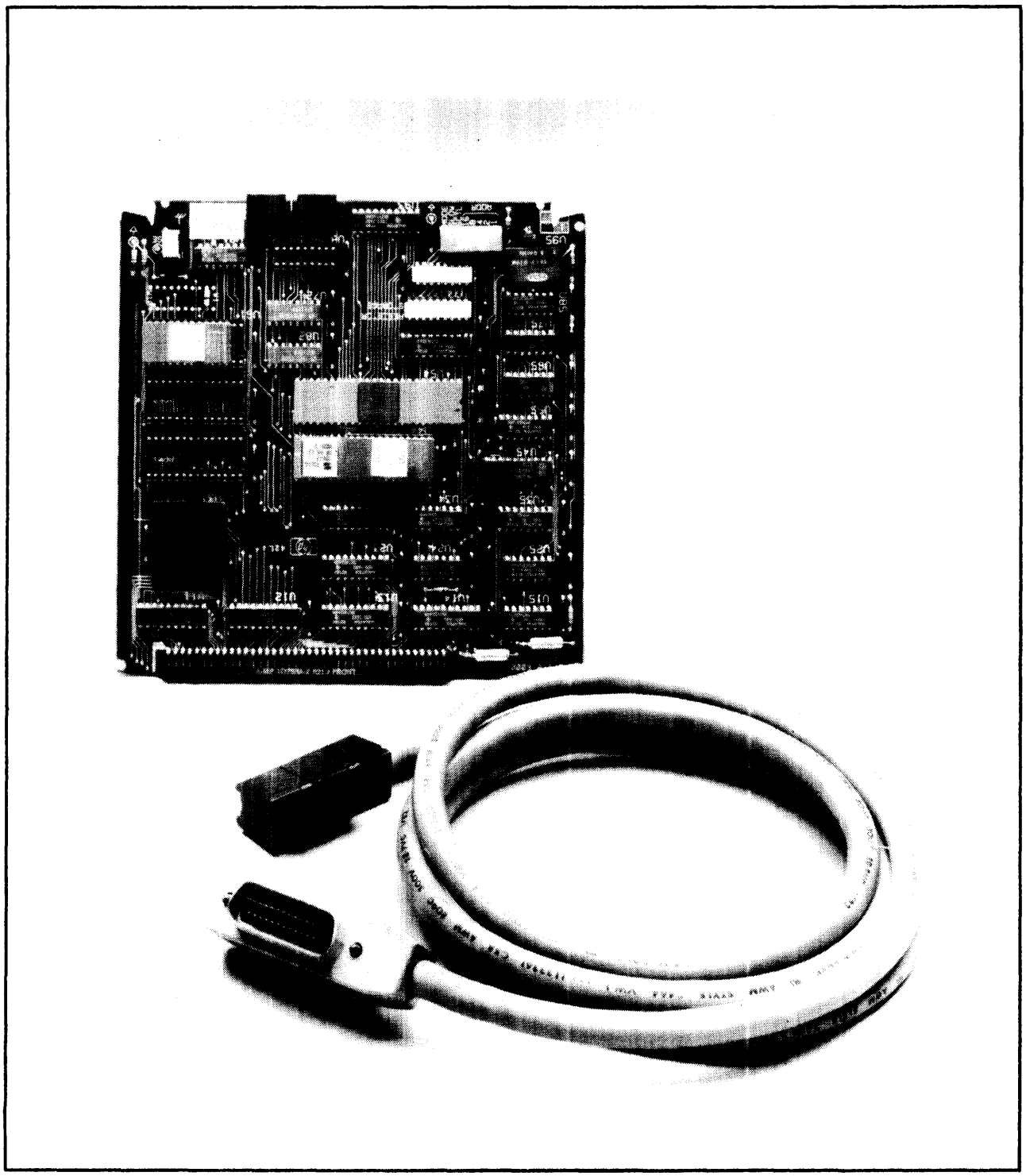


Figure 1-1. HP 27110A HP-IB Interface

GENERAL INFORMATION

SECTION I

This manual provides general information, installation, theory of operation, maintenance instructions, replaceable parts information, and servicing diagrams for the Hewlett-Packard HP 27110A Hewlett-Packard Interface Bus (HP-IB) Interface Card. This section contains general information concerning the HP-IB card, and includes a description and specifications.

PHYSICAL DESCRIPTION

The HP 27110A Hewlett-Packard Interface Bus (HP-IB) Interface Card is shown in figure 1-1 and consists of a printed-circuit assembly, an interface cable, and an installation manual.

FUNCTIONAL DESCRIPTION

The Hewlett-Packard Interface Bus (HP-IB) is Hewlett-Packard's implementation of the IEEE Standard 488-1978 and Supplement 488-1978A-1980.

The HP-IB card provides an interface between a host computer and up to 14 HP-IB-compatible peripheral devices such as disc drives, tape drives, printers, printer/plotters, etc.

Figure 1-2 shows a Hewlett-Packard computer system using CHANNEL I/O and the HP-IB interface bus. (CHANNEL I/O is a Hewlett-Packard standard defining the physical and electrical characteristics for an I/O system consisting of an I/O channel adapter, an I/O channel, and I/O cards. The HP-IB card is one of the I/O cards.)

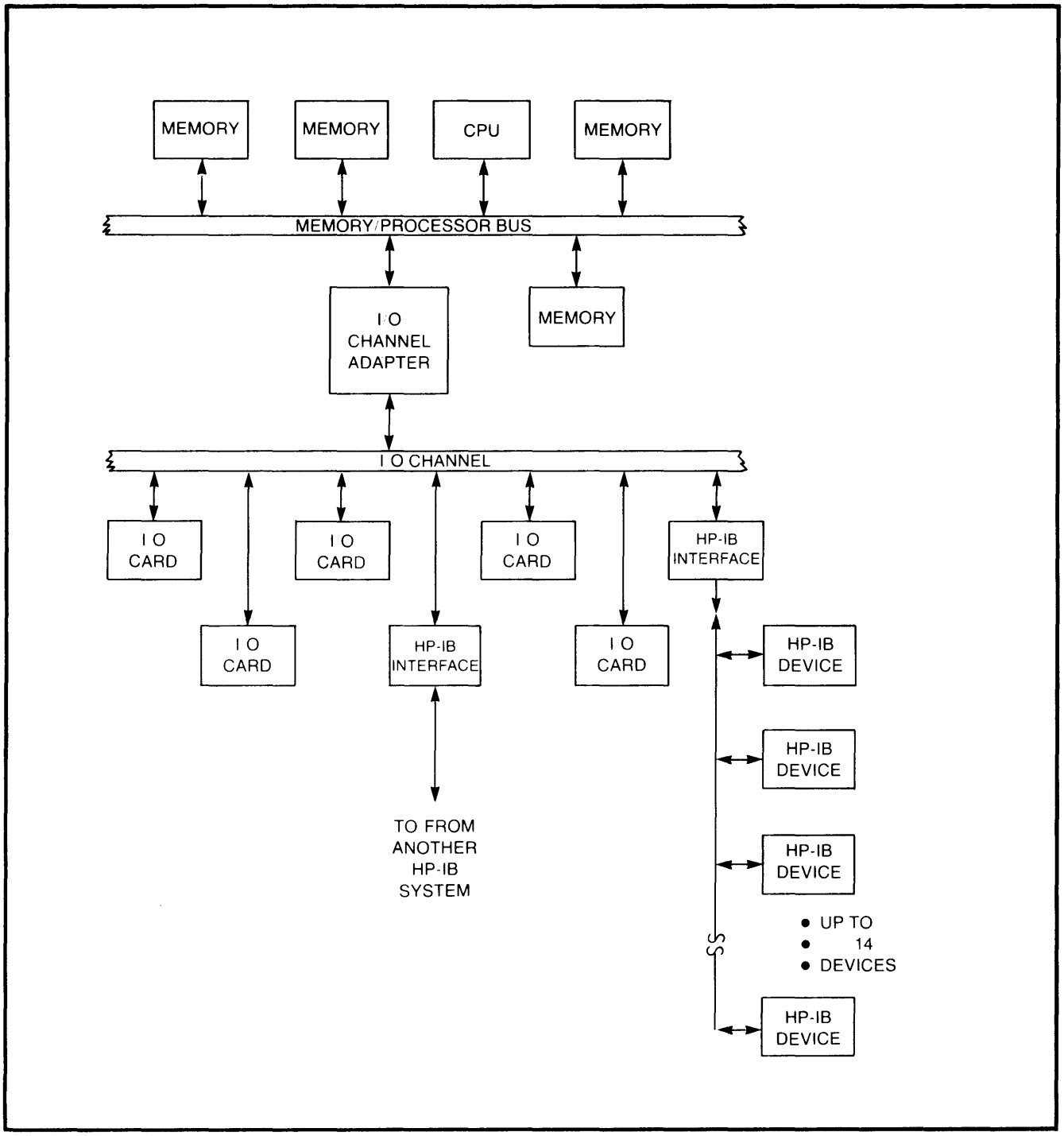


Figure 1-2. HP-IB Interface Card in a Hewlett-Packard Computer System

Note that the computer system CPU and memory communicate directly along a Memory/Processor Bus (MPB). I/O data to/from peripheral devices reaches the CPU/memory through the I/O channel, the I/O channel adapter, and an I/O card such as the HP-IB card. The I/O data is received from and transmitted to peripheral devices by the I/O card, which converts device-specific data to a format compatible with the I/O channel, and thus the computer. The I/O channel adapter (see figure 1-2) controls the flow of data traffic between the I/O channel and the memory/processor bus.

The HP-IB card can interface to up to 14 standard HP-IB peripheral devices (such as instruments), or up to seven high-speed HP-IB peripheral devices (such as disc drives). The HP-IB card is an intelligent interface card utilizing a Z8 microprocessor, and has the capability of relieving the host CPU of a large amount of overhead.

EQUIPMENT SUPPLIED

The standard HP 27110A HP-IB Interface Card consists of the following items (see figure 1-1):

HP-IB interface card, part number 27110-60001

Two-meter HP-IB cable, part number 8120-4010

HP 27110A Installation Manual, part number 27110-90001

IDENTIFICATION

The Product

Up to five digits and a letter (27110A in this case) are used to identify Hewlett-Packard products. The five digits identify the product; the letter indicates the revision level of the product.

Interface Card

The interface card supplied with the HP 27110A product is identified by a part number marked on the card. In addition to the part number, the card is further identified by a letter and a four-digit date code (e.g., D-2230). This designation is placed below the part number. The letter identifies the version of the etched circuit on the card. The date code (the four digits following the letter) identifies the electrical characteristics of the card with components mounted. Thus, the complete part number on the HP-IB card could be:

27110-60001
D-2321

If the date code stamped on the card does not agree with the date code on the title page of this manual, there are differences between your card and the card described herein. These differences are described in manual supplements available at the nearest Hewlett-Packard Sales and Service Office (a list of Hewlett-Packard Sales and Service Offices is contained at the back of this manual).

Manuals

The Installation Manual (part number 27110-90001, supplied with the product) and this manual (HP 27110A Technical Reference Manual, part number 27132-90002) are identified by name and part number. (Note that this manual is part of the HP 27132A Technical Reference Package.) The name, part number, and publication date are printed on the title page of each manual. If the manual is revised, the publication date is changed. In this manual, the "Printing History" page (page ii) records the reprint dates. Reprint dates for the Installation Manual are printed on the title page.

SPECIFICATIONS

Table 1-1 lists the specifications of the HP-IB.

Table 1-1. Specifications

FEATURES

HP-IB Bus Signal Lines:

DI01	Data Input/Output 1
DI02	.
DI03	.
DI04	.
DI05	.
DI06	.
DI07	.
DI08	Data Input/Output 8
DAV	Data Valid
NRFD	Not Ready For Data
NDAC	Not Data Accepted
IFC	Interface Clear
ATN	Attention
SRQ	Service Request
REN	Remote Enable
EOI	End or Identify

Logic Levels: High > 2.4V
Low < 0.5V

All signals are low true

Line Termination:

Each of the 16 HP-IB signal lines is terminated with a 2.3K ohm resistor to Vcc and a 4.7K ohm resistor to common without the optional load resistors.

Line Drivers:

Each of the 16 HP-IB signal lines is driven with a circuit having the following typical characteristics:

Type: Tri-state, open collector
Output Voltage, Low State: < 0.5V, 48 mA
Output Voltage, High State: < 2.5V, -5.2 mA

Table 1-1. Specifications (Continued)

Line Receivers:

Each of the 16 HP-IB signal lines is received with a circuit having the following characteristics:

Type:	Schmitt Trigger
Threshold, Positive Transition:	1.6V
Threshold, Negative Transition:	0.9V for data lines 1.0V for control lines
Input Current, Low State:	-1.3 mA minimum to -3.2 mA maximum @ 0.5V
Input Current, High State:	0.7 mA minimum to 2.5 mA maximum between 5V and 5.5V

Maximum Transfer Rates:

Standard Speed:	500K bytes/second
High Speed:	980K bytes/second

(Dependent on host computer and software)

Maximum Cable Length:

Standard Operation:	2 meters per device connected with a 20-meter maximum length and a settling time of greater than 500 ns.
High-Speed Operation:	15 meters total maximum length, and a settling time of less than 350 ns. See Section 2 for more information on high-speed operation.

Operating Temperature: 0 to 55 degrees Celsius

Address: 30 decimal when Controller-In-Charge (CIC), and set by switches or host computer when not CIC.

Table 1-1. Specifications (Continued)

PHYSICAL CHARACTERISTICS

Size:	172.7 mm long by 172 mm wide (6.80 by 6.75 inches)
Weight:	234 grams (8.2 ounces)
I/O Channel Interconnects:	80-pin connector, J1
Device Interconnects:	26-pin connector, J2

POWER REQUIREMENTS

Voltage	Current	Power Dissipation
+5V	1.8 A	9.0 watts
+12V	35 mA	0.42 watts

HP-IB CAPABILITIES

The Hewlett-Packard Interface Bus provides the capability of connecting from one to 14 compatible peripheral devices to a host computer via one interface card. Data is transferred over the HP-IB bidirectionally in 8-bit bytes. Data can be transferred from a device to the computer and to other devices simultaneously, or from the computer to one or more devices simultaneously, or from one device to other devices under the control of the computer.

Some HP-IB features must be used while other features are optional. For example, all devices must be capable of being addressed, but they need not be capable of being operated by remote control. An HP-IB system may have some devices operating under remote control, while other devices in the same system are operating under local (their own front and rear panel controls) control.

The same pins of all HP-IB connectors of all devices are connected in parallel making a parallel communication network. This permits information to flow in any direction on the bus and allows any device to talk directly with another device without going through a central control unit.

HP-IB SUPPORTED FUNCTIONS

The interface card is designed to support the following HP-IB Interface Functions as defined by the IEEE Standard 488-1978. (The HP-IB is Hewlett-Packard's implementation of the IEEE Standard 488-1978.) These functions are fully supported by the HP 27110A unless noted otherwise.

Controller Functions:

C1 -- System Controller

C2 -- Send Interface Clear and Take Charge

C3 -- Send Remote Enable

C4 -- Respond to Service Request

C5 -- Send Interface Messages, Receive Control, Pass Control, Pass Control to Self, Parallel Poll, Take Control Synchronously

Controlled Device Functions:

SR1 -- Service Request

RL2 -- Remote Local

PP1 -- Parallel Poll

DC1 -- Device Clear

DT1 -- Device Trigger

The following utility functions are provided to support the above listed functions:

SH1 -- Source Handshake

AH1 -- Acceptor Handshake

T1 -- Basic Talker, Serial Poll, Talk Only

TE1 -- Basic Extended Talker, Serial Poll, Talk Only, Unaddress if My Listener Address and My Secondary Address (requires host software support)

L1 -- Basic Listener, Listen Only Mode

LE1 -- Basic Extended Listener, Listener Only Mode, Unaddress if My Secondary Address and Talker Primary Addressed State (requires host software support)

ADDRESSING-TALKING-LISTENING-HANDSHAKING

An addressing technique is used to determine which device is to "talk" and which devices are to "listen". Data is sent from one device to another device in a bit-parallel, byte-serial format using an interlocked "Handshake" technique. This technique assures that the sender does not remove data before the receiver has finished using the data. It also ensures that data is not lost when devices having inherently different speeds communicate on the same bus.

FUNCTIONS OF DEVICES ON THE HP-IB

Devices connected to the bus must be addressed by the Controller before they can function in one or more of the following ways:

TALKER - Any device that is capable of sending or transmitting information on the bus. There can be only one talker at a time on the bus.

LISTENER - Any device that is capable of receiving or accepting information on the bus is a listener. There may be up to 15 listeners at the same time on the bus.

TALKER-LISTENER - A device that has the capability of both sending and receiving information on the bus as defined previously is both a talker and a listener. For example, a counter is a talker when sending data and a listener when it is being programmed.

CONTROLLER - Any device that has been programmed to have the responsibility of managing the flow of information between devices connected to the bus is a controller. It is capable of addressing one of the devices as a talker and one or more of the others as listeners. The HP-IB permits a system to have more than one controller, but only one controller may be active at a time. (The Controller-in-Charge may be the System Controller.)

SYSTEM CONTROLLER - The system designer must designate one device as the System Controller at the time the system is configured. The System Controller can assert IFC and REN. The System Controller becomes the Controller-In-Charge by asserting IFC.

HP-IB BUS LINES

The HP-IB bus structure consisting of 16 signal lines is shown in figure 1-3. There are eight additional bus conductors, as follows: one ground, one cable shield, and six twisted-pair commons for six of the signal lines.

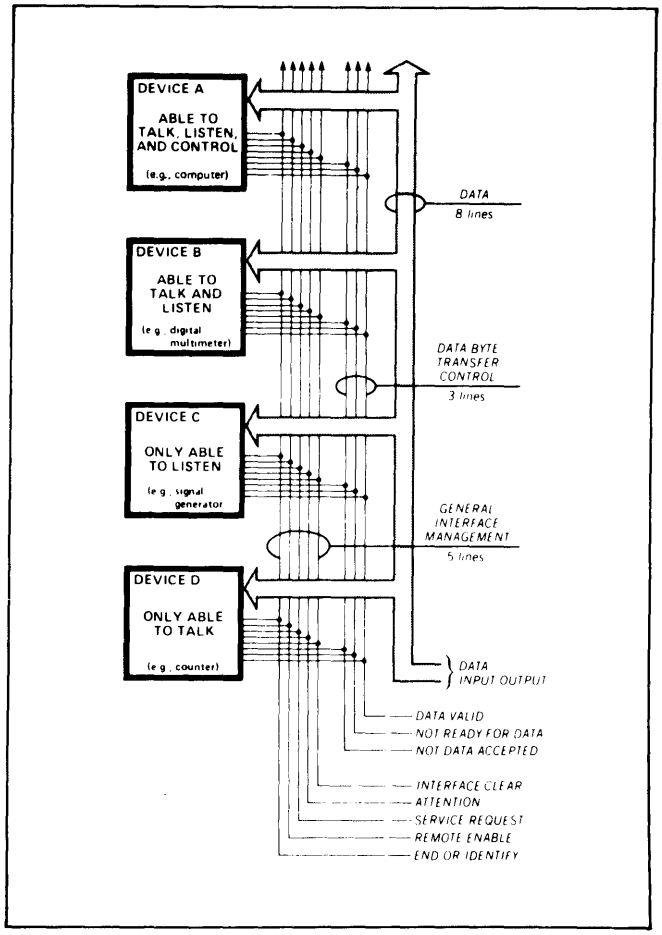


Figure 1-3. HP-IB Bus Structure

All 16 signal lines have been given names and mnemonic acronyms that describe the message being carried on each line. There are three types of lines: Data (8), Transfer (handshake) (3), and Control (management) (5).

NOTE

All devices connected to the bus, including the controller, must conform to the descriptions presented in the following paragraphs.

CONTROL LINES

The five control lines are used to manage the flow of information over the data and transfer lines. They communicate control and status information between the active controller and the devices connected to the bus. All devices must use ATN and IFC. A device may or may not use REN, SRQ, and EOI.

ATN (Attention) is driven by the active controller to place the bus in either the COMMAND (low) or DATA (high) mode. All other devices must monitor ATN at all times.

When the controller sets ATN to its low state, the bus is in the Command Mode. The primary purpose of the Command Mode is to permit the controller to send commands or address those devices that are to communicate when the bus is placed in the Data Mode. Also, the controller may send "universal commands" while the bus is in the Command Mode.

When the controller sets ATN to its high state, the bus is in the Data Mode. The device that was addressed to talk and those that were addressed to listen will now communicate on the Data Lines.

ATN may be set low or high at any time by a controller, however, it is usually at the end of a transfer (handshake) cycle so that data is not lost. Timing of the transfer lines with respect to ATN is described in the paragraph "Transfer Lines".

IFC (Interface Clear) is used by the system controller to initialize the bus. Only the System Controller can drive IFC and it must be monitored by all other devices on the bus. When the System Controller sets IFC low, the following takes place: all talkers and listeners are stopped and unaddressed, serial poll mode is disabled, and control is returned to the HP-IB System Controller. When IFC is high it has no effect on the bus operation. The System Controller may set IFC low at any time.

REN (Remote Enable) is used by the System Controller to inform devices that are capable of remote operation that they are to operate under Remote Control. Such devices monitor REN at all times. Devices that are not capable of remote operation terminate REN in a resistive load. Only the System Controller may assert REN and may change its state at any time.

SRQ (Service Request) is driven to its low state by a device to indicate that it wants the attention of the System Controller. SRQ may be set low by a device at any time except when IFC is in the low state. Only the Controller-In-Charge senses SRQ. Some devices do not use SRQ, but all must terminate it in a resistive load.

EOI (End or Identify) may be used to indicate the end of a device's character string. When the bus is in the Data Mode (ATN is high), the addressed talker may indicate the end of its data by setting EOI low at the same time it places the last byte on the Data Lines. When ATN and EOI are both low, the bus is in the PPOLL mode.

DATA LINES (DI01-DI08)

The Data Lines are used to communicate all data, including input, output, program codes, addresses, and control and status information between devices connected to the bus. This data is passed character (byte) at a time (i.e., byte serial and bit parallel) under control of the Transfer Lines.

TRANSFER LINES

Three Transfer (handshake) Lines are used to execute the transfer of each byte of information on the data lines. All devices use these lines and employ an interlocked handshake technique to pass information. This allows asynchronous data transfer without timing restrictions being placed on any device connected to the bus. The transfer of each byte is accomplished at the speed of the slowest device. The three transfer lines are: NRFD, NDAC, and DAV.

NRFD (Not Ready For Data) is the transfer (handshake) line that indicates all listeners are ready to accept information on the data lines. NRFD is driven by all the listeners (all devices when ATN is low, and only by those devices addressed to listen when ATN is high). It is sensed by talkers as follows: the controller when ATN is low, and the device addressed to talk when ATN is high.

When NRFD is high, all listeners are unconditionally ready for data. The talker may, at its own time, put a byte of information on the data lines and set DAV low. When NRFD is low, one or more listeners are not ready for data.

When the controller sets ATN true (low), all devices must prepare to receive interface messages within 200 nsec.

A listener must not set NRFD low until it senses DAV is low. It may do so before or at the same time that it sets NDAC high. It must not return NRFD to its high state until it senses DAV is high and may do so after, or at the same time that it sets NDAC low.

NDAC (Not Data Accepted) is the transfer line that indicates the acceptance of data on the data lines. NDAC is driven by all listeners. That is, all devices when ATN is low, and only those devices addressed to listen when ATN is high. It is sensed by the controller when ATN is low and by the device addressed to talk when ATN is high.

When NDAC is high, all listeners have unconditionally accepted the byte of information that is on the date lines and no longer need it. The talker may, at its own time, set DAV high, remove the byte of information, and continue. When NDAC is low, one or more listeners have not accepted the information on the data lines.

When the controller sets ATN high, the devices that have not been addressed to listen will not drive NDAC.

A listener must not set NDAC low until it senses DAV is high. It may do so before or at the same time that it sets NRFD high. It must not return NDAC high until it senses DAV is low and it may do so after or at the same time that it sets NRFD low.

DAV (Data Valid) is the transfer line that indicates the validity of information on the data lines. DAV is driven by the talkers: the controller when ATN is low and the device addressed to talk when ATN is high. DAV is sensed by all devices if ATN is low, and by those devices addressed to listen when ATN is high.

When DAV is low, the states of data lines DI01 through DI08 are unconditionally valid and may be accepted by all listeners at their own time. DAV can only be driven low if NRFD and IFC are high. When DAV is high, the information on the data lines is not valid. DAV cannot be set high unless NDAC is high and NRFD is low.

The talker has the responsibility of allowing enough time for cable rise time and ringing. It does this with DAV. After placing the bus in the Address Mode (setting ATN low), the controller must wait before setting DAV low. Of course DAV must not be asserted unless NRFD is high. In either the Address or Data Mode, a talker designed with open-collector circuits must not set DAV low for at least two microseconds after placing valid data at its output connector. Those designed with tri-state logic must wait at least 500 nsec.

The conditions described in the preceding paragraphs are summarized in tables 1-2 and 1-3.

DATA TRANSFER

The transfer of data on the bus is asynchronous and therefore places no restrictions on the data rates of devices connected to the bus. The timing and levels required to transfer a byte of data on the data lines are shown in figure 1-4. The transfer is under the control of the three lines DAV, NRFD, and NDAC. The talker (sender of data) drives the Data Lines and DAV (Data Valid), and the listeners (acceptors of data) drive both NRFD (Not Ready For Data) and NDAC (Not Data Accepted).

The transfer of a byte of data is initiated by all listeners signifying they are ready for data by setting NRFD high. When the talker recognizes NRFD is high and has placed valid data on the data lines, it sets DAV low. When the listeners sense that DAV is low and have finished using the data, they set NDAC high. Note that the assertion or active state of both NRFD and NDAC is low. Since all devices on the bus have their corresponding lines connected together (e.g., NRFD), all listeners must be in a high state before that line goes high. This wired-AND condition allows a talker to recognize when the slowest listener has accepted a byte of data and is ready for the next byte.

Figure 1-4 shows the timing of the transition to the assertive state of these lines. A listener may set NRFD low as soon as it recognizes that DAV has been set low and must do so before or at the same time it sets NDAC high. The talker may return DAV to its high state after it detects that NDAC is high. A listener may set NDAC low as soon as it recognizes that DAV is high and must do so before or at the same time it sets NRFD to its high state.

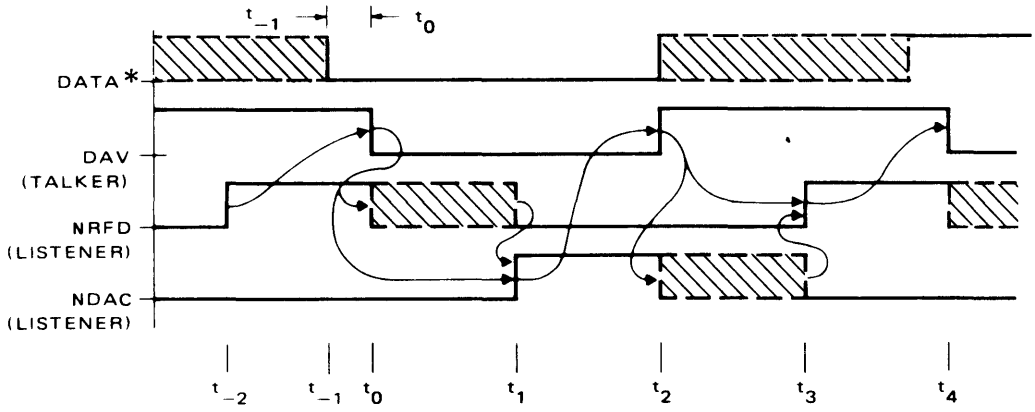
Table 1-2. Relationship Between ATN and Transfer (Handshake) Lines (NRFD, NDAC, and DAV)

MODE	ATN	NFRD		NDAC		DAV	
		LOW	HIGH	LOW	HIGH	LOW	HIGH
COMMAND	LOW	One or more units not ready for data	All units ready for data	One or more units have not accepted data	All units have accepted data	Controller has valid data on DIO lines	Controllers data is not valid
		1. Driven by all units except controller 2. Sensed by controller 3. All units set NFRD and NDAC to valid state within 200 nsec after ATN goes low				1. Driven by controller 2. Sensed by listeners 3. See DAV above for timing	
DATA	HIGH	One or more listeners not ready for data	All addressed listeners ready for data	One or more listeners have not accepted data	All addressed listeners have accepted data	The addressed talker has valid data on lines	The addressed talker data is not valid
		1. Driven by all units address to listen 2. Sensed by the unit addressed to talk 3. All units not addressed will not drive 4. All addressed listeners set both NRFD and NDAC to valid within 200 nsec after ATN goes high				1. Driven by the devices addressed to TALK 2. Sensed by all devices addressed to LISTEN 3. See DAV above for timing	
		NOTE Valid means either both asserted or both not asserted					

Table 1-3. Summary of Bus Timing

IFC INTERFACE CLEAR	The System Controller must set IFC low for at least 100 usec to clear the bus
TRANSFER LINES WITH RESPECT TO ATN	When sending an Address or a Universal Command the controller may set DAV low only after sensing that NRFD is high, and ATN has been low for a minimum time. When a controller changes ATN from its high to the low state, all non-listeners assert NRFD and NDAC in less than 200 nsec.
TRANSFER LINES WITH RESPECT TO THE DATA	After changing the information on one or more Data Lines, the talker (the Controller when ATN is low, or the device addressed to talk when ATN is high) must wait before setting DAV low. It waits 2 usec if designed with open-collector circuits, 500 nsec if designed with tri-state integrated circuits at standard speed, and 350 nsec if operated at high speed.

SEQUENTIAL REQUIREMENTS OF THE THREE WIRE TRANSFER



EVENTS

t_{-2} : Listener becomes ready to accept data.

t_{-1} : Talker has put data on the lines.

t_0 : Indicates data is valid.

t_1 : Listener has accepted the data and no longer requires it held valid.

t_2 : Talker indicates the data is no longer valid and may change it.

t_3 : Listener indicates it is ready for new data.

t_4 : A new cycle begins (equivalent to t_0).

t_{-1} to t_0 : Time that data is put on lines before DAV is set low.

* A composite of the DIO1 through DIO7 lines for illustrative purposes. The curved lines indicate transfer (handshake) signal sequence.

Figure 1-4. Transfer Timing

NRFD

When the card is Controller-In-Charge and PPOLL is disabled and the card is neither sending or receiving data, Not Ready For Data (NRFD) will be asserted. The significance of this is: when the controller addresses one device to talk and another device to listen, the transfer will be blocked by this card's assertion of NRFD.

PPOLL and ATN

The assertion of ATN during idle time is a function of whether PPOLL is to be asserted.

Normally, the ATN signal is not asserted except in the following cases:

1. A PPOLL interrupt has been enabled.
2. The last HP-IB message sent by the card was an interface message.
3. The assert ATN transaction is invoked.
4. During the execution of the "read PPOLL response" transaction.

The ATN signal will be deasserted in the following cases:

1. PPOLL interrupts are disabled and neither of conditions 2 or 3 above are true.
2. Last HP-IB message sent by the card was a data message.
3. The deassert ATN transaction is invoked.
4. The card is reset (PPON, DCL, or IFC).
5. The card is not System Controller and an IFC message is received.
6. The card sends a TCT (Take Control) message.

DEFAULT AND POWER ON CONFIGURATIONS

Offline/Online

Following a power on, the HP-IB card will be offline from the HP-IB bus. This means that it will not interact with the HP-IB bus in any way. The card will go online upon receipt of a "Go Online" transactions. Once the card is online it will not go offline unless another power reset is done or upon receipt of a "Go Offline" transaction.

The control of online timing allows you to configure the card for activities if different from the default - e.g., PPOLL sense - before the critical action of going online.

REN and IFC

If the card comes online as System Controller, the REN (Remote Enable) signal will be deasserted by the card until explicitly controlled by the "Send Interface Clear" transaction; that is, the IFC signal is not automatically asserted when the card goes online.

The IFC signal is required before a card configured as the System Controller can assume the role of Controller-In-Charge (this may be accomplished offline).

INSTALLATION

SECTION II

This section provides information on installing and checking the operation of the HP-IB card.

COMPUTATION OF CURRENT REQUIREMENTS

The HP-IB circuit card obtains its operating voltages from the computer power supply through the I/O channel. Before installing the card, it is necessary to determine whether the added current will overload the power supply. The current requirements of the HP-IB card are listed in the power requirements entry of table 1-1. Current requirements for all other I/O cards can be found in the appropriate Service Manuals.

FIRMWARE (ROM/EPROM) INSTALLATION

CAUTION

SOME OF THE COMPONENTS USED IN THIS PRODUCT ARE SUSCEPTIBLE TO DAMAGE BY STATIC DISCHARGE. REFER TO THE SAFETY CONSIDERATIONS INFORMATION AT THE FRONT OF THIS MANUAL BEFORE REMOVING OR REPLACING THESE COMPONENTS.

The firmware ROM is installed in a socket provided on the HP-IB card as shown in figure 2-1. Ensure that it is installed properly and that it has not been damaged or loosened from its socket during shipping.

Additionally, when installing or removing the ROM, guard against bending or breaking the pins on the component. These pins also can become folded between the component and its socket, which would result in intermittent operation of the HP-IB. In most cases, a bent or damaged pin can be straightened with careful use of needle-nose pliers.

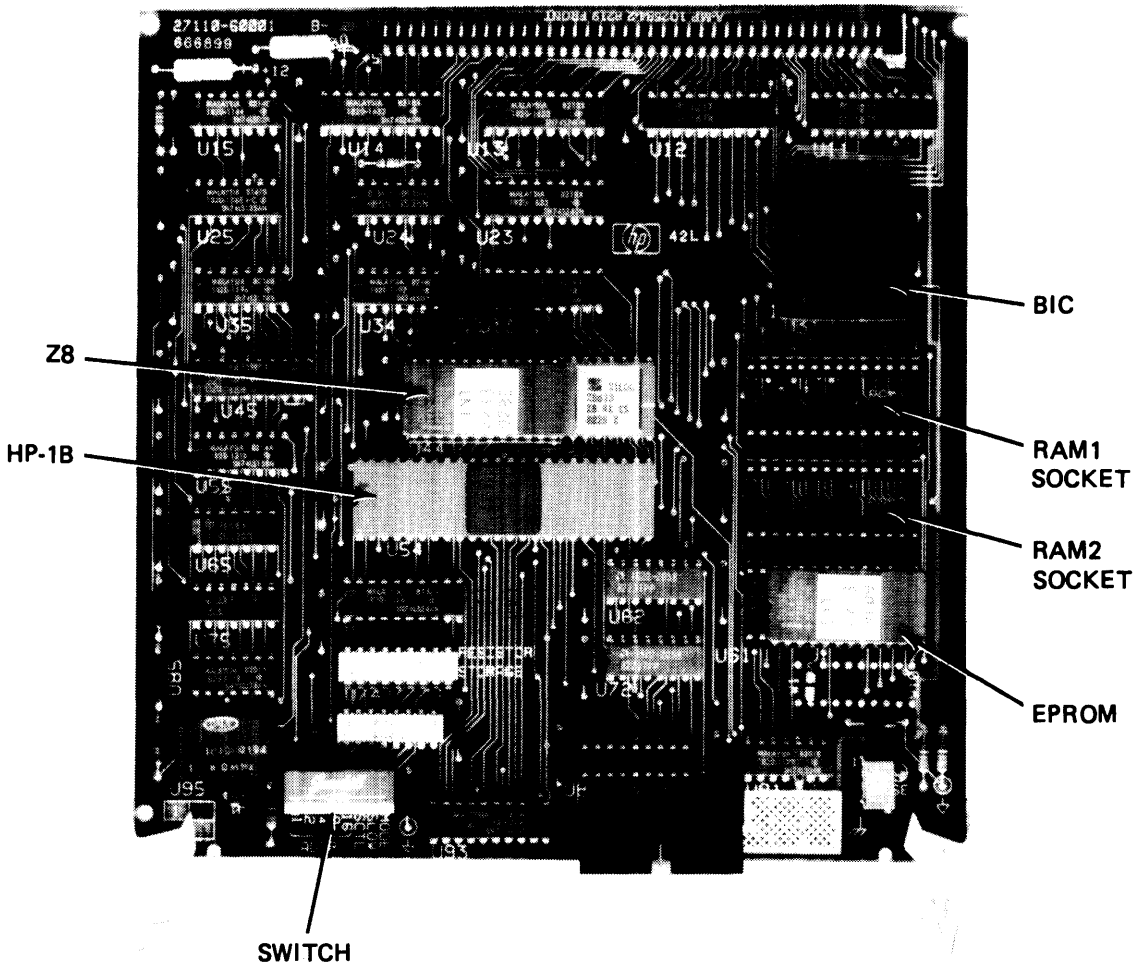


Figure 2-1. Major Component Locations

CONFIGURATION SWITCH DEFINITIONS

An eight-switch assembly is used to configure the HP-IB. The function of each switch is listed in table 2-1 and the location of the switch assembly is shown in figure 2-1. Note that the switches are ON in the up position and OFF in the down position.

Table 2-1. Configuration Switch Definitions

SWITCH	FUNCTION	SETTINGS
S8	Self-Test Mode	UP = Self-Test Mode 1 DOWN = Self-Test Mode 0
S7	Data Settling Time Selection	UP = Normal Speed DOWN = High Speed
S6	System Controller Selection	UP = System Controller DOWN = Not System Controller
S1 - S5	HP-IB Address Selection (when not Controller-In-Charge)	S5 = MSB S1 = LSB UP = Logic One DOWN = Logic Zero

The factory settings for the configuration switches are as follows:

S1	S2	S3	S4	S5	S6	S7	S8
DOWN	UP	UP	UP	UP	UP	UP	DOWN

The foregoing switch settings correspond to:

Test Mode - 1
Speed - STANDARD
System Controller - ON
Address - 30 DECIMAL

Self-Test Mode Selection

Switch S8 selects self-test mode 1 or mode 2. This switch should be DOWN, for self-test mode 1.

Data Settling Time Selection

Switch S7 determines the time delay between the assertion of the data on the bus and the assertion of the Data Valid (DAV) signal. With the switch in the standard (up) position, a delay of approximately 500 nsec is selected. When the switch is set to the high-speed (down) position, the delay is reduced to approximately 350 nsec. This delay time satisfies IEEE Standard 488-1978 for fast settling time required for high-speed operation. Refer to the paragraph "High-Speed Operation" for additional information on high-speed operation.

System Controller Selection

Switch S6 determines if the HP-IB card will be the System Controller for the HP-IB bus. If the switch is open (up), the card will function as the System Controller.

HP-IB Address Selection

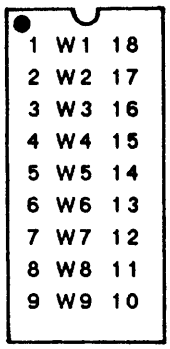
Switches S1 through S5 determine the HP-IB card address when the card is not Controller-In-Charge. An open (up) switch represents a logic one and a closed (down) switch represents a logic zero. Switch S4 selects the Most Significant Bit (MSB) and S8 selects the Least Significant Bit (LSB). The switches are set to decimal 30 at the factory. Note that decimal 31 is not a legal address and results in a flashing LED on the HP-IB card.

EXTERNAL MEMORY SELECTION

Three 28-pin sockets on the HP-IB printed circuit card accomodate external, byte-wide memory. One socket (U61) is used for program memory (ROM/EPROM), and the other two (U41 and U51) are used for data memory (RAM). The HP-IB card is shipped from the factory with the correct ROM/RAM circuits installed and strapped for correct operation. Memory updates are performed by changing/adding appropriate memory components and changing the memory jumpers located on the 18-pin DIP (Dual Inline Package) socket, U71. Jumper configurations for external memory updates are shown on the next page.

ROM SIZE (bytes)	INSTALL	RAM1 SIZE	INSTALL	RAM2 SIZE	INSTALL
8K	W3	2K	W6	2K	W8
4K	No jumper installed	8K	W7	8K	W9

U71



I/O CHANNEL INTERFACE

All interface between the HP-IB and the host computer occurs on the I/O channel. An 80-pin connector (J1) located on the HP-IB card mates with a receptacle on the I/O channel. Connections to J1 are listed in table 2-2.

PERIPHERAL DEVICE INTERFACE CABLE

As listed below, several cables are available with the HP 27110A product. The selected cable connects from the 26-pin connector (J2) on the HP-IB card to the HP-IB-compatible peripheral device. Connections to J2 are listed in table 2-3.

HP-IB CABLE	LENGTH (meters)
10833A	1
10833B	2
10833C	4
10833D	0.5

Table 2-2. I/O Channel Bus Connector J1

PIN NO.	SIGNAL MNEMONIC	SIGNAL DEFINITION
A1	SAFETY	Safety Ground
A2	DB14	Data Bus, bit 14
A3	DB12	Data Bus, bit 12
A4	GND	Ground
A5	DB10	Data Bus, bit 10
A6	DB8	Data Bus, bit 8
A7	GND	Ground
A8	DB6	Data Bus, bit 6
A9	DB4	Data Bus, bit 4
A10	GND	Ground
A11	DB2	Data Bus, bit 2
A12	DB0	Data Bus, bit 0
A13	GND	Ground
A14	AD2	Address Bus, bit 2
A15	AD0	Address Bus, bit 0
A16	GND	Ground
A17	DOUT	Data Out
A18	BP0	Bus Primitive, bit 0
A19	CEND	Channel End
A20	SYNC	Synchronize
A21	GND	Ground
A22	CCLK	Common Clock
A23	GND	Ground
A24	BR	Burst Request
A25	DBYT	Device Byte
A26	MYAD	My Address
A27	GND	Ground
A28	---	Not used
A29	---	Not used
A30	---	Not used
A31	---	Not used
A32	---	Not used
A33	PPON	Primary Power On
A34	GND	Ground
A35	---	Not used
A36	---	Not used
A37	---	Not used
A38	+12	+12V
A39	---	Not used
A40	+5	+5V

Table 2-2. I/O Channel Bus Connector J1 (Continued)

PIN NO.	SIGNAL MNEMONIC	SIGNAL DEFINITION
B1	SAFETY	Safety Ground
B2	DB15	Data Bus, bit 15
B3	DB13	Data Bus, bit 13
B4	GND	Ground
B5	DB11	Data Bus, bit 11
B6	DB9	Data Bus, bit 9
B7	GND	Ground
B8	DB7	Data Bus, bit 7
B9	DB5	Data Bus, bit 5
B10	GND	Ground
B11	DB3	Data Bus, bit 3
B12	DB1	Data Bus, bit 1
B13	GND	Ground
B14	AD3	Address Bus, bit 3
B15	AD1	Address Bus, bit 1
B16	GND	Ground
B17	UAD	Unary Address
B18	BP1	Bus Primitive, bit 1
B19	CBYT	Channel Byte
B20	POLL	Poll
B21	GND	Ground
B22	IOSB	I/O Strobe
B23	GND	Ground
B24	ARQ	Attention Request
B25	DEND	Device End
B26	RST	Reset
B27	GND	Ground
B28	---	Not used
B29	---	Not used
B30	---	Not used
B31	---	Not used
B32	---	Not used
B33	---	Not used
B34	GND	Ground
B35	---	Not used
B36	---	Not used
B37	---	Not used
B38	+12	+12V
B39	---	Not used
B40	+5	+5V

Table 2-3. Device Connector J2

PIN NO.	SIGNAL MNEMONIC	SIGNAL DEFINITION
A1	GND	Ground
A2	---	Not used
A3	ATN	Attention
A4	SRQ	Service Request
A5	IFC	Interface Clear
A6	NDAC	Not Data Accepted
A7	NRFD	Not Ready For Data
A8	DAV	Data Valid
A9	EOI	End Or Identify
A10	DIO4	Data Input/Output, Bit 4
A11	DIO3	Data Input/Output, Bit 3
A12	DIO2	Data Input/Output, Bit 2
A13	DIO1	Data Input/Output, Bit 1
B1	GND	Ground
B2	GND	.
B3	GND	
B4	GND	
B5	GND	.
B6	GND	
B7	GND	.
B8	GND	Ground
B9	REN	Remote Enable
B10	DIO8	Data Input/Output, Bit 8
B11	DIO7	Data Input/Output, Bit 7
B12	DIO6	Data Input/Output, Bit 6
B13	DIO5	Data Input/Output, Bit 5

GENERAL GUIDELINES FOR HP-IB OPERATION

The following general guidelines should be observed when configuring an HP-IB system:

1. Devices or cable segments should not be added to an HP-IB system that is active.

   If a device is to be added to an active HP-IB system, the possibility of errors will be minimized if the following procedure is used:

   a. Attach all new cables to the new device (the device to be added). Do not attach any unterminated cables to the existing bus.

   b. Power on the new device.

c. Attach the new device (with power on) and its cable to the existing bus as a unit.

2. Devices which talk at a slower rate may be configured in the same system as high-speed devices, provided all of the requirements for high-speed operation are met.

3. If the card is NOT being used as the System Controller (SCTL switch DOWN), the high-speed load resistors should NOT be installed, regardless of speed configuration. In an HP-IB system, it is the duty of the System Controller to provide the necessary additional high-speed termination resistors. ADDING TERMINATION RESISTORS TO MORE THAN ONE CARD IN AN HP-IB SYSTEM MAY RESULT IN PERMANENT DAMAGE TO ANY OR ALL CARDS IN THE SYSTEM. Also, a powered-down System Controller will not allow the system to be used (as long as the System Controller is connected) because HP-IB bus drivers cannot drive the powered-down termination resistors.

4. Bus configuration is unimportant as long as the guidelines in the following paragraphs are observed.

MEDIUM-SPEED OPERATION

In order to ensure proper operation of the HP-IB bus, some rules must be observed regarding the total length of cables being used, as follows:

1. The total length of cable permitted to be used with one interface card must be less than or equal to two meters times the number of devices connected together for standard speed operation (the interface card is counted as one device).

2. The total length of cable in standard speed systems must not exceed 20 meters.

3. At least four out of every five devices should be powered on.

4. Refer to the following paragraph for high-speed operation.

HIGH-SPEED OPERATION

To achieve the maximum possible data transfer rate within a system, the following guidelines must be followed:

1. Switch S7 should be set to high speed (down). Switch S7 determines the delay between data assertion and DAV during an HP-IB write from the computer to the device. With the switch in normal (up) position, a delay of approximately 500 nsec is realized. In the high-speed (down) position, the delay is reduced to approximately 350 nsec.

2. All devices expected to talk at high speed must use a settling time of 350 nsec or less.

3. All devices expected to talk at the higher rates should use 48 mA three-state drivers.

4. The device capacitance on each HP-IB line (except REN and IFC) should be less than 50 pF per device. In a system configuration, the total device capacitance should be no more than 50 pF for each equivalent resistive load in the system.

5. The optional load resistor pack must be installed for high-speed operation. The 18-pin Dual In-line Package (DIP) is marked 1810-0081, and is carried in a socket on the interface card marked "LOAD RESISTOR STORAGE". Remove the load resistor pack from the storage socket and install it in the socket directly behind connector J2 (peripheral device cable connector), with pin 1 on the package oriented toward the U82 marking next to the socket.

6. Interconnecting cable links should be as short as possible, with a maximum of 15 meters total length per system, and should have at least one equivalent resistive load per meter of cable (the high-speed resistor pack adds seven equivalent resistive loads).

Number of Devices	Maximum Total Cable Length (meters)	Maximum Average Cable Length Between Devices (meters)
1	9	9
2	10	5
3	11	3
4	12	3
5	13	2
6	14	2
7 (maximum)	15	2

No more than eight devices are allowed in the system (the HP-IB interface card counts as one device). A maximum system would therefore be composed of the System Controller, with its high-speed resistor pack, and seven peripherals.

7. All devices should be powered on.

INSTALLATION

CAUTION

SOME OF THE COMPONENTS USED ON THE PRINTED CIRCUIT CARD ARE SUSCEPTIBLE TO DAMAGE BY STATIC DISCHARGE. REFER TO THE SAFETY CONSIDERATIONS INFORMATION AT THE FRONT OF THIS MANUAL BEFORE HANDLING THE CARD.

To install the HP-IB card, proceed as follows:

1. Determine if your computer system can supply the power needed for the HP-IB card. Refer to table 1-1 for power requirements.

2. Set switch S7 up (standard speed) or down (high speed) depending on whether or not the card is going to require the normal or fast settling mode of operation. All high-speed devices should be labeled appropriately. Check that the optional load resistor pack (see the "HIGH-SPEED OPERATION" paragraph) is installed if high-speed devices are going to be connected to the card.

3. Set switch S6 up (System Controller ON) or down (System Controller OFF) depending on whether the card is going to operate as the System Controller.

4. Set switches S1 through S5 to the card's HP-IB address. If the card is to be the System Controller (switch S7 UP), set the address to 30 decimal (S1 DOWN, S2 through S5 UP).

5. Turn off power to the computer and the HP-IB devices. Insert the HP-IB card into the desired slot in the I/O channel. Make sure that the components on the card are on the same side as the other installed cards. When installing the card, use care not to damage the components or traces on the card or on adjacent cards. Press the card firmly into place.

6. Connect the appropriate cable from J2 on the card to the device. See the paragraph "PERIPHERAL DEVICE INTERFACE CABLES" for cable information.

START-UP

To start-up and verify correct operation of the HP-IB card, perform the following:

1. Turn on computer system power.

2. A self-test is contained on the card. The host computer system determines if the self-test is run automatically at power-on or must be invoked by the user. Refer to the appropriate manual for your system for a description of self-test initiation.

   When the self-test executes, the LED located on the card should light briefly and go out. This indicates that the card passed self-test. If the LED does not light at all, the card is defective. If the LED stays on, the card did not pass self-test.

   If the LED flashes continuously, the address switches have been set to an illegal address (31 decimal, all address switches UP). Set the address switches (S1 through S5) to a valid address (zero through 30) and issue a system reset. The LED should go out, indicating a valid address has been read and the card has passed self-test.

   If the self-test indicates that the card is defecive, it is recommended that you return the card to Hewlett-Packard; refer to the next paragraph for reshipment information. If you wish to perform maintenance on the card, however, refer to Sections 5, 6, and 7 for maintenance information, replaceable parts lists, and schematic logic diagrams, respectively.

RESHIPMENT

If the HP-IB is to be shipped to Hewlett-Packard for any reason, attach a tag identifying the owner and indicating the reason for shipment. Include the part number of the HP-IB.

Pack the HP-IB in the original factory packing material, if available. If the original material is not available, good commercial packing material should be used. Reliable commercial packing and shipping companies have the facilities and materials to repack the item. BE SURE TO OBSERVE ANTI-STATIC PRECAUTIONS.

PRINCIPLES OF OPERATION

SECTION III

The HP 27110A HP-IB Interface card provides an interface between a Hewlett-Packard computer system and an HP-IB system of up to 14 devices. Several such HP-IB systems, each connected to an HP-IB interface card, can be connected to one host computer.

OVERVIEW

Block and schematic diagrams for the HP-IB card are contained in Section VII. The functional block diagram of the HP-IB card is shown in figure 7-1; the schematic logic diagram is shown in figure 7-2. Reference is made to these two figures during the following discussions. Note that figure 7-2 consists of two sheets. References to this figure will be as follows: 1-A11, 7-2; 2-C23, 7-2, etc., where the first number, 1 or 2, refers to the sheet number, the combination of letters A through G and numbers 11 through 28 (A11, C23, etc.) refer to the quadrants on the individual sheets, and 7-2 refers to the figure number.

As shown in figure 7-1, six devices have access to all eight lines of the data bus as follows:

Device	Access Direction
HP-IB Circuit	Read/Write
Address Latch	Write
Z8 Microcomputer	Read/Write
External ROM	Read
Switch Register	Read
Backplane Interface Circuit (BIC)	Read/Write

The devices are controlled by the Z8 or the DMA controller (see figure 7-1.)

Interface between the HP-IB card and the I/O channel is accomplished via the Backplane Interface Circuit (BIC, see 7-1 and 2-A22, 7-2) gate array and transceivers. Interface between the card and the HP-IB bus is accomplished via the HP-IB circuit (see 7-1 and 2-A25, 7-2).

Direct memory access (DMA) is used on HP-IB data transfers, and is accomplished via a DMA state machine controller contained in a programmable logic array (see 7-1 and 1-E15, 7-2), and controlled by the Z8 microcomputer (7-1 and 1-A12, 7-2). The Z8 does not allow other devices (including itself) to use the data bus while DMA is in progress.

The Address Latch (7-1 and 1-B13, 7-2) latches the lower eight address bits (A0 - A7) from the multiplexed Address/Data bus. Only the memory components (ROM, RAM) require these address bits - all other devices are addressed via A8 - A12.

The Switch Register (1-A16, 7-2) buffers the HP-IB address of the card to the Z8.

BACKPLANE INTERFACE

The Backplane Interface Circuit (BIC, a CMOS gate array chip, see 2-A22, figure 7-2) provides a standard method of interfacing to the I/O channel (backplane).

From a hardware standpoint, the BIC performs as a simple microprocessor peripheral. As used in the HP-IB card, the BIC has the following standard signal lines:

* Eight-bit bidirectional tri-state data bus
* Three-bit address bus
* Chip Select line to enable the chip for addressed data transfers
* Data Strobe line to strobe incoming data
* Read/Write line to specify data transfer direction
* Interrupt line to alert the Z8 of important events occurring on the I/O channel

Table 3-1 lists pin connections and describes signals to the BIC.

Table 3-1. BIC Chip Pin Connections

PIN NO.	SIGNAL MNEMONIC	BIC MNEMONIC	DESCRIPTION
1	D0	D0	Data Bus, Bit 0
2	D2	D2	Data Bus, Bit 2
3	D4	D4	Data Bus, Bit 4
4	D6	D6	Data Bus, Bit 6
5	END-	END-	Indicates end of data read or write
6	A8	A0	Register Address, Bit 0
7	A10	A2	Register Address, Bit 2
8	Z8RD	DS0-	Z8 Read (Read Data Strobe)
9	RDY-		Asserted by BIC when ready for data transfer
10	---		Not used
11	---		Not used
12	BIC:INT-	INT-	BIC Interrupt
13	NMI	NMI	Non-Maskable Interrupt
14	IFC (RST)	IFC	Interface Clear (Reset)
15	POLL	POLL	Poll
16		SYNC_MYAD-	In conjunction with DE, determines data bus drivers mode of operation
17	DOUT	DOUT	Data Out, specifies data bus direction
18	BP0	BP0	Bus Primitive, Bit 0. With BP1, specifies bus primitive operation
19	UAD	UAD	Unary Address, latches BIC channel address after a PPON or IFC
20	AD0	AD0	Address Bus, Bit 0
21	AD2	AD2	Address Bus, Bit 2
22	CEND	CEND	Channel End
23	DB0	BIOD0-	Backplane I/O Data, Bit 0
24	DB1	BIOD1-	Backplane I/O Data, Bit 1
25	DB3	BIOD3-	Backplane I/O Data, Bit 3
26	DB5	BIOD5-	Backplane I/O Data, Bit 5
27	DB7	BIOD7-	Backplane I/O Data, Bit 7
28	DB9	BIOD9-	Backplane I/O Data, Bit 9
29	DB10	BIOD10-	Backplane I/O Data, Bit 10
30	DB11	BIOD11-	Backplane I/O Data, Bit 11
31	DB13	BIOD13-	Backplane I/O Data, Bit 13
32	DB15	BIOD15-	Backplane I/O Data, Bit 15
33	BR	BR	Burst Request - at least one more transfer after current one
34	DBYT	DBYT	Device Byte, indicates current transfer is a byte
35	IOSB	IOSB	I/O Strobe

Table 3-1. BIC Chip Pin Connections (Continued)

PIN NO.	SIGNAL MNEMONIC	BIC MNEMONIC	DESCRIPTION
36	D1	D1	Data Bus, Bit 1
37	D3	D3	Data Bus, Bit 3
38	D5	D5	Data Bus, Bit 5
39	D7	D7	Data Bus, Bit 7
40	GND	GND	Ground
41	A9	A1	Register Address, Bit 1
42	BIC:SEL-	CHSEL-	BIC Select, enables the BIC to read or write
43	DS-	DS1-	Data Strobe (Write Data Strobe)
44	DTR-	DTR-	Data Transfer Request
45	RESET-	RST-	Reset
46	ARQ	ARQ	Attention Request
47	+5		+5 V
48	SYNC	SYNC	Synchronize, signals that an addressed bus operation will occur
49	MYAD	MYAD	My Address
50	BP1	BP1	Bus Primitive, Bit 1 - with BP0, specifies bus primitive operation
51	AD1	AD1	Address Bus, Bit 1
52	AD3	AD3	Address Bus, Bit 3
53	CBYT	CBYT	Channel Byte, indicates that current transfer is a byte
54	GND	GND	Ground
55	DB2	BIOD2-	Backplane I/O Data, Bit 2
56	DB4	BIOD4-	Backplane I/O Data, Bit 4
57	DB7	BIOD7-	Backplane I/O Data, Bit 7
58	DB8	BIOD8-	Backplane I/O Data, Bit 8
59	DB12	BIOD12-	Backplane I/O Data, Bit 12
60	DB14	BIOD14-	Backplane I/O Data, Bit 14
61	---		Not used
62	DEND	DEND	Device End, indicates end of transfer
63	DE	DE	Direction Enable
64	PPON	PPON-	Primary Power On

A set of eight BIC registers, addressed by the 3-bit address bus, perform the following functions:

Register Number	Write Direction	Read Direction
0	<========== DATA ==========>	
1	COMMAND	SRQ ADDRESS
2	ORDER	BIC STATUS
3	BACKPLANE STATUS	BACKPLANE CONTROL
4	<======== CONFIGURATION ======>	
5	<======== INTERRUPT ==========>	
6	<====== INTERRUPT MASK =======>	
7	<========= RESERVED ==========>	

In addition to the eight registers, the BIC provides:

A "ninth" data bit called END-. This open collector line is bi-directional. When the HP-IB card is performing a host write, this data bit is set true (LOW) to indicate the associated data byte is the last of that transfer. When reading from the host, the BIC drives END- true when the data byte on the 8-bit bus is the last of the transfer. Timing for END- is identical to data bus timing, thus the term "ninth data bit".

DMA lines DTR- (Data Transfer Request) and RDY- (Ready) for unaddressed data transfers. These lines allow the BIC to transfer data in or out quickly without the necessity of repeatedly addressing the FIFO (First In First Out) data register in the HP-IB circuit. The DTR- and RDY- lines provide a 2-wire handshake for performing unaddressed FIFO data transfers (DMA). DTR- is driven by the DMA controller when the controller is ready to begin a DMA transfer. RDY- is driven by the BIC when it is ready to begin a data transfer (when the FIFO data register has room on a host read or the FIFO is not empty on a host write). DTR- is not allowed to be driven true unless RDY- is true.

A reset line (RESET-) to initialize the Z8. RESET- informs the Z8 that one or more of the following events has occurred:

* Primary power has been turned on

* A CHANNEL I/O Interface Clear has been issued (global reset)

* A CHANNEL I/O Device Clear has been issued (addressed reset)

RESET- connects directly to the Z8 reset input. By polling the BIC registers after a reset, the Z8 can determine which of the three types of reset occurred, and take the appropriate action.

A timing diagram for a BIC DMA - host read is shown in figure 3-1. BIC DMA - host write timing is shown in figure 3-2.

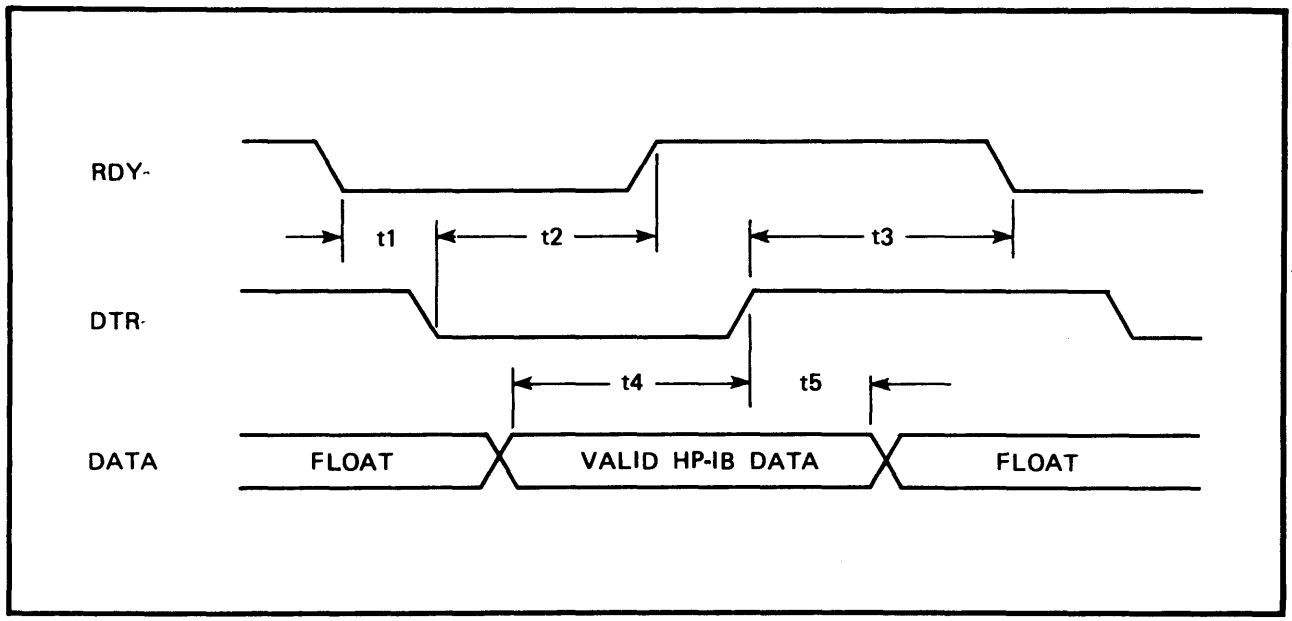


Figure 3-1. BIC DMA - Host Read Timing Diagram

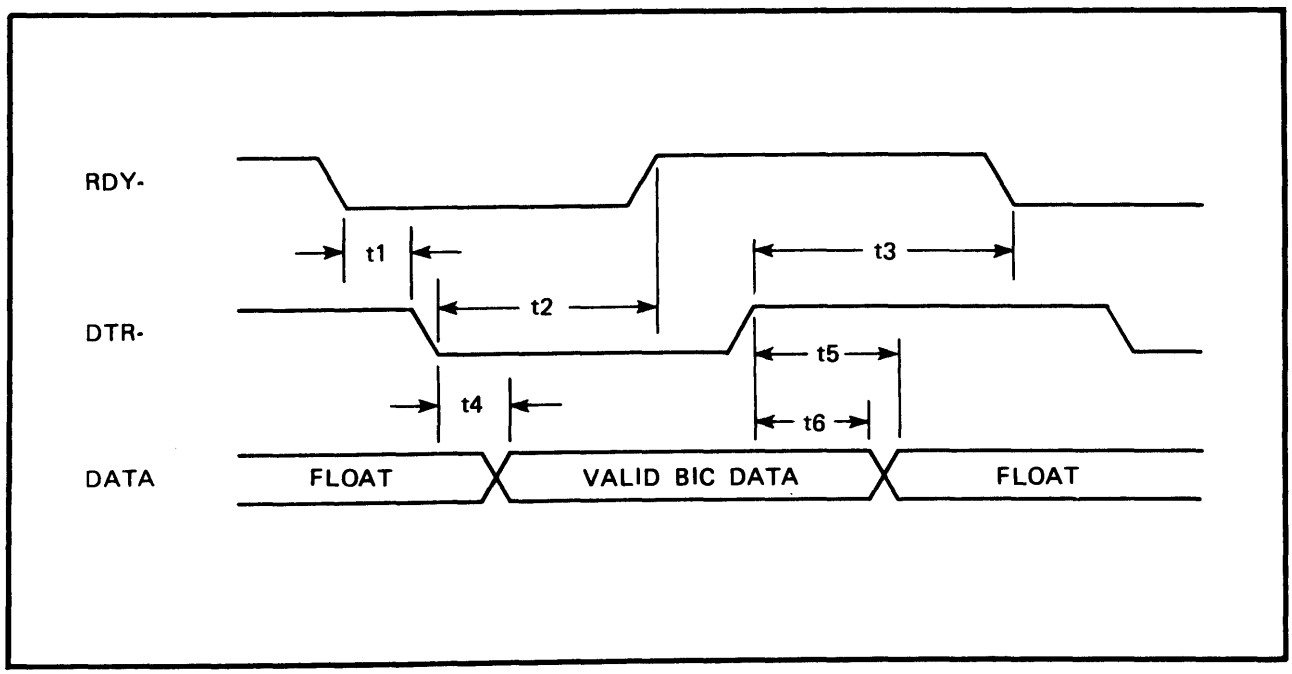


Figure 3-2. BIC DMA - Host Write Timing Diagram

HP-IB INTERFACE

The HP-IB circuit (an NMOS chip, see 2-A25, 7-2) provides a high-speed interface between the Z8 and the HP-IB bus. As with the BIC chip, the HP-IB chip appears to the Z8 as a simple microprocessor peripheral.

The HP-IB chip contains the following lines:

* A ten-bit wide data bus

* Three register-select lines for selecting among the HP-IB chip's eight registers. Table 3-2 shows the HP-IB chip registers selected by the register-select codes.

Table 3-2. HP-IB Chip Register Selection

HP-IB REGISTER SELECT CODE			REGISTER NUMBER	REGISTER NAME
A13	A14	A15		
0	1	0	0	FIFO
0	1	1	1	HP-IB Chip Status
0	0	0	2	Interrupt
0	0	1	3	Interrupt Mask
1	1	0	4	Parallel Poll Mask
1	1	1	5	Parallel Poll Sense
1	0	0	6	HP-IB Control
1	0	1	7	HP-IB Address

* Chip select

* Read/write line

* Data strobe line (IOGO-)

The ninth and tenth bits of the 10-bit data bus are used by the HP-IB chip registers to provide a special meaning to the 8-bit register value. For example, in the inbound FIFO direction, these two bits indicate whether or not a secondary has been addressed, if the last byte or a record has occurred, if the last byte of a subgroup has occurred, or if a counted transfer has ended. In the outbound FIFO direction, the two bits are used to specify ATN and EOI true.

HP-IB chip pin connections are listed in table 3-3.

Table 3-3. HP-IB Chip Pin Connections

PIN NO.	CHIP MNEMONIC	TYPE	DESCRIPTION
			HP-IB DATA LINES - LOW TRUE
44	DIO1-	B	Data Input/Output, Bit 1 - low true
45	DIO2-	B	.
46	DIO3-	B	.
47	DIO4-	B	.
48	DIO5-	B	.
2	DIO6-	B	.
3	DIO7-	B	.
4	DIO8-	B	Data Input/Output, Bit 8 - low true
			HP-IB HANDSHAKE LINES
18	ATN-	B	Attention
16	RFD	B	Ready For Data
15	DAC	B	Data Accepted
			HP-IB BUS MANAGEMENT LINES - LOW TRUE
6	DAV-	B	Data Available
5	EOI-	B	End Or Identify
14	REN-	B	Remote Enable
13	IFC-	B	Interface Clear
17	SRQ-	B	Service Request
			INTERNAL DATA LINES
30	D0	B	These two bits indicate the following bus
29	D1	B	conditions when read from register 2: D0 D1 -- -- 0 0 Normal data 0 1 Secondary Address 1 0 Last byte of subgroup 1 1 Last byte of record
28	D8	B	Z8 Data Bus, Bit 7
27	D9	B	Z8 Data Bus, Bit 6
26	D10	B	Z8 Data Bus, Bit 5
25	D11	B	Z8 Data Bus, Bit 4
24	D12	B	Z8 Data Bus, Bit 3
23	D13	B	Z8 Data Bus, Bit 2
22	D14	B	Z8 Data Bus, Bit 1
21	D15	B	Z8 Data Bus, Bit 0

Table 3-3. HP-IB Chip Pin Connections (Continued)

PIN NO.	CHIP MNEMONIC	TYPE	DESCRIPTION
33	A13	I	Register address lines used by Z8 to access HP-IB chip registers, along with IB:WRT and IB:SEL-.
34	A14	I	
35	A15	I	
7	SCTRL	I	Makes HP-IB card System Controller
40	PON	I	When low, initializes HP-IB chip for >500ns
39	W	I	Write enable, read disable (IB:WRT)
36	IOGO-	I	Initiates a register read/write
32	CHSEL-	I	Enables IOGO-
41	DMARQ-	O	DMA request, indicating that the HP-IB chip FIFO register is ready
38	INT-	O	Requests interrupt from Z8 (ABI:INT-)
37	IOEND-	O	Handshake complete
19	TRIG	O	Pulse generated when HP-IB card gets Group Execute Trigger (GET)
12	CIC	O	Enables ATN driver when true and SRQ driver when false
11	HSE	O	Transceivers use active pullups (vs open collector)
10	DEE	O	DAV/EOI enable (send DAV and EOI, vs receive)
9	DIOE	O	DIO enable (send data, vs receive)
43	VDD	P	+12V
1	GND	P	Ground
8	VCC	P	+5V
31	VDC	P	+5
42	RS	T	Delay stabilizing resistor
20	RTL	I	Return to local (tied permanently false)

Line types: B = Bidirectional
I = Input
O = Output
P = Power
T = Timing

The signals IOEND- and DMARQ- (see figure 7-2, 2E26) are used for DMA purposes only (no handshaking occurs on an addressed HP-IB chip access). IOEND- false (high) and DMARQ- true (low) indicate that the HP-IB chip is ready to transfer a byte via DMA in the direction specified by its read/write line. This condition (IOEND- false and DMARQ- true) is ANDed with the BIC RDY- signal to generate Interface Ready (IF:RDY-). When the DMA controller detects IF:RDY- true, it is ready to begin DMA upon command from the Z8.

The IOGO- signal (1-E16, 7-2) is asserted by the DMA controller to handshake DMA data through the HP-IB chip, and also for normal HP-IB chip register accesses. Note that IOGO- is a combination of the Z8 data strobe, and the DMA controller strobe. The DMA controller ensures that the timing relationships between data and IOGO- are maintained.

Because the HP-IB chip generates its IEEE-488 timing via RC timing constants, a tuning network (2-F25, 7-2) is provided to extract the maximum possible data rate. A potentiometer is used, with a firmware routine, to adjust the pulse widths of a continuous stream of pulses. The potentiometer is set at the factory and requires no further adjustment.

The HP-IB chip TRIG signal (2-F26, 7-2) goes high when a Group Execute Trigger (GET signal, see 1-B15, figure 7-2) occurs on the HP-IB card. The GET signal is a means of triggering a number of devices, such as voltmeters, to take readings simultaneously. ABI:INT- becomes true if any of its nine interrupting conditions exists. The HP-IB chip Interrupt register defines these conditions, as follows:

Parity Error

Status Change

Processor Handshake Abort

Parallel Poll Response

Service Request

FIFO Room Available

FIFO Bytes Available

FIFO Idle

Device Clear

The ABI:INT- signal is deasserted when the interrupting condition no longer exists.

The HP-IB bus transceivers (2-B27, 7-2) have two types of control inputs: One input determines the direction of the transceiver (send or receive), and is labeled "TE" for Talk Enable. The other input determines whether the outputs facing the HP-IB are open collector or active TTL (when Talk Enable is true). Each transceiver has a pullup to +5 and a pulldown to ground.

All signals and data on the HP-IB card are low true, except NRFD and NDAC. When NRFD is high, all devices on the bus are ready for data. When NDAC is high, all devices that were to receive data have received the data. In a powered-down system, all lines are true, except that all devices are not ready and have not accepted data.

HP-IB Chip DMA Read Timing

The following steps describe the sequence of events during a host read from the HP-IB chip. A timing diagram is shown in figure 3-3. The signals are referenced to their origins on figure 7-2 in Section VII.

1. The first step in a host read from the HP-IB chip is to wait until DMARQ- (2-E26, 7-2) goes true (indicating that the HP-IB chip FIFO is ready to move another byte), and IOEND- (2-E26, 7-2) goes false (indicating that the previous handshake has completed).

2. IOGO- (1-E16 and 2-C25, 7-2) may now be asserted. On a host read, IOGO- indicates to the HP-IB chip that the HP-IB card is prepared to accept inbound data. Once asserted, data from the HP-IB chip will become valid 25-140ns later.

3. Up to 250ns after IOGO- is asserted, IOEND- will become true, indicating that the HP-IB chip has completed the inbound data transfer. DMARQ- momentarily goes false 100ns (maximum) after IOEND- goes true.

4. IOEND- is acknowledged by deasserting IOGO-.

5. IOEND- will go false in response to IOGO- deassertion. If the inbound FIFO has more data in it, DMARQ- goes true within 150ns after IOGO- is deasserted. If no data is left in FIFO, then DMARQ- remains false until the FIFO receives another data byte from the HP-IB bus. To continue a host read, the process is repeated beginning at step 1.

HP-IB Chip DMA Write Timing

The steps listed below describe the sequence of events during a host write to the HP-IB chip. A timing diagram is shown in figure 3-4. The signals are referenced to their origins on figure 7-2.

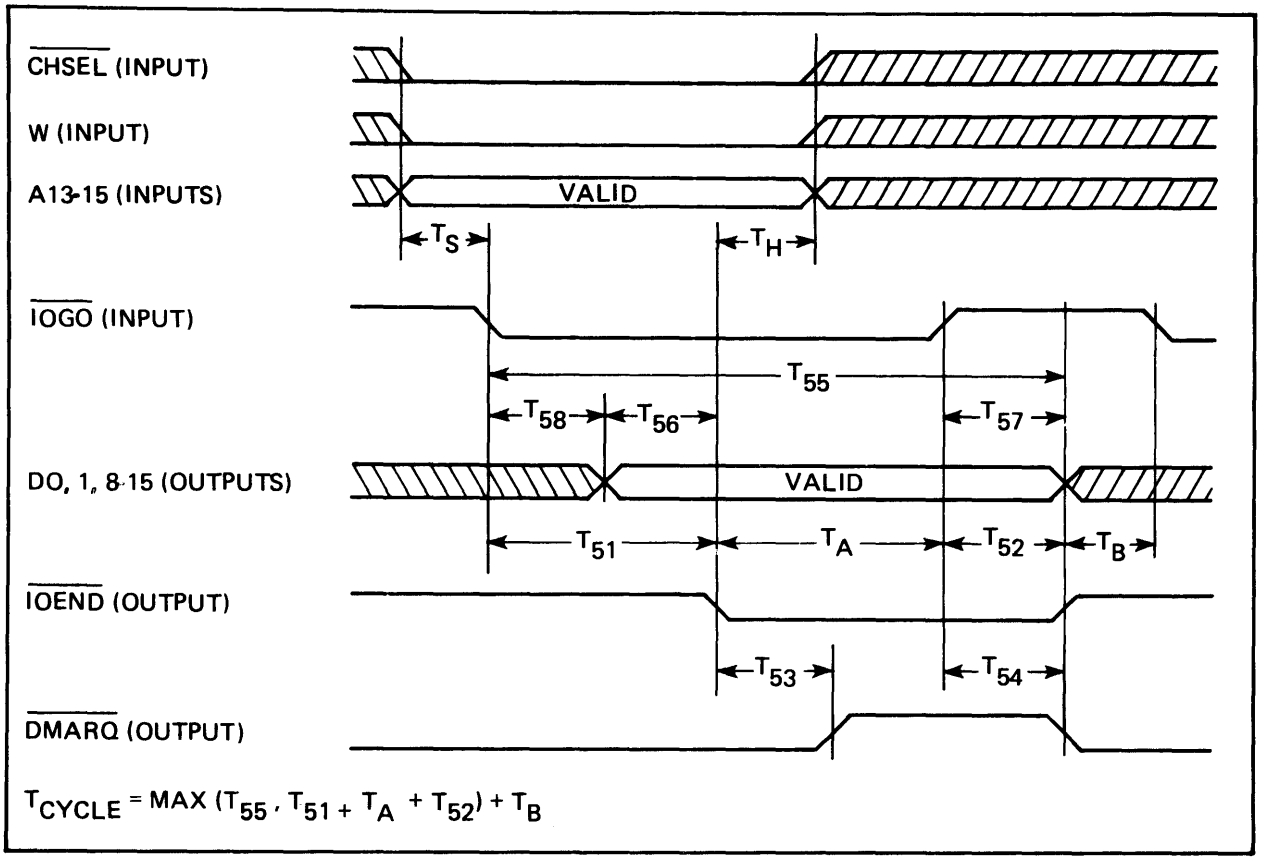
1. Assuming the data source (BIC) has data ready to send, the first step in a host write operation is to wait for IOEND- (2-E26, 7-2) false and DMARQ- (2-E26, 7-2) true, as in a host read.

2. IOGO- (1-E16, 7-2) is asserted to initiate the transfer.

3. A maximum of 150ns later, IOEND- is asserted, indicating that the HP-IB chip has accepted the data. Then, 100ns (maximum) after IOEND- goes true, DMARQ- goes false.

4. IOEND- is recognized and IOGO- is deasserted.

5. IOEND- goes false in response to IOGO- deassertion. If the outbound FIFO is not full, DMARQ- goes true; if the outbound FIFO is full, DMARQ- goes false until the FIFO is not full. To continue the host write, the steps are repeated beginning at step 1.



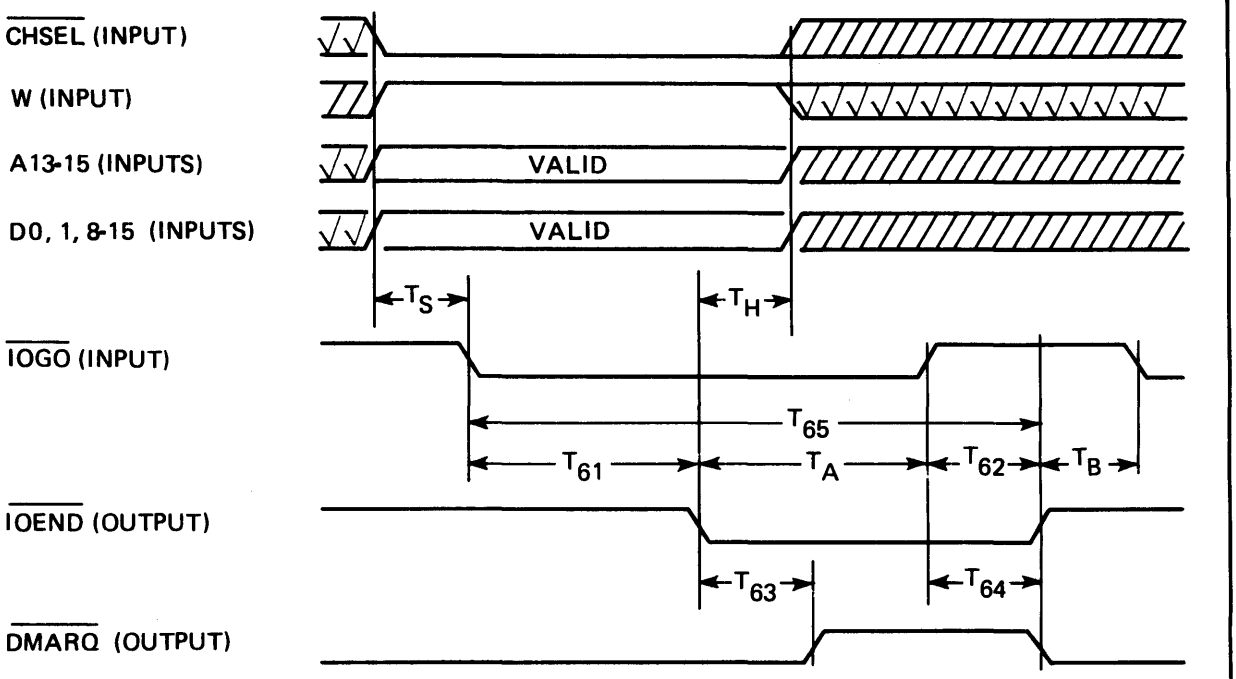
SWITCHING CHARACTERISTICS, V_{DD} = 12V±5%, V_{DC}= 12V±5% OR 5V±5% OR 0°C ≤T≤70°C

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
T_{51} $\overline{IOGO}$ ⌉ TO $\overline{IOEND}$ ⌉				250	NS
T_{52} $\overline{IOGO}$ ⌋ TO $\overline{IOEND}$ ⌋				150	NS
T_{53} $\overline{IOEND}$ ⌉ TO $\overline{DMARQ}$ ⌋	A13-A15 = 010, REG 4 (14) = 0	FIFO NOT EMPTY		125	NS
T_{54} $\overline{IOGO}$ ⌋ TO $\overline{DMARQ}$ ⌉		1 BYTE IN FIFO		150	NS
T_{55} $\overline{IOGO}$ ⌉ TO $\overline{IOEND}$ ⌋	T_A = ONS			450	NS
T_{56} DATA TO $\overline{IOEND}$ ⌉	A13-A15 = 010, FIFO NOT EMPTY		25		NS
	ALL REGISTERS EXCEPT ABOVE		−30*		NS
T_{57} $\overline{IOGO}$ ⌋ TO DATA OFF			25	140	NS
T_{58} $\overline{IOGO}$ ⌉ TO DATA ON	A13-A15 = 010, FIFO NOT EMPTY		25	140	NS

RECOMMENDED SAMPLE AND HOLD TIMES: $T_S \geq$ ONS, $T_H \geq$ ONS

*NEGATIVE SIGN INDICATES IOEND MAY RESPOND BEFORE DATA

Figure 3-3. HP-IB Chip DMA Read Timing



$T_{CYCLE} = MAX\ (T_{65}, T_{61}+T_A+T_{62}) + T_B$

SWITCHING CHARACTERISTICS, V_{DD} = 12V±5%, V_{DC} = 12V±5% OR 5V±5%, 0 °C ≤ T_A ≤ 70°C

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
T_{61} $\overline{IOGO}$ ⌉ TO $\overline{IOEND}$ ⌉				150	NS
T_{62} $\overline{IOGO}$ ⌋ TO $\overline{IOEND}$ ⌋				150	NS
T_{63} $\overline{IOEND}$ ⌉ TO $\overline{DMARQ}$ ⌋	A13-A15 =010, REG 4 (14) =1	FIFO NOT FULL		100	NS
T_{64} $\overline{IOGO}$ ⌋ TO $\overline{DMARQ}$ ⌉		< 7 BYTES IN FIFO		150	NS
T_{65} $\overline{IOGO}$ ⌉ TO $\overline{IOEND}$ ⌋	T_A = 0NS			350	NS

RECOMMENDED SAMPLE AND HOLD TIMES: $T_S \geq$ 0NS, $T_H \geq$ 0NS

Figure 3-4. HP-IB Chip DMA Write Timing

Z8 INTERFACE

The Z8 (U44, see 1-A12, 7-2) is a single-chip microcomputer that, under software control, can assume different memory and I/O configurations. Thirty-two lines are dedicated to I/O. These lines are grouped into four ports of eight lines each, and are configurable as input, output, or bidirectional. Under software control, the ports can provide timing, status signals, address outputs, and serial or parallel I/O with or without handshake. In the HP-IB card, all device communication is done via memory-mapped I/O. That is, the BIC and HP-IB chip registers and the DMA/PPOL control lines are all addressed as external memory.

Table 3-4 shows the Z8 pin connections grouped according to the four ports; the Z8 pin connections are listed again in table 3-5 with the signals described in greater detail.

Table 3-4. Z8 Pinouts Grouped by Port

PORT 0	PORT 1	PORT 2	PORT 3
P00: A8	P10: D0	P20: BUCKET	P30: IB:IFC-
P01: A9	P11: D1	P21: SEND:ATN	P31: BCINTS-
P02: A10	P12: D2	P22: SEND:EOI-/EOC	P32: IBINTS-
P03: A11	P13: D3	P23: LED:ON	P33: DMA:INT-
P04: A12	P14: D4	P24: EN:END-	P34: DM-
P05: A13/IO Select 1	P15: D5	P25: LAST:EOI-	P35: DMA:PAUSE
P06: A14/IO Select 2	P16: D6	P26: GET:CLR-	P36: DMA:RST
P07: A15/IO Select 3	P17: D7	P27: ODD	P37: DMA:READ

The Z8 control signals are:

XTAL1	-	Clock Input
AS-	-	Address Strobe
DS-	-	Data Strobe
RESET-	-	Z8 Reset
Z8RD	-	Read/Write Line

Port 0 outputs the upper address byte, valid on the rising edge of AS-.

Port 1 multiplexes the lower address byte and the data byte. A0 through A7 (1-B14, 7-2) are valid on the rising edge of AS-, D0 through D7 (1-B12, 7-2) are valid on the rising edge of DS-.

Port 2 provides general-purpose outputs (see table 3-4).

Port 3 provides interrupt inputs and DMA control lines (see table 3-4).

Table 3-5. Z8 Pin Connections

Z8 MNEMONIC	PIN NO.	DESCRIPTION
	21-28	Port 1. Used for bidirectional internal data bus. Addresses are multiplexed with the data, and latched on the rising edge of AS- (pin 9). On power-on these lines are configured as inputs. After power-on the port is always configured for external memory reference.
	31-38	Port 2. Used for DMA control, Group Execute Trigger Clear, and to send ATN and EOI data. On power-on these lines are configured as inputs, and float high due to external pullups.
P20	31	BUCKET, used to discard data without causing the DMA transfer to end
P21	32	SEND:ATN, used to send ATN data
P22	33	SEND:EOI-/EOC, used to send EOI data; EOC (End On Count) is used to enable device end on counted reads
P23	34	LED:ON, when asserted, turns LED on
P24	35	EN:END, enables END bit generation
P25	36	LAST:EOI-, represents the status of EOI- on the most recent byte transferred across HP-IB.
P26	37	GET:CLR, Group Execute Trigger Clear. Used to clear the GET flip-flop.
P27	38	ODD, driven by the ODD flip-flop, set on every odd byte

Table 3-5. Z8 Pin Connections (Continued)

Z8 MNEMONIC	PIN	DESCRIPTION
P00-P07	13-20	Port 0. Used to provide additional address bits/chip selects for external memory (A8-A15). A13-A15 is used as a "chip" select for I/O, which includes all HP-IB chip and BIC chip registers, the switch (read-only), and the two external RAM sockets.
	6	RESET-. The Z8 will be initialized if PPON is held low for 50 msec or more after power is applied and if the voltage is between 4.75 and 5.25 V.
	7	Z8RD. When high, the Z8 addresses both the ABI and the BIC to be read from, according to the appropriate chip selects. When low, the Z8 is writing to external memory/IO.
	8	Z8DS-, Z8 data strobe. Used to generate the BIC strobe, to latch switch data, and to generate IOGO- from C:IOGO-
	9	AS-, address strobe. Used to latch the lower 8 bits of address from the multiplexed data/address bus (port 1).
	2, 3	Clock inputs (7.3728 MHz frequency, 0.1356 usec period)
	1,11	+5 and GND, respectively
		Port 3. Configured as serial I/O, interrupts, and DMA control lines. P30-33 are always inputs, P34-37 are always outputs.
P30	5	IB:IFC, interface bus IFC line

Table 3-5. Z8 Pin Connections (Continued)

Z8 MNEMONIC	PIN	DESCRIPTION
P31	39	BIC:INT-, BIC interrupt
P32	12	ABI:INT-, ABI interrupt
P33	30	DMA:INT-, DMA controller interrupt
P37	4	DMA:READ, asserted when the Z8 wants to initialize a DMA read operation. Deasserted when the Z8 wants to terminate a DMA read without data loss.
P35	10	DMA:PAUSE, asserted when the Z8 wants to pause DMA with no loss of data.
P36	40	DMA:RST, aborts DMA and acknowledges DMA interrupt
P34	29	DM-, when true, drives chip enable for BIC chip, HP-IB chip, switches, or RAM; when false, drives chip enable for ROM.

Addressing

Devices are selected using the upper three bits (A13, A14, A15) of the 16-bit address bus. This divides the I/O address range into eight 8K segments as shown in table 3-6.

For example, if the firmware references an external, non-program memory address between 8000 and 9FFF, the HP-IB chip will be accessed, with address bits A8 - A10 specifying a particular HP-IB chip register.

Table 3-6. Addressing Codes

A13 - A15	DEVICE SELECTED	ADDRESS RANGE (HEX)
0	Unassigned	0000 - 1FFF
1	Unassigned	2000 - 3FFF
2	BIC	4x00 - 5xFF
3	Switch	6000 - 7FFF
4	HP-IB chip	8x00 - 9xFF
5	RAM1	A000 - BFFF
6	RAM2	C000 - DFFF
7	Unassigned	E000 - FFFF
x = 3-bit register address for the seven BIC or HP-IB chip registers		

Program memory and data memory (I/O) can share the same 16-bit address when the DM- (Data Memory) line is used to distinguish between the two. When the Z8 has a jump to an address over 4K, it knows that program memory is being addressed, and deasserts DM- (set it high). When the Z8 addresses I/O via a Z8 LDE (Load External Data) instruction, the Z8 knows I/O or RAM is being addressed, and asserts DM-. Thus, the HP-IB card uses the DM- signal to:

Enable the I/O device select decoder

and

Disable program memory (ROM)

to avoid bus contention. Data memory can now occupy 64K memory locations, and program memory can occupy 60K external memory locations (4K internal). Other times when DM- is deasserted are when:

Internal code is being executed (no I/O)

and

The Z8 LDC (Load Constant) command is being used to load a byte from ROM (used for register initialization, checksum verification, etc.).

The device select decoder (U55, see C13, figure 7-2) implements the decoding shown in table 3-6 to select the appropriate device.

Switch Register Interface

The Switch register (U74, see 1-A16, figure 7-2) buffers the address switch (S1, 1-A15, 7-2) settings onto the Z8 data bus. When the Z8 reads from the Switch register, the output enable lines from the Switch register become true, and the status of the switch is driven onto the Z8 data bus. In addition to the address switch status, NDAC (Not Data Accepted) and GET (Group Execute Trigger) are read via the Switch register.

The NDAC signal comes directly from the HP-IB bus (no transceivers in line), and is used by the Z8 to determine if outbound data has been accepted. Data has been accepted when the signal is high.

The Group Execute Trigger (GET) signal is sent to all devices in the system. If a device (such as some voltmeters) understands GET, that device will perform a function receives the trigger. In this manner, several devices can be triggered simultaneously on the bus. The HP-IB chip detects the trigger signal, and outputs a 60 nsec (minimum) pulse on TRIG, which is sent to the edge input of a D flip-flop (U85, 1-B15, 7-2). The output of this flip-flop is buffered through the Switch register and is used by the Z8 to determine if a GET signal has been received from the HP-IB chip. The GET:CLR signal from the Z8 (1-B12, 7-2) clears the flip-flop after it has been read.

Z8 Control Signals

The Z8 is driven to its maximum clock frequency with a TTL clock oscillator (U95, 1-G12, 7-2) running at 8 MHz. The Z8 is reset by only one signal: the BIC RESET- line (1-C11, 7-2). This line goes true if power is cycled to the host computer, an IFC signal is issued, or an addressed device clear is issued to the HP-IB card. When the Z8 is reset, it begins executing code at location 0C (hex), and the following conditions exist:

* Port 2 lines are defined as inputs (floating)
* Port 3 lower four bits are inputs, upper four bits are outputs
* Ports 0 and 1 are defined as inputs (floating
* Memory cycle timing is normal (instead of slow)
* Stack is internal

NOTE

All Z8 inputs are high impedance (maximum +/- 10 uA, 0V - 5.25V), which is essentially floating.

To initialize the Z8 on the HP-IB card, RESET- must be held low for

50 msec after power is applied and is within the supply tolerance,

or

5 usec after power and clock have stabilized.

This means that the RESET- due to Primary Power On (PPON) must be 50 msec, and other RESETs due to Interface Clear (IFC) or Device Clear (DCL) can be 5 usec long (assuming they occur after power-up). While RESET- is held low, the Z8 should be driving a low on Data Strobe (DS-), and a square wave (4 MHz, or half the Z8 input frequency) on Address Strobe (AS-).

Address Strobe (AS-) and Data Strobe (DS-) clock address and data information, respectively. Addresses on port 1 (lower byte) and port 0 (upper byte) are valid on the rising edge of AS- (1-B12, 7-2). Outbound data is valid on the rising edge of Z8DS- (1-E13, 7-2). Incoming data is latched on the rising edge of Z8DS-. An HP 1610B Logic Analyzer can monitor all Z8 activity using the rising edge of AS- to clock the 16-bit address, and the rising edge of DS- to clock the 8-bit data.

The Z8RD signal (1-D13, 7-2) specifies whether the Z8 is reading from or writing to the 8-bit internal data bus.

SEND:ATN, SEND:EOI, LAST:EOI, and LED:ON Interface Signals

The SEND:ATN and SEND:EOI signals (1-E13, 7-2) are used by the HP-IB chip on host writes. The SEND:ATN signal is asserted by the Z8 before writing command sequences to HP-IB peripherals, as a means of selecting devices to talk or listen. In addition, the signal is used to send special commands which inform peripherals to go into local or remote mode, take control of the bus, clear themselves, etc.

The SEND:EOI signal (1-E13, 7-2) enables the END- line to generate an EOI signal on the HP-IB bus. The EOI and ATN control signals go into the ninth and tenth data bits of the HP-IB chip FIFO register. The HP-IB chip outbound FIFO reserves these bits to specify ATN or EOI on the HP-IB bus.

The LAST:EOI- signal is derived from NDAC and EOI- and allows the Z8 to distinguish between an inbound "Line Feed" character and a "Line Feed" character with EOI true.

When reading data, the HP-IB chip sets IB:D0 and IB:D1 true when a "Line Feed" occurs, or when any character with EOI true occurs. Both of these conditions are considered "end-of-record" terminating conditions, and the HP-IB chip treats them identically.

The DMA controller has been programmed to sense when IB:D0 and IB:D1 are simultaneously true. When this occurs, DMA is halted and the Z8 is interrupted. The Z8 polls IB:D0 and IB:D1 and recognizes that one of the two possible "end-of-record" conditions has occurred.

The LAST:EOI- signal allows the Z8 to distinguish between the two types of "end-of-record" terminations by polling LAST:EOI- when it polls IB:D0 and IB:D1. LAST:EOI- low means the last byte transferred across HP-IB had an EOI attached to it.

This distinction is required when reading data from instruments that use LF and LF with/EOI as two different levels of termination. The great majority of HP-IB applications do not require this distinction.

The LED:ON signal (1-C13, 7-2) lights the LED on the HP-IB card. When the Z8 is reset, pin P23 (LED:ON) is made an input to the Z8, and the external pullup forces the LED on. When the reset line is released, the Z8 begins initialization (and self-test, if invoked) which will eventually turn the LED off.

Interrupts

The Z8 microcomputer has eight sources of interrupts, four of which are implemented on the HP-IB card. Each interrupt input is negative edge-triggered, with the minimum pulse width of the interrupt equal to 100 nsec.

The four interrupts are:

HP-IB Interface Clear (IB:IFC- signal). When the HP-IB is not the System Controller, an interrupt occurs when the System Controller asserts IFC.

BIC Interrupt (BIC:INT- signal).

HP-IB Chip Interrupt (ABI:INT- signal).

DMA Interrupt (DMA:INT- signal). This interrupt informs the Z8 of an END condition on a host read.

Interrupts 2 (BIC:INT-) and 3 (ABI:INT-) are continuous-edge interrupts. That is, as long as the device is interrupting, a clock (3.6864 MHz) will generate negative-going interrupt edges to the Z8. With this technique, the Z8 can detect any interrupts that may have occurred when interrupts are disabled. When the Z8 re-enables interrupts, the edges will continue to occur until the specific interrupting condition is acknowledged. The interrupt clock is the system clock (14.7456 MHz) divided by four. This provides a period of 271 nsec, or a half-period of 135 nsec, which is 35 nsec more than the interrupt inputs require.

Interrupt 4 is the DMA interrupt, informing the Z8 of an END condition on a host read. By interrogating the HP-IB chip, the Z8 can determine why the DMA interrupt occurred (end-of-record, end-of-subgroup, secondary address, or end-of-count).

DIRECT MEMORY ACCESS INTERFACE

The DMA controller (U45, see 1-E15, 7-2) is a single-IC synchronous logic array (Monolithic Memories Incorporated HAL16R8) with eight inputs and eight outputs. The DMA controller allows the HP-IB chip and BIC chip to converse over the internal data bus at high speed. The Z8 microcomputer controls the DMA controller via five signals: DMA:PAUSE, DMA:RST, DMA:READ, BUCKET, and EOC.

An algorithmic state diagram of the DMA controller operation is shown in Section VII, figure 7-3. Refer to this diagram, as well as the schematic diagram (figure 7-2) when reading the following paragraphs.

The DMA:RST signal (1-F13, 7-2) resets all DMA controller flip-flops when latched through U35 on the rising edge of CCLK-. This is the way the Z8 initializes the DMA controller.

The READ signal (1-F14, 7-2) controls the DMA direction (host read or host write) of the DMA controller. (READ true = host read, READ false = host write.)

The PAUSE signal (1-F14, 7-2) provides a means of terminating DMA without losing data. The DMA controller completes transfers before monitoring PAUSE. If PAUSE is true, a new DMA cycle is not started until PAUSE goes false. This means that several hundred nsec may pass after PAUSE is asserted before the DMA controller actually pauses (if PAUSE is asserted just after teh Z8 has begun a new DMA cycle). Because each Z8 instruction takes approximately 1 usec to execute, the DMA controller will have paused by the time the Z8 executes its next instruction.

The BUCKET signal (1-E13, 7-2) causes the DMA controller to perform a DMA read out of the HP-IB chip, but the data is not passed to the BIC. This allows the Z8 to monitor END conditions on device-to-device transfers.

The SEND:EOI-/EOC signal (1-E13, 7-2) performs two functions:

When writing, the signal is SEND:EOI for End Or Identify,

When reading, the signal is SEND:EOC for End On Count.

The signal can be used for EOI and EOC because the DMA does not monitor the signal during a write (thus EOC is meaningless), and the IB:D0 signal is disabled during a read (thus EOI is meaningless).

If the HP-IB card is performing a counted transfer of 256 bytes or less, EOC should be true, indicating to the DMA controller that a device end (END-) is needed when the DMA controller detects an end-of-count from the HP-IB chip. The Z8 is interrupted when an enabled end-on-count condition occurs. For counted transfers of more than 256, the Z8 still needs to be interrupted on end-on-count condition, but the DMA controller will NOT generate END- because the Z8 will be ready to start another 256-byte counted transfer. Therefore, in this case, EOC is set false, disabling the end-on-count device end. When the last 256 (or less) bytes of an extended counted transfer are ready to be transferred, the Z8 re-enables EOC before starting another DMA cycle.

Of the DMA controller's eight outputs, two (ODD, via the Odd/Even flip-flop, U85, 1-F17, 7-2; and DMA:INT-) go to the Z8. The ODD signal is a 1-bit counter that keeps track of whether an odd or even number of bytes has been DMA transferred. The Q- output of the Odd/Even flip-flop is connected to the D input, forming a toggle flip-flop that changes state on each rising edge of DTR-. The ODD signal is only used by the Z8 on host reads. The Odd/Even flip-flop is reset by the DMA:RST (1-F13, 7-2) command from the Z8. If the host is reading data in word mode, it needs to know if the last word read contains one or two bytes. If ODD is true, the host is informed that the last word is only half full, or one byte.

See the paragraph "Interrupts" for a description of the DMA:INT signal. Briefly, this interrupt is a means of calling attention to certain end conditions that may be generated by a peripheral on a host read.

The C:END- bit from the DMA controller is enabled by the EN:END- signal (1-E13, 7-2) from the Z8. When the DMA controller senses an end condition during a host read, it interrupts the Z8 and drives C:END true. This line is connected to the enable line of a 3-state driver (U25, 1-E15, 7-2). The input to the driver is EN:END-. This effectively peforms an inverting NAND function (END- true only if EN:END- true and C:END- true). The EN:END- signal is set up before DMA begins, and the 3-state enable line going true (low) controls the state of END-. If EN:END- is true, it takes 25 nsec to pull END- low from the leading edge of C:END-.

In addition to the control inputs from the Z8, described in the preceding paragraphs, three other inputs (IB:D0, IB:D1, and READY) are provided for the DMA controller.

The IB:D0 and IB:D1 signals are the two extra HP-IB chip bidirectional data bits (bits 9 and 10). In the host write direction, these signals specify ATN and EOI data. In the read direction, the DMA controller uses them to detect the following END conditions:

IB:D0	IB:D1	CONDITION
0	0	No end condition (normal data)
0	1	Last byte of record
1	0	Last byte of subgroup
1	1	Secondary address

If one of the end conditions occurs, the DMA controller will halt and assert DMA:INT-, which informs the Z8 of the end condition. The Z8 can interrogate the HP-IB chip to determine the cause of the DMA interrupt.

READY is a composite signal which indicates that both the HP-IB and BIC chips are ready to transfer a data byte (= IOEND- * DMARQ * RDY). The READY, DMA:PAUSE, DMA:RST, and DMA:READ signals are double buffered, because they are asynchronous inputs that are monitored by the DMA controller at any given moment. The other inputs to the DMA controller are also asynchronous, but are guaranteed not to change once the DMA cycle begins.

Refer to quadrant A31 of figure 7-3. Regardless of the current state, a RESET input will force state 04 hex (all states are pin 12 = LSB, pin 19 = MSB). State 04 asserts RST:ACK (Reset Acknowledge), which resets the Odd/Even flip-flop. Once RESET is released, the card idles, waiting for PAUSE to be de-asserted and for READY to become true. When both of these conditions exist, the DMA controller will begin a DMA cycle in the direction specified by READ. Note that READ must be stable before PAUSE and RESET are made false.

The DMA controller will now perform a DMA read or write, and is in "free run" mode. The DMA cycle is running independent of the HP-IB chip, BIC, or Z8 (except for the RESET input) until the byte has been transferred. The READY signal has guaranteed that there is room in the appropriate HP-IB chip and BIC FIFO registers, so the transfer should never "hang up". The read and write cycles are tailored to meet the worst-case timing of the BIC and HP-IB chip. Refer to figures 3-1, 3-2, 3-3, and 3-4.

DMA Write

A DMA write timing diagram for the DMA controller is shown in figure 3-5. In the host write direction, the DMA controller must first extract data from the BIC. It does this by asserting DTR- in state 20 (see figure 3-5). BIC timing dictates that data from the BIC can be delayed as much as 200 nsec following the assertion of DTR-, thus DTR- must be held true for three states (68 nsec x 3 = 204). Q0 and Q1 are used in states 21 and 22 as wait qualifiers, thus the DMA controller can leave DTR- asserted and still distinguish between states. After the 200 nsec wait, IOGO- is asserted to inform the HP-IB chip that there is valid BIC data on the bus. The HP-IB chip timing needs 150 nsec to accept the data, so IOGO- is held asserted for three states. During the last of these three states, DTR- is released, because the BIC can only remove data within 20 nsec maximum. This allows the BIC FIFO register one extra state to recover and become ready for the next DMA transfer. This completes a DMA write cycle, and the DMA controller returns to the IDLE loop and waits for the READY signal.

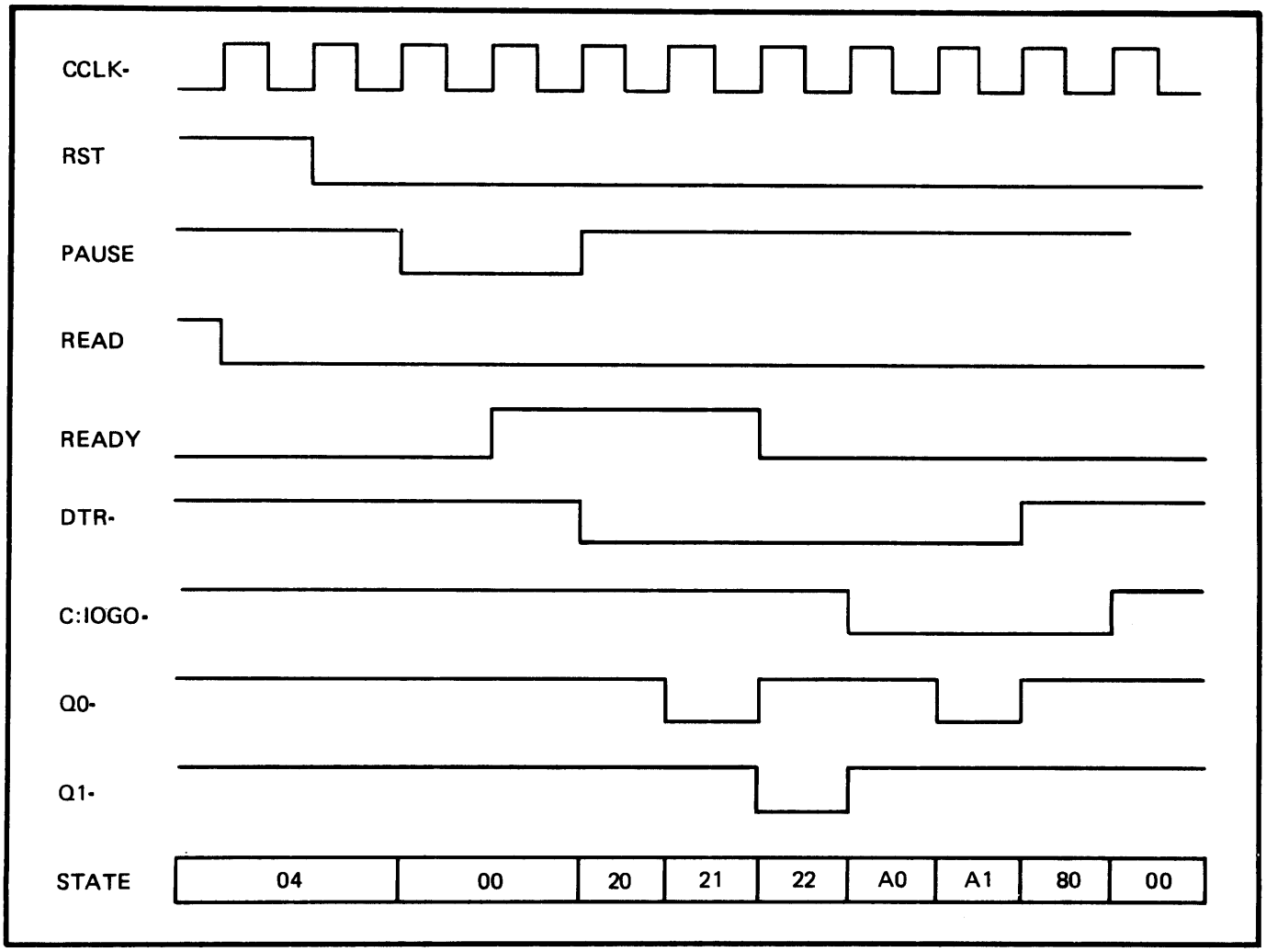


Figure 3-5. DMA Controller Host Write Timing

Refer to the BIC DMA write timing diagram (figure 3-2). The timing values are defined as shown below (recall that RDY- is asserted by the BIC and DTR- is asserted by the DMA controller. DATA is supplied by the BIC).

t1: RDY- assertion to DTR- assertion

The BIC requires that this time be no less than zero. Because RDY- is combined with HP-IB chip signals, synchronized with CCLK, and then input to the DMA controller which again samples it at CCLK-, a non-zero time can be guaranteed (RDY- is gated and double-buffered).

t2: DTR- assertion to RDY- removal

t3: DTR- removal to RDY- assertion

The BIC can become ready as quickly as 40 nsec after removal of DTR-. Because the first six bytes into an empty FIFO will have about 150 nsec each (900 nsec total), time t3 is not critical to DMA operation.

t4: DTR- assertion to DATA

The BIC provides data to the internal data bus within 0 to 200 nsec after DTR- is asserted.

t5: DTR- removal to data float

The BIC releases the data bus within 130 nsec of DTR- removal.

t6: Data hold time from DTR- removal

The BIC keeps valid data on the data bus for at least 20 nsec after the removal of DTR-. The t5 timing allows 130 nsec maximum for t6.

DMA Read

A DMA read timing diagram for the DMA controller is shown in figure 3-6.

A DMA read shares the same idle loop as a DMA write. The DMA controller must first extract data from the HP-IB chip on a read. It does this by asserting IOGO-. When data is being written to the BIC, as in a DMA read, the BIC latches the data on the trailing edge of DTR-; thus, DTR- can be asserted now, and removed (de-asserted) once the data is on the internal data bus. State A8 in figure 3-6 demonstrates this.

The IOGO- signal must be held true for 140 nsec (three states) to allow the HP-IB chip time to drive data. IOGO- is asserted and an internal 2-bit counter is started to count off two wait states. (Asserting COUNT starts the counter.) States A8 through AA show DTR- and IOGO- asserted and the counter running.

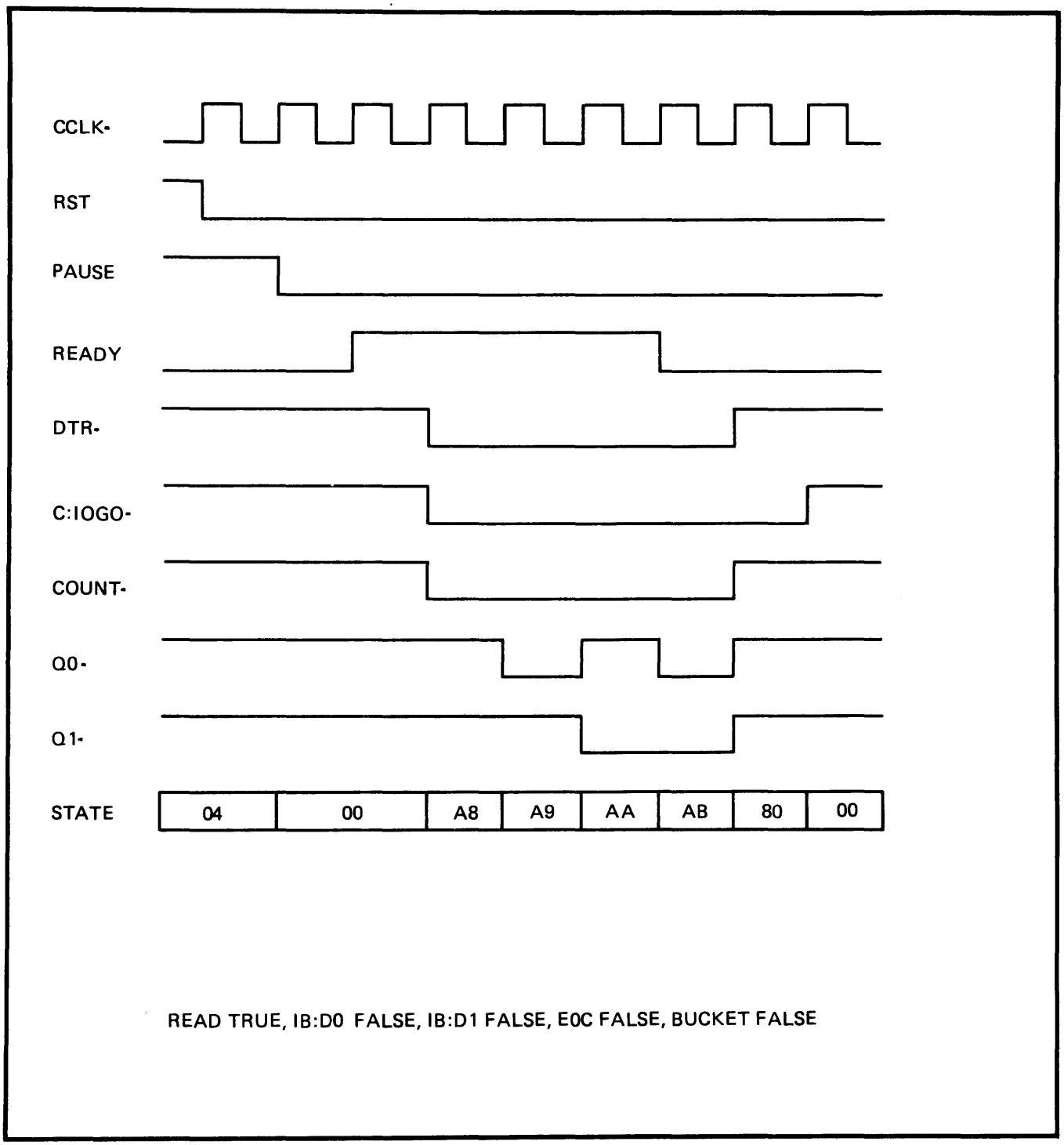


Figure 3-6. DMA Controller Host Read Timing

After state AA, the HP-IB chip data is on the bus, and DTR- can be removed, allowing the BIC to latch the data. The BIC has a data setup time of 20 nsec. Because data is guaranteed 140 nsec after IOGO-, a delay of three states (3 x 68 = 204) is implemented, thus giving the BIC at least 60 seconds of setup time. State 80 shows the DMA controller removing DTR- while continuing to drive the data bus. Because the BIC needs the data to remain on the bus for 45 nsec after removal of DTR-, state 80 guarantees that 68 nsec (one state) of hold time will be provided.

After state 80, the DMA controller returns to its idle loop. Beginning at state 00, the HP-IB chip needs 140 nsec to "float" the data bus (return it to neutral with no data passing in either direction). Because it takes several microseconds to initiate a write cycle, BIC data cannot collide with HP-IB chip data.

Refer to the BIC DMA read timing diagram in figure 3-1. The timing values are defined as follows (recall that RDY- is asserted by the BIC and DTR- is asserted by the DMA controller. DATA is provided by the HP-IB chip.):

t1: RDY- assertion to DTR- assertion

The BIC requires this time be no less than zero. Because RDY- is combined with HP-IB signals, synchronized with CCLK-, and then input to the DMA controller which again samples it at CCLK-, a non-zero time is guaranteed (RDY- is gated and double-buffered).

t2: DTR- assertion ot RDY- removal

t3: DTR- removal to RDY- assertion

The BIC can become ready as quickly as 40 nsec after removal of DTR-. Because the first six bytes into an empty FIFO will have about 150 nsec each (900 nsec total), time t3 is not critical to DMA operation.

t4: DATA setup time (before DTR- is removed)

The BIC requires that the data from the HP-IB chip is prese nt on the data bus at least 20 nsec before DTR- is de-asserted. Because the HP-IB guarantees that it can drive the data bus within 150 nsec of the time when IOGO- is set true (asserted), IOGO- needs to be asserted for 170 nsec before DTR- can be removed.

t5: DTR- removal to data float

The BIC has a hold time on data of 45 nsec, and the fastest that the HP-IB chip can remove data from the bus following the de-assertion of IOGO- is 25 nsec. Therefore, IOGO- (and DATA) need to remain asserted 20 nsec following the removal of DTR-. This is accomplished via state 80.

PROGRAMMING

SECTION IV

This section contains firmware information for the HP-IB interface card. The information contained in this section will help you when programming the host computer system to control the HP-IB card.

The HP-IB card supports high-speed and standard-speed devices using a transaction protocol with the host computer system. Additionally, the card may function as a device, Controller in Charge (CIC), or System Controller (SC).

COMMANDS SUPPORTED

The HP-IB card interfaces to the host using CHANNEL I/O Level 2 Control, Data, and Status messages to construct "transactions". Thus a "transaction" is a command, and the execution and reporting messages associated with it. Refer to the appropriate computer system reference manual for a discussion of CHANNEL I/O Level 2 protocol.

Summary of Controls, Commands, and Orders

WRITE CONTROL OPERATION (WR CNTL) CONTROL BYTE

Control Byte	7	6	5	4	3	2	1	0
			DCL	DEN	NMK	RQA	ARE	ARD

Bit	Mnemonic	Name
0	ARD	Attention Request Disable
1	ARE	Attention Request Enable
2	RQA	Request Attention
3	NMK	Non-Maskable Interrupt Acknowledge (not supported)
4	DEN	Device Enable
5	DCL	Device Clear
6		Not supported
7		Not supported

The card will accept and discard (thus effectively terminating) controls which are not supported.

WRITE COMMAND (WR CMD) OPCODES

Opcode	Mnemonic	Name
0	DSC [subch]	Disconnect Subchannel and abort transaction, if any
1	AEK [n]	Asynchronous Event Acknowledge n
2	CSC [subch]	Connect Subchannel
3		Not supported
4	RSC [subch]	Resume Subchannel and the transaction in progress in that subchannel
5 - 15		Not supported

The opcode is in bits 7:4 of the command byte.

The card will accept and discard (thus effectively terminating) commands which are not supported.

WRITE ORDER (WR ORDER) OPCODES

Opcode	Mnemonic	Name
0	IDY	Identify
1	DLD [b]	Download (not supported)
2	PAU	Pause
3	DIS	Disconnect
4	RS [b]	Read Status
5	WC [b]	Write Control
6	RD [b]	Read Data
7	WD [b]	Write Data
8	RTS	Read Transparent Status (not supported)
9	WTC	Write Transparent Control (not supported)
10 - 15		Not supported

The opcode is in bits 7:4 of the order byte.

If an order which is not supported is received by the card, the card will accept and discard the order and associated data. If an order which is supported is received when not expected, the card will terminate the data portion of the order with DEND (Data End) at the first chance (if the order is a host read, a garbage byte will be sent), the card will then set the Transaction Status, TSTAT, (see "Transactions" paragraph for detail) and terminate all orders until the RS[b] Order is received and status is sent to the host.

Attention Request (ARQ) Mechanism

All Attention Requests (ARQs) must be acknowledged before further ARQ causing events can be reported or enabled.

The HP-IB card will post CHANNEL I/O Level 2 status bytes (the kind that enable the Level 1 ARQ line) in response to certain Level 1 control and command operations as outlined in the host computer reference manual. In addition, the card asserts ARQ (responds to ARQ polling) and presents an AES (Asynchronous Event Sensed) status byte as a way of telling the host that a desired event or state occurred (refer to the "Reason for Interrupt" paragraph)

There is a one-to-one correspondence between unacknowledged ARQs and posted status bytes. An acknowledged ARQ is one that the host detects, and eventually responds to by reading the corresponding status byte via the CHANNEL I/O read_status operation.

Posting Status Bytes

The following paragraphs describe how the card's microprocesser (Z8) interacts with the BIC (Backplane Interface Circuit) to handle ARQ generating situations, i.e., posting of status bytes.

The BIC allows posting of only one status byte at a time. There are three signals in the BIC associated with Attention Request: SRE, RQA, and CMD. Depending upon the BIC Interrupt Mask register, these signals may cause interrupts to the microprocessor; in addition, they can always be polled. (These signals are expressed as bits in the BIC Interrupt register, which may be read by the Z8 microprocessor at any time.)

SRE. The SRE (Status Register Empty) signal tells the microprocesser that the status register in the BIC is empty, i.e., the host removed the last status byte via read_status, or there never was a status byte present. In this state, the microprocesser is free to post a status byte which, in turn, enables the ARQ logic in the BIC.

The deassertion of this signal indicates that the status register is NOT empty i.e., an unacknowledged status byte is still present.

RQA. Request Attention (RQA) assertion indicates that the host issued a write_control operation with the RQA bit set. The CHANNEL I/O specified response to this is to assert ARQ and supply a status byte of RFC (Ready For Command).

CMD. CMD assertion indicates the presence of a command byte in the BIC's Command Byte register (the result of a write_command operation).

The microprocesser sequence for ARQ control is as follows:

The powerup and idle state of SRE is active, i.e., the status byte port is available. The SRE interrupt is disabled to prevent continuous interrupts. The RQA and CMD interrupts are enabled for interrupting the Z8.

When the need to post a status byte arises, the byte can be immediately posted (thus also enabling the ARQ logic in the BIC). The SRE bit will be inactive until the host does a read_status operation.

In order to return to the idle state without the possiblility of overwriting the pending status byte, the microprocesser "freezes" any process which may be required to post a status byte. The freeze is accomplished by disabling the RQA and CMD interrupts and, in the case where one of the enabled "reason for interrupt" transaction events becomes true, the posting of the AES is qualified by SRE. The SRE interrupt is enabled.

The re-enabling of the RQA and CMD interrupts and the ability to post AES is accomplished when the SRE signal is asserted, i.e., a host read_status operation occurs. The RQA and CMD interrupts are re-enabled and SRE interrupt is disabled in the interrupt service routine (isr) servicing SRE; the idle state is resumed.

The various interrupts are enabled and disabled by the microprocessor writing to the BIC Interrupt Mask register.

EFFECT OF "FREEZE". One write_command may be issued following activation of the card's ARQ logic. The command will not be processed until the status byte port is freed. The reason that commands are not processed when an unacknowledged status byte is present is because some commands require the posting of a status byte.

The write_control operation with RQA asserted may be sent, and will not be lost; however, the response (the RFC status byte) will be backed up behind the unacknowledged status byte. Multiple write_controls with RQA sent during this freeze-out will map onto one RFC status byte.

The AES status byte - posted when an enabled "reason for interrupt" occurs - will be inhibited until the status byte port is empty (SRE becomes true). This is accomplished by the microprocessor polling SRE during idle time.

Error Handling

In the event of an error, all Level 2 messages will be terminated until a Level 2 Status Message response is sent by the card. If a Level 2 Status Message causes an error, recovery will be satisfied if the response is successfully sent to the host. A Level 2 Status Message could cause an error if it was sent to the card when the card was expecting a different kind of Level 2 Message.

The first error detected in any transaction is the only one posted for that transaction; further errors are not logged.

Level 2 Abort Command

Upon receipt of a Level 2 Disconnect Subchannel command, the card will cease activity on the current transaction for the subchannel to be aborted. The indicated subchannel will be disconnected and the Level 2 Status message SCDn will be sent. Up to 14 bytes of data on the card will be lost.

Once the SCDn status is read by the host, the card is in normal state, that is, is ready for a connect and subsequent transaction.

Level 2 Identify Order

The message sent in response to a Level 2 identify order is shown below:

BITS	7	6	5	4	3	2	1	0	
BYTE 1	0	0	0	0	0	0	1	0	id code
BYTE 2	cccc				rrrr				capability (cccc), and revision level (rrrr)

where,

id code = device identity - a code from 0 to 255
cccc = capability code - 0 0 0 0 for the HP-IB card
rrrr = revision level code - 0 0 1 0 for the HP-IB card

Card's Response to PPON, DCL, ABTn, and RST

Reset is a function of the four messages Reset (RST), Primary Power On (PPON), Disconnect Subchannel (DSCn), and Device Clear (DCL). The I/O channel interface and HP-IB bus interface are affected differently by the four messages as outlined below. (The I/O channel response is determined by the BIC.)

PPON causes a complete reset of the I/O channel and HP-IB bus interfaces.

RST causes a complete reset of the I/O channel. The current HP-IB interface transaction, if any, is aborted by RST (with up to 14 bytes still on the card lost). The HP-IB chip is asynchronously pulled offline and the HP-IB card is reset. The Z8 microprocessor performs the card self-test, causing the LED to light, then go out if the card passes self-test.

DSCn aborts the HP-IB transaction. The I/O channel interface is unaffected except that up to 14 bytes (residing in on-card buffers) are lost.

DCL resets all of the I/O channel interface except the device address (DA). (DCL has the same effect as RST except that the DA is not reset.)

The microprocessor is reset by PPON, DCL, and RST.

Note that the HP-IB IFC signal is not asserted until the card is online, is System Controller, and is commanded to assert IFC explicitly via a transaction. That is, IFC is not asserted on power-up.

NRFD

When the card is Controller-in-Charge and PPOLL is disabled and the card is neither sending or receiving data, Not Ready For Data (NRFD) will be asserted. The significance of this is: when the controller addresses one device to talk and another device to listen, the transfer will be blocked by this card's assertion of NRFD.

PPOLL and ATN

The assertion of ATN during idle time is a function of whether PPOLL is to be asserted.

Normally, the ATN signal is not asserted during idle time except in the following cases:

1. A PPOLL interrupt has been enabled.
2. The last HP-IB message sent by the card was an interface message.
3. The assert ATN transaction is invoked.
4. The last transaction was one which leaves ATN asserted.

The ATN signal will be deasserted in the following cases:

1. Last HP-IB message sent by the card was a data message.
2. The deassert ATN transaction is invoked.
3. The card is reset (PPON, DCL, or RST).
4. The card is not System Controller and an IFC message is received.
5. The card sends a TCT (Take Control) message.
6. The last transaction was not one which leaves ATN asserted.

DEFAULT AND POWER ON CONFIGURATIONS

Offline/Online

Following a power on, the HP-IB card will be offline from the HP-IB bus. This means that it will not interact with the HP-IB bus in any way. The card will go online upon receipt of a "Go Online" transaction. Once the card is online, it will go offline if another reset is done.

The control of online timing allows you to configure the card for activities if different from the default - e.g., PPOLL sense - before the critical action of going online.

Note that when offline, the HP-IB chip has System Controller status regardless of the switch setting. This enables diagnostics to be run against the HP-IB chip without affecting the HP-IB bus.

REN and IFC

If the card comes online as System Controller, the REN (Remote Enable) signal will be deasserted by the card until explicitly controlled. Similarly, the IFC line is not pulsed until explicitly controlled by a transaction.

The IFC signal is required before a card configured as the System Controller can assume the role of Controller-In-Charge (this also applies to offline access).

TRANSACTIONS

Concept

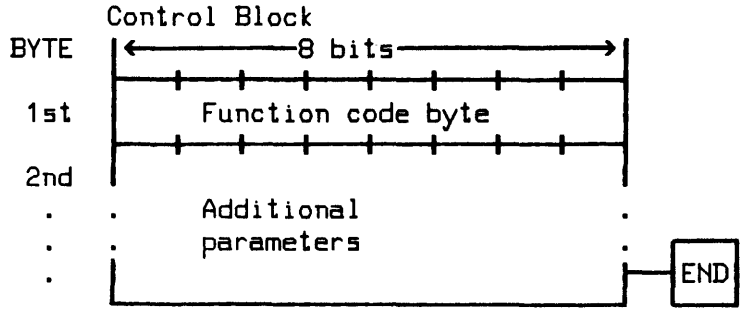
Transactions are the standard way of communication between the host and the HP-IB card. Each request to the card is called a transaction and has a standardized format. It represents a single driver request (Read or Write Data; Read or Write Configuration or Status; and Control device or card).

Each transaction is composed of three parts; Control Block, Data Block, and Status Block, CDS. These correspond to the three CHANNEL I/O Level 2 Interactions: Control, Data (referred to below as either Read or Write), and Status. All transactions are composed of three parts except transactions which have no data to send or receive, and thus will have no data part (C-S).

Control Block

The Control Block informs the card what type of request (Read, Write, etc.) is to be performed. Additional information in the form of request subfunctions and parameters is also provided by the Control Block.

The format of the Control Block is as follows:



The function code byte is provided to tell the card what type of request is being made. The values of the function code are divided into groups. The function codes and their corresponding meanings are tabulated in the following paragraphs.

Function Code

Overview of Function Code Byte

11 HP-IB Data Transfer	0	0	data	read/ write	check CRC	read/ write
10 CS/80	0	0	data	read/ write	check CRC	read/ write
10 MAG TAPE	1	0	data	read/ write	check CRC	read/ write
01 reserved	reserved					
00 General	opcode					

NOTE

CS/80 refers to the Hewlett-Packard Command Set '80, which is an HP protocol for commands used in controlling devices such as tape or disc drives.

GENERAL TRANSACTIONSs. Opcodes and descriptions of general transactions are shown in table 4-1.

Additional Parameters

Any additional parameters needed by the HP-IB card to complete the request follow the function code byte. Because the block is of variable length, there is no absolute restriction on the number of parameters; however, the card will only accept and process relevent parameters, and will assert DEND (Device End) to terminate the transfer of excess parameters.

If the block is terminated by the host before sufficient bytes for the request are received, the missing bytes will be interpreted as having a zero value. The fact that the host did not supply the missing bytes will not be apparent to the card. This allows the host to terminate the buffer on the last non-zero byte.

Table 4-1. General Transactions

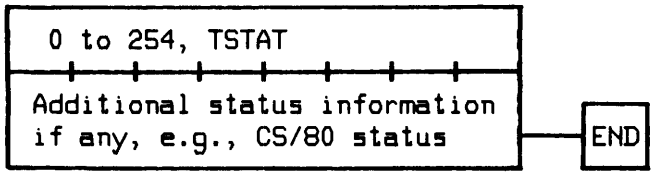
OPCODE (hex)	DESCRIPTION
0	Reserved
1	Set REN (Remote Enable)
2	Clear REN
3	Send IFC (Interface Clear)
4	Configure card's PPOLL (Parallel Poll) Response
5	Read card's PPOLL Response configuration
6	Configure card's SRQ response / SRQ
7	Read reason for interrupt
8	Write interrupt mask
9	Read interrupt mask
A	Wait for interrupt conditions
B	Go online
C	Go offline (use not recommended)
D	Assert ATN
E	Deassert ATN
F	Configure bus PPOLL sense
10	Conduct PPOLL and read response
11	Configure HP-IB address
12	Read HP-IB address configuration and current status
13	AMIGO* Identify configuration
14	Last secondary address
15	Enable freeze on interface message parity failure
16	Disable freeze on interface message parity failure
17	Reserved
.	.
.	.
.	.
3F	Reserved

* - AMIGO is a Hewlett-Packard term for a particular implementation of HP-IB.

STATUS BLOCK

The Status Message is the last Level 2 interaction of a transaction. The Status Block is read into the host at the end of a request to inform the driver how the request went. The TSTAT (Transaction Status) value of the Status Block is basically an "OK" or "not OK because..." message summarizing the transaction results, and may also contain additional information about transaction termination conditions.

Status Block



As with the Request Block, the Status Block may be terminated "early" by the host.

TSTAT

The TSTAT (Transaction Status) provides status information regarding the request. The meaning of a particular value of TSTAT is the same for all transactions. Some meanings, however, are not applicable to all transactions and thus will never be returned for those transactions. The TSTAT values and their meanings are presented in table 4-2. The range of the values is 0 to 254. The value 255 is not used.

TSTAT will reflect the first failure detected in the most recent transaction, or may indicate terminating conditions, or will indicate no exceptional conditions.

Table 4-2. Transaction Status Summary

TSTAT (hex)	DESCRIPTION
00	No exceptional conditions. (Does not mean QSTAT = 0) (QSTAT is a one-byte message indicating the success or failure of the CS/80 transaction.)
01	Read transaction was terminated by EOI
02	Read transaction was terminated by EOI. Count was odd.
03	Read transaction was terminated by count
04	Read Transaction was terminated by count. Count was odd.
05	Read Transaction was terminated by LF
06	Read Transaction was terminated by LF. Count was odd.
07	Read Transaction was terminated by MSA
08	Read Transaction was terminated by MSA. Count was odd.
09	Transaction was terminated by host - data transfer to host was terminated by CEND instead of DEND
0A	Transaction command code not supported by the card
0B	Transaction requires card to be SC and it is not
0C	Transaction requires card to be CIC and it is not
0D	Transaction requires card to not be CIC and it is
0E	Transaction requires card to be either addressed or not CIC (so another device can address it) and it is not
0F	Unexpected Level 2 Message has arrived since last Level 2 Status Message
10	HP-IB DCL was detected during a data transfer
11	IFC abort of data transfer
12	Card failure due to card causing HP-IB chip "processor abort"
13	Card failure due to illegal DMA interrupt
14	Card outbound data frozen due to presence of inbound data on the card (only occurs when card is not CIC)

Table 4-2. Transaction Status Summary (Continued)

TSTAT (hex)	DESCRIPTION
15	CRC error occurred
16	Reserved
17	Can't be performed because PPOLL interrupt is enabled. Can be returned in response to a set ATN false transaction.
20	The data portion of the CS/80 command buffer was missing from the WC command buffer
21	End of a FIFO disabled transfer occurred with an EOI on the last byte and the count ran down at the same time
22	End of a FIFO disabled transfer occurred with an EOI on the last byte and the count was odd
23	End of a FIFO disabled transfer occurred with an EOI and a LF
24	End of a FIFO disabled transfer occurred with an EOI and a LF and the count was odd
25	End of a FIFO disabled transfer occurred with an EOI on the match byte
26	End of a FIFO disabled transfer occurred with an EOI on the match byte and the count was odd
27	End of a FIFO disabled transfer occurred with a match byte
28	End of a FIFO disabled transfer occurred with a match byte and the count was odd
29	A write transfer was terminated by a byte arriving in the card's inbound FIFO when the card was not the CIC

Table 4-2. Transaction Status Summary (Continued)

TSTAT (hex)	DESCRIPTION
2A	A read or write was terminated by the card receiving a DCL or SDC when the card was not the CIC. For reads, an extra byte is sent to the host in order to terminate the transfer. This byte is counted in the odd/even sense of the status.
2B	A read was terminated by the card receiving a DCL or SDC when the card was not the CIC and the byte count was odd. An extra byte is sent to the host in order to terminate the transfer.
2C to FD	Reserved
FE	No status available. This status is set upon receiving a function byte, and indicates that the card did not complete the transaction but no error was detected. This value will also be set upon reset and power on.

INDIVIDUAL TRANSACTION DESCRIPTIONS

Send Interface Clear (IFC Line Asserted For 100us)

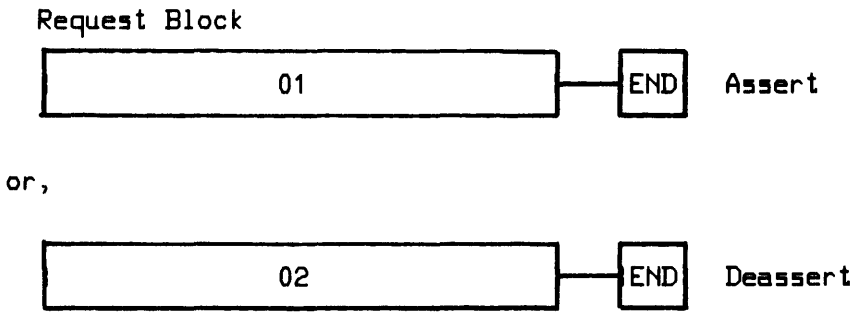
Request Block

If the card is the System Controller, the IFC line is asserted for at least 100 usec. The card delays the response to the Level 3 Status message until IFC is complete.

If the card is not the System Controller, an error will be returned.

The IFC signal is NOT asserted in response to PPON, IFC, or DCL; nor is it asserted when "going online".

Remote Enable (REN)

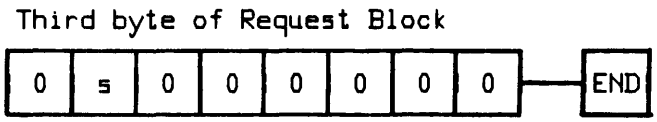


If the card is the System Controller, the REN line is asserted, or deasserted as directed by the opcode. The card will not assert SRQ for the Status Order until 100 usec after the REN line is changed.

If the card is not the System Controller, an error will be returned.

The default for REN control is "deasserted".

Configure Serial Poll Response & Request Service (SRQ)



s = Request service message.

s = 1: Set SRQ until SPOLL and respond to SPOLL with 40 hex

s = 0: Do not set SRQ and respond to SPOLL with 80 hex

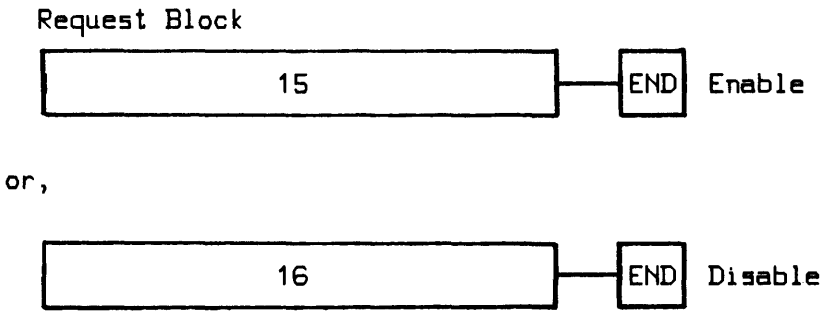
This transaction is used only to the extent of sending or not sending the request service (rsv) message, which in turn controls the assertion of the SRQ line. If request service is true, then <01000000> will be sent as the status byte, otherwise <10000000> will be sent.

The default state is s = 0, that is, send <1000000> as the status byte.

NOTE

This transaction has the same effect whether or not the card is currently the Controller-In-Charge.

Configure Interface Message Parity Freeze

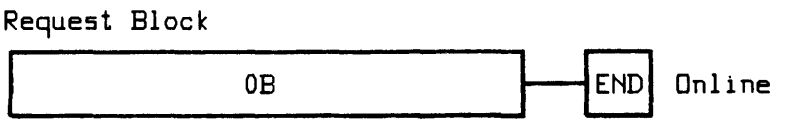


If the function code specifies enable (15), an interface message with bad odd parity will cause the HP-IB chip to refuse to accept or interpret any interface command (including device addresses) that does not have odd parity. This will force the HP-IB to remain frozen with DAV asserted until the HP-IB controller aborts the transfer by removing DAV. This does not affect in any way the parity error interrupt.

If the function code specifies disable, interface messages will be interpreted regardless of parity.

Default is parity off.

Online

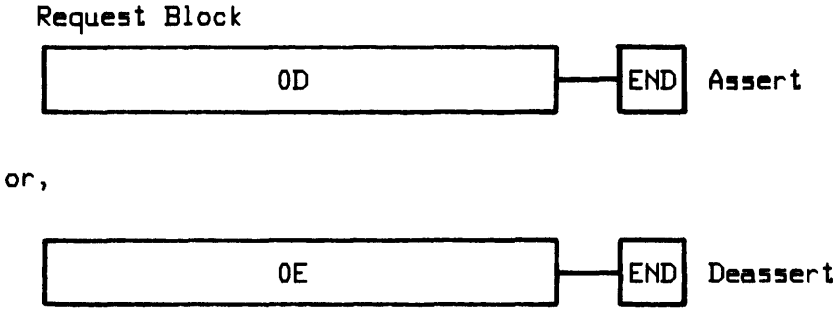


This transaction causes the HP-IB chip to go online the HP-IB bus. When the chip is offline, it does not interact with the HP-IB bus in any way. The default state at initiation is offline.

In order for the card to interact with the HP-IB bus, it must be put online. No special TSTAT value will be returned for any transaction if the chip is offline at the time the transaction is sent to the card.

Because of the nature of IEEE-488, the chip should not be put offline once it is put online.

ATN Control



The ATN signal will be asserted or deasserted as directed by the function code if the card is CIC. If the card is not CIC an error will be returned.

NOTE

These requests give manual control of the ATN line. ATN is also controlled automatically by the card as associated with PPOLL and the interface message portion of a data transfer between the card and an HP-IB device. See the paragraph "PPOLL and ATN" for a further discussion of ATN.

Data Transfer Between Card and Another HP-IB Device

Request Block Function Code

1	1	0	0	data	read/ write	CRC	read/ write

Details of HP-IB data transfer and CS/80 function code bits:

DATA	READ/WRITE	
1	1	Data buffer to host, read from device
1	0	Data buffer from host, write to device
0	1	No data buffer to or from host, "sink" data from device. The "sink" data case supports data transfers in which the host is not addressed to listen or talk.
0	0	No data buffer to or from host, no device data. Last case allows the sending of an interface message without a data message.

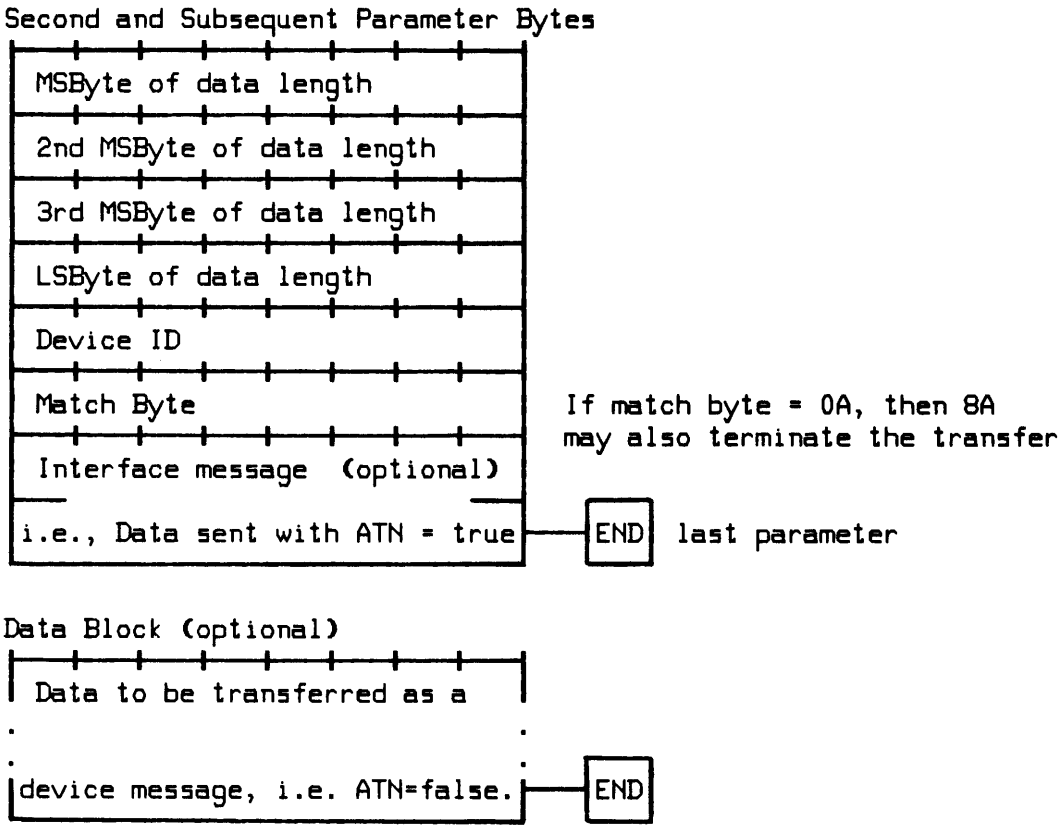
CRC	READ/WRITE	
0	X	No CRC check is done and CRC is disabled.
1	X	Card's CRC is enabled and is left enabled at end of transaction.
1	1	If card is CIC, the CRC is read from the device and compared to the card's CRC using interface messages before the transaction's interface message, and after the transaction's data message. If card is not CIC, nothing more is done.
1	0	If card is CIC, the card's CRC is sent to the other device using interface messages before the transaction's interface message, and after the transaction's data message. If card is not CIC, nothing more is done.

NOTE

To "sink" data is to read and discard the data; that is, the transfer is "allowed" between two or more devices.

First Parameter Byte of HP-IB Data Transfers

0	0	0	0	Match Byte	Count	LF	EOI



The lower bits in the function code control the CRC of the data transfer. The entire transaction may be terminated due to data integrity, i.e., CRC failure. Such a failure is detected outside of the data transfer and is discussed in the following paragraphs.

A transfer may be terminated for reasons other than those specified in the function code. These other reasons include reset of the card by PPON, IFC, or DCL; HP-IB "device clear"; and data in HP-IB chip's inbound FIFO when the card is trying to write data to the bus. The causes of termination are first summarized below and then discussed in more detail.

Outbound data transfer termination reasons and special actions required before next outbound data transfer:

CEND: Normal

DCL: May cause a host interrupt

Inbound Data and card is not CIC: Inbound data must be read. May also cause a host interrupt.

Inbound data transfer termination reasons and special actions required before next inbound data transfer.

CEND: Normal

EOI: Normal

MSA: Normal. May also cause a host interrupt.

Count: Normal

LF: Normal. Last byte may have been either 0A or 8A.

If match is enabled on inbound transfer, the following terminations may also occur:

EOI and Count: Normal

EOI and LF: Normal

EOI and Match: Normal. If match byte = 0A, last byte may have been 8A or 0A.

Match: Normal. If match byte = 0A, last byte may have been 0A or 8A.

This transaction, "Data Transfer Between Card and Another HP-IB Device", optionally sends an interface message out onto the HP-IB bus and optionally sends to or receives from the HP-IB bus a data message. A data message received from the HP-IB bus may be either sent to the host as a Data Block or may be read and discarded by the card.

An MSA (My Secondary Address), arriving during a read device message, will end the data transfer with the byte preceding the MSA. The MSA will also be sent to the host as the last byte sent to the host (if not in "sink mode"). The TSTAT value will be set to "terminated on MSA". If the card receives an MSA but does not read it out of the HP-IB chip inbound FIFO during the current transaction, it will remain in the inbound FIFO until read out by a future transaction. The current transaction in this case would not have a TSTAT of "terminated on MSA". Since data messages are usually terminated with EOI (End Or Identify), an MSA will usually be sent to the host as the first and only byte of a read transaction. A host which is not a CIC can use the MSAs to determine what to do next, for example, read data or write status. The host would therefore do a read data transaction after each data transfer to get the next MSA.

The outbound FIFO of the HP-IB chip will be frozen when any data enters the inbound FIFO from another device. The card will terminate a write data transaction if this occurs. The status returned will be "terminated on inbound byte". The card will clear the outbound bytes from its buffers. The inbound FIFO will not be disturbed. The card will reset (clear) the freeze if commanded by the host, or if a read data transaction leaves the HP-IB chip FIFO empty.

The data length is applicable only when data is being received by the card from the HP-IB, the card is CIC, count is enabled or minimal, and FIFO has been selected. For the host write direction, the data length is not used. The data length is used as the maximum number of bytes to be received from the HP-IB bus by the card. Best HP-IB bus performance occurs when count is not enabled. Lengths in excess of 256 bytes will be subdivided into blocks with length less than or equal to 256 bytes. This subdivision of the data transfer is transparent to the host.

The Device ID is required if data integrity tests are to be performed on the data message. The match byte is used if character match is enabled.

The request block optional data will be sent as an interface message if the card is CIC. The interface message will be forced to odd parity. If the card is not the CIC, and header data is present, an error will be generated and the transaction will be terminated. If the card is CIC and is not appropriately addressed at the time data is to be transferred, an error will be generated.

If the card is not CIC, the card will accept data from the bus up to the limits of its buffers whenever it is addressed to listen. The maximum number of bytes the card may accept beyond what is sent to the host is 14. Normally this limit is eight bytes, as the card will stop the transfer of bytes out of the HP-IB chip when an EOI or MSA is read out of the HP-IB chip.

Data buffers on the card will be cleared under the following conditions:

1. PPON becomes false.

2. The card is CIC and read data transaction is terminated by CEND. Note: Normally at end of read data transactions the buffers will be empty.

3. The card is CIC and Abort n occurs.

4. The write data transaction is terminated by data freeze. In this case, the inbound FIFO is not cleared. The outbound FIFO and the BIC FIFO will be cleared.

5. Self test is invoked.

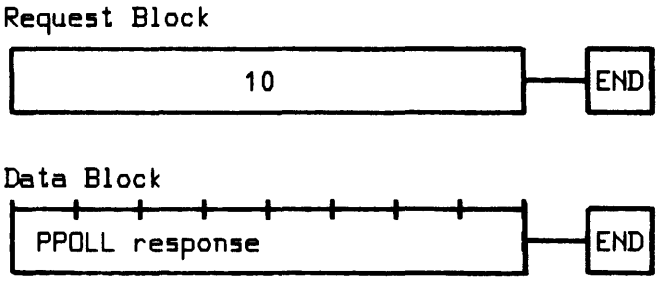
TSTAT informs the host about the transaction data termination conditions or exception conditions. The card will not send a special TSTAT value if it is unaddressed during a data transfer by an interface message. The precedence which will be used to determine the TSTAT value to be returned is shown on the next page.

TSTAT	PRECEDENCE
Error	The first occurrence of any error will determine TSTAT.
IFC	If a transfer is terminated by IFC, IFC will be reported.
Byte	If an outbound data freeze termination occurs, byte termination will be reported.
MSA	The arrival of an MSA will always be reported.
Match	The arrival of the Match byte (or 8A if Match byte is 0A) will be reported ahead of LF.
LF	The arrival of line feed (0A or 8A) will always be reported if termination on line feed is enabled.
EOI	EOI will be reported if EOI occurs and LF termination does not occur.
End on Count	End on count will be reported if the count runs out before any other termination. If count runs out simultaneously with another event, the other event will be reported.

Sending GET, DCL, SDC, TCT, LLO, SPE

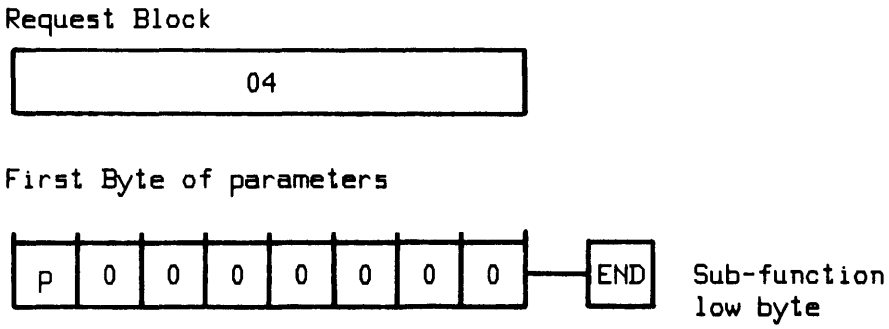
Interface messages, e.g., HP-IB Addressed Commands and Universal Commands such as GET (Group Execute Trigger), DCL (Device Clear), SDC (Send Device Clear), TCT (Take Control), LLO (Local Lock Out), and SPE (Serial Poll Enable) are single byte transactions and are sent with ATN (Attention) enabled. See the paragraph "Data Transfer Between Card and Another HP-IB Device" for further details.

Conduct PPOLL and Read Response



If the card is Controller-In-Charge, a PPOLL will be conducted and one byte of PPOLL results will be returned. The state of the ATN line will be restored to the state it had before this transaction. An error status will be returned if the card is not CIC.

Configure Card's Response to PPOLL



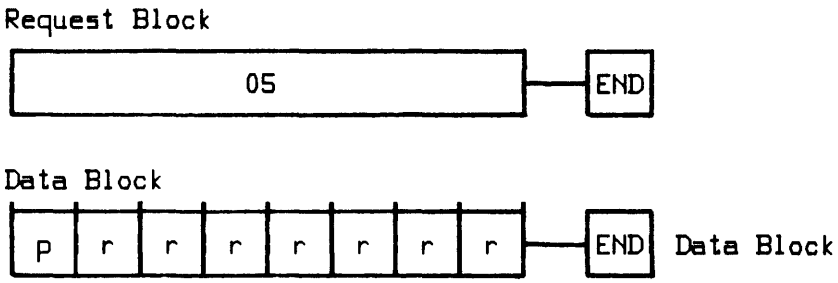
p = 1 Respond to PPOLL.
p = 0 Do not respond to PPOLL. Default configuration.

This transaction will enable the PPOLL response, i.e., the PPR (Parallel Poll Response) message, of the HP-IB card. The configuration of the response of a device other than the card itself is done using the data transfer transaction to send interface messages.

This transaction is executed by the card whether or not it is CIC. If the card is CIC, the card will not respond to PPOLL but the configuration will remain in effect after the card ceases to be CIC.

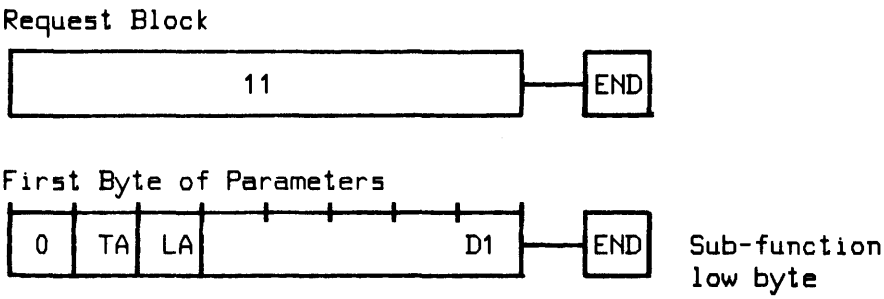
If the card is not the CIC and its address is from 0 to 7, the card will respond to Parallel Polls using the DIO line corresponding to its address. Lines DIO8 through DIO1 correspond to addresses 0 through 7 respectively. If the card has address greater than 7, then its Parallel Poll response must be assigned to it by the CIC.

Read Card's PPOLL Response Configuration



p = 1. Respond to PPOLL
p = 0. Do not respond to PPOLL
r = reserved

HP-IB Address Configuration



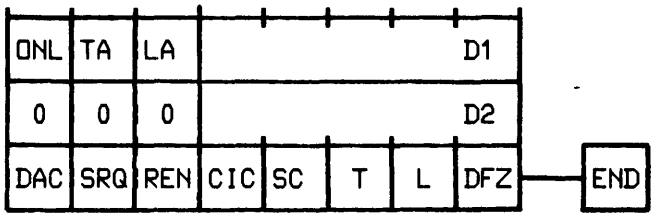
D1 = address with value: 0 - 30
TA = TALK ALWAYS
LA = LISTEN ALWAYS

The address to which the card will respond when it is not CIC is set by this transaction. This transaction will override the address obtained from the card's address switch which establishes the address at reset time. If the host sends an address of 31, an error will be reported. When the card is System Controller, its address is 30 decimal.

HP-IB Address and SC, CIC, TLK, and LTN Read

Request Block

Data Block

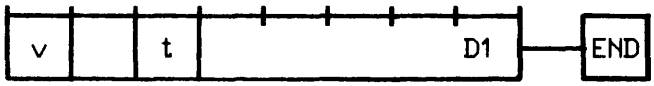


ONL = 1 - Card is online
TA = card is configured to talk always
LA = card is configured to listen always
D1 = card's not CIC address with value 0 - 30
D2 = card's CIC address with value = 30
SC = 1 - Card is System Controller
CIC = 1 - Card is Controller in Charge
T = 1 - Card is addressed to talk or talk always is true
L = 1 - Card is addressed to listen or listen always is true
REN = 1 - Card is in HP-IB remote state, i.e., REN is asserted
SRQ = 1 - SRQ is being asserted on the bus by someone, and card is CIC
DAC = 1 - NDAC is being asserted on the bus by someone
DFZ = 1 - Outbound buffer is frozen because of data in inbound buffer

Last Secondary

Request Block

Data Block

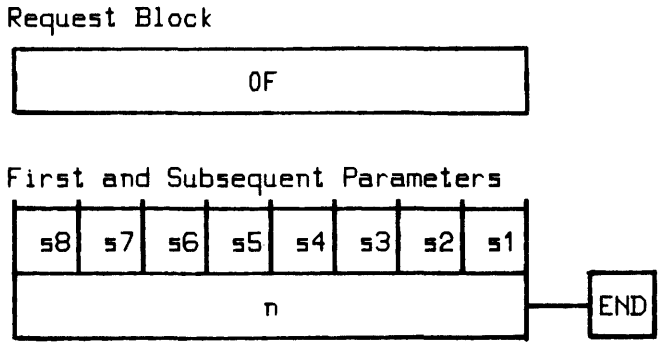


Data Block

```
D1 = 0 - 30 Most recent secondary address
t = 1       Preceding primary address was card's talk address
t = 0       Preceding primary address was card's listen address
v = 1       Secondary address is valid
```

The most recently received secondary address is returned.

Bus PPOLL Sense Configuration




```
s8-s1 = 0 Test is true if corresponding DIO line is 1, i.e.,
          asserted low
s8-s1 = 1 Test is true if corresponding DIO line is 0, i.e.,
          passive high
n =       delay 25*(n**2) usec before reading PPOLL in the
          Bus PPOLL Read RESPONSE transaction
```

The default sense is all zeros, i.e., PPOLL is true if DIO line is true.

The default for n is 1 (25 usec delay).

INTERRUPT TRANSACTIONS

There are four transactions associated with interrupts, as follows:

Write interrupt mask

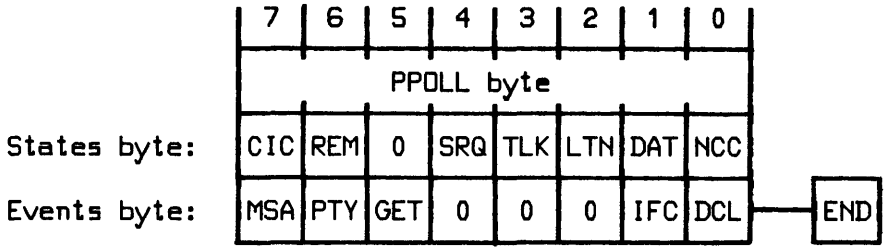
Read interrupt mask

Read reason for interrupt

Wait for interrupt conditions

Format of Interrupt Block

The format of the additional bytes and/or a data block associated with interrupt transactions is:



Write Interrupt Mask

The card interprets the interrupt block in this transaction as enables for host interrupts for those corresponding bits in the block that are ones (1's). If there are one or more bits set in the interrupt block, the card will enable host interrupts.

Read Interrupt Mask

This transaction returns the current enabled interrupt conditions bits in an interrupt block in the data portion of the transaction.

The command interrupt block of a Write Interrupt Mask transaction will match the data block of a Read Interrupt Mask transaction.

Read Reason for Interrupt

This transaction reports a data interrupt block in which the ones (1's) indicate the result of occurred and enabled interrupt conditions. All resetable interrupts reported are reset.

Wait for Interrupt Conditions

This transaction has no affect on the interrupt mask as described in the preceding paragraphs.

The command interrupt block sets conditions upon which the transaction will resume. The transaction will resume when any one of the conditions are met. The data interrupt block will indicate which condition(s) enabled the transaction to resume. The host may also resume the transaction with a RESn command.

The suspension of the transaction is accomplished by preventing the card from issuing SRQ for the CHANNEL I/O Read Data (RD) order until such time as an enabled condition for resumption is detected. The suspend produces the same effect as the CHANNEL I/O pause order (PAUSE).

This transaction has no effect on other interrupt transactions, and the command block parameters only have significance for the life of the transaction.

Events, however, are "consumed" by this transaction. For example, if interrupt on DCL in enabled, then a wait for DCL is issued and the DCL occurs, the DCL interrupt will be cleared by the Wait for Interrupts transaction and the interrupt via ARQ will not be detected until the next DCL.

If the PPOLL byte is non-zero, a check for CIC is done and an error is returned if the card is not CIC. If the card is not System Controller, however, and if it becomes non-CIC one the wait has started, no error will be reported. The way to detect this is to enable the wait-for-interrupt bit NCC, and test the reason for resuming.

Interrupt Operation

The card performs the following idle process in order to report interrupts:

NOTE

DISABLED is a flag used on the card. The "blocks" referred to below all have the same format as the block described in the "Format of Interrupt Block" paragraph.

1. Update a "conditions occured" block until DISABLED = true.
2. Update a "reason(s) for interrupt" block by ORing to it the ANDed bits of the "conditions occurred" and the "conditions enabled" blocks.
3. If the "reason(s) for interrupt" block is all zeros or DISABLED = true, go to step 1.
4. Interrupt the host (via a STT status byte), set DISABLED true and reset the resettable "reason(s) for interrupt" in the "conditions occured" block.
5. Go to step 1.

In order for the card to interrupt again (clear DISABLED in above algorithm), the host must do one of:

1. Reset the card via PPON, DCL, or RST.
2. Write a non-zero interrupt mask.

In order to clear the reasons for interrupt, the host must do one of:

1. Reset the card via PPON, DCL, or RST (mask will be zero).
2. Read the reason for interrupting.

Bit Definitions

The PPOLL byte contains bits corresponding to the eight PPOLL bits defined in the IEEE-488 standard. The bits are defined as states, i.e., they cannot be reset and still reflect the most current asserted/deasserted level. When any of these bits become enabled, there is the side effect that POLLing will be done during otherwise idle times (if CIC).

The byte following the PPOLL byte (states byte) contains the following detectable states (from least significant bit (LSB) to most significant bit (MSB), or left to right):

CIC: Controller-In-Charge

REN: IEEE-488 defined "remote control". Detected only if not CIC.

SRQ: Assertion of Service ReQuest

TLK: Configured to TaLK

LTN: Configured to lisTeN

DAT: At least one byte is available on the card's inbound FIFO. Not detected if the card's inbound FIFO is involved in current transaction.

NCC: Not Controller in Charge.

None of the bits in the states byte have side effects as in the PPOLL byte.

The last byte of one of these blocks is the events byte. The bits are similar to the states byte bits except that they are resettable; some of these bits, however, have side effects as explained below:

MSA: A secondary address was intercepted during an HP-IB data transfer operation. Note: This interrupt will not be detected until a read request causes the MSA to be read from the HP-IB chip's FIFO. The secondary has side effects on the "data transfer transaction" and the "read-last-secondary" transactions - see these transaction descriptions for detail.

PTY: Interface command odd parity error.

GET: Group Execute Trigger.

IFC: HP-IB Interface Clear (Also aborts ongoing data transfers)

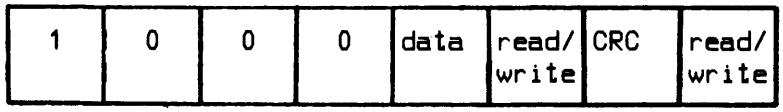
DCL: HP-IB Device Clear

CS/80 TRANSACTION

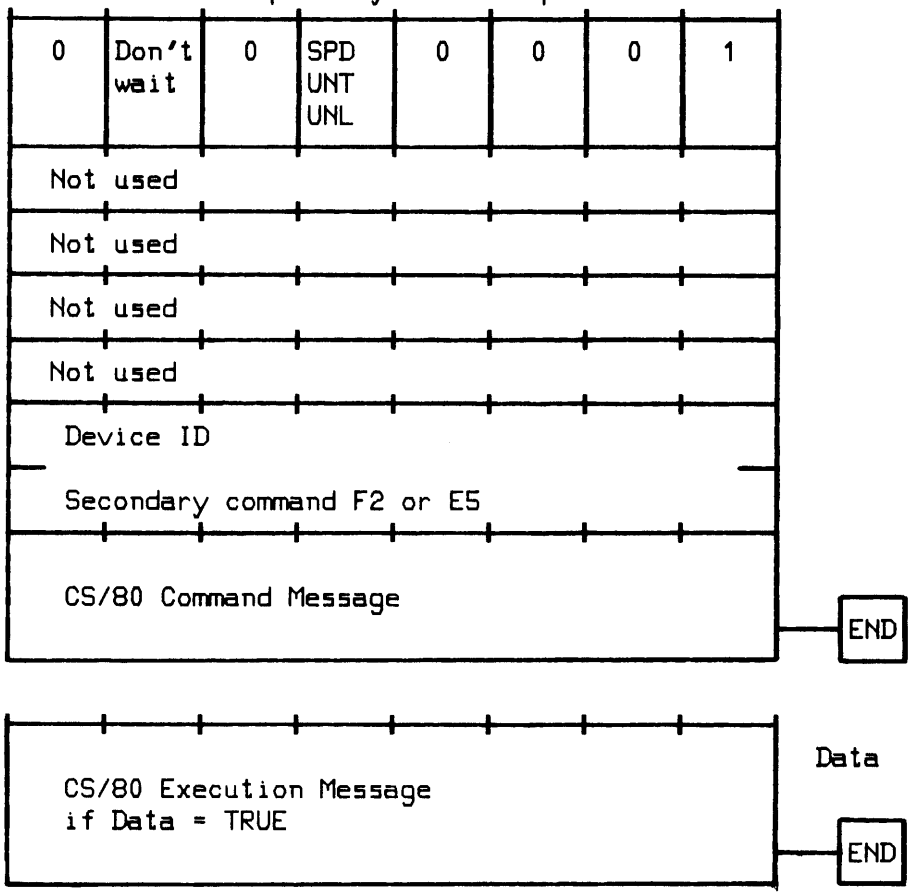
NOTE

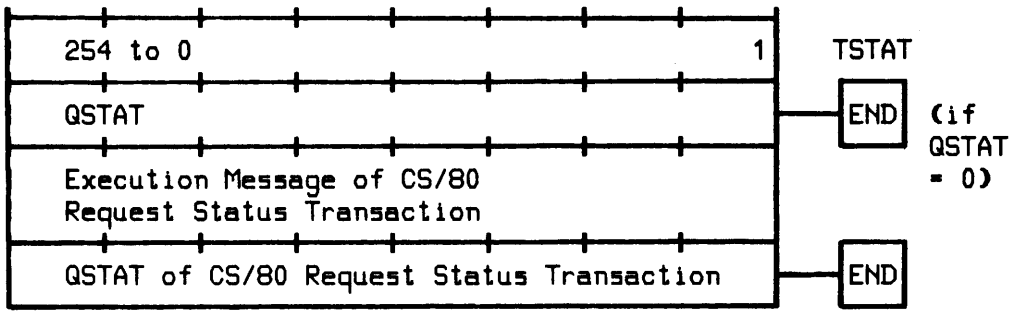
CS/80 refers to the Hewlett-Packard Command Set '80, which is an HP protocol for commands used in controlling devices such as tape or disc drives.

Request Block



Second and Subsequent Bytes of Request Block





Device ID = 0...7 Device address

Secondary command = Control or Transparent Transaction

QSTAT = CS/80 QSTAT

If QSTAT <> 0, then the CS/80 Request Status transaction will be carried out and the Execution Message and Report Message will also be returned.

The CS/80 transaction provides support of the controller's CS/80 transaction protocol for control transactions. In a particular case, this transaction also supports CS/80 transparent transactions. The presence and direction of the CS/80 Excecution Message is determined by the Request Code. The implementation is described below, first the host-to-card interaction and then card-to-device interaction. For meanings of CRC bits, see the paragraph "Data Transfer Between Card and Another HP-IB Device".

HOST-TO-CARD INTERACTION:

Part 1: Write Command consisting of nine or more bytes as shown in request block

Part 2: Data. Read or Write per Request Code, or absent if no data

Part 3: Read status

Byte 1: TSTAT. Card dependent status. Does not reflect QSTAT

Byte 2: CS/80 QSTAT

Byte 3 to up to 22: QSTAT of CS/80 Request Status execution message if QSTAT <> 0

Byte n: QSTAT of CS/80 Request Status if QSTAT <> 0

CARD-TO-DEVICE INTERACTION:

Control:

Card receives write control message from host

Card determines transaction type is CS/80

Card sends interface message:

card talk address (30)

UNL (unlisten)

device listen address

secondary for command or transparent

data message starting with byte 9 from host

UNL (unlisten)

Execute:

Card uses PPOLL and device's ID to determine when device is ready.

When device is ready, card requests a data transfer from host.

When host acknowledges with data transfer, card addresses the device.

card talk or listen address

device listen or talk address

execute secondary

data message

UNL

Report:

When device is ready, card requests a read status from host

Host acknowledges with read status

Card sends TSTAT to host

Card addresses the device and reads QSTAT

card address

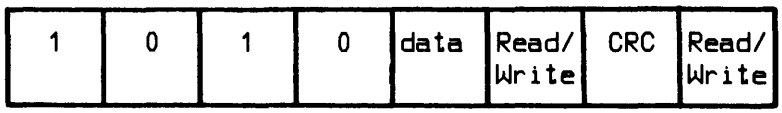
device address

report secondary

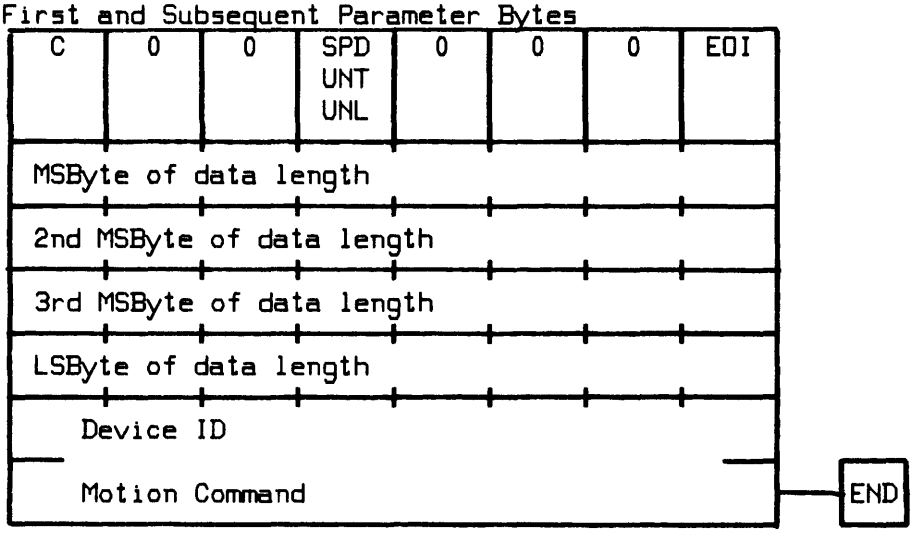
QSTAT read by card

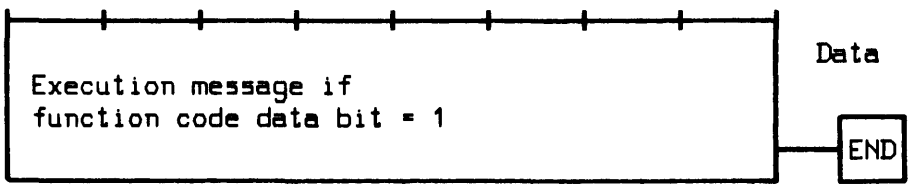
QSTAT is sent to host and, if QSTAT = 0, read status is terminated. If QSTAT <> 0, a CS/80 Request Status transaction is made and the resulting execution message and QSTAT are sent to the host.

MAGNETIC TAPE TRANSACTION



First and Subsequent Parameter Bytes





Device ID = 0 - 7 - Device address.
Motion command = HP 7970 command

For meanings of CRC bits, see the paragraph "Data Transfer Between Card and Another HP-IB Device".

The Magnetic Tape transaction supports data transfers with the HP 7970 Magnetic Tape Drive. The HP-IB interactions are shown below. If the QSTAT value returned from the magnetic tape after the motion command is not zero, the transaction is terminated early. The TSTAT will indicate the transaction was terminated early due to non-zero DSJ value.

```
HP-IB Mag Tape interactions

  HP-IB Card                  Magnetic Tape

    <UNL>
    <bus t>
    <dev 1>
    <sec 61>
    <motion command>
    <begin PPOLL>
                               <respond to PPOLL>
    <UNL>
    <bus 1>
    <dev  t>
    <sec 70>
                               <send dsj>

    IF DSJ.NE.0 THEN ERROR EXIT
    IF WRITE
       THEN
         <UNL>
         <bus t>
         <dev 1>
         <sec E0>
         <send data message>
    ELSE
         <sec E0>
                                <send data message>
    END
```

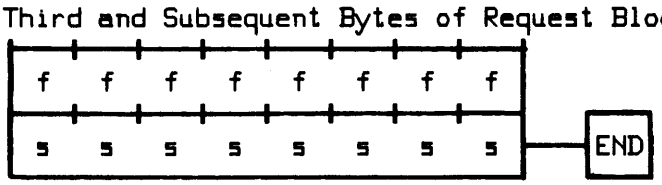
AMIGO IDENTIFY TRANSACTION

The AMIGO Identify transaction is not supported as a unique transaction. The command and data sequences of an AMIGO Identify can by constructed using the HP-IB Data Transfer Transaction.

NOTE

AMIGO is a Hewlett-Packard term for a specific implementation of HP-IB.

AMIGO Identify Configuration



ffffffff = First ID Byte.
ssssssss = Second ID Byte.

The response to an Amigo Identify is set by this transaction, if the card is not the CIC. This transaction disrupts any configuration of conditions for interrupt due PPOLL response which may have been previously set. If the card is the CIC, an error will be returned.

MAINTENANCE

SECTION V

The only maintenance recommended by Hewlett-Packard for the HP-IB card is to return a malfunctioning card to Hewlett-Packard for repair.

To determine if a card is malfunctioning, run the self-test as outlined in the "Start-Up" paragraph in Section 2.

If the HP-IB card is malfunctioning, remove it from the system and return it to Hewlett-Packard. Refer to "Reshipment" in Section 2 for instructions on shipping the card.

If desired, isolation to a defective part may be performed. Please be advised, however, that such work is at your discretion and is your responsibility; moreover, NOTE THAT CUSTOMER REPAIR OR MODIFICATION OF THE HP-IB CARD WILL INVALIDATE WARRANTY AND RENDER THE CARD INELIGIBLE FOR EXCHANGE OR REPAIR BY HEWLETT-PACKARD COMPANY. If such service is performed, the replaceable parts information in Section 6 and the schematic logic diagrams in Section 7 will be of assistance.

REPLACEABLE PARTS

SECTION VI

This section contains information for ordering replaceable parts for the HP-IB card. Table 6-1 contains a list of replaceable parts, table 6-2 contains the names and addresses of the manufacturers indexed by the code numbers used in table 6-1, and figure 6-1 shows the locations of the parts on the HP-IB card.

REPLACEABLE PARTS

Table 6-1 contains a list of replaceable parts in reference designation order. The following information is listed for each part:

1. Reference designation of the part.
2. The Hewlett-Packard part number.
3. Part number check digit (CD).
4. Total quantity (QTY).
5. Description of the part.
6. A five-digit manufacturer's code number of a typical manufacturer of the part. Refer to table 6-2 for a cross-reference of the manufacturers.
7. The manufacturer's part number.

ORDERING INFORMATION

To order replacement parts or to obtain information on parts, address the order or inquiry to the nearest Hewlett-Packard Sales and Service Office (Sales and Service Offices are listed at the back of this manual).

To order a part listed in the replaceable parts table, quote the Hewlett-Packard part number (with the check digit), and indicate the quantity required. The check digit will insure accurate and timely processing of your order.

To order a part that is not listed in the replaceable parts table, specify the following information:

1. Identification of the kit containing the part (refer to the product identification information supplied in Section 2).

2. Description and function of the part.

3. Quantity required.

Table 6-1. HP 27110A Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	27110-60001	2	1	PCA-HPIB HPIO	28480	27110-60001
C1	0180-0228	6	1	CAPACITOR-FXD 22UF+-10% 15VDC TA	56289	150D226X9015B2
C2	0180-0116	1	1	CAPACITOR-FXD 6.8UF+-10% 35VDC TA	56289	150D685X9035B2
C3	0160-4832	4	31	CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C4	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C5	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C6	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C7	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C8	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C9	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C10	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C11	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C12	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C13	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C14	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C15	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C16	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C17	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C18	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C19	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C20	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C21	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C22	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C23	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C24	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C25	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C26	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C27	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C28	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C29	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C30	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C31	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C32	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C33	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
CR1	1990-0486	6	1	LED-LAMP LUM-INT=1MCD IF=20MA-MAX BVR=5V	28480	5082-4684
J1	1251-7276	0	1	CONNECTOR-80 PIN	28480	1251-7276
J2	1251-7589	8	1	CONNECTOR-26 PIN MALE	28480	1251-7589
R1	0698-0084	9	1	RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
R2	0698-3442	9	1	RESISTOR 237 1% .125W F TC=0+-100	24546	C4-1/8-T0-237R-F
R3	0757-0123	3	2	RESISTOR 34.8K 1% .125W F TC=0+-100	28480	0757-0123
R4	0757-0123	3		RESISTOR 34.8K 1% .125W F TC=0+-100	28480	0757-0123
R5	2100-3869	1	1	RESISTOR-TRMR 100K 10% C SIDE-ADJ 17-TRN	28480	2100-3869
R6	0698-3447	4	1	RESISTOR 422 1% .125W F TC=0+-100	24546	C4-1/8-T0-422R-F
R7	0698-3445	2	1	RESISTOR 348 1% .125W F TC=0+-100	24546	C4-1/8-T0-348R-F
S1	3101-2243	6	1	SWITCH-DIP 8 ROCKER	28480	3101-2243
TP1	0360-1682	0	1	TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
U11	1820-2862	7	2	IC-DS 3667	28480	1820-2862
U12	1820-2862	7		IC-DS 3667	28480	1820-2862
U13	1820-1633	8	3	IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U14	1820-1633	8		IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U15	1820-1144	6	1	IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
U23	1820-1633	8		IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U24	1820-0684	7	1	IC INV TTL S HEX 1-INP	01295	SN74S05N
U25	1820-1568	8	1	IC BFR TTL LS BUS QUAD	01295	SN74LS125AN
U31	1820-2975	3	1	IC-BIC C2000	28480	1820-2975
U33	1820-2102	8	1	IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U34	1820-1197	9	1	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U35	1820-1196	8	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS174N
U41	1200-0567	1	3	SOCKET-IC 28-CONT DIP DIP-SLDR	28480	1200-0567
U44	1820-2857	0	1	IC- Z8611PS	28480	1820-2857
U45	1820-2920	8	1	HAL 16R 8CN	28480	1820-2920
U51	1200-0567	1		SOCKET-IC 28-CONT DIP DIP-SLDR	28480	1200-0567
U54	1AD5-6101	9	1	ABI CHIP	28480	1AD5-6101
U55	1820-1216	3	1	IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
U61	1818-3078	4	1	ROM-4K X 8- (27110)	28480	1818-3078
U61	1200-0567	1		SOCKET-IC 28-CONT DIP DIP-SLDR	28480	1200-0567
U62	1820-2058	3	2	IC MISC TTL S QUAD	07263	MC3448AL
U64	1820-2024	3	1	IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U65	1820-1208	3	1	IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
U72	1820-2058	3		IC MISC TTL S QUAD	07263	MC3448AL
U74	1200-0539	7	2	SOCKET-IC 18-CONT DIP DIP-SLDR	28480	1200-0539

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-1. HP 27110A Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U75	1820-1201	6	1	IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
U81	1820-1199	1	1	IC INV TTL LS HEX 1-INP	01295	SN74LS04N
U82	1810-0081	7	1	NETWORK-RES 18-DIP MULTI-VALUE	28480	1810-0081
U82	1200-0539	7		SOCKET-IC 18-CONT DIP DIP-SLDR	28480	1200-0539
U84	1810-0235	3	1	NETWORK-RES 16-DIP2.2K OHM X 15	01121	316A222
U85	1820-1112	8	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U93	1820-2485	0	1	IC RCVR TTL LS BUS OCTL	01295	SN75160N
U95	1813-0194	9	1	CRYSTAL OSCILLATOR 8 MHZ	28480	1813-0194
W2	8159-0005	0	1	RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	8159-0005
	1480-0116	8	2	PIN-GRV .062-IN-DIA .25-IN-LG STL	28480	1480-0116
	1818-1633	3	2	EPROM 2732A-3	34649	D2732A-3
	5041-3467	2	2	HPIO EXTRACTOR HANDLE	28480	5041-3467
	27110-80001	4	1	PC BOARD-BLANK	28480	27110-80001
	27110-80002	5		1818-1633 HPIB	28480	27110-80002
	27110-80003	6		1818-1633 HPIB	28480	27110-80003

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Manufacturer's Code List

MFR NO.	MANUFACTURER NAME	ADDRESS	ZIP CODE
01121	ALLEN-BRADLEY CO.	MILWAUKEE, WI.	53204
01295	TEXAS INSTRUMENTS, INC. SEMICONDUCTOR COMPONENTS DIV.	DALLAS, TX	75222
07263	FAIRCHILD SEMICONDUCTOR DIV.	MOUNTAIN VIEW, CA.	94042
24546	CORNING GLASS WORKS (BRADFORD)	BRADFORD, PA.	16701
28480	HEWLETT-PACKARD CO. CORPORATE HQ.	PALO ALTO, CA.	94304
34649	INTEL CORP.	MOUNTAIN VIEW, CA.	95051
56289	SPRAGUE ELECTRIC CO.	NORTH ADAMS, MA.	01247

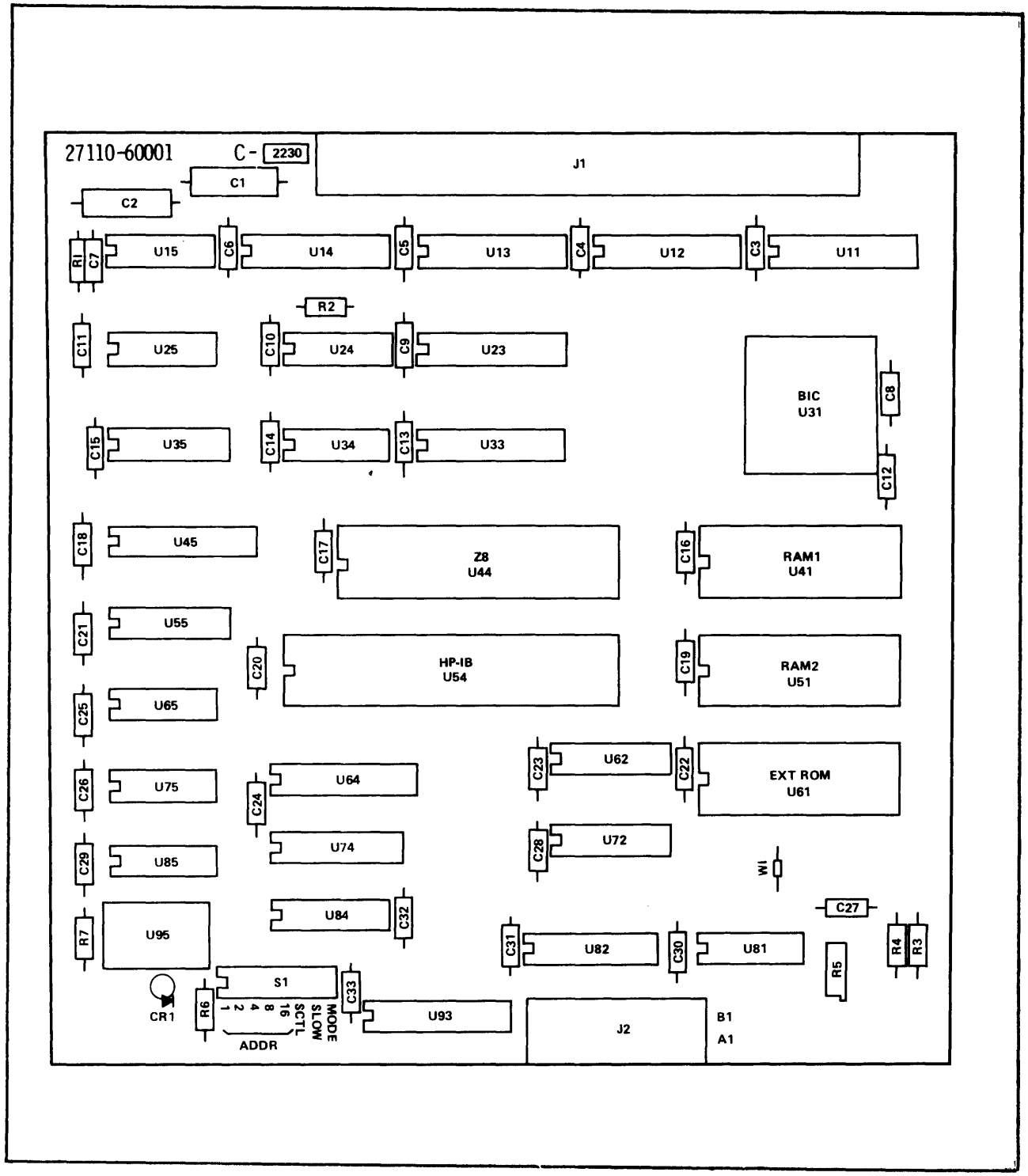


Figure 6-1. HP 27110A Parts Location Diagram

SCHEMATIC DIAGRAMS

SECTION VII

This section contains a functional block diagram and schematic logic diagrams for the HP-IB card, and an algorithmic state diagram for the DMA controller.

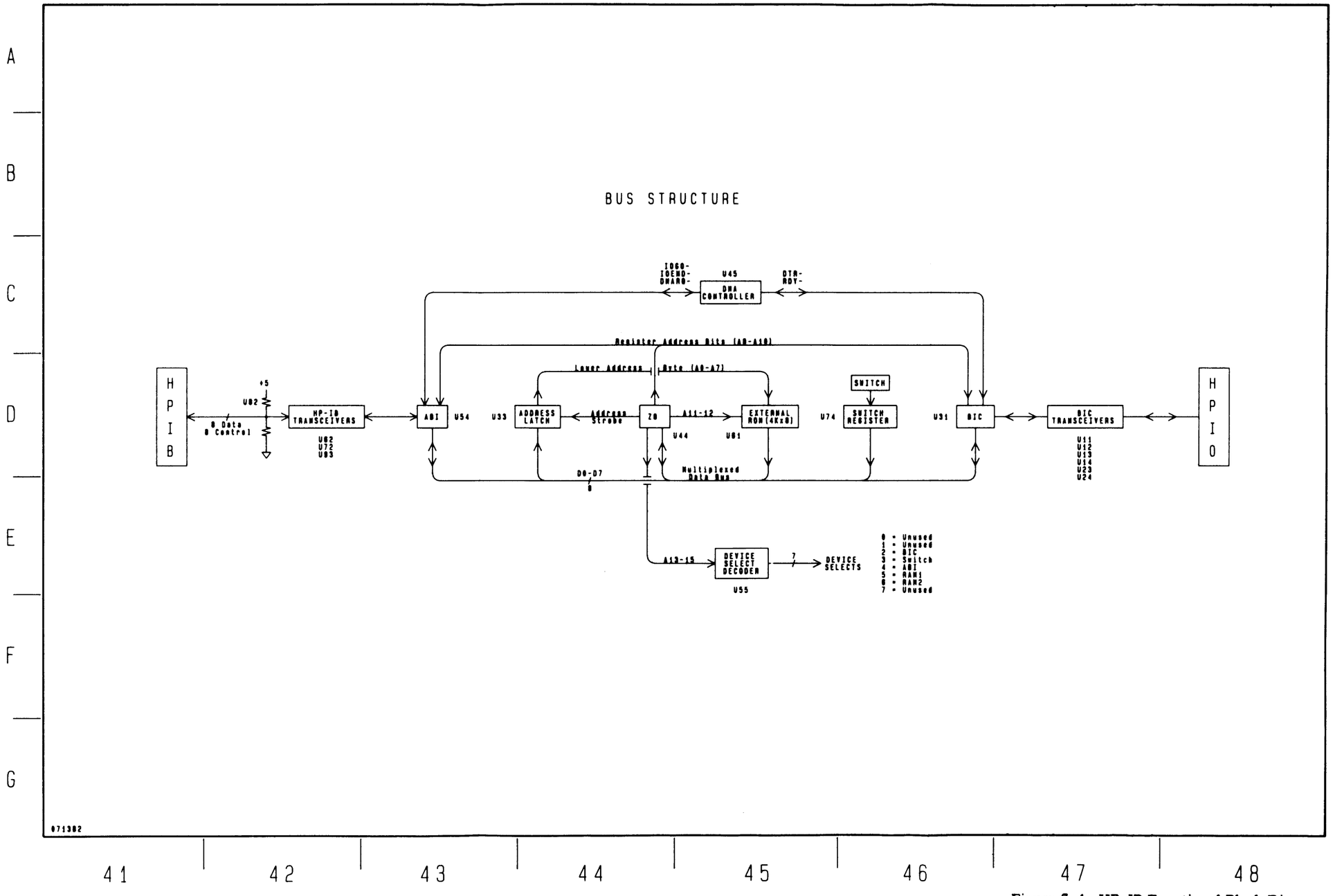


Figure 7-1. HP-IB Functional Block Diagram

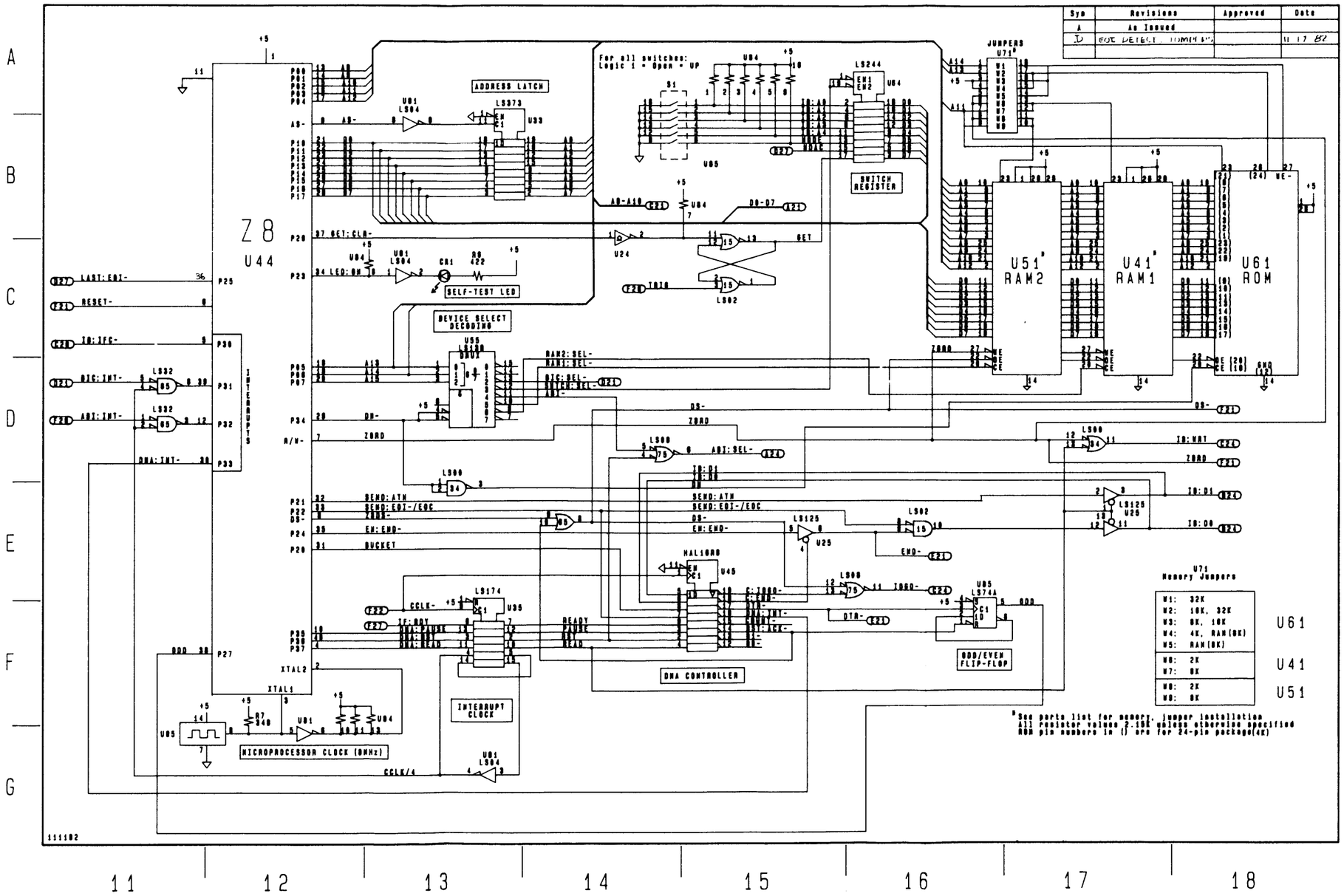
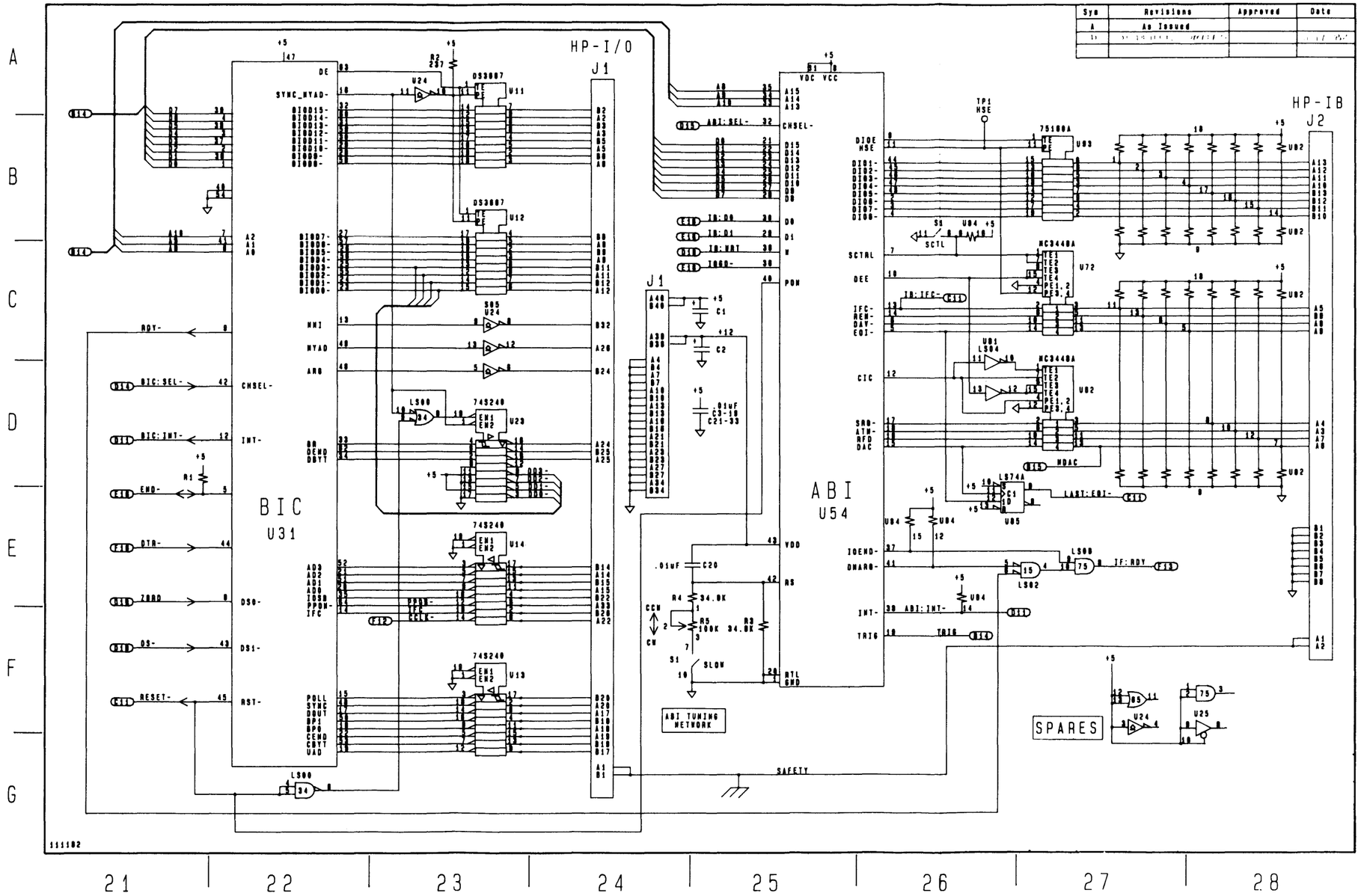


Figure 7-2. HP-IB Schematic Logic Diagram (Sheet 1 of 2)



Sym	Revisions	Approved	Date
A	As Issued		

Figure 7-2. HP-IB Schematic Logic Diagram (Sheet 2 of 2)

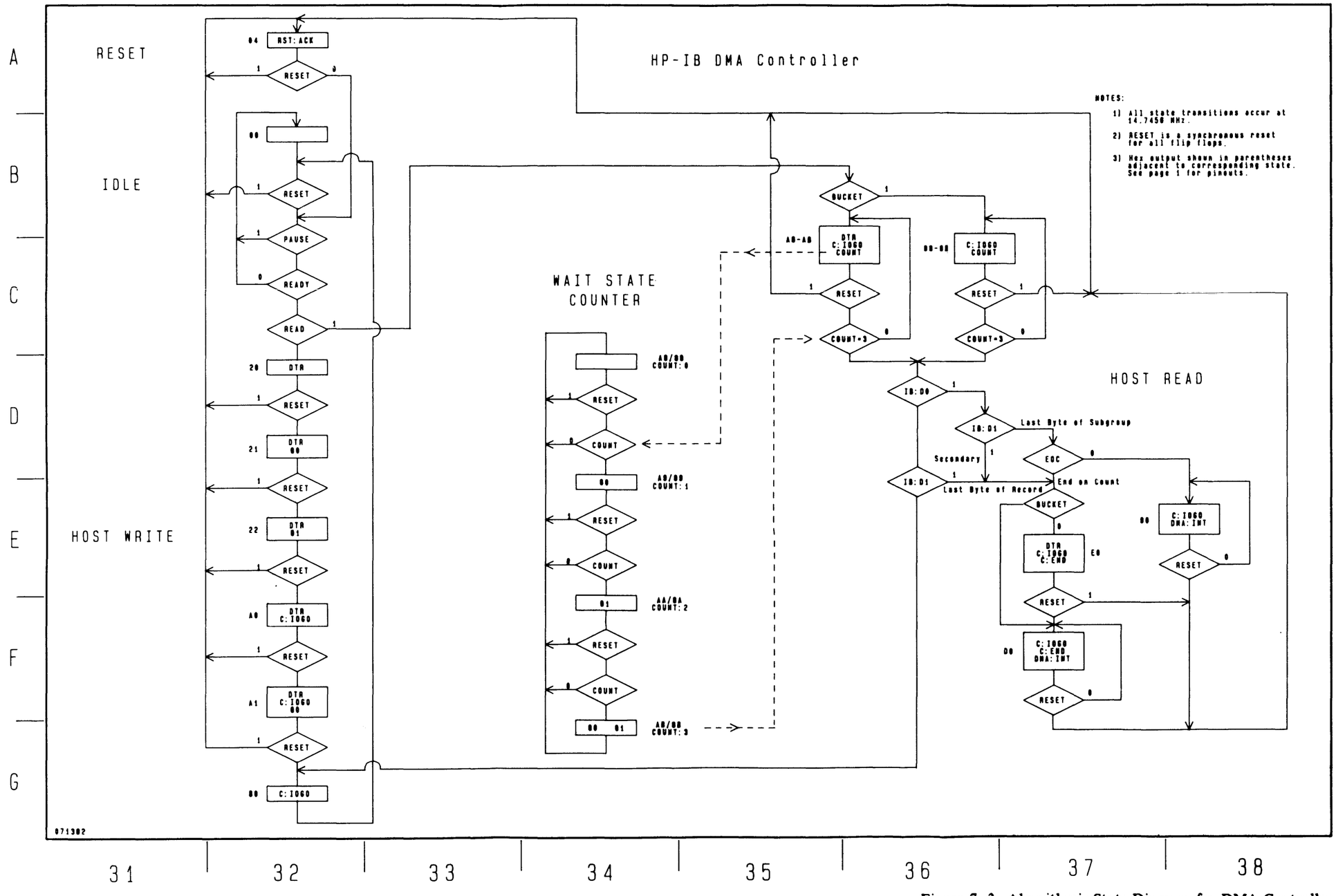


Figure 7-3. Algorithmic State Diagram for DMA Controller

ASCII CHARACTERS AND BINARY CODES

APPENDIX A

	0	1	2	3	4	5	6	7
0	NUL	DLE	sp	0	@	P	`	p
1	SOH	DC1	!	1	A	Q	a	q
2	STX	DC2	"	2	B	R	b	r
3	ETX	DC3	#	3	C	S	c	s
4	EOT	DC4	$	4	D	T	d	t
5	ENQ	NAK	%	5	E	U	e	u
6	ACK	SYN	&	6	F	V	f	v
7	BEL	ETB	'	7	G	W	g	w
8	BS	CAN	(	8	H	X	h	x
9	HT	EM	)	9	I	Y	i	y
A	LF	SUB	*	:	J	Z	j	z
B	VT	ESC	+	;	K	[	k	{
C	FF	FS	,	<	L	\	l	|
D	CR	GS	-	=	M	]	m	}
E	SO	RS	.	>	N	^	n	~
F	SI	US	/	?	O	_	o	DEL

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