HP 27128A
Asynchronous Serial Interface (ASI)

Technical Reference Manual

Card Assembly: 27128-60101
Date Code: A-2322

HEWLETT PACKARD

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PRINTING HISTORY

The Printing History below identifies the Edition of this Manual and any Updates that are included. Periodically, update packages are distributed which contain replacement pages to be merged into the manual, including an updated copy of this Printing History page. Also, the update may contain write-in instructions.

Each reprinting of this manual will incorporate all past updates; however, no new information will be added. Thus, the reprinted copy will be identical in content to prior printings of the same edition with the user-inserted update information. New editions of this manual will contain new information, as well as updates.

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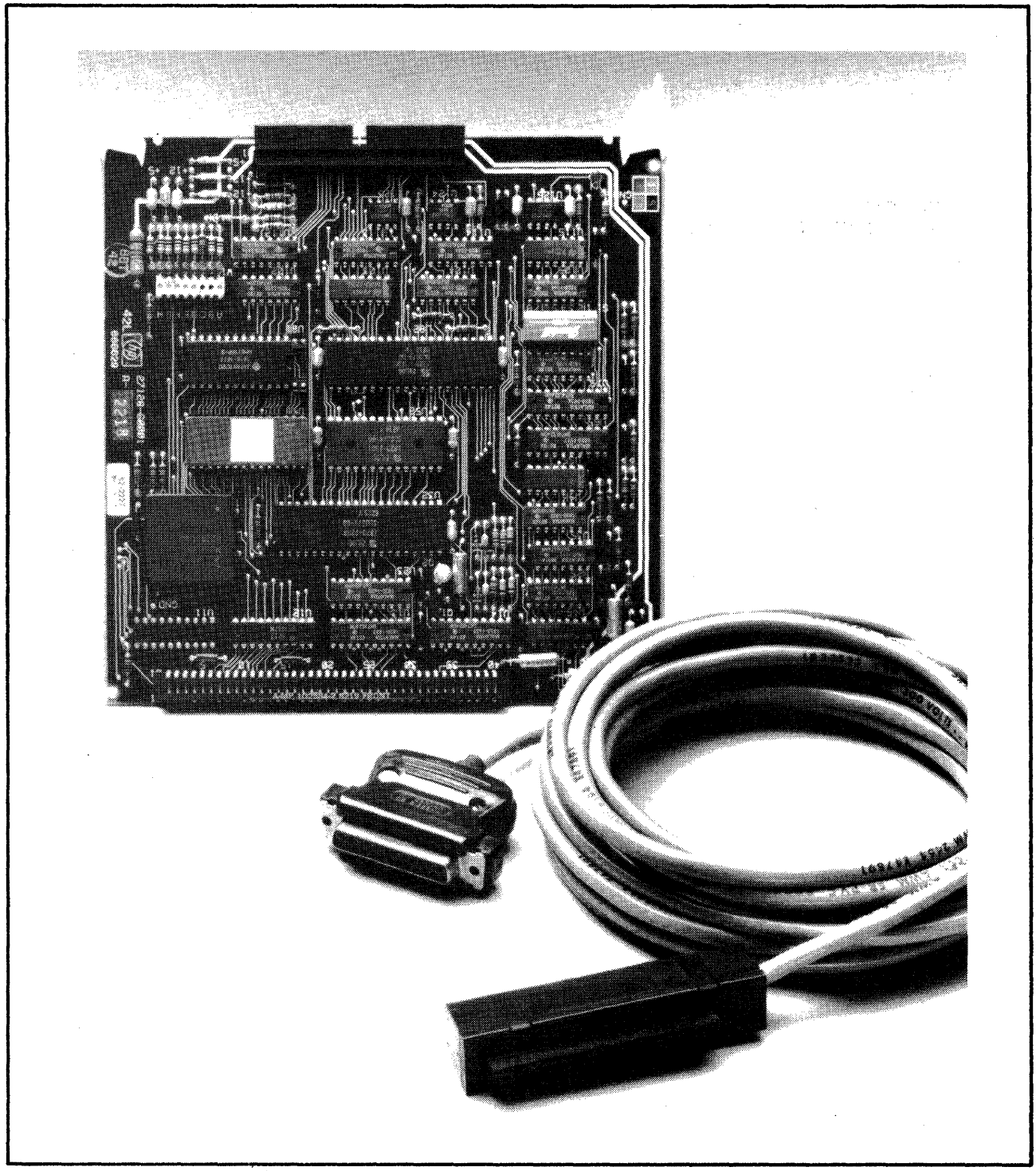


Figure 1-1. HP 27128A Asynchronous Serial Interface

GENERAL INFORMATION

SECTION I

This manual provides general information, installation, theory of operation, maintenance instructions, replaceable parts information, and servicing diagrams for the Hewlett-Packard HP 27128A Asynchronous Serial Interface (ASI). This section contains general information concerning the ASI, and includes a description and specifications.

PHYSICAL DESCRIPTION

The HP 27128A Asynchronous Serial Interface (ASI) is shown in figure 1-1 and consists of a printed circuit card, a cable, and an installation manual.

FUNCTIONAL DESCRIPTION

The HP 27128A Asynchronous Serial Interface (ASI) provides an asynchronous serial communications link between a Hewlett-Packard computer system and an EIA RS-232-C/RS-423-compatible or CCITT V.24/V.28-compatible terminal or other similar peripheral device. The ASI allows modem control or direct interfacing to the peripheral device.

Figure 1-2 shows a Hewlett-Packard computer system using CHANNEL I/O and the ASI. (CHANNEL I/O is a Hewlett-Packard standard defining the physical and electrical characteristics for an I/O system consisting of an I/O channel, an I/O channel adapter, and I/O cards. The ASI is one of the I/O cards.)

Note that the computer system CPU and memory communicate directly along a Memory/Processor Bus (MPB). I/O data to/from peripheral devices reaches the CPU/memory through the I/O channel, the I/O channel adapter, and an I/O card such as the ASI card. The I/O data is received from and transmitted to peripheral devices by the I/O card, which converts device-specific data to a format compatible with the I/O channel, and thus the computer. The I/O channel adapter (see figure 1-2) controls the flow of traffic between the I/O channel and the memory/processor bus.

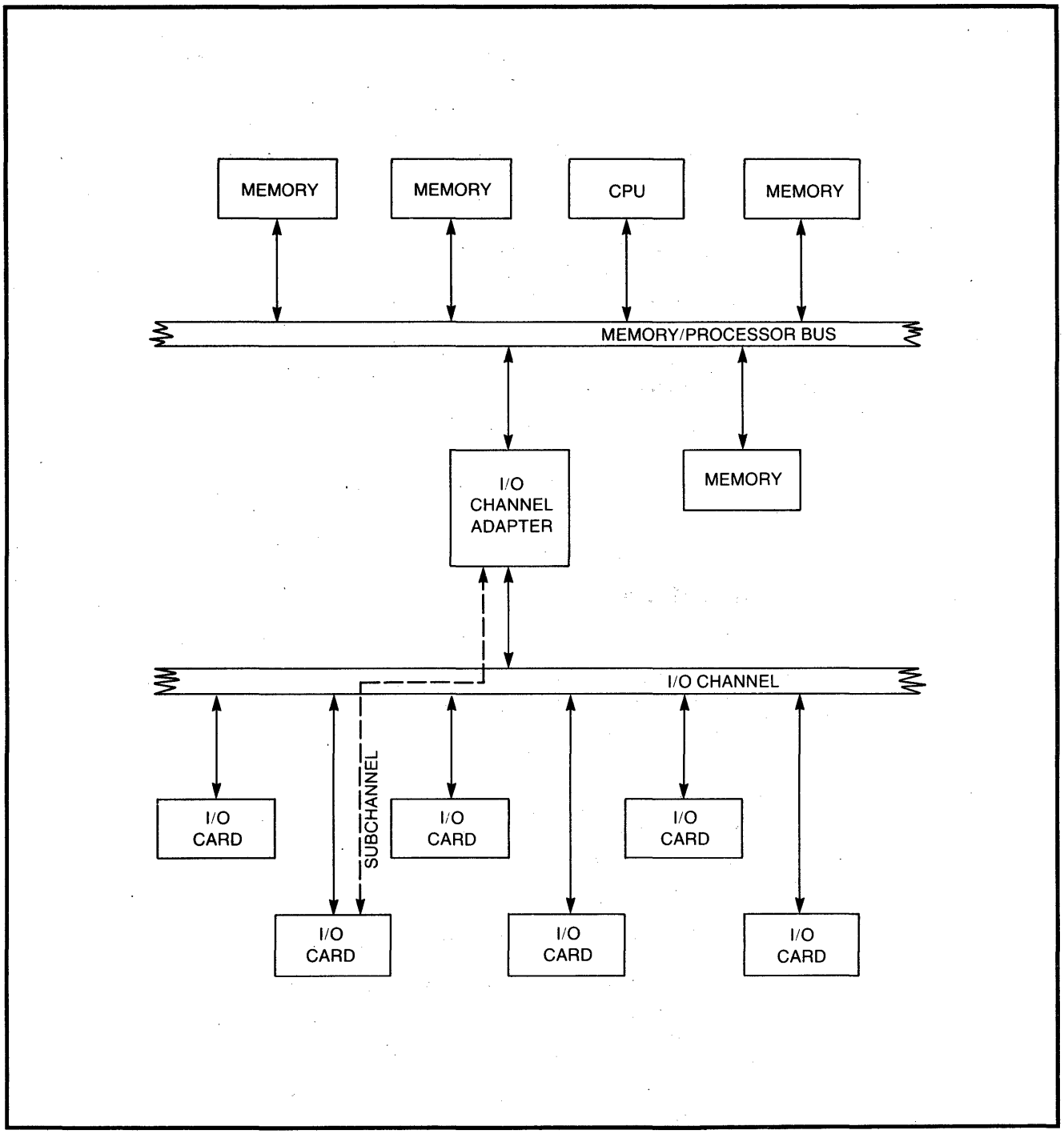


Figure 1-2. ASI in a Typical Hewlett-Packard Computer System

EQUIPMENT SUPPLIED

The standard HP 27128A ASI Interface consists of the following items (see figure 1-1):

ASI card, part number 27128-60001

Five meter female RS-232-C cable, part number 27128-63002

Installation manual, part number 27128-90001

The following option is available with the HP 27128A product:

Option 001:

Five meter male (modem) RS-232-C cable, part number ~~27128-63001~~ ORDER 27122-63001

IDENTIFICATION

The Product

Up to five digits and a letter (27128A in this case) are used to identify Hewlett-Packard products. The five digits identify the product; the letter indicates the revision level of the product.

Interface Card

The interface card supplied with the HP 27128A product is identified by a part number marked on the card. In addition to the part number, the card is further identified by a letter and a four-digit date code (e.g., A-2322). This designation is placed below the part number. The letter identifies the version of the etched circuit on the card. The date code (the four digits following the letter) identifies the electrical characteristics of the card with components mounted. Thus, the complete part number on the ASI card could be:

27128-60101
A-2322

If the date code stamped on the card does not agree with the date code on the title page of this manual, there are differences between your card and the card described herein. These differences are described in manual supplements available at the nearest Hewlett-Packard Sales and Service Office (a list of Hewlett-Packard Sales and Service Offices is contained at the back of this manual).

Manuals

The Installation Manual (part number 27128-90001, supplied with the HP 27128A product) and this manual (HP 27128 Technical Reference Manual, part number 27132-90001) are identified by name and part number. (Note that this manual is part of the HP 27132A Technical Reference Package.) The name, part number, and publication date are printed on the title page of each manual. If the manual is revised, the publication date is changed. In this manual, the "Printing History" page (page ii) records the reprint dates and manual update record. Reprint dates for the Installation Manual are printed on the title page.

SPECIFICATIONS

Table 1-1 lists the specifications of the ASI.

Table 1-1. Specifications

FEATURES

* Microprocessor subsystem (Zilog Z-80A) is programmed to perform the following functions:

  Parity generation and checking

  Backspace and line delete processing

  Host and device character handshake

  Termination character detection

  Full-duplex modem handshake

* EIA RS-232-C, RS-423, and CCITT V.24, V.28 compatibility

* Modem control signals configurable by software to allow operation with most available modems

* Full-duplex, echoplex, or simplex operation

* Data rates selectable up to 19,200 bits per second (baud)

* Full-duplex communications at 19.2K baud without receive buffer overflow

Table 1-1. Specifications (Continued)

* Character buffering: up to 500 bytes in transmit mode, up to 480 bytes in receive mode
* Can send or receive 5, 6, 7, or 8 bits per character, plus even, odd, or no parity
* Will operate with 1, 1.5, or 2 stop bits
* Will detect and generate BREAK signal

PHYSICAL CHARACTERISTICS

Size:	193.04 mm long by 171.45 mm wide by 16.383 mm thick (7.6 by 6.75 by 0.645 inches)
Weight:	203.6 grams (0.448 pound)
I/O Channel Interconnects:	80-pin connector, J1
Device Interconnects:	50-pin connector, J2

POWER REQUIREMENTS

Voltage	Current	Power Dissipation
+5V	1.29A	6.45W
+12V	54mA	0.65W
-12V	73mA	0.87W

MTBF = 133K HRS

INSTALLATION

SECTION II

This section provides information on installing and checking the operation of the ASI.

COMPUTATION OF CURRENT REQUIREMENTS

The ASI circuit card obtains its operating voltages from the host computer power supply through the I/O channel. Before installing the card, it is necessary to determine whether the added current will overload the power supply. The current requirements of the card are listed in the power requirements entry of table 1-1. Current requirements for all other I/O cards can be found in the appropriate Technical Reference Manuals.

FIRMWARE (EPROM) INSTALLATION

CAUTION

SOME OF THE COMPONENTS USED IN THISPRODUCT ARE SUSCEPTIBLE TO DAMAGE BY STATIC DISCHARGE. REFER TO THE SAFETY CONSIDERATIONS INFORMATION AT THE FRONT OF THIS MANUAL BEFORE HANDLING THE CARD OR REMOVING OR REPLACING COMPONENTS.

The EPROM and RAM are installed in a socket provided on the ASI card as shown in figure 2-1. Ensure that they are installed properly, and that they have not been damaged or loosened from their sockets during shipping.

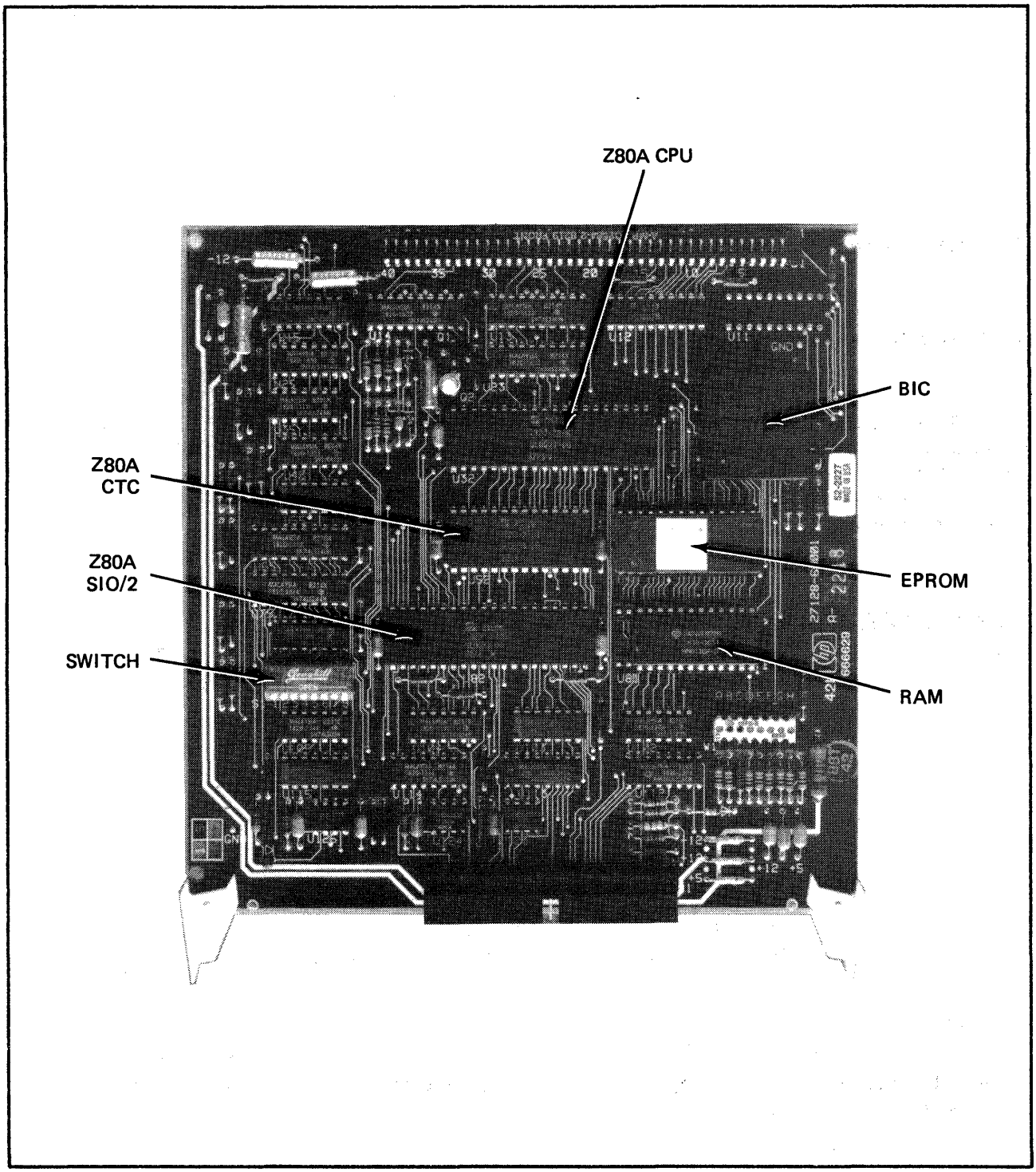


Figure 2-1. EPROM, RAM, and Switch Locations

Additionally, when installing or removing the EPROM or RAM, guard against bending or breaking the pins on the component. These pins also can become folded between the component and its socket, which would result in intermittent operation of the ASI. In most cases, a bent or damaged pin can be straightened with careful use of needle-nose pliers.

CONFIGURATION SWITCH DEFINITIONS

Eight switches on the ASI card (see figure 2-1 for locations) allow you to select configuration options. Switch definitions are shown in table 2-1.

Table 2-1. Configuration Switch Definitions

SWITCH NUMBER							
SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8
BIT NUMBER							
D7	D6	D5	D4	D3	D2	D1	D0
FUNCTION							
SINGLE TEXT TERM	HARD-WIRED	NO PARITY	8 DATA BITS	BAUD RATE BIT 3	BAUD RATE BIT 2	BAUD RATE BIT 1	BAUD RATE BIT 0

Single Text Termination Switch

If switch SW1 is open, single text termination is enabled. See Section 4 for a discussion of single text termination.

Hard-Wired Switch

If switch SW2 is open, it signifies that a device is directly connected to the ASI and that all modem control lines are disabled (the host computer, however, can control the modem control lines directly). If this switch is closed, the card will not receive or transmit any data until the host makes a line connection request. This mode can be disabled programmatically.

No Parity Switch

If switch SW3 is open, no parity is used. If the switch is closed, odd parity is programmed into the SIO. The other parity options may be selected programmatically. See Section 4 for a discussion of the parity options.

8-Bit Data Rate Switch

Switch SW4 is used to set the character length. If this switch is open, the character length is 8 bits; if closed, the character length is 7 bits.

Baud Rate Switches

Switches SW5 through SW8 are used to select the baud rate of the ASI. The switch settings and corresponding baud rates are shown in table 2-2. Note that a 1 in table 2-2 signifies an open switch; a 0 means the switch is closed.

I/O CHANNEL INTERFACE

All interface between the ASI and the host computer occurs on the I/O channel. An 80-pin connector (J1) located on the ASI mates with a receptacle on the I/O channel. Connections to J1 are listed in table 2-3.

PERIPHERAL DEVICE INTERFACE

A cable with a 25-pin female RS-232-C connector (cable part number 27128-63002) is provided with the standard HP 27128A product, and a 25-pin male RS-232-C connector (part number 27128-63001) is available as an option. Pinouts of these two cables are shown in tables 2-4 and 2-5.

Table 2-2. Baud Rate Switch Settings

SWITCHES				BAUD RATE
SW5	SW6	SW7	SW8	
0	0	0	0	50
0	0	0	1	75
0	0	1	0	110
0	0	1	1	134.5
0	1	0	0	150
0	1	0	1	300
0	1	1	0	600
0	1	1	1	900
1	0	0	0	1200
1	0	0	1	1800
1	0	1	0	2400
1	0	1	1	3600
1	1	0	0	4800
1	1	0	1	7200
1	1	1	0	9600
1	1	1	1	19200

Table 2-3. I/O Channel Connector J1

PIN NO.	SIGNAL MNEMONIC	SIGNAL DEFINITION
A1	RES	Not used
A2	DB14	Data Bus, Bit 14
A3	DB12	Data Bus, Bit 12
A4	GND	Ground
A5	DB10	Data Bus, Bit 10
A6	DB8	Data Bus, Bit 8
A7	GND	Ground
A8	DB6	Data Bus, Bit 6
A9	DB4	Data Bus, Bit 4
A10	GND	Ground
A11	DB2	Data Bus, Bit 2
A12	DB0	Data Bus, Bit 0
A13	GND	Ground
A14	AD2	Address Bus, Bit 2
A15	AD0	Address Bus, Bit 0
A16	GND	Ground
A17	DOUT	Data Out
A18	BP0	Bus Primitive Bit 0
A19	CEND	Channel End
A20	SYNC	Synchronize
A21	GND	Ground
A22	CCLK	Common Clock
A23	GND	Ground
A24	BR	Burst Request
A25	DBYT	Device Byte
A26	MYAD	My Address
A27	GND	Ground
A28	---	Not used
A29	---	Not used
A30	---	Not used
A31	RES	Reserved
A32	PFW	Power-Fail Warning
A33	PPON	Primary Power On
A34	GND	Ground
A35	AC-	Not used
A36	AC+	Not used
A37	-12	-12V
A38	+12	+12V
A39	+5S	Not used
A40	+5P	+5P

Table 2-3. I/O Channel Connector J1 (Continued)

PIN NO.	SIGNAL MNEMONIC	SIGNAL DEFINITION
B1	---	Not used
B2	DB15	Data Bus, Bit 15
B3	DB13	Data Bus, Bit 13
B4	GND	Ground
B5	DB11	Data Bus, Bit 11
B6	DB9	Data Bus, Bit 9
B7	GND	Ground
B8	DB7	Data Bus, Bit 7
B9	DB5	Data Bus, Bit 5
B10	GND	Ground
B11	DB3	Data Bus, Bit 3
B12	DB1	Data Bus, Bit 1
B13	GND	Ground
B14	AD3	Address Bus, Bit 3
B15	AD1	Address Bus, Bit 1
B16	GND	Ground
B17	UAD	Unary Address
B18	BP1	Bus Primitive Bit 1
B19	CBYT	Channel Byte
B20	POLL	Poll
B21	GND	Ground
B22	IOSB	I/O Strobe
B23	GND	Ground
B24	ARQ	Attention Request
B25	DEND	Device End
B26	RST	Reset
B27	GND	Ground
B28	---	Not used
B29	---	Not used
B30	RES	Reserved
B31	RES	Reserved
B32	NMI	Non-Maskable Interrupt
B33	SPON	Secondary Power On
B34	GND	Ground
B35	AC-	Not used
B36	AC+	Not used
B37	-12	-12V
B38	+12	+12V
B39	+5S	Not used
B40	+5P	+5P

Table 2-4. RS-232-C Male Cable Pinouts

CABLE CONNECTOR PIN NO.	ASI CARD CONNECTOR J2 PIN NO.	FUNCTION
1	Shield	
2	A22	Transmitted Data
3	A9	Received Data
4	B15	Request to Send
5	A8	Clear to Send
6	A12	Data Set Ready
7	B7,B8,B9,B10 B11,B12,B13,B14,	Signal Ground
8	A14	Receiver Ready
9	---	Not Used
10	---	Not Used
11	---	Not Used
12	B16	Secondary Receiver Ready
13	A16	Secondary Clear to Send
14	B17	Secondary Tranmitted Data
15	---	Not Used
16	B18	Secondary Received Data
17	---	Not Used
18	---	Not Used
19	A17	Secondary Request to Send
20	A15	Data Terminal Ready
21	---	Not Used
22	B19	Incoming Call
23	B21	Data Signal Rate Selector
24	---	Not Used
25	---	Not Used

Table 2-5. RS-232-C Female Cable Pinouts

CABLE CONNECTOR PIN NO.	ASI CARD CONNECTOR J2 PIN NO.	FUNCTION
1	Shield	
2	A9	Received Data
3	A22	Transmitted Data
4	A8	Clear to Send
5	B15	Request to Send
6	A15	Data Terminal Ready
7	B7,B8,B9,B10, B11,B12,B13,B14	Signal Ground
8	---	Not Used
9	---	Not Used
10	---	Not Used
11	---	Not Used
12	---	Not Used
13	A17	Secondary Request to Send
14	---	Not Used
15	---	Not Used
16	---	Not Used
17	---	Not Used
18	---	Not Used
19	A16	Secondary Clear to Send
20	A12	Data Set Ready
21	---	Not Used
22	---	Not Used
23	---	Not Used
24	---	Not Used
25	---	Not Used

INSTALLATION

CAUTION

ALWAYS ENSURE THAT THE POWER TO THE COMPUTER IS OFF BEFORE INSERTING OR REMOVING THE ASI CIRCUIT CARD AND CABLE. FAILURE TO DO SO MAY RESULT IN DAMAGE TO THE ASI.

CAUTION

SOME OF THE COMPONENTS USED ON THE PRINTED CIRCUIT CARD ARE SUSCEPTIBLE TO DAMAGE BY STATIC DISCHARGE. REFER TO THE SAFETY CONSIDERATIONS INFORMATION AT THE FRONT OF THIS MANUAL BEFORE HANDLING THE CARD.

Install the ASI as follows:

1. Determine if your computer system can supply the power needed for the ASI card. Refer to table 1-1 for power requirements.

2. Set the switches on the card for proper operation in your system. Refer to tables 2-1 and 2-2 for switch locations on the card.

3. Install the card in the appropriate slot in the computer. Refer to the computer system installation manual to determine the correct slot. Components on the card must be on the same side as for other cards in the computer. When installing the card, use care not to damage components or traces on the card or on adjacent cards. Press the ASI card firmly in place.

4. Connect the cable supplied with the card from J2 to the modem or peripheral device.

NOTE

A "grounding grommet" on the interface cable allows the cable shield to be "grounded" at that point in some applications. Refer to your computer installation manual.

START UP

To start up and verify correct operation of the ASI, perform the following:

1. Turn on computer system power.

2. A self-test is contained on the card. The host computer system determines if the self-test is run automatically at power-on or must be invoked by the user. Refer to the appropriate manual for your system for a description of self-test initiation.

   When the self-test executes, the LED located on the card should light briefly and go out. This indicates that the card passed self-test. If the LED does not light at all, the card is defective. If the LED stays on, the card did not pass self-test. For either of these latter two cases, it is recommended that you return the card to Hewlett-Packard; refer to the next paragraph for reshipment information. If you wish to perform maintenance on the card, however, refer to Sections 5, 6, and 7 for maintenance information, replaceable parts lists, and schematic logic diagrams, respectively.

3. Refer to your system documentation for information on using the ASI card in your system.

RESHIPMENT

If the ASI is to be shipped to Hewlett-Packard for any reason, attach a tag identifying the owner and indicating the reason for shipment. Include the part number of the ASI.

Pack the card in the original factory packing material, if available. If the original material is not available, good commercial packing material should be used. Reliable commercial packing and shipping companies have the facilities and materials to repack the item. BE SURE TO OBSERVE ANTI-STATIC PRECAUTIONS.

PRINCIPLES OF OPERATION

SECTION III

The ASI is an EIA RS-232-C/RS-423 single-channel interface for Hewlett-Packard computer systems. It allows modem control and direct interfacing to a variety of devices for asynchronus data communication.

The ASI contains firmware implemented capabilities that simplify interfacing tasks for the host CPU and give more CPU time and space for users. The firmware functions can be disabled to allow the host CPU to directly control most operations so that special needs can be met.

FUNCTIONAL THEORY OF OPERATION

A functional block diagram of the ASI card is shown in figure 3-1. Reference also should be made, as necessary, to the schematic logic diagram contained in figure 7-1. Note that figure 7-1 consists of three sheets. References to this figure will be as follows: 1-A2, 7-1; 2-C6, 7-1, etc.; where the first number, 1 through 3, refers to the sheet number; the combination of letters A through E and numbers 1 through 38 (A2, C6, etc.) refer to the quadrants on the individual sheets; and 7-1 refers to the figure number.

The ASI card contains the following major components:

* Z-80A CPU (Central Processing Unit)
* Z-80A SIO/2 (Serial Input/Output)
* Z-80A CTC (Counter/Timer Circuit)
* BIC (Bus Interface Circuit) plus support circuits
* 8K-byte EPROM
* 2K-byte static RAM
* RS-423 receivers and transmitters (with compatibility for RS-232C and CCITT V.28)
* Connector (J1) to I/O channel
* Connector (J2) to peripheral device

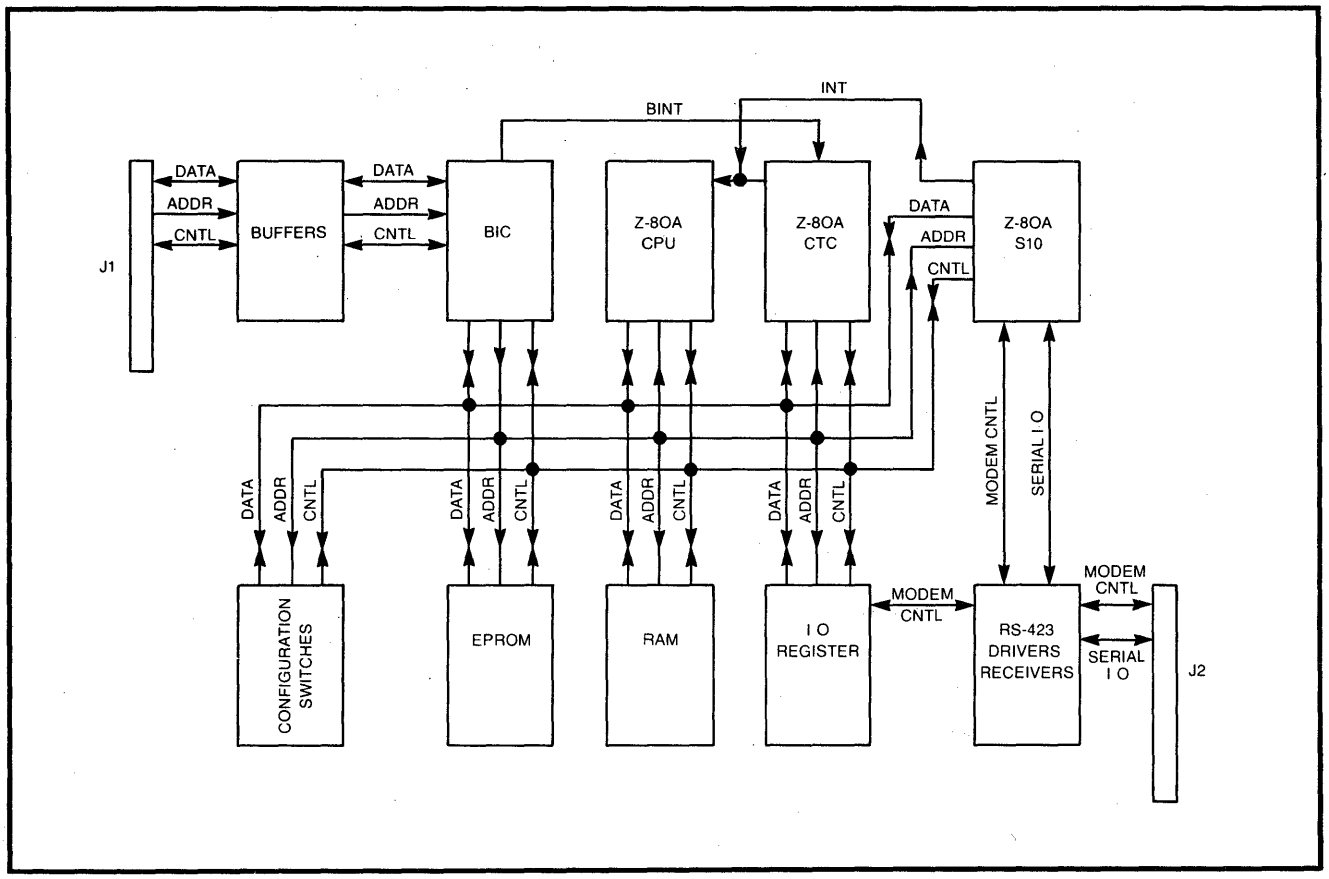


Figure 3-1. ASI Functional Block Diagram

The heart of the ASI is the Z-80A CPU (2-A26,7-1). The CPU controls the Z-80A SIO/2 (3-B34, 7-1), the Z-80A CTC (3-B33, 7-1), the EPROM (2-B24, 7-1), the RAM (2-B22, 7-1), and the BIC gate array (1-A4, 7-1).

The serial asynchronous data and modem control signals are received and transmitted through the RS-423 drivers and receivers. The RS-423 drivers and receivers are controlled by both the SIO and the I/O register (3-E34, 7-1).

A brief description of the function of each block shown in figure 3-1 is as follows:

The BIC is used to bridge the communication between the I/O channel and the Z-80A CPU.

The 8K-byte EPROM is used to store the firmware.

The 2K-byte static RAM is used for I/O buffering and storage of temporary data.

The CTC contains four separate timer/counters, the function of each timer/counter is as follows:

* The first timer/counter is used to generate transmit and receive baud rates for both SIO channels.

* The second timer/counter is used as a character-relative timer. Note that the character-relative timer divides the baud rate from a bit-per-second value to a character-per-second value. Although the bits are sent as fast as before, the character-relative timer can cause a time interval to be inserted once a character has been sent. This gives the device more time to handle the data (print it out, for example). The number of start and stop bits are considered during the division.

* The third timer/counter is used by the ASI's firmware for general purpose tasks such as host ENQ/ACK timer, modem connection timer, no activity disconnection timer, etc.

* The fourth timer/counter is used to detect interrupts from the BIC.

The SIO performs parallel-to-serial and serial-to-parallel conversion of the data on the data bus. The SIO also generates some of the modem control signals.

The I/O Register, which can be read from or written to, contains latches and buffers for the special modem control signals.

The internal loop back circuit provides the signal loop back paths for testing the transmit and receive circuits on the ASI card (with the exception of the receivers and drivers).

The 8-bit switch is used for setting the power-up state of the card. See Section 2 for switch settings.

MEMORY ADDRESS SPACE

An 8K-byte EPROM (see 2-B24, 7-1) and a 2K-byte RAM (see 2-B22, 7-1) are used for memory. The memory address space is allocated as shown in table 3-1.

I/O ADDRESS SPACE

The Z-80A CPU's I/O capability is used to access five devices:

* Power Up Default States Switches (3-A36, 7-1)
* Read/Write Register (3-D34, E34, 7-1)
* CTC circuit (3-B33, 7-1)
* BIC circuit (1-A4, 7-1)
* SIO circuit (3-B34, 7-1)

Table 3-2 shows the I/O address space.

CONFIGURATION JUMPERS

An 8-position programmed jumper is included on the ASI card. The definitions of the jumper are shown in table 3-3. The jumpers are set at the factory and should not require any additional modification.

INTERFACING TO BIC

Interface between the I/O channel and the ASI card is handled by the BIC gate array (see 1-A4, 7-1). Briefly, the BIC provides a standard method of interfacing to the I/O channel bus. I/O addresses between the BIC and the I/O channel are shown in table 3-2.

The BIC configures the direction of the data path between the backplane and the Z-80A CPU, and provides the necessary handshake signals for interfacing to the backplane.

Connections between the BIC and the Z-80A CPU are shown in table 3-4.

Table 3-1 Memory Address Map

		BIT ASSIGNMENTS			MEMORY ADDRESS
	FUNCTION	A15	A14	A13 - A0	HEX
--64K					
	Not used				FFFF H
--32K					--8000 H---
	This area is for RAM expansion	Because the RAM is always selected in this part of memory, multiple images of the RAM exist			7FFF H
--18K					--4800 H---
	RAM	X	1		47FF H
--16K					--4000 H---
	Presently not used. This location can be used to address the additional 8K bytes of EPROM.	X	0		3FFF H
-- 8K					--2000 H---
	EPROM	X	0	X	1FFF H
--- 0					--0000 H---

X=Don't Care.

Table 3-2. I/O Address Space

	BIT ASSIGNMENTS								I/O ADDRESS
FUNCTION	A7	A6	A5	A4	A3	A2	A1	A0	HEX
Power Up Switch	1	1	1	1	X	X	X	0	F0
R/W Register	1	1	1	1	X	X	X	1	F1
CTC Channel 0	1	1	0	1	X	X	0	0	D0
CTC Channel 1	1	1	0	1	X	X	0	1	D1
CTC Channel 2	1	1	0	1	X	X	1	0	D2
CTC Channel 3	1	1	0	1	X	X	1	1	D3
BIC Register 0	1	0	1	1	X	0	0	0	B0
BIC Register 1	1	0	1	1	X	0	0	1	B1
BIC Register 2	1	0	1	1	X	0	1	0	B2
BIC Register 3	1	0	1	1	X	0	1	1	B3
BIC Register 4	1	0	1	1	X	1	0	0	B4
BIC Register 5	1	0	1	1	X	1	0	1	B5
BIC Register 6	1	0	1	1	X	1	1	0	B6
BIC Register 7	1	0	1	1	X	1	1	1	B7

Table 3-2. I/O Address Space (Continued)

	BIT ASSIGNMENTS								I/O ADDRESS
FUNCTION	A7	A6	A5	A4	A3	A2	A1	A0	HEX
SIO Chan. A Data	0	1	1	1	X	X	0	0	70
SIO Chan. A Control	0	1	1	1	X	X	0	1	71
SIO Chan. B Data	0	1	1	1	X	X	1	0	72
SIO Chan. B Control	0	1	1	1	X	X	1	1	73
X = Don't care									

Table 3-3. Jumper Definitions

JUMPER	FUNCTION (IF CONNECTED)	PURPOSE
1	WE to pin 23 of RAM socket	Configuration for 2K-8K
2	A11 to pin 23 of RAM socket	Used with jumper 1
3	Enable wait state generator	Allows 450 nsec EPROM
4	Enable m1 from Z80	Manufacturing Test
5	Not used	
6	Not used	
7	Not used	
8	Not used	

Table 3-4. Connections Between BIC And Z-80A CPU

SIGNAL LINES IN BIC	TERMINATION	DIRECTION OF SIGNAL WITH RESPECT TO BIC	FUNCTION
SEL-	Output of the address Decoder for the BIC	in	Enable one of the 8 BIC registers (addressed by lower 3 bits of address bus)
INT-	CLK/TRG3 of CTC	out	Interrupt Z-80A CPU. INT- maskable by software
RESET-	RESET- of Z-80A CPU, CTC and SIO	out	Resets card when an IFC or DCL is asserted, or PPON is de-asserted
D[7:0]	D7-D0 of Z-80A CPU	in/out	Bidirectional tri-state data bus lines
DS[0]	WE- of Z-80A CPU	in	Write enable. Data will be written into one of the BIC registers
DS[1]	RD- of Z-80A CPU	in	Read enable. Data will be read from one of the BIC registers
A[2:0]	A2-A0 of Z-80A CPU	in	Address lines for addressing BIC regs.
AS-	Ground	in	Not used
XEND-	+5 through 10K resistor	in/out	Not used
DTR-	+5 through 10K resistor	in	Not used
RDY-	Floating	out	Not used
DTACK	Floating	out	Not used

INTERFACING TO RS-232-C/RS-423 DEVICES

Asynchronous serial data and modem control signals are transmitted and received through the SIO (3-B34, 7-1) and the I/O Register (3-D34, E34, 7-1), (a read/write port).

A summary of RS-232C/RS-423 signals which are supported by the ASI is presented in Section 2, table 2-4.

Z-80A SUBSYSTEM

The Z-80A CPU, SIO, and CTC control the operation of the ASI. The following paragraphs describe the operation of these components and related circuitry:

* CPU (Central Processor Unit)
* System Clocks
* SIO (Serial Input/Output)
* CTC (Counter/Timer Circuit)
* Priority Interrupt Structure
* EPROM
* Power-Up Default States Switches
* I/O Register
* Reset Circuit
* Wait State Generating Circuits

CPU (Central Processor Unit)

The CPU (2-A26, 7-1), an MOS LSI microprocessor, operates from a single 5-volt supply, uses a single phase clock, and has a typical instruction time of 1 microsecond. The data bus is eight bits wide, and the address bus is sixteen bits wide (the ASI only uses 15 bits). All CPU pins are TTL compatible. The CPU provides the intelligence for the ASI to function as a preprocessor to relieve the host computer of a majority of protocol processing.

The Z-80A CPU employs a register-based architecture which includes two sets of six general-purpose registers which can be used as individual 8-bit registers or 16-bit register pairs. Additional 8-bit registers include two sets of accumulator and flag registers, and the interrupt vector and memory refresh registers. Additional 16-bit registers include the stack pointer, program counter, and two index registers.

System Clocks

A 74LS161A counter (see 2-D22, 7-1) is used to derive two system clocks from the 14.7456 MHZ I/O channel clock signal CCLK. The names and functions of the clocks are as follows:

PHISYS, which has a frequency of 3.6864 MHZ, is used for driving the Z-80A CPU, SIO and CTC circuits.

PHICTC, which has a frequency of 1.8432 MHZ, is used as an external clock for the CTC to generate the baud rates.

SIO (Serial Input/Output)

The I/O addresses of the SIO (3-B34, 7-1) are shown in table 3-2. There are two independent full-duplex channels on the SIO, channel A and Channel B. Channel B is the primary channel, and Channel A is a secondary channel. The SIO also generates some of the modem control signals, as shown below:

INPUT MODEM CONTROL SIGNALS:

CTSB, CTSA

USed as CS (Clear To Send) for the primary and secondary channels, respectively.

DCDB, DCDA

Used as RR (Carrier Detect) for the primary and secondary channels, respectively.

SYNCA

Used to detect the change of state in DM (Data Mode) input signal. The SYNCA is initially programmed to interrupt the Z-80A at the falling edge of the input signal at the beginning of a communication. After the communication is established, the SIO interrupts the Z-80A CPU at the rising edge of the input when the communication is terminated.

OUTPUT MODEM CONTROL SIGNALS:

RTSB, RTSA

Used as RS (Request To Send) for the primary and secondary channels, respectively.

DTRB

Used as TR (Data Terminal ready) for the primary channel.

CTC (Counter/Timer Circuit)

The CTC (3-B33, 7-1) is an I/O addressable port from the Z-80A CPU perspective; its addresses are defined in table 3-2. The CTC circuit has four independent counter/timers. The functions of the counter/timers are:

Channel 0 is used as programmable baud rate generator for both channel A and channel B of the SIO chip.

Channel 1 is used as programmable baud rate generator for character-relative timing (i.e., the GAP timer). Note that character-relative timing divides the baud rate from a bit-per-second value to a character-per-second value. The number of start and stop bits are considered during the division.

Channel 2 is reserved for the use of firmware for general purposes tasks such as host ENQ/ACK timer, modem connection timer, and no activity disconnection timer, etc.

Channel 3 is used to detect BIC interrupts. Basically, the CTC interrupts when the BINT- output of the BIC goes low, and no higher priority I/O device is interrupting.

Figure 3-2 is a block diagram of the hardware for generating baud rates. Table 3-5 shows the settings of M (Prescaler of the CTC) and N (Time Constant Register of the CTC) for generating the baud rate. Figure 3-3 and 3-4 show the circuitry and the timing diagram for the BIC interrupt detecting circuits.

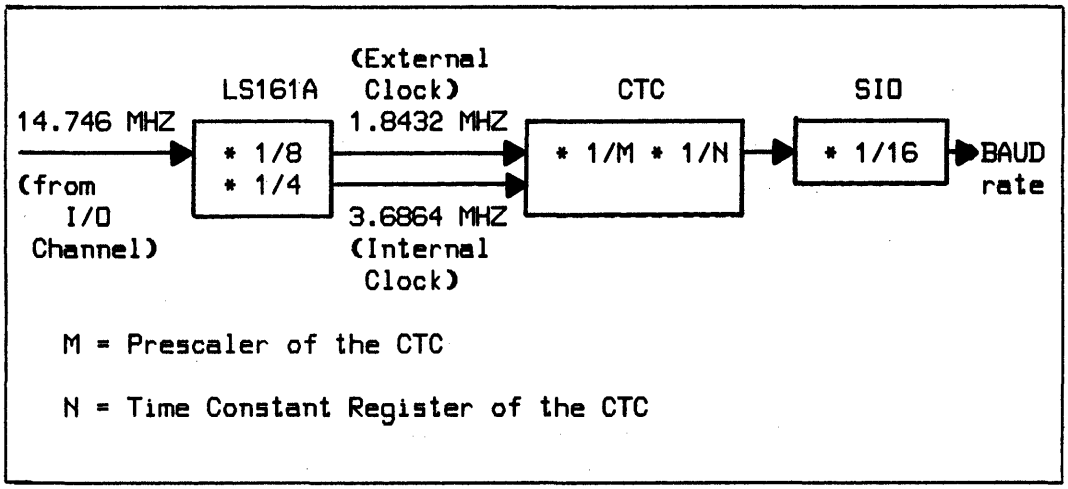


Figure 3-2. Block Diagram of the Hardware for Generating Baud Rate

Table 3-5. M and N Settings For Generating Supported Baud Rates

COUNT SOURCE	M	N	BAUD RATE	ERROR*
From external clock (1.8432 MHZ) To CLK/TRG0 of the CTC	X	6	19200	
	X	12	9600	
	X	16	7200	
	X	24	4800	
	X	32	3600	
	X	48	2400	
	X	64	1800	
	X	96	1200	
	X	128	900	
	X	192	600	
From the internal clock (3.6864 MHZ) of the CTC	16	48	300	
	16	96	150	
	16	107	134.5	0.06%
	16	131	110	0.07%
	16	192	75	
	256	18	50	

* No Error Unless Otherwise Noted

M = Prescaler Of CTC
N = Time Constant Register of CTC
X = Don't Care

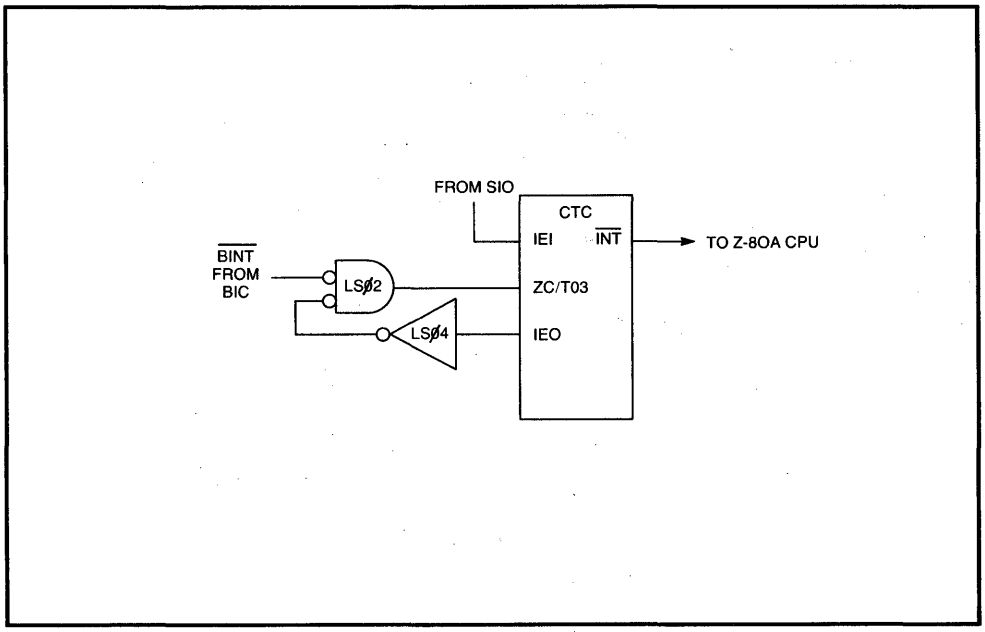


Figure 3-3. BIC Interrupt Detecting Circuits

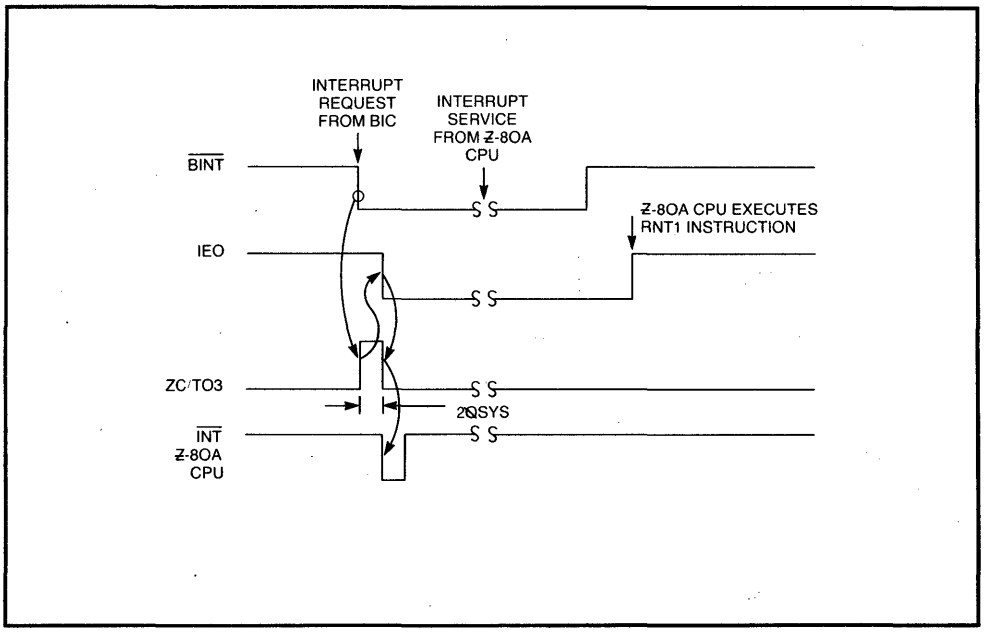


Figure 3-4. BIC Interrupt Detecting Circuits Timing Diagram

Priority Interrupt Structure

The Z-80A CPU is programmed in Mode 2 for vector interrupt. The maskable INT- (Interrupt) pin of the Z-80A CPU is driven by the open drain gates from the INT- (interrupt) pins of the SIO and CTC. The SIO and CTC are configured in a daisy-chain structure, where the SIO has higher priority.

The priority interrupt structure of the Z-80A Subsystem is:

Highest Priority

SIO Channel A Receive
SIO Channel A Transmit
SIO Channel A External/Status
SIO Channel B Receive
SIO Channel B Transmit
SIO Channel B External/Status
CTC Channel 0
CTC Channel 1
CTC Channel 2
CTC Channel 3 (BIC)

Lowest Priority

EPROM

The memory address of the EPROM (2-B24, 7-1) is shown in table 3-1. The standard EPROM has an access time of 250 nsec. The ASI can fetch instructions from this EPROM without any wait states. If the wait state generator is enabled (see jumper configuration), EPROMs as slow as 450 nS can be used.

Power Up Default State Switches

Eight switches (see 3-A36, 7-1) are provided for configuring the default state/mode of the card during power up. Definitions of the functions of the switches are shown in Section 2, table 2-1.

I/O Register

The port address of the I/O Register (U65 and U85, see 3-D34, E34, 7-1) is shown in table 3-2. This register can be read from and written to. The definitions of bits of the register are shown in table 3-6. Writes are to U85, reads are from U65. (Note that when you read the register, you do not get back what you wrote to it.)

Table 3-6. Definitions Of The Bits of the I/O Register

BIT ASSIGNMENTS								
OPER-ATION	D7	D6	D5	D4	D3	D2	D1	D0
Read	Not used						IC note 2	DM note3
Write	SR note 6	Fiber note 1	LED note 4	Self-Test note 5	not used			

Note 1: Set this bit to select TTL level read data for fiber optics.

Note 2: IC (Incoming Call), which is B19 at the card edge

Note 3: DM (Data Mode), A11,B11, A12 at the card edge

Note 4: LED Driver bit. The LED is ON when this bit is low

Note 5: When Self-Test bit is cleared, the transmitting lines will loop back to the receiving lines and the data outputs will be disabled. Bit D6 must be zero for data to loop back properly.

Note 6: SR (Data Rate Select), B21 at the card edge

Reset Circuit

The output of the Reset circuit (see 2-D23, 7-1) drives the RESET pins of the Z-80A CPU, SIO, and CTC; and the CLEAR pins of the I/O Register. The Reset circuit is activated by the RESET- pin of the BIC. When the Reset circuit is activated, its output will be pulled low for more than 3 clock cycles of PHISYS.

Figures 3-5 and 3-6 show the Reset circuit and the timing diagram, respectively.

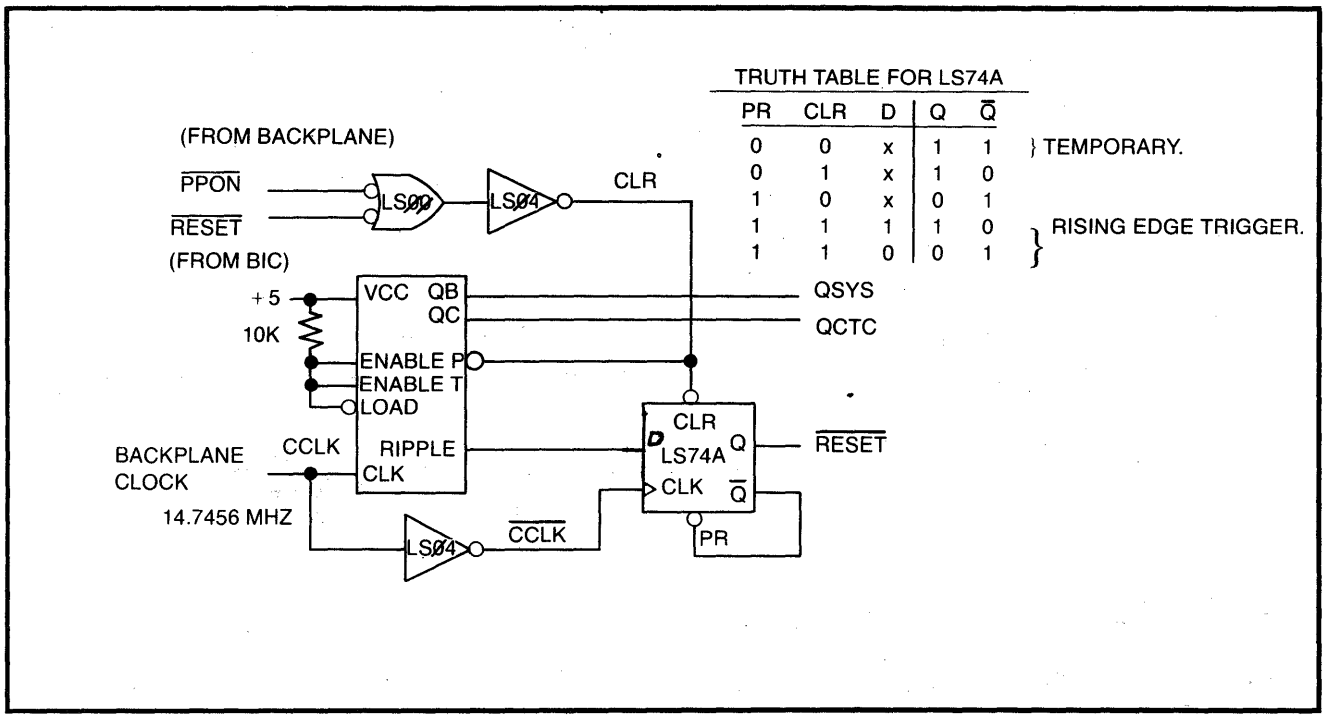


Figure 3-5. Reset Circuits

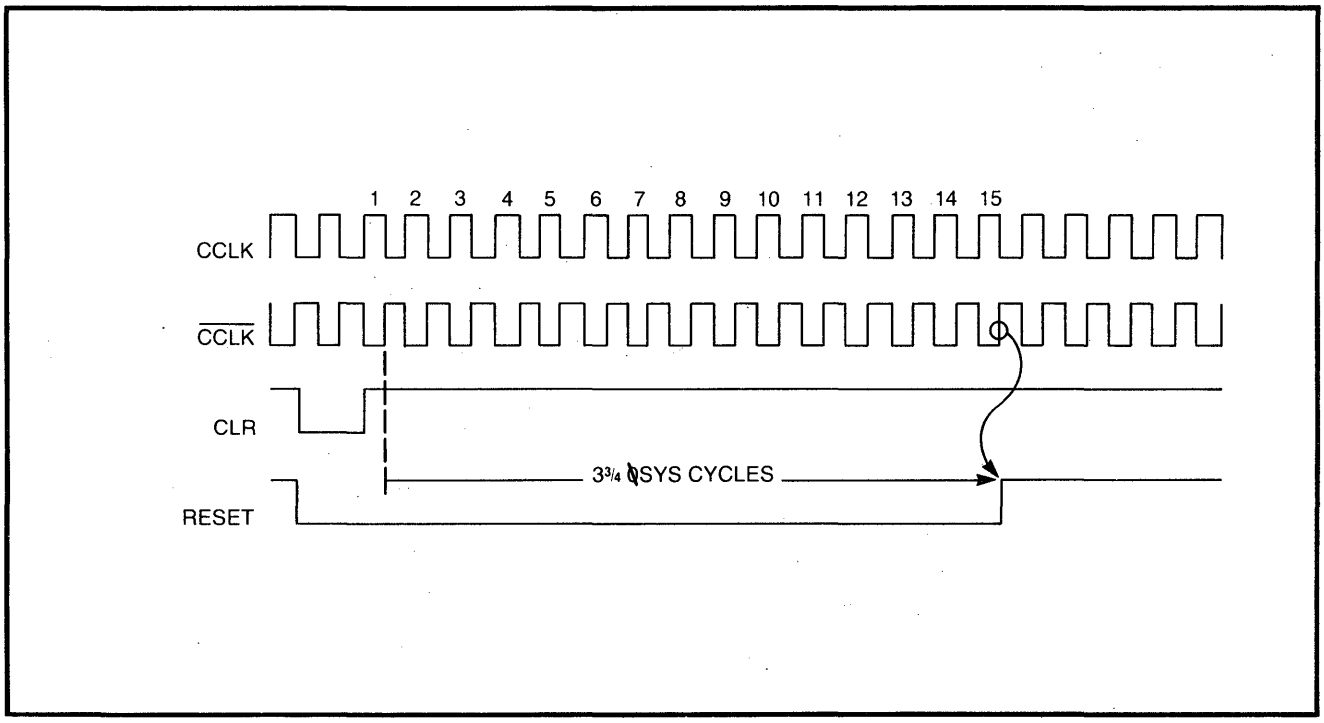


Figure 3-6. Reset Circuit Timing Diagram

Wait State Generating Circuit

The standard EPROM has a 250 nsec access time and does not require the use of the Wait State Generating circuit. Wait states are provided to allow use of slow EPROMs. The maximum memory access time that can be used is 450 nsec, which is longer than the memory access cycle of the Z-80A CPU. The Wait State Generating circuit, and its timing diagram are shown in figures 3-7 and 3-8, respectively.

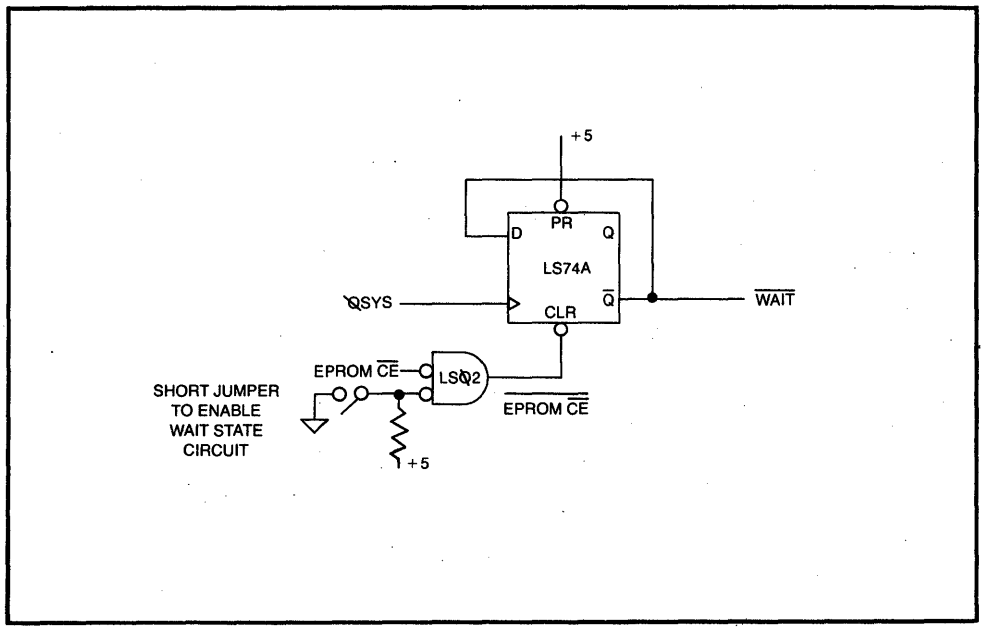


Figure 3-7. Wait State Generating Circuit

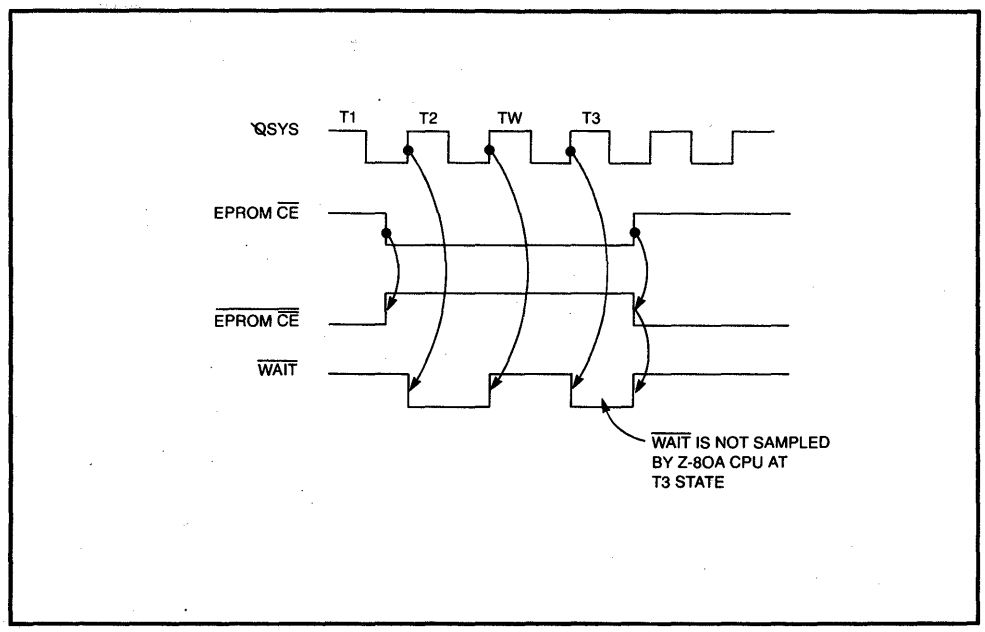


Figure 3-8. Wait State Generating Circuit Timing Diagram

PROGRAMMING

SECTION IV

Many of the ASI's firmware features are programmable by the user. Firmware features include provisions for meeting U.S. and European modem requirements. The firmware also provides complete flexibility for software handshake to most terminals, and for terminal emulation. In addition, options such as baud rate, break detection and generation, etc., are programmable.

A Z-80A microprocessor Central Processing Unit (CPU), a Z-80A Serial Input/Output (SIO), and a Z-80A Counter/Timer Circuit (CTC) allow the ASI to achieve functional flexibility. This allows modem control as well as direct interface to a wide variety of devices.

The ASI contains firmware implemented capabilities that simplify interfacing tasks for the host computer. This allows the host computer to provide more time and space for users. These firmware functions can be disabled to allow the host computer to directly control most operations so that special needs can be met.

ASI PROGRAMMABLE FEATURES

Features and options of the ASI which can be controlled programmatically are as follows:

- Types of Protocol (EIA RS-232-C and RS-423, and CCITT V.24 and V.28)
- Number of Stop Bits (1, 1.5, or 2)
- Transmission Mode (asynchronous only in simplex, full-duplex, or echoplex)
- Parity (none, odd, even, 0, or 1)
- Baud Rate (50, 75, 110, 134.5, 150, 300, 600, 900, 1200, 1800, 2400, 3600, 4800, 7200, 9600, or 19200)
- Break Detection and Generation
- Edit Mode Option to Process Backspace and Line Deletion
- Backspace Character
- Line Delete Character

- Single Text Terminator Character(s)
- Double Text Terminator Character
- Prompt Sequence Detection
- Host controlled ENQ/ACK Handshake to Device with Programmable Time-Out
- Device controlled ENQ/ACK Handshake
- Host controlled X-ON/X-OFF Handshake
- Device controlled X-ON/X-OFF Handshake
- Type-ahead Mode
- Alert 1 Mode
- Automatic Output Separator(s) for Transmitted Text
- Single Text Terminator (echo a CR-LF in echoplex mode)

PERFORMANCE

The ASI will allow communications with a terminal at 19200 baud in full-duplex mode with all the above features enabled. This mode relies on the TYPICAL HUMAN INTERACTION speed to perform some of the special character processing. If the receive data is coming in continuously with no pause between each character (as in large screen, block-mode transfer), THE CARD CAN ACCEPT THE DATA AT THAT SPEED IF ALL THE CAPABILITIES, LIKE EDIT MODE, SOFTWARE HANDSHAKE, 2-CHARACTER SEQUENCE SEARCH, ETC., ARE DISABLED. HOWEVER, ONE TEXT TERMINATING CONDITION SUCH AS SINGLE TEXT TERMINATION WITH ONE TERMINATING CHARACTER SPECIFIED, MAY BE ENABLED TO TERMINATE THE INCOMING TEXT.

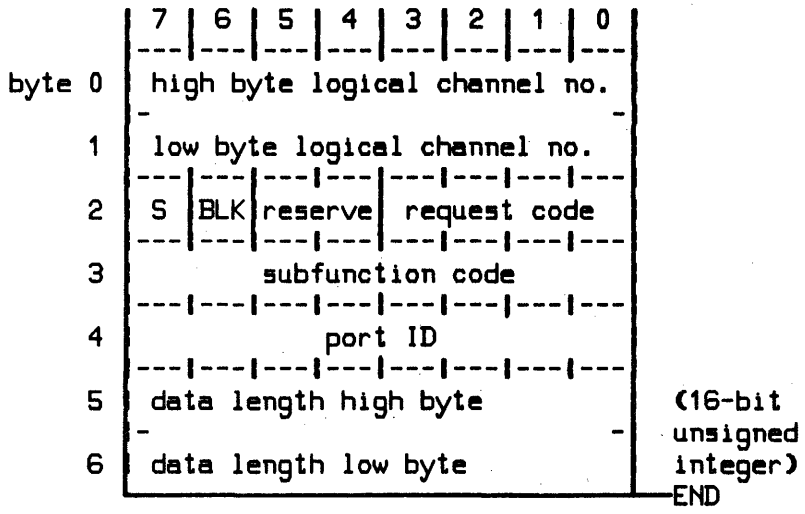
TRANSACTIONS

Each transfer between the ASI and the host computer is called a "transaction", and occurs over the I/O channel. Each transaction represents a single read or write (data, status, etc.)

Each read or write is preceded by a Connect Logical Channel (CLC) order followed by a request block from the host computer. The CLC request is in response to an SRQ signal, requesting the next order, from the ASI.

Connect Logical Channel (CLC) Request Format

The Connect Logical Channel (CLC) request block has the following format:



where

logical channel number

Assigned by the host for each transaction. The card firmware will keep the ID with each transaction until it is completed.

S bit

Used by all nonblock read device data requests and by the last block of the block read device data request. If the S bit is set, any remaining data in the current read record will be available for the next read request. If the S bit is clear, any data remaining in the current record will be discarded after the read is completed.

BLK

0 = non-block data transfer

1 = block data transfer

request code

0 = not used

1 = read device data

2 = write device data

3 = control device

4 = read card information

5 = write card configuration data

6 = control card

7 = read trace data (not available on the ASI card)

8-15 = reserved

subfunction code

The content of this field is dependent on the type of the request.

port ID

The ASI supports only one port; therefore, this value will always be zero.

data length

Required for all read or write requests. All other requests should contain zeros.

CAPABILITIES

The following paragraphs provide detailed descriptions of the ASI's capabilities.

Receive Character Processing

Each received character is processed in the following order:

1. a. If any error condition occurred, the current receive record is terminated. The record is then made available for the host. The error condition includes data overrun, parity, and framing. If the firmware is controlling a modem, the loss of the DM signal or the loss of the RR signal will also terminate the record.

   b. If the Signal Character Detection option is enabled, check for signal character match. See the paragraph "Additional Options" (see table of contents for page number) for details.

2. If any of the four software handshake options is enabled, check the character as follows:

   a. For the Host ENQ/ACK Handshake option, check the character for an ACK.

   b. For the Device ENQ/ACK Handshake option, check the character for an ENQ.

   c. For the Device X-ON/X-OFF Handshake option, check the character for either X-ON or X-OFF.

   d. For the Host X-ON/X-OFF Handshake option, send an X-OFF if there is not enough space remaining in the receive buffer.

3. If the Edit Mode option is enabled, check the character for backspacing and line deletion. If the Quoting Mode option is enabled, and an edit character is encountered, and the previously received character is a quote character, replace the quote character with the edit character.

4. If the Character Stripping option is enabled, check for the null, the "DEL", or the "FF" characters.

5. a. If the Single Text Termination option is enabled, check the character to see if it is a single text terminator. If yes, terminate the current receive record and make it available to the host. If the Strip The Single Text Terminator option is disabled, add the single text terminator to the buffer.

   b. If the Quoting Mode option is enabled and the previously received character is a quote character, replace the quote character with the single text terminator. The record is not terminated in this case.

6. If the Double Text Termination option is enabled, check each sequence of characters for a double text terminator. If a sequence is found, terminate the current receive record and make it available to the host.

7. If the Prompt Sequence Detection option is enabled, check the incoming characters for a prompt sequence. If a prompt sequence is found, terminate the current receive record and make it available to the host.

If the received character does not match any of the conditions described in conditions 1 through 7, the character is now added to the current record.

8. a. If the End-On-Count option is enabled, a check against the end-on-count is made. If the count is exhausted, the current record is terminated with the "end-on-count" termination.

   b. If the read request length is enabled, decrement the counter. If the count reaches zero, terminate the record with the "text terminated by the card, no more data" code.

   c. If the current count matches the internal buffer count limit, terminate the record with the "text terminated by the card, more data coming" code.

9. If the Alert 1 option is enabled, the card will notify the host that at least one character was received. See the paragraph "Alert 1 Read Mode" (see table of contents for page number) for a further discussion of the Alert 1 option.

As mentioned earlier, the order of processing the received character as described in steps 1 through 9 is the precedence implemented by the ASI firmware. Only one type of termination is assigned to each receive record.

The preceding descriptions frequently use the term "current receive record". The "current receive record" is the currently active record that can receive data from the device. If the current receive record does not exist, a record is created and the character, or the termination condition, is added to the record.

Note that some conditions, such as single text termination, double text termination, or prompt sequence detection may cause a generation of a record which contains no data. You should be aware that the text record may be of zero length. In this case, you will be notified of the condition that caused the termination in the request status block.

The host may post a read request to the card even when no receive data is available on the I/O channel. The card will suspend the read request until a record is received. If no read request is pending, and the card has a record available for the host, and the host interrupt mask allows "data available" interrupt, an asynchronous event is sent to the host to start the read. See the "Asynchronous Events" paragraph " (see table of contents for page number) for additional details.

Receive Error Conditions

The firmware will normally terminate the current receive record when any error condition is sensed. If the Do Not Terminate On Error option is set, the firmware will not terminate the record. Instead, a user specified replacement character will replace the bad incoming character, see the "Error Handling" paragraph (see table of contents for page number) for further details.

For data overrun, parity, and framing error, the character causing the error will be added to the current receive buffer. For the lost of DM or RR modem signal, any data remaining in the SIO receive buffer will be read and added to the current receive buffer.

Software Handshake with the Device

Four software handshakes are available between the host and the device:

1. Host controlled ENQ/ACK handshake
2. Device controlled ENQ/ACK handshake
3. Host controlled X-ON/X-OFF handshake
4. Device controlled X-ON/X-OFF handshake

Individual software handshakes are enabled by using the WCC, SF 9 (Write Card Configuration, Subfunction 9). The handshake processing firmware is enabled by using WCC, SF 1. The characters defined for the ENQ, ACK, X-ON, and X-OFF characters are programmable by using the WCC, SF 22, 23, 24, and 26. The following discussion will assume the default characters defined as follows.

handshake character	default ASCII character	hex value
ENQ	ENQ	05
ACK	ACK	06
X-ON	DC1	11
X-OFF	DC3	13

HOST CONTROLLED ENQ/ACK HANDSHAKE. This option is used to pace the data transfer from the card to the device to prevent the device from losing any data due to its slow internal processing speed.

The firmware sends an ENQ character after the pacing counter has counted down to zero. The card then waits for an ACK character before proceeding to transmit more characters from the transmit buffer. This will ensure that buffer space in the device is available.

You can program the pacing counter by using the Write Card Configuration, Subfunction 25 (WCC, SF 25). The default count is 80 bytes. The counter is decremented after each character is transmitted.

There is a programmable host ENQ/ACK timer to prevent the firmware from being hung if the ACK is lost or if the device is off-line and then comes on-line. The card will transmit an ENQ again until an ACK is received. You have the option of disabling the ENQ retry after the time-out by setting the "send message after ENQ timer time out" bit in the Write Card Configuration, Subfunction 9 (WCC, SF 9). In this case the card will proceed with the data transmission from where it stopped.

The host ENQ/ACK timer is programmed by using the WCC, SF 18. The default value used is 5 seconds.

To prevent any deadlock problems this handshake should not be enabled if the device X-ON/X-OFF handshake is enabled.

DEVICE CONTROLLED ENQ/ACK HANDSHAKE. For the ENQ/ACK handshake from the device, the card will send an ACK for every ENQ received if there is enough space available to hold 80 characters.

To prevent any deadlock problems, this handshake should not be enabled if the host X-ON/X-OFF handshake is enabled.

HOST CONTROLLED X-ON/X-OFF HANDSHAKE. This handshake protocol allows the card to pace the data transfer from the device to the card. The card will send the X-OFF character (DC3 or CTRL-S) to the device to stop data transmission when there is not enough space in the receive buffer (the user has at least ten character times to stop transmission). The card will send the X-ON character (DC1 or CTRL-Q) when buffer space becomes available again.

If the device continues to transmit data to the card after the card has sent an X-OFF, the data will be added to the receive buffer until it overflows. Once the data buffer overflows, data will be lost. If echoing is enabled, the received data will be echoed even if the device had sent an X-OFF.

To prevent any deadlock situation, the card will transmit the X-ON character even if the device has sent an X-OFF character. This handshake should not be used if the device ENQ/ACK handshake is enabled.

DEVICE CONTROLLED X-ON/X-OFF HANDSHAKE. This handshake protocol allows the device to pace the data transfer from the card to the device. The device will signal the card to stop transmitting data by sending an X-OFF character. The receiving device restarts data transmission by sending the X-ON character, or by sending any characters if the Implicit Device X-ON option is enabled with WCC, SF 31.

The ASI firmware will stop data transmission as soon as the X-OFF character is received; however, up to two characters may be transmitted before the stoppage.

To prevent any deadlock situation, this handshake should not be enabled if the host ENQ/ACK handshake is enabled.

Edit Mode

The Edit Mode option is enabled by setting the Edit Mode bit in the data block of the WCC, SF 1. The Edit Mode option is disabled by clearing the Edit Mode bit.

When working at a terminal connected to this card, 2 types of editing capabilities are available. The first is backspace, which deletes the previously typed character; and the second deletes the current line. In addition, a Quoting Mode option allows the insertion of the edit character into the text buffer without performing any editing.

BACKSPACE. The firmware uses the character BS (hex 08) to indicate a backspace function. This character is generated by pressing the BACK SPACE key or by typing CNTL-H. In addition, you can programmatically change the backspace character to any desired character by using the WCC, SF 6.

Three options are available to indicate that a backspace has occurred when the card is in echoplex mode. The first option is "backspace echo". This option echoes a backslash character, followed by the character that was deleted from the input buffer. The second option is "backspace overwrite". This option is very useful for CRT-type terminals. The firmware backspaces a character, writes a space character, and then backspaces again.

The third option is "backspace only". This option echoes only the backspace character to move the cursor under the deleted character.

The Backspace option is programmable by using WCC, SF 8.

If you have used backspace to delete the current line, any further backspace will cause no action.

Note that if the Do Not Terminate Text Record On Error option is enabled, the error bit in the text terminator code will not be cleared even if the bad character is deleted by backspacing.

LINE DELETION. The firmware uses the character DEL (hex 7F) as the line deletion character. As with the backspace character, you can program the line deletion character by using the WCC, SF 7.

The line deletion character causes the card to delete the current line, if any. If the card is in echoplex mode, it will write one backslash, then do a carriage-return/linefeed.

Character Stripping

You have the option of stripping certain characters from the input stream. This includes stripping null's, DEL's, and FF's (base 16). Any character stripping, except for text terminator character stripping, must be enabled by setting the Character Stripping option in the data block of the WCC, SF 1. If the Character Stripping option is enabled, you specify which character to strip with the WCC, SF 8.

Note that the "DEL" character is also used in edit mode to delete a line. If the Edit Mode option is enabled and "DEL" is the line deletion character, the "DEL" character will be processed as a line deletion character.

You also have the option of not stripping any text terminators by using the WCC, SF 8. Normally, all text terminators are stripped. For single text termination, the character is always returned in the event status block and the request status block.

Single Text Termination

For single text termination, you have the option of determining which characters are to be used as the text terminator. An example of a single text terminator is the carriage-return character (CR, 0DH).

The Single Text Termination option is enabled by setting the End On Single Text Terminator option in the data block of the WCC, SF 1.

The single text terminator characters are programmed by specifying the actual ASCII characters by using the WCC, SF 32. The number of single text terminators is limited to eight characters.

A Quoting Character Mode option allows the insertion of a specific single text terminator into the text buffer without terminating the record.

Double Text Termination

For text termination by a two-character sequence, you can only specify one set of two characters to terminate the text by using the WCC, SF 29. An example of a two-character sequence is carriage-return/linefeed (CR/LF or 0DH 0AH).

The double text terminator is not added to the current receive record unless the stripping text terminator option is disabled. The card will tell the host in the message type of the event or the request status block that a double text terminator was received.

The double text termination option is enabled by setting the End On Double Text Terminator option in the data block of the WCC, SF 1.

Note that there will be no back tracking for double text termination and prompt sequence detection when edit mode is enabled. An example will illustrate the problem: Assume the double text terminator is programmed for the characters "X" and "Y", respectively. You type "X", "W", <backspace>, "Y". No double text termination will be detected for this case. You must correct the mistake by erasing the two characters and retyping the desired characters "X" and "Y". Furthermore, if the first "X" should cause a record termination for any reason, no correction to the mistake is possible.

Prompt Sequence Detection

The Prompt Sequence Detection option can be configured to be either a one- or two-character sequence. This option functions the same way as the double text terminator described above, except the message type in the event or request status block will indicate termination by a prompt sequence.

The Prompt Sequence Detection option is enabled by setting the End On Prompt Sequence option in the data block of the WCC, SF 1. The prompt sequence is programmed by using the WCC, SF 30. The prompt sequence length is implied from the data transfer length given in the logical channel transaction request block.

End-On-Count Termination

The End-On-Count Text Termination option is enabled by setting the End-On-Count option in the data block of the WCC, SF 1. The count is programmed by using the WCC, SF 2. When the count decrements to zero, the current receive record will be terminated with the message type indicating an end-on-count. The count is then reset to the programmed value for the next record.

The End-On-Count option should not be confused with the internal card end-on-count which is set by the ASI firmware to 200 bytes. This internal count is used to manage the receive buffers on the card. When this count is exhausted, the current record will be terminated and will be made available to the host. The termination type will be set to "message terminated by the card, more data coming". This procedure allows the host to start reading data from the card while the card is still receiving data from the device.

Alert 1 Read Mode

When this mode is enabled, and if there is no read device data request pending on the card, and if none of the conditions discussed above were encountered to terminate the record, the firmware will notify the host by a "data available" event that at least one character was received. The host should post a read device data request upon receiving this notification. The card will return all characters received from the time that the alert event status was posted up to the execution of the read. The read buffer must be large enough to hold the maximum number of characters; otherwise, data will be discarded unless the S-bit is set.

If any of the text termination options discussed above are enabled, they may terminate the record early and the host will receive the text termination code and not the alert code for the message type.

If the alert 1 read mode is enabled and the host posts a read device data request, the card will not suspend the read when no data is available on the I/O channel-to-card interface ("backplane") or the ASI-to-device interface ("frontplane"). Instead, a transmission log of zero length will be sent.

The alert 1 read mode is enabled by setting the alert 1 bit in the data block of the WCC, SF 3. When the mode is enabled, and there <u>is</u> data on the frontplane, and there is <u>no</u> data on the backplane, a "data available" event will be generated immediately.

In summary, the alert 1 read mode has the following characteristics:

1. If the backplane has no receive record, an event will be generated when the frontplane receives a character which does not meet any of the terminating conditions described above. See the "Asynchronous Events" paragraph (see table of contents for page number) for information on when the character is not generated.

2. If the backplane has no receive record and the frontplane has an active record, the backplane will cause the frontplane to terminate the record to satisfy the read.

3. If the backplane and the frontplane both have no active record, the read will be terminated immediately with a transmission log of zero.

The text terminating code will always be alert 1.

Type Ahead and Echoing

The card has enough RAM space to buffer several text lines. This will allow the device to send many lines before stopping.

If the receive buffer should become full, any new incoming data will be lost. If echoplex is enabled, you will notice this when the typed character is not echoed.

NOTE

IF YOU SHOULD CHANGE ANY OF THE READ PARAMETERS, SUCH AS TEXT TERMINATION OPTION, END-ON-COUNT, AND SO ON, THE NEW PARAMETERS WILL NOT AFFECT ANY TEXT RECORD THAT HAS ALREADY BEEN TERMINATED. IF THE FRONTPLANE HAS AN ACTIVE RECEIVE RECORD, THE SINGLE-TEXT TERMINATORS, THE DOUBLE-TEXT TERMINATOR, THE END-ON-COUNT, OR THE PROMPT SEQUENCE RECONFIGURATION WILL BECOME ACTIVE AFTER THE CURRENT RECORD IS TERMINATED. OTHERWISE, THE NEW READ PARAMETERS WILL BECOME EFFECTIVE IMMEDIATELY.

In echoplex mode, if a transmit record is active, any incoming characters will be echoed after the transmit record is empty. This should prevent incoming characters from interrupting any outgoing escape sequences, which are less than or equal to 200 bytes. However, if software handshaking is enabled, the handshake characters will not be prevented from interrupting any outgoing text.

Character echoing is enabled by setting the echo bit in the data block of the WCC, SF 1. Echoing is only available for full-duplex transmission mode.

The card will not echo any double text termination or prompt sequence characters. However, the card can be enabled to echo a CR-LF for every CR received as a single text terminator by setting the "echo CR-LF for CR text terminator" in the data block of the WCC, SF 9. By using the WCC, SF 27, you may select which single text terminator in place of the CR to cause the CR-LF echoing. Furthermore, the card can be enabled to echo all single text terminators which do not match the one used to echo a CR-LF. This selection is made by using WCC, SF 9.

NOTE

THE ASI HAS A 128-BYTE CIRCULAR ECHO BUFFER. IF THIS BUFFER SHOULD OVERFLOW, ECHO INFORMATION WILL BE LOST. HOWEVER, THIS WILL NOT AFFECT THE RECEIVE TEXT BUFFER. THE OVERFLOW CONDITION IS USUALLY CAUSED BY TYPING IN DATA WHEN THE ASI HAS RECEIVED A TERMINAL X-OFF CHARACTER OR WHEN A HOST ACK IS NOT SENT FOR A HOST ENQ.

Receiving Transparent or Binary Data

Transparent, or binary, data is defined to be data read with no processing by the firmware. The data is always terminated by using the End-On-Count option. All special processing such as software handshake, edit mode, single text termination, double text termination, prompt sequence detection, and character stripping, should be disabled. However, any type of error condition will terminate the binary read early, unless the Do Not Terminate The Text Record On Error option is set.

Function of Read Request Length

The read request will invoke the special read processing when:

1. No current receive record is available on the I/O channel,

   and

2. Alert 1 read mode is disabled.

If the special read processing is invoked, the firmware will perform two different types of actions depending on the status of the data on the frontplane. If the frontplane has a current record which can satisfy the read request, the record will be terminated with the "text terminated by card, no more data" code and given to the backplane to satisfy the read request.

NOTE

IF THE READ REQUEST HAS THE S-BIT SET, ANY FUTURE READ WILL BE SATISFIED BY THE REMAINING DATA IN THE CURRENT RECORD UNTIL THE BUFFER IS EXHAUSTED.

The preceding note has several implications. If the next read request length exceeds the remaining data, the read will be terminated early with the above termination code. Note that the read request length will not be satisfied. If the read request length is less than the remaining data length, the read will be satisfied by the given length. If the S-bit is set, the remaining unread data will be available for future read requests. Furthermore, if enabled for the data available event, no event will be generated until the current record is empty.

If the frontplane has no active receive read or if the frontplane receive record is less than the read request length, the firmware will set the downcounter to the remaining count needed to satisfy the read. The firmware will suspend the read request until the receive record is available for the backplane.

In either case, the terminating code for the record is "card terminated read, no more data".

Host Initiated Text Termination

There are many occasions when the host would like to terminate data transfer early without losing what has already been read. For example, an application may require the read to be terminated by satisfying the length, or by timing out.

Control card request with subfunction 4 would allow the host to terminate the frontplane receive record with the "host initiated text termination" code. If no read request is active, a receive record will be generated and it may or may not contain data. However, no record is generated if there is no buffer space.

TRANSMIT CHARACTER PROCESSING

If echoing or software handshaking is enabled, the transmit interrupt processor will give priority to those characters before transmitting any user data. However, if a current transmit record is active, the echoing will be delayed until the current record is empty, see the "Type Ahead and Echoing" paragraph (see table of contents for page number) for additional details.

Automatic Output Separators Appendage

The firmware will append one or two characters to the transmitted message depending upon the write option. To enable the Automatic Output Separator Appendage option, the "write device data subfunction code" must be set to 1 for each write request. To disable the appendage, set the subfunction code to 0. The output separator is programmed by using WCC, SF 28. The output separator length is obtained from the data transfer length given in the write control request block when the output separator is programmed.

Transmitting Transparent or Binary Data

Transparent, or binary, data is defined to be data written with no intervention by the firmware. This may be achieved by disabling the options Automatic Output Separators Appendage and Conditional Output Separators Appendage. Furthermore, echoing and software handshaking must also be disabled to eliminate those characters from being transmitted within the user's binary data.

Transmit Hardware Handshaking

You must manually control all hardware handshaking such as RS/CS. The handshake control is performed by using the control device request with subfunctions 4 through 11.

You can determine the state of the modem signal by polling, or by configuring for an interrupt on line state change.

Force Restart of the Transmitter

A control card request with subfunction 5 is available for the host to restart the transmitter if the transmitter is stopped due to waiting for a host ACK or a device X-ON character from the device or terminal. This option is normally used when the handshaking is enabled, then disabled by the host software without determining the state of the card's firmware.

BUFFER FLUSHING

Several control card requests (see paragraph "Control Card, Request Code = 6") are provided to flush or clear any receive or transmit records on the card. The control card request with subfunction 1 or 2 is used to flush the current receive buffer, and to flush all the data in the receive buffers, respectively. The control card request with subfunction 3 is used to flush all the queued transmit buffers.

The current receive buffer is defined to be the record for the next host read. If the S-bit is set for the host read and if there is any data remaining, the remaining data is the current receive buffer. If the previous read has the S-bit set and there is no remaining data, the current buffer is defined to be the next record for the host read.

If no buffer exists on the card, the control card request will be a no op.

PROGRAMMING THE RECEIVER AND TRANSMITTER

The selection of the transmission mode is programmed by using the WCC, SF 5. The main selection is between hardwired and modem. If the modem mode is selected, the firmware will control all the modem signals. In the hardwired mode, the firmware provides no modem signal control. Data received will be added to the buffer, and data will be transmitted regardless of the modem signal state.

Simplex receive and simplex transmit are provided to turn off the transmitter and receiver, respectively.

The character size for the receiver and the transmitter may be specified at 5, 6, 7, or 8 bits per character, not including an optional bit for even or odd parity. On transmit, the user data will be processed byte-by-byte, passing the 5, 6, 7, or 8 least significant bits in each byte to the transmitter, depending on the programmed character size. A parity bit will be added by the ASI if even or odd parity is enabled. On receive, the incoming data will be passed to the user's buffer into the 5, 6, 7, or 8 least significant bits of each byte, with the unused bits being zeros. The parity bit is never returned to the user. The character length is programmed by using WCC, SF 11. The format of an asynchronous message is shown in figure 4-1.

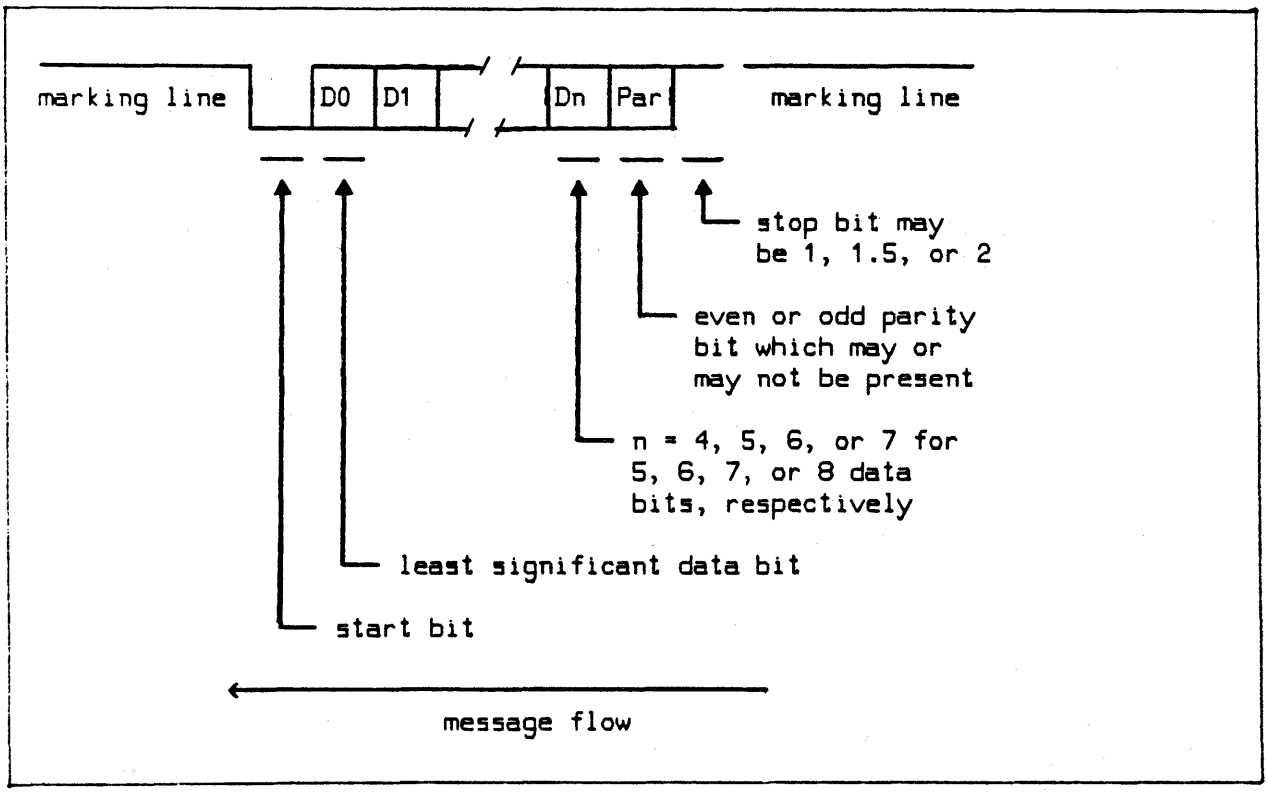


Figure 4-1. Asynchronous Message Format

The baud rate and the number of stop bits are programmed by using the WCC, SF 10 and 12, respectively.

PARITY IN TRANSMITTED OR RECEIVED DATA

There are five parity options available for transmitted or received data:

no parity

odd parity

even parity

'0' parity

'1' parity

The first parity option generates no parity nor will it check for any parity. The character length specified is the actual data element sent and received.

The second and third parity options cause the generation and detection of parity for the transmitted and received data, respectively, by the SIO. An additional bit is added to the data element for parity.

The fourth and fifth parity options clear or set the most significant bit of every character transmitted. For the character length of 5, 6, 7, or 8 bits, the 5th, 6th, 7th, or 8th bit, respectively, of the character will be clear or set before the character is transmitted. On incoming characters, the force parity bit will be stripped with no checking.

The parity option is programmed by using the WCC, SF 13.

You may transmit with parity and receive with no parity by setting the Ignore Parity Error option in WCC, SF 13. See the paragraph "Error Handling" for additional details.

BREAK DETECTION AND GENERATION

The firmware notifies the host of receiving a break from the device by sending an unsolicited event status, if enabled.

The host can request the ASI to generate a break condition for the device as soon as the control device request with subfunction 3 is received. The break generation length can be programmed by the host, see the "Break Timer" paragraph.

TIMERS

The ASI provides the following timers:

1. **Modem Connection Timer.** This is the time allowed to establish modem connection by waiting for the DM and RR signals for full-duplex modem. If the DM and RR signals are not asserted within the time given, the line connection request from the originating mode will be aborted. For the auto answer mode, the firmware will go back into the waiting for the IC signal mode. The default value is 25 seconds. The clock resolution is 1 second. The timer can be programmed from 0 to 255 seconds by using the WCC, SF 14.

2. **No Activity Disconnect Timer.** This time is used to prevent excessive connect charges from being incured due to no activity over a modem connection. The default value is 600 seconds. The clock resolution is 1 second. The timer can be programmed from 0 to 65535 seconds by using the WCC, SF 15.

3. **Lost Receiver Ready Timer.** For full-duplex modems, this timer is activiated by the firmware whenever the RR modem control signal is lost. If the control signal should return before the timer times out, the timer will be reset to 0. If the timer times out before the control signal returns, the firmware will lower TR and RS and inform the host of the disconnection.

   The ASI firmware also uses this timer during the initial modem connection phase. When the DM signal is first asserted, this timer is started. After the timer has timed out, the firmware checks the DM signal. If the signal is still asserted, a successful modem connection has been established. Otherwise, the firmware will continue the modem connection sequence.

   The resolution of the timer is 10 milliseconds. The default is 400 milliseconds. The timer range is from 0 to 2550 milliseconds (0 to 255 counts) by using the WCC, SF 16.

4. **Gap Timer.** The firmware inserts a time delay between each character transmitted to the device. The time count is character relative. The default is zero. The resolution is 1 character. The timer can be programmed from 0 to 254 characters by using the WCC, SF 17. (Note that the value 255 is the same as 0.)

   An active gap timer will not prevent the transmission of the host X-OFF character for the host X-ON/X-OFF handshake. This is used to prevent data overrun on the receiver when the gap timer is set to a large value.

5. **Host ENQ/ACK Timer.** The firmware will wait up to the specified time out for the ACK. If the ACK is not received within the time given and if the ENQ retry is enabled, an ENQ is sent again. This continues until an ACK is received. The default value will be 5 seconds. The clock resolution is 1 second. The timer can be programmed from 1 to 255 seconds by using the WCC, SF 18.

6. **Break Timer.** This is the wait time for break generation. The timer is character relative. The resolution is 1 character. The default is 4. The timer can be programmed from 2 to 255 characters by using the WCC, SF 19.

For all of the timers except for the Break Timer, a zero value will defeat the timer; that is, there will be no time out.

MODEM SUPPORT

The following modem lines are supported by the ASI:

signal direction card	device	modem line description	EIA RS-449 symbol
-->		send data	SD
<--		receive data	RD
-->		request to send	RS
<--		clear to send	CS
<--		receiver ready	RR
-->		secondary request to send	SRS
<--		secondary clear to send	SCS
<--		secondary receiver ready	SRR
<--		incoming call	IC
-->		terminal ready	TR
<--		data mode	DM
-->		signal rate selector	SR
<->		signal ground	SG

Host Control of the Modem Signal

When the ASI is not set to full-duplex modem transmission mode, the firmware will not provide any modem control. However, you may control all the modem lines by using the control device request subfunctions 4 through 11. Subfunctions 4, 6, 8, and 10 will set the specified lines until they are cleared by subfunctions 5, 7, 9, 11, respectively. Any timers for modem control will not be active. No error checking will be provided, such as checking for lost DM.

The firmware allows the host to specify the option of receiving an unsolicited event interrupt if there are any changes in the input modem lines. This is accomplished by setting the appropriate interrupt mask by using WCC, SF 21.

Firmware Control of the Modem Signal

When the ASI is enabled for full-duplex modem transmission mode, the firmware provides full modem control as described below. Note that none of the secondary modem control lines are controlled by the firmware. They are controlled by the host as described above.

There are three modem control timers implemented by the card firmware: the modem connection timer, the no activity disconnect timer, and the lost receiver ready timer. The modem connection timer is used to time the initial connection. It may be disabled or set to a value up to 255 seconds (default is 25 seconds). The no activity disconnect timer disconnects the modem if there is no transmit or receive data activity in the specified time interval. It may be disabled or set to a value up to 65535 seconds (default is 600 seconds). The lost receiver ready timer times a loss of receiver ready (RR) for full-duplex modem. Its default value is 400 milliseconds; however, it may be disabled or set to a new value up to 2.5 seconds.

The lost receiver ready timer is also used in the initial modem connection phase. Upon receiving the DM signal, the timer is started. After the timer times out, the firmware checks the DM signal. If the DM signal is still asserted, a successful modem connection was made. Otherwise, the firmware continues the modem connection sequence by waiting for the DM signal for the originating mode, or by restarting the IC poll for the answer mode.

The terminal ready (TR) signal is set low whenever the data mode (DM) signal is lost after the link has been opened. In addition, the request-to-send signal is turned off for full-duplex modem.

If the ASI is configured for modem control, it will not transmit or receive data until the host has performed a line connection request by using the control device request with subfunction 1.

There are two ways of connecting a modem: The first is answer mode where the card will wait for an incoming call, and the second is origination mode where the card will initiate the call or connection. The answer mode is enabled by specifying a zero in the data block for the WCC, SF 4. The originating mode is enabled by specifying a one for the data block for the WCC, SF 4.

Full-Duplex Modem

The full-duplex modem connection uses the send data (SD) line to send data to the modem, and the receive data (RD) line to accept data from the modem. The request to send (RS), clear to send (CS), data mode (DM), receiver ready (RR), and incoming call (IC) lines are used to handshake with the modem. The secondary request to send (SRS), secondary receiver ready (SRR), and signal rate selector (SR) lines can be controlled by the host.

In answer mode, the firmware waits for the IC line to be asserted. The firmware then responds by asserting the RS and TR signal and starting the modem connection timer. These lines are deasserted if DM and RR are not turned on when the timer times out. In this case, the firmware will return to the mode of waiting for the IC signal. The solicited event for the link open request will not be returned until an actual modem connection has been established.

To originate a call, TR and RS are asserted and the modem connection timer will be started. These lines are deasserted if DM and RR do not turn on within the time out of the timer. In this case the card will return a solicited event indicating that the open request failed.

Once a connection has been established, the firmware enables the no activity disconnect timers.

FULL-DUPLEX MODEM TIMING DIAGRAMS. Figures 4-2 through 4-7 contain timing diagrams for full-duplex modem functions.

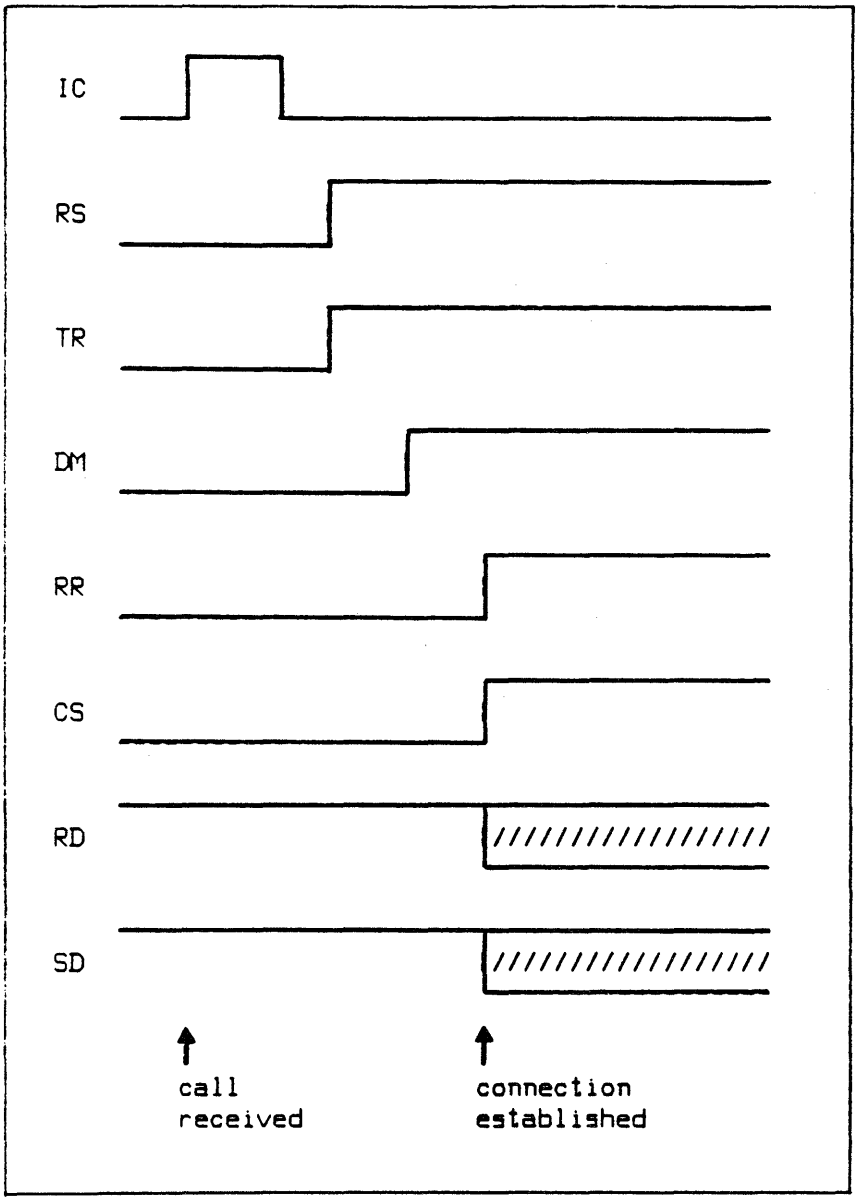


Figure 4-2. Timing Diagram, Normal Connection - Auto Answer

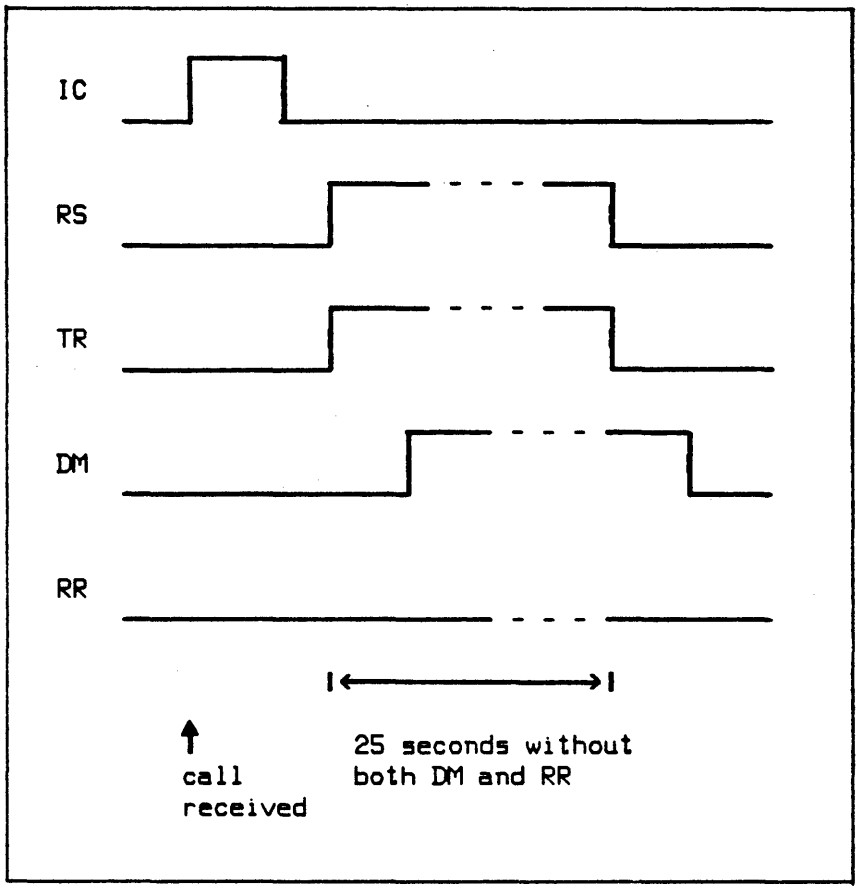


Figure 4-3. Timing Diagram, Wrong Number Call - Auto Answer

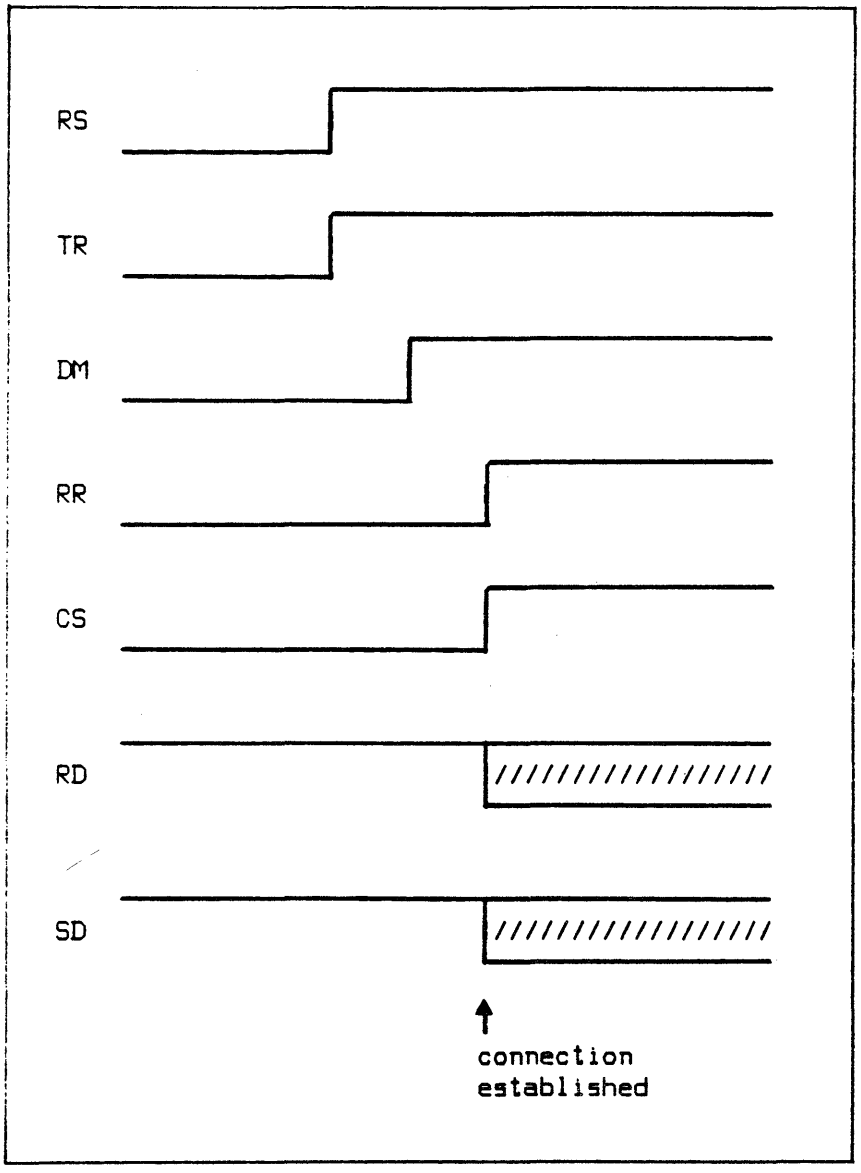


Figure 4-4. Timing Diagram, Normal Connection - Originate

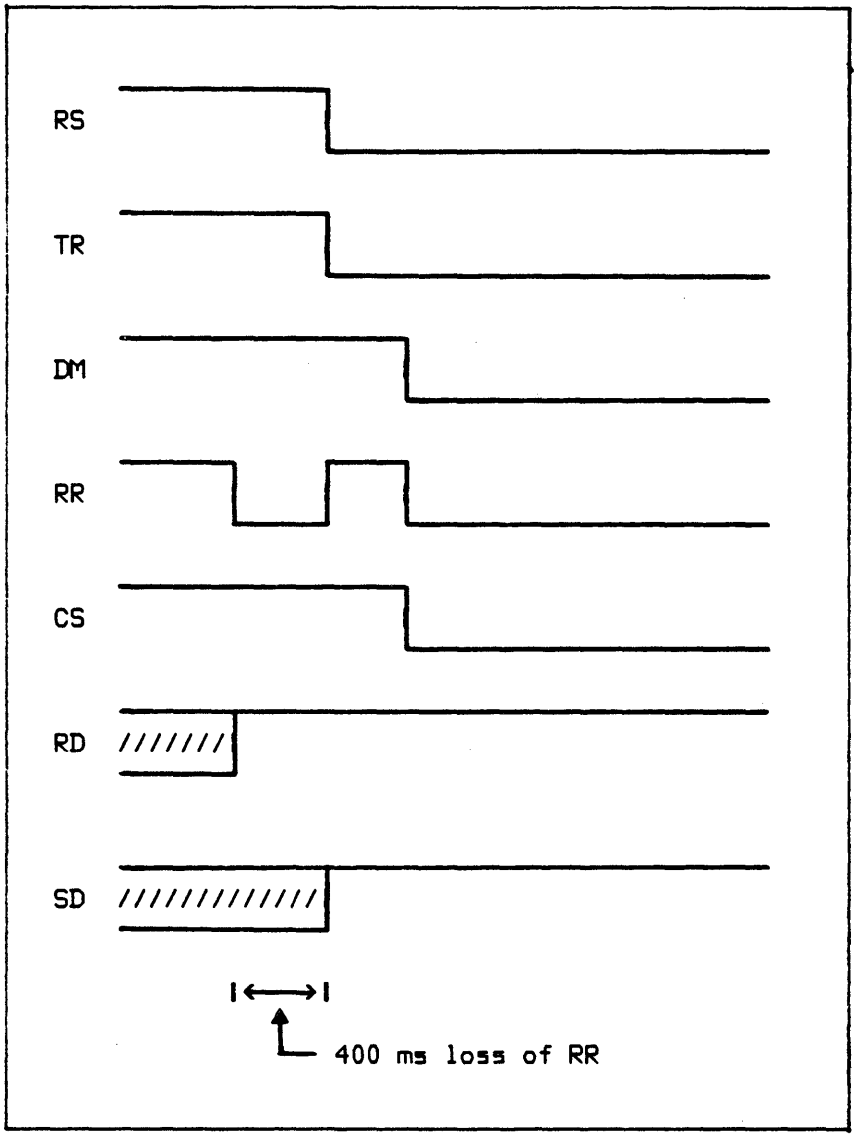


Figure 4-5. Timing Diagram, Lost Receiver Ready Disconnect

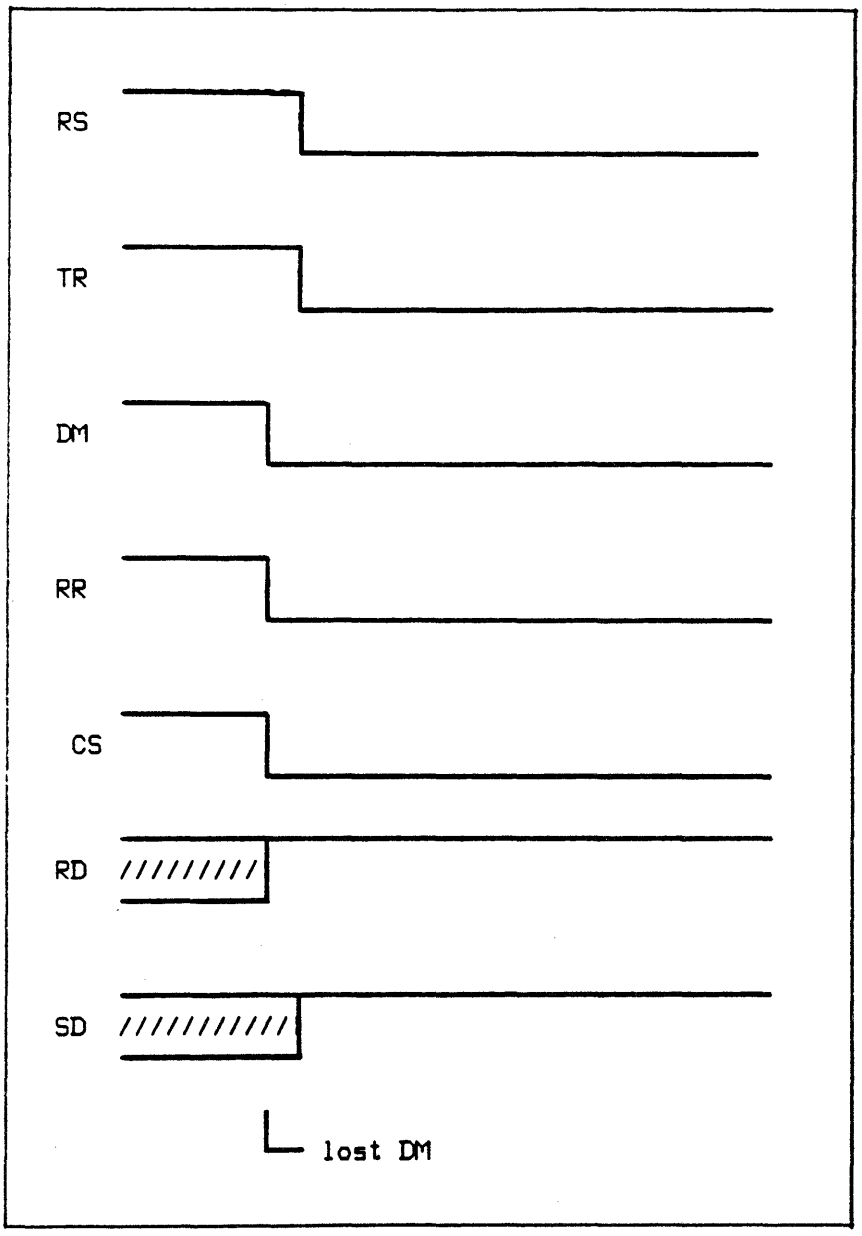


Figure 4-6. Timing Diagram, Lost Data Mode Disconnect

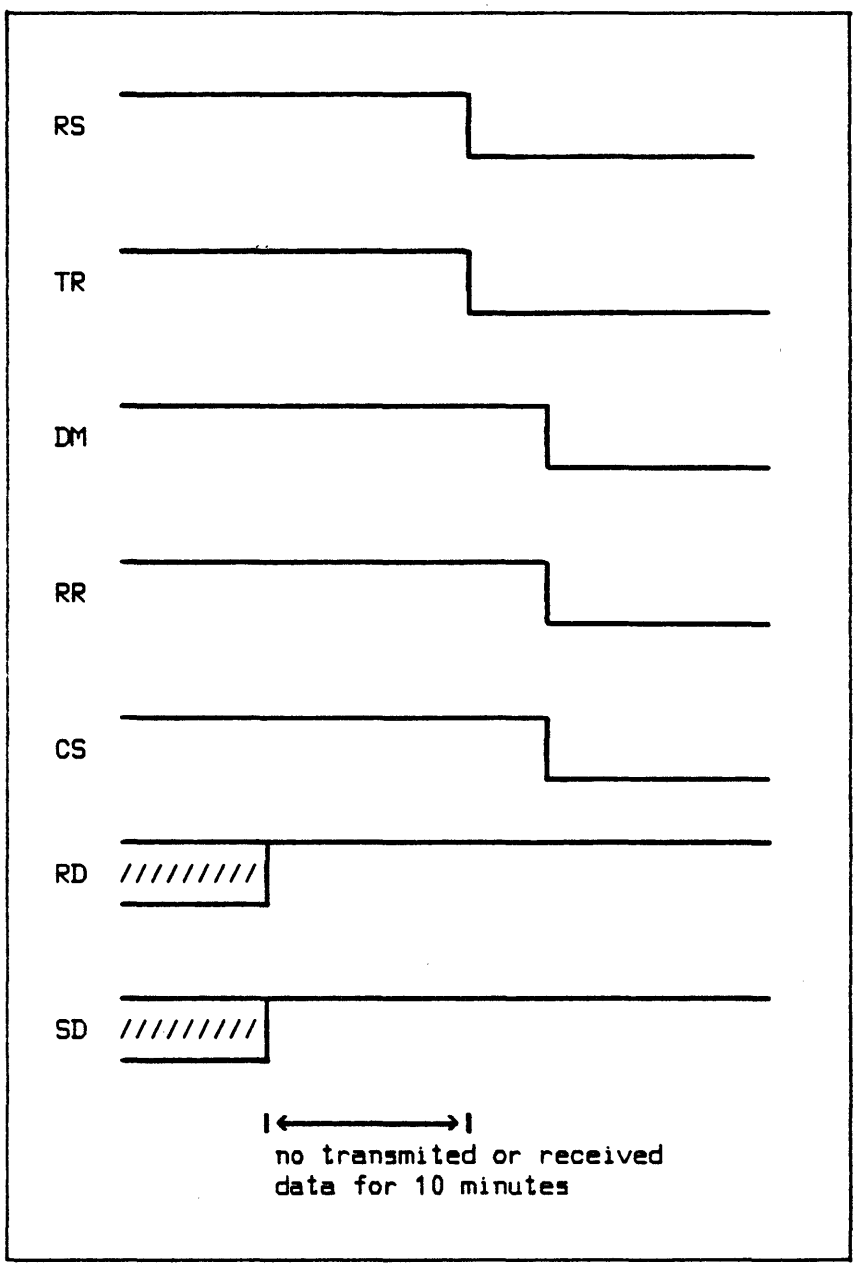


Figure 4-7. Timing Diagram, No Activity Disconnect

ADDITIONAL OPTIONS

Six additonal options are available for special use, as follows:

1. Do not terminate the text record on errors
2. Quoting character mode
3. Conditional output separators appendage
4. Signal character detection
5. Implicit device X-ON
6. Insert the null character into the receive buffer when a break condition is detected.

All six options are configured by using write card configuration, subfunction 31 (WCC, SF31).

Error Handling

Under normal ASI firmware operation, the incoming text is terminated when any error is encountered. Furthermore, the character causing the error is added to the text record for the host. This allows the host to detect undesirable error conditions.

If the Do Not Terminate Text Record On Error option is enabled, the firmware will not terminate the text record. The incoming character with the error will be replaced by the user-specified replacement character which has a default value of 7FH ("DEL"). The replacement character will be added to the text buffer and will be echoed, if echoing is enabled.

If the Ignore Parity option in WCC, SF 13 is set, the firmware will ignore all parity error conditions. The character will be processed as if no error had occurred.

Finally, if the Ignore All SIO Errors option in WCC, SF 13 is set, all received characters with an error will not be processed. However, the error bit in the termination code will be set to indicate that an error had occurred and that characters have been discarded.

Figure 4-8 contains a flow diagram showing how a received character with an error is processed.

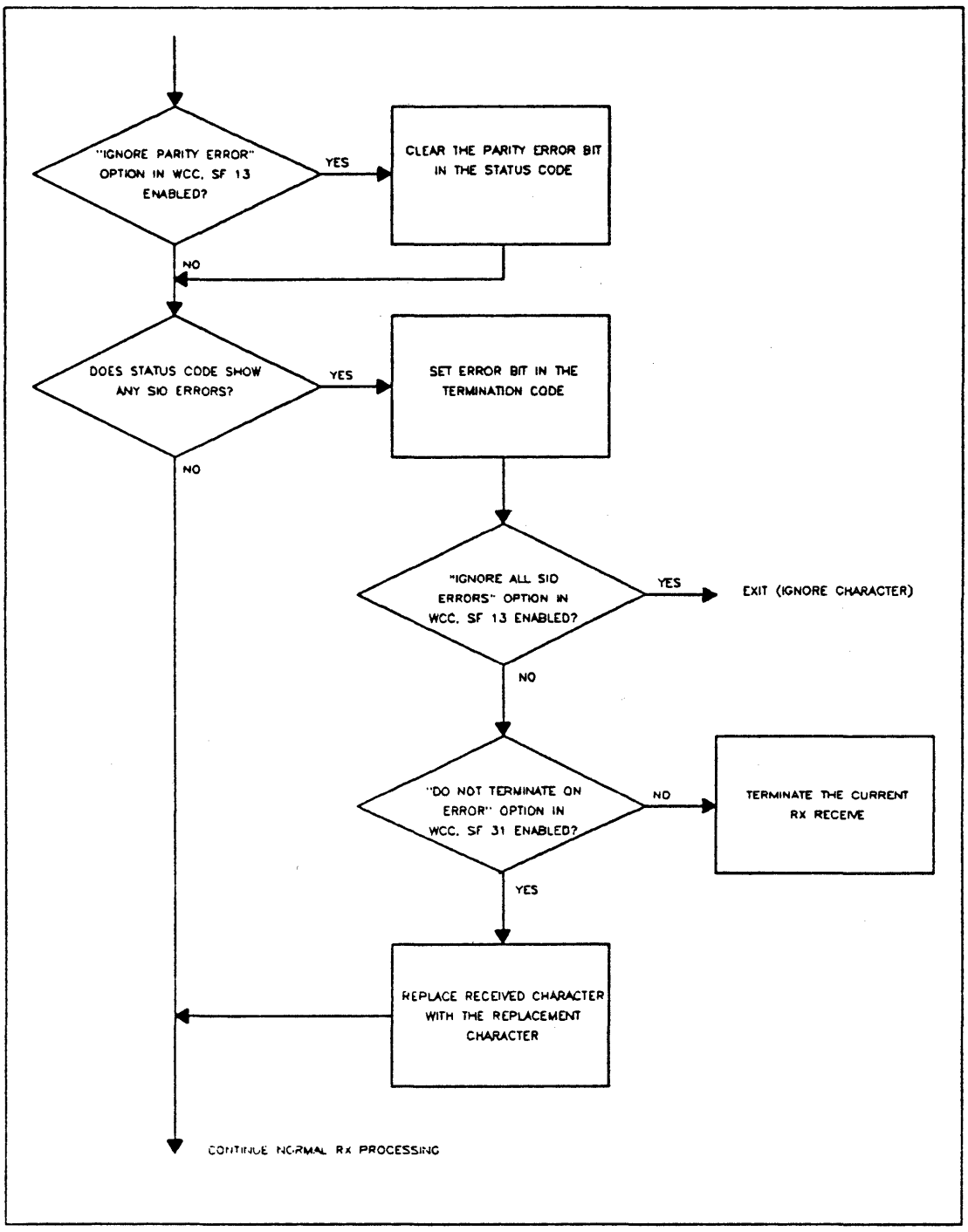


Figure 4-8. Error Handling Flow Diagram

INTENTIONALLY BLANK

Quoting Character Mode Option

When the Quoting Character Mode option is enabled, all edit characters used for backspacing and line deletion and a specific single text terminator can be treated literally by preceding them with a backslash (\). For example, if you type \ BACK SPACE, the back space is put into the user's read buffer without any editing function being performed. You are able to erase the BACK SPACE character as any other character typed, even though the echoing of such erasure may not look right on the terminal. The quoting character is programmable and has a default value of the backslash (\) character.

Conditional Output Separators Appendage

When the Conditional Output Separators Appendage option is enabled, the firmware will examine every outgoing character for the user-specified record separator, which has a default value of the linefeed character. If the user-supplied record separator is found, the firmware sends the the output separators in place of the record separator.

If the Automatic Output Separators Appendage option is also enabled, the output separators are also added to the end of each message. If this is not desired, disable this option.

Signal Character

When the Signal Character option is enabled, every received character is checked for a match to signal character1 or signal character2, which are programmable by the user. If a match occurs, the firmware generates the appropriate status event.

The signal character is very similar to the use of the BREAK key on a terminal, except that you can specify any character for this function. For example, the EM character (CTRL-Y) may be used to interrupt a program from a terminal.

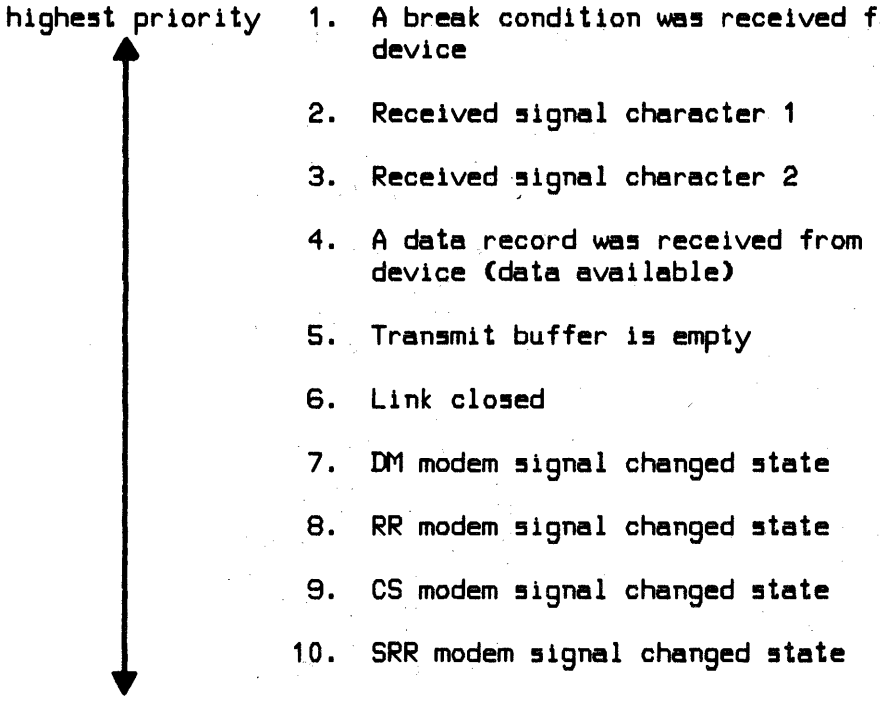
If only one signal character is desired, program both signal characters to be the same.

Null Character Insertion

When this option is enabled, a null character will always be inserted into the receive buffer where the break condition occurred.

ASYNCHRONOUS EVENTS

The host may poll the card or may be interrupt driven by the card for any asynchronous unsolicited event detected by the ASI firmware. The events are listed on the next page in the order of their priority.



The events may be enabled or disabled by using the WCC, SF 21. The event interrupt is enabled by setting the corresponding mask and disabled by clearing the mask.

If the interrupt mask for an event is disabled, you may poll for the event by using read card information (RCI), subfunction (SF) 254 and 255.

When the transmission mode of the ASI is full-duplex modem, the loss of the modem signals DM and RR will not cause an event. Instead, the firmware will perform a link disconnect sequence and report the event as "link closed". The reason for the "link closed" will be given in byte 3.

See the "RTS and WTC Block Definitions" paragraph for a detailed description of the event block format returned to the host.

NOTE

IF ALL INTERRUPT CONDITIONS ARE DISABLED, NO ASYNCHRONOUS INTERRUPT WILL OCCUR.

THE "TRANSMIT BUFFER EMPTY" EVENT IMPLIES THAT ALL DATA HAS BEEN GIVEN TO THE SIO FOR TRANSMISSION. NOTE THAT THE SIO CAN BUFFER UP TO TWO CHARACTERS FOR TRANSMISSION. IF THE BAUD RATE, THE CHARACTER LENGTH, THE PARITY, OR THE NUMBER OF STOP BITS ARE CHANGED BEFORE THE SIO BUFFER IS EMPTY, THE CHARACTERS WILL BE LOST.

NO DATA AVAILABLE EVENT WILL BE GENERATED FOR THE CURRENT RECEIVE RECORD WHEN A PARTIAL READ HAS ALREADY BEEN PERFORMED, AND THE S-BIT WAS SET NOT TO PURGE THE RECORD. YOU CAN CHECK THE READ STATUS REQUEST BLOCK FOR THIS CONDITION. IF THE S-BIT IS SET AND IF THE RESIDUAL COUNT IS NON-ZERO, NO DATA AVAILABLE WILL BE GENERATED UNTIL THE CURRENT RECORD IS EMPTY.

SOLICITED EVENTS

The ASI firmware has one solicited event defined. The solicited event is only active when the transmission mode is full-duplex modem.

The event is activiated when you specify an "open the modem link" control device request. The firmware will return a "no error" status back to the host immediately after starting the connection sequence. When the connection is established, the firmware will return an "event sensed" response to an RTS order. The event code will be 255 with the error code given in byte 3. If the error code is 0, no error occurred during the connection sequence.

You should be aware that the auto answer modem connection sequence will not complete until a successful connection has been established.

This event cannot be masked or polled.

DIAGNOSTICS

The ASI self-test performs diagnostic tests to detect malfunctions. Self-test is executed 'off-line'. That is, it does not run concurrent with the standard ASI firmware. It is executed on a hardware reset of the card following a CHANNEL I/O "Addressed Device Clear" (DCL) or "InterFace Cleared" (IFC) assertion. It exercises the major components and data paths on the card. If no problems are found, the card is made functional and the standard ASI firmware is invoked. If a hardware malfunction is detected, the card is left disabled, indicating that self-test failed.

The following tests are performed by self-test:

- **ROM test:** To ensure that no bits have changed on the ROM (EPROM), a cyclic redundancy check is done using the polynomial X**16+X**2+X+1. The test is performed in 4K segments to insure accuracy of the CRC.

- **RAM test:** RAM is checked for both stuck-at-0 and stuck-at-1 conditions and address decoder failures.

- **ASYNC SIO loopback test:** Verifies that the SIO can perform basic asynchronous transmit and receive functions.

- **Front edge test:** Tests modem/control lines and all other front edge circuitry possible for stuck-at faults. This test requires that the diagnostic hood be installed.

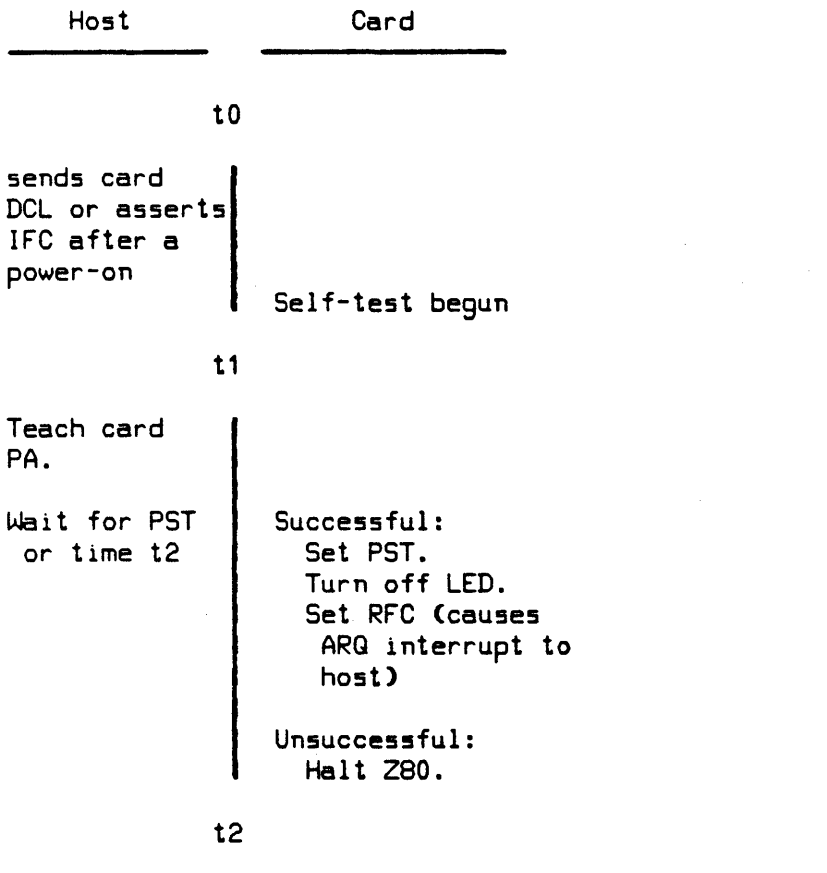
- **CTC test:** Detects stuck-at faults in the data lines, system control, interrupt control, and the four channel signals.

- **BIC Test:** Checks the Backplane Interface Circuit (BIC) for functional faults. Checks for some stuck-at faults in internal BIC registers. The BIC circuitry is tested using the internal loopback functionality built into it. Testing of I/O channel driver and receiver hardware external to the BIC is not done by self-test. The combination of the host diagnostic and ASI loopback support in the 'standard' ASI firmware will exercise the host/ASI interface.

Upon successful completion, self-test will set 'Passed self-test' status (PST), turn off the LED on the card, and invoke the standard ASI firmware. The standard firmware will then wait for the host to 'teach' it its peripheral address (PA) and set 'ready for command' (RFC) status.

If self-test fails, the LED is left on, the 'Passed self-test' status (PST) is not set, and the Z80 is 'Halted'.

The following time-line illustrates the host/card interactions during the self-test sequence:



where:

t1 = 1.0 seconds, t2 = maximum of 3 seconds if IFC;
maximum of 15 seconds if DCL

CONFIGURATION SWITCH DEFINITIONS

The switches on the ASI card are user-definable. The contents may be obtained by using the "read card information request" with subfunction code 253. The switches will have meanings as defined on the next page on interface clear (IFC) or device clear (DCL) condition. You can programmatically change each switch assignment.

SW1 D7	SW2 D6	SW3 D5	SW4 D4	SW5 D3	SW6 D2	SW7 D1	SW8 D0
single text term	hard-wired	no parity	8 data bits	baud rate bit 3	baud rate bit 2	baud rate bit 1	baud rate bit 0
0 = closed, 1 = open							

Baud Rate Switches

The baud rate switches are used to select the baud rate of the SIO channel at reset or power up. The baud rate assignments are shown in table 4-1.

Please note that the switch value assignment does not correspond to the programmatic value assignment defined for WCC, SF 10.

8-Bit Data Switch

If this switch is open, the character length for data is eight bits. Otherwise, seven data bits will be used. The character length may be selected programmatically.

No-Parity Switch

If this switch is open, no parity will be used. Otherwise, odd parity is programmed into the SIO. The other parity options may be selected programmatically.

Table 4-1. Baud Rate Switch Assignments

SW5	SW6	SW7	SW8	BAUD RATE
0	0	0	0	50
0	0	0	1	75
0	0	1	0	110
0	0	1	1	134.5
0	1	0	0	150
0	1	0	1	300
0	1	1	0	600
0	1	1	1	900
1	0	0	0	1200
1	0	0	1	1800
1	0	1	0	2400
1	0	1	1	3600
1	1	0	0	4800
1	1	0	1	7200
1	1	1	0	9600
1	1	1	1	19200

Hardwired Switch

If this switch is open, a device is directly connected to the card and all modem control lines are disabled. The host, however, can control the lines directly.

If this switch is closed, the card will not receive or transmit any data until the host makes a line connection request. This mode can be disabled by the host.

Single Text Termination Switch

This switch, when open, enables single text termination. The other read options may be selected programmatically.

TRANSACTION REQUEST BLOCK SUBFUNCTION DEFINITIONS

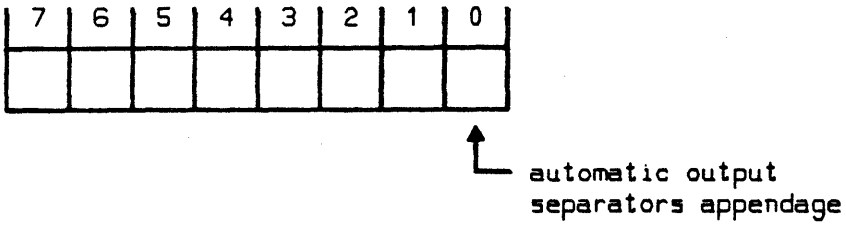
The following paragraphs describe the subfunction options that are available for each logical channel transaction request.

Read Device Data, Request Code = 1

Subfunction code - none defined

Write Device Data, Request Code = 2

Subfunction code



Control Device, Request Code = 3

Subfunction	Description
0	No operation.
1	Open (connect) the modem link. The card will notify the host when the link is connected by generating a solicited event.
2	Close (disconnect) the modem link
3	Generate a break to the device
4	Set the RS modem control signal
5	Clear the RS modem control signal
6	Set the TR modem control signal
7	Clear the TR modem control signal
8	Set the SRS modem control signal
9	Clear the SRS modem control signal
10	Set the SR modem control signal
11	Clear the SR modem control signal

Read Card Information, Request Code = 4

For the read card information request the residue count in the read request status block will reflect the number of bytes of information not returned in the request. This will always be nonzero when the requested data transfer length is not large enough to hold all the information that can be returned for the requested subfunction.

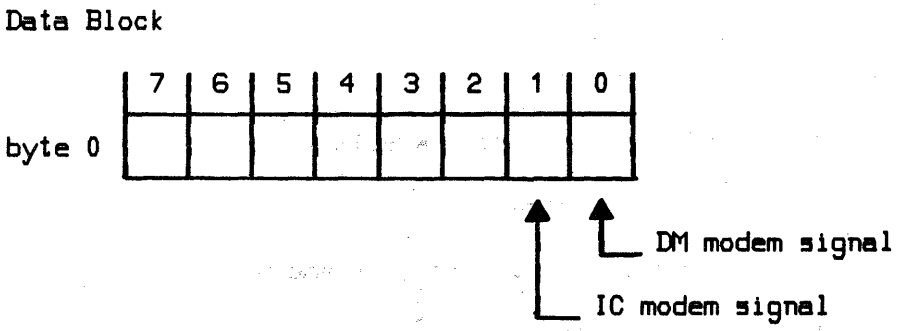
SUBFUNCTION 0. This will read back all the configuration data defined for subfunction 0 of the write card configuration.

SUBFUNCTIONS 1 THROUGH 32. Read back the information defined in subfunctions 1 through 32 of the write card configuration, respectively.

Note that subfunction 32 will return up to 8 bytes of information. To obtain all possible single text terminators, the user must specify a request for 8 bytes of data. The firmware will return only those characters which are being used as a single text terminator. The actual data transfer length which is the number of single text terminators will be given in the read request status.

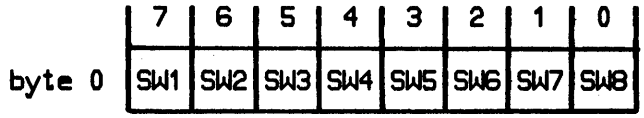
SUBFUNCTION 250. GET THE CARD RAM. All of the card RAM memory is sent to the host in the data block. The host buffer must be large enough to hold the data.

SUBFUNCTION 251. GET THE CARD READ REGISTER. The card Read register contents are sent to the host. This subfunction is used for on-line card diagnostics.



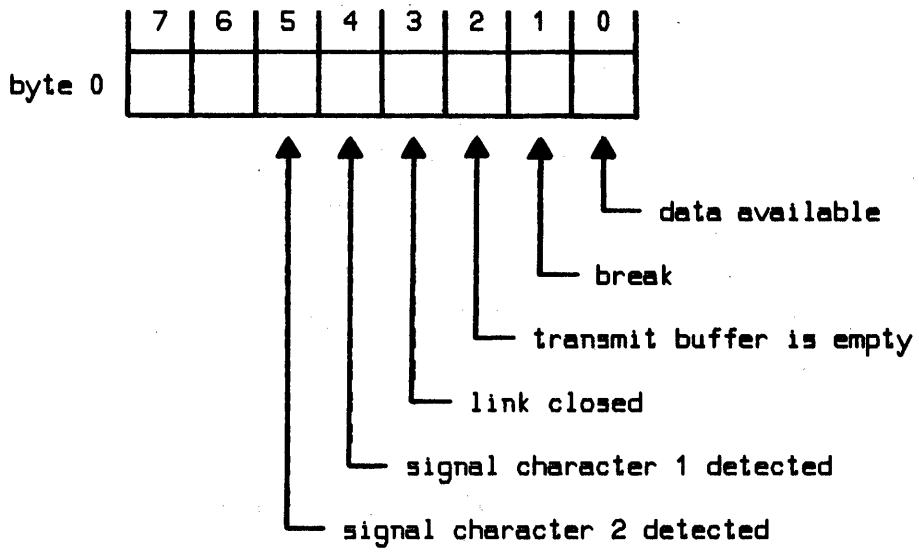
SUBFUNCTION 252. GET THE CARD WRITE REGISTER. The card Write register contents are sent to the host. This subfunction is used for on-line card diagnostics.

SUBFUNCTION 253. GET THE CARD SWITCH SETTING. The content of the switch setting is returned in the data block (1 => open).



SUBFUNCTION 254. GET CARD STATUS. The following status is returned in the data block.

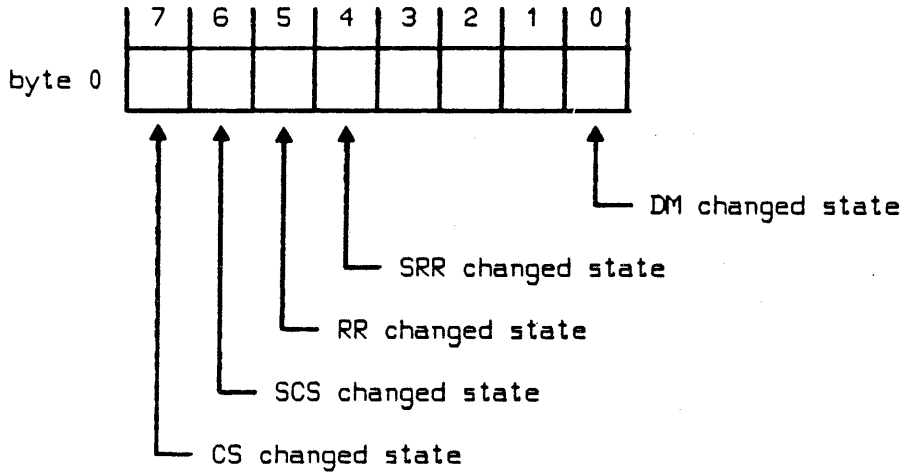
Data block

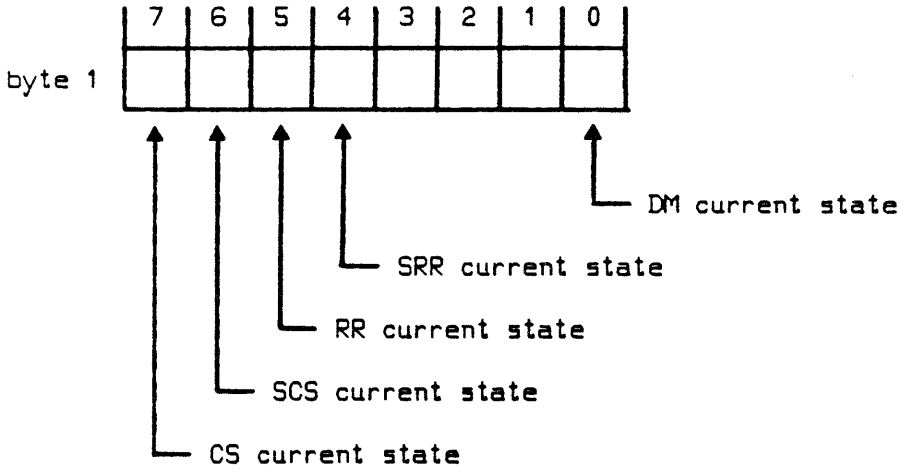


This status will be cleared after the read.

SUBFUNCTION 255. READ MODEM LINE STATUS. The modem line which changed state is returned in byte 0. Byte 1 will contain the current modem line state. Byte 0 will be cleared after the read.

Data block





Write Card Configuration, Request Code = 5

The firmware will perform parameter validation where possible. Every write card configuration request data transfer length must match exactly the length specified for the request; otherwise, the illegal configuration parameter length error will be returned in the read request status block. If the data transfer length is not specified for the subfunction validation below, the length is assumed to be 1 byte. (Note that data transfers shorter than the required length are not zero filled and will give an error as stated above.)

If the subfunction code is not described in this document, an illegal subfunction error will be returned.

For each of the subfunctions defined below, a brief description of the type of validation performed on the parameter passed in the data block is given. If the parameter is not valid, an illegal configuration parameter value error will be returned.

SUBFUNCTION 0. This consists of all configuration data defined in subfunctions 1 through 32. The data is position dependent according to each subfunction code. This subfunction allows one call to configure everything, instead of calling each individual item. After the initial configuration a particular item can be changed as needed.

Note that if you use this subfunction, every item must be specified with new values. The default values or the previous values that were specified will be set to the new values given.

The data block is defined as follows:

byte: function

0: configure frontplane control

1: high byte end-on-count length

2: low byte end-on-count length

3: alert 1 read mode option

4: modem connection mode

5: transmission mode

6: backspace character

7: line delete character

8: character stripping mask and other options

9: device handshake option

10: baud rate

11: character length

12: number of stop bits

13: parity

14: modem connection timer

15: high byte no activity timer

16: low byte no activity timer

17: lost data mode timer

18: gap timer

19: host controlled ENQ/ACK timer

20: break generation timer

21: 0

22: host interrupt mask

23: modem interrupt mask

24: host controlled X-ON character

25: host controlled X-OFF character

26: device controlled X-ON character

27: device controlled X-OFF character

28: host controlled ENQ character

29: host controlled ACK character

30: host controlled ENQ/ACK pacing counter

31: device controlled ENQ character

32: device controlled ACK character

33: a single text terminator character for echoing CR-LF

34: number of output separators

35: 1st output separator character or null

36: 2nd output separator character or null

37: 1st character of double text terminator or null

38: 2nd character of double text terminator or null

39: number of prompt sequence characters

40: 1st prompt sequence character or null

41: 2nd prompt sequence character or null

42: additional options

43: replacement character for bad incoming character

44: quoting character

45: record separator character

46: signal character 1

47: signal character 2

48: quotable single text terminator character

49: number of single text terminators

50: 1st single text terminator character

51: 2nd single text terminator character

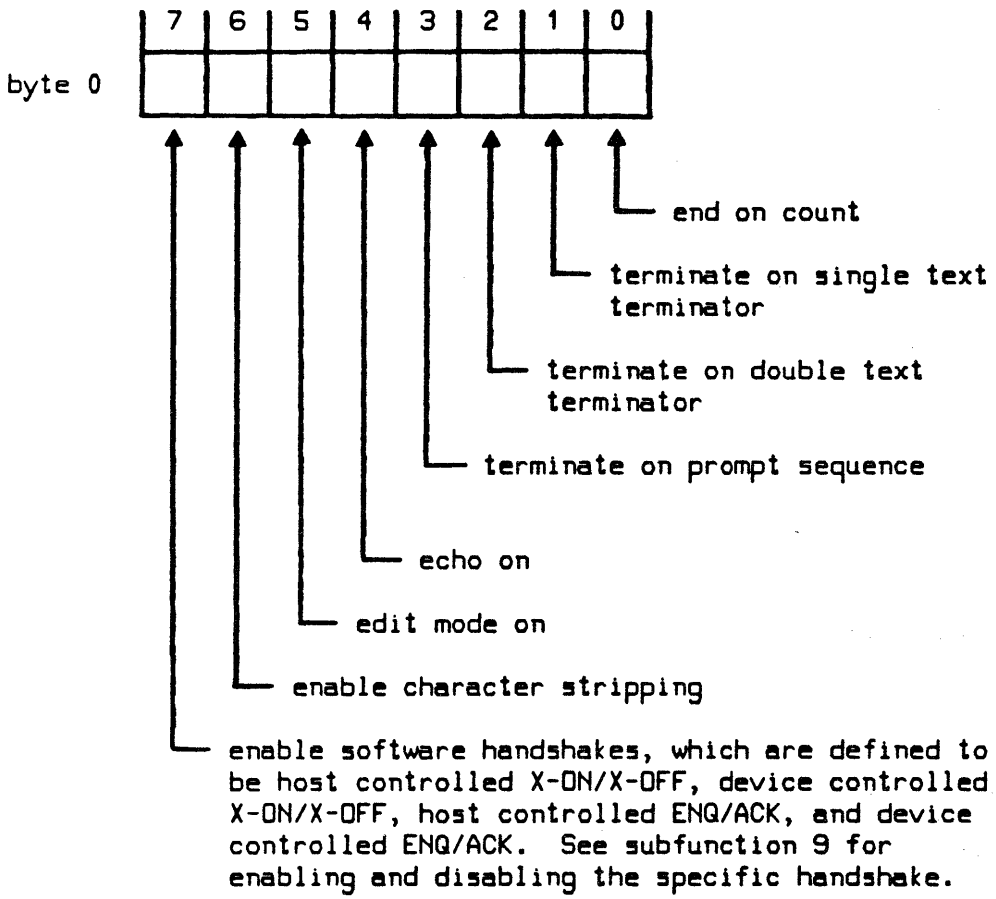
57: 8th single text terminator character

Validation: The request must specify a data transfer length of 58 bytes. No other validation will be performed.

Note that the transmission mode will not be changed when subfunction 0 is used. This is done to allow changing any other parameters without affecting the integrity of the modem connection. To change the transmission mode, subfunction 5 must be used. (See the paragraph "Subfunction 5. Transmission Mode" for additional details.)

SUBFUNCTION 1. CONFIGURE ASI-TO-DEVICE CONTROL.

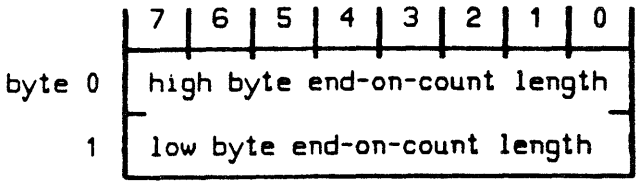
Data block



Validation: If the echo bit is set, the transmission mode must be full duplex modem or full duplex hardwired. The transmission mode must be programmed first before setting the read option.

SUBFUNCTION 2. END-ON-COUNT LENGTH.

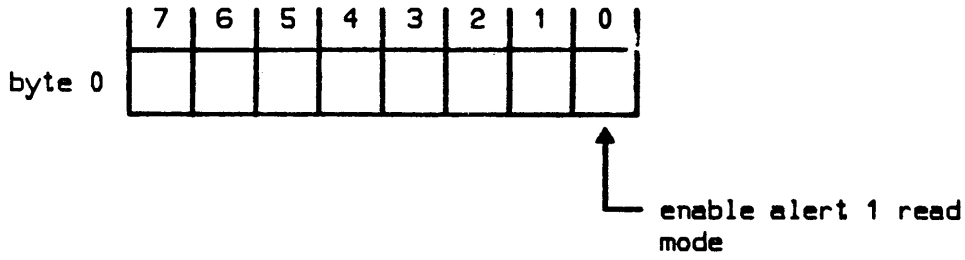
Data block



Validation: none

SUBFUNCTION 3. ALERT 1 READ MODE.

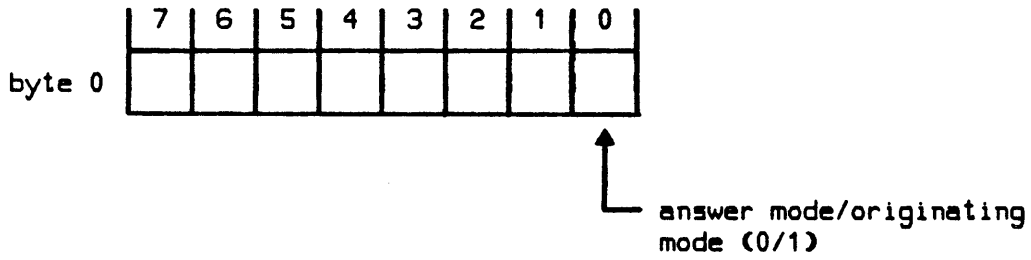
Data block



Validation: none

SUBFUNCTION 4. MODEM CONNECTION MODE.

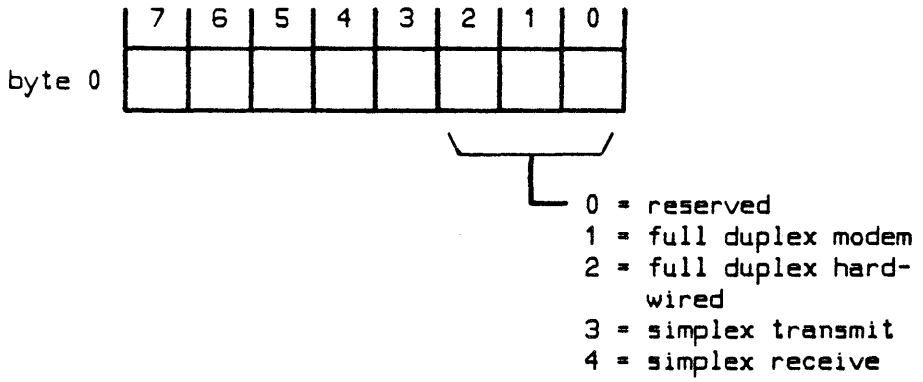
Data block



Validation: none

SUBFUNCTION 5. TRANSMISSION MODE.

Data block



Validation: The parameter value must be within the range 1 through 4, inclusive. The transmission mode must be set before setting the read option. Note that the echo bit will be reset if the transmission mode is not full duplex.

CAUTION

IF THE CURRENT TRANSMISSION MODE IS FULL-DUPLEX MODEM AND IF THE LINK IS STILL OPENED AT THE TIME THIS REQUEST IS ISSUED, THE MODEM WILL BE DISCONNECTED WHEN THE REQUEST IS EXECUTED BY THE FIRMWARE. THE SIO IS RESET BEFORE THE NEW TRANSMISSION MODE IS PROGRAMMED, WHICH IS THE REASON FOR THE MODEM DISCONNECT. LICENSING REQUIREMENTS REQUIRE CONTINUOUS MONITORING OF THE MODEM SIGNALS WHENEVER THE LINK IS CONNECTED UNDER THE CARD FIRMWARE.

SUBFUNCTION 6. BACKSPACE CHARACTER. The character specified in the data block will be used as the backspace character for the edit mode.

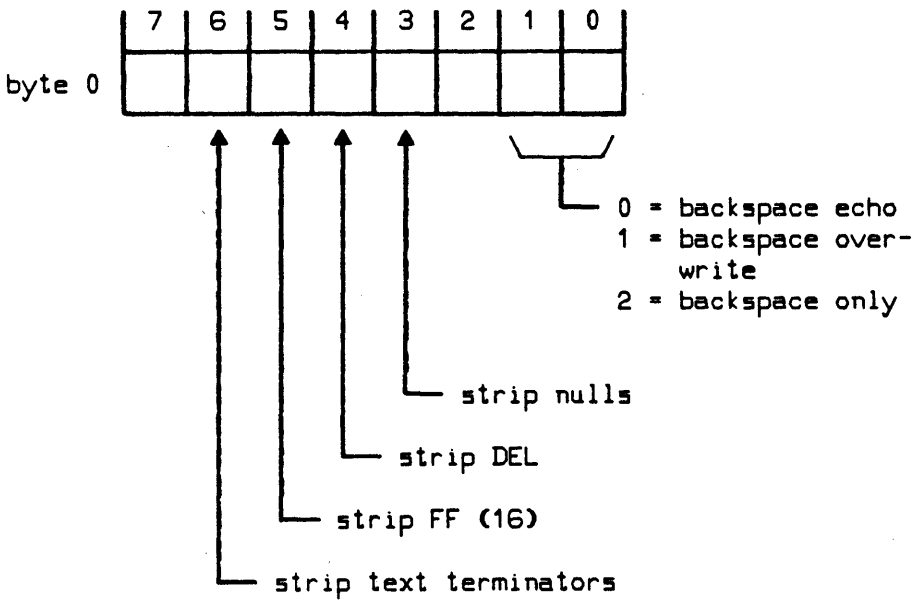
Validation: none

SUBFUNCTION 7. LINE DELETE CHARACTER. The character specified in the data block will be used as the line delete character for the edit mode.

Validation: none

SUBFUNCTION 8. CHARACTER STRIPPING MASK AND BACKSPACE OPTIONS.

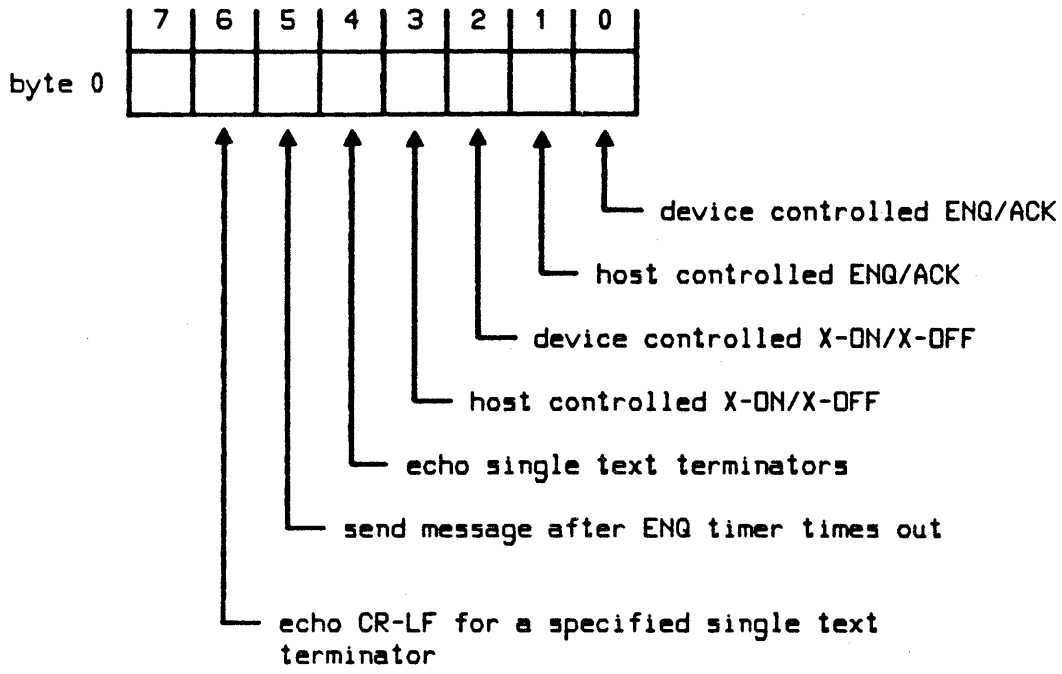
Data block



Validation: none

SUBFUNCTION 9. DEVICE HANDSHAKE OPTION.

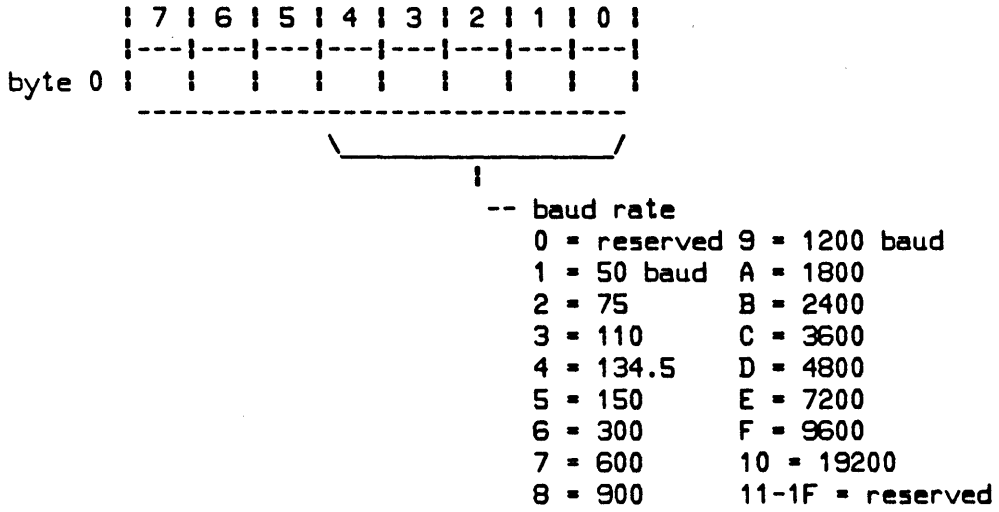
Data block



Validation: none

SUBFUNCTION 10. BAUD RATE.

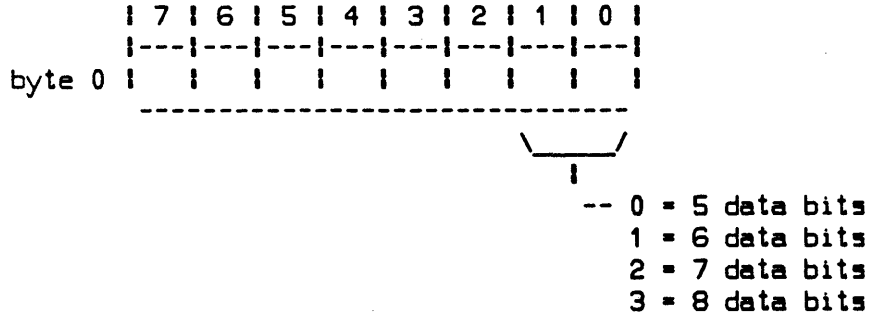
Data block



Validation: The value must be within the range 1 through 10H, inclusive.

SUBFUNCTION 11. CHARACTER LENGTH.

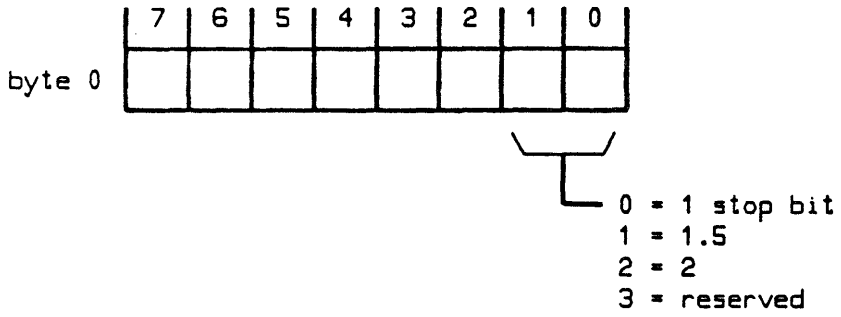
Data block



Validation: The value must be within the range 0 through 3, inclusive.

SUBFUNCTION 12. NUMBER OF STOP BITS.

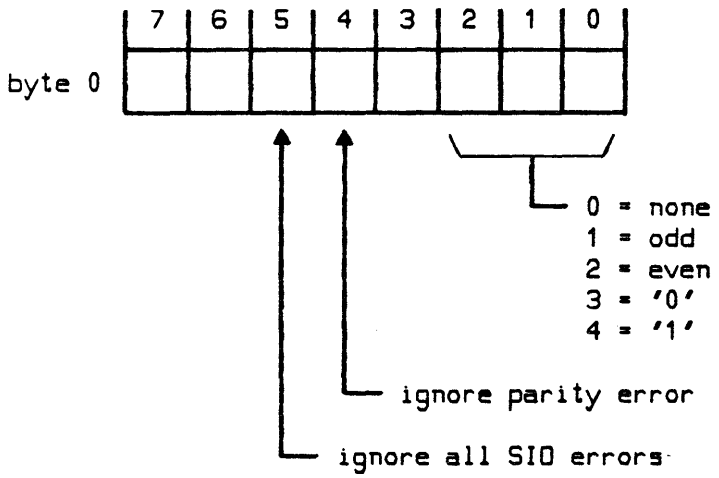
Data block



Validation: The value must be within the range of 0 through 2, inclusive.

SUBFUNCTION 13. PARITY.

Data block



Validation: The value must be within the range 0 through 4, inclusive. (The ignore error options will not be included in the validation.)

For subfunctions 14 to 19, the timer value is specified in the data block of the write configuration request. All timers have a data block length of one byte except for the no activity timer which has a data block length of two bytes.

SUBFUNCTION 14. MODEM CONNECTION TIMER. The clock resolution is one second. The timer can be programmed from 0 to 255 seconds.

Validation: none

SUBFUNCTION 15. NO ACTIVITY TIMER. The clock resolution is one second. The timer can be programmed from 0 to 65535 seconds.

Validation: The request must have a data transfer length of two bytes.

SUBFUNCTION 16. LOST RECEIVER READY TIMER. is ten milliseconds. The timer can be programmed from 0 to 2550 milliseconds (0 to 255 counts of 10's milliseconds).

Validation: none

SUBFUNCTION 17. GAP TIMER. The clock resolution is one character. The timer can be programmed from 0 to 254 characters (the value of 255 is the same as 0).

Validation: none

SUBFUNCTION 18. HOST CONTROLLED ENQ/ACK TIMER. The clock resolution is one second. The timer can be programmed from 1 to 255 seconds.

Validation: The value must be greater than or equal to one.

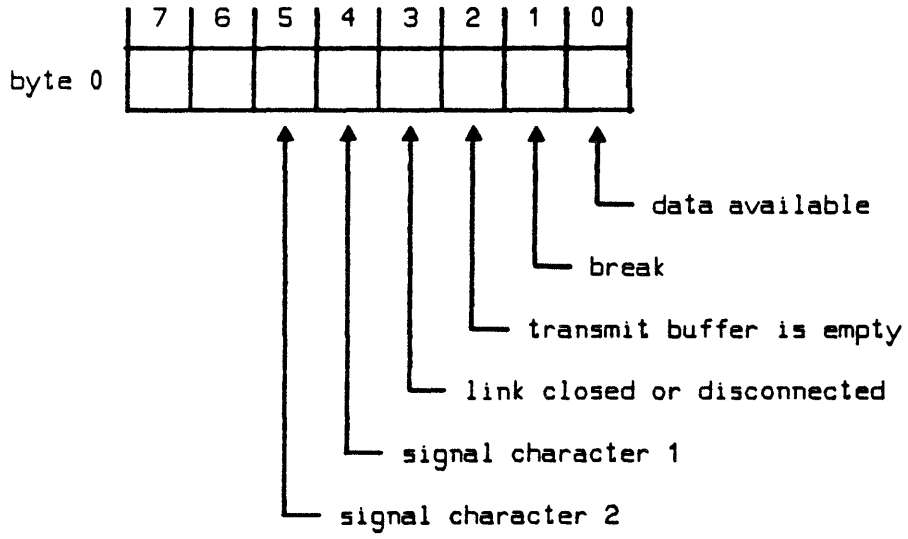
SUBFUNCTION 19. BREAK GENERATION TIMER. The clock resolution is one character. The timer can be programmed from 2 to 255 characters.

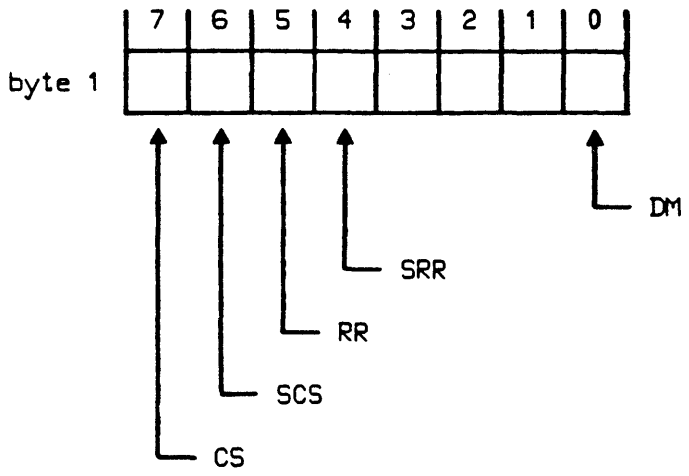
Validation: The value must be greater than 1.

SUBFUNCTION 21. HOST AND MODEM INTERRUPT MASK. The host interrupt mask is used to specify which conditions will cause an unsolicited interrupt (or asynchronous event) to the host. The modem interrupt mask specify which modem signal will cause an interrupt when the signal changes state.

Note that the modem signals RR and DM will not cause an event if the transmission mode is full-duplex modem. The loss of these signals will cause the modem link to be closed.

Data block





Validation: The request must specify a data transfer length of two bytes.

SUBFUNCTION 22. HOST CONTROLLED X-ON/X-OFF CHARACTERS.

Data block

```
byte 0: character for host X-ON function
     1: character for host X-OFF function
```

Validation: The request must specify a data transfer length of 2 bytes.

SUBFUNCTION 23. DEVICE CONTROLLED X-ON/X-OFF CHARACTERS.

Data block

```
byte 0: character for device X-ON function
     1: character for device X-OFF function
```

Validation: The request must specify a data transfer length of two bytes.

SUBFUNCTION 24. HOST CONTROLLED ENQ/ACK CHARACTERS.

Data block

```
byte 0: character for host ENQ function
     1: character for host ACK function
```

Validation: The request must secify a data transfer length of two bytes.

SUBFUNCTION 25. HOST CONTROLLED ENQ/ACK PACING COUNTER.

Data block

```
byte 0: the number of characters to transmit before sending an ENQ and waiting
for an ACK (count should be 1 to 255)
```

Validation: The value must be greater than 0.

SUBFUNCTION 26. DEVICE CONTROLLED ENQ/ACK CHARACTERS.

Data block

```
byte 0: character for device ENQ function
     1: character for device ACK function
```

Validation: The request must specify a data transfer length of two bytes.

SUBFUNCTION 27. SINGLE TEXT TERMINATOR FOR ECHOING CR-LF Any one of the single text terminator characters may be specified to cause the echoing of the CR-LF characters. However, only one character may be used for the special echoing function. This character is specified in the data block for this subfunction.

Validation: none

SUBFUNCTION 28. OUTPUT SEPARATOR.

Data block

```
byte 0: 1st output separator char
     1: 2nd output separator char
```

Validation: The request must specify a data transfer length of one or two bytes.

SUBFUNCTION 29. DOUBLE TEXT TERMINATOR.

Data block

```
byte 0: 1st character of the double text terminator
     1: 2nd character of the double text terminator
```

Validation: The request must specify a data transfer length of two bytes.

SUBFUNCTION 30. PROMPT SEQUENCE.

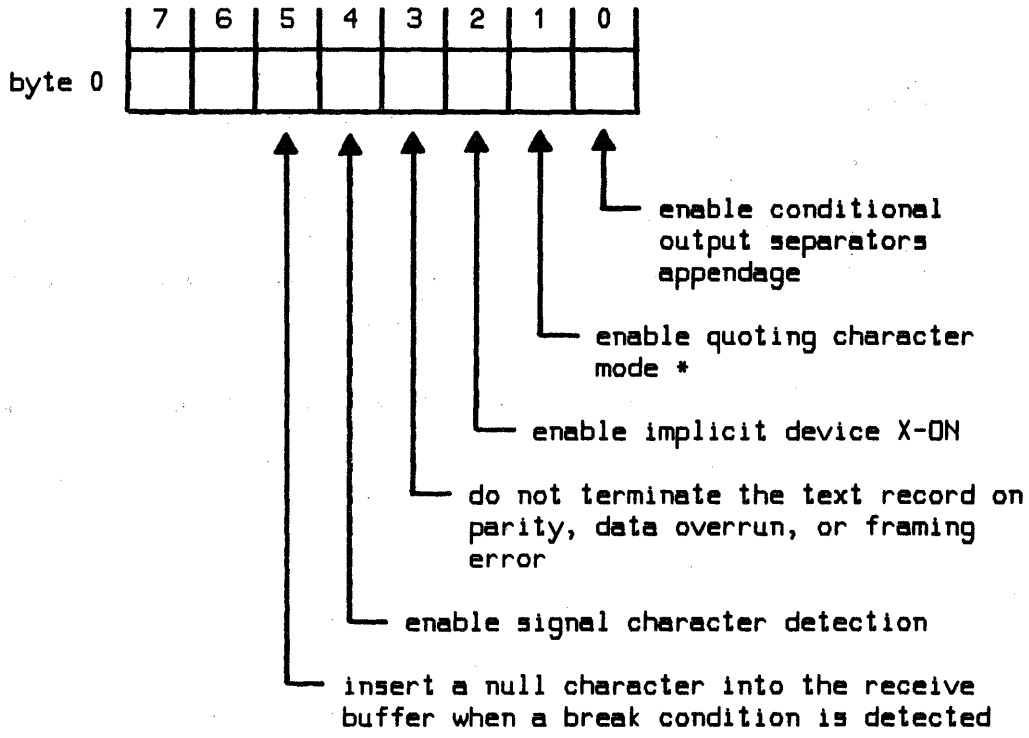
Data block

```
byte 0: 1st char of prompt sequence
     1: 2nd char of prompt sequence
```

Validation: The request must specify a data transfer length of one or two bytes.

SUBFUNCTION 31. ADDITIONAL OPTIONS.

Data block



* When the quoting character mode is enabled, byte 2 specifies the quoting character to be used for the quotable single text terminator character in byte 6, the backspace character, and the line delete character.

```
byte 1: replacement character for the bad incoming character
byte 2: quoting character
byte 3: record separator character to invoke sending the
        output separators
byte 4: signal character 1
byte 5: signal character 2
byte 6: quotable single text terminator
```

Validation: The request must specify a data transfer length of seven bytes.

SUBFUNCTION 32. SINGLE TEXT TERMINATOR.

Data block

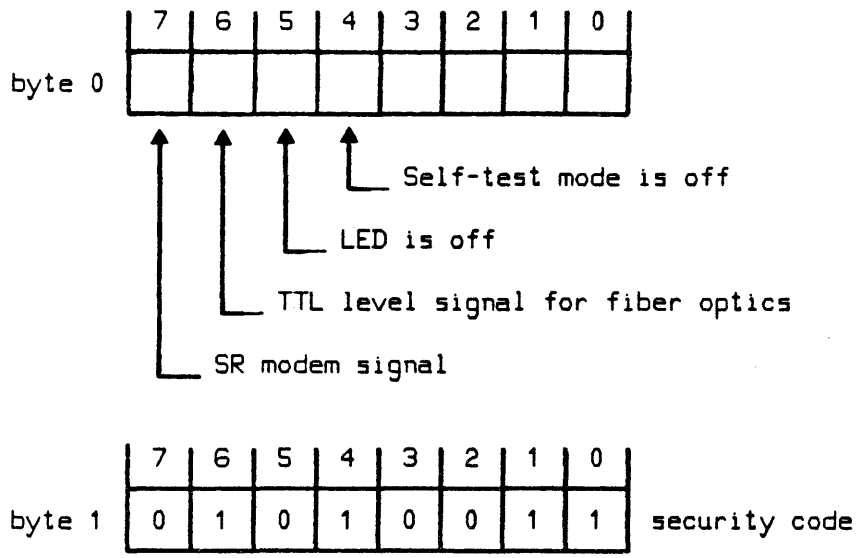
```
byte 0:  1st character to be used as a single text terminator
byte 1:  2nd character to be used as a single text terminator
         .
         .
         .
byte 7:  8th character to be used as a single text terminator

   where 1 <= n <= 8
```

Validation: The request data transfer length must be within the range of one through eight, inclusive.

SUBFUNCTION 33. CARD WRITE REGISTER. This subfunction is used for on-line diagnostics capability.

Data Block



NOTE

THE SECURITY CODE IS USED TO PREVENT THE USER FROM INADVERTENTLY WRITING TO THIS REGISTER

The request data transfer length must be two bytes long. The security code must match exactly.

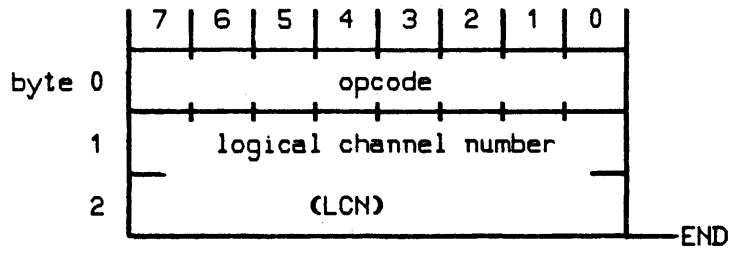
Control Card, Request Code = 6

SUBFUNCTION	DESCRIPTION
0	No operation.
1	Flush the current receive buffer.
2	Flush all data in the receive buffer.

3	Flush all of the queued transmit buffer.
4	Host initiates termination of frontplane receive record.
5	Force restart of the transmitter if it was stopped due to waiting for host ACK or device X-ON. This control request is normally used after turning off the handshake option to prevent a deadlock condition.
8	Suspend the transmitter. The transmitter will be suspended as if a device controlled X-OFF was received. Either a device X-ON (if the device controlled X-ON/X-OFF handshake in WCC, SF 9 is enabled and if the handshake bit in WCC, SF 1 is enabled) or a restart the transmitter request (subfunction 5 above) may be used to resume the data transmission. This may be used to suspend the output on the receipt of some external event (e.g., a break condition).

RTS AND WTC BLOCK DEFINITIONS

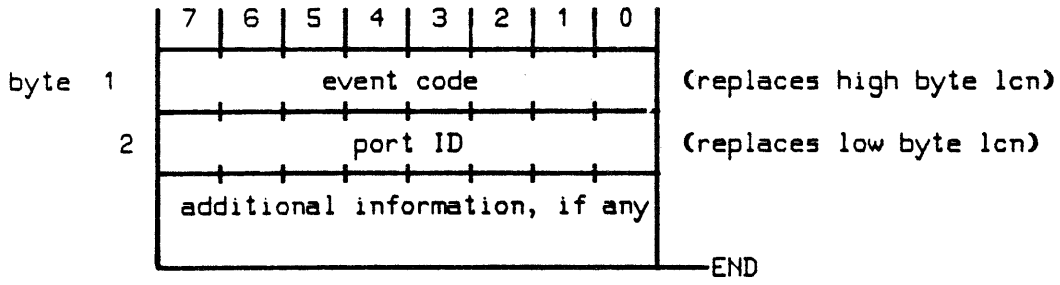
The Read Transparent Status (RTS) and Write Transparent Control (WTC) block definitions are as follows:



opcode	RTS description	WTC description
0	IDL (idle) - Nothing to do. The logical channel number (LCN) field is not used.	Not used.
1	SWI (switch) - Switch to the logical channel given in the LCN field and continue the transaction there.	Resume the transaction in the logical channel given in the LCN field.

2	EOD (end of data) - End of the data transfer for the transaction given in the LCN field.	EOD - End of data transfer for the transaction given in the LCN field.
3	LCD (logical channel destroyed) - The logical channel has been destroyed and the transaction aborted.	DLC (destroy logical channel) Abort the transaction given in the LCN field.
4	AES (asynchronous event sensed) - The event block as defined below is returned to the host in place of the logical channel number. The ASI card will return up to 6 bytes for the event block.	AEK (asynchronous event acknowledged). Acknowledement to the event. The LCN field is not used.
5	ERT (error trap) - Error trap in transaction given in the LCN field.	Not used.

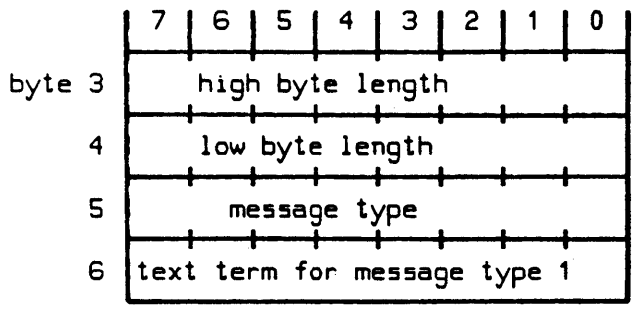
EVENT BLOCK DESCRIPTION



event code

0 = reserved

1 = data message received. Message length and type are given in the information field.



message type

1 = text terminated on single text terminator. The text terminator which terminated the message is given in byte 6.

2 = text terminated by a double text terminator sequence

3 = text terminated by prompt sequence

4 = text terminated by count

5 = text terminated by parity error

6 = text terminated by data overrun

7 = text terminated by framing error

8 = alert, received at least one character

9 = text terminated by the card, more data coming

10 = text terminated by the loss of RR

11 = text terminated by the loss of DM

12 = text terminated by the card, no more data

13 = text terminated by buffer overflow

14 = host initiated text termination

If the message type code is greater than 16, then a parity, data overrun, or framing error has occurred for the terminated record. Subtract 16 to obtain the message type code.

2 = break received from the device

3 = transmit buffer is empty

4 = an opened link was closed or disconnected
Byte 3 contains the reason for the link disconnection:

1 = the card lost the modem DM signal

2 = the card lost the modem RR signal

3 = the no activity timer timed out

5 = signal character 1 received

6 = signal character 2 received

7-8 = reserved

9 = modem DM signal changed state. Byte 3 will contain the current modem signal state.

10-12 = reserved

13 = modem SRR signal changed state. Byte 3 will contain the current modem signal state.

14 = modem RR signal changed state. Byte 3 will contain the current modem signal state.

15 = modem SCS signal changed state. Byte 3 will contain the current modem signal state.

16 = modem CS signal changed state. Byte 3 will contain the current modem signal state.

The modem signal state format for 9, 13, 14, 15, and 16 is:

	7	6	5	4	3	2	1	0
Byte 3	CS	SCS	RR	SRR				DM

17-254 = reserved.

255 = completion for open link request. Byte 3 will contain an error code.

0 = no error, link opened.

1 = modem connection timer timed out.

port ID

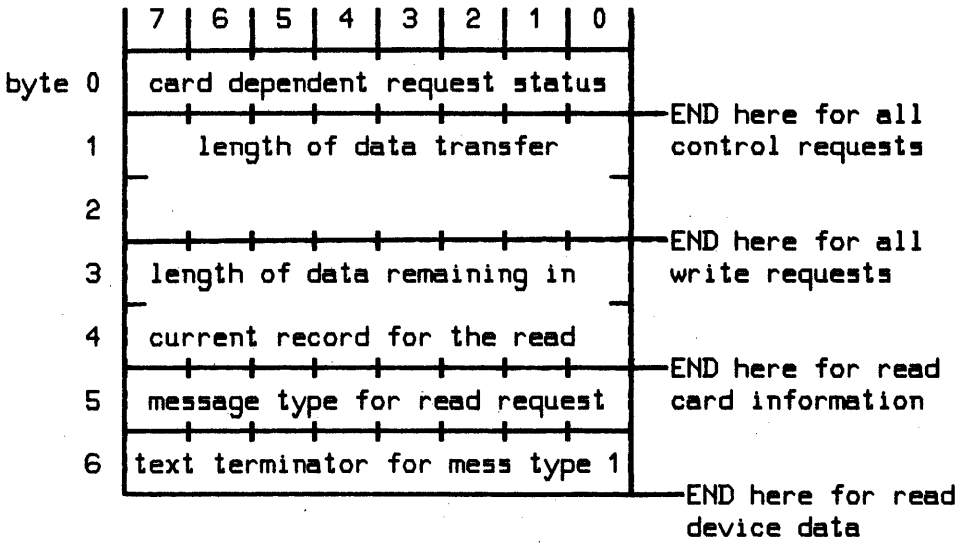
Always zero

additional information

The information contained in this field is dependent on the event code as given above.

READ STATUS (RS) BLOCK DEFINITIONS

The following status block is returned in response to a Read Status order during the status part of a transaction. Following the status block, the logical channel is automatically disconnected and the LCN (Logical Channel Number) is released.



card dependent request status

0 = no error

1 = illegal subfunction

2 = illegal configuration parameter values

3 = illegal configuration parameter length

4 = illegal request or request not implemented

5 = illegal port ID

6 = data overrun in host write data (the host wrote more data than was specified in the request)

7 = block mode data transfer is not allowed for the request

8 = data transfer length is too large

9 = cannot execute control request, no buffer space

10 = link connected already

252 = transmission mode not defined as modem for link open or close request

253 = modem link is closed

254 = transmit not allowed in simplex receive mode

255 = receive not allowed in simplex transmit mode

length of data transfer

This field gives the length in bytes of the data transfer initiated by the card for the host read or write request.

Note that the length does not reflect any early termination initiated by the host. For example, if the host started a host read request of 200 bytes and the card is able to send 200 bytes, the card will return the length as 200 even though the host invoked END to terminate the transfer early.

message type

1 = text terminated on single text terminator. The text terminator which terminated the message is given in byte 6.

2 = text terminated by a double text terminator sequence.

3 = text terminated by prompt sequence.

4 = text terminated by count.

5 = text terminated by parity error.

6 = text terminated by data overrun.

7 = text terminated by framing error.

8 = text terminated by alert one condition.

9 = text terminated by the card, more data coming.

10 = text terminated by the lost of RR.

11 = text terminated by the lost of DM.

12 = text terminated by the card, no more data.

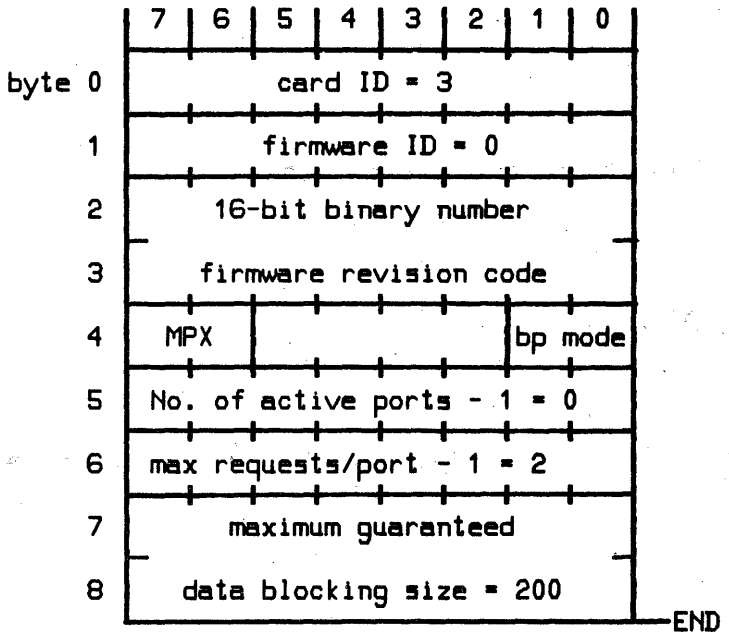
13 = text terminated by buffer overflow.

14 = host initiated text termination.

If the message type code is greater than 16, then a parity, data overrun, or framing error has occurred for the terminated record. Subtract 16 to obtain the message type code.

IDENTITY INFORMATION BLOCK DEFINITION

The following identity information block is returned by the ASI for the IDY order.



MPX = 0 for subchannel multiplexing only

1 for in-channel multiplexing only

2 for both

3 is reserved

The ASI card is configureed with MPX = 1

```
bp mode = 0 for 16-bit I/O channel data path only

          1 for 8-bit I/O channel data path only

          2 for 8- or 16-bit I/O channel data path
            available

          3 is reserved


          The ASI card is configured with bp mode = 1
```

DEFAULT ASI CONFIGURATIONS

Upon a reset or power up condition, the ASI will be set to the configuration states defined below:

* enable software handshake: no
* character stripping: disabled
* edit mode: disabled
* echoing: disabled
* terminate on prompt sequence: disabled
* terminate on double text terminator: disabled
* terminate on single text terminator: switch selectable
* end on count: disabled
* end on count length: 200

- alert 1 read mode: disabled
- modem lines SR, TR, SRS, and RS are cleared
- modem connection mode: answer mode
- transmission mode: switch selectable for full-duplex modem or hardwired
- backspace character: BS
- line delete character: DEL
- strip text terminators: enabled
- strip FF (base 16): disabled
- strip DEL: disabled
- strip nulls: disabled
- type of backspace notification: backspace echo
- echo CR-LF for a specified single text terminator: enabled
- send message after ENQ timeout: disabled
- echo single text terminator: disabled
- host controlled X-ON/X-OFF handshake: disabled
- device controlled X-ON/X-OFF handshake: disabled
- host controlled ENQ/ACK handshake: disabled
- device controlled ENQ/ACK handshake: disabled
- baud rate: switch selectable
- character length: switch selectable for 7 or 8
- number of stop bits: 1
- parity: switch selectable for none or odd
- modem connection timer: 25 seconds
- no activity timer: 600 seconds
- lost receiver ready timer: 400 milliseconds

- gap timer: 0 character
- host controlled ENQ/ACK timer: 5 seconds
- break generation time: 4 characters
- host interrupt mask: all cleared to disable interrupt
- modem line interrupt mask: all cleared to disable interrupt
- host controlled X-ON character: DC1
- host controlled X-OFF character: DC3
- device controlled X-ON character: DC1
- device controlled X-OFF character: DC3
- single text terminaor character for echoing CR-LF: CR
- host controlled ENQ character: ENQ
- host controlled ACK character: ACK
- host controlled ENQ/ACK pacing counter: 80
- device controlled ENQ character: ENQ
- device controlled ACK character: ACK
- number of output separator: 2
- output separator characters: CR-LF
- double text terminator characters: CR-LF
- number of prompt sequence character: 1
- prompt sequence characters: null, null
- signal character detection: disabled
- do not terminate the text record on error: disabled
- quoting character mode: disabled
- conditional output separators appendage: disabled
- replacement character for bad incoming character: DEL
- quoting character: \

- record separator: LF
- signal character 1: FF
- signal character 2: FF
- quotable single text terminator character: EOT
- number of single text terminators: 1
- single text terminator character: CR

SUBFUNCTION ASSIGNMENT SUMMARY

A summary of all subfunction assignments is listed in the following paragraphs.

Read Device Data

SUBFUNCTION = none defined

Write Device Data

SUBFUNCTION =

0 no output separator appendage

1 append output separators

Control Device

SUBFUNCTION =

0 no operation

1 open (connect) the modem link

2 close (disconnect) the modem link

3 generate a break to the device

4 set the RS modem control signal

5 reset the RS modem control signal

6 set the TR modem control signal

7 reset the TR modem control signal

8 set the SRS modem control signal

9 reset the SRS modem control signal

10 set the SR modem control signal

11 reset the SR modem control signal

Read Card Information

SUBFUNCTION = 0 through 33 see write card configuration

250 get the card RAM

251 get the card read register content

252 get the card write register content

253 get the card switch setting

254 get the card status

255 get the modem line status

Write Card Configuration

SUBFUNCTION = 0 configure subfunctions 1 through 32

1 configure the read option

2 end-on-count length

3 alert 1 read mode option

4 modem connection mode

5 transmission mode

6 backspace character

7 line delete character

8 character stripping mask & other options

9 device handshake option

10 baud rate

11 character length

12 number of stop bits

13 parity

14 modem connection timer

15 no activity timer

16 lost receiver ready timer

17 gap timer

18 host ENQ/ACK timer

19 break generation timer

20 reserved

21 host & modem interrupt masks

22 host X-ON/X-OFF characters

23 device X-ON/X-OFF characters

24 host ENQ/ACK characters

25 host ENQ/ACK pacing counter

26 device ENQ/ACK characters

27 single text terminator for echoing CR-LF

28 output separator

29 double text terminator

30 prompt sequence

31 additional options

32 single text terminator

Control Card

SUBFUNCTION =

0 no operation

1 flush the current receive buffer

2 flush all of the queued receive buffers

3 flush all of the queued transmit buffers

4 host initiated frontplane receives text termination

5 force restart of the transmitter if it was stopped due to waiting for a host ACK of a device X-ON. This control request is normally used after turning off the handshake option to prevent a deadlock condition.

8 suspend the transmitter

MAINTENANCE

SECTION V

If the ASI card did not pass the self-test described in Section 2, it is recommended that you return the card to Hewlett-Packard. If further testing is desired, however, a diagnostic test hood, which tests slightly more of the card's circuitry, can be ordered. The diagnostic test hood part number is 1258-0207.

To test the ASI card using the diagnostic test hood, perform the following:

1. Turn computer system power off.

2. Connect the test hood to connector J2 on the card.

3. Refer to the appropriate computer system manual to determine if the self-test is run automatically at power-on, or only when specifically invoked by you.

4. Turn on computer system power.

5. When the self-test executes, the LED located on the test hood should light briefly and go out if the card passed self-test. If the LED does not light at all, the card is defective. If the LED stays lit, the card did not pass self-test.

If desired, isolation to a defective part may be performed. Please be advised, however, that such work is at your discretion and is your responsibility; moreover, NOTE THAT CUSTOMER REPAIR OR MODIFICATION OF THE ASI CARD WILL INVALIDATE WARRANTY AND RENDER THE CARD INELIGIBLE FOR EXCHANGE OR REPAIR BY HEWLETT-PACKARD COMPANY. If such service is performed, the replaceable parts information in Section 6 and the schematic logic diagrams in Section 7 will be of assistance.

REPLACEABLE PARTS

SECTION VI

This section contains information for ordering replaceable parts for the ASI card. Table 6-1 contains a list of replaceable parts, table 6-2 contains the names and addresses of the manufacturers indexed by the code numbers used in table 6-1, and figure 6-1 shows the locations of the parts on the ASI card.

REPLACEABLE PARTS

Table 6-1 contains a list of replaceable parts in reference designation order. The following information is listed for each part:

1. Reference designation of the part.
2. The Hewlett-Packard part number.
3. Part number check digit (CD).
4. Total quantity (QTY).
5. Description of the part.
6. A five-digit manufacturer's code number of a typical manufacturer of the part. Refer to table 6-2 for a cross-reference of the manufacturers.
7. The manufacturer's part number.

ORDERING INFORMATION

To order replacement parts or to obtain information on parts, address the order or inquiry to the nearest Hewlett-Packard Sales and Service Office (Sales and Service Offices are listed at the back of this manual).

To order a part listed in the replaceable parts table, quote the Hewlett-Packard part number (with the check digit), and indicate the quantity required. The check digit will insure accurate and timely processing of your order.

To order a part that is not listed in the replaceable parts table, specify the following information:

1. Identification of the kit containing the part (refer to the product identification information supplied in Section 2).

2. Description and function of the part.

3. Quantity required.

Table 6-1. HP 27128A Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	27128-60001	2	1	CSGIO ASI	28480	27128-60001
C1	0160-4832	4	19	CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C2	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C2	0160-4835	7	13	CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C3	0180-0374	3	2	CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C4	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C5	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C6	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C7	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C8	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C9	0180-0228	6	1	CAPACITOR-FXD 22UF+-10% 15VDC TA	56289	150D226X9015B2
C10	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C11	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C12	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C13	0180-0100	3	1	CAPACITOR-FXD 4.7UF+-10% 35VDC TA	56289	150D475X9035B2
C14	0160-4807	3	2	CAPACITOR-FXD 33PF +-5% 100VDC CER 0+-30	28480	0160-4807
C15	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C16	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C17	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C18	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C19	0160-4807	3		CAPACITOR-FXD 33PF +-5% 100VDC CER 0+-30	28480	0160-4807
C20	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C22	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C23	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C24	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C25	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C26	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C27	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C28	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C29	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C30	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C31	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C32	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C33	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C34	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C35	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C36	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C37	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C38	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
CR1	1901-0518	8	2	DIODE-SM SIG SCHOTTKY	28480	1901-0518
CR2	1901-0518	8		DIODE-SM SIG SCHOTTKY	28480	1901-0518
CR3	1902-3002	3	1	DIODE-ZNR 2.37V 5% DO-7 PD=.4W TC=-.074%	28480	1902-3002
CR4	1990-0486	6	1	LED-LAMP LUM-INT=1MCD IF=20MA-MAX BVR=5V	28480	5082-4684
F1	2110-0301	1	2	FUSE .125A 125V .281X.093	28480	2110-0301
F2	2110-0301	1		FUSE .125A 125V .281X.093	28480	2110-0301
F3	2110-0099	4	1	FUSE 1A 125V .281X.093	28480	2110-0099
Q1	1853-0015	7	1	TRANSISTOR PNP SI PD=200MW FT=500MHZ	28480	1853-0015
Q2	1854-0019	3	1	TRANSISTOR NPN SI TO-18 PD=360MW	28480	1854-0019
R1	0757-0442	9	22	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R2	0757-0405	4	1	RESISTOR 162 1% .125W F TC=0+-100	24546	C4-1/8-T0-162R-F
R3	0698-0082	7	3	RESISTOR 464 1% .125W F TC=0+-100	24546	C4-1/8-T0-4640-F
R4	0698-0082	7		RESISTOR 464 1% .125W F TC=0+-100	24546	C4-1/8-T0-4640-F
R5	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R6	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R7	0757-0346	2	2	RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R8	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R9	0698-0082	7		RESISTOR 464 1% .125W F TC=0+-100	24546	C4-1/8-T0-4640-F
R10	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R11	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R12	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R13	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R14	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R15	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R16	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R17	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R18	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R19	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R20	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R21	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R22	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R23	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R24	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R25	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-1. HP 27128A Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
R26	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R27	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R28	0698-3405	4	1	RESISTOR 422 1% .5W F TC=0+-100	28480	0698-3405
R28	0698-4590	0	1	RESISTOR 422 1% .25W F TC=0+-100	24546	C5-1/4-T0-422R-F
R29	0698-3476	9	12	RESISTOR 6K 1% .125W F TC=0+-100	03888	PME55-1/8-T0-6001-F
R30	0698-3476	9		RESISTOR 6K 1% .125W F TC=0+-100	03888	PME55-1/8-T0-6001-F
R31	0698-3476	9		RESISTOR 6K 1% .125W F TC=0+-100	03888	PME55-1/8-T0-6001-F
R32	0698-3476	9		RESISTOR 6K 1% .125W F TC=0+-100	03888	PME55-1/8-T0-6001-F
R33	0698-3476	9		RESISTOR 6K 1% .125W F TC=0+-100	03888	PME55-1/8-T0-6001-F
R34	0698-3476	9		RESISTOR 6K 1% .125W F TC=0+-100	03888	PME55-1/8-T0-6001-F
R35	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R36	0698-3476	9		RESISTOR 6K 1% .125W F TC=0+-100	03888	PME55-1/8-T0-6001-F
R37	0698-3476	9		RESISTOR 6K 1% .125W F TC=0+-100	03888	PME55-1/8-T0-6001-F
R38	0698-3476	9		RESISTOR 6K 1% .125W F TC=0+-100	03888	PME55-1/8-T0-6001-F
R39	0698-3476	9		RESISTOR 6K 1% .125W F TC=0+-100	03888	PME55-1/8-T0-6001-F
R40	0698-0083	8	1	RESISTOR 1.96K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1961-F
R41	0698-3476	9		RESISTOR 6K 1% .125W F TC=0+-100	03888	PME55-1/8-T0-6001-F
R42	0698-3476	9		RESISTOR 6K 1% .125W F TC=0+-100	03888	PME55-1/8-T0-6001-F
R43	0757-0199	3	3	RESISTOR 21.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2152-F
R44	0757-0199	3		RESISTOR 21.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2152-F
R45	0757-0199	3		RESISTOR 21.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2152-F
R46	0698-3447	4	1	RESISTOR 422 1% .125W F TC=0+-100	24546	C4-1/8-T0-422R-F
S1	3101-2243	6	1	SWITCH- DIP 8 ROCKER	28480	3101-2243
U12	1820-2862	7	1	IC-DS 3667	28480	1820-2862
U13	1820-1633	8	3	IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U14	1820-1633	8		IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U15	1820-0684	7	1	IC INV TTL S HEX 1-INP	01295	SN74S05N
U23	1820-1633	8		IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U25	1820-1430	3	1	IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
U31	1820-2975	3	1	IC-BIC C2000	28480	1820-2975
U32	1820-2298	3	1	IC-Z80A CPU	28480	1820-2298
U35	1820-1112	8	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U45	1820-1322	2	1	IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U51	1818-1747	0	1	IC-EPROM 2764-250NS	28480	1818-1747
U51	27128-80002	5		1818-1747	28480	27128-80002
U51	1200-0567	1	2	SOCKET-IC 28-CONT DIP DIP-SLDR	28480	1200-0567
U52	1820-2301	9	1	IC-Z80A CTC	28480	1820-2301
U65	1820-1917	1	1	IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U75	1820-2024	3	1	IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U81	1818-1611	7	1	IC-16K RAM HM6116LP	54013	HM6116P-3
U81	1200-0567	1		SOCKET-IC 28-CONT DIP DIP-SLDR	28480	1200-0567
U82	1820-2300	8	1	IC-Z80A SIO/2	28480	1820-2300
U85	1820-1195	7	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS175N
U101	1810-0617	5	1	JUMPER ARRAY	28480	1810-0617
U101	1200-0607	0	1	SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
U102	1820-1204	9	1	IC GATE TTL LS NAND DUAL 4-INP	01295	SN74LS20N
U103	1820-1208	3	1	IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
U104	1820-1199	1	1	IC INV TTL LS HEX 1-INP	01295	SN74LS04N
U105	1820-1144	6	1	IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
U112	1820-2594	2	2	IC RCVR TTL LS LINE RCVR QUAD 2-INP	28480	1820-2594
U113	1820-2594	2		IC RCVR TTL LS LINE RCVR QUAD 2-INP	28480	1820-2594
U114	1820-1244	7	1	IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL	01295	SN74LS153N
U115	1820-1197	9	1	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U123	1820-2117	5	3	IC DRVR TTL LINE DRVR DUAL	07263	9636ATC
U124	1820-2117	5		IC DRVR TTL LINE DRVR DUAL	07263	9636ATC
U125	1820-2117	5		IC DRVR TTL LINE DRVR DUAL	07263	9636ATC
	1251-7276	0	1	CONNECTOR-80 PIN	28480	1251-7276
	1251-7884	6	1	CONNECTOR-50 PIN MALE	28480	1251-7884
	1480-0116	8	2	PIN-GRV .062-IN-DIA .25-IN-LG STL	28480	1480-0116
	7121-1010	9	1	LABEL-EPROMS	28480	7121-1010
	5041-3467	2	2	HPTO EXTRACTOR HANDLE	28480	5041-3467
	27128-80001	4	1	PC BOARD-BLANK	28480	27128-80001

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Manufacturer's Code List

MFR. NO.	MANUFACTURER NAME	ADDRESS	ZIP CODE
S4013	HITACHI	TOKYO, JP.	
01295	TEXAS INSTRUMENTS INC. SEMICONDUCTOR COMPONENTS DIV.	DALLAS, TX.	75222
03888	K D I PYROFILE CORP.	WHIPPANY, N.J.	07981
07263	FAIRCHILD SEMICONDUCTOR DIV.	MOUNTAIN VIEW, CA.	94042
24546	CORNING GLASS WORKS (BRADFORD)	BRADFORD, PA.	16701
28480	HEWLETT-PACKARD CO. CORPORATE HQ.	PALO ALTO, CA.	94304
56289	SPRAGUE ELECTRIC CO.	NORTH ADAMS, MA.	01247

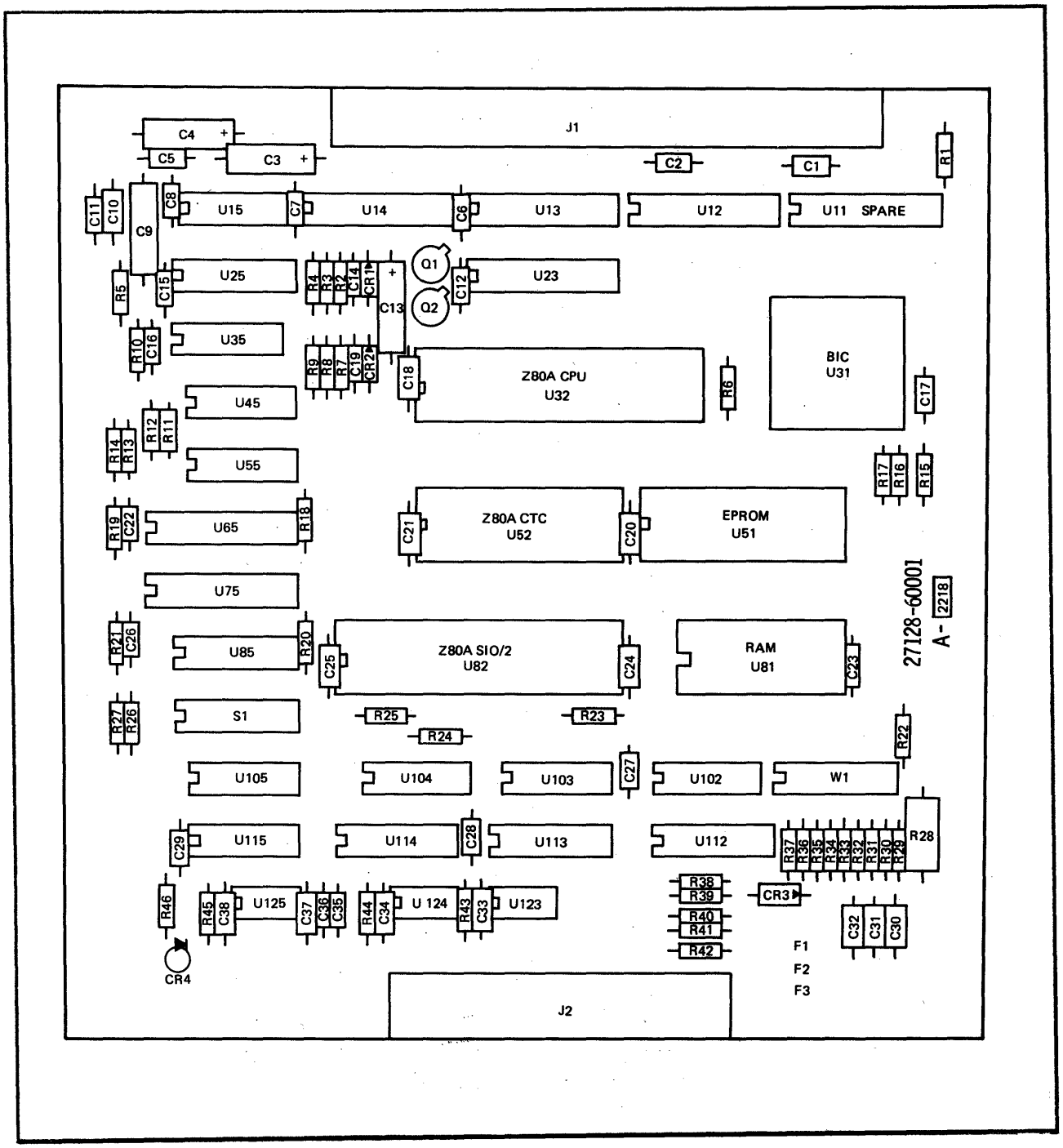


Figure 6-1. HP 27128A Parts Location Diagram

SCHEMATIC DIAGRAMS

SECTION VII

This section contains schematic logic diagrams for the ASI card.

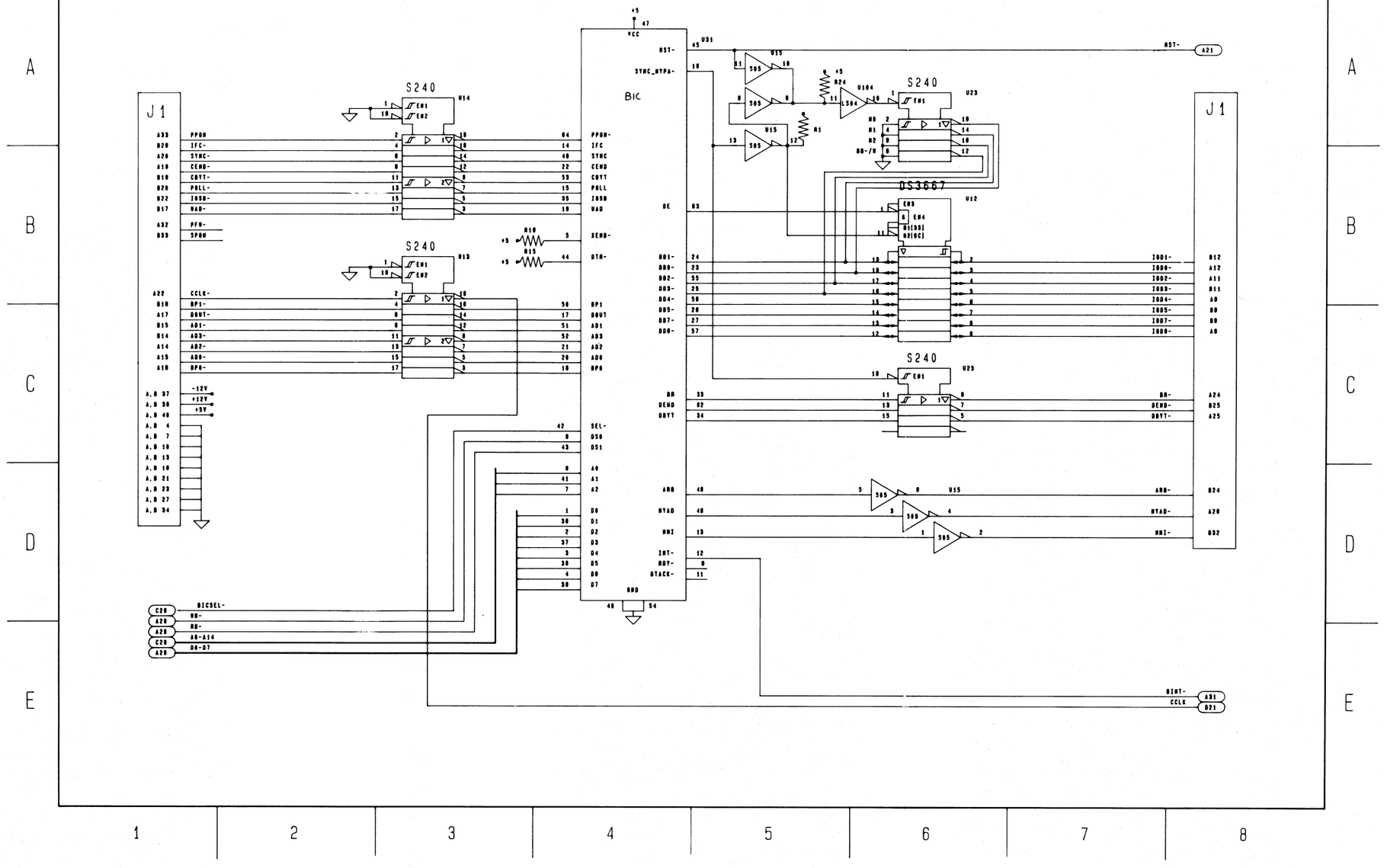


Figure 7-1. ASI Schematic Logic Diagram (Sheet 1 of 3)

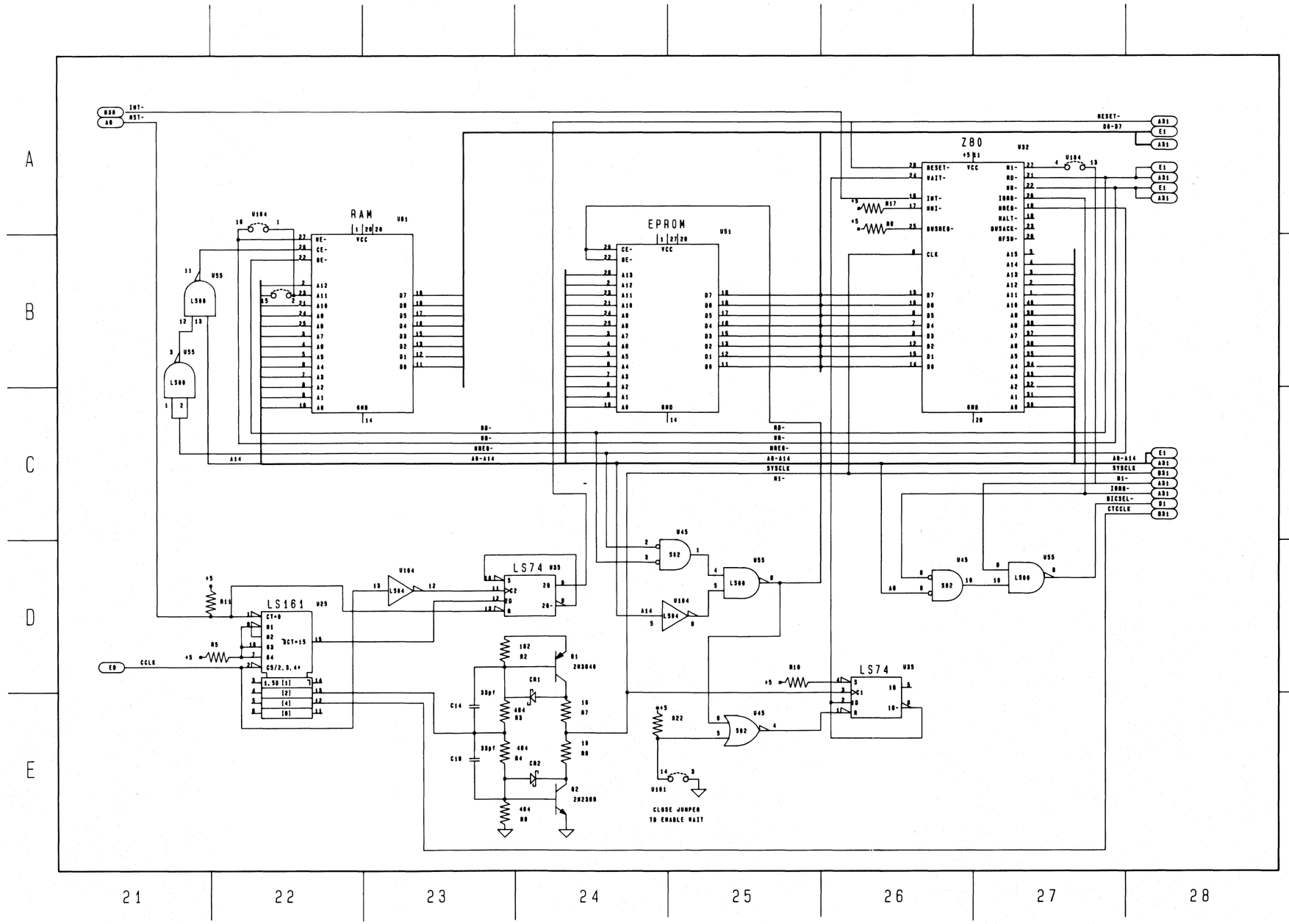


Figure 7-1. ASI Schematic Logic Diagram (Sheet 2 of 3)

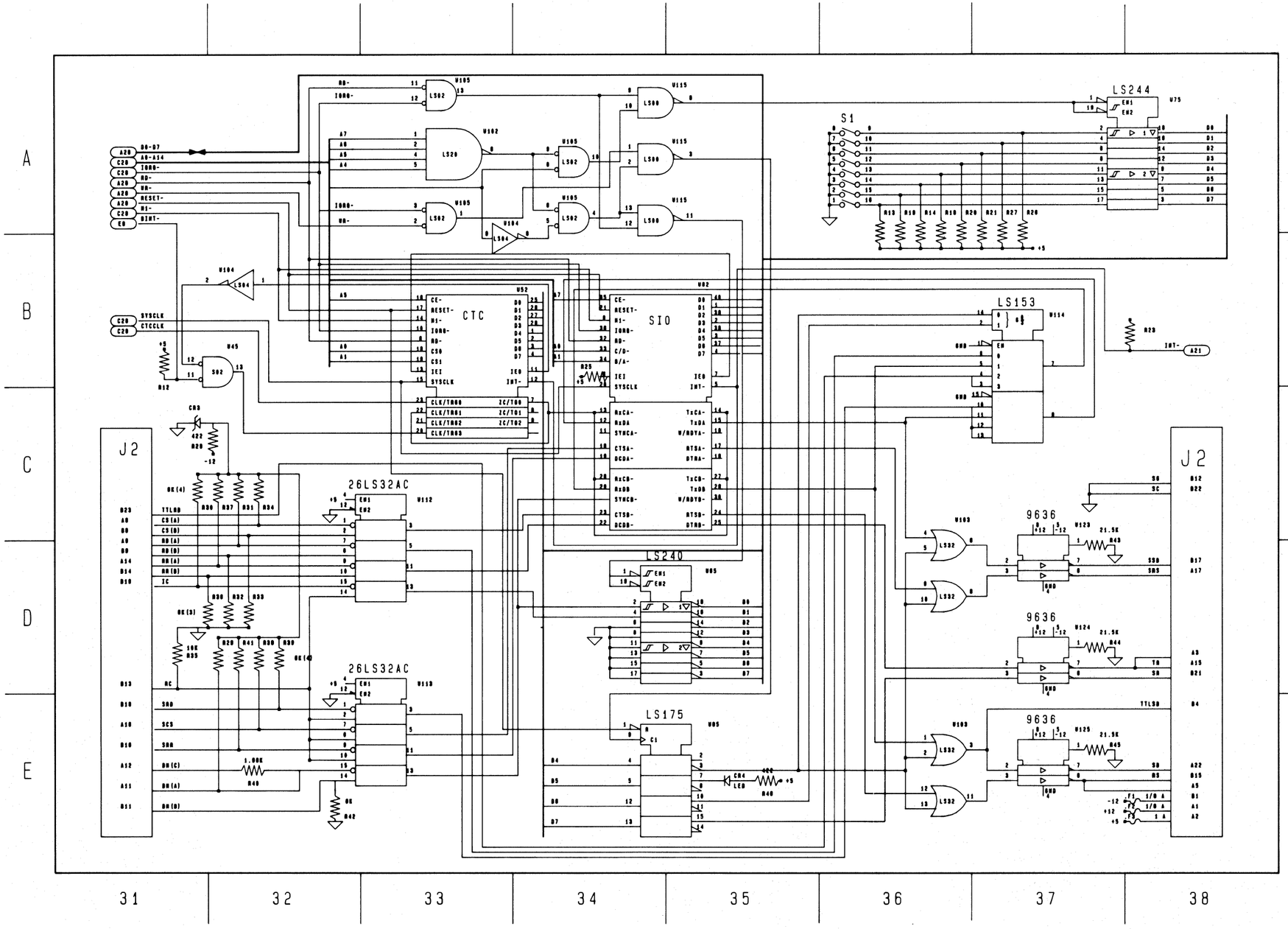


Figure 7-1. ASI Schematic Logic Diagram (Sheet 3 of 3)

ASCII CHARACTERS AND BINARY CODES

APPENDIX A

	0	1	2	3	4	5	6	7
0	NUL	DLE	sp	0	@	P	`	p
1	SOH	DC1	!	1	A	Q	a	q
2	STX	DC2	"	2	B	R	b	r
3	ETX	DC3	#	3	C	S	c	s
4	EOT	DC4	$	4	D	T	d	t
5	ENQ	NAK	%	5	E	U	e	u
6	ACK	SYN	&	6	F	V	f	v
7	BEL	ETB	'	7	G	W	g	w
8	BS	CAN	(	8	H	X	h	x
9	HT	EM	)	9	I	Y	i	y
A	LF	SUB	*	:	J	Z	j	z
B	VT	ESC	+	;	K	[	k	{
C	FF	FS	,	<	L	\	l	|
D	CR	GS	-	=	M	]	m	}
E	SO	RS	.	>	N	^	n	~
F	SI	US	/	?	O	_	o	DEL

INDEX

A

B

C

INDEX

C (Continued)

D

E

F

INDEX

H

I

J

L

M

N

O

INDEX

P

Q

R

S

INDEX

S (Continued)

T

W

Z

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June, 1983

HEWLETT-PACKARD COMPANY
Roseville Networks Division
8000 Foothills Boulevard
Roseville, California 95678