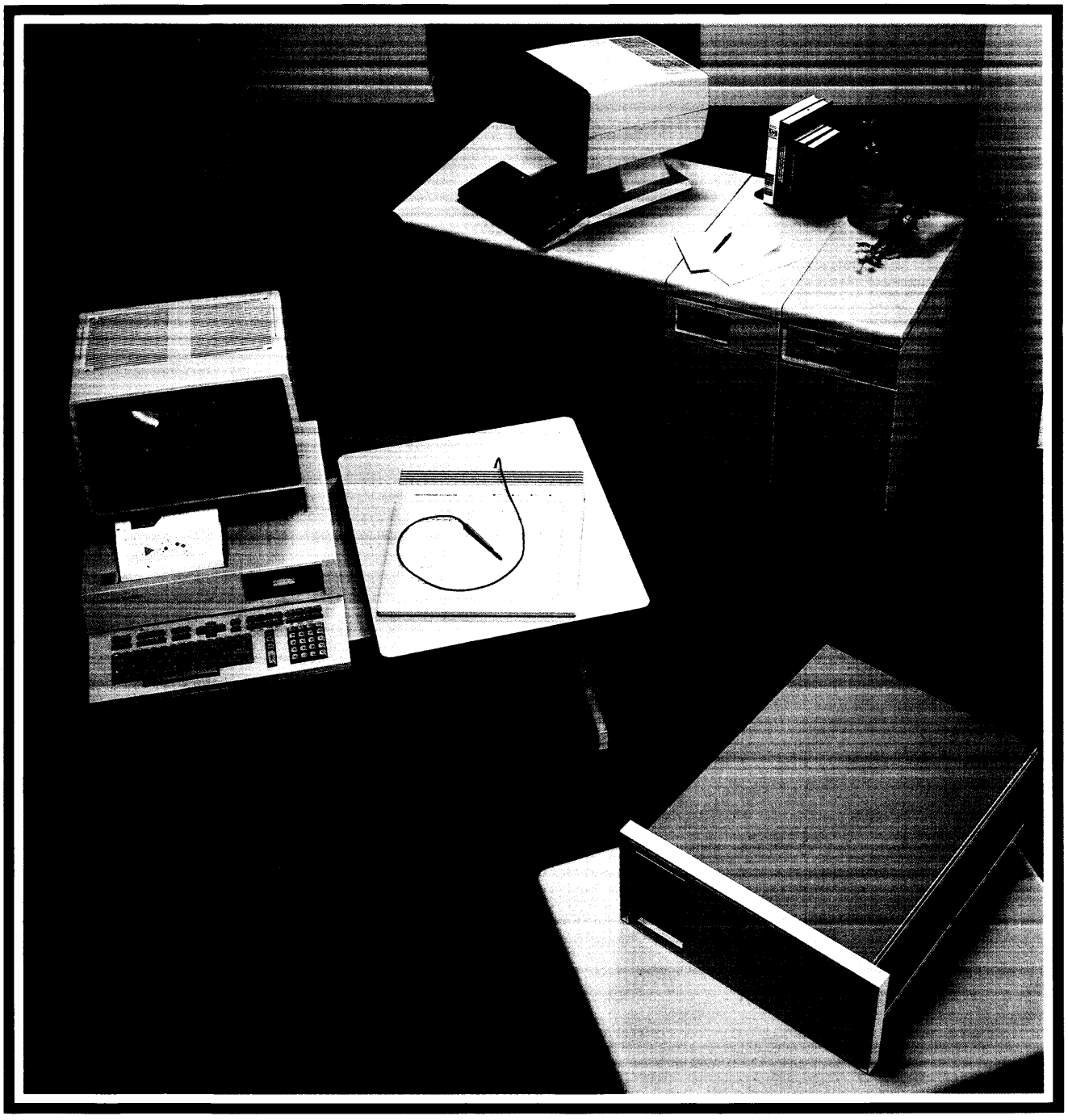
HEWLETT PACKARD

HP 97060A Graphics Processor Service Manual



HP 97060A Graphics Processor Service Manual

Part No. 97060-90030

Hewlett-Packard Company
3404 East Harmony Road, Fort Collins, Colorado 80525

Printing History

New editions of this manual will incorporate all material updated since the previous edition. Update packages may be issued between editions and contain replacement and additional pages to be merged into the manual by the user. Each updated page will be indicated by a revision date at the bottom of the page. A vertical bar in the margin indicates the changes on each page. Note that pages which are rearranged due to changes on a previous page are not considered revised.

The manual printing date and part number indicate its current edition. The printing date changes when a new edition is printed. (Minor corrections and updates which are incorporated at reprint do not cause the date to change.) The manual part number changes when extensive technical changes are incorporated.

November 1983...First Edition

| August 1984...First Edition with update

97060-90030, rev: 8/84

Table of Contents

Chapter 4. Assembly Access

Chapter 5. Replaceable Parts

Figures

Tables

Chapter 1
General Information

Introduction

Note

Hewlett-Packard assumes no responsibility for customer repairs or modifications.

This manual contains servicing information for the Hewlett-Packard (HP) 97060A Graphics Processor (hereinafter referred to as the 97060A). HP supports repairing the 97060A to the assembly level, that is, isolating the problem to the replaceable assembly. Then the defective assembly is exchanged for a new or rebuilt assembly.

This chapter contains general information about the 97060A and its servicing.

Additional information in this manual includes:

- Theory of Operation
- Testing and Troubleshooting Procedures
- Assembly Access Procedures
- Replaceable Parts

Complete installation instructions are provided in the HP 97060A Graphics Processor Installation Note, part number 97060-90001.

Description

The HP 97060A is a high-performance graphics processor. The 97060A has eight planes of 1024 X 1024 pixels.

Installation consists of unpacking, connecting power, connecting the RGB coax cables to the monitor, and connecting the interface cable to the GPIO card in the HP 9000 Series 500 computer.

The 97060A has refresh rate and voltage options which are preset at the factory. Refer to 33/60 Hz Display Mode Selection and Voltage Options which follow in this chapter for additional information.

Extensive self-test capability is built into the 97060A, and the **READY** light on the front panel gives a highly reliable indication that the self-tests have passed. Normally, the **READY** light turns on about 8 seconds after the **ON** light turns on at powerup. However, if a fault occurs, the **READY** light does not turn on.

Environmental Specifications

Temperature:	−40°C to +75°C non-operating 0°C to +55°C operating	
Humidity:	+40°C @ 95% non-condensing operating	
Vibration: (operating)	Cycle range: Amplitude (p-p): Sweeptime: Dwell: Amplitude:	5-55-5 Hz 0.015 inch 1 minute per octave, 15 minutes total 10 minutes each resonance 0.125 inch @ 5-10 Hz 0.060 inch @ 10-25 Hz 0.015 inch @ 25-55 Hz
Shock: (non-operating)	Magnitude: Duration: No. of shocks: Waveform: Bench drop:	30 G 11 msec 18 (3 each on 6 surfaces) Half sine 4-inch tilt
Altitude:	50,000 feet, 0-55°C, non-operating 15,000 feet, 0-55°C, operating	
Drop Test: (non-operating, packaged)	30 inches each face and corner	
EMI:	VDE Class A FCC Class A	
Safety:	UL114 (Office Machines) UL478 (EDP) CSA154 (EDP) IEC380 (Office Machines with Amendment 1) IEC435 (EDP 1982)	

Electrical Characteristics

Rated Line Voltage:	Low Range:	90 to 132V ac
	High Range:	180 to 264V ac
Frequency Range:	47 to 66 Hz	
Power Dissipated:	<100W; 85W typical	
Supply Ratings:	+5V @ 20A −5V @ 12A	
Fuse:	4A Low Voltage Range, fast blow 6.3A High Voltage Range, fast blow	
Video:	RS-343 compatible. 1V p-p with sync on Green. 0.7V video, 0.3V sync within 5%	

Functional Specifications

Resolution:	1024 X 768 @ 33 Hz interlaced 736 X 552 @ 60 Hz non-interlaced Other options are soft programmable, such as 640 X 480, 30 Hz, RS-170
Host Interface:	Compatible with HP 27112A General Purpose I/O (GPIO) Interface Card with Option 001 interface cable
Tablet Interface:	Compatible with HP 9111A Data Tablet
Self Test:	>90% of IC failures detected Data bus counter check Bit slice register increment check Loop counter check I/O loopback check Scratchpad RAM check, load with address Memory test: write all 1s, 0s, 1s, 0s; read back Write Mask, Write Data, check with read back Vector drawing test followed by signature read
Reset:	Power up causes full self-test Host reset causes full self-test

33/60 Hz Display Mode Selection

The 97060A may be set for either 33 or 60 Hz frame refresh rate (display mode), as follows:

Access the controller pc assembly according to procedures in Chapter 4. Two jumpers near U291 on the controller pc assembly determine display mode selection. Ensure that both jumpers are in either the 33 Hz or the 60 Hz positions, depending on the monitor used. See Figure 1-1 for 33/60 Hz jumper positions. The other four jumpers are set at the factory and should not be changed. Ensure that they are in the positions shown in Figure 1-1.

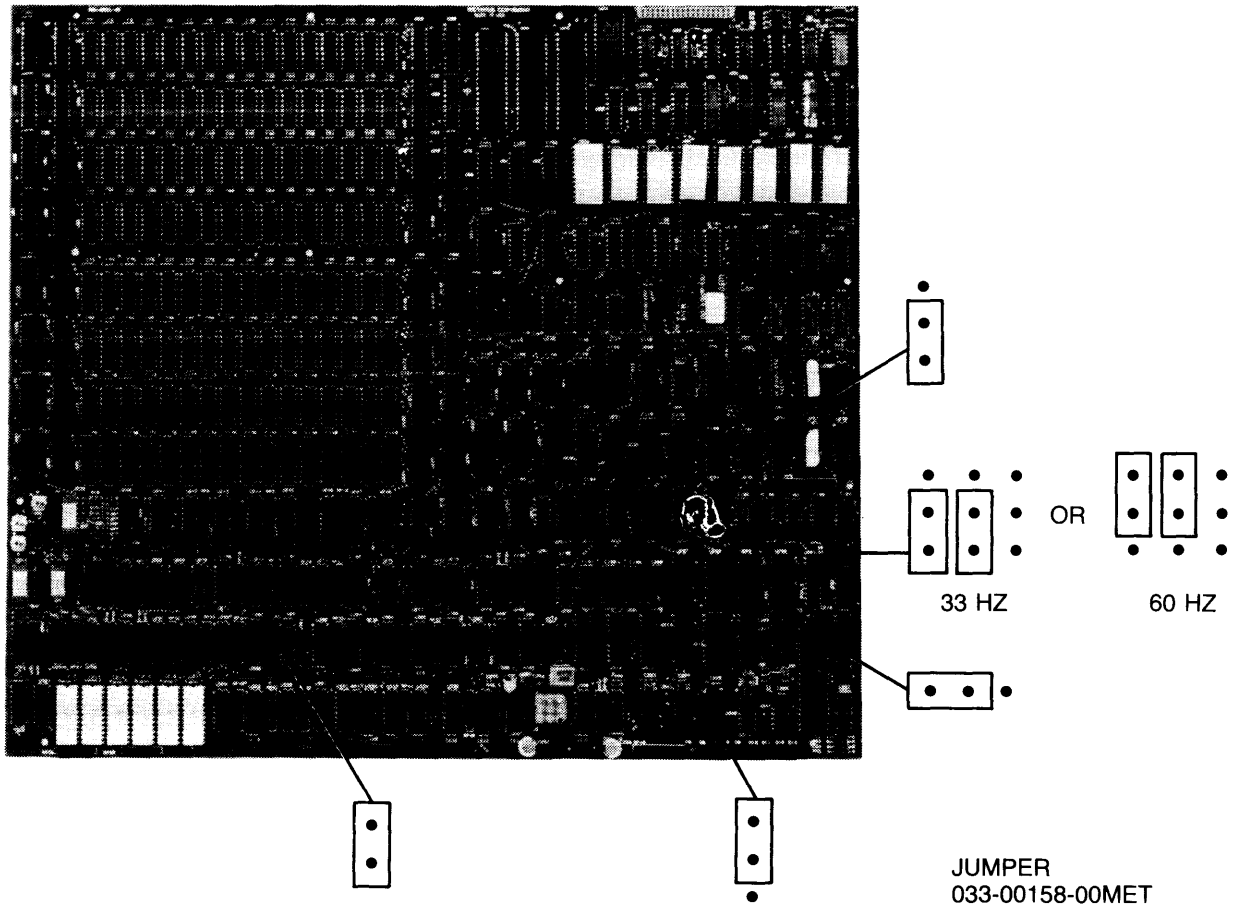


Figure 1-1. Controller Pc Assembly Jumpers

Parallel Interface Pc Assembly Jumpers

Four jumpers are contained on the parallel interface pc assembly (Figure 1-2). Three concern handshaking, the fourth concerns the INIT signal. The jumpers are set at the factory and should not be changed. Ensure that they are in the positions shown in Figure 1-2.

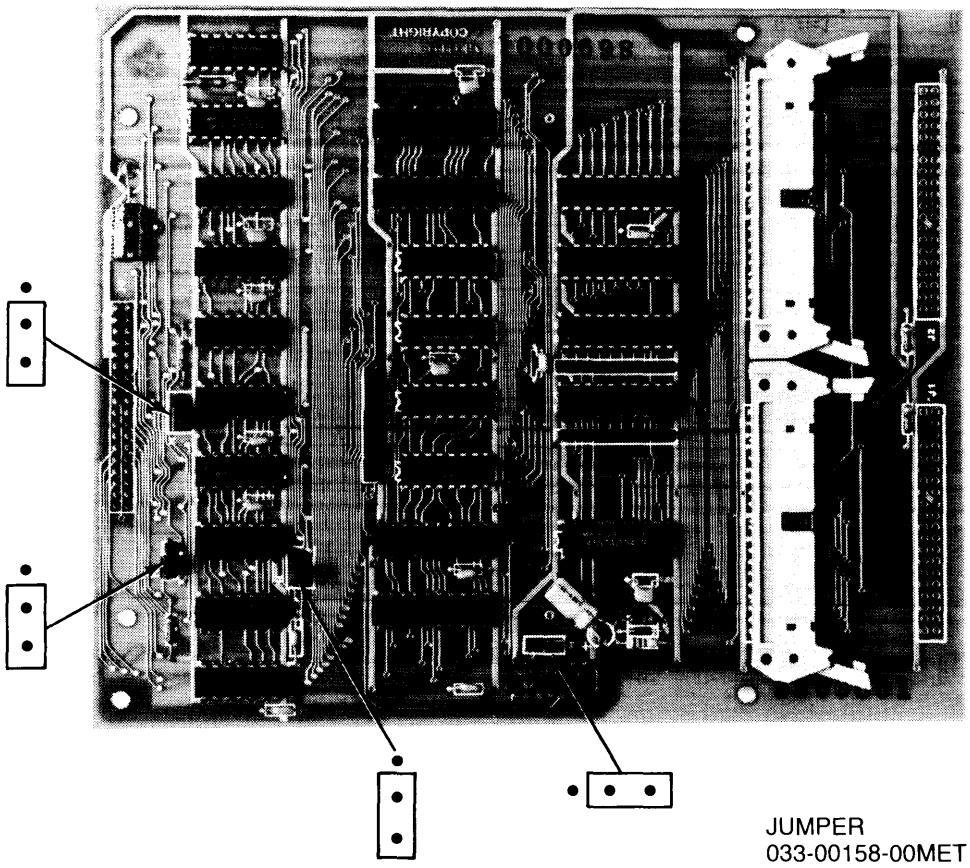


Figure 1-2. Parallel Interface Pc Assembly Jumpers

GPIO Interface Card Switch Settings

The HP 27112A General Purpose I/O (GPIO) Interface Card interfaces the HP 9000 Series 500 computer to the 97060A. The GPIO card switches should be set as follows. Note that a switch that is up is in the open position and represents a logic one; a switch that is down is in the closed position and represents a logic zero.

SW1: S1 through S8 - Down

SW2: S1, S2, and S5 - Up
S3 and S4 - Down

Warnings, Cautions, and Notes

Warnings, cautions, and notes are used in this manual. Warnings call attention to potential hazards for personnel. Cautions call attention to potential hazards for equipment. Notes emphasize important information or instructions.

Repair Philosophy

The 97060A is repaired at an assembly replacement level. Parts that are most commonly replaced are exchange parts and are on the Computer Support Division (CSD) exchange program. When an exchange part fails, it should be returned to CSD for repair, and a rebuilt part should be obtained. If a new part is purchased instead, it is unnecessary to return the failed part. Chapter 5 contains a list of all replaceable parts. Tables in Chapter 5 also list exchange parts with new and rebuilt part numbers and module-level non-exchange parts.

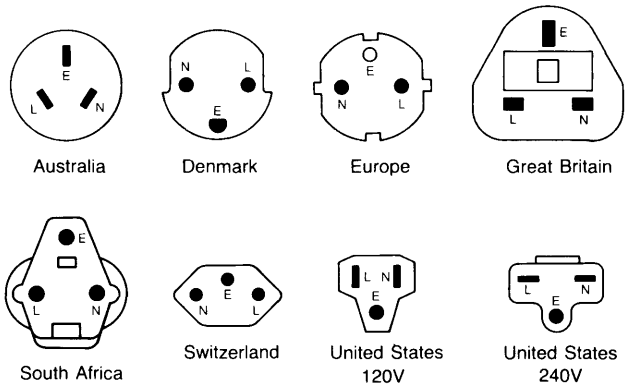
Ac Components/Power Cord

A detachable ac power cord plugs into an ac outlet to provide primary power to the 97060A. Other ac components are an on/off **POWER** switch, line fuse, line filter, fan, and wiring.

WARNING

IF IT IS NECESSARY TO REPLACE THE POWER CORD, THE REPLACEMENT CORD MUST HAVE THE SAME POLARITY AS THE ORIGINAL CORD. OTHERWISE, A SHOCK HAZARD MIGHT EXIST WHICH COULD RESULT IN INJURY OR DEATH. ALSO, THE EQUIPMENT COULD BE SEVERELY DAMAGED IF EVEN A RELATIVELY MINOR INTERNAL FAILURE OCCURRED.

Power cords with different plugs are available for the 97060A; plug configurations are shown in Figure 1-3. Each plug has a ground connector. The cord packaged with the 97060A depends upon where the equipment is to be delivered. If your equipment has the wrong power cord for your area, please contact your local HP Sales and Support Office.



Country	Part Number	Opt.	Voltage
Australia	8120-1369	901	250V, 6A
Denmark	8120-2956	912	250V, 6A
Europe	8120-1689	902	250V, 6A
Great Britain	8120-1351	900	250V, 6A
South Africa	8120-4211	917	250V, 10A
Switzerland	8120-2104	906	250V, 6A
United States	8120-1378	903	120V, 10A
United States	8120-0698	904	240V, 10A

NOTE: Plugs are viewed from connector end. Shape of molded plug may vary within country.

Power cords supplied by HP have polarities matched to the power-input socket on the computer:
- L = Line or Active Conductor (also called "live" or "hot")
- N = Neutral or Identified Conductor
- E = Earth or Safety Ground

Figure 1-3. Power Cords

Voltage Options

The 97060A is configured at the factory for either 110V or 220V input line voltage. Table 1-1 lists the parts which are unique to the 110V and 220V options. Figure 1-4 shows power supply jumper configurations for the voltage options.

Table 1-1. Voltage Configuration Part Numbers

Description	110V	220V
Power cord	8120-1378	Country dependent
Fan	050-00342-00MET	050-00694-00MET
Line fuse	2110-0055	2110-0715

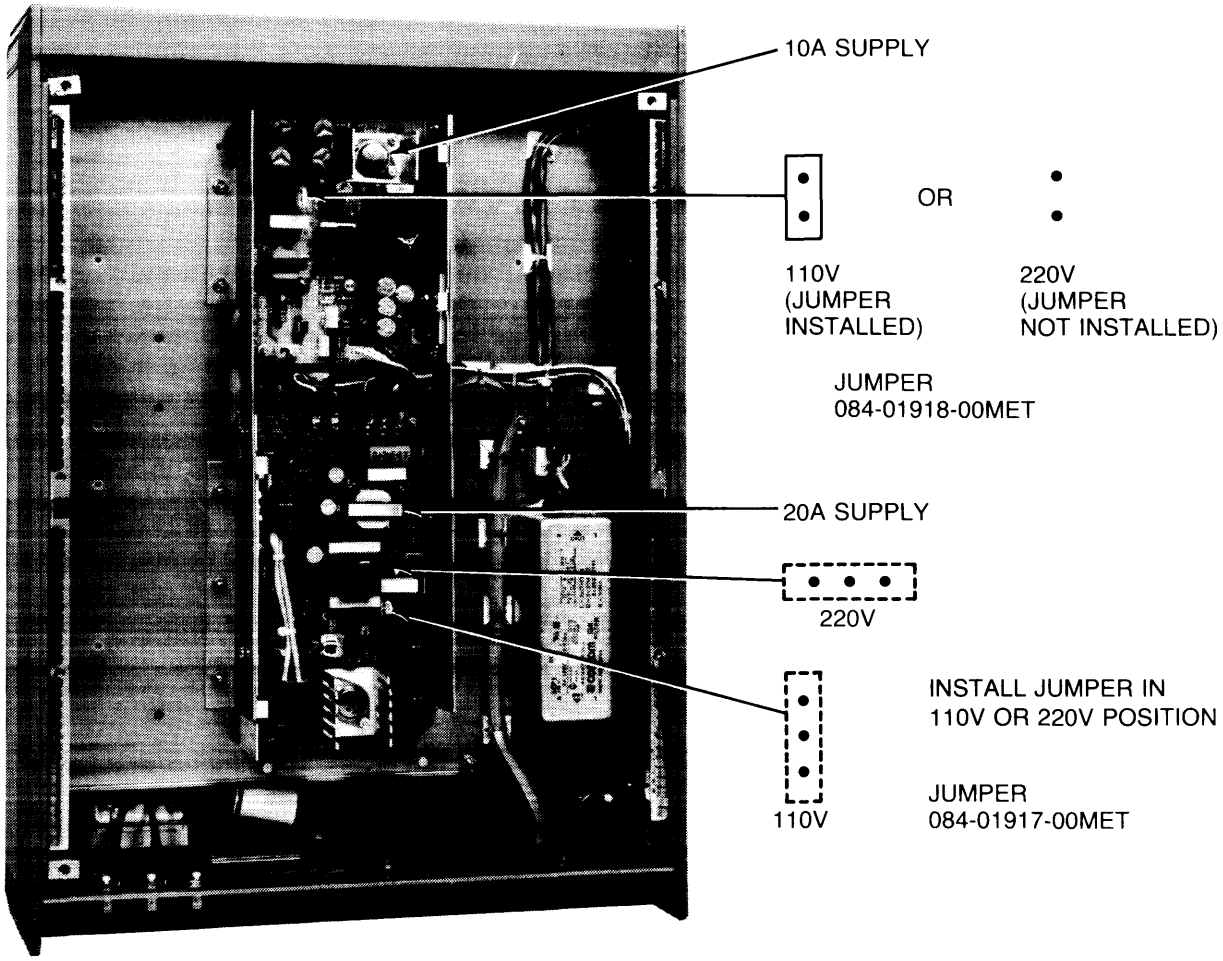


Figure 1-4. Power Supply Voltage Jumpers

Grounding Requirements

To protect operating personnel, the National Electrical Manufacturers' Association (NEMA) recommends that the 97060A chassis be grounded. The 97060A is equipped with a three-conductor power cable which, when connected to an appropriate power receptacle, grounds the computer chassis.

Safety

WARNING

LETHAL VOLTAGES ARE PRESENT INSIDE THE 97060A. OBSERVE ALL WARNINGS IN THIS MANUAL, AND OBSERVE THE FOLLOWING SAFETY PROCEDURES.

- Do all possible operations with the 97060A unplugged from the power source.
- If installation, maintenance, or repair must be done with the 97060A energized, take the following precautions:
    a. Never work alone in high-voltage areas. In case of accidental shock, a life may depend on rapid removal from the energized source and appropriate first-aid action.
    b. Personnel working in high-voltage areas should know where to obtain respiratory resuscitation and/or cardiopulmonary resuscitation (CPR), in case a fellow worker needs assistance.
    c. In case of burns, treat only after the person is breathing and has a normal heartbeat.
- If primary wiring change is made, perform continuity test between power cord ground and metal chassis. Record results on Repair Order.

Chapter 2
Theory of Operation

Introduction

The HP 97060A is a high-performance raster graphics processor constructed from a mixture of MOS and bipolar ECL technology. The architectural components include:

- Bit-slice processor with 64-bit microword
- Megabyte of dynamic RAM (DRAM), organized as eight megabit planes of 1024 X 1024
- Integrated signature analyzer
- Hardware pan and zoom
- Line and area pattern generators
- EPROM-based character generator
- 36 MHz pixel clock

System

Communications with the HP 9000 computer is via the 16-bit parallel interface with the HP 27112A GPIO interface card and its Option 001 2.5-metre cable.

An HPIB graphics tablet interface option is supported, allowing a local cursor to track the tablet stylus. The HP 9111A Data Tablet is the supported device.

Figure 2-1 shows a fully configured system.

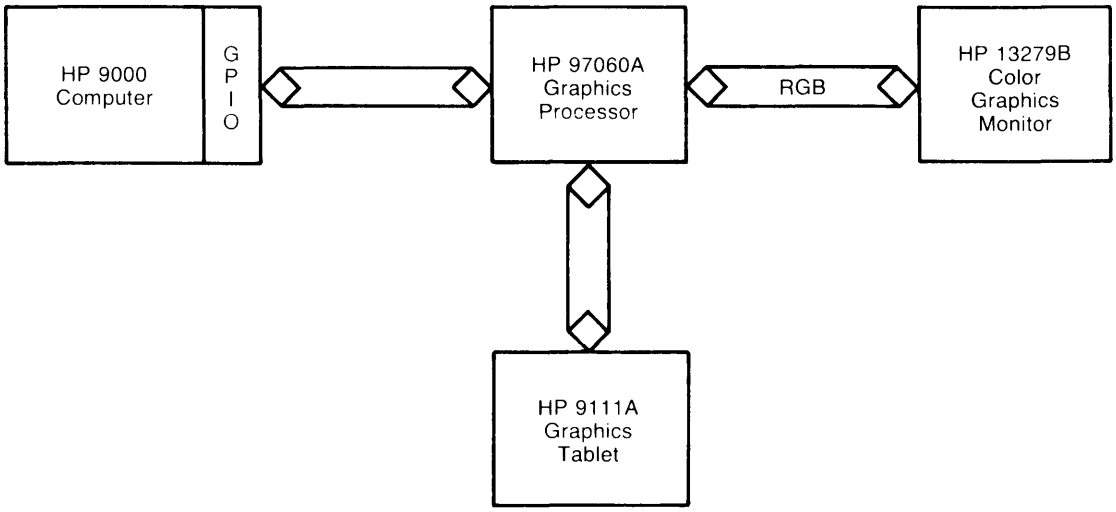


Figure 2-1. System Block Diagram

The link between the computer and 97060A is bidirectional. The computer sends op codes and arguments in the 97060A syntax, and thus builds a picture in display memory. The computer may also read display memory or 97060A status.

The link to the graphics tablet is also bidirectional, although the tablet functions primarily as a sender. The tablet is software configurable and can be set under host control.

The link between the 97060A and monitor is three coaxial cables carrying composite video conforming to the RS-343 standard for RGB transmission.

97060A Graphics Processor

Figure 2-2 is a block diagram of the 97060A hardware. Access to the dynamic RAM bit-map is shared by the processor and screen refresh circuitry.

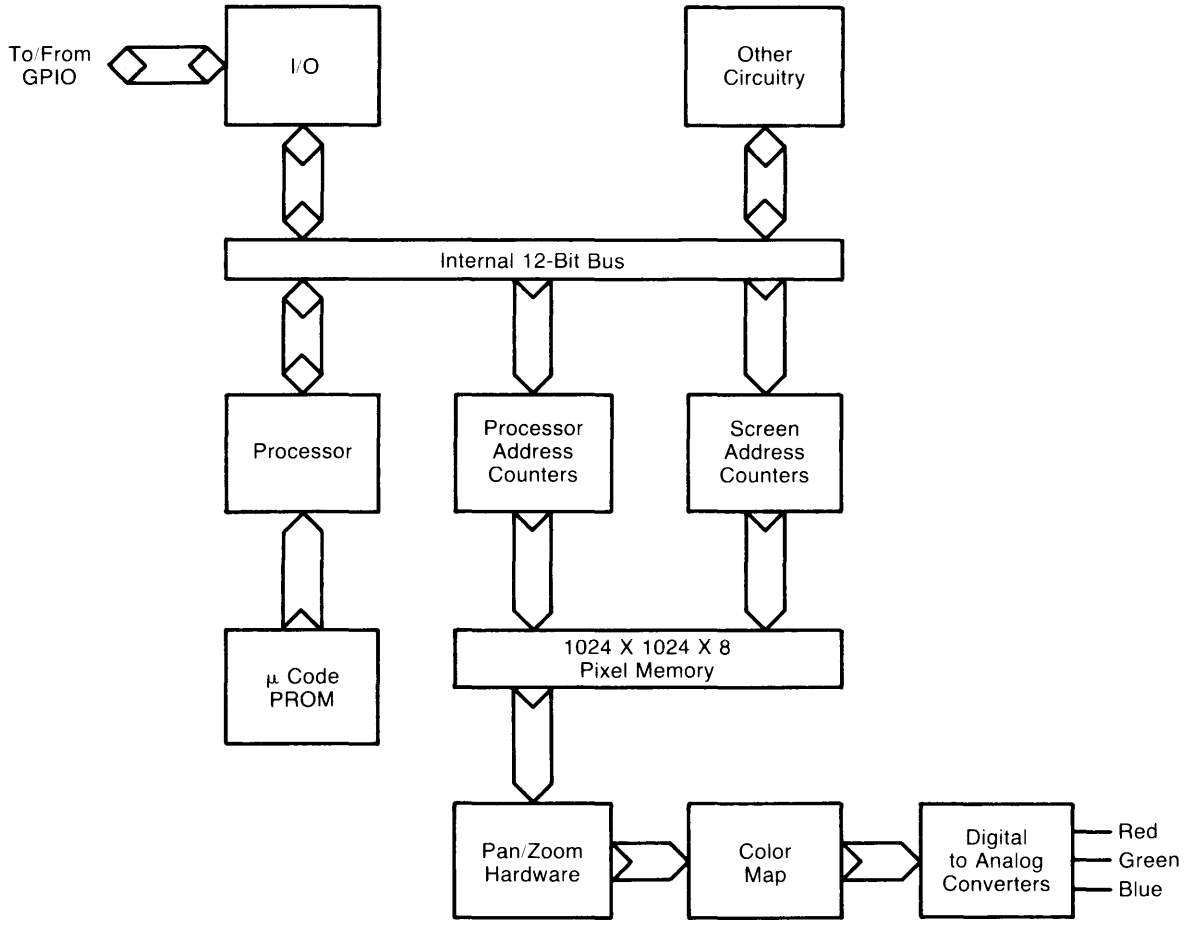


Figure 2-2. 97060A Block Diagram

The functions of the 97060A blocks are as follows:

I/O

This is the interface port to the HP 9000. The 97060A communicates with a "2-wire" handshake, PCTL and PFLG.

Processor

Composed of three 2901B bit slices, the 12-bit processor runs at a 220 ns cycle time.

Microcode PROM

This is a 64-bit-wide PROM array controlling processor ALU, source and destination for data transfers, load of the processor counters, and other important 97060A functions. Only the high speed functions such as memory cycle timing are performed independently, in state machines or random logic.

Processor Address Counters

These two 12-bit counters, one for X and one for Y, respond to the commands Load, Up/Down, and Count.

Screen Address Counters

These two counters, a 6-bit counter for X and a 10-bit counter for Y, only count up. However, they can be loaded with a start count other than zero to achieve the Pan function. They are automatically loaded on each vertical retrace. Counting can be prescaled by a modulo Zoom value.

Pixel Memory

Pixel memory consists of 128 DRAMs, 16 chips of 64K bits per plane. Memory is organized such that blocks of 16 adjacent pixels on a raster line are each contributed by a different DRAM output. Memory operates at a 220 ns write cycle and a 440 ns read cycle. The eight planes are individually addressable through the Write Mask, Write Data, and Read Mask. These are each 8-bit registers with a flip-flop for each of the eight planes. Only when the Write Mask is set for a particular plane is its write enable line allowed to pulse. When written, the value of the particular Write Data flip-flop determines whether a 1 or a 0 is written. The Read Mask affects the planes read out and has no effect on data read by the processor.

In the following example, plane 0 is neither read nor written. Plane 1 is written with a 1, and is viewed. Plane 2 is not written, but is viewed. Plane 3 is written with a 0, and viewed. Plane 4 is written with a 1, and not viewed, and so forth.

Example:

Plane	Write Mask	Write Data	Read Mask
0	0	1	0
1	1	1	1
2	0	1	1
3	1	0	1
4	1	1	0
5	0	0	1
6	1	0	1
7	1	1	0

Pan/Zoom

This circuitry contains modulo counters which essentially mirror the function of the screen address counters. Zoom is achieved by slowing down the entire pipeline from DRAM to the output digital-to-analog converters, causing pixel replication. Pan is achieved primarily by the screen address counters, but these only address 16 contiguous pixel blocks. To obtain a finer offset, a circular buffer is used as a programmable delay line.

Color Map

The 8-bit path through Pan/Zoom continues to the Color Map, a 256 X 24 RAM that allows the user to work with 256 colors simultaneously from a palette of 16.7 million colors.

Digital to Analog Converters

The 24 bits from the Look Up Table are broken into three groups and routed to three 8-bit Digital to Analog Converters: Red, Green, and Blue. Composite sync is added to the Green output to create a 1V p-p signal.

Microcode Word Definition

The 64-bit microcode word resides in eight 16K PROMs, allowing 2048 steps of control memory. These PROMs are addressed by a 12-bit sequencer comprising two 2911As and a 2909A. The sequencer in turn is driven by microcode control bits and branching conditions from various sections of the hardware. The next section will explain these conditions in more detail.

The microcode word is subdivided into five major groups called fields:

- Control Field. These 13 bits of control lines regulate the processor address counters, the write enable generator for pixel memory, and other functions described below.
- Data Bus Source and Destination Control. Every instruction must specify a driver and a receiver for the internal data bus. This occurs even if no actual data transfer is required, in which case the destination is a dummy location. The sub-fields are:

Data Source	3 bits
Data Destination	5 bits

- Conditional Branch Control. These 11 bits directly control the activity of the microcode sequencer, which in turn selects the next microcode word decoded. There are three sub-fields:

Branch Type	3 bits
Condition Code	8 bits

- Bit Slice ALU Controls. These 20 bits specify internal action of the three 2901B bit slice parts. There are five sub-fields:

External Carry/Borrow	3 bits
ALU Destination	3 bits
ALU Function	3 bits
ALU Source	3 bits
Register Address	8 bits

- Data Field. The microcode often must drive the data bus, either to load the ALU with a constant operand, preset data bus destinations to some value, specify a branch location to the sequencer, or other operation. This is a single 12-bit field.

Op Codes

Unless otherwise specified, all writes to pixel memory observe the Write Data, Write Mask, and present Area Pattern. That is, a write in plane k occurs only if bit k of the Write Data Register and Write Mask Register are = 1 and the present Area Pattern function A(x,y) = 1.

Byte arguments are indicated by lower case, word arguments by upper case. Word arguments are read in the order: low byte, high byte.

The following are state variables:

P1 (pointer 1)
P2 (pointer 2)
WRITE DATA (also called "current color")
WRITE MASK (determines planes written)
PATTERN REGISTER (including line and area patterns)
READ MASK (planes viewed)
BLANK
BLINK
CMAP (contents of 256 locations)
CONFIGURATION (33 Hz, 8 planes, tablet)
SETCORN, SETCSZ, FSIZE, CSPACE (character information)
SZCUR (cursor size)
CURRENT POLYGON STRUCTURE (vertex list)

Mnemonic	Hex	Description
AFILL1	68	Read pixel at P1 Do while neighbor color = P1 pixel color Write neighbor with Write Data End P1 and P2 unmodified.
AFILL2 <f>	69	Read pixel at P1 Do until neighbor color = f Write neighbor with Write Data End P1 and P2 unmodified
ARC <l>	62	Draw arc of length l using Write Data and center of curvature P1. Begin at P2. P2 left at end of arc upon completion. 0<l<2047.
BLANK <b>	4B	b is LSB of argument byte. If b = 1 then blank screen and give processor access. If b = 0 then return to screen-priority mode.
BLINK <b>	4D	b is LSB of argument byte. If b = 1 then toggle plane 7 at 2 Hz, using Read Mask. If b = 0 then restore steady plane 7.
CHAR <c1,c2...cn>	6B	Draw text starting with P1 pointing to the lower left corner of the 16 X 8 character cell. c1, c2, etc., are ASCII codes 0-127. cn is the ESC character (#27) and terminates text mode. See also SETCSZ, FSIZE, and CSPACE. Control characters decoded: CR Return to left margin LF Move pointer down one line BS Move pointer back one space ESC Exit text mode
CLEAR	60	Fill screen with Write Data.
CMAP <a,r,g,b>	51	Load color map location a with values r, g, and b.
COMPDR	72	Draw a vector between P1 and P2 complementing present pixel values. Leave P1 at P2. WRMASK and SETCOL not used.
CRTWR <r,d>	46	Write the 6845-1 CRT Controller Register r with d.
CSPACE <Δx,Δy>	48	Auto increment between successive characters. Apply increment Δx,Δy from lower left corner of cell, then apply transformation specified by SETORN.
CURS	71	Draw cursor at P1. Drawn in complement mode, with crosshair width and height as set by SZCUR. Automatically removed upon receipt of next op code. Write Mask and Area Pattern ignored.
DRAW	61	Draw vector from P1 to P2. Leave P1 at P2.
FFILL	65	Fill rectangle defined by diagonal P1,P2. Approximately 16 times faster than RECT2; no patterns allowed.
FSIZE <Δx,Δy>	49	Font size. 0<Δx≤8, 0<Δy≤16. These define a window on the 16 X 8 character cell.

<table>
<tr><th>Mnemonic</th><th>Hex</th><th>Description</th></tr>
<tr><td>GRAFIN <f></td><td>4A</td><td>
Set Graphic Input (from tablet). The argument (f), which is the GRAFIN mode select byte, selects the current GRAFIN mode. It is one of the following:

0 Software INIT Mode. This mode resets all GRAFIN attributes to their default values and clears the coordinate queue. The offset and scale factors are also reset to their default values.

The GPIB tablet interface pc assembly sends the following to the graphics tablet:

The DEVICE CLEAR signal.

The IN message--the Initialize (IN) messsage instructs the graphics tablet to run its self test and to return to the power-on condition.

The DF message – the Default (DF) message sets the graphics tablet to a predetermined power-on state.

Note
Refer to the Hewlett-Packard 9111A Graphics Tablet User's Manual for information about messages sent to the graphics tablet.

1 Local Cursor Control Mode. When in this mode, the tablet sends a continuous stream of x,y coordinates in the tablet's usual 8-bit, 6-byte format. The coordinates are buffered on the GPIB tablet interface pc assembly, and the stylus position is indicated by the cursor on the attached monitor. The cursor appears in the color complement of existing pixels.

A 5-byte message is sent to the host whenever the stylus on the tablet is depressed. The message format is shown in the following table. Bits 1 and 2 of byte 1 indicate the stylus position. When the stylus is depressed, the bits go high and the current stylus position is transmitted to the host.

<table>
<tr><th rowspan="2">Byte</th><th colspan="8">Bit</th></tr>
<tr><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>sp</td><td>sp</td><td>0</td></tr>
<tr><td>2</td><td>0</td><td>0</td><td>x5</td><td>x4</td><td>x3</td><td>x2</td><td>x1</td><td>x0</td></tr>
<tr><td>3</td><td>0</td><td>0</td><td>0*</td><td>0*</td><td>x9</td><td>x8</td><td>x7</td><td>x6</td></tr>
<tr><td>4</td><td>0</td><td>0</td><td>y5</td><td>y4</td><td>y3</td><td>y2</td><td>y1</td><td>y0</td></tr>
<tr><td>5</td><td>0</td><td>0</td><td>0*</td><td>0*</td><td>y9</td><td>y8</td><td>y7</td><td>y6</td></tr>
</table>
* Coordinates are those of the screen cursor, after applying offset and scaling. Transparent mode should be used if full tablet precision is required.

sp (stylus position): 1 = stylus depressed
</td></tr>
</table>

Mnemonic	Hex	Description
GRAFIN <f> (continued)	4A	2 Transparent Mode. Transparent mode allows the host to interact directly with the graphics tablet, without converting the graphics tablet data to the 97060A's 5-byte format. Full-duplex communications continues until a delimiter (default: hex 80) is received to terminate Transparent mode. This mode is useful primarily in two cases: Transparent mode may be used to run programs that were not specifically written for use with the 97060A/9111A Graphics Tablet configuration. These programs may require graphics tablet data that has not been converted to the 97060A's 5-byte format. Transparent mode may also be used to issue any of the commands described in the 9111A Graphics Tablet User's Manual, e.g., "RC;" or "RC" <LF>. **Note** When in Transparent mode, do not issue the Input Masks instruction using the Status Mask (S-mask) parameter. The S-mask parameter causes the graphics tablet to respond by activating SRQ (request service message) on the data line. The SRQ function on the data line is not supported on the GPIB tablet interface. In Transparent mode, the graphics tablet sends one 6-byte message in response to each semicolon (;) it receives from the host. In Transparent mode, all responses from the 9111A are padded to an even number of bytes. Responses that would normally have an odd byte count have a null character (00H) appended to the end. Commands sent to the tablet may be padded with as many ASCII space characters (20H) as desired. These are filtered from the character stream and not sent to the 9111A. 3 Set Offset and Scale Factors Mode. The device coordinates are subjected to an offset and scale operation in the 97060A for cursor position control. The next eight bytes specify the following in two's complement format: 1 - x offset low byte 2 - x offset high byte 3 - x multiplier fraction 4 - x multiplier integer 5 - y offset low byte 6 - y offset high byte 7 - y multiplier fraction 8 - y multiplier integer 4 Set Delimiter Mode. The next byte specifies the delimiter, replacing the default delimiter. Transmitting the delimiter during Transparent mode causes exit from Transparent mode. The delimiter can range from 0 to FE (hex); the default delimiter is 80 (hex).

<table>
<tr><th>Mnemonic</th><th>Hex</th><th>Description</th></tr>
<tr><td>GRAFIN <f>
(continued)</td><td>4A</td><td>5 Sample Position - Screen Coordinates. This instruction causes the full device status message to be sent to the host regardless of the device's status message value. (No stylus switch closure is necessary.) See the preceding table under mode 1 for the full device status message format. The x,y values are returned in 97060A (5-byte) coordinates.

6 Sample Position - Tablet Coordinates. The full tablet coordinate mesage is relayed upon receipt of this command.

7 Set Mode Register. The mode register has the following bit definitions:

<table>
<tr><th>Bit</th><th>IF = 0(default)</th><th>IF = 1</th></tr>
<tr><td>0</td><td>Wrap around</td><td>Clip to screen Boundary</td></tr>
<tr><td>1</td><td>Level Buttons</td><td>Edge Buttons</td></tr>
<tr><td>2</td><td>Button Xmit</td><td>Button not Xmit</td></tr>
<tr><td>3</td><td>Report Button Depression During GRAFIN 1</td><td>No Output During GRAFIN 1</td></tr>
</table>
These bits may be written as a group, by sending GRAFIN 7 followed by a byte with bits 0, 1, and 2 appropriately set and bit 7 = 1.

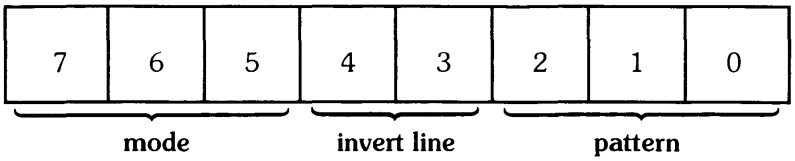
Alternately, one may set or clear an individual bit without modifying the others by setting bit 7 to a zero, bit 3 to zero or one (for clear or set, respectively) and bits 0, 1, and 2 to a pointer value (i.e., 000 for bit 0, 001 for bit 1, and 010 for bit 2).</td></tr>
<tr><td>INIT</td><td>5E</td><td>Soft Init. Receipt of this code causes the following:

Write Mask set to FF
Write Data set to 0
Set solid pattern
Set No Zoom and Pan
Turn on Read Mask for all planes
Load Character Generator with ESC
Clear line pattern counter
Clear Scratchpad RAM
Set default parameters in Scratchpad:
Font Width = 8
Font Height = 16
Auto Increment Δx = 8
Auto Increment Δy = 0
Initialize tablet, delimiter, etc.
Load Color Map with default values

The default Color Map values are most easily specified in terms of pixel value (address) for a given ratio of red, green, and blue:

pixel value = 224*R + 28*G + 3*B where R and G are chosen from the set (0,1/7,2/7,...,7/7) and B is chosen from (0,1/3,2/3,3/3)</td></tr>
<tr><td>MOVP1 <lox,hix,loy,hiy></td><td>52</td><td>Move P1 from lo x to hi x and from lo y to hi y.</td></tr>
<tr><td>MOVP2 <lox,hix,loy,hiy></td><td>53</td><td>Move P2 from lo x to hi x and from lo y to hi y.</td></tr>
</table>

<table>
<tr><th>Mnemonic</th><th>Hex</th><th>Description</th></tr>
<tr><td>PATERN <p></td><td>50</td><td>Set pattern as specified in p. Area patterns remain in effect through all drawing operations except cursor and flash fill; in these instances drawing is in solid mode, i.e., line pattern 0.

Bit
 

Bit 3 selects line pattern if a 1, area if a 0. Bit 4 selects normal mode if 0, or swaps the foreground with background if = 1.

Mode: The pattern is considered a binary function of run length (line pattern) or x,y (area pattern). If the function = 1, then this is defined as Foreground (FG). Similarly, a value of 0 is defined as Background (BG). These definitions can be interchanged via bit 4 in the Pattern argument byte.

Abbreviate the Write Data register byte as WD, and the Write Mask register byte as WM. Then the pattern mode options and mode bit values are:

<table>
<tr><th>Option</th><th>Bit Value</th><th>Meaning</th></tr>
<tr><td>FG←WD</td><td>Bit 6 = 0</td><td>write all</td></tr>
<tr><td>FG←WD*WM</td><td>Bit 6 = 1</td><td>write selected</td></tr>
<tr><td>BG←BG*WM'</td><td>Bit 7 = 1</td><td>zero selected</td></tr>
<tr><td>BG←0</td><td>Bit 7 = 0; Bit 5 = 0</td><td>zero all</td></tr>
<tr><td>BG←BG</td><td>Bit 7 = 0; Bit 5 = 1</td><td>no change</td></tr>
</table>
</td></tr>
<tr><td>PIXBLT <Δx,Δy,d></td><td>70</td><td>Copy a rectangle of pixels of width Δx and height Δy relative to P1 to a rectangle of identical size relative to P2. The direction byte is used to prevent problems with overlapped regions; one must avoid writing a pixel before it is read.

<table>
<tr><th>Direction Bit</th><th>IF = 0</th><th>IF = 1</th></tr>
<tr><td>0</td><td>normal</td><td>swap x,y axes on destination</td></tr>
<tr><td>1</td><td>increment destination y</td><td>decrement destination y</td></tr>
<tr><td>2</td><td>increment destination x</td><td>decrement destination x</td></tr>
<tr><td>3</td><td>increment source y</td><td>decrement source y</td></tr>
<tr><td>4</td><td>increment source x</td><td>decrement source x</td></tr>
</table>
</td></tr>
<tr><td>POLYC</td><td>44</td><td>Sub polygon delimiter command; used for concatenated polygons, holes, etc. Inserted after POLYS, POLYV<X0,Y0>, POLYV<X1,Y1>,... POLYV<Xk,Yk> to define a k + 1 vertex figure. The following POLYV<Xk + 1,Yk + 1>, POLYV<Xk + 2,Yk + 2>, ...POLYV<Xn,Yn>, POLYC will define another sub polygon of n-k vertices. This process may continue up to the stack limit (900 vertices).

A subsequent POLYO will cause outline drawing of the various sub polygons, without drawing any ties. A POLYF will perform a parity fill on the sub polygons (see POLYF below).</td></tr>
</table>

Mnemonic	Hex	Description
POLYF	67	Polygon Fill. The current list of sub polygons in the stack will be scan converted and filled inclusive of edges. A parity fill occurs, meaning that only those regions are filled which are reached from the screen boundary via an odd number of edge crossings.
POLYM <x,y>	45	Polygon Move. The polygon edge from the previous point to x,y is flagged so as not to be drawn during POLYO. It is in other respects treated as a normal polygon edge.
POLYO	66	Polygon Outline. Outline the individual sub polygons, except where POLYM occurs.
POLYS	56	Polygon Start. Clears polygon working area.
POLYV <x,y>	57	Polygon Vertex. Adds vertex x,y to the present sub polygon.
PPAN	5B	Set origin of display to P1. Confined to 16 pixel increments in X when no zoom.
RDCONF	5D	Read Configuration. Upon receipt, the 97060A returns two bytes. The first is an 18 hex, signifying 33 Hz and Grafin installed. The second byte specifies the microcode release level as two hex numbers. For example, the byte 33 hex means version 3.3 microcode is installed.
RDMASK <m>	4C	Read Mask. The byte m specifies which planes are to be viewed, and has no effect on readback functions such as RDR, RPIXEL, AFILL, COMPDR, or XDRAW. Overridden by blink function.
RDR	6E	Read Rectangle. The 97060A returns a stream of pixel values from the rectangle defined by P1,P2 beginning at the upper left corner and progressing left to right within top to bottom. Read is exclusive of right and bottom edges, so that the total number of pixels transferred is: ABS(P1X – P2X)*ABS(P1Y – P2Y) P1 and P2 are not modified.
RECT1	63	Outline the rectangle defined by P1,P2 diagonal. P1 and P2 are left unmodified.
RECT2	64	Fill rectangle defined by P1,P2 diagonal, inclusive of edge. P1 and P2 are left unmodified.
RLFILL <Δx>	6A	Run Length Fill. Write Δx successive pixels from P1, including P1, and leave P1 one pixel past the sequence. $0 \leq \Delta x \leq 1023$.
RMOVP1 <Δx,Δy>	54	Relative move of P1. Argument is 2s complement. $-2048 \leq \Delta x, \Delta y \leq 2047$.
RMOVP2 <Δx,Δy>	55	Relative move of P2. Argument is 2s complement. $-2048 \leq \Delta x, \Delta y \leq 2047$.
RPIXEL	6C	Read pixel at P1. A single byte is returned.
SETCOL <c>	4E	Set Color, or Write Data Register.

<table>
<tr><th>Mnemonic</th><th>Hex</th><th>Description</th></tr>
<tr><td>SETORN <d></td><td>59</td><td>Set Character Orientation. The direction byte assigns meaning to the lower three bits; these indicate character rotation and mirror inversion. Assume a relative 360-degree axis with ccw angle:
<table>
<tr><th>d</th><th>Rotation</th><th>Inversion</th></tr>
<tr><td>0</td><td>0</td><td>no</td></tr>
<tr><td>1</td><td>−90</td><td>yes</td></tr>
<tr><td>2</td><td>180</td><td>yes</td></tr>
<tr><td>3</td><td>−90</td><td>no</td></tr>
<tr><td>4</td><td>0</td><td>yes</td></tr>
<tr><td>5</td><td>90</td><td>no</td></tr>
<tr><td>6</td><td>180</td><td>no</td></tr>
<tr><td>7</td><td>90</td><td>yes</td></tr>
</table>
Transformations applied by CSPACE happen after this one.</td></tr>
<tr><td>SETCSZ <x,y></td><td>58</td><td>Set Character Size. In text mode, characters are drawn within the constraints of FSIZE, CSPACE, SETORN, and this parameter. Its effect is to zoom characters via pixel replication, and the bytes x and y specify the replication number in the x and y directions prior to rotation. 0≤x,y≤255.</td></tr>
<tr><td>SIGRD</td><td>5C</td><td>Read signature. A CRC polynomial is returned as two sorted bytes. In non-interlace mode the two bytes are identical; in interlace mode they are odd and even field signatures.</td></tr>
<tr><td>SYNCH <f></td><td>5F</td><td>Wait until f fields have occurred before accepting further commands. Useful for animation.</td></tr>
<tr><td>SZCUR <Δx,Δy></td><td>47</td><td>Set Cursor Size. The cursor is displayed either in response to the CURS command, or during GRAFIN cursor tracking mode. It is a complementing crosshair with dimensions set by Δx and Δy of this command. The cursor dimensions will be twice these values. Δx,Δy≤4095.</td></tr>
<tr><td>WPIXEL</td><td>6D</td><td>Write pixel at P1 using current color.</td></tr>
<tr><td>WRMASK <m></td><td>4F</td><td>Set Write Mask to byte value m; this determines the particular planes written for most drawing operations. It is ignored in cursor drawing and under certain pattern conditions.</td></tr>
<tr><td>WRR <b1,b2...bn></td><td>6F</td><td>Write Rectangle defined by P1 and P2, beginning in the upper left and proceeding left to right within top to bottom. Fill is exclusive of the bottom and right edges, and the number of pixels expected is the same as for RDR. P1,P2 unmodified.</td></tr>
<tr><td>XDRAW</td><td>73</td><td>Exclusive OR vector draw from P1 to P2. The pixel written is the EXOR of the previous value and the Write Data register. P1 is left at P2 afterwards.</td></tr>
<tr><td>ZOOM <z></td><td>5A</td><td>Zoom screen via pixel replication by a count of z. The position of the origin remains unchanged. P1,P2 unmodified. 0≤z≤15.</td></tr>
</table>

Chapter 3
Testing and Troubleshooting

Introduction

This chapter contains a list of the equipment required to test and troubleshoot the 97060A. It describes the self test and all LED error indications.

Required Equipment

- Multimeter
- Monitor, color graphics, HP 13279B

Self Test

The built-in self test starts on powerup. Nine LEDs on the controller board indicate the results of self test. They are labeled D5 through D13. D12 indicates Hardware Clock (HWCLK) and D13, Processor Clock (PROCCLK). If these LEDs are off, the clock circuit is faulty or -5 volts is not present. If the self test terminates without error, all nine LEDs are on and the **READY** LED on the front panel is lit.

The self test compares the signature on a displayed star pattern with the signature stored in the PROMs. If they match, the **READY** LED is lit; if not, the **READY** LED is not lit and the diagnostic LEDs indicate a Signature failure (Table 3-1). Note that some programs can still be executed after a Signature failure has occurred.

Diagnostic LED Failure Indications

Table 3-1 defines the various failures indicated by the LEDs. A lit LED is indicated by an "X". Failures are more thoroughly described in text following the tables.

LEDs D5 and D6 are not used to interpret an error. They are normally on but go off when an error occurs.

Table 3-1. Diagnostic LED Failure Indications

LEDs									Error
D5	D6	D7	D8	D9	D10	D11	D12	D13	
						X	X	X	Not Sequencing
					X		X	X	2901 Processor
					X	X	X	X	Data Bus
				X			X	X	Loop Counter
				X		X	X	X	I/O
				X	X		X	X	Scratch Pad
				X	X	X	X	X	(Undefined)
			X				X	X	Write/Read Back
			X			X	X	X	Signature
		X					X	X	RAM Row 0
		X				X	X	X	RAM Row 1
		X			X		X	X	RAM Row 2
		X			X	X	X	X	RAM Row 3
		X		X			X	X	RAM Row 4
		X		X		X	X	X	RAM Row 5
		X		X	X		X	X	RAM Row 6
		X		X	X	X	X	X	RAM Row 7
		X	X				X	X	RAM Row 8
		X	X			X	X	X	RAM Row 9
		X	X		X		X	X	RAM Row A
		X	X		X	X	X	X	RAM Row B
		X	X	X			X	X	RAM Row C
		X	X	X		X	X	X	RAM Row D
		X	X	X	X		X	X	RAM Row E
		X	X	X	X	X	X	X	RAM Row F

Not Sequencing

The sequencer (U24, U55, U56) is faulty.

2901 Processor

The 2901 processor (U21, U22, U23) is faulty.

Data Bus

The self test counts up the data bus. This error is indicated if two data lines are shorted together or shorted to ground or +5 volts, or if two devices are driving the data bus at the same time.

Loop Counter

The self test counts down the loop counter.

I/O

The microcode loops, sending 0s and 1s to the parallel interface pc assembly and reading them back.

Scratch Pad

Scratch pad test loops passing address to data and then writes. Then, address 1 contains data 1, address 2 contains data 2, etc. It then reads back. If an error occurs, the test stops. If there is no error, the data is complemented, written, and checked.

Write/Read Back

The test writes to memory and reads it back through the read back shift registers. If they don't match, an error is indicated. Possible causes of this error are outputs of two RAMs shorted together, RAS or CAS bad, or shift register bad.

Signature

This part of the self test displays the star pattern and checks it against the signature in PROM. If there's not a match, an error is indicated. Possible problems are bad RAM or bank of RAMs, signature hardware bad, color map bad, or pan and zoom bad. The error is usually evident on the display.

RAM

If LED D7 is lit, there is a RAM error. The combination of LEDs D8 through D11 indicate the row in which the error occurred. The address lines on a scratch pad RAM indicate which bank of RAMs is failing.

Table 3-2 is a matrix which indicates the specific failing RAM. To find the failing RAM, determine the row according to LEDs D7 through D11 and determine the bank according to the high scratch pad address line as indicated by the U341 pins. For example, if LEDs D7, D9, and D11 are lit, and U341 pin 4 is high, U103 is the failing RAM. If more than one scratch pad address line is high, the problem is probably with the control lines, such as the address lines, write, enable, RAS, or CAS.

Table 3-2. Failed RAM Locater

LEDs					ROW	SCRATCH PAD ADDRESS*							
D7	D8	D9	D10	D11		A0	A1	A2	A3	A4	A5	A6	A7
X					0	U18,	49,	77	108	140	172	192	224
X				X	1	U17,	48,	76	107	139	171	191	223
X			X		2	U16,	47,	75	106	138	170	190	222
X			X	X	3	U15,	46,	74	105	137	169	189	221
X		X			4	U14,	45,	73	104	136	168	188	220
X		X		X	5	U13,	44,	72	103	135	167	187	219
X		X	X		6	U12,	43,	71	102	134	166	186	218
X		X	X	X	7	U11,	42,	70	101	133	165	185	217
X	X				8	U10,	41,	69	100	132	164	184	216
X	X			X	9	U9,	40,	68,	99	131	163	183	215
X	X		X		A	U8,	39,	67,	98	130	162	182	214
X	X		X	X	B	U7,	38,	66,	97	129	161	181	213
X	X	X			C	U6,	37,	65,	96	128	160	180	212
X	X	X		X	D	U5,	36,	64,	95	127	159	179	211
X	X	X	X		E	U4,	35,	63,	94	126	158	178	210
X	X	X	X	X	F	U3,	34,	62,	93	125	157	177	209

* High scratch pad address line is determined as follows:
A0 - U341 pin 5 high
A1 - U341 pin 6 high
A2 - U341 pin 7 high
A3 - U341 pin 4 high
A4 - U341 pin 3 high
A5 - U341 pin 2 high
A6 - U341 pin 1 high
A7 - U341 pin 17 high

Troubleshooting Hints

The parallel interface pc assembly must be connected to the GPIO interconnect assembly for the 97060A to execute self test. If the GPIO host interface cables are not properly connected, the controller pc assembly hangs at an I/O error.

J3 is the 16-bit DMA into the 97060A, and J4 is the 16-bit DMA to the GPIO.

If LEDs D9 and D11 are on, indicating an I/O problem, and all others except clock LEDs D12 and D13 are off, check the following in the order indicated:

- Parallel interface pc assembly not plugged in
- GPIO host interface cables not connected
- Parallel interface pc assembly bad
- Controller pc assembly bad

During self test the 2901 processor writes a byte of 0s and then a byte of 1s to the parallel interface pc assembly, and then reads them back. If the handshake or data readback is bad, the 97060A hangs at I/O error.

If self test passes, but the op codes don't function correctly, the input section from the parallel interface pc assembly is suspect.

Chapter 4
Assembly Access

Introduction

This chapter describes how to access all the replaceable 97060A assemblies. The table of contents of this manual lists the replaceable assemblies and the corresponding page numbers in this chapter where the access procedures are located. Read this introduction carefully before performing assembly access.

The procedures help you to disassemble the 97060A in order to access the assemblies. Reassembly procedures are the reverse of disassembly procedures. Special instructions required for reassembly are clearly noted.

This chapter is organized in several sections, as follows:

- General Safety Procedure
- Electrostatic Discharge
- Covers
- Replaceable Assemblies

The Covers subsection describes how to remove the top and bottom covers. The Replaceable Assemblies subsection describes how to access and replace assemblies.

The following tools are required to disassemble the 97060A:

- #1 Pozidriv screwdriver
- Flat-blade screwdriver
- 1/4-inch nutdriver
- 3/8-inch nutdriver or wrench
- 5/16-inch wrench
- Portable conductive antistatic kit, PN 9300-0933

CAUTION

THE 97060A HAS ASSEMBLIES AND COMPONENTS SENSITIVE TO ELECTROSTATIC DISCHARGE. READ THE FOLLOWING SECTION AND OBSERVE THE PROCEDURES TO AVOID DAMAGING THE 97060A AND ITS PARTS.

Electrostatic Discharge

Electrostatic discharge (ESD) causes failure in many PC assemblies, other assemblies, and components. Static electricity doesn't appear to be dangerous because much of the ESD that can cause component or assembly failure is too small to be felt. Humans can sense ESD of 3500-5000V. However, a discharge of 300V is enough to destroy some components.

Assemblies and equipment containing ESD-sensitive parts are often as sensitive as the most sensitive part they contain. Protective circuitry in these assemblies and equipment provides varying degrees of protection from ESD applied to their terminals. Such assemblies and equipment, however, are still vulnerable to induced ESD caused by strong electrostatic fields or by contact of electrical connections or paths with a charged object.

Static damage is not always catastrophic. Sometimes a part slowly degrades, resulting in deteriorating performance. For example, internal resistance changes cause speed or voltage changes. Results include intermittent or latchup problems (for example, a line printer prints bad data).

When disassembling the 97060A, a portable conductive field service antistatic kit should be used to eliminate ESD when handling or temporarily setting aside ESD-sensitive parts. The kit contains a wrist strap, antistatic mat, and ground cable.

Carefully observe the following procedures when disassembling the 97060A:

- Components, PC assemblies, and other assemblies and equipment should always be stored, transported, and shipped in antistatic or conductive containers.
- ESD-sensitive items must never be handled by ungrounded personnel, nor should they ever be stored on nonconductive surfaces or near nonconductive materials.
- Field support should keep all replacement PC assemblies and components in antistatic or conductive bags. The failed board should be placed in a static-free bag for return to manufacturing site.
- Removal of ESD-sensitive devices from an assembly must be done at a static-safe work station using all precautions. Suspect or rejected components, PC boards, and subassemblies are to be treated with the same care as good devices. Otherwise, further damage may result which prevents tracing the cause of the original failure.

  Before removing devices from protective container:

  a. Clear work area of static hazards such as plastic cups, bags, envelopes, and papers.
  b. Connect wrist strap.
  c. Neutralize charges of ESD protective packaging containing an ESD-sensitive item and of tools by placing the packaged item on an ESD-grounded work bench surface to remove any charge prior to opening the packaging material. Alternately, charges can be removed by grounded personnel touching the package.
  d. Ensure that the 97060A is properly grounded before inserting ESD-sensitive items.
  e. Remove ESD-sensitive item from ESD protective packaging using finger or metal grasping tool only after grounding, and then place on the ESD-grounded work bench surface.

- Place PC boards and components on table mat when not in static-shielding bags or other protective containers.
- Clothing must never contact ESD-sensitive parts. Wrist strap does not bleed off charges from clothing.
- Personnel handling ESD-sensitive items should avoid physical activities which are static producing in the vicinity of those items. Such activities include wiping feet and removing or putting on jackets or sweaters.
- Where ground straps cannot be used, personnel should ground themselves prior to removing ESD-sensitive items from their protective packaging.
- Tools and test equipment used in ESD-protective areas should be properly grounded; hand tools should not contain insulation on the handles or, if used, tools with insulated handles should be treated with a topical antistat.
- Ensure that all containers, tools, test equipment, and fixtures used in ESD-protective areas are grounded before and during use either directly or by contacting with a grounded surface. Grounding of electrical test equipment should be via a grounded plug, not through the conductive surface of the ESD-grounded work station.
- Do not assume that insulators are fully discharged when placed on a conductive work surface. Once the insulator is lifted off the surface, it retains its charge.
- All PC boards are to be handled only by grounded personnel. If possible, they should be held only by the ejectors. If necessary, they can be handled by the side edges.

Covers

WARNING

TURN POWER SWITCH OFF AND UNPLUG POWER CORD FROM AC OUTLET BEFORE REMOVING ANY ASSEMBLY.

The top and/or bottom covers must be removed to provide access to replacable assemblies. Follow the procedures and CAUTIONS carefully to avoid damaging covers.

CAUTION

THE COVERS AND CHASSIS HAVE METAL GASKETING WHICH CAN BE DAMAGED BY MISHANDLING. PERFORM THE FOLLOWING PROCEDURES CAREFULLY.

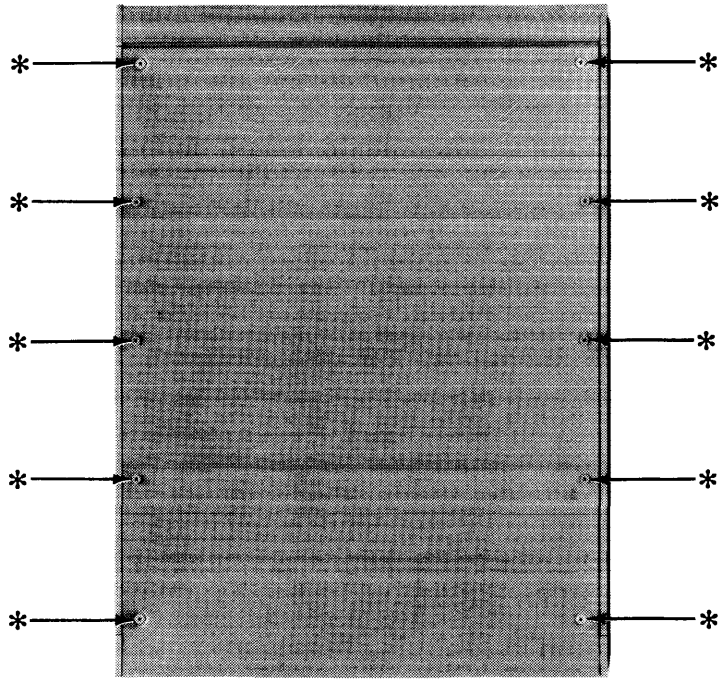
Top Cover

1. Turn off the **POWER** switch and unplug power cable from ac outlet.
2. Remove the 10 #1 Pozidriv screws and washers that attach top cover to chassis (Figure 4-1).
3. Lift cover slightly at the back and slowly pull cover away from the chassis, ensuring that the RFI gasketing does not bind.

REASSEMBLY CAUTION

WHEN REPLACING TOP COVER, HOLD COVER AT A SLIGHT ANGLE AND INSERT COVER FLANGE INTO CHASSIS SLOT. THEN LOWER COVER INTO PLACE. THIS PREVENTS DAMAGE TO RFI GASKETING FROM SIDEWAYS MOTION OF COVER AND CHASSIS.

FROM OUTSIDE OF FRONT PANEL, VISUALLY CHECK RFI GASKETING FOR PROPER SEATING BEFORE TIGHTENING COVER SCREWS.



* #1 POZIDRIV SCREW
SCREW 038-01507-00MET
WASHER 039-00367-00MET

FOUR #8 TINNERMAN CLIPS INSIDE COVER

Figure 4-1. Top Cover

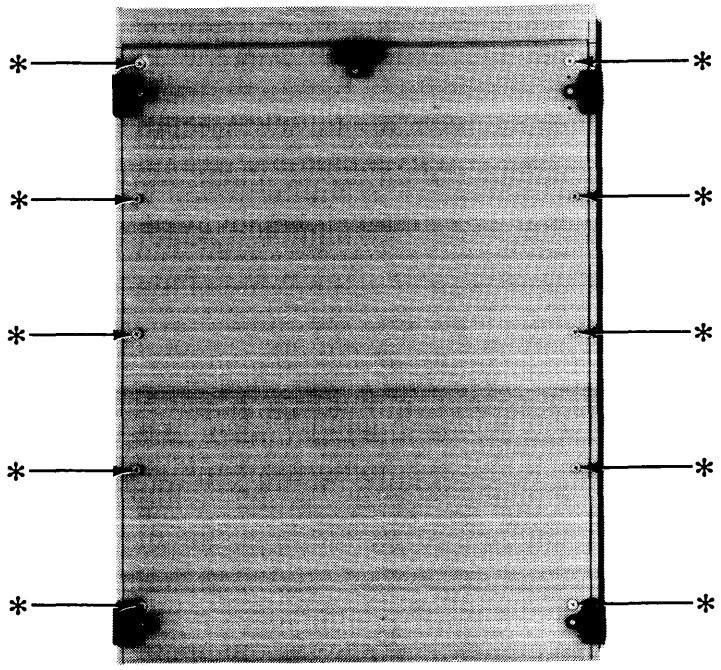
Bottom Cover

1. Turn off the **POWER** switch and unplug power cable from ac outlet. Disconnect power cable and interface cables from 97060A.
2. Place 97060A on its top. Be careful to avoid damaging the top.
3. Remove the 10 #1 Pozidriv screws and washers that attach bottom cover to chassis (Figure 4-2).
4. Lift cover slightly at the back and slowly pull cover away from the chassis, ensuring that the RFI gasketing does not bind.

REASSEMBLY CAUTION

WHEN REPLACING BOTTOM COVER, HOLD COVER AT A SLIGHT ANGLE AND INSERT COVER FLANGE INTO CHASSIS SLOT. THEN LOWER COVER INTO PLACE. THIS PREVENTS DAMAGE TO RFI GASKETING FROM SIDEWAYS MOTION OF COVER AND CHASSIS.

FROM OUTSIDE OF FRONT PANEL, VISUALLY CHECK RFI GASKETING FOR PROPER SEATING BEFORE TIGHTENING COVER SCREWS.



* #1 POZIDRIV SCREW
SCREW 038-01507-00MET
WASHER 039-00367-00MET

FOUR #8 TINNERMAN CLIPS INSIDE COVER

Figure 4-2. Bottom Cover

Replaceable Assemblies

The following procedures describe the removal of replaceable assemblies. The reassembly procedures are the reverse of the removal procedures. If specific procedures are required for reassembly they are provided.

A list of the assemblies that have replacement procedures in this chapter follows:

- Parallel Interface Pc Assembly
- GPIB Tablet Interface Pc Assembly
- Controller Pc Assembly
- Power Supply, −5V, 10A
- Power Supply, +5V, 20A
- Fan

Chapter 5 lists all replaceable parts and part numbers. Photographs identify replaceable parts.

Parallel Interface Pc Assembly

1. Prerequisite removal:
   - Top Cover
2. Disconnect both GPIO host interface cables from the parallel interface pc assembly (Figure 4-3).
3. Remove the four slotted screws and washers from the parallel interface pc assembly (Figure 4-3).

CAUTION

USE CARE WHEN REMOVING THE PARALLEL INTERFACE PC ASSEMBLY TO AVOID DAMAGING THE CONNECTORS WHICH INTERCONNECT IT WITH THE GPIB TABLET INTERFACE PC ASSEMBLY.

4. Lift the parallel interface pc assembly from the GPIB tablet interface pc assembly.

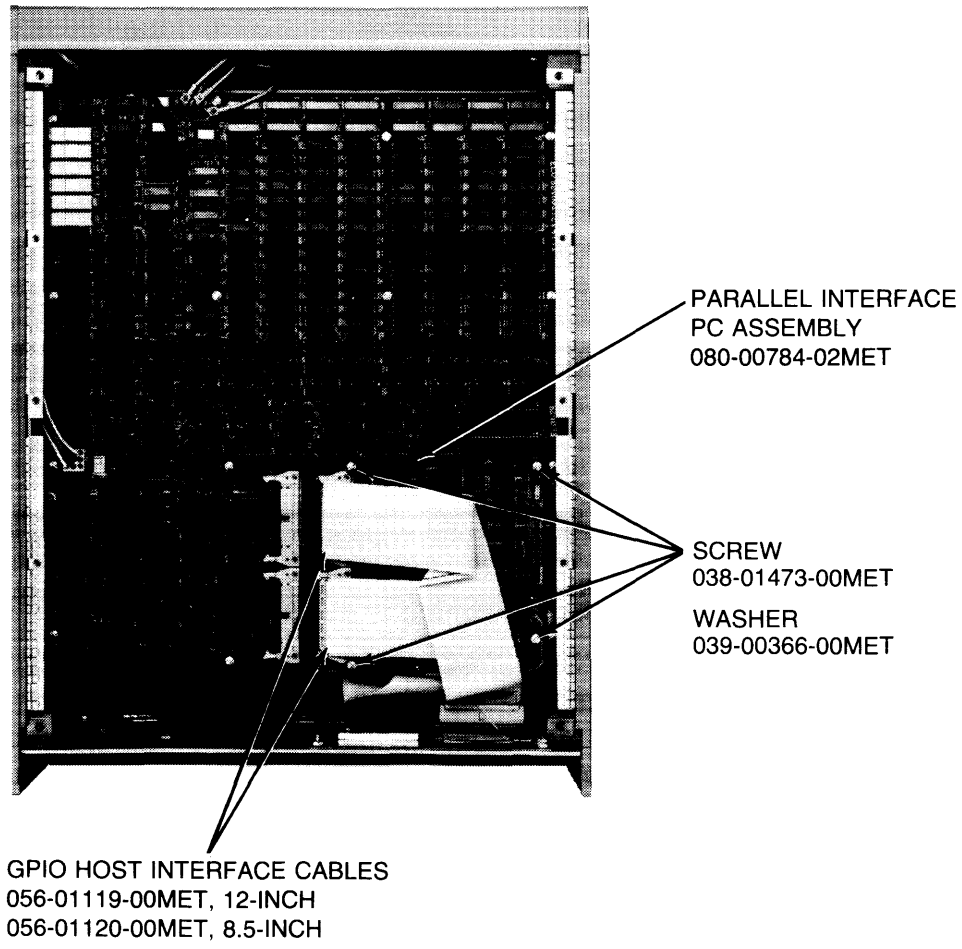


Figure 4-3. Parallel Interface Pc Assembly

GPIB Tablet Interface Pc Assembly

1. Prerequisite removals:
   - Top Cover
   - Parallel Interface Pc Assembly
2. Disconnect the GPIB cable from the GPIB tablet interface pc assembly (Figure 4-4).
3. Remove the four slotted screws and washers from the GPIB tablet interface pc assembly (Figure 4-4).

CAUTION

USE CARE WHEN REMOVING THE GPIB TABLET INTERFACE PC ASSEMBLY TO AVOID DAMAGING THE CONNECTORS WHICH INTERCONNECT IT WITH THE CONTROLLER PC ASSEMBLY.

4. Lift the GPIB tablet interface pc assembly from the controller pc assembly.

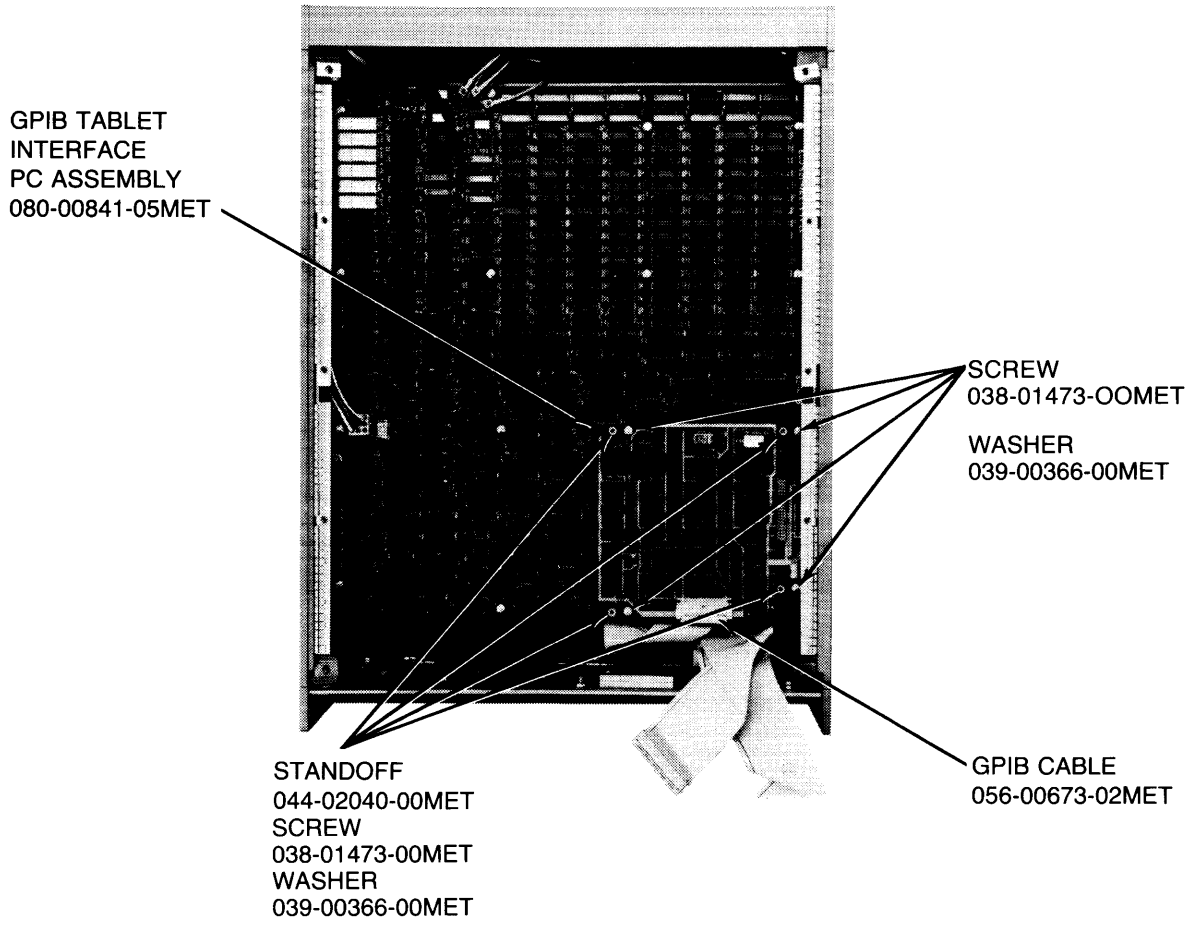


Figure 4-4. GPIB Tablet Interface Pc Assembly

Controller Pc Assembly

1. Prerequisite removals:
   - Top Cover
   - Parallel Interface Pc Assembly
   - GPIB Tablet Interface Pc Assembly

CAUTION

RECORD ALL CABLE POSITIONS BEFORE DISCONNECTING CABLES FROM ASSEMBLY. NOTE ESPECIALLY THE R, G, AND B VIDEO CABLES AND THE POSITION OF THE LED CABLE CONNECTOR.

2. Remove the power cable, LED cable, and the three video cables from the controller pc assembly (Figure 4-5).
3. Remove the four hex standoffs and washers from the controller pc assembly (Figure 4-5).
4. Remove the 12 slotted screws and washers from the controller pc assembly (Figure 4-5).
5. Bend cables out of the way and remove controller pc assembly from chassis.

REASSEMBLY CAUTION

WHEN REPLACING CONTROLLER PC ASSEMBLY, ENSURE THAT ALL 16 STANDOFF SLEEVES ARE IN PLACE OVER THE STANDOFFS. A MISSING SLEEVE COULD RESULT IN DAMAGE TO THE PC ASSEMBLY.

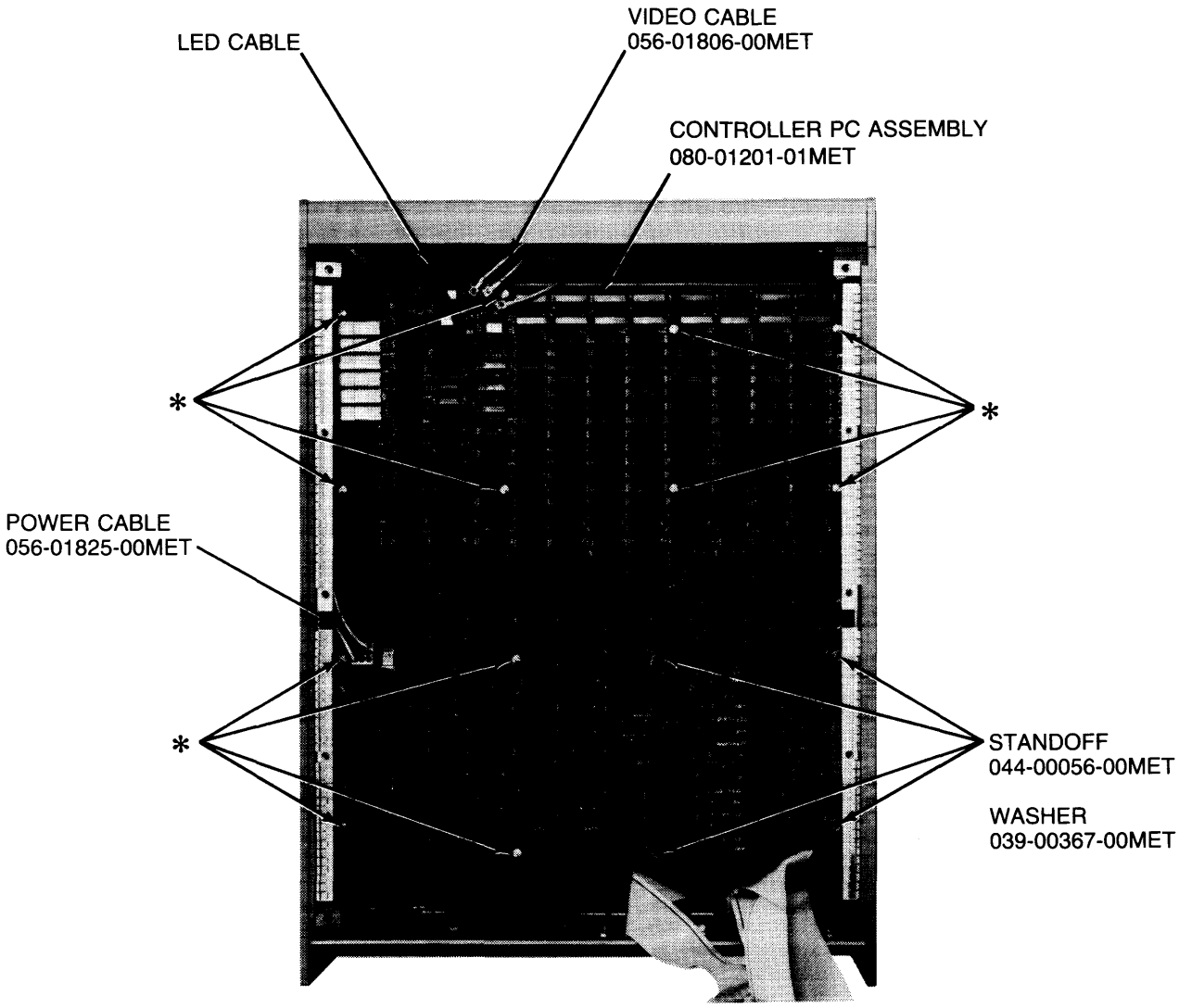


Figure 4-5. Controller Pc Assembly

Power Supply, −5V, 10A

1. Prerequisite removal:
   - Bottom Cover
2. Disconnect connectors P1 and P2 and ground wire from supply (Figure 4-6).
3. Remove the two slotted screws from the side bracket (Figure 4-6).
4. Loosen the two 5/16-inch hex nuts opposite the removed screws to enable easy removal and replacement of the power supply (Figure 4-6).
5. Lift power supply by tabs and remove from chassis (Figure 4-6).

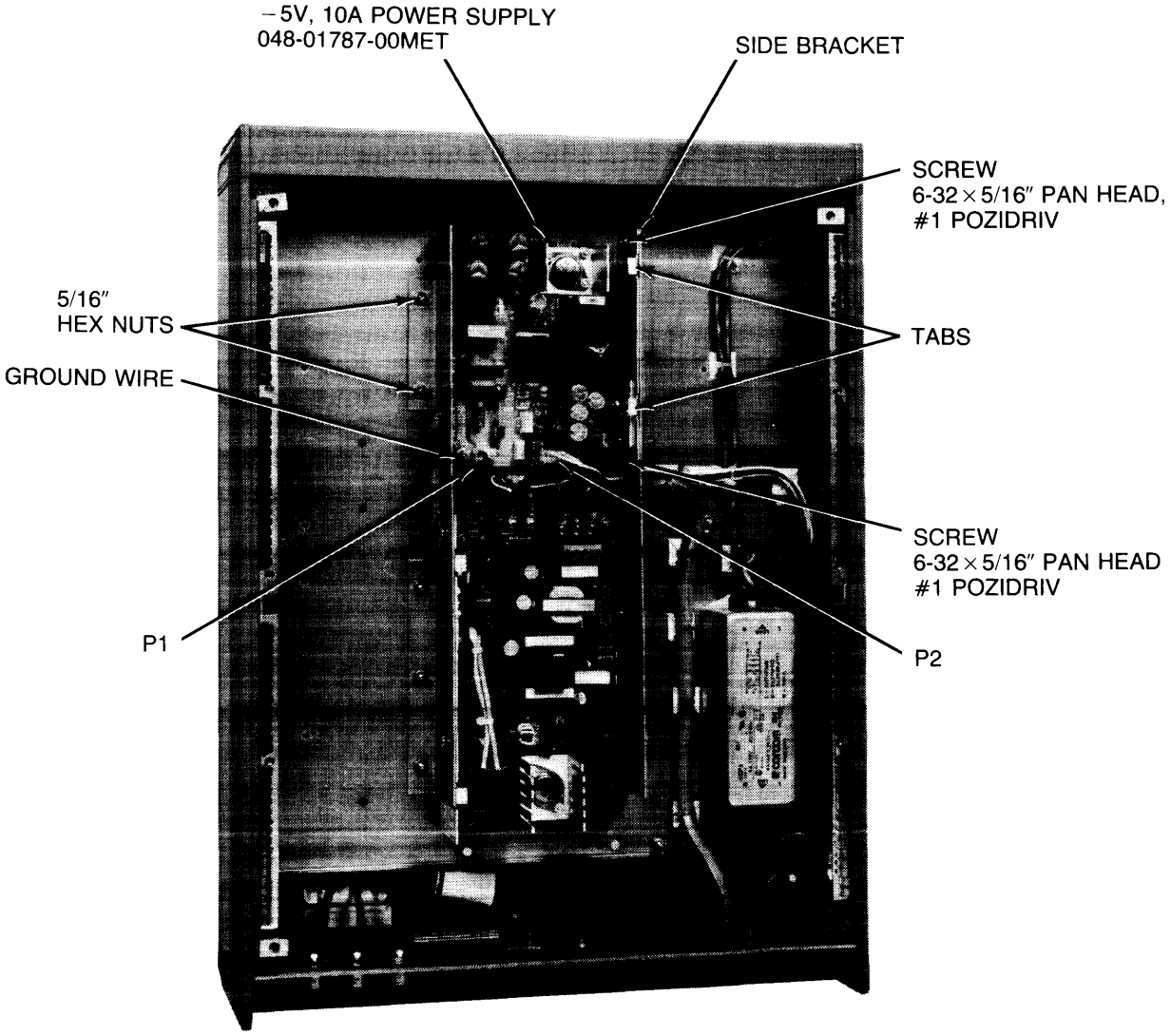


Figure 4-6. −5V, 10A Power Supply

Power Supply, +5V, 20A

1. Prerequisite removal:
   - Bottom Cover

CAUTION

TAG ALL WIRES AS YOU DISCONNECT THEM SO YOU CAN RECONNECT WIRES TO THE CORRECT TERMINALS.

2. Disconnect +OUT and -OUT wires and six wires from TB1 (Figure 4-7).
3. Remove the two slotted screws, washers, and 5/16-inch hex nuts from the side bracket (Figure 4-7).
4. Loosen the two 5/16-inch hex nuts opposite the removed screws to enable easy removal and replacement of the power supply (Figure 4-7).
5. Lift power supply by tabs and remove from chassis (Figure 4-7).

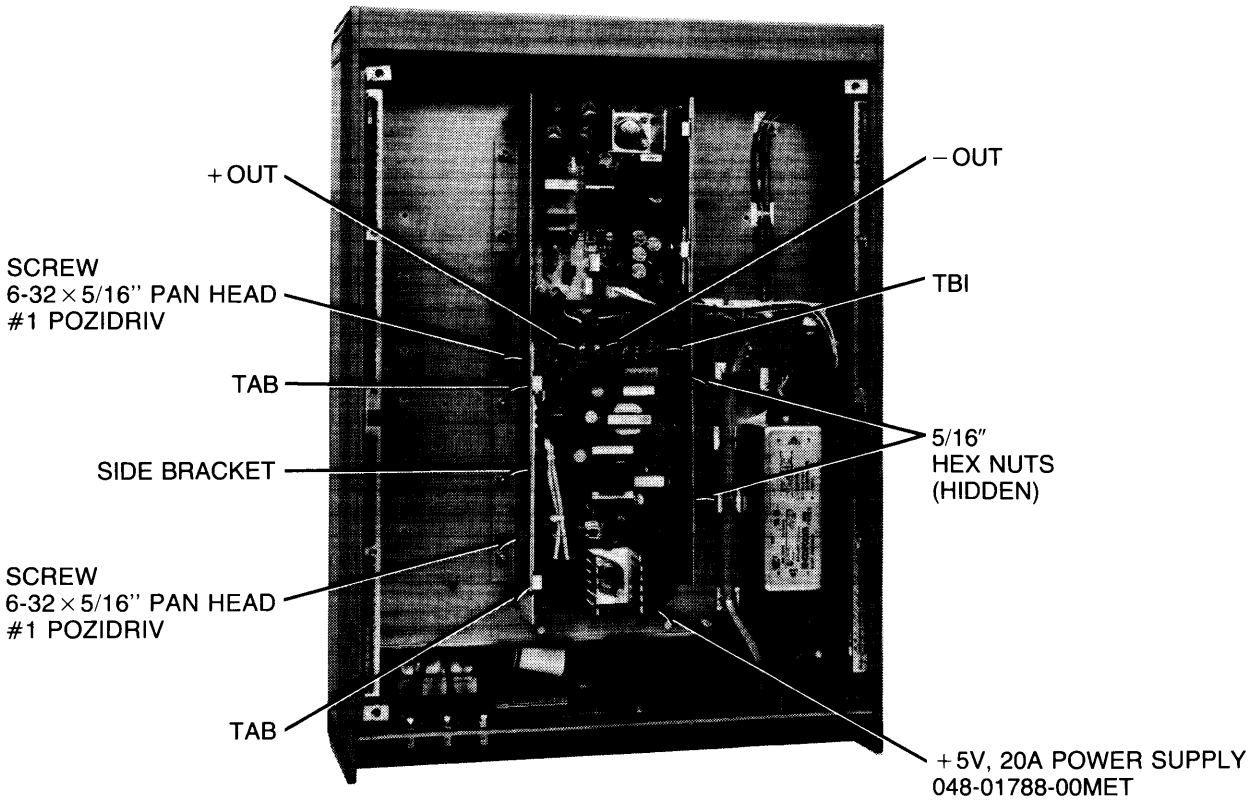


Figure 4-7. +5V, 20A Power Supply

Fan

1. Prerequisite removals:
   - Top Cover
   - Bottom Cover
2. Disconnect the power cable from the fan.
3. Remove the three 5/16-inch nuts that connect the fan to the chassis and remove the fan.

Chapter 5
Replaceable Parts

Introduction

This chapter lists and locates all of the replaceable parts in the 97060A and provides information required to order replacement parts. All parts listed can be ordered from the Corporate Parts Centers except for the Controller Pc Assembly, an exchange assembly which is ordered from the Computer Support Division.

Figures 5-1 and 5-2 identify most replaceable parts.

Exchange Part

The Controller Pc Assembly is the only part on the Computer Support Division (CSD) exchange program. When it fails, it should be returned to CSD for repair, and a rebuilt part should be obtained. Table 5-1 provides the part number.

Table 5-1. Exchange Part

Part Number	Description
97060-69500	Controller Pc Assembly

Non-Exchange Parts

Table 5-2 lists the non-exchange parts.

Table 5-2. Non-Exchange Parts

Part Number	Description
038-01507-00MET	Screw, 6-32 X 3/4" flat head, #1 Pozidriv
039-00367-00MET	Washer, #6 nylon, 0.03"
038-01473-00MET	Screw, 6-32 X 5/16" pan head, slotted
039-00366-00MET	Washer, #6 nylon, 0.06"
044-02040-00MET	Standoff, 6-32 X 1/2", female/female
044-00056-00MET	Standoff, 6-32 X 1/2", male/female
044-01745-00MET	Sleeve, standoff
033-00158-00MET	Jumper, 2-pin
084-01918-00MET	Jumper, 10A power supply configuration
084-01917-00MET	Jumper, 20A power supply configuration
048-01787-00MET	Power supply, −5V, 10A
048-01788-00MET	Power supply, +5V, 20A
045-00347-00MET	Switch, ac power, DPST, with cable
056-01825-00MET	Power cable
056-01806-00MET	Video cable, 26"
056-00512-00MET	Coax cable
026-00417-00MET	LED, red, ON
026-00418-00MET	LED, green, READY
085-01189-00MET	Front panel
085-01190-00MET	Rear panel, 110V
085-01824-00MET	Rear panel, 220V
080-00841-05MET	GPIB tablet interface pc assembly
056-00673-02MET	GPIB cable
080-00784-02MET	Parallel interface pc assembly
056-01119-00MET	GPIO host interface cable, 12-inch
056-01120-00MET	GPIO host interface cable, 8.5-inch
080-01129-01MET	GPIO interconnect assembly
042-01198-00MET	Line filter
050-00342-00MET	Fan, 110V
050-00694-00MET	Fan, 220V
023-01387-00MET	Area pattern PROM, U148
023-00916-01MET	Line pattern PROM, U149
023-00914-00MET	Character set PROM, U150
078-01200-00MET	Microcode kit PROM, U83-U90
0363-0170	RFI gasketing, strip fingers, 16 inches
2110-0715	Fuse, line, 6.3A, 220V
2110-0055	Fuse, line, 4A, 110V
2110-0003	Fuse, power supply, 3A
2110-0010	Fuse, power supply, 5A
8120-1351	Power cord, Great Britain
8120-1369	Power cord, Australia
8120-1689	Power cord, Europe
8120-1378	Power cord, U.S.A., 110V
8120-0698	Power cord, U.S.A., 220V
8120-2104	Power cord, Switzerland
8120-2956	Power cord, Denmark
8120-4211	Power cord, South Africa

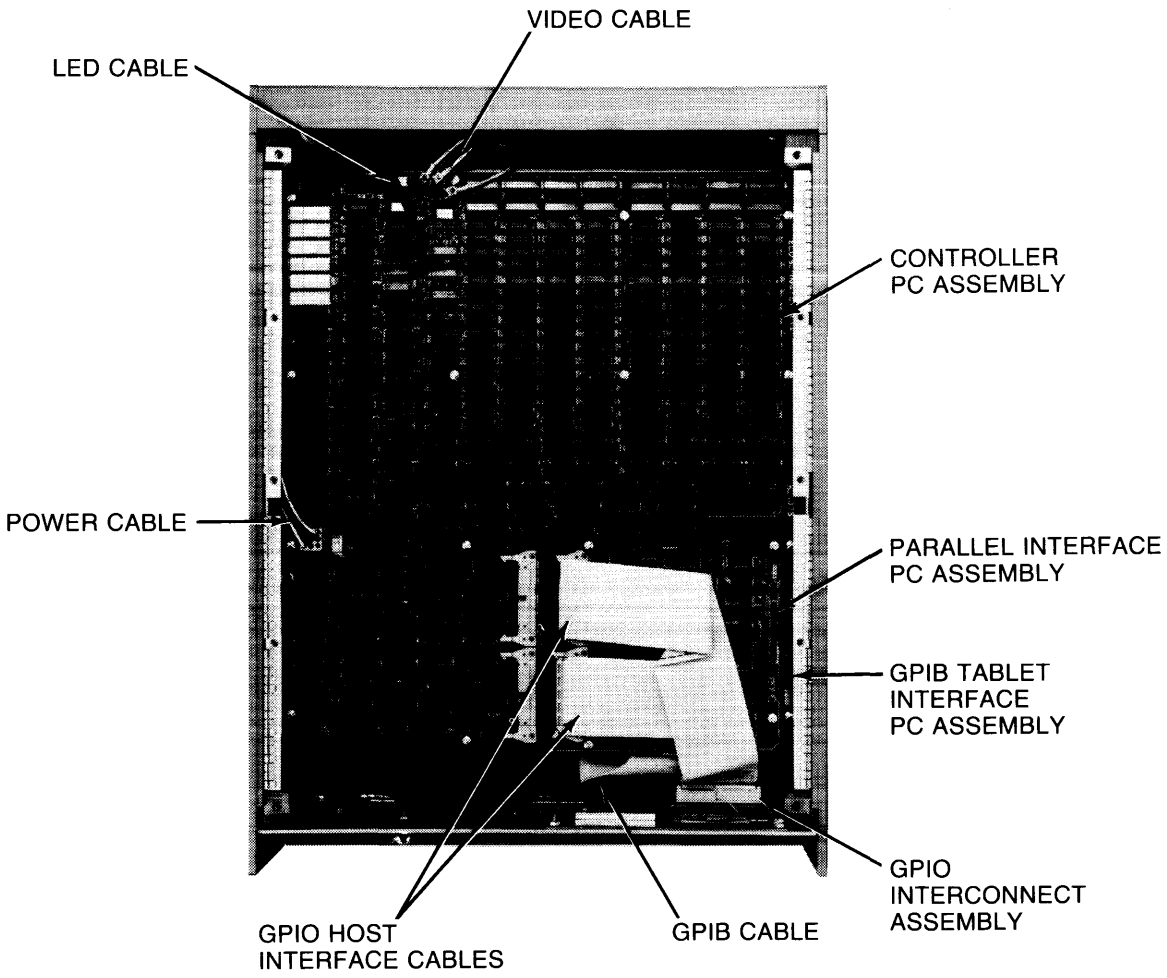


Figure 5-1. Replaceable Parts, Top View

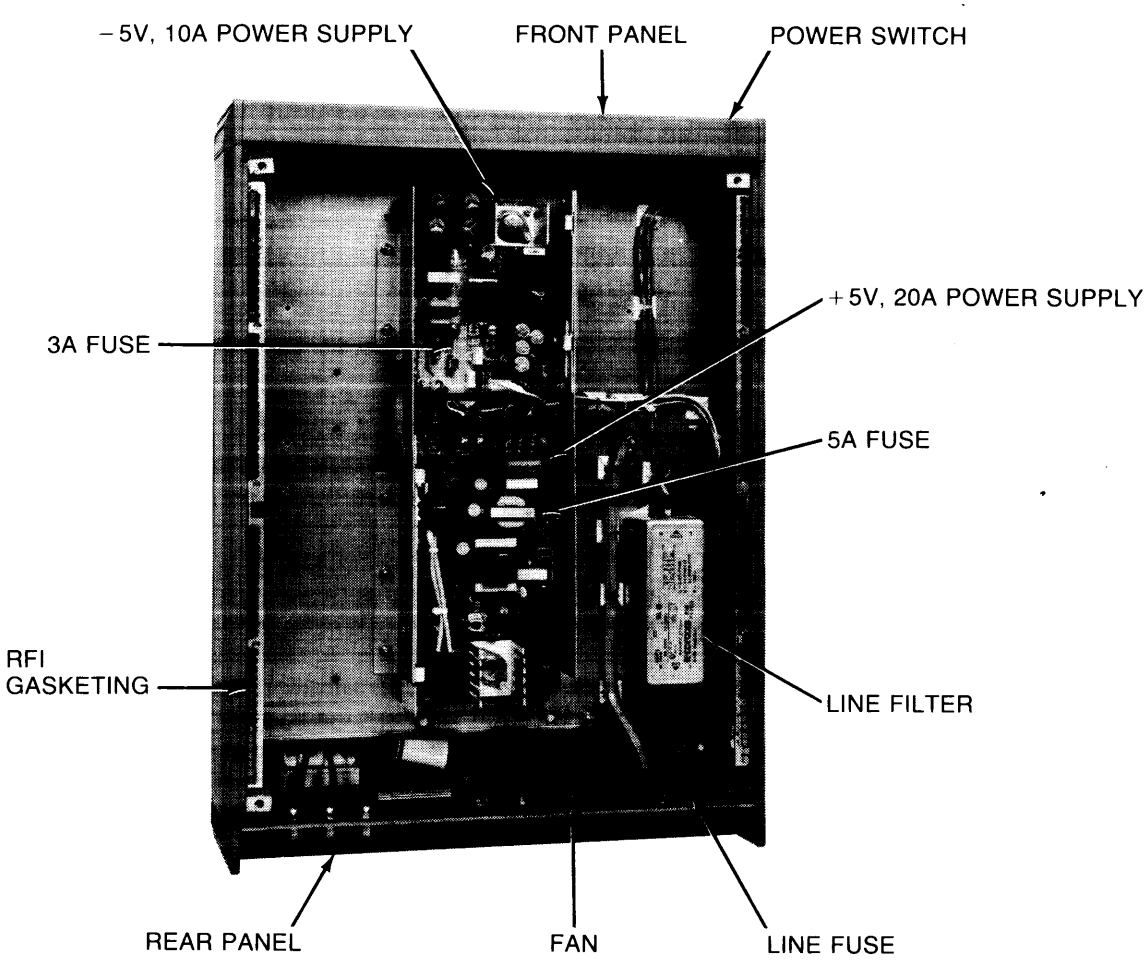


Figure 5-2. Replaceable Parts, Bottom View

Part No. 97060-90030
E 0884
Microfiche No. 97060-99030

Printed in U.S.A.
First Edition with update
August 1984