64000

HP64000 Logic Development System

Model 64161A/162A/163A Emulation Memory

HEWLETT PACKARD

CERTIFICATION

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

WARRANTY

This Hewlett-Packard system product is warranted against defects in materials and workmanship for a period of 90 days from date of installation. During the warranty period, HP will, at its options, either repair or replace products which prove to be defective.

Warranty service of this product will be performed at Buyer's facility at no charge within HP service travel areas. Outside HP service travel areas, warranty service will be performed at Buyer's facility only upon HP's prior agreement and Buyer shall pay HP's round trip travel expenses. In all other cases, products must be returned to a service facility designated by HP.

For products returned to HP for warranty service. Buyer shall prepay shipping charges to HP and HP shall pay shipping charges to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to HP from another country.

HP warrants that its software and firmware designated by HP for use with an instrument will execute its programming instructions when properly installed on that instrument. HP does not warrant that the operation of the instrument, or software, or firmware will be uninterrupted or error free.

LIMITATION OF WARRANTY

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside of the environmental specifications for the product, or improper site preparation or maintenance.

NO OTHER WARRANTY IS EXPRESSED OR IMPLIED. HP SPECIFICALLY DISCLAIMS THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

EXCLUSIVE REMEDIES

THE REMEDIES PROVIDED HEREIN ARE BUYER'S SOLE AND EXCLUSIVE REMEDIES. HP SHALL NOT BE LIABLE FOR ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, WHETHER BASED ON CONTRACT, TORT, OR ANY OTHER LEGAL THEORY.

ASSISTANCE

Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products.

For any assistance, contact your nearest Hewlett-Packard Sales and Service Office. Addresses are provided at the back of this manual.

CW&A 2/81

SERVICE MANUAL

MODEL 64161A/162A/163A

EMULATION MEMORY

REPAIR NUMBERS

This manual applies to Model 64161A all repair number prefixes. For more information on repair numbers refer to "Instruments Covered by This Manual" in Section I.

Manual Part No. 64161-90901
Microfiche Part No. 64161-90801

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SAFETY SUMMARY

The following general safety precautions must be observed during all phases of operation, service, and repair of this instrument. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the instrument. Hewlett-Packard Company assumes no liability for the customer's failure to comply with these requirements.

GROUND THE INSTRUMENT.

To minimize shock hazard, the instrument chassis and cabinet must be connected to an electrical ground. The instrument is equipped with a three-conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE.

Do not operate the instrument in the presence of flammable gases or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS.

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE.

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT SUBSTITUTE PARTS OR MODIFY INSTRUMENT.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification of the instrument. Return the instrument to a Hewlett-Packard Sales and Service Office for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

Dangerous voltages, capable of causing death, are present in this instrument. Use extreme caution when handling, testing, and adjusting.

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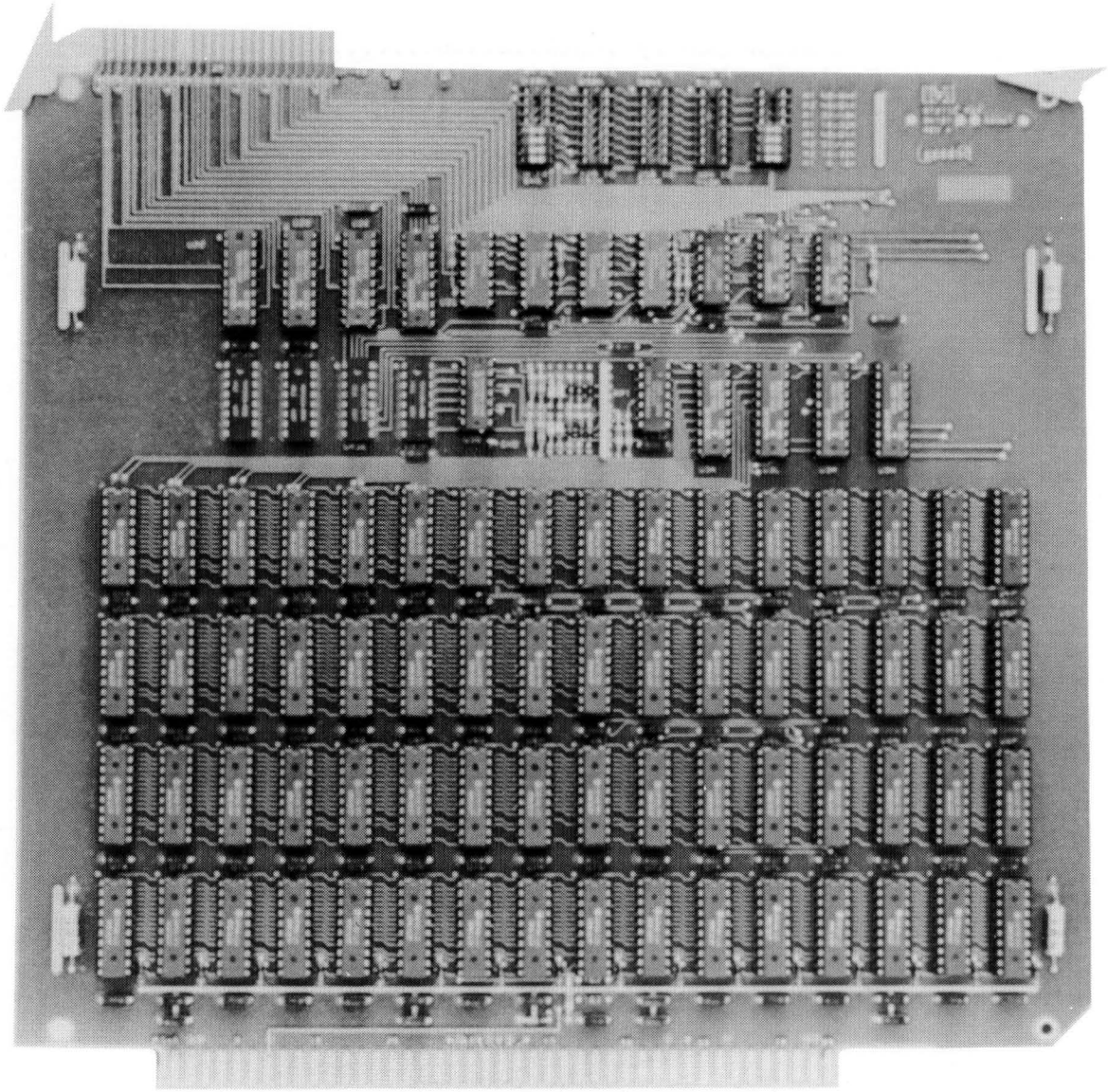


Figure 1-1. Model 64161A/162A/163A Emulation Memory

SECTION I

GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. This Service Manual contains information required to install, test and service the Hewlett-Packard Model 64161A/162A/163A Emulator Memory.

1-3. Shown on the title page is a microfiche part number. This number can be used to order a 4 X 6-inch microfilm transparency of the manual. Each microfiche contains up to 96 photoduplicates of the manual pages.

1-4. INSTRUMENTS COVERED BY THIS MANUAL.

1-5. Attached to the instrument or printed on the printed circuit board is the repair number. The repair number is in the form: 0000A0000. It is in two parts; the first four digits and the letter are the repair prefix, and the last five are the suffix. The prefix is the same for all identical instruments. The suffix, however, is assigned sequentially and is different for each instrument. The contents of this manual apply to instruments with the repair number prefix(es) listed under REPAIR NUMBERS on the title page.

1-6. An instrument manufactured after the printing of this manual may have a repair number prefix that is not listed on the title page. This unlisted repair number prefix indicates that the instrument is different from those described in this manual. The manual for this newer instrument is accompanied by a Manual Changes Supplement. The supplement contains "change information" that explains how to adapt the manual for the newer instrument.

1-7. In addition to change information, the supplement contains information for correcting errors in the manual. To keep this manual as current as possible, Hewlett-Packard recommends that you periodically request the latest Manual Changes Supplement. The supplement for this manual is identified with the manual print date and part number, both of which appear on the manual title page. Complimentary copies of the supplement are available from Hewlett-Packard.

1-8. For information concerning a repair number prefix that is not listed on the title page or in the Manual Changes Supplement, call your nearest Hewlett-Packard office.

1-9. DESCRIPTION.

1-10. The 64000 microprocessor emulation systems, illustrated in Figure 1-2, allow software designers to develop and debug software modules for specific microprocessors. The emulation plug replaces the microprocessor physically in the target system permitting hardware in the emulation system to simulate the functions of the target microprocessor while driving target system hardware with the software being developed.

1-11. The emulation memory can be used to duplicate the target system memory. Address space can be allocated to target system RAM, target system ROM, emulation RAM, and emulation ROM, and illegal address space.

1-12. Models 64161A, 64162A, and 64163A Emulation Memory provide the possibility of up to 128K bytes of memory on one card. The three models differ from each other in the number of memory chips loaded on each board. The Model 64163A, 32k byte memory, has one 16-chip row of 16K x 1 static RAM chips loaded; Model 64162A, 64k byte memory, has two rows of chips loaded and the Model 64161A, 128k byte memory has four rows of chips.

1-13. The 64161A, 64162A and 64163A feature fast access time, low-power standby and operation modes, and the ability to access bytes as well as 16-bit words.

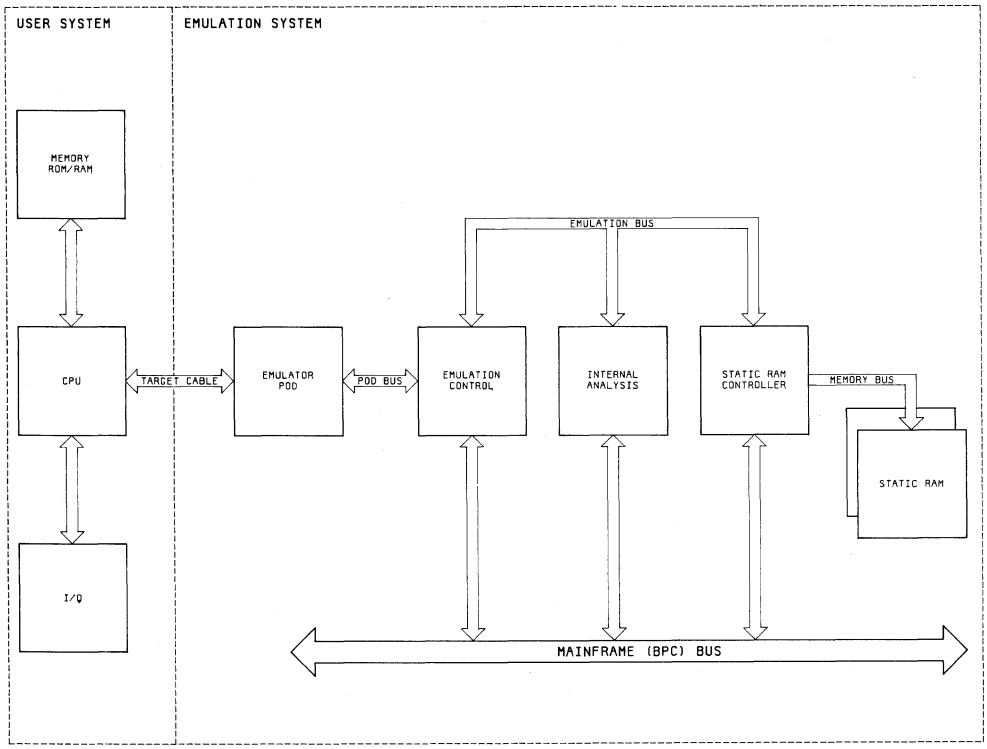


Figure 1-2. Emulation Subsystem

1-14. EQUIPMENT REQUIRED BUT NOT SUPPLIED.

1-15. A 64151 or 64155-66502 Memory Control Board is required to drive the 64161A, 64162A, or 64163A Emulator Memories.

1-16. TEST EQUIPMENT.

1-17. Table 1-1 lists the test equipment needed to repair and maintain Models 64161A/162A/163A.

Table 1-1

INSTRUMENT	RECOMMENDED MODEL	USE
Dual-trace Oscilloscope	HP1740A	Troubleshooting
Digital Voltmeter	HP3465A	Troubleshooting
64000 Extender Card	64100-66510	Troubleshooting
64000 Extender Cables (2)	8120-3350	Troubleshooting
Signature Analyzer	HP5004A, HP5005A	Troubleshooting
Memory Controller	HP64151A, HP64155	Troubleshooting

1-18. SPECIFICATIONS.

1-19. Specifications for the Model 64161A/162A/163A are listed in Table 1-2.

Table 1-2. Specifications.

	64161A	64162A	64163A
Power (Max Typ) mW			
0 rows selected	5283.7	5285.7	5285.7
1 row selected	8161.8	8163.7	8167.5
Current (Max Typ) mA			
0 rows selected	1056.7	1057.1	1057.9
1 row selected	1632.3	1632.7	1633.5

1-20. RELATED MANUALS.

1-21. Service Manuals.

64151A Memory Control Service Manual
64155 Memory Control Service Manual
64152A 32K Memory Service Manual

SECTION II

INSTALLATION

2-1. INTRODUCTION.

2-2. This section contains information for installing and removing the Model 64161A/162A/163A. Included are initial inspection procedures and instructions for repacking the instrument for shipment.

2-3. INITIAL INSPECTION.

2-4. Inspect the shipping container for damage. If the shipping container or cushioning material is damaged, it should be kept until contents of the shipment have been checked for completeness and the instrument has been checked mechanically and electrically. Procedures for checking electrical performance are given in Section IV. If the contents are incomplete, if there is mechanical damage or defect, or if the instrument does not pass the Performance Tests, notify the nearest Hewlett-Packard office. Keep the shipping materials for carrier`s inspection. The HP office will arrange for repair or replacement at HP's option without waiting for claim settlement.

2-5. INSTALLATION.

NOTE

If the following installation procedures are not followed, imaging problems may result.

2-6. The Models 64161A/162A/163A Emulation Memory Boards are installed using the following procedure. Figures 2-1 and 2-2 shows the recommended location of the emulation option boards in the HP64000 mainframes for two typical configurations: Emulation Memory only and Emulation Memory with Analysis. Note that with emulators which use the 64271A or 64274A Control Card, an analyzer is required; therefore, ignore the configurations shown without an analyzer when installing these emulator control cards.

a. Turn off power to the 64000 station.

b. Loosen the two hold-down screws and remove the card cage access cover (64100A). (Refer to 64110A Mainframe Service Manual for information on removing the card cage access cover of the 64110A.)

c. Install the emulation subsystem (control card and pod). Refer to the appropriate service manuals for the emulator concerned.

d. If an analyzer module (64300A or 64302A) is to be used, install it at this time. Refer to the 64300A/64302A Service Manuals for installation instructions.

e. Install the Memory Controller Module (64151A or 64155). Refer to the Service Manual for the Memory Controller in use for installation instructions. Do not install the Emulation Memory Boards or ribbon cables. This will be done later.

f. The address range jumpers on the Emulation Memory Boards must now be configured to select the base address range of each Memory Board (64161A/162A/163A) used in the mainframe. The address range selection is dependent on the number of Memory Boards installed in the development station. Refer to Table 2-1 through 2-4 and Figure 2-3 for information on where jumpers should be installed.

g. Once the address range jumper on each board is in the proper position, the Memory Boards must be installed in the development station. (Please refer to the Memory Space Configuration in the paragraphs beginning at 2-7 before installing your memory system.) Hold the board by the extractor levers, with the component side of the board facing the front of the development station, and the large motherboard connector (labeled "P1") pointing towards the bottom of the statin. Insert the board in the guide rails of the desired slot and push down until the P1 connector seats firmly in the motherboard connector at the bottom of the station.

h. Connect the Emulation Memory Bus ribbon cable across the left-hand set of edge connectors (as you face the front of the development station). The bus cables are keyed so that they will fit on the edge connectors in only one position.

i. Connect the Emulation Bus cables across the two right-hand sets of edge connectors (as you face the front of the development station). The bus cables are keyed so that they will fit on the edge connectors in only one position.

j. Reinstall the card cage access cover and tighten the 2 screws (64100A). (Refer to the 64110A Mainframe Service Manual for information on replacing the card cage access cover of the 64110A.)

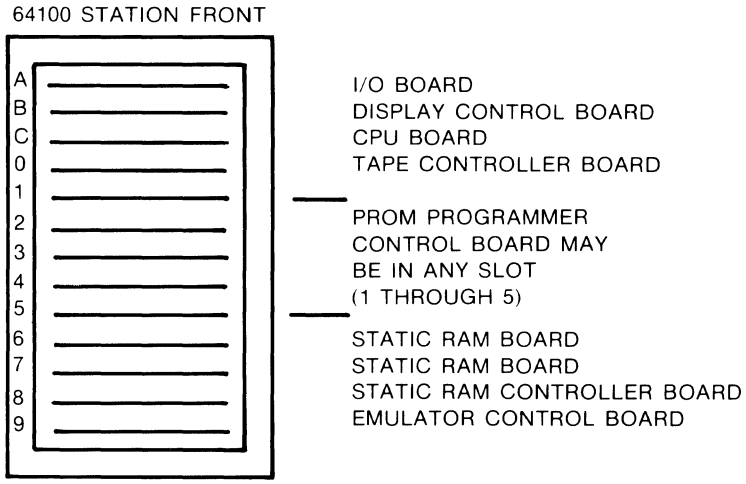


Figure 2-1. Emulation Memory Installation (with 6416X series memory only)

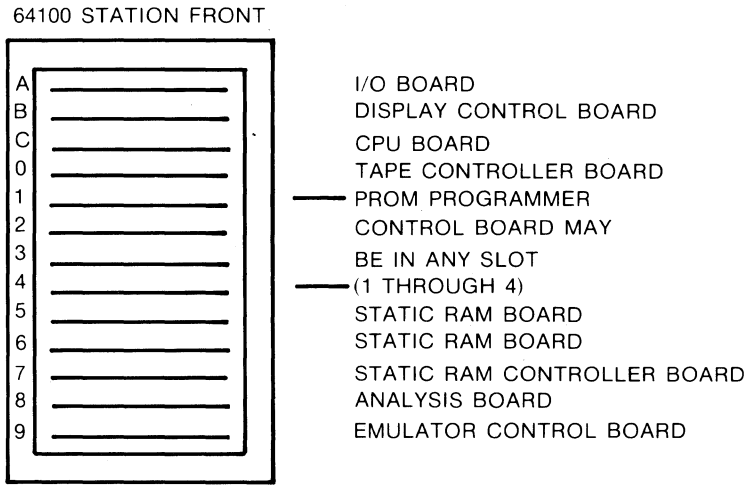
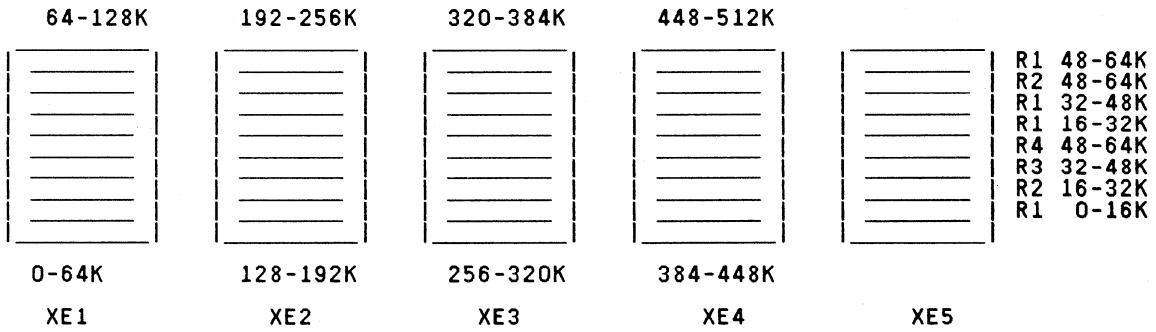


Figure 2-2. Emulation Memory Installation with Analysis



XE1-4 determine the addressable range of the Memory Card. The primary purpose for XE5 is to configure the 6416X series Memory to be compatible with the 6415X series Memory. XE5 performs row mapping. The following guidelines will help you avoid memory mapping errors.

When using 6416X series Memory Cards only.

1. The memory space defined by the 8-pin DIP jumper in XE1-4 may not overlap the address space assigned to any other memory card in systems using 64161A.

2. When using the 64161A the jumper in XE5 must be in the row 1-4.

3. When using a mixture of 64162A and 64163A cards the address space assigned in XE5 must not overlap when more than one card is assigned to the same address space in XE1-4.

When using a mixture of 6416X and 6415X Memory Cards.

1. When combining 6416X and 6415X Memory Cards you cannot assign address space higher than 64K words.

2. Be certain that the address space assigned to one card does not overlap the address space assigned to any other card.

3. Follow the configuration guides in Table 2-1 to Table 2-4.

Figure 2-3. Address Range Jumper Installation

2-7. MEMORY SPACE CONFIGURATION GUIDE

2-8. MEMORY SPACE CONFIGURATIONS WITH THE 64151A STANDARD MEMORY CONTROLLER

Model 64161A

64161A (128k bytes) cannot be attached to a 64151A memory controller that is attached to any of the 64152A/3A/4A or 64152B/3B/4B memory boards. A 64161A Memory Board must have an 8-pin DIP jumper in row 1-4 of XE5. Another 8-pin DIP jumper must be located in the 0-64k address range position in XE1.

Model 64162A

The 64162A (32K words) would normally be all the memory that could be used with the 64151A Memory Controller. Although the 64151A can be configured for 16 bit operation, the Model 64155A is usually recommended for 16 bit emulation. If your 16-bit emulation system permits the use of the 64151A Memory Controller, follow the configuration guide listed in Table 2-2 to expand to 64K words of memory.

Model 64163A

One of these boards may be attached to a Model 64151A along with one of the 64152/3/4 memory boards. If 6416X and 6415X memory boards are used together install the 6416X memory boards next to the 64151A Memory Controller. The 8-pin DIP jumper on the 64163A must be in XE1 in the position labeled 0-64K; the single jumper must be in XE5, in a position labeled R1. The address space of the 64152/3/4 memory boards being used must not overlap the address space assigned to the 64163A. Possible combinations of the 64163A and 64152/3/4 memory boards are listed in Table 2-1. Refer to Table 2-3 to assign address space to 64k word configurations when using the 64163A. The 8-pin DIP jumper must be in XE1, address range 0-64k on the 64162A board. The two single jumpers must be in XE5; one must be in a position labeled R1 and the other must be in a position labeled R2. The address space of R1 and R2 must not overlap. With 16-bit emulation two 64162A cards may be used.

Table 2-1.

	64163 row 1	64152/3/4
1	0-16K	16-32K
2	16-32K	0-16K

2-9. MEMORY CONFIGURATIONS WITH THE 64155A WIDE MEMORY CONTROLLER (with the 6416X memory you must use the 64155-66502 version)

Model 64161A

64161A (128k bytes) cannot be attached to a 64155A Memory Controller that is attached to any of the 64152/3/4 Memory Boards. A 64161A Memory Board must have a 8-pin DIP jumper in row 1-4 of XE5. Another 8-pin DIP jumper must be located in any one of the eight possible address range positions in XE1-XE4.

Model 64162A

The 64162A (64k bytes) can be used with a memory controller which has 64152A/64153A/64154A and/or 64152B/64153B/64154B Memory Boards. If 6416X and 6415X memory boards are used together DO NOT install the 6416X memory boards next to the 64155A Memory Controller. The 8-pin DIP jumper must be in XE1, address range 0-64k on the 64162A board. The two single jumpers must be in XE5; one must be in a position labeled R1 and the other must be in a position labeled R2. The address space of labels R1 and R2 must not overlap. The address space of the 64152/153/154 must not overlap the address space of the 64162A. A sample of address range configurations are listed in Table 2-2.

Table 2-2.

	64162		64152/3/4	64152/3/4
	row 1	row 2		
1*	0-16k	16-32k	32-48k	48-64k
2*	0-16k	48-64k	16-32k	32-48k
3+	16-32k	48-64k	0-16k	32-48k
4+	32-48k	16-32k	0-16k	48-64k
5+	32-48k	48-64k	0-16k	16-32k
6+	48-64k	16-32k	0-16k	32-48k

*In configuration 1 and 2 if there is only one 64152/3/4 it can occupy either address space listed for the 64152/3/4 boards.
+In configurations 3-6 there must be a block of memory with physical location at 0-16k; if there is only one 64152/3/4 it must be set to location 0-16k.

Model 64163A

One, two, or three of these boards can be attached to a memory control board along with three, two or one of the 64152/3/4 memory boards. If 6416X and 6415X memory boards are used together DO NOT install the 6416X memory boards next to the 64155 Memory Controller.

The 8-pin DIP jumper on the 64163A must be in XE1 in the position labeled 0-64k; Each board has a single jumper which must be put in a position labeled R1. If more than one of the 64163A Memory Boards are being used the address space of the R1 labels must not overlap.

The address space of the 64152/3/4 memory boards being used must not overlap the address space assigned to the 64163A memory boards being used. Possible combinations of 64152/3/4 memory boards and 64163A memory boards are listed in Table 2-3.

Table 2-3.

	64163 row 1	64152/3/4	64152/3/4	64152/3/4
1*	0-16k	16-32k	32-48k	48-64k
2+	16-32k	0-16k	32-48k	48-64k
3+	32-48k	0-16k	16-32k	48-64k
4+	48-64k	0-16k	16-32k	32-48

	64163 row 1	64163 row 1	64152/3/4	64152/3/4
5*	0-16k	16-32k	32-48k	48-64k
6*	0-16k	32-48k	16-32k	48-64k
7*	0-16k	48-64k	16-32k	32-48k
8+	16-32k	32-48k	0-16k	48-64k
9+	16-32k	48-64k	0-16k	32-48k
10+	32-48k	48-64k	0-16k	16-32k

	64163 row 1	64163 row 1	64163 row 1	64152/3/4
11	0-16k	16-32k	32-48k	48-64k
12	0-16k	32-48k	48-64k	16-32k
13	0-16k	16-32k	48-64k	32-48k
14+	16-32k	32-48k	48-64k	0-16k

*in configurations 1,5,6,7 if there is only one 64152/3/4 memory board it can occupy either address space listed for 64152/3/4 memory boards.
+in configurations 2-4,8-10, 14; there must be a block of memory located at 0-16k, so one of the 64152/3/4 memory boards must be set to location 0-16k.

Model 64162 with Model 64163

A combination of 64162A and 64163A boards may be attached to a memory controller with one 64152/3/4 memory board.

The 8-pin DIP jumper on the 64162 and the 64163 must be in the position 0-64k. For the two single jumpers of the 64162, one must be in a position labeled with R1 and the other must be in a position labeled with R2. The single jumper must be in a position labeled R1 on the 64163. The address spaces of the single jumpers must not over lap each other.

The address space assigned to each board must not overlap the address space assigned to any of the other boards.

Table 2-4

	64162 row 1	64162 row 2	64163 row 1	64163 row 1
1	0-16k	16-32k	32-48k	48-64k
2	0-16k	16-32k	48-64k	32-48k
3	0-16k	48-64k	16-32k	32-48k
4	0-16k	48-64k	32-48k	16-32k
5	16-32k	48-64k	0-16k	32-48k
6	16-32k	48-64k	32-48k	0-16k
7	32-48k	16-32k	0-16k	48-64k
8	32-48k	16-32k	48-64k	0-16k
9	32-48k	48-64k	0-16k	16-32k
10	32-48k	48-64k	16-32k	0-16k
11	48-64k	16-32k	0-16k	32-48k
12	48-64k	16-32k	32-48k	0-16k

2-10. OPERATING ENVIRONMENT.

2-11. The 64161A/162A/163A may be operated in environments within the following limits:

Temperature.....0°C to 40°C
Humidity.....5 to 80% relative humidity at 40°C
Altitude.....4 600 M (15 000 ft)

It should be protected from temperature extremes which cause condensation within the instrument.

2-12. STORAGE AND SHIPMENT.

2-10. Environment.

2-13. The 64161A/162A/163A may be stored or shipped in environments within the following limits:

Temperature.....-40°C to +75°C
Humidity.....5 to 80% relative humidity
Altitude.....15 000 m (50 000 ft)

2-14. Packaging.

2-15. Original Packaging. Containers and materials identical to those used in factory packaging are available through Hewlett-Packard offices. If the instrument is being returned to Hewlett-Packard for servicing, attach a tag indicating the type of service required, return address, model number, and full serial number. Also, mark the container FRAGILE to ensure careful handling. In any correspondence, refer to the instrument by model number and full serial number.

2-17. Other Packaging. The following general instructions should be used for repacking with commercially available materials:

a. Wrap instrument in heavy paper or plastic. (If shipping to Hewlett-Packard office or service center, attach tag indicating service required, return address, model number, and full serial number.)

b. Use strong shipping container. A double-wall carton made of 350-pound test material is adequate.

c. Use a layer of shock-absorbing material 70 to 100 mm (3- to 4-inch) thick around all sides of the instrument to provide firm cushioning and prevent movement inside container.

d. Seal shipping container securely.

e. Mark shipping container FRAGILE to ensure careful handling.

f. In any correspondence, refer to instrument by model number and full serial number.

SECTION III

OPERATION

Operation of the Model 64161A/162A/163A is beyond the scope of this manual. Emulation memory is an integral part of the emulation subsystem.

SECTION IV

PERFORMANCE VERIFICATION AND TROUBLESHOOTING

4-1. INTRODUCTION.

4-2. This section describes the Performance Verification for the Models 64161A/64162A/64163A Emulation Memory Boards.

4-3. This section is divided into two subsections: How to Run Performance Verification, and How to Interpret Performance Verification. Although the first subsection provides instructions on running several tests, only two tests will be described in the interpretation.

4-4. Use the following instructions to find the paragraphs which describe the Performance Verification of your system.

a. Be certain that your Memory subsystem is installed according to the directions in Section II.

b. For a system that is configured with a 64151A Memory Control Board.

4-9. How to Run Performance Verification
4-15. How to Interpret Performance Verification

c. For a system that is configured with a 64155 Memory Control
4-12. How to Run Performance Verification with a mixture of 6416X and 6415X Memory Boards.
4-12. How to Run Performance Verification with only 6416X memory boards.
4-20. How to Interpret Performance Verification.

4-5. PERFORMANCE VERIFICATION.

4-6. The Performance Verification for the Models 64161A/64162A/64163A Emulation Memory is a subset of the 64000 system opt_test Performance Verification. The opt_test Performance Verification tests all possible option modules that can be configured within the expansion slots of the 64000 mainframe. Table 4-1 defines the softkey options available.

4-7. The scope of the Performance Verification procedures in this section is to provide the minimum amount of information necessary to completely verify the operation of the Emulation Memory Boards. Procedures for complete verification of the Emulation Memory subsystem are treated in the Service Manulas for the Emulation Memory Controllers and are not repeated here (although the user may be referred to these manuals while using the Performance Verification procedures).

Table 4-1. Option Test Softkey Definitions

<end>	Causes the test currently executing to abort and returns to the overview menu.
<cycle>	Causes the performance verification software to test each block of memory in turn, stepping to the next block as the testing of each block is completed.
<next_test>	Causes the inverse video bar to move highlighting the address range of the next block of emulation memory to be tested.
<start>	Causes the performance verification software to begin testing emulation memory in the address range currently highlighted by the inverse video bar.
<print>	Causes the performance verification test results (the area above the status line on the display) to be copied to the system printer, if one is connected.
<prev_test>	Causes the inverse video bar to highlight the address range immediately prior to the one currently highlighted. Used to select a desired block of memory for testing.
<img_test>	Causes image testing to be commenced on the block of memory whose address range is highlighted by the inverse video bar on the display. Used to check for address line problems.
<retn_test>	Causes the Performance Verification software to initiate the retention testing sequence, which is used to verify that the static RAM will hold a "0" or "1" for a certain amount of time.
<print>	Causes the test results above the status line to be copied to the system printer if one is connected.

4-8. HOW TO RUN PERFORMANCE VERIFICATION.

4-9. Memory PV With Model 64151A Memory Controller. (Configured in an 8-bit mode)

4-10. To run Performance Verification for the Emulation Memory Boards when a Model 64151A is being used as the emulation controller, use the following procedure:

a. Disconnect the target system.

b. Install the Emulation Memory subsystem in the HP 64000 development station. Refer to Section II of this manual for installation instructions. NOTE: FOR PERFORMANCE VERIFICATION--IF YOU ARE USING A COMBINATION OF 6416X AND 6415X MEMORY BOARDS ONE OF THE 6416X MEMORY BOARDS MUST BE INSTALLED NEXT TO THE 64151 MEMORY CONTROLLER.

c. With the operating system initialized and awaiting a command , manually type or use the softkey:

```
opt_test      RETURN
<slot #> (of 64151A)    RETURN
<next_test>  (until inverse video bar highlights the
              Processor Control Test)
<start>
<cycle>
```

This will test all available blocks of emulation memory. NOTE: If emulation memory is unavailable in any particular address range, then "FFFF" will be displayed as the status; however, "# of fails" will be displayed as a "0".

d. If all available blocks of emulation memory test correctly, then the Emulation Memory Boards function correctly. It is then advisable to proceed with the remainder of the Emulation Memory subsystem testing as outlined in the appropriate Emulation Memory Controller Service Manual.

4-11. Memory Performance Verification with Model 64155A Memory Controller.

4-12. The following instructions cover Performance Verification for the Memory Controller and the Memory Boards. Only the "Memory Test" is described in this manual (paragraph 4-20). If the other tests fail, please refer to the 64155A Memory Control Service Manual. To run Performance Verification for the Emulation Memory Boards when a Model 64155A is being used as the Emulation Memory Controller, proceed as follows:

Running PV with a mixture of 6415X and 6416X memory boards.

a. Disconnect the target system.

b. Install the Emulation Memory subsystem in the HP64000 development station. Refer to Section II of this manual for installation instructions. NOTE: WHEN USING BOTH 6416X SERIES MEMORY AND 6415X MEMORY IN AN EMULATION SUBSYSTEM THE 6416X MEMORY BOARDS MUST NOT BE INSTALLED IN AN OPTION SLOT ADJACENT TO THE MODEL 64155 MEMORY CONTROLLER.

Running PV with 6416X Memory Boards only.

a. Disconnect the target system.

b. Install the Emulation Memory subsystem in the HP64000 development station. Refer to Section II of this manual for installation instructions. NOTE: FOR PERFORMANCE VERIFICATION--THE 6416X MEMORY BOARD MUST BE INSTALLED IN A SLOT ADJACENT TO THE MEMORY CONTROLLER.

The following steps are identical for any memory board configuration with the 64155A Memory Controller.

c. With the operating system initialized and awaiting a command, manually type or use the softkey:

```
opt_test    RETURN
<slot #> (for 64155A)  RETURN
select the memory range *
```

*select the maximum memory range in "K words" of the memory boards being tested. For example, if the highest memory range of the boards being tested is 256K-320K (as indicated by the jumper located in XE1,XE2,XE3,XE4) depress the softkey corresponding to that range. When using a mixture of 6416X and 6415X memory always select 0-64k. It is not necessary to RETURN.

<next_test> (until inverse video bar highlights the "System->Board Access Test")
<select>

This will display the "System->Board Access Test"

<cycle>

Cycle through the test several times. If no failures occur, press the <end> softkey which will return the display to the Memory Performance Verification overview menu.

<next_test> (until inverse video bar highlights the "Memory Mapper" test)
<select>

This will display the "Memory Mapper" test.

<cycle>

Cycle through the Memory Mapper test sequence several times. If no failures occur, press the <end> softkey to return to the Memory PV overview menu.

<next_test> (until inverst video bar highlights "Memory Control" test)
<select>

This will display the "Memory Control" test.

<cycle>

Cycle through the "Memory Control" test several times. If no failures occur, press the <end> softkey to return to the Memory PV overview menu.

<next_test> (until inverse video bar highlights "Memory Test")

<select>

This will display the "Memory Test"

<cycle>

NOTE: if emulation memory is unavailable in any particular address range, then "FFFF" will be displayed as the status; however, "# of fails" will be displayed as a "0".

Allow the "Memory Test" to cycle through the test several times. This will test all available blocks of memory up to the limit specified when the address range was selected. If desired, each individual block may also be tested for possible imaging problems and data retention failures by moving the highlighted inverse video bar to the desired block of memory with the <next_test> and <prev_test> keys, then pressing the <img_test> or <retn_test> softkeys to perform the necessary tests.

If all available blocks of memory test with no failures, then the Emulation Memory Boards work correctly. It is advisable to proceed with the remainder of the Emulation Memory Subsystem testing as outlined in the Emulation Memory Controller Service Manual.

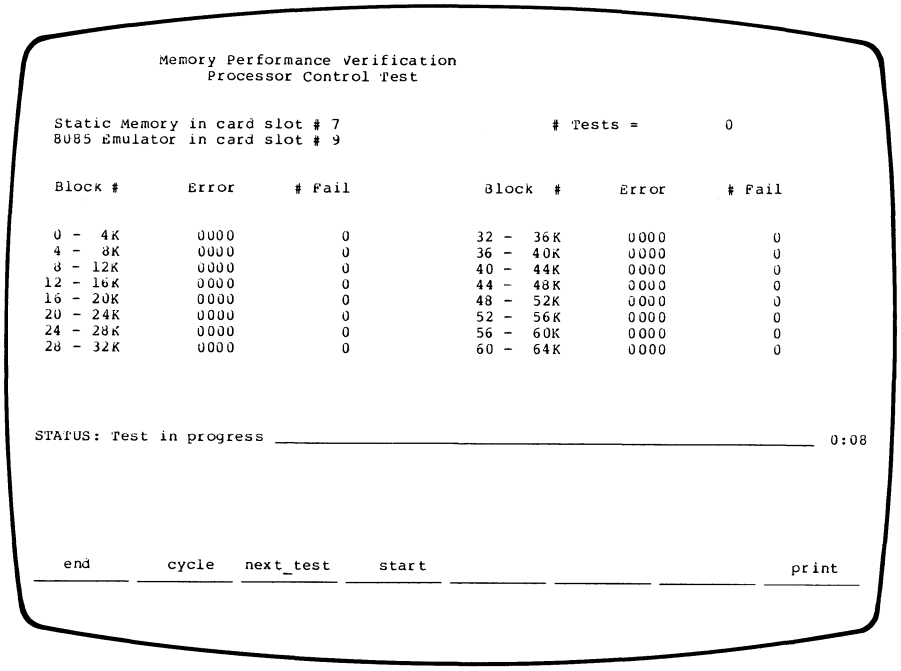


Figure 4-1. Processor Control Test Display.

4-13. HOW TO INTERPRET PERFORMANCE VERIFICATION.

4-14. Theory of Operation for the Memory Performance Verification is treated on a software test/results interpretation basis only; and is treated separately for Emulation Memory Boards driven by the 64151A and 64155 Emulation Memory Controllers.

4-15. Model 64151A/Emulation Memory--Processor Control Test.

4-16. Purpose--verifies that all the memory cells in a selected row can be written with random data patterns and that the data written can be read back correctly.

4-17. How--The Mainframe CPU initializes the Memory Controller Board and programs the memory mapper. Random data is then written to the first cell in the selected row of memory (a row is 16K deep by 16 bits wide). The data just written to this cell is immediately read back and compared with that written. The process then continues with each cell in turn. At the end of this process, the entire row of memory is read back and checked to verify that no RAM cells were overwritten by an address imaging problem (image testing is described further in the following paragraph). Errors are logged in a cumulative fashion to the status display.

4-18. Results--if no failures occur in the tested block of memory, the # fails indicator will be left at "0" and the "Error" message will display 0000 (hexadecimal), opposite the address range information for the selected block. However, if failures do occur in the tested block of memory, the # fails indicator will be incremented for each time that the test is run, and the "Error" message of 0000H will be replaced with a hexadecimal status message that indicates the position of the failing data bits. A "one" is placed in the status message for every data bit that is failing. To decode the status message, use the Table 4-1.

4-19. Because the memory is tested in 4K blocks and each IC is 16k long, imaging of 4K block sections is tested. The upper two address bits (A13, A12) are represented in the line "Image Errors" X1X2. If X1 is a "1" A13 is bad, if X0 is "1" A12 is bad.

Table 4-2. Data Failure Status Decoding

XXXX =	0000	0000	0000	0000	
	----	----	----	---1	D0
	----	----	----	--1-	D1
	----	----	----	-1--	D2
	----	----	----	1---	D3
	----	----	---1	----	D4
	----	----	--1-	----	D5
	----	----	-1--	----	D6
	----	----	1---	----	D7
	----	---1	----	----	D8
	----	--1-	----	----	D9
	----	-1--	----	----	D10
	----	1---	----	----	D11
	---1	----	----	----	D12
	--1-	----	----	----	D13
	-1--	----	----	----	D14
	1---	----	----	----	D15

Table 4-3.

ERROR CODE		1		C		0		9	
BINARY		0 0 0 1		1 1 0 0		0 0 0 0		1 0 0 1	
1	0-16 16-32 32-48 48-64	U7P U7O U7N U7M		U7L U7K U7J U7I		U7H U7G U7F U7E		U7D U7C U7B U7A	
2	16-32 48-64	U6P U6O U6N U6M		U6L U6K U6J U6I		U6H U6G U6F U6E		U6D U6C U6B U6A	
3	32-48	U5P U5O U5N U5M		U5L U5K U5J U5I		U5H U5G U5F U5E		U5D U5C U5B U5A	
4	48-64	U4P U4O U4N U4M		U4L U4K U4J U4I		U4H U4G U4F U4E		U4D U4C U4B U4A	
ROW	ADDRESS RANGE								
DATA BITS		D15 D14 D13 D12		D11 D10 D9 D8		D7 D6 D5 D4		D3 D2 D1 D0	
DATA BUFFERS		U3N		U3M		U3L		U3K	
		UPPER BYTE				LOWER BYTE			

4-20. Memory Test with the 64155 Controller.

4-21. Purpose--Verifies that all memory cells in the selected row can be written with random data patterns and that the data written can be read back correctly. If desired, the test can also verify that no address imaging problems exist, and that the RAM cells can retain data for a certain amount of time.

4-22. What--Each possible test is described in the paragraphs below.

a. Memory Test. The Mainframe CPU initializes the Memory Controller Board and programs the memory mapper. Random data is then written to the first cell in the selected row of memory (a row is 16K deep by 16 bits wide). The data just written to this cell is immediately read back and compared with that written. The process then continues with each cell in turn. At the end of this process, the entire row of memory is read back and checked to verify that no RAM cells were overwritten by an address imaging problem (image testing is described further in the following paragraph). Errors are logged in a cumulative fashion to the status display.

b. Image Test. If the <img_test> softkey is pressed, the Performance Verification software initiates image testing of the selected row of RAM. This testing checks for open or shorted address lines. The reasons for and process of image testing are best explained by examining the case of an 8 X 1 RAM device.

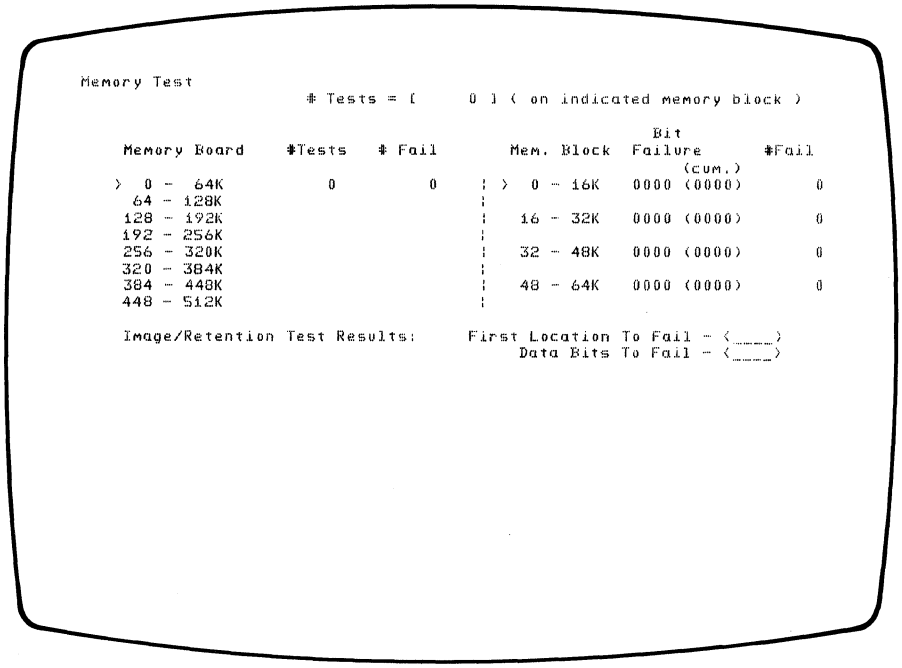


Figure 4-2. Memory Test Display

Suppose we proceed to image test the RAM, and there are no address line problems or other problems associated with the RAM. We would proceed with image testing the Most Significant address line of the RAM by pulling it low, then high, while incrementing the least significant address bits. Note that at the same time that the most significant address bit is changed, we also change the data written into the RAM from a "0" to a "1". The loaded RAM appears as follows:

8 x 1 RAM

ADDRESS	DATA
000	0
001	0
010	0
011	0
100	1
101	1
110	1
111	1

If the data is now read back, and there are no address line problems, then the correct data is interpreted as coming from each location.

Now let's examine the same situation, but with a different twist. We're still testing the most significant address bit for an imaging problem, but this time, it's not making contact with the address input of the RAM because of a bad socket (or for whatever other reason). Note: it is important to remember that unconnected inputs in TTL and MOS generally float to the high state. When we try to load the first four locations, here's what happens:

8 x 1 RAM

ADDRESS	DATA
000	x
001	x
010	x
011	x
100	0
101	0
110	0
111	0

No data is loaded into the first four locations because the most significant address line could not be pulled low.

Instead, the 0's are loaded into the next four locations because the most significant address bit floats to the high state. When the next four locations are loaded the results are as follows:

8 x 1 RAM

ADDRESS	DATA
000	x
001	x
010	x
011	x
100	1
101	1
110	1
111	1

Notice that the 1's are loaded into the correct locations, because the MSB address line has floated high, however, they overwrite the 0's that were written earlier.

What happens now? When the performance verification software attempts to read the RAM back, it will begin by attempting to read loactions 000-011, at which it tried to store 0's. However, since the most significant address line is open, it reads back the 1's that were stored at 1000-111--which is the "image" of the lower address range. The 1's were not the correct response; therefore, an error message is displayed for loactions 000-011. To trouble-shoot this type of failure, the technician only needs to determine which address line would have to be open to cause one set of addresses to fail and another set of addresses to pass.

c. Retention Test. This test checks the ability of each RAM cell to hold data for a defined length of time. To do this, the mainframe CPU writes 0&s to every location in memory, waits 60 seconds, then reads every location back, The process is repeated by writing 1's to all locations, then reading the locations back after approximately 60 seconds. As soon as a failure is detected in either test, the testing is aborted.

4-23. Results.

a. Memory Test. If no data failures are encountered during testing of the selected 64K address range, then the "#FAIL" status is left at 0. This information is displayed on the left hand side of the screen. If failures occur during the course of the test, then "# FAIL" status is incremented once for every time the test is run. The right side of the display divides each 64K memory block

into four 16K blocks which correspond to the four rows of memory chips. The "BIT FAILURE" status will display a hexadecimal status message indicating the position of the failing bits. To interpret the status message refer to Table 4-x.

b. Image Test. If no failures are found during the image testing, then the "First Location to Fail" status and the "Data Bits to Fail" status will be left blank. These status lines are located directly across from the "Image/ Retention Test Results" line on the display. If a failure is encountered during the course of the image testing, then the blank "First Location to Fail" status will be replaced by a hexadecimal status message which shows the address of the first failure location; and the "Data Bits to Fail" status will be replaced by a hexadecimal status message which shows the data bits which failed at that locations. For information on decoding the data status, refer to Table 4-x.

c. Retention Test. If no failures are found during the retention testing, then the "First Location to Fail" status and the "Data Bits to Fail" status will be left blank. These status lines are located directly across from the "Image/Retention Test Results" line on the display. However, if a failure is encountered during the retention testing, then the test aborts. The blank "First Location to Fail" status will be replaced with a hexadecimal status message which shows the address location of the memory cell that changed during the lag time between the write and the read; the "Data Bits to Fail" status will be replaced with a hexadecimal status message which shows the data RAM's that were unable to retain the information for the required length of time. For information on decoding the data status, refer to Table 4-1.

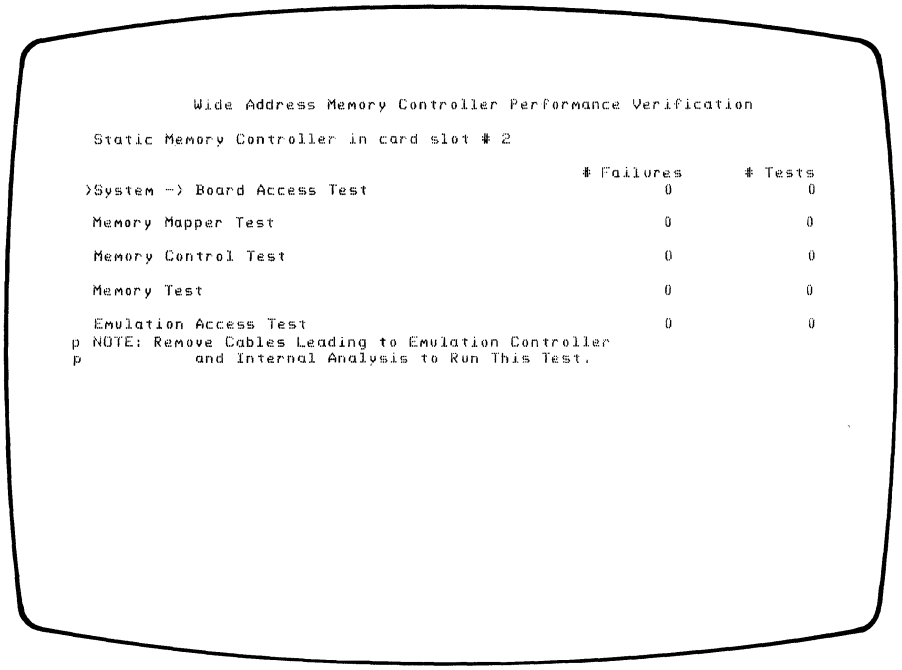


Figure 4-3. Performance Verification Overview Display

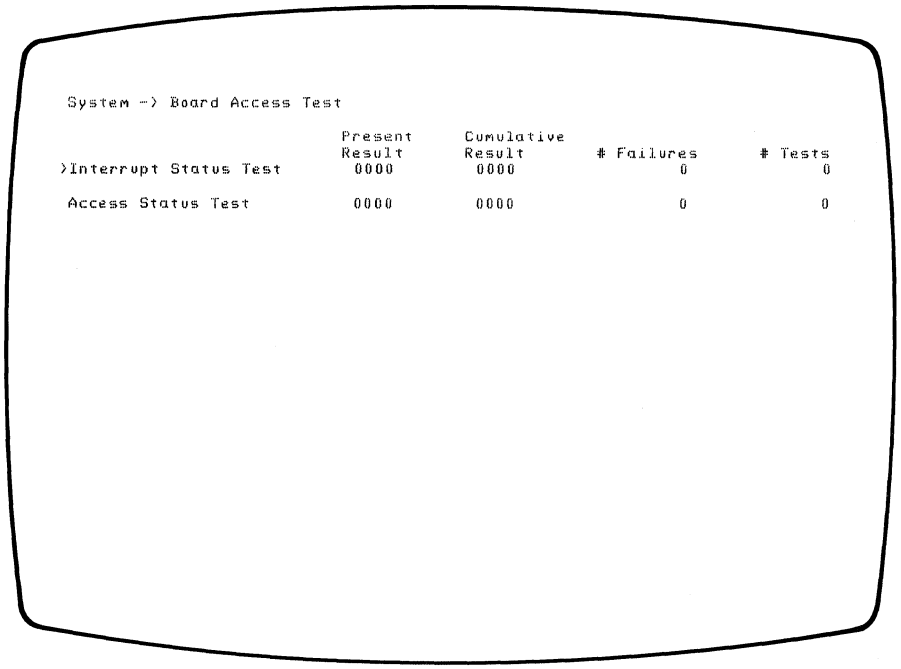


Figure 4-4. System-Board Access Test Display

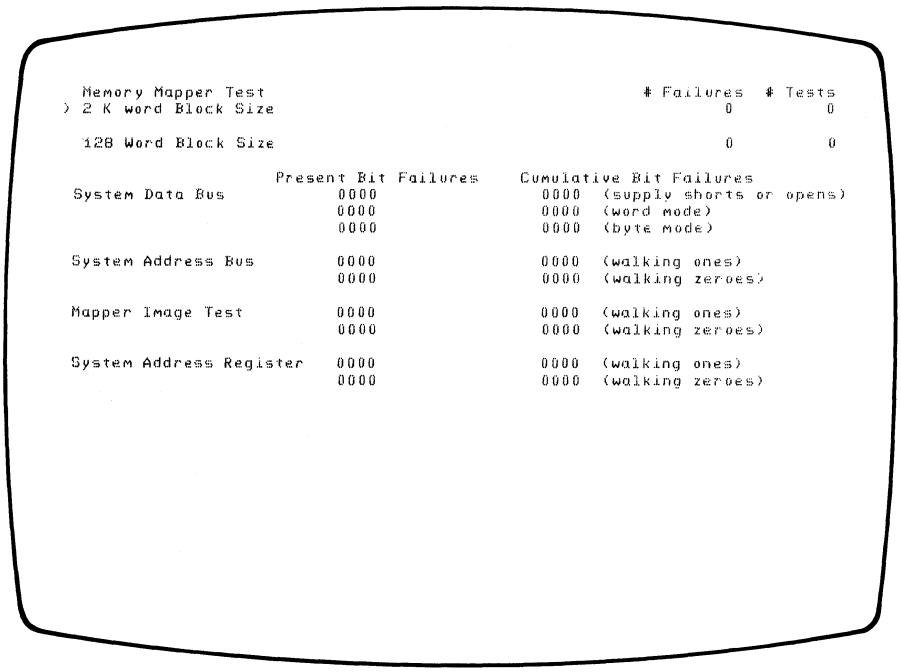


Figure 4-5. Memory Mapper Test Display

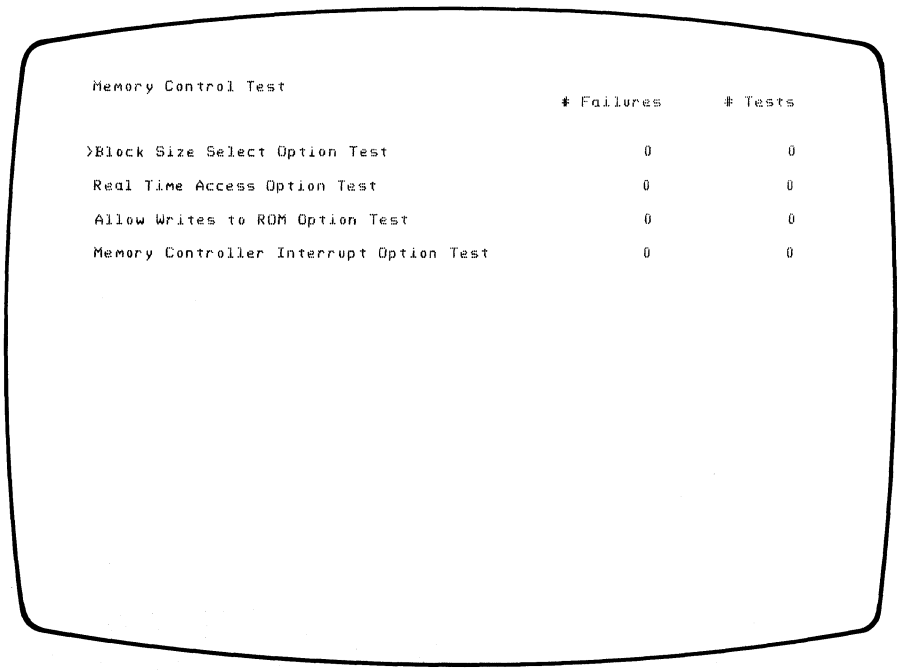


Figure 4-6. Memory Control Test Display

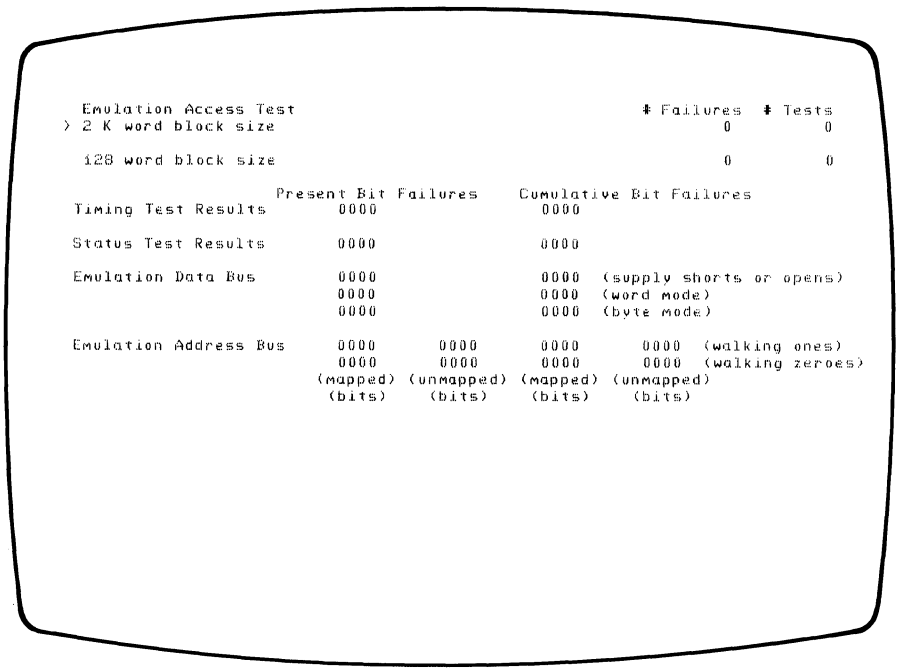


Figure 4-7. Emulation Access Test Display.

SECTION V

ADJUSTMENTS

Models 64161A/162A/163A Emulation Memory require no adjustments.

SECTION VI

REPLACEABLE PARTS

6-1. INTRODUCTION.

6-2. This section contains information for ordering parts. Table 6-1 lists abbreviations used in the parts list and throughout the manual. Table 6-2 lists all replaceable parts in reference designator order. Table 6-3 contains names and addresses that correspond to the manufacturers' code numbers.

6-3. ABBREVIATIONS.

6-4. Table 6-1 lists abbreviations used in the parts list, the schematics and throughout the manual. In some cases, two forms of the abbreviations are used, one all in capital letters, and one partial or no capitals. This occurs because the abbreviations in the parts list are always all capitals. However, in the schematics and other parts of the manual , other abbreviation forms are used with both lower case and upper case letters.

6-5. REPLACEABLE PARTS LIST.

6-6. Table 6-2 is the list of replaceable parts and is organized as follows:

a. Electrical assemblies and their components in alphanumerical order by reference designation.

b. Chassis-mounted parts in alphanumerical order by reference designation.

c. Miscellaneous parts.

d. Illustrated parts breakdowns, if appropriate.

The information given for each part consists of the following:

a. The Hewlett-Packard part number.
b. The total quantity (Qty) in the instrument.
c. The description of the part.
d. A typical manufacturer of the part in a five-digit code.
e. The manufacturer`s number for the part.

The total quantity for each part is given only once--at the first appearance of the part number in the list.

6-7. ORDERING INFORMATION.

6-8. To order a part listed in the replaceable parts table, quote the Hewlett-Packard part number, indicate the quantity required, and address the order to the nearest Hewlett-Packard office.

6-9. To order a part that is not listed in the replaceable parts table, include the instrument model number, instrument serial number, the description and function of the part, and the number of parts required. Address the order to the nearest Hewlett-Packard Office.

6-10. SPARE PARTS KIT.

6-11. At this time no Spare Parts Kit is available for this instrument

6-12. DIRECT MAIL ORDER SYSTEM.

6-13. Within the USA, Hewlett-Packard can supply parts through a direct mail order system. Advantages of using the system are as follows:

a. Direct ordering and shipment from the HP Parts Center in Mountain View, California.

b. No maximum or minumum on any mail order (there is a minimum order amount for parts ordered through a local HP office when orders require billing and invoicing).

c. Prepaid transportation (there is a small handling charge for each order).

d. No invoices--to provide these advantages, a check or money order must accompany each order.

6-14. Mail order forms and specific ordering information is available through your local HP office. Addresses and phone numbers are located at the back of this manual.

Table 6-1. Reference Designators and Abbreviations

REFERENCE DESIGNATORS

A	= assembly	**F**	= fuse	**MP**	= mechanical part	**U**	= integrated circuit
B	= motor	**FL**	= filter	**P**	= plug	**V**	= vacuum, tube, neon bulb, photocell, etc
BT	= battery	**IC**	= integrated circuit	**Q**	= transistor		
C	= capacitor	**J**	= jack	**R**	= resistor	**VR**	= voltage regulator
CP	= coupler	**K**	= relay	**RT**	= thermistor	**W**	= cable
CR	= diode	**L**	= inductor	**S**	= switch	**X**	= socket
DL	= delay line	**LS**	= loud speaker	**T**	= transformer	**Y**	= crystal
DS	= device signaling (lamp)	**M**	= meter	**TB**	= terminal board	**Z**	= tuned cavity network
E	= misc electronic part	**MK**	= microphone	**TP**	= test point		

ABBREVIATIONS

A	= amperes	**H**	= henries	**N/O**	= normally open	**RMO**	= rack mount only
AFC	= automatic frequency control	**HDW**	= hardware	**NOM**	= nominal	**RMS**	= root-mean square
AMPL	= amplifier	**HEX**	= hexagonal	**NPO**	= negative positive zero (zero temperature coefficient)	**RWV**	= reverse working voltage
		HG	= mercury				
BFO	= beat frequency oscillator	**HR**	= hour(s)				
BE CU	= beryllium copper	**HZ**	= hertz	**NPN**	= negative-positive-negative	**S-B**	= slow-blow
BH	= binder head					**SCR**	= screw
BP	= bandpass			**NRFR**	= not recommended for field replacement	**SE**	= selenium
BRS	= brass	**IF**	= intermediate freq			**SECT**	= section(s)
BWO	= backward wave oscillator	**IMPG**	= impregnated	**NSR**	= not separately replaceable	**SEMICON**	= semiconductor
		INCD	= incandescent			**SI**	= silicon
CCW	= counter-clockwise	**INCL**	= include(s)			**SIL**	= silver
CER	= ceramic	**INS**	= insulation(ed)	**OBD**	= order by description	**SL**	= slide
CMO	= cabinet mount only	**INT**	= internal	**OH**	= oval head	**SPG**	= spring
COEF	= coeficient			**OX**	= oxide	**SPL**	= special
COM	= common	**K**	= kilo=1000			**SST**	= stainless steel
COMP	= composition					**SR**	= split ring
COMPL	= complete	**LH**	= left hand	**P**	= peak	**STL**	= steel
CONN	= connector	**LIN**	= linear taper	**PC**	= printed circuit		
CP	= cadmium plate	**LK WASH**	= lock washer	**PF**	= picofarads= 10^{-12} farads	**TA**	= tantalum
CRT	= cathode-ray tube	**LOG**	= logarithmic taper			**TD**	= time delay
CW	= clockwise	**LPF**	= low pass filter	**PH BRZ**	= phosphor bronze	**TGL**	= toggle
				PHL	= phillips	**THD**	= thread
DEPC	= deposited carbon	**M**	= milli=10^{-3}	**PIV**	= peak inverse voltage	**TI**	= titanium
DR	= drive	**MEG**	= meg=10^{6}	**PNP**	= positive-negative-positive	**TOL**	= tolerance
		MET FLM	= metal film			**TRIM**	= trimmer
ELECT	= electrolytic	**MET OX**	= metallic oxide	**P/O**	= part of	**TWT**	= traveling wave tube
ENCAP	= encapsulated	**MFR**	= manufacturer	**POLY**	= polystyrene		
EXT	= external	**MHZ**	= mega hertz	**PORC**	= porcelain	**U**	= micro=10^{-6}
		MINAT	= miniature	**POS**	= position(s)		
F	= farads	**MOM**	= momentary	**POT**	= potentiometer	**VAR**	= variable
FH	= flat head	**MOS**	= metal oxide substrate	**PP**	= peak-to-peak	**VDCW**	= dc working volts
FIL H	= fillister head	**MTG**	= mounting	**PT**	= point		
FXD	= fixed	**MY**	= "mylar"	**PWV**	= peak working voltage	**W/**	= with
						W	= watts
G	= giga (10^{9})	**N**	= nano (10^{-9})	**RECT**	= rectifier	**WIV**	= working inverse voltage
GE	= germanium	**N/C**	= normally closed	**RF**	= radio frequency		
GL	= glass	**NE**	= neon	**RH**	= round head or right hand	**WW**	= wirewound
GRD	= ground(ed)	**NI PL**	= nickel plate			**W/O**	= without

Table 6-2. Replaceable Parts List

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1	64161-66501	8	1	BOARD ASSEMBLY-MEMORY 128K	28480	64161-66501
C1-C2	0160-5246	6	80	CAPACITOR-FXD .1 UF +80-20% 50 VDC CER	28480	0160-5246
C3-C4	0180-0229	4	4	CAPACITOR-FXD 22 UF +-10% 15 VDC TA	28480	0180-0229
C5-C62	0160-5246	6		CAPACITOR-FXD .1 UF +80-20% 50 VDC CER	28480	0160-5246
TP1-TP3	0360-0535	0	3	TERM TEST POINT	28480	0360-0535
R1-R2	0757-0280	3	6	RESISTOR 1K 1% .125W F TC=0+-100	28480	0757-0280
R3-R4	0698-3432	7	2	RESISTOR 26.1 1% .125W F TC=0+-100	28480	0698-3432
R5	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	28480	0757-0280
R6-R9	0757-0399	5	4	RESISTOR 82.5 1% .125W F TC=0+-100	28480	0757-0399
R10-R12	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	28480	0757-0280
XE1-XE5	1200-0607	0	5	SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
E1-E2	1251-4398	1	2	SHUNT DIP 4 POSITION; DUAL INLINE PKG	28480	1251-4398
RP1	1810-0275	1	1	NETWORK-RES 10-SIP 1.0K OHM X 9	28480	1810-0175
UR3C-UR3F	1810-0600	6	4	NETWORK-RES 16-DIP 40.0 OHM X 8	28480	1810-0600
U2C	1820-1633	8		IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U2D	1820-1633	8		IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U2E	1820-1633	8		IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U2F	1820-1633	8		IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U2G	1820-2861	5	4	IC DCDR TTL F 3-TO-8 LINE 3-INP	07263	74F138PC
U2H	1820-2861	5		IC DCDR TTL F 3-TO-8 LINE 3-INP	07263	74F138PC
U2I	1820-2861	5		IC DCDR TTL F 3-TO-8 LINE 3-INP	07263	74F138PC
U2J	1820-2861	5		IC DCDR TTL F 3-TO-8 LINE 3-INP	07263	74F138PC
U2K	1820-2690	9	1	IC GATE TTL F OR QUAD 2-INP	07263	74F32
U2L	1820-1198	0	2	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS03N
U2M	1820-1198	0		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS03N
U3G	1820-1204	9	1	IC GATE TTL LS NAND DUAL 4-INP	01295	SN74LS20
U3J	1820-2684	1	1	IC GATE TTL F NAND QUAD 2-INP	07263	74F00
U3K	1820-1633	8	8	IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U3L	1820-1633	8		IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U3M	1820-1633	8		IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U3N	1820-1633	8		IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U4A-U4P	1818-1969	8	64	IC CMOS F16384 (16K) STAT RAM 70NS	S4013	HM6167P
U5A-U5P	1818-1969	8		IC CMOS F16384 (16K) STAT RAM 70NS	S4013	HM6167P
U6A-U6P	1818-1969	8		IC CMOS F16384 (16K) STAT RAM 70NS	S4013	HM6167P
U7A-U7P	1818-1969	8		IC CMOS F16384 (16K) STAT RAM 70NS	S4013	HM6167P
E3,4	1258-0182	7	2	CONNRP IM PLUG	28480	1258-0182

See introduction to this section for ordering information

Table 6-3. List of Manufacturers' Codes

Mfr No.	Manufacturer Name	Address	Zip Code
00000	ANY SATISFACTORY SUPPLIER		
01295	TEXAS INSTR INC SEMICOND CMPNT DIV	DALLAS TX	75222
07263	FAIRCHILD SEMICONDUCTOR DIV	MOUNTAIN VIEW CA	94042
S4013	HITACHI	TOKYO JP	

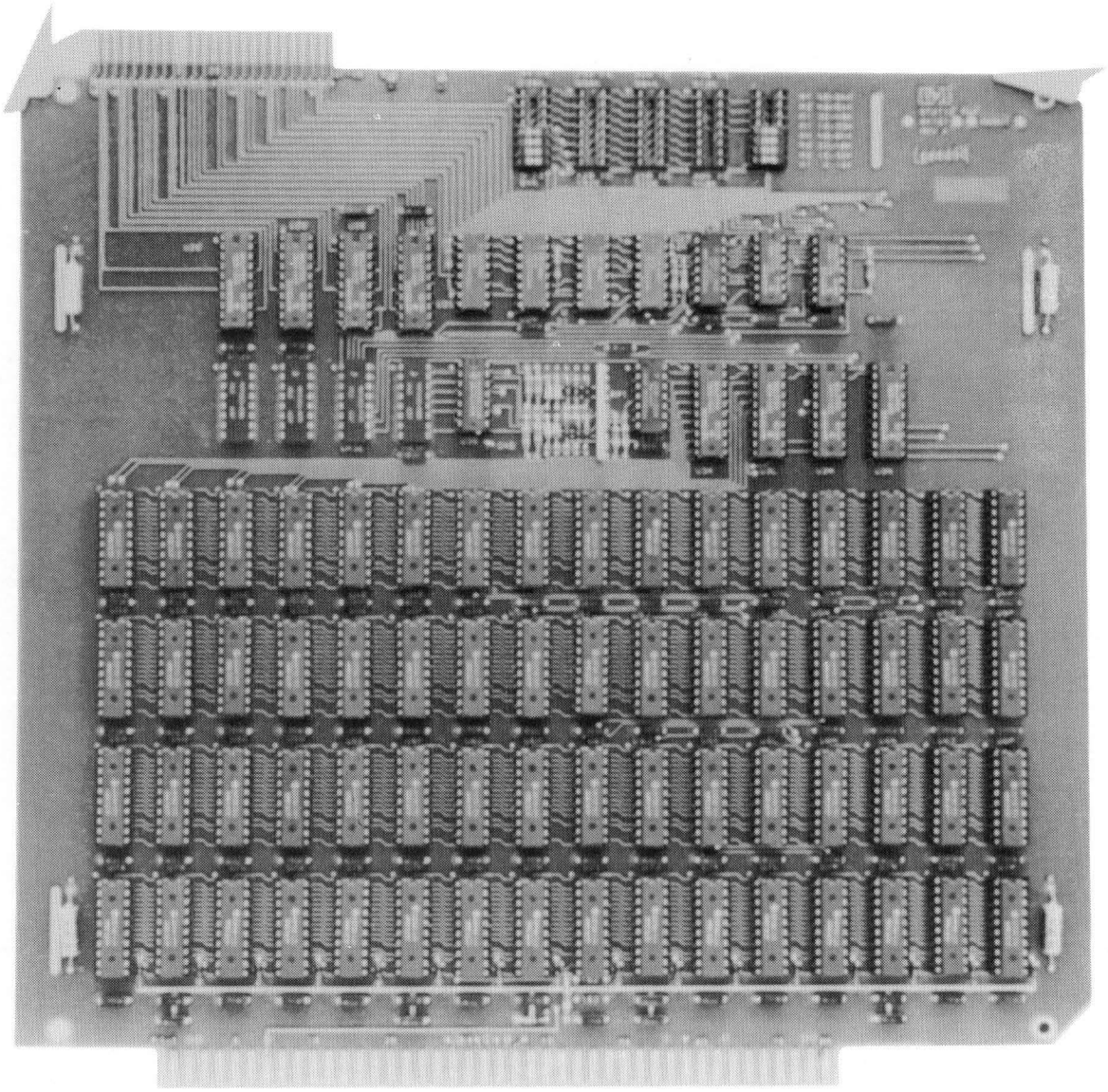


Figure 6-1. Replaceable Parts Locator

SECTION VII

MANUAL CHANGES

This section normally contains information for backdating this manual for models with repair numbers prior to the one shown on the title page. Because this edition includes the information for the first repair number there is no backdating material.

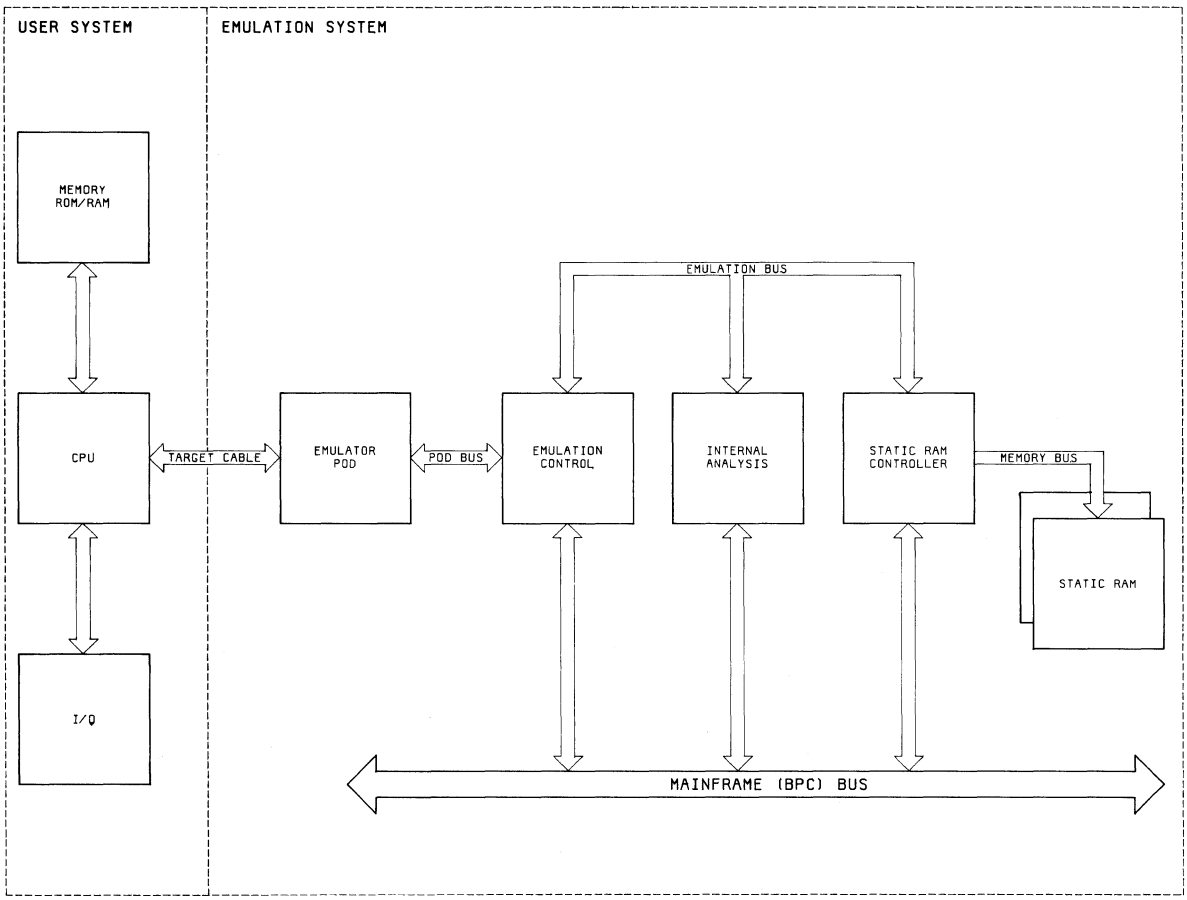


Figure 8-1. Emulation Subsystem

SECTION VIII

THEORY AND SCHEMATICS

8-1. INTRODUCTION.

8-2. This section contains block and component level theory and schematics for the 64161A, 64162A and 64163A Emulation Memories.

8-3. LOGIC CONVENTIONS. The positive logic convention is used for logic variables and circuits within the 64161A/162A/163A. Positive logic defines a "1" as the more positive voltage (high) and a "0" as the move negative logic (low).

8-4. LOGIC LEVELS. TTL high- 2.0 low 0.8

8-5. POWER SUPPLIES. The mainfrome supplies +5 volts and +12 volts to the emulation memory for operating power.

8-6. The block diagram, schematic, component locator, and other service information are provided in foldout service sheets to help in servicing the emulation memory.

8-7. THEORY.

8-8. OVERVIEW.

8-9. The 64000 microprocessor emulation systems, illustrated in figure 1-2, allow software designers to develop and debug software modules for specific microprocessors. The emulation plug replaces the microprocessor physically in the target system permitting hardware in the emulation system to simulate the functions of the target microprocessor while driving target system hardware with the software being developed.

8-10. The emulation memory can be used to duplicate the target system memory. Address space can be allocated to target system EAM, target system ROM, emulation RAM, and emulation ROM, and illegal address space.

8-11. The Memory Controller is the interface between the emulation memory, the installed Emulator, and the 64000 operating system. This option also maps the users address received via the emulation bus into available emulation memory. The mapping process is performed by mapper RAM's which reside on the Memory Controller. A read/write operation to emulation memory is performed via the memory bus.

8-12. The mapper RAM's also output signals which specify what type of memory the given block of emulation memory is supposed simulate (RAM, ROM, or GUARDED Memory), or whether a given address is

to be regarded as user address space and not acted upon. The Memory Controller will also signal the analysis equipment and halt emulation when a GUARDED memory access is attempted and, if optionally configured, when a write to ROM is attempted.

8-13. When the 64161A/162A/163A Memory Boards are installed each Memory Board is hardwired with DIP jumpers to enable a specific memory range so that only one Memory Board will respond to each address.

8-14. The hardware on the Memory Boards simulates address decoder circuitry and some type of memory space which has been defined on the Memory Controller.

8-15. BLOCK THEORY.

8-16. The Model 64161A/162A/163A Block Diagram illustrates the three functional blocks of the memory board: decoder circuitry, address and data buffers, and the memory array. The decoder circuitry specifies the address range of the memory board, decodes the memory rows selected, produces a read enable signal and configures the 64162A and 64163A memory mapping to be compatible with 64152A, 64153A and 64154A memory boards. The address and data buffers drive the signals which are direct inputs to the RAM array.

8-17. U2G through U2J, ROW SELECT DECODERS, demultiplex the upper five address lines A14-A18 to select row numbers of the memory to be accessed. An 8-pin DIP jumper plugged into one of the sockets XE1-XE4 specifies the 64K word addressable range of the memory board.

8-18. The ADDRESS RANGE SELECT JUMPER, XE5 configures the 64162A and 64163A to be compatible with the 64152A, 64153A and 64154A memory boards. If the 64161A, 64162A, or 64163A are not combined with other memory boards an 8-pin DIP jumper should be plugged into the lower half of the socket. Please refer to Section II for complete information on the memory mapping configurations which are possible.

8-19. The network composed of R6-R9 and CR1,2,6,7 deselects the RAM array when the circuitry is powered up. Pulling the circuitry to +12 volts through RP1 brings the voltage in Row 1-4 up quickly when the system is powered on, and the zener diodes CR1,2,6,7 clamp the voltage at approximately +5 volts. This deselection process prevents the RAM array from drawing a large surge of current by putting the RAMs on their low power standby mode.

8-20. Whenever the ROW SELECT DECODERS pull one of the ROWs 1-4 low, the BOARD SELECT GATE, U3GB, produces HRDEN. The READ ENABLE GATE, U3JA, gates LWRT (high) and HRDEN to produce LRD.

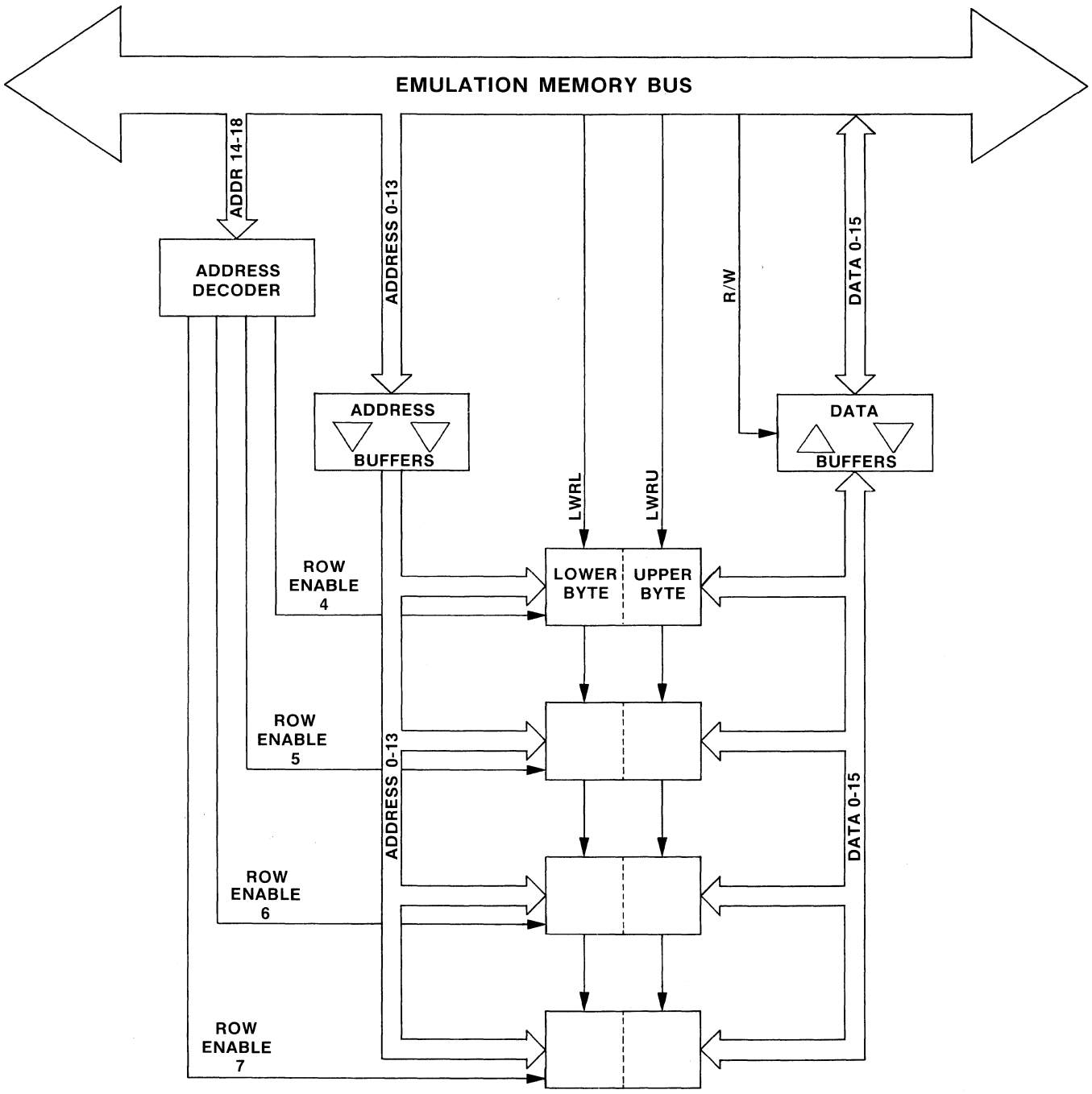


Figure 8-2. Emulation Memory Block Diagram.

8-21. From the Memory Controller on the Emulation Memory Bus the Memory Board receives 19 address lines, 16 data lines and three control lines. The 16 data lines and the lower 14 address lines are buffered through the DATA BUFFERS, U3K-U3N, and the ADDRESS BUFFERS, U2C-U2F, then used as direct inputs to the RAM array. CR11-26 and R12 form a pullup network for the data inputs to the RAMs. This guarantees that the proper voltage levels are applied to the RAM inputs during a write cycle so that correct data is written. LWRT is a directional control for the DATA BUFFERS. LWRL and LWRU enable the lower and/or upper bytes of the RAM array.

8-22. The RAM array consists of an upper byte and a lower byte, which may also be accessed as a single 16-bit word. The Hitachi 6167 16k x 1-bit static Rams feature 70 nsec access time, low power standby mode, low power operation and asynchronous operation.

8-23. Power and ground connections and an 8-bit I.D. signal are the only connections between the memory board and the mainframe. The codes produced by the EMULATION MEMORY BOARD ID CIRCUITRY are listed in Table 8-1.

Table 8-1. Memory Board ID Code.

CODE	# OF ROWS LOADED
01F8	4
01F9	2
01FA	1

8-24. MNEMONICS.

8-25. Signals in the 64161A/162A/163A/162A/163A have been assigned mnemonics which describe the active state and function of the signal line. A prefix letter (H,L, P, OR N) indicates the active state of the signal and the remaining letters indicate its function. An H prefix indicates that the function is active in the high state; an L prefix indicates that it is active in the low state. For devices that are edge sensitive the prefix "P" indicates that the function is active on the positive going edge; the prefix "N" indicates that the device is active on the negative going edge.

TO/FROM MEMORY CONTROLLER

LED0-15 LOW EMULATOR DATA 0-15. Bidirectional bus between the data transceivers (U3K-U3N) and the emulation memory control board. This bus carries all data information for emulation processor and mainframe computer data transactions with emulation memory.

LMA0-18 LOW MEMORY ADDRESS 0-18. Input to the address decoders and the address buffers from the emulation memory controller. These are active low lines. LMA14-LMA18 are input to the address decoders, which select the correct row of RAM for a transaction; and LMA0-13 are input to the address buffers, which drive the address lines of the RAM's to select the desired memory location within the row.

LWRL LOW WRITE LOWER. Input to U2K from the Memory Controller. When low, indicates that the controller wishes to write data into the lower byte of the selected and addressed row of RAM (D0-7), either for an emulation or mainframe computer write cycle.

LWRU LOW WRITE UPPER. Input to U2K from the emulation memory controller. When low, indicates that the controller wishes to write data into the upper byte of RAM (D8-15), either for an emulation or mainframe computer write cycle.

RD/LWRT READ/WRITE. Input from the emulation memory control board to the data buffer control gating and the data transc eiver control logic. A low on this line enables one-half of transceivers U3K-U3N so that data from the emulation memory controller may be driven to the RAM data inputs during a write cycle. When RD/LWRT is high it allows the transceivers to be oriented for a data read cycle whenever a row of RAM is selected on the board.

TO/FROM CPU MAINFRAME

LID LOW ID. Enables Memory Board to output its ID code onto the Low Data Bus to the CPU.

LSEL LOW SLOT SELECT. When low enables the slot select buffer on the mainframe.

LD0-8 LOW DATA 0-8. When low these lines identify the Memory Board to the Mainframe CPU.

01F8	64161A/162A/163A
01F9	64162A
01FA	64163A

LSTB LOW STROBE. Active low, during write operation, indicates data bus information is valid; during read operation indicates CPU is not driving the data bus and addressed device can drive data bus.

INTRABOARD MNEMONICS

A0-13" ADDRESS 0-13". Output from address buffers U2C-U2F, and input to the RAM array. These lines are used to select the desired memory location in the rows 3 and 4 of RAM for the data transfer (read or write cycle).

A0-13' ADDRESS 0-13'. Output from address buffers U2C-U2F, and input to the RAM array. These lines are used to select the desired memory location in the rows 1 and2 of RAM for the data transfer (read or write cycle).

DIN0-15 DATA IN 0-15. Input to the RAM array from data transceivers U3k-3N. This bus is used to provide the desired information for storage in the selected RAM location during a data write cycle.

DOUT0-15 DATA OUT 0-15. Output to the memory bus from the RAM array through data transceivers Ux-Ux. Valid data will be presented on this bus by the selected row of the RAM array whenever a location is addressed, the CS/line is asserted, and the WE/ line of the RAM's is left high.

HRDEN HIGH READ ENABLE. Output generated by U3GB whenever any one of the four rows of memory are selected by the Row Select Decoders. When HRDEN and RD/LWRT are both high U3JA generates a low signal which enables the data transceivers U3K-U3N.

LINVMA18 LOW INVERTED MEMORY ADDRESS 18. When this signal is low (LMA18 is high) and LMA17 is high U2J is enabled; when this signal is low and LMA 17 is low U2I is enabled.

LRD LOW READ. This signal, generated when HRDEN and RD/WRT are both high enables the data transceivers to be read.

ROWSEL1-4 ROW SELECT 1-4. Output from the pullup/damping network (CR1-7 and RP1,R6-9), which is driven by the address decoders through the address range jumpers. A low on one of these lines selects the corresponding row of RAM for a data transaction by asserting the RAM's chip select line.

Table 8-2. Logic Symbols

GENERAL

All signals flow from left to right, relative to the symbol's orientation with inputs on the left side of the symbol, and outputs on the right side of the symbol (the symbol may be reversed if the dependency notation is a single term.)

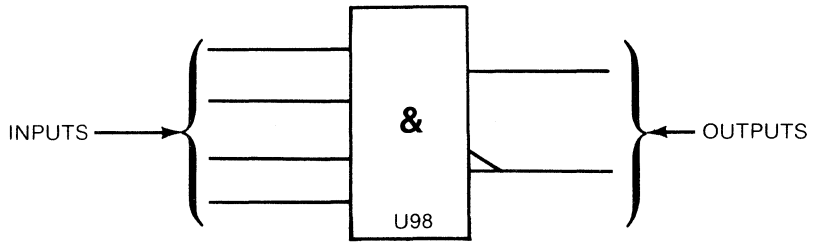
All dependency notation is read from left to right (relative to the symbol's orientation).

An external state is the state of an input or output outside the logic symbol.

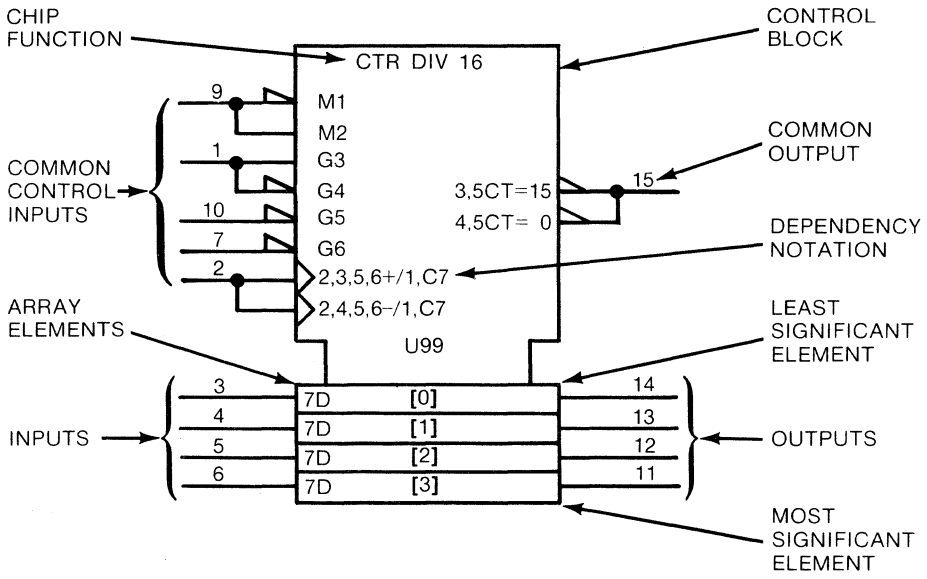
An internal state is the state of an input or output inside the logic symbol. All internal states are True = High.

SYMBOL CONSTRUCTION

Some symbols consist of an outline or combination of outlines together with one or more qualifying symbols, and the representation of input and output lines.



Some have a common Control Block with an array of elements:



CONTROL BLOCK - All inputs and dependency notation affect the array elements directly. Common outputs are located in the control block. (Control blocks may be above or below the array elements.)

ARRAY ELEMENTS -All array elements are controlled by the control block as a function of the dependency notation. Any array element is independent of all other array elements. Unless indicated, the least significant element is always closest to the control block. The array elements are arranged by binary weight. The weights are indicated by powers of 2 (shown in **[ ]**).

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Table 8-2. Logic Symbols (con't)

INPUTS - Inputs are located on the left side of the symbol and are affected by their dependency notation.

Common control inputs are located in the control block and control the inputs/outputs to the array elements according to the dependency notation.

Inputs to the array elements are located with the corresponding array element with the least significant element closest to the control block.

OUTPUTS - Outputs are located on the right side of the symbol and are effected by their dependency notation.

Common control outputs are located in the control block.

Outputs of array elements are located in the corresponding array element with the least significant bit closest to the control block.

CHIP FUNCTION - The labels for chip functions are defined, i.e., CTR - counter, MUX - multiplexer.

DEPENDENCY NOTATION

Dependency notation is always read from left to right relative to the symbol's orientation.

Dependency notation indicates the relationship between inputs, outputs, or inputs and outputs. Signals having a common relationship will have a common number, i.e., C7 and 7D....C7 controls D. Dependency notation 2,3,5,6+/1,C7 is read as when 2 and 3 and 5 and 6 are true, the input will cause the counter to increment by one count....or (/) the input (C7) will control the loading of the input value (7D) into the D flip-flops.

The following types of dependencies are defined:

a. AND (G), OR (V), and Negate (N) denote Boolean relationship between inputs and outputs in any combination.

b. Interconnection (Z) indicates connections inside the symbol.

c. Control (C) identifies a timing input or a clock input of a sequential element and indicates which inputs are controlled by it.

d. Set (S) and Reset (R) specify the internal logic states (outputs) of an RS bistable element when the R or S input stands at its internal 1 state.

e. Enable (EN) identifies an enable input and indicates which inputs and outputs are controlled by it (which outputs can be in their high impedance state).

f. Mode (M) identifies an input that selects the mode of operation of an element and indicates the inputs and outputs depending on that mode.

g. Address (A) identifies the address inputs.

h. Transmission (X) identifies bi-directional inputs and outputs that are connected together when the transmission input is true.

DEPENDENCY NOTATION SYMBOLS

A	Address (selects inputs/outputs) (indicates binary range)	N	Negate (compliments state)
C	Control (permits action)	R	Reset Input
EN	Enable (permits action)	S	Set Input
G	AND (permits action)	V	OR (permits action)
M	Mode (selects action)	Z	Interconnection
		X	Transmission

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Table 8-2. Logic Symbols (con't)

OTHER SYMBOLS

Analog Signal	Inversion	Shift Right (or down)
& AND	O Negation	/ Solidus (allows an input or output to have more than one function)
Bit Grouping	Nonlogic Input/Output	▽ Tri-State
Buffer	Open Circuit (external resistor)	, Causes notation and symbols to effect inputs/outputs in an AND relationship, and to occur in the order read from left to right.
! Compare	Open Circuit (external resistor)	( ) Used for factoring terms using algebraic techniques.
Dynamic	≥1 OR	[ ] Information not defined.
=1 Exclusive OR	Passive Pull Down (internal resistor)	Φ Logic symbol not defined due to complexity.
Hysteresis	Passive Pull Up (internal resistor)	
? Interrogation	Postponed	
— Internal Connection	← Shift Left (or up)	

LABELS

BG	Borrow Generate	CO	Carry Output	J	J Input
BI	Borrow Input	CP	Carry Propagate	K	K Input
BO	Borrow Output	CT	Content	P	Operand
BP	Borrow Propagate	D	Data Input	T	Transition
CG	Carry Generate	E	Extension (input or output)	+	Count Up
CI	Carry Input	F	Function	–	Count Down

MATH FUNCTIONS

Σ	Adder	>	Greater Than
ALU	Arithmetic Logic Unit	<	Less Than
COMP	Comparator	CPG	Look Ahead Carry Generator
DIV	Divide By	π	Multiplier
=	Equal To	P-Q	Subtractor

CHIP FUNCTIONS

BCD	Binary Coded Decimal	DIR	Directional	RAM	Random Access Memory
BIN	Binary	DMUX	Demultiplexer	RCVR	Line Receiver
BUF	Buffer	FF	Flip-Flop	ROM	Read Only Memory
CTR	Counter	MUX	Multiplexer	SEG	Segment
DEC	Decimal	OCT	Octal	SRG	Shift Register

DELAY and MULTIVIBRATORS

	Astable
100 ns	Delay
1	Nonretriggerable Monostable
NV	Nonvolatile
	Retriggerable Monostable

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Table 8-3. Schematic Diagram Notes

ETCHED CIRCUIT BOARD

FRONT PANEL MARKING

REAR-PANEL MARKING

MANUAL CONTROL

SCREWDRIVER ADJUSTMENT

TP1 ELECTRICAL TEST POINT TP (WITH NUMBER)

1 NUMBERED WAVEFORM NUMBER CORRESPONDS TO ELECTRICAL TEST POINT NO.

A LETTERED TEST POINT NO MEASUREMENT AID PROVIDED

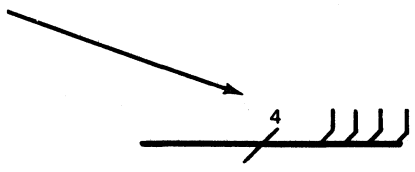
A COMMON CONNECTIONS. ALL LIKE-DESIGNATED POINTS ARE CONNECTED.

1 3 NUMBER ON WHITE BACKGROUND = OFF-PAGE CONNECTION. LARGE NUMBER ADJACENT = SERVICE SHEET NUMBER FOR OFF-PAGE CONNECTION.

A CIRCLED LETTER = OFF-PAGE CONNECTION BETWEEN PAGES OF SAME SERVICE SHEET.

INDICATES SINGLE SIGNAL LINE

NUMBER OF LINES ON A BUS



(925) WIRE COLORS ARE GIVEN BY NUMBERS IN PARENTHESES USING THE RESISTOR COLOR CODE

[(925) IS WHT-RED-GRN]

0 - BLACK	5 - GREEN
1 - BROWN	6 - BLUE
2 - RED	7 - VIOLET
3 - ORANGE	8 - GRAY
4 - YELLOW	9 - WHITE

* OPTIMUM VALUE SELECTED AT FACTORY, TYPICAL VALUE SHOWN; PART MAY HAVE BEEN OMITTED.

UNLESS OTHERWISE INDICATED:
RESISTANCE IN OHMS
CAPACITANCE IN PICOFARADS
INDUCTANCE IN MICROHENRIES

μP	=	MICROPROCESSOR
P/O	=	PART OF
NC	=	NO CONNECTION
CW	=	CLOCKWISE END OF VARIABLE RESISTOR

STD-20-09-81

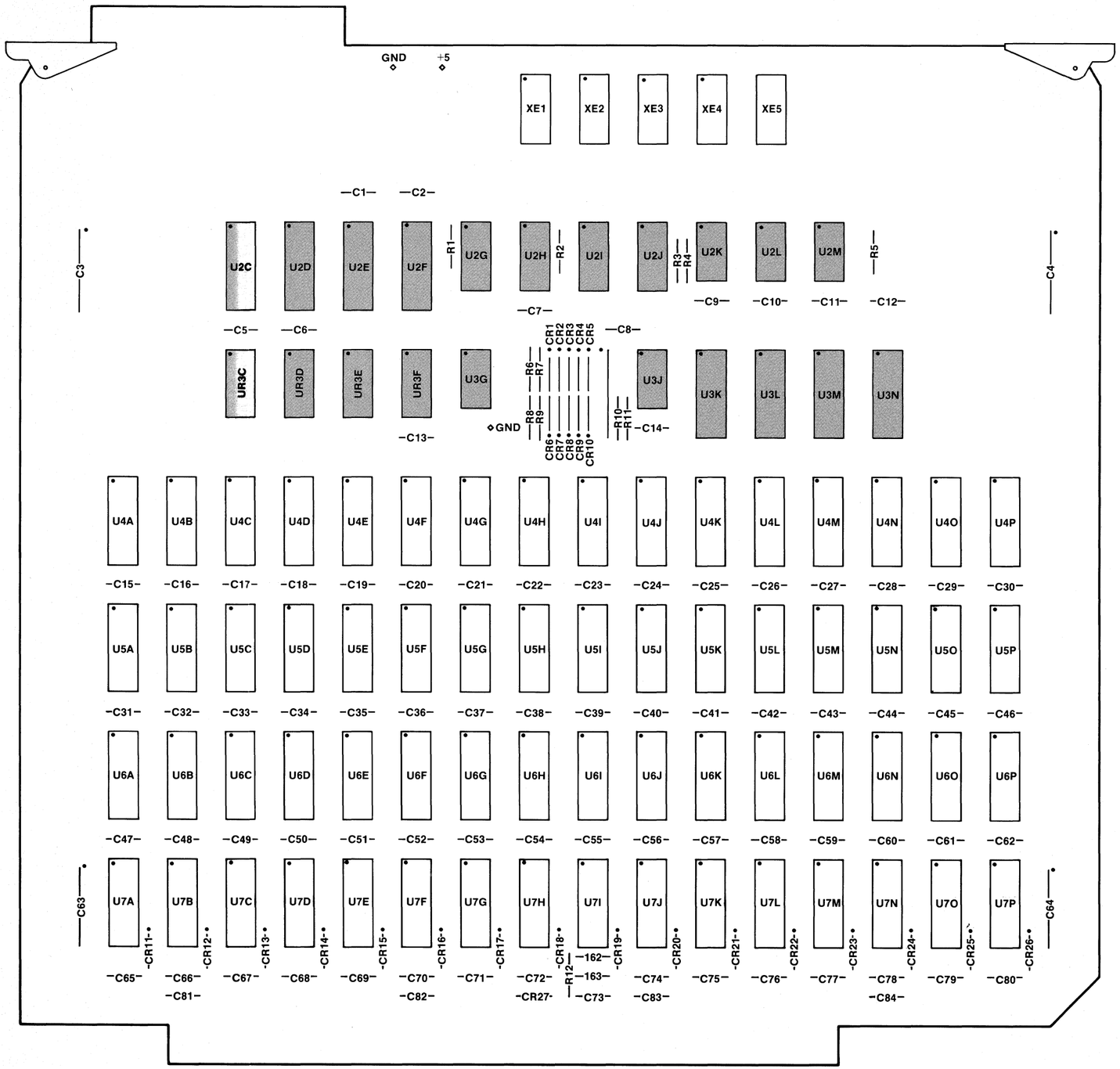
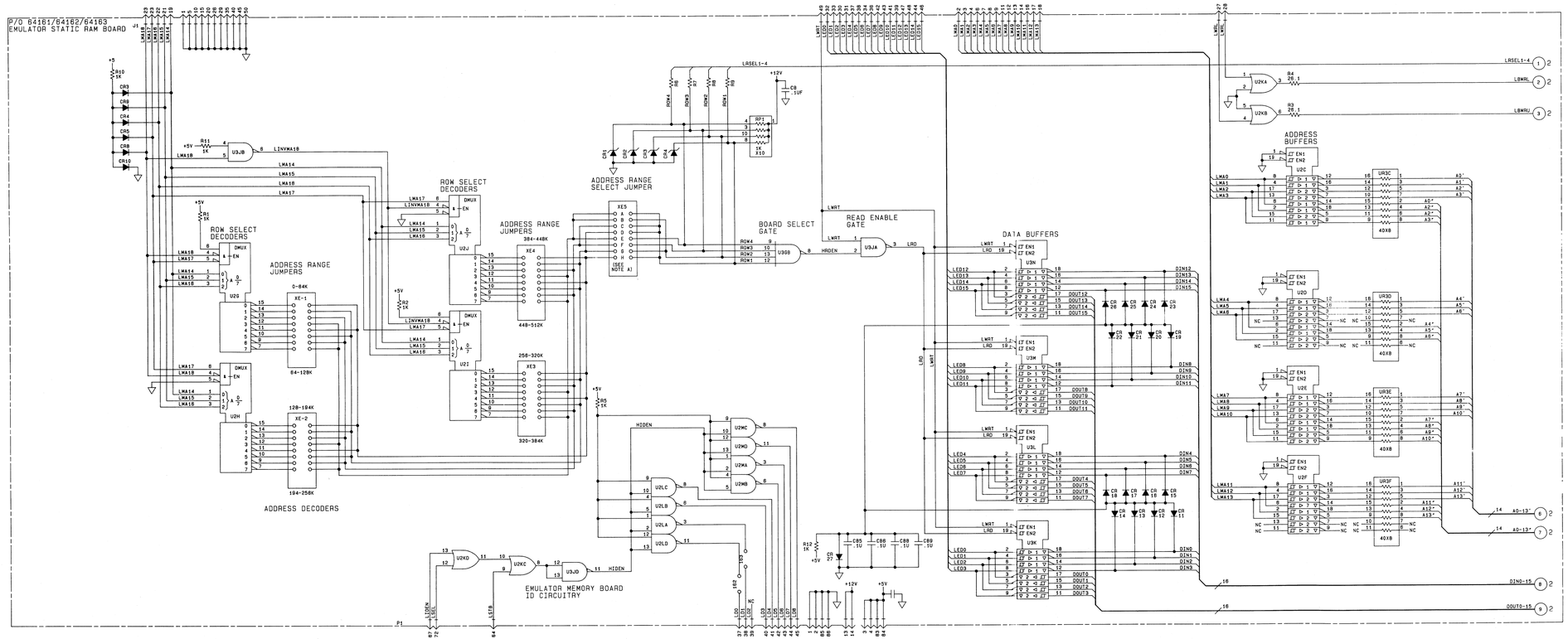


Figure 8-3. Model 64161A/162A/163A Component Locator



IC'S ON THIS SCHEMATIC

U2G-U2J	74F138	1820-2861
U2K	74LS03	1820-1198
U2L-U2M	74F32	1820-2690
U3G	74LS20	1820-1204
U3J	74F00	1820-2684
U2C-U2F	74S240	1820-1633
U3J	74F00	1820-2684
U3K-U3N	74S240	1820-1633

PARTS ON THIS SCHEMATIC

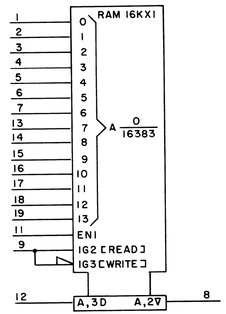
R1-R9, R11, RP1, CR1-CR9

+5V 16 8 U2G-U2J

+5V 14 7 U2K, U2L-U2M, U3G, U3J

+5V 14 7 U3J

+5V 20 10 U2C-U2F, U3K-U3N



NOTE A

A=row 1 48-64K
B=row 2 48-64K
C=row 3 32-48K
D=row 1 16-32K
E=row 4 48-64K
F=row 3 32-48K
G=row 2 16-32K
H=row 1 0-16K

Figure 8-4. Service Sheet 1

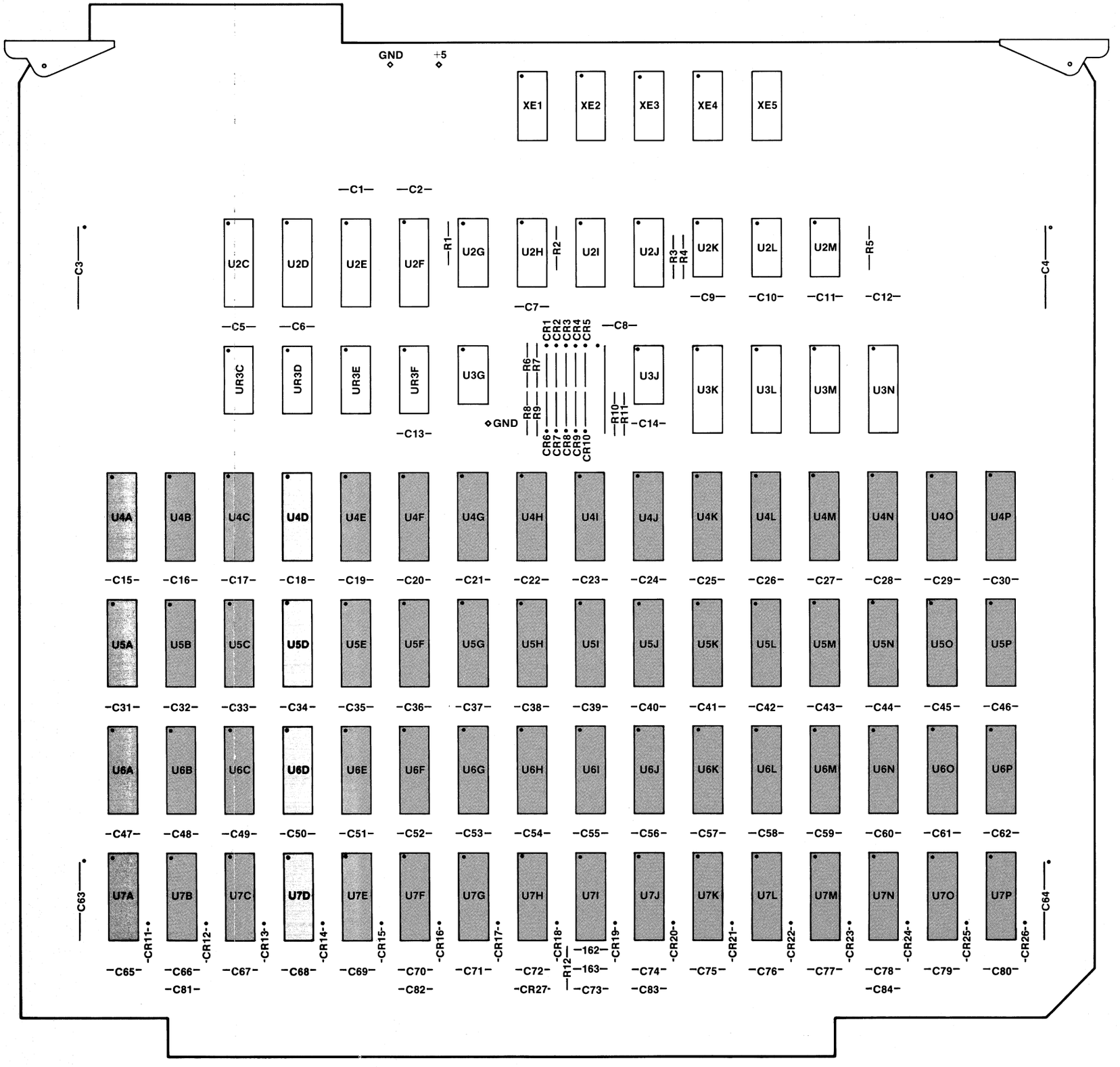
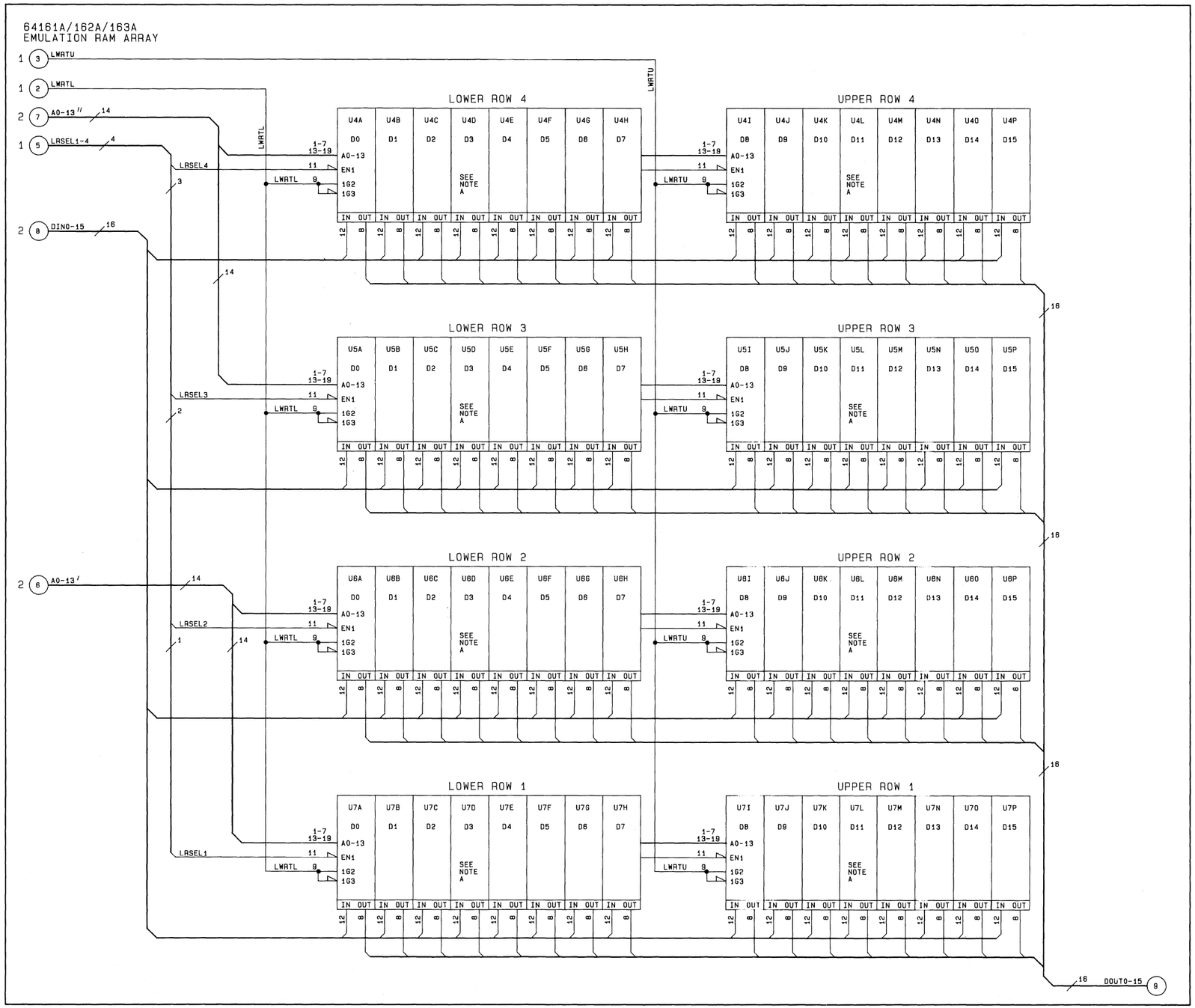


Figure 8-5. Model 64161A/162A/163A Component Locator



IC'S ON THIS SCHEMATIC

U4A-U4P	HM6167	1818-1969
U5A-U5P	HM6167	1818-1969
U6A-U6P	HM6167	1818-1969
U7A-U7P	HM6167	1818-1969

PARTS ON THIS SCHEMATIC

CR15-30, CR31-46, CR47-62, CR65-84

+5V 20 10 U4A-U4P, U5A-U5P, U6A-U6P, U7A-U7P

Figure 8-6. Service Sheet 2

64161-90901, JANUARY 1984
Replaces: 64161-90901, October 1982

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