64000

HP64000 Logic Development System

Model 64100A Mainframe Service Manual

CERTIFICATION

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

WARRANTY

This Hewlett-Packard system product is warranted against defects in materials and workmanship for a period of 90 days from date of installation. During the warranty period, HP will, at its options, either repair or replace products which prove to be defective.

Warranty service of this product will be performed at Buyer's facility at no charge within HP service travel areas. Outside HP service travel areas, warranty service will be performed at Buyer's facility only upon HP's prior agreement and Buyer shall pay HP's round trip travel expenses. In all other cases, products must be returned to a service facility designated by HP.

For products returned to HP for warranty service. Buyer shall prepay shipping charges to HP and HP shall pay shipping charges to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to HP from another country.

HP warrants that its software and firmware designated by HP for use with an instrument will execute its programming instructions when properly installed on that instrument. HP does not warrant that the operation of the instrument, or software, or firmware will be uninterrupted or error free.

LIMITATION OF WARRANTY

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside of the environmental specifications for the product, or improper site preparation or maintenance.

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ASSISTANCE

Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products.

For any assistance, contact your nearest Hewlett-Packard Sales and Service Office. Addresses are provided at the back of this manual.

CW&A 2/81

SERVICE MANUAL

MODEL 64100A

MAINFRAME

SERIAL NUMBERS

This manual applies directly to MAINFRAMES with serial numbers prefixed 2336A.

Manual Part No. 64100-90910
Microfiche Part No. 64100-90810

PRINTED: DECEMBER 1983

SAFETY SUMMARY

The following general safety precautions must be observed during all phases of operation, service, and repair of this instrument. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the instrument. Hewlett-Packard Company assumes no liability for the customer's failure to comply with these requirements.

GROUND THE INSTRUMENT.

To minimize shock hazard, the instrument chassis and cabinet must be connected to an electrical ground. The instrument is equipped with a three-conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE.

Do not operate the instrument in the presence of flammable gases or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS.

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE.

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

USE CAUTION WHEN EXPOSING OR HANDLING THE CRT.

Breakage of the Cathode-ray Tube (CRT) causes a high-velocity scattering of glass fragments (implosion). To prevent CRT implosion, avoid rough handling or jarring of the instrument. Handling of the CRT shall be done only by qualified maintenance personnel using approved safety mask and gloves.

DO NOT SUBSTITUTE PARTS OR MODIFY INSTRUMENT.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification of the instrument. Return the instrument to a Hewlett-Packard Sales and Service Office for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

Dangerous voltages, capable of causing death, are present in this instrument. Use extreme caution when handling, testing, and adjusting.

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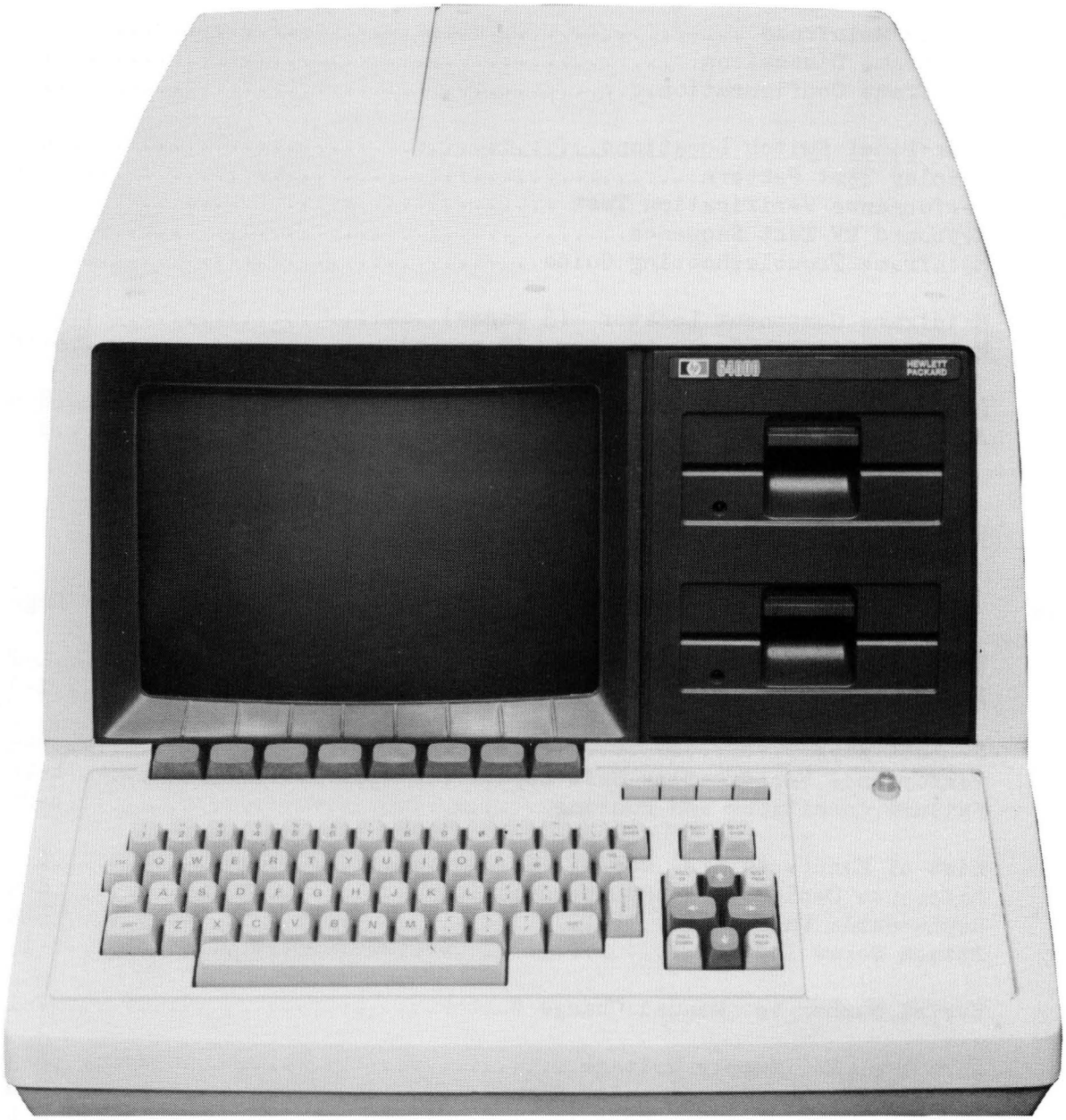

Figure 1-1. 64100A Mainframe.

SECTION I

GENERAL INFORMATION

1-1. MANUAL INTRODUCTION.

1-2. This manual contains technical information to troubleshoot, install, and maintain the 64100A Logic Development Station. Each of the five chapters (Mainframe, CPU, Display Controller, I/O, and Power Supply) is seperated by a Tab. This allows the user to easily find any chapter.

1-3. Each of the five chapters is organized into eight sections: Section I introduces the reader to the manual and gives a brief physical description of the product. Section II presents the installation and removal procedures for the system components. Section III covers operation and handling. Section IV describes how to troubleshoot and repair the system. Section V references those components that have adjustments. Section VI lists the replaceable parts and Section VII contains backdating information needed to make this manual applicable to older machines. Section VIII presents the theory-of-operation to the block diagram level and is intended to support the troubleshooting procedures.

1-4. CHAPTER INTRODUCTION.

1-5. This chapter contains technical information concerning the installation, maintenance, troubleshooting and theory-of-operation of the 64100A Mainframe. The information contained in the Mainframe Chapter describes the overall system and how the various components relate to each other with the emphasis on troubleshooting and repairing. More detailed information on the components can be found under the respective Chapter or the component in question (i.e., CPU, DISPLAY CONTROLLER and DRIVER, I/O, POWER SUPPLY, and OPTIONS).

1-6. PHYSICAL DESCRIPTION.

1-7. The 64100A Mainframe is a single enclosure similar to a CRT terminal (see figure 1-1). It weighs 34.02 Kg (75 pounds) and thus some care should be used in moving it. The Mainframe dimensions are given in figure 1-2. The five major areas of the developement station mainframe are:

a. CRT Display
b. Keyboard
c. Rear Panel
d. Card Cage
e. Power Supply

1-8. The four areas of display generation consist of the display controller board, display driver, the CRT and CRT bezel assembly.

1-9. The four areas of the Rear panel are Power Control, HP-IB system interface bus, RS-232 serial interface, and system control source. The power functions are on the lower right-hand side of the rear panel. The model 64100A requires 110/220 VAC +/-15%, 48-66 HZ. The position of the LINE SELECTOR determines either 110 V (10 AT fuse) or 220 V (5 AT fuse) operation. The power ON/OFF switch is a rocker type.

1-10. A card cable opening is provided to the outside of the mainframe through the space between the rear of the top cover and rear panel. Three slots with clamps are provided for access. Cable length for option boards is determined at the factory and are shipped at maximum length.

1-11. There are 13 PC board slots (see figure 1-3). The first three slots have printed circuit boards installed at the factory. These PC boards must be installed in the order given for the 64000 system to operate. The three required boards are:

slot A - I/O PC Board
slot B - Display Control PC Board
slot C - CPU PC Board

1-12. For convenience, board identifier labels for the first three boards are located just above the cardcage on the left-hand side. The remaining ten option slots are numbered 0-9.

1-13. The PC boards interface to the system through the motherboard on the bottom of the card cage. A cable from the Rear Panel PC board (on the rear panel) makes connection to the top center connector on the I/O board.

1-14. There is a limit to the number and types of option boards that may be installed in the cardcage without exceeding the capability of the 400 watt Power Supply. This limit is determined by the amount of available current from the power supplies. Table 1-1 lists the power supply current drain for the mainframe with only the three mandatory boards installed.

Table 1-1. Basic Power Supply Current Drain

(NO OPTIONS INSTALLED)

ITEM	+12V	+5V	-5V	-12V	-3V
Processor,ROM	0.595	1.429	0.0003		0.0003
I/O	0.164	0.708		0.078	
Disp Control,RAM	0.640	1.533	0.0064		0.0064
Keyboard			0.239		0.239
Display Driver	1.500	0.100			
Rear Panel		0.714			
Bus Pullups		0.070			
Subtotal	2.899	4.793	0.2457	0.078	0.2457
Available Current	4 Amps	45 Amps	25 Amps	1 Amp	30 Amps

1-15. SPECIFICATIONS.

1-16. The environmental specifications and power requirements for the 64100A Mainframe are supplied in Table 1-2.

Table 1-2. Power and Environmental Requirements

ITEM	OPERATING REQUIREMENTS
Line Voltage	110/220, + or - 15% Single Phase
Line Frequency	50/60 Hz +15% or -10%
Operating Temperature	0 Deg C (32 Deg F) to 40 Deg C (104 Deg F)
Operating Humidity	0% to 80% RH, non-condensing (max wet bulb temp: 26 Deg C (78 Deg F)
Power Outlets:	
US, Canada, Japan	NEMA 5-15 (15A)
UK	BS 1363 (13A)
Australia, New Zealand	AS C112 (7-5A)
Europe (except UK and Switzerland)	CEE 7-V11 (10/16A)
Switzerland	SEV 1011 (10A)

1-17. INSTRUMENTS COVERED BY THIS MANUAL.

1-18. Attached to the instrument is a serial number plate. The serial number is in the form: 0000A 00000. It is in two parts; the first four digits and the letter are the serial prefix and the last five digits are the suffix. The prefix is the same for all identical instruments; it changes only when a change is made to the instrument. However, the suffix is assigned sequentially and is different for each instrument. The contents of this manual apply to instruments with serial number prefix(es) listed under SERIAL NUMBERS on the title page.

1-19. An instrument manufactured after the printing of this manual may have a serial number prefix that is not listed on the title page. This unlisted serial number prefix indicates the instrument is different from those described in this manual. The manual for this modified instrument is accompanied by a yellow Manual Changes supplement. the supplement contains "change information" that explains how to adapt the manual to the newer instrument.

1-20. In addition to change information, the supplement may contain information for correcting errors in the manual. To keep this manual as current and accurate as possible, Hewlett-Packard recommends that you periodically request the latest Manual Changes supplement. The supplement for this manual is identified with the manual print date and part number, both of which appear on the manual title page.

1-21. For information concerning a serial number prefix that is not listed on the title page or in the Manual Changes supplement, contact your nearest Hewlett-Packard Sales/Service Office.

1-22 RELATED DOCUMENTS.

1-23. The following documents provide additional information pertaining to the use of the HP 64000 system. It is recommended that the System Overview Manual be referenced first.

System Overview Manual

System Software Reference Manual

Installation and Configuration Manual

Editor Manual

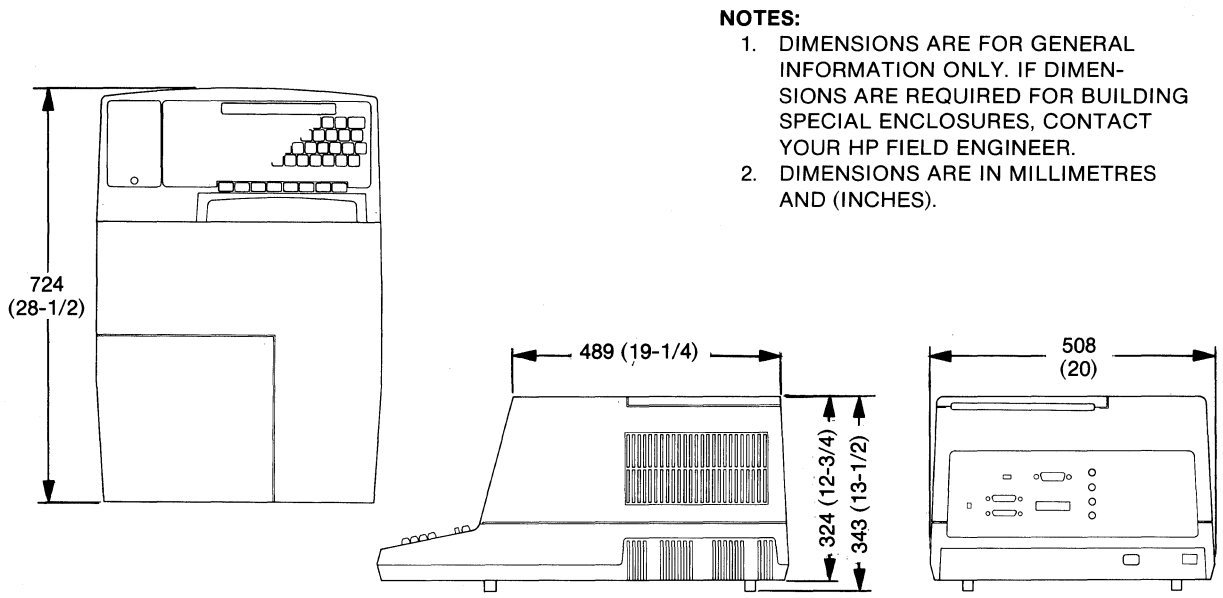

Figure 1-2. Mainframe Dimensions

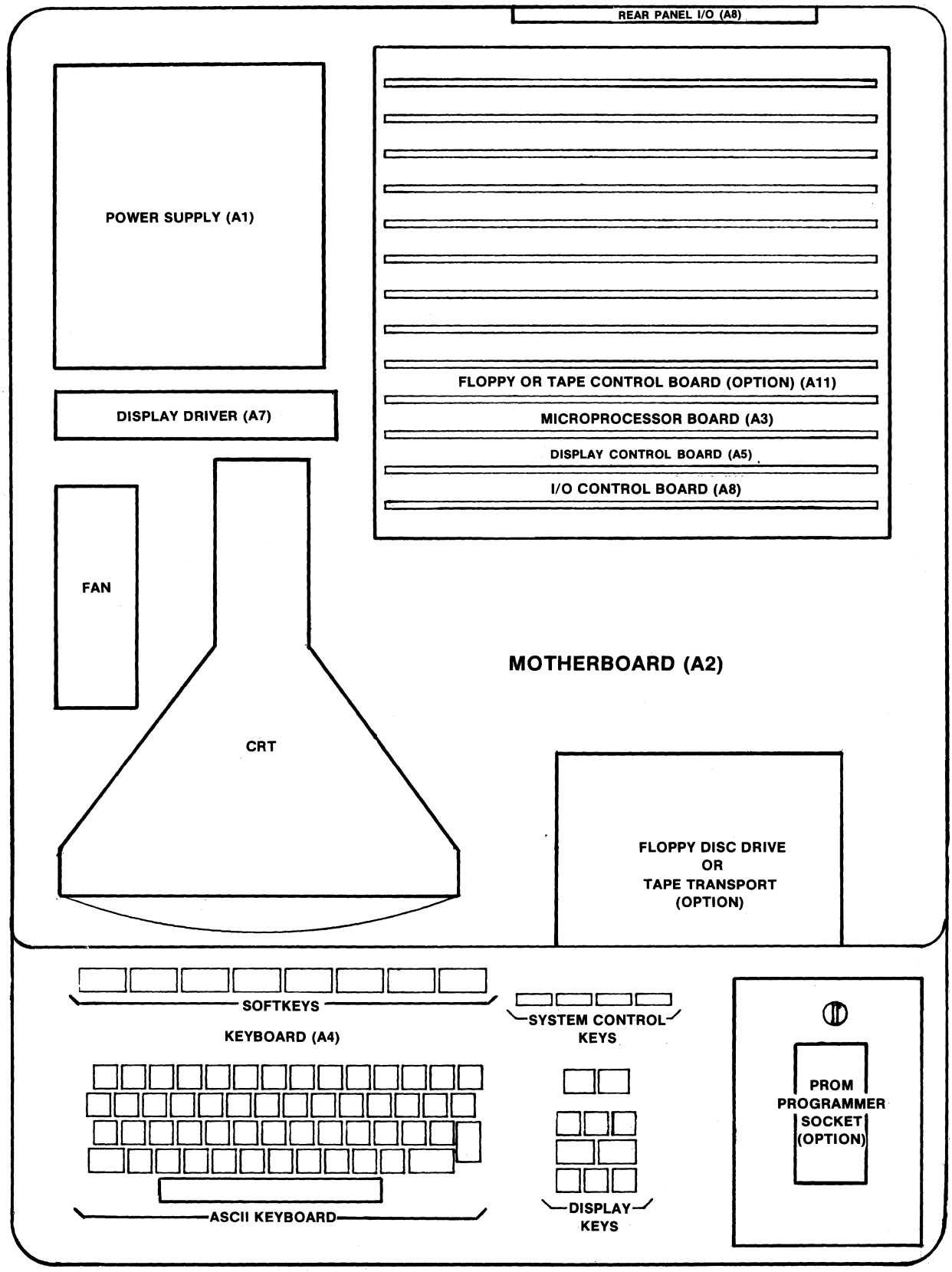

Figure 1-3. Mainframe Configuration

SECTION II

INSTALLATION

2-1. INTRODUCTION.

2-2. This section contains information for unpacking, initial inspection, and installation and removal of the model 64100A mainframe components. For more information refer to paragraph 1-20 (related documents) for more information on installation and site selection instructions.

2-3. INITIAL INSPECTION.

a. Unpack the mainframe.

b. Keep the shipping carton and cushioning material until the contents have been checked. The carrier will want to inspect the shipping materials if a claim is made.

c. Check the mainframe mechanically and electrically. The electrical performance verification is given in Section IV. For initial inspection, the "CYCLE" softkey selection should be used.

d. If the contents are not complete, there is mechanical damage or defect, or it does not pass the performance verification test then notify the carrier as well as the Hewlett-Packard Sales/Service Office. They will arrange for repair or replacement at HP option without waiting for the claim against the carrier to be settled.

2-4. PACKAGING.

2-5. ORIGINAL PACKAGING.

2-6. Containers and packing materials identical to those used in factory packaging are available through Hewlett-Packard Sales/Service Offices.

2-7. OTHER PACKAGING

2-8. The following general instructions should be used for repacking with commercially available materials:

a. Wrap the Model 64100A in heavy paper or plastic.

b. Use a strong shipping container. A double-wall carton made of 350-pound test material is adequate.

c. Use a layer of shock-absorbing material 70 to 100 mm (3 to 4 in) thick around all sides of the 64100A to provide firm cushioning and prevent movement inside the container.

d. Seal shipping container securely.

e. Mark shipping container FRAGILE to ensure careful handling.

f. In any correspondence, refer to the instrument by model number and full serial number.

2-9. INSTALLATION AND REMOVAL OF THE MAINFRAME COMPONENTS.

2-10. This section contains the installation and removal instructions for the Mainframe components excluding the Power Supply, CPU PC board, I/O PC board, Display Controller PC board, and the Display Driver PC board. The installation and removal instructions for these components are contained in Section II of the respective service tabs for these items.

2-11. The removal and installation of Mainframe components is straight-forward since the mounting/attach scheme for the various components is obvious. As an aid, however, the number location and purpose of the mounting screws are shown in figure 6-2, sheets 1 through 7.

SECTION III

OPERATION

3-1. GENERAL.

3-2. Refer to paragraph 1-20 (related documents) for information on operating instructions for the Mainframe.

SECTION IV

PERFORMANCE VERIFICATION

4-1. INTRODUCTION.

4-2. This section describes the use of mainframe Performance Verification (PV), self test on Power-Up, Boot-Up and the use of PV, and troubleshooting PV using Signature Analysis (SA).

4-3. Performance Verification (PV) is a series of tests, resident in the mainframe, that confirm the operation of the mainframe hardware and firmware. PV can be initiated at any time via the Rear-Panel switches or keyboard as explained in Performance Verification Boot procedure.

NOTE

PV can also be initiated from the Front Panel when a boot is from a hard disc or floppy disc if the operating system software has been loaded. To do this press the CNTL and RESET keys together. For more information, see section IV under System Chapter.

4-4. BOOY-UP MODES.

4-5. The mainframe Boot-Up mode is determined by the position of the control source switches on the Rear-Panel. The display at completion, with no errors, is determined by the boot source. The four control source options are described in this section.

BIT 1	BIT 0	CONTROL SOURCE
1	1	PERFORMANCE VERIFICATION
1	0	LOCAL MASS STORAGE ADDRESSABLE
0	1	LOCAL MASS STORAGE TALK ONLY
0	0	SYSTEM BUS

NOTE

If the rear panel switches are set to "PERFORMANCE VERIFICATION", the system will boot up with the performance verification display test pattern appearing on the CRT. However, if the source switches are set to either of the "LOCAL MASS STORAGE" modes and the self test sequence was initiated, the display will read "SELF TEST COMPLETE". If the switches are in the "SYSTEM BUS" mode, the boot is from hard disc. Then, the system bus configuration will be displayed if a disc is properly connected on the system bus.

4-6. POWER-UP SEQUENCE.

4-7. The 64100A Mainframe executes a Power On ROM and RAM test every time the mainframe does a power on boot. The definition of a Power On Boot is when the power has been removed, or cycled. However, there are four other actions that will cause a boot sequence. These are: 1) pressing the SHIFT and RESET key together, 2) when the auto reset circuitry on the I/O board generates a Low Power ON Pulse (LPOP), 3) pressing the END TESTS key during PV, and 4) if the operator presses the processor reset switch located on the I/O board. The beeper is used to indicate the successful completion of certain tests upon power-up. The sequence is as follows:

a. BEEP - hardware initiated - Happens on Power On Boot only. Does not happen when the SHIFT and RESET keys are pressed together. or the END TESTS softkey is pressed.

b. BEEP - software initiated - After initialization sequence, the display is also enabled.

c. BEEP BEEP BEEP - ROM test completed (approximately a 7 second delay before the next beep sequence).

d. BEEP BEEP - successful completion of RAM test.

NOTE

The 64100A now boots up according to boot switch configuration. If the ROM or RAM test fails upon power up, a signature analysis loop is automatically entered for troubleshooting purposes. This will be indicated by a RAM or ROM errror message on the screen.

4-8. Upon power up, the following sequence of events occur under software Controll.

a. The operating system software checks for Power-On or cycled power by reading a reseverved location in RAM.

b. CRT controller chip (U33) is initialized.

c. Blank the screen.

d. ROM test is initiated; a failing ROM address range and byte will be displayed if the test fails.

e. RAM test is initiated; if a failure occurs an SA loop is entered and the failing RAM IC number is displayed. NOTE: The display may be unreadable due to a display RAM failure. If this occurs then go to the Display tab, section IV, SA loop E to troubleshoot.

f. Read rear panel dipswitches and boot accordingly.

4-9. POWER-UP ROM TEST.

Purpose:
The ROM test verifies that all of the firmware in ROM used for boot-up and performance verification is good. The test also checks that the CPU is able to access ROM memory via the bi-directional address and data busses.

Area Tested:
All ROMs, the multiplexed memory Address/Data bus to ROM, the address latches data buffers, the CPU and its associated timing and control circuitry, and the demultiplexed Address/data bus to/from ROM.

Operation:

a. This test executes a checksum on each of the ROMs as long as the kernal of ROM needed to run the test is operational.

b. If an error is detected, then a bit is set in an error mask.

c. The error mask is then used to output an error message to the screen: stating a ROM failure, the address range of the failure, and the byte (0 or 1).

d. If a failure is detected, the test will loop continuously. See CPU section IV for more information.

e. On failures, the power up ROM test will display the following error message assuming that the kernal of ROM required to run the power up test is good:

```
SELF-TEST FAILURE  <-------- [ blinking ]
ROM TEST:
FAILING ADDRESS RANGE        BYTE(S)
--------------------         -------
     XXXX-XXXX                  XX
```

f. Use the table below to determine which ROM unit number is failing. Note that the error message might give an address range that includes more than one ROM. SA might be necessary to isolate the fault.

Failed Addresses	Byte	Failed ROM #
0020-1FFF	0	U9
0020-1FFF	1	U10
2000-3BFF	0	U9
2000-3BFF	1	U10

g. When the ROM test passes, the mainframe beeper will sound three times and begin the RAM test.

4-10. POWER-UP RAM TEST.

Purpose:
The RAM test verifies the ability to read and write from the upper 32K of RAM located on the Display Control board and checks refresh. Note that this test occurs only on Power-up. Another RAM test occurs during PV and has a different error message.

Area Tested:
Upper 32K of RAMs including refresh ability, the multiplexed memory Address/Data Bus from the CPU, motherboard connections between the CPU and Display Controller board, the demultiplexed Address/Data bus to/from RAM, and the timing and control circuitry.

Operation:
a. The Power-Up Test is a different test than the one performed during PV.

b. The RAM test takes approximately 7 seconds.

c. All upper 32K RAM locations are toggled to insure READ/WRITE operation.

d. Refresh ability is verified.

e. The operation of the routine is as follows:

1. Load RAM with a count, starting with zero.

2. Read RAM and compare with count.

3. Check for an error. If error occurs go to error sequence.

4. If there is no previous error, wait one second.

5. Read RAM and compare with count.

6. Check for an error. If error occurs go to error sequence.

7. If there is no previous error load RAM with compliment of count, starting at zero.

8. Read RAM and compare with the compliment of the count.

9. Check for an error. If error occurs go to error sequence.

10. If there is no previous error, wait one second.

11. Read RAM and compare with count.

12. Check for an error. If error occurs go to error sequence.

NOTE

If there are no errors in the RAM error mask then the system will beep twice. But, if an error exists then the following error sequence occurs:

1. Reset the delta timer to prevent auto restart.

2. Set the SA latch.

3. Write to and read from all of the upper 32K of RAM.

4. Provide stimulus to CRT controller.

5. Output RAM error display header information (including refresh error message if refresh error flag set).

6. Reset SA latch.

7. Output individual failing unit number for lower 16K RAM.

8. Output individual failing unit number for upper 16K RAM.

g. When a failure occurs, the routine attempts to output an error message as follows:

```
SELF-TEST FAILURE          blinking
RAM TEST:
FAILING UNIT NUMBERS (S)
-------------------------
XY
```

"XY" corresponds to the U# of the failing RAM. Depending on which RAM is failing, the display could be affected. Evidence of this is a random pattern on the CRT or incorrect spelling of messages. For this reason the accuracy of a RAM test failure is always suspect. Because the RAMs are 1 bit wide, 16 of the 32 RAMs are used to store display information. U23-U30 and U38-U45 on the display controller board are used for display memory. Thus, if any of these 16 RAMs is failing, the display will be unintelligible to various degrees. If this occurs see display section IV, SA table E, to troubleshoot the outputs of the RAMs.

4-11. PERFORMANCE VERIFICATION BOOT PROCEDURE.

a. Place the control source switches in the Performance verification position shown on the control source label on the rear panel. See Figure 4-1 for the switch locations.

b. Turn power off and then back on. The display test pattern, figure 4-2, should be on screen after the boot tests. However, there are several steps that occur before the display test pattern is shown.

1. Suspend operation of the PHI chip (U20 on I/O board) and take it off line.
2. Initialize the CRT chip (U33 on Display Control board).
3. Enable the display and sound the beeper once.
4. Disable interrupts.
5. Disable CPU direct memory access.
6. Clear base page RAM (F000- FFFF hex).
7. Set up interrupt vector.
8. Clear keyboard power up interrupts.
9. Clear display screen.
10. Set up and enable keyboard interrupts for display test.
11. move cursor off screen.
12. Determine what local mass storage is present so the correct softkey will appear.

13. Display the softkeys.

SA 14. Start SA interval.

15. Write display test pattern to screen.

16. Enable keyboard interrupts.

17. Toggle I/O data lines.

18. Service the delta time interrupt.

19. Cycle through interrupt masks.

20. Service the delta time interrupt.

21. Read rear panel switches.

22. Write to floppy control board.

23. Toggle all even I/O address lines.

24. Read keyboard.

25. Send "move cursor" commands.

SA 26. Clear SA interval.

27. Read and write from RAM.

28. Read keyboard.

29. Issue an I/O write.

30. Begin SA interval again.

c. After the test pattern is displayed refer to table 4-2 and make the desired softkey selection.

Table 4-1. PV Boot Keys.

PV TESTS	Performance Verification Test - First softkey on the left. Press this softkey to display the performance verification procedures.
DIAG	Diagnostic- Third softkey from the left. Press this softkey to perform the Floppy Disc Diagnostic. Notice, that this softkey will not be shown if a cassette tape option 64100-64940 is installed. Refer to the local mass storage service manual for details on the use of this test.

END TEST — End Test - Eighth softkey from the left. Press this soft key to reboot. Notice that unless the rear panel source switches are in the system bus mode the reboot will be to the display test pattern.

B — Pressing the "B" key causes the mainframe beeper to beep. This indicates that the CPU is able to recognize and process interupts. A failure to beep indicates the CPU is malfunctioning or the I/O or beeper circuitry is faulty.

4-12. PERFORMANCE VERIFICATION PROCEDURE.

4-13. The steps given below will enable the operator to gain access to any of the mainframe performance verification tests.

a. Perform the PV Boot procedure descibed in the previous paragraph.

b. The performance verification menu (figure 4-2) should be displayed at the bottom of the display test pattern. Press the "PV TESTS" softkey.

c. Press "NEXT TEST". Repeat as necessary, until the desired test is displayed in inverse video. The example in figure 4-3 shows that the FLOPPY tests are to be performed.

d. Refer to table 4-2 and make the desired softkey selection.

e. Press "END TEST" to exit the PV tests.

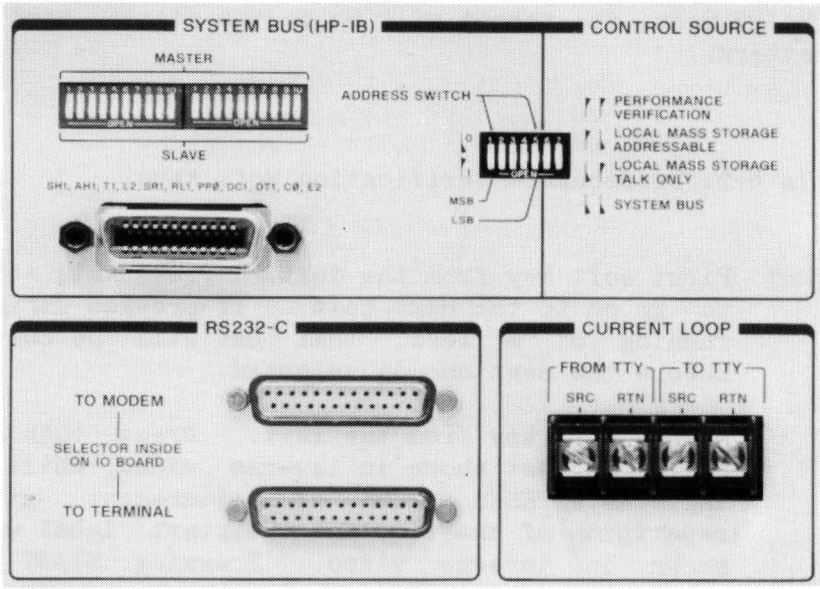

Figure 4-1. Rear Panel Switch Locations.

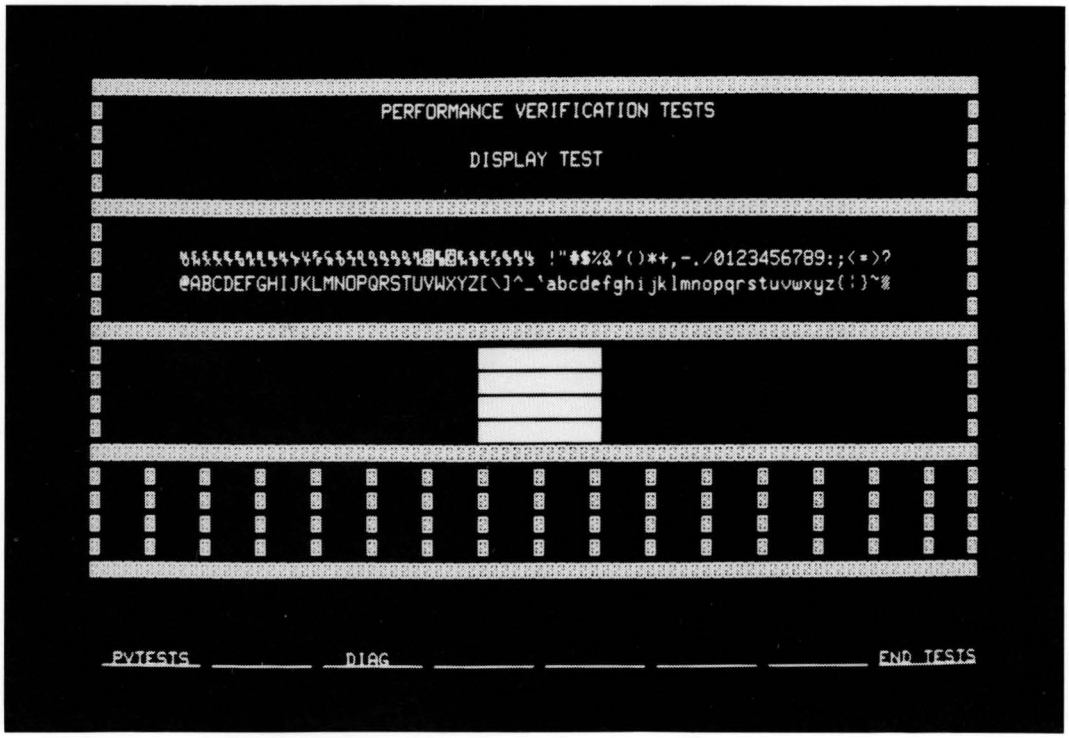

Figure 4-2. Display Test Pattern.

NOTE

If the rear panel control source switches are in the PV mode, the reboot will be to the display test pattern.

Table 4-2. Performance Verification Soft Keys.

NEXT TEST	First soft key from the left. Press this soft key to go on to the next test. If pressed during the running of a test, that test will be completed before the next one is selected.
START	second soft key from the left. Press this key to begin the test shown in inverse video. While running, the # TESTS column will increment at each repetition of the test and the start label will be shown in inverse video. Pressing START while executing a test causes the test to complete and then stop.
CYCLE	third softkey from the left. Press this soft key to cycle through all tests, except the keyboard test. This is recommended as an initial test.
DISPLAY	fourth softkey from the left. Press this soft key to return to the display test pattern. If pressed during the running of a test, the system returns to the test pattern after completion of that test.
END TESTS	fifth softkey from the left. Press this key to reboot. If pressed during a test, the finishes and then rebooting occurs.

NOTES 1) If the configuration source switches are unaltered the reboot will be back to the display test pattern.

2) The key being pressed is displayed in the lower left corner as: Key Down="X"

4-14. The following performance verification procedures allow the operator to verify all operations of the 64100A Logic System mainframe. Portions of the performance verification tests are used in conjunction with the signature analysis and troubleshooting in section IV of the appropriate manual.

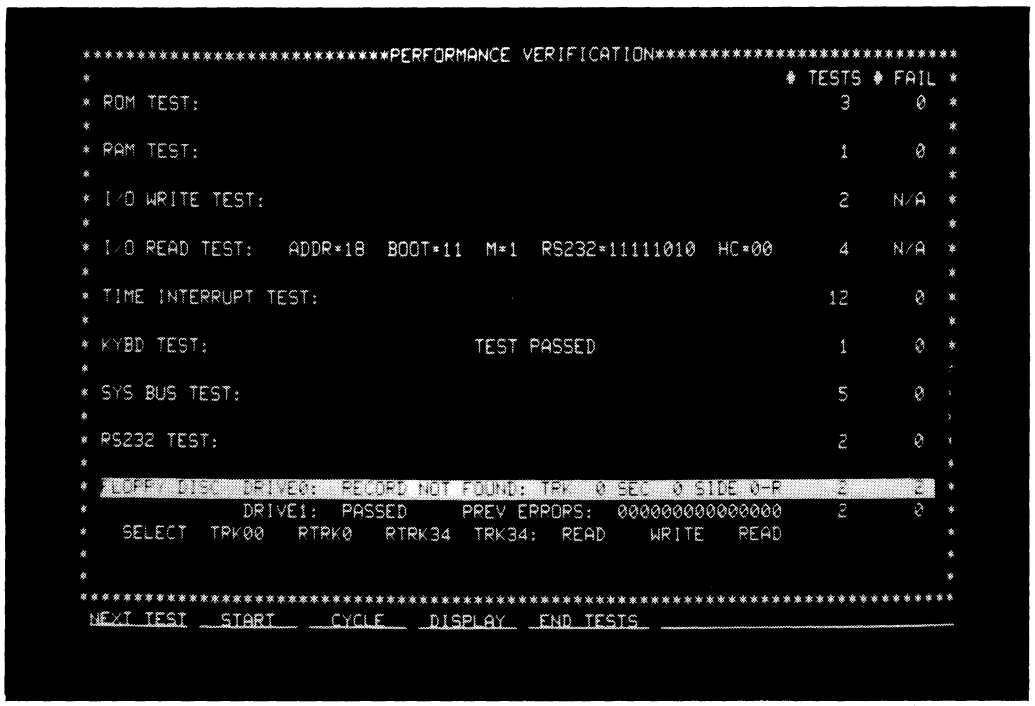

Figure 4-3. Performance Verification Test.

4-15. ROM TEST PROCEDURE.

Purpose:

The ROM test verifies that all of the firmware in ROM used for boot-up and performance verification is good. The test also checks that the CPU is able to access ROM memory via the bi-directional address and data busses.

Area Tested:

All ROMs, the multiplexed memory Address/Data bus to ROM, the address latches data buffers, the CPU and its associated timing and control circuitry, and the demultiplexed Address/data bus to/from ROM.

Operation:

a. This test is simialar to the ROM test which is performed during power up. Although, there is a different error message.

b. Each test takes approximately 1/2 second.

c. A routine reads the ROM contents, computes a checksum and compares it with a checksum also located in ROM.

d. See CPU section IV for more information about this test.

e. Assuming that the kernal of ROM required to run the ROM TEST is operating, the test will attempt to output an error mask if the test fails. The mask is a 16 bit word as follows:

```
IC MASK = 000000000000ABCD
          15--------------0
```

A "1" in any of the bits signifies a bad ROM where:

D = ROM # 0 = lower byte of lower 8K of ROM (U9)
C = ROM # 1 = upper byte of lower 8K of ROM (U10)
B = ROM # 0 = lower byte of upper 8K of ROM (U9)
A = ROM # 1 = upper byte of upper 8K of ROM (U10)

f. Note that the error message might give an address range that includes more than one ROM. SA might be necessary to isolate the fault.

4-16. RAM TESTS.

4-17. POWER-UP RAM TEST.

Purpose:

This RAM test verifies the ability to read and write from the upper 32K x 16 locations of RAM (address 8002 HEX thru FFFF HEX) located on the Display Controller board. Note that this test occurs only on power up. The lower 32K x 16 locations of RAM (memory mapped address 4000 HEX thru 7FFF HEX) are tested under option test. The option test is initiated by pressing the "opt _test" softkey. The upper and lower 32K of RAM have their own PV and display different error messages.

Area Tested:

All upper 32K x 16 locations of RAM including refresh ability, the multiplexed memory Address/Data bus from the CPU, Motherboard connections between CPU and Display Controller board, the demultiplexed Address/Data bus to/from RAM, and the timing and control circuitry.

Operation:

a. The power up RAM test operates differently from the PV test.

b. The RAM test takes approximately 7 seconds.

c. All upper 32 x 16 locations of RAM are toggled to insure READ/WRITE operation.

d. Refresh ability is verified.

e. The operation of the routine is as follows:

1. Load RAM with a pseudo random count, starting with zero.
2. Read RAM and compare with count.
3. Check for an error. If error occurs go to error sequence.
4. If there is no previous error, wait one second.
5. Read RAM and compare with count.
6. Check for an error. If error occurs go to error sequence.
7. If there is no previous error, load RAM with complement of count, starting at zero.
8. Read RAM and compare with the complement of the count.
9. Check for an error. If error occurs go to error sequence (see step f).
10. If there is no previous error, wait one second.
11. Read RAM and compare with count.
12. Check for an error. If error occurs, go to error sequence.

f. If there are not any errors in either RAM error mask then the system will beep twice. But, if an error exists, then the following error sequence occurs for steps a thru e:

1. Reset the delta timer to prevent auto restart.
2. Set the SA latch.
3. Write to and read from the upper 32K locations of RAM.
4. Provide stimulus to CRT controller.
5. Output RAM error display header information (including refresh error message if refresh error flag set).
6. Reset SA latch.
7. Output individual failing IC number for the upper 32K x 16 memory locations which are contained on all 16 RAM ICs.

NOTE

The Display Controller board has 64K x 16 memory locations on 16 RAM ICs. The older Display Controller boards (with serial prefix numbers less than on the title page of this manual) have 32K x 16 memory locations on 32 RAM ICs. When a RAM failure occurs, the failing unit number might display two failure RAM numbers. When the message is read, use the lower value number and disregard the larger number. The reason this occurs is the firmware has not changed and so the coded RAM failure message remains the same.

g. When a failure occurs, the routine attempts to output an error message as follows:

```
SELF-TEST FAILURE <------- blinking
RAM TEST:
FAILING UNIT NUMBER (S)
------------------------
XY   <--- older failing RAM numbers (U51-U58 or U65-U72 not used)

XY   <--- failing RAM number (U23-U30 or U38-U45)
```

"XY" corresponds to the U# of the failing RAM. Depending on which RAM is failing, the display could be affected. Evidence of this is a random pattern on the CRT or incorrect spelling of messages. For this reason the accuracy of a RAM test failure is always suspect. Because each RAM is 1 bit wide, all 16 RAMs are used to store display information. Thus, if any of these 16 RAMs is failing, the display will be unintelligible to various degrees. If the error message displays two failing RAMs, use the lower IC number.

4-18. UPPER 32K RAM PV TEST.

Purpose:

The RAM test verifies the ability to read and write from the upper 32K addressable locations of RAM located on the Display Control board and checks for refresh. Note that this test only occurs during PV and is intended to troubleshoot intermittent problems. This test can be run in single step or continuous mode. It displays the number of tests run versus the number of tests failed. If a failure occurs, an error message code will be displayed on the same line.

Area Tested:

All upper 32K x 16 memory locations including refresh ability, the multiplexed memory Address/Data bus from the CPU, Motherboard connections between CPU and Display Controller board, the demultiplexed Address/Data bus to/from RAM, and the timing and control circuitry.

Operation:

a. This test takes approximately eight seconds.

b. Data from ROM is written into RAM, and then read back and compared to the ROM contents.

c. The second step writes walking 1's and 0's to each RAM address and reads it back. The walking 1's and 0's are visable on the CRT as a blinking pattern with characters moving to the bottom of the screen.

NOTE

Since the display uses a portion of all 16 RAMs, a failure may affect the ability to display the failed RAM IC number.

Example of PV ERROR MESSAGE.

RAM TEST: BIT ERROR MASK UPPER BANK=XXXX LOWER BANK=XXXX

The XXXX is the hexidecimal representation of the 16 bit error mask. Since there are 64K x 16 locations of RAM, each RAM IC is one data bit for the entire upper 32K address range. There is a one to one correlation between the data bit set in the error mask and the failing RAM.

Table 4-3. PV ERROR CODE

A "1" indicates a failure when the HEX error code is converted to BINARY.

Example error: RAM TEST: BIT ERROR MASK UPPER BANK=2004 LOWER BANK=0000

2	0	0	4
U45 U44 U43 U42	U41 U40 U39 U38	U30 U29 U28 U27	U26 U25 U24 U23
0 0 1 0	0 0 0 0	0 0 0 0	0 1 0 0

U43 and U25 have failed.

Example error: RAM TEST: BIT ERROR MASK UPPER BANK=0000 LOWER BANK=A010

A	0	1	0
U45 U44 U43 U42	U41 U40 U39 U38	U30 U29 U28 U27	U26 U25 U24 U23
1 0 1 0	0 0 0 0	0 0 0 1	0 0 0 0

U45, U43, and U27 have failed.

NOTE

The error message display shows "UPPER BANK" and "LOWER BANK". There is only one bank of RAM on the Display Controller board for mainframes identified by the serial prefix number on the title page of this manual. The XXXX message is still valid. Ignore which BANK the message appears in. Table 4-3 should simplify the error message.

4-19. I/O WRITE TEST PROCEDURE.

Purpose:
This test provides audible feedback that the test is executing by beeping, and provides the following SA stimulus. The I/O WRITE TEST cycles the PHI chip register addresses, cycles the interrupt masks, cycles the slot select lines and stimulates the four rear panel BNC connectors.

Area Tested:
This test is not a pass/fail test. It provides stimulus for signature analysis for the following circuitry: Option slot select lines on the motherboard, all connections from option slots to the rear panel BNC connectors, the beeper circuitry, PHI register address latch, and the interrupt mask circuitry.

Operation:
a. This test will not display a failure. The main purpose of the test is for signature analysis (SA).

b. The only noticeable failure will be the loss of the audible beeper.

c. See I/O section IV for more information about this test.

4-20. I/O READ TEST PROCEDURE.

Purpose:
This test reads the rear panel switches, the hardware configuration jumpers, the RS232 switch settings, and the master controller/non controller configuration (SLAVE configuration). It is also used with signature analysis.

Area Tested:
Rear panel dipswitches, the cable to the rear panel, I/O circuitry, and the RS232 dipswitches.

Operation:
a. Upon initiation of the I/O READ TEST, the PV menu displays the following in inverse video:

I/O READ TEST: ADDR=XX BOOT=XX M=X RS232=XXXXXXXX HC=XX XXXXX N/A

ADDR=XX is the HPIB address (0-1F) as set by the rear panel switches.

BOOT=XX is the boot source set by the rear panel switches as follows:

Bit 1	Bit 0	Control Source
0	0	System Bus
0	1	Local Mass Storage Talk only
1	0	Local Mass Storage Addressable
1	1	Performance Verification

M=X X=1 for CONTROLLER (MASTER)
X=0 for NON-CONTROLLER (SLAVE)

RS232=XXXXXXXX Read from S4 on the I/O board.
Bit 76543210

Bit 0 Term/Modem 0= Terminal 1= Modem

Bit 1 Baud rate X1/X16

Bit 2 Word Length
Bit 3 Word Length

Bit 3	Bit 2	Word Length
0	0	5
0	1	6
1	0	7
1	1	8

Bit 4 Parity Enable 0= Parity Disabled
1= Parity Enabled

Bit 5 Parity Odd/Even 0= Odd Parity
1= Even Parity
Bit 6 Number of stop bits
Bit 7 Number of stop bits

Bit 7	Bit 6	# of Stop Bits
0	0	INVALID
0	1	1
1	0	1.5
1	1	2

HC=XX is the hexidecimal representation of the six hardware jumpers. They are not read in this test.

4-21. TIME INTERRUPT TEST PROCEDURE.

Purpose:
The TIME INTERRUPT TEST indicates proper operation of the 50 to 60 Hz line sync to the CPU via the delta time interrupt circuitry.

Area Tested:
LINE SYNC a 50 to 60 Hz signal from the power supply, the delta time interrupt circuitry on the I/O board, and interrupts to the CPU.

Operation:
a. Upon initiation, the PV test counts and displays line sync interrupts to the CPU.

b. If a failure occurs, refer to I/O section IV for more information.

4-22. KEYBOARD TEST PROCEDURE.

Purpose:
The KEYBOARD TEST indicates proper keyboard switch closures and keyboard decoding.

Area Tested:
All 77 keyswitches, keyboard decoding electronics, keyboard cable, and the keyboard RAM/state machine.

Operation:
a. When initiated, the KEYBOARD TEST instructs the user to press all of the keyboard keys in a left-to-right top-tobottom sequence.

b. The sequence begins with the leftmost softkey and includes all display and cursor control keys.

c. The keyboard test requires this specific sequence. Furthermore, even if all keyswitches and the decoding circuitry are working, a key that is pressed out of sequence will cause a "FAILED TEST" message and end the test.

d. For more information, see I/O section IV.

e. The order in which the keys are pressed is given below in figure 4-4.

f. Note the KEYBOARD TEST is skipped while PV is in the cycle mode.

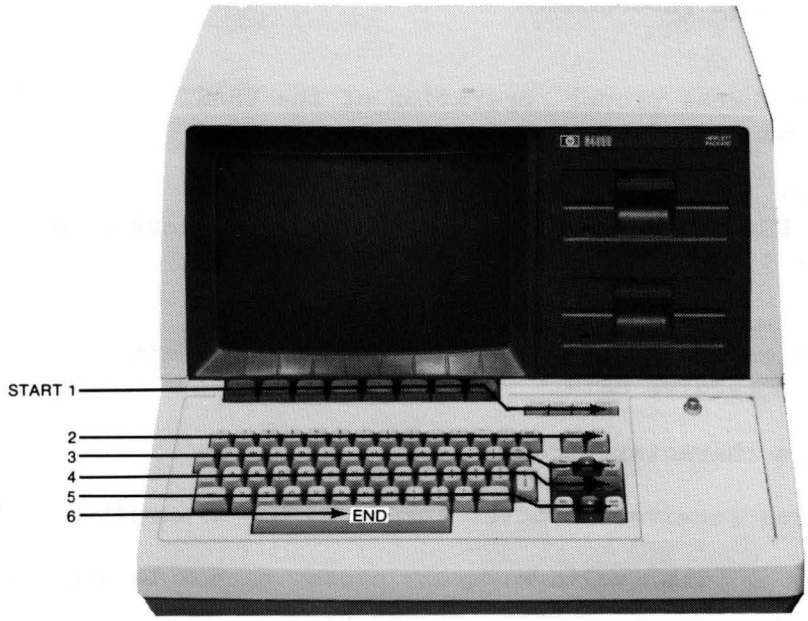

Figure 4-4. Keyboard PV Test Sequence.

4-23. SYSTEM BUS TEST PROCEDURE.

CAUTION

THIS TEST SHOULD NOT BE RUN IF THE MAINFRAME IS CONNECTED TO A SYSTEM BUS AND IS THE MASTER CONTROLLER!

Purpose:
During the System Bus Test the PHI (U20 I/O board) chip is taken off line and the CPU writes to and reads from its internal registers. The circuitry on the input side of the PHI chip and most of the PHI chip itself is tested. None of the output circuitry to the system bus is tested.

Area Tested:
Data, address, control and interrupt lines from the CPU to the PHI chip.

Operation:

a. The SYSTEM BUS TEST takes the PHI chip off line and reads and writes to various registers in the PHI chip.

b. The transceiver lines and the cable to the rear panel HPIB connector are not presently being checked.

c. If a failure occurs, see section IV of the I/O tab.

d. This test may take up to two minutes if a failure occurs.

4-24. RS232 TEST PROCEDURE.

Purpose:

This test checks proper operation of the USART (U28 I/O PCB) and the data and control circuitry associated with RS-232.

Area Tested:

The 8251 USART, the baud rate generator, loop-back relays, line drivers, the interface to the CPU, and the rear panel cable.

Operation:

a. Energizes the loop back relays to loop transmit data, and handshake lines back on receive data.

b. Sends a character stream.

c. compares receive character stream to the transmit character stream.

d. Notes:

1. The voltage translators cannot be signaturized on the higher voltage side.

2. This test may take up to two minutes for a failure to be detected. See section IV of the I/O tab for more information.

4-25. PV ON THE EXISTING LOCAL MASS STORAGE OPTION.

NOTE

If the mainframe under test contains a floppy disc option then PV for the floppy disc will be given and explained in the floppy service manual. If the mainframe contains the cassette tape option then the PV will be explained in the tape controller service manual.

4-26. FLOPPY DISC TEST PROCEDURE.

NOTE

A formatted disc must be used when performing the floppy PV. However, the WRITE electronics are not tested if a disc containing data on track 34 is present in the drive being tested. Furthermore, the floppy PV will only verify to an 85% confidence level that the mini drives are operational. In order to completely test the drives the floppy diagnostics must also be done. Refer to the local mass storage manual for more information regarding the floppy PV and the diagnostic tests.

Purpose:
The FLOPPY DISC TEST tests several functions of the two floppy disc drives and the controller board electronics.

Area Tested:
CPU and I/O data lines, floppy controller board electronics, the cable from the controller board to the drives, drive READ/WRITE electronics and mechanics, and the CPU, I/O and interface circuitry.

Operation:

a. Response from floppy controller chip is tested by writting a pattern to the track register and reading it back.

b. When initiated, each floppy drive is cycled through the following series of tests:

1. The drive is selected.
2. The drive is restored (head moved to track 00).
3. Step inward to track 1 (check TRK00 indicator OFF)
4. Step out to track 00, check track 0 indicator ON.
5. Read all sectors on track 0, side 0; check for all errors.
6. Step to track 34, read all sectors on both sides.

c. The PV routines now check to see if there is any data on track 34. Track 34 will be a spare track on a disc with no bad tracks. However, if there is a bad track on a disc, then track 34 is allocated as useable even though it may contain information.

d. If data exists on track 34, a READ/WRITE test is not performed and a message indicating this is displayed on the CRT. If track 34 is available, the following is performed:

7. Known data on side 0, sector 0 is READ.

8. A random data pattern is written to side 0, sector 1.

9. The pattern is read from side 0 sector 1 and compared with what was written.

10. Steps 7,8 and 9 are repeated on track 34,side 1.

4-27. TAPE TEST PROCEDURE.

NOTE

It is recommended that PV on the cassette tape option not be performed with a cassette with data stored on it. During PV read/write functions are done which will result in loss of existing data on the tape. Refer to the tape control and drive manual for more information.

Purpose:
The TAPE TEST will test every function of the tape system.

Area Tested:
The hole detectors, high speed reverse, high speed forward search, the record capabilities, read/write circuitry and servo fail detection.

Operation:

When executing the PV, The following sequence is performed:

a. Rewind tape to load point.

b. Write an ID file on track 0

c. Write data file on track 0.

d. Write end of valid data gap on track 0.

e. Rewind tape to load point.

f. Write ID 1 file on track 1.

g. Write data 1 file on track 1.

h. Write ID 2 file on track 1.

i. Write data 2 file on track 1.

j. Write end of valid data gap on track 1.

k. Rewind tape to load point.

l. Read data file on track 0 and compare.

m. Rewind tape to load point.

n. Search track 1 for data 2 file.

o. Read data 2 file on track 1 and compare.

p. Start again at beginning.

4-28. TROUBLESHOOTING PV FAILURES USING SIGNATURE ANALYSIS.

4-29. All PV tests set an SA interval at the beginning of the test and clear it at the end (except for the Keyboard Test and the Delta-Time Interrupt time). The tests will repeat as long as desired whether or not there is a failure.

4-30. A unique "Vh" signature is also provided in the display pattern test. This allows you to verify that the CPU is operating properly even when failures such as the loss of high voltage render the CRT display useless. However, the "B" key may be pressed to determine if the CPU is servicing interrupts. The beeper will sound indicating proper operation of the CPU.

4-31. TROUBLESHOOTING.

4-32. The purpose of the information in this section is to guide you as quickly as possible to the functional area that is failing in the Mainframe.

NOTE

If an error is detected while running PV, remove all PC boards from the cardcage except for the first three mainframe boards (I/O, DISP CNTL, and CPU) and repeat the mainframe PV tests before continuing. This narrows the failure down to either the mainframe or options.

4-33. Figure 4-5 is a troubleshooting diagnostic diagram that will serve as a guide when troubleshooting the 64100A mainframe. This diagram summarizes the troubleshooting routes and procedures that are detailed in the following paragraphs and in the other sections (Tabs) of this manual to which you may be directed.

4-34. Table 4-3 lists several types of failures that could occur, and will direct you either to one of five tabs (PWR SUPP, CPU, DISPLAY, I/O, FLOPPY or TAPE CONTROL).

Table 4-4. Failure Conditions and Routing

FAILURE CONDITION	ROUTING (GO TO)
1. Can not intiate PV	CPU Chapter (Section IV)
2. No Beeps or No Display or Wrong Test Display Pattern	Check +12 and +-5 Vdc and then go to table 4-3.
3. NEXT TEST softkey doesn't work.	I/O Chapter (Section IV)
4. ROM TEST fails	CPU Chapter (Section IV)
5. RAM TEST fails	Display Chapter (Section IV)
6. I/O WRITE TEST:	I/O Chapter (Section IV)
a) READ TEST	
b) TIME INTERVAL TEST	
c) KEYBOARD TEST	
d) SYS BUS TEST	
e) RS-232 BUS TEST	
7. TAPE TEST	Tape Control and Drive Chapter (option) (Section IV).
8. FLOPPY TEST	Local Mass Storage and Flexible Drive Chapter (option) (Section IV).

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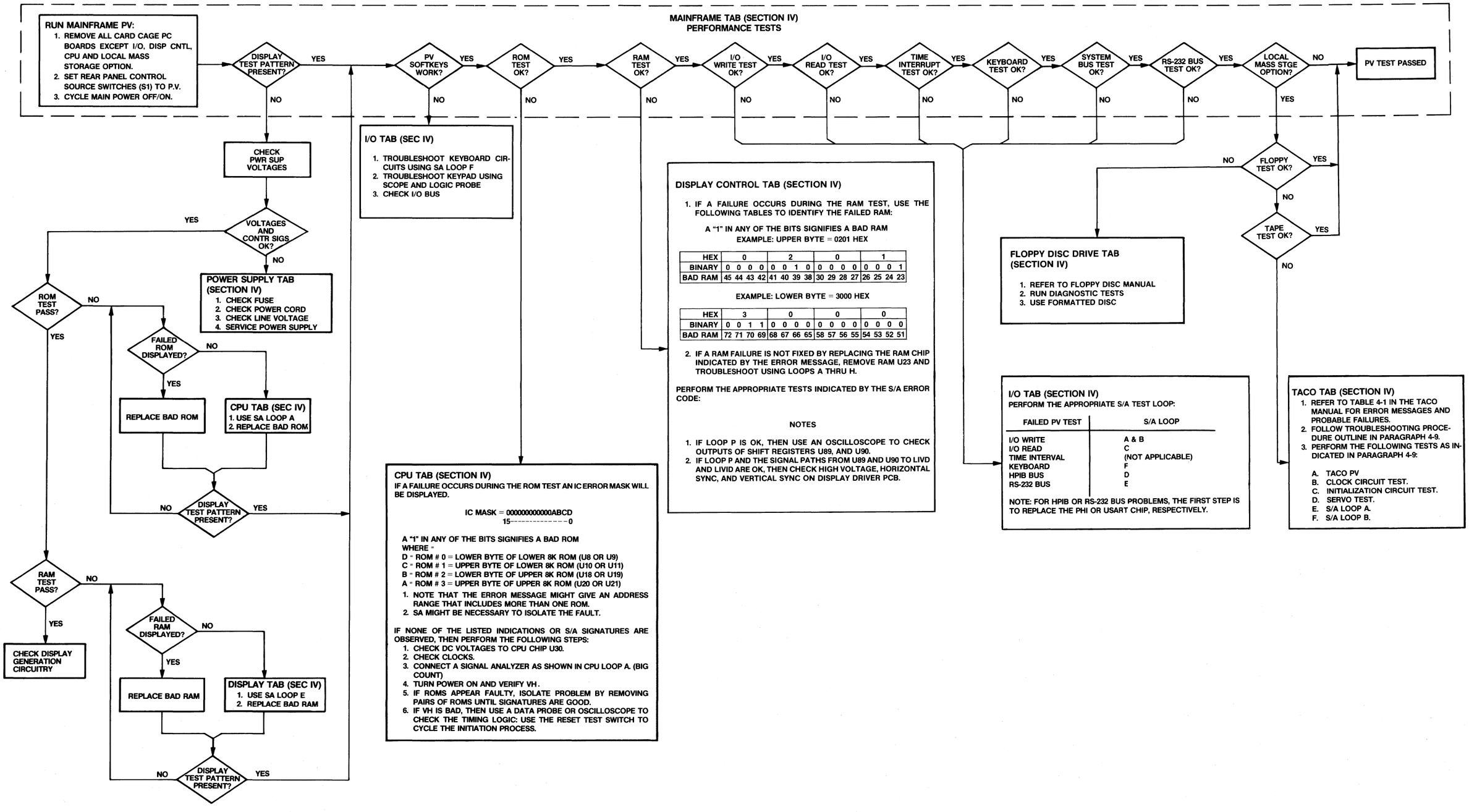


Figure 4-5.
Mainframe Troubleshooting Guide
MF 4-25/(4-26 blank)

SECTION V

ADJUSTMENTS

5-1. GENERAL.

5-2. There are no adjustments that apply strictly to the Mainframe structure. Refer to the Display Driver, CPU and Power Supply Chapter for adjustments that pertain to these PC boards and the CRT.

Section VI

REPLACEABLE PARTS

6-1. INTRODUCTION

6-2. This section contains information for ordering parts. Table 6-1 lists the names and addresses that correspond to the manufacturers' code numbers. Table 6-2 lists the abbreviations used in the parts list and throughout this manual. Table 6-3 lists all replaceable parts for the 64100A Mainframe in reference designator order.

6-3. ABBREVIATIONS

6-4. Table 6-2 lists abbreviations used in the parts list, the schematics, and elsewhere in this manual. In some cases, two forms of the abbreviation are used; one, all in capital letters, and two, partial or no capitals. This occurs because the abbreviations in the parts list are always all capitals. However, in the schematics and other parts of the manual, other abbreviation forms may be used with both lowercase and uppercase letters.

6-5. MAJOR COMPONENTS

6-6. The major components comprising the Model 64100A Mainframe are listed below. Figure 6-1 shows the location of the Mainframe components excluding the mounting/attach screws. The attach screws are shown in figure 6-2. Figure 6-2 is to be used in conjunction with the instructions presented in Section II (Installation and Removal) for replacing the various Mainframe parts when necessary. The reference designators shown on figure 6-1 (Mainframe Component Locator) refer to table 6-3 (Replaceable Parts).

COMPONENT	H-P PART NUMBER
1. Motherboard	64100-66526
2. Rear Panel PC Board	64100-66524
3. CPU PC Board	64100-66532
4. I/O PC Board	64100-66520
5. Disp. Cont. PC Board	64100-66530
6. Disp. Driver PC Board	64100-66531
7. Keyboard Assy	64100-66504
8. Extender Board	64100-66510
9. Display Extender Board	64100-66512
10. Power Supply	64100-62602
11. Cathode Ray Tube/Yoke Assy	64100-67301
12. Fan	3160-0349

Table 6-1. List of Manufactures' Codes

MFR NO.	MANUFACTURER NAME	ADDRESS	ZIP CODE
00000	Any Satisfactory Supplier		
00466	Norelco N. Amer Phillips Corp	Los Angeles Ca	90021
01121	Allen-Bradley Co	Milwaukee Wi	53204
01295	Texas Instr Semicond Div	Dallas Tx	75222
01928	RCA Corp Solid State Div	Somerville NJ	08876
03888	KDI Pyrofilm Corp	Whippany NJ	07981
04713	Motorola Semicond Products	Phoenix Az	85062
07263	Fairchild Semicond Div	Mountain View Ca	94042
09023	Cornell-Dubilier Eleck Div	Sanford NC	27330
13103	Thermalloy Co	Dallas Tx	75234
19701	Mepco/Electra Corp	Mineral Wells Tx	76067
20940	Micro-Ohm Corp	El Monte Ca	91731
24546	Corning Glass Wks	Bradford Pa	16701
26654	Varadyne Inc	Santa Monica Ca	90404
27014	National Semicond Corp	Santa Clara Ca	95051
27777	Varo Semicond Inc	Garland Tx	75040
28480	Hewlett-Packard Hq	Palo Alto Ca	94304
30983	Mepco/Electra Corp	San Diego Ca	92121
32997	Bourns Trimpot Div	Riverside Ca	92507
34344	Motorola Inc	Franklin Park Il	60131
34649	Intel Corp	Mountain View Ca	95051
56289	Sprague Elect Co	North Adams Ma	01247
71590	Centralab Eleck Div	Milwaukee Wi	50501
72136	Electro Motive Corp	Willimantic Ct	06226
75042	TRW Inc	Philadelphia Pa	19108
75382	Kulka Elect Corp	Mt Vernon NY	10550
75915	Littlefuse Inc	Des Plaines Il	60016

6-7. ORDERING INFORMATION

6-8. To order a part listed in the replaceable parts list (table 6-3), quote the Hewlett-Packard part number and check digit, indicate the quantity required, and address the order to the nearest HewlettPackard Office (refer to Sales and Service offices listed at the back of this manual).

6-9. To order a part that is not listed in table 6-3, include the instrument model number, instrument serial number, the description and function of the part, and the number of parts required. Address the order to the nearest Hewlett-Packard office.

6-10. DIRECT MAIL ORDER SYSTEM

6-11. Within the USA, Hewlett-Packard can supply parts through a direct mail order system. Advantages of using this system are:

1. Direct ordering and shipment from the HP Parts Center in Mountain View, California.

2. No maximum or minimum on any mail order (there is a minimum order amount for parts ordered through a local HP office when the orders require billing and invoicing).

3. Prepaid transportation (there is a small handling charge for each order).

4. No invoices (to provide these advantages, a check or money order must accompany each order).

6-12. Mail-order forms and specific ordering information are available through your local HP office. Addresses and phone numbers are located at the back of this manual.

6-13. PARTS LIST

6-14. Table 6-3 lists the replaceable parts for the Model 64100A Mainframe and is organized as follows:

1. Electrical assemblies and their components in alphanumerical order by reference designation.

2. Miscellaneous parts.

6-15. The information given for each part consists of the following:

1. Hewlett-Packard part number and check digit. (for HP internal use).
2. Total quantity (Qty).
3. Description of the part.
4. Typical manufacturer of the part in a five-digit code.
5. Manufacturer's number for the part.

NOTE

The total quantity for each part is given only at the first appearance of the part number in the list.

Table 6-2. Reference Designators and Abbreviations

REFERENCE DESIGNATORS

A	= assembly	**F**	= fuse	**MP**	= mechanical part	**U**	= integrated circuit
B	= motor	**FL**	= filter	**P**	= plug	**V**	= vacuum, tube, neon bulb, photocell, etc
BT	= battery	**IC**	= integrated circuit	**Q**	= transistor		
C	= capacitor	**J**	= jack	**R**	= resistor	**VR**	= voltage regulator
CP	= coupler	**K**	= relay	**RT**	= thermistor	**W**	= cable
CR	= diode	**L**	= inductor	**S**	= switch	**X**	= socket
DL	= delay line	**LS**	= loud speaker	**T**	= transformer	**Y**	= crystal
DS	= device signaling (lamp)	**M**	= meter	**TB**	= terminal board	**Z**	= tuned cavity network
E	= misc electronic part	**MK**	= microphone	**TP**	= test point		

ABBREVIATIONS

A	= amperes	**H**	= henries	**N/O**	= normally open	**RMO**	= rack mount only
AFC	= automatic frequency control	**HDW**	= hardware	**NOM**	= nominal	**RMS**	= root-mean square
AMPL	= amplifier	**HEX**	= hexagonal	**NPO**	= negative positive zero (zero temperature coefficient)	**RWV**	= reverse working voltage
		HG	= mercury				
BFO	= beat frequency oscillator	**HR**	= hour(s)				
BE CU	= beryllium copper	**HZ**	= hertz	**NPN**	= negative-positive-negative	**S-B**	= slow-blow
BH	= binder head					**SCR**	= screw
BP	= bandpass			**NRFR**	= not recommended for field replacement	**SE**	= selenium
BRS	= brass	**IF**	= intermediate freq			**SECT**	= section(s)
BWO	= backward wave oscillator	**IMPG**	= impregnated	**NSR**	= not separately replaceable	**SEMICON**	= semiconductor
		INCD	= incandescent			**SI**	= silicon
CCW	= counter-clockwise	**INCL**	= include(s)			**SIL**	= silver
CER	= ceramic	**INS**	= insulation(ed)	**OBD**	= order by description	**SL**	= slide
CMO	= cabinet mount only	**INT**	= internal	**OH**	= oval head	**SPG**	= spring
COEF	= coeficient			**OX**	= oxide	**SPL**	= special
COM	= common	**K**	= kilo=1000			**SST**	= stainless steel
COMP	= composition					**SR**	= split ring
COMPL	= complete	**LH**	= left hand	**P**	= peak	**STL**	= steel
CONN	= connector	**LIN**	= linear taper	**PC**	= printed circuit		
CP	= cadmium plate	**LK WASH**	= lock washer	**PF**	= picofarads= 10^{-12} farads	**TA**	= tantalum
CRT	= cathode-ray tube	**LOG**	= logarithmic taper			**TD**	= time delay
CW	= clockwise	**LPF**	= low pass filter	**PH BRZ**	= phosphor bronze	**TGL**	= toggle
				PHL	= phillips	**THD**	= thread
DEPC	= deposited carbon	**M**	= milli=10^{-3}	**PIV**	= peak inverse voltage	**TI**	= titanium
DR	= drive	**MEG**	= meg=10^{6}	**PNP**	= positive-negative-positive	**TOL**	= tolerance
		MET FLM	= metal film			**TRIM**	= trimmer
ELECT	= electrolytic	**MET OX**	= metallic oxide	**P/O**	= part of	**TWT**	= traveling wave tube
ENCAP	= encapsulated	**MFR**	= manufacturer	**POLY**	= polystyrene		
EXT	= external	**MHZ**	= mega hertz	**PORC**	= porcelain	**U**	= micro=10^{-6}
		MINAT	= miniature	**POS**	= position(s)		
F	= farads	**MOM**	= momentary	**POT**	= potentiometer	**VAR**	= variable
FH	= flat head	**MOS**	= metal oxide substrate	**PP**	= peak-to-peak	**VDCW**	= dc working volts
FIL H	= fillister head	**MTG**	= mounting	**PT**	= point		
FXD	= fixed	**MY**	= "mylar"	**PWV**	= peak working voltage	**W/**	= with
						W	= watts
G	= giga (10^{9})	**N**	= nano (10^{-9})	**RECT**	= rectifier	**WIV**	= working inverse voltage
GE	= germanium	**N/C**	= normally closed	**RF**	= radio frequency		
GL	= glass	**NE**	= neon	**RH**	= round head or right hand	**WW**	= wirewound
GRD	= ground(ed)	**NI PL**	= nickel plate			**W/O**	= without

Table 6-3. Replaceable Parts List

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1	64100-62602	9	1	POWER SUPPLY	28480	64100-62602
A2	64100-66526	4	1	MOTHER BOARD ASSEMBLY	28480	64100-66526
A3	64100-66532	0	1	CPU/ROM BOARD ASSEMBLY	28480	64100-66532
A4	64100-66504	8	1	KEYBOARD ASSEMBLY	28480	64100-66504
A5	64100-66530	6	1	DISPLAY CONTROLLER BOARD ASSEMBLY	28480	64100-66530
A6	64100-66520	8	1	I/O BOARD ASSEMBLY	28480	64100-66520
A7	64100-66527	1	1	DISPLAY DRIVER BOARD ASSEMBLY	28480	64100-66527
A8	64100-66524	2	1	REAR PANEL BOARD ASSEMBLY	28480	64100-66524
	8120-1351	0	1	POWER CORD CABLE (900 OPT)	28480	8120-1351
	8120-1369	0	1	POWER CORD CABLE (901 OPT)	28480	8120-1369
	8120-2857	3	1	POWER CORD CABLE (902 OPT)	28480	8120-2857
	8120-2104	3	1	POWER CORD CABLE (906 OPT)	28480	8120-2104
	8120-1378	1	1	CABLE ASSY 18AWG 3-CNDCT JGK-JKT (900, 901, 902, 906, OPT)	28480	8120-1378
	8120-2818	5	1	HP-IB CABLE	28480	8120-2818
	64100-61618	5	1	REAR BNC CABLE	28480	64100-61618
	64100-61605	0	1	EXTENSION CABLE	28480	64100-61605
	8120-3349	0	1	IOD BUS CABLE (2 CONNECTOR)	28480	8120-3349
	3160-0349	3	1	FAN (AXIAL)	28480	3160-0349
	64100-66510	6	1	EXTENDER BOARD	28480	64100-66510
	64100-66512	8	1	DISPLAY EXTENDER BOARD	28480	64100-66512
H1	0380-0643	3	2	STUD (METRIC)	00000	ORDER BY DESCRIPTION
H2	0403-0004	0	4	BUMPER FOOT-SCR 1-IN-OD .812-IN-THK BLK	28480	0403-0004
H3	2200-0105	4	15	SCREW-MACH 4-40 .312-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H4	2200-0111	2	13	SCREW-MACH 4-40 .5-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H5	2200-0151	0	1	SCREW-MACH 4-40 .75-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H6	2360-0115	4	38	SCREW-MACH 6-32 .312-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H7	2360-0117	6	18	SCREW-MACH 6-32 .375-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H8	2360-0121	2	17	SCREW-MACH 6-32 .5-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H9	2360-0123	4	17	SCREW-MACH 6-32 .625-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H10	2360-0125	6	4	SCREW-MACH 6-32 .75-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H11	2360-0129	0	2	SCREW-MACH 6-32 1-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H12	2360-0197	2	7	SCREW-MACH 6-32 .375-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H13	2510-0103	9	5	SCREW-MACH 8-32 .375-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H14	2680-0103	8	4	SCREW-MACH 10-32 .5-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H15	2950-0054	1	4	NUT-HEX-DBL-CHAM 1/2-28-THD .125-IN-THK	00000	ORDER BY DESCRIPTION
H16	3050-0002	2	4	WASHER-FL MTLC NO. 10 .203-IN-ID	28480	3050-0002
H17	3050-0010	2	17	WASHER-FL MTLC NO. 6 .147-IN-ID	28480	3050-0010
H18	3050-0066	8	6	WASHER-FL MTLC NO. 6 .147-IN-ID	28480	3050-0066
H19	3050-0235	3	1	WASHER-FL MTLC NO. 4. .117-IN-ID	28480	3050-0235
H20	2190-0005	0	1	WASHER-LK EXT T NO. 4 .116-IN-ID	28480	2190-0005
H21	2190-0006	1	7	WASHER-LK HLCL NO. 6 .141-IN-ID	28480	2190-0006
H22	2190-0017	4	5	WASHER-LK HLCL NO. 8 .168-IN-ID	28480	2190-0017
H23	2190-0034	5	3	WASHER-LK HLCL NO. 10 .194-IN-ID	28480	2190-0034
H24	2190-0068	5	4	WASHER-LK INTL T 1/2 IN .505-IN-ID	28480	2190-0068
MP1	7101-0649	6	1	CABINET BASE	28480	7101-0649
MP2	7101-0650	9	1	CABINET TOP	28480	7101-0650
MP3	7101-0651	0	1	CABINET DOOR	28480	7101-0651
MP4	64100-04112	4	1	BOTTOM COVER	28480	64100-04112
MP5	64100-00101	3	1	MAIN DECK	28480	64100-00101
MP6	64100-00206	9	1	REAR PANEL	28480	64100-00206
MP7	7101-0652	1	1	CRT BEZEL	28480	7101-0652
MP8	5041-1533	9	1	BLANK PANEL	28480	5041-1533
MP9	64100-00205	8	1	POWER INPUT PANEL	28480	64100-00205
MP10	64100-00601	8	1	FAN MAG SHIELD	28480	64100-00601
MP11	64100-04701	7	2	FAN SUPPORT	28480	64100-04701
MP12	3160-0092	3	1	FAN GUARD	28480	3160-0092
MP13	64100-01203	8	2	CABLE CLAMP	28480	64100-01203
MP14	1400-0611	0	2	CABLE CLAMP	28480	1400-0611
MP15	5041-1526	0	2	CARD GUIDE	28480	5041-1526
MP16	64100-65201	7	1	BLANK PROM PANEL ASSY	28480	64100-65201
MP17	64100-04703	9	1	REAR GUIDE SUPPORT	28480	64100-04703
MP18	64100-04704	0	1	FRONT GUIDE SUPPORT	28480	64100-04704
MP19	64100-01201	6	1	SUPPORT STRAP (FOR WIRE SUPPORTS)	28480	64100-01201
MP20	64100-01202	7	2	BEZEL STRAP	28480	64100-01202
MP21	5041-1525	9	6	SUPPORT BRACKET	28480	5041-1525
MP22	1400-0617	6	1	CLIP-TENSION 0.38-IN RND CAPACITY	28480	1400-0617
MP23	1460-1733	5	1	RIGHT SUPPORT WIRE	28480	1460-1733
MP24	1460-1734	6	1	LEFT SUPPORT WIRE	28480	1460-1734
MP25	8160-0442	7	8 ft	CONDUCTIVE GASKET	28480	8160-0442
MP26	64100-04113	5	1	POWER SUPPLY ACCESS PORT	28480	64100-04113
MP27	64100-01204		2	STATE/TIMING GROUND LIPS	28480	64100-01204
MP28	1600-1231		1	KEYBOARD SHIELD	28480	1600-1231
W1	64100-61620	9	1	FAN CABLE	28480	64100-61620
W2	64100-61621	8	1	CRT PLUG CABLE ASSEMBLY	28480	64100-61621
W3	64100-67301	4	1	CRT/YOKE ASSY	28480	64100-67301

See introduction to this section for ordering information

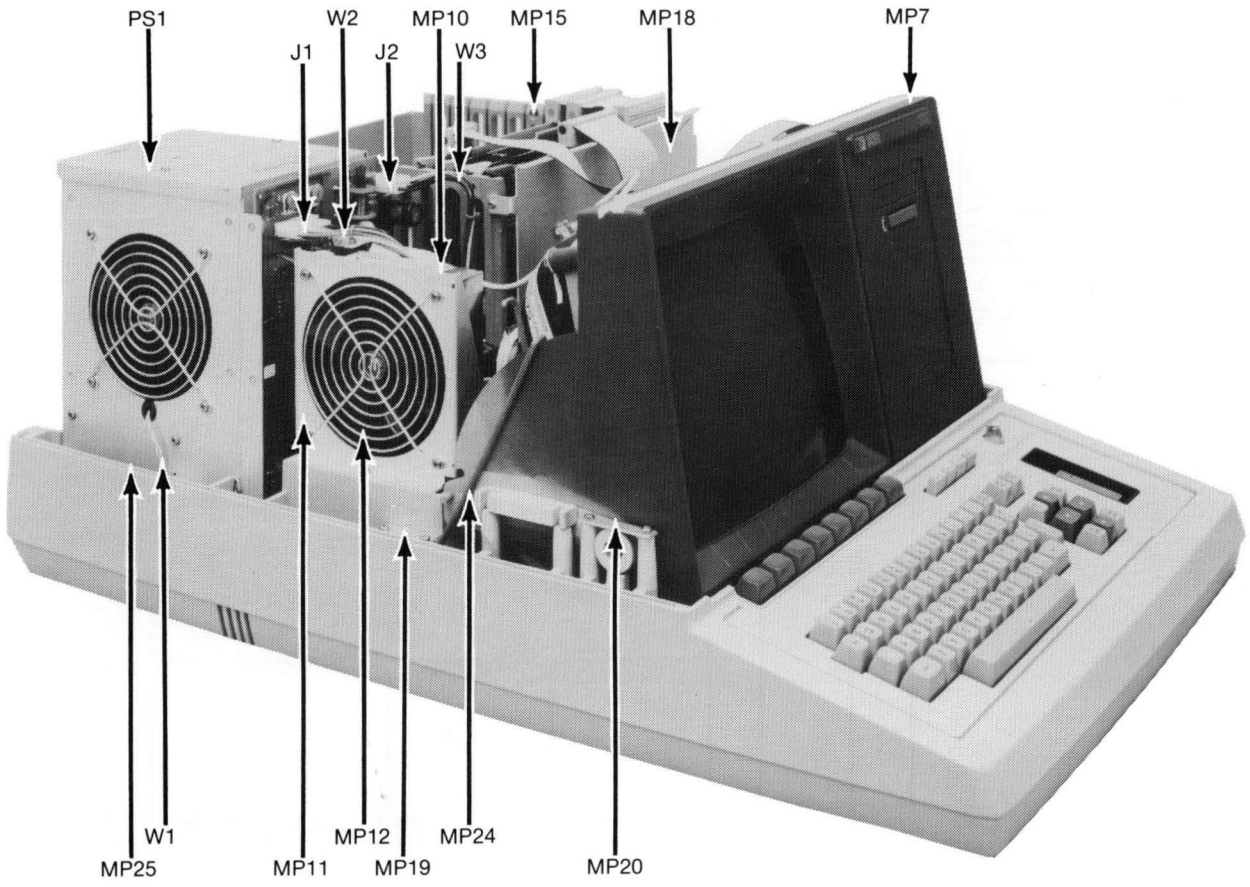


Figure 6-1. Mainframe Component Locator (Left View)

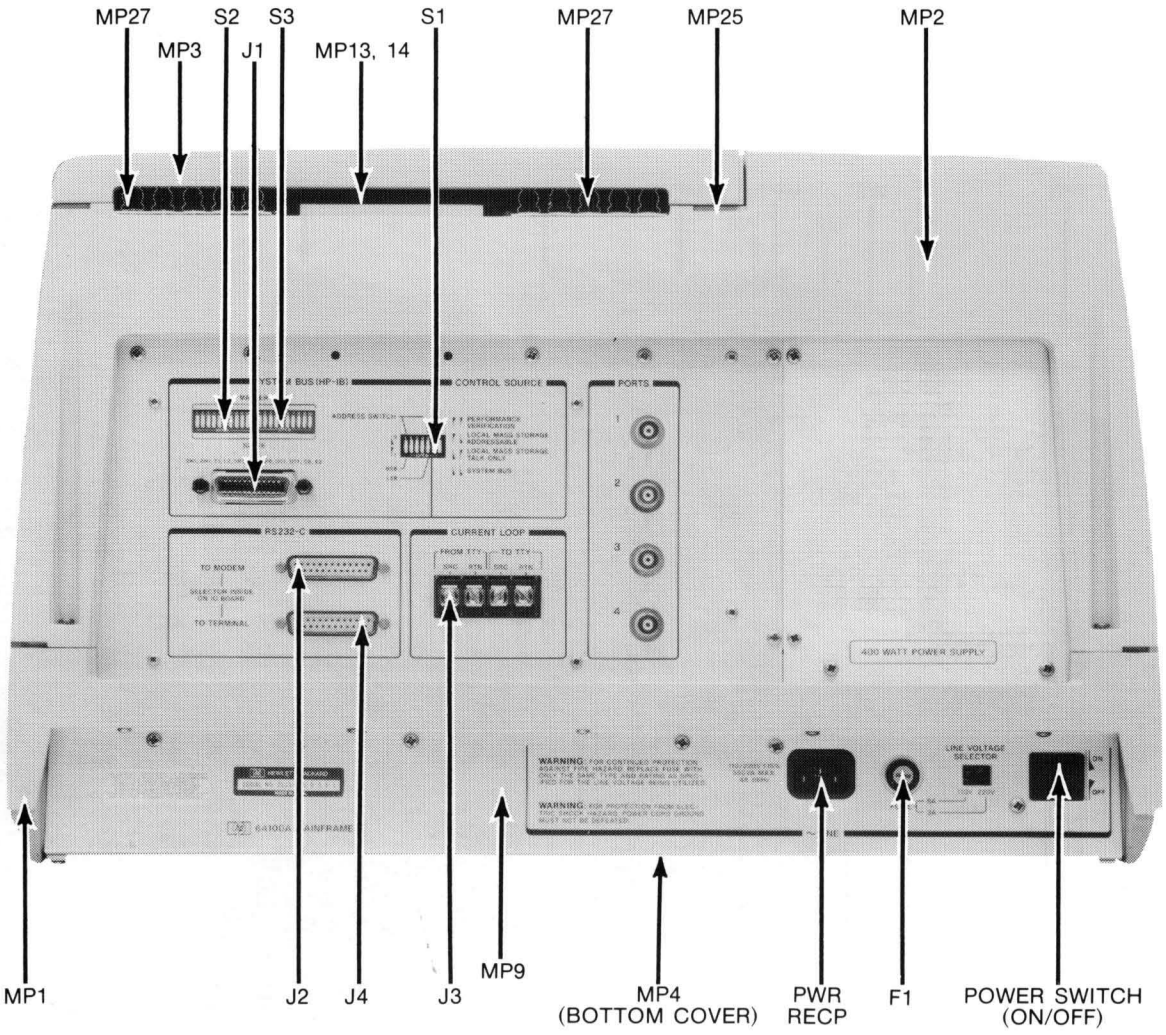


Figure 6-1. Mainframe Component Locator (Rear View)

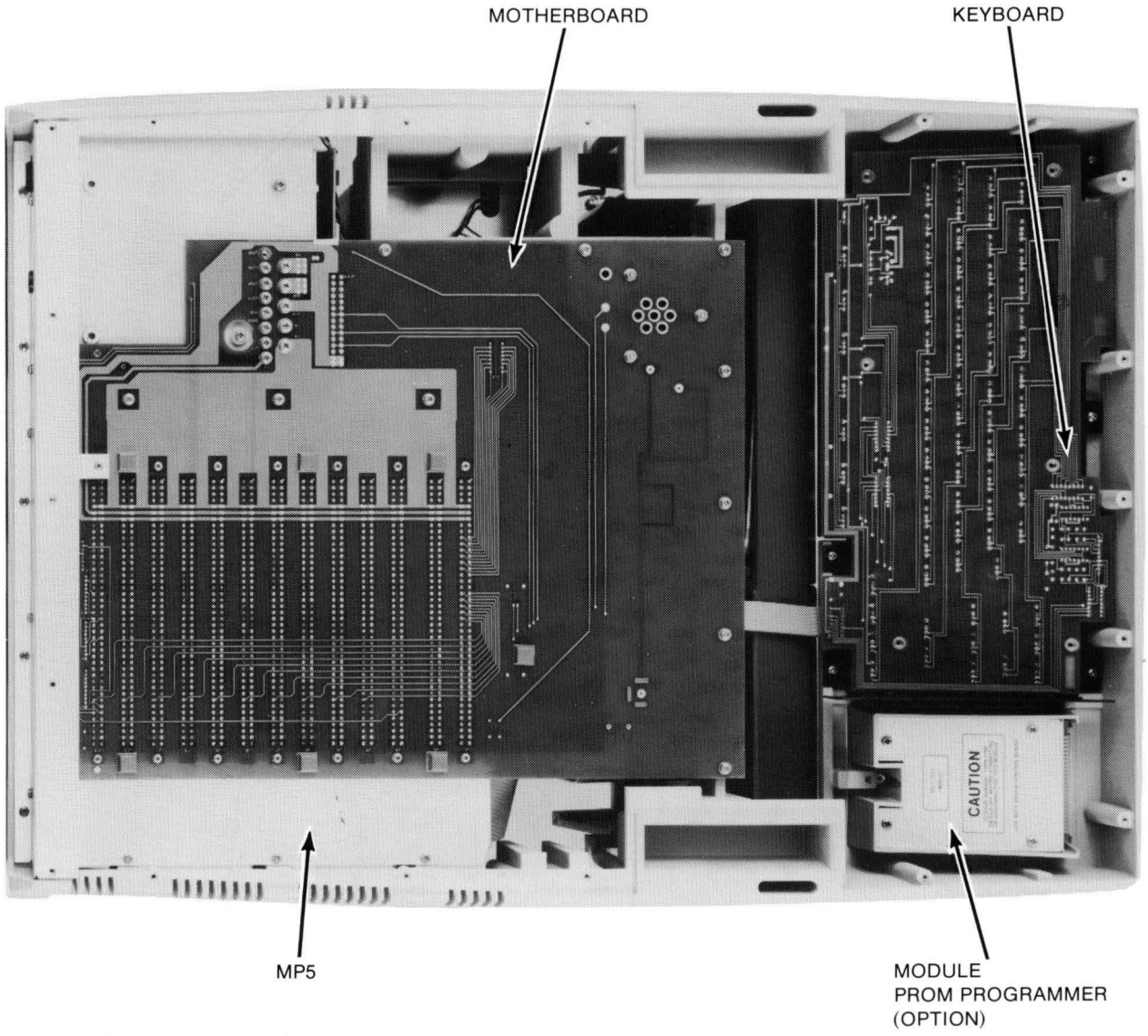


Figure 6-1. Mainframe Component Locator (Bottom View)

Figure 6-2. Mainframe Attach Screw Locator (Sheet 1 of 7)

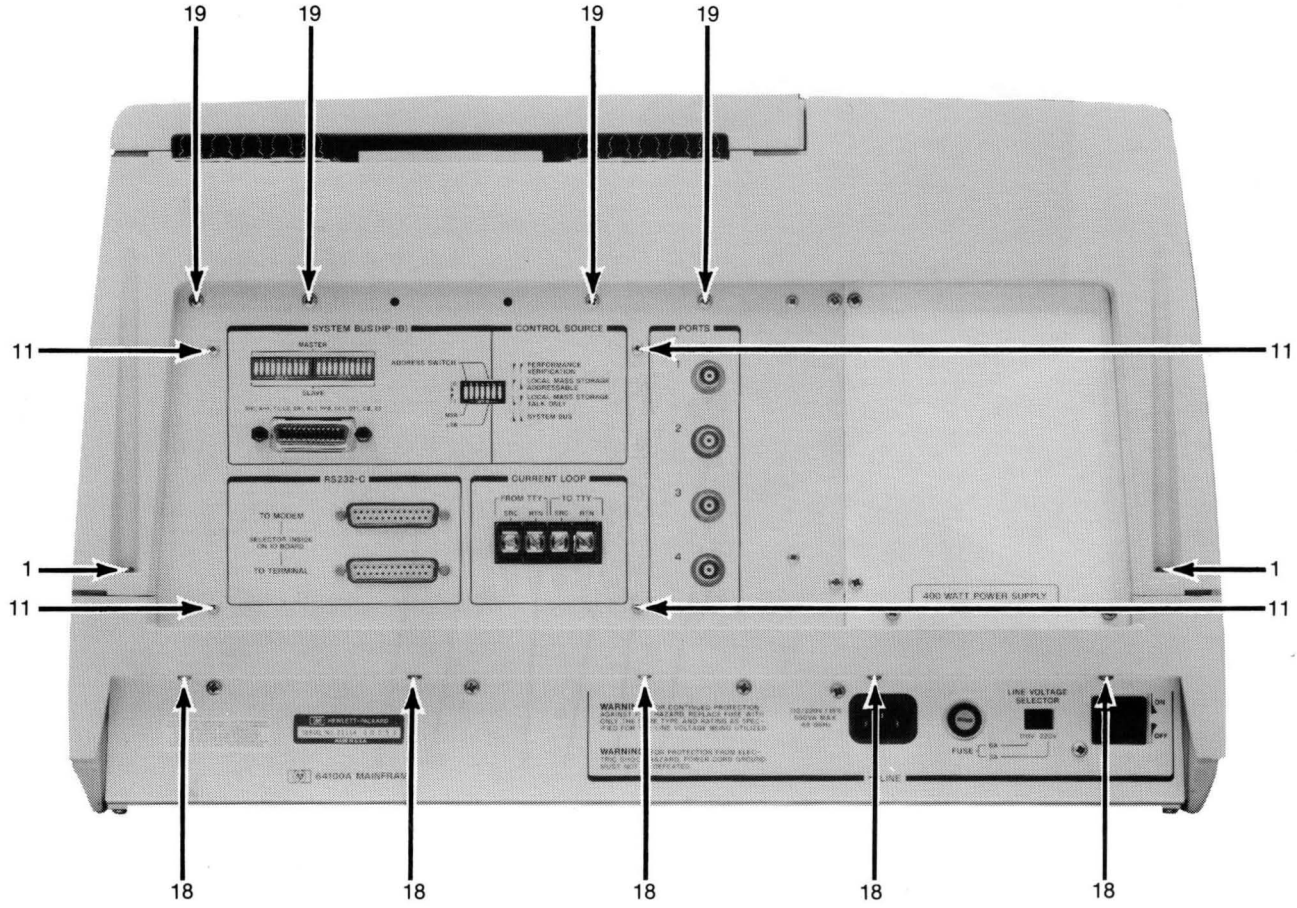


Figure 6-2. Mainframe Attach Screw Locator (Sheet 2 of 7)

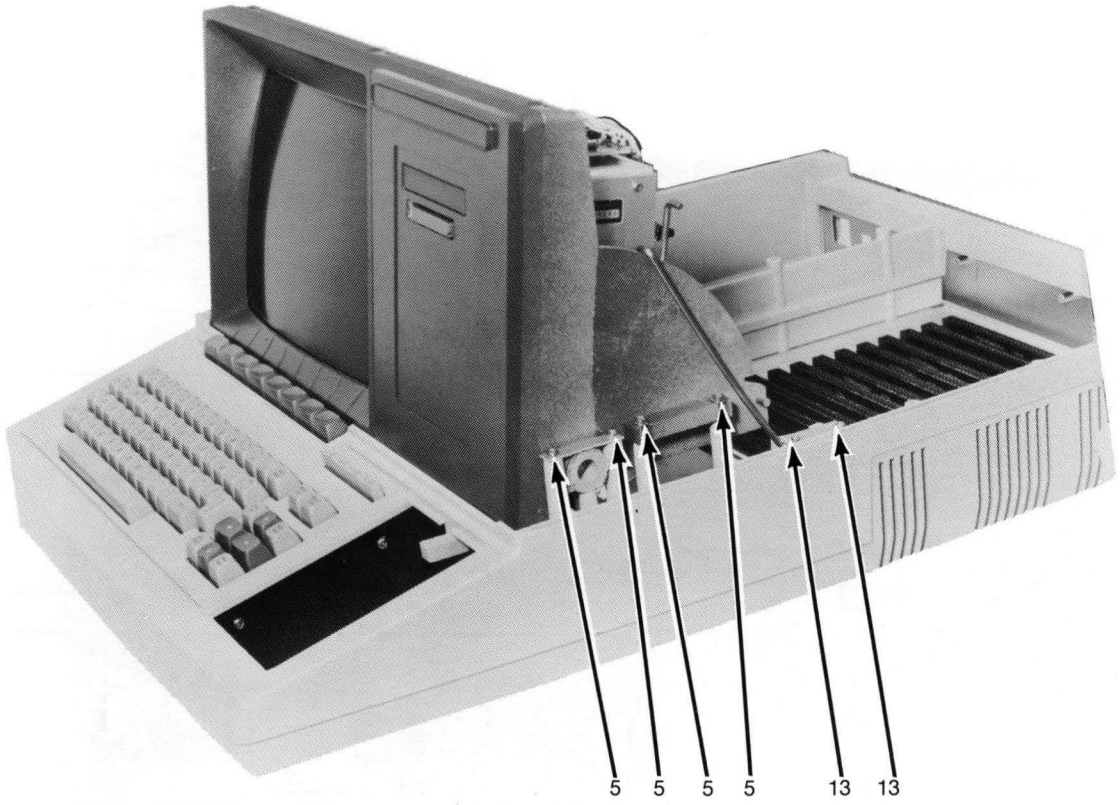


Figure 6-2. Mainframe Attach Screw Locator (Sheet 3 of 7)

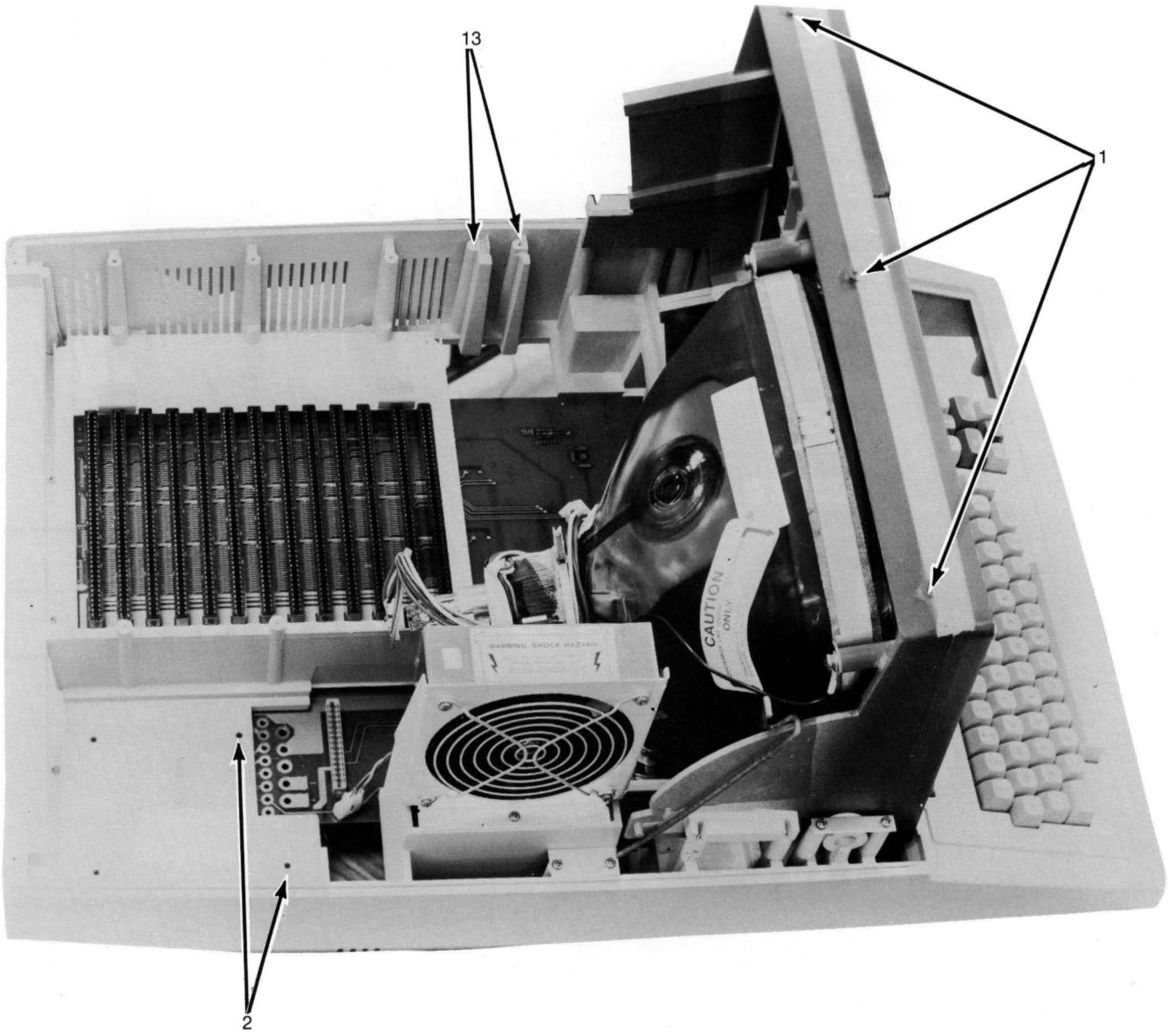


Figure 6-2. Mainframe Attach Screw Locator (Sheet 4 of 7)

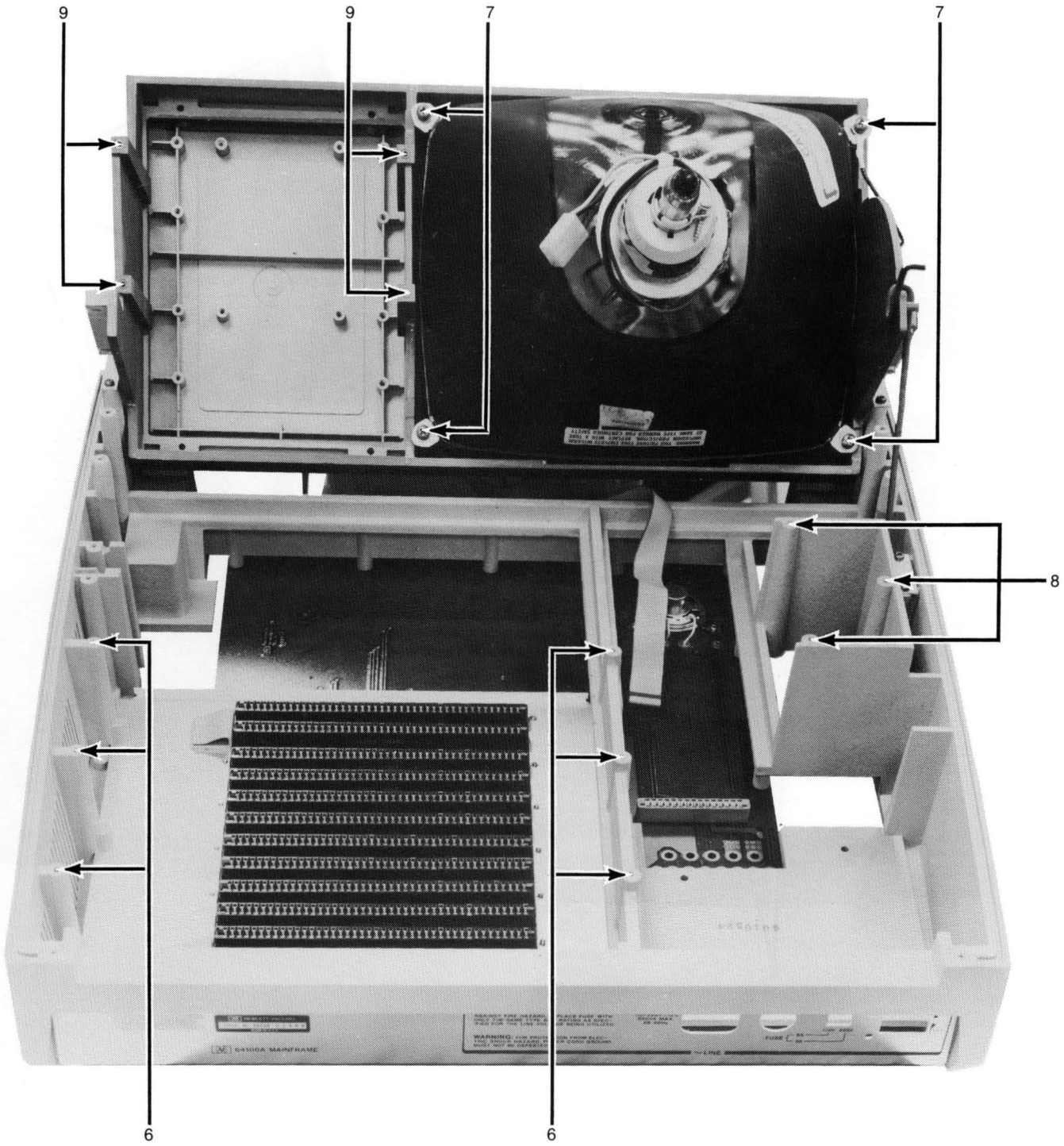


Figure 6-2. Mainframe Attach Screw Locator (Sheet 5 of 7)

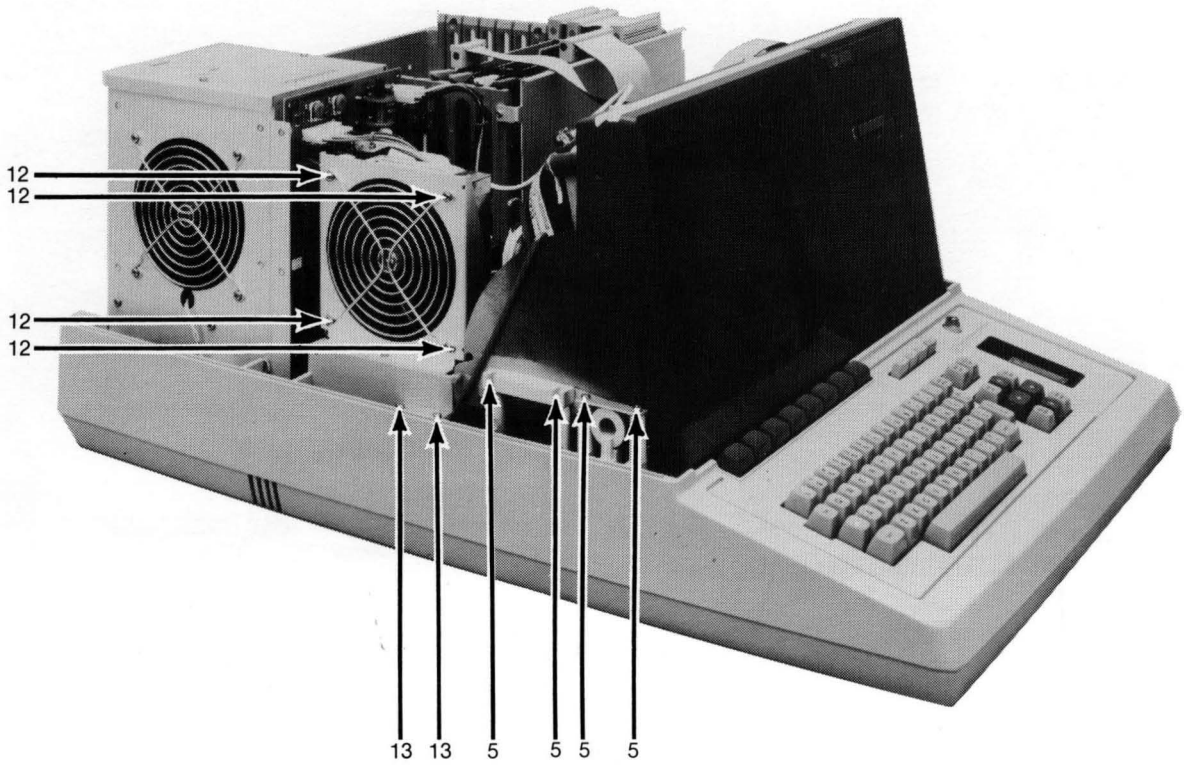
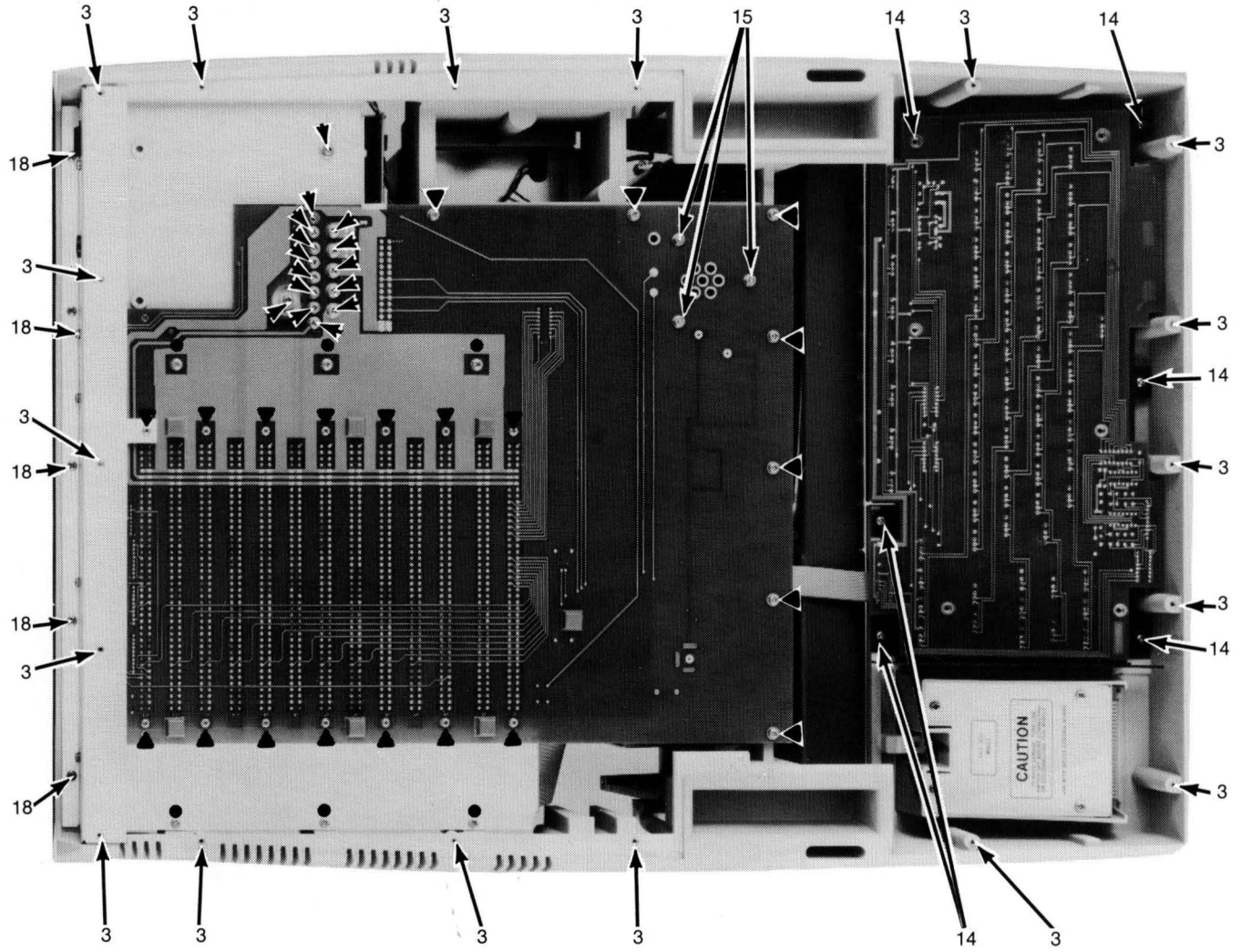


Figure 6-2. Mainframe Attach Screw Locator (Sheet 6 of 7)



SYMBOL KEY: ▲ - Screw, 16

● - Screw, 17

◄ - Screw, 2

Figure 6-2. Mainframe Attach Screw Locator (Sheet 7 of 7)

Table 6-4. Attach Screw Index

Item (see figure 6-2)	Description and Quantity of Items
1	Top Cover attach screws (5)
2	Power Supply attach screws (2) (plus 12 electrical connections; see PWR SUPP Tab)
3	Bottom Cover attach screws (18)
4	Prom Programmer hold-down thumbscrew (1)
5	Display Bezel attach screws (8)
6	Card cage attach screws (6)
7	CRT mounting screws (4)
8	Fan mounting screws (3)
9	Tape Transport and Floppy Drive mounting screws (4)
10	Power supply access port (2)
11	Rear-panel PC board mounting screws (4)
12	Fan Shroud attach screws (7)
13	Support Spring attach screws (4)
14	Keyboard mounting screws (6)
15	Beeper Speaker mounting screws (3)
16	Motherboard mounting screws (21)
17	Motherboard Top Plate mounting screws (6)
18	Rear-panel attach screws (10)
19	State/Timing Grounding Clips (2 or 4)

SECTION VII

MANUAL BACKDATING

7-1. INTRODUCTION.

7-2. This section contains information for adapting this manual to Mainframe units with earlier serial prefix numbers.

7-3. MANUAL CHANGES.

7-4. This manual applies directly to the instrument having the same serial prefix shown on the manual title page. If the serial prefix of the instrument is not the same as the one on the title page, find your serial prefix in table 7-1 and make the changes to the manual that are listed for that serial prefix. When making changes listed in table 7-1, make the change with the highest number first. Example: if backdating changes 1, 2, and 3 are required for your serial prefix, do change 3 first, then change 2, and finally change 1. If the serial prefix of the instrument is not listed either in the title page or in table 7-1, refer to an enclosed MANUAL CHANGES sheet for updating information. Also, if a MANUAL CHANGES sheet is supplied, make all indicated ERRATA corrections.

Table 7-1. Serial No. vs Manual Change No.

Serial Prefix	Make Changes	Affects

7-5. This chapter has no backdating information for the mainframe at the publication date of this manual.

SECTION VIII

SERVICE

8-1. BLOCK DIAGRAM DESCRIPTION. (see figure 8-1)

8-2. The 64100A basic Mainframe is comprised of the following functional areas:

a. Power Supply
b. Keyboard and Softkeys
c. CRT Display
d. Cardcage

1) Central Processor Unit PCB
2) Input/Output PCB
3) Display Controller and Driver PCB's

e. Rear Panel PCB
f. Bus Cabling
g. Motherboard (signal and power distribution)

8-3. In addition to the above basic functions, the following options can be added:

a. Floppy Disc System
b. PROM Programmer
c. Emulation Memory
d. Emulation Memory Control
e. Emulation Control
f. Logic Analyzer

8-4. The items listed in the first list are mandatory in order to have an operating system. These functions are shown on the left side of figure 8-1. The items listed in the second list (options) are shown on the right side of figure 8-1. A brief functional description of each of these items and how they interrelate is presented in the following paragraphs.

8-5. CENTRAL PROCESSOR UNIT (CPU). The CPU PC board contains a 16-bit microprocessor that controls the execution of software/firmware instructions and also: (1) services interrupt requests from the various external peripheral devices (e.g., mass storage disc and line printer), (2) services interrupt requests from the I/O interface circuits (e.g., RS-232, HP-IB, floppy disc system, emulators, and time-interval monitoring circuits), (3) provides the basic timing for the overall 64100A system, and (4) controls the transfer of data and instructions along two independent 16-bit buses (I/O and the IDA buses). Additionally, the CPU board stores programs for "boot-up" and performance verification in an array of on-board ROM's. The CPU's scratch-pad memory is located on the Display Controller PC board.

8-6. INPUT/OUTPUT (I/O). The I/O PC board contains the necessary circuits for: (1) processing the various interrupt requests and informing the CPU that an interrupt condition exists, (2) providing the necessary "hand-shake" operations with RS-232C and HP-IB peripheral devices (e.g., the mass storeage disc, line printer or teletype), (3) decoding instructions from the CPU and thereby providing a means by which the CPU can select specific circuits or peripheral devices to communicate with, and (4) providing an audible alarm to indicate when certain events have occurred.

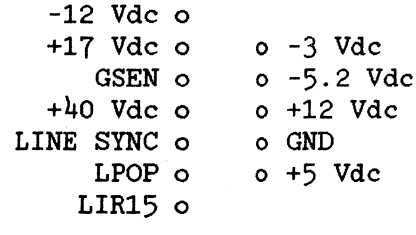
8-7. DISPLAY CONTROLLER, DRIVER AND CRT. The display section of the 64100A system consists of the Display Controller and Display Driver PC boards and the CRT. The Display Controller provides the CPU with "scratch-pad" memory capability via an array of random-access (RAM) read/write memory chips. In addition, it generates the various video control signals for displaying system operation on the CRT display. The Display Driver PC board develops the necessary sync, drive and high voltage signals for creating the CRT display.

8-8. REAR PANEL. The Rear Panel PC board contains: (1) operator-controlled switches for controlling the mode of operation of the 64100A Mainframe, (2) two RS-232 interface connectors; one for when the Mainframe is serving as a "modem" and one for when it is serving as a "terminal", (3) two sets of RS-232 current loop (i.e., teletype) input/output terminals, (4) a HP-IB interface connector, and (5) a "loop-back" circuit for testing the RS-232 circuits.

8-9. KEYBOARD. The 64100A Mainframe uses a keyboard that provides the operator with three basic means of communicating with the 64000 system: (1) a 77-character ASCI-II typewriter format basic keyboard, (2) a set of edit keys, and (3) a set of "softkeys" for increasing the versitility and "friendliness" of the system during system development operations and Mainframe self-testing.

8-10. MAINFRAME SIGNAL DISTRIBUTION. Two methods are used to distribute and route the various power, control and data signals throughout the 64100A Mainframe: (1) a printed circuit Motherboard and (2) a system of ribbon cables. The Motherboard, however, is the primary vehicle for distributing power and most of the data and control signals to and from the various PC boards in the Mainframe cardcage.

8-11. The Mainframe Power Supply is mounted directly to the Motherboard by means of 12 screws that also serve as electrical connections between the power supply and the Motherboard. The screw pattern and the associated electrical signals are shown below:



Power Supply Connections (Bottom View)

8-12. The appropriate power signals are routed to the Mainframe cardcage and also to the Display Drive PCB (via J14) and the Keyboard PCB (via J15). The Power Supply provides seven voltages (plus signal ground) and although all seven voltages are routed to each of the 13 PC boards in the cardcage, not all of the voltages are used by each card type that can be installed. The 64100A block diagram (figure 8-1) and table 8-1 show the voltages used by the various card types. Also, a component locator is given for the motherboard (figure 8-2).

Table 8-1. Card-Type vs Supply Voltage

VDC	I/O	DISP CONT	CPU	KYBD	DISP DVR	TACO/ FLOPPY	PROM PRGR CONT	EMUL MEM	EMUL CONT	MEM	ANAL	EMUL CONT
-3	0	0	0	0	0	0	0	0	0		0	0
+5	X	X	X	X	0	X	X	X	X		X	X
-5	X	X	X	0	0	X	X	0	0		X	X
+12	X	X	X	0	X	X	X	0	0		0	X
-12	X	0	0	0	0	X	X	0	0		0	0
+17	0	0	0	0	0	X/0	0	0	0		0	0
+40	0	0	0	0	0	0	X	0	0		X	0

NOTE:
"X" Indicates Voltage Used
"0" Indicates No Voltage Used

8-13. As with the power supply signals, the control and data signals that are distributed to the cardcage are also (in most cases) routed to the same pin location (number) in each of the 13 card slots (see Table 8-5). Of course, not all signals are used by each cardtype. Thus, if a particular PC board does not use a certain signal that is tied to pin number 20, for example, this is handled by simply creating a dead-end at pin 20 (i.e. there is no conductive path on the PCB). In this manner the PC boards can be interchanged freely (except for the first three slots) without fear of the signals being incompatible with the board. Table 8-5 shows the signal distribution for the cardcage; it does not show the card-type vs. signal relationship since this can be found from the appropriate circuit schematics.

8-14. SIGNAL ROUTING OFF THE MOTHERBOARD. For signals that must leave the Motherboard or the PC boards loaded in the cardcage, a series of ribbon cables and connectors located on the Motherboard are used.

8-15. DISPLAY DRIVER CONNECTOR J14. The Display Driver PCB receives its signals by being plugged directly into J14 which is located on the Motherboard immediately in front of the power supply. The signal vs. pin number is shown in table 8-2.

Table 8-2. Display Driver Connector J14 Signals

Pin No.	Signal	Pin No.	Signal
1	Sig. Gnd.	16	LVID
2	Sig. Gnd.	17	NC
3	Sig. Gnd.	18	NC
4	Sig. Gnd.	19	LVSYN
5	+5 Vdc	20	LVSYN
6	-5 Vdc	21	NC
7	-5 Vdc	22	NC
8	-5 Vdc	23	LHSYN
9	NC	24	LHSYN
10	NC	25	NC
11	LIVID	26	NC
12	LIVID	27	+12 Vdc
13	HDE	28	+12 Vdc
14	HDE	29	+12 Vdc
15	LVID	30	+12 Vdc

8-16. KEYBOARD CONNECTOR J15. The Keyboard receives its signals via a ribbon cable plugged into J15 (on the Motherboard) directly below the neck of the CRT. The signal vs. pin number is shown in table 8-3.

Table 8-3. Keyboard Connector J15 Signals

Pin No.	Signal	Pin No.	Signal
1	LPST	9	Gnd.
2	NC	10	NC
3	HKA2	11	LKA3
4	HKA6	12	LKBCLK
5	HKA5	13	HKA3
6	HKA4	14	HKDN
7	HKA1	15	HKA0
8	GND	16	(No Name)

8-17. CONNECTOR J16. Four test signals from cardcage connector pins 73, 75, 77 and 78 are routed through J16 (at rear of Motherboard) to the four BNC connectors on the Rear-panel. Although all four like-numbered pins in all card slots are tied together, typically only the LTP and LMC signals, from the analyzer PCB, on pins 78 (BNC port 1) and 77 (BNC port 2), respectively, are used. Table 8-4 shows the pin assignment of J16.

Table 8-4. BNC Connector J16 Signals

J16 Pin No.	Cardcage Pin No.	Destination	Signal
1	78	BNC 1	LTP
2	1,2		GND
3	77	BNC 2	LMC
4	1,2		GND
5	75	BNC 3	Not Used
6	1,2		GND
7	73	BNC 4	Not Used
8	1,2		GND

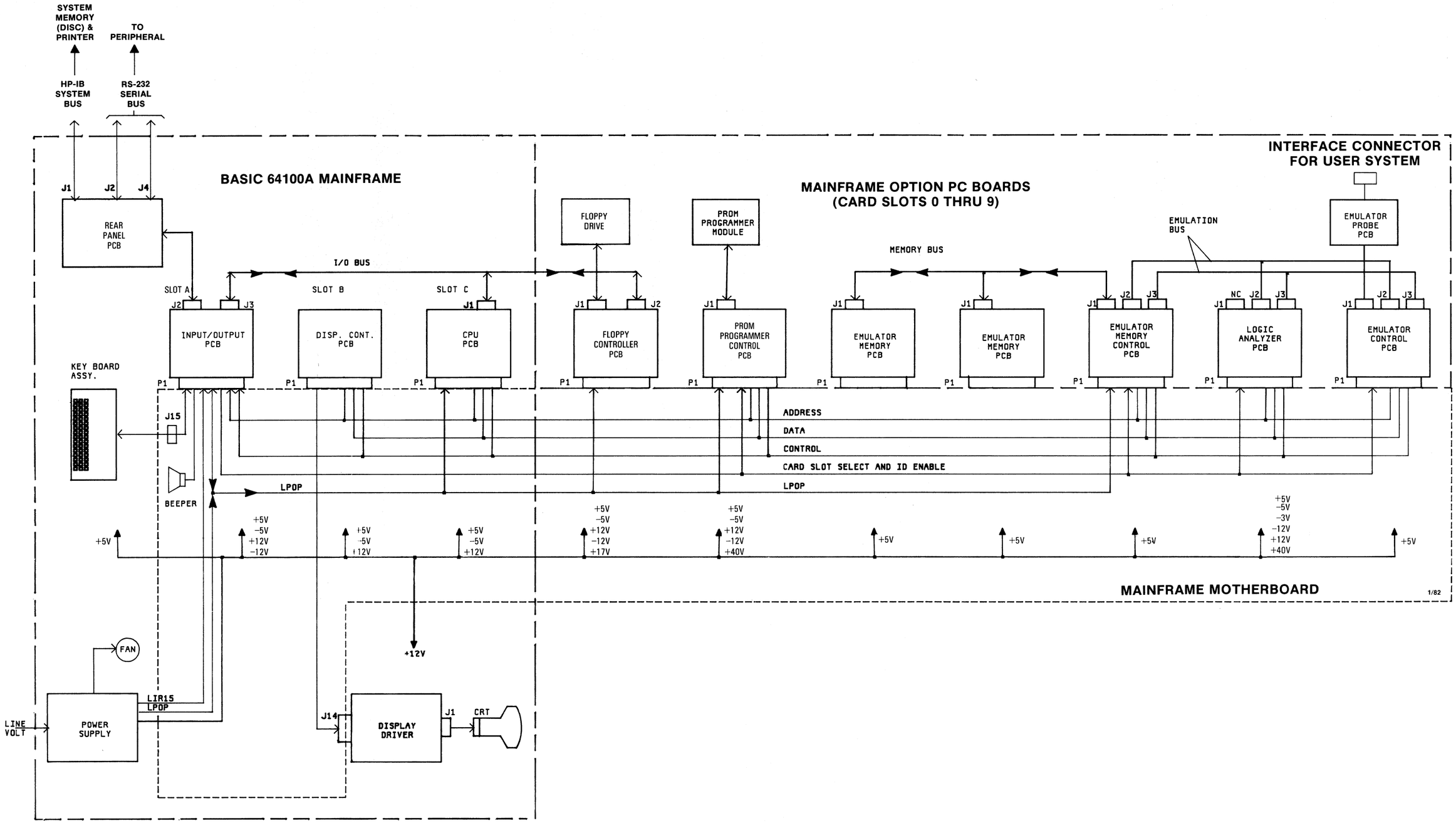


Figure 8-1.
Mainframe Simplified Block Diagram
MF 8-6

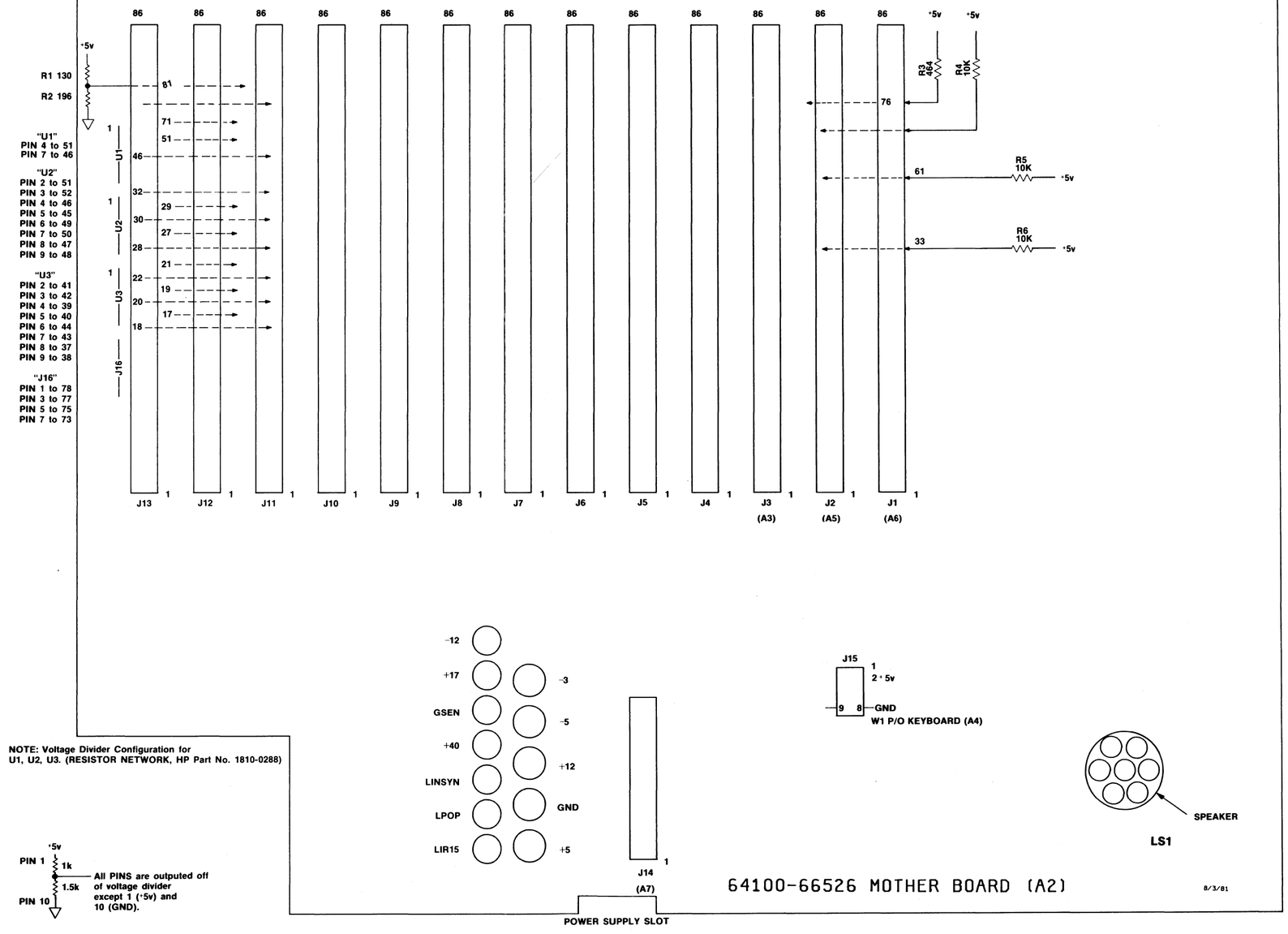
SIGNAL MNEMONIC	PIN#	J1	J2	J3	J4	J5	J6	J7	J8	J9	J10	J11	J12	J13
GND	1	X	X	X	X	X	X	X	X	X	X	X	X	X
GND	2	X	X	X	X	X	X	X	X	X	X	X	X	X
+5	3	X	X	X	X	X	X	X	X	X	X	X	X	X
+5	4	X	X	X	X	X	X	X	X	X	X	X	X	X
-5	5	X	X	X	X	X	X	X	X	X	X	X	X	X
-5	6	X	X	X	X	X	X	X	X	X	X	X	X	X
-5	7	X	X	X	X	X	X	X	X	X	X	X	X	X
-5	8	X	X	X	X	X	X	X	X	X	X	X	X	X
-3	9	X	X	X	X	X	X	X	X	X	X	X	X	X
-3	10	X	X	X	X	X	X	X	X	X	X	X	X	X
-12	11	X	X	X	X	X	X	X	X	X	X	X	X	X
-12	12	X	X	X	X	X	X	X	X	X	X	X	X	X
+12	13	X	-12	X	X	X	X	X	X	X	X	X	X	X
+12	14	X	-12	X	X	X	X	X	X	X	X	X	X	X
GND	15	X	X	X	X	X	X	X	X	X	X	X	X	X
+17	16	X	X	X	X	X	X	X	X	X	X	X	X	X
+40	17	X	X	X	X	X	X	X	X	X	X	X	X	X
NC	18	X	X	X	X	X	X	X	X	X	X	X	X	X
LA0	19	J15-10	X	X	X	X	X	X	X	X	X	X	X	X
LA1	20	J15-11	X	X	X	X	X	X	X	X	X	X	X	X
LA2	21	J15-12	X	X	X	X	X	X	X	X	X	X	X	X
LA3	22	J15-13	X	X	X	X	X	X	X	X	X	X	X	X
LA4	23	J15-14	X	X	X	X	X	X	X	X	X	X	X	X
LA5	24	J15-15	X	X	X	X	X	X	X	X	X	X	X	X
LA6	25	J15-16	X	X	X	X	X	X	X	X	X	X	X	X
LA7	26	J15-1	X	X	X	X	X	X	X	X	X	X	X	X
LA8	27	J15-3	X	X	X	X	X	X	X	X	X	X	X	X
LA9	28	J15-4	X	X	X	X	X	X	X	X	X	X	X	X
LA10	29	J15-5	X	X	X	X	X	X	X	X	X	X	X	X
LA11	30	J15-6	X	X	X	X	X	X	X	X	X	X	X	X

SIGNAL MNEMONIC	PIN#	J1	J2	J3	J4	J5	J6	J7	J8	J9	J10	J11	J12	J13
LA12	31	J15-7	X	X	X	X	X	X	X	X	X	X	X	X
LA13	32	X	X	X	X	X	X	X	X	X	X	X	X	X
LA14	33	X	X	X	X	X	X	X	X	X	X	X	X	X
LA15	34	X	X	X	X	X	X	X	X	X	X	X	X	X
GND	35	X	X	X	X	X	X	X	X	X	X	X	X	X
GND	36	X	X	X	X	X	X	X	X	X	X	X	X	X
LD0	37	J4-72	X	X	X	X	X	X	X	X	X	X	X	X
LD1	38	J5-72	X	X	X	X	X	X	X	X	X	X	X	X
LD2	39	J6-72	X	X	X	X	X	X	X	X	X	X	X	X
LD3	40	J7-72	X	X	X	X	X	X	X	X	X	X	X	X
LD4	41	J8-72	X	X	X	X	X	X	X	X	X	X	X	X
LD5	42	J9-72	X	X	X	X	X	X	X	X	X	X	X	X
LD6	43	J10-72	X	X	X	X	X	X	X	X	X	X	X	X
LD7	44	J11-72	X	X	X	X	X	X	X	X	X	X	X	X
LD8	45	J12-72	X	X	X	X	X	X	X	X	X	X	X	X
LD9	46	J13-72	X	X	X	X	X	X	X	X	X	X	X	X
LD10	47	S	X	X	X	X	X	X	X	X	X	X	X	X
LD11	48	S	X	X	X	X	X	X	X	X	X	X	X	X
LD12	49	HDE	X	X	X	X	X	X	X	X	X	X	X	X
LD13	50	X	X	X	X	X	X	X	X	X	X	X	X	X
LD14	51	X	X	X	X	X	X	X	X	X	X	X	X	X
LD15	52	X	X	X	X	X	X	X	X	X	X	X	X	X
GND	53	X	X	X	X	X	X	X	X	X	X	X	X	X
GND	54	X	X	X	X	X	X	X	X	X	X	X	X	X
LHSYN	55					J14 PINS 23 & 24								
LVSYN	56					J14 PINS 19 & 20								
LVID	57					J14 PINS 15 & 16								
LIVID	58				HDE J14 PIN 13 & 14	J14 PINS 11 & 12								
GND	59	X	X	X	X	X	X	X	X	X	X	X	X	X
GND	60	X	X	X	X	X	X	X	X	X	X	X	X	X

SIGNAL MNEMONIC	PIN#	J1	J2	J3	J4	J5	J6	J7	J8	J9	J10	J11	J12	J13
LBYTE	61	X	X	X	X	X	X	X	X	X	X	X	X	X
LUPB	62	X	X	X	X	X	X	X	X	X	X	X	X	X
LSTM	63	X	X	X	X	X	X	X	X	X	X	X	X	X
LSTB	64	X	X	X	X	X	X	X	X	X	X	X	X	X
LWRT	65	X	X	X	X	X	X	X	X	X	X	X	X	X
LMSYN	66	X	X	X	X	X	X	X	X	X	X	X	X	X
LID	67	X	X	X	X	X	X	X	X	X	X	X	X	X
LMAP1	68	X	X	X	X	X	X	X	X	X	X	X	X	X
LMAP2	69	X	X	X	X	X	X	X	X	X	X	X	X	X
LMAP3	70	X	X	X	X	X	X	X	X	X	X	X	X	X
LIRI	71	X	X	X	X	X	X	X	X	X	X	X	X	X
LSEL	72	X	X	X	X	J1-37	J1-38	J1-39	J1-40	J1-41	J1-42	J1-43	J1-44	J1-45	J1-46
BNC1	73		LIR15							J16 PIN 9				
LOPCODE	74													
BNC2	75		LINESYNC							J16 PIN 5				
LPOP	76	X	X	X	X	X	X	X	X	X	X	X	X	X
	77	X	X	X						J16 PIN 3				
LSCLK1	78	X	X	X						J16 PIN 1				
GND	79	X	X	X	X	X	X	X	X	X	X	X	X	X
GND	80	X	X	X	X	X	X	X	X	X	X	X	X	X
L25MHZ	81	X	X	X	X	X	X	X	X	X	X	X	X	X
	82	X	X	X	X	X	X	X	X	X	X	X	X	X
+5	83	X	X	X	X	X	X	X	X	X	X	X	X	X
+5	84	X	X	X	X	X	X	X	X	X	X	X	X	X
GND	85	X	X	X	X	X	X	X	X	X	X	X	X	X
GND	86	X	X	X	X	X	X	X	X	X	X	X	X	X

NOTE:
"X" INDICATES PIN CONNECTIONS BETWEEN J1 THROUGH J13, OTHERS ARE CONNECTED AS INDICATED.

NOTE: For R1-R5, U1-U3, and J16, each pin that attaches to J13/J1 goes all the way through J1-J13.



NOTE: Voltage Divider Configuration for U1, U2, U3. (RESISTOR NETWORK, HP Part No. 1810-0288)

Figure 8-2.
A2 Motherboard Component Locator
MF 8-7

SERVICE MANUAL

MODEL 64100A

CENTRAL PROCESSING UNIT (CPU)

Manual Part No.: Part of Mainframe Manual
Microfiche Part No.: See Mainframe Manual

Table of Contents

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List of Illustrations

List of Tables

SECTION I

GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. This Chapter contains the information for servicing the Central Processing Unit (CPU) in the Model 64100A Logic Development Station. The CPU cannot operate independently, and has no operator functions. Operation instructions for the Logic Development Station, and the System are provided in separate operating manuals supplied with the system.

1-3. INSTRUMENTS COVERED BY THIS MANUAL.

1-4. The CPU Board is not serialized, nor is it assigned a repair number. Because the CPU is a part of the Logic Development Station (Mainframe), some changes on the CPU Board can cause the serial number of the Logic Development Station (Mainframe) to change. The history of serial number prefix changes is recorded in Section VII of the Mainframe Chapter. The details of a change for a given assembly can be found in Section VII of the appropriate Tab, i.e., Mainframe, CPU, Display Control and Driver, Input/Output, or Power Supply.

1-5. RELATED DOCUMENTS.

1-6. The following documents provide additional information pertaining to the use of the HP 64000 system. It is recommended that the System Overview Manual be referred to.

System Overview Manual

System Software Reference Manual

Installation and Configuration Manual

Editor Manual

1-7. DESCRIPTION.

* The CPU has no operator functions.

* The CPU communicates directly with the Display Controller and Input/ Output boards.

* The CPU's scratch pad memory is provided by the RAM located on the Display Controller board.

* The path for the CPU to communicate with periphial devices is provided by the Input/Output board.

* The programs for boot-up and Performance Verification are stored in the ROMs located on the CPU Board.

* The CPU Board generates the timing and control signals for the Microprocessor and its associated bus circuits.

* The Microprocessor is clocked at 6.25MHz. The clock originates on the Display Control board.

* The CPU Board contains the CPU Bus, consisting of a 16-bit bi-directional data bus, a 16-bit address bus, and several control lines.

* The CPU Board contains the I/O bus, consisting of a 16-bit bi-directional data bus, a 4-bit address bus, and several control lines.

* The CPU bus and I/O bus are controlled independently by the Microprocessor.

* The Microprocessor is located on the CPU Board. The microprocessor is a 16-bit machine with separate multiplexed instruction/data/address and I/O busses.

* The SA latch located on the CPU board is used for determining that the ROM outputs are operational. To use this latch while troubleshooting, see section IV.

SECTION II

INSTALLATION

2-1. INTRODUCTION.

2-2. The CPU Board is shipped from the factory installed in the Logic Development Station (Mainframe). The CPU Board can only be purchased as a replacement part and installation is described in the following paragraph.

2-3. CARD CAGE LOCATION.

2-4. When the CPU Board is removed from the Mainframe, it must always be reinstalled in the third position from the front of the Card Cage (identified by the blue board extractors and blue CPU label on the Card Cage).

WARNING

When removing or installing the CPU Board, the Mainframe A.C. line power must be turned off!

SECTION III

OPERATION

3-1. GENERAL.

3-2. The CPU has no operator functions. The CPU is both physically and operationally part of the Mainframe. For the operation of the Mainframe, see section III of the Mainframe Chapter.

SECTION IV

PERFORMANCE VERIFICATION AND TROUBLESHOOTING

4-1. INTRODUCTION.

4-2. This section provides Performance Verfication for the CPU using Signature Analysis.

4-3. In the event the ROM Test fails, you will be directed to this portion of the Performance Verification from the Mainframe Chapter.

4-4. There is no separate Performance Verification available that will check the operation of the CPU Board alone. Refer to the Mainframe Chapter of this manual for an explanation of how to initiate the Performance Verification for the Mainframe. Optional models, i.e., PROM Programmer, Emulators, etc., have their own Performance Verifications.

4-5. If the ROM Test fails, and replacing the ROM that was displayed as bad does not correct the problem, then the SA ROM loop (counting sequence) must be used to troubleshoot the CPU board.

4-6. If a count sequence can not be produced then the Microprocessor or its control circuits are not operating correctly. They must be repaired by using an Oscilloscope and/or Logic Probe.

4-7. CPU ROM TESTS.

4-8. The ROM test sequence used during power-up and performance verification is the same. However, each test will display a ROM failure differently. The following ROM test procedures will describe each test and how to interpret the given failure.

4-9. POWER-UP ROM TEST.

Purpose:

The ROM test verifies that all of the firmware in ROM used for boot-up and performance verification is good. The test also checks that the CPU is able to access ROM memory via the bi-directional address and data buses.

Area Tested:

All ROMs, the multiplexed memory Address/Data bus to ROM, the address latches and data buffers, and the CPU and its associated timing and control circuitry.

Operation:

a. This test executes a checksum on each of the ROMs as long as the kernal of good ROM needed to run the test is operational.

b. If an error is detected then a bit is set in the error mask.

c. The error mask is then used to output an error message to the screen stating a ROM failure, the address range of the failure, and the byte (0 or 1).

d. If a failure is detected, the test will loop continuously.

e. On failures, the power up ROM test will display the following error message assuming that the kernal of ROM required to run the power up test is good:

```
SELF-TEST FAILURE <----------< blinking
ROM TEST:
FAILING ADDRESS RANGE       BYTE(S)
--------------------        -------
     XXXX-XXXX                 XX
```

f. Use the table below to determine which ROM unit number is failing. Note that the error message might give an address range that includes more than one ROM. SA loop A might be necessary to isolate the fault (see Table 4-2).

Failed Addresses	Byte	Failed ROM #	
0020-1FFF	0	U9	Lower 8K ROM
0020-1FFF	1	U10	
2000-3BFF	0	U9	Upper 8K ROM
2000-3BFF	1	U10	

g. When the ROM test passes, the mainframe will beep three times and begin the RAM test.

4-10. ROM TEST DURING PV.

Purpose:

The ROM test verifies that all of the firmware in ROM used for boot-up and performance verification is good. The test also checks that the CPU is able to access ROM memory via the bi-directional address and data buses.

Area Tested:

All ROMs, the multiplexed memory Address/Data bus to ROM, the address latches and data buffers, and the CPU and its associated timing and control circuitry.

Operation:

a. This test is the same ROM test which is performed during power-up, but will display a different error message.

b. Each test takes aproximately 1/2 second.

c. A routine reads the ROM contents, computes a checksum and compares it with a checksum also located in ROM.

d. Assuming that the kernal of ROM required to run the ROM TEST is operational, the test will attempt to output an error mask if the test fails. The mask is a 16 bit word as follows:

```
IC MASK = 000000000000ABCD
          15--------------0
```

A "1" in any of the bits signifies a bad ROM where:

D = ROM # 0 = lower byte of lower 8K ROM (U9)
C = ROM # 1 = upper byte of lower 8K ROM (U10)
B = ROM # 0 = lower byte of upper 8K ROM (U9)
A = ROM # 1 = upper byte of upper 8K ROM (U10)

e. Note that the error message might give an address range that includes more than one ROM. SA loop A might be necessary to isolate the fault (see Table 4-2).

4-11. TROUBLESHOOTING.

4-12. In the event that a critical component has failed, and the performance Verification is not able to run at all, the Microprocessor will most likely be running in some unknown loop, or will be executing random code (lost). If this should happen the Microprocessor can be forced into a counting loop by changing the jumpers E4 and E5 to the test position, and removing CPU data bus buffers U27 and U28. When the CPU is in the counting mode and the Mainframe is powered up, the Microprocessor begins counting at 0020 Hex and counts to 3C00 Hex on the 16 bit address line. Stable signatures will then be on the data bus for troubleshooting.

4-13. LOOP A SIGNATURES

4-14. The loop A signature analysis table given in this section should be used when a ROM failure is unreadable or no display is present. Follow the setup procedure as explained in table 4-1, loop A signature analysis. Using the CPU schematic as a reference and the signatures shown for loop A, begin checking the signatures on the ROM data buffer inputs. If a bad signature is found, begin pulling out the ROMs as indicated in table 4-2.

4-15. If any of these signatures were not obtained and the Microprocessor does not appear to be working, check the power supply voltages. If they are correct then force the Microprocessor address lines into the counting loop as described in paragraph 4-12.

4-16. COUNTING MODE.

4-17. Following are some things to look for with an Oscilloscope or Logic Probe, if "Vh" for LOOP A is incorrect.

4-18. In the "counting" mode you should be able to observe data changing on the Low Instruction/Data/Address Bus (LIDA). High Address Latch (HADL) should be changing states. The falling edge of HADL can be used to trigger an oscilloscope to observe the Address Bus on the outputs of U32 and U33. HADL is derived from Low Start Memory which indicates the information on the LIDA Bus is valid.

* The output of the Address Bus Inverters, U25, U26, and part of U34 can be observed using the falling edge of HADL for triggering.

* Using Low ROM address (LRADDR) as a trigger for an Oscilloscope, you should be able to observe U1's outputs changing state. These are the ROM chip selects.

* Using Low Data Buffer (LDBUF) as a trigger you can observe the outputs of the ROMs, and the outputs of the Data Bus Buffers, U27 and U28.

* If the Microprocessor is not outputing a count sequence, then check the Timing, Control, and Clock Circuits using an oscilloscope.

* The Clock is two nonoverlapping waveforms. Clock frequency is 6.25 MHz.

* Low Power On Pulse (LPOP), pin 11 of the Microprocessor should be high. Push the processor reset switch on the I/O board and LPOP should go low momentarily.

* Low Bus Request (LBR), pin 18 of the Microprocessor should be high.

* Low Unsynchronized Memory Complete (LUMC) can be changing states but should never be high. A high state will cause the Microprocessor to "wait".

* Low Memory Sync (LMSYN) should be high.

* Check the following lines for the state indicated while LPOP is low. During initialization, the indicated states must occur to properly initialize the Microprocessor. If this does not happen correctly, the Microprocessor may not count correctly.

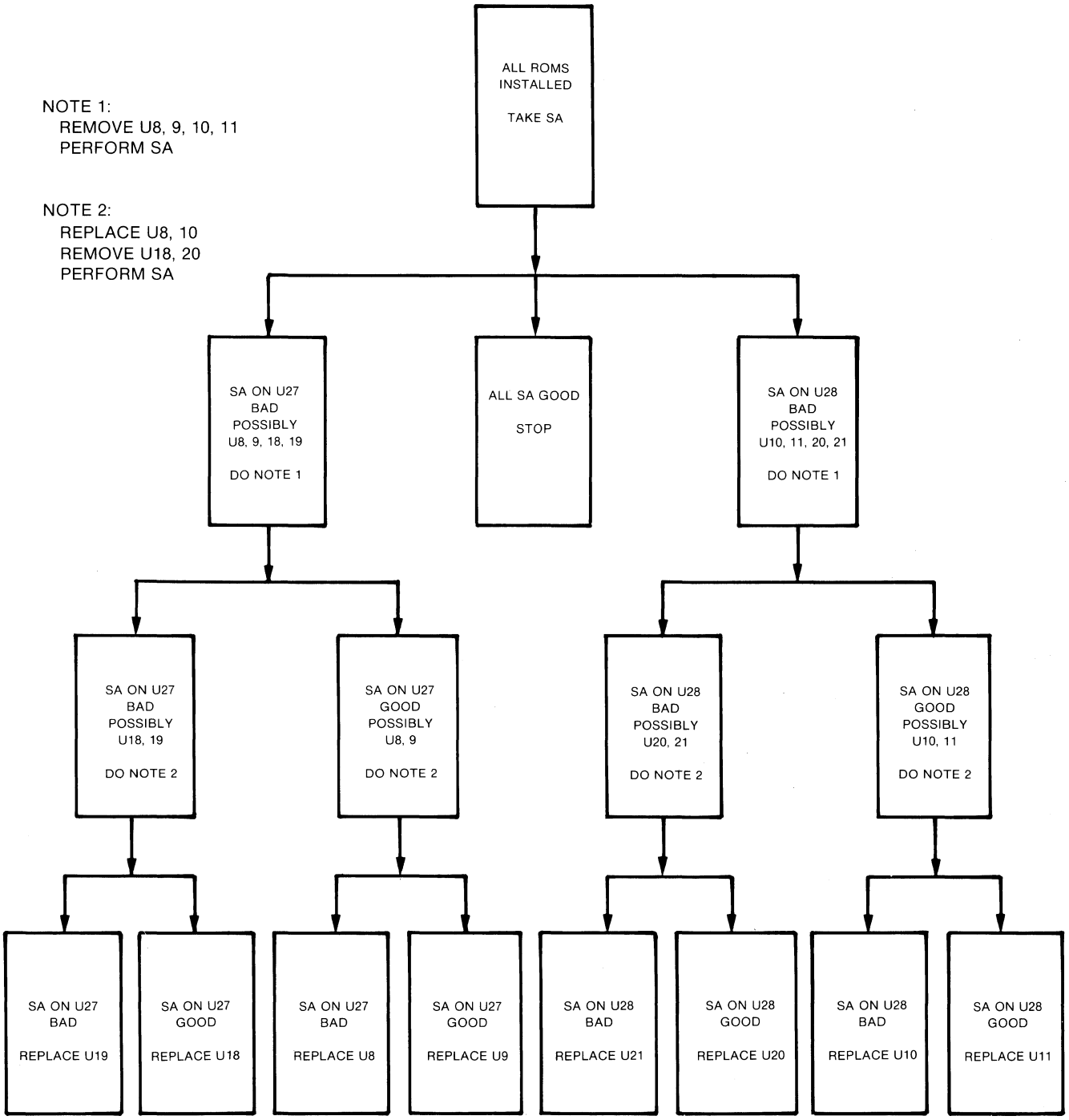
********** High State **********					****** Low State *******
LBR	LSMC	LERA	LUMC	LIDA 2,4-11,14,15	LPBO
LDOUT	LSTM	LINT	HRD		HRAL

Table 4-1. Loop A Signature Analysis

PC Board: CPU/ROM Board
Test failure or circuit: No recognizable display or fails power-up ROM test.
Procedure: Remove Display Driver board.
Move E4 and E5 jumpers to test position.
Remove U27 and U28 (ROM data buffers).
S/A hookup:
START = NEG EDGE CPU BD TP5 (LDBUF)
STOP = NEG EDGE CPU BD TP5 (LDBUF)
CLOCK = POS EDGE CPU BD TP1 (LSTB)
Vh = 15C8
* = Probe Blinking

Node	Sig	Node	Sig	Node	Sig
U1-1	0001	U25-2	U368	U33-2	338C
U1-2	8A0H	U25-4	5127	U33-5	2C4U
U1-3	0U39	U25-6	PUA1	U33-6	H2PC
U1-4	H1C1	U25-8	2F39	U33-9	54H0
U1-5	FC30	U25-10	476C	U33-12	9UC5
U1-6	4P04	U25-12	3927	U33-15	1A81
U1-7	413F			U33-16	15C8*
U1-11	15C8	U26-2	8638	U33-19	15C8*
U1-12	0001	U26-4	1P06		
U1-13	0001	U26-6	4168	U34-5	2633
U1-14	0000	U26-8	F753	U34-9	8A0H
U1-15	0000*	U26-10	3PU7		
U2-5	15C8	U32-2	3981		
		U32-5	UA19		
		U32-6	449U		
		U32-9	P6H0		
		U32-12	52H3		
		U32-15	2F9U		
		U32-16	9380		
		U32-19	0CCP		
ALL ROMs INSTALLED		U8, 9, 10, 11 REMOVED		U9, 11, 18, 20 REMOVED	
U27-2	FH75	U27-2	9P1C	U27-2	46H6
U27-4	H7CH	U27-4	A9UA	U27-4	6CUU
U27-6	HC41	U27-6	H7A0	U27-6	1959
U27-8	2UCU	U27-8	5910	U27-8	6317
U27-11	F2H7	U27-11	8571	U27-11	521P
U27-13	5296	U27-13	6969	U27-13	2P47
U27-15	97FC	U27-15	HH4C	U27-15	5U38
U27-17	456H	U27-17	7HU1	U27-17	2H24
U28-2	PPHA	U28-2	FCPH	U28-2	308U
U28-4	417P	U28-4	3HUC	U28-4	693H
U28-6	57F2	U28-6	H205	U28-6	907U
U28-8	6917	U28-8	9AP8	U28-8	P647
U28-11	644F	U28-11	C0U9	U28-11	F10H
U28-13	4862	U28-13	7H98	U28-13	2042
U28-15	A77P	U28-15	CPFP	U28-15	0F08
U28-17	C13F	U28-17	09UH	U28-17	AH79

Table 4-2. ROM Signature Analysis Troubleshooting



SECTION V

ADJUSTMENTS

5-1. INTRODUCTION.

5-2. This section describes the adjustment required to return the +7 volt regulator to normal operating capability after repairs have been made on the CPU board.

5-3. SAFETY REQUIREMENTS.

5-4. Although this instrument has been designed in accordance with international safety standards, general safety precautions must be observed during all phases of operation, service, and repair of the instrument. Failure to comply with precautions listed in the Safety Summary at the front of this manual (Mainframe) or with specific warnings given throughout the manual could result in serious injury or death. Service adjustments should be performed only by qualified service personnel.

5-5. EQUIPMENT REQUIRED.

5-6. A Voltmeter capable of .01 Volt accuracy is required for this Adjustment Procedure.

5-7. +7V ADJUSTMENTS.

5-8. There is only one Adjustment on the Central Processing Unit Board. It is for the Regulator that provides +7V for the Microprocessor.

5-9. The Test Point, labeled +7V, is located in the center of the top edge of the P.C. Board.

5-10. The positive lead of the voltmeter is connected to the +7V Test Point, and the negative lead is connected to ground. R2 (located near the +7V Test Point) is adjusted for +6.7V to +7.3V.

SECTION VI

REPLACEABLE PARTS

6-1. INTRODUCTION.

6-2. This section contains information concerning replaceable parts. Table 6-1 lists abbreviations used in the parts list and throughout the manual. Table 6-2 lists all replaceable parts in reference designator order. Table 6-3 contains the names and addresses that correspond to the manufacturers' five digit code numbers.

6-3. ABBREVIATIONS.

6-4. Table 6-1 lists abbreviations used in the parts list, on the schematics and throughout the manual. In some cases, two forms of the abbreviations are used: one, all in capital letters, and two, partial or no capitals. This occurs because the abbreviations in the parts list are always capitals. However, in the schematics and other parts of the manual, other abbreviation forms are used with both lowercase and uppercase letters.

6-5. REPLACEABLE PARTS LIST.

6-6. Table 6-2 is the list of replaceable parts and is organized as follows:

a. Chassis-mounted parts in alphanumerical order by reference designation.

b. Electrical assemblies and their components in alphanumerical order by reference designation.

c. Miscellaneous parts.

6-7. The information given for each part consists of the following:

a. The Hewlett-Packard part number and the check digit (CD).

b. The total quantity (Qty) in the instrument.

c. The description of the part.

d. A five-digit code that indicates the manufacturer.

e. The manufacturer's part number.

6-8. The total quantity for each part is given only once at the first appearance of the part number in the list.

6-9. For ordering information see Section VI of the Mainframe Tab.

Table 6-1. Abbreviations

REFERENCE DESIGNATORS

A	= assembly	**F**	= fuse	**MP**	= mechanical part	**U**	= integrated circuit
B	= motor	**FL**	= filter	**P**	= plug	**V**	= vacuum, tube, neon bulb, photocell, etc
BT	= battery	**IC**	= integrated circuit	**Q**	= transistor		
C	= capacitor	**J**	= jack	**R**	= resistor	**VR**	= voltage regulator
CP	= coupler	**K**	= relay	**RT**	= thermistor	**W**	= cable
CR	= diode	**L**	= inductor	**S**	= switch	**X**	= socket
DL	= delay line	**LS**	= loud speaker	**T**	= transformer	**Y**	= crystal
DS	= device signaling (lamp)	**M**	= meter	**TB**	= terminal board	**Z**	= tuned cavity network
E	= misc electronic part	**MK**	= microphone	**TP**	= test point		

ABBREVIATIONS

A	= amperes	**H**	= henries	**N/O**	= normally open	**RMO**	= rack mount only
AFC	= automatic frequency control	**HDW**	= hardware	**NOM**	= nominal	**RMS**	= root-mean square
AMPL	= amplifier	**HEX**	= hexagonal	**NPO**	= negative positive zero (zero temperature coefficient)	**RWV**	= reverse working voltage
		HG	= mercury				
BFO	= beat frequency oscillator	**HR**	= hour(s)				
BE CU	= beryllium copper	**HZ**	= hertz	**NPN**	= negative-positive-negative	**S-B**	= slow-blow
BH	= binder head					**SCR**	= screw
BP	= bandpass			**NRFR**	= not recommended for field replacement	**SE**	= selenium
BRS	= brass	**IF**	= intermediate freq			**SECT**	= section(s)
BWO	= backward wave oscillator	**IMPG**	= impregnated	**NSR**	= not separately replaceable	**SEMICON**	= semiconductor
		INCD	= incandescent			**SI**	= silicon
CCW	= counter-clockwise	**INCL**	= include(s)			**SIL**	= silver
CER	= ceramic	**INS**	= insulation(ed)	**OBD**	= order by description	**SL**	= slide
CMO	= cabinet mount only	**INT**	= internal	**OH**	= oval head	**SPG**	= spring
COEF	= coeficient			**OX**	= oxide	**SPL**	= special
COM	= common	**K**	= kilo=1000			**SST**	= stainless steel
COMP	= composition					**SR**	= split ring
COMPL	= complete	**LH**	= left hand	**P**	= peak	**STL**	= steel
CONN	= connector	**LIN**	= linear taper	**PC**	= printed circuit		
CP	= cadmium plate	**LK WASH**	= lock washer	**PF**	= picofarads= 10^{-12} farads	**TA**	= tantalum
CRT	= cathode-ray tube	**LOG**	= logarithmic taper			**TD**	= time delay
CW	= clockwise	**LPF**	= low pass filter	**PH BRZ**	= phosphor bronze	**TGL**	= toggle
				PHL	= phillips	**THD**	= thread
DEPC	= deposited carbon	**M**	= milli=10^{-3}	**PIV**	= peak inverse voltage	**TI**	= titanium
DR	= drive	**MEG**	= meg=10^{6}	**PNP**	= positive-negative-positive	**TOL**	= tolerance
		MET FLM	= metal film			**TRIM**	= trimmer
ELECT	= electrolytic	**MET OX**	= metallic oxide	**P/O**	= part of	**TWT**	= traveling wave tube
ENCAP	= encapsulated	**MFR**	= manufacturer	**POLY**	= polystyrene		
EXT	= external	**MHZ**	= mega hertz	**PORC**	= porcelain	**U**	= micro=10^{-6}
		MINAT	= miniature	**POS**	= position(s)		
F	= farads	**MOM**	= momentary	**POT**	= potentiometer	**VAR**	= variable
FH	= flat head	**MOS**	= metal oxide substrate	**PP**	= peak-to-peak	**VDCW**	= dc working volts
FIL H	= fillister head	**MTG**	= mounting	**PT**	= point		
FXD	= fixed	**MY**	= "mylar"	**PWV**	= peak working voltage	**W/**	= with
						W	= watts
G	= giga (10^{9})	**N**	= nano (10^{-9})	**RECT**	= rectifier	**WIV**	= working inverse voltage
GE	= germanium	**N/C**	= normally closed	**RF**	= radio frequency		
GL	= glass	**NE**	= neon	**RH**	= round head or right hand	**WW**	= wirewound
GRD	= ground(ed)	**NI PL**	= nickel plate			**W/O**	= without

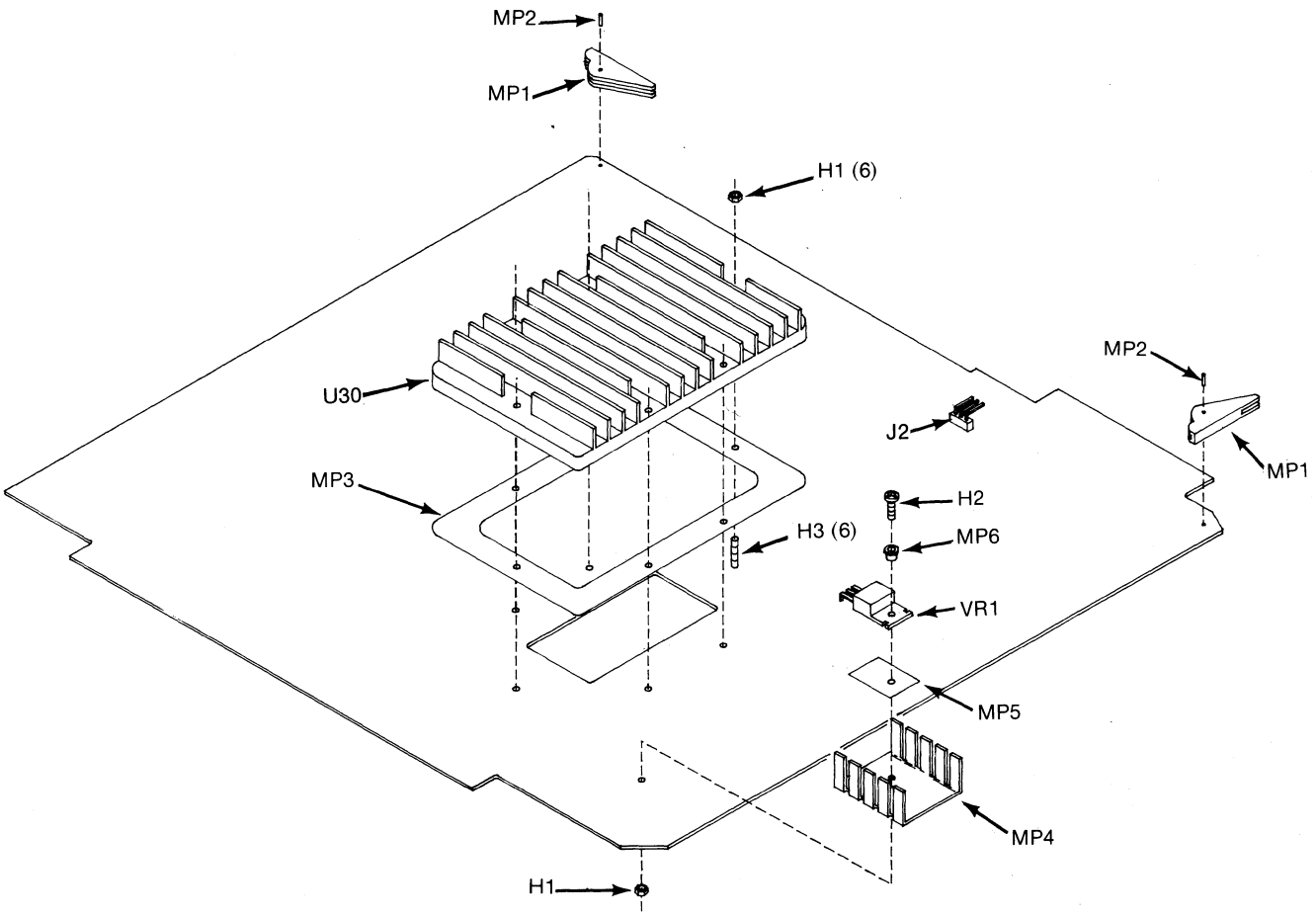


Figure 6-1. Illustrated Parts Breakdown

Table 6-2. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A3	64100-66532	2	1	BOARD ASSEMBLY, CPU	28480	64100-66532
C1	0160-2308	5	1	CAPACITOR-FXD 36PF ±5% 300VDC MICA	28480	0160-2308
C2	0160-5321	8	18	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
C3	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
C4	0160-5321	8		CAPACITOR-FXD .01UF+80-20% 100VDC CER	28480	0160-5321
C5	0160-5321	8		CAPACITOR-FXD .01UF+80-20% 100VDC CER	28480	0160-5321
C6	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
C7	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
C8	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
C9	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
C10	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
C11	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
C12	0160-3470	4		CAPACITOR-FXD .01UF +80-20% 50 VDC CER	28480	0160-3470
C13	0160-3470	4		CAPACITOR-FXD .01UF +80-20% 50 VDC CER	28480	0160-3470
C14	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
C15	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
C16	0140-0200	0	2	CAPACITOR-FXD 390PF ±5% 300VDC MICA	72136	DM15F391J0300WV1CR
C17	0140-0200	0		CAPACITOR-FXD 390PF ±5% 300VDC MICA	72136	DM15F391J0300WV1CR
C18	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
C19	0160-5321	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
C20	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
C21	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
C22	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
C23	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
C24	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
C25	0180-0347	3		CAPACITOR-FXD 10UF ±10% 20VDC TA	56289	150D106X9020B2
C26	0180-0347	3		CAPACITOR-FXD 10UF ±10% 20VDC TA	56289	150D106X9020B2
C27	0180-0116	1		CAPACITOR-FXD 6.8UF ±10% 20VDC TA	28480	0180-0116
C28	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
C29, C30	0180-0347	3		CAPACITOR-FXD 10UF ±10% 20VDC TA	56289	150D106X9020B2
H1	2260-0009	3	7	NUT-HEX-W/LKWR 4-40-THD .094-IN-THK	00000	ORDER BY DESCRIPTION
H2	2200-0143	0	1	SCREW-MACH 4-40 .375-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H3	0360-0679	3	6	TERMINAL-STUD SPCL-STDF PRESS-MTG	28480	0360-0679
J2	1251-4388	9	1	CONNECTOR 3-PIN M POST TYPE	28480	1251-4388
L1	9140-0112	2	1	COIL-MLD 4.7UH 10% Q=33 .155DX .375 LG-NOM	28480	9140-0112
MP1	5040-6069	4	2	EXTRACTOR, BLUE	28480	5040-6069
MP2	1480-0116	8	2	PIN-GRV .062-IN-DIA .25-IN-LG-STL	28480	1480-0116
MP3	09825-67908	8	1	GASKET, MICROPROCESSOR	28480	09825-67908
MP4	1205-0338	4	1	HEAD SINK SGL PLSTC-PWR-C8	28480	1205-0338
MP5	0340-0511	0	1	INSULATOR-XSTR KAPTON	28480	0340-0511
MP6	3050-0791	6	1	INSULATOR-XSTR NYLON	28480	3050-0791
R1	0757-0282	5	1	RESISTOR 221 1% .125W F TC=0±100	24546	C4-1/8-T0-221R-F
R2	2100-3350	5	1	RESISTOR-TRMR 200 10% C SIDE-ADJ 1-TRN	28480	2100-3350
R3	0757-0422	5	1	RESISTOR 909 1% .125W F TC=0±100	24546	C4-1/8-T0-909R-F
R4	0698-3446	3	1	RESISTOR 383 1% .125W F TC=0±100	24546	C4-1/8-T0-383R-F
R5	0757-0200	7	3	RESISTOR 5.62K 1% .125W F TC=0±100	24546	C4-1/8-T0-5621-F
R6	0757-0279	0	2	RESISTOR 3.16K 1% .125W F TC=0±100	24546	C4-1/8-T0-3161-F
R7	0698-3432	7	2	RESISTOR 26.1 1% .125W F TC±0±100	03888	PME55-1/8-T0-26R1-F
R8	0757-0200	7		RESISTOR 5.62K 1% .125W F TC=0±100	24546	C4-1/8-T0-5621-F
R9	0757-0200	7		RESISTOR 5.62K 1% .125W F TC=0±100	24546	C4-1/8-T0-5621-F
R10	0698-3432	7		RESISTOR 26.1 1% .125W F TC=0±100	03888	PME55-1/8-T0-26R1-F
R11	0757-0280	3	4	RESISTOR 1K 1% .125W F TC=0±100	24546	C4-1/8-T0-1001-F
R12	0757-0280	3		RESISTOR 1K 1% .125W F TC=0±100	24546	C4-1/8-T0-1001-F
R13	0757-0280	3		RESISTOR 1K 1% .125W F TC±0±100	24546	C4-1/8-T0-1001-F
R14	0757-0279	0		RESISTOR 3.16K 1% .125W F TC=0±100	24546	C4-1/8-T0-3161-F
R15	0757-0280	3		RESISTOR 1K 1% .125W F TC=0±100	24546	C4-1/8-to-1001-F
TP1 thru 22	0360-0535	0	22	TERMINAL TEST PONT PCB	00000	ORDER BY DESCRIPTION
U1	1820-1281	2	2	IC DCDR TTL LS 2-TO-4-LINE DUAL 2-INP	01295	74LS139
U2	1820-1112	8	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	74LS74
U3	1820-0693	8	3	IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	74S74
U4	1820-0693	8	3	IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	74S74
U5	1820-2024	3	4	IC DRVR TTL LS LINE DRVR OCTL	01295	74LS244
U6	1820-2024	3	4	IC DRVR TTL LS LINE DRVR OCTL	01295	74LS244
U7	1810-0275	1	1	NETWORK RES 10-SIP 1.0K OHM X 9	01121	210A102
U9	64100-80028	1	1	ROM 0	28480	64100-80028
U10	64100-80029	2	1	ROM 1	28480	64100-80029
U12	1820-1243	6	1	IC GATE TTL LS AND TPL 3-INP	01295	SN74LS15N
U13	1820-0693	8		IC FF TTL 8 D-TYPE POS-EDGE-TRIG	01295	74874
U14	1820-1112	8	2	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	74LS74
U15	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	74LS74

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (con't)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U16	1820-1322	2	1	IC GATE TTL 8 NOR QUAD 2-INP	01295	74S02
U17	1810-0276	2	1	NETWORK-RES 10-SIP 1.5K OHM X 9	01121	210A152
U22	1820-1281	2	1	IC DCDR TTL LS 2-TO-4-LINE DUAL 2-INP	01295	74LS139
U23	1810-0280	8	2	NETWORK-RES 10-SIP 10.0K OHM X 9	01121	210A103
U24	1810-0280	8		NETWORK-RES 10-SIP 10.0K OHM X 9	01121	210A103
U25	1820-1199	1	2	IC INV TTL LS HEX 1-INP	01295	74LS04
U26	1820-1199	1		IC INV TTL LS HEX 1-INP	01295	74LS04
U27	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	74LS244
U28	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	74LS244
U29	1820-1204	9	1	IC GATE TTL LS NAND DUAL 4-INP	01295	74LS20
U30	5061-3011	4	1	MICROPROCESSOR W/HEAT SINK	28480	5060-3011
U31	1820-1288	9	1	IC DRVR TTL CLOCK DRVR TTL-TO-MOS 1-INP	04713	MMH0026CL
U32	1820-2102	8	2	IC LCH TTL LS D-TYPE OCTL	01295	74LS373
U33	1820-2102	8		IC LCH TTL LS D-TYPE OCTL	01295	74LS373
U34	1820-1917	1	1	IC BFR TTL LS LINE DRVR OCTL	01295	74LS240
U35	1820-1198	0	1	IC GATE TTL LS NAND QUAD 2-INP	01295	74LS03
U36	1820-0539	1	1	IC BFR TTL NAND QUAD 2-INP	01295	7437
U37	1820-1307	3	1	IC SCHMITT-TRIG TTL S NAND QUAD 2-INP	01295	74S132
VR1	1826-0393	7	1	IC RGLTR.TO=220	27014	LM317T
				MISCELLANEOUS PARTS		
E1 thru E6	8151-0013	9	6	JUMPER CLIP	28480	8151-0013
XU9	1200-0567	1	2	SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0567
XU10	1200-0567	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0567
XU27	1200-0639	8	2	SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
XU28	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639

See introduction to this section for ordering information

Table 6-3. Manufacturers' Codes

Mfr No.	Manufacturer Name	Address		Zip Code
00000	ANY SATISFACTORY SUPPLIER			
01121	ALLEN-BRADLEY CO	MILWAUKEE	WI	53024
01295	TEXAS INSTR INC SEMICOND CMPNT DIV	DALLAS	TX	75222
03888	KDI PYROFILM CORP	WHIPPANY	NJ	07981
04713	MOTOROLA SEMICONDUCTOR PRODUCTS	PHOENIX	AZ	85062
24546	CORNING GLASS WORKS (BRADFORD)	BRADFORD	PA	16701
27014	NATIONAL SEMICONDUCTOR CORP	SANTA CLARA	CA	95051
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO	CA	94304
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS	MA	01247
72136	ELECTRO MOTIVE CORP SUB IEC	WILLIMANTIC	CT	06226

SECTION VII

MANUAL CHANGES

7-1. INTRODUCTION.

7-2. This manual has no backdating information for the CPU manual at the publication date of this manual.

SECTION VIII

SERVICE

8-1. INTRODUCTION.

8-2. This section contains information for troubleshooting and repairing the Model 64100A's Central Processing Unit (CPU).

8-3. The CPU Block Diagram (see figure 8-2), Component Locator (see figure 8-6), Schematic (see figure 8-7), and other service information are provided on fold-out service sheets to help you in servicing the CPU.

8-4. BLOCK DIAGRAM THEORY.

a. Microprocessor U30 controls Data and Addresses on both the CPU bus and the Input/Output Bus.

b. Microprocessor Clock Generator U31, U37A,B,D develop LCLK1 and LCLK2.

c. Low Power On Pulse Generator U3A, U16A,B and part of U34 syncronize LPOP with LCLK1. The Generator also insures that any pulse from LPOP has a minimum pulse width of approximately 35nS.

d. Low Upper Byte, part of U34, indicates to the device being addressed if the information on the Data Bus is either the upper or lower byte of a word.

e. Low Byte part of U34, and U14B indicates to the device being addressed the length of the word on the Data Bus: eight or 16 bits.

f. Timing Circuits U4A, U12C, U13, U14A, U15, U16D, part of U34, U36B,C,D, and U37C develop the signals necessary for the Microprocessor to communicate with the devices connected to it, i.e., Display Controller, Prom Programmer, Proms, etc.

g. Addresses Latches U32 and U33 Latch the address from the Instruction/Data/Address Bus. The information in these Latches is routed out on the CPU multiplexed address/data Bus.

h. Address Buffers U25, U26, and P/O U34 provide the inversion for developing the ROM Addresses.

i. Chip Select U1 (NOT USED) decodes the CPU Address Bus allowing the CPU's Counter to select the ROM for execution of Software. NOTE: The 27128 ROMs presently used are jumpered to ground thru E6. If the 2764 ROMs (4) are used then jumper E6 must be moved to position A.

j. ROMs U9 and U10 contain utility routines for power up of the Mainframe, and Performance Verifications for the Mainframe including the Floppy and Tape Control and Drive Options.

k. Data Buffers U27 and U28 Provide isolation buffering between the ROMs outputs and the CPU Data Bus.

l. Test/Reset Circuit U16C and U35 will cause the Microprocessor to count from 0020 Hex to 3C00 Hex when the Test Mode jumpers E4 and E5 are in the TEST position and U27 and U28 are removed.

m. SA latch U2 is used as an aid in taking signature analysis.

n. Input/Output Bus U3A,U4B,U5, and U6 is the path the Microprocessor uses to communicate with the I/O Board, which in turn communicates with the Periphial Devices (Disc, Printer, other Stations).

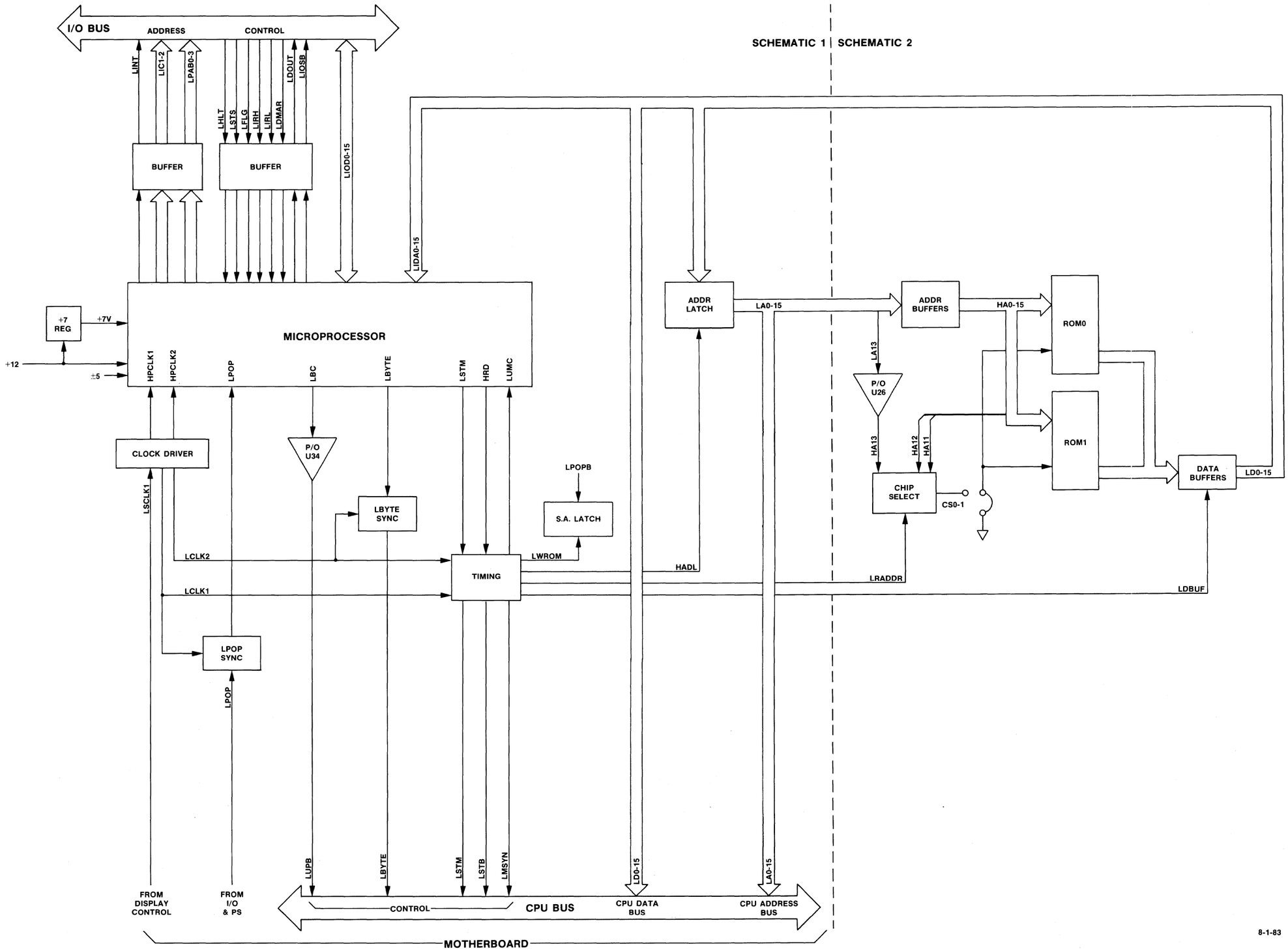


Figure 8-1.
CPU Board Block Diagram
CPU 8-3

8-5. THEORY OF OPERATION.

8-6. GENERAL.

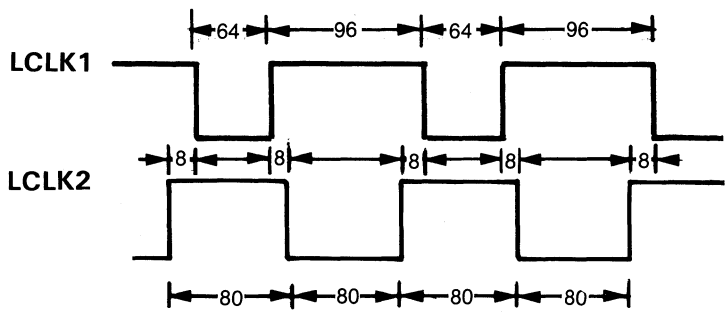
8-7. The Microprocessor used in the Model 64100A Mainframe CPU is made by Hewlett-Packard. The Microprocessor uses INMOS II Silicon on Sapphire technology. The version being used in the Model 64100A does not have Calculator Math Capability. The Microprocessor can be thought of as two Microprocessors combined on one substrate. (1) The basic Microprocessor, called the CPU Processor, has a 16 bit bi-directional bus with the Data and Address time multiplexed. The 16 bit bus is demultiplexed into a 16 bit Data Bus and a 16 bit Address Bus. The Data Bus, Address Bus, and some Control Lines, e.g., LWRT, LSTB, etc., are called the CPU Bus. The CPU Bus is distributed throughout the Mainframe over the Mother Board. (2) The second half of the Microprocessor is called the Input/Output Processor. The I/O Processor has a 16 bit bi-directional data bus, with a 4 bit address bus. Along with the 4 bit address bus, there are two other control lines that can be used to expand the I/O Address Bus. In addition there are control lines that are independent of the CPU Control Lines. The I/O Data Bus, Address Bus, and I/O Control Lines form the I/O Bus.

8-8. CPU POWER SUPPLIES.

8-9. The CPU operates on +5V, -5V, +12V, and +7V. The +7V supply is derived from an on board regulator (VR1) that is supplied by +12V on the CPU board. All other supplies are derived from the power supply assembly

8-10. CLOCK GENERATOR.

8-11. Clock Generators U31 and U37A,B,D develop LCLK1 and LCLK2 (see figure 8-1). The Clock is derived from LSCLK1 (from the Display Control Board). The frequency is 6.25 MHZ. LCLK1 and LCLK2 are non-overlapping signals.



NOTE: TIMES ARE IN NS. THEY ARE TYPICAL OF THE PROP DELAY THROUGH U37.

Figure 8-2. Clock Generator Timing

8-12. LOW POWER ON PULSE GENERATOR.

8-13. U3A, U16A,B and P/O U34 form the Low Power On Pulse Generator. The Pulse Generator synchronizes LPOP with LCLK1, and ensures LPOP has a minimum pulse width of approx. 35 nS. LPOP is generated by the Power Supply and the I/O board in the event the system software is not running correctly. In either case, LPOP will cause the Microprocessor to be initialized.

8-14. LOW BYTE SYNC.

8-15. U14B synchronizes Low Byte with LCLK2.

8-16. MEMORY CYCLE TIMING.

8-17. U4A, U12C, U13, U14A, U15, U16D, part of U34, U36B,C,D and U37C develop the signals necessary or the Microprocessor to communicate with the devices connected to it, i.e., ROM, PROM Programmer, Display Controller, etc. These signals are developed from LCLK1, LCLK2, and five signals from the Microprocessor; HRAL, LSTM, LPDR, HSYNC, and HRD. The timing relationship of the signals needed for the Microprocessor to communicate are shown in figure 8-3 and 8-4. These signals are listed in table 8-1.

8-18. CPU ADDRESS BUS.

8-19. Latches U32 and U33 capture the address from the Low Instruction/Data/Address Bus (LIDA) when High Address Latch (HADL) goes high.

8-20. ADDRESS BUFFERS.

8-21. Buffers U25, U26, and part of U34 inverts the Addresses for the ROMs.

8-22. CHIP SELECT.

8-23. Data selector U1 decodes the addresses for ROM chip selection.

8-24. ROMS.

8-25. U9 and U10 contain utility routines for power-up of the Mainframe, and Performance Verifications for the Mainframe and the floppy and tape Control and Drive options. Jumpers E1, E2 and E3 have several combinations to allow different storage capacity of ROMs to be used. Jumper information is given on the two CPU schematics.

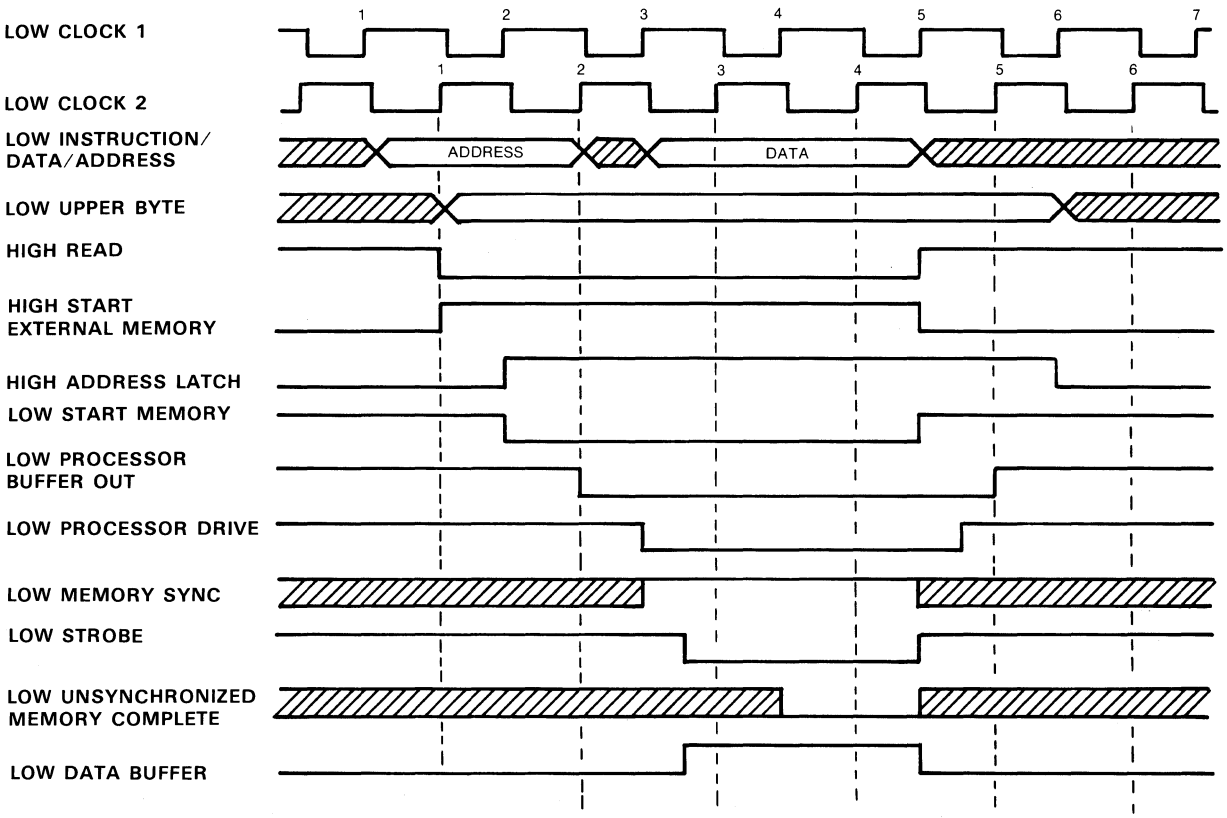


Figure 8-3. Typical Write Memory Cycle

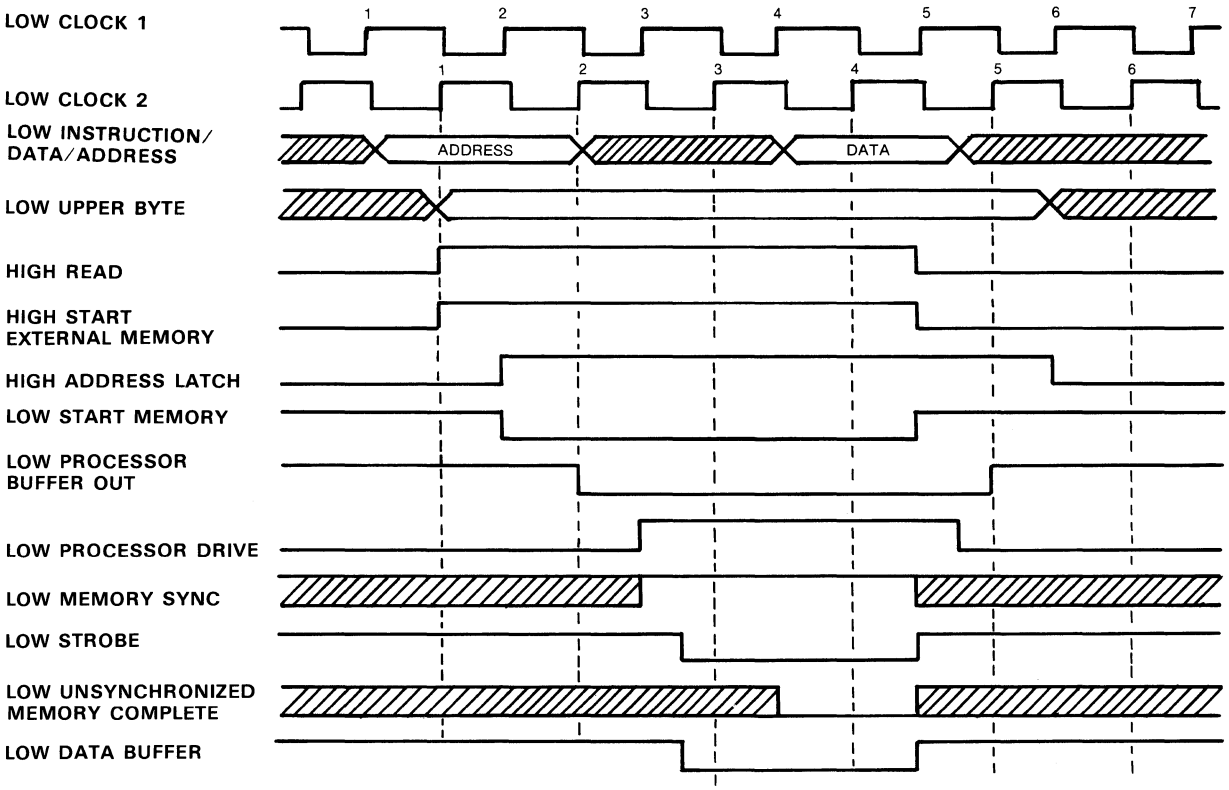


Figure 8-4. Typical Read Memory Cycle

8-26. DATA BUS.

8-27. Buffers U27 and U28 provide buffering between the ROM outputs and the CPU Data Bus. Because the Data Bus has addresses multiplexed on it, the data can only be on the Data Bus at certain times. Therefore, the outputs of U27 and U28 are active only when Low Data Buffered (LDBUF) is true.

8-28. TEST/RESET.

8-29. U16C and U35 will cause the Microprocessor to increment the address lines from 0020 HEX to 3C00 Hex, then reset to 0020 Hex and count to 3C00 Hex again. This will continue as long as Jumpers, E4 and E5, are in the Test mode and the buffers U27 and U28 are removed or disabled. The test mode is used by a service person when troubleshooting with signature analysis (see Section IV).

8-30. INPUT/OUTPUT BUS.

8-31. Activity on the Input/Output Bus is Software dependent. However, when there is activity, the timing sequence is predictable. Timing Diagrams for both Read and Write Cycles are shown in figure 8-5.

8-32. SA LATCH.

8-33. The SA latch U2 is used while taking signature analysis for setting up the intervals required to get valid signatures. See CPU section IV for information on the use of SA on the CPU board.

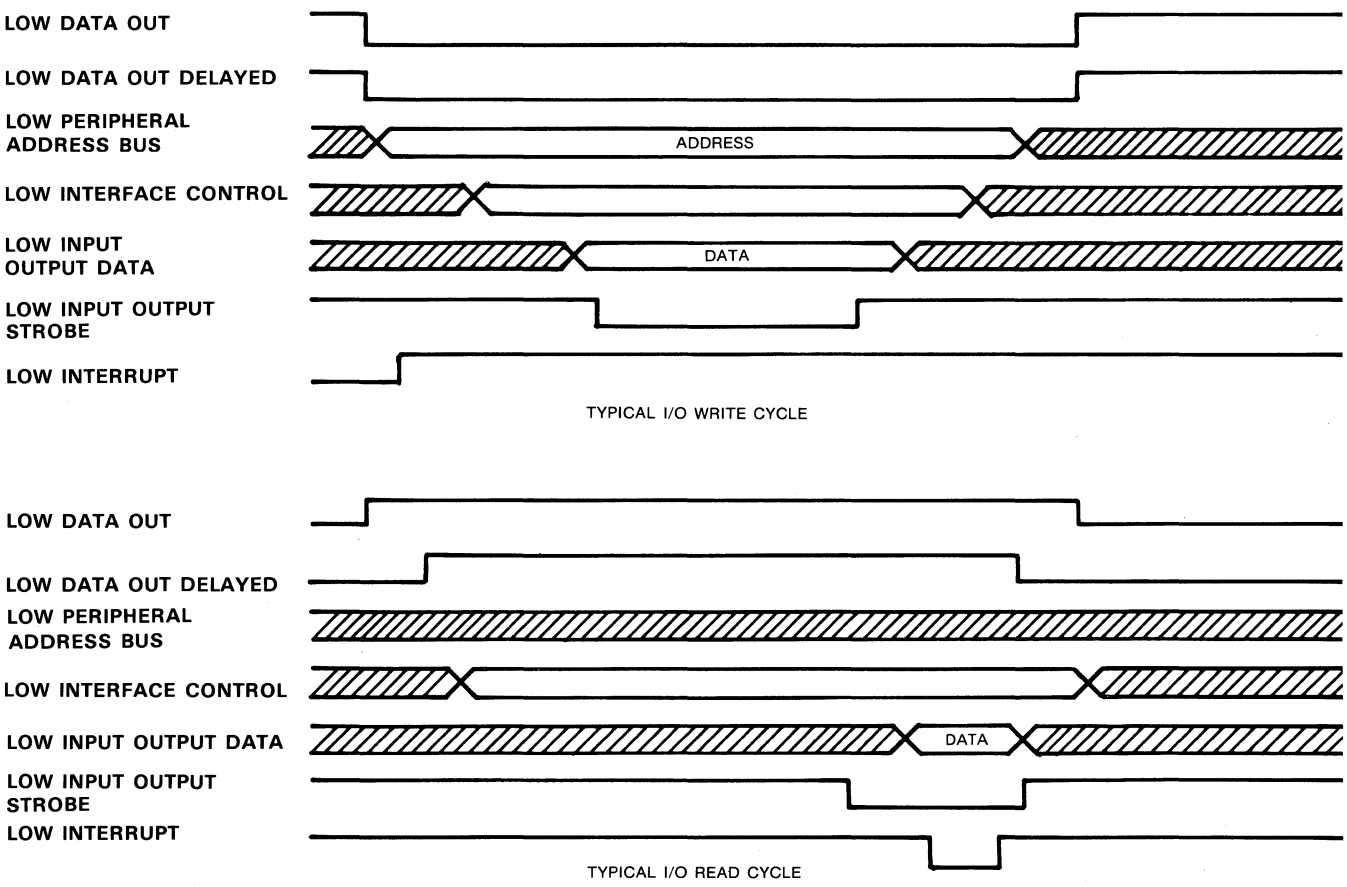


Figure 8-5. Typical I/O Read and Write Cycle

8-34. MNEMONICS.

8-35. Signals on the CPU Board have been assigned Mnemonics that describe the active state and function of the signal line. Mnemonic functional definitions are listed alphabetically in table 8-1.

Table 8-1. CPU Mnemonics

CLKIN	Clock Input - not used in this system.
HADL	High Address Latch - when high, latches the 16 bit address from the ID Address Bus (IDA) into two 8 bit latches, to be sent out on the Address Bus.
HBG	High Bus Grant - when high, acknowledges Low Bus request has been received. However, the requesting device must wait until High External Bus Grant is true before using the IDA Bus.
HCLKCNTL	High Clock Control - when high, allows HPCLK1 and 2 to be input directly, as opposed to inputing the clock into CLKIN and having the Microprocessor derive its own HPCLK1 and 2.
HDOUTD	High Data Out Delayed - normally high. When low, indicates to the addressed peripheral device the Microprocessor will read data from it.
HEXBG	High External Bus Grant - when high, indicates to the requesting device that it may use the ID Address Bus (IDA).
HPCLK1-2	High Processor Clock 1 and 2 - two complementary, nonoverlapping clocks; required by the Microprocessor Chip.
HRAL	High Register Access Line - when an address on the ID Address Bus is within the range reserved for register designation, HRAL goes high to prevent external memory from responding to any memory cycle having the same address.
HRD	High Read - when high, indicates the Microprocessor will read from devices external to it. When low, the Microprocessor will write to devices such as memory.
HSEM	High Start External Memory - Goes high at the begining of an external memory cycle. There are also memory cycles for the Microprocessor's internal memory.
HSYNC	High Sync - when high, indicates the Microprocessor is fetching an Opcode.
LA0-15	Low Address 0 through 15 - a 16 bit bus demultiplexed from the LIDA0-15 bus. Used by the Microprocessor to address various devices in the system, including ROM. The bus is send only from the Microprocessor.

Table 8-1. CPU Mnemonics (Cont'd)

LBL	Low Byte Left - when low, indicates the left or upper eight data bits of a memory cycle will be used, as opposed to the right or lower eight data bits and is used only when LBYTE is low.
LBR	Low Bus Requested - provides the way for an external device to request uninterrupted use of the ID Address Bus (IDA).
LBYTE	Low Byte - when low, indicates that a memory cycle is to involve an eight bit byte, rather than the full sixteen bits of the word.
LCLK1-2	Low Clock 1-2 - two complementary, nonoverlapping clocks; required by several devices on the CPU Board for timing.
LCS0-3	Low Chip Select 0-3 - goes low to select the desired ROM. Controlled by the Microprocessor's Address Bus.
LD0-15	Low Data 0 through 15 - a 16 bit bidirectional bus connected to the LIDA0-15 bus. Used to transfer data to and from the Microprocessor. When LSTB is low, data is present on the bus.
LDBUF	Low Data Buffered - when low, enables two 8 bit buffers to transfer data from the ROMs to the Data Bus.
LDMAR	Low Direct Memory Access Request - a peripheral device forces this line low when it wants direct access to memory.
LDOUT	Low Data Out - when low, indicates to the addressed peripheral device, that the Microprocessor will write to it. LIOSB must also be low.
LDOUTD	Low Data Out Delayed - normally low. When high, indicates to the addressed peripheral device that the Microprocessor will read data from it.
LDSTM	Low Delayed Start Memory - not used in this system.
LERA	Low Extended Register Addressing - when forced low by an external device, the internal registers have increased addressing range on the ID Address Bus (IDA).
LFLG	Low Flag - can be tested by software. A hardware line used as a "Flag" by any peripheral device which is connected to the Microprocessor. They are wire ORed "Flags".
LHLT	Low Halt - can be tested by software. Used as a "Flag" to the Microprocessor by the System Bus Controller for interrupts.
LIC1-2	Low Interface Control 1 and 2 - these two lines can provide up to four states used to control peripheral devices. How these lines are controlled is determined by software.

Table 8-1. CPU Mnemonics (Cont'd)

LIDA0-15	Low Instruction/Data/Address 0 through 15 - a 16 bit bidirectional bus which the Microprocessor communicates over. Bus information is true low. The Bus is demultiplexed into separate address and data buses.
LINT	Low Interrupt - the Microprocessor pulls this line low in response to LIRH or LIRL to allow polling the Input/Output Bus to determine which peripheral requested the interrupt.
LIOD0-15	Low Input/Output Data 0 through 15 - a 16 bit bidirectional bus. The Microprocessor uses this bus to communicate with I/O Ports. Information is true low, and is used in conjuction with LPAB0-3.
LIORD	Low Input/Output Read - when low, indicates that the CPU is reading information from the I/O bus.
LIOSB	Low Input/Output Strobe - when low, indicates the data on the Input/Output Bus is valid.
LIOWRT	Low Input/Output Write - when low, the CPU is writing information to the I/O bus.
LIRH	Low Interrupt Request High - an external device requests an interrupt by forcing this line low. LIRN has a higher priority than Low Interrupt Request Low (LIRL), and can preempt the lower priority even while it is in process. LPOP can preempt LIRH.
LIRL	Low Interrupt Request Low - an external device requests an interrupt by pulling this line low. LIRL is the lowest priority interrupt, and has no preempt abilities, therefore, must wait its turn. LIRH and LPOP can preempt LIRL.
LMSYN	Low Memory Sync - a signal from addressed devices. When low, forces the Microprocessor to wait until the addressed devices can complete the read or write operation.
LOPCODE	Low Opcode - for factory use only.
LPAB0-3	Low Peripheral Address Bus 0 through 3 - identifies which one of 16 peripheral devices will be involved in an I/O operation.
LPBE	Low Processor Buffer Enable - Always low. Enables the internal Microprocessor buffers for the Instruction/Data/Address Bus.
LPBO	Low Processor Buffer Out - controls the direction of the Microprocessor's internal, bidirectional, ID Address Buffers. When low, information is transmitted from the Microprocessor.

Table 8-1. CPU Mnemonics (Cont'd)

LPDR	Low Processor Drive - when low, the Microprocessor is driving the Instruction/Data/Address Bus.
LPOP	Low Power On Pulse - when low, initializes and prevents the Microprocessor from running. When LPOP is released, the Microprocessor begins operation at address 20 Hex. LPOP is synchronized with LCLK2 before being input to the Microprocessor. LPOP can preempt LIRL and LIRH.
LRADDR	Low ROM Address - when low, indicates the microprocessor is addressing ROM (0000-4000 Hex).
LSCLK1	Low System Clock 1 - a 6.25 MHz clock used throughout the System.
LSMC	Low Synchronized Memory Complete - a Microprocessor output, not used in this system.
LSTB	Low Strobe - when low, and in the write mode, indicates the data bus has valid information on it. When low, and in the read mode, indicates the Microprocessor is not driving the bus, and the device addressed can now drive it.
LSTM	Low Start Memory - used to initiate a memory cycle. When low, indicates that the information on the Address Bus is valid.
LSTS	Low Status - can be tested by software. Used as a "Flag" by any peripheral device connected to the Microprocessor. The peripheral devices are wire ORed to this line.
LUMC	Low Unsychronized Memory Complete - when low, allows the Microprocessor to complete its memory cycle. If the Memory needs to make the Microprocessor wait, due to long access times, it pulls LMSYN low, causing LUMC to go high. When LUMC is high the Microprocessor must wait.
LUPB	Low Upper Byte - when low, indicates the upper byte is being written or read and is used only when LBYTE is low.
LWROM	Low Write ROM - when low, this signal clocks the SA latch forcing an SA interval to occur.
LWRT	Low Write - when low, the Microprocessor will write to the addressed device.

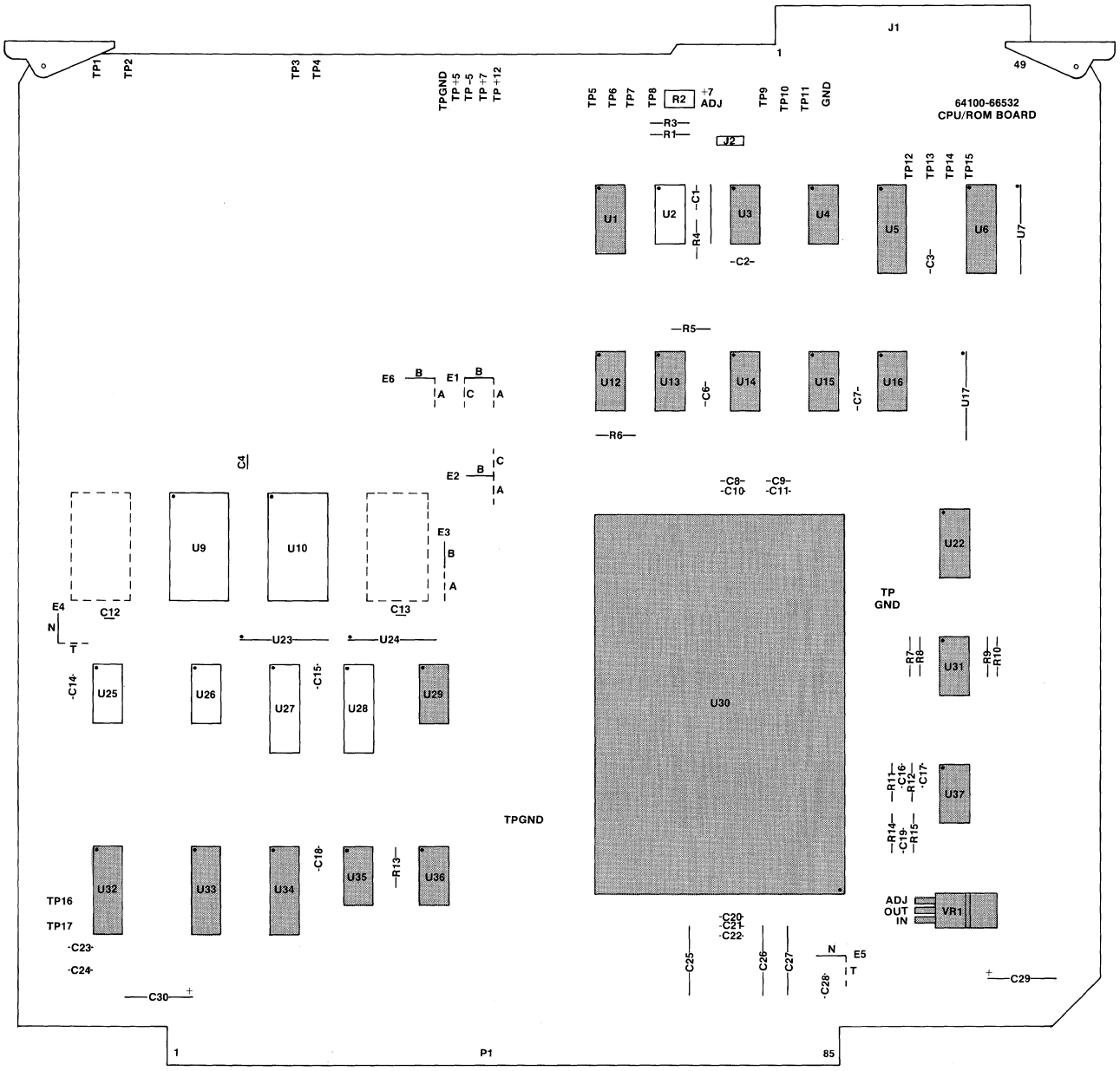


Figure 8-6. CPU Component Locator

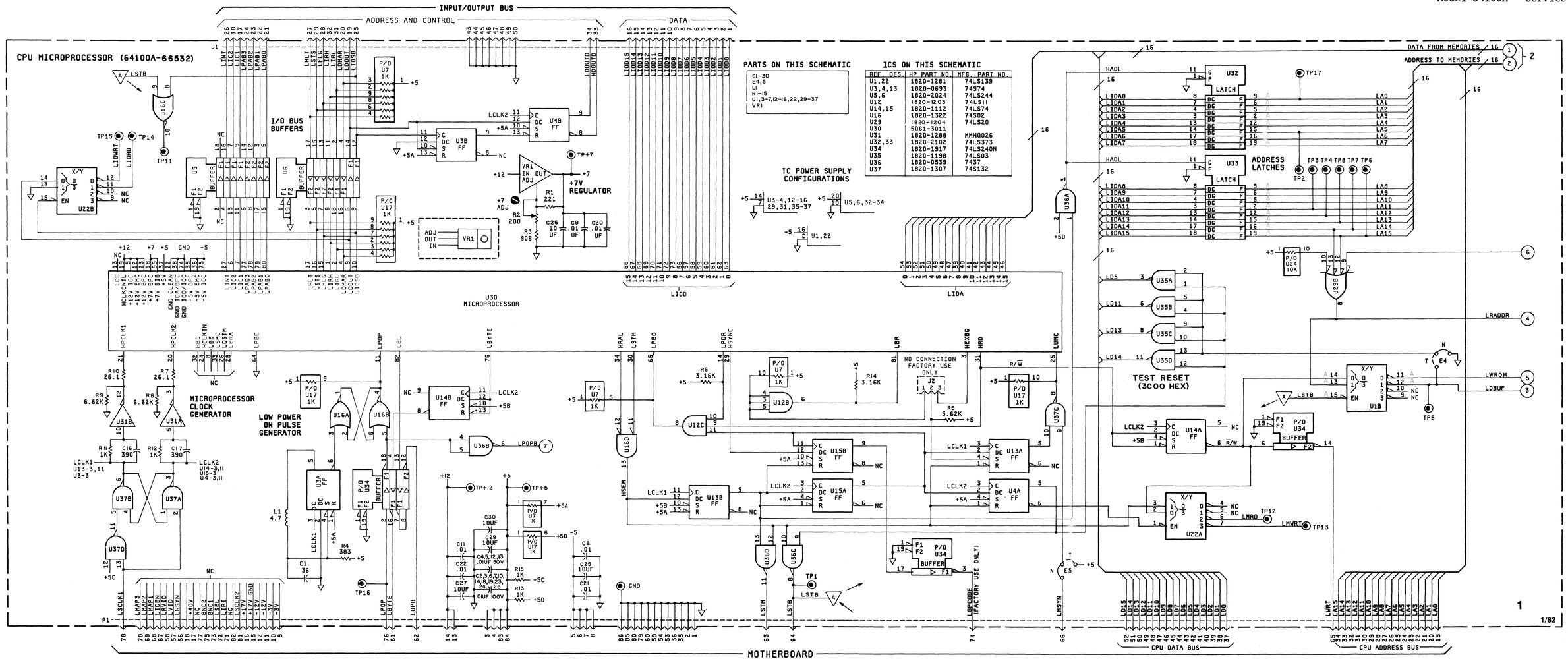
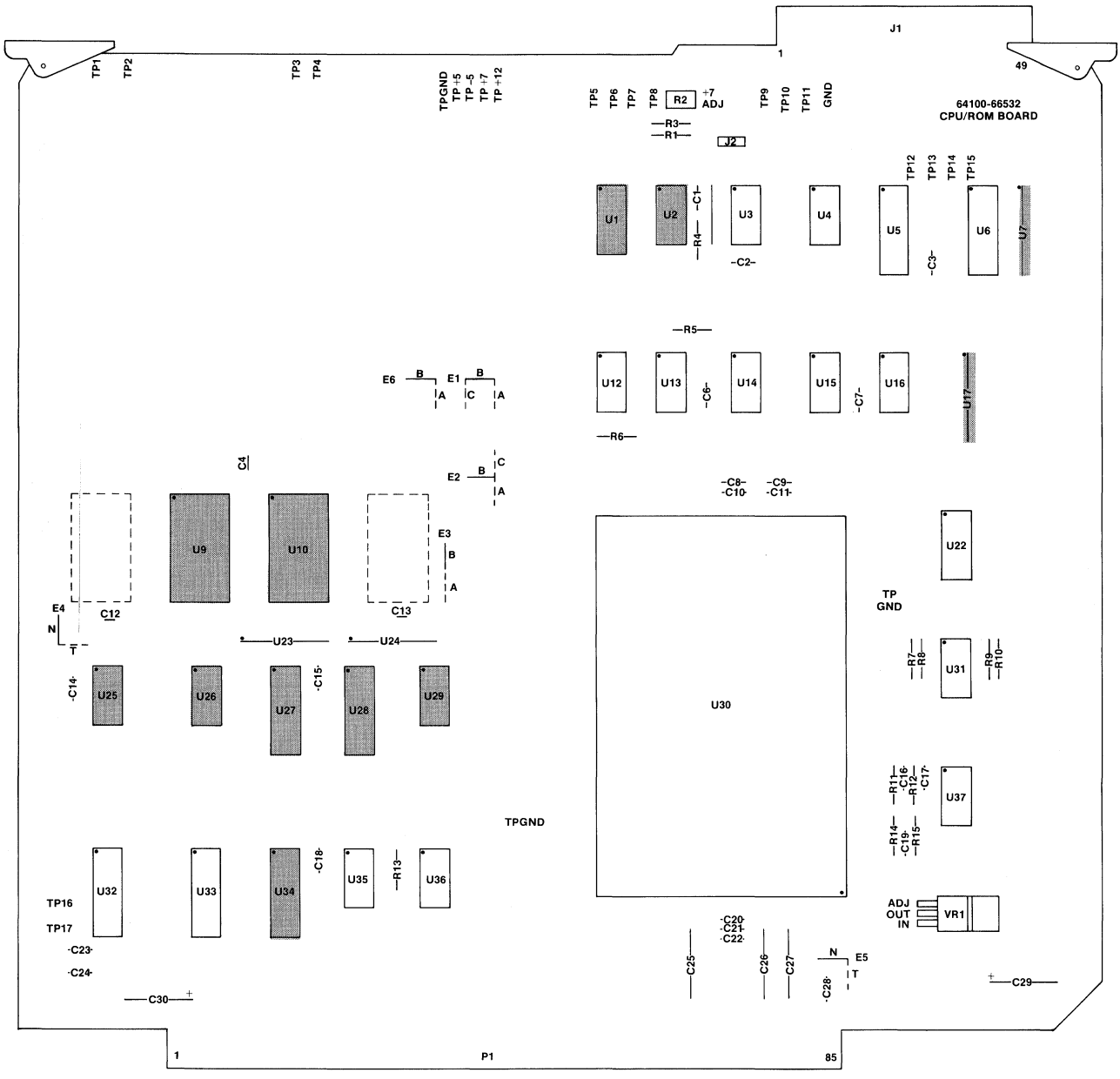
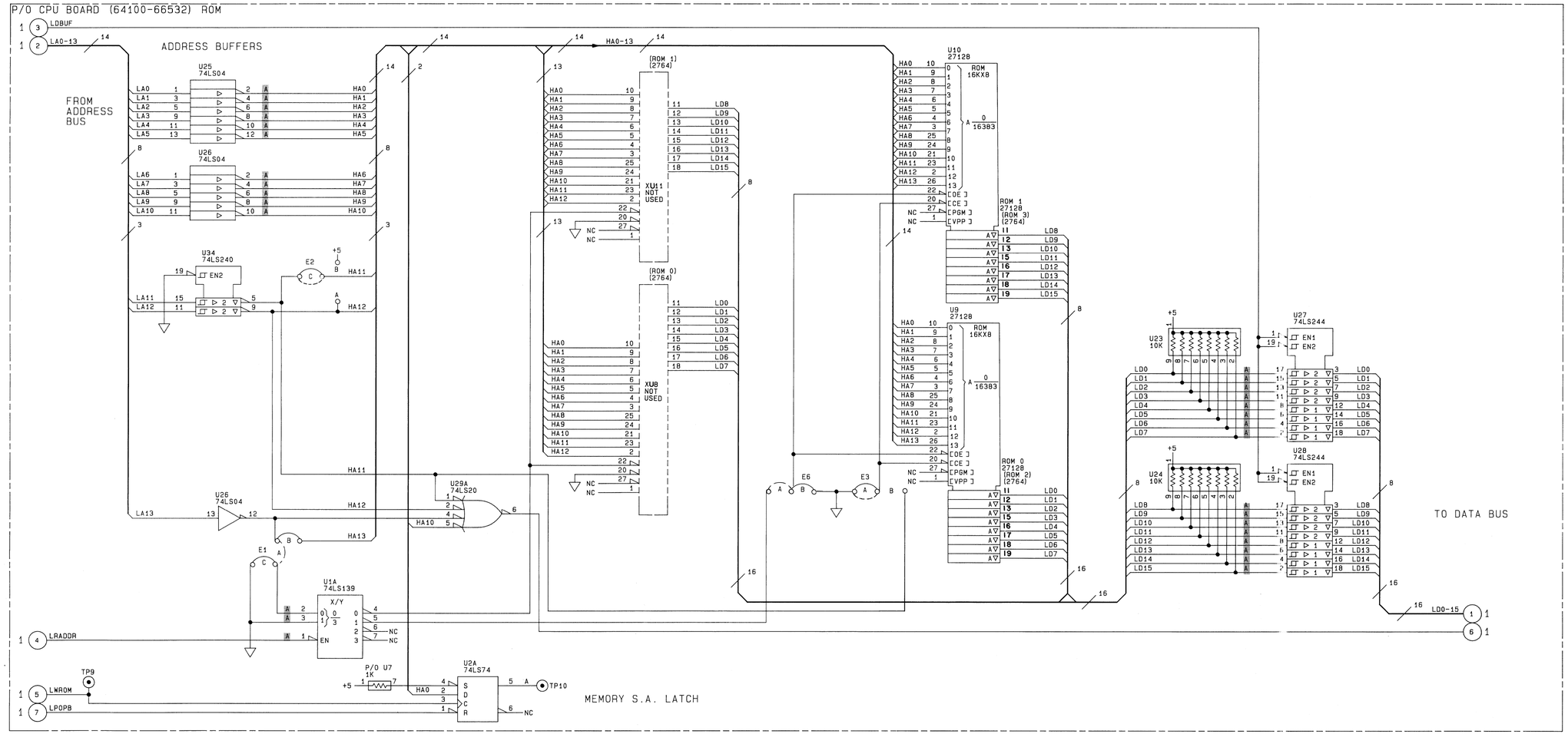


Figure 8-7.
CPU Schematic 1 (1 of 2)
CPU 8-15



CPU Component Locator



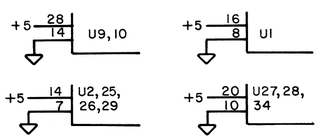
ICs ON THIS SCHEMATIC

REF. DES.	HP PART NO.	MFR. PART NO.
U1	1820-1281	74LS139N
U2	1820-1112	74LS74N
U7	1810-0275	NET 1K x 9
U9	64100-80028	ROM 0
U10	64100-80029	ROM 1
U24,24	1810-0280	NET 1K x 9
U25,26	1820-1199	74LS04N
U27,28	1820-2024	74LS244N
U29	1820-1204	74LS20N
U34	1820-1917	74LS240N

PARTS ON THIS SCHEMATIC

E1-3,6
U1,2,7,9,10,23-29,34
TP9,10

IC POWER SUPPLY CONFIGURATIONS



NOTE:
Two 128K ROMs are used on the 64100-66532 CPU Board. XU8 and XU11 are on the board to support the older 64K ROMs.

denotes the 2764 ROMs (U8,9,10,11)

denotes the 27128 ROMs (U9,10)

Board comes configured in this setting.

Figure 8-7.
CPU Schematic 2 (Sheet 2 of 2)
CPU 8-17/(8-18 blank)

SERVICE MANUAL

MODEL 64100A

DISPLAY CONTROLLER AND DRIVER

Manual Part No. : Part of Mainframe Manual
Microfiche Part No. : See Mainframe Manual

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LIST OF ILLUSTRATIONS

SECTION I

GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. The following subsections provide the service information for the display section of the HP 64100A LOGIC DEVELOPMENT SYSTEM. Included are detailed removal and installation instructions, adjustments for the CRT, and a block diagram level theory-of-operation. Standard service information includes schematics, parts lists, component locators, signature analysis tables, troubleshooting guide, and a table of mnemonics.

1-3. DESCRIPTION.

1-4. The display section functions are handled by three electronic assemblies; the Display Controller assembly, the Display Driver assembly, and the cathode ray tube (CRT) assembly. The display screen format provides for 80 characters and 25 rows. The horizontal sweep sync runs at a frequency of 25 KHz; the vertical sweep sync runs at 60 Hz. The dot matrix size for each character is 7 dots wide by 9 dots high. To allow for a border around and between characters, each character is allotted a space 9 dots wide by 15 dots high. The horizontal scanning rate is 25 MHz, 40 nanoseconds per dot (see figure 1-1. Example of Display Format).

1-5. The display controller board utilizes an Intel 8275A CRT controller to simplify display circuitry. The primary function of the 8275A is to refresh the display by buffering the information from RAM memory and keeping track of the display position of the screen.

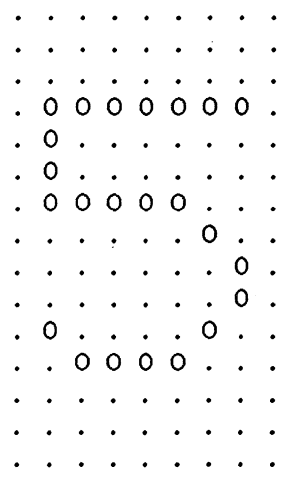


Figure 1-1. Example of Display Format

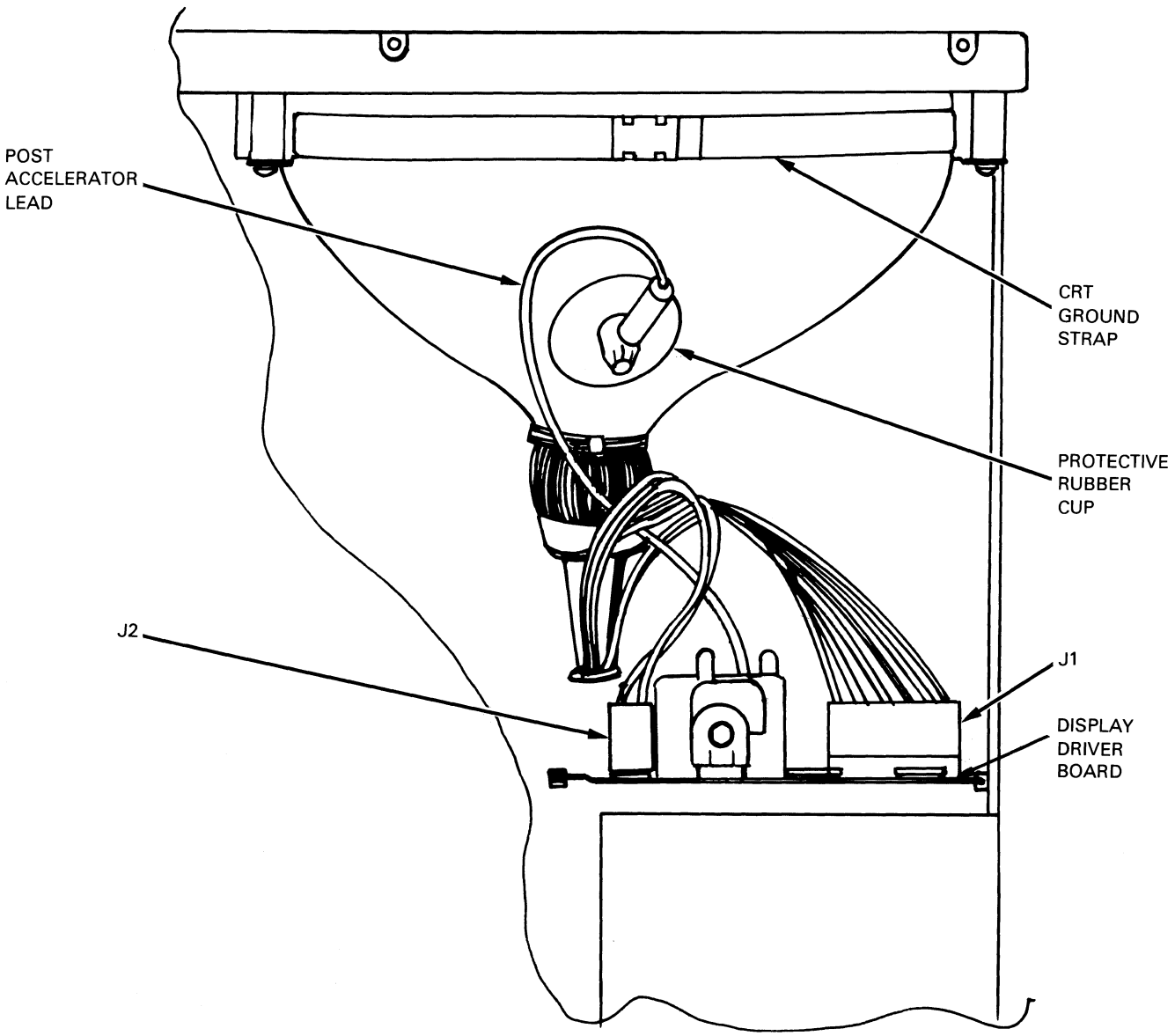


Figure 1-2. Location of Display Components

SECTION II

INSTALLATION AND REMOVAL

2-1. DISPLAY CONTROLLER.

CAUTION

NEVER INSTALL OR REMOVE ANY CIRCUIT BOARD WITH THE POWER SWITCHED ON. COMPONENT DAMAGE WILL OCCUR!

WARNING

LETHAL VOLTAGES EXIST THROUGHOUT THE MAINFRAME. POWER LINE SWITCH OFF BEFORE SERVICING OR REMOVING CIRCUIT BOARDS.

2-2. The Display Controller board must be installed in the second card cage slot from the front of the machine. The slot is labeled "DSPL CNTL". Be sure the card is aligned with the connector on the Motherboard before complete insertion. To remove the Display Controller board, first disconnect any cables that cross over the top of the Display Controller board. The board can now be removed by lifting on the two card extractor levers simultaneously.

2-3. DISPLAY DRIVER.

WARNING

HAZARDOUS POTENTIALS EXIST ON THE DISPLAY DRIVER BOARD AND ON THE CRT. TO AVOID ELECTRICIAL SHOCK THE FOLLOWING PROCEDURE SHOULD BE CLOSELY ADHERED TO. WEAR SAFETY GLASSES!!!

2-4. REMOVAL:

1. Switch power OFF and disconnect the AC power cord.

2. Completely remove the five screws that secure the top cover. Also, remove the two (or four) screws that secure the state and timing ground clips to the rear panel. Lift and remove cover.

CAUTION

Discharge the post accelerator lead to the grounding strap only. Component damage will occur if discharged to other areas.

NOTE

THE CRT MAY CHARGE UP BY ITSELF EVEN WHILE DISCONNECTED. DISCHARGE THE CRT BY SHORTING THE POST ACCELERATOR TERMINAL OF THE CRT TO THE CRT GROUND STRAP WITH A JUMP LEAD, BEFORE HANDLING.

3. Short out the charge on the CRT by connecting a jumper lead between the ground strap of the CRT and the shaft of the screwdriver. Slip the screwdriver under the protective rubber cup of the Post Accelerator lead and then momentarily touch the screwdriver to the metal clip of the Post Accelerator lead.

4. Disconnect the Post Accelerator lead from the CRT .

5. Disconnect the cables at J1 and J2 of the display driver, see figure 2-1.

6. Pull the Display Driver board straight up from the Motherboard socket.

The Display Driver can be installed by reversing the order of the removal procedure.

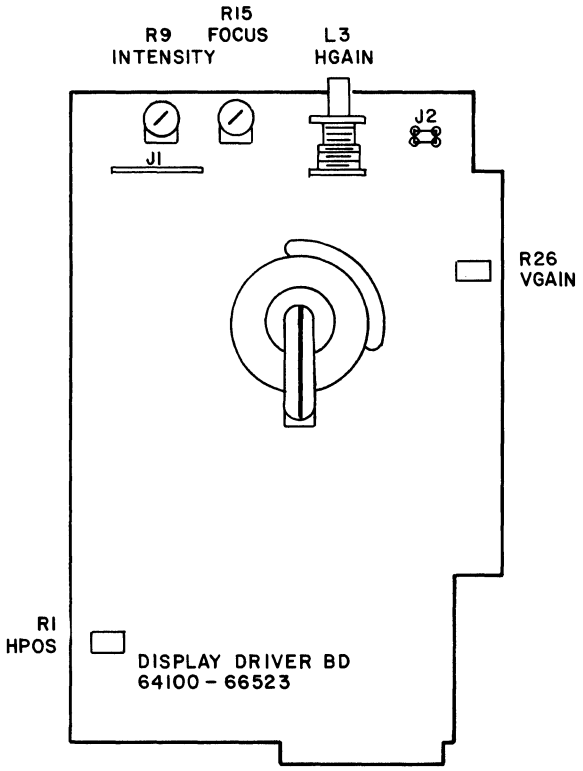


Figure 2-1. Location of Connectors J1 and J2

2-5. CATHODE RAY TUBE.

WARNING

HAZARDOUS POTENTIALS EXIST ON THE CRT. TO AVOID ELECTRICAL SHOCK THE FOLLOWING PROCEDURE SHOULD BE CLOSELY ADHERED TO. SAFETY GLASSES SHOULD BE WORN WHILE WORKING WITH THE INTERIOR OF THE UNIT EXPOSED.

2-6. REMOVAL:

1. Switch power OFF and disconnect the AC power cord.

2. Completely remove the five screws that secure the top cover. Also, remove the two (or four) screws that secure the state and timing ground clips to the rear panel. Lift and remove cover.

CAUTION

Discharge the post accelerator lead to the grounding strap only. Component damage will occur if discharged to other areas.

3. Short out the charge on the CRT by connecting a jumper lead between the ground strap of the CRT and the shaft of the screwdriver. Slip the screwdriver under the protective rubber cup of the Post Accelerator lead and then momentarily touch the screwdriver to the metal clip of the Post Accelerator lead.

NOTE

THE CRT MAY CHARGE UP BY ITSELF EVEN WHILE DISCONNECTED. DISCHARGE THE CRT BY SHORTING THE POST ACCELERATOR TERMINAL OF THE CRT TO THE CRT GROUND STRAP WITH A JUMPER LEAD.

4. Disconnect the Post Accelerator lead from the CRT.

5. Disconnect the cables at J2 of the Display Driver and the cable at the end of the CRT.

6. Completely remove the four CRT mounting screws, then lift and remove CRT from chassis.

2-7. INSTALLATION:

The CRT can be installed by reversing the order of the removal procedure. Don't forget to replace the ground wire to the upper right CRT mounting screw.

SECTION III

OPERATION

3-1. GENERAL.

3-2. The Performance Verification section of the Mainframe contains the procedure for testing the various functional areas of the processor to help in isolating malfunctions. There are no external user controls.

SECTION IV

PERFORMANCE VERIFICATION

4-1. INTRODUCTION.

4-2. If the Mainframe has failed in a display or RAM test, troubleshoot using this section. If there is some doubt as to the failure mode, return to section IV of the Mainframe chapter.

4-3. RAM TESTS.

4-4. POWER-UP RAM TEST.

Purpose:

This RAM test verifies the ability to read and write from the upper 32K x 16 locations of RAM (address 8002 HEX thru FFFF HEX) located on the Display Controller board. Note that this test occurs only on power up. The lower 32K x 16 locations of RAM (memory mapped address 4000 HEX thru 7FFF HEX) are tested under option test. The option test is initiated by pressing the "opt-test" softkey. The upper and lower 32K of RAM have their own PV and display different error messages.

Area Tested:

All upper 32K x 16 locations of RAM including refresh ability, the multiplexed memory Address/Data bus from the CPU, Motherboard connections between CPU and Display Controller board, the demultiplexed Address/Data bus to/from RAM, and the timing and control circuitry.

Operation:

a. The power up RAM test operates differently from the PV test.

b. The RAM test takes approximately 7 seconds.

c. All upper 32K x 16 locations of RAM are toggled to insure READ/WRITE operation.

d. Refresh ability is verified.

e. The operation of the routine is as follows:

1. Load RAM with a pseudo random count, starting with zero.

2. Read RAM and compare with count.

3. Check for an error. If error occurs go to error sequence.

4. If there is no previous error, wait one second.

5. Read RAM and compare with count.

6. Check for an error. If error occurs go to error sequence.

7. If there is no previous error, load RAM with complement of count, starting at zero.

8. Read RAM and compare with the complement of the count.

9. Check for an error. If error occurs go to error sequence (see step f).

10. If there is no previous error, wait one second.

11. Read RAM and compare with count.

12. Check for an error. If error occurs, go to error sequence.

f. If there are not any errors in either RAM error mask then the system will beep twice. But, if an error exists, then the following error sequence occurs for steps a thru e:

1. Reset the delta timer to prevent auto restart.

2. Set the SA latch.

3. Write to and read from the upper 32K locations of RAM.

4. Provide stimulus to CRT controller.

5. Output RAM error display header information (including refresh error message if refresh error flag set).

6. Reset SA latch.

7. Output individual failing IC number for the upper 32K x 16 memory locations which are contained on all 16 RAM ICs.

NOTE

The Display Controller board has 64K x 16 memory locations on 16 RAM ICs. The older Display Controller boards (with serial prefix numbers less than on the title page of this manual) have 32K x 16 memory locations on 32 RAM ICs. When a RAM failure occurs, the failing unit number might display two failure RAM numbers. When the message is read, use the lower value number and disregard the larger number. The reason this occurs is the firmware has not changed and so the coded RAM failure message remains the same.

g. When a failure occurs, the routine attempts to output an error message as follows:

```
SELF-TEST FAILURE <------- blinking
RAM TEST:
FAILING UNIT NUMBER (S)
-----------------------
XY   <--- older failing RAM numbers (U51-U58 or U65-U72 not used)

XY   <--- failing RAM number (U23-U30 or U38-U45)
```

"XY" corresponds to the U# of the failing RAM. Depending on which RAM is failing, the display could be affected. Evidence of this is a random pattern on the CRT or incorrect spelling of messages. For this reason the accuracy of a RAM test failure is always suspect. Because each RAM is 1 bit wide, all 16 RAMs are used to store display information. Thus, if any of these 16 RAMs is failing, the display will be unintelligible to various degrees. If the error message displays two failing RAMs, use the lower IC number.

4-5. UPPER 32K RAM PV TEST.

Purpose:

The RAM test verifies the ability to read and write from the upper 32K addressable locations of RAM located on the Display Control board and checks for refresh. Note that this test only occurs during PV and is intended to troubleshoot intermittent problems. This test can be run in single step or continuous mode. It displays the number of tests run versus the number of tests failed. If a failure occurs, an error message code will be displayed on the same line.

Area Tested:

All upper 32K x 16 memory locations including refresh ability, the multiplexed memory Address/Data bus from the CPU, Motherboard connections between CPU and Display Controller board, the demultiplexed Address/Data bus to/from RAM, and the timing and control circuitry.

Operation:

a. This test takes approximately eight seconds.

b. Data from ROM is written into RAM, and then read back and compared to the ROM contents.

c. The second step writes walking 1's and 0's to each RAM address and reads it back. The walking 1's and 0's are visable on the CRT as a blinking pattern with characters moving to the bottom of the screen.

NOTE

Since the display uses a portion of all 16 RAMs, a failure may affect the ability to display the failed RAM IC number.

Example of PV ERROR MESSAGE.

RAM TEST: BIT ERROR MASK UPPER BANK=XXXX LOWER BANK=XXXX

The XXXX is the hexidecimal representation of the 16 bit error mask. Since there are 64K x 16 locations of RAM, each RAM IC is one data bit for the entire upper 32K address range. There is a one to one correlation between the data bit set in the error mask and the failing RAM.

Table 4-1. PV ERROR CODE

A "1" indicates a failure when the HEX error code is converted to BINARY.

Example error: RAM TEST: BIT ERROR MASK UPPER BANK=2004 LOWER BANK=0000

2	0	0	4
U45 U44 U43 U42	U41 U40 U39 U38	U30 U29 U28 U27	U26 U25 U24 U23
0 0 1 0	0 0 0 0	0 0 0 0	0 1 0 0

U43 and U25 have failed.

Example error: RAM TEST: BIT ERROR MASK UPPER BANK=0000 LOWER BANK=A010

A	0	1	0
U45 U44 U43 U42	U41 U40 U39 U38	U30 U29 U28 U27	U26 U25 U24 U23
1 0 1 0	0 0 0 0	0 0 0 1	0 0 0 0

U45, U43, and U27 have failed.

NOTE

The error message display shows "UPPER BANK" and "LOWER BANK". There is only one bank of RAM on the Display Controller board for mainframes identified by the serial prefix number on the title page of this manual. The XXXX message is still valid. Ignore which BANK the message appears in. Table 4-1 should simplify the error message.

4-6. LOWER 32K RAM TEST.

4-7. PERFORMANCE VERIFICATION TESTS.

4-8. The Performance Verification for the lower 32K of memory is a software routine used by the mainframe to test about 99 % of the circuitry used by the RAM.

Purpose:

This RAM test verifies the ability to read and write from the lower 32K x 16 memory locations of RAM located on the Display Controller board and checks for refresh operation.

Area Tested:

All lower 32K x 16 memory locations of RAM including refresh ability, the multiplexed memory Address/Data bus from the CPU, Motherboard connections between the CPU and Display Controller boards, the demultiplexed Address/Data bus to/from RAM, and the timing and control circuitry. Signature analysis loops can also be tested.

operation:

a. With the operating system initialized and awaiting a command (figure 4-1), press the opt_test softkey command. The display should show:

option_test .....press [RETURN]

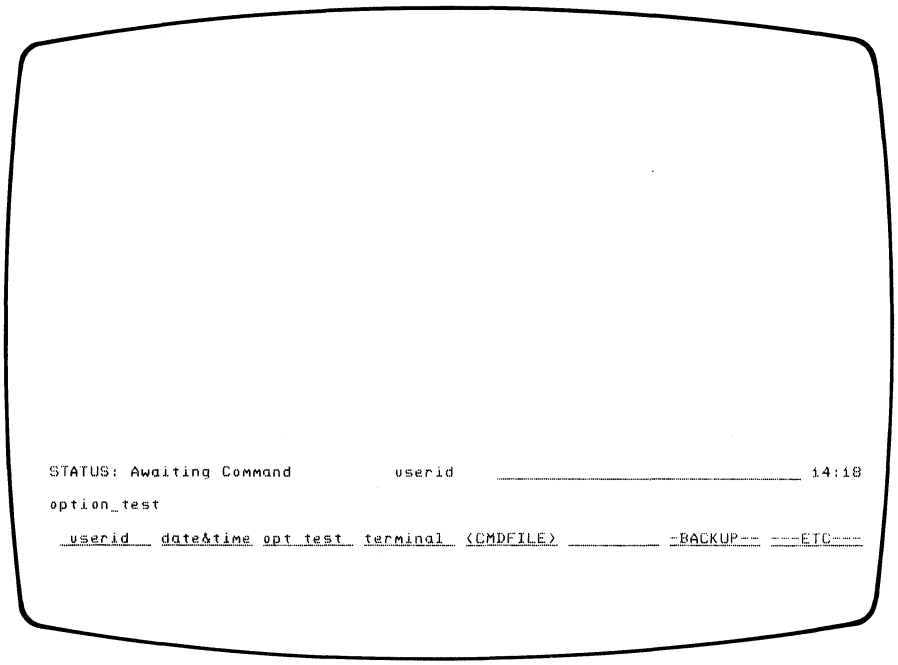


Figure 4-1. System Awaiting Command Display

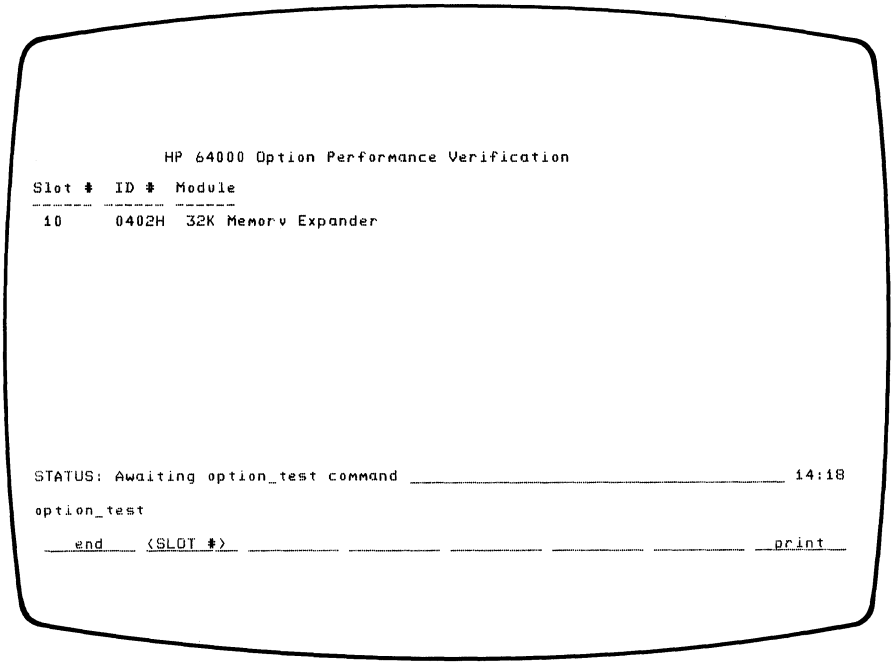


Figure 4-2. Card Cage Directory Display

b. The PV now displays a directory of the installed option boards and their card slot numbers (figure 4-2). The lower 32K locations of memory are addressed as a "32K Memory Expander" option and is accessed through option slot 10 with an ID of 0402 HEX.

   ENTER: 10 .....press [RETURN]

c. Bank 1 and Bank 2 refer to the upper 16K and lower 16K of the lower 32K locations of memory in RAM under test. See figure 4-3.

4-9. PERFORMANCE VERIFICATION COMMANDS.

4-10. Each PV display provides prompting for the commands that can be executed. These commands are selected by "softkeys" which are defined on the following page.

NOTE

The BANK 1 and BANK 2 commands refer to the lower 32K addressable locations of RAM divided into two 16K MEMORY BANKs for PV. Both BANK 1 and BANK 2 operate identically except for the address range they occupy in RAM. Only one set of PV commands will be explained using BANK 1 as the model.

cycle.....initiates highlighted test and continues through other tests until the end, next_test, softkey is pressed.

end.....terminates test activity and returns display to next higher level. At Total PV Display (Figure 4-3), also resets failure counters to zero.

next_test.....moves highlight line to following test category.

print.....outputs display to attached printer.

disp_test.....sets the display to the next lower level where the "start" and "exit_test" softkeys start and stop the PV test.

4-11. TOTAL PV TEST.

4-12. Display. All test categories available are shown in this display. When one or more test categories have been executed the results are displayed. Use the display to choose the test categories to be performed or to review the overall results of the PV.

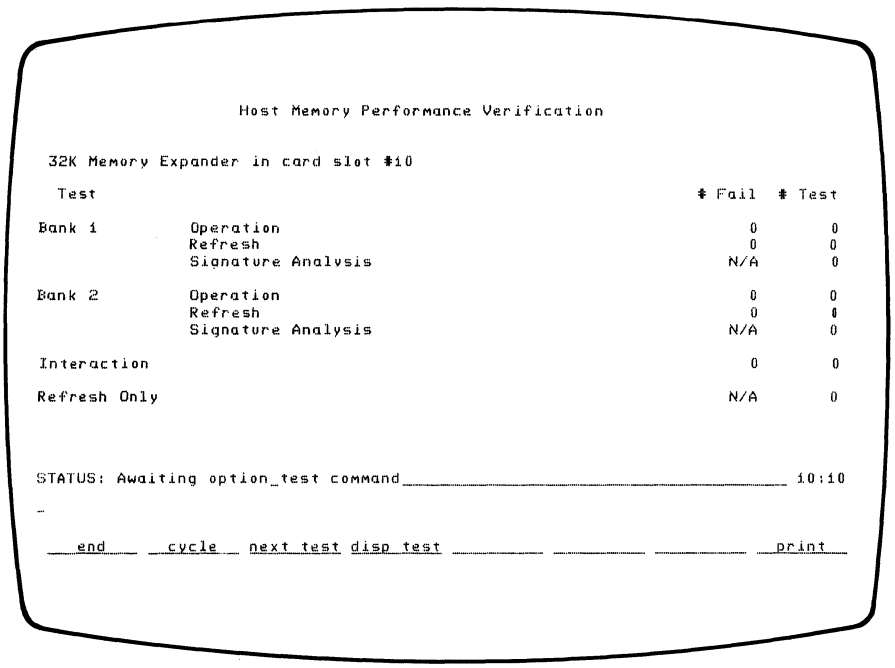


Figure 4-3. Total PV Display

4-13. Running the Total PV. To run all the tests shown on the display, press the "cycle" softkey. Each test category is executed and the results are displayed. A complete cycle requires approximately fifteen seconds. Press the "next_text" softkey to halt the iterations.

4-14. Using the Total PV Results. When the tests are complete, examine the # Fail column. All entries zero indicate that approximately 99% of the circuitry has been checked and no errors have been found.

4-15. A non-zero value represents the number of errors detected in the test category. Determine the exact cause of the error by running the failed test category and viewing the results in detail. Do this by positioning the highlight line over the failed test category and pressing the "disp_test" softkey. This places the display in the next lower level where the "start" initiates the PV test and the "exit_test" ends the PV test.

4-16. OPERATION TEST.

4-17. Display. This display shows the four Operation test categories and the test results. Use the display to view test conditions in detail.

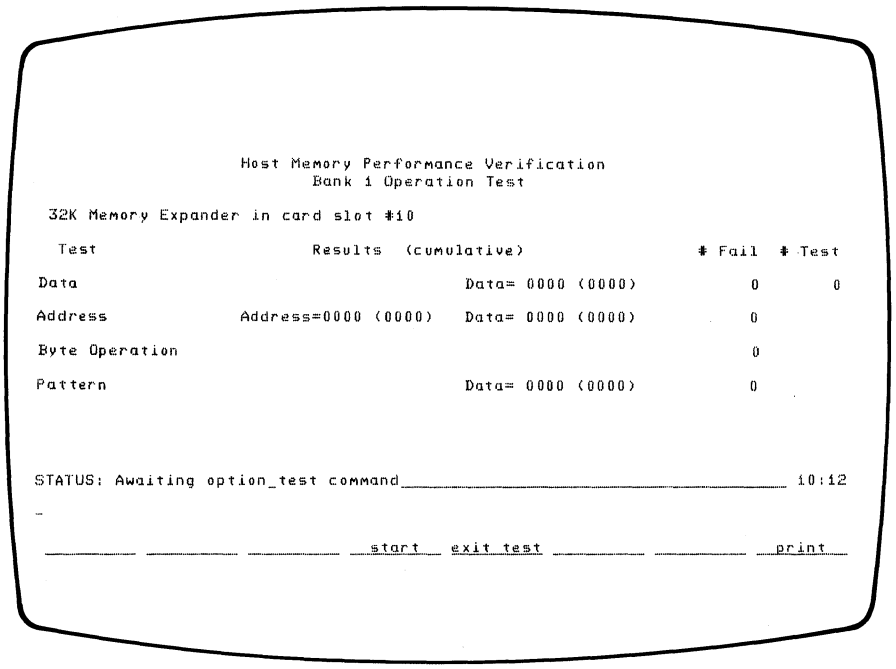


Figure 4-4. Operation Test Display

4-18. Running the Operation Tests. The Operation tests are started by pressing "disp_test" and then the "start" softkeys. To stop the tests and return to the Display, press the "exit_test" softkey. Each iteration of the tests takes less than one second.

4-19. Using the Operation Test Results. The total number of errors detected during the tests is shown in the # Fail column. Each error code in the Results column represents a single failure encountered during the last iteration. Each error code in the (cumulative) column represents the sum of all errors detected during the test. Cumulative error codes that differ from Results error codes indicate multiple, or intermittent errors. When the error codes are the same, the errors are systematic. Refer to the appropriate test for an explanation of what the test does and how to decode the errors.

4-20. DATA TEST.

4-21. Purpose. This test (figure 4-4) checks all data paths for signals LD0 through LD15 by writing data to the memory RAMs and then reading it back. When a bit cannot be written and read back in both its high and low level, an error is flagged. During the test, data is written to only one address in each of the 16 RAMs, therefore, a successful test indicates that the data paths are functioning correctly, but it does not imply that all cells in all RAMs are operating properly. See Pattern Test for RAM cell check. Note that address bus failures generally do not affect the reliability of this test.

4-22. Decoding Data Test Errors. All errors found are formatted as a four character hexidecimal word. Each character represents four binary digits, each digit corresponding to a single data line. To decode an error word, convert each character to its binary equivalent and compare it with the chart shown below. If necessary, refer to Table 4-2. for hexidecimal-to-binary conversion. For example, if the error word is 0005, there are errors on the LD0 and LD2 data paths. The U-number shown in the chart indicates the RAM that may have a failure.

a. Data Test Errors.

Hex	Binary	Signal in error/RAM	
xxxx=	0000 0000 0000 0000	None	
	---- ---- ---- ---1	LD0	U1
	---- ---- ---- --1-	LD1	U17
	---- ---- ---- -1--	LD2	U2
	---- ---- ---- 1---	LD3	U18
	---- ---- ---1 ----	LD4	U3
	---- ---- --1- ----	LD5	U19
	---- ---- -1-- ----	LD6	U4
	---- ---- 1--- ----	LD7	U20
	---- ---1 ---- ----	LD8	U5
	---- --1- ---- ----	LD9	U21
	---- -1-- ---- ----	LD10	U6
	---- 1--- ---- ----	LD11	U22
	---1 ---- ---- ----	LD12	U7
	--1- ---- ---- ----	LD13	U23
	-1-- ---- ---- ----	LD14	U8
	1--- ---- ---- ----	LD15	U24

LD = Low Data

4-23. ADDRESS TEST.

4-24. Purpose. Fourteen address lines are checked in this test (figure 4-4) to make certain they are intact. Data is written to selected addresses in the RAMs and read back. When each bit at the selected addresses cannot be written and read at its high and low state, an error is noted.

4-25. Decoding Address Test Errors. Because data errors can cause an address test to fail, both the address bits and data bits are flagged when a failure occurs. After the failure occurs, decode the four character "address error word" using the chart shown below. To decode the "data error word", use the chart shown in the Data Test. Refer to Table 4-2 for hexidecimal-to-binary conversion, if necessary. Significant error conditions follow.

a. Address Test Errors.

Hex	Binary	Signal in error
xxxx=	0000 0000 0000 0000	None
	00-- ---- ---- ---1	LA0
	00-- ---- ---- --1-	LA1
	00-- ---- ---- -1--	LA2
	00-- ---- ---- 1---	LA3
	00-- ---- ---1 ----	LA4
	00-- ---- --1- ----	LA5
	00-- ---- -1-- ----	LA6
	00-- ---- 1--- ----	LA7
	00-- ---1 ---- ----	LA8
	00-- --1- ---- ----	LA9
	00-- -1-- ---- ----	LA10
	00-- 1--- ---- ----	LA11
	00-1 ---- ---- ----	LA12
	001- ---- ---- ----	LA13

LA = Low Address

NOTE

When.....LA15 = False
and...LA14 = True
then the Memory Mapped I/O is addressed. The lower 32K of RAM is addressed over the Memory Mapped I/O.

When.....LMAP1 = False then BANK 2 is addressed

When.....LMAP1 = True then BANK 1 is addressed

b. Address Error = 3FFF. Indicates all address lines are failing. This is because there are only 14 address lines and an error of FFFF cannot be returned from the test.

c. Multiplexed Address Errors. When two address bits are in error, check to see if they are separated by seven bits. This may indicate a single line is failing that is carrying both bits in multiplexed form. Multiplexed address bits are shown below.

Multiplexed Address Bits

Bits	Node	Hex
0 and 7	U37 - 11	0081
1 and 8	U37 - 13	0101
2 and 9	U37 - 12	0204
3 and 10	U37 - 18	0408
4 and 11	U37 - 17	0810
5 and 12	U37 - 16	1020
6 and 13	U37 - 19	2040

4-26. BYTE OPERATION TEST.

4-27. Purpose. This test (figure 4-4) checks the module's ability to perform byte operations. When the upper and lower bytes cannot be written and read back correctly, an error condition is noted.

4-28. Decoding Byte Operation Errors. The errors found in this test are not decoded. When this test fails and all other tests pass, the failure is probably associated with signals LWRTL and LWRTU in the read/write control circuit.

4-29. PATTERN TEST.

4-30. Purpose. All of the cells in each RAM are checked by this test (figure 4-4). When both the high and low state cannot be written and read back from each cell, a failure is noted.

4-31. Decoding Pattern Test Errors. All errors found are formatted as a four character hexidecimal word. Each character represents four binary digits, each digit corresponding to a single bit. To decode an error word, convert each character to its binary equivalent and compare it with the chart shown below. If necessary, see Table 4-2 for hexidecimal-to-binary conversion. For example, if the error word is 0060, there are errors on the LD5 and LD6 data paths. The U-number shown in the chart indicates the RAM that may have a failure.

a. Pattern Test Errors.

Hex	Binary	Signal in error/RAM	
xxxx=	0000 0000 0000 0000	None	
	---- ---- ---- ---1	LD0	U1
	---- ---- ---- --1-	LD1	U17
	---- ---- ---- -1--	LD2	U2
	---- ---- ---- 1---	LD3	U18
	---- ---- ---1 ----	LD4	U3
	---- ---- --1- ----	LD5	U19
	---- ---- -1-- ----	LD6	U4
	---- ---- 1--- ----	LD7	U20
	---- ---1 ---- ----	LD8	U5
	---- --1- ---- ----	LD9	U21
	---- -1-- ---- ----	LD10	U6
	---- 1--- ---- ----	LD11	U22
	---1 ---- ---- ----	LD12	U7
	--1- ---- ---- ----	LD13	U23
	-1-- ---- ---- ----	LD14	U8
	1--- ---- ---- ----	LD15	U24

LD = Low Data

4-32. REFRESH TEST.

4-33. Display. This display shows the two Refresh test categories available and their test results. Use the display to review test conditions.

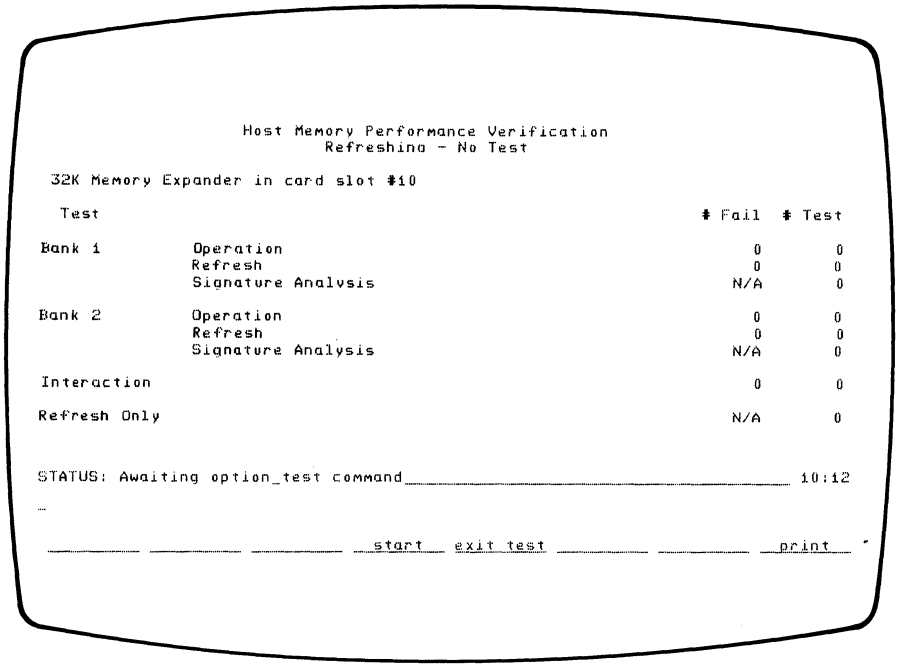


Figure 4-5. Refresh Test Display

4-34. Running the Refresh Tests. When this screen is displayed, the two tests are always running. Press the "exit_test" softkey to stop the tests and return to the Total PV Display. Each iteration takes approximately ten seconds.

4-35. Using the Refresh Results. The total number of errors detected during the tests is shown in the # Fail column. Each error code in the Results column represents a single failure encountered during the last iteration. Each error code in the (cumulative) column represents the sum of all errors detected during the test. Cumulative error codes that differ from Results error codes indicate multiple, or intermittent errors. When the error codes are the same, the errors are systematic. Refer to the appropriate test for an explanation of what the test does and how to decode the errors.

4-36. DELAY TEST.

4-37. Purpose. This test (figure 4-5) checks for hard failures in the refresh circuitry (a HARD FAILURE implies firmware failure). When data cannot be written to the RAMs and read back correctly after waiting several refresh cycles, an error is noted. When this test fails and all other tests pass, the problem lies in the refresh circuit.

4-38. Decoding Delay Test Errors. All errors found are formatted as a four character hexidecimal word. Each character represents four binary digits, each digit corresponding to a single bit. To decode an error word, convert each character to its binary equivalent and compare it with the chart shown below. See Table 4-2 for hexidecimal-to-binary conversion,if necessary. For example, if the error word is 0A00, there are errors on the LD9 and LD11 data paths. The U-number shown in the chart indicates the RAM that may have a failure.

a. Delay Test Errors.

Hex	Binary	Signal in error/RAM	
xxxx=	0000 0000 0000 0000	None	
	---- ---- ---- ---1	LD0	U1
	---- ---- ---- --1-	LD1	U17
	---- ---- ---- -1--	LD2	U2
	---- ---- ---- 1---	LD3	U18
	---- ---- ---1 ----	LD4	U3
	---- ---- --1- ----	LD5	U19
	---- ---- -1-- ----	LD6	U4
	---- ---- 1--- ----	LD7	U20
	---- ---1 ---- ----	LD8	U5
	---- --1- ---- ----	LD9	U21
	---- -1-- ---- ----	LD10	U6
	---- 1--- ---- ----	LD11	U22
	---1 ---- ---- ----	LD12	U7
	--1- ---- ---- ----	LD13	U23
	-1-- ---- ---- ----	LD14	U8
	1--- ---- ---- ----	LD15	U24

LD = Low Data

4-39. TIMING TEST.

4-40. Purpose. Soft failures of the refresh circuit are detected in this test (figure 4-5). A SOFT FAILURE implies a software failure. When the circuit refreshes memory more frequently than necessary, the power consumption on the +12 volt supply increases. Also, the mainframe CPU accesses may be delayed by this condition. The test detects statistically significant deviations from normal CPU access rates over a timed interval. When the access rate is not within the normal range, a failure is flagged.

4-41. Decoding Timing Errors. The errors found in this test are not decoded. When the test fails and all other tests pass, the failure is probably associated with refresh operation or the multiplexers U49, U50, or U79 - U82.

4-42. SIGNATURE ANALYSIS TEST

4-43. There is no separate display for this test. This test is not used.

4-44. INTERACTION TEST.

4-45. Display. There is no seperate display for this test. See the total PV Display, figure 4-3.

4-46. Running the Interaction Test. Position the highlight line over the words "Interaction" on the Total PV display and press the "disp_test" softkey. Then press the "start" softkey which appears on the lower level display. To exit the test, press the "exit_test" softkey.

4-47. Purpose. Tests whether BANK 1 and BANK 2 are operating independently. It will also test whether or not RAM is always enabled. The test writes 0000 HEX to BANK 1 and writes FFFF HEX to BANK 2. It then reads BANK 1 and writes 0000 to BANK 2 and then reads BANK 2. This test is repeated with the same data but with the BANKs switched. Any bits which do not have the expected values are flagged as errors.

4-48. Decoding the Errors. Any interacion where some or all of the data written to one BANK is found in the other will probably be associated with the address bus. If LMAP1 is true during the address cycle, then BANK 1, the lower 16K, is being addressed. If LMAP1 is false during the address cycle, then BANK 2, the upper 16K, is being addressed. The enable lines should be checked.

4-49. REFRESH ONLY TEST.

4-50. Display. There is no separate display for this test because this test is not used.

Table 4-2. Error Code Conversion

Hex	Binary	Hex	Binary	Hex	Binary	Hex	Binary
0	----	4	-1--	8	1---	C	11--
1	---1	5	-1-1	9	1--1	D	11-1
2	--1-	6	-11-	A	1-1-	E	111-
3	--11	7	-111	B	1-11	F	1111

4-51. TROUBLESHOOTING USING SIGNATURE ANALYSIS.

4-52. Signature Analysis (SA) offers a fast and convenient method of isolating hardware logic failures down to the component level. The basic concept is to utilize a known set of start, stop and clock signals that constantly repeat (loop) with the same timing relationships. When a suspect logic node is probed with a Signature Analyzer while using the start, stop, and clock signals as control inputs, the digital readout (signature) displayed on the analyzer can be compared with the normal signature of that node to determine if the timing relationships are proper. With the 64100A Mainframe, looping is provided by the PV software program and the normal signatures for various nodes are listed in the tables 4-10 thru 4-28.

4-53. SERVICE TOOLS.

4-54. SUGGESTED SERVICE TOOLS ARE:

1. HP 5004A or 5005A Signature Analyzer
2. Digital Voltmeter
3. Oscilloscope
4. Standard hand tools for electronic PC board repair.

4-55. SA TABLES.

4-56. The basic procedure is to refer to the appropriate table (i.e., the one that corresponds to the loop that PV was exercising when the failure was noted) and connect the Signature Analyzer to the Test Points called for in the table. Next, verify that the Vh signature indicated in the test set-up is proper. This signature is very important since it verifies that the start, stop and clock signals are normal. If this signature is good, proceed with the signatures listed in the table while referring to the appropriate schematic for guidance. If an improper signature is noted, check on both sides of the device to determine if it is causing the problem or if the problem has its origin further upstream.

4-57. If SA is taken using a 5004A Signature Analyzer, and loop S is good, it will be necessary to troubleshoot the shift registers U76 and U77 to the video output signals LIVID and LIVD with an oscilloscope and logic probe. However, if a 5005A Signature Analyzer is used, SA can be taken. The reason being, this circuitry is run by a 25 MHz signal called DOTCLK and the 5004A will not operate at that speed. If the signatures in loop S are good, and the circuitry from the shift registers U76 and U77 to the video output check good, then check the high voltage, the horizontal sync, and the vertical sync on the Display Driver board. Waveforms for the sync signals are provided in section VIII.

4-58. DISPLAY CONTROLLER TROUBLESHOOTING.

4-59. RAM TROUBLESHOOTING.

4-60. RAM troubleshooting is divided into simple RAM failure and RAM refresh failure. Different circuitry may be causing the different failure types.

Table 4-3. RAM Troubleshooting

REFRESH ERROR ON DISPLAY....go to RAM refresh failure trouble-shooting table.

SIMPLE RAM ERROR ON DISPLAY....go to simple RAM failure trouble-shooting table.

ILLEGIBLE DISPLAY....use signature analysis test loop determination table to discern failure type.

REFRESH ERROR....go to RAM refresh failure troubleshooting table.

SIMPLE RAM ERROR....go to simple RAM failure troubleshooting table.

Table 4-4. Simple RAM Failure Troubleshooting

STEP 1. LEGIBLE DISPLAY?

YES....replace RAM(s)

DOESN'T FIX PROBLEM....go to step 2. Since the RAM is used to store display information, the failure may be corrupting the displayed failure information. The SA RAM failure summary table will give you this information.

NO....go to step 2. Since the RAM is used to store display information, the failure may be corrupting the displayed failure information. The SA RAM failure summary table will give you this information.

STEP 2. RAM FAILURE SUMMARY....use the RAM failure summary SA setup table to find failing RAM IC(s) and replace.

DOESN'T FIX PROBLEM....go to step 3. The failure may be due to a failure in the data path to the RAM, addressing or control. CPU RAM writes will allow you to check for this type of failure.

STEP 3. CPU RAM WRITES....use signature analysis setup K table (CPU RAM writes setup). First, check the ability of the CPU to write information to the RAM.

GOOD Vh....take signatures

BAD SIGS ON RAM TIMING AND CONTROL SIGNALS....use signature analysis setup U table (RAM cycle selector/generator setup) to troubleshoot. If these signals are not correct information may not be written to or read from RAM correctly. Since these signals are mostly Vh and 0000, an error in these signals may not be detected.

BAD SIGS ON MEMORY DATA OR ADDRESS BUS.
These bad signatures indicate a failure of the CPU to write correct data to RAM. This could be due to the CPU, the connections from the CPU to the RAM, the pullups on the MB, the address latches on the CPU I/O board, any IC that connects to the buses, or the address multiplexers.

NO BAD SIGNATURES....go to step 4. The addresses checked in CPU RAM writes was only during the CAS strobe portion of the address. A failure in the row/column multiplexers might not be detected. CPU RAS address check will let you find a failure of this type.

BAD Vh....troubleshoot the signature analysis latch and the CPU timing and control circuitry on the CPU,I/O board using a scope.

STEP 4. CPU RAS ADDRESS CHECK....use signature analysis setup L table (CPU RAS address check setup).

BAD Vh....go to signature analysis setup U table (RAM cycle selector/generator setup) to troubleshoot.

GOOD Vh.

NO BAD SIGS....go to step 5.

TIMING AND CONTROL SIGNATURE ERRORS....use signature analysis setup U table (RAM cycle select/generator setup) to troubleshoot.

STEP 5. ADDRESS SIGNATURE ERRORS....use signature analysis setup M table (CPU RAM reads setup). Before signatures on the output of the RAM can be correct, addressing and data from the CPU must be correct. You should have already checked these functions using CPU RAM writes and CPU RAS address check.

BAD Vh.

NO CLOCK SIGNAL....go to signature analysis setup U table (RAM cycle selector/generator setup) to troubleshoot.

NO START/STOP SIGNAL....go to ROM troubleshooting table.

GOOD Vh.

RAM or RAM ADDRESS TIMING AND CONTROL SIG ERRORS....go to signature analysis setup U table (RAM cycle selector/generator setup) to troubleshoot.

DATA CONTROL AND DECODE SIG. ERRORS....use signature analysis setup N table (RAM access control and decode setup) to troubleshoot.

DATA OR ADDRESS SIGNATURE ERRORS....troubleshoot.

4-61. RAM REFRESH FAILURE TROUBLESHOOTING.

4-62. RAM refresh is accomplished by the display accesses to RAM. Circuitry in the display counters causes a RAS address for each of the 128 row addresses of both banks of RAM to be generated as the display accesses the RAM for display information. Troubleshooting in this section will allow you to isolate problems with individual RAM ICs or with the display address counters, CRT controller, and control circuitry.

4-63. Retention of the RAM ICs may be greater than 1 sec. Even with refresh not operating, only a few RAM ICs may fail the RAM refresh test. Taking the key signatures in display RAS Address check will verify that the refresh circuitry is working.

Table 4-5. RAM Refresh Failure Troubleshooting

STEP 1. LEGIBLE DISPLAY?

YES....replace failing RAM IC(s)

DOESN'T FIX PROBLEM....go to step 2. Since the RAM is used to store display information, the failure may be corrupting the displayed failure information. The RAM failure summary SA setup table will give you this information.

NO....go to step 2. Since the RAM is used to store display information, the failure may be corrupting the displayed failure information. The signature analysis RAM failure summary table will give you this information.

STEP 2. RAM FAILURE SUMMARY....use the RAM failure summary SA setup table to find the failing RAM IC(s) and replace.

DOESN'T FIX PROBLEM....go to step 3. Refresh is accomplished by the display accesses to RAM, CRT controller outputs-hardware setup will check to see that the CRT controller is operating correctly.

STEP 3. CRT CONTROLLER OUTPUTS-HARDWARE....use signature analysis setup 0 table (CRT controller outputs-hardware loop setup).

BAD Vh.

NO CLOCK....troubleshoot.

NO START/STOP....go to step 5.

VALID Vh.

CRT CONTROLLER IC PINS 1-5, 7-8 SIGNATURE ERRORS....go to step 5. The CRT controller is not operating correctly, CPU program of the CRT controller will allow you to verify that the CRT controller is being programmed correctly by the CPU.

OTHER SIGNATURE ERRORS....troubleshoot

NO BAD SIGNATURES....go to step 4. If the display address counters are not working correctly, refresh may not be done. Addresses are checked only during the RAS portion of the address since the RAS addressing is what does the refresh for the RAM.

STEP 4. DISPLAY RAS ADDRESS CHECK....use signature analysis setup R table (display RAS address check setup).

BAD Vh.

NO CLOCK....use signature analysis setup U table (RAM cycle selector/generator setup) to troubleshoot.

NO START/STOP....go to step 5.

VALID Vh.

ADDRESS TIMING AND CONTROL SIG ERRORS....use signature analysis setup U table (RAM cycle selector/generator setup) to troubleshoot.

OTHER SIG ERRORS....troubleshoot.

STEP 5. CPU PROGRAM OF CRT CONTROLLER....use signature analysis setup P table (CPU program of CRT controller setup).

BAD Vh.

NO CLOCK....use signature analysis setup N table (RAM access control and decode setup) to troubleshoot.

NO START/STOP....go to ROM troubleshooting table, step 4.

VALID Vh.

BUFFER TIMING AND CONTROL SIG ERRORS....use signature analysis setup N table (RAM access control and decode setup) to troubleshoot.

NO BAD SIGNATURES....check power supplies and clock to CRT controller. If outputs are bad and all inputs are good, replace the CRT controller.

Table 4-6. Display Troubleshooting

ARE THE DISPLAY AND CHARACTERS THE CORRECT SIZE AND INTENSITY?.... First, isolate the problem to the Display Controller or driver boards.

YES....go to Display Controller troubleshooting table. The correct size indicates that the driver boards are operating correctly. If the display is wrong, it is because the display controller is sending the wrong video information.
NO....are HSYN, VSYN, and VIDEO signals correct coming from the Display Controller board?

YES....troubleshoot Display Driver

NO....go to Display Controller troubleshooting table.

Table 4-7. Display Controller Troubleshooting

STEP 1. CRT CONTROLLER OUTPUTS-DISPLAY TEST....use signature analysis setup S table (CRT controller outputs-display test setup).

BAD Vh.

NO CLOCK....troubleshoot with scope

NO START/STOP....go to step 3.

VALID Vh.

CRT CONTROLLER IC PINS 1-5, 7-8 SIGNATURE ERRORS....go to step 3. The CRT controller is not operating correctly, CPU program of the CRT controller will allow you to verify that the CRT controller is being programmed correctly by the CPU.

CRT CONTROLLER IC HCC0-6 OUTPUT SIGNATURE ERRORS....go to step 2. If the character code outputs are wrong, it may be because the CRT controller is getting wrong information from RAM

OTHER SIGNATURE ERRORS....troubleshoot.

NO BAD SIGNATURES....use scope to troubleshoot video circuitry. The video circuitry runs at 25 MHz; this is too fast for signature analysis so a scope is required to troubleshoot.

STEP 2. CRT CONTROLLER READ FROM RAM....use signature analysis setup T table (CRT controller read from RAM setup).

BAD Vh.

NO CLOCK....use signature analysis setup U table (RAM cycle selector/generator setup) to troubleshoot.

NO START/STOP....use signature analysis setup O table (CRT controller outputs-hardware loop setup) to troubleshoot.

VALID Vh.

RAM TIMING AND CONTROL OR ADDRESS MUX CONTROL SIG ERRORS.. use signature analysis setup U table (RAM cycle selector-generator setup) to troubleshoot.

RAM DATA OUTPUT SIGNATURE ERRORS ONLY....use signature analysis setup R table (display RAS address check setup) to check RAS address to RAM. If no errors are found, suspect the RAM or any IC connected to the RAM memory data bus.

OTHER BAD SIGNATURES....troubleshoot.

NO BAD SIGNATURES....check power supplies and clock to CRT controller. If outputs are bad and all inputs are good, replace the CRT controller.

STEP 3. CPU PROGRAM OF CRT CONTROLLER....use signature analysis setup P table (CPU program of CRT controller).

BAD Vh.

NO CLOCK....signature analysis setup N table (RAM access control and decode setup) to troubleshoot.

NO START/STOP....go to ROM troubleshooting table, step 4.

BUFFER TIMING AND CONTROL SIG ERRORS....use signature analysis setup N table (RAM access control and decode setup) and signature analysis setup U table (RAM cycle selector/generator setup) to troubleshoot.

OTHER SIGNATURE ERRORS....troubleshoot.

NO BAD SIGNATURES....check power supplies and clock to CRT controller. If outputs are bad and all inputs are good, replace the CRT controller.

Table 4-8. SA Loop Determination

LOOPNAME and SETUP NAME: TEST LOOP DETERMINATION

The memory signature analysis latch is set and reset during the execution of the software tests. The interval is unique to the test being performed.

In the event that the display is not functioning correctly, this test can be used to determine which of the tests the mainframe is executing.

All option boards removed
All jumpers in the NORMAL position
ST/SP/START = pos. edge : CPU Bd. TP10 (MEM SA LATCH)
QUAL/STOP = neg. edge : CPU Bd. TP10 (MEM SA LATCH)
CLOCK = pos. edge : CPU Bd. TP1 (LSTB)

Signatures

Vh = CA27 POWER-ON RAM TEST LOOP - SIMPLE RAM FAILURE
Go to simple RAM failure troubleshooting.

Vh = AH68 POWER-ON RAM TEST LOOP - REFRESH FAILURE
Go to RAM refresh failure troubleshooting.

Vh = AU94 DISPLAY TEST
If wrong or no display, go to display troubleshooting.

Vh = XXXX NO RECOGNIZABLE Vh
Go to ROM troubleshooting

Table 4-9. RAM Failure Sumary

LOOPNAME: POWER-ON RAM TEST FAILURE OR REFRESH FAILURE

If a failure is detected during the power-on RAM self-test, the test enters a signature analysis loop that writes and reads RAM and stimulates the CRT controller. The loop also outputs the error mask onto the memory data bus and the CPU attempts to display the failing IC numbers.

Since the display information is stored in RAM, the output to the display of the failing RAM IC numbers may be illegible. This setup allows the taking of signatures on the memory data bus during the time that the error mask are present. The value of the signatures and data bit may be decoded to isolate the failing RAM IC numbers.

Executing power-on RAM test or refresh failure loop:

ST/SP/START = pos. edge : CPU Bd. TP10 (MEM SA LATCH)
QUAL/STOP = pos. edge : CPU Bd. TP10 (MEM SA LATCH)
CLOCK = pos. edge : CPU Bd. TP9

Vh = 0007

	Signature			
	0000	0002	0004	0006
Bit		Failing RAM on Display Controller Bd.		
LD0	no failure	U23	U51	U23, U51
LD1	no failure	U24	U52	U24, U52
LD2	no failure	U25	U53	U25, U53
LD3	no failure	U26	U54	U26, U54
LD4	no failure	U27	U55	U27, U55
LD5	no failure	U28	U56	U28, U56
LD6	no failure	U29	U57	U29, U57
LD7	no failure	U30	U58	U30, U58
LD8	no failure	U38	U65	U38, U65
LD9	no failure	U39	U66	U39, U66
LD10	no failure	U40	U67	U40, U67
LD11	no failure	U41	U68	U41, U68
LD12	no failure	U42	U69	U42, U69
LD13	no failure	U43	U70	U43, U70
LD14	no failure	U44	U71	U44, U71
LD15	no failure	U45	U72	U45, U72

Table 4-10. Signature Analysis Loop A

PC Board: Display Controller Board
Test failure or circuit: Power-up RAM Test failure
Procedure:
S/A hookup:
Start = Pos edge CPU Bd. TP10 (S.A. Interval)
Stop = Neg edge CPU Bd. TP10 (S.A. Interval)
Clock = Pos edge CPU Bd. TP1 (LSTB)
VH = CA27

Node	Sig	Node	Sig
U 65- 2	P29H	U 70- 3	F8UF
U 65- 5	9CPU	U 70- 5	3963
U 65-11	6445	U 70- 7	PA14
U 66- 2	50C0	U 70- 9	U175
U 66- 5	U94H	U 70-12	0UU7
U 66-11	APHS	U 70-14	H5H2
U 66-14	4534	U 70-16	C6FA
U 67- 2	A91A	U 70-18	F47H
U 67- 5	U664	U 71-11	F864
U 67-11	F8FF	U 71-12	1A71
U 68- 2	5FAC	U 71-13	C564
U 68- 5	2830	U 71-14	5CH1
U 68-11	4P85	U 71-15	H467
U 68-14	0128	U 71-16	1A92
		U 71-17	38HF
		U 71-18	PUUF

Table 4-11. Signature Analysis Loop B

PC Board: Display Controller Board
Test failure or circuit: Power-up RAM failure - Data writes to RAM
Procedure:
S/A hookup:
Start = Pos edge CPU Bd. TP10 (S.A. Interval)
Stop = Neg edge CPU Bd. TP10 (S.A. Interval)
Clock = Neg edge Disp Controller U21-10 (HWRT)
VH = 40P9
* = Probe Blinking

Node	Sig	Node	Sig
U 70- 1	40P9	U 71- 1	0000
U 70- 3	CPPZ	U 71-11	17F2
U 70- 5	F7C2	U 71-12	PCH0
U 70- 7	H7H9	U 71-13	643A
U 70- 9	07H2	U 71-14	9A6A
U 70-12	1H3P	U 71-15	PC5C
U 70-14	7C0C	U 71-16	8658
U 70-16	0CC1	U 71-17	A730
U 70-18	379A	U 71-18	6U1A
		U 71-19	40P9

Table 4-12. Signature Analysis Loop C

PC Board: Display Controller Board
Test failure or circuit: Power-up Ram failure
Procedure:
S/A hookup:
Start = Pos edge CPU Bd. TP10 (S.A. Interval)
Stop = Neg edge CPU Bd. TP10 (S.A. Interval)
Clock = Pos edge Disp Controller TP11 (HPRAS)
VH = 7H37
* = Probe Blinking

Node	Sig	Node	Sig
U 18- 7	0000	U 65- 2	2HP3
U 48- 5	7H37	U 65- 4	50H4
U 49- 4	2HP3	U 65- 5	626H
U 49- 7	626H	U 65- 7	1U5A
U 49- 9	170P	U 65- 9	6A39
U 50- 4	96CP	U 65-11	170P
U 50- 7	HACA	U 68- 2	96CP
U 50- 9	FH20	U 68- 4	PC89
U 50-12	463H	U 68- 5	HACA
		U 68-11	FH20
		U 68-12	3C0A
		U 68-14	463H

Table 4-13. Signature Analysis Loop D

PC Board: Display Controller
Test failure or circuit: Power-up RAM failure - Data write to RAM and column address
Procedure:
S/A hookup:
Start = Pos edge CPU Bd. TP10 (S.A. Interval)
Stop = Neg edge CPU Bd. TP10 (S.A. Interval)
Clock = Neg edge Disp Controller TP6 (LPCAS)
VH = 7H37
* = Probe Blinking

Node	Sig	Node	Sig
U 18- 7	0000	U 70- 3	H49A
U 48- 5	0000	U 70- 5	7957
U 49- 4	8C0C	U 70- 7	381P
U 49- 7	38HU	U 70- 9	PFP8
U 49- 9	40P0	U 70-12	A004
U 50- 4	0UH9	U 70-14	7929
U 50- 7	0337	U 70-16	UF98
U 50- 9	7143	U 70-18	2U5U
U 50-12	0U51	U 71-11	254F
U 66- 2	0UH9	U 71-12	295P
U 66- 4	72PP	U 71-13	U278
U 66- 5	0337	U 71-14	CF9A
U 66- 7	7P00	U 71-15	0HU4
U 66-11	7143	U 71-16	U506
U 66-12	7266	U 71-17	C763
U 66-14	0U51		
U 67- 2	8C0C		
U 67- 4	U63F		
U 67- 5	38HU		
U 67- 7	45P8		
U 67- 9	3HH7		
U 67-11	40P0		

Table 4-14. Signature Analysis Loop E

PC Board: Display Controller
Test failure or circuit: Power-up RAM failure, RAM outputs
Procedure:
S/A hookup:
Start = Pos edge CPU Bd. TP10 (S.A. Interval)
Stop = Neg edge CPU Bd. TP10 (S.A. Interval)
Clock = Pos edge Disp Controller TP15
Vh = P000

Node	Sig	Node	Sig
U 23-14	8AAA	U 38-14	AH28
U 31-3	8AAA	U 70-3	AH28
U 71-11	8AAA		
U 24-14	P444	U 39-14	C211
U 31-5	P444	U 70-5	C211
U 71-12	P444		
U 25-14	9838	U 40-14	APH6
U 31-7	9838	U 70-7	APH6
U 71-13	9838		
U 26-14	4A2H	U 41-14	6251
U 31-9	4A2H	U 70-9	6251
U 71-14	4A2H		
U 27-14	PU53	U 42-14	CF46
U 31-12	PU53	U 70-12	CF46
U 71-15	PU53		
U 28-14	4013	U 43-14	FF7H
U 31-14	4013	U 70-14	FF7H
U 71-16	4013		
		U 44-14	F8AA
U 29-14	5AH3	U 70-16	F8AA
U 31-16	5AH3		
U 71-17	5AH3		
		U 45-14	CUUU
U 30-14	A247	U 70-18	CUUU
U 31-18	A247		
U 71-18	A247		

Table 4-15. Signature Analysis Loop G

PC Board: Display Controller
Test failure or circuit: Power-up RAM failure
Procedure:
S/A hookup:
Start = Pos edge Disp Controller TP3 (Vert Sync)
Stop = Neg edge Disp Controller TP3 (Vert Sync)
Clock = Pos edge Disp Controller TP7 (HDRAS)
Vh = P5H2
* = Probe Blinking

Node	Sig	Node	Sig
U 17-3	CP11	U 58-11	A77S
U 18-7	P5H2*	U 58-12	8H02
U 21-2	SFC1	U 58-13	2P42
U 48-5	P5H2*	U 58-14	C963
U 49-4	CP11	U 58-15	S2A
U 49-7	AAU8	U 65-4	SCF3
U 49-9	4P5P	U 65-7	4U2A
U 50-4	6H2U	U 65-9	AC8F
U 50-7	A77S	U 68-4	88UH
U 50-9	8H01	U 68-7	42A7
U 50-11	1734	U 68-9	68H0
U 56-11	P2A0	U 68-12	FC90
U 56-12	AAU8		
U 56-13	4P5P		
U 56-14	6H2U		
U 56-15	SU8F		

NOTE: If the signatures of U65 and U68 are unstable, use NEG clock edge for these two components.

Table 4-16. Signature Analysis Loop H

PC Board: Display Controller
Test failure or circuit: Power-up RAM failure
Procedure:
S/A hookup:
Start = Pos edge Disp Controller TP3 (Vert Sync)
Stop = Neg edge Disp Controller TP3 (Vert Sync)
Clock = Neg edge Disp Controller TP13
Vh = P5H2
* = Probe Blinking

Node	Sig	Node	Sig
U 1 -11	P5H2*	U 57-11	6C86
		U 57-12	8P54
U 17-5	P5H2*	U 57-13	U2P6
U 17-6	0000*	U 57-14	73P7
U 18-7	P5H2*	U 66-4	8P54
		U 66-7	6C86
U 47-6	P5H2*	U 66-9	1734
		U 66-12	9635
U 48-5	0000*		
		U 67-4	P5H2*
U 49-4	0000*	U 67-7	P5H2*
U 49-7	0000*	U 67-9	P5H2*
U 49-9	0000*		
U 50-4	6C86		
U 50-7	8P54		
U 50-9	U2P6		
U 50-12	73P7		

Table 4-17. Signature Analysis Loop I

PC Board: Display Controller
Test failure or circuit: Any test - Arbitrator circuit - No clocks on TP6, TP7, or TP11.

Procedure:
Remove CPU Bd., I/O Bd., and Disp Driver Bd. Move TEST jumper to TEST position.

S/A hookup:
Start = Pos edge TP14
Stop = Pos edge TP14
Clock = Pos edge TP2
Vh = UP73
* = Probe Blinking

Node	Sig	Node	Sig
U1-3	55H1	U20-6	UP73
U1-8	UP51	U20-8	H4C1
U2-11	8135	U22-1	0000
U2-12	86F1	U22-4	0000
U2-14	ACA2	U22-13	669P
U5-11	8117	U35-1	0022
		U35-4	2275
U9-13	ACA2		
U10-6	UP73*	U36-8	UP73
U10-7	55H1	U36-11	HF06
U15-3	7U24	U37-3	7U46
U15-6	UP73	U37-6	UP51
U15-8	UP73	U37-8	7U46
		U37-11	7U24
U16-6	UF74		
U16-8	UF74	U48-5	7U46
		U48-9	7U06
U18-7	HF06	U48-11	0022
U18-9	2275		

Table 4-18. Signature Analysis Loop K

LOOPNAME: POWER ON RAM TEST - SETUP NAME: CPU RAM WRITES

If a failure is detected during the power-on RAM self test, the test enters a signature analysis loop that writes and reads RAM and stimulates the CRT controller. The loop outputs the error mask onto the memory data bus and the CPU attempts to display the failing IC number(s).

This setup allows the checking of the CPU data path to the RAM during the write to RAM by the CPU. The CPU address path from the CPU to the multiplexers is also checked. The mainframe may be forced to execute the power-on RAM failure test by removing RAM IC A5U23.

ST/SP/START = pos. edge : CPU TP10 (SA LATCH) [NORMAL MODE]
QUAL/STOP = neg. edge : CPU TP10 (SA LATCH)
CLOCK = pos. edge : CPU TP13 (LMWRT)

VH = H37A

U 16- 6	0001	U 70- 3	728H
U 16- 8	0001	U 70- 5	UH82
		U 70- 7	UF05
U 23- 3	0001	U 70- 9	1UPA
U 23- 4	0001	U 70-12	9093
		U 70-14	P58U
		U 70-16	84H6
U 37- 8	0001	U 70-18	F35F
U 38- 3	0001	U 71-11	7045
		U 71-12	P6FF
U 65- 2	63F3	U 71-13	C9HH
U 65- 5	P8FC	U 71-14	3H08
U 65-11	61C1	U 71-15	P1H6
U 65-14	1P30	U 71-16	4F3A
		U 71-17	2AU8
U 66- 2	U7H3	U 71-18	3121
U 66- 5	HA56		
U 66-11	44P6		
U 66-14	8A4P		
U 67- 2	0001		
U 67- 5	1A8F		
U 67-11	F7PA		
U 67-14	683U		
U 68- 2	6U3A		
U 68- 5	87F2		
U 68-11	6019		
U 68-14	U08C		

Table 4-19. Signature Analysis Loop L

LOOPNAME: POWER-ON RAM TEST - SETUP NAME: CPU RAS ADDRESS CHECK

This setup checks CPU addressing during the RAS address to RAM. The mainframe may be forced to execute the RAM failure by removing RAM IC A5U23.

ST/SP/START = pos. edge : CPU TP10 (SA LATCH) [NORMAL MODE]
QUAL/STOP = neg. edge : CPU TP10 (SA LATCH)
CLOCK = pos edge : DSP TP11 (HPRAS)

VH = 7H37

U 16- 6	7H37	U 65- 2	2HP3	U68-11	FH20
U 16- 8	7H37	U 65- 4	50H4	U68-12	3C0A
		U 65- 5	626H	U68-14	463H
U 18- 7	0000	U 65- 7	1U5A		
U 18-11	0000	U 65- 9	6A39		
U 18-12	0000	U 65-11	170P		
		U 65-12	7266		
U 23- 3	7H37	U 65-14	0U51		
U 23- 5	463H				
U 23- 6	HACA	U 66- 2	40P0		
U 23- 7	FH20	U 66- 4	3HH7		
U 23- 9	0U51	U 66- 5	0UH9		
U 23-10	626H	U 66- 7	72PP		
U 23-11	170P	U 66- 9	7P00		
U 23-12	96CP	U 66-11	0337		
U 23-13	2HP3	U 66-12	0F74		
U 23-15	7H37	U 66-14	7143		
U 38- 3	7H37	U 67- 2	0000		
		U 67- 4	7H37		
U 48- 4	7H37	U 67- 5	8694		
U 48- 5	7H37	U 67- 7	UCA3		
		U 67- 9	U63F		
U 49- 4	2HP3	U 67-11	8C0C		
U 49- 7	626H	U 67-12	45P8		
U 49- 9	170P	U 67-14	38HU		
U 49-12	0U51				
		U 68- 2	96CP		
U 50- 4	96CP	U 68- 4	PC89		
U 50- 7	HACA	U 68- 5	HACA		
U 50- 9	FH20	U 68- 7	A78H		
U 50-12	463H	U 68- 9	C017		

Table 4-20. Signature Analysis Loop M

LOOPNAME: POWER-ON RAM TEST - SETUP NAME: CPU READS RAM

This setup checks the data as it is being read from RAM by the CPU, addressing by the CPU, and CAS addressing to RAM. The mainframe may be forced to execute the RAM failure loop by removing RAM IC A5U23.

ST/SP/START = pos. edge : CPU TP10 (SA LATCH) [NORMAL MODE]
QUAL/STOP = neg. edge : CPU TP10 (SA LATCH)
CLOCK = pos. edge : DSP TP15 (U31 ENABLE)

VH = P000

U 1- 8	P000	U 31- 3	8AAA
		U 31- 4	5AH3
U 7- 3	P000	U 31- 5	P444
		U 31- 6	4013
U 15- 4	H555	U 31- 7	9838
U 15- 5	high	U 31- 8	PU53
U 15- 6	high	U 31- 9	4A2H
U 15- 8	high	U 31-11	4A2H
U 15-10	3555	U 31-12	PU53
		U 31-13	9838
U 16- 1	high	U 31-14	4013
U 16- 2	0000	U 31-15	P444
U 16- 4	P000	U 31-16	5AH3
U 16- 5	0000	U 31-17	8AAA
U 16- 6	P000	U 31-18	A247
U 16- 8	P000	U 31-19	0000
U 18- 7	0000	U 35-10	0000
U 18- 9	P000		
		U 37- 8	P000
U 21- 8	3555	U 37-10	0000
U 21-10	0000	U 37-11	P000
		U 37-12	0000
U 23- 3	P000		
U 23- 4	P000	U 46- 1	P000
U 23- 5	H555	U 46-11	P000
U 23- 6	9F7F		
U 23- 7	5CCC	U 48- 2	P000
U 23- 9	3C89	U 48- 4	0000
U 23-10	1PFH	U 48- 5	P000
U 23-11	PAFA		
U 23-12	CH21	U 49- 4	C2F8
U 23-13	C2F8	U 49- 7	1PFH
U 23-15	P000	U 49- 9	PAFA
		U 49-12	3C89
U 31- 1	0000		
U 31- 2	A247		

Table 4-20. Signature Analysis Loop M (Cont'd)

U 50- 4	CH21
U 50- 7	9F7F
U 50- 9	5CCC
U 50-12	H555
U 51- 6	0000
U 51- 8	955U
U 65- 2	C2F8
U 65- 4	52F8
U 65- 5	1PFH
U 65- 7	UPFH
U 65- 9	0AFA
U 65-11	PAFA
U 65-12	HC89
U 65-14	3C89
U 66- 2	3AP7
U 66- 4	HAP7
U 66- 5	U293
U 66- 7	1293
U 66- 9	HPP0
U 66-11	3PP0
U 66-12	2H70
U 66-14	FH70
U 67- 2	0000
U 67- 4	P000
U 67- 5	955U
U 67- 7	755U
U 67- 9	3827
U 67-11	H827
U 67-12	3C96
U 67-14	HC96
U 68- 2	CH21
U 68- 4	5H21
U 68- 5	9F7F
U 68- 7	7F7F
U 68- 9	CCCC
U 68-11	5CCC

U 69- 8	P000
U 70- 1	P000
U 70- 2	CUUU
U 70- 3	AH28
U 70- 4	F8AA
U 70- 5	C211
U 70- 6	FF7H
U 70- 7	APH6
U 70- 8	CF46
U 70- 9	6251
U 70-11	6251
U 70-12	CF46
U 70-13	APH6
U 70-14	FF7H
U 70-15	C211
U 70-16	F8AA
U 70-17	AH28
U 70-18	CUUU
U 71- 1	P000
U 71-11	8AAA
U 71-12	P444
U 71-13	9838
U 71-14	4A2H
U 71-15	PU53
U 71-16	4013
U 71-17	5AH3
U 71-18	A247
U 71-19	P000

Table 4-21. Signature Analysis Loop N

LOOPNAME: POWER-ON RAM TEST - SETUP NAME: RAM ACCESS CONTROL AND DECODE

This setup is used to troubleshoot the control circuitry used to enable the RAM data buffers during CPU accesses to RAM and to the CRT controller. The mainframe may be forced to execute the power-on RAM test failure loop by removing RAM ICA5U23.

ST/SP/START = pos. edge : CPU TP10 (SA LATCH) [NORMAL MODE]
QUAL/STOP = neg. edge : CPU TP10 (SA LATCH)
CLOCK pos. edge : CPU TP1 (LSTB)

VH = CA27

U 1- 8	HC2U	U 69- 1	HC2U
		U 69- 2	HF62
U 5- 3	75FC	U 69- 3	074H
		U 69- 5	HC2U
U 7- 3	3785	U 69- 6	APP5
		U 69- 8	U869
U 15-11	2347	U 69-10	0000
		U 69-11	3785
U 21- 3	6645		
U 21- 4	HF62		
U 21-10	U869		
U 21-11	424P		
U 35-10	8HA2		
U 47- 3	2347		
U 64- 1	U664		
U 64- 2	F8FF		
U 64- 3	5FAC		
U 64- 4	APH5		
U 64- 5	A91A		
U 64- 6	2838		
U 64- 7	4P85		
U 64- 9	5HCA		
U 64-10	U94H		
U 64-11	6445		
U 64-12	9CPU		
U 64-13	50C0		
U 64-14	4534		
U 64-15	P29H		

Table 4-22. Signature Analysis Loop 0

LOOPNAME and SETUP NAME: CRT CONTROLLER OUTPUTS-HARDWARE LOOP

By moving jumpers A5J2 and A5J3 to the test position, the CRT accesses to RAM are disabled. The CRT controller still is still accessed by the CPU and configured. The CRT controller provides horizontal and vertical retrace signals to horizontal and vertical sync circuitry.

This setup allows checking the horizontal and vertical sync circuitry for proper configuration of the CRT controller IC.

ST/SP/START pos. edge : DSP TP16 (HVRTC) [NORMAL MODE]
QUAL/STOP pos. edge : DSP TP16 (HVRTC)
CLOCK pos. edge : DSP TP4 (HCHAR)

VH = HU61

U 3- 3	745H	U 53- 6	FU65
U 3- 7	8C75	U 53- 9	34A6
U 3- 9	212H		
		U 61-11	P54H
U 11- 6	589H		
U 11- 8	4179	U 62-15	268H
U 11- 9	AC3F		
		U 63- 5	08PU
U 12- 9	9A00	U 63- 9	2A82
U 12-11	FU65		
		U 72- 8	P54H
U 33- 1	AC3F		
U 33- 2	5414	U 74-11	3A2F
U 33- 3	63UP		
U 33- 4	UP4F	U 78- 5	2HCC
U 33- 5	3763	U 78- 9	P54H
U 33- 7	HA1H		
U 33- 8	2008		
U 33-30	HU61		

Table 4-23. Signature Analysis Loop P

LOOPNAME: POWER ON RAM TEST - SETUP NAME: CPU PROGRAM OF CRT CONTROLLER

This setup allows the checking of the data path from the CPU to the CRT controller IC, addressing, and control. The mainframe may be forced to execute the RAM failure loop by removing RAM IC A5U23.

ST/SP/START = pos. edge : CPU TP10 (SA LATCH) [NORMAL MODE]
QUAL/STOP = neg. edge : CPU TP10 (SA LATCH)
CLOCK = pos. edge : DSP TP17 (LCS)

VH = H7P4

U 5- 3	0000	U 69- 8	H7P4
U 5- 6	AP7C	U 69-11	0000
		U 69-12	H7P4
U 7- 3	0000		
U 7- 6	H7P4	U 71- 1	0000
		U 71- 2	A391
U 15-11	H7P4	U 71- 3	2235
		U 71- 4	8242
U 17- 6	0000	U 71- 5	HPU1
		U 71- 6	A9A4
U 21- 3	H7P4	U 71- 7	AA06
U 21- 4	0000	U 71- 8	H2A3
		U 71- 9	U898
U 31- 1	H7P4	U 71-11	U898
		U 71-12	H2A3
U 32- 1	H7P4	U 71-13	AA06
		U 71-14	A9A4
U 33-12	7172	U 71-15	HPU1
U 33-13	0547	U 71-16	8242
U 33-14	F9F3	U 71-17	2235
U 33-15	0A5F	U 71-18	A391
U 33-16	0915	U 71-19	0000
U 33-17	55A6		
U 33-18	U5H1	U 75- 8	H7P4
U 33-19	7475	U 75-10	0000
		U 75-11	0000
U 35-13	12U8		
U 46- 1	H7P4		
U 46-11	H7P4		
U 47- 8	H7P4		

Table 4-24. Signature Analysis Loop R

LOOPNAME: POWER-ON RAM TEST FAILURE - SETUP NAME: DISPLAY RAS ADDRESS CHECK

The refresh of dynamic RAM is performed by a RAS to each row address of RAM as the CRT controller IC accesses RAM for display data. The display addressing and refresh circuitry are checked during RAS. Since the display is operated during the RAM failure loop, the mainframe may be forced into this loop by removing RAM IC A5U23.

ST/SP/START = pos. edge : DSP TP16 (HVRTC) [NORMAL MODE]
QUAL/STOP = pos. edge : DSP TP16 (HVRTC)
CLOCK = pos. edge : DSP TP7 (HDRAS)

VH = 279A

U 5- 8 279A	U 35- 4 low	U 58-11 0H97
U 5- 9 279A		U 58-12 AH4P
		U 58-13 861H
U 7-11 279A	U 37- 6 high	U 58-14 F513
U 7-12 P5H2	U 37-11 279A	U 58-15 8447
	U 37-12 0000	
U 8- 6 72P9		U 65- 4 C811
U 8- 8 0000		U 65- 7 12F0
U 8- 9 279A	U 38- 3 279A	U 65- 9 19A8
		U 65-12 FCHU
U 15- 5 high	U 48- 5 279A	
U 15- 6 high		U 66- 4 279A
U 15- 8 high	U 49- 4 9U8C	U 66- 7 8P54
	U 49- 7 355A	U 66- 9 U424
U 16- 2 0000	U 49- 9 3P32	U 66-12 4AHP
U 16- 6 279A	U 49-12 PF45	
U 16- 8 279A		U 67- 4 279A
U 16-10 0000	U 50- 4 46H1	U 67- 7 279A
	U 50- 7 0H97	U 67- 9 279A
U 17- 3 9U8C	U 50- 9 AH4P	U 67-12 279A
	U 50-12 861H	
U 18- 7 279A		U 68- 4 614C
	U 56-11 7H02	U 68- 7 2A0H
U 21- 2 P289	U 56-12 355A	U 68- 9 8AH4
	U 56-13 3P32	U 68-12 A187
U 23- 3 279A	U 56-14 46H1	
U 23- 4 279A	U 56-15 1355	
U 23- 5 861H		
U 23- 6 0H97	U 57-11 A9FP	
U 23- 7 AH4P	U 57-12 H3CP	
U 23- 9 PF45	U 57-13 6H44	
U 23-10 355A	U 57-14 PF45	
U 23-11 3P32		
U 23-12 46H1		
U 23-13 9U8C		
U 23-15 279A		

Table 4-25. Signaure Analysis Loop S

LOOPNAME: DISPLAY TEST - SETUP NAME: CRT CONTROLLER OUTPUTS-DISPLAY TEST

During the display test, signature analysis loops are set and reset around the repetitive display pattern. Control stimulus is provided to the CRT controller IC during the display loop.

This setup allows the checking of the CRT controller IC outputs including the character code outputs and control signals. It also allows the checking of the character generator ROM and HSYN and VSYN circuitry.

ST/SP/START = pos. edge : DSP TP16 (HVRTC) [NORMAL MODE]
QUAL/STOP = neg. edge : DSP TP16 (HVRTC)
CLOCK = pos. edge : DSP TP4 (HCHAR)

VH = UA11

U 3- 3	676P	U 33- 1	9H7U	U 54- 2	0000
U 3- 5	5HP8	U 33- 2	A903	U 54- 6	0000
U 3- 7	5312	U 33- 3	CP98	U 54-10	0000
U 3- 9	C18H	U 33- 4	4C9F	U 54-11	UA11
U 3-12	676P	U 33- 7	8554		
U 3-14	5312	U 33- 8	UA11	U 60- 9	738F
U 3-16	4489	U 33-23	A7U9	U 60-10	C67P
U 3-18	C18H	U 33-24	731A	U 60-11	3930
		U 33-25	1939	U 60-13	417H
U 4- 3	U239	U 33-26	58H3	U 60-14	C8PU
U 4- 5	P328	U 33-27	73F8	U 60-15	56A6
U 4- 7	890C	U 33-28	U239	U 60-16	2PP7
U 4- 9	7U45	U 33-29	0828	U 60-17	0000
U 4-12	A2F2	U 33-35	UA11		
U 4-14	89H9	U 33-36	0000	U 61-15	9FA1
U 4-16	0828	U 33-37	0000		
U 4-18	0000			U 62-15	3F33
		U 53- 3	0000		
U 9- 1	0472	U 53- 6	8719	U 63- 5	06H6
		U 53- 8	UP63	U 63- 9	0520
U 11- 6	1U91	U 53- 9	0472		
U 11- 8	P1F7	U 53-11	0000	U 72- 8	127U
U 12- 9	UA11			U 74-11	P86P
U 17- 8	9H7U			U 78- 3	UA11
				U 78- 5	8719
				U 78- 9	127U

Table 4-26. Signature Analysis Loop T

LOOP NAME: DISPLAY TEST - SETUP NAME: CRT CONTROLLER READ FROM RAM

During the display test, signature analysis loops are set and reset around the repetitive display pattern.

This setup checks circuitry associated with the CRT controller accesses to RAM which consists of address counters, data path, and control of the data buffers and data latch.

ST/SP/START = pos. edge : DSP TP3 (VSYN) [NORMAL MODE]
QUAL/STOP = neg. edge : DSP TP3 (VSYN)
CLOCK = pos. edge : DSP TP13 (LDCAS)

VH = P5H2

		U 19- 3	A6FC
U 1- 8	P5H2	U 19- 6	PUC9
U 1-11	5FC1	U 19- 8	96UA
U 2-11	0000	U 21- 2	5FC1
U 5- 6	0000	U 23- 3	P5H2
U 5- 8	0000	U 23- 4	P5H2
		U 23- 5	U2P6
U 7- 6	P5H2	U 23- 6	6C86
U 7-11	P5H2	U 23- 7	8P54
		U 23- 9	0000
U 8- 6	72P9	U 23-10	0000
U 8- 8	0000	U 23-11	0000
U 8- 9	P5H2	U 23-12	0000
		U 23-13	0000
U 9-10	H5AU	U 23-15	0000
U 12- 5	P5H2	U 32- 2	75CF
U 12- 6	0000	U 32- 3	901U
		U 32- 4	CF87
U 13- 1	74P7	U 32- 5	A454
U 13- 4	6179	U 32- 6	78AH
U 13-10	4186	U 32- 7	84AC
U 13-13	75FH	U 32- 8	2AF2
		U 32- 9	9135
U 15-11	P5H2	U 32-11	5616
		U 32-12	0A6C
U 16- 6	P5H2	U 32-13	7U21
U 16- 8	P5H2	U 32-14	307H
		U 32-15	72CP
U 17- 3	CP11	U 32-16	4319
U 17- 6	P5H2	U 32-17	A164
		U 32-18	7328
U 18- 5	P5H2	U 32-19	5FC1
U 18- 7	P5H2		
U 18- 9	0000	U 33- 5	0000

Table 4-26. Signature Analysis Loop T (Cont'd)

U 35-13	0000
U 37- 3	low
U 37- 6	high
U 37- 8	P5H2
U 37-11	0000
U 38- 3	P5H2
U 46- 2	7328
U 46- 3	4657
U 46- 4	FPP0
U 46- 5	4319
U 46- 6	307H
U 46- 7	CH8H
U 46- 8	2522
U 46- 9	0A6C
U 46-12	9135
U 46-13	FPHC
U 46-14	6U9U
U 46-15	84AC
U 46-16	A454
U 46-17	1315
U 46-18	PFUA
U 46-19	901U
U 47- 3	P5H2
U 47- 6	C963
U 47- 8	P5H2
U 49- 4	0000
U 49- 7	0000
U 49- 9	0000
U 49-12	0000
U 50- 4	0000
U 50- 7	6C86
U 50- 9	8P54
U 50-12	U2P6
U 56-11	P2A0
U 56-12	AAU8
U 56-13	4P5P
U 56-14	6H2U
U 56-15	5U8F
U 57-11	6C86
U 57-12	8P54
U 57-13	U2P6
U 57-14	73P7
U 57-15	high
U 58-11	A775
U 58-12	8H02
U 58-13	2P42
U 58-14	C963
U 58-15	52A2
U 65- 4	5CF3
U 65- 7	4U2A
U 65- 9	AC8F
U 65-12	9635
U 66- 4	P5H2
U 66- 7	8P54
U 66- 9	6C86
U 66-12	1734
U 67- 4	P5H2
U 67- 7	P5H2
U 67- 9	P5H2
U 67-12	P5H2
U 68- 4	88UH
U 68- 7	42A7
U 68- 9	68H0
U 68-12	FC90
U 69- 5	P5H2
U 69- 6	P5H2
U 69-11	P5H2
U 69-12	P5H2
U 69-13	P5H2
U 75- 8	P5H2

Table 4-27. Signature Analysis Loop U

LOOPNAME and SETUP NAME: RAM CYCLE SELECTOR/GENERATOR

This is a hardware loop. By moving the test jumper A5P4 from the normal (XU2) to the test (XU1) position, the RAM cycle selector/generator is forced to run at the RAM clock rate.

This setup checks the RAM cycle selector/generator circuitry.

ST/SP/START = pos. edge : DSP TP14 (RCARRY) [NORMAL MODE]
QUAL/STOP = pos. edge : DSP TP14 (RCARRY)
CLOCK = pos. edge : DSP TP2 (HRAMCLK)

VH = UP73

U 1- 3	ACA2		
U 1- 8	UP51	U 22- 1	low
		U 22- 4	low
U 2-11	8135	U 22- 8	low
U 2-12	86F1	U 22- 9	high
U 2-13	98PH	U 22-10	low
U 2-14	ACA2	U 22-13	669P
U 5-11	8117	U 23- 3	UF74
		U 23- 4	7U46
U 9-11	ACA2	U 23-15	7U06
U 9-12	low		
U 9-13	55H1		
		U 35- 1	0022
U 15- 3	7U24	U 35- 4	low
U 15- 5	high		
U 15- 6	high	U 36- 3	high
U 15- 8	high	U 36- 6	ACU7
U 16- 6	UF74		
U 16- 8	UF74	U 37- 3	low
		U 37- 6	high
U 18- 7	HF06	U 37- 8	7U46
U 18- 9	2275	U 37-11	7U06
U 18-12	high		
		U 38- 3	UF74
U 20- 6	high		
U 20- 8	H4C1	U 48- 5	7U46
		U 48- 8	8175
U 21- 3	high	U 48- 9	7U06
U 21- 4	low		
U 21- 6	7U46	U 51-15	high
U 21- 8	low		
U 21-10	high	U 73-13	0022
U 21-11	low		

SECTION V

ADJUSTMENTS

5-1. DISPLAY DRIVER AND CRT ADJUSTMENTS.

a. Completely remove the five screws that secure the top cover. Also, remove the two (or four) screws that secure the state and timing ground clips to the rear panel. Lift and remove cover.

b. Set the system control source switches (see figure 5-1), located on the back panel, to the Performance Verification position; top part of both rocker switches should be pressed in.

c. Set the main power switch OFF and then ON. Note, the display test pattern should now be on the screen, as shown in figure 5-2.

d. Adjust variable inductor L3,(H Gain) for a display width of between 22.0cm (8-1/2 in) and 23.0cm (9 in).

e. Adjust potentiometer R1(H POS) so that the display test pattern is centered in the bezel as close as possible.

f. Adjust potentiometer R26 (V GAIN) so that the display test pattern is from 14.0cm (5-1/2 in) to 15.0cm (5-3/4 in) high.

NOTE

There is no vertical position adjustment and pattern may be offset up to .6cm (1/4 in). Magnetic fields from soldering irons, transformers, and other electromagnetic field producing electronics may cause a portion of the display to be off screen in the vertical direction. Reducing the vertical gain or removing the electromagnetic field producing device should fix this problem.

g. Adjust potentiometer R15 (FOCUS) for the best overall focus.

h. If the display is not level, loosen the yoke neck screw, rotate until the display is level, then retighten yoke neck screw (see figure 5-3).

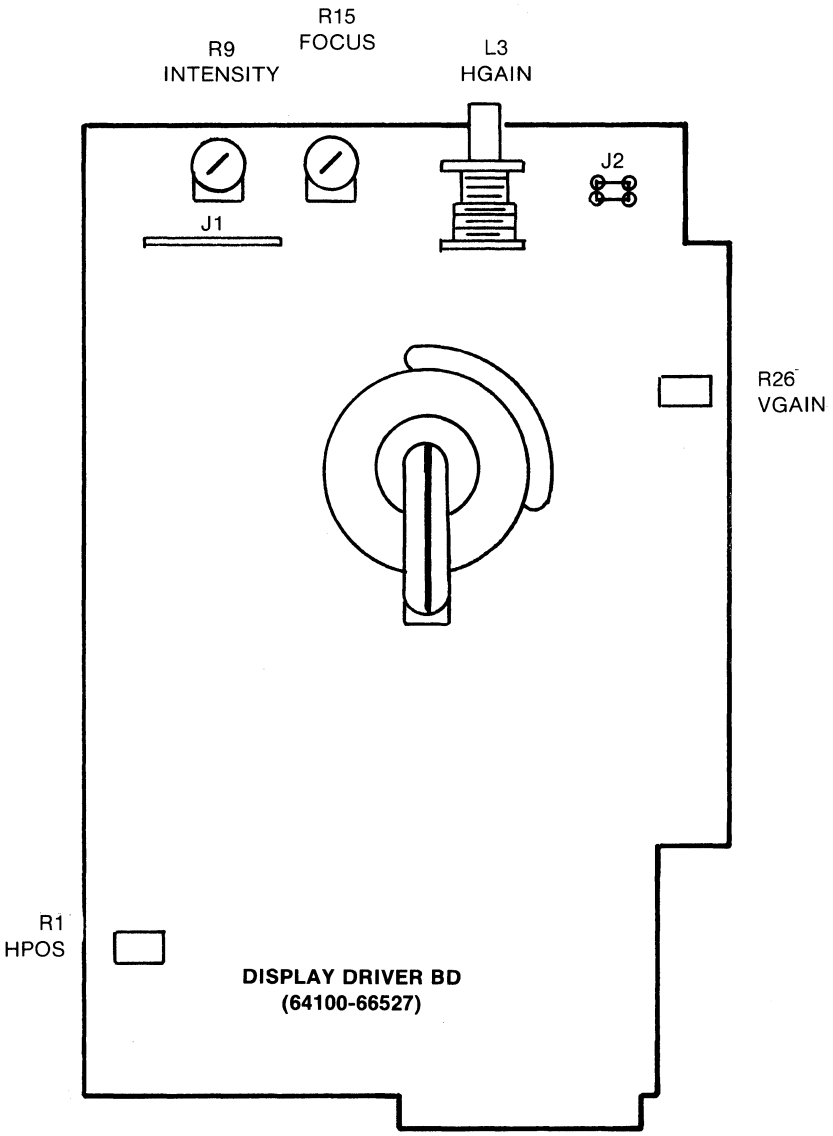


Figure 5-1. Location of Display Driver Adjustments

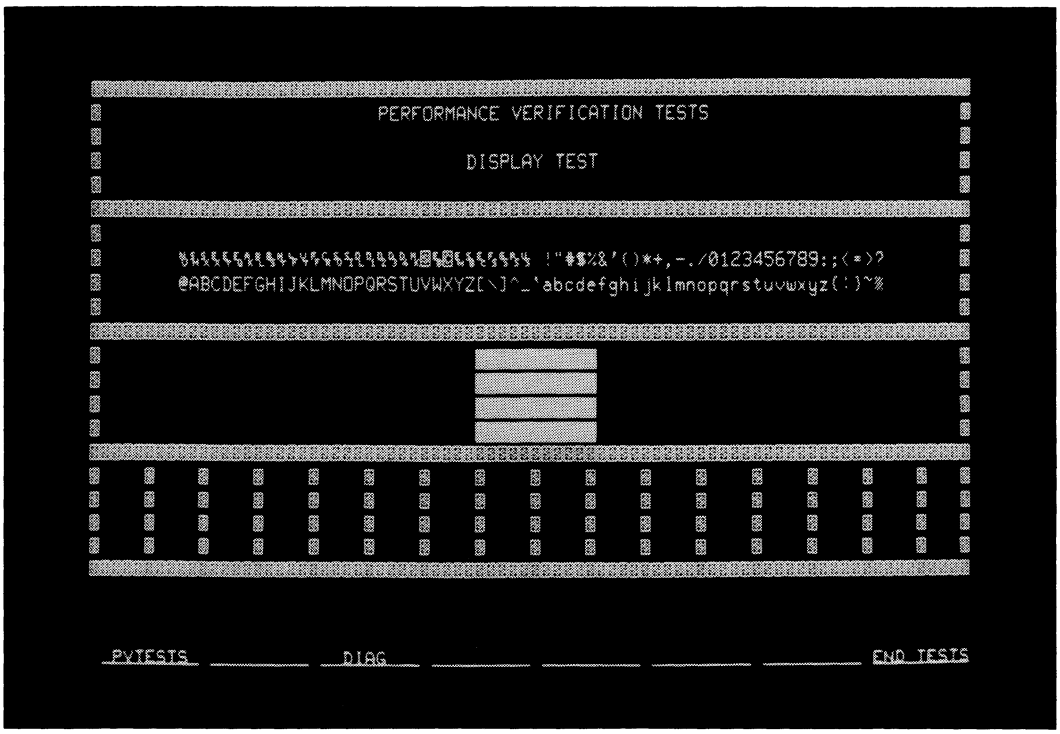


Figure 5-2. Display Test Pattern

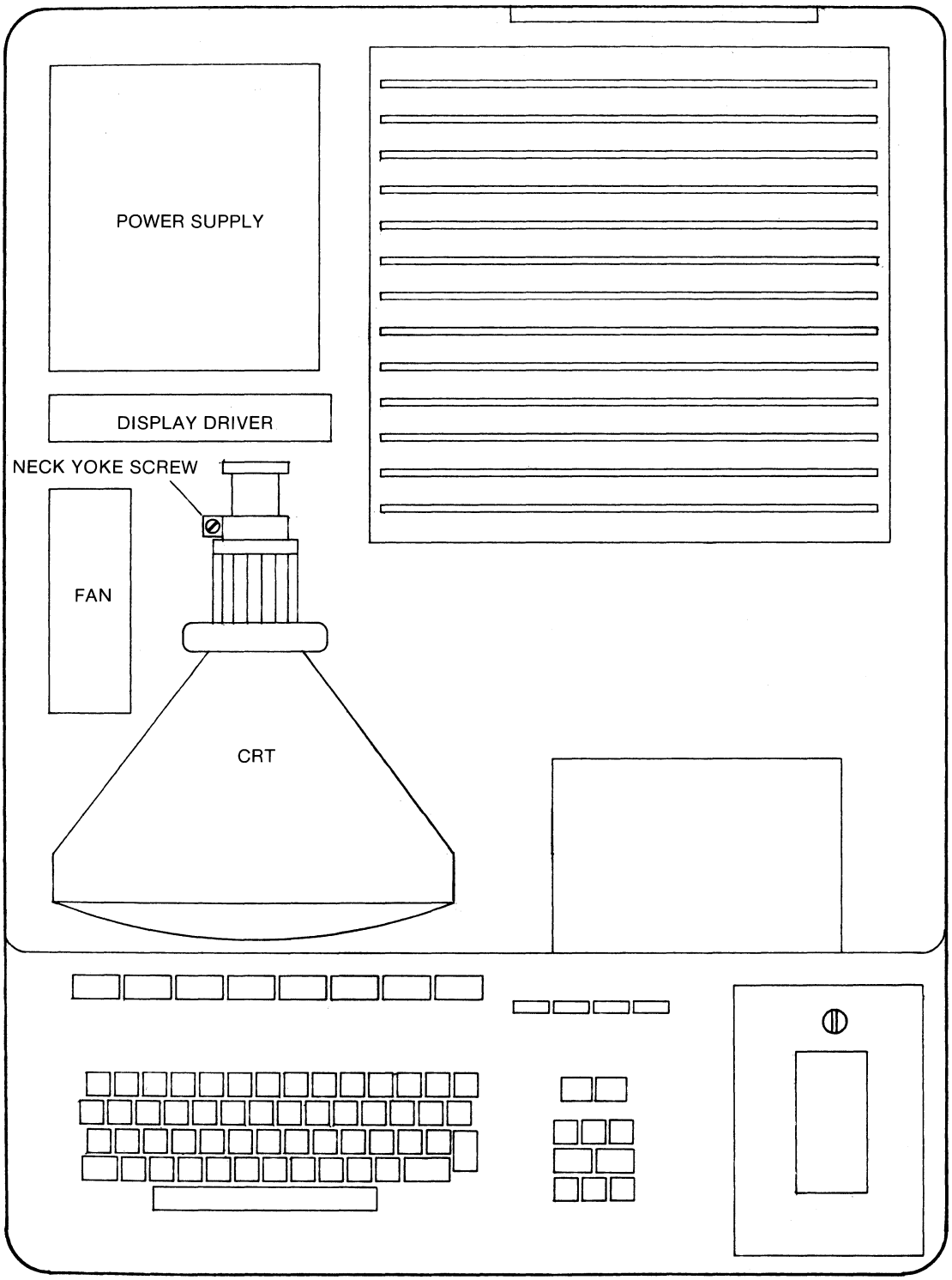


Figure 5-3. Location of Yoke Neck Screw

SECTION VI

REPLACEABLE PARTS

6-1. INTRODUCTION

6-2. This section contains information for ordering parts for your 64100A Display circuitry. Table 6-1 lists abbreviations used in the parts list and throughout this manual. Table 6-2 lists all the replaceable parts for the Display circuitry. Table 6-3 contains the names and addresses that correspond to the manufacturers' code numbers.

6-3. REPLACEABLE PARTS LIST

6-4. The organization of the parts list in table 6-2 is by electrical assemblies and their components in alphanumerical order by reference designation. The information given for each part consists of the following:

1. The reference designation as used on component locators and schematics.

2. The Hewlett-Packard part number.

3. The check digit (CD), for HP internal use only.

4. The quantity. The total quantity for each part is given only once, at the first appearance of the part number for each assembly.

5. The part description.

6. The manufacturer's code (a five digit number).

7. The manufacturer's part number.

6-5. ORDERING INFORMATION

6-6. To order a part listed in the replaceable parts table, quote the Hewlett-Packard part number and check digit, indicate the quantity required, and address the order to the nearest Hewlett-Packard office.

6-7. To order a part that is not listed in the replaceable parts table, include the instrument serial number, the description and function of the part, and the number of parts required. Address the order to the nearest Hewlett-Packard office.

6-8. DIRECT MAIL ORDER SYSTEM

6-9. Within the USA, Hewlett-Packard can supply parts through a direct mail order system. The advantages of using the system are as follows:

1. Direct ordering and shipment from the HP parts center in Mountain View, California.
2. No maximum or minimum on any mail order (there is a minimum order amount for parts ordered through a local HP when the order requires billing and invoicing).
3. Prepaid transportation (there is a small handling charge for each order).
4. No invoicing (to provide these advantages, a check or money order must accompany each order).

6-10. Mail order forms and specific ordering information are available through your local Hewlett-Packard office.

Table 6-1. Reference Designator Abbreviations

REFERENCE DESIGNATORS

A	= assembly	**F**	= fuse	**MP**	= mechanical part	**U**	= integrated circuit
B	= motor	**FL**	= filter	**P**	= plug	**V**	= vacuum, tube, neon bulb, photocell, etc
BT	= battery	**IC**	= integrated circuit	**Q**	= transistor		
C	= capacitor	**J**	= jack	**R**	= resistor	**VR**	= voltage regulator
CP	= coupler	**K**	= relay	**RT**	= thermistor	**W**	= cable
CR	= diode	**L**	= inductor	**S**	= switch	**X**	= socket
DL	= delay line	**LS**	= loud speaker	**T**	= transformer	**Y**	= crystal
DS	= device signaling (lamp)	**M**	= meter	**TB**	= terminal board	**Z**	= tuned cavity network
E	= misc electronic part	**MK**	= microphone	**TP**	= test point		

ABBREVIATIONS

A	= amperes	**H**	= henries	**N/O**	= normally open	**RMO**	= rack mount only
AFC	= automatic frequency control	**HDW**	= hardware	**NOM**	= nominal	**RMS**	= root-mean square
AMPL	= amplifier	**HEX**	= hexagonal	**NPO**	= negative positive zero (zero temperature coefficient)	**RWV**	= reverse working voltage
		HG	= mercury				
BFO	= beat frequency oscillator	**HR**	= hour(s)				
BE CU	= beryllium copper	**HZ**	= hertz	**NPN**	= negative-positive-negative	**S-B**	= slow-blow
BH	= binder head					**SCR**	= screw
BP	= bandpass			**NRFR**	= not recommended for field replacement	**SE**	= selenium
BRS	= brass	**IF**	= intermediate freq			**SECT**	= section(s)
BWO	= backward wave oscillator	**IMPG**	= impregnated	**NSR**	= not separately replaceable	**SEMICON**	= semiconductor
		INCD	= incandescent			**SI**	= silicon
CCW	= counter-clockwise	**INCL**	= include(s)			**SIL**	= silver
CER	= ceramic	**INS**	= insulation(ed)	**OBD**	= order by description	**SL**	= slide
CMO	= cabinet mount only	**INT**	= internal	**OH**	= oval head	**SPG**	= spring
COEF	= coeficient			**OX**	= oxide	**SPL**	= special
COM	= common	**K**	= kilo=1000			**SST**	= stainless steel
COMP	= composition					**SR**	= split ring
COMPL	= complete	**LH**	= left hand	**P**	= peak	**STL**	= steel
CONN	= connector	**LIN**	= linear taper	**PC**	= printed circuit		
CP	= cadmium plate	**LK WASH**	= lock washer	**PF**	= picofarads= 10^{-12} farads	**TA**	= tantalum
CRT	= cathode-ray tube	**LOG**	= logarithmic taper			**TD**	= time delay
CW	= clockwise	**LPF**	= low pass filter	**PH BRZ**	= phosphor bronze	**TGL**	= toggle
				PHL	= phillips	**THD**	= thread
DEPC	= deposited carbon	**M**	= milli=10^{-3}	**PIV**	= peak inverse voltage	**TI**	= titanium
DR	= drive	**MEG**	= meg=10^{6}	**PNP**	= positive-negative-positive	**TOL**	= tolerance
		MET FLM	= metal film			**TRIM**	= trimmer
ELECT	= electrolytic	**MET OX**	= metallic oxide	**P/O**	= part of	**TWT**	= traveling wave tube
ENCAP	= encapsulated	**MFR**	= manufacturer	**POLY**	= polystyrene		
EXT	= external	**MHZ**	= mega hertz	**PORC**	= porcelain	**U**	= micro=10^{-6}
		MINAT	= miniature	**POS**	= position(s)		
F	= farads	**MOM**	= momentary	**POT**	= potentiometer	**VAR**	= variable
FH	= flat head	**MOS**	= metal oxide substrate	**PP**	= peak-to-peak	**VDCW**	= dc working volts
FIL H	= fillister head	**MTG**	= mounting	**PT**	= point		
FXD	= fixed	**MY**	= "mylar"	**PWV**	= peak working voltage	**W/**	= with
						W	= watts
G	= giga (10^{9})	**N**	= nano (10^{-9})	**RECT**	= rectifier	**WIV**	= working inverse voltage
GE	= germanium	**N/C**	= normally closed	**RF**	= radio frequency		
GL	= glass	**NE**	= neon	**RH**	= round head or right hand	**WW**	= wirewound
GRD	= ground(ed)	**NI PL**	= nickel plate			**W/O**	= without

Table 6-2. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A5	64100-66530	6	1	DISPLAY CONTROLLER BOARD ASSEMBLY	28480	64100-66530
C1	0160-5321	8	28	CAPACITOR-FXD .01uf +80-20% 100VDC CER	28480	0160-5321
C2	0160-5321	8		CAPACITOR-FXD .01uf +80-20% 100VDC CER	28480	0160-5321
C3	0160-4822	2	1	CAPACITOR-FXD 100pf +-5% 100VDC CER	28480	0160-4822
C4	0160-5321	8		CAPACITOR-FXD .01uf +80-20% 100VDC CER	28480	0160-5321
C5	0160-5321	8		CAPACITOR-FXD .01uf +80-20% 100VDC CER	28480	0160-5321
C6	0160-5321	8		CAPACITOR-FXD .01uf +80-20% 100VDC CER	28480	0160-5321
C7	0160-5321	8		CAPACITOR-FXD .01uf +80-20% 100VDC CER	28480	0160-5321
C8	0160-5321	8		CAPACITOR-FXD .01uf +80-20% 100VDC CER	28480	0160-5321
C9	0160-5321	8		CAPACITOR-FXD .01uf +80-20% 100VDC CER	28480	0160-5321
C10	0160-5321	8		CAPACITOR-FXD .01uf +80-20% 100VDC CER	28480	0160-5321
C11	0160-5321	8		CAPACITOR-FXD .01uf +80-20% 100VDC CER	28480	0160-5321
C12	0160-5321	8		CAPACITOR-FXD .01uf +80-20% 100VDC CER	28480	0160-5321
C13	0160-5321	8		CAPACITOR-FXD .01uf +80-20% 100VDC CER	28480	0160-5321
C14	0160-5321	8		CAPACITOR-FXD .01uf +80-20% 100VDC CER	28480	0160-5321
C15	0160-5321	8		CAPACITOR-FXD .01uf +80-20% 100VDC CER	28480	0160-5321
C16	0160-5321	8		CAPACITOR-FXD .01uf +80-20% 100VDC CER	28480	0160-5321
C17	0160-5321	8		CAPACITOR-FXD .01uf +80-20% 100VDC CER	28480	0160-5321
C18	0160-5321	8		CAPACITOR-FXD .01uf +80-20% 100VDC CER	28480	0160-5321
C19	0160-5321	8		CAPACITOR-FXD .01uf +80-20% 100VDC CER	28480	0160-5321
C20	0160-5321	8		CAPACITOR-FXD .01uf +80-20% 100VDC CER	28480	0160-5321
C21	0160-5321	8		CAPACITOR-FXD .01uf +80-20% 100VDC CER	28480	0160-5321
C22	0160-5321	8		CAPACITOR-FXD .01uf +80-20% 100VDC CER	28480	0160-5321
C23	0160-5321	8		CAPACITOR-FXD .01uf +80-20% 100VDC CER	28480	0160-5321
C24	0160-5321	8		CAPACITOR-FXD .01uf +80-20% 100VDC CER	28480	0160-5321
C25	0180-0374	3	1	CAPACITOR-FXD 10uf +-10% 20VDC TA	28480	0180-0374
C26	0160-5321	8		CAPACITOR-FXD .01uf +80-20% 100VDC CER	28480	0160-5321
C27	0160-5321	8		CAPACITOR-FXD .01uf +80-20% 100VDC CER	28480	0160-5321
C28	0160-5321	8		CAPACITOR-FXD .01uf +80-20% 100VDC CER	28480	0160-5321
C29	0160-5321	8		CAPACITOR-FXD .01uf +80-20% 100VDC CER	28480	0160-5321
C30	0160-5321	8		CAPACITOR-FXD .01uf +80-20% 100VDC CER	28480	0160-5321
CR1	1901-0535	9	4	DIODE-SM SIG SCHOTTKY	28480	1901-0535
CR2	1901-0535	9		DIODE-SM SIG SCHOTTKY	28480	1901-0535
CR3	1901-0535	9		DIODE-SM SIG SCHOTTKY	28480	1901-0535
CR4	1901-0535	9		DIODE-SM SIG SCHOTTKY	28480	1901-0535
L1	9170-0029	3	2	CORE-SHIELDING BEAD	28480	9170-0029
MP1	5040-6067	2	2	PC-EXTRACTOR	28480	5040-6067
MP2	5040-6067	2		PC-EXTRACTOR	28480	5040-6067
P2	1258-0182	7	2	TEST JUMPER	28480	1258-0182
P3	1258-0182	7		TEST JUMPER	28480	1258-0182
P4	1810-0307	0	1	NETWORK-CNDCT MODULE DIP;16 PINS; .1	28480	1810-0307
R1	0757-0280	3	12	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R2	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R3	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R4	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R5	0698-3438	3	1	RESISTOR 147 1% .125W F TC=0+-100	28480	0698-3438
R6	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R7	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R8	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R9	0698-3444	3		RESISTOR 316 1% .125W F TC=0+-100	24546	C4-1/8-T0-316-F
R10	0683-1015	7	1	RESISTOR 100 1% .125W F TC=0+-100	28480	0683-1015
R11	0757-0280	3		RESISTOR 1K 1% .125W F TC=-0+-100	28480	0698-7028
R12	0698-7028	5	7	RESISTOR 27 10% .125W CC TC=-270/+540	28480	0698-7028
R13	0698-7028	5		RESISTOR 27 10% .125W CC TC=-270/+540	28480	0698-7028
R14	0698-7028	5		RESISTOR 27 10% .125W CC TC=-270/+540	28480	0698-7028
R15	0698-7028	5		RESISTOR 27 10% .125W CC TC=-270/+540	28480	0698-7028
R16	0698-7028	5		RESISTOR 27 10% .125W CC TC=-270/+540	28480	0698-7028
R17	0698-7028	5		RESISTOR 27 10% .125W CC TC=-270/+540	28480	0698-7028
R18	0698-7028	5		RESISTOR 27 10% .125W CC TC=-270/+540	28480	0698-7028
R19	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R20	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R21	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R22	0684-1211	7	1	RESISTOR 120 10% .25W FC TC=-400/+600	01121	CB1211
R23	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R24	0698-3633	0	1	RESISTOR 390 5% 2W MO TC=0+-200	28480	0698-3633
TP1-13	0360-0535	0	20	TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
TPGND	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
U1	1820-0681	4	3	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U2	1820-1453	0	2	IC CNTR TTL S BIN SYNCHRO POS-EDGE-TRIG	01295	SN74S163N
U3	1820-1917	1	2	IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U4	1820-1917	1		IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U5	1820-1201	6	1	IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
U6	1820-1453	0		IC CNTR TTL S BIN SYNCHRO POS-EDGE-TRIG	01295	SN74S163N
U7	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U8	1820-1112	8	3	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74N

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (continued)

Reference Designation	HP Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
U9	1820-1322	2	2	IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U10	1820-0629	0	2	IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
U11	1820-1449	4	1	IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U12	1820-0693	8	3	IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
U13	1820-1144	6	3	IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
U14	1820-0683	6	2	IC INV TTL S HEX 1-INP	01295	SN74S04N
U15	1820-1208	3	4	IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
U16	1820-0688	1	2	IC GATE TTL S NAND DUAL 4-INP	01295	SN74S20N
U17	1820-1211	8	1	IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS86N
U18	1820-0629	0		IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
U19	1820-1197	9	1	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U20	1820-0688	1		IC GATE TTL S NAND DUAL 4-INP	01295	SN74S20N
U21	1820-0683	6		IC INV TTL S-HEX 1-INP	01295	SN74S04N
U22	1820-1322	2		IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U23	1818-3005	7	16	IC NMOS 64K DYNAMIC RAM 150-NS	28480	1818-3005
U24	1818-3005	7		IC NMOS 64K DYNAMIC RAM 150-NS	28480	1818-3005
U25	1818-3005	7		IC NMOS 64K DYNAMIC RAM 150-NS	28480	1818-3005
U26	1818-3005	7		IC NMOS 64K DYNAMIC RAM 150-NS	28480	1818-3005
U27	1818-3005	7		IC NMOS 64K DYNAMIC RAM 150-NS	28480	1818-3005
U28	1818-3005	7		IC NMOS 64K DYNAMIC RAM 150-NS	28480	1818-3005
U29	1818-3005	7		IC NMOS 64K DYNAMIC RAM 150-NS	28480	1818-3005
U30	1818-3005	7		IC NMOS 64K DYNAMIC RAM 150-NS	28480	1818-3005
U31	1820-2024	3	3	IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U32	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U33	1820-2191	5	1	IC MICROPROC-ACCESS NMOS 8-BIT	34649	C8275
U34	1810-0536	7	1	NETWORK-RES 27 OHM 16 PIN DIP	28480	1810-0536
U35	1820-1144	6		IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
U36	1820-1208	3		IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
U37	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U38	1818-3005	7		IC NMOS 64K DYNAMIC RAM 150-NS	28480	1818-3005
U39	1818-3005	7		IC NMOS 64K DYNAMIC RAM 150-NS	28480	1818-3005
U40	1818-3005	7		IC NMOS 64K DYNAMIC RAM 150-NS	28480	1818-3005
U41	1818-3005	7		IC NMOS 64K DYNAMIC RAM 150-NS	28480	1818-3005
U42	1818-3005	7		IC NMOS 64K DYNAMIC RAM 150-NS	28480	1818-3005
U43	1818-3005	7		IC NMOS 64K DYNAMIC RAM 150-NS	28480	1818-3005
U44	1818-3005	7		IC NMOS 64K DYNAMIC RAM 150-NS	28480	1818-3005
U45	1818-3005	7		IC NMOS 64K DYNAMIC RAM 150-NS	28480	1818-3005
U46	1820-1997	7	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL_IN	01295	SN74LS374N
U47	1820-1208	3		IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
U48	1820-0693	8		IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
U49	1820-1015	0	2	IC MUXR/DATA-SEL S 2-TO-1 LINE DRVR	01295	SN74S158N
U50	1820-1015	0		IC MUXR/DATA-SEL S 2-TO-1 LINE DRVR	01295	SN74S158N
U51	1820-1210	7	1	IC GATE TTL LS AND-OR INV DUAL 2-INP	28480	1820-1210
U52	1820-1144	6	3	IC GATE TTL S NOR QUAD 2-INP	01295	SN74LS02N
U53	1820-1112	3		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74N
U54	1820-1191	3	2	IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S175N
U55	1820-0697	2	1	IC DRVR TTL S NAND LINE DUAL 4-INP	01295	SN74S140N
U56	1820-1435	8	3	IC CNTR TTL LS BIN UP/DOWN SYNCHRO	01295	SN74LS669N
U57	1820-1435	8		IC CNTR TTL LS BIN UP/DOWN SYNCHRO	01295	SN74LS669N
U58	1820-1435	8		IC CNTR TTL LS BIN UP/DOWN SYNCHRO	01295	SN74LS669N
U59	0960-0530	7	1	OSCILLATOR 25MHZ	28480	0960-0530
U60	1816-1496	3	1	IC ROM 2K x 8	28480	1816-1496
U61	1820-1432	5	2	IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS163N
U62	1820-1432	5		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS163N
U63	1820-1112	3		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74N
U64	1820-1130	0	1	IC GATE TTL S NAND 13-INP	01295	SN74S133N
U65	1820-1428	9	4	IC MUXR/DATA-SEL TTL LS 2-TO-1 LINE QUAD	01295	SN74LS158N
U66	1820-1428	9		IC MUXR/DATA-SEL TTL LS 2-TO-1 LINE QUAD	01295	SN74LS158N
U67	1820-1428	9		IC MUXR/DATA-SEL TTL LS 2-TO-1 LINE QUAD	01295	SN74LS158N
U68	1820-1428	9		IC MUXR/DATA-SEL TTL LS 2-TO-1 LINE QUAD	01295	SN74LS158N
U69	1820-1208	3		IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
U70	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U71	1820-2075	4	1	IC MISC TTL LS	01295	SN74LS245N
U72	1820-1451	8	1	IC GATE TTL L NAND QUAD 2-INP	01295	SN74S38N
U73	1820-1492	7	1	IC BFR TTL LS INV HEX 1-INP	28480	1820-1492
U74	1820-1191	3		IC FF TTL S D-TYPE POS-EDGE-TRIG COM	01295	SN74S175N
U75	1820-0685	8	1	IC GATE TTL S NAND TPL 3-INP	01295	SN74S10N
U76	1820-1303	9	2	IC SHF-RGTR TTL S R-S PRL_IN PRL_OUT	01295	SN74S195N
U77	1820-1303	9		IC SHF-RGTR TTL S R-S PRL_IN PRL_OUT	01295	SN74S195N
U78	1820-0693	8		IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
XU1	1200-0607	0	3	SOCKET-IC 16 CONT DIP-SLDR	28480	1200-0607
XU2	1200-0607	0		SOCKET-IC 16 CONT DIP-SLDR	28480	1200-0607
XU33	1200-0654	7	1	SOCKET-IC 40 CONT DIP-SLDR	28480	1200-0654
XU34	1200-0607	0		SOCKET-IC 16 CONT DIP-SLDR	28480	1200-0607

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A7	64100-66531	9	1	DISPLAY DRIVER BOARD ASSEMBLY	28480	64100-66531
C1	0140-0149	6	2	CAPACITOR-FXD 470PF +-5% 300VDC MICA	72136	DM15F4NJ0300WV1CR
C2	0180-0229	7	3	CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X901082
C3	0140-0149	6	1	CAPACITOR-FXD 470PF +-5% 300VDC MICA	72136	DM15F471J0300WV1CR
C4	0180-2913	0	1	CAPACITOR-FXD 470UF+50-10% 50VDC AL	28480	0180-2913
C5	0180-2881	1	2	CAPACITOR-FXD 10UF+50-10% 50VDC AL	28480	0180-2881
C7	0180-2880	0	2	CAPACITOR-FXD 2200UF+50-10% 16VDC AL	28480	0180-2880
C8	0160-4740	3	1	CAPACITOR-FXD .015F +-5% 400VDC POLYP	28480	0160-4740
C9	0160-4706	1	1	CAPACITOR-FXD 1.75UF +-5% 200VDC	28480	0160-4706
C10	0160-2902	5	1	CAPACITOR-FXD .01UF +-20% 1KVDC CER	28480	0160-2902
C11	0180-2881	1		CAPACITOR-FXD 10UF+50-10% 50VDC AL	28480	0180-2881
C12	0160-4230	6	3	CAPACITOR-FXD .01UF +80-20% 1KVDC CER	71590	GAP-103
C13	0160-4230	6		CAPACITOR-FXD .01UF +80-20% 1KVDC CER	71590	GAP-103
C14	0160-4230	6		CAPACITOR-FXD .01UF +80-20% 1KVDC CER	71590	GAP-103
C15	0160-2055	9	5	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C16	0160-0157	8	1	CAPACITOR-FXD 4700PF +-10% 200VDC POLYE	28480	0160-0157
C17	0160-0168	1	1	CAPACITOR-FXD .1UF +-10% 200VDC POLYE	28480	0160-0168
C18	0180-0291	3	1	CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
C19	0180-0229	7	5	CAPACITOR-FXD 33UF +-10% 10VDC TA	56289	150D336X901082
C20	0160-3508	9	1	CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
C21	0180-2879	7		CAPACITOR-FXD 22UF+50-10% 25VDC AL	28480	0180-2879
C22	0180-2879	7		CAPACITOR-FXD 22UF+50-10% 25VDC AL	28480	0180-2879
C23	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C24	01A0-2880	0		CAPACITOR-FXD 2200UF+50-10% 16VDC AL	28480	01A0-2880
C25	0180-0229	7		CAPACITOR-FXD 33UF +-10% 10VDC TA	56289	150D336X901082
C26	0180-2879	7		CAPACITOR-FXD 22UF+50-10% 25VDC AL	28480	0180-2879
C27	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C28, C29	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
CR1, CR2	1901-0050	3	12	DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
CR3	1901-0719	1	2	DIODE-PWR RECT 400V 3A 300NS	28480	1901-0719
CR4	1901-0719	1		DIODE-PWR RECT 400V 3A 300NS	28480	1901-0719
CR5	1901-0845	4	1	DIODE-HV RECT 2KV 50MA 250NS	27777	VG-2X
CR6	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
CR7	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
CR8	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
CR9	1901-0022	9	4	DIODE-STABISTOR 10V 250MA	28480	1901-0022
CR10	1901-0022	9		DIODE-STABISTOR 10V 250MA	28480	1901-0022
CR11	1901-0022	9		DIODE-STABISTOR 10V 250MA	28480	1901-0022
CR12	1901-0022	9		DIODE-STABISTOR 10V 250MA	28480	1901-0022
CR13	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
CR14 thru CR19	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
CR20, 21	1901-0919	3		DIODE-VOLTAGE SUPPRESSOR		1901-0919
DS1	2140-0013	5	2	LAMP-GLOW 5AB-A 70/57VDC 300UA T-2-BULB	0046G	5AB(NE-23)
DS2	2140-0013	5		LAMP-GLOW 5AB-A 70/57VDC 300UA T-2-BULB	0046G	5AB(NE-23)
J2	1251-5502	1	1	CONNECTOR-MALE 4-PIN	28480	1251-5502
L1	9100-2276	9	1	COIL-MLD 100UH 10% Q=50 .095DX.25LG-NOM	28480	9100-2276
L2	9140-0319	1	1	COIL-FIXED LINEARITY; DEFL CURRENT: 4 A	28480	9140-0319
L3	9140-0306	6	1	COIL-VAR 20UH-80UH PC-MTG	28480	9140-0306
L4	9140-0179	1	2	COIL-MLD 22UH 10% Q=75 .155DX.375LG-NOM	28480	9140-0179
L5	9140-0114	4	1	COIL-MLD 10UH 10% Q=55 .155DX.375LG-NOM	28480	9140-0114
L6	9140-0179	1		COIL-MLD 22UH 10% Q=75 .155DX.375LG-NOM	28480	9140-0179
MP1	1251-3475	3	1	CONNECTOR 10-PIN M POST TYPE	27264	1251-3475
MP2	1400-0249	0	1	CABLE TIE .062-.625-DIA .091-WD NYL	28480	1400-0249
Q1	1854-0090	0	2	TRANSISTOR NPN 2N4401 SI TO-92 PD=310MW	04713	2N4401
Q2	1854-0623	5	1	TRANSISTOR NPN 2N6306 SI TO-3 PD=125W	04713	2N6306
Q3	1853-0271	7	1	TRANSISTOR PNP 2N4403 SI TO-92 PD=310MW	04713	2N4403
Q4	1854-0798	7	1	TRANSISTOR NPN S TO152 MPS U45	28480	1854-1798
Q5	1853-0449	1	1	TRANSISTOR PNP SI DARL PD=1W	04713	MPS-U95
Q6	1854-0215	1	2	TRANSISTOR NPN 2N3904 SI PD=350MW FT=300MHZ	04713	2N3904
Q7	1854-0215	1		TRANSISTOR NPN 2N3904 SI PD=350MW FT=300MHZ	04713	2N3904
Q8	1854-0467	5		TRANSISTOR NPN 2N4401 SI TO-92 PD=310MW	04713	2N4401
R1	2100-3353	8	1	RESISTOR-TRMR 20K 10% C SIDE-ADJ 1-TRN	32997	3386X-Y46-203
R2	0683-2725	8	1	RESISTOR 2.7K 5% .25W FC TC=-400/+700	01121	CB2725
R3	0698-3450	9	3	RESISTOR 42.2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4222-F
R4	0683-1025	9	4	RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R5	0683-1015	7	4	RESISTOR 100 5% .25W FC TC=-400/+500	01121	CB1015

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
R6	0764-0016	8	2	RESISTOR 1K 5% 2W MO TC=0+-200	28480	0764-0016
R7	0683-1015	7		RESISTOR 100 5% .25W FC TC=-400/+500	01121	CB1015
R8	0683-6825	7	1	RESISTOR 6.8K 10% .25W FC TC=0+-100	28480	0683-6825
R9	2100-3892	0	2	RESISTOR -TRMR 2.5M 10% C TOP-ADJ 1-TRN	28480	2100-3892
R10	0683-5645	7	6	RESISTOR 560K 5% .25W FC TC=800/+900	28480	0683-5645
R11	0683-5645	7		RESISTOR 560K 5% .25W FC TC=800/+900	28480	0683-5645
R12	0683-1055	5		RESISTOR 1M 5% .25W FC TC=-800/+900	01121	CB1055
R13	0683-1055	5		RESISTOR 1M 5% .25W FC TC=-800/+900	01121	CB1055
R14	0683-4745	6		RESISTOR 470K 5% .25W FC TC=0+-100	28480	0683-4745
R15	2100-3892	0		RESISTOR-TRMR 2.5M 10% C TOP-ADJ 1-TRN	28480	2100-3892
R16	0683-1055	5		RESISTOR 1M 5% .25W FC TC=-800/+900	01121	CB1055
R17	0683-1045	3	4	RESISTOR 100K 5% .25W FC TC=-400/+800	01121	CB1045
R18	0683-1045	3		RESISTOR 100K 5% .25W FC TC=-400/+800	01121	CB1045
R19	0683-2215	1	1	RESISTOR 220 5% .25W FC TC=-400/+600	01121	CB2215
R20	0683-2225	3		RESISTOR 2.2K 5% .25W FC TC=-400/+700	01121	CB2225
R21	0683-2225	3		RESISTOR 2.2K 5% .25W FC TC=-400/+700	01121	CB2225
R22	0683-2225	3		RESISTOR 2.2K 5% .25W FC TC=-400/+700	01121	CB2225
R23	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R24	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R25	0686-2215	7	1	RESISTOR 220 5% .5W CC TC=0+529	01121	EB2215
R26	2100-3356	1	1	RESISTOR-TRMR 200K 10% C SIDE-ADJ 1-TRN	28480	2100-3356
R27	0683-1045	3		RESISTOR 100K 5% .25W FC TC=-400/+800	01121	CB1045
R28	0683-1045	3		RESISTOR 100K 5% .25W FC TC=-400/+800	01121	CB1045
R29	0683-1035	1	1	RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R30	0757-0463	4	2	RESISTOR 82.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-8252-F
R31	0757-0470	3	1	RESISTOR 162K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1623-F
R32	0757-0463	4		RESISTOR 82.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-8252-F
R33	0757-0280	3	2	RESISTOR 1K 1% .125W FTC=0+-100	24546	C4-1/8-TO-1001-F
R34	0683-1015	7		RESISTOR 100 5% .25W FC TC=-400/+500	01121	CB1015
R35	0683-2235	5	1	RESISTOR 22K 5% .25W FC TC=-400/+800	01121	CB2235
R36	0698-3450	9		RESISTOR 42.2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4222-F
R37	0698-3450	9		RESISTOR 42.2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4222-F
R38	0683-3315	4	1	RESISTOR 330 5% .25W FC TC=-400/+600	01121	CB3315
R39	0686-0335	8	1	RESISTOR 3.3 5% .5W CC TC=0+412	01121	EB3305
R40	0684-1211	7	2	RESISTOR 120 10% .25W FC TC=-400/+600	01121	CB1211
R41	0684-1211	7		RESISTOR 120 10% .25W FC TC=-400/+600	01121	CB1211
R42	0683-6815	5	2	RESISTOR 680 5% .25 W FC TC=400/+600	28480	0683-6815
R43	0683-6815	5		RESISTOR 680 5% .25 W FC TC=400/+600	28480	0683-6815
R44 thru R46	0683-8215	3	3	RESISTOR 820 5% .25W FC TC=-400/+600		
R47	0764-0016	8		RESISTOR 1K 5% 2W MO TC=0+-200	28480	0764-0016
R48	0683-1015	7		RESISTOR 100 5% .25W FC TC=-400/+500	01121	CB1015
R49	0757-0124	4		RESISTOR 39.2K 1% .12W F TC=0+-100	28480	0757-0124
R50	0683-1025	0		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
T1	9100-4195	6	1	TRANSFORMER-HORIZONTAL DRIVE	28480	9100-4195
T2	9100-0491		1	TRANSFORMER FLYBACK, HI V 12.5 KV ±500V	28480	9100-0491
TP1-TP7	0360-0535	0	7	TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
U1	1820-1437	0	1	IC MV TTL LS MONOSTBL DUAL	01295	SN74L8221N
U2	1826-0120	8	1	IC OP AMP GP QUAD 14-DIP-P	27014	LM3900N
U3	1820-1451	8	1	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S38N
U4	1820-0471	0	1	IC INV TTL HEX 1-INP	01295	SN7406N
VR1	1902-0025	5	1	DIODE-ZNR 10V 5% DO-7 PD=.4W	28480	1902-0025
VR2	1902-0041	4	1	DIODE-ZNR 5.11V 5% DO-7 PD=.4W TC=-.009%	28480	1902-0041
VR3	1902-0644	3	1	DIODE-ZNR 1N5363B 30V 5% PD=5W TC=+29MV	28480	1902-0644
VR4	1902-0049	2	1	DIODE-ZNR 6.19V 5% DO 35 PD=.4W	28480	1902-0049
VR5	1902-3036	3	1	DIODE-ZNR 3.16V 2% DO-7 PD=4W TC=-0.64%	28480	1902-3036

See introduction to this section for ordering information

Table 6-3. Manufacturers' Codes

Mfr No.	Manufacturer Name	Address		Zip Code
00000	ANY SATISFACTORY SUPPLIER			
0046G	NORELCO NORTH AMER PHILIPS LTG CORP	LOS ANGELES	CA	90021
01121	ALLEN-BRADLEY CO	MILWAUKEE	WI	53204
01295	TEXAS INSTR INC SEMICOND CMPNT DIV	DALLAS	TX	75222
04713	MOTOROLA SEMICONDUCTOR PRODUCTS	PHOENIX	AZ	85062
09023	CORNELL-DUBILIER ELEK DIV FED PAC	SANFORD	NC	27330
24546	CORNING GLASS WORKS (BRADFORD)	BRADFORD	PA	16701
27014	NATIONAL SEMICONDUCTOR CORP	SANTA CLARA	CA	95051
27264	MOLEX PRODUCTS CO	DOWNERS GROVE	IL	60515
27777	VARO SEMICONDUCTOR INC	GARLAND	TX	75040
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO	CA	94304
32997	BOURNS INC TRIMPOT PROD DIV	RIVERSIDE	CA	92507
50088	MOSTEK CORP	CARROLLTON	TX	75006
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS	MA	01247
71590	CENTRALAB ELEK DIV GLOBE-UNION INC	MILWAUKEE	WI	50501
72136	ELECTRO MOTIVE CORP SUB IEC	WILLIMANTIC	CT	06226

See introduction to this section for ordering information

SECTION VII

MANUAL BACKDATING

7-1. INTRODUCTION.

7-2. This section contains information for adapting this manual to instruments with various serial prefix numbers.

7-3. MANUAL CHANGES.

7-4. To adapt this manual to your instrument, refer to table 7-1 and make all of the manual changes listed under the serial prefix number for your instrument. Perform these changes in the sequence listed.

Table 7-1. Manual Changes

Serial Prefix	Make Changes	Affects
2210A	1, 2	DSP
2212A	1, 2	DSP

NOTE: DSP is the abbreviation for Display Controller and Driver boards.

CHANGE 1

NOTE

The 64100-66523 Display Driver board is compatible with the 64100-66527 board with the following changes:

Table 6-2 DSP, Replaceable Parts List,
- A7: Change HP Part No. to 64100-66523, CD=1.
- CR2: Change HP Part No. to 1901-0719, CD=1.
- T1: Change HP Part No. 9100-4075, CD=0.
- CR19: Delete.
- CR29: Delete.
- R50: Delete.
- VR5: Delete.

Page 8-22 DSP,
Figure 8-6, Display Driver Component Locator. Replace with component locator on page 7-4 DSP.

Page 8-23 DSP,
Figure 8-7, Display Driver Schematic. Replace with Display Driver schematic on page 7-5 DSP.

CHANGE 2

NOTE

The 64100-66519 Display Controller board is compatable with the 64100-66530 board. The newer 64100-66530 board has 64K x 16 memory locations of RAM while the 64100-66519 board has only 32K x 16 memory locations of RAM. The 64100-66519 Display Controller board experiences LMSYN PROBLEMS when several option cards (using LMYSYN) are loaded into the card cage. To correct this problem refer to SERVICE NOTE 64100A-12. Contact the nearest Sales/Service Office for additional information.

Section IV
Pages 4-1 thru 4-29 DSP, Section IV, Performance Verification and SA Tables,
Change: Replace Section IV with Section IV pages 7-7 thru 7-23 DSP.

Section VI
Page 6-5 DSP, Replaceable Parts List,
Change: Replace Display Controller Material list with material list on pages 7-25 DSP and 7-26 DSP.

Section VIII
Pages 8-13 DSP thru 8-19 DSP, Display Controller Schematics 4A - 4D,
Change: Replace Schematics 4A - 4D with Display Controller Schematics on pages 7-27 DSP thru 7-34 DSP.

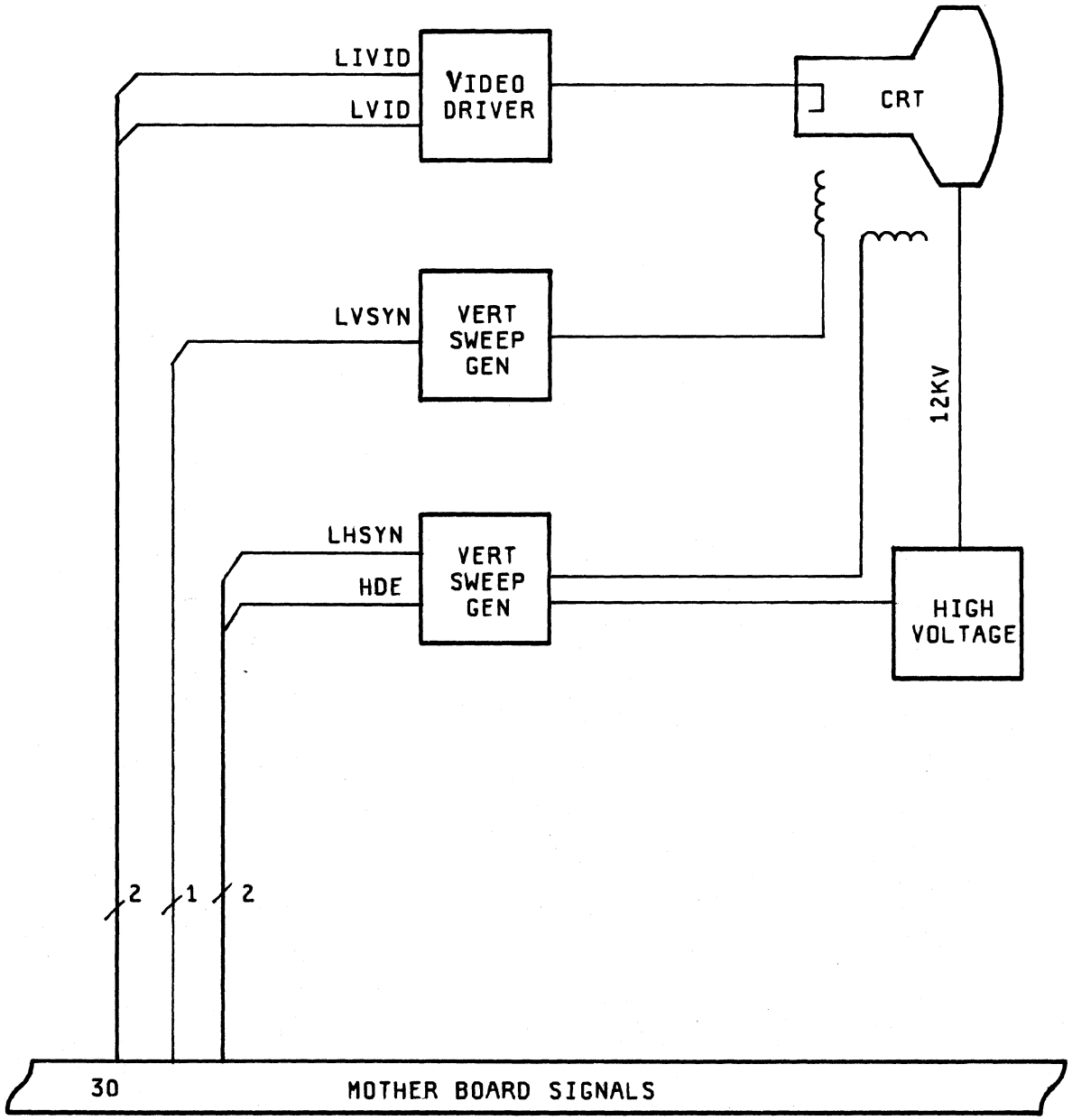


Figure 7-1. Display Driver Block Diagram

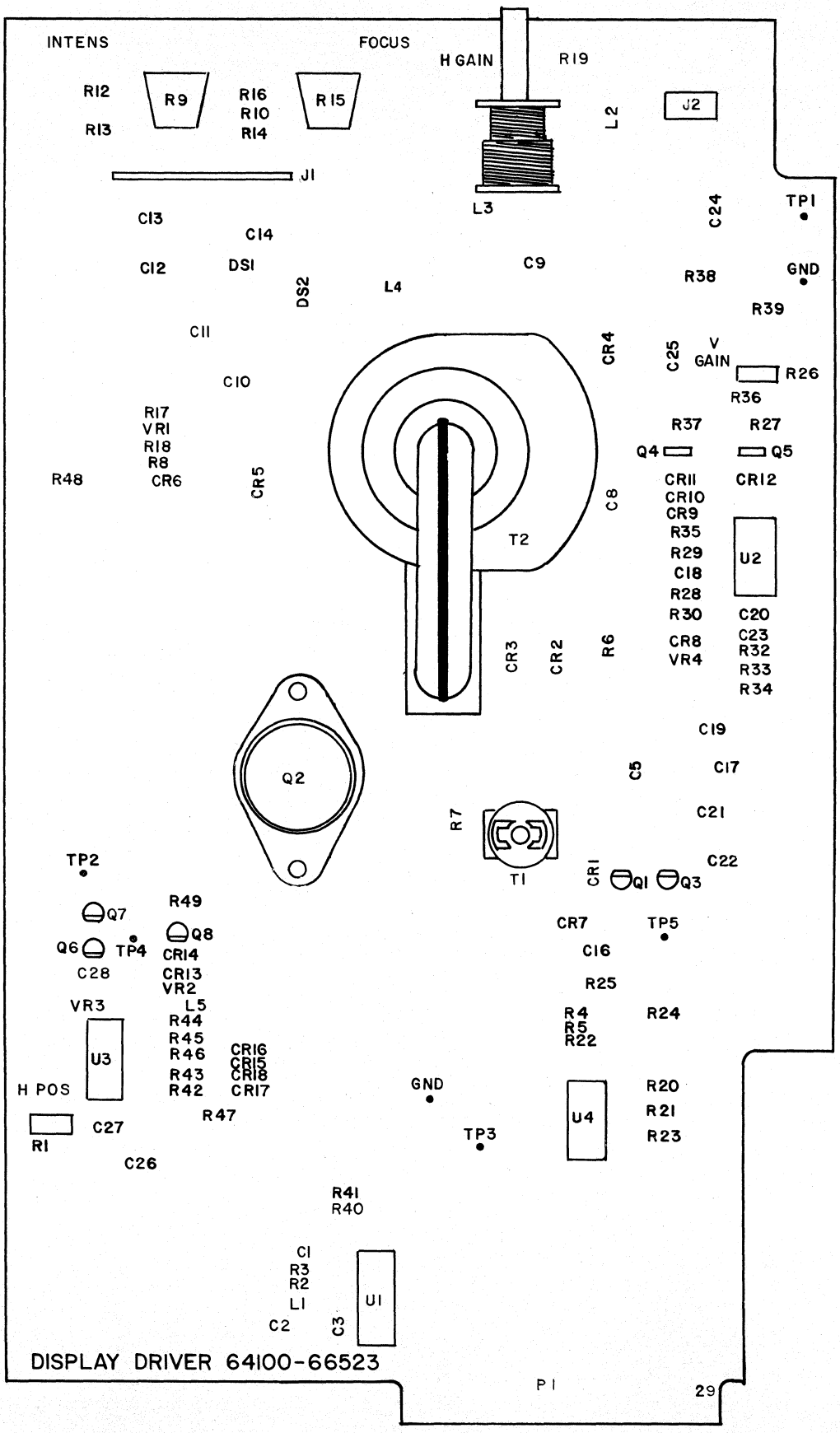


Figure 7-2. Display Driver Component Locator

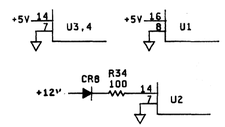
ICS ON THIS SCHEMATIC

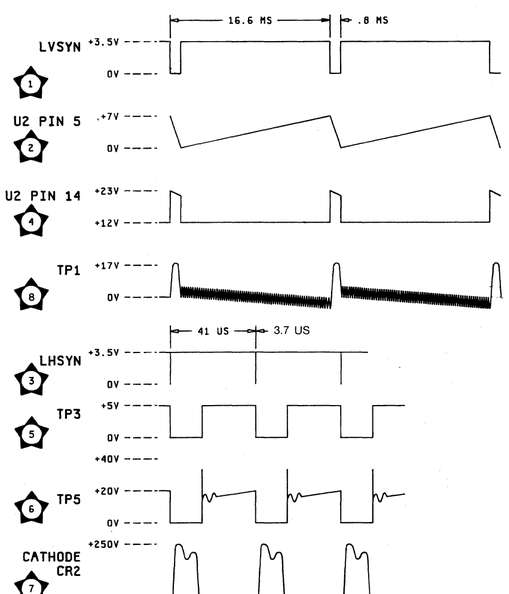
REF. DES.	HP PART NO.	MFG. PART NO.
U1	1820-1437	74LS221
U2	1826-0120	LM3900
U3	1820-1451	74S38
U4	1820-0471	7406

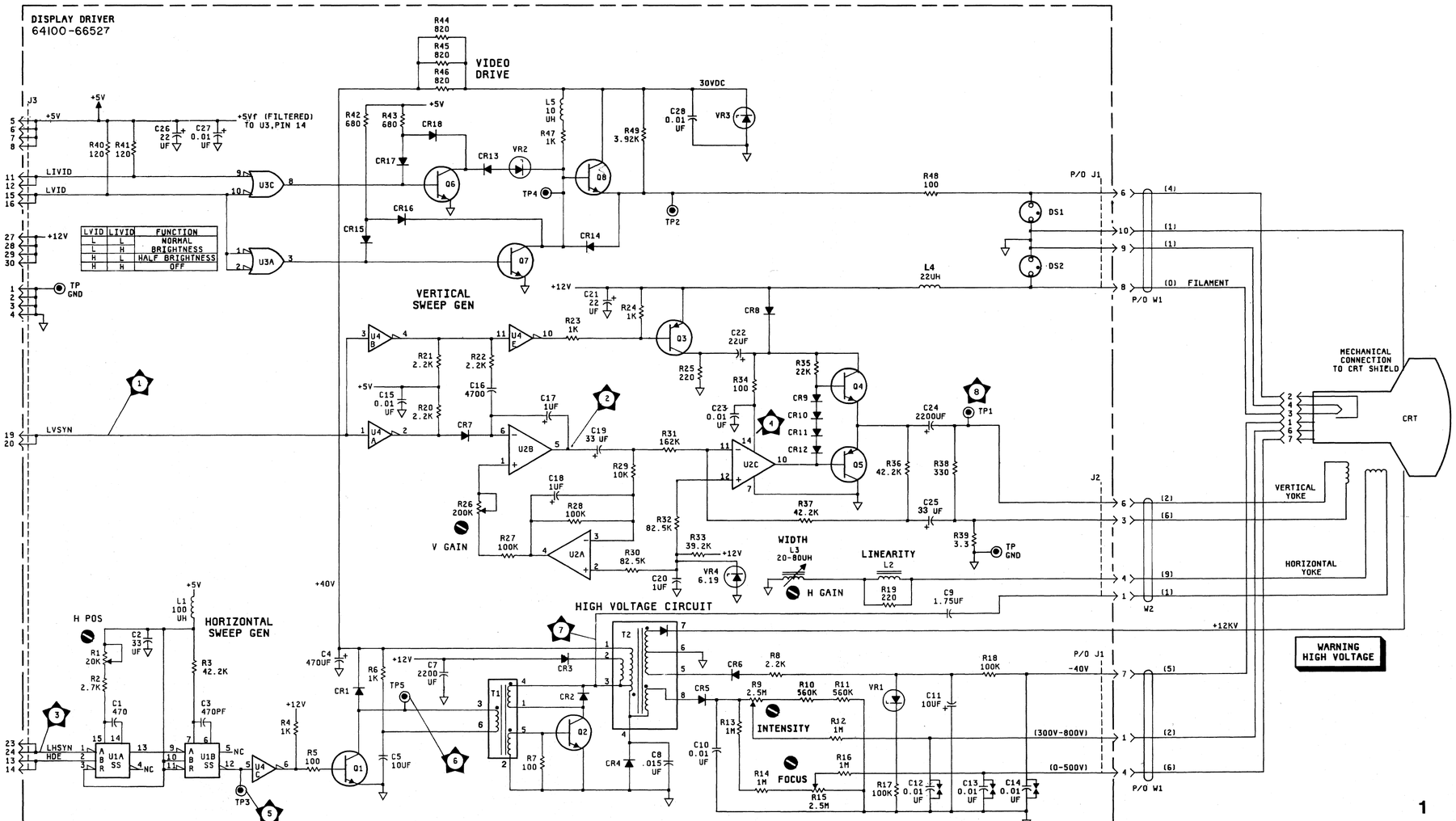
PARTS INCLUDED ON THIS SCHEMATIC

REF. DES.	HP PART NO.
CRT	2090-0042
W1(CRT CABLE)	64100-61603

IC POWER SUPPLY CONFIGURATIONS







1

Figure 7-2.
Display Driver Schematic
MANUAL BACKDATING DSP 7-5/(7-6 blank)

SECTION IV

PERFORMANCE TESTS

4-1. INTRODUCTION.

4-2. If the mainframe has failed in a display or RAM test, proceed to use this section. This section on Performance Verification applies directly to the 64100-66519 Display Controller board. If there is some doubt as to the failure mode, return to section IV of the Mainframe chapter.

4-3. RAM TESTS.

4-4. POWER UP RAM TEST.

Purpose:

The RAM test verifies the ability to read and write from all RAM located on the Display Control board. Note that this test occurs only on power up. Another RAM test occurs during PV and has a different error message. Use SA table E to isolate a RAM failure.

Area Tested:

All RAMs including refresh ability, the multiplexed memory Address/Data Bus from the CPU, motherboard connections between CPU and Display Controller board, the demultiplexed Address/Data bus to/from RAM, and the timing and control circuitry.

Operation:

a. This is a different test than the one performed during PV.

b. The RAM test takes approximately 7 seconds.

c. All RAM locations are toggled to insure READ/WRITE operation.

d. Refresh ability is verified.

e. The operation of the routine is as follows:

1. Load RAM with a count, starting with zero.

2. Read RAM and compare with count.

3. Check for an error. If error occurs go to error sequence.

4. If there is no previous error, wait one second.

5. Read RAM and compare with count.

6. Check for an error. If error occurs go to error sequence.

7. If there is no previous error load RAM with complement of count, starting at zero.

8. Read RAM and compare with the complement of the count.

9. Check for an error. If error occurs go to error sequence.

10. If there is no previous error, wait one second.

11. Read RAM and compare with count.

12. Check for an error. If error occurs go to error sequence.

f. If there are aren't any errors in either RAM error mask then the system will beep twice. But, if an error exists then following error sequence occurs:

1. Reset the delta timer to prevent auto restart.

2. Set the SA latch.

3. Write to and read from all of RAM.

4. Provide stimulus to CRT controller.

5. Output RAM error display header information (including refresh error message if refresh error flag set).

6. Reset SA latch.

7. Output individual failing unit number for lower 16K RAM.

8. Output individual failing unit number for upper 16K RAM.

g. When a failure occurs the routine attempts to output an error message as follows:

```
SELF-TEST FAILURE          blinking
RAM TEST:
FAILING UNIT NUMBERS (S)
-------------------------
XY
```

"XY" corresponds to the U# of the failing RAM. Depending on which RAM is failing, the display could be affected. Evidence of this is a random pattern on the CRT or incorrect spelling of messages For this reason the accuracy of a RAM test failure is always suspect. Because the RAMs are 1 bit wide, 16 of the 32 RAMs are used to store display information. U23-U30 and U38-U45 on the display controller board are used for display memory. Thus, if any of these 16 RAMs is failing, the display will be unintelligible to various degrees.

4-5. PV RAM TEST.

Purpose:

The RAM test verifies the ability to read and write from all RAM located on the display control board and checks for refresh. Note that this test occurs during PV. Another RAM test occurs during PV and has a different error message. Use SA table E to isolate a RAM failure.

Area Tested:

All RAMs including refresh ability, the multiplexed memory Address/Data Bus from the CPU, motherboard connections between CPU and Display Controller board, the demultiplexed Address/Data bus to/from RAM, and the timing and control circuitry.

Operation:

a. This test takes approximately eight seconds.

b. Data from ROM is written into RAM, and then read back and compared to the ROM contents.

c. The second step writes walking 1's and 0's to each RAM address and reads it back. The walking 1's and 0's are visable on the CRT as a blinking pattern with characters moving to the bottom of the screen.

d. The RAM test is interpreted as follows:

NOTE

Since the display uses 16 of the 32 RAMs, a RAM failure may affect the ability to display the bad RAM number.

RAM TEST: BIT ERROR MASK UPPER BANK=XXXX LOWER BANK=XXXX

The XXXX is the hexidecimal representation of the 16 bit error mask. Since each RAM is 16K x 1 bit, each RAM IC is one data bit for the entire 16K address range of the upper or lower bank. There is a one to one correlation between the data bit set in the error mask and the failing RAM.

If the error message reads, "UPPER BANK = 0201."

The problem is with U39 and U23.

If the error message reads, "LOWER BANK = 3000."

The problem is with U70 and U69.

4-6. TROUBLESHOOTING USING SIGNATURE ANALYSIS.

4-7. Signature Analysis (SA) offers a fast and convenient method of isolating hardware logic failures down to the component level. The basic concept is to utilize a known set of start, stop and clock signals that constantly repeat (loop) with the same timing relationships. When a suspect logic node is probed with a Signature Analyzer while using the start, stop, and clock signals as control inputs, the digital readout (signature) displayed on the analyzer can be compared with the normal signature of that node to determine if the timing relationships are proper. With the 64100 Mainframe, looping is provided by the PV software program and the normal signatures for various nodes are listed in the tables 4-1 thru 4-13.

4-8. SERVICE TOOLS.

4-9. SUGGESTED SERVICE TOOLS ARE:

1. HP 5004A or 5005A Signature Analyzer
2. Digital Voltmeter
3. Oscilloscope
4. Standard hand tools for electronic PC board repair.

4-10. SA TABLES.

4-11. The basic procedure is to refer to the appropriate table (i.e., the one that corresponds to the loop that PV was exercising when the failure was noted) and connect the Signature Analyzer to the Test Points called for in the table. Next, verify that the Vh signature indicated in the test set-up is proper. This signature is very important since it verifies that the start, stop and clock signals are normal. If this signature is good, proceed with the signatures listed in the table while referring to the appropriate schematic for guidance. If an improper signature is noted, check on both sides of the device to determine if it is causing the problem or if the problem has its origin further upstream.

4-12. If SA is taken using a 5004A Signature Analyzer, and loop P is good, it will be necessary to troubleshoot the shift registers U89 and U90 to the video output signals LIVID and LIVD with an oscilloscope and logic probe. However, if a 5005A Signature Analyzer is used, SA can be taken. The reason being, this circuitry is run by a 25 MHz signal called DOTCLK and the 5004A will not operate at that speed. If the signatures in loop P are good, and the circuitry from the shift registers U89 and U90 to the video output check good, then check the high voltage, the horizontal sync, and the vertical sync on the display driver board. Waveforms for the sync signals are provided in section VIII.

Table 4-1. SA Loop A

PC Board: Display Controller Board
Test failure or circuit: Power-up RAM Test failure
Procedure:
S/A hookup:
Start = Pos edge CPU Bd. TP10 (S.A. Interval)
Stop = Neg edge CPU Bd. TP10 (S.A. Interval)
Clock = Pos edge CPU Bd. TP1 (LSTB)
VH = CA27

Node	Sig	Node	Sig
U 79- 2	P29H	U 84- 3	P8UF
U 79- 5	9CPU	U 84- 5	3963
U 79-11	6445	U 84- 7	PA14
		U 84- 9	U175
U 80- 2	S0C0	U 84-12	0UU7
U 80- 5	U94H	U 84-14	H5H2
U 80-11	APHS	U 84-16	C6FA
U 80-14	4534	U 84-18	F47H
U 81- 2	A91A	U 85-11	F865
U 81- 5	U664	U 85-12	1A71
U 81-11	F8FF	U 85-13	C564
		U 85-14	5CH1
U 82- 2	5FAC	U 85-15	H467
U 82- 5	2830	U 85-16	1A92
U 82-11	4P85	U 85-17	38HF
U 82-14	0123	U 85-18	PUUF

Table 4-2. SA Loop B

PC Board: Display Controller Board
Test failure or circuit: Power-up RAM failure - Data writes to RAM
Procedure:
S/A hookup:
Start = Pos edge CPU Bd. TP10 (S.A. Interval)
Stop = Neg edge CPU Bd. TP10 (S.A. Interval)
Clock = Neg edge Disp Controller U21-10 (HWRT)
VH = 40P9
* = Probe Blinking

Node	Sig	Node	Sig
U 84- 1	40P9	U 85- 1	0000
U 84- 3	CPP7	U 85-11	17F2
U 84- 5	F7C2	U 85-12	PCH0
U 84- 7	H7H9	U 85-13	e43A
U 84- 9	07H2	U 85-14	9A6A
U 84-12	1H3P	U 85-15	PC5C
U 84-14	7C0C	U 85-16	8658
U 84-16	0CC1	U 85-17	A730
U 84-18	379A	U 85-18	6U1A
		U 85-19	40P9

Table 4-3. SA Loop C

PC Board: Display Controller Board
Test failure or circuit: Power-up Ram failure
Procedure:
S/A hookup:
Start = Pos edge CPU Bd. TP10 (S.A. Interval)
Stop = Neg edge CPU Bd. TP10 (S.A. Interval)
Clock = Pos edge Disp Controller TP11 (HPRAS)
Vh = A6U4
* = Probe Blinking

Node	Sig	Node	Sig
U18-7	0000*	U79-5	4HC3
		U79-7	PC47
U48-5	VH*	U79-9	472H
		U79-11	P1H9
U49-4	CF7U	U82-2	H7Hf
U49-7	4HC3	U82-4	7128
U49-9	P1H9	U82-5	574F
		U82-11	A41P
U50-4	H7HF	U82-12	6158
U50-7	574F	U82-14	F7AF
U50-9	A41P		
U50-12	F7AF		
U79-2	CF7U		
U79-4	1A8C		

Table 4-4. SA Loop D

PC Board: Display Controller
Test failure or circuit: Power-up RAM failure - Data reads from RAM and column address
Procedure:
S/A hookup:
Start = Pos edge CPU Bd. TP10 (S.A. Interval)
Stop = Neg edge CPU Bd. TP10 (S.A. Interval)
Clock = Neg edge Disp Controller TP6 (LPCAS)
Vh = A6U4
* = Probe Blinking

Node	Sig	Node	Sig
U18-7	0000*	U84-3	9343
		U84-5	2A93
U48-5	0000*	U84-7	03FP
		U84-9	9H0U
U49-4	6173	U84-12	008C
U49-7	1CPA*	U84-14	253C
U49-9	1F19	U84-16	9316
		U84-18	PCPP
U50-4	UC32		
U50-7	66UP	U85-11	A996
U50-9	286P	U85-12	2CF3
U50-12	PA39	U85-13	4U1F
		U85-14	935P
U80-2	UC32	U85-15	CP86
U80-4	5HF6	U85-16	A0HC
U80-5	66UP	U85-17	PF69
U80-7	F00A	U85-18	5U76
U80-11	1F19		
U80-12	4FFH		
U80-14	PA39		
U81-2	6173		
U81-4	F787		
U81-5	1CPA		
U81-7	CH1P		
U81-9	CAPH		
U81-11	1F19		

Table 4-5. SA Loop E

PC Board: Display Controller
Test failure or circuit: Power-up RAM failure, RAM outputs
Procedure:
S/A hookup:
Start = Pos edge CPU Bd. TP10 (S.A. Interval)
Stop = Neg edge CPU Bd. TP10 (S.A. Interval)
Clock = Pos edge Disp Controller TP15
Vh = P000

Node	Sig	Node	Sig
U23-14	8AAA	U38-14	AH28
U31-3	8AAA		
U85-11	8AAA		
U24-14	P444	U39-14	C211
U31-5	P444		
U85-12	P444		
U25-14	9838	U40-14	APH6
U31-7	9838		
U85-13	9839		
U26-14	4A2H	U41-14	6252
U31-9	4A2H		
U85-14	4A2H		
U27-14	PU53	U42-14	CF46
U31-12	PU53		
U85-15	PU53		
U28-14	4013	U43-14	FF7H
U31-14	4013		
U85-16	4013		
U29-14	5AH3	U44-14	F8AA
U31-16	5AH3		
U85-17	5AH3		
U30-14	A247	U45-14	CUUU
U31-18	A247		
U85-18	A247		

Table 4-6. SA Loop G

PC Board: Display Controller
Test failure or circuit: Power-up RAM failure
Procedure:
S/A hookup:
Start = Pos edge Disp Controller TP3 (Vert Sync)
Stop = Neg edge Disp Controller TP3 (Vert Sync)
Clock = Pos edge Disp Controller TP7 (HDRAS)
Vh = P5H2
* = Probe Blinking

Node	Sig	Node	Sig
U17-3	CP11	U64-11	A775
		U64-12	8H02
U18-7	P5H2*	U64-13	2P42
		U64-14	C963
U21-2	5FC1	U64-15	52A2
U48-5	P5H2*	U79-4	5CF3
		U79-7	4U2A
U49-4	CP11	U79-9	AC8F
U49-7	AAU8		
U49-9	4P5P	U82-4	88UH
		U82-7	42A7
U50-4	6H2U	U82-9	68H0
U50-7	A775	U82-12	FC90
U50-9	8H02		
U50-11	1734		
U62-11	P2A0		
U62-12	AAU8	NOTE: If the signatures of U79 and U82 are unstable, use NEG clock edge for these two components.	
U62-13	4P5P		
U62-14	6H2U		
U62-15	5U8F		

Table 4-7. SA Loop H

PC Board: Display Controller
Test failure or circuit: Power-up RAM failure
Procedure:
S/A hookup:
Start = Pos edge Disp Controller TP3 (Vert Sync)
Stop = Neg edge Disp Controller TP3 (Vert Sync)
Clock = Neg edge Disp Controller TP13
Vh = P5H2
* = Probe Blinking

Node	Sig	Node	Sig
U1-11	P5H2*	U63-11	6C86
		U63-12	8P54
U17-5	P5H2*	U63-13	U2P6
U17-6	0000*	U63-14	73P7
U18-7	P5H2*	U80-4	8P54
		U80-7	6C86
U47-6	P5H2*	U80-9	1734
		U80-12	9635
U48-5	0000*		
		U81-4	P5H2*
U49-4	0000*	U81-7	P5H2*
U49-7	0000*	U81-9	P5H2*
U49-9	0000*		
U50-4	6C86		
U50-7	8P54		
U50-9	U2P6		
U50-12	73P7		

Table 4-8. SA Loop I

PC Board: Display Controller
Test failure or circuit: Any test - Arbitrator circuit - No clocks on TP6, TP7, or TP11.

Procedure:
Remove CPU Bd., I/O Bd., and Disp Driver Bd. Move TEST jumper to TEST position.

S/A hookup:
Start = Pos edge TP14
Stop = Pos edge TP14
Clock = Pos edge TP2
Vh = UP73
* = Probe Blinking

Node	Sig	Node	Sig
U1-3	55H1	U20-6	UP73
U1-8	UP51	U20-8	H4C1
U2-11	8135	U22-1	0000
U2-12	86F1	U22-4	0000
U2-14	ACA2	U22-13	669P
U5-11	8117	U35-1	0022
U9-13	ACA2	U35-4	2275
10-6	UP73*		
U10-7	55H1	U36-8	UP73
		U36-11	HF06
U15-3	7U24		
U15-6	UP73	U37-3	7U46
U15-8	UP73	U37-6	UP51
		U37-8	7U46
U16-6	UF74	U37-11	7U24
U16-8	UF74		
		U48-5	7U46
U18-7	HF06	U48-9	7U06
U18-9	2275	U86-11	0022

Table 4-9. SA Loop P

PC Board: Display Controller
Test failure or circuit: Display pattern
Procedure:
S/A hookup:
Start = Neg edge Disp Controller TP3 (Vert Sync)
Stop = Pos edge Disp Controller TP3 (Vert Sync)
Clock = Pos edge Disp Controller TP4
Vh = UA11
* = Probe Blinking

Node	Sig	Node	Sig
U1-6	0000	U59-2	UA10
		U59-3	0000*
U5-8	7P31	U59-8	UFF7
U7-11	UA11*	U59-9	06H6
U9-1	06H6	U60-2	0000*
		U60-6	0000*
U11-8	FHCF	U60-10	0000*
		U60-11	UA11*
U12-9	UA11*		
		U74-9	P719
U33-1	34FH	U74-10	6FUF
U33-2	5F34	U74-11	7260
U33-3	7H30	U74-13	82UA
U33-4	990C	U74-14	71HU
U33-5	8F61	U74-15	AH4F
U33-7	049A	U74-16	5HFP
U33-8	UA10	U74-17	0000*
U33-23	4UU3		
U33-24	P635	U75-11	24UU
U33-25	3272		
U33-26	C1A6	U76-15	7867
U33-27	0000*		
U33-28	PA40	U77-5	0HAH
U33-29	1051	U77-9	0472
U33-35	UA11*		
U33-36	0000*	U91-5	0000*
U33-37	0000*	U91-9	24UU

Table 4-10. SA Loop Q

PC Board: Display Controller
Test failure or circuit: Display pattern
Procedure:
S/A hookup:
Start = Pos edge Disp Controller TP3 (Vert Sync)
Stop = Neg edge Disp Controller TP3 (Vert Sync)
Clock = Pos edge Disp Controller TP13
Vh = P5H2
* = Probe Blinking

Node	Sig	Node	Sig
U9-10	H5AU	U46-2	7328
		U46-5	4319
U13-1	74P7	U46-6	307H
U13-4	6176	U46-9	0A6C
U13-10	4186	U46-12	9135
U13-13	75FH	U46-14	6U9U
		U46-15	84AC
U19-3	A6FC	U46-16	A454
U19-6	PUC9		
U19-8	96AU	U49-6	307H
		U49-9	0A6C
U35-13	0000*	U49-12	9135
		U46-14	6U9U
		U46-15	84AC
		U46-16	A454
		U49-6	4U2A

Table 4-11. SA Loop R

PC Board: Display Controller
Test failure or circuit: Display pattern
Procedure:
S/A hookup:
Start = Pos edge Disp Controller TP3 (Vert Sync)
Stop = Neg edge Disp Controller TP3 (Vert Sync)
Clock = Pos edge Disp Controller U1-11
Vh = 1F8C

Node	Sig	Node	Sig
U23-14	F5U0	U38-14	0HF9
U24-14	F88P	U39-14	1F61
U25-14	260A	U40-14	3734
U26-14	H0H7	U41-14	60PF
U27-14	6536	U42-14	5448
U28-14	2C74	U43-14	06C6
U29-14	C71P	U44-14	U5U9
U30-14	P8PH	U45-14	8H26
U32-3	0HF9		
U32-5	1F61		
U32-7	3734		
U32-12	5448		
U32-14	06C6		
U32-16	U5U9		
U32-18	8H26		

Table 4-12. SA Loop S

PC Board: Display Controller Board
Test failure or circuit: Display Pattern
Procedure:
S/A hookup:
Start = Pos edge Disp Controller TP3 (Vert Sync)
Stop = Neg edge Disp Controller TP3 (Vert Sync)
Clock = Pos edge Disp Controller U47-6
Vh = 1F8C

Node	Sig	Comments
U23-14	U767	These signatures are at the RAM outputs. When looking at latched data from previous clock, they show that the refresh addressing and RAM output is OK and have nothing to do with U42 signatures.
U24-14	HA7H	
U25-14	175F	
U26-14	355A	
U27-14	9015	
U28-14	210U	
U29-14	U711	
U30-14	2HA7	
U46-2	P8PH	These are the same as RAM output in loop R; RAM output is verified in loop R.
U46-5	C71P	
U46-6	2C74	
U46-9	6535	
U46-12	H0H7	
U46-15	260A	
U46-16	F88P	
U46-19	F5U0	

Table 4-13. SA Loop T

PC Board: Display Controller Board
Test failure or circuit: Display Pattern
Procedure:
S/A hookup:
Start =Pos edge CPU Bd. TP10 (S.A. Interval)
Stop =Neg edge CPU Bd. TP10 (S.A. Interval)
Clock = Pos edge CPU Bd. TP1 (LSTB)
Vh = AU94
* = Probe Blinking

Node	Sig	Node	Sig
U5-3	1021	U78-10	0UUP
		U78-11	H98H
U7-3	51P7	U78-12	9UU9
		U78-13	5586
U15-11	4472	U78-14	7F46
		U78-15	859U
U21-10	PP52		
		U83-1	AA21
U33-21	90A9	U83-2	UCF6
		U83-3	51P7
U35-10	UP73	U83-5	AA21
		U83-6	CA01
U47-3	4472	U83-8	PP52
		U83-10	0000*
U78-1	F99P	U83-11	51P7
U78-2	7942		
U78-3	5CH4		
U78-4	5452		
U78-5	5452		
U78-6	9C8H		
U78-7	6855		
U78-9	51P7		

Table 7-1. Replaceable Parts List

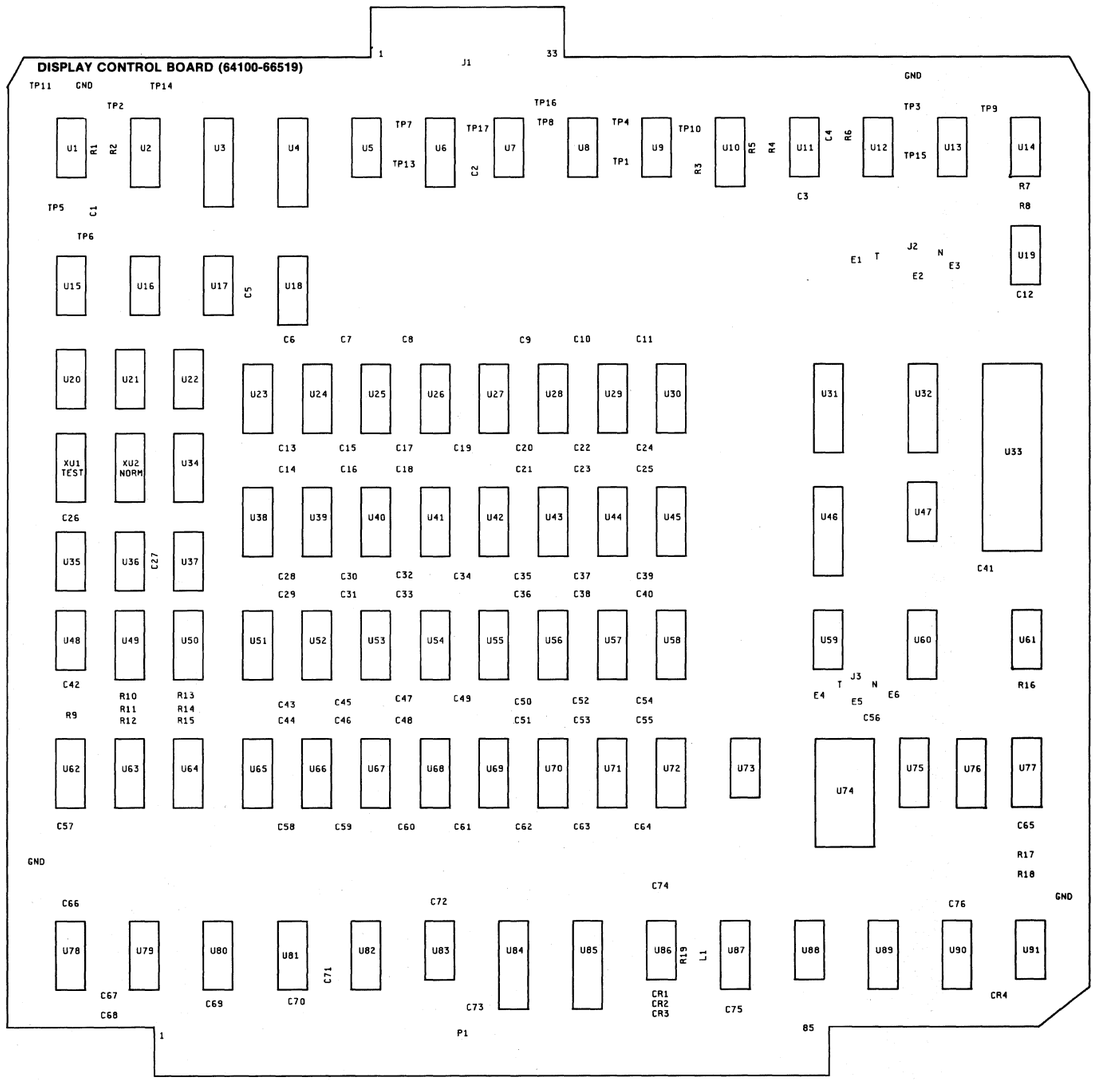
Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A5	64100-66519	5	1	DISPLAY CONTROLLER BOARD ASSEMBLY	28480	64100-66519
C1,2	0160-2055	9	30	CAPACITOR-FXD .01μF +80-20% 100VDC CER	28480	0160-2055
C3	0160-4822	2	1	CAPACITOR-FXD 1000Pf +-5% 100VDC CER	28480	0160-4822
C4,5	0160-2055	9		CAPACITOR-FXD .01μF +80-20% 100VDC CER	28480	0160-2055
C6	0160-3622	8	42	CAPACITOR-FXD .1μF +80-20% 100VDC CER	28480	0160-3622
C7	0160-2055	9		CAPACITOR-FXD .01μF +80-20% 100VDC CER	28480	0160-2055
C8,9	0160-3622	8		CAPACITOR-FXD .1μF +80-20% 100VDC CER	28480	0160-3622
C10	0160-2055	9		CAPACITOR-FXD .01μF +80-20% 100VDC CER	28480	0160-2055
C11	0160-3622	8		CAPACITOR-FXD .1μF +80-20% 100VDC CER	28480	0160-3622
C12	0160-2055	9		CAPACITOR-FXD .01μF +80-20% 100VDC CER	28480	0160-2055
C13,-15	0160-3622	8		CAPACITOR-FXD .1μF +80-20% 100VDC CER	28480	0160-3622
C16	0160-2055	9		CAPACITOR-FXD .01μF +80-20% 100VDC CER	28480	0160-2055
C17-22	0160-3622	8		CAPACITOR-FXD .1μF +80-20% 100VDC CER	28480	0160-3622
C23	0160-2055	9		CAPACITOR-FXD .01μF +80-20% 100VDC CER	28480	0160-2055
C24,25	0160-3622	8		CAPACITOR-FXD .1μF +80-20% 100VDC CER	28480	0160-3622
C26,27	0160-2055	9		CAPACITOR-FXD .01μF +80-20% 100VDC CER	28480	0160-2055
C28,30	0160-3622	8		CAPACITOR-FXD .1μF +80-20% 100VDC CER	28480	0160-3622
C31	0160-2055	9		CAPACITOR-FXD .01μF +80-20% 100VDC CER	28480	0160-2055
C32-37	0160-3622	8		CAPACITOR-FXD .1μF +80-20% 100VDC CER	28480	0160-3622
C38	0160-2055	9		CAPACITOR-FXD .01μF +80-20% 100VDC CER	28480	0160-2055
C39,40	0160-3622	8		CAPACITOR-FXD .1μF +80-20% 100VDC CER	28480	0160-3622
C41,42	0160-2055	9		CAPACITOR-FXD .01μF +80-20% 100VDC CER	28480	0160-2055
C43-45	0160-3622	8		CAPACITOR-FXD .1μF +80-20% 100VDC CER	28480	0160-3622
C46	0160-2055	9		CAPACITOR-FXD .01μF +80-20% 100VDC CER	28480	0160-2055
C47-52	0160-3622	8		CAPACITOR-FXD .1μF +80-20% 100VDC CER	28480	0160-3622
C53	0160-2055	9		CAPACITOR-FXD .01μF +80-20% 100VDC CER	28480	0160-2055
C54,55	0160-3622	8		CAPACITOR-FXD .1μF +80-20% 100VDC CER	28480	0160-3622
C56,57	0160-2055	9		CAPACITOR-FXD .01μF +80-20% 100VDC CER	28480	0160-2055
C58	0160-3622	8		CAPACITOR-FXD .1μF +80-20% 100VDC CER	28480	0160-3622
C59	0160-2055	9		CAPACITOR-FXD .01μF +80-20% 100VDC CER	28480	0160-2055
C60-62	0160-3622	8		CAPACITOR-FXD .1μF +80-20% 100VDC CER	28480	0160-3622
C63	0160-2055	9		CAPACITOR-FXD .01μF +80-20% 100VDC CER	28480	0160-2055
C64	0160-3622	8		CAPACITOR-FXD .1μF +80-20% 100VDC CER	28480	0160-3622
C65,66	0160-2055	9		CAPACITOR-FXD .01μF +80-20% 100VDC CER	28480	0160-2055
C67,68	0180-0374	3	2	CAPACITOR-FXD 10μF +-10% 20VDC TA	56289	150D106X902082
C69	0160-2055	9		CAPACITOR-FXD .01μF +80-20% 100VDC CER	28480	0160-2055
C70	0180-0116	1	1	CAPACITOR-FXD 6.8μF +-10% 35VDC TA	56289	150D685X9035B2
C71-76	0160-2055	9		CAPACITOR-FXD .01μF +80-20% 100VDC CER	28480	0160-2055
CR1-4	1901-0535	9	4	DIODE-SM SIG SCHOTTKY	28480	1901-0535
L1	9170-0029	3	2	CORE-SHIELDING BEAD	28480	9170-0029
MP1,2	5040-6067	2	2	PC EXTRACTOR	28480	5040-6067
P2,3	1258-0182	7	2	TEST JUMPER	28480	1258-0182
P4	1810-0307	0	1	NETWORK-CNDCT MODULE DIP; 16 PINS; 0.100	28480	1810-0307
R1-4	0757-0280	3	11	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R5	0698-3438	3	1	RESISTOR 147 1% .125W F TC=0+-100	28480	0698-3438
R6-9	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R10-15	0698-7028	5	6	RESISTOR 27 10% .125W CC TC=-270/+540	01121	BB2701
R16-18	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R19	0684-1211	7	1	RESISTOR 120 10% .25W FC TC=-400/+600	01121	CB1211
TP1-13	0360-0535	0	20	TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
TPGND	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
U1	1820-0681	4	3	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U2	1820-1453	0	2	IC CNTR TTL S BIN SYNCHRO POS-EDGE-TRIG	01295	SN74S163N
U3,4	1820-1917	1	2	IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U5	1820-1201	6	1	IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
U6	1820-1453	0		IC CNTR TTL S BIN SYNCHRO POS-EDGE-TRIG	01295	SN74S163N
U7	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U8	1820-1112	8	3	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74N
U9	1820-1322	2	2	IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U10	1820-0629	0	2	IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
U11	1820-1449	4	1	GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U12	1820-0693	8	3	IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
U13	1820-1144	6	2	IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02
U14	1820-0683	6	2	IC INV TTL S HEX 1-INP	01295	SN74S04N
U15	1820-1208	3	4	IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
U16	1820-0688	1	2	IC GATE TTL S NAND DUAL 4-INP	01295	SN74S20N
U17	1820-1211	8	1	IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS86N
U18	1820-0629	0		IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
U19	1820-1197	9	1	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U20	1820-0688	1		IC GATE TTL S NAND DUAL 4-INP	01295	SN74S20N
U21	1820-0683	6		IC INV TTL S HEX 1 INP	01295	SN74S04N
U22	1820-1322	2		IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U23-30	1818-1396	5	32	IC NMOS 16348-BIT RAM DYN 200NS 3S	50088	MK4116N-3
U31,32	1820-2024	3	3	IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U33	1820-2191	5	1	IC MICROPROC-ACCESS NMOS 8-BIT	34649	C8275
U34	1810-0536	7	1	NETWORK-RES 27OHM 16 PIN DIP	28480	1810-0536
U35	1820-1144	6		IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
U36	1820-1208	3		IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
U37	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U38-45	1818-1396	5	32	IC NMOS 16384-BIT RAM DYN 200-NS 3-S	50088	MK4116N-3
U46	1820-1997	7	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U47	1820-1208	3		IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
U48	1820-0693	8		IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
U49,50	1820-1015	0	2	IC MUXR/DATA-SEL S 2-TO-1-LINE QUAD	01295	SN74S158N
U51-58	1818-1396	5	32	IC NMOS 16384-BIT RAM DYN 200-NS 3-S	50088	MK4116N-3
U59	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74
U60	1820-1191	3	2	IC FF TTL S D-TYPE POS-EDGE-TRIG COM	01295	SN74S175N
U61	1820-0697	2	1	IC DRVR TTL S NAND LINE DUAL 4-INP	01295	SN74S140N
U62-64	1820-1435	8	3	IC CNTR TTL LS BIN UP/DOWN SYNCHRO	01295	SN74LS669N
U65-72	1818-1396	5	32	IC NMOS 16384-BIT RAM DYN 200-NS 3-S	50088	MK4116N-3
U73	0960-0530	7	1	OSCILLATOR 25MHz	28480	0960-0530
U74	1816-1496	3	1	IC ROM 2KX8	28480	1816-1496
U75,76	1820-1432	5	2	IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS163AN
U77	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74
U78	1820-1130	0	1	IC GATE TTL S NAND 13-INP	01295	SN74S133N
U79-82	1820-1428	9	4	IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS158N
U83	1820-1208	3		IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
U84	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U85	1820-2075	4	1	IC MISC TTL LS	01295	SN74LS245N
U86	1820-1451	8	1	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S38N
U87	1820-1191	3		IC FF TTL S D-TYPE POS-EDGE-TRIG COM	01295	SN74S175N

See introduction to this section for ordering information

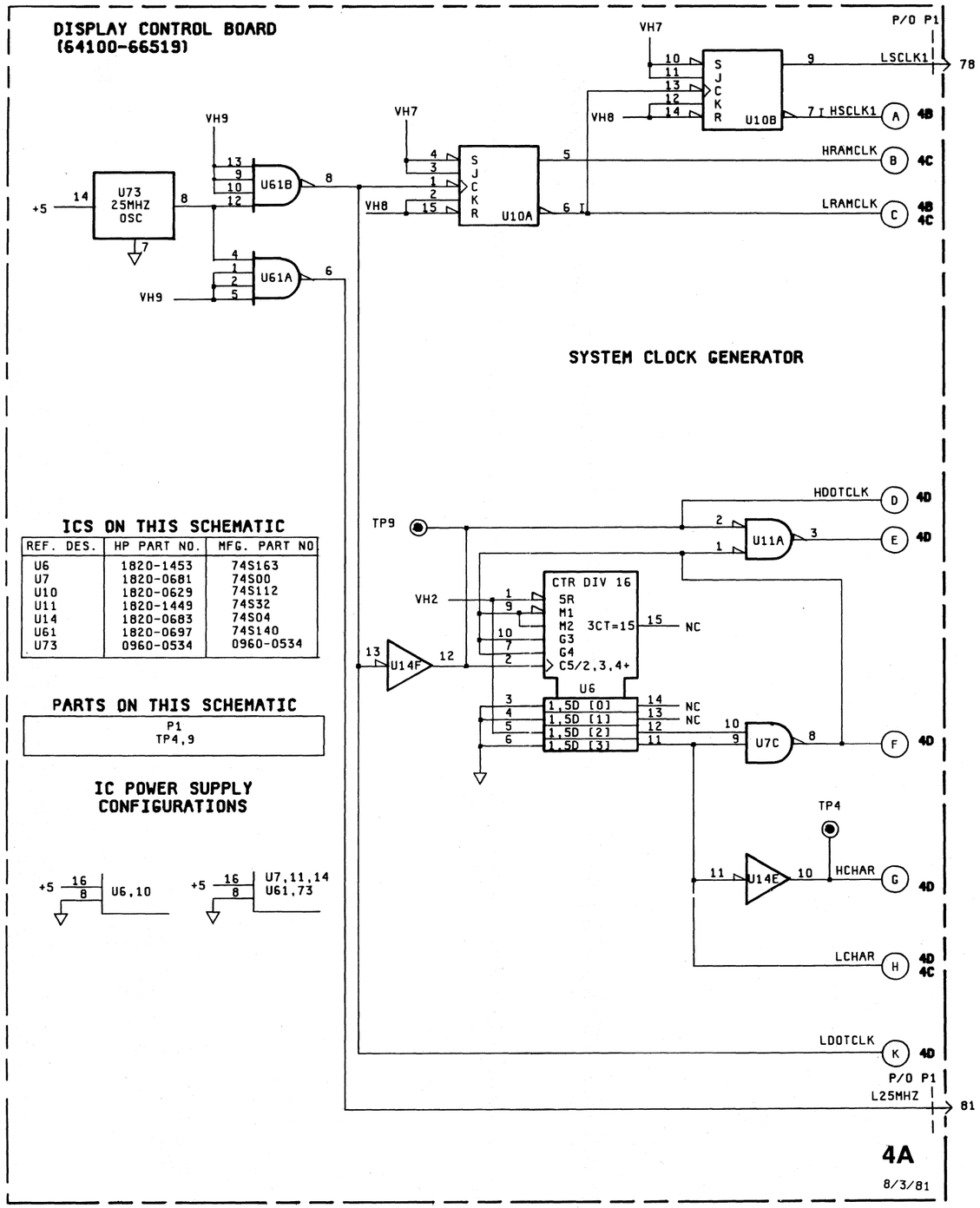
Table 7-1. Replaceable Parts List (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U88	1820-0685	8	1	IC GATE TTL S NAND TPL 3-INP	01295	SN74S10N
U89,90	1820-1303	9	2	IC SHF-RGTR TTL S R-S PRL-IN PRL-OUT	01295	SN74S195N
U91	1820-0693	8		IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
XU1,2	1200-0607	0	32	SOCKET-IC 16-CONT DIP-SLDR	28480	1200-0607
XU23-30	1200-0607	0		SOCKET-IC 16-CONT DIP-SLDR	28480	1200-0607
XU33	1200-0654	7	1	SOCKET-IC 40-CONT DIP-SLDR	24840	1200-0654
XU34	1200-0607	0		SOCKET-IC 16-CONT DIP-SLDR	28480	1200-0607
XU38-45	1200-0607	0		SOCKET-IC 16-CONT DIP-SLDR	28480	1200-0607
XU51-58	1200-0607	0		SOCKET-IC 16-CONT DIP-SLDR	28480	1200-0607
XU65-72	1200-0607	0		SOCKET-IC 16-CONT DIP-SLDR	28480	1200-0607
XU74	1200-0541	1	1	SOCKET-IC 24 CONT DIP SLDR	28480	1200-0541

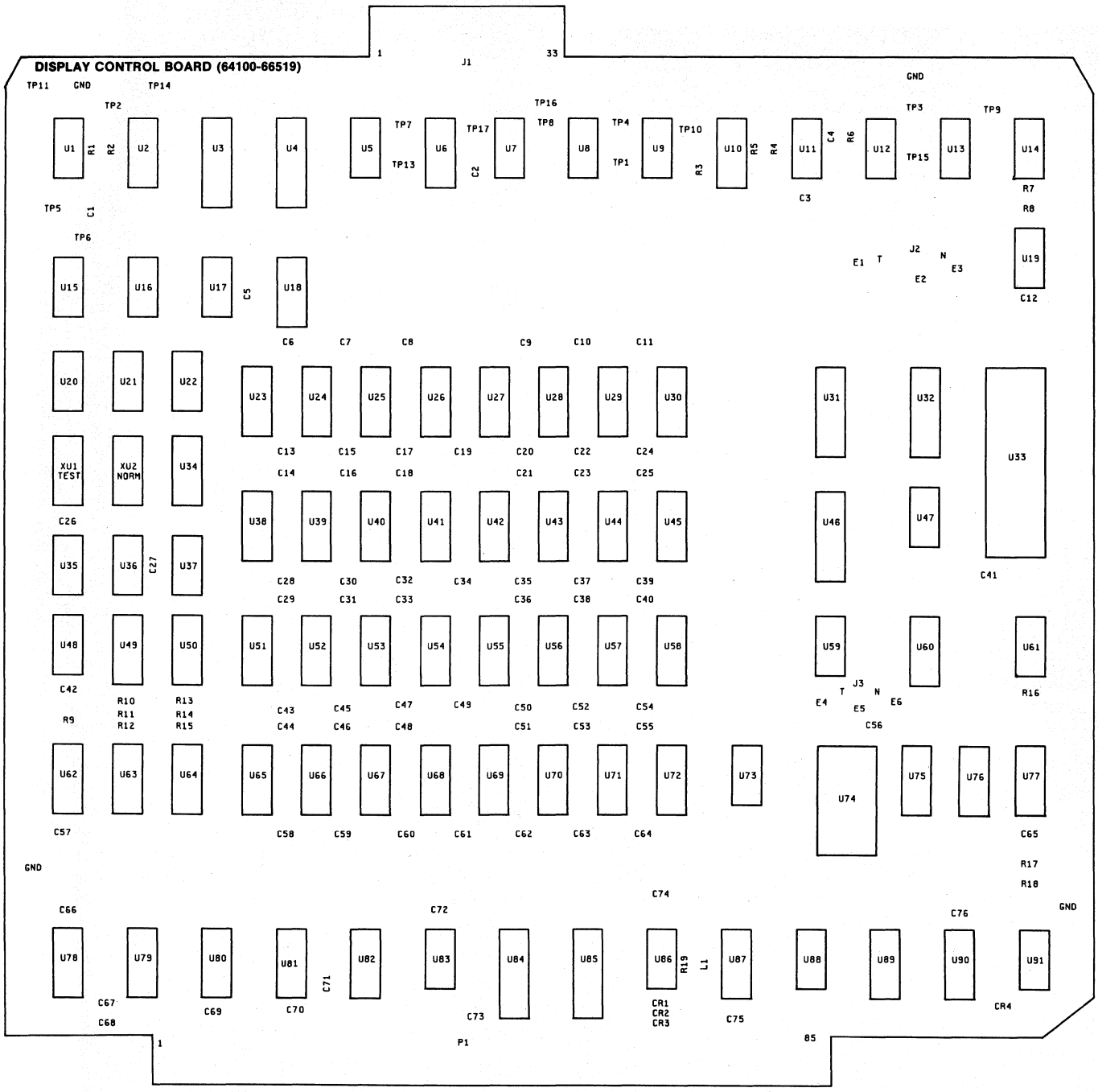
See introduction to this section for ordering information



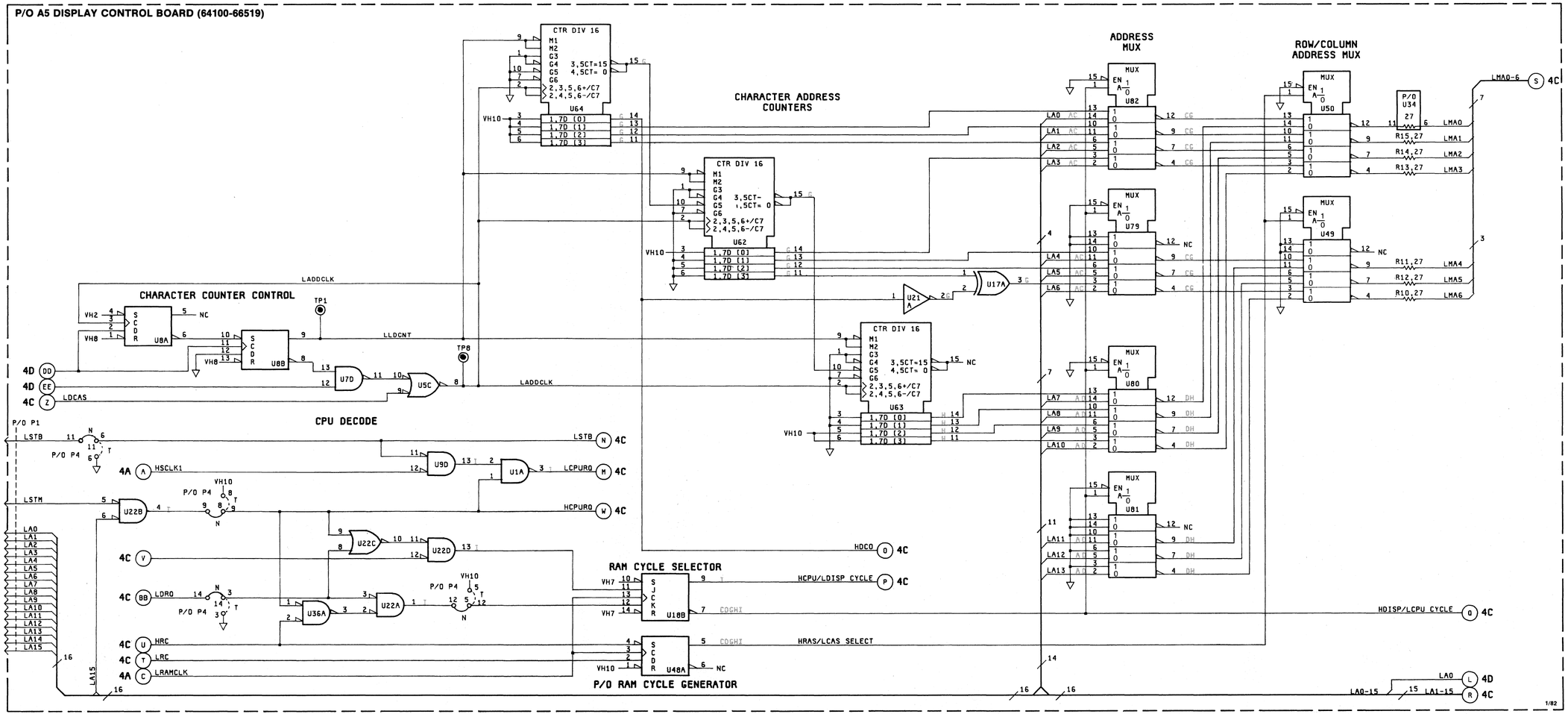
Display Controller Component Locator



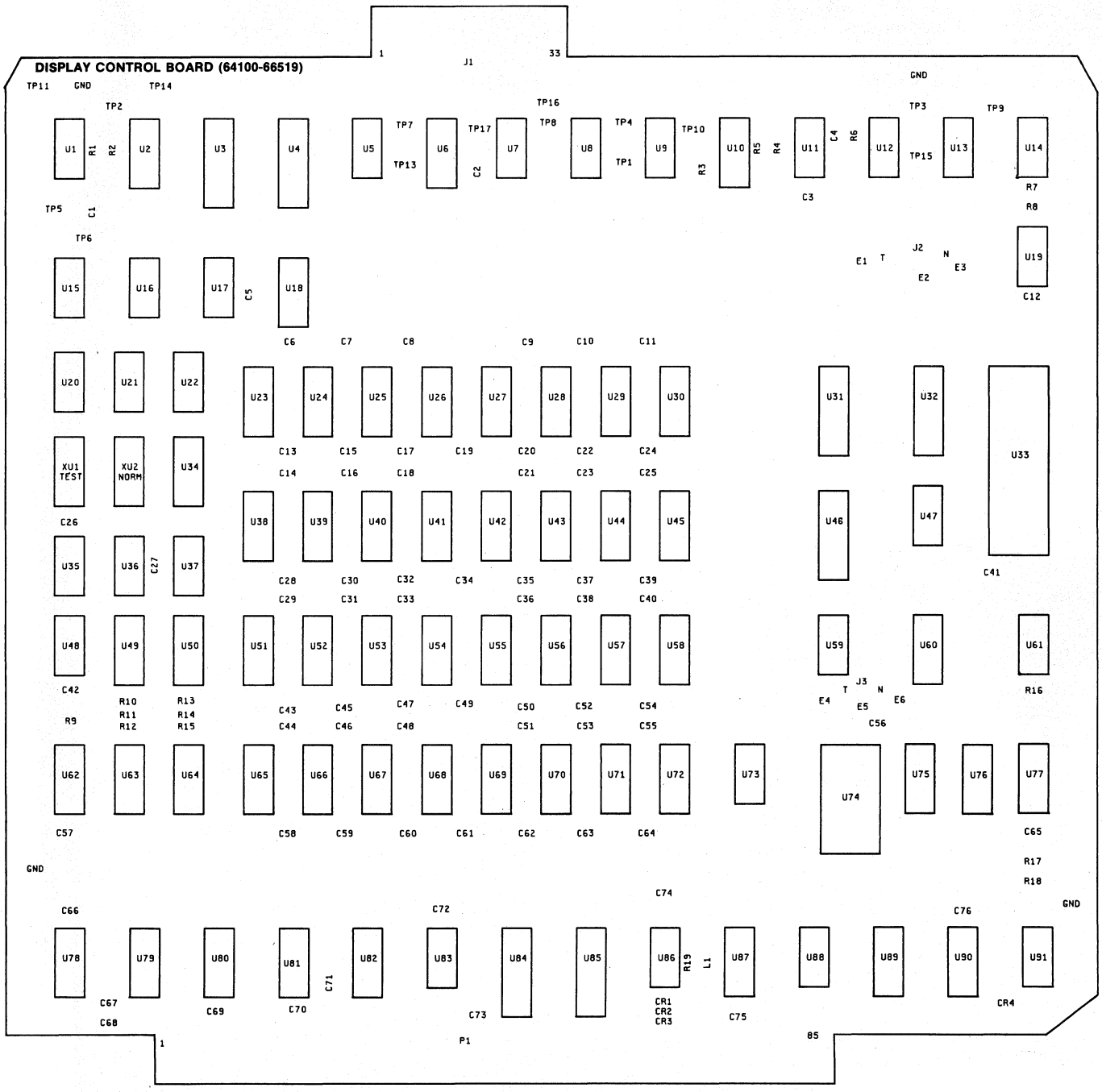
Display Controller Schematic 4A (Sheet 1 of 4)
MANUAL BACKDATING DSP 7-27



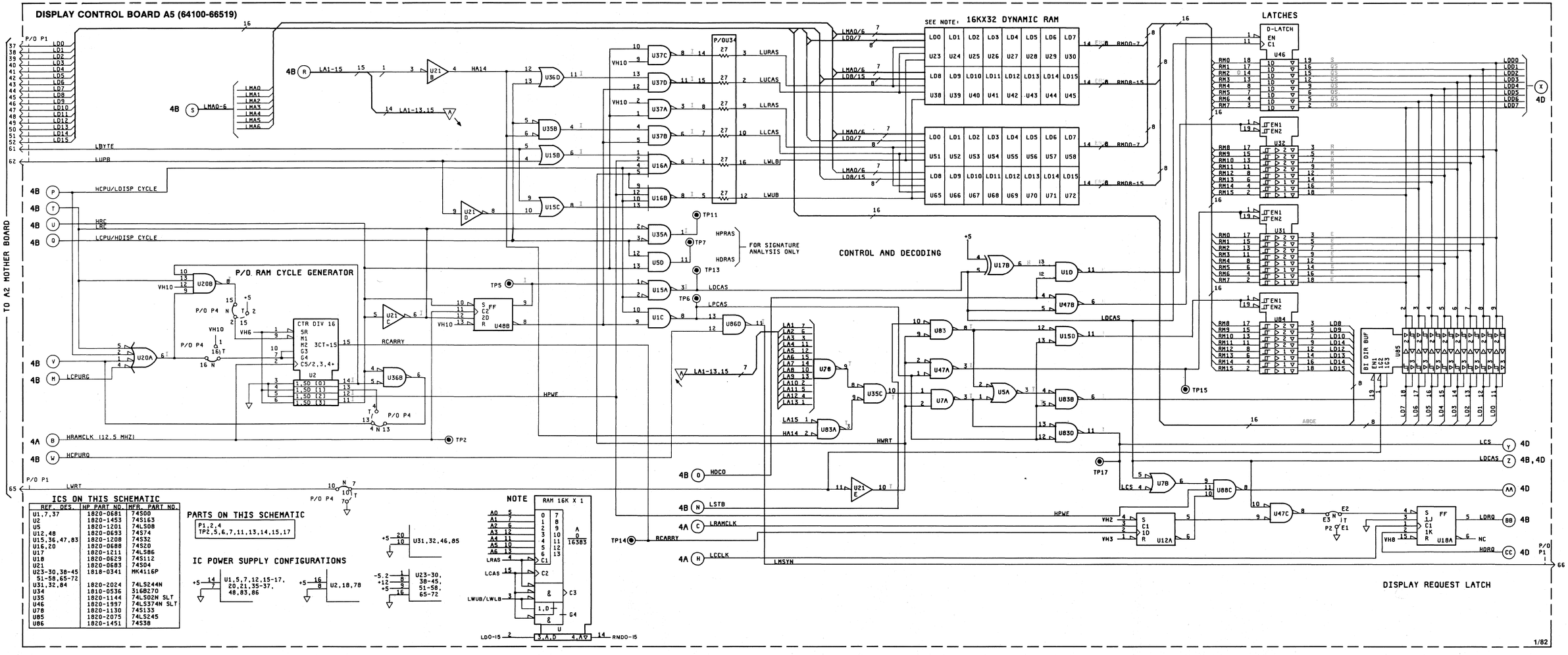
Display Controller Component Locator



Display Controller Schematic 4B (Sheet 2 of 4)
MANUAL BACKDATING DSP 7-29



Display Controller Component Locator



REF. DES.	HP PART NO.	MFR. PART NO.
U1,7,37	1820-0681	74S00
U2	1820-1453	74S163
U5	1820-1201	74LS08
U12,48	1820-0693	74S74
U15,36,47,83	1820-1208	74S32
U16,20	1820-0688	74S20
U17	1820-1211	74LS86
U18	1820-0629	74S112
U21	1820-0683	74S04
U23-30,38-45 51-58,65-72	1818-0341	MK4116P
U31,32,84	1820-2024	74LS244N
U34	1810-0536	316B270
U35	1820-1144	74LS02N SLT
U46	1820-1997	74LS374N SLT
U70	1820-1130	74S133
U85	1820-2075	74LS245
U86	1820-1451	74S38

PARTS ON THIS SCHEMATIC

P1,2,4
TP2,5,6,7,11,13,14,15,17

IC POWER SUPPLY CONFIGURATIONS

+5 14 7 U1,5,7,12,15-17, 20,21,35-37, 48,83,86

+5 16 8 U2,18,78

+5 20 10 U31,32,46,85

-5.2 1 +12 8 +5 9 16 U23-30, 38-45, 51-58, 65-72

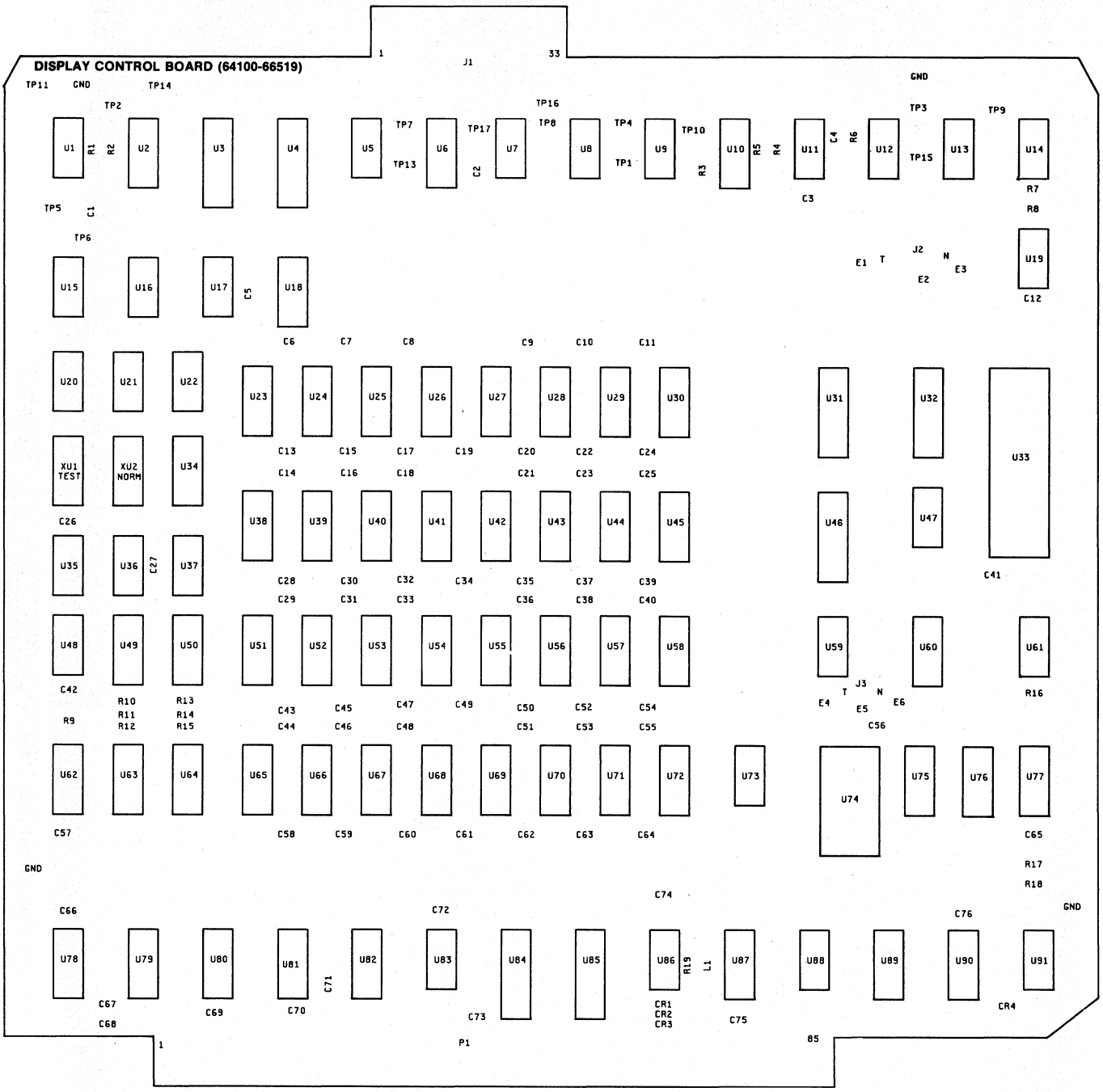
NOTE

RAM 16K X 1

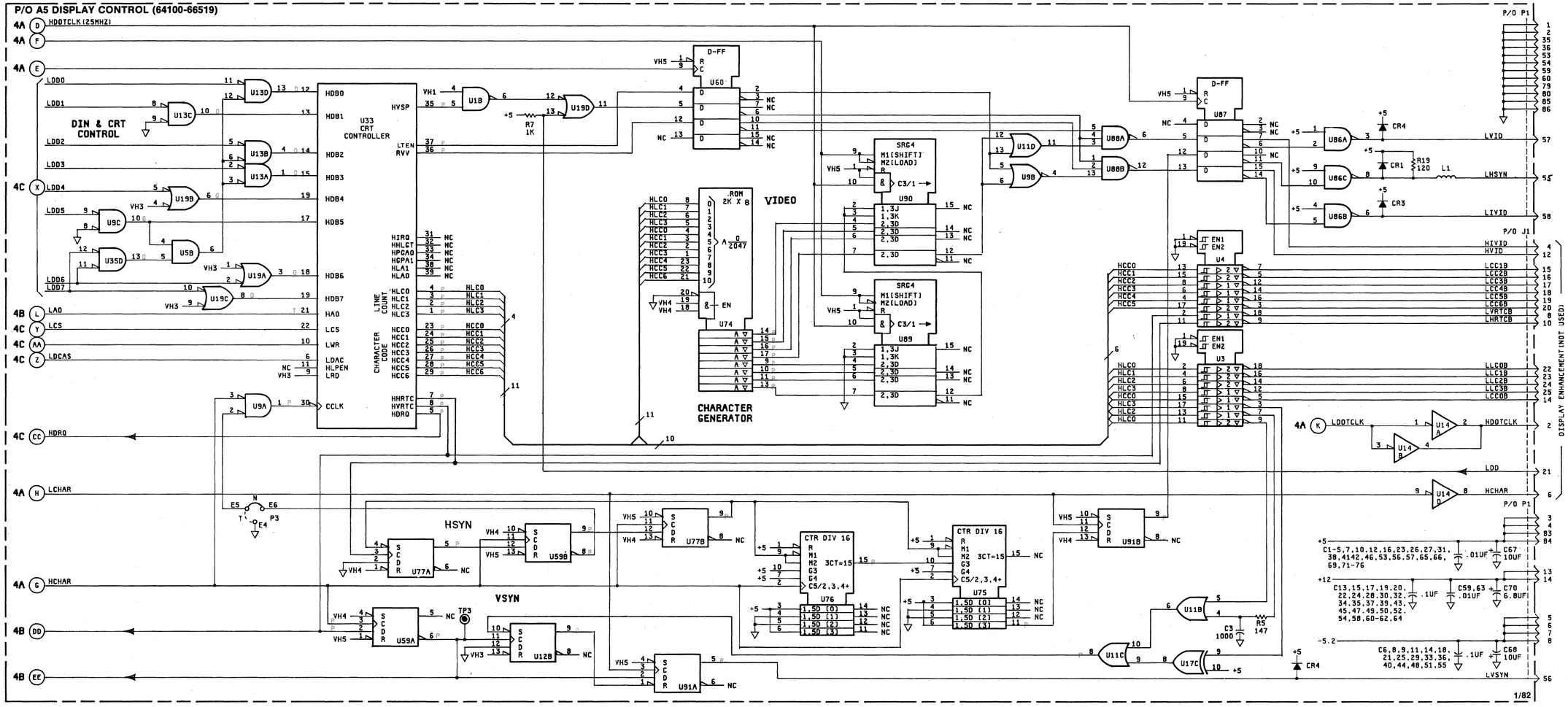
A0 A1 A2 A3 A4 A5 A6 DI WE RAS CAS LWUB/LWLB LDO-15 RMDO-15

U 16383

C1 C2 C3 G4 1,D 3,A,D 4,A



Display Controller Component Locator



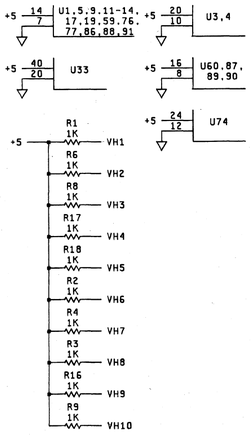
ICS ON THIS SCHEMATIC

REF. DES.	HP PART NO.	MFG. PART NO.
U1	1820-0681	74S00
U3,4	1820-1927	74LS240N
U5	1820-1201	74LS08
U9	1820-1322	74S02
U11	1820-1449	73S32
U12,91	1820-0693	74S74
U13	1820-1144	74LS02N SLT
U14	1820-0683	74S04
U17	1820-1211	74LS86
U19	1820-1197	74LS00
U33	1820-2191	8275A
U58,77	1820-1112	74LS74AN SLT
U60,87	1820-1191	74S175
U74	1816-1496	1816-1496
U75,76	1820-1432	74LS163
U86	1820-1451	74S38N
U88	1820-0685	74S10
U89,90	1820-1303	74S195

PARTS ON THIS SCHEMATIC

C1-76
CR1-4
L1
P3
R1-9,16-19
TP3
U1,3-5,9,11-14,17,19,33,59,60,74-77,86-91

IC POWER SUPPLY CONFIGURATIONS



4D

Display Controller Schematic 4D (Sheet 4 of 4)
MANUAL BACKDATING DSP 7-33/(7-34 blank)

SECTION VIII

SERVICE

8-1. BLOCK DIAGRAM THEORY.

8-2. The display section of the system consists of two circuit boards and a CRT (Cathode Ray Tube). The two boards are called the Display Controller and the Display Driver. All three of these components are represented on the Display Block Diagram in figure 8-1. Table 8-2 provides a list of mnemonics.

8-3. THE DISPLAY CONTROLLER BOARD.

8-4. The Display Controller A5 board serves two main functions, (1) provides the processor with a read/write (RAM) memory, and (2) generates the video control signals.

8-5. There are 16 RAMs (HM4864) used on the Display Controller board. Each RAM is a Dynamic Random Access Memory IC with 65,536-word x 1-bit of memory locations. The HM4864 operates from +5 volts relative to ground.

8-6. The use of the 16-pin package is made possible by multiplexing the 16 address bits (required to address 1 of the 64K bits) into the HM4864 on 8 address input pins. The two 8-bit address words are latched into the HM4864 by two TTL clocks, Low Row Address Strobe (LRAS) and Low Colomn Address Strobe (LCAS). Non-critical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

8-7. Data is stored in the HM4864 in single transistor, dynamic storage cells. The storage cells require refresh for data retention. Refreshing is accomplished by performing a memory read cycle at each of the 128 row addresses every 2 milliseconds. There are actually 256 row addresses (8-bit), but the RAMs are internally configured to 128 row (7-bit) addresses to be compatible with the Intel 2116 16K RAMs which were used on the earlier Display Controller board. A0 thru A6 are the refresh address pins.

8-8. ADDRESS AND DATA LATCHES. The 8-bit row and colomn address words are latched into internal latches by the LRAS and LCAS signals respectively. Both the Data Input and Data Output information is latched by the HM4864. The input data is latched by the logical AND function of LRAS, LCAS, and Low Write Enable (LWE). When a Data Input cycle is being performed (LRAS low), the data will be latched by the falling edge of the last two control signals (LCAS or LWE). The Data Output latch and buffer is controlled by LCAS. The leading (falling) edge of LCAS in any cycle causes the Data Output to assume an open-circuit (HI-Z) state. At access time (a delay time after LCAS goes low), the Data Output will assume a data state (high or low) dependent upon the type of data cycle performed. The Data Output remains valid until the next cycle during which a LCAS occurs.

8-9. REFRESH MODE. Read Cycle Refresh: A read cycle at each of the 128 row addresses (A0 - A6) will refresh all the storage cells. Write cycles also fulfill the refresh requirements but the selected cell (determined by the column address) on the row being refreshed, will have new data written into it while the remaining 127 cells on the row are simply refreshed.

8-10. There are 64K x 16 memory locations of RAM on the Display Controller board. The RAM is divided into two 32K x 16 memory locations. The address range for the upper 32K memory locations of RAM are from 8002 HEX to FFFF HEX. A part of this memory (F9F0 HEX to FF00 HEX) is dedicated to storing display information. The lower 32K x 16 memory locations of RAM are addressed over the Memory Mapped I/O and treated as if they were a Memory Expansion option in option slot 10. This method of addressing is used because the address range 0000 HEX to 3FFF HEX is dedicated to ROM and CPU memory.

8-11. When the CPU needs additional memory, it will poll the Slot Select lines (LSSEL0-10) and check the option slots for the additional memory. The Display Controller board uses option slot 10 (imaginary) as the location where the additional RAM (lower 32K x 16) can be memory mapped into. When the CPU reads slot 10, the ID 0402 HEX is read back. It then treats slot 10 as having a 32K x 16 Memory Expansion option installed.

8-12. RAM WRITE FUNCTION. The processor writes data into the RAM by placing the address of the location to be written on the address bus, selecting the memory and write functions by means of the arbitration and sequencer circuitry, and then presenting the data to be stored on the data bus. The arbitration and sequencer circuitry is responsible for gating the address through to the RAM address lines. Since the RAM address lines are multiplexed into two 8-bit segments, the sequencer must also control the byte select function (U50,U49).

8-13. RAM READ FUNCTION. The processor reads data from the RAM by placing the address of the location to be read on the address bus, selecting the memory and read function and then gating the RAM data out to the data bus through buffers U31,U70, and U71. The arbitrator sequencer and the RAM data out routing are responsible for the correct selection of the RAM output buffers.

8-14. DISPLAY SETUP. The CRT controller U33 must be programmed with display parameters, i.e. number of characters per row, number of rows, and number of lines per character row, before a display can be generated. The bi-directional buffer U71, allows the processor to directly load the display parameters into the CRT controller. This programming takes place very early in the system`s operating program and is latched into the CRT controller, thus occurring only once during power up.

8-15. DISPLAY OPERATION. A display operation is similar to a RAM read operation. However, the address for the display data is not taken from the address bus, but from the binary counters U56,U57,U58. When the binary counters are reset by the LLDCNT (Load Counter) signal, the address of the first display location (FA18 HEX) is loaded into the counters. The arbitration circuitry now gates the display address (FA18 HEX - FDFF hex), instead of the address bus, through to the address input lines of the RAM. address input lines of the RAM.

8-16. The 16-bit display data from RAM (ASCII code) is gated through Display Buffer U32 and Latch U46 to the CRT Controller U33. The least significant bit from the Display Address Counter U58 is used to enable the Buffer U32 or Latch U46. This bit is not used as an address bit to RAM. Since 16 bits of data are availible from RAM and the CTR Controller U33 can only use 8 bits at a time, 8 bits are passed through the Buffer U32 and 8 bits are latched in U46. The next time the CRT Controller U33 requests RAM and increments the Display Address Counters (U56-U58), bit 0 changes state to enable the latch U46. Then the CRT Controller reads the data that was latched into U46 during the previous cycle.

8-17. The very act of reading RAM refreshes the row that was accessed. When the CRT Controller U33 does a RAM access and reads the Buffer U32, it has refreshed a row of RAM. The next time it does an access, it reads the latched data in U46. But, the least significant bit has changed state and the row address that is going to RAM has been mapped by the XOR gate U17A causing a Read-Only-Refresh to be performed on another row of memory. In this manner the CRT Controller U33 reads at least 128 rows within 2 milliseconds required to guarantee that RAM is refreshed.

8-18. Internal to the CRT Controller U33 are two 80 character buffers that have dual roles. While the CRT Controller is requesting data and filling one buffer, the other buffer is being emptied to the output port. Typically, the 80 character input buffer is filled by the time the output buffer has written two or three of the fifteen lines in each row of characters. When the input buffer is filled, the CRT Controller U33 no longer requests RAM. When the CRT Controller reaches the end of the row of characters, the filled input buffer becomes the output buffer and the CRT Controller does 80 more RAM requests.

8-19. Every time a 80 character CRT controller buffer is reading the RAM for display information, a refresh operation occurs. It takes a little over three 80 character CRT controller buffer read operations to refresh all 128 rows in RAM. Each time a 80 character buffer is filled, 40 rows of RAM are refreshed.

8-20. The CRT controllers (U33) primary function is to refresh the display by buffering the display data and to keep track of the character position. The CRT controller outputs a code to the character generating ROM at U60 that describes the character to be displayed and what horizontal line is to be sent to the video drive circuits. The character generating ROM parallel loads the display information into the shift registers U76 and U77, which serially output the display information to the Display Driver board. The CRT controller also generates the vertical and horizontal sync pulses used to trigger the sweep circuits of the Display Driver board.

8-21. The Character Generater ROM is responsible for the correct dot pattern on the screen. It decodes the ASCII code into a dot pattern for each character of the 80 characters. The characters are placed on the screen one line of dots at a time for all 80 characters. It takes 15 lines to place the one row of 80 characters on the screen.

8-22. DISPLAY DRIVER BOARD.

8-23. The Display Driver board provides the video drive, voltage sweeps, and bias voltages to drive the CRT. The video drive circuit features two drive

levels, one for regular video, one for inverse video. The inverse video operates with half the intensity to reduce glare.

8-24. The high voltage circuit generates grid voltage of -40v, +300 to 800v, and 0 to 500v necessary to provide intensity and focus adjustments.

8-25. THEORY OF OPERATION.

8-26. DISPLAY CONTROLLER. The Display Controller board contains a system clock, RAM, and display circuitry. The RAM is shared by both the CPU and CRT controller. The arbitrator sequencer circuitry controls timesharing of the RAM between the Display Controller board and the CPU.

8-27. Information to be displayed on the screen is written into the RAM space by the CPU at the addresses that are addressed by the counters (FA18 HEX - FDFF HEX) for the display circuitry. Sixteen address bits are required to decode one location in RAM.

8-28. RAM WRITE. The CPU initiates a RAM write function to the upper 32K memory locations of RAM by pulling address bit 15 (LA15) low on U51 pin 3 and LSTM low on U51 pins 4, 5. The CPU initiates a write to the lower 32K memory location of RAM using LSSEL 10. LA15 must be high for a Memory Mapped I/O access, so LSSEL 10 is pulled low which places a low on U51 pin 2. When LSTM is true, a RAM write is initiated. The output of U51 is sent to the arbitrator sequencer circuitry producing a gating signal, output from U18, pin 7. This gating signal selects the CPU address lines LA0 - LA15 from the address select circuit. The address lines (LA0-15) are input to the byte select circuit and the upper or lower byte is selected by a gating signal from U48A, pin 5 to produce output address lines LMA0-7 to the RAM.

8-29. ADDRESS LINES. The CPU addresses RAM over 17 address lines (LA0-15 and LMAP1). The upper 32K x 16 memory locations of RAM are addressed using LA0-14 with LA15 pulled low. The address range is from 8002 HEX to FFFF HEX. The lower 32K x 16 memory locations of RAM are addressed over the Memory Mapped I/O. The lower 32K of RAM is accessed as if it were in option slot 10 (imaginary) with an ID of 0402 HEX. LA14 must be pulled low and LA15 must be forced high to access the Memory Mapped I/O. LMAP1 acts as LA14 does in the upper 32K of RAM. If LMAP1 is high, then the address range is in the upper 16K x 16 of the lower 32K of RAM. If LMAP1 is low then the address range is in the lower 16K x 16 of the lower 32K of RAM.

8-30. Address lines LMA0-7 are sent to the RAM circuit (see figure 8-4, sheet 4C), and determine where data (LD0-15) from the CPU will be stored in RAM. Control signals LWLB and LWUB determine whether data is written into the upper or lower byte or a READ operation is taking place.

8-31. RAM READ. The CPU reads data from the upper 32K of RAM by placing the address of the location to be read on the address bus (LA0-15). If the READ operation is from the lower 32K of RAM, then access is over the Memory Mapped I/O Slot Select. LA15 must be high and LA14 low to access the Memory Mapped I/O. LA0-13 and LMAP1 are the address bus for lower 32K RAM read operation.

Data (LD0-15) is read from the RAM when signals LWLB and LWUB are inactive (high). Data LD0-15 is gated to the data bus through buffers U31, U71, and U70.

8-32. DISPLAY FUNCTION. The CRT controller (U33) is loaded with display parameters (D0-7) directly from the CPU by means of U71. The display parameters are loaded once during power up. The CRT controller's primary function is to refresh the display and keep track of character position.

8-33. The addresses for display information (FA18 HEX - FDFF HEX) is taken from the character counter circuit (U56 thru 58). Signal Low Load Counter (LLDCNT) resets the address counters and the address of the first display location is loaded. This address is set to the address select circuitry. The arbitrator sequencer circuitry now gates the display address, instead of the address bus through the Row/Column Address MUX circuitry to the address input lines of the RAM.

8-34. The output data (D0-7) is gated through the Display Controller (U33). Since the CRT controller (see figure 8-4, sheets 4B and 4D) can accept only 8 bits of data at a time, U46 latches half of the 16 bit output of the RAM. Data from U46 is accepted by the CRT controller after the data from U32 is accepted. The CRT controller then outputs an ASCII code which is sent to the character generator ROM circuit U60 describing the character to be displayed and what horizontal line is to be sent to the video drive circuits. The character generator ROM circuit then parallel loads the display information into the shift register circuit (U76 and U77). The character dot patterns are shifted to the output circuitry in serial form one row at a time.

8-35. DISPLAY DRIVER. The Display Driver Board provides the video drive, voltage sweeps, and bias voltages to drive the CRT.

8-36. Display Controller U33 on the Display Controller Board provides horizontal and vertical retrace signals and the low video and low inverse video signals. The Display Driver is enabled by high display enable HDE from the I/O Board. (See figure 8-8.)

8-37. With no video signal applied, low inverse video (LIVID) and low video (LVID) are high, forcing the open-collector outputs of U3A and U3C low. Q8 is an emitter follower and supplies current necessary to keep the Q8 emitter voltage near 30V and the video off.

8-38. If LVID goes low with LIVID high, the open-collector output of U3A releases the base of Q7 and allows it to turn on, CR15 and CR16 prevent it from saturating. When Q7 turns on, it holds the base voltage of Q8 low forcing the emitter voltage of Q8 low and the video full on.

8-39. If LIVID were to go low while LVID was low, Q6 would be allowed to turn on. But since the base voltage of Q8 is being held low by Q7, it makes no difference what state Q6 is in.

8-40. If LIVID is low while LVID is high, the open-collector input of U3C releases Q6 to turn on while U3A holds Q7 off. The voltage drop across VR2, CR13, and Q6 establishes an intermediate base voltage on the emitter follower, Q8, and the video is at an intermediate intensity level.

Table 8-1. Truth Table for Video

LVID	LIVID	FUNCTION
L	H	NORMAL BRIGHTNESS
L	L	NORMAL BRIGHTNESS
H	L	HALF BRIGHTNESS
H	H	OFF

8-41. HORIZONTAL SWEEP AND HIGH VOLTAGE. When low Horizontal Sync (LHSYN) occurs, the falling edge triggers the single shot U1A. By adjusting the pulse width of U1A, the falling edge of the output of U1A is being delayed in triggering U1B, thus providing horizontal position control (TP3). The pulse width of U1B is fixed (TP5).

8-42. The negative output of U1B gets reinverted by U4C (a high voltage output open-collector inverter). U4C switches Q1 off and on to drive current through T1. When T1 turns Q2 on, current is drawn from the 12V supply through the primary of T2 and the other secondary of T1. Q2 drives the current through the yoke for horizontal deflection. CR4 and C4 form the rectifier/filter for the +40V supply. The +12KV supply is internally rectified by the flyback, T2, with the "aquadag" of the CRT acting as the filter. The -40V supply is rectified and filtered by CR6 and C11, aided by clamp VR1. The intensity and focus voltages are formed by voltage divider networks supplied by CR5.

8-43. When low Vertical Sync (LVSYN) occurs, it's inverted through the high voltage, open-collector output, U4A to drive the inverting input of the current mode op-amp U2B which is configured as an integrator. Variable feedback from U2A provides a means of adjusting vertical gain. The threshold detector, U2C, drives the complimentary pair, Q4 and Q5, for Vertical Sweep (TP1).

8-44. LVSYN is also used to switch Q3 on and off. Q3, C22 and blocking diode CR8 form a voltage doubler circuit to double the voltage available to U2 and the pair, Q4 and Q5, during retrace (see signal on U2P14).

Table 8-2. Mnemonics

DOTCLK	Dot Clock - 25 MHz clock for video circuitry.
HCHAR	High Character - active high, signal that is used to clock the CRT controller and the delay counters for HSYN.
HCPURQ	High CPU Request - active high, this signal along with LPCAS make LMSYN.
HDCO	High Display Counter Zero - active high, indicates least significant bit of the display address counter is logic low.
HRAS	High Display Row Address Strobe - active high, indicates display accessing RAM, used only for signature analysis troubleshooting.
HDRQ	High Data Request - active high, signal from CRT controller requesting data.
HDISP/CPU CYCLE	High Display Low CPU Cycle - this signal enables the address selectors and is used in strobing the display RAMs.
HPRAS	High BPC Row Address Strobe - active high, indicates processor accessing RAM, used only for Signature Analysis troubleshooting.
HPWE	High CPU Write Enable - active high, enables write operation either into RAM or CRT controller.
HSCLK1	High System Clock 1 - Used in arbitrator sequencer circuitry to make LCPURQ signal.
L25MHz	Low 25 MHz Clock for general purpose bus use.
LADDCLK	Low Address Clock - active low, clock signal that increments the display counters.
LBYTE	Low Byte - active low, indicates memory operation will involve only an eight bit data word; can be either the upper or lower part of the data bus.
HRC	High RAM Cycle in Process - active high, used to determine if the Display RAM is to be asserted by the CPU or the Display. Also, used by the HRAS/LCAS selector.
LCHAR	Low Character - active low, signal that synchronizes LVSYN with LHSYN.

Table 8-2. Mnemonics (Cont'd)

LCPURQ	Low CPU Request - active low, this signal is used in the arbitrator sequencer circuitry to determine if the sequence has gone to it's initial state.
LCS	Low Chip Select - active low, enables both the read and write functions for the CRT controller.
LDCAS	Low Display Column Address Strobe - active low, indicates data request from CRT controller is being serviced.
LDD	Low Disable Display - active low, this signal not used currently on enhancement bus.
LDISP/HCPU CYCLE	Low Display High CPU Cycle - this signal is used in writing to the display RAMs.
LDRQ	Low Data Request - active low. Used by Arbitrator Sequencer Circuitry to enable Address Select.
LHSYN	Low Horizontal Sync - active low, signal from display controller to Display Driver circuitry that enables the horizontal electron beam retrace function.
LIVID	Low Inverse Video - active low, signal from display controller to Display Driver circuitry that enables half-bright dot on CRT screen.
LLDCNT	Low Load Display Counter - active low, loads the first address of display memory into the display address counters.
LMSYN	Low Memory Sync - active low, indicates memory operation in process, puts microprocessor into wait state.
LPCAS	Low Processor Column Address Strobe - active low, indicates microprocessor is accessing Random Access Memory (RAM) in either read or write operation.
LRAMCLK	Low RAM Clock - 12.5 MHz RAM clock for display functions.
LRC	Low RAM Cycle in Process - active low signal used by the HRAS/ LCAS selector.
HSCLK1	High System Clock 1 - 6.25 MHz clock for CPU board.
LSTB	Low Strobe - active low, during write operation, indicates data bus information is valid; during read operation indicates microprocessor is not driving the data bus and addressed device can drive data bus.

Table 8-2. Mnemonics (Cont'd)

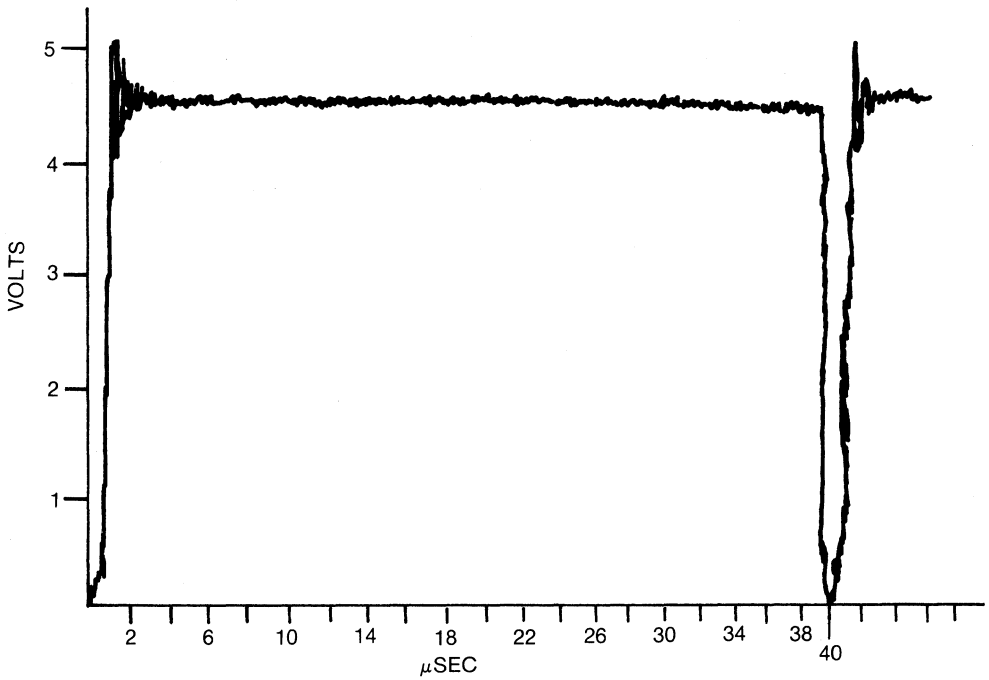
LSTM.	Low Start Memory - active low, indicates valid address bus and start of memory cycle.
LUPB.	Low Upper Byte - active low, indicates only upper eight bits of data bus involved in memory operation. When this signal is high, indicates lower eight bits being used. LUPB is gated by LBYTE.
LVID.	Low Video - active low, signal from Display Controller to Display Driver that enables full-bright dot on CRT screen.
LVSYN.	Low Vertical Sync - active low, signal from display controller to Display Driver circuitry that enables the vertical electron beam retrace function.
LWRT.	Low Write - active low, microprocessor writes to addressed device.
RCARRY.	Ripple Carry - indicates sequencer U2 has returned to initial state.

8-45. The following figure shows how the memory is sectioned by addresses.

Table 8-3. Memory Map

ADDRESS	MEMORY FUNCTION
FFFF	BASE PAGE RAM (512)
FE00	
FDFF	DISPLAY (1040)
FA18	
FA17	BLANKED DISPLAY ROW
F9F0	
F9EF	HOST RAM (15,216)
C000	
BFFF	HOST RAM (16K)
8002	
8001	DISPLAY CONTROL
8000	
7FFF	MEMORY MAPPED I/O SLOT SELECTED (16K)
4000	
3FFF	HOST ROM (16K)
0020	
001F	BPC REGISTERS (INTERNAL)
0000	

THE LOWER 32K (OUT OF 64K) IS ACCESSED AS AN EXPANDED MEMORY MODULE. THE LOWER 32K IS LOCATED ON THE DSP CONTROLLER BOARD AND IS ADDRESSED OVER THE MEMORY MAPPED I/O USING LSSEL 10.



HORIZONTAL SYNC P1,PIN 55

VERTICAL SYNC P1,PIN 56

Figure 8-1. Horizontal and Vertical Sync Waveforms

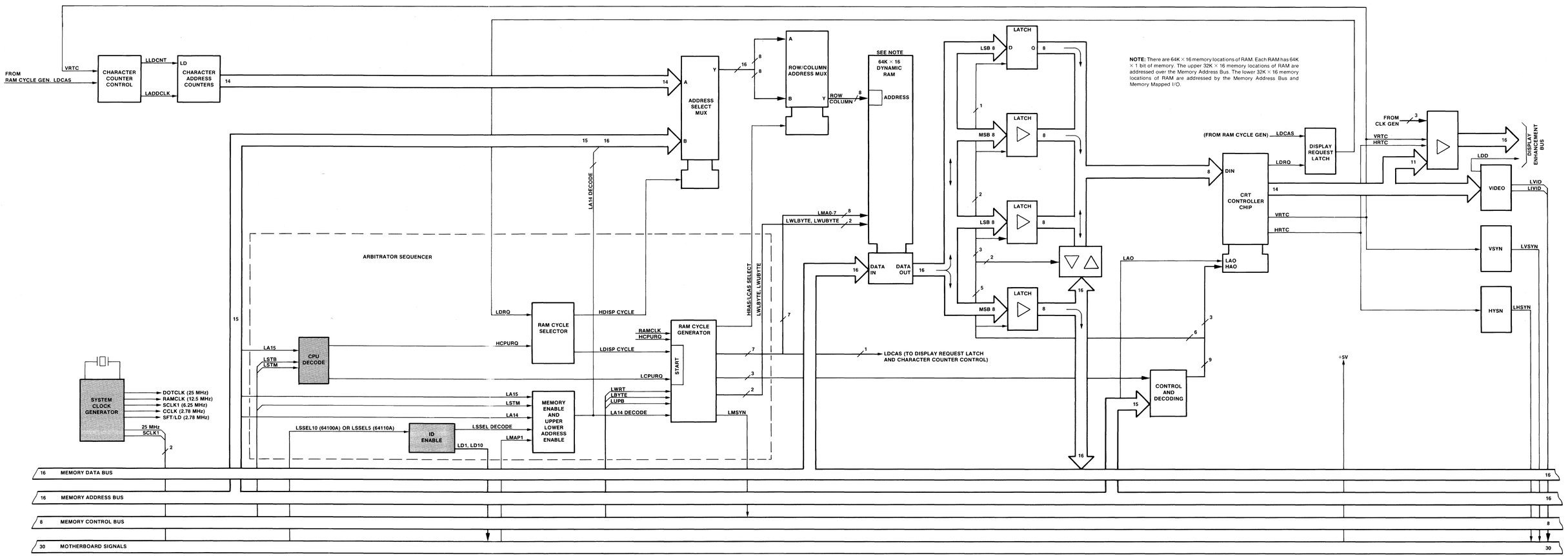


Figure 8-2.
Display Controller Block Diagram
DSP 8-12

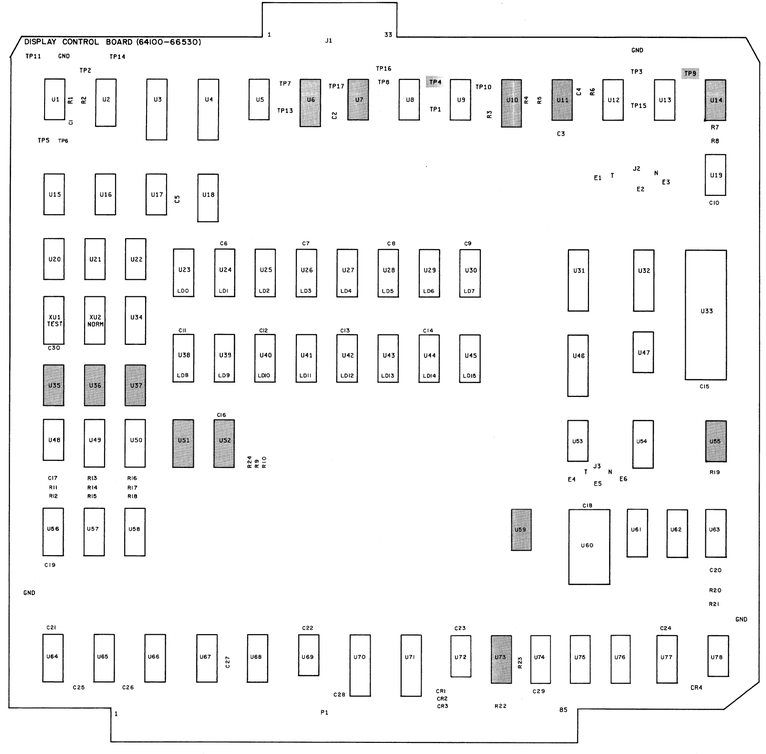
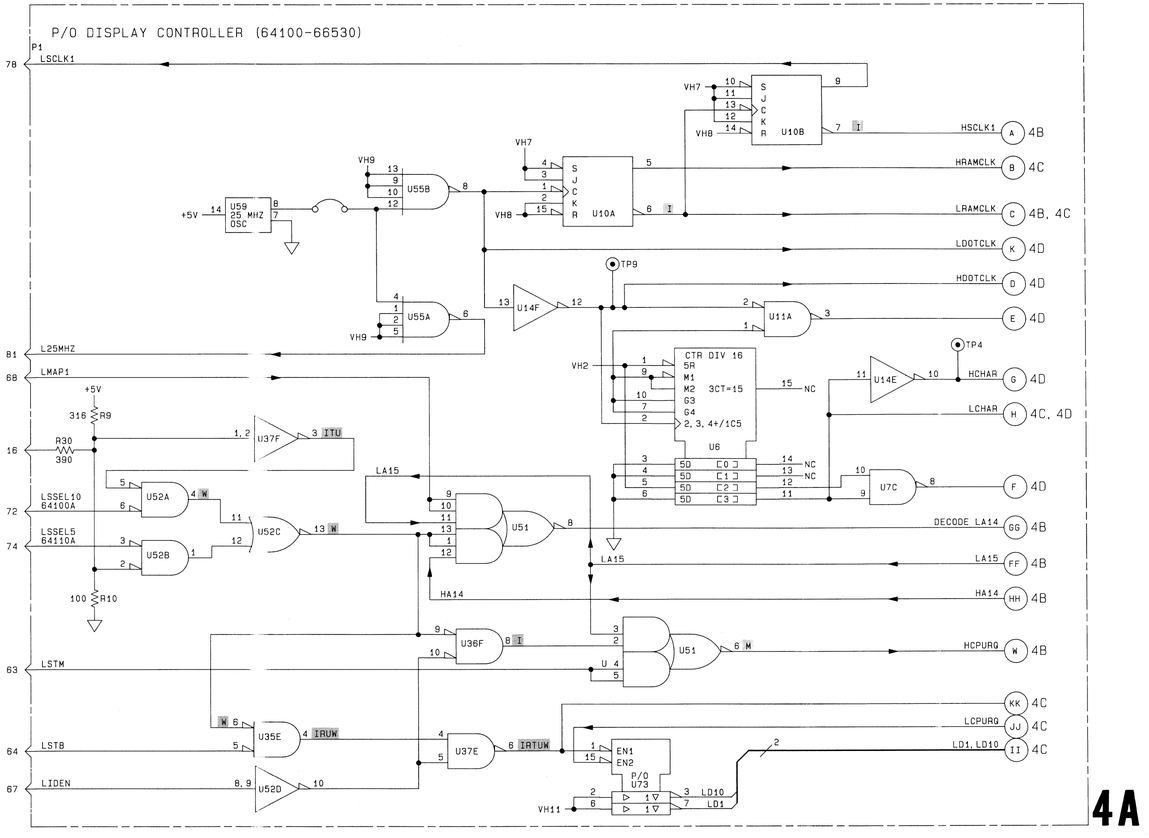


Figure 8-3. Display Controller Component Locator



ICs ON THIS SCHEMATIC

REF DES	HP PART NO.	MFR PART NO.
U6	1820-1453	74S163N
U7	1820-0681	74S00N
U10	1820-0629	74S112N
U11	1820-1449	74S32N
U14	1820-0683	74S04N
U35,52	1820-1144	74LS02N
U36	1820-1208	74LS32N
U37	1820-0681	74S00N
U51	1820-1210	GATE AND-OR
U55	1820-0697	74S140N
U59	0960-0530	OSC 25MHZ
U73	1820-1492	BFR INV HEX

PARTS ON THIS SCHEMATIC

P1
TP4,9
U6,7,10,11,14,35-37,51,
U52,55,59,73

IC POWER CONFIGURATION

```
        14 |
+5V -------| U7,11,14,35-37,
           |
           | U51,52
         7 |
GND -------|
           |_____________

        16 |
+5V -------|
           |
           |   U6,10
           |
         8 |
GND -------|
           |_____________
```

Figure 8-4.
Display Controller Schematic (Sheet 1 of 4)
DSP 8-13

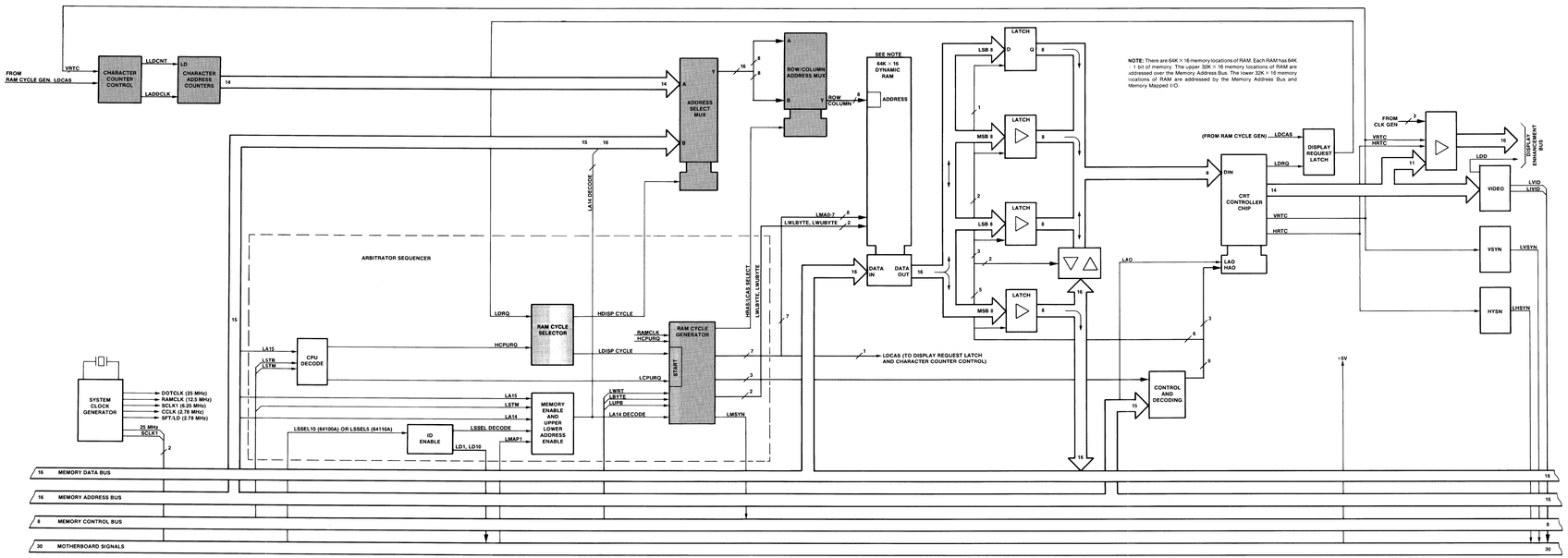


Figure 8-2. Display Controller Block Diagram

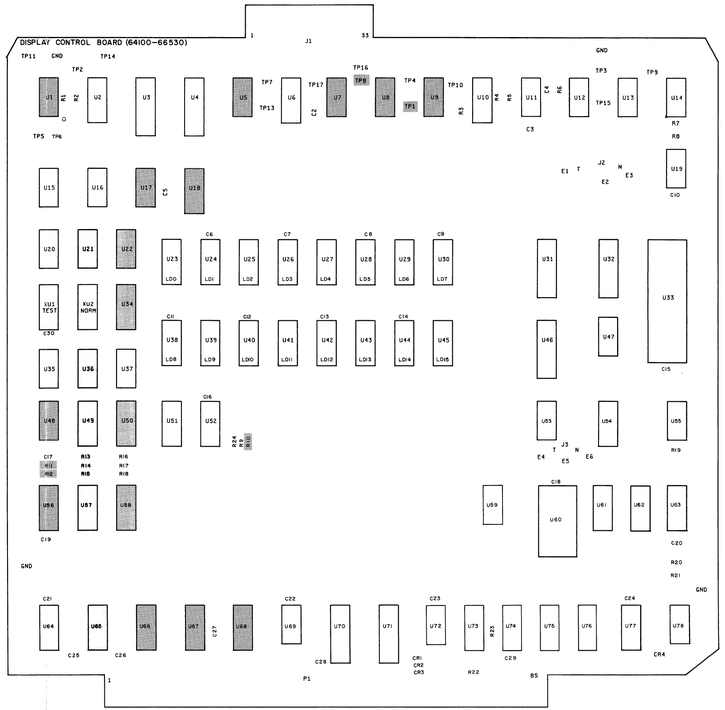
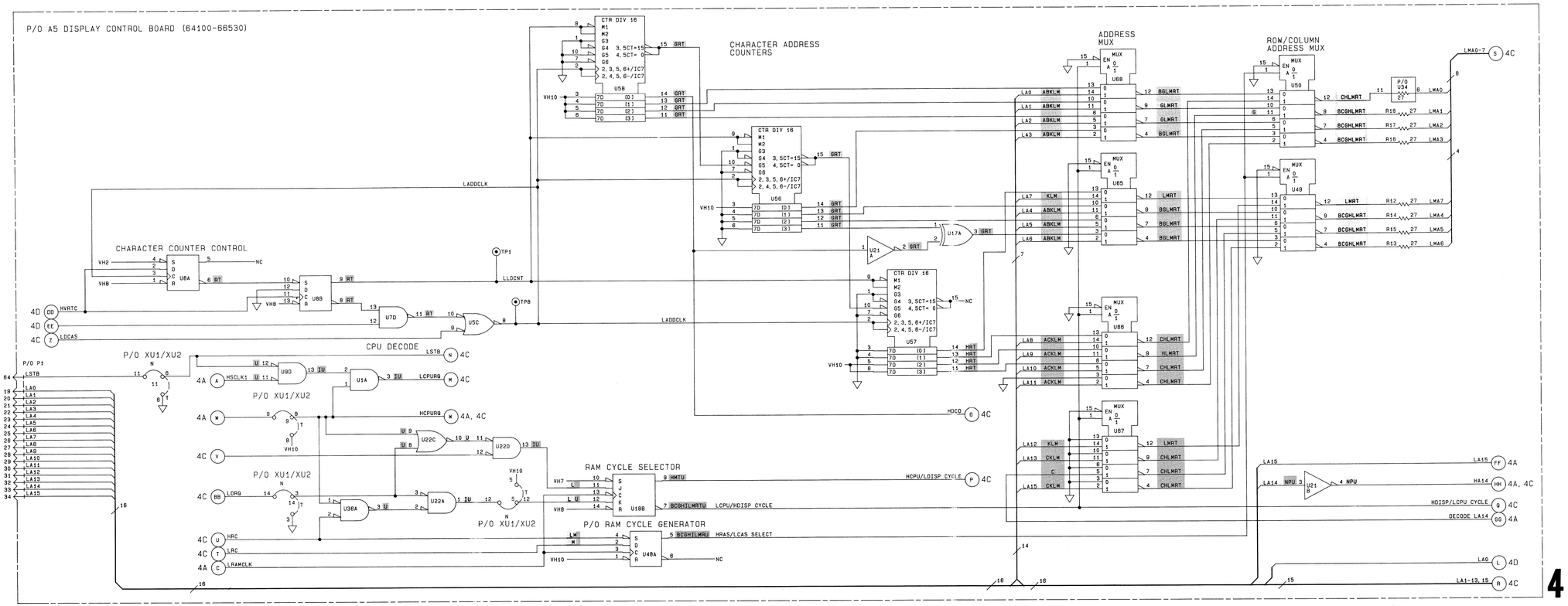


Figure 8-3. Display Controller Component Locator



ICs ON THIS SCHEMATIC

REF DES	HP PART NO.	MFR PART NO.
U1,7	1820-0681	74S00N
U5	1820-1201	74LS08N
U8	1820-1112	74LS74N
U9,22	1820-1322	74S02N
U17	1820-1211	74LS86N
U18	1820-0629	74S112N
U21	1820-0683	74S04N
U34	1810-0536	NETWORK 27 OHM
U36	1820-1208	74LS32N
U48	1820-0693	74S74N
U49,50	1820-1015	74S158N
U56-58	1820-1435	74LS669N
U65-68	1820-1425	74LS158N

PARTS ON THIS SCHEMATIC

P4
R10-15
TP1,8
U1,5,7-9,17,18,21,22,34
U36,48-50,56-58,65-68

IC POWER CONFIGURATION

14 | +5V ----- | U1,5,7-9,17,18,
| U21,22,48
7 | GND -----

16 | +5V ----- | U34,36,49,50,
8 | GND ----- | U56-58,65-68

Figure 8-4.
Display Controller Schematic (Sheet 2 of 4)
DSP 8-15

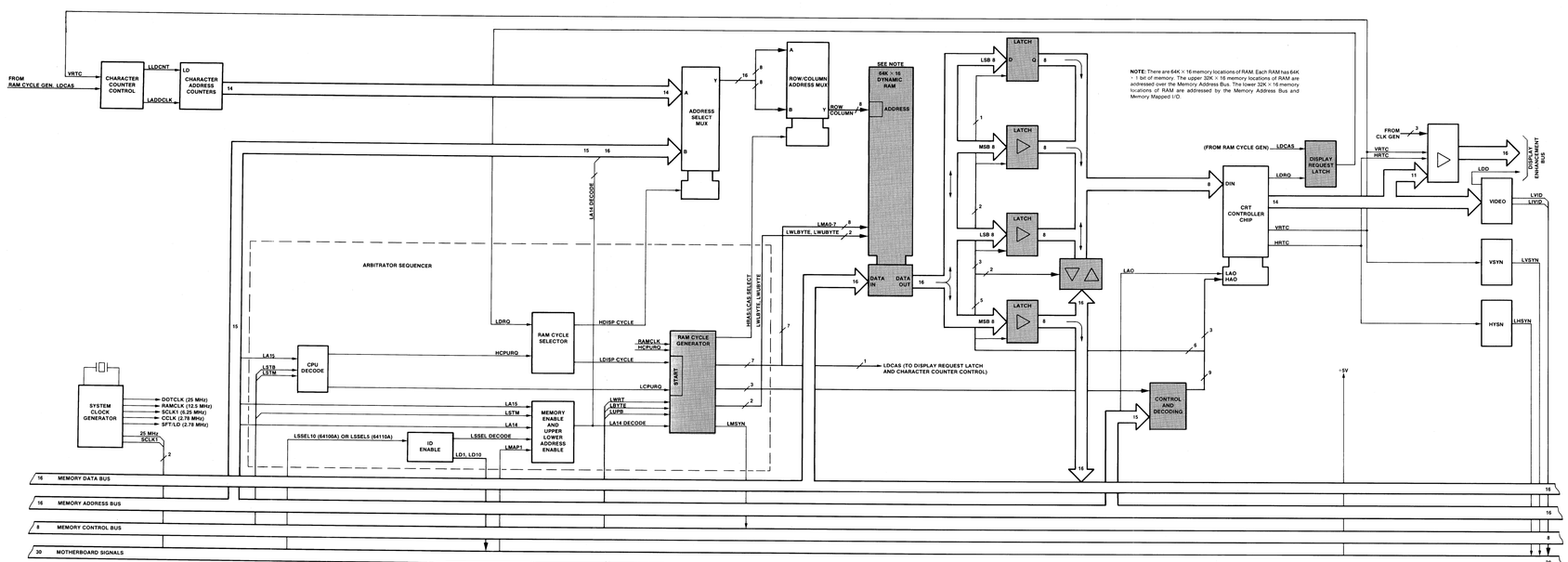


Figure 8-2. Display Controller Block Diagram

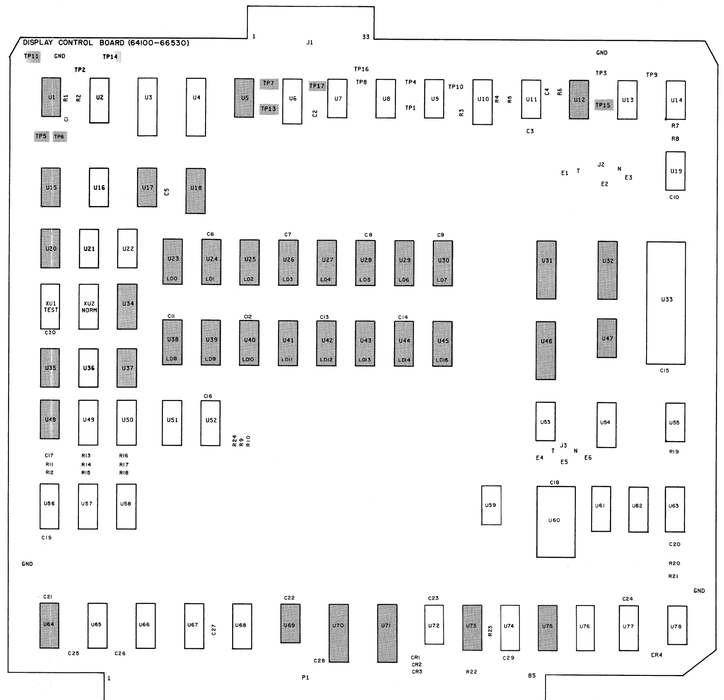
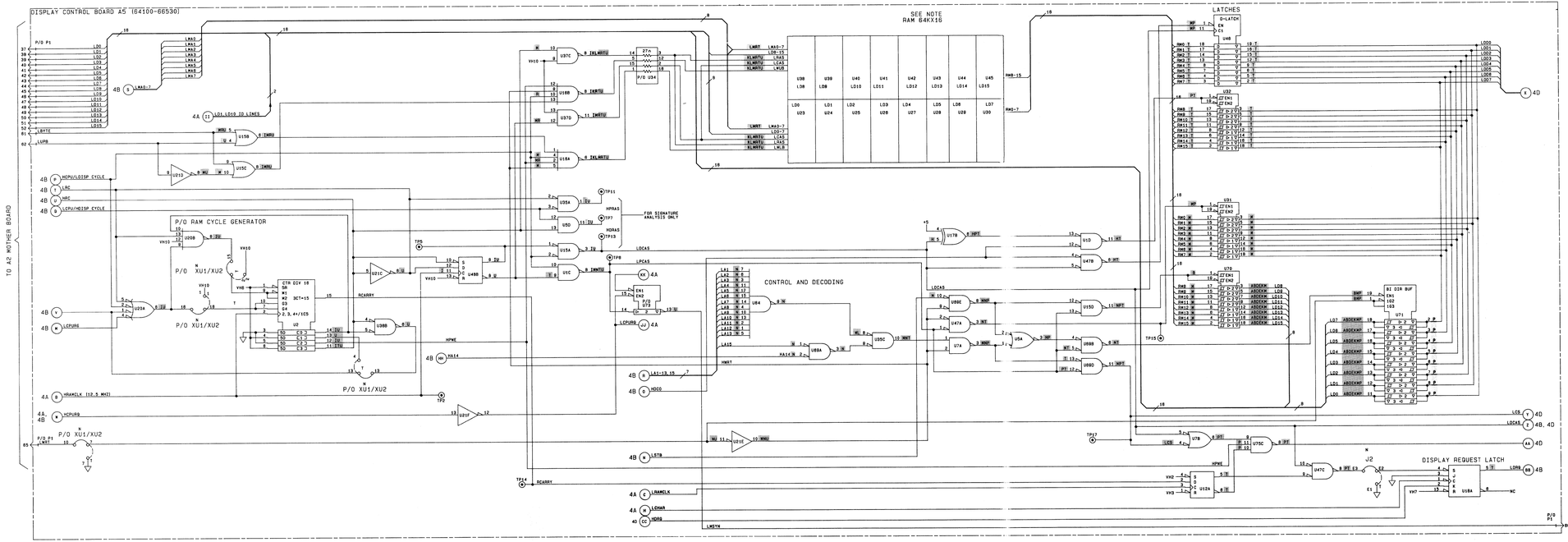
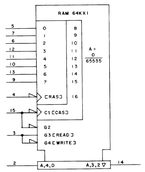


Figure 8-3. Display Controller Component Locator



NOTE



ICs ON THIS SCHEMATIC

REF DES	HP PART NO.	MFR PART NO.
U1,37	1820-0681	74S00N
U2	1820-1453	74S163
U5	1820-1201	74LS08N
U12,48	1820-0693	74S74N
U15,36,47,69	1820-1208	74LS32N
U16,20	1820-0688	74S20N
U17	1820-1211	74LS86N
U18	1820-0629	74S112N
U21	1820-0683	74S04N
U23-30,38-45	1818-3005	64K X 1 RAM
U31,32,70	1820-2024	74LS244N
U34	1810-0536	NETWORK 27 OHM
U35	1820-1144	74LS02N
U46	1820-1997	74LS374N
U64	1820-1130	74S133N
U71	1820-2075	74LS245N
U73	1820-1492	BFR HEX 1-INP
U75	1820-0685	74S10N

PARTS ON THIS SCHEMATIC

TP2,5,-7,11,13-15,17
U1,2,5,12,15-18,20,21,
U23-30,31,32,34-48,64,
U69,70,71,73,74

IC POWER CONFIGURATION

14		16	
+5V	U1,5,7,12,	+5V	
	U15-17,20,21,		U2,18,64
7		8	
GND	U35-37,48,69	GND	

8		20	
+5V	U23-30,	+5V	
	U38-45		U31,32,42,71
16		10	
GND		GND	

Figure 8-4.
Display Controller Schematic (Sheet 3 of 4)
DSP 8-17

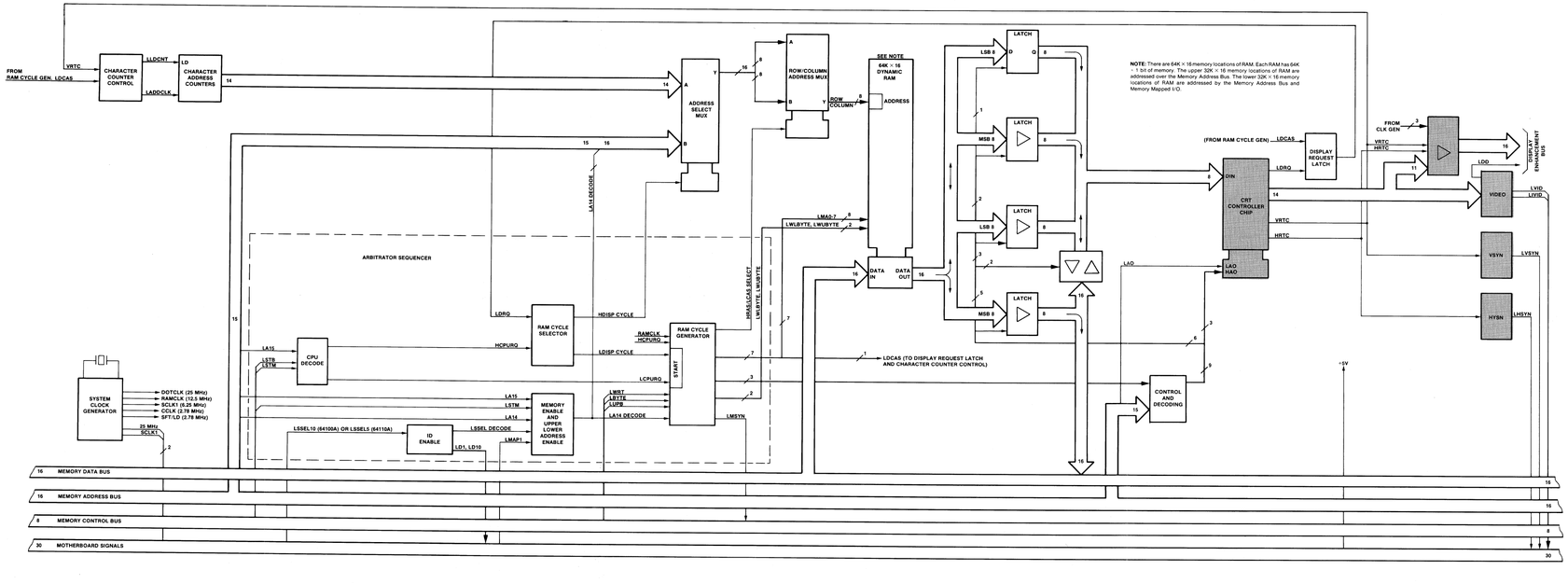


Figure 8-2. Display Controller Block Diagram

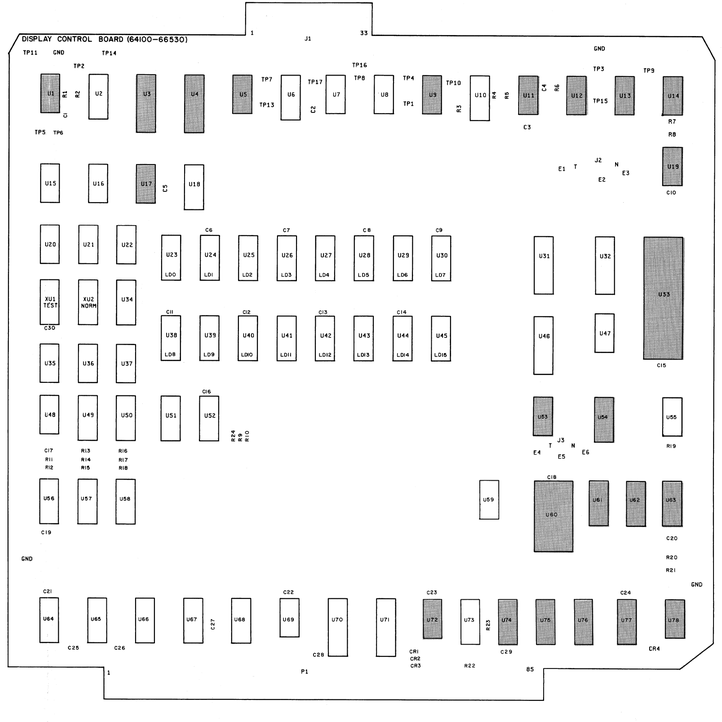
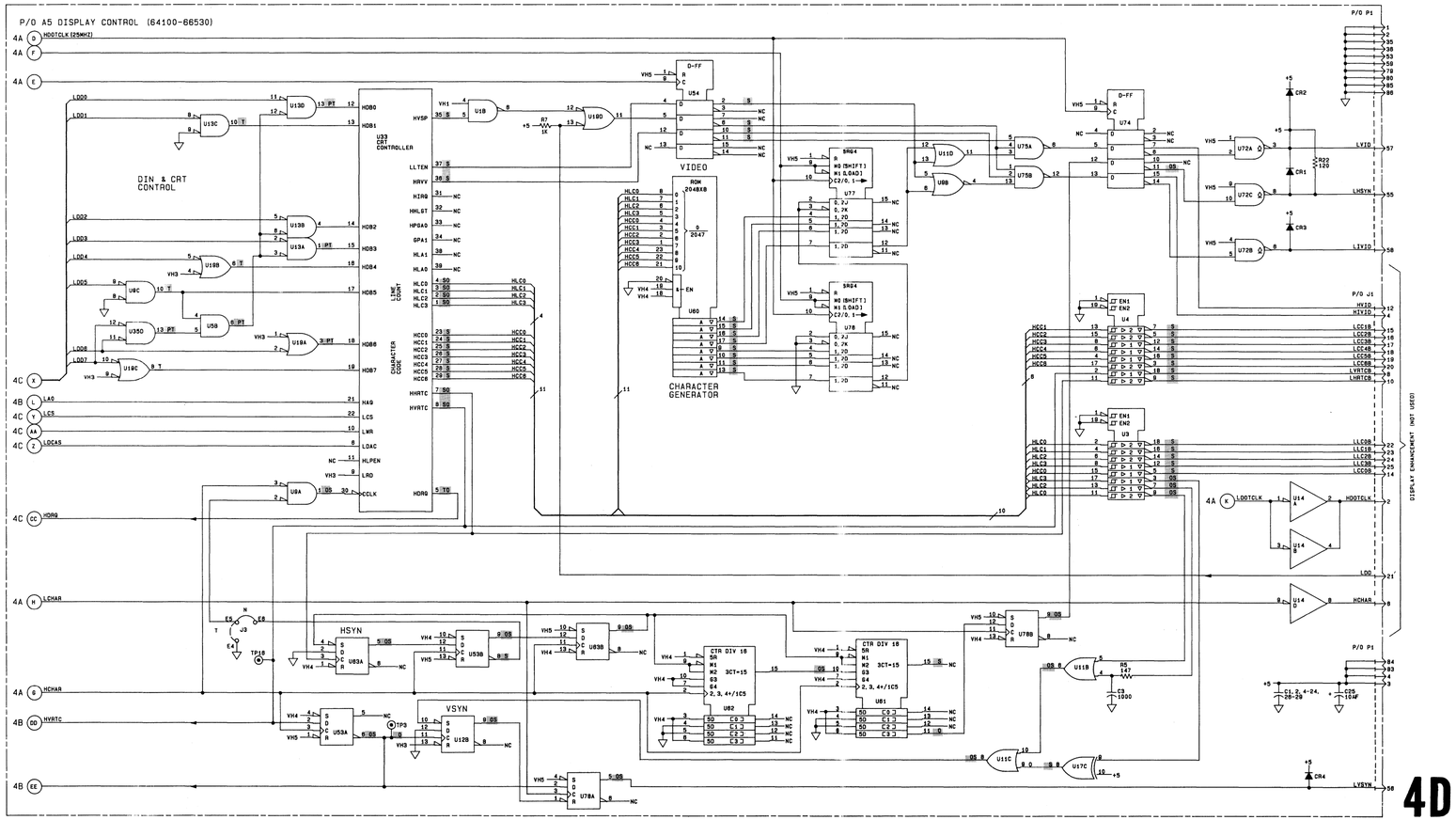


Figure 8-3. Display Controller Component Locator



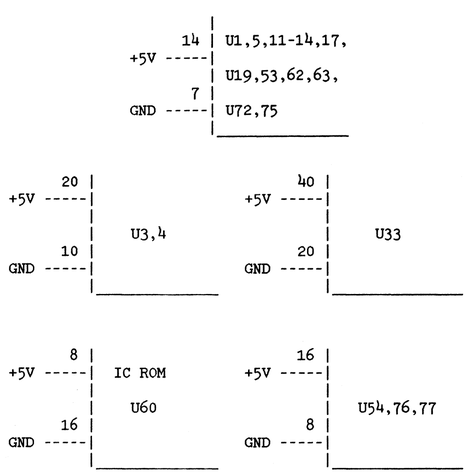
ICs ON THIS SCHEMATIC

REF DES	HP PART NO.	MFR PART NO.
U1	1820-0681	74S00N
U3,4	1820-1917	74LS240N
U5	1820-1201	74LS08N
U9	1820-1322	74S02N
U11	1820-1449	74S32N
U12,78	1820-0693	74S74N
U13	1820-1144	74LS02N
U14	1820-0683	74S04N
U17	1820-1211	74LS86N
U19	1820-1197	74LS00N
U33	1820-2191	C8275
U53,63	1820-1112	74LS74N
U54,74	1820-1191	74S175N
U60	1816-1496	IC ROM
U61,62	1820-1432	74LS163N
U72	1820-1451	74S38N
U75	1820-0685	74S10N
U76,77	1820-1303	74S195N

PARTS ON THIS SCHEMATIC

CR1-3
L1
P3
R1-9,16-18,22
TP3,16
U1,3,4,5,9,11-14,17,19
U33,53,54,60-63,72,74-78

IC POWER CONFIGURATION



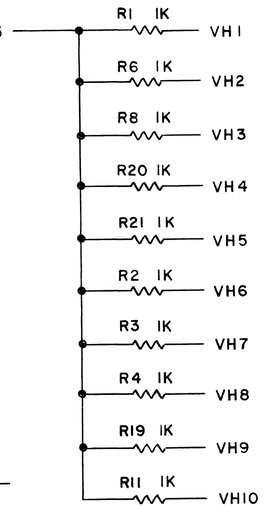


Figure 8-4.
Display Controller Schematic (Sheet 4 of 4)
DSP 8-19/(8-20 blank)

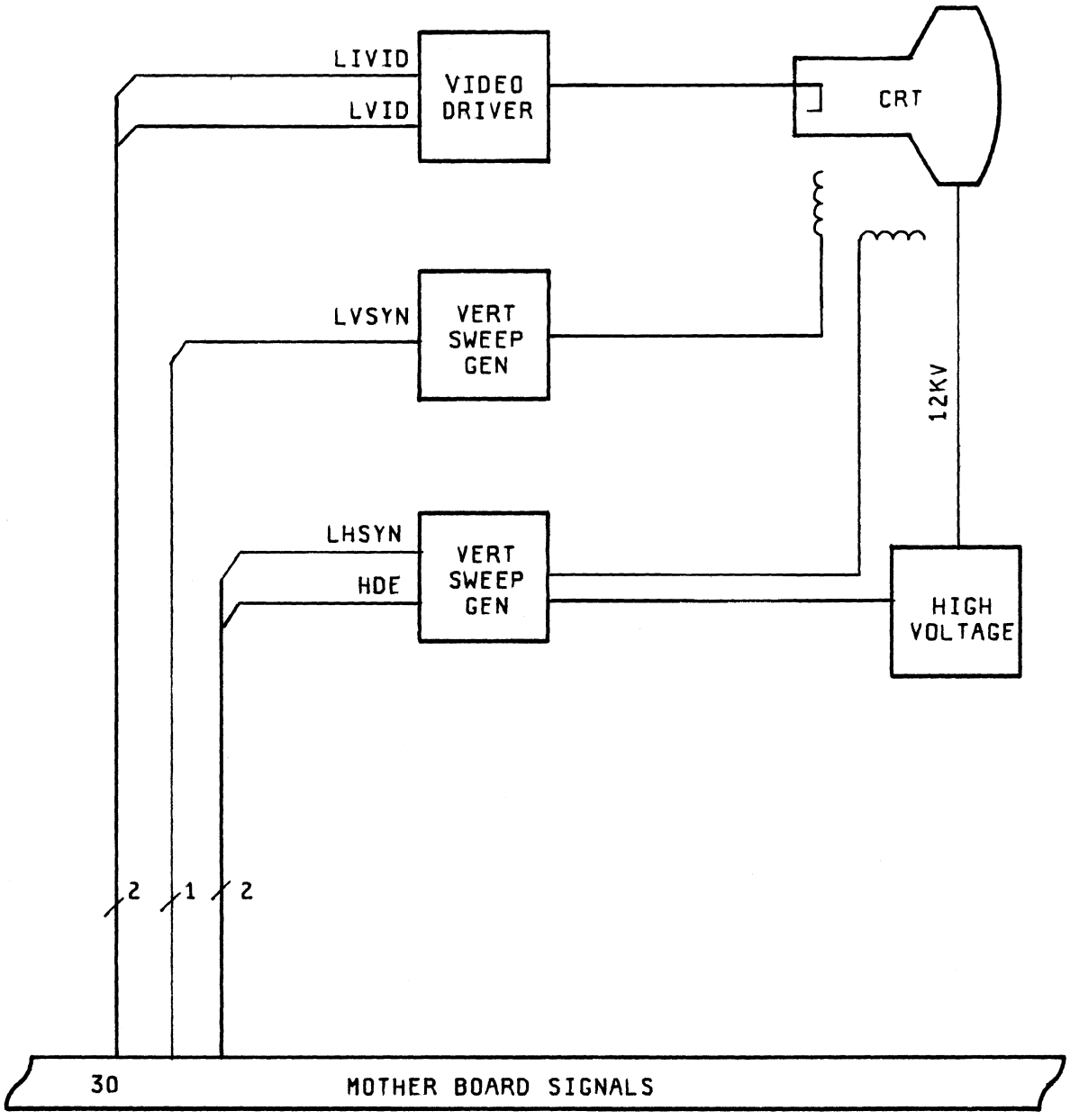


Figure 8-5. Display Driver Block Diagram

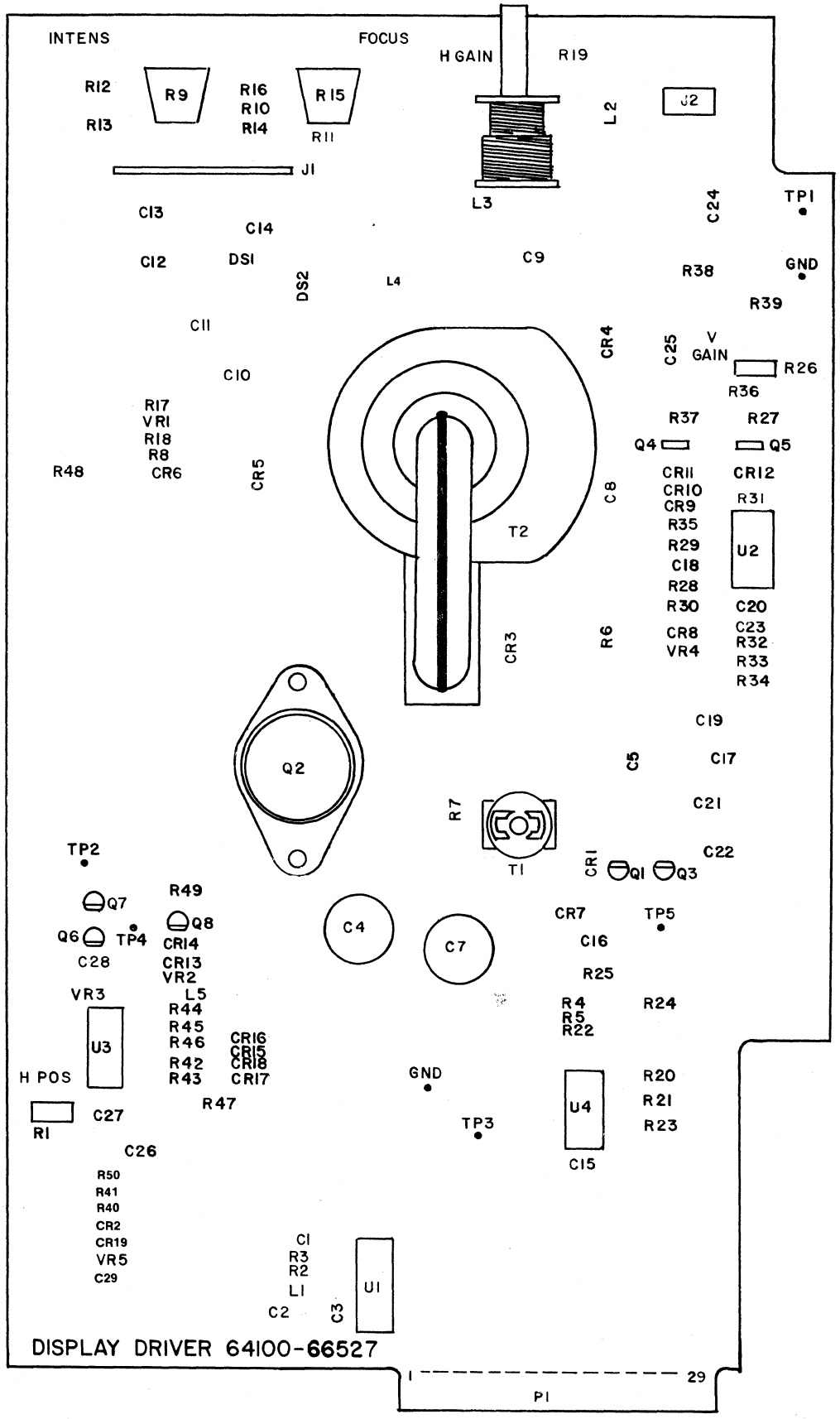


Figure 8-6. A7 Display Driver Component Locator

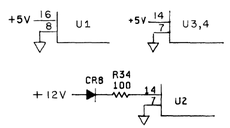
ICS ON THIS SCHEMATIC

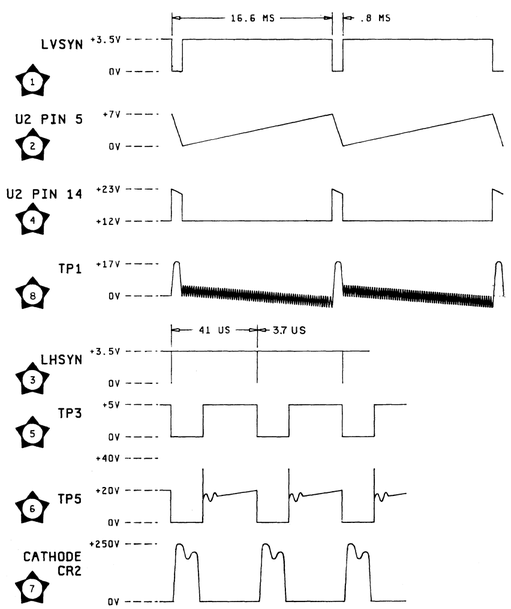
REF. DES.	HP PART NO.	MFG PART NO.
U1	1820-1437	74LS221
U2	1826-0120	LM3900
U3	1820-1451	74S38
U4	1820-0471	7406

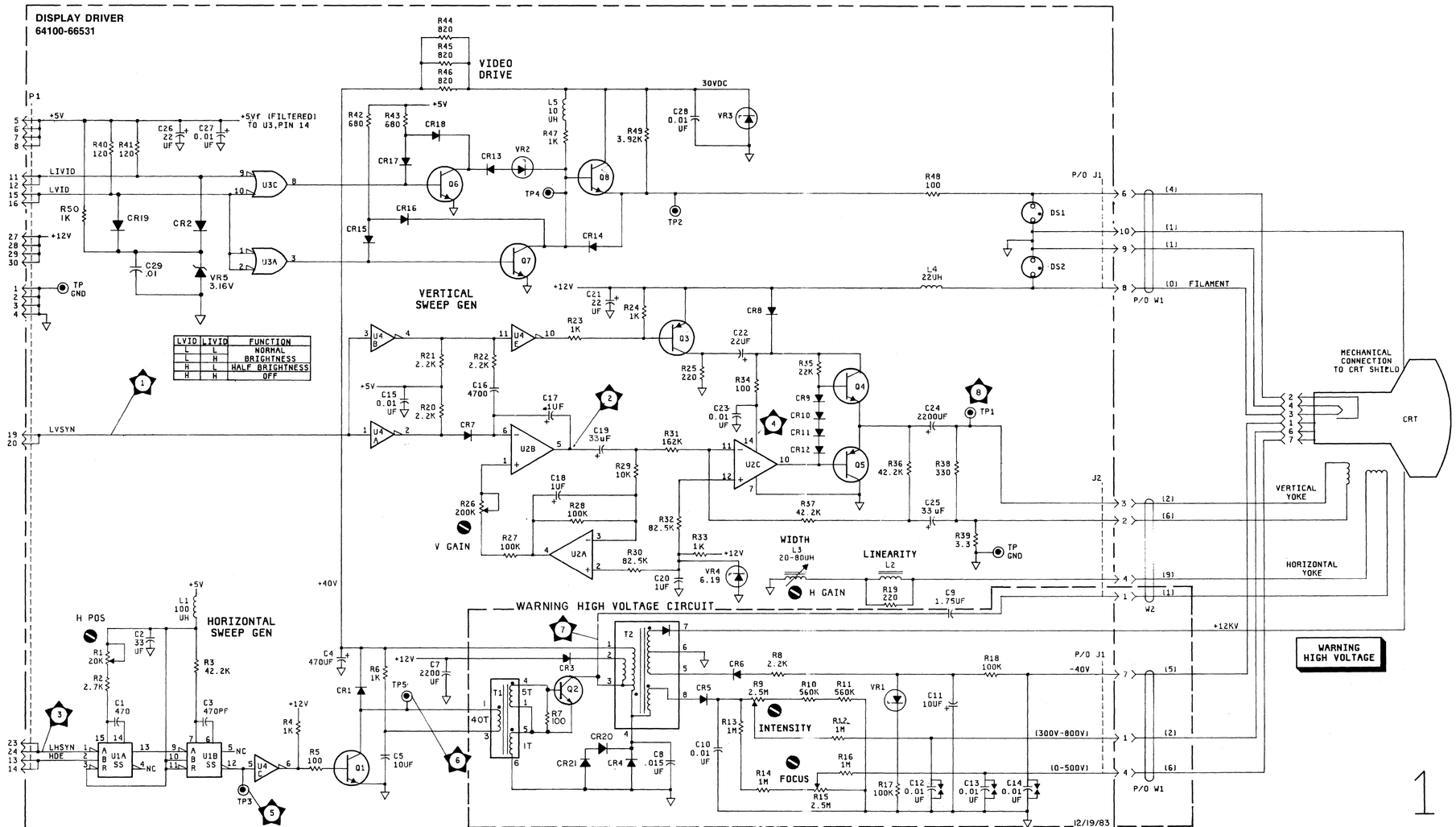
PARTS INCLUDED ON THIS SCHEMATIC

REF. DES.	HP PART NO.
CRT	2090-0042
W1(CRT CABLE)	64100-61603

IC POWER SUPPLY CONFIGURATIONS







LVID	LVID	FUNCTION
L	L	NORMAL BRIGHTNESS
L	H	HALF BRIGHTNESS
H	L	OFF
H	H	

1

Figure 8-7.
Display Driver Schematic
DSP 8-23/(8-24 blank)

SERVICE MANUAL

MODEL 64100A

INPUT OUTPUT/FUNCTIONS

Manual Part No.: Part of Mainframe Manual
Microfiche Part No.: See Mainframe Manual

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LIST OF TABLES (Cont'd)

LIST OF ILLUSTRATIONS

SECTION I

GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. This Chapter contains the physical description, troubleshooting and theory-of-operation for the Input/Output, Rear-panel, and the Keyboard PC boards.

1-3. The I/O, Rear-panel, and Keyboard PC boards comprise part of the set of mandatory circuit boards that are required for operation of the basic 64000 Logic Development Station. This means that all of these boards, (plus the CPU, Display Control and Display Driver PCB's), must be installed in every 64100A Mainframe before operation is possible.

1-4. PURPOSE.

1-5. The I/O, Rear-panel, and Keyboard PC boards contain circuits required by the Mainframe CPU board to: (1) process data and instructions sent to and received from remote peripheral equipment (e.g., disc drives, printers, modems, etc.) via various buses, (2) process interrupts from remote peripherals and internal (Mainframe) circuits, (3) decode card select signals, (4) decode Keyboard status signals, and (5) generate a beeper tone when certain events occur. In addition, the I/O and Rear-panel boards contain many of the switches that allow the operator to select the system mode of operation (see Section III).

1-6. Table 1-1 lists the power supply current loads for the I/O, Rear Panel and Keyboard PC boards.

Table 1-1. Power Supply Current Loading

PC BOARD	+12V Supply	+5V Supply	-5V & -3V Supply
I/O	0.164 Amps	0.708 Amps	
Rear panel		0.714 "	
Keyboard		0.239 "	

SECTION II

INSTALLATION AND REMOVAL

2-1. REMOVING THE I/O PC BOARD.

a. Shut off system power.

b. Remove the 50-pin I/O ribbon cable and the 50-pin Rear-panel ribbon cable.

c. Pull up on the two extractor levers until the board can be lifted from the Motherboard slot.

2-2. REMOVING THE REAR-PANEL PC BOARD.

a. Remove the 50-pin ribbon cable from the I/O PCB to the Rear-Panel PCB.

b. Remove two studs holding System Bus connector (J1 on Rear-Panel).

c. Remove two studs holding each RS232C connector (J2 and J4 on Rear-Panel).

d. Remove four screws holding Rear-Panel PCB to rear of Mainframe.

2-3. REMOVING THE KEYBOARD PC BOARD.

a. Tilt front panel bezel forward and disconnect keyboard ribbon cable from Motherboard connector J15.

b. Remove PROM Programmer Module and remove two screws securing Keyboard Assembly to Mainframe.

c. Carefully stand mainframe on the Rear-panel and remove the bottom cover.

d. Remove the six screws holding the Keyboard PCB to the Mainframe.

2-4. INSTALLING THE I/O PC BOARD.

2-5. To install the I/O PC board, perform the removal steps in reverse order being careful that the board is properly aligned with the Motherboard connector before seating the board. Be sure that the component-side of the PC board is facing the front of the Mainframe.

CAUTION

The I/O PC board is ALWAYS installed in the forward-most slot in the Mainframe card cage (identified as the "I/O" slot on the slot identification label).

2-6. INSTALLING REAR-PANEL AND KEYBOARD PCB'S.

2-7. To re-install the Rear-Panel and Keyboard PCB's, perform the removal steps in reverse order.

SECTION III

OPERATION

3-1. INTRODUCTION.

3-2. There are no special handling instructions for these PC boards. The only operating instructions concern defining the function of the various mode control switches on the I/O and Rear-panel PC boards. The functions of these switches are defined for the I/O and Rear-panel PC boards in tables 3-1 and 3-2 respectively. Refer to Section VIII of this manual for more information about their use.

Table 3-1. I/O PCB Switch Functions

SWITCH	NAME	FUNCTION
S1	20 MA/60 MA	Selects appropriate current level of 20 mA or 60 mA for peripherals such as a teletype (TTY).
S2	INT/EXT Clock	Selects either internal or external clock source for asynchronous operations. The internal clock frequency is determined by the baud rate dip switch S5 on the I/O PCB.
S3	CUR LOOP/RS-232	Selects current loop or RS-232 operation modes. In the current loop operation, a logic 1 is 20 mA/ 60 mA while a logic 0 is 0 mA. In the RS-232 operation, a logic 1 is any voltage between -3 and -25 volts while a logic 0 is any voltage between +3 and +25 volts.
S4	RS-232 MODE	Controls the parameters of the RS-232 mode by the position of the 8 bit dip switch S4. Bits 1 and bit 2 set the number of stop bits. Bit 3 sets the Even/Odd Parity line. Bit 4 sets the Parity Enable. Bits 5 and 6 set the Character Length.

S4 (cont'd)		Bit 7 sets the baud rate factor (X1 or X16) which will configure the USART chip via the CPU to recieve transmission at a faster rate. This will give the CPU more time to perform other functions (see the 64100A operating manual). Bit 8 sets the terminal as either a Modem or Terminal.
S5	BAUD RATE	Is a 5 bit dip switch that controls the Baud rate and Duplex mode. Bit 1 sets the terminal in the Full or Half Duplex. The other four switches set the Baud rate from 50 to 19200 in 16 steps.

NOTE: Refer to figure 3-1 for more information on the location and function of the I/O PCB dip switches S1 - S5.

Table 3-2. Rear-Panel Switch Functions

SWITCH	NAME	FUNCTION
S2 & S3	SYSTEM BUS	S2 and S3 are both 8 bit dip switches which control the mainframe as a controller or as a non-controller (see the 64100A operating manual for description of how to set S2 and S3).
S1	CONTROL SOURCE	S1 is a 7 bit dip switch which controls the boot-up source and the mainframe's address. Bits 1 - 5 select the mainframe addresses. There are 32 addresses available, but only up to 6 mainframes are allowed on the the system bus. Bits 6 and 7 are Boot-up source addresses (System Bus, Local Mass Storage, etc.).

NOTE: Refer to figure 3-2 for more information on the locations and functions of Rear-panel dip switches S1 - S3.

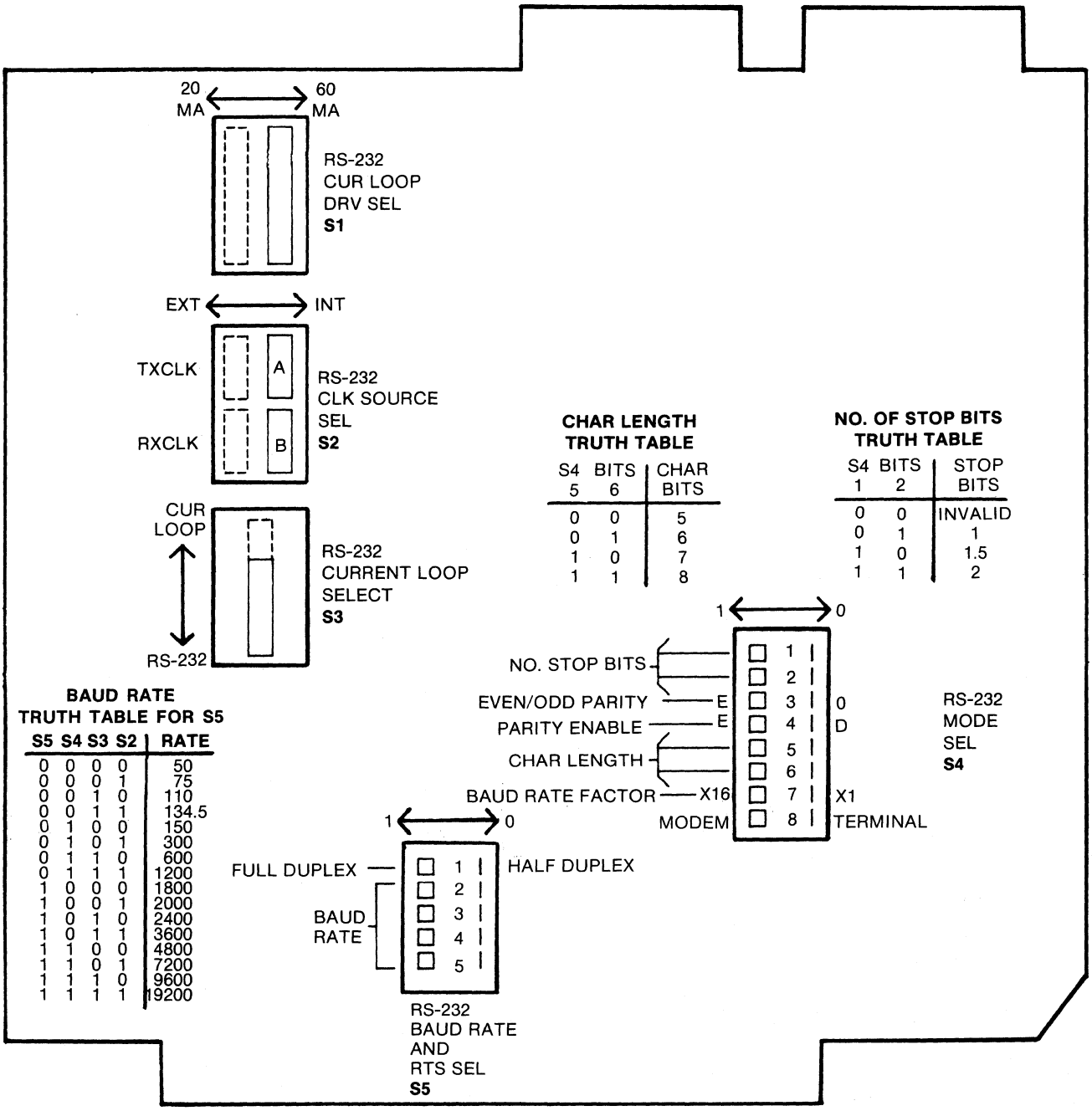
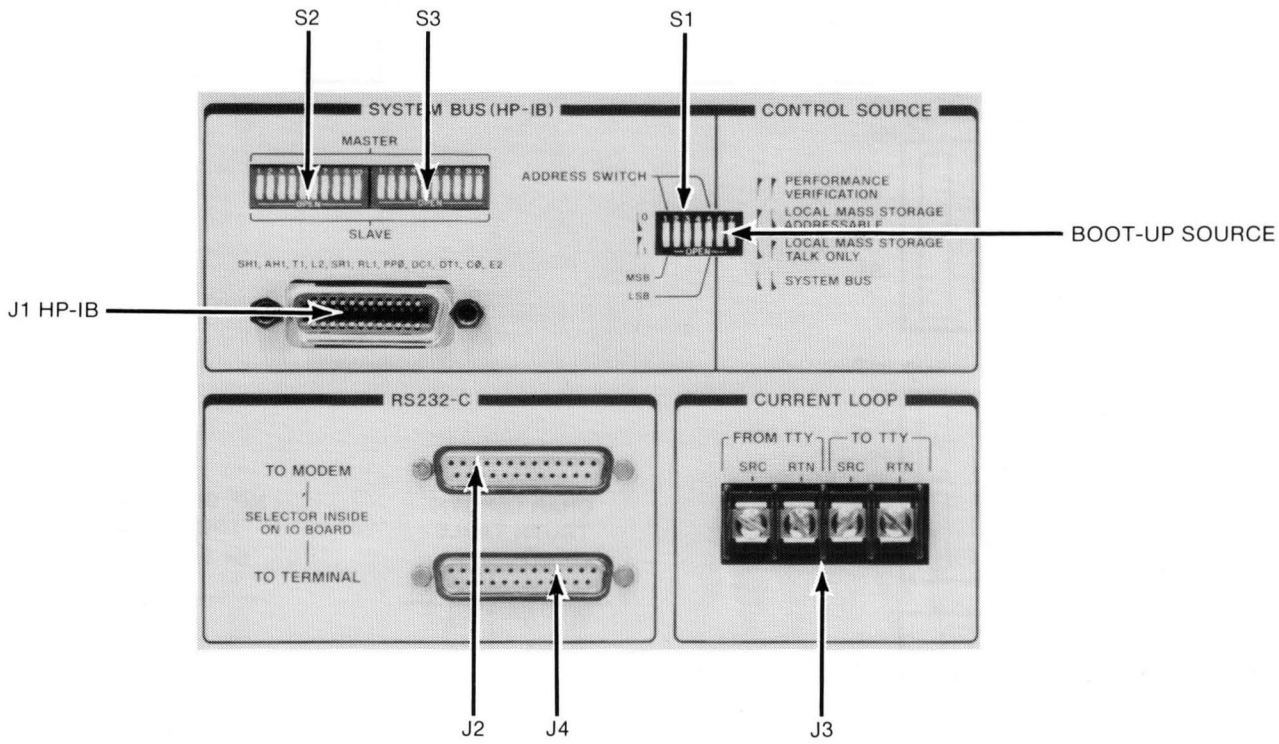


Figure 3-1. I/O PCB Switch Locations and Functions



BOOT-UP SOURCE ADDRESSES

MSB	LSB	CONTROL
0	0	SYS BUS (DISC)
0	1	LOCAL MASS STORAGE TALK ONLY
1	0	LOCAL MASS STORAGE ADDRESSABLE
1	1	PERFORMANCE VERIFICATION

MAINFRAME ADDRESSES

NOT USED	MSB		LSB	ADDRESS	
00	0	0	0	0	NOT VALID
00	0	0	1	1	
00	0	1	0	2	VALID MAINFRAME ADDRESSES
00	0	1	1	3	
00	1	0	0	4	
00	1	0	1	5	
00	1	1	0	6	
00	1	1	1	7	

Figure 3-2. Rear-Panel Switch Locations and Functions

SECTION IV

PERFORMANCE VERIFICATION

4-1. PV THEORY.

4-2. The following paragraphs briefly describe the I/O circuits that are being exercised by the various I/O PV tests.

NOTE

Refer to section IV of the Mainframe tab for an explanation of PV initiation.

4-3. I/O WRITE TEST PROCEDURE.

Purpose:

This test provides audible feedback that the test is executing by beeping, and provides the following SA stimulus. The I/O WRITE TEST increments the PHI chip register addresses, accessess the interrupt masks, cycles the slot select lines, and stimulates the four Rear-panel BNC connectors. Use SA loops A and B for trouble isolation.

Area Tested:

This test is not of the pass/fail type. It provides stimulus signature analysis for the following cicuitry: Option slot select lines on the Motherboard, all connections from option slots to the Rear-panel BNC connectors, the beeper circuitry, PHI register address latch, all LMAP lines, and the interrupt mask circuitry.

Operation:

a. This test will not display a failure. The main purpose of the test is for signature analysis (SA).

b. The only noticeable failure will be the loss of the audible beeper.

4-4. I/O READ TEST PROCEDURE.

Purpose:

This test checks the Rear-panel switches, the hardware configuration jumpers, the RS-232 switch settings, and the master controller and non controller configuration and displays the information on the screen. If the information differs from the switch settings then use SA loop C for trouble isolation.

Area Tested:

Rear panel dipswitches, the cable to the Rear-panel, I/O circuitry, and the RS-232 dipswitches.

Operation:

a. Upon initiation of the I/O READ TEST, the PV menu displays the following in inverse video:

I/O READ TEST: ADDR=XX BOOT=XX M=X RS-232=XXXXXXXX HC=XX

ADDR=XX is the HPIB address (0-1F) as set by the Rear-panel switches.

BOOT=XX is the boot source set by the Rear-panel switches as follows:

Bit 1	Bit 0	Control Source
0	0	System Bus
0	1	Local Mass Storage Talk only
1	0	Local Mass Storage Addressable
1	1	Performance Verification

M=X X=1 for CONTROLLER (MASTER)
X=0 for NON-CONTROLLER (SLAVE)

RS232=XXXXXXXX Read from S4 on the I/O board.
Bit 76543210

Bit 0 Term/Modem 0= Terminal 1= Modem

Bit 1 Baud rate X1/X16

Bit 2 Word Length
Bit 3 Word Length

Bit 3	Bit 2	Word Length
0	0	5
0	1	6
1	0	7
1	1	8

Bit 4 Parity Enable 0= Parity Disabled
1= Parity Enabled

Bit 5 Parity Odd/Even 0= Odd Parity
1= Even Parity

Bit 6 Number of stop bits
Bit 7 Number of stop bits

Bit 7	Bit 6	# of Stop Bits
0	0	INVALID
0	1	1
1	0	1.5
1	1	2

HC=XX The hexidecimal representation of the six hardware jumpers. HC is not used for this test.

b. Use SA loop C for trouble isolation.

4-5. TIME INTERRUPT TEST PROCEDURE.

Purpose:

The TIME INTERRUPT TEST checks the operation of the 50 to 60 Hz line sync to the CPU via the delta time interrupt circuitry.

Area Tested:

The LINE SYNC a 50 to 60 Hz signal from the power supply, the delta time interrupt circuitry on the I/O board, and interrupts to the CPU.

Operation:

a. Upon initiation, the PV test counts and displays line sync interrupts to the CPU. The display will show the amount tests that have passed or failed.

NOTE

Since LINE SYNC is asynchronous with the CPU timing, SA cannot be used for troubleshooting. The circuit functions must be verified by checking the I/O "Write" and "Read" SA's (Loops A, B and C) and by using a scope or logic probe to confirm operation of other IC circuits.

4-6. KEYBOARD TEST PROCEDURE.

Purpose:

The KEYBOARD TEST checks for keyboard switch closure and keyboard decoding. Use SA loop F for trouble isolation.

Area Tested:

All 77 keyswitches, keyboard decoding electronics, keyboard cable, and the keyboard RAM/state machine.

Operation:

a. When initiated, the KEYBOARD TEST instructs the user to press all of the keyboard keys in a left-to-right top-to-bottom sequence.

b. The sequence begins with the left-most softkey and includes all display and cursor control keys.

c. The keyboard test requires this specific sequence. Furthermore, even if all keyswitches and the decoding circuitry are working, a key that is pressed out of sequence will cause a "FAILED TEST" message and end the test.

d. The order in which the keys are pressed is given on figure 4-1.

e. There is a second test that involves observing if the correct character is displayed on the CRT each time a key is depressed while the system is in the PV mode. This latter test can be observed any time during PV and is useful for checking intermittent operation of the keyboard.

f. Note the keyboard test is skipped while PV is in the cycle mode.

NOTE

Neither of the above tests is useful if the keyboard is completely dead since the keyboard must be working so that you can press NEXT TEST in the Display Pattern to get to the above tests.

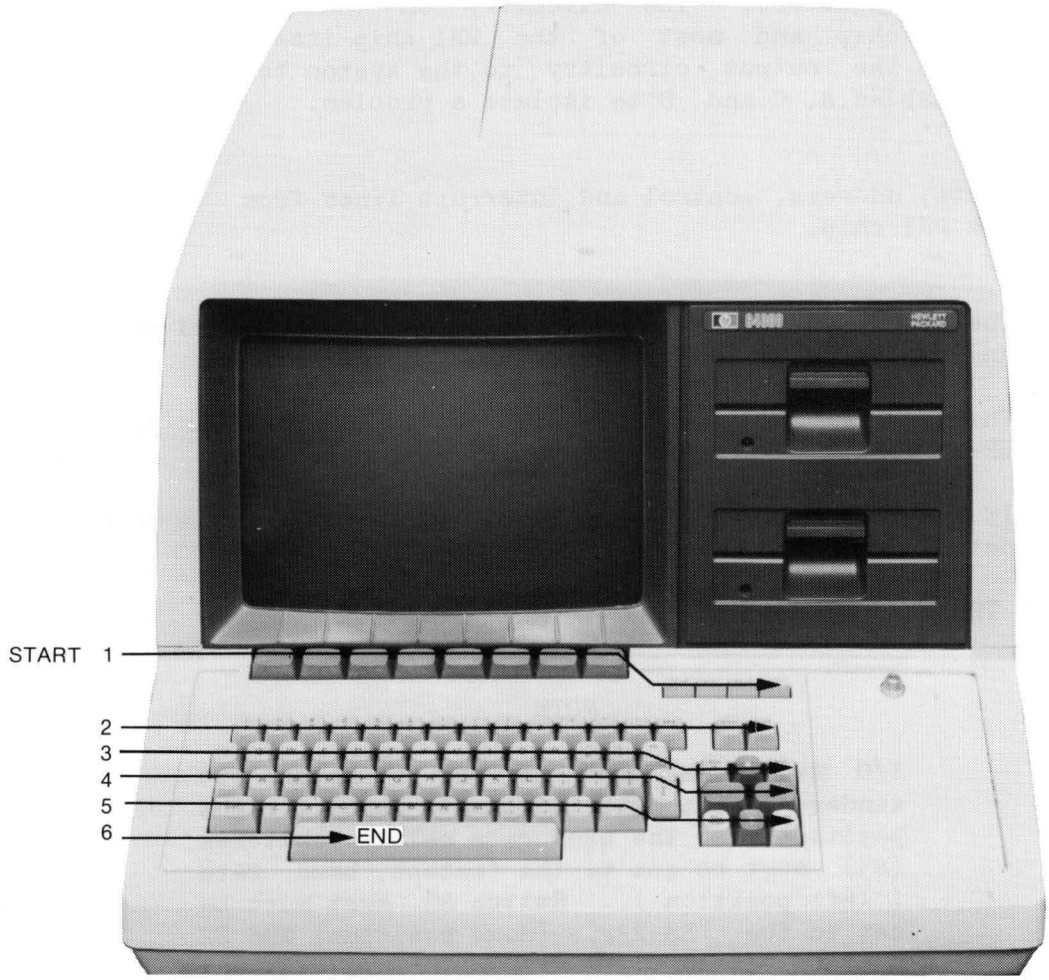


Figure 4-1. Keyboard Test Sequence

4-7. SYSTEM BUS TEST PROCEDURE.

CAUTION

THIS TEST SHOULD NOT BE RUN IF THE MAINFRAME IS CONNECTED TO THE SYSTEM BUS. IT WILL CAUSE THE OTHER MAINFRAMES ON THE BUS TO ABORT THERE SESSION.

Purpose:

During the System Bus Test, the PHI (U20 I/O board) chip is taken off line and the CPU writes to and reads from its internal registers. The circuitry on the input side of the PHI chip and most of the PHI chip itself is tested. None of the output circuitry to the system bus is tested. Use SA tables A, C and D to isolate a problem.

Area Tested:

The Data, address, control and interrupt lines from the CPU to the PHI chip.

Operation:

a. The SYSTEM BUS TEST takes the PHI chip off line and reads and writes to various registers in the PHI chip.

b. The transceiver lines and the cable to the Rear-panel HP-IB connector are not presently being checked.

c. If an error occurs, it may take up to 2 minutes to be detected.

4-8. RS-232 TEST PROCEDURE.

NOTE

I/O switch S5 must be set to return to sender - grant aknowledgement "RTS" (right position). The baud rate select switches (S5) must be set to the fastest baud rate (left position). Switch S3 must must be set to the "RS-232" (down position) and S2 must be set to "INTERNAL" (unless external clocks are used) before tests can be run.

Purpose:

This test checks proper operation of the USART (U28 I/O PCB) and the data/control circuitry associated with RS-232. Use SA loop E for trouble isolation.

Area Tested:

The 8251 USART, the baud rate generator, loop back relays, line drivers, the interface to the CPU, and the Rear-panel cable.

1. The voltage translators cannot be signaturized on the higher voltage side.

Operation:

a. Energizes the loop back relays to loop transmit data, and handshake lines back on receive data.

b. Sends a character stream.

c. compares receive character stream to the transmit character stream.

d. Notes:

1. If an error occurs it may take up to two minutes to to be detected.

2. If all previous PV tests have passed, a problem in this test will almost always indicate a failure in the mentioned circuits under RS-232 Test Procedure "Area Tested". Also, this test does not check the setting of the RS-232 mode switches on the I/O board (S1,S2, S3 and S4) or the baud rate select switch (S5).

4-9. TROUBLESHOOTING USING SIGNATURE ANALYSIS.

4-10. Signature Analysis (SA) offers a good method of isolating hardware logic failures down to the component level. The basic concept is to utilize a known set of start, stop and clock signals that constantly repeat (loop) with the same timing relationships. When a suspect logic node is probed with a Signature Analyzer while using the start, stop, and clock signals as control inputs, the digital readout (signature) displayed on the analyzer can be compared with the normal signature of that node to determine if the timing relationships are proper. With the 64100A Mainframe, looping is provided by the PV software program and the normal signatures for various nodes are listed in the tables 4-1 thru 4-6.

4-11. SERVICE TOOLS.

4-12. Suggested service tools are:

1. HP 5004A or 5005A Signature Analyzer
2. Digital Voltmeter
3. Oscilloscope
4. Standard hand tools for electronic PC board repair.

4-13. SA TABLES.

4-14. The I/O function signatures are categorized into 6 groups (loops) that are a result of the type of test the PV was performing at the time a failure or problem was noted. These loops are:

1. I/O Write (Loops A and B)
2. I/O Read (Loop C)
3. Time Interrupt (SA does not apply)
4. Keyboard (Loop F)
5. System HP-IB Bus (Loop D)
6. RS-232 Bus (Loop E)

4-15. The basic procedure is to refer to the appropriate table (i.e., the one that corresponds to the loop that PV was exercising when the failure was noted) and connect the Signature Analyzer to the Test Points called for in the table. Next, verify that the "Vh" signature indicated in the test set-up is proper. This signature is very important since it verifies that the start, stop and clock signals are normal. If this signature is good, proceed with the signatures listed in the table while referring to the appropriate schematic for guidance. If an improper signature is noted, check on both sides of the device to determine if it is causing the problem or if the problem has its origin further upstream.

NOTE

One of the first things that should be done when isolating System Bus (HP-IB) and RS-232 failures is to replace the PHI or USART chip. If this doesn't fix the problem, go back to I/O write and I/O read and verify the various signatures that show that the buffered bus is working properly. In I/O read, it is not necessary every time to take signatures; simply toggle the switches that are shown on the CRT display and verify that the display is correct.

Table 4-1. I/O Write Signature Analysis

Loop: A
PC Board: I/O Board.
Test failure: I/O S.A latch failure.
Procedure: Execute I/O Write test (to disable the beeper, jumper Q5 base (center lead) to emitter (dot).
S/A hookup:
START = POS EDGE CPU BD TP10 (S.A. INTERVAL)
STOP = POS EDGE CPU BD TP10 (S.A. INTERVAL)
CLOCK = POS EDGE I/O BP TP1 (LIOSB)
VH = 91C2
* = Probe blinking

Node	Sig	Node	Sig
U2-1	0021	U5-2	A14H
U2-2	5807	U5-3	0000*
U2-3	FCU6	U5-4	P405
U2-4	68P0	U5-5	9A2U
U2-5	1CPF	U5-6	0021
U2-6	PP8H	U5-7	0858
U2-7	H72H	U5-8	52F5
U2-8	5A37	U5-9	5A9H
U2-9	3FC8	U5-11	5A9H
U2-11	AH0A	U5-12	52F5
U2-12	FC85	U5-13	0858
U2-13	469U	U5-14	0021
U2-14	7U3U	U5-15	9A2U
U2-15	8A5P	U5-16	P405
U2-16	U952	U5-17	91C2
U2-17	5A44	U5-18	A14H
U2-18	F9C5	U5-19	0000
U2-19	0000*		
		U6-2	91C2
U4-1	0021	U6-9	0000
U4-2	5C53	U6-11	0021
U4-3	F54C	U6-18	0000
U4-4	9CCP		
U4-5	P947	U7-3	0C8U
U4-6	U639	U7-6	91C2
U4-7	3H09	U7-8	91C2
U4-8	0743	U7-11	OC8U
U4-9	CCA3		
U4-11	2A11	U11-2	CC15
U4-12	96U1	U11-7	7C65
U4-13	AFCC	U11-11	6987
U4-14	678C	U11-15	96U3
U4-15	78U5		
U4-16	0A0F	U14-2	90UU
U4-17	54U9	U14-5	P5P2
U4-18	FAP1	U14-6	3460
U4-19	0000*	U14-9	2153
		U14-12	7756
		U14-15	6C86
		U14-16	2H0C
		U14-19	9P4F

Table 4-1. I/O Write Signature Analysis (Cont'd)

Loop: A
PC Board: I/O Board.
Test failure: I/O S.A latch failure.
Procedure: Execute I/O Write test (to disable the beeper, jumper Q5 base (center lead) to emitter (dot).
S/A hookup:
START = POS EDGE CPU BD TP10 (S.A. INTERVAL)
STOP = POS EDGE CPU BD TP10 (S.A. INTERVAL)
CLOCK = POS EDGE I/O BP TP1 (LIOSB)
VH = 91C2
* = Probe blinking

Node	Sig	Node	Sig
U16-8	0C9H	U43-8	C363
U16-12	91C2	U43-9	2A11
		U43-10	22H1
U17-9	F8U8		
U17-10	F0C2	U44-1	91C2
U17-12	9265	U44-2	AU70
U17-15	91C2	U44-5	F7HF
		U44-6	CU1F
U18-7	91C2	U44-9	HHU6
U18-10	91A0	U44-11	F0C2
U18-13	91C2	U44-16	7HU0
U18-14	91C2	U44-19	C927
U18-15	0C8U		
		U45-1	0000
U22-12	91C2	U45-2	30UU
		U45-3	HU55
U23-2	0000	U45-4	85FF
U23-3	91C2	U45-5	FC2C
U23-5	0000	U45-6	2481
U23-6	91C2	U45-7	UCH4
U23-8	91C2	U45-9	9193
U23-10	0000	U45-10	F8H9
U23-11	91C2	U45-11	91C2
U23-13	0000	U45-12	91C2
U24-2	0000	U53-1	91C2*
U24-3	91C2	U53-2	91C2*
U24-6	91C2	U53-3	91C2*
U24-8	91C2	U53-4	91C2*
U24-10	0000	U53-5	91C2*
U24-11	91C2	U53-6	91C2*
U24-13	0000	U53-7	91C2*
		U53-8	91C2*
U30-6	91C2	U53-9	91C2*
U30-8	91C2	U53-10	91C2*
		U53-11	91C2*
U31-4	0021		
U31-10	9193	U54-3	UCH4
U31-14	0000*	U54-5	FC2C
		U54-14	85FF
		U54-16	2481

Figure 4-2. I/O Write Signature Analysis

Loop: B
PC Board: I/O Board.
Test failure or circuit: I/O WRITE TEST.
Procedure: Execute I/O Write Test. (To disable the beeper, Q5 may be jumpered, base to emitter.)
S/A hookup:

START = POS EDGE I/O BD TP2 (S.A. INTERVAL)
STOP = NEG EDGE I/O BD TP2 (S.A. INTERVAL)
CLOCK = POS EDGE CPU BD TP1 (LSTB)
VH = 7468

Node	Sig	Node	Sig
U43-8	C79A	U53-8	53P5
U43-9	CU6P	U53-9	FAC1
		U53-10	4AFC
U53-1	P291	U53-11	6H3U
U53-2	U197	U53-18	C79A
U53-3	U4A1	U53-19	CC65
U53-4	CUOP	U53-20	APH6
U53-5	AC3A	U53-21	3UOP
U53-6	C265	U53-22	OU77
U53-7	HO18	U53-23	8UHP

Table 4-3. I/O Read Signature Analysis

Loop: C
PC Board: I/O Board.
Test failure or circuit: I/O READ.
Procedure: Execute I/O Read Test.
S/A hookup:
START = POS EDGE I/O BD TP2 (S.A. INTERVAL)
STOP = NEG EDGE I/O BD TP2 (S.A. INTERVAL)
CLOCK = POS EDGE I/O BD TP1 (LIOSB)
VH = 0007
* = Probe Blinking

Node	Sig	Node	Sig	Node	Sig	Node	Sig
ALL S4 SET ON (RIGHT), S3 SET SET TO CL (UP)				ALL S4 SET OFF (LEFT), S3 SET TO RS-232 (DOWN)			
U4-2	0007*	U35-3	0003	U4-2	0007*	U35-3	0007*
U4-3	0001	U35-5	0001	U4-3	0005	U35-5	0005
U4-4	0003	U35-7	0003	U4-4	0007	U35-7	0007*
U4-5	0001	U35-9	0007*	U4-5	0005	U35-9	0007*
U4-6	0003	U35-12	0003	U4-6	0007*	U35-12	0007*
U4-7	0003	U35-14	0003	U4-7	0007*	U35-14	0007*
U4-8	0003	U35-16	0003	U4-8	0007*	U35-16	0007*
U4-9	0003	U35-18	0003	U4-9	0007*	U35-18	0007*
IMMATERIAL HOW S3 OR S4 ARE SET							
U5-3	000*	U14-2	0007*	U22-12	0007		
U5-5	0006	U14-5	0000				
U5-7	0001	U14-6	0000	U23-2	0000		
U5-8	0004	U14-9	0000	U23-3	0007		
U5-9	0001	U14-12	0000	U23-5	0000		
U5-11	0001	U14-15	0000	U23-6	0007		
U5-12	0004	U14-16	0000	U23-8	0007		
U5-13	0001	U14-19	0000	U23-10	0000		
U5-15	0006			U23-11	0007		
U5-17	0007*	U17-9	0006	U23-13	0000		
		U17-10	0007				
U6-2	0007	U17-12	0007*	U24-2	0000		
U6-9	0000*	U17-15	0007	U24-3	0007		
U6-11	0007*			U24-5	0000*		
U6-18	0000	U18-7	0007	U24-6	0007		
		U18-10	0007*	U24-8	0007		
U7-3	0007	U18-13	0007	U24-10	0000		
U7-5	0005	U18-14	0003	U24-11	0007		
U7-6	0005	U18-15	0005	U24-13	0000		
U7-8	0007						
		U22-12	0007	U31-4	0007*		
				U31-10	0000*		
				U31-13	0000*		

Table 4-4 I/O Bus Signature Analysis

Loop: D
PC Board: I/O Board.
Test failure or circuit: I/O SYS BUS TEST.
Procedure: Execute System Bus Test.
S/A hookup:
START = POS EDGE I/O BD TP2 (S.A. INTERVAL)
STOP = NEG EDGE I/O BD TP2 (S.A. INTERVAL)
CLOCK = POS EDGE I/O BD TP1 (LIOSB)
VH = 9A4A
* = Probe blinking

Node	Sig	Node	Sig	Node	Sig
U2-2	4F66	U5-11	0001	U16-2	0A63
U2-3	4PUH	U5-12	0000*	U16-3	9A4A*
U2-4	5549	U5-13	0001	U16-4	0000*
U2-5	H32F	U5-15	9A4C	U16-10	0000*
U2-6	A18F	U5-17	9A4A*	U16-11	9A4A*
U2-7	8CP6				
U2-8	574F	U6-2	9A4A*	U17-9	9A4C
U2-9	61U6	U6-9	0A63	U17-10	9A4A
U2-11	UCCF	U6-11	9029	U17-12	9A4A*
U2-12	FH06	U6-18	0000*	U17-14	9A4A
U2-13	11AF				
U2-14	3CF6	U7-2	9029	U18-7	9A4A
U2-15	4966	U7-3	HU64	U18-10	9A4A*
U2-16	FU03	U7-4	0A63	U18-13	9A4A
U2-17	H4C7	U7-6	9A4A	U18-14	9A4A
U2-18	H62F	U7-9	452U	U18-15	0001
		U7-11	HU64		
U4-2	C415	U7-12	HU65	U22-12	9A4A*
U4-3	98A3	U7-13	0001		
U4-4	3A12			U23-2	0000
U4-5	3C9P	U11-1	9A4A	U23-3	9A4A*
U4-6	3C9P	U11-2	2427	U23-5	0000
U4-7	3C9P	U11-4	C415	U23-6	9A4A*
U4-8	ACC6	U11-5	3A12	U23-8	9A4A*
U4-9	ACC6	U11-7	17FA	U23-10	0000*
U4-11	31UF	U11-11	9A4A	U23-11	9A4A
U4-12	31UF	U11-12	3C9P	U23-13	9A4A
U4-13	A1H4	U11-13	98A3		
U4-14	A1H4	U11-15	07A8	U24-2	0000
U4-15	A1H4			U24-3	9A4A
U4-16	A058	U14-2	0000*	U24-5	9A4A/3951
U4-17	02P9	U14-5	0000	U24-6	9A4A
U4-18	2P5U	U14-6	0000	U24-8	9A4A
		U14-9	0000	U24-10	0000
U5-3	0000*	U14-12	0000	U24-11	9A4A
U5-5	9A4C	U14-15	0000	U24-13	0000
U5-7	0001	U14-16	0000		
U5-8	0000*	U14-19	0000*	U31-4	9029
U5-9	0001			U31-13	0000*

Table 4-5. I/O RS232 Signature Analysis

Loop: E
PC Board: I/O Board.
Test failure or circuit: RS-232 FAILURE.
Procedure: Set S5 to half-duplex and fastest baud rate. Set S3 to RS-232.
Set all switches on S4 to the left. Execute RS-232 Test.
S/A hookup:
START = POS EDGE I/O BD TP2 (S.A. INTERVAL)
STOP = NEG EDGE I/O BD TP2 (S.A. INTEVAL)
CLOCK = POS EDGE I/O BD TP1 (LIOSB)
VH = 00UP
* = Probe blinking

Node	Sig	Node	Sig
U2-2	0019	U18-7	00UP
U2-3	005U	U18-10	00UF
U2-4	001H	U18-13	009A
U2-5	001H	U18-14	00P6
U2-6	001H	U18-15	007U
U2-7	001H		
U2-8	003H	U22-12	00UP*
U2-9	005H		
U2-11	00A3		U23-2
U2-12	00F3	U23-3	00UP
U2-13	00P3	U23-5	0000*
U2-14	00P3	U23-6	00UP*
U2-15	00P3	U23-8	00UP
U2-16	00P3	U23-10	0000
U2-17	00A1	U23-11	00UP*
U2-18	00P7	U23-13	0000*
U5-3	0000*	U24-2	0000
U5-5	00UU	U24-3	00UP
U5-7	0003	U24-5	00UH
U5-8	001A	U24-6	00UP
U5-9	0065	U24-8	00UP
U5-11	0065	U24-10	0000
U5-12	001A	U24-11	00UP
U5-13	0003	U24-13	0000
U5-15	00UU		
U5-17	00UP*	U28-3	00UP*
		U28-17	003U
U17-9	00UU	U28-19	00UP*
U17-10	00UP	U28-22	001U
U17-12	00UP*	U28-23	003U
U17-15	00UP	U28-24	001U
		U31-4	0019
		U31-10	00P7
		U31-13	0000*

Table 4-6. I/O Keyboard Signature Analysis

Loop: F
PC Board: I/O Board.
Test failure or circuit: KEYBOARD FAILURE.
Procedure: Set all test jumpers to "Test" position, Except E1 and E2. Executer Keyboard Test.
S/A hookup:

START = POS EDGE I/O BOARD TP7
STOP = POS EDGE I/O BOARD TP7
CLOCK = POS EDGE I/O BOARD TP8
VH = 8P54
* = Probe Blinking

Node	Sig	Node	Sig
U25-6	C4FP	U38-1	84H4
U25-8	3A9A	U38-4	18A5
		U38-8	2046
U34-3	0863	U38-10	AP12
U34-4	HH53	U38-13	A492
U34-5	H10F		
U34-6	3A9A	U39-1	0000*
U34-8	FCF2	U39-5	HH89
U34-9	2946	U39-6	53HH
U34-10	F61C	U39-7	29PP
U34-11	0108	U39-9	A7CA
		U40-5	FCF2
		U40-6	0A80
		U40-8	314C

SECTION V

ADJUSTMENTS

5-1. GENERAL.

5-2. The I/O, Keyboard and Rear-Panel PC boards have no adjustments.

SECTION VI

REPLACEABLE PARTS

6-1. INTRODUCTION.

6-2. This section contains information for ordering parts. Table 6-1 lists the names and addresses that correspond to the manufacturers' code numbers. Table 6-2 lists the abbreviations used in the parts list and throughout this manual. Table 6-3 lists all replaceable parts for the I/O, Rear-panel, and Keyboard PC boards in reference designator order.

6-3. ABBREVIATIONS.

6-4. Table 6-2 lists abbreviations used in the parts list, the schematics, and elsewhere in this manual. In some cases, two forms of the abbreviation are used; one, all in capital letters, and two, partial or no capitals. This occurs because the abbreviations in the parts list are always all capitals. However, in the schematics and other parts of the manual, other abbreviation forms may be used with both lowercase and uppercase letters.

6-5. ORDERING INFORMATION.

6-6. To order a part listed in the replaceable parts list (See table 6-3), quote the Hewlett-Packard part number and check digit, indicate the quantity required, and address the order to the nearest Hewlett-Packard Office (refer to Sales and Service offices listed at the back of the mainframe manual).

6-7. To order a part that is not listed in table 6-3, include the HP Part Number for the part, the description and function of the part, and the quantity of parts required. Address the order to the nearest Hewlett-Packard office.

Table 6-1. List of Manufacturers' Codes

MFR NO.	MANUFACTURER NAME	ADDRESS	ZIP CODE
00000	Any Satisfactory Supplier		
00466	Norelco N. Amer philips Corp	Los Angeles Ca	90021
01121	Allen-Bradley Co	Milwaukee Wi	53204
01295	Texas Instr Semicond Div	Dallas Tx	75222
01928	RCA Corp Solid State Div	Somerville NJ	08876
03888	KDI Pyrofilm Corp	Whippany NJ	07981
04713	Motorola Semicond Products	Phoenix Az	85062
07263	Fairchild Semicond Div	Mountain View Ca	94042
09023	Cornell-Dubilier Eleck Div	Sanford NC	27330
13103	Thermalloy Co	Dallas Tx	75234
19701	Mepco/Electra Corp	Mineral Wells Tx	76067
20940	Micro-Ohm Corp	El Monte Ca	91731
24546	Corning Glass Wks	Bradford Pa	16701
26654	Varadyne Inc	Santa Monica Ca	90404
27014	National Semicond Corp	Santa Clara Ca	95051
27777	Varo Semicond Inc	Garland Tx	75040
28480	Hewlett-Packard Hq	Palo Alto Ca	94304
30983	Mepco/Electra Corp	San Diego Ca	92121
32997	Bourns Trimpot Div	Riverside Ca	92507
34344	Motorola Inc	Franklin Park Il	60131
34649	Intel Corp	Mountain View Ca	95051
56289	Sprague Elect Co	North Adams Ma	01247
71590	Centralab Eleck Div	Milwaukee Wi	50501
72136	Electro Motive Corp	Willimantic Ct	06226
75042	TRW Inc	Philadelphia Pa	19108
75382	Kulka Elect Corp	Mt Vernon NY	10550
75915	Littlefuse Inc	Des Plaines Il	60016

6-8. DIRECT MAIL ORDER SYSTEM

6-9. Within the USA, Hewlett-Packard can supply parts through a direct mail order system. Advantages of using this system are:

1. Direct ordering and shipment from the HP Parts Center in Mountain View, California.

2. No maximum or minimum on any mail order (there is a minimum order amount for parts ordered through a local HP office when the orders require billing and invoicing).

3. Prepaid transportation (there is a small handling charge for each order).

4. No invoices (to provide these advantages, a check or money order must accompany each order).

6-10. Mail-order forms and specific ordering information are available through your local HP office. Addresses and phone numbers are located at the back of this manual.

6-11. PARTS LIST

6-12. Table 6-3 lists the replaceable parts for the I/O, Rear-panel, and Keyboard PC boards and is organized as follows:

1. Electrical assemblies and their components in alphanumerical order by reference designation.

2. Miscellaneous parts.

6-13. The information given for each part consists of the following:

1. Hewlett-Packard part number and check digit. (for HP internal use).

2. Total quantity (Qty) on the PC board.

3. Description of the part.

4. Typical manufacturer of the part in a five-digit code.

5. Manufacturer's number for the part.

NOTE

The total quantity for each part is given only at the first appearance of the part number in the list.

Table 6-2. Reference Designators and Abbreviations

REFERENCE DESIGNATORS

A	= assembly	**F**	= fuse	**MP**	= mechanical part	**U**	= integrated circuit
B	= motor	**FL**	= filter	**P**	= plug	**V**	= vacuum, tube, neon bulb, photocell, etc
BT	= battery	**IC**	= integrated circuit	**Q**	= transistor		
C	= capacitor	**J**	= jack	**R**	= resistor	**VR**	= voltage regulator
CP	= coupler	**K**	= relay	**RT**	= thermistor	**W**	= cable
CR	= diode	**L**	= inductor	**S**	= switch	**X**	= socket
DL	= delay line	**LS**	= loud speaker	**T**	= transformer	**Y**	= crystal
DS	= device signaling (lamp)	**M**	= meter	**TB**	= terminal board	**Z**	= tuned cavity network
E	= misc electronic part	**MK**	= microphone	**TP**	= test point		

ABBREVIATIONS

A	= amperes	**H**	= henries	**N/O**	= normally open	**RMO**	= rack mount only
AFC	= automatic frequency control	**HDW**	= hardware	**NOM**	= nominal	**RMS**	= root-mean square
AMPL	= amplifier	**HEX**	= hexagonal	**NPO**	= negative positive zero (zero temperature coefficient)	**RWV**	= reverse working voltage
		HG	= mercury				
BFO	= beat frequency oscillator	**HR**	= hour(s)				
BE CU	= beryllium copper	**HZ**	= hertz	**NPN**	= negative-positive-negative	**S-B**	= slow-blow
BH	= binder head					**SCR**	= screw
BP	= bandpass			**NRFR**	= not recommended for field replacement	**SE**	= selenium
BRS	= brass	**IF**	= intermediate freq			**SECT**	= section(s)
BWO	= backward wave oscillator	**IMPG**	= impregnated	**NSR**	= not separately replaceable	**SEMICON**	= semiconductor
		INCD	= incandescent			**SI**	= silicon
CCW	= counter-clockwise	**INCL**	= include(s)			**SIL**	= silver
CER	= ceramic	**INS**	= insulation(ed)	**OBD**	= order by description	**SL**	= slide
CMO	= cabinet mount only	**INT**	= internal	**OH**	= oval head	**SPG**	= spring
COEF	= coeficient			**OX**	= oxide	**SPL**	= special
COM	= common	**K**	= kilo=1000			**SST**	= stainless steel
COMP	= composition					**SR**	= split ring
COMPL	= complete	**LH**	= left hand	**P**	= peak	**STL**	= steel
CONN	= connector	**LIN**	= linear taper	**PC**	= printed circuit		
CP	= cadmium plate	**LK WASH**	= lock washer	**PF**	= picofarads= 10^{-12} farads	**TA**	= tantalum
CRT	= cathode-ray tube	**LOG**	= logarithmic taper			**TD**	= time delay
CW	= clockwise	**LPF**	= low pass filter	**PH BRZ**	= phosphor bronze	**TGL**	= toggle
				PHL	= phillips	**THD**	= thread
DEPC	= deposited carbon	**M**	= milli=10^{-3}	**PIV**	= peak inverse voltage	**TI**	= titanium
DR	= drive	**MEG**	= meg=10^{6}	**PNP**	= positive-negative-positive	**TOL**	= tolerance
		MET FLM	= metal film			**TRIM**	= trimmer
ELECT	= electrolytic	**MET OX**	= metallic oxide	**P/O**	= part of	**TWT**	= traveling wave tube
ENCAP	= encapsulated	**MFR**	= manufacturer	**POLY**	= polystyrene		
EXT	= external	**MHZ**	= mega hertz	**PORC**	= porcelain	**U**	= micro=10^{-6}
		MINAT	= miniature	**POS**	= position(s)		
F	= farads	**MOM**	= momentary	**POT**	= potentiometer	**VAR**	= variable
FH	= flat head	**MOS**	= metal oxide substrate	**PP**	= peak-to-peak	**VDCW**	= dc working volts
FIL H	= fillister head	**MTG**	= mounting	**PT**	= point		
FXD	= fixed	**MY**	= "mylar"	**PWV**	= peak working voltage	**W/**	= with
						W	= watts
G	= giga (10^{9})	**N**	= nano (10^{-9})	**RECT**	= rectifier	**WIV**	= working inverse voltage
GE	= germanium	**N/C**	= normally closed	**RF**	= radio frequency		
GL	= glass	**NE**	= neon	**RH**	= round head or right hand	**WW**	= wirewound
GRD	= ground(ed)	**NI PL**	= nickel plate			**W/O**	= without

Table 6-3. Replaceable Parts List

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A6	64100-66520	8	1	I/O CIRCUIT BOARD ASSEMBLY	28480	64100-66520
C1	0160-2055	9	35	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C2	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C3	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C4	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C5	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C6	0140-0207	7	5	CAPACITOR-FXD 330PF +-5% 500VDC MICA	72136	DM15F331J0500WV1CR
C7	0140-0207	7		CAPACITOR-FXD 330PF +-5% 500VDC MICA	72136	DM15F331J0500WV1CR
C8	0140-0207	7		CAPACITOR-FXD 330PF +-5% 500VDC MICA	72136	DM15F331J0500WV1CR
C9	0180-0197	8		CAPACITOR-FXD 2.2UF +-10% 20VDC TA	56289	150D225X9020A2
C10	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C11	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C12	0140-0207	7		CAPACITOR-FXD 330PF +-5% 500VDC MICA	72136	DM15F331J0500WV1CR
C13	0140-0207	7		CAPACITOR-FXD 330PF +-5% 500VDC MICA	72136	DM15F331J0500WV1CR
C14	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C15	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C16	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C17	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C18	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C19	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C20	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C21	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C22	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C23	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C24	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C25	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C26	0140-0195	2	1	CAPACITOR-FXD 130PF +-5% 300VDC MICA	72136	DM15F131J0300WV1CR
C27	0160-0154	5	1	CAPACITOR-FXD 2200PF +-10% 200VDC POLYE	28480	0160-0154
C28	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C29	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C30	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C31	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C32	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C33	0180-0197	8	3	CAPACITOR-FXD 2.2UF+-10% 20VDC TA	56289	150D225X9020A2
C34	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C35	0160-0161	4	1	CAPACITOR-FXD .01UF +-10% 200VDC POLYE	28480	0160-0161
C36	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C37	0180-0197	8		CAPACITOR-FXD 2.2UF+-10% 20VDC TA	56289	150D225X9020A2
C38	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C39	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C40	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C41	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C42	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C43	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C44	0180-0374	3	4	CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X902082
C45	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X902082
C46	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X902082
C47	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C48						
C49	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C50	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C51	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X902082
CR1	1901-0040	1	4	DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
CR2	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
CR3	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
CR4	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
CR5	1901-0535	9	1	DIODE-SM SIG SCHOTTKY	28480	1901-0535
MP1	5040-6073	0	1	EXTRACTOR (RED)	28480	5040-6073
MP2	8151-0013	4	1	WIRE 22AWG 1X22	28480	8151-0013
MP3	1200-0475	0	6	CONNECTOR-SGL CONT SKT .016-IN-BSC-SZ	28480	1200-0475
MP4	1200-0539	7	1	SOCKET-IC 16-CONT DIP-SLDR	28480	1200-0539
MP5	1200-0638	7	1	SOCKET-IC 14-CONT DIP-SLDR	28480	1200-0638
MP6	1200-0567	1	1	SOCKET-IC 28-CONT DIP-SLDR	28480	1200-0567
MP7	1200-0839	0	1	SOCKET-IC 48-PIN (FOR U20, PHI)	28480	1200-0839
MP8	1251-4388	9	1	CONNECTOR 3-PIN M POST TYPE	28480	1251-4388
MP9	1480-0116	8	1	PIN-GRV .062-IN-DIA .25-IN-LG STL	28480	1480-0116
Q1	1853-0006	6	1	TRANSISTOR PNP 2N3134 SI TO-5 PD=600MW	04713	2N3134
Q2	1854-0472	2	2	TRANSISTOR NPN SI DARL PD=500MW	04713	MPS-A14
Q3	1854-0246	8	2	TRANSISTOR NPN SI PD=350MW FT=250MHZ	04713	SPS 233
Q4	1854-0472	2		TRANSISTOR NPN SI DARL PD=500MW	04713	MPS-A14
Q5	1854-0246	8		TRANSISTOR NPN SI PD=350MW FT=250MHZ	04713	SPS 233

Table 6-3. Replaceable Parts List (continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
R1	0757-0290	5	7	RESISTOR 6.19K 1% .125W F TC=0+-100	19701	MF4C1/8-T0-6191-F
R2	0757-0290	5		RESISTOR 6.19K 1% .125W F TC=0+-100	19701	MF4C1/8-T0-6191-F
R3	0757-1001	8	1	RESISTOR 56.2 1% .5W F TC=0+-100	28480	0757-1001
R4	0757-0724	0	1	RESISTOR 392 1% .25W F TC=0+-100	24546	C5-1/4-T0-392R-F
R5	0757-0443	0	5	RESISTOR 11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1102-F
R6	0757-0720	6	1	RESISTOR 243 1% .25W F TC=0+-100	24546	C5-1/4-T0-243R-F
R7	0757-0796	6	1	RESISTOR 82.5 1% .5W F TC=0+-100	28480	0757-0796
R8	0757-0460	1		RESISTOR 61.9K 1% .125W F TC=0+-100	24546	C4-1/8-T0-6192-F
R9	0698-3629	4	1	RESISTOR 270 5% 2W MO TC=0+-200	28480	0698-3629
R10	0760-0024	0	1	RESISTOR 100 5% 1W MO TC=0+-200	28480	0760-0024
R11	0757-0443	0		RESISTOR 11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1102-F
R12	0757-0443	0		RESISTOR 11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1102-F
R13	0757-0280	3	4	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R14	0757-0717	1	1	RESISTOR 182 1% .25W F TC=0+-100	24546	C5-1/4-T0-182R-F
R15	0698-3159	5	1	RESISTOR 26.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2612-F
R16	0757-0290	5		RESISTOR 6.19K 1% .125W F TC=0+-100	19701	MF4C1/8-T0-6191-F
R17	0757-0290	5		RESISTOR 6.19K 1% .125W F TC=0+-100	19701	MF4C1/8-T0-6191-F
R18	0757-0411	2	1	RESISTOR 332 1% .125W F TC=0+-100	24546	C4-1/8-T0-332R-F
R19	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R20	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R21	0757-0290	5		RESISTOR 6.19K 1% .125W F TC=0+-100	19701	MF4C1/8-T0-6191-F
R22	0757-0473	6	1	RESISTOR 221K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2213-F
R23	0698-3443	0	1	RESISTOR 287 1% .125W F TC=0+-100	24546	C4-1/8-T0-287R-F
R24	0698-3428	1	1	RESISTOR 14.7 1% .125W F TC=0+-100	03888	PME55-1/8-T0-14R7-F
R25	0757-0460	1	2	RESISTOR 61.9K 1% .125W F TC=0+-100	24546	C4-1/8-T0-6192-F
R26	0687-1001	9	1	RESISTOR 10 10% .5W CC TC=0+412	01121	EB1001
R27	0757-0443	0		RESISTOR 11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1102-F
R28	0698-3447	4	1	RESISTOR 422 1% .125W F TC=0+-100	24546	C4-1/8-T0-422R-F
R29	0698-3157	3	2	RESISTOR 19.6K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1962-F
R30	0698-3157	3		RESISTOR 19.6K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1962-F
R31	0757-0290	5		RESISTOR 6.19K 1% .125W F TC=0+-100	19701	MF4C1/8-T0-6191-F
R32	0757-0290	5		RESISTOR 6.19K 1% .125W F TC=0+-100	19701	MF4C1/8-T0-6191-F
R33	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R34	0757-0449	6	1	RESISTOR 20K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2002-F
R35	0757-0443	0		RESISTOR 11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1102-F
R36	0757-0438	3	1	RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
SW1	3101-2370	0	1	SWITCH-SL DPDT DIP-SLIDE-ASSY .1A 50VDC	28480	3101-2370
SW2	3101-2363	1	1	SWITCH-SL 2-3PDT DIP-SLIDE-ASSY .1A	28480	3101-2363
SW3	3101-2179	7	1	SWITCH-SL 4PDT DIP-SLIDE-ASSY .25A 30VDC	28480	3101-2179
SW4	3101-2371	1	1	SWITCH-SL 8-1A DIP-SLIDE-ASSY .1A 50VDC	28480	3101-2371
SW5	3101-2372	2	1	SWITCH-SL 5-1A DIP-SLIDE-ASSY .1A 50VDC	28480	3101-2372
TP1- TP6+ Gnds	0360-0535	0	8	TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
U1	1810-0276	2	5	NETWORK-RES 10-SIP1.5K OHM X 9	01121	210A152
U2	1820-2206	3	2	IC MISC TTL LS	01295	SN74LS640N
U3	1810-0276	2		NETWORK-RES 10-SIP1.5K OHM X 9	01121	210A152
U4	1820-2206	3		IC MISC TTL LS	01295	SN74LS640N
U5	1820-2024	3	5	IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U6	1820-1917	1	2	IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U7	1820-1208	3	2	IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
U8	1820-0509	5	2	IC DRVR DTL LINE DRVR QUAD	04713	MC1488L
U9	1820-0990	8	2	IC RCVR DTL NAND LINE QUAD	04713	MC1489AL
U10	1820-2024	3	2	IC OCT-BFRS-LINE DRVR	04713	SN74LS244N
U11	1820-1195	7	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS175N
U12	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U13	1810-0276	2		NETWORK-RES 10-SIP1.5K OHM X 9	01121	210A152
U14	1820-1730	6	2	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
U15	1820-1205	0	1	IC GATE TTL LS AND DUAL 4-INP	01295	SN74LS21N
U16	1820-1199	1	1	IC INV TTL LS HEX 1-INP	01295	SN74LS04N
U17	1820-1216	3	2	IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
U18	1820-1216	3		IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
U19	1820-0509	5		IC DRVR DTL LINE DRVR QUAD	04713	MC1488L
U20	1AA6-6104	1	1	HP-IB INTERFACE CONTROLLER	28480	1AA6-6104
U21	1820-1917	1		IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U22	1820-1243	6	1	IC GATE TTL LS AND TPL 3-INP	01295	SN74LS15N
U23	1820-1197	9	4	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U24	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U25	1820-1416	5	2	IC SCHMITT-TRIG TTL LS INV HEX 1-INP	01295	SN74LS14N
U26	1816-1092	4	1	IC-256-BIT RAM	28480	1816-1092
U27	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U28	1820-2289	2	1	IC UART NMOS	34649	C8251A
U29	1820-1112	8	3	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74N
U30	1820-1208	3		IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N

Table 6-3. Replaceable Parts List (continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U31	1820-1144	6	2	IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
U32	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74N
U33	1820-1423	4	1	IC MV TTL LS MONOSTBL RETRIG DUAL	01295	SN74LS123N
U34	1820-1989	7	2	IC CNTR TTL LS BIN DUAL 4-BIT	07263	74LS393PC
U35	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U36	1810-0276	2		NETWORK-RES 10-SIP1.5K OHM X 9	01121	210A152
U37	1820-1989	7		IC CNTR TTL LS BIN DUAL 4-BIT	07263	74LS393PC
U38	1820-1144	6		IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
U39	1820-1212	9	1	IC FF TTL LS J-K NEG-EDGE-TRIG	01295	SN74LS112N
U40	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74N
U41	1826-0180	0	1	IC TIMER TTL MONO/ASTBL	04713	MC1455P1
U42	1820-1415	4	1	IC SCHMITT-TRIG TTL LS NAND DUAL 4-INP	01295	SN74LS13N
U43	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U44	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
U45	1820-1281	2	1	IC DCDR TTL LS 2-TO-4-LINE DUAL 2-INP	01295	SN74LS139N
U46	1820-0990	8		IC RCVR DTL NAND LINE QUAD	04713	MC1489AL
U47	1810-0276	2		NETWORK-RES 10-SIP1.5K OHM X 9	01121	210A152
U48	1813-0131	4	1	IC GEN DUAL	34344	K1135A
U49	1820-1432	5	1	IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS163AN
U50	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U51	1820-0621	2	1	IC BFR TTL NAND QUAD 2-INP	01295	SN7438N
U52	1820-1422	3	1	IC MV TTL LS MONOSTBL RETRIG	01295	SN74LS122N
U53	1820-0495	8	1	IC DCDR TTL 4-TO-16-LINE 4-INP	01295	SN74154N
U54	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U55	1820-1416	5		IC SCHMITT-TRIG TTL LS INV HEX 1-INP	01295	SN74LS14N
VR1	1902-3002	3	1	DIODE-ZNR 2.37V 5% DO-7 PD=.4W TC=-.074%	28480	1902-3002
VR2	1902-3104	6	1	DIODE-ZNR 5.62V 5% DO-7 PD=.4W TC=+.016%	28480	1902-3104

Table 6-3. Replaceable Parts List (continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A4	64100-66504	8	1	KEYBOARD CIRCUIT BOARD ASSEMBLY	28480	64100-66504
C1	0180-0230	0	1	CAPACITOR-FXD 1UF+-20% 50VDC TA	56289	150D105X0050A2
C2	0160-2055	9	4	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C3	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C4	0140-0196	3	1	CAPACITOR-FXD 150PF +-5% 300VDC MICA	72136	DM15F151J0300WV1CR
C5	0160-2204	0	1	CAPACITOR-FXD 100PF +-5% 300VDC MICA	28480	0160-2204
C6	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C7	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C8	0160-3443	1	2	CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
C9	0160-2198	1	8	CAPACITOR-FXD 20PF +-5% 300VDC MICA	28480	0160-2198
C10	0160-2198	1		CAPACITOR-FXD 20PF +-5% 300VDC MICA	28480	0160-2198
C11	0160-2198	1		CAPACITOR-FXD 20PF +-5% 300VDC MICA	28480	0160-2198
C12	0160-2198	1		CAPACITOR-FXD 20PF +-5% 300VDC MICA	28480	0160-2198
C13	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
C14	0160-2198	1		CAPACITOR-FXD 20PF +-5% 300VDC MICA	28480	0160-2198
C15	0160-2198	1		CAPACITOR-FXD 20PF +-5% 300VDC MICA	28480	0160-2198
C16	0160-2198	1		CAPACITOR-FXD 20PF +-5% 300VDC MICA	28480	0160-2198
C17	0160-2198	1		CAPACITOR-FXD 20PF +-5% 300VDC MICA	28480	0160-2198
H1	2360-0113	2	6	SCREW-MACH 6-32 .25-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
MP1	3101-2137	7	77	KEY SWITCH (INDUCTIVE)	28480	3101-2137
Q1	1854-0246	8	1	TRANSISTOR NPN SI PD=350MW FT=250MHZ	04713	SPS 233
Q2	1853-0015	7	1	TRANSISTOR PNP SI PD=200MW FT=500MHZ	28480	1853-0015
Q3	1854-0215	1	2	TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
Q4	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
R1	0757-0389	5	1	RESISTOR 33.2 1% .125W F TC=0+-100	28480	0757-0389
R2	0757-0442	9	1	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R3	0757-0401	0	1	RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
R4	0757-0280	3	2	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R5	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R6	0757-0438	3	1	RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
R7	0698-3151	7	2	RESISTOR 2.87K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2871-F
R8	0698-3151	7		RESISTOR 2.87K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2871-F
R9	0757-0420	3	1	RESISTOR 750 1% .125W F TC=0+-100	24546	C4-1/8-T0-751-F
R10	0757-0416	7	1	RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
R11	0757-0424	7	1	RESISTOR 1.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1101-F
U1	1820-0491	4	2	IC DCDR TTL BCD-TO-DEC 4-TO-10-LINE	01295	SN74145N
U2	1820-0491	4		IC DCDR TTL BCD-TO-DEC 4-TO-10-LINE	01295	SN74145N
U3	1810-0325	2	1	NETWORK-RES 16-DIP150.0 OHM X 8	01121	3168151
U4	1821-0002	5	2	TRANSISTOR ARRAY	01928	CA3045
U5	1821-0002	5		TRANSISTOR ARRAY	01928	CA3045
U6	1810-0275	1	1	NETWORK-RES 10-8IP1.0K OHM X 9	01121	210A102
U7	1820-0622	3	1	IC MUXR/DATA-SEL TTL 8-TO-1-LINE 8-INP	01295	SN74151AN
H2	64100-00606	3	1	KEYBOARD SHIELD	28480	64100-00606
H3	00180-09104	6	5	KEYBOARD GROUNDING CLIPS	28480	00180-09104
				NOTE **THE PARTS LISTED BELOW HAVE PART NUMBERS SEPARATE TO THE KEYBOARD ASSEMBLY.**		
MP2	5001-2815	8	1	SPACE BAR RUBBER GROMMET	28480	5001-2815
MP3	5001-2816	9	2	SPACE BAR PLUNGER	28480	5001-2816
MP4	1530-1983	6	2	SPACE BAR HOUSING	28480	1530-1983
MP5	1460-1562	8	1	SPACE BAR TORSION SPRING	28480	1460-1562

See introduction to this section for ordering information

Table 6-3. Replaceable Parts List (continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
8KI-8	0371-0544	4	1	KEY CAP -8PACEBAR	28480	0371-0544
	0371-1134	0	8	KEY CAP, SOFT KEY	28480	0371-1134
	0371-1363	7	1	KEY CAP, A	28480	0371-1363
	0371-1364	8	1	KEY CAP, B	28480	0371-1364
	0371-1365	9	1	KEY CAP, C	28480	0371-1365
	0371-1366	0	1	KEY CAP, D	28480	0371-1366
	0371-1367	1	1	KEY CAP, E	28480	0371-1367
	0371-1368	2	1	KEY CAP, F	28480	0371-1368
	0371-1369	3	1	KEY CAP, G	28480	0371-1369
	0371-1370	6	1	KEY CAP, H	28480	0371-1370
	0371-1371	7	1	KEY CAP, I	28480	0371-1371
	0371-1372	8	1	KEY CAP, J	28480	0371-1372
	0371-1373	9	1	KEY CAP, K	28480	0371-1373
	0371-1374	0	1	KEY CAP, L	28480	0371-1374
	0371-1375	1	1	KEY CAP, M	28480	0371-1375
	0371-1376	2	1	KEY CAP, N	28480	0371-1376
	0371-1377	3	1	KEY CAP, O	28480	0371-1377
	0371-1378	4	1	KEY CAP, P	28480	0371-1378
	0371-1379	5	1	KEY CAP, Q	28480	0371-1379
	0371-1380	8	1	KEY CAP, R	28480	0371-1380
	0371-1381	9	1	KEY CAP, S	28480	0371-1381
	0371-1382	0	1	KEY CAP, T	28480	0371-1382
	0371-1383	1	1	KEY CAP, U	28480	0371-1383
	0371-1384	2	1	KEY CAP, V	28480	0371-1384
	0371-1385	3	1	KEY CAP, W	28480	0371-1385
	0371-1386	4	1	KEY CAP, X	28480	0371-1386
	0371-1387	5	1	KEY CAP, Y	28480	0371-1387
	0371-1388	6	1	KEY CAP, Z	28480	0371-1388
	0371-1389	7	1	KEY CAP, BACK 8PACE	28480	0371-1389
	0371-1635	6	1	KEY CAP, TAB	28480	0371-1635
	0371-1636	7	1	KEY CAP, RT BRACE	28480	0371-1636
	0371-1637	8	1	KEY CAP, LFT BRACE	28480	0371-1637
	0371-1638	9	1	KEY CAP, QUES MARK	28480	0371-1638
	0371-1639	0	1	KEY CAP, COMMA	28480	0371-1639
	0371-1640	3	1	KEY CAP, PERIOD	28480	0371-1640
	0371-1641	4	1	KEY CAP, 8	28480	0371-1641
	0371-1642	5	1	KEY CAP, 7	28480	0371-1642
	0371-1643	6	1	KEY CAP, 6	28480	0371-1643
	0371-1644	7	1	KEY CAP, 5	28480	0371-1644
	0371-1645	8	1	KEY CAP, 4	28480	0371-1645
	0371-1646	9	1	KEY CAP, 3	28480	0371-1646
	0371-1647	0	1	KEY CAP, 2	28480	0371-1647
	0371-1648	1	1	KEY CAP, 1	28480	0371-1648
	0371-1649	2	1	KEY CAP, DELETE CHAR	28480	0371-1649
	0371-1650	5	1	KEY CAP, INSERT CHAR	28480	0371-1650
	0371-1651	6	1	KEY CAP, TILDA	28480	0371-1651
	0371-1652	7	1	KEY CAP, =	28480	0371-1652
	0371-1653	8	1	KEY CAP, 8	28480	0371-1653
	0371-1654	9	1	KEY CAP, DEL	28480	0371-1654
	0371-1655	0	1	KEY CAP, SEMICOL	28480	0371-1655
	0371-1656	1	1	KEY CAP, COLON	28480	0371-1656
	0371-1657	2	1	KEY CAP, ROLL UP	28480	0371-1657
	0371-1658	3	1	KEY CAP, NEXT PAGE	28480	0371-1658
	0371-1659	4	1	KEY CAP, ROLL DOWN	28480	0371-1659
	0371-1660	7	1	KEY CAP, PREV PAGE	28480	0371-1660
	0371-1661	8	1	KEY CAP, SM ARROW	28480	0371-1661
	0371-1662	9	1	KEY CAP, CNTL	28480	0371-1662
	0371-1663	0	1	KEY CAP, /	28480	0371-1663
	0371-1664	1	1	KEY CAP, ZERO	28480	0371-1664
	0371-1665	2	1	KEY CAP, 9	28480	0371-1665
	0371-1666	3	1	KEY CAP, RESET	28480	0371-1666
	0371-1667	4	1	KEY CAP, CAPS LOCK	28480	0371-1667
	0371-1668	5	1	KEY CAP, RECALL	28480	0371-1668
	0371-1669	6	1	KEY CAP, CLR LINE	28480	0371-1669
	0371-1670	9	1	KEY CAP, RETURN	28480	0371-1670
	0371-1671	0	1	KEY CAP, LG ARROW	28480	0371-1671
	0371-1672	1	1	KEY CAP, SHIFT	28480	0371-1672

Table 6-3. Replaceable Parts List (continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A8	64100-66524	2	1	REAR PANEL CIRCUIT BOARD ASSEMBLY	28480	64100-66524
C1	0160-2055	9	3	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C2	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C3	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C4	0180-0230	0	1	CAPACITOR-FXD 1UF+-20% 50VDC TA	56289	150D105X0050A2
CR1	1901-0040	1	1	DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
J1	1251-4040	0	1	CONNECTOR, 24-PIN HP-IB	28480	1251-4040
J2	1251-4946	5	2	CONNECTOR 25-PIN F D SUBMIN (RS-232)	28480	1251-4946
J3	0360-1946	9	1	BARRIER BLOCK 4-TERM PC BOARD POLYP	75382	4693-4
J4	1251-4946	5		CONNECTOR 25-PIN F D SUBMIN (RS-232)	28480	1251-4946
K1	0490-0617	4	3	RELAY-REED IC 250MA	28480	0490-0617
K2	0490-0617	4		RELAY-REED IC 250MA	28480	0490-0617
K3	0490-0617	4		RELAY-REED IC 250MA	28480	0490-0617
P1	0360-1706	9	1	TERMINAL, RIBBON CABLE	28480	0360-1706
Q1	1854-0215	1	1	TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
Q2	1854-0472	2	1	TRANSISTOR NPN SI DARL PD=500MW	04713	MPS-A14
R1	0757-0280	3	2	RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-TO-1001-F
R2	0757-0280	3		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-TO-1001-F
R3	0757-0346	2	9	RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-TO-10R0-F
R4	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-TO-10R0-F
R5	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-TO-10R0-F
R6	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-TO-10R0-F
R7	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-TO-10R0-F
R8	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-TO-10R0-F
R9	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-TO-10R0-F
R10	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-TO-10R0-F
R11	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-TO-10R0-F
S2	3101-1974	8	1	SWITCH-SL DPST DIP-SLIDE-ASSY .1A 50VDC	28480	3101-1974
S1	3101-2102	6	1	SWITCH-RKR DIP-RKR-ASSY 5-1A .05A 50VDC	28480	3101-2102
U1	1820-2058	3	4	IC MISC TTL S QUAD	28480	1820-2058
U2	1820-2058	3		IC MISC TTL S QUAD	28480	1820-2058
U3	1200-0607	0	4	IC SOCKET, 16 PIN		1200-0607
U4	1200-0607	0		IC SOCKET, 16 PIN		1200-0607
U5	1820-2058	3		IC MISC TTL S QUAD	28480	1820-2058
U6	1820-2058	3		IC MISC TTL S QUAD	28480	1820-2058
U7	1810-0270	6	2	NETWORK-RES 10-SIP680.0 OHM X 9	01121	210A681
U8	1810-0270	6		NETWORK-RES 10-SIP680.0 OHM X 9	01121	210A681
U9	1810-0298	8	2	NETWORK-RES 10-SIP240.0 OHM X 9	01121	210A241
U10	1810-0298	8		NETWORK-RES 10-SIP240.0 OHM X 9	01121	210A241
U11	1200-0607	0		IC SOCKET, 16 PIN	28480	1200-0607
U12	1200-0607	0		IC SOCKET, 16 PIN	28480	1200-0607
U13	1820-1917	1	1	IC BFR TTL LS LINE DRVR OCTL	01295	8N74LS240N
U14	1810-0307	0	2	CNDT JUMPER MODULE, 16 PIN	28480	1810-0307
W1	8120-3771	2	1	RIBBON CABLE, REAR PANEL	28480	8120-3771

See introduction to this section for ordering information

SECTION VII

MANUAL BACKDATING

7-1. INTRODUCTION.

7-2. There is no backdating information for the I/O chapter at the publication of this manual.

SECTION VIII

SERVICE

8-1. INTRODUCTION.

8-2. This section contains the theory-of-operation for the I/O circuits. The first part discusses the block diagram functions while the second part elaborates on these functions by referring to detailed circuit schematics and other aids such as truth tables and timing diagrams.

8-3. BLOCK DIAGRAM DESCRIPTIONS.

8-4. GENERAL. The I/O circuits are contained on the I/O Control, Keyboard and Rear-panel PC boards (see figure 8-3). The I/O Control PC board contains the control and handshake circuits for communicating over the HP-IB link to the disc and printer and the RS-232C link to the various peripheral devices connected to this bus. The I/O board also contains circuits necessary for:

1. Processing the various interrupts from the keyboard, RS-232 and HP-IB circuits.

2. Driving the beeper.

3. Allowing the CPU to select and interchange data with any of the several PC boards in the card cage.

4. Monitoring line sync and power fail status and providing such information to the CPU.

8-5. The I/O circuits are divided into four major functional areas on Figure 8-3: (1) I/O Control (upper left on the block diagram), (2) Keyboard Control (lower left), (3) HP-IB Control (upper right), and (4) RS-232 Control (lower right).

8-6. I/O CONTROL SECTION.

8-7. The I/O Control section provides most of the control functions for the other three I/O sections (i.e., HP-IB, RS-232 and Keyboard) and also serves as the data and interrupt service interface between the CPU and the other three I/O sections. Interfacing between the CPU and the I/O control circuits is accomplished via the I/O Bus and Motherboard connector J1. Interfacing with the internal I/O sections is accomplished via the internal buffered I/O bus and discrete lines (i.e., the peripheral addresses and interrupt signals shown on figure 8-3).

8-8. I/O BUS. The CPU communicates with the I/O circuits primarily via the I/O bus. This bus is a traditional bus in that it carries data, address and control information. The data bus is a 16-bit bi-directional bus that carries data to and from the HP-IB interface chip, the RS232 interface chip, and the Low Priority Interrupt circuit. This bus also receives data from the keyboard circuits and switch mode status from the RS-232 circuits.

8-9. The address portion of the I/O bus consists of 4-bits of peripheral address (LPA0-LPA3). These bits allow up to 16 peripheral addresses to be decoded (by the Peripheral Address Decoder) which allows the CPU to select the various I/O circuits it wants to talk to. However, only 9 of the possible 16 peripheral addresses are used in the 64000 system (see Table 8-1).

Table 8-1. I/O Internal Addresses

MNEMONIC	FUNCTION
LKYBD	Keyboard Address
L(DELTA)T	Time Interval Address
LRSWR	RS-232 Write Address
LRSRD	RS-232 Read Address
LHP-IB	HP-IB Select and Read/Write Control Address
LBEEP	Beeper Select Address
LSSEL	Card Slot Select Address
LIMASK	Sets Interrupt Mask Latch Address
LPFS	Power Fail Set Address

8-10. BEEPER, SA INTERVAL, CARD ID ENABLE AND DISPLAY ENABLE. In addition to the nine peripheral addresses, there are two interface control addresses (LIC1 and LIC2) that the CPU uses to control the beeper, the signature analyzer start-stop signals (SA INT) and the card ID address decoder. This latter circuit produces the ID enable signal (LIDEN) that is distributed to each of the option card slots where it enables the various option PC boards to communicate their unique identification codes to the CPU.

8-11. The output of the Beeper Decoder is sent to the Display Enable Latch and the beeper circuits. When the first beeper signal is generated (by signals LBEEP, LDOUT, LIC1 and LIC2), a binary "1" is latched into the display enable latch and causes the CRT to be activated by HDE (display enable). This latch keeps the CRT display enabled until power is turned off or when a power failure is eminent as indicated by the high priority interrupt flag (LIR15). This flag resets the display enable latch causing the CRT to go blank and also sets the high priority interrupt latch (when interrogated by peripheral address Power Fail Set, LPFS). This in turn causes the high priority interrupt signal (LIRH) to be sent to the CPU (via the I/O bus) .

8-12. LOW PRIORITY INTERRUPT LOGIC. The low priority interrupt circuitry is a series of gates and latches. By generating a particular peripheral address (LKYB, LRSRD, LRSWR, or LBEEP), the CPU can turn on I/O Data Buffers U2/U4. It writes an interrupt mask into this logic, and then the low priority interrupt (LIRL) will only be generated when one of the enabled (unmasked) circuits requests an interrupt. When this happens, the CPU again enables I/O Data Buffers U2/U4 and reads the "Interrupt ID" to determine which circuits have requested the interrupts. Once it determines this, the CPU then writes out another peripheral address to the device which will service the circuit that requested the interrupt.

8-13. DELTA TIME LATCH. This circuit monitors (counts) the 60Hz line sync pulses (LINE SYNC) from the power supply and simultaneously sends a low level interrupt (HIR2) to the CPU during each sync pulse. If the CPU becomes "lost" (i.e., loses track of time) and doesn't respond with peripheral address L(DELTA)T before 128 pulses have been counted (approx. 2.2 seconds), the Delta Time Latch circuit triggers the Auto Reset circuit which in turn generates the LPOP reset signal. LPOP is routed to the seven I/O circuits listed below where it serves as a reset pulse:

1. SA Latch
2. High Priority Interrupt Latch
3. Power Fail Latch
4. Delta-Time Counters
5. Slot-Select Address Latch
6. Interrupt Mask Latch
7. PHI Address Latch

8-14. HIGH PRIORITY INTERRUPT LATCH. Whenever power is about to fail, the Power Supply sends interrupt request signal LIR15 to the high priority interrupt latch. This produces high priority interrupt request LIRH which is sent to the CPU to inform it that power is failing. The CPU then responds with the appropriate address code for generating the power fail set peripheral address (LPFS).

8-15. POWER FAIL SET LATCH. The power fail set address (LPFS) sets the power fail set latch thus producing the power fail signal LPFAIL. This signal is sent to the auto-reset circuits where it disables the output from the delta-time counters. The purpose of disabling the delta-time counters is to inhibit the generation of power-on pulse LPOP. This in turn prevents the CPU cicuits from being reset during a power-fail condition.

8-16. AUTO RESET CIRCUIT. This circuit produces the power-on signal (LPOP) whenever either of two events occur: (1) when the delta-time counters are allowed to time-out due to the CPU taking too long to respond to the sync-pulse interrupts, and (2) when the processor reset switch is pressed. The delta-time feature is disabled by either the power-fail signal (LPFAIL) or by the Auto-Reset Enable jumper E8 (on the I/O board).

8-17. I/O DATA BUFFERS. The I/O data buffers are bi-directional transceivers that interface the I/O bus with the buffered I/O bus. These transceivers allow communication between the CPU and the various I/O circuits.

8-18. SLOT SELECT ADDRESS LATCH AND DECODER. This circuitry provides the ability to address up to 48K specific locations on each of the option cards occupying any of the 10 option card slots. This is accomplished by decoding four I/O address bits from the CPU (the other two bits indicated on figure 8-3 are for enabling the decoder chip) thus producing a total capability of selecting 1 of 16 outputs (only 11 are used). Each of these 11 card-slot select signals (LSS0 thru LSS10) is routed to a specific card slot in the cardcage where it causes that particular card slot to be enabled. Slot Select signal LSS10 is routed to the Display Controller and CPU card slots but has no function.

8-19. HP-IB CONTROL SECTION.

8-20. GENERAL. This circuitry allows the CPU to communicate over the Hewlett-Packard Interface Bus (HP-IB) with peripheral devices that are designed to be compatible with the IEEE 488 general purpose interface bus. However, since the 64000 operating system (software) incorporates instruction code only for the HP 7910, 7906, 7920, 7908 and 7925 disc Drives and the HP 2631A and 2608 Line Printers. Thus, these are the only peripheral devices that can be driven from the HP-IB bus.

8-21. CONTROL LOGIC, ADDRESS LATCH AND STATUS BUFFER. The Control Logic decodes four control signals (LIC1, LIC2, LDOUT, and LBEEP) and produces a set of outputs that control the selection of Status Buffer U12, Address Latch U11, and PHI chip U20. Address latch U11 stores I/O bits 8-11 which are used to select specific registers internal to the PHI chip. Status Buffer U12 reads (stores) the status of Rear-panel Switch S1. Switch S1 controls the system "boot-up" source (i.e., disc, local mass storage, or performance verification). Switch S1 also selects the desired ID address for the subject mainframe (see figure 8-2). Switches S2 and S3 determine controller (MASTER) or non-controller (SLAVE) station status.

8-22. PHI CHIP U20. The acronym "PHI" stands for Processor to HP-IB Interface. This chip is a self-contained microcontroller that adapts a wide variety of microprocessor chips to the HP-IB bus. Some of the general characteristics of the PHI chip are: (1) data is sent at the rate of the slowest listener (up to one megabyte per second), (2) data transfer is asynchronous, and (3) more than one peripheral device can accept data simultaneously. To ensure that the transfer of data is accomplished in an orderly manner, a set of three "handshake" signals are used: Data Valid (DAV), Ready for Data (RFD), and Data Accepted (DAC). These three handshake signals ensure: (1) that each listener is ready to accept data, (2) that the data on the data bus in valid, and (3) that the data has been accepted by all listeners.

8-23. BUFFERS/INVERTORS. HP-IB Data XCVRS, and Bus Loads. The transmit control signals from the PHI chip are buffered and inverted by U9 before being sent to the HP-IB Data Transceivers. These signals control channel selection and the direction of data flow thru the data transceivers. The HP-IB Data Transceivers are bi-directional and handle three types of signals: (1) HP-IB data, (2) handshake, and (3) bus management. The HP-IB data consists of instructions and data that are passed back and forth between the CPU and the peripheral devices on the HP-IB bus (i.e., printer or disc). The handshake signals were discussed above and are used to control and coordinate the transfer of data. The Bus Management signals consist of five control/status signals that are used for such things as activating all peripheral devices at the same time, clearing the interface, service request, etc. The Bus Loads block represents a resistive load that can be applied or removed from the data lines. The two states are controlled by switches S2 and S3. In one position, the subject Mainframe is configured as the "master" controller station and in the other position it is a "slave" non-controller station.

8-24. RS-232 CONTROL SECTION.

8-25. GENERAL. This circuitry allows the CPU to communicate over the RS-232C serial interface bus to peripheral devices that require this type of interface. In addition, this section also allows selecting the "current loop" mode of operation for interfacing with teletypes and other peripherals that require this type of electrical interface.

8-26. RS-232C STANDARD. Most voltage interfaces in North America conform to the EIA RS-232C Interface Standard (the corresponding European standard is CCITT V24). This standard specifies a 25-pin connector as the standard interface in datacomm networks, with lettered pin assignments for ground, data, control and timing circuits. The standard also specifies the mechanical and electrical requirements of an interface, within an operating range of 0 to 20,000 bps in bit-serial operation, synchronous or asynchronous. It provides interface compatibility between many types of equipment and manufacturers and thus provides great flexibility in the selection of equipment for datacomm networks.

8-27. BUFFER AND RS-232 MODE SWITCHES. Buffer U35 reads the status of RS-232 Mode Switches S4 and S3 on the I/O board. Switch S3 controls the selection of the RS-232 or current loop modes while S4 controls the following five parameters (see figure 8-1):

1. The number of stop bits (1, 1.5 or 2)
2. Type of parity (odd, even or none)
3. Character length (5-8 bits)
4. Baud rate factor (X1 or X16)
5. Terminal or Modem

8-28. BAUD RATE SWITCHES AND GENERATOR. Switch S5 on the I/O board allows the operator to select the baud rate at which the RS-232 data is transmitted and received by the RS-232 circuitry. Sixteen discrete rates can be selected within the range of 50 to 19200 baud (See figure 8-1). Switch S5 has five segments. The first of which selects full duplex or half duplex operation while the remaining four segments control the baud rate by selecting the operating frequency of Baud Rate Generator U48. The output of the Baud Rate Generator is applied to a divider circuit that is controlled by a segment of switch S4 to select the baud rate factor (X1 or X16).

8-29. CLOCK SOURCE SWITCH AND JUMPERS. The 64100A RS-232 circuits have the capability to drive or receive both the TX and RX clocks independently. Control of these options is provided by switch S2, and jumpers E1 and E2, on the I/O board. This option allows the operator to select the source of transmit and receive clocks for the USART chip U28. The dual SPDT dip switch S2 selects, independently for TX and RX, whether the clock for the USART is supplied by the internal baud rate generator or from an external remote terminal or modem type equipment. The following is how the switch and jumpers must be configured to take advantage of this option:

a. When the RXCLK switch is set for internal clock, the E1 jumper does the following:

   1. If the RS-232 cable is connected to the PERIPHERAL connector, on the Rear-panel, placing a jumper from A to B will connect the TXCLK on J2, pin 15.

   2. If the RS-232 cable is connected to the MODEM connector, placing a jumper from B to C will supply the identical clock on the RXCLK output on J4, pin 17.

   3. If an output clock is not desired then no jumper is required.

b. When the TXCLK switch is set for internal clock, the E2 jumper does the following:

   1. With the RS-232 cable connected to the PERIPHERAL connector, on the Rear-panel board, placing a jumper from A to B supply the RXCLK on J2, pin 17.

   2. With the RS-232 cable connected to the MODEM connector, placing a jumper from A to C will supply the clock on the TXCLK output of J4, pin 15.

   3. If an output clock is not desired then no jumper is required.

c. If the RXCLK switch is in the external clock position then the E1 jumper does the following:

   1. With the RS-232 cable connected to the PERIPHERAL connector, a jumper from A to C is required to receive TXCLK from J2, pin 15.

   2. If the RS-232 cable is connected to the MODEM connector, no jumper is required to receive RXCLK from J4, pin 17.

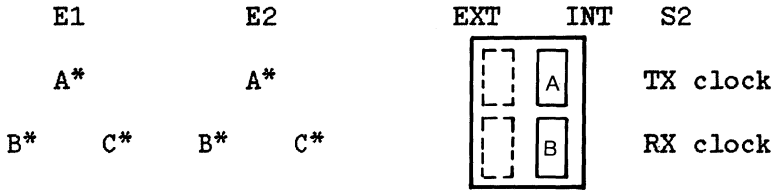
d. With the TXCLK switch set to external clock then the E2 jumper does the following:

   1. With the RS-232 cable connected to the PERIPHERAL connector, a jumper from A to C is required to receive RXCLK from J2, pin 17.

   2. If the RS-232 cable is connected to the MODEM connector, a jumper is not required to receive TXCLK from J4, pin 15.

NOTE

The E1 jumper corresponds with the RX clock switch. The E2 E2 jumper corresponds with the TX clock switch.



8-30. MODE SELECT AND DRIVE. The RS-232C transmit and receive data passes through the mode select switches and drive circuitry. The mode select switches allow the operator to select: (1) Current Loop or RS-232, (2) Full Duplex or Half Duplex, and (3) 20mA or 60mA (current loop) modes of operation.

8-31. LOOP-BACK TEST FEATURE. To test the RS-232 circuits during performance verification, the transmitted data and handshake signals are "looped-back" to the RS-232 circuits as "receive" data. This feature is under software control and is used during the RS-232 segment of the PV test.

8-32. KEYBOARD CONTROL SECTION.

8-33. GENERAL. This circuitry allows the operator to interface with the CPU and Operating System Software via the Mainframe Keyboard. The Keyboard consists of four blocks of keys: (1) a 128-character ASCII main keyboard, (2) 10 edit keys, (3) four special function keys, and (4) eight softkeys. The function of these keys are described in the 64000 system operating manual.

8-34. DATA BUFFER. This 8-line buffer connects the 7-bit key address code from the Keyboard Address Counter and the key status bit (bit 7) onto the internal I/O bus when the CPU produces peripheral address LKYBD. This is a uni-directional buffer and is enabled as a result of an interrupt request from the keyboard circuits (i.e., a change in key status).

8-35. BASIC CONCEPT. The State Machine is clocked by HSTB from the CPU and sequentially generates a series of strobe signals that: (1) clock the Keyboard Strobe Generator, (2) clock the Keyboard Address Counter, (3) activate the Past State Memory and control the read/write functions, and (4) clock he interrupt Latches. The general concept is to sequentially step the Keyboard Address Counter through its entire counting range of 255 and applying this count code simultaneously to a one-bit wide RAM (Past State Memory) and also to a 1-of-16 column selector (U1/U2) and a 1-of-8 row selector (U7).

8-36. The row and column selectors select a X-Y coordinate on the keyboard which in effect reads the status of a specific key for each step of the address code. This status information (i.e., key up or key down) is encoded in signal HKYDN which is sent to the interrupt latches where it is stored momentarily. The chip select signal from the state Machine causes the "present-state" key status to be stored in the RAM in a specific location that is a function of the address code of the current key being interrogated. When the Keyboard Address Counter completes a complete cycle, the address location that initially stored the "present state" data is now caused to read this data out of RAM as "past state" data. The past state status is compared with the present state status by the interrupt Latches. If the present state and past state are not the same, this indicates that the key status has changed and an interrupt request (HIRKB) is sent to the CPU. Simultaneously, a stop signal is sent to the State Machine which causes the Address Counter to stop on the address of the subject key. When it has time, the CPU responds with the keyboard peripheral address (LKYBD) which enables Data Buffer U27 and puts the address code on the I/O bus so that the CPU can determine which key is involved. LKYBD also resets the interrupt Latches thus enabling the State Machine and allowing the address cycling to begin again.

8-37. An "n-key" scanning techinque is used when scanning the keyboard. This means that any number of keys can be depressed or released in any order or at any time and the keyboard interrupts will be processed rapidly enough to prevent missing any status changes.

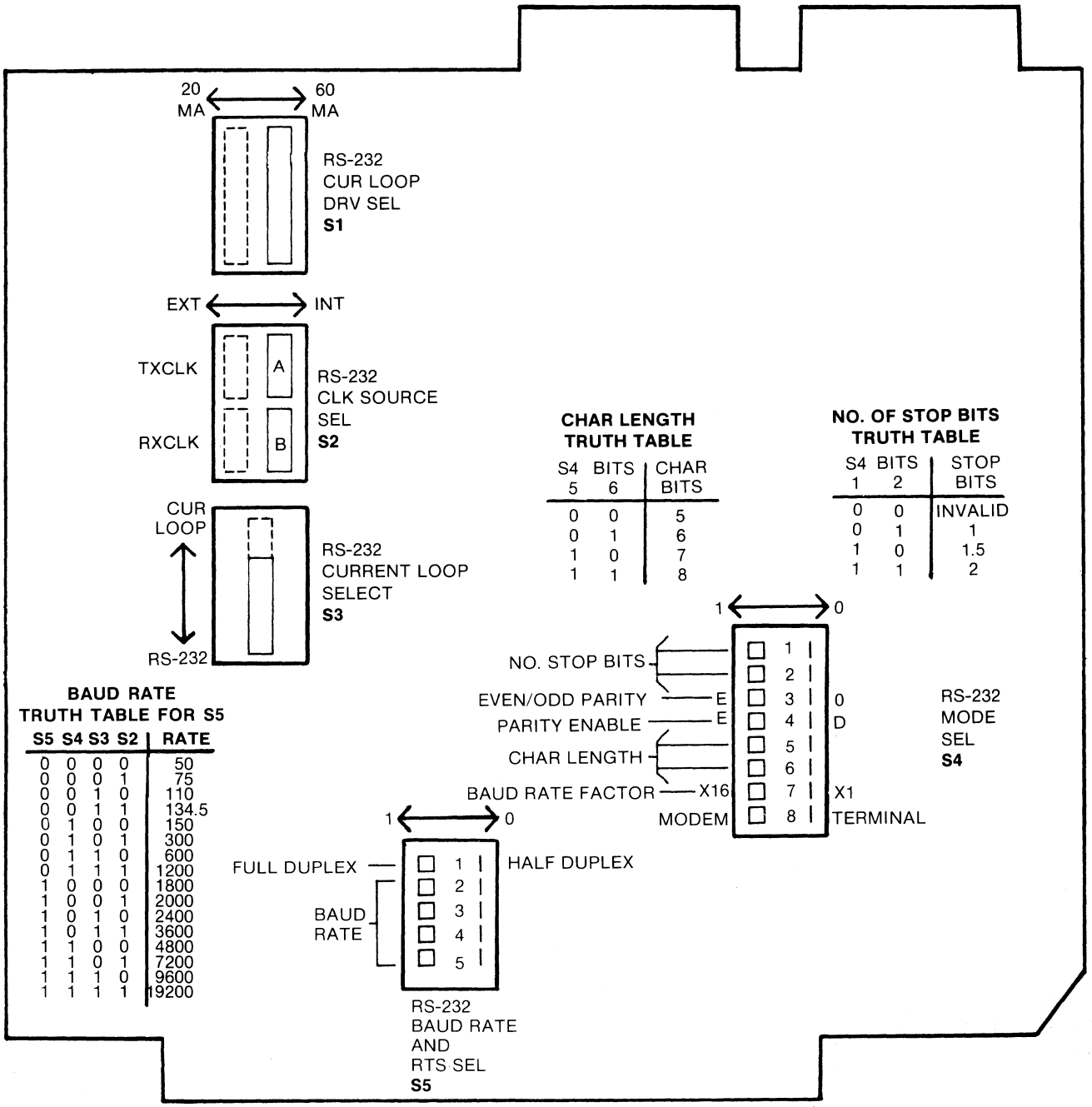
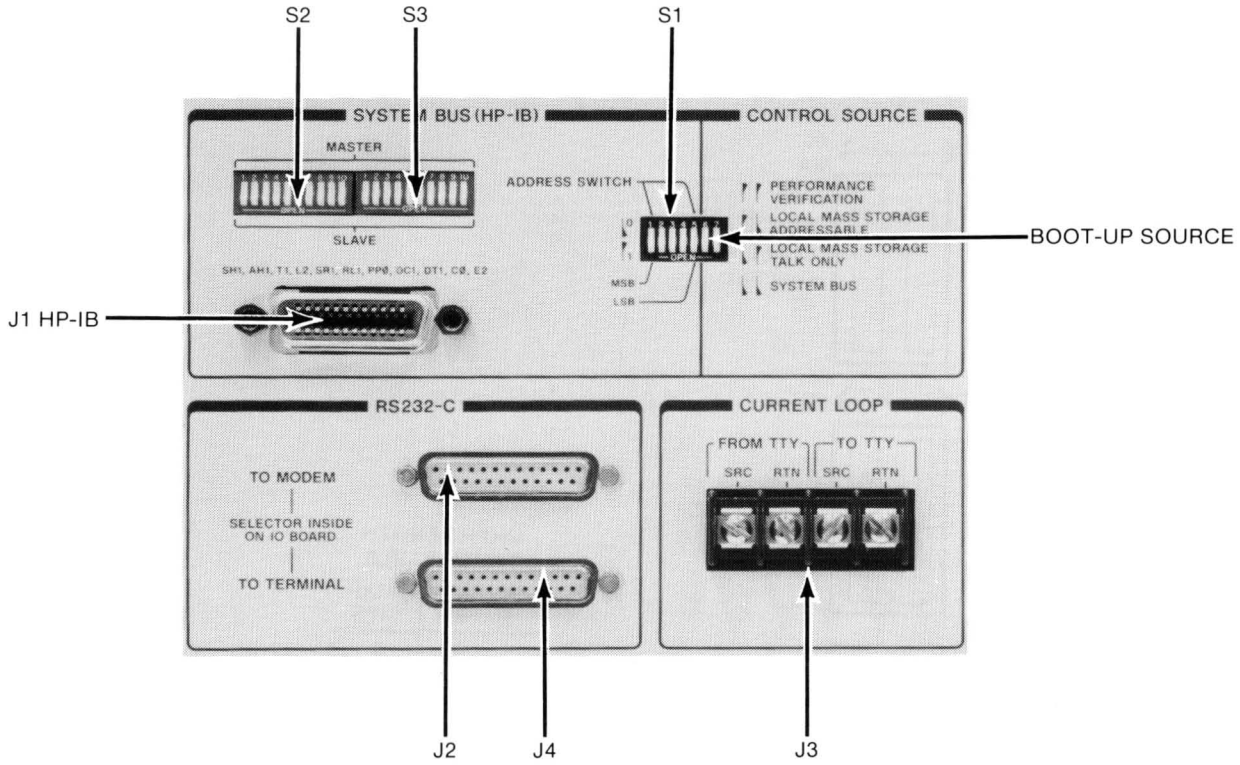


Figure 8-1. I/O PCB Switch Locations and Functions



BOOT-UP SOURCE ADDRESSES

MSB	LSB	CONTROL
0	0	SYS BUS (DISC)
0	1	LOCAL MASS STORAGE TALK ONLY
1	0	LOCAL MASS STORAGE ADDRESSABLE
1	1	PERFORMANCE VERIFICATION

MAINFRAME ADDRESSES

NOT USED	MSB		LSB	ADDRESS	
00	0	0	0	0	
					NOT VALID
00	0	0	1	1	
00	0	1	0	2	
00	0	1	1	3	VALID
00	1	0	0	4	MAINFRAME
00	1	0	1	5	ADDRESSES
00	1	1	0	6	
00	1	1	1	7	

Figure 8-2. Rear-panel Switch Locations and Functions

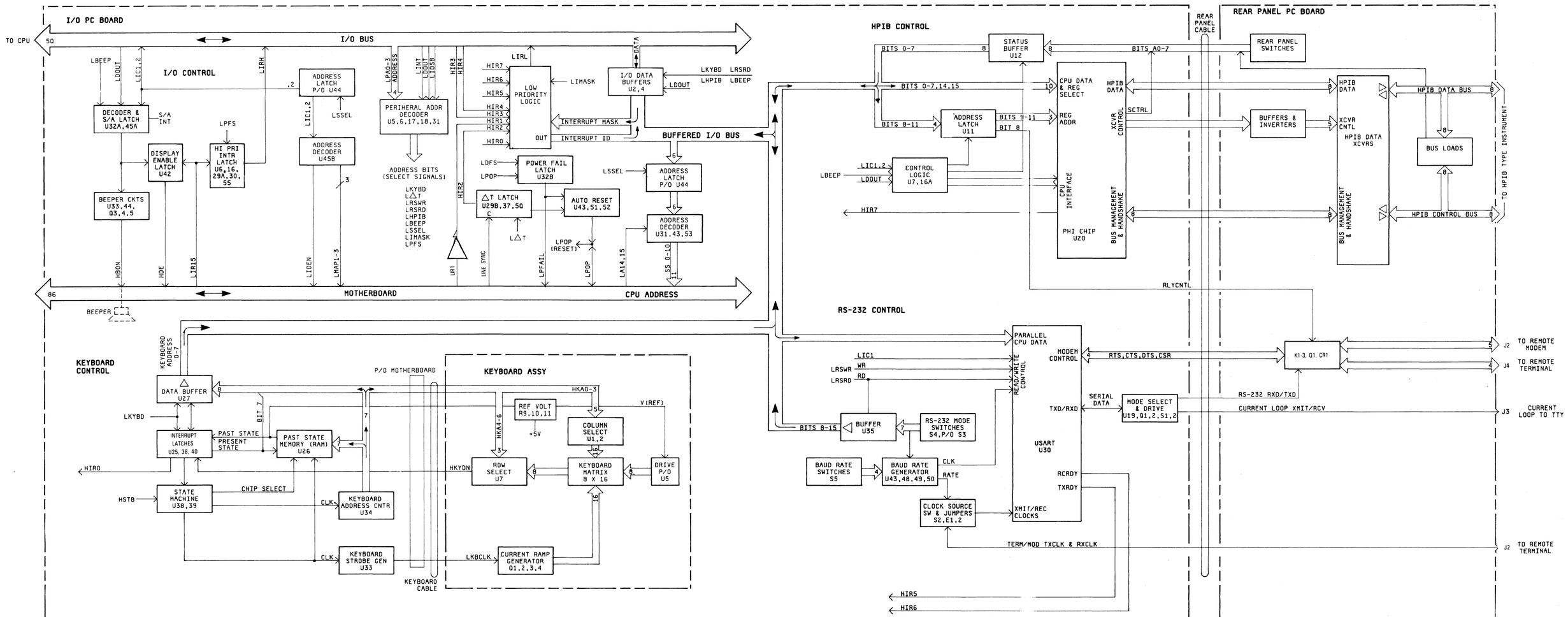


Figure 8-3.
I/O Block Diagram
I/O 8-11

8-38. SCHEMATIC DESCRIPTIONS.

8-39. This section provides additional detailed information concerning the I/O circuits that was not appropriate for the Block Diagram description. This includes more details on how the various circuits perform the specific functions. Logic truth tables and timing diagrams are used to illustrate some of the relationships. Schematics are provided on 5 sheets, figure 8-14.

8-40. LOGIC CONVENTION. The positive logic convention is used for logic variables and the circuits comprising the 64100A I/O circuits. This convention defines a logic 1 as the more positive voltage (high) and a logic 0 as the more negative voltage (low). Most integrated circuit logic devices in the 64100A are 7400 devices and ultilize transistor-to-transistor logic (TTL) levels. Ideally, the low and high voltage levels for 7400 devices are 0V and +5V, respectively. But due to voltage drops over the interconnecting PC board traces and other causes, the actual levels can vary from these ideal values. Therefore, the voltage levels for a logic 1 and 0 are defined as follows:

TTL VOLTAGE LEVELS

BINARY QUANTITY		VOLTAGE LIMIT
Input	0	< 0.8V
Input	1	> 2.0V
Output	0	< 0.4V
Output	1	> 2.4V

8-41. MNEMONICS. Signals in the 64100A have been assigned mnemonics that describe the active state and function of the signal line (see table 8-12). A prefix letter (H or L) or superscript bar is used to indicate the active state of the signal and the remaining letters indicate its function. A "H" prefix or the absence of a bar indicates that the function is active in the "high" state; a "L" prefix or the presence of a bar above a mnemonic indicates that the function is active in the low state.

8-42. SIGNATURE ANALYSIS LOOPS. The letters on the I/O schematics identify circuit nodes where signature analysis "signatures" have been taken to aid in troubleshooting the logic circuits. Refer to Section IV for instructions on how to use signature analysis for troubleshooting.

8-43. I/O CONTROL.

8-44. BEEPER DECODER U45A (see figure 8-14, sheet 1)

U45A is a 2-to-4 line decoder that decodes the LDOUT and LIC1 commands from the CPU for the purpose of generating the SA start-stop interval and activating the beeper circuits. Peripheral command LBEEP from U17 enables this decoder when the CPU Operating System has determined the proper conditions exist. Table 8-2 is the Truth Table for U45A.

Table 8-2. Beeper Decoder U45A Truth Table

G LBEEP	F1 LIC1	F2 LDOUT	Output Pins				
Pin 15	Pin 13	Pin 14	12	11	10	9	Function Activated
1	X	X	1	1	1	1	None
0	1	0	1	1	0	1	Beeper & Display
0	1	1	1	1	1	0	S/A Interval

8-45. BEEPER START PULSE GEN U33. Monostable multivibrator U33 is triggered when LBEEP and LIC1 are true and LDOUT is false (see table 8-2). When triggered, U33 generates a pulse approximately 220 milliseconds in duration which turns Q3 on and causes C33 to rapidly charge up to +5 Vdc thru R24. When the U33 output pulse terminates, C33 exponentially discharges thru R25 thus creating a pulse that has a steep leading edge and a sloping trailing edge which causes the beeper to produce a "bell" sound. This pulse turns on Q4 thus providing +5 Vdc (HBON) to one side of the beeper speaker.

8-46. 2500 HZ TONE GENERATOR U41. Timer U41 is a monolithic timing circuit that is operated in the astable (free running) mode to generate a 2500 Hz tone. The tone frequency is determined by R29, R30 and C35. The output of U41 controls Q5 which in turn modulates the five volts, appearing across R27, with the 2500 Hz tone signal.

8-47. DISPLAY ENABLE LATCH U42. Latch U42 is set simultaneously with the activation of the Beeper Start Pulse Generator. When U42 is set, the Display On signal (HDE) is produced which is sent to the Display Driver PCB to activate the CRT display. U42 is reset whenever system power is cycled OFF and ON and whenever a power interrupt (LIR15) is generated by the mainframe power supply.

8-48. SA LATCH U32A. This is one-half of a D-type flip-flop that has interface command LIC2 as its D input and is clocked by the pin 9 output of Decoder U45A (see table 8-2). The output of U32A is fed to test point TP2 and serves as the SA start-stop signal for troubleshooting the I/O circuits. U32A is reset by power-on pulse LPOP.

8-49. CARD ID LATCH AND DECODER U44 AND U45B. Latch U44 is a D-type flipflop, a portion of which is used for storing interface commands LIC1 and LIC2 when the CPU causes peripheral address LSSEL to occur. The remaining segment of U44 is used for latching the address bits for generating the card slot select commands (see Slot Select circuit description).

8-50. The two outputs on pins 12 and 15 of U44 are fed to decoder U45B where they are decoded into four discrete signals: ID Enable (LIDEN) and MAP commands LMAP1 thru LMAP3. Signal LIDEN is output on pin 67 of J1 and enables the option card ID circuits for the PROM Controller, Emulation Memory Control, Logic Anayzer, and Emulation Control that may be located in any of the ten option card slots. The three MAP signals serve as address lines for future expansion of the option card memory capabilities. Table 8-3 is the truth table for U45B.

Table 8-3. Card ID Decoder U45B Truth Table

LIC2	LIC1	LIDEN	LMAP1	LMAP2	LMAP3
0	0	0	1	1	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	1	1	1	0

8-51. PERIPHERAL DECODER ENABLE LOGIC U5, U6, U31. The I/O strobe (LIOSB), Interrupt (LINT), Data Out Delayed (LDOUTD), and Data Out (LDOUT) commands from the CPU are ANDed by U31B and U31C and then ORed by U31D to produce an enable signal for enabling Peripheral Address Decoders U17 and U18. This enable signal appears at output pin 12 of U31D and is fed to gate input pin 5 of both U17 and U18 (Note, however, that the two other gate inputs to U17 and U18 must also be of the proper state). Table 8-4 is the truth table for the Decoder Enable Logic.

Table 8-4. Decoder Enable Logic Truth Table

LIOSB	LDOUT	LINT	LDOUTD	U31D-13 OUTPUT
0	0	X	X	0
X	X	1	1	0

U31D-13 = 1 for all other combinations

8-52. PERIPHERAL ADDRESS DECODERS U17, U18. Decoders U17 and U18 decode one-of-eight lines each (for a maximum capability of 16 lines) depending on the states of the three binary select inputs (pins 1, 2, and 3) and the three enable inputs (pins 4, 5 and 6). The same address inputs can be used for both decoder chips because only one chip is enabled at a time. This is implemented by feeding peripheral address signal LPA3 to the low true enable input of U18 and to the high true enable input of U17. This means that U17 and U18 are never enabled at the same time. Also, note that pin 4 of U17 is tied to ground thus requiring that only pins 5 and 6 be low for U17 to be enabled.

8-53. Although U17 and U18 have the capability of decoding up to 16 lines, only 9 are used in the current 64100A system application. Five of the peripheral addresses (LKYBD, L(delta)T, LRSWR, LRSRD, and LHPIB) are produced by U18 and the remaining four addresses (LBEEP, LSSEL, LIMASK, and LPFS) are produced by U17. Table 8-5 is the truth table for U17 and U18. Notice in this table that the address selected depends both on the state of the peripheral addresses binary outputs (LPA0 thru LPA2) and also LPA3 which determines which decoder chip (U17 or U18) is enabled.

Table 8-5. Peripheral Address Decoder
U17/U18 Truth Table

U17/U18 SELECT	ADDRESS FROM CPU U17 U17 U18	U18 U17 U18	PERIPHERAL ADDRESSES U18 U18 U17 U18
	LPA3 LPA2 LPA1 LPA0 LBEEP LKYBD	HPIB/LPFS	LRSRD LRSWR LIMASK L T/LSSEL
0=HP-IB	0 0 0	0	1 1 1 1
1=LPFS	0 0 0	0	1 1 1 1
0=LRSRD	0 0 1	1	0 1 1 1
0=LRSWR	0 1 0	1	1 0 1 1
1=LIMASK	0 1 1	1	1 1 0 1
0=L T	1 0 1	1	1 1 1 0
1=LSSEL	1 0 1	1	1 1 1 0
1=LBEEP	1 1 0	1	1 1 1 1
0=LKYBD	1 1 1	1	1 1 1 1

8-54. INTERRUPT BUFFER ENABLE LOGIC U16, U30. Inverters U16F and U16D together with gates U30A and U30B decode LPA3, LINT and LDOUTD to produce the Interrupt Buffer Enable signal (LIBE). Table 8-6 is the truth table for LIBE.

Table 8-6. Interrupt Buffer Enable Truth Table

LPA3	LINT	LDOUTD	LIBE
1	0	1	0

LIBE = 1 for all other combinations

8-55. HIGH PRIORITY INTERRUPT LATCH U29A. This latch is a D-type flip-flop that is clocked by the negative-going edge of Power Fail Interrupt (LIR15) and set by either LPOP or peripheral address LPFS.

8-56. Latch U29A is set by HPOP at system power-up (or by pressing the Reset Test switch). This is done by HPOP passing thru OR gate U30D, invertor U55F and on to the set input of U29A, pin 4. Latch U29A remains in the set state until a power fail interrupt (LIR15) occurs. When the power supply senses that a power failure is eminent, LIR15 goes low which is inverted by U55C before clocking U29A. The clocking of U29A causes output pin 6 (HLIRH) to go high which is inverted by U6G thus producing the high priority (unmaskable) interrupt signal LIRH. This signal is sent via the I/O bus to the CPU and informs the controller that power is failing.

8-57. After receiving the message that power is failing, the CPU responds by writing to Peripheral Address Decoder U17/U18 to produce the Power Fail Set (LPFS) address. The LPFS bit performs two functions: (1) it sets Power Fail Latch U32B to disable the LPOP Pulse Generator U52, and (2) it sets High Priority Interrupt Latch U29A thus canceling the high priority interrupt caused earlier by LIR15.

8-58. DELTA-T INTERRUPT LATCH U29B. The 60/50Hz LINE SYNC signal from the Power Supply enters on pin 75 of J1 and is buffered by U54F before being applied to D-type flip-flop U29B and modulo-16 counter U37A. Latch U29B is clocked by each positive-going edge of LINE SYNC thus causing the Q output at U29B-9 to latch high due to the D input of U29B being tied to +5 Vdc. The Q output of U29B is interrupt signal HIR(Delta). It is routed to the Low Priority Interrupt Logic and causes a low priority interrupt (LIRL) to be sent to the CPU via the I/O bus. After a nominal delay, the CPU responds with peripheral address L (Delta) T which resets latch U29B which in turn causes HIR (Delta) T to go low and reset counters U37A and U37B.

8-59. If the CPU takes longer than 2.24 seconds (2.6 seconds for 50Hz line frequency) to respond with the L(Delta)T address, the Delta-T Interrupt Timers (U37A and U37B) will time-out thus producing a high output on U37B-8 which is fed to gate U51D. The output to U51D-11 then goes low and is routed thru U54 (assuming the Auto Reset Enable mode is selected) to the A2 trigger input of LPOP Pulse Generator U52. The triggering of U52 causes the LPOP signal to be produced which in turn resets all of the circuits to which it is tied.

8-60. DELTA-T INTERRUPT COUNTERS U37A/B. Binary counters U37A and U37B are each modulo-16 counters that are a modulo-128 counter. Counter 37A is incremented one count by each occurrence of LINE SYNC. When this counter reaches a count of 8, pin 8 goes high. At a count of 16, pin 8 goes low at which time U37B is incremented. When U37B has been incremented 8 times, its pin 8 output goes high which corresponds to 16X8=128 pulses of LINE SYNC or about 2.2 seconds for a line frequency of 60Hz. If the output of U37B is allowed to go high (i.e., time out) before being reset by the occurrence of L(Delta)T, the LPOP reset signal is generated.

8-61. POWER FAIL LATCH U32B. Latch U32B is a D-type flip-flop that is clocked by each occurrence of LPOP (i.e., at system power-on and any time the Mainframe is reset). LPOP causes output pin 8 to latch high which enables NAND gate U51D thus enabling the output from counter U37B.

8-62. If a Power Fail Set (LPFS) address is received from the Peripheral Address Decoder as a result of the CPU responding to a power fail interrupt request (LIR15), latch U32B is set thus causing output pin 8 to latch low.

8-63. MANUAL RESET DE-BOUNCE LATCH U43. This circuit is latched with the first contact closure of the Processor Reset Switch and thus prevents multiple triggering (due to contact bounce) of LPOP Generator U52 when the system is manually reset.

8-64. LOW PRIORITY INTERRUPT LOGIC U22,23,23,14,21 (see figure 8-13, sheet 2). The eight, low priority interrupts are gated thru NAND gates U23 and U24. These gates can be disabled (masked) by the CPU as a result of latching the masking code into the Interrupt Mask Latch U14. Latching is under CPU control (i.e., enabled) by means of peripheral address LIMASK from U17. Latch U14 is cleared by LPOP.

8-65. The unmasked interrupts are routed to Interrupt Data Buffer U21 and also are ORed by U22 to produce low priority interrupt signal LIRL. This signal is routed to the CPU and causes the CPU to initiate an interrupt poll to determine which peripheral device requested the interrupt. The interrupt poll consists of the CPU sending interrupt signals LINT and LDOUT to the 16-bit wide I/O Data Transceivers U2 and U4 via OR gate U15B. LINT enables the two transceivers while LDOUT controls the direction of data flow which in this case is back towards the CPU. LIBE enables buffer U21 to put the interrupt code on the I/O data lines. The format of the interrupt code sent to the CPU identifies the device that requested the interrupt (i.e., the location of the logic 0 in bits LIOD0 thru LIOD7 identifies the interrupting device). Table 8-7 shows the ID code for the eight interrupts.

Table 8-7. Interrupt ID Codes

	I/O Data Bits							
Interrupting Device	7	6	5	4	3	2	1	0
HP-IB	0	1	1	1	1	1	1	1
RS-232 Receive	1	0	1	1	1	1	1	1
RS-232 Transmit	1	1	0	1	1	1	1	1
(not used)	1	1	1	0	1	1	1	1
Local Mass Storage	1	1	1	1	0	1	1	1
Delta Time	1	1	1	1	1	0	1	1
Emulator	1	1	1	1	1	1	0	1
Keyboard	1	1	1	1	1	1	1	0

8-66. I/O DATA TRANSCEIVERS U2, U4. I/O data and instructions are routed thru transceivers U2 and U4 to the various I/O circuits that require communications with the CPU. This includes the Low Priority Interrupt Logic, Card Slot Select Logic, HP-IB Controller, RS-232 Transceiver, and the Keyboard. These two transceivers are bi-directional and are each 8 bits wide. The transceivers are enabled by either LDOUT or LINT or by any of the following peripheral addresses: LKYBD, LRSRD, LRSWR, or LBEEP. The direction of data flow is controlled by LDOUT where the flow is to the CPU when LDOUT = 1 and from the CPU to the I/O circuits when LDOUT = 0.

8-67. SLOT SELECT LATCH U44. Latch U44 consists of six segments of an 8-element D-type flip-flop (the other two sections serve as the Card ID Latch). Its purpose is to latch (store) I/O address bits 8-13 and is under CPU control (i.e., enabled) via peripheral address LSSE1. When the CPU wants to store I/O bits 8-13, it causes the LLSEL perpheral address line to be pulsed. This causes I/O bits 8-13 to be latched at the positive-going edge of LLSEL.

8-68. SLOT SELECT DECODER U53. Address bits 8-11 from latch U44 serve as the address input to Slot Select Decoder U53. Address bits 12 and 13 from U44 are combined with CPU addresses LA14 and LA15 to provide the chip select function of U53 as shown in truth table 8-8.

Table 8-8. Slot Select Decoder U53 Enable Truth Table

I/O Bits		CPU Address Bits		
13	12	LA15	LA14	U53 Selected
0	0	1	0	Yes
All other conditions				No

8-69. Decoder U53 is a 4-line to 16-line decoder that decodes the four input address lines (in the Model 64100A only eleven of the 16 outputs are wired). Each of the eleven outputs from U53 (LSS0-LSS10) is routed to pin 72 of each of the option card slots as follows:

LSS0	J4-72	LSS6	J10-72
LSS1	J5-72	LSS7	J11-72
LSS2	J6-72	LSS8	J12-72
LSS3	J7-72	LSS9	J13-72
LSS4	J8-72	LSS10	J2/3-72 (not used)
LSS5	J9-72		

8-70. A truth table for U53 is unnecessary since the ANSI chip symbol defines the input addresses and corresponding output line selected.

8-71. HP-IB CONTROL.

8-72. REAR-PANEL SWITCH BUFFER U12 (see figure 8-14, sheet 3). This is an uni-directional, 8 channel buffer that relays the status of the Rear-panel mode control switch S1 to the CPU. Control is provided by the PHI Control Logic.

8-73. ADDRESS LATCH U11. This is a D-type flip-flop that is used to store four bits (HIOD8-HIOD11) of the I/O address data. Bits 9-11 control the selection of the PHI chip internal address registers while bit 8 serves to control the RS-232 loop-back test feature.

8-74. PHI CONTROL LOGIC U7. This circuit is an array of four NAND gates (U7A-U7D) that decode five input control signals from the CPU. Its purpose is to control the selection of Rear-panel Switch Buffer U12, Address Latch U11, and PHI chip U20. The five input control signals are: HDOUTD, LIC1, LIC2, LDOUT and LHP-IB. Truth table 8-9 shows the control relationships.

Table 8-9. PHI Control Logic Truth Table

Input Control Signals					Chip Select Status		
LIC1	LIC2	LHP-IB	LDOUT	HDOUTD	BUF U14	LTCH U11	PHI U20
X	0	0	X	0	Yes	No	No
X	0	0	0	X	No	Yes	No
0	X	0	X	X	No	No	Yes

X=Don't Care

8-75. PROCESSOR TO HP-IB INTERFACE (PHI) U20. The PHI chip provides a high speed (up to 1 Mbyte/sec) interface to the HP Interface Bus (HP-IB) for processors and other state-oriented devices. It is compatible with nearly any 8 or 16-bit CPU and requires a minimum of external logic. Together with the four bipolar tri-state transceivers (U5-U8 on the Rear-panel), the PHI chip provides the complete logical and electrical interface between the CPU and the HP-IB. In addition, it provides buffering for inbound and outbound data transfer through two First-In-First-Out (FIFO) registers which can be addressed by the host CPU.

8-76. The following I/O signals are provided by the PHI chip for CPU interfacing:

1. An 8-bit wide bi-directional data bus (D8-D15).
2. D0 and D1 are status bits that indicate which byte of the record is being transferred.
3. A 3-bit address (A13-A15) for selecting one of eight internal registers
4. A read/write control (R/W) that controls the direction of data flow.
5. An interrupt line (INT) to alert the CPU of selected events.
6. Three handshake lines RFD, DAC and DAV to cooridinate data transfer with the HP-IB.
7. A Direct Memory Request line (DMARQ) for directly accessing the CPU memory (not used).

8-77. HP-IB LINES AND OPERATIONS. The HP Interface Bus transfers data and commands between the components of the 64000 Logic Development System on 16 signal lines. The interface functions for each system component are performed within the component so only passive cabling is needed to connect the system. The cables connect all instruments, controllers, and other components of the system in parallel.

8-78. The eight Data I/O lines (DIO1 thru DIO8) are reserved for the transfer of data and other messages in a byte-serial, bit-parallel manner. Data and message transfer is asynchronous and is coordinated by the three handshake lines: Data Valid (DAV), Not Ready for Data (NRFD), and Not Data Accepted (NDAC). The other five lines are for management of bus activity (see figure 8-4).

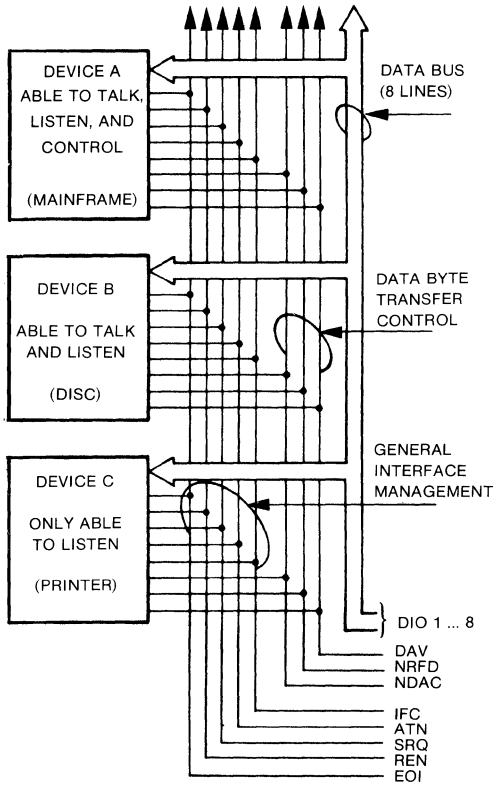


Figure 8-4. HP-IB Signal Lines

8-79. Devices connected to the bus may be talkers, listeners, or controllers. The controlling Mainframe dictates the role of each of the other devices (disc or printer) by setting the ATN (Attention) line true and sending talk or listen addresses on the data lines.

8-80. Addresses are set into each device by switches built into the device. While the ATN line is true, all devices must listen to the data lines. When the ATN line is false, only devices that have been addressed will actively send or receive data; all others ignore the data lines.

8-81. Several listeners can be active simultaneously but only one talker can be active at a time. Whenever a talker address is put on the data lines (while ATN is true), all other talkers are automatically inhibited from talking.

8-82. Information is transmitted on the data lines under sequential control of the three handshake lines (DAV, NRFD and NDAC). No step in the sequence can be initiated until the previous step is completed. Information transfer can proceed as fast as devices can respond, but no faster than allowed by the slowest device presently addressed as active. This permits several devices to receive the same message byte concurrently (for timing, see figure 8-5).

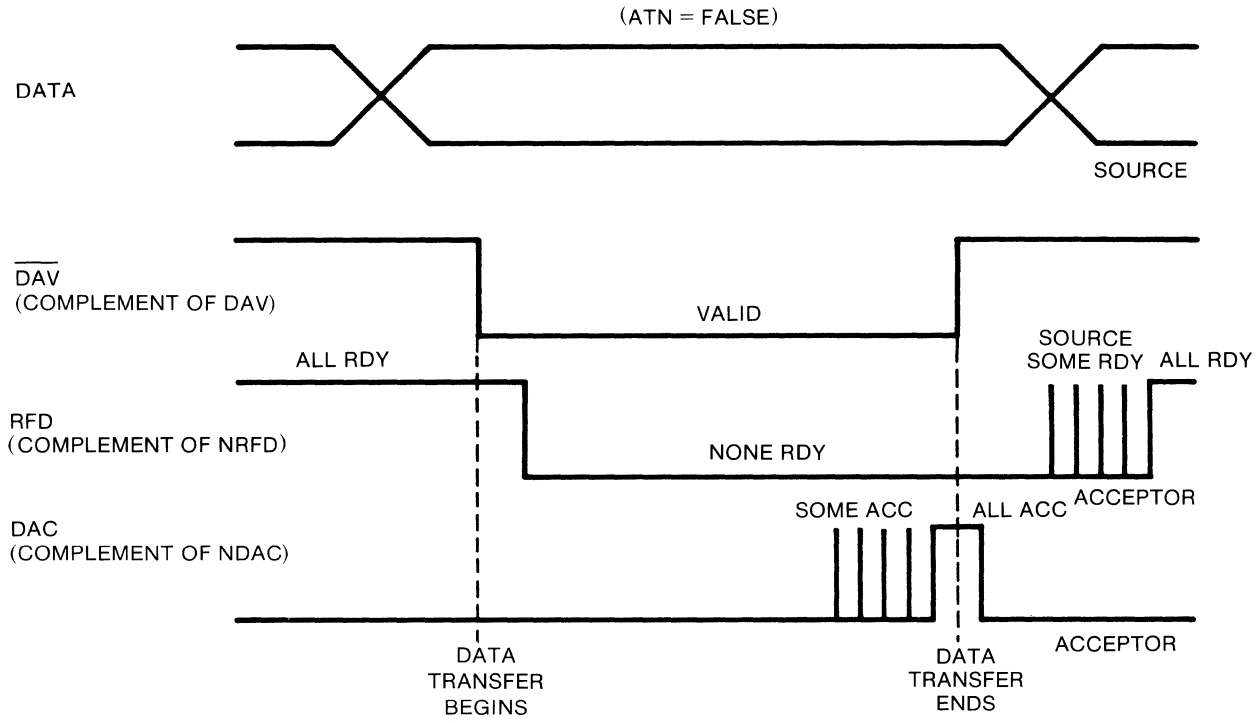


Figure 8-5. HP-IB Handshake Timing

8-83. The ATN line is one of the five bus management lines. When ATN is true, addresses and universal commands are transmitted on only seven of the data lines using the ASCII code. When ATN is false, any code of 8 bits or less understood by both the talker and listener(s) may be used. The IFC (Interface Clear) line places the interface system in a quiescent state via the abort message. The REN (Remote Enable) line is used with the Remote, Local and Clear Lockout/Set Local messages to select either local or remote control of each device. Any active device can set the SRQ (Service Request) line true. This indicates to the CPU that the device on the bus wants attention. The EOI (End or Identify) line is used by a device to indicate the end of a multiple-byte transfer sequence. When the controlling mainframe sets both the ATN and EOI lines true, each device capable of a parallel poll indicates its current status on the DIO line assigned to it.

8-84. RS-232 CONTROL.

8-85. RS-232 INTERFACE (see figure 8-14, sheet 4). The Electronic Industries Associations (EIA) standard RS-232C defines the electrical characteristics for an interface between Data Communication Equipment (DCE) and Data Terminal Equipment (DTE). A DCE is a modulator/ demodulator (modem) for encoding digital data for transmission on the telephone system. A DTE is a terminal for the time-share user. Normally, a male connector is used on the computer or terminal end; and a female connector is used on the modem end. The 64100A Mainframe has two identical female connectors labled: "TO MODEM" (J2) and "TO TERMINAL" (J4) that have the transmit and receive lines reversed so it can act like either as a modem or as a terminal (see figure 8-6).

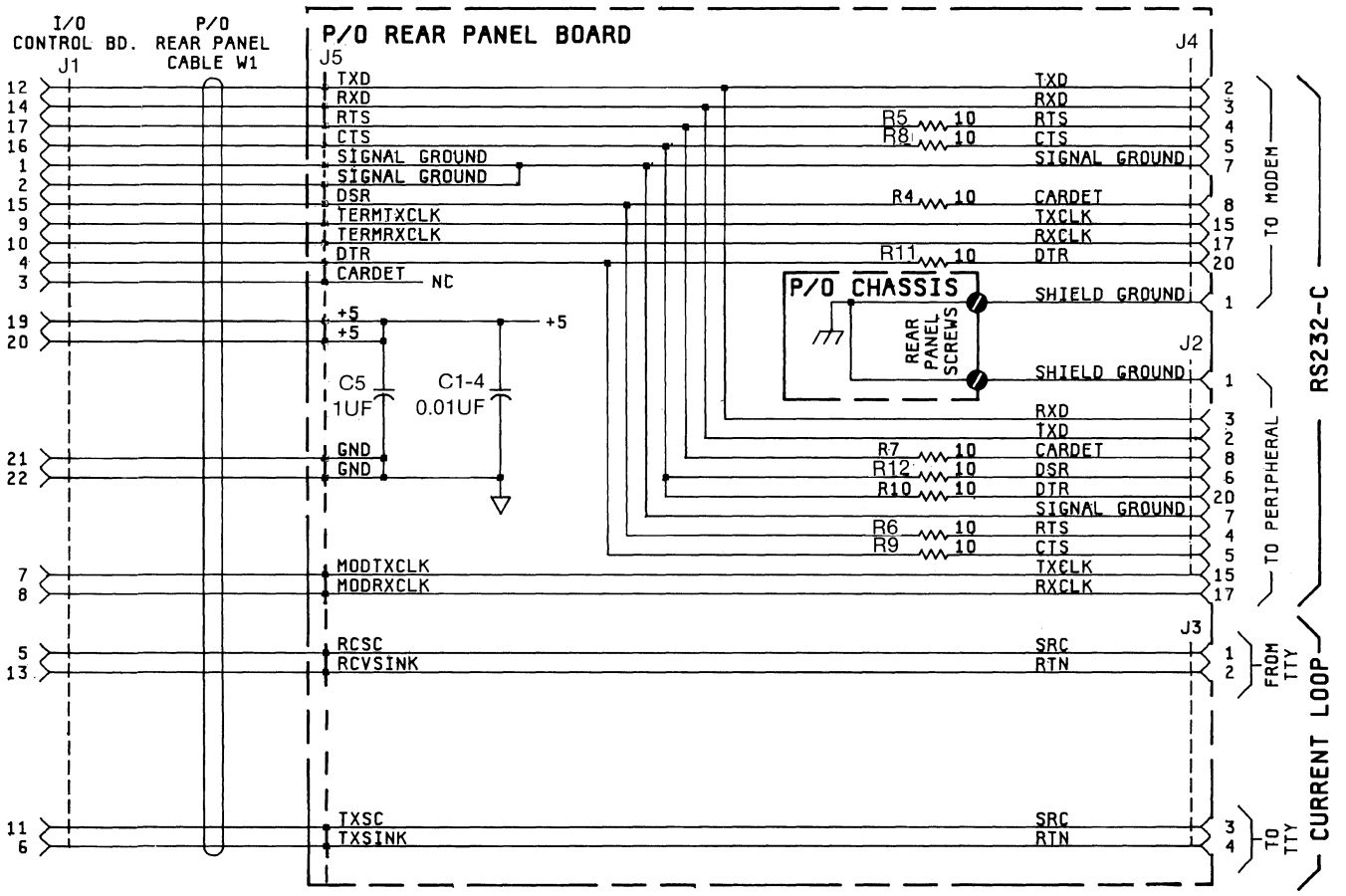


Figure 8-6. RS-232C and Current Loop Schematic

8-86. There are several wires (up to 25) used to provide the RS-232 interface but only 11 are used with the 64000 System. Two of these are the data-carrying wires: one each for transmitted and received data. In addition, there is a signal ground wire and many more that serve as control wires between the DTE and the DCE (see table 8-10).

Table 8-10. RS-232C Interface Connector Pin Functions

CONN. PIN	DESCRIPTION	MNEMONIC	DATA TO	DATA FROM	CONTROL TO	CONTROL FROM	TIMING TO	TIMING FROM
1	Shield Gnd							
2	Transmitted Data	TXD	X					
3	Received Data	RXD		X				
4	Request to Send	RTS			X			
5	Clear to Send	CTS				X		
6	Data Set Ready	DSR				X		
7	Signal Ground	---						
8	Rec'd Line Sig. Det.	CARDET				X		
9	Data Set Testing	N/U						
11	Unassigned	---						
12	Sec.Rec'd Line Sig.Det.	N/U				X		
13	Sec. Clear to Send	N/U				X		
14	Sec. Transmitted Data	N/U		X				
15	Xmtr Sig.Ele.Timing (CPU)	TXCLK						X
16	Sec. Received Data	N/U	X					
17	Revr Sig.Ele.Timing(CPU)	RXCLK						X
18	Unassigned	---						
19	Sec. Request to Send	N/U			X			
20	Data Terminal Ready	DTR			X			
21	Signal Quality Detector	N/U				X		
22	Ring Indicator	N/U				X		
23	Data Sig.Rate Selector(CPU)	N/U				X		
24	Xmtr Sig.Ele.Timing(DTE)	N/U					X	
25	Unassigned	---						

Legend: To = To CPU (Mainframe)
From = From CPU (Mainframe)
DTE = Data Terminal Device
N/U = Not Used

8-87. Since the RS-232 interface involves bi-directional data flow (both half-duplex and full-duplex), it is important to know which device is acting as the DCE and which is acting like the DTE. In RS-232, all of the signal names are from the DTE's point of view: i.e., the DTE transmits on the Transmitted Data line (TXD, pin 2) and receives on the Received Data line (RXD, pin 3). The DCE, on the other hand, is just the opposite. Since a RS-232 peripheral device may be configured like either a modem or a terminal, the 64000 Mainframe Rear-panel has two connectors (J2 and J4) and a mode switch. This permits configuring the Mainframe as either a modem or terminal and makes it compatible with the peripheral. That is, if the peripheral equipment is a "terminal", use the J4 port ("To Terminal"); if the peripheral is a "modem", use the J2 port ("To Modem").

8-88. Figures 8-7 through 8-10 illustrate the four functional situations that can exist:

1. Mainframe as "terminal talker" (figure 8-7)
2. Mainframe as "terminal listener" (figure 8-8)
3. Mainframe as "modem talker" (figure 8-9)
4. Mainframe as "modem listener" (figure 8-10)

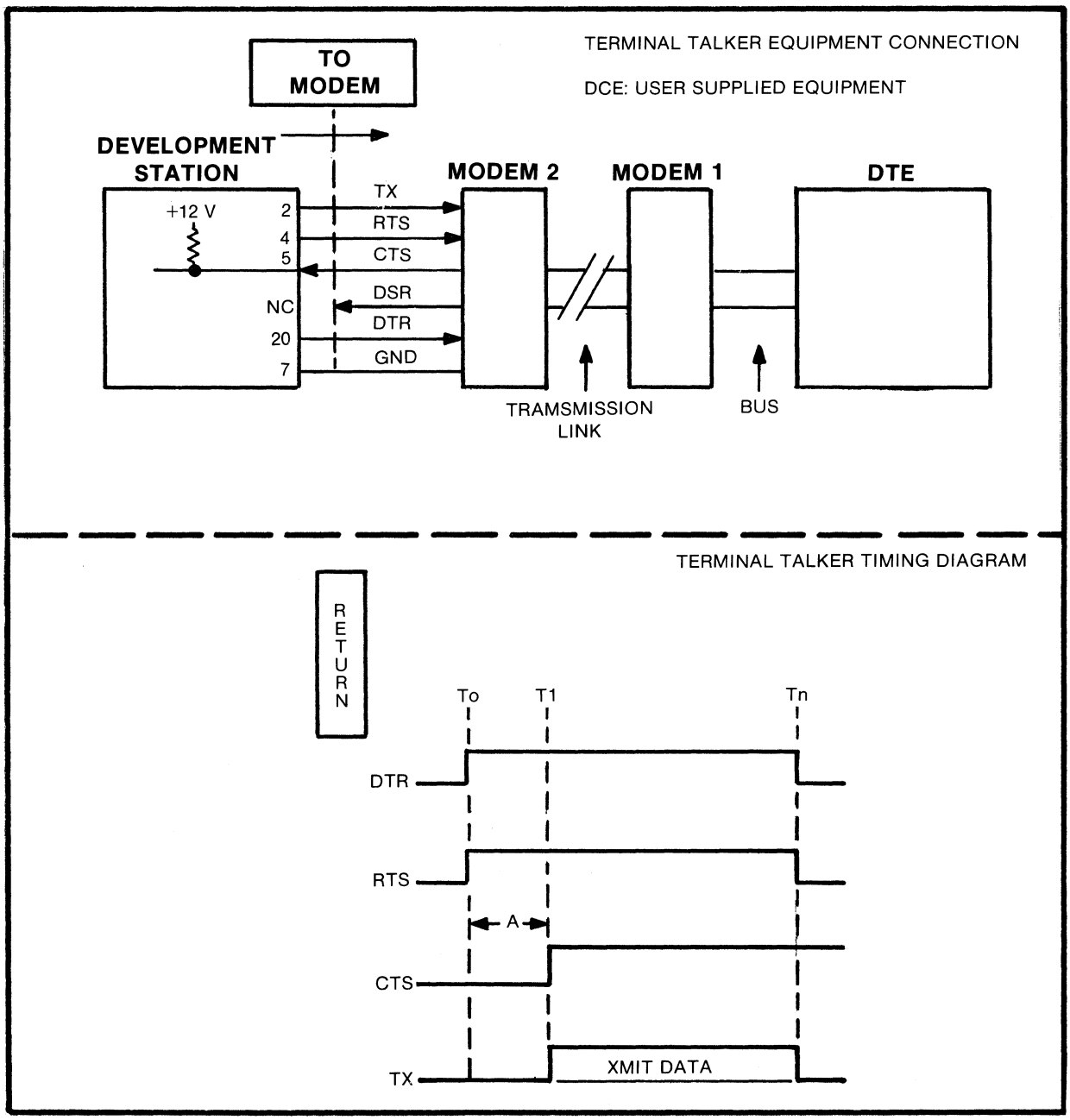


Figure 8-7. Terminal as Talker

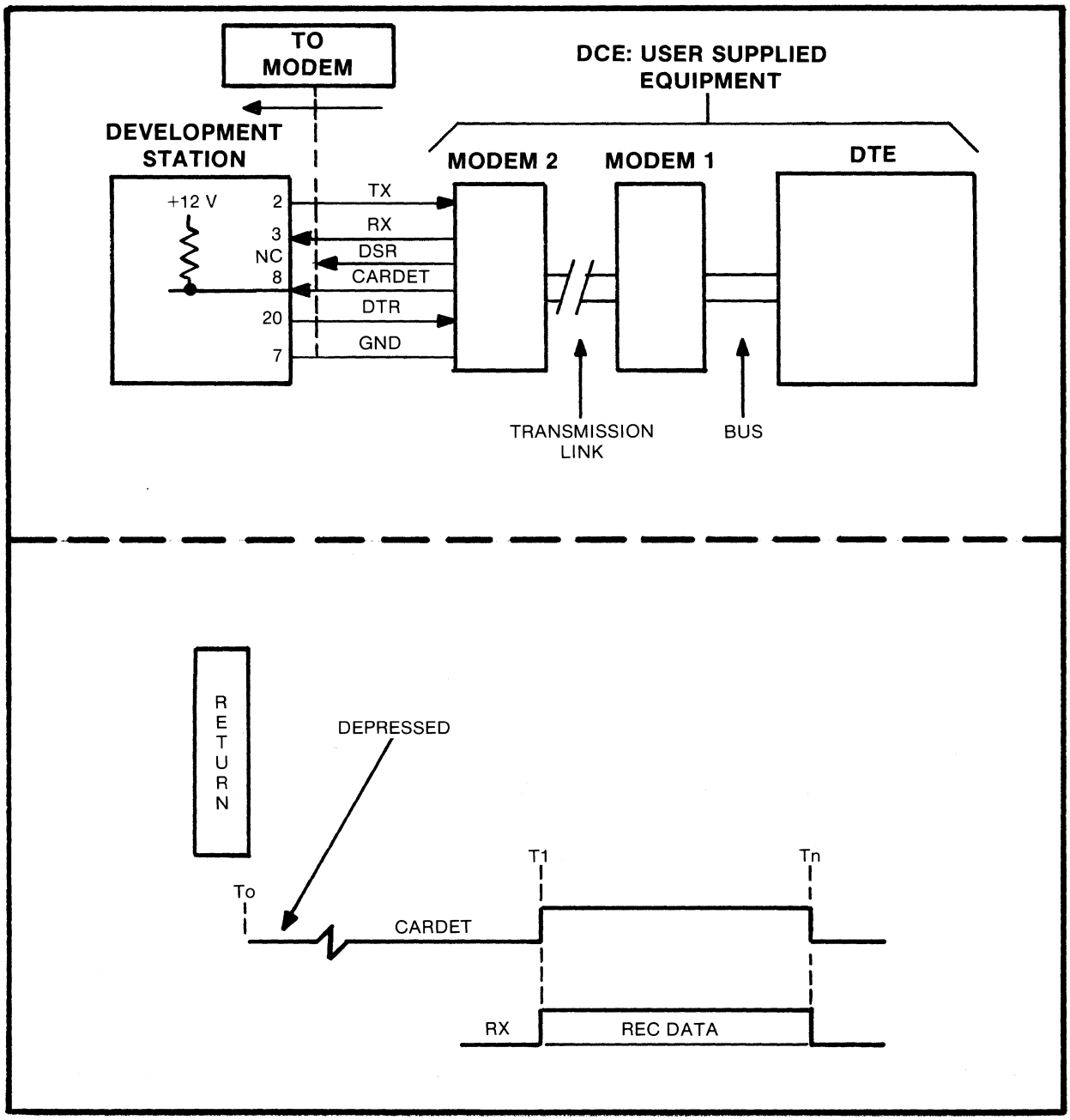


Figure 8-8. Terminal as Listener

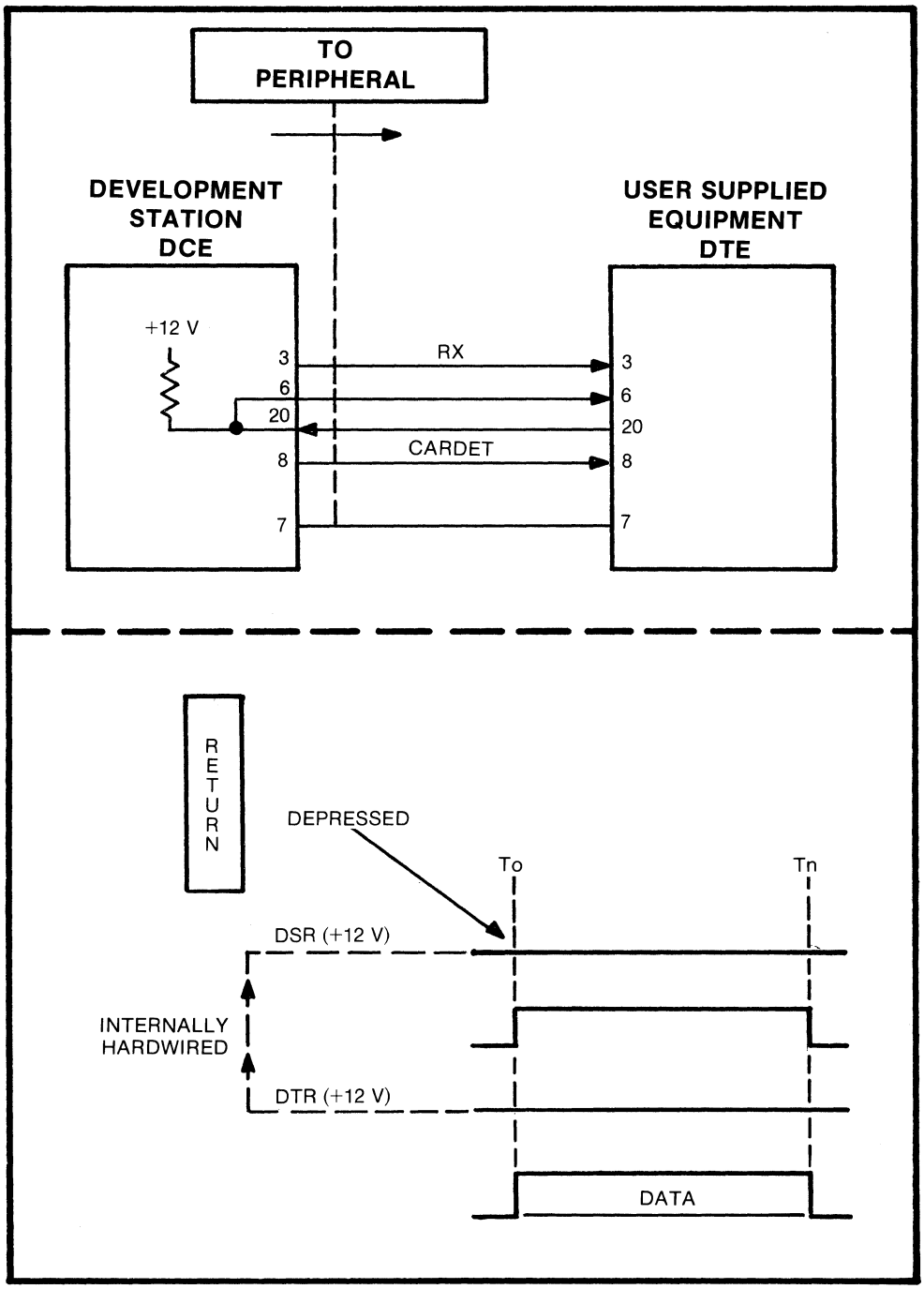


Figure 8-9. Modem as Talker

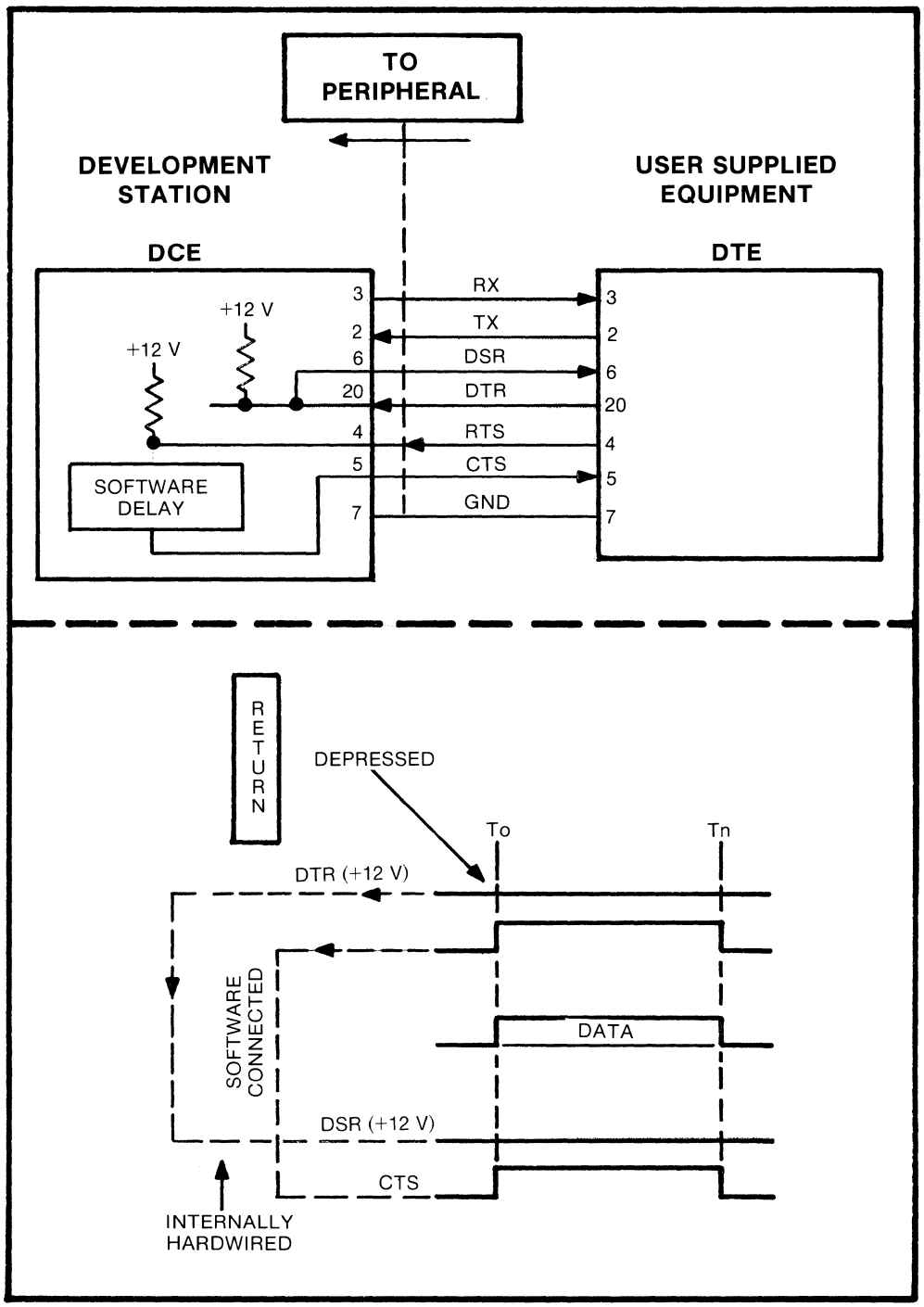


Figure 8-10. Modem as Listener

8-89. Figure 8-11 illustrates the RS-232C bit-serial data format. The bit-serial transmission mode produces a waveform that is unique for each character. Figure 8-11 shows the letter "E" in ASCII (binary 01000101). Since RS-232C transmits the LSB first, you must read the 01000101 from left to right. Leading off is a start bit (at the left), then comes the character (LSB to MSB), then a parity bit (odd parity is shown), and finally the stop bit(s). Note the use of negative-true logic in which the negative level represents a logic one; the positive level a logic zero. Figure 8-12 shows the typical timing sequence when a terminal is talking to a modem.

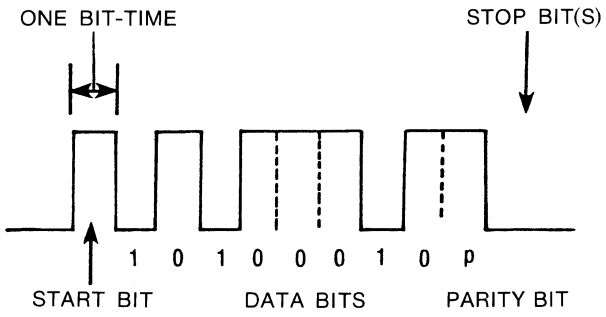


Figure 8-11. RS-232 Data Format

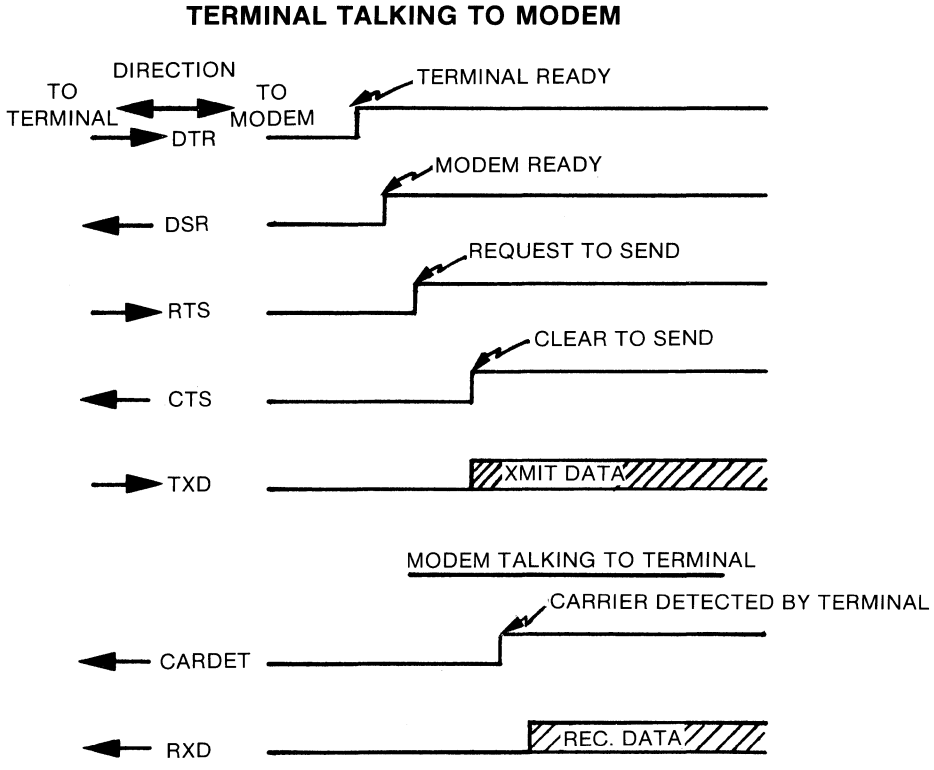


Figure 8-12. Typical Sequence of Events for RS-232C Data Transfer

8-90. RS-232 INTERFACE VOLTAGES. Except for protective and signal grounds, all RS-232C circuits carry bi-polar, low-voltage signals. Also, these circuits are "failsafe"; that is, if power is lost at the transmitter, the receiver interprets the signal condition as OFF. Table 8-11 defines the voltage ranges vs. binary value for the RS-232C signals.

Table 8-11. RS-232C Voltage Levels

TYPE OF CIRCUIT		NEGATIVE VOLTS (-3 TO -25 VDC)	POSITIVE VOLTS (+3 TO +25 VDC)
Data	Binary	1	0
	Signal	Mark	Space
Control		OFF	ON

8-91. RS-232 MODE CONTROL SWITCHES. The RS-232 mode of operation is controlled by five switches located on the I/O board. The function of these switches are described in table 3-1 and on figure 8-1.

8-92. SIGNAL MNEMONICS - Signals Mnemonics are listed on table 8-12.

Table 8-12. I/O Signal Mnemonics

NOTE: This table is divided into the following groups:
Overall Mnemonics; Internal I/O Address Signals; Interrupt Signals; Low Priority Interrupts; I/O Data Bus; PHI I/O Signals; USART I/O Signals; Rear-Panel I/O Signals; Keyboard I/O Signals.

MNEMONIC	COMMON NAME	ACTIVE STATE	CHARACTERISTIC AND FUNCTION
		OVERALL MNEMONICS	
HBON	Beeper On	High	When high, activates the beeper.
HDE	Display Enable	High	When high, enables the CRT display.
HPOP	Pwr. O Pulse	High	Same as LPOP.
LA14 & LA15	Peripheral Address Bits	Low	Generated by CPU to address various devices in the system; in the I/O these address bits enable Slot Select Decoder U53.
LBRTN	Beeper Return	Low	Return line for HBON signal.

Table 8-12. I/O Signal Mnemonics (Cont'd)

MNEMONIC	COMMON NAME	ACTIVE STATE	CHARACTERISTIC AND FUNCTION
LDOUT	Data Out	Low	Generated by the CPU; when active low, indicates to the addressed peripheral device that the CPU is ready to write to it (LIOSB must also be active). When high, indicates to addressed peripherial device that the CPU is ready to receive data; used by I/O to select peripherial address decoder and to control the I/O data transceivers.
LDOUTD	Data Out Delayed	Low	When low, indicates to the addressed peripheral device that the CPU is ready to receive data; used by I/O to select peripheral address decoders, to control the I/O data transceivers, and select the keyboard data.
LHLT or HHLT	Halt	Low	Initiates direct memory access from CPU to PHI chip.
LIBE	Interrupt Buffer	Low	Enables Interrupt Buffer U21.
LIC1 & LIC2	Interface Commands	Low	Used in conjunction with each other to: (1) control the beeper, (2) generate the S/A start-stop interval, (3) select the PHI chip, and (4) select command or data mode for the USART chip.
IDEN	Ident. Enable	Low	When low, enables all PC boards in slots 0 thru 9 (option slots) to generate card-type ID codes after interrogated by the slot select (SS) command.
LINE SYNC	Line Sync		Generated by the Pwr. Supp.; the sync pulses are counted by Delta-T Counter U37 which reaches its terminal count in about 2 seconds. Then the time reset signal LPOP is generated if the CPU doesn't reset the counter before the terminal count is reached.

Table 8-12. I/O Signal Mnemonics (Cont'd)

MNEMONIC	COMMON NAME	ACTIVE STATE	CHARACTERISTIC AND FUNCTION
LIOSB	Input/Output Strobe	Low	Indicates data on I/O bus is valid.
LMAP1-LMAP3	Address Map	Low	Extends address selection capability to 48K locations on each option card.
LPA0-LPA3	Peripheral Addresses	Low	Select one of nine peripheral address commands used for enabling or activating various I/O circuits.
LPOP	Pwr. On Pulse	Low	Initializes CPU, resets Interrupt Enable Latch U44, resets S/A Interval FF U32A, enables Pwr On Pulse One Shot U52, and generates high priority interrupt LIRH via FF U29.
LSS0-LSS10	Slot Select	Low	Goes to each of 9 card slots and causes each card to generate it's unique code (LIDEN must also be present).
	INTERNAL I/O ADDRESS SIGNALS		
LHP-IB	HP-IB Address	Low	Used in conjunction with LIC1, LIC2, LDOUT, and LDOUTD to enable buffer U12 (reads Rear-panel sw. status), Latch U11 (register select address for PHI), and PHI chip select (U20).
LIMASK	Interrupt Mask Address	Low	When low, enables Interrupt Mask Latch (U14).
LKYBD	Keyboard Address	Low	Used in conjunction with LDOUTD to enable and select Keyboard data.
LPFS	Power Fail	Low	When low, sets Power Fail Latch (U32B).

Table 8-12. I/O Signal Mnemonics (Cont'd)

MNEMONIC	COMMON NAME	ACTIVE STATE	CHARACTERISTIC AND FUNCTION
LRSRD	RS-232 Read Address	Low	When low, serves as Read command to RS-232 Transceiver (USART, U28). It acts the same as WR under USART Signal.
LRSWR	RS-232 Write Address	Low	When low, serves as write command to RS-232 transceiver (USART, U28). Same as WR under USART Signals.
LSSEL	Slot Select Address	Low	When low, enables Slot Select Address Latch (P/O U44) and Card ID Latch (P/O U44).
L(Delta)T	Time Interval Address	Low	When low resets Delta Time Interrupt Latch U29B as response to the CPU answering HIR(Delta)T Interrupt.
	INTERRUPT SIGNALS		
LIBE	Interrupt Enable Buffer	Low	Enables the Interrupt Buffer U21.
LINT	Interrupt	Low	The CPU pulls this line low in response to LIRH or LIRL to allow polling the I/O bus to determine which peripheral device requested the interrupt.
LIR15	Interrupt 15	Low	Generated by Power Supply to indicate that a power failure is eminent and causes high level interrupt LIRH.
LIRH	High Priority Interrupt	Low	When low, indicates that a high priority interrupt (power fail) has been requested.
LIRL	Low Priority Interrupt	Low	When low, indicates that a low priorty interrupt has been requested by one of the seven circuits with interrupt service (see Low Priority Interrupt signals below).
	LOW PRIORITY INTERRUPTS		
HIRIB	HP-IB Interrupt	High	Goes high when PHI chip has an interrupt condition (see INT under PHI signals in this table).

Table 8-12. I/O Signal Mnemonics (Cont'd)

MNEMONIC	COMMON NAME	ACTIVE STATE	CHARACTERISTIC AND FUNCTION
HIRKB	Keyboard Interrupt	High	Goes high when a Keyboard Key has had a change of state.
HIRRX	RS-232 Receive Interrupt	High	Goes high when RS-232 USART is ready to receive (see RXRDY under USART Signals).
HIR(Delta)T	Time Interval Interrupt	High	Goes high on first neg. to pos. transition of LINE SYNC sent to Low Priority Interrupt Logic Gate U24B.
HIRTX	RS-232 Transmit Interrupt	High	Goes high when RS-232 USART is ready to transmit (see TXRDY under USART signals).
LIR1	Emulator Interrupt	Low	Goes low when Emulators are in need of service.
LIR3	TACO Interrupt	Low	Goes low when TACO is in need of service.
LIR4		Low	(Not Assigned)
	I/O DATA BUS		
HIOD0-HIOD15	I/O Data	High	(Same LIOD0-15)
LIOD0-LIOD15	I/O Data	Low	16-bit bidirectional I/O bus used for transferring data between the CPU and the I/O circuits. Information is active Low.
	PHI I/O SIGNALS		
A13-A15	Address bits 13-15	High	Specifies the internal register being written to or read from.
ATN	Attention	Low	Ties to HP-IB ATN line via transceiver; defines type of data on data bus (addresses/commands or data).
CHSEL	Chip Select	Low	When low, allows PHI chip to respond to read or write cycles initiated by IOGO Line.

Table 8-12. I/O Signal Mnemonics (Cont'd)

MNEMONIC	COMMON NAME	ACTIVE STATE	CHARACTERISTIC AND FUNCTION
CIC	Controller in Charge	High	Asserted when host PHI is current controller in charge of HP-IB. Used as an enable for the ATN and SRQ line drivers (one of which is on at all times).
D0 & D1	CPU Data bits 0-1	High	Allows CPU to select internal PHI registers.
D8-D15	CPU Data bits 8-15	High	Carry bi-directional data during to or writes from PHI chip by CPU.
DAC	Data Accepted	High	Indicates acceptance of data by all devices.
DAV	Data Valid	Low	Ties to HPIB DAV line via transceiver chip, indicates availabilty and validity of data on data bus.
DIO1-DIO8	Data I/O Bits	High	Connected to HP-IB I/O lines via transceiver chips.
DIOE	DIO Enable	High	When asserted enables the Data I/O transceivers.
DMARQ	Direct Memory Request	Low	Used to request direct memory access cycles to transfer data to the out-bound FIFO or from the inbound FIFO (see LHLT).
EOI	End of Identify	Low	Bi-directional line that ties to HP-IB EOI line via transceiver chip. Indicates end of data transfer or identifies initiation of polling operation.
HSE	High State Enable	High	Asserted whenever DIO, DAV or EOI are required to have active pullup. Tied to high state enable inputs of transceivers.
IFC	Interface Clear	Low	Ties to HP-IB IFC line via trans-ceiver chip. Places I/O system into know quiescent (idle) state.

Table 8-12. I/O Signal Mnemonics (Cont'd)

MNEMONIC	COMMON NAME	ACTIVE STATE	CHARACTERISTIC AND FUNCTION
INT	Interrupt	Low	Alerts CPU that one of the following events has occured: Intrpt. pending, parity error, status change, handshake abort, poll response, service request, FIFO available, or device clear.
IOEND	I/O End	Low	Not applicable for PHI used in synchonous mode.
IOGO	I/O Go	Low	When low, causes a read from or write to a specific register in PHI.
PON	Power ON	High	When high, causes internal circuits to be initiated.
REN	Remote Enable	Low	Ties to HP-IB REN Line via transceiver Enables alternate devices to provide programming data.
RFD	Ready for Data	High	Indicates that devices are ready to accept data. Ties to HP-IB NRFD line via transceiver chip.
RS	Delay Resistor		Resistor load that controls internal propagation delay.
R/W	Read/Write Command		When high specifies that the PHI perform a write function; when low specifies a Write function.
SCTRL	System Control	High	When high, provides PHI with system control capabilities.
SRQ	Service Request	Low	Ties to HP-IB SRQ Line via transceiver Indicates a need for service; causes interrupt of current sequence in CPU.

Table 8-12. I/O Signal Mnemonics (Cont'd)

MNEMONIC	COMMON NAME	ACTIVE STATE	CHARACTERISTIC AND FUNCTION
		USART I/O SIGNALS	
C/D	Command/ Data		When Low informs USART that the word on the data bus is a data character; a high indicates a control character (either WR or RD must also be active).
CLK	Clock		Controls internal timing of USART; must be at least 30X TXC or RXC.
CS	Chip Select	Low	A Low enables the USART chip.
CTS	Clear to Send	Low	Enables USART to send serial data to external peripheral (if TXEN is also high).
D0-D7	Data	High	Parallel input/output data or control words to and from CPU.
DSR	Data Set Ready	Low	Used for testing status of modem data status.
DTR	Data Terminal Ready	Low	Controlled by CPU; used for external peripheral control (e.g. data terminal ready or rate select).
RD	Read	Low	A Low informs the USART that the CPU is reading status or data from the USART.
RESET	Reset	High	A high forces USART into idle mode until a new set of control words is received from the CPU.
RTS	Request to Send	Low	Controlled by CPU; used for external peripheral control (e.g. request to send).
RXC	Receiver Clock	Low	Controls rate at which characters are received.
RXD	Receive Data	High	Serial data received from external RS-232 peripheral device.

Table 8-12. I/O Signal Mnemonics (Cont'd)

MNEMONIC	COMMON NAME	ACTIVE STATE	CHARACTERISTIC AND FUNCTION
RXRDY	Receive Ready	High	Tells the CPU that USART contains a character that is ready to be input to CPU. Serves as an Interrupt.
TXC	Transmitter Clock	Low	Controls rate at which characters are are transmitted.
TXD	Transmit Data	High	Serial data sent to external RS-232 peripheral device.
TXRDY	Transmit Ready	High	Tells CPU that USART is ready to accept a data character. Serves as an interrupt. (See HIRTX).
WR	Write	Low	A Low informs the USART that the CPU is outputting data or control words (i.e. writing to the USART).
		REAR PANEL I/O SIGNALS	
MODRXCLK	Modem Receive Clock		Modem receive clock to or from external Modem.
MODTXCLK	Modem Transmit		Modem transmit clock to or from external Modem.
RCSC	Receive Source Current		Source current for receive signal.
RCVSINK	Receiver Current Sink		Serves as return for receive source current.
TERMRXCLK	Terminal Receive Clock		Terminal receive clock to or from peripheral terminal.
TERMTXCLK	Terminal Transmit Clock		Terminal transmit clock to or from peripheral terminal.

Table 8-12. I/O Signal Mnemonics (Cont'd)

MNEMONIC	COMMON NAME	ACTIVE STATE	CHARACTERISTIC AND FUNCTION
TXSC	Transmitter Source Current		Source current for transmit signal.
TXSINK	Transmitter Current Sink		Serves as return for transmit source current.
	KEYBOARD I/O SIGNALS		
HKA0-HKA6	Key Addresses	High	Key address bits HKA0-HKA3 and LKA3 (see below) select one of the 16 vertical columns of keys, Address bits HKA4-HKA6 select one of the 8 horizontal rows of keys.
HKYDN	Key Down	High	When high, indicates that a key is depressed.
HSTB	Strobe	High	(Same as LSTB)
LKA3	Key Address	Low	(see HKA0-6 above)
LKBCLK	Keyboard Clock	Low	Clocks the Current Ramp Generator which enables all 16 columns of keys.
LSTB	Strobe	Low	Clocks Keyboard Scan State Machine circuit.

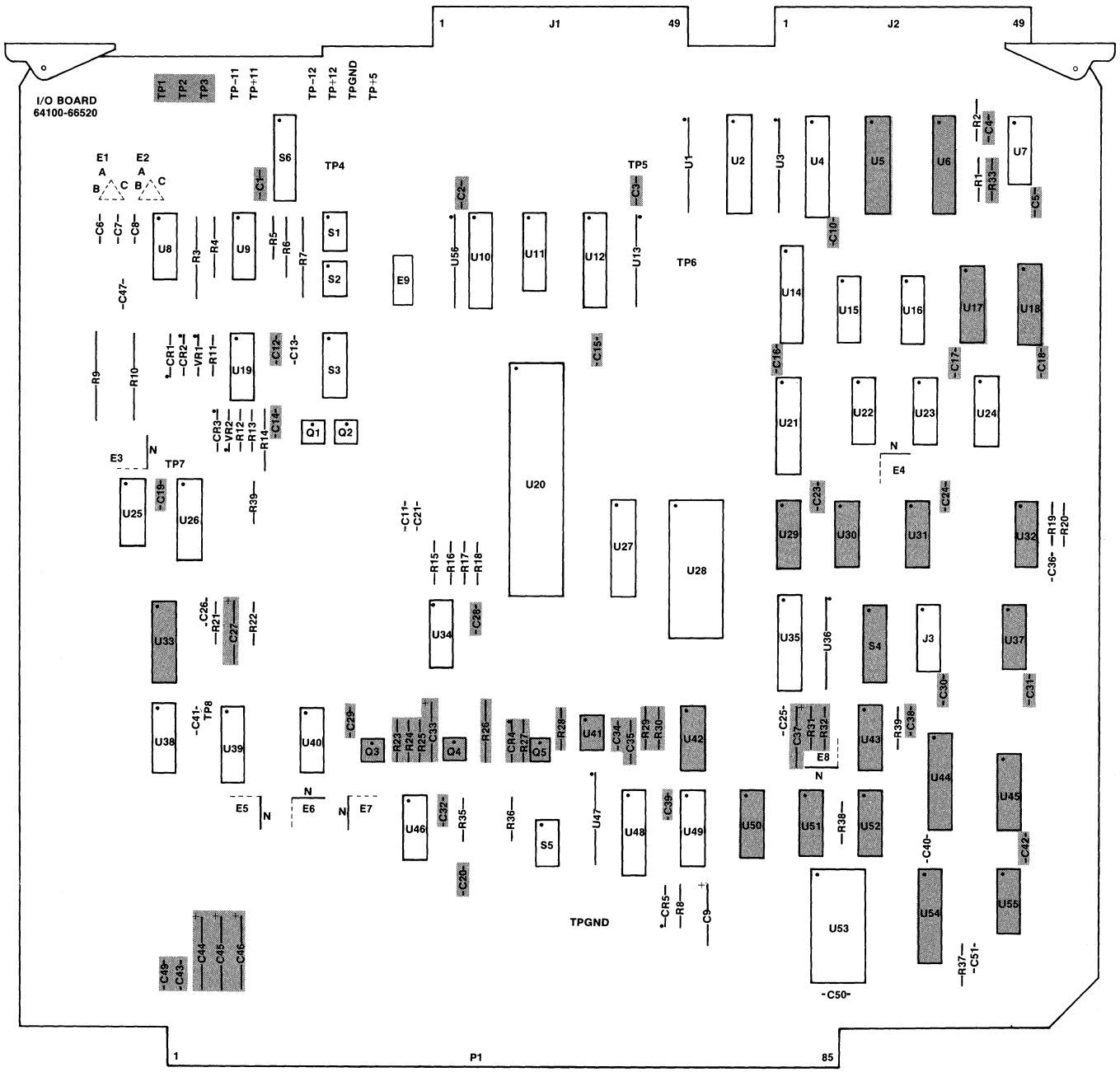
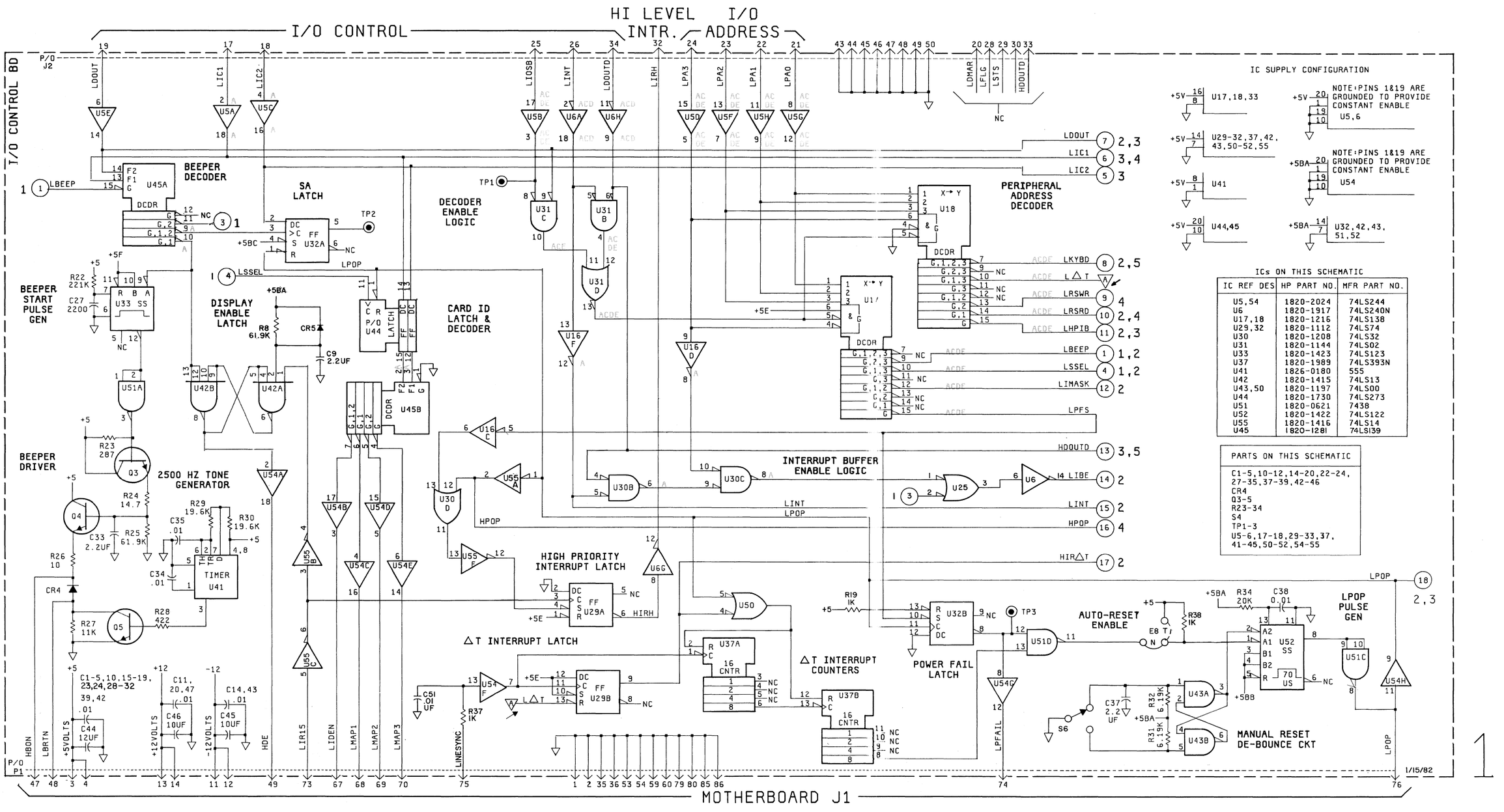


Figure 8-13. I/O Component Locator



IC SUPPLY CONFIGURATION

+5V	U17,18,33
+5V	U29-32,37,42, 43,50-52,55
+5V	U41
+5V	U44,45
+5V	NOTE:PINS 1&19 ARE GROUNDED TO PROVIDE CONSTANT ENABLE U5,6
+5BA	NOTE:PINS 1&19 ARE GROUNDED TO PROVIDE CONSTANT ENABLE U54
+5BA	U32,42,43, 51,52

ICs ON THIS SCHEMATIC

IC REF DES	HP PART NO.	MFR PART NO.
U5,54	1820-2024	74LS244
U6	1820-1917	74LS240N
U17,18	1820-1216	74LS138
U29,32	1820-1112	74LS74
U30	1820-1208	74LS32
U31	1820-1144	74LS02
U33	1820-1423	74LS123
U37	1820-1989	74LS393N
U41	1826-0180	555
U42	1820-1415	74LS13
U43,50	1820-1197	74LS00
U44	1820-1730	74LS273
U51	1820-0621	7438
U52	1820-1422	74LS122
U55	1820-1416	74LS14
U45	1820-1281	74LS139

PARTS ON THIS SCHEMATIC

C1-5,10-12,14-20,22-24, 27-35,37-39,42-46
CR4
Q3-5
R23-34
S4
TP1-3
U5-6,17-18,29-33,37, 41-45,50-52,54-55

Figure 8-14.
I/O Schematic 1 (Sheet 1 of 5)

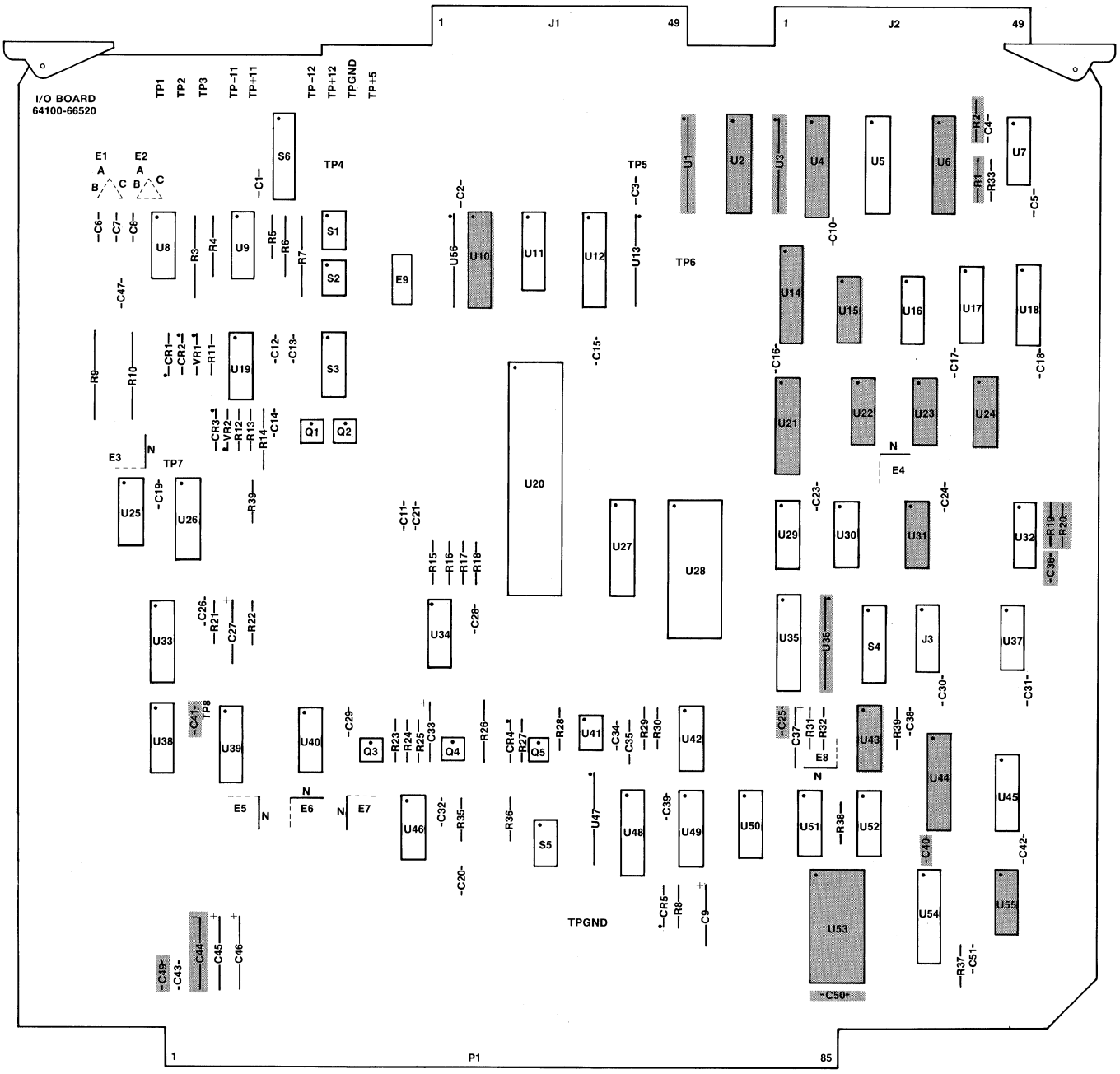
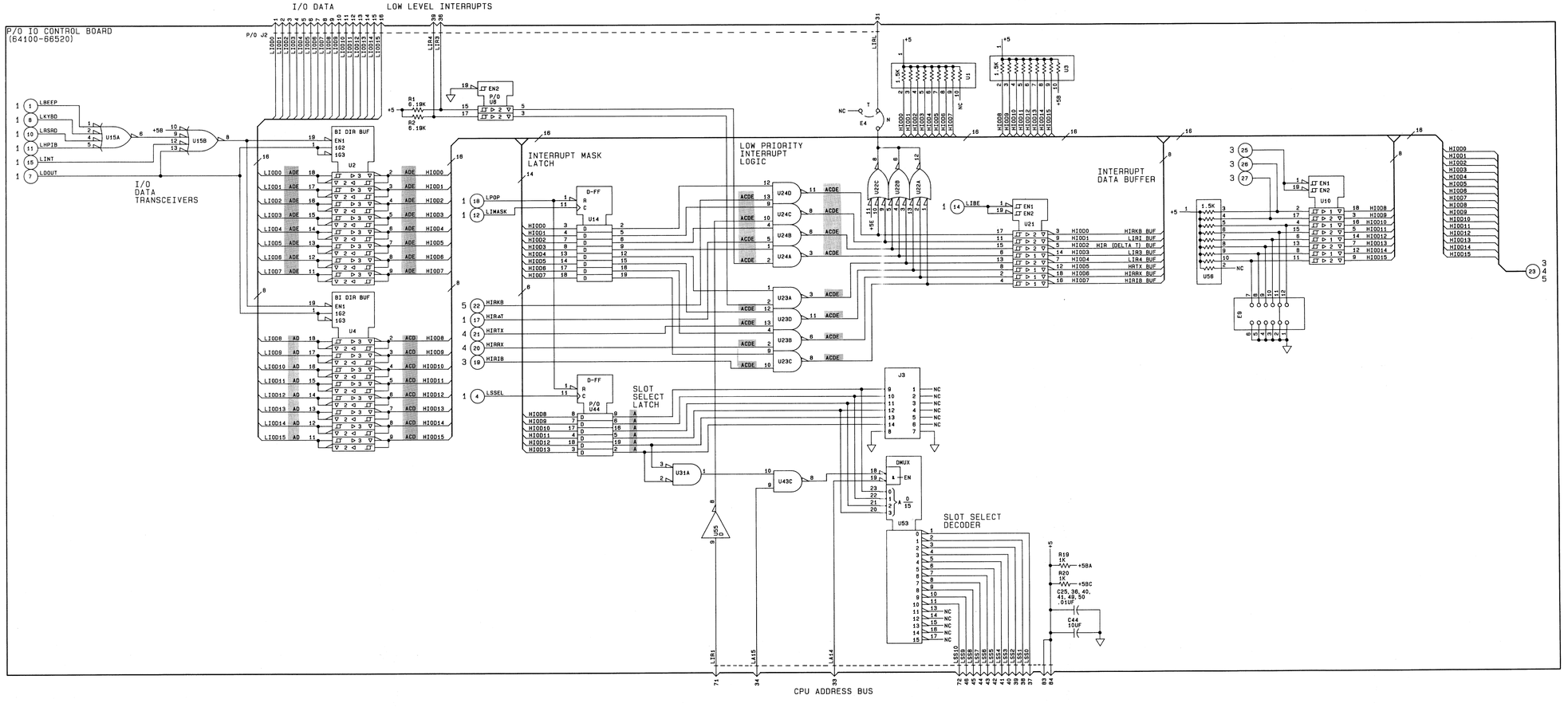


Figure 8-13. I/O Component Locator



2

ICs ON THIS SCHEMATIC

REF DES	HP PART NO.	MFR PART NO.
U1,3,36	1810-0276	210A152
U2.4	1820-2206	74LS640N
U6,21	1820-1917	74LS240N
U10	1820-2024	74LS244N
U14,44	1820-1730	74LS273N
U15	1820-1205	74LS21N
U22	1820-1243	74LS15N
U23,24.43	1820-1197	74LS00N
U31	1820-1144	74LS02N
U53	1820-0495	74LS04N
U55	1820-1416	74LS14N

PARTS ON THIS SCHEMATIC

C25,36,40,41,49,50	.01UF
C44	10UF
R1,2	6.19K
R19,20	1K

IC POWER CONFIGURATION

20	+5V	U6,10,14,44
10	GND	
14	+5V	U15,22,23, U24,31,43, U53,55
7	GND	

Figure 8-14.
I/O Schematic 2 (Sheet 2 of 5)

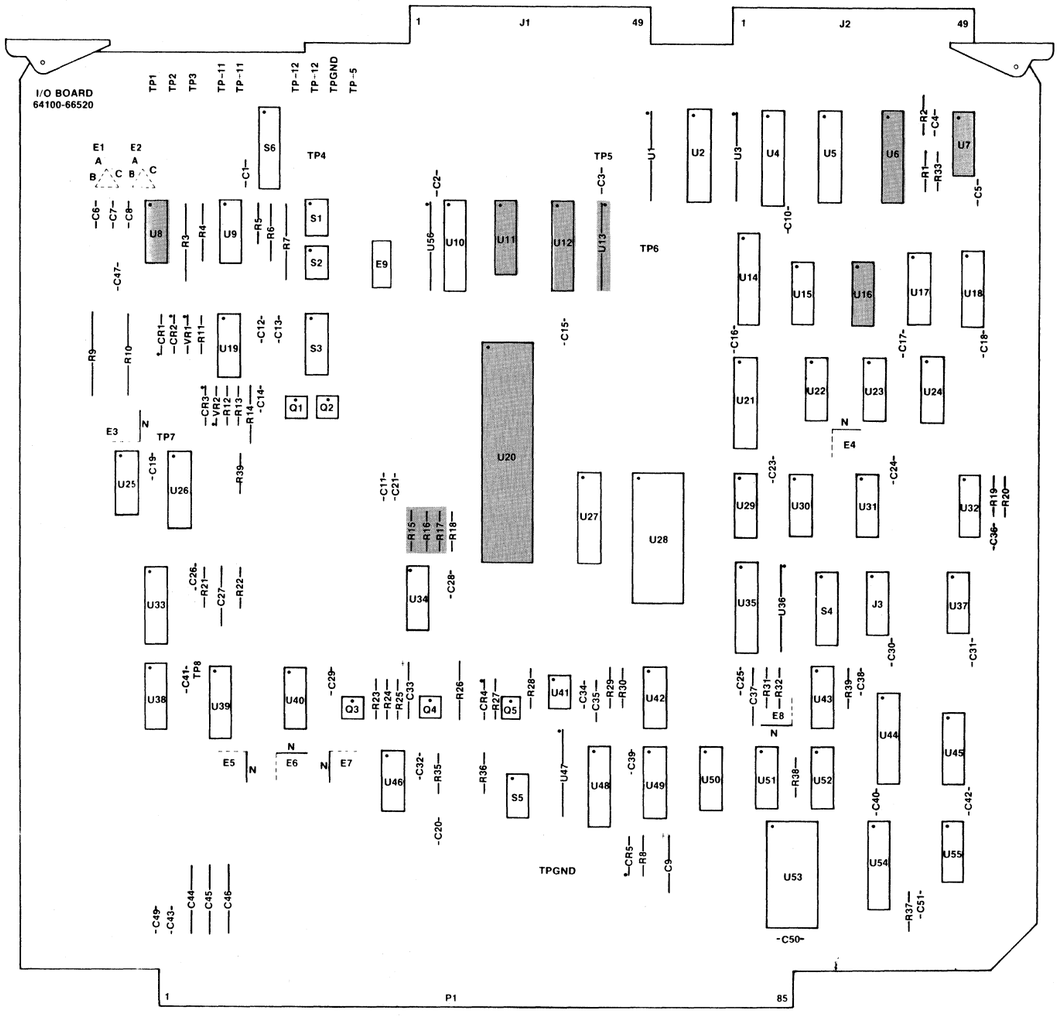


Figure 8-13. I/O Component Locator

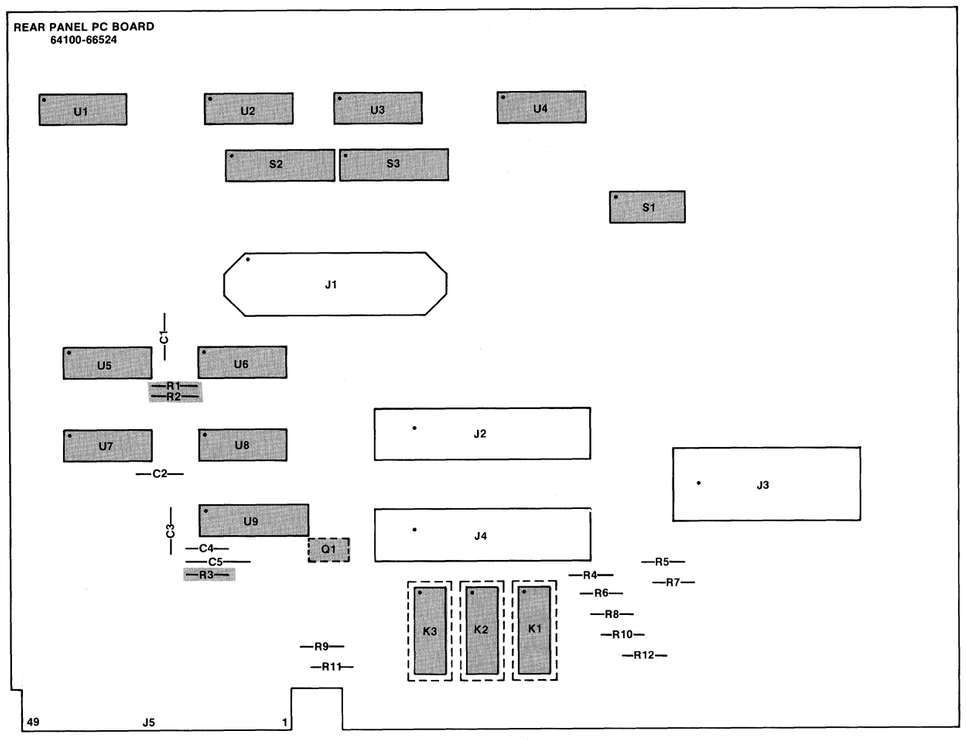


Figure 8-15. Rear-Panel Component Locator

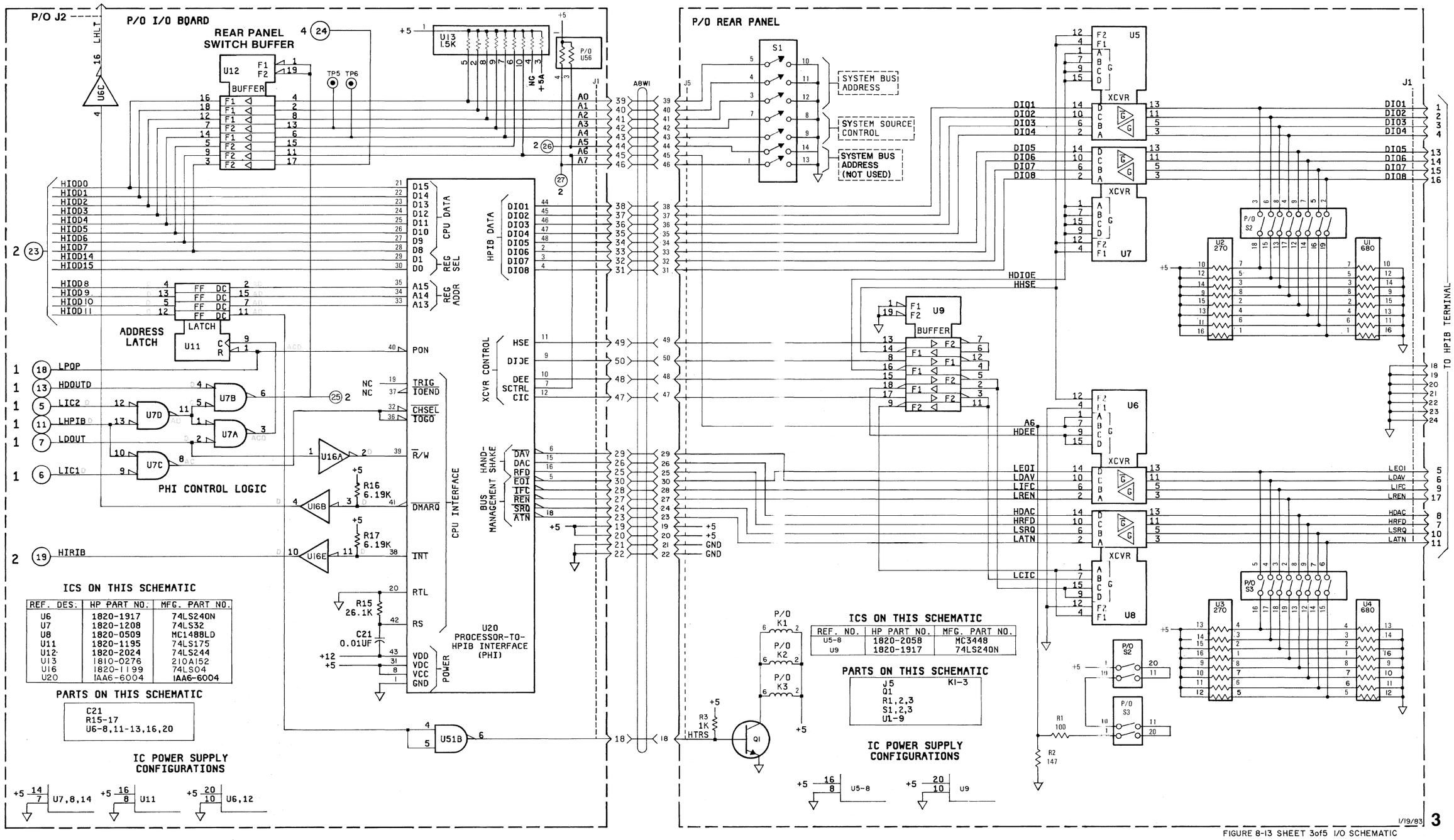


FIGURE 8-13 SHEET 3of5 I/O SCHEMATIC

Figure 8-14
I/O Schematic 3 (Sheet 3 of 5)

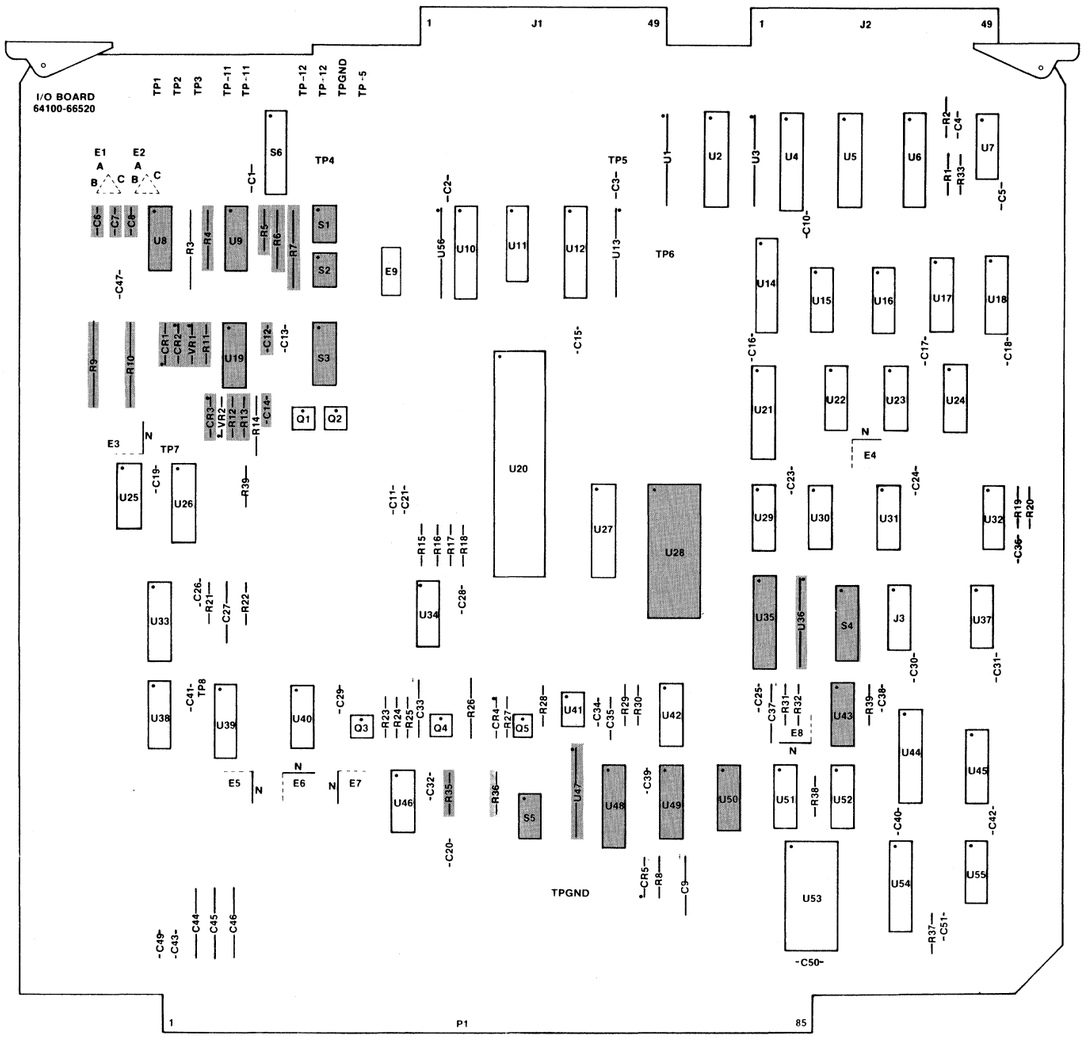


Figure 8-13. I/O Component Locator

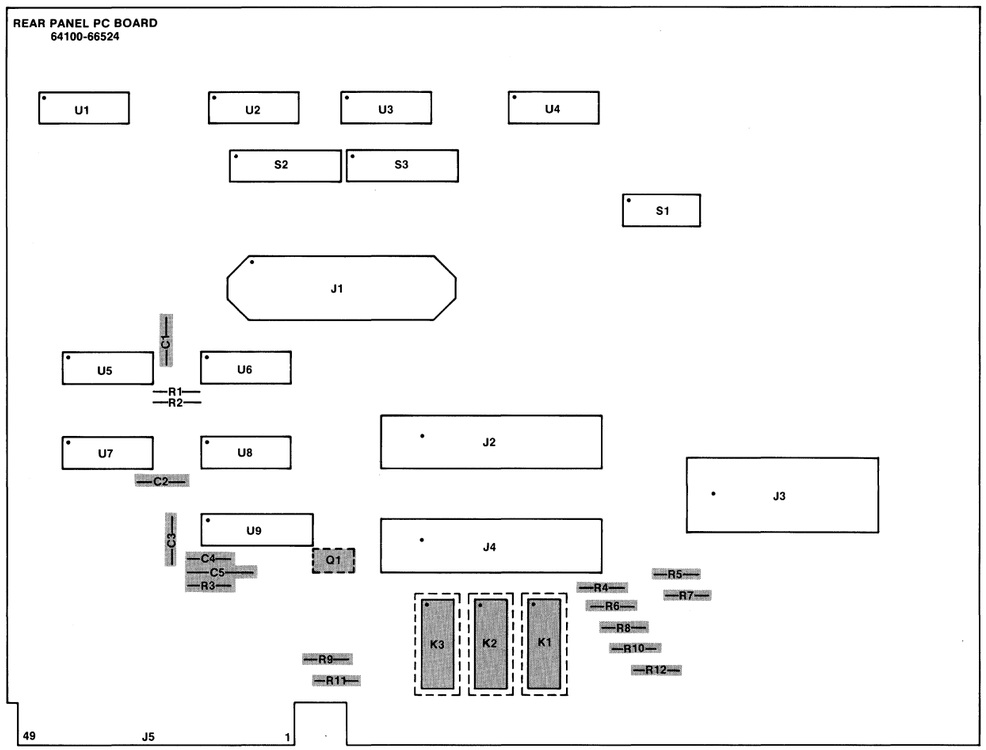
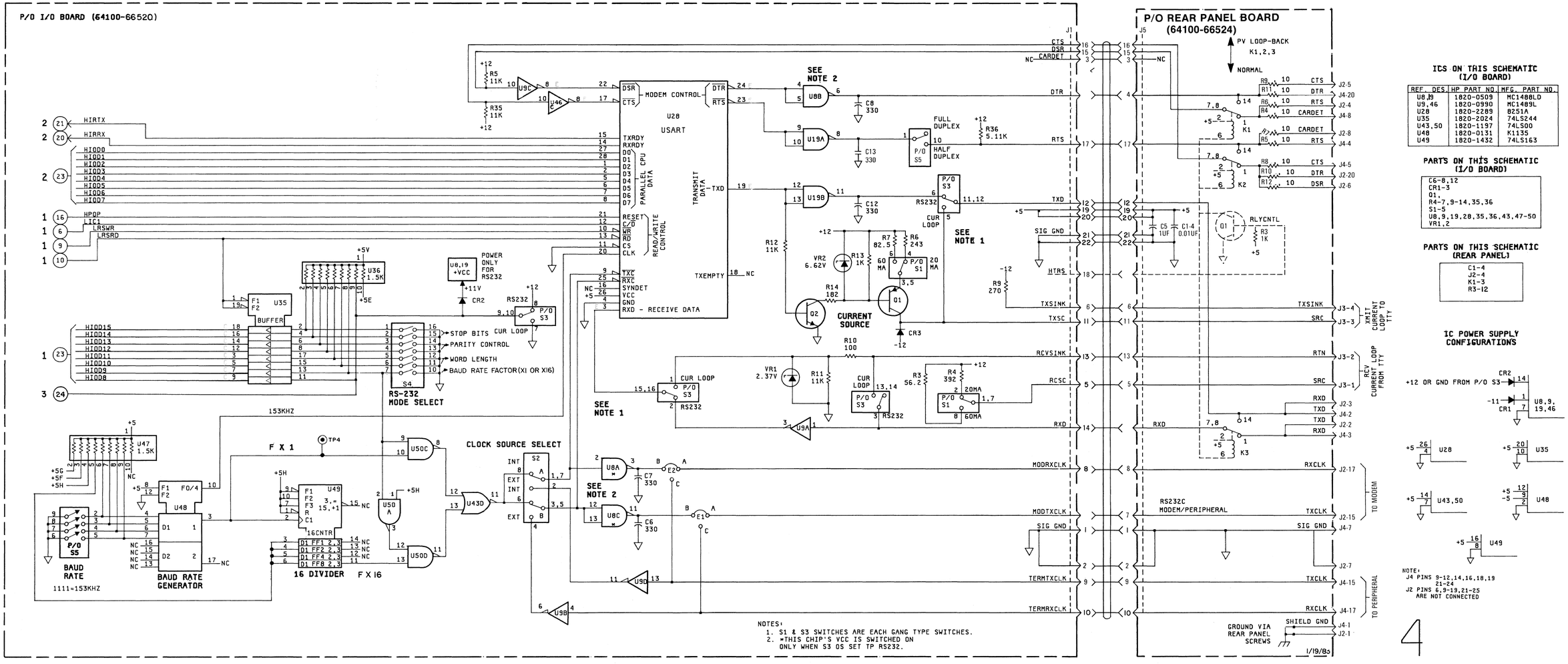


Figure 8-15. Rear-Panel Component



ICs ON THIS SCHEMATIC (I/O BOARD)

REF. DES	HP PART NO.	MFG. PART NO.
U8,19	1820-0509	MC1488LD
U9,46	1820-0990	MC1489L
U28	1820-2289	8251A
U35	1820-2024	74LS244
U43,50	1820-1197	74LS00
U48	1820-0131	K1135
U49	1820-1432	74LS163

PARTS ON THIS SCHEMATIC (I/O BOARD)

C6-8,12
CR1-3
D1
R4-7,9-14,35,36
S1-5
U8,9,19,28,35,36,43,47-50
VR1,2

PARTS ON THIS SCHEMATIC (REAR PANEL)

C1-4
J2-4
K1-3
R3-12

IC POWER SUPPLY CONFIGURATIONS

4

Figure 8-14.
I/O Schematic 4 (Sheet 4 of 5)

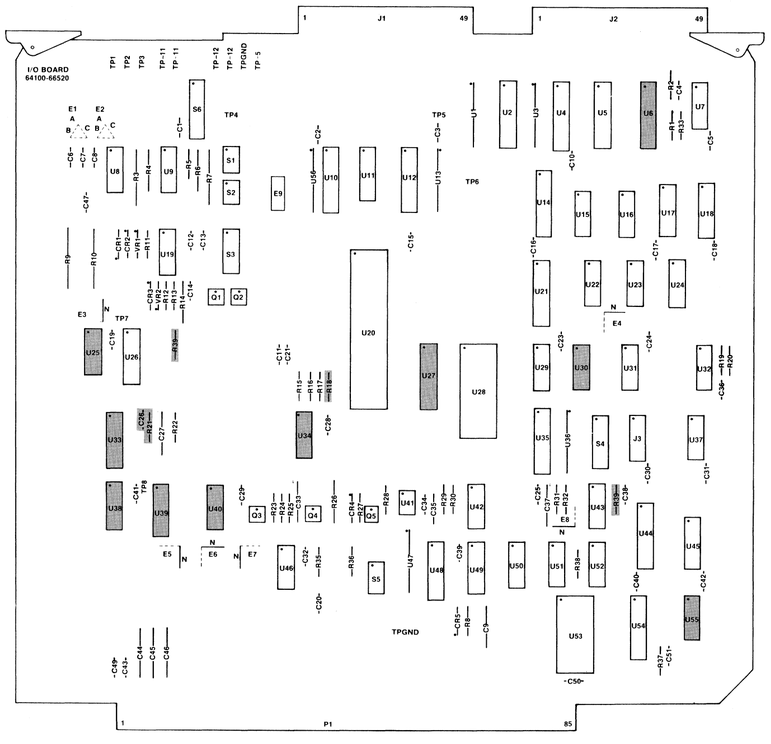


Figure 8-13. I/O Component Locator

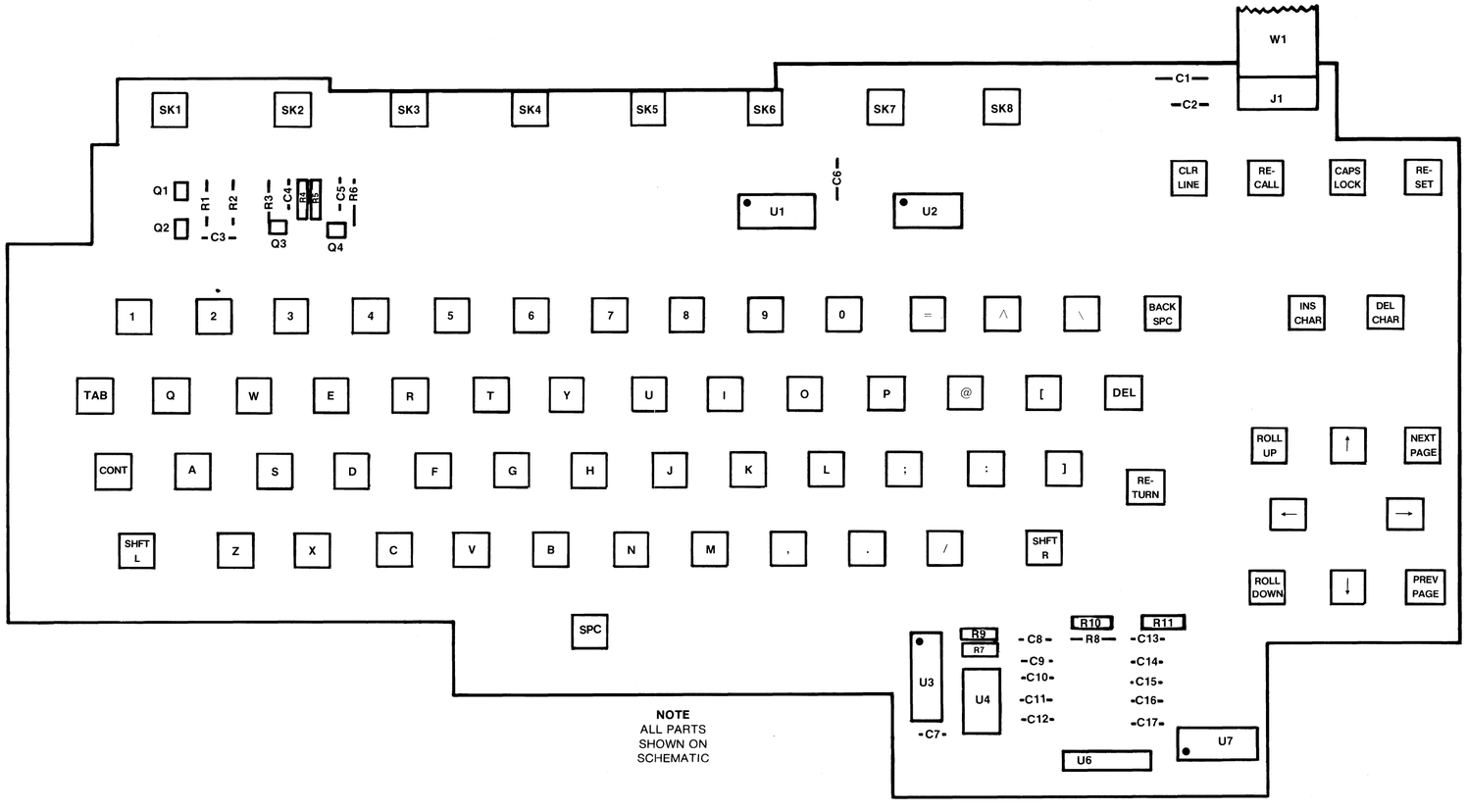
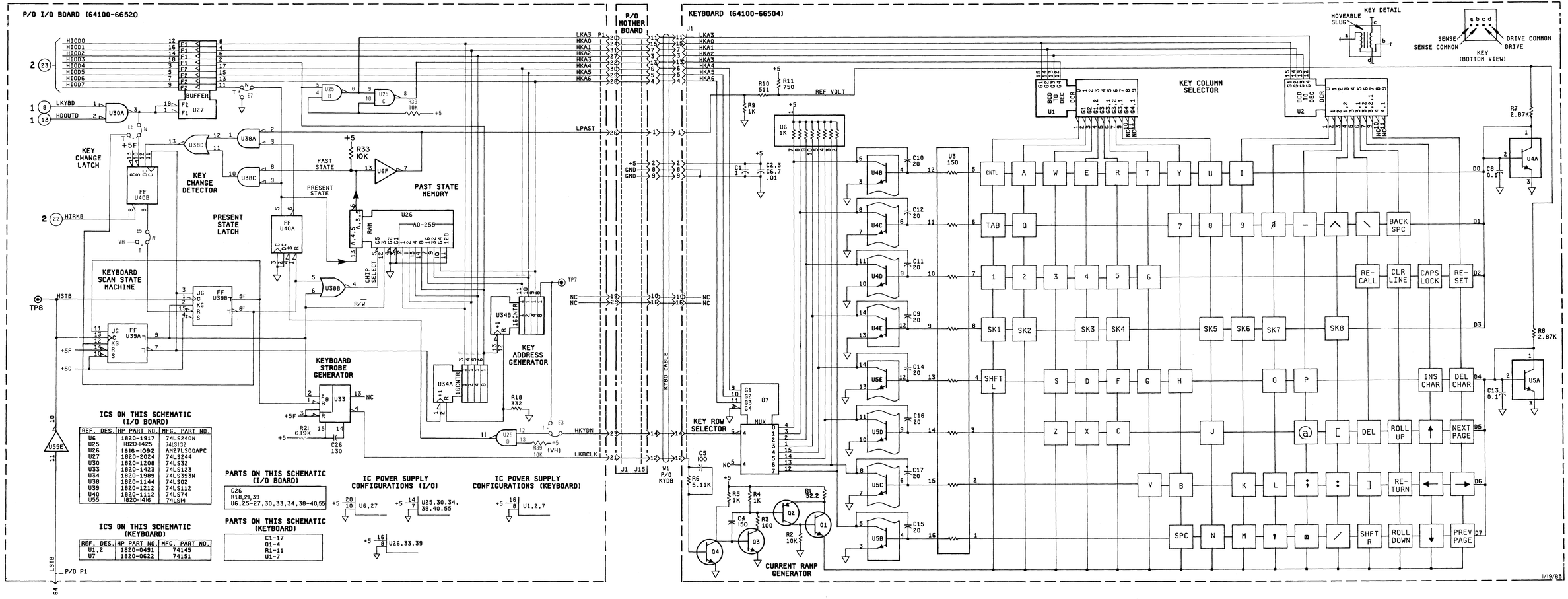


Figure 8-16. Keyboard Component Locator



REF. DES.	HP PART NO.	MFG. PART NO.
U6	1820-1917	74LS240N
U25	1820-1425	74LS132
U26	1816-1092	AM27LS00APC
U27	1820-2024	74LS244
U30	1820-1208	74LS32
U33	1820-1423	74LS123
U34	1820-1989	74LS393N
U38	1820-1144	74LS02
U39	1820-1212	74LS112
U40	1820-1112	74LS74
U55	1820-1416	74LS14

REF. DES.	HP PART NO.	MFG. PART NO.
U1,2	1820-0491	74145
U7	1820-0622	74151

PARTS ON THIS SCHEMATIC (I/O BOARD)

C26
R18,21,39
U6,25-27,30,33,34,38-40,55

PARTS ON THIS SCHEMATIC (KEYBOARD)

C1-17
Q1-4
R1-11
U1-7

IC POWER SUPPLY CONFIGURATIONS (I/O)

+5 20/10 U6,27
+5 14/7 U25,30,34, 38,40,55
+5 16/8 U26,33,39

IC POWER SUPPLY CONFIGURATIONS (KEYBOARD)

+5 16/8 U1,2,7

Figure 8-14.
I/O Schematic 5 (Sheet 5 of 5)
8-49/(8-50 blank)

SERVICE MANUAL

MODEL 64100A

POWER SUPPLY

Manual Part No.: Part of Mainframe Manual
Microfiche Part No.: Part of Mainframe Manual

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LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Cont'd)

LIST OF TABLES

SECTION I

GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. The 64100-62602 power supply is a switching supply designed for component level repair. It is modular in design and easily disassembled. The boards are all edge connected into sockets, except for the main filter board, and have solderless interconnections. LEDs have been placed in the circuitry to indicate strategic failure modes and probable causes.

1-3. The 64100-62602 is a 400 watt power supply that contains three switching supplies, three linear supplies, and one unregulated supply. All of these are on four PC boards within the 64100-62602 container. These are:

a. Filter board and primary wiring	A1	64100-66514
b. Primary board	A2	64100-66515
c. Secondary board	A3	64100-66517
d. Control board	A4	64100-66528

1-4. In addition, the power supply provides three control signals for the mainframe LPOP, LIR15 and LINE SYNC.

1-5. SPECIFICATIONS.

Table 1-1. Specifications

Weight: 13 lbs

Size: 10.75 in X 7.25 in X 5.75 in

Maximum Output Power: 400 watts

Input Voltage: 110 VAC +-15%
220 VAC +-15%

Maximum Input Power: 560 watts 640 VA

Table 1-1. (cont'd)

Supply Voltage		Current Ratings	Type
+5	at	45 Amps max	switching
-5.25	at	25 Amps max	switching
-3.25	at	30 Amps max	switching
+12	at	1 Amp max	linear
-12	at	1 Amp max	linear
+40	at	.25 Amp max 1.6 Amps peak	linear
+17	at	1 Amp max	unregulated

SECTION II

INSTALLATION AND REMOVAL

WARNING

HAZARDOUS voltages are present in the power supply, the CRT, and on the CRT driver board, even with the main power switch set in the OFF position and power cord removed. Use extreme CAUTION while servicing the unit with the top cover removed.

2-1. REMOVAL.

a. Set the power switch to OFF. Disconnect the power cord.

b. Completely remove the five screws that secure the top cover. Lift and remove top cover.

c. Carefully stand the unit on the Rear-panel. Completely remove the 18 screws that secure the bottom panel to the main chassis (see Figure 2-1).

d. Completely remove the 12 screws and lockwashers that connect the power supply to the Motherboard (see Figure 2-2).

e. Completely remove the two screws and washers that connect the bottom of the power supply to the main chassis (see Figure 2-2).

f. Carefully lay unit on its bottom.

CAUTION

Be sure area under unit is clear of screws or other matter which could damage the Motherboard or other circuitry.

CAUTION

Discharge the post accelerator lead to the grounding strap only. Component damage will occur if discharged to other areas.

g. Short out the charge on the CRT by connecting a jumper lead between the ground strap of the CRT and the shaft of a screwdriver. Slip the screwdriver under the protective rubber cup of the post accelerator lead and then momentarily touch the screwdriver to the metal clip of the post accelerator lead.

NOTE

The CRT may charge up by itself even while disconnected. Discharge the CRT by shorting the post accelerator terminal of the CRT to the ground strap with a jumper lead, before handling.

h. Disconnect the post accelerator lead from the CRT.

i. Disconnect the cables at J1 and J2 of the Display driver (see Figure 2-3).

j. Pull the Display driver board straight up from the Motherboard socket.

NOTE: The Display driver can be installed by reversing the order of the removal procedure.

k. Disconnect the fan power cable from the power supply.

l. Completely remove the four screws that secure the power supply to the Rear-panel (see Figure 2-4).

m. Move power supply about half an inch toward the front of instrument and lift supply from chassis.

2-2. INSTALLATION.

a. Place the power supply into the chassis and secure it to the back panel.

b. Slide the Display driver board into the Motherboard slot just in front of power supply.

c. Connect CRT cables to J1 and J2 on the Display driver board.

d. Connect the fan cable to the power supply.

e. Carefully stand unit on the Rear-panel and secure the Motherboard to the main chassis.

f. Secure the bottom cover to the main chassis.

g. Carefully lay unit back to its proper bottom-down position.

h. Secure top cover onto chassis with the top cover screws.

i. Connect the power cable to Rear-panel jack.

j. Installation complete.

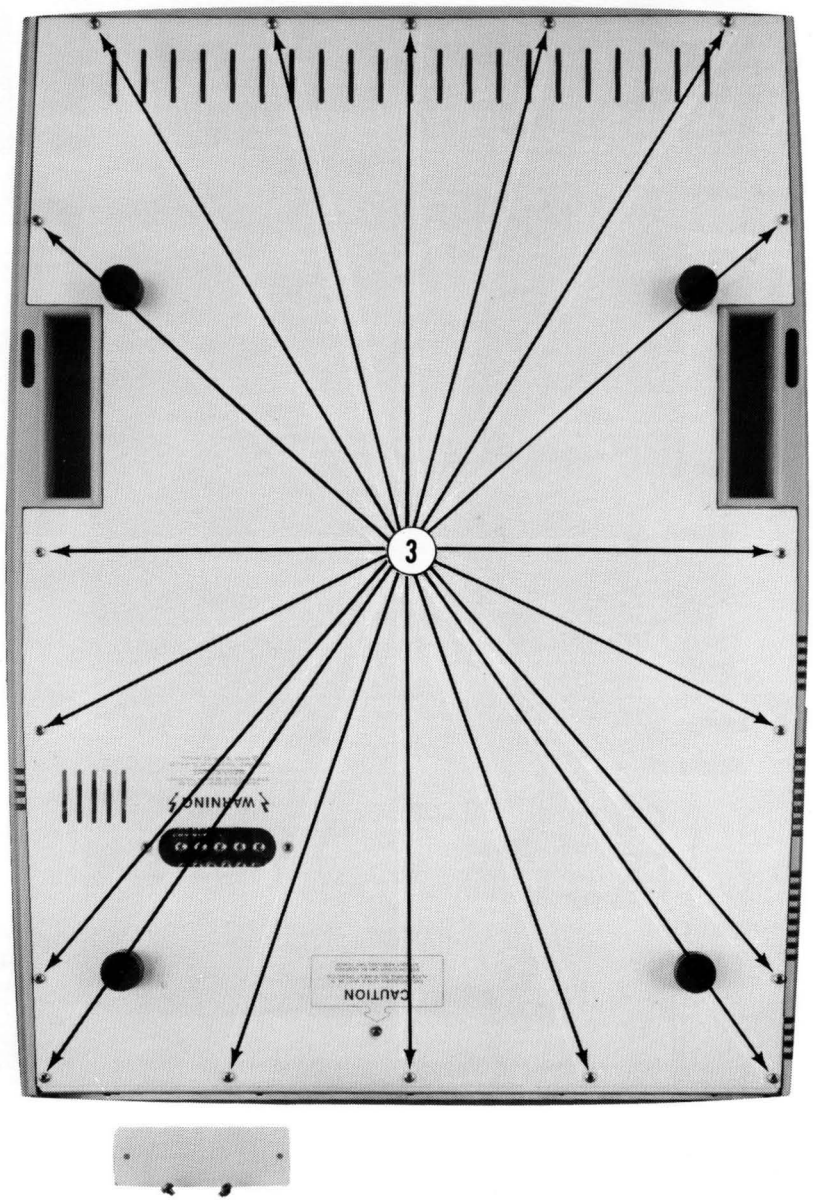


Figure 2-1. Bottom Cover Screw Locations

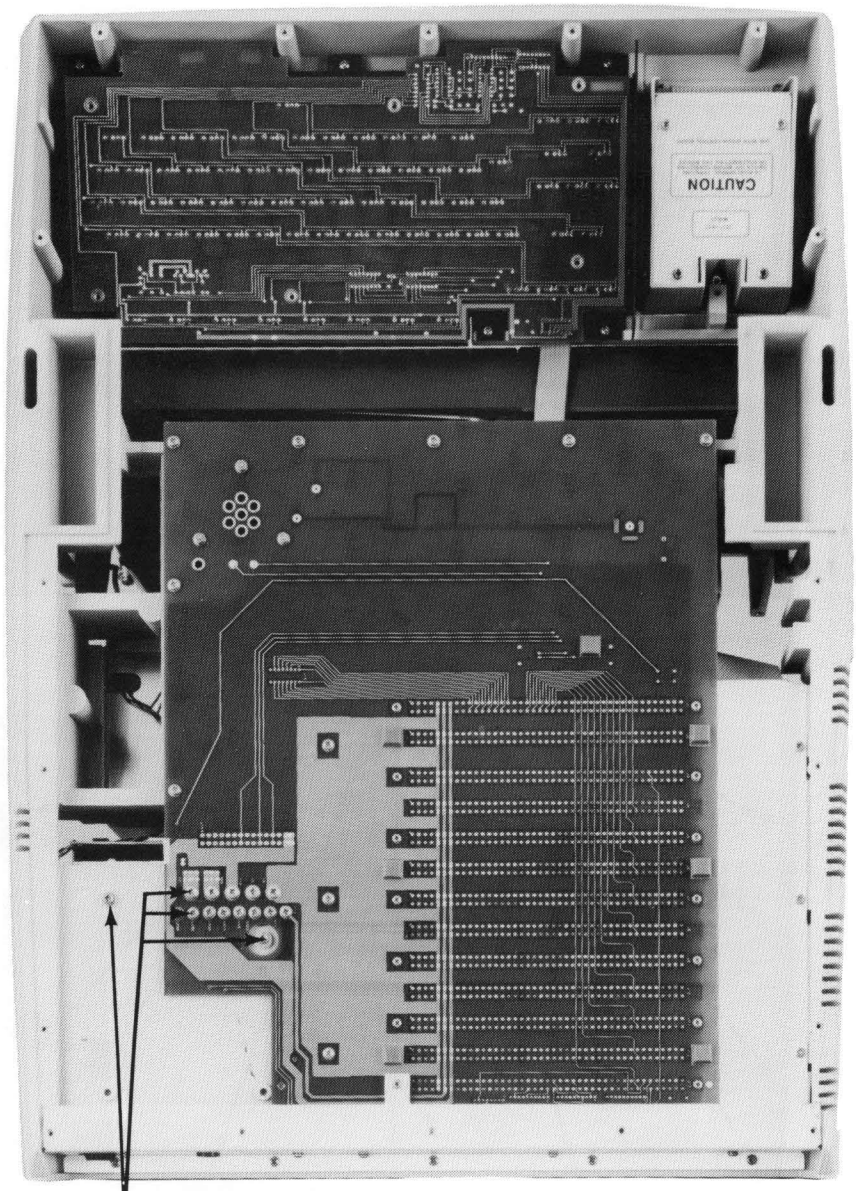


Figure 2-2. Motherboard Screw Locations

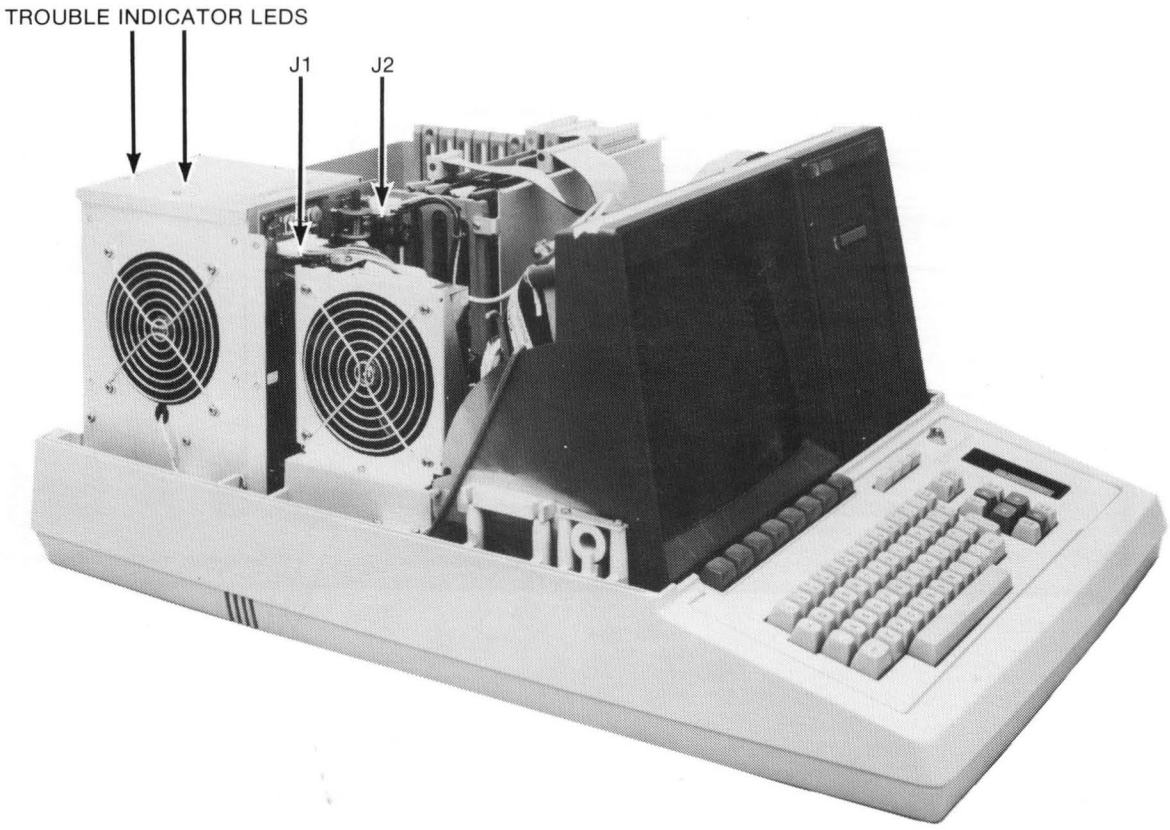


Figure 2-3. Locations of J1, J2 and the LED Indicators

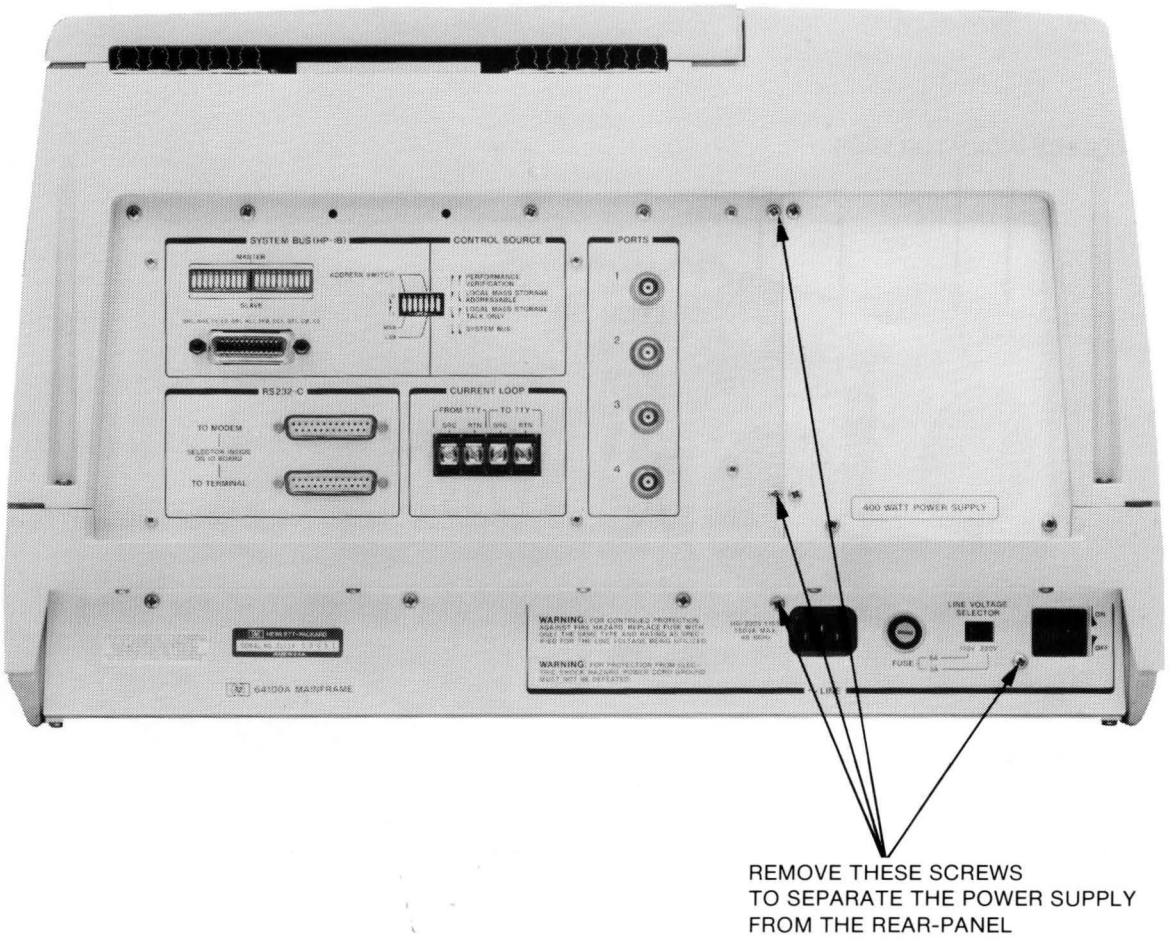


Figure 2-4. Rear-Panel Screw Locations

SECTION III

OPERATION

3-1. GENERAL.

3-2. The power supply operates by setting the power switch to the ON position. Be sure that the AC voltage select switch is in the proper setting for the available line voltage (110V/220V).

3-3. The internal power supply fan must be operating after the mainframe has been tuned ON. The supply will overheat and cause permanent damage to components if the fan is not operating. Turn OFF mainframe if fan is not operating.

SECTION IV

PERFORMANCE VERIFICATION

4-1. REQUIRED EQUIPMENT.

4-2. The test equipment recommended to troubleshoot this power supply are:

Oscilloscope.....100MHz BW, Triggered
Digital Voltmeter.....HP 3466A or equivalent

4-3. POWER SUPPLY VOLTAGES.

4-4. Power supply voltages can be measured at the Motherboard pins listed in table 4-1 or on any card cage board that receives that voltage.

4-5. The power supply can also be checked by using the following procedure.

1. Set the power switch to the OFF position.

2. Remove the five screws that secure the top cover. Lift and remove top cover.

3. Remove all the boards in the card cage. (Refer to Section II for the proper method to remove the Display driver board)

CAUTION

This supply does not need a minimum load to operate. Failure to remove all option and mainframe boards from the card cage could result in permanent damage to parts on these boards.

4. Turn on the supply.

5. Look at the indicator LEDs showing through the top cover of the supply (Figure 2-3). The -3.25V, -5.25V, +5V, +12V and -12V LEDs should only be ON. If this condition does not exist refer to table 4-2.

Table 4-1. Power Supply Voltages on Motherboard Pins

Voltage	Range		Pins	Boards
+5	+4.75	+5.25	3,4,83,84	ALL
-5.25	-4.94	-5.46	5,6,7,8	Disp, CPU, TACO Prom, Floppy
-3.25	-3.32	-3.18	10	
-12	-11.4	-12.6	11,12	I/O, TACO, Prom, Floppy
+12	+11.4	+12.6	13,14	ALL
+17	UNREGULATED ~27V no load		16	Floppy and Tape Control boards only
+40	+38.8	+41.2	17	Prom

Table 4-2. Troubleshooting Guide

LED	ABNORMAL CONDITION	COMMENTS
none		If the +12V or the +5REF voltages are completely off then the following conditions will not exist.
+5	OFF	If the +5V LED is OFF, check the +5V switching circuitry. Refer to paragraphs 8-20 thru 8-29. The -5V supply must be working for this LED to be on.
+5 OV	ON	If this LED is ON, the +5V supply has crowbarred, try a power reset. Check the +5V level and/or the +5 OV circuitry. Repeated firing of the SCR can damage the SCR. Refer to paragraphs 8-35 to 8-38 and 8-44.
-5.25	OFF	If the -5.25V supply is OFF, then all the supplies (including the +5V and -3.25V) will be OFF. Check the -5.25V switching circuitry. If the fans are not running, check the main fuse. Refer to paragraphs 8-20 thru 8-29.

Table 4-2. Troubleshooting Guide (Cont'd)

-5.25 OV	ON	If this LED is ON, the -5.25V supply has crowbarred. Try a power reset. Check the -5.25V level and/or the -5.25 OV circuitry. Repeated firing of the SCR can damage the SCR. Refer to paragraphs 8-35 thru 8-38 and 8-44.
OVER-TEMP or TH	ON	If this LED is ON, the power supply is too warm to operate. Allow the supply to cool. If the TH LED stays ON with the supply being cool, try reseating the boards and P2 cable. Also, check the normally closed thermal switch. Refer to paragraph 8-30.
RATIO	ON	This circuitry uses the sum of the +12V,-5.25V and +5V supplies. If the -5.25V is not present while any of the other two are, this circuit will generate SHUTDOWN. Check other failure LED's. Refer to paragraph 8-47.
PCL	ON	Primary Current Limit detects an unlinear surge of current internal to the supply. If "PCL" comes ON, reseat the boards to get rid of possible intermittant connections. Check for unusual loading of the supply and/or the PCL circuitry. Check to see that the screws connecting the supply to the Motherboard are tight. Refer to paragraph 8-30.
-3.25	OFF	If the -3.25V LED is OFF, check the -3.25V switching circuitry. Refer to paragraphs 8-20 thru 8-29. The -5.25V supply must be working for this LED to be ON
-3.25 OV	ON	When this LED is ON, it indicates that the -3.25V has crowbarred. Check the overvoltage/crowbar circuitry for the -3.25V supply. Refer to paragraphs 8-35 thru 8-38 and 8-44.
-12	OFF	This supply depends on the -5.25V switching circuitry. If the -5.25V is up, check the -12V circuitry. Refer to paragraphs 8-39.
+12	OFF	This supply depends on the -5.25V switching circuitry. If the -5.25V is up, check the +12V circuitry. Refer to paragraphs 8-39.

SECTION V

ADJUSTMENTS

5-1. INTRODUCTION.

5-2 The power supply has three adjustments. These are all on the primary board and effect the +5, -5.25 and -3.25 volt current limits.

5-3. CURRENT LIMIT ADJUSTMENT PROCEDURE.

a. Turn OFF the instrument and remove the top cover.

b. Remove all the boards from the card cage.

c. Remove top cover of the supply.

WARNING

Hazardous voltages are present in the power supply, even with the main power switch OFF and the power cord removed. Use extreme caution while servicing unit with the top cover removed.

d. Remove access port on the bottom cover and apply a 45 amp load (use the ET19705) on the +5V supply (see figure 5-1).

e. Locate the +5V current limit (+5CL) pot R2 as shown in Figure 5-2.

f. Turn ON the supply.

g. Monitor the voltage on the +5 volt supply and turn the pot clockwise until the +5 voltage just begins to drop. Turn the pot counterclockwise until the +5 volt supply is restored to full value and stop.

h. Check the +5V supply to see that it meets specifications.

i. Repeat the above procedure for the -5.25 and -3.25 volt supplies using the appropriate maximum loads for each.

-3.25V = 30 Amps

-5.25V = 25 Amps

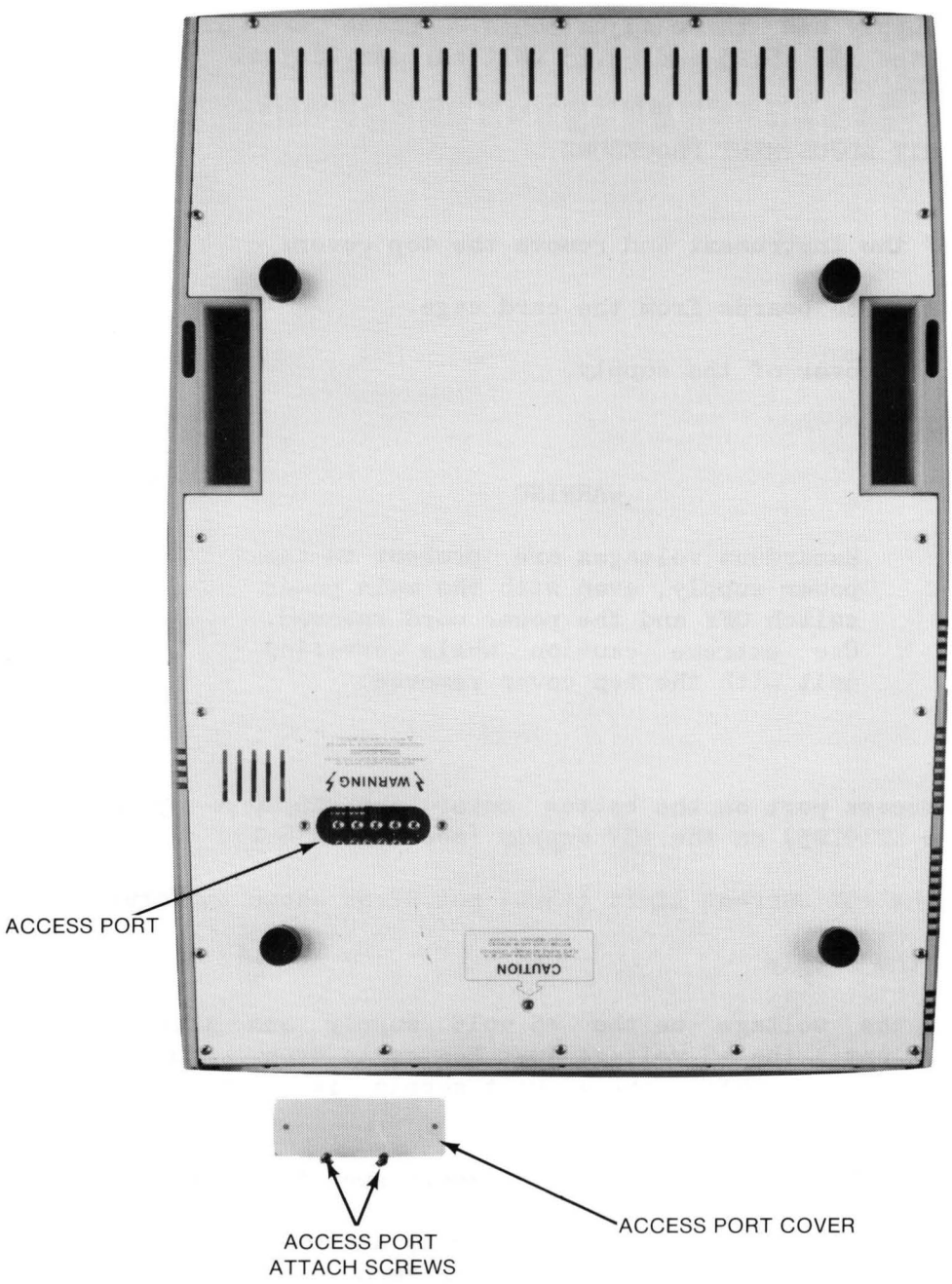


Figure 5-1. Access Port Location

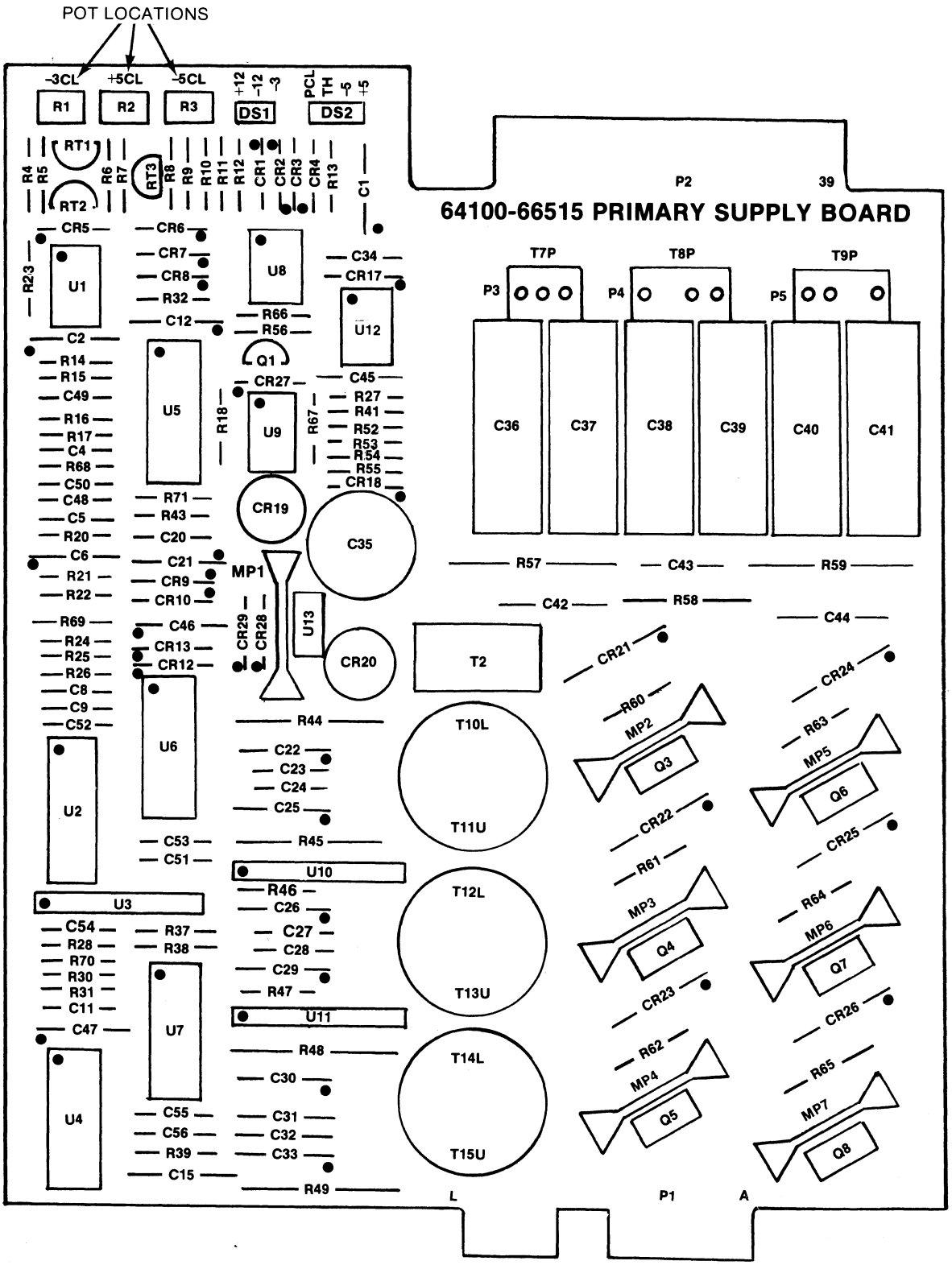


Figure 5-2. Current Limit Pot Locations

SECTION VI

REPLACEABLE PARTS

6-1. INTRODUCTION.

6-2. This section contains information for ordering parts. Table 6-3 lists the names and addresses that correspond to the manufacturers' code numbers. Table 6-1 lists the abbreviations used in the parts list and throughout this manual. Table 6-2 lists all replaceable parts for the power supply.

6-3. ABBREVIATIONS.

6-4. Table 6-1 lists abbreviations used in the parts list, the schematics, and elsewhere in this manual. In some cases two forms of the abbreviation are used; one, all in capital letters, and two, partial or no capitals. This occurs because the abbreviations in the parts list are always all capitals. However, in the schematics and other parts of the manual, other abbreviation forms may be used with both lowercase and uppercase letters.

6-5. ORDERING INFORMATION.

6-6. To order a part listed in the replaceable parts list (See table 6-2), quote the Hewlett-Packard part number and check digit, indicate the quantity required, and address the order to the nearest Hewlett-Packard Office (refer to Sales/Service Offices listed at the back of this manual).

6-7. To order a part that is not listed in table 6-2, include the HP Part Number for the part, the description and function of the part, and the quantity of parts required. Address the order to the nearest Hewlett-Packard Office.

Table 6-1. Reference Designators and Abbreviations

REFERENCE DESIGNATORS

A	= assembly	**F**	= fuse	**MP**	= mechanical part	**U**	= integrated circuit
B	= motor	**FL**	= filter	**P**	= plug	**V**	= vacuum, tube, neon bulb, photocell, etc
BT	= battery	**IC**	= integrated circuit	**Q**	= transistor		
C	= capacitor	**J**	= jack	**R**	= resistor	**VR**	= voltage regulator
CP	= coupler	**K**	= relay	**RT**	= thermistor	**W**	= cable
CR	= diode	**L**	= inductor	**S**	= switch	**X**	= socket
DL	= delay line	**LS**	= loud speaker	**T**	= transformer	**Y**	= crystal
DS	= device signaling (lamp)	**M**	= meter	**TB**	= terminal board	**Z**	= tuned cavity network
E	= misc electronic part	**MK**	= microphone	**TP**	= test point		

ABBREVIATIONS

A	= amperes	**H**	= henries	**N/O**	= normally open	**RMO**	= rack mount only
AFC	= automatic frequency control	**HDW**	= hardware	**NOM**	= nominal	**RMS**	= root-mean square
AMPL	= amplifier	**HEX**	= hexagonal	**NPO**	= negative positive zero (zero temperature coefficient)	**RWV**	= reverse working voltage
		HG	= mercury				
BFO	= beat frequency oscillator	**HR**	= hour(s)				
BE CU	= beryllium copper	**HZ**	= hertz	**NPN**	= negative-positive-negative	**S-B**	= slow-blow
BH	= binder head					**SCR**	= screw
BP	= bandpass			**NRFR**	= not recommended for field replacement	**SE**	= selenium
BRS	= brass	**IF**	= intermediate freq			**SECT**	= section(s)
BWO	= backward wave oscillator	**IMPG**	= impregnated	**NSR**	= not separately replaceable	**SEMICON**	= semiconductor
		INCD	= incandescent			**SI**	= silicon
CCW	= counter-clockwise	**INCL**	= include(s)			**SIL**	= silver
CER	= ceramic	**INS**	= insulation(ed)	**OBD**	= order by description	**SL**	= slide
CMO	= cabinet mount only	**INT**	= internal	**OH**	= oval head	**SPG**	= spring
COEF	= coeficient			**OX**	= oxide	**SPL**	= special
COM	= common	**K**	= kilo=1000			**SST**	= stainless steel
COMP	= composition					**SR**	= split ring
COMPL	= complete	**LH**	= left hand	**P**	= peak	**STL**	= steel
CONN	= connector	**LIN**	= linear taper	**PC**	= printed circuit		
CP	= cadmium plate	**LK WASH**	= lock washer	**PF**	= picofarads= 10^{-12} farads	**TA**	= tantalum
CRT	= cathode-ray tube	**LOG**	= logarithmic taper			**TD**	= time delay
CW	= clockwise	**LPF**	= low pass filter	**PH BRZ**	= phosphor bronze	**TGL**	= toggle
				PHL	= phillips	**THD**	= thread
DEPC	= deposited carbon	**M**	= milli=10^{-3}	**PIV**	= peak inverse voltage	**TI**	= titanium
DR	= drive	**MEG**	= meg=10^{6}	**PNP**	= positive-negative-positive	**TOL**	= tolerance
		MET FLM	= metal film			**TRIM**	= trimmer
ELECT	= electrolytic	**MET OX**	= metallic oxide	**P/O**	= part of	**TWT**	= traveling wave tube
ENCAP	= encapsulated	**MFR**	= manufacturer	**POLY**	= polystyrene		
EXT	= external	**MHZ**	= mega hertz	**PORC**	= porcelain	**U**	= micro=10^{-6}
		MINAT	= miniature	**POS**	= position(s)		
F	= farads	**MOM**	= momentary	**POT**	= potentiometer	**VAR**	= variable
FH	= flat head	**MOS**	= metal oxide substrate	**PP**	= peak-to-peak	**VDCW**	= dc working volts
FIL H	= fillister head	**MTG**	= mounting	**PT**	= point		
FXD	= fixed	**MY**	= "mylar"	**PWV**	= peak working voltage	**W/**	= with
						W	= watts
G	= giga (10^{9})	**N**	= nano (10^{-9})	**RECT**	= rectifier	**WIV**	= working inverse voltage
GE	= germanium	**N/C**	= normally closed	**RF**	= radio frequency		
GL	= glass	**NE**	= neon	**RH**	= round head or right hand	**WW**	= wirewound
GRD	= ground(ed)	**NI PL**	= nickel plate			**W/O**	= without

6-8. DIRECT MAIL ORDER SYSTEM.

6-9. Within the USA, Hewlett-Packard can supply parts through a direct mail order system. Advantages of using this system are:

a. Direct ordering and shipment from the HP Parts Center in Mountain View, California.

b. No maximum or minimum on any mail order (there is a minimum order amount for parts ordered through a local HP office when the orders require billing and invoicing).

c. Prepaid transportation (there is a small handling charge for each order).

d. No invoices (to provide these advantages, a check or money order must accompany each order).

6-10. Mail-order forms and specific ordering information are available through your local HP office. Addresses and phone numbers are located at the back of this manual.

6-11. PARTS LIST.

6-12. Table 6-2 lists the replaceable parts for the power supply.

6-13. The information given for each part consists of the following:

a. Hewlett-Packard part number and check digit. (for HP internal use).

b. Total quantity (Qty) on the PC board.

c. Description of the part.

d. Typical manufacturer of the part in a five-digit code.

e. Manufacturer's number for the part.

NOTE

The total quantity for each part is given only at the first appearance of the part number in the parts list.

Table 6-2. Replaceable Parts List A1

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1	64100-62602	9	1	POWER SUPPLY (CHASSIS MOUNTED PARTS)	28480	64100-62602
F1	2110-0010	9	1	FUSE 5A 250V NTD 1.25X.25 UL (FOR 220V OPERATION)	75915	312005
F1	2110-0528	4	1	FUSE 10A 125V NTD 1.25X.25 (FOR 110V OPERATION)	75915	312010
MP1	64100-62101	3	1	POWER SUPPLY-FAN ASSEMBLY	28480	64100-62101
MP2	9135-0143	8	1	FILTER-LINE	28480	9135-0143
MP3	2110-0565	9	1	FUSE CARRIER	28480	2110-0565
MP4	2110-0566	0	1	FUSE HOLDER BODY	28480	2110-0566
MP5	64100-04707	3	1	SUPPORT PC BOARD	28480	64100-04707
H1	64100-04115	7	1	TOP COVER	28480	64100-04115
H2	2110-0569	3	1	NUT-FUSE HOLDER	28480	2110-0569
S1	3101-0428	5	1	LINE SWITCH (OFF/ON)	28480	3101-0428
S2	3101-2298	1	1	LINE SELECT SWITCH	28480	3101-2298

See introduction to this section for ordering information

Table 6-2. Replaceable Parts List A1 (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1	64100-66514	0	1	FILTER-PC ASSEMBLY	28480	64100-66514
C1	0160-4048	4	1	CAPACITOR-FXD .022UF +-20% 250VAC(RMS)	C0633	PME 271 M 522
C2	0160-4962	1	1	CAPACITOR-FXD 1.0UF 250VDC	28480	0160-4962
C3	0160-5347	3	1	CAPACITOR-FXD 1.0UF 400VDC	28480	0160-5347
C4	0180-3126	9	2	CAPACITOR-FXD 1200UF 200VDC	28480	0180-3126
C5	0180-3126	9		CAPACITOR-FXD 1200UF 200VDC	28480	0180-3126
DS1	1970-0050	8	2	SPARK GAP VOLTAGE	28480	1970-0050
DS2	1970-0050	8		SPARK GAP VOLTAGE	28480	1970-0050
H1	0362-0449	9	4	TERMINAL-CRIMP LUG	28480	0362-0449
H2	0362-0449	9		TERMINAL-CRIMP LUG	28480	0362-0449
H3	0362-0449	9		TERMINAL-CRIMP LUG	28480	0362-0449
H4	0362-0449	9		TERMINAL-CRIMP LUG	28480	0362-0449
H5	0403-0285	9	2	BUMPER FOOT-ADH MTG 12.7-MM-WD	28480	0403-0285
H6	0403-0285	9		BUMPER FOOT-ADH MTG 12.7-MM-WD	28480	0403-0285
H7	0590-0076	1	1	NUT-HEX-PLSTC LKG 4-40-THD .143-IN-THK	28480	0590-0076
RT1	0837-0172	2	3	THERMISTOR DISC 2.5-OHM	15454	SG-3
RT2	0837-0172	2		THERMISTOR DISC 2.5-OHM	15454	SG-3
RT3	0837-0172	2		THERMISTOR DISC 2.5-OHM	15454	SG-3
H11	2190-0011	8	4	WASHER-LK INTL T NO. 10 .195-IN-ID	28480	2190-0011
H12	2190-0011	8		WASHER-LK INTL T NO. 10 .195-IN-ID	28480	2190-0011
H13	2190-0011	8		WASHER-LK INTL T NO. 10 .195-IN-ID	28480	2190-0011
H14	2190-0011	8		WASHER-LK INTL T NO. 10 .195-IN-ID	28480	2190-0011
H15	2200-0121	4	1	SCREW-MACH 4-40 1.125-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H16	2360-0117	6	2	SCREW-MACH 6-32 .375-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H17	2360-0117	6		SCREW-MACH 6-32 .375-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H18	2680-0129	8	4	SCREW-MACH 10-32 .312-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H19	2680-0129	8		SCREW-MACH 10-32 .312-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H20	2680-0129	8		SCREW-MACH 10-32 .312-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H21	2680-0129	8		SCREW-MACH 10-32 .312-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H22	3050-0003	3	5	WASHER-FL NM NO. 6 .141-IN-ID .375-IN-OD	28480	3050-0003
H23	3050-0003	3		WASHER-FL NM NO. 6 .141-IN-ID .375-IN-OD	28480	3050-0003
H24	3050-0003	3		WASHER-FL NM NO. 6 .141-IN-ID .375-IN-OD	28480	3050-0003
H25	3050-0003	3		WASHER-FL NM NO. 6 .141-IN-ID .375-IN-OD	28480	3050-0003
H26	3050-0003	3		WASHER-FL NM NO. 6 .141-IN-ID .375-IN-OD	28480	3050-0003
L1	9140-0624	1	1	INDUCTOR-270UH	28480	9140-0624
P1	1251-0578	9	1	CONNECTOR 19-PIN M 2D SERIES	28480	1251-0578
P2	1251-5339	2	1	CONNECTOR- 9 PIN MALE	28480	1251-5339
R1	0757-0059	4	1	RESISTOR 1M 1% .5W F TC=0+-100	28480	0757-0059
R2	0757-0367	7	2	RESISTOR 100K 1% .5W F TC=0+-100	28480	0757-0367
R3	0757-0367	7		RESISTOR 100K 1% .5W F TC=0+-100	28480	0757-0367
RV1	0837-0120	0	2	VARISTOR - 130VAC	28480	0837-0120
RV2	0837-0120	0		VARISTOR - 130VAC	28480	0837-0120
T1	9100-0417	6	1	TRANSFORMER-POWER	28480	9100-0417
T2	9100-4192	2	1	TRANSFORMER-BALUN	28480	9100-4192

Table 6-2. Replaceable Parts List A2

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A2	64100-66515	1	1	PRIMARY PC ASSEMBLY	28480	64100-66515
C1	0180-0291	3	11	CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
C2	0180-0291	3		CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
C4	0160-4832	4	11	CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C6	0180-0291	3		CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
C8	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C5	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C9	0160-4830	2	1	CAPACITOR-FXD 2200PF +-10% 100VDC CER	28480	0160-4830
C11	01 9-4833	5		CAPACITOR-FXD .022UF +-10% 100VDC CER	28480	0160-4833
C12	0180-0197	8	1	CAPACITOR-FXD 2.2UF+-10% 20VDC TA	56289	150D225X9020A2
C15	0160-0159	0	1	CAPACITOR-FXD 6800PF +-10% 200VDC POLYE	28480	0160-0159
C20	0160-4811	9	2	CAPACITOR-FXD 270PF +-5% 100VDC CER	28480	0160-4811
C21	0180-0291	3		CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
C22	0180-0291	3		CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
C23	0160-4846	0	6	CAPACITOR-FXD 1500PF +-5% 100VDC CER	28480	0160-4846
C24	0160-4846	0		CAPACITOR-FXD 1500PF +-5% 100VDC CER	28480	0160-4846
C25	0180-0291	3		CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
C26	0180-0291	3		CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
C27	0160-4846	0		CAPACITOR-FXD 1500PF +-5% 100VDC CER	28480	0160-4846
C28	0160-4846	0		CAPACITOR-FXD 1500PF +-5% 100VDC CER	28480	0160-4846
C29	0180-0291	3		CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
C30	0180-0291	3		CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
C31	0160-4846	0		CAPACITOR-FXD 1500PF +-5% 100VDC CER	28480	0160-4846
C32	0160-4846	0		CAPACITOR-FXD 1500PF +-5% 100VDC CER	28480	0160-4846
C33	0180-0291	3		CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
C34	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C35	0180-2946	9	1	CAPACITOR-FXD 330UF+50-10% 35VDC AL	28480	0180-2946
C36	0160-5347	8	6	CAPACITOR-FXD 1.0UF 400VDC	28480	0160-5347
C37	0160-5347	8		CAPACITOR-FXD 1.0UF 400VDC	28480	0160-5347
C38	0160-5347	8		CAPACITOR-FXD 1.0UF 400VDC	28480	0160-5347
C39	0160-5347	8		CAPACITOR-FXD 1.0UF 400VDC	28480	0160-5347
C40	0160-5347	8		CAPACITOR-FXD 1.0UF 400VDC	28480	0160-5347
C41	0160-5347	8		CAPACITOR-FXD 1.0UF 400VDC	28480	0160-5347
C42	0140-0180	5	1	CAPACITOR-FXD 2000PF +-2% 300VDC MICA	72136	DM19F202G300WV1CR
C43	0140-0156	5	2	CAPACITOR-FXD 1500PF +-2% 300VDC MICA	72136	DM19F152G300WV1CR
C44	0140-0156	5		CAPACITOR-FXD 1500PF +-2% 300VDC MICA	72136	DM19F152G300WV1CR
C45	0180-1743	3	1	CAPACITOR-FXD .1UF +-10% 35VDAC TC	56289	150D105X9035A2
C46	0180-0229	7	1	CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
C47	0180-0291	3		CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
C48	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C49	0160-4822	2	2	CAPACITOR-FXD 1000PF +-5% 100VDC CER	28480	0160-4822
C50	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C51	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C52	0160-4822	2		CAPACITOR-FXD 1000PF +-5% 100VDC CER	28480	0160-4822
C53	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C54	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C55	0160-4811	9		CAPACITOR-FXD 270PF +-5% 100VDC CER	28480	0160-4811
C56	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
CR1	1901-0050	3	13	DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
CR2	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
CR3	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
CR4	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
CR5	1901-0029	6	3	DIODE-PWR RECT 600V 750MA DO-29	28480	1901-0029
CR6	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
CR7	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
CR8	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
CR9	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
CR10	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
CR12	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
CR13	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
CR17	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
CR18	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
CR19	1906-0051	4	1	DIODE-FW BRDG 100V 1A	28480	1906-0051
CR20	1906-0006	9	1	DIODE-FW BRDG 400V 1A	27777	VE48
CR21	1901-0719	1	6	DIODE-PWR RECT 400V 3A 300NS	04713	MR854
CR22	1901-0719	1		DIODE-PWR RECT 400V 3A 300NS	04713	MR854
CR23	1901-0719	1		DIODE-PWR RECT 400V 3A 300NS	04713	MR854
CR24	1901-0719	1		DIODE-PWR RECT 400V 3A 300NS	04713	MR854
CR25	1901-0719	1		DIODE-PWR RECT 400V 3A 300NS	04713	MR854
CR26	1901-0719	1		DIODE-PWR RECT 400V 3A 300NS	04713	MR854
CR27	1902-3082	9	1	DIODE-ZNR 4.64V 5% DO-35 PD=.4W	28480	1902-3082
CR28	1901-0029	6		DIODE-PWR RECT 600V 750MA DO-29	28480	1901-0029
CR29	1901-0029	6		DIODE-PWR RECT 600V 750MA DO-29	28480	1901-0029

See introduction to this section for ordering information

Table 6-2. Replaceable Parts List A2 (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
DS1	1990-0836	0	1	LED-LAMP ARRAY LUM-INT=500UCD	28480	1990-0836
DS2	1990-0662	0	1	LED-LAMP ARRAY LUM-INT=200UCD IF=5MA-MAX	28480	1990-0662
H1	0590-0076	1	3	NUT-HEX-PLSTC LKG 4-40-THD .143-IN-THK	28480	0590-0076
H2	0590-0076	1		NUT-HEX-PLSTC LKG 4-40-THD .143-IN-THK	28480	0590-0076
H3	0590-0076	1		NUT-HEX-PLSTC LKG 4-40-THD .143-IN-THK	28480	0590-0076
H4	2190-0469	0	7	WASHER-LK INTL T NO. 4 .116-IN-ID	28480	2190-0469
H5	2190-0469	0		WASHER-LK INTL T NO. 4 .116-IN-ID	28480	2190-0469
H6	2190-0469	0		WASHER-LK INTL T NO. 4 .116-IN-ID	28480	2190-0469
H7	2190-0469	0		WASHER-LK INTL T NO. 4 .116-IN-ID	28480	2190-0469
H8	2190-0469	0		WASHER-LK INTL T NO. 4 .116-IN-ID	28480	2190-0469
H9	2190-0469	0		WASHER-LK INTL T NO. 4 .116-IN-ID	28480	2190-0469
H10	2190-0469	0		WASHER-LK INTL T NO. 4 .116-IN-ID	28480	2190-0469
H11	2200-0139	4	7	SCREW-MACH 4-40 .25-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H12	2200-0139	4		SCREW-MACH 4-40 .25-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H13	2200-0139	4		SCREW-MACH 4-40 .25-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H14	2200-0139	4		SCREW-MACH 4-40 .25-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H15	2200-0139	4		SCREW-MACH 4-40 .25-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H16	2200-0139	4		SCREW-MACH 4-40 .25-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H17	2200-0139	4		SCREW-MACH 4-40 .25-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H21	2260-0009	4	7	NUT-HEX-DBL-CHAM 4-40-THD .093-IN-THK	28480	2260-0009
H22	2260-0009	4		NUT-HEX-DBL-CHAM 4-40-THD .093-IN-THK	28480	2260-0009
H23	2260-0009	4		NUT-HEX-DBL-CHAM 4-40-THD .093-IN-THK	28480	2260-0009
H24	2260-0009	4		NUT-HEX-DBL-CHAM 4-40-THD .093-IN-THK	28480	2260-0009
H25	2260-0009	4		NUT-HEX-DBL-CHAM 4-40-THD .093-IN-THK	28480	2260-0009
H26	2260-0009	4		NUT-HEX-DBL-CHAM 4-40-THD .093-IN-THK	28480	2260-0009
H27	2260-0009	4		NUT-HEX-DBL-CHAM 4-40-THD .093-IN-THK	28480	2260-0009
H28	3050-0003	3	3	WASHER-FL NM NO. 6 .141-IN-ID .375-IN-OD	28480	3050-0003
H29	3050-0003	3		WASHER-FL NM NO. 6 .141-IN-ID .375-IN-OD	28480	3050-0003
H30	3050-0003	3		WASHER-FL NM NO. 6 .141-IN-ID .375-IN-OD	28480	3050-0003
MP1	64100-01104	8	7	HEAT SINK SGL PLSTC-PWR-CS	28480	64100-01104
MP2	64100-01104	8		HEAT SINK SGL PLSTC-PWR-CS	28480	64100-01104
MP3	64100-01104	8		HEAT SINK SGL PLSTC-PWR-CS	28480	64100-01104
MP4	64100-01104	8		HEAT SINK SGL PLSTC-PWR-CS	28480	64100-01104
MP5	64100-01104	8		HEAT SINK SGL PLSTC-PWR-CS	28480	64100-01104
MP6	64100-01104	8		HEAT SINK SGL PLSTC-PWR-CS	28480	64100-01104
MP7	64100-01104	8		HEAT SINK SGL PLSTC-PWR-CS	28480	64100-01104
P3	1251-3192	1	1	CONNECTOR 3-PIN M POST TYPE	28480	1251-3192
P4	1251-3195	4	2	CONNECTOR 4-PIN M POST TYPE	28480	1251-3195
P5	1251-3195	4		CONNECTOR 4-PIN M POST TYPE	28480	1251-3195
Q1	1853-0036	2	1	TRANSISTOR PNP SI PD=310MW FT=250MHZ	28480	1853-0036
Q3	1854-0827	1	6	TRANSISTOR NPN SI TO-220AB PD=100W	04713	MJE-13009
Q4	1854-0827	1		TRANSISTOR NPN SI TO-220AB PD=100W	04713	MJE-13009
Q5	1854-0827	1		TRANSISTOR NPN SI TO-220AB PD=100W	04713	MJE-13009
Q6	1854-0827	1		TRANSISTOR NPN SI TO-220AB PD=100W	04713	MJE-13009
Q7	1854-0827	1		TRANSISTOR NPN SI TO-220AB PD=100W	04713	MJE-13009
Q8	1854-0827	1		TRANSISTOR NPN SI TO-220AB PD=100W	04713	MJE-13009
R1	2100-2514	1	3	RESISTOR-TRMR 20K 10% C SIDE-ADJ 1-TRN	30983	ET50W203
R2	2100-2514	1		RESISTOR-TRMR 20K 10% C SIDE-ADJ 1-TRN	30983	ET50W203
R3	2100-2514	1		RESISTOR-TRMR 20K 10% C SIDE-ADJ 1-TRN	30983	ET50W203
R4	0757-0424	7	3	RESISTOR 1.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1101-F
R5	0757-0447	4	1	RESISTOR 16.2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1622-F
R6	0757-0424	7		RESISTOR 1.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1101-F
R7	0757-0451	0	1	RESISTOR 24.3K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2432-F
R8	0757-0424	7		RESISTOR 1.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1101-F
R9	0757-0458	7	1	RESISTOR 51.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5112-F
R10	0757-0429	2	3	RESISTOR 1.82K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1821-F
R11	0757-0429	2		RESISTOR 1.82K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1821-F
R12	0757-0409	8	1	RESISTOR 274 1% .125W F TC=0+-100	24546	C4-1/8-T0-274R-F
R13	0757-0442	9	11	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R14	0757-0465	6	2	RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
R15	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R16	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R17	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R18	0757-0283	6	1	RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2001-F
R20	0757-0280	3	4	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R21	0757-0469	0	1	RESISTOR 150K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1503-F
R22	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R23	0757-0388	2	1	RESISTOR 30.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-30R1-F
R24	0757-0448	5		RESISTOR 18.2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1822-F
R25	0698-6977	1	1	RESISTOR 30K .1% .125W F TC=0+-25	28480	0698-6977
R26	0757-0453	2	2	RESISTOR 30.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3012-F
R27	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R28	0698-4157	5	2	RESISTOR 10K .1% .125W F TC=0+-50	28480	0698-4157

Table 6-2. Replaceable Parts List A2 (Cont'd)

Reference Designation	HP Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
R30	0698-4157	5		RESISTOR 10K .1% .125W F TC=0+-50	28480	0698-4157
R31	0757-0458	9		RESISTOR 51.1K 1% .125W F TC=0+-100	28480	0757-0458
R32	0757-0453	2		RESISTOR 30.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3012-F
R37	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R38	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R39	0757-0436	1	1	RESISTOR 4.32K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4321-F
R41	0757-0481	6	1	RESISTOR 475K 1% .125W F TC=0+-100	19701	MF4C1/8-T0-4753-F
R43	0698-3432	7	1	RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
R44	0757-1090	5	4	RESISTOR 261 1% .5W F TC=0+-100	28480	0757-1090
R45	0757-1090	5		RESISTOR 261 1% .5W F TC=0+-100	28480	0757-1090
R46	0757-0414	5	2	RESISTOR 432 1% .125W F TC=0+-100	24546	C4-1/8-T0-432R-F
R47	0757-0414	5		RESISTOR 432 1% .125W F TC=0+-100	24546	C4-1/8-T0-432R-F
R48	0757-1090	5		RESISTOR 261 1% .5W F TC=0+-100	28480	0757-1090
R49	0757-1090	5		RESISTOR 261 1% .5W F TC=0+-100	28480	0757-1090
R52	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R53	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R54	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R55	0757-0199	3	1	RESISTOR 21.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2152-F
R56	0757-0401	0	1	RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101 -F
R57	0764-0013	5	1	RESISTOR 56 5% 2W MO TC=0+-200	28480	0764-0013
R58	0761-0044	6	1	RESISTOR 82 5% 1W MO TC=0+-200	28480	0761-0044
R59	0698-3618	1	1	RESISTOR 82 5% 2W MO TC=0+-200	27167	FP42-2-T00-82R0-J
R60	0757-0394	0	6	RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-51R1 -F
R61	0757-0394	0		RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-51R1-F
R62	0757-0394	0		RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-51R1 -F
R63	0757-0394	0		RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-51R1-F
R64	0757-0394	0		RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-51R1-F
R65	0757-0394	0		RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-51R1-F
R66	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R67	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R68	0757-0429	2		RESISTOR 1.82K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1821-F
R69	0757-0428	1	1	RESISTOR 1.62K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1621-F
R70	0757-0417	8	1	RESISTOR 562 1% .125W F TC=0+-100	24546	C4-1/8-T0-562R-F
R71	0757-0442	9	1	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
RT1	0837-0180	2	3	THERMISTOR 1K-OHM	01295	TSP102J
RT2	0837-0180	2		THERMISTOR 1K-OHM	01295	TSP102J
RT3	0837-0180	2		THERMISTOR 1K-OHM	01295	TSP102J
T2	9100-4163	7	1	TRANSFORMER	28480	9100-4163
T10	9100-4304	9	6	TRANSFORMER-BASE DRIVE	28480	9100-4304
T11	9100-4304	9		TRANSFORMER-BASE DRIVE	28480	9100-4304
T12	9100-4304	9		TRANSFORMER-BASE DRIVE	28480	9100-4304
T13	9100-4304	9		TRANSFORMER-BASE DRIVE	28480	9100-4304
T14	9100-4304	9		TRANSFORMER-BASE DRIVE	28480	9100-4304
T15	9100-4304	9		TRANSFORMER-BASE DRIVE	28480	9100-4304
U1	1826-0718	0	1	IC-5V REFERENCE	28480	1826-0718
U2	1826-0565	5	3	IC-TL494	28480	1826-0565
U3	1810-0279	5	2	NETWORK-RES 10-SIP4.7K OHM X 9	01121	210A472
U4	1826-0565	5	3	IC-TL494	28480	1826-0565
U5	1826-0565	5		IC-TL494	28480	1826-0565
U6	1820-2111	9	2	IC DRVR TTL INV	01295	SN75468N
U7	1820-2111	9		IC DRVR TTL INV	01295	SN75468N
U8	1826-0468	7	2	IC COMPARATOR GP 8-DIP-P PKG	04713	MC3423P1
U9	1826-0468	7		IC COMPARATOR GP 8-DIP-P PKG	04713	MC3423P1
U10	1810-0279	5		NETWORK-RES 10-SIP4.7K OHM X 9	01121	210A472
U11	1810-0273	9	1	NETWORK-RES 10-SIP470.0 OHM X 9	01121	210A471
U12	1826-0346	0	1	IC OP AMP GP DUAL 8-DIP-P PKG	27014	LM358N
U13	1826-0345	9	1	IC V RGLTR TO-220	07263	UA78M12UC

Table 6-2. Replaceable Parts List A3

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A3	64100-66517	3	1	SECONDARY-PC ASSEMBLY	28480	64100-66517
C1	0170-0066	9	2	CAPACITOR-FXD .027UF +-10% 200VDC POLYE	28480	0170-0066
C2	0180-3046	2	6	CAPACITOR-FXD 3300UF 6.3VDC	28480	0180-3046
C3	0180-3046	2		CAPACITOR-FXD 3300UF 6.3VDC	28480	0180-3046
C4	0160-0168	1	1	CAPACITOR-FXD .1UF +-10% 200VDC POLYE	28480	0160-0168
C5	0180-3046	2		CAPACITOR-FXD 3300UF 6.3VDC	28480	0180-3046
C6	0180-3046	2		CAPACITOR-FXD 3300UF 6.3VDC	28480	0180-3046
C7	0160-0174	9	1	CAPACITOR-FXD .47UF +-10% 50VDC CER	28480	0160-0174
C8	0160-0158	9	1	CAPACITOR-FXD 5600PF +-10% 200VDC POLYE	28480	0160-0158
C9	0180-2946	9	1	CAPACITOR-FXD 330UF 35VDC	28480	0180-2946
C10	0180-0197	8	1	CAPACITOR-FXD 2.2UF+-10% 20VDC TA	56289	150D225X9020A2
C11	0180-0094	4	1	CAPACITOR-FXD 100UF+75-10% 25VDC AL	56289	30D107G025DD2
C12	0170-0066	9		CAPACITOR-FXD .027UF +-10% 200VDC POLYE	28480	0170-0066
C13	0180-3046	2		CAPACITOR-FXD 3300UF 6.3VDC	28480	0180-3046
C14	0180-3046	2		CAPACITOR-FXD 3300UF 6.3VDC	28480	0180-3046
C15	0160-0161	4	1	CAPACITOR-FXD .01UF +-10% 200VDC POLYE	28480	0160-0161
C16	0160-4822	2	1	CAPACITOR-FXD 1000PF +-5% 100VDC CER	28480	0160-4822
C17	0160-0298	8	1	CAPACITOR-FXD 1500PF +-10% 200VDC POLYE	28480	0160-0298
CR1	1906-0079	6	2	DIODE-FW BRDG 100V 10A	27777	VJ148X
CR2	1906-0079	6		DIODE-FW BRDG 100V 10A	27777	VJ148X
CR3	1901-0028	5	1	DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
CR4	1901-0050	3	3	DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
CR5	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
CR6	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
CR8	1901-0727	1	6	DIODE-PWR RECT 35V 60A 10NS DO-5	28480	1901-0727
CR9	1901-0727	1		DIODE-PWR RECT 35V 60A 10NS DO-5	28480	1901-0727
CR10	1901-0727	1		DIODE-PWR RECT 35V 60A 10NS DO-5	28480	1901-0727
CR11	1901-0727	1		DIODE-PWR RECT 35V 60A 10NS DO-5	28480	1901-0727
CR12	1901-0727	1		DIODE-PWR RECT 35V 60A 10NS DO-5	28480	1901-0727
CR13	1901-0727	1		DIODE-PWR RECT 35V 60A 10NS DO-5	28480	1901-0727
E1	0340-0473	3	1	INSULATOR-XSTR THERMA-FILM	28480	0340-0473
E2	0380-0339	4	2	STANDOFF-RVT-ON .25-IN-LG 4-40THD	00000	ORDER BY DESCRIPTION
E3	0380-0339	4		STANDOFF-RVT-ON .25-IN-LG 4-40THD	00000	ORDER BY DESCRIPTION
E4	0380-0741	2	2	STANDOFF-RVT-ON .187-IN-LG 6-32THD	00000	ORDER BY DESCRIPTION
E5	0380-0741	2		STANDOFF-RVT-ON .187-IN-LG 6-32THD	00000	ORDER BY DESCRIPTION
E6	3050-0791	6	1	INSULATOR-TRANSISTOR, NYLON	28480	3050-0791
H1-17	2190-0017	4	17	WASHER-LK HLCL NO. 8 .168-IN-ID	28480	2190-0017
H18	2200-0105	4	3	SCREW-MACH 4-40 .312-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H19	2200-0105	4		SCREW-MACH 4-40 .312-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H20	2200-0105	4		SCREW-MACH 4-40 .312-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H21	2200-0111	2	2	SCREW-MACH 4-40 .5-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H22	2200-0111	2		SCREW-MACH 4-40 .5-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H23	2200-0121	4	4	SCREW-MACH 4-40 1.125-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H24	2200-0121	4		SCREW-MACH 4-40 1.125-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H25	2200-0121	4		SCREW-MACH 4-40 1.125-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H26	2200-0121	4		SCREW-MACH 4-40 1.125-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H27	2200-0180	5	3	SCREW-MACH 4-40 1.375-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H28	2200-0180	5		SCREW-MACH 4-40 1.375-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H29	2200-0180	5		SCREW-MACH 4-40 1.375-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H30	2360-0121	2	2	SCREW-MACH 6-32 .5-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H31	2360-0121	2		SCREW-MACH 6-32 .5-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H32	0590-0076	1	7	NUT-HEX-PLSTC LKG 4-40-THD .143-IN-THK	28480	0590-0076
H33	0590-0076	1		NUT-HEX-PLSTC LKG 4-40-THD .143-IN-THK	28480	0590-0076
H34	0590-0076	1		NUT-HEX-PLSTC LKG 4-40-THD .143-IN-THK	28480	0590-0076
H35	0590-0076	1		NUT-HEX-PLSTC LKG 4-40-THD .143-IN-THK	28480	0590-0076
H36	0590-0076	1		NUT-HEX-PLSTC LKG 4-40-THD .143-IN-THK	28480	0590-0076
H37	0590-0076	1		NUT-HEX-PLSTC LKG 4-40-THD .143-IN-THK	28480	0590-0076
H38	0590-0076	1		NUT-HEX-PLSTC LKG 4-40-THD .143-IN-THK	28480	0590-0076
H39-52	2510-0103	9	14	SCREW-MACH 8-32 .375-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H53	2580-0004	6	3	NUT-HEX-DBL-CHAM 8-32-THD .125-IN-THK	00000	ORDER BY DESCRIPTION
H54	2580-0004	6		NUT-HEX-DBL-CHAM 8-32-THD .125-IN-THK	00000	ORDER BY DESCRIPTION
H55	2580-0004	6		NUT-HEX-DBL-CHAM 8-32-THD .125-IN-THK	00000	ORDER BY DESCRIPTION
H56	3050-0003	3	6	WASHER-FL MM NO. 6 .141-IN-ID .375-IN-OD	28480	3050-0003
H57	3050-0003	3		WASHER-FL MM NO. 6 .141-IN-ID .375-IN-OD	28480	3050-0003
H58	3050-0003	3		WASHER-FL MM NO. 6 .141-IN-ID .375-IN-OD	28480	3050-0003
H59	3050-0003	3		WASHER-FL MM NO. 6 .141-IN-ID .375-IN-OD	28480	3050-0003
H60	3050-0003	3		WASHER-FL MM NO. 6 .141-IN-ID .375-IN-OD	28480	3050-0003
H61	3050-0003	3		WASHER-FL MM NO. 6 .141-IN-ID .375-IN-OD	28480	3050-0003
H62	3050-0100	1	4	WASHER-FL MTLC NO. 6 .147-IN-ID	28480	3050-0100

Table 6-2. Replaceable Parts List A3 (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
H63	3050-0100	1		WASHER-FL MTLC NO. 6 .147-IN-ID	28480	3050-0100
H64	3050-0100	1		WASHER-FL MTLC NO. 6 .147-IN-ID	28480	3050-0100
H65	3050-0100	1		WASHER-FL MTLC NO. 6 .147-IN-ID	28480	3050-0100
H66	3050-1049	9	3	WASHER-FLAT, INSL	86928	5620-35-31
H67	3050-1049	9		WASHER-FLAT, INSL	86928	5620-35-31
H68	3050-1049	9		WASHER-FLAT, INSL	86928	5620-35-31
L1	9140-0618	3	1	INDUCTOR-39UH	28480	9140-0618
L2	9140-0623	0	2	INDUCTOR-2UH	28480	9140-0623
L3	9140-0617	2	2	INDUCTOR-14UH	28480	9140-0617
L4	9140-0619	4	1	INDUCTOR-3UH	28480	9140-0619
L5	9140-0625	2	1	INDUCTOR-10UH	28480	9140-0625
L6	9140-0617	2		INDUCTOR-14UH	28480	9140-0617
L7	9140-0623	0		INDUCTOR-2UH	28480	9140-0623
MP1	64100-61103	3	1	HEAT SINK ASSY+5	28480	64100-61103
MP2	64100-61102	2	1	HEAT SINK ASSY-5	28480	64100-61102
MP3	64100-61101	1	1	HEAT SINK ASSY-3	28480	64100-61101
MP4	1205-0266	7	1	HEAT SINK SGL TO-3-CS	28480	1205-0266
MP5	64100-01101	5	1	HEAT SINK-BRIDGE	28480	64100-01101
MP6	64100-01103	7	1	HEAT SINK-+12	28480	64100-01103
MP7	64100-47501	5	1	TERMINAL BLOCK	28480	64100-47501
P3	1251-3767	6	1	CONNECTOR 7-PIN M POST TYPE	28480	1251-3767
P4	1251-3195	4	3	CONNECTOR 4-PIN M POST TYPE	28480	1251-3195
P5	1251-3618	6	1	CONNECTOR 2-PIN M POST TYPE	28480	1251-3618
Q1	1854-0828	2	1	TRANSISTOR NPN SI TO-220AB PD=65W	01295	TIP-122
Q2	1884-0295	0	2	THYRISTOR-SCR	04713	MCR69-1
Q3	1884-0295	0		THYRISTOR-SCR	04713	MCR69-1
R1	0698-0093	0	3	RESISTOR 10 5% 1W MO TC=0+-200	28480	0698-0093
R2	0811-3579	5	1		28480	0811-3579
R3	5080-1814	1	4	SHUNT-DMS 25M	28480	5080-1814
R4	0757-0280	3	2	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R5	0698-0093	0		RESISTOR 10 5% 1W MO TC=0+-200	28480	0698-0093
R6	5080-1814	1		SHUNT-DMS 25M	28480	5080-1814
R7	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R8	0757-0420	3	1	RESISTOR 750 1% .125W F TC=0+-100	24546	C4-1/8-T0-7501-F
R9	0698-3444	1	1	RESISTOR 316 1% .125W F TC=0+-100	24546	C4-1/8-T0-316R-F
R10	0757-0465	6	2	RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
R11	0757-0795	5	1	RESISTOR 75 1% .5W F TC=0+-100	19701	MF-1/2-T0-75R0-F
R12	0698-3132	4	1	RESISTOR 261 1% .125W F TC=0+-100	24546	C4-1/8-T0-2610-F
R13	0757-0274	5	1	RESISTOR 1.21K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1211-F
R14	0698-0093	0		RESISTOR 10 5% 1W MO TC=0+-200	28480	0698-0093
R15	5080-1814	1		SHUNT-DMS 25M	28480	5080-1814
R16	0757-1000	7	1	RESISTOR 51.1 1% .5W F TC=0+-100	28480	0757-1000
R17	5080-1814	1		SHUNT-DMS 25M	28480	5080-1814
R18	0757-0420	3	1	RESISTOR 750 1% .125W F TC=0+-100	24546	C4-1/8-T0-751-F
R19	0757-0465	6		RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
R20	0757-0452	1	1	RESISTOR 27.4K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2742-F
R21	0698-3401	0	1	RESISTOR 215 1% .5W F TC=0+-100	28480	0698-3401
R22	0757-0409	8	1	RESISTOR 274 1% .125W F TC=0+-100	24546	C4-1/8-T0-274R-F
R23	0698-8812	7	1	RESISTOR 1 1% .125W F TC=0+-100	28480	0698-8812
S1	3103-0091	2	1	THERMAL SWITCH	28480	3103-0091
T7	9100-4161	5	1	TRANSFORMER	28480	9100-4161
T8	9100-4160	4	1	TRANSFORMER	28480	9100-4160
T9	9100-4152	4	1	TRANSFORMER	28480	9100-4152
U1	1826-0346	0	1	IC OP AMP GP DUAL 8-DIP-P PKG	27014	LM358N
U2	1826-0677	0	1		28480	1826-0677

See introduction to this section for ordering information

Table 6-2. Replaceable Parts List A4

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A4	64100-66528	6	1	CONTROL PC ASSEMBLY	28480	64100-66528
C1	0160-3622	8	3	CAPACITOR-FXD .1UF +80-20% 100VDC CER	26654	2130Y5V100R104Z
C2	0160-3622	8		CAPACITOR-FXD .1UF +80-20% 100VDC CER	26654	2130Y5V100R104Z
C3	0160-3508	9	1	CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
C4	0160-3622	8		CAPACITOR-FXD .1UF +80-20% 100VDC CER	26654	2130Y5V100R104Z
C5	0180-0197	8	5	CAPACITOR-FXD 2.2UF+-10% 20VDC TA	56289	150D225X9020A2
C6	0180-0197	8		CAPACITOR-FXD 2.2UF+-10% 20VDC TA	56289	150D225X9020A2
C7	0160-4822	2	1	CAPACITOR-FXD 1000PF +-5% 100VDC CER	28480	0160-4822
C8	0160-4833	5	1	CAPACITOR-FXD .022UF +-10% 100VDC CER	28480	0160-4833
C9	0180-2946	9	2	CAPACITOR-FXD 330UF+50-10% 35VDC AL	28480	0180-2946
C10	0180-0197	8		CAPACITOR-FXD 2.2UF+-10% 20VDC TA	56289	150D225X9020A2
C11	0180-3127	0	1	CAPACITOR-FXD 180UF 75VDC	28480	0180-3127
C12	0180-0141	2	1	CAPACITOR-FXD 50UF+75-10% 50VDC AL	56289	30D506G050DD2
C13	0180-0197	8		CAPACITOR-FXD 2.2UF+-10% 20VDC TA	56289	150D225X9020A2
C14	0160-4832	4	1	CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C15	0180-2946	9		CAPACITOR-FXD 330UF+50-10% 35VDC AL	28480	0180-2946
C16	0180-0197	8		CAPACITOR-FXD 2.2UF+-10% 20VDC TA	56289	150D225X9020A2
CR1	1901-0050	3	5	DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
CR2	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
CR3	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
CR4	1901-0028	5	3	DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
CR5	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
CR6	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
CR7	1901-0028	5		DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
CR8	1901-0028	5		DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
CR9	1906-0051	4	1	DIODE-FW BRDG 100V 1A	28480	1906-0051
CR10	1901-0535	9	1	DIODE-SM SIG SCHOTTKY	28480	1901-0535
DS1	1990-0662	0	1	LED-LAMP ARRAY LUM-INT=200UCD IF=5MA-MAX	28480	1990-0662
H1	0590-0076	1	3	NUT-HEX-PLSTC LKG 4-40-THD .143-IN-THK	28480	0590-0076
H2	0590-0076	1		NUT-HEX-PLSTC LKG 4-40-THD .143-IN-THK	28480	0590-0076
H3	0590-0076	1		NUT-HEX-PLSTC LKG 4-40-THD .143-IN-THK	28480	0590-0076
H4	2200-0121	4	3	SCREW-MACH 4-40 1.125-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H5	2200-0121	4		SCREW-MACH 4-40 1.125-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H6	2200-0121	4		SCREW-MACH 4-40 1.125-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H7	2360-0113	2	2	SCREW-MACH 6-32 .25-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H8	2360-0113	2		SCREW-MACH 6-32 .25-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H9	2420-0003	7	2	NUT-HEX-DBL-CHAM 6-32-THD .094-IN-THK	00000	ORDER BY DESCRIPTION
H10	2420-0003	7		NUT-HEX-DBL-CHAM 6-32-THD .094-IN-THK	00000	ORDER BY DESCRIPTION
H11	3050-0003	3	3	WASHER-FL MM NO. 6 .141-IN-ID .375-IN-OD	28480	3050-0003
H12	3050-0003	3		WASHER-FL MM NO. 6 .141-IN-ID .375-IN-OD	28480	3050-0003
H13	3050-0003	3		WASHER-FL MM NO. 6 .141-IN-ID .375-IN-OD	28480	3050-0003
L1	9140-0622	9	1	INDUCTOR-1200UH	28480	9140-0622
L2	9140-0620	7	1	INDUCTOR-680UH	28480	9140-0620
L3	9140-0621	8	1	INDUCTOR-680UH	28480	9140-0621
MP1	1205-0373	7	2	HEAT SINK SGL PLSTC-PWR-CS	13103	6030B-TT
MP2	1205-0373	7		HEAT SINK SGL PLSTC-PWR-CS	13103	6030B-TT
Q1	1853-0020	4	2	TRANSISTOR PNP SI PD=300MW FT=150MHZ	28480	1853-0020
Q2	1854-0215	1	2	TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
Q3	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
Q4	1853-0468	4	1	TRANSISTOR PNP SI DARL TO-220AB PD=65W	01295	TIP-127
Q5	1853-0020	4		TRANSISTOR PNP SI PD=300MW FT=150MHZ	28480	1853-0020
R1	0757-0415	6	1	RESISTOR 475 1% .125W F TC=0+-100	24546	C4-1/8-T0-475R-F
R2	0757-0426	9	2	RESISTOR 1.3K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1301-F
R3	0757-0280	3	8	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R4	0698-3405	4	1	RESISTOR 422 1% .5W F TC=0+-100	28480	0698-3405
R5	0757-0402	1	2	RESISTOR 110 1% .125W F TC=0+-100	24546	C4-1/8-T0-111-F
R6	0757-0426	9		RESISTOR 1.3K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1301-F
R7	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R8	0757-1090	5	1	RESISTOR 261 1% .5W F TC=0+-100	28480	0757-1090
R9	0757-0402	1		RESISTOR 110 1% .125W F TC=0+-100	24546	C4-1/8-T0-111-F
R10	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R11	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R12	0757-0438	3	1	RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
R13	0757-0283	6	1	RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2001-F
R14	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R15	0757-0418	9	1	RESISTOR 619 1% .125W F TC=0+-100	24546	C4-1/8-T0-619R-F
R16	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R18	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R19	0757-0458	7	2	RESISTOR 51.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5112-F
R20	0757-0442	9	4	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R21	0757-0481	6	2	RESISTOR 475K 1% .125W F TC=0+-100	19701	MF4C1/8-T0-4753-F

Table 6-2. Replaceable Parts List A4 (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
R22	0757-0465	6	4	RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
R23	0757-0438	3	1	RESISTOR 5.11K 1% .125W F TC=0 +-100	24546	C4-1/8-T0-5111-F
R24	0757-0472	5	2	RESISTOR 200K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2003-F
R25	0757-0465	6		RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
R26	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R27	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R28	0757-0413	4	1	RESISTOR 392 1% .125W F TC=0+-100	24546	C4-1/8-T0-392R-F
R29	0811-1659	8	1	RESISTOR .27 5% 2W PW TC=0+-800	75042	BWH2-27/100-J
R30	0757-0284	7	1	RESISTOR 150 1% .125W F TC=0+-100	24546	C4-1/8-T0-151-F
R31	0757-0465	6		RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
R32	0757-0452	1	1	RESISTOR 27.4K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2742-F
R33	0757-0458	7		RESISTOR 51.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5112-F
R34	0757-0465	6		RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
R35	0757-0281	4	1	RESISTOR 2.74K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2741-F
R36	0757-0448	5	1	RESISTOR 18.2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1822-F
R37	0698-0085	0	1	RESISTOR 2.61K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2611-F
R38	0757-0472	5		RESISTOR 200K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2003-F
R39	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R40	0757-0481	6		RESISTOR 475K 1% .125W F TC=0+-100	19701	MF4C1/8-T0-4753-F
R41	0761-0010	6	1	RESISTOR 1.8K 5% 1W MO TC=0+-200	28480	0761-0010
U1	1820-1577	9	1	IC SCHMITT-TRIG CMOS NAND QUAD 2-INP	0192B	CD4093BF
U2	1820-2019	6	1	IC SCHMITT-TRIG CMOS HEX	04713	MC14584BCP
U3	1826-0346	0	1	IC OP AMP GP DUAL 8-DIP-P PKG	27014	LM358N
U4	1826-0680	5	4	IC 8-DIP-P PKG	28480	1826-0680
U5	1826-0680	5		IC 8-DIP-P PKG	28480	1826-0680
U6	1826-0680	5		IC 8-DIP-P PKG	28480	1826-0680
U7	1826-0680	5		IC 8-DIP-P PKG	28480	1826-0680
U8	1826-0221	0	1	IC -12 V RGLTR TO-220	04713	MC7912CT
U9	1818-0277	9	1	RES NETWORK 2.2K X 9	28480	1810-0277
XU4	1200-0796	8	4	8 PIN DIP SOCKET	28480	1200-0796
XU5	1200-0796	8		8 PIN DIP SOCKET	28480	1200-0796
XU6	1200-0796	8		8 PIN DIP SOCKET	28480	1200-0796
XU7	1200-0796	8		8 PIN DIP SOCKET	28480	1200-0796

See introduction to this section for ordering information

Table 6-3. List of Manufacturers' Codes

MFR NO.	MANUFACTURER NAME	ADDRESS	ZIP CODE
00000	Any Satisfactory Supplier		
00466	Norelco N. Amer Philips Corp	Los Angeles Ca	90021
01121	Allen-Bradley Co	Milwaukee Wi	53204
01295	Texas Instr Semicond Div	Dallas Tx	75222
01928	RCA Corp Solid State Div	Somerville NJ	08876
03888	KDI Pyrofilm Corp	Whippany NJ	07981
04713	Motorola Semicond Products	Phoenix Az	85062
07263	Fairchild Semicond Div	Mountain View Ca	94042
09023	Cornell-Dubilier Eleck Div	Sanford NC	27330
13103	Thermalloy Co	Dallas Tx	75234
19701	Mepco/Electra Corp	Mineral Wells Tx	76067
20940	Micro-Ohm Corp	El Monte Ca	91731
24546	Corning Glass Wks	Bradford Pa	16701
26654	Varadyne Inc	Santa Monica Ca	90404
27014	National Semicond Corp	Santa Clara Ca	95051
27777	Varo Semicond Inc	Garland Tx	75040
28480	Hewlett-Packard Hq	Palo Alto Ca	94304
30983	Mepco/Electra Corp	San Diego Ca	92121
32997	Bourns Trimpot Div	Riverside Ca	92507
34344	Motorola Inc	Franklin Park Il	60131
34649	Intel Corp	Mountain View Ca	95051
56289	Sprague Elect Co	North Adams Ma	01247
71590	Centralab Eleck Div	Milwaukee Wi	50501
72136	Electro Motive Corp	Willimantic Ct	06226
75042	TRW Inc	Philadelphia Pa	19108
75382	Kulka Elect Corp	Mt Vernon NY	10550
75915	Littlefuse Inc	Des Plaines Il	60016

SECTION VII

MANUAL CHANGES

7-1. INTRODUCTION.

7-2. There is no backdating information for the power supply as of the publication of this manual.

SECTION VIII

SERVICE

8-1. INTRODUCTION.

8-2. This section contains the theory-of-operation for the power supply. The first part discusses the block diagram functions while the second part elaborates on these functions by referring to detailed circuit schematics.

8-3. BLOCK DIAGRAM THEORY (Figure 8-1).

8-4. PRIMARY RECTIFIER and FILTER BOARD (A1). This board provides the supply with a rectified and conditioned "plus and minus" primary DC rail, along with transformation for control power. The rails are used as the source for the switching supplies. The A1 board provides protection to the supply from AC input surge current and overvoltage conditions. Furthermore, this board supplies the power for the forward mainframe fan and the internal cooling fan.

8-5. PRIMARY BOARD (A2). The -5.25, +5 and -3.25 volt supplies are generated on the Primary board along with some control and reference signals. LED failure indicators are installed for convenient troubleshooting references on the Primary board.

8-6. SECONDARY BOARD (A3). The secondary board is responsible for filtering, rectification and feedback for the DC power supplies. Furthermore, the secondary board provides the -5.25V, +5V, -3.25V, +12V and GND outputs to the Motherboard.

8-7. CONTROL BOARD (A4). LED failure indication and failure execution are the main functions of the control board. However, this board also creates LIR15, LINE SYNC, +40V, -12V, GSEN and +17V for the 64100A system.

8-8. THEORY OF OPERATION.

8-9. FILTER BOARD AND PRIMARY WIRING (Figure 8-7).

8-10. 110 VOLT OPERATION.

8-11. The primary side of T1 is stacked by S2 so there is effectively 220V across it. Outputs are in parallel. The varistors (RV1 and RV2) on the primary side of T1 are for transient suppression.

8-12. Because of the way that the neutral line is wired to the primary output rails of the bridge rectifier (CR1), only two of the diodes are being used. These are the two that connect the hot AC line to the + and - outputs. Configuratively, this produces ~315 VDC across the primary rails. Also notice that the neutral line does not have to be connected to the bridge diode for normal operation at 110V.

8-13. 220 VOLT OPERATION.

8-14. The windings on the primary side of T1 are wired in series by S2 so that there is still 220V across them.

8-15. During 220 VAC operation, all four diodes of the bridge rectifier are in use and the output across the primary is still ~315 VDC. In this mode both AC inputs to the bridge rectifier must be connected.

8-16. SAFETY CONSIDERATIONS.

8-17. R2/C4 and R3/C5 have a time constant of 2 min. The primary bus has ~315V across it, + or - 160VDC to ground. The main filter bank is a potential hazard to life, even with the supply off!

8-18. PRIMARY BOARD (Figure 8-7).

8-19. DESCRIPTION (See Figure 8-4 for timing waveforms).

8-20. The Primary board consists of the three pulse width modulators PWM (U5, U2, U4) and the switching circuitry for the primary side of the switching transformers. It also includes some control circuitry. As an overview, each modulator requires four signals for proper modulation. A reference voltage, a feed back voltage from the output to compare to the reference voltage for error detection, feedback current from the output for output current limiting, and a predetermined switching frequency. The PWMs control the switching transistors that alternate the current through the primary side of the switching transformers (T10-T15). Since all three PWMs are similar in operation, the +5V PWM will be explained.

8-21. OPERATION.

8-22. The PWMs modulate the output pulse width according to the demands of the system. In this manner they can control the amount of current each switcher can deliver and therefore they control the power. In reference to the +5V PWM, if the +5V feedback voltage going to pin 1, U5, is higher than the reference voltage going to pin 2, U5, the PWM determines that the output voltage is too high and reduces the pulse width to return it to within limits. If the +5CL (Current Limit voltage determined by the voltage drop across L4, a coil in the current return path of the +5V supply) becomes more positive than it should, more current flows into pin 15, U5. The PWM detects this condition and reduces the output pulse width for current limiting. The thermister (RT2) is to compensate for the thermal characteristics of the coil in the current return path of the +5V supply output. The potentiometer (R2) provides a means for adjusting the current limit.

8-23. The open collector outputs, U5 pins 8 and 11, are complimentary and nonoverlapping. For zero on-time (zero modulation time), both outputs are high. As demand increases, each output stays low (at different times, nonoverlapping) for longer and longer until one is going high as the other is going low or until one of the feedback signals limits the pulse duration. Each output is inverted through U6, another open-collector device, and alternately causes changing current through the primaries of T10 and T11. These transformers alternately turn Q6 and Q3 on and off which causes the current in the primary of T7 to alternate. The signals +5A and +5B are used to prevent or delay the switching of Q6 and Q3. For example, suppose the following condition exists. The power supply is experiencing a heavy demand and must allow close to 100% modulation to meet it. Q6 has turned on per the request of the PWM and has pulled the one node of T7 to the + primary rail voltage. Then the PWM tells Q6 to turn off and Q3 to turn on. Q3 can turn on immediately, but Q6 cannot turn off that quickly because of charge storage considerations. The +5B signal is a feedback signal from the secondary of T7 that senses this condition and and will not allow Q3 to turn on until Q6 turns off and the voltage on the secondary of T7 stabilizes. To allow Q3 to turn on sooner would have the effect of shorting the + primary rail to the - primary rail for a short period of time may damage other components.

8-24. Other signals that have to be present for the PWMs to operate are: U5 pin 3 (FEEDBACK control) must be allowed to float. It is pulled high by several error states to turn off the outputs. And U5 pin 4 (DEADTIME control) must be held low. It is forced high by several error states to turn off the outputs. The 20 KHz switching frequency of the PWMs is determined by a R/C time constant on pins 5 and 6 of U4. The 20 KHz clock is tied to all three PWMs to switch them syncronously.

8-25. PRIMARY PCB CONTROL CIRCUIT OPERATION.

8-26. As soon as the filter board is switched ON, CR20 rectifies the AC and starts charging C35, a ripple filter for the +12V regulator U13. The output of U13 lags the input by about 1V on power-up until it stabilizes at +12V. U13 is the power supply +12C (a control power supply used only in the power supply assembly). +12C supplies U1 which is the +5 REF source. Observe the sequence of events on power-up. As +12C first comes up (this happens very rapidly), C12 has not had time to develop a voltage drop across it and both sides are at 4.64V as determined by the zener diode CR27. The collector of Q1 also goes to pin 4 (DEADTIME control) of all three PWMs. As C12 charges through R32 and R13, the collector voltage of Q1 goes to 0v and allows the PWMs to gradually modulate to 100% or until limited by some other signal.

8-29. The SHUTDOWN signal (which can be generated in several places) enters this circuit between R13 and R32 and is used for the following purpose: Suppose there was a momentary power interruption that caused the power supply to start its shutdown procedure and then the power came back on. When SHUTDOWN was generated on powerfail, C12 was discharged immediately so that if power was quickly restored, DEADTIME would be high and would not allow the PWMs to attempt to draw a huge surge current to recover. Once again, as DEADTIME goes low (according to the time constant of C12 x [R32+R13]) the PWMs are allowed a greater and greater percent of modulation unless limited by some other signal.

8-30. U8 and U9 are overvoltage sensors. Both of them will turn ON an LED if an error condition is detected and both of them will generate SHUTDOWN. They work in the following manner: TH2 is a line that is normally grounded by a thermal switch on the Secondary board and travels through a jumper trace on the Control board to U8 on the Primary board. This is used to detect several errors; first, if the temperature of the heat sink on the secondary board exceeds 105 C then the thermal switch opens and an error is detected, second, if the control board is removed for service, an error is detected, third, if one of the boards is not plugged into the edge connector, an error is detected. If any of these three errors are detected by U8, it turns on the TH LED and sets SHUTDOWN high. U9 works in a similar fashion except that it detects its errors via T2. The primary side of T2 is in the return loop to the "Minus Primary Rail" for all three switchers. The change of current through the primary of T2 establishes a voltage drop in the secondary, rectified by CR19, divided by R43 and R71, and detected at pin 2, U9. If the voltage at pin 2, U9 is greater than ~+2.6V, (a slight delay is provided by C20), U9 latches and turns on the Primary Current Limit LED and sets SHUTDOWN high.

8-31. The rest of the control circuitry on the Primary board has to do with the -5.25 CL which is slightly different than the other two PWMs. One of the considerations of this supply is that when the -5.25 supply is down, the others are also disabled. This is done to protect the Dynamic RAMs. So when -5.25 CL exceeds the limits set for it, pin 1, U12 goes high. This generates SHUTDOWN and also forces the FEEDBACK control high on all three PWMs. Notice also that if SHUTDOWN is generated elsewhere, it forces the FEEDBACK control high on all three PWMs.

8-32. SAFETY CONSIDERATIONS.

The primary bus has ~315VDC across it and can supply 400 Watts of power. The main filter bank contains a lot of energy and is a potential hazard to life, even when the supply is off!

8-33. SECONDARY BOARD (Figure 8-10).

8-34. OPERATION.

8-35. The three switching supply secondaries are relatively simple. The +5V supply will be used for an example of this boards' operation.

8-36. The alternating voltage on the center tapped secondary of T7 is full wave rectified by two schottky diodes (CR8, CR9) mounted on a heat sink. The R5/C4 combination is a snubber network that limits the "dv/dt" to protect the diodes. +5A and +5B are taken from here to prevent both switching transistors from being on at the same time and shorting the + and - primary rails together. L3, C5, and C6 are the filter for the supply. The voltage drop across L4, in the return path, provides the signal +5CL for current limiting. The gate current for the SCR Q3 is called +5CB (crowbar) and is generated on the Control board.

8-37. Except for polarity and the lack of an SCR, the -3.25 supply is the same as the +5V supply.

8-38. Except for polarity considerations and the addition of Q1 and U1, the -5.25V supply is the same as the +5V supply.

8-39. Q1 and U1 combine to form an active minimum load for the -5.25V supply under the following conditions: Suppose that the -5.25V supply has an extremely light load on it. In this case the switcher for the -5.25V supply might have a very narrow duty cycle or indeed it might skip several cycles before it turns on again to supply the -5.25V. If this happens, because the -5.25V secondary also supplies the +12V,+17V, and +40V, these supplies can lose power and go out of regulation. The integrator, C7 and U1, detects that the switcher has been off for several cycles and causes Q1 to load the -5.25V supply causing the -5.25V switcher to increase its duty cycle. CR2/U2 is the rectifier/regulator for +12VDC. CR1 rectifies for the +17VDC supply and also for U1, a SHUTDOWN generator. There are also secondary windings for the +40VDC supply.

8-40. SAFETY CONSIDERATIONS

8-41. The secondary circuits can supply high current. The three heat-sinks for the secondaries could be very warm. Also, the primary sides of the switching transformers (T10-T15) are connected to the primary rails. These rails are a potential hazard to life even with the supply off!

8-42. CONTROL BOARD (Figure 8-10)

8-43. OPERATION.

8-44. U4, U5, and U7 are overvoltage protectors (OVP) that work in the following manner: when the voltage at pin 2 exceeds the voltage at pin 7 by +2.6V, the output pin 8 latches high to turn on the failure LEDs and, in the case of the +5 and -5.25 volt supplies, to supply current to crowbar the respective circuits. Also, whenever any one of the OVPs turn on, pin 6 goes low drawing current through R1, turning Q1 on and producing SHUTDOWN. The capacitors on pin 3 and pin 4 of the OVPs determine the minimum amount of time that the error has to exist before they turn on, a means of transient protection.

8-45. U1 and U2 combine to provide the signal Low Interrupt Request 15 (LIR15) to the I/O board. This signal goes low to signal the CPU that a powerfail has been detected. U2 and Q2 provide Low Power On Pulse (LPOP) to the mainframe. This signal goes low for a short time during power-on to initialize circuitry. U2 and Q3 provide Line Sync (LINE SYNC). This signal enables a square wave at the same frequency as the line. U1 and U2 are CMOS devices.

8-46. The signal THERMAL comes onto the power supply from the secondary board. There is a jumper trace installed in-line, and it leaves this board as TH2 to go to U8, OVP sensor, on the Primary board. In normal operation this line is at or near ground. If the thermal switch opens or the interconnect cable P2 is removed, SHUTDOWN will be generated on the Primary board and the TH LED will be ON.

8-47. U6 provides voltage ratio protection in case of a loss or reduction of the +12, +5 and -5.25 volt supplies. For example: if the sum of the voltage drops between R10, 11, 12 should change, resulting in a +2.6V increase of pin 2 over pin 7, then pin 8 would turn on the RATIO LED and in turn produce SHUTDOWN. This is important because a loss of one of the the ratio voltages would cause substrate damage to mainframe memory.

8-48. CR9 is the rectifier for the 40 VDC supply. Q4 is the regulator. Q5 and R29 form the high level current limiter that turns Q4 off if the current is too large. U3 is the overvoltage sensor that will turn Q4 off if the voltage formed by the voltage divider R36/37 goes too high. U3 and C13 form an integrator that limits the average current through Q4.

8-49. SAFETY AND HANDLING CONSIDERATIONS.

8-50. The power supply boards contain CMOS devices. C11 in the 40v supply will remain charged after the supply is shut off!

8-51. MNEMONICS.

Table 8-1. Mnemonics

Mnemonics		Description
CB	Crowbar	Used by the -5.25V and the +5V supplies. When crowbar goes high, the corresponding SCR conducts, and effectively puts a short across the supply, causing the supplies to shutdown.
CL	Current Limit	Used by the +5V,-5.25V and -3.25V supplies. Current limit is used by the supply as feedback to the PWMs to determine if the maximum current of the individual supply is being exceeded. The current limit of each switching supply is adjustable.
GSEN	Ground Sense	GSEN is used by the supply to determine the voltage drop of the high current carrying control ground, due to the parasitic resistance of the Motherboard. Then, this voltage drop is used to adjust the +5V REF regulator.
LINE SYNC	Line Sync	LINE SYNC is processed from the line input and used for timing throughout the mainframe.
LIR15	Low Interrupt Request 15	This signal is used as a power fail indicator which is sent to the I/O board.
LPOP	Low Power On Pulse	LPOP is generated shortly after the power is turned on. This signal initializes several ICs throughout the mainframe.
OV	Over Volt	Used by the +5V,-5.25V and -3.25V supplies. If any of the above supplies should increase enough to bring about a +2.6V difference between pin 2 and 7 of U4, U5, or U7 on the Control board then SHUTDOWN will be generated and the supplies will turn off.
PCL	Primary Current Limit	PCL detects an unlinear surge of current internal to the supply. If a surge is encountered then a shutdown is initiated.

Table 8-1. Mnemonics (Cont'd)

PON	Power On	PON is generated on a power up of the system. This signal is used for initializing the LIR15 circuitry.
RATIO		The ratio signal is used in detecting loss or reduction in the +12V,-5.25V and +5V supplies and generating SHUTDOWN.
SHUTDOWN		SHUTDOWN is generated in several places and is responsible for turning off the PWMs by pulling U2, U4, U5 pin 3 high.
SYNC	Sychronize	AC line frequency and sync are the same.
TH	Thermal	Thermal, TH and TH2 all relate to the thermal switch located on the secondary board. The switch will open when the internal temperature of the supply is greater than 105 degrees C. Also, the TH LED will be indicating a problem.
+5 REF	+5V Reference	This signal is used throughout the supply and provides a stable reference voltage for the PWMs.
+12C	+12V Control	+12C is the control signal used throughout the supply. If +12C is not up the supply will not operate.

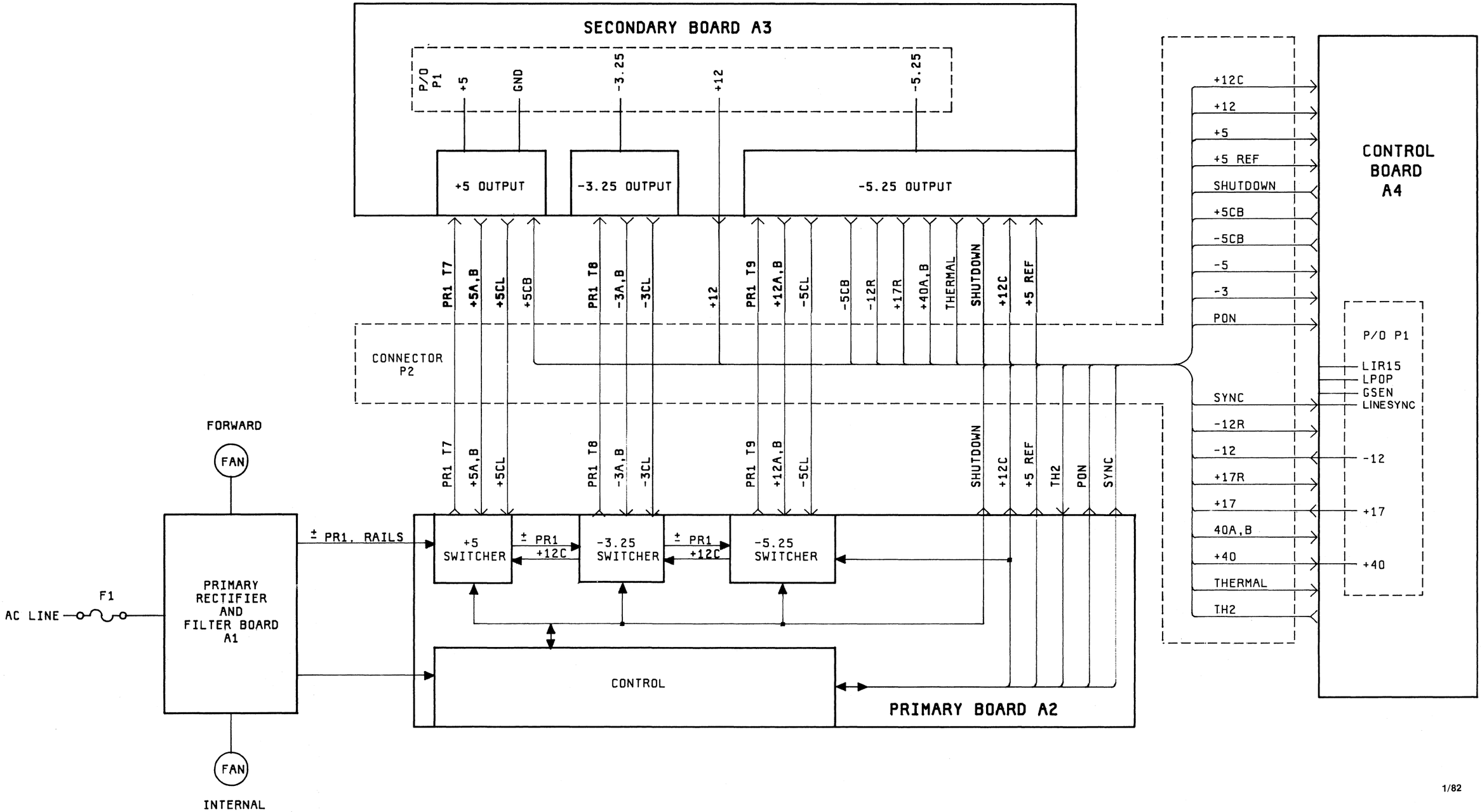


Figure 8-1.
Power Supply Block Diagram
PS 8-9

Table 8-2. P2 Board Connections

Pin Label	P2 Pin No.	A2 Primary Bd	A3 Secondary Bd	A4 Control Bd
———	1			
+12C	2	X	X	X
SENSE GND	3	X	X	X
-12R	4		X	X
———	5			
+17R	6		X	X
———	7			
+17R	8		X	X
+5REF	9	X	X	X
+17R	10		X	X
-5CB	11		X	X
-3CL	12	X	X	
-3A	13	X	X	
+12	14	X	X	X
RETURN GND	15		X	X
-3B	16	X	X	X
RETURN GND	17		X	X
-5CL	18	X	X	
RETURN GND	19		X	X
-12	20	X		X
SHUTDOWN	21	X	X	X
TH2	22	X		X
+5CB	23		X	X
THERMAL	24		X	
+5	25	X	X	X
+12B	26	X	X	
CUR.SEN.GND	27	X	X	
+12A	28	X	X	
-3	29	X	X	X
———	30			
-5.2	31	X	X	X
40B	32		X	X
CONTROL GND	33	X	X	X
40A	34		X	X
PON	35	X		X
+5B	36	X	X	
SYNC	37	X		X
+5A	38	X	X	
———	39			
+5CL	40	X	X	

NOTE: An X on a given Pin Number denotes a line connection.

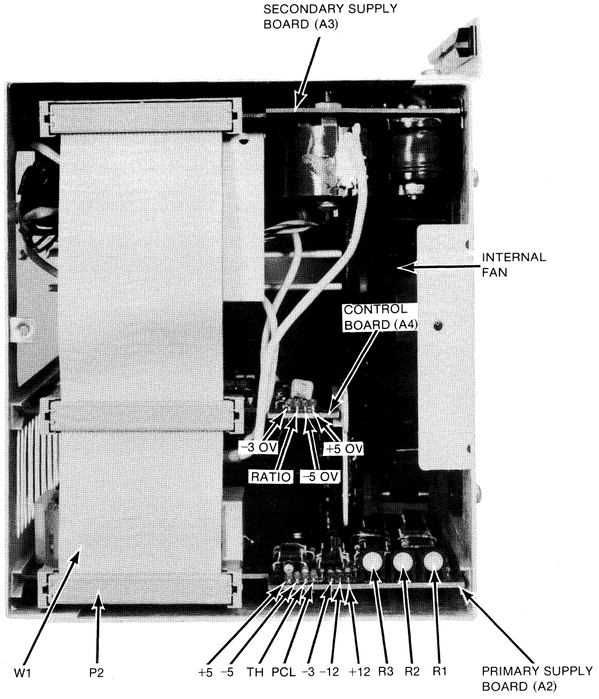


Figure 8-2. Board Placement and Partial Component Locator

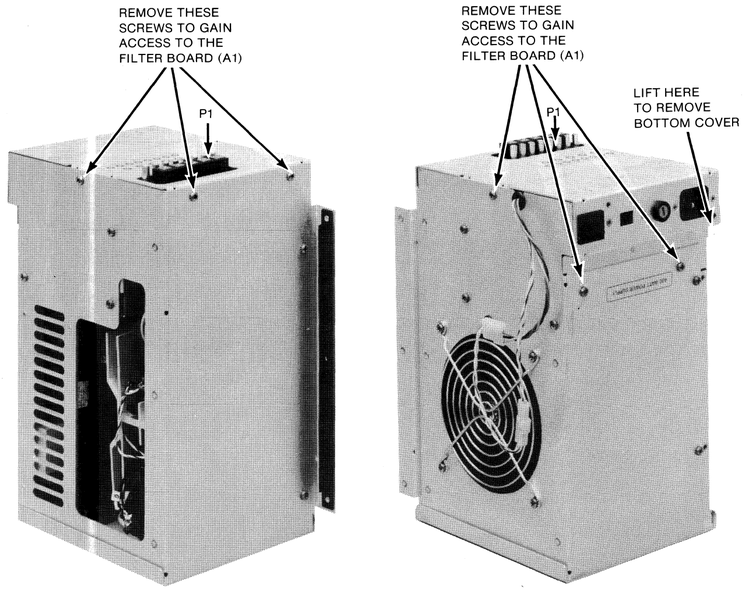
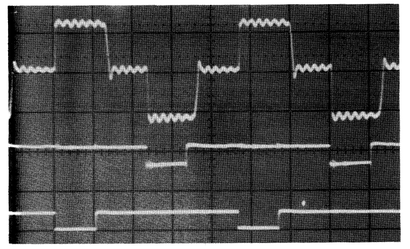


Figure 8-3. Primary Filter Board Removal

NOTE

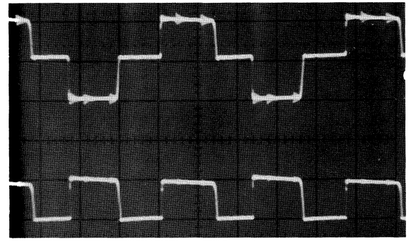
The waveforms below relate to the +5V switching supply. The numbered stars below represent the signals seen at the location of the numbered stars on the schematics (Figures 8-7 and 8-10). Note that the same signals can be seen on the corresponding parts on the -5.25V and -3.25V supplies.



① Top waveform - The primary of T7 with the +5V supply loaded; this signal 320V p-p.

② Middle waveform - The signal shown is the output of U5 pin 8 at 12V p-p.

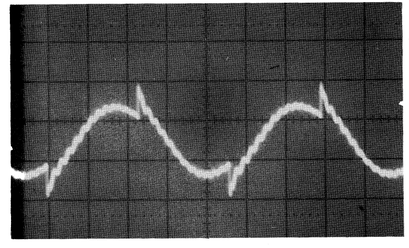
③ Bottom waveform - This signal is the other output of U5 pin 11 at 12V p-p.



④ Top waveform - The signal on the the left is the anode of CR8.

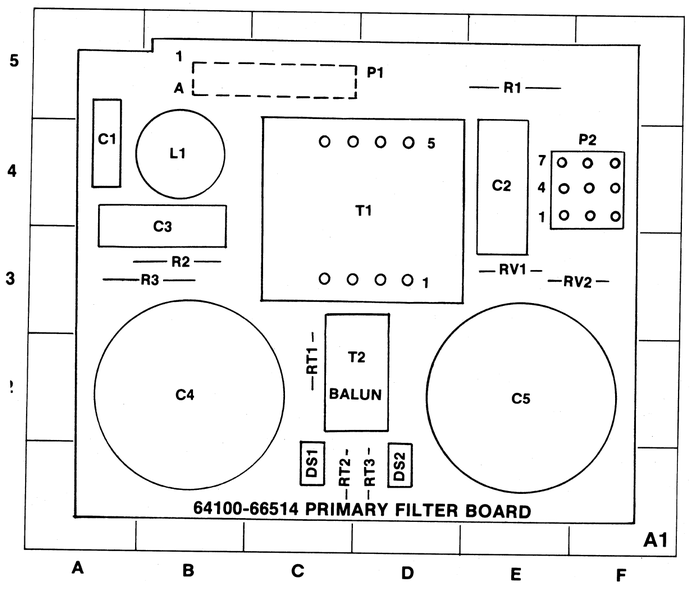
Note: These signals are with the +5V supply loaded.

④ Bottom waveform - This signal is on the cathode of CR8.



① This waveform is the primary of T7 with the +5V supply unloaded.

Figure 8-4.
Timing Waveforms



REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C-1	A-4	R1	E-5	RT3	D-1
C2	E-4	R2	B-3	T1	D-4
C3	B-3	R3	B-3	T2	D-2
C4	B-2	RV1	E-3	P1	D-5
C5	E-2	RV2	F-3	P2	F-4
DS1	C-1	RT1	L-2		
DS2	D-1	RT2	C-1		

Figure 8-5. Primary Filter Board Component Locator

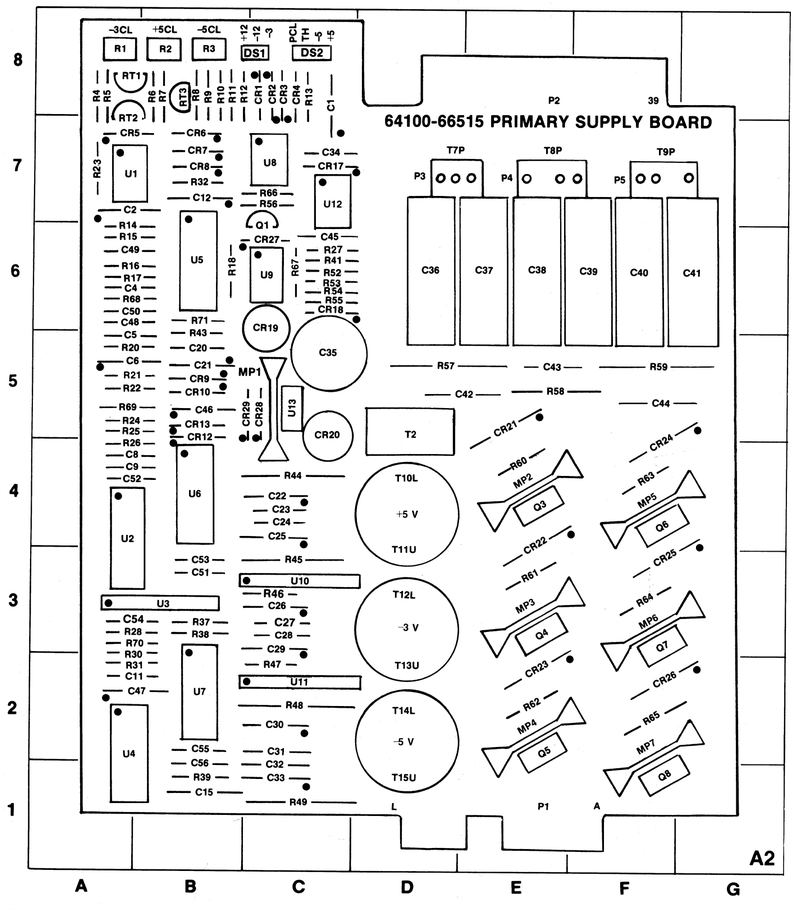


Figure 8-6. Primary Supply Board Component Locator

REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	C-8	C30	C-2	C50	A-6	CR18	B-6	MP7	F-2	R8	B-8	R30	A-2	R59	F-5	T13U	D-2
C2	A-7	C31	C-2	C51	B-3	CR19	C-6	P1	E-1	R9	B-8	R31	A-2	R60	E-4	T14L	D-2
C4	A-6	C32	C-1	C52	A-4	CR20	C-5	P2	E-8	R10	B-8	R32	B-7	R61	E-3	T15U	D-1
C5	A-5	C33	C-1	C53	B-3	CR21	E-5	P3	D-7	R11	B-8	R37	B-3	R62	E-2	U1	A-7
C6	A-5	C34	C-7	C54	B-3	CR22	E-4	P4	E-7	R12	B-8	R38	B-3	R63	F-4	U2	C-7
C8	A-4	C35	C-5	C55	B-2	CR23	E-2	P5	F-7	R13	C-8	R39	B-1	R64	F-3	U3	B-3
C9	A-4	C36	D-6	C56	B-1	CR24	F-4	Q1	C-6	R14	A-6	R41	C-6	R65	F-2	U4	A-2
C11	A-2	C37	E-6	CR1	C-8	CR25	F-3	Q3	E-4	R15	A-6	R43	B-5	R66	C-7	U5	B-6
C12	B-7	C38	E-6	CR2	C-8	CR26	F-2	Q4	E-3	R16	A-6	R44	C-4	R67	C-6	U6	B-4
C15	B-1	C39	F-6	CR3	C-8	CR27	C-6	Q5	E-2	R17	A-6	R45	C-3	R68	A-6	U7	B-2
C20	B-5	C40	F-6	CR4	C-8	CR28	C-5	Q6	F-4	R18	B-6	R46	C-3	R69	A-5	U8	C-7
C21	B-5	C41	G-6	CR5	A-7	CR29	C-5	Q7	F-3	R20	A-5	R47	C-2	R70	A-3	U9	C-6
C22	C-4	C42	E-5	CR6	B-7	DS1	C-8	Q8	F-1	R21	A-5	R48	C-2	R71	B-6	U10	C-3
C23	C-4	C43	E-5	CR7	B-7	DS2	C-8	R1	A-8	R22	A-5	R49	C-1	RT1	A-8	U11	C-2
C24	C-4	C44	F-5	CR8	B-7	MP1	L-5	R2	B-8	R23	A-7	R52	C-6	RT2	A-7	U12	A-4
C25	C-4	C45	C-6	CR9	B-5	MP2	E-4	R3	B-8	R24	A-5	R53	C-6	RT3	B-8	U13	C-5
C26	C-3	C46	B-5	CR10	B-5	MP3	E-3	R4	A-8	R25	A-5	R54	C-6	T2	D-5		
C27	C-3	C47	B-2	CR12	B-5	MP4	E-2	R5	A-8	R26	A-4	R55	C-6	T10L	D-4		
C28	C-3	C48	A-6	CR13	B-5	MP5	F-4	R6	B-8	R27	C-6	R56	C-7	T11U	D-4		
C29	C-3	C49	A-6	CR17	C-7	MP6	F-3	R7	B-8	R28	A-3	R57	D-5	T12L	D-3		
												R58	E-5				

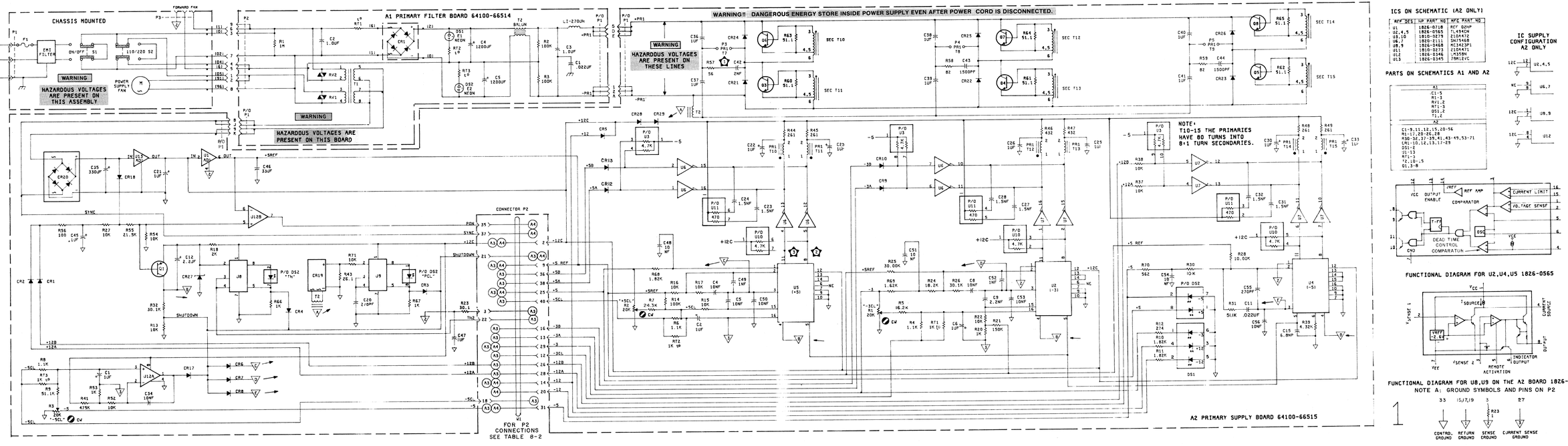
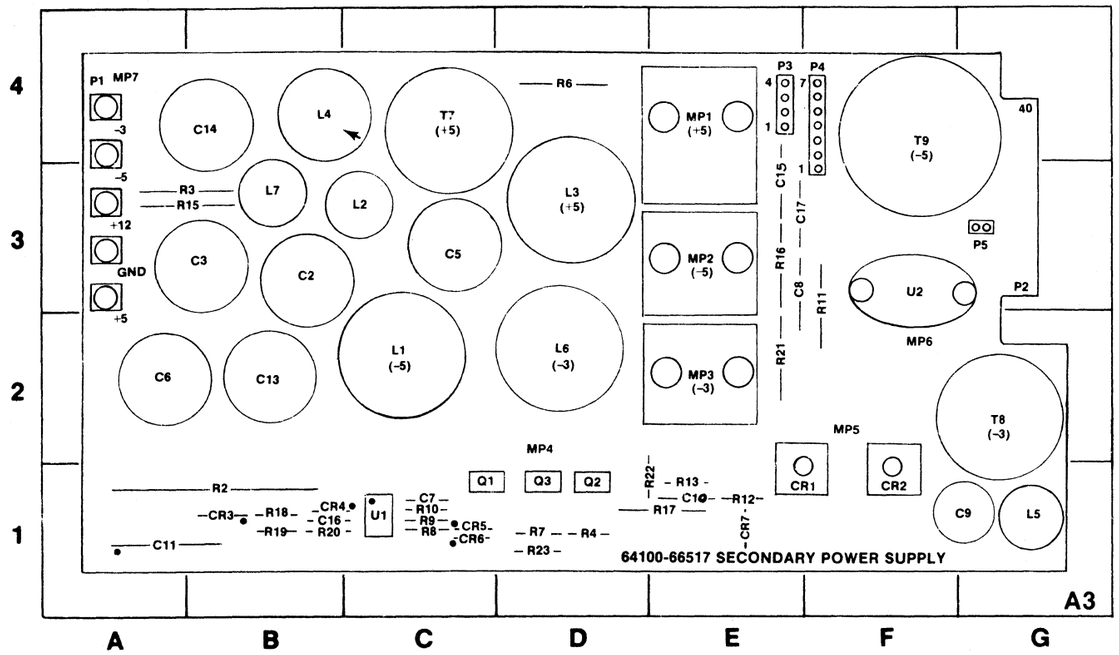


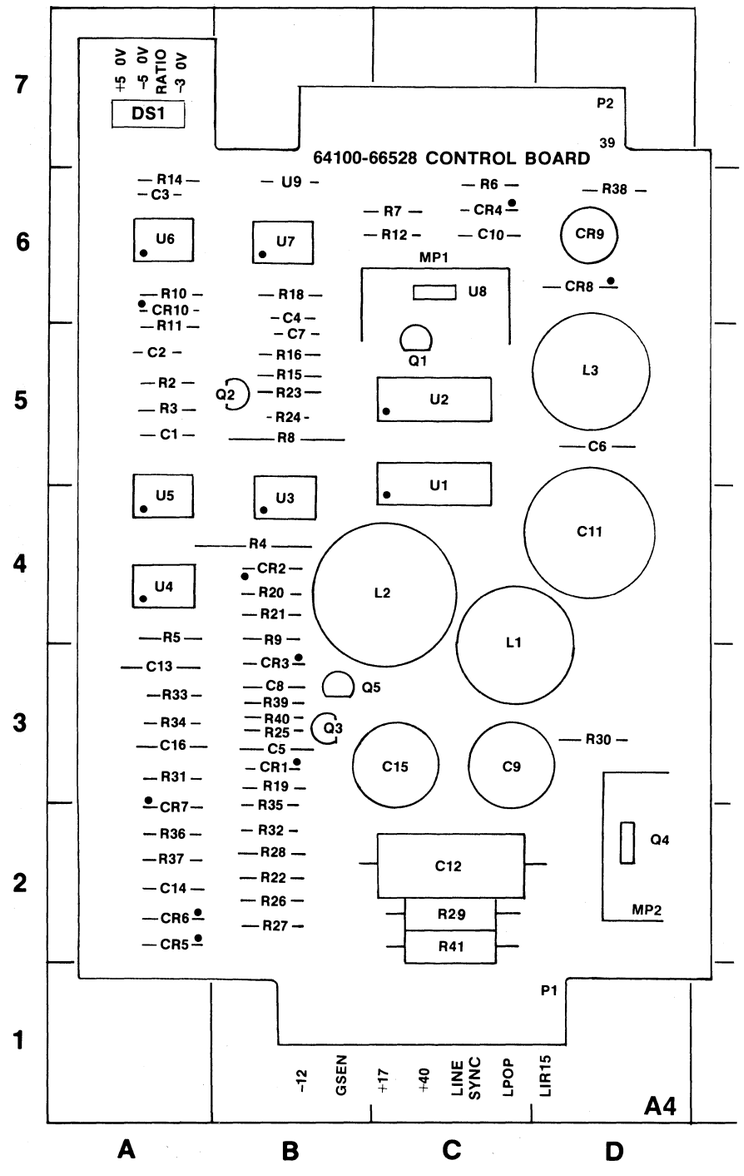
Figure 8-7.
Primary Filter (A1) and Primary Supply (A2) Board Schematics
PS 8-13



REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	E-3 †	C11	A-1	CR4	B-1	L2	C-3	MP5	F-2	Q3	D-1	R10	C-1	R20	B-1
C2	B-3	C12	E-2††	CR5	C-1	L3	D-3	MP6	F-2	R1	E-3 †	R11	F-3	R21	E-2
C3	B-3	C13	B-2	CR6	C-1	L4	B-4	MP7	A-4	R2	B-1	R12	E-1	R22	D-1
C4	E-4 *	C14	B-4	CR7	E-1	L5	G-1	P1	A-4	R3	A-3	R13	E-1	R23	D-1
C5	C-3	C15	E-3	CR8	E-4 *	L6	D-2	P2	G-3	R4	D-1	R14	E-2††	S1	E-4 *
C6	A-2	C16	B-1	CR9	E-4 *	L7	B-3	P3	E-4	R5	E-4 *	R15	A-3	T7	C-4
C7	C-1	C17	E-3	CR10	E-2††	MP1	E-4 *	P4	F-4	R6	D-4	R16	E-3	T8	G-2
C8	E-3	CR1	F-1	CR11	E-2††	MP2	E-3 †	P5	G-3	R7	D-1	R17	E-1	T9	F-4
C9	G-1	CR2	F-1	CR12	E-3 †	MP3	E-2††	Q1	C-1	R8	C-1	R18	B-1	U1	C-1
C10	E-1	CR3	B-1	CR13	E-3 †	MP4	D-2	Q2	D-1	R9	C-1	R19	B-1	U2	F-3
				L1	C-2										

*These parts mounted on assembly MP1
†These parts mounted on assembly
††These parts mounted on assembly MP3

Figure 8-8. Secondary Board Component Locator



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C3	A-6	R7	C-6
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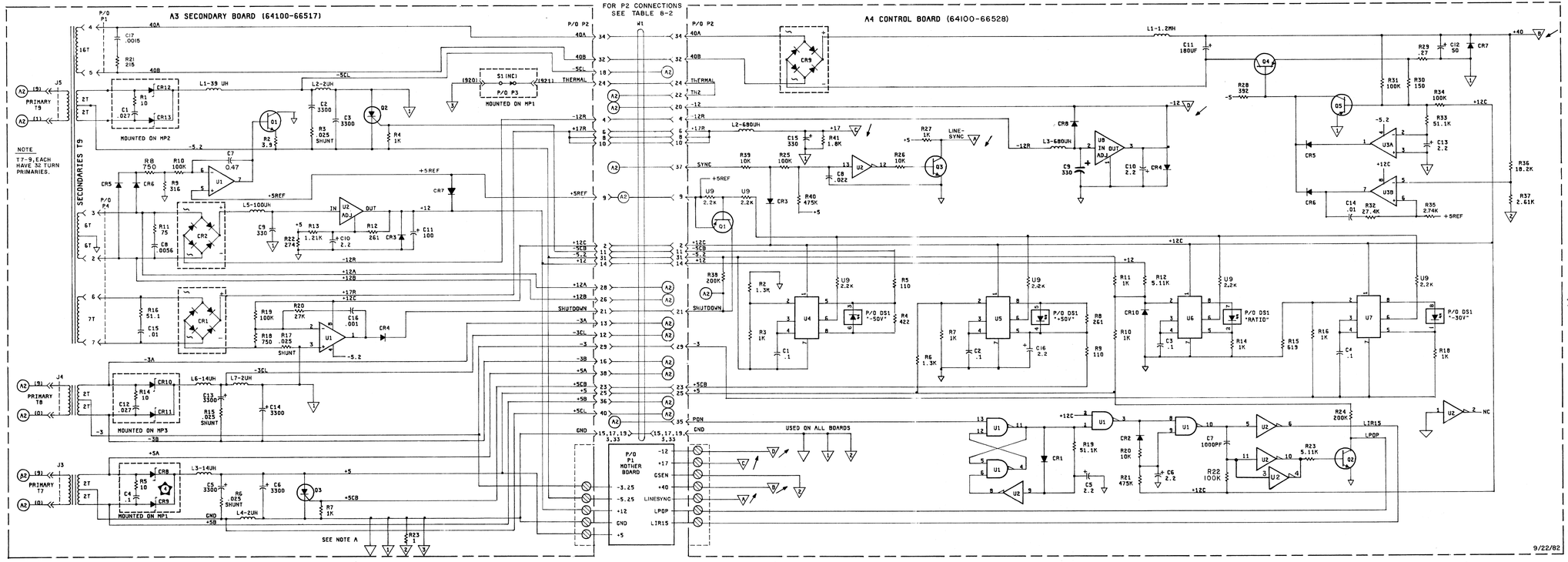
C5	B-3	R9	B-4
C6	D-5	R10	A-6
C7	B-5	R11	A-5
C8	B-3	R12	C-6
C9	C-3		
C10	C-6	R14	A-6
C11	D-4	R15	B-5
C12	C-2	R16	B-5
C13	A-3	R18	B-6
C14	A-2	R19	B-3
C15	C-3	R20	B-4
C16	A-3	R21	B-4
CR1	B-3	R22	B-2
CR2	B-4	R23	B-5
CR3	B-3	R24	B-5
CR4	C-6	R25	B-3
CR5	A-2	R26	B-2
CR6	A-2	R27	B-2
CR7	A-2	R28	B-2
CR8	D-6	R29	C-2
CR9	D-6	R30	D-3
CR10	A-6	R31	A-3
DS1	A-7	R32	B-2
L1	C-4	R33	A-3
L2	C-4	R34	A-3
L3	D-5	R35	B-2
MP1	C-6	R36	A-2
MP2	D-2	R37	A-2
P1	D-1	R38	D-6
P2	D-7	R39	B-3
Q1	C-5	R40	B-3
Q2	B-5	R41	C-2
Q3	B-3	U1	C-4
Q4	D-2	U2	C-5
Q5	B-3	U3	B-4
		U4	A-4
R2	A-5	U5	A-4
R3	A-5	U6	A-6
R4	B-4	U7	B-6
		U8	C-6
		U9	B-6

Figure 8-9. Control Board Component Locator



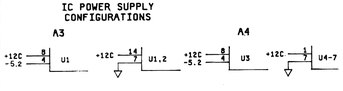
ICS ON THIS SCHEMATIC (A3,A4)

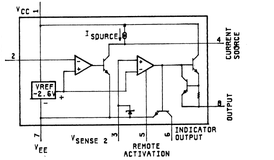
REF. DES.	HP PART NO.	MFG. PART NO.
	A3	
U1	1826-0346	LM358
U2	1826-0677	LM338
	A4	
U1	1820-1577	CD4093BF
U2	1820-2019	MC1458BCP
U3	1826-0346	LM358
U4-7	1826-0680	3423A
U8	1826-0221	UA7912

PARTS ON THIS SCHEMATIC (A3,A4)

A3
C1-17 CR1-6,8-13 L1-2 Q1-3 R1-23 S1 T7-9 U1,2
A4
C1-16 CR1-10 DS1 L1-3 Q1-5 R1-16,18-41 U1-8

IC POWER SUPPLY CONFIGURATIONS





FUNCTIONAL DIAGRAM FOR U4-7 ON THE A4 BOARD 1826-0680

NOTE A: GROUND SYMBOLS AND PINS ON P2

33 CONTROL GROUND; 15,17,19 RETURN GROUND; 3 SENSE GROUND (R23 1); 27 CURRENT SENSE GROUND

NOTE B: ALL CAPS IN μF UNLESS SPECIFIED DIFFERENTLY

Figure 8-10.
Secondary (A3) and Control (A4) Board Schematics

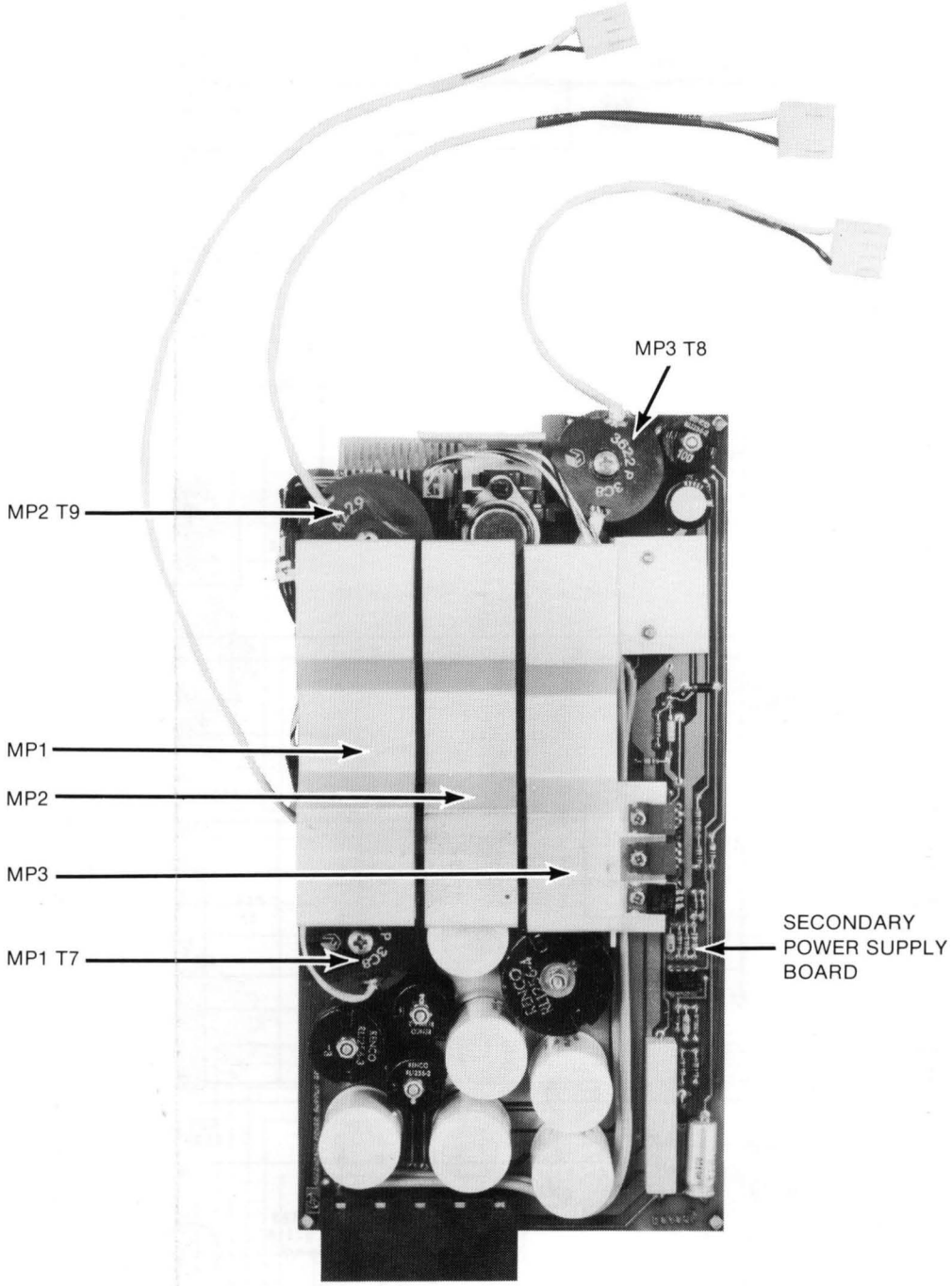
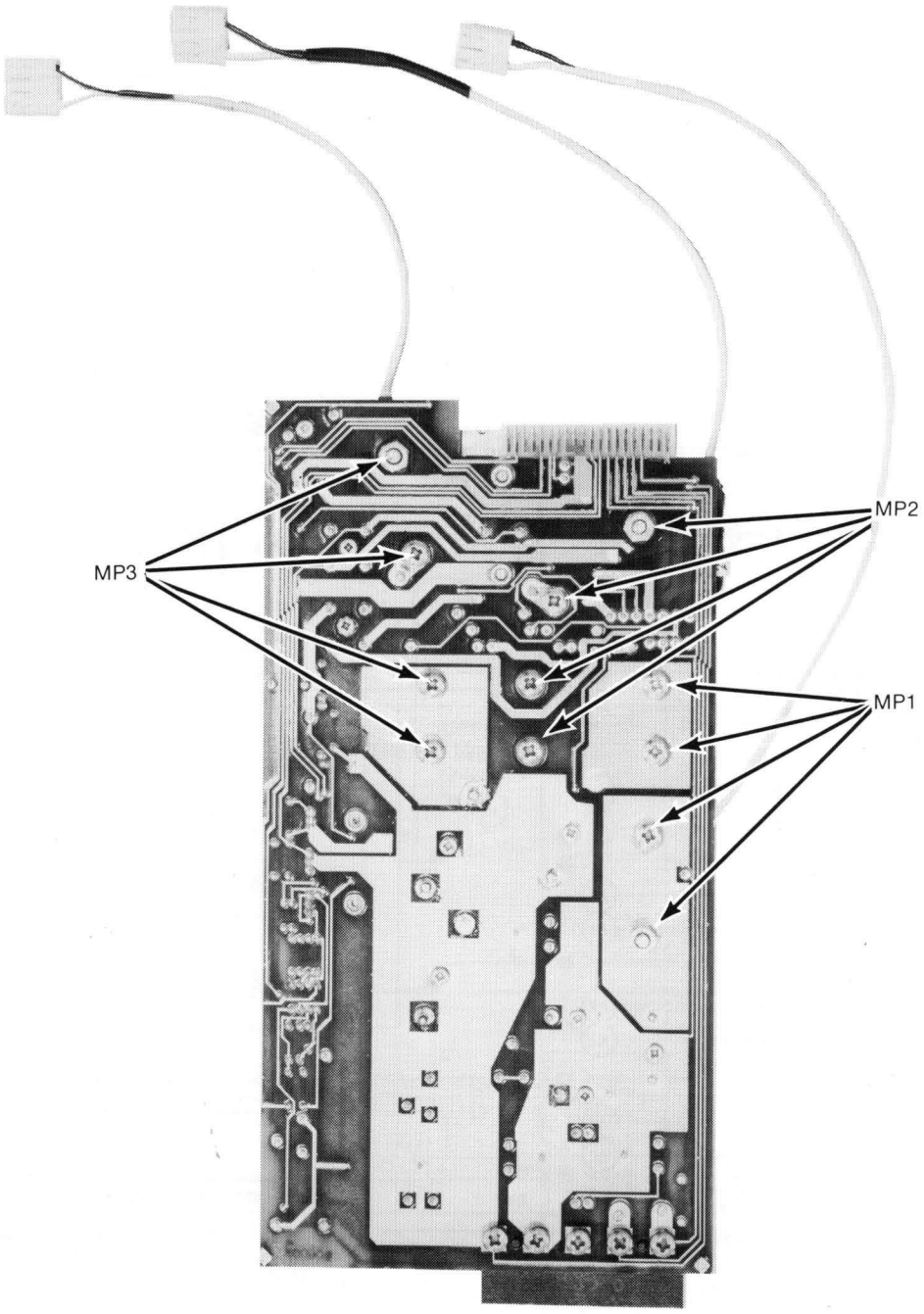
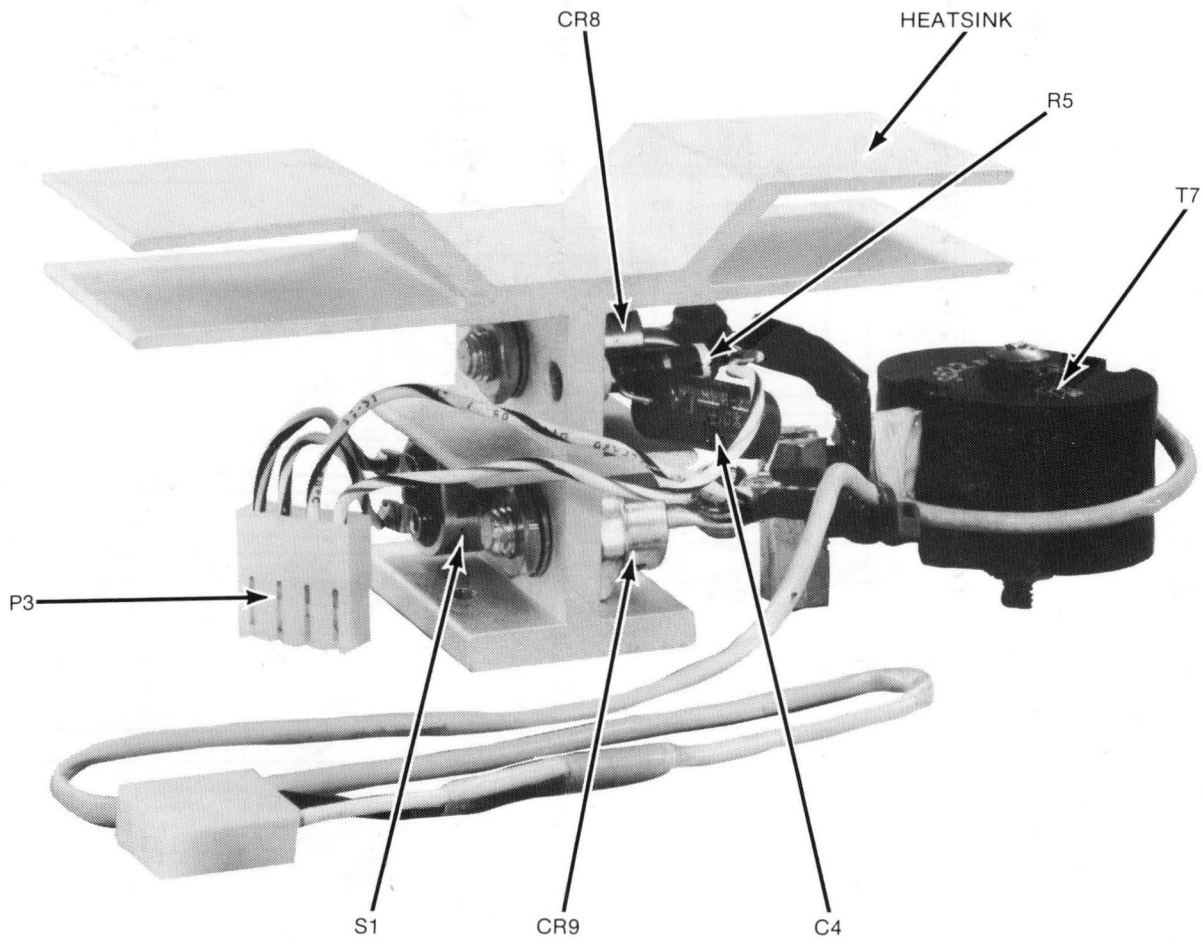


Figure 8-11. Locations of MP1, MP2, and MP3 heatsink assemblies



Note: Remove the screws and/or nut and lockwasher that go with the faulty MP assembly. Also, the faulty assembly must be ordered as a complete assembly. Each assembly P/N is given in section VI, table 6-2.

Figure 8-12. MP1, MP2, and MP3 Heatsink Assembly Removal



Note: The MP1 and MP3 assemblies are nearly identical in component locations.

Figure 8-13. Separate MP1 Assembly