HEWLETT PACKARD

TITLE: 16K MEMORY EXPANSION MODULE
SERVICE MANUAL

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LIST OF ILLUSTRATIONS

LIST OF TABLES

SECTION I

GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. This service manual contains information required to install, test and service the Hewlett-Packard Model 64032A 16k Memory Expansion Module.

1-3. Shown on the title page is a microfiche part number. This number can be used to order 4 x 6 inch microfilm transparencies of the manual. Each microfiche contains up to 96 photoduplicates of the manual pages.

1-4. INSTRUMENTS COVERED BY THIS MANUAL.

1-5. Attached to the instrument or printed on the printed circuit board is the repair number. The repair number is in the form: 0000A00000. It is in two parts; the first four digits and the letter are the repair prefix, and the last five are the suffix. The prefix is the same for all identical instruments. The suffix, however, is assigned sequentially and is different for each instrument. The contents of this manual apply to instruments with the repair number prefix(es) listed under REPAIR NUMBERS on the title page.

1-6. An instrument manufactured after the printing of this manual may have a repair number prefix that is not listed on the title page. This unlisted repair number prefix indicates that the instrument is different from those described in this manual. The manual for this newer instrument is accompanied by a Manual Changes supplement. This supplement contains "change information" that explains how to adapt the manual for the newer instrument.

1-7. In addition to change information, the supplement contains information for correcting errors in the manual. To keep this manual as current as possible, Hewlett-Packard recommends that you periodically request the latest Manual Changes supplement. The supplement for this manual is identified with the manual print date and part number, both appear on the manual title page. Complimentary copies of the supplement are available from Hewlett-Packard Sales/Service Office.

1-8. For information concerning a repair number prefix that is not listed on the title page or in the Manual Changes supplement, contact your nearest Hewlett-Packard Sales/Service office.

1-9. DESCRIPTION.

1-10. The Hewlett-Packard Model 64032A 16k Memory Expansion Module provides additional memory for the HP 64000 software. Memory is contained on one printed circuit board that fits in the 64000 mainframe card cage (figure 1-1).

1-11. Memory capacity of 16k, 16 bit words is achieved through the use of 16 dynamically refreshed RAMs. Each word is stored in memory in the form of an upper and lower byte, with each bit located in an individual RAM chip. Refer to Section VIII Service for a more detailed description.

1-12. SPECIFICATIONS.

    a.   Memory expansion of 16k, 16 bit words.

    b.   Board ID 0401H.

    c.   Typical power consumption, in watts.
             1.9 at +5 V, .1 at −5 V, .5 at +12 V.

1-13. LEVEL OF SERVICE.

1-14.   This is a Final Component Level Manual. It contains information that provides component level servicing of the Model 64032A. Detailed schematics, theory of operation and Signature Analysis loops are provided in sections IV and VIII.
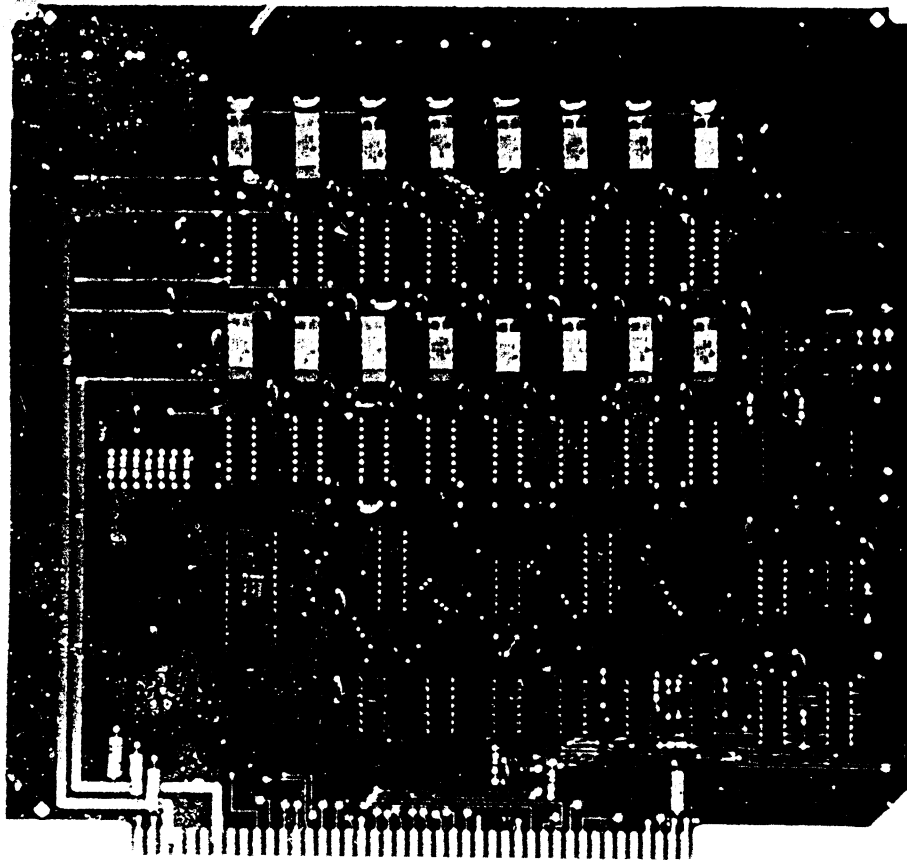
Figure 1-1. Model 64032A 16k Memory Expansion Module

SECTION II

INSTALLATION

2-1. INTRODUCTION.

2-2. This section contains information for installing and removing the Model 64032A. Also included are initial inspection procedures.

2-3. INITIAL INSPECTION.

2-4. Inspect the shipping container for damage. If the shipping container or cushioning material is damaged, it should be kept until contents of the shipment have been checked for completeness and the instrument has been checked mechanically and electrically. Procedures for checking electrical performance are given in section IV. If the contents are incomplete, if there is mechanical damage or defect, or if the instrument does not pass the performance tests, notify the nearest Hewlett-Packard Sales/Service office. If the shipping container is damaged, or if the cushioning material shows signs of stress, notify the carrier as well as the Hewlett-Packard Sales/Service office. Keep the shipping materials for the carrier's inspection. The HP office will arrange for repair or replacement at HP option without waiting for claim settlement.

> **CAUTION**
>
> The Model 64032A 16k Memory Expansion Module must be installed and removed with the mainframe power off!

2-5. INSTALLATION.

  a. Remove the access cover from the mainframe.

  b. Orient the module so that the 86 pin edge connector is pointed toward the bottom of the card cage, and the component side is facing the CPU board. Insert the module into any numbered slot and press down firmly until it is seated.

  c. Replace the access cover.

2-6. REMOVAL.

  a. Remove the access cover from the mainframe.

  b. Locate the module; its extraction tabs are labeled M16KDYN and 64032A. Remove the module by lifting up the extraction tabs.

  c. Replace the access cover.

SECTION III

OPERATION

The operation of the 16k Memory Expansion Module is a function of the HP 64000 software and is beyond the scope of this service manual. All operating features of the module are transparent to the user of the software.

SECTION IV

PERFORMANCE TESTS

4-1. INTRODUCTION.

4-2. This section explains servicing of the 16k Memory Expansion Module. The paragraphs on Performance Verification (PV) describe what the PV is, how it is run, what it does, and how to decode PV errors. The troubleshooting paragraphs explain how the PV tests are used to identify failures. Using this section, the schematic in section VIII, and Signature Analysis it is possible to service the module to the individual component level.

4-3. REQUIRED EQUIPMENT.

a. A 64000 series mainframe with most recent PV software.

b. To print PV results a printer must be attached to the system.

c. To perform PV generated signature analysis, an HP Model 5004A or equivalent signature analyzer is required.

4-4. SYSTEM CONSIDERATIONS.

4-5. Failure isolation must be performed to eliminate other sections of the Logic Development System as the source of the failure. It is assumed in this manual that the mainframe PV has been successfully conducted and that other option cards have been removed from the card cage.

4-6. PERFORMANCE VERIFICATION TESTS.

4-7. The Performance Verification for the 16k Memory Expansion Module is a software routine used by the mainframe to test about 99% of the circuitry of the memory module. It is a subsection of the system Option Test Performance Verification that allows testing of each module located in the mainframe card cage. The following paragraphs describe how to perform the 16k Memory Expansion Module PV, what is checked, and how to decode the errors.

4-8. STARTING PERFORMANCE VERIFICATION.

4-9. To test the memory proceed as follows.

a. With the operating system initialized and awaiting a command (figure 4-1), enter the **option_test** command.

option_test RETURN

STATUS: Awaiting command   userid   14:10

option test

   edit   compile assemble   link   emulate prom prog SIMDE1012   etc.
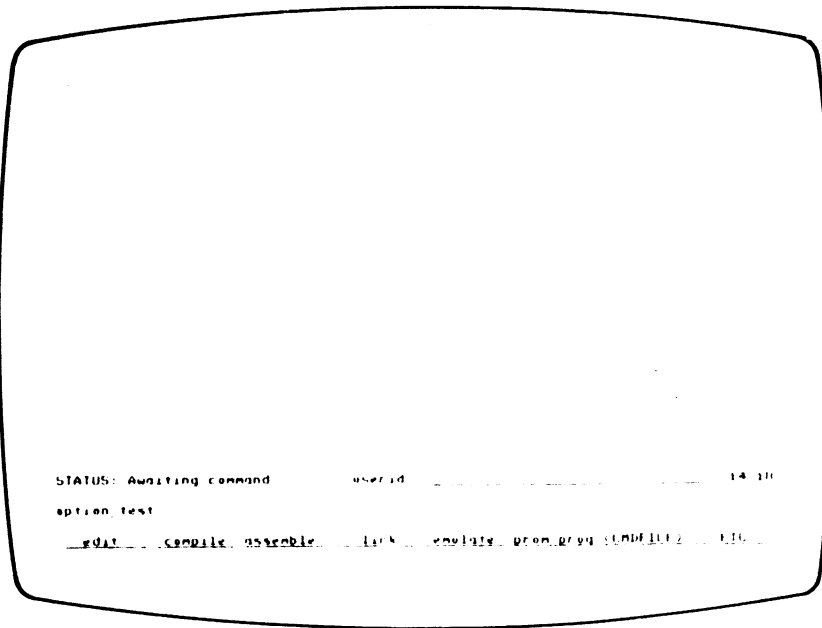
Figure 4-1. System Awaiting Command Display

HP 64000 Option Performance Verification

Card # ID # Module

1   0401H 16K Memory Expander

STATUS: Awaiting test selection   14:10

   end   (SLOT#)   print
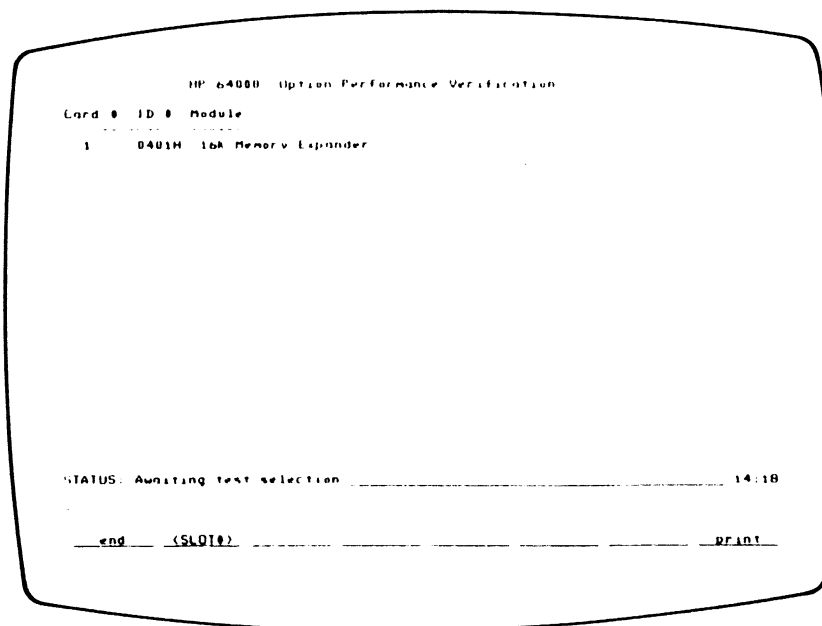
Figure 4-2. Card Cage Directory Display

b. The PV now displays a directory of the installed option boards and their card slot numbers (figure 4-2). The first step in the PV is to locate the card slot of the 16k Memory Expansion Module and enter the slot number. For example, if the memory is in slot 1, enter:

<div align="center">1   RETURN</div>

4-10. PERFORMANCE VERIFICATION COMMANDS.

4-11. Each PV display provides prompting for the commands that can be executed. These commands are selected by "softkeys" which are defined below.

cycle   starts highlighted test and continues through other tests until the **end**, **next_test**, or **start** softkey is pressed.

end   terminates test activity and returns display to next higher level. At Total PV Display (figure 4-3) also resets failure counters to zero.

next_test   moves highlight line to following test category.

print   outputs display to attached printer.

start   begins execution of selected test.

4-12. TOTAL PV TESTS.

4-13. **Display.** All test categories available are shown in this display. When one or more test categories have been executed the results are displayed. Use the display to choose the test categories to be performed or to review the overall results of the PV.
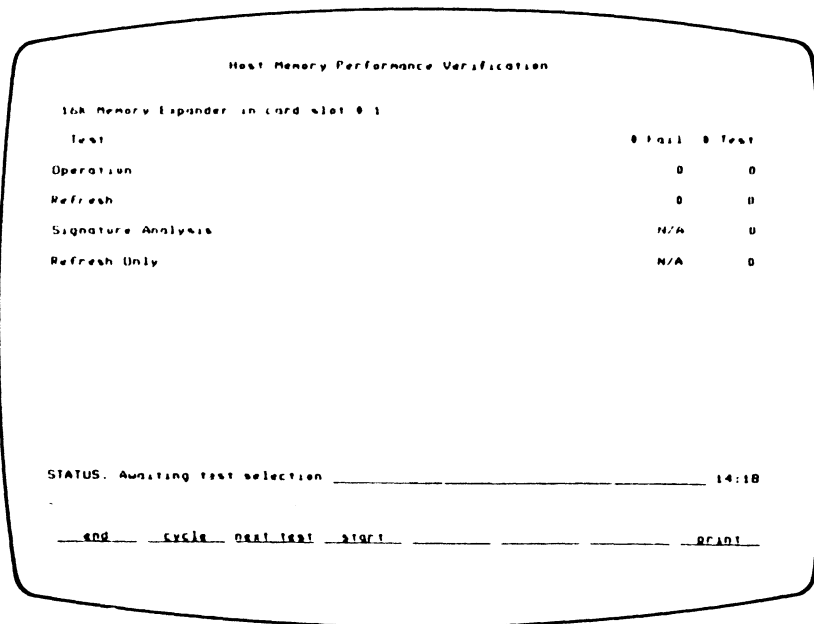
Figure 4-3. Total PV Display

4-14. Running the Total PV. To run all the tests shown on the display, press the **cycle** softkey. Each test category is executed and the results are displayed. A complete cycle requires approximately fifteen seconds. Press the **next_text** softkey to halt the iterations.

4-15. Using the Total PV Results. When the tests are complete, examine the # Fail column. When all entries are zero it indicates approximately 99% of the circuitry has been checked and no errors have been found.

4-16. A non-zero value represents the number of errors detected in the test category. Determine the exact cause of the error by running the failed test category and viewing the results in detail. Do this by positioning the highlight line over the failed test category and pressing the **start** softkey.

4-17. OPERATION TEST.

4-18. Display. This display shows the four Operation test categories and the test results. Use the display to view test conditions in detail.
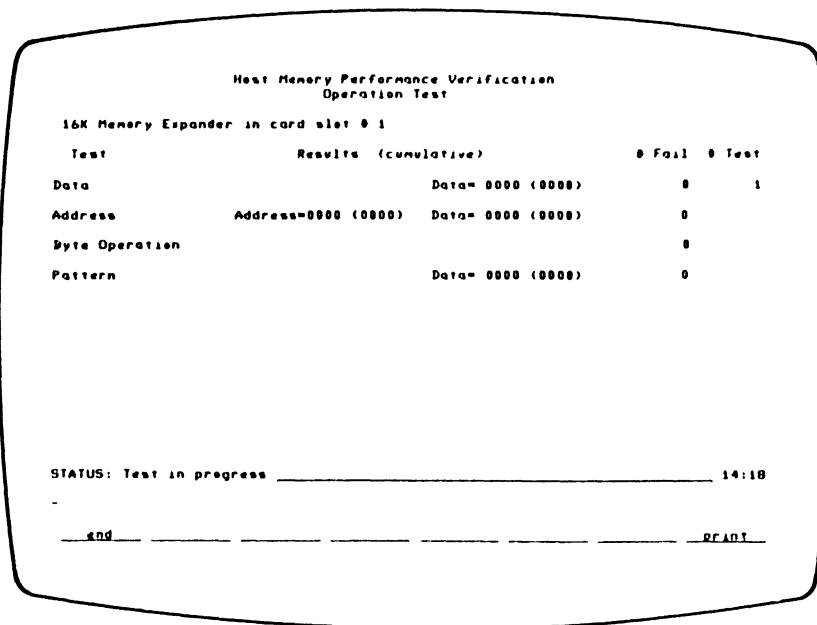
Figure 4-4. Operation Test Display

4-19. Running the Operation Tests. The Operation tests are always running while this screen is displayed. To stop the tests and return to the Total PV Display, press the **end** softkey. Each iteration of the tests takes less than one second.

4-20. Using the Operation Test Results. The total number of errors detected during the tests is shown in the # Fail column. Each error code in the Results column represents a single failure encountered during the last iteration. Each error code in the (cumulative) column represents the sum of all errors detected during the test. Cumulative error codes that differ from Results error codes indicate multiple, or intermittent errors. When the error codes are the same the errors are systematic. Refer to the appropriate test for an explanation of what the test does and how to decode the errors.

4-4

4-21. DATA TEST.

4-22. Purpose. This test (figure 4-4) checks all data paths for signals LD0 through LD15 by writing data to the memory RAMs and then reading it back. When a bit cannot be written and read back in both its high and low level, an error is flagged. During the test, data is written to only one address in each of the 16 RAMs, therefore, a successful test indicates that the data paths are functioning correctly, but it does not imply that all cells in all RAMs are operating properly. See Pattern Test for RAM cell checks. Note that address bus failures generally do not affect the reliability of this test.

4-23. Decoding Data Test Errors. All errors found are formatted as a four character hexidecimal word. Each character represents four binary digits, each digit corresponding to a single data line. To decode an error word, convert each character to its binary equivalent and compare it with the chart shown below. If necessary, refer to table 4-2 for hexidecimal-to-binary conversion. For example, if the error word is 0005, there are errors on the LD0 and LD2 data paths. The U-number shown in the chart indicates the RAM that may have a failure.

a. Data Test Errors.

```
Hex    Binary                     Signal in error/RAM
xxxx=  0000  0000  0000  0000     None
       ----  ----  ----  ---1     LD0    U1
       ----  ----  ----  --1-     LD1    U17
       ----  ----  ----  -1--     LD2    U2
       ----  ----  ----  1---     LD3    U18
       ----  ----  ---1  ----     LD4    U3
       ----  ----  --1-  ----     LD5    U19
       ----  ----  -1--  ----     LD6    U4
       ----  ----  1---  ----     LD7    U20
       ----  ---1  ----  ----     LD8    U5
       ----  --1-  ----  ----     LD9    U21
       ----  -1--  ----  ----     LD10   U6
       ----  1---  ----  ----     LD11   U22
       ---1  ----  ----  ----     LD12   U7
       --1-  ----  ----  ----     LD13   U23
       -1--  ----  ----  ----     LD14   U8
       1---  ----  ----  ----     LD15   U24
       LD = Low Data
```

4-24. ADDRESS TEST.

4-25. Purpose. All 14 address lines are checked in this test (figure 4-4) to make certain they are intact. Data is written to selected addresses in the RAMs and read back. When each bit at the selected addresses cannot be written and read at its high and low state, an error is noted.

4-26. Decoding Address Test Errors. Because data errors can cause an address test to fail, both the address bits and data bits are flagged when a failure occurs. Decode the four character address error word using the chart shown below, and decode the data error word using the chart shown in the Data Test. Refer to table 4-2 for hexidecimal-to-binary conversion, if necessary. Significant error conditions follow.

a. Address Test Errors.

```
Hex     Binary                        Signal in error
xxxx=  0000 0000  0000  0000  None
       00--  ----  ----  ---1  LA0
       00--  ----  ----  --1-  LA1
       00--  ----  ----  -1--  LA2
       00--  ----  ----  1---  LA3
       00--  ----  ---1  ----  LA4
       00--  ----  --1-  ----  LA5
       00--  ----  -1--  ----  LA6
       00--  ----  1---  ----  LA7
       00--  ---1  ----  ----  LA8
       00--  --1-  ----  ----  LA9
       00--  -1--  ----  ----  LA10
       00--  1---  ----  ----  LA11
       00-1  ----  ----  ----  LA12
       001-  ----  ----  ----  LA13
       LA = Low Address
```

b. Address Error = 3FFF. Indicates all address lines are failing. This is because there are only 14 address lines and an error of FFFF cannot be returned from the test.

c. Multiplexed Address Errors. When two address bits are in error, check to see if they are separated by seven bits. This may indicate a single line is failing that is carrying both bits in multiplexed form. Multiplexed address bits are shown in below.

<div align="center">

Multiplexed Address Bits

Bits	Node	Hex
0 and 7	U37 - 11	0081
1 and 8	U37 - 13	0101
2 and 9	U37 - 12	0204
3 and 10	U37 - 18	0408
4 and 11	U37 - 17	0810
5 and 12	U37 - 16	1020
6 and 13	U37 - 19	2040

</div>

4-27. BYTE OPERATION TEST.

4-28. Purpose. This test (figure 4-4) checks the module's ability to perform byte operations. When the upper and lower bytes cannot be written and read back correctly, an error condition is noted.

4-29. Decoding Byte Operation Errors. The errors found in this test are not decoded. When this test fails and all other tests pass, the failure is probably associated with signals LWRTL and LWRTU in the read/write control circuit.

4-30. PATTERN TEST.

4-31. Purpose. All of the cells in each RAM are checked by this test (figure 4-4). When both the high and low state cannot be written and read back from each cell, a failure is noted.

4-32. Decoding Pattern Test Errors. All errors found are formatted as a four character hexidecimal word. Each character represents four binary digits, each digit corresponding to a single bit. To decode an error word, convert each character to its binary equivalent and compare it with the chart shown below. If necessary, see table 4-2 for hexidecimal-to-binary conversion. For example, if the error word is 0060, there are errors on the LD5 and LD6 data paths. The U-number shown in the chart indicates the RAM that may have a failure.

   a. Pattern Test Errors.

```
Hex     Binary                     Signal in error/RAM
xxxx =  0000 0000 0000 0000 None
        ---- ---- ---- ---1 LD0   U1
        ---- ---- ---- --1- LD1   U17
        ---- ---- ---- -1-- LD2   U2
        ---- ---- ---- 1--- LD3   U18
        ---- ---- ---1 ---- LD4   U3
        ---- ---- --1- ---- LD5   U19
        ---- ---- -1-- ---- LD6   U4
        ---- ---- 1--- ---- LD7   U20
        ---- ---1 ---- ---- LD8   U5
        ---- --1- ---- ---- LD9   U21
        ---- -1-- ---- ---- LD10  U6
        ---- 1--- ---- ---- LD11  U22
        ---1 ---- ---- ---- LD12  U7
        --1- ---- ---- ---- LD13  U23
        -1-- ---- ---- ---- LD14  U8
        1--- ---- ---- ---- LD15  U24
        LD = Low Data
```

4-33. REFRESH TEST.

4-34. Display. This display shows the two Refresh test categories available and their test results. Use the display to review test conditions.
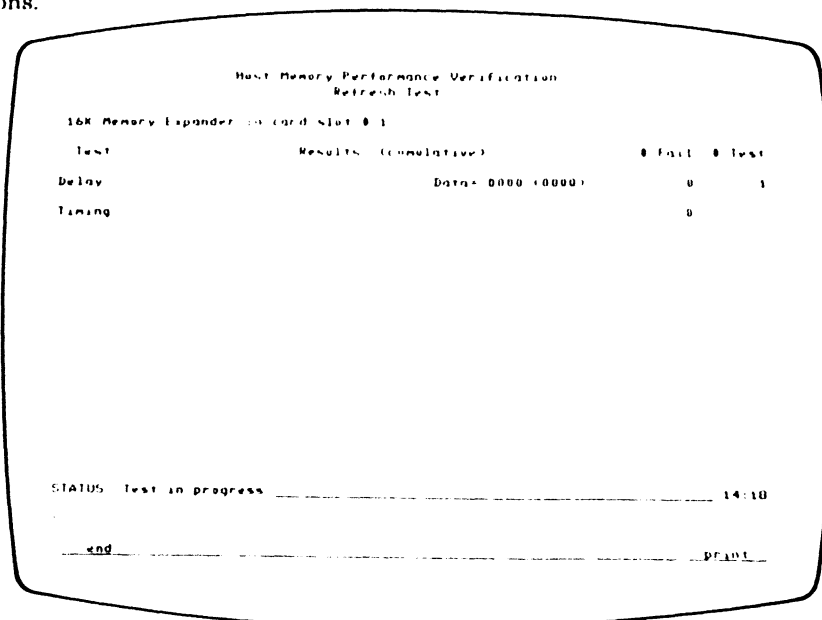
Figure 4-5. Refresh Test Display

4-35. Running the Refresh Tests. When this screen is displayed, the two tests are always running. Press the **end** softkey to stop the tests and return to the Total PV Display. Each iteration takes approximately ten seconds.

4-36. Using the Refresh Results. The total number of errors detected during the tests is shown in the # Fail column. Each error code in the Results column represents a single failure encountered during the last iteration. Each error code in the (cumulative) column represents the sum of all errors detected during the test. Cumulative error codes that differ from Results error codes indicate multiple, or intermittent errors. When the error codes are the same, the errors are systematic. Refer to the appropriate test for an explanation of what the test does and how to decode the errors.

4-37. DELAY TEST.

4-38. Purpose. This test (figure 4-5) checks for hard failures in the refresh circuitry. When data cannot be written to the RAMs and read back correctly after waiting several refresh cycles, an error is noted. When this test fails and all other tests pass, the problem lies in the refresh circuit.

4-39. Decoding Delay Test Errors. All errors found are formatted as a four character hexidecimal word. Each character represents four binary digits, each digit corresponding to a single bit. To decode an error word, convert each character to its binary equivalent and compare it with the chart shown below. See table 4-2 for hexidecimal-to-binary conversion, if necessary. For example, if the error word is 0A00, there are errors on the LD9 and LD11 data paths. The U-number shown in the chart indicates the RAM that may have a failure.

    a.   Delay Test Errors.

```
Hex    Binary                        Signal in error/RAM
xxxx=  0000 0000 0000 0000 None
       ——— ——— ——— ——1  LD0    U1
       ——— ——— ——— —1-  LD1    U17
       ——— ——— ——— -1—  LD2    U2
       ——— ——— ——— 1—   LD3    U18
       ——— ——— ——1 ———  LD4    U3
       ——— ——— —1- ———  LD5    U19
       ——— ——— -1— ———  LD6    U4
       ——— ——— 1— ———   LD7    U20
       ——— ——1 ——— ———  LD8    U5
       ——— —1- ——— ———  LD9    U21
       ——— -1— ——— ———  LD10   U6
       ——— 1— ——— ———   LD11   U22
       ——1 ——— ——— ———  LD12   U7
       —1- ——— ——— ———  LD13   U23
       -1— ——— ——— ———  LD14   U8
       1— ——— ——— ———   LD15   U24
       LD = Low Data
```

4-40. TIMING TEST.

4-41. Purpose. Soft failures of the refresh circuit are detected in this test (figure 4-5). When the circuit refreshes memory more frequently than necessary, the power consumption on the +12 volt supply increases. Also, the mainframe CPU accesses may be delayed by this condition. The test detects statistically significant deviations from normal CPU access rates over a timed interval. When the access rate is not within the normal range, a failure is flagged.

4-42. Decoding Timing Errors. The errors found in this test are not decoded. When the test fails and all other tests pass, the failure is probably associated with the refresh clock, components U49 and U50 or multiplexer U37.

4-43. SIGNATURE ANALYSIS TEST.

4-44. Display. There is no separate display for this test. See the Total PV Display, figure 4-3.

4-45. Running the Signature Analysis Test. There are two separate Signature Analysis loops used to test the module, Loop A and Loop B. Loop A tests all circuitry, except the refresh circuit, and is run while the PV is in the Signature Analysis mode. To run the loop A test, proceed as follows. Locate the highlight line over the words Signature Analysis on the Total PV display and press the **start** softkey. In this mode the PV places signals on the lines of the module that generate known signatures when read by an HP Signature Analyzer. Press the **end** softkey to stop the test.

4-46. A complete description of how to connect the Signature Analyzer and take signatures on Loop A is provided in the paragraphs on troubleshooting.

4-47. REFRESH ONLY TEST.

4-48. Display. There is no separate display for this test. See the Total PV Display, figure 4-3.

4-49. Running the Refresh Only Test. Position the highlight line over the words Refresh Only on the Total PV display and press the **start** softkey. To stop the test, press the **end** softkey.

4-50. Purpose. This test provides two functions during servicing of the refresh circuitry. First, the test checks the mainframe CPU and increments the counter on the display to indicate the CPU is running. Second, this PV mode generates signatures for the Loop B Signature Analysis which checks the refresh circuitry.

4-51. A complete description of how to connect the Signature Analyzer and take signatures on Loop B is provided in the paragraphs on troubleshooting.

Table 4-1. Error Code Conversion

Hex	=Binary		Hex	= Binary
1	---1		8	1---
2	--1-		9	1--1
3	--11		A	1-1-
4	-1--		B	1-11
5	-1-1		C	11--
6	-11-		D	11-1
7	-111		E	111-
			F	1111

4-52. TROUBLESHOOTING.

4-53. When servicing to the component level is not practical, use the Performance Verification tests to quickly check the overall condition of the module. When any of the tests fail, try swapping with a good module. Because the 16k Memory Expansion Module interacts only with the 64000 mainframe, a failed memory PV can only be due to a module failure or to a mainframe failure.

4-54. The Performance Verification tests can be used to good advantage to isolate the functional area of the module that is failing. After determining the faulty functional area, Signature Analysis can be used to identify the faulty component.

4-55. When the Operation test fails, use Signature Analysis Loop A for component level servicing. When the Refresh test fails, use Signature Analysis Loop B.

4-56. When Low Memory Synchronization (LMSYN) is held low, the CPU is placed in a wait mode. Therefore, if this signal is stuck in the low state, the CPU will hang up the system. To release the system, remove buffers U38 and U40, and use a jumper wire to connect TP4 to ground. Remove jumper and replace buffers when finished.

4-57. TROUBLESHOOTING WITH SIGNATURE ANALYSIS.

4-58. Set up the memory module for Signature Analysis using the basic steps shown below.

```
┌──────────────┐
│   CAUTION    │
└──────────────┘
```

The Model 64032A 16k Memory Expansion Module must be installed and removed with the mainframe power off!

4-59. General Set-Up Procedure.

a. Turn off the power to the mainframe and remove the card cage access cover.

b. Remove the memory board. Insert an extender board in the card cage and insert the memory module in the extender.

4-60. Troubleshooting with Signature Analysis Loop A.

a. Connect the SA Start lead to U26 pin 5 and set Start on the on the falling edge.

b. Connect the SA Stop lead to U35 pin 11 and set Stop on the rising edge.

c. Connect the SA Clock lead to U50 pin 11 and set Clock to the falling edge.

d. Disable the refresh circuit by connecting TP2 on the memory module to the ground test point (TP6) with a jumper wire.

e. Connect the SA ground lead to the memory module ground test point (TP6).

f. Turn on power to mainframe and begin memory module PV.

g. Locate the highlight line over the words Signature Analysis on the Total PV display and press the start softkey. Press the end softkey to stop the test.

h. Use signatures shown in table 4-2.

4-61. Troubleshooting with Signature Analysis Loop B.

a. Connect the SA Start and Stop lead(s) to TP1 on the memory board. Set Start on the rising edge and set Stop on the falling edge.

b. Connect the SA clock lead to U42, pin 3, and set to the rising edge.

c. Connect the SA ground lead to the memory module ground test point (TP6).

d. Turn on power to mainframe and begin memory module PV.

e. Locate the highlight line over the words Refresh Only Test on the Total PV display and press the start softkey. Press the end softkey to stop the test.

f. Use signatures shown in table 4-3.

Table 4-2. Signature Analysis Loop A

Performance Verification Mode: Signature Analysis.
Procedure: Ground TP2.

Start=U26 pin 5, falling edge (LBPCPEND).
Stop=U35 pin 11, rising edge (LSTM).
Clock=U50 pin 14, falling edge.
Vh=001U.

Node	Sig	Comments	Node	Sig	Comments
U25 - 4	0018		U43 - 1	001U	
U25 - 5	001U		U43 - 2	0000	
U25 - 6	0018		U43 - 3		unstable
U25 - 11	000U		U43 - 4		unstable
U25 - 12	001U*		U43 - 5	001U*	
			U43 - 6	0000*	
U26 - 5	0007		U43 - 8	0007	
U26 - 6	0018*		U43 - 9	0018	
U26 - 8	001U				
U26 - 9	0000		U44 - 1	001U	
			U44 - 3	0000*	
U35 - 1	000U		U44 - 6	001U*	
U35 - 2	0010		U44 - 8	001U*	
U35 - 3	000U		U44 - 11	0018	
U35 - 4	0010				
U35 - 5	000U		U45 - 6		unstable
U35 - 6	0010		U45 - 8		unstable
U35 - 10	001U*				
U35 - 11	0000*		U46 - 6		unstable
			U46 - 8	0018	
U36 - 3	001U				
U36 - 6	001U*		U47 - 1	0000	
U36 - 8	0000*		U47 - 3	0018	
U36 - 11	0018		U47 - 4	001U	
			U47 - 6	001U	
U39 - 6	0003				
U39 - 8		unstable	U48 - 8	001U*	
U39 - 12		unstable	U49 - 12		unstable
			U50 - 15		unstable
U41 - 3	000U				
U41 - 4	0007				
U41 - 5	0007				
U41 - 13	0000*				
U42 - 5	001U*				
U42 - 6	0010				
U42 - 8	0000				
U42 - 9	001U				

*indicates blinking probe.

Table 4 3. Signature Analysis Loop B

Performance Verification Mode: Refresh Only.
Procedure: NA.

Start=Memory Board, TP1, rising edge.
Stop=Memory Board, TP1, falling edge.
Clock=Memory Board U42, pin 3, rising edge.
Vh=76U0.

Node	Sig	Comments	Node	Sig	Comments
TP1	76U0		U41 - 3	276C	
			U41 - 4	U163	
U35 - 2	5196		U41 - 5	9A67	
U35 - 4	5196		U41 - 13	F5AF	
U37 - 1	93F8		U47 - 3	76U0	
U37 - 2	76U0		U47 - 6	76U0	
U37 - 3	8793				
U37 - 11	8AUC				
U37 - 12	1U5P				
U37 - 13	9241				
U37 - 16	826P				
U37 - 17	U665				
U37 - 18	AAHU				
U37 - 19		Unstable			

*indicates blinking probe.

SECTION V

ADJUSTMENT

There are no adjustments on the 16k Memory Expansion Module.

SECTION VI

REPLACEABLE PARTS

6-1. INTRODUCTION.

6-2. This section contains information for ordering parts. Table 6-1 lists abbreviations used in the parts list and throughout the manual. Table 6-2 lists all replaceable parts in reference designator order. Table 6-3 contains the names and addresses that correspond to the manufactures' five-digit code numbers.

6-3. ABBREVIATIONS.

6-4. Table 6-1 lists abbreviations used in the parts list, schematics, and throughout the manual. In some cases, two forms of the abbreviation are used: one all in capital letters, and one partial or no capitals. This occurs because the abbreviations in the parts list are always capitals. However, in the schematics and other parts of the manual, other abbreviation forms are used with both lowercase and uppercase letters.

6-5. REPLACEABLE PARTS LIST.

6-6. Table 6-2 is the list of replaceable parts and is organized as follows:

    a. Chassis-mounted parts in alphanumerical order by reference designation.

    b. Electrical assemblies and their components in alphanumerical order by reference designation.

    c. Miscellaneous.

The information given for each part consists of the following:

    a. The Hewlett-Packard part number and the check digit.

    b. The total quantity (Qty) in the instrument.

    c. The description of the part.

    d. A five-digit code that indicates the manufacturer.

    e. The manufacturers' part number.

The total quantity for each part is given only once - at the first appearance of the part number in the list.

6-7. ORDERING INFORMATION.

6-8. To order a part listed in the replaceable parts table, quote the Hewlett-Packard part number and check digit, indicate the quantity.

6-9. To order a part that is not listed in the replaceable parts table, include the instrument model number, instrument repair number, the description and function of the part, and the number of parts required. Address the order to the nearest Hewlett-Packard office.

6-10. DIRECT MAIL ORDER SYSTEM.

6-11. Within the USA, Hewlett-Packard can supply parts through a direct mail order system. Advantages of using the system are as follows:

    a. Direct ordering and shipment from the HP Parts Center in Mountain View, California.

    b. No maximum or minimum on any mail order (there is a minimum order amount for parts ordered through a local HP office when the orders require billing and invoicing).

    c. Prepaid transportation (there is a small handling charge for each order).

    d. No invoices - to provide these advantages, a check or money order must accompany each order.

6-12. Mail-order forms and specific ordering information are available through your local HP office. Addresses and phone numbers are located at the back of this manual.

Table 6-1. Reference Designators and Abbreviations

REFERENCE DESIGNATORS

A	assembly	F	fuse	MP	mechanical part	U	integrated circuit		
B	motor	FL	filter	P	plug	V	vacuum, tube, neon		
BT	battery	IC	integrated circuit	Q	transistor		bulb, photocell, etc		
C	capacitor	J	jack	R	resistor	VR	voltage regulator		
CP	coupler	K	relay	RT	thermistor	W	cable		
CR	diode	L	inductor	S	switch	X	socket		
DL	delay line	LS	loud speaker	T	transformer	Y	crystal		
DS	device signaling lamp	M	meter	TB	terminal board	Z	tuned cavity network		
E	misc electronic part	MK	microphone	TP	test point				

ABBREVIATIONS

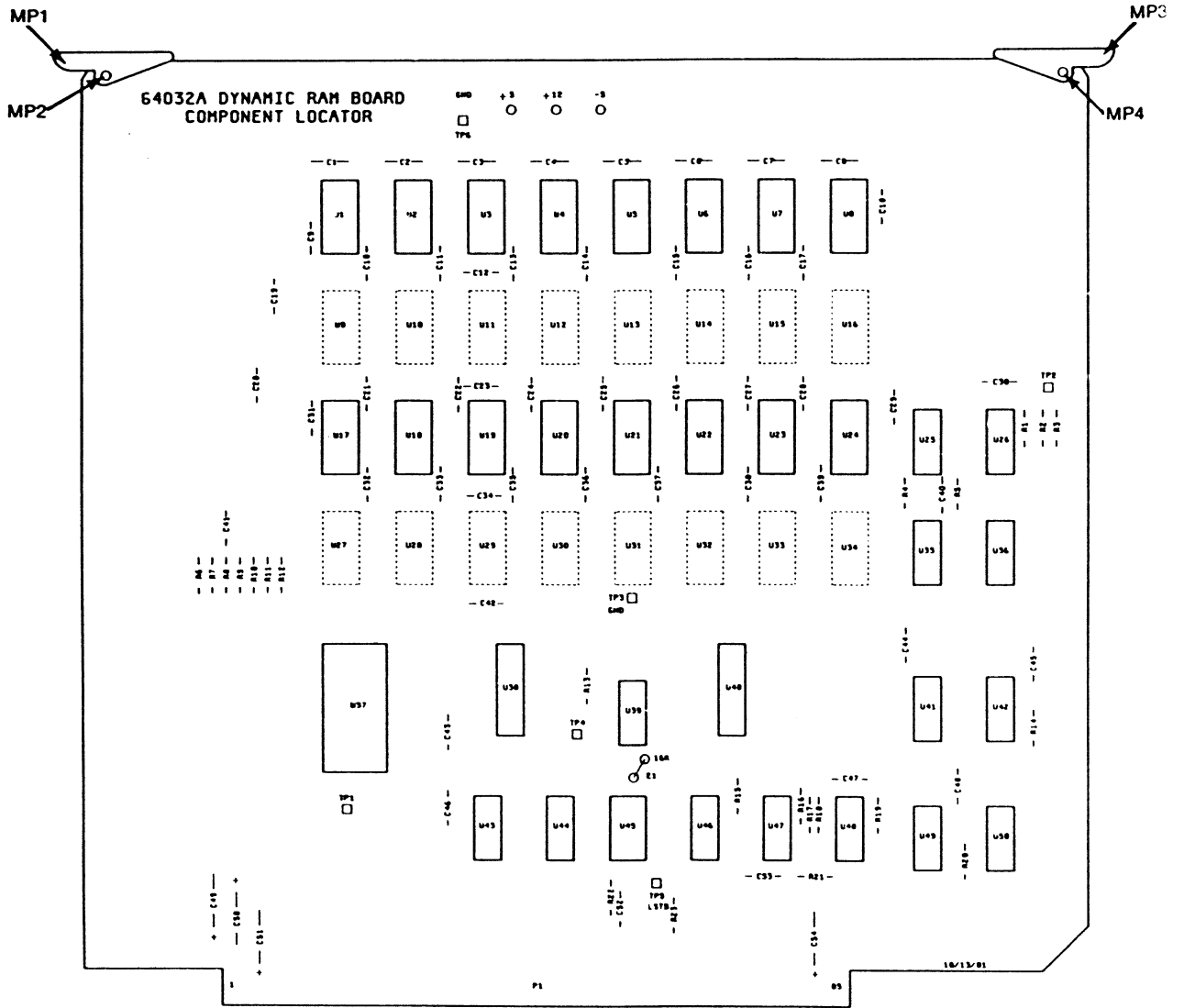|									
A	amperes	H	henries	N/O	normally open	RMO	rack mount only		
AFC	automatic frequency control	HDW	hardware	NOM	nominal	RMS	root-mean square		
AMPL	amplifier	HEX	hexagonal	NPO	negative positive zero	RWV	reverse working voltage		
		HG	mercury		(zero temperature				
BFO	beat frequency oscillator	HR	hour(s)		coefficient)				
BE CU	beryllium copper	HZ	hertz	NPN	negative-positive	S-B	slow-blow		
BH	binder head				negative	SCR	screw		
BP	bandpass			NRFR	not recommended for	SE	selenium		
BRS	brass	IF	intermediate freq		field replacement	SECT	section(s)		
BWO	backward wave oscillator	IMPG	impregnated	NSR	not separately	SEMICON	semiconductor		
		INCD	incandescent		replaceable	SI	silicon		
CCW	counter-clockwise	INCL	include(s)			SIL	silver		
CER	ceramic	INS	insulation(ed)	OBD	order by description	SL	slide		
CMO	cabinet mount only	INT	internal	OH	oval head	SPG	spring		
COEF	coeficient			OX	oxide	SPL	special		
COM	common	K	kilo 1000			SST	stainless steel		
COMP	composition					SR	split ring		
COMPL	complete	LH	left hand	P	peak	STL	steel		
CONN	connector	LIN	linear taper	PC	printed circuit				
CP	cadmium plate	LK WASH	lock washer	PF	picofarads 10 12	TA	tantalum		
CRT	cathode-ray tube	LOG	logarithmic taper		farads	TD	time delay		
CW	clockwise	LPF	low pass filter	PH BRZ	phosphor bronze	TGL	toggle		
				PHL	phillips	THD	thread		
DEPC	deposited carbon	M	milli 10 3	PIV	peak inverse voltage	TI	titanium		
DR	drive	MEG	meg 10⁶	PNP	positive-negative-	TOL	tolerance		
		MET FLM	metal film		positive	TRIM	trimmer		
ELECT	electrolytic	MET OX	metallic oxide	P/O	part of	TWT	traveling wave tube		
ENCAP	encapsulated	MFR	manufacturer	POLY	polystyrene				
EXT	external	MHZ	mega hertz	PORC	porcelain	U	micro 10 6		
		MINAT	miniature	POS	position(s)				
F	farads	MOM	momentary	POT	potentiometer	VAR	variable		
FH	flat head	MOS	metal oxide substrate	PP	peak-to-peak	VDCW	dc working volts		
FIL H	fillister head	MTG	mounting	PT	point				
FXD	fixed	MY	mylar	PWV	peak working voltage	W/	with		
						W	watts		
G	giga (10⁹)	N	nano (10 9)	RECT	rectifier	WIV	working inverse voltage		
GE	germanium	N/C	normally closed	RF	radio frequency				
GL	glass	NE	neon	RH	round head or	WW	wirewound		
GRD	ground(ed)	NI PL	nickel plate		right hand	W/O	without		

Figure 6-1. Component Locator

Table 6-2. Replaceable Parts List

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	64032-66501	2	1	MEMORY BOARD-16K DYN	28480	64032-66501
C1	0160-2055	9	50	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C2	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C3	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C4	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C5	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C6	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C7	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C8	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C9	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C10	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C11	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C12	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C13	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C14	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C15	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C16	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C17	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C18	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C19	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C20	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C21	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C22	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C23	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C24	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C25	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C26	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C27	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C28	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C29	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C30	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C31	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C32	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C33	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C34	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C35	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C36	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C37	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C38	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C39	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C40	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C41	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C42	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C43	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C44	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C45	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C46	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C47	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C48	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C49	0180-0474	4	4	CAPACITOR-FXD 15UF+-10% 20VDC TA	28480	0180-0474
C50	0180-0474	4		CAPACITOR-FXD 15UF+-10% 20VDC TA	28480	0180-0474
C51	0180-0474	4		CAPACITOR-FXD 15UF+-10% 20VDC TA	28480	0180-0474
C52	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C53	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C54	0180-0474	4		CAPACITOR-FXD 15UF+ 10% 20VDC TA	28480	0180-0474
E1	8159-0013	4	AR	WR 22G BARE	00000	
MP1	64032-85001	7	1	EXTRACTOR-PC	28480	64032-85001
MP2	1480-0116	8	2	PIN-GRV .062-IN-DIA .25-IN-LG STL	28480	1480-0116
MP3	64032-85002	8	1	EXTRACTOR-PC	28480	64032-85002
MP4	1480-0116	8		PIN-GRV .062-IN-DIA .25-IN-LG STL	28480	1480-0116
R1	0757-0442	9	10	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1002-F
R2	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1002-F
R3	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1002-F
R4	0683-3305	2	13	RESISTOR 33 5% .25W FC TC=-400/+500	01121	CB3305
R5	0683-3305	2		RESISTOR 33 5% .25W FC TC=-400/+500	01121	CB3305
R6	0683-3305	2		RESISTOR 33 5% .25W FC TC=-400/+500	01121	CB3305
R7	0683-3305	2		RESISTOR 33 5% .25W FC TC=-400/+500	01121	CB3305
R8	0683-3305	2		RESISTOR 33 5% .25W FC TC=-400/+500	01121	CB3305
R9	0683-3305	2		RESISTOR 33 5% .25W FC TC=-400/+500	01121	CB3305
R10	0683-3305	2		RESISTOR 33 5% .25W FC TC=-400/+500	01121	CB3305

Table 6-2. Replaceable Parts List (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
R11	0683-3305	2		RESISTOR 33 5% .25W FC TC=-400/+500	01121	CB3305
R12	0683-3305	2		RESISTOR 33 5% .25W FC TC=-400/+500	01121	CB3305
R13	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R14	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R15	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R16	0683-3305	2		RESISTOR 33 5% .25W FC TC=-400/+500	01121	CB3305
R17	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R18	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R19	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R20	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R21	0683-3305	2		RESISTOR 33 5% .25W FC TC=-400/+500	01121	CB3305
R22	0683-3305	2		RESISTOR 33 5% .25W FC TC=-400/+500	01121	CB3305
R23	0683-3305	2		RESISTOR 33 5% .25W FC TC=-400/+500	01121	CB3305
TP1	0360-0535	0	6	TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
TP2	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
TP3	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
TP4	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
TP5	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
TP6	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
U1	1818-1396	5	16	IC-MEMORY	00037	UP416C-2(SELECTED)
U2	1818-1396	5		IC-MEMORY	00037	UP416C-2(SELECTED)
U3	1818-1396	5		IC-MEMORY	00037	UP416C-2(SELECTED)
U4	1818-1396	5		IC-MEMORY	00037	UP416C-2(SELECTED)
U5	1818-1396	5		IC-MEMORY	00037	UP416C-2(SELECTED)
U6	1818-1396	5		IC-MEMORY	00037	UP416C-2(SELECTED)
U7	1818-1396	5		IC-MEMORY	00037	UP416C-2(SELECTED)
U8	1818-1396	5		IC-MEMORY	00037	UP416C-2(SELECTED)
U17	1818-1396	5		IC-MEMORY	00037	UP416C-2(SELECTED)
U18	1818-1396	5		IC-MEMORY	00037	UP416C-2(SELECTED)
U19	1818-1396	5		IC-MEMORY	00037	UP416C-2(SELECTED)
U20	1818-1396	5		IC-MEMORY	00037	UP416C-2(SELECTED)
U21	1818-1396	5		IC-MEMORY	00037	UP416C-2(SELECTED)
U22	1818-1396	5		IC-MEMORY	00037	UP416C-2(SELECTED)
U23	1818-1396	5		IC-MEMORY	00037	UP416C-2(SELECTED)
U24	1818-1396	5		IC-MEMORY	00037	UP416C-2(SELECTED)
U25	1820-1201	6	1	IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
U26	1820-0693	8	3	IC FF TTL S D-TYPE POS EDGE-TRIG	01295	SN74S74N
U35	1820-1199	1	2	IC INV TTL LS HEX 1-INP	01295	SN74LS04N
U36	1820-1197	9	2	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U37	1820-2076	5	1	IC MISC TTL S	34649	P3242
U38	1820-2024	3	2	IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U39	1820-0907	7	1	IC GATE TTL NAND TPL 3-INP	01295	SN7412N
U40	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U41	1820-1433	6	1	IC SHF-RGTR TTL LS R-S SERIAL-IN PRL-OUT	01295	SN74LS164N
U42	1820-0693	8		IC FF TTL S D-TYPE POS EDGE TRIG	01295	SN74S74N
U43	1820-1199	1		IC INV TTL LS HEX 1-INP	01295	SN74LS04N
U44	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U45	1820-1204	9	2	IC GATE TTL LS NAND DUAL 4-INP	01295	SN74LS20N
U46	1820-1204	9		IC GATE TTL LS NAND DUAL 4-INP	01295	SN74LS20N
U47	1820-1208	3	1	IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
U48	1820-0693	8		IC FF TTL S D-TYPE POS EDGE-TRIG	01295	SN74S74N
U49	1820-1430	3	2	IC CNTR TTL LS BIN SYNCHRO POS-EDGE TRIG	01295	SN74LS161AN
U50	1820-1430	3		IC CNTR TTL LS BIN SYNCHRO POS-EDGE TRIG	01295	SN74LS161AN
XU1	1200-0607	0	16	SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU2	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU3	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU4	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU5	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU6	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU7	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU8	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU17	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU18	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU19	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU20	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU21	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU22	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU23	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU24	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU37	1200-0567	1	1	SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0567
XU38	1200-0639	8	2	SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
XU40	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639

See introduction to this section for ordering information

Table 6-3. Manufacturers' Codes

Mfr No.	Manufacturer Name	Address		Zip Code
00000	ANY SATISFACTORY SUPPLIER			
0003J	NIPPON ELECTRIC CO	TOYKO	JAPAN	
01121	ALLEN-BRADLEY CO	MILWAUKEE	WI	53204
01295	TEXAS INSTR INC SEMICOND CMPNT DIV	DALLAS	TX	75222
24546	CORNING GLASS WORKS (BRADFORD)	BRADFORD	PA	16701
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO	CA	94304
34649	INTEL CORP	MOUNTAIN VIEW	CA	95051
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS	MA	01247

SECTION VII

MANUAL CHANGES

This section normally contains information for backdating this manual for models with repair numbers prior to the one shown on the title page. Because this edition includes the information for the first repair number, there is no backdating material.

SECTION VIII

SERVICE

8-1. INTRODUCTION.

8-2.   This section contains background information for repairing the Model 64032A 16k Memory Expansion Module. For convenience, the schematic and other service information is provided on a fold-out service sheet.

8-3. BLOCK DIAGRAM THEORY.

8-4.   Refer to figure 8-1 Block Diagram for the relationships between the seven functional blocks of the memory module. Each of the blocks is described below.

8-5. IDENTIFY/SLOT SELECT.

8-6.   At various times the BPC requests the board's ID number. The identify/slot select circuit returns the ID 0401H to the BPC via the data bus.

8-7. RAM STORAGE.

8-8.   The memory is organized into 16k, 16 bit words, with each word comprised of an upper and lower 8 bit byte. Sixteen dynamically refreshed, 16k by one bit MOS RAMs are used for the storage. Each RAM's internal addressing is arranged as a square matrix of 128 rows by 128 columns, yielding addresses 0 through 16,343.

8-9. ADDRESS MULTIPLEXER.

8-10.   All RAMs are addressed by multiplexing the RAMs' internal row and column address via U37. The mode select on the multiplexer chooses between BPC initiated read/write activities and module initiated refresh requests.

8-11. TIMING/REFRESH CLOCK.

8-12.   The timing circuit uses the 25 MHz signal generated by the Display Controller and Driver board as the input for clocking purposes. The circuit produces two timing clocks, a 12.5 MHz module clock, and a 97.6 kHz signal for refreshing the memory RAMs.

8-13. READ/WRITE CONTROL.

8-14.   This circuit converts BPC read and write signals into the necessary RAM internal row and column control signals. During write operations the circuit selects upper, lower, or full word access. Read operations are always by full word, with the BPC performing byte functions after the access.

8-15. ARBITRATOR/SEQUENCER.

8-16.   The arbitrator/sequencer circuit schedules competing requests for memory operations between the BPC and the refresh circuit. When a BPC memory operation occurs, the arbitrator sequencer locks out refresh requests until the BPC memory operations are completed. In a similar manner, refresh operations cannot be interrupted by a BPC request for a read or write.

8-17. DATA BUFFERS.

8-18.   During a BPC read, the data buffers are enabled to output the 16 bit word onto the Low Data Out lines.
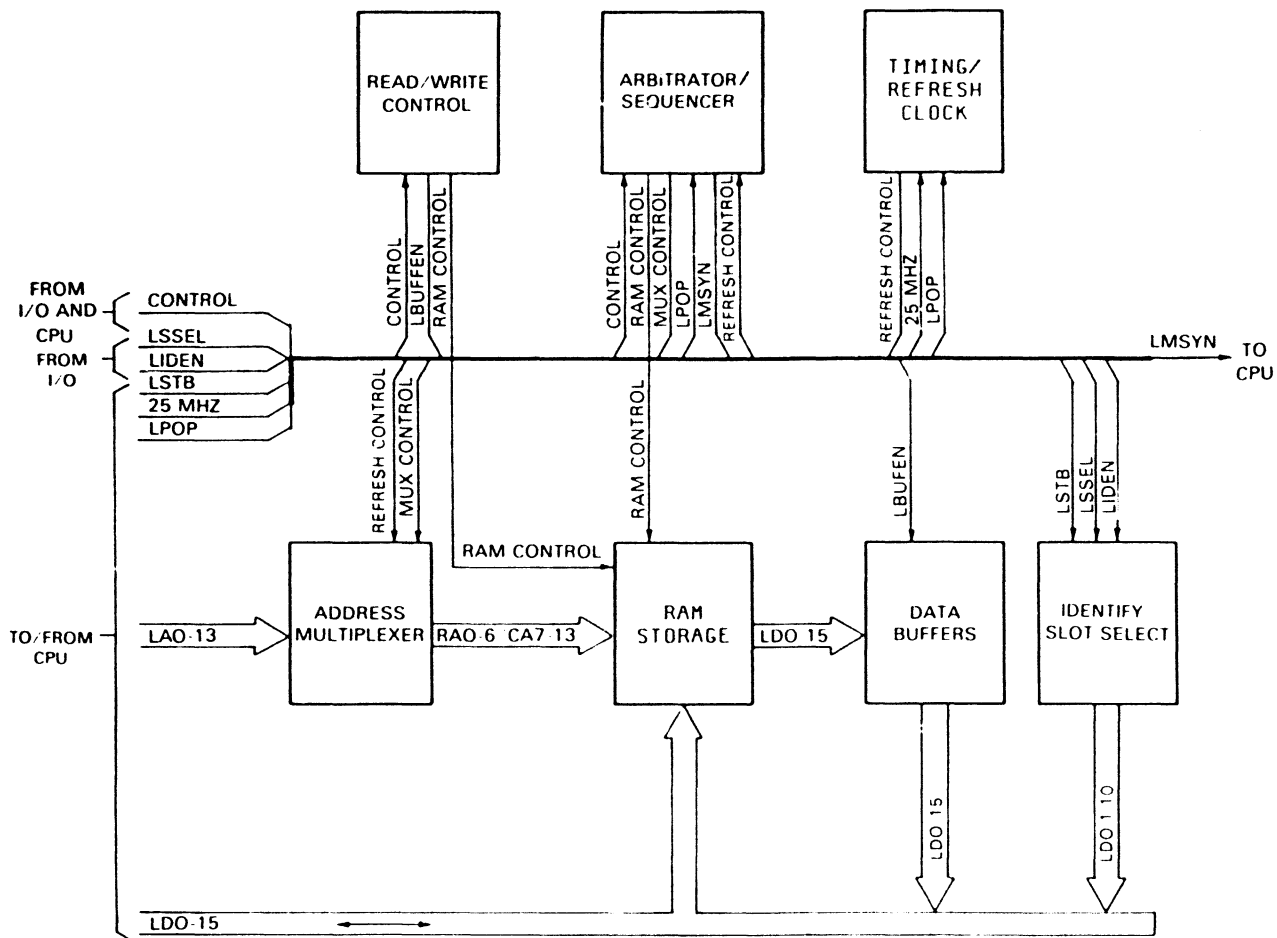
Figure 8-1. Block Diagram

8-19. DETAILED CIRCUIT THEORY.

8-20.   The following paragraphs provide a detailed description of the circuit operation within each functional block of the memory module. The circuits are shown in figure 8-4, Service Sheet 1.

8-21.   IDENTIFY SLOT/SELECT CIRCUIT.

8-22.   The board ID code is requested by the BPC. Control signals LSTB, LSS, and LID are inverted by U43A, U43D, and U43F. The high outputs from U43 are AND'd in U39A and U39C to form output data LD00, and LD010 on the LD0-15 data bus. The BPC reads and stores the ID (0401H) and slot number for future operations.

8-23.   RAM STORAGE CIRCUIT.

8-24.   The RAMs (U1-U8, U17-U24) circuit provides three major operations; read, write, and refresh. During a read operation, the RAM internal row addresses HRA0-HRA6 are latched into the chip by LRAS1 and the internal column addresses HCA0-HCA6 are latched by LCAS1. Data is made available on pin 14 of the RAMs for access by the data buffers circuit.

8-25.   In a write memory cycle, internal RAM row and column addresses are strobed into the RAMs as in the read cycle. Data (LD0-15) is written into the RAMs in the selected cell by active signal LWRTL and LWRTU.

8-26.   Refresh of the RAMs circuit is accomplished by performing a memory cycle at each of the 128 row addresses within a 2 millisecond time interval. The abitrator/sequencer circuit allows the address multiplexer to enable HRA0-HRA6, and LRAS1 to latch the address into the RAMs. The address multiplexer has an internal 7-bit counter capable of reading (i.e. refreshing) all 128 row addresses.

8-27.   ADDRESS MULTIPLEXER CIRCUIT.

8-28.   The address multiplexer, U37, provides internal RAM row and column address multiplexing and address indexing for refresh. The address multiplexer receives LA0-LA13 from the CPU and multiplexes it to seven inverted output pins. When chip controls M1 and M4 are active, internal RAM row addresses are output. When controls M2 and M4 are active, the internal RAM column addresses are output to the RAMs.

8-29.   During a refresh cycle, control signal REFRESH is activated and combined with the 97.6 kHz clocking signal on U37 pin 1. The multiplexer increments the address and refreshes one memory location. At the 97.6 kHz frequency rate, the entire memory is refreshed in 128 cycles within the required 2 millisecond period.

8-30.   REFRESH CLOCK CIRCUIT.

8-31.   The refresh clock circuit is initialized by LPOP. Clocking signal L25 MHz is input to U48A producing an output clock used by U49, U50 and the arbitrator/sequencer circuit. The output of U48A is 12.5 MHz and is divided by U50 and U49. The 97.6 kHz output from U49, pin 12, clocks the refresh counter in U37 (address multiplexer circuit) and enables the arbitrator/sequencer to start a refresh cycle at the completion on a BPC memory cycle.

8-32.   READ/WRITE CONTROL CIRCUIT.

8-33.   The read/write control circuit produces control signals for column address, write for upper or lower byte, and buffer enable, respectively. Control signal LMAP1 is sent to U47A. When HBPC and a clocking signal from the arbitrator/sequencer circuit are sent to U44D, a low is output on pin 11 of U44D. This low output is combined with LMAP1 in U47A producing LCAS1 Control signal LCAS1 enables the column address from the address multiplexer circuit into the RAMs.

8-34.   The CPU sends control signals LBYTE, LUPB and LWRT to U43B, U43C, and U43E in the read/write control circuit to select either a byte or word operation. When HBPC and the 97.6k clocking signal are active, the following functions can also occur.

8-35.   When LUPB is active, LWRTU is output from U45B. Signal LBYTE must be active to provide a byte operation. When LBYTE is inactive, LWRTU and LWRTL produce a word operation. When LUPB is inactive U45A outputs LWRTL. When LWRT is inactive and the CPU enables LSTB; U46A is enabled and outputs signal LBUFEN. When LBUFEN is active, data is enabled through the data buffers circuit to the CPU on the data bus.

8-36.   ARBITRATOR/SEQUENCER CIRCUIT.

8-37.   The arbitrator/sequencer circuit produces timing, refresh, BPC read or write, and sync control signals. The arbitrator/sequencer is responsible for control of refresh or BPC memory operation. The control signals cause multiplexing of the address lines and send LMSYN to the BPC. Signal LMSYN forces the BPC to wait until the read or write operation is complete. The arbitrator sequencer is also responsible for the timing of control signals to the RAMs and Data Buffers.

8-38.   When the correct address, data and read/write control signals are present, the BPC requests access to the RAMs by sending LSTM and LSS via U35, U25, and U44. This request is latched into U26A producing HBPCPEND. LMSYN becomes active via U39B, telling the BPC to wait until the memory cycle is complete.

8-39.   Any refresh cycle in progress is allowed to complete. HMEMOP goes low signifying the completion of the current memory cycle. LBPCPEN is clocked into U42A making HMEMOP true again beginning another memory cycle which allows the BPC to read or write. The transition of HMEMOP from low to high latches HBPCPEN into U42B producing signal HBPC. Signal HBPC in conjunction with a timing signal from U41 enables the read write control circuit and clears HBPCPEND, thus removing LMSYN. This sequence allows the BPC to complete its operation.

8-40. The dynamic RAMs used have only 7 address lines. In order to access the 16k locations in each RAM, 14 address bits are needed. The 14 signals are provided by loading the row address (LA0-6) by means of the row address strobe (LRAS) and the column address (LA7-13) by means of a column address strobe (LCAS). When HMEMOP becomes true, shift register U41 begins shifting ones to produce control signals that sequence the row and column address strobes and row and column address. After the memory cycle is complete, HMEMOP is cleared via U36B, U36C, U48B and U42A. HMEMOP is cleared when set and reset on U42A are both low.

8-41. DATA BUFFERS CIRCUIT.

8-42. Data from the RAMs circuit is enabled to the data bus (LD0-15), through the data buffers circuit, by means of signal LBUFEN (Low Buffer Enable).

8-43. CONVENTIONS.

8-44. The following conventions are used in this manual.

    a.   Components are numbered in upper left to lower right convention.

    b.   Logic symbology; see table 8-2.

    c.   TTL Logic Levels.

Electrical Level	Voltage
Input Low	< 0.8 V
Input High	> 2.0 V
Output Low	< 0.4 V
Output High	> 2.4 V

    d.   Mnemonics (signal names); see table 8-1.

First Letter	Active TTL Level
H	High
L	Low

    e.   Signature analysis locations are indicated in red on the schematic.

    f.   Abbreviations; see Section VI.

Table 8-1. Mnemonics

Mnemonic	Mnemonic Meaning	Active Level	Function
HBPC	BPC	High	When active, enables the read/write control circuit.
HBPCPEND	BPC Pending	High	When active, produces signal LMSYN forcing the microprocessor to wait until a read or write operation is complete.
HMEMOP	Memory Operation	High	When active, memory read, write, or Operation refresh is in progress.
HRA0-6/ HCA7-16	Row Address 0-6/Column Address 7-13	High	The row address and column address are selected by U37 to address RAM memory.
HREFRESH	Refresh	High	When active, enables refresh circuitry.
LA0-13	Address Bits 0-13	Low	A 14 bit address bus used to address RAM space.
LBPCPEND	BPC Pending	Low	When active, enables the refresh circuitry.
LBUFEN	Buffer Enable	Low	When active, enables buffers U38 and U40. Buffers enable data from the RAMs to the CPU. Only active during a read cycle.
LBYTE	Byte	Low	When low, indicates that a memory cycle is to involve an eight bit byte, rather than the full 16 bits of the word.
LCAS1	Column Address Strobe One	Low	When active, strobes the column address into RAM.
LD0-15	Data Bits 0-15	Low	A 16 bit bidirectional bus used to transfer data to and from the microprocessor. When LSTB is low, data is present on the bus.
LD0, LD10	Data Bits 0 and 10	Low	LD0 and LD10 are used to generate card ID code after being requested by the CPU.
LID	Identify Enable	Low	When active, enables all PC boards in slots 0 thru 9 (option slots) to generate card-type ID codes after interrogation by the slot select command (LSSEL).
LMAP1	Address Map 1	Low	When active, enables bank one of RAM.
LRAS2	Row Address Strobe Two	Low	Not used.
LMSYN	Memory Sync	Low	When active, forces the microprocessor to wait until the read or write operation is complete.
LPOP	Power On Pulse	Low	Initializes CPU and all option cards.

Table 8-1. Mnemonics (Cont'd)

Mnemonic	Mnemonic Meaning	Active Level	Function
LRAS1	Row Address Strobe One	Low	When active, strobes the row address into bank one of RAM. Also used during refresh.
LRAS2	Row Address Strobe Two	Low	When active, strobes the row address into bank two of RAM. Also used during refresh.
LREFPEND	Refresh Pending	Low	When active, enables the refresh circuitry.
LSS	Slot Select	Low	When active, allows module to place ID on CPU data bus.
LSTB	Strobe	Low	When active, and in the write mode, indicates the data bus has valid information. When active in the read mode, indicates the microprocessor is not driving the bus and the device addressed can now drive the bus.
LSTM	Start Memory	Low	Used to initiate a memory cycle. When active, indicates information on the Address Bus is valid.
LUPB	Upper Byte	Low	When active, indicates the upper byte is being written into, or read from. Used only when LBYTE is active.
LWRT	Write	Low	When active, the microprocessor writes to the addressed device.
LWRTL	Write Lower	Low	When active, the lower byte of RAM is written into.
LWRTU	Write Upper	Low	When active, the upper byte of RAM is written into.
L25MHz	25 MHz	Low	25 MHz clock used for general clocking. Generated by the display board.

Table 8-2. Logic Symbols

GENERAL

All signals flow from left to right, relative to the symbol's orientation with inputs on the left side of the symbol, and outputs on the right side of the symbol (the symbol may be reversed if the dependency notation is a single term.)

All dependency notation is read from left to right (relative to the symbol's orientation).

An external state is the state of an input or output outside the logic symbol.

An internal state is the state of an input or output inside the logic symbol. All internal states are True = High.

SYMBOL CONSTRUCTION

Some symbols consist of an outline or combination of outlines together with one or more qualifying symbols, and the representation of input and output lines.
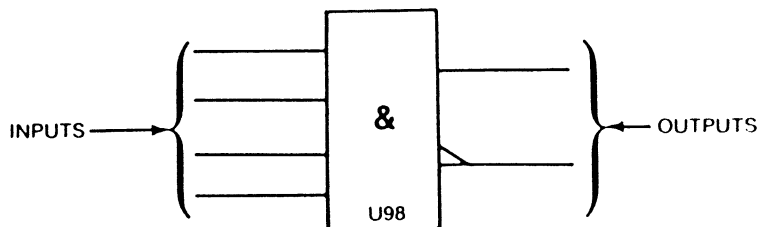
Some have a common Control Block with an array of elements:
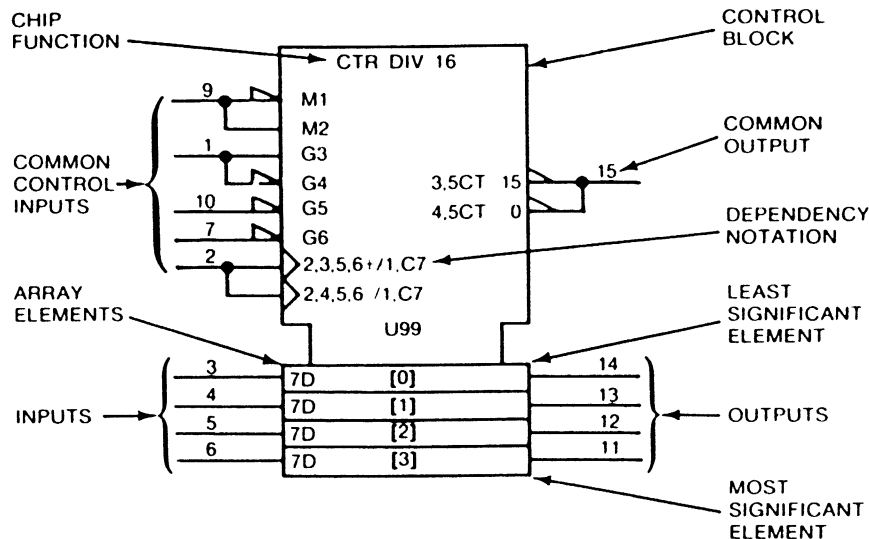
CONTROL BLOCK - All inputs and dependency notation affect the array elements directly. Common outputs are located in the control block. (Control blocks may be above or below the array elements.)

ARRAY ELEMENTS -All array elements are controlled by the control block as a function of the dependency notation. Any array element is independent of all other array elements. Unless indicated, the least significant element is always closest to the control block. The array elements are arranged by binary weight. The weights are indicated by powers of 2 (shown in [ ]).

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Table 8-2. Logic Symbols (Cont'd)

INPUTS - Inputs are located on the left side of the symbol and are affected by their dependency notation.

Common control inputs are located in the control block and control the inputs/outputs to the array elements according to the dependency notation.

Inputs to the array elements are located with the corresponding array element with the least significant element closest to the control block.

OUTPUTS - Outputs are located on the right side of the symbol and are effected by their dependency notation.

Common control outputs are located in the control block.

Outputs of array elements are located in the corresponding array element with the least significant bit closest to the control block.

CHIP FUNCTION - The labels for chip functions are defined, i.e., CTR - counter, MUX - multiplexer.

DEPENDENCY NOTATION

Dependency notation is always read from left to right relative to the symbol's orientation.

Dependency notation indicates the relationship between inputs, outputs, or inputs and outputs. Signals having a common relationship will have a common number, i.e., C7 and 7D....C7 controls D. Dependency notation 2,3,5,6+/1,C7 is read as when 2 and 3 and 5 and 6 are true, the input will cause the counter to increment by one count....or (/) the input (C7) will control the loading of the input value (7D) into the D flip-flops.

The following types of dependencies are defined:

a. AND (G), OR (V), and Negate (N) denote Boolean relationship between inputs and outputs in any combination.

b. Interconnection (Z) indicates connections inside the symbol.

c. Control (C) identifies a timing input or a clock input of a sequential element and indicates which inputs are controlled by it.

d. Set (S) and Reset (R) specify the internal logic states (outputs) of an RS bistable element when the R or S input stands at its internal 1 state.

e. Enable (EN) identifies an enable input and indicates which inputs and outputs are controlled by it (which outputs can be in their high impedance state).

f. Mode (M) identifies an input that selects the mode of operation of an element and indicates the inputs and outputs depending on that mode.

g. Address (A) identifies the address inputs.

h. Transmission (X) identifies bi-directional inputs and outputs that are connected together when the transmission input is true.

DEPENDENCY NOTATION SYMBOLS

A	Address (selects inputs/outputs) (indicates binary range)	N	Negate (compliments state)
C	Control (permits action)	R	Reset Input
EN	Enable (permits action)	S	Set Input
G	AND (permits action)	V	OR (permits action)
M	Mode (selects action)	Z	Interconnection
		X	Transmission

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Table 8-2. Logic Symbols (Cont'd)

OTHER SYMBOLS

∩ Analog Signal

▷◁ Inversion

⟶ Shift Right (or up)

& AND

O Negation

/ Solidus (allows an input or output to have more than one function)

}{ Bit Grouping

⟶✻⟶ Nonlogic Input/Output

▷ Buffer

Ω Open Circuit (NPN) (external resistor)

∇ Tri-State

! Compare

♂ Open Circuit (PNP) (external resistor)

, Causes notation and symbols to effect inputs/outputs in an AND relationship, and to occur in the order read from left to right.

▷ Dynamic

≥1 OR

=1 Exclusive OR

♁ Passive Pull Down (internal resistor)

( ) Used for factoring terms using algebraic techniques.

Ⴑ Hysteresis

♁ Passive Pull Up (internal resistor)

[ ] Information not defined.

? Interrogation

⅂ Postponed

Φ Logic symbol not defined due to complexity.

— Internal Connection

⟵ Shift Left (or down)

LABELS

BG	Borrow Generate	CO	Carry Output	J	J Input
BI	Borrow Input	CP	Carry Propagate	K	K Input
BO	Borrow Output	CT	Content	P	Operand
BP	Borrow Propagate	D	Data Input	T	Transition
CG	Carry Generate	E	Extension (input or output)	+	Count Up
CI	Carry Input	F	Function	..	Count Down

MATH FUNCTIONS

Σ	Adder	>	Greater Than
ALU	Arithmetic Logic Unit	<	Less Than
COMP	Comparator	CPG	Look Ahead Carry Generator
DIV	Divide By	π	Multiplier
=	Equal To	P-Q	Subtractor

CHIP FUNCTIONS

BCD	Binary Coded Decimal	DIR	Directional	RAM	Random Access Memory
BIN	Binary	DMUX	Demultiplexer	RCVR	Line Receiver
BUF	Buffer	FF	Flip-Flop	ROM	Read Only Memory
CTR	Counter	MUX	Multiplexer	SEG	Segment
DEC	Decimal	OCT	Octal	SRG	Shift Register

DELAY and MULTIVIBRATORS

ЛЛ Astable

|100 ns| Delay

!Л Nonretriggerable Monostable

NV Nonvolatile

ЛЛ Retriggerable Monostable

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ETCHED CIRCUIT BOARD

FRONT PANEL MARKING

REAR PANEL MARKING

MANUAL CONTROL

SCREWDRIVER ADJUSTMENT

ELECTRICAL TEST POINT
TP (WITH NUMBER)

TP1

NUMBERED WAVEFORM
NUMBER CORRESPONDS TO
ELECTRICAL TEST POINT NO

LETTERED TEST POINT
NO MEASUREMENT AID
PROVIDED

COMMON CONNECTIONS ALL LIKE DESIGNATED POINTS ARE CONNECTED

NUMBER ON WHITE BACKGROUND — OFF-PAGE CONNECTION.
LARGE UMBER ADJACENT — SERVICE SHEET NUMBER FOR OFF-PAGE CONNECTION.

CIRCLED LETTER — OFF PAGE CONNECTION BETWEEN PAGES OF SAME SERVICE
SHEET

INDICATES SINGLE SIGNAL LINE

NUMBER OF LINES ON A BUS

(925)

WIRE COLORS ARE GIVEN
BY NUMBERS IN PARENTHESES
USING THE RESISTOR COLOR
CODE

| (925) IS WHT RED GRN |
| 0 BLACK   5 GREEN |
| 1 BROWN   6 BLUE |
| 2 RED   7 VIOLET |
| 3 ORANGE   8 GRAY |
| 4 YELLOW   9 WHITE |

•   OPTIMUM VALUE SELECTED
     AT FACTORY, TYPICAL
     VALUE SHOWN, PART MAY
     HAVE BEEN OMITTED

UNLESS OTHERWISE INDICATED
RESISTANCE IN OHMS
CAPACITANCE IN PICOFARADS
INDUCTANCE IN MICROHENRIES

μP   MICROPROCESSOR
P-O   PART OF
NC   NO CONNECTION
CW   CLOCKWISE END OF VARIABLE
        RESISTOR

STD-20-09-81

Figure 8-2. Schematic Diagram Notes
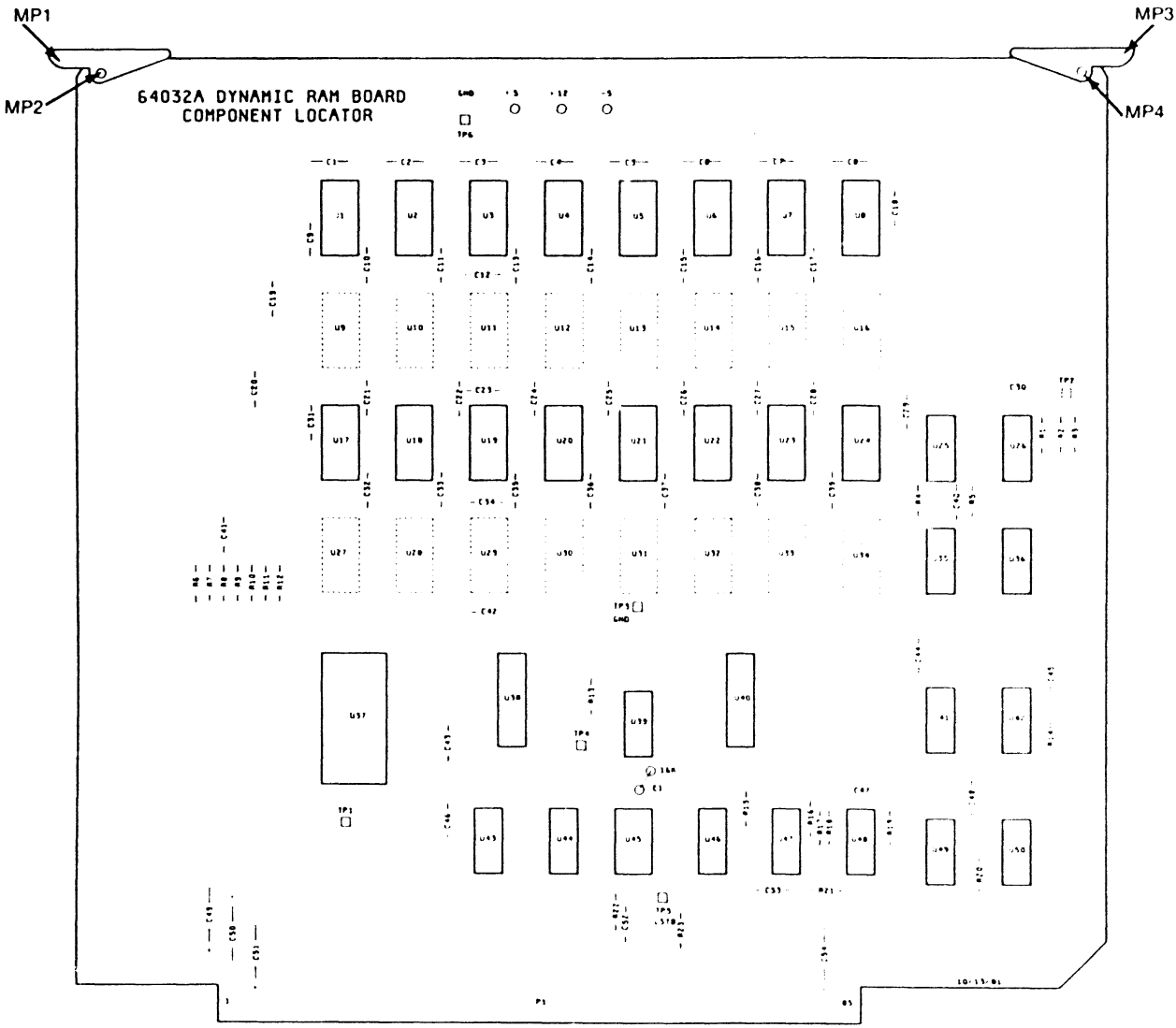
Figure 8-3. Component Locator

16K MEMORY EXPANSION MODULE (64032-66501)

REFRESH CLOCK

ADDRESS MULTIPLEXER

MUX/CNTR DIV 12C

TP6 GND

DATA BUFFERS

MEMORY

UPPER BYTE (SEE NOTE 1)

LOWER BYTE (SEE NOTE 1)

UPPER BYTE

LOWER BYTE

NOTE 1

RAM 16K X 1

TYPICAL RAM CONNECTIONS

CNTR DIV 16

CNTR DIV 16

12.5 MHZ

97.6 KHZ

READ/WRITE CONTROL

IDENTIFY/SLOT SELECT

ARBITRATOR SEQUENCER

P/O P1

HBPC

LDO-15

10/14/81

REFRESH MEMORY OPERATION

12.5 MHz clock

U49 P12 — High Start Refresh cycle from U48 (HIGH FOR 5.12us)

U26 P8 — Low Refresh latch

U36 P11 — High Set Memory OP latch

U42 P5 — High Memory OP

U42 P8 — High Refresh (stays high until reset by a BPC memory operation)

U41 P3 — HRAS

U41 P4 — H Column Enable

U41 P5 see note 1 — HCAS

U41 P13

U48 P8

Note 1 HCAS has no function during refresh. It was included to show the sequence

BCP MEMORY OPERATION

12.5 MHz clock

LS

LSTM

U26 P5 — Low Set Mem OP

U42 P5 — High Mem OP

U42 P9 — High BPC (stays high until a refresh occurs)

U41 P3 — HRAS

U41 P4 — H Column Enable
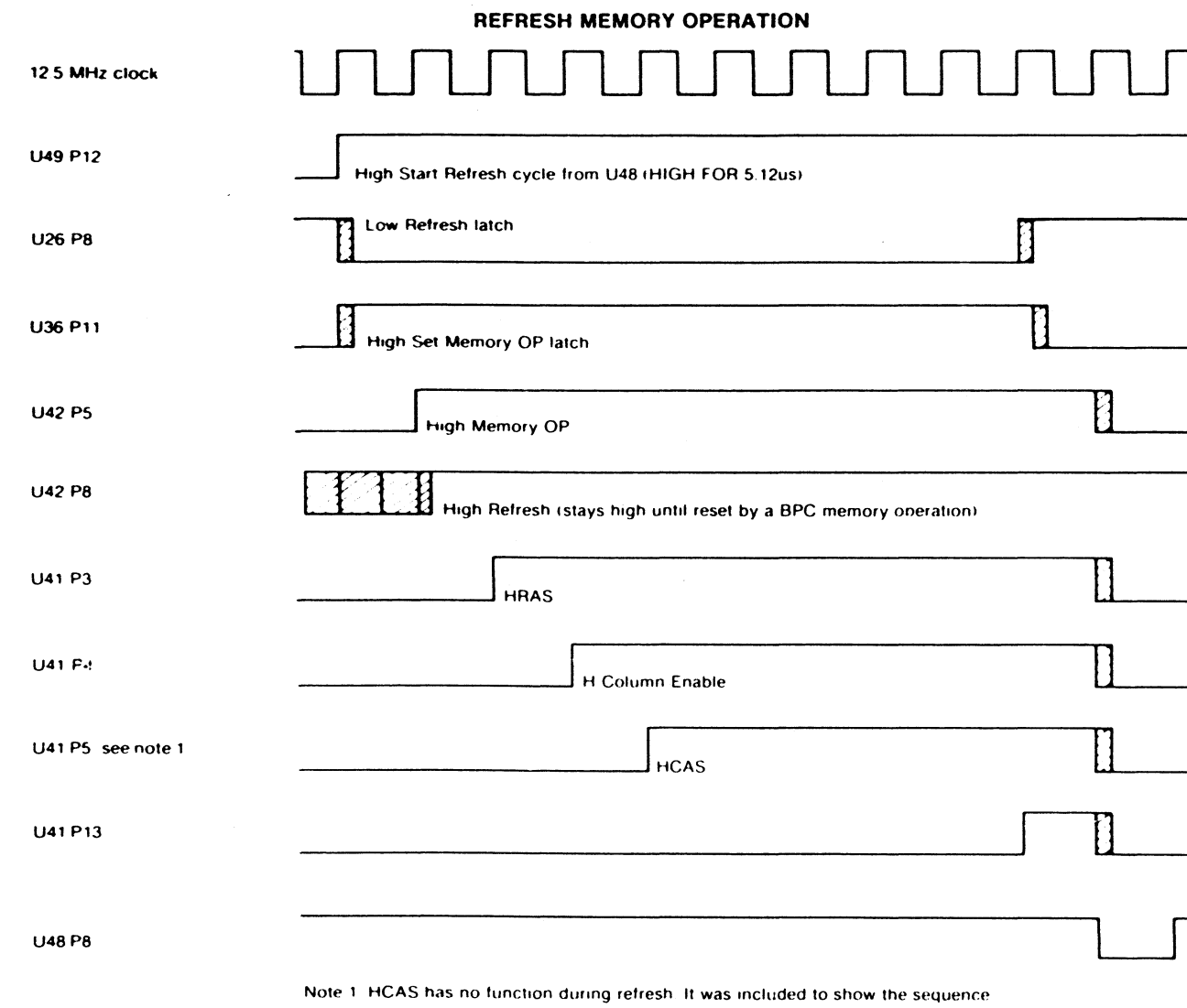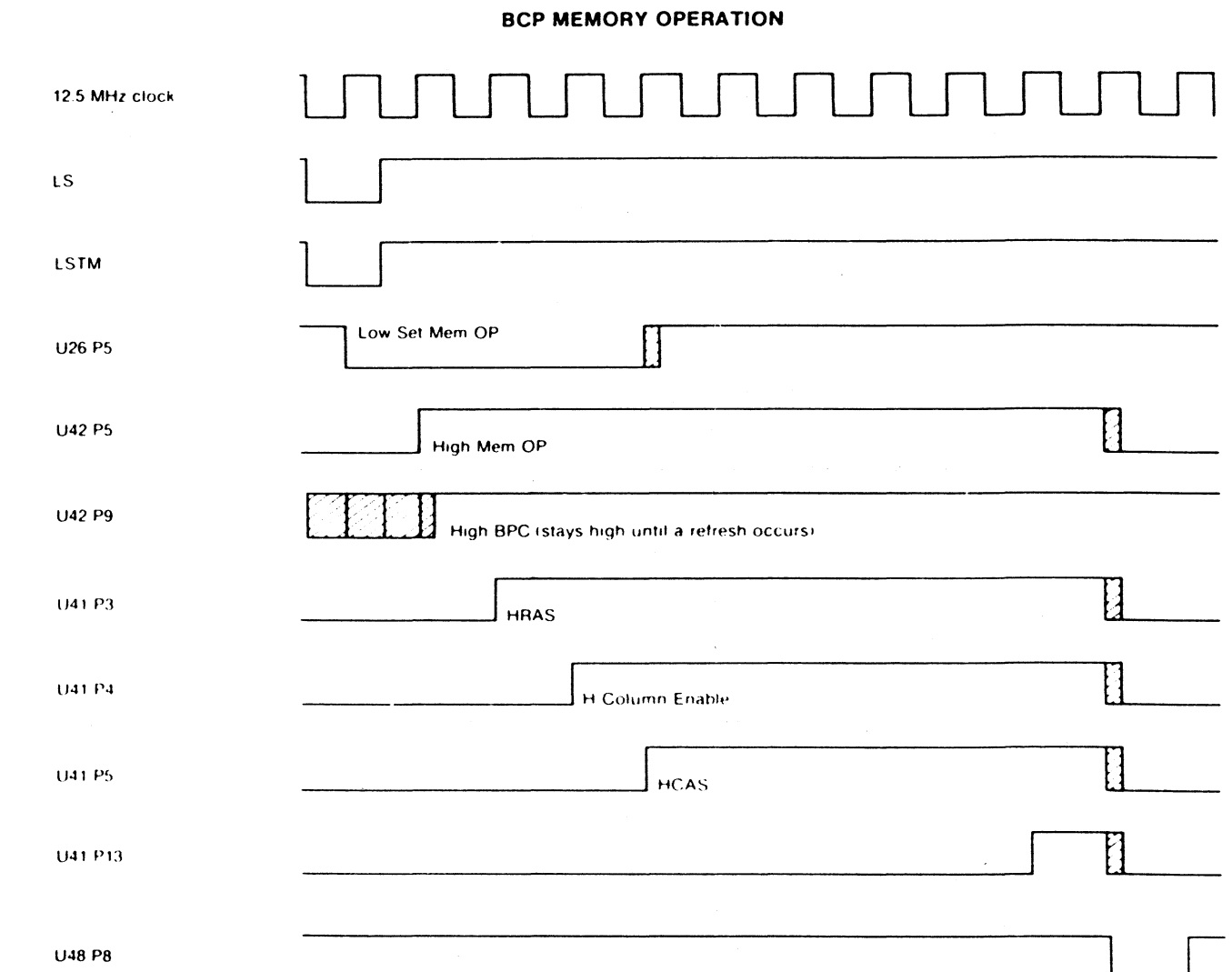
U41 P5 — HCAS

U41 P13

U48 P8

Figure 8-5. Refresh Memory Operation Timing

Figure 8-6. BPC Memory Operation Timing