HP 3000 SERIES II
COMPUTER SYSTEM
MANUAL OF STAND-ALONE DIAGNOSTICS

STAND-ALONE HP 30055A
SYNCHRONOUS LINE CONTROLLER
DIAGNOSTIC

Diagnostic No. D434A

HEWLETT **hp** *PACKARD*

TABLE OF CONTENTS

TABLES

1. INTRODUCTION

This HP 3000 Series II Computer System stand-alone diagnostic serves to verify the operation of the HP 30055A Synchronous Single Line Controller (SSLC).

It consists of eight test sections. Test sections one through six provide a fairly complete test of the SSLC board. In these test sections the output from the SSLC is connected to the input through test connector, HP 30055-60009 which must be installed at the end of the interface cable. Test sections seven and eight are complementary tests, providing operation between two SSLC boards installed in two separate HP 3000 computers. To run test section seven in one computer, the computer at the other end should run test section eight and vice versa. (The connection between the two SSLC's could be through two modems and possibly through telephone lines between the modems.

2. SIMPLIFIED OPERATING INSTRUCTIONS

The procedure to run the first six test sections with preset configuration is covered in this section. For detailed operating instructions see section 4 of this manual.

1. For running the first six test sections the interface cable should be terminated by HP 30055-60009 test connector.

2. Cold load diagnostic D434A from the stand-alone diagnostic tape. Hit "carriage return" on console. Title message will be printed and then a message instructing the operator to enter switch register options.

3. Program halts (HALT 6). Set bit 0 of the operating panel switch register OFF to run the pre-configured version of the diagnostic. To change the DRT # of the SSLC, set bits 0 and 1 of the operating panel switch register ON. A message will appear on the console requesting the new DRT # after the RUN switch has been pressed. Press RUN.

4. The program will start to execute. If the SSLC is error free, it will print "End of Section" message upon completion of each test section and "End of Pass" after the completion of all six test sections.

    In case of hardware error, error messages will be printed. For further explanation of the error messages see Table 3.

    Preset configuration

DB+0	Switch register	0
DB+1	Section Select Options	%177000 1,2,3,4,5,6
DB+2	Version Update	
DB+3	Device Number	
DB+4	Max Error Number	200
DB+5	Clock DRT	3

3. DETAILED DESCRIPTION

The diagnostic is divided into eight test sections. Each test
section tests one or more functions of the controller. Each functional
test consists of one or more steps. A step is the minimum sequence of
instructions that may be looped by setting switch 11. Steps may con-
sist of a number of minor operations, such as I/O instructions, which
could possibly generate errors. These minor operations, or substeps,
may not be looped individually. If an error does occur in a substep,
setting the loop flag will not initiate a loop until the end of the
step is reached. In most cases, however, any minor operation will have
been exclusively tested in a previous step where it may be looped
individually (since it is the only operation within that step). The
sections of the diagnostic are described in detail below.

3.1 TEST SECTION 1

This section tests the response to I/O commands (CIO,TIO,RIO,WIO,SIO) and makes initial status check. Tests the ability to set the interrupt flip-flop with the SIN instruction. Tests the ability to enable and disable interrupts originating from the interface board. Also tests the function of programmed I/O Reset and interrupt reset.

Step No.	Function
50	Test condition code for equal after CIO
51	Test condition code for equal after TIO
52	Test condition code for equal after WIO
53	Test condition code for equal after RIO
54	Test condition code for equal after SIO
55	Test ability to enable interrupt with control word %121000
56	Test function of SIN instruction
57	Test ability to disable interrupts with control word %120000
58	Tests function of I/O control word %100000 (I/O RESET) to set status lines to initial state
59	Tests ability to set interrupt - pending status bit
60	Tests ability of control word %122000 (interrupt reset) to reset interrupt - pending status bit

3.2 TEST SECTION 2

This section tests the control and device status lines, and ability of status lines S0-S3 to cause an external interrupt.

Step No.	Function
75	Tests ability to set and reset control and status lines.
76	Tests ability of status lines S0-S3 to cause interrupts when enabled and state is changed from 0 to 1.
77	Tests ability of status lines S0-S3 to cause interrupts when enabled and state is changed from 1 to 0.
78	Tests inability of status lines S0-S3 to cause interrupts when disabled and state is changed from 0 to 1.
79	Tests inability of status lines S0-S3 to cause interrupts when disabled and state is changed from 1 to 0.

3.3 TEST SECTION 3

Transmits and receives a block of data using direct write, SIO read, then SIO write, direct read. Tests ability to interrupt upon transmit and receive. Checks ability to blind receiver and to disable transmitter. Overrun status bit, overrun interrupt, and programmed receiver reset are also checked.

Step No.	Function
100	Tests direct write, SIO read with character length = 8 bits, BAUD-rate = 2400 BPS (bit/sec).
101	Same as step 100 except character length = 7 bits.
102	Same as step 100 except character length = 6 bits.
103	Same as step 100 except BAUD-rate = 4800 BPS.
104	Same as step 100 except BAUD-rate = 9600 BPS.
105	Tests SIO write, direct read with character length = 8 bits, BAUD-rate = 2400 BPS.
106	Tests ability of control word 034000_8 to blind the receiver.
107	Tests the ability of control word 032000_8 to disable transmitter.
108	Tests overrun interrupt.

3.4 TEST SECTION 4

Tests the parity circuitry including the capability to transmit and receive odd or even parity, to enable or disable parity error interrupts, and to set the parity error status bit upon detecting an error.

Step No.	Function
125	Tests odd parity generation for 128 8-bit (including parity bit) character.
126	Same as step 125 except tests even parity.
127	Tests odd parity generation for 64 7-bit (including parity bit) characters.
128	Same as step 127 except tests even parity.
129	Tests odd parity generation for 32 6-bit (including parity bit) characters.
130	Tests parity error interrupt.

3.5 TEST SECTION 5

Checks the unpacking capability of the transmit circuitry and the packing capability of the receiver circuitry. Checks status bit 6 (byte).

Step No.	Function
150	Tests ability of transmit circuitry to unpack 16-bit words into two 8-bit characters and transmit them correctly.
151	Tests ability of receive circuitry to correctly receive 8-bit characters and pack them two to a word.
152	Tests status bit 5 (byte).

3.6 TEST SECTION 6

Checks the associate character function. That is, the ability of
pre-selected characters to generate conditional jump, device end,
and interrupt signals, and to disable service request upon reception.

Step No.	Function
175	Tests ability of associate character circuitry to store a character and to generate a JUMP signed upon receiving an identical character.
176	Same as step 175 except tests ability to generate a DEVICE END signal.
177	Same as step 175 except tests ability to generate an INTERRUPT signal.
178	Same as step 175 except tests ability to generate a DISABLE SERVICE REQUEST signal.
179	Checks that the associated memory addresses are decoded correctly by loading all memory cells with a valid function and insuring that each address executes its function correctly.

3.7 TEST SECTION 7 & 8

These two test sections are complementary to each other. They should run in a 2 computer configuration both of which contains a SSLC interface.

The interfaces are linked together through modems which transmit and receive over telephone lines. To run this test, Section 7 is selected and run on one computer, while Section 8 is selected and run simultaneously on the other computer. Section 8 will unpack and transmit 256 characters through the modem and over telephone lines to the other modem, and finally to the interface in the other computer, which is running Section 7 of the diagnostic. After data has been received, it is transmitted back to the first computer. Received data is checked for errors at both computers. Explicit instructions for executing this test are found in the operating instructions section of this document.

TEST SECTION 7

An SIO program is executed which receives 256 characters (transmitted by another board running under Test Section 8), and packs them into a buffer. The same buffer is then unpacked and transmitted to the other board. Then the input buffer is checked for errors.

Step No.	Function
200	Receives and packs 256 characters, then unpacks and transmits them. Checks for receive errors.

TEST SECTION 8

An SIO program is executed which transmits 256 characters to another board running under Test Section 7. It then receives the same data (transmitted by the other board) and packs it into a buffer. The buffer is then checked for errors.

Step No.	Function
225	Unpacks and transmits 256 characters, then receives and packs them. Checks for receive errors.

4. OPERATING INSTRUCTIONS

1. For running test sections 1 through 6 install test connector
   HP 30055-60009 on the end of the device cable. For running test
   sections 7 & 8 between the two computers the two computers must
   be linked through modems.

2. Cold-load diagnostic D434A from stand-alone diagnostic tape.
   When the loading is completed hit "carriage return" on the
   console. Title message will be printed followed by a message
   instructing the operator to make switch register option selection.

3. Program halts (HALT 6) for switch register selection. The options
   should be entered through the operating panel switch register.
   Options are given in Table 1. To run diagnostic with preset con-
   figuration push RUN with bit 0 of the operating panel switch
   register set to OFF. The switch register options will be updated
   from the operating panel switch register if bit 0 is set ON. For
   changing the section select options, or the configuration data set
   bit 0 and 1 to ON before pushing RUN.

4. Message will be displayed on the terminal to enter section select
   options if bit 0 and 1 of the switch register were set to ON in
   step 3. Program halts (HALT 5) for entering section select options.
   Use bits 1-8 of the operating panel switch register to select the
   corresponding test sections. Bit 0 set to ON calls for "reconfigur-
   ation". It is done through the console. Questions Q26, Q27 and
   Q28 will be displayed. After each question, the correct answer
   should be typed. Upon completion of the reconfiguration, the
   program returns to step 3 (of this Operating Instructions).

5. Program starts to execute the selected sections. Errors will be
   indicated by Error Messages and/or error halts.

6. Operating Instructions for Special Test Sections (Sections 7 & 8).

   a. Prior to running the test, communications (normally a phone call)
      should be established between the two operators in order to syn-
      chronize their operations and to decide which operator is to run
      Section 7, and which is to run Section 8. Each operator should
      select his section exclusively. That is, the operator running
      Section 7 should select only that section, and the other operator

should have only Section 8 selected. Each operator should
also select option switch 15 (pause at end of cycle).

b. The operator running Section 8 places his data set into
"automatic answer", then starts the diagnostic by pushing
RUN.

c. The operator running Section 7 starts his diagnostic running
and then places a data call to the other data set. (He has
approximately 2 minutes to do this starting from the time the
other operator starts his diagnostic). Upon receiving a
carrier tone, he places his data set in "data" mode before the
tone stops.

d. The test should complete within 20 seconds from the placing of
the data call. If an error in operating procedure is made, the
test may be aborted from its two minute wait loop by the section
select procedure.

e. The diagnostic will print the end-of-pass message and halt. The
test may be repeated by hanging up the data phones, then starting
with step 6.

TABLE 1
Switch Register Options

Bit	Function If Set
0	Update Switch Register
1	Section Selection
2	
3	
4	
5	
6	
7	Use Line Printer
8	
9	Suppress Non-Error Messages
10	Suppress Error Messages
11	Loop on step
12	Halt on Error
13	Halt after Step
14	Halt after Section
15	Halt after complete test cycle

TABLE 2

Halt Codes

Halt Code %

0	
1	
2	
3	
4	
5	Enter Section Select Options
6	Enter Switch Register Options
7	
10	
11	
12	Error Halt
13	End of Step or End of Section
14	
15	End of Test Cycle
16	
17	Max Error # Reached

TABLE 3
Diagnostic Messages

30055A SYNC SINGLE LINE CTLR TEST (D434A.00.0)

P10 ENTER SWITCH REG. OPTIONS	Enter switch register options through panel switch register.
P11 ENTER SECTION SEL OPTIONS	Enter section select options through panel switch register.
Q26 DECIMAL DRT OF INTERFACE=	Type DRT of SSLC on console.
Q27 DECIMAL DRT OF CLOCK=	Type DRT of clock on console.
Q23 MAX ERROR #=	Type desired error limit. Type 0 for no limit.
E55 ENABLE INTPT FAILED	Control word 121000_8 failed to enable interrupts.
E57 DISABLE INTPT FAILED	Control word 120000_8 failed to disable interrupts.
E76 NO INTPT WHEN STATUS LINE Si SET	Status line Si should cause interrupt when reset, then enabled and set.
E77 NO INTPT WHEN STATUS LINE Si RESET	Status line Si should cause interrupt when set, then enabled and reset.
E78 UNESPECTED INTPT WHEN STATUS LINE Si SET	Status line Si should not cause interrupt when disabled, then set.
E79 UNESPECTED INTPT WHEN STATUS LINE Si RESET	Status line Si should not cause interrupt when disabled, then reset.
E106 BLIND-RCVR FAILED	Control word 034000_8 did not disable the receiver section.
E107 DISABLE-XMIT FAILED	Control word 032000_8 did not disable the transmitter section.
E150 UNPACK ERR. DATA IS xxxxxx, SHOULD BE xxxxxx	Data was not unpacked and transmitted correctly.
E151 PACK ERR. DATA IS xxxxxx, SHOULD BE xxxxxx	Data was not received and packed correctly.
E175 ASSOC CHARx=xxxxxx DID NOT CAUSE JUMP	JUMP signal should have been generated.
E176 ASSOC CHARx=xxxxxx DID NOT CAUSE DEV END	DEVICE END signal should have been generated.
E177 ASSOC CHARx=xxxxxx DID NOT CAUSE INTP	INTERRUPT signal should have been generated.
E178 ASSOC CHARx=xxxxxx DID NOT CAUSE DISABLE SR	DISABLE SERVICE REQUEST should have been generated.

TABLE 3 (Cont.)
Diagnostic Messages

30055A SYNC SINGLE LINE CTLR TEST (D434A.00.0)

E300 NO RESPONSE TO TIO IN STEP XXX   Condition code = CCL after TIO instruction in Step Number XXX.

E301 NO RESPONSE TO CIO IN STEP XXX   Condition code = CCL after CIO instruction in Step Number XXX.

E302 NO RESPONSE TO WIO IN STEP XXX   Condition code = CCL after WIO instruction in Step Number XXX.

E303 NOT READY FOR WIO IN STEP XXX   Condition code = CCG after WIO instruction in Step Number XXX.

E304 NO RESPONSE TO RIO IN STEP XXX   Condition code = CCL after RIO instruction in Step Number XXX.

E305 NOT READY FOR RIO IN STEP XXX   Condition code = CCG after RIO instruction in Step Number XXX.

E306 NO RESPONSE TO SIO IN STEP XXX   Condition code = CCL after SIO instruction in Step Number XXX.

E307 NOT READY FOR SIO IN STEP XXX   Condition code = CCG after SIO instruction in Step Number XXX.

E308 NO RESPONSE TO SIN IN STEP XXX   Condition code = CCL after SIN instruction in Step Number XXX.

E325 NO INTPT IN STEP XXX

E326 UNEXPECTED INTPT IN STEP XXX

E327 DATA ERR IN STEP XXX
     DATA IS xxxxxx,
     SHOULD BE xxxxxx

E328 STATUS ERR IN STEP XXX   Status Error. A "D" in any
     STATUS IS x xxx xxx xxx xxx xxx   position indicates a "don't
     SHOULD BE x xxx xxx xxx xxx xxx   care" bit.

P340 PAUSED AT STEP XX   Push RUN to restart.

D345 END OF SECTION X

P346 PAUSES AFTER SECTION X   Push RUN to restart.

D350 END OF PASS XXX