HP 3000 SERIES II
COMPUTER SYSTEM
MANUAL OF STAND-ALONE DIAGNOSTICS

STAND-ALONE HP 30036A
MULTIPLEXER CHANNEL DIAGNOSTIC

Diagnostic No. D422A

HEWLETT hp PACKARD

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I. INTRODUCTION

The Stand-Alone HP 300036A Multiplexer Channel Test verifies the functional level operation of the Multiplexer Channel Board. The tested area includes Order RAM, Order Register, Address RAM, Address Register, State RAM, State Register, and the SIO related to the multiplexer. A detailed description of the test is available in the subsequent sections.

II. MINI-OPERATING INSTRUCTIONS

A. Operations

1. Cold Load Diagnostic File # (associated with D422A) from non-cpu Cold Load Tape.
2. Respond to Speed-Sense by asserting "CR" at the Console.
3. Respond to the dialogue at the Console.

B. Switch-Register Options

-SWITCH-	-FUNCTION IF SET-
0	SELECT EXTERNAL SWITCH REGISTER
1	SET TO CHANGE SECTION SELECTION REGISTER
2	SET TO BYPASS SECTION (AREG)
3	SET TO BYPASS SECTION (OREG)
4	SET TO BYPASS SIOTEST SECTION (STEPS 63 AND 68)
5	LOOP CURRENT SECTION
6	SET TO BYPASS SIOTEST (STEPS 75 THRU 78)
7	OUTPUT TO LINE PRINTER (IF CONFIGURED IN SDUP)
8	SPARE
9	SUPPRESS NON ERROR MESSAGES
10	SUPPRESS ERROR MESSAGES
11	LOOP ON LAST STEP
12	HALT ON ERROR
13	HALT AT END OF STEP
14	HALT AT END OF SECTION
15	HALT AFTER A COMPLETE PROGRAM CYCLE

C. Section Switch - Register Options

BIT #	SECTION
0	RE-CONFIGURE
1	IORES
2	ARADDR
3	ARDATA
4	ARCPP
5	ORADDR
6	ORDATA
7	ORCP
8	AREG
9	OREG
10	NSGP1
11	NSGP2
12	NSGP3
13	NSGP4
14	STPAR
15	SIOTEST

D. HALT ASSIGNMENTS

NO. (OCTAL)	FUNCTION
0	HALT FOR EXTERNAL SWITCH REG.
1	HALT FOR SECTION SWITCH REG.
2	HALT TO RESTORE EXTERNAL SW. REG.
3	HALT ON ERROR COUNT REACHED
4-10	SPARE
11	ABNORMAL INTERRUPT
12	HALT ON ERROR
13	HALT AFTER STEP
14	HALT AFTER SECTION
15	HALT AFTER COMPLETE PROGRAM CYCLE
16	SPARE
17	SPARE

III. REQUIREMENTS

A. Hardware

The hardware required to run the Multiplexer Channel Diagnostic is the minimum HP 3000 Series II Computer System with the addition of up to two Selector Channel Maintenance Boards.

- HP 30000A Central Processor Unit (CPU)
- HP 30005A Memory Module Control Unit
- HP 30006A Semi-Conductor Memory Module (2 Mods - 64K)
- HP 30031A System Clock/Console Interface Card
- HP 30036A Multiplexer Channel
- HP 30003-60013 Control Panel
- One System Console Device
- One Magnetic Tape Subsystem
- One Moving-Head Disc Subsystem (not used by this test).
- One (1) 30033A-90002 Selector Channel Maintenance PCA.
- One (1) Additional 30033A-90002 Selector Channel Maintenance PCA. (Optional) for checking Multi-Device Capability. (Set Switch Register switch 6 to bypass steps 75 through 78 if this board is not installed.)

B. Software

The Stand-Alone Diagnostic Utility Program (SDUP) is required to create the Stand-Alone Diagnostic Tape. This cold-loadable tape is comprised of cold load program, the Relocating Loader, and one or more diagnostic programs including the Stand-Alone HP 30036A Multiplexer Channel Test. All the programs are coded in System Programming Language (SPL/3000). For more detailed description of usage of SDUP, see System Diagnostic Utility Program Manual (03000-90125 for model 5 and 7).

IV. DETAILED OPERATING INSTRUCTIONS

A. Operating Instructions

The following are the instructions for loading, executing, and configuring the Stand-Alone HP 30036A Multiplexer Channel Test:

1. Cold Load by entering %3006 into the 30003-60013 Control Panel and simultaneously depress "LOAD" and "ENABLE" switches on the 30003-60013 control panel.

2. Select an appropriate Diagnostic File # (associated with the Multiplexer Channel Diagnostic) and enter the number via the Switch-Register. The Cold-Loadable diagnostic tape supplied is identified by file names and their respective position (File #) on the tape.

3. Depress "RUN" switch on the 30003-60013 Control Panel. The selected program is, now, loaded into the memory. The tape rewinds at the end of the program load.

4. The Multiplexer Channel Diagnostic program is now executable.

5. Depress "RETURN" key on the console to respond to the Speed-Sense. Upon completion of the previous operation the program prints the diagnostic header information and then requests necessary parameters to begin the diagnostic program execution cycle.

B. Options

Under Stand-Alone HP 30036A Multiplexer Channel Test, the operator can control the test sections to be executed; control halts after sections or steps or upon program completion; control suppression of error and non-error messages; and control loop on a specific test step or a section. These control options may be selected when the program requests for a specific option entry via the console during program execution.

1. The following describes the options associated with each bit of the Switch-Register for a program request of an option entry of the following form:

   "Q01 SELECT OPTIONS"
   (Same options as those described in Section II.B) Description of the usage of bits (Ø and 1) under this Option is as follows:

Bit #Ø	Bit #1	Function
Ø	Ø	Uses previously configured values.
Ø	1	Uses previously configured values.
1	Ø	The program uses whatever options currently selected on the Switch-Register of the Control Panel or it will use whatever options entered for a request under a message: "PØ5 RESTORE SELECT OPTIONS".
1	1	If this option is selected, it suggests possible re-configuration (see bit Ø of Section IV.B.2)

2. The following describes the options associated with each bit of the Section Select Switch Register for the program request for a following message format:

   "Q02 SELECT SECTION OPTIONS"
   (Same options as those described in Section II.C)

   If bit Ø is not selected (Ø), the program requests to restore the External Switch-Register Option and continue execution using previously configured values.

2. Continued

If bit Ø is selected (1), the program requests restoration of External Switch-Register Options, requests Multiplexer Channel Device # (must be decimal and 3 ≤ Dev # ≤ 127), and requests maximum error count (must be decimal and 0 ≤ Max. Error Count ≤ 9999). Furthermore, if bit 15 is selected (1) at the same time, an additional information is requested to execute SIOTEST Section. The information requested is; device # for the 1st Selector Channel Maintenance Board, device # for the 2nd Selector Channel Maintanance Board (if any), device # for the Clock/Console, upper Bank #, and the upper address for the specified Bank #. A detailed description regarding SIOTEST Section is available in Subsequent Section.

C. Halts and Message Tables

1. Halt Assignments
When a program halts, an instruction is displayed in the Current Instruction Register (CIR) of the 3ØØØ3-6ØØ13 Control Panel. The register is displayed as (Ø ØØ1 ØØØ ØØ1 11X XXX: where X's is the Halt #).

See Halt Assignment Table as described in Section II.D.

2. Message Formats
There are basically four types of message classfications: D,E,P and Q classes.

D-class
Messages which describe program boundaries. Some operator intervention is necessary.

E-class
Messages related to error or step number. Some operator intervention is necessary.

P-class
Messages which describe the test completion of a Section or step or an indication for a certain tested properties. Some operator intervention is necessary.

Q-class
Inquiry messages by the program for the parameter entry. Operator intervention is required.

2.1 Message Descriptor

2.1.1 DØ 30036A MPX CHANNEL TEST (HP D422X.YY.ZZ)

:This is the header information for this diagnostic program; where

X=Version number

YY=Update number
ZZ Fix number

2.1.2 D02 END MPX CHAN TEST
:This Message indicates that the program has completed one test cycle for those test sections selected.

2.1.3 D03 END: PROGRAM CYCLE: PASS=XXXX
:This message indicates the number of test passes which the program has completed for those test sections selected.

2.1.4 Q01 SELECT OPTIONS
:The program is requesting any of the option entry available and described in Section II.B.

The options available in Section II.B is very much self-explanatory with the exception of option for bits 2, 3, 4 and 6. The exception is defined as follows:

Bit	Definition
2	Set to bypass AREG Section. :Allows option to bypass Address Register test which is somewhat lengthy in test time.
3	Set to bypass OREG Section :Allows option to bypass Oder Register test which is somewhat lengthy in test time.
4	Set to bypass SIOTEST Section (Steps 63 and 68). :Allows Option to bypass the data transfer time measurement under Fast Mode for Step 63 (Read Mode - 2K transfer) and Step 68 (Write Mode - 2K transfer).
6	Set to bypass SIOTEST Section (Steps 75 thru 78) :Allows option to bypass multiple device controller access test (two Selector Channel Maintenance Boards).

2.1.5 Q02 SELECT SECTION OPTIONS
:This message indicates that the program is requesting any of the option entries available and described in Section II.C

2.1.6 Q03 RESTORE SELECT OPTIONS
:This message indicates that the program is requesting any of the option entries available and described in Section II.B.

2.1.7 Q04 ENTER MPX DEVICE # =
:This message indicates that the program is requesting the Multiplexer device number as configured currently in the system. The device number is specified in decimal and its range is: ($3 \leq$ DEVICE ≤ 127). Programmed pre-defined value is 4.

2.1.8 Q05 ENTER MAXIMUM ERROR COUNT #=
:This message indicates that the program is requesting the maximum error count number. The number is specified in decimal and its range is: (0 ≤ COUNT ≤ 9999).
The programmed pre-defined value is 999 (10).

2.1.9 Q06 ENTER SEL. CHAN. MAINTENANCE BOARD DRT #=
:This message is requesting the device number (decimal) for the currently installed Selector Channel Maintenance Board. The device number's range is: (3 ≤ DEVICE # ≤ 127).

NOTE: Sections IV. C. 2.1.9 thru IV. C. 2.1.13 are dialogue for the SIOTEST Section.

NOTE: If two Selector Channel Maintenance Boards are currently installed on the Multiplexer Channel SIO Bus then insure that the device numbers are configured correctly and they are not the same.

The programmed pre-defined value is 0.

2.1.10 Q07 ENTER 2ND SCMB DRT#=
: This message requests the device number of the second Selector Channel Maintenance Board (if two (2) SCMB's are currently installed). The device # must differ from the one specified in Section IV.C. 2.1.9. The device # is specified in decimal and its range is:
(3 ≤ DEVICE ≤ 127).

2.1.11 Q08 ENTER CLOCK/CONSOLE DRT #=
: This message requests the device # (in decimal) of the Clock/Console which is currently installed in the system. The device # range is:
(3 ≤ DEVICE # ≤ 127).
The programmed pre-defined value is 3.

2.1.12 Q09 ENTER UPPER BANK #
:This message requests the highest bank # (decimal) for the memory configured currently. The range is: (0 ≤ BANK # ≤ 3).

2.1.13 Q10 ENTER UPPER ADDRESS (OCTAL) =
:This message is requesting the highest address (octal) that is addressable for the memory bank specified in Section IV.C.2.1.12.

NOTE: With the selection of SIOTEST Section, the Multiplexer Channel Diagnostic is capable of being executed only in the following memory configuration:

Memory Size (wds)	(Equivalent) Bank#	Address
64K	0	%177777
96K	1	%077777
128K	1	%177777
160K	2	%077777
192K	2	%177777
224K	3	%077777
256K	3	%177777

2.1.14 PØ2 END SECTION XXXXXX
:This message indicates the section number which has just been completed.

2.1.15 PØ3 END STEP XXX
: This message indicates the step number which has just been completed.

2.1.16 PØ6: MAX. ERROR COUNT REACHED
:This message indicates that the error count which has been either entered or predefined has been reached.

2.1.17 P11 IF SEL. CHAN. MAINTENANCE BOARD ALREADY IN HIT *CR*
P11 OTHERWISE INSERT BOARD, CONNECT POLLS, AND RE-COLD LOAD.
:This message indicates that if no SCMB is currently installed then installation is required. Otherwise depress Carriage Return Key on the console to continue the test.

2.1.18 P15 END SIO TEST CONFIGURATION
:This message indicates that the all the parameters necessary to execute SIOTEST Section have been entered. The test execution resumes and no other messages are expected until either the occurrence of test completion or error or any other events which might be controlled by the current External Switch Register.

2.1.19 P16 FAST SR READ MODE (2K XFER); TIME=X MSEC; BANKYY; STEP 63
:This message is resulted from step 63 (if External Switch Register Option bit #4 is not on (Ø)). The 2K read data transfer time (X) in millisecond (unit) is measured under Fast Service Request Mode for each existing memory Bank YY in the system.

2.1.20 P17 FAST SR WRITE MODE (2K XFER); TIME=X MSEC; BANKYY; STEP 68
:This message is resulted from step 68 (if External Switch Register Option bit #4 is not on (Ø)). The 2K write data transfer time (X) in millisecond (unit) is measured under Fast Service Request Mode for each existing memory Bank YY in the system.

2.1.21 P18 1ST SCMB DRT# NOT ENTERED; STEPS 41-74 ABORTED
:This message indicates that the Multiplexer Channel Diagnostic program was not preconfigured under SDUP or an attempt was made to execute SIOTEST Section without first configuring the device #. The SIO test using a single SCMB in SIOTEST Section is aborted.

2.1.22 P19 2ND SCMB DRT# NOT ENTERED; STEPS 75-78 ABORTED
:This message indicates that the Multiplexer Channel Diagnostic program was not preconfigured or an attempt was made to execute SIO test using two SCMB without first configuring the device #.

To cite an example, begin configuring with External Switch Register bit #6 on (1) and without further reconfiguration attempt was later made to execute multiple SCMB SIO test in SIOTEST Section by resetting bit #6 (Ø) of the External Switch Register.

2.1.23 Exxx
:This message indicates the appropriate error number associated with the type of error. See Section IV.C.3 for detailed error messages.

2.1.24 Exxx:
:This message is an error indicator where XXX is the step number. This error indicator always precedes the following type of Messages:

2.1.24.1 STATUS=X XXX XXX XXX XXX XXX
:This message displays the actual device status appropriate to the test.

2.1.24.2 SHOULD=X XXX XXX XXX XXX XXX
:This message displays the expected value.

2.1.24.3 TIX CT=X XXX XXX XXX XXX XXX (Toggle In Count)

2.1.24.4 EOT CT=X XXX XXX XXX XXX XXX (End of Xfer Count)

2.1.24.5 RNW CT=X XXX XXX XXX XXX XXX (Read Next Word Count)

2.1.24.6 DATA =X XXX XXX XXX XXX XXX (Actual Data)

2.1.24.7 RD STB=X XXX XXX XXX XXX XXX (P RD STB Count)

2.1.24.8 RT RES=X XXX XXX XXX XXX XXX (Actual Return Residue)

2.1.24.9 WR STB=X XXX XXX XXX XXX XXX (P RW STB Count)

3.0 Type Exxx Error Messages and Fault Description

The Exxx type of error messages are individually defined as follows:

IORES	EØ5 I/O RESET DID NOT RESET EOT FF	I/O Reset command did not properly reset EOT flip-flop.
ARADDR	E07 A-RAM ADDR ERR OUT = xx IN = xx	The decimal select code, OUT, stored in the corresponding "Address RAM" location did not equal the value IN, that was retrieved from it.
ARDATA	E08 A-RAM(sc) DATA ERR OUT = xxxxxx IN = xxxxxx	The data pattern OUT, stored in an "Address RAM" location, sc (for select code), did not equal the value IN, read back from it.
ARCPP	E09 A-RAM RESTORE ERR GOOD = xxxxxx BAD = xxxxxx	Data read from the "Address RAM" to register, GOOD, was not properly restored to RAM from register. Data read was equal to BAD instead.
ARCPP	E10 A-RAM PARITY ERR DATA = XXXXXX	Parity error circuitry detected even parity while restoring register data to "Address RAM". Should be odd parity.
ORADDR	E11 O-RAM ADDR ERR OUT = xx IN = xx	The decimal select code number, OUT, stored in the corresponding "Order RAM" location did not equal the value IN, read back.

3.0 Continued

Section	Message	Comments
ORDATA	E12 O-RAM (sc) DATA ERR OUT = xxxxxx IN = xxxxxx	The data pattern OUT, stored in the "Order RAM" location, sc (for select code), did not equal the value IN, retrieved from it.
ORCP	E13 O-RAM RESTORE ERR GOOD = xxxxxx BAD = xxxxxx	Data read from the "Order RAM" to register, GOOD, was not properly restored to RAM from register. Data read was equal to BAD instead.
AREG	E14 A-RAM REG IS xxxxxx, SHOULD BE xxxxxx	"Address RAM" register counting error during increment test.
OREG	E15 O-RAM REG IS xxxxxx, SHOULD BE xxxxxx	"Order RAM" register counting error during increment test.
NSGP1	E16 STATE FOR I/O order IS xxxx, SHOULD BE x	The next state (x = A, B, or C) for "I/O order" (CO = control, RR = return residue, JC = jump conditional, JU = jump unconditional, SE = sense, IN = interrupt) was incorrect. xxxx may contain A, B, C, D (or any combination), or 0 if no state.
NSGP2	E17 STATE FOR I/O order IS xxxx, SHOULD BE x	The next state (x = A or B) for "I/O order" (EN = end, EI = end/interrupt) was incorrect. xxxx may contain A, B, C, D (or any combination), or 0 if no state.
NSGP3	E18 NEXT STATE FOR I/O order IS xxxx, SHOULD BE x	The next state (A, B, C or D) for "I/O order" (RD = read, WR = write) was incorrect. xxxx may contain A, B, C, D (or any combination), or 0 if no state.
STPAR	E19 STATE PARITY IS x, SHOULD BE#	Parity circuitry generated even parity on state bits.
OREG	E20 EOT SET BEFORE ROLLOVER OREG = xxxxxx	EOT should not set until count in order RAM register exceeds 7777_8.
IORES, NSGP3 OREG	E21 EOT NOT SET IN STEP xx	EOT should be set when count in order RAM register exceeds 7777_8.
NSGP3	E22 EOT SET IN STEP xx	EOT was not reset by transition of state from B to D.
NSGP4	E23 STATE FOR I/O order IS XXXX, SHOULD BE X	The next state (A,D, or C) for "I/O order" (SB Set Bank) was incorrect. xxxx may contain A,D, or C (or any combination), or Ø if no state.

3.0 Continued

Section	Message	Comments
Any	E3Ø NO RESPONSE TO WIO; DRT# XXX; IN STEP	Condition Code = CCL XXX = Device #; YY = Step #
Any	E31 NOT RDY FOR WIO; DRT # XXX; IN STEP YY	Condition Code = CCG. XXX = Device #; YY = Step #
Any	E32 NO RESPONSE TO RIO; DRT # XXX STEP YY	Condition Code = CCL XX = Device #; YY = Step #
Any	E33 NOT RDY FOR RIO DRT # XXX IN STEP YY	Condition Code = CCG XXX= Device #; YY = Step #
Any	E34 NO RESPONSE TO CIO: DRT # XXX IN STEP YY	Condition Code = CCL XXX = Device #; YY = Step #
Any	E5Ø NO RESPONSE TO TIO; DRT # XXX IN STEP YY	Condition Code = CCL XXX = Device #; YY = Step #
NSGP1, NSGP2 NSGP3, NSGP4	E51 ILLEGAL STATE DETECTED IN SR (XX)	XX = Select Code
NSGP1, NSGP2 NSPG3, NSGP4	E52 BANK # SHOULD BE X; IS Y	X = Expected Bank # Y = Actual Bank #
NSGP1, NSGP2	E53 TC SHOULD BE XX: IS YY	XX= Expected Terminal count YY= Actual Terminal count (Ø or 1)
NSGP1, NSGP2 NSPG3, NSGP4	E54 EOT SHOULD BE XX; IS YY	XX= Expected EOT bit YY= Actual Parity bit (Ø or 1)
NSGP1, NSGP2 NSGP3, NSGP4	E55 ADDR PAR SHOULD BE XX; IS YY	XX= Expected Parity bit YY= Actual parity bit (Ø or 1)
NSGP1, NSGP2 NSGP3, NSGP4	E56 STATE PAR SHOULD BE XX; IS YY	XX= Expected State Parity bit (Ø or 1) YY= Actual State Parity bit (Ø or 1)

The following are the error messages from SIOTEST Section. They are listed by step numbers from where the error message is resulted.

Step #	Message	Comments
46	E36 NO INTERRUPT TO SIN; DRT# XXX IN STEP YY	XXX = Device # YY = Step #
46	E37 NO RESPONSE TO SIN, DRT # XXX IN STEP YY	XXX = Device # YY = Step #
Any	E38 NOT RDY FOR SIO; DRT # XXX IN STEP YY	Condition Code = CCG XXX = Device #; YY = Step #
47,51,52, 54,55	E4Ø NO END WITH INTERRUPT IN STEP XX	XX = Step #
Any	E41 CURRENT PTR = %XXXXXX IN STEP YY	XXXXXX = DRT pointer YY = Step #
Any	E42 SHOULD PTR = %XXXXXX IN STEP YY	XXXXXX = DRT pointer YY = Step #

3.0 Continued

Step #	Message	Comments
48	E43 UNEXPECTED INTERRUPT IN STEP XX	XX = Step #
49	E44 NO INTERRUPT FOR INTERRUPT ORDER IN STEP XX	XX = Step #
53	E45 JUMP CONDITIONAL ILLEGAL IN STEP XX	XX = Step #
59,61,64,69, 70	E46 END W/INTERRUPT STATUS ERROR FOR BANK XX IN STEP YY	XX = Bank # YY = Step #
59	E47 DATA READ ERR: ADDR = % XXXXXX; BANK YY; STEP ZZ	XXXXXX = Address YY = Bank # ZZ = Step #
60,69,70	E48 READ NEXT WORD COUNTER ERROR FOR BANK XX IN STEP YY	XX = Bank # YY = Step #
60,69,70	E49 PRD STB COUNTER ERR FOR BANK XX IN STEP YY	XX = Bank # YY = Step #
65,71	E58 PWR STB COUNT FAILED; BANK XX; STEP YY	XX = Bank # YY = Step #
65,71	E59 TOX COUNT FAILED; BANK XX; STEP YY	XX = Bank # YY = Step #
60	E60 TOGGLE IN XFER COUNT ERR FOR BANK XX IN STEP XX	XX = Bank # YY = Step #
60,65,69,70, 71	E61 EOT COUNT ERROR FOR BANK XX IN STEP YY	XX = Bank # YY = Step #
61	E62 FAST MODE DATA READ ERR FOR BANK XX IN STEP YY.	XX = Bank # YY = Step #
62	E63 FAST MODE RNW ERR: BANK XX IN STEP YY	XX = Bank # YY = Step #
62	E64 FAST MODE PRD STB COUNT ERR: BANK XX IN STEP YY	XX = Bank # YY = Step #
62	E65 FAST MODE XFER TOGGLE IN COUNT ERR: BANK XX IN STEP YY	XX = Bank # YY = Step #
62	E66 FAST MODE EOT COUNT ERR: BANK XX IN STEP YY	XX = Bank YY = Step #

3.0 Continued

Step #	Messsge	Comments
Any	E68 STATUS ERR FROM TIO; BANK XX; STEP YY	XX = Bank # YY = Step #
64	E69 SIO WRITE ORDER (1 WD) FAILED; BANK XX; STEP YY	XX = Bank # YY = Step #
59,64,69,71	E70 RETURN RESIDUE FAILED: BANK XX; STEP YY	XX = Bank # YY = Step #
75,76,77 78	E71 RETURN RESIDUE FAILED: DRT # XXX; BANK YY; STEP ZZ	XXX= Device # YY = Bank # ZZ = Step #
66	E8Ø DATA WR ERR: FAST MODE: BANK XX; STEP YY	XX = Bank # YY = Step #
67,72	E81 FAST MODE: PWR STB CNT FAILED; BANK XX; STEP YY	XX = Bank # YY = Step #
67,72	E82 FAST MODE: TOX COUNT FAILED; BANK XX; STEP YY	XX = Bank # YY = Step #
67,72	E83 FAST MODE: EOT COUNT FIALED; BANK XX; STEP YY	XX = Bank # YY = Step #
69	E84 UUU; DATA CAP ERR AT %XXX; BANK YY; STEP ZZ	UUU= RNW, EOT TIX PRD XXX= Location YY = Bank # ZZ = Step #
67,79	E85 ERR: STATUS RTN'D FOR 2ND END W/INT; BANKXX;	XX = Bank # YY = Step #
7Ø	E86 FAST MODE: UUU DATA GAP ERR AT %XXX; BANK YY; STEP ZZ	UUU= RNW,EOT PRD TIX XXX= Count YY = Bank # ZZ = Step #
60,62,69,70	E87 TIX COUNT ERR: ADDR = %XXXXXX; BANK YY; STEP ZZ	XXXXXX= Address YY = Bank # ZZ = Step #
71	E88 RETURN RESIDUE ERR: BANK XX; STEP YY	XX = Bank # YY = Step #
73	E89 XFER ERROR DETECTED: BANK XX; STEP YY	XX = Bank # YY = Step #
74	E90 XFER ERR UNDETECTED: BANK XX; STEP YY	XX = Bank # YY = Step #
75,76,77	E91 NO END WITH INTERRUPT FOR DRT # XXX: BANK YY, STEP ZZ	XXX= Device # YY = Bank # ZZ = Step #

3.0 Continued

Step #	Message	Comments
75,76,77	E92 END W/INT STATUS ERR: DRT# XXX: BANK YY; STEP ZZ	XXX= Device # YY = Bank # ZZ = Step #
75,77	E93 DATA READ ERR AT % XXXXXX: DRT # UUU; BANK YY; STEP ZZ	XXXXXX= Address UUU= Device # YY = Bank # ZZ = Step #
75,76,77	E94 DRT POINTER ERR FOR DRT # XXX: STEP YY	XXX= Device # YY = Step #
78	E95 NO END W/INT; FAST MODE; DRT # XXX; BANK YY; STEP ZZ	XXX= Device # YY = Bank # ZZ = Step #
78	E96 END W/INT STATUS ERR: FAST MODE; DRT # XXX; BANK YY; STEP ZZ	XXX= Device # YY = Bank # ZZ = Step #
78	E97 DRT POINTER ERR: FAST MODE; DRT # XXX; BANK YY; STEP XX	XXX= Device # YY = Bank # ZZ = Step #

D. Pre-Configuration Option

1. The HP 30036A Multiplexer Channel Diagnostic Program has been pre-configured to execute in best load and go configuration using the options available from Section II.B and II.C. The pre-configured values can be modified at the time when the Cold-Tape is being created under SDUP (System Diagnostic Utility Program).

2. The following are the DB Locations containing data that can be changed during pre-configuration using SDUP:

DB+0	Switch Register Setting
DB+1	Section Register Setting
DB+2	Version and Update Level
*DB+3	MUX DRT Number
DB+4	Maximum Error Print Count
**DB+5	SCMB #1 DRT#
**DB+6	SCMB #2 DRT#
DB+10	0 to 3 Maximum
DB+11	Address Memory Size Upper

* must be entered
** must be entered if installed

1.1

0	1	2 3 4 5	6	7	8	9	10	11 12 13 14 15
A		B	C	D	E	F	G	

A Programmed I/O Reset (Bit Ø = 1; Reset).

B Bits 2-5: Select Code from V/O(0-17).

C Bit 6: Select Address Ram and Register

D Bit 7: Selects Order Ram and Register.

E Bit 8: Select State Ram and Register.

F Bit 9: Load Register from Ram Enable.

G Bit 1Ø: Increment Register Enable.

1.2 Status Word Format (TIO)

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	1	0						0	0	0	0	0	0	0	0

Bit#	
0	SIO Not OK (always Ø)
1	Read/Write OK (always 1)
2	Always Ø
3	Error - illegal State detected
4-7	Select Code number which is associated with an error (Bit 3)
8-15	Always Ø

1.3 State Word Format (RIO)

0	1	2	3	4	5	6 7	8 9 10 11 12	13	14	15
Ø	Ø	Ø	Ø	Ø	Ø	A	B C	D	E	F

Field	Bit#	Function
A	6-7	Bank Ram (if Load = Ø, the current register)
B	8	TC=1 after a word count is exhausted.
C	(9-12)	State Ram
	9	State A
	1Ø	State B
	11	State C
	12	State D
D	13	EOT FF
E	14	Address Parity (Odd, total number of one's)
F	15	State Parity (1 equals an error)

1.4 State Word Format (WIO)

0	1	2 3 4 5	6	7	8	9	10	11	12	13	14 15
Ø	Ø	A	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	B

1.4 Continued

Field	Bit#	Function
A	(2-5)	State Ram
	2	State A
	3	State B
	4	State C
	5	State D
B	14-15	Bank Ram Content

2. HP 30033A Selector Channel Maintenance Board

2.1 Control Word Format

MR	RI	JM	IDE	TA	TS	CONTROL CODE		F	SDN	TTC	TNC	CLR IL	COUNT CODE		
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

Bit#

0 MASTER RESET - issues a programmed I/O reset which clears the maintenance card, including the control register and data buffer, and sends clear interface to the channel if the channel is active..

1 RESET INTERRUPT - clears the interrupt request flip flop.

2 JUMP MET - sets condition met for conditional jumps.

3 IMMEDIATE DEVICE END - forces device end at the beginning of any data transfer on the selector channel. No effect on the multiplexer channel.

4 TIMEOUT ACKNOWLEDGE - causes channel acknowledge to be inhibited following the current control order. Any subsequent channel service out will timeout. The selector channel will restore the DRT pointer, but no clear interface will occur. The maintenance card will remain busy until a direct master reset is issued. The multiplexer channel ignores this control bit.

5 TIMEOUT SERVICE REQUEST - inhibits device service request after the current control order. The selector channel will issue a clear interface, forcing an interrupt, and restore the DRT pointer. The multiplexer channel program will simply stop, and no interrupt will be issued.

6:7 CONTROL CODE - defines how SIO program control orders will be treated.

00 - Ignore IOCW, use IOAW as a control word (default).

01 - Load IOCW into data buffer only (the control register is unchanged).

10 - Load IOAW into data buffer only.

11 - Load IOCW, then IOAW into data buffer.

2.1 Continued

Bit#

8 FAST BIT - overrides normal data service request delay (5 μs → 200 KHz) to force continuous service requests in data transfers.

9 SPECIAL DEVICE NUMBER - specifies that the maintenance card, when asked to supply its device number, will gate out bits 8:15 of its data buffer, allowing the card to simulate any device number in running SIO programs. Interrupts and direct commands will continue to correspond to the hardwired device number.

10 TERMINATE ON TERMINAL COUNT - specifies that counter rollover will terminate the current data transfer by device end (selector channel only) or clear interface (both) depending on bit 12.

11 TERMINATE ON NO COMPARE - enables a comparator and disables counter/buffer loading by programmed write strobes. Data sent to the card is compared with the current buffer contents, and a compare failure will terminate the transfer by device end (selector channel only) or clear interface (both) depending on bit 12.

12 CLEAR INTERFACE - specifies that a clear interface, rather than the default device end, should be issued if either or both of the above termination tests is met.

13:15 COUNT CODE - controls the counter/buffer. The normal mode is NOP, i.e., no count, buffer operation only. Codes are as follows:

000	NOP	100	P WR STB
001	READ NEXT WORD	101	TOGGLE OUT XFER
010	P RD STB	110	EOT
011	TOGGLE IN XFER	111	CHANNEL SO

Octal codes 1 to 7 specify that the counter will be incremented by the occurrence of the selected signal. Codes 4 to 7 inhibit loading of the counter/buffer to preserve the count. Code 7 (count channel service out) should not be issued by an SIO control order since there is a timing ambiguity as to whether the current cycle itself should be counted.

2.2 Status Word Format

SIO OK	R/W OK	INT REQ	INT ACT	XFER ERR	ENB	DEV END	EOT	NC	TC	INX	OUTX	CLR IL	0
0	1	2	3	4	5	6	7	8	9	10	11	12	13 14 15

The status word is returned by a direct TIO or by a P SENSE STB. Reading status does not in itself change any of the test board states. As indicated below, certain transfer related status bits are cleared by direct SIO or channel directives to begin a new transfer.

2.2 Continued

Bit#

0 SIO OK - True if the channel is inactive and the test board is not currently executing an SIO program.

1 READ/WRITE OK - Always true.

2 INTERRUPT REQUEST - True if the test board is currently interrupt requesting for any reason.

3 INTERRUPT ACTIVE - True if the test board interrupt circuit is currently in the active state.

4 TRANSFER ERROR - True if the channel has sent transfer error to the test board. Cleared by the next SIO or reset.

5 ENABLE - True if the channel is inactive. This is a positive true version of the "ENABLE" signal from the channel.

6 DEVICE END - True if the test board has issued device end. This bit is cleared at the beginning of a new transfer, by SIO and by reset.

7 EOT - True if the channel has asserted EOT (end of transfer). Cleared by the beginning of a new transfer, by SIO and by reset.

8:9 NO COMPARE and TERMINAL COUNT flip flops - Set if the respective condition has occurred. Cleared by SIO, reset, or the beginning of a new transfer.

10:11 IN TRANSFER and OUT TRANSFER flip flops - Indicate the state of the bus logic flip flops, one of which will be set by the channel during data transfers (READ = INBOUND, WRITE = OUTBOUND).

12 CLEAR INTERFACE - Set if the test board has issued clear interface to the channel. Cleared by SIO or reset.

13:15 Currently unassigned (zero).

V. DETAILED TEST DESCRIPTION

The Stand-Alone HP 30036A Multiplexer Channel Diagnostic Program is composed of fifteen (15) test sections. The test description per section is given as follows:

1. Description by Sections

1.1 IORES — Tests the I/O Reset functions.

1.2 ARADDR — Stores address value of Address RAM (Random Access Memory) location into each RAM location. Then reads back contents to verify that the unique address value is in that location. The 30036A Multiplexed Channels has two RAM's: The "Address RAM" and the "Order RAM", each having 16 locations addressed 0 to 15 octal.

1.3 ARDATA — Stores one pattern into all 16 Address RAM locations, then reads it back from all 16 to verify data. Cycle is repeated for each pattern given below. Data patterns are the following:

No.	Pattern	No.	Pattern	No.	Pattern	No.	Pattern
1	000000	10	000040	19	100000	28	177377
2	177777	11	000100	20	177776	29	176777
3	125252	12	000200	21	177775	40	175777
4	052525	13	000400	22	177773	31	173777
5	000001	14	001000	23	177767	32	167777
6	000002	15	002000	24	177757	33	157777
7	000004	16	004000	25	177737	34	137777
8	000010	17	020000	26	177677	35	077777
9	000020	18	040000	27	177577	36	010000

1.4 ARCPP — Tests Address RAM-to-register and register-to-Address RAM circular path integrity; then tests parity generation. Octal data patterns given under ARDATA section, above, are used.

1.5 ORADDR — Same test as ARADDR, except that test is performed on Order RAM.

1.6 ORDATA — Same test as ARDATA, except that test is performed on Order RAM, and only the first 35 patterns are tested.

1.7 ORCP — Duplicates RAM/register portion of ARCPP, except that test is performed on Order RAM, and only the first 35 patterns are tested.

1.8 AREG — Tests the counting function of the Address RAM register.

1.9 OREG — Same as AREG only performed on Order RAM register.

1.10 NSGP1 — Tests "Next State Logic" portion of MPX Channel card. Performs test using the following I/O Orders: Control, Return Word Count Residue, Jump Conditional, Jump Unconditional, Sense and Interrupt.

1.11 NSGP2 — Tests "Next State Logic" portion of MPX Channel card. Performs test using the following two I/O Orders: End and End/Interrupt.

1.12 NSGP3 — Tests "Next State Logic" using the following two I/O Orders: Read and Write.

1.13 NSGP4 — Tests "Next State Logic" using the Set Bank Order.

1.14 STPAR — Tests "Next State Logic" parity generation with all possible combinations of the four states A, B, C, and D.

1.15 SIOTEST — This section uses the Selector Channel Maintenance Board which is designed to test the Multiplexer channel's execution of SIO program orders and Direct Commands. Those Direct I/O Command execution/response tests are:

Direct Command Responses

- SIN - sets interrupt request flip flop
- CIO - loads control register
- SIO - rejected (CCG) if channel is currently active. CCL should never occur.

1.15 Continued

Direct Command Responses (Continued)

WIO - loads the 16 bit counter/buffer
RIO - returns the 16 bit counter/buffer
TIO - returns the test board status

In conjunction with the Direct I/O Command execution/response tests, the Selector Channel Maintenance Board is used to exercise the eight (8) SIO program orders under all normal mode of Operation. For this section test, the Maintenance Board is installed on the Multiplexer's SIO Bus like a device controller with the appropriate device number and its interrupt - poll connected the multiplexer diagnostic then tests channel operation by specifying the appropriate control options by direct I/O command, setting up a SIO test program and issuing SIO command. In the default mode, the Maintenance Board behaves as a simple 16-bit turn-around buffer which is reset to zero (Ø) upon I/O Reset and it is loaded and read by both Direct and SIO Read/Write commands.

By specifying the certain control word options, the diagnostic program can cause incrementing of the buffer upon specific signal occurrences, and terminate the data transfer or the program upon word count rollover. The outbound data can be compared with the buffer contents and the termination can be specified on a compare failure. Those SIO program order/response tested are:

SIO Program Responses

JUMP	normal jump operation, with the jump met bit controlling conditional jumps
RETURN RESIDUE	strictly a channel function
INTERRUPT	sets interrupt request flip flop
END	normal end order execution
CONTROL	see discussion of control code
SENSE	returns test board status
WRITE	loads the counter/buffer or compares the word from memory with the current contents of the buffer, depending on the TNC control bit.

2.0 Description by Steps Within Section

The following are the description of the test step which is within section.

Section Name	Step Number	Test Function
IORES	5	Reset EOT (End of Transfer) Flip-flop.
ARADDR	7	Store into, then read back from the contents of an Address RAM location. Step is repeated once for each RAM location.
ARDATA	8	Store one of the data patterns into all 16 locations of the Address RAM. Step is repeated once for each data pattern.

2.0 Continued

Section Name	Step Number	Test Function
ARCPP	9	Perform Address RAM/register circular path test.
	10	Test odd-parity generation circuitry.
ORADDR	11	Same as Step 7 except that test is performed on Order RAM.
ORDATA	12	Same as Step 8 except that test is performed on Order RAM.
ORCP	13	Same as Step 9 except that test is performed on Order RAM.
AREG	14	Increment and check count in the Address RAM register.
OREG	15	Increment and check count in the Order RAM register.
NSGP1	16	Set up and execute test for an I/O Order. Step is repeated for each separate I/O Order. (Control, Return word count residue, Jump Conditional, Jump Unconditional, Sense and Interrupt).
NSGP2	17	Set up and execute test for an I/O Order. Step is repeated for each separate I/O Order. (End, End/Interrupt.)
NSGP3	18	Perform test step for two I/O Orders; Read and Write.
NSGP4	20	Performs test step for Set Bank Order
STPAR	19	Perform parity check for a given state combination. Step is repeated for each possible state of the "Next State Logic".
SIO TEST	41	CIO command execution/response test
	42	TIO command execution/response test
	43	WIO command execution/response test
	44	RIO command execution/response test
	45	CIO command test by TIO, CIO, TIO and test status word.
	46	SIN command execution/response test (100 millisecond timeout)
	47	End with Interrupt Order, Test DRT pointer, End W/Int Status, and TIO status word are tested. (100 millisecond timeout)
	48	End W/O Interrupt Test.
		The interrupt is not expected. The DRT pointer is tested. End W/O Interrupt Status and TIO status words are tested.

2.0 Continued

Section Name	Step Number	Test Function
	49	Interrupt Order Test (100 millisecond timeout). DRT pointer, Interrupt Order Status and TIO Status words are tested.
	50	Sense Order Test (100 millisecond timeout). DRT pointer, Sense Order Status word and End W/O Int. Status word, are tested
	51	Sense order Test Beyond 32K
	52	Test Jump Order (Unconditional)
	53	Test Jump Order (Conditional)
	54	Test Jump Order (Condition) with met bit on.
	55	Test Control Word (IOCW) with even bits.
	56	Test Control Word (IOCW) with odd bits
	57	Test IOAW Load with even bit pattern
	58	Test IOAW Load with odd bit pattern
	59	Test Read Order; no chaining
	60	Test RNW, RD STB, TOGGLE XFER, EOT counter
	61	Test Fast Mode data read pattern
	62	Test Fast Mode RNW, PRD STB, TIX, and EOT count
	63	Test Fast SR Read Mode and clock time
	64	Write Order test; no chaining
	65	Test on no compare (TNC) and count WR STB
	66	Test Write (1 wd) in Fast Mode
	67	Test Fast Mode; TNC, CLRIL, Pwr STB
	68	Test Fast Write Mode; 2K transfer and clock transfer
	69	Test chained read
	70	Test RNW, PRD STB, TIX, and EOT Count under Fast SR Mode.
	71	Chained Write Order Test
	72	Fast Mode: TNC and count PWR STB with CLRIL
	73	Error Response Test
	74	Transfer Error Test of non-existent memory
	75	Multi-Device access test with SIO read of 4K data
	76	Multi-Device access test with SIO write of 4K data

2.0 Continued

Section Name	Step Number	Test Function
	77	Multi-Device Read/Write of 4K data under SIO
	78	Multi-Device access with the write of 4K (unchained); Fast Mode.