CUSTOMER SUPPORT HANDBOOK

HP 3000
PRE-SERIES II
CE
HANDBOOK

HEWLETT PACKARD

GENERAL SYSTEMS DIVISION

30000-90070

PRINTED IN U.S.A.
SEPTEMBER 1977

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INTRODUCTION

INTRODUCTION

SECTION I

The pre-Series II CE Handbook is intended to provide any HP 3000 Series II trained CE with the necessary information to repair most hardware failures in the following systems:

HP 3000)
HP 3000 CX > = pre-Series II
HP 3000 Series I)

The CE Handbook is arranged into eight sections. All sections contain general information regarding all three pre-Series II configurations plus specific information for each individual configuration.

A summary of each section follows:

I. INTRODUCTION

This section provides a brief description of each pre-Series II configuration and supplies information for adding additional device controllers to any HP 3000 pre-series II system. Included are:

* PCA Board Map

* Recommended PCA Slot Assignments

* Voltage and Current Specifications

* Interrupt Polling Priority Sequence

* Data Service Request Priority Sequence

* Logical and Physical Device Number Assignments

Cabinet tie-together information is provided for both HP 29402B and HP 30390A style cabinetry.

II. AC - DC POWER

This section contains two parts. The first part deals with all DC power. Wiring and power specifications are included for all HP 3000 pre-Series II systems. The second part gives all AC power wiring and jumpering specifications for all HP 3000 pre-Series II systems.

III. COLD-LOAD

This section explains the cold-load as developed by all pre-Series II computers and a description of the Cold-Load Analyzer PCA and its usefullness in troubleshooting.

IV. DIAGNOSTICS

This section contains configuration, loading, and commands for the Stand-Alone Diagnostic Utility Program (SDUP) and the System Diagnostic Monitor (SDM).

Also included are loading examples for CPU, non-CPU, and On-LIne diagnostics, along with the program diagnostic numbers. SLEUTH differences and a list of mnemonics are included. A description of the WORKOUT program is provided to exercise disc and tape on-line.

V. MPE CONFIGURATION

This section lists MPE differences from Series II; configuration parameters; and console operator, system manager, system supervisor, and account manager commands.

In addition, a list of EDIT/3000 commands, a description of MPE system operations, and a list MPE error messages is included.

VI. MPE ANALYSIS

This section contains two parts. The first part deals with those problems can be analyzed using a DPAN listing. The examples included deal with isolating disc related problems. The second part deals with the Supported Utilities for all HP 3000 pre-Series II systems. A complete discussion including examples is given to aid the CE in the proper recovery techniques.

VII. MISCELLANEOUS

This section contains preventive maintenance information, a list of all the current acceptable PCA date code levels, an octal to decimal conversion chart, a set of ASCII to EBCDIC character code charts, a set of Hollerith to ASCII and ASCII to Hollerith code charts, and a service manual index for pre-Series II.

VIII. GENERAL HARDWARE

This section presents summary descriptions of all the subsystems starting with the CPU (30001A) and continuing through the Maintenance Panels (30354D). Each summary description is part of this section and lists differences from Series II, general information, cabling and/or configuration, diagnostics, and halt codes.

HP 3000

HP 3000 Hardware includes:

* Three 52 inch high cabinets with modular doors (30390A)
* Table and console (2749B, 2762A)
* System Disc (7900A, 2888A, 2660A, 7905A)
* Magnetic Tape Unit (7970B or 7970E)

The CPU cabinet consists of three or four card cages (four if selector channel is present), two HP 30310A Power Supplies, one mini-control panel, one power control module, and one cooling fan.

The I/O cabinet consists of one or two card cages, one or two HP 30310A Power Supplies, a power distribution unit, and a cooling fan.

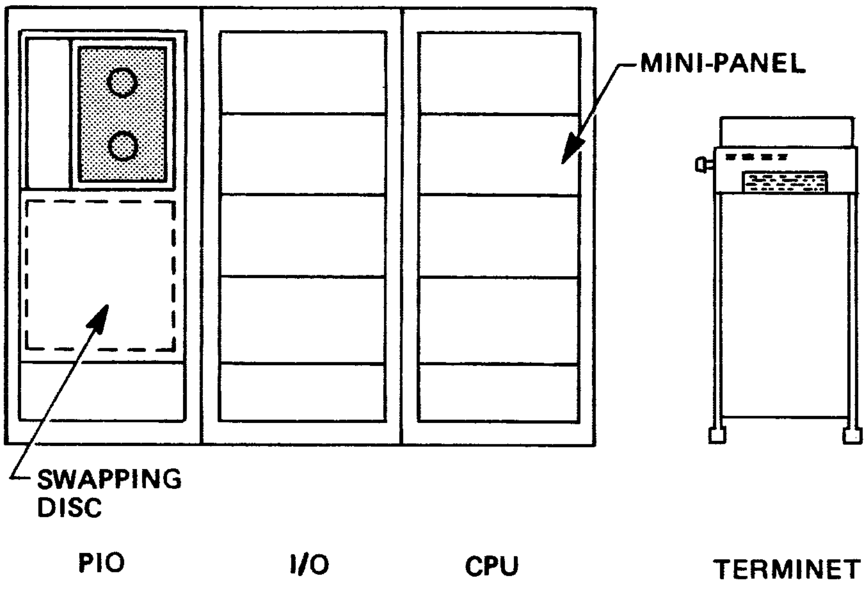
NOTE

> An additional power control unit and signal distribution panel for the HP 2888A disc may be installed in the I/O cabinet.

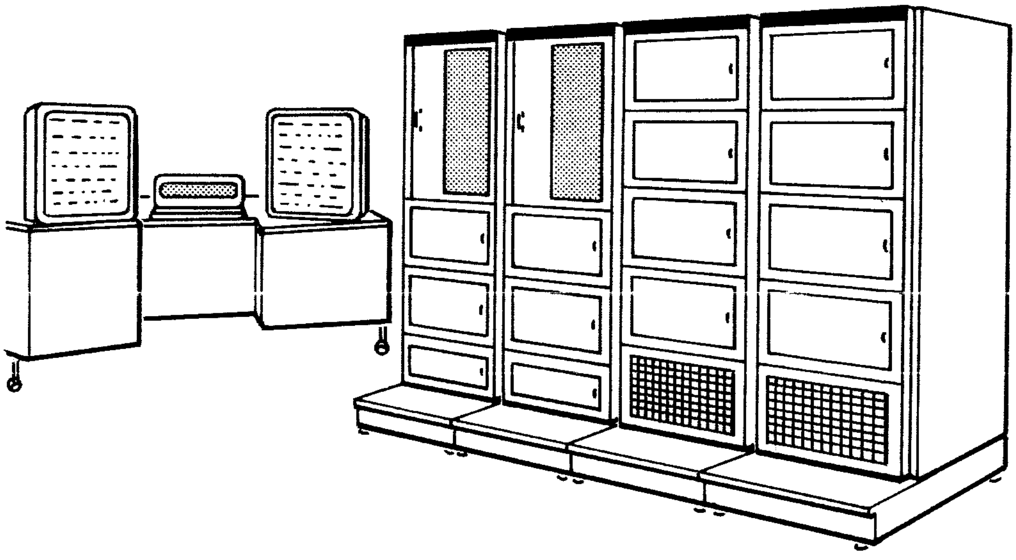
The Peripheral cabinet consists of one magnetic tape unit, one terminal control panel, a power distribution unit, and a cooling fan. In addition, any one of three system discs may be installed beneath the magnetic tape unit.

One HP 30030A/B Selector Channel subsystem may be installed on any HP 3000 or HP 3000 CX at any time. Refer to the HP 30030A Selector Channel Add-On Installation manual (30030-90015).

A sixth HP 3002A card cage and a fourth HP 30310A Power Supply may be installed on any HP 3000 or HP 3000 CX at any time. Refer to the HP 3000 Pre-Series II Add-On Power Supply Installation Manual (30412-90001).



(WITHOUT MAINTENANCE PANELS)



(WITH MAINTENANCE PANELS)

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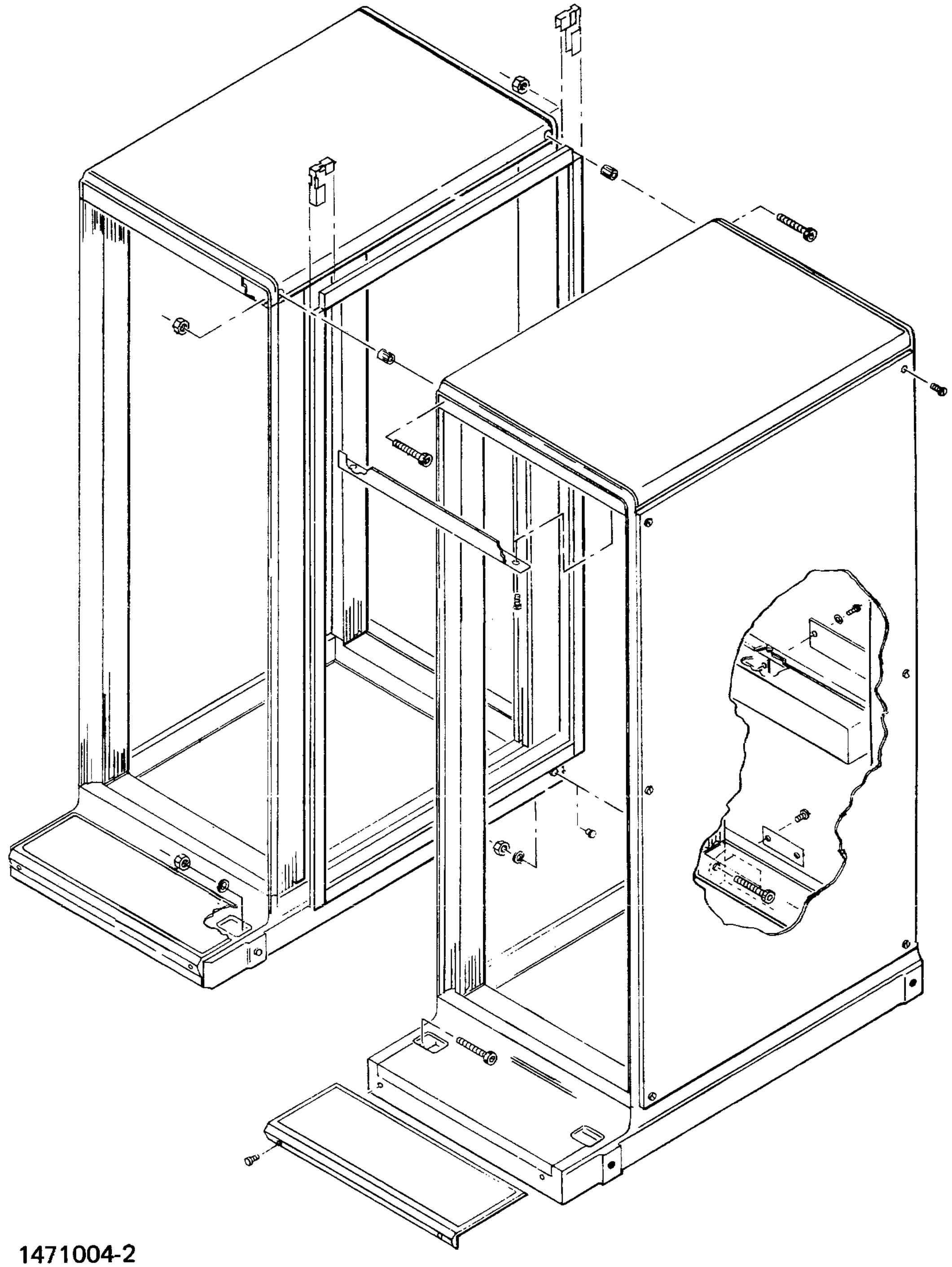
HP 3000 FRONT VIEW



MULTI-BAY CONFIGURATION, ASSEMBLY DETAILS

HP 3000 CX

HP 3000 CX hardware includes:

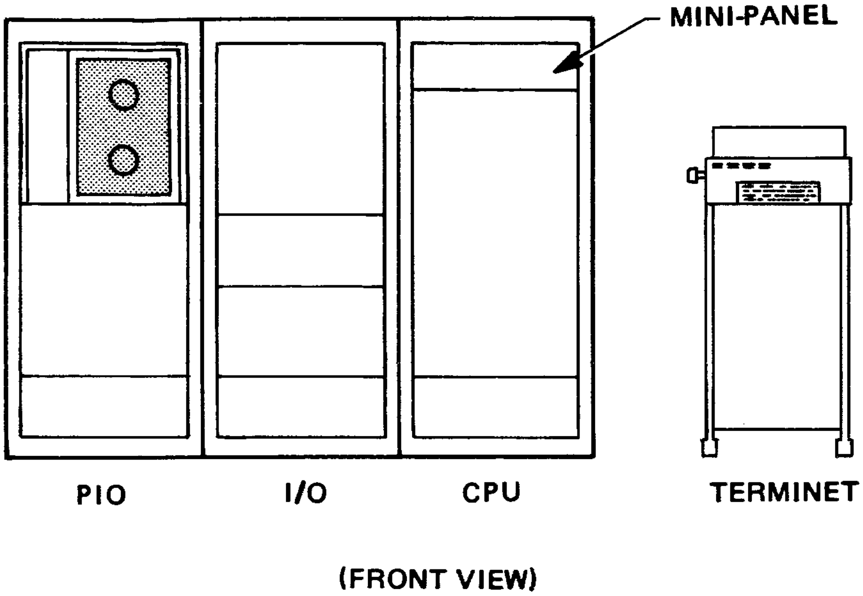
- Three Series II type cabinets (29402B)
- Table and Console (2762A, 2640A)
- System Disc (7900A, 2888A, 2660A, 7905A)
- Magnetic Tape Unit (7970B or 7970E)

The hardware included within the CPU, I/O, and Peripheral cabinets is identical to the HP 3000 systems, i.e., pre-CX.

NOTE

> Some CX models had an additional HP 7900A or 7905A Disc Drive mounted in the I/O cabinet.

HP 3000-0002 = 24.5 inch panel with key
HP 40015-00005 = 11 inch panel.



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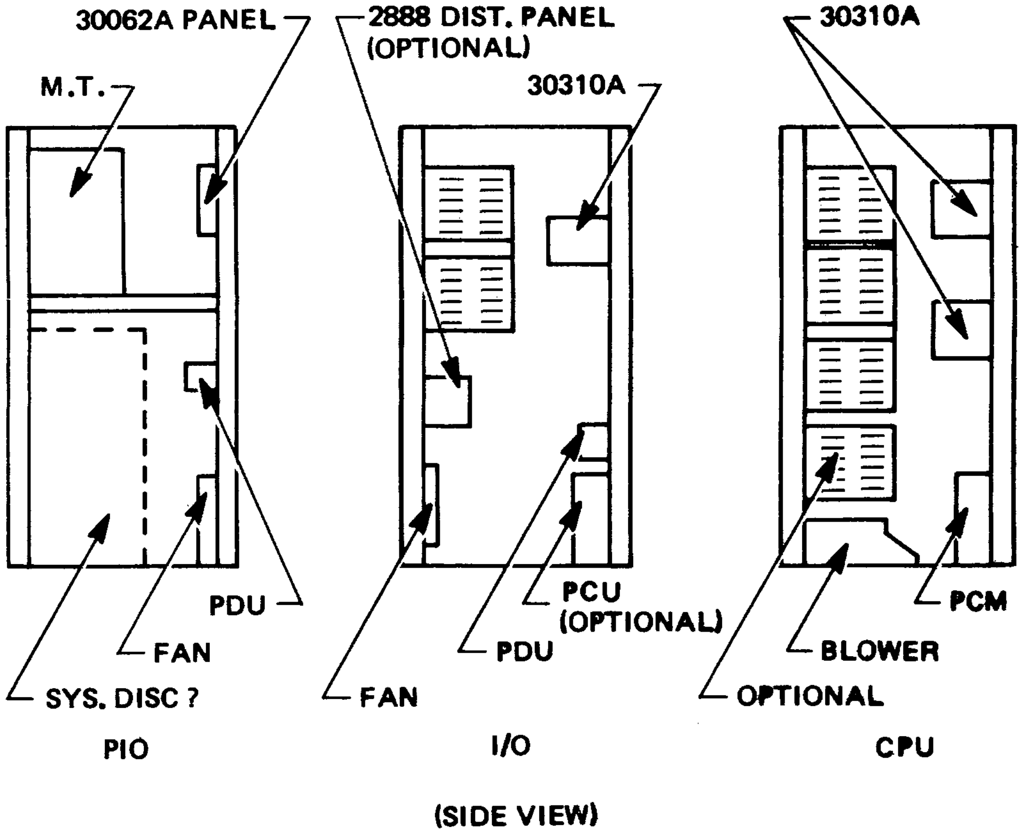

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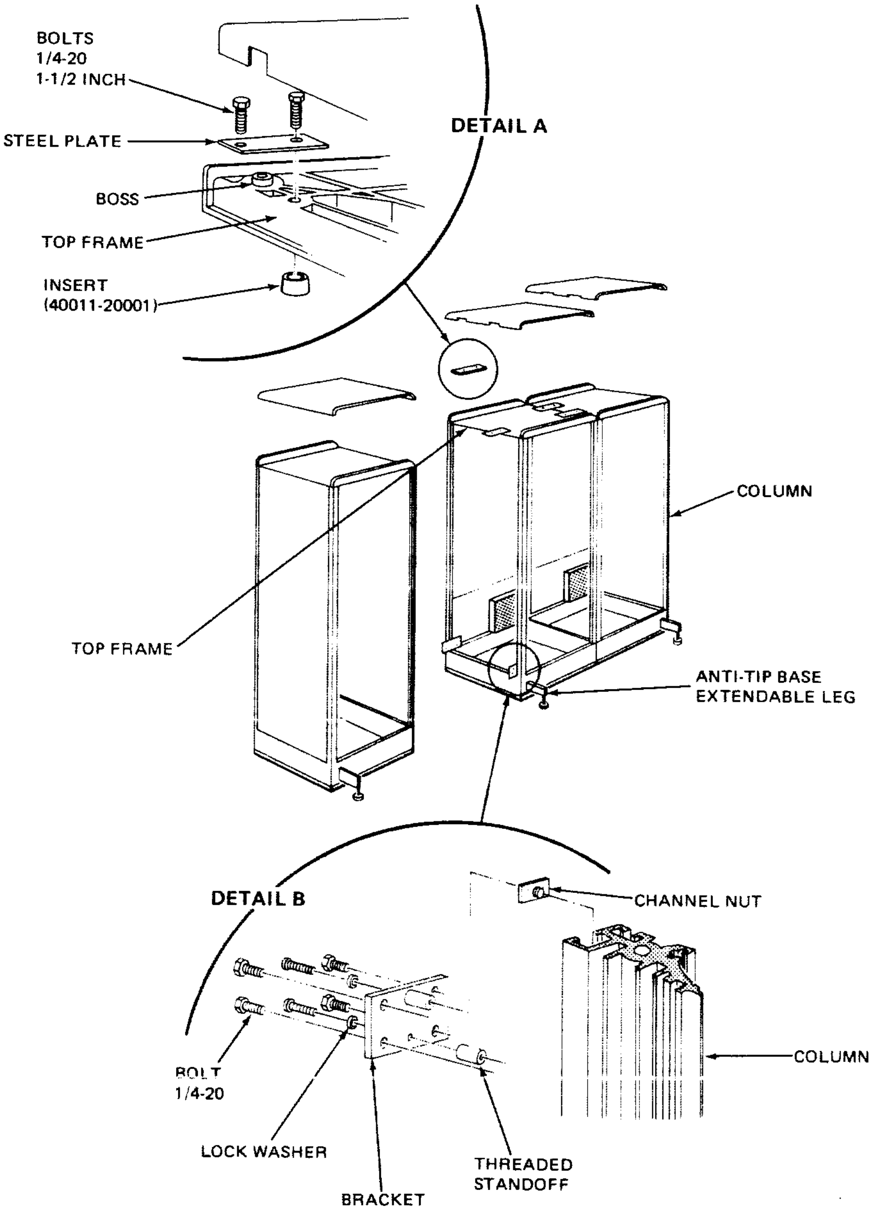
HP 3000 CX (with SEL-CHAN option)



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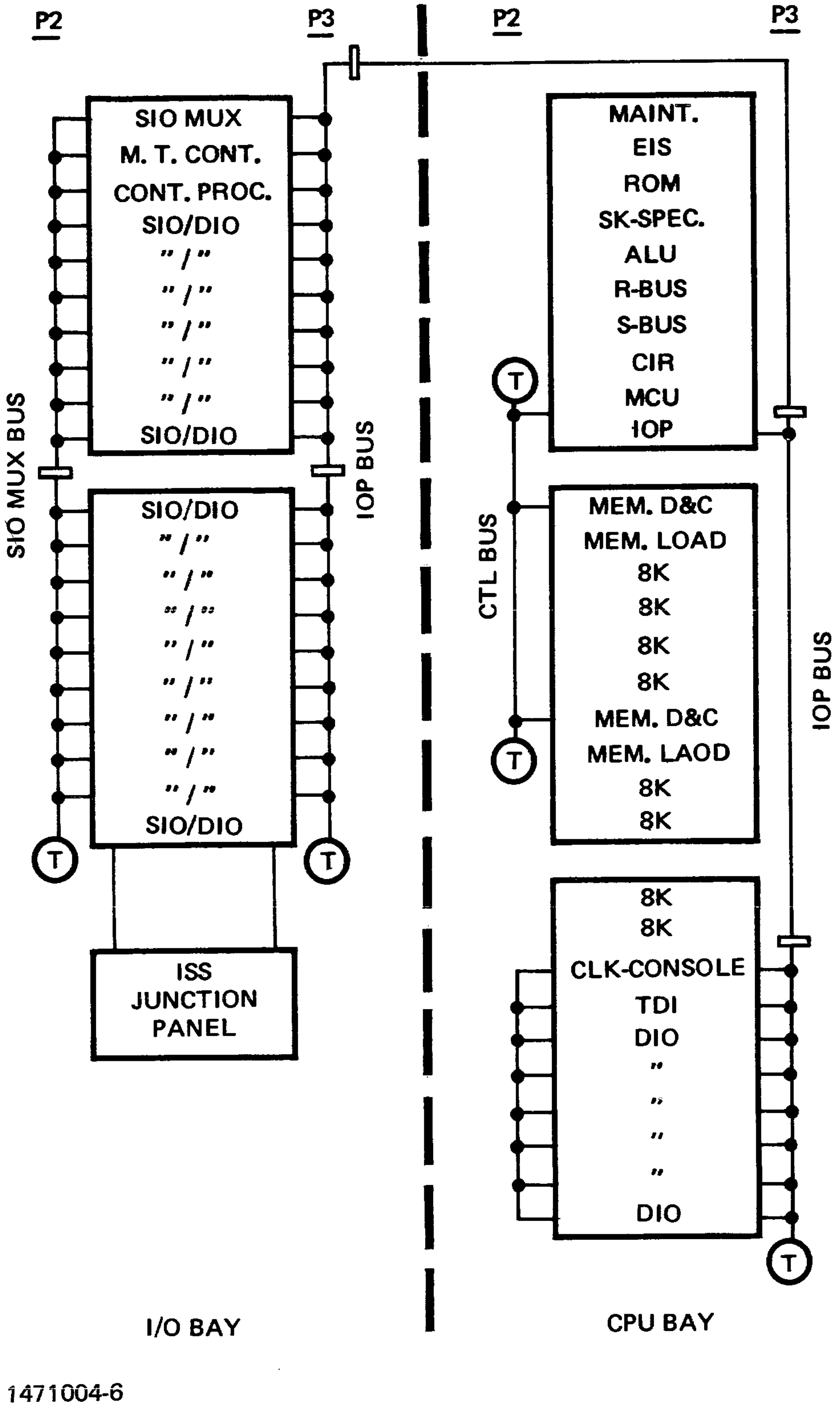
TIE-TOGETHER KIT INSTALLATION



HP 3000 CX BOARD MAP (without SEL-CHAN option)

HP 3000 and HP 3000 CX Systems
Recommended PCA Slot Assignments
(CPU Bay)

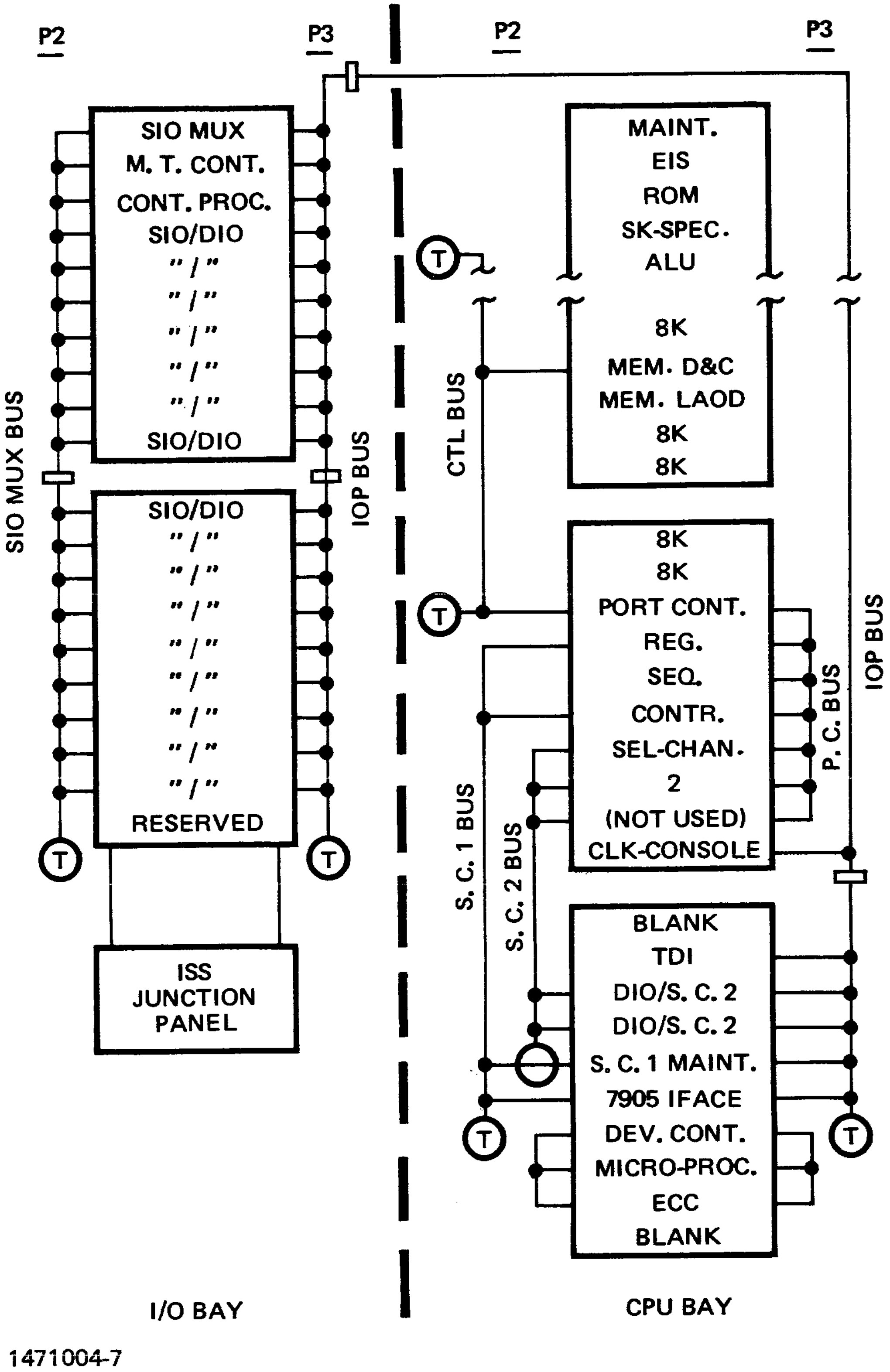
MIN DATE CODE	LOC	DESCRIPTION	DRT(%)	SLEUTH TYPE	SR	INT PRI	MISC.
	1A1	RESERVED FOR MPI					MOD #5
	1A2	EIS					MOD #5
	1A3	ROM					MOD #5
	1A4	SSF					MOD #5
	1A5	ALU					MOD #5
	1A6	R BUS					MOD #5
	1A7	S BUS					MOD #5
	1A8	CIR					MOD #5
	1A9	MCU					MOD #5
	1A10	IOP					MOD #5
	2A1	MEM DATA & CONT.					MOD #0
	2A2	MEM LOAD					
	2A3	MEM DRIVE & SENSE					8K WD.
	2A4	MEM DRIVE & SENSE					16K WD.
	2A5	MEM DRIVE & SENSE					24K WD.
	2A6	MEM DRIVE & SENSE					32K WD.
	2A7	MEM DATA & CONT.					MOD #1
	2A8	MEM LOAD					
	2A9	MEM DRIVE & SENSE					40K WD.
	2A10	MEM DRIVE & SENSE					48K WD.

HP 3000 and HP 3000 CX Systems
Recommended PCA Slot Assignments
(CPU Bay w/o Selector Channel)

LOC	DESCRIPTION	DRT (%)	SLEUTH TYPE	SR	INT PRI	MISC.
3A1	MEM DRIVE & SENSE					56K WD.
3A2	MEM DRIVE & SENSE					64K WD.
3A3	CLOCK-CONSOLE	3	8	-	1	MAX OF 1
3A4	TERM DATA INTF	7	6	-	2	MAX OF 1
3A5	TERM CONT INTF	8(10)	7	-	8	103 MODEM
3A6	TERM CONT INTF	9(11)	7	-	8	202 MODEM
3A7						NOT USED
3A8						NOT USED
3A9						NOT USED
3A10						NOT USED

HP 3000 AND HP 3000 CX Systems
Recommended PCA Slot Assignments
(I/O Bay)

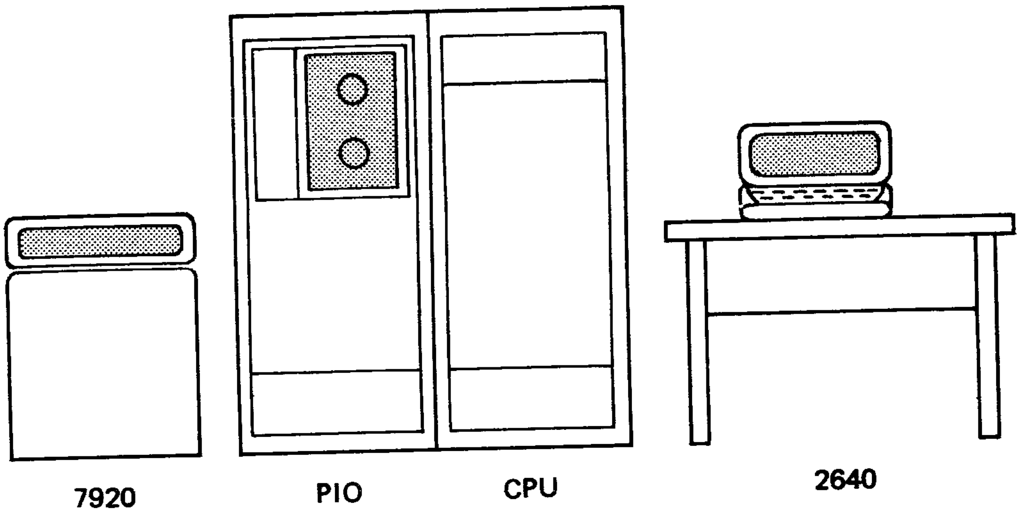
LOC	DESCRIPTION	DRT(%)	SLEUTH TYPE	SR	INT PRI	MISC.
5A1	SIO MUX	127(177)	1	-	-	MAX OF 1
5A2	PAPER TAPE READER	13(15)	20	14	3	MAX OF 1
5A3	SSLC	12(14)	3	6	4	MAX OF 2
5A4	SSLC		3	7	4	optional
5A5	30103A OR 30110A	5,4	17/3	2	6/7	MAX OF 1/2
5A6	30103A OR 30110A					
5A7	PLOTTER INTF	16(20)	22	8	9	MAX OF 1
5A8	PROG CONT	17(21)	25	10	10	MAX OF 1
5A9	MAG TAPE CONT	6	18,19	3,4	11	MAX OF 2
5A10	MAG TAPE CONT PROC					
6A1	MAG TAPE CONT	6	18,19	3,4	11	MAX OF 2
6A2	MAG TAPE CONT PROC					optional
6A3	LINE PRINTER (ALL)	11(13)	5,23	11	12	MAX OF 2
6A4	LINE PRINTER (ALL)		5,23	12	13	optional
6A5	CARD READER	10(12)	2	5	13	MAX OF 1
6A6	CARD READER/PUNCH	15(17)	24	15	14	MAX OF 1
6A7	PAPER TAPE PUNCH	14(16)	21	9	16	MAX OF 1
6A8	2888A DISC CONT PROC					
6A9	2888A DISC READ/WRITE	5,4	14	1	6/7	MAX OF 1
6A10	2888A DISC FILE BUS					



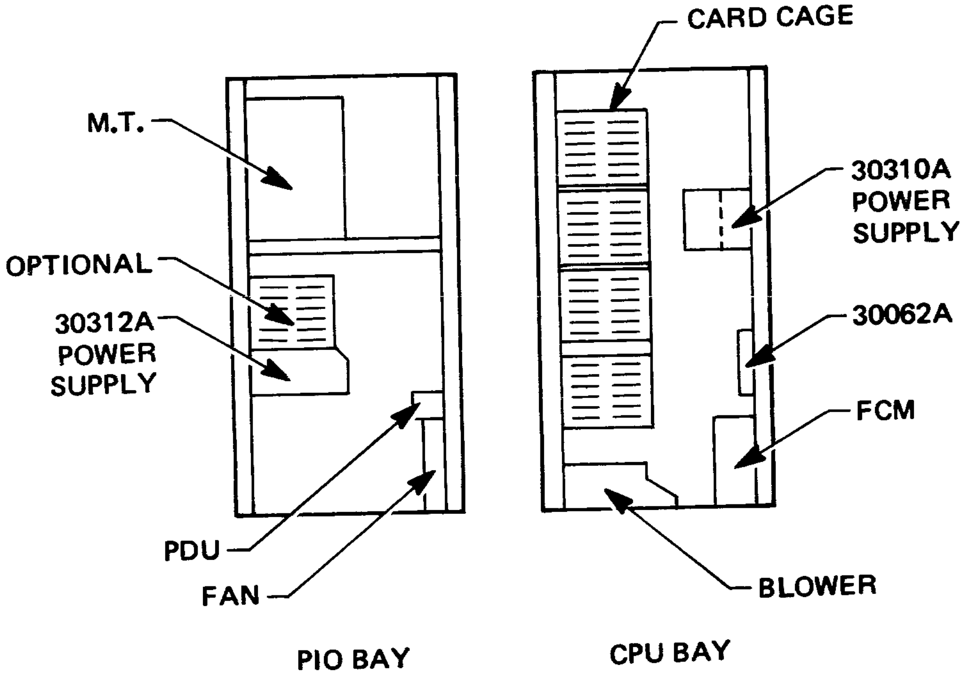
HP 3000 AND HP 3000 CX BOARD MAP (with SEL-CHAN option)

HP 3000 and HP 3000 CX Systems
Recommended PCA Slot Assignments
(CPU Bay with Selector Channel)

LOC	DESCRIPTION	DRT(%)	SLEUTH TYPE	SR	INT PRI	MISC.
3A1	MEM DRIVE & SENSE					56K WD.
3A2	MEM DRIVE & SENSE					64K WD.
3A3	PORT CONTROLLER					MOD #4
3A4	SEL CHAN REGISTER					
3A5	SEL CHAN SEQUENCER					MAX OF 1
3A6	SEL CHAN CONTROL					
3A7						NOT USED
3A8						NOT USED
3A9						NOT USED
3A10	CLOCK-CONSOLE	3	8	-	1	
4A1						NOT USED
4A2	TERM DATA INTF	7	6	-	2	MAX OF 1
4A3	TERM CONT INTF	8(10)	7	-	8	103 MODEM
4A4	TERM CONT INTF	9(11)	7	-	8	202 MODEM
4A5	SEL CHAN MAINT BOARD					
4A6	CART DISC INTF	5,4	15		5	MAX OF 1
4A7	7905A DEV CONT					
4A8	7905A MICRO PROC					MAX OF 8
4A9	7905A ERROR CORRECT					
4A10						NOT USED



(FRONT VIEW)



(SIDE VIEW WITH I/O CAGE)

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HP 3000 SERIES I

HP 3000 Series I hardware includes:

* Two Series II type cabinets (29402B)

* Table and console (2640B or 2762A)

* System Disc (HP 7920A). This is the only supported disc.

* Magnetic Tape Unit (7970B or 7970E)

* Isolation Transformer (12.6 KVA)

The CPU cabinet consists of a HP 30310A Power Supply, four Series II type card cages, one mini-control panel, a power control module, and a cooling fan.

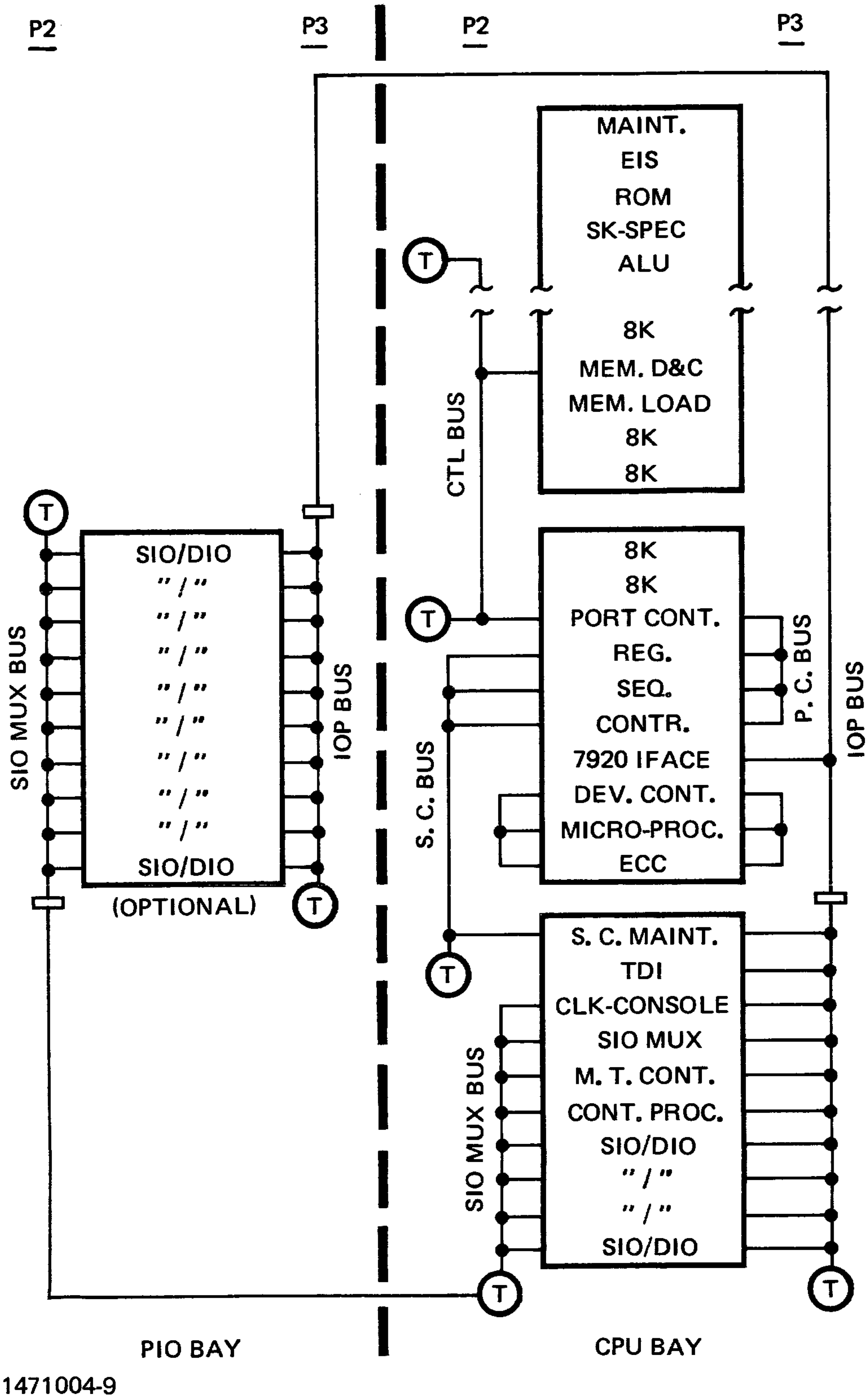
The Peripheral cabinet consists of one HP 7970B/E Magnetic Tape Unit, an HP 30312A Power Supply, a terminal control panel, a power distribution unit, and a cooling fan.

Up to five I/O slots are provided in the bottom card cage of the CPU cabinet.

ADDITIONAL I/O SLOTS

Optionally, ten additional I/O slots are provided by a fifth Series II type card cage located directly below the magnetic tape unit in the Peripheral cabinet. DC power for this card cage is supplied by an additional HP 30312A Power Supply. In this case, both HP 30312A Power Supplies are mounted side-by-side directly below the fifth card cage.

A second HP 30312A Power Supply and fifth HP 30002C card cage may be installed on any HP 3000 Series I system at any time. Refer to the HP 3000 Series I Computer System I/O Expansion Kit Installation Manual (30413-90001).



HP 3000 SERIES I BOARD MAP

HP 3000 Series I
Recommended PCA Slot Assignments
(CPU Bay)

LOC	DESCRIPTION	DRT(%)	SLEUTH TYPE	SR	INT PRI	MISC.
1A1	RESERVED FOR MPI					MOD #5
1A2	EIS					MOD #5
1A3	ROM					MOD #5
1A4	MOD #5					
1A5	ALU					MOD #5
1A6	R BUS					MOD #5
1A7	S BUS					MOD #5
1A8	CIR					MOD #5
1A9	MCU					MOD #5
1A10	IOP					MOD #5
2A1	MEM DATA & CONT					MOD #0
2A2	MEM LOAD					
2A3	MEM DRIVE & SENSE					8K WD.
2A4	MEM DRIVE & SENSE					16K WD.
2A5	MEM DRIVE & SENSE					24K WD.
2A6	MEM DRIVE & SENSE					32K WD.
2A7	MEM DATA & CONT					MOD #1
2A8	MEM LOAD					
2A9	MEM DRIVE & SENSE					40K WD.
2A10	MEM DRIVE & SENSE					48K WD.

HP 3000 Series I
Recommended PCA Slot Assignments
(CPU Bay)

LOC	DESCRIPTION	DRT(%)	SLEUTH TYPE	SR	INT PRI	MISC.
3A1	MEM DRIVE & SENSE					
3A2	MEM DRIVE & SENSE					
3A3	PORT CONT					MOD #4
3A4	SEL CHAN REGISTER	|				
3A5	SEL CHAN SEQUENCER	|-				MAX OF 1
3A6	SEL CHAN CONTROL	|				
3A7	CART DISC INTF	5	15	-	5	
3A8	7920A DEV CONT	|				
3A9	7920A MICRO PROC	|-				MAX OF 8
3A10	7920A ERROR CORRECT	|				
4A1	SEL CHAN MAINT BOARD					
4A2	TDI	7	5	-	2	MAX OF 1
4A3	TCI	8(10)	7	-	8	103 MODEM
4A4	TCI	9(11)	7	-	8	202 MODEM
4A5	CLOCK-CONSOLE	3	8	-	-	MAX OF 1
4A6	SIO MUX	127(177)	1	-	-	MAX OF 1
4A7	MAG TAPE CONT	6	18,19	3	11	MAX OF 2
4A8	MAG TAPE CONT PROC					
4A9	LINE PRINTER (ALL)	11(13)	5,23	11	12	MAX OF 2
4A10	CARD READER	10(12)	2	5	13	MAX OF 1

HP 3000 Series I (with Additional I/O Cage)
Recommended PCA Slot Assignments
(CPU Bay)

LOC	DESCRIPTION	DRT(%)	SLEUTH TYPE	SR	INT PRI	MISC.
4A1	SEL CHAN MAINT BOARD					
4A2	TDI	7	6	-	2	MAX OF 1
4A3	TCI	8(10)	7	-	8	103 MODEM
4A4	TCI	9(11)	7	-	8	203 MODEM
4A5	CLOCK-CONSOLE	3	8	-	1	MAX OF 1
4A6	SIO MUX	127(177)	1	-	-	MAX OF 1
4A7	SSLC	12(14)	3	6	4	MAX OF 2
4A8	SSLC		3	7	4	optional
4A9	PLOTTER	16(20)	22	8	9	MAX OF 1
4A10	CARD READER	10(12)	2	5	13	MAX OF 1
	(ADITIONAL I/O CAGE - PIO BAY)					
7A1	PAPER TAPE READER	13(15)	20	14	3	MAX OF 1
7A2	PROG CONT	17(21)	25	10	10	MAX OF 1
7A3	MAG TAPE CONT	6	18,19	3	11	MAX OF 2
7A4	MAG TAPE CONT PROC					
7A5	MAG TAPE CONT		18,19	4	11	optional
7A6	MAG TAPE CONT PROC					
7A7	LINE PRINTER (ALL)	11(13)	5,23	11	12	MAX OF 2
7A8	LINE PRINTER (ALL)		5,23	12	12	optional
7A9	CARD READER/PUNCH	15(17)	24	15	14	MAX OF 1
7A10	PAPER TAPE PUNCH	14(16)	21	9	16	MAX OF 1

ADD-ON PERIPHERALS TO HP 3000 AND HP 3000 CX SYSTEMS

The following chart provides the DC voltage and current requirements for all supported interfaces. When adding new controller PCA´s, a check must be made to determine whether the HP 30310A Power Supply can supply the additional current. Add up all the currents for each controller. If the total exceeds 55 amperes, then an additional HP 30310A Power supply is required. Refer to the recommended PCA slot assignments for HP 3000 and HP 3000 CX systems when installing additional I/O´s.

NOTE

> This check is necessary for all controller PCA´s in the I/O cabinet.

ADD-ON PERIPHERALS TO AN HP 3000 SERIES I SYSTEM

The Series I system differs from the HP 3000 and HP 3000 CX systems because of the DC voltage limitations when the additional I/O card cage is provided. This additional card cage is powered by one HP 30312A Power Supply. Only +5Vdc is provided, therefore not all supported controllers can be installed in this card cage. The voltage and current configurations chart indicates where each controller can be installed. Refer to the recommended PCA slot assignment for HP 3000 Series I systems when installing additional I/O´s. No current checks are necessary.

7905A mounted in HP 3000 cabinets require:

1 each HP 12904A Rack Slide Mount Kit

2 each HP 5000-8080 Brackets

In all cases, the 7905A is mounted below the Magnetic Tape Unit.

Voltage and Current Configurations

	+15V	+5V	-5V	-15V	TOTALS
TDI 30032B	0.07	2.8	0.06	0.17	3.10
TCI 30061A	0.16	1.3	0.10	0.22	1.78
Clock-Console 30031A	0.11	3.3		0.06	3.47
SIO MUX 30035A		3.6	0.11		3.71
Plotter Interface 30226A	0.08	2.2			2.28
Emulator Subsystem 30055A	0.2	3.5		0.20	3.9
Card Reader 30206A	0.1	3.3		0.006	3.406
Disc Controller 30202A	.10	14.3		.07	14.47
Disc Controller 30203A		5.5			5.5
Disc Controller 30210A	.10	9.9	.06	.08	10.14
Disc Interface 30229A		3.6			3.6
Programmable Controller 30300A (see Note)		4.4			4.4
Line Printer 30051A (see Note)		4.4			4.4
Card Punch 30051A (see Note)		4.4			4.4
Card Reader/Punch 30050A (see Note)		4.0			4.0
Paper Tape Reader 30050A (see Note)		4.0			4.0
Paper Tape Punch 30050A (see Note)		4.0			4.0
Magnetic Tape Controller 30215A (see Note)		9.9			9.9

NOTE

Only these PCA's can be installed in the additional I/O slots of the PIO cabinet in an HP 3000 Series I system.

HP 3000 pre-Series II I/O System Interrupt Polling Sequence

INT.#	PRODUCT	DESCRIPTION
1	30031A	CLOCK-CONSOLE
2	30032B	TERMINAL DATA INTERFACE
3	30104A	PAPER TAPE READER
4	30055A	SSLC (ALL USES)
5	30129A	7905A DISC DRIVE
6,7	30103A	2660A DISC DRIVE
6,7	30110A	7900A DISC DRIVE
6,7	30102A	2888A DISC DRIVE
8	30032B-001, -002	TERMINAL CONTROL INTERFACE
9	30126A	PLOTTER
10	30300/1A	PROGRAMMABLE CONTROLLER
11	30115A	7970B/E MAGNETIC TAPE UNIT
12		ALL LINE PRINTERS
13	30106/7A	CARD READER
14	30119A	CARD READER/PUNCH
15	30112A	CARD PUNCH
16	30105A	PAPER TAPE PUNCH

HP 3000 pre-Series II I/O System
Service Request Priority Sequence

SR #	PRODUCT	DESCRIPTION
0	30033A	SEL CHAN MAINT BOARD
1	30102A	2888A DISC DRIVE
2	30103A	2660A DISC DRIVE
2	30110A	7900A DISC DRIVE
3,4	30115A	7970B/E MAGNETIC TAPE UNIT
5	30106/7A	CARD READER
6,7	30055A	SSLC
8	30126A	PLOTTER
9	30105A	PAPER TAPE PUNCH
10	30300/1A	PROGRAMMABLE CONTROLLER
11,12		ALL LINE PRINTERS
13	30112A	CARD PUNCH
14	30104A	PAPER TAPE READER
15	30119A	CARD READER/PUNCH

HP 3000 pre-Series II
Device Number Assignments

LOGICAL DEVICE	DESCRIPTION	DEVICE NUMBER
*1	SYSTEM DISC (UNIT 0)	*5
2	ADDITIONAL DISC (UNIT 1)	5
*3	CLOCK-CONSOLE	*3
4	DISC CONTROLLER (UNIT 0)	4
5	CARD READER	10
6	LINE PRINTER (FIRST)	11
7-10	MAG TAPE (FIRST)	*6
11,12	ADDITIONAL DISCS (UNIT 1 AND 2)	4
13	SSLC (FIRST)	12
14	SSLC (SECOND)	18
15	PAPER TAPE READER	13
16	PAPER TAPE PUNCH	14
17	CARD READER/PUNCH	15
18	PLOTTER	16
19	LINE PRINTER (SECOND)	19
20-35	TERM DATA INTF	7
NONE	TERM CONT INTF (103 MODEM)	8
NONE	TERM CONT INTF (202 MODEM)	9
36	PROG CONT	17
NONE	SIO MUX	127

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* This number must not be changed.

NOTE

All disc drivers must be core resident.

Connect all interface and ground cables to peripherals. Turn on AC power, then AC power switches to both power supplies and the magnetic tape unit. Check that all fans are operating properly.

Connect the maintenance panels and turn on DC power via the DC Enable switch.

Check all DC voltage levels to all card cages. Adjust voltages as required. (See AC - DC Power Section for specifications.)

Load %3704 in RAR and run the memory micro-diagnostic. Memory +20V must be "schmooed" if additional memory is installed.

Load and run all five sections of the CPU diagnostic.

Load and run Memory, SIO Mux, Selector Channel, SLEUTH Configurator, Floating Point, Decimal Firmware and Magnetic Tape Unit diagnostics in this order.

Load MPE Cold-Load tape and run the WORKOUT program (see instructions in the DIAGNOSTICS section of this manual).

NOTE

Disc drive unit numbers must be contiguous.

MPE can only be Cold-Loaded from the magnetic tape controller strapped for DEVNO 6, otherwise a "UNIT NOT READY" message will appear at the console.

AC-DC POWER

AC-DC POWER

SECTION II

AC - DC POWER DIFFERENCES

All HP 3000 Series I systems have a single 12.6 KVA isclation transformer.

All HP 3000 pre-Series II systems have provisions for the HP 30350A and HP 30352A maintenance panels on the Power Control Module (PCM).

HP 3000 AND HP 3000 CX DC POWER DISTRIBUTION

GENERAL

The HP 30310A Power Supply is the only power supply used in the HP 3000 and CX systems.

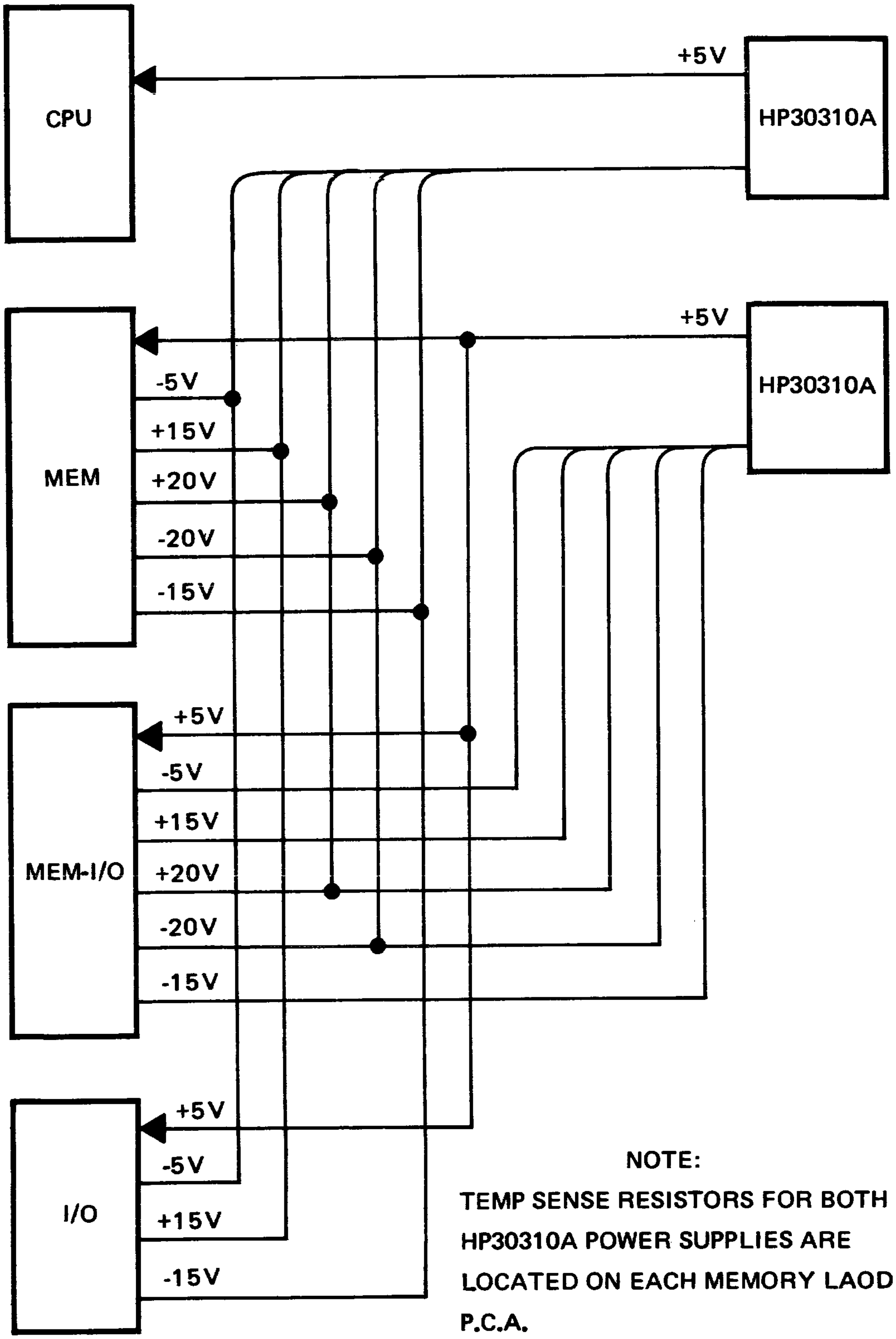
There are always two HP 30310A Power Supplies mounted in the CPU cabinet to provide +20, +15, +5, -5, -15, and -20 volts to all card cages.

The upper most power supply provides only +5 volts to the first (CPU) card cage and +20, +15, -5, -15, and -20 volts to the second (memory) card cage. If the selector channel option is installed then this supply also supplies +15, -5, and -15 volts to the fourth (I/O) card cage.

The lower most power supply provides +5 volts to the second (memory) card cage and +20, +15, +5, -5, -15, and -20 volts to the third (memory - I/O) card cage. If the selector channel option is installed, then this supply only provides +5 volts to the fourth (I/O) card cage.

The fourth (I/O) card cage does not have +20 or -20 volts. Only the memory boards require this voltage. Note that the +20 and -20 volts from both power supplies must track together (i.e. as the temperature increases, the +20 volts decreases, and when the temperature decreases, the +20 volts increases).

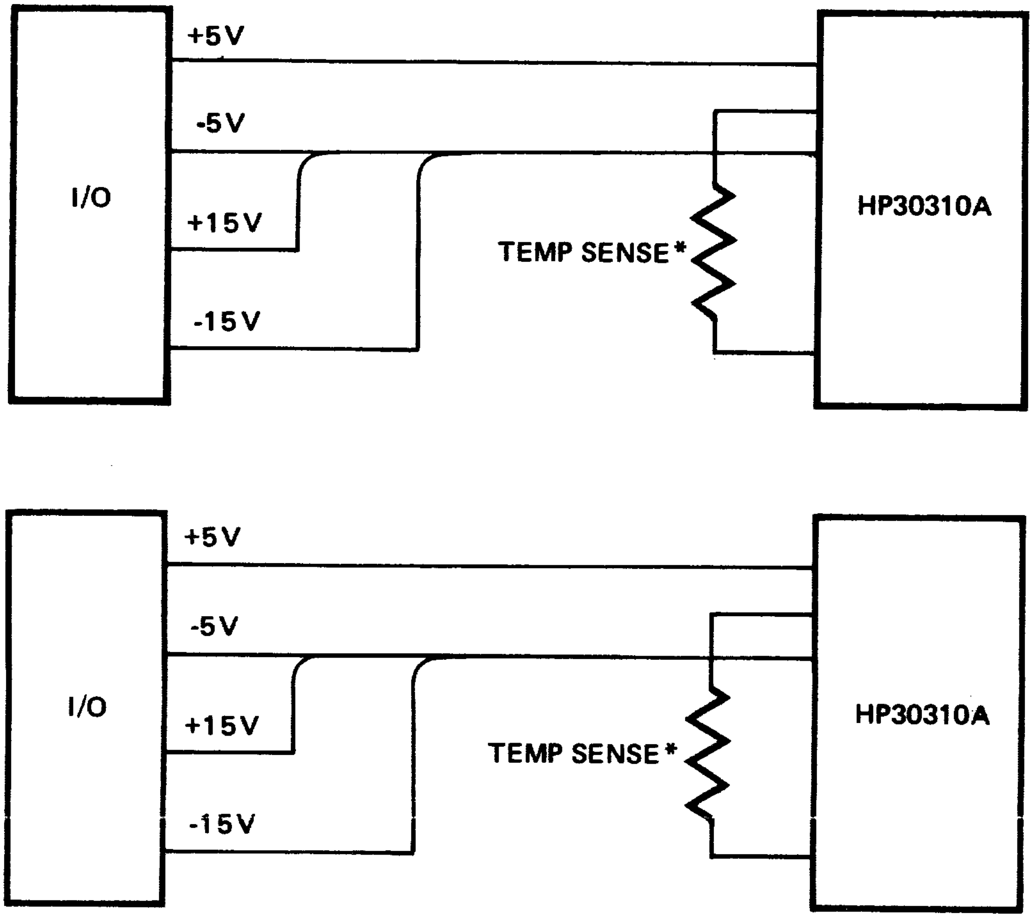
There is always one HP 30310A Power Supply in the I/O cabinet. Some configurations may require a second HP 30310A Power Supply in the I/O cabinet. In any case, the HP 30310A Power Supply provides +15, +5, -5, and -15 volts to the fifth (I/O) or sixth (I/O) card cages.



NOTE:
TEMP SENSE RESISTORS FOR BOTH HP30310A POWER SUPPLIES ARE LOCATED ON EACH MEMORY LAOD P.C.A.

1471004-10

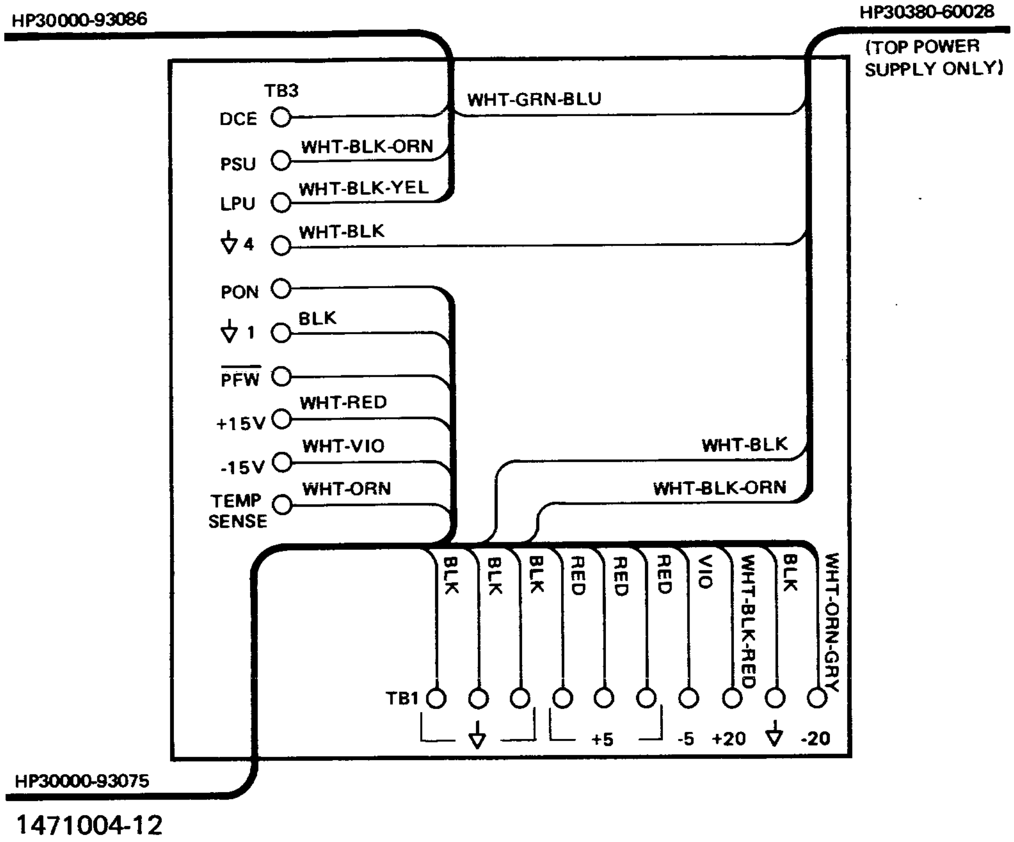
CPU BAY (side view)



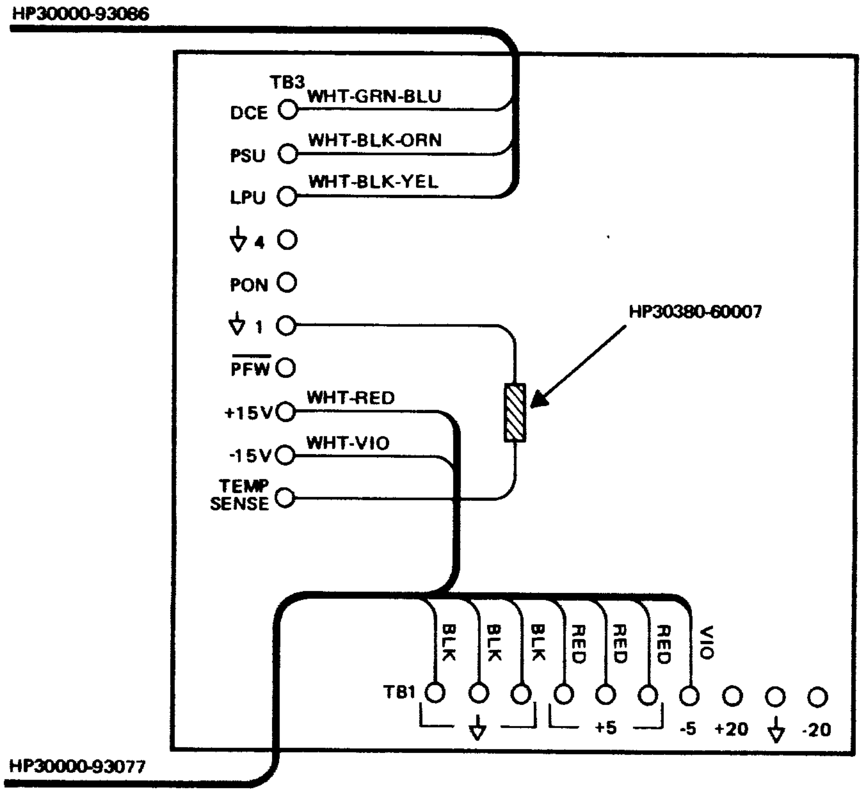
* A 1.21K ohm temperature sense resistor must be used when there is no load on the +20 volt circuit.

1471004-11

I/O BAY (side view)

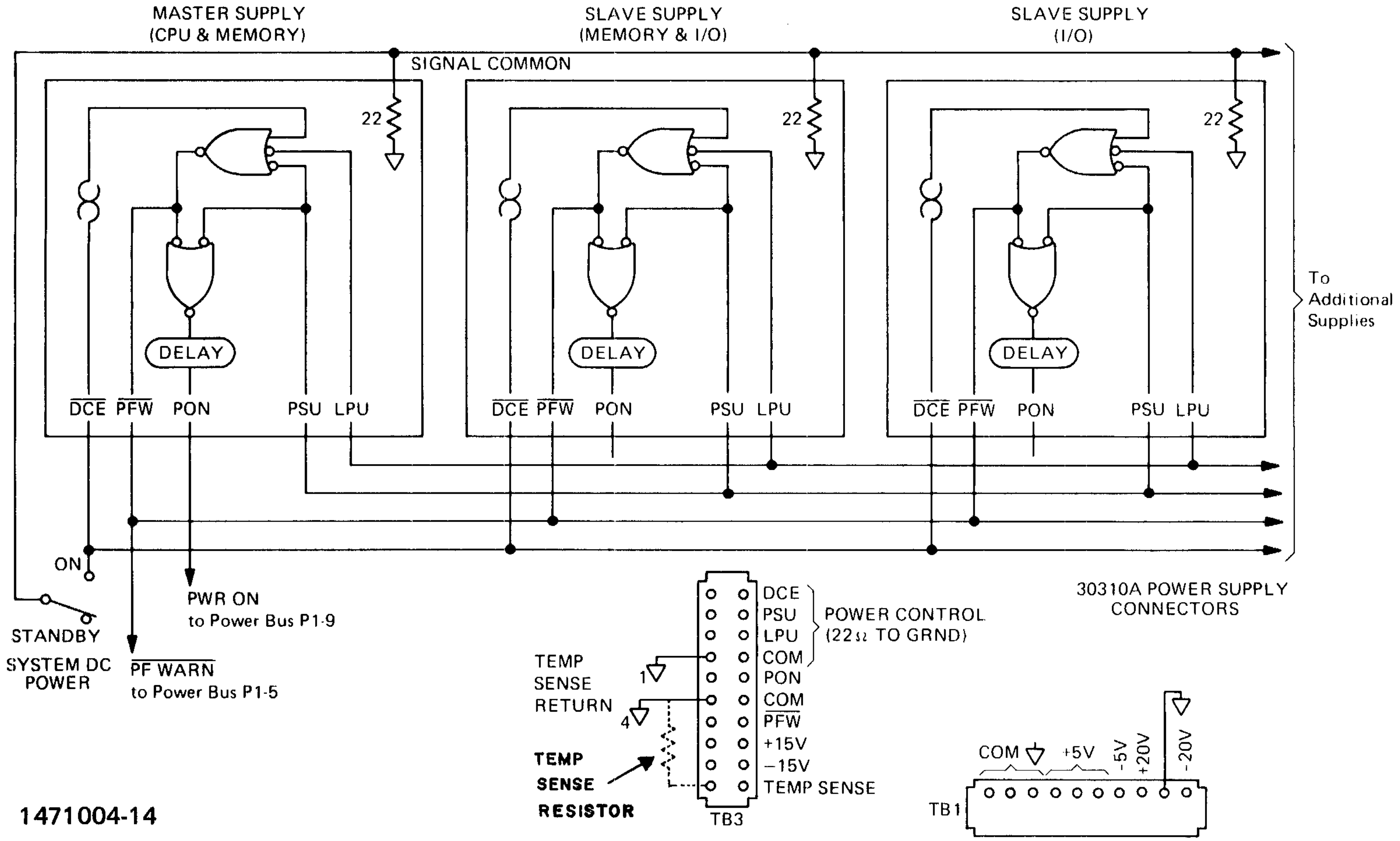


CPU BAY POWER SUPPLY CABLE CONNECTION



1471004-13

I/O BAY POWER SUPPLY CABLE CONNECTION



DC POWER CONTROL SIGNALS

HP 3000 SERIES I DC POWER CONFIGURATION

GENERAL

The HP 3000 Series I system uses both the HP 30310A and HP 30312A Power Supplies.

The CPU cabinet only contains one HP 30310A Power Supply. This supply provides +5 volts to the first (CPU) card cage, +20, +15, -5, and -15 volts to the second (memory) and third (memory) card cages. It also supplies +15, -5, and -15 volts to the fourth (I/O) card cage.

The HP 30312A Power Supply provides only +5 volts to the second (memory), third (memory - I/O), and fourth (I/O) card cages.

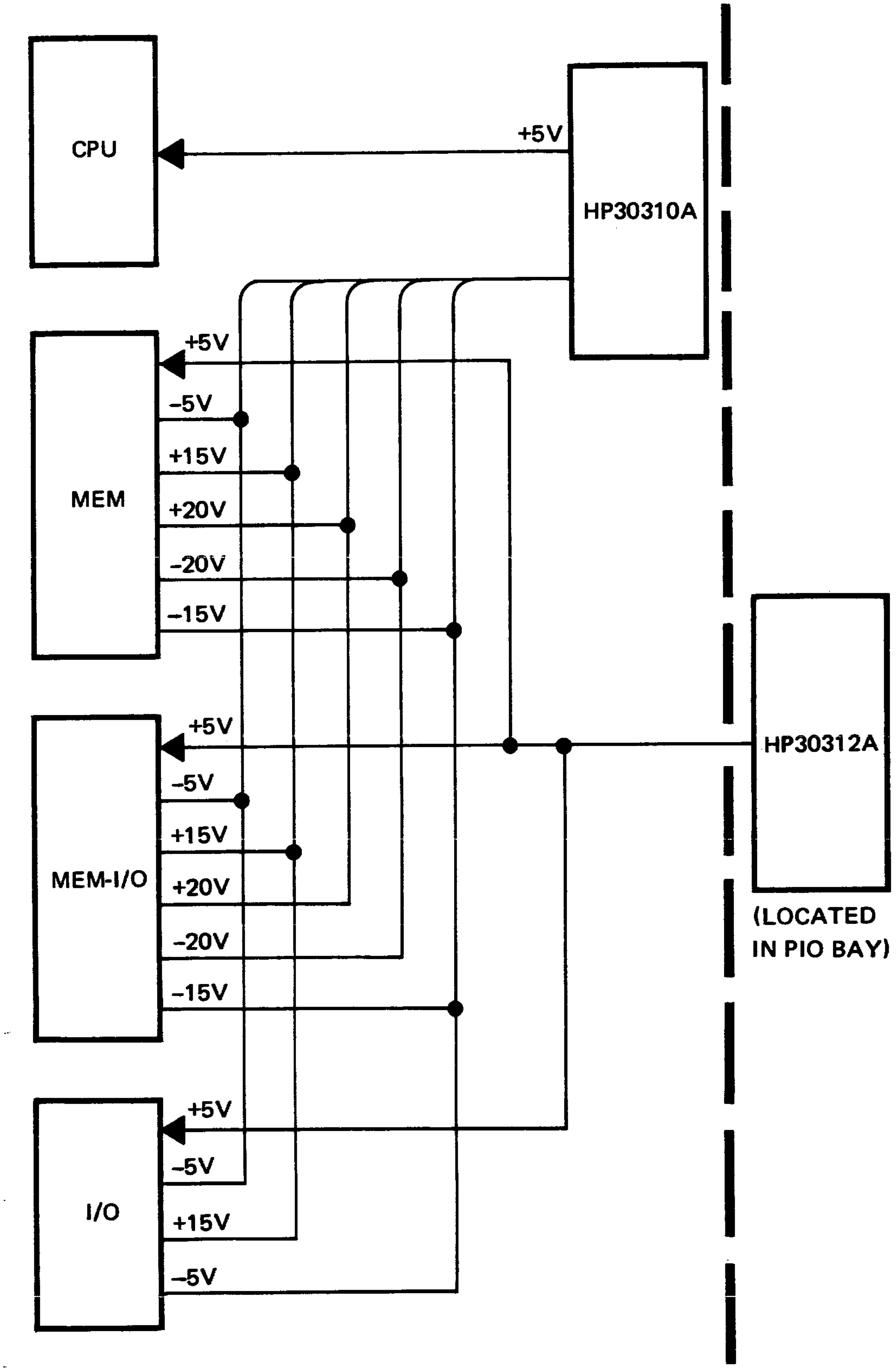
The fourth (I/O) card cage does not have +20 or -20 volts. Only the memory boards require this voltage.

The HP 30312A Power Supply is mounted beneath the magnetic tape unit in the PIO Bay. It is mounted there in order to facilitate servicing (i.e. removal) and to better balance the AC power loads.

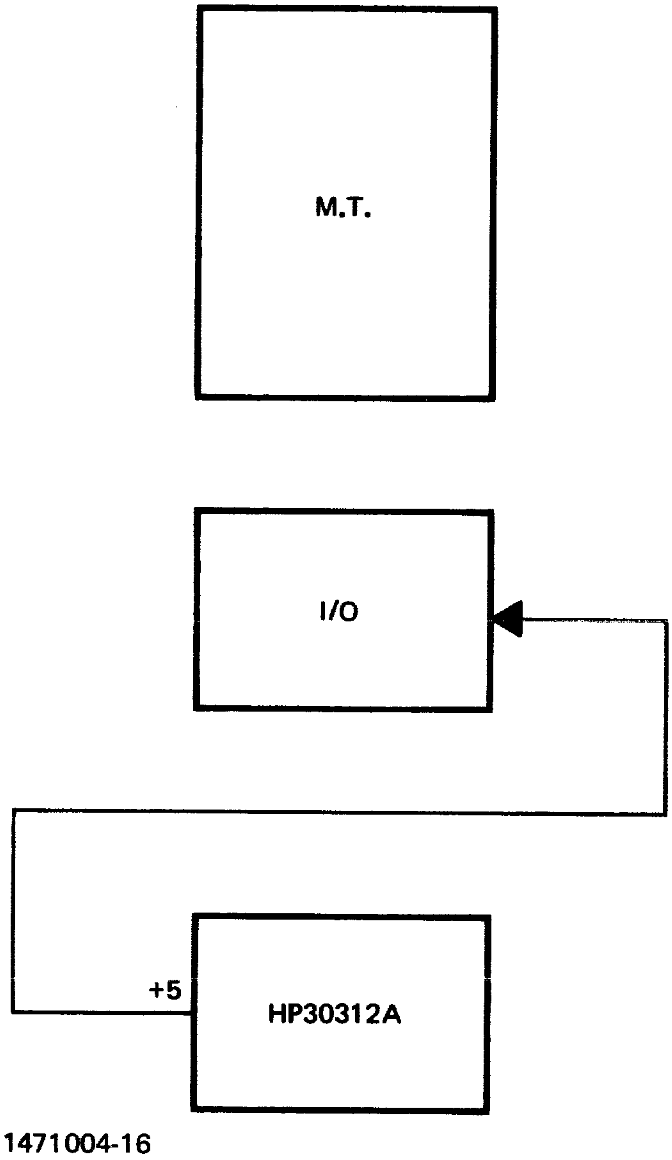
When the additional I/O option is installed, another HP 30312A Power Supply and card cage are provided beneath the magnetic tape unit in the PIO Bay.

NOTE

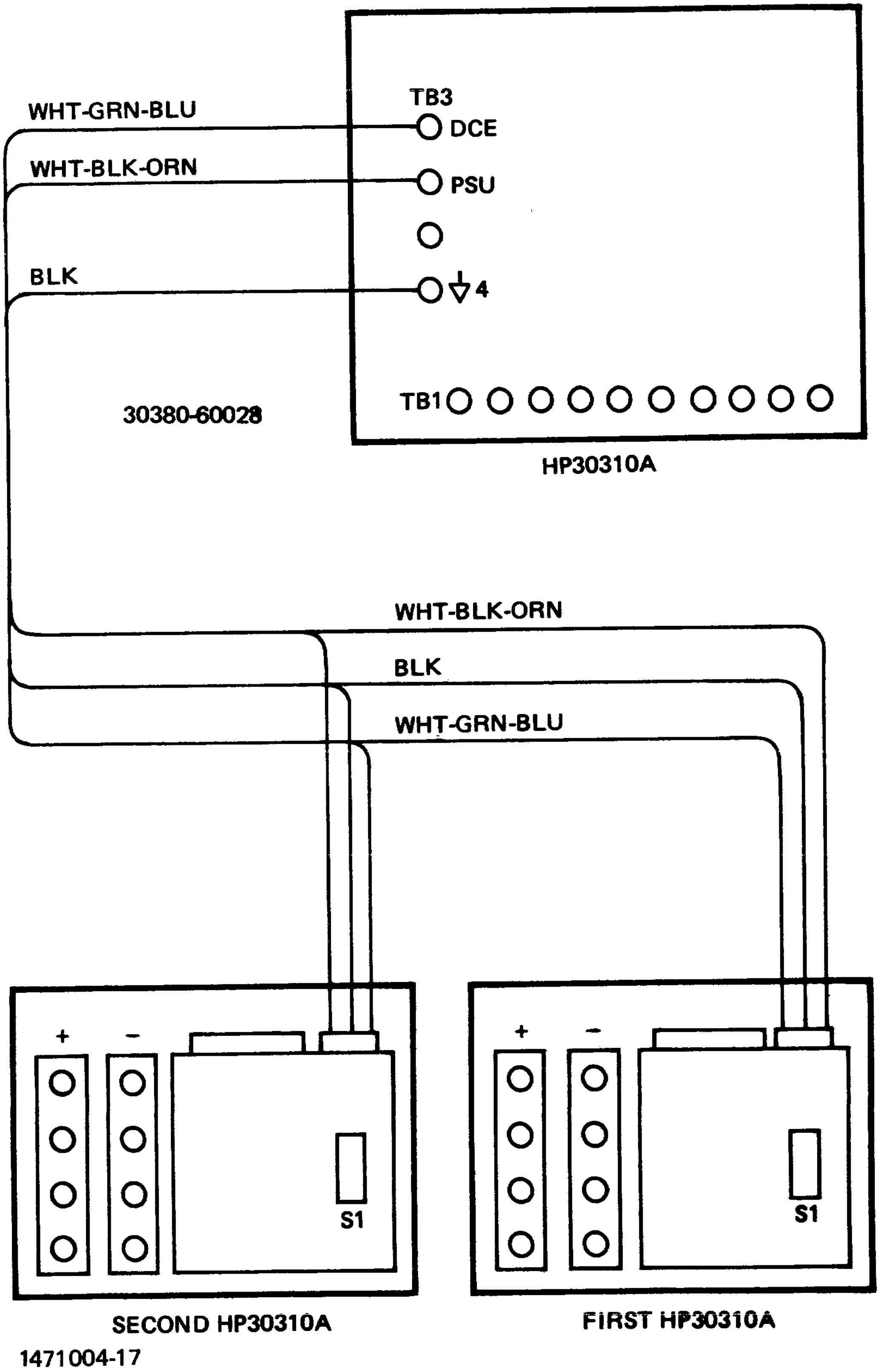
> Both HP 30312A Power Supplies are mounted side-by-side.



CPU BAY (side view)



PIO BAY (side view) WITH ADDITIONAL I/O OPTION



DC POWER CONTROL SIGNALS FOR HP 3000 SERIES I

POWER REQUIREMENTS

LINE VOLTAGE:	208V ac ±10%, 3-phase, 5A, or 230V to 240V ac ±10%, 1-phase, 5A
LINE FREQUENCY:	47.5 to 66 Hertz
POWER CONSUMPTION:	830 watts (1000 volt-amperes), maximum

POWER CABLE (CONNECTED TO AC LINE)

LENGTH:	5 feet (152.4 centimeters)
CONNECTOR:	CEE 22 Type VI (for ac line) CEE 22 Type V (for power supply)

DC SUPPLY VOLTAGES AND CURRENTS

+20V ±1%, 7.5A*
+15V ±5%, 2.5A
+5V ±5%, 55.0A
-5V ±5%, 6.0A
-15V ±5%, 2.5A
-20V ±1%, 1.0A*

ENVIRONMENTAL LIMITS

AMBIENT TEMPERATURE RANGE:	Operating: 0° to 55°C (32° to 131°F) Non-operating: -40° to 75°C (-40° to 167°F)
RELATIVE HUMIDITY:	50 to 95% at 25°C to 40°C (77° to 104°F) without condensation
ALTITUDE:	Operating: 15,000 feet (4572 meters) Non-operating: 25,000 feet (7620 meters)

VENTILATION

AIR FLOW:	100 cubic feet (2.8317 cubic meters) per minute
HEAT DISSIPATION:	2550 BTU's (642.549 kilocalories) per hour, maximum

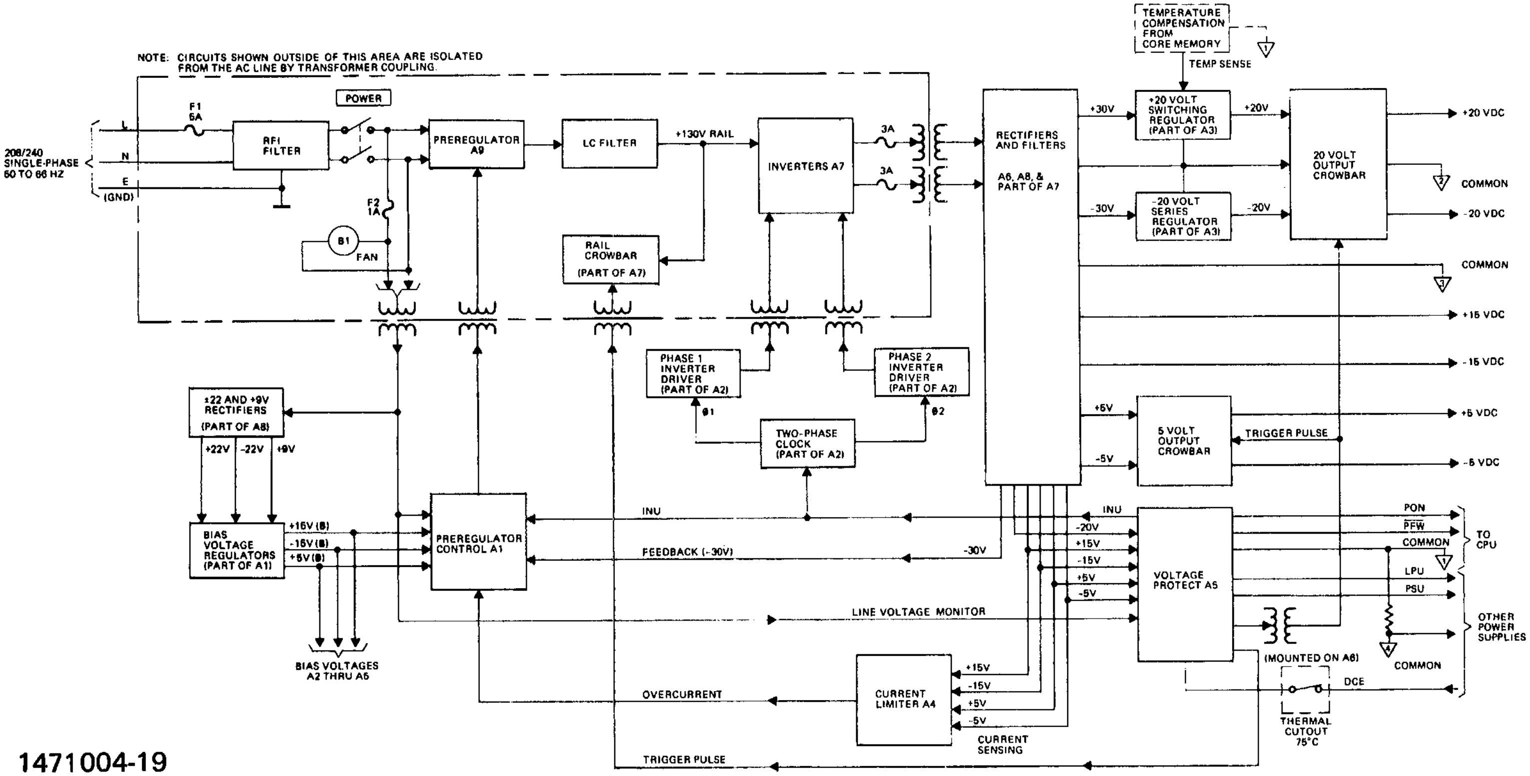
WEIGHT AND DIMENSIONS (See figure 1-2.)

WEIGHT:	50 pounds (22.7 kilograms)
HEIGHT:	8.875 inches (225.4 millimeters)
WIDTH:	19.0 inches (482.6 millimeters)
DEPTH:	10.22 inches (259.5 millimeters)

*Temperature compensation resistor provides negative regulation of -0.26%/°C.

1471004-18

Table HP 30310A, POWER SUPPLY SPECIFICATIONS



1471004-19

HP 30310A POWER SUPPLY BLOCK DIAGRAM

DC Output Voltages

VOLTAGE TEST POINT	MINIMUM READING	MAXIMUM READING	RIPPLE VOLTAGE TOLERANCE
+20	(See Miscellaneous Section)		
+15	+14.2	+16.7	0.4 VOLT PEAK-PEAK
+5	SET AT +5.10 VOLTS		0.3 VOLT PEAK-PEAK
-5	-4.4	-5.3	0.3 VOLT PEAK-PEAK
-15	-14.2	-16.7	0.4 VOLT PEAK-PEAK
-20	(See Miscellaneous Section)		

HP 30310A ADJUSTMENTS

PREREGULATOR ADJUSTMENT

The +15, +5, -15 volt supply outputs are controlled by preregulator adjustment resistor A1R1 (+5, +15V ADJ) on the preregulator control PCA. If one or more of these voltages were not within tolerance when the voltage check was made, the preregulator should be adjusted as described in the following paragraphs.

The procedure consists of adjusting the preregulator until the +15, +5, -5, and -15 volt outputs are within tolerance. The procedure is as follows:

a. Set the power supply POWER switch to the ON position. Verify that there is no computer program running.

b. Connect the voltmeter to the +5V and COM on the PCA cage backplane. While observing the voltmeter, adjust the +5 +15, +15V ADJ resistor (A1R1) until the +5 volt output is within the limits specified in the DC Output Voltages table above.

c. Using the same COM as a return, connect the voltmeter, in turn, to the +15V, -5V, and -15V test jacks and verify that each output is within the limits specified in the DC Output Voltages table. If any voltage is not within the specified limits, readjust resistor A1R1 until a proper reading is obtained. Then check the other voltages to ensure that they remain within the limits.

d. Start the computer program (any program may be used) and verify that all voltages are within specified limits. If any voltage exceeds the lower limits, readjust resistor A1R1 until all voltages are within limits.

e. Repeat steps "a" through "d" until the voltages remain the same under normal load and minimum load conditions without further adjustment of resistor A1R1.

f. Set the power supply POWER switch to OFF and disconnect the voltmeter.

20-VOLT SUPPLY ADJUSTMENT

(See "Memory Schmoo" in MISCELLANEOUS Section)

OVERCURRENT ADJUSTMENT

(See the power supply manual)

TROUBLESHOOTING

Troubleshooting in the field is limited to visual checkout, voltage checks, alignment if necessary, and, if the system is still down, replacement of the entire power supply. Proceed as follows:

a. Open the read door of the cabinet and observe that the POWER switch is set to ON and that the indicator is lit. If the switch is ON but the indicator is out, the indicator is bad or the AC input power is not available to the power supply. Check the fuse.

b. Observe that the +5 volt red indicator is lighted. If it is not, check that the DCE signal at terminal TB3 is low and that the indicator is good.

c. Check the output voltages of the power supply at the test points furnished on the front panel. If the voltages are not correct, follow an appropriate alignment procedure.

d. If the power supply remains down or does not respond to alignment, replace the power supply.

VOLTAGE PROTECT PCA ADJUSTMENT (emergency adjustments only)

The purpose of this procedure is to check and if necessary adjust the +4.30 volt reference supply and line voltage monitor circuits on the A5 voltage protect PCA for proper operation.

PROCEDURE. The procedure for adjusting the reference voltage and line voltage monitor circuits is as follows:

a. Set POWER switch to ON position.

b. Connect voltmeter to terminal (E1(+) and E2(-, COMMON 1) on A5. Adjust A5R2 until voltmeter reads +4.30, +-0.01 volts dc.

c. Use multimeter to insure that both PON and "not" PFW are at a high level (+4 volts dc, minimum).

d. Adjust A5R1 so that the "not" PFW voltage drops to zero, then adjust A5R1 an additional 1/2-turn in the other direction. This adjustment allows "not" PFW to go low at approximately 175 volts AC.

NOTE

Each time "not" PFW goes low, the circuit must be reset.

INPUT:
104-127Vac, single phase, 48-63Hz. See Option 106.

OUTPUT:
See chart, Page 1-1.

LOAD REGULATION:
Less than 0.05% for a load current change equal to the current rating of the supply.

LINE REGULATION:
Less than 0.05% for any change within the specified input voltage rating.

RIPPLE AND NOISE:
Models 62605L, 62605M: Less than 15mVrms and 50mV p-p (20Hz to 20MHz).
Model 62615M: Less than 15mVrms and 65mVp-p (20Hz to 20MHz).

TEMPERATURE RANGES:
Operating: 0 to 40°C ambient. Output current derated linearly for temperatures greater than 40°C.
Storage: −55°C to +85°C.
Cooling: Built-in fan.

TEMPERATURE COEFFICIENT:
Less than 0.02% output voltage change per degree Centigrade over the operating range from 0 to 40°C at constant load and line voltage after 30 minutes warmup.

THERMAL PROTECTION:
Heat sink mounted thermostat shuts-off output if supply overheats due to high ambient temperature. Thermostat automatically opens when temperature cools to safe operating level.

STABILITY:
Less than 0.1% total drift for 8 hours after an initial warm-up time of 30 minutes at constant ambient, constant line voltage, and constant load.

LOAD TRANSIENT RECOVERY:
Output voltage returns to within 1% of nominal in less than 600μsec (62605M) 500μsec (62605L) or 300μsec (62615M), following a full to half load change.

CURRENT LIMIT PROTECTION:
Screwdriver adjustment, factory set to approximately 105% of rated current maximum. Current is cutback to approximately 70% under short circuit conditions. Minimum adjustment range is approximately 75 to 107% of rated output current.

OVERVOLTAGE PROTECTION:
Trip Level: The trip voltage is fixed at 120 ±6% of nominal output voltage.
Trip Input: A contact closure between terminals A1 and +S can be used to remotely trip the overvoltage circuit.
Trip Output: The potential across terminals A1 and +S falls to approximately 0.8V when the overvoltage circuit trips.

VOLTAGE CONTROL:
Screwdriver adjustment accessible through hole in front panel. Minimum adjustment range is ±5%.

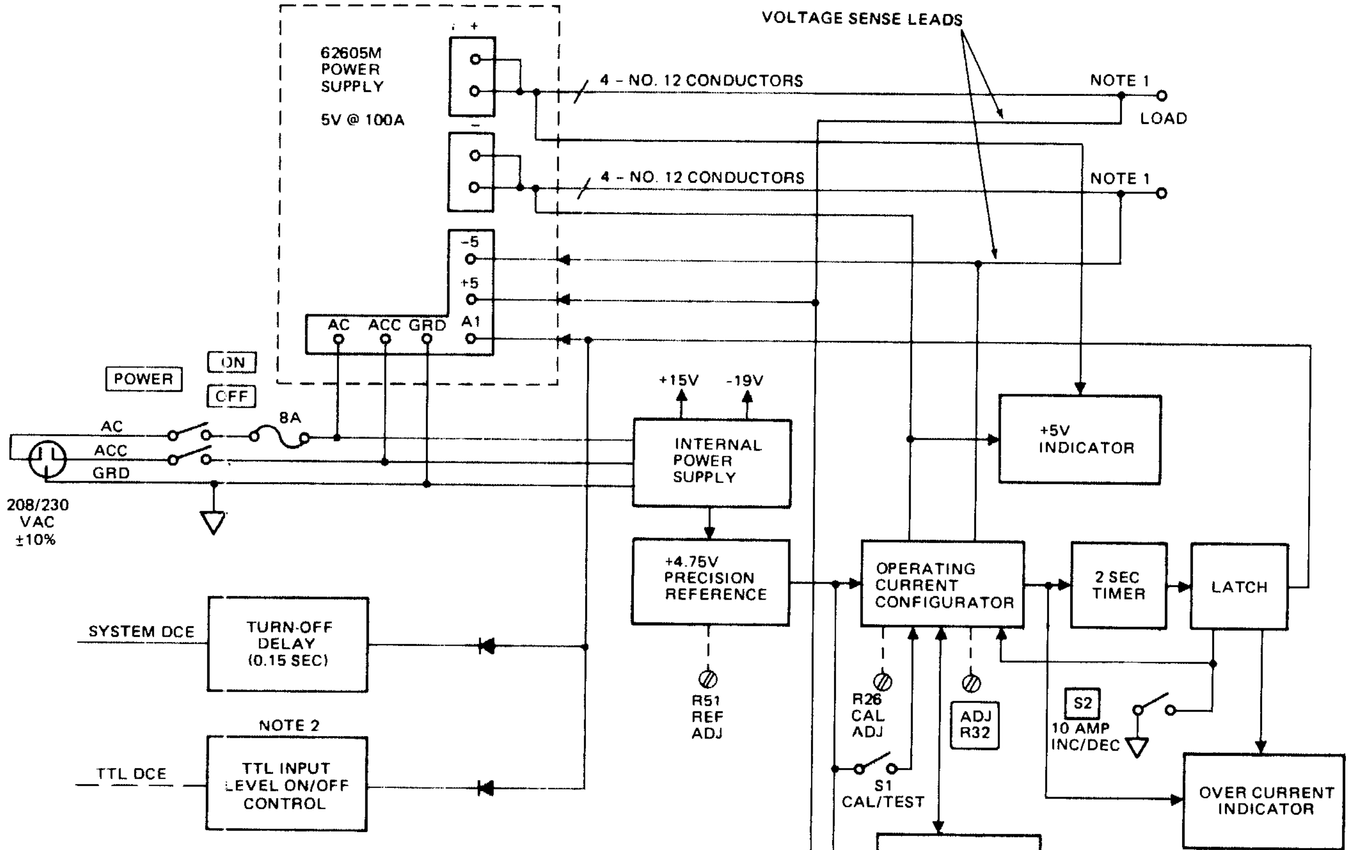
REMOTE SENSING:
Separate remote sensing terminals are provided which will correct for load lead voltage drops of up to 0.25V total (Models 62605M, 62605L) or 0.75V total (62615M). Load is protected if sensing terminals are inadvertently opened.

DIMENSIONS:
Refer to Figure 2-1.

WEIGHT (net/shipping):
14 lbs. (6.4kg)/18 lbs. (8.2kg)

1471004-19a

AC–DC POWER SUPPLY SPECIFICATIONS

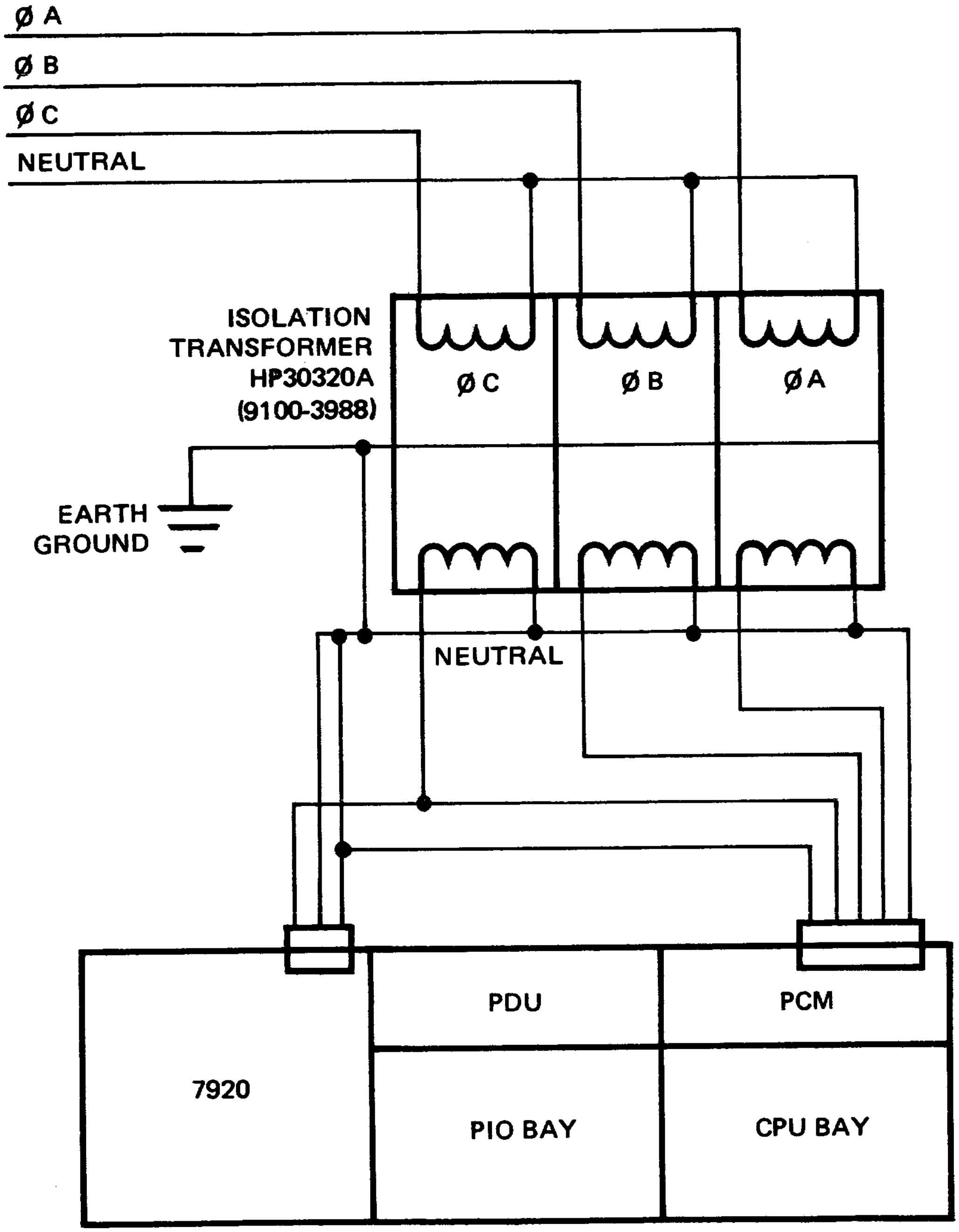


NOTES:

1. THIS CONNECTION PHYSICALLY LOCATED AT THE END OF THE NO. 12 AWG CONDUCTORS
2. THIS CIRCUIT NOT USED IN THE HP 3000 COMPUTER SYSTEM.

1471004-20

HP 30312A SUPPLY SIMPLIFIED BLOCK DIAGRAM



NOTE:

NEUTRAL ON SECONDARY SIDE OF TRANSFORMER AND CASE MUST BE CONNECTED TO SEPARATE EARTH GROUND, THE 7920IS CONNECTED TO PHASE C AND NEUTRAL IN ORDER TO BETTER BALANCE THE CURRENT DRAW ON EACH PHASE.

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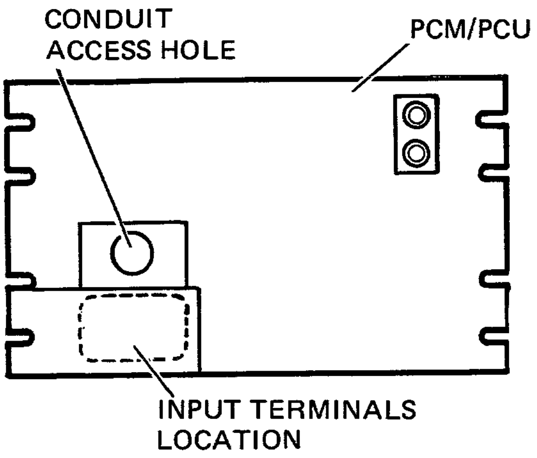
INPUT POWER CONNECTIONS WITH 12.6 KVA ISOLATION

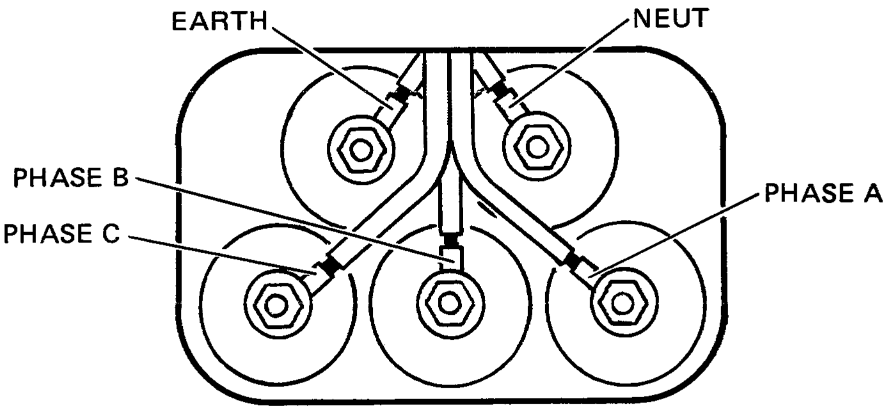
TROUBLE ISOLATION

If the +5 volt output is absent, disconnect the wire at terminal A1 of the HP 30312A Power Supply. If the +5 volts is restored, the interface PCA is defective; if the +5 volts is not present, the HP 30312A Power Supply is defective.

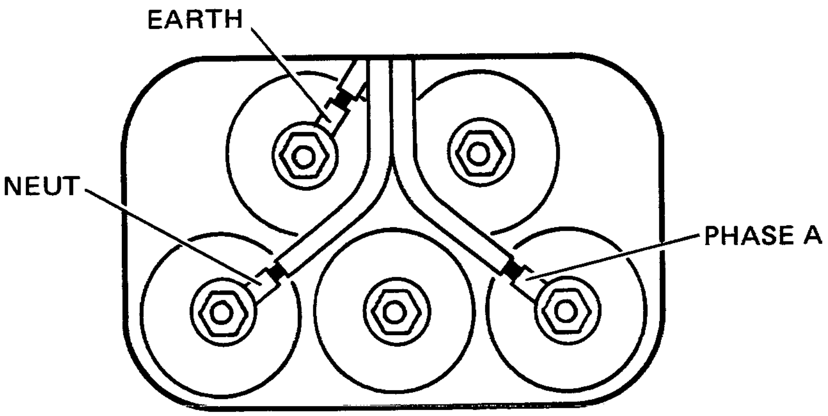
NOTE

> Neutral on secondary side of transformer and case MUST be connected to separate earth ground. The 7920 is connected to phase C and neutral in order to better balance the current draw on each phase.





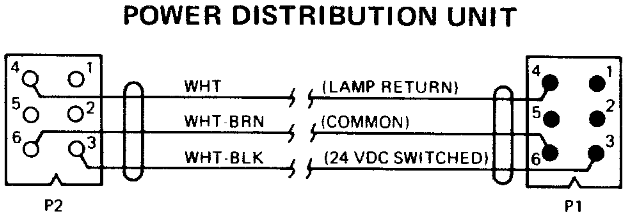
A. OPTION 002



B. OPTION 015

1471004-22

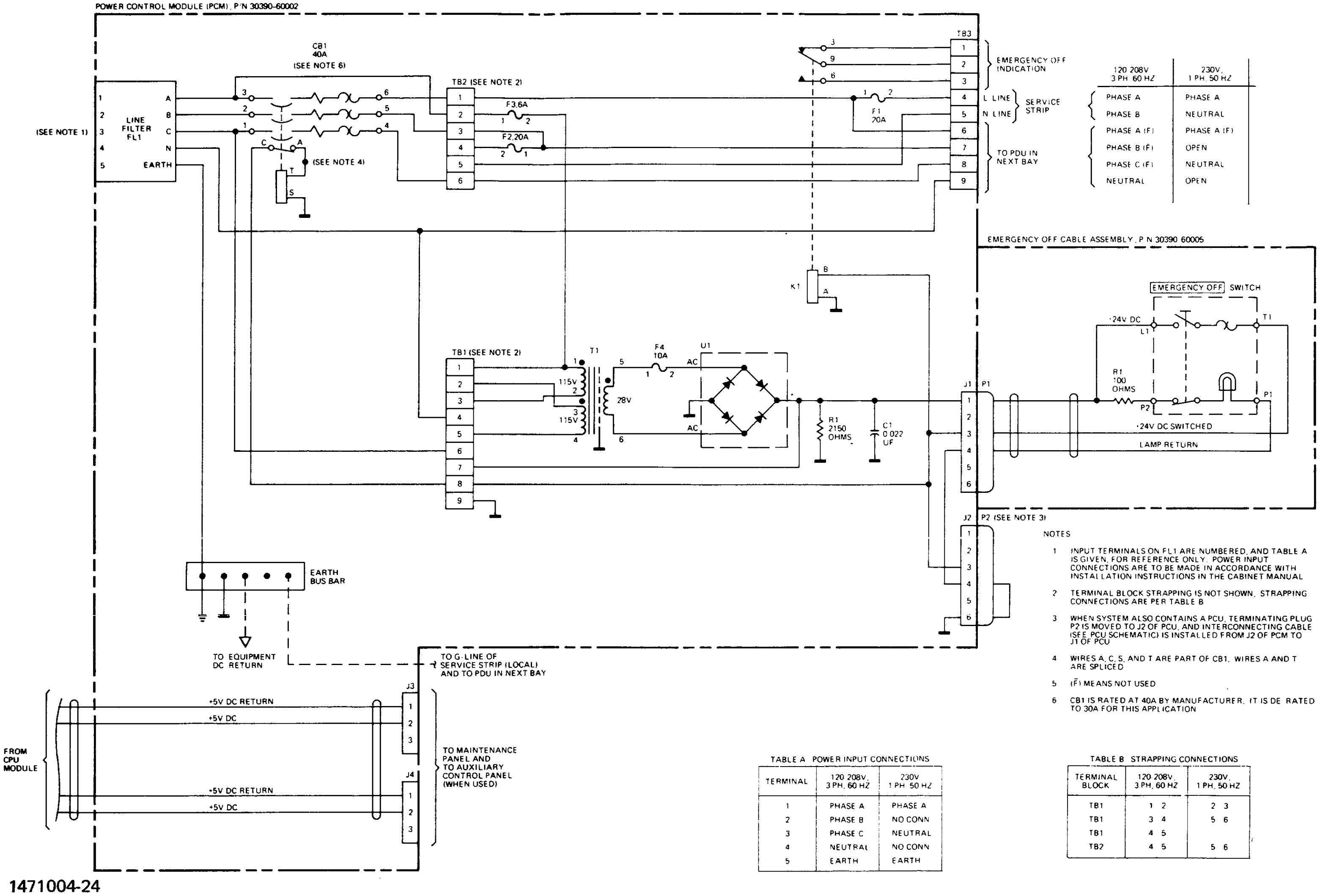
LINE FILTER POWER INPUT CONNECTIONS



PCU-to-PCU/PCM Interconnecting Cable

1471004-23

PCU-to-PCU/PCM INTERCONNECTING CABLE



120 208V 3 PH 60 HZ	230V, 1 PH, 50 HZ
PHASE A	PHASE A
PHASE B	NEUTRAL
PHASE A (F)	PHASE A (F)
PHASE B (F)	OPEN
PHASE C (F)	NEUTRAL
NEUTRAL	OPEN

1471004-24

NOTES

1 INPUT TERMINALS ON FL1 ARE NUMBERED, AND TABLE A IS GIVEN, FOR REFERENCE ONLY. POWER INPUT CONNECTIONS ARE TO BE MADE IN ACCORDANCE WITH INSTALLATION INSTRUCTIONS IN THE CABINET MANUAL

2 TERMINAL BLOCK STRAPPING IS NOT SHOWN. STRAPPING CONNECTIONS ARE PER TABLE B

3 WHEN SYSTEM ALSO CONTAINS A PCU, TERMINATING PLUG P2 IS MOVED TO J2 OF PCU, AND INTERCONNECTING CABLE (SEE PCU SCHEMATIC) IS INSTALLED FROM J2 OF PCM TO J1 OF PCU

4 WIRES A, C, S, AND T ARE PART OF CB1. WIRES A AND T ARE SPLICED

5 ($\bar{F}$) MEANS NOT USED

6 CB1 IS RATED AT 40A BY MANUFACTURER. IT IS DE RATED TO 30A FOR THIS APPLICATION

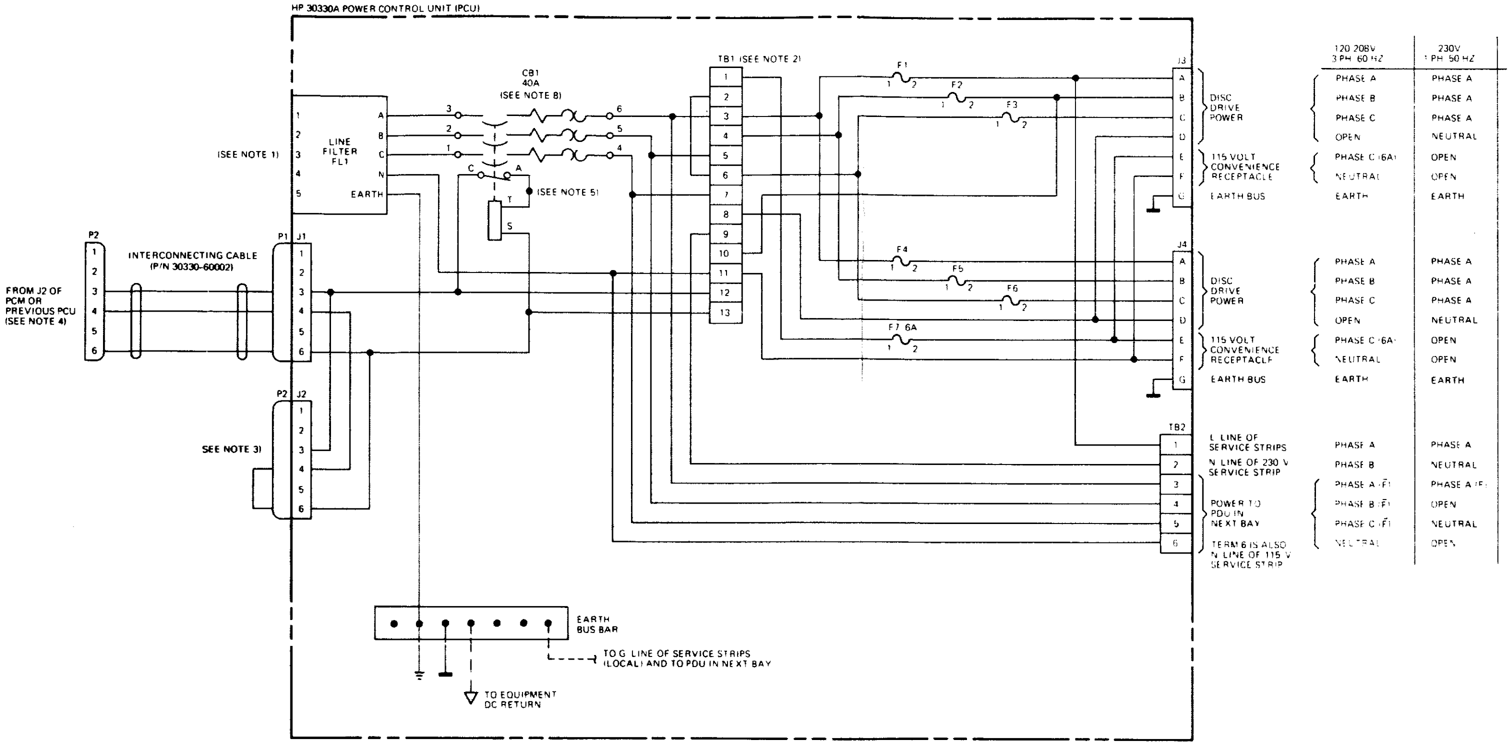
TABLE A POWER INPUT CONNECTIONS

TERMINAL	120 208V, 3 PH, 60 HZ	230V 1 PH 50 HZ
1	PHASE A	PHASE A
2	PHASE B	NO CONN
3	PHASE C	NEUTRAL
4	NEUTRAL	NO CONN
5	EARTH	EARTH

TABLE B STRAPPING CONNECTIONS

TERMINAL BLOCK	120 208V, 3 PH, 60 HZ	230V, 1 PH, 50 HZ
TB1	1 2	2 3
TB1	3 4	5 6
TB1	4 5	
TB2	4 5	5 6

30390-60002
POWER CONTROL MODULE (PCM)



NOTES

1. INPUT TERMINALS ON FL1 ARE NUMBERED, AND TABLE A IS GIVEN FOR REFERENCE ONLY POWER INPUT CONNECTIONS ARE TO BE MADE IN ACCORDANCE WITH INSTRUCTIONS IN THE CABINET MANUAL
2. TERMINAL BLOCK STRAPPING IS NOT SHOWN STRAPPING CONNECTIONS ARE PER TABLE B
3. TERMINATING PLUG P2 OBTAINED FROM J2 OF PCM OR NEIGHBORING PCU
4. P2 OF INTERCONNECTING CABLE MATES WITH J2 OF PCM OR NEIGHBORING PCU
5. WIRES A, C, S, AND T ARE PART OF CB1 WIRES A AND T ARE SPLICED
6. FUSES F1 THRU F6 ARE RATED 20A
7. (F̄) MEANS NOT FUSED
8. CB1 IS RATED 40A BY MANUFACTURER IT IS DE RATED TO 30A FOR THIS APPLICATION
9. NOT USED WHEN PCU IS BEING USED TO POWER DISC DRIVES

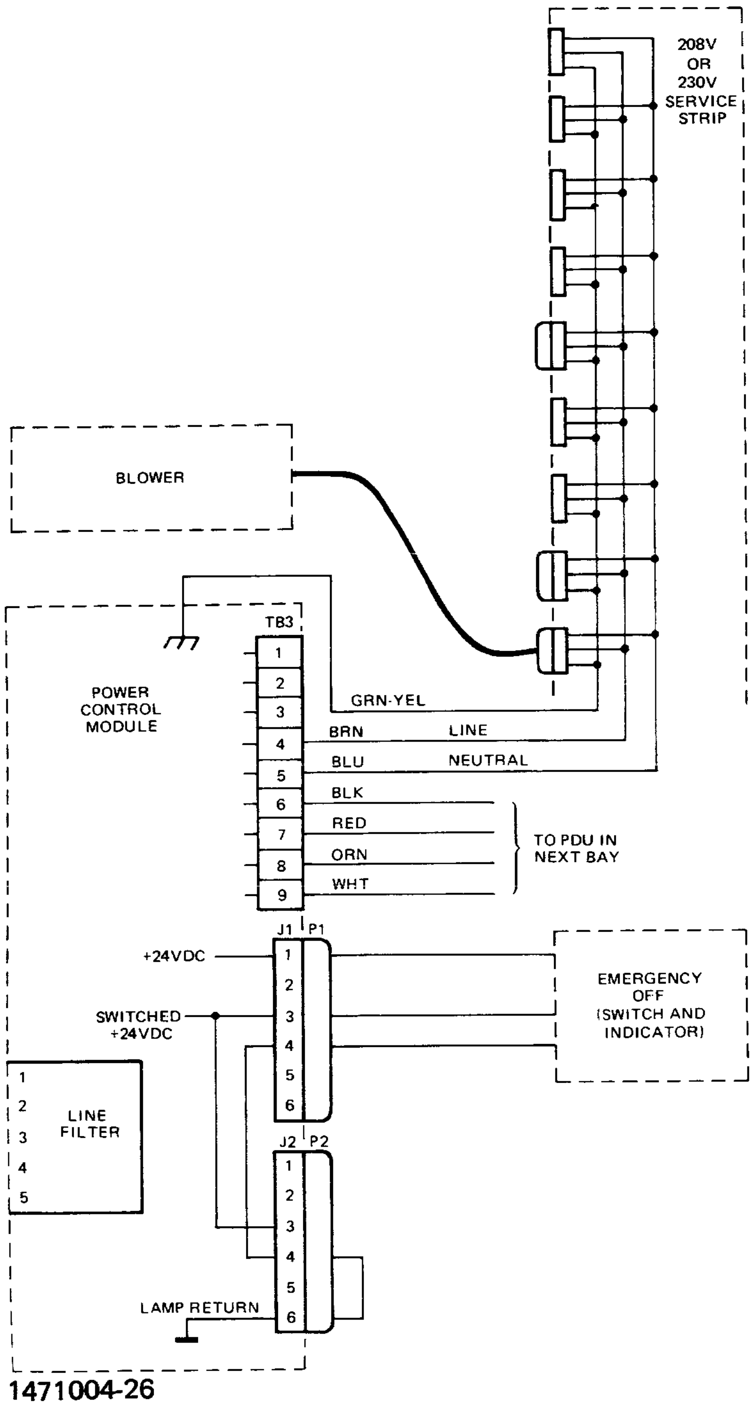
TABLE A POWER INPUT CONNECTIONS

TERMINAL	120 208V 3 PH 60 HZ	230V 1 PH 50 HZ
1	PHASE A	PHASE A
2	PHASE B	NO CONN
3	PHASE C	NEUTRAL
4	NEUTRAL	NO CONN
5	EARTH	EARTH

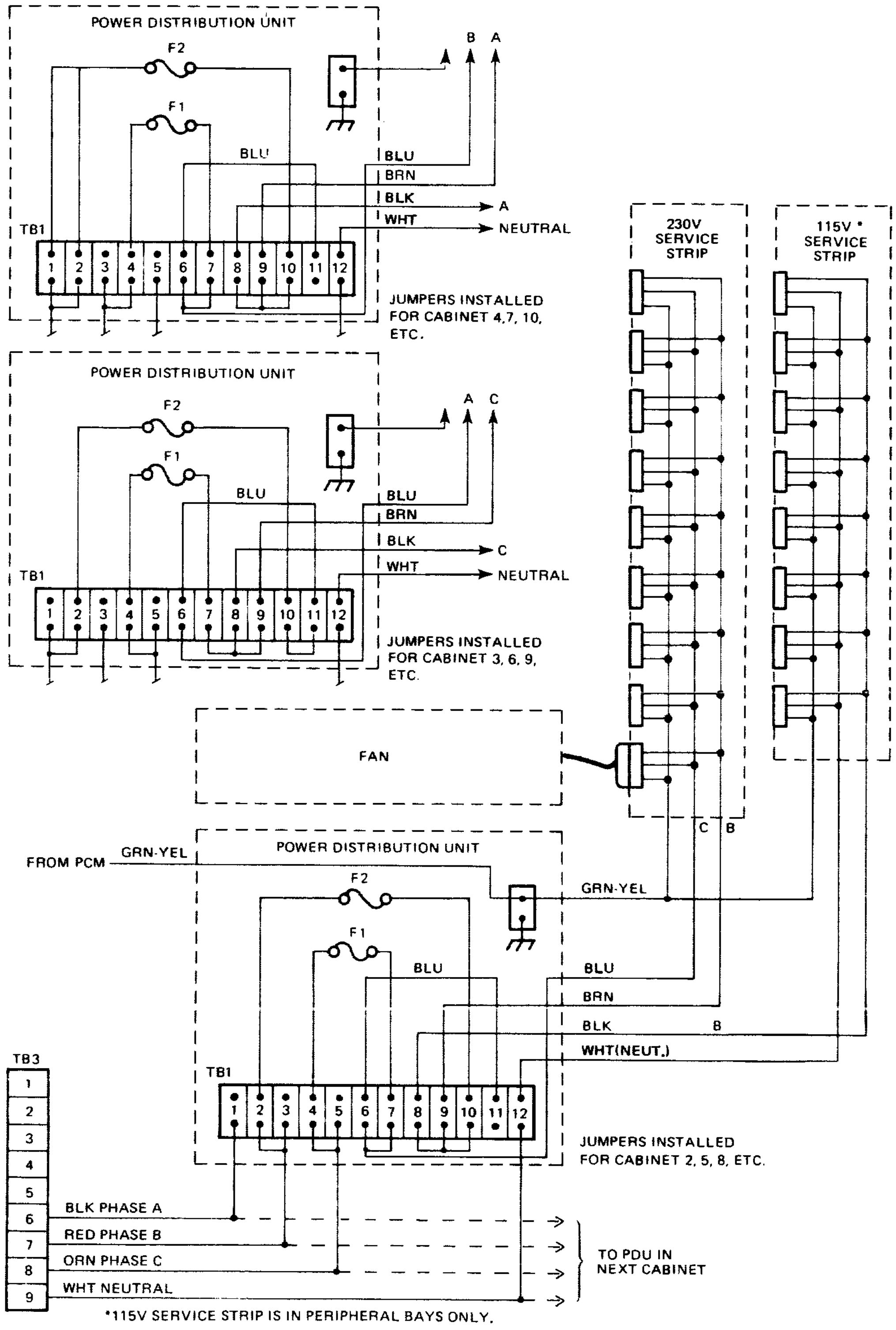
TABLE B STRAPPING CONNECTIONS

TERMINAL BLOCK	120 208V 3 PH 60 HZ	230V 1 PH 50 HZ
TB1	1 2	2 3
TB1	4 5	3 4
TB1	6 7	7 8
TB1	9 10	8 9

30330A POWER CONTROL UNIT (PCU)

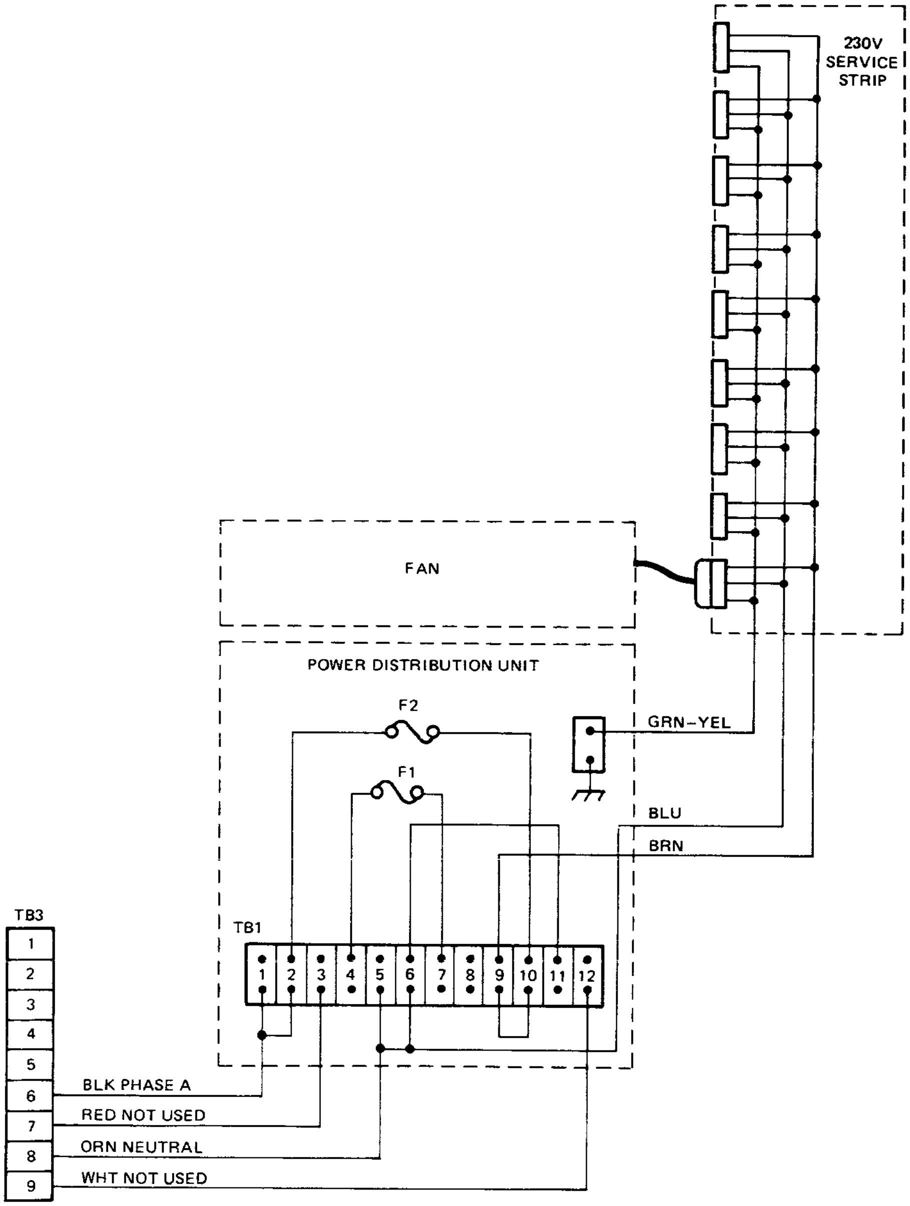


AC DISTRIBUTION, CPU CABINET



1471004–27

AC DISTRIBUTION, AUX. CABINETS (120/208V, 60 Hz)



1471004-28

AC DISTRIBUTION, AUX. CABINETS (230V, 50 Hz)

PDU Straps Connections at TB-1

AC Input Voltage

120/208 V, 3 PH, 60 Hz		230V, 1 PH, 50 Hz	
Bay Number (counted from rear left)	pin to pin	Bay Number (counted from rear left)	pin to pin
2,5,8, . . .	2-3 4-5 6-7 8-9 9-10	2,3,4, . . .	1-2 5-6 9-10
3,6,9, . . .	1-2 4-5 7-8 8-9 10-11	N/A	N/A
4,7,10,. . .	1-2 3-4 6-7 8-9 9-10	N/A	N/A

N/A = Not Applicable

PCU Straps Connections at TB-1

AC Input Voltage

120/208 V, 3 PH, 60 Hz	230V, 1 PH, 50 Hz
1 to 2	2 to 3
4 to 5	3 to 4
6 to 7	7 to 8
9 to 10	8 to 9

PDU to PCM Connections

Wire Color	PDU at TB1	PCU at TB2
black	1	3
red	3	4
orange	5	5
white	12	6
green-yellow	Earth Bus	Earth Bus

COLD-LOAD

COLD-LOAD

SECTION III

HP 3000 PRE-SERIES II COLD-LOAD

The micro-code builds the following SIO cold-load program in memory whenever the Cold-Load Switch is depressed, as shown on the next page.

```
                     0         7 8        15
                     ----------------------
       B-Register    | COMMAND  |  DEVNO  |
                     ----------------------



                     ----------------------       )
                     |        *+1         | ---   |
       (DEVNO*4)     ----------------------   |   |
                                              |   |
                     ----------------------   |   |
                     |       040000       | <--   |
                     |--------------------|       >  DRT FOR DEVNO
                     |    0     | COMMAND |       |
                     ----------------------       |
                                                  |
                     ----------------------       |
                     |       077740       |       |
                     |--------------------|       )
                     |        *+1         | --|
                     ---------------------- . |
                                              |
                  (  ----------------------   |
                  |  |       XXXXXX       | <--
                  |  |--------------------|
                  |  |       XXXXXX       |
                  |  ----------------------
                  |  .                    .
    32 WORDS      |  .                    .
  READ IN FROM    <  .   14 ORDER PAIR    .
  DISC OR TAPE    |  .                    .
                  |  .                    .
                  |  ----------------------
                  |  |       034000       |
                  |  |--------------------|
                  |  |       000000       |
                  (  ----------------------
```

The micro-code then issues an SIO command to the DEVNO in B-Register (8-15) and goes into a loop waiting for an external interrupt from the selected device controller. Then the Cold-Load routine sets up the PB, and PL registers. Memory location 1 contains the address for P. Then DL, DB, Q, S, and Z are also set up and the micro-code returns to the Halt loop.

First, verify that the CPU correctly built the Cold-Load program correctly in memory.

Second, use the cold-load analyzer PCA, part no. 30000-60004, to establish the extent of the I/O progression following the cold load.

```
                    LABL RBUS SBUS FUNC SHFT STOR SPEC SKIP      COMMENTS

                    *
                    *    COLD LOAD
                    *
1725  37777777777   COLD           ADD                           COLD LOAD ENTRY
1726  37776777037                  INC            CCPX           PUT MACHINE IN RUN STATE
1727  07537774777             SWCH ADD  RRZ  SP3                 COLD LOAD
1730  16137772756        UBUS UBUS ADD  SL1  BSP0 CWA            AT DEVICE # * 4.
1731  16176777777             UBUS INC       DATA                PUT * + 1
1732  37136777755        SP0       INC       BSP0 CWA            AT D+1
1733  37171640000                  ROM       DATA 040000         PUT IOCW (CONTROL)
1734  37136777755        SP0       INC       BSP0 CWA            AT D+2
1735  07177770777             SWCH ADD  LRZ  DATA                PUT CNNTROL WORD
1736  37136777755        SP0       INC       BSP0 CWA            AT D+3
1737  37171677740                  ROM       DATA 077740         PUT IOCW (READ 32)
1740  37136777755        SP0       INC       BSP0 CWA            AT D+4
1741  16176777457             UBUS INC       DATA CF1            PUT IOAW (*+1)
1742  37511740006                  ROM       STA  140006         SET STATUS
1743  25531301000             SP3  ROM1      SP3  101000         FORM SIO CMD
1744  37722363540                  JSB  CIOP SP2       UNC       AND SEND TO DEVICE
1745  04761600200   CLD1      CPX1 ROMN           000200
1746  16766001745             UBUS JMP  CLD1 .         ZERO      WAIT FOR EXTERNAL INTERRUPT
1747  16777777037             UBUS ADD            CCPX           CLEAR INTERRUPT
1750  11317777437             IOA  ADD       SP1  CF2            SEE WHO IT WAS
1751  16531302000             UBUS ROM1      SP3  102000         FORM RIL CMD
1752  37762363540                  JSB  C1OP           UNC       SEND TO DEVICE
1753  07763374774        SP1  SWCH XOR  RRZ                      COLD LOAD DEVICE NUMBER ?
1754  16766011745             UBUS JMP  CLD1           NZRO      GO BACK AND WAIT IF NOT
1755  37116777777                  INC       BUSL RWA
1756  37757777177                  ADD       PB   CF3            PB = 0
1757  26417777777             OPND ADD       P                   P ← (A1)
1760  05136774777             MOD  INC  RRZ  BSP0 RWA
1761  37227377777                  CAD       PL                  PL = 2**16 - I
1762  26437777777             OPND ADD       Q                   Q = QI
1763  37116777775        SP0       INC       BUSL RWA
1764  21456777777             Q    INC       SM                  S = Q+1
1765  37477777777                  ADD       DB                  DB = 0
1766  37717777117                  ADD       DL   SIFG           DL = 0
1767  26246362735             OPND JMP  WAIT Z         UNC       Z = ZI GO TO HALT STATE
                    *
                    *
                    *

                    *
                    *    CIOP IS A ROUTINE THAT DOES THE CPU - IOP COMMUNICATION
                    *
3540  37766173543   CIOP           JMP  CP1            NF2       F2 MEANS OUTBOUND TRANSFER
3541  35772377777             SP2  REPC
3542  16057547777             UBUS ADD       IOD       F1        XFER DATA
3543  25772377777   CP1       SP3  REPC
3544  16037547777             UBUS ADD       IOA       F1        XFER COMMAND
3545  37772377437                  REPC           CF2
3546  25777747457             SP3  ADD            CF1  F3        WAIT FOR COMPLETION
3547  12737777177             IOD  ADD       SP2  CF3            UNLOAD IOD
3550  06761600040             CPX2 ROMN           000040
3551  16777417777             UBUS ADD                 NZRO      I/O TIMEOUT ?
3552  37777707777                  ADD                 RSB       NO. RETURN
3553  37777707417                  ADD            SF2  RSB       YES. SET F2 AND RETURN
```

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MICRO-CODE COLD-LOAD

COLD-LOAD ANALYZER PCA

DESCRIPTION:

The cold load analyzer PCA, part no. 30000-60004, is an I/O type PCA that monitors certain signals on the IOP, MUX CHAN, and SEL CHAN buses. The signals are latched and will sequentially light six LED´s located near the front of the PCA, when a good Cold-Load operation is recognized.

FUNCTION:

A Cold-Load operation is divided into six progressive steps. The successful completion of each step is latched and will light its respective LED. A good Cold-Load will therefore light all six LED´s.

OPERATION:

To operate, insert the cold load analyzer PCA into any polled or unpolled slot on the MUX CHAN bus to analyze any device controller the MUX CHAN bus or into any polled or unpolled slot on the SEL CHAN bus to analyze any device controller on the SEL CHAN bus. Load the switch register with the DEVNO and a Cold-Load Read command for the failing device controller. Depress I/O reset, CPU reset, and Cold-Load switches.

Each successful step will light its respective LED. The first LED that does not light points to the failing step. For example, if when analyzing a mag tape cold-load problem only the first two LED´s light, then the first LED not to light would indicate that the SIO MUX is not functioning properly.

The cold load analyzer PCA was initially designed to aid in troubleshooting 7905A/7920A disc subsystem problems. The complexity of the Port Controller, Selector Channel, and Disc Controller presents up to eight separate PCA´s that have to be tested at full speed. The decision of where to begin is made easier with the help of the cold-load analyzer PCA.

MAINTENANCE:

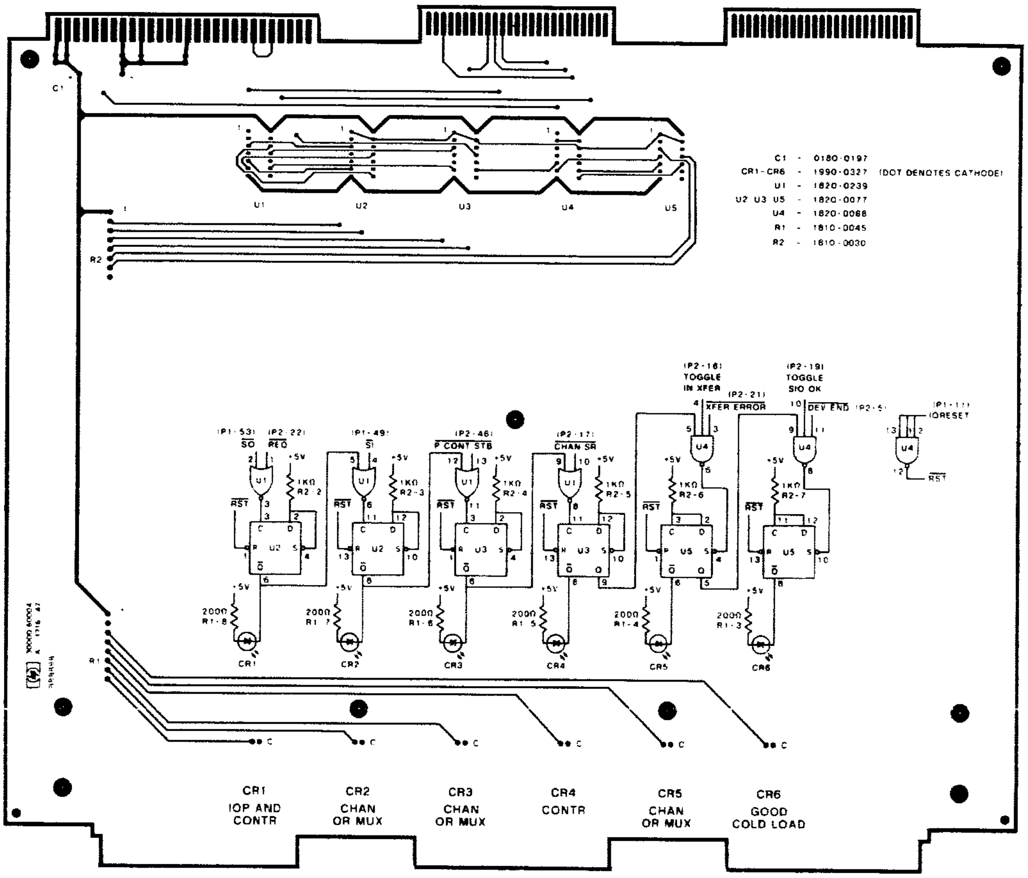
The cold-load analyzer PCA has its schematic diagram etched on its component side. All components are coded for ease of identification. The HP part numbers are listed in the upper right-hand corner. Troubleshooting is made easy by cold-loading a known good device controller and following the flow of events with a logic probe or oscilloscope.

Each LED can be individually tested by momentarily grounding the cathode (c) while the PCA is inserted into any DIO/SIO slot.

OPERATIONAL DESCRIPTION

LED	DEVICE	OPERATION
1	IOP	Issue SO, SIO command, and DEVNO word to all device controllers.
	DEV CONTR	Recognize DEVNO in SIO command word and issue REQ to the SIO MUX or SEL CHAN.
2	SIO MUX or SEL CHAN	Issue SI to the IOP in response to REQ and request the device controller to place its DEVNO*4 on the IOP or SEL CHAN bus. Begin DRT fetch operation.
3	SIO MUX or SEL CHAN	Inform the device controller that the IOAW is on the IOP or SEL CHAN bus.
4	DEV CONTR	Acknowledge receipt of the Cold-Load Read command and Unit Number. Inform SIO MUX or SEL CHAN to fetch next I/O doubleword order pair.
5	SIO MUX or SEL CHAN	Toggle INXFER to signal the device controller to begin sending data to memory.
	DEV CONTR	Place 16 bit DATA word on the IOP or SEL CHAN bus until EOT is received from the IOP, SIO MUX, or SEL CHAN.
	SIO MUX or SEL CHAN	Count DATA words received and issue EOT when count is reached. Continue fetching I/O doubleword order pairs until END order with interrupt is received.
6	SIO MUX or SEL CHAN	Inform device controller to interrupt CPU.
	DEV CONTR	Issue INT REQ to IOP.
	SIO MUX or	Issue TOGGLE SIO OK signal to device controller.

All LED´s lighted indicate a good cold-load, otherwise the data the device was incofrom rrect or absent.



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COLD-LOAD ANALYZER PCA

DIAGNOSTICS

CONFIGURING STAND-ALONE DIAGNOSTICS

Log on the system as follows:

```
:HELLO FIELD.SUPPORT,HPOFFLN;TERM=[TERM TYPE]

:RUN SDUP;NOPRIV

> Enter 1  << to create a CPU diagnostic tape >>
  Enter 2  << to create a non-CPU diagnostic tape >>
  Enter /  << to terminate SDUP >>

                        << IMPORTANT >>

      All other inputs not specified above are illegal and
      may prematurely abort the SDUP program.

> 1  << to create a CPU diagnostic tape >>
> Program Name? PD320A
> Program Name? PD320A1
> Program Name? PD320A2
> Program Name? PD320A3
> Program Name? PD320A4
> /  << to terminate SDUP >>
```

When the tape is completed, SDUP will print the PL address. Write the Program Limit (PL) on the tape label of the CPU diagnostic tape.

If a listing of the CPU diagnostic is required, mount the stand-alone source tape (30000-1X005) and perform the following:

```
:HELLO FIELD.SUPPORT,HPOFFLN;TERM=[TERM TYPE]
:FILE T;DEV=TAPE
:RESTORE *T;SD320A,SD320A1,SD320A2,SD320A3,SD320A4;SHOW
```

DIAGNOSTICS

Mount the stand-alone maintenance tape (30000-1X006) and perform the following:

```
  :RESTORE *T;MD320A,MD320A1,MD320A2,MD320A3,MD320A4&
  JD320A,JD320A1,JD320A2,JD320A3,JD320A4;SHOW
  :STREAM JD320A,JD320A1,JD320A3,JD320A4
```

CPU DIAGNOSTIC LEVELS (Order on tape)

FILE NAME	LEVEL	SECTION
PD320A	03.0	1
PD320A1	03.0	2
PD320A2	03.0	3
PD320A3	03.0	4
PD320A4	03.0	5

COLD LOAD INSTRUCTIONS
FOR LOADING
A STAND-ALONE CPU DIAGNOSTIC TAPE

1. Mount stand-alone CPU diagnostic tape on logical unit 0.
2. Enter %003006 in SWITCH REGISTER
3. Press CPU RESET, I/O RESET, LOAD
4. Press RUN (except for section 1, see NOTE)
5. Enter program options in SWITCH REGISTER
6. Press RUN

NOTE

To run Section 1, press RUN three times until a HALT 3 appears in the CIR.

Load all even numbers in the SWITCH REGISTER and press RUN until a HALT 4 appears in the CIR.

Load all odd numbers in the SWITCH REGISTER and press RUN until a HALT 5 appears in the CIR.

Go to step 5.

STAND-ALONE NON-CPU DIAGNOSTIC TAPE

The stand-alone diagnostics are not configured for load-and-go operation as on the HP 3000 Series II diagnostic tape. All diagnostics must have B-SWITCH REGISTER bits set to execute each test.

The 7905A cartridge disc diagnostic is the only pre-Series II diagnostic to utilize the Section Register technique employed by all Series II diagnostics. The Section Register may invoke operator action and thus are not entirely load-and-go.

CONFIGURING A NON-CPU DIAGNOSTIC TAPE

```
:RUN SDUP;NOPRIV
>2  << to create a non-CPU diagnostic tape >>
>Program Name? PD321B
>Program Name? PD322A
          .
          .
          .
>Program Name? PD319A
>Enter DRT # for Console?  << Enter 3 >>
>Enter DRT # for Line Printer?  << Enter 0 if unavailable >>
>Program XXXX Any Changes?  << Enter Y or N >>
>DB+Y?  << Enter value between 0 and 7 >>
>(DB+Y) = YYYYYY?  << Enter new contents or CR to keep
                      previous contents >>
          .
          .
          .
>/  << to terminate SDUP >>
```

OFF-LINE DIAGNOSTICS (Order on tape)

1	SLEUTH	PD211A	02.0
2	CART DISC 7905A	PD319A	02.0
3	MEMORY PATTERN	PD321B	00.0
4	MUX CHAN	PD322A	00.0
5	DISC FILE 2888A	PD323A	01.0
6	CART DISC 7900A	PD324A	01.0
7	SYS CLK	PD325A	00.0
10	TELEPRINTER	PD326A	00.0
11	FIXED HEAD DISC	PA328A	02.0
12 *1	SEL CHAN/MUX CHAN	PD329A	00.0
13	TERMINET	PD330A	01.0
14	EXT FLT PT	PD331A	00.0
15	9 TRK MAG TAPE	PD333A	01.0
16 *2	SSLC INTERFACE	PD334A	01.0
17 *3	UI DIAG	PD335A	01.0
20	READER/PUNCH	PD336A	01.0
21	DECIMAL FIRMWARE	PD337A	00.0
	SDUP	D217A	04.0

*1 REQUIRES TEST BOARD HP 30033A

*2 REQUIRES TURNAROUND JUMPER PLUG HP 30055-60005

*3 REQUIRES TEST HOOD HP 30049B

COLD LOAD INSTRUCTIONS
FOR LOADING
NON-CPU DIAGNOSTICS

1. Mount non-CPU diagnostic tape on logical unit 0.
2. Enter %003006 in switch register.
3. Depress CPU reset, I/O reset.
4. Depress cold load.
5. Depress run.
6. Set two fields in switch register as follows:

MEMORY SIZE	BIT		
	0	1	2 thru 15
64K	0	0	Program number
48K to 56K	0	1	Program number
32K to 40K	1	0	Program number

7. Depress run (three times to skip steps 8 and 9).
8. Enter program origin (%4000 or greater).
9. Depress run.
10. Program loads and execution begins.

RUNNING AND CONFIGURING ON-LINE DIAGNOSTICS

Always log on from the system console.

```
:HELLO FIELD.SUPPORT,HPONLN
:RUN SDM
*[type in any command]
```

<< CAUTION >>

Control Y should return control back to the system console. However, it may also crash the system. SDM therefore should only be executed during preventive maintenance times.

SDM can cause system failures, therefore, it is a good idea to COOLSTART after using SDM to ensure proper reloading of MPE after each use.

NOTE

The first two letters of any command are all that is necessary to invoke the command.

```
*NEw MTTEST
*PROGRAM NAME ? PD362A
*DEVICE NUMBER IN DECIMAL ? 6
*SET FLAGS ? 4,5,6,7,8,9,10,17,PE,NA
*DIAGNOSTIC CONFIGURED
*SAve MTTEST
*RUn MTTEST
```

The above will invoke tests 4-10, 17 and will pause after any error and print the UD name (MTTEST) before every message.

= TAKE [LDN] allows spooled devices to be tested on-line.

= GIVE [LDN] returns spooled devices to the system.

SDM SYSTEM COMMANDS, sheet 1 of 2

Command	Parameters	Meaning
ABORT	[<UD name>]	Terminate immediately
BATCH	<fspec>	Batch command input
BRANCH	[UD name>]	Branch on UD resumption
CATALOG	[table][;<ident list>]	List symbol table entries
CLEAR	[<flag list>[;<ident list>]	Clear UD control flags
CONTINUE	[<ident list>]	Continue UD
DEFINE	<ident>=<text>	Define string
END		End batch input
EXIT		Terminate SDM execution
FLAGS	[<ident list>][;<spec>]	List UD control flags
GO	[<ident section list>][;<device>]	Start UD execution
LDEFINES	[<table>][;<fspec>]	List defined strings
LOG	<limit>[;<ident list>]	Log all UD output
NEW	<UD name>	Prepare NEW UD
OFF	[<step number>][;<ident list>	Terminate UD at step number
ON	<ident list>[;<device>]	Make UD active
OUTPUT	[<fspec>][;<ident list>]	Outputs errors on device
PAUSE	[<step number>[];<ident list>]	Pause UD execution
PLOG	[<fspec>][;<ident list>]	Print logged output
PTAB	[<fspec>][;<ident list>]	Print error tabulation
PURGE	<UD name>[;PST]	Remove ident from table
RESTORE	[<ident list>]	Restore UD control flags
RUN	[<ident times list>][;<device>]	Run UD specified times
SAVE	[<UD name>]	Save entry in PST
SET	<flag list>[;<ident list>]	Set UD control flags
SKIP	[<UD name>]	Skip rest of section
STATUS	[<ident list>]	Output UD status
TABULATE	<limit>[;<ident list>]	Tabulate errors
TIME	[<fspec>]	Output time of day

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SDM SYSTEM COMMANDS, sheet 2 of 2

WHEN ALLOWED:

Command	INACTIVE	READY	RUNNING	PAUSED	WAITING	CONFIGURING
ABORT		X	X	X	X	X
BRANCH				X		
CLEAR		X	X	X	X	
CONTINUE				X		
FLAGS		X	X	X	X	
GO	X	X		X	W	
LOG		X	X	X	X	
NAME		X	X	X	X	
OFF		X	X	X	X	X
ON	X	X	X	X	X	
OUTPUT		X	X	X	X	
PAUSE		X	X		X	
PLOG		X	X	X	X	
PTAB		X	X	X	X	
RESTORE		X	X	X	X	
RUN	X	X		X	W	
SAVE	X	X	X	X	X	
SET		X	X	X	X	
SKIP			X	X	X	
TABULATE		X	X	X	X	

where:

X = Command is allowed
W = Command allowed only when waiting for NEW section

471004-31, 2 of 2

DEFINITIONS IN SDM COMMANDS, sheet 1 of 2

The ::= symbol means "is defined as."

<UD name> ::= A symbol representing a single UD.

<fspec>::= This parameter specifies the source of destination file name or device name. A device is specified by a fspec of DEV= <device>. If a file is specified it must be a sequential file and be previously opened.

<ident list>::= A list of one or more symbols, which in general use UD names, separated by commas. If the ident list parameter is optional and the ident list parameter is omitted, then the command will be directed to all the UD´s currently on the Acitve list.

<flag list>::= A list of one or more numbers from 1 through 32 and the symbols, PA, PE, SP, EP, NP, LP, CS. The numbers refer to Flag Table elements. The first N Flag Table elements (where N is the number of Sections) are used as section selection flags. The remaining flags may be used for any purpose.

<step number>::= A decimal number between one and 511.

<device>::= A list of zero to two numbers, separated by commas, in the range from zero to 255. These numbers are passed tc the diagnostic program and may be logical device numbers, DRT numbers or unit numbers as specified by the diagnostic program. The device numbers may range freeom zero to 255. If a device number is not specified, the previously defined value will be used.

MNEMONIC FLAGS

PA - PAUSE AFTER STEP

Causes the UD to pause after each step and the step number to be output. This flag, if effect, causes the UD to single step. Execution is resumed with a CONTINUE or BRANCH command.

PE - PAUSE ON ERROR

Causes the UD to pause whenever an error message is output. Execution is resumed with a CONTINUE or BRANCH command.

SP - SHORT PRINT

Print only the message number and any variable data.

471004-32, 1 of 2

DEFINITIONS IN SDM COMMANDS, sheet 2 of 2

NP - NO PRINT

This flag causes the UD to suppress all error and data messages and certain pause and question messages, thus providing high speed test execution for such purposes as "scoping loops."

EP - ERROR PRINT ONLY

This flag causes SDM to suppress D class messages.

NA - NAME OUTPUT

This flag causes the UD name to be appended to the first line of any message output by the UD.

CS - CYCLE SECTION

This flag causes the UD to re-execute a section instead of advancing to the next selected section.

LP - LOOP

This flag causes the UD to loop on the current step or to loop back to the logical beginning of a sequence of steps and repeatedly execute the sequence.

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UD STATES

INACTIVE - The UD is known only to SDM through a UD entry in the PST or TST.

ACTIVE - The UD has been loaded and configuration data passed to it. It may be in any of the possible ACTIVE substates listed below.

READY - The UD is set up to execute but will not enter the RUNNING state until referenced by a RUN (see Section 3.24) or a GO (see Section 3.25) command. The UD enters the READY state when referenced by an ON (see Section 3.23) command.

RUNNING - The UD has been activated and is executing as far as SDM is concerned. The UD enters this state from the READY or INACTIVE state when referenced by a RUN or GO command.

PAUSED - Execution of the UD has been suspended by a PAUSE (see Section 3.27) command or by a pause request from the diagnostic.

WAITING - UD execution has been suspended while waiting for operator input, an interrupt, a timing delay or a new section to be selected.

TERMINATED - Transitory state between Running and Inactive.

STATUS COMMAND

The status of the UD is listed after the UD Name and current step number using the following mnemonics:

CF - Configuring
RE - Ready
RU - Running
IP - Waiting for Input
TM - Waiting for Timeout
IN - Waiting for Interrupt
NS - Waiting for New Section
PA - Paused
ON - Return to READY after execution
LO - Log Output
TE - Tabulate Errors
PR - Program runs in Privileged Mode

The Step Number output is the number of the last step executed or if the UD has not run then a Step Number of zero will be output. If the ident list specifies a UD which is in the INACTIVE state, the UD name will be output followed by the word "INACTIVE".

471004-33

The following diagnostics and diagnostic fix levels are current date code 1610.

ON-LINE DIAGNOSTICS

	DEVICE NAME	FILE NAME	LEVEL
1	DISC FILE - 2888A	PD360A	00.0
2	CART DISC - 7900A	PD361A	00.0
3	MAG TAPE	PD362A	03.0
4	TERMINAL DATA	PD363A	02.0
5	CARD READER	PD365A	05.0
6	LINE PRINTER - 2607/10/14	PD366B	03.0
6	LINE PRINTER - 2607/13/17/18	PD366A	01.0
7	TELEPRINTER	PD367A	02.0
10	TERM-CONTR	PD368A	01.0
11	TERMINAL - 2640A	PD369A	00.0
12	CARD PUNCH	PD370A	00.0
13	CRT - 2600A	PD371A	00.0
14	PAPER TAPE READER	PD372A	01.0
15	PAPER TAPE PUNCH	PD373A	01.0
16	TERMINET - 2762A	PD375A	01.0
17	CALCOMP PLOTTER	PD376A	00.0
20	CRT - 2615A (BEE-HIVE)	PD378A	01.0
21	CARD READER/PUNCH	PD379A	01.0

SLEUTH

Differences from Series II

* Does not have PUT and GET subroutines.

* Operates in 48K to 64K systems.

* The console interrupt switch, located on the 3000 mini-control panel, terminates any SLEUTH program and returns SLEUTH to the input mode.

* Control A is not recognized.

* Does not have 7920 device type (soon to be implemented as 12).

B Switch Reg. Control

0 - Enable Ext. Switch Reg.
7 - Enable Status Checking
11 - No Print
12 - Enable SIO Program Dump on Error
14 - Pause On Error (Halt %16)
15 - Switch Output to Alternate Device

HALT CODES	SEG. NO.	DESCRIPTION
XX	06	Cold Load Halt.
01	22	Stand Alone Loader (First Halt) Request Program Number
02	22	Stand Alone Loader (Second Halt) Request Program Origin
03	22	Stand-Alone Loader (Occurs if answer to Halt 02 < %4000)
15	XX	Interrupt from Segment No. other than 0,1,2 or 5.
16	20	Halt on Error.
17	20	Orderly termination by user execution of Halt command.

Table A-1. Index of Commands and Mnemonics

INDEX OF COMMANDS AND MNEMONICS

MNEMONIC	VARIABLE	COMMAND NAME
ACB ✱	BUF(INDEX) PRIMARY VARIABLE BUF(INDEX)	ACCESS BUFFER
AR	LUN [,CYL,HD,SEC]	ADDRESS RECORD
AUTO	[STEPN]	AUTO NUMBER STEPS
BA	[RECORD/E]	BATCH IN TESTS
BSF	LUN	BACKSPACE FILE
BSR	LUN	BACKSPACE RECORD
BUMP	[P]	BUMP PASS COUNT
CA	LUN	COMPARE ADDRESS
CB	LUN,BUF1,BUF2,ERRCOUNT	COMPARE BUFFERS
CC	LUN,SECOUNT[,CYL,HEAD,SEC]	CYCLIC CHECK
CCI	LUN,SECOUNT	CC IMMEDIATE
CHB	BUF,TYPE	CHANGE BUFFER
CIO	LUN,CONTROLWORD	CONTROL I O
CL	LUN	CLEAR
CLR	LUN,BUFFER[,CYL,HEAD,SEC]	COLD LOAD READ
CLUB	LUN	CLEAR UNIT BUSY
CONF		CONFIGURE
CONT	WORD1,WORD2	CONTROL ORDER, SIO
CORB ✱	LUN,BUF	CORRECT BUFFER
DB	NAME,LENGTH,DATA TYPE	DEFINE BUFFER
DELY	RESOLUTION	DELAY
DEV	LUN,DRT,TYP,ERR,UNIT[,BAUD]	DEVICE
DISP	LUN,TYPE	DISPLAY
DS	LUN[,CYL,HEAD,SEC]	DECREMENTAL SEEK
DUMP	PARAM[,PARAM]	DUMP QUANTITY
END		END COMMAND
ENDS	[,I]	END ORDER SIO
EP	[S]	ERASE PROGRAM
ES		ENABLE STATUS
ESTA ✱	STATUS,MASK	EXPECTED STATUS
FMT	LUN[,L,U]	FORMAT
FOR	VAR PRI TO PRI	FOR
FSF	LUN	FORWARD SPACE FILE
FSR	LUN	FORWARD SPACE RECORD
FTD	LUN, CYL,HEAD,SEC	FLAG TRACK DEFECTIVE
FTDI	LUN	FTD IMMEDIATE
GAP	LUN	GAP MAG TAPE
GET ✱	VAR LUN	GET
GO	STEPN,EXPSTATUS,MASK	CONDITIONAL BRANCH
HALT		HALT %17
ID	LUN,BUFF CYL,HEAD,SEC	INITIALIZE DATA
IDI	LUN,BUFF	ID IMMEDIATE
IF	PRI RELOP PRI THEN STEP	IF
INT		INTERRUPT ORDER, SIO
IR	LUN,BUFF,TRACK,ARC	INCREMENTAL READ
IS	LUN[,CYL,HEAD,SEC]	INCREMENTAL SEEK
IT	LUN[,CYL,HEAD,SEC]	INCREMENTAL TRACK
IW	LUN,BUFF,TRACK,ARC	INCREMENTAL WRITE
JUMP	ADDRESS[,C]	JUMP ORDER SIO
LET	VAR EXPR	LET
LIST ✱	VAR[,BASE]	LIST
LOOP	STEPN TIMES	BRANCH
LTIO	LUN,WORD	LOAD TIO REGISTER
MAKT	A N	MAKE TEST TAPE
MC	LUN	MASTER CLEAR
NAME	SIOPROG	NAME SIO PROGRAM
NEXT	VAR	NEXT
NOPR		NO PRINT
PCT	LUN,PATTERN	PACK CERTIFICATION
PE		PAUSE ON ERROR
POLL	LUN	RESUME POLLING
PR		PRINT
PROC [,N]		PROCEED
PUT ✱	"STRING"	PUT
RA	LUN[,CYL,HEAD,SEC]	READ ADDRESS
RAI	LUN	RA IMMEDIATE
RAND	VAR	RANDOMIZE
RC	LUN	RECALIBRATE
RCLK ✱	VAR	READ CLOCK
RD	LUN,BUF[,MODE,ETC]	READ DATA
RDA	LUN	REQUEST DISC ADDRESS
RDC	LUN,BUFFER	READ RECORD W CRCC
RDI	LUN,BUFFER	RD IMMEDIATE
READ	BUF[,C]	READ ORDER, SIO
REN		RENUMBER PROGRAM
REW	LUN	REWIND MAG TAPE
RFS	LUN,BUF[,BUF,CYL,HEAD,SEC]	READ FULL SECTOR
RFSI	LUN,BUF	RFS IMMEDIATE
RIO	LUN,BUF	READ I O
RMSK	BUF	READ MASK
RNFI	LUN,BUF	RNFS IMMEDIATE
RNFS	LUN,BUF, CYL,HEAD,SEC	READ NEXT FULL SECTOR
RP	LUN,LINELENGTH	RIPPLE PRINT
RQST	LUN	REQUEST STATUS
RRES		RTN RESIDUE ORDER SIO
RS	LUN	RANDOM SEEK
RSA	LUN	REQUEST SECTOR ADDRESS
RST	LUN	REWIND & RESET
RSYN	LUN	REQUEST SYNDROME
RUA	LUN	REQUEST UNIT ALLOCATION
RUN		RUN COMMANDS
RWO	LUN,BUF,MASK,OFFSET CYL,HD,SEC	READ WITH OFFSET
RWOI	LUN,BUF,MASK,OFFSET	READ WITH OFFSET IMMEDIATE
RWV	LUN,BUF[,MASK, CYL,HD,SEC]	READ WITHOUT VERIFY
RWVI	LUN,BUF[,MASK]	READ WITHOUT VERIFY IMMEDIATE
SA	LUN,BUF[,CYL,HEAD,SEC]	SKIP ADDRESS READ
SAI	LUN,BUF	SA IMMEDIATE
SBNK	BANK	SET BANK
SCLK ✱	VALUE	SET CLOCK
SED	0 1	SET ENABLE DISABLE INT
SEEK	LUN CYL,HEAD,SEC	SEEK
SELU	LUN,UNIT	SELECT UNIT MAG TAPE
SENS		SENSE ORDER, SIO
SETJ	LUN,JUMPERS	SET JUMPERS UNIV IFACE
SFM	LUN,MASK	SET FILE MASK
SIN	LUN	SET INTERRUPT
SIO	LUN,PROG,INTS,TIME EST,MASK	START I O
SKRD	LUN,BUF[[,MASK],CYL,HD,SEC	SEEK READ DATA
SKWD	LUN,BUF[,MASK] CYL,HD,SEC	SEEK WRITE DATA
SMSK	MASKWORD	SET MASK
SOUT		SWITCH OUTPUT
SS		SUPPRESS STATUS
STAT	S T D	STATUS DUMP
TAB		TABULATE
TDIL	LUN1,LUN2,BUF1,BUF2	TERM DATA IFACE LOOP
TIO	LUN	TEST I O
VER	LUN,SECCOUNT[,CYL,HD,SEC]	VERIFY
VERI	LUN,SECCOUNT	VERIFY IMMEDIATE
WA	LUN ,CYL,HEAD,SEC	WRITE ADDRESS
WAI	LUN	WA IMMEDIATE
WD	LUN,BUF[,MODE,ETC]	WRITE DATA
WDI	LUN,BUF	WD IMMEDIATE
WFM	LUN	WRITE FILE MARK
WFS	LUN,BUF,CYL,HEAD,SECTOR	WRITE FULL SECTOR
WFSI	LUN,BUF	WFS IMMEDIATE
WIO	LUN,WORD	WRITE I O
WRIT	BUF[,C]	WRITE ORDER, SIO
WRZ	LUN,BUF	WRITE REC W 0 PARITY
XDUI	LUN,BUF1,BUF2,MODE	XFR DATA UNIV IFACE
ZBUF	BUF	ZERO BUFFER

✱ Series II commands only

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LIST OF COMMANDS BY DEVICE TYPES

SLEUTH CONFigure COMMAND

Configuration Codes

1	SIO MUX
2	Card Reader (2893A)
3	Syncrhonous Single-Line Controller
4	Hardwired Serial Interface
5	Line Printers (2607A, 2613A, 2617A, 2618A)
6	Terminal Data Interface
7	Terminal Control Interface
8	Clock-Console
9	Unused
10	Unused
11	Unused
12	7920A
13	Disc Drive (7900A)
14	Disc Drive (2888A)
15	Disc Drive (7905A, 7920A)
16	2MB Disc Drive (2660A)
17	4MB Disc Drive (2660A)
18	Magnetic Tape Unit (7970B)
19	Magnetic Tape Unit (7970E)
20	Paper Tape Reader (2748B)
21	Paper Tape Punch (2895A)
22	Plotter Interface
23	Line Printers (2610A, 2614A)
24	Special Interface
25	30050A, 30051A

The CONFigure command should be run every time a configuration change has taken place. If the CONFigure command does not run successfully, it is an indication that MPE may not function.

The following pages contain lists of possible HALTS and their meanings.

Coded Halts

CONFIGURATOR HALT	MEANING
0	I/O command rejected. (CC = CCL)
1	Unexpected interrupt. (RA = Device Number)
2	I/O command rejected. (CC = CCG)
3	Interrupt from unidentifiable device. (RA = Device Number)
4	Device interrupted more than once per test. (RA = Device Number)
6	SIO MUX has two non-zero RAM´s.
%10	Interrupted by declared non-interrupt device.
%11	Unexpected module violation. (RA = Parameter)
%12	SIO program did not complete. (RA = Device Status) (RB = Device Number)
%13	DRT contains wrong SIO program pointer. (RA = SIO Pointer) (RB = Expected Pointer) (RC = Device Number)
%14	SIO MUX address RAM was wrong value.

INSTRUCTIONS FOR RUNNING THE WORKOUT PROGRAM

The WORKOUT program allows the user to exercise up to six disc drives and one mag tape on-line while under control of MPE. This program requires no special capabilities or knowledge.

After the :RUN WORKOUT command is entered, the following questions will be asked. A carriage return will imply the default answer.

a. Number of disc files?

   Any number from 0 to 6 can be input. This will be the number of disc files that WORKOUT will attempt to open.

b. Number of Passes?

   Any number from 0 to 32766 can be input. WORKOUT will execute the number of passes entered and terminate. If zero passes is input, the program will terminate immediately.

   Default: Zero.

c. LDN for file #N?

   This question will be asked if the answer to "a" was greater than zero. Any number from 0 to 255 can be input.

   Default: Zero.

d. Do you want SORT?

   This question will be asked if the answer to "a" was greater than one. A "Y" will cause file #1 to be sorted and written to file #N where N is the last file specified.

   Default: No Sort.

e. Do You Want Tape Transfer?

   A "Y" will attempt to open a tape file. If the answer to "a" was zero and this answer is "N" then the program will terminate.

   Default: No.

At this point WORKOUT will attempt to open all the files. If for any reason all the files cannot be opened, a tombstone will be printed for that file and the program will terminate.

During the first pass, seven more extents for each file will be opened as it is written. If a file runs out of disc space, a tombstone will be printed for that file and the program will terminate. After the first pass, the extents remain allocated and the program should not run out of disc space anymore.

DIAGNOSTICS

If sort was selected and it cannot open its scratch file because of disc space, a tombstone will be printed for that file and the program will terminate.

At the end of each pass, a message is printed showing the time of day and the number of the pass.

MPE CONFIGURATION

MPE CONFIGURATION

SECTION V

MPE DIFFERENCES, sheet 1 of 2

PRE-SERIES II Software	SERIES II Software
MPE-C	MPE-II,larger enhanced version of MPE-C with additional Terminal handling capability & provisions for future enhancements. Externally to the user very similiar to MPE-C but internally different.
File Access & Organization Methods	File Access & Organization Methods
- Sequential	- Sequential
- Direct (random)	- Direct (random)
-IMAGE/QUERY o up to 16 Data Extents o Data set cannot cross volume boundry	- IMAGE/QUERY o up to 32 Data Extents o Data set can cross volume boundry on Extent boundary
- Index-indexed File Organization Method o 1 key o Single user of file when adding and deleting records o multiple user inquiry	- KSAM-Keyed Sequential Access Method o 16 keys o concurrent add, delete, update and inquiry
Languages	Languages
- COBOL (see note below on COBOL)	- COBOL (see note below on Cobol)
- RPG	- RPG
- FORTRAN	- FORTRAN
- BASIC(Compiler and Interpreter)	- BASIC (compiler & Interpreter)
- SPL	- SPL
NO APL	- APL

MPE DIFFERENCES, sheet 2 of 2

PRE-SERIES II	SERIES II
Terminal Type recognition user specifiable	Terminal type recognition Automatic
Powerfail/Manual Restart	Powerfail/Auto Restart
Up to 96 open files per program	Up to 255 open files program
Up to 16 file extents	Up to 32 file extents
Files cannot cross volume boundaries	Files can cross volume boundaries on Extent Boundaries
	SOFTWARE CHANNELS I/O ERROR LOGGING
SYSTEM DISC MUST BE LOGICAL DEVICE 1, DEVNO 5 CLOCK-CONSOLE MUST BE LOGICAL DEVICE 3, DEVNO 3	

DRIVER NAMES, TYPES, SUBTYPES, AND SIZES, sheet 1 of 4

DEVICE	PART NO.	DRIVER NAME	TYPE	SUB-TYPE	RECORD WIDTH (Decimal Words)
System Clock/Console	30031A	IOCLTTY0	16		36
ASR 33/35	30124A			0	
Terminet 10cps	30114A			1	
" 15cps				2	
" 30cps				3	
HP2600A 10cps	30132A			4	
" 15cps				5	
" 30cps				6	
" 60cps				7	
" 120cp				8	
" 240cp				9	
HP2640A/B	30123A			10	40
Asynchronous Terminal Controller:	30032A or 30032B	IOTERM0	16		36/40
Hardwired Terminal speed sensing				0*a	
Full duplex modem (103 or V.21), speed sensing				1	
Asynchronous half-duplex modem (202 or V.23), Data Rate Select ON, speed sensing				2	
Asynchronous half-duplex modem (202 or V.23), Data Rate Select OFF, speed sensing				3	
Hardwired Terminal speed specified				4	

*a These terminals should be configured with Sub-Type = 1 when hardwired: ASR 37, IBM Selectric, Memorex 1240.

471004-36/37, 1 of 4

DRIVER NAMES, TYPES, SUBTYPES, AND SIZES, sheet 2 of 4

DEVICE	PART NO.	DRIVER NAME	TYPE	SUB-TYPE	RECORD WIDTH (Decimal Words)
Full duplex modem (103 or V.21), speed specified				5	
Asynchronous half-duplex modem (202 or V.23), Data Rate Select ON, speed specified				6	
Asynchronous half-duplex modem (202 or V.23), Data Rate Select OFF, speed specified				7	
Nine-channel Magnetic Tape Unit (7970B/E)	30115A	IOTAPE0	24	0	128
Fixed-Head Disc (2660A):	30103A	IOFDISC0*b	1		128
2 megabyte	-001			1	
4 megabyte	-002			2	
Cartridge Disc (7900A):	30110A	IOMDISC0*b	0	2	128
Lower Platter only				1	
Upper Platter only				0	
Disc Drive (7905A/7920A):	30129A	IOMDISC1*b	0		128
7905A (Removable Platter)				4	
7905A (Fixed Platter)				5	
7905A (Cylinder Mode)				6	
7905A (System Disc Mode)				7*c	
7920A				8	

*b Core resident.
*c Fixed Head Disc replacement; uses first 200 cylinders only.

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DRIVER NAMES, TYPES, SUBTYPES, AND SIZES, sheet 3 of 4

DEVICE	PART NO.	DRIVER NAME	TYPE	SUB-TYPE	RECORD WIDTH (Decimal Words)
Disc File (2888A)	30102A	IOMDISC0*b	0	3	128
Card Reader (2893A)	30106A	IOCDRD0	8	0	40
Paper Tape Reader (2748B)	30104A	IOPTRD0	9	0	40
Paper Tape Punch (2895A)	30105A	IOPTPN0	34	0	128
Line Printer (2607/08/10/13/14/17/18):	30108A 30109A	IOLPRT0	32		66
2610/14				0	
2607/08				1	
2613/17/18				2	
Plotter:	30226A	IOPLOT0	35		128
0.010 in.				0	
0.005 in.				1	
0.0025 in.				2	
0.00125 in.				3	
0.002 in.				4	
0.1 mm				5	
0.05 mm				6	
0.025 mm				7	
Printing Reader/Punch (2894A)	30119A	IOPRPN0	20	0	40
Programmable Controller (UI)	30361A	IOREM0	23	0	128
Synchronous Single-Line Controller:	30055A	IOSBSC0	22		128
ASCII Switched Modem (dial up)				0	
ASCII Non-switched Modem (private or leased)				1	

471004-36/37, 3 of 4

DRIVER NAMES, TYPES, SUBTYPES, AND SIZES, sheet 4 of 4

DEVICE	PART NO.	DRIVER NAME	TYPE	SUB-TYPE	RECORD WIDTH (Decimal Words)
EBCDIC Switched Modem (dial up)				2	
EBCDIC Non-switched Modem private or leased)				3	
Hardwired Serial Interface	30360A	CSHBSC0	19	3	N/A
DS/3000 Communications Line		IODS0	41	0	128
DS/3000 Pseudo Terminal		IODSTRM0	16	0	36

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Memory Size Configurator Question	48	64	Unit of Measure	Maximum Allowed
*MAX = OF OPEN SPOOFLES = xxx.?	20	20	– –	256-N
CST = xxx.?	256	256	entries	256
DST = xxx.?	192	256	entries	1024
PCB = xxx.?	56	80	entries	256
I/O QUEUE = xxx.?	**48	**64	entries	255
TERMINAL BUFFERS = xxx.?	24	48	buffers	255
IOCB = xxx.?	32	48	entries	255
ICS = xxxx.?	384	512	words	1024
UCOP REQUEST QUEUE = xxx.?	16	32	entries	256
TIMER REQUEST LIST = xxx.?	16	20	– –	128
*BREAKPOINT TABLE = xxx.?	20	30	entries	255
≠ OF RINS MIN = 5, MAX = 64.?	32	64	– –	1024
= OF GLOBAL RINS USED = 0, MAX = 32.?	16	32	– –	1024
≠ OF SECONDS TO LOGON = xxx.?	120	120	– –	600
*MAX ≠ OF CONCURRENT RUNNING SESSIONS = xxx.?	10	16	– –	255
*MAX ≠ OF CONCURRENT RUNNING JOBS = xxx.?	1	1	– –	255
DEFAULT JOB CPU TIME LIMIT = xxxxx.?	0	0	– –	32767
LOG FILE RECORD SIZE (SECTORS0 = x.?	2	2	– –	8
LOG FILE SIZE (RECORDS0 = xxxxx.?	1024	1024	– –	32767
VIRTUAL MEMORY = xxxx.?	2048	3072	sectors	8192
DIRECTORY USED = xxx, MIN = 242, MAX = 512.?	384	512	sectors	512
*MAX ≠ OF SPOOFLE KILOSECTORS = xxxxx.?	128	128	– –	%777777D
TIME QUANTUM –CS SUBQUEUE = xxxxx.?	1000	1000	milliseconds	32767
TIME QUANTUM – DS SUBQUEUE = xxxxx.?	1000	1000	milliseconds	32767
MAX CODE SEG SIZE = xxxxx.?	4096	4096	words	16384
MAX = OF CODE SEGMENTS/PROCESS = xxx.?	40	40	– –	255
MAX STACK SIZE = xxxxx.?	24567	31232	words	31232
MAX EXTRA DATA SEG SIZE = xxxxx.?	3072	4096	words	32767
MAX ≠ OF EXTRA DATA SEGMENTS/PROCESS = x.?	3	4	– –	4
STD STACK SIZE = xxxx.?	800	800	words	4096

*New for Release C.

**This value is based on installations supporting one spooled line printer and one spooled card reader. Should this not be the case, add or subtract 15 for each spooled output device and 10 for each spooled input device. N = Number of configured devices.

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DEFAULT PARAMETER SETTINGS FOR CONFIGURATION

```
=ABORTIO {ldn}

=ALTFILE {devicefileid}

[;OUTPRI = outputpriority]
[;COPIES = numcopies]

[          {ldn     }]
[;OUTDEV = {devclass}]

=DELETE {devicefileid}

=DOWN {ldn}

=GIVE {ldn}

=SHOWDEV [ldn     ]
         [devclass]

         [#Innn                             ]
=SHOWIN  [STATUS                            ]
         [qualification [;qualification]    ]

         [#Onnn                             ]
=SHOWOUT [STATUS                            ]
         [qualification [;qualification]    ]

  where
     #Innn
     a request for a particular input devicefile
     #Onnn
     a request for a particular output devicefile
     STATUS
     a request for summarizing information regarding
     devicefile status

     qualification (list)
     is a request for all input (or output) devicefiles that
     satisfy the qualifications, which are:

     [      {ldn       }]
     [DEV = {devclass *}]             ACTIVE
                                      READY        are specific devicefile states
     [      {@J   }]                  OPENED
     [JOB = {@S   }]
     [      {jsnum}]                  N
                                      (output only) requests only non-deferred files
     [ACTIVE   [,N]  * ]
     [READY    [,D]  * ]              D
     [OPENED           ]              (output only) requests only deferred files

     (* = =SHOWOUT only)

                                                          [,STARTOUT                            ]
=SPOOL {ldn} [,STARTIN             ]                      [,RESUME                              ]
             [[,STOP] [,DELETE]    ]    =SPOOL {ldn}      [[,STOP]        [,DELETE]] [,OPENQ]
                                                          [[,WAIT]        [,DEFER ]] [,SHUTQ]
=TAKE {ldn}

=UP {ldn}
```

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CONSOLE OPERATOR COMMANDS – DEVICE AND FILE MANAGEMENT

```
≡ABORTJOB {jsnum}

≡ACCEPT [JOBS]  {ldn}        If the first parameter is omitted, both
        [DATA]               :JOB (or :HELLO) and :DATA
                             commands are allowed.
≡ALTJOB  jsnum
         [;INPRI = inputpriority] The job must be introduced or waiting

       [ ;OUTDEV = { ldn      } ]
       [           { devclass } ]

≡BREAKJOB {jnum}

≡JOBFENCE { priorityfence}

≡LIMIT[numberjobs] [,numbersessions]

≡LOGOFF

≡LOGON

≡OUTFENCE {priorityfence}

≡REFUSE [JOBS, ]  {ldn}
        [DATA, ]

≡REPLY PIN,reply

≡RESUMEJOB {jnum }

≡SESSION

           [jsnum]
           [STATUS]
≡SHOWJOB   [qualifier 1 [;qualifier 2]       @J
           [qualifier 2 ;qualifier 1]        @S
                                      JOB=[userjsname,] username.acctname
                                             @,username.acctname
                                             [@,] @ .acctname

≡SHOWQ [subqueuename]

≡SHUTDOWN
                                      [ INTRO     [,N] ]
≡STREAMS  ldn                         [ WAIT      [,D] ]
          OFF                         [ EXEC           ]

       { @      }
≡TELL  { jsnum  } ;message
       { jsname }

       { @      }
≡WARN  { jsnum  } ;message
       { jsname }

≡WELCOME cr
#message cr
#message cr
#cr
```

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Commands	Parameters	Function	When Issued
:ALTACCT	acctname [;PASS=[password]] [;FILES=[filespace]] [;CPU=[cpu]] [;CONNECT=[connect]] [;CAP=[capabilitylist]] [;ACCESS=fileaccess]] [;MAXPRI=[subqueuename]] [;LOCATTR=[localattribute]]	Changes an account's characteristics.	Job, session, break, or programmatically.
:LISTACCT	[@ accountname] [,listfile]	Lists attributes of an account.	Job, session, break, or programmatically.
:LISTGROUP	[groupset] [,listfile]	Lists attributes of a group.	Job, session, break, or programmatically.
:LISTUSER	[userset] [,listfile]	Lists attributes of a user.	Job, session, break, or programmatically.
:NEWACCT	acctname,mgrname [;PASS=[password]] [; FILES=[filespace]] [;CPU=[cpu]] [;CONNECT=[connect]] [;CAP=[capabilitylist]] [;ACCESS=[fileaccess]] [;MAXPRI=[subqueuenamel]] [;LOCATTR=[localattribute]]	Creates a new account.	Job, session, break, or programmatically.
:PURGEACCT	acctname	Deletes an account.	Job, session, break, or programmatically.
:REPORT	[groupset] [,listfile]	Displays an account's resource usage.	Job, session, break, or programmatically.
:RESETACCT	[@ acctname] [,CPU ,CONNECT]	Resets resource-use counters for an account and its groups	Job, session, break, or programmatically.

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SYSTEM MANAGER CAPABILITY COMMANDS

CAPABILITY LIST

User Attributes:

SM = System Manager

AM = Account Manager

AL = Account Librarian

GL = Group Librarian

DI = Diagnostician

OP = System Supervisor

File Access Attributes:

SF = Permanent Files

ND = Access of non-sharable I/O devices

Capability Class Attributes:

PH = Process-Handling

DS = Extra Data Segments

MR = Multiple RINS

PM = Priviledge Mode

IA = Interactive Access

BA = Local Batch Access

(Pages MPECNFG-12 through -18 are reserved for future information.)

(Do NOT print. See preceding page.)

(Do NOT print. See preceding page.)

(Do NOT print. See preceding page.)

(Do NOT print. See preceding page.)

(Do NOT print. See preceding page.)

(Do NOT print. See preceding page.)

Commands	Parameters	Function	When Issued
:ALLOCATE	*[code],name*	Permanently allocates a program or procedure in virtual memory.	Job or session.
:DEALLOCATE	*[code],name*	Removes a program or procedure from virtual memory.	Job, session, break, or pro-
:QUANTUM	*subqueuename,time*	Changes a circular subqueue time-quantum.	Job, session, break, or programmatically.
:RESUMELOG		Resumes logging following suspension caused by an error.	Job, session, break, or programmatically.
:SHOWLOG		Displays Log-File status.	Job, session, break, or programmatically.
:SHOWQ	*[subqueuename]*	Displays scheduling subqueue information.	Job, session, break, or programmatically.
:SWITCHLOG		Closes current Log File, opens a new Log File, and treats this as current Log File.	Job, session, break, or programmatically.
:SYSDUMP	*dumpfile[,auxlistfile]*	Copies MPE/3000 to tape.	Job or session.

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SYSTEM SUPERVISOR CAPABILITY COMMANDS

Commands	**Parameters**	**Function**	**When Issued**
:ALTGROUP	*groupname* *[;PASS=[password]]* *[;CAP=[capabilitylist]]* *[;FILES=[filespace]]* *[;CPU=[cpu]]* *[;CONNECT=[connect]]* *[;ACCESS=[fileaccess]]*	Changes a group's attributes.	Job, session, break, or programmatically.
:ALTUSER	*username* *[;PASS=[password]]* *[;CAP=[capabilitylist]]* *[;MAXPRI=[subqueuename]]* *[;LOCATTR=[localattribute]]* *[;HOME=[homegroupname]]*	Changes a user's attributes.	Job, session, break, or programmatically.
:LISTACCT	*[acctname] [,listfile]*	List attributes of user's log-on account.	Job, session, break, or programmatically.
:LISTGROUP	*[groupset] [,listfile]*	List attributes of a group in user's log-on account.	Job, session, break, or pro-
:LISTUSER	*[userset] [,listfile]*	Lists attributes of a user in log-on account.	Job, session, break, or programmatically.
:NEWGROUP	*groupname* *[;PASS=[password]]* *[;CAP=[capabilitylist]]* *[;FILES=[filespace]]* *[;CPU=[cpu]]* *[;CONNECT=[connect]]* *[;ACCESS=[fileaccess]]*	Creates a new group in log-on account.	Job, session, break, or programmatically.
:NEWUSER	*USERNAME* *[;PASS=[password]]* *[;CAP=[capabilitylist]]* *[;MAXPRI=[subqueuename]]* *[;LOCATTR=[localattribute]]* *[;HOME=[homegroupname]]*	Creates a new user in log-on account.	Job, session break, or programmatically.
:PURGEGROUP	*groupname*	Deletes a group from log-on account.	Job, session, break, or programmatically.
:PURGEUSER	*username*	Deletes a user from log-on account.	Job, session, break, or programmatically.
:REPORT	*[groupset] [,listfile]*	Displays resource-usage counts for log-on account and its groups.	Job, session, break, or programmatically.

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ACCOUNT MANAGER CAPABILITY COMMANDS

FOR NEW FILES:

```
:FILE formaldesignator        { = $NEWPASS                  }
                              {[= filereference] [,NEW]     }

   [:DEV = device]

   [:DISC = [filesize] [.[numextents] [,initalloc] ] ]

                                           [ [F] [          ] ] ] ]
   [:REC = [recsize] [.[block factor] [ [U] [.BINARY  ] ] ] ]
                                           [ [V] [.ASCII    ] ] ] ]

   [:NOBUF]
   [:CCTL]
   [:MR]

   [ :EXC ]
   [ :EAR ]
   [ :SHR ]

   [:ACC = accesstype]
   [:BUF = numbuffers]

   [ :DEL  ]
   [ :SAVE ]
   [ :TEMP ]

   [:CODE = filecode]
```

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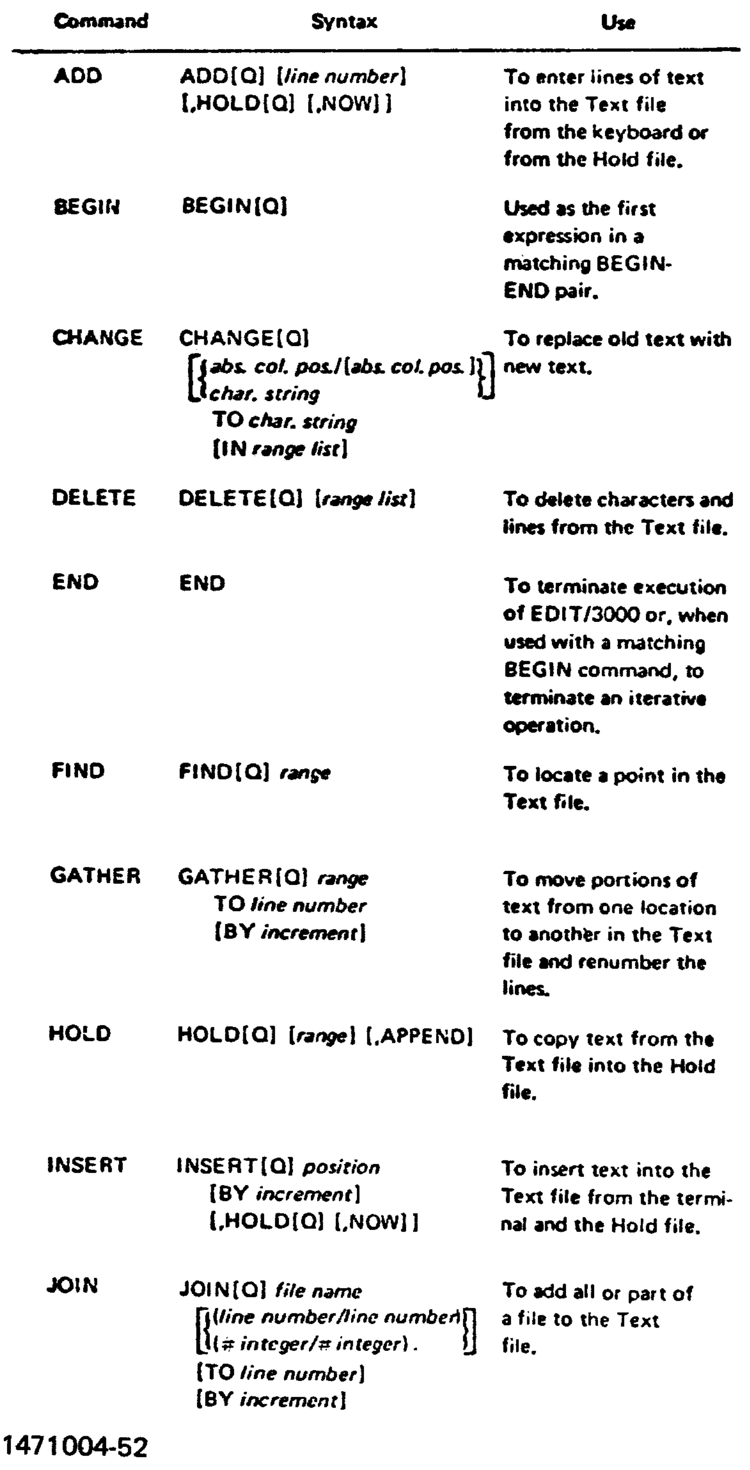
FILE COMMAND FORMAT



Command	Syntax	Use
ADD	ADD[Q] [*line number*] [,HOLD[Q] [,NOW]]	To enter lines of text into the Text file from the keyboard or from the Hold file.
BEGIN	BEGIN[Q]	Used as the first expression in a matching BEGIN-END pair.
CHANGE	CHANGE[Q] [{*abs. col. pos./*[*abs. col. pos.*]} {*char. string*}] TO *char. string* [IN *range list*]	To replace old text with new text.
DELETE	DELETE[Q] [*range list*]	To delete characters and lines from the Text file.
END	END	To terminate execution of EDIT/3000 or, when used with a matching BEGIN command, to terminate an iterative operation.
FIND	FIND[Q] *range*	To locate a point in the Text file.
GATHER	GATHER[Q] *range* TO *line number* [BY *increment*]	To move portions of text from one location to another in the Text file and renumber the lines.
HOLD	HOLD[Q] [*range*] [,APPEND]	To copy text from the Text file into the Hold file.
INSERT	INSERT[Q] *position* [BY *increment*] [,HOLD[Q] [,NOW]]	To insert text into the Text file from the terminal and the Hold file.
JOIN	JOIN[Q] *file name* [{(*line number/line number*)} {(# *integer*/# *integer*).}] [TO *line number*] [BY *increment*]	To add all or part of a file to the Text file.

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EDITOR COMMAND FORMAT, 1 of 3

Command	Syntax	Use
KEEP	KEEP[Q] *file name* [(*range*)] [,UNNUMBERED]	To save all or part of the Text file in a user file
LIST	LIST[Q] [*range*] [,UNNUMBERED] [,OFFLINE] [,TRANSLATE] [,NOTEXT]	To print out any portion or all of the Text file.
MODIFY	MODIFY[Q] *range list*	To modify text in the Text file using three operations: delete (D), insert (I), and replace (R).
NOT	NOT	Causes setting of FLAG to be reversed after the next following expression is interpreted.
OR	OR	Resets FLAG to true if it is false, or to false if FLAG is true.
PROCEDURE	PROCEDURE *pname,* $\begin{Bmatrix} G \\ P \\ S \end{Bmatrix}$ *, range list*	Calls logical procedure stored in a library outside the subsystem.
Q	Q *character string*	To print a message at the terminal while in Use mode.
REPLACE	REPLACE[Q] *range list* [,HOLD[Q][,NOW]]	To replace lines in the Text file.

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EDITOR COMMAND FORMAT, 2 of 3

Command	Syntax	Use
SET	SET[FROM=*line number*] [,DELTA=*increment*] [,LEFT=*column position*] [,RIGHT=*column position*] [,LENGTH=*line length*] [,{QUIET DISPLAY}] [,{SHORT LONG}] [,{BATCH POLL}] [,DEPTH=*unsigned integer*] [,TIME=*unsigned integer*] [,SIZE=*unsigned integer*] [,{FRONT REAR}] [,{FIXED VARIABLE}]	To alter options that are normally set by the subsystem and that govern editing operations.
TEXT	TEXT *file name* [{(*line number/line number*) (*# integer/# integer*)}] [,UNNUMBERED]	To copy contents of a user file into the Text file to be edited.
USE	USE *file name*	To instruct the subsystem to read commands from a user file but to send messages to and expect input from the terminal.
VERIFY	VERIFY[{ALL *option list*}]	To obtain a reminder of the values of options declared in the SET command.
WHILE	WHILE[FLAG]	Causes EDIT/3000 to iterate the next two edit expressions (or one, if FLAG is declared) until the first one fails.
XPLAIN	XPLAIN[{*com. name list* ALL}] [,OFFLINE]	To obtain an explanation of the commands.
YES	YES	Sets the FLAG to true
Z : :=	Z : := *object record*	To assign the value of the object record to Z : :=.

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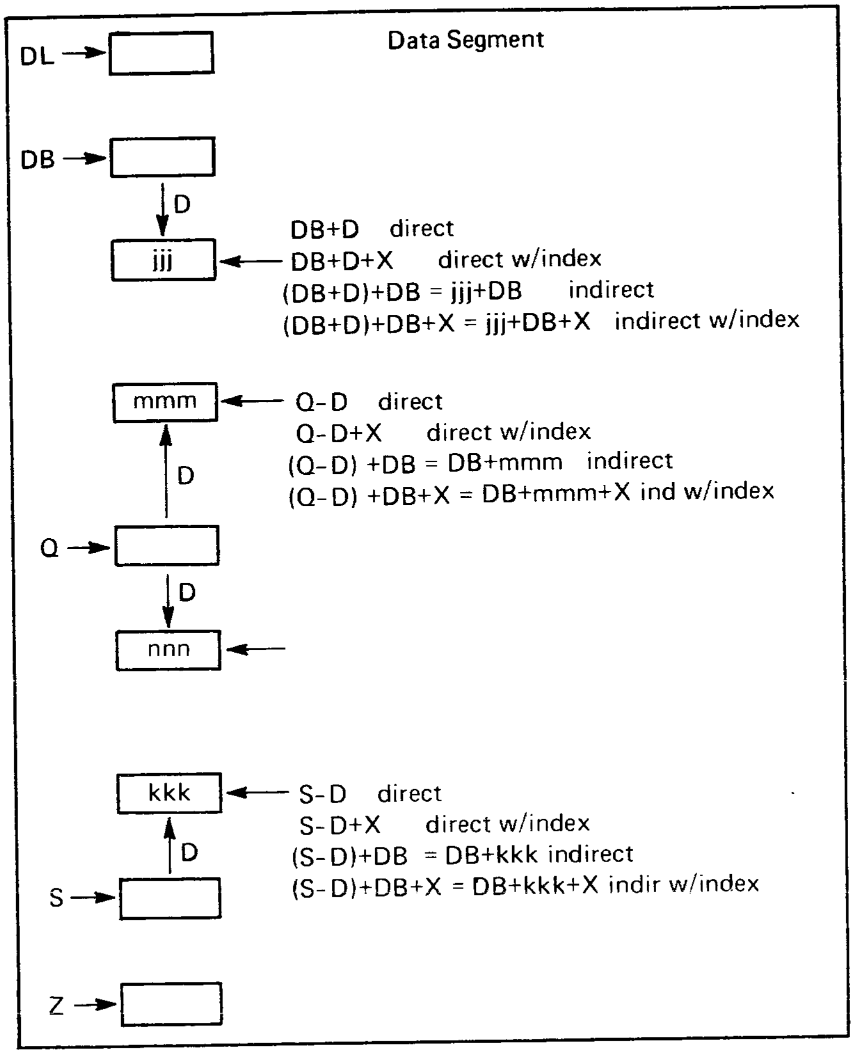
EDITOR COMMAND FORMAT, 3 of 3



Bounds checking DL <= E <= SM + SR
RA = E - DB
Indirect address in indirect cell is DB relative

Addressing arithmetic is done MOD 65K. For array Byte and Double addressing Index register contains entry index. For Byte array X(15) indicates position, 0 = left E(0:7); 1 = right E(8:15). Shift X right to get word address. If out of bounds microcode adds 32K. For Double array, shift left to get word address. For byte indirect, word in indirect cell is byte address.

1471004-55

ADDRESSING MODES

INTERRUPTS/TRAPS/SYSTEM HALTS, sheet 1 of 2

Interrupt	Parameter (on the ICS @ Q+2)	
0 External Interrupt	DEV #	
1 Power Fail	-	
2 Power On	-	
3 Stack Overflow	-	
4 Module Interrupt	MODL #)	> in SP1 Register
5 Console Interrupt	CPU ID)	
6 Cold Load	-	
7 -	-	
	Parameter (on the current stack at Q+1)	
10 -	-	
11 Module Error:		
Illegal Address	1000	
Bounds Violation	2000	
Non-responding Module	4000	
12 Parity Error:	Type	
System P.E.	40000	
Memory Address P.E.	20000	
Data P.E.		
13 Miscellaneous:		
Stack Underflow	1	
CST Bounds Violation	2	
STT Bounds Violation	3	
14 Code Segment Absence:		
PCAL	P-Label	
EXIT	N	
15 STT Entry Uncallable	P-Label	
16 TRACE (PCAL only)	P-Label	

471004-56, 1 of 2

INTERRUPTS/TRAPS/SYSTEM HALTS, sheet 2 of 2

17 User Traps:

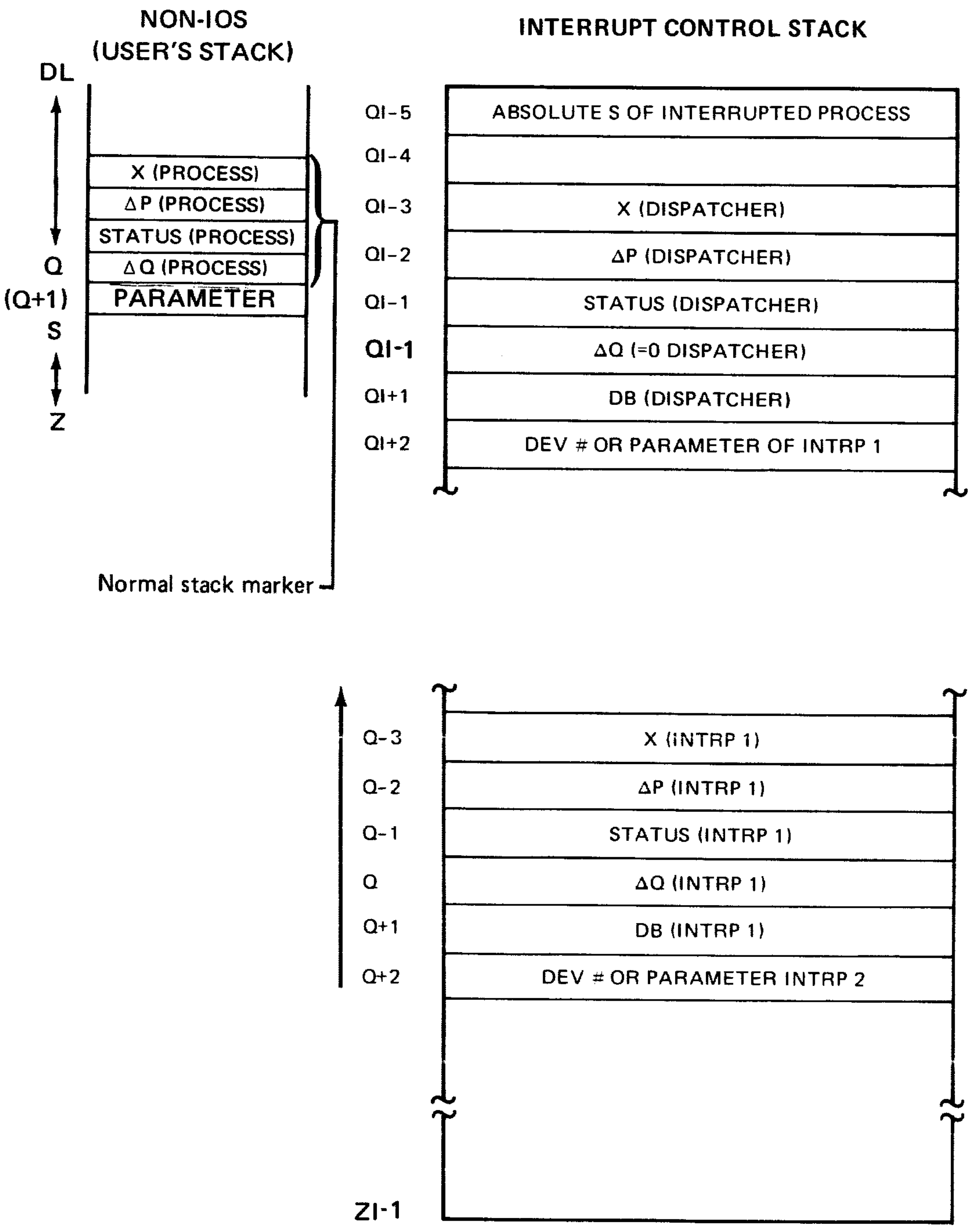
-	0
Integer Overflow	1
Floating Point Overflow	2
Floating Point Underflow	3
Integer Divide by 0	4
Floating Point Divide by 0	5
System (always enabled):	
Privileged Instruction	6
Unimplemented Instruction	7

CONDITIONS OF HARDWARE SYSTEM HALTS

A Hardware System HALT will occur if:

1. A parity error while attempting to process a parity error interrupt or while executing in the parity error segment (%12).
2. A module error while attempting to process a module error interrupt or while executing in the module error segment (%11).
3. Unable to reset interrupt line of the interrupting device during exit from the external interrupt routine.
4. The absence bit is set in one of the first 15 CST entries.
5. The code segment table length is less than 32 words.

471004-56, 2 of 2



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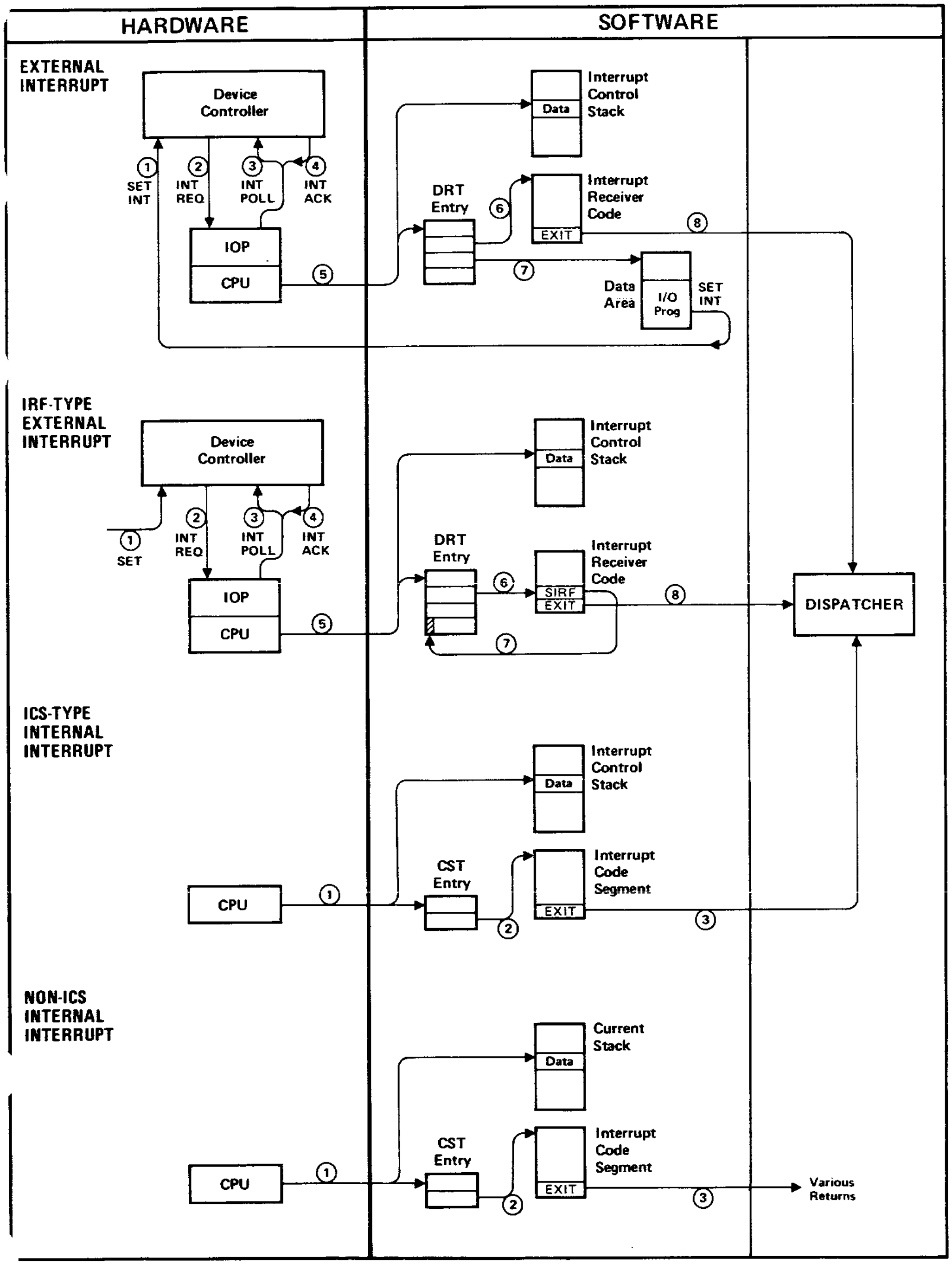
STACK MARKERS



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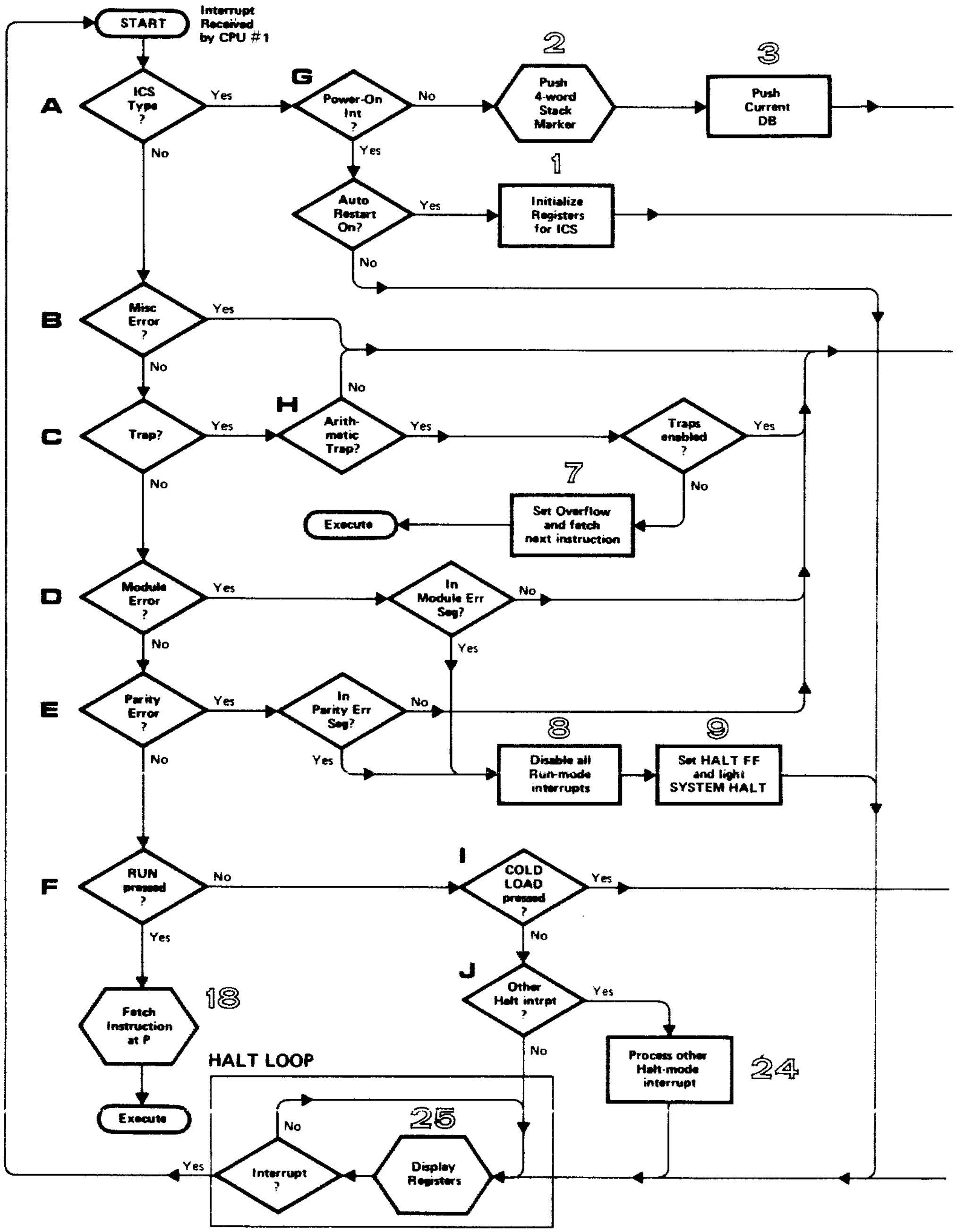
INTERRUPT SYSTEM OVERVIEW



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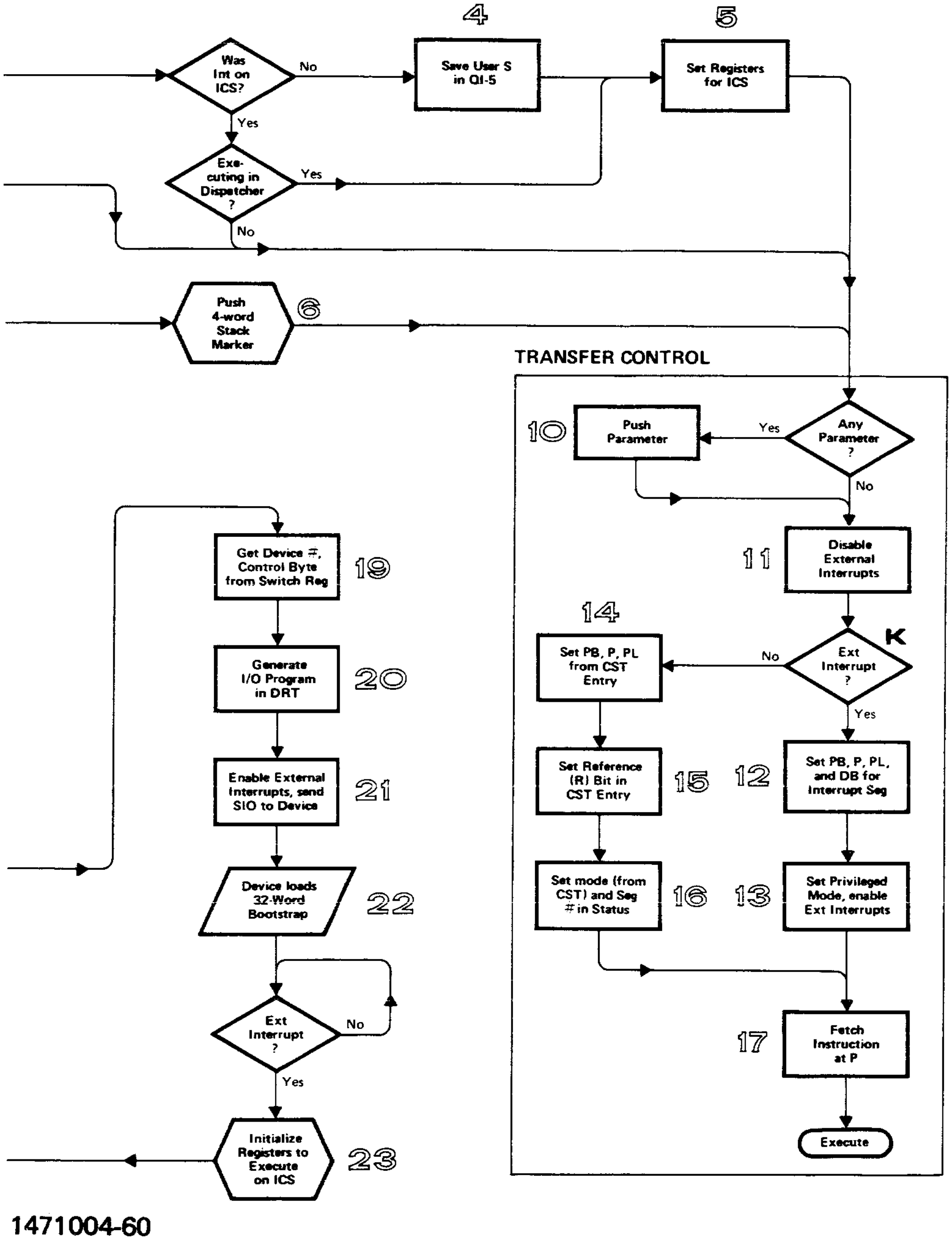
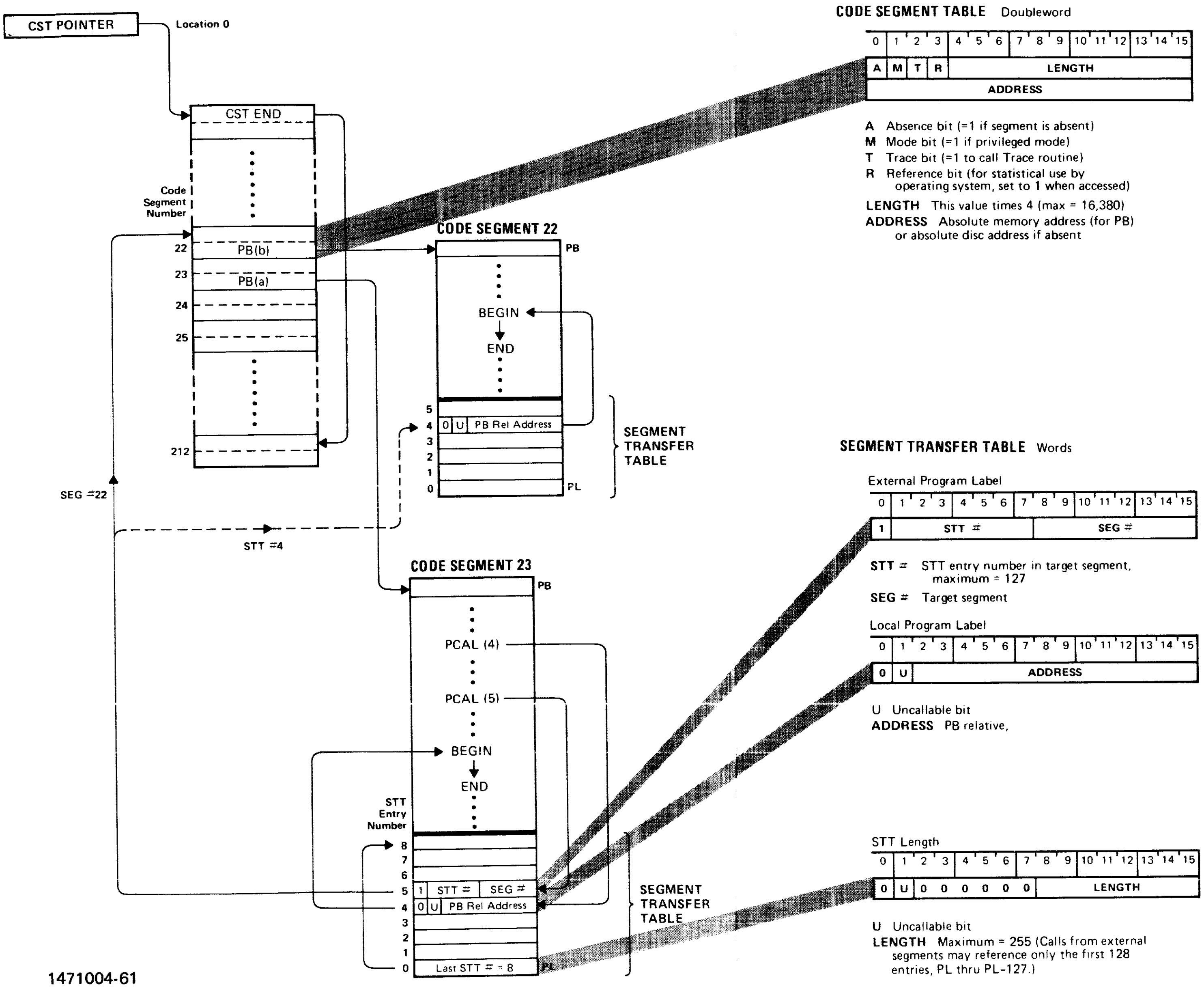
INTERRUPT HANDLER, PART A



INTERRUPT HANDLER,
PART B



CST/STT SEGMENT TRANSFER

0	CSTP	Pointer to the "Code Segment Table".		
1	P/DSTP	Cold Load program pointer/DSTP pointer to the "Data Segment Table"		
2	PCBP	Pointer to the "Process Control Block"		
3	DB	System (DB) global area		
4	CPCB1	Pointer to the current PCB entry	Processor 1	
5	QI1	Interrupt Control Stack		
6	ZI1			
7	I/C1	Interrupt Counter		
10	CPCB2	Pointer to the current PCB entry	Processor 2 (Not Used)	
11	QI2	Interrupt Control Stack		
12	ZI2			
13	I/C2	Interrupt Counter		
14		DRT entry for device #3	SIO	Program Pointer
15			PI	Interrupt Program Pointer
16			DBI	Interrupt Data Base
17			IRF	Interrupt Reference Flag
20-23		DRT for device #4, etc.		
1774-1777		Last possible DRT entry, for device #127		

SIO	Program pointer points to the absolute address of the next SIO order pair to be executed.
PI	Interrupt program address is the absolute address of this device's interrupt process program pointer.
DBI	Interrupt data base is the absolute address (DB) of this device's interrupt process data area (IOQH).
IRF	Interrupt reference flag (used by dispatcher)

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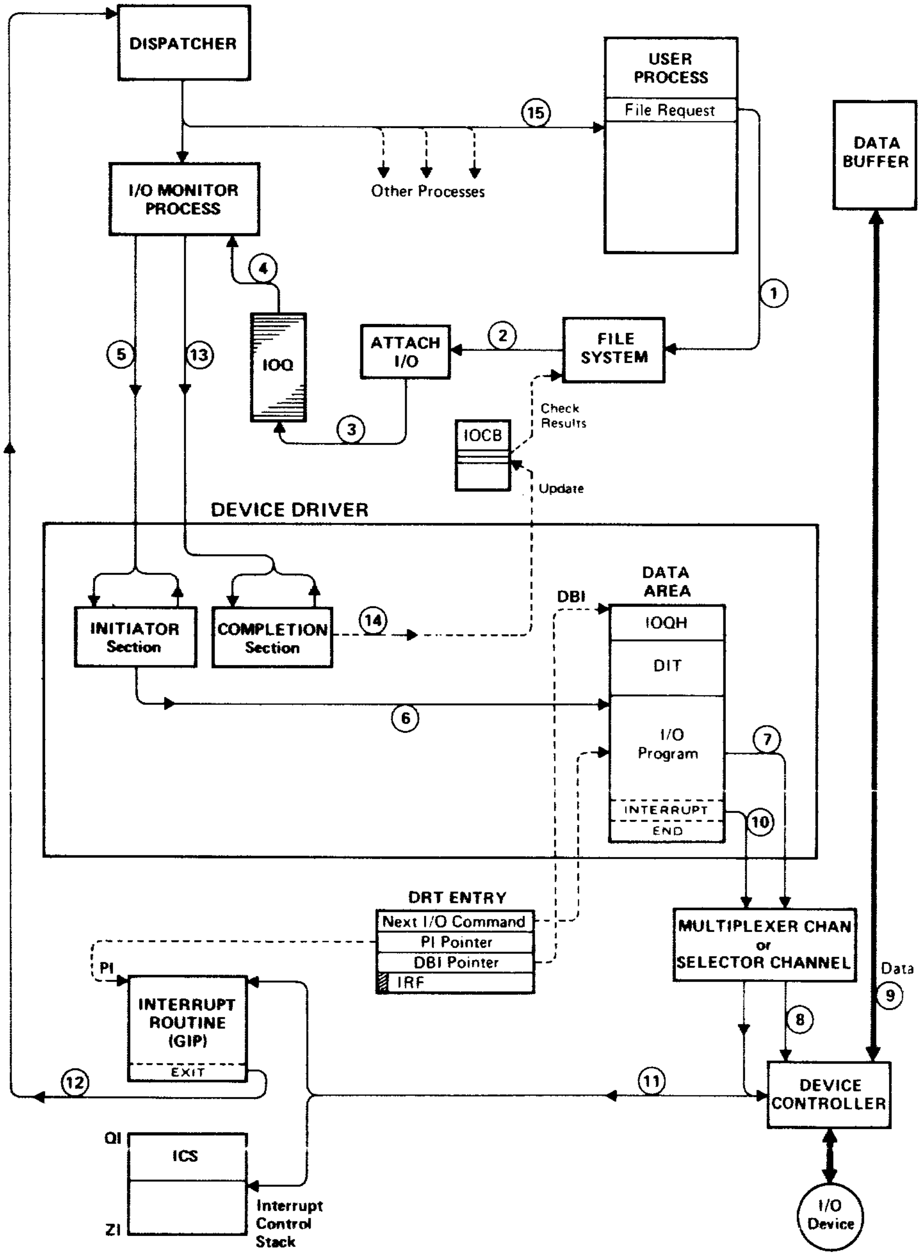
FIXED CORE LOCATIONS



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I/O SYSTEM OVERVIEW

GENERAL I/O OPERATION

Figure MPECNFG-5 is a general overview of operations in the I/O system (does not apply to direct I/O devices.) To provide a complete sequence of operations, it will be assumed that the file request will result in a need for physical I/O to be performed; as stated earlier, this will not always be the case. The sequence of operations is as follows.

1. An executing user process generates a file request to the file system.
2. The file system tests the validity of the request and calls the Attach I/O (ATTIO) intrinsic. This is the entry point to the I/O system.
3. Attach I/O inserts the request parameters in the I/O Queue for the requested device.
4. When all earlier requests for the device have been completed, and when the I/O Monitor Process has highest priority among all other processes, the I/O Monitor Process begins execution for this request.
5. The I/O Monitor process ensures that the data buffer for the file is present and frozen in memory. It then issues a PCAL to the initiator section of the device driver, passing the request parameters to that routine.

   NOTE

   A device driver normally consists of three parts: an initiator section, a completion section, and a data area. With multiple data areas, one driver may drive several devices.

6. The initiator section assembles the I/O program (using the request parameters), issues an SIO instruction to the device controller, and exits back to the I/O Monitor Process. The SIO instruction initializes the DRT to point at the starting location of the I/O program.
7. The I/O program issues commands via a multiplexer or selector channel to the device controller, on demand by the channel.
8. The device controller, on receiving a read or write command from the I/O program, transfers a block of data to or from the data buffer. The length of the block is specified by the I/O command.
9. On completion of the data transfer, the I/O program commands the device controller to request an interrupt. The I/O program then ends.

10. The device controller causes a CPU interrupt to an interrupt routine, which tells the I/O Monitor Process that an interrupt has occurred.

    NOTE

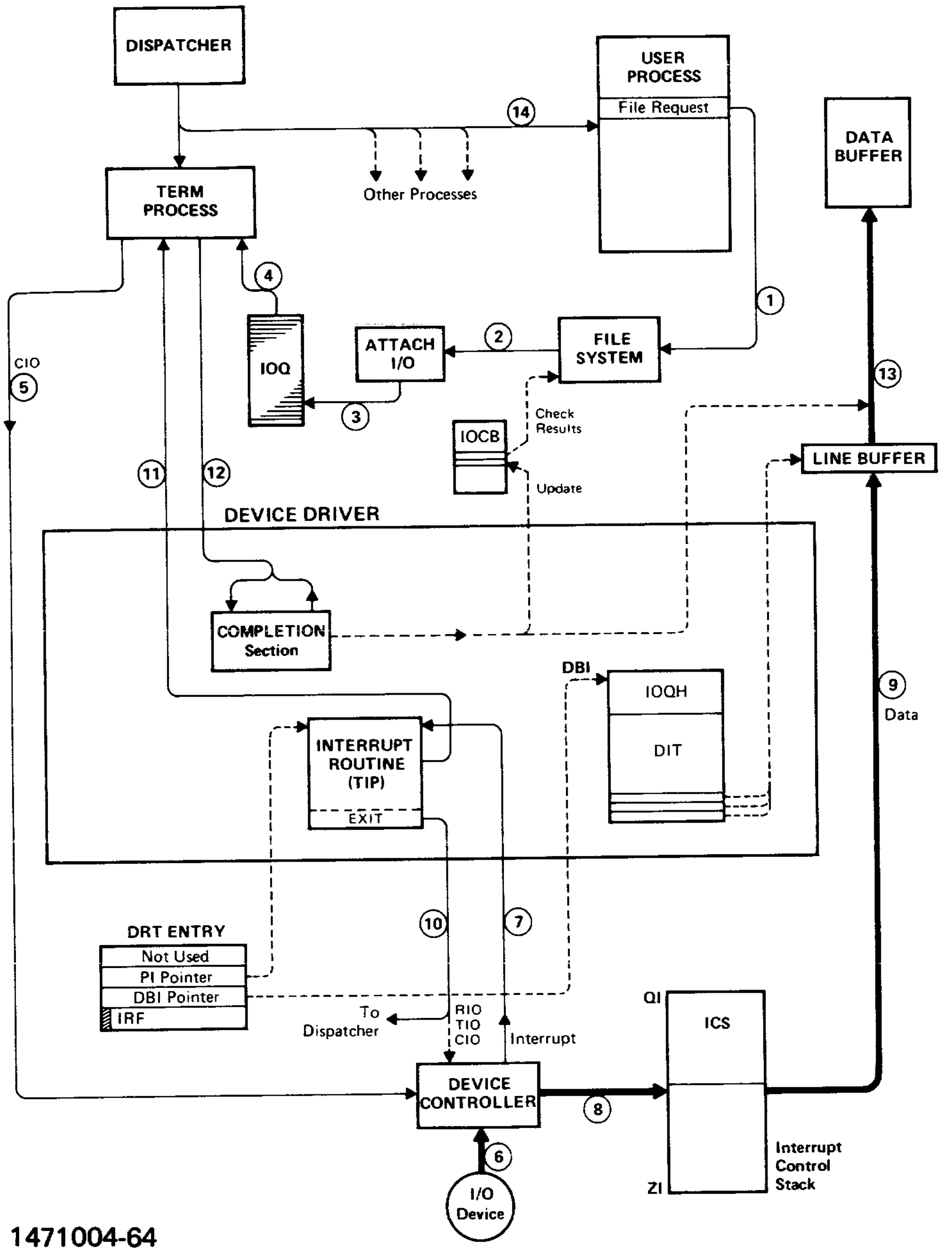
    There are currently two interrupt routines for external interrupts. One is the General Interrupt Processor (GIP) for all types of devices except terminals, and the other is the Terminal Interrupt Processor (TIP). Other interrupt routines may exist, depending on the requirements of newly developed interfaces.

11. The interrupt routine (or the last routine to use the Interrupt Control Stack) exits to the Dispatcher. It also may awaken the related I/O process if necessary.

12. When the I/O Monitor Process is again dispatched, it recognizes that an interrupt has occurred and accordingly calls the completions section of the device driver.

13. The completion section checks the results of the transfer. If necessary, it may initiate additional transfers by telling the I/O Monitor Process to call the initiator section again. Otherwise, it updates the I/O Control Block with information regarding results of the original request. The file system may then check these results. The I/O Control Block is a table of doubleword entries, with one entry for each I/O request. Each entry contains a transmission log (number of words or bytes transferred), logical I/O status, and the process number of the process to activate upon I/O completion.

14. When the user process is again dispatched, return is made to a point following the file request, depending on whether blocked or unblocked I/O was specified.



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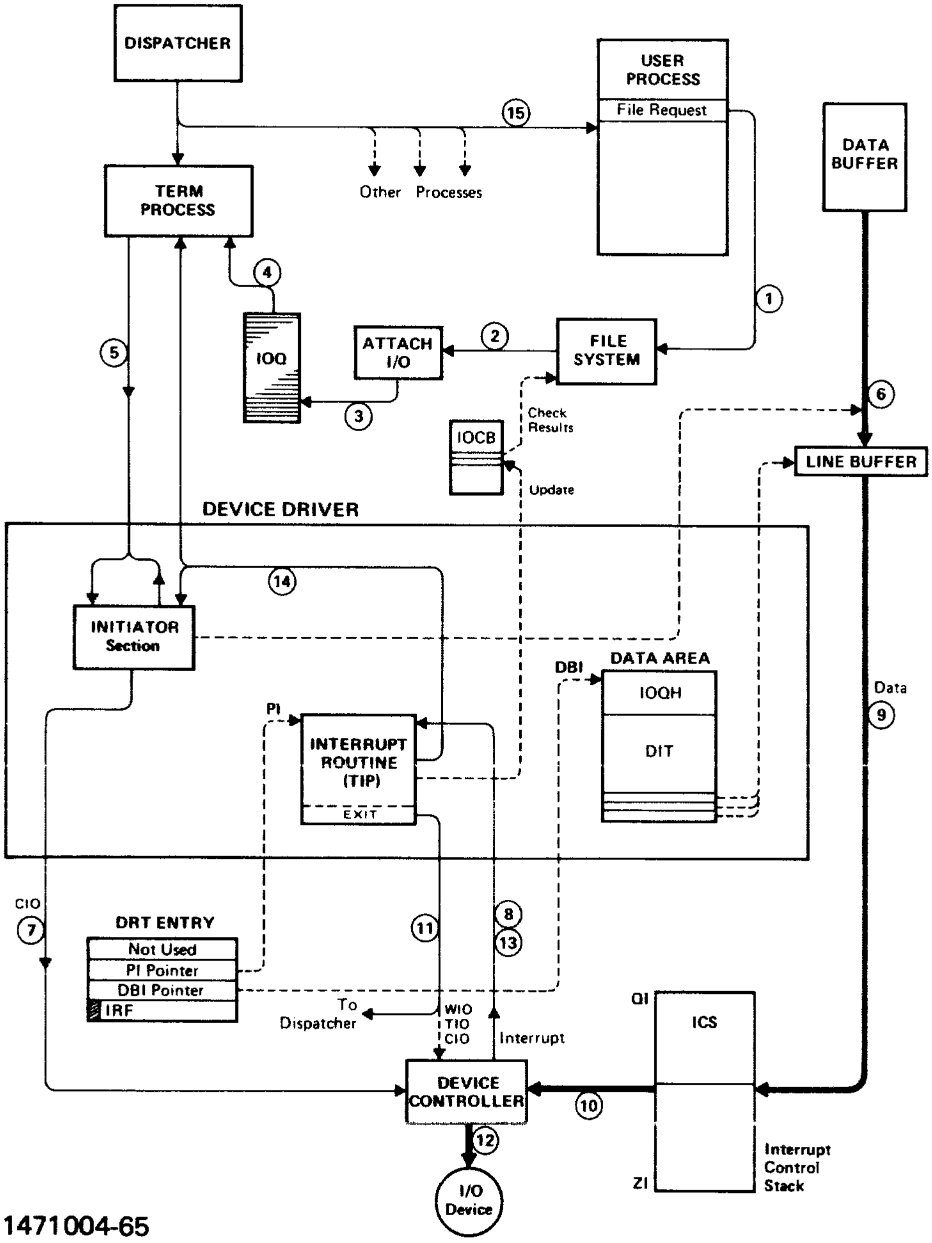
DIRECT READ FOR TERMINAL DEVICES



DIRECT WRITE FOR TERMINAL DEVICES

DIRECT I/O OPERATION

The operations for direct I/O involve considerably more software overhead than the operations for the SIO transfer mode. This is due to the varied nature of the terminal devices that use direct I/O, and also to the fact that the system must respond to commands entered via the terminal as well as to file requests affecting that terminal.

In addition, the operation is complicated by such factors as speed sensing, error sensing, whether the device is synchronous or asynchronous, whether the device is capable of reading or writing or both, what controls exist, and which mode or modes the device is capable of. Also, the log-on sequence is handled by an entirely different set of routines than those used for data handling.

Thus, the sequences described in the following paragraphs present only a broad generalization of direct I/O terminal operations. The sequences given should not be construed as representing any particular device or even a "typical" device. It will be assumed that the log-on sequence has been accomplished.

Figures MPECNFG-6 and MPECNFG-7 illustrate the handling of data viq direct I/O terminal devices. Figure MPECNFG-6 shows input (read) operations and figure MPECNFG-7 shows output (write) operations.

In comparison with figure MPECNFG-5, note that there is no I/O program in the data area; instead, the interrupt routine performs the functions of an I/O program. The interrupt routine, in this case, is part of the device driver.

Note also that direct read uses no initiation section and direct write uses no completion section. Also: no multiplexer or selector channel is involved.

One element not preciously present is the line buffer. The line buffer consists of a number of buffer tanks, which are pointed to by address words in the Device Information Table for a particular terminal. A sufficient number of these tanks is used to accommodate the line or record length of the associated device. Data is transferred between the line buffer and the device (via the Interrupt Control Stack) on a character-by-character basis. Data is tansferred between the line buffer and the data buffer on a record basis. This scheme conserves main memory space by allowing the data buffer to be absent on disc while the comparatively slow terminal device is transferring individual characters.

DIRECT READ

The sequence of operations for direct read, illustrated in figure MPECNFG-6, is as follows. Again, it will be assumed that the file request does require a physical read from the terminal.

1. The executing user process generates a file request to the file system.

2. The file system tests the validity of the request and calls the Attach I/O intrinsic.

3. Attach I/O inserts the request parameters in the I/O Queue for the requested device. Unlike the general (SIO) case, which uses a first-in/first-out queue for the requests, terminal requests are analyzed for relative importance and are then inserted into an appropriate place in the queue. The factors involved in assessing request importance are: mode (standard, escape, break, and console), and request type (standard, soft, and hard).

4. When all higher priority requests for the terminal have been completed, and when the TERM process has highest priority among all other processes, the TERM process begins execution for this request. (There is one TERM process for each terminal device controller.)

5. The TERM process enables interrupts and links together a sufficient number of buffer tanks to accommodate the request. It then issues a CIO (Control I/O) instruction directly to the device controller to enable read interrupt. TERM then exits to the dispatcher.

6. The device controller enables the device to read a character. When a key is pressed, the device returns the character to the controller.

7. On receipt of the character, the device controller causes the CPU to interrupt to the interrupt routine for terminals, TIP (Terminal Interrupt Processor).

8. TIP issues an RIO instruction to the device controller. This causes the character to be loaded onto the Interrupt Control Stack, and also causes a command to be issued to the device to read the next character. TIP now checks the character on the ICS to see if it is a data character or a control character.

9. If the character on the ICS is a data character, it is transferred by TIP to the line buffer. If it is a control character, TIP performs the appropriate control function.

10. TIP exits to the Dispatcher and the sequence repeats back to step 7 until the entire record has been read.

11. When TIP detects a CR character (Carriage Return), TIP sets a bit in the Device Information Table to signify that the record is complete, then exits back to the TERM process.

12. The TERM process, after checking the Device Information Table, issues a PCAL to the completion section of the device driver.

13. The completion section transfers the content of the line buffer to the data buffer. Then the transmission log in the I/O Control Block is updated and the completion section exits back to the TERM process.

14. TERM releases the buffer tanks and goes to sleep. The Dispatcher then returns control to the user process. To read another record, the file system must make another I/O request to Attach I/O.

DIRECT WRITE

The sequence of operations for direct write, illustrated in figure MPECNFG-7, is as follows:

1. The executing user process generates a file request to the file system.
2. The file system tests the validity of the request and calls the Attach I/O intrinsic.
3. Attach I/O inserts the request parameters in the I/O Queue for the requested device.
4. When all higher priority requests for the terminal have been completed, and when the TERM process has highest priority among all other processes, the TERM process begins execution for this request.
5. The TERM process enables interrupts and links together a sufficient number of buffer tanks to accommodate the request. TERM then issues a PCAL to the initiator section of the device driver.
6. The initiator transfers one line (maximum of 132 bytes) from the data buffer to the line buffer.
7. The initiator issues a CIO (Control I/O) instruction to the device controller to enable write interrupt and exits back to the TERM process.
8. The device controller causes the CPU to interrupt to TIP, the Terminal Interrupt Processor.
9. TIP transfers a byte to the ICS. If the byte is a control character, TIP does the control function and gets the next byte from the line buffer. If it is a data character, proceed to 10.
10. TIP executes a WIO instruction, transferring the character from the ICS to the device controller.
11. TIP then exits to the Dispatcher, while hardware takes control from this point.
12. The device controller writes the character out to the device.
13. On completion of the write, the device controller generates another interrupt to TIP. The sequence repeats back to step 9 until all characters in the record have been written out to the terminal.

14. When TIP detects a CR character (Carriage Return) in step 9, TIP checks a counter to see if this was the last line. If not, TIP calls the initiator again repeating back to step 6. If this was the last line, TIP exits back to the TERM process, which disables interrupts, releases the buffer tanks, and goes to sleep.

15. The Dispatcher then returns control to the user process.

I/O TABLES (CORE RESIDENT)

LOGICAL PHYSICAL DEVICE TABLE - LPDT

Maps a logical device number into a DRT and UNIT number. This table also contains flags defining the logical state of the device.

DEVICE REFERENCE TABLE - DRT

Defines interrupt handler and contains a pointer to the IOQ head for the controller and thus links the device to the appropriate I/O process.

I/O QUEUE HEAD - IOQH

One IOQH is associated with each controller. It contains external program labels for the I/O monitor and driver procedures, the PCB number of the I/O process and defines the number and size of the DIT's. It also contains flags defining the type and state of the I/O monitor.

DEVICE INFORMATION TABLE - DIT

One DIT is associated with each device on the controller. This table defines the location of the I/O request queue for the device and contains information defining the current state of the device.

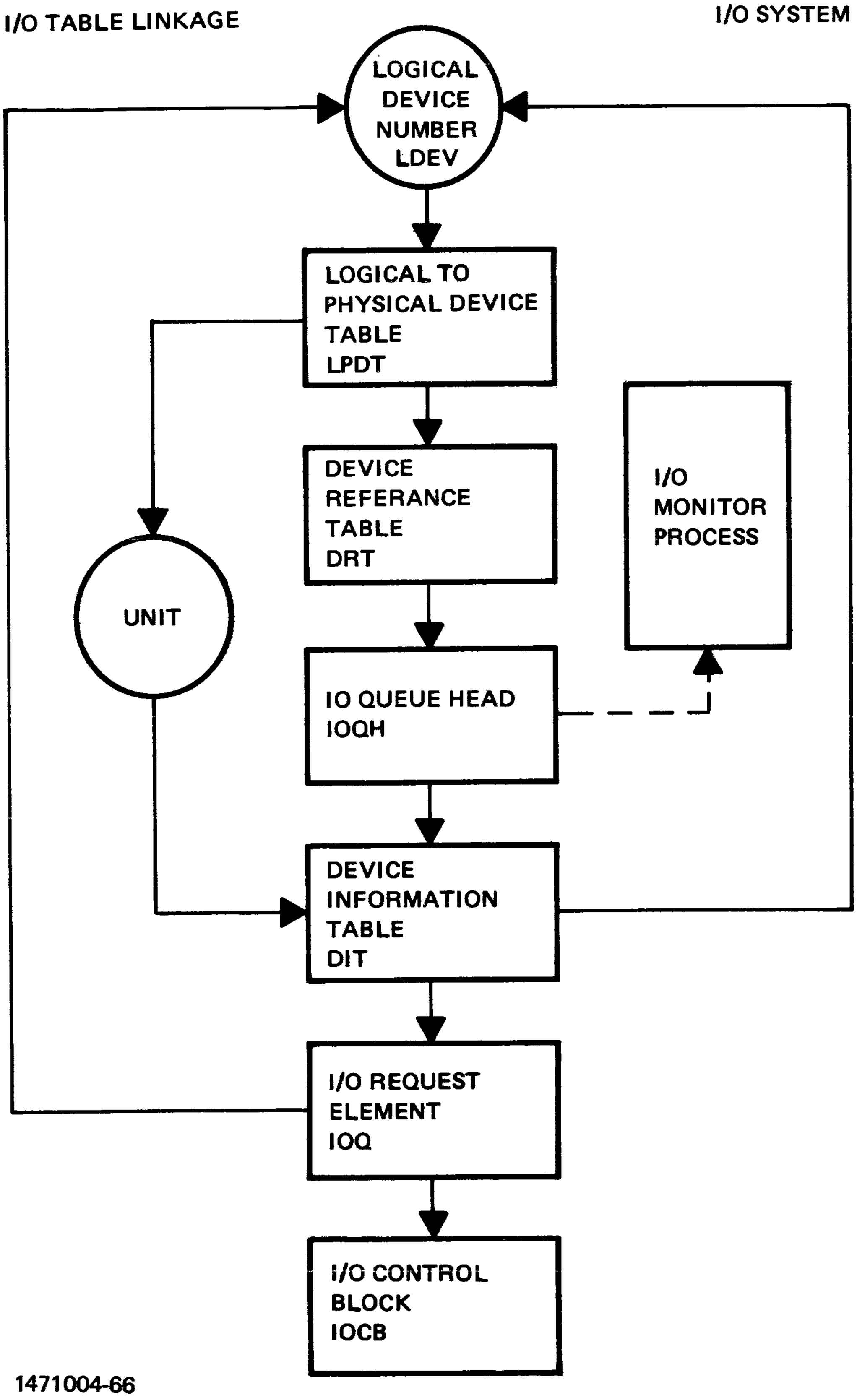
I/O Request Block - IOQ

One IOQ element is associated with each I/O request. The IOQ element contains all the necessary parameters to perform the I/O and information defining the state of the request. Linked entries form the request queue for the device.

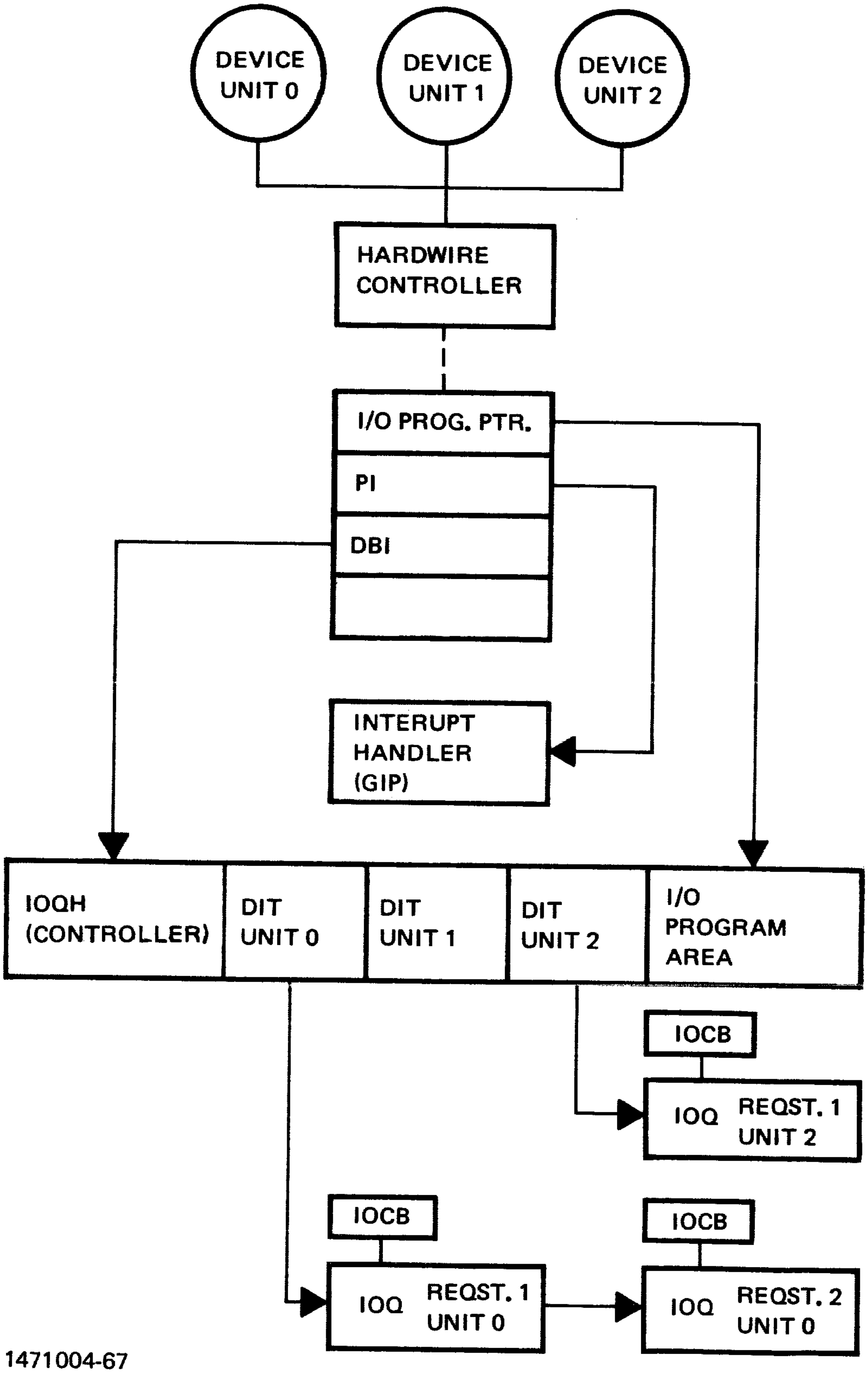
I/O Control Block - IOCB

At the end of an I/O request a logical status and transmission log is returned to the user through this entry.

From any one table and knowing the unit number of the device it is possible to get to any table in the system as shown in the I/O TABLE LINKAGE Diagrams.



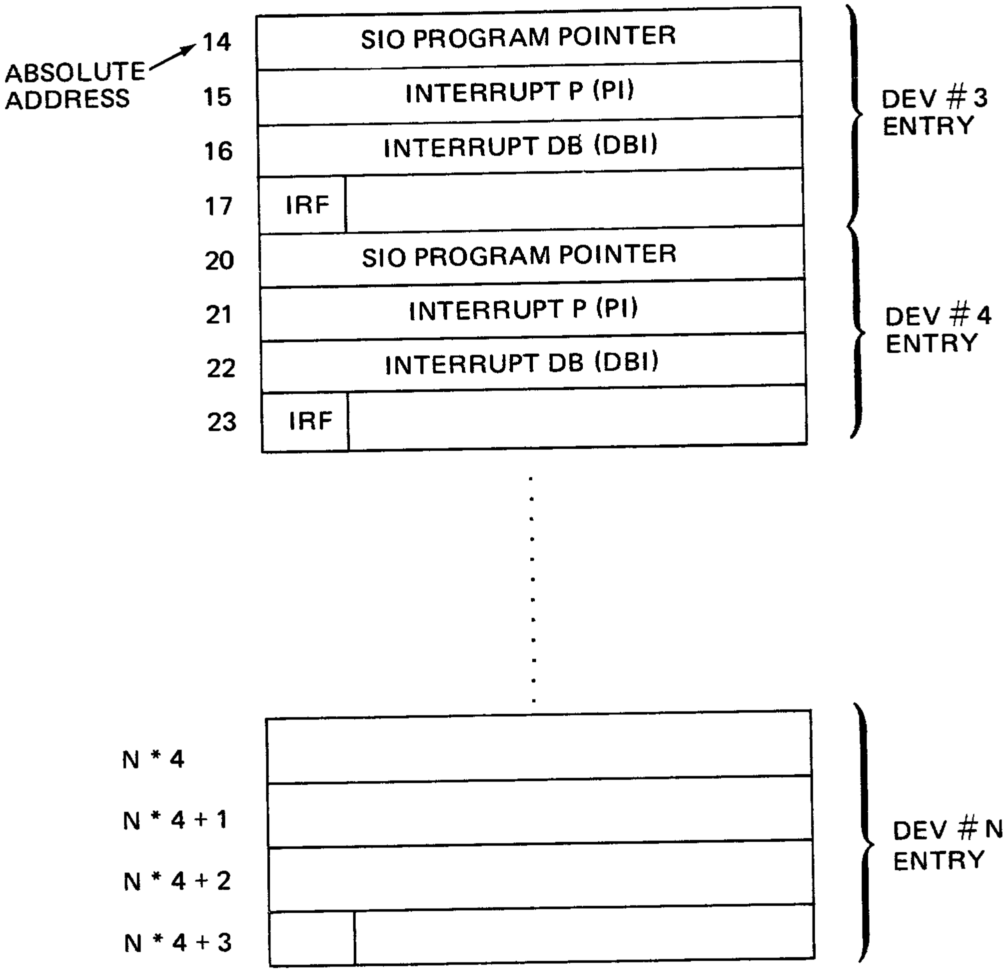
I/O TABLE LINKAGE



1471004-67

I/O TABLE RELATIONSHIPS

THIS DEDICATED TABLE CONTAINS ONE 4 WORD ENTRY FOR EACH DEVICE NUMBER, UP TO THE MAXIMUM OF 253 DEVICES. THE FIRST WORD OF EACH ENTRY CORRESPONDS TO A UNIQUE DEVICE AND CONTAINS THE ADDRESS OF THE NEXT I/O COMMAND INSTRUCTION FOR THAT DEVICE. THE SECOND WORD OF EACH ENTRY CONTAINS THE ABSOLUTE PROGRAM ADDRESS PI AT WHICH EXECUTION WILL BEGIN FOR THAT EXTERNAL INTERRUPT, AND THE THIRD WORD CONTAINS THE ABSOLUTE DATA BASE ADDRESS DBI ASSOCIATED WITH THAT EXTERNAL INTERRUPT. BIT 0 OF THE FOURTH WORD IS THE INTERRUPT REFERENCE FLAG, IRF. IT MAY BE SET BY THE SIRF INSTRUCTION TO INDICATE THE PRESENCE OF AN INTERRUPT FROM THE DEVICE. NOTE THAT DEVICE NUMBERS 0, 1, 2 DO NOT EXIST.



NOTE: $3 \leqslant N \leqslant 255_{10}$

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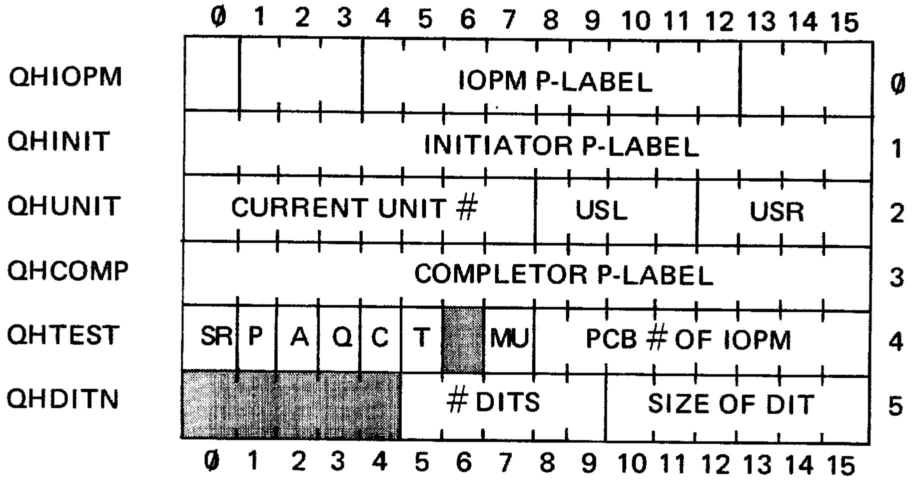
DEVICE REFERENCE TABLE (DRT)

IOQH TABLE FORMAT



QHIOPM · (0:8) – UNIT # OF DEVICE CURRENTLY BEING SERVICED BY IOPM

· (8:4) – USL = UNIT SHIFT LEFT

· (12:4) – USR = UNIT SHIFT RIGHT

NOTE: TO EXTRACT UNIT NO. FROM DEVICE STATUS:

1. IF BOTH USL AND USR ARE 0 THEN THE UNIT NUMBER IS ALWAYS ZERO.
2. OTHERWISE, SHIFT THE STATUS LEFT BY USL.
3. SHIFT THE RESULT RIGHT BY USR. THE RESULT IS THE UNIT NUMBER, RIGHT ADJUSTED.

QHCOMP P-LABEL OF DRIVER COMPLETOR SECTION

QHTEST · (0:1) – SR = 1 IF SERVICE REQUESTED FOR THIS CONTROLLER

· (1:1) – P = 1 IF IOPM IS A PROCEDURE

· (2:1) – A = 1 IF IOPM IS ACTIVE

· (3:1) – Q = 1 IF REQUESTS FOR IOPM MAY BE QUEUED ON MONITOR REQUEST QUEUE

· (4:1) – C = 1 IF IOPM IS CORE RESIDENT WHICH MAY

· (5:1) – T = 1 IF DEVICE IS TERMINAL CONTROLLER

· (7:1) – MU = 1 IF MULTIPLE UNITS ON THIS CONTROLLER

· (8:8) – PHYSICAL PCB # OF IOPM PROCESS

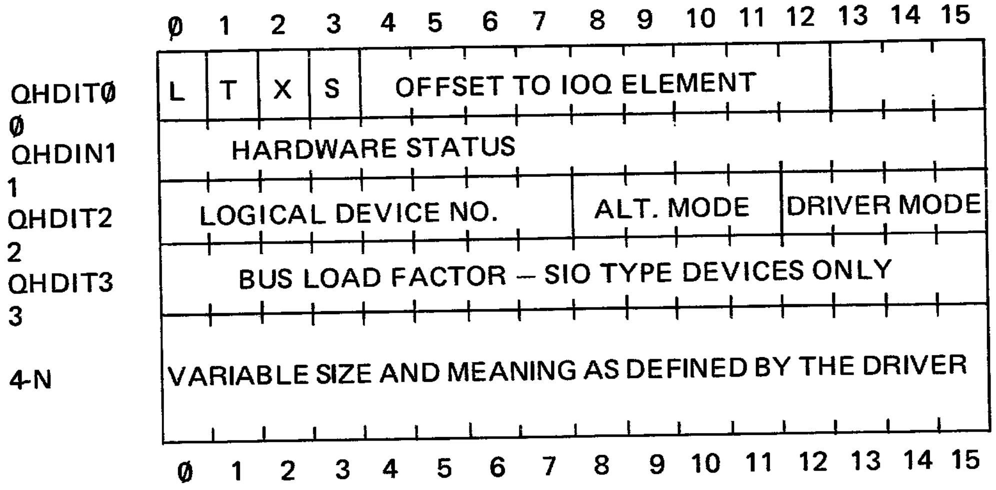
QHDITN · (5:5) – # DITS FOR THIS CONTROLLER

· (10:6) – SIZE OF EACH DIT IN WORDS

1471004-69

IOQH TABLE FORMAT

DIT GENERAL FORMAT



DIT – FIELD DEFINITIONS

QHDIT0 . (0:1) – L ON LINE BIT.
L=0 MEANS DEVICE OFF LINE.
L=1 MEANS DEVICE ON LINE.
. (1:1) – T TIME OUT BIT.
T=0 MEANS NO TIME OUT.
T=1 MEANS TIME OUT.
. (2:1) – X BYPASS THIS DIT BIT.
X=0 MEANS CHECK THIS DIT FOR POSSIBLE SERVICE.
X=1 MEANS IGNORE THIS DIT.
. (3:1) – S SUB MODE SELECT.
S=0 MEANS GET MODE FROM IOQ ELEMENT.
S=1 MEANS GET MODE FROM QHDIT2.(8:4), ALT MODE FIELD.
. (4:12)– OFFSET FROM BASE OF IOQ TO THE IEQ ELEMENT CURRENTLY BEING USED BY THIS DIT.

QHDIT1 . (0:16)– HARDWARE STATUS OF DEVICE CONTROLLER AT TIME OF LAST INTERRUPT ASSOCIATED WITH THIS DIT.

QHDIT2 . (0:8) – LOGICAL DEVICE NUMBER OF THIS DIT.
. (8:4) – ALTERNATE MODE – USED ONLY WHEN S-BIT OF QHDIT0 IS SET. (I.E. ONLY WHEN THERE IS NO IOQ ELEMENT ASSOCIATED WITH THIS DIT).

QHDIT3 . (0.16) – BUS LOAD FACTOR. USED BY SIO TYPE DRIVERS TO MONITOR THE LOAD ON THE SIO BUS. THE VALUES CORRESPOND TO "EFFECTIVE" WORD RATES IN KILO-WORDS PER SECOND.

1471004-70

DIT GENERAL FORMAT

```
          0   1   2    3   4   5   6   7   8   9  10 11 12 13 14 15
        ------------------------------------------------------------
QLINK|                                                              |
0    |          NEXT IOQ LINK (IOQ TABLE DISPLACEMENT)              |
     |--------------------------------------------------------------|
QLDEV|    |   |        |               |                            |
1    |PR  | X |        |      SC       |  LOGICAL DEVICE NUMBER     |
     |--------------------------------------------------------------|
QFLAG|    |NO | NO |   |   |   |   |   |                            |
2    | Z  |PCB|IOCB|AW | D |   | B | M |        PCB NUMBER          |
     |--------------------------------------------------------------|
QDSTN|    |   |                |                                    |
3    |ABT| I |      MODE      |          DST NUMBER                |
     |--------------------------------------------------------------|
QIOCB|                                                              |
4    |                     IOCB ADDRESS                             |
     |--------------------------------------------------------------|
QBUFF|                                                              |
5    |                    BUFFER ADDRESS                            |
     |--------------------------------------------------------------|
QFUNC|                                                       |FUNC  |
6    |                                                       |CODE  |
     |--------------------------------------------------------------|
QWBCT|                                                              |
7    |                   COUNT (WORD/BYTE)                          |
     |--------------------------------------------------------------|
QPAR1|                                                              |
8    |                    FIRST PARAMETER                           |
     |--------------------------------------------------------------|
QPAR2|                                                              |
9    |                   SECOND PARAMETER                           |
     |--------------------------------------------------------------|
QMISC|                                                              |
10   |               EXTRA STORAGE FOR DRIVER                       |
     |--------------------------------------------------------------|
QMEM |                                                              |
11   |            PARTIAL READ ABSOLUTE ADDRESS                     |
        ------------------------------------------------------------
          0   1   2    3   4   5   6   7   8   9  10 11 12 13 14 15
```

471004-71/72, sheet 1 of 3

IOQ ENTRY GENERAL FORMAT

IOQ ENTRY FIELD DEFINITIONS, sheet 1 of 2

```
QLINK   (0:1) - INDEX OF NEXT IOQ ELEMENT RELATIVE TO IOQ TABLE
                 BASE. ZERO INDICATES END OF LIST.
QLDEV   (0:1) - PR PARTIAL READ OF DATA SEGMENT. USED ONLY FOR
                 TERMINAL WRITES.
        (1:1) - X IGNORE THIS REQUEST.
        (2:2) - NOT USED.
        (4:4) - SC NUMBER OF SECTORS FOR PARTIAL READ.
        (8:8) - LOGICAL DEVICE NUMBER.
QFLAG   (0:1) - DATA FROZEN
                 IF DST NUMBER >0 THEN
                 Z = 0 DATA NOT FROZEN
                 Z = 1 DATA FROZEN
        (1:1) - NO PCB NUMBER IS TO BE ASSOCIATED WITH THIS
                 REQUEST. USED ONLY FOR CONTROL FUNCTIONS WHERE
                 NO DATA BUFFER IS NECESSARY. CAUSES NO IOCB FLAG
                 TO BE SET ALSO.
        (2:1) - N = 0 MEANS THE USER SUPPLIED THE IOCB.
              - N = 1 MEANS THE SYSTEM SUPPLIED THE IOCB.
        (3:1) - AW = 0 DO NOT WAKE CALLER WHEN I/O REQUEST IS
                 FINISHED.
        (4:1) - RESERVED FOR DIAGNOSTIC REQUEST FLAG.
        (5:1) - NOT USED.
        (6:1) - BLOCKED I/O BIT.
                 B = 0 MEANS UNBLOCKED (BUFFERED)
                 B = 1 MEANS BLOCKED (UNBUFFERED)
        (7:1) - MEMORY MANAGEMENT BIT.
                 M = 0 MEANS THIS REQUEST NOT FROM MEMORY
                        MANAGEMENT.
                 M = 1 MEANS THIS REQUEST IS FROM MEMORY
                        MANAGEMENT
        (8:8) - PROCESS CONTROL BLOCK (PCB) NUMBER.
QDSTN   (0:1) - ABORT REQUEST IF ABT = 1
        (1:1) - INTERRUPT ACKNOWLEDGE BIT
                 1 BIT SET TO 1 BY INTERRUPT ROUTINE AT INTERRUPT
                 1 BIT SET TO 0 BY DRIVER WHEN SERVICED
        (2:4) - MODE FIELD
                 00 = NEW I/O REQUEST
                 01 = DATA BUFFER PRESENT
                 02 = CALL INITIATOR
                 03 = CALL COMPLETOR
                 04 = CALL ERROR SECTION
                 05 = END OF I/O REQUEST
                 06 = DEVICE RECOGNITION
                 07 = UNUSED
                 10 = RESORT REQUEST ON INTERRUPT
                 11 = UNFREEZE DATA BUFFER THEN MODE SET TO 10
                 12 = WAIT FOR INTERRUPT OR CLOCK THEN GO TO INIT.
                 13 = WAIT FOR INTERRUPT OR CLOCK THEN GO TO COMP.
```

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IOQ ENTRY FIELD DEFINITIONS, sheet 2 of 2

14 = WAIT FOR INTERRUPT OR CLOCK THEN GO TO ERROR.
15 = WAKE CALLER BUT DO NOT FINISH REQUEST UNTIL INTERRUPT.
16 = WAKE CALLER THEN MODE SET TO 15
17 = UNASSIGNED.

QDSTN (6:10) - DST NUMBER. IF <> 0 THEN REQUEST IS "DST RELATIVE" ELSE THE REQUEST IS "ABSOLUTE".
QIOCB (0:16) - ADDRESS OF INPUT/OUTPUT CONTROL BLOCK ENTRY.
QBUFF (0:16) - ADDRESS OF DATA BUFFER
QFUNC (14:2) - FUNCTION CODE OF REQUESTED I/O.
QWBCT (0:16) - COUNT. POSITIVE MEANS WORDS. NEGATIVE MEANS BYTES.
QPAR1 (0:16) - FIRST PARAMETER. DEFINED BY FILE SYSTEM.
QPAR2 (0:16) - SECOND PARAMETER. DEFINED BY FILE SYSTEM.
QMISC (0:16) - EXTRA STORAGE FOR DRIVER. REQUEST DEPENDENT. (NOT PASSED TO ATTIO).
QMEM - IF PARTIAL READ THEN CONTAINS ABSOLUTE CORE ADDRESS OF PARTIAL READ BUFFER.

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```
          0                  7 8               15
          |------------------|-----------------|
          | HIGHEST ENTRY NO. | ENTRY SIZE = 2  |
    0     |------------------------------------|
          |  TOTAL NO. OF DEVICES REQ. SERVICE |
          |------------------------------------|

          0                  7 8               15
          -------------------|------------------
          |    DEVNO         |    UNIT NO.     |
    1     |------------------------------------|
          |S|S|J |A|C|D|I|X|Y|E|B  | L |SUB TYPE |
          --|-|-|-|-|-|-|-|-|-|-|--|--|--|--|--|--|
           0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

          .
          .
    N     .
          .


          ------------------------------------------
          |SS=0 | AVAILABLE                        |
          |  =1 | RECOGNIZED OR OWNED              |
          |  =2 | REQUESTING SERVICE               |
          |  =3 | SERVICE GRANTED                  |
          | J=1 | ACCEPT JOB OR SESSION            |
          | A=1 | ACCEPT DATA                      |
          | C=1 | CONTROL Y OCCURRED               |
          | D=1 | DUPLICATIVE                      |
          | I=1 | INTERACTIVE                      |
          | X=1 | COLON                            |
          | Y=1 | :JOB, :EOJ, :DATA, :EOD          |
          | E=1 | END-OF-FILE (PHYSICAL)           |
          | B=1 | BREAK OCCURRED                   |
          | L=1 | COMD. BRK OCCURRED OR IS DISALLOWED |
          |                                        |
          | SUB TYPE: SAME AS DEFINED IN MPE MANUAL |
          ------------------------------------------
```

LOGICAL PHYSICAL DEVICE TABLE (LPDT)
INDEXED BY LOGICAL DEVICE NUMBER

ERROR NUMBER (enum) (1)	SEGMENT NAME (2)	DELTA-P (pnum) (3)	PROCEDURE NAME (4)	OFFSET IN PROCEDURE (5)	CAUSE OF ERROR (6)
1	MMCORER	1406	GETMAINMEM	11	No memory condition where recovery was impossible.
2	MMDISKR	714	GETDATASEG	14	Data segment request of zero length.
3	MMDISKR	2561	RETRUNENTRYS	100	Attempt to return a CST, DST, or PCB unassigned entry.
4	DIRC	4425	DIRREAD	44	I/O error reading directory block.
4	DIRC	4603	DIRWRITE	55	I/O error writing directory block.
4	DIRC	5056	DWRITEBITMAP	27	I/O error writing directory space bit map.
6	MMCORER	700	MAKEPRESENT	275	Attempt to make present a segment of zero length.
7	MMCORER	454	MAKEPRESENT	51	Attempt to make present a DST entry which contains a 0 in first word of descriptor.
10	MMCORER	461	MAKEPRESENT	56	Attempt to make present an unassigned CST or DST entry.
14	MMDISKR	261	CHANGESTACK	75	Illegal stack operation (expansion, contraction) while locked in memory.
15	UCOP	1254	CHANGESTACK	435	System stack overflow.
16	UCOP	1161	CHANGESTACK	342	PCBX expansion overflow.
17	UCOP	771	CHANGESTACK	633	Stack was not overlayed due to multiple setting of freeze counter.
17	UCOP	1452	CHANGESTACK	152	

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LIST OF SYSTEM FAILURES, sheet 1 of 7

ERROR NUMBER (enum) (1)	SEGMENT NAME (2)	DELTA-P (pnum) (3)	PROCEDURE NAME (4)	OFFSET IN PROCEDURE (5)	CAUSE OF ERROR (6)
20	ABORTRAP	1727	ABORT	1242	System process abort.
21	ABORTRAP	1736	ABORT	1251	Critical mode abort.
22	MORGUE	141	EXPIRE	54	Process terminates with a SIR.
23	MORGUE	600	EXPIRE	522	Terminated process runs.
30	CXSTOREST	164	CXRESTORE	164	Error returned from ZSIZE to reduce main process stack.
30	CXSTOREST	1143	CXRESTORE	1143	Error returned from ZSIZE to increase main process stack.
30	CXSTOREST	1333	CXRESTORE	1333	Error returned from ZSIZE to reduce main process stack.
30	CXSTOREST	2400	CXSTORE	146	Error returned from ZSIZE to reduce main process stack.
30	CXSTOREST	3151	CXSTORE	717	Error returned from ZSIZE to increase main process stack.
30	STORE	570	IRESTORE	570	Bad data returned from PRODUCEPARMS.
30	STORE	2551	FSTORE	1070	Error in computing file size while dumping file.
30	RESTORE	7	ADSUSTFPTR	7	Error in call from DIRECSCAN.

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LIST OF SYSTEM FAILURES, sheet 2 of 7

ERROR NUMBER (enum) (1)	SEGMENT NAME (2)	DELTA-P (pnum) (3)	PROCEDURE NAME (4)	OFFSET IN PROCEDURE (5)	CAUSE OF ERROR (6)
30	RESTORE	214	TAPESWITCH	165	Error returned from FCONTROL for forward file space.
30	RESTORE	264	FRESTORE	36	Error returned from DEALLOCATE for deallocation of disc where file is being written.
30	RESTORE	456	FRESTORE	230	Error returned from FCONTROL for forward file space.
30	RESTORE	1042	FRESTORE	614	Error in parameters to DISKSPACE when returning space for old copy of file which is being restored.
30	RESTORE	1051	FRESTORE	623	Disk free space table full when returning disc space which may later have to be retrieved. Reload to compact disc space map.
30	RESTORE	2503	FRESTORE	2255	Bad extent size parameters passed to DISKALLOC
30	RESTORE	2514	FRESTORE	2266	Bad logical device passed to DISKALLOC.
30	RESTORE	2562	FRESTORE	2334	Bad extent size parameters passed to DISKALLOC.
30	RESTORE	2652	FRESTORE	2424	Attempt to get specific disc space failed because guaranteed space is no longer available.
30	RESTORE	2655	FRESTORE	2427	
30	RESTORE	2730	FRESTORE	2502	Bad device class passed to DISKALLOC.

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LIST OF SYSTEM FAILURES, sheet 3 of 7

ERROR NUMBER (enum) (1)	SEGMENT NAME (2)	DELTA-P (pnum) (3)	PROCEDURE NAME (4)	OFFSET IN PROCEDURE (5)	CAUSE OF ERROR (6)
30	RESTORE	3436	FRESTORE	3210	Error returned from DEALLOCATE for deallocation of disc where file is being written.
31	CROUTINE	316	PSEUDOINT	56	Pseudo interrupt mode is 0.
32	MORGUE	316	EXPIRE	240	Still a RIN locked after ABORTRIN.
33	PINT	554	ABORTPROG	14	No son while :ABORTing.
36	PCREATE	3113	INSERT	42	Expects a sub queue block as parameter.
37	MORGUE	152	EXPIRE	74	TERMINATE called in critical mode.
40	PCREATE	432	LOG	432	Log record not defined.
41	PCREATE	321	LOG	321	Parameter type not defined.
42	PCREATE	1144	LOG	1144	Both buffers are full.
50	IOCDRD0	55	CARDCOMP	34	CIO instruction failure.
50	IOCDRD0	146	CARDCOMP	125	CIO instruction failure.
50	IOCDRD0	330	CARDINIT	17	CIO instruction failure.
50	IOCDRD0	360	CARDINIT	47	TIO instruction failure.
50	IOCDRD0	433	CARDINIT	122	TIO instruction failure.
52	IOUTILTY	1545	DISKIO	151	Irrecoverable disc error.
53	IOMDISK0	271	IOMDISK0	271	Illegal write to protected area on disc.
53	IOFDISK0	43	IOFDISK0	43	Illegal write to protected area on disc.
53	IOMDISK1	673	IOMDISK1	673	Illegal write to protected area on disc.

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LIST OF SYSTEM FAILURES, sheet 4 of 7

ERROR NUMBER (enum) (1)	SEGMENT NAME (2)	DELTA-P (pnum) (3)	PROCEDURE NAME (4)	OFFSET IN PROCEDURE (5)	CAUSE OF ERROR (6)
54	PROGEN	3515	CONSABORT JOB	47	Invalid main PIN.
55	RINS	615	UNLOCKGLORIN	65	Global RIN flag reset (error).
56	RINS	510	FREELOGRIN	117	Attempt to deallocate a non-allocated RIN.
62	FILESYS4	1422	FTROUBLE	2	File system error*
65	DISKSPC	215	XDISKSPACE	215	Disc space requested not available.
70	IOUTILTY	4452	GETIOENTRY	14	No more entries available in table: IOQ (I/O Queue), TBUF (Terminal Buffer), IOCB (I/O Control Block), MPRQ (Make Present Request Queue), TRL (Timer Request List).
71	IOUTILTY	1753	GETIOPOINTERS	10	Bad logical device number.
72	ALLOCATE		GETCLASS		Bad class address passed.
73	ALLOCATE		ALLOCATE		Bad logical device number in class table.
74	ALLOCATE		ALLOCATE		Device owned by caller but no entry.
76	ALLOCATE		ALLOCATE		INDX invalid.
100	ALLOCATE	3547	SOPEN	54	An output devicefile is destined for an undefined class.
101	ALLOCATE	3761	SALLOCSACB	22	Attempt to allocate more than the configured maximum number of opened spoofles.

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LIST OF SYSTEM FAILURES, sheet 5 of 7

ERROR NUMBER (enum) (1)	SEGMENT NAME (2)	DELTA-P (pnum) (3)	PROCEDURE NAME (4)	OFFSET IN PROCEDURE (5)	CAUSE OF ERROR (6)
102	ALLOCATE	4062	SALLOCSACB	123	Allocated Spool Data Segment is full.
103	ALLOCATE	4120	SALLOCSACB	161	Virtual device being allocated is already in use.
104	ALLOCUTIL	3477	SDEALLOCSACB	47	Spool Data Segment in use is not in primal spool table.
105	ALLOCUTIL	3513	SDEALLOCSACB	63	There are no Spool Access Control Blocks in the Spool Data Segment being allocated.
106	SPOOLUTIL	1614	SMAPPER	31	Invalid number of sectors requested for spoofle extent.
107	IOUTILITY	632	ATTIO	56	Hardware address is zero for logical device specified.
110	IOUTILITY	637	ATTIO	63	Logical device specified is not positive.
111	IOUTILITY	647	ATTIO	73	Logical device number too big.
120	ALLOCUTIL		ALLOCENTRY		Altering XDD segment size failed.
121	ALLOCUTIL		DEALLOCENTRY		Altering XDD segment size failed.
122	SPOOLCOMS		INITSPOOLING		Initial spooling attempt failed.
123	SPOOLCOMS		DELETEJOB		ABORTJOB failed.
130	ININ		PARITYERR		Memory Address parity error.
131	ININ		PARITYERR		System parity error.
132	ININ		PARITYERR		Irrecoverable memory parity error.

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LIST OF SYSTEM FAILURES, sheet 6 of 7

ERROR NUMBER (enum) (1)	SEGMENT NAME (2)	DELTA-P (pnum) (3)	PROCEDURE NAME (4)	OFFSET IN PROCEDURE (5)	CAUSE OF ERROR (6)
200	IOUTILTY	4511	GETIOENTRY	23	Index of allocated entry is out of bounds.
201	IOUTILTY	4521	GETIOENTRY	33	
202	IOUTILTY	4446	RELIOENTRY	23	Index of deallocated entry is out of bounds.
203	IOUTILTY	4453	RELIOENTRY	30	
204	IOPM	2044	TERMIOPM	1541	IOCB accessed although not allocated.
205	IOTERMO	42	MINIT	12	IOCB accessed although not allocated.
206	IOTERMO	42	MINIT	12	IOCB accessed although not allocated.

*A file system error is caused by one of the following reasons:

- ALTDSEGSIZE error
- CORESEG failure
- DEALLOCATE error
- DIRECFINDFILE error
- DIRECPURGEFILE error
- DISKSPACE error
- REMJTENTRY error
- I/O error initializing extent

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LIST OF SYSTEM FAILURES, sheet 7 of 7

MPE ANALYSIS

MPE ANALYSIS

WHAT PROBLEMS CAN BE ANALYZED FROM A DPAN LISTING?

1. Most Halts with no message on the console can be traced to CST no. 11. Of these, the majority are Bounds Violations (parm = %2000), followed by Non-Responding Module (parm = %4000).

   The parameters are on the current stack at Q+1.

   Bounds Violations can be caused by the following:

   a. Bad or intermittent CPU PCA.

   b. CPU PCA not seated all the way forward in card cage.

   c. Noisy Selector Channel power.

   d. CPU backplane induced.

   Non-Responding Module violations can be caused by the following:

   a. Bad or intermittent Memory Data & Control PCA.

   b. Bad or intermittent MCU PCA.

   c. CPU backplane induced. (Installing maintenance panels can cause the problem to go away).

2. System Failure no. 021 << Critical Mode Abort >> is generally system disc related. For example, a process I/O request requires that system code be read (from disc) into memory. If an error prevents this from happening, then a System Failure no. 021 will result.

4. System Failure no. 053 << Attempted to write in protected area of system disc >>

5. System Failure no. 070 << Ran out of IOQ, IOCB, or TBUFF entries >>.

6. System Failure no. 130 << Memory Address Parity Error >>

7. System Failure no. 131 << System Parity Error >>

8. System Failure no. 132 << Memory Data Parity Error >>

NOTE

> This failure may also print the absolute failing address on the console. If no address is printed, then a similar compare dumps to determine if same P-reg or S-reg.

SIMPLIFIED TROUBLESHOOTING OF SYSTEM FAILURE NO. 052 AND 021

1. Take a SYSTEMDUMP of the first two occurrences of a System Failure no. 052. Only one dump is needed for System Failure no. 021. Two dumps give a better picture of the failure (i.e., same track, head, memory address).

2. The console will printout three octal words.

   1st word = Logical Device Number of failing disc.

   2nd word = Failing TIO status word. | MAY BE
   |--
   3rd word = Last TIO status word | INVALID

3. Examine the xxx IOQ TABLE xxx (FREE ENTRIES) in the DUMP listing. The IOQ request for the failing disc is generally the top entry.

LDEV (Bits 8:8) = 1st word printed on console.

FUNC (Bits 14:2) = 0 means READ operation. | DRIVER
= 1 means WRITE operation. |-- REQUEST
| CODES

IOCB (Bits 0:16) = ABS, ADDR, or WORD INDEX in the xxx IOCB TABLE xxx.

BUFF (Bits 0:16) = ADDR of DATA BUFFER.

PAR1, PAR2 = Logical Sector Address

MISC (Bits 0:16) = EXTRA Storage word for MH DRIVERS.

QMEM (Bits 0:16) = EXTRA Storge word for FH DRIVER.

4. Examine the xxx IOCB TABLE xxx (ASSIGNED ENTRIES) in the DUMP listing. The IOCB entry for the failing disc is referenced by IOCB word in the IOQ table (top entry). Each two word entry contains the DRIVER RETURN CODES.

STATUS WORD

%15 - Transfer Error.
%45 - SIO failure.
%55 - Unit failure.
%65 - Invalid memory address (i.e., the address does not reside within the linked memory boundaries).
%75 - Invalid disc address.

XLOG WORD

Positive (Bit 0 = 0) - Number of words transferred.
Negative (Bit 0 = 1) - Number of bytes transferred.

5. MPE performs more READ operations than WRITE operations. Also, the hardware has more checks for READ operations. Therefore, the majority of problems detected will occur for READ operations.

Most probable causes for a bad READ operation are:

a. Bad spot on disc platter. |
|-- See appropriate DIT (CEDA)
b. Bad head. |

c. Any drive fault. | See appropriate IOQ (QMEM)
|-- For 7905/7920, see STATUS 2
d. Faulty controller logic. | word in DIT

e. Bad power, ground, environment.

Most probable causes for a bad WRITE operation are:

```
a.  Any drive fault.          |     See appropriate IOQ
                              |--   (QMEM).  For 7905/7920,
b.  Faulty controller logic.  |     see STATUS 2 word in DIT

c.  Memory data parity error.       See IOQ (BUFF) for memory
                                    address
```

6. The following examples convert a logical sector address into a physical disc address.

The HP 2660 has 32 arcs per head.

```
               (HEAD)
          -------------------
     32 | log. sect. addr.

               (ARC)
```

The HP 2888 has 23 sectors per head and
460 sectors per cylinder.

```
               (CYL)                      (HEAD)
          -------------------          -----------
    460 | log. sect. addr.        23 | Remainder
                                            .
                                           . .
                                            |
        Remainder ----------------------|
                                         (SECT)
```

The HP 7900 has 24 sectors per head and
96 sectors per cylinder

```
               (CYL)                     (HEAD)
          ------------------           -----------
     96 | log. sect. addr.        24 | Remainder
                                              .
                                             . .
                                              |
             Remainder----------------------|
                                           (SECT)
```

The HP 7905 has 48 sectors per head and
144 sectors per cylinder.

```
               (CYL)                     (HEAD)
          ------------------           -----------
    144 | log. sect. addr.        48 | Remainder
                                             .
                                            . .
                                             |
             Remainder---------------------|
                                          (SECT)
```

The HP 7920 has 48 sectors per head and
240 sectors per cylinder.

```
               (CYL)                     (HEAD)
          ------------------           -----------
    240 | log. sect. addr.        48 | Remainder
                                             .
                                            . .
                                             |
             Remainder---------------------|
                                          (SECT)
```

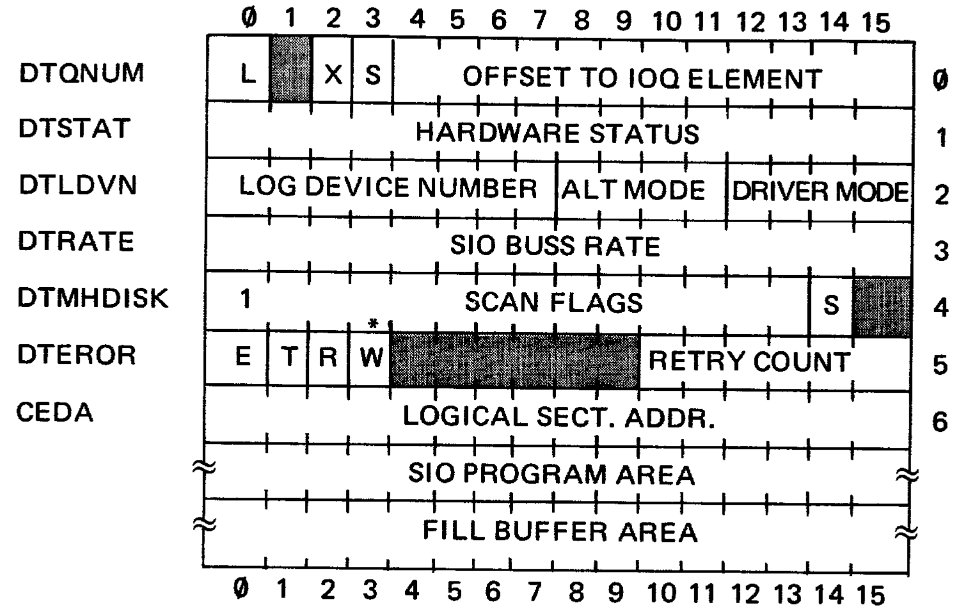
7. The following example converts a physical disc address into a logical sector address.

```
                       HP 7905/7920
                       ------------

                 R1 = 48 (HEAD + SECT)

                 R2 = 240 (CYL)

            R1 + R2 = Logical Sector Address
```



DTSTAT – HARDWARE STATUS
- (0:1) SIO OK
- (1:1) 0
- (2:1) INTERRUPT REQUEST
- (3:1) NOT READY
- (4:1) CRC CHECK ERROR
- (5:1) ABORT (AN ERROR HAS OCCURRED)
- (6:1) TRANSFER ERROR
- (7:1) TRACK ADDRESS TOO BIG
- (8:1) WRITE REJECT
- (9:1) ARC ADDRESS TOO BIG
- (10:6) CURRENT ARC ADDRESS UNDER THE HEADS

DTLDVN
- (0:8) LOGICAL DEVICE NUMBER
- (12:4)– DRIVER MODE
  0 = NO INTERRUPT EXPECTED
  1 = DATA TRANSFER COMPLETION INTERRUPT EXPECTED

DTRATE – SIO BUSS RATE (KILO-WORDS PER SECOND)

DTMHDISK – SCAN FLAGS
- (0:1) – ONE TO INDICATE FIXED HEAD DISC
- (14:1)– SOMETHING FOUND IN IOQ LIST FOR THIS DEVICE WHICH IS READY FOR PROCESSING.

DTEROR – ERROR AND RETRY INFORMATION
- (0:1) – E=1 ERROR HAS OCCURRED
- (1:1) – T=1 READING OR WRITING DEFECTIVE TRACK TABLE
- (2:1) – R=1 READING DEFECTIVE TRACK TABLE
- (3:1) – W=1 WRITING DEFECTIVE TRACK TABLE
- (4:6) – NOT USED
- (10:6)– RETRY COUNT

CEDA
- (0:16)– CURRENT ERROR DISC ADDRESS

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DIT ENTRY FORMAT FOR IOFDISK0

DRIVER INFORMATION
(IOFDISK0)

DRIVER REQUEST CODES   IOQ (6) BITS 14:2

0 - READ
1 - WRITE
2 - CONTROL
3 - FILL

Transfer Error = 120 or more entries in the Defective Track Table.

= Any error while writing the Defective Track Table.

= Track already in the Defective Track Table.

Unit Failure = Greater than 10 retires.

= 10 consecutive CRC errors.

DRIVER RETURN CODES   IOCB (0) BITS 8:8

QUALIFYING (8:5)	GENERAL (13:3)	OVERALL
	1 -TRANSFER OK	1
	33 -CANCEL REQUEST	33
1X - TRANSFER ERROR	X5 -[IRRECOVERABLE	15
4X - SIO FAILURE	X5 ---------------	45
5X - UNIT FAILURE	X5 ---------------	55
7X - INVALID DISC ADDRESS.	X5 --------ERRORS]	75

XLOG   IOCB (1) BITS 0:16
POSITIVE (WDS); NEGATIVE (BYTES).

IOQ (PAR1, PAR2) = LOGICAL DISC ADDRESS

IOQ (QMEM) BIT 0:10 = DISC ERROR STATUS << SAME AS TIO >>
BIT 10:6 = RETRY COUNT

0	L T X S IOQ LINK	QHDIT0
1	HARDWARE STATUS	QHDIT1 (TIO)
2	LOGICAL DEVICE # ALT MODE DVR MODE	QHDIT2
3	BUS LOAD FACTOR = 0	QHDIT3
4	0	SCFLAG
5	CURRENT DATA BUFFER ADDRESS	CDBA
6	CURRENT LOGICAL DISC ADDRESS	*CLDA
7		
8	CYL	CPDA (Current Physical Disc Address)
9	HEAD SECTOR	
10	WORD COUNT REMAINING	WCR
11	CURRENT WORD COUNT	CWC
12	S P D STATUS 1 RETURNED	STAT 1 (Request Status)
13	STATUS 2 RETURNED	STAT 2 (Request Status)
14	CYL	CEDA (Current Error Disc Address)
15	HEAD SECTOR	
16	STATUS (S1)	REQUEST SYNDROME
17	CYL	
18	HEAD SECTOR	
19	DISPLACEMENT	
20	PATT1	
21	PATT2	
22	PATT3	
0	SIO PROGRAM AREA	
63		
0	FILL BUFFER AREA (0 IF BINARY; BLANK IF ASCII)	
127		

QMISC WORD IN IOQ TABLE (IOMDISK1 ONLY)

*	N	S	E	M	W	U	R	C	D	RETRY COUNT

Used For Multiple Interface Operations Only

N – Not a new request
S – Request syndrome
E – Error status read
M – Reading bad track, may update track table
W – Write bad track into track table (cyl 0; trk 0; sec 1)

U – Clear unit allocation
R – Retry same transfer
C – Recalibrate complete
D – Retry determination

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7905/7920 DIT ENTRY FOR IOMDISK1

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
QHDIT0	L	T	X	S	OFFSET TO IOQ ELEMENT											
QHDIT1 1	HARDWARE CONTROLLER STATUS															
QHDIT2 2	LOGICAL DEVICE NO.								ALT. MODE				DRIVER MODE			
QHDIT3 3	BUS LOAD FACTOR															
SCFLAG 4	M	SCAN FLAG													S	D
CURCYL 5	CURRENT CYLINDER															
WCR 6	WORD COUNT REMAINING															
BUFF 7	CURRENT DATA BUFFER ADDRESS															
DADR 8	CURRENT DISC ADDRESS – HIGH ORDER															
DADR 9	CURRENT DISC ADDRESS – LOW ORDER															
DADRT 10	ALT. TRACK DISC ADDRESS – HIGH ORDER															
DADRT 11	ALT. TRACK DISC ADDRESS – LOW ORDER															
NCWC 12	NEGATIVE CURRENT WORD COUNT															
DRATE 13	SIO BUS DATA RATE															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

QHDIT1 — HARDWARE STATUS

		ISS	HP 7900
DRIVE STATUS	· (0:1) –	SIO OK	SAME
	· (1:1) –	200 TRKS/INCH	SAME
	· (2:1) –	INTERRUPT REQUEST	SAME
	· (3:1) –	DRIVE ON LINE	SAME
	· (4:1) –	DRIVE UNSAFE	SAME
	· (5:1) –	SEEK INCOMPLETE	DRIVE NOT READY
	· (6:1) –	DRIVE BUSY	ACCESS NOT READY
	· (7:1) –	PACK CHANGE	UNUSED
	· (8:5) –	CONTROLLER STATUS (ENCODED)	
		0 = NO ERROR	SAME
		1 = ILLEGAL OPCODE	SAME
		3 = CYLINDER #TOO BIG	UNUSED
		4 = SECTOR #TOO BIG	SAME
		5 = TIME OUT	UNUSED
		6 = DEFECTIVE TRACK	SAME
		7 = HEADS MISPOSITIONED	SAME
		10 = CYCLIC ERROR (ADDR)	UNUSED
		11 = CYCLIC ERROR (DATA)	CYCLIC ERROR
		12 = I/O PROGRAM ERROR	SAME
		13 = SEQUENCE ERROR	UNUSED
		14 = CYLINDER OVERRUN	SAME
		15 = ZERO SECTOR COUNT	SAME

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DIT ENTRY FORMAT FOR IOMDISK0, sheet 1 of 2

			16 = DATA OVERRUN	SAME
			20 = ILLEGAL TERMINATION	UNUSED
			22 = UNUSED	HD/SECTOR COMPARE ERROR
			23 = DRIVE ERROR	ACCESS NOT READY
			24 = TRANSFER ERROR	SAME
			26 = UNUSED	DATA PROTECTED
			37 = DRIVE ATTENTION	SAME
	· (13:3)	–	UNIT NUMBER	SAME

QHDIT2 · (12:4) – MONITOR MODE WHEN I/O PROGRAM STARTED
    2 – INITIATING
    %13 – COMPLETING

SCFLAG · – SCAN FLAGS
· (0:1) – MOVING HEAD DISC
· (14:1) – SOMETHING FOUND. A REQUEST IN THE IOQ LIST FOR THIS DEVICE IS READY TO BE INITIATED
· (15:1) – SCAN DOWN FLAG. DO ALL REQUESTS WHOSE CYLINDER NUMBER IS EQUAL TO OR LESS THAN CURRENT CYLINDER FIRST.

CURCYL – CURRENT CYLINDER WHERE HEAD IS
WCR – WORD COUNT REMAINING
BUFF – CURRENT BUFFER ADDRESS
DADR – CURRENT SECTOR ADDRESS (2 WORDS)
DADRT – ALTERNATE TRACK SECTOR ADDR (2 WORDS)
NCWC – NEGATIVE WORD COUNT FOR CURRENT I/O PROGRAM
DRATE – SIO BUSS DATA RATE FOR CURRENT I/O PROGRAM

QMISC WORD IN IOQ TABLE (IOMDISK0 ONLY)

N	X	A	M	W	R	S	T	E	RETRY COUNT

N – NOT A NEW REQUEST
X – XFERING FROM ALT. TRK.
A – READING ALT. TRK. NUMB.
M – RD/WRT BAD TRK. MAP
W – WRITING BAD TRK. MAP
R – RECALIBRATE TRIED
S – SEEK OR RECALIBRATE
T – TRK. BY TRK. XFER
E – ERROR HAS OCCURRED

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DIT ENTRY FORMAT FOR IOMDISK0, sheet 2 of 2

The following MPE Supported Utilities are discussed in this section of the manual.

```
*SAVIOR.PUB.SYS
*SAEDIT.PUB.SYS
 RECOVER.PUB.SYS
 DPAN.PUB.SYS
 LISTLOG.PUB.SYS
 LISTEQ.PUB.SYS
```

*Implies these programs run Stand-Alone while others run On-Line under MPE.

To obtain a LOADMAP while MPE is On-line, do the following:

```
 FILE P;DEV=LP
 RUN FCOPY.PUB.SYS
     .
     .
     .
>FROM=LOADMAP.PUB.SYS;TO=*P
>EXIT
     .
     .
     .
```

LOAD MAP will now be printed on the line printer.

SAVIOUR/SAEDIT/RECOVER

The set of three programs: SAVIOUR (File Recovery), SAEDIT (Disc Edit) and RECOVER (File Creation) makes possible the recovery of files from an HP 3000 system that has become logically inoperable due to some catastrophic conditon such as Cold Load information or System Directory corruption. Such conditons currently reduce the options to bring the system up to only one: RELOAD. It is at this time that the stand-alone cold loadable programs SAVIOUR and SAEDIT can be employed to retrieve files from the disc and copy them to magnetic tape for later recovery.

The File Retrieval program runs stand-alone (independent of MPE) in spite of existing inconsistencies such as invalid volume label or invalid cold load information. Files can be selected for retrieval by the following three options.

1. <file name>.<group name>.<account name>

   In this mode, the specified file will be located, if possible, using the System Directory.

2. <logical device number of disc>, <sector address of file label>

   In this mode, the file is located directly by using the <ldev>, <sector address> obtained after a file has STOREd or RESTOREd if the SHOW option had been specified. When a file is located in this way, the <filename group account> from the file label is displayed for verification before the file is allowed to be retrieved.

   The locating of files by this method would normally be resorted to because of the invalidity in some way of the System Directory.

3. @.@.@

   In this mode, all files described in the System Directory are retrieved using the Directory in locating the files.

A restriction of only retrieving those files accessed since some specified date can be imposed when retrieving files using modes (1) and (3).

The format of each magnetic tape created is that of one or more files, where each file is separated by an EOF mark and the last file by an additional EOF mark. A file consists of 128 word blocks, where the first block is the file label followed by user labels, if any, and data. An individual file on tape will not be allowed to span multiple tape reels. When end of tape is sensed, the tape will be backspaced to the previous EOF mark and the second EOF mark written, a prompt to mount a new output reel will be made and the copying of the file, in its entirety, will continue.

Certain assumptions are made by the File Retrieval program when it is executed:

1. Sector 18 word 14, the Directory Base Address and word 13 the Directory Size, must be valid in order to locate the Directory and to perform range checking on addresses referencing the Directory. If a disc error is detected when reading sector 18, then the following dialogue will be entered in an attempt to continue.

   ```
   CAN´T READ SECTOR 18 OF SYSTEM DISC

   THIS CONTAINS DIRECTORY BASE SECTOR AND LIMIT SECTOR

   MAY INPUT VALUES FOR DIRECTORY BASE AND LIMIT OR HIT CR TO
   STOP

   STARTING SECTOR OF DIRECTORY? <sector address>

   NO. OF SECTORS IN DIRECTORY? <Directory size>
   ```

2. The Defective Tracks Table, sector 1 of the System Disc, must be valid in order to locate alternate tracks assigned to data residing on discs other than fixed-head discs (tracks are never reassigned on the fixed-head disc).

Failures due to bad tracks when accessing the Directory will be indicated by the following messages as to the reason a file could not be retrieved. The following messages that refer to "ABOVE ERROR" or "ABOVE ERRORS" will be referring to the general disc error message:

```
             | READ   |
     DISC   -| WRITE  |-  ERR ON LDEV#<lDEV>
             | SEEK   |

                          STATUS = %<controller status>

                          ADDR = %<sector>

                          WORD = <word count>
```

The specific messages are:

```
SYS/ACT PREFIX CAN´T BE READ
RUN STAND-ALONE DISKEDIT TO INVESTIGATE
ABOVE ERROR DUE TO BAD TRACK - SYS/ACT INDEX
```

NOTE

> The program cannot continue and will halt because of the above conditions.

```
ABOVE ERRORS DUE TO BAD TRACK - ACCOUNT ENTRY

ACT/GROUP PREFIX CAN´T BE READ
FOR - <account name>

ABOVE ERROR DUE TO BAD TRACK - ACT/GRP INDEX

ABOVE ERRORS DUE TO BAD TRACK - GROUP ENTRY

GROUP/FILE PREFIX CAN´T BE READ
FOR - <group name>
```

```
ABOVE ERROR DUE TO BAD TRACK - GRP/FILE INDEX

ABOVE ERRORS DUE TO BAD TRACK - FILE ENTRY

BAD TRACK - CAN'T READ LABEL
```

Errors caused by bad addresses in the contents of the Directory or invalid values in sector 18 of the System Disc could be indicated by these messges.

```
ERROR - TRYING TO READ SECTOR OUTSIDE DIRECTORY
```

A bad file entry or file label could be indicated by:

```
LABEL COMPARE FAILED
REQUESTED SECTOR NOT ON DISK
LDEV #<ldev> SECTOR #%<sector address>
```

Errors due to invalid definition of the disc configuration can cause the following error messges to be emitted:

```
ERROR - DESCRIPTION FOR DRT 5 WASN'T ENTERED
LDEV#<ldev>NO SUCH TYPE - SUBTYPE
```

Failures in magnetic tape operations will cause the program to go into a hard halt after indicating one of the following detail messages:

```
UNIT WENT OFF LINE
NOT READY INTERRUPT
TRANSFER ERROR
CMD REJECT
TAPE RUN AWAY
TIMING ERROR
TAPE PARITY ERROR
```

followed by one of these operation messages:

```
CAN'T WRITE TO TAPE
CAN'T BACKSPACE
CAN'T WRITE EOF
```

OPERATING PROCEDURES (Stand-Alone File Recovery)

The operator must have a current list of the I/O configuration in order to correctly describe the discs from which files are to be retrieved. The Volume # of a disc is the relative position that a volume definition occuies in the Volume Table. Volume Table entries can be displayed, by their physical ordering, by listing the Volume Table via the INITIAL dialogue.

1. Mount the Cold Load tape containing the two stand-alone programs for File Retrieval and Disc Edit on a tape drive whose DRT is 6 with the unit set to 0.

2. Set the B-register to %003006.

3. Push CPU Reset, I/O Reset, and Cold Load switches on the software panel in that order.

4. Push the RUN switch.

5. Set the B-register to %000001.

   (This indicates that the first program on the Cold Load tape is to be loaded. The instructions for creating the Cold Load tape will show that the File Retrieval program is created first.)

6. Push the RUN switch.

7. Set the B-register to %004000.

   (This indicates the starting absolute core location that the program is to be loaded.)

8. Push the RUN switch.

   (The program is now loaded into core from tape and then begins execution.)

9. The following lines are printed on the console.

```
*****STAND-ALONE FILE RECOVERY (CU.05)*****
ALL NUMERIC INPUT IS DECIMAL - MAY USE OCTAL IF
   PRECEDED WITH %
DISC CONFIGURATION SECTION
```

   The operator is now prompted with the following dialogue in order to describe the discs on the system. This is repeated until a CR is hit for LDEV#?

```
LDEV#?
DRT#?
UNIT?
TYPE?
SUBTYPE?
```

10. The operator is now prompted as to where to list the names of those files that have been successfully retrieved. Either a line printer or the system console can be chosen.

```
DRT # of LP? (A CR MEANS USE CONSOLE)
```

    The following message will be output before proceeding to step 11:

```
MOUNT TAPE WITH WRITE RING ON MAG.
TAPE UNIT 0 OF DRT 6.
```

FILE SPECIFICATION SECTION

11. FILE NAME? (OR LDEV#, %SECTOR ADDRESS)

    a. Enter particular File Name or,

    b. Logical Device Number, %Sector Address or where you believe a particular file resides or,

    c. "@" to indicate all files on the system are to be retrieved.

    If log.device #, %Sector was input, then proceed to step 16 or else proceed as follows:

```
12. GROUP?    |
              |-  Must use @ in both cases if @ was used
              |   in response to FILE NAME?
13. ACCOUNT?  |
```

14. DATE? May input a date in form of MM/DD/YY to restrict recovery of files having been accessed from the date entered to the current date.

    (CR means ignore the date test.)

15. The File Name retrieved will be printed on the line printer or console along with the logical device number and sector address of the label. Control will return to step 11 if F.G.A. was entered. If @,@,@, was entered, then a listing of all files retrieved will be printed as each file is stored to tape or the F.G.A. and error message as to why it could not be retrieved will be printed. If @,@,@, was entered, then upon completion, the program prints FINISHED on the console and produces a HALT 0.

16. Since a Ldev#, Sector Address was entered, the following promp occurs after the label at the specified address has been read:

    ```
    FILE GROUP ACCOUNT - CONTENTS OF LABEL
    DO YOU WISH TO RETRIEVE THIS FILE (Y/N)?
    ```

    The File Name, Group, and Account found at the specified address is printed as a check and then you may choose to retrieve the file or not.

17. Control returns to step 11.

ERROR CONDITIONS

Upon serious error conditions, such as:

```
SECTORS OUTSIDE OF DIRECTORY
NO ACCOUNT ENTRIES
BAD TRACK
LABEL COMPARE FAILED
```

You may investigate the Directory and file labels using the STAND-ALONE DISK-EDIT program.

To load this program, perform steps 1-4, in step 5, set the register to %000002 and do steps 6-10.

To get the STAND-ALONE DISK-EDIT instructions, type in HELP or see the instruction description later in this article.

SAEDIT is the stand-alone disc edit and is cold loaded by using the same instructions used to cold load the File Recovery program with the exception of step 5, where instead of setting the B-register to %000001, the B-register is set to %000002.

INSTRUCTIONS FOR STAND-ALONE DISK-EDIT

NOTE

> All input is decimal unless preceded by a "%". Dump output may be terminated by setting Bit 0 to a "1" in the B-register as the dump is being produced. When the dump is terminated, reset Bit 0 to "0".

Commands:

<BASE X
where X = the base sector address

<DISC X
where X = the logical device number of the DISC to be selected

<DUMP X,Y
where X = relative sector starting address
      Y = number of sectors to dump

<FORMAT
allows changing the dump format (octal, character, or both)

<HELP
prints the instructions and commands for using
STAND-ALONE DISK-EDIT

<LIST X
where X = DRT of the line printer (X = 0 means console)

<MODIFY X,Y,Z
where X = relative sector address
      Y = starting word within the sector
      Z = number of words to modify

(When in the MODIFY mode, two special characters may be input:

'*' - do not change the present value

'/' - terminate the MODIFY operation that is, no words are modified)

<RESTART

restarts the program to allow re-entering the disc descriptions

The program RECOVER is a privileged mode program that runs under MPE. This program is used to recreate files back on the the HP 3000 system from the tapes produced by the Stand-Alone File Recovery program. After all the necessary files have been retrieved by the Stand-Alone File Recovery program, the required RELOAD is performed to regenerate the operating system. The account structure must be recreated as well. Next, the RECOVER program should be executed from MANAGER.SYS to restore the files from the recovery tapes. This should be done before restoring all files since the RECOVER program does not delete an existing file and so a file with the same name on the recovery tape will not be restored. Upon completion of the RECOVER program, a complete RESTORE with a KEEP may be performed to return all remaining files to the most up-to-date level.

The building of the Cold Load tapes containing the Stand-Alone File Recovery and Stand-Alone Disk Edit programs is accomplished by the use of the DIAGNOSTIC UTILITY PROGRAM (HP32217A.04.0) named SDUP.PUB.SYS.

An example creation of this Cold Load tape is listed below:

```
=SESSION

:HELLO MANAGER.SYS
 SESSION NUMBER = #S3
 MON, MAY 5, 1975, 7:30 PM
 HP32000C.F0.69

 ST/19:30/#S3/LOGON FOR:MANAGER.SYS ON LDEV#3
:RUN SDUP; NO PRIV

 3000A DIAGNOSTIC UTILITY PROGRAM (HP 32217A.04.0)

 ENTER 1 FOR CREATE CPU TAPE
 ENTER 2 FOR BUILD STANDALONE TAPE
 ENTER / TO TERMINATE

 PROGRAM NAME?
 SAVIOUR
 PROGRAM NAME?
 SAEDIT
 PROGRAM NAME?
 /
 ?IO/19:31/#S3/32/LDEV# FOR "DT1" ON TAPE (NUM)
 =REPLY 32.8
 ENTER DRT NUMBER FOR CONSOLE DEVICE
 3
 ENTER DRT NUMBER FOR LINE PRINTER
 0
 PROGRAM SAVIOUR  ANY CHANGES?

 PROGRAM SAEDIT   ANY CHANGES?

        1 SAVIOUR  A
        2 SAEDIT   A
 ENTER 1 FOR CREATE CPU TAPE
 ENTER 2 FOR BUILD STANDALONE TAPE
 ENTER / TO TERMINATE

 END OF PROGRAM
```

DPAN (CU.05)

The program DPAN produces a simple analysis and a listing of the content of memory as recorded on tape through the core dump procedure. There are cases when the best way to diagnose a software or hardware problem is to take a dump (picture) of the content of core at the time of the crash and to analyze the data so obtained.

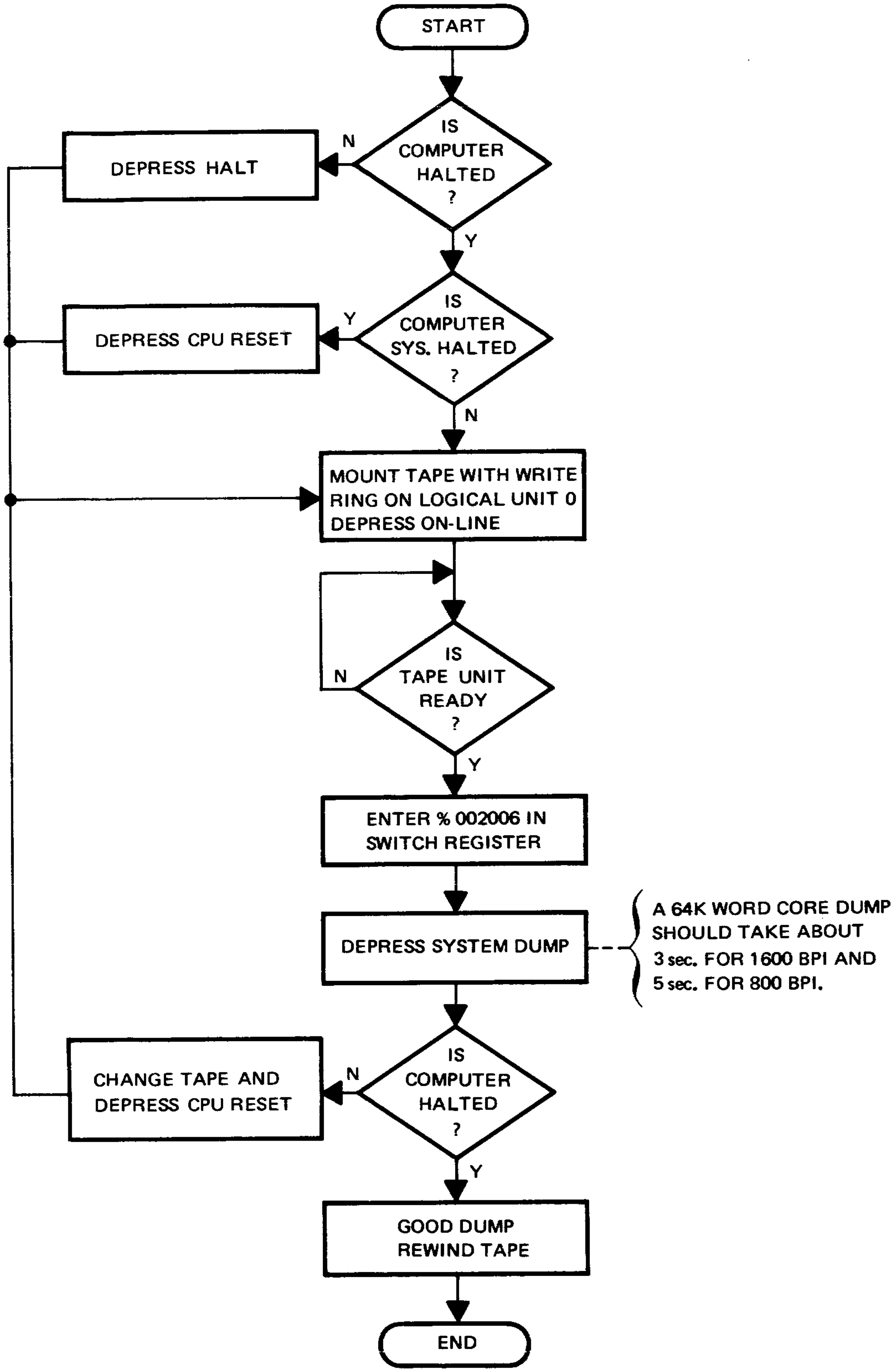
The first step of dumping core to a mag tape is performed by a special microcoded function of the system and is initiated by pressing the "SYSTEM DUMP" button (which could as well be labeled "CORE DUMP" in order to avoid confusion with the SYSDUMP command whose purpose is to back the system up). Once the picture of the memory is on the tape, the program DPAN can produce a formatted listing of it which may be analyzed to determine the cause of the problem.

It is highly recommended that those operations be performed each time the system goes down for an unknown reason.

Once it has been determined that a CORE DUMP should be taken, use the following flowchart for instructions.

Some common causes for unsuccessful SYSTEM DUMP execution on first try are:

- Mag tape drive not ON LINE and ready.
- Mag tape Unit 0 not selected.
- Mag tape does not contain a write ring.
- CPU RESET not pressed when SYSTEM HALT light was on.
- Wrong octal code in switch register.
- Bad magnetic tape itself which causes "Read after Write error".
- IO RESET not pressed after tape was mounted.



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CORE DUMP FLOWCHART

SYSTEM DUMP (LOW CORE OVERLAY)

```
%7      SW. REG.   )
        DL         |
        DB         |
        X          |
        Q          |
        S          |
        Z          |     LOST IF
        STATUS     |  FIRST ATTEMPT
        PB          >    TO DUMP
%20     P          |  MEMORY FAILS
        PL         |   (OVERLAYED)
        CIR        |
        MASK       |
        CPX1       |
        CPX2       |
%26     MEM SIZE   )
```

EXECUTION OF DPAN

The program DPAN can then be run as any ordinary HP 3000 program. Input data to the program is the core dump tape generated as previously described and the output is a formatted printout.

The input file (core dump tape) formal designator is "DPANMAST" and defaults to the class "TAPE" and therefore will require operator intervention to select proper drive. The output file (printout) formal designator is "DPANLIST" and defaults to "LP" class if the program is run from a session, to "$STDLIST" if run from batch job. File equations are necesary to modify those files.

Once in memory and executing. DPAN:

a. Outputs HP 3000 MEMORY DUMP ANALYZER message on the Job List Device, followed by its own version numbers and date.

b. Opens all files it will need during execution. At this time, MPE will request operator intervention on DPAN´s behalf for opening DPANMAST file. Enter appropriate response on system console.

c. Reads the SYSTEM DUMP tape and creates a "core-image" file it will use for accessing memory in lieu of the SYSTEM DUMP tape.

Once the SYSTEM DUMP tape has been read and rewound, it may be unloaded and removed from the MT drive.

```
:RUN DPAN <<NORMAL DUMPS>>
:RUN DPAN;PARM=[%SYSDB] <<ALL DUMPS THAT HAD TO BE RETRIED>>
```

DPAN OUTPUT

Assuming the dump is correct, DPAN will analyze and list the following information:

a. ID page
b. Register pages
c. Low fixed core
d. System global area
e. DRT
f. CST
g. DST
h. PCB
i. Scheduling queue
j. Linked memory
k. Octal main memory dump

NOTE

> The diagnostic of a crashed system through an analysis of the DPAN printout is a delicate operation and should be left to field and factory specialists.

LISTLOG (CU.05)

PURPOSE

The object of the LISTLOG program is to output, in a readable form, the content of a Log file generated by MPE when the system is running. The output is directed to any device and the type of records listed can be selected.

For more information about the Log file, refer to the HP 3000 Manager/Supervisor Manual, part no. 32000-90006 - section IX.

RUNNING LISTLOG

Before running the program, two file equations have to be entered to determine the input file (Log file) and the output file (List file). Formal designators for those files are "LOGFILE" and "LOGLIST", respectively.

The creator of the Log file is "MANAGER.SYS".

The parameter of the RUN command can be used to selectively specify the record types to be output when PARM is 0, all records will be listed; to suppress the listing of a given record type, say X, set a 1 in bit position (15-x) of the PARM word.

RECORD TYPE	X
Logging Error	0
System Up	1
Job Initiation	2
Job Termination	3
Process Termination	4
File Close	5
System Shutdown	6
Spool Input/Output	7

Examples:

To list all log records of LOG0034 on line printer:

```
:FILE LOGFILE = LOG0034
:FILE LOGLIST, DEV = LP
:RUN LISTLOG
```

To list Job Initiation and Job Termination records on tape:

```
:FILE LOGFILE = LOG0034
:FILE LOGLIST; DEV = TAPE
:RUN LISTLOG; PARM = %163
```

To list the Log File Error records (if any) to a Terminal (LDEV=21):

```
:FILE LOGFILE = LOG0034
:FILE LOGLIST; DEV = 21
:RUN LISTLOG; PARM = %176
```

ERROR

The program quits (by call to intrinsic QUIT) with the following conditions:

QUIT #1 Log file cannot be opened
QUIT #2 Output file cannot be opened
QUIT #3 Head failure on Log file
QUIT #4 Unknown record type (>8)

LISTEQ UTILITY (CU.05)

LISTEQ is used to print file equations and temporary files created during a job/session. The utility does this by accessing the JOB DIRECTORY TABLES (JDT) and listing all current file equations and job/session temporary files.

To use the LISTEQ Utility, issue:

```
:RUN LISTEQ.PUB.SYS
```

Example:

```
:FILE TAPE;DEV.=TAPE
:FILE PRINT;DEV=LP
:BUILD INPUT;REC=40,3,F,ASCII;TEMP
:RUN LISTEQ

LISTEQ     (CU.05)

***TEMP FILES

INPUT.PUB.SYS

***FILE EQUATIONS

:FILE TAPE;DEV=TAPE
:FILE PRINT;DEV=LP

END OF PROGRAM
```

NOTE

When no TEMP files or File Equation, such an indication is given as output of the program.

MISCELLANEOUS

PREVENTIVE MAINTENANCE
(EVERY 2 MONTHS)

On the Power Control Module (PCM) check the AC voltages from each phase-to-neutral on the RFI filters of the Power Control Module (PCM). The voltages must be within +, -5% of each other.

Check the AC voltage from neutral-to-ground on the RFI filter. The voltage must be less than 1 volt.

Check all fan motors in the following equipment:

1. All power supplies
2. All card cages

NOTE

> Only Series I card cage fans are removable from the front without completely removing the card cage from the cabinet.

Check all filters and vacuum the inside of all cabinets.

Check and adjust if necessary all DC power supply voltages (See "Power Section" for DC Supply Voltages and Currents.)

Check and replace all lamps and LED´s on power supplies and in the CPU cabinet (mini-panel, etc.).

All PCA´s should be removed for cleaning and inspection at six month intervals.

Run memory microcode, all CPU and stand alone diagnostics

Verify the ability to dump memory (SYSTEMDUMP) to mag tape.

Run on-line diagnostics and the WORKOUT program.

MEMORY SCHMOO

GENERAL DESCRIPTION

Schmooing consists of adjusting the +20 volt memory voltage of the HP 30310A power supply to the mid-point of its non-error range. Should be done anytime a memory PCA is replaced.

ADJUSTING PROCEDURE

Load memory checkerboard micro-diagnostic and adjust the +20 volt pot slowly clockwise until the diagnostic fails.

Measure +20V bus and record this upper limit.

Adjust +20 volt pot counterclockwise one full turn.

Restart micro-diagnostic and adjust +20 volt pot counterclockwise until the diagnostic fails again.

Measure +20 volt bus and record this lower limit.

$$\underline{\text{Upper limit -Lower limit}}$$

$$\text{Non-Error Range/2 + Lower limit = mid-point range.}$$

Divide the non-error range in half and add to the lower limit range.

Adjust the +20 volt pot to the mid-point you just calculated.

HP 3000 PRE-SERIES II SERVICE MANUAL INDEX

(not yet available)

GENERAL HARDWARE

GENERAL HARDWARE

SECTION

VIII

This section presents Summary Descriptions of all the subsystems starting with the CPU (30001A) and continuing through the Maintenance Panels (30354D). Each Summary Description is part of this section and tells of differences from Series II, general information, cabling and/or configuration, diagnostics, and halt codes.

Here is a list of the Summary Descriptions in their order of appearance in this section. Headings at the top of each page, and page numbers at the bottom of each page tell you which text you are reading. The page number prefixes and this list can help you find other texts in this section.

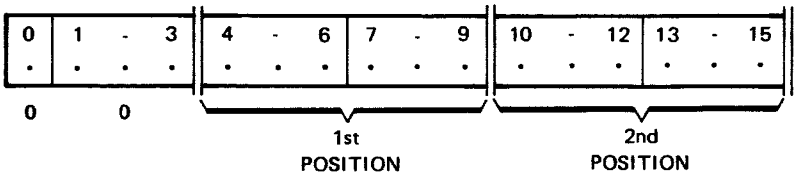
CENTRAL PROCESSOR UNIT

HP 30001A
CENTRAL PROCESSOR UNIT

HARDWARE DIFFERENCES

PRE-SERIES II	SERIES II
Hardware	**Hardware**
128KB Core Memory with parity	128KB to 512KB Fault Control Semiconductor Memory
Memory Interleaving	
32 Bit Floating Point (Stndrd)	48 Bit Floating Point (Stndrd)
48 Bit Floating Point (optnl)	64 Bit Floating Point (optnl)
192 Firmware Instructions	209 Firmware Instructions
880KB per Multiplexor Channel	990KB per Multiplexor Channel
1.9MB/Second Selector Channel & Central Data Bus	2.86MB/Second Selector Channel & Central Data Bus
30119A Card Reader/Punch -Read @ 175 CPM -Punch/Print @ 27 to 40 CPM	30119A Card Reader Punch -Read @ 200 CPM -Punch/Print @ 45 to 75 CPM

00 STACK OPS



00	NOP	20	ADD	40	DEL	60	LADD
01	DELB	21	SUB	41	ZROB	61	LSUB
02	DDEL	22	MPY	42	LDXB	62	LMPY
03	ZROX	23	DIV	43	STAX	63	LDIV
04	INCX	24	NEG	44	LDXA	64	NOT
05	DECX	25	TEST	45	DUP	65	OR
06	ZERO	26	STBX	46	DDUP	66	XOR
07	DZRO	27	DTST	47	FLT	67	AND
10	DCMP	30	DFLT	50	FCMP	70	FIXR
11	DADD	31	BTST	51	FADD	71	FIXT
12	DSUB	32	XCH	52	FSUB	72	SPARE
13	MPYL	33	INCA	53	FMPY	73	INCB
14	DIVL	34	DECA	54	FDIV	74	DECB
15	DNEG	35	XAX	55	FNEG	75	XBX
16	DXCH	36	ADAX	56	CAB	76	ADBX
17	CMP	37	ADXA	57	LCMP	77	ADXB

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HP 3000 PRE SERIES II INSTRUCTION SET (STANDARD), sheet 1 of 5

01 SHIFTS/BRANCHES

0 •	1 - 3 • • •	4 - 6 • • •	7 - 9 • • •	10 - 12 | 13 - 15 • • • | • • •	
0	1	X 0 0	0	← Shift Count →	ASL
		X 0 0	1	← SC →	ASR
		X 0 0	2	← SC →	LSL
		X 0 0	3	← SC →	LSR
		X 0 0	4	← SC →	CSL
		X 0 0	5	← SC →	CSR
		X 0 0	6	0 0	SCAN
		X 0 0	7	+/- ← P (0-31) →	IABZ
		X 0 1	0	← SC →	TASL
		X 0 1	1	← SC →	TASR
		I 0 1	2	+/- ← P (0-31) →	IXBZ
		I 0 1	3	+/- ← P (0-31) →	DXBZ
		I 0 1	4	+/- ← P (0-31) →	BCY
		I 0 1	5	+/- ← P (0-31) →	BNCY
		X 0 1	6	← SC →	TNSL
		1	7	0 0	SPARE
		X 1 0	0	← SC →	DASL
		X 1 0	1	← SC →	DASR
		X 1 0	2	← SC →	DLSL
		X 1 0	3	← SC →	DLSR
0	1	X 1 0	4	← SC →	DCSL
		X 1 0	5	← SC →	DCSR
		I 1 0	6	+/- ← P (0-31) →	CPRB
		I 1 0	7	+/- ← P (0-31) →	DABZ
		I 1 1	0	+/- ← P (0-31) →	BOV
		I 1 1	1	+/- ← P (0-31) →	BNOV
		X 1 1	2	bit position	TBC
		X 1 1	3	bit position	TRBC
		X 1 1	4	bit position	TSBC
		X 1 1	5	bit position	TCBC
		I 1 1	6	+/- ← P (0-31) →	BRO
		I 1 1	7	+/- ← P (0-31) →	BRE

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HP 3000 PRE SERIES II INSTRUCTION SET (STANDARD), sheet 2 of 5

02 MOVES/IMMEDIATES

0	1 - 3	4 - 6	7 - 9	10 - 12	13 - 15	
0	2	0	0	0 PB/DB 0	. SDEC	MOVE
		0	0	1 PB/DB 0	. SDEC	MVB
		0	1	0	. SDEC	MVBL*
		0	1	2	. SDEC	SCW
		0	1	4	. SDEC	MVLB*
		0	1	6	. SDEC	SCU
		0	2	0 N A	U SDEC	MVBW
		0	2	1 PB/DB 0	. SDEC	CMPB
		0	3	0	0	RSW
		0	3	0	1	LLSH*
		0	3	2	0	PLDA*
		0	3	2	1	PSTA*
		0	4	4	0	SPARE
		1	0 ←	Imm Opr	→	LDI
		1	1 ←	Imm Opr	→	LDXI
		2	0 ←	Imm Opr	→	CMPI
		2	1 ←	Imm Opr	→	ADDI
		3	0 ←	Imm Opr	→	SUBI
		3	1 ←	Imm Opr	→	MPYI
		4	0 ←	Imm Opr	→	DIVI
		4	1 0 DB*	DL* Z* STA*	X Q S	PSHR
		5	0 ←	Imm Opr	→	LDNI
		5	1 ←	Imm Opr	→	LDXN
		6	0 ←	Imm Opr	→	CMPN
		6	1 J J	J J K	K K K	EXF
		7	0 J J	J J K	K K K	DPF
		7	1 0 DB	DL Z STA	X Q S	SETR

JJJJ	Beginning bit position (0 - 15)
KKKK	Field length (0 - 15)

* Privileged instructions

1471004-96, 3 of 5

HP 3000 PRE SERIES II INSTRUCTION SET (STANDARD), sheet 3 of 5

03 I/O, LINKAGE, CONTROL

0	1 - 3	4 - 6	7 - 9	10 - 12	13 - 15	
•	• • •	• • •	• • •	• • •	• • •	
0	3	0	0	0	0	SPARE
		0	0	0 1 K	K K K	PAUS *
		0	0	1 0 K	K K K	SED *
		0	0	1 1 K	K K K	XCHD *
		0	1	0 0 K	K K K	SMSK *
		0	1	0 1 K	K K K	RMSK
		0	1	1 0 K	K K K	XEQ
		0	1	1 1 K	K K K	SIO *
		0	2	0 0 K	K K K	RIO *
		0	2	0 1 K	K K K	WIO *
		0	2	1 0 K	K K K	TIO *
		0	2	1 1 K	K K K	CIO *
		0	3	0 0 K	K K K	CMD *
		0	3	0 1 K	K K K	SIRF *
		0	3	1 0 K	K K K	SIN *
		0	3	1 1 K	K K K	HALT *
		0	1	← STT →		SCAL
		1	0	← STT →		PCAL
		1	1	← SDEC +(4) →		EXIT
		2	0	← SDEC +(1) →		SXIT
		2	1	← Imm Opr →		ADXI
		3	0	← Imm Opr →		SBXI
		3	1	← PL-Disp →		LLBL
		4	0	← P + Disp →		LDPP
		4	1	← P - Disp →		LDPN
		5	0	← Imm Opr →		ADDS
		5	1	← Imm Opr →		SUBS
		6	0	← DB + Disp →		TSBM
		6	1	← Imm Opr →		ORI
		7	0	← Imm Opr →		XORI
		7	1	← Imm Opr →		ANDI

KKKK	Stack displacement (0 - 15)
ST	Entry position (0 - 255)

---

* Privileged instructions

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HP 3000 PRE SERIES II INSTRUCTION SET (STANDARD), sheet 4 of 5

MEMORY REFERENCE

0	1 - 3	4 - 6	7 - 9	10 - 12	13 - 15	
0	4	X I 0	← P →			LOAD
		X I 1	← DQS →			
0	5	0	+/- ← P rel branch →			TBA
		2	+/- ← P rel branch →			MTBA
		4	+/- ← P rel branch →			TBX
		6	+/- ← P rel branch →			MTBX
		X I 1	← DQS →			STOR
0	6	X I 0	← P →			CMPM
		X I 1	← DQS →			
0	7	X I 0	← P →			ADDM
		X I 1	← DQS →			
1	0	X I 0	← P →			SUBM
		X I 1	← DQS →			
1	1	X I 0	← P →			MPYM
		X I 1	← DQS →			
1	2	X I 0	← DQS →			INCM
		X I 1	← DQS →			DECM
1	3	X I 0	← P →			LDX
		X I 1	← DQS →			
1	4	X I 0	+/- ← P rel branch →			BR
		X I 1	← DQS indirect →			BR
		I 0 1	GEL	+/- P branch		BCC
1	5	X I 0	← DQS →			LDB
		X I 1	← DQS →			LDD
1	6	X I 0	← DQS →			STB
		X I 1	← DQS →			STD
1	7	X I 0	← P →			LRA
		X I 1	← DQS →			

---

		7 - 9	10 - 12	13 - 15	
P	P+	0 . .	. . .	. . .	0:377
	P–	1 . .	. . .	. . .	
DQS	DB+	0 . .	. . .	. . .	0:377
	Q+	1 0 .	. . .	. . .	0:177
	Q–	1 1 0	. . .	. . .	0:77
	S–	1 1 1	. . .	. . .	0:77

GEL	1	Less than	4	Greater	7	Always
	2	Equal	5	Not equal	0	Never
	3	Less than or equal	6	Greater or equal		

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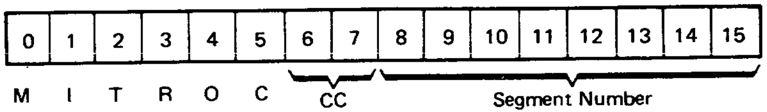
HP 3000 PRE SERIES II INSTRUCTION SET (STANDARD), sheet 5 of 5

STATUS REGISTER



M Mode User/Privileged
I Interrupts Enabled
T Traps Enabled (User Only)
R Right Stack-op Pending
O Overflow
C Carry
CC Condition Code
CCL = 01
CCE = 10
CCG = 00

CCA	CCL	Operand<0
	CCE	Operand = 0
	CCG	Operand>0
CCB	CCL	Special ASCII
	CCE	Alphabetical
	CCG	Numeric
CCC	CCL	Operand1<Operand2
	CCE	Operand1 = Operand2
	CCG	Operand1>Operand 2

Status register bits 0-7, are cleared by CPU reset. The current executing segment number in bits 8-15 is not affected.

Attempts to execute privileged instructions in User mode result in a trap to segment %17 with a parameter of 6 left on the interrupted stack "stack marker". The instruction is not executed.

Mode determines bounds checking as follows:	User/Privileged
Program Transfer	Yes/Yes
Operand Read or Write	Yes/No
Stack Overflow	Yes/Yes
Stack Underflow	Yes/No

Interrupts Enabled (bit 1) enables or disables "External Interrupt" and "Module Interrupt"; if Status(1)=0 and the Dispatcher Flag is set, disables "Console Interrupt" also. "External" or "Module" Interrupt will then result in an interrupt

if in "RUN" and "Run Mode Intrpts" are enabled
or if in "HALT" and "Halt Mode Intrpts" are enabled.

Internal interrupts are always enabled when in "HALT".

Traps Enabled (bit 2) enables or disables user math traps (integer or floating point overflow, floating point underflow, integer or floating point divide by 0). A trap results when Status(2,4)=1.

Right Stack-op Pending (bit 3) indicates the pending execution of Stack-op B in a dual stack-op **(STKOPA,STKOPB).**

CPX REGISTERS

BIT	**CPX1 (RUN)**	CCPX	**CPX2 (HALT)**
0	Integer Overflow	XFER NIR-CIR (Diag)	→ ✱Run FF ←
1	System Parity Error ←	Clear System PE FF	✱Cold Load
2	Address Parity Error ←	Clear ADDR PE FF	✱Single Instruction
3	Data Parity Error ←	Clear Data PE FF	✱Load Register
4	CPU Timer ←	Clear Timer FF	✱Display Memory
5	Bounds Violation ←	Clear BNOV FF	✱Load Memory
6	Illegal Address ←	Clear Ill. ADDR FF	✱Execute Switch Reg
7	Module Interrupt ←	Clear Mod Int. FF	Increment Address
8	External Interrupt ←	Clear Ext Int. FF	Decrement Address
9	Console Interrupt ←	Reset Front Panel FF	Inh. Auto Restart
10	Power Fail	Turn Off Interrupts	I/O Timer
11	-Unused-	Clear Intrp Stack Flag →	Intrp Stack Flag
12	-Unused-	Clear Dispatcher Flag →	Dispatcher Flag
13	-Unused-	Set System HALT Light	-Unused-
14	-Unused-	Microcode Halt (Diag)	-Unused-
15	-Unused-	Reset Front Panel FF	✱System Dump

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INTERRUPTS/TRAPS, sheet 1 of 2

Interrupt	Parameter (on the ICS @ Q+2)	
0 External Interrupt	DEV #	
1 Power Fail	-	
2 Power On	-	
3 Stack Overflow	-	
4 Module Interrupt	MODL #)	> in SP1 Register
5 Console Interrupt	CPU ID)	
6 Cold Load	-	
7 -	-	

	Parameter (on the current stack at Q+1)
10 -	-
11 Module Error (MCU ERRORS):	
Illegal Address	1000
Bounds Violation	2000
Non-responding Module	4000
12 Parity Error (CPU ERRORS):	
System P.E.	40000
Memory Address P.E.	20000
Data P.E.	
13 Miscellaneous:	
Stack Underflow	1
CST Bounds Violation	2
STT Bounds Violation	3
14 Code Segment Absence:	
PCAL	P-Label
EXIT	N
15 STT Entry Uncallable	P-Label
16 TRACE (PCAL only)	P-Label

INTERRUPTS/TRAPS, sheet 2 of 2

17 User Traps:

-	0
Integer Overflow	1
Floating Point Overflow	2
Floating Point Underflow	3
Integer Divide by 0	4
Floating Point Divide by 0	5
System (always enabled):	
Privileged Instruction	6
Unimplemented Instruction	7

CPX1(2,3,6) indicate CPU/memory errors only. I/O errors appear as follows:

- Address Parity - sets IOP APE, generates transfer error*.
- System Parity - sets IOP APE, generates transfer error*.
- Module Violation - sets IOP Illegal Address, generates transfer error*.
- Data Parity (IOAW/IOCW/DRT) - generates transfer error*.

CCPX(10,13,14 are irrevocable.

CCPX(15) clears general interrupts, Single Instruction/Execute B-Register, and MCU breakpoint halt circuits.

CCPX(9) clears general interrupt circuit only (Console Interrupt).

Cold Load and System Dump set RUN, execute, and terminate in HALT.

* Transfer errors are retried under MPE.

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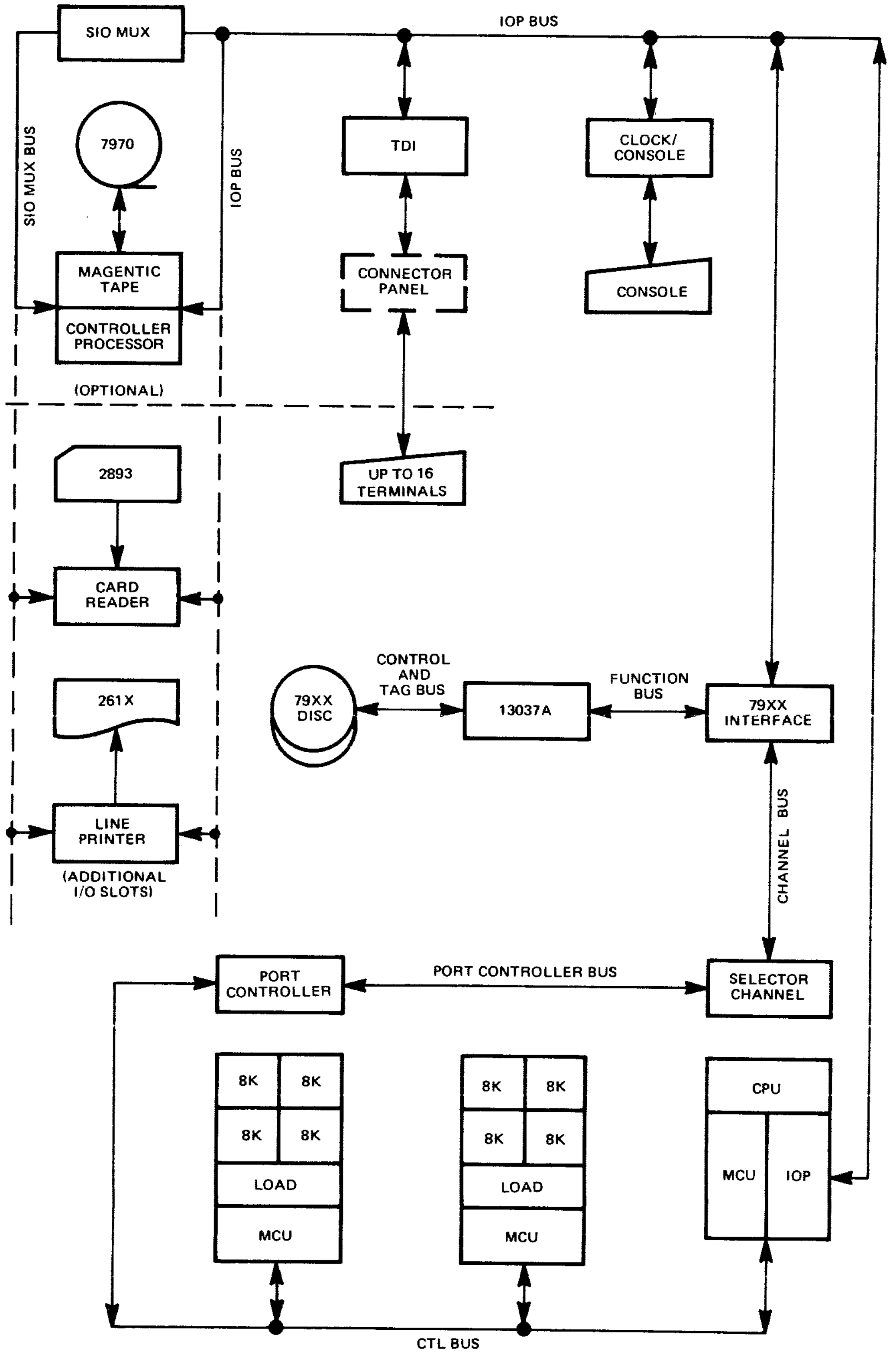

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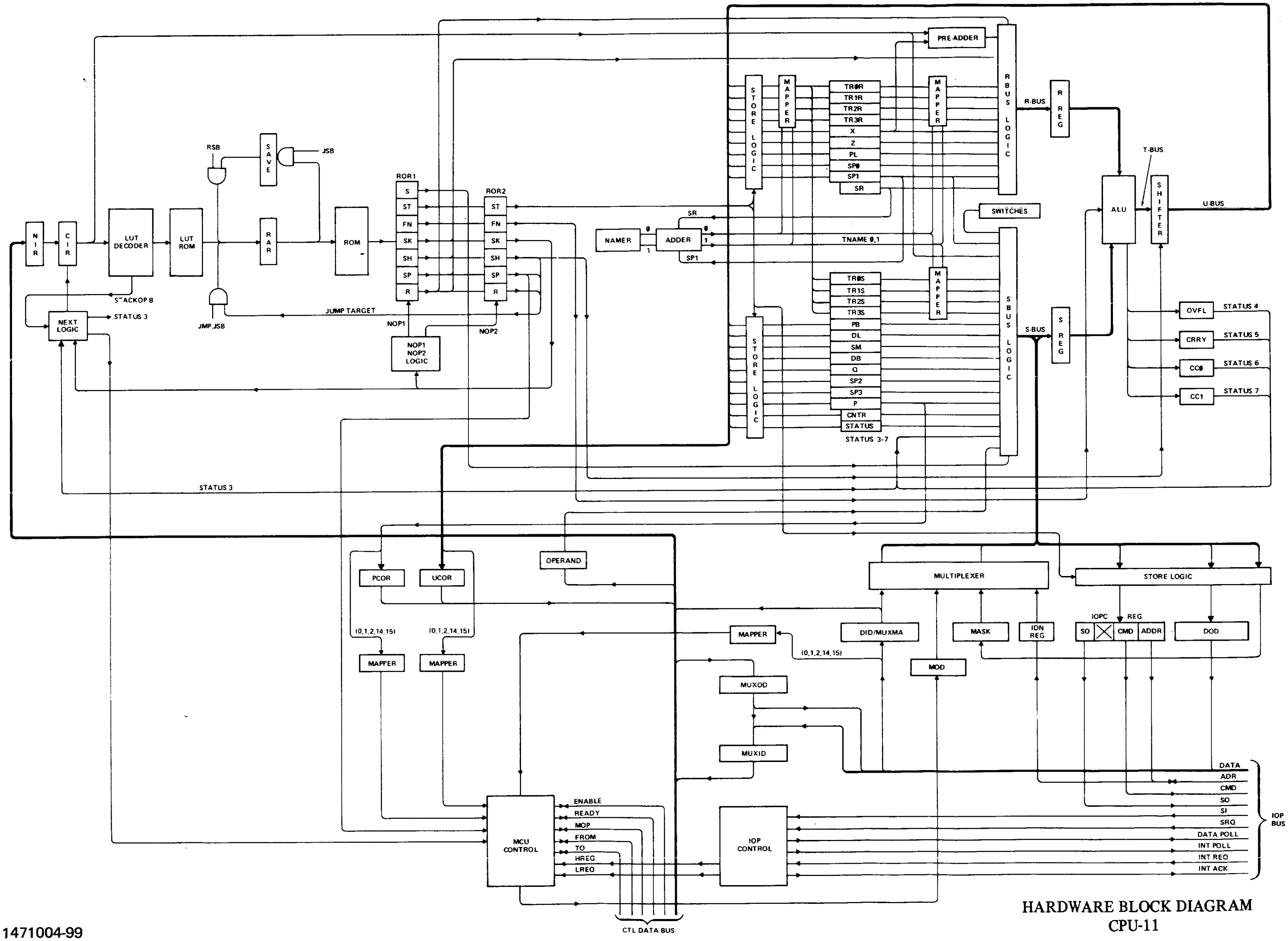
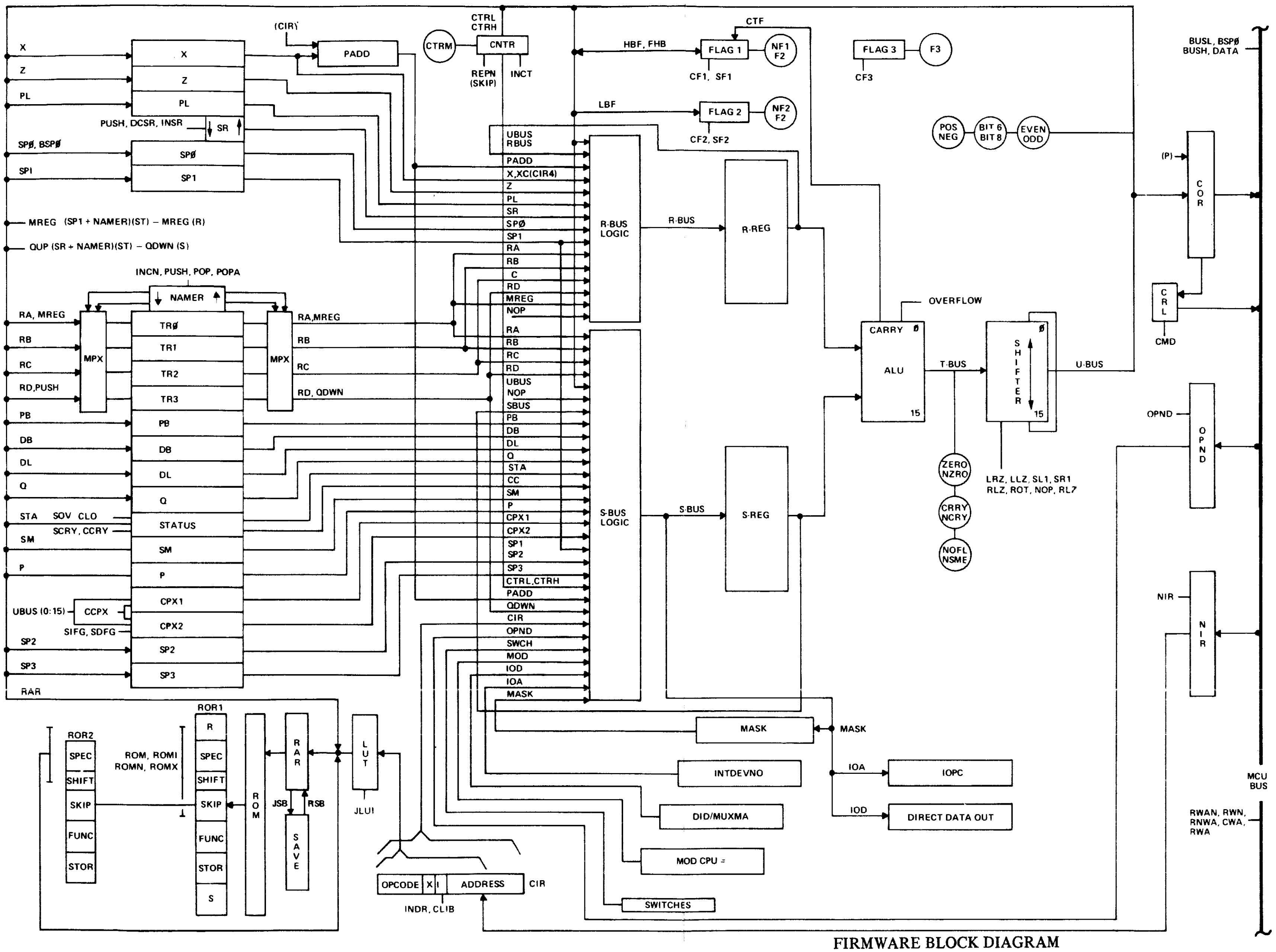
HP 3000 PRE SERIES II SYSTEM FUNCTIONAL DIAGRAM



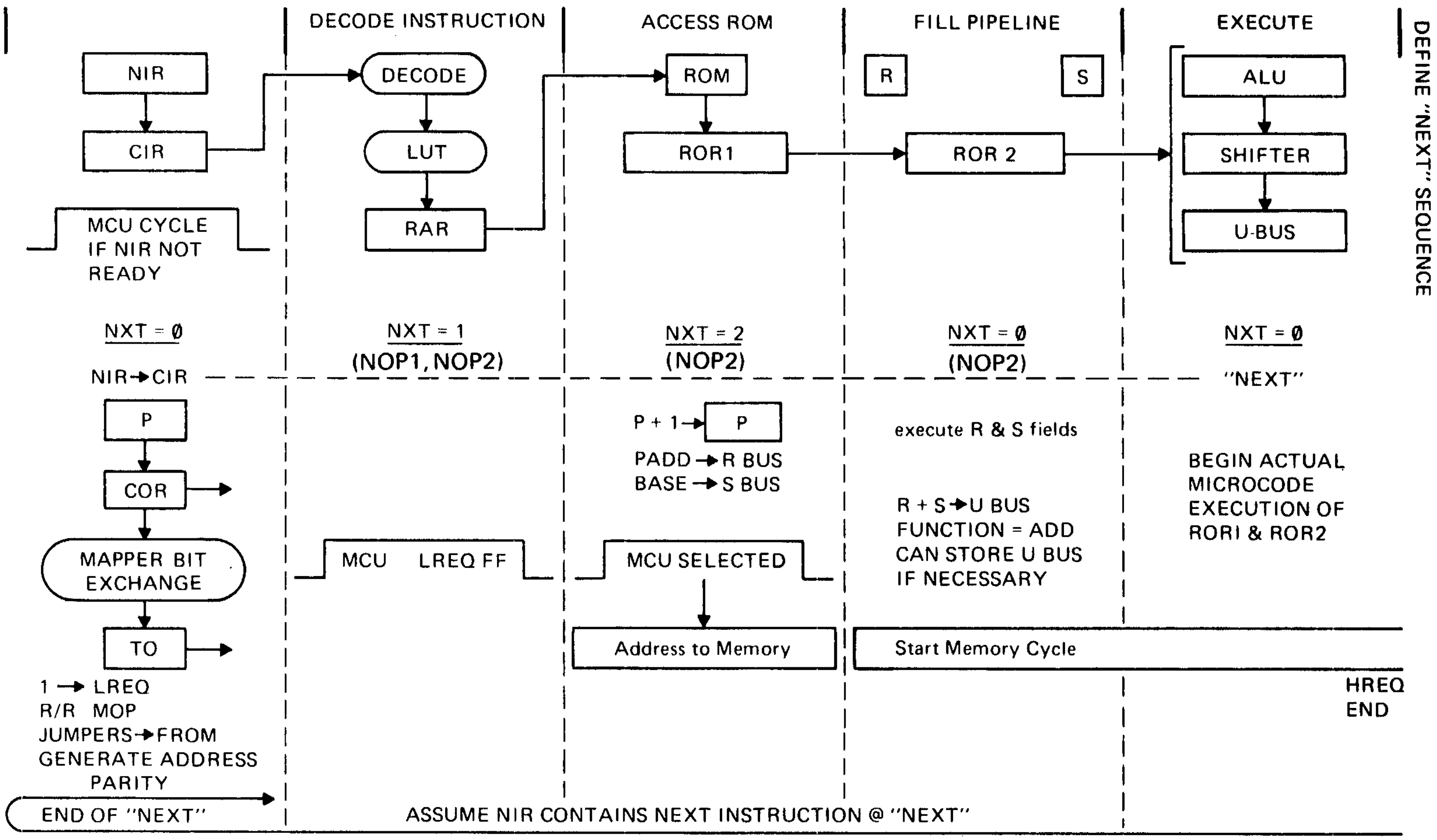
HARDWARE BLOCK DIAGRAM
CPU-11

CENTRAL PROCESSOR UNIT

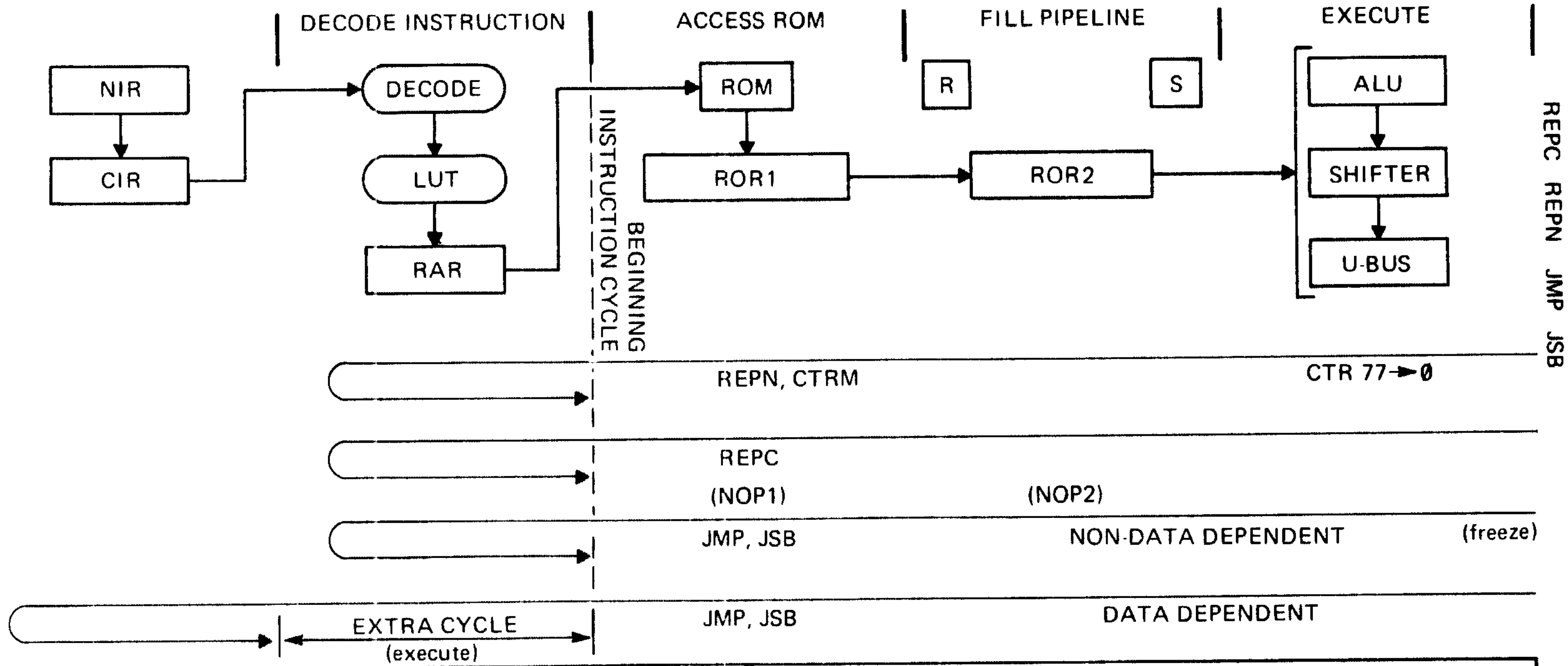


FIRMWARE BLOCK DIAGRAM
CPU-12

1471004-100

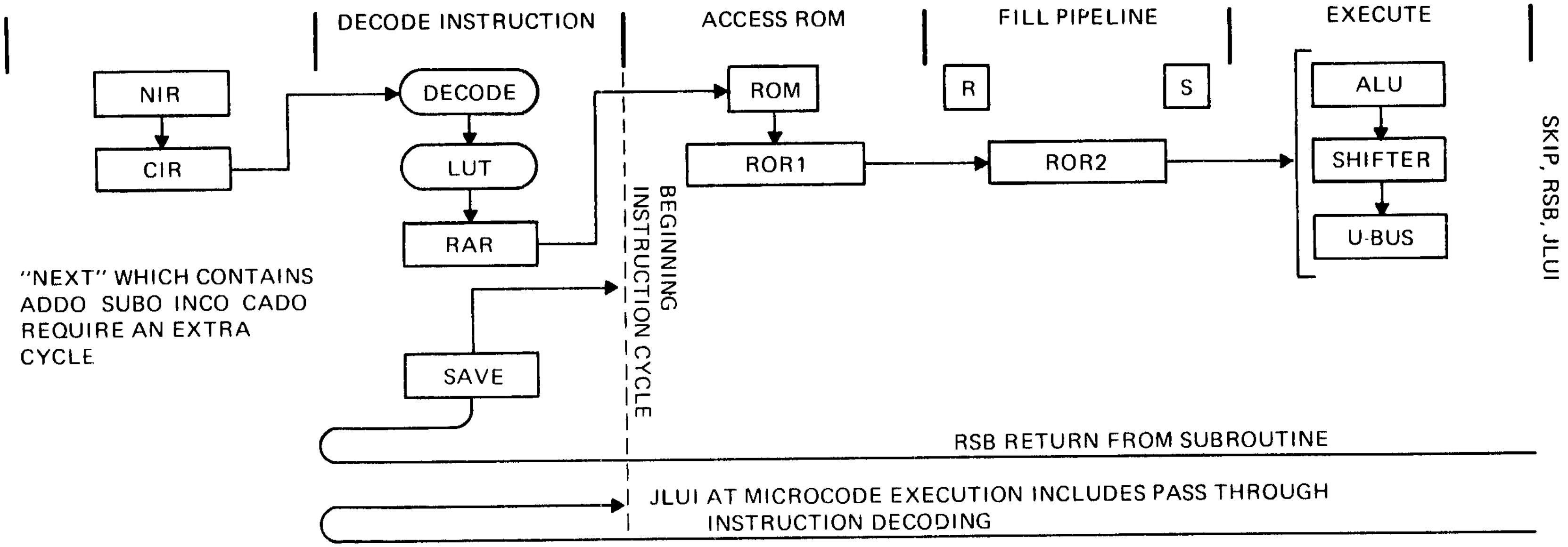


ROM CYCLES, sheet 1 of 3



DATA DEPENDENT	NON-DATA DEPENDENT
BIT 6 BIT 8 CARRY NCRY EVEN ODD NEG POS NOFL NSME NZRO ZERO	CTRM INDR NPRV TEST F1 NF1 F2 NF2 F3 SRZ SRNZ SRL2 SRL3 SR4 SRN4 UNC RSB JLUI NEXT

ROM CYCLES, sheet 2 of 3



"NEXT" WHICH CONTAINS ADDO SUBO INCO CADO REQUIRE AN EXTRA CYCLE.

If SKIP condition is met, ROR2 is NOP'd at execution time. Thus the skipped instruction must still be counted.

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ROM CYCLES, sheet 3 of 3

JUMPERS

CPU #1 (MCU)

W1 In
W2 Out

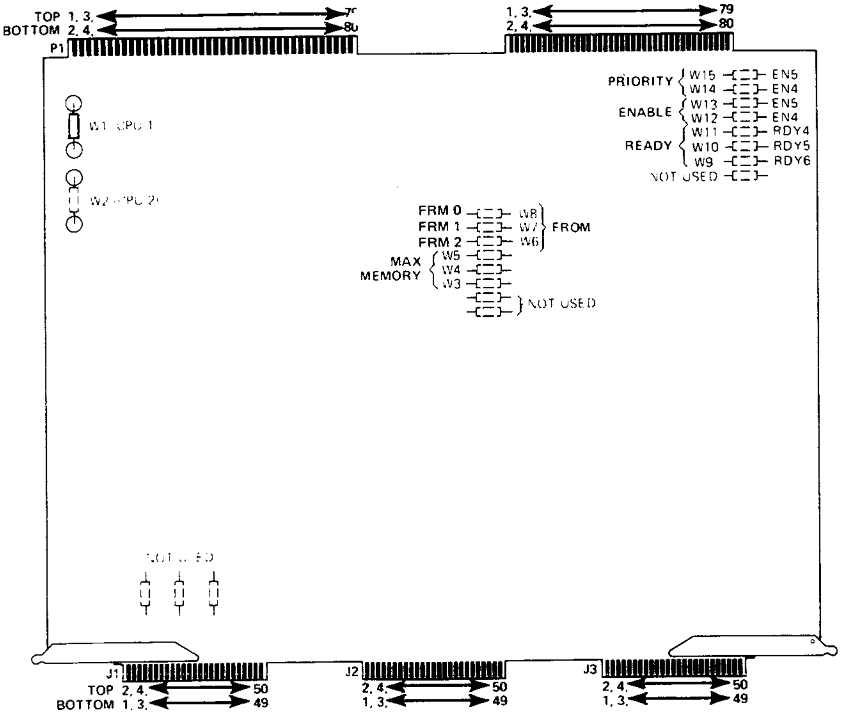
CPU Module #		4	5 *	6 (MCU)
FROM	W6	In	Out	In
	W7	In	In	Out
	W8	Out	Out	Out
READY	W9	Out	Out	In
	W10	Out	In	Out
	W11	In	Out	Out
ENABLE	W12	In	Out	Out
	W13	Out	In	Out
PRIORITY	W14	Out	In	In
	W15	Out	Out	In

* Standard Configurations

Maximum Memory Jumpers (MCU, IOP)
(Total Number of Words)

IOP/MCU	40K	48K *	56K	64K *
W1/W3	Out	Out	Out	Out
W2/W4	In	In	Out	Out
W3/W5	In	Out	In	Out

* Standard Configurations



MODULE CONTROL UNIT (MCU)

30001-60007

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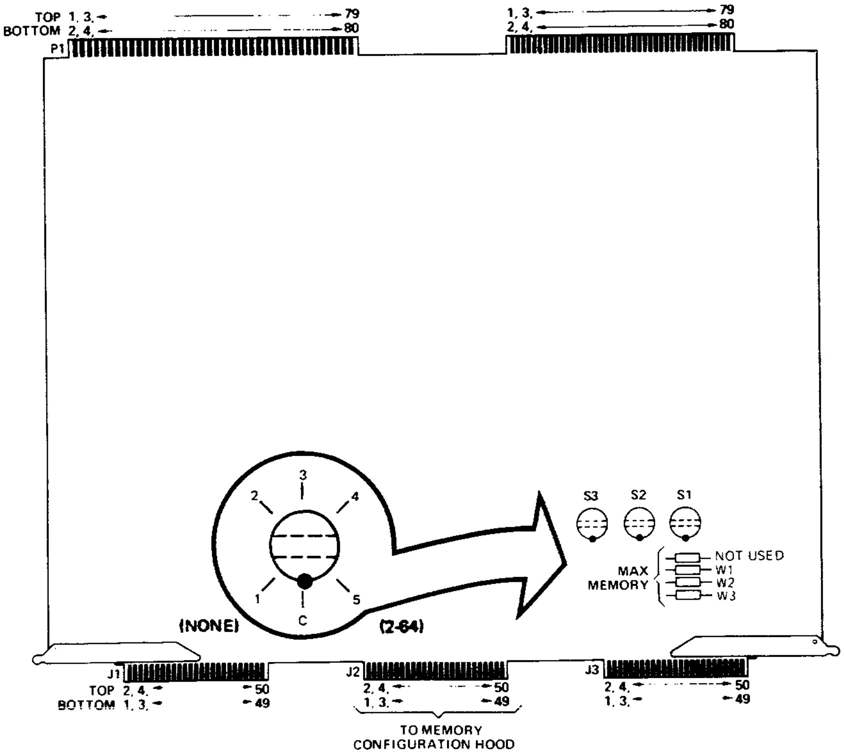

INPUT/OUTPUT PROCESSOR (IOP)

30001-60008

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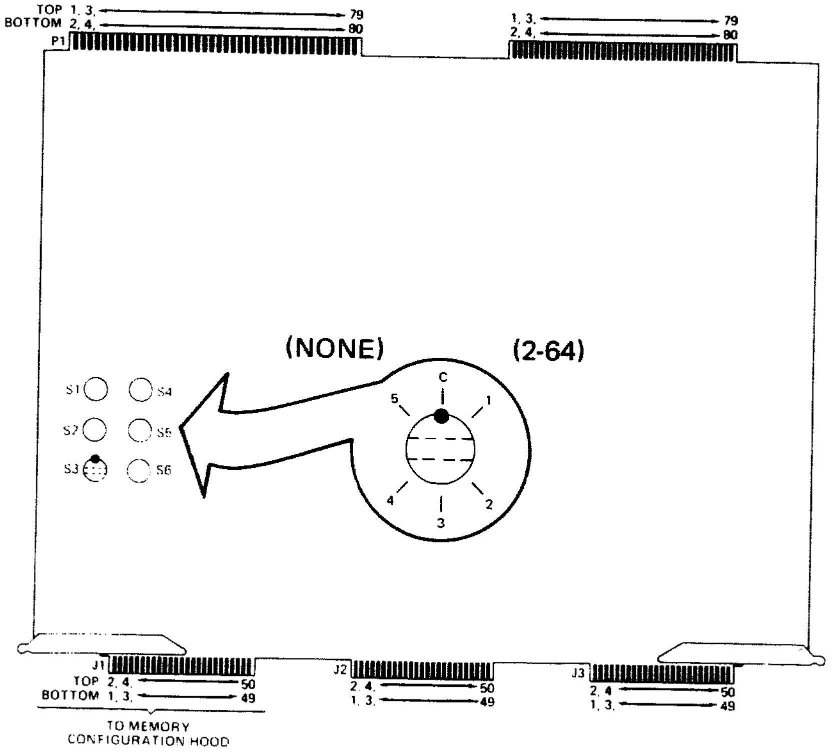
MCU-IOP-MEMORY CONFIGURATION, sheet 1 of 2

PCA CARD CONFIGURATION



S-BUS PCA (30001-60005)

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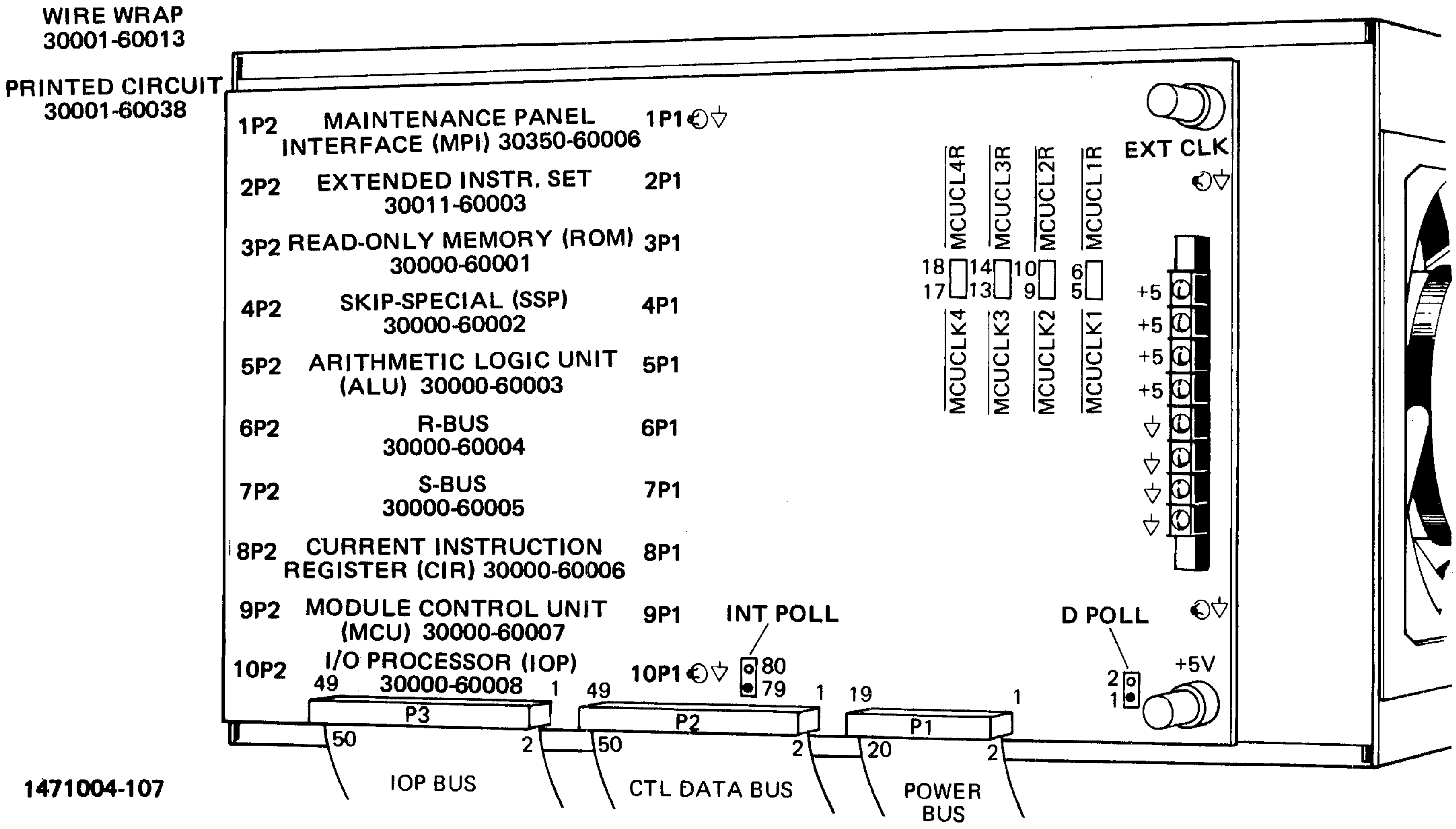
MCU-IOP-MEMORY CONFIGURATION, sheet 2 of 2



30001A CPU BACKPLANE

SIGNALS

CONNECTOR	SIGNAL		INTERFACE LOGIC
P2 (TOP)			
1			
3	MCUD	1	TRI-STATE
5	MCUD	3	
7	MCUD	5	
9	MCUD	6	TRI-STATE
11	MCUD	8	
13	MCUD	10	
15	MCUD	11	TRI-STATE
17	MCUD	13	
19	MCUD	15	
21	⏚		
23	TO	1	TRI-STATE
25	FROM	0	
27	FROM	2	
29	MOP	1	
31	READY	6	OPEN COLLECTOR
33	READY	0	OPEN COLLECTOR
35	READY	2	
37	READY	4	
39	⏚		
41	ENABLE	1	
43	ENABLE	3	
45	ENABLE	5	
47	$\overline{\text{MCUD PE}}$		OPEN COLLECTOR
49	$\overline{\text{MCU RST}}$		

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CONNECTOR	SIGNAL		INTERFACE LOGIC
P2 (BOTTOM)			
2	MCUD	0	TRI-STATE
4	MCUD	2	
6	MCUD	4	
8	⏚		
10	MCUD	7	TRI-STATE
12	MCUD	9	
14	⏚		
16	MCUD	12	TRI-STATE
18	MCUD	14	
20	MCUDPRTY		
22	TO	0	TRI-STATE
24	TO	2	
26	FROM	1	
28	MOP	0	
30	⏚		
32	SYSPRTY		TRI-STATE
34	READY	1	OPEN COLLECTOR
36	READY	3	
38	READY	5	
40	ENABLE	0	
42	ENABLE	2	
44	ENABLE	4	
46	⏚		
48	$\overline{\text{SYS PE}}$		OPEN COLLECTOR
50	⏚		

CENTRAL DATA BUS (CTL)

SIGNAL INDEX

P1

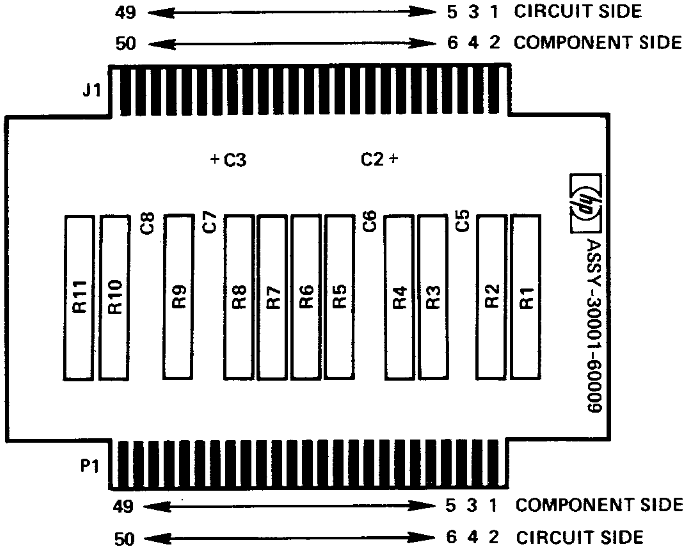
PIN	SIGNAL
1	COM
2	MCUD00
3	MCUD01
4	MCUD02
5	MCUD03
6	MCUD04
7	MCUD05
8	XXX
9	MCUD06
10	MCUD07
11	MCUD08
12	MCUD09
13	MCUD10
14	XXX
15	MCUD11
16	MCUD12
17	MCUD13
18	MCUD14
19	MCUD15
20	MCUDPRTY
21	XXX
22	TO00
23	TO01
24	TO02
25	FROM00
26	FROM01
27	FROM02
28	MOP00
29	MOP01
30	XXX
31	READY06
32	SYSPRTY
33	READY00
34	READY01
35	READY02
36	READY03
37	READY04
38	READY05
39	XXX
40	ENABLE00
41	ENABLE01
42	ENABLE02
43	ENABLE03
44	ENABLE04
45	ENABLE05
46	XXX
47	$\overline{\text{MCUDPE}}$
48	$\overline{\text{SYSPE}}$
49	$\overline{\text{MCUDRST}}$
50	XXX

J1

PIN	SIGNAL
1	COM
2	+5V
3	COM
4	+5V
5	COM
6	+5V
7	—
8	—
9	—
10	—
11	—
12	—
13	—
14	—
15	—
16	—
17	—
18	—
19	—
20	—
21	—
22	—
23	—
24	—
25	—
26	—
27	—
28	—
29	—
30	—
31	—
32	—
33	—
34	—
35	—
36	—
37	—
38	—
39	—
40	—
41	—
42	—
43	—
44	—
45	+5V
46	COM
47	+5V
48	COM
49	+5V
50	COM

I.C. INDEX

U	1820-
No I.C.s	



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CENTRAL DATA BUS (CTL)

STAND-ALONE CPU DIAGNOSTIC

This diagnostic program confirms the proper operation of the HP 30001A Central Processing Unit, configured CPU1 or CPU2. All program instructions which may be tried by a stand-alone program are tested. The instruction set is verified. Most of the conditions which result in interrupts and traps are tested.

The program can be used by field service, manufacturing and system test personnel for the isolation of instruction failures, interrupt failures and trap failures.

Core memory is not exhaustively tested; nor are instructions at the microcode level. Separate diagnostics are available for those purposes.

BRIEF DESCRIPTION OF SECTIONS

The CPU Diagnostic is divided into five sections. Each section is an independently-loadable program.

* Program Section 1

  Approximately half of the CPU instruction set is tested in this section. Once tested, these instructions are used to test other instructions.

* Program Section 2

  The remaining instructions are tested (except the I/O instructions).

* Program Section 3

  I/O instructions are tested (except those which involve Interrupts).

* Program Section 4

  All interrupt situations are tested including: I/O interrupt sequences, arithmetic overflow and underflow, privileged instructions in nonprivileged mode, and other interrupt conditions within the CPU.

* Program Section 5

  All address-out-of-bounds conditions are tested, including CPU hardware tests for program accesses of addresses out of program area, stack area, or core boundries. Four optional unrecoverable system halt tests are also available.

GENERAL LIMITATIONS OF TESTS

1. The purpose of these tests is to exercise go-nogo reliability of the CPU. An exhaustive test of all possible program characteristics is not done.
2. The stand-alone CPU diagnostics do not check core memory completely.
3. Intermittent errors may be detected, but the diagnostic does not contain any specific loops designed to catch them.
4. Except for the TSTB instruction, where all 256 possibilities on the TOS are checked, there are no data pattern tests.
5. I/O instruction tests are incomplete (cooperating I/O devices are required).
6. Parity errors cannot be forced and tested.
7. Module violation cannot be forced and tested.
8. The following parts of the microprogram are not tested:
   a. Any routines executed in the halt mode.
   b. This diagnostic does not check out the panel. This includes cold dump, which is considered a panel function.
   c. The system halt when a parity error occurs while in segment %12.
9. External interrupts on more than one device are not tested.
10. The time span available for program execution following a power fail is not checked.
11. The temporary store of all 1´s into memory by the TSBM instruction cannot be tested.

Stand-alone HP 30001A CPU Diagnostic

Loading

After cold load of Section 1, the core image is as follows:

Octal location	
0	CSTP = %2000
1	COLD LOAD P = %2140
2-3	0
4	CPCB1 = DB + 10 = %2440
5	QI(1) = %3710
6	ZI(1) = %3777
7	0
10	CPCB2 = %2410
11	Q(12) = %3710
12	Z(12) - %3777
13	0
14-1777	DRT TABLE
2000-2045	CST TABLE
2046-2077	0's
2100-2117	halt instructions for unexpected interrupts
2120-2137	0's
2140-2177	initialization routine (code)
2200-3660	program (stack): DL = %2200 DB = %2400 S = Q = %3200 (after loading only) Z = %3660
3661-3677	0's
3700-3777	interrupt control stack: QI = %3710 ZI = %3777
4000	program PB main segment is segment 16 (%20)

DRT table

For each 4 word entry: SIOP = 0
PI = %2100
DBI = 0
IRF = 0

CST TABLE

```
2000:  CSTL = %40
2001:  0
2002:  %40001  (M = 1, L = 1)
2003:  %2101  address of halt 2 instruction (seg 1)
2004:  %40001  (M = 1, L = 1)
2005:  %2102  address of halt 2 instruction (seg 2)
  .
  .
  .
2036:  %$40001
2037:  %2117   address of halt 2 instruction (seg 17)
2040:  %40000  + L, where L = function of program size and
       M = 1.
2141:  %4000   PB of segment 16
```

Halt instructions

```
2100:  Halt 1 unexpected external interrupt
2101:  Halt 2 unexpected interrupt-segment 1
2102:  Halt 2 unexpected interrupt-segment 2
  .
  .
  .
2117:  Halt 2 unexpected interrupt-segment 17
```

Initialization Routine (Code)

```
Absolute Core               Octal
Octal Location    Label   Contents  Code        Contents

     2140                  040014   LOAD C0;    <<TOS <-- S-DB>>
     2141                  040014   LOAD C1;    <<TOS <-- Q-DB+4>>
     2142                  040014   LOAD C2;    <<TOS <-- Z-DB>>
     2143                  040014   LOAD C3;    <<TOS <-- DL-DB>>
     2144                  040014   LOAD C4;    <<TOS <-- DB>>
     2145                  027563   SETR %163   <<SET(DB,DL,Z,Q,S)>>
     2146                  040013   LOAD C5;    <<FORM EXIT MARKER
                                                  X = 0>>
     2147                  040013   LOAD C6;    <<DELTA P>>
     2150                  040013   LOAD C7;    <<STATUS>>
     2151                  040013   LOAD C8;    <<DELTA Q>>
     2152                  04006    LOAD C4;    <<TOS <-- DB>>
     2153                  031400   EXIT 0;     <<GO START DIAGNOSTIC
                                                  SEGMENT>>
     2154          C0:     000600   %600 ;      <<S-DB>>
     2155          C1:     000604   %604 ;      <<Q-DB+4>>
     2156          C2:     001260   %1260 ;     <<Z-DB>>
     2157          C3:     177600   %200 ;      <<DL-DB>>
     2160          C4:     002400   %2400 ;     <<DB>>
     2161          C5:     000000   0;          <<X>>
     2162          C6:     000000   0:          <<DELTA P=PB-P>>
     2163          C7:     100020   %100020 ;   <<STATUS>>
     2164          C8:     000004   4;          <<DELTA Q>>
```

CPU STAND-ALONE DIAGNOSTICS

SECTION 1

```
         ( MCU INTRPT FREEZE <-- INHIBIT  )
SWITCHES < RUN MODE INTRPT <-- ENABLE     >  DOWN POSITION
         ( HALT MODE INTRPT <-- INHIBIT   )
```

COLD LOAD SECTION 1

PRESS RUN - PAUSE 0 INSTRUCTION IN RUN %030020
PRESS RUN - PAUSE 0 INSTRUCTION IN HALT
*PRESS RUN - HALT 3 030363

B-REGISTER <-- %125252 (EVEN SWITCHES), PRESS RUN - HALT 4
B-REGISTER <-- %052525 (ODD SWITCHES), PRESS RUN - HALT 5
SELECT OPTIONS, PRESS RUN

0-5	UNUSED
6	VERIFY SR REGISTER HALT 6 - CNTR=0 HALT 7 - CNTR=2 HALT %10 - CNTR=4
7-8	UNUSED
9	VERIFY PROGRAM LIMITS HALT %11 - PB = %4027,PL= %4046
10-14	UNUSED
15	HALT AT END OF SECTION - HALT %17

MANUAL INITIALIZATION:

DL - %2200   PB - %4000
DB - %2400   P - %4000
Q - %3200   PL - %4000+SEG. LENGTH - 1 (%16247)
S - %3200   (PL LISTED ON REEL OF TAPE)
Z - %3660   STA - %100020

*SWITCH REGISTER TEST CAN BE BYPASSED BY SETTING P <-- %4044 AND SELECTING OPTIONS

SECTION 2

```
         ( MCU INTRPT FREEZE <-- INHIBIT
SWITCHES < RUN MODE INTRPT <-- ENABLE
         ( HALT MODE INTRPT <-- INHIBIT
```

COLD LOAD SECTION 2
SELECT OPTIONS, PRESS RUN

0-14	UNUSED
15	HALT AT END OF SECTION -HALT %17

SECTION 3

```
         ( TIMERS <-- ENABLE
         | MCU INTRPT FREEZE <-- INHIBIT
SWITCHES < RUN MODE INTRPT <-- ENABLE
         | HALT MODE INTRPT <-- INHIBIT
         (
```

COLDLOAD SECTION 3,
SELECT OPTIONS, PRESS RUN

DEFAULT VALUES:
CPU1
MAG TAPE = DEV #6
SYSTEM CLOCK = DEV #3

0-2	UNUSED
3	TO CHANGE MAG TAPE DEV # - HALT 3 B-REGISTER <-- MAG TAPE DEV #, PRESS RUN
4	TO CHANGE SYS CLOCK DEV # -HALT 4 B-REGISTER <-- SYS CLOCK DEV #
5	UNUSED
6	USE SYS CLOCK (I/O) INSTRUCTIONS
7	CPU1/CPU2 SELECT (SIRF INSTRUCTION)
8-14	UNUSED
15	HALT AT END OF SECTION -HALT %17

SECTION 4

```
            ( TIMERS <-- ENABLE
            | MCU INTRPT FREEZE <-- INHIBIT
   SWITCHES < RUN MODE INTRPT <-- ENABLE
            | HALT MODE INTRPT <-- INHIBIT
            (
```

COLD LOAD SECTION 4,
SELECT OPTIONS, PRESS RUN

DEFAULT VALUES
CPU1
CORE < 65K WORDS
MAG TAPE = DEV #6
SYSTEM CLOCK = DEV #3

0-1	UNUSED
2	TEST INTERRUPT MASK (not necessary)
3	TO CHANGE MAG TAPE DEV# -HALT 3 B REGISTER <-- MAG TAPE DEV#, PRESS RUN
4	TO CHANGE SYS CLOCK DEV# - HALT 4 B-REGISTER <-- SYS CLOCK DEV#, PRESS RUN
5	UNUSED
6	USE SYS CLOCK (I/O INSTRUCTIONS)
7	CPU1/CPU2 SELECT (CONSOLE INTERRUPT)
8	INDICATES 65K WORDS OF CORE
9	DO HALT MODE INTERRUPT TEST -HALT %11 HALT MODE INTRPT <-- ENABLE, PRESS SINGLE INSTRUCTION EXECUTE (INTEGER OVERFLOW) HALT 6, HALT MODE INTRPT <-- INHIBIT
10	DO CONSOLE INTERRUPT TEST - PAUSE %12 PRESS CONSOLE INTERRUPT
11	DO CONSOLE INTERRUPT TEST WHILE ON DISPATCHER AND INHIBITED - PAUSE %13 PRESS CONSOLE INTERRUPT NO INTERRUPT, PRESS RUN ONCE OR TWICE TO HALT, ONCE MORE TO RUN
12	DO POWER FAIL/ON TEST - PAUSE %14 TURN DC OFF AND ON
13	TO CHANGE CPU AND/OR CORE MODULE NUMBERS - HALT %15 B-REGISTER <-- (10*3) = CPU MODULE #, (13:3) = CORE MODULE #, PRESS RUN - HALT 5
15	HALT AT END OF SECTION - HALT %17

SECTION 5

```
                ( TIMERS <-- ENABLE
                | MCU INT. FREEZE <-- INHIBIT
       SWITCHES < RUN MODE INT. <-- ENABLE
                | HALT MODE INT. <-- INHIBIT
                (

COLD LOAD SECTION 5
SELECT OPTIONS, PRESS RUN

          0     - UNUSED

SEE       1     - SYSTEM HALT TEST (ABSENCE BIT IS SET IN CODE
                  SEGMENT).

        ( 2     - SYSTEM HALT TEST (CST LENGTH IS LESS THAN 32 WORDS).
NOTE  <
        ( 3     - SYSTEM HALT TEST (MODULE ERROR IS MODULE ERROR
                  SEGMENT).

BELOW     4     - SYSTEM HALT TEST (UNABLE TO RESET AN EXT.
                  INTERRUPT).

         5-7     -UNUSED

          8     - INDICATES MEMORY SIZE = 64K WORDS.

          9     - INDICATES MEMORY SIZE = 48K WORDS.

         10     - INDICATES MEMORY SIZE = 24K WORDS.

       10-14    - UNUSED

         15     - HALT AT END OF SECTION - %17
```

TROUBLESHOOTING CPU DIAGNOSTIC FAILURES

Halt 0 - CPU Diagnostic Error Halts.
Halt 1 - Unexpected External Interrupt (I/O).
halt 2 - Unexpected Internal Interrupt (CPU).

HALT 1 FAILURES

Any time a Mag Tape, Card Reader, or 7905/7920 comes On-Line an External Interrupt is generated. The address (DEVNO) of the device controller is stored in the Interrupting Device Number Register of the Aux. Control Panel.

HALT 2 FAILURES

There are numerous ways to cause Internal Interrupt or Traps. The Status Register bits 8-15 of the Aux. Control Panel will contain the CST number that invoked the Internal Interrupt i.e., Power Fail, CST #1; Console Interrupt, CST #5; Parity Error, CST #%12.

HALT 0 FAILURES

Most numerous and may be caused by any CPU PCA, Memory PCA or SIO Multiplexer PCA.

RELATION BETWEEN LISTING AND THE P REGISTER

To find a location in the listing given an address in the P register:

1. Subtract %4000 (PB of the diagnostic).
2. Determine which procedure (or outer block) from the PMAP.
3. Subtract its base.
4. Look for this resulting address in the listing.

Two examples follow using the partial listing and PMAP on the following pages.

Example 1 finds location in listing from P register.

Example 2 calculates breakpoint address.

Example 1: Given a halt 0 with the P register = %4541 while running Section 3.

1. P-%4000 = %4541 - %4000 = %541
2. This is in procedure CKSMSKRMSK (base - %532)
3. %541 - %532 = 7 . This points to the halt 0 at location 6 in procedure CKSMSKRMSK.

This halt suggests that something is wrong with the SMSK instruction.

Example 2: To set a breakpoint halt at relative location %27 in procedure CKSMSKRMSK, the absolute address to be set into the B register is:

1. base of CKSMSKRMSK = %532
2. %532 + %27 = %561
3. %561 + %4000 = %4561

NOTE

> The following information is for illustrative purposes only. Any actual code or PMAP´s is subject to change.

```
PAGE 0003   HEWLETT-PACKARD


00080000  00000 1
00081000  00000 1   PROCEDURE CKSED;   << CHECK SED INSTRUCTION >>
       PL-004
00082000  00000 1      BEGIN
00083000  00000 2         TOS←%100020;  SET(STATUS);  AS SED 1);  PUSH(STATUS);
00084000  00004 2         IF TOS<>%140020 THEN HALT0;             << STA(1) NOT SET >>
00085000  00010 2         AS SED 0);  PUSH(STATUS);
00086000  00012 2         IF TOS<>%101020 THEN HALT0;             << STA NOT %101020 >>
00087000  00016 2      END;  << CKSED >>

 00000  040017 027410 030041 024410 040014 001700 141202 030360    00010  030040 024410 040007
 00020  140020 101020

00088000  00000 1
00089000  00000 1   PROCEDURE CKSMSKRMSK;  << CHECK SMSK & RMSK INSTRUCTIONS >>
       PL-005
00090000  00000 1      BEGIN
00091000  00000 2
00092000  00000 2   << MASK=0;  SR=4 >>
00093000  00000 2         TOS←3;  TOS←2;  TOS←1;  TOS←0;  AS SMSK);  << SR=4 >>
00094000  00005 2         IF <> THEN HALT0;                       << NOT CCE >>
00095000  00007 2         IF TOS<>1 THEN HALT0;                   << STACK TROUBLE >>
00096000  00012 2         TOS←1;  TOS←2;  TOS←3;  TOS←4;  AS RMSK);  << SR=4;  CCG >>
00097000  00017 2         IF <= THEN HALT0;                       << NOT CCG >>
00098000  00021 2         IF TOS<>0 THEN HALT0;                   << TOS NOT 0 >>
00099000  00024 2         IF TOS<>4 THEN HALT0;                   << STACK TROUBLE >>
00100000  00027 2
00101000  00027 2   << MASK=%177777;  SR=0 >>
00102000  00027 2         TOS←-1;  AS PSHR 0;  SMSK);   << SR=0 >>
00103000  00032 2         IF <> THEN HALT0;                       << NOT CCE >>
00104000  00034 2         AS PSHR 0;  RMSK);  << SR=0 >>
00105000  00036 2         IF TOS<>-1 THEN HALT0;                  << TOS NOT -1 >>
00106000  00042 2      END;  << CKSMSKRMSK >>

 00000  021003 021002 021001 000600 030100 141202 030360 022001    00010  141202 030360 021001
 00020  030360 022000 141202 030360 022004 141202 030360 025001    00030  024400 030100 141202
 00040  141202 030360 031400

00107000  00000 1
00108000  00000 1   PROCEDURE CKDIO;
       PL-006
00109000  00000 1   << CHECK CIO, TIO, WIO, & RIO USING SYSTEM CLOCK IF SWITCH 6 >>
00110000  00000 1      BEGIN
00111000  00000 2         TOS←GSR;  AS TBC 6);  IF = THEN RETURN;  << RETURN IF SW 6 DOWN >>
00112000  00005 2
00113000  00005 2   << CIO/TIO;  CHS←2;  SR=0 >>
00114000  00005 2         TOS ← SCDN;  TOS←%50000;  AS PSHR 0;  CIO 1);  << SR=0 >>
00115000  00011 2         IF <> THEN HALT0;                       << NOT CCE >>
00116000  00013 2         IF TOS<>SCDN THEN HALT0;                << STACK TROUBLE >>
00117000  00016 2         TOS←SCDN;  AS PSHR 0;  TIO 0);   << SR=0 >>
00118000  00021 2         IF <> THEN HALT0;
00119000  00023 2         IF TOS.(2:3)<>2 THEN HALT0;             << DEV STA(2:4) NOT 2 >>
00120000  00027 2         IF TOS<>SCDN THEN HALT0;                << STACK TROUBLE >>
00121000  00032 2
00122000  00032 2   << CIO/TIO;  CHS=5;  SR=4 >>
```

1471004-110

PORTION OF LISTING USED TO FIND LOCATION IN CKSMSKRMSK
sheet 1 of 2

Portion of Listing Used to Find Location in CKSMSKRMSK
sheet 2 of 2

```
PMAP

     PROGRAM FILE SEC3.PUB.SYS

     SEG´            0       BASE   ENTRY

       CB´              34      0      0
       TERMINATE        47                   ?
       CKNRD            35     62     62
       CKCB             36    122    122
       CKBUSY           37    141    141
       CKSIO            40    206    206
       CKDIO            41    356    356
       CKSMSKRMSK       42    532    532
       CKSED            43    575    575
       CKSIRF           44    617    617
       GSR              45    720    720
       DELAY            46    731    731
       SEGMENT LENGTH         1020

     PRIMARY DB            27          INITIAL STACK      1440


     SECONDARY DB           0          INITIAL DL            0
     TOTAL CODE          1020          TOTAL RECORDS        11
```

The P-Register may be loaded so as to start from the beginning of the failing routine. Use the single-instruction switch to step through the failing instruction. Check all registers for proper information following execution of the failing instruction.

HP 30011A/OPT1/OPT2

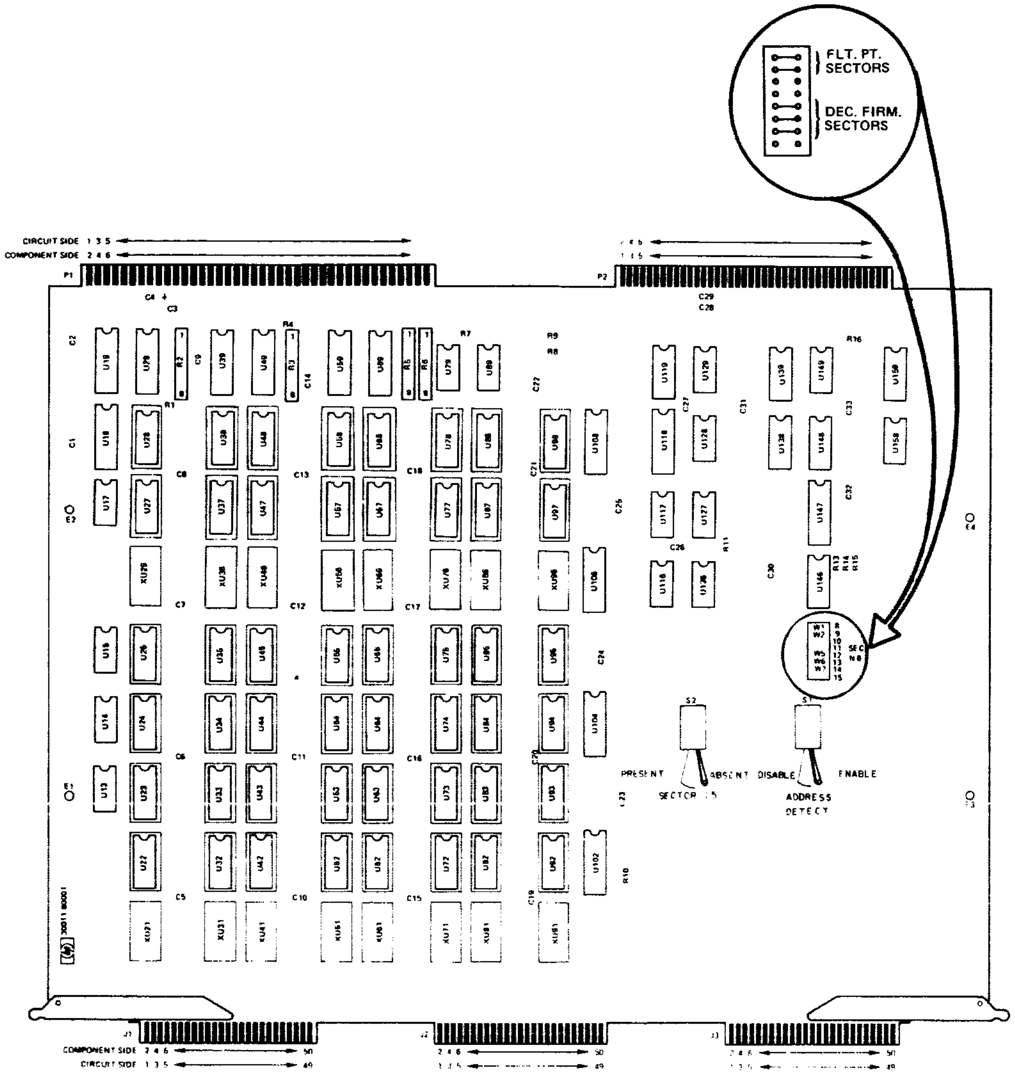
EXTENDED INSTRUCTION SET

This board installs in slot 1A2 and contains the micro-code to execute all Extended Precision Floating Point Arithmetic or Decimal Firmware Instructions Set or both.

Both Stand-Alone diagnostics for the Extended Floating Point Arithmetic and Decimal Firmware are GO/NO-GO.

If any failures occur while running either diagnostics then replace with a service kit board or disable switch S1 on the board.

Any customer software will automatically be executed much slower by software routines in MPE when the PCA is disabled or removed.



1471004-111

EXTENDED INSTRUCTION SET PCA, 30011-60003

DATA STORAGE FORMATS

THE HP3000 processes six types of data: integer, double integer, real, long (extended precision real), byte, and logical. Each data type has its own representation in memory, as described in the following paragraphs.

INTEGER FORMAT

Integers are whole numbers containing no fractional part. Integer values are stored in one 16-bit computer word. The leftmost bit (bit 0) represents the arithmetic sign of the number (1=negative, 0=positive). The remaining 15 bits represent the binary value of the number. Integer numbers are represented in two´s complement form in the range -32768 to +32767.

Decimal Value	Two´s Complement
+32767	%077777
.	.
.	.
.	.
+ 1	%000001
0	%000000
- 1	%177777
- 2	%177776
.	.
.	.
.	.
-32768	%100000

```
|---|-----------|-----------|-----------|-----------|-----------|
| 0|  1|  2|  3|  4|  5|  6|  7|  8|  9| 10| 11| 12| 13| 14| 15|
|---|-----------|-----------|-----------|-----------|-----------|
   FIELD DEFINITIONS:

| ^ |<--------------------- value ---------------------------->|
  |                        (15-bits)
  |-----sign bit (bit 0)
```

471004-112,113,114; sheet 1 of 5

DOUBLE INTEGER FORMAT

Integer values with magnitudes greater than the integer format range use the double integer format. Double integers use 2 computer words for a total of 32 bits. The leftmost bit of the first word (bit 0) is the sign bit (1=negative, 0=positive). The remaining 31 bits represent the binary value of the number. Double integer numbers are represented in two´s complement form in the range -2,147,483,648 to +2,147,483,647.

```
|<-------- Word 1 --------->|  |<--------- Word 2 ---------->|
|-|-----|---.. ..-----|-----|  |-|-----|---.. ..-|-----|-----|
|0| | | | | .. .. | | | | 15|  |0| | | | | .. .. | | | | | 15|
|-|-----|---.. ..-----|-----|  |-|-----|---.. ..-|-----|-----|
  Field/bit Definitions:

|^|<--------.. ..----------- value --------.. ..------------>|
 |                         (31-bits)
 |-----sign bit (bit 0)
```

REAL FORMAT

Real numbers are represented in memory by 32 bits (two consecutive 16-bit words) with three fields. The fields are the sign, the exponent, and the mantissa. The format is that known as "excess of 256" because exponents are biased by +256. Thus, a real number consists of:

Sign (S)
Bit 0 of the first word (positive=0, negative=1). A value X and its negative, -X, differ only in the sign bit.

Exponent (E)
bits 1 through 9 of the first word. The exponent ranges from 0 to 777 octal (511 decimal). This number represents a binary exponent, biased by 400 octal (256 decimal). The true exponent is E-256; it ranges from -256 to +255.

Fraction (F)
A binary number of the form 1.xxx, where xxx is represented by 22 bits, stored in bits 10 through 15 of the first word and all of the second word. Note that the 1. is not actually stored, but is assumed to the left of the binary point. Floating-point zero is the only exception: it is represented by all 32 bits being zero.

The range of the magnitude of non-zero real values is from 8.63617 * 10^-78 to 1.157921 * 10^77. Real numbers are accurate to 6.9 decimal places.

471004-112,113,114; sheet 2 of 5

The internal representation for real numbers is:

```
|<-------- Word 1 --------->|  |<--------- Word 2 ---------->|
|-|-----|---.. ..-----|-----|  |-|-----|---.. ..-|-----|-----|
|0|     |   .. ..     |   15|  |0|     |   .. .. |     |   15|
|-|-----|---.. ..-----|-----|  |-|-----|---.. ..-|-----|-----|
  Field/bit Definitions:

|^|<--exponent--->|<---------------fraction----------------->|
 |     (9-bits)                    (22-bits)
 |
 |-----sign bit (bit 0)
```

The formula for computing the decimal value of a floating-point representation is:

```
     Decimal value = (-1)^S * F * 2^(E-256)
```

which is equivalent to:

```
     Decimal value = (-1)^S * (1.0 + (xxx * 2^-22)) * 2^(E-256)
```

For example, 7.0 is represented as

```
|<---------- Word 1 ----------->|<---------- Word 2 ----------->|
                      1.  (assumed)
|-|-----|-----|-----|-----|-----|-|-----|-----|-----|-----|-----|
|0|1|0|0|0|0|0|0|1|0|1|1|0|0|0|0|0|0|0|0|0|0|0|0|0|0|0|0|0|0|0|0|
|-|-----|-----|-----|-----|-----|-|-----|-----|-----|-----|-----|
|0                 9|10       15|0                            15|
| |                 |                                           |
|^|<--- exponent -->|<-------------- fraction ----------------->|
 |
 |----- sign bit
```

```
   Sign (S) = 0 (positive)

   Exponent (E) = 402 (octal) = 258 (decimal)

   Fraction (F) = 1.11 (binary) = (1 x 2^0)+(1 x 2^-1)+(1 x 2^-2)
                                =    1     +    1/2    +    1/4
                                =1.75 (decimal)
```

So, the decimal value of the real number is:

```
   (-1)^0 x 1.75 x 2^(258 - 256) = 1 x 1.75 x 2^2
                                 = 1.75 x 4
                                 = 7.0
```

471004-112,113,114; sheet 3 of 5

LONG FORMAT

Long numbers are represented in memory by 64 bits (four consecutive 16-bit words) with three fields. The fields are the sign, the exponent, and the mantissa. The format is that known as "excess of 256" because exponents are biased by +256. Thus, a long number consists of:

Sign (S)
Bit 0 of the first word (positive=0, negative=1). A value X and its negative, -X, differ only in the sign bit.

Exponent (E)
Bits 1 through 9 of the first word. The exponent ranges from 0 to 777 octal (511 decimal). This number represents a binary exponent, biased by 400 octal (256 decimal). The true exponent is E-256; it ranges from -256 to +255.

Fraction (F)
A binary number of the form 1.xxx, where xxx is represented by 54 bits, stored in bits 10 through 15 of the first word and all of the second, third, and fourth words. Note that the 1. is not actually stored, but is assumed to the left of the binary point. Floating-point zero is the only exception: it is represented by all 64 bits being zero.

The range of the magnitude of non-zero long values is from 8.636168555094445 * 10^-78 to 1.157920892373162 * 10^77. Long numbers are accurate to 16.5 decimal places. The formula for computing the decimal value of a floating-point representation is:

```
Decimal value = (-1)^S * F * 2^(E-256)
```

which, for long values, is equivalent to:

```
Decimal value = (-1)^S * (1.0 + (xxx * 2^-54)) * 2^(E-256)
```

The internal representation for long numbers is:

```
|<--Word 1--->| |<---Word 2--->| |<---Word 3--->| |<---Word 4-->|
|-------------| |--------------| |--------------| |-------------|
|0          15| |0           15| |0           15| |0          15|
|-------------| |--------------| |--------------| |-------------|
  Field/bit Definitions:

|^|<-v->|<------------------fraction----------------------->|
 |  |                      (54-bits)
 |  |
 |  |-----exponent (9-bits)
 |
 |-----sign bit (bit 0)
```

471004-112,113,114; sheet 4 of 5

BYTE FORMAT

Character strings are stored using byte format. Character values are represented by 8-bit ASCII codes, two characters packed in one 16-bit computer word. The number of words used to represent a character value depends on the actual number of characters in the string.

The internal representation of two byte values is:

```
|--|--------|--------|--------|--------|--------|
| 0| 1| 2| 3| 4| 5| 6| 7| 8| 9|10|11|12|13|14|15|
|--|--------|--------|--------|--------|--------|
  Field/bit Definitions:

|<----- character ----->|<----- character ----->|
         (8-bits)               (8-bits)
```

LOGICAL FORMAT

Logical values are stored in one 16-bit computer word. They are treated as unsigned integer values ranging from 0 to 65,535. A value is considered true if it is odd and false if it is even (i.e., only the last bit is checked). When a value is set to TRUE, a word of all ones is used (%177777). A value set to FALSE is all zeros.

The internal representation of a logical value is:

```
|--|--------|--------|--------|--------|--------|
| 0| 1| 2| 3| 4| 5| 6| 7| 8| 9|10|11|12|13|14|15|
|--|--------|--------|--------|--------|--------|
  Field/bit Definition:

|<------------------- value ------------------->|
                   (16-bits)
```

471004-112,113,114; sheet 5 of 5

DIAGNOSTICS STAND-ALONE

EXTENDED PRECISION FLOATING POINT S-A
30011A

1. COLD LOAD DIAG FILE # FROM NON-CPU COLD LOAD TAPE
   D1 HP 3000 EXTENDED FLOATING POINT OFF-LINE DIAG HP 3233
2. Q1 ENTER NUMBER OF ERRORS TO BE PRINTED? XX ((WHATEVER #))

SWITCH REGISTER OPTIONS:

0	SELECT EXTERNAL REGISTER
1	EADD AND ESUB TEST
2	EMPY TEST
3	EDIV TEST
4	ENEG TEST
5	ECMP TEST
*6	PROGRAM TRAP TEST
7	HALT AT END OF CYCLE FOR RECONFG
8	DO NOT CHECK FOR ERRORS
9	PRINT ERRORS ON LINE PRINTER
10	SUPPRESS NON-ERROR MSG´S
11	SUPPRESS ERROR MSG´S
12	
13	REPEAT CURRENT STEP
14	HALT ON NON-FATAL ERROR
15	HALT AT END OF CURRENT STEP

* WILL CAUSE A TRAP AND HALT SYSTEM

HALT CODES

When the diagnostic halts, a HALT instruction is displayed in the CIR indicators on the Auxiliary Control Panel. The halt-code part of the instruction is displayed in the CIR (12:15) indicators. The halts are described in table 2. The diagnostic may not function properly after halts %030372 and %030373; these halts therefore cannot be suppressed by switch register bit 14.

HALT CODES

Halt Code in CIR (octal)	Type of Halt
030364	Reconfiguration halt. (Switch-register bit 7 is set.)
030372	S should have equaled Q, but did not. This error may be fatal. (After a fatal error, the diagnostic may not function properly.) During the halt TOS contains the failing step number; TOS-1 contains the section number. An El message is provided.
030373	Unexpected interrupt. This error is fatal. (The diagnostic must be cold loaded again.) TOS contains the code segment number corresponding to the type of interrupt. TOS-1 contains the interrupt parameter (if any).
030374	Error message limit has been reached.
030375	End-of-step halt. (Switch-register bit 15 is set.)
030376	Test-step failure. During the halt TOS contains the failing step number; TOS-1 contains the section number. An El message is provided.
030377	End-of-program halt. (Switch-register bit 12 is set.)

DECIMAL FIRMWARE DIAGNOSTICS (S/A)

SWITCH REGISTER OPTIONS:

0 = Select External Switch Reg. (approx. 2 min/pass)
1 = Select Test 1 Double Multiply
2 = Select Test 2 Convert (CVAD)
3 = Select Test 3 Convert (CVBD)
4 = Select Test 4 Convert (CVDB)
5 = Select Test 5 (SRD)
6 = Select Test 6 Add Double (ADDD)
7 = Select Test 7 Stack Overflow
8 = Select Test 8 Byte Addressing
9 = Unused
10 = Suppress NON Error Messages
11 = Suppress NON Error Messages
12 = Halt After Complete Pass
13 = Loop on last step
14 = Halt on Error
15 = Halt after Step

HALT CODES

Halt Code Octal	Indication
0	Irrecoverable HALT (see next page)
1	
2	
3	
4	
5	
6	
7	
8	
9	
10	
11	
12	
13	
14	Maximum Error Number reached
15	HALT after step
16	Error Halt
17	Halt after Complete Cycle

IRRECOVERABLE HALTS (HALT 5)

ERROR CODE	ERROR TYPE
1	WRONG DB AFTER NON-TRAPPING TEST STEPS ALSO AFTER STEPS TRAPPING TO SEGMENT 17
2	WRONG Q AFTER NON-TRAPPING TEST STEPS ALSO AFTER STEPS TRAPPING TO SEGMENT 17
3	WRONG DB AFTER BOUNDS VIOLATION TEST STEPS
4	WRONG Q AFTER BOUNDS VIOLATION TEST STEPS
5	WRONG DB AFTER STACK-OVERFLOW TEST (STEP 701)
6	WRONG Q AFTER STACK-OVERFLOW TEST (STEP 701)
7	WRONG Q (OR DB) AFTER STACK UNDERFLOW TEST (STEP 702) DB IS TEMPORARILY ALTERED DURING THE TEST AT THIS POINT IS ALREADY RESET TO THE ORIGINAL VALUE THIS HALT WILL OCCURE IF Q-TEST DB IS WRONG.
11	WRONG Q IN TRAP 17
12	UNEXPECTED TRAP 17 - NOT DURING DECIMAL INSTRUCTION
13	WRONG Q IN TRAP 11
14	TRAP 11 ENTERED PRIVILEGED THIS TRAP EXPECTED ONLY FOR BOUNDS VIOLATION TEST STEPS. THEY ARE EXECUTED UNPRIVILEGED.
15	UNEXPECTED TRAP 11 - NOT DURING DECIMAL INSTRUCTION
16	WRONG TRAP CODE IN TRAP 11 - NOT BOUNDS VIOLATION
17	WRONG Q IN TRAP 3
20	UNEXPECTED TRAP 3 - NOT IN DECIMAL INSTRUCTION
21	WRONG 0 IN TRAP 13
22	TRAP 13 ENTERED PRIVILEGED THIS TRAP IS EXPECTED ONLY FOR STACK-UNDERFLOW TEST (STEP 702) EXECUTED UNPRIVILEGED.
23	UNEXPECTED TRAP 13 - NOT DURING DECIMAL INSTRUCTION
24	WRONG TRAP CODE IN TRAP 13 - NOT STACK-UNDERFLOW.

CORE MEMORY 30005A/6A

CORE MEMORY USED BY HP 3000 PRE SERIES II

Maximum size 64K words
Minimum size 32K words
2 Memory Modules
Maximum Module size 32K words
Minimum Module size 8K words

MCU logic will detect all single bit Parity Errors.

NOTE

> All HP 3000 and HP 3000CX systems were either sold with 48K word or 64K word configurations. All 64K word configurations should be jumpered for 2-way interleaving to take advantage of increased memory speed (up to 10% faster).

Each Memory Module consists of the following:

1 - Memory Data and Control PCA

1 - Memory Load PCA

1-4 - Memory Drive and Sense PCA (8K words each)

A memory Write cycle takes three clock cycles to complete (175 nsec x 3 cycles = 525 nsec).

A memory Read cycle takes six clock cycles to complete (175 nsec x 6 cycles = 1050 nsec).

TO FETCH NEXT INSTRUCTION

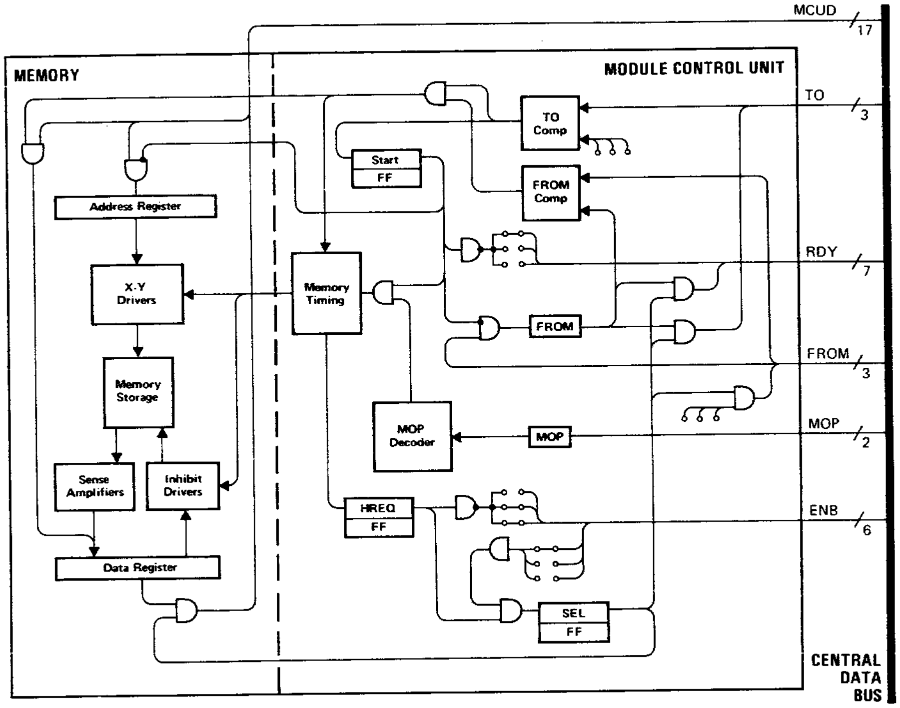
CPU TRANSMIT. The first step in fetching an instruction is to send an address to memory and tell memory what to do with that address (read contents and send back to CPU). The following three paragraphs describe this step.

When the NEXT micro-order is decoded from the ROM Skip field, a NEXT signal loads the contents of the P-register (address of instruction to be fetched) into the CPU Output Register. NEXT also transfers the Next Instruction Register contents into the Current Instruction Register (CIR). The CPU may proceed to execute the CIR contents while the following operations are in progress.

The objective now is to refill the Next Instruction Register. Assumming that the transmission may proceed, NEXT sets the LREQ (Low Request) flip-flop in the MCU. (The difference between low request and high request is that low request always checks to see if the destination module is ready to receive a transmission; high request assumes that the destination module is expecting the transmission, so readiness is not checked.) By this time, the MCU Operation Decoder has encoded the appropriate memory opcode (MOP), which is now in the MOP register. The memory opcode is a two-bit code which tells memory what to do when it receives bus data. The four possible codes are NOP (No Operation), CW (Clear/Write), RR (Read/Restore), and RNW (Read/No Write). In this case the memory opcode is RR. NEXT locks this code in the MOP register, and sets the NIP (Next In Process) flip-flop. Setting NIP "opens" the Next Instruction Register, so that it will load all central data bus transmissions until told to stop (by resetting NIP, later). NEXT also locks the TO register, which now contains the destination module number from the mapper.

The LREQ signal reads the TO register contents into the Ready Comparator, which checks the RDY (Ready) line from the intended destination to see if that module is ready to receive. If not, nothing further happens until the RDY line is true. The output of the Ready Comparator (through a set of changeable jumpers) pulls low on the Enable (ENB) line for this module number. Since each module cannot transmit unless all ENB lines of higher priority modules are high, this pulling low on one ENB line disables all lower priority modules (those with higher module numbers). Provided that no higher priority module has pulled low on its ENB line to this module (through a second set of jumpers), and provided the I/O Processor is not requesting the bus, the output of the Ready Comparator now sets the Select (SEL) flip-flop. The SEL signal reads out the CPU Output Register contents to the central data bus, as well as the TO and FROM module numbers and the memory opcode. SEL also pulls low on the destination module's RDY line for one cycle, so that other modules will not assume the memory module is ready before memory has a chance to pull the RDY line low itself on the next cycle.

MEMORY RECEIVE AND TRANSMIT. The next step in the process is for memory to receive the address from the bus, read the contents of the addressed location, and transmit the contents back to the CPU. The following two paragraphs describe this step.



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A TYPICAL MEMORY MODULE

The TO Comparator identifies the code on the TO lines as its own module number and sets a Start flip-flop. The Start signal locks the address word from the bus into the address register, and locks the FROM bits into the FROM register. The Start signal also keeps the module's RDY line pulled low (the CPU has pulled it low temorarily in the preceding cycle), and together with the decoded memory opcode begins the read/write memory cycle. The X-Y drivers begin to read the contents of the addressed memory location into the data register, via the sense amplifiers. Meanwhile, after a fixed delay, the MCU begins the process of requesting access to the bus by setting the HREQ flip-flop. (Since memory transmits only to modules that are expecting the transmission, only high request are used.) The HREQ signal pulls low its ENB line to lower priority modules and, provided no higher priority module has pulled low on its ENB line to this module, sets the Select flip-flop.

By this time, the memory location contents are in the data register, and the SEL signal reads the contents out to the central data bus. SEL also reads out the wired FROM code and the TO code (which is simply the saved FROM code, since transmission is back to the CPU).

CPU RECEIVE. The last step in the process is for the CPU to receive the instruction word, which is now on the central data bus, and load it into the Next Instruction Register. The following paragraph describes this step.

The TO Comparator identifies the code on the TO lines as its own module number, and gives a true output. Also, the FROM Comparator identifies the transmission as the one it was waiting for by comparing the saved TO register contents with the FROM lines of the bus; it therefore also gives a true output. (If the FROM code is not the expected one, it is loaded into the FROM register, and the bus information is processed as an interrupt from the identified module.) The two true outputs together reset the NIP flip-flop. The Next Instruction Register, which up until now has been freely loading all bus transmissions into itself, is now inhibited from further loading, since it now contains the expected next instruction.

TO FETCH AN OPERAND

The procedure for fetching an operand from memory is very similar to the procedure for fetching an instruction. The main differences are that the initiating signals are different, and the receiving register is the Operand (OPND) Register rather than the Next Instruction Register. The following descriptions are therefore somewhat abbreviated, primarily giving the overall flow of information. Refer back to the preceding descriptions if further logical details are necessary.

CPU TRANSMIT. The process of sending an address to memory begins when a BUSL (Bus Low) signal from the ROM Store field loads the U-bus contents into the CPU Output Register and sets the LREQ flip- flop. The MCU Operation Decoder gives a memory opcode to the MOP register and set the OPINP (Operand In Process) flip-flop. The OPND register now begins to load all bus transmissions. The LREQ signal causes the Ready Comparator to check if the destination module is ready and, if so, enters the priority structure.

When priority allows (ENB present), the Select flip-flop is set, causing the address in the CPU Output Register to be read out to the central data bus.

MEMORY RECEIVE AND TRANSMIT. The memory module, after recognizing its TO code and setting the Start flip-flop, locks the address from the bus into the address register. The Start signal, together with the decoded memory opcode, initiates the reading of the addressed location into the data register. Meanwhile, the HREQ flip-flop is set and priority is established. When ENB is present, the Select flip-flop is set causing the operand, now in the data register, to be read out to the central data bus. The saved FROM code is used to identify the destination (TO) as the CPU module.

CPU RECEIVE. The TO and FROM Comparators together cause the OPINP flip-flop to reset, thus locking the operand from the bus into the OPND register.

TO STORE AN OPERAND

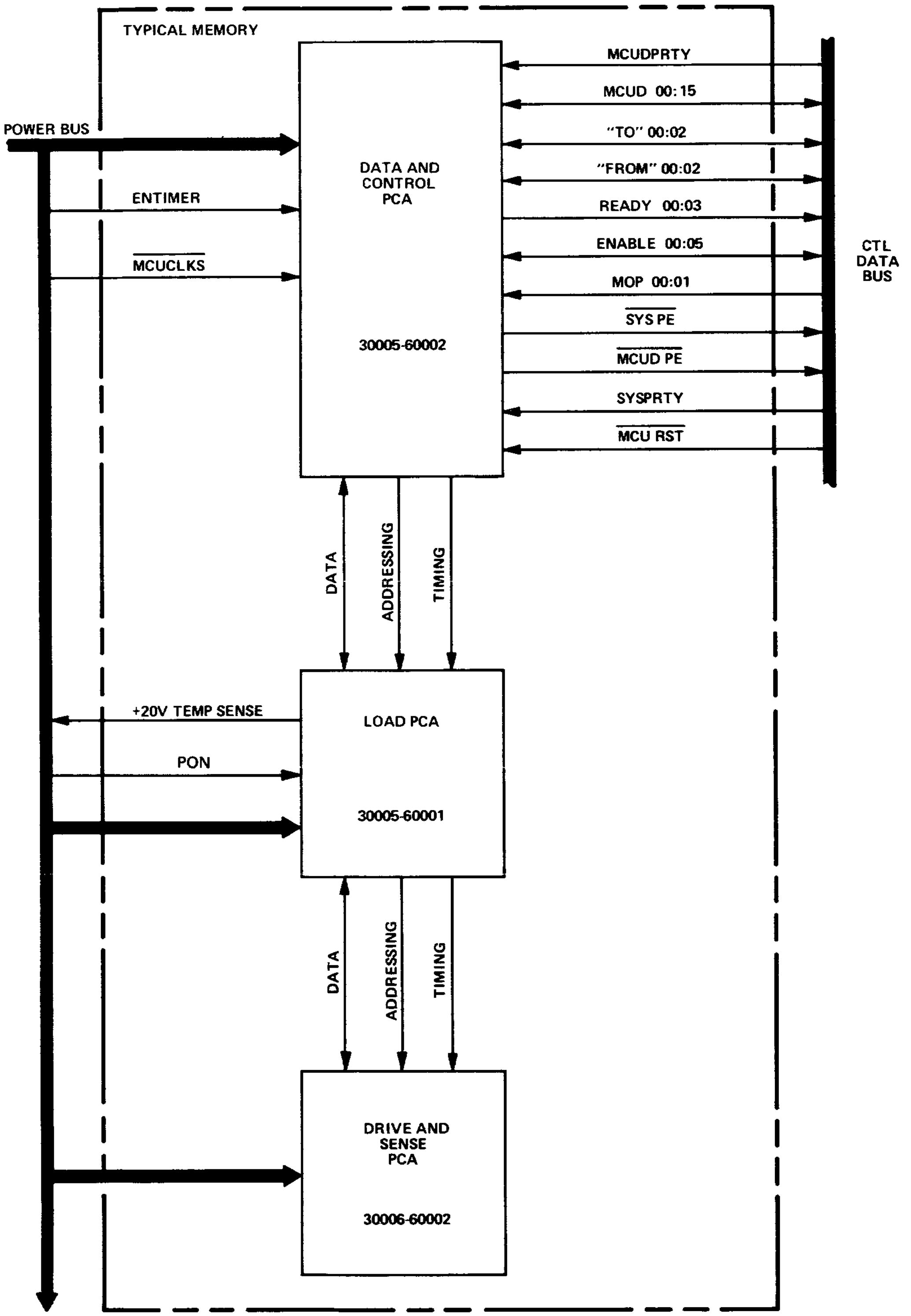
Storing an operand in memory involves much the same logic operations that were discussed in the preceding fetch transmissions. The main difference here is that instead of being a round trip, CPU to memory and then memory to CPU, there are two consecutive transmissions from the CPU to memory. The first transmission is the address, the second is the operand. The following paragraphs, again condensed to illustrate the overall flow of information, describe these transmissions.

CPU ADDRESS TRANSMIT. A BUSL signal from the ROM Store field loads the U-bus contents into the CPU Output Register and sets the LREQ flip-flop. The MCU Operation Decoder gives a memory opcode to the MOP register; in this case the opcode is Clear/Write rather than Read/Restore as in the previous cases. (Neither NIP nor OPINP flip-flops are set.) After checking if the destination module is ready and ENB is present, the LREQ signal causes the Select flip-flop to be set. This reads out the address to the central data bus.

MEMORY RECEIVE. The memory module, after recognizing its TO code and setting the Start flip-flop, locks the address from the bus into the address register. The Start signal, together with the decoded memory opcode, causes a "clear" half-cycle. The Start flip-flop remains set, and the FROM, MOP and address registers remain locked. Also the RDY line remains low, so no other modules may send a new address to this memory module.

CPU DATA TRANSMIT. The CPU, meanwhile, has put the operand on the U-bus, and a DATA signal from the ROM Store field loads it into the CPU Output Register. The DATA signal also sets the HREQ flip-flop. (Destination readiness does not need to be checked, since memory is expecting a data transmission from this module.) After priority checks, the HREQ signal sets the Select flip-flop, which reads out the operand to the central data bus. (The memory opcode is NOP, since memory is already holding the appropriate opcode.)

MEMORY RECEIVE. In the memory module the TO Comparator recognizes its TO code and the FROM Comparator verifies transmission from the correct module. The true outputs from both of these comparators cause the operand from the bus to be loaded into the data register, and additionally cause the memory timing to proceed with the second half of the clear/write memory cycle. This causes the operand to be stored into the addressed location.



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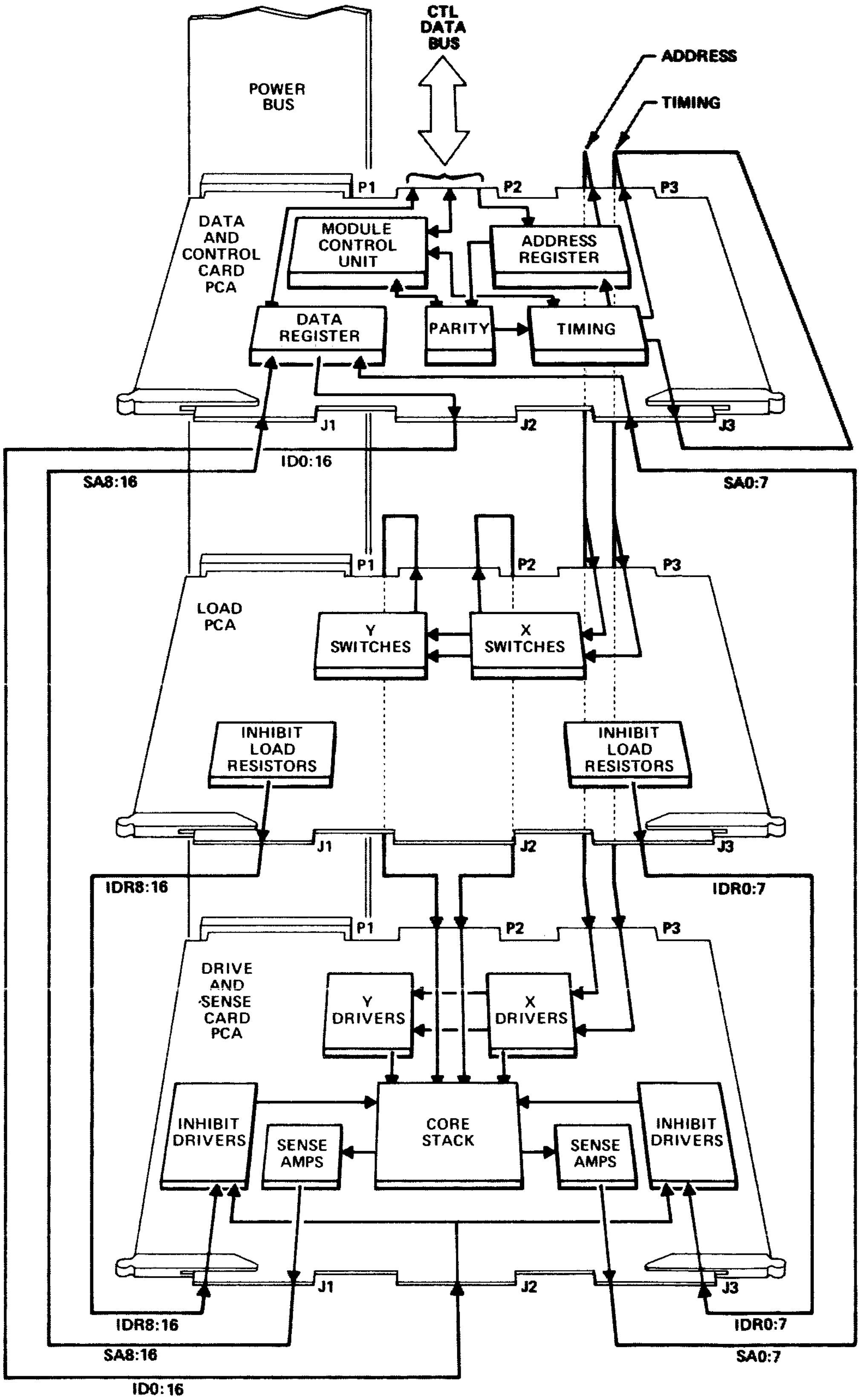
MEMORY INTERFACE DIAGRAM



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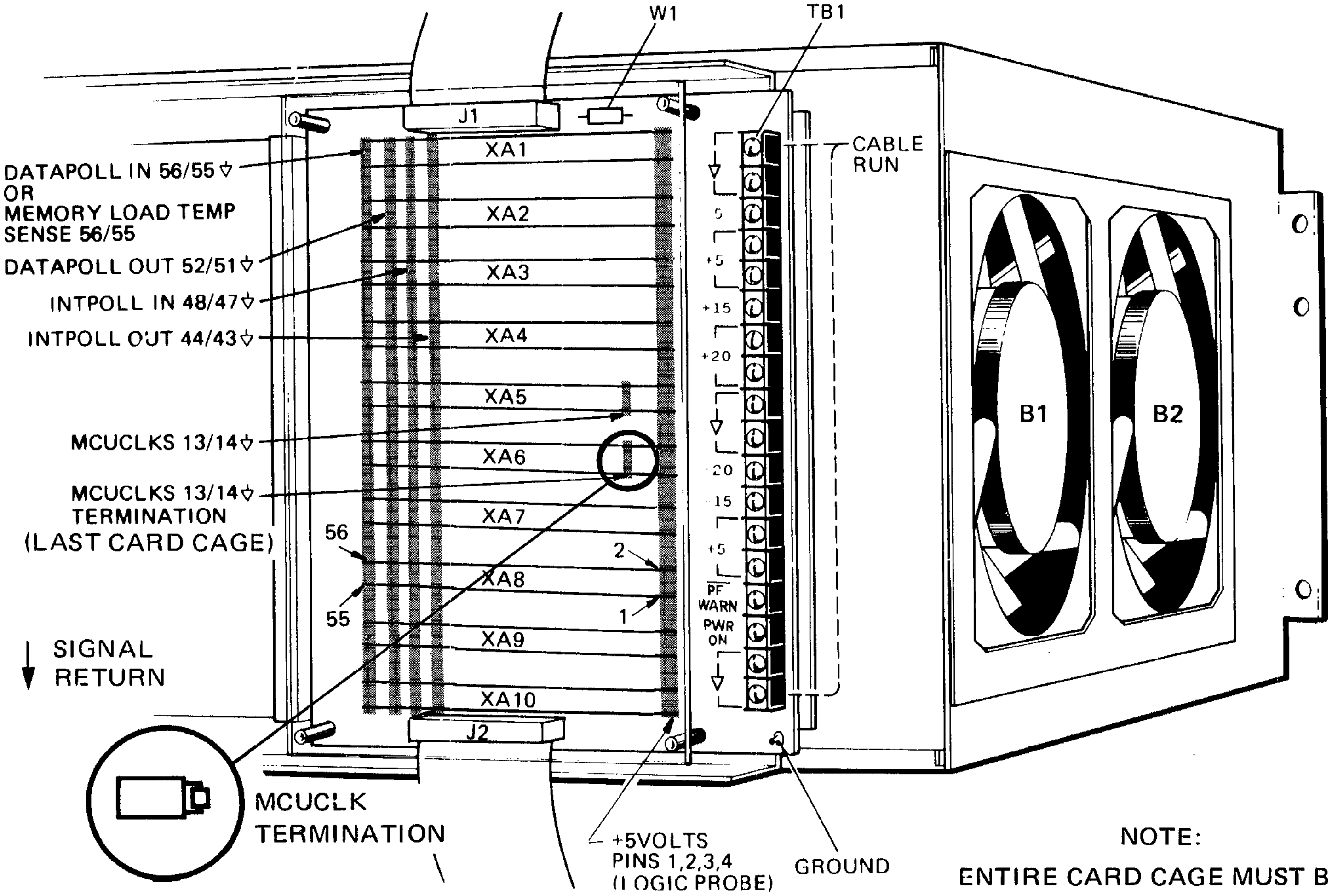
MEMORY MODULE BLOCK DIAGRAM
COREMEM-8



NOTE:
ENTIRE CARD CAGE MUST BE REMOVED TO REPLACE B1 OR B2 FANS.

51 Ω TERMINATION RESISTOR AND PLUG (USED ON CARD CAGE #2 ALWAYS AND CARD CAGE #3 IF SEL-CHAN OPTION IS INSTALLED)

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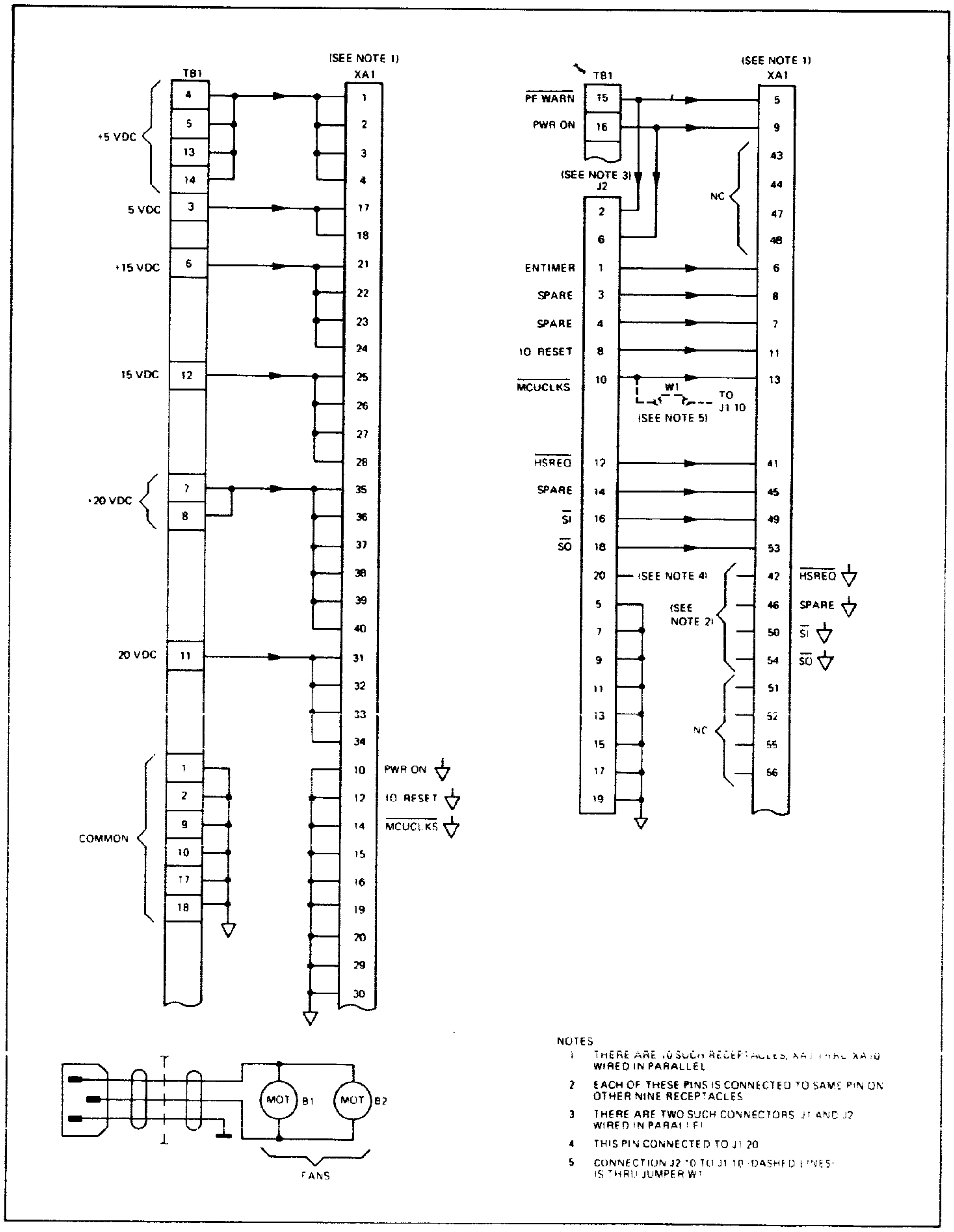
DATA AND INTERRUPT POLLING

POWER BUS DIAGRAM



NOTES

1 THERE ARE 10 SUCH RECEPTACLES, XA1 THRU XA10 WIRED IN PARALLEL

2 EACH OF THESE PINS IS CONNECTED TO SAME PIN ON OTHER NINE RECEPTACLES

3 THERE ARE TWO SUCH CONNECTORS J1 AND J2 WIRED IN PARALLEL

4 THIS PIN CONNECTED TO J1 20

5 CONNECTION J2 10 TO J1 10 (DASHED LINES) IS THRU JUMPER W1

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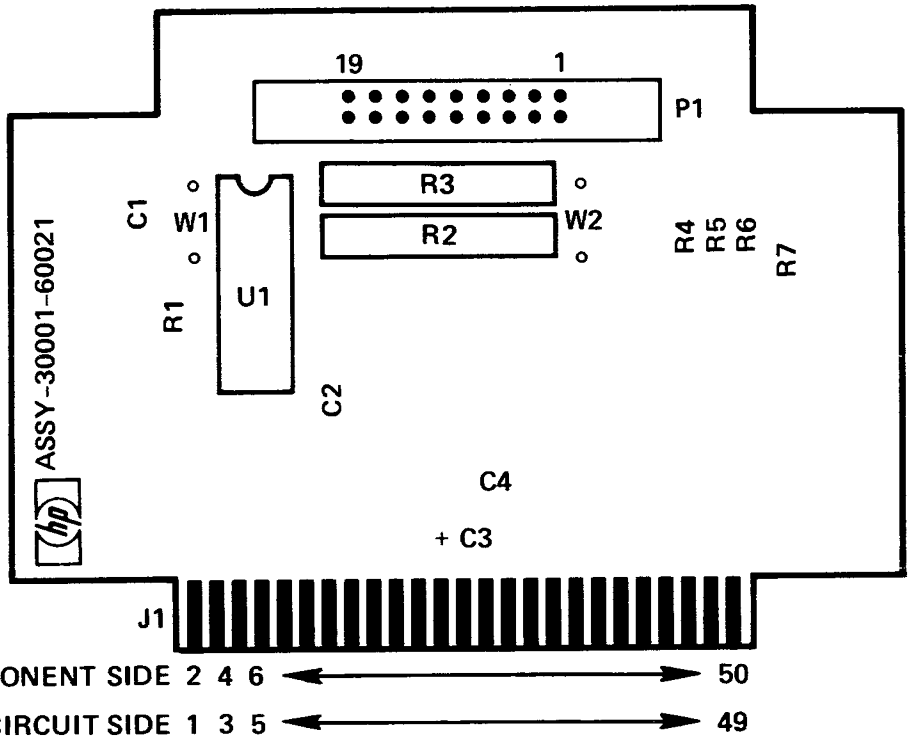
POWER BUS DIAGRAM

I.C. INDEX

U	1820-
1	0756



W1 = MASKRTN (REOVE IN BAY 1 ONLY)

W2 = MCU CLK TERM

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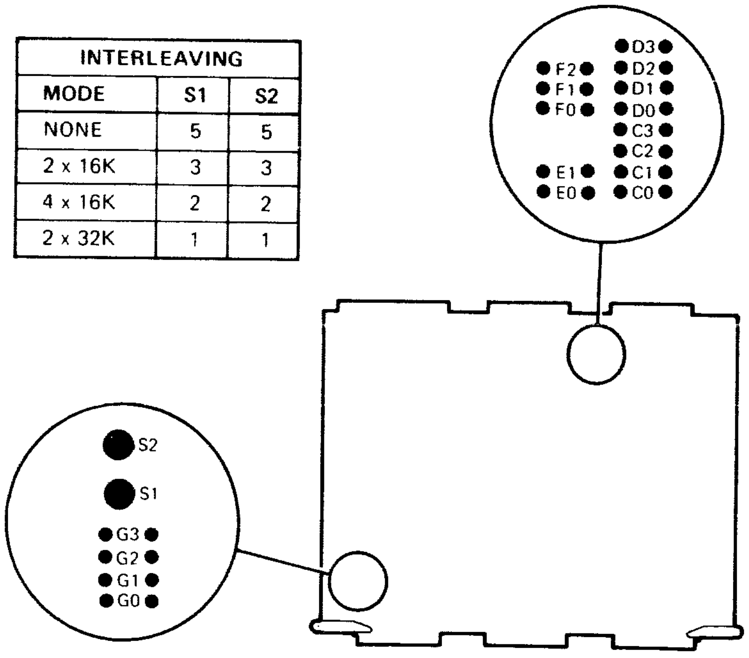
POWER BUS TERMINATOR PCA

JUMPER	POSITION	MODULE				FUNCTION
		0	1	2	3	
W3	F2	○ ○	○ ○	○ ○	●—●	ENABLE 02
W4	F1	○ ○	○ ○	●—●	●—●	ENABLE 01
W5	F0	○ ○	●—●	●—●	●—●	ENABLE 00
W4	E1	●—●	●—●	○ ○	○ ○	TO/FROM
W3	E0	●—●	○ ○	●—●	○ ○	TO/FROM
W1	D3	○ ○	○ ○	○ ○	●—●	READY 03
	D2	○ ○	○ ○	●—●	○ ○	READY 02
	D1	○ ○	●—●	○ ○	○ ○	READY 01
	D0	●—●	○ ○	○ ○	○ ○	READY 00
W2	C3	○ ○	○ ○	○ ○	●—●	$\overline{\text{ENABLE 03}}$
	C2	○ ○	○ ○	●—●	○ ○	$\overline{\text{ENABLE 02}}$
	C1	○ ○	●—●	○ ○	○ ○	$\overline{\text{ENABLE 01}}$
	C0	●—●	○ ○	○ ○	○ ○	$\overline{\text{ENABLE 00}}$

JUMPER	POSITION	MODULE CORE SIZE			
		8K	16K	24K	32K
W6	G3	●—●	○ ○	○ ○	○ ○
	G2	○ ○	●—●	●—●	●—●
W7	G1	●—●	●—●	○ ○	○ ○
	G0	○ ○	○ ○	●—●	●—●

INTERLEAVING		
MODE	S1	S2
NONE	5	5
2 x 16K	3	3
4 x 16K	2	2
2 x 32K	1	1



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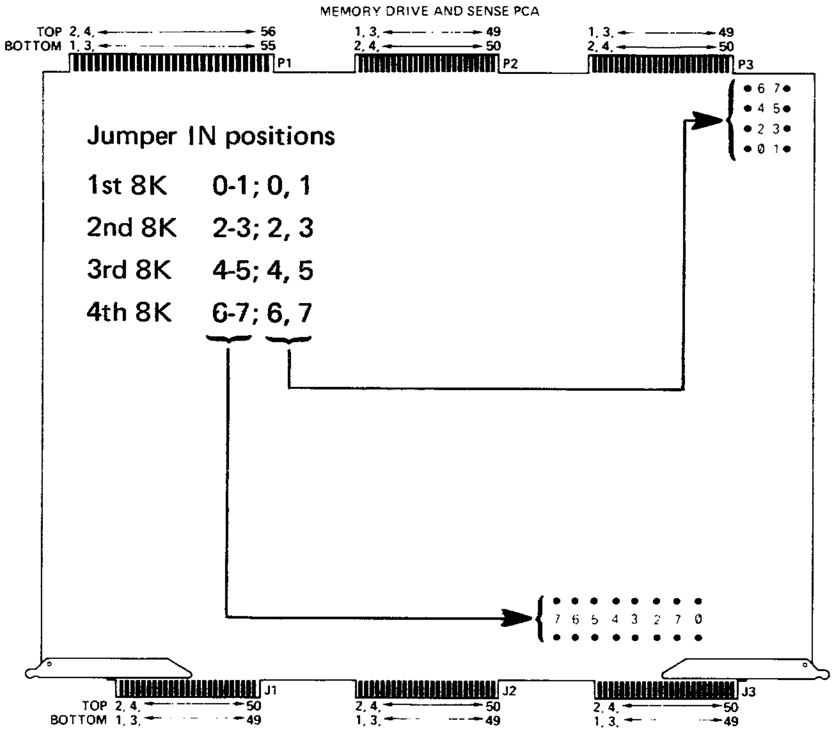
MEMORY DATA AND CONTROL PCA JUMPER LOCATIONS
AND INTERLEAVING SWITCH POSITIONS

PCA CARD CONFIGURATION



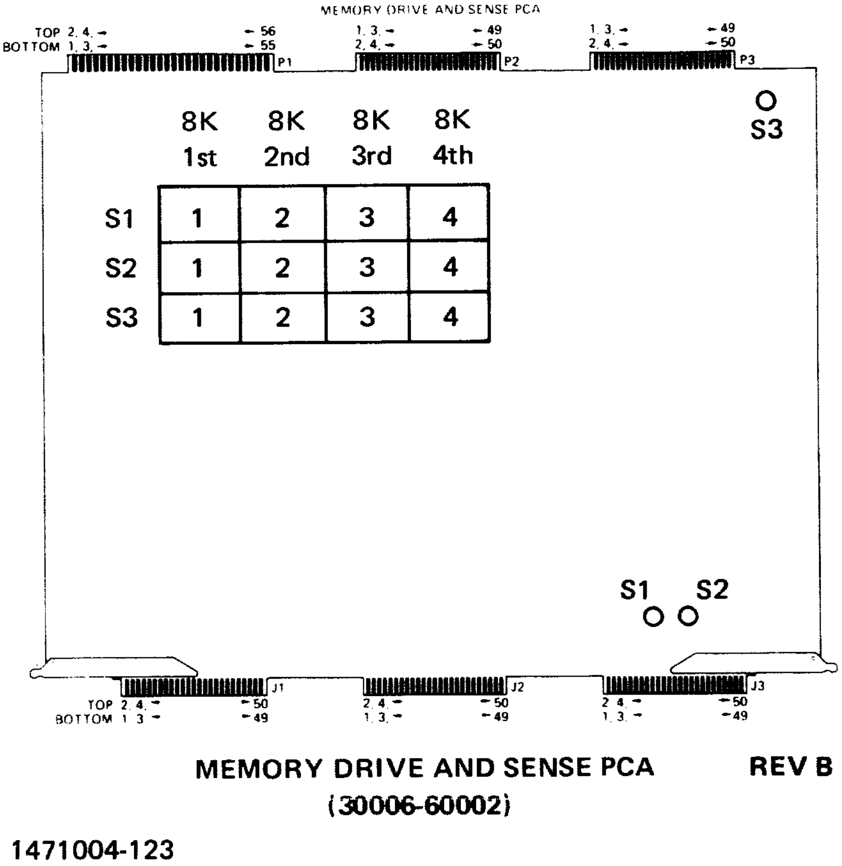
MEMORY DRIVE AND SENSE PCA REV A.
(30006-60002)

1471004-122

MEMORY DRIVE AND SENSE PCA (30006-60002) Rev. A

"S" Buss PCA switches must = Mem CTRL
TO UNINTERLEAVE:

1) Mem ctrl + data
2) IOP S1, 2, 3 Position #1, From 5
3) "S" BUS S, 1, 2, 3, 4, 5, 6 Position #5, From 1
4) Selector Reg S1, 2, 3 Position #1, From 5



	8K 1st	8K 2nd	8K 3rd	8K 4th
S1	1	2	3	4
S2	1	2	3	4
S3	1	2	3	4

MEMORY DRIVE AND SENSE PCA (30006-60002) Rev. B

INTERLEAVING MEMORY MODULES

Interleaving is a feature supported on all HP 3000 pre Series II systems with 64K words of memory.

Interleaving is a method which decreases the time that the CPU or I/O spends waiting for memory to complete a Read or Write cycle.

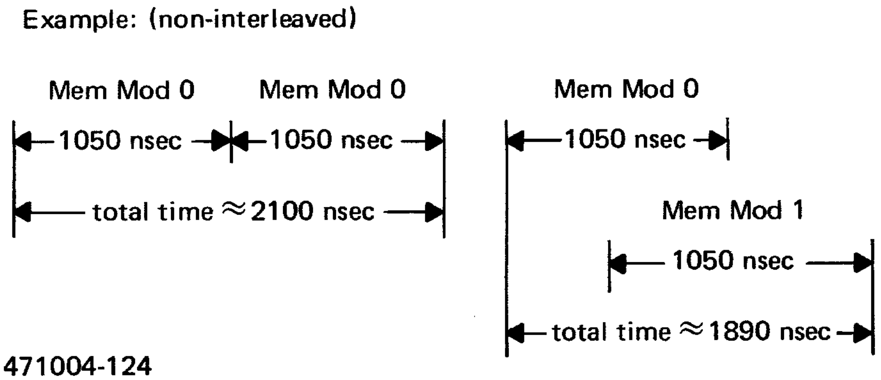
This represents about a 10% increase in speed when Reading sequential addesses with the memory interleaving feature.

Interleaving is accomplished by using specific bits in the Address word to select the proper cell to either Read or Write.

Bit 15 selects the Memory Module (0 or 1)

Bits 1 and 2 select the 8K core stack within the selected Memory Module.

Bit 0 selects every other cell within each 8K stack.



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MEMORY CYCLES, NON-INTERLEAVED vs INTERLEAVED

```
|---|-----------|-----------|-----------|-----------|-----------|
|  0|  1|  2|  3|  4|  5|  6|  7|  8|  9| 10| 11| 12| 13| 14| 15|
|---|-----------|-----------|-----------|-----------|-----------|

   MEMORY MODULE 0:

|  0|  0   0   -|  -   -   -|  -   -   -|  -   -   -|  -   -   0|
   (All even addresses      0 through  17776 octal)

|---|-----------|-----------|-----------|-----------|-----------|
|  1|  0   0   -|  -   -   -|  -   -   -|  -   -   -|  -   -   0|
   (All even addresses 100000 through 117776 octal)

|---|-----------|-----------|-----------|-----------|-----------|
|  0|  0   1   -|  -   -   -|  -   -   -|  -   -   -|  -   -   0|
   (All even addresses  20000 through  37776  octal)

|---|-----------|-----------|-----------|-----------|-----------|
|  1|  0   1   -|  -   -   -|  -   -   -|  -   -   -|  -   -   0|
   (All even addresses 120000 through 137776  octal)

|---|-----------|-----------|-----------|-----------|-----------|
|  0|  1   0   -|  -   -   -|  -   -   -|  -   -   -|  -   -   0|
   (All even addresses  40000 through  57776 octal)

|---|-----------|-----------|-----------|-----------|-----------|
|  1|  1   0   -|  -   -   -|  -   -   -|  -   -   -|  -   -   0|
   (All even addresses 140000 through 157776 octal)

|---|-----------|-----------|-----------|-----------|-----------|
|  0|  1   1   -|  -   -   -|  -   -   -|  -   -   -|  -   -   0|
   (All even addresses  60000 through  77776 octal)

|---|-----------|-----------|-----------|-----------|-----------|
|  1|  1   1   -|  -   -   -|  -   -   -|  -   -   -|  -   -   0|
   (All even addresses 160000 through 177776 octal)
```

471004-125, 1 of 2

2-64K INTERLEAVED MEMORY ADDRESSING, sheet 1 of 2

```
|---|-----------|-----------|-----------|-----------|-----------|
|  0|  1|  2|  3|  4|  5|  6|  7|  8|  9| 10| 11| 12| 13| 14| 15|
|---|-----------|-----------|-----------|-----------|-----------|

   MEMORY MODULE 1:

|---|-----------|-----------|-----------|-----------|-----------|
|  0|  0   0   -|  -   -   -|  -   -   -|  -   -   -|  -   -   1|
   (All odd addresses      1 through  17777 octal)

|---|-----------|-----------|-----------|-----------|-----------|
|  1|  0   0   -|  -   -   -|  -   -   -|  -   -   -|  -   -   1|
   (All odd addresses 100001 through 117777 octal)

|---|-----------|-----------|-----------|-----------|-----------|
|  0|  0   1   -|  -   -   -|  -   -   -|  -   -   -|  -   -   1|
   (All odd addresses  20001 through  37777 octal)

|---|-----------|-----------|-----------|-----------|-----------|
|  1|  0   1   -|  -   -   -|  -   -   -|  -   -   -|  -   -   1|
   (All odd addresses  12001 through 137777 octal)

|---|-----------|-----------|-----------|-----------|-----------|
|  0|  1   0   -|  -   -   -|  -   -   -|  -   -   -|  -   -   1|
   (All odd addresses  40001 through  57777 octal)

|---|-----------|-----------|-----------|-----------|-----------|
|  1|  1   0   -|  -   -   -|  -   -   -|  -   -   -|  -   -   1|
   (All odd addresses 140001 through 157777 octal)

|---|-----------|-----------|-----------|-----------|-----------|
|  0|  1   1   -|  -   -   -|  -   -   -|  -   -   -|  -   -   1|
   (All odd addresses  60001 through  77777 octal)

|---|-----------|-----------|-----------|-----------|-----------|
|  1|  1   1   -|  -   -   -|  -   -   -|  -   -   -|  -   -   1|
   (All odd addresses 160001 through 177777 octal)
```

471004-125, 2 of 2

2-64K INTERLEAVED MEMORY ADDRESSING, sheet 2 of 2

MICRO-DIAGNOSTIC FEATURE OF THE HP 3000 PRE SERIES II

All pre Series II ROM PCA´s have a built-in memory "Checkerboard" micro-diagnostic. This memory diagnostic can only be invoked, however, through the Maintenance panels.

This built-in diagnostic is very effective in analyzing most single bit memory failures.

Note that this diagnostic cannot be used to track down Memory Address failures.

To start the Memory checkerboard micro-diagnostic:

All switches should be down,

-Load RAR = %3704
-Depress CPU Reset then LOAD RAR switch
-Set B-Reg switch to lower limit memory address
-Depress LOAD FROM B-Reg switch.
-Set B-Reg switch to *upper limit memory address
-Depress LOAD FROM B-Reg switch
Micro-diag will run until a failure occurs

NOTE

Maximum upper limit memory address must not exceed %177776 for 64K words, or %137776 for 48K words.

MEMORY MICRO-DIAGNOSTIC TROUBLESHOOTING TIPS

Flag 1 will toggle ON for first pass, OFF for second pass.

Mem. Adr. Reg. (SP0) = (upper limit)
SP2 = (lower limit)
SP3 = (Failing Adr.)
MEM. DATA REG. (SP1) = MEM DATA (GOOD)
OPERAND Reg. = Mem Data (BAD)

IF NO INTERLEAVING THEN:

BIT´S 0 = 0 Means Mem Mod 0; = 1 means Mem Mod 1
BIT´S 1 and 2 = 00 Means Mem Stack 0
01 Means Mem Stack 1
12 Means Mem Stack 2
13 Means Mem Stack 3

IF 2-WAY INTERLEAVING THEN:

BIT´S 15 = 0 Means Memory Module 0
1 Means Memory Module 1

BIT´S 1 and 2 = 00 Means Mem Stack 0
01 Means Mem Stack 1
12 Means Mem Stack 2
13 Means Mem Stack 3

NOTE

If all of Module 0 or 1, but not both fails then suspect MEMORY LOAD BOARD for each module.

TO FIND A FAILING BIT:

LOAD MemAdr-Reg WITH FAILING ADDRESS. MOVE SINGLE-CYCLE REG SWITCH TO REG POSITION.
MOVE FREE RUN SWITCH TO SINGLE CYCLE POSITION.
HOLD DOWD DISPLAY SWITCH WHILE STEPPING SINGLE-CYCLE CLOCK SWITCH. CONTINUE STEPPING UNTIL THE DATA PATTERN IS READ FROM MEMROY AND IS ON THE CTL-BUS.
COMPARE WITH CONTENTS OF OPERAND-REG TO FIND THE FAILING BIT (INCLUDE DATA PARITY BIT).

IF DATA IS ALWAYS %177777 THEN SUSPECT JUMPERS on the memory stack boards.

DIAGNOSTIC STAND-ALONE

MEMORY PATTERNS S-A
30005A/6A

1. COLD LOAD DIAG FILE # FROM NON-CPU COLD LOAD TAPE
2. THIS DIAG WILL NOT WORK ON SYSTEMS WITH LESS THAN 64K WORDS WITHOUT DOING THE FOLLOWING DURING THE COLD LOAD:

SET BIT 0 = 1 FOR 32K OR 40K WORD SIZE
SET BIT 1 = 1 FOR 48K OR 56K WORD SIZE
SET BITS 2 - 15 = DIAG PROGRAM NUMBER

HALT0	(%30360)	SET B-REG TO INTERLEAVING FACTOR - PRESS RUN (0 = NONE 1 = 2WAY)
HALT1	(%30361)	SET B-REG TO LOW-LIMIT - PRESS RUN
HALT2	(%30362)	SET B-REG TO HIGH-LIMIT - PRESS RUN
HALT3	(%30363)	SET B-REG TO DIAG. OPTIONS - PRESS RUN

SWITCH REGISTER OPTIONS:

0	SELECT EXTERNAL REGISTER
3	SUPPRESS NON-FATAL ERROR HALTS (SCOPING)
6	SELECT CONFIGURATION SECTION
9	ADDRESS TEST
10	CHECKERBOARD TEST
11	SUPPRESS ERROR HALTS, REPORT VIA INTERNAL TABLES
15	HALT AT END OF CURRENT SECTION

HALT CODES

HALT Number	%0303XX (in CIR)	Segment Number*	Definition
n/a	n/a	06	Cold loader is finished; press RUN-HALT
01	61	22	Stand-alone relocating loader requests a program number; see "LOADING".
02	62	22	Stand-alone relocating loader requests a program number; see "LOADING".
00	60	20	Set the B-Register for the Interleave Factor; see step 1 of "Configuration Section".
01	61	20	Set B-Register to the low-limit; see step 2 of "Configuration Section".
02	62	20	Set B-Register to the high-limit; see step 3 of "Configuration Section".
03	63	20	Set B-Register for program options; see step 4 of "Configuration Section".
04	64	20	The low-limit was set to 0 (the CST pointer address) or to an address higher than the high- limit; press RUN-HALT to return to HALT 00 for Segment 20 (above).
05	65	20	A CPU fatal error has occurred; return to "LOADING".
06	66	20	The Checkerboard Test has found an error. See the failure absolute address in the RA Register, the correct data in the RB Register, and the bad data in the RC Register. Press RUN-HALT to resume.
07	67	20	The "table of errors" for the Checkerboard Test is full. To resume the program press RUN- HALT; further data will be displayed with HALT 06 (above).
10	70	20	The Address Test has found an error. See the good address in the RA Register and the bad address in the RB Register. Press RUN-HALT to resume the program.
11	71	20	A parity error in the program area has occurred (PE-Z, fatal). Return to "LOADING".

12	72	20	A parity error has occurred during a write operation (fatal). See the RA Register for the address that should have accepted the write data. Return to "LOADING".
16	76	20	The Address Test is finished; press RUN-HALT to resume the program.
17	77	20	The program has finished a complete run. Press RUN-HALT to run the program again.

* The segment number can be seen in the computer Status Register bits 8 through 15

PROGRAM ORGANIZATION

This test program is separated into two functional test sections: The Address Test and the Checkerboard Test. Either or both can be run. In any case, two runs should be made, once with an origin (starting address) in lower memory to test upper memory, and once with an origin in upper memory to test lower memory.

NOTE

> This program tests all locations between a low-limit and a high-limit except the area it reserves for itself (PB through Z).

ADDRESS TEST

First, the address of each location in the area to be tested is written in sequential order into those locations, from the low-limit through the high-limit. Then the addresses are read back in sequence from the high-limit through the low-limit, checking for errors.

Next, the addresses of each location are written in sequential order into those locations, from the high-limit through the low-limit. Finally, the addresses are read back in sequence from the low-limit through the high-limit, checking for errors.

CHECKERBOARD TEST

First, the Worst-Case Pattern shown in Figure COREMEM-11 is written into memory from the low-limit through the high-limit. Then these tests are made:

1. The first location is read and checked for error.
2. The pattern in that first location is complemented, written into the same location, then read back to check for error.
3. The pattern is changed to 0-000-000-000-000-001, written into that same location, the read back to check for error.
4. The pattern just used is complemented (1-111-111-111-111-110) written back into the same location, then read back to check for error.
5. Steps 3 and 4 are used again, but with the set bit shifted left one position (0-000-000-000-000-010 and 1-111-111-111-111-101).
6. Steps 3, 4, and 5 are repeated until all 16 bits have been tested.
7. Then the Worst-Case Pattern is restored to that first location, and steps 1 through 6 are used for the next location.

8. Steps 1 through 7 are repeated until all locations from low-limit through high-limit have been tested.

9. Next the NOT Worst-Case Pattern shown in Figure COREMEM-11 is written from low-limit through high-limit.

10. The first location is read and checked for error.

11. The complement of that NOT Worst-Case Pattern is written into the current location then read back to check for error.

12. The NOT Worst-Case Pattern is written back into the current location.

13. Steps 10 through 12 are repeated for each successive location until all in the test area have been tested.

```
                                         Absolute
                 Content                 Location
------------------------------------
| 0 000 101 110 011 000 | 005630 |    000000     (CST pointer)
| 0 000 000 000 000 000 | 000000 |    000001
~                       ~        ~
                                       through
~                       ~        ~
| 0 000 000 000 000 000 | 000000 |    000037
| 1 111 111 111 111 111 | 177777 |    000040
~                       ~        ~
                                       through
~                       ~        ~
| 1 111 111 111 111 111 | 177777 |    000137
| 0 000 000 000 000 000 | 000000 |    000140
~                       ~        ~
```

(cycle continues, alternating patterns at every 100_8 th address)

Worst-Case Pattern in Lower Memory

```
                                         Absolute
                 Content                 Location
------------------------------------
| 0 000 101 110 011 000 | 005630 |    000000     (CST pointer)
| 1 111 111 111 111 111 | 177777 |    000001
~                       ~        ~
                                       through
~                       ~        ~
| 1 111 111 111 111 111 | 177777 |    000037
| 0 000 000 000 000 000 | 000000 |    000040
~                       ~        ~
                                      through
~                       ~        ~
| 0 000 000 000 000 000 | 000000 |    000137
| 1 111 111 111 111 111 | 177777 |    000140
~                       ~        ~
```

(Cycle continues, alternating patterns at every 100_8 th address)

NOT Worst-Case Pattern in Lower Memory

471004-126

Figure COREMEM-11. CHECKERBOARD TEST PATTERNS

HP 3000 Pre Series II
All Serial Numbers

Simplified Troubleshooting of Memory Data Parity Errors Using Maintenance Panels

Set up maintenance panels, Old [New].

* Inhibit Timers Switch
* Enable MCU INT Freeze [Error Freeze] Switch
* Set Single-Cycle Register Display Switch to Register Position

CPU will freeze (Run Lamp On) when the MCU board detects a Mem Data Parity Error

* Set Clock Switch to Single-Cycle [Inhibit] position

Mem Adrs. Register (SP-0) contains the failing memory address, examine the address to determine the following:

If no interleaving, Bit 0 = 0 means Mem. Mod. 0
= 1 means Mem. Mod. 1
Bits 1 and 2 = 0 means Mem. Stack 0
= 1 means Mem. Stack 1
= 2 means Mem. Stack 2
= 3 means Mem. Stack 3

If 2-way interleaving, Bit 15 = 0 means Mem. Mod. 0
= 1 means Mem. Mod. 1
Bits 1 and 2 = 0 means Mem. Stack 0
= 1 means Mem. Stack 1
= 2 means Mem. Stack 2
= 3 means Mem. Stack 3

Always move failing PCA to another Mod. and another Stack and repeat to determine if problem follows the Mem. Stack or the Mem. Mod. before replacing.

*Mem. Mod. = Mem. Data and Control and Mem. Load PCA

INPUT-OUTPUT

INPUT-OUTPUT (General)

DIFFERENCES FROM SERIES II

Each device controller has four interrupt states:

1. Quiescent: Device is not attempting to request an interrupt.
2. Requesting: Device is requesting an interrupt, and will be serviced when the followong conditions are met:
    a. Mask bit is set for that device.

    b. External interrupts bit in CPU STATUS WORD is set.

    c. No higher priority device is being serviced.
3. Active: Device´s interrupt routine is correctly being executed on the I.C.S. The device´s Active flip-flop is set.
4. Pre-empted: Device´s Active flip-flop is set, but a higher priority interrupt has occurred which is now executing on the I.C.S.

SIO Start I/O

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	1	1	0	0	0	0	0	1	1	1				
												K			

Indicators:
- CCL = non responding device controller
- CCE = device ready
- CCG = device not ready

This is a privileged instruction.

The SIO instruction expects the absolute starting address of an I/O program to be on the TOS, and a device number to be in the stack at S-K. The instruction first checks if the device is ready by checking bit 0 of the device controller's Status register. If it is ready (bit = "1"), the TOS is stored into the first word location of the DRT entry for the device specified at S-K; an SIO command is then issued to the device controller to begin execution of its I/O program, the TOS is deleted, and the Condition Code is set to CCE. If the device is not ready (bit 0 of device status = "0"), the content of the device controller's Status register is pushed onto the stack and the Condition Code is set to CCG. If the device controller does not respond to the readiness test, the Condition Code is set to CCL and the instruction is terminated.

COND	LUTA	LABEL	RAR	W
UNC.	137	SIO	2233	0

```
  Device # := (S-K(8:15));
  If non-responding device
    controller then
  CC = CCL and terminate instruction;
Begin
  If SIO not ready then
    Begin
      S := S + 1;
      (S) := Device Status;
      CC := CCG;
    End else
    Begin
      (4*Device #) := (S);
    S := S-1
      Send SIO command to device;
      CC = CCE;
    End
End;
```

1471004-128

I/O AND INTERRUPT INSTRUCTIONS, sheet 1 of 5

RIO Read I/O

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	1	1	0	0	0	0	1	0	0	0				
												K			

Indicators:
CCL = non-responding device controller
CCE = device ready
CCG = device not ready
This is a privileged instruction.

This instruction expects a device number to be given in the stack at S−K. RIO first checks if the device is ready by checking bit 1 of the device controller's Status register. If it is ready (bit = "1"), the 16-bit direct data word from the device is pushed onto the stack and the Condition Code is set to CCE. If it is not ready (bit = "0"), the content of the device controller's Status register is pushed onto the stack and the Condition Code is set to CCG. If the device controller does not respond to the readiness test, the Condition Code is set to CCL and the instruction is terminated.

COND	LUTA	LABEL	RAR	W
UNC.	143	RIO	2252	0

```
  Device # := (S-K(8:15));
  If non-responding device
    controller then
  CC = CCL else
Begin
  If RIO not ready then
    Begin
      S := S + 1;
      (S) := Device Status;
      CC := CCG;
    End else;
    Begin
      S := S + 1;
      (S) := 16 bit word from device;
      CC := CCE;
    End;
End;
```

1471004-129

I/O AND INTERRUPT INSTRUCTIONS, sheet 2 of 5

WIO Write I/O

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	1	1	0	0	0	0	1	0	0	1				
												K			

Indicator:
CCL = non-responding device controller
CCE = device ready
CCG = device not ready
This is a privileged instruction.

This instruction assumes that the TOS contains a direct data word and expects a device number to be given in the stack at S-K. WIO first checks if the device is ready by checking bit 1 of the device controller's Status register. If it is ready (bit = "1"), the word is transmitted to the specified device and then deleted from the stack; the Condition Code is set to CCE. If it is not ready (bit = "0"), the content of the device controller's Status register is pushed onto the stack and the Condition Code is set to CCG. If the device controller does not respond to the readiness test, the Condition Code is set to CCL and the instruction is terminated.

COND	LUTA	LABEL	RAR	W
UNC.	147	WIO	2265	0

```
  Device # := (S-K(8:15));
  If non-responding device
    controller then
  CC = CCL else
Begin
  If WIO not ready then
    Begin
      S := S + 1;
      (S) := Device Status;
      CC := CCG;
    End else
    Begin
      16 bit word to device := (S)
      S = S - 1;
      CC := CCE;
    End;
End;
```

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I/O AND INTERRUPT INSTRUCTIONS, sheet 3 of 5

CIO Control I/O

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	1	1	0	0	0	0	1	0	1	1				
												K			

Indicators:
CCE = responding device controller
CCL = non-responding device controller
This is a privileged instruction.

This instruction assumes that the TOS contains a control word and expects a device number to be given in the stack at S–K. CIO transmits the TOS to the specified device controller, along with a CIO signal. If the device controller acknowledges receiving the word, the TOS is deleted and the Condition Code is set to CCE. If the device controller does not respond, the Condition Code is set to CCL and the instruction is terminated.

COND	LUTA	LABEL	RAR	W
UNC.	157	CIO	2306	0

```
  Device # := (S-K(8:15));
  If non-responding device
    controller then
  CC := CCL else
Begin
  16 bit control word to device := (S);
  S := S - 1;
  CC := CCE;
End;
```

SMSK Set mask

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	1	1	0	0	0	0	0	1	0	0				
												Not Used			

Indicators:
CCE if no error
CCL if error
This is a privileged instruction.

The SMSK instruction assumes that the TOS contains the mask word and transmits this word to all device controllers. Each "1" bit in the mask word sets each Mask flip-flop in the group of device controllers which are specifically wired to be controlled by that bit. Each "0" bit in the mask clears each Mask flip-flop in its group. If there is an I/O error (no acknowledgement), it means that the external interrupt system is in an unknown state. In this case, the SMSK instruction disables the external interrupt system (clears Status bit 1 to "0"), set CCL Condition Code, and leaves the mask on the TOS. If there is no I/O error, the SMSK instruction deletes the mask from the stack and sets the Condition Code to CCE.

COND	LUTA	LABEL	RAR	W
UNC.	123	SMSK	2332	1

```
16 bit mask word to all device
  controllers := (S);
if I/O error then CC := CCL else
  Begin
    MASKREG := (S)
    S := S - 1;
    CC := CCE;
  End;
```

TIO Test I/O

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	1	1	0	0	0	0	1	0	1	0				
												K			

Indicators:
CCE = responding device controller
CCL = non-responding device controller
This is a privileged instruction.

This instruction expects a device number to be given in the stack at S-K. TIO obtains a copy of the device status word from the device controller, pushes it onto the stack, and sets the Condition Code to CCE. If the device controller does not respond, the Condition Code is set to CCL and the instruction is terminated.

```
  Device # := (S-K(8:15));
  If non-responding device
    controller then
  CC := CCL else
Begin
  S := S + 1;
  (S) := Device Status;
  CC := CCE;
End;
```

COND	LUTA	LABEL	RAR	W
UNC.	153	TIO	2300	0

SIN Set interrupt

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	1	1	0	0	0	0	1	1	1	0				
												K			

Indicators:
CCE = responding device controller
CCL = non-responding device controller
This is a privileged instruction.

This instruction expects a device number to be given in the stack at S-K. SII sets the Interrupt Request flip-flop in the specified device controller and sets the Condition Code to CCE. If the device controller does not respond, the Condition Code is set to CCL and the instruction is terminated.

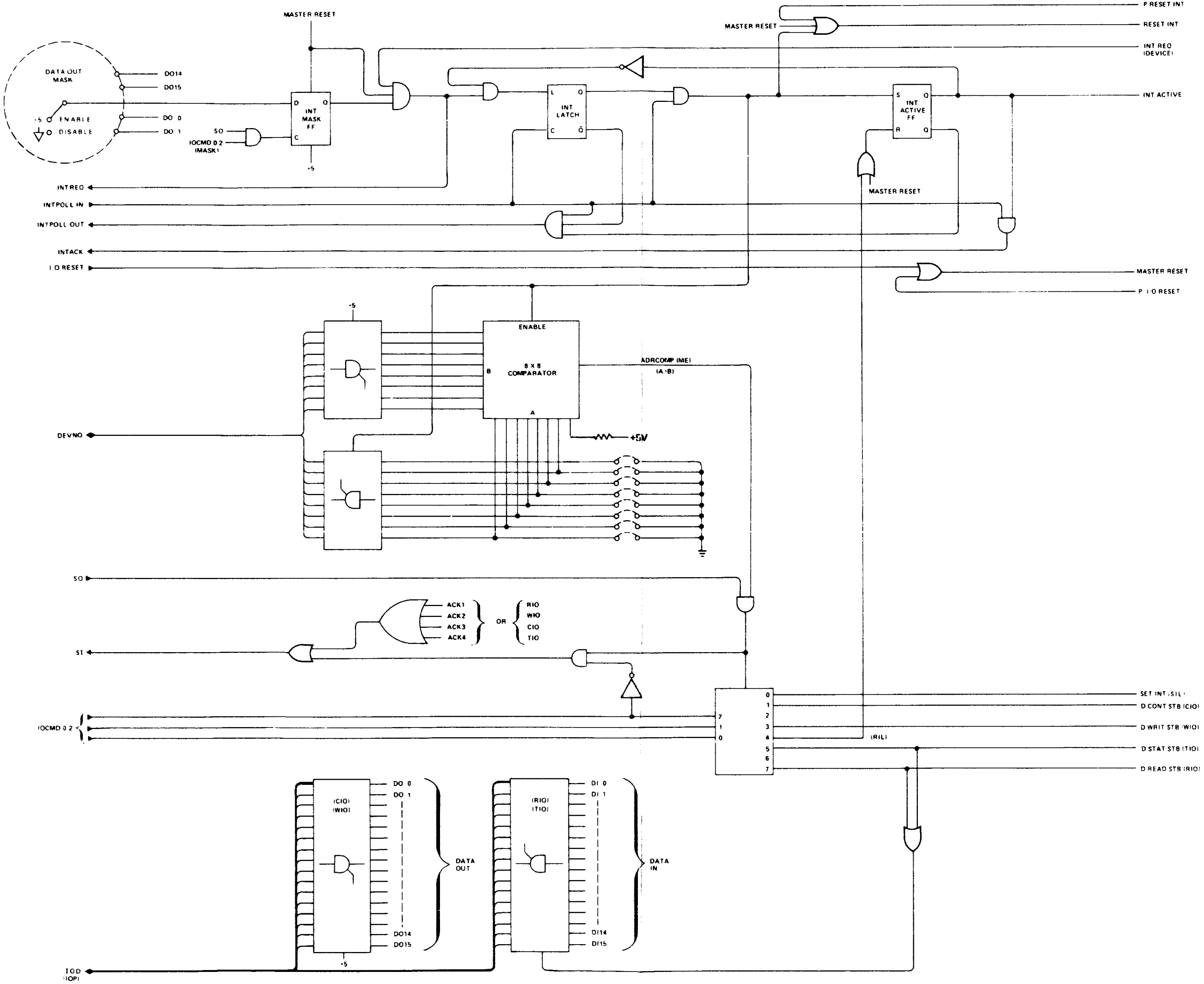
```
Device # := (S-K(8:15));
If non-responding device
  controller then
CC := CCL and terminate instruction else
CC := CCE and set device interrupts
```

COND	LUTA	LABEL	RAR	W
UNC.	173	SIN	2323	0

COMMAND	$\overline{\text{IOCMD}}$			DESCRIPTION
	$\overline{00}$	$\overline{01}$	$\overline{02}$	
CIO	1	1	0	Control I/O. Transfers a 16-bit control word from the computer system to the interface PCA (see figure 2-1).
RESET INT **(Only used by micro code)**	0	1	1	Reset Interrupt. Clears the interface PCA interrupt active condition but does not clear the conditional logic that specifies the cause of an interrupt request.
RIO	0	0	0	Read I/O. Transfers a 16-bit data word from the interface PCA to the computer system.
SIN	1	1	1	Set Interrupt. Sets the I/O system interrupt and causes an interrupt request to be initiated.
SIO	1	0	1	Start I/O. Initiates a microprogram routine that allows the multiplexer channel to control operation of the interface PCA.
SMSK	0	0	1	Set Mask. Transfers a mask word from top of stack (TOS) to all interface PCA's.
TIO	0	1	0	Test I/O. Transfers a 16-bit status word from the interface PCA to the computer system (see figures 2-2, 2-3, and 2-4).
WIO	1	0	0	Write I/O. Transfers a 16-bit data word from the computer system to the interface PCA.

1471004-133

DIRECT I/O COMMAND CODES TABLE



1471004-134

DIRECT ONLY BUS LOGIC

INOUT-8

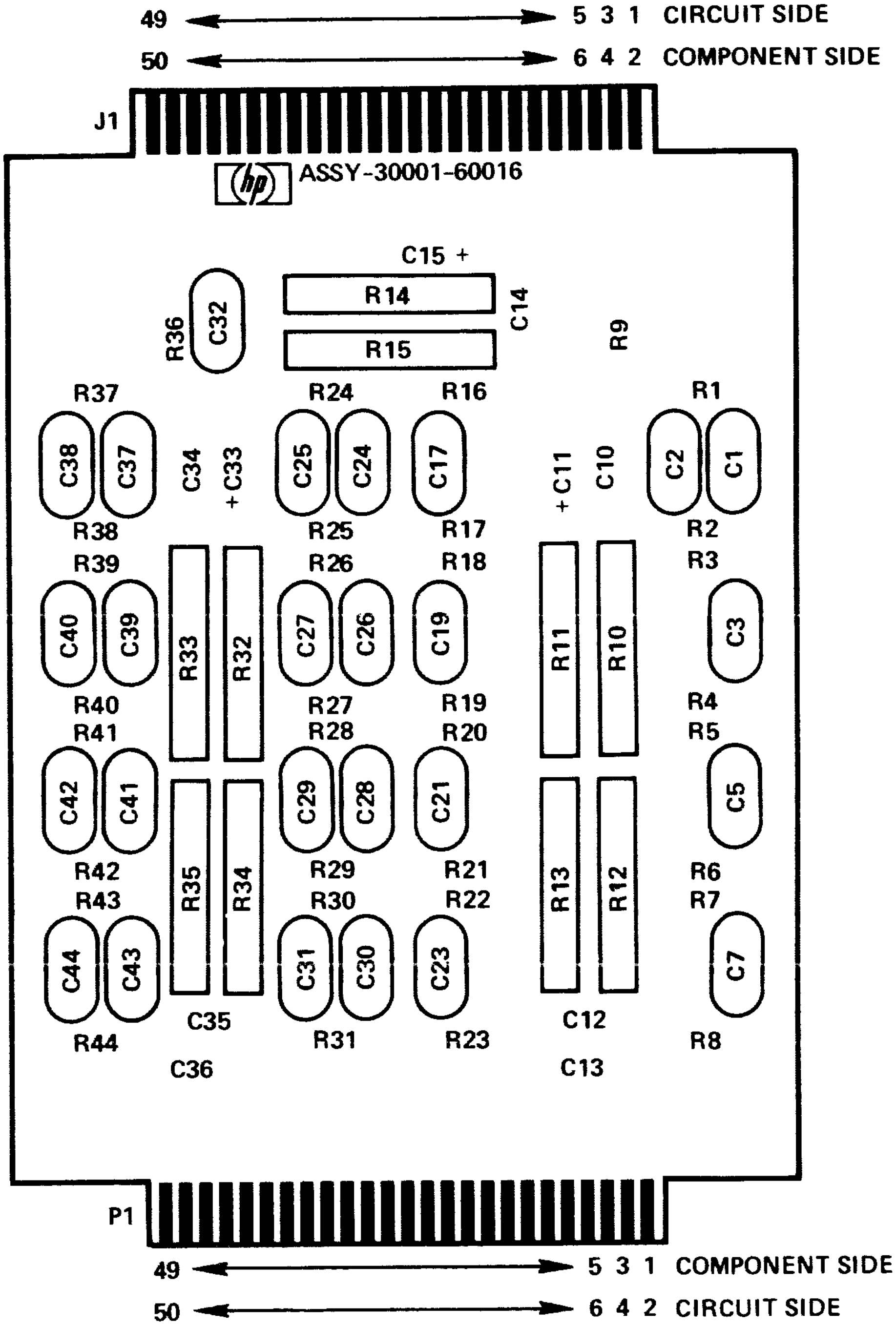
IOP DATA BUS

SIGNALS

Connector P3 (TOP)	Connector P3 (BOTTOM)
2 IOD PE	1 IODPRTY
4 IOCMD 00	3 COM
6 IOCMD 01	5 IOCMD 02
8 DEVNO 00	7 COM
10 COM	9 DEVNO 01
12 DEVNO 03	11 DEVNO 02
14 DEVNO 04	13 COM
16 COM	15 DEVNO 05
18 DEVNO 07	17 DEVNO 06
20 IOD 00	19 COM
22 COM	21 IOD 01
24 IOD 03	23 IOD 02
26 IOD 04	25 COM
28 COM	27 IOD 05
30 IOD 07	29 IOD 06
32 IOD 08	31 COM
34 COM	33 IOD 09
36 IOD 11	35 IOD 10
38 IOD 12	37 COM
40 COM	39 IOD 13
42 IOD 15	41 IOD 14
44 INTREQ	43 COM
46 COM	45 UNUSED
48 UNUSED	47 UNUSED
50 INTACK	49 COM

IC INDEX

U	1820-
No I.C.s	



1471004-135

IOP BUS TERMINATOR PCA (30001-60016)

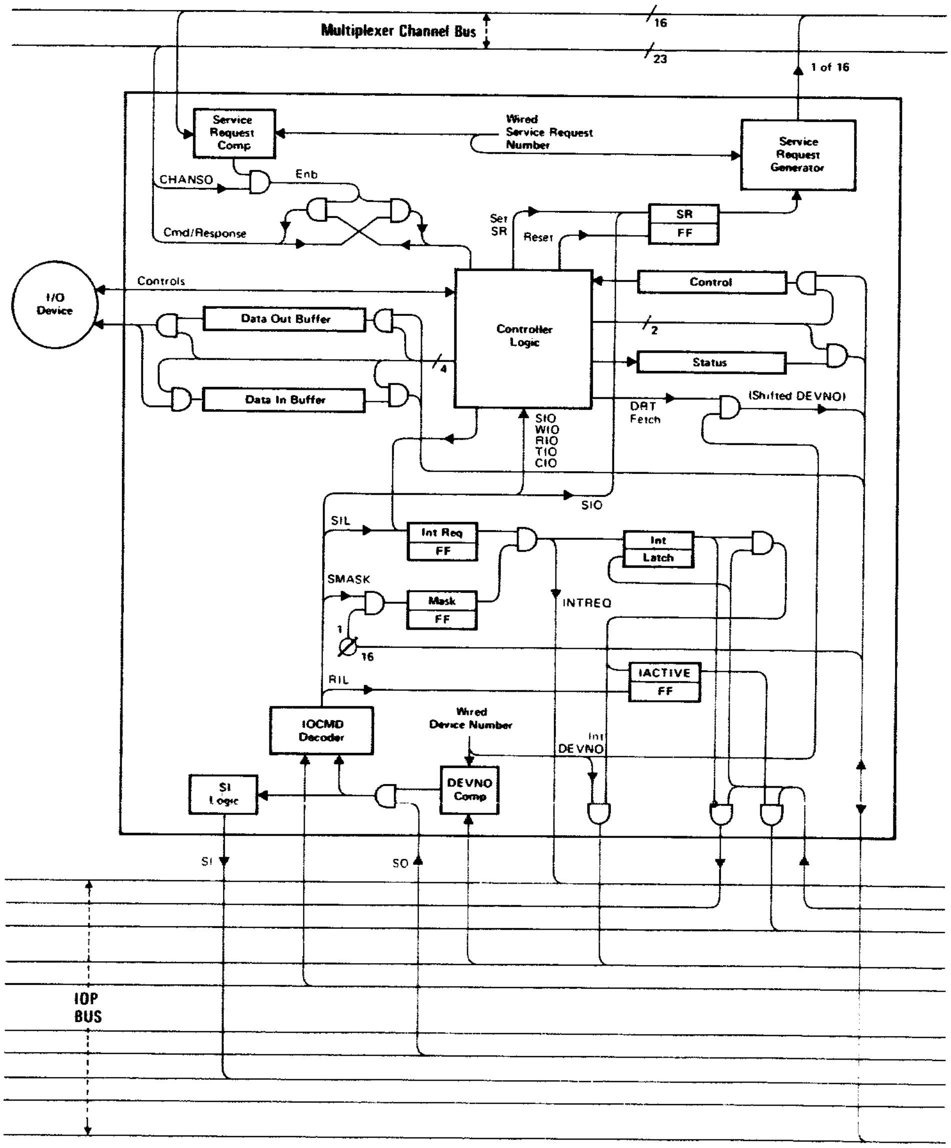
SIO MULTIPLEXER 30035A

DIFFERENCES FROM SERIES II

No Bank Bits
Less Error Checking
Slower operating (one more clock necessary)
DEVNO only used for diagnostic (set to 127)

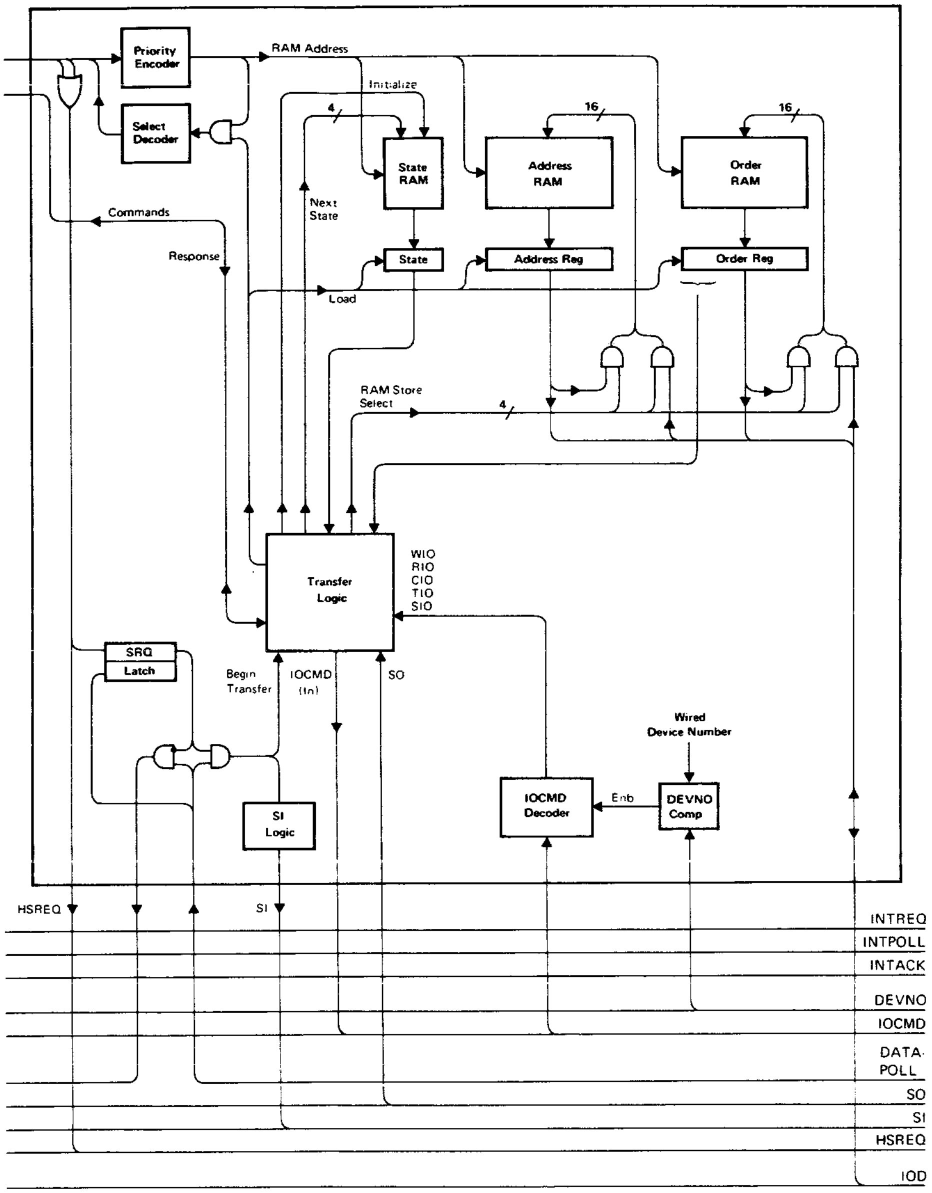
NOTE

> All SIO type device controllers on the MUX bus require DEVNO parity bit configured for odd parity.



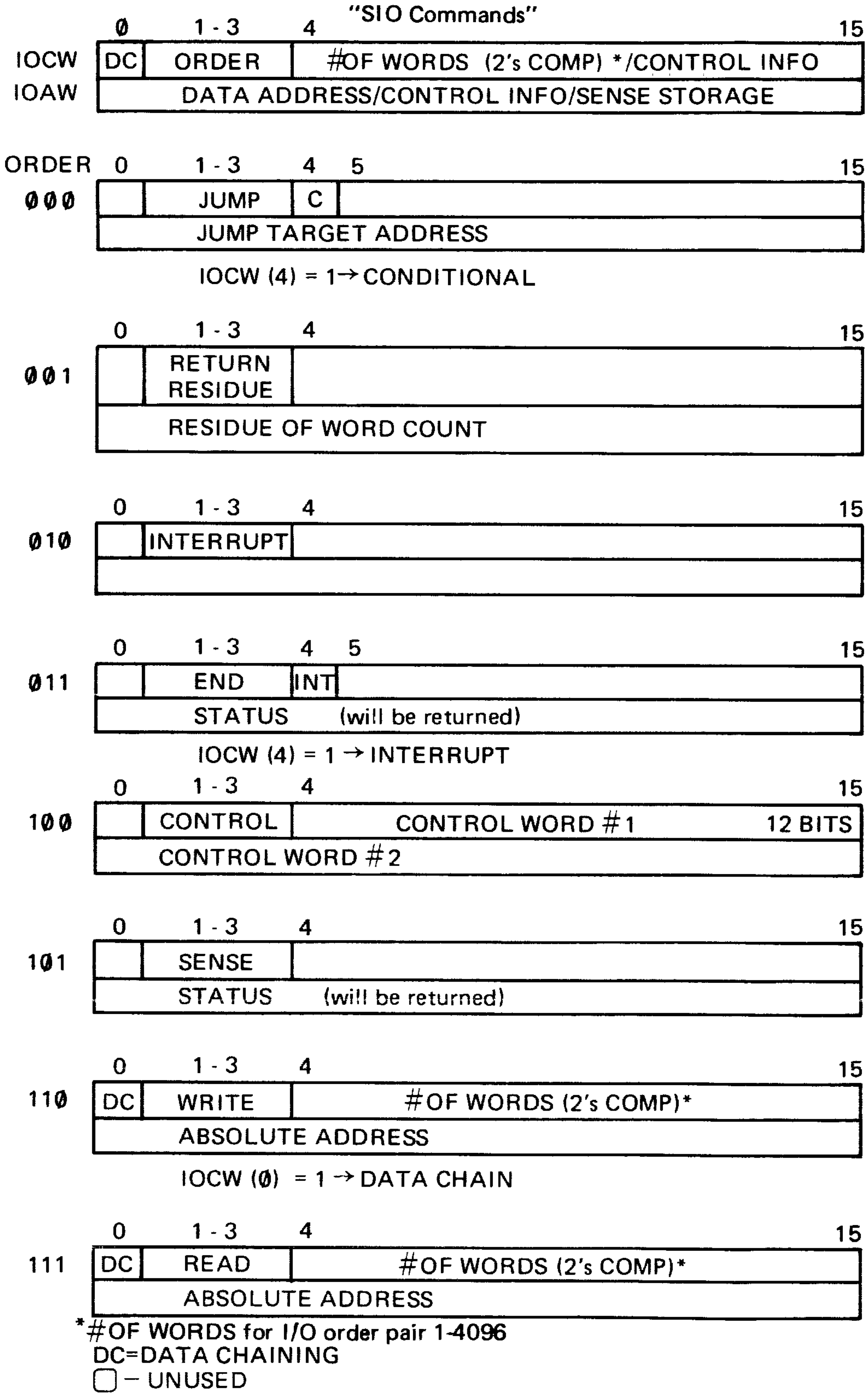
1471004-136

MULTIPLEXER CHANNEL BLOCK DIAGRAM, sheet 1 of 2



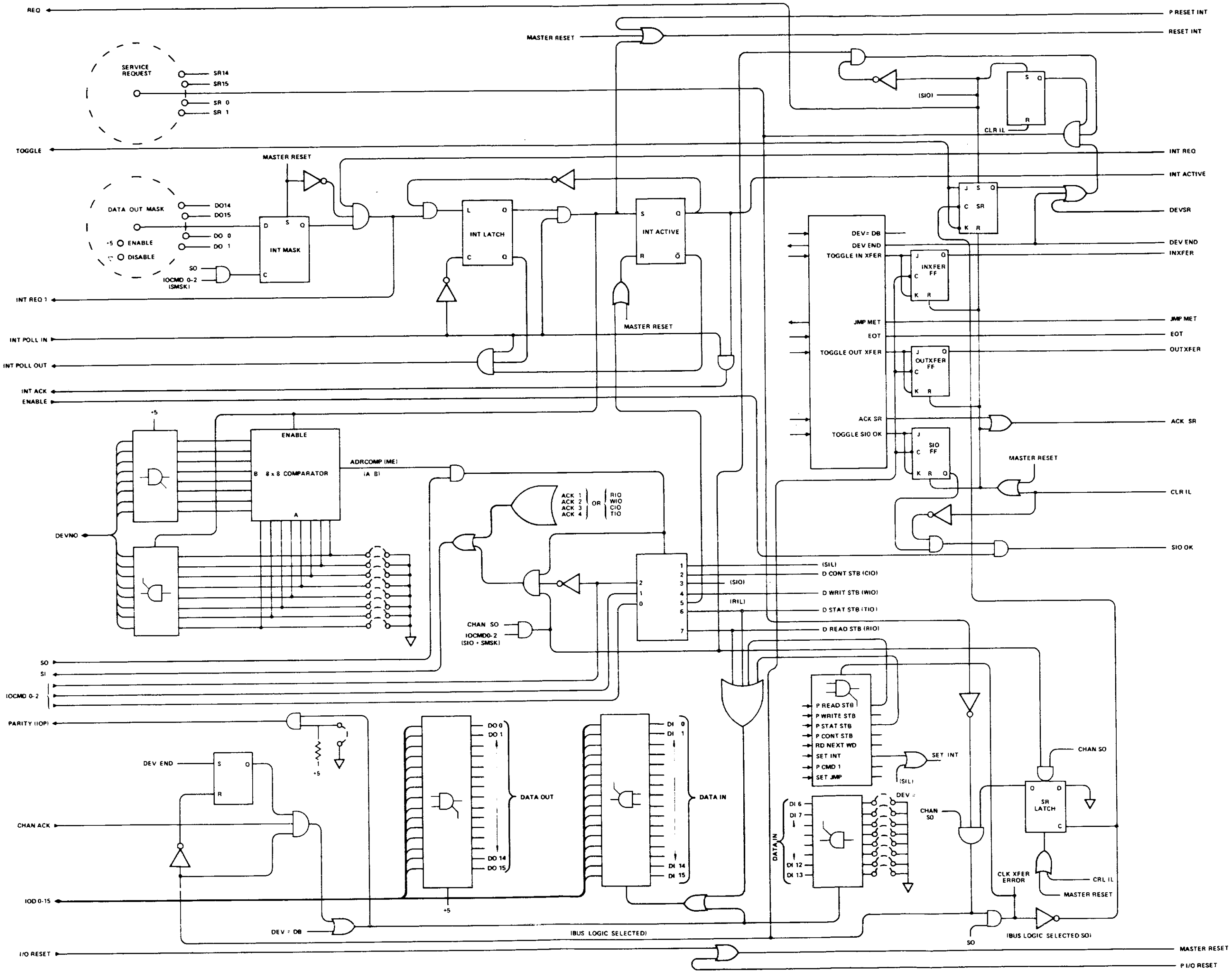
1471004-137

MULTIPLEXER CHANNEL BLOCK DIAGRAM, sheet 2 of 2



1471004-138

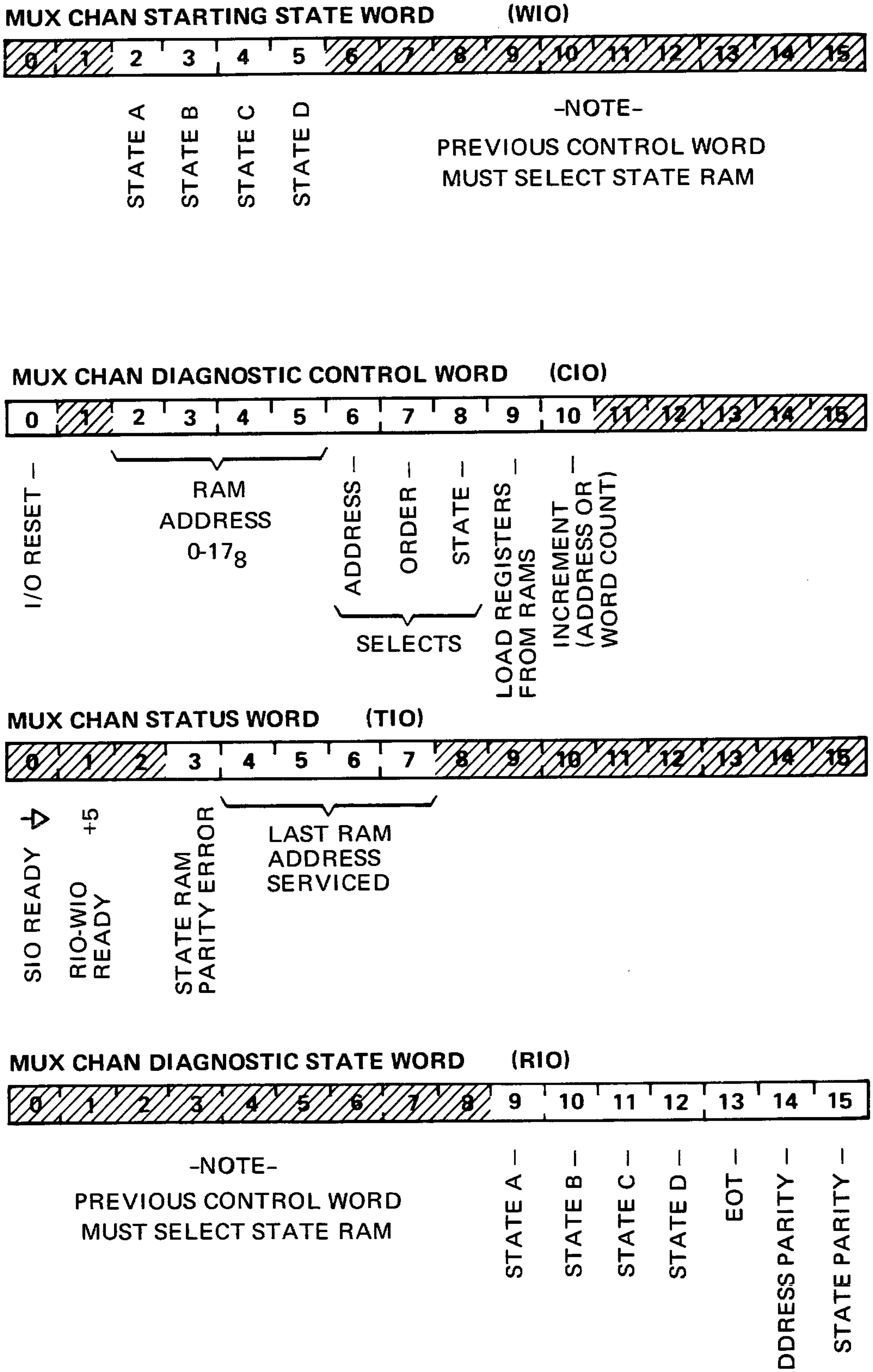
MULTIPLEXER CHANNEL I/O ORDERS



SIO BUS LOGIC
SIOMUX-5

SIO MUX BUS
SIGNALS

Connector P2 (Top)	Connector P2 (Bottom)
1 CHAN SO	2 COM
3 SR CLOCK	4 COM
5 DEV END	6 COM
7 ACK SR	8 COM
9 CHAN ACK	10 COM
11 DEVNO DB	12 SIO ENABLE
13 EOT	14 JMP MET
15 COM	16 TOGGLE INXFER
17 TOGGLE SR	18 TOGGLE OUTXFER
19 TOGGLE SIO OK	20 COM
21 XFER ERROR	22 REQ
23 COM	24 SR 15
25 SR 14	26 SR 13
27 SR 12	28 SR 11
29 SR 10	30 COM
31 SR 9	32 SR 8
33 SR 7	34 SR 6
35 SR 5	36 COM
37 SR 4	38 SR 3
39 SR 2	40 SR 1
41 SR 0	42 COM
43 P CND 1	44 SET JMP
45 P STATUS STB	46 P CONT STB
47 RD NEXT WD	48 P WRITE STBRD NEXT WD
49 SET INT	50 P READ STB



1471004-140

MULTIPLEXER CHANNEL DIAGNOSTIC WORDS

SIO MULTIPLEXER

DIAGNOSTIC STAND-ALONE

MULTIPLEXED CHANNEL S-A
30035A

1. COLD LOAD DIAG FILE # FROM NON-CPU COLD LOAD TAPE
   D01 30035A MPX CHANNEL TEXT (HP32322A.NN.N)
2. Q01 ENTER MPX DEVICE #? XX ((DRT # (DECIMAL)))
3. P01 SELECT OPTIONS ((SET SW REG THEN RUN))

SWITCH REGISTER OPTIONS:

0	ENTER CONFIGURATION ON NEXT CYCLE
6	OMIT OR ABORT AREG
7	OMIT OR ABORT OREG
8	PRINT END OF SECTION MSG AND HALT
9	LOOP ON CURRENT SECTION
10	SUPPRESS NON-ERROR MSG´S
11	SUPPRESS ALL MSG´S
12	HALT AFTER COMPLETE CYCLE
13	LOOP ON CURRENT STEP
14	SUPPRESS ERROR HALTS
15	PRINT END OF STEP MSG AND HALT

NOTE

DEVNO on Multiplexer are only for diagnostic purposes. (127) Multiplexer does not interrupt the CPU.

SELECTOR CHANNEL 30030A/B
and
SELECTOR CHANNEL MAINTENANCE BOARD 30033A

DIFFERENCES FROM SERIES II

Most HP 3000CX and pre CX systems have two Selector Channel capability even though only one selector channel is supported.

All HP 3000 Series I have only one Selector Channel capability.

NOTE

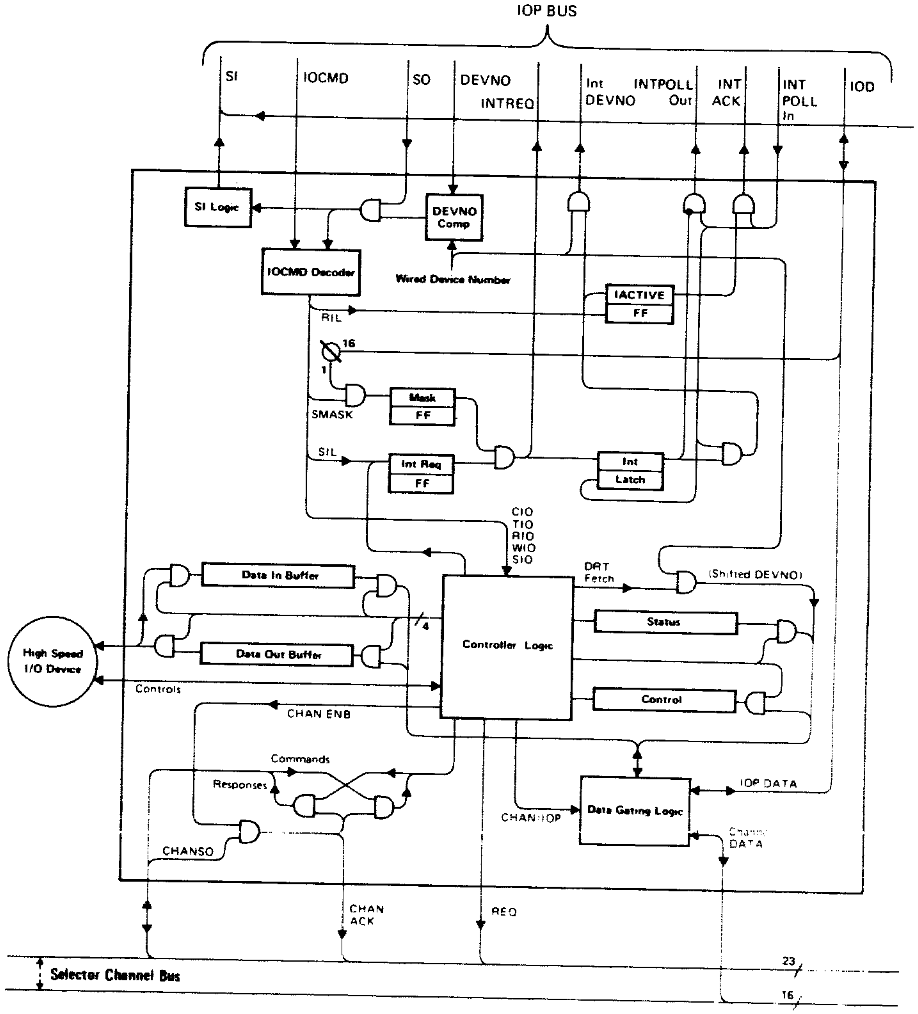
> Device controllers on the Sel-Chan do not require DEVNO parity bit.

Differences between the HP 30030A used in all HP 3000 pre Series II systems and the HP 30030B used in all HP 3000 Series II systems include:

-No bank bits (0 & 1)
-More Diagnostic capability on the HP 30030A Port Controller PCA

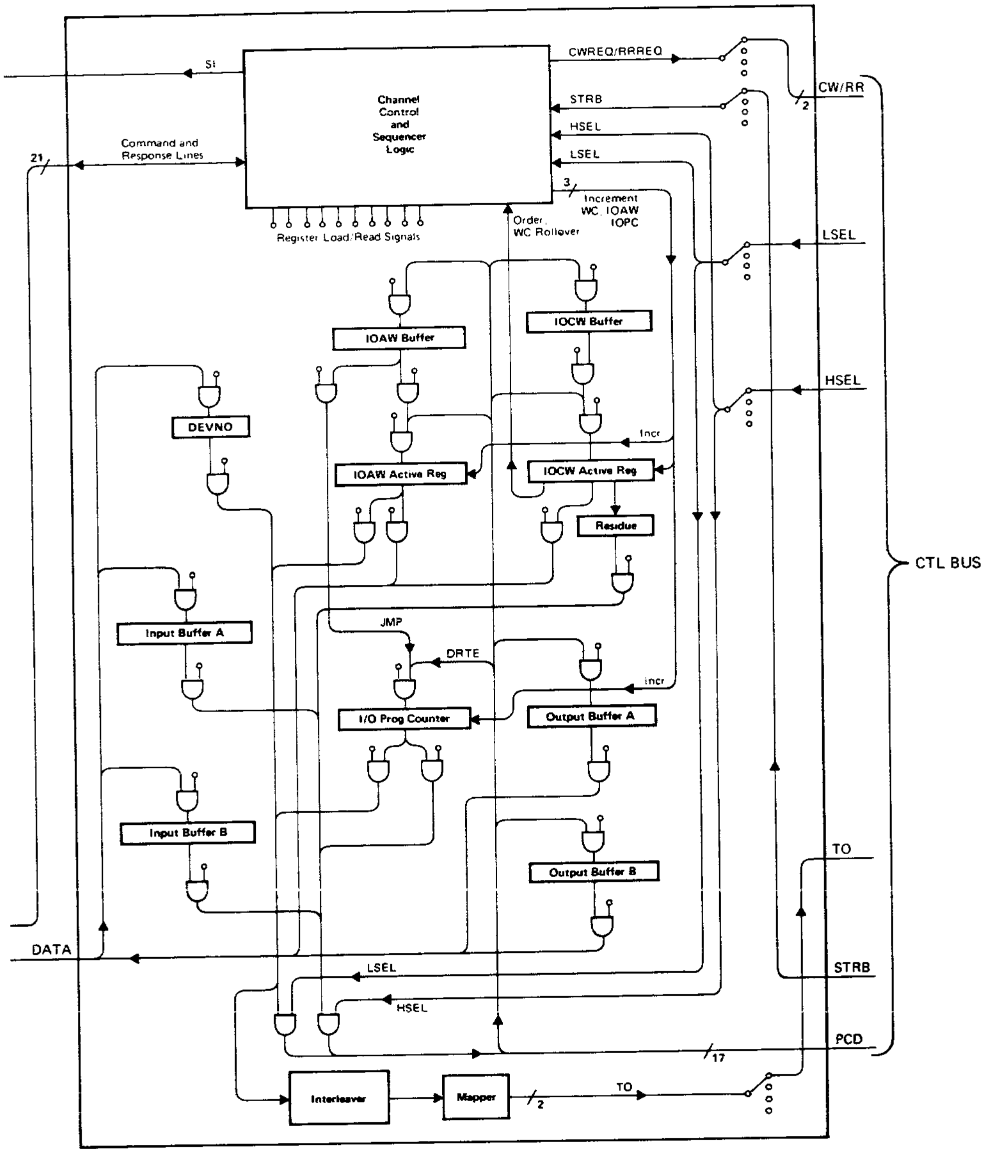
It should be noted that both HP 30030A and HP 30030B will both function properly in any HP 3000 pre Series II system. In other words, the HP 30030B is downward compatible. Also, any combination of HP 30030A or HP 30030B will work in any HP 3000 pre Series II system.

It should be noted that a non-responding module will time-out in the Port Controller logic. This error is treated as a Transfer Error in which the currently operating device controller will interrupt the CPU and the operation will be retried under MPE.



1471004-142

HIGH-SPEED DEVICE CONTROLLER



1471004-143

SELECTOR CHANNEL

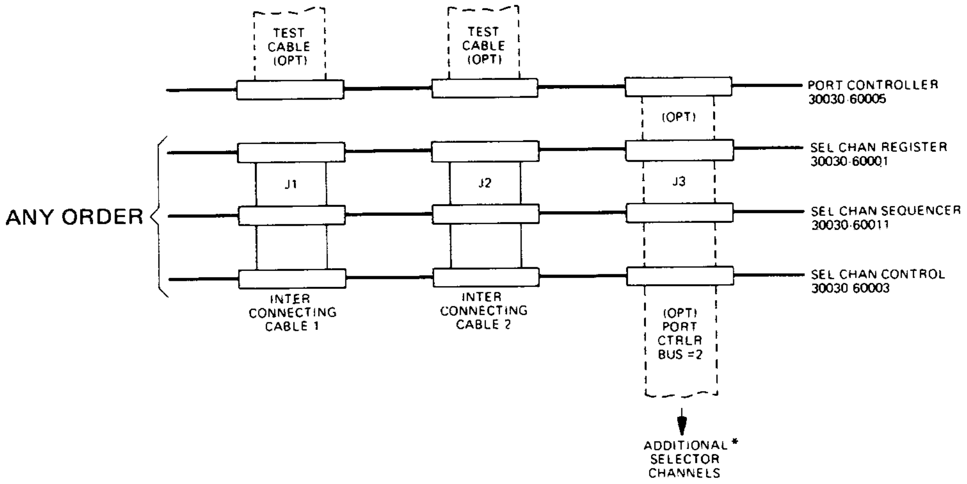
SELECTOR CHANNEL BUS

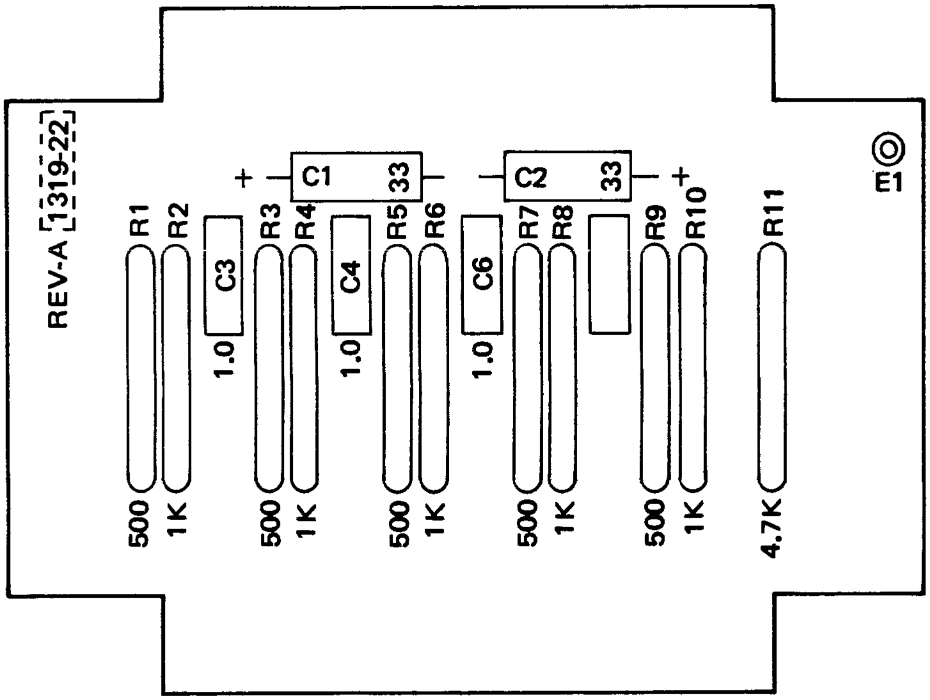
SIGNALS

Connector P2 (Top)	Connector P2 (Bottom)
1 CHAN SO	2 COM
3 SR CLOCK	4 COM
5 DEV END	6 COM
7 ACK SR	8 COM
9 CHAN ACK	10 COM
11 DEVNO DB (Not Used)	12 SIO ENABLE
13 EOT	14 JMP MET
15 COM	16 TOGGLE INXFER
17 CHAN SR	18 TOGGLE OUTXFER
19 TOGGLE SIO OK	20 COM
21 XFER ERROR	22 REQ
23 COM	24 SR 15
25 SR 14	26 SR 13
27 SR 12	28 SR 11
29 SR 10	30 COM
31 SR 9	32 SR 8
33 SR 7	34 SR 6
35 SR 5	36 COM
37 SR 4	38 SR 3
39 SR 2	40 SR 1
41 SR 0	42 COM
43 P CMD 1	44 SET JMP
45 P STATUS STB	46 P CONT STB
47 RD NEXT WD	48 P WRITE STB
49 SET INT	50 P READ STB

CABLE CONFIGURATION

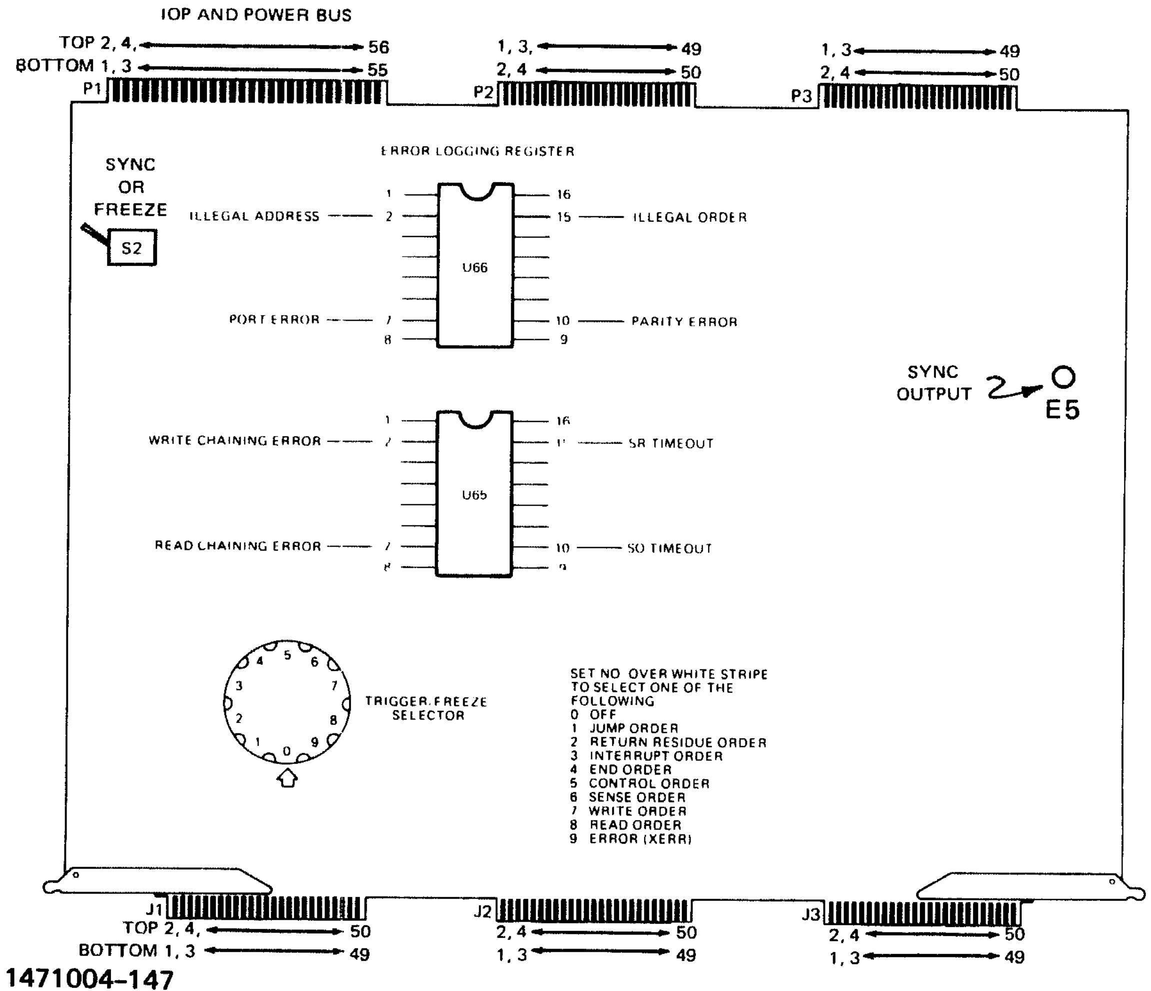
FRONT VIEW



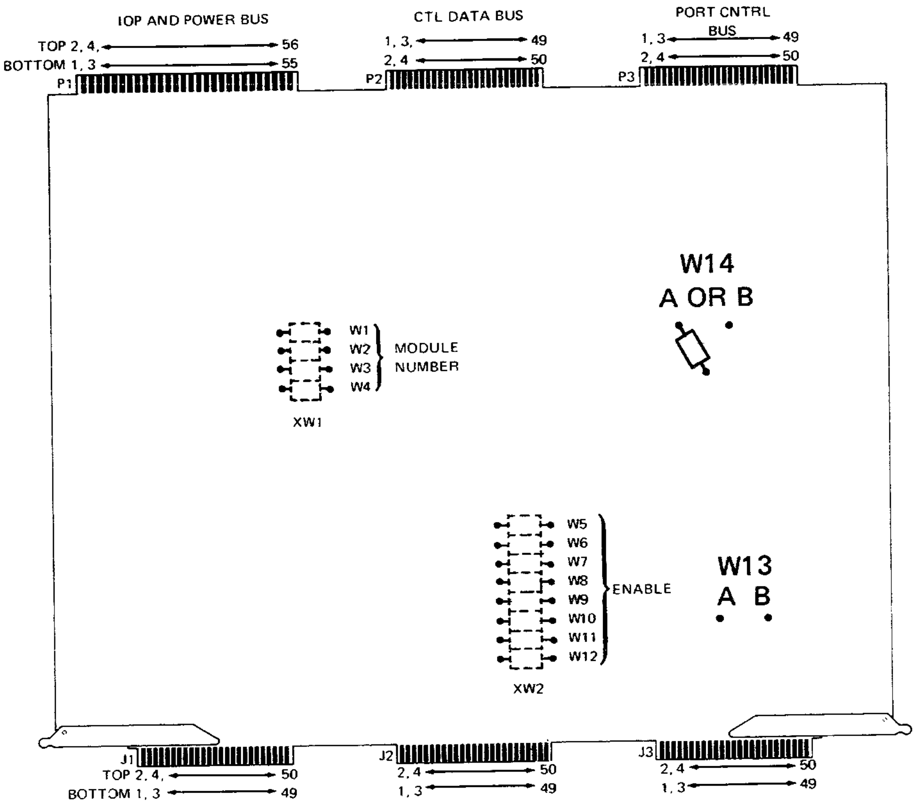


1471004-144

SELECTOR CHANNEL BUS TERMINATOR PCA



SELECTOR CHANNEL CONTROLLER 30030-60003



PORT CONTROLLER
30030-60005

Port Controller Module Number

Module #		2	3	4*	5	6
Module #	W1	O	I	O	I	I
	W2	I	O	I	O	I
	W3	O	O	I	I	O
	W4	I	I	O	O	O
ENABLE	W5	I	O	O	O	O
	W6	O	I	O	O	O
	W7	O	O	I	O	O
	W8	O	O	O	I	O
	W9	O	I	I	I	I
	W10	O	O	I	I	I
	W11	O	O	O	I	I
	W12	O	O	O	O	I

*Only number supported by General Systems Division.

1471004-145

PORT CONTROLLER MODULE NUMBER

	Module #	2	3	4*	5	6
Module #	W1	0	1	0	1	1
	W2	1	0	1	0	1
	W3	0	0	1	1	0
	W4	1	1	0	0	0
ENABLE	W5	1	0	0	0	0
	W6	0	1	0	0	0
	W7	0	0	1	0	0
	W8	0	0	0	1	0
	W9	0	1	1	1	1
	W10	0	0	1	1	1
	W11	0	0	0	1	1
	W12	0	0	0	0	1

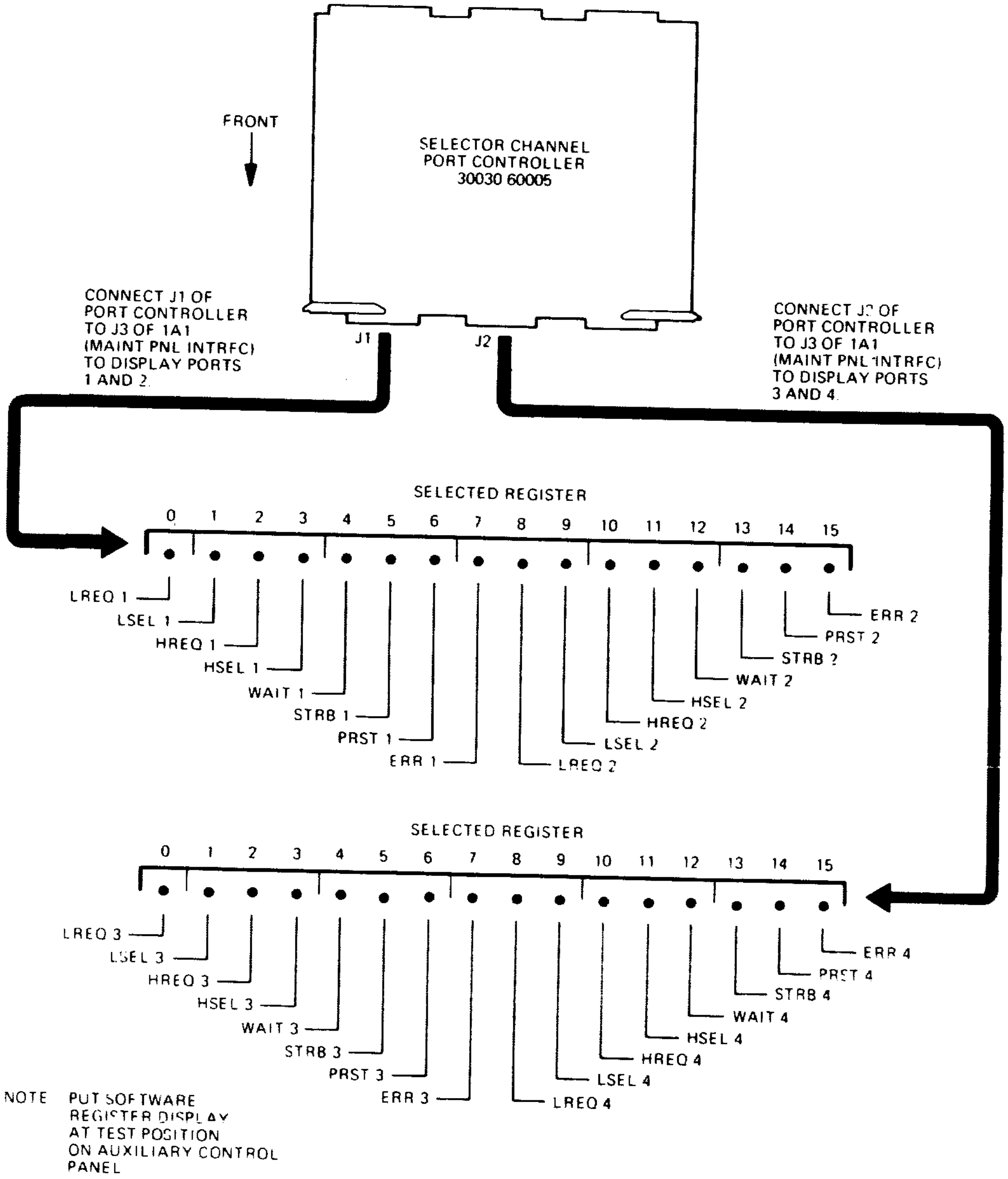
*Only number supported by General Systems Division

ILLEGAL ADDRESS AND "TO" DECODE JUMPERS
SELECTOR CHANNEL REGISTER

SIZE (WORDS)	48K	56K	64K
MODULES	2	2	2
DISTRIBUTION	(32K-16K)	(32K-24K)	(32K-32K)
Selector Channel Reg.			
W50	0	0	0
W51	0	0	0
W52	0	0	0
W53	0	0	0
W54	0	0	0
W55	0	0	0
W56	1	0	0
W57	1	1	0
W60	0	0	0
W61	0	0	0
W62	0	0	0
W63	0	0	0
W64	0	0	0
W65	0	0	0
W66	1	0	0
W67	1	1	0
W70	0	0	0
W71	0	0	0
W72	0	0	0
W73	0	0	0
W74	1	1	1
W75	1	1	1
W76	1	1	1
W77	1	1	1

CHANNEL NUMBER
SELECTOR CHANNEL REGISTER

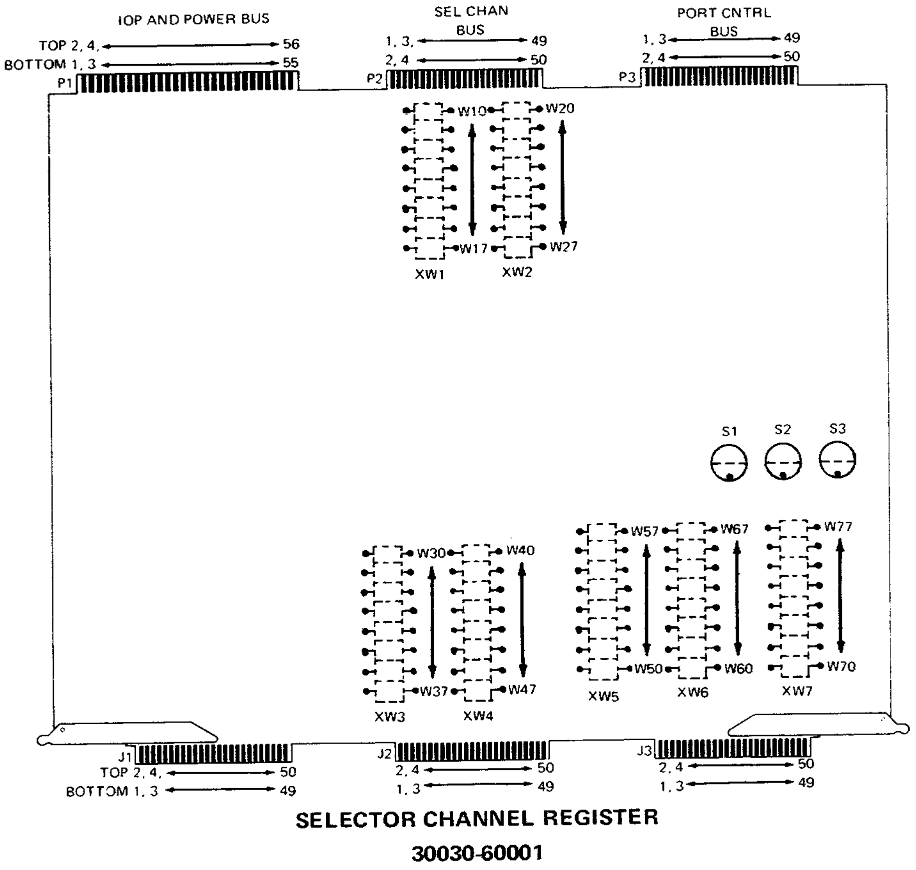
	(XW1) W10-17	(XW2) W20-27	(XW3) W30-37	(XW4) W40-47
CHANNEL1	1	0	0	0
CHANNEL2	0	1	0	0
CHANNEL3	0	0	1	0
CHANNEL4	0	0	0	1



NOTE PUT SOFTWARE REGISTER DISPLAY AT TEST POSITION ON AUXILIARY CONTROL PANEL

1471004-148

PORT CONTROLLER STATE DISPLAY



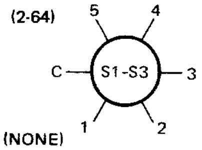
1471004-146

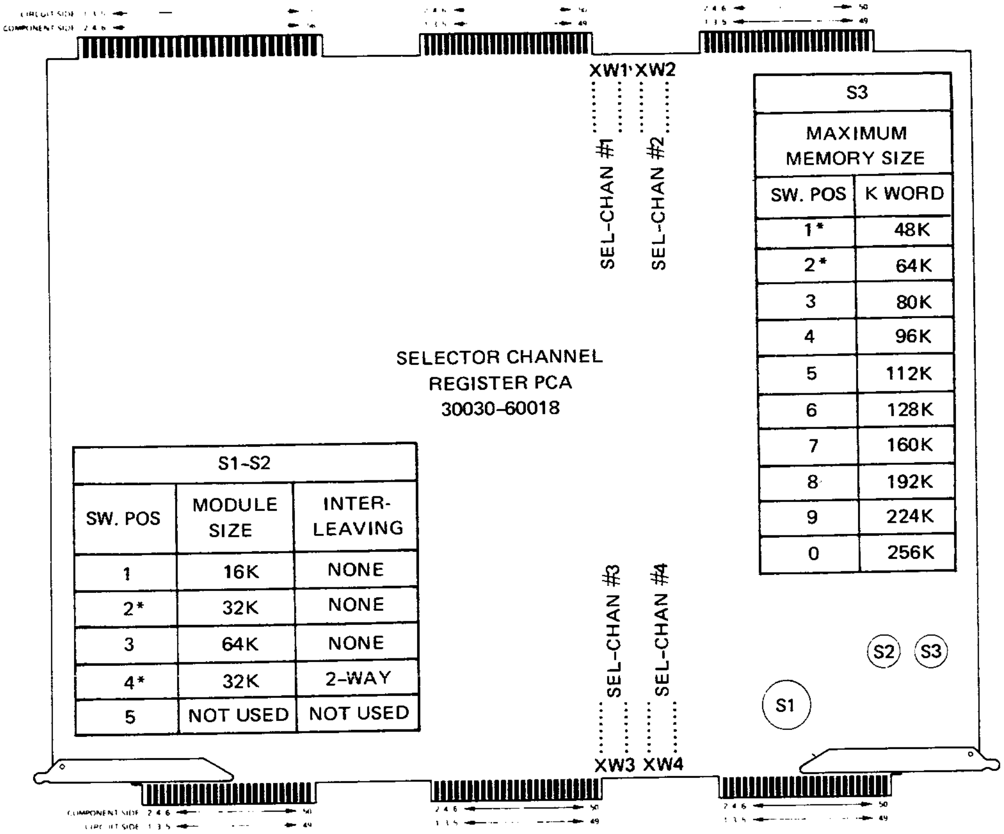
SELECTOR CHANNEL REGISTER 30030-60001

INTERLEAVING AND ADDRESS SPACE

Selector Channel Register

MODULE SIZE (WORDS)	INTER-LEAVING	SWITCH POSITIONS S1	S2	S3
32K	NONE	1	1	1
32K	2-WAY	1	1	5





S3	
MAXIMUM MEMORY SIZE	
SW. POS	K WORD
1*	48K
2*	64K
3	80K
4	96K
5	112K
6	128K
7	160K
8	192K
9	224K
0	256K

S1-S2		
SW. POS	MODULE SIZE	INTER-LEAVING
1	16K	NONE
2*	32K	NONE
3	64K	NONE
4*	32K	2-WAY
5	NOT USED	NOT USED

* = ONLY POSITIONS SUPPORTED ON SERIES I

SELECTOR CHANNEL REGISTER PCA (30030-60018)

The Selector Channel Register PCA has a 10-position switch S3 that is changed to agree with the size of memory in thousands of words. See figure C-3. Switch positions are as follows:

EXAMPLES:		S1	S2	S3
48K WORD	CONFIGURATION	2	2	1
64K WORD	CONFIGURATION (W/O INTERLEAVING)	2	2	2
64K WORD	CONFIGURATION (WITH INTERLEAVING)	4	4	2

147004-148a

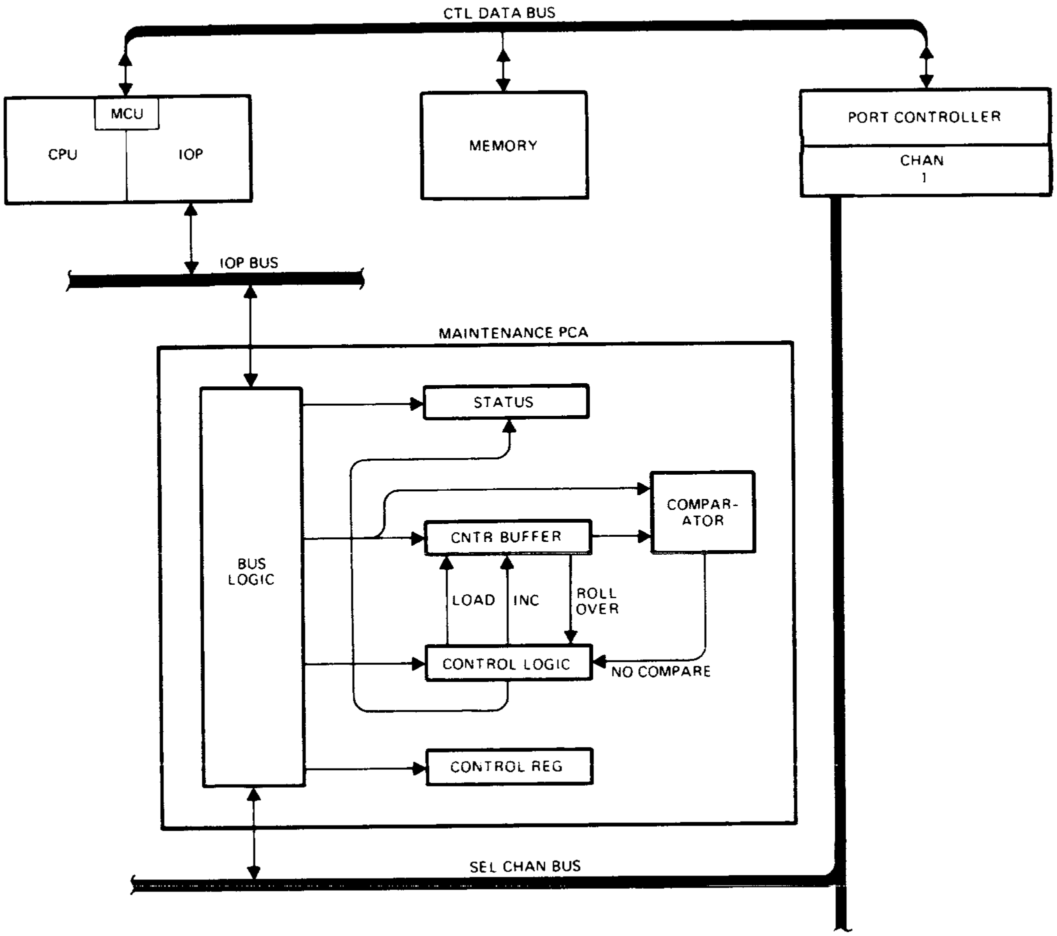
SELECTOR CHANNEL REGISTER PCA 30030-60018

Selector Channel Register PCA (30030-60018)

The Selector Channel Register PCA has a 10-position switch S3 that is changed to agree with the size of memory in thousands of words. Switch positions are as follows:

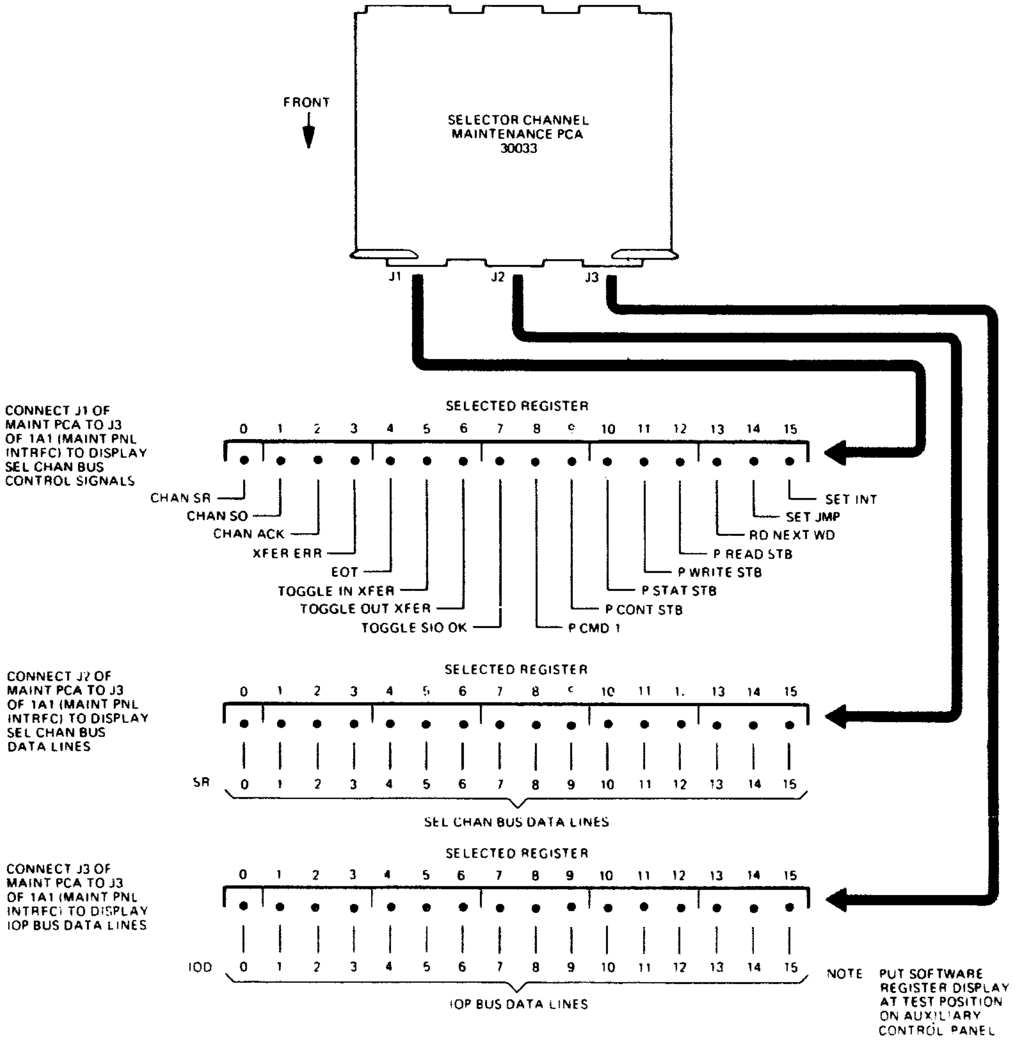
EXAMPLES:	S1	S2	S3
48K WORD configuration	2	2	1
64K WORD configuration (w/o interleaving)	2	2	2
64K WORD configuration (with interleaving)	4	4	2

SELECTOR CHANNEL MAINTENANCE BOARD BLOCK DIAGRAM



1471004-154

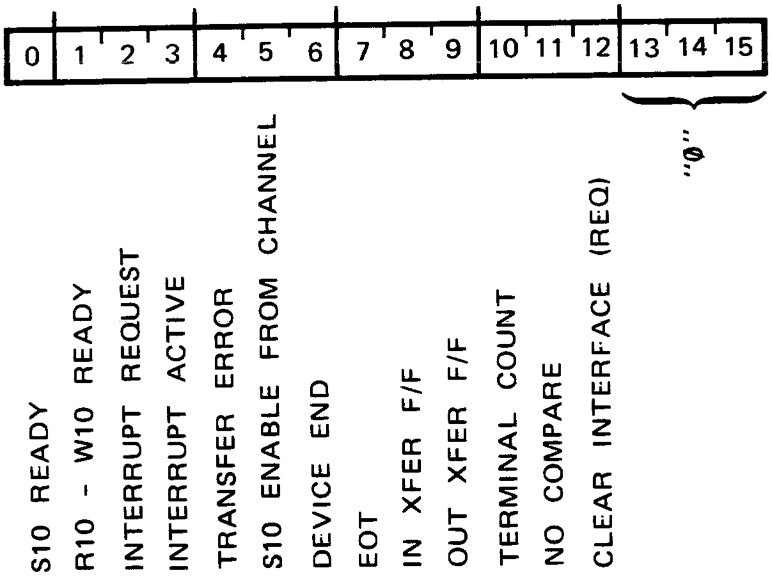
SELECTOR CHANNEL MAINTENANCE BOARD BLOCK DIAGRAM



1471004-155

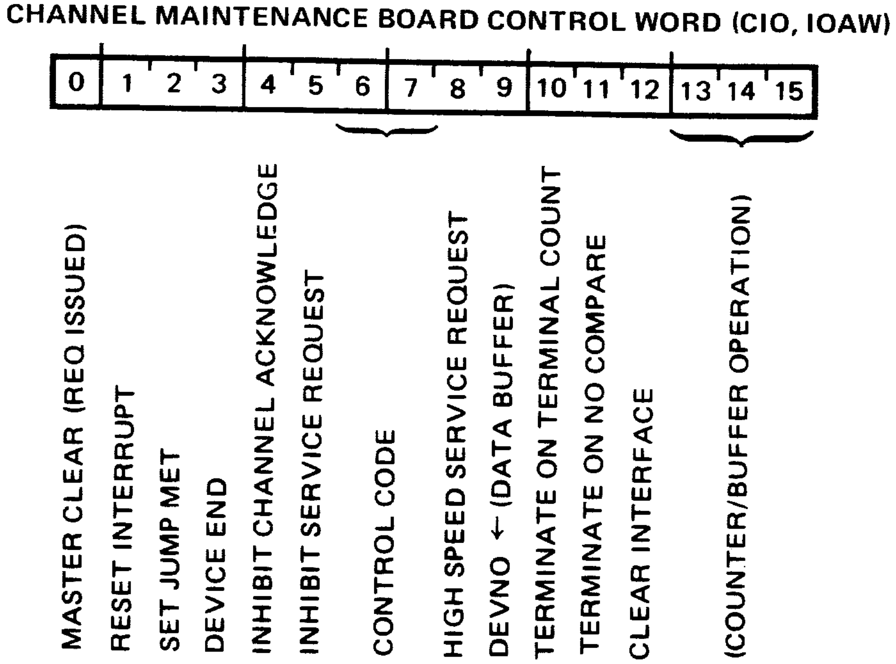
CHANNEL MAINTENANCE BOARD STATE DISPLAY

CHANNEL MAINTENANCE BOARD STATUS WORD (TIO, SENSE, END)



1471004-149

CHANNEL MAINTENANCE BOARD STATUS (TIO, Sense, End)



1471004-150

CHANNEL MAINTENANCE BOARD STATUS (CIO, IOAW)

6	7	
0	0	IGNORE IOCW, USE IOAW AS CONTROL
0	1	LOAD IOCW INTO DATA BUFFER
1	0	LOAD IOAW INTO DATA BUFFER
1	1	LOAD IOCW, THEN IOAW INTO DATA BUFFER

1471004-151

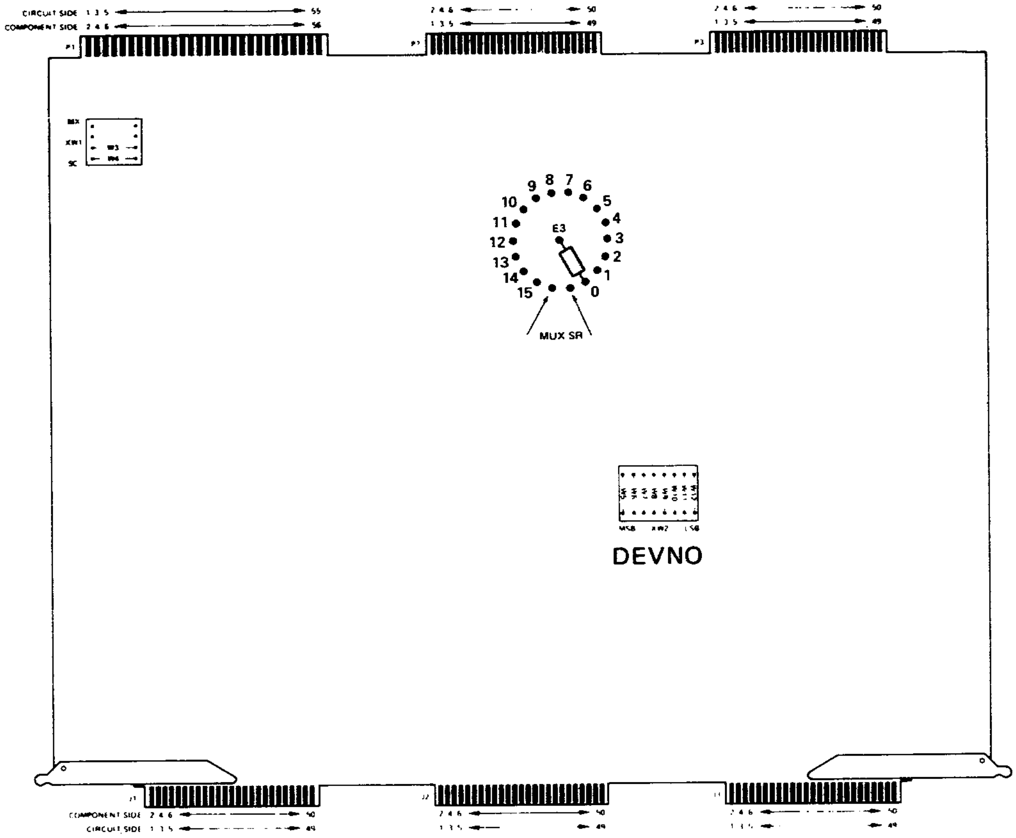
CONTROL CODE

COUNTER/BUFFER OPERATION

13	14	15	
0	0	0	NO COUNT (USE AS BUFFER)
0	0	1	COUNT RD NEXT WORD
0	1	0	COUNT P READ STB
0	1	1	COUNT TOGGLE INXFER
1	0	0	COUNT PWRITE STB
1	0	1	COUNT TOGGLE OUT XFER
1	1	0	COUNT EOT
1	1	1	COUNT CHAN50

1471004-152

COUNTER/BUFFER OPERATION



	SIO – MUX	CHANNEL
W1	I	O
W2	I	O
W3	O	I
W4	O	I

SIO – MUX SERVICE REQUEST SELECT

ONLY ENABLED WHEN W1 and W2 are IN.

NOTE: There is no IODPRTY jumper. Selection is automatic.

1471004-153

SELECTOR CHANNEL MAINTENANCE BOARD

SELECTOR CHANNEL

DIAGNOSTIC STAND-ALONE

SELECTOR CHANNEL S-A
*30030A

1. COLD LOAD DIAGNOSTIC FILE # FROM NON-CPU COLD LOAD TAPE
   D100 HP 30030A SELECTOR CHANNEL DIAG (HP32329.XX.X)
2. Q101 SET MAINT CARD DEV NUM? XX ((DRT # (OCTAL)))
3. Q102 SET TIMER/CONSOLE DEV NUM? XX ((DRT # (OCTAL)))
4. Q103 SET CORE SIZE? XX ((# OF KWORDS))
5. P104 SET SWITCHES? ((SET SW REG THEN RUN))
6. Q105 ERR PRINT LIMIT? XXXX ((0-%7777-0 IMPLIES NO LIMIT))
   *REQUIRES USE OF 30033A MAINTENANCE CARD

PROGRAM OPTION SWITCH SETTINGS

SWITCH	FUNCTION IF SET
0	READ SW 1-15 INTO INTERNAL SWITCH REGISTER
1	EXECUTE SECTION 1 (DIRECT I/O)
2	EXECUTE SECTION 2 (CONTROL ORDERS)
3	EXECUTE SECTION 3 (READ ORDERS, NO CHAINING)
4	EXECUTE SECTION 4 (WRITE ORDERS, NO CHAINING)
5	EXECUTE SECTION 5 (READ ORDERS, CHAINED)
6	EXECUTE SECTION 6 (WRITE ORDERS, CHAINED)
7	EXECUTE SECTION 7 (ERROR CONDITIONS)
8	OUTPUT ALL MESSAGES TO LINE PRINTER
9	**RUN ON MUX CHANNEL
10	SUPPRESS NON-ERROR MESSAGES
11	SUPPRESS ERROR MESSAGES
12	HALT AFTER A COMPLETE PROGRAM CYCLE
13	LOOP ON LAST STEP EXECUTED
14	HALT ON ERROR
15	HALT AT END OF PRESENTLY EXECUTING STEP

** 30033A JUMPER MUST BE SELECTED FOR CHAN OR MUX.
SR = 0

* Core Size	Parameters
32K words	40
40K words	50
48K words	60
56K words	70
64K words	100

Coded Halt Summary

HALT Number	Segment Number	Meaning
-	06	Cold load HALT.
00	21	Unexpected I/O trouble in the IOCM was encountered.
01	22	First HALT in Relocating Loader. Diagnostic Program Index is entered via switch register; press RUN-HALT.
02	22	Second HALT in Relocating Loader. Program load address is entered via switch register; press RUN-HALT.
03	22	Third HALT in Relocating Loader; only occurs if program address entered was less than %4000. Enter correct address; press RUN-HALT.
04	20	Configuration HALT. Enter program options according to Table 1 into switch register; press RUN-HALT.
14	20	Error Print Limit has been reached (see Q105 in Table 2).
15	20	HALT after step; switch 15 was set.
16	20	Selector Channel test failure HALT; switch 14 was set. RA = Step number RB = Device Status
17	20	HALT after complete cycle of diagnostic; switch 12 was set.

CLOCK-CONSOLE PCA
30031A

DIFFERENCES FROM SERIES II

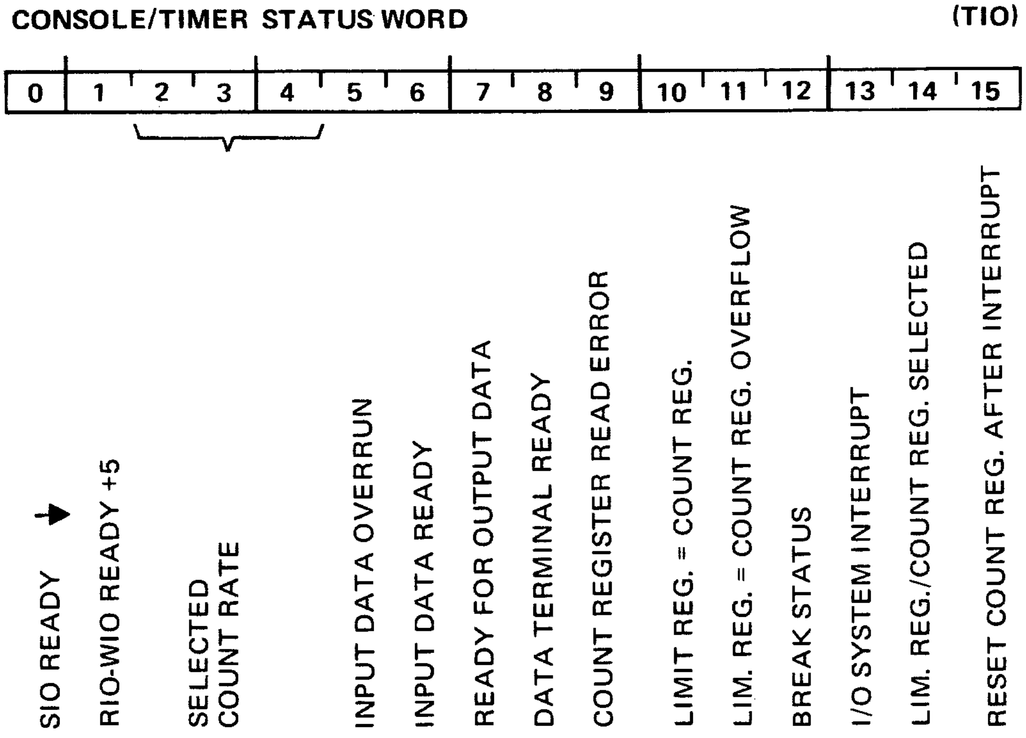
The Clock/Console PCA shares a dual purpose in all HP 3000 pre Series II systems.

Primarily, this PCA communicates into and from the computer as a system console.

Secondly, the PCA has clocking logic that is used by MPE and diagnostics to keep track of time - slicing processes, etc.

Supported Console Devices On Pre Series II

-ASR 33,35 - 10 cps
-Terminet 10 cps - 30 cps
-2600 10 cps - 240 cps
-2640A/B 10 cps -240 cps



1471004-156

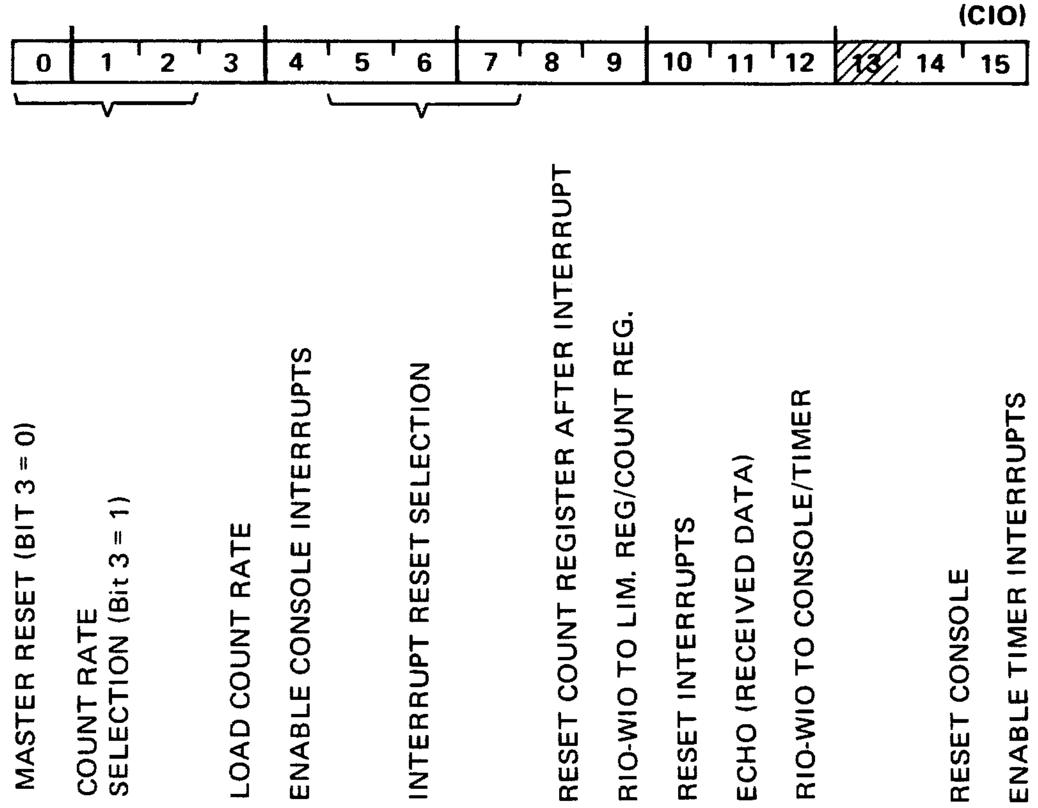
CONSOLE/TIMER STATUS WORD

COUNT RATE

2	3	4	
0	0	0	1 μsec
0	0	1	10 μsec
0	1	0	100 μsec
0	1	1	1 msec
1	0	0	10 msec
1	0	1	100 msec
1	1	0	1 sec
1	1	1	10 sec

1471004-157

COUNT RATE



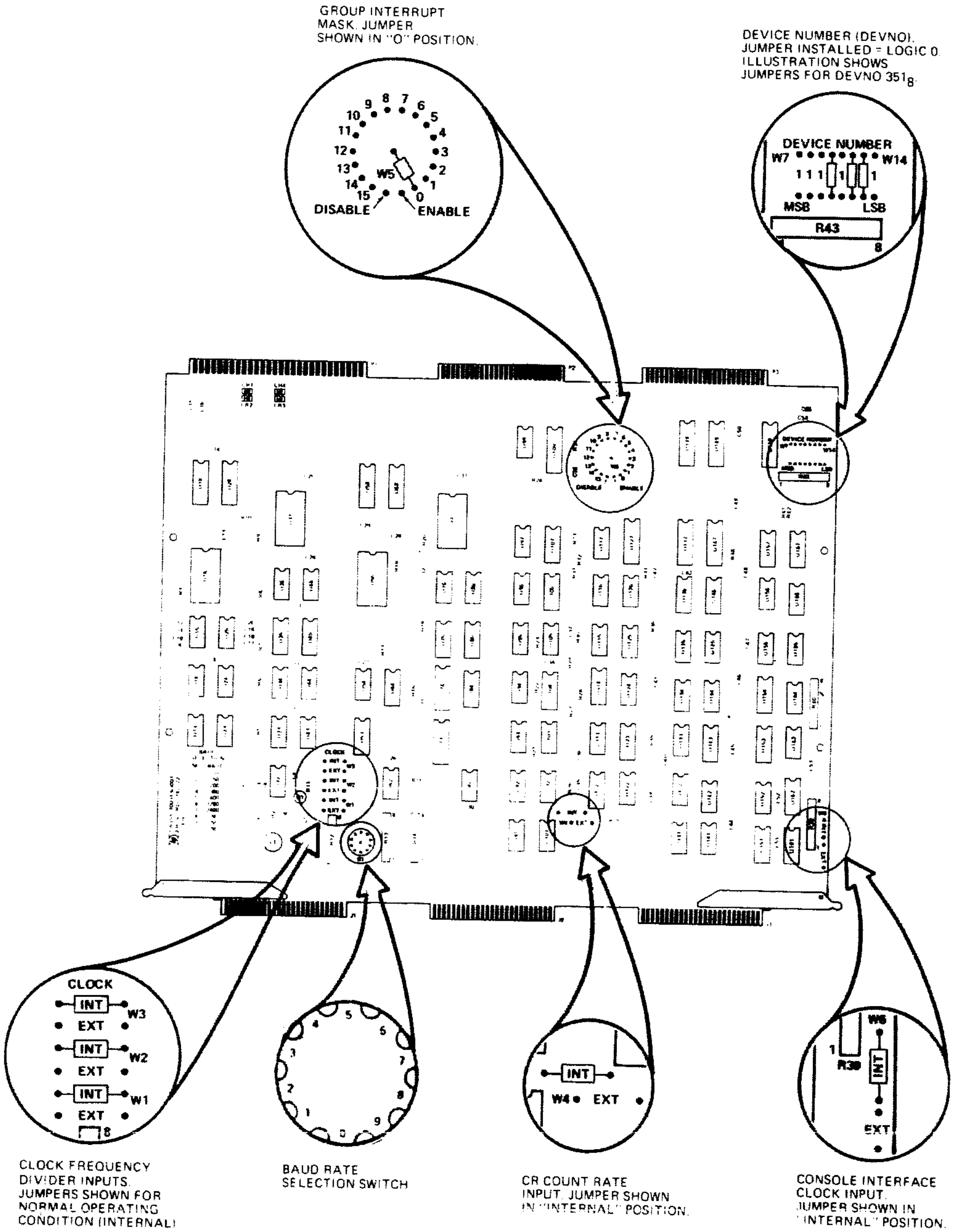
1471004-158

CONSOLE/TIMER CONTROL WORD

5	6	7	
0	0	0	NO RESET
0	0	1	LIMIT REG. = COUNT REG. (CLK)
0	1	0	LIMIT REG. = COUNT REG. OVERFLOW (CLK)
0	1	1	I/O SYSTEM (SIN)
1	0	0	INPUT DATA OVERRUN (CONSOLE)
1	0	1	INPUT DATA READY (CONSOLE)
1	1	0	READY FOR OUTPUT DATA (CONSOLE)
1	1	1	COUNT REGISTER READ ERROR (CLK)

1471004-159

INTERRUPT RESET SELECTION



GROUP INTERRUPT MASK JUMPER SHOWN IN "O" POSITION.

DEVICE NUMBER (DEVNO). JUMPER INSTALLED = LOGIC 0. ILLUSTRATION SHOWS JUMPERS FOR DEVNO 351_8.

CLOCK FREQUENCY DIVIDER INPUTS. JUMPERS SHOWN FOR NORMAL OPERATING CONDITION (INTERNAL)

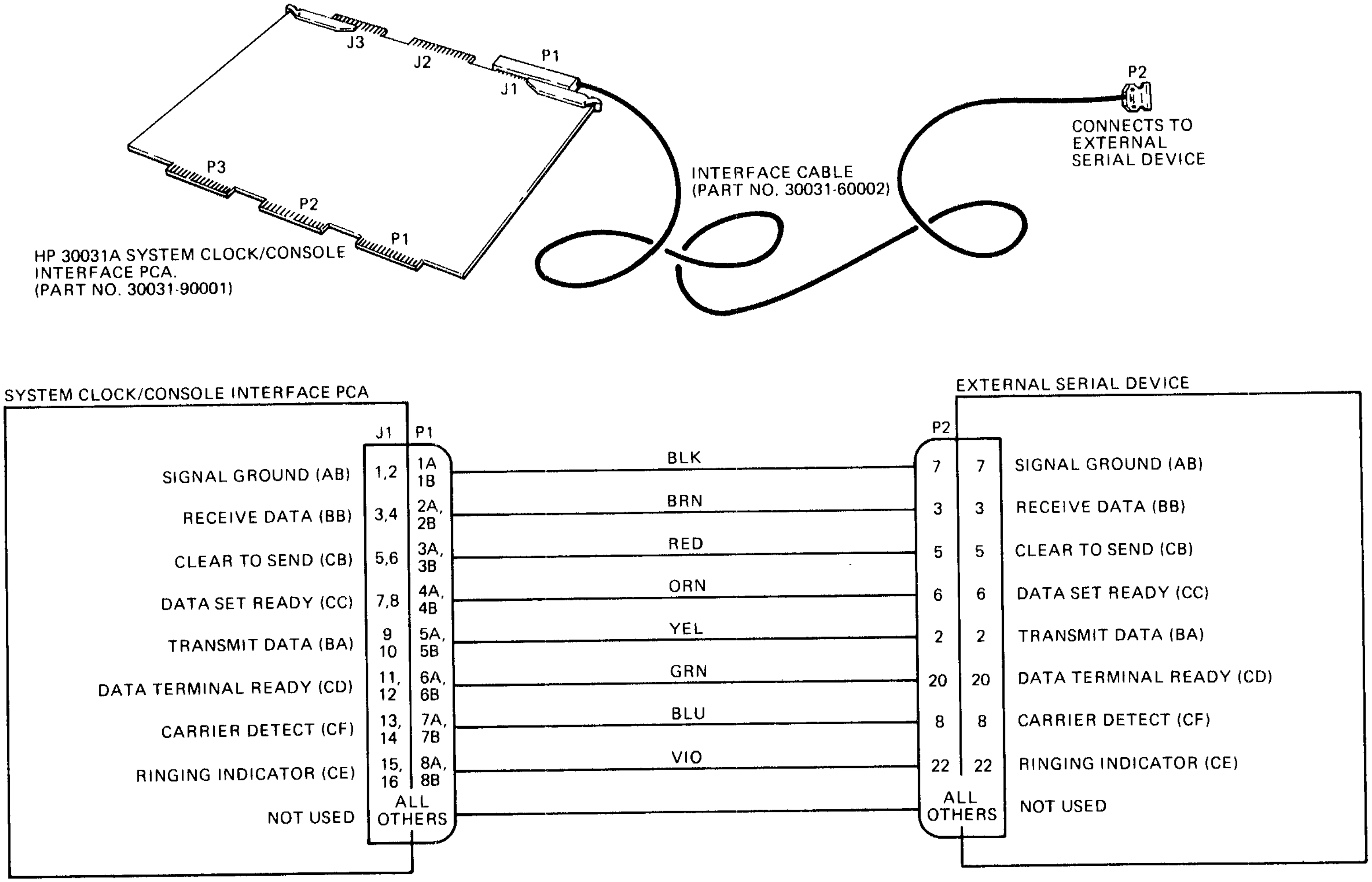
BAUD RATE SELECTION SWITCH

CR COUNT RATE INPUT. JUMPER SHOWN IN "INTERNAL" POSITION.

CONSOLE INTERFACE CLOCK INPUT. JUMPER SHOWN IN "INTERNAL" POSITION.

1471004-160

SYSTEM CLOCK/CONSOLE JUMPER AND SWITCH LOCATIONS



1471004-161

INTERFACE CABLE ASSEMBLY WIRING DIAGRAM

DIAGNOSTIC STAND-ALONE

SYSTEM CLOCK/CONSOLE S-A
30031A

1. COLD LOAD DIAG FILE # FROM NON-CPU COLD LOAD TAPE
   HALT2 (% 30362)
2. SET DRT # IN SWITCH REG - PRESS RUN
   *DIAGNOSTIC WILL LOOP UNTIL SWITCH REGISTER OPTIONS ARE SELECTED

SWITCH REGISTER OPTIONS

*0	SELECT EXTERNAL REGISTER
1	COUNTING/LIMIT - REGISTER, INTERRUPT & OVERFLOW TEST
2	CR = LR COUNTING RATES TEST
3	COMMAND BITS FOR SYS CLOCK TEST
4	STATUS BITS FOR SYS CLOCK TEST
5	COMMAND/STATUS BITS FOR CONSOLE TEST
8	BYPASS OP INTERVENTION IN TEST 5
9	HALT AFTER CURRENT SECTION
12	HALT AFTER COMPLETE DIAG CYCLE
13	LOOP ON CURRENT STEP
14	SUPPRESS ERROR HALTS
15	HALT AT END OF CURRENT STEP

* Select Last

CODED HALT TABLE:

HALT #	CIR	DEFINITION
3	%30363	ERROR HALT, SEE RA FOR ERROR CODE
4	%30364	HALT AFTER STEP
5	%30365	HALT AFTER CURRENT SELECTION
6	%30366	HALT AFTER COMPLETE CYCLE
7	%30367	ECHO ON TEST, PRESS RUN AND TYPE THEN CR
10	%30370	ECHO OFF TEST, PRESS RUN AND TYPE THEN CR
11	%30371	INPUT DATA OVERRUN TEST, TYPE THEN PRESS
13	%30373	PRESS BREAK KEY, THEN PRESS RUN
14	%30374	PRESS RUN THEN BREAK KEY
15	%30375	UNEXPECTED EXTERNAL INTERRUPT
16	%30376	UNEXPECTED INTERNAL INTERRUPT

DIAGNOSTICS STAND-ALONE

TELEPRINTER
30124A

1. COLD LOAD DIAG FILE # FROM NON-CPU COLD LOAD TAPE
   D1 TELEPRINTER TEST (HP32326A.NN.N)
   P2 SET SWITCHES ((SET SW REG OPTIONS THEN RUN))

SWITCH REGISTER OPTIONS

0	REPORT ONLY 1ST OCCURRANCE OF SPECIFIC ERROR
1	PRINTER TEST
2	KEYBOARD TEST
3	PUNCH TEST
4	PUNCH TEST
5	READER TEST
6	OPERATOR DESIGNED TEST
8	SUPPRESS MSG PRINTING, HALT INSTEAD
9	HALT AFTER CURRENT SECTION
10	SUPPRESS NON-ERROR MSG´S
11	SUPPRESS ERROR MSG´S
12	HALT AFTER COMPLETE DIAG CYCLE
13	LOOP ON CURRENT SECTION
14	HALT ON ERROR
15	HALT AFTER CURRENT STEP

CODED HALT TABLE:

HALT #	CIR	DEFINITION
3	%30363	ERROR HALT
4	%30365	HALT AFTER CURRENT SECTION
6	%30366	P-CLASS HALT, NEEDS OPERATOR ACTION
7	%30367	MSG HALT, CHECK FRONT PANEL (CPU - SW8)
10	%30370	COULDN´T FIND MSG!!!!
17	%30377	HALT AFTER COMPLETE CYCLE

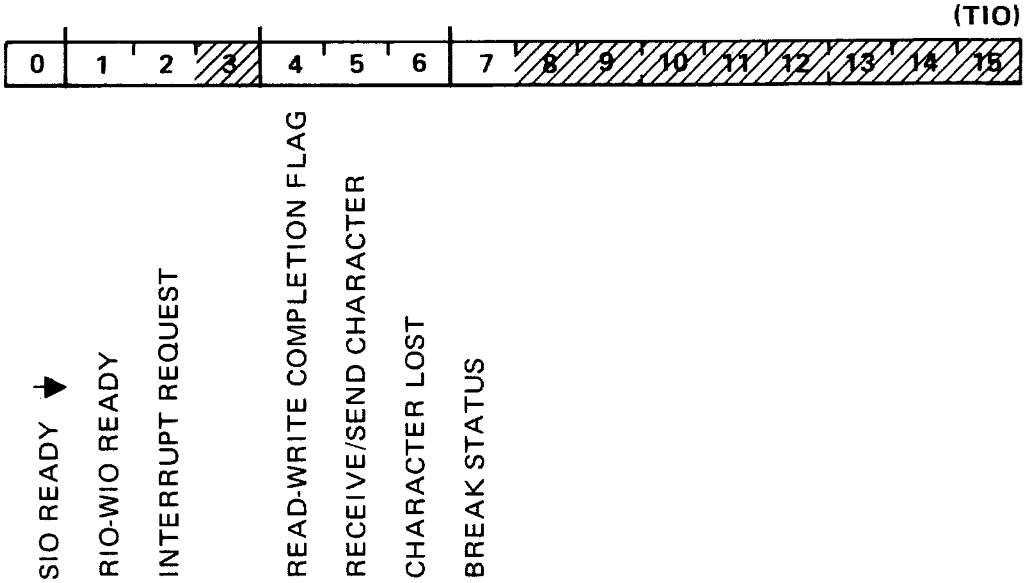
ASYNCHRONOUS TERMINAL CONTROLLER

ASYNCHRONOUS TERMINAL CONTROLLER
30032B:
TERMINAL DATA INTERFACE
30060A

MODEMS SUPPORTED ON PRE SERIES II

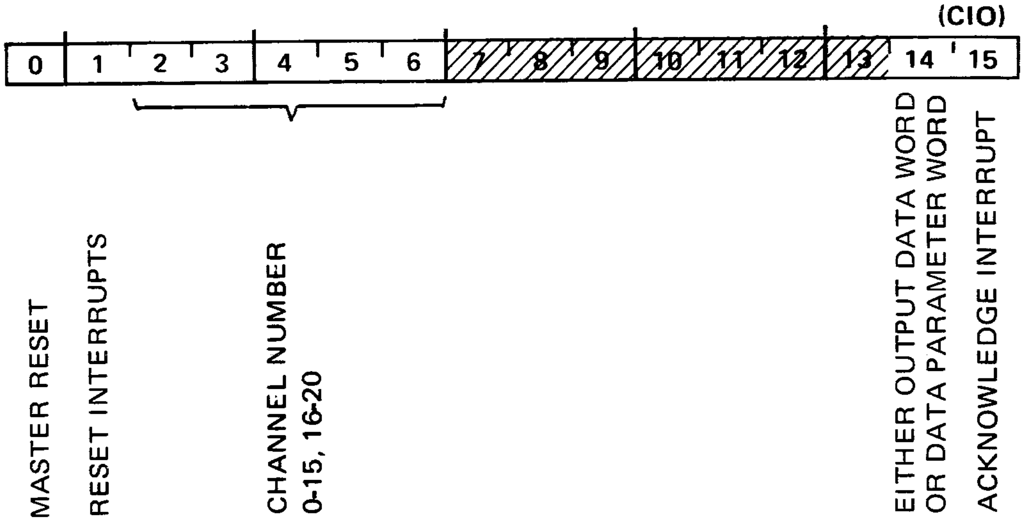
103A	FULL DUPLEX 30 CPS
113B	FULL DUPLEX 30 CPS
202C	HALF DUPLEX 120 CPS
VADIC 300	FULL DUPLEX 30 CPS
VADIC 3400	FULL DUPLEX 120 CPS

HP does not support leased lines with any pre Series II 3000 Computer.



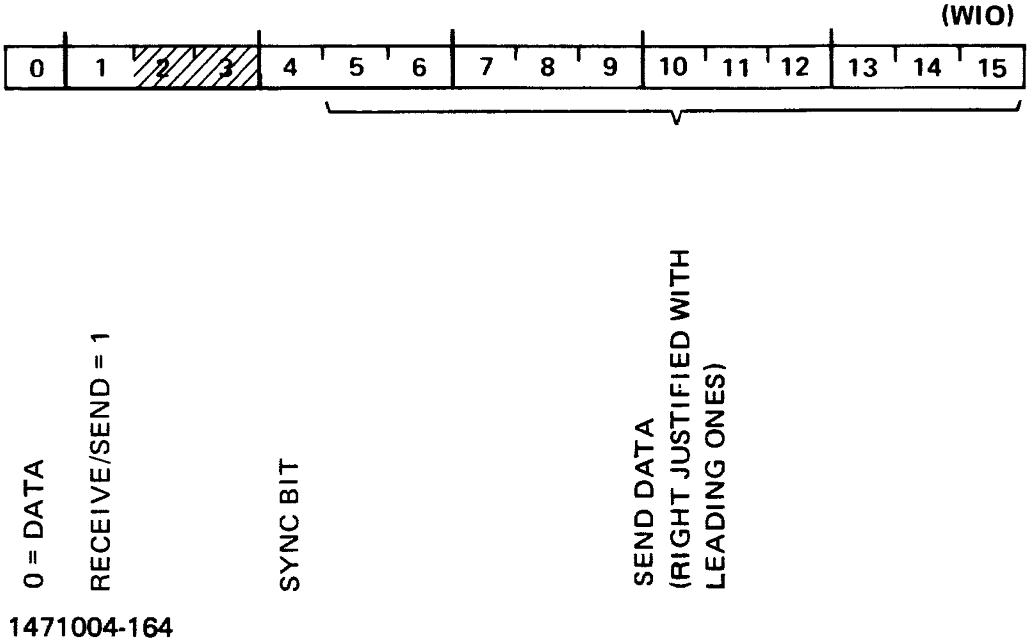
1471004-162

TERMINAL DATA STATUS WORD

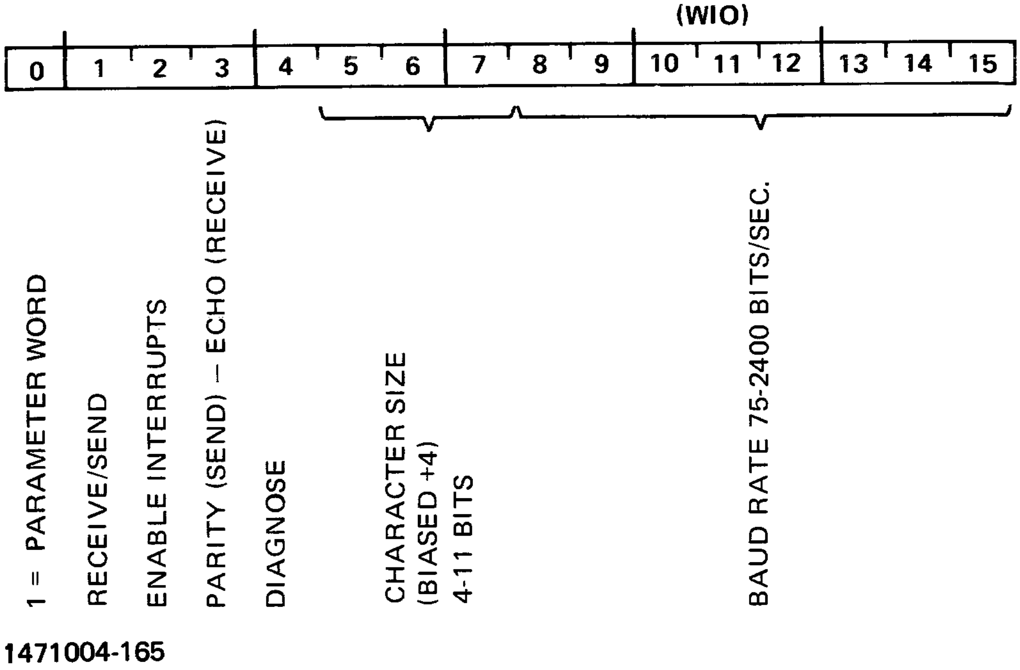


1471004-163

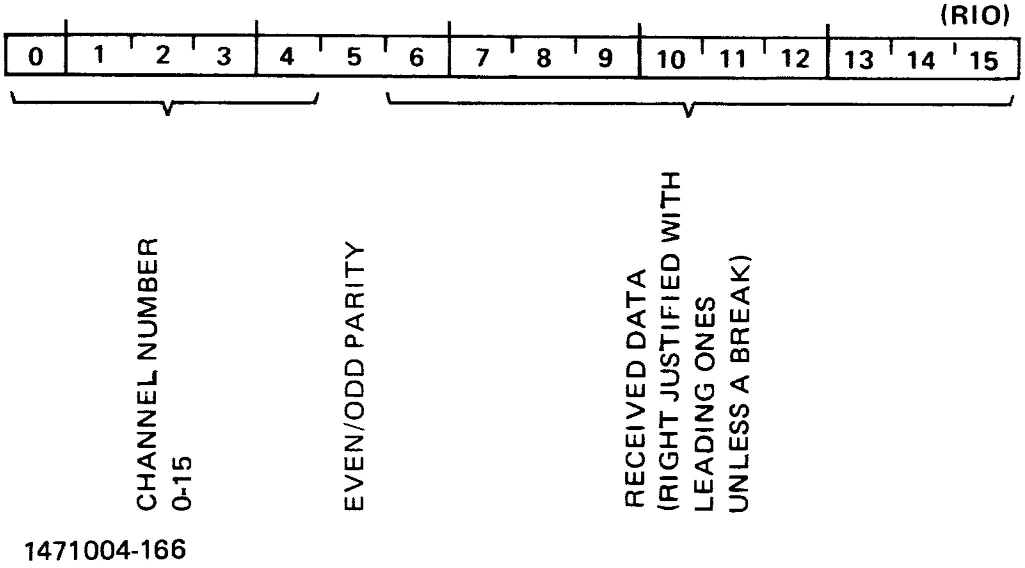
TERMINAL DATA CONTROL WORD



TERMINAL DATA OUTPUT DATA WORD



TERMINAL DATA PARAMETER WORD

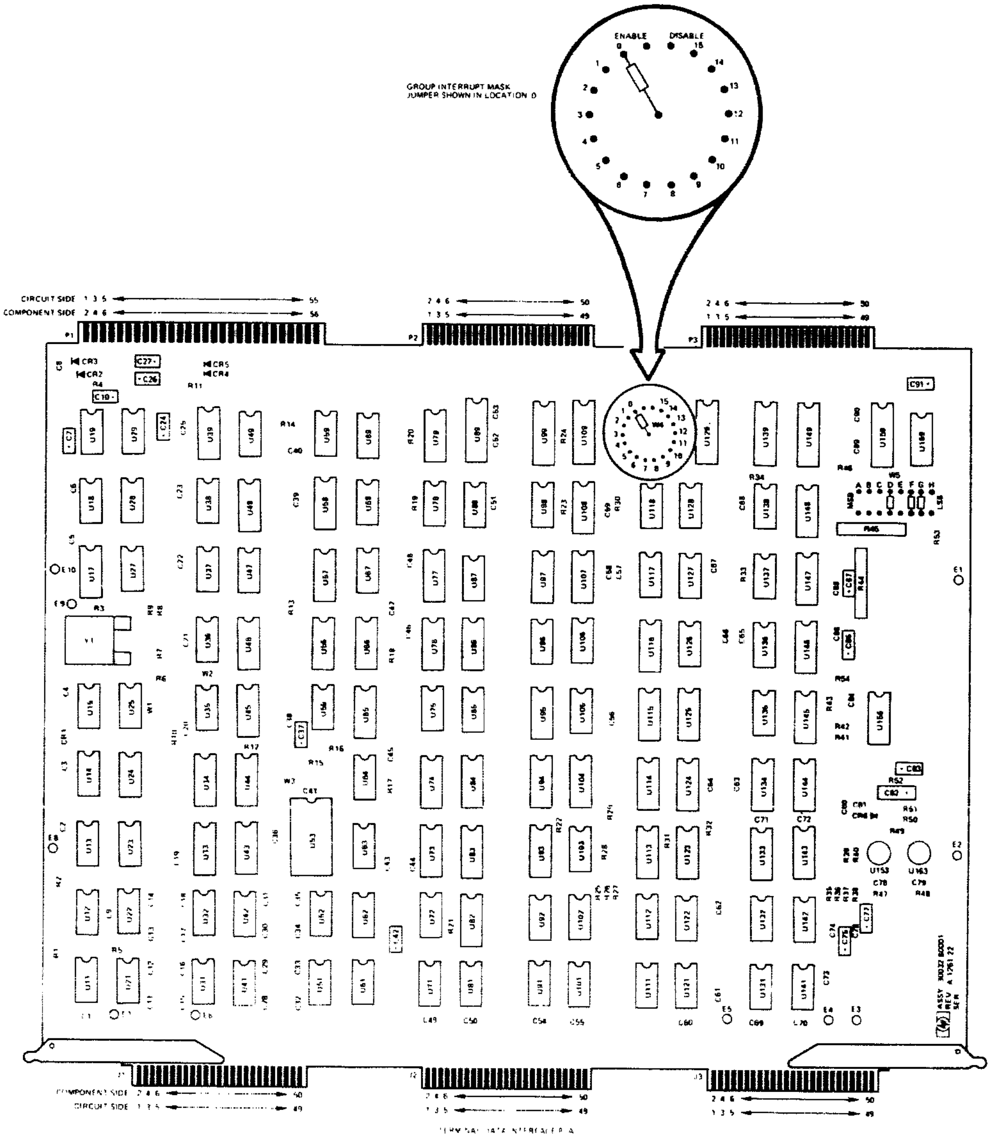


TERMINAL DATA INPUT DATA WORD

BAUD RATE		CHARACTER SIZE (BIT LENGTH)
10	%202	7
15	%137	6
30	% 57	6
60	% 27	6
120	% 13	6
240	% 5	6

HARDWARE EXTENSION CABLES

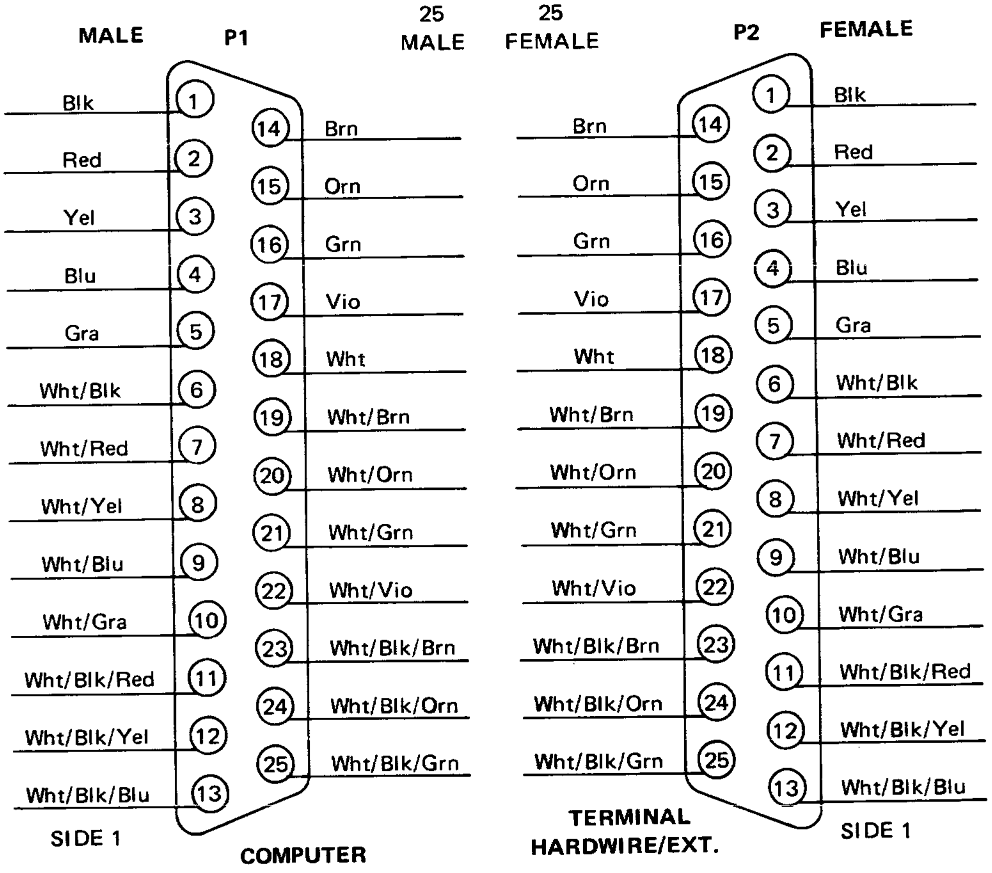
30062-60006 (25 FT)
30062-60009 (50 FT)
30062-60012 (100 FT)



1471004-167

TERMINAL DATA INTERFACE JUMPER LOCATIONS

COMPUTER				EIA COMPATIBLE DEVICE
	1		1	
(BB) RECEIVE DATA	—2	←	2	— RECEIVE DATA (BB)
(BA) SEND DATA	—3	→	3	— SEND DATA (BA)
(CF) CARRIER DETECT	—4	←	4	— CARRIER DETECT (CF)
	5		5	
(CD) DATA TERMINAL READY	—6	→	6	— DATA TERMINAL READY (CD)
(AB) COMMON RETURN	—7	↔	7	— COMMON RETURN (AB)
(CA) REQUEST TO SEND	—8	→	8	— REQUEST TO SEND (CA)
	9		9	
	10		10	
(SB) SECONDARY RECEIVE DATA	—11	←	11	— SECONDARY RECEIVE DATA (SB)
(SA) SECONDARY SEND DATA	—12	→	12	— SECONDARY SEND DATA (SA)
	13		13	
	14		14	
	15		15	
	16		16	
	17		17	
	18		18	
	19		19	
(CC) DATA SET READY	—20	←	20	— DATA SET READY (CC)
	21		21	
(CB) CLEAR TO SEND	—22	←	22	— CLEAR TO SEND (CB)
(CH) FREQUENCY SELECT	—23	→	23	— FREQUENCY SELECT (CH)
	24		24	
	25		25	
	MALE		FEMALE	



1471004-168

HARDWARE/EXTENSION CABLE PIN CONNECTIONS

TERMINAL DATA ONLINE
30032B

```
*NEW TERMDATA    ((WHATEVER))
PROGRAM FILE?   PD363A.XXXXXX.XXXXXX
DEVICE?  XX   ((DECIMAL # OF DRT #))
SET FLAGS? X,X,X,X,X    ((WHATEVER))
Q1 AUTOMATIC MODE? YES OR NO   ((YES = 16 CH TEST))
Q2 PRESELECT CHANNELS? YES OR NO
Q3 CH X = ? XX ((1ST PORT TO BE PRESELECTED))
Q4 CH Y = ? XX ((LAST PORT TO BE PRESELECTED))
*SAVE TERMDATA     ((SAVES IT INTO THE PST))
*ON AND RUN OR RUN TERMDATA
```

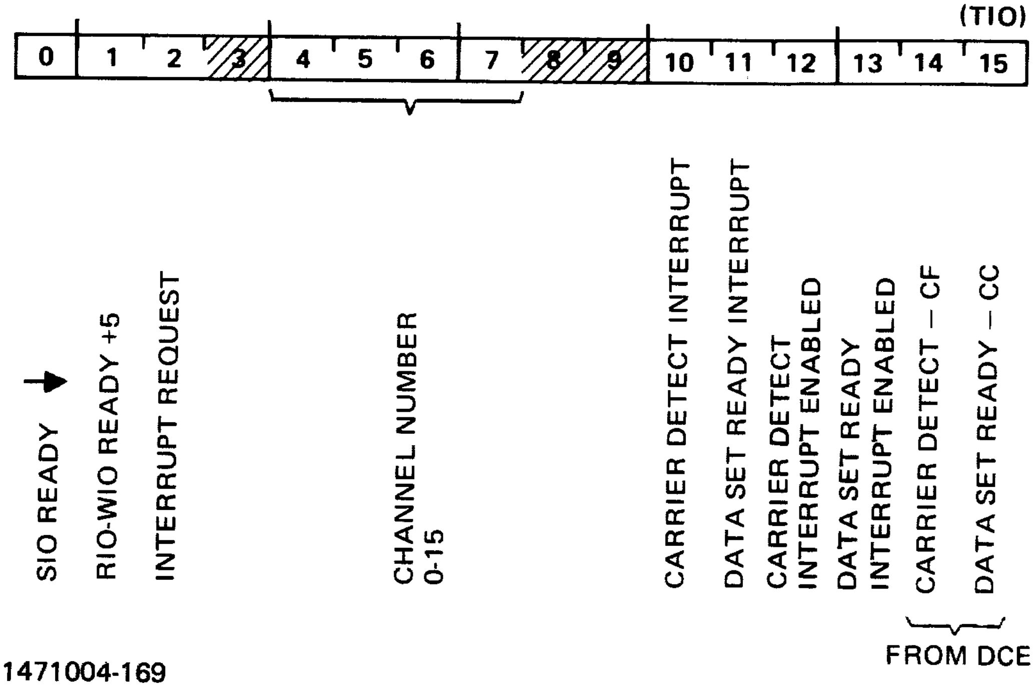
FLAGS:

1	INTERRUPT TEST
2	SEND/RECEIVE TEST
3	BREAK TEST
4	PARITY TEST
5	DIAGNOSE TEST
6	ECHO TEST
7	SYNC TEST
8	CHARACTER - LOST TEST
9	READ/WRITE TEST
10	NOT USED
11	USE PRESELECTED CHANNELS
12	PRINTS END OF SECTION MSG
13	PAUSE AFTER COMPLETION OF SECTION

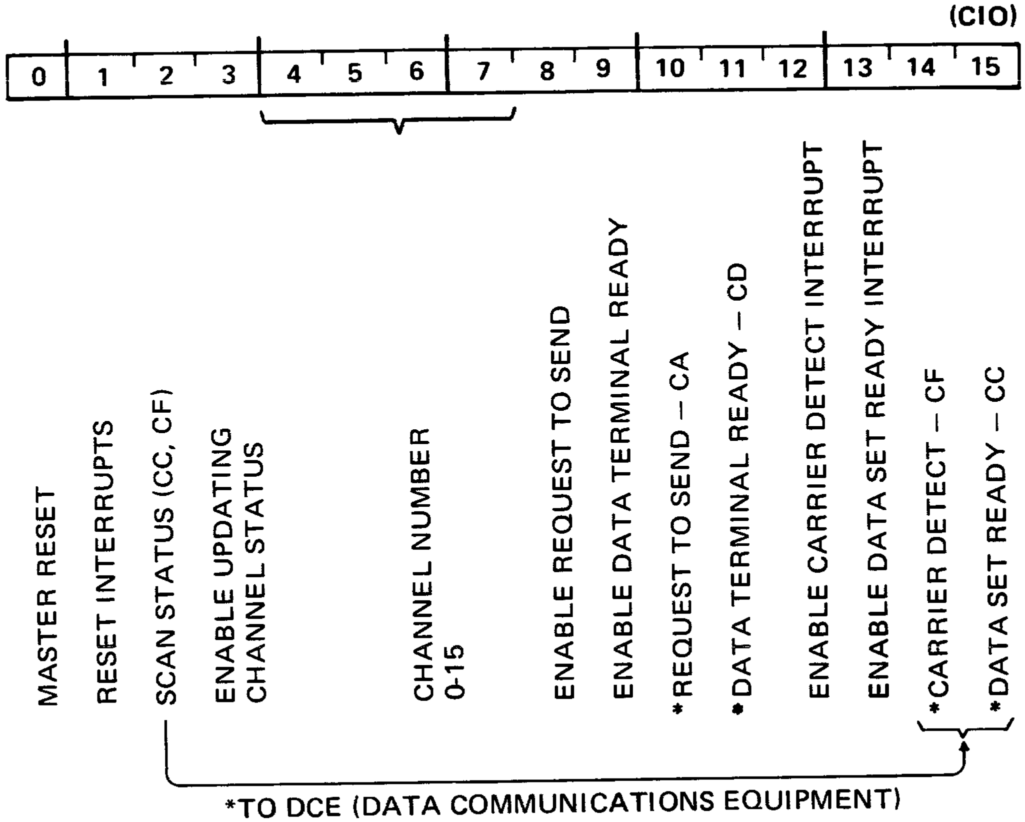
DEVNO = TDI + 1 for 103 MODEM CAPABILITY
DEVNO = TDI + 2 for 202 MODEM CAPABILITY

<<CAUTION>>

The absence of a second TCI board may cause secondary Receive Data (SB) to float. As a result, any spike during data transmission in any one terminal can cause SB to go low. The solution is to terminate the unused connectors J17 and J19 of the Asyn Terminal Junction Panel with (HP 30063-60019) terminators.

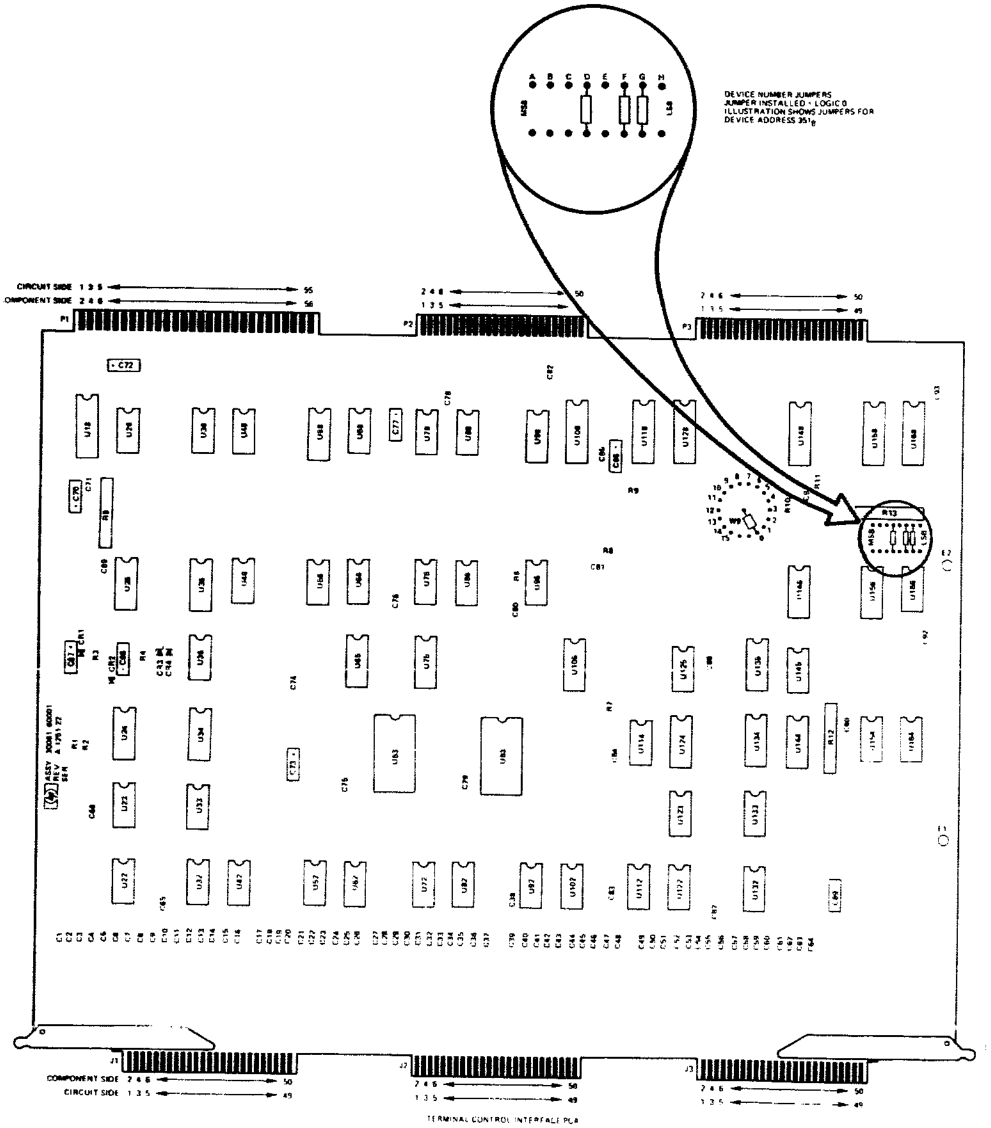


TERMINAL CONTROL #1 STATUS WORD



1471004-170

TERMINAL CONTROL #1 CONTROL WORD



1471004-171

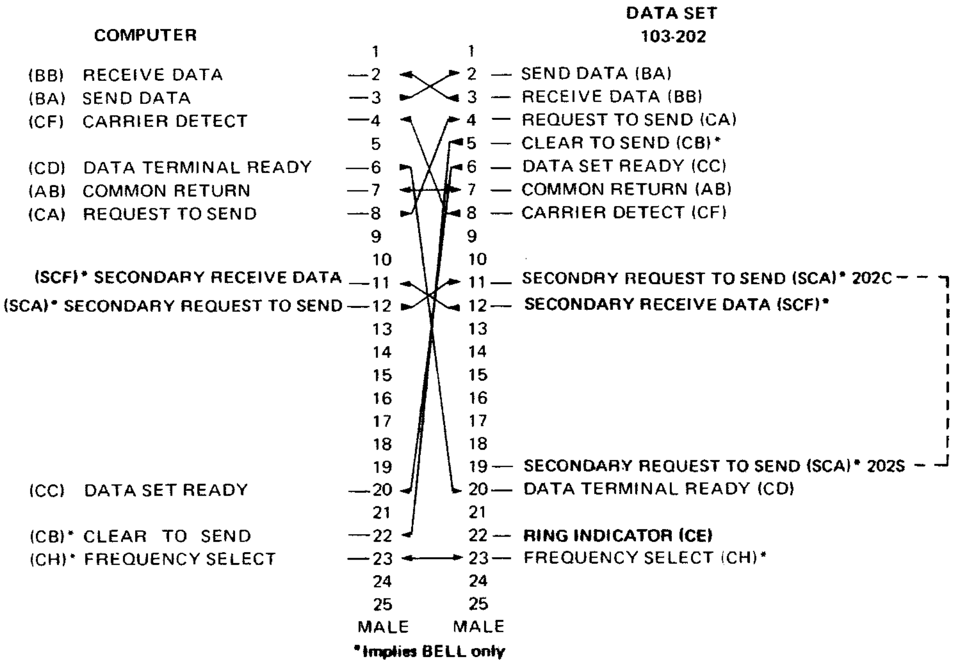
TCI JUMPER LOCATIONS

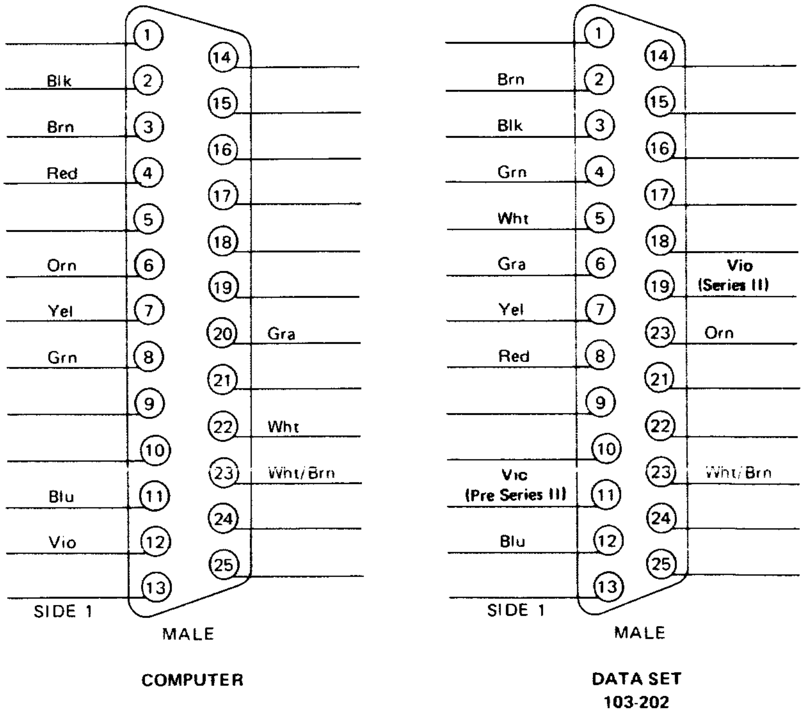
		GND	DATA		CONTROL		TIMING	
CIRCUIT	SIGNAL DESCRIPTION		FROM DCE	TO DCE	FROM DCE	TO DCE	FROM DCE	TO DCE
AA	Protective Ground	X						
AB	Signal Ground/Common Return	X						
BA	Transmitted Data			X				
BB	Received Data		X					
CA	Request to Send					X		
CB	Clear to Send				X			
CC	Data Set Ready				X			
CD	Data Terminal Ready					X		
CE	Ring Indicator				X			
CF	Carrier Detect				X			
CG	Signal Quality Detector				X			
CH	Data Signal Rate Selector (DTE)					X		
CI	Data Signal Rate Selector (DCE)				X			
DA	Transmitter Signal Element Timing (DTE)							X
DB	Transmitter Signal Element Timing (DCE)						X	
DD	Receiver Signal Element Timing (DCE)						X	
SBA	Secondary Transmitted Data			X				
SBB	Secondary Received Data		X					
SCA	Secondary Request to Send					X		
SCB	Secondary Clear to Send				X			
SCF	Secondary Carrier Detect				X			

DTE (Data Terminal Equipment)
DCE (Data Communications Equipment)

1471004-172

SIGNAL DESCRIPTION TABLE





MODEM CABLES FOR HP 3000 PRE SERIES II ONLY
30062-60004 (25 ft.)
30062-60007 (50 ft.)

MODEM CABLES FOR HP 3000 SERIES II ONLY
30062-60020 (7.5 meters)
30062-60021 (15 meters)

1471004-173

MODEM CABLE PIN CONNECTIONS

TERMINAL CONTROL ONLINE
30061A

```
*NEW TERMCNTRL   ((WHATEVER))
PROGRAM FILE?    PD368A.XXXXXX.XXXXXX
DEVICE?  XX  ((DECIMAL # OF DRT #))
SET FLAGS? X,X,X,X,X   ((WHATEVER))
Q1 AUTOMATIC MODE? YES OR NO  ((YES = 16 CH TEST))
Q2 PRESELECT CHANNELS? YES OR NO
Q3 CH X = ? XX ((1ST PORT TO BE PRESELECTED))
Q4 CH Y = ? XX ((LAST PORT TO BE PRESELECTED))
*SAVE TERMCNTL    ((SAVES IT INTO THE PST))
*ON AND RUN OR RUN TERMCNTL
```

FLAGS:

1	INTERRUPT TEST
2	CHANNEL NUMBER REGISTER TEST
3	CONTROL AND STATUS WORD TEST
4	CHANNEL ADDRESSING TEST
5	STATUS INTERRUPT TEST
6	SCAN TEST
11	USE PRESELECTED PORTS
12	PRINTS END OF SECTION MSG
13	PAUSE AFTER COMPLETION OF SECTION

UNIVERSAL INTERFACES
30050A/30051A

DIFFERENCES FROM SERIES II

Must be Date Code 1504 or higher to run on Series II. Must be Date Code 1401 or higher to run on pre Series II.

```
        STATUS WORD
|---|-----------|-----------|-----------|-----------|-----------|-----------|
| 0|  1|  2|  3|  4|  5|  6|  7|  8|  9| 10| 11| 12| 13| 14| 15|
|---|-----------|-----------|-----------|-----------|-----------|-----------|
  Field/bit Definitions:

|<------------ A -------------->|<------------ B -------------->|
```

where:

Field A = Interface Status Byte. bits 0 through 6 always contain Interface PCA Status, as listed below:

Field B = Interrupt or Device Status Byte. When bit 6 of Field A is ON (logic state 1), Field B contains Device Status. Otherwise, Field B contains Interrupt Status.

bit 0 = SIO OK. A logic 1 indicates that it is permissable to execute an SIO instruction.

bit 1 = RIO, WIO OK. A logic 1 indicates that it is permissable to execute an RIO or WIO instruction.

bit 2 = Interrupt pending. A logic 1 indicates that at least one of the eight possible interface PCA operations is requesting an interrupt.

bits 3 & 4 = Sequence Counter. These two bits indicate the condition of the data transfer sequence counter.

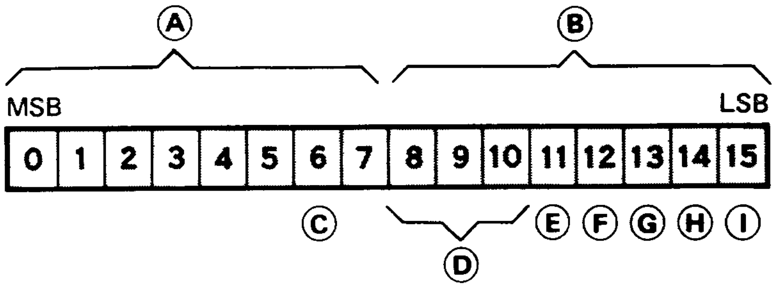
bit 5 = Device Flag. A logic 1 indicates I/O operation has begun. Between I/O operations this bit is normally at logic 0.

bit 6 = Interrupt/Device Status. This bit indicates the contents of the lower eight bits. A logic 1 indicate indicates Device Status, and a logic 0 indicates Interrupt Status.

bit 7 = is always "0."

471004-174

30050A/51A STATUS WORD



Ⓐ Interface Status Byte. These upper eight bits always indicate the interface PCA status.

Ⓑ Interrupt Status Byte. These lower eight bits indicate interrupt status when bit 6 is a logic 0.

Ⓒ Interrupt/Device Status. This bit indicates content of the lower eight status bits and must be a logic 0 for interrupt status.

Ⓓ Device Status Interrupts. Device status bits 8, 9, and 10 can be used to initiate interrupt requests. When used to initiate an interrupt request, device status bits 8, 9, and 10 also initiate interrupt status bits 8, 9, and 10 respectively.

Ⓔ Data Transfer Interrupt. A logic 1 indicates that control word bit 11 is a logic 1 and that an interrupt request will occur after each data transfer.

Ⓕ Clear Interface Interrupt. A logic 1 indicates that an I/O program was cancelled by the external device.

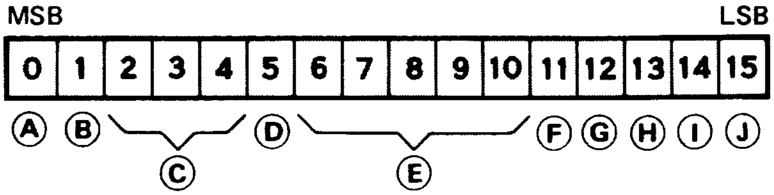
Ⓖ I/O System Interrupt. A logic 1 indicates that a direct SIN command or I/O program INTERRUPT code was executed.

Ⓗ Transfer Error Interrupt. A logic 1 indicates that an error has occurred in the transfer of data between the interface PCA and the computer system.

Ⓘ Transfer Timer Interrupt. A logic 1 indicates that the transfer timer was enabled by control word bit 15 and the time expired before the timer was cleared.

1471004-175

INTERFACE/INTERRUPT STATUS WORD FORMAT



Ⓐ Master Clear. A logic 1 initializes interface PCA.

Ⓑ Clear All Interrupts. A logic 1 clears all processes on the interface PCA that could initiate an Interrupt Request signal.

Ⓒ Selective Interrupt Clear. These three bits are programmed in octal code to selectively clear each of the eight processes that can initiate an Interrupt Request signal (refer to table 2-4).

Ⓓ Initiate Data Transfer. This bit must be set to a logic 1 by a CIO instruction before every RIO instruction to signal the interface PCA to accept another data word from the device. Bits 0 and 1 of the status word must also be set to a logic 1.

Ⓔ Device Control. These five control bits are available to the external device through differential line drivers.

Ⓕ Data Transfer Interrupt. A logic 1 allows the interface PCA to issue an Interrupt Request signal at the completion of each data transfer sequence.

Ⓖ Interrupt/Device Status. This bit selects the lower eight bits (8 through 15) of the status word. A logic 1 selects device status, and a logic 0 selects interrupt status.

Ⓗ Enable Byte Transfer. A logic 1 enables byte transfer for packing during read and unpacking during write.

Ⓘ Enable Interrupt Request. A logic 1 enables the Interrupt Request signal.

Ⓙ Enable Transfer Timer. A logic 1 enables the transfer timer.

1471004-176

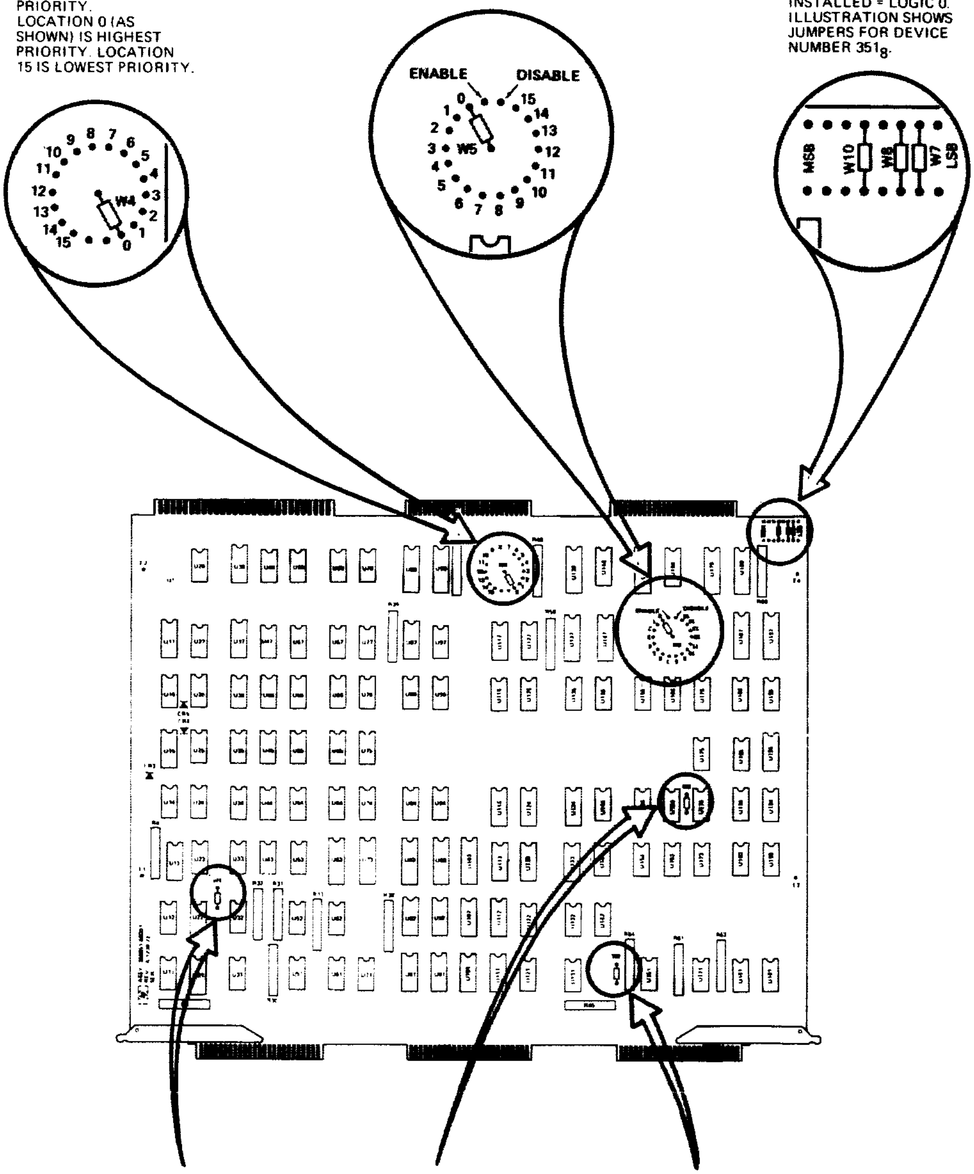
CONTROL WORD FORMAT

Sequence Counter Status Bit Decoding Table

STATUS BIT		DESCRIPTION
3	4	
0	0	Sequence counter at rest.
1	0	Request for operation to device.
1	1	Begin operation from device.
0	1	Request for operation to begin transfer of second byte.

Interrupt Request Selective Clear Table

CONTROL WORD BITS			INTERRUPT PROCESS CLEARED
2	3	4	
0	0	0	Inactive state, no action
0	0	1	Transfer Timer and Transfer Error, interrupt status bits 15 and 14
0	1	0	I/O System, interrupt status bit 13
0	1	1	Clear Interface, interrupt status bit 12
1	0	0	Data Transfer, interrupt status bit 11
1	0	1	Device Status bit 8, interrupt status bit 8
1	1	0	Device Status bit 9, interrupt status bit 9
1	1	1	Device Status bit 10, interrupt status bit 10



GROUP INTERRUPT
MASK. JUMPER SHOWN
IN LOCATION 0.

SERVICE REQUEST
PRIORITY.
LOCATION 0 (AS
SHOWN) IS HIGHEST
PRIORITY. LOCATION
15 IS LOWEST PRIORITY.

DEVICE NUMBER JUMPER
INSTALLED = LOGIC 0.
ILLUSTRATION SHOWS
JUMPERS FOR DEVICE
NUMBER 351_8.

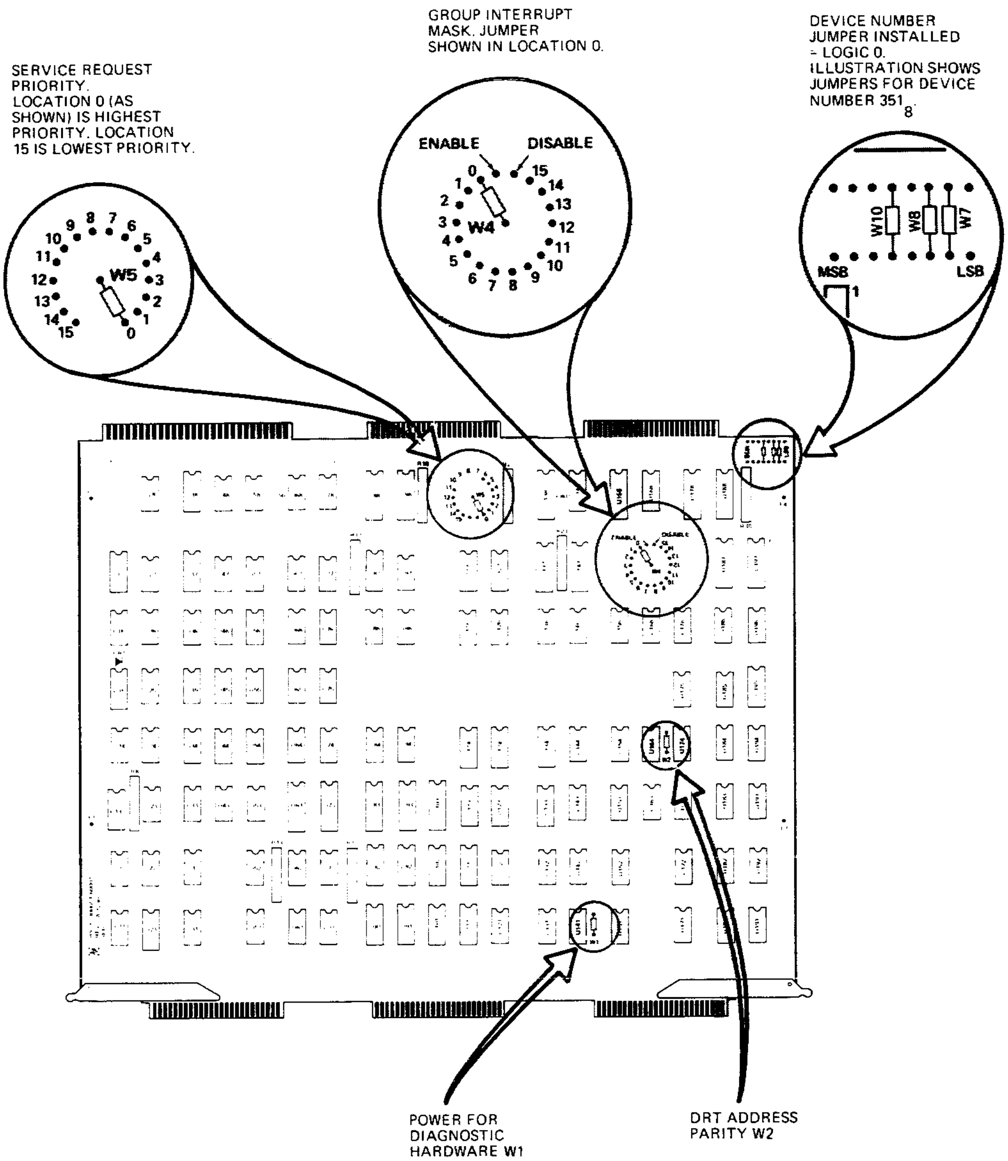
DIAGNOSTIC
HARDWARE
LOGIC W1.

DRT ADDRESS
PARITY W3.

POWER FOR
DIAGNOSTIC
HARDWARE W2.

1471004-177

INTERFACE PCA JUMPER WIRE LOCATIONS (30050A)



1471004-178

INTERFACE PCA JUMPER WIRE LOCATIONS (30051A)

DESIGNATION	PIN NO.		WITH JUMPER WIRE REMOVED (NORMAL)	WITH JUMPER WIRE INSTALLED
	FROM	TO		
J2W1	7	8	I/O program continues normally after program control strobe.	I/O program halts after a program control stobe and waits for Device Status Bit 11 to continue operation.
J2W2	9	10	Leading edge of Device Flag signal advances sequence counter from Count 1 to Count 2.	Trailing edge of Device Flag signal advances sequence counter from Count 1 to Count 2.
J2W3	11	12	Device Command signal operates in response mode.	Device Command signal operates in pulse mode.
J2W4	13	14	Inhibits Device Status Bit 8 from causing an interrupt request.	Permits interrupt request at trailing edge of Device Status Bit 8.
J2W5	15	16	Data input registers enabled by sequence counter counts 1 and 3.	Data input registers permanently enabled.
J2W6	21	22	Leading edge of Device Flag signal advances sequence counter from Count 2 to Count 3.	Trailing edge of Device Flag signal advances sequence counter from Count 2 to Count 3.
J2W7	25	26	Normal write transfer operation.	Test write transfer operation.
J2W8	35	36	Inhibits Device Status Bit 9 from causing an interrupt request.	Permits interrupt request at trailing edge of Device Status Bit 9.
J2W9	37	38	Inhibits Device Status Bit 10 from causing an interrupt request.	Permits interrupt request at leading edge of Device Status Bit 10.
J2W10	39	40	Device Command sginal not inverted.	Device Command signal logic inverted with respect to Data Out lines.

1471004-179

CONNECTOR J2 JUMPER WIRE FUNCTIONS

INTERFACE PCA SIGNALS TO CABLE CONNECTOR, sheet 1 of 2

MATING CONNECTOR PIN NO.	INTERFACE CARD CONNECTORS			
	PIN NO.	J1 FUNCTION	J2 FUNCTION	J3 FUNCTION
A1,B1	1,2	Device Status bit 8	Power Fail	Data Out bit 2
A2,B2	3,4	Device Flag	Power ON (PON), Ret	Data Out bit 4
A3,B3	5,6	Write Delay	Master Clear Delay, Ret	Control Word bit 6
A4,B4	7,8	Set Trans Err FF, Ret	Jumper Wire J2W1, Ret	Control Word bit 8
A5,B5	9,10	Device Status bit 10	Jumper Wire J2W2, Ret	Control Word bit 7
A6,B6	11,12	Device Status bit 9	Jumper Wire J2W3, Ret	Self-Test +5V, Ret
A7,B7	13,14	Data Out bit 13	Jumper Wire J2W4, Ret	Self-Test +5V, Ret
A8,B8	15,16	Data Out bit 12	Jumper Wire J2W5, Ret	Data Out bit 1
A9,B9	17,18	Data In bit 8	NC	Data Out bit 3
A10,B10	19,20	Data In bit 14	NC	Data Out bit 7
A11,B11	21,22	Data In bit 15	Jumper Wire J2W6, Ret	Data Out bit 5
A12,B12	23,24	Data In bit 12	NC	Data Out bit 6
A13,B13	25,26	Data In bit 13	Jumper Wire J2W7, Ret	Data Out bit 0
A14,B14	27,28	Data In bit 10	NC	Device Status bit 12
A15,B15	29,30	Data In bit 11	NC	Data In bit 7
A16,B16	31,32	Data In bit 9	NC	Data In bit 6
A17,B17	33,34	Data Out bit 8	NC	Data In bit 4
A18,B18	35,36	Self-Test Logic, NC	Jumper Wire J2W8, Ret	Data In bit 5
A19,B19	37,38	Control Word bit 10	Jumper Wire J2W9, Ret	Device Status bit 14
A20,B20	39,40	Device Command	Jumper Wire J2W10, Ret	Data In bit 1
A21,B21	41,42	Data Out bit 15	Control Word bit 9	Data In bit 0

471004-180, 1 of 2

INTERFACE PCA SIGNALS TO CABLE CONNECTOR, sheet 2 of 2

MATING CONNECTOR PIN NO.	INTERFACE CARD CONNECTORS			
	PIN NO.	J1 FUNCTION	J2 FUNCTION	J3 FUNCTION
A22,B22	43,44	Data Out bit 14	Master Clear	Device Status bit 15
A23,B23	45,46	Data Out bit 9	Device Status bit 11	Data In bit 3
A24,B24	47,48	Data Out bit 10	Clear Interface	Data In bit 2
A25,B25	49,50	Data Out bit 11	Device End	Device Status bit 13

NOTES:

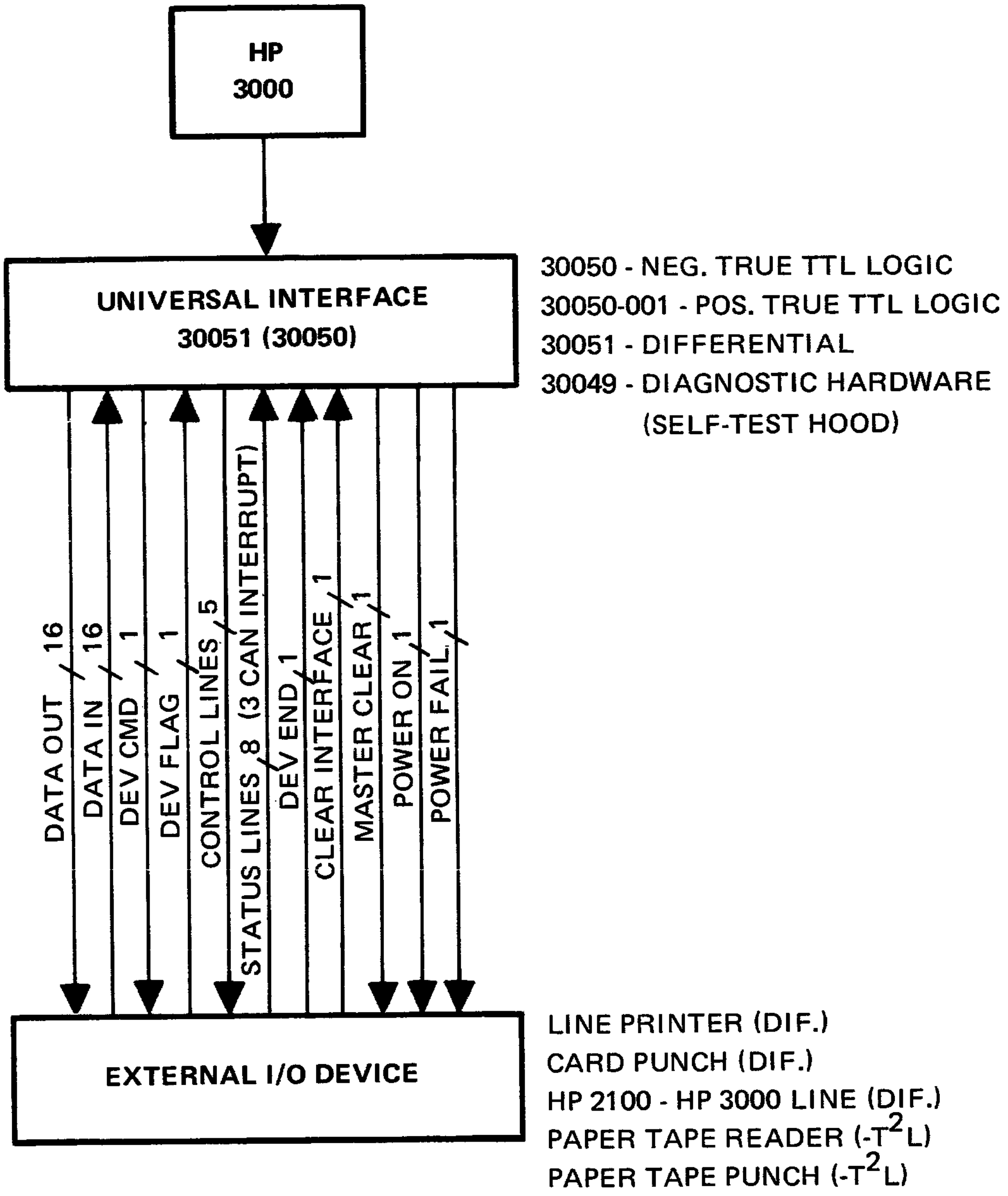
1. Functions listed are for PCA's with positive-true logic, part no. 30050-60003. For PCA's with negative-true logic, part no. 30050-60001, add an inversion line over each function name.

2. In the pin no. columns, signal connections are listed first with the common return connection for the same signal listed following the comma. All even numbered pins are connected together.

3. When used, jumper wires are connected in the mating connector hood between the two pins listed on the same line.

4. Abbreviation NC indicates no connection.

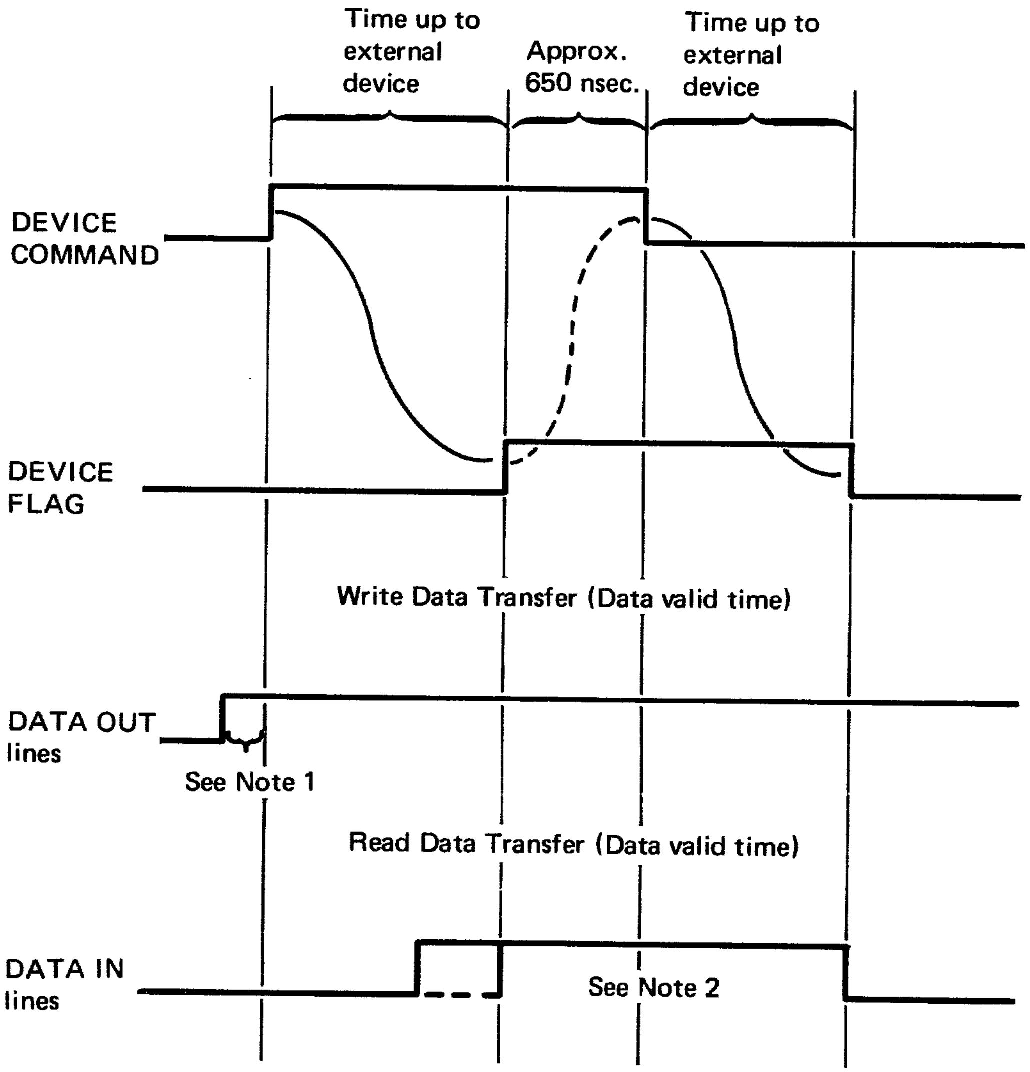
471004-180, 2 of 2



1471004-181

INTERFACE–DEVICE CONTROL SIGNALS

MODES OF OPERATION-"HANDSHAKE"



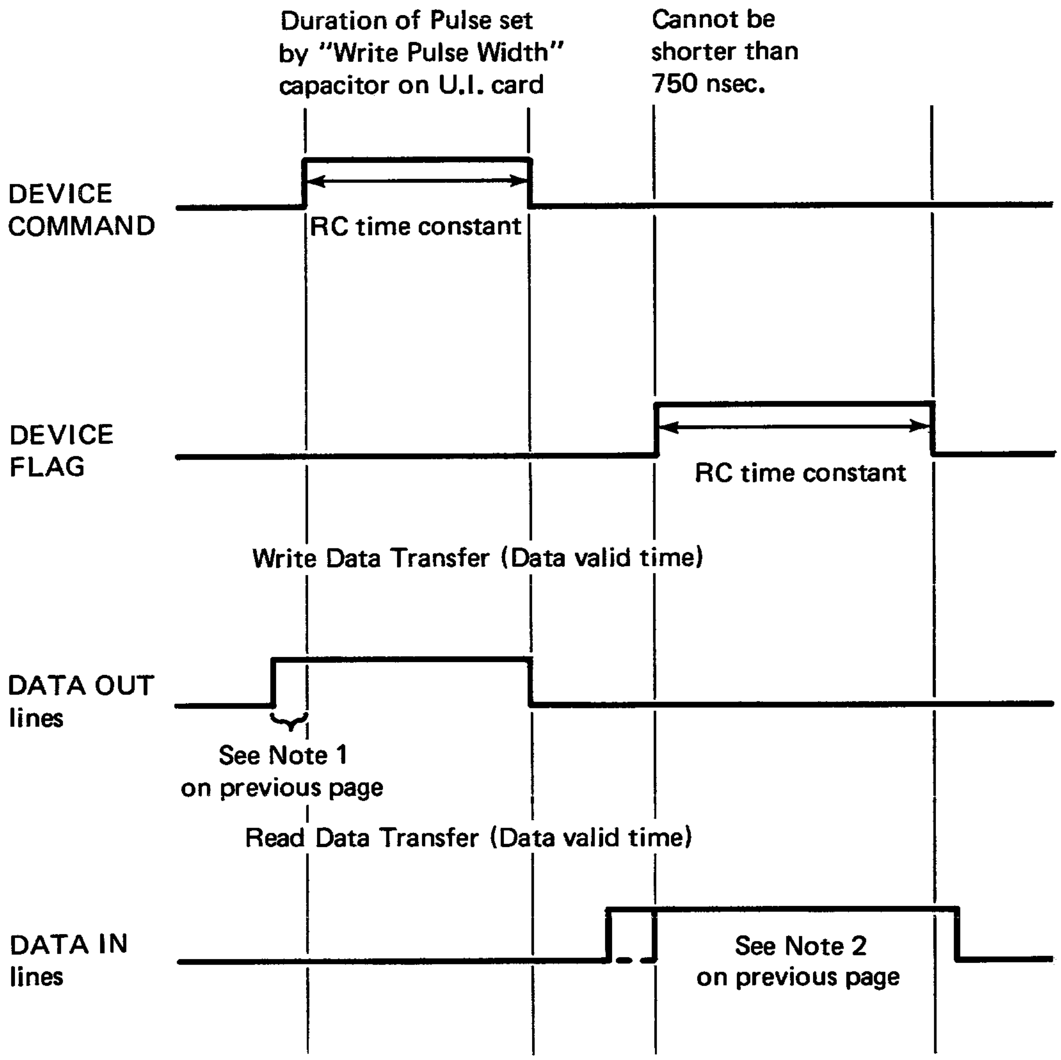
Note 1: Data is out on the lines at least 200 nsec. min. before the DEVICE COMMAND lines goes high. This period of time can be controlled by changing the value of a capacitor in a delay circuit on the board. The DATA OUT lines are valid until the next data transfer is initiated. During a read DATA TRANSFER the DATA OUT lines remain stable.

Note 2: If jumper W4 (DATA WINDOW ON/OFF) is off, the data is strobed into the U.I. card's data register approximately 650 nsec. after the edge of the DEV. FLAG line specified by jumper W3. (If W3 off, it will be the leading edge; W3 on, trailing edge.) The data must be stable at least for about 750 nsec. after the DEV FLAG is asserted for proper loading into buffer. If jumper W4 is on, the U.I. will return whatever is currently present on the data in lines whenever a read instruction is requested.

1471004-182, 1 of 2

PARALLEL DATA TRANSFER, sheet 1 of 2

MODES OF OPERATION-"PLUS MODE"(JUMPER W3 AND W9 OFF)



Note: These time constants are true only if capacitor on the DEV FLAG receiver is 100 pf.

1471004–182, 2 of 2

PARALLEL DATA TRANSFER, sheet 2 of 2

UNIVERSAL INTERFACE S-A
30050A/30051A

1. COLD LOAD DIAG FILE # FROM NON-CPU COLD LOAD TAPE
   D100 UNIV INTERFACE TEST (HP32335A.NN.N) DEVICE = XXX
   *IF THE DIAG WAS PRECONFIGURED, EXECUTION BEGINS, OTHERWISE THE FOLLOWING CONFIGURATION ROUTINE IS ENTERED.
2. Q110 DEVICE NUMBER? XX OR %XX((DRT # (DECIMAL OR OCTAL)))
3. Q111 INTERRUPT MASK? D, E, OR 0 THRU 15
4. Q112 NEGATIVE TRUE? Y OR N
5. P113 INTERNAL SWITCH REGISTER ((SET SWITCHES - PRESS))
6. Q114 SECTION LIST? X,X,X,X,X ((WHATEVER))
7. D102 END OF SECTION

SWITCH REGISTER OPTIONS:

0 SELECT EXTERNAL REGISTER
1-3 SPECIFY A NUM OF WDS XFERRED IN STEP 320 & 321
4 SHORT PRINT
5 ADD SECTION TO SECTIONS LIST - VALID IN ESR
6 DELETE SECTION FROM SECTIONS LIST - VALID IN ESR
7 SKIP TO END OF SECTION - VALID IN ESR MODE ONLY
8 PRINT ALL MSG´S EXCEPT E6, E10, AND E12
9 PRINT D AND E CLASS MSG´S TO THE LINE PRINTER
10 HALT AT THE END OF SECTION
11 SUPPRESS ALL MSG´S
12 HALT AT THE COMPLETION OF DIAG CYCLE
13 LOOP ON CURRENT STEP
14 HALT ON ERROR
15 HALT AT END OF STEP

SECTION NUMBER OPTIONS:

0 CONFIGURATION
1 HP30049B USER CHECKS
2 HP30049B PROGRAM CHECKS
3 DATA XFER AND DEVICE STATUS BYTE TEST
4 DEVICE STATUS INTERRUPT BIT TEST
5 INTERFACE INTERRUPT STATUS BIT TEST
6 INTERRUPT TEST
7 SIO TEST
8 SIO-DEVICE END TEST
9 JUMPER OPTION TEST
10 BASIC FUNCTIONS
11 WRITE-READ FUNCTIONS
12 DEVICE END FUNCTIONS
13 N/A
14 RETURN TO S-A RELOCATING LOADER
15 HALT AT THE END OF SPECIFIC STEP

CODED HALT TABLE:

HALT #	CIR	DEFINITION
0	%30360	UNEXPECTED EXTERNAL INTERRUPT
4	%30364	SYSTEM CLOCK ERROR
6	%30366	SET INTERNAL REGISTER
7	%30367	OBSERVE LAMPS ON HP30049B
10	%30370	CHECK JUMPERS ON HP30049B
11	%30371	CHECK DEV END ON HP30049B
12	%30372	PRESS I/O RESET, CHECK CONT 6 & 7 ON HP3049B FOR OFF
13	%30373	CHECK PINS ON HP30049B
14	%30374	SECTION UU HAS FINISHED - (SEE RA, RB RC, RD)
15	%30375	STEP SSS HAS FINISHED - (SEE RA, RB, RC, RD)
		RA = SECTION OR STEP NUMBER RB = INTERRUPT STATUS WORD RC = DATA WORD READ, WHERE APPLICABLE RD = DATA WORD WRITTEN, WHERE APPLICABLE
16	%30376	PROGRAM ERROR (SEE RA, RB, RC, RD)
17	%30377	END OF PASS

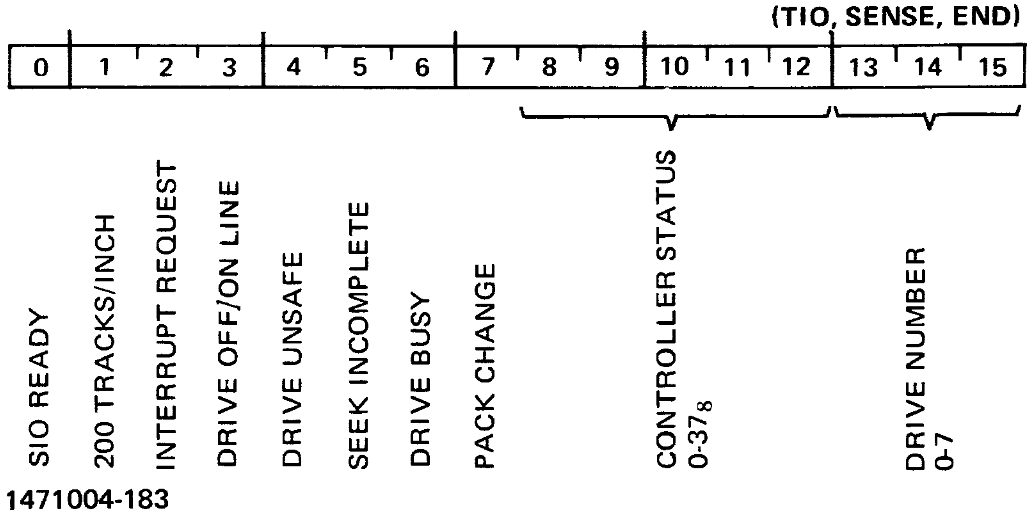
DISC FILE
30102A/30202A/2888A

DIFFERENCES FROM SERIES II

Sometimes this interface is configured for the Sel-Chan only on 3000 pre Series II systems.

DEVNO must be 5 if configured as System Disc.

DISC FILE 2888

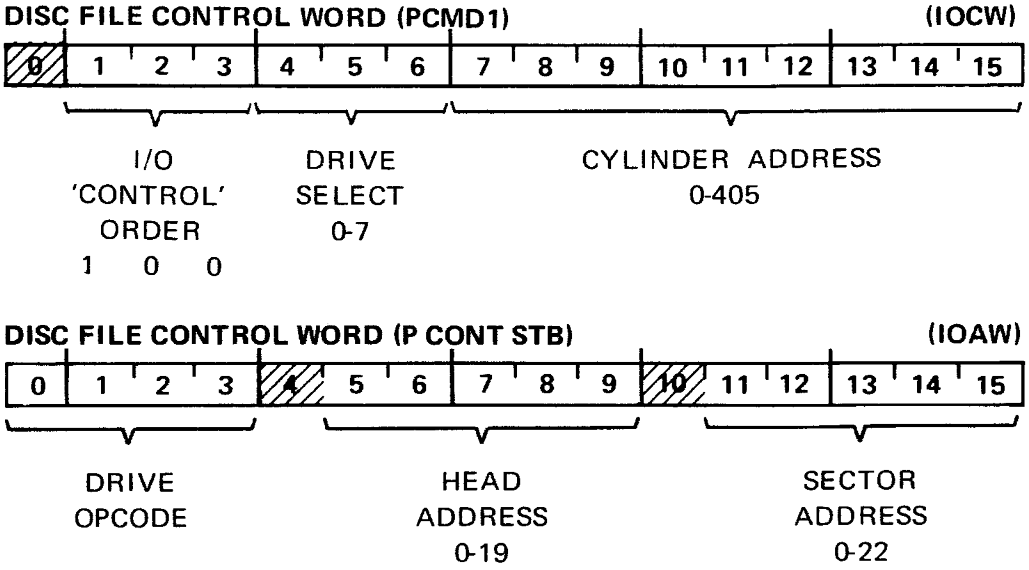


DISC FILE STATUS WORD

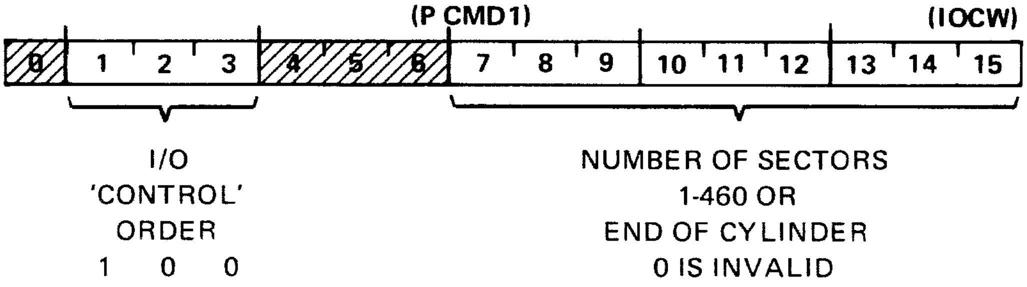
8	9	10	11	12	
0	0	0	0	0	ERROR FREE
0	0	0	0	1	ILLEGAL OPCODE
0	0	0	1	1	CYLINDER NUMBER > 405
0	0	1	0	0	HEAD NUMBER > 19
0	0	1	0	1	TIME-OUT, SEARCH FOR ADDRESS (HEAD, SECTOR) > 100 ms
0	0	1	1	0	DEFECTIVE TRACK ADDRESSED
0	0	1	1	1	HEADS MISPOSITIONED
0	1	0	0	0	CYCLIC ERROR IN ADDRESS FIELD
0	1	0	0	1	CYCLIC ERROR IN DATA FIELD
0	1	0	1	0	I/O PROGRAM ERROR
0	1	0	1	1	SEQUENCE ERROR – DATA FIELD DOES NOT FOLLOW AN ADDRESS FIELD DURING SEARCH
0	1	1	0	0	CYLINDER OVERRUN
0	1	1	0	1	ZERO SECTOR COUNT IN CYCLIC CHECK OPCODE
0	1	1	1	0	DATA OVERRUN
1	0	0	0	0	ILLEGAL TERMINATION – I/O TERMINATED BEFORE COMPLETING A READ OR WRITE ADDRESS
1	0	0	1	1	DRIVE ERROR
1	0	1	0	0	TRANSFER ERROR
1	1	1	1	1	DRIVE ATTENTION

1471004-184

CONTROLLER STATUS



When the drive opcode is a 'Cyclic Check,' a second IOCW is required containing the number of sectors to be checked. The second IOAW in this case is ignored.



1471004-185

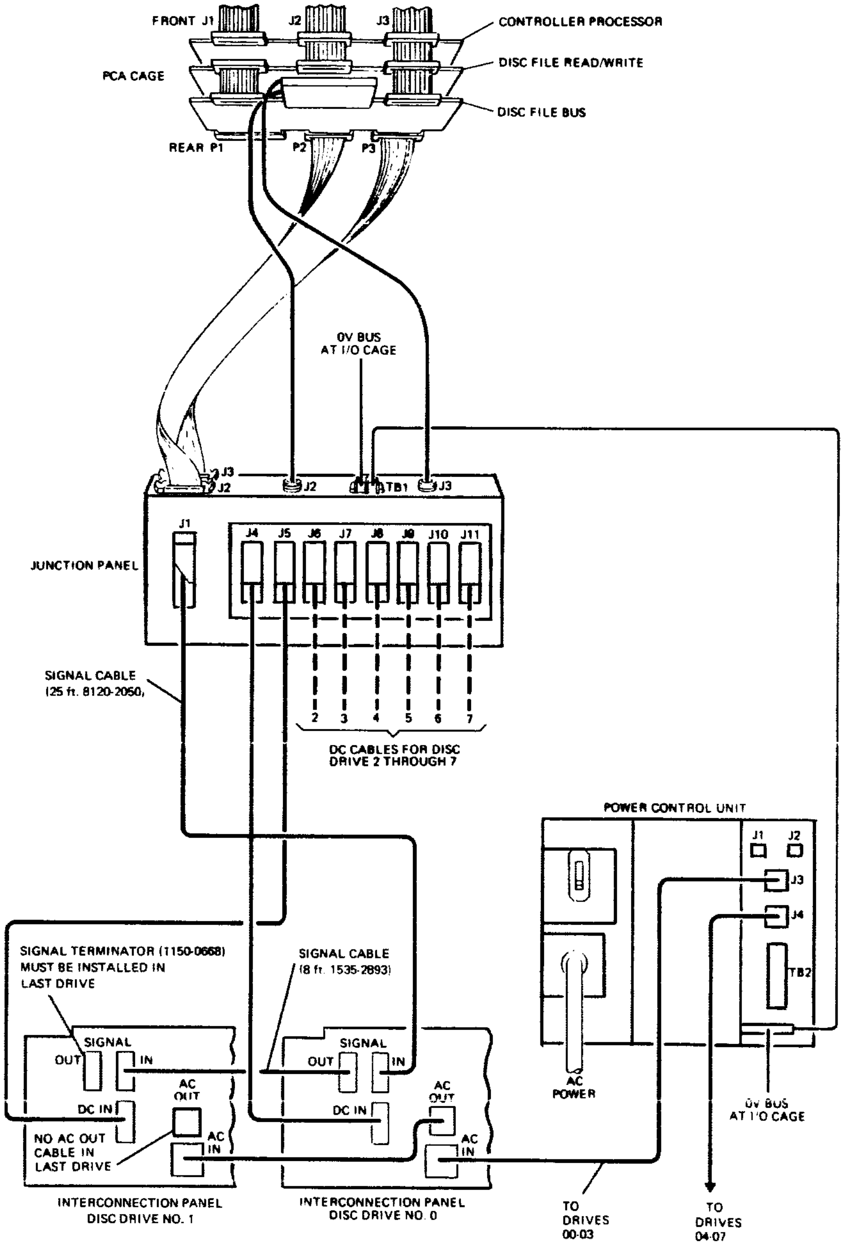
DISC FILE CONTROL WORDS

	0	1	2	3	
CLR	0	0	0	0	COLD LOAD READ
RC	0	0	0	1	RECALIBRATE
SEEK	0	0	1	0	SEEK
SC	0	0	1	1	STATUS CHECK
RA	0	1	0	0	READ ADDRESS
RD	0	1	0	1	READ DATA
*RFS	0	1	1	0	READ FULL SECTOR
CC	0	1	1	1	CYCLIC CHECK
WD	1	0	0	0	WRITE DATA
*WFS	1	0	0	1	WRITE FULL SECTOR
*SA	1	0	1	0	SKIP ADDRESS - READ DATA
WA	1	0	1	1	WRITE ADDRESS
*PCT	1	1	0	0	PACK CERTIFICATION

*For diagnosing purposes.

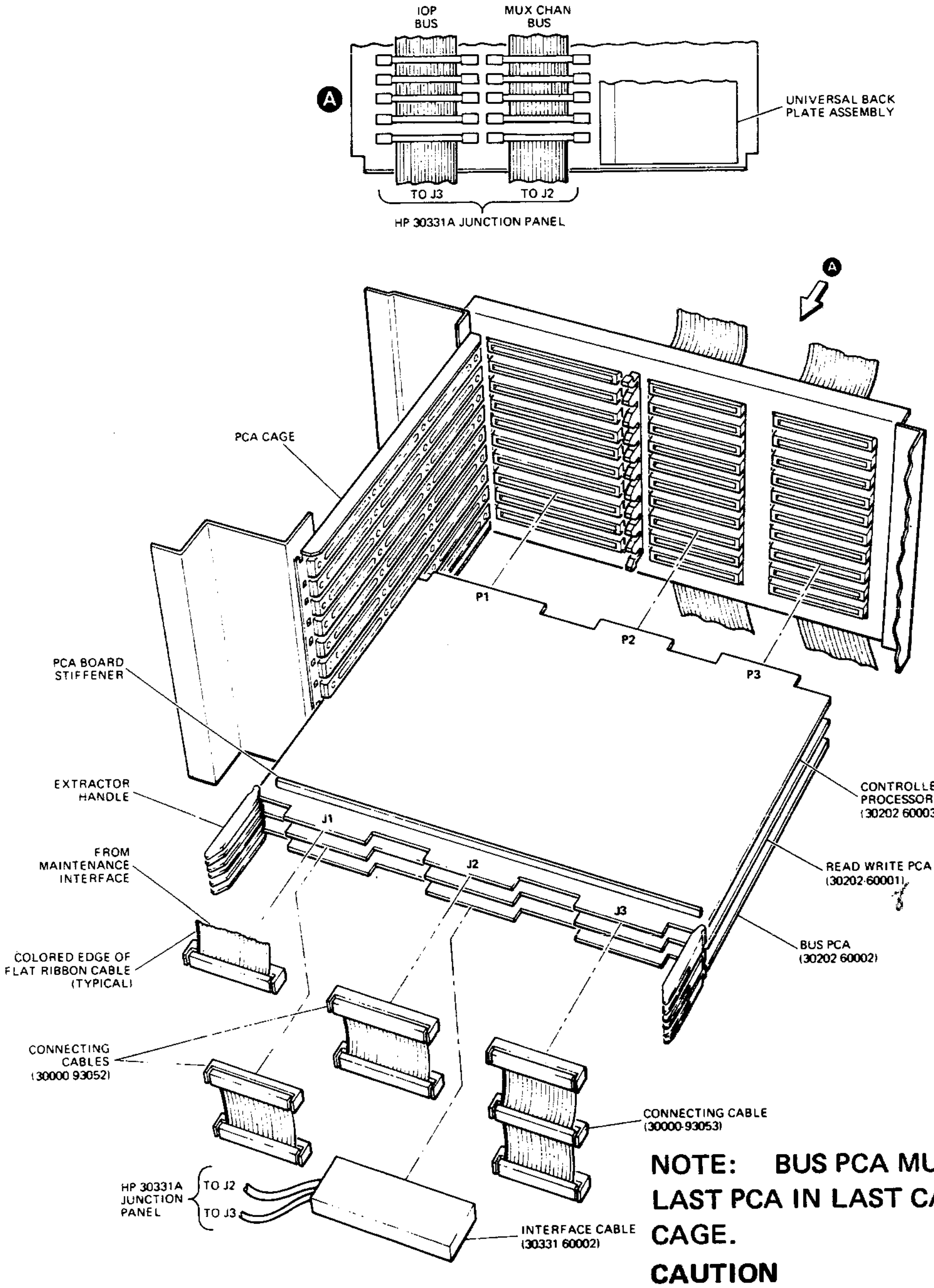
1471004-186

DRIVE OPCODE



1471004-187

30102A DISC FILE SUBSYSTEM, CABLING ARRANGEMENT



NOTE: BUS PCA MUST BE LAST PCA IN LAST CARD CAGE.

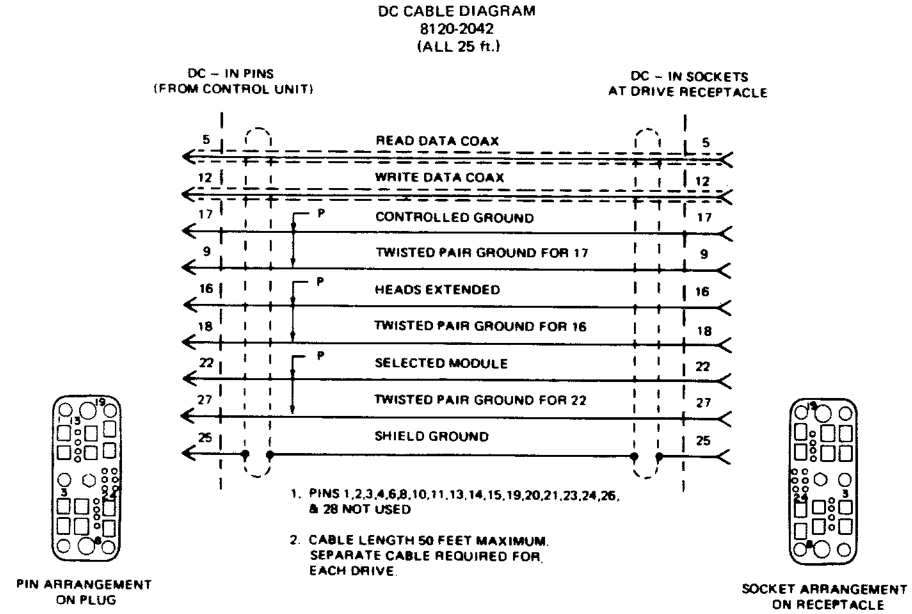
CAUTION

30V PRESENT ON BUS PCA P2

30202A Disc File Interface
PCA Position and Connection Details

1471004-188

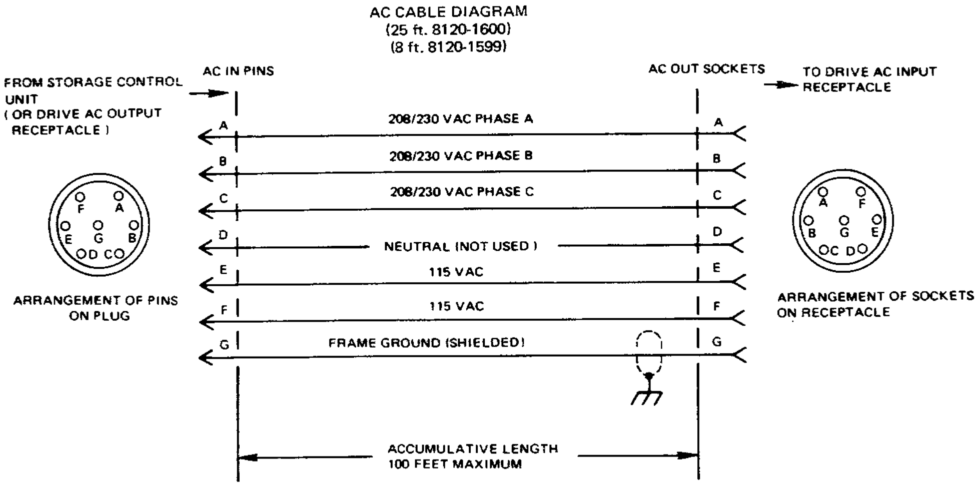
30202A DISC FILE INTERFACE BOARDS POSITIONS AND CONNECTIONS



1. PINS 1,2,3,4,6,8,10,11,13,14,15,19,20,21,23,24,26, & 28 NOT USED
2. CABLE LENGTH 50 FEET MAXIMUM. SEPARATE CABLE REQUIRED FOR EACH DRIVE.

1471004-189

DC CABLE DIAGRAM

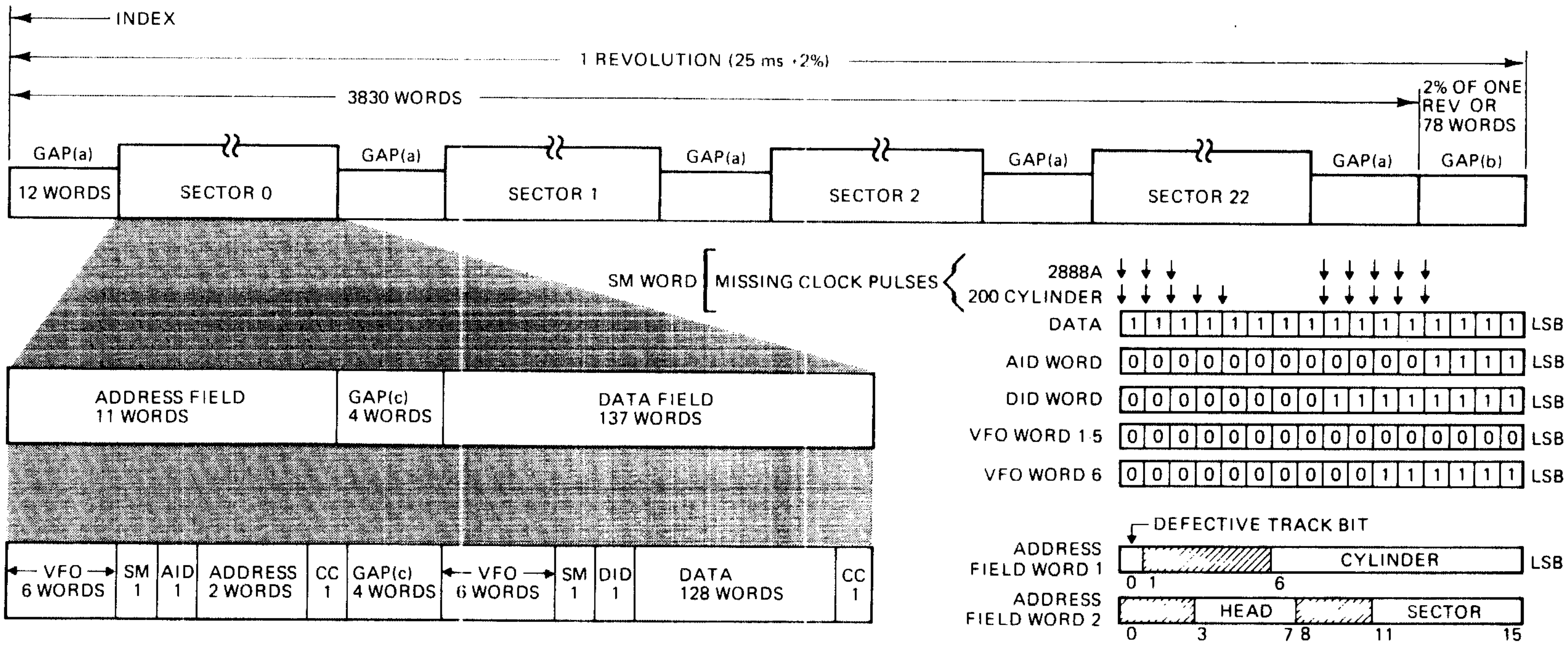


NOTES

1. CABLE LENGTHS MAY VARY FOR A GIVEN NUMBER OF DRIVES INSTALLED IN A SUBSYSTEM
2. PHASES AT PINS A, B, & C WILL VARY DEPENDING UPON RELATIVE POSITION OF DRIVE TO OTHER DRIVES IN SUBSYSTEM
3. SHIELD OF PIN G IS TIED TO SHELL OF CONNECTORS

1471004-190

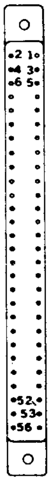
AC CABLE DIAGRAM



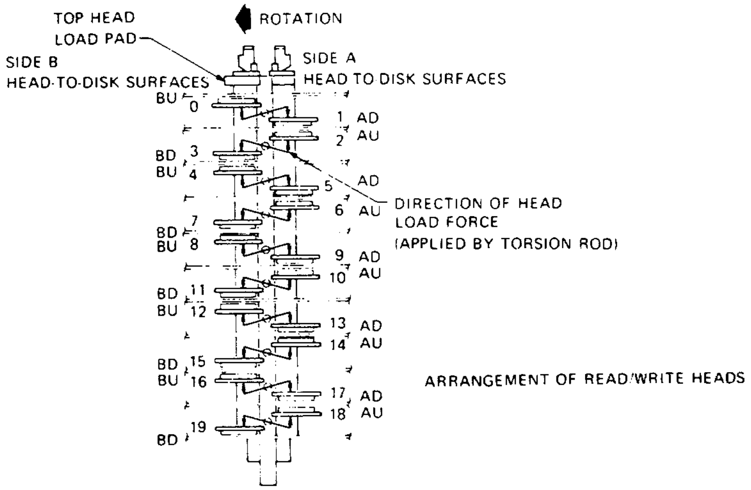
GAP(a), (b), (c), (d) FILLED WITH ONES
GAP(a) > (5 WORDS + 6% OF PREVIOUS SECTOR)

1471004-191

DISC PACK RECORDING FORMAT

GATE POS.	PART NUMBER	PWA TITLE
1	INTERFACE	READ/WRITE PADDLE
2	75000003-X	SELECT 0-9
3	75000068-X	SELECT 10-19
4	75000004-X	WRITE
5	75003548-X	READ
6	75003978-X	DEFECT DETECTOR
7	INTERFACE	SCU SIGNAL PADDLE
8	75004483-X	HEAD ADDRESS REGISTER (HAR)
9	75003727-X	CYLINDER ADDRESS REGISTER (CAR)
10	INTERFACE	DIAG UNIT DISPLAY PADDLE
11	NOT USED	
12	75000011-X	FILE STATUS
13	75003728-X	DIFFERENCE COUNTER
14	75003370-X	ACCESS CONTROL
15	75002523-X	CURVE GENERATOR
16	75000070-X	LOGICAL ADDRESSING
17	75000015-X	INDEX TRANSDUCER
18	75004139-X	TEMPERATURE COMP & SAFETY
19	INTERFACE	TRANSDUCER PADDLE
20	75003713-X	CYLINDER DETECTOR
21	75002521-X	AUTOMATIC GAIN CONTROL (AGC)
22	NOT USED	
23	75003719-X	TACHOMETER
24	75003720-X	PULSER AND SUMMING AMP
25	75004138-X	CYLINDER SELECTOR
26	INTERFACE	PWR SEQ AND PULSER PADDLE
27	75000019-X	POWER CONTROL
*28	75000065-X	MATRIX A
*29	75000065-X	MATRIX B

*These PWA's located on CAM Tower Assembly.



ARRANGEMENT OF READ/WRITE HEADS

BD 1150-0657	AD 1150-0659
BU 1150-0658	AU 1150-0660

1471004-192

PWA ASSIGNMENTS IN ELECTRONIC GATE

DISC/FILE READ/WRITE PCA JUMPER DESCRIPTION

DESIGNATION	SIO MUX	SEL CHAN
W1	OUT	IN
W2	SIO	CHAN
W3	SIO	CHAN
W4	DEVICE NUMBER ODD PARITY JUMPER	
W5	OUT	IN
W6 - W13	DEVICE NUMBER	
W14	INTERRUPT MASK IN ENABLE	
W15	SIO MUX SR NUMBER	CH
W16	IN	OUT

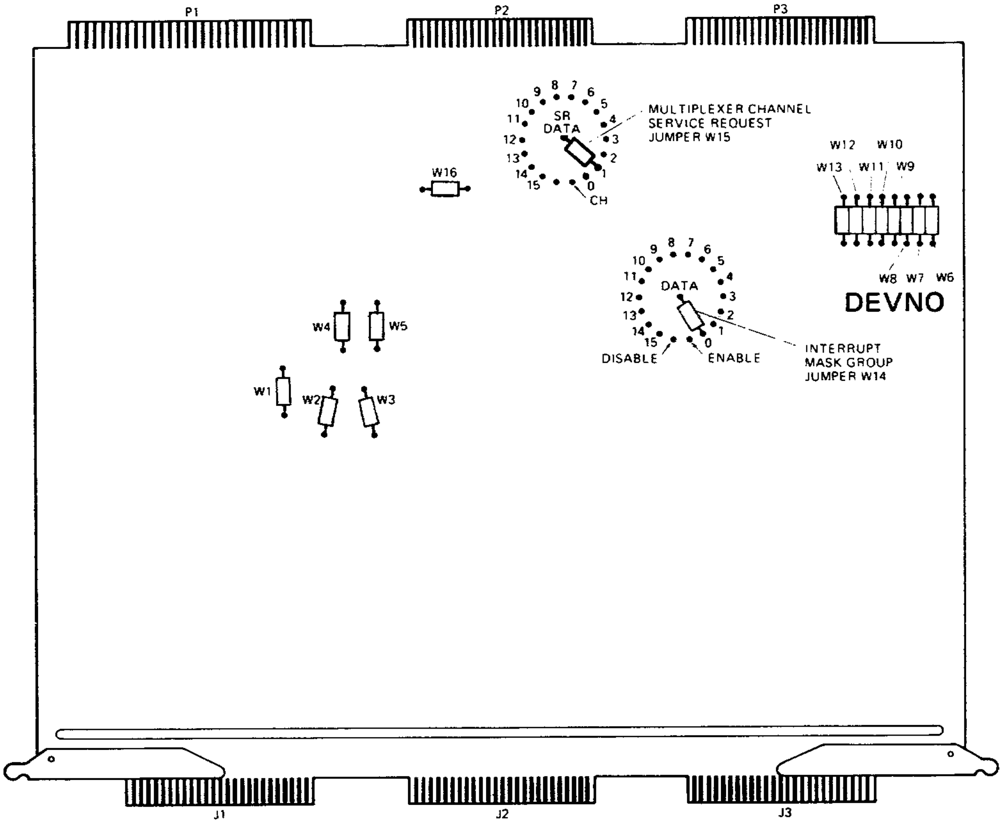
CIRCUIT SIDE
ACTIVE FF
MUX
U48 PIN 5 TO U58 PIN 11
SEL CHAN
U58 PIN 11 TO U58 PIN 13

NOTE

SIO MUX JUMPER MUST BE OUT FOR SEL CHAN OPERATION AND CONVERSELY

2888 MODULE PLUG PART NUMBERS

(UNIT NO.)
0 - HP1258-0106
1 - HP1258-0107
2 - HP1258-0108
3 - HP1258-0109
4 - HP1258-0110
5 - HP1258-0111
6 - HP1258-0104
7 - HP1258-0105



471004-194

JUMPER POSITIONS

DIAGNOSTIC STAND-ALONE

DISC FILE
30102A/2888A

1. COLD LOAD DIAG FILE # FROM NON-CPU COLD LOAD TAPE
   D99 01 DISC FILE (30102A) DIAG CONFG (HP32323A.NN.N)
2. Q99 02 WHAT IS DEVICE NUMBER? XX ((DRT # (DECIMAL)))
3. Q99 03 INTERRUPTS ON OR OFF? ON OR OFF
4. P61 04 PAUSE AFTER CONFIGURATION
   *SET SWITCH OPTIONS FOLLOWED BY CR TO START DIAG

SWITCH REGISTER OPTIONS:

0	SELECT EXTERNAL REGISTER
1	SET UP AND IGNORE DEFECTIVE TRACKS
2	SHORTEN TEST BY 40%
3	OPERATOR DESIGN
4	SHORTEN TEST SEVERELY
5	RESTRICT CYLINDERS
6	CHANGE UNIT #, CYLINDER, PATTERN, AND/OR HEAD TABLES
7	REPEAT CURRENT SECTION
8	SHORT PRINT
9	PAUSE AFTER CURRENT SECTION
10	SUPPRESS D-CLASS MSG´S
11	SUPPRESS ALL MSG´S, HALT ON P-CLASS MSG´S
12	PAUSE AFTER COMPLETED DIAG CYCLE
13	LOOP ON CURRENT STEP
14	PAUSE ON ERROR
15	PAUSE ON END OF CURRENT STEP

FORMAT INSTRUCTIONS

```
SD (UNIT NO.)
LB NN
IT
WAI
RT NN,8119
EN
```

DIAGNOSTIC ONLINE

DISC FILE ONLINE
30102A/2888A

```
*NEW DISC        ((WHATEVER))
PROGRAM FILE?   PD360A.XXXXXX.XXXXXX
DEVICE?      XX  ((DECIMAL NO. OF DRT))
SET FLAGS    X,X,X,X,X ((WHATEVER))
D99 1 DISC FILE (30102A) DIAGNOSTIC CONFIGURATION
  (HP 32360A.X.X)
*SAVE DISC        ((SAVES IT INTO PST))
*ON AND RUN OR RUN DISC
D99 7 DISC (30102A) DIAGNOSTIC ON-LINE (HP 32360A.X.X)
D99 2 WHAT IS MODE (A=CONTROLLER B=FILE SYSTEM)?
```

FLAG	FUNCTION IF SET
1-5	SECTION FLAGS
6-10	NOT USED
11	IGNORE DEFECTIVE TRACKS
12	SHORT TEST (60% AS LONG)
13	SECTION 6 OP DESIGN
14	SEVERELY SHORTENED TEST (10% AS LONG)
15	RESTRICT CYLINDERS
16	CHANGE UNIT NUMBER TABLE
17	PAUSE AFTER PASS
18	PAUSE AFTER CURRENT SECTION
19	PAUSE AT END OF ERROR REPORT
20	DUMP STATUS OBTAINED FROM ERROR
21	DUMP CURRENT SIO PROGRAM
CS	REPEAT CURRENT SECTION
SP	SHORT PRINT
EP	SUPPRESS D-CLASS MESSAGES
NP	SUPPRESS ALL MESSAGES
LP	LOOP ON CURRENT STEP
PE	PAUSE ON ERROR
PA	PAUSE AT END OF CURRENT STEP

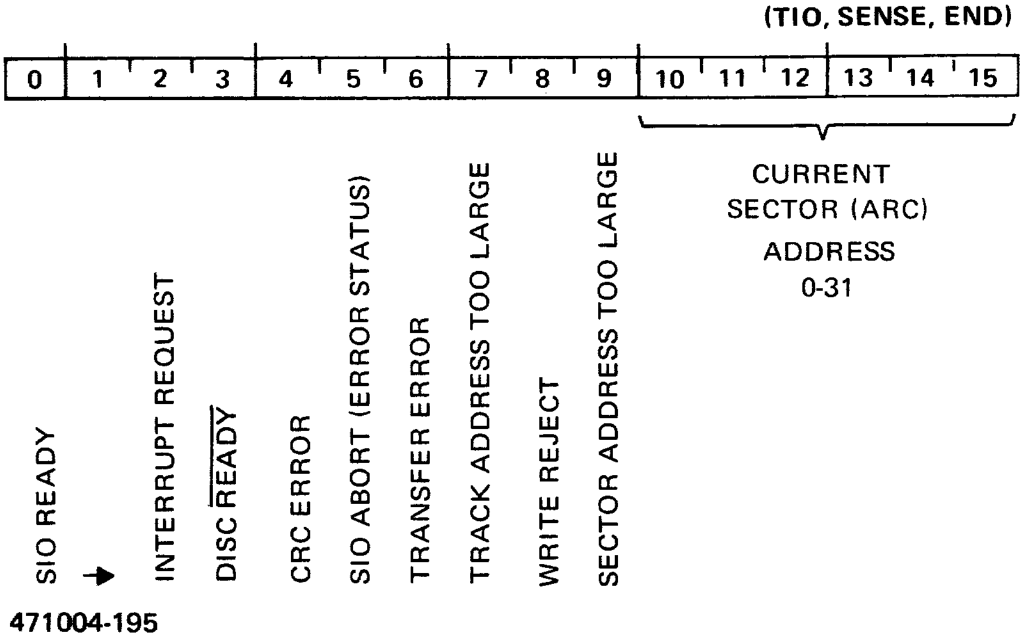
FIXED HEAD DISC
30103A/30203A/2660A

DIFFERENCES FROM SERIES II

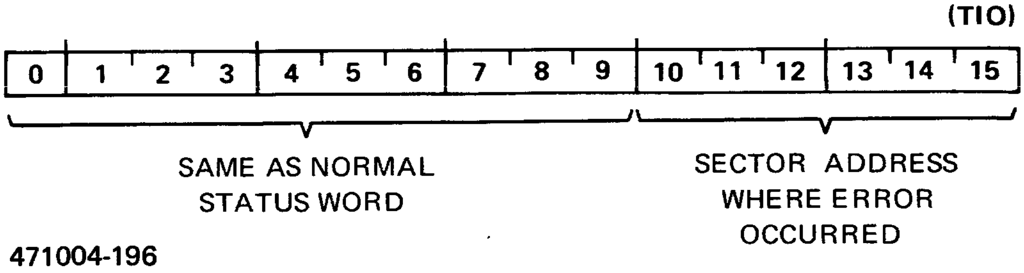
Sometimes this interface is configured to run on the SIO MUX channel for pre Series II.

2M Byte versions are not supported on Series II.

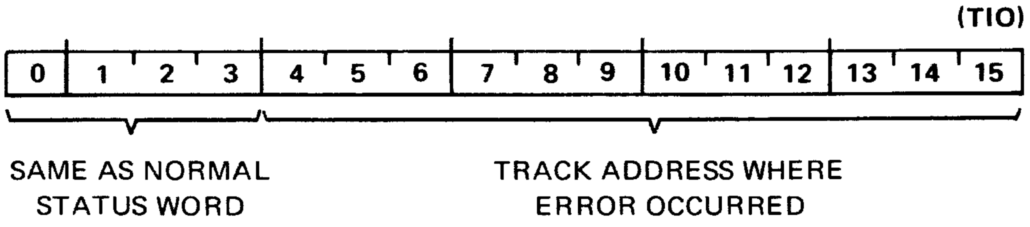
DEVNO must be 5 if configured as System Disc.



FIXED HEAD DISC STATUS WORD

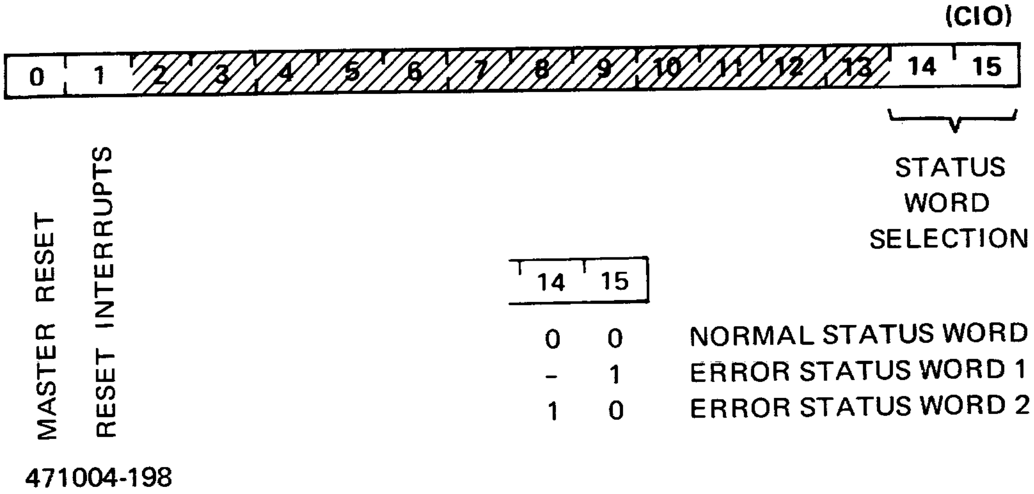


FIXED HEAD DISC ERROR STATUS WORD 1



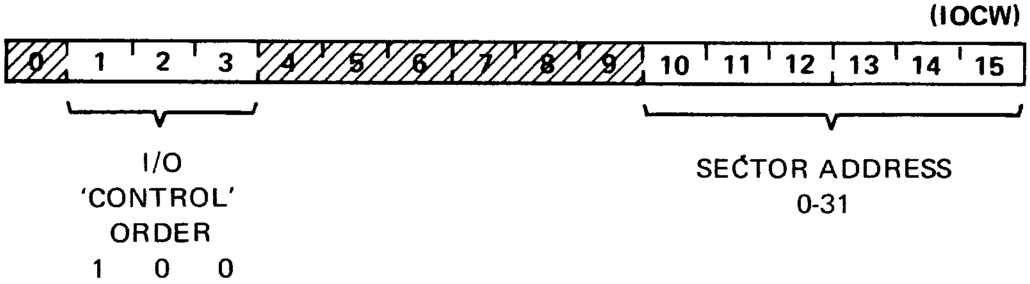
471004-197

FIXED HEAD DISC ERROR STATUS WORD 2



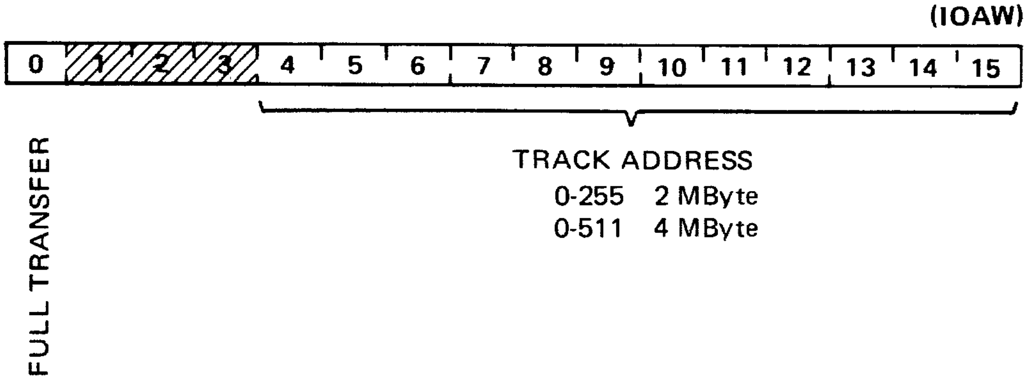
14	15	
0	0	NORMAL STATUS WORD
-	1	ERROR STATUS WORD 1
1	0	ERROR STATUS WORD 2

FIXED HEAD DISC CONTROL WORD



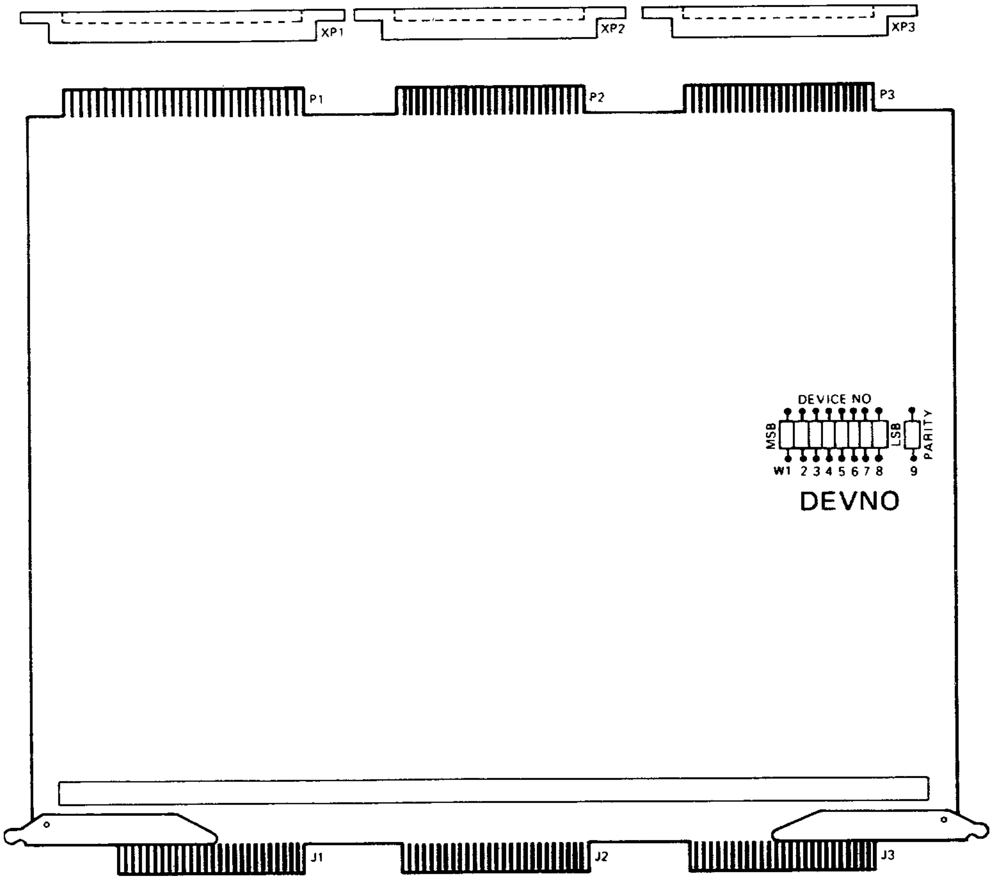
471004-199

FIXED HEAD DISC CONTROL WORD (P CMD 1)



471004-200

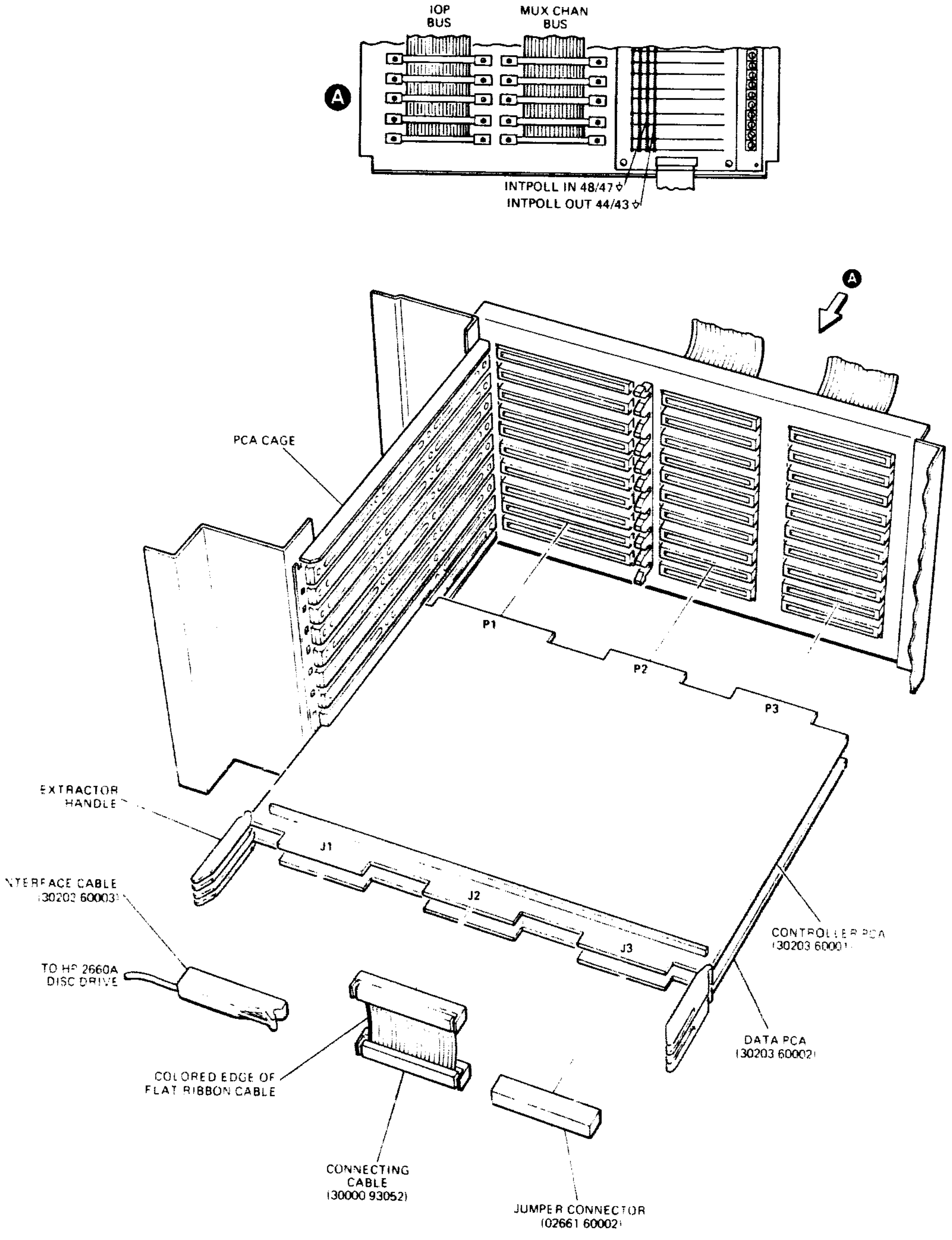
FIXED HEAD DISC CONTROL WORD (P CONT STB)



	DATA PCA JUMPERS
W1-W8	DEVNO JUMPERS
W9	DEVNO PARITY

471004-201

DISC MEM. DATA PCA JUMPER POSITIONS



1471004-202

PCA AND CABLES INSTALLATION DIAGRAM

Table FIXEDHD-1.
Data PCA Connector J1 and Device Cable Signal List

	CABLE		
PCA J1	P1 (PCA)	P2 (DEVICE)	SIGNAL
1	1A	D	TO(-)
2	1B	B	TO(+)
3	2A	E	AC(+)
4	2B	H	AC(-)
5	3A	L	W(+)
6	3B	N	W(-)
7	4A	A	DR(+)
8	4B	C	DR(-)
9	5A	P	R(+)
10	5B	S	R(-)
11	6A	J	WC(-)
12	6B	F	WC(+)
13	7A	-	-
14	7B	-	-
15	8A	-	-
16	8B	-	-
17	9A	K	-
18	9B	M	-
19	10A	f	BL6(-)
20	10B	d	BL6(+)
21	11A	X	BL2(-)
22	11B	V	BL2(+)
23	12A	k	BL7(-)
24	12B	h	BL7(+)
25	13A	a	BL3(-)
26	13B	Y	BL3(+)
27	14A	Z	BL4(+)
28	14B	b	BL4(-)
29	15A	R	BL0(+)
30	15B	T	BL0(-)
31	16A	c	BL5(+)
32	16B	e	BL5(-)
33	17A	U	BL1(+)
34	17B	W	BL1(-)
35	18A	S	BL10(-)
36	18B	p	BL10(+)
37	19A	w	BL12(-)
38	19B	u	BL12(+)
39	20A	AA	BL14(-)
40	20B	y	BL14(+)
41	21A	v	BL11(-)
42	21B	t	BL11(+)
43	22A	DD	BL15(-)
44	22B	BB	BL15(+)
45	23A	n	BL9(+)
46	23B	r	BL9(-)
47	24A	j	BL8(+)
48	24B	m	BL8(-)
49	25A	x	BL13(+)
50	25B	Z	BL13(-)

Table FIXEDHD-2. Data PCA Connector J3 Signal List

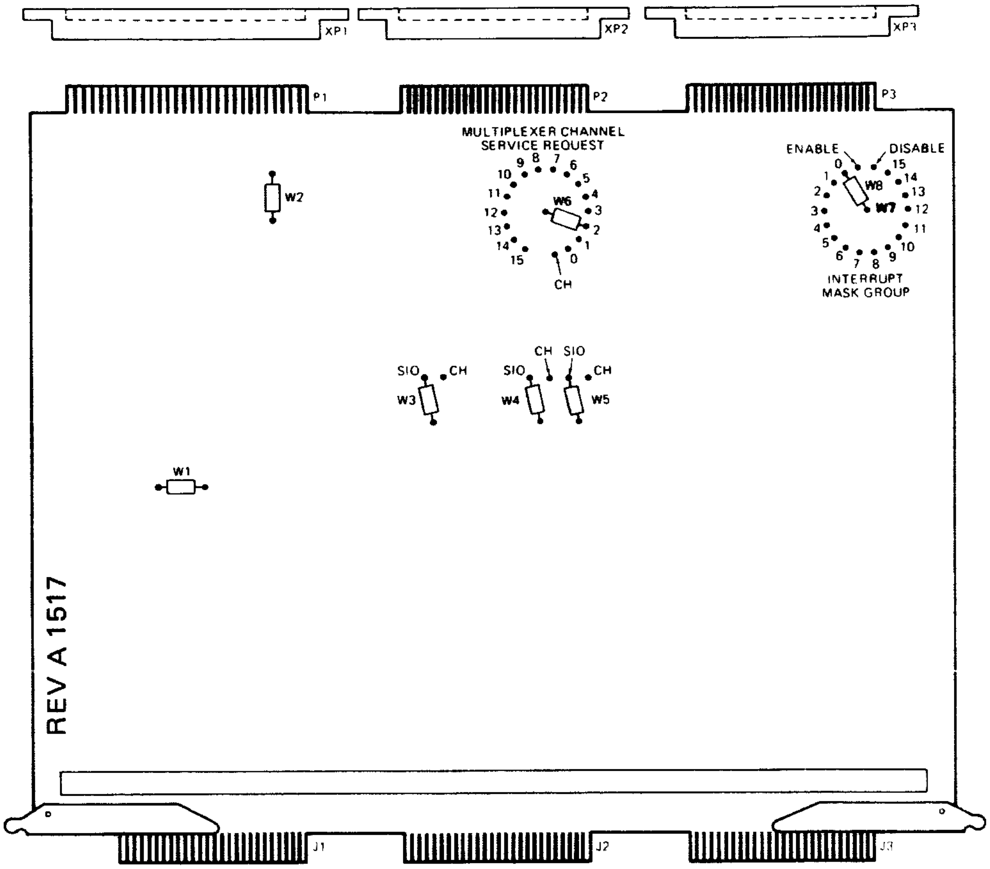
PIN NO.	SIGNAL	PIN NO.	SIGNAL
1	TRACK PROT 6	26	*2
2	*2	27	*1
3	TRACK PROT 7	28	*2
4	*2	29	*1
5	TRACK PROT 8	30	*2
6	*2	31	*1
7	TRACK PROT 9	32	*2
8	*2	33	*1
9	TRACK PROT 10	34	*2
10	*2	35	*1
11	TRACK PROT 11	36	*2
12	*2	37	*1
13	TRACK PROT 12	38	*2
14	*2	39	*1
15	TRACK PROT 13	40	*2
16	*2	41	DISC SIZE 4
17	TRACK PROT 14	42	*2
18	*2	43	DISC SIZE 5
19	TRACK PROT 15	44	*2
20	*2	45	DISC SIZE 6
21	*1	46	*2
22	*2	47	DISC SIZE 7
23	*1	48	*2
24	*2	49	DISC SIZE 8
25	*1	50	

```
*1 Not used.
*2 =  |     )
     ---    >  (ground symbol)
      V     )
```

Table FIXEDHD-3. Disc Drive Controls and Indicators

NAME	FUNCTION
MOTOR RESET Switch	Depressing this momentary contact restores ac power after interruption by thermal overload has been corrected.
MOTOR POWER ON	Illumination of this green lamp indicates that 115 VAC power is applied to drive motor.
BOTTLE PRESSURE LOW	This amber lamp lights when helium supply bottle pressure is below 200 psi.
PUMP ON	This amber lamp lights when actuation pressure pump is pumping. After discs attain operating speed, this pump is energized for approximately two to four seconds.
SPEED LOW	This amber lamp is lit if disc speed or dc voltage is low while 115 VAC power is applied to system. During the start-up phase, lamp remains lit until motor drives the discs to 95% of synchronous speed (3380 RPM at 60 Hz). When the discs reach that speed the lamp is turns off. If speed drops below 91% of synchronous speed (3280 RPM at 60 Hz) the lamp lights. When a low speed condition is detected data and timing heads are automatically retracted.
TEMP HIGH	This amber lamp lights if the temperature of disc housing rises above 160 degree F or the temperature of motor winding rises above 270 degree F as monitored by thermostats on disc housing and motor. When either temperature limit is exceeded the respective thermostat causes activation of relays that remove ac power from the motor winding, retract read/write heads, light TEMP HIGH lamp, and extinguish MOTOR POWER ON lamp.
Low Pressure Gauge	This 0-5 psi gauge continually shows the difference between controlled environment pressure and ambient pressure. This difference is normally less than 1/2 psi at room temperature but greater than zero. As the memory system operates temperature rise will effect an increase in this pressure but it should not exceed 3 psi.

471004-203



1471004-204

DISC MEM. CONTROLLER PCA JUMPER POSITIONS

DESIGNATION	SIO MUX	SEL CHAN
W1	OUT	IN
W2	IN	OUT
W3	SIO	CH
W4	SIO	CH
W5	SIO	CH
W6	SIO MUX SR NUMBER	CH
W7	INTERRUPT MASK TO ENABLE	

471004-205

FIXED HEAD DISC 2660

DIAGNOSTICS STAND-ALONE

FIXED HEAD DISC S-A (7)
30103A/2660A

1. COLD LOAD DIAG FILE # FROM NON-CPU COLD LOAD TAPE
   D000 FIXED HEAD DISC DIAGNOSTIC (HP32328A.NN.N)
2. P008 ENTER DEVICE NUMBER? XX ((DRT # (DECIMAL)))
3. P009 ENTER FIRST AVAILABLE TRACK? XXXX ((DECIMAL))
4. P010 ENTER LAST AVAILABLE TRACK? XXXX ((DECIMAL))

SWITCH REGISTER OPTIONS:

0 SELECT EXTERNAL REGISTER
1 TIO, CIO, STATUS, TRACKING AND ADDRESSING
2 READ/WRITE WITH CRC DISABLED
3 READ/WRITE WITH CRC ENABLED
4 VERIFIES READ FOLLOWING WRITE
5 SURFACE ANALYSIS AND PROPER HEAD SELECTION
6 RANDOM READ/WRITE
7 POWER-FAIL PROTECTION
8 N-A
9 HALT AT END OF TEST SECTION; PRINT MSG D008
10 SUPPRESS NON-ERROR MSG´S
11 SUPPRESS ERROR MSG´S
12 HALT AFTER COMPLETE DIAG CYCLE
13 LOOP ON LAST STEP
14 HALT ON ERROR
15 HALT AT END OF STEP; PRINT MSG D007

HP 30103A Subsystem
HP 2660 Disc Drive
Stand-Alone SLEUTH Testing

The 3000 Product Support Group of General Systems Division recently completed an investigation of the 30103A Disc subsystem to determine if this subsystem could cause a system crash under MPE.

SLEUTH programs were designed to test the data handling logic of the 30203A controller to determine whether any data could be written or read incorrectly without detection.

Weaknesses in the System I/O logic were discovered during the testing but these were not attributed to the 30203A controller. All data overruns (real and imaginary) were being detected by all 30203A controllers with the Field Change Order 30203-FC004 installed. This FCO will occasionally report false occurrances of data overruns (which accounts for the term imaginary above).

Included below is an example of one SLEUTH test with an explanation of possible errors that may occur.

DATA OVERRUN TEST

```
 10 DEV 0,5,17,999,0         2660 Disc (4 MB)
 10 DEV 1,7,14,999,0         2888 Disc
 10 DEV 2,6,18,99,0          7970B
 10 DB AA,2944,R
 10 DB AB,2944,0
 10 DB BA,1024,R
 10 WD 0,AA                  HEAD 0,ARC 0
 20 PROC D
 30 WD 1,AA                  CYL 0, HEAD 0, SECTOR 0
 40 WD 2,BA
 50 RD 0,AB
 60 WD 0,AB,0,16             HEAD 0, ARC 16
 70 RD 0,AB,0,16
 80 WD 0,AB                  HEAD 0, ARC 0
 90 LOOP 30,999
100 REW 2
110 CB 1,AA,AB,2
120 BUMP P
130 GO 10,0,0
140 END
```

Write Data, Read Data, and Compare Buffer errors will be reported on the console. See EXAMPLES I and II below:

EXAMPLE 1

```
E2 WD FAILED IN STEP 80
STATUS IS  1 000 011 000 010 100
SHOULD BE  1 000 000 000 DDD DDD
TRACK=0,ARC=20

E2 RD FAILED IN STEP 50
STATUS IS  1 000 110 000 010 101
SHOULD BE  1 000 000 000 DDD DDD
TRACK=0,ARC=21

E2 CB FAILED IN STEP 110
DATA WORD 2583 IS X XXX XXX XXX XXX XXX
SHOULD BE         Y YYY YYY YYY YYY YYY
```

In the above example, a data overrun was detected during a write and was detected again during the subsequent read. The compare buffer word (2583) corresponds to ARC address 20 of the write operation. Not all error detected during a write operation cause bad CRC, therefore, the subsequent read and compare buffer operations may or may not fail. This does no harm as the write operation would have been retired under MPE.

EXAMPLE II

```
E2 RD FAILED IN STEP 50
STATUS IS  1 000 110 000 010 011
SHOULD BE  1 000 000 000 DDD DDD
TRACK=0,ARC=19

E2 CB FAILED IN STEP 110
DATA WORD 2367 IS X XXX XXX XXX XXX XXX
SHOULD BE         Y YYY YYY YYY YYY YYY
```

In the above example, a data overrun occurred and was not detected during the write operation but was detected during the read and compare buffer operations. Note the ARC address for the read operations is always one greater than where actual error occurred on the disc.

```
          18
       -------
128 |   2367
       -128
        ----
        1087
       -1024
        ----
          63
```

Counting 0´s this translates to the 63rd word (data word 62) in the 19th ARC (ARC address 18) did not compare.

PAPER TAPE READER/PUNCH

30104A/30105A

DIFFERENCES FROM SERIES II

Must be Date Code 1504 or higher to run on both Series II and Pre-Series II.

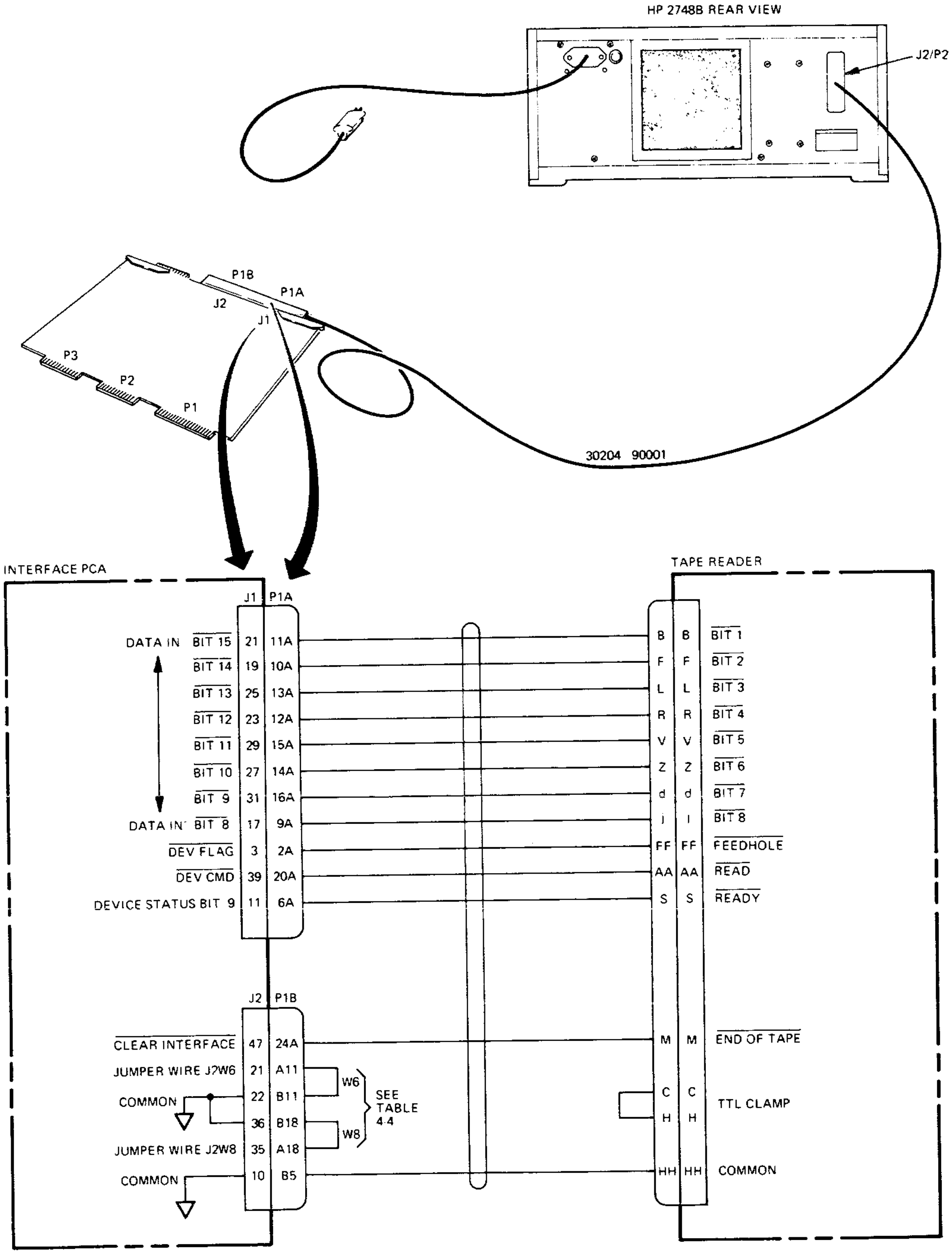
PAPER TAPE PUNCH
30105A

DIFFERENCES FROM SERIES II

Same as 30050A

<< CAUTION >>

The paper tape punch turns on a DC motor cooling fan only while punching tape. Noise from this motor may cause intermittent loss of characters.



1471004-206

SUBSYSTEM INTERCONNECTING CABLE

JUMPER WIRE	JUMPER INSTALLED ?	INTERFACE PCA CONNECTOR J2 PIN NO.	INTERCONNECTING CABLE CONNECTOR P1B PIN NO.	OPERATION OF HP 30104A TAPE READER SUBSYSTEM
J2W1	No	7,8	A4, B4	I/O program continues normally after a control order (does not halt).
J2W2	No	9, 10	A5, B5	Leading edge of Device Flag signal ($\overline{\text{FEEDHOLE}}$) advances sequence counter from count 1 to count 2 and from count 3 to count 0.
J2W3	No	11, 12	A6, B6	Selects response mode; ie, Device Command ($\overline{\text{READ}}$) signal active until Device Flag ($\overline{\text{FEEDHOLE}}$) signal received.
J2W4	No	13, 14	A7, B7	Not functional.
J2W5	No	15, 16	A8, B8	Data input registers enabled by sequence counter counts 1 and 3.
J2W6	Yes	21, 22	A11, B11	Trailing edge of Device Flag advances sequence counter from count 2 to count 3.
J2W7	No	25, 26	A13, B13	Not functional.
J2W8	Yes	35, 36	A18, B18	Leading edge of Device Status Bit 9 ($\overline{\text{READY}}$) causes interrupt.
J2W9	No	37, 38	A19, B19	Not functional.
J2W10	No	39, 40		Device Command ($\overline{\text{READ}}$) signal not inverted.

1471004-207

INTERCONNECTING CABLE JUMPER WIRES

```
*NEW PTR              ((WHATEVER))
PROGRAM FILE?      PD372A.XXXXXX.XXXXXX
DEVICE?    XX    ((DECIMAL # OF DRT #))
SET FLAGS?   X,X,X,X,X       ((WHATEVER))
D2 CONFIGURATION COMPLETED
*SAVE PTR             ((SAVES IT INTO THE PST))
*ON AND RUN OR RUN PTR
```

FLAGS:

1	MISCELLANEOUS TEST
2	INTERRUPT TEST
3	DATA PATTERN TEST
4	START/STOP TEST
5	SCOPE TEST
6	OPERATOR-DESIGNED TEST
10	REPORT ONLY FIRST ERROR PER STEP
12	PRINTS END OF SECTION MSG
13	PAUSE AT THE END OF EACH SECTION

1471004-208

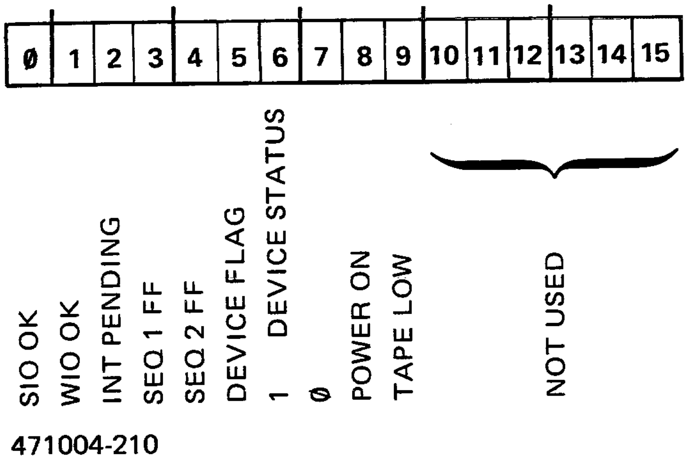
PAPER TAPE READER ON-LINE DIAGNOSTIC 30104A/2748B

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
SIO OK	WIO OK	INT PENDING	SEQ 1 FF	SEQ 2 FF	DEVICE FLAG	0 → INTERRUPT STATUS	0	POWER ON	TAPE LOW	NOT USED	DATA TRANSFER INT	*CLEAR INTERFACE INT	I/O INT	TRANSFER ERROR	TIMER EXPIRED

*1 → Tape problems, binding, slack, or broken.

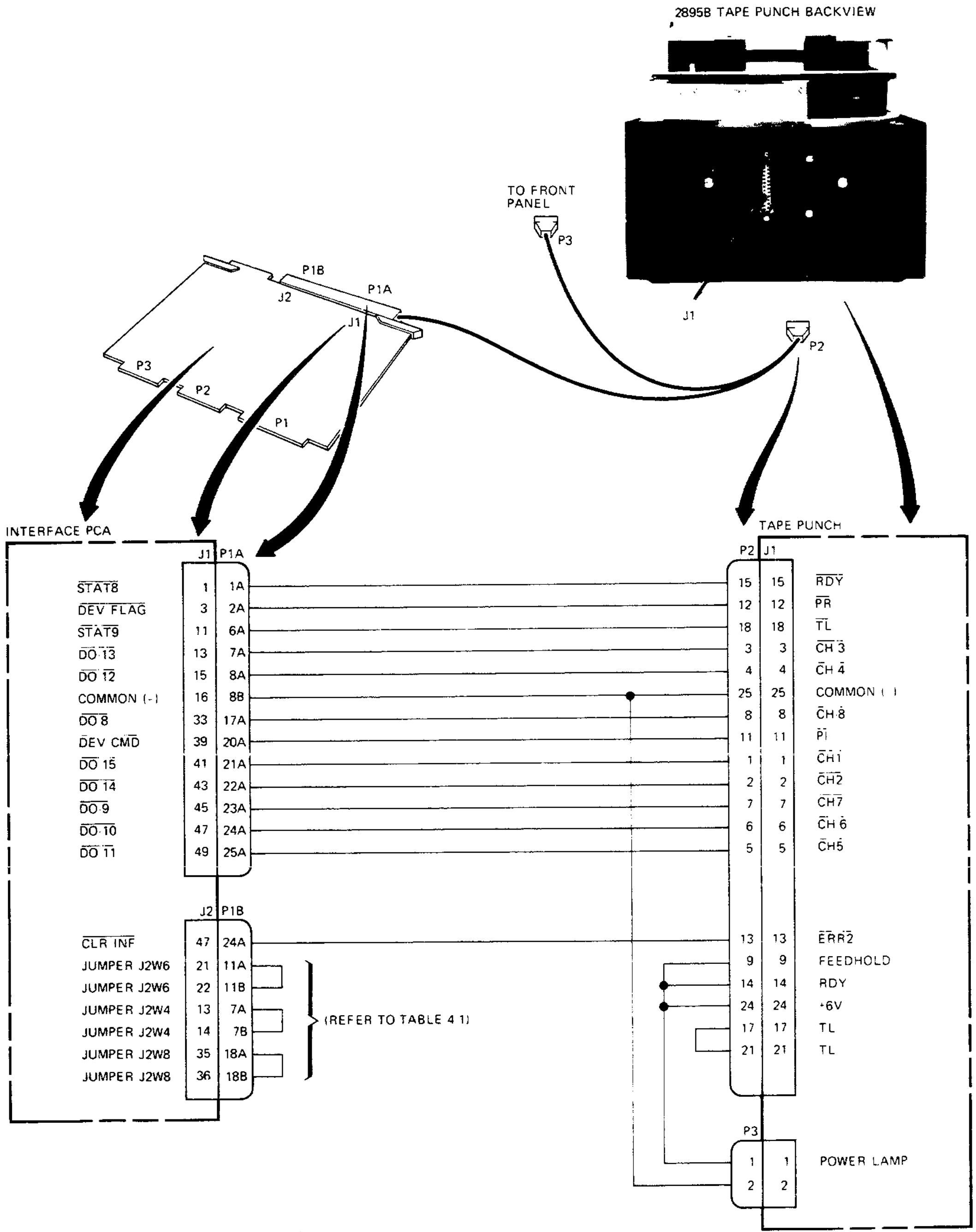
1471004-209

INTERRUPT STATUS



DEVICE STATUS

JUMPER INFORMATION - See Universal Interface



Note. INTERFACE PCA J1 PINS 2, 4, 12, 14, 16, 34, 40, 42, 44, 46, 48 AND 50 ARE TIED TOGETHER TO COMMON(-) ONLY PIN 16 IS SHOWN FOR SIMPLICITY.

1471004-213

SUBSYSTEM INTERCONNECTING CABLE

JUMPER WIRE	JUMPER INSTALLED ON 30105A SUBSYSTEM?	INTERFACE CARD CONNECTOR J2 PIN NO.	INTERCONNECTING CABLE CONNECTOR PIB PIN NO.	OPERATION OF HP 30105A TAPE PUNCH SUBSYSTEM
J2W1	No	7, 8	4A, 4B	I/O program continues normally after a control order (does not halt).
J2W2	No	9, 10	5A, 5B	Negative-going edge of DEVICE FLAG advances sequence counter from state 1 to state 2 and state 3 to state 0.
J2W3	No	11, 12	6A, 6B	Selects response mode (Device Command up until Device Flag occurs).
J2W4	Yes	13, 14	7A, 7B	Leading edge of device status bit 8 causes interrupt.
J2W5	No	15, 16	8A, 8B	Applies to read operation only. Does not effect HP 30105A Tape Punch Subsystem.
J2W6	Yes	21, 22	11A, 11B	Negative-going edge of Device Flag signal advances sequence counter from state 2 to state 3 and produces OP DONE.
J2W7	No	25, 26	13A, 13B	Output data lines static during an input byte transfer.
J2W8	Yes	35, 36	18A, 18B	Leading edge of device status bit 9 causes interrupt.
J2W9	No	37, 38	19A, 19B	Inhibits device status bit 10 from causing an interrupt request.
J2W10	No	39, 40	20A, 20B	Device command not inverted.

1471004-214

INTERCONNECTING CABLE JUMPER WIRES

```
*NEW PTP              ((WHATEVER))
PROGRAM FILE?       PD373A.XXXXXX.XXXXXX
DEVICE?     XX     ((DECIMAL # OF DRT #))
SET FLAGS?     X,X,X,X,X        ((WHATEVER))
D5 END CONFIGURATION
*SAVE PTP             ((SAVES IT INTO THE PST))
*ON AND RUN OR RUN PTP
```

FLAGS:

1	DIO COMMANDS ACCEPTANCE TEST
2	CONTROL WORD FUNCTIONS TEST
3	STATUS WORD TEST
4	PATTERN GENERATION TEST
5	OPERATOR-DESIGNED TEST
6	CREATE SCOPE-TEST TAPE
8	PUNCH 10 INCHES OF LEADER AT START OF FLAG 4
12	PRINTS END OF SECTION MSG
13	PAUSE AT END OF SECTION
14	SUPPRESS P40 MSG

1471004-215

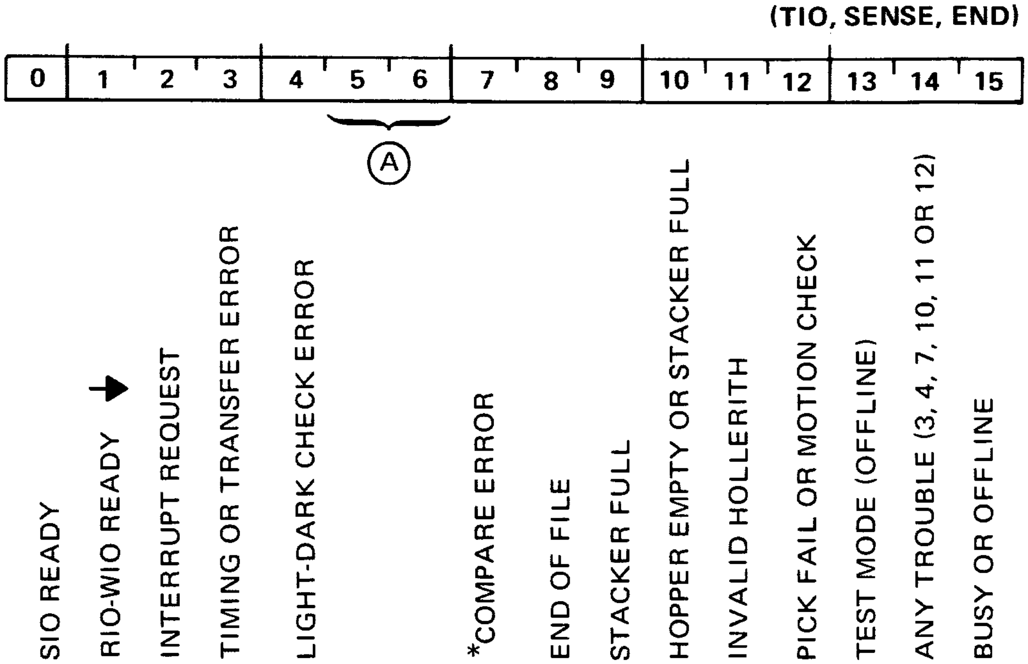
PAPER TAPE PUNCH ONLINE DIAGNOSTIC 30105A/2895B

CARD READER
30106A/2893A/2905A

DIFFERENCES FROM SERIES II

None for 2893A.

2950A not supported on Series II.

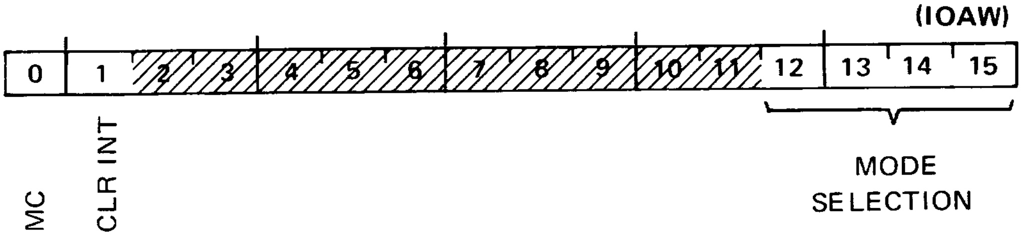


0	0	COLUMN BINARY
0	1	N/A
1	0	PACKED BINARY
1	1	ASCII

*Compare error logic exists on the interface for use by the 2950A reader having a dual read station (option 001).

1471004-216

CARD READER STATUS WORD



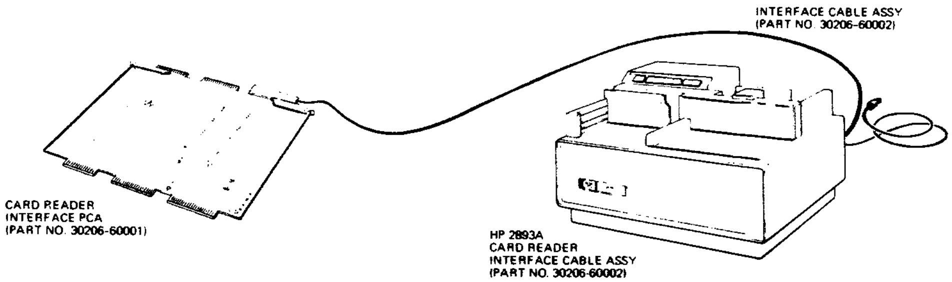
MODE SELECTION

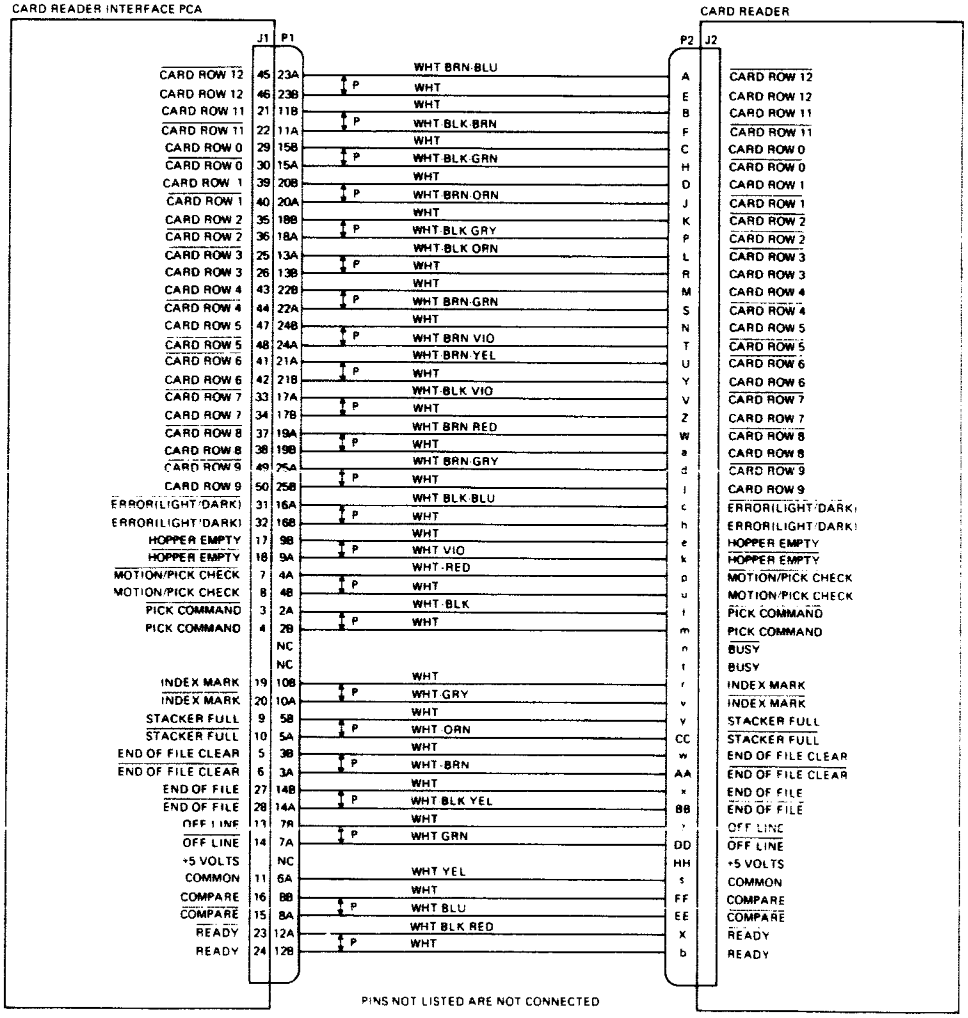
10	11	12	13	14	15		WORD COUNT
		0	1	0	1	COLUMN BINARY	7660 (% 120)
	x	1	0	0	1	PACKED BINARY	7704 (% 74)
	x	1	0	1	0	ASCII CONVERTED HOLLERITH	7730 (% 50)
	x	0	0	0	0	NO MODE CHANGE	
1	x	x	x	x	x	OFFSET CARD	

1471004-217

CARD READER CONTROL WORD

CARD READER





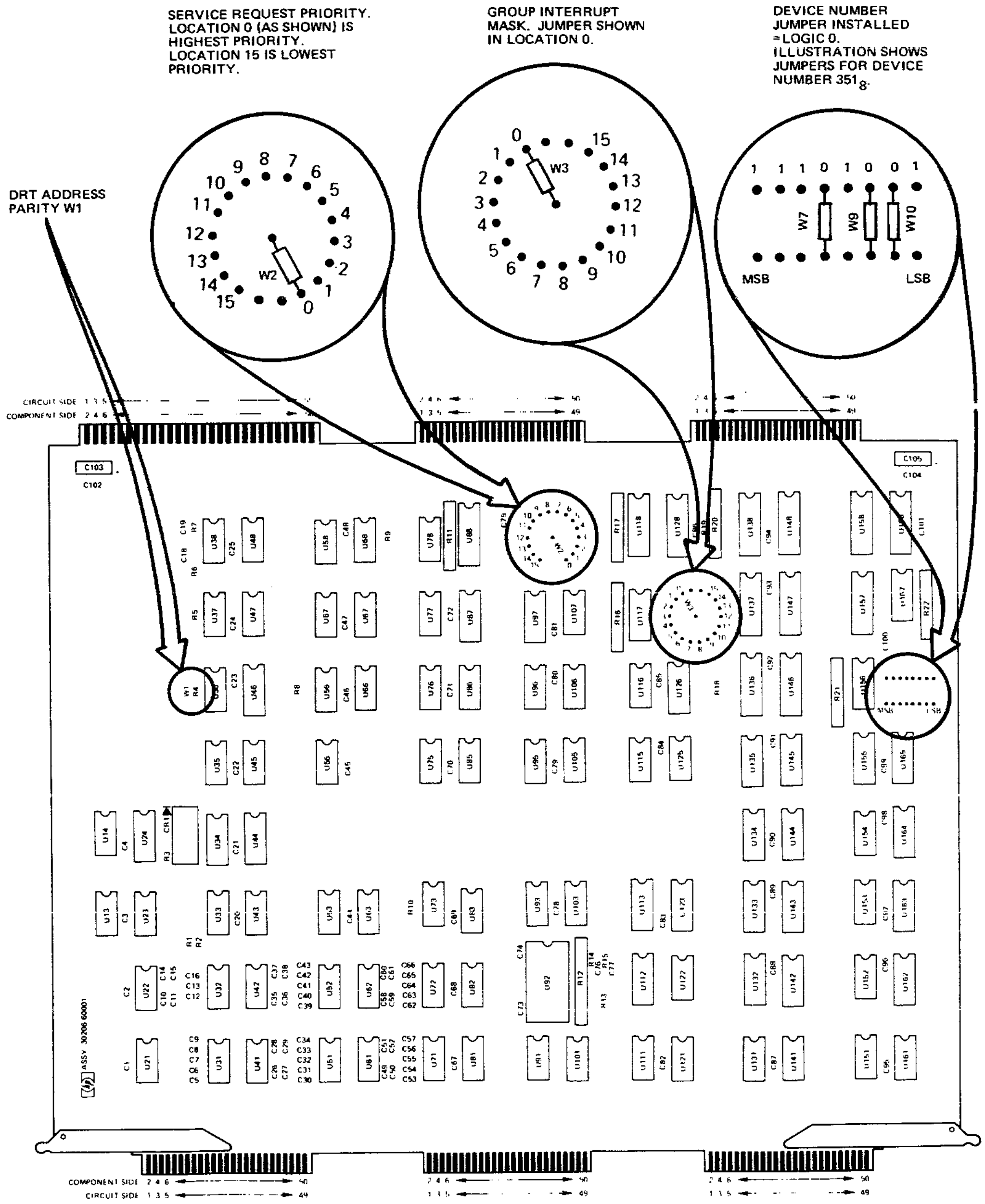
	J1	P1			P2	J2
$\overline{\text{CARD ROW 12}}$	45	23A		WHT BRN-BLU	A	$\overline{\text{CARD ROW 12}}$
CARD ROW 12	46	23B	P	WHT	E	CARD ROW 12
CARD ROW 11	21	11B		WHT	B	CARD ROW 11
$\overline{\text{CARD ROW 11}}$	22	11A	P	WHT-BLK-BRN	F	$\overline{\text{CARD ROW 11}}$
CARD ROW 0	29	15B		WHT	C	CARD ROW 0
$\overline{\text{CARD ROW 0}}$	30	15A	P	WHT-BLK-GRN	H	$\overline{\text{CARD ROW 0}}$
CARD ROW 1	39	20B		WHT	D	CARD ROW 1
$\overline{\text{CARD ROW 1}}$	40	20A	P	WHT-BRN-ORN	J	$\overline{\text{CARD ROW 1}}$
CARD ROW 2	35	18B		WHT	K	CARD ROW 2
$\overline{\text{CARD ROW 2}}$	36	18A	P	WHT-BLK GRY	P	$\overline{\text{CARD ROW 2}}$
$\overline{\text{CARD ROW 3}}$	25	13A		WHT-BLK ORN	L	$\overline{\text{CARD ROW 3}}$
CARD ROW 3	26	13B	P	WHT	R	CARD ROW 3
CARD ROW 4	43	22B		WHT	M	CARD ROW 4
$\overline{\text{CARD ROW 4}}$	44	22A	P	WHT BRN-GRN	S	$\overline{\text{CARD ROW 4}}$
CARD ROW 5	47	24B		WHT	N	CARD ROW 5
$\overline{\text{CARD ROW 5}}$	48	24A	P	WHT BRN VIO	T	$\overline{\text{CARD ROW 5}}$
$\overline{\text{CARD ROW 6}}$	41	21A		WHT-BRN-YEL	U	$\overline{\text{CARD ROW 6}}$
CARD ROW 6	42	21B	P	WHT	Y	CARD ROW 6
$\overline{\text{CARD ROW 7}}$	33	17A		WHT-BLK VIO	V	$\overline{\text{CARD ROW 7}}$
CARD ROW 7	34	17B	P	WHT	Z	CARD ROW 7
$\overline{\text{CARD ROW 8}}$	37	19A		WHT BRN RED	W	$\overline{\text{CARD ROW 8}}$
CARD ROW 8	38	19B	P	WHT	a	CARD ROW 8
$\overline{\text{CARD ROW 9}}$	49	25A		WHT BRN-GRY	d	$\overline{\text{CARD ROW 9}}$
CARD ROW 9	50	25B	P	WHT	j	CARD ROW 9
$\overline{\text{ERROR(LIGHT/DARK)}}$	31	16A		WHT BLK-BLU	c	$\overline{\text{ERROR(LIGHT/DARK)}}$
ERROR(LIGHT/DARK)	32	16B	P	WHT	h	ERROR(LIGHT/DARK)
HOPPER EMPTY	17	9B		WHT	e	HOPPER EMPTY
$\overline{\text{HOPPER EMPTY}}$	18	9A	P	WHT VIO	k	$\overline{\text{HOPPER EMPTY}}$
$\overline{\text{MOTION/PICK CHECK}}$	7	4A		WHT-RED	p	$\overline{\text{MOTION/PICK CHECK}}$
MOTION/PICK CHECK	8	4B	P	WHT	u	MOTION/PICK CHECK
$\overline{\text{PICK COMMAND}}$	3	2A		WHT-BLK	t	$\overline{\text{PICK COMMAND}}$
PICK COMMAND	4	2B	P	WHT	m	PICK COMMAND
		NC			n	$\overline{\text{BUSY}}$
		NC			t	BUSY
INDEX MARK	19	10B		WHT	r	INDEX MARK
$\overline{\text{INDEX MARK}}$	20	10A	P	WHT-GRY	v	$\overline{\text{INDEX MARK}}$
STACKER FULL	9	5B		WHT	y	STACKER FULL
$\overline{\text{STACKER FULL}}$	10	5A	P	WHT ORN	CC	$\overline{\text{STACKER FULL}}$
END OF FILE CLEAR	5	3B		WHT	w	END OF FILE CLEAR
$\overline{\text{END OF FILE CLEAR}}$	6	3A	P	WHT-BRN	AA	$\overline{\text{END OF FILE CLEAR}}$
END OF FILE	27	14B		WHT	x	END OF FILE
$\overline{\text{END OF FILE}}$	28	14A	P	WHT BLK YEL	BB	$\overline{\text{END OF FILE}}$
OFF LINE	13	7B		WHT	z	OFF LINE
$\overline{\text{OFF LINE}}$	14	7A	P	WHT GRN	DD	$\overline{\text{OFF LINE}}$
+5 VOLTS		NC			HH	+5 VOLTS
COMMON	11	6A		WHT YEL	s	COMMON
COMPARE	16	8B		WHT	FF	COMPARE
$\overline{\text{COMPARE}}$	15	8A	P	WHT BLU	EE	$\overline{\text{COMPARE}}$
$\overline{\text{READY}}$	23	12A		WHT BLK RED	X	$\overline{\text{READY}}$
READY	24	12B	P	WHT	b	READY

PINS NOT LISTED ARE NOT CONNECTED

30107A/HP 2950A USES THIS CABLE AND INTERFACE.

1471004-218

INTERFACE CABLE



1471004-219

INTERFACE PCA JUMPER LOCATIONS

30106A/30107A
2893A/2950A

```
*NEW CARD           ((WHATEVER))
PROGRAM FILE?       PD365A.XXXXXX.XXXXXX
DEVICE?    XX    ((DECIMAL # OR DRT #))
SET FLAGS?    X,X,X,X,X        ((WHATEVER))
Q1 IS READER SPEED 1200 CARD/MIN? YES OR NO ((Y = 2950A))
Q1 DUAL READ STATION? YES OR NO  ((2950A))
*SAVE CARD    ((SAVES IT INTO THE PST))
*ON AND RUN OR RUN CARD
```

FLAGS:

1 READY/NOT READY STATUS TEST
2 STATUS INDICATORS TEST
3 WORST CASE DATA TEST
4 DATA PATTERN TEST
5 OPERATOR DESIGNED TEST

1471004-220

CARD READER ONLINE DIAGNOSTIC

LINE PRINTERS (all)

DIFFERENCES FROM SERIES II

Same as 30051A.

IMPORTANT

HP 2613, 2617, and 2618 Line Printer OUT OF PAPER status when TOP OF FORM is sensed on the VFU Tape. When using non-standard forms, the correct VFU tape must also be used. Failure to do this may cause a loss of data.

IOCB0

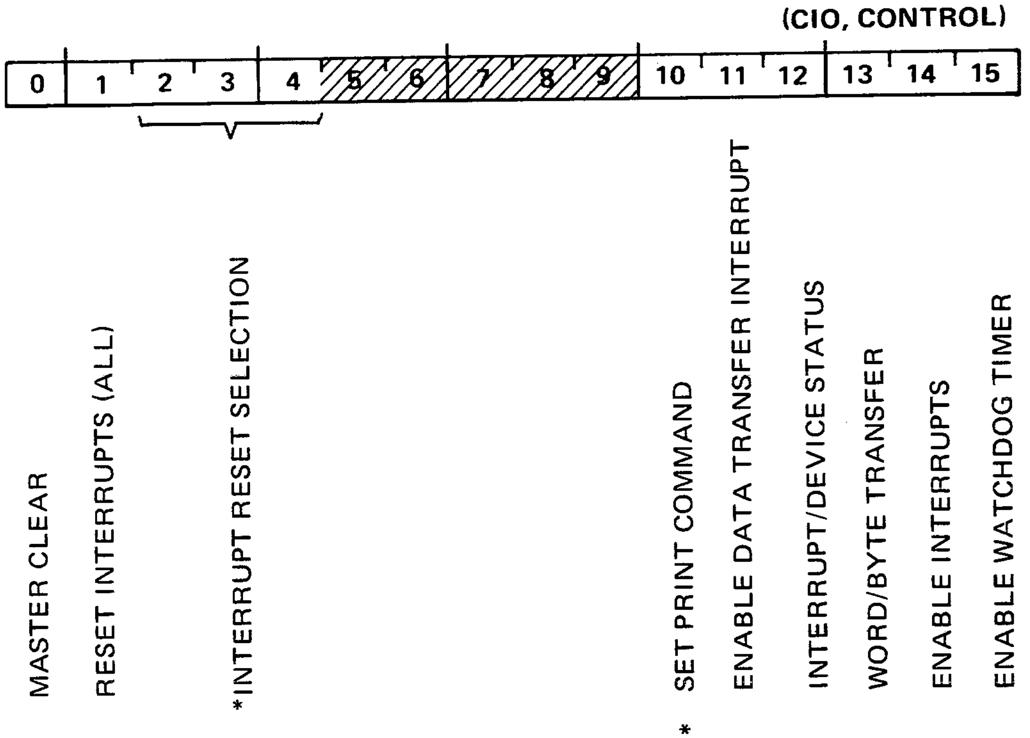
DEV. DEPENDENT (8:5)	GENERAL (13:3)	OVERALL
	0 - PENDING	
3X - WAIT FOR COMPLETION		30
10X - NOT READY WAIT		100
	1 - SUCCESSFUL	1
	3 - UNUSUAL	
0X - INVALID CONTROL REG.		03
3X - REG. ABORTED		33
	5 - IRRECOVERABLE	
0X - INVALID FUNCTION CODE		05
1X - TRANSFER ERROR		15
2X - SID PGM. TIMED OUT		25
4X - SID FAILED		45
5X - CIO-TID FAILED		55

IOCB1

BIT 0 = 0 MEANS WORDS TRANSFERRED
= 1 MEANS BYTES TRANSFERRED

1471004-221

IOLPRT0 RETURN CODES



***Control Word (bit 10) sets Print Command FF.**
The next WIO (format word) initiates a print.

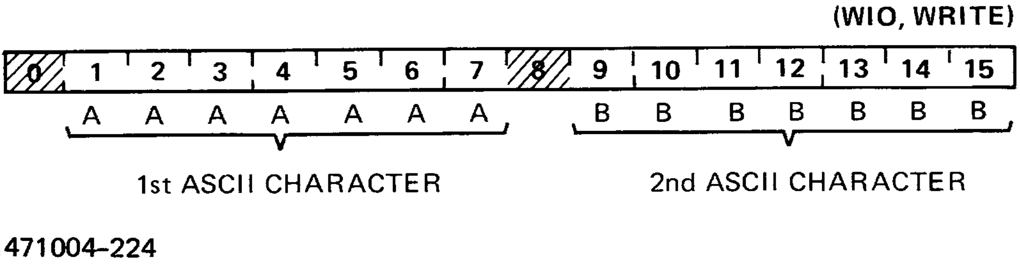
1471004-222

LINE PRINTER CONTROL WORD

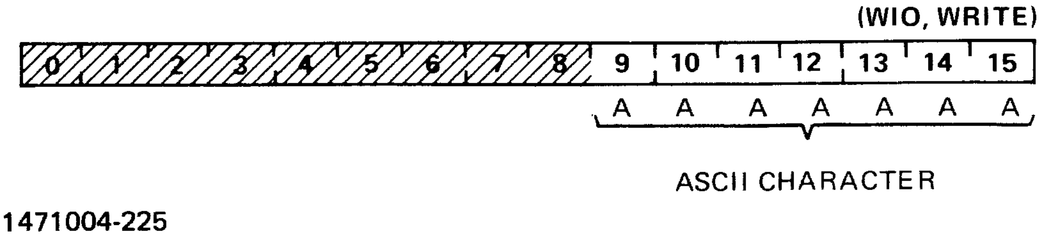
1	2	3	4	
0	0	0	0	NO RESET
0	0	0	1	WATCHDOG TIMER AND TRANSFER ERROR
0	0	1	0	I/O SYSTEM
0	0	1	1	CLEAR INTERFACE
0	1	0	0	DATA TRANSFER COMPLETION
0	1	0	1	LINE READY
0	1	1	0	READY
0	1	1	1	NOT READY

1471004-223

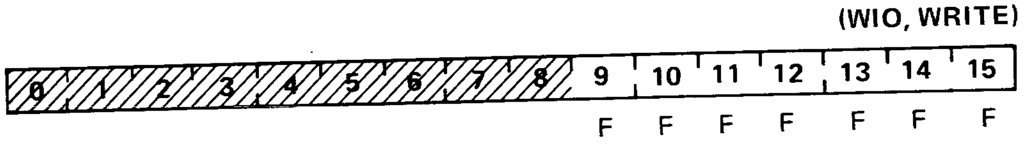
INTERRUPT RESET SELECTION



LINE PRINTER BYTE MODE DATA WORD



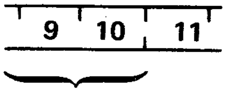
LINE PRINTER WORD MODE DATA WORD



A LINE PRINTER FORMAT WORD FOLLOWS A CONTROL WORD HAVING BIT 10 SET, AND CAUSES THE PRINTER TO PRINT AND FORMS CONTROL.

1471004-226

LINE PRINTER FORMAT WORD

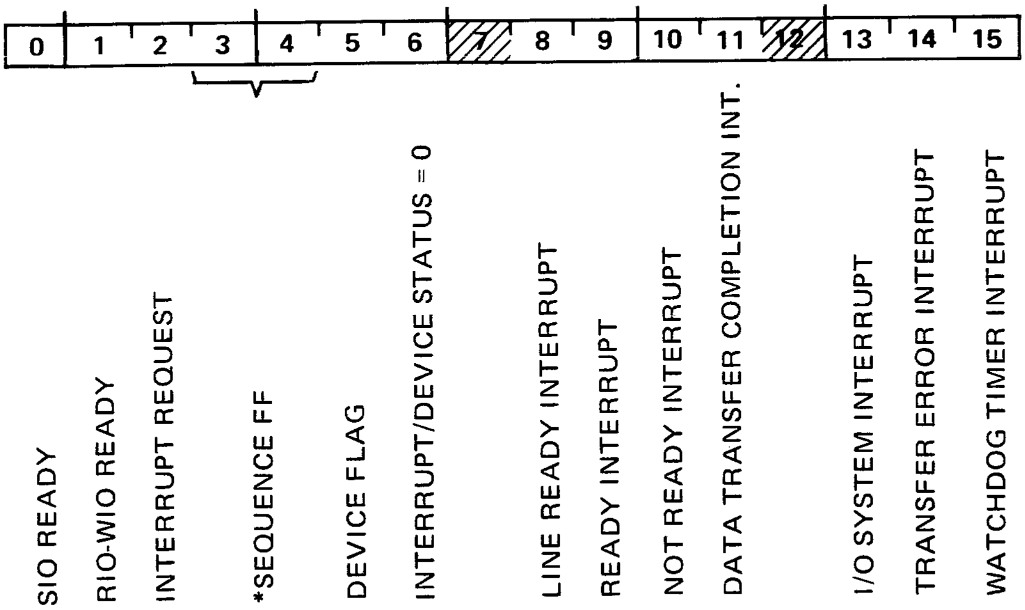


0	0	NOT READY
0	1	PAPER OUT
1	0	READY TO PRINT
1	1	POWER OFF

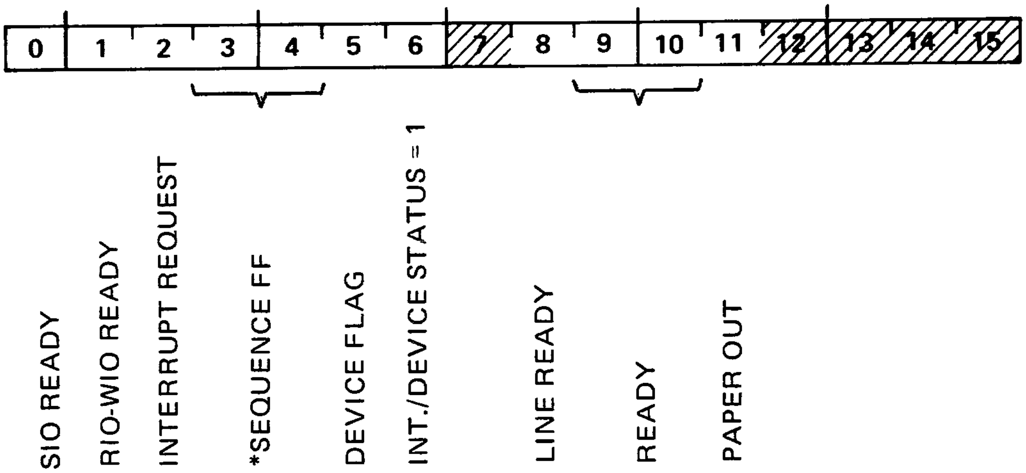
1471004-227

DEV STATUS (ALL)

LINE PRINTER INTERRUPT STATUS WORD **(TIO, SENSE, END)**



LINE PRINTER DEVICE STATUS WORD **(TIO, SENSE, END)**

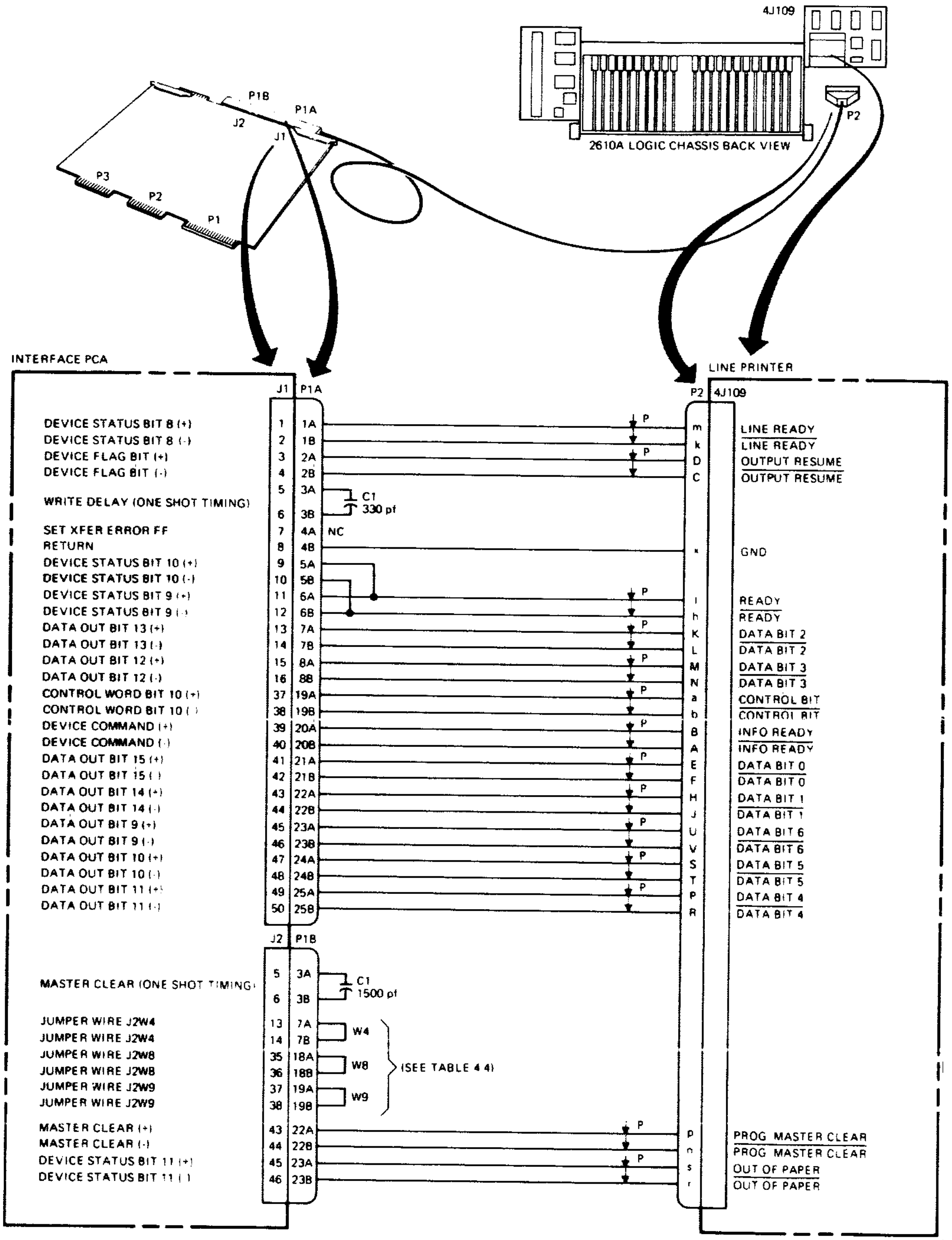


***SEQUENCE FLIP FLOPS**

	3	4	
(CNT = 0)	0	0	NO TRANSFER IN PROGRESS
(CNT = 1)	1	0	DEVICE COMMAND ISSUED (3000 → DEV)
(CNT = 2)	1	1	DEVICE FLAG RECEIVED (DEV → 3000)
(CNT = 3)	0	1	SECOND DEVICE COMMAND ISSUED (BYTE TRANSFER) 3000 → DEV

1471004-228

LINE PRINTER STATUS WORDS



1471004-229

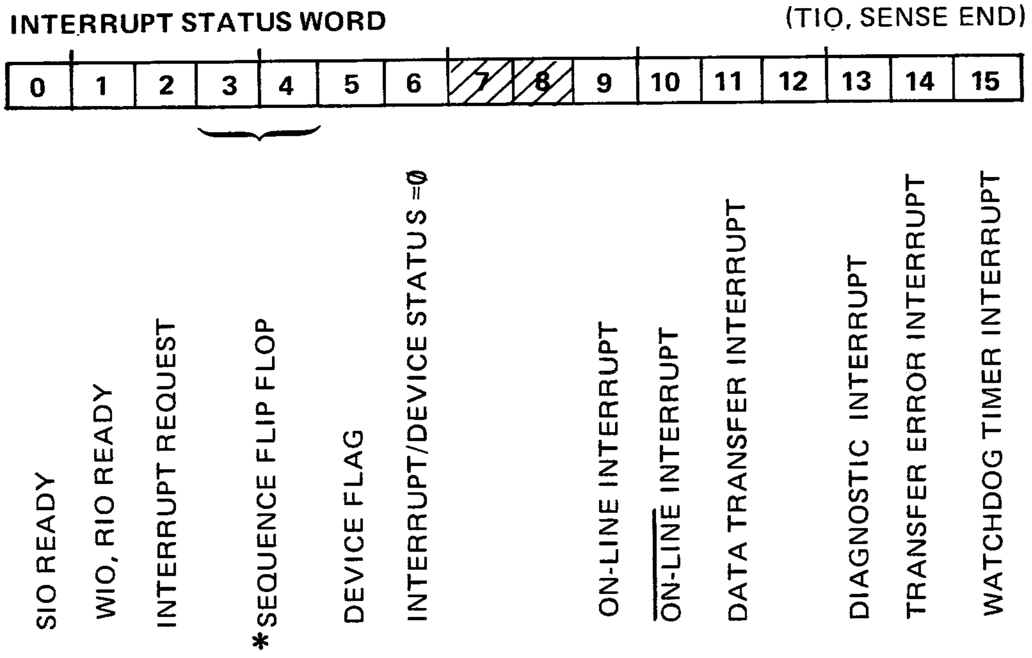
SUBSYSTEM INTERCONNECTING CABLE (2 CONNECTOR)

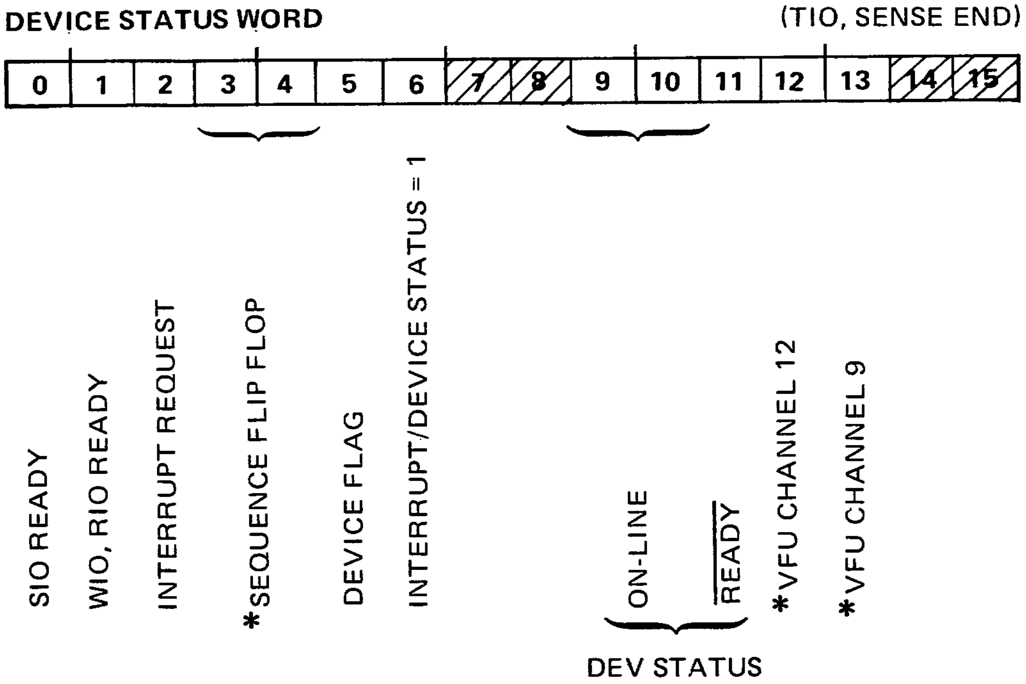
JUMPER WIRE	JUMPER INSTALLED ON 30108A SUBSYSTEM?	INTERFACE CARD CONNECTOR J2 PIN NO.	INTERCONNECTING CABLE CONNECTOR P1B PIN NO.	OPERATION OF HP 30108A LINE PRINTER SUBSYSTEM
J2W1	No	7,8	A4,B4	I/O program continues normally after a control order (does not halt).
J2W2	No	9,10	A5,B5	Leading edge of DEVICE FLAG advances sequence counter from state 1 to state 2 and state 3 to state 0.
J2W3	No	11,12	A6,B6	Selects response mode (Device Command up until Device Flag occurs).
J2W4	Yes	13,14	A7,B7	Leading edge of device status bit 8 causes interrupt.
J2W5	No	15,16	A8,B8	Applies to read operation only. Does not effect HP 30108A Line Printer Subsystem.
J2W6	No	21,22	A11,B11	Trailing edge of Device Flag signal advances sequence counter from state 2 to state 3 and produces OP DONE.
J2W7	No	25,26	A13,B13	Output data lines static during an input byte transfer.
J2W8	Yes	35,36	A18,B18	Leading edge of device status bit 9 causes interrupt.
J2W9	Yes	37,38	A19,B19	Trailing edge of device status bit 10 causes interrupt.
J2W10	No	39,40		Device command not inverted.

1471004-230

INTERCONNECTING CABLE JUMPER WIRES

(JUMPER INFORMATION - See Universal Interface)

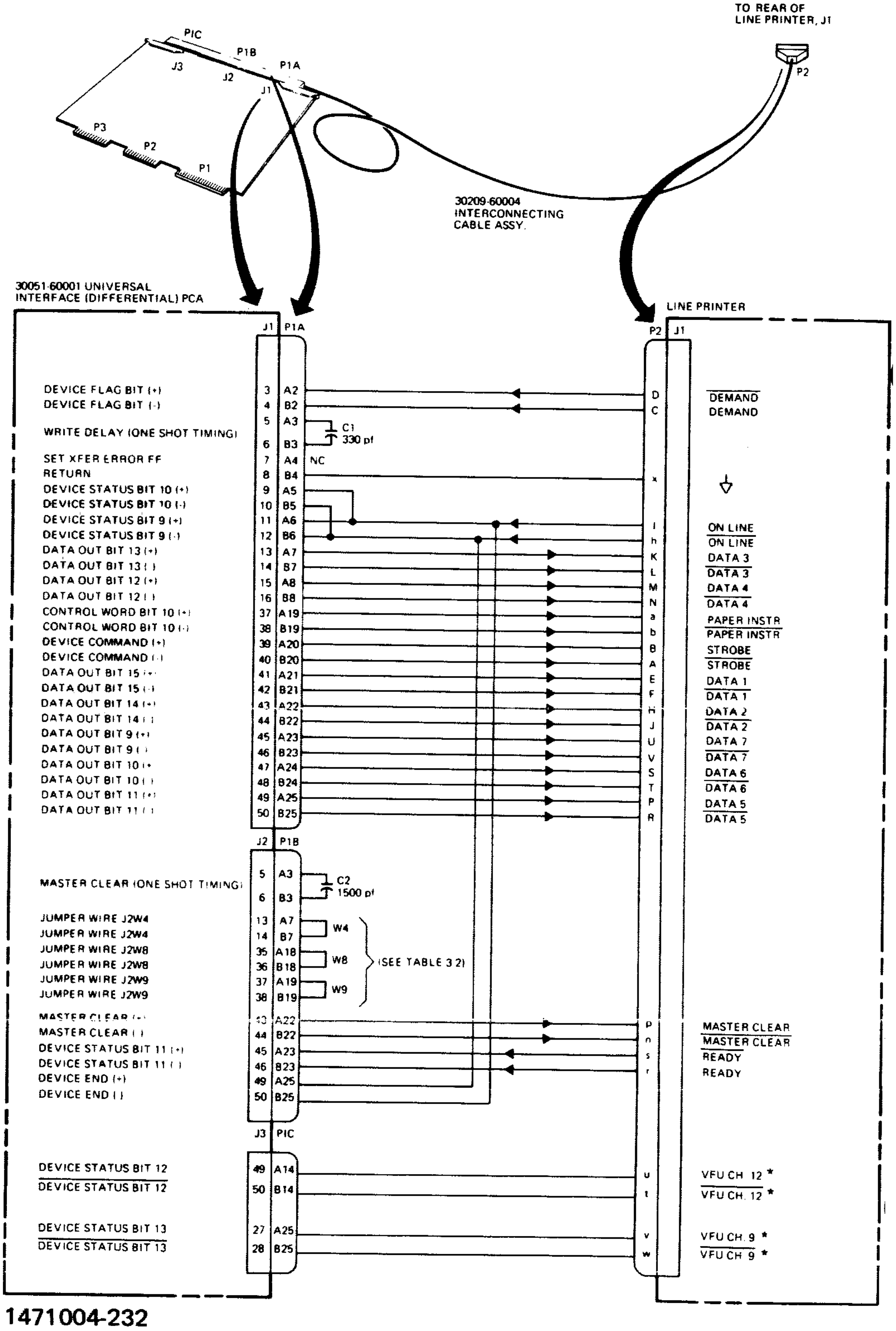




*EXCEPT 2607

1471004-231

STATUS WORDS



INTERCONNECTING CABLE (3 CONNECTOR)

JUMPER	INSTALLED ON SUBSYSTEM	PIN NO.		EFFECT ON SYSTEM
		INTERFACE PCA, J2	CABLE, P1B	
J2W1	No	7,8	A4, B4	I/O program does not halt after a CONTROL order is executed.
J2W2	No	9, 10	A5, B5	Leading edge of DEV FLAG signal (DEMAND signal in printer) advances sequence counter on PCA from state 1 to state 2, or from state 3 to state 0 if second byte.
J2W3	No	11, 12	A6, B6	Printer is in response mode (interlocked in handshake). Specifically, the DEV FLAG signal (DEMAND signal in printer) is high during the DEV COMD (STROBE) signal.
J2W4	Yes	13, 14	A7, B7	**Leading edge of device status bit 8 causes interrupt request.**
J2W5	No	15, 16	A8, B8	No effect on 30118A subsystem. (Applies to read operation only.)
J2W6	No	21, 22	A11, B11	**Leading edge of DEV Flag signal advances sequence counter from state 2 to state 3.**
J2W7	No	25, 26	A13, B13	DATA (1:7) bits (interface PCA to printer) do not change until the interface PCA receives a new 16-bit data word from the CPU.
J2W8	Yes	35, 36	A18, B18	An on-line transition of the printer sets bit 9 of the interrupt-status word. An on-line transition occurs when the last of the following takes place: a. Printer PRINT switch is on (lighted). b. Paper is installed in the printer. c. The printer platen is closed.
J2W9	Yes	37, 38	A19, B19	An off-line transition of the printer sets bit 10 of the interrupt-status word. An off-line transition occurs when one of the following takes place: a. Printer PRINT switch is released. b. Paper movement to top-of-form has been initiated by programming, but there is no paper. c. The printer platen is opened. d. An electronic fault is detected in the printer.
J2W10	No	39, 40	A20, B20	The DEV CMD signal sent to the printer by the interface PCA is not in inverted form.

1471004-233

CONTROL JUMPERS

```
*NEW LPTEST          ((WHATEVER))
PROGRAM FILE?        PD366A.XXXXXX.XXXXXX
DEVICE?    XX    ((DECIMAL # OF DRT #))
SET FLAGS?    X,X,X,X,X        ((WHATEVER))
Q1 64/96/128 CHARACTER?    XXX       ((WHATEVER))
Q2 2607/2610/2614?  XXXX     ((WHATEVER))
D2 LINE PRINTER TEST CONFIGURED
*SAVE LPTEST     ((SAVES IT INTO PST))
*ON AND RUN OR RUN LPTEST
```

FLAGS:

1	STATUS TEST
2	MASTER CLEAR AND VERTICAL FORMAT CNTRL TST
3	CHARACTER TEST
4	RIPPLE TEST
5	TRIANGLE PATTERN TEST
6	HORIZONTAL, VERTICAL TEST (2607)
7	NON-PRINTING CHARACTER CODES (2610/2614 ONLY))
8	DIRECT I/O TEST
9	OPERATOR DESIGN TEST
10	PRINTS END OF SECTION MSG (0-9)
11	PAUSE AFTER COMPLETION OF SECTION (0-9)

1471004-234

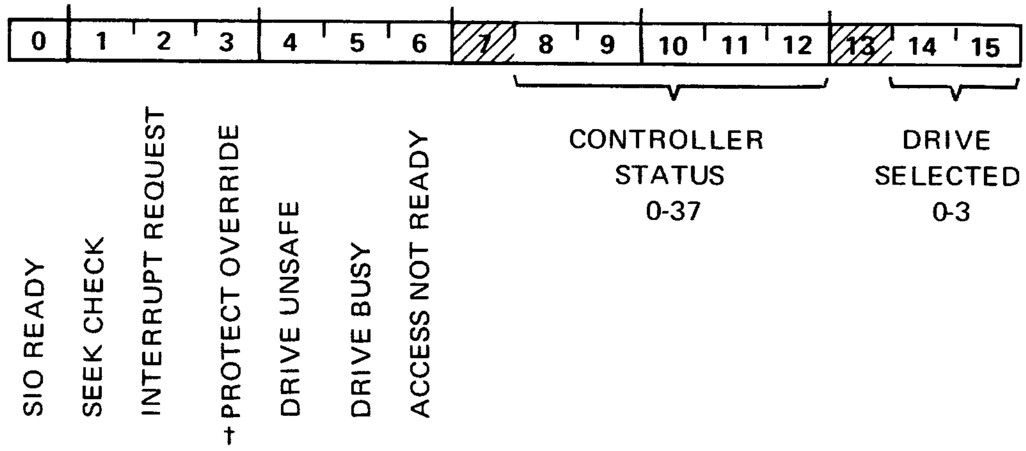
ON LINE DIAGNOSTIC

CARTRIDGE DISC
30110A/30210A/7900A

DIFFERENCES FROM SERIES II

DEVNO must be 5 if configured as System Disc.

CARTRIDGE DISC STATUS WORD **(*TIO, SENSE, END)**



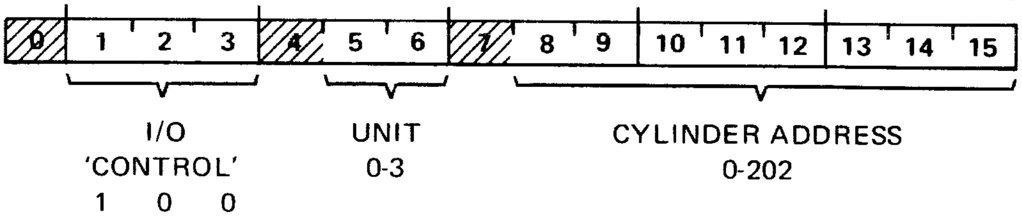
*During data transfer only status bits 0, 2, 14 and 15 are valid using a 'TIO' instruction.

†7900 PROTECT must be in OVERRIDE.

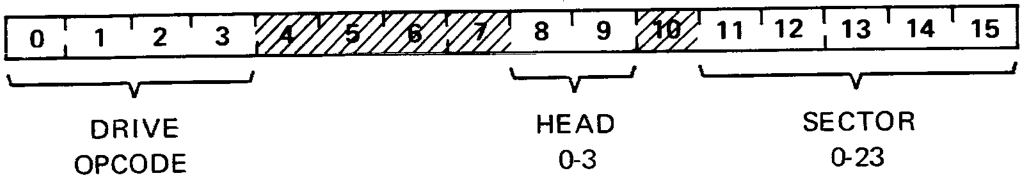
CONTROLLER STATUS

8	9	10	11	12	
0	0	0	0	0	ERROR FREE
0	0	0	0	1	ILLEGAL OPCODE
0	0	1	0	0	SECTOR TOO LARGE
0	0	1	1	0	OP ATTEMPTED ON DEFECTIVE TRACK
0	0	1	1	1	HEADS MISPOSITIONED
0	1	0	0	1	CYCLIC ERROR
0	1	0	1	0	I/O PROGRAM ERROR
0	1	1	0	0	CYLINDER OVERRUN
0	1	1	0	1	ZERO SECTOR COUNT IN CYCLIC CHECK OPCODE
0	1	1	1	0	DATA OVERRUN
1	0	0	1	0	HEAD-SECTOR COMPARE ERROR
1	0	0	1	1	ACCESS NOT READY
1	0	1	0	0	TRANSFER ERROR
1	0	1	1	0	PROTECT NOT OVERRIDEN
1	1	1	1	1	DRIVE ATTENTION

CARTRIDGE DISC CONTROL WORD (P CMD1) **(IOCW)**

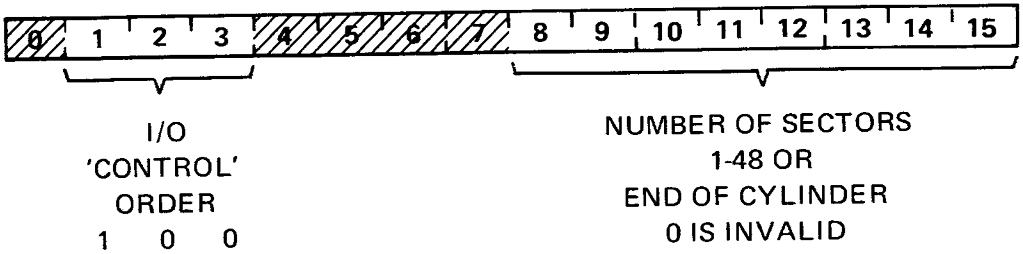


CARTRIDGE DISC CONTROL WORD (P CONT STB) (IOAW)



When the drive opcode is a 'Cyclic Check,' a second IOCW is required containing the number of sectors to be checked. The second IOAW in this case is ignored. Jump condition always false.

CARTRIDGE DISC CONTROL WORD (P CMD 1) (IOCW)*



*As a result of a cyclic check opcode.

DRIVE OPCODE

	0	1	2	3	
RD	0	0	0	0	READ DATA (COLD LOAD)
RC	0	0	0	1	RECALIBRATE (RESET SEEK CHECK ERROR)
SEEK	0	0	1	0	SEEK
SC	0	0	1	1	STATUS CHECK
FTD	0	1	0	0	FLAG TRACK DEFECTIVE
RD	0	1	0	1	READ DATA (PROGRAMMATIC)
*RFS	0	1	1	0	READ FULL SECTOR
CC	0	1	1	1	CYCLIC CHECK
WD	1	0	0	0	WRITE DATA
*WFS	1	0	0	1	WRITE FULL SECTOR
RNFS	1	0	1	0	READ NEXT FULL SECTOR (I/O SCHEDULING)
ID	1	0	1	1	INITIALIZE DATA

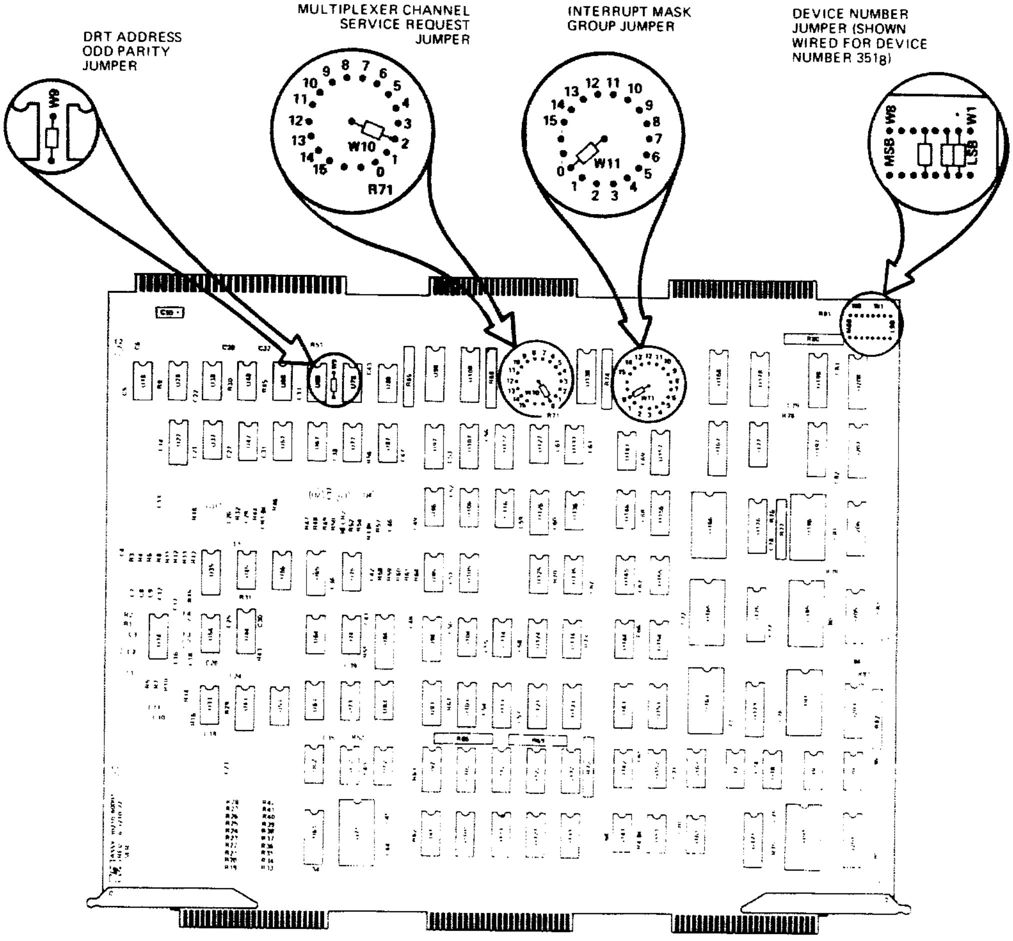
*For diagnosing purposes.

Stand-alone HP 30110A Cartridge Disc Diagnostic - Appendix B

OCTAL CODE (Bits 8, 9, 10, 11 and 12)

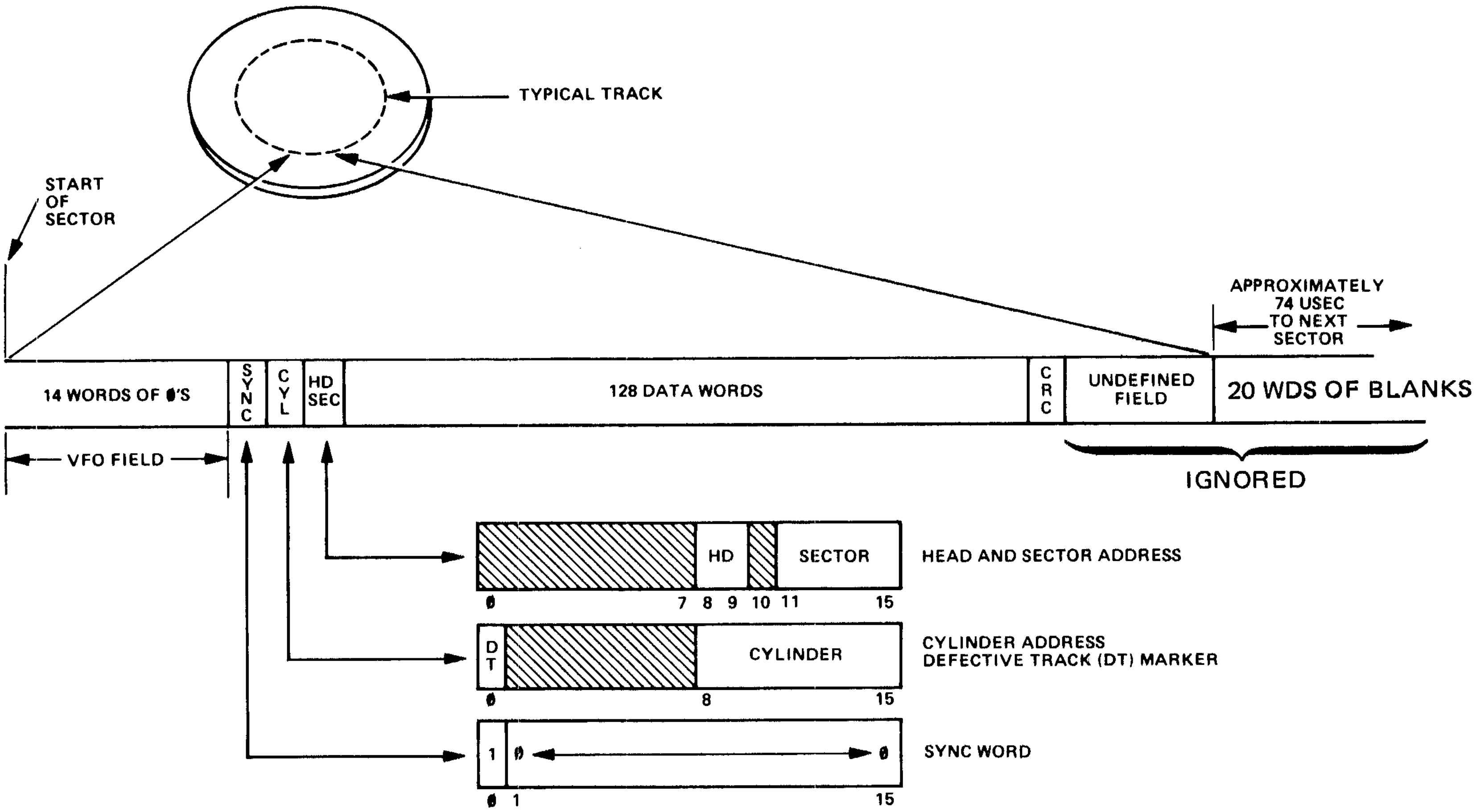
00	No Error.
01	Illegal opcode-The Opcode in bits 0-3 of the I/O address word are illegal.
04	Sector number too big-The sector address received from the CPU is too large (asserted for all commands).
06	Defective track-An operation has been attempted on a track which is flagged defective (RD, WD, WF, CD).
07	Heads mis-positioned. The cylinder address read from the track does not compare with the address received from the current command. This could mean that either 1) The heads are truly positioned at the wrong track or, 2) The cylinder address of the current command does not match the cylinder address of the most recent SK command (RD, WD, WF, CD).
11	Cyclic error-A cyclic error has been detected in the sector immediately preceding the sector to be written. No writing takes place (WD, WF) or cyclic error has been detected in data field (RD, CD).
12	I/O program error-There is a discrepancy between the command sent to the controller and the current order from the I/O program. That is, the program is executing an order for a data transfer in one direction and the controller is expecting data transfer in the other direction. In the case where a control order is expected to follow another control order, some other error condition may be indicated, such as data overrun (RD, RF, RN, WD, WF, ID).
14	Cylinder overrun-A read or write operation has been attempted beyond the last sector in a cylinder on the disc selected. A read or write operation may be continued from head 00 to 01 or from 10 to 11 but NOT from head 01 to 10. That is, a data transfer operation may not cross the boundary from one disc to another, but rather only from the top surface to the bottom surface of the same physical disc. (RD, RF, RN, WD, WF, ID, CD. In the case of the CD command, the sector count is checked only for zero. If the sector count is too large, it will be detected as a cylinder overrun.)
15	Zero sector count-The sector count accompanying a CD command is zero. Also, see 14 above (cylinder overrun). (CD only).

22	Erroneous head/sector compare-The head address and/or the sector address read from the disc does not compare with the head/sector field of the current command (RD, WD, WF).
23	Access not ready-The drive´s access not ready status bit was asserted during some controller operation.
24	Transfer error-There has been a system I/O or memory parity error or an address was out of bounds.
26	Data protected-The data protect switch for the disc being accessed is in the "protect" position.
37	Drive attention-The drive has been placed on or off line or has completed a seek.



1471004-237

DISC CONTROLLER PCA JUMPER LOCATIONS



1471004-238

SECTOR FORMAT

1. COLD LOAD DIAG FILE # FROM NON-CPU COLD LOAD TAPE
2. D99 01 CARTRIDGE DISC (30110A) DIAG CONFG (HP32324A.N)
   Q99 02 WHAT IS DEVICE NUMBER? XX ((DRT # (DECIMAL)))
3. Q99 03 INTERRUPTS ON OR OFF? ON OR OFF
4. P99 61 PAUSE AFTER CONFIGURATION
   *SET SWITCH OPTIONS FOLLOWED BY CR TO START DIAG

SWITCH REGISTER OPTIONS:

0 SELECT EXTERNAL REGISTER
1 N-A
2 SHORTEN TEST BY 40%

FORMAT INSTRUCTIONS

```
SD << UNIT NO. >>
LB NN
IS << IS, 2 FORMATS FIXED PLATTER >>
IDI
RT NN, 202
EN
```

3 OPERATOR DESIGN
4 SHORTEN TEST SEVERELY
5 RESTRICT CYLINDERS
6 CHANGE UNIT #, CYLINDER, PATTERN AND/OR HEAD TABLES
7 REPEAT CURRENT SECTION
8 SHORT PRINT
9 PAUSE AFTER CURRENT SECTION
10 SUPPRESS D-CLASS MSG'S
11 SUPPRESS ALL MSG'S, HALT ON P-CLASS MSG'S
12 PAUSE AFTER COMPLETED DIAG CYCLE
13 LOOP ON CURRENT STEP
14 PAUSE ON ERROR
15 PAUSE ON END OF CURRENT STEP

1471004-239

STAND ALONE DIAGNOSTIC

```
*NEW CDISC            ((WHATEVER))
PROGRAM FILE?      PD361A.XX.X
DEVICE?    XX     ((DECIMAL # OF DRT))
SET FLAGS?    X,X,X,X,X        ((WHATEVER))
D99 1 CARTRIDGE DISC (30110A) DIAGNOSTIC CONFIGURATION
   (HP32361A.X.X)
*SAVE CDISC           ((SAVES IT INTO PST))
*ON AND RUN OR RUN CDISC
D99 1 CARTRIDGE DISC (30110A) DIAGNOSTIC ON-LINE (HP32361A.X.X)
Q99 2 WHAT IS MODE (A = CONTROLLER, B = FILE SYSTEM)?
```

FLAG	FUNCTION IF SET
1	SECTION 1 CONTROLLER FUNCTIONS
2	SECTION 2 DATA PATTERN READ/WRITE
3	SECTION 3 SEEK AND DATA TRANSFER TEST
4	SECTION 4 CHECKSUM, CYLINDER, HEAD, SECTOR SELECT
5	SECTION 5 MULTI UNIT TEST
6-11	NOT USED
12	SHORT TEST (60% AS LONG)
13	SECTION 6 OP DESIGN
14	SEVERELY SHORTENED TEST (10% AS LONG)
15	RESTRICT CYLINDERS
16	CHANGE UNIT NUMBER TABLE
17	PAUSE AFTER PASS
18	PAUSE AFTER CURRENT SECTION
19	PAUSE AT END OF ERROR REPORT
20	DUMP STATUS OBTAINED FROM ERROR
21	DUMP CURRENT SIO PROGRAM
CS	REPEAT CURRECT SECTION
SP	SHORT PRINT
EP	SUPPRESS D-CLASS MESSAGES
NP	SUPPRESS ALL MESSAGES
LP	LOOP ON CURRENT STEP
PE	PAUSE ON ERROR
PA	PAUSE AT END OF CURRENT STEP

1471004-240

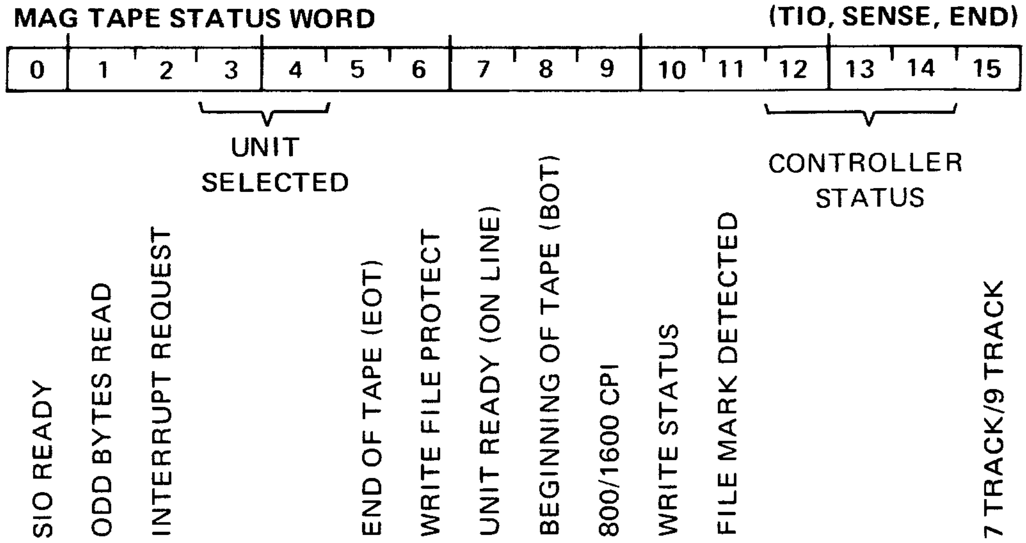
ONLINE DIAGNOSTIC

MAGNETIC TAPE UNITS

MAGNETIC TAPE
30115A/30215A/7970B/E

DIFFERENCES FROM SERIES II

MPE-C must only be cold loaded from DEVNO 6 unit 0.

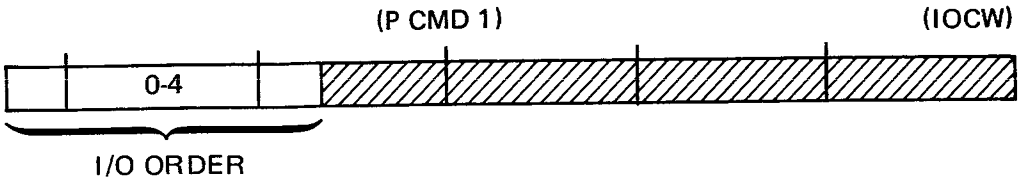


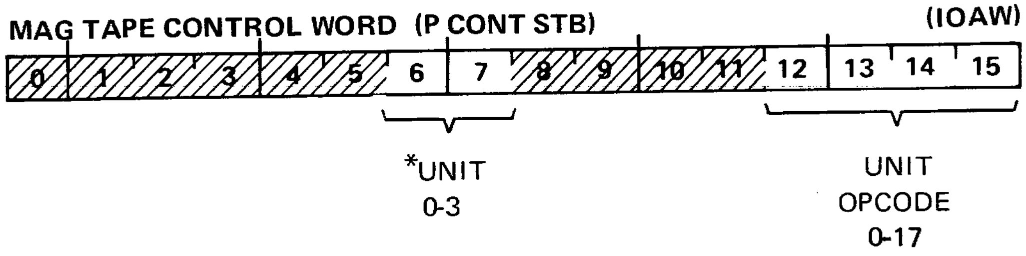
CONTROLLER STATUS

12	13	14	
0	0	0	UNIT READY TO READY INTERRUPT
0	0	1	TRANSFER ERROR
0	1	0	COMMAND REJECTED
0	1	1	TAPE RUNAWAY (25 FEET)
1	0	0	TIMING ERROR
1	0	1	TAPE ERROR (PARITY, CRC, etc.)
1	1	1	ERROR FREE

471004-241

STATUS WORDS





*Used for a 'Unit Select' opcode only

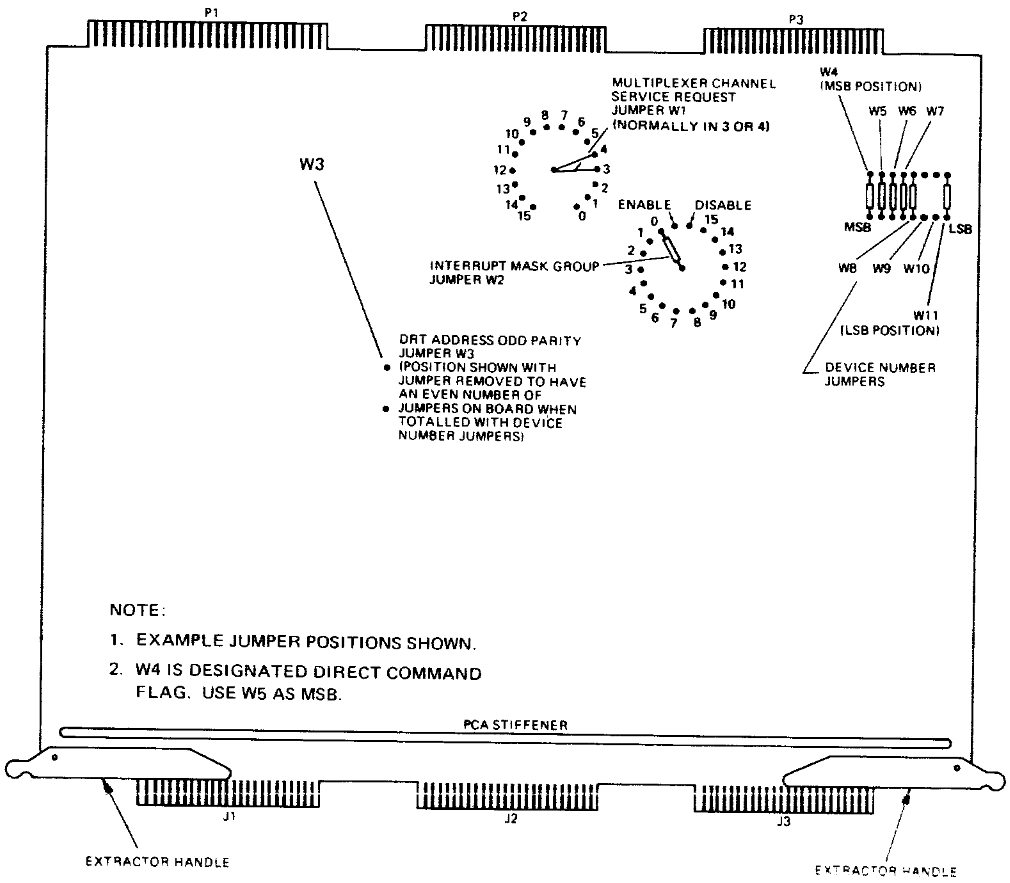
UNIT OPCODE

	12	13	14	15	
SEL	0	0	0	0	UNIT SELECT
WRR	0	1	0	0	WRITE RECORD
GAP	0	1	0	1	WRITE GAP
RDR	0	1	1	0	READ RECORD
FSR	0	1	1	1	FORWARD SPACE RECORD
REW	1	0	0	0	REWIND
RST	1	0	0	1	REWIND AND RESET (OFF LINE)
BSR	1	0	1	0	BACKSPACE RECORD
BSF	1	0	1	1	BACKSPACE FILE
ΔWRZ	1	1	0	0	WRITE RECORD WITH ZERO PARITY
WFM	1	1	0	1	WRITE FILE MARK
ΔRDC	1	1	1	0	READ RECORD WITH CRCC
FSF	1	1	1	1	FORWARD SPACE FILE

ΔUsed for diagnosing purposes.

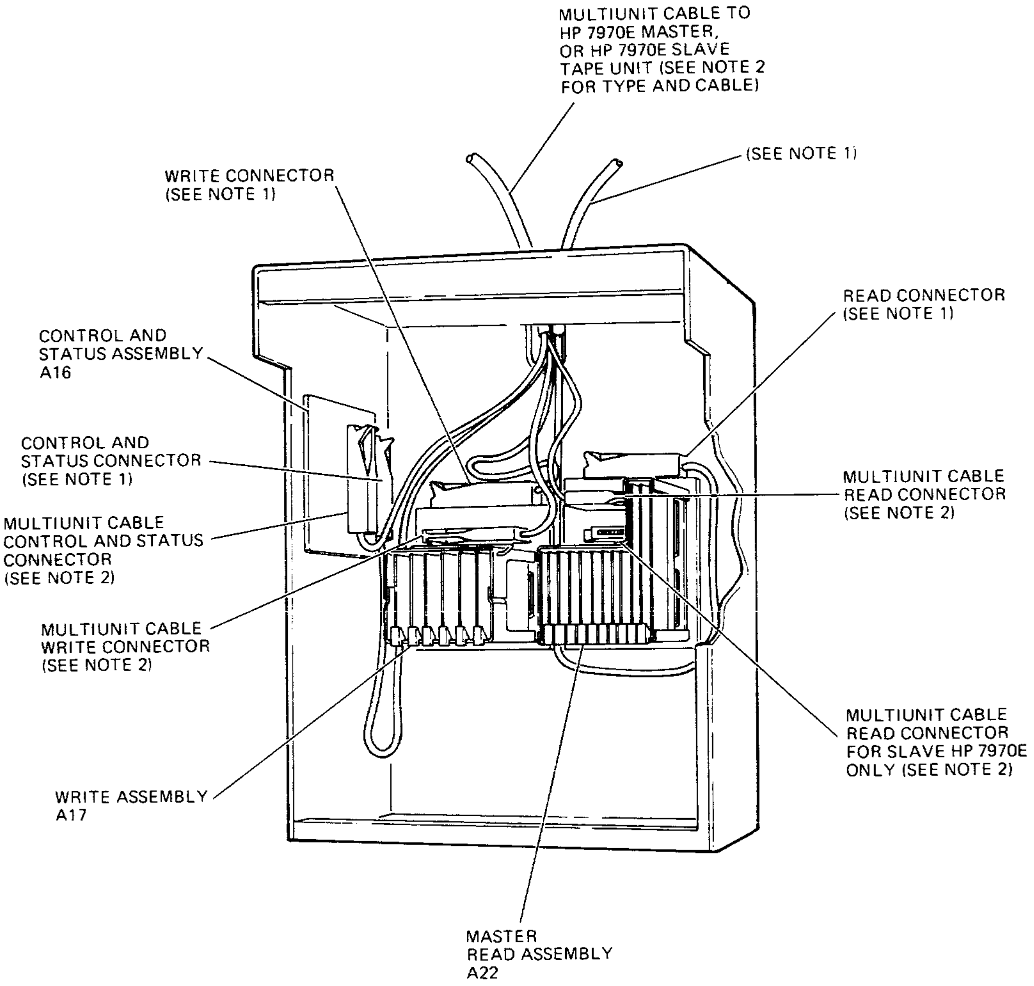
1471004-242

IOCW, IOAW



1471004-243

TAPE CONTROLLER PCA, JUMPER LOCATIONS

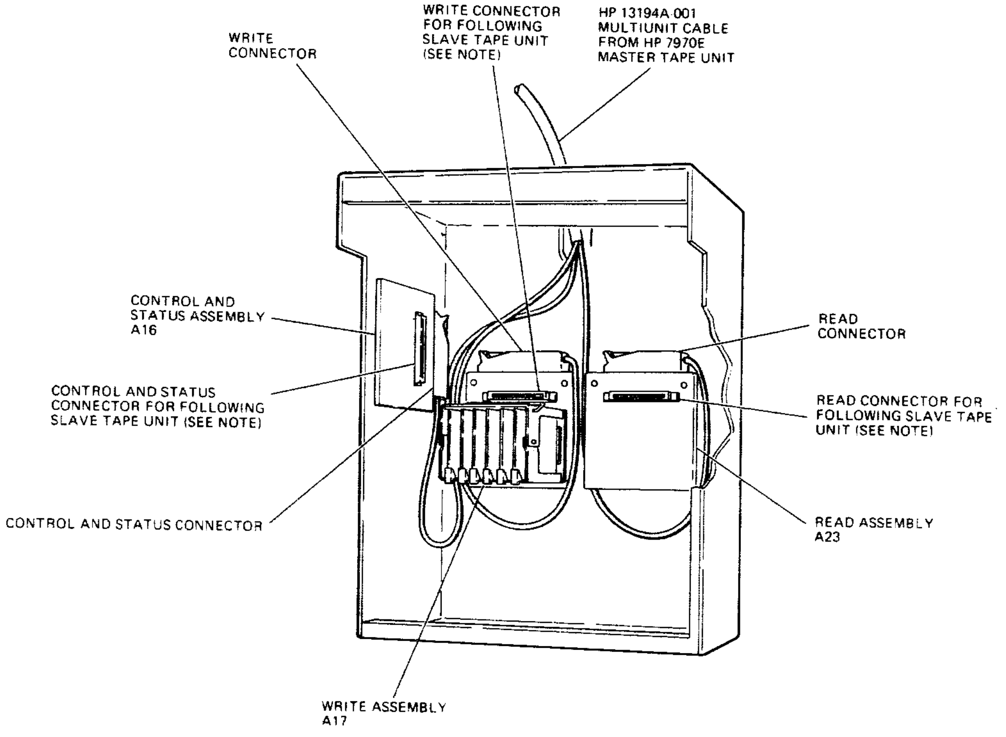


NOTES:

1. IF THE HP 7970E MASTER TAPE UNIT SHOWN IS UNIT 0, THIS WILL BE INTERFACE CABLE PART NO. 30215-60003. OTHERWISE IT WILL BE AN HP 13194A MULTIUNIT CABLE COMING FROM HP 7970B OR ANOTHER HP 7970E MASTER TAPE UNIT.
2. IF THE FOLLOWING UNIT IS ANOTHER HP 7970E MASTER TAPE UNIT, THIS CABLE WILL BE AN HP 13194A MULTIUNIT CABLE WITH READ CONNECTOR INSTALLED AS SHOWN. IF FOLLOWING UNIT IS AN HP 7970E SLAVE TAPE UNIT, THIS MUST BE AN HP 13194A-001 MULTIUNIT CABLE WITH READ CONNECTOR INSTALLED IN SLAVE READ POSITION AS DESIGNATED IN DRAWING.

1471004-244

MASTER HP 7970E MAG TAPE (PE) CABLE CONNECTIONS



NOTE. IF ADDITIONAL HP 7970E SLAVE TAPE UNIT IS USED, HP 13194A-001 MULTIUNIT CABLE MUST BE USED TO CONNECT TO THE FOLLOWING UNIT

1471004-245

SLAVE HP 7970E TAPE UNIT (PE) CABLE CONNECTIONS

9-TRACK MAG TAPE S-A
30115A/7970B/E

1.
```
COLD LOAD DIAG FILE # FROM NON-CPU COLD LOAD TAPE
30115A 9-TRACK MAGNETIC TAPE (HP32333.00.0)
PD333B (STAND-ALONE DIAGNOSTIC PROGRAM)
D023 CONFIGURATION SEC. STARTED
Q010 TAPE DEVICE NUMBER?  XX  ((DECIMAL # OF DRT))
D024 CONTROL SECTION STARTED
P005 ENTER ONE OF THE FOLLOWING CONTROL CODES:
   AUTO        ((RUN AUTO PROCESS))
   MANU        ((RUN MANUAL PROCESS))
   RESTART     ((JUMP TO START))
   'CR'        ((RESUME))
   END         ((EXIT))
 YOUR CODE? XXXXX   ((WHATEVER))
```

FLAG	FUNCTION IF SET	
	SW 9 SET	SW 9 NOT SET
0	SELECT EXTERNAL SWITCH REGISTER	
1	MAN. SEC. 11 HEAD TEST	AUTO SEC. 01 BASIC CONTROL
2	MAN. SEC 12 START-STOP	AUTO SEC. 02 CONTROL, DS, SPACE
3	MAN. SEC. 13 REEL PROT	AUTO SEC. 03 FM (800 CPI)
4	MAN. SEC. 14 TAPE TEST	AUTO SEC. 04 CRCC, DROP-OUT
	E313 STEP 472 E310 STEP 474	EXPECTED WITH 7970B (D.C. 1643 OR HIGHER)
5	MAN. SEC. 15 WRITE/READ	AUTO SEC. 05 TIMING
6	NOT USED	AUTO SEC. 06 BOT, EOT, CREEPING
7	CONTROL SECTION	AUTO SEC. 07 READ/WRITE
8	OUTPUT TO LINE PRINTER	
9	MANUAL TEST PROCESS	AUTOMATIC TEST PROCESS
10	SUPPRESS NON ERROR PRINTS	
11	SUPPRESS ERROR PRINTS	
12	HALT AFTER A COMPLETE PROGRAM CYCLE	
13	LOOP ON LAST STEP	
14	HALT ON ERROR	
15	HALT AT END OF STEP	

1471004-246

MESSAGES AND HALT ANALYSIS

This program reports to the operator through console or line printer (Control Switch 9) messages and halts. The messages are identified through a unique step number which is prefixed with an alphabetic message class identifier. The message classes are listed below:

D class	Date or information message (Optional print-Switch 10)
E class	Error messages (Optional print-switch 11)
P class	Pause (or Halt) wait for operator action
Q class	Operator information needed

ERROR MESSAGES

Error messages are issued if an error appears and switch 10 is not set. The error message included the number (EXXX), Step number (STEPXXXX) and a text. Some messages have more than 1 line such as listing of SIO program, expected/actual read data or DS. Some of these values are printed in binary form; mostly in octal form.

NON ERROR MESSAGES

All messages from previous paragraph and all D-messages can be printed as non-error messages if switch 11 is set and no error appears.

HALTS

Coded Halts sent by Initialization, Control and all Sections are used to indicate to the operator the reason the program has halted. They are listed below:

HALT NUMBER	SEGMENT NUMBER	
00	20	Unexpected I/O trouble
01		Loader first halt
02		Loader second halt
03		Loader answer to halt 2 < %4000
04	20	No CCE after CIO
05	20	No CCE after RIO
06	20	No CCE after SIN
07	20	No CCE after SIO
10	20	No CCE after TIO
11	20	No CCE after WIO
12	20	Unexpected I/O trouble from LP
13	20	Unexpected I/O from Tape
14	20	Unexpected I/O from Console
15	20	Halt after STEP (SW15 set)
16	20	Error halt (SW14 set)
17	20	Halt after complete cycle (SW12 set)

TOS AFTER HALT
ERROR HALT

S-0 HALT (Halt Code = %16)
S-1 STEP NUMBER XXYY

NON ERROR HALT

S-0 HALT (Halt Code = %17)
S-1 STEP NUMBER XXYY

XX - indicates the section number
YY - indicates the step number

9-TRACK MAG TAPE ONLINE
30115A/7970B/7970E

```
*NEW MAGTEST        ((WHATEVER))
PROGRAM FILE?       PD362A.XXXXXX.XXXXXX
DEVICE?     XX    ((DECIMAL  # OF DRT #))
SET FLAGS?    X,X,X,X,X        ((WHATEVER))
D200 9 TRACK MAG TAPE TEST (HP 32362A.NN.NN) CONFIGURED
*SAVE MAGTEST       ((SAVES IT INTO THE PST))
*ON AND RUN OR RUN MAGTEST
```

FLAGS:

4	PRELIMINARY CONTROLLER TEST
5	READY INTERRUPT TEST
6	COMMAND REJECT TEST
7	SPACING COMMAND TEST
8	FILE MARK RECOGNITION TEST
9	READ AFTER WRITE ERROR TEST
10	READ ERROR TEST
16	1600 DRIVE COMMAND RECOGNITION TEST
17	WRITE/READ TEST
18	TAPE EXCHANGE TEST

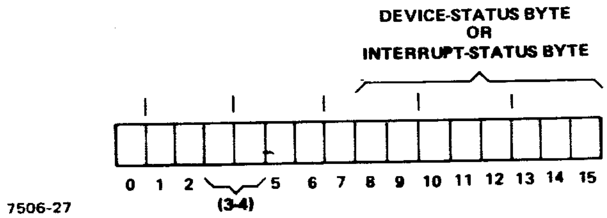
471004-247

CARD READER AND PUNCH

CARD READER & PUNCH
30119A/2894A

DIFFERENCES FROM SERIES II

None.



NOTE: The status word is acquired by a TIO instruction.

BIT FUNCTIONS

Bit 0.	Not used. Remains 1.
Bit 1.	RIO/WIO OK (RWK). When 1, this bit indicates that an RIO or WIO instruction can be performed. A 0 indicates that neither instruction can be performed because data transfer (initiated by a prior RIO or WIO) is taking place between the card reader punch and the interface PCA. RWK is set by completion of data transfer. It can also be set by a CIO instruction which transfers a control word in which bit 0 or bit 6 is 1. The RWK bit becomes 0 at the start of each RIO or WIO instruction.
Bit 2.	Interrupt Pending (INP). A 1 indicates that one or more bits of the interrupt-status byte are 1. The INP bit is cleared by a CIO instruction which transfers a control word in which bit 0 or bit 1 is 1, or in which bits (2-4) clear the pending interrupt.
Bits (3-4).	Sequence Counter (SEQ). These bits are for equipment test and troubleshooting. They indicate the state of the data-transfer sequence counter on the interface PCA. States are as follows:

STATUS WORD BITS		COUNTER STATE	INTERFACE PCA CONDITION
3	4		
0	0	0	No data transfer in progress.
1	0	1	DEV CMD signal sent to card reader punch to initiate data transfer
1	1	2	DEV FLAG signal received from card reader punch to indicate that data transfer is complete
0	1	3	This counter state never attained with card reader punch, except momentarily when passing from 11 to 00.

Bit 5. Device Flag Status (DFS).

- For punching or printing, DFS is set by the FRQ which initiates the action for the entire card. DFS is then cleared by each WIO which transfers punch or print data for one card column. DFS becomes set again when the card reader punch is ready for the next WIO; however, DFS remains clear after the 80th WIO (or 160th if SPD).
- When the computer is acquiring card column data, DFS becomes set when the 80 columns of data are in the card reader punch input memory. DFS then becomes clear when IDT is programmed after each RIO which acquires a column of data. DFS becomes set again when the card reader punch is ready to supply the next card column of data; however, DFS remains clear after the 80th column has been transferred.

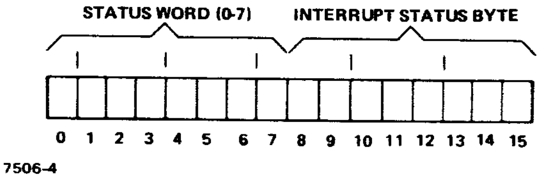
When the DFS bit becomes 1, DTI also becomes 1 (if enabled), and RWK becomes 1.

16-BIT STATUS WORD, BITS (0-7), 1 of 2

Bit 6.	Interrupt/Device Status (IDS). If this bit is 0, bits (8-15) of this status word are the interrupt-status byte. If the IDS bit is 1, bits (8-15) contain the device-status byte. IDS is set or cleared by control word bit 12.
Bit 7.	Not used. Always 0.
Bits (8-15).	Interrupt-status byte or device-status byte.

1471004-249

16-BIT STATUS WORD, BITS (0-7), 2 of 2



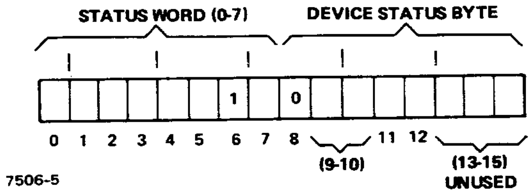
NOTE: Interrupt status bits are cleared by control word bits 0, 1, (2-4).

BIT FUNCTIONS

Bit 8.	Ready for Command Interrupt (RCI). The RCI bit becomes 1 when device-status bit 8 (RFC) becomes 1. After RCI is cleared, it remains 0 until RFC is cleared and returned to 1.
Bit 9.	Ready Interrupt (RIN). RIN becomes 1 when the READY lamp on the card reader punch becomes lighted. After being cleared by a CIO instruction, the RIN bit remains 0 until the READY lamp goes off and again becomes lighted.
Bit 10.	Not Ready Interrupt (NRI). NRI becomes 1 when the READY lamp on the card reader punch goes out. After being cleared by a CIO instruction, the NRI bit remains 0 until the READY lamp lights and goes out again.
Bit 11.	Data Transfer Interrupt (DTI). When enabled by control word bit 11, the DTI bit becomes 1 upon completion of transfer of one card column of data to or from the card reader punch.
Bit 12.	Input Buffer Full Interrupt (IBI). This bit becomes 1 when 80 columns of data from a card have been stored in the input memory in the card reader punch. The IBI bit is also set when a card fails to leave the hopper. The IBI bit does not become set when a card remains in the hopper because the IIF bit was previously set. (IIF is bit 4 of the 6-bit control word.)
Bit 13.	I/O System Interrupt (ISI). This bit becomes 1 when the SIN instruction is performed
Bit 14.	Not used.
Bit 15.	Time Out Interrupt (TOI). When 1, the timer was started (by control-word bit 15), but not terminated within 5 seconds (by bit 0, 1, or 2-4 of another control word).

1471004-250

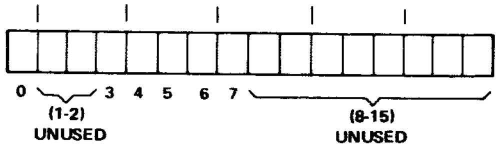
INTERRUPT STATUS BYTE



Bit 8.	Ready For Command (RFC). When RFC is 1, the card reader punch can accept FRQ (control word bit 10), resulting in card feed. RFC is 0 under either of the following conditions. • IBF (R00) is 1. This indicates that the input memory in the card reader punch contains card column data which has not been acquired by an RIO instruction. • The punch memory and/or print memory in the card reader punch has not been filled. (The total amount of data required is 80 card columns for each memory.)
Bits 9 & 10.	Ready (REA). Both bits are 1 when the card reader punch is on-line and the READY lamp is lighted. Both bits are 0 when off-line or not ready.
Bit 11.	Card in Wait Station (CWS). This bit is 1 when a card is in the visible wait station. The bit is cleared by either of the following: • FRQ (control word bit 10) moves the card to a stacker, and IIF (bit 4 of 5-bit control word) prevents another card from entering the visible wait station. • The card is moved to a stacker by momentarily setting the ON-LINE switch down. (If the card reader punch has no keyboard, the RUNOUT switch must be pressed while the ON-LINE switch is down.)
Bit 12.	Secondary Hopper Empty (SHE). This bit is 1, and the HOPPER EMPTY lamp is lighted, when the front input hopper is empty. The bit is cleared by the following steps: • Place cards in the secondary hopper. • Press the STOP switch. (Press twice if the card reader punch has a keyboard.) • Press the START switch.
Bits (13-15).	Not used.

1471004-251

DEVICE STATUS BYTE



7506-6

NOTE: The 6-bit status word is acquired by an RIO instruction. When the instruction is executed, the card reader punch input memory must be empty.

BIT FUNCTIONS

Bit 0.	Input Buffer Full (IBF). This bit must be 0. If it is 1, the RIO instruction which acquired this word obtained it from the input memory, which was not empty. The input memory is cleared by programming CBF (bit 0 of the 5-bit control word), or by executing sufficient RIO's to read all data from the input memory.
Bits 1-2.	Not used.
Bit 3.	Read Check (RCH). When 1, the RCH bit indicates that a read check error occurred when a card was read. (In a read check error a punched hole is displaced to the left or right of its proper position. A read check error also occurs when a card is picked, but does not leave the hopper.) When the RCH bit is set, the READ CHECK lamp lights. The RCH bit is cleared in the 6-bit status word, and the READ CHECK lamp is extinguished, by either of the following: • Execution of a CIO instruction to transfer a control word in which bit 10 (FRQ) is 1. • Pressing the START switch.
Bit 4	Input Check (ICH). This bit becomes 1 when a card fails to reach the visible wait station within 200 milliseconds after FRQ (control bit 10) is programmed and when, also, IIF (bit 4 of the 5-bit control word) allows card feeding. The fault results from failure of a card to leave the hopper, or a card jam between the hopper and the visible wait station. When ICH becomes 1, the REA bits (device status bits 9 and 10) both become 0, the INPUT CHECK lamp lights, and the READY lamp goes out. The ICH bit is cleared by performance of the following in the sequence stated: • If the card reader punch has a keyboard, momentarily set the ON LINE/OFF switch to OFF. • Press the STOP switch. • Clear the card jam (if any). • Press the START switch.
Bit 5.	Output Check (OCH). The OCH bit becomes 1 when the upper front cover is opened or when there is a card jam between the punch station and the stacker. When OCH becomes 1, the REA bits (device status bits 9 and 10) both become 0, the STACKER CHECK lamp lights, and the READY lamp goes out. The OCH bit is cleared in the same manner as the ICH bit.

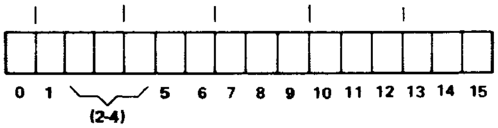
1471004-252

6-BIT STATUS WORD, 1 of 2

Bit 6.	Primary Hopper Empty (PHE). This bit is 1 when the rear hopper is empty. The bit is cleared as follows: • Load cards in the hopper. • Press the STOP switch. (Press twice if the card reader punch has a keyboard.) • Press the START switch.
Bit 7.	Stacker Full (STF). In stacker control operation, this bit is 1 when either stacker is full. In stacker select operation, the STF bit is 1 when stacker 2 (left stacker) is full. (Stacker control and stacker select operation are established by bits 1 and 2 of the 5-bit control word.) When STF is 1 the STACKER FULL lamp is lighted. The STF bit is cleared and the lamp extinguished by emptying the stacker and pressing the START switch.
Bits (8-15).	Not used.

1471004-253

6-BIT STATUS WORD, 2 of 2



7506-9

NOTE: The 16-bit control word is transferred to the interface PCA by a CIO instruction. The control word is stored on the interface PCA until bits are cleared as follows:

a. Control word bits 0, 1, 2, 3, 4, and 5 always becomes clear immediately after performing their function.

b. The entire control word is cleared to zero when either of the following takes place:

(1) An I/O reset occurs.

(2) Another control word which has 1 in position 0 is sent to the interface PCA by a CIO instruction.

c. A particular bit of the control word is cleared when another control word, with 0 in that bit position, is sent to the interface PCA by a CIO instruction.

BIT FUNCTIONS

Bit 0. Master Clear (MAC). When 1, this bit clears the interface PCA. The result in the subsystem is the same as when an I/O reset occurs.

Bit 1. Clear All Interrupts (CAI). When 1, this bit clears all interrupt pending flip-flops on the interface PCA. The interrupt timer is reset. Bits (8-15) of the interrupt status byte are cleared. Bit 2 of the status word (Interrupt Pending Bit) is cleared.

Bits (2-4). Selective Interrupt Clear (SIC). Functions are as follows:

CONTROL WORD BITS			**INTERRUPT STATUS BIT CLEARED**	**INTERRUPT CONDITION CLEARED**
2	**3**	**4**		
0	0	0	None.	None.
0	0	1	Bits 14 and 15.	Clear transfer error interrupt and time-out interrupt.*
0	1	0	Bit 13.	Clear programmed interrupt.
0	1	1	Bit 12.	Clear input buffer full interrupt.
1	0	0	Bit 11.	Clear data transfer interrupt.
1	0	1	Bit 8.	Clear ready-for-command interrupt.
1	1	0	Bit 9.	Clear ready interrupt.
1	1	1	Bit 10.	Clear not-ready interrupt.

*Also terminates the 5-second I/O time-out cycle,without an interrupt, if issued during the 5-second cycle.

Bit 5. Initiate Data Transfer (IDT). When 1, this bit initiates transfer of one card-column data word from the card reader punch input memory to the computer. IDT must be programmed after each RIO instruction which acquires card-column data.

Bit 6. Set Device End (SDE). When 1, this bit clears the sequence counter on the interface PCA. The SDE bit must be set by a CIO instruction immediately after:

- A WIO instruction has transferred a 5-bit control word to the interface PCA.
- Execution of the last of a series of WIO's and/or RIO's which transfer data for one card.

The SDE bit must be set, then cleared, by *consecutive* CIO instructions. If the bit is set after a WIO instruction, it immediately sets DTI (bit 11 of the interrupt status byte); to prevent this, DTE (control word bit 11) must be cleared by the same CIO instruction which sets SDE.

Bit 7. Print (PRI). When 1, this bit prepares the card reader punch for printing in one or more columns of a card. Bit 8 (Punch Bit) of the same control word may also be 1, and bit 9 (Separate Print Data Bit) may be 1. Results are as follows:

- If bits 7, 8, and 9 are 111, 160 WIO instructions are programmed to follow. The first 80 WIO's fill the punch memory in the I/O device with 80 card columns of data for punching. (If no punching is desired, these columns are Hollerith blanks.) The 81st through 160th WIO instructions fill the print memory in the I/O device with 80 card columns of Hollerith data for printing.
- If bits 7, 8, and 9 are respectively 110, 80 WIO instructions are programmed to follow. These fill the punch memory and print memory in the I/O device with 80 card columns of data to be punched and printed. The Hollerith character punched in each column is printed at the head of the column.
- If bits 7, 8, and 9 are respectively 100, 80 WIO instructions are programmed to follow. These fill the print memory in the I/O device with 80 columns of data to be printed.

Data is printed or punched on a first-in-first out basis. That is, the first WIO-supplied print or punch character appears in column 1 of the card, the second character supplied appears in column 2, etc.

Bit 8. Punch (PUN). When 1, this bit prepares the I/O device for punching in one or more columns of a card.

Bit 9. Separate Print Data (SPD). When 1, this bit prepares the I/O device for printing data other than that which is punched.

Bit 10. Feed Request (FRQ). When 1, this bit causes card movement if device status-byte bit 8 (RFC) is 1. FRQ must be programmed twice to move a card from the hopper to the stacker. The first FRQ moves the card to the visible wait station. The second FRQ moves the card to the hopper. Each time FRQ is programmed, the following takes place:

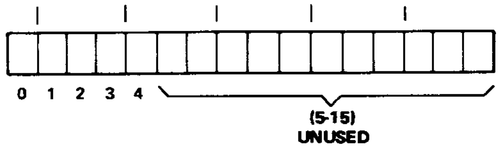
- If no card is in the visible wait station, a card is moved from an input hopper to the visible wait station. However, this occurs only if the last IIF bit programmed was 0.
- If a card is in the visible wait station, it is moved to a stacker. Card motion starts immediately if the card will not be punched or printed. If punching and/or printing are programmed, card motion does not start until 80 WIO's (160 for SPD) have filled the punch memory or print memory. When card motion starts, another card moves from a hopper to the visible wait station if the last IIF bit programmed was 0.

In the above operations, the hopper and stacker were previously selected by a 5-bit control word.

Bit 11.	Data Transfer Interrupt Enable (DTE). When 1, this bit allows interrupt status-byte bit 11 to be set.
Bit 12.	Device Status Enable (DSE). When DSE is 1, interrupt status is furnished in bits (8-15) of the status word. When this bit is 1, device status is furnished instead.
Bit 13.	Byte Transfer (BYT). Must be 0.
Bit 14.	Enable Interrupt Requests (EIR). When this bit is 1, interrupt requests can be sent to the CPU. When this bit is 0, interrupt bits can be set in the interrupt status word, but interrupt requests cannot be made.
Bit 15.	Start Transfer Timer (STT). When this bit is set to 1. a 5-second time-out delay is started. If the bit is not cleared within 5 seconds, bit 15 of the interrupt status word is set.

1471004-256

16-BIT CONTROL WORD, 3 of 3



7506-10

NOTE: Each 5-bit control word is transferred to the interface PCA by a WIO instruction. The word is stored on the PCA until one of the following occurs:

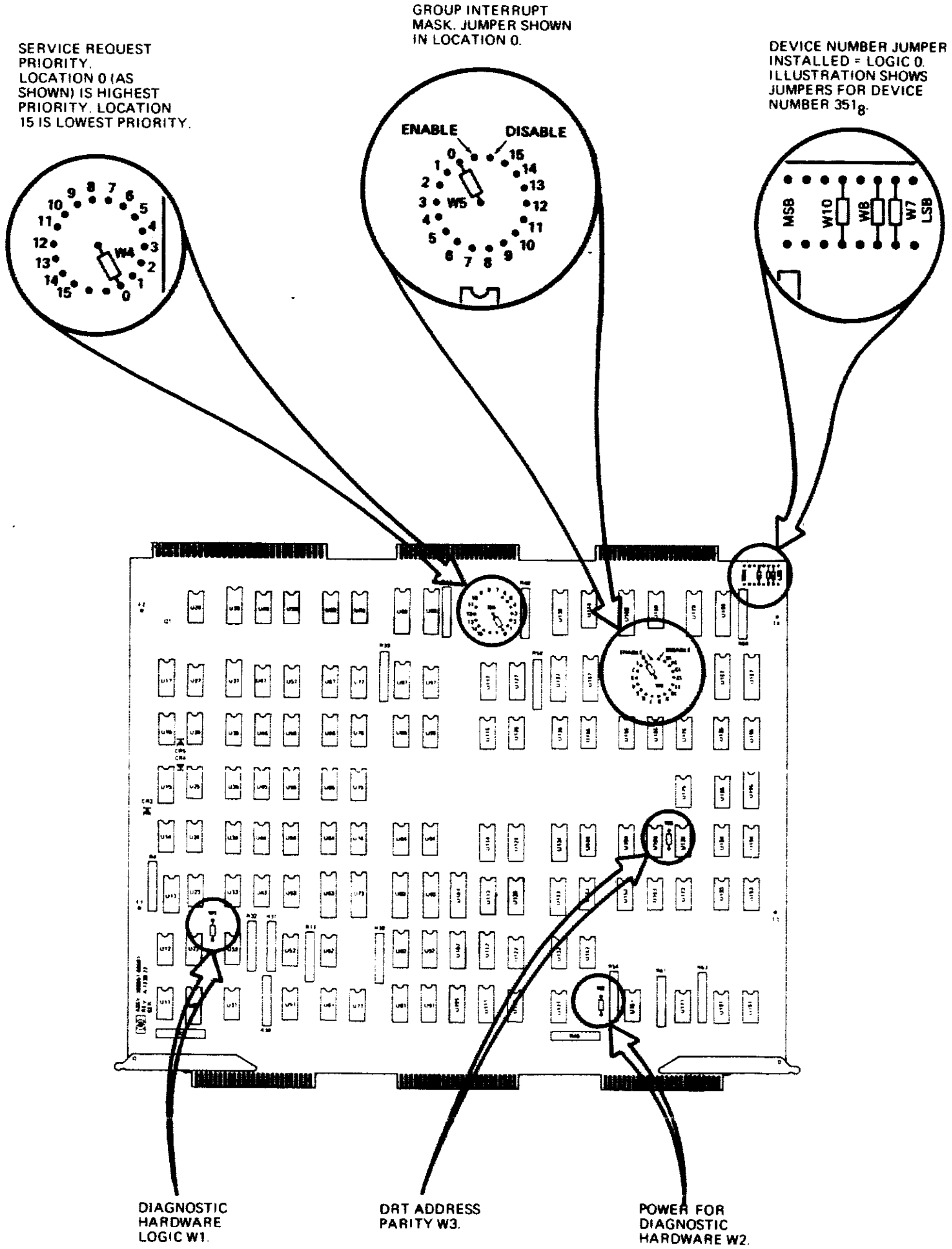
- Another WIO instruction is executed. (However, bit 1 below is not affected.)
- A CIO instruction transfers to the interface PCA a 16-bit control word in which bit 0 (Master Clear) is 1. (Bit 1 below is not affected.)
- An I/O reset occurs. (Bit 1 below is not affected.)

BIT FUNCTIONS

Bit 0.	Clear Buffer Full (CBF). When CBF is 0, 80 columns of data from the next card leaving the hopper will be stored in the card reader punch input memory. The storing takes place as the card passes the read station. When CBF is 1, data in the input memory is cleared as the next card passes the read station. Also, when CBF is 1 the IBF bit is cleared; as a result, an RIO instruction acquires the 6-bit status word rather than a word from the input memory. (The IBF bit is bit 0 of the 6-bit status word. Refer to tables 2-2 and 2-8.) When the CBF bit is programmed as 1, the SDE bit must be programmed as 1 immediately after to transfer the sequence counter on the interface PCA from the 10 state to 00. (SDE is control word bit 6. Refer to table 2-3.)
Bit 1.	Stacker Control Mode (SCM). • When SCM is 0, cards are discharged to stacker 1 (right-hand stacker). When stacker 1 is full, cards are discharged to stacker 2. • When SCM is 1, the SST bit (below) determines the stacker used. After SCM has been returned to 0, the card reader punch must be momentarily placed off-line before the 1 bit can again be effective. This is done by momentarily setting the ON-LINE switch to the down position.
Bit 2.	Select Stacker Two (SST). This bit is enabled when bit 1 above is 1. When the SST bit is 1, cards are stacked in stacker 2 (left-hand stacker). When SST is 0, stacker 1 is used.
Bit 3.	Secondary Hopper Select (SHS). When this bit is 1, cards are acquired from the secondary (front) hopper. When the SHS bit is 0, the primary (rear) hopper is used.
Bit 4.	Inhibit Input Feed (IIF). When 1, this bit prevents a card from being acquired from either input hopper. However, a card in the visible wait station can move to the stacker.
Bits (5-15).	Not used.

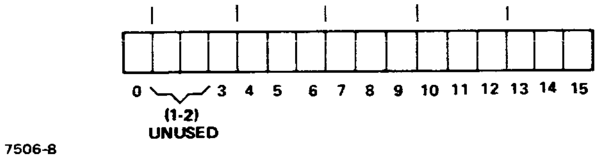
1471004-257

5-BIT CONTROL WORD



471004-258

INTERFACE PCA JUMPER LOCATIONS



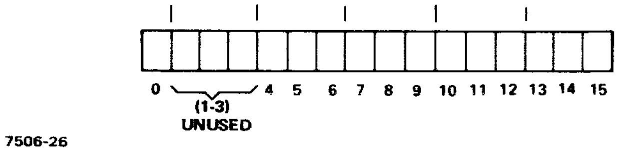
NOTE: When this word is acquired by an RIO instruction, the card reader punch input memory must not be empty. (IBF must be 1.)

BIT FUNCTIONS

Bit 0.	Input Buffer Full (IBF). This bit must be 1. IBF becomes 1 when 80 columns of data have been read from a card and stored in the input memory. IBF becomes 0 when 80 RIO instructions have been executed to acquire the data. IBF also becomes 0 when CBF is programmed. (Refer to bit 0, table 2-8.)
Bits (1-2).	Not used.
Bit 3.	Read Check (RCH). If this bit is 1, a read check occurred when one or more columns in the card were read. (Refer to bit 3, table 2-8.) This bit is set in all 80 16-bit words, regardless of the card column(s) which provided the read check.
Bit 4.	Bit read from card row 12.
Bit 5.	Bit read from card row 11.
Bits (6-15).	Bits read from card rows 0-9 respectively.

1471004-259

DATA WORD (READ)



Bit 0.	Clear Buffer Full (CBF). This bit performs the same function as the CBF bit (bit 0) in the 5-bit control word. (Refer to table 2-4.) In a write data word, CBF can be 0 or 1 for all columns except the 80th (or 160th if SPD). If CBF is 1 in the 80th (or 160th) write word, the next card leaving the hopper is not read unless CBF is first cleared by means of a 5-bit control word.
Bits (1-3).	Not used.
Bit 4.	Bit for card row 12.
Bit 5.	Bit for card row 11.
Bits (6-15).	Bits for card rows 0-9 respectively.

1471004-260

DATA WORD (WRITE)

CARD READER PUNCH			INTERFACE PCA		
SIGNAL ABBREVIATION	SIGNAL NAME	PCA PIN	SIGNAL ABBREVIATION	SIGNAL NAME	PCA PIN
CBF	Clear Buffer Full LO	J14-R	BIT 0	Data Out Bit 0	J3-25
CWS*	Card In Wait Station LO	J14-T	BIT 11*	Status Bit 11	J2-45
FRQ	Feed Request LO	J14-P	BIT 10	Control Bit 10	J1-37
IBF*	Input Buffer Full LO	J14-U	BIT 0*, IBI*	Data In Bit 0, Input Buffer Full Interrupt	J3-41, J2-47
OBA*, PBA*, IDA*	Output Buffer Available LO, Print Buffer Available LO, Input Data Available LO	J15-d, J15-c, J14-V	DEV FLAG*	Device Flag	J1-3
I00*/PHE*	Input Data 0 LO/Primary Hopper Empty LO	J14-X	BIT 6*	Data In Bit 6	J3-31
I01*/STF*	Input Data 1 LO/Stacker Full LO	J14-N	BIT 7*	Data In Bit 7	J3-29
I02*	Input Data 2 LO	J14-A	BIT 8*	Data In Bit 8	J1-17
I03*	Input Data 3 LO	J14-B	BIT 9*	Data In Bit 9	J1-31
I04*	Input Data 4 LO	J14-D	BIT 10*	Data In Bit 10	J1-27
I05*	input Data 5 LO	J14-f	BIT 11*	Data In Bit 11	J1-29
I06*	Input Data 6 LO	J14-e	BIT 12*	Data In Bit 12	J1-23
I07*	Input Data 7 LO	J14-d	BIT 13*	Data In Bit 13	J1-25
I08*	Input Data 8 LO	J14-b	BIT 14*	Data In Bit 14	J1-19
I09*	Input Data 9 LO	J14-c	BIT 15*	Data In Bit 15	J1-21
I11*/OCH*	Input Data 11 LO/Output Check LO	J14-a	BIT 5*	Data In Bit 5	J3-35
I12*/ICH*	Input Data 12 LO/Input Check LO	J14-L	BIT 4*	Data In Bit 4	J3-33
LOB, NDR	Load Output Buffer LO, New Data Request LO	J15-U, J14-S	DEV CMD	Device Command	J1-39
O00	Output Data 0 LO	J15-B	BIT 6	Data Out Bit 6	J3-23
O01	Output Data 1 LO	J15-A	BIT 7	Data Out Bit 7	J3-19
O02	Output Data 2 LO	J15-f	BIT 8	Data Out Bit 8	J1-33
O03	Output Data 3 LO	J15-e	BIT 9	Data Out Bit 9	J1-45
O04	Output Data 4 LO	J15-Y	BIT 10	Data Out Bit 10	J1-47
O05	Output Data 5 LO	J15-X	BIT 11	Data Out Bit 11	J1-49
O06	Output Data 6 LO	J15-a	BIT 12	Data Out Bit 12	J1-15
O07	Output Data 7 LO	J15-b	BIT 13	Data Out Bit 13	J1-13

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CONNECTIONS, CARD PUNCH: INTERFACE PCA, 1 of 2

CARD READER PUNCH			INTERFACE PCA		
SIGNAL ABBREVIATION	SIGNAL NAME	PCA PIN	SIGNAL ABBREVIATION	SIGNAL NAME	PCA PIN
O08	Output Data 8 LO	J15-W	BIT 14	Data Out Bit 14	J1-43
O09	Output Data 9 LO	J15-Z	BIT 15	Data Out Bit 15	J1-41
O11	Output Data 11 LO	J15-H	BIT 5	Data Out Bit 5	J3-21
O12/IIF	Output Data 12 LO/Inhibit Input Feed LO	J15-V	BIT 4	Data Out Bit 4	J3-3
PRI	Print LO	J15-P	BIT 7	Control Bit 7	J3-9
PUN	Punch LO	J15-N	BIT 8	Control Bit 8	J3-7
REA*	Ready LO	J14-K	BIT 9*, BIT 10*	Status Bit 9, Status Bit 10	J1-11, J1-9
RFC*	Ready for Command LO	J14-W	BIT 8*	Status Bit 8	J1-1
SCM	Stacker Control Mode LO	J14-F	BIT 1	Data Out Bit 1	J3-15
SHE*	Secondary Hopper Empty LO	J15-S	BIT 12	Status Bit 12	J3-27
SPD	Separate Print Data LO	J15-J	BIT 9	Control Bit 9	J2-41
SST	Select Stacker Two LO	J14-J	BIT 2	Data Out Bit 2	J3-1
–	(Not connected)	–	W2	Jumper 2, Jumper 2	J2-9, J2-10
–	(Not connected)	–	W4	Jumper 4, Jumper 4	J2-13, J2-14
–	(Not connected)	–	W5	Jumper 5, Jumper 5	J2-15, J2-16
–	(Not connected)	–	W6	Jumper 6, Jumper 6	J2-21, J2-22
–	(Not connected)	–	W7	Jumper 7, Jumper 7	J2-35, J2-36
–	(Not connected)	–	W8	Jumper 8, Jumper 8	J2-37, J2-38
–	(Not connected)	–	SDE	Control Bit 6, Device End	J3-5, J2-49

Notes: An asterisk indicates signal origin is in card reader punch. Otherwise, signal origin is in the interface PCA.

In the PCA PIN columns, a comma indicates connection (in the plug) to the pin listed on the line beneath.

Each signal in this table has a signal-return wire. The return wire is connected to the pin matching that listed for the signal. Matching pins are on opposite sides of the PCA. For instance, the return wire for signal SST connects to pin J14-8 in the card reader punch. The other end of the same return wire connects to J3-2 on the interface PCA. On the card reader punch the return wires connect to *numbered* pins. On the interface PCA the return wires connect to *even*-numbered pins.

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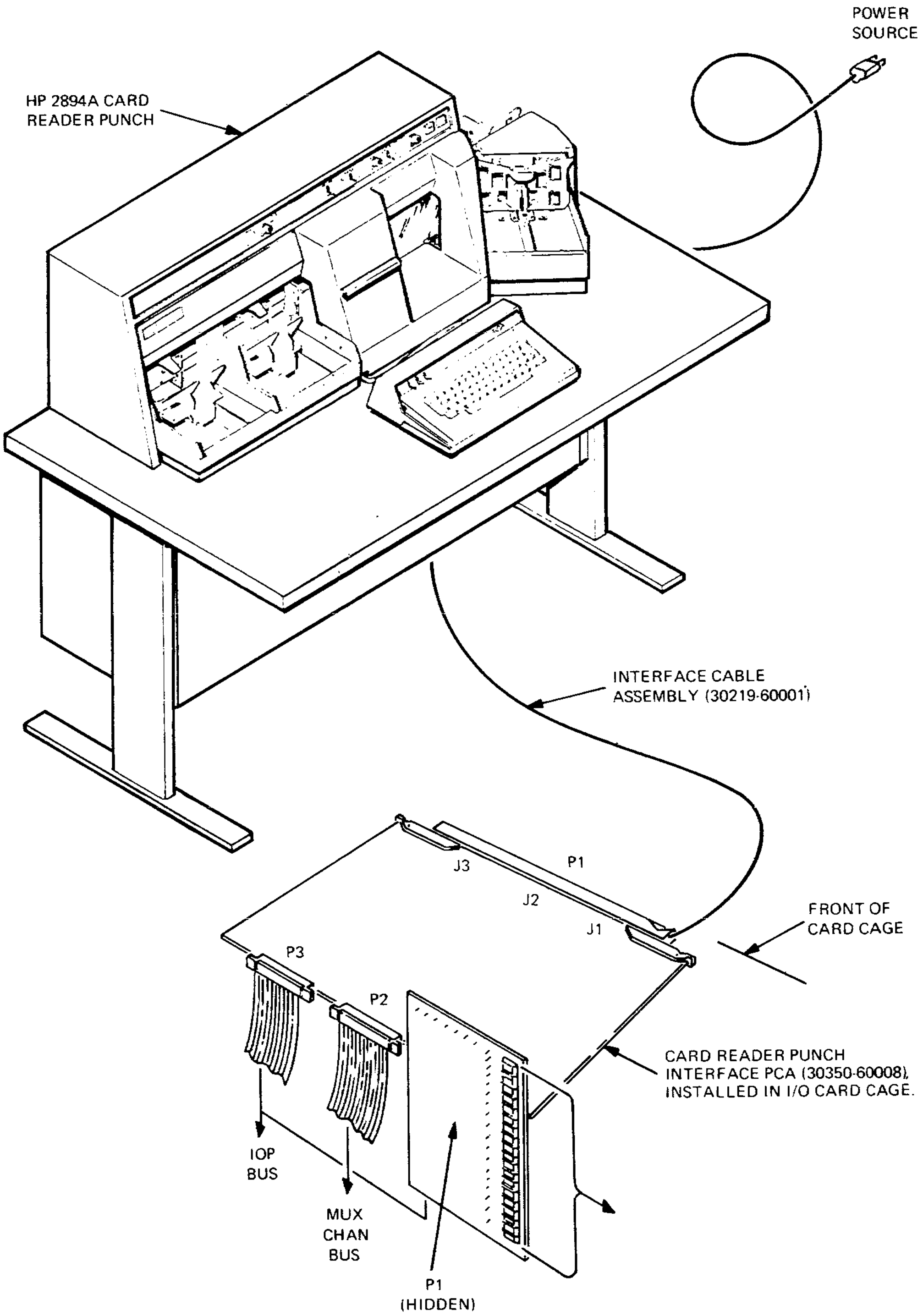
CONNECTIONS, CARD PUNCH: INTERFACE PCA, 2 of 2



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SUBSYSTEM CONNECTIONS

DIAGNOSTICS STAND-ALONE

Card Reader and Punch S-A
30119A/2894A

COLD LOAD DIAG FILE # FROM NONCPU COLD LOAD TAPE
D100 RDR/PUNCH DIA (D336A.XX) DEVICE = ddd D100 ddd
Q110 DEVICE NUMBER? XX ((DECIMAL # OF DRT))
Q111 INTERRUPT MASK? X ((ENTER E FOR ENABLE))
Q112 NEGATIVE TRUE? NO/YES ((NO = 30050 60003,
YES = 30050 60001 OR 60008))
P113 INTERNAL SWITCH REGISTER ((SET B REG THEN PRESS RUN/HALT))
Q114 SECTION LIST? X,X,X,X,X ((WHATEVER))

SWITCH REGISTER	(FUNCTION WHEN SET)
0	OVERRIDES THE INTERNAL SWITCH REGISTER
1-3	# OF WORDS FOR STEPS 320 AND 321
4	SHORTEN ALL MESSAGES
5	ADD PROGRAM SECTIONS
6	DELETE PROGRAM SECTIONS
7	SKIP TO END OF CURRENT SECTION
8	PRINT ALL MESSAGES
9	PRINT ALL MESSAGES ON LINE PRINTER
10	HALT AT END OF EACH SECTION
11	SUPPRESS ALL MESSAGES
12	HALT AT END OF PROGRAM
13	LOOP ON CURRENT STEP
14	HALT ON ERROR
15	HALT AT END OF STEP

SECTION NUMBER	NAME
0	CONFIGURATION
1	HP 30049B DIAGNOSTIC HARDWARE USER CHECKS
2	HP 30049B DIAGNOSTIC HARDWARE PROGRAM TESTS
3	DATA TRANSFER AND DEVICE STATUS BYTE TESTS
4	DEVICE STATUS INTERRUPT BIT TESTS
5	INTERFACE INTERRUPT STATUS BIT TESTS
6	INTERRUPT TESTS
7	SIO TESTS
8	SIO-DEVICE END TESTS
9	JUMPER OPTION TESTS
10	BASIC FUNCTIONS
11	WRITE-READ FUNCTIONS
12	DEVICE END FUNCTIONS
13	(NONE)

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CARD READER PUNCH ONLINE

30119/2894A

```
*NEW CDRDRPCH     ((WHATEVER))
PROGRAM FILE?     PD379A.XX.X
DEVICE?    XX    ((DECIMAL #OF DRT))
SET FLAGS?    X,X,X,X,X
Q105 KEYBOARD VERSION?    ((YES/NO))
D106 HP 2894A CARD READER PUNCH DIAG (D379.XX.X) CONFIGURED
*SAVE CDRDRPCH     ((SAVES IT INTO PST))
*ON AND RUN OR RUN CDRDRPCH
```

FLAG	FUNCTION IF SET
1	INTERFACE TEST
2	READY STATUS – INTERRUPT TEST
3	HOPPER-STACKER TEST
4	ERROR STATUS TEST
5	PUNCH READ CHECK CARDS
6	READ CHECK STATUS TEST
7	PUNCH-PRINT CARDS A-K
8	PUNCH CARD 0
9	PUNCH CARDS 1-15
10	READ CARDS A-K
11	READ CARD 0
12	READ CARDS 1-15
13	CARD SPEED TEST
14	FEED CARDS
15	INTERPRET CARDS
16	DUPLICATE CARDS
17	PUNCH OPERATOR'S CARD
18	READ OPERATOR'S CARD
25	PAUSE AT END OF SECTION
26	PAUSE AT END OF PASS
27	SUPPRESS TITLE MESSAGES
28	PRINT ALL MESSAGES
NP	NO PRINT
PA	PAUSE AFTER EACH STEP
LP	LOOP ON CURRENT STEP OR STEPS

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ADDITIONAL TERMINALS
SUPPORTED ON HP 3000 PRE SERIES II

Term Type	Terminal	Misc. Info
0	ASR 33/35	
1	*ASR 37	
2	DCT 500	
3	EXECUPORT 300	
4	DATAPOINT 3300	
5	MEMOREX 1240	
6	GE TERMINET	
7	*IBM 2741	Call 360
8	*IBM 2741	PTTC/EBCDIC
9	MINI-BEE	
10	HP 264X	Cartridge capability not supported via FCOPY utility.

*Must be configured as SUB-TYPE =1 when hardwired

TERMINET ONLINE
30120A/2762A/B

```
*NEW CONSOLE        ((WHATEVER))
PROGRAM FILE?       PD375A.XXXXXX.XXXXXX
DEVICE?     XX     ((DECIMAL # OF DRT #))
SET FLAGS?    X,X,X,X,X        ((WHATEVER))
Q1 SPECIFY CPS (10/15/30)?     XX
Q2 TAB OPTION (Y OR N)?  Y OR N
D9 END CONFIGURATION
*SAVE CONSOLE       ((SAVES IT INTO THE PST))
*ON AND RUN OR RUN CONSOLE
```

FLAGS:

1	PRINTER TEST
2	KEYBOARD TEST
3	NULL CHARACTER TEST
4	HORIZONTAL TAB TEST
5	ALL CAPS SWITCH TEST
6	OPERATOR DESIGNED TEST
12	PRINT END OF SECTION MSG
13	PAUSE AT COMPLETION OF SECTION
14	SUPPRESS HEADER MSG
15	SUPPRESS COMPLETION MSG

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TERMINET ONLINE DIAGNOSTIC

Use Tally Oil (HP 6040-0244) as a lubricant for all main shaft, clutches, idler pulleys, etc. DO NOT lubricate the ribbon reversal clutches.

2615 CRT ONLINE

30122/2615A

THE 2615A ON-LINE DIAGNOSTIC MAY BE RUN UNDER EITHER MPE/3000 OR SDM/3000

```
:RUN  PD378A  ((UNDER MPE))

*NEW CRT              ((WHATEVER UNDER SDM))
PROGRAM FILE?       PD378A.XX.X
DEVICE?     XX     ((DECIMAL # OF DRT))
SET FLAGS?    X,X,X,X,X        ((WHATEVER))
Q1 SPECIFY CPS (10, 15, 30, 60, 120, 240)?  ((WHATEVER))
D2 END CONFIGURATION
*SAVE CRT             ((SAVES IT INTO PST))
*ON AND RUN OR RUN CRT
```

FLAG	FUNCTION IF SET
1	EXECUTE SECTION 1 – MEMORY TEST
2	EXECUTE SECTION 2 – DOT MATRIX
3	EXECUTE SECTION 3 – CHARACTER SET
4	EXECUTE SECTION 4 – KEYBOARD
5	EXECUTE SECTION 5 – CURSOR FUNCTIONS
6	EXECUTE SECTION 6 – ERASE FUNCTIONS
7	EXECUTE SECTION 7 – CALIBRATION
8-10	NOT USED
11	NO DISPLAY PAUSE
12	PRINT SECTION END MESSAGE
13	PAUSE AT SECTION END
14	SUPPRESS HEADER MESSAGE
15	SUPPRESS COMPLETION MESSAGE
PA	PAUSE AFTER EACH STEP
NP	NO PRINT
LP	LOOP ON CURRENT STEP
CS	CYCLE SECTION
CP	CYCLE PROGRAM

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2615 CRT ONLINE DIAGNOSTIC

2600 CRT ONLINE

30123/2600A

```
*NEW CRT              ((WHATEVER))
PROGRAM FILE?     PD371A.XX.X
DEVICE?    XX    ((DECIMAL # OF DRT))
SET FLAG?     X,X,X,X,X       ((WHATEVER))
Q1 SPECIFY BAUD RATE?  ((110, 150, 300, 600, 1200 OR 2400))
Q2 SPECIFY INTERFACE?  ((1⇒TCI, 0⇒SYS TIMER/CONSOLE))
D9 END CONFIGURATION
*SAVE CRT             ((SAVES IT INTO PST))
*ON AND RUN OR RUN CRT
```

FLAG	FUNCTION IF SET
1	SELECT SECTION 1 – CHARACTER TEST
2	SELECT SECTION 2 – MOS? @ TEST
3	SELECT SECTION 3 – DOT MATRIX TEST
4	SELECT SECTION 4 – SPOW AND ERASE TEST
5	SELECT SECTION 5 – CURSOR AND DISPLAY TEST
6	SELECT SECTION 6 – KEYBOARD TEST
7	SELECT SECTION 7 – OSCILLATOR TEST
8	SELECT SECTION 8 – CALIBRATION TEST
9	SELECT SECTION 9 – OP DESIGN SECTION
10,11	NOT USED
12	PRINT SECTION END MESSAGE
13	PAUSE AT END OF SECTION
14	SUPPRESS HEADER MESSAGE
15	SUPPRESS DIAGNOSTIC COMPLETION MESSAGE

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2600 CRT ONLINE DIAGNOSTIC

TELETYPE ONLINE

30124A/2749B (ASR33)

```
*NEW CONSOLE        ((WHATEVER))
PROGRAM FILE?       PD367A.XXXXXX.XXXXXX
DEVICE?     XX     ((DECIMAL # OF DRT #))
SET FLAGS?    X,X,X,X,X          ((WHATEVER))
D5 END CONFIGURATION
*SAVE CONSOLE       ((SAVES IT INTO THE PST))
*ON AND RUN OR RUN CONSOLE
```

FLAGS:

1	PRINTER TEST
2	KEYBOARD TEST
3	PUNCH TEST
4	READER TEST
5	OPERATOR DESIGNED TEST
6	REPORT ONLY FIRST ERROR PER STEP
8	PAUSE AT COMPLETION OF SECTION
9	SUPPRESS HEADER MSG
10	SUPPRESS COMPLETION MSG

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TELETYPE ONLINE DIAGNOSTIC

2640A/B INTERACTIVE DISPLAY
TERMINAL ONLINE

2640 DIAGNOSTIC DOES NOT RUN UNDER SDM, ALTHOUGH IT IS FOUND IN THE HPONLN GROUP

```
:RUN  PD369A  ((UNDER MPE/3000))
D369A.00.0  HP2640A INTERACTIVE DISPLAY
   TERMINAL DIAGNOSTIC
>SET  X,X,X,X,X   ((WHATEVER FLAGS))
```

FLAG	FUNCTION IF SET
1	PROCESSOR TEST
2	FIRMWARE TEST
3	MEMORY TEST
4	ADDRESSING TEST
5	CURSOR CONTROL TEST
6	DISPLAY TEST
7	DOT MATRIX TEST
8	CHARACTER SET
9	CALIBRATION PATTERNS
10	EXTENDED DISPLAY ENHANCEMENTS TEST
11	ALTERNATE CHARACTER SET TEST
12	KEYBOARD TEST
13	FREE INPUT
14	KEYBOARD SWITCHES TEST
15	KEYBOARD LIGHTS TEST

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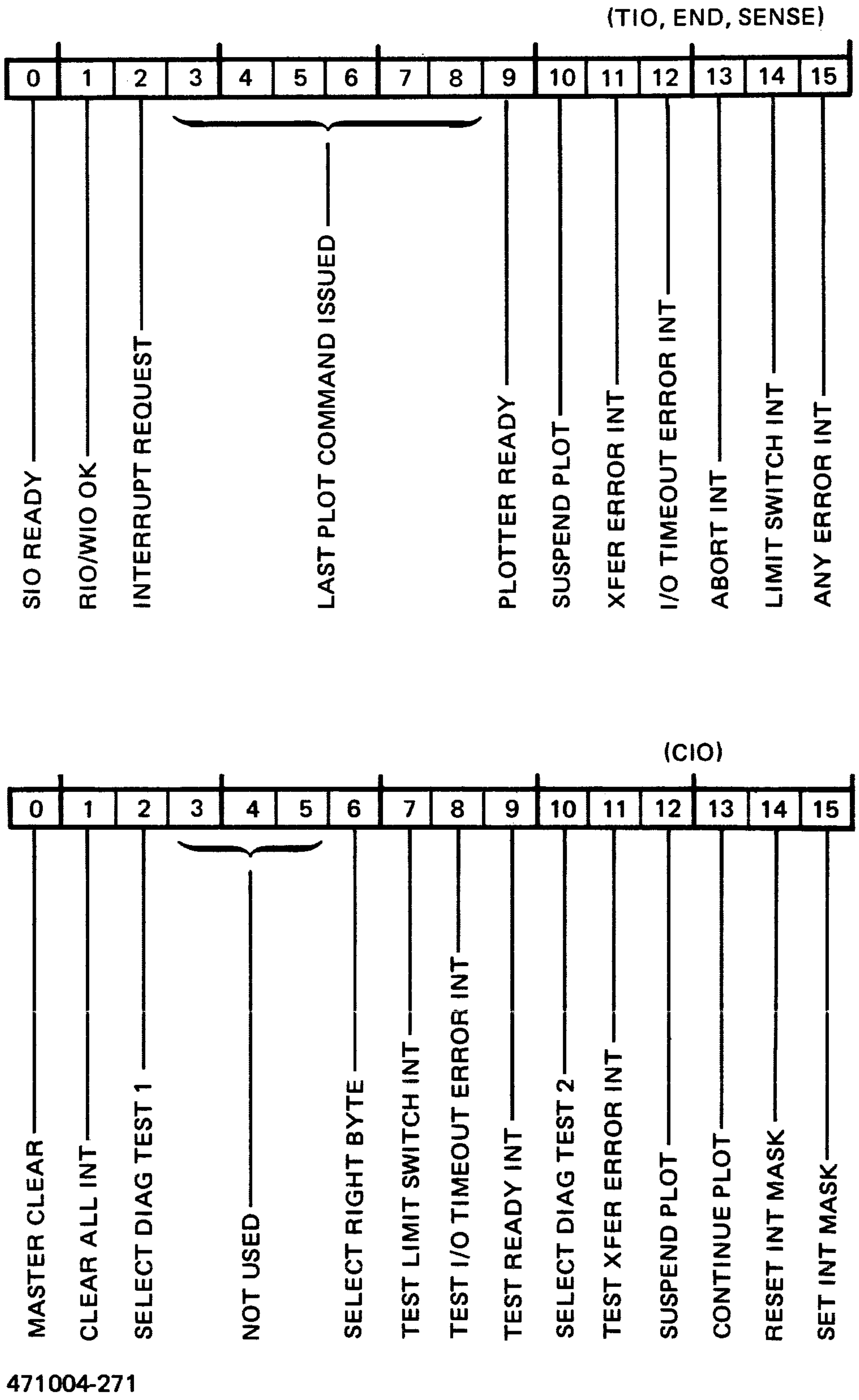
2640A/B INTERACTIVE DISPLAY ONLINE DIAGNOSTIC

PLOTTER INTERFACE 30126A
HP 30226A

DIFFERENCES FROM SERIES II

None.



STATUS/CONTROL WORDS

DIAGNOSTIC TEST HOOD JUMPER FUNCTIONS, sheet 1 of 2

JUMPER CONNECTION		FUNCTION
FROM	TO	
A4 (J1-7)	A5 (J1-9)	Connects the clear-side of the Limit-Switch Diagnostic flip-flop (U141B) to the clock input of the Limit Switch Interrupt flip-flop (U38B). Permits the diagnostics to check the limit switch interrupt function.
B5 (J1-100	A6 (J1-11)	Connects the +5V supply to the VIN (J1-11) pin on the plotter interface PCA to provide +5V plotter input signals rather than the normal +15V signals.
B8 (J1-16)	A7 (J1-13)	Grounds the input to inverter (U26D) to force the Good Data Clock signal active. This enables all plot command data transfer circuitry decoders.
A7 (J1-13)	A12 (J1-23)	Grounds one input to the diagnostic multiplexer (U154) to cause bit 3 of the diagnostic status word to be a "0" when series 600/700 plot command data is selected, i.e., when the select line is inactive.
A12 (J1-23)	A25 (J1-49)	Grounds the enable line of the diagnostic multiplexer (U154 and U164). This allows either series 500 or series 600/700 plot command data to be provided as part of the diagnotic status word (bits 3 through (8).
A9 (J1-17)	A15 (J1-29)	Simulates the clock jumper W1 to ensure that the full step clock output will be used during all diagnostic testing.
A10 (J1-19)	A17 (J1-33)	Connects data out bits 3 or 11 (series 600/700) to the input of the diagnostic multiplexer (U154) to provide bit 4 of the diagnostic status word when the select line is inactive.
A11 (J1-21)	B23 (J1-46)	Connects the pen down plot command (series 500) to the input of the diagnostic multiplexer (U154) to provide bit 4 of the diagnostic status word when the select line is active.

471004-272/273, 1 of 2

DIAGNOSTIC TEST HOOD JUMPER FUNCTIONS, sheet 2 of 2

JUMPER CONNECTION		FUNCTION
FROM	TO	
A13 (J1-25)	A23 (J1-45)	Connects the pen up plot command (series 500) to the input of the diagnostic multiplexer (U154) to provide bit 3 of the diagnostic status word when the select line is active.
A14 (J1-27)	A22 (J1-43)	Connects the +Y plot command (series 500) to the input of the diagnostic multiplexer (U164) to provide bit 7 of the diagnostic status word when the select line is active.
A16 (J1-31)	B9 (J1-18)	Connects data out bits 6 or 14 (series 600/ 700) to the input of the diagnostic multiplexer (U164) to provide bit 7 of the diagnostic status word when the select line is inactive.
A18 (J1-35)	B15 (J1-30)	Connects data out bits 5 or 13 (series 600/ 700) to the input of the diagnostic multiplexer (U164) to provide bit 6 of the diagnostic status word when the select line is inactive.
A21 (J1-41)	B14 (J1-28)	Connects the +X plot command (series 500) to the input of the diagnostic multiplexer (U164) to provide bit 6 of the diagnostic status word when the select line is active.
B10 (J1-20)	B21 (J1-42)	Connects the -Y plot command (series 500) to the input of the diagnostic multiplexer (U164) to provide bit 8 of the diagnostic status word when the select line is active.

471004-272/273, 2 of 2

<table>
<tr><th rowspan="2">FUNCTION</th><th colspan="10">DATA OUT BITS ISSUED*</th><th colspan="6">STATUS WORD BITS</th></tr>
<tr><th>3</th><th>11</th><th>4</th><th>12</th><th>5</th><th>13</th><th>6</th><th>14</th><th>7</th><th>15</th><th>3</th><th>4</th><th>5</th><th>6</th><th>7</th><th>8</th></tr>
<tr><td>+Y</td><td colspan="2">0</td><td colspan="2">0</td><td colspan="2">0</td><td colspan="2">0</td><td colspan="2">0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>+Y,+X</td><td colspan="2">0</td><td colspan="2">0</td><td colspan="2">0</td><td colspan="2">0</td><td colspan="2">1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>+X</td><td colspan="2">0</td><td colspan="2">0</td><td colspan="2">0</td><td colspan="2">1</td><td colspan="2">0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>−Y,+X</td><td colspan="2">0</td><td colspan="2">0</td><td colspan="2">0</td><td colspan="2">1</td><td colspan="2">1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>−Y</td><td colspan="2">0</td><td colspan="2">0</td><td colspan="2">1</td><td colspan="2">0</td><td colspan="2">0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>−Y,−X</td><td colspan="2">0</td><td colspan="2">0</td><td colspan="2">1</td><td colspan="2">0</td><td colspan="2">1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>−X</td><td colspan="2">0</td><td colspan="2">0</td><td colspan="2">1</td><td colspan="2">1</td><td colspan="2">0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>+Y,−X</td><td colspan="2">0</td><td colspan="2">0</td><td colspan="2">1</td><td colspan="2">1</td><td colspan="2">1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>Not Used</td><td colspan="2">0</td><td colspan="2">1</td><td colspan="2">0</td><td colspan="2">0</td><td colspan="2">0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Pen Up</td><td colspan="2">0</td><td colspan="2">1</td><td colspan="2">0</td><td colspan="2">0</td><td colspan="2">1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Pen Down</td><td colspan="2">0</td><td colspan="2">1</td><td colspan="2">0</td><td colspan="2">1</td><td colspan="2">0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td colspan="17">*Left Byte = Data Out Bits 3 thru 7
Right Byte = Data Out Bits 11 thru 15</td></tr>
</table>

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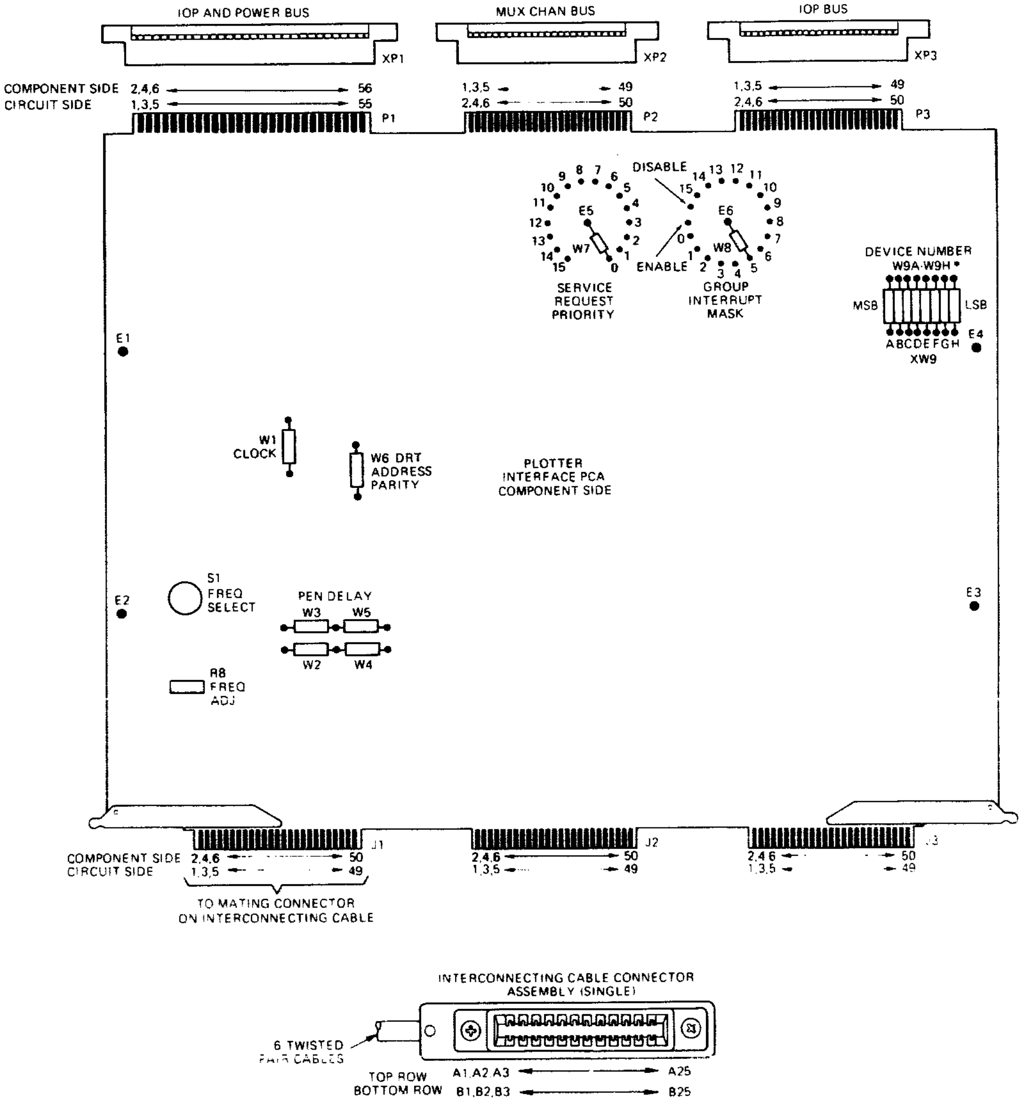
SERIES 500 INPUT/OUTPUT PLOT COMMAND DATA



* W9A HAS NO SIGNIFICANCE. USE W9B AS MOST SIGNIFICANT BIT WHEN SELECTING DEVICE NUMBER.

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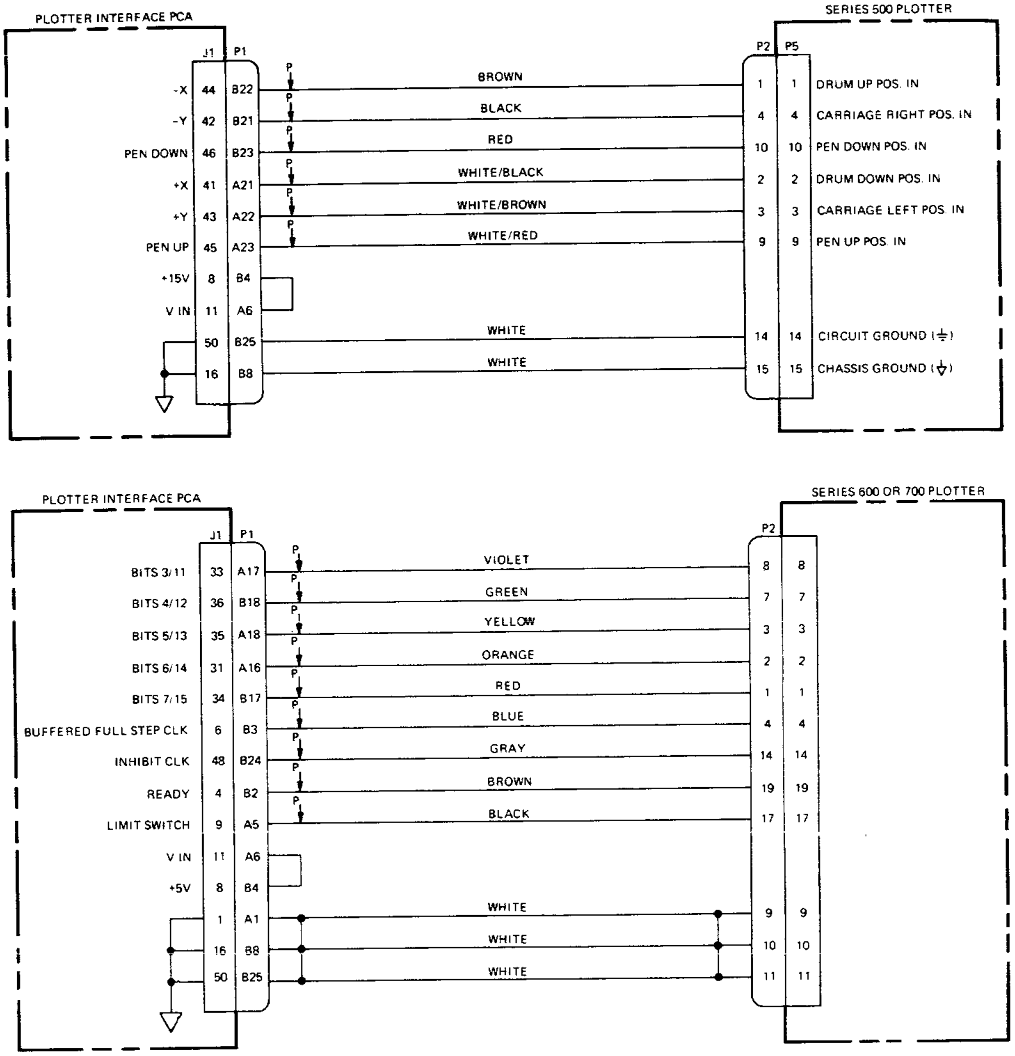
CONNECTOR PIN NUMBERING AND JUMPER WIRE LOCATION



NOTES 1 "P" INDICATES A TWISTED PAIR

2 SERIES 500 PLOTTER

P1 a. WHITE WIRES OF TWISTED PAIRS P1 B21, P1 B22, AND P1 B23 ARE TERMINATED AT P1 B25

b WHITE WIRES OF TWISTED PAIRS P1 A21, P1 A22, AND P1 A23 ARE TERMINATED AT P1 B8

P2 a. WHITE WIRES OF TWISTED PAIRS P2 1, P2 4, AND P2 10 ARE TERMINATED AT P2 14.

b WHITE WIRES OF TWISTED PAIRS P2 2, P2 3, AND P2 9 ARE TERMINATED AT P2 15.

3. SERIES 600 OR 700 PLOTTER

P1 a WHITE WIRES OF TWISTED PAIRS P1 A17, P1 A18, AND P1 A16 ARE TERMINATED AT P1 B8

b WHITE WIRES OF TWISTED PAIRS P1 B18, P1 B17, AND P1 B24 ARE TERMINATED AT P1 B25

c WHITE WIRES OF TWISTED PAIRS P1 B3, P1 B2, AND P1 A5 ARE TERMINATED AT P1 A1

P2 a WHITE WIRES OF TWISTED PAIRS P2 8, P2 14, AND P2 17 ARE TERMINATED AT P2 10.

b WHITE WIRES OF TWISTED PAIRS P2 3, P2 7, AND P2 19 ARE TERMINATED AT P2 11

c WHITE WIRES OF TWISTED PAIRS P2 1, P2 2, AND P2-4 ARE TERMINATED AT P2-9.

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PLOTTER INTERCONNECTIONS

CALCOMP PLOTTER ONLINE
3026A

```
*NEW CALCOMP        ((WHATEVER))
PROGRAM FILE?       PD376A.XXXXXX.XXXXXX
DEVICE?     XX     ((DECIMAL # OF DRT #))
SET FLAGS?     X,X     ((WHATEVER))
D327 CONFIGURATION SECTION COMPLETED
*SAVE CALCOMP       ((SAVES IT INTO THE PST))
*ON AND RUN OR RUN CALCOMP
```

FLAGS:

1 INTERFACE SELFTEST ((USING TEST HOOD))
2 DEVICE AND SUBSYSTEM TEST

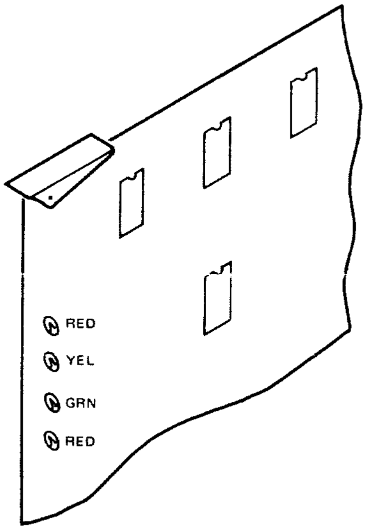
1471004-277

30129A/7905/7920
DISC MEMORY
SUBSYSTEMS

7905 (1629 D.C.)

FAULT	LED COLOR
CB	Yellow
T	Red
AGC	Yellow, Red
IL	Green
$W \cdot \overline{AR}$	Yellow, Green
$R \cdot W$	Green, Red
$W \cdot \overline{AC}$	Yellow, Green, Red
MH	Red, Red
$DC \cdot \overline{W}$	Red, Red, Yellow

LED's mounted on the side of the Control PCA (07905-60002) can be viewed from the front (thru the glass)



1471004-285

DISC CONTROLLER FAULT INDICATORS

```
       STATUS WORD    (TIO,SENSE,END)
|---|-----------|-----------|-----------|-----------|-----------|
| 0|  1   2   3|  4   5   6|  7   8   9| 10  11  12| 13  14  15|
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
|<------------ S1 ------------->|              |<----- U ----->|
```

where:
U = Unit Number, in the range 0 thru 12 (octal)
S1 = Status bits, as follows:

bit 0 - SIO READY
bit 1 - TEST MODE
bit 2 - INTERRUPT REQUEST
bits 3 through 7 - ENCODED TERMINATION STATUS (octal, as defined within the following list:)

(The values listed are octal; the two digit values are read only from bits 3 through 7, and the others are read from the complete status word:)

```
00 (0000U) = Normal completion
01 (0004U) = Illegal opcode <%26
02 (0010U) = Set wakeup
07 (0034U) = Cylinder compare error      )
10 (0040U) = Uncorrectable data error    > Track specific
11 (0044U) = Head-sector compare errror  )  errors
12 (0050U) = I/O program error
14 (0060U) = End of cylinder
16 (0070U) = Overrun (transfer error)
17 (0074U) = Possibly correctable data error
20 (0100U) = Illegal access to spare track
21 (0104U) = Defective track
22 (0110U) = Access not ready during data operation (heads
              still moving)
23 (0114U) = Status - 2 error
26 (0130U) = Write attempt to protected or defective track
27 (0134U) = Unit unavailable
37 (0174U) = Drive attention (seek complete)
```

All other bits of this STATUS WORD are unused.

471004-278, 1 of 2

STATUS WORDS, sheet 1 of 3

```
          STATUS-1 WORD    (Regular status)
|---|-----------|-----------|-----------|-----------|-----------|
|  0|  1   2   3|  4   5   6|  7   8   9| 10  11  12| 13  14  15|
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
            |<------ S1 ------->|               |<----- U ----->|
```

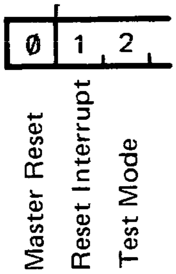
where:
  bit 0 - Flag spare track
  bit 1 - Flag protected track
  bit 2 - Flag defective track
  U = (Same as defined for STATUS WORD)
  S1 = (Same as defined for STATUS WORD)

All other bits of this STATUS-1 WORD are unused.

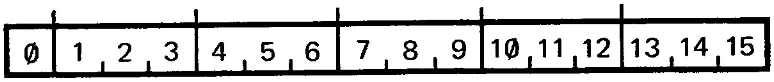
471004-278, 2 of 2

STATUS WORDS, sheet 2 of 3

CONTROL WORD (CIO)

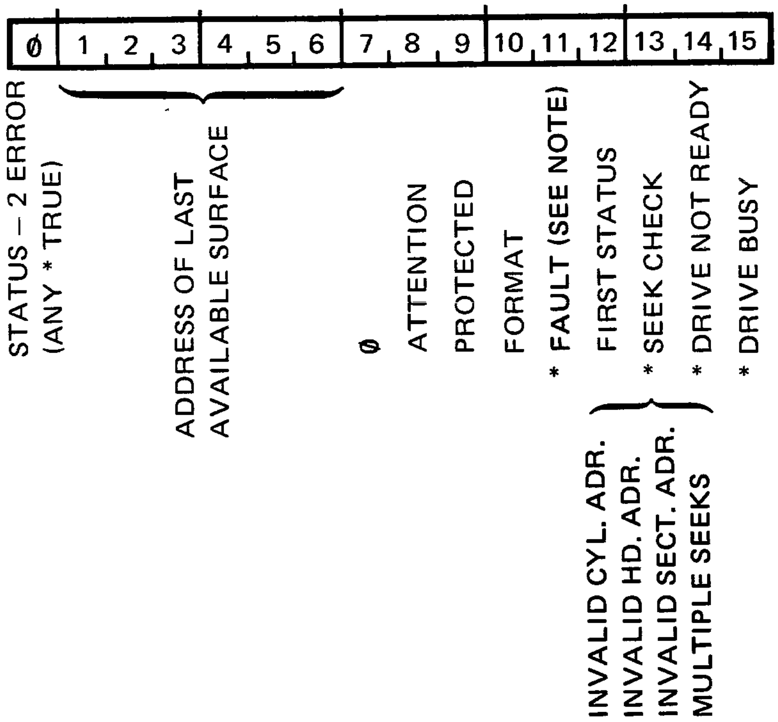


(WIO)



Diagnostic Uses WIO to load/check Data Buffer Reg.
Note: Data Buffer Reg. is used for Data or Status.

STATUS – 2 WORD (REQUEST STATUS)
(STATUS – 1 WORD IS SAME AS STATUS WORD BITS 3–15)



NOTE: SEE FAULT LAMP DEFINITION TABLE

1471004-279

STATUS WORDS, sheet 3 of 3

HP 7905/7920 DRIVE FAULT LAMPS

IL	(Interlock)-caused by DC power failure, voltage out of tolerance, improper PCA seating, DMR PCA heat sink too hot, pack chamber not connected, or spindle fault.
T	(Timeout)-exceeded forward or reverse seek, initial head load, normal head unload, or recalibrate maximum time limit.
AGC	(Automatic Gain Control)-agc signal lost while heads were over servo surface.
CB	(Carriage back)-successful head load, but carriage back detected or showed heads still back.
*R/W	(Read/Write)-Simultaneous read and write operations.
MH	(Multihead)-more than one head selected.
*DC.NW	(DC Write current. not write)-heads receiving write current but drive not in write mode.
W.NAC	(Write. not AC Current)-drive in write mode but no data being written on disc.
*W.NAR	(Write. not Access Ready)-heads not positioned over valid cylinder and drive in write mode.

* Implies non destructive fault. All others will retract the heads.

(SIO)

	0							7			10					15	
000	0	0	0	0	0	0	0	0	H	D	S	E	C	T	O	R	COLD LOAD READ
	0							7		9						15	
001	0	0	0	0	0	0	0	1	H	U	N	I	T		N	O.	RECALIBRATE *
002	0	0	0	0	0	0	1	0	H	U	N	I	T		N	O.	SEEK*
003	0	0	0	0	0	0	1	1	▨	U	N	I	T		N	O.	REQUEST STATUS
004	0	0	0	0	0	1	0	0	▨	U	N	I	T		N	O.	REQUEST SECTOR ADDRESSES
005	0	0	0	0	0	1	0	1	▨	U	N	I	T		N	O.	READ
006	0	0	0	0	0	1	1	0	H	U	N	I	T		N	O.	READ FULL SECTOR
007	0	0	0	0	0	1	1	1	H	U	N	I	T		N	O.	VERIFY
010	0	0	0	0	1	0	0	0	H	U	N	I	T		N	O.	WRITE
011	0	0	0	0	1	0	0	1	H	U	N	I	T		N	O.	WRITE FULL SECTOR
	0							7									
012	0	0	0	0	1	0	1	0	▨	▨	▨	▨	▨	▨	▨	▨	CLEAR
	0	1	2	3				7		9						15	
013	S	P	D	0	1	0	1	1	H	U	N	I	T		N	O.	INITIALIZE
	0							7									
014	0	0	0	0	1	1	0	0	▨	▨	▨	▨	▨	▨	▨	▨	ADDRESS RECORD

*13037A Will Disconnect After Execution.

1471004-280

COMMAND DESCRIPTIONS, sheet 1 of 2

(SIO)

	0							7	8	9–15	
015	0	0	0	0	1	1	0	1			REQUEST SYNDROME
016	0	0	0	0	1	1	1	0	H	UNIT NO.	READ WITH OFFSET
017	0	0	0	0	1	1	1	1	RETRY COUNT	12 I/D, 13 S, 14 S/C, 15 AS	SET FILE MASK
020	0	0	0	1	0	0	0	0		UNIT NO.	CLEAR UNIT BUSY
021	0	0	0	1	0	0	0	1		UNIT NO.	REQUEST UNIT ALLOCATION
022	0	0	0	1	0	0	1	0	H	UNIT NO.	READ WITHOUT VERIFY
023	0	0	0	1	0	0	1	1			LOAD TIO REGISTER
024	0	0	0	1	0	1	0	0			REQUEST DISC ADDRESS
025	0	0	0	1	0	1	0	1			POLL DISCONNECT*
026	0	0	0	1	0	1	1	0		UNIT NO.	WAKEUP

*13037A Will Disconnect After Execution.

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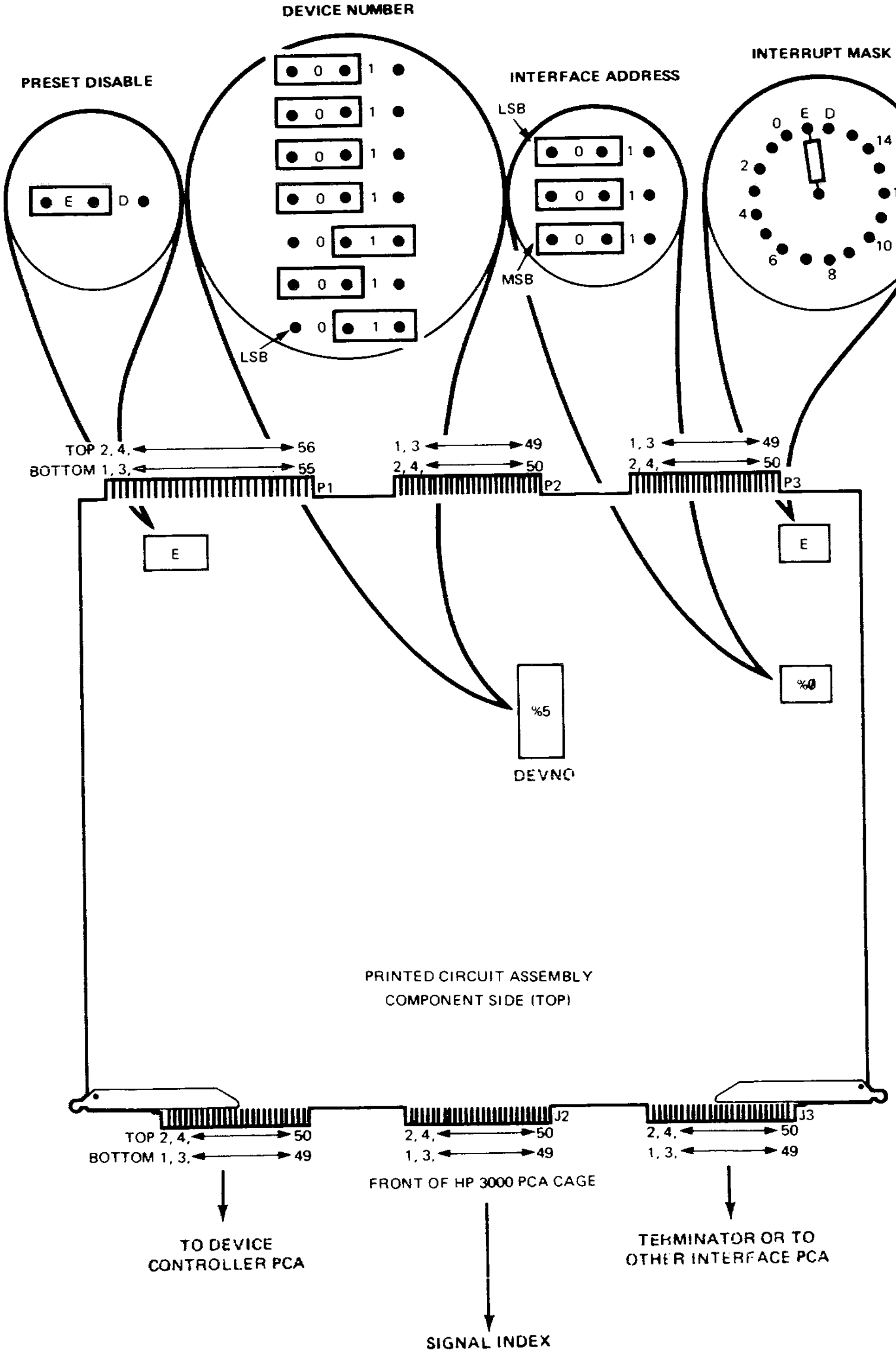
COMMAND DESCRIPTIONS , sheet 2 of 2



1471004-282

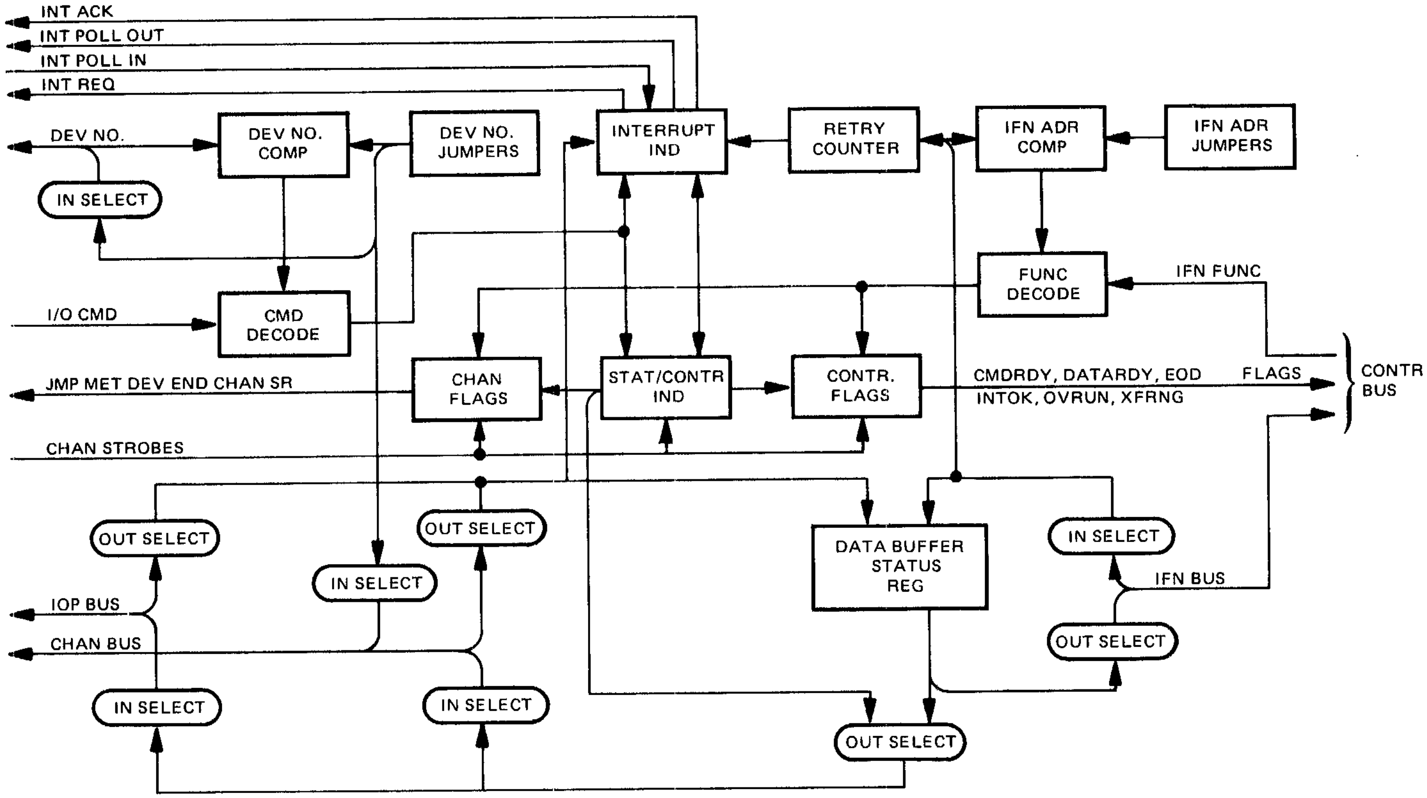
INTERFACE BOARD JUMPERS

DSC0520-9

HP 30229A INTERFACE J2 SIGNAL INDEX

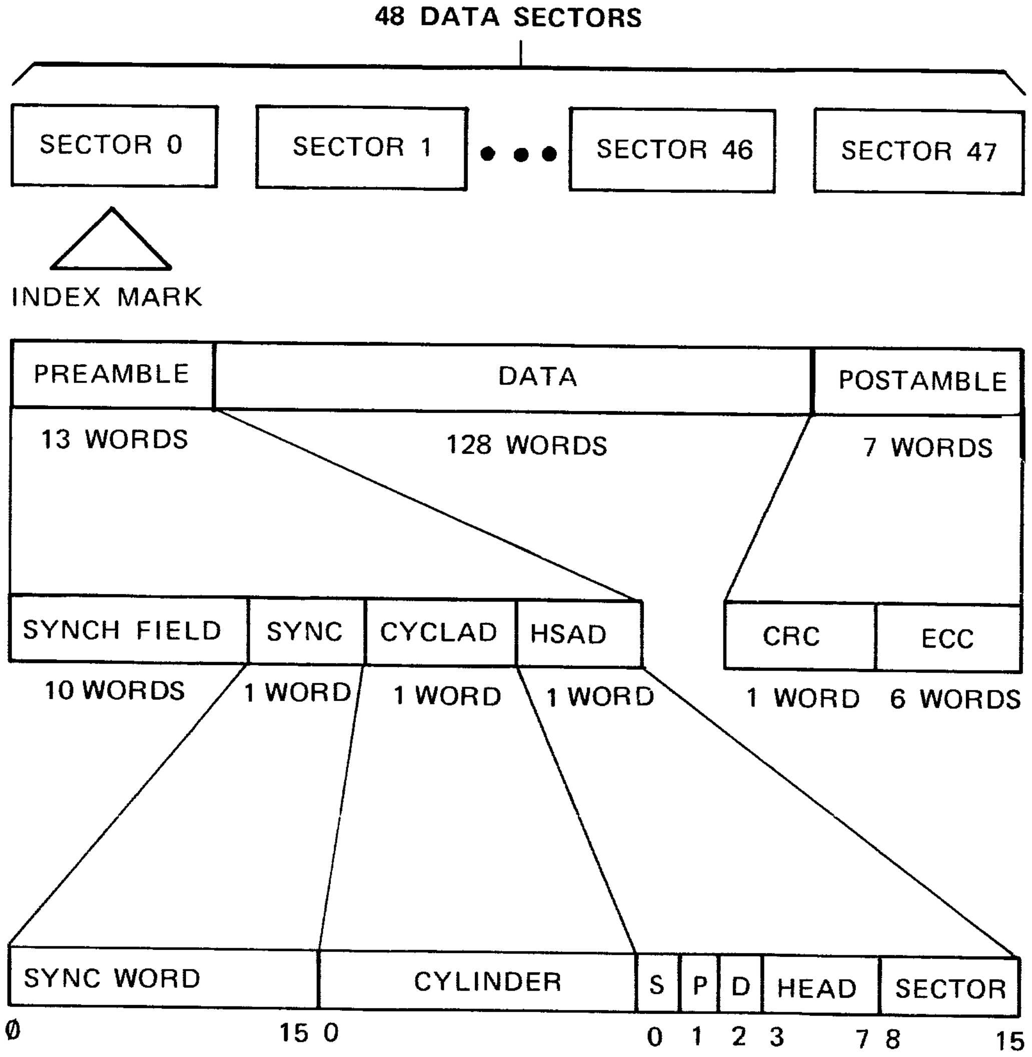
TEST REG. DISPLAY (J3)

BIT NO.	DESCRIPTION	SOURCE (J2)
0	SER REQ (1) CHAN	11
1	SER REQ (2) CONTR	7
2	*EOD (3) CONTR	23
3	JUMP MET CONTR	25
4	OUTXFER CHAN	27
5	INXFER CHAN	29
6	*WAIT CHAN	31
7	DEV END CONTR	9
8	INVALID CONTR	35
9	*CMD RDY CHAN	13
10	*DATA OVRN IFACE	15
11	*DATA RDY CHAN	41
12	IFACE SEL CONTR	43
13	SIO BUSY SIO	45
14	XFER ERR CHAN	42
15	CHAN SO CHAN	48
	SIO OK SIO	4
	EOD (1) CHAN	21
	EOD (2) CHAN	17
	INT MASK IOP	37
	INT ACTIVE	39
	NSEEK CHAN	40
	SO IOP	44
	INT REQ CONTR/CHAN	46
	TEST MODE IOP	47
	+5V (RESISTOR)	2
	GND	5,19,33,49



1471004-283

CARTRIDGE DISC INTERFACE BLOCK DIAGRAM



PREAMBLE – 15 Words for synchronization and addressing
DATA – 128 Words of data
POSTAMBLE – Data checking and error correction information
SYNC FIELD – 12 Words (192 bits) of 0's
SYNC - SYNC WORD – 100376_8 If ECC field is valid
– 100377_8 Otherwise
CYLAD – Cylinder address
HSAD – Head address (logical)
– Sector address (logical)
– S - If "1", spare track in active use
– P - If "1", protected track
– D - If "1", defective track

CRC – CYCLIC REDUNDANCY CHECK – 1 Word of check information
ECC – ERROR CORRECTION CODE – 6 Words of check and correction information

1471004-284

TRACK AND SECTOR RECORDING FORMAT

DIAGNOSTIC STAND ALONE

CARTRIDGE DISC (7905A)

1. Cold Load Diagnostic File Number from Non-CPU Cold Load Tape.
2.

Switch Register Options:

BIT 0 - Select External Register
1 - Select Section Register Options
2 -
3 -
4 -
5 -
6 -
7 -
8 -
9 -
10 -
11 -
12 - Pause at End of Program
13 - Loop on current Step
14 - Pause on Error
15 - Pause at End of Step

Section Register Options:

BIT 0 - Initialization
1 - Basic Function
2 - Write/Read to limited addresses
3 - Random Write/Read
4 - Random Read Unique Data
5 - Multi-Unit Test
6 - Interface Test in Test Mode
7 - Change Unit Table
8 - Change Cylinder Table
9 - Change Head Table
10 - Change Pattern Data Table
11 - Loop on current section
12 - Interactive Section 1 (Disc Format)
13 - List all D-Class Messages
14 - Shorten test about 70%
15 - Restrict cylinders

SLEUTH COMMANDS

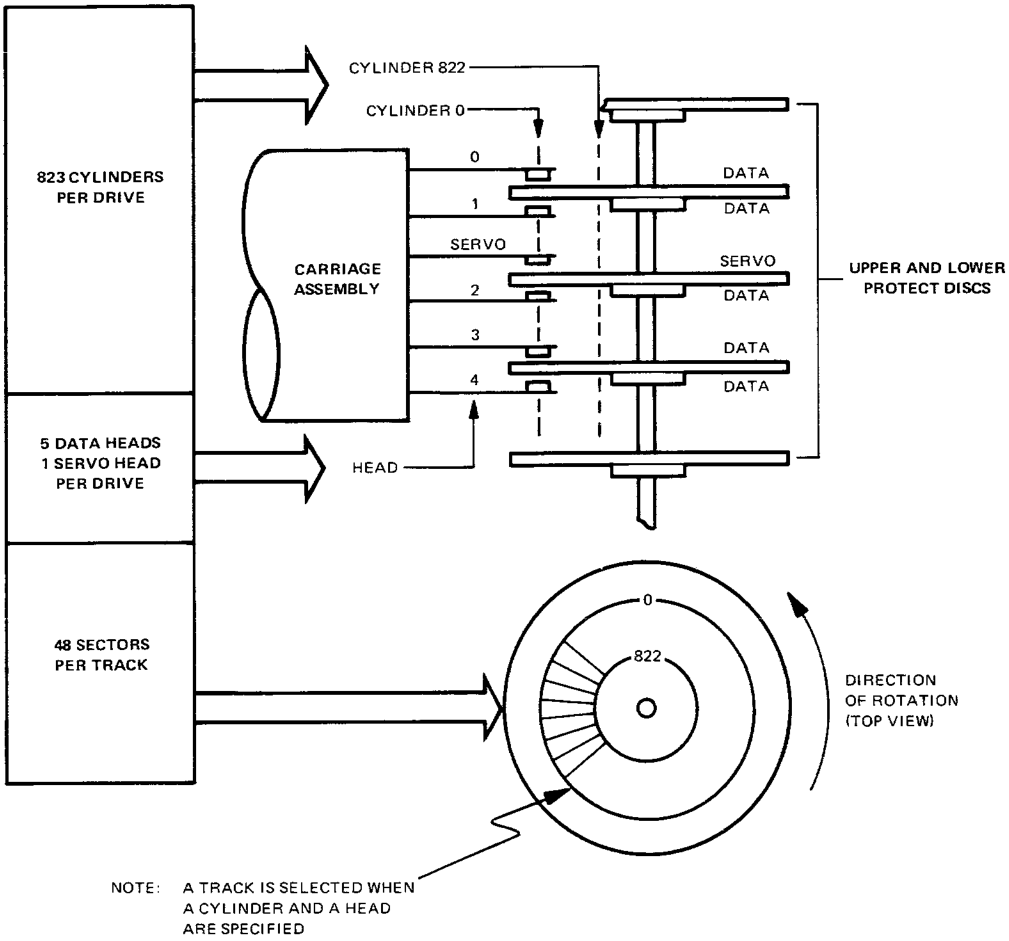
FORMAT COMMAND GENERATES THE FOLLOWING SIO DOUBLE WORD COMMANDS FOR THE 7905/7920
FMT [LUN]

```
SFM (2)                 << CYLINDER MODE >>
WRT (2WORDS)            << CYL, HD, SECTOR >>
INIT (UNIT)
WRT (4K WORDS);WRT (4K WORDS)   - DATA CHAINED
WRT (4K WORDS);WRT (4K WORDS)   - DATA CHAINED
WRT (2K WORDS)
ADR.REC (UNIT)
WRT (2WORDS)            << CYL, HD, SECTOR >>
VER (UNIT)
WRT (1 WORD)            << SECT COUNT >>
JMP (C)
END (0)
```

THIS SIO PROGRAM INITIALIZES THE ENTIRE CYLINDER THEN VERIFIES THE ENTIRE CYLINDER.

THE FOLLOWING COMMANDS APPLY TO BOTH THE 7905 AND 7920 DISCS.

RQST[LUN] DISD[LUN],R	DISPLAYS STATUS -1 AND STATUS -2 WORDS
RSA[LUN] DISP[LUN],S	DISPLAYS THE LOGICAL SECTOR ADDRESS CURRENTLY UNDER THE HEADS.
RSYN[LUN] DISP[LUN],Y	DISPLAYS 7 WORDS OF ERROR CORRECTION.
RDA[LUN] DISP[LUN],D	DISPLAYS 2 WORDS CONTAINING THE CURRENT CYLINDER CYLINDER, HEAD, AND SECTOR.
RUA[LUN] DISP[LUN],u	DISPLAYS 1 WORD OF UNIT STAUS.



1471004-287

ADDRESSING STRUCTURE OF A HP 7920 DISC DRIVE

DEFECTIVE TRACKS ON 7920 DISC PACKS

Effective immediately DMD division will begin to include a list of all marginal tracks on 7920A disc packs. This list is a result of their testing the pack in a special ET that utilizes weak heads and offset seeking. These tracks will also be flagged.

To guarantee pack interchange these tracks must remain flagged. When a pack is installed in a given drive the majority of the flagged tracks will not be detected by the verifier if the pack has been formatted. This is to be expected since the normal drive has much better heads than the ET. If the pack is formatted it is imperative that the tracks on the list be reflagged. These flagged tracks must be deleted or resigned when bringing up MPE.

<< IMPORTANT >>

> A record of previous defective tracks on all disc drives should be kept in order to avoid having a repeat of the same failures. These known bad tracks must be DELETED or REASSIGNED during every RELOAD operation.
>
> If a record was not kept, then the stand-alone disc edit program should be run in an effort to dump the Defective Track Table (sector 1 for 1 on each disc) to the line printer or console. See part II of the MPE Analysis section for more detailed operating instructions.

Spindle Logic PCA

GRN	Speed Up (SPU) lights when the spindle motor is at normal speed.
YEL	OFF lights when power to the spindle motor is removed.
RED	Spindle Fault (SPFLT) lights when an overcurrent is sensed. This fault also forces an interlock fault and retracts the heads.

SLEUTH FORMAT PROGAMS FOR 7920 DISC

```
10 DEV 0,DEVNO,15,99,unit
10 DB AA,6144,0
10 FOR A=0 TO 822                   << CYL >>
20 FOR B=0 TO 4                     << HD >>
30 SEEK 0,A,B,0
40 IDI 0,AA,2                       << CYL MODE >>
50 VER 0,48,A,B,0
60 NEXT B
70 NEXT A
80 END
```

CANNED VERIFIER PROGRAM (VERI7920)

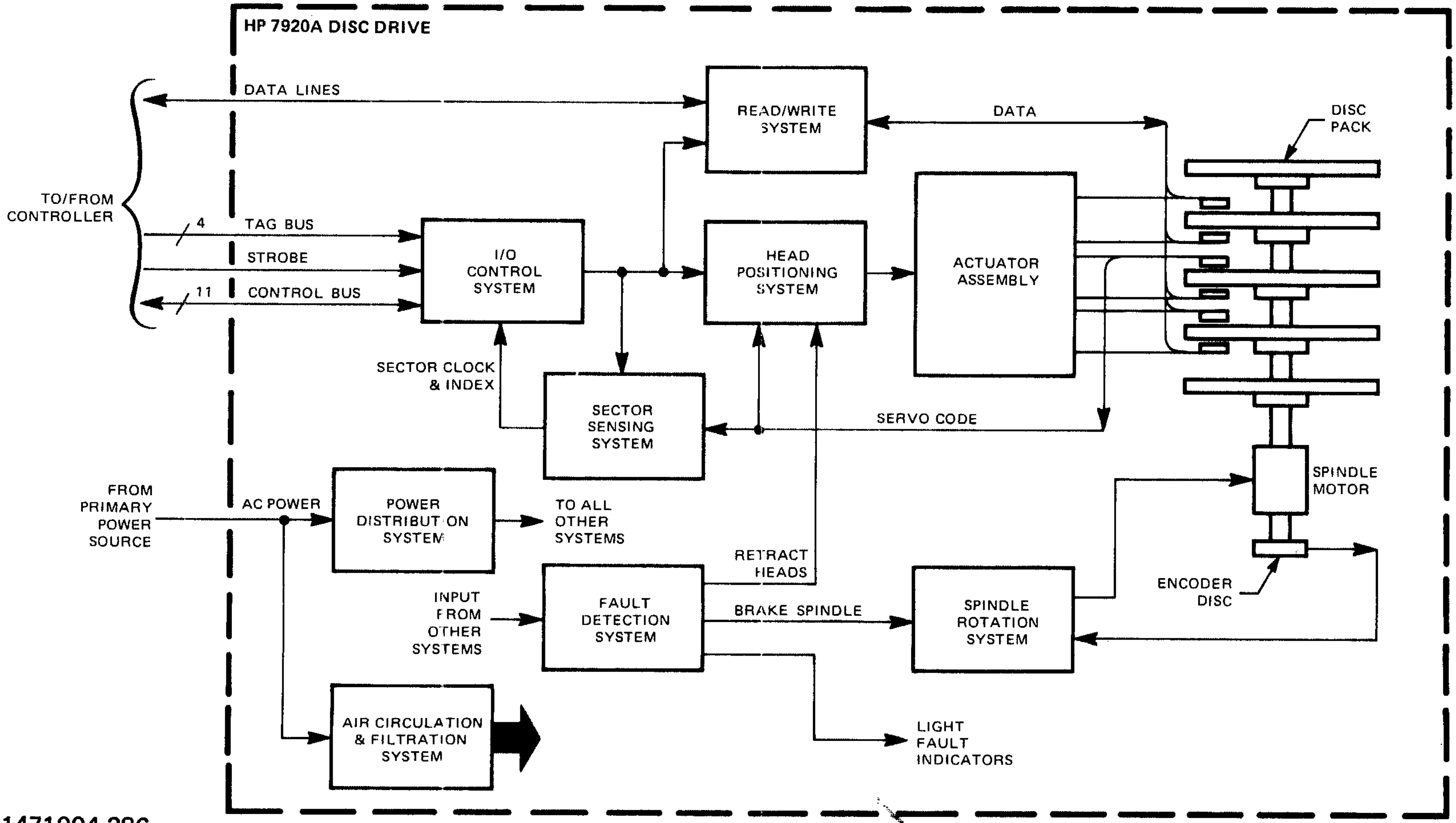
```
10 BA 1             << IF TAKEN FROM MAKT >>
|
|
|
670 10 LET W=0 SKIP TEST
           =1 TEST UNIT SELECT SWITCH

    11 LET X=0 SKIP TEST
           =1 FORMAT PACKK

    12 LET Y=0 SKIP TEST
           =1 CERTIFY PACK

    IF Y=1 THEN
    13 LET Z=0 RUN SHORT PASS (8 minutes per pass)
           =1 RUN LONG PASS (25 minutes per pass)
    ELSE Z=DON´T CARE
    14 AUTO

10 BA E           << IF TAKEN FROM EDITOR FILE >>
10 LET W=0
       =1
|
|
|
10 AUTO
670
```



1471004-286

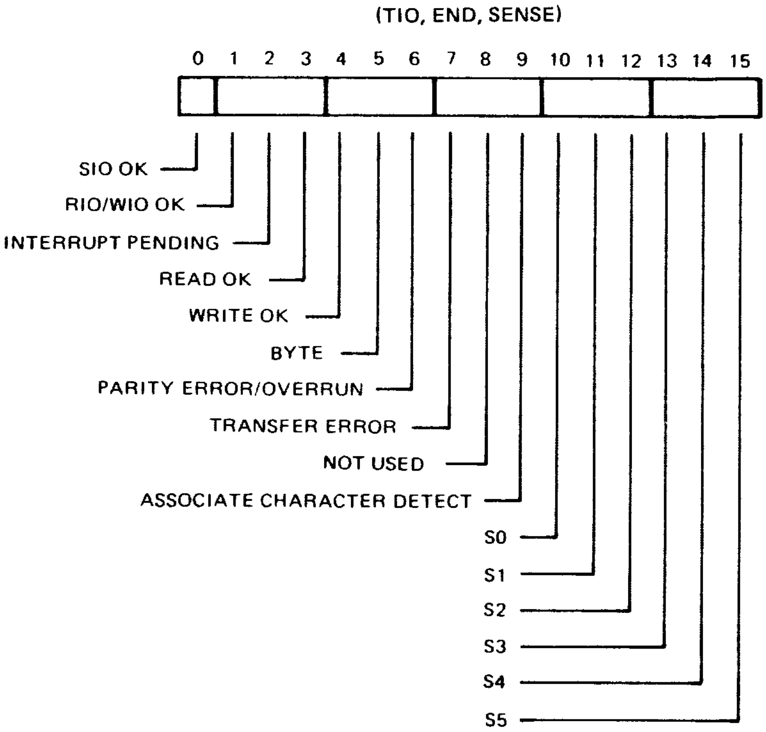
7920 SIMPLIFIED BLOCK DIAGRAM

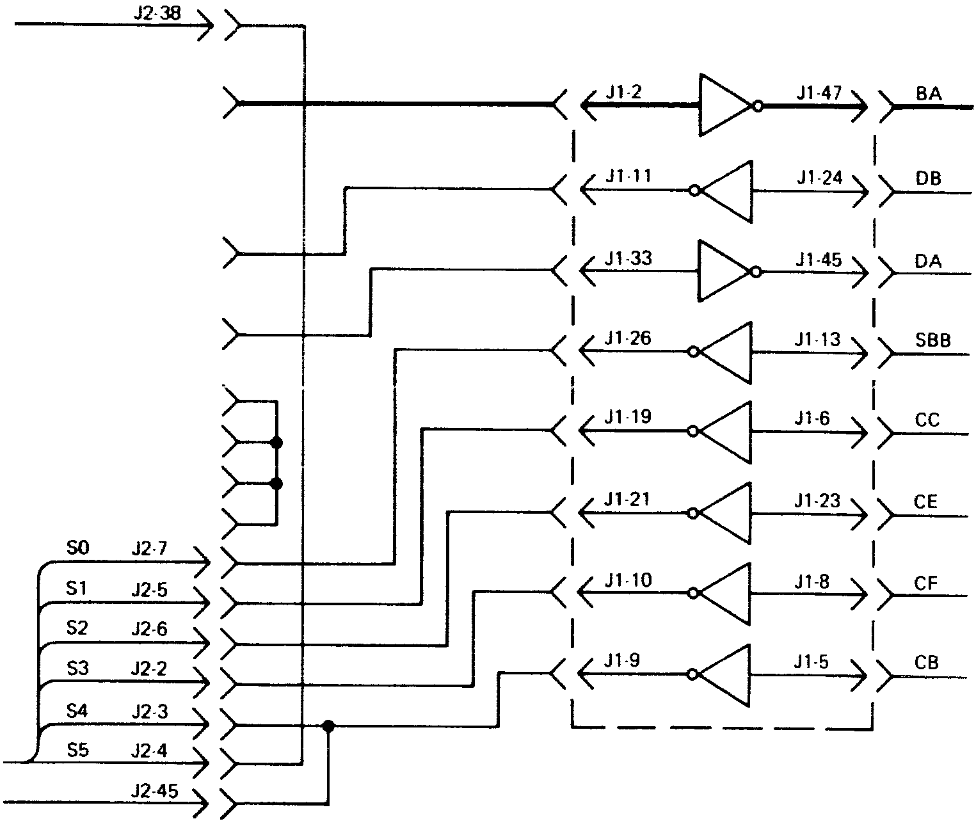
SYNCHRONOUS SINGLE LINE CONTROLLER

SYNCHRONOUS SINGLE LINE CONTROLLER PCA
30130A/30055A

DIFFERENCES FROM SERIES II

None.





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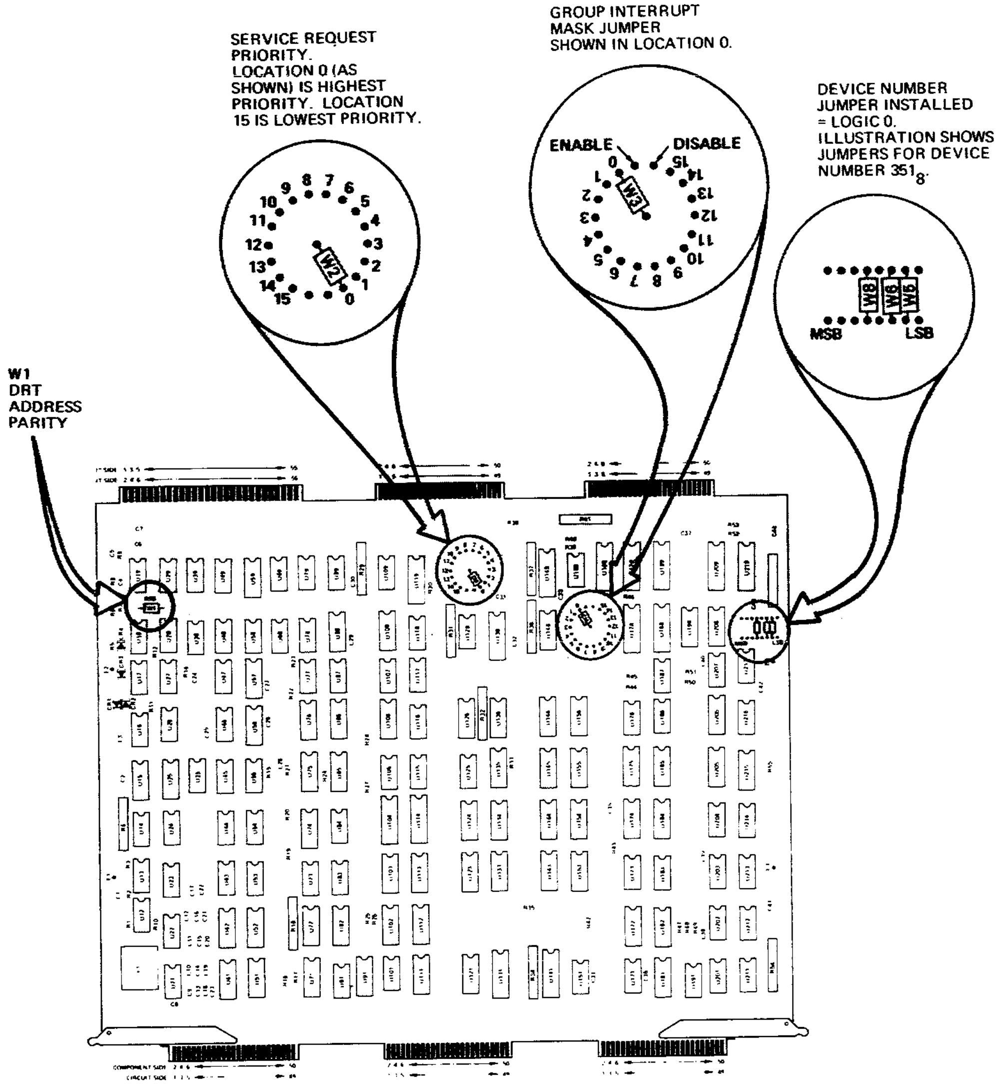
STATUS FORMAT

SSLC-2



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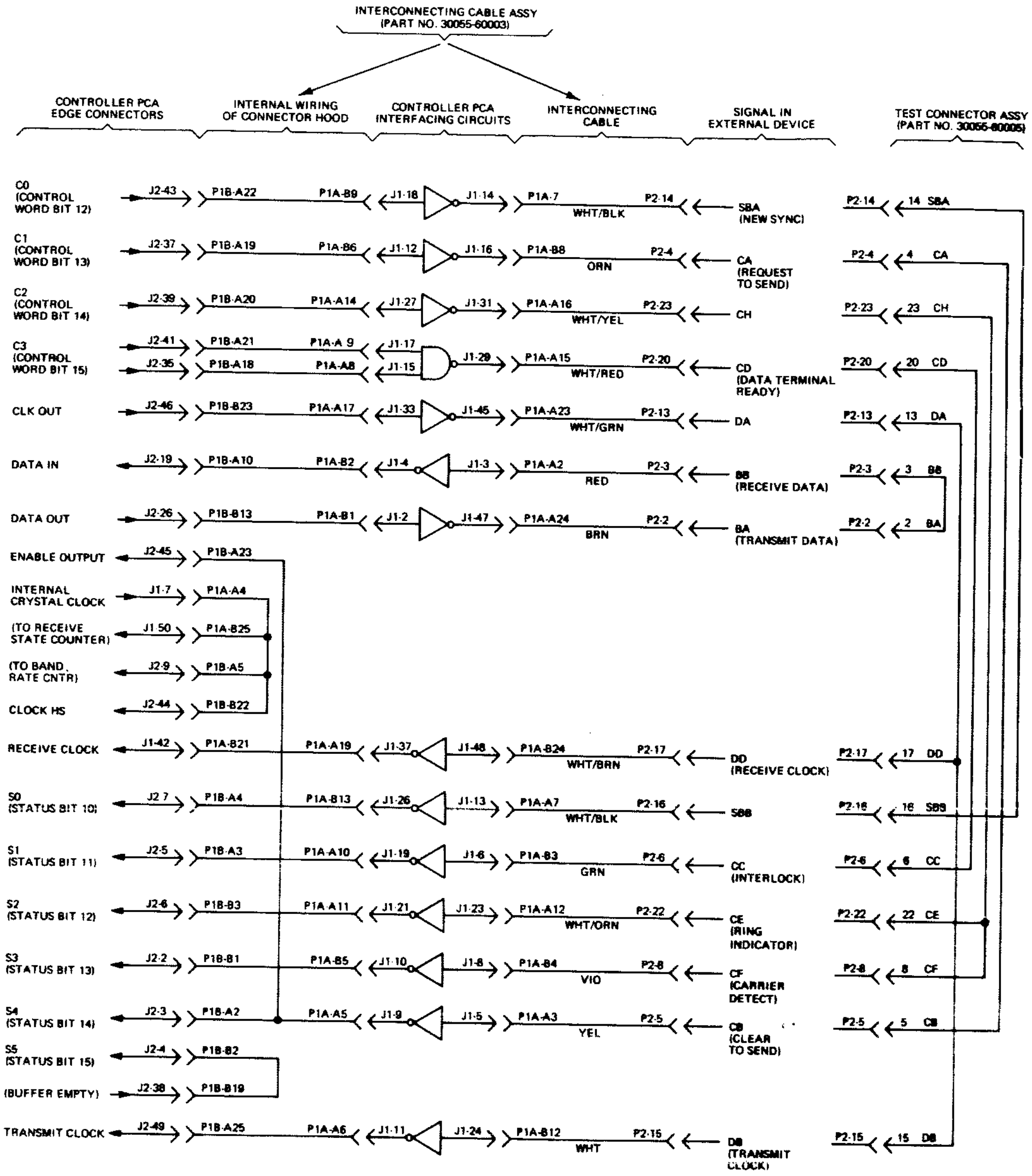
JUMPER LOCATIONS



1471004-290

CABLE AND TEST CONNECTOR WIRING DIAGRAM

SYNCHRONOUS SINGLE LINE CONTROLLER S-A

30055A

1. COLD LOAD DIAGNOSTIC FILE # FROM NON-CPU COLD LOAD TAPE D25 30055A SYNCHRONOUS SINGLE LINE CONTROLLER TEST (HP32334.00.0) (INSTALL TURN-AROUND CONNECTOR 30055-60005)
2. Q26 DEVICE # ? XX ((OCTAL DRT #))
3. P27 SELECT OPTIONS? ((SET SW REG THEN RUN))

SWITCH REGISTER OPTIONS

SWITCH	FUNCTION IF SET
0	USE AND STORE EXTERNAL SWITCH REGISTER
1	EXECUTE SECTION 1 (I/O COMMANDS)
2	EXECUTE SECTION 2 (STATUS/CONTROL)
3	EXECUTE SECTION 3 (SIO READ/WRITE DIRECT)
4	EXECUTE SECTION 4 (PARITY)
5	EXECUTE SECTION 5 (PACK/UNPACK)
6	EXECUTE SECTION 6
7	EXECUTE SECTION 7
8	EXECUTE SECTION 8
9	USE LINE PRINTER FOR A AND E TYPE MESSAGES
10	SUPPRESS D-TYPE MESSAGES
11	SUPPRESS E-TYPE MESSAGES
12	HALT AFTER PRINTING END-OF-PASS MESSAGE
13	LOOP ON CURRENT STEP OR SET OF LOGICAL STEPS
14	HALT AFTER PRINTING ERROR MESSAGES
15	HALT AT END OF EACH STEP AND PRINT STEP NUMBER

1471004-291

SSLC STAND-ALONE DIAGNOSTIC

PROGRAMMABLE CONTROLLER
30300/30301

DIFFERENCES FROM SERIES II

None.

JUMPER INFORMATION - See Universal Interface

2	3	4	
0	0	0	NO RESET
0	0	1	WATCHDOG TIMER & TRANSFER ERROR
0	1	0	I/O SYSTEM
0	1	1	CLEAR INTERFACE
1	0	0	DATA TRANSFER COMPLETION
1	0	1	LINE READY (H DEV CMD)
1	1	0	READY (INTERRUPT)
1	1	1	NOT READY (N/A)

SEQUENCE FLIP FLOPS

3	4	
0	0	NO TRANSFER IN PROGRESS
1	0	DEV CMD. ISSUED
1	1	DEV FLAG RECEIVED
0	1	ISSUE 2ND DEV CMD (BYTE XFER ONLY)

471004-292

	SWITCH 1	SWITCH 2	SWITCH 3
U85	2	5	0
U87	2	4	8
U97	1	5	9
U102	2	6	0
U106	1	5	9

471004-293

UNIV. INTF. BOARD SWITCH SETTINGS

HP 3000

PROG. CONTR. CONTROL WD. (CIO. CONTROL)

```
|---|-----------|-----------|-----------|-----------|-----------|
|  0|  1|  2|  3|  4|  5|  6|  7|  8|  9| 10| 11| 12| 13| 14| 15|
|---|-----------|-----------|-----------|-----------|-----------|
 Field/bit Definitions:

        |<--- A --->|   |<------- B ------->|
```

where:

bit 0 = MASTER CLEAR

bit 1 = RESET INTERRUPTS

Field A = INTERRUPT RESET SELECTION (bits 2-4)

bit 5 = INITIATE TRANSFER

Field B = DEV. CONTR.

```
    bit 6  = (H DEV FLAG)
    bit 7  = ERROR
    bit 8  = (EOF)    )
    bit 9  = (WRITE)  > USER CONTROLLED
    bit 10 = (READ)   )
```

bit 11 = ENABLE DATA TRANSFER INTERRUPT

bit 12 = INTERRUPT/DEVICE STAT.

bit 13 = WORD/BYTE TRANSFER

bit 14 = ENABLE INTERRUPTS

bit 15 = ENABLE WATCHDOG TIMER

471004-294, sheet 1 of 2

12930A U.I. CARD

HP 2100

PROG. CONTR. CONTROL WD. (OTA/B CMD CHAN)

```
|---|-----------|-----------|-----------|-----------|-----------|
| 15| 14| 13| 12| 11| 10|  9|  8|  7|  6|  5|  4|  3|  2|  1|  0|
|---|-----------|-----------|-----------|-----------|-----------|
  Field/bit Definitions:

                 |<----A---->|
```

where:

Field A = USER CONTROLLED:

    bit 10 = (READ)
    bit 11 = (WRITE)
    bit 12 = (EOF)

bit 13 = ERROR

bit 14 = INTERRUPT

bit 15 = STOP SIO (DEV END)

471004-294, sheet 2 of 2

CONTROL WORDS

HP 3000

PROG. CONTR. STATUS WD. (TIO, SENSE, END)

```
|---|-----------|-----------|-----------|-----------|-----------|
| 0|  1|  2|  3|  4|  5|  6|  7|  8|  9| 10| 11| 12| 13| 14| 15|
|---|-----------|-----------|-----------|-----------|-----------|
 Field/bit Definitions:

        |<- A ->|
```

where:

Field A = SEQUENCE F/F (bits 2 and 3)

bit 0 = SIO READY

bit 1 = RIO - WIO READY

bit 2 = INTERRUPT REQUEST

bit 5 = DEVICE FLAG (L DEV CMD)

bit 6 = INTERRUPT/DEVICE STATUS

bit 8 = (H DEV CMD)

bit 9 = INTERRUPT

bit 12 = ERROR

```
bit 13 = (EOF)    )
                  |
bit 14 = (WRITE)  >  USER CONTROLLED
                  |
bit 15 = (READ)   )
```

471004-295, 1 of 2

12930A U.I. CARD

HP 2100

PROG. CONTR. STATUS WD. (LIA/B CMD CHAN)

```
|---|-----------|-----------|-----------|-----------|-----------|
| 15| 14 | 13| 12| 11| 10|  9|  8|  7|  6|  5|  4|  3|  2|  1|  0|
|---|-----------|-----------|-----------|-----------|-----------|
 Field/bit Definitions:

|<--------- A --------->|          |<--------- B --------->|
```

where:

bit 0 = CMD CHAN FLAG F/F

Field B = USER DEFINED:
    bit 1 = (READ))
    bit 2 = (WRITE) > USER CONTROLLED
    bit 3 = (EOF)   )
    bit 4 = ERROR
    bit 6 = POWER FAIL

bit 7 = POWER ON NORMAL

bit 8 = CRS STRETCHED

bit 9 = CMD CHAN CMD

Field A = COMMAND (bits 10-15)

471004-295, 2 of 2

STATUS WORDS

INTERFACE CABLE SIGNAL INDEX

HP 30361-60001

SIGNAL NAME (3000)	P1	P2	SIGNAL NAME (2100)	SIGNAL NAME (3000)	P1	P2	SIGNAL NAME (2100)
DO 2	C1A	28A	BI 13	W8	B18A/B		
DO 4	C2A	30A	BI 11	CONT 9	B21A	46A	STS 2
CONT 6	C3A	48A	HDFLG	DEV END	B25A	17A	CW 15
CONT 8	C4A	45A	STS3				
CONT 7	C5A	44A	STS 4	STAT 8	A1A	23A	HDCMD
DO 1	C8A	27A	BI 14	DEV FLAG	A2A	24A	LDCMD
DO 3	C9A	29A	BI 12	STAT 9	A6A	18A	CW 14
DO 7	C10A	33A	BI 8	DO 13	A7A	39A	BI 2
DO 5	C11A	31A	BI 10	DO 12	A8A	38A	BI 3
DO 6	C12A	32A	BI 9	DI 8	A9A	9A	BO 7
DO 0	C13A	26A	BI 15	DI 14	A10A	15A	BO 1
STAT 12	C14A	19A	CW 13	DI 15	A11A	16A	BO 0
DI 7	C15A	8A	BO 8	DI 12	A12A	13A	BO 3
DI 6	C16A	7A	BO 9	DI 13	A13A	14A	BO 2
DI 4	C17A	5A	BO 11	DI 10	A14A	11A	BO 5
DI 5	C18A	6A	BO 10	DI 11	A15A	12A	BO 4
STAT	C19A	21A	CW11	DI 9	A16A	10A	BO 6
DI 1	C20A	2A	BO 14	DI 8	A17A	34A	BI 7
DI 0	C21A	1A	BO 15	CONT 10	A19A	47A	STS 1
STAT 15	C22A	22A	CW 10	DEV CMD	A20A	49A	LDFLG
DI 3	C23A	4A	BO 12	DO 15	A21A	41A	BI 0
DI 2	C24A	3A	BO 13	DO 14	A22A	40A	BI 1
STAT 13	C25A	20A	CW 12	DO 9	A23A	35A	BI 6
				DO 10	A24A	36A	BI 5
POWFAIL	B1A	42A	STS 6	DO 11	A25A	37A	BI 4
PON	B2A	25A	PON	–	C6B	50A	GND

Note: *The above table shows only the positive line outputs and inputs of the differential line drivers. In all cases, the negative line is the same pin number on the B side of the connector i.e., D02 (negative) pin numbers are P1-C1B and P2-28B.*

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INTERFACE CABLE SIGNAL INDEX

LINE TESTER

The Line Tester gives you a simple, effective check of the physical link between the HP 3000 and the Controller. It tests the two interface cards and the cable that connects them. The interface is tested by transmitting a known data pattern from the HP 3000 to the Controller. The Controller then transmits the data pattern it received back to the HP 3000 where it is compared against the data pattern set. If the two data patterns do not compare exactly, and error message is reported on the HP 3000 interactive terminal.

The Line Tester consists of two software components, LTEST and LINETEST. LTEST is an absolute binary program you load onto the Controller with the Basic Binary Loader (BBL). LINETEST is an HP 3000 program installed when the system is generated. To test the interface, load LTEST on the Controller and put it in a run state before activating LINETEST on the HP 3000.

LOAD AND START

The following table shows how to load and run LTEST

NOTE

> The steps outlined in the table assume that BBL is loaded on the controller.

Load and Run LTEST

STEP COMMENT

A. Start the Basic Binary Loader

1. On the Controller front panel, press the HALT/CYCLE button to light it.
2. Press the P button
3. Press CLEAR DISPLAY
4. Enter the octal starting address of BBL, as shown, in the DISPLAY

   4K = 007700 16K = 037700
   8K = 017700 24K = 057700
   12K = 027700 32K = 077700

5. Press EXTERNAL RESET
6. Press INTERNAL PRESET
7. Press LOADER ENABLE

B. Load the paper tape reader

1. Press the POWER switch to turn the reader ON
2. Press the LOAD switch
3. Insert the paper tape containing LTEST
4. Press the READ switch
5. Press RUN on the Controller front panel

NOTE

> After the tape is read, the Controller halts. 1020XX is in the DISPLAY REGISTER if:
>
> xx=11 a checksum error occurred. Check for torn tape or dust in the reader. Check for ragged edges or torn holes. Return to step 2A.
>
> xx=55 an address error occurred. LTEST attempted to enter the area reserved for BBL, or a location not available in the Controller. Check that the proper tape was used and that it is properly placed in the reader.
>
> xx=77 LTEST was loaded correctly.

C. Start LTEST

1. On the Controller front Panel press the P button.
2. Press CLEAR DISPLAY
3. Enter 000002 octal into the DISPLAY REGISTER
4. Press RUN
5. Press the S button
6. Press CLEAR DISPLAY
7. Enter the lowest select code of the interface board in the DISPLAY REGISTER
8. Press RUN
9. Press the P button
10. Press CLEAR DISPLAY
11. Enter the starting address of LTEST, as shown below.

    Enter 100 octal for use with DMA

    Enter 150 octal to test using hood supplied with interface PCA

12. Press RUN

    LTEST is now is a run state. The EXTEND lamp is lit, indicating that the Controller is ready to read data. When the Controller is ready to write data, the OVFLO lamp is lit.

RUN LINETEST IN NORMAL MODE

To run LINETEST in the normal mode, use the following procedure.

```
:RUN LINETEST

     HP 30300A.00.0 LINE TEST

     LOGICAL DEVICE #?-------
```

Enter the lcgical device number of the interface card.

```
     PAUSE AFTER ERROR (Y/N)?-
```

Enter Y to pause or N to terminate.

```
     LINE TEST COMPLETE ::PASSES:nnn**ERRORS:nnn

     END OF PROGRAM
```

If an error occurs in any read/write cycle, an error message is displayed on the HP 3000 interactive terminal.

If you select the PAUSE option and after all errors from a given pass are printed, the program prints:

```
     CONTINUE TEST (Y/N)?
```

This enables you to manually halt the HP 2100 and display the contents of the data buffer. By comparing the words in error on both the HP 3000 and HP 2100, you can determine if the word was received correctly by the HP 2100.

If you respond with Y, the test continues with the next cycle. Otherwise, the program terminates.

The test cycle starts with a block transfer length of one word, then two words, then three words until the transfer length equals decimal 512 complete write/read cycles, the test continues with 100 additional write/read cycles with a block transfer of decimal 2048 words.

The test terminates with:

```
     LINE TEST COMPLETE**PASSES:nnn**ERRORS:nnn
```

RUN LINETEST IN DIAGNOSTIC MODE

In the diagnostic mode of LINETEST, you can select the number of passes to be made, the word pattern to be transmitted, and the size of the block to be transmitted. To do this, use the following procedure:

```
:HELLO FIELD.SUPPORT,HP 30361

:RUN LINETEST,DIAG

HP 30300A.00.0 LINETEST

LOGICAL DEVICE#?-----
```

Enter the logical device number of the interface card.

```
SELECT OPTIONS

NUMBER OF PASSES?------
```

Enter the number of passes desired. Maximum number is decimal 32767. Zero or CR causes a default value of one to pass to be used.

```
WORD PATTERN--?---
```

Enter a decimal or octal word to be transferred. Illegal input causes the message INPUT ERROR to be printed. Enter a correct value to continue or enter a CR to use the default value of octal 177777.

```
BLOCK SIZE(<=2048)?
```

Enter the desired block size of the transfer. A non-numeric entry or CR causes the block size to ba variable as described for normal mode operation. If a value greater than 2048 us entered, a default value of 2048 is used.

```
PAUSE AFTER ERRORS (Y/N)?
```

Enter Y to pause or N to report errors only.

After the requested number of passes have been made, LINETEST prints a completion message and asks if you want to continue. If you want to terminate, enter zero or CR to:

```
LINE TEST COMPLETE**PASSES:nnn**ERRORS:nnn  CONTINUE TEST
(Y/N)?
```

To continue, enter Y, otherwise enter N.

ERROR REPORTING

Errors are reported on the HP 3000 interactive terminal in the following format.

```
***ERROR***WORDnnn SHOULD BE xxxxxx IS yyyyyy
```

The message means that the word transmitted from the Controller to the HP 3000 does not match the word sent from the HP 3000 to the Controller. You can tell whether the Controller received the word properly by displaying the word received in the DISPLAY REGISTER. The Controller input buffer begins at location octal 2000 and the message tells you what word in the buffer to display. Word 1 would be in location octal 2000, word 8 in location octal 2007, word 9 in location octal 2010, word 17 in location octal 2028, etc.

BLOCK SIZE(<=2048)?

Enter the desired block size of the transfer. A non-numeric entry or CR causes the block size to ba variable as described for normal mode operation. If a value greater than 2048 us entered, a default value of 2048 is used.

PAUSE AFTER ERRORS (Y/N)?

Enter Y to pause or N to report errors only.

After the requested number of passes have been made, LINETEST prints a completion message and asks if you want to continue. If you want to terminat, enter zero or CR to:

```
LINE TEST COMPLETE**PASSES:nnn**ERRORS:nnn CONTINUE TEST
(Y/N)?
```

To continue, enter Y, otherwise enter N.

ERROR REPORTING

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MAINTENANCE PANELS
30350A/30352A/30354A/30354D

DIFFERENCES FROM SERIES II

The 30350A and 30352A Maintenance Panels were designed for the Pre-Series II systems.

The 30354A Maintenance Panel was designed for the Series II.

The 30354D Maintenance Panel was designed for the Pre-Series II.

MAINTENANCE PANELS

GENERAL INFORMATION

All HP 3000 pre Series II Computer Systems come equipped with a mini-Control Panel. This panel enables Cold-Load, Console Interrupt, System Dump, and Power Fail functions.

Hardware and Software diagnosis requires the use of the HP 30350A Auxiliary Maintenance panel and the HP 30352A Hardware Maintenance Panel or the new HP 30354A option 001 Hardware Maintenance Panel.

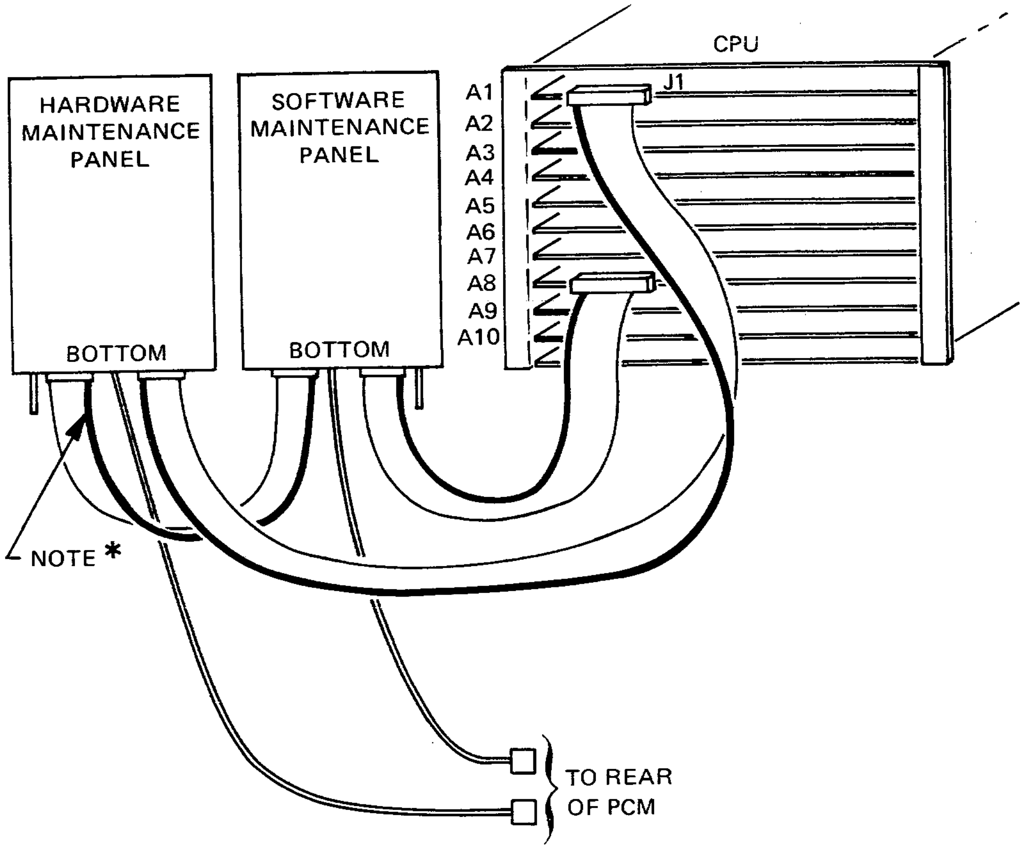
Either type of maintenance panel must be installed before running any stand-alone diagnostic in order to read the Halt codes in the Current Instruction Register (CIR).

All stand-alone diagnostics require the switches on the panels to be in the "DOWN" position before starting.

INSTALLING MAINTENANCE PANELS

CAUTION

> The additional current load required by the maintenance panels may cause the top HP 30310A power supply in the CPU bay to crowbar.
>
> This is not the case on the HP 3000 Series I. All DC power is provided by the HP 30312A power supply in the PIO bay.



* RED WIRE IS SOMETIMES CONNECTED AT LEFT SIDE (CONNECTOR IS REVERSED)

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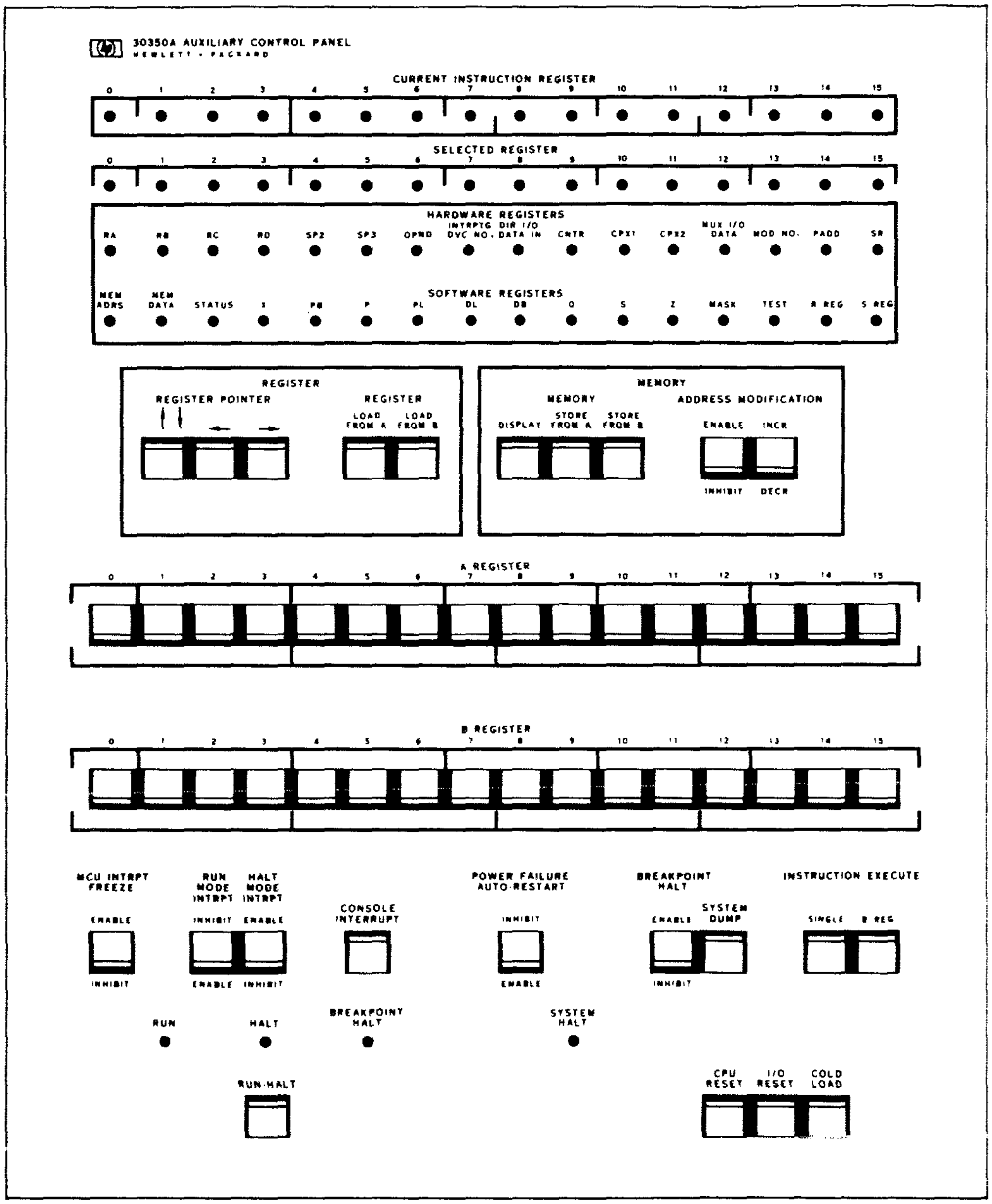
MAINTENANCE PANEL CONNECTIONS



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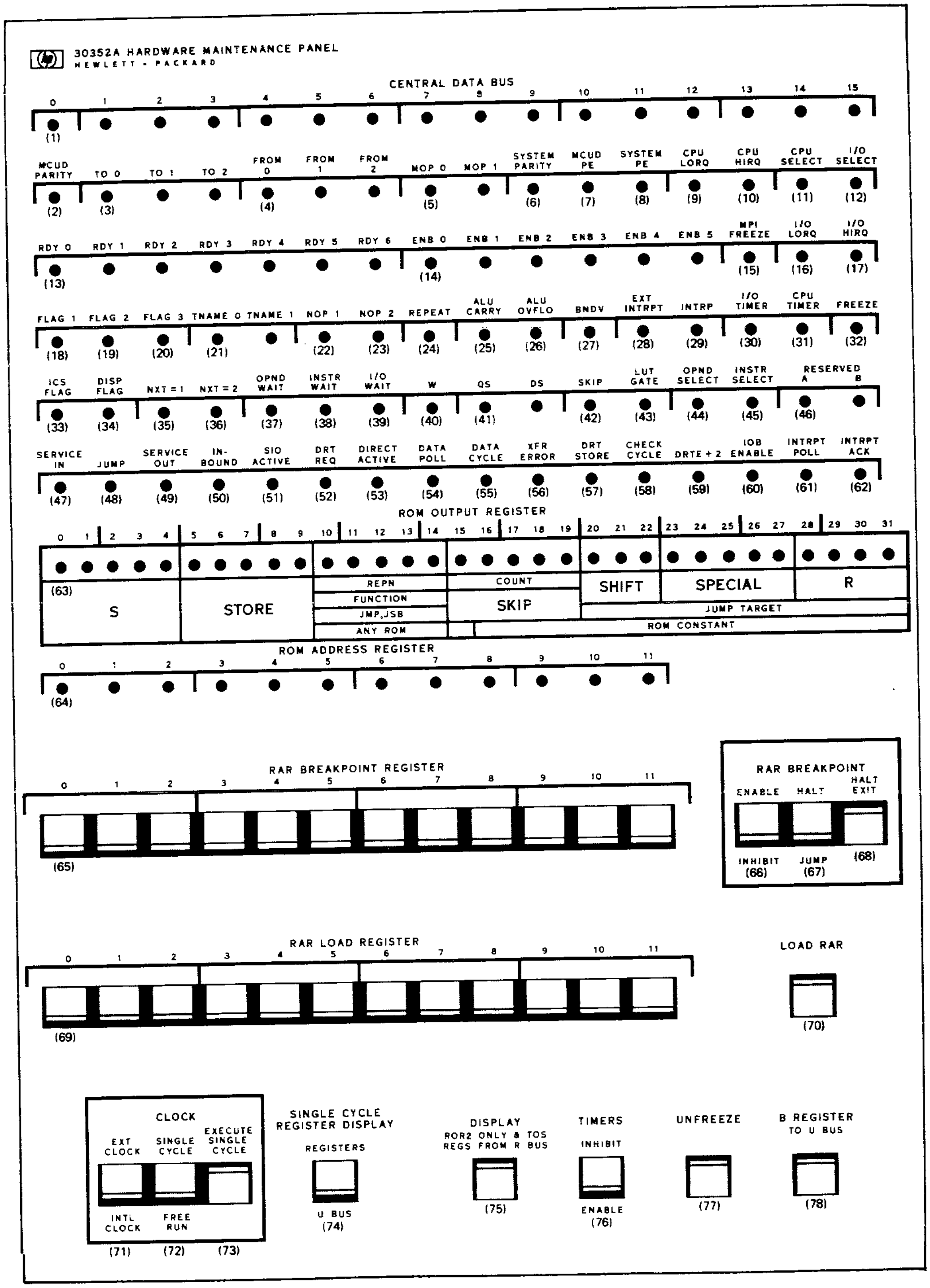
AUXILIARY CONTROL PANEL



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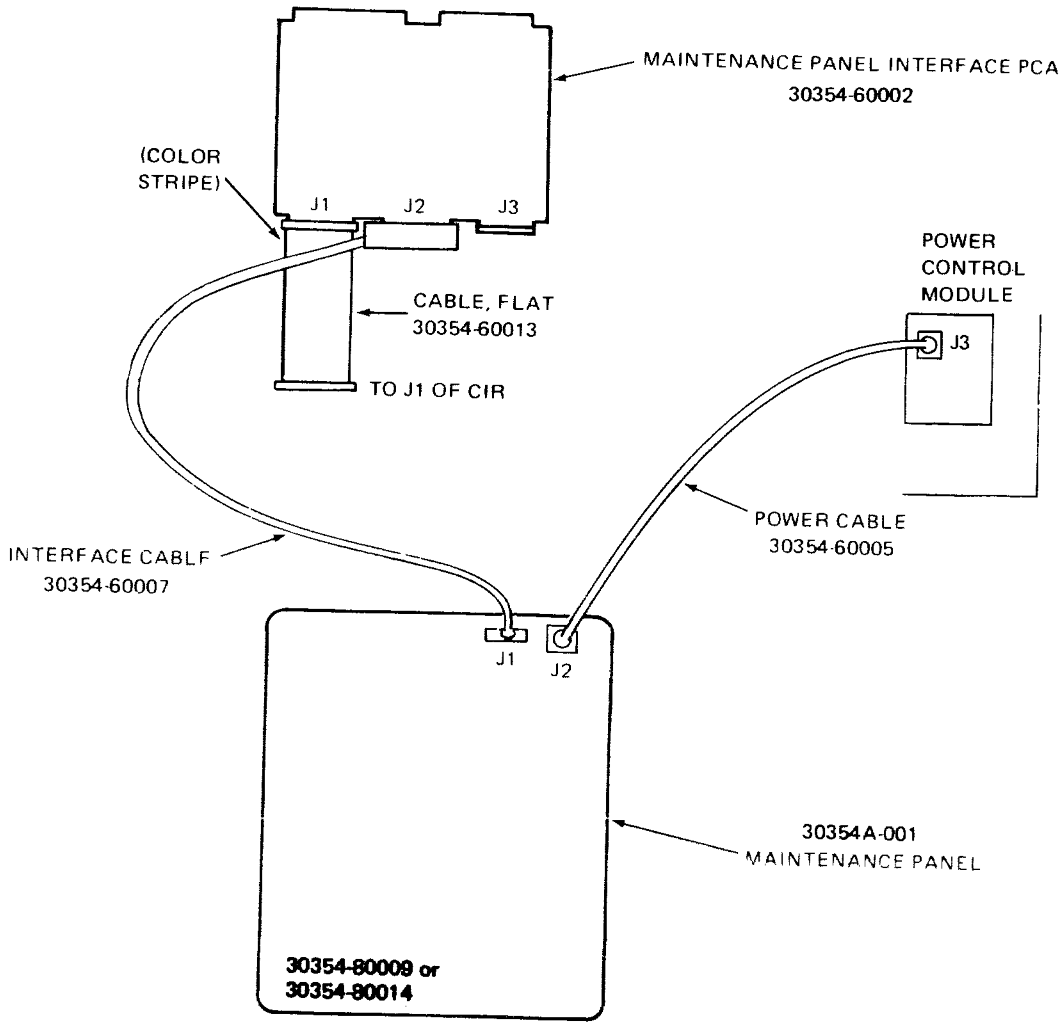
HARDWARE MAINTENANCE PANEL



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CONNECTIONS FOR USE

CIR	Current Instruction Register — contains the current executing/ed, instruction.
CNTR	Counter register — used as a microcode counter. When in halt, contains the number of valid TOS hardware registers.
COR	CPU Output Register — serves as the data path to the central data bus for the CPU. Sourced either from the U-bus for Read/Write Address or Write Data or from the P-register for the read address of the next instruction to be fetched.
CPX1	CPU interrupt status (RUN) register — run mode status
CPX2	CPU interrupt status (HALT) register — halt mode status
DB	Data Base register — contains the absolute address of the first location of the stack global area.
DIR I/O DATA IN	Direct I/O Data In register — contains the data read by a "RIO" instruction.
DL	Data Limit register — contains the absolute address of the first location of the stack.
INTRPTG DVC NO	Interrupting Device Number register — contains the device number of the last device to have interrupted.
MUX I/O DATA	Multiplexor I/O Data register — contains the multiplexed data to be written to memory. Can only be read in single cycle with register display.
MASK	Mask register — contains the last interrupt mask word issued to all I/O devices. It does not necessarily reflect the state of a device's interrupt mask. This may have been set by a master reset to that device issued since a "SMSK" instruction.
MEM ADRS	Memory Address — Scratch Pad 0 used in halt to contain the address of a "panel" memory display or store.
MEM DATA	Memory Data — Scratch Pad 1 used in halt to "panel" display memory data.
MOD NO.	Module Number register — contains the CPU ID number in bits 8-10 and (if) the interrupting module number in bits 0-2. The remaining bits are zero.
NIR	Next Instruction Register — receiver register for instructions returned to the CPU on the central data bus.
OPND	Operand register — receiver register for data returned to the CPU on the central data bus.
P	Program register — when in halt, contains the absolute address of the next instruction to be executed. When running, contains the absolute address of the next instruction to be fetched. States between the two are microcode dependent.

PADD	Preadder — contains the hardware preadd result of the current executing instruction.
PB	Program Base register — contains the absolute address of the first location of the code segment.
PL	Program Limit register — contains the absolute address of the last location of the code segment, the start of the Segment Transfer Table.
Q	Q register — contains the absolute address of the first location of the current temporary stack.
RA,RB, RC,RD	Four TOS registers — they map thru the TNAME logic to the four hardware registers TR0, TR1, TR2, TR3.
RAR	ROM Address Register — contains the address of the current ROM instruction being fetched.
ROR1	ROM Output Register 1 — contains the contents of the addressed location previously specified by RAR (current RAR-1).
ROR2	ROM Output Register 2 — contains the previous contents of ROR1 or the contents of the addressed location specified two clock cycles prior by RAR (current RAR-2).
S	Stack (memory) register — contains the absolute address of the last word of the stack in memory. S as displayed by the "panel", is always the SM register. Pseudo register S is equal to SM+SR and when in halt, SR always equals zero; therefore SM=S. In other words, S is used rather than SM strictly for software purposes, although the display is always SM.
SAVE	Save register — contains the return address of a microcode jump subroutine call.
SP2	Scratch Pad 2 — microcode scratch register.
SP3	Scratch Pad 3 — microcode scratch register.
SR	Stack Register — contains the number of valid hardware registers. SR is pushed into CNTR during halt, TOS registers "QDOWN"ed, and SR zeroed.
STATUS	Status register — contains the current CPU status.
TEST	Test register — an MPI register whose input is derived from an edge connector on the Maintenance Panel interface PCB.
X	X register — hardware index register and general purpose software register.
Z	Z register — contains the absolute address of the last available word of the data segment.