OPERATING AND SERVICE MANUAL
13181B

DIGITAL MAGNETIC TAPE UNIT INTERFACE KIT
(FOR 21MX SERIES COMPUTERS)

13181-60074, Series 2145
13181-60075, Series 2145

Manual Part No. 13181-90901
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GENERAL INFORMATION

1-1. INTRODUCTION

This manual covers general information, installation, programming, theory of operation, maintenance, and replaceable parts for the HP 13181B Tape Unit Interface Kit (see figure 1-1). Options 001, 002, and 003 for the interface kit are also covered in this manual.

1-2. GENERAL DESCRIPTION

The HP 13181B Tape Unit Interface Kit interfaces up to four nine-track HP 7970 Series Digital Magnetic Tape Units with a single HP 21MX Series Computer. The interface kit includes two plug-in printed circuit assemblies, which contain complete tape motion and data transfer control circuitry. An interconnect cable is provided to connect the printed-circuit assemblies to the tape unit. DMA is recommended for 45 ips configurations. For all other configurations DMA may be used but is not required.

1-3. INTERFACE KIT CONTENTS

The HP 13181B Tape Unit Interface Kit contains:

a. Mag Tape 1 (Control) Card.

   1. Part number 13181-60074 (45 ips) (37.5 ips, option 001) (25 ips, option 002) (12.5 ips, option 003).

b. Mag Tape 2 (Data) Card, part number 13181-60075

c. Interconnect cable, part number 13181-60030.

d. *Operating and Service Manual*, part number 13181-90901.

1-4. IDENTIFICATION

Hewlett-Packard utilizes five digits and a letter (00000X) to identify standard HP interface kits. Options to the standard kit are identified by a three-digit numerical suffix (001, 002, etc.). If the HP designation on the interface kit does not correspond to the designation on the title page of this manual (13181B), the kit received is different from the kit described in this manual.

Printed-circuit assembly revisions are identified by a letter, a series code, and a division code marked beneath the part number on the card. The letter identifies the etched trace pattern on the unloaded board. The four-digit series code identifies a particular configuration of the loaded printed-circuit board. The two-digit division code identifies the division of Hewlett-Packard that manufactured the assembly. If the series code numbers do not correspond exactly with the code numbers on the title page of this manual, the assemblies differ from those described in this manual. These differences are covered in manual supplements available at the nearest HP Sales and Service Office.

The interconnect cable is identified by a part number marked on one of the attached connectors.

1-5. OPTIONS

The standard version of the interface kit is for use with tape units that operate at 45 ips. Option 001 provides the interface assemblies used for operation at 37.5 ips, option 002 for 25 ips, and option 003 for 12.5 ips. The only physical difference between the assemblies is in the jumper arrangement on the printed-circuit board. All information in this manual applies to options 001, 002, and 003, as well as the standard interface kit, except where differences are noted.

1-6. SPECIFICATIONS

Specifications for the interface kit are listed in tables 1-1 and 1-2.

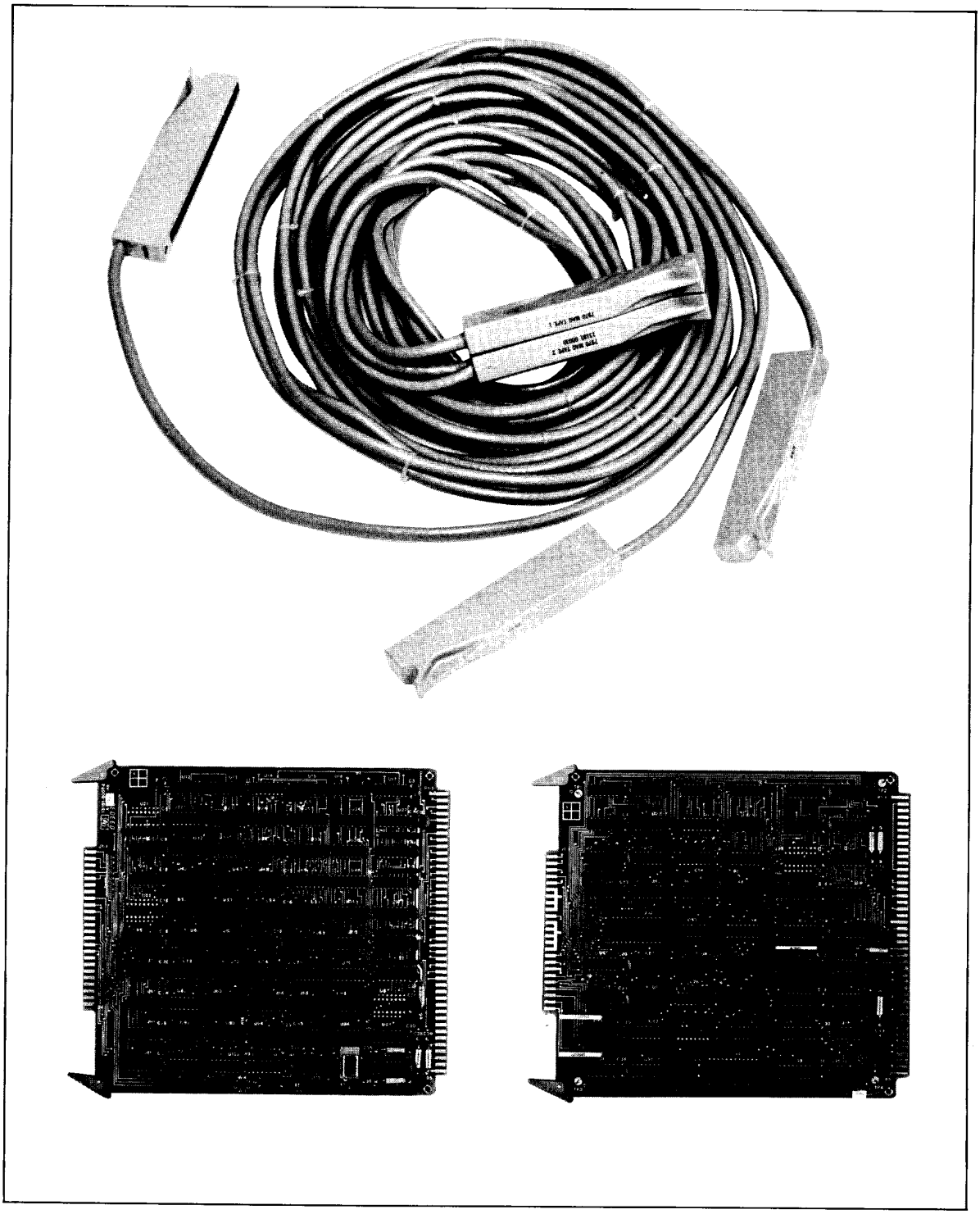


Figure 1-1. HP 13181B Tape Unit Interface Kit

TABLE 1-1. INTERFACE KIT SPECIFICATIONS

POWER REQUIRED FROM COMPUTER

+4.85 Volt Supply: 2.0 amperes
-2.0 Volt Supply: 0.05 amperes

MINIMUM DATA RECORD

One computer word (two EBCDIC or ASCII data characters) plus CRCC and LRCC.

TAPE DENSITY

800 characters (bytes) per inch (Refer to table 1-2.)

TAPE SPEEDS

12.5, 25, 37.5, and 45 inches per second (Refer to table 1-2.)

OPERATING TEMPERATURE

0° C to 55° C

STORAGE TEMPERATURE

-40° C to 75° C

TABLE 1-2. MULTISPEED CHARACTERISTICS

TAPE SPEED (IPS)	DATA CHANNEL BYTE RATE (IN CPS)	MAXIMUM DATA CHANNEL FLAG READ SERVICE TIME (IN μs)	DATA CHANNEL FLAG OCCURRENCE INTERVAL (IN μs)
12.5	10,000	82	200
25	20,000	41	100
37.5	30,000	27	67
45	36,000	22	56

SECTION II
INSTALLATION

2-1. INTRODUCTION

This section provides instructions for unpacking, initial receiving inspection, and installation of the HP 13181B Tape Unit Interface Kit. The computer and tape unit should be installed and in an operating condition prior to interface kit installation.

2-2. UNPACKING AND INSPECTION

If the shipping carton is damaged upon receipt, request that the carrier's agent be present when the kit is unpacked. Inspect the kit for damage (cracks, broken parts, etc.). If the kit is damaged and fails to meet specifications, notify the carrier and the nearest Hewlett-Packard Sales and Service Office immediately. (Sales and Service Offices are listed at the back of this manual.) Retain the shipping container and the packing material for the carrier's inspection. The Hewlett-Packard Sales and Service Office will arrange for the repair or replacement of the damaged kit.

2-3. POWER REQUIREMENTS

The two interface assemblies obtain operating power directly from the power supply of the associated computer. The assemblies require 2.0 amperes from the +4.85 volt source and .05 amperes from the −2.0 volt source. Prior to interface assembly installation, check that the assemblies will not overload the computer power supply. If the addition of the two assemblies will result in an overload, a power supply extender should be ordered for the computer. Prior to installation, ensure that the tape unit to be interfaced with the computer is close enough to allow the cable to be properly routed and connected.

2-4. INSTALLATION PROCEDURES

Interface kit installation consists of inserting the Mag Tape 1 (control) printed-circuit assembly into appropriate computer I/O slot and then routing the interconnect cable to the tape unit.

2-5. INTERFACE ASSEMBLY INSTALLATION

Install the Mag Tape 1 and Mag Tape 2 printed-circuit assemblies as follows (see figure 2-1):

a. Turn off all power to the tape unit.

b. Set the computer power switch off.

c. Access the computer card cage and select the two adjacent slots corresponding to the desired I/O select codes. Make certain that all higher priority slots have either another I/O card or a priority jumper card installed.

CAUTION

The printed-circuit assemblies are keyed to prevent improper insertion. Do not use force when inserting the assemblies and make certain the slots in the printed-circuit boards correspond to the proper keys in the connectors.

d. Insert the Mag Tape 1 assembly into the higher priority (lower) slot.

e. Insert the Mag Tape 2 assembly into the lower priority slot.

2-6. INTERCONNECT CABLE INSTALLATION

The interconnect cable consists of three, twisted-pair cables with keyed connectors and is installed as described below (see figure 2-2):

a. Connect MAG TAPE 1 and MAG TAPE 2 hooded connectors P1 and P2 to the Mag Tape 1 and Mag Tape 2 assemblies, respectively, as illustrated in figure 2-1.

b. Gain access to the tape unit interconnect facilities and route the cable within the tape unit as illustrated in figure 2-2.

c. Connect READ hooded connector P3 to the Read Data assembly.

d. Connect WRITE hooded connector P4 to the Write Data assembly.

e. Connect CONTROL hooded connector P5 to the Control and Status printed-circuit assembly.

2-7. INSTALLATION CHECKOUT

After installing the interface kit, restore power to the tape unit and computer and prepare the system for operation. Refer to the computer and tape unit operating instructions, and perform the diagnostic test contained in the *Diagnostic Manual*, part number 13181-90095.

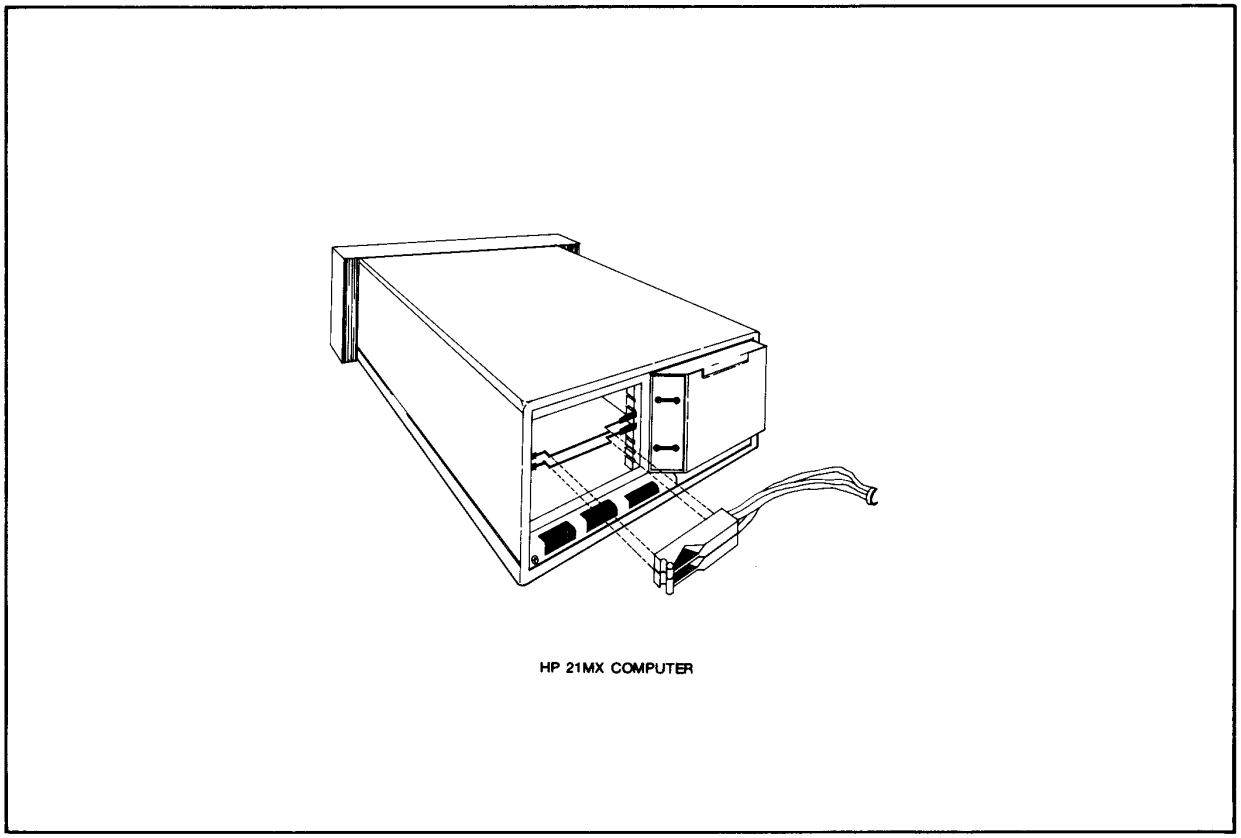


Figure 2-1. Typical Interconnect Cable Installation at the Computer

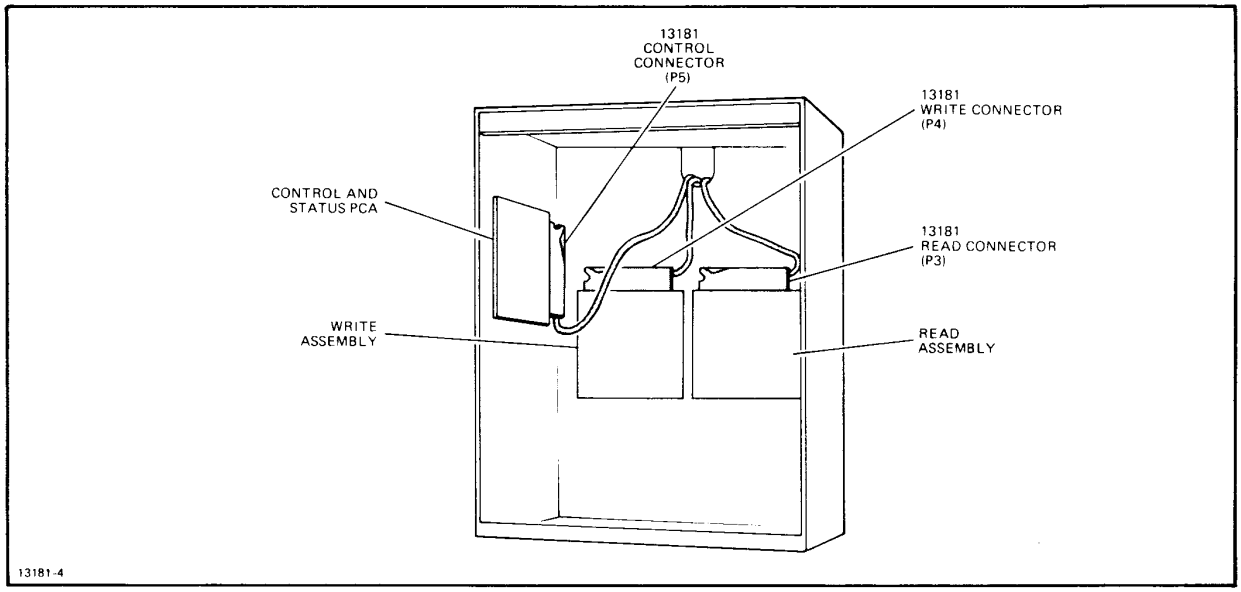


Figure 2-2. Interconnect Cable Installation at the Tape Unit

SECTION III
PROGRAMMING

3-1. INTRODUCTION

This section contains programming information for the interface kit, including tape unit characteristics, controller commands and status, parity, packing densities, and data transfer rates.

3-2. TAPE UNIT CHARACTERISTICS

The HP 13181B Tape Unit Interface Kit provides a complete nine-track interface between up to four HP 7970B/C Series Digital Magnetic Tape Units and a single HP 21MX-Series Computer. The interface provides all tape motion and data transfer control signals required for generating IBM-compatible nine-track formats. The multi-speed capability of the interface kit permits interfacing with tape units operating at 12.5, 25, 37.5 or 45 inches per second with a packing density of 800 characters per inch. (Commonly controlled parallel tape units must be at the same tape speeds.)

The interface kit requires two computer I/O addresses: a command channel address and a data channel address. The data channel is assigned the higher priority I/O address. DMA is recommended for 45 ips tape units. For all other configurations DMA may also be used.

3-3. CONTROLLER COMMANDS

All commands are transferred through the A- or B-register of the computer to the command channel by an OTA/B instruction. The commands are stored in the controller and executed when a Set Control (STC) instruction is transmitted to the control circuits, except for tape unit select commands. The STC instruction causes the controller to execute the command. In the event of multiple OTA/B instructions before an STC instruction, the controller will execute the last instruction.

All valid commands switch the interface from the ready to the busy state and clear the controller-oriented status bits.

The four unit select commands, unless rejected, are output by the OTA/B instruction in one computer cycle. The unit select commands are executed immediately; do not require buffering and do not cause an interrupt.

NOTE

The Reject flip-flop (FF) will be set if either a command which requires write current is given while the write enable ring is not installed on the tape unit, a reverse motion command is given at the beginning-of-tape (BOT), a command which requires motion is given when the tape unit or controller is not ready, or a unit select command is given when the controller is ready.

When all on-line operations requiring tape motion have been completed, a clear operation is completed, or a Rewind or Rewind/Off-Line command has been initiated, the interface generates a command channel flag. The command channel flag sets when the interface is not busy. The control bits in each channel of the interface operate as in a normal I/O assembly, except that clearing a control bit in the data channel during a write operation initiates the writing of an end-of-record sequence and stops tape motion. Clearing the control bit in the data channel during a read operation inhibits transfer of data to the computer, although the read operation continues in the tape unit and the controller until the inter-record gap is reached. At this time, the controller is ready and the command channel flag is set.

The bits that make up command words are detailed in table 3-1.

TABLE 3-1. COMMAND WORD BITS

BIT	FUNCTION	BIT	FUNCTION
0	Motion	7	File
1	Forward	8	Change Select
2	Gap/Off-Line	9	Select 0
3	Write/Clear	10	Select 1
4	Data Transfer	11	Select 2
5	Reverse		
6	Rewind/Clear	12	Select 3

TABLE 3-2. COMPUTER TO CONTROLLER COMMANDS

CODE (OCTAL)	MNEMONIC	FUNCTION
31	WCC	Write One Record
15	GAP	Write 4 Inches Blank Tape
23	RRF	Read One Record
3	FSR	Forward Space One Record
41	BSR	Backspace Record
105	RWO	Rewind and Off-Line
101	REW	Rewind
110	CLR	Clear Controller
211	WFM	Write File Mark
1400	SEL0	Select Unit 0 (1)
2400	SEL1	Select Unit 1 (1)
4400	SEL2	Select Unit 2 (1)
10400	SEL3	Select Unit 3 (1)
203	FSF	Forward Space File
241	BSF	Backspace File
215	GFM	Gap and Write File Mark

Note:

1. Tape unit select commands are to be applied only with an OTA/B instruction; do not apply a subsequent STC,C instruction.

The interface responds to the commands listed in table 3-2. Commands other than those listed will cause improper operation. The following paragraphs describe each of the computer commands for the command channel.

3-4. Write One Record (WCC)

The WRITE ONE RECORD command switches the tape unit to the write mode, which turns on the write head current, initiates forward motion, and causes the interface to set the data flag for each computer word to be written on the tape. The computer word is unpacked and written on tape. (The high eight bits of the computer word are written first, the low eight bits second.) At 45 ips the computer has 27 microseconds to output the requested word after the data channel flag bit is set.

The interface generates odd parity for each character resulting from the output word as the character is written. The Longitudinal and Cyclic Redundancy Check Character (LRCC and CRCC) signals are automatically generated after the end-of-record sequence is started by a Clear Control Instruction (CLC). The CLC instruction is addressed to the data channel to clear the data channel control bit immediately following the last word to be written. If the tape is at BOT when the WCC command is given, the interface will automatically erase four inches of tape before requesting the first computer word. All written records are automatically read by the tape unit and vertical parity, LRCC, and CRCC are checked. (The CRCC is not checked except for its contribution to the LRCC.) Thus each record can be verified by checking the parity/timing error bit of the status word after writing.

When the read-after-write check is complete, the tape drive stops and the command channel flag bit is set to signal that the interface is ready to accept the next command.

3-5. Gap 4-Inches (GAP)

The GAP 4-INCHES command enables the write current and causes the tape unit to erase four inches of tape. When the operation is completed, motion is terminated, the command channel flag bit is set, and the interface is ready for the next command.

3-6. Read One Record (RRF)

The READ ONE RECORD command causes the interface to input characters read from tape via bits 0 through 15 of the input data channel. The first of each pair of bytes is placed in the high eight bits of the computer word, the second byte in the low eight bits. Tape characters are read, vertical parity is checked, the parity bit is discarded, and the characters are packed into one 16-bit computer word.

The data channel flag sets when the second byte is read. Failure to respond to the flag within the data channel flag occurrence interval (refer to table 1-2) will set the parity/timing error bit and the timing error status bit. If the available core area in the computer is smaller than the tape record, the program should clear the data channel control bit when the available core area is full. This prevents the data channel flag from being set and thus prevents a timing error.

Tape motion continues until the next IRG is detected. The parity of the entire record (including the CRC and LRC character) is checked and the tape is halted in the IRG. The CRCC and LRCC signals are not input to the computer. If a parity error occurred, the parity/timing error bit (bit 1) in the status word is set. The flag on the command channel is set to signal that the interface is ready to accept the next command. A file mark is treated as a record. The 023 octal file mark character is input and the EOF bit (bit 7) and the Odd Number of Bytes Read bit (bit 11) within the status word are set. The program can terminate reading anywhere within a record by addressing a Clear Control (CLC) instruction to the data channel. The tape will continue until the IRG is found, but additional data channel flags will not occur. However, both vertical and longitudinal parity will be checked.

NOTE

Records written by the controller will always contain an even number of bytes; however, records written on other systems may contain an odd number of bytes. During a Read One Record forward operation, the controller will read the final (odd) byte but will not immediately set the data channel flag bit since the byte only fills the high eight bits of the data word.

The read operation will be interrupted for the equivalent of three byte times. At this time, an internal counter will signal end-of-data. The combination of the odd byte and the end of data is sensed, and command channel status bit 11 is set. The same combination now sets the data flag bit to load the final byte. The final byte occupies the upper eight bits of the final word. The lower eight bits are indeterminate. When reading a record written on a system that records an odd number of bytes, always load the command channel status bit 11 following an RRF operation. This will allow bit 11 to be tested in order to determine the actual number of tape bytes (2n or 2n-1 bytes, where n = number of words transmitted). Bit 11 should be ignored if bit 7 (EOF) is set.

3-7. Forward Space One Record (FSR)

The FORWARD SPACE ONE RECORD command moves the tape forward until the next IRG is detected, and tape motion ceases. The command channel flag is then set to signal that the interface is ready. Data is not transferred, but a parity error can be detected.

3-8. Backspace One Record (BSR)

The BACKSPACE ONE RECORD command moves the tape backwards until either the IRG or the BOT (beginning-of-tape) is detected. Motion is then terminated, the command channel flag is set, and bit 6 of the status word is set if BOT was detected. Data is not transferred, but a parity error can be detected.

NOTE

A record containing an odd number of data bytes will set the parity error bit during a BSR because the CRCC for such records has even vertical parity.

3-9. Rewind (REW)

The REWIND command causes the tape to rewind until the BOT reflective marker is found. If the tape is already at BOT, no action is taken. The command reject bit is not set.

After the REWIND command is output to the tape unit, the controller is set ready for use with any other tape drive while the rewind is in process. (A different tape unit may be selected.) While the selected tape unit is rewinding, the rewind bit (bit 10) and the transport busy bit (bit 9) will be set in the status word.

Any command that requires tape motion is rejected if given while the selected unit is rewinding, and the Reject FF and the reject status bit (bit 3) will be set.

3-10. Rewind Off-Line (RWO)

The REWIND OFF-LINE command positions the tape at BOT and switches the transport from on-line to off-line status. It operates in the same manner as the REWIND command, except the selected tape unit is switched to off-line status as well. When the command is issued at load-point, rewind is not affected but the tape unit does go off-line.

NOTE

Use of this command will require operator intervention to restore on-line status before another command may be given to the tape unit addressed by the RWO signal.

3-11. Write File Mark (WFM)

The WRITE FILE MARK command writes the file mark code (023 octal) on tape, and then the accompanying LRCC (023 octal) eight character-spaces following. When tape motion has ceased, the interface sets the command channel flag bit.

3-12. Clear Controller (CLR)

The CLEAR CONTROLLER command may be given at any time. The command clears the command and data channel control flag FFs to the initial states (normal, ready state), terminating any tape unit operation except rewind. The parity/timing error bit, reject bit, data timing error bit, end of file bit, and odd number of bytes read bit are cleared. The command channel flag and not busy status is set at the end of a tape unit operation.

3-13. Forward Space File (FSF)

The FORWARD SPACE FILE command moves the tape forward until the next file mark or the end of tape is detected. The command channel flag is set, and bit 7 of the status word (EOF) is set when the tape stops if the file mark was detected. If the end of tape was detected, the EOT status bit (bit 5) is set, the FSF signal is changed to an FSR signal, and the tape will stop in the next IRG rather than after the file mark. If the previous record contained an odd number of bytes, the odd number of bytes status bit is set.

3-14. Backspace File (BSF)

The BACKSPACE FILE command moves the tape in the reverse direction until a file mark or the beginning of tape is detected. The command channel flag is set, and bit 7 of the status word is set when tape motion ceases if the file mark was detected. If the load-point was detected, the load-point status bit (bit 6) is set.

3-15. Gap and Write File Mark (GFM)

The GAP AND WRITE FILE MARK command combines GAP and WFM to erase four inches of tape and writes the file mark code (023 octal) and the accompanying LRCC character in the eighth character space following.

3-16. Select Unit 0, 1, 2, or 3 (SEL)

The Select Unit 0, 1, 2, or 3 command causes the designated tape unit to be selected for subsequent computer commands, and status from that tape unit to be sent to the controller. Tape unit selection must be made after power turn-on, as the selected register contents are random at that time.

3-17. CONTROLLER STATUS

Status information is transferred via the computer A- or B-register through the command channel with the standard I/O instructions : Load into A- or B-register (LIA/B), or Merge into A- or B-register (MIA/B). The status word bits are listed in table 3-3, and the bits are described in the following paragraphs. The tape unit status bits are available only when that tape unit is selected.

The 12-bit status word may be input through the command channel at any time using an LIA or LIB instruction. Normally, status is only checked when the interface signals "ready" after an operation has been completed.

3-18. Local (Bit 0)

The local bit is high when the selected tape unit is in the local mode (under manual control only). When the local bit is low, the unit is under computer control.

3-19. Parity/Timing Error (Bit 1)

The parity/timing error bit is high if a vertical or longitudinal parity error is detected during a read, read-after-write, BSR, FSR, BSF, or FSF operation. This bit is also set if the data channel flag bit has not been cleared or the interrupt request has not been acknowledged within one data channel flag occurrence interval (refer to table 1-2) while reading or writing (timing error).

NOTE

During a read operation, if the record on the tape is larger than the available computer input buffer area, the data channel control bit should be cleared after the required number of words are transferred . This prevents setting bit 1 unless a parity error has occurred.

3-20. No Write Ring (Bit 2)

The no write ring (file protected) bit is high when the tape unit supply reel is not equipped with a write enable ring. The tape unit is write-enabled when this bit is low.

3-21. Reject (Bit 3)

The reject bit is set when one of the following conditions occurs at OTA/B time:

a. Tape motion is required but the tape unit or controller is busy.

b. BACKSPACE command (BSR or BSF) received, but tape is at beginning of tape (BOT).

c. Command requiring write current s received but no write ring is installed.

d. A SELECT TAPE UNIT command is given and the controller is busy.

TABLE 3-3. CONTROLLER STATUS WORD BITS

BIT	STATUS	BIT	STATUS
0	Local	6	Load Point
1	Parity/Timing Error	7	End of File
2	No Write Ring	8	Controller Busy
3	Reject	9	Transport Busy
4	Data Timing Error	10	Rewind
5	End of Tape	11	Odd Number of Bytes Read

NOTE

Under no circumstances should the STC,C be given if bit 3 is set since improper operation may result.

Because the reject bit is set at OTA/B time, it is necessary to load the status word and test this bit between OTA/B time and STC,C time. The reject bit is cleared by the next executable (non-rejectable) OTA/B command.

3-22. Data Timing Error (Bit 4)

The data timing error bit is high if, while in the read mode (RRF), the computer has not accepted a word by the time the next one is ready, or, while in the write mode (WCC), the computer has not output a output a word by the time the next one is required.

3-23. End of Tape (Bit 5)

The end-of-tape (EOT) bit is high when the EOT reflective marker passes under the tape unit photosense head while the tape is moving forward. The bit remains high until a REW or RWO command is given, a BSR or BSF command positions the EOT marker ahead of the photosense head, or another tape unit is selected which has not sensed the EOT marker. (The former tape unit will re-establish the EOT but after it is selected again.)

3-24. Load Point (Bit 6)

The beginning of tape (BOT) bit is high when the tape is at the load point, which is indicated when the tape load point marker (of the selected unit) is under the tape unit photo-sensor.

3-25. End of File (Bit 7)

The end-of-file (EOF) bit is set when the end-of-file mark (023 octal) is detected through the read circuits, while moving a record or file (FSR, BSR, FSF, BSF), while reading (RRF), or after writing the file mark (WFM, GFM).

3-26. Controller Busy (Bit 8)

The controller busy bit is set when the interface is executing a command. When the bit is low, the interface is ready to accept a new command.

3-27. Transport Busy (Bit 9)

The transport busy bit is high when the tape transport is busy, and low when the transport is ready to be used.

3-28. Rewind (Bit 10)

The rewind bit is high when the transport is rewinding and low when the transport is not rewinding. Rewind is still considered to be in operation while the tape moves forward to the load point following the actual rewind.

3-29. Odd Number of Bytes Read (Bit 11)

The odd number of bytes read bit is set if the previous record read or spaced over contains an odd number of data bytes.

NOTE

Since the controller always writes at least one computer word at a time (two tape bytes), this condition only occurs following a file mark for tapes written with this controller.

3-30. TYPICAL PROGRAMS

Tables 3-4 and 3-5 contain typical assembly language programs. The program in table 3-4 will transfer data from the tape unit to the computer (read) using the computer interrupt method. The program in table 3-5 transfers data from the computer to the tape unit (write) using the DMA method.

TABLE 3-4. ASSEMBLY LANGUAGE PROGRAM (READ) USING COMPUTER INTERRUPT SYSTEM

```
0001  00000                NAM SHOWN
0002                       ENT SHOWN
0003  00000          A     EQU 0
0004  00001          B     EQU 1
0005  00010          DATA  EQU 10B
0006  00011          CMND  EQU 11B
0007*
0008*     13181 CONTROLLER INTERRUPT BINARY READ OPERATION
0009*     CONTROLLER ASSUMED TO BE IN SLOTS 10,11
0010*
0011  00000                ORB           .BASE PAGE LINKAGE
0012  00000 000023R I.1    DEF I1        .DATA LINK (L1)
0013  00001 000035R C.1    DEF C1        .COMMAND LINK (L2)
0014  00000                ORR           .RELOCATIBLE PROGRAM
0015  00000 000000  SHOWN NOP
0016  00001 102100         STF 0         .TURN ON INTERRUPTS
0017  00002 062040R        LDA JSBL1
0018  00003 070010         STA DATA      .INTERRUPT LINK FOR DATA CHANNEL
0019  00004 062041R        LDA JSBL2
0020  00005 070011         STA CMND      .INTERRUPT LINK FOR CMND CHANNEL
0021  00006 062042R        LDA BUFAD
0022  00007 072043R        STA POINT     .SET BUFFER POINTER
0023  00010 062044R        LDA LBUF
0024  00011 072045R        STA COUNT     .SET BUFFER COUNTER
0025  00012 062046R        LDA READ      .READ COMMAND
0026  00013 102611  REJCT OTA CMND       .OUTPUT READ COMMAND TO CONTROLL
0027  00014 106511         LIB CMND      .TEST FOR REJECT
0028  00015 005323         RBR,RBR
0029  00016 005310         RBR,SLB       .REJECT?
0030  00017 026013R        JMP REJCT     .YES, KEEP TRYING
0031  00020 103711         STC CMND,C    .SET CMND CHANNEL
0032*     CONTROLLER STARTS TAPE MOTION
0033  00021 103710         STC DATA,C    .SET DATA CHANNEL
0034*
0035*     DATA TRANSFER WILL NOW TAKE PLACE
0036*     A JUMP SELF LOOP FOLLOWS
0037  00022 026022R        JMP *         .JUMP SELF UNTIL INTERRRUPT OCCURS
0038  00023 000000  I1     NOP           ..DATA TRANSFER ROUTINE
0039  00024 072047R        STA SAVA      .SAVE A REGISTER
0040  00025 103510         LIA DATA,C    .INPUT DATA FROM CONTROLLER
0041  00026 172043R        STA POINT,I   .STORE POINTER
0042  00027 036043R        ISZ POINT     .NEXT
0043  00030 062047R        LDA SAVA
0044  00031 036045R        ISZ COUNT     .DONE ?
0045  00032 126023R        JMP I1,I      .NO
0046  00033 106710         CLC DATA      .YES
0047  00034 126023R        JMP I1,I
0048  00035 000000  C1     NOP           .OPERATION COMPLETE ROUTINE
0049  00036 106711         CLC CMND      .TRANSFER DONE
0050  00037 102077         HLT 77B
0051*
0052*     PROGRAM SHOULD COME TO A HLT 77B
0053*
0054*     PROGRAM CONSTANTS
0055*
0056  00040 114000B JSBL1 JSB I.1,I
0057  00041 114001B JSBL2 JSB C.1,I
0058  00042 000050R BUFAD DEF BUFF
0059  00043 000000  POINT NOP
0060  00044 177634  LBUF  DEC -100
0061  00045 000000  COUNT NOP
0062  00046 000023  READ  OCT 23
0063  00047 000000  SAVA  NOP
0064  00050 000000  BUFF  BSS 124
0065                      END SHOWN
**   NO ERRORS*
```

TABLE 3-5. ASSEMBLY LANGUAGE PROGRAM (WRITE) USING DMA

```
0001  00000                NAM EXAMP
0002                       ENT EXAMP
0003  00010          DATA  EQU 10B
0004  00011          CMND  EQU 11B
0005*
0006*     13181 CONTROLLER DMA BINARY WRITE OPERATION
0007*     CONTROLLER ASSUMED TO BE IN SLOTS 10,11
0008*     DMA CHANNEL 6 IS USED
0009*
0010  00000                ORB           .BASE PAGE RELOCATIBLE
0011  00000 000030R LINK1  DEF COMPL     .CMND COMPLETE LINK
0012  00000                ORR           .RELOCATIBLE PROGRAM
0013  00000 000000  EXAMP  NOP
0014  00001 102100         STF 0         .TURN ON INTERRUPTS
0015  00002 062033R        LDA JSBL1
0016  00003 070011         STA 11B       .SET CMND TRAP CELL
0017  00004 062035R        LDA CLDMA      .TURN DMA OFF
0018  00005 070006         STA 6          .WHEN IT INTERRUPTS
0019  00006 062034R        LDA PWC
0020  00007 102606         OTA 6B        .SET DMA PROGRAM CONTROL WORD
0021  00010 106702         CLC 2B
0022  00011 062036R        LDA BUFF
0023  00012 102602         OTA 2B        .SET DMA BUFFER ADDRESS
0024  00013 102702         STC 2B
0025  00014 062233R        LDA LBUFF
0026  00015 102602         OTA 2B        .SET DMA BUFFER LENGTH
0027*
0028*     DMA IS NOW READY TO MAKE A WRITE TRANSFER
0029*
0030  00016 066234R        LDB WCC        .WRITE COMMAND
0031  00017 106611  REJCT  OTB CMND      .OUTPUT WRITE COMMAND TO CONTROLL
0032  00020 102511         LIA CMND       .TEST FOR REJECT
0033  00021 012235R        AND MASK2
0034  00022 002002         SZA            .REJECT?
0035  00023 026017R        JMP REJCT      .YES, KEEP TRYING
0036  00024 103711         STC CMND,C     .NO,SET CMND CHANNEL
0037*     CONTROLLER STARTS TAPE MOTION
0038  00025 103710         STC DATA,C    .SET DATA CHANNEL
0039  00026 103706         STC 6B,C      .START DMA
0040*
0041*     DATA TRANSFER WILL NOW TAKE PLACE
0042*      A JUMP SELF FOLLOWS
0043*
0044  00027 026027R        JMP *         .JUMP SELF UNTIL INTERRUPT OCCURS
0045  00030 000000  COMPL  NOP           .OPERATION COMPLETE
0046  00031 106711         CLC CMND
0047  00032 102077         HLT 77B
0048*
0049*     PROGRAM SHOULD COME TO A HALT 77B
0050*
0051*     PROGRAM CONSTANTS
0052*
0053  00033 114000B JSBL1  JSB LINK1,I
0054  00034 020010  PWC    OCT 20010
0055  00035 107706  CLDMA  CLC 6,C
0056  00036 000037R BUFF   DEF BUFF1
0057  00037 000000  BUFF1  BSS 124
0058  00233 177634  LBUFF  DEC -100
0059  00234 000031  WCC    OCT 31
0060  00235 000010  MASK2  OCT 10
0061                       END EXAMP
**  NO ERRORS*
```

SECTION IV
THEORY OF OPERATION

This section contains block diagrams and timing information for interface kit operations.

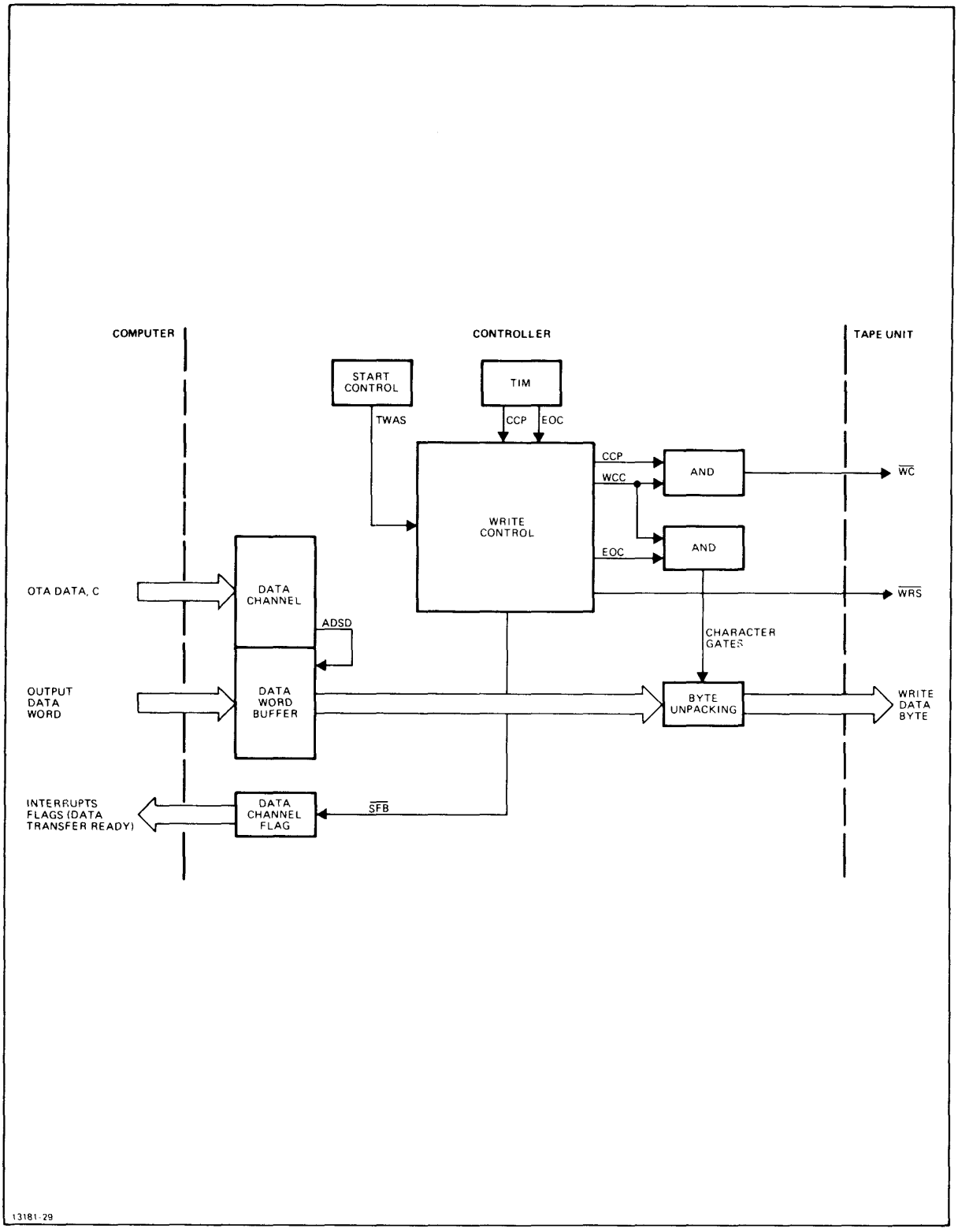


Figure 4-1. Write Data Control Block Diagram

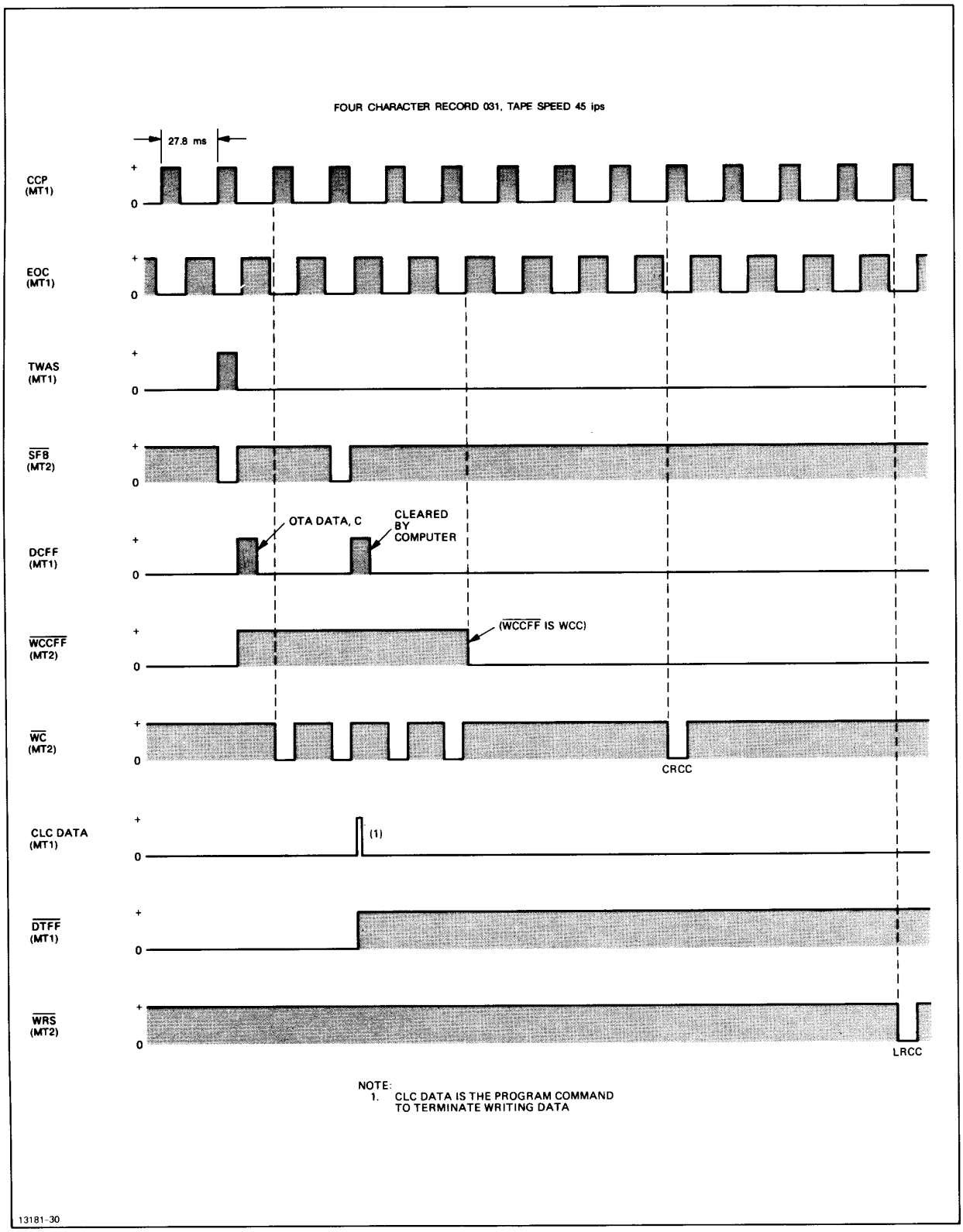


Figure 4-2. Write Data Control Timing Diagram

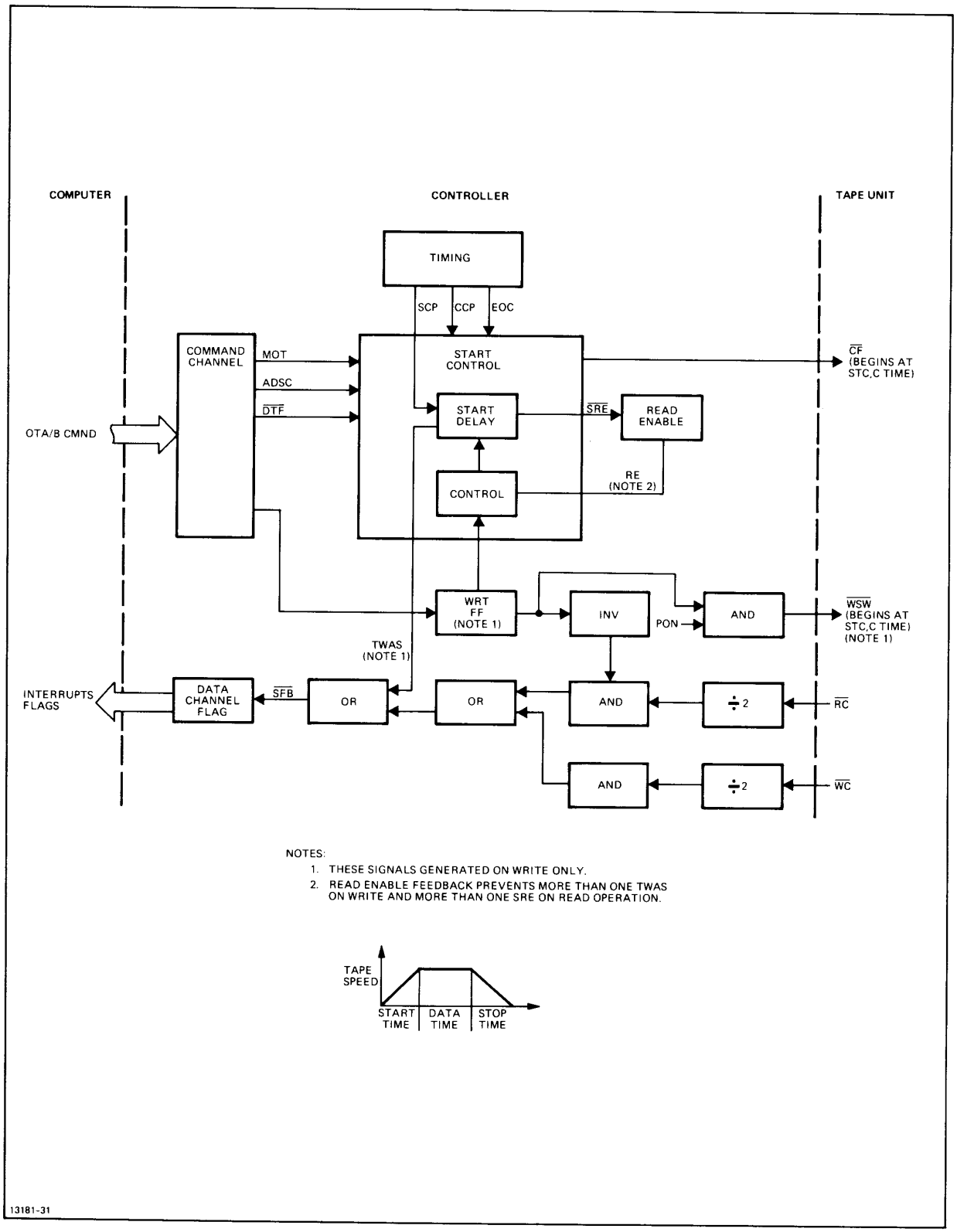


Figure 4-3. Start Data Operation Block Diagram

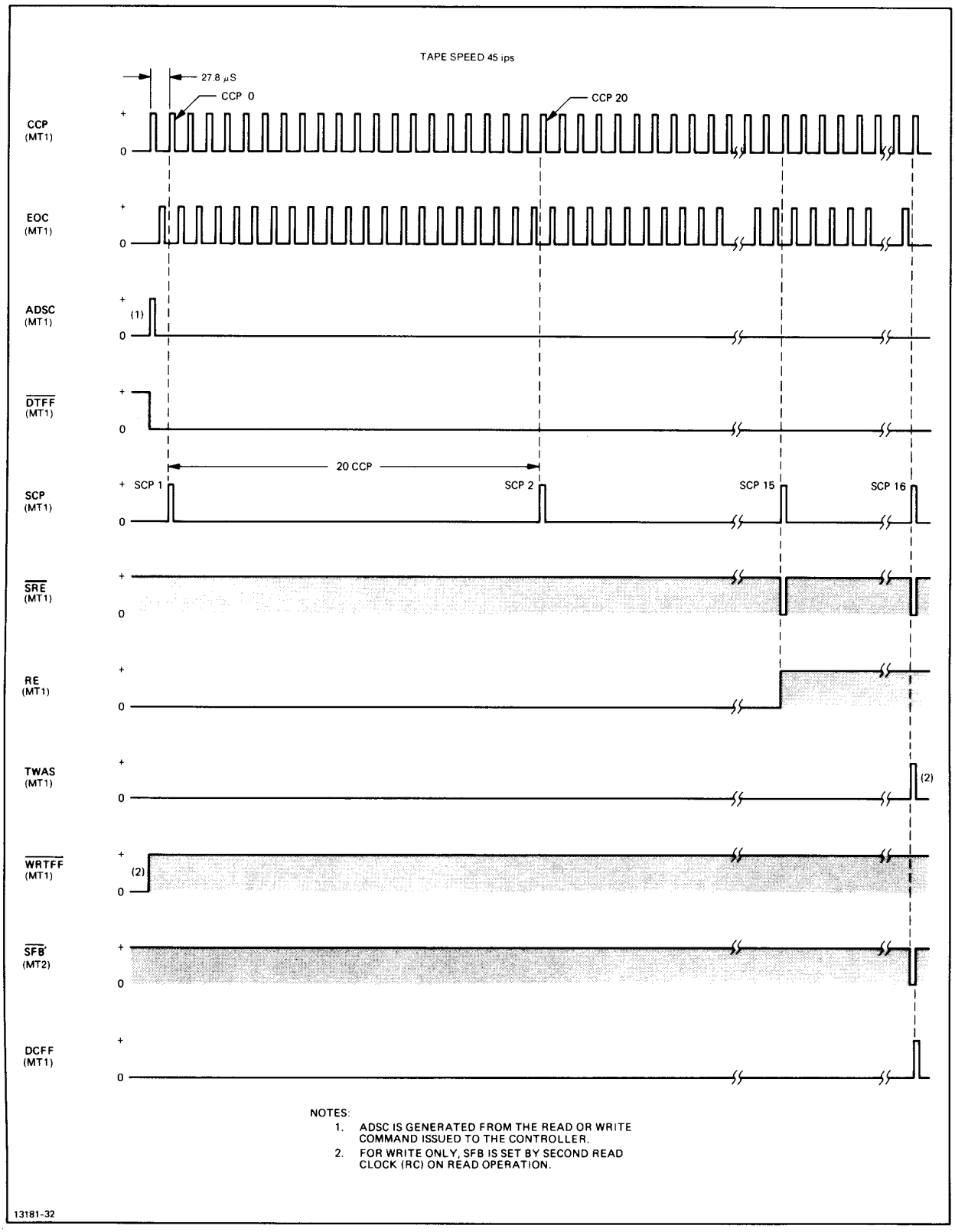


Figure 4-4. Start Data Operation Timing Diagram

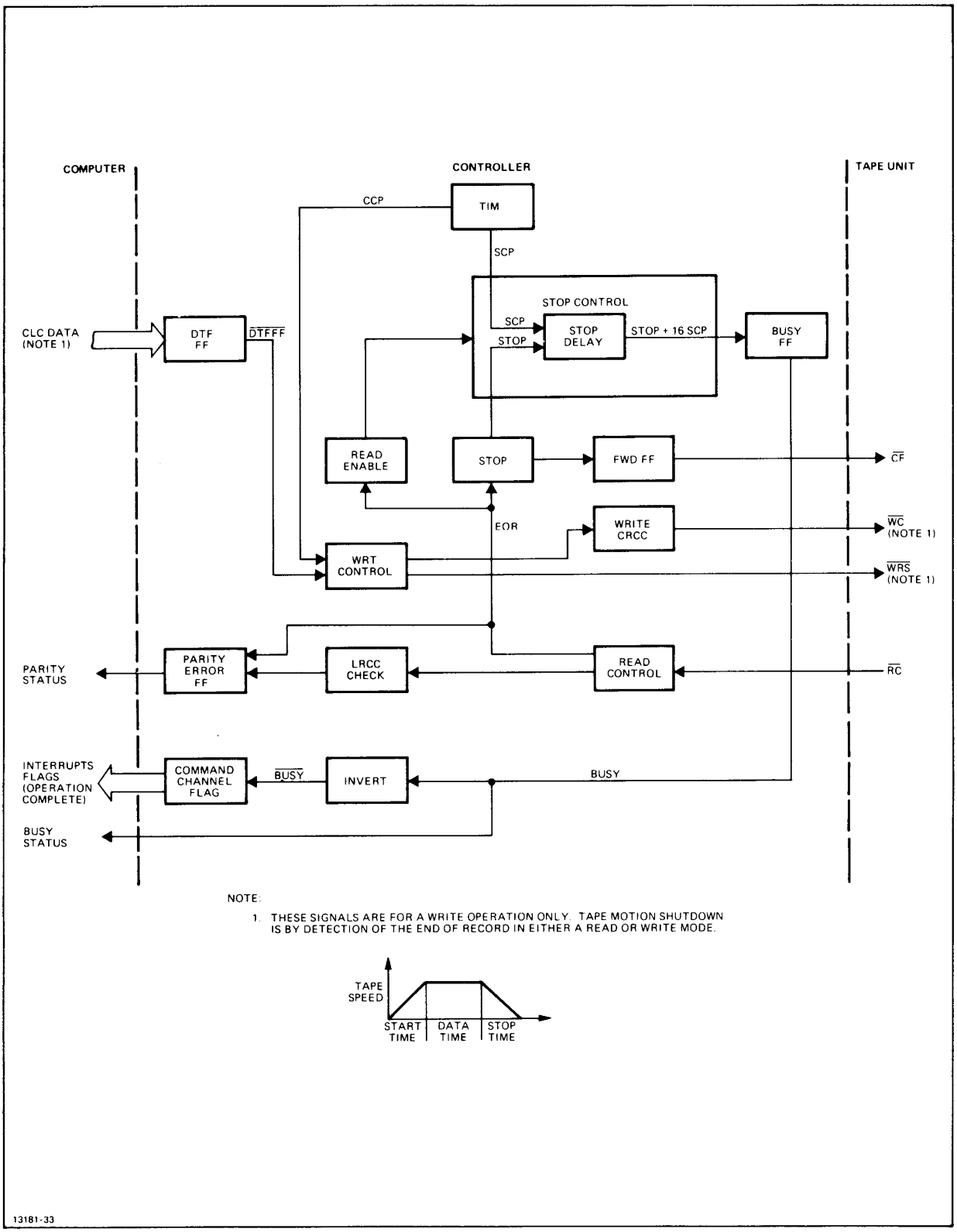


Figure 4-5. Stop Data Operation Block Diagram

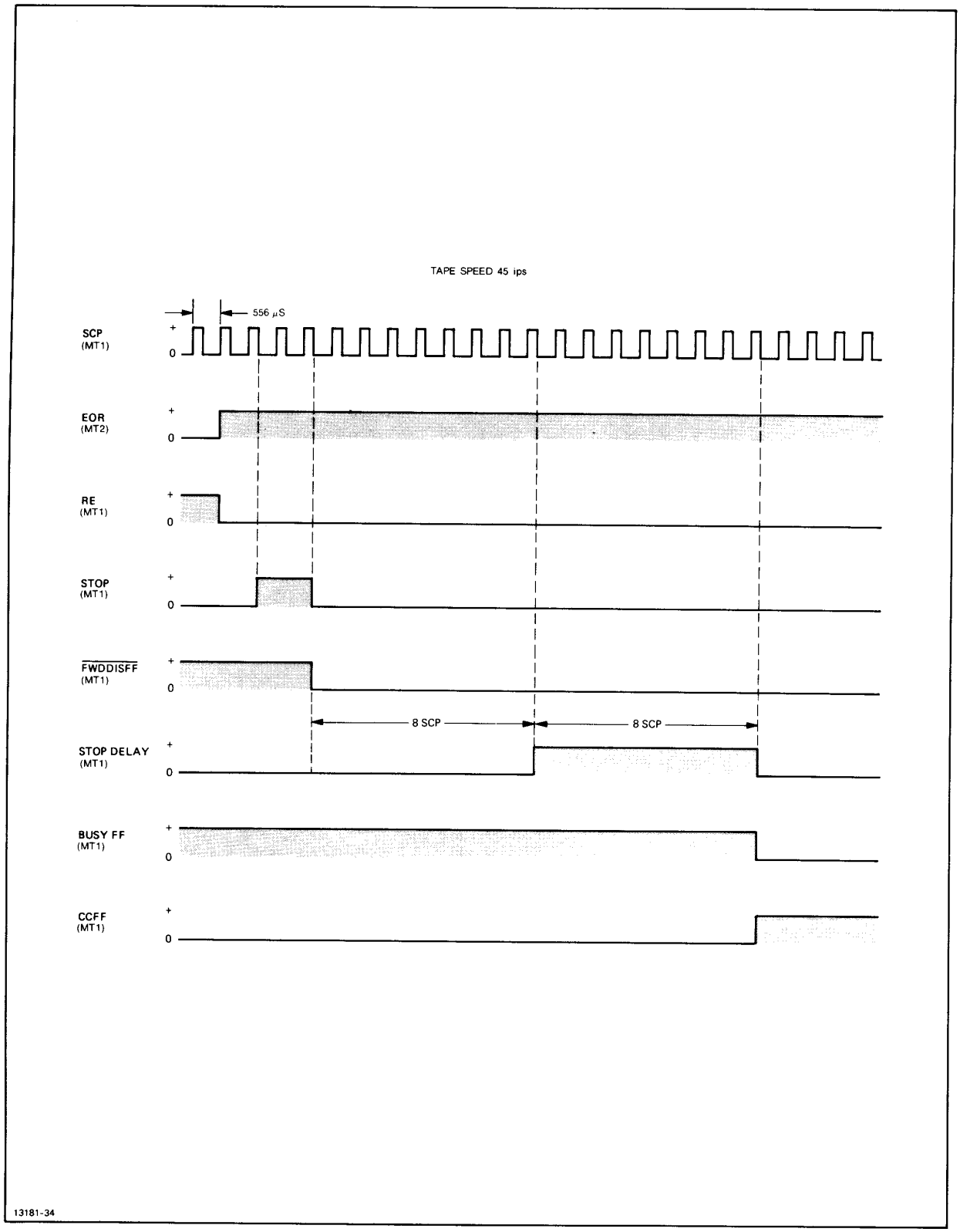


Figure 4-6. Stop Data Operation Timing Diagram

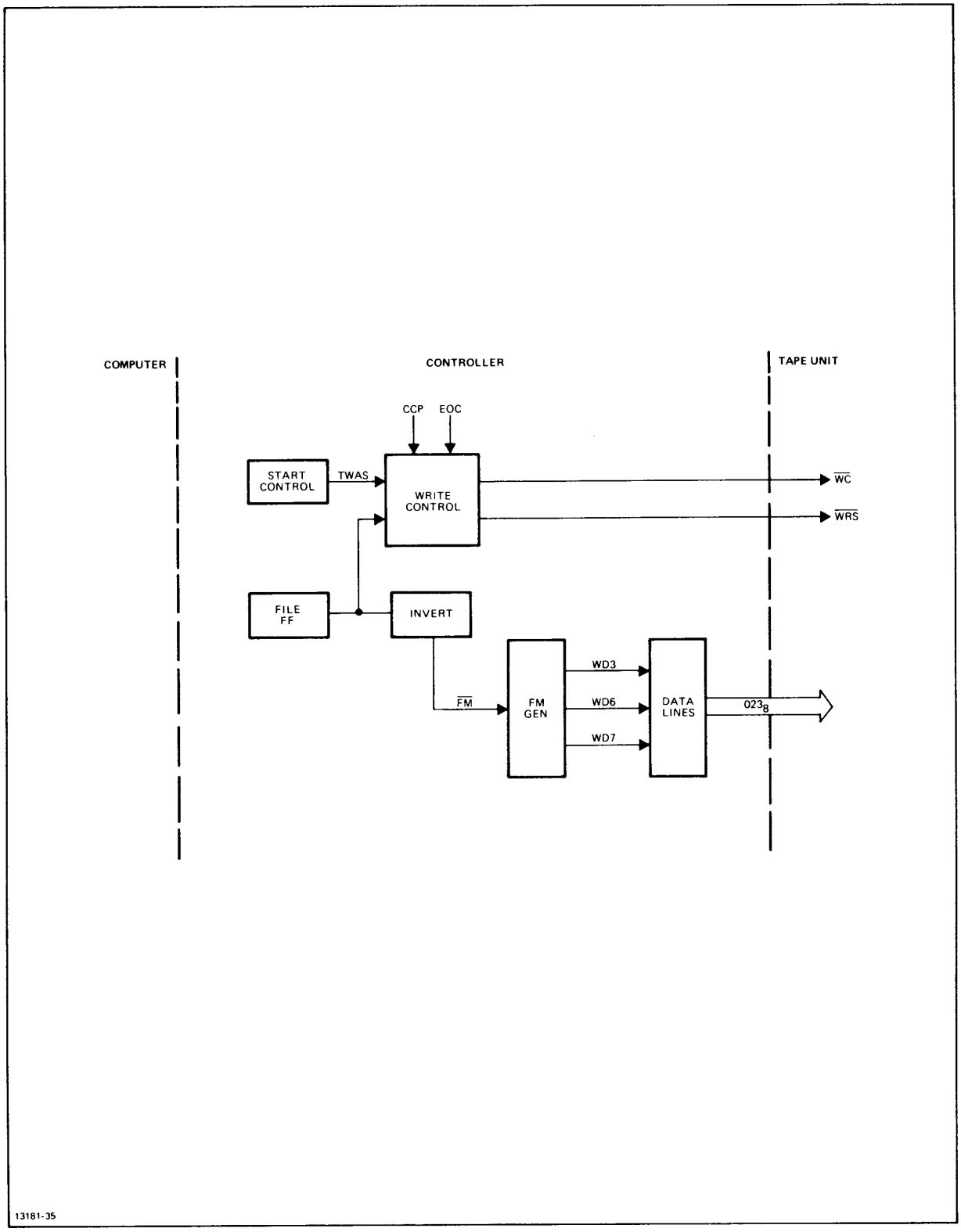


Figure 4-7. Write File Mark Block Diagram

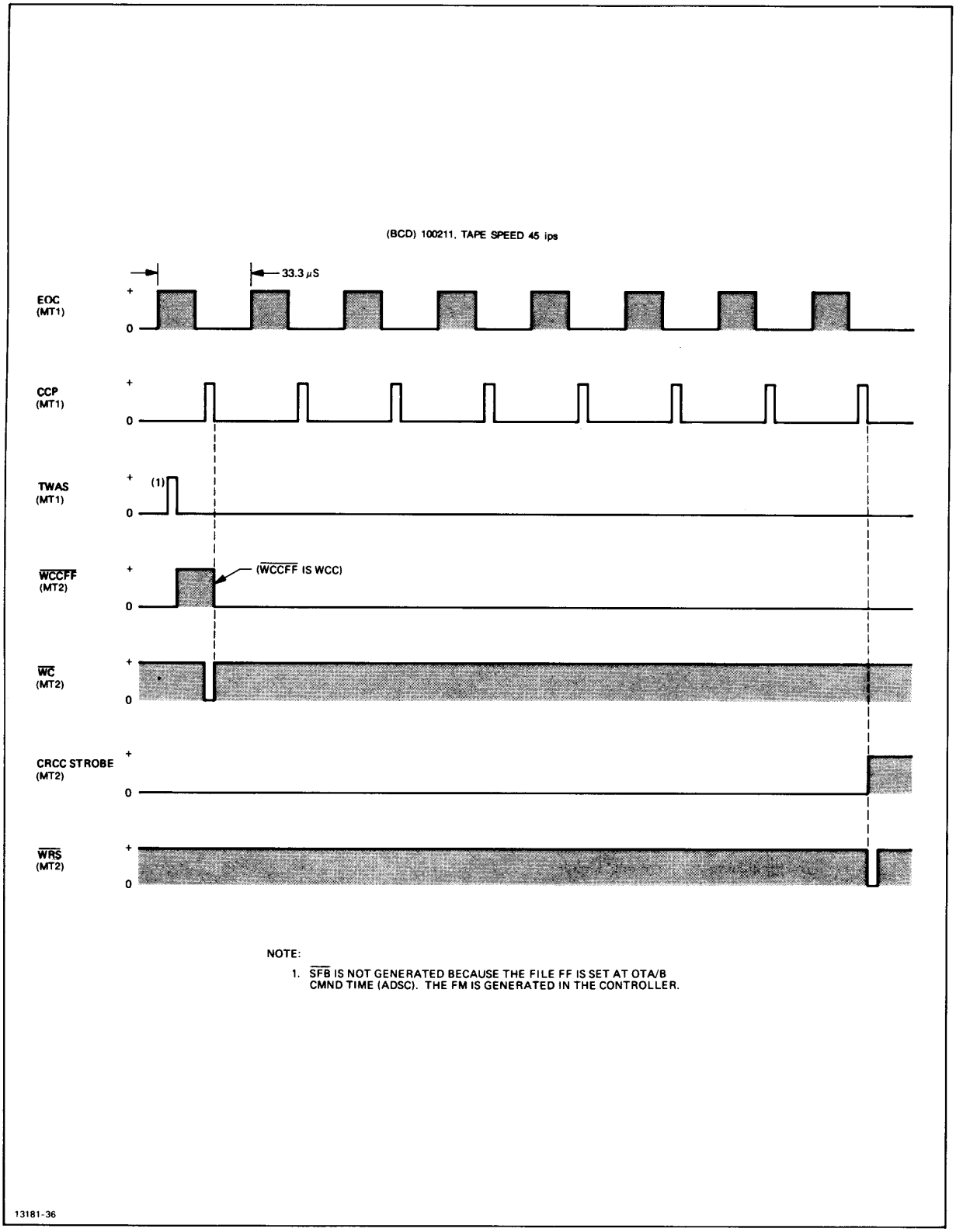


Figure 4-8. Write File Mark Timing Diagram

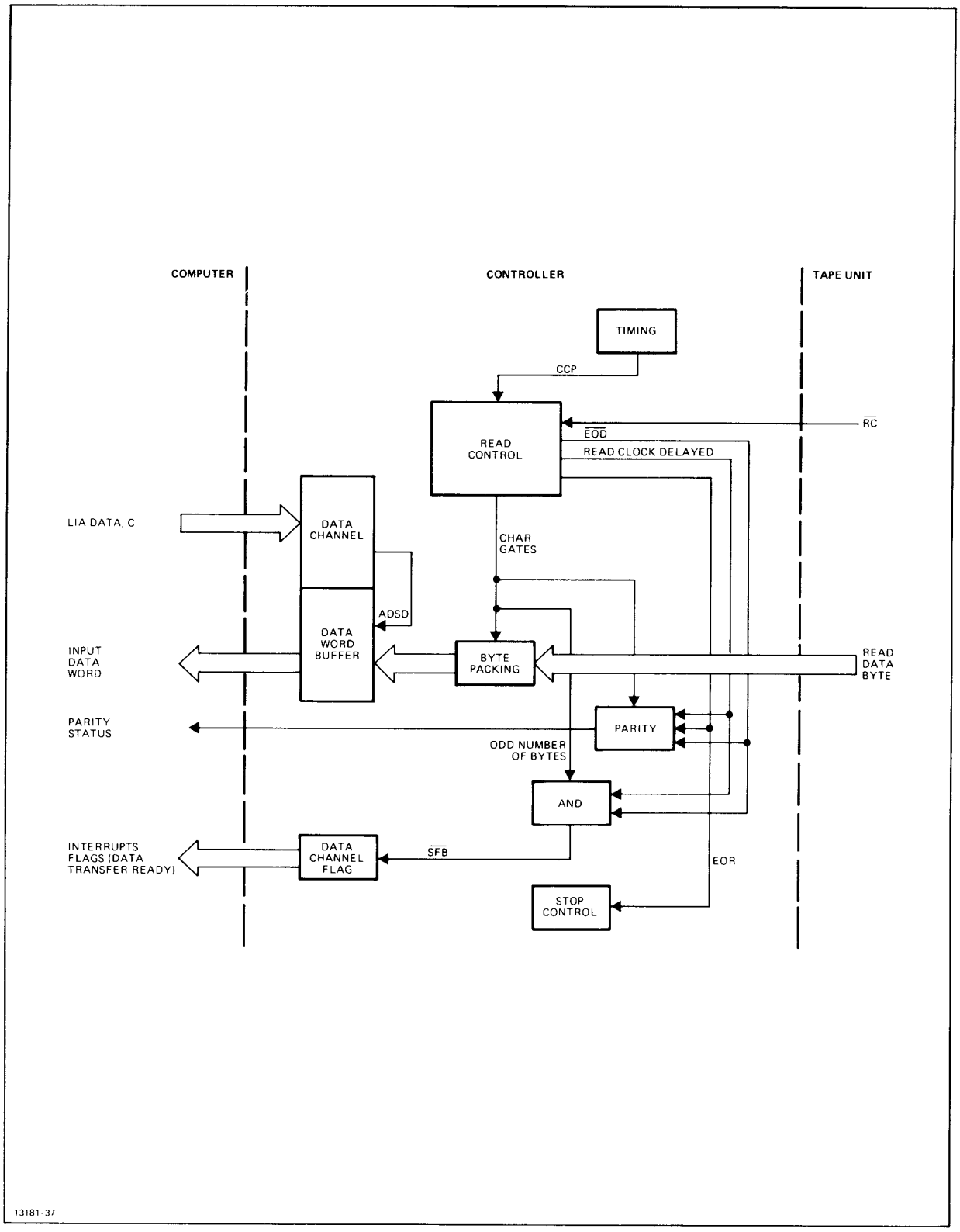
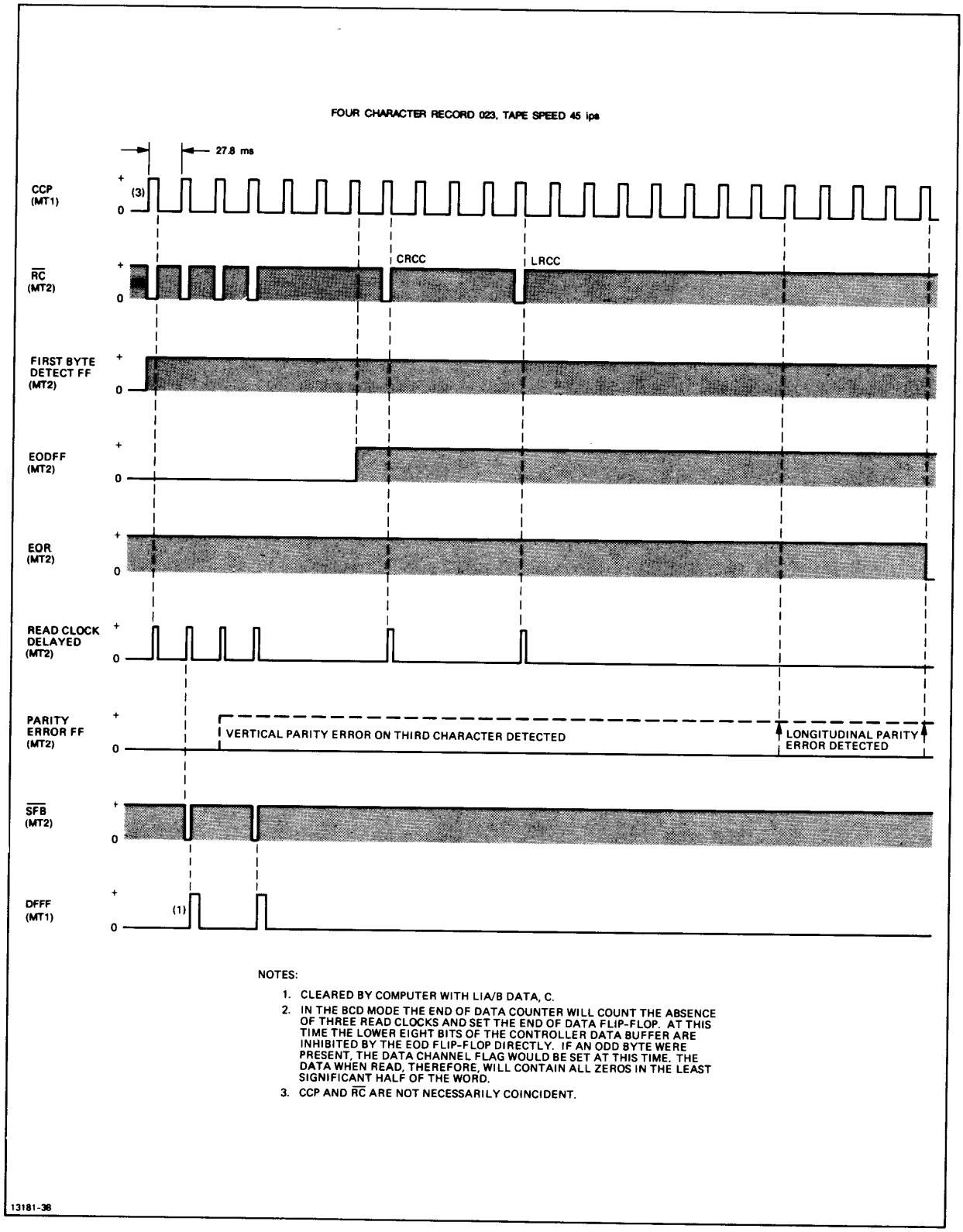


Figure 4-9. Read Data Control Block Diagram



NOTES:

1. CLEARED BY COMPUTER WITH LIA/B DATA, C.
2. IN THE BCD MODE THE END OF DATA COUNTER WILL COUNT THE ABSENCE OF THREE READ CLOCKS AND SET THE END OF DATA FLIP-FLOP. AT THIS TIME THE LOWER EIGHT BITS OF THE CONTROLLER DATA BUFFER ARE INHIBITED BY THE EOD FLIP-FLOP DIRECTLY. IF AN ODD BYTE WERE PRESENT, THE DATA CHANNEL FLAG WOULD BE SET AT THIS TIME. THE DATA WHEN READ, THEREFORE, WILL CONTAIN ALL ZEROS IN THE LEAST SIGNIFICANT HALF OF THE WORD.
3. CCP AND $\overline{RC}$ ARE NOT NECESSARILY COINCIDENT.

Figure 4-10. Read Data Control Timing Diagram

SECTION V
MAINTENANCE

5-1. INTRODUCTION

This section contains maintenance information for the tape unit interface kit.

5-2. PREVENTIVE MAINTENANCE

Detailed preventive maintenance procedures and schedules are provided in the HP computer documentation for the computer. There are no separate preventive maintenance procedures for the interface kit.

5-3. DIAGNOSTICS

Procedures for running the interface kit diagnostic test are contained in the Diagnostic Program Procedure section of the *Diagnostic Manual*, part number 13181-90095. The diagnostic test should be run after installation of the interface kit and periodically as a confidence check of the system operation.

5-4. TROUBLESHOOTING

Toubleshooting for the interface assemblies is accomplished by performing the diagnostic test (paragraph 5-3) and analyzing the error halts that occur as the test is being run. To further isolate the trouble, refer to the schematic and parts location diagrams in figures 5-2 thru 5-5.

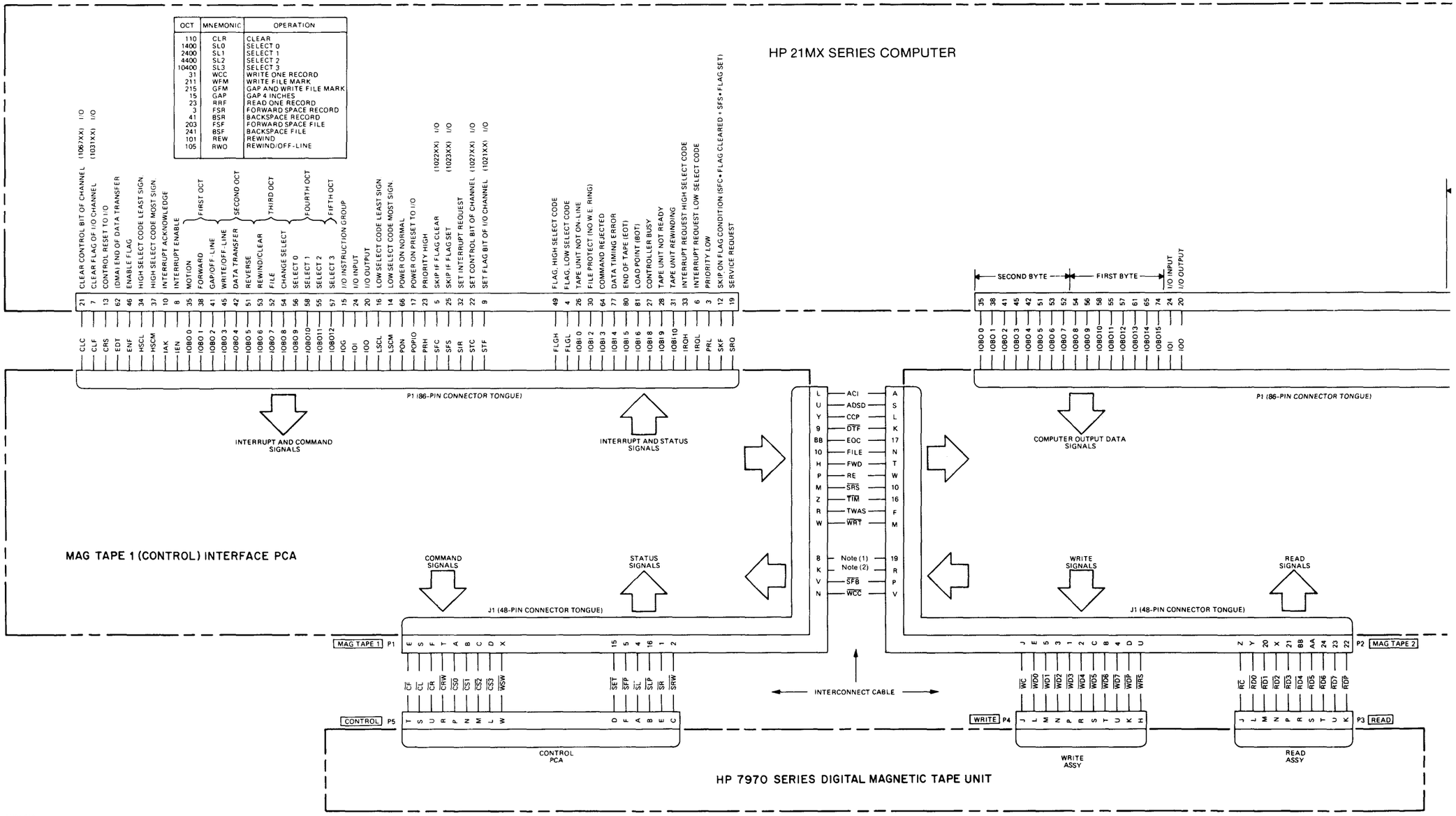
Figure 5-1 is the interconnection diagram for the tape unit to computer interface. Tables 5-1 and 5-2 list mnemonic definitions for the tape unit and controller, respectively.

TABLE 5-1. TAPE UNIT MNEMONICS

MNEMONIC	DEFINITION	MNEMONIC	DEFINITION
CF	Forward Command	SL	On-Line Status
CL	Off-Line Command	SLP	Load Point Status
CR	Reverse Command	SR	Ready Status
CRW	Rewind Command	SRW	Rewind Status
CS0-CS3	Select Unit 0 thru 3	WC	Write Clock
RC	Read Clock	WDP	Write Data, Channel P
RDP	Read Data, Channel P	WD0	Write Data, Channel 0
RD0	Read Data, Channel 0	WD1	Write Data, Channel 1
RD1	Read Data, Channel 1	WD2	Write Data, Channel 2
RD2	Read Data, Channel 2	WD3	Write Data, Channel 3
RD3	Read Data, Channel 3	WD4	Write Data, Channel 4
RD4	Read Data, Channel 4	WD5	Write Data, Channel 5
RD5	Read Data, Channel 5	WD6	Write Data, Channel 6
RD6	Read Data, Channel 6	WD7	Write Data, Channel 7
RD7	Read Data, Channel 7	WRS	Write Reset
SET	End-of-Tape Status	WSW	Set Write Command
SFP	File Protect Status		

TABLE 5-2. CONTROLLER MNEMONICS

MNEMONIC	DEFINITION	MNEMONIC	DEFINITION
ACI	Address Command Input	RC	Read Clock
ADSC	Address Command Channel	RE	Read Enable
ADSD	Address Data Channel	REV	Reverse
BOT	Beginning of Tape (Load Point)	SCP	Spacing Clock Pulse
CCP	Control Clock Pulse	SFB	Set Flag Buffer
CLR	Clear (Controller)	SRE	Set Read Enable
DTF	Data Transfer Latch	SRS	Start Reset
DFL	Data Flag	TIM	Timing Error
EOC	Even-Odd Clock	TWAS	Time, Write After Start
EOR	End-of-Record	WCC	Write Character Command
FM	File Mark	WFM	Write File Mark
FWD	Forward	WRS	Write Reset
LRC	Longitudinal Redundancy Character	WRT	Write
		FILE	File Operation


HP 21MX SERIES COMPUTER
OCT | MNEMONIC | OPERATION
110 CLR CLEAR
1400 SL0 SELECT 0
2400 SL1 SELECT 1
4400 SL2 SELECT 2
10400 SL3 SELECT 3
31 WCC WRITE ONE RECORD
211 WFM WRITE FILE MARK
215 GFM GAP AND WRITE FILE MARK
15 GAP GAP 4 INCHES
23 RRF READ ONE RECORD
3 FSR FORWARD SPACE RECORD
41 BSR BACKSPACE RECORD
203 FSF FORWARD SPACE FILE
241 BSF BACKSPACE FILE
101 REW REWIND
105 RWO REWIND/OFF-LINE
CLC 21 CLEAR CONTROL BIT OF CHANNEL (106?XX) I/O
CLF 7 CLEAR FLAG OF I/O CHANNEL (103?XX) I/O
CRS 13 CONTROL RESET TO I/O
EDT 62 (DMA) END OF DATA TRANSFER
ENF 46 ENABLE FLAG
HSCL 34 HIGH SELECT CODE LEAST SIGN.
HSCM 37 HIGH SELECT CODE MOST SIGN.
IAK 10 INTERRUPT ACKNOWLEDGE
IEN 8 INTERRUPT ENABLE
IOBO 0 35 MOTION FIRST OCT
IOBO 1 38 FORWARD
IOBO 2 41 GAP/OFF-LINE
IOBO 3 45 WRITE/OFF-LINE
IOBO 4 42 DATA TRANSFER SECOND OCT
IOBO 5 51 REVERSE
IOBO 6 53 REWIND/CLEAR THIRD OCT
IOBO 7 52 FILE
IOBO 8 54 CHANGE SELECT
IOBO 9 56 SELECT 0
IOBO10 58 SELECT 1 FOURTH OCT
IOBO11 55 SELECT 2
IOBO12 57 SELECT 3 FIFTH OCT
IOG 15 I/O INSTRUCTION GROUP
IOI 24 I/O INPUT
IOO 20 I/O OUTPUT
LSCL 16 LOW SELECT CODE LEAST SIGN.
LSCM 14 LOW SELECT CODE MOST SIGN.
PON 66 POWER ON NORMAL
POPIO 17 POWER ON PRESET TO I/O
PRH 23 PRIORITY HIGH
SFC 5 SKIP IF FLAG CLEAR (1022XX) I/O
SFS 25 SKIP IF FLAG SET (1023XX) I/O
SIR 32 SET INTERRUPT REQUEST
STC 22 SET CONTROL BIT OF CHANNEL (1027XX) I/O
STF 9 SET FLAG BIT OF I/O CHANNEL (1021XX) I/O
FLGH 49 FLAG, HIGH SELECT CODE
FLGL 4 FLAG, LOW SELECT CODE
IOBI 0 26 TAPE UNIT NOT ON-LINE
IOBI 2 30 FILE PROTECT (NO W.E. RING)
IOBI 3 64 COMMAND REJECTED
IOBI 4 77 DATA TIMING ERROR
IOBI 5 80 END OF TAPE (EOT)
IOBI 6 81 LOAD POINT (BOT)
IOBI 8 27 CONTROLLER BUSY
IOBI 9 28 TAPE UNIT NOT READY
IOBI10 31 TAPE UNIT REWINDING
IRQH 33 INTERRUPT REQUEST HIGH SELECT CODE
IRQL 6 INTERRUPT REQUEST LOW SELECT CODE
PRL 3 PRIORITY LOW
SKF 12 SKIP ON FLAG CONDITION (SFC • FLAG CLEARED + SFS • FLAG SET)
SRQ 19 SERVICE REQUEST
SECOND BYTE
FIRST BYTE
IOBO 0 35
IOBO 1 38
IOBO 2 41
IOBO 3 45
IOBO 4 42
IOBO 5 51
IOBO 6 53
IOBO 7 52
IOBO 8 54
IOBO 9 56
IOBO10 58
IOBO11 55
IOBO12 57
IOBO13 61
IOBO14 65
IOBO15 74
IOI 24 I/O INPUT
IOO 20 I/O OUTPUT
P1 (86-PIN CONNECTOR TONGUE)
INTERRUPT AND COMMAND SIGNALS
INTERRUPT AND STATUS SIGNALS
COMPUTER OUTPUT DATA SIGNALS
P1 (86-PIN CONNECTOR TONGUE)
MAG TAPE 1 (CONTROL) INTERFACE PCA
L ACI A
U ADSD S
Y CCP L
9 DTF K
BB EOC 17
10 FILE N
H FWD T
P RE W
M SRS 10
Z TIM 16
R TWAS F
W WRT M
8 Note (1) 19
K Note (2) R
V SFB P
N WCC V
COMMAND SIGNALS
STATUS SIGNALS
WRITE SIGNALS
READ SIGNALS
J1 (48-PIN CONNECTOR TONGUE)
J1 (48-PIN CONNECTOR TONGUE)
MAG TAPE 1 P1
E S F T A B C D X
15 5 4 16 1 2
CF CL CR CRW CS0 CS1 CS2 CS3 WSW
SET SFB SL SLP SIR SFRW
INTERCONNECT CABLE
J E 5 3 1 2 C B 4 D U
Z Y 20 X 21 BB AA 24 23 22 P2 MAG TAPE 2
WC WD0 WD1 WD2 WD3 WD4 WD5 WD6 WD7 WDP WRS
RC RD0 RD1 RD2 RD3 RD4 RD5 RD6 RD7 RDP
CONTROL P5
T S U R P N M L W
D F A B E C
WRITE P4
J L M N P R S T U K H
J L M N P R S T U K P3 READ
CONTROL PCA
WRITE ASSY
READ ASSY
HP 7970 SERIES DIGITAL MAGNETIC TAPE UNIT
13181-21A

F

OCT	MNEMONIC	OPERATION
110	CLR	CLEAR
1400	SL0	SELECT 0
2400	SL1	SELECT 1
4400	SL2	SELECT 2
10400	SL3	SELECT 3
31	WCC	WRITE ONE RECORD
211	WFM	WRITE FILE MARK
215	GFM	GAP AND WRITE FILE MARK
15	GAP	GAP 4 INCHES
23	RRF	READ ONE RECORD
3	FSR	FORWARD SPACE RECORD
41	BSR	BACKSPACE RECORD
203	FSF	FORWARD SPACE FILE
241	BSF	BACKSPACE FILE
101	REW	REWIND
105	RWO	REWIND/OFF-LINE

HP 21MX SERIES COMPUTER

P1 (86-PIN CONNECTOR TONGUE)

INTERRUPT AND COMMAND SIGNALS

INTERRUPT AND STATUS SIGNALS

P1 (86-PIN CONNECTOR TONGUE)

COMPUTER OUTPUT DATA SIGNALS

COMPUTER INPUT DATA SIGNALS

NTROL) INTERFACE PCA

COMMAND SIGNALS

STATUS SIGNALS

J1 (48-PIN CONNECTOR TONGUE)

WRITE SIGNALS

READ SIGNALS

J1 (48-PIN CONNECTOR TONGUE)

MAG TAPE 2 (DATA) INTERFACE PCA

INTERCONNECT CABLE

CONTROL PCA

WRITE ASSY

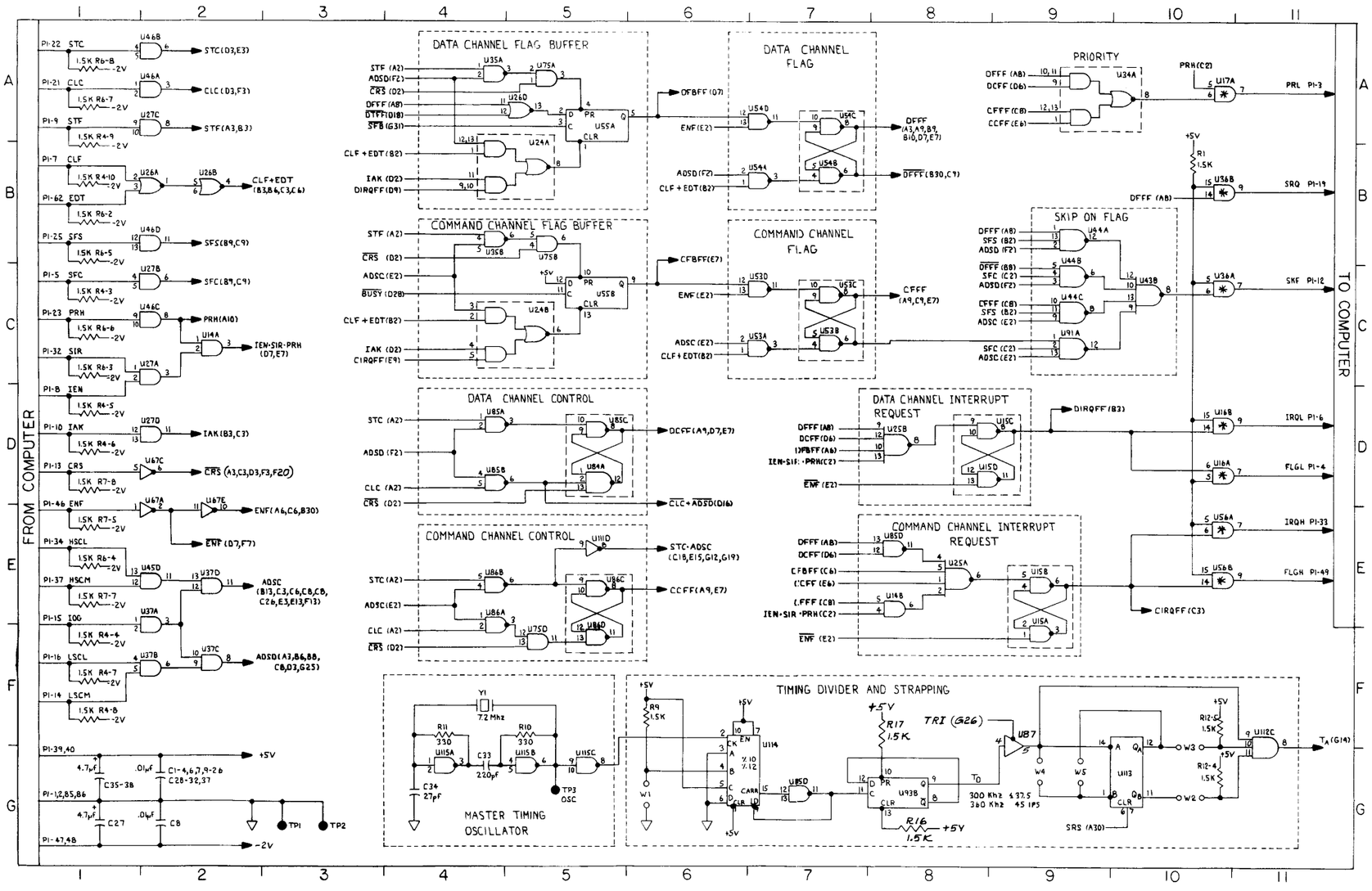
READ ASSY

HP 7970 SERIES DIGITAL MAGNETIC TAPE UNIT

Note: (1) TIM Error EN

Note: (2) (EOR + FILE) (FM + FILE)

Figure 5-1. Interface Kit Interconnection Diagram



TAPE SPEED (IPS)	T_A (KHZ)	JUMPER POSITIONS W1	W2	W3	W4	W5
45	180			▨		
37.5	150	▨				
25	100	▨	▨		▨	
12.5	50	▨	▨	▨		▨

▨ JUMPER INSTALLED

Figure 5-2. Mag Tape 1 PCA Schematic Diagram (1 of 3)

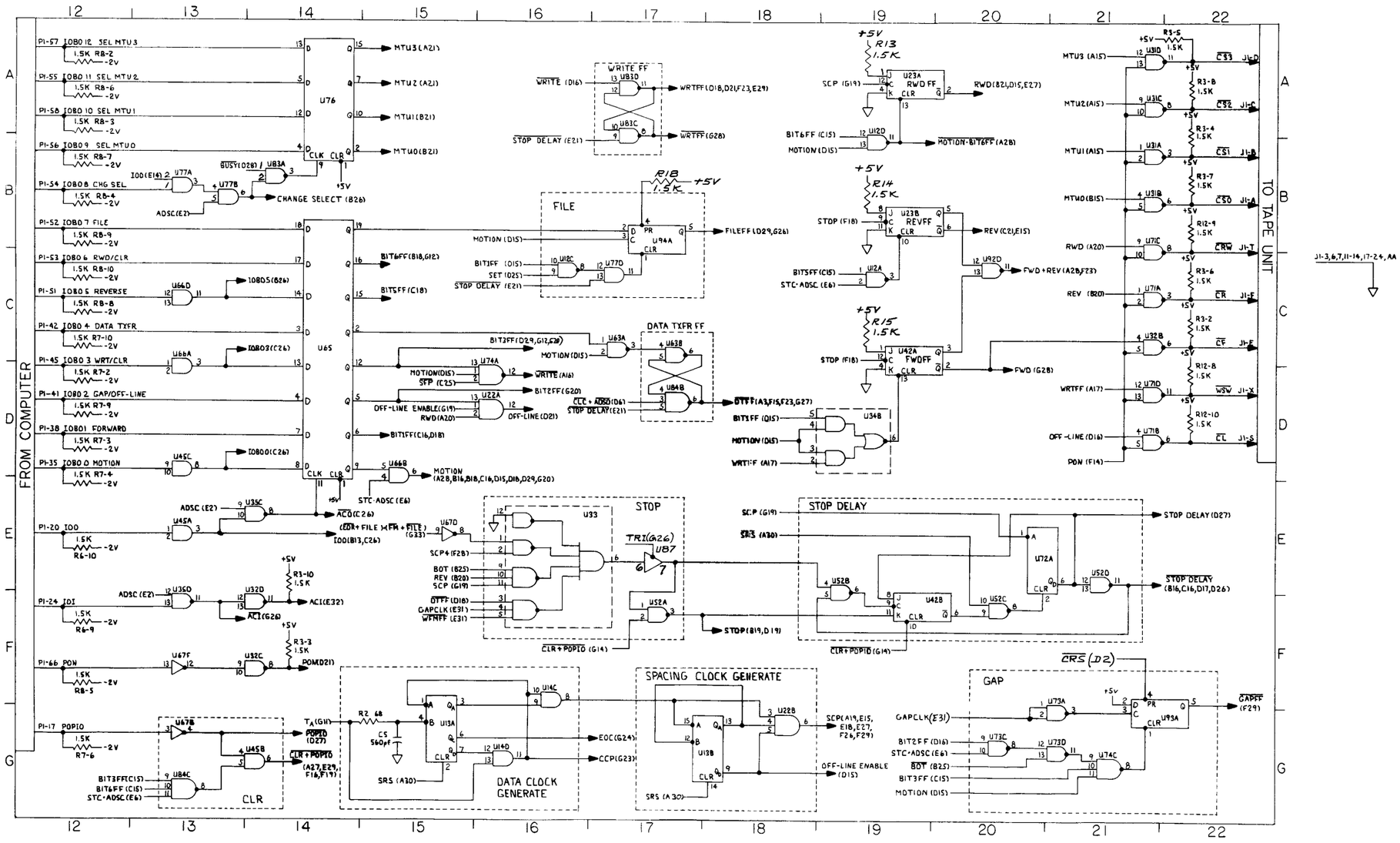


Figure 5-2. Mag Tape 1 PCA Schematic Diagram (2 of 3)

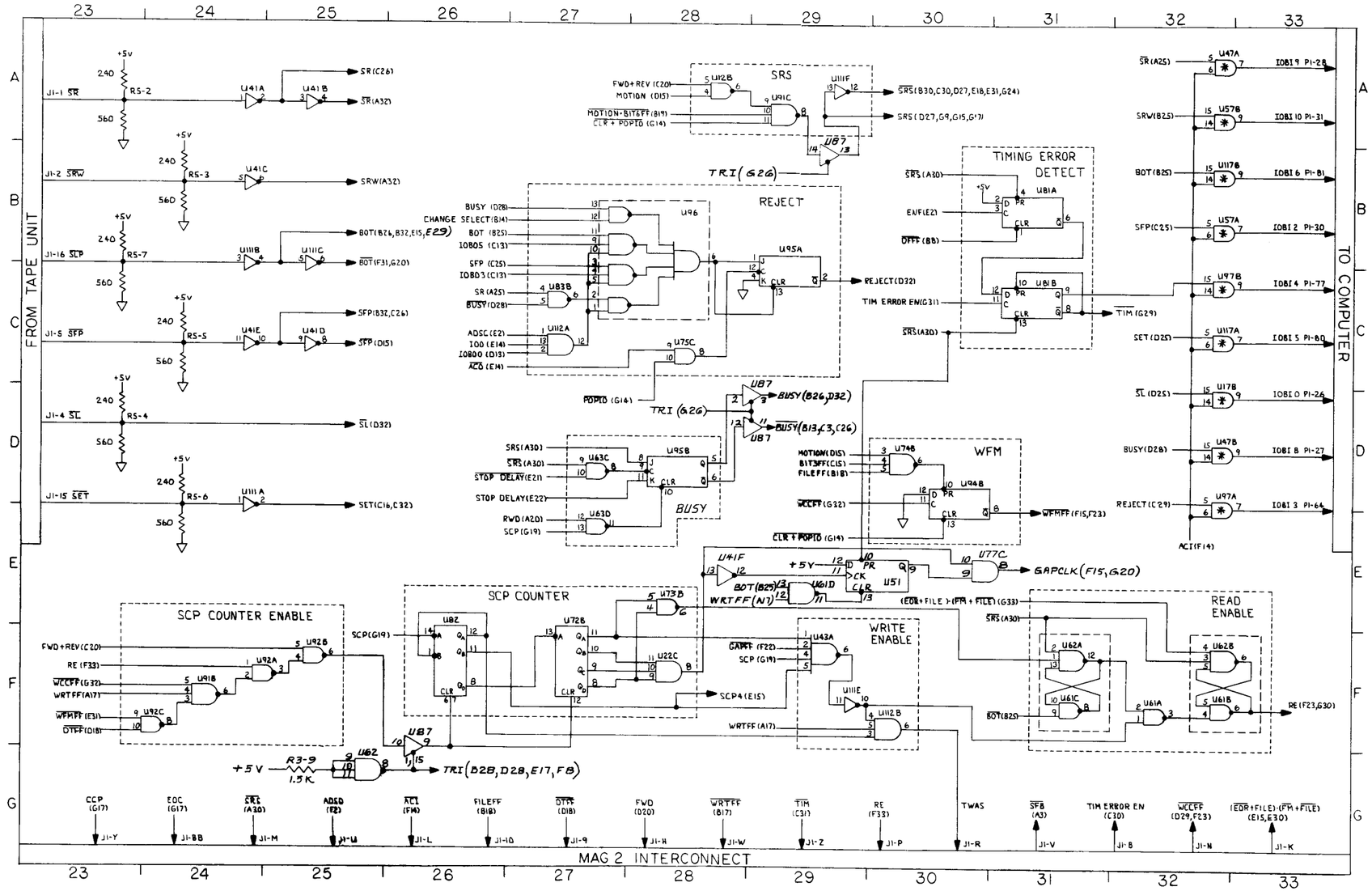


Figure 5-2. Mag Tape 1 PCA Schematic Diagram (3 of 3)

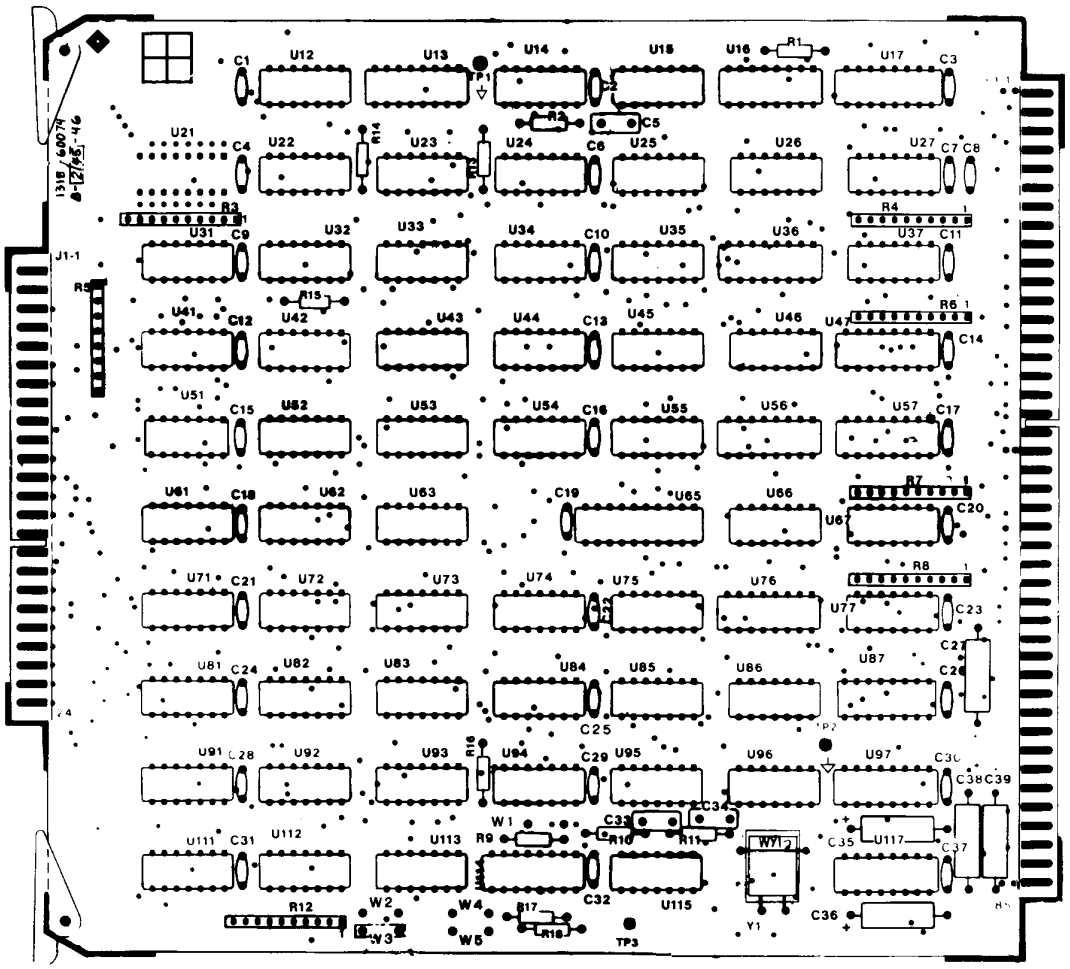


Figure 5-3. Mag Tape 1 PCA Parts Location Diagram

TABLE 5-3. MAG TAPE 1 PCA REPLACEABLE PARTS

REFERENCE DESIGNATION	DESCRIPTION	PART NUMBER
	MAG TAPE 1 PCA	13181-60074
C1 thru C4 C6 thru C26 C28 thru C32 C37	CAPACITOR: Fixed .01 μF	0160-2055
C5	CAPACITOR: Fixed	0160-3535
C27, C35, C36, C38, C39	CAPACITOR: Fixed 4.7 μF	0180-0100
C33	CAPACITOR: Fixed 220 pF	0160-0134
C34	CAPACITOR: Fixed 27 pF	0160-2306
R1, R9, R13 thru R18	RESISTOR: Fixed 1.5K	0683-1525
R2	RESISTOR: Fixed 68 Ω	0683-6805
R3, R4, R6 thru R8, R12	RESISTOR: 1.5K pack	1810-0276
R5	RESISTOR: Network	1810-0127
R10, R11	RESISTOR: Fixed 330 Ω	0683-3315
U12, U15, U35, U52 thru U54, U61, U63, U73 U83, U85, U86, U92, U115	IC: SN74LS00N	1820-1197
U13	IC: 74LS390N	1820-1991
U14, U27, U37, U45, U46, U66, U75, U77	IC: DGTL: GATE 7408	1820-0511
U16, U17, U36, U47, U56, U57, U97, U117	IC: SN75121N DRVR	1820-1080
U22, U112	IC: SN74LS11	1820-1203
U23, U42, U95	IC: SN74107N	1820-0281
U24, U34	IC: SN74LS51N	1820-1210

TABLE 5-3. MAG TAPE 1 PCA REPLACEABLE PARTS (Continued)

REFERENCE DESIGNATION	DESCRIPTION	PART NUMBER
U25, U43	IC: SN74LS20N	1820-1204
U26	IC: DGTL GATE 7402	1820-0328
U31, U32, U71	IC: SN7438N	1820-0621
U33, U96	IC: 74LS54	1820-1285
U41, U67, U111	IC: DGTL INV 7404	1820-0174
U44, U62, U74 U84, U91	IC: SN74LS10N	1820-1202
U51, U55, U81, U93, U94	IC: SN74LS74N	1820-1112
U65	IC: Digital	1820-1461
U72	IC: SN74LS393N	1820-2096
U76	IC: DGTL FF 74175	1820-0839
U82, U113	IC: 74LS92N	1820-1420
U114	IC: SN74LS161N	1820-1430
W3	JUMPER	1258-0124
WY1	WR24G: Bare	8151-0014
Y1	CRYSTAL: 7.2 MHz	0410-0449
	PC EXTRACTOR: LWR	13181-40005
	PC EXTRACTOR: UPR	13181-40006
U87	IC: SN74LS367AN	1820-1491

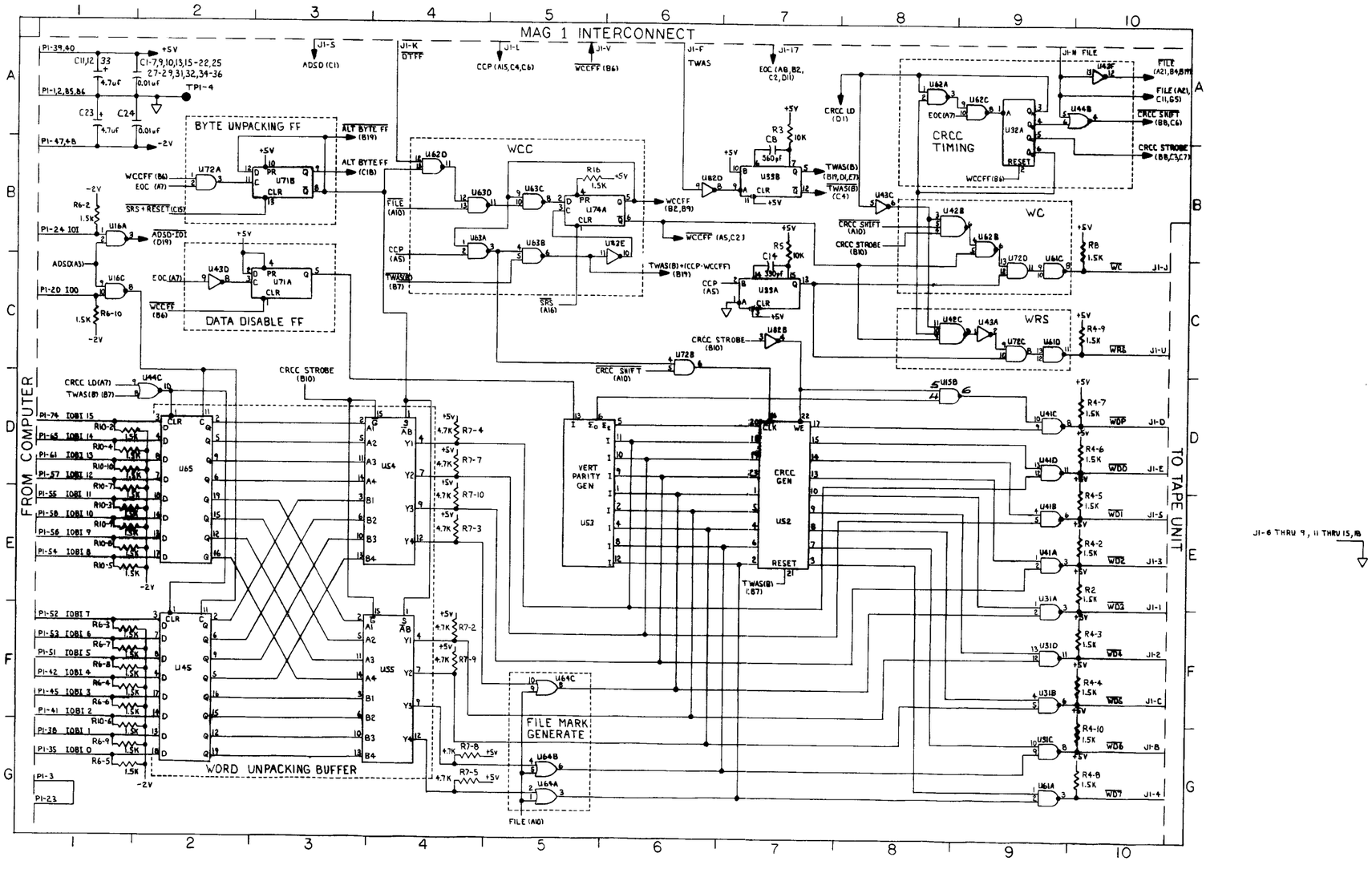


Figure 5-4. Mag Tape 2 PCA Schematic Diagram (1 of 2)

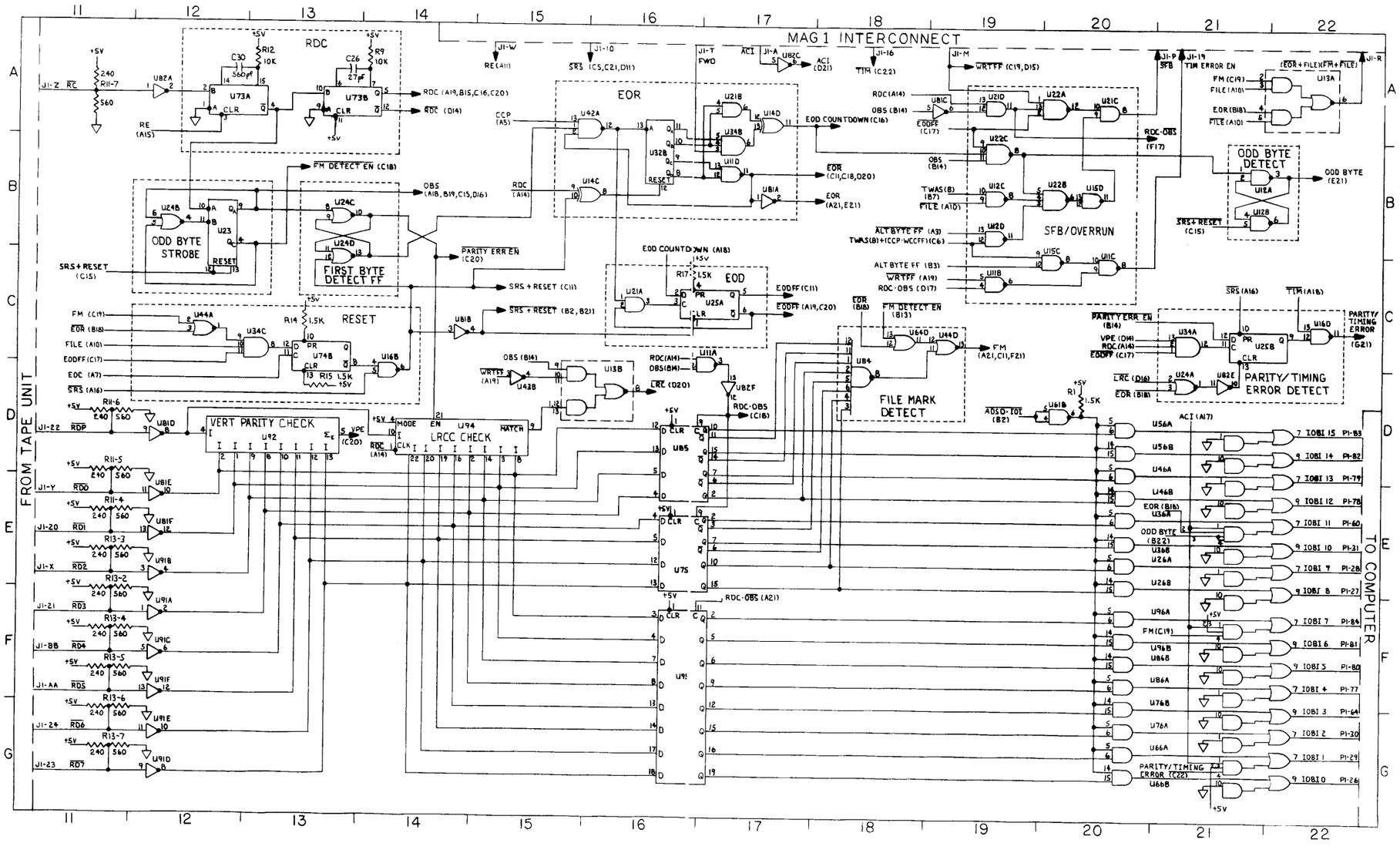


Figure 5-4. Mag Tape 2 PCA Schematic Diagram (2 of 2)

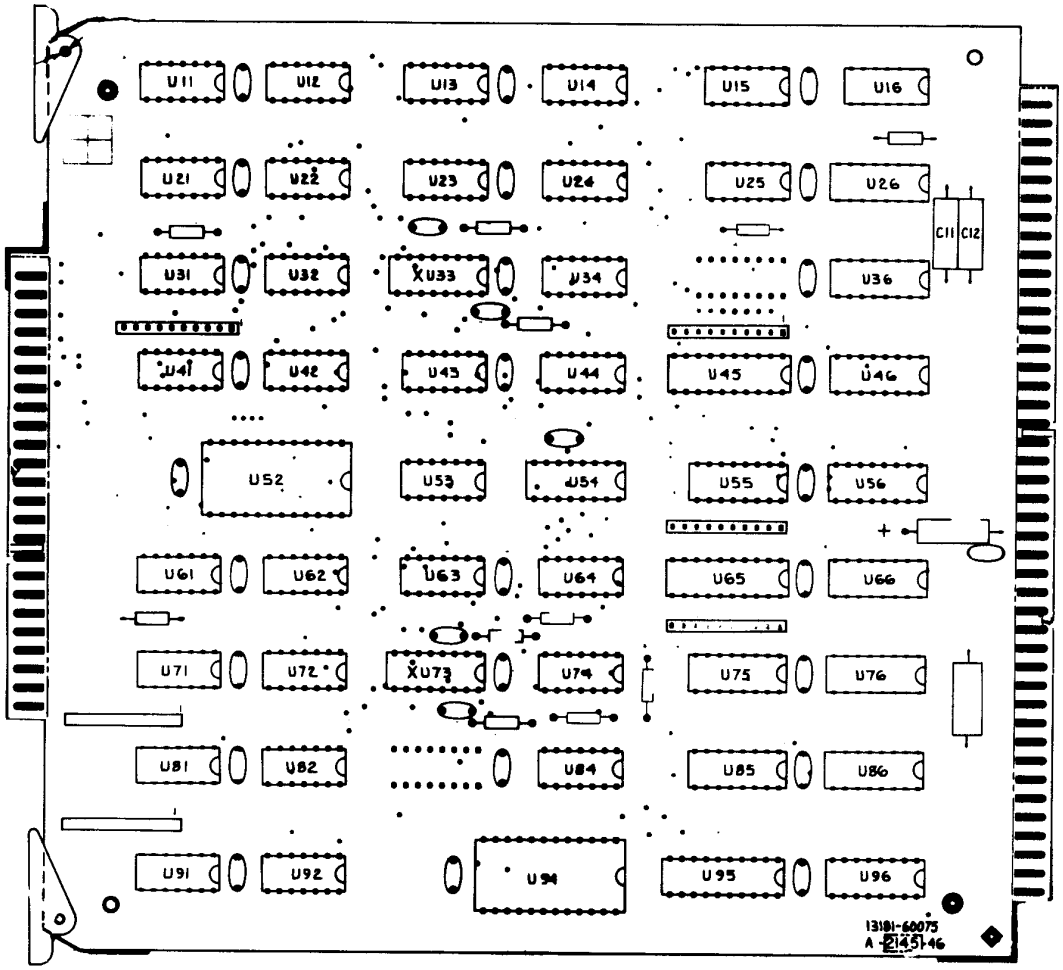


Figure 5-5. Mag Tape 2 PCA Parts Location Diagram

TABLE 5-4. MAG TAPE 2 PCA REPLACEABLE PARTS

REFERENCE DESIGNATION	DESCRIPTION	PART NUMBER
	MAG TAPE 2 PCA	13181-60075
C1 thru C7, C9, C10, C13, C15 thru C22, C24, C25, C27 thru C29, C31 C32, C34 thru C36	CAPACITOR: Fixed .01 μF	0160-2055
C8, C30	CAPACITOR: Fixed	0160-3535
C11, C12, C23, C33	CAPACITOR: Fixed 4.7 μF	0180-0100
C14	CAPACITOR: Fixed 330 pF	0160-2208
C26	CAPACITOR: Fixed 27 pF	0160-2306
R1, R2, R8, R14 thru R17	RESISTOR: Fixed 1.5K	0683-1525
R3, R5, R9, R12	RESISTOR: Fixed 10K	0683-1035
R4, R6, R10	RESISTOR: 1.5K Pack	1810-0276
R7	RESISTOR: Network	1810-0279
R11, R13	RESISTOR: Network	1810-0127
U11, U12, U15, U62, U63	IC: SN74LS00N	1820-1197
U13	IC: SN74LS51N	1820-1210
U14	IC: SN74LS86	1820-1211
U16	IC: DGTL GATE 7400	1820-0054
U21, U72	IC: SN74LS08N	1820-1201
U22, U42	IC: SN74LS10N	1820-1202
U23	IC: DIGITAL	1820-1443
U24, U44	IC: SN74LS02	1820-1144

TABLE 5-4. MAG TAPE 2 PCA REPLACEABLE PARTS (Continued)

REFERENCE DESIGNATION	DESCRIPTION	PART NUMBER
U25, U71, U74	IC: SN74LS74N	1820-1112
U26, U36, U46, U56, U66, U76, U86, U96	IC: SN75121N DRVR	1820-1080
U31, U41, U61	IC: SN7438N	1820-0621
U32	IC: SN74LS393N	1820-2096
U33, U73	IC: SN74LS221N	1820-1437
U34	IC: SN74LS11	1820-1203
U43	IC: SN74LS04N	1820-1199
U45, U65, U95	IC: DIGITAL	1820-1461
U52	IC: Generator	1820-2297
U53, U92	IC: SN74LS280N	1820-1859
U54, U55	IC: 74LS257	1820-1438
U64	IC: SN74LS32	1820-1208
U75, U85	IC: SN74LS175	1820-1195
U81, U91	IC: DGTL INV 7404	1820-0174
U82	IC: DIGITAL	1820-1053
U84	IC: SN74LS30N	1820-1207
U94	IC: DIGITAL	1820-2296
	PC EXTRACTOR: LWR	13181-40005
	PC EXTRACTOR: UPR	13181-40007

SECTION VI
REPLACEABLE PARTS

6-1. INTRODUCTION

This section contains information for ordering replacement parts for the HP 13181B Tape Unit Interface Kit. Table 6-1 lists the replaceable parts for the interface kit. Parts location diagrams for the printed-circuit assemblies in the kit are in section V of this manual. Tables 5-2 and 5-3 are listed in alphanumeric order by reference designation.

Tables 5-3, 5-4 and 6-1 list the following information for each part:

a. Circuit reference designation (if applicable).

b. Hewlett-Packard part number.

c. Description of the part. (Refer to table 6-2 for an explanation of abbreviations used in the Description column.)

6-2. ORDERING INFORMATION

To order replacement parts, address the order or inquiry to the local HP Sales and Service Office. (Refer to the list at the back of this manual.) Specify the following information for each part ordered.

a. Kit model number.

b. HP stock number for each part.

c. Description of each part.

d. Circuit reference designation (if applicable).

TABLE 6-1. HP 13181B TAPE UNIT INTERFACE KIT REPLACEABLE PARTS

HP PART NO.	DESCRIPTION
13181-60030	INTERCONNECT CABLE
13181-60074	MAG TAPE 1 PRINTED-CIRCUIT ASSEMBLY, 45 ips, 37.5 ips (option 001), and 25 ips (option 002), (Refer to table 5-3.) and 12.5 ips (option 003)
13181-60075	MAG TAPE 2 PRINTED-CIRCUIT ASSEMBLY (Refer to table 5-4.)
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