HEWLETT PACKARD

OPERATING AND SERVICE MANUAL

12587B

ASYNCHRONOUS DATA SET INTERFACE KIT

(FOR 2100, 2114, 2115, AND 2116 COMPUTERS)

Card Assembly
12587-60004, Rev. 1101

Note

Retain this manual with the applicable computer system documentation.

12587-90006

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GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. This operating and service manual covers general information, installation, programming, theory of operation, maintenance, and replaceable parts for the Hewlett-Packard 12587B Asynchronous Data Set Interface Kit. (See figure 1-1.)

1-3. DESCRIPTION.

1-4. The HP 12587B Asynchronous Data Set Interface Kit includes a single plug-in printed-circuit card that allows Hewlett-Packard 2100, 2114, 2115, and 2116 Computers to input or output control signals and data signals via common-carrier data transmission equipment. The control signals conform to signals that are defined by Electronic Industries Association Standard RS-232-B. The control signals ensure a communication link between two data sets and prepare a Bell Telephone System 103 or 202 Data Set, or equivalent, for data transmission or reception. In the transmit mode, the interface kit converts parallel data output from a computer to serial data that is compatible with the data set. In receive mode, the interface kit converts serial data output from a data set to parallel data for computer input. The interface kit adds a parity bit when required and start and stop bits to the serial data during transmission and removes start and stop bits from the serial data while receiving. If selected, a parity check may be performed by the interface kit. The interface kit includes the following items:

a. Asynchronous data set card (part no. 12587-60004).

b. Interconnecting cable assembly, 50 feet (part no. 12587-60006).

c. Test connector (part no. 12587-60009).

d. Operating and service manual (part no. 12587-90006).

1-5. IDENTIFICATION.

1-6. Printed-circuit card revisions are identified by a letter, a date code, and a division code stamped on the board (e.g., A-1005-22). The letter code identifies the version of the etched trace pattern on the unloaded board. The date code (four middle digits) refers to the electrical characteristics of the loaded board. The division code (last two digits) identifies the Hewlett-Packard division that manufactured the board. If the date code stamped on the printed-circuit board does not agree with the date code shown on the title page of this manual, there are differences between your board and the board described in this manual. These differences are described in manual supplements available at the nearest HP Sales and Service Office.

1-7. SPECIFICATIONS.

1-8. Specifications for the interface kit are listed in table 1-1.

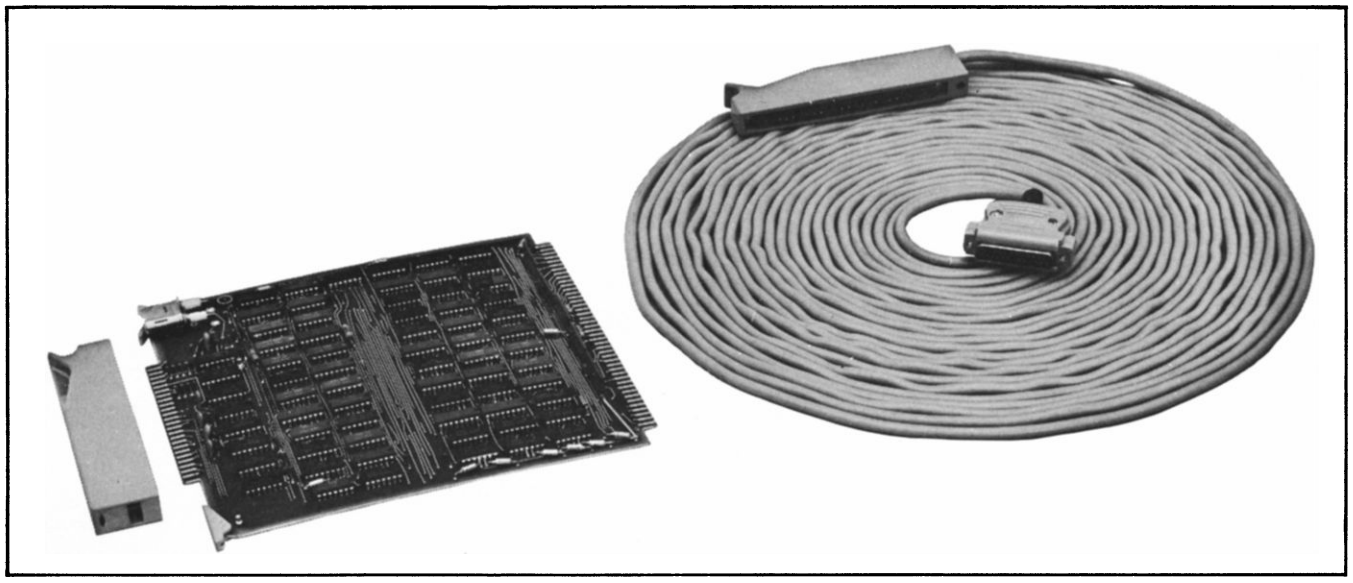

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Figure 1-1. HP 12587B Asynchronous Data Set Interface Kit

Table 1-1. Interface Kit Specifications

CHARACTERISTICS	SPECIFICATIONS
Function:	Asynchronous device operating in the half duplex mode that converts parallel data to serial data for transmission and converts received serial data to parallel data.
Compatibility:	Used with Bell Telephone System 103 or 202 type data sets, or equivalent.
Interface Requirements:	Conforms to Electronic Industries Association Standard RS-232-B.
Data Transfer Rate to/from Data Set:	Adjustable with jumpers to discrete rates between approximately 26 and 3,110 bits per second.
Character Size: (Input/Output of Computer)	1 to 8 bits
Power Consumption from Computer:	
+4.5-volt supply:	1.6A
+12-volt supply:	80 mA
-2-volt supply:	70 mA
-12-volt supply:	45 mA

SECTION II
INSTALLATION

2-1. INTRODUCTION.

2-2. This section contains information on unpacking, inspection, preparation for use, installation, and reshipment of the interface kit.

2-3. UNPACKING AND INSPECTION.

2-4. If the shipping carton is damaged upon receipt, request that the carrier's agent be present when the kit is unpacked. Inspect the kit for damage (cracks, broken parts, etc.). If the kit is damaged and fails to meet specifications, notify the carrier and the nearest HP Sales and Service Office immediately. (Sales and Service Offices are listed at the back of this manual.) Retain the shipping container and the packing material for the carrier's inspection. The HP Sales and Service Office will arrange for the repair or replacement of the damaged kit without waiting for any claims against the carrier to be settled.

2-5. PREPARATION FOR USE.

2-6. The interface kit is prepared at the factory to provide a data transfer rate of 1200 bits per second. If the bit transfer rate of the terminal used is not 1200 bits per second, the transfer rate of the interface kit must be changed. This is done by changing the position of jumper W1 on the circuit board and/or changing jumpers on the cable connector that connects to the circuit board. The jumpers on the cable connector are used to provide an 8-bit binary number to which the programmable scaler on the circuit card is preset. Pins J, H, 7, 6, D, C, 3, and B correspond to bit positions 2^7 through 2^0 respectively.

2-7. Some common bit transfer rates and associated preset codes are given in table 2-1. If the preset code for a selected transfer rate contains a "0" in a given column, jumper the pin shown at the bottom of that column to pin BB (ground). If a given column contains a "1", do not jumper the listed pin to ground. For example, if a bit transfer rate of 600 bits per second is desired, locate 600 in the TRANSFER RATE column of table 2-1. The table shows that jumper W1 on the circuit card must be placed in position A and that the programmable scaler must be preset to 10101000 (168 decimal). The 2^0, 2^1, 2^2, 2^4, and 2^6 columns contain "0's" so the corresponding pins, B, 3, C, 6, and H respectively, must be connected to pin BB (ground). Pin jumpering is done on the 48-pin cable connector as shown in figure 2-1.

2-8. If the required bit transfer rate is not given in table 2-1, the preset code for the required rate can be found by using the following formula:

$$\text{PRESET CODE (rounded off to the nearest decimal integer)} = 256 - \frac{423{,}000}{X \cdot R}$$

when: 256 is the count capacity of the programmable scaler;

423,000 is the oscillator frequency in pulses per second;

X is 8 if jumper W1 is in position A, or 64 if W1 is in position B. Position A allows an approximate range of discrete transfer rates of 207 to 3,110 bits per second; position B allows an approximate range of discrete transfer rates of 26 to 388 bits per second;

R is required transfer rate.

Note

For proper operation, the transfer rate of the interface kit must be within ± 0.5 percent of the transfer rate of the terminal used and at least one of the four most significant bits (pins J, H, 7 and 6) must be a "0".

Convert the decimal result to binary form, and jumper each pin that has a "0" in its corresponding bit position to pin BB. Use table 2-1 to determine which pin corresponds to each bit position.

Example: To set the interface kit transfer rate to 300 bits per second (300 bits per second is shaded in table 2-1), place jumper W1 in position B and solve the equation as follows:

$$\text{PRESET CODE (in decimal)} = 256 - \frac{423{,}000}{64 \cdot 300}$$

$$= 256 - 22.\cancel{091}$$

$$= 234$$

$$\text{234 in binary form} = 11101010$$

Bit positions 2^0, 2^2, and 2^4 contain "0's". Table 2-1 shows that pins B, C, and 6 on the 48-pin cable connector correspond to these three bit positions, so pins B, C, and 6 must be jumpered to pin BB to provide a 300 bit-per-second transfer rate.

2-9. INSTALLATION.

2-10. After the bit transfer rate of the interface kit has been set to the correct value for the terminal used, install the kit as follows:

Table 2-1. Jumper Connections for Common Bit Transfer Rates

TRANSFER RATE BITS/SEC	W1 POSITION	*PRESET CODE							
		2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
45	B	0	1	1	0	1	1	0	1
50	B	0	1	1	1	1	1	0	0
75	B	1	0	1	1	1	1	1	1
110	B	1	1	0	0	0	1	0	0
134.5	B	1	1	0	0	1	1	0	1
150	B	1	1	0	1	0	1	0	0
165	B	1	1	0	1	1	0	0	0
200	B	1	1	0	1	1	1	1	1
220	B	1	1	1	0	0	0	1	0
300	B	1	1	1	0	1	0	1	0
330	B	1	1	1	0	1	1	0	0
440	A	1	0	0	0	1	0	0	0
600	A	1	0	1	0	1	0	0	0
880	A	1	1	0	0	0	1	0	0
900	A	1	1	0	0	0	1	0	1
1050	A	1	1	0	0	1	1	1	0
1200	A	1	1	0	1	0	1	0	0
1760	A	1	1	1	0	0	0	1	0
2400	A	1	1	1	0	1	0	1	0
48-Pin Connector Pins		J	H	7	6	D	C	3	B

* If selected code has a "0" in a given column, connect pin listed at bottom of that column to pin BB. (Pins 6, C, and B in shaded example above). For proper operation, at least one of the four most significant bits (pins J, H, 7, and 6) must be a "0".

If code has a "1" in a given column, ensure that a jumper does not connect pin at bottom of column to pin BB.

Figure 2-1 shows how to connect jumpers.

a. Halt computer and turn computer power off.

b. Gain access to computer card cage and insert the interface card in an unused I/O slot. Make sure that every higher priority slot has either an interface card or a priority jumper card installed.

c. Connect the 48-pin connector of the kit interconnecting cable to the interface card. Pass other end of cable out rear of computer.

d. Close computer door or replace panel and connect the interconnecting cable 25-pin connector to rear of data set.

e. Verify proper operation of the interface kit by performing the diagnostic test using the Send/Receive Interface Test diagnostic tape. Refer to the Diagnostic Program Procedure (part no. 12587-90005 for the 2100 Computer or part no. 12587-90002 for the 2114, 2115, and 2116 Computers) in the Manual of Diagnostics for operating procedures.

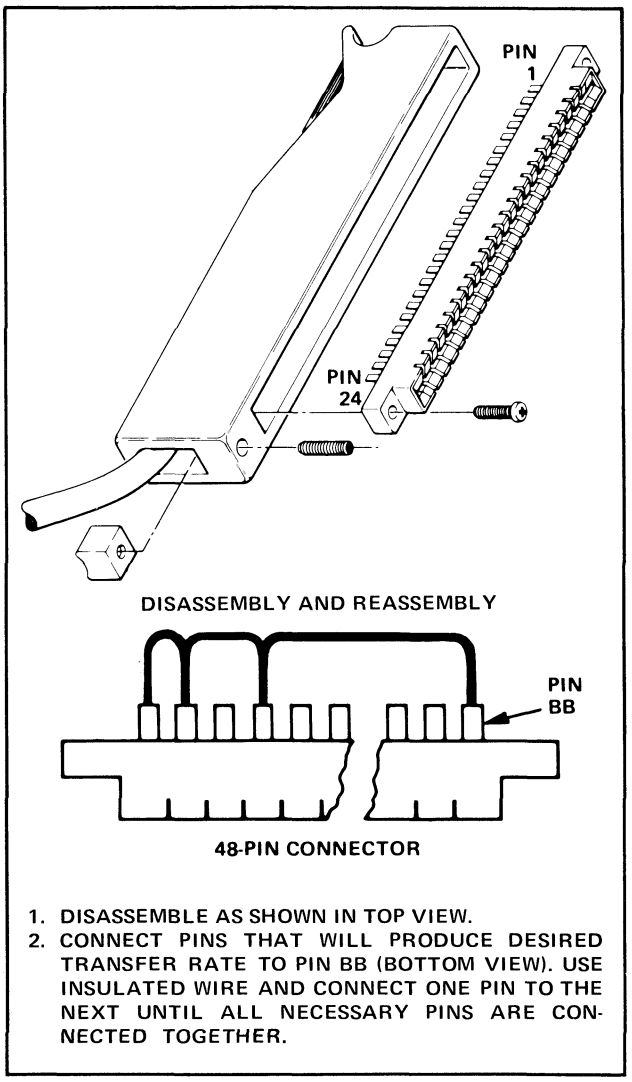

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Figure 2-1. Preset Code Jumpering Instructions

2-11. RESHIPMENT.

2-12. If an item of the kit is to be shipped to Hewlett-Packard for service or repair, attach a tag to the item identifying the owner and indicating the service or repair to be accomplished. Include the accessory number of the kit.

2-13. Package the item in the original factory packaging material, if available. If the original material is not available, standard factory packaging material can be obtained from a local Hewlett-Packard Sales and Service Office.

2-14. If standard factory packaging material is not used, wrap the item in Air Cap TH-240 cushioning (or equivalent) manufactured by Sealed Air Corp., Hawthorne, N.J., and place in a corrugated carton (200 pound test material). Seal the shipping carton securely and mark it "FRAGILE" to assure careful handling.

Note

In any correspondence, identify the kit by number. Refer any questions to the nearest Hewlett-Packard Sales and Service Office.

SECTION III
PROGRAMMING

3-1. INTRODUCTION.

3-2. This section contains assembly language programming information for the interface kit. A sample assembly-language program, with explanatory comments, is included.

3-3. For information concerning software systems used with the computer, software interfacing, and operating procedures, refer to the applicable software manuals provided with the computer documentation.

3-4. CONTROL WORD FORMAT.

3-5. The computer must output control words to set the interface card to the desired operating parameters. The control word, for example, sets the interface card to the receive or transmit mode, selects parity check or no parity check, etc. Table 3-1 lists the function of each bit in a control word. Use the information in table 3-1 to establish control words to effect desired program operation.

3-6. Bits 0 through 3 of each control word that specifies a transmit or receive operation must contain the two's complement of the number of bits in each character. Table 3-2 shows the condition of bits 0 through 3 for character lengths of one to nine bits.

3-7. DATA WORD FORMAT.

3-8. Bits 0 through 7 of a data word are reserved for the actual data character. Bits 8 through 15 of a data word provide control and status check functions. Functions of bits 8 through 15 in a computer output data word are different than the functions of the same bits in an input data word. Table 3-3 lists functions of bit 0 through bit 15 for both input and output data words.

3-9. INTERFACE CARD OPERATION.

3-10. Section IV of this manual contains theory of operation for the interface card. A flowchart, figure 4-4, is provided to show the sequence of operations of the interface card. Use the flowchart and the functional descriptions in section IV as an aid to programming.

3-11. TIMING.

3-12. Timing diagrams that are useful for programming data transfers are provided in section V of this manual. Diagrams that show interface card operation in response to a control word, to reception of data, and to transmission of data are included.

Table 3-1. Control Word Bit Functions

BIT POSITION	BIT VALUE	BIT FUNCTION
0 thru 3	–	Two's complement of bits per character. (Refer to table 3-2.)
4,5,6	–	Not used.
7	0	Selects even parity when parity is used.
	1	Selects odd parity when parity is used.
8	0	Parity check and generation is not used.
	1	Parity check and generation is used.
9	0	Echo operation not used.
	1	Echo operation used. (Received data retransmitted to originator.)
10	0	Not used.
	1	Not used.
11	–	Not used.
12	0	Loss of one of three line status checks (CF, CC, SBB) in input word does not cause a Flag signal.
	1	Loss of one of three line status checks (CF, CC, SBB) in input word causes a Flag signal.
13	0	Sets the interface card to the receive mode.
	1	Sets the interface card to the transmit mode.
14	0	Turns off interface card by disabling Data Terminal Ready Signal to the data set.
	1	Turns on interface card by enabling Data Terminal Ready Signal to the data set.
15	0	Not used.
	1	Denotes a control word.

Table 3-2. Two's Complement of Bits Per Character

BITS 0-3 OF CONTROL WORD (BINARY)				BITS PER CHARACTER (SEE NOTE)
BIT 3	BIT 2	BIT 1	BIT 0	
1	1	1	1	1
1	1	1	0	2
1	1	0	1	3
1	1	0	0	4
1	0	1	1	5
1	0	1	0	6
1	0	0	1	7
1	0	0	0	8
0	1	1	1	9

Note: The bits-per-character value includes one parity bit but does not include start or stop bits. The start and stop bits are generated (output) and deleted (input) by the interface card. If parity is not used, decrease the bits-per-character value by one and use the corresponding two's complement.

3-13. SAMPLE PROGRAM.

3-14. An example of a typical program using the interface kit is provided in table 3-4. The program is written for a Bell Telephone System 202 Data Set and accomplishes the following:

a. Initializes the interface card.

b. Uses the reverse channel capability of the 202 Data Set to indicate that the data set is prepared to receive data.

c. Alternately sends and receives 10 8-bit characters.

3-15. The program includes operating instructions and comments that explain the instructions, and figures 3-1 and 3-2 show the function of each bit in the two control words used in the program.

Table 3-3. Data Word Bit Functions

BIT POSITION	BIT VALUE	BIT FUNCTION IN INPUT DATA WORD	BIT FUNCTION IN OUTPUT DATA WORD
0 thru 7	–	Received information (one character right justified).	Transmitted information (one character).
8	–	Not used.	Not used.
9	0	No errors detected (Error FF set).	Not used.
	1	Parity error detected or the interface card was not serviced resulting in a lost character.	Not used.
10	0	Another data set is not attempting to establish a connection with data set associated with the interface card.	Disables Secondary (Supervisory) Data Send signal line.
	1	Data set is ringing (CE signal) indicating another data set is attempting to establish a connection.	Enables Secondary (Supervisory) Data Send signal line.
11	0	A distant data set carrier signal is not detected; therefore, the data set cannot receive data.	Not used.
	1	The Carrier Detect (CF) signal of a distant data set is present and the data set can receive data.	Not used.
12	0	The data set is not prepared to transmit or receive data.	Not used.
	1	A Data Set Ready (CC) signal indicates the data set is ready to transmit or receive data.	Not used.

Table 3-3. Data Word Bit Functions (Continued)

BIT POSITION	BIT VALUE	BIT FUNCTION IN INPUT DATA WORD	BIT FUNCTION IN OUTPUT DATA WORD
13	0	The interface card is not busy.	Not used.
	1	The interface card is in the process of transmitting or receiving data.	Not used.
14	0	Secondary (Supervisory) Data Receive signal line disabled.	Not used.
	1	Secondary (Supervisory) Data Receive signal line enabled.	Not used.
15	0	Interface card is not prepared for a forthcoming send or receive operation.	Denotes data word.
	1	Interface card parallel data output buffer is cleared of data and is ready to accept another character (transmit mode) or parallel data input buffer contains data to input to the computer (receive mode).	Not used.

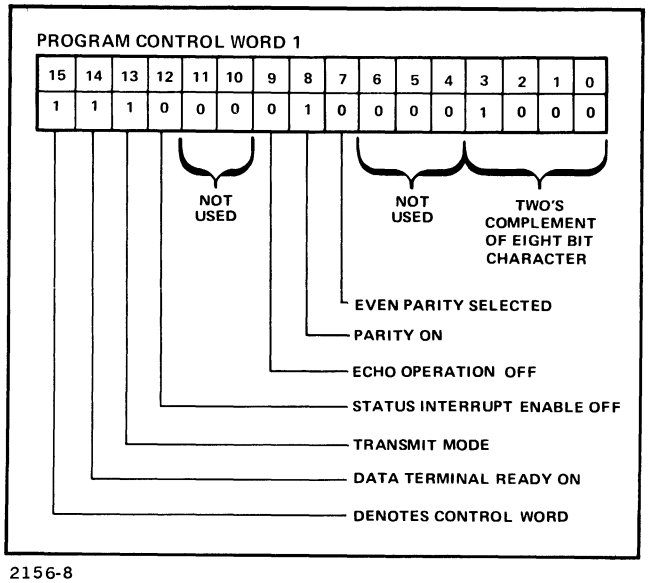

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Figure 3-1. Transmit Control Word

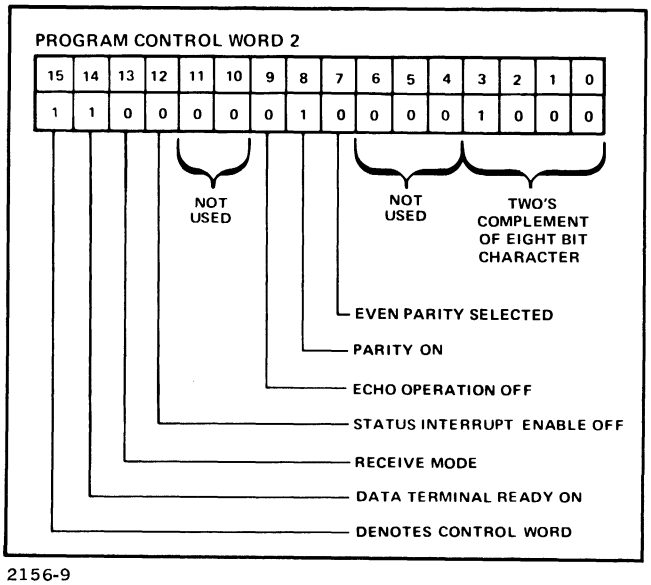

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Figure 3-2. Receive Control Word

Table 3-4. Typical Program

```
0001  ASMB,A,B,L
0002        ORG 100B
0003  *
0004  *
0005  *       PROGRAM SENDS TO AND RECEIVES FROM
0006  *       A COMPUTER,TERMINAL, OR TELEPHONE.
0007  *
0008  *
0009  *       MINIMUM EQUIPMENT NEEDED IS:
0010  *       202 TYPE DATASET, 12587B INTERFACE AND CABLES,
0011  *       2100 SERIES COMPUTER.
0012  *
0013  *       TO RUN THE PROGRAM WITHOUT A TERMINAL OR ANOTHER COMPUTER,
0014  *       DELETE THE "JSB STC" AND THE "STA B,I" IN THE
0015  *       RECEIVE SECTION.
0016  *
0017  *       1)  LOAD ADDRESS 100B.
0018  *
0019  *       2)  PRESS "PRESET" AND "RUN".
0020  *
0021  *       3)  FROM THE 202 DATASET TELEPHONE, CALL A NEARBY
0022  *           TELEPHONE (IT DOESN'T HAVE TO BE A DATASET).
0023  *
0024  *       4)  PRESS THE DATA BUTTON.  IT SHOULD STAY LIT
0025  *           INDICATING THAT THE DATASET IS RECEIVING THE
0026  *           DATA TERMINAL READY INDICATION FROM THE COMPUTER.
0027  *
0028  *       5)  LISTEN ON THE NORMAL TELEPHONE TO DETERMINE THE
0029  *           EFFECTS OF THE LINE TURNAROUNDS.  THE PROGRAM SHOULD
0030  *           OSCILLATE BETWEEN SEND AND RECEIVE.
0031  *
0032  *
0033  *       TO RUN THE PROGRAM WITH TWO COMPUTERS,
0034  *       START THE PROGRAM IN EACH AND ESTABLISH
0035  *       A DATA CONNECTION BETWEEN THE 202 DATASETS.
0036  *       IF THE PROGRAM HANGS UP, THEN BOTH ENDS ARE
0037  *       IN THE RECEIVE MODE. RESTART ONE COMPUTER
0038  *       AT LOCATION 100B AND OSCILLATION BETWEEN
0039  *       SEND AND RECEIVE SHOULD TAKE PLACE.
0040  *
0041  *
0042  *       TO RUN THE PROGRAM WITH A TERMINAL, START THE
0043  *       PROGRAM AND ESTABLISH A DATA CONNECTION WITH
0044  *       THE TERMINAL.  TYPE A LINE FOLLOWED BY THE ETX
0045  *       CHARACTER, AND THE COMPUTER SHOULD TYPE IT BACK.
0046  *
0047  *
0048  *       202 NOTES
0049  *
0050  *       BEFORE "REQUEST TO SEND" IS TURNED OFF AT
0051  *       THE END OF TRANSMISSION. A ONE MILLISECOND
0052  *       DELAY IS REQUIRED TO ALLOW  THE LAST DATA
0053  *       BIT TO CLEAR THE DATA SET.  THE DELAY IS PROVIDED
0054  *       BY THE PAD CHARACTER FOLLOWING THE ".ETX".
0055  *
```

Table 3-4. Typical Program (Continued)

```
0056  *       LINE TURNAROUND IS 200 MILLISECONDS DURING WHICH
0057  *       TIME THE INTERFACE HOLDS OFF TRANSMISSION.
0058  *
0059  *       DURING TRANSMISSION, CARRIER DETECT IS THE DATASET'S
0060  *       OWN CARRIER, SECONDARY RECEIVED DATA IS THE DISTANT
0061  *       STATIONS'S REVERSE CHANNEL.
0062  *
0063  *       DURING RECEPTION,  CARRIER DETECT IS THE DISTANT
0064  *       STATIONS'S CARRIER,  SECONDARY RECEIVED DATA IS THE
0065  *       DATASET'S OWN REVERSE CHANNEL.
0066  *
0067  *       DURING LINE TURNAROUND, CARRIER DETECT AND
0068  *       SECONDARY RECEIVED DATA GO OFF, AND THEN BACK ON.
0069  *
0070  *
0071  *
0072  *
0073  SEND  JSB BUSY          SWITCH PARAMETERS WHEN DEVICE NOT BUSY.
0074        LDA CW1           OCTAL 160410-SEND MODE,EVEN PARITY
0075        OTA SC              8 BIT CHARACTER.
0076  *
0077        LDA LENG          PLACE TWO'S COMPLEMENT OF THE
0078        CMA,INA,SZA,RSS   NUMBER OF CHARACTERS TO BE SENT
0079        JMP ETX             IN "COUNT".  OMIT IF 00 CHARACTERS.
0080        STA COUNT
0081        LDB ADDR          B REGISTER CONTAINS CHARACTER POINTER.
0082  *
0083  LOOP1 LDA B,I           CHARACTER IS IN LOWER BYTE.
0084        AND MSK           ISOLATE.
0085        OTA SC            SEND CHARACTER.
0086        JSB STC           WAIT FOR FLAG SET.
0087        INB               BUMP CHARACTER POINTER.
0088        ISZ COUNT         INCREMENT AND TEST COUNT.
0089        JMP LOOP1
0090  *
0091  ETX   LDA .ETX          SEND END OF TRANSMISSION CODE.
0092        OTA SC
0093        JSB STC
0094  *
0095        LDA MSK         CHARACTER BEFORE .ETX IS BEING TRANSMITTED,
0096        OTA SC            .ETX IS WAITING IN BUFFER.
0097        JSB STC         PAD GETS .ETX OUT BEFORE TURNAROUND.
0098  *
0099  RECV  JSB BUSY          CHANGE PARAMETERS WHEN NOT BUSY.
0100        LDA CW2           OCTAL 140410-RECEIVE MODE, EVEN PARITY
0101        OTA SC              8 BIT CHARACTER.
0102        LDA SBA           OCTAL 2000.  REVERSE CHANNEL ON
0103        OTA SC              INDICATES READY TO RECEIVE.
0104  *
0105        CLA               ZERO CHARACTER COUNTER.
0106        STA LENG
0107        LDB ADDR          B IS POINTER TO CHARACTER.
0108  *
0109        LIA SC            RESET READY FLIP-FLOP.
0110  *
```

Table 3-4. Typical Program (Continued)

```
0111  L2     JSB STC          WAIT FOR CHARACTER.
0112         LIA SC
0113         AND MSK          ISOLATE CHARACTER.
0114         CPA .ETX         IF ETX THEN GO BACK TO SEND SECTION.
0115         JMP EXIT
0116         STA B,I        STUFF IN BUFFER.
0117         INB
0118         ISZ LENG
0119         JMP L2           GET NEXT CHARACTER.
0120         JMP SEND
0121  *
0122  EXIT   CLA           TURN OFF REVERSE CHANNEL.
0123         OTA SC
0124  L3     LIA SC        THIS ROUTINE
0125         RAL             FOLLOWS THE SWITCH OF REVERSE
0126         SSA               CHANNEL FROM THE LOCAL STATION
0127         JMP L3              TO THE DISTANT STATION.
0128  *
0129  L4     LIA SC
0130         RAL           ROUTINE WILL NOT ALLOW TRANSMISSION
0131         SSA,RSS         UNTIL REVERSE CHANNEL
0132         JMP L4            IS ON.
0133         JMP SEND
0134  *
0135  BUSY   NOP
0136         LIA SC           GET STATUS
0137         RAL,RAL          ROTATE BUSY BIT TO BIT 15
0138         SSA             IF 0 THEN OK TO SWITCH MODE.
0139         JMP BUSY+1
0140         JMP BUSY,I
0141  *
0142  STC    NOP
0143         STC SC,C         WAIT FOR OPERATION
0144         SFS SC             COMPLETION
0145         JMP *-1              FLAG.
0146         JMP STC,I
0147  *
0148  A      EQU 0
0149  B      EQU 1
0150  SC     EQU 15B          I/O SLOT OF 12587B.
0151  LENG   DEC 10
0152  COUNT  NOP
0153  ADDR   DEF BUFFR
0154  .ETX   OCT 3          THIS WOULD BE LF, 12B, FOR TTY.
0155  CW1    OCT 160410
0156  CW2    OCT 140410
0157  SBA    OCT 2000
0158  MSK    OCT 177
0159  BUFFR  EQU *
0160         REP 10
0161         NOP
0162  *
0163  *
0164  *
0165         END
```

SECTION IV
THEORY OF OPERATION

4-1. INTRODUCTION.

4-2. This section contains an overall functional description and a detailed circuit description for the interface card. Located at the back of this section is a flow chart (figure 4-4) that illustrates the operating sequence of the interface card.

4-3. OVERALL FUNCTIONAL DESCRIPTION.

4-4. The interface kit includes a single plug-in printed-circuit card that provides parallel-to-serial or serial-to-parallel data conversion. The interface card also provides data set control signals which conform to Electronic Industries Association Standard RS-232-B. The data conversion function and data set control signals allow a computer to transmit or receive data via common-carrier data transmission lines.

4-5. Figure 4-1 is a functional block diagram showing the operational relationship of the computer, the data set, and the interface card. Three functions are achieved by the interface card: data transmission, data reception, and line status checks. The following paragraphs describe each function.

4-6. DATA TRANSMISSION.

4-7. In the transmit mode, parallel data is output from the computer to the interface card, and is converted to serial data. The serial data is transmitted over common-carrier equipment by the data set. In operation, a control word from the computer sets the interface card control logic for the transmit mode. The control logic places the data set in the transmit mode and prepares the parallel data output buffer for a load operation. Parallel data is output from the computer to the parallel data output buffer. If the 8-bit shift register is clear and Clear-to-Send (CB) is enabled, the control logic allows the contents of the parallel data output buffer to enter the 8-bit shift register. The clock (synchronized with the computer timing) is enabled and shifts the contents of the 8-bit shift register to the data set in serial format. The bit register/counter section of the control logic disables the clock when one character bit stream is transmitted serially. (The parity bit, if selected, and start and stop bits are added by the interface card.) The data set transmits the serial data over common-carrier lines.

4-8. DATA RECEPTION.

4-9. In the receive mode, serial data is transferred from the data set to the interface card and is converted to parallel data. The parallel data is then input to the computer. In operation, a control word from the computer sets the interface card control logic for the receive mode. The control logic notifies the data set that the interface card is ready to accept data. The first bit (start bit) of serial data enters the 8-bit register and enables the clock. The clock shifts the subsequent serial data bits into the 8-bit shift register. The bit register/counter right justifies the data. The control logic checks parity (if selected) and transfers the contents of the 8-bit shift register to the parallel data input buffer. The data in the parallel data input buffer is then transferred to the computer.

4-10. LINE STATUS CHECKS.

4-11. Three of the common-carrier lines (Data Set Ready, Secondary Data Receive, and Carrier Detect) connecting the transmit and receive data sets are monitored by the interface card. The line status check signals are transferred from the interface card to the computer. When selected by the program, an absence of any one of the line status check signals generates an interface card Flag signal.

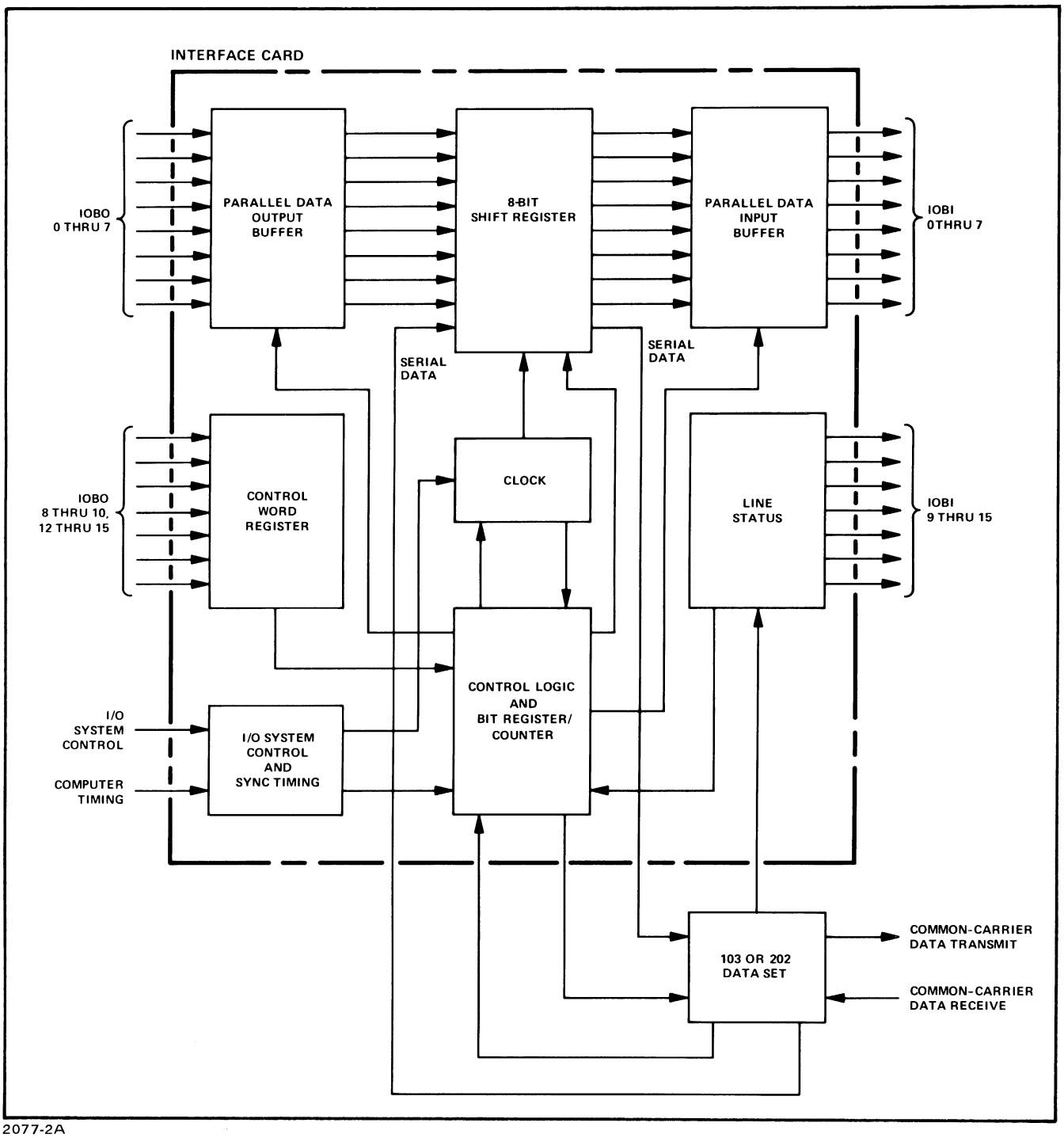
4-12. DETAILED CIRCUIT DESCRIPTION.

4-13. The following paragraphs contain a detailed circuit description for the interface card. The description covers the I/O system controls, the control word register, the 8-bit shift register, the bit register/counter, the clock and synchronize circuit, the control logic, and line status. See the logic diagram for the interface card (figure 5-14) when referencing the detailed circuit description.

4-14. INPUT/OUTPUT SYSTEM CONTROLS.

4-15. When power is initially applied by the POWER switch of the computer, the Interrupt System Enable FF on the I/O control card is cleared, which disables the computer interrupt system. Initial power disables the interface card with the POPIO and CRS signals. The CRS signal clears the Control FF, Clock Enable FF, and On/Off FF. The POPIO signal sets the Flag Buffer FF and Ready FF. The output signals from these flip-flops clear the Parity FF, Start Bit FF, Justify FF, Load 9's FF, and set the N-Zero FF, Stop Bit FF, and Flag FF at computer time T2 (ENF).

4-16. After initialization, a STF instruction with the select code of 00 (octal) sets the Interrupt System Enable FF and the computer IEN signal enables the I/O control card. The interface card will not interrupt until a STC,CLF instruction with the select code of the interface card is output from the computer. The select code, the IOG(B) signal, and the STC signal set the Control FF. The Control FF enables an interrupt, but does not affect the functioning of the data set associated with the interface card. The CLF signal clears the Flag Buffer FF and the Flag FF.



2077-2A

Figure 4-1. Interface Card Functional Block Diagram

4-17. When the interface card generates a Flag signal, the set output from the Control FF, combined with the IEN signal and set-side output of the Flag FF, sets the IRQ FF at computer time T5 (SIR) if the PRH signal is true. This causes a program interrupt, which usually occurs at the end of the current phase of computer operation. At the next time T2, the IRQ FF clears, allowing any higher-priority device to use the requested interrupt. If no higher-priority device requests an interrupt, the IRQ FF sets again at time T5 (SIR signal). The FLG and IRQ signals indicate the service request address of the interface card, and the computer services the card.

4-18. CONTROL WORD REGISTER.

4-19. The control word register consists of seven flip-flops and a gate network. Signal inputs from the computer to the control word register set the interface card for the

Table 4-1. Control Word Register Functions

IOBO LINE	FLIP-FLOP	FUNCTION	
		LOGIC 0 INPUT	LOGIC 1 INPUT
7	Odd/Even	Even parity selected	Odd parity selected
8	Parity On	Parity check disable	Generate and check parity
9	Echo	Echo disabled	Echo enabled
12	Mask (Status Interrupt Enable)	Data Set Ready (CC), Carrier Detect (CF), and Secondary Data Receive (SBB) interrupts disabled.	Data Set Ready (CC), Carrier Detect (CF), and Secondary Data Receive (SBB) interrupts enabled.
13	Send/Receive and Request-to-Send	Receive mode	Send mode
14	On/Off	Data Terminal Ready (CD) signal disabled to data set.	Data Terminal Ready (CD) signal enabled to data set.
15	Gate Network	Signal input on IOBO lines is data.	Signal input on IOBO lines is control.

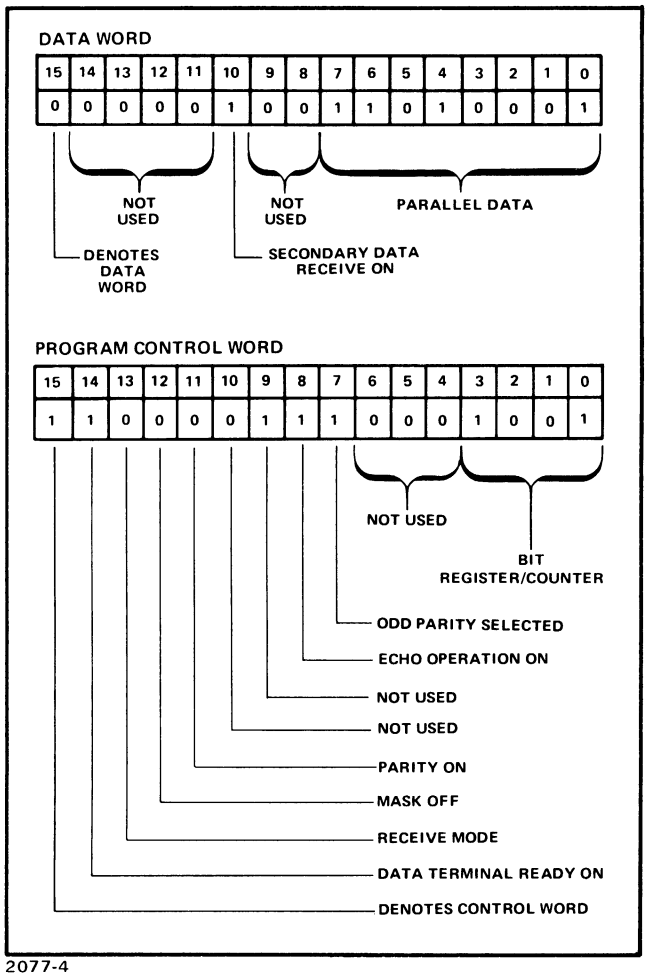
desired operating mode. Table 4-1 lists each input line from the computer to the card (IOBO lines 7 through 15), the associated flip-flop in the control word register, and the function of each flip-flop. In operation, a logic 1 from the output of gate U47B (LSCM, IOGB, and LSCL) combines with a logic 1 IOO signal, allowing capacitor C6 to charge through resistor R64. When the IOO signal changes to a logic 0 (at the end of computer time T4), a short negative-going pulse appears at the output of gate U46A and enables the decoding of bit 15. If input signal IOBO 15 is a logic 1 (denoting a control word), the output of gate U56C provides a clock signal at the clock input of the control word register flip-flops. To prevent the control word from entering the parallel data output buffer, a logic 1 at pin 8 of gate U56D disables the gate and a parallel data output buffer clock signal is not produced. However, should input signal IOBO 15 be a logic 0 (denoting data), U56D and U56A would produce a parallel data output buffer clock signal and the control word register flip-flops would be inhibited. The control word also contains the word size of the parallel data. The word size information is coupled to the bit register/counter by IOBO lines 0 through 3. Typical program word formats for a control word and data word are shown in figure 4-2.

4-20. 8-BIT SHIFT REGISTER.

4-21. The 8-bit shift register consists of two 4-bit shift register integrated circuits that provide parallel-to-serial or serial-to-parallel data conversion. This is accomplished by switching the inputs of the 8-bit shift register between two sources. A logic 0 Parallel Enable signal loads parallel data into the shift register for a parallel-to-serial data conversion (transmit mode for the interface card). A logic 1 Parallel Enable signal loads serial data into the shift register for a serial-to-parallel data conversion (receive mode of operation for the interface card).

4-22. PARALLEL-TO-SERIAL DATA CONVERSION. Parallel-to-serial data conversion occurs in the following manner. Parallel data from the computer enters the 8-bit shift register via the eight flip-flops of the parallel data output buffer. The converted serial data is output from the 8-bit shift register at pin 12 of integrated circuit U95. The serial data is clocked through the Start Bit FF and the Stop Bit FF. With the Stop Bit FF set and the Start Bit FF cleared at the beginning of a transmit operation, the serial data from the 8-bit shift register will be preceded by a stop bit and a start bit. (See figure 4-3.) The stop bit provides a separation of transmitted and received data when changing the operating mode. The start bit signifies the beginning of a character bit stream. Serial data is supplied, through U42A, U42C, and U71A, to line driver U81A which applies the character bit stream to the data set.

4-23. SERIAL-TO-PARALLEL DATA CONVERSION. Serial-to-parallel data conversion begins with the reception of a character bit stream from the data set. Line receiver U91B accepts the data bits and applies them, through U71D, to U93A. Because the Request-to-Send FF is cleared, the inverted data bits are output from gate U93A. The first data bit of the character bit stream from U93A sets the Clock Enable FF. With the Parallel Enable signal a logic 1 and the clock operating, the bits are shifted through

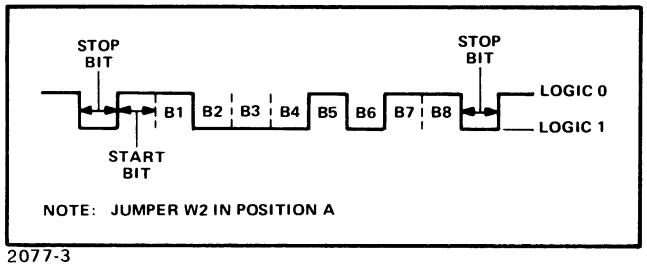


2077-4

Figure 4-2. Typical Control Word and Data Word Formats

the Serial In FF to the 8-bit shift register. After the bits are shifted into the 8-bit shift register and placed in the right justified position (least significant bit located at output pin 12 of integrated circuit U95), a clock pulse from the bit register/counter loads the parallel data into the Parallel Data Input Buffer FFs. The data is input to the computer from the parallel data input buffer.

4-24. PARITY COMPUTATION. Parity computation is accomplished with the Parity On FF and the Odd/Even FF of the control word register, the Parity FF, and the Error FF. Operation of the interface card without the use of parity is possible by not setting the Parity On FF during the control word output. In the transmit mode, each bit of the



2077-3

Figure 4-3. Typical Serial Character Bit Stream

character bit stream is applied to the Parity FF by gate U73C. The output of the Parity FF and the output of the Odd/Even FF are compared by gates U52B and U52C to determine the logic level of the parity, and the result is inserted as the last bit of the character bit stream by gate U42D. (The Odd/Even FF is set or cleared by the IOBO 7 line during the output of the control word from the computer. A logic 1 causes odd parity and a logic 0 causes even parity.) In the receive mode, gate U73D applies each bit of the character bit stream to the Parity FF. The output of the Parity FF and the output of the Odd/Even FF are compared by gates U52B and U52C. If the logic levels of the flip-flops do not agree, a fault is detected and the Error FF is cleared. The Error FF remains clear only for that one particular character bit stream.

Note

If the Ready FF remains set due to the failure of the program to service the interface card, the Error FF is held clear indicating the loss of the preceding character bit stream.

4-25. BIT REGISTER/COUNTER.

4-26. The bit register/counter consists of a four flip-flop register (CTR 0 through CTR 3) and associated gating, a 4-bit binary counter (U102), a BCD-to-decimal decoder (U112), a Load 9's FF and a Justify FF. The bit register/counter controls the shifting of one complete character bit stream from the 8-bit shift register during the transmit mode of operation and right justifies a character bit stream in the 8-bit shift register during the receive mode of operation. The number of shifts required for proper operation is determined by the two's complement portion of the control word from the computer. (Refer to paragraph 4-19 and figure 4-1.)

4-27. TRANSMIT MODE. In the transmit mode, the register portion of the bit register/counter is loaded with the two's complement (a negative number) of the total number of bits that constitutes one complete character bit stream. The counter portion of the bit register/counter counts forward to one, adds the parity bit if the control word register Parity FF is set, and provides the desired number of stop bits to complete the character bit stream. In operation, a combination of IOO and IOBO 15 signals provides a clock signal to load FFs CTR 0 through CTR 3 with the complement of the two's complement of the character bit stream. (The complement of the two's complement is derived from inversion by gates U75A through U75D.) Because the Justify FF is cleared during the transmit mode, gates U72C, U92A, and U92C apply the information contained in FFs CTR 0 through CTR 3 to 4-bit binary counter U102 in the two's complement form. The information loads into the 4-bit binary counter when the Parallel Enable signal becomes a logic 0. At each clock signal from gate U72B, the 4-bit binary counter counts forward and the BCD count is decoded by BCD-to-decimal decoder U112. When the number "1" is decoded at pin 12 of U112, the computer parity (if selected by the control

word) is added to the serial data by gate U42D. With jumper wire W2 in the B position and the count at "2" (pin 11 of U112), the Clock Enable FF is cleared which disables the clock circuit. The stop bit at the start of the next character bit stream provides a one stop bit separation between data. If W2 is in the A position, the count is allowed to reach "3" (pin 3 of U112) and one stop bit is placed in the character data stream before the clock circuit is disabled. This stop bit combined with the stop bit at the start of the next character bit stream provides the two stop bit separation between data. After the clock circuit is disabled, a clock signal from gate U122C is applied to the Error FF to check for errors, and the N-Zero FF is set by a logic 0 signal from gate U52D. (Setting the N-Zero FF indicates the character bit stream has been transmitted.) The signal from the clear-side output of the N-Zero FF clears the Parity FF and provides a logic 0 Parallel Enable signal to the 4-bit binary counter and the 8-bit shift register. A logic 0 Parallel Enable signal reloads the 4-bit binary counter with the two's complement of the next character bit stream that was stored in the CTR 0 through CTR 3 FFs during the output of the control word. The 8-bit shift register is loaded from the parallel data output buffer and another character bit stream is transmitted.

4-28. RECEIVE MODE. In the receive mode, bits 0 through 3 of the control word (the two's complement of the number of bits in one complete character) are inverted and loaded into the register portion of the bit register/counter. Because the clear side of the N-Zero FF holds a low level (logic 0) on U102 pin 9, these bits, inverted back to the two's complement, are loaded into the 4-bit counter portion of the bit register/counter.

4-29. When the first bit of the character bit stream is received from the data set, the Clock Enable FF sets as described in paragraph 4-23. As each bit of received data is clocked into the 8-bit shift register, the 4-bit counter increments by one. When the 4-bit counter "wraps around" and U112 BCD-to-decimal decoder reaches the count of "1", gate U83A sets the Justify FF and gate U93B sets the Load 9's FF. The set outputs of these flip-flops provide a low enabling signal to the 4-bit counter and allow loading the 4-bit counter from the clear sides of CTR 0 through CTR 3 FFs. This number equals the required number of justifying shifts subtracted from 16. At computer time T3, the Load 9's FF is cleared and the justify cycle begins. Time T3 and a high (logic 1) from the Justify FF combine at gate U62D to produce a 4-bit counter clock signal from gate U72B that increments the counter every machine cycle. At the same time, gate U122A causes an 8-bit shift register clock signal. A justify shift, therefore, occurs every machine cycle.

4-30. When the output of the BCD-to-decimal decoder equals the count of "0" (pin 13 of U112), the Justify FF clears, ending the justify cycle. Gate U73A clears the Clock Enable FF and provides a clock signal to the Error FF to check for errors. The Clock Enable FF disables the clock circuit and sets the N-Zero FF. Setting the N-Zero FF indicates that data is justified. The clear-side output of the N-Zero FF clears the Parity FF and reloads the two's complement of the next character bit stream into the 4-bit binary counter.

4-31. CLOCK AND SYNCHRONIZE CIRCUIT.

4-32. The clock and synchronize circuit provides a shift signal to the 8-bit shift register and an increment signal to the bit register/counter that coincides with the computer timing but is not the same time interval as a machine cycle. Once each shift cycle, three computer timing signals (T2, T3, and T5) provide synchronization. The clock and synchronize circuit consists of a crystal-controlled oscillator, a programmable scaler, a Clock Enable FF, a frequency divider, and two synchronizing flip-flops.

4-33. CRYSTAL-CONTROLLED OSCILLATOR. The clock oscillator is a free-running, crystal-controlled oscillator consisting of U41A, U41B, U41C, and crystal Y1. Frequency of oscillation is 423,000 pulses per second. The oscillator output is connected to pin 4 of the 48-pin connector. Pin 4 is externally wired to pin F of the 48-pin connector; pin F is connected to the input of the programmable scaler.

4-34. PROGRAMMABLE SCALER. The programmable scaler consists of two, 4-bit binary counters (U51 and U61) connected to form a scaler with a 256-count capacity. The scaler can be preset to any number from 0 through 239 with external jumpers (see table 2-1). The scaler counts pulses from the crystal-controlled oscillator and generates one output pulse at U61 pin 15 each time the preset number of counts plus the accumulated pulses from the oscillator equal 255. When count 255 occurs, an output pulse is applied to U12B pin 5, and gate U41D enables the scaler preset lines. The next pulse from the oscillator sets the scaler to its preset value. By presetting the scaler to the appropriate value, the oscillator frequency can be divided by any number between 2 and 256.

4-35. CLOCK ENABLE FF. The set-side output of the Clock Enable FF combines with the oscillator signal at gate U12B to initiate the frequency divider. Due to the Clock Enable FF, the first half of the first cycle from U12B will always be a logic 0. The clear-side output of the Clock Enable FF clears the frequency divider, clocks the Request-to-Send FF, and sets the N-Zero FF. The Clock Enable FF is set during the receive mode by the output of the first bit of a character bit stream from gate U93A. In the transmit mode, the Clock Enable FF is set if the Request-to-Send FF is set, the Ready FF is cleared, and the data set Clear-to-Send signal is a logic 1. The Clock Enable FF is cleared by a Clear Control (CRS) signal or by the bit register/counter. Because the Clock Enable FF is set only when the interface card is shifting data, the set-side output of the Clock Enable FF is also used as a Busy signal (IOBI line 13) to the computer.

4-36. FREQUENCY DIVIDER. The output of the programmable scaler is reduced in frequency to the bit transfer rate of the interface card by the frequency divider. The frequency divider consists of a Divide-by-2 FF, a Divide-by-4

FF, and a Divide-by-2/8 FF. This circuit divides the programmable scaler output by 8 when jumper W1 is in the A position and by 64 when W1 is in the B position. Table 2-1 shows how to position jumper W1 and how to preset the programmable scaler to effect a desired data transfer rate.

4-37. SYNCHRONIZING FLIP-FLOPS. The synchronizing flip-flops, Sync 1 FF and Sync 2 FF, provide a shift and increment signal that is coincident with the computer timing signals. The Sync 1 FF input signal is from the frequency divider and the Sync 2 FF input is the SIR signal at time T5 of the computer cycle. In the transmit mode, the first half cycle of the bit shift frequency from gate U13A sets positive-edge-trigger Sync 1 FF. With a logic 1 at the J-input and a logic 0 at the K-input of the Sync 2 FF, gate U57E sets the Sync 2 FF at the end of computer time T5. The set output of the Sync 2 FF combines with ENF, T3B, and SIR computer signals to provide computer time periods T2, T3, and T5 from gates U67B, U67D, and U67C, respectively. The leading edge of T5 from U67C clears the Sync 1 FF and the trailing edge of T5 clears the Sync 2 FF; consequently, only one set of T2, T3, and T5 computer timing signals are available for a single bit shift cycle. In the receive mode, the only operational change is that the Sync 1 FF is set during the last half of the bit shift frequency from gate U13D. For this reason, the character bit stream is transmitted at the start of a bit shift cycle and received in the center of a bit shift cycle.

4-38. CONTROL LOGIC.

4-39. The control logic monitors and controls the input and output sequence of data conversion by the interface card. The control logic consists of the N-Zero FF, the Ready FF, the Ringing FF, and the Buffer Ready FF.

4-40. N-ZERO FF. The N-Zero FF initializes the control logic after the last bit of the current character bit stream has been transmitted or received. After the last bit of the character bit stream is processed, the setting of the N-Zero FF produces the Parallel Enable signal for the 8-bit shift register and bit register/counter, clears the Parity FF, sets the Stop Bit FF, and clears the Start Bit FF. The N-Zero FF is set each time the Clock Enable FF is cleared.

4-41. READY FF. The Ready FF signals the computer via the flag circuit that the interface card is ready to input data to the computer or that the card is ready to transmit another character bit stream to the data set. In the receive mode, the Ready FF is cleared by an LIA/B or MIA/B instruction: in the transmit mode, the Ready FF is cleared by an OTA/B instruction. An input or output instruction such as LIA,C or OTA,C clears the Ready FF and the Flag FF; however, an attempt to clear the Flag FF without executing an input or output instruction will result in another Flag signal. (The set condition of the Ready FF holds the Flag FF set until the interface card is serviced.)

Note

In the transmit mode, the Ready FF may be set if the parallel data output buffer is ready to accept new data. This does not indicate that the 8-bit shift register is empty; the 8-bit shift register may be processing the data received from the parallel data output buffer.

4-42. RINGING FF. The Ringing FF detects if common-carrier equipment is attempting to contact the data set associated with the interface card. In operation, the Ringing (CE) signal from the data set associated with the interface card is buffered by line receiver U101D, inverted by U111B, and applied as a clock signal to the Ringing FF. The resulting set output from the Ringing FF sets the Flag Buffer FF. A CLF instruction from the computer clears the Ringing FF.

4-43. BUFFER READY FF. The Buffer Ready FF retains the set condition of the Ready FF long enough for an LIA/B or MIA/B instruction to couple the condition of the Ready FF to the computer. The retention capability is necessary because any of these instructions will clear the Ready FF if the interface card is in the receive mode. The Buffer Ready FF is set by the Ready FF and is cleared by an ENF (T2) signal from the computer. The set output of the Buffer Ready FF is connected to IOBI line 15.

4-44. LINE STATUS.

4-45. The line status circuit consists of three line receivers, the Mask FF of the control register, and associated gates. The line status circuit monitors the signal lines that connect the data set associated with the interface card to the common-carrier equipment. During each computer input instruction, the Data Set Ready (CC), Secondary Data Received (SBB), and Carrier Detect (CF) signals are coupled to the computer by the receivers. During normal operation, the output of the line receivers cause a logic 0 output from gate U113A. If the Mask FF is set by the control word and one of the line signals goes off, the output of U113A sets the interface card Flag Buffer FF and the interface card generates an interrupt. If the Mask FF is not set, the Flag Buffer will not be set; however, the line signals are part of the input word to the computer.

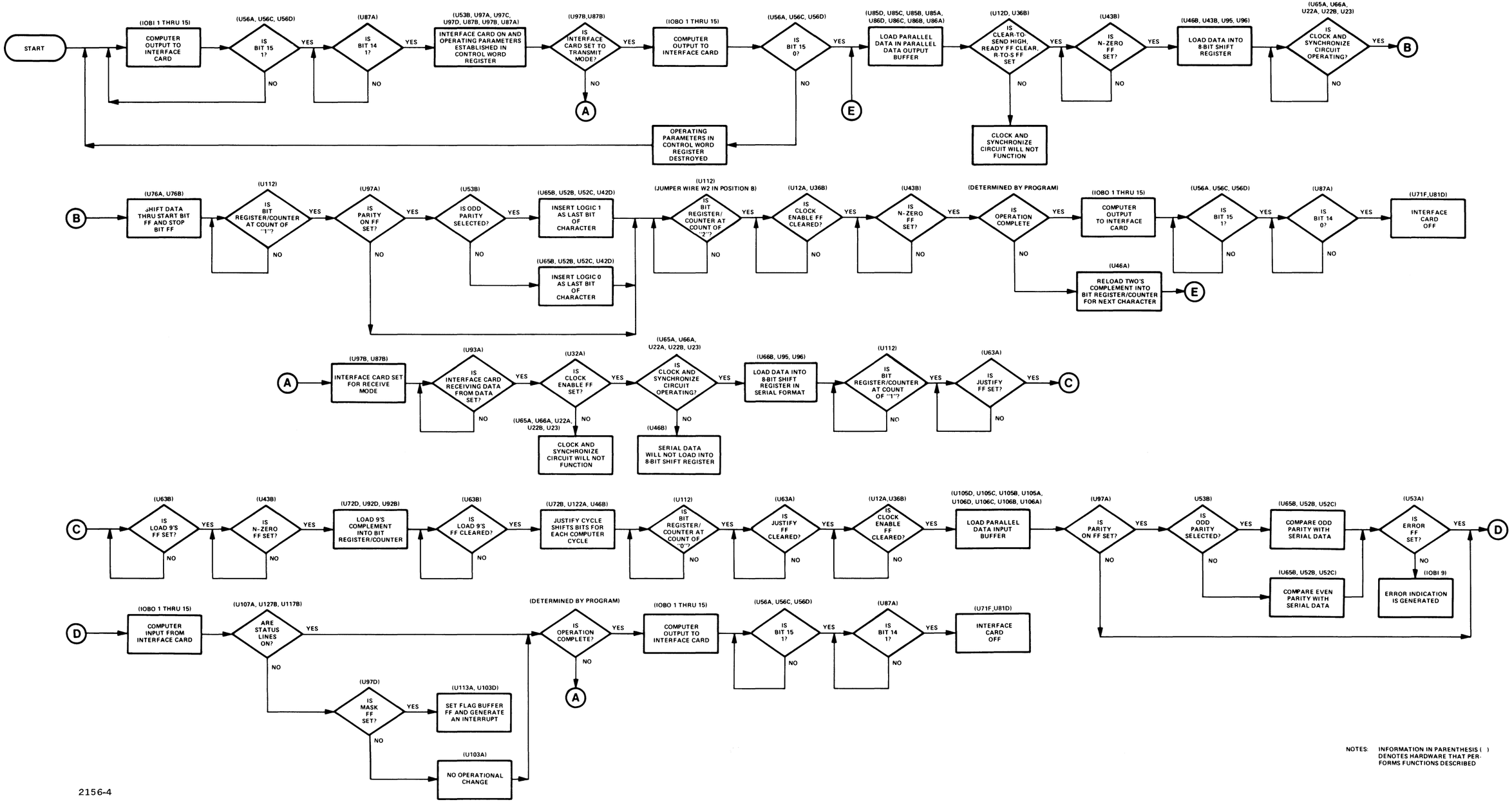


Figure 4-4. Flowchart of Interface Card Operating Sequence

SECTION V
MAINTENANCE

5-1. INTRODUCTION.

5-2. This section contains information on the diagnostics and troubleshooting for the interface card.

5-3. PREVENTIVE MAINTENANCE.

5-4. Detailed preventive maintenance procedures and schedules are given in the Installation and Maintenance Manual for the computer. There are no separate preventive maintenance procedures for the interface kit.

5-5. DIAGNOSTICS.

5-6. Complete diagnostic program operating procedures are contained in the Manual of Diagnostics. Refer to procedure part number 12587-90002 when using a 2114, 2115, or 2116 Computer or procedure part number 12587-90005 when using a 2100 Computer.

5-7. TROUBLESHOOTING.

5-8. Troubleshooting the interface card is accomplished by performing the diagnostic test described in the Manual of Diagnostics and analyzing the error halts that occur as the test is being run. Figure 5-1 and table 5-1 contain wiring and signal information for the test connector that is used to run the diagnostic test. After analyzing the error halts, see figure 5-15 of this manual for the logic and parts location diagrams of the interface card and table 5-2 for interconnecting cable pin functions. Refer to the appropriate computer documentation for additional information on backplane wiring, signal data, etc., not included in this manual. To further isolate trouble, perform the following test program, check the timing diagrams in this section, and refer to the list of equations provided in table 5-4.

5-9. TEST PROGRAM.

5-10. The test program sets the interface card for the transmit mode of operation, then transmits the information in the computer switch register (bits 0 through 7) in a serial character bit stream. An HP 180A Oscilloscope (or equivalent) with X10 probes and the card extender are required to perform the test. To conduct the test, proceed as follows:

CAUTION

Turn the power off at the computer before removing or replacing interface cards or damage may result.

a. Plug interface card with test connector attached into card extender and insert card extender in appropriate slot in computer. A resistor is attached to the test connector on the Request to Send function to cause a slight delay and eliminate a race condition.

b. Set oscilloscope sensitivity adjustment of A input to read 1 V/CM and connect A input to pin 11 of 48-pin connector.

c. Set oscilloscope sensitivity adjustment of B input to measure 0.2 V/CM and connect B input to pin 11 of gate U122C on interface card. (The signal at U122C pin 11 is the clear-side output of the N-Zero FF.) Connect external sync of oscilloscope to same location as the B input and set external sync adjustment to trigger on the positive signal.

d. Using computer front-panel controls, load test program shown in table 5-3. Return to address 100 (octal) and press computer RUN switch.

e. Adjust TIME/DIV and variable time base adjustment of oscilloscope until one character bit stream appears on screen of oscilloscope. (See figure 5-2.)

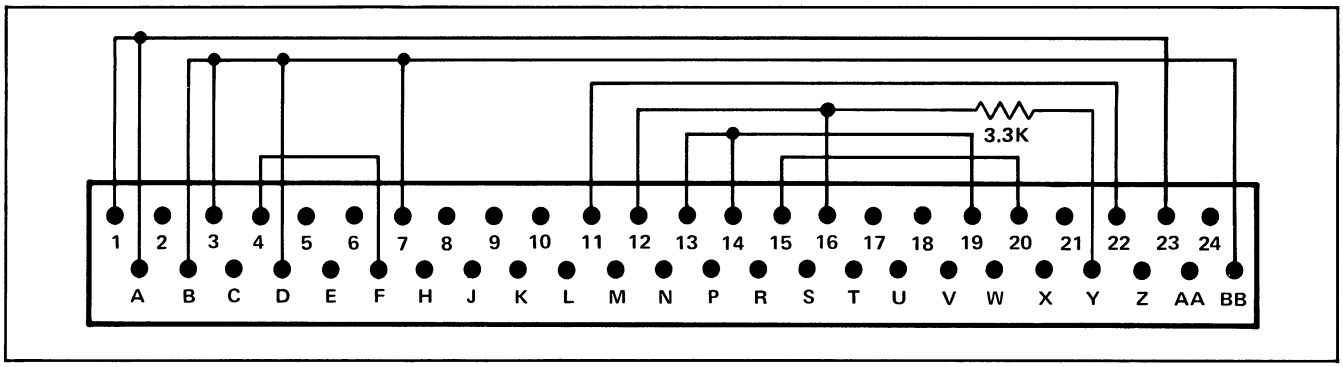


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Figure 5-1. Test Connector Wiring Diagram

Table 5-1. Test Connector Signal Information

IOBO BIT	CARD OUTPUT SIGNALS EIA STANDARD CIRCUIT	NAME	TEST CONNECTOR PINS	CARD INPUT SIGNALS EIA STANDARD NAME	CIRCUIT	IOBI BIT
10	SBA	Secondary Data Send	14 — 19 13	Secondary Data Receive Serial Data Input	SBB BB	14
13	CA	Request-to-Send	16 — 12	Clear-to-Send	CB	–
14	CD	Data Terminal Ready	20 — 15	Ringing	CE	10
–	–	Internal Clock	1 — 23 A	Data Set Ready	CC	12
–	BA	Serial Data Output	11 — 22	Carrier Detect	CF	11
–	–	Internal Oscillator	4 — F	Programmable Scaler	–	–
–	–	Ground	BB — B 3 D 7	Programmable Scaler Preset (1200 bits/sec)	–	–

Note

Figure 5-2 is for an interface card operating with jumper W2 in position B (only one stop bit at the end of the character bit stream). If two stop bits were selected (W2 in position A), the N-Zero FF output would coincide with the last stop bit.

f. Switch bits 0 through 7 of computer switch register off and on, one at a time, and check resulting waveform. Each waveform bit should be near -6 volts when respective switch register bit is in the logic 1 (on) position.

g. Halt computer. Change control word located at address 105 (octal) to indicate a character bit stream of six bits (120012 octal). Return to address 100 (octal) and press RUN switch.

h. Switch bits 0 through 7 of computer switch register off and on again and check that only bits 0 through 5 change the waveform.

5-11. TIMING DIAGRAMS.

5-12. Figures 5-3 and 5-4 contain general timing diagrams for typical transmission and reception of a character bit stream. Figures 5-5 through 5-13 contain detailed timing diagrams of the interface card for the following operations. (Refer to theory of operation section for a detailed circuit description.)

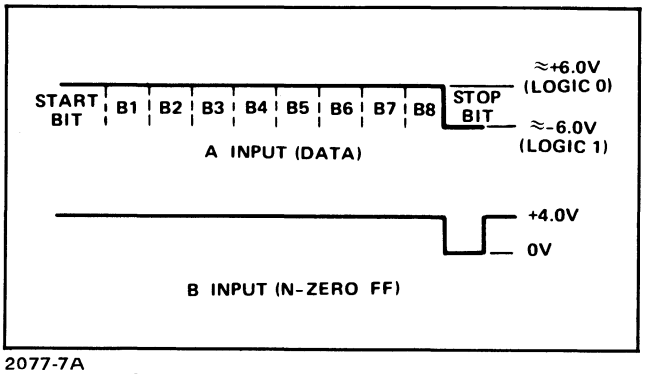

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Figure 5-2. Test Program Waveform

a. Operation in the transmit mode with the bit register/counter at the count of "1" (figure 5-5).

b. Output a control word that sets the interface card for the transmit mode of a character bit stream consisting of eight bits (figure 5-6).

c. Initial power on (figure 5-7).

d. Operation in the transmit mode with the bit register/counter at the count of "2" (jumper W2 in position A) (figure 5-8).

e. Output data (figure 5-9).

f. Operation in the justify cycle with the bit register/counter at the count of "0" (figure 5-10).

Table 5-2. Interconnecting Cable Pin Index

25-PIN CONNECTOR	48-PIN CONNECTOR	EIA STANDARD RS-232-B CIRCUIT	SIGNAL NAME
1	BB	AA	Protective Ground
2	11	BA	Transmit Data
3	13	BB	Receive Data
4	16	CA	Request-to-Send
5	12	CB	Clear-to-Send
6	23	CC	Data Set Ready
7	24	AB	Signal Ground
8	22	CF	Carrier Detect
11	14	SBA	Secondary (Supervisory) Data Send
12	19	SBB	Secondary (Supervisory) Data Receive
20	20	CD	Data Terminal Ready
22	15	CE	Ringing
Pins 1, 3, 4, 6, 7, A, B, C, D, F, H, and J on the 48-pin connector are used as jumper tiepoints for various interface card functions. They do not connect to pins on the 25-pin connector. All other pins are unused.			

g. Output a control word that sets the interface card for the receive mode of a character bit stream consisting of eight bits (figure 5-11).

h. Receive data (figure 5-12).

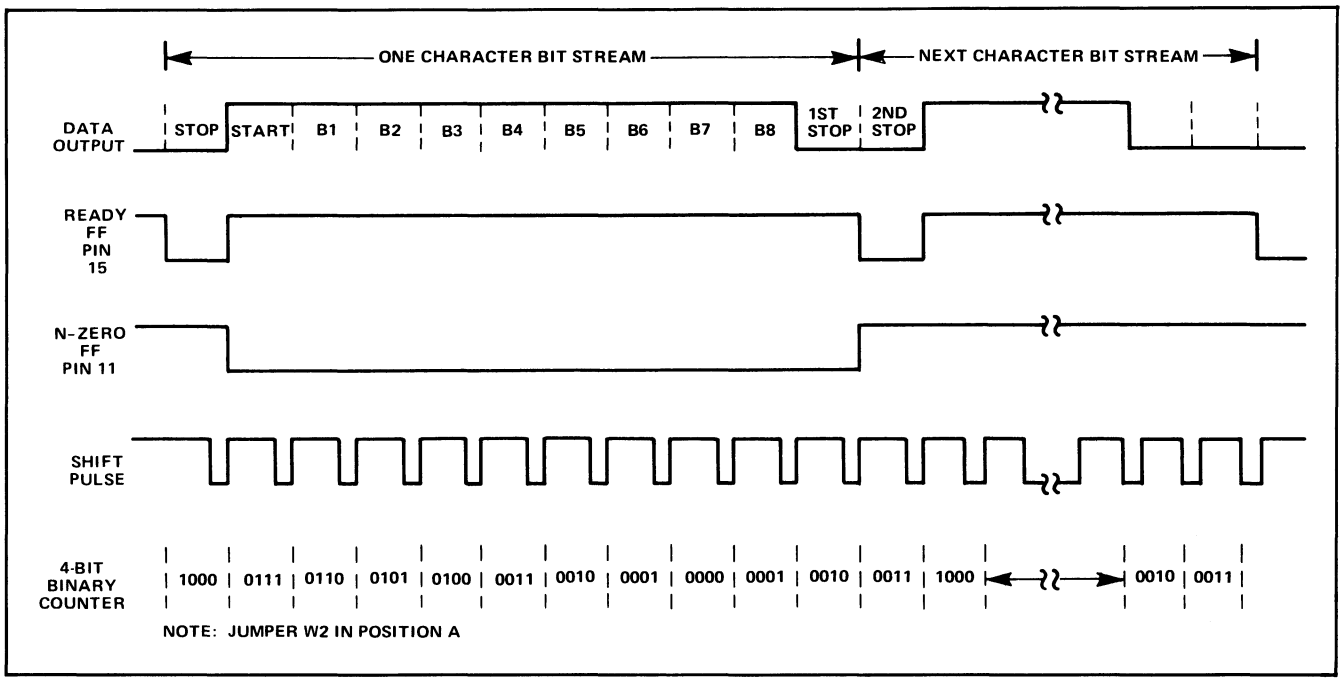
i. Operation in the receive mode with the bit register/ counter at the count of "1" (figure 5-13).

5-13. LOGIC EQUATIONS.

5-14. A list of logic equations for each flip-flop on the interface card is shown in table 5-4. These equations may be used along with the integrated circuit information (figure 5-14), the logic and parts location diagrams (figure 5-15), and the replaceable parts list for the card (table 5-5) for maintenance purposes. The parts in table 5-5 are in order of reference designation.

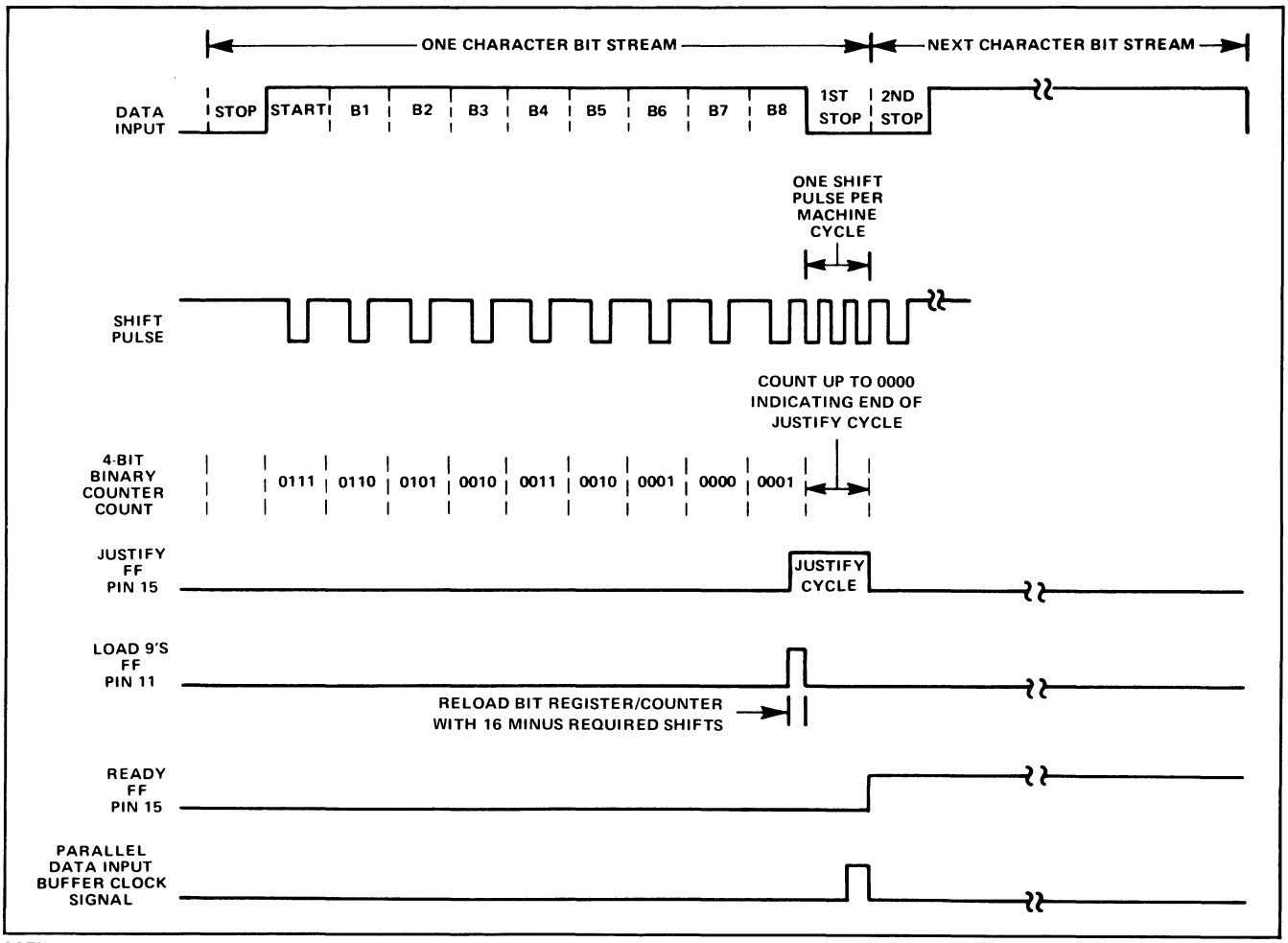
Table 5-3. Test Program

LABEL	OPERATING CODE	OPERAND	REMARKS	
			ADDRESS (OCTAL)	MACHINE CODE INSTRUCTION (OCTAL)
	LDA	CW	100	060105
	OTA	10	101	102610
LOOP	LIA	01	102	102501
	OTA	10	103	102610
	JMP	LOOP	104	026102
CW	Control Word		105	120010
NOTE: The test program assumes the interface card is located in the slot corresponding to select code 10.				



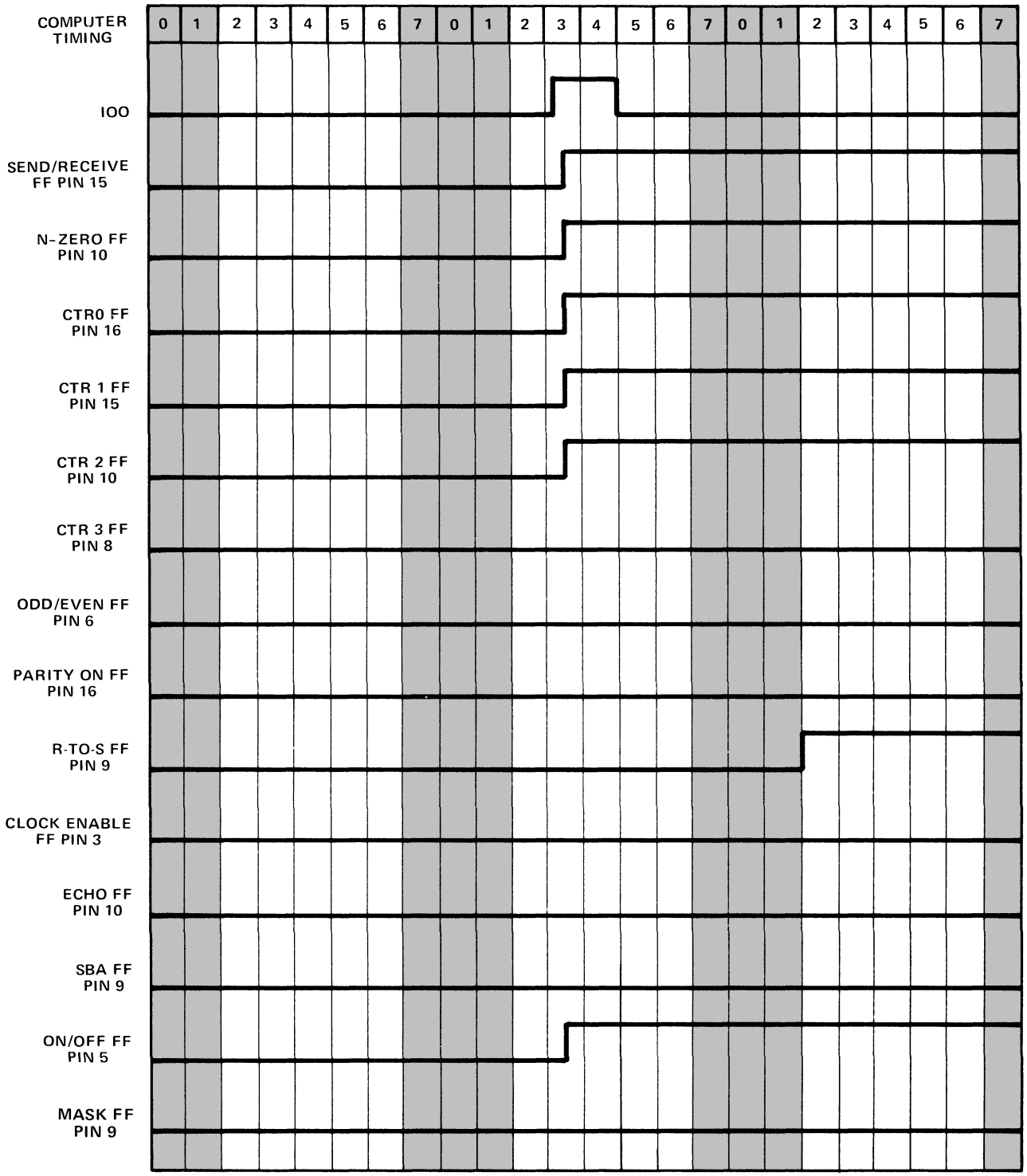
2077-8

Figure 5-3. Timing Diagram for Transmission of a Character Bit Stream



2077-9

Figure 5-4. Timing Diagram for Reception of a Character Bit Stream

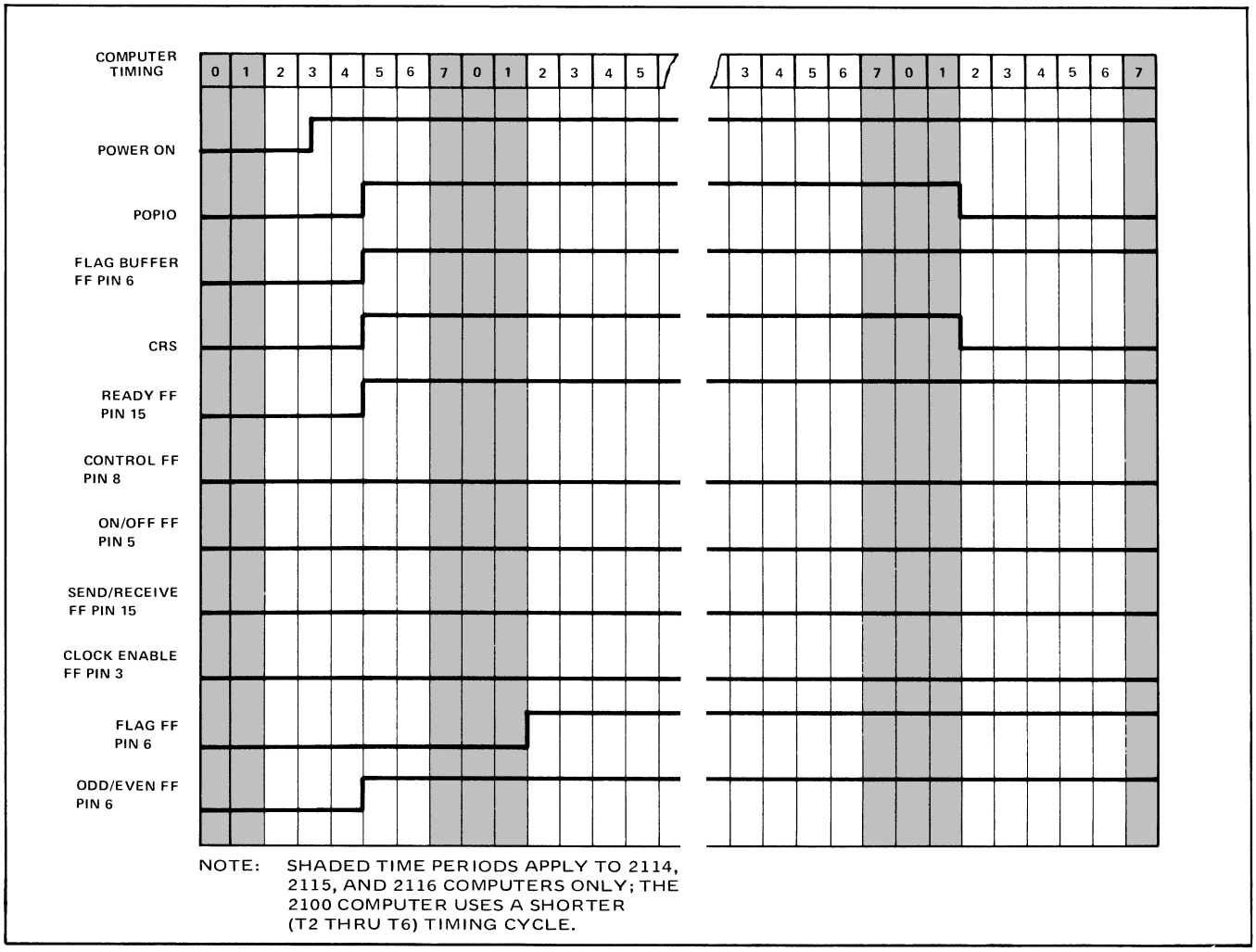


NOTES:

1. CONTROL WORD IS 160010 (OCTAL).
2. SHADED TIME PERIODS APPLY TO 2114, 2115, AND 2116 COMPUTERS ONLY; THE 2100 COMPUTER USES A SHORTER (T2 THRU T6) TIMING CYCLE.

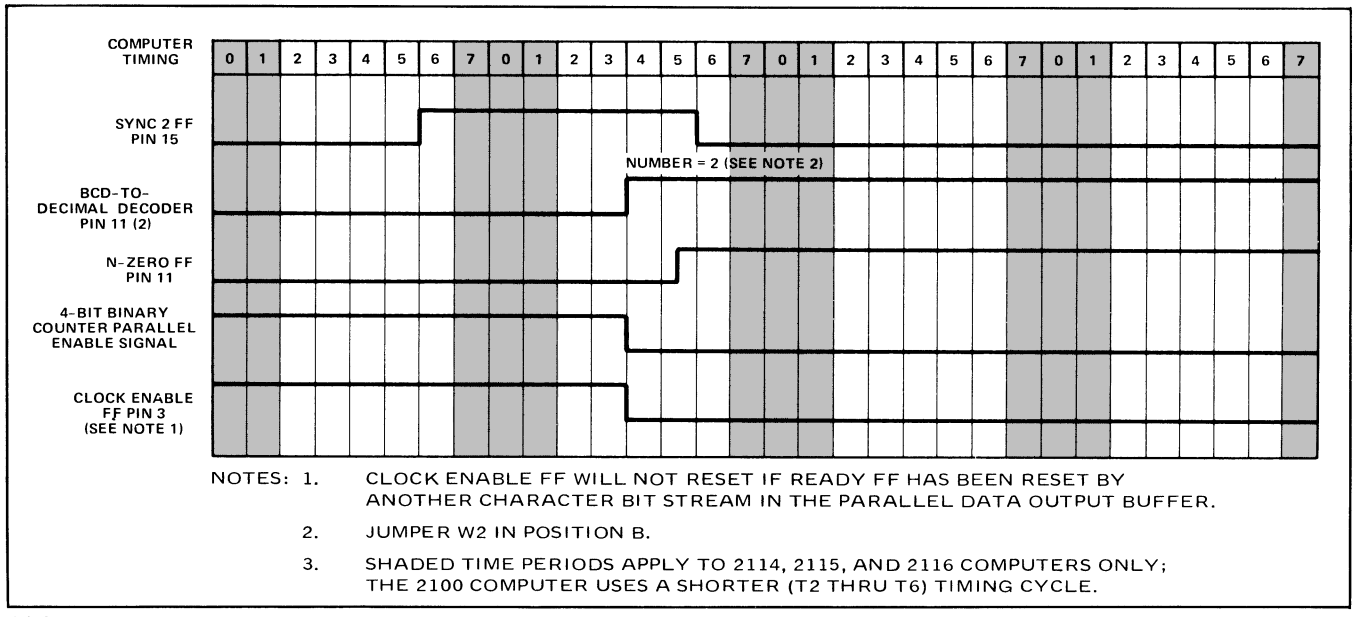
REF. 2077-11

Figure 5-5. Timing Diagram for a Control Word to Transmit Data



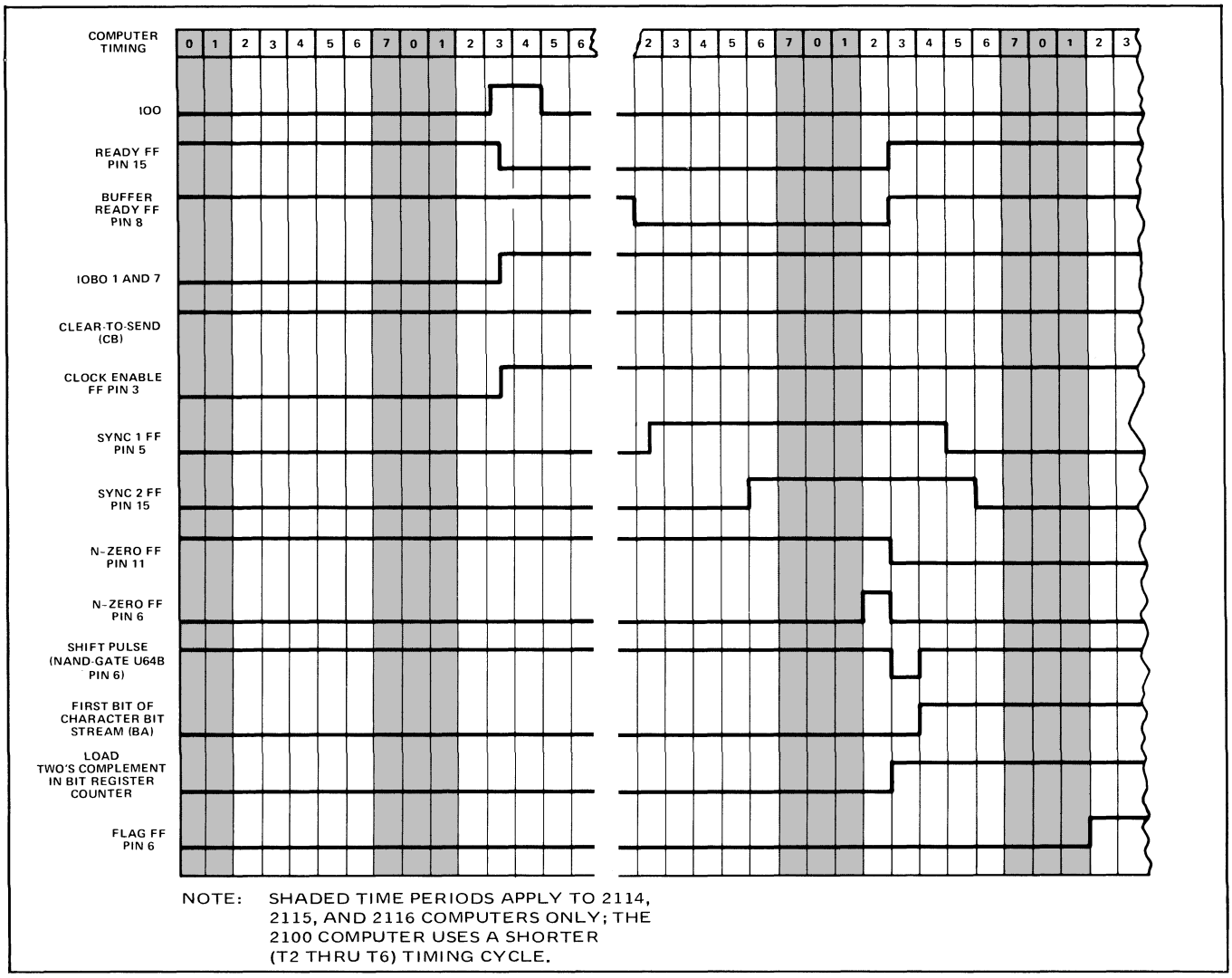
REF. 2077-10

Figure 5-6. Timing Diagram for an Initial Power-On Sequence



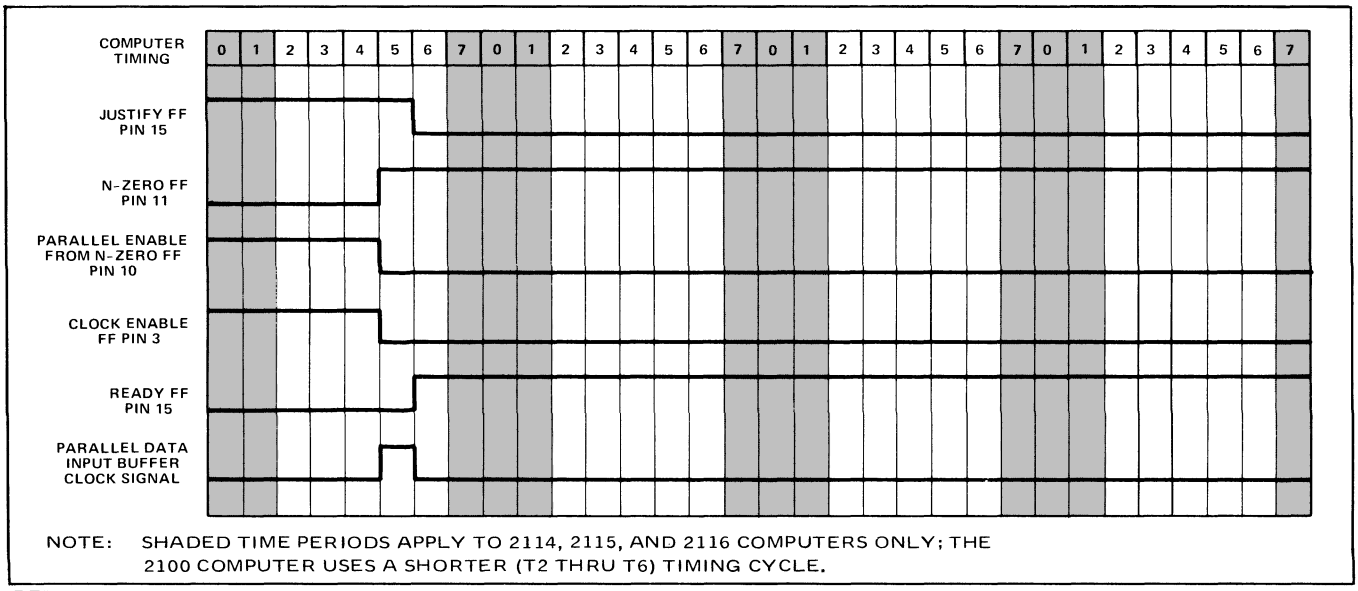
REF. 2077-14

Figure 5-7. Timing Diagram for the Transmit Mode with the Bit Register/Counter at the Count of "2"



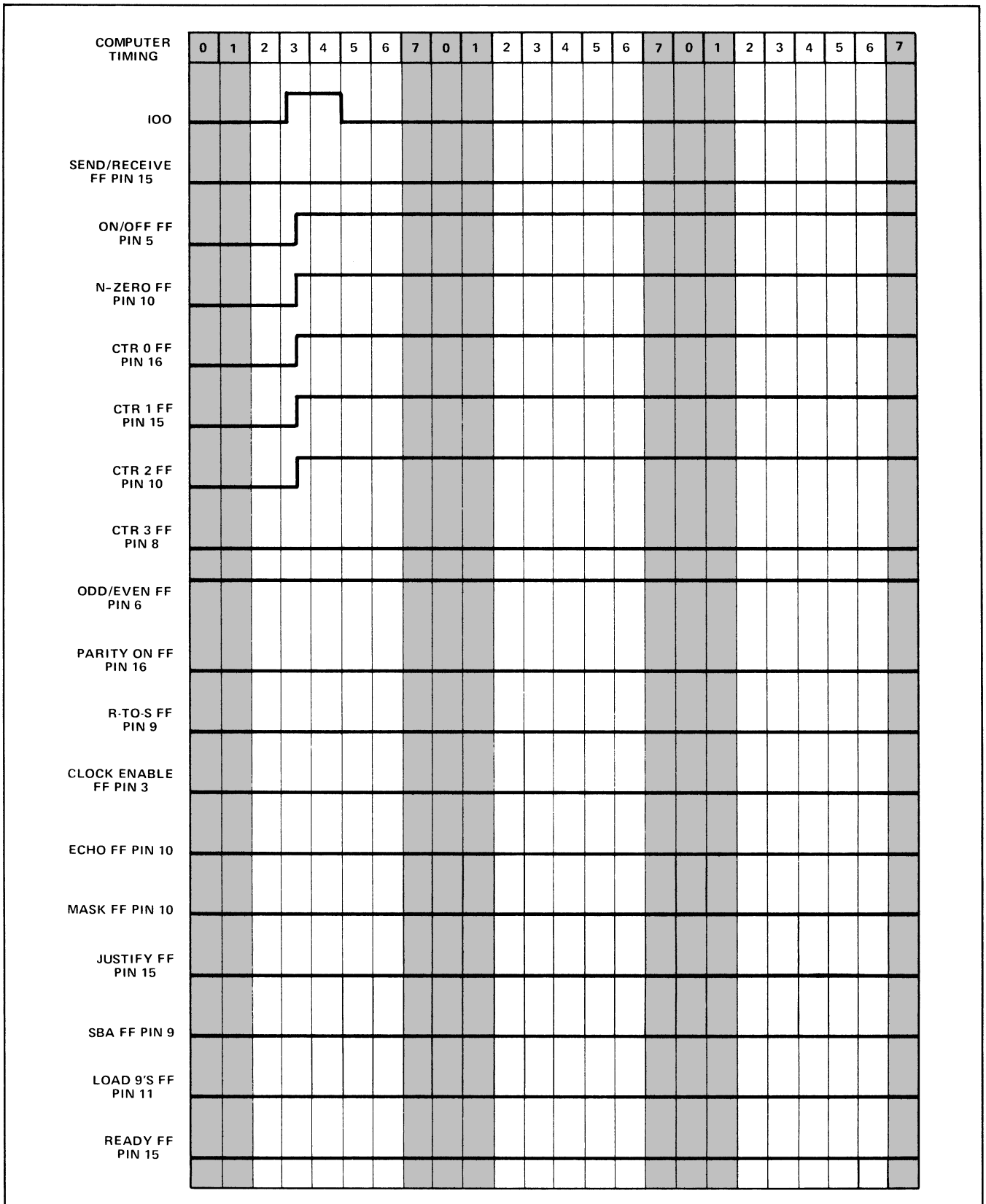
REF. 2077-12

Figure 5-8. Timing Diagram for Transmitting Data



REF. 2077-18

Figure 5-9. Timing Diagram for the Justify Cycle with the Bit Register/Counter at the Count of "0"

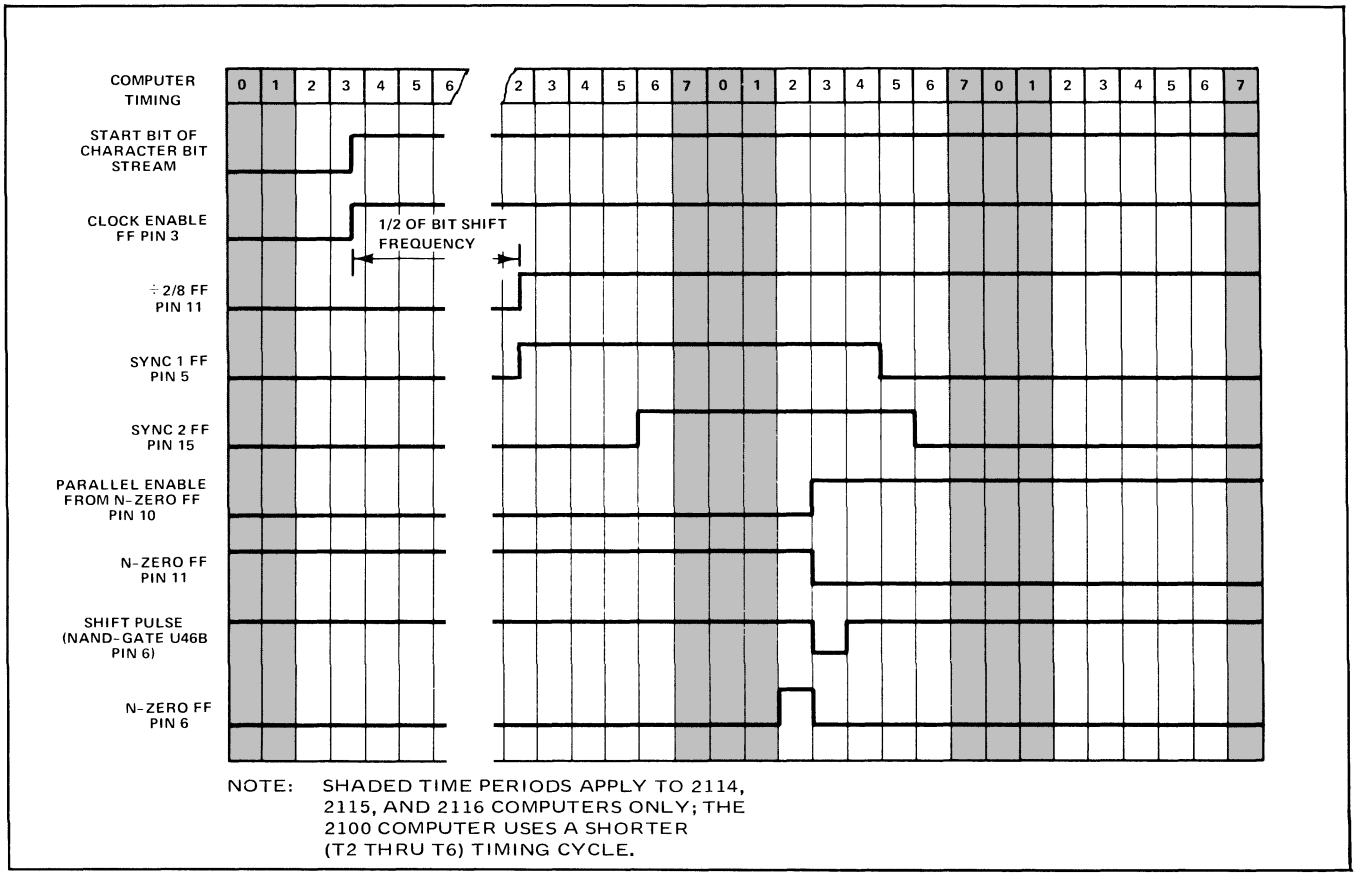


NOTES: 1. CONTROL WORD IS 140010 (OCTAL).

2. SHADED TIME PERIODS APPLY TO 2114, 2115, AND 2116 COMPUTERS ONLY; THE 2100 COMPUTER USES A SHORTER (T2 THRU T6) TIMING CYCLE.

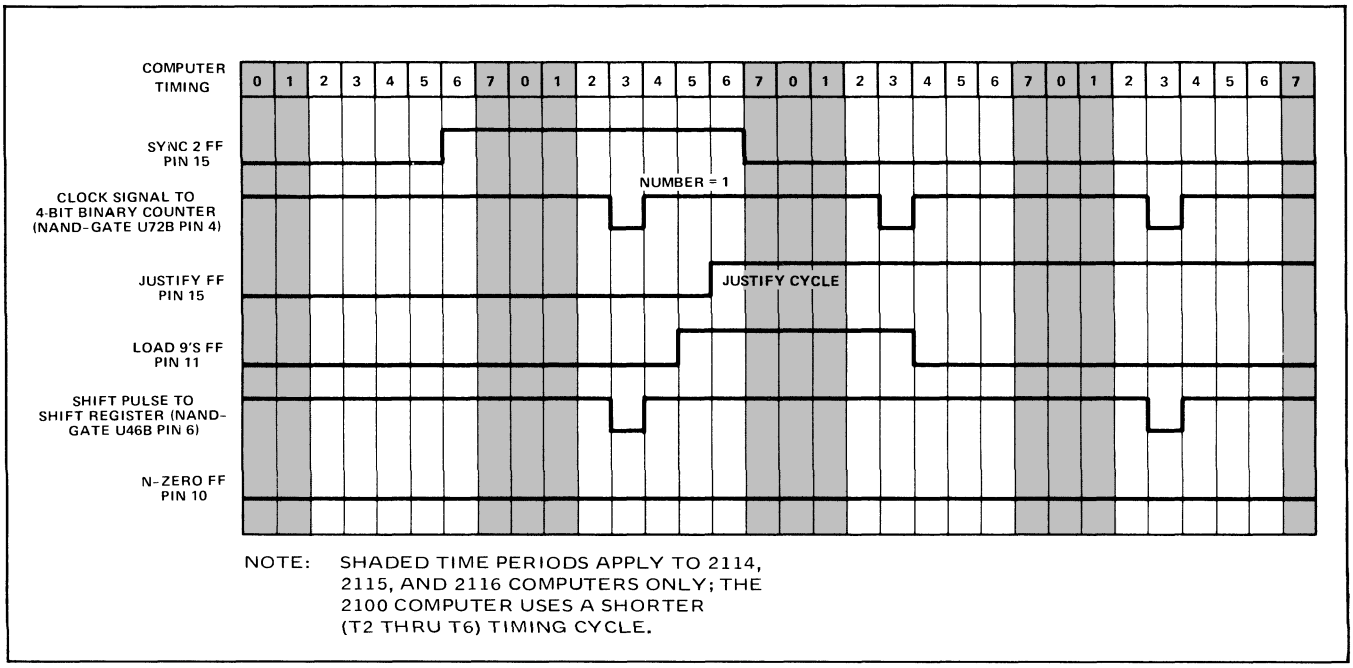
REF. 2077-15

Figure 5-10. Timing Diagram for a Control Word to Receive Data



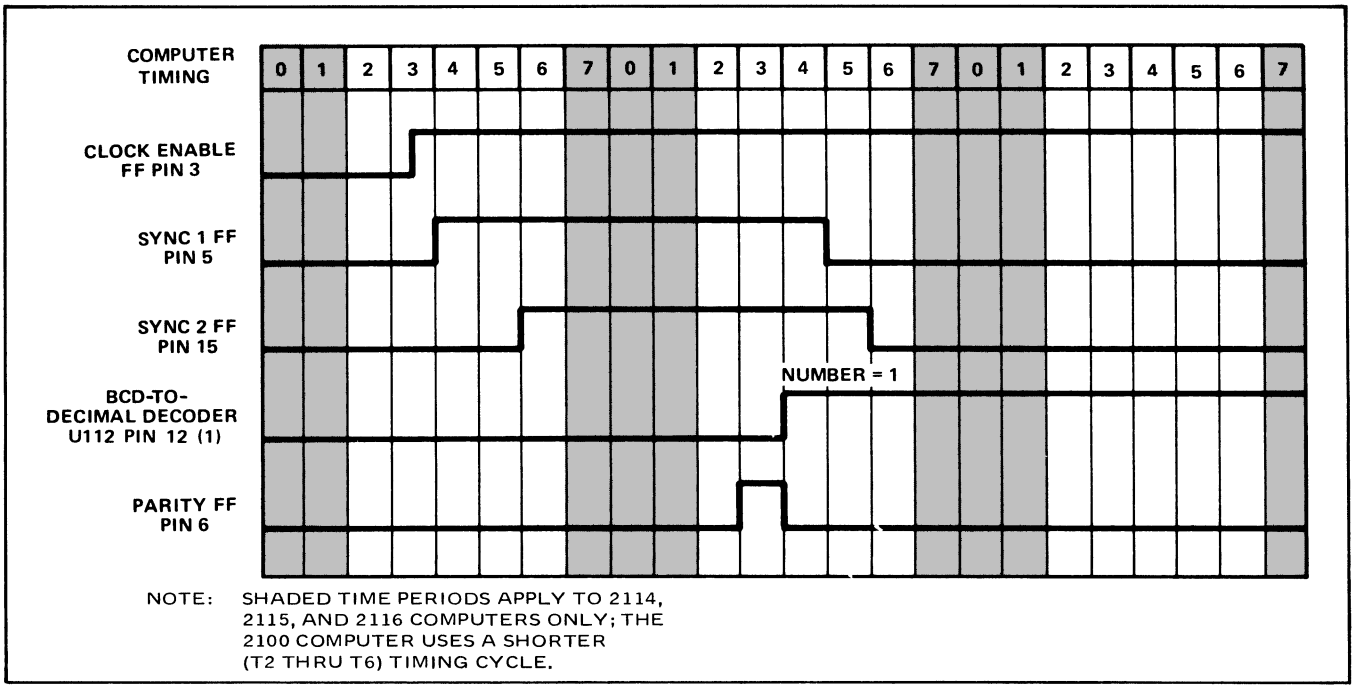
REF. 2077-16

Figure 5-11. Timing Diagram for Receiving Data



REF. 2077-17

Figure 5-12. Timing Diagram for the Receive Mode with the Bit Register/Counter at the Count of "1"



REF. 2077-13A

Figure 5-13. Timing Diagram for the Transmit Mode with the Bit Register/Counter at the Count of "1"

Table 5-4. Logic Equations

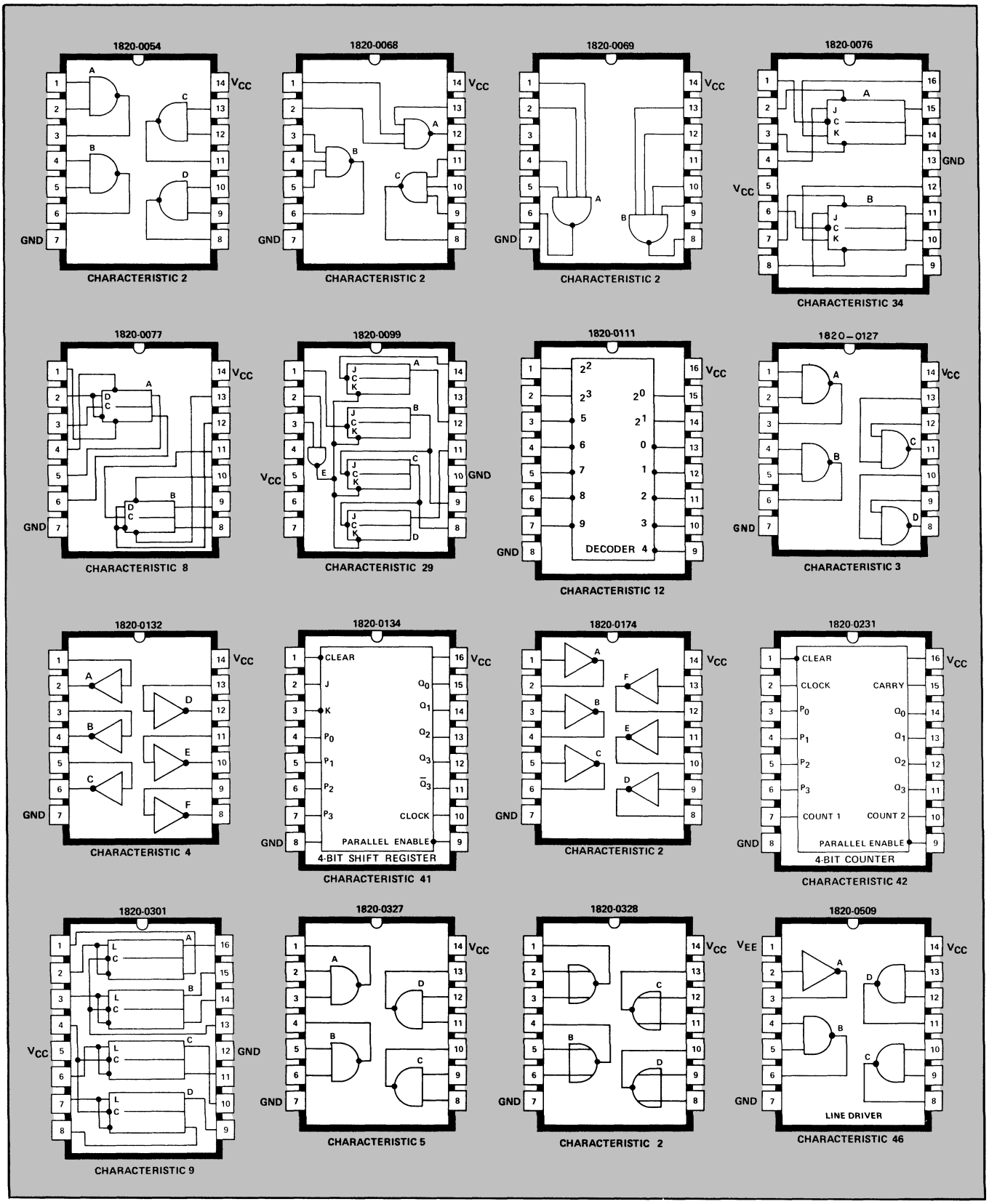
FLIP-FLOP	EQUATION
Buffer Ready FF	Set = Ready FF Clear = ENF
Clock Enable FF	Set = [R-to-S FF · ($\overline{\text{Ready FF}}$ · Clear-to-Send)] + (Receive Data · $\overline{\text{R-to-S FF}}$) Clear = CRS + BCD-to-Decimal Decoder + [Justify FF · (BCD-to-Decimal Decoder · SIR)]
Control FF	Set = STC · (LSCM · IOGB · LSCL) Clear = CLC · (LSCM · IOGB · LSCL) + CRS
CTR 0 FF	Data = IOBO 0 Clock = CRS + {IOBO 15 · [IOO · (LSCM · IOGB · LSCL)]}
CTR 1 FF	Data = IOBO 1 Clock = CRS + {IOBO 15 · [IOO · (LSCM · IOGB · LSCL)]}
CTR 2 FF	Data = IOBO 2 Clock = CRS + {IOBO 15 · [IOO · (LSCM · IOGB · LSCL)]}
CTR 3 FF	Data = IOBO 3 Clock = CRS + {IOBO 15 · [IOO · (LSCM · IOGB · LSCL)]}
÷2 FF	J = +4.5V K = +4.5V Clock = Clock Enable FF · Oscillator Frequency
÷4 FF	J = +4.5V K = +4.5V Clock = ÷ 2 FF
÷ 2/8 FF	÷ 8 = Clock Enable FF · Oscillator Frequency (Jumper W1 in Position A) ÷ 2 = ÷ 4 FF Clear = Clock Enable FF
Echo FF	Data = IOBO 9 Clock = IOBO 15 · [IOO · (LSCM · IOGB · LSCL)]
8-Bit Shift Register	Parallel Data = Parallel Data Input Buffer · Parallel Enable · Clock Serial Data = Serial In FF · Parallel Enable · Clock Parallel Enable = $\overline{\text{N-Zero FF}}$ Clock = $\overline{\text{Load 9's FF}}$ · {[(Sync 2 FF · T3B) + (T3B · Justify FF)] + [$\overline{\text{N-Zero FF}}$ · (Sync 2 FF · ENF)] · R-to-S FF}
Error FF	Data = ($\overline{\text{Odd/Even FF}}$ · Parity FF) + (Odd/Even FF · $\overline{\text{Parity FF}}$) Clock = Parity On FF · (Justify FF · BCD-to-Decimal Decoder · SIR) Direct Set = IOBO 15 · [IOO · (LSCM · IOGB · LSCL)] Direct Clear = Ready FF · (Justify FF · BCD-to-Decimal Decoder · SIR)
Flag FF	Set = Flag Buffer FF · ENF Clear = CLF

Table 5-4. Logic Equations (Continued)

FLIP-FLOP	EQUATION
Flag Buffer FF	Set = POPIO + [STF · (LSCM · IOGB · LSCL)] + [$\overline{\text{Flag FF}}$ · (ENF · Ringing FF)] Clear = CLF · (LSCM · IOGB · LSCL)
4-Bit Binary Counter	Two's Complement = ($\overline{\text{Justify FF}}$ · CTR 0 FF thru CTR3 FF) · $\overline{\text{Parallel Enable}}$ · Clock Justify cycle = (Justify FF · CTR 0 FF thru CTR 3 FF) · $\overline{\text{Parallel Enable}}$ · Clock Parallel Enable = N-Zero FF + (Load 9's FF · Justify FF) Clock = {[N-Zero FF + (Load 9's FF · Justify FF)] · SIR} + [(Sync 2 FF · T3B) + (T3B · Justify FF)]
IRQ FF	Set = PRH · SIR · [Flag Buffer FF · (Flag FF · IEN · Control FF)] Clear = ENF
Justify FF	J = $\overline{\text{R-to-S FF}}$ · BCD-to-Decimal Decoder No. 1 K = $\overline{\text{R-to-S FF}}$ · BCD-to-Decimal Decoder No. 1 Clock = SIR Direct Clear = IOBO 15 · [IOO · (LSCM · IOGB · LSCL)]
Load 9's FF	J = GND K = Load 9's FF Clock = T3B Direct Set = ($\overline{\text{R-to-S FF}}$ · BCD-to-Decimal Decoder No. 1) · SIR Direct Clear = IOBO 15 · [IOO · (LSCM · IOGB · LSCL)]
Mask FF	Data = IOBO 12 Clock = IOBO 15 · [IOO · (LSCM · IOGB · LSCL)]
N-Zero FF	J = GND K = N-Zero FF Clock = N-Zero FF · (ENF · Sync 2 FF) Direct Set = $\overline{\text{Clock Enable FF}}$
Odd/Even FF	Data = IOBO 7 Clock = CRS + {IOBO 15 · [IOO · (LSCM · IOGB · LSCL)]}
On/Off FF	Data = IOBO 14 Clock = IOBO 15 · [IOO · (LSCM · IOGB · LSCL)] Direct Clear = CRS
Parallel Data Input Buffer	Data = 8-Bit Shift Register Clock = Justify FF · (BCD-to-Decimal Decoder · SIR)
Parallel Data Output Buffer	Data = IOBO 0 thru IOBO 7 Clock = $\overline{\text{IOBO 15}}$ · [IOO · (LSCM · IOGB · LSCL)]
Parity FF	* J = +4.5V K = +4.5V Clock = Sync 2 FF · T3B Direct Clear = N-Zero FF

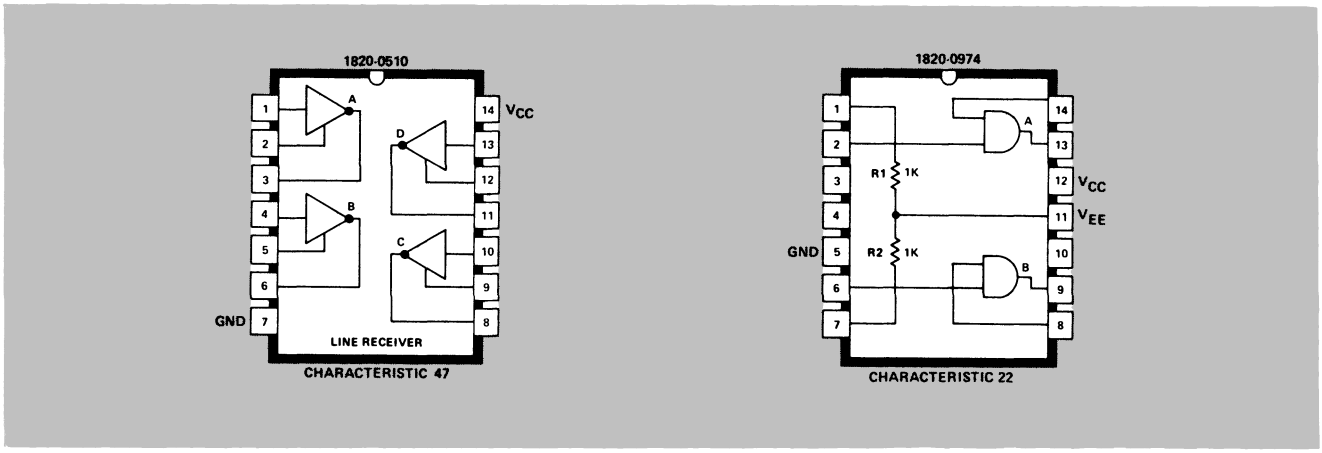
Table 5-4. Logic Equations (Continued)

FLIP-FLOP	EQUATION
Parity On FF	Data = IOBO 8 Clock = IOBO 15 · [IOO · (LSCM · LOGB · LSCL)]
Ready FF	J = $\overline{\text{Ready FF}}$ K = GND Clock = {R-to-S FF · [N-Zero FF · (ENF · Sync 2 FF)]} + {R-to-S FF · [Justify FF · (BCD-to-Decimal Decoder · SIR)]} Direct Set = POPIO Direct Clear = R-to-S FF · [$\overline{\text{IOI}}$ + ($\overline{\text{LSCM}}$ + $\overline{\text{IOGB}}$ + LSCL)] + R-to-S FF · {$\overline{\text{IOBO}}$ 15 · [IOO · (LSCM · IOGB · LSCL)] }
Ringing FF	Data = + 4.5V Clock = CE Amplifier Direct Clear = CLF · (LSCM · IOGB · LSCL)
R-To-S FF	Data = Send/Receive FF Clock = ENF • $\overline{\text{Clock Enable FF}}$ Direct Clear = CRS
SBA FF	Data = IOBO 10 Clock = IOBO 15 · [IOO · (LSCM · IOGB · LSCL)]
Send/Receive FF	Data = IOBO 13 Clock = IOBO 15 · [IOO · (LSCM · IOGB · LSCL)]
Serial In FF	Data = Receive Data · $\overline{\text{R-to-S FF}}$ Clock = $\overline{\text{Load 9's FF}}$ · {[(Sync 2 FF · T3B) + (T3B · Justify FF)] + [$\overline{\text{N-Zero FF}}$ · (Sync 2 FF · ENF)] · R-to-S FF} Direct Set = R-to-S FF
Start Bit FF	Data = 8-Bit Shift Register Clock = Sync 2 FF · T3B Direct Clear = N-Zero FF
Stop Bit FF	Data = Start Bit FF Clock = Sync 2 FF · T3B Direct Set = N-Zero FF
Sync 1 FF	Data = + 4.5V Clock = ÷2/8 FF ÷ (R-to-S FF + $\overline{\text{R-to-S FF}}$) Direct Clear = Sync 2 FF · SIR
Sync 2 FF	J = Sync 1 FF K = Sync 1 FF Clock = SIR



2156-6

Figure 5-14. Integrated Circuit Diagrams and Characteristics



2156-6

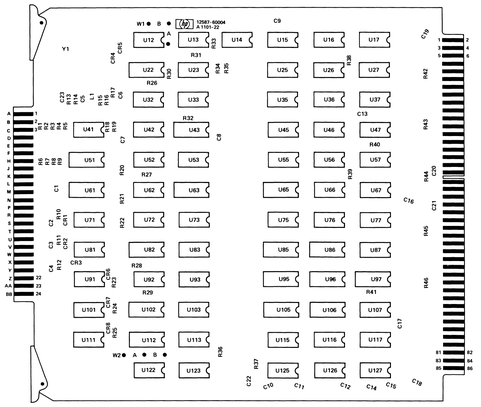
CHARACTERISTIC	INPUT LEVEL		OUTPUT LEVEL		OPEN INPUT ACTS AS:	MAXIMUM PROPAGATION DELAY	
	LOGIC 1 (VOLTS, MIN)	LOGIC 0 (VOLTS, MAX)	LOGIC 1 (VOLTS, MIN)	LOGIC 0 (VOLTS, MAX)		TO LOGIC 1 (NANOSECONDS)	TO LOGIC 0 (NANOSECONDS)
2	+2.0	+0.8	+2.4	+0.4	Logic 1	15	15
3	+2.0	+0.8	+2.4	+0.4	Logic 1	12	10
4	+1.9	+0.8	+2.4	+0.45	Logic 1	15	13
5	+2.0	+0.8	(Note 1)	+0.4	Logic 1	45	15
8	+2.0 (Note 2)	+0.8	+2.4	+0.4	Logic 1	35	50
9	+2.0 (Note 3)	+0.8	+2.4	+0.4	Logic 1	40	25
12	+2.0	+0.8	+0.4 (Note 4)	+2.4	Logic 1	35	30
22	+1.5	+0.4	+2.2	-0.3	Logic 0	24	24
29	+2.0	+0.8	+2.4	+0.4	Logic 1	135	135
34 (Note 5)	+2.0	+0.8	+2.4	+0.4	Logic 1	30	45
41	+1.7	+0.9	+2.4	+0.4	–	–	–
42	+1.4	+0.8	+2.4	+0.4	Logic 1	14	14
46	+1.9	+0.8	+6.0	-6.0	Logic 1	50	25
47	+3.0	-3.0	+2.6	+0.45	–	90	80

NOTES:
1. Depends on load.
2. Required pulse width of 30 nanoseconds minimum.
3. Required pulse width of 30 nanoseconds minimum (clock) and 75 nanoseconds minimum (data).
4. BCD 0 through BCD 9 only one output equals zero; BCD greater than 9 allows all outputs to equal one.
5. Required pulse width of 20 nanoseconds minimum.

Figure 5-14. Integrated Circuit Diagrams and Characteristics (Continued)

Table 5-5. Interface Card Replaceable Parts

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C1 thru C5	0150-0050	Capacitor, Fxd, Cer, 1000 pF, +80 -20%, 1000 VDCW	28480	0150-0050
C6	0160-2055	Capacitor, Fxd, Cer, 0.01 uF, +80 -20%, 100 VDCW	28480	0150-0093
C7,8	0160-0153	Capacitor, Fxd, My, 0.001 uF, 10%, 200 VDCW	56289	192P10292-PTS
C9 thru C12, C14 thru C21	0180-0291	Capacitor, Fxd, Elect, 1.0 uF, 10%, 35 VDCW	56289	150D105X9035-A2-DYS
C13	0160-2307	Capacitor, Fxd, Mica, 47 pF, 5%, 300 VDCW	28480	0160-2307
C22	0160-2139	Capacitor, Fxd, Cer, 220 pF, +80 -20%, 1000 VDCW	28480	0160-2139
C23	0160-2143	Capacitor, Fxd, Cer, 0.002 uF, +80 -20%, 1000 VDCW	28480	0160-2143
CR1 thru CR3, CR6 thru CR8	1901-0159	Diode, Si, 0.75A, 200 PIV	28480	1901-0158
CR4,CR5	1901-0040	Diode, Si, 30 mA, 30 WV	07263	FDG 1088
L1	9100-1639	Coil, Fxd, RF, 150 uH, 5%	82142	15-1315-16J
R1 thru R4, R6 thru R9	0698-7248	Resistor, Fxd, Flm, 3.16k, 5%, 1/8W	28480	0698-7248
R5, R10 thru R12, 14,15,18,19, R21 thru R29, R31 thru R37, R39 thru R41	0757-0280	Resistor, Fxd, Flm, 1k, 1%, 1/8W	28480	0757-0280
R13,16	0698-7242	Resistor, Fxd, Flm, 1.78k, 2%, 1/8W	28480	0698-7242
R17	0698-4241	Resistor, Fxd, Flm, 270 ohms, 5%, 1/8W	28480	0698-4241
R20,30	0698-4245	Resistor, Fxd, Flm, 348 ohms, 1%, 1/8W	28480	0698-4245
R38	0698-3445	Resistor, Fxd, Flm, 348 ohms, 1%, 1/8W	28480	0698-3445
R42 thru R46	1810-0020	Resistor, Network (7 fxd flm resistors)	28480	1810-0020
U12,26,27,35,45,46,62,67,93	1820-0054	Integrated Circuit, TTL	01295	SN7400N
U13,33,42,52,72,73,92,103	1820-0327	Integrated Circuit, TTL	01295	SN7401N
U14 thru U17, 107,115,116,117, U125 thru U127	1820-0974	Integrated Circuit, CTL	28480	1820-0974
U22,43,63,65	1820-0076	Integrated Circuit, TTL	01295	SN7476N
U23	1820-0099	Integrated Circuit, TTL	01295	SN7493N
U25,37,113	1820-0068	Integrated Circuit, TTL	01295	SN7410N
U32,56,83,122	1820-0328	Integrated Circuit, TTL	01295	SN7402N
U36	1820-0069	Integrated Circuit, TTL	01295	SN7420N
U41	1820-0127	Integrated Circuit, TTL	07263	U6A900259X
U47,55,57,75,123	1820-0132	Integrated Circuit, TTL	07263	U6A901659X
U51,61,102	1820-0231	Integrated Circuit, TTL	07263	U6B931659X
U53,66,76,77,87	1820-0077	Integrated Circuit, TTL	01295	SN7474N
U71,111	1820-0174	Integrated Circuit, TTL	01295	SN7404N
U81	1820-0509	Integrated Circuit, DTL	04713	MC1488L
U82,85,86,97,105,106	1820-0301	Integrated Circuit, TTL	01295	SN7475N
U91,101	1820-0510	Integrated Circuit, DTL	04713	MC1489L
U95,96	1820-0134	Integrated Circuit, TTL	07263	U6B930059X
U112	1820-0111	Integrated Circuit, TTL	07263	U6B930159X
W1,2	8159-0005	Jumper Wire	28480	8159-0005
XY1	1200-0199	Socket, Crystal	91506	8000-AG9
Y1	0410-0439	Crystal, Quartz	28480	0410-0439



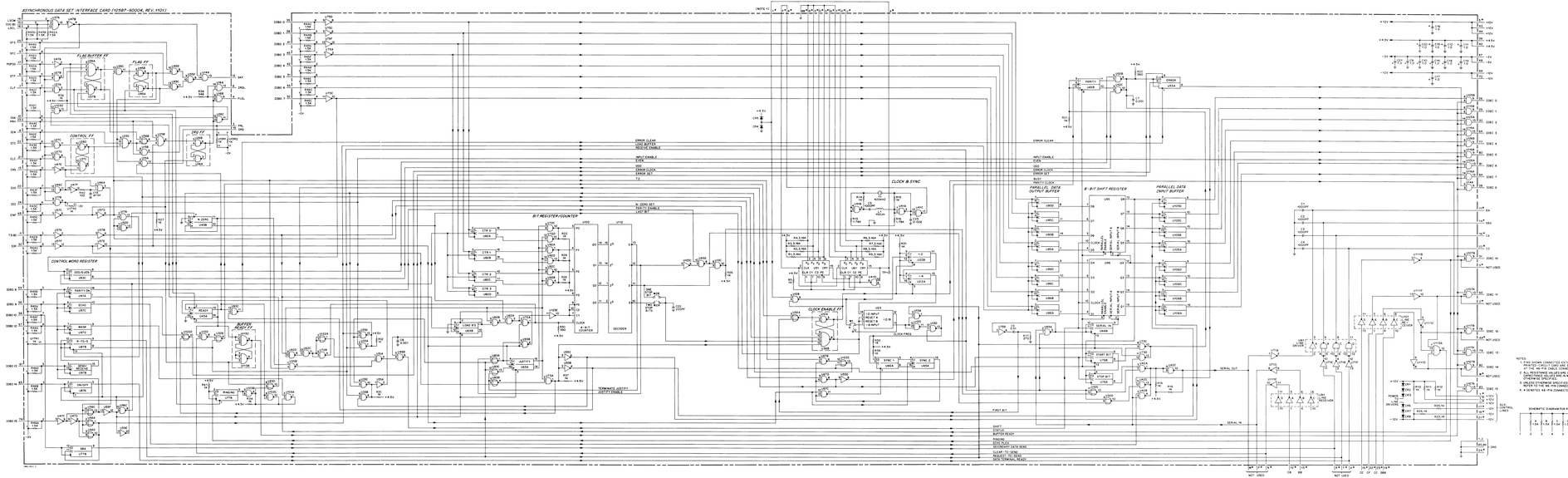


Figure 5-15. Asynchronous Data Set Printed-Circuit Card Logic and Parts Location Diagrams

SECTION VI
REPLACEABLE PARTS

6-1. INTRODUCTION.

6-2. This section contains information for ordering replacement parts for the interface kit. Table 6-1 lists parts in alphanumeric order of the HP stock numbers and lists the following information on each part:

a. Description of the part. (Refer to table 6-2 for an explanation of abbreviations and reference designations used in the DESCRIPTION column.)

b. Typical manufacturer of the part in a five-digit code; refer to list of manufacturers in table 6-3.

c. Manufacturer's part number.

d. Total quantity of each part used in the interface kit.

6-3. A separate parts list is provided along with the parts location diagram for the interface card in Section V of this manual. This parts list lists the parts in alphanumeric order of reference designations.

6-4. ORDERING INFORMATION.

6-5. To order replacement parts, address the order or inquiry to the local Hewlett-Packard Sales and Service Office. (Refer to the list at the end of this manual for addresses.) Specify the following information for each part ordered:

a. Interface Kit model number.
b. Circuit board revision number.
c. Hewlett-Packard part number for each part.
d. Description of each part.
e. Circuit reference designation.

Table 6-1. Numerical Listing of Replaceable Parts

HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	TQ
0150-0050	Capacitor, Fxd, Cer, 1000 pF, +80 -20%, 1000 VDCW	28480	0150-0050	5
0160-0153	Capacitor, Fxd, My, 0.001 uF, 10%, 200 VDCW	56289	192P10292-PTS	2
0160-2055	Capacitor, Fxd, Cer, 0.01 uF, +80 -20%, 100 VDCW	28480	0160-2055	1
0160-2139	Capacitor, Fxd, Cer, 220 pF, +80 -20%, 1000 VDCW	28480	0160-2139	1
0160-2143	Capacitor, Fxd, Cer, 0.002 uF, +80 -20%, 1000 VDCW	28480	0160-2143	1
0160-2307	Capacitor, Fxd, Mica, 47 pF, 5%, 300 VDCW	28480	0160-2307	1
0180-0291	Capacitor, Fxd, Elect, 60 uF, 10%, 35 VDCW	56289	150D105X9035A2-DYS	15
0410-0439	Crystal, Quartz	28480	0410-0439	1
0698-3445	Resistor, Fxd, Flm, 348 ohms, 1%, 1/8W	28480	0698-3445	1
0698-4241	Resistor, Fxd, Flm, 270 ohms, 5%, 1/8W	28480	0698-4241	1
0698-4245	Resistor, Fxd, Flm, 390 ohms, 5%, 1/8W	28480	0698-4245	2
0698-7242	Resistor, Fxd, Flm, 1.78k, 2%, 1/8W	28480	0698-7242	2
0698-7248	Resistor, Fxd, Flm, 3.16k, 5%, 1/8W	28480	0698-7248	8
0757-0280	Resistor, Fxd, Flm, 1k, 1%, 1/8W	28480	0757-0280	27
1200-0199	Socket, Crystal	91506	8000-A69	1
1810-0020	Resistor, Network, (7 fxd flm resistors)	28480	1810-0020	5
1820-0054	Integrated Circuit, TTL	01295	SN7400N	9
1820-0068	Integrated Circuit, TTL	01295	SN7410N	3
1820-0069	Integrated Circuit, TTL	01295	SN7420N	1
1820-0076	Integrated Circuit, TTL	01295	SN7476N	4
1820-0077	Integrated Circuit, TTL	01295	SN7474N	5
1820-0099	Integrated Circuit, TTL	01295	SN7493N	1
1820-0111	Integrated Circuit, TTL	07263	U6B930159X	1
1820-0127	Integrated Circuit, TTL	07263	U6A900259X	1
1820-0132	Integrated Circuit, TTL	07263	U6A901659X	5
1820-0134	Integrated Circuit, TTL	07263	U6B930059X	2
1820-0174	Integrated Circuit, TTL	01295	SN7404N	2
1820-0231	Integrated Circuit, TTL	07263	U6B931659X	3
1820-0301	Integrated Circuit, TTL	01295	SN7475N	6
1820-0327	Integrated Circuit, TTL	01295	SN7401N	8
1820-0328	Integrated Circuit, TTL	01295	SN7402N	4
1820-0509	Integrated Circuit, DTL	04713	MC 1488L	1
1820-0510	Integrated Circuit, DTL	04713	MC 1489L	2
1820-0974	Integrated Circuit, CTL	28480	1820-0974	11
1901-0040	Diode, Si, 30 mA, 30 WV	07263	FDG1088	7
1901-0159	Diode, Si, 0.75A, 200 PIV	28480	1901-0158	6
8159-0005	Jumper Wire	28480	8159-0005	2
9100-1639	Coil, Fxd, RF, 150 uH, 5%	82142	15-1315-16J	1
12587-60004	Asynchronous Data Set Transmit/Receive Card	28480	12587-60004	1
12587-60006	Interconnecting Cable Assembly	28480	12587-60006	1
12587-60009	Test Connector	28480	12587-60009	1
12587-90006	Operating and Service Manual	28480	12587-90006	1

Table 6-2. Reference Designations and Abbreviations

REFERENCE DESIGNATIONS

A	= assembly	K	= relay	TB	= terminal board
B	= motor, synchro	L	= inductor	TP	= test point
BT	= battery	M	= meter	U	= integrated circuit, non-repairable assembly
C	= capacitor	MC	= microcircuit	V	= vacuum tube, photocell, etc.
CB	= circuit breaker	P	= plug connector	VR	= voltage regulator
CR	= diode	Q	= semiconductor device other than diode or microcircuit	W	= cable, jumper
DL	= delay line	R	= resistor	X	= socket
DS	= indicator	RT	= thermistor	Y	= crystal
E	= Misc electrical parts	S	= switch	Z	= tuned cavity, network
F	= fuse	T	= transformer		
FL	= filter				
J	= receptacle connector				

ABBREVIATIONS

A	= amperes	gra	= gray	ph	= Phillips head
ac	= alternating current	grn	= green	pk	= peak
ad	= anode			p-p	= peak-to-peak
Al	= aluminum	H	= henries	pt	= point
AR	= as required	Hg	= mercury	PIV	= peak inverse voltage
adj	= adjust	hr	= hour(s)	PNP	= positive-negative-positive
assy	= assembly	Hz	= hertz	PWV	= peak working voltage
		hdw	= hardware	porc	= porcelain
B	= base	hex	= hexagon, hexagonal	posn	= position(s)
bp	= bandpass			pozi	= pozidrive
blk	= black	ID	= inside diameter		
blu	= blue	IF	= intermediate frequency		
brn	= brown	in.	= inch, inches	rf	= radio frequency
brs	= brass	I/O	= input/output	rdh	= round head
Btu	= British thermal unit	int	= internal	rmo	= rack mount only
Be Cu	= beryllium copper	incl	= include(s)	rms	= root-mean-square
		insul	= insulation, insulated	RWV	= reverse working voltage
C	= collector	impgrg	= impregnated	rect	= rectifier
cw	= clockwise	incand	= incandescent	r/min	= revolutions per minute
ccw	= counterclockwise			RTL	= resistor-transistor logic
cer	= ceramic	k	= kilo (10^3), kilohm		
cmo	= cabinet mount only			s	= second
com	= common	lp	= low pass	SB	= slow blow
crt	= cathode-ray tube			Se	= selenium
CTL	= complementary-transistor logic	m	= milli (10^{-3})	Si	= silicon
		M	= mega (10^6), megohm	scr	= silicon controlled rectifier
cath	= cathode	My	= Mylar	sil	= silver
cd pl	= cadmium plate	mfr	= manufacturer	sst	= stainless steel
Comp	= composition	mom	= momentary	stl	= steel
conn	= connector	mtg	= mounting	spcl	= special
compl	= complete	misc	= miscellaneous	spdt	= single-pole, double-throw
		Met Ox	= metal oxide	spst	= single-pole, single-throw
dc	= direct current	mintr	= miniature	semicond	= semiconductor
dr	= drive				
DTL	= diode-transistor logic	n	= nano (10^{-9})	Ta	= tantalum
depc	= deposited carbon	n.c.	= normally closed or no connection	td	= time delay
dpdt	= double-pole, double-throw			Ti	= titanium
dpst	= double-pole, single-throw	Ne	= neon	tgl	= toggle
		no.	= number	thd	= thread
E	= emitter	n.o.	= normally open	tol	= tolerance
ECL	= emitter-coupled logic	np.	= nickel plated	TTL	= transistor transistor logic
ext	= external	NPN	= negative-positive-negative		
encap	= encapsulated	NPO	= negative-positive zero (zero temperature coefficient)	U(μ)	= micro (10^{-6})
elctlt	= electrolytic				
		NSR	= not separately replaceable		
F	= farads	NRFR	= not recommended for field replacement	V	= volt(s)
FF	= flip-flop			var	= variable
flh	= flat head			vio	= violet
Flm	= film	OD	= outside diameter	VDCW	= direct current working volts
Fxd	= fixed	OBD	= order by description		
filh	= fillister head	orn	= orange	W	= watts
		ovh	= oval head	WW	= wirewound
G	= giga (10^9)	oxd	= oxide	wht	= white
Ge	= germanium			WIV	= working inverse voltage
gl	= glass	p	= pico (10^{-12})		
gnd	= ground(ed)	PC	= printed circuit	yel	= yellow

Table 6-3. Code List of Manufacturers

The following code numbers are from the Federal Supply Code for Manufacturers Cataloging Handbooks H4-1 and H4-2, and their latest supplements.

Code No.	Manufacturer	Address	Code No.	Manufacturer	Address
01295	Texas Instruments, Inc., Transistor Products Div.	Dallas, Texas	28480	Hewlett-Packard Co.	Palo Alto, Calif.
07263	Fairchild Camera & Inst. Corp. Semiconductor Div.	Mountain View, Calif.	56289	Sprague Electric Co.	North Adams, Mass.
14674	Corning Glass Works	Corning, N.Y.	80294	Bourns, Inc.	Riverside, Calif.
18324	Signetics Corp.	Sunnyvale, Calif.	91418	Radio Materials Co.	Chicago, Ill.
			91637	Dale Electronics, Inc.	Columbus, Nebr.
			95265	National Coil Co.	Sheridan, Wyo.

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The Hewlett-Packard Company certifies that this instrument was thoroughly tested and inspected and found to meet its published specifications when it was shipped from the factory. The Hewlett-Packard Company further certifies that its calibration measurements are traceable to the U.S. National Bureau of Standards to the extent allowed by the Bureau's calibration facility.

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