HONEYWELL EDP

HARDWARE BULLETIN

SERIES 200

TYPE 212-1 CENTRAL PROCESSOR ADAPTER

SUBJECT: Equipment Specifications for the Type 212-1 Central Processor Adapter Compatible with All Series 200 Central Processors

SPECIAL INSTRUCTIONS: This bulletin supersedes the Customer Information Bulletin, Number 200-54, dated May 18, 1965. References used in the text are the Honeywell Series 200 Models 200/1200/2200 Programmers' Reference Manual, Order No. 139, and the Honeywell Series 200 Model 120 Programmers' Reference Manual, Order No. 141.

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TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

EQUIPMENT SPECIFICATIONS FOR THE
TYPE 212-1 CENTRAL PROCESSOR ADAPTER

I. BASIC DEFINITION

The Type 212-1 Central Processor Adapter provides on-line communication between any two central processors having Series 200 peripheral interfaces. The central processor adapter consists of two back-to-back general-purpose peripheral adapters. As shown in Figure 1, page 2, the peripheral adapters may be separated one from another by a maximum 130 feet of cable. The Type 212-1 is compatible with all Series 200 central processors. (The Models 200/1200/2200 Programmers' Reference Manual and Model 120 Programmers' Reference Manual give comprehensive descriptions of the Series 200 central processors.)

II. DESCRIPTION OF THE TYPE 212-1

A. General

1. Interchangeable Use as an Input or Output Device

Each peripheral adapter in the Type 212-1 can be used interchangeably as an input or an output device, but both can not be used at the same time for the same function. In other words, while one side is being used as an input device, the other must be used an an output device. Since both sides are used simultaneously, each requires its independent read/write channel (RWC) and peripheral input/output device address. Each peripheral adapter is capable of storing one six-bit data character; together they transfer data at the rate of one character per six microseconds. With respect to each central processor, this transfer is completely asynchronous.

2. Accessibility to Central Processor

The Type 212-1 Central Processor Adapter is accessible to either central processor. However, its availability is on a "first-come, first-serve" basis. If both central processors request service simultaneously, both receive a device-busy signal.

The Type 212-1 operates with Series 200 central processors irregardless of whether they have the program interrupt capability; this capability is standard on all processors except the Type 201, but even here optional Feature 012 (Model 200/1200/2200 Programmers' Reference Manual, pages 1-15 and 1-16) is not required.

B. Data Transfer

Data transfer requires two phases of operation: first, the transfer of control characters between the initiating and the responding central processor; second, the transfer of data.

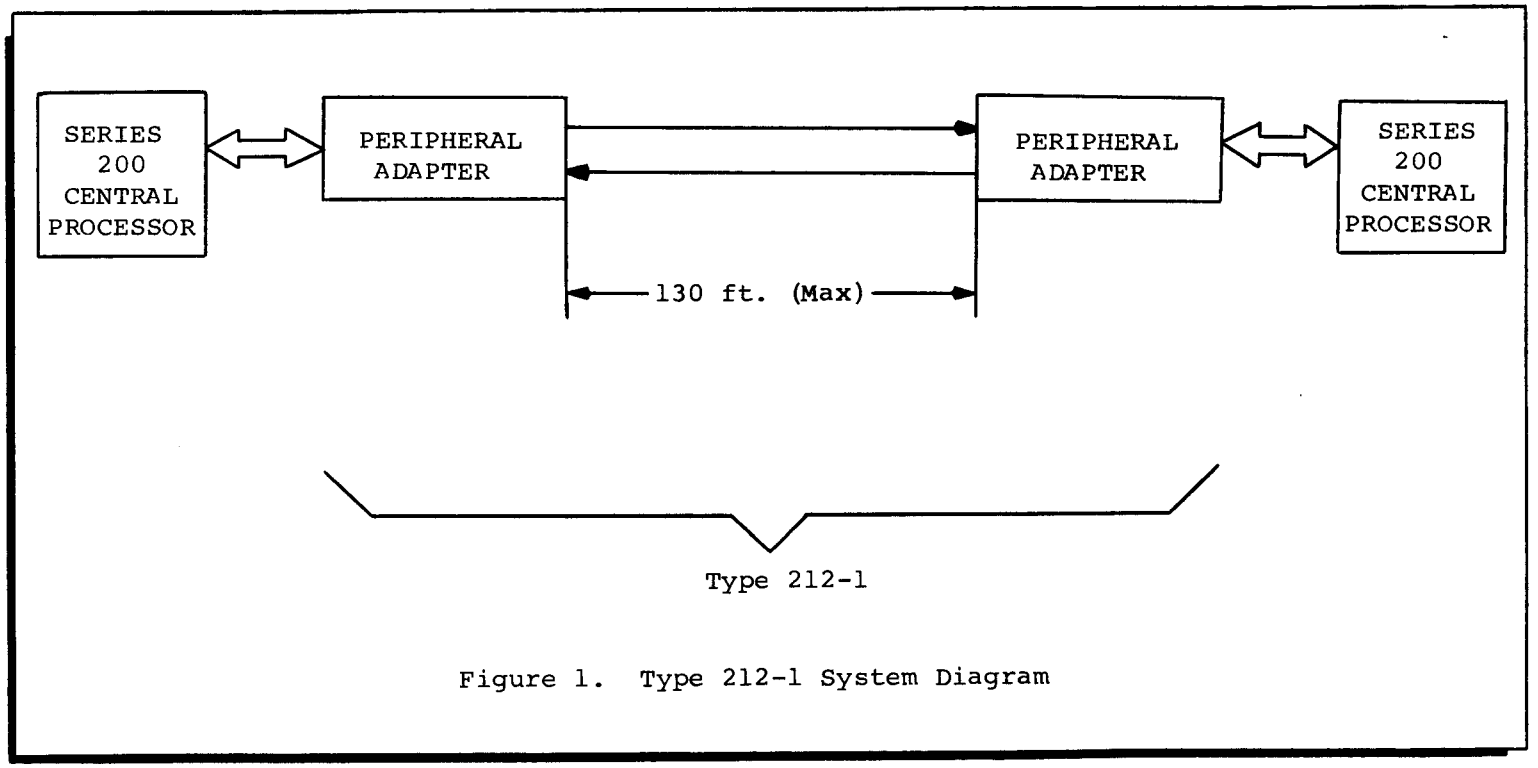


Figure 1. Type 212-1 System Diagram

1. Transfer of Control Characters

The initiating central processor issues a Peripheral Control and Branch (PCB) instruction and a Peripheral Data Transfer (PDT) instruction to the Type 212-1. The responding central processor then issues a PDT instruction to the Type 212-1. This phase ends when the Type 212-1 receives a record mark from either central processor (Section II,B,3). The record mark terminates the PDT instruction issued by the responding central processor.

The "n" control characters start at location A (the address specified in the initiating processor's PDT instruction) and end at A+(n-1). Location A+n contains a record mark. The contents of location A+n are not transferred. The next location whose contents are transferred is A+n+1.

2. Transfer of Data Characters

After the transfer of control characters, the Type 212-1 receives a second PDT instruction from the responding central processor. Data is now transferred between the two central processors. This transfer ends when the Type 212-1 receives a record mark from either central processor (Section II,B,3) terminating both PDT instructions.

The data storage area in the initiating central processor begins at location A+n+1. Data is transferred into this area or out of it depending upon the direction of data flow. The storage area is terminated by a record mark. Again, location A is the address specified in the initiating central processor's PDT instruction.

3. Data Transfer Termination

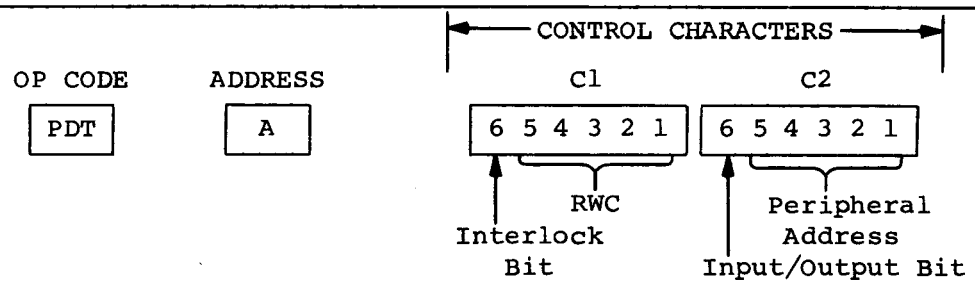
Normally, the sending central processor issues the record mark terminating data transfer. However, data transfer is also terminated if the Type 212-1 receives a record mark from the receiving central processor.

When data transfer is terminated by a record mark from the receiving central processor, the current location counter of the sending central processor may be set to either A+n+1 or A+n+2, whereas the receiver current location counter is always set to A+n+1. When data transfer is terminated by a record mark from the sending central processor, the sender's current location counter is set to A+n+1 and the receiver's current location counter is set to A+n.

III. PERIPHERAL INSTRUCTIONS

A. Peripheral Data Transfer (PDT) Instruction

This instruction causes the transfer of data from one central processor to another by way of the Type 212-1 Central Processor Adapter. Data transfer continues until a record mark is encountered. The PDT instruction format is shown below:



A Address - Memory location to which data is transferred.

Interlock Bit - zero: Memory access granted to RWC1'.

Read/Write Channel (RWC) - Selects the read/write channel between main memory and the Type 212-1.

RWC1 = 01001	RWC3 = 01011
RWC2 = 01010	RWC1'= 01101

Input/Output Bit - The input/output bit is issued by the responding central processor and controls the direction of data transfer: Input = 1, Output = 0

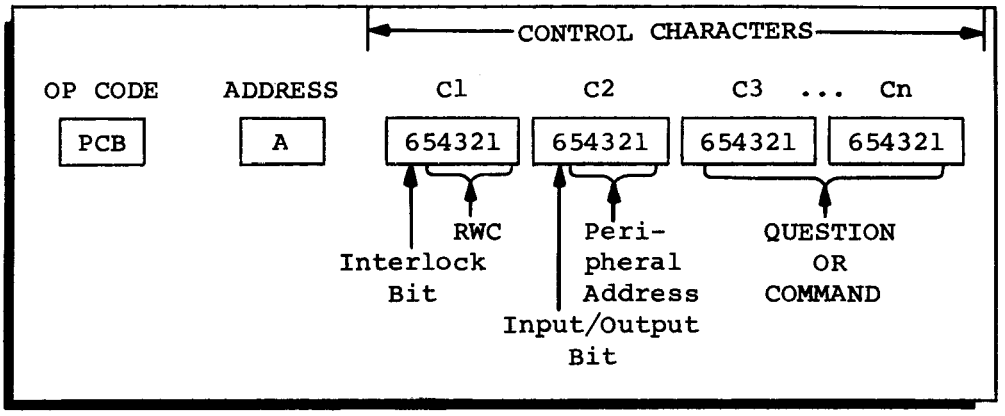
Peripheral Address - Logical address of the Type 212-1 on the peripheral bus.

NOTE

The interlock bit and the RWC allocation described in this section pertain only to the Type 201-0 and 201-1 Central Processors. For Series 200 central processors, see the appropriate programmers' reference manual.

B. Peripheral Control and Branch (PCB) Instructions

1. PCB Instruction Format



2. PCB Control Characters

Table I. PCB Control Characters

CHARACTER AND CODING	FUNCTION	COMMENT
C1 Innnnn C2 innnnn	Interlock bit = I RWC = nnnnn I/O bit = i Peripheral Address = nnnnn	I/O bit is immaterial. Logical address of Type 212-1 on peripheral bus.
a. Control characters C3 through Cn have the following functions:		
1. Test for Busy, Inactive System, and Device Interrupt.		
000XXX	System busy or Type 212-1 inactive? If yes, branch to A.	
001000	Busy? If yes, branch to A.	
111001	Interrupt? If yes, branch to A.	Ask if both Allow and Interrupt functions are set.
2. Set and reset Allow function and reset Interrupt function.		
111001	Set Allow function.	
111000	Reset Allow function.	
111100	Reset Interrupt function.	

(Continued)---

Table I. PCB Control Characters (Cont'd)

CHARACTER AND CODING	FUNCTION	COMMENT
3. Reserve the Type 212-1 for the initiating central processor. Control characters C3...Cn have the following functions:		
C3 = 010000 and C4 = 000000	Busy and reserve? If busy, branch to A.	If not busy, device is set busy to the other central processor. This reserves the device for the initiating central processor.
C3 = 110001 (Initiator)	Is the Type 212-1 set for transfer of data? If no, branch to A.	The "no" condition will exist from the time the initiator issues the control (reserving) PCB instruction until the responder issues its second PDT instruction.
110 100 (Responder)	Is the Type 212-1 set for transfer of data? If yes, branch to A.	The "yes" condition will exist from the time the initiator issues the control (reserving) PCB instruction until the responder issues its second PDT instruction.
C5 = 110001 (with C3 = 010000 and C4 = 000000	Was "reserve" action by this central processor successful? If no, branch to A.	This prevents possible race conditions and two central processors acting simultaneously.

C. Programming Comments

Depression of INITIALIZE at either processor clears both halves of the Type 212-1.

When the operation of one central processor is halted, the program functions of the other are affected only in that data transfer via the Type 212-1 is impossible. Any PCB instruction test is answered with a busy signal; no PDT instruction should be sent to the Type 212-1.

IV. OPERATION

A. General Discussion

This section describes Type 212-1 operation during a typical transfer of data between two central processors. Type 212-1 operations are implemented by PDT and PCB instructions issued from both receiving and sending central processors. Either half of the Type 212-1 accepts a PDT instruction under the conditions established in this section. The PCB instruction is used to instruct and test the Type 212-1.

B. Initiating Operation

The initiating central processor sends a PCB instruction to determine whether the Type 212-1 is busy. If the adapter is not busy, the central processor sends another PCB instruction to reserve the Type 212-1, thus "locking out" the other central processor as an initiator.

If the corresponding Allow function has been set, the Type 212-1 sets the Interrupt function on the responding central processor. When the responding central processor has the interrupt capability, it receives a program interrupt; otherwise, it must sense the situation by means of a PCB instruction.

Both the initiating and responding central processor now issue "Transfer" PDT instructions to the Type 212-1.

C. Operation During Control Transfer

The Type 212-1 issues a frame demand to the sending central processor and the control characters are transferred from the area specified by the PDT instruction of the sender to the area specified by the PDT instruction of the receiver. The transfer of control characters terminates when a record mark is encountered on either side.

The central processor adapter disconnects the responding central processor; the initiator remains connected. The responding central processor issues a second PDT instruction to the Type 212-1. The central processor adapter issues a frame demand to the central processor which is to be the sender. Either the initiator or the responding central processor may be the sender; this depends upon the input/output bit of the C2 character in the second PDT instruction issued by the responding central processor.

D. Operation During Data Transfer

Data is now transferred between the two central processors by way of the Type 212-1 Central Processor Adapter. The areas in memory which are affected - depending on direction of data flow - are established by two factors: The A address of the second PDT instruction issued by the responding central processor; The

setting of the current location counter originally specified by the initiator's PDT instruction.

Data is transferred until a record mark is encountered on either side. The record mark causes disconnection of both central processors from the Type 212-1, which becomes not busy and therefore available to either central processor.

V. HOUSING AND POWER SOURCE

Each half of the Type 212-1 Adapter is housed in its associated central processor. Each half also receives power from its associated central processor.

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HARDWARE BULLETIN

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