HONEYWELL EDP

HARDWARE BULLETIN

SERIES 200

TYPE 281-1M COMMUNICATION CONTROL AND TYPE 285-1M COMMUNICATION ADAPTER

SUBJECT: Equipment Specifications for the Type 281-1M Communication Control and the Type 285-1M Communication Adapter for Use with a Honeywell Remote Data Station and the Bell DATA-PHONE Dataset 202C or 202D on Switched Voice-Grade Telephone Lines or Leased Voice-Grade Telephone Lines.

SPECIAL INSTRUCTIONS: References include the bulletins entitled Type 286-1, -2 and -3 Multi-Channel Communication Controls, Order No. 160, and Type 281-1 Communication Controls, Order No. 086; also the Honeywell Series 200 Models 200/1200/2200 Programmers' Reference Manual, Order No. 139. A general reference is the Series 200 Data Station Remote Communication Terminal Reference Manual, Order No. 032.

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I. GENERAL DESCRIPTION

The Honeywell Type 281-1M Single-Channel Communication Control and Type 285-1M Communication Adapter provide the interconnection of a Series 200 central processor with a Honeywell Remote Data Station by means of Bell DATA-PHONE Dataset 202C on switched, voice-grade telephone lines or Bell DATA-PHONE Dataset 202D on leased, point-to-point voice-grade private lines. Also — if located within 50 feet of the remote station — the Type 281/285-1M provide a direct interconnection with the Honeywell Data Station.

As illustrated in Figure 1, the Type 281-1M connects one voice-grade telephone line to the Series 200 central processor. The Type 285-1M Communication Adapter is used in conjunction with a Type 286 Multi-Channel Communication Control to connect one voice-grade telephone line when a maximum of 63 communication lines are to be connected to a Series 200 central processor.

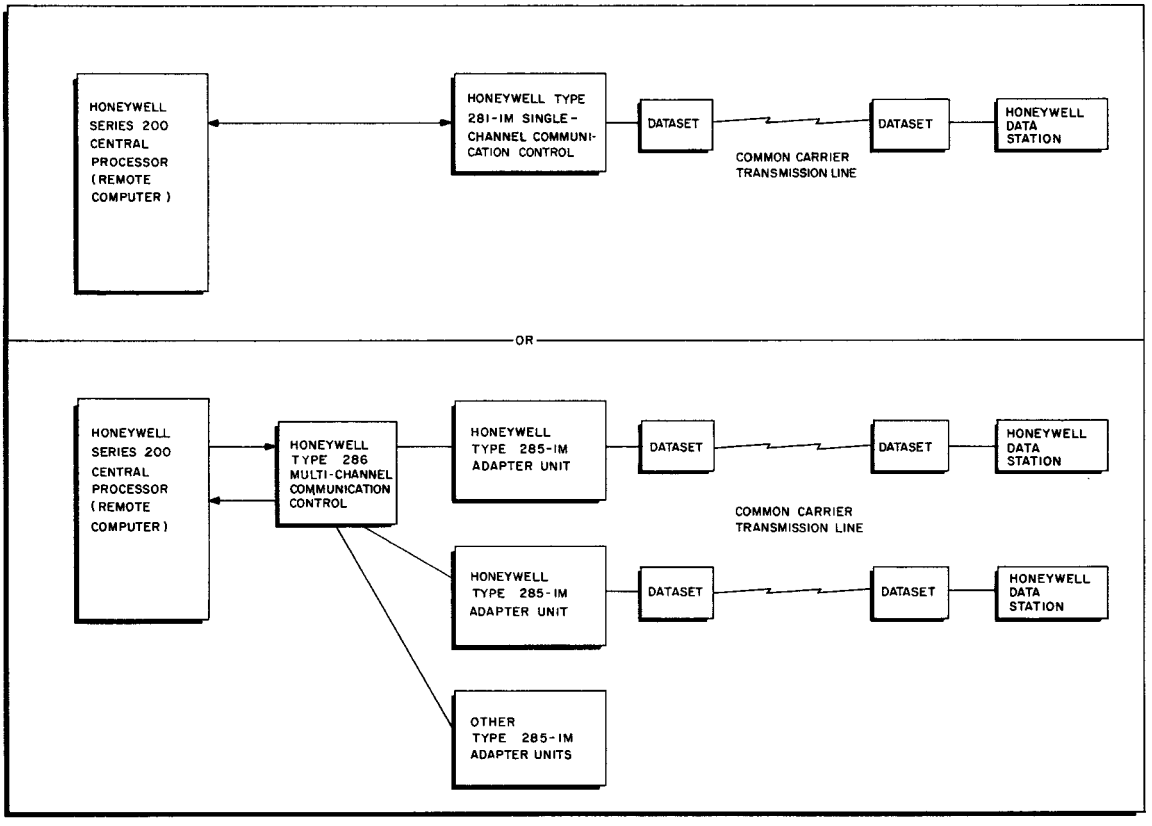

Figure 1. Data Flow Between the Central Processor and the Honeywell Data Station

The communication line is characterized by start-stop, asynchronous serial-by-bit transmission of eight-level (seven data bits plus an even-parity check bit) American Standard Code for Information Interchange (ASCII) in half-duplex mode. Table 1, page 3, illustrates the ASCII code.

The Types 281-1M and 285-1M transmit at the rate of 120 characters per second.

Equipment at the remote terminals (see the Series 200 Data Station Reference Manual) consists of the Honeywell Data Station, which may be equipped with the Bell DATA-PHONE Dataset 202C or 202D.

Even character parity generation and checking in the Type 281-1M Communication Control is described in Section VIII. Character parity generation and checking for the Type 285-1M Communication Adapter Unit is described in the bulletin Type 286-1, -2 and -3 Multi-Channel Communication Controls.

The standard Series 200 logic drawers contain one Type 281-1M Communication Control or eight Type 285-1M Communication Adapter Units.

II. INTERFACE WITH THE SERIES 200 CENTRAL PROCESSOR OR THE TYPE 286 MULTI-CHANNEL COMMUNICATION CONTROL

A. The Type 281-1M Interface with the Series 200 Central Processor

Standard peripheral interface logic for non-simultaneous input and output connects the Type 281-1M to the standard Series 200 peripheral bus.

B. The Type 285-1M Interface with the Type 286 Multi-Channel Communication Control

The Type 285-1M Communication Adapter Unit interface with the Type 286 is described in Section IV of the bulletin Type 286-1, -2 and -3 Multi-Channel Communication Controls.

III. INTERFACE WITH THE COMMON CARRIER

The common-carrier line termination is a Bell DATA-PHONE Dataset 202C or 202D.

IV. CODE CHARACTERISTICS

The signals sent out by the Types 281-1M and 285-1M are illustrated in Figure 2, page 4. The datasets convert voltage-level signals into audio-frequency signals for transmission over the line.

Table 1. American Standard Code for Information Interchange

Bits b_4 b_3 b_2 b_1	Row	b_7 b_6 b_5 = 0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
	Col. →	0	1	2	3	4	5	6	7
0 0 0 0	0	NUL	DLE	SP	0	\	P	@	p
0 0 0 1	1	SOH	DC1	!	1	A	Q	a	q
0 0 1 0	2	STX	DC2	"	2	B	R	b	r
0 0 1 1	3	ETX	DC3	#	3	C	S	c	s
0 1 0 0	4	EOT	DC4	$	4	D	T	d	t
0 1 0 1	5	ENQ	NAK	%	5	E	U	e	u
0 1 1 0	6	ACK	SYN	&	6	F	V	f	v
0 1 1 1	7	BEL	ETB	′	7	G	W	g	w
1 0 0 0	8	BS	CAN	(	8	H	X	h	x
1 0 0 1	9	HT	EM	)	9	I	Y	i	y
1 0 1 0	10	LF	SS	*	:	J	Z	j	z
1 0 1 1	11	VT	ESC	+	;	K	[	k	{
1 1 0 0	12	FF	FS	,	<	L	~	l	←
1 1 0 1	13	CR	GS	-	=	M	]	m	}
1 1 1 0	14	SO	RS	.	>	N	^	n	|
1 1 1 1	15	SI	US	/	?	O	—	o	DEL

CONTROL CHARACTERS

NULL Null/Idle
SOH Start of Heading (CC)
STX Start of Text (CC)
ETX End of Text (CC)
EOT End of Transmission (CC)
ENQ Enquiry (CC)
ACK Acknowledge (CC)
BELL Audible or attention signal
BS Backspace (FE)
HT Horizontal Tabulation (punch card skip) (FE)
LF Line Feed
VT Vertical Tabulation (FE)
FF Form Feed (FE)
CR Carriage Return (FE)
SO Shift Out
SI Shift In

DLE Data Link Escape (CC)
DC1, DC2, DC3 } Device Controls
DC4 Device Control (stop)
NACK Negative Acknowledge (CC)
SYNC Synchronous Idle (CC)
ETB End of Transmission Block (CC)
CNCL Cancel

EM End of Medium
ESC Escape
FS File Separator (IS)
GS Group Separator (IS)
RS Record Separator (IS)
US Unit Separator (IS)
DEL Delete

NOTE

(CC) Communication control
(FE) Format effector
(IS) Information separator

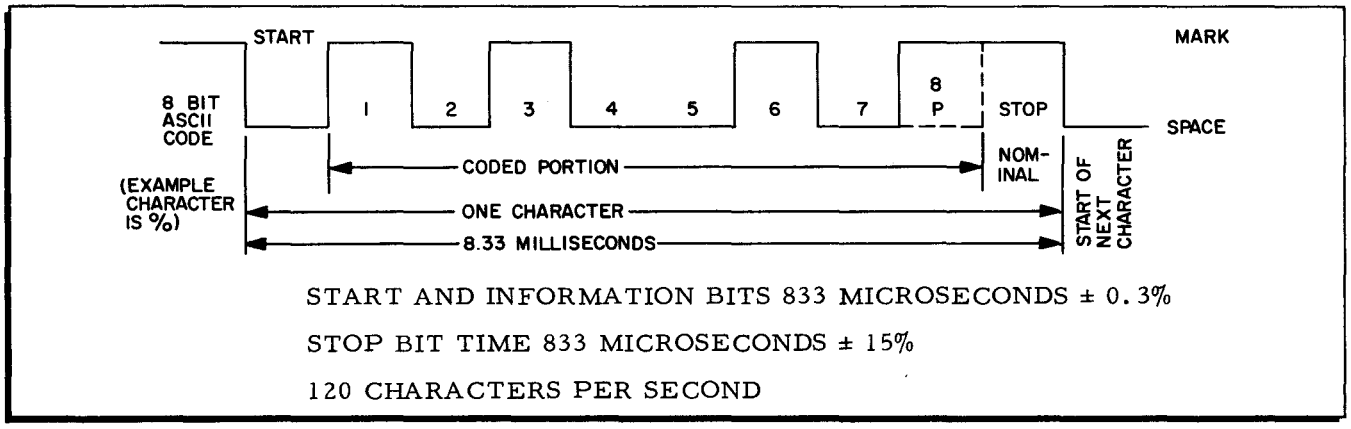

Figure 2. Signal at Communication Control/Dataset Interface

V. FUNCTIONAL DESCRIPTION OF THE TYPES 281-1M AND 285-1M

The Type 281-1M uses standard peripheral interface logic for non-simultaneous input or output. The Type 281-1M includes an eight-bit (seven data bits, plus one bit for parity) shift register which serves as a buffer and serializes data while receiving and transmitting; a strobe generator delivering a pulse for sampling and shifting individual bits; logic switches which indicate to the central processor whether the communication control is in the input or output mode, whether it is active, or whether busy and error conditions prevail.

A. Type 281-1M Reception

A "space" signal (0) on the communication line enduring more than one-half of a bit time switches the Type 281-1M to the receive mode.

A bit from the line moves into the buffer shift register, causing the bits already stored to be shifted one position. When all bits of one character are stored in the shift register, an Input Frame Demand is set.

The system handles messages by two modes of transmission: "block" and "single-character." In both modes, data is processed as n characters, where $n \geq 1$.

In the block method of transmission, the Type 281-1M Communication Control has continuous access to the central processor by way of its read/write channel (RWC), and an Input Frame Demand is honored during the next memory cycle.

During the single-character method of transmission, two means exist for notifying the central processor of activity requests:

1. The Input Frame Demand is tested by a Peripheral Control and Branch (PCB) instruction frequently enough to ensure the removal of the stored character from the shift register within the stop-bit time.
2. A program interrupt saves repetitive testing for frame demands, although the Input Frame Demand should be checked before issuance of the subsequent "Input" PDT instruction. (This method requires the program interrupt feature, which is standard equipment for all Series 200 central processors except the Type 201; Type 201 must be equipped with Feature 012, as described in the Models 200/1200/2200 Programmers' Reference Manual, pages 1-15 and 1-16.)

B. Type 281-1M Transmission

Type 281-1M reception of an "Output" PDT instruction sets the Transmit function. Data arriving thereafter from the central processor over the output bus (six bits in parallel) is stored in the buffer shift register. Two six-bit transfers are required to transfer an eight-bit character.

Before the data is sent to the line, a start bit is generated. The character is then shipped through the shift register and onto the line. During part of the last-bit and stop-bit time an Output Frame Demand becomes active, as described in Section V, B.

Activity requests to the central processor are handled as described in Section V, B.

C. Type 285-1M Functional Description

The functional description of the Type 285-1M is similar to that given in the preceding Section V, A, for the Type 281-1M, with these exceptions: the Type 285-1M mode of data transfer is always single-character and its activity requests are sent to the Type 286 Multi-Channel Communication Control. When a complete character is accumulated, an interrupt is sent to the central processor.

VI. PROGRAMMING REFERENCE DATA

NOTE

The following description is based on the presence of the program interrupt feature, which is standard equipment for all Series 200 central processors, except the Type 201. However, the basic Type 281-1M does not require this feature, since the system can be programmed using PCB instructions to test for "busy," thereby initiating a program branch whenever a request is made for service. Also, the following description applies mainly to the Type 281-1M; for Type 285-1M programming, see the bulletin Types 286-1, -2 and -3 Multi-Channel Communication Controls.

A. General Description

Though the Type 285-1M — operating in conjunction with the Type 286 Multi-Channel Communication Control — uses only the single-character method of transmission, the Type 281-1M Communication Control handles data on a single-character or a block (message) basis.

Block transmission with the Type 281-1M permits handling of more data with less manipulation and fewer program interruptions than does single-character transmission. Therefore, block transmission is essential for use with very high-speed lines; also, it is often convenient for use with lower-speed lines, especially when communication is sharing computer time with other processing.

Whether operating on a single-character or block basis, the Type 281-1M Communication Control requires that a record mark be set in the data storage area of main memory to terminate data transfer and to release the read/write channel.

B. Initial Start

The Type 281-1M starts when INITIALIZE is pressed on the central processor control panel.

C. Type 281-1M Stand-By Condition

Unless transmitting or receiving, the Type 281-1M is in a neutral state, permitting transmission by the program onto the line, but also interrupting the program when a character is received from the line.

If no characters are received from the line during a half-character period, the Type 281-1M interrupts the program with an output request. Thus, if characters are being received at less than two-thirds the line rate, there may be two interrupts per character.

D. Type 281-1M Reception

Reception of the start bit of the first character switches the Type 281-1M to the "busy" state. The first full character received causes a program interrupt if the Type 281-1M has been conditioned — by execution of a "Set Allow" PCB instruction — to allow interrupts. The Allow Interrupt function remains set until specifically reset by the program or by depression of INITIALIZE. In response to this interrupt, the program issues a Peripheral Data Transfer (PDT) instruction bringing that character and succeeding characters into main memory.

Reception continues until a record mark is encountered in main memory; then the read/write channel is released. If no further characters are received during a half-character period, the Type 281-1M reverts to Not Busy and sends an interrupt requesting output when Allow is set. This interrupt (identified by a positive response to the PCB "Output Request" query) may be utilized by the programmer to indicate the end of a received message.

When a received message occupies less than the assigned memory area, the record mark terminating data transfer is not encountered. A timer in the Type 281-1M is therefore activated and — after a specified interval — it releases the assigned read/write channel, sets the Device Error condition, and allows the Type 281-1M to revert to "not busy." If Allow is set, an interrupt requesting output then occurs. When the Type 281-1M utilizes a Bell DATA-PHONE Data-set 202C operating on switched service, a Disconnect is also generated by the "Time-out."

E. Type 281-1M Transmission

Starting in the "initialized" condition (interrupts not allowed), the Type 281-1M may then accept an "Allow Interrupt" PCB instruction. This is followed by a PDT instruction beginning transmission of data from the central processor. Such data is transferred from the assigned memory location until a record mark is encountered; then the read/write channel is released. When the read/write channel is released and the last character goes onto the line, an interrupt occurs. A second PDT instruction continues data transmission or — if such transmission is complete — a "Reset Interrupt" PCB instruction acknowledges the interrupt and signifies the completion of transmission. An interrupt can still occur if data is received, or a "Reset Allow" PCB instruction can be given to the Type 281-1M to prevent further interrupts.

When interrupts are not allowed, testing of Input and Output Frame Demands is required.

F. Peripheral Control and Branch (PCB) Instructions

1. Type 281-1M

Format for the Type 281-1H Peripheral Control and Branch instructions is found in Section II of the bulletin Type 281-1 Single-Channel Communication Controls.

2. Type 285-1M

Format for the Types 286/285-1M Peripheral Control and Branch instructions is found in Section VI of the bulletin Type 286-1, -2 and -3 Multi-Channel Communication Controls.

G. Peripheral Data Transfer (PDT) Instructions

1. Type 281-1M

Format for the Type 281-1M Peripheral Data Transfer instruction is given in Section II of the bulletin Type 281-1 Single-Channel Communication Controls.

2. Type 285-1M

This PDT instruction format is given in Section VI of the bulletin Type 286-1, -2 and -3 Multi-Channel Communication Controls.

H. Record Marks and Characters in Main Memory

1. Record Marks Required in Memory

When the Type 281-1M is transmitting data by the single-character method, a record mark is placed in memory location A+2 to terminate a character. When receiving data in the single-character mode, a record mark in location A+1 indicates character termination.

When transmitting data in the block mode, a record mark is placed in memory location A+2 n (where n is the number of characters) to terminate a character group. During reception of data transmitted by the block method, the Type 281-1M requires that the record mark be placed in location A+(2n-1) to terminate the message and to release the read/write channel.

In Type 285-1M programming, no record marks are required.

2. Type 281-1M Character Configuration in Main Memory

Character Configuration in main memory is shown below:

Bit Position	8	7	6	5	4	3	2	1	MEMORY LOCATION
Series 200 CP RECEIVING	Ø	Ø	Ø	Ø	Ø	Ø	*Ø	B7	A
	IM	WM	B6	B5	B4	B3	B2	B1	A + 1
Series 200 CP SENDING			Ø	Ø	Ø	Ø	Ø	B7	A
			B6	B5	B4	B3	B2	B1	A + 1
	IM	WM							A + 2

IM = Item Mark
WM = Word Mark
IM + WM = Record Mark
Bn = Code Bit

*If hardware parity checking is used, then the eighth bit is not sent from the control unit to the central processor memory. If the hardware parity checking is not used, then the eighth bit appears in this position.

I. Series 200 and Type 281-1M Interface Signals

1. Single-Character Transmission

During single-character transmission between the Type 281-1M and the Series 200 central processor, the following interface signals occur.

a. Device Busy

This busy signal indicates that a PDT instruction cannot be accepted by the control unit. Busy is active whenever the read/write channel associated with a PDT instruction addressed to the control unit is busy or when the control unit is receiving or transmitting data on the line.

b. Interrupt

Activation of Interrupt indicates that the control unit is requesting service. Interrupt responds to the first "Set Allow" PCB instruction when the control unit is "initialized"; thereafter, it responds only when an Input or Output Frame Demand becomes active. The communication control Interrupt signal is reset when a PDT instruction is sent to the unit, when a "Turn Off Interrupt" PCB instruction is sent to the unit, or when the system is "initialized."

c. Input Frame Demand (IFD)

The IFD signal indicates that the communication control — having assembled a character from the line and readied it for the computer — is requesting a "Receive" PDT instruction. The next PDT instruction to the communication control resets the IFD signal; if no further PDT instruction is executed, the IFD signal is not reset.

d. Output Frame Demand (OFD)

The OFD signal indicates that the communication control is capable of accepting a "Transmit" PDT instruction. This signal may be actuated when the communication control is neither transmitting nor receiving, and when the IFD signal is inactive.

The Output Frame Demand, then, becomes active in the transmit mode when the communication control is ready to transmit the next character. In the receive mode, after a one-half character duration of inactivity on the line, and after a PDT instruction has reset the IFD signal, the Output Frame Demand becomes active.

The OFD signal is reset by a "Transmit" or "Receive" PDT instruction, or when the communication control senses a character on the line.

e. Timing Error

The timing error signal indicates the loss of a control-unit data character. In the receive mode, the signal is set when a "Receive" PDT instruction does not respond to an Input Frame Demand before the next character is sensed on the line.

Timing Error is reset when the next PDT instruction is issued to the communication control.

f. Parity Error

The Parity Error signal is associated only with the receive mode. The signal is set — if the communication control is capable of checking parity — by a character demonstrating bad parity when the Input Frame Demand becomes active. Parity Error is reset by the next PDT instruction issued to the communication control.

g. Turn Off Interrupt

The "Turn Off Interrupt" PCB instruction permits the effectiveness of a Resume Normal Mode (RNM) instruction without executing a PDT instruction to the communication control.

h. Reset Allow

The "Reset Allow" PCB instruction prevents future interrupts from the communication control. A current interrupt is not reset by this PCB instruction; either a "Turn Off Interrupt" PCB instruction or a PDT instruction is needed to render an RNM instruction effective.

2. Single-Character Timing Considerations

a. Set Allow

The timing of the interrupt responding to the "Set Allow" PCB instruction is unpredictable.

b. Received Data

Data offered in response to a "Receive" PDT instruction is entered into main memory within eleven memory cycles after the extraction of the PDT instruction.

c. Transmitted Data

Data in main memory which is to be transferred by a "Transmit" PDT instruction can not be changed until fourteen main memory cycles are completed after the extraction of that instruction.

NOTE

The read/write channel is busy until all the data is transferred. The control unit is busy two main memory cycles longer than the read/write channel.

3. Block-Method Transmission

During the block method of transmission between the Type 281-1M and the Series 200 central processor, the following interface signals occur.

a. Input Frame Demand

The IFD signal is activated when the communication control has assembled the first block (message) character from the line for transfer to the computer. This signal is reset by a PDT instruction and not activated again by a character on the line until the assigned RWC is released. Such a release is accomplished either by the sensing of a record mark in memory or by a line inactivity period of approximately 30 seconds.

b. Output Frame Demand

The OFD signal is activated in the transmit mode when the communication control is ready to transmit a block. In the receive mode, the OFD signal becomes active after a line inactivity period of one-half of a character time, providing the RWC has been released. If the RWC has not been released, an inactivity period of 30 seconds elapses before the release is effective and the OFD signal is activated.

c. Timing Error

In the receive mode, Timing Error is set when the control unit releases the RWC after the 30-second period of inactivity described in paragraph b, above.

VII. FORMAT OF DATA AND CONTROL TRANSMISSION

Transmission control procedures and data and control message format for operation of the Type 281-1M Communication Control or Type 285-1M Communication Adapter are highly dependent upon the configuration of the Data Station with which the control or adapter communicates. It is therefore imperative that this publication be used in conjunction with the Series 200 Data Station Reference Manual. The reference manual Table 2-1, "Data Station Message Formats," and Tables 3-1 and 3-2 on input/output device activations are particularly applicable.

VIII. TYPE 281-1M PARITY GENERATION AND CHECKING

A. General

As mentioned in Section I, parity generation and checking for the Type 285-1M Communication Adapter Unit is described in the bulletin Type 286-1, -2 and -3 Multi-Channel Communication Controls. Even-parity generation and checking for the Type 281-1M Communication Control is described in the following paragraphs.

B. Transmitting

Characters to be sent from Series 200 main memory need have only the low-order seven bits (B7 in location A; B6 through B1 in location A + 1) specified in accordance with the ASCII Code. Bit 8 is immaterial, as the Type 281-1M automatically generates even parity for each character transmitted.

C. Receiving

During reception, the Type 281-1M strips bit 8 from all incoming characters when checking parity; thus only the low-order seven bits are received in the main memory. Bit 8 is zero, as are the high-order bits of location A. The test for parity errors which may have occurred during reception is accomplished by issuing a PCB instruction with a C3 control character of octal 40. This test must be made before any subsequent PDT instruction is issued. A branch to the location specified by the PCB instruction A address occurs if bad parity is detected in the execution of the preceding PDT instruction.

IX. MAINTENANCE FACILITIES

The Types 281-1M and 285-1M have no maintenance panel, indicator lights, or switches.

NOTES

NOTES

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TITLE: SERIES 200 TYPE 281-1M COMMUNICATION CONTROL AND TYPE 285-1M COMMUNICATION ADAPTER HARDWARE BULLETIN

DATED: APRIL, 1966

FILE NO: 112.0005.1100.0-108

ERRORS NOTED:

Fold

SUGGESTIONS FOR IMPROVEMENT:

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