HARDWARE BULLETIN

SERIES 200

TYPES 281-1E, 285-1E COMMUNICATION UNITS

SUBJECT: Equipment Specifications for the Type 281-1E Communication Control and the Type 285-1E Communication Adapter Unit (for use with the IBM 1050 Remote Terminals and the Model 103A DATA-PHONE Data Sets).

SPECIAL INSTRUCTIONS: This bulletin supersedes the Customer Information Bulletion 200-34 dated November 2, 1964. It will, in turn, be superseded by more detailed programming and operating procedures in forthcoming publications. The reference used in this text is the bulletin entitled Equipment Specification for the Type 286-1, -2 and -3 Multi-Channel Communication Controls, File No. 112.0005.1100.00.03.

DATE: October 27, 1965

FILE NO. 112.0005.1100.0-061

31065
Printed in U.S.A.

Questions and comments regarding this manual should be addressed to:

Honeywell Electronic Data Processing
Information Services
60 Walnut Street
Wellesley Hills, Massachusetts 02181

EQUIPMENT SPECIFICATIONS FOR THE TYPE 281-1E COMMUNICATION CONTROL AND THE TYPE 285-1E COMMUNICATION ADAPTER UNIT

I. GENERAL DESCRIPTION

The Honeywell Type 281-1E Communication Control and Type 285-1E Communication Adapter Unit provide the interconnection of a Series 200 central processor with IBM 1050 Remote Terminals by means of Bell 103A DATA-PHONE datasets on switched, voice-grade telephone lines or on TWX CE (TWX Customer Equipment) switched narrow-band lines. (Appendix I of this bulletin designates possible Honeywell/IBM 1050 operation via other common carrier facilities.)

As illustrated in Figure 1, page 2, the Type 281-1E Communication Control is used to connect one voice-grade telephone line or TWX CE line to the Series 200 central processor, while the Type 285-1E Communication Adapter Unit is used in conjunction with a Type 286 Multi-Channel Communication Control to connect one voice-grade telephone line or one TWX Prime line when a maximum of 63 communication lines are to be connected to a central processor.

The communication line is characterized by start-stop, synchronous, serial transmission of seven-level (six-bit plus an odd-parity check bit) code in two-way, non-simultaneous, half-duplex mode.

One character comprises seven code bits plus stop and start bits. The duration of the complete character is 68.18 milliseconds, and the maximum line speed is 14.8 characters per second, or 134.98 baud (the baud rate being the reciprocal of the information bit duration expressed in seconds).

Equipment at the remote stations consists of an IBM 1051 Data Communication Control Unit in combination with one or more of the following IBM devices:

1052 Printer Keyboard (Selectric Model)
1053 Printer
1054 Paper Tape Reader which will reverse and read for error correction
1055 Paper Tape Punch
1056 Card Reader which will reread a card for error correction
1057 Card Punch
1058 Printing Card Punch

The standard Series 200 logic drawer contains one Type 281-1E Communication Control or eight Type 285-1E Communication Adapter Units.

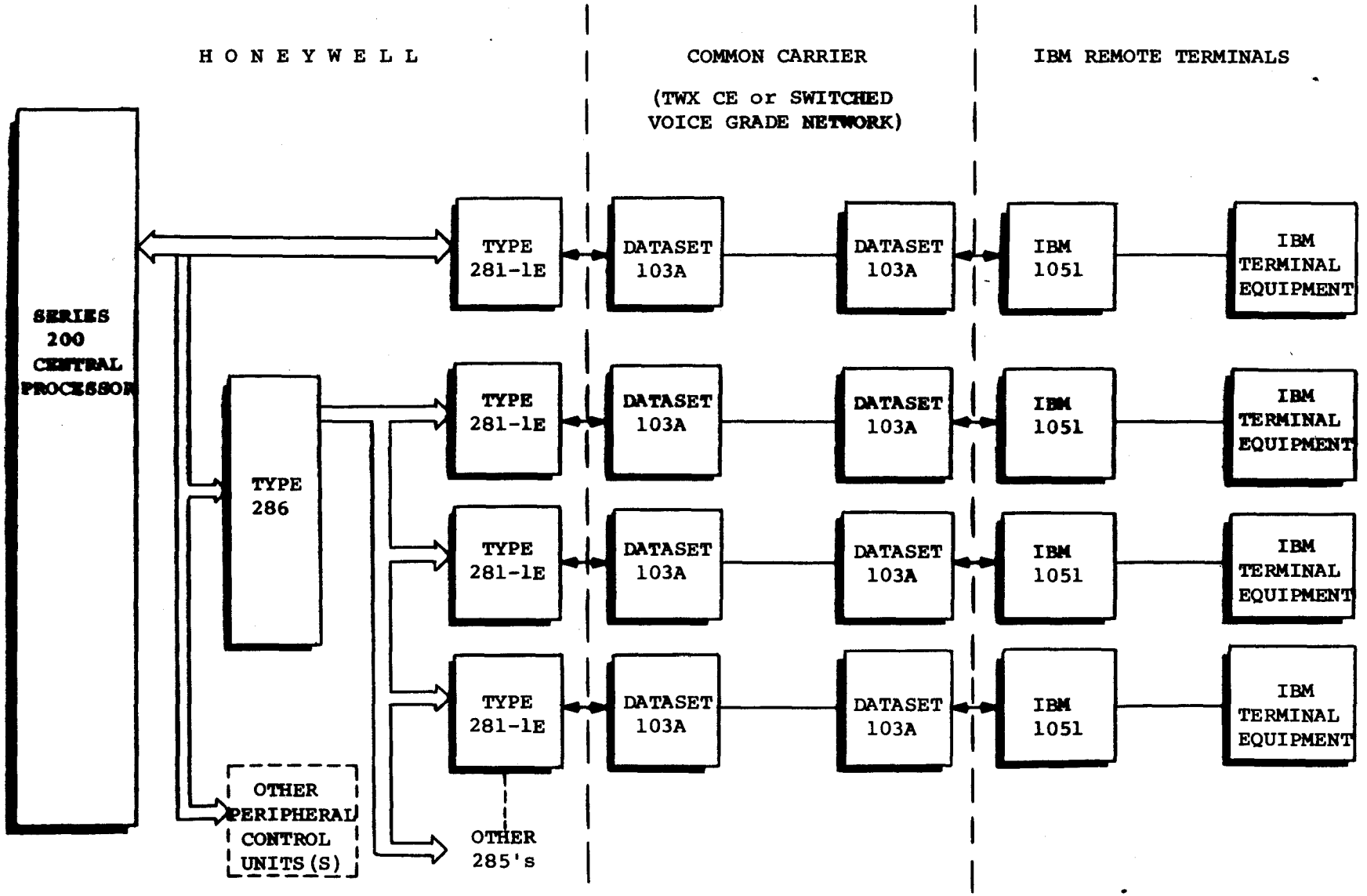


Figure 1. Applications of Types 281-1E and 285-1E

II. INTERFACE WITH THE SERIES 200 CENTRAL PROCESSOR OR THE TYPE 286 MULTI-CHANNEL COMMUNICATION CONTROL

A. The Type 281-1E/Central Processor Interface

Standard peripheral interface logic for non-simultaneous input and output connects the Type 281-1E to the Series 200 standard peripheral bus.

B. The Types 285-1E/286 Interface

This interface is demonstrated below:

2 DATA LINES

286 ——▶ 285	Information out (serial by bit)
286 ◀—— 285	Information in (serial by bit)

6 ADDRESS LINES

286 ——▶ 285	Select a particular Type 285

2 REQUEST LINES

286 ◀—— 285	Type 285 requests a bit from Type 286
286 ◀—— 285	Type 285 requests Type 286 to take a bit

2 TIMING LINES

286 ——▶ 285	Bit ready on Data-Out line
286 ——▶ 285	Bit received on Data-In line

1 RESET LINE

CP ——▶ 286 ——▶ 285	Reset by depressing INITIALIZE on central processor control panel

1 SPECIAL STROBE LINE

286 ——▶ 285	Control information to the Type 285

All signals are at the voltage level of ground or +5 vdc, nominal.

III. INTERFACE WITH THE COMMON CARRIER

A. General

The common carrier line termination is a Bell 103A DATA-PHONE dataset.

B. Interface Signals

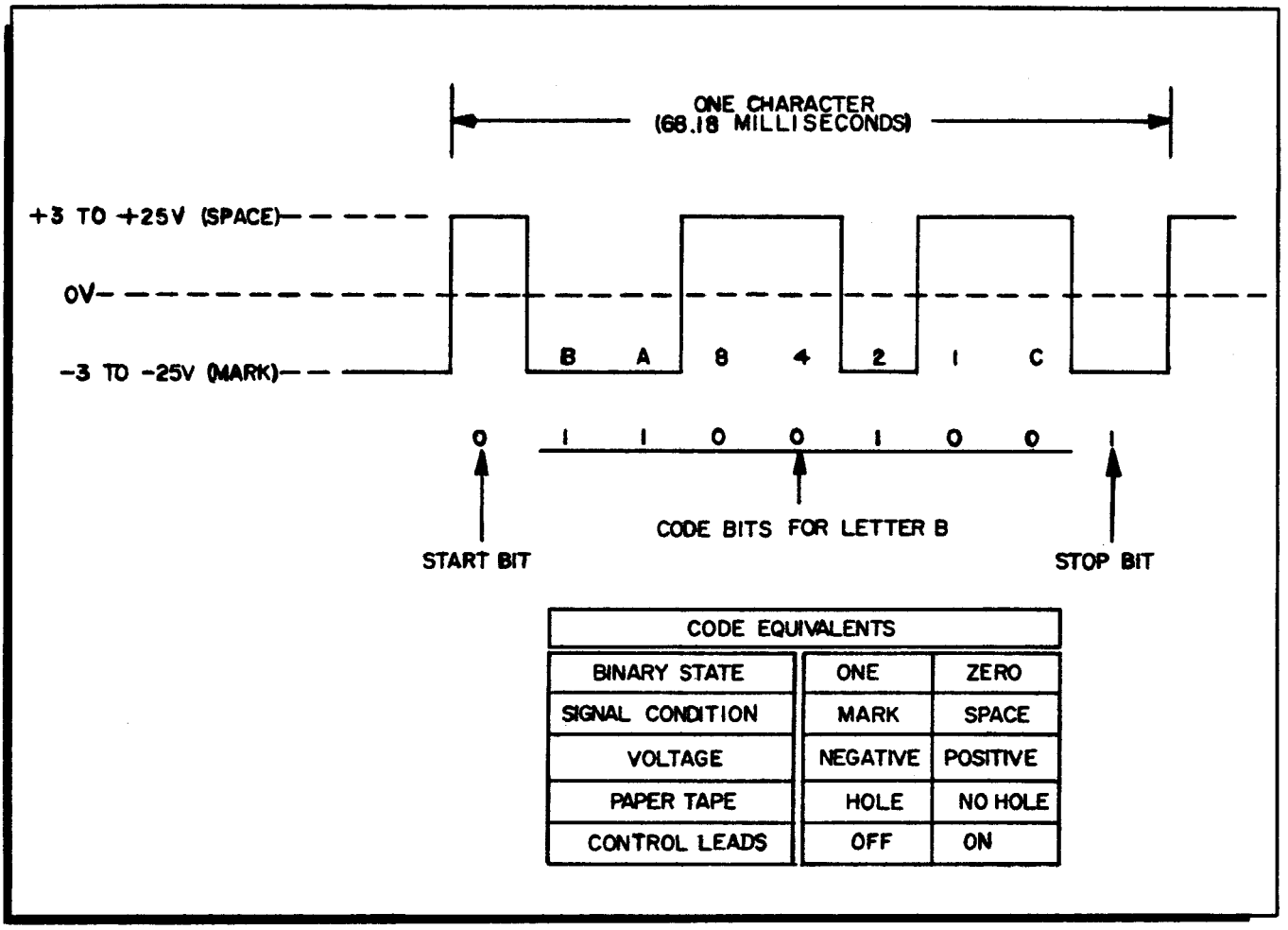
The voltage-level signals of these communication controls are converted by the dataset into audio-frequency signals for transmission on the line.

The interface signals between the dataset and the communication controls are listed in Table I, below.

Table I. Interface with BELL 103A DATA-PHONE Dataset

PIN NUMBER	BELL DESIGNATOR	DESCRIPTION	SIGNAL SOURCE
1	AA	Frame Ground	---
2	BA	Transmitted Data	281-1E or 285-1E
3	BB	Received Data	Dataset
5	CB	Clear To Send	Dataset
6	CC	Data Set Ready	Dataset
7	AB	Signal Ground	---
8	CF	Carrier Detector	Dataset
20	CD	Data Terminal Ready	281-1E or 285-1E
4		Reserved for Tel. Co. use	
10		Reserved for Tel. Co. use	
22		Reserved for Tel. Co. use	

Data signals correspond to the format shown in Figure 2, below.



CODE EQUIVALENTS		
BINARY STATE	ONE	ZERO
SIGNAL CONDITION	MARK	SPACE
VOLTAGE	NEGATIVE	POSITIVE
PAPER TAPE	HOLE	NO HOLE
CONTROL LEADS	OFF	ON

Figure 2. Data Signal at Control Unit/Dataset Interface

More detailed information on the 103A DATA-PHONE dataset interface may be found in the AT&T Data and Teletype Planning Engineer "Blue Book".

IV. REMOTE STATION EQUIPMENT AND CODE CHARACTERISTICS

A. Remote Station Equipment

An IBM remote terminal system consists of an IBM 1051 Control Unit and one or more of the other IBM devices listed below.

1. The 1051 Control Unit

This unit is the center for all data flow. It contains data channels, control circuit code translator and power supply for the entire system. The unit transmits at the maximum rate of 14.8 characters per second (Section I, fourth paragraph).

2. The 1052 Printer Keyboard

The 1052 Printer Keyboard is a modified IBM 26 Keyboard housed in the same cover as the printing mechanism of the IBM Selectric ("golf ball") Typewriter. It is connected by means of data channels in the control unit.

3. The 1053 Printer

This is the printing mechanism from the IBM Selectric Typewriter.

4. The 1054 Paper Tape Reader

The unit reads system code from either one-inch, eight-track paper tape or eight-track edge-punched documents. It can backspace over a record, then reread it.

5. The 1055 Paper Tape Punch

This unit punches into one-inch, eight-track paper tapes or edge-punched documents.

6. The 1056 Card Reader

The IBM 1056 Reader reads cards serially, translating the card code into system code. Cards are fed into the unit singly or - by means of a special feature - in packs of 300 cards each (maximum).

7. The 1057/1058 Card Punch

This unit is an IBM 534 Card Punch or an IBM 536 Printing Card Punch with a translator which converts system code to card code.

NOTE:

An annotated bibliography of "References for IBM 1050 System Available at Honeywell EDP Engineering" forms Appendix II of this bulletin.

B. Code and Message Characteristics

Messages are transmitted in variable-length blocks in the IBM six-bit BCD code plus a seventh - C - bit which provides a parity check on each character. Figure 3, below, illustrates a sample message. Table II, page 8, gives the appropriate IBM code.

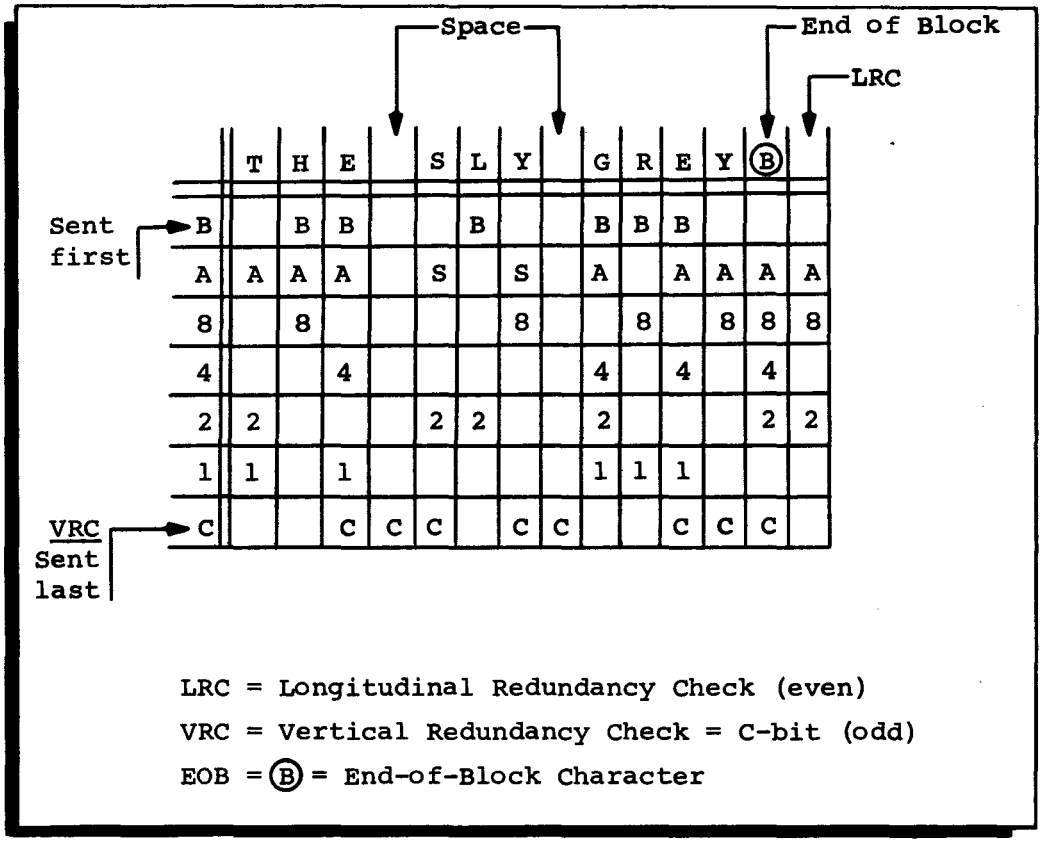


Figure 3. IBM 1050 Block Transmission

Each message block is terminated by an end-of-block (EOB) character followed by a longitudinal redundancy check (LRC) character. This LRC character is formed by seven half-adders which count all transmitted or received code bits, including vertical redundancy check (VRC) C-bits and the bits of the EOB character. Because the C-bit is counted, the LRC character may have either odd or even parity. Over-all longitudinal parity of a block including the LRC character is even.

Table II. IBM 1050 System Code

CHARACTERS	ODD PARITY BCD CODE						
NORMAL SHIFT	8	4	2	1	B	A	C
1				1			
2			2				
3			2	1			C
4		4					
5		4		1			C
6		4	2				C
7		4	2	1			
8	8						
9	8			1			C
0	8		2				C
A				1	B	A	
B			2		B	A	
C			2	1	B	A	C
D		4			B	A	
E		4		1	B	A	C
F		4	2		B	A	C
G		4	2	1	B	A	
H	8				B	A	
I	8			1	B	A	C
J				1	B		C
K			2		B		C
L			2	1	B		
M		4			B		C
N		4		1	B		
O		4	2		B		
P		4	2	1	B		C
Q	8				B		C
R	8			1	B		
S			2			A	C
T			2	1		A	
U		4				A	C
V		4		1		A	
W		4	2			A	
X		4	2	1		A	C
Y	8					A	C
Z	8			1		A	
.	8		2	1	B	A	
$	8		2	1	B		C
,	8		2	1		A	C
@						A	
/				1		A	C
#	8		2	1			
&					B	A	C
-					B		

FUNCTIONS	ODD PARITY BCD CODE						
	8	4	2	1	B	A	C
BKSP	8	4	2		B		C
EOT	8	4	2	1			C
DELETE	8	4	2	1	B	A	C
DOWN-SHIFT	8	4	2		B	A	
CR AND LF	8	4		1	B		C
PREFIX	8	4	2	1		A	
IDLE	8	4	2	1	B		
RDR STOP	8	4		1			
SPACE							C
EOB	8	4	2			A	C
UP-SHIFT	8	4	2				
LF	8	4		1		A	C
TAB	8	4		1	B	A	
RESTORE	8	4			B		
BYPASS	8	4				A	
EOA	8		2	1			

V. OPERATIONAL CONTROLS

The Bell 103A DATA-PHONE dataset provides the operational controls for these communication systems.

A. Voice-Grade Line System

Calls are initiated by dialing the remote station with the dataset. Voice communication is thus established and the DATA push-button switches at each station are depressed so that data transfer is initiated.

B. TWX Prime System

Here calls are placed and data transfer is initiated by means of the dataset as in the voice-grade line system, but without establishment of voice communication.

VI. PROGRAMMING INFORMATION

A. General

The Type 281-1E handles data on either a single-character or message-block basis, whereas the Type 285-1E transmits via a Type 286 Multi-Channel Communication Control only in the single-character method. These factors - together with others mentioned in the following paragraphs of this section - cause some basic programming differences between the two systems.

B. Type 281-1E Programming

Its block transmission capabilities allow the Type 281-1E to handle more data with less manipulation and fewer program interruptions than single-character operation. Thus, block transmission is essential with very high-speed lines. Also, it is convenient with low-speed lines when communications share computer time with other processing.

Whichever the method of Type 281-1E transmission - single-character or message-block - only a record mark in the main memory data storage area terminates data transfer and releases the read/write channel involved.

NOTE

In the following discussion of the Type 281-1E, we assume the system includes the Program Interrupt capability (standard on all Series 200 central processors except Type 201). However, actual operation of this communications control

NOTE (Cont)

unit does not require such system capability; the Type 281-1E may be tested frequently by the program to ensure that a character is moved to or from its shift register during stop-bit time.

1. Initial Start

The Type 281-1E is activated by depressing INITIALIZE on the central processor control panel during application of power to the system.

2. Receive

Reception of the first character's start bit from the line switches this communication control to "busy". The first full character received by the 281-1E causes a program interrupt if the interrupt has been allowed by execution of the "Set Allow" Peripheral Control and Branch (PCB) instruction. The Allow switch remains set until specifically reset by the program or by activation of the INITIALIZE button.

In response to this interrupt, the program must issue a Peripheral Data Transfer (PDT) instruction to bring that character and succeeding ones into the assigned main memory area. Reception continues until a record mark is encountered in memory, then the read/write channel is released. If no more characters are received during the half-character period after the record mark is encountered, the 281-1E reverts to "not busy", and an interrupt requesting output occurs when Allow is set. This latter interrupt may be used to indicate the end of a received message. Thus, if characters are being received at the less than two-thirds of a line rate, two interrupts per character may occur.

When a received message occupies less than the assigned memory area, the record mark terminating data transfer is not encountered. In this case, a timer in the Type 281-1E is activated and - after 30 seconds - the assigned read/write channel is released, the Device Error switch is set, the control reverts to Not Busy. An interrupt requesting output now occurs if Allow is set.

3. Transmit

Starting from the "initialized" condition, where no interrupts are allowed, an "Allow Interrupt" PCB instruction is given, followed by a PDT instruction to begin transmission of data from the central processor. Data is transferred from the assigned memory location until a record mark is encountered; then the read/write channel is released. Here, an interrupt

occurs after the last character goes onto the line. A second PDT instruction is now given to continue data transmission or - if transmission is complete - a "Reset Interrupt" PCB instruction is sent to acknowledge receipt of the last interrupt and to indicate that no more data will be sent. An interrupt next occurs if data is received, or a "Reset Allow" PCB instruction can be given to prevent any interrupt from the Type 281-1E.

C. Line-Disconnect Capability

The three line-disconnect capabilities - any one of which may be supplied for the Type 281-1E or 285-1E - are described below:

1. No automatic line disconnect; manual disconnect only.
2. Automatic line disconnect only by program:

   a. Type 281-1E

      Here line disconnect is accomplished by a PDT instruction having a control character C3 of octal 01. This instruction causes the communications control to send the single character specified by the A address, then to send a disconnect signal to the data set. When the disconnect signal has been sent, the control unit is disabled for five seconds.

   b. Type 285-1E

      Line disconnect is accomplished in the Type 285-1E by the "Special Strobe" PDT instruction. This causes the 285-1E to send a disconnect signal to the dataset. When the disconnect signal is sent, the 285-1E is disables for five seconds.

3. Automatic disconnect by means of the no-operation timer or program.

   a. Type 281-1E

      During reception, with an input instruction stored in the Type 281-1E, a period of inactivity on the line of approximately thirty seconds causes release of the assigned read/write channel. Approximately thirty seconds after this release - if there is still no activity on the line - the 281-1E sends a disconnect signal to the dataset and is itself disabled for five seconds.

      When no input instruction is stored in the Type 281-1E, a 30-second period of inactivity causes the line to disconnect and the 281-1E is disabled for five seconds.

      Line disconnect by program is accomplished as described in Section VI,C,2.

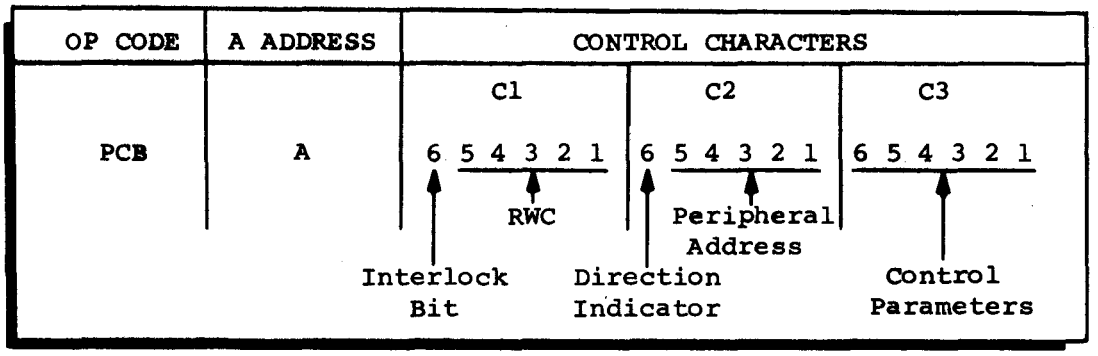
b. Type 285-1E

Because there is no instruction storage available in this unit, one 30-second period of inactivity on the line during transmission or reception, causes disconnection of the dataset and a five-second disablement of the 285-1E.

Line disconnect by program is accomplished as described in Section VI,C,2.

D. Peripheral Control and Branch (PCB) Instructions

1. General Format



A Address - This is the memory location to which the program branches (in a branching PCB instruction) if the condition tested by the PCB instruction is true.

Interlock Bit - The interlock bit is immaterial.

Read/Write Channel (RWC) - This selects the read/write channel between main memory and the peripheral device. C1 contains the number of the RWC being tested for availability and must be set to zero if no RWC is to be tested.

RWC1 = 01001 RWC3 = 01011
RWC2 = 01010 RWC1'= 01101

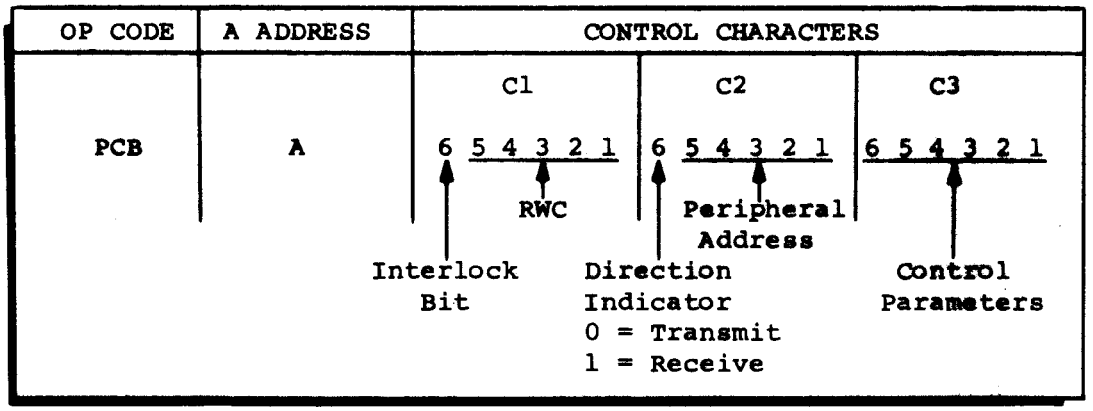
Direction Indicator Bit - This bit is immaterial.

Peripheral Address - This is the logical address of the communication control on the peripheral bus.

Control Parameters (C3) - The C3 character of the PCB instruction specifies questions and control for the Type 281-1E. Additional control characters may be used if required. See Table III, page 15, for the description and coding of C3.

E. Peripheral Data Transfer (PDT) Instructions

1. General Format



A Address - This contains the address of the main memory location to or from which data is transferred by the Type 281-1E. For Type 285-1E PDT instruction programming, see the reference bulletin Type 286-1, -2 and -3, Section VI,E.

Interlock Bit - If the interlock bit is a one, memory access is not granted to RWC1'. If this bit is a zero, memory access is granted to RWC1'.

Read/Write Channel (RWC) - This selects the read/write channel between main memory and the peripheral device.

RWC1 = 01001 RWC3 = 01011
RWC2 = 01010 RWC1'= 01101

Direction Indicator - This indicator shows the direction of data transfer.

1 = Move data from the Type 281-1E to memory location A, A+1,.... A+n, until a record mark is encountered.

0 = Move data from memory locations A, A+1,....A+n, to the Type 281-1E until a record mark is encountered.

Peripheral Address - This is the logical address of the communication control on the peripheral bus.

Parameters (C3) - See Table IV, below, for description and coding of C3 for the Type 281-1E.

Table IV. PDT Control Character C3

C3 (Octal)	Description
50	Present character being transferred to the control unit has even parity. This character is used when required for the LRC character. See Section VI,I, re: the LRC character.
01	Causes the control unit to send the single character specified by the A Address, then send the disconnect signal to the dataset. See Section VI,C, re: the disconnect capability.

Note 1. For the description on Type 285-1E programming, see the reference bulletin Type 286-1, -2 and -3, Section VI,E.

F. Record Marks and Character Location in Main Memory

1. Record Marks Required

a. The Type 281-1E Single-Character Method

When transmitting data by the single-character method, a record mark is placed in memory location A+1 to terminate a character. During data reception, a record mark in location A indicates character termination. At the termination of either reception or transmission, the RWC current location counter contains the address of A+1.

Table III. PCB Instructions for the Type 281-1E

PCB	Description	C3 (Octal)
Non-Branching		
1 Set Allow	Allows the Type 281-1E to interrupt the central processor.	71
2 Reset Allow	Prevents interrupts.	70
3 Reset Interrupt	Resets present interrupt by resetting Interrupt. Allows RNM instruction to be effective.	74
Branching		
4 Interrupt	Are Allow and Interrupt both set? If yes, branch to A.	75
5 Busy	Is the Type 281-1E busy? If yes, branch to A.	1Ø
6 Parity	Did any character have even parity? If yes, branch to A.	4Ø
7 Device Error	Has an error other than parity occurred? If yes, branch to A.	5Ø
8 Output Request	Is the Type 281-1E requesting data for transmission onto the line? If yes, branch to A.	6Ø
9 Input Request	Is the Type 281-1E requesting that the CP take received data? If yes, branch to A.	61

Note 1. PCB instructions numbered 1, 2, 3, and 4 exist on the Type 201 Central Processor only if the latter has Program Interrupt capability. They are standard on all other Series 200 processors.

Note 2. For Type 285-1E PCB instructions, see the reference bulletin, Type 286-1, -2 and -3, Section VI,D.

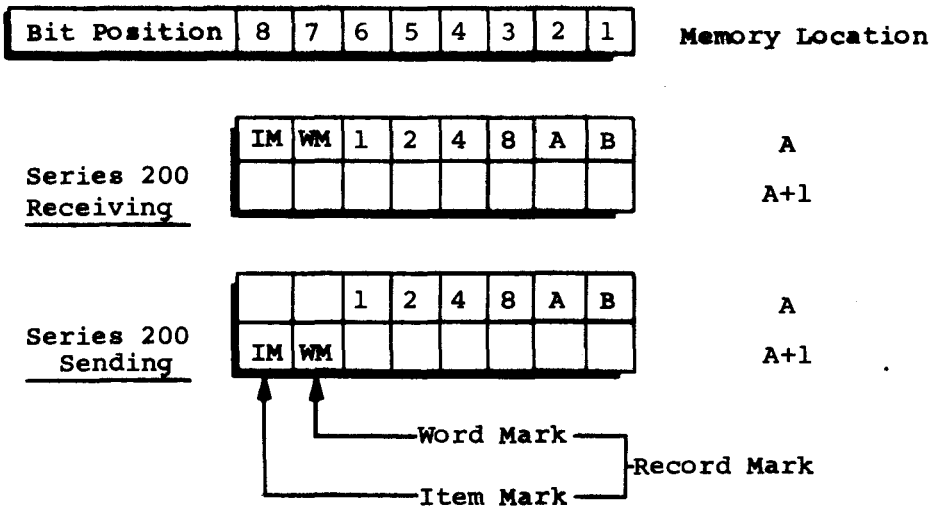
b. Type 281-1E Block Method

During block-method transmission, a record mark is placed in memory location A+n (n being the number of characters in a block) to terminate the transmission of a group of characters. Upon reception of data in the block mode, the record mark is placed in memory location A+(n-1) to terminate the message and release the read/write channel. At termination of either data transmission or reception, the RWC current location counter contains the address of A+n.

c. Type 285-1E

No record marks are required in transmission or reception of data in the case of this unit.

2. Character in Main Memory (Type 281-1E, Single-Character Mode)



NOTE

When the central processor is receiving, the C-bit (parity) is checked in the Type 281-1E and does not pass into main memory. When the central processor is sending, the C-bit is supplied by the Type 281-1E.

For Type 285-1E main memory character programming, see the reference bulletin, Type 286-1, -2 and -3, Section VI.

G. IBM 1050 Code in Series 200 Main Memory

Codes transmitted from IBM 1050 terminals or to them are shown Table V, below, as they appear in the Series 200 main memory. This table provides the basis for the Move and Translate (MAT) table.

Table V. Codes From or to IBM 1050 Terminals as Placed in Series 200 Memory

LETTERS AND NUMBERS

	IBM	1	2	4	8	A	B
	HONEYWELL	6	5	4	3	2	1
CHARACTER	OCTAL	BINARY					
1	40	1	0	0	0	0	0
2	20	0	1	0	0	0	0
3	60	1	1	0	0	0	0
4	10	0	0	1	0	0	0
5	50	1	0	1	0	0	0
6	30	0	1	1	0	0	0
7	70	1	1	1	0	0	0
8	04	0	0	0	1	0	0
9	44	1	0	0	1	0	0
Ø	24	0	1	0	1	0	0
A	43	1	0	0	0	1	1
B	23	0	1	0	0	1	1
C	63	1	1	0	0	1	1
D	13	0	0	1	0	1	1
E	53	1	0	1	0	1	1
F	33	0	1	1	0	1	1
G	73	1	1	1	0	1	1
H	07	0	0	0	1	1	1
I	47	1	0	0	1	1	1
J	41	1	0	0	0	0	1
K	21	0	1	0	0	0	1
L	61	1	1	0	0	0	1
M	11	0	0	1	0	0	1
N	51	1	0	1	0	0	1
O	31	0	1	1	0	0	1
P	71	1	1	1	0	0	1
Q	05	0	0	0	1	0	1
R	45	1	0	0	1	0	1
S	22	0	1	0	0	1	0
T	62	1	1	0	0	1	0
U	12	0	0	1	0	1	0
V	52	1	0	1	0	1	0
W	32	0	1	1	0	1	0
X	72	1	1	1	0	1	0
Y	06	0	0	0	1	1	0
Z	46	1	0	0	1	1	0

SYMBOLS AND CONTROLS

	IBM	1	2	4	8	A	B
	HONEYWELL	6	5	4	3	2	1
CHARACTER	OCTAL	BINARY					
.	67	1	1	0	1	1	1
$	65	1	1	0	1	0	1
,	66	1	1	0	1	1	0
@	02	0	0	0	0	1	0
/	42	1	0	0	0	1	0
#	64	1	1	0	1	0	0
&	03	0	0	0	1	1	0
-	01	0	0	0	0	0	1
BKSP	35	0	1	1	1	0	1
EOT	74	1	1	1	1	0	0
DELETE	77	1	1	1	1	1	1
DOWN-SHIFT	37	0	1	1	1	1	1
CR AND LF	55	1	0	1	1	0	1
PREFIX	76	1	1	1	1	1	0
IDLE	75	1	1	1	1	0	1
RDR STOP	54	1	0	1	1	0	0
SPACE	00						
EOB	36	0	1	1	1	1	0
UP-SHIFT	34	0	1	1	1	0	0
LF	56	1	0	1	1	1	0
TAB	57	1	0	1	1	1	1
RESTORE	15	0	0	1	1	0	1
BYPASS	16	0	0	1	1	1	0
EOA	64	1	1	0	1	0	0

The octal conversion of IBM 1050 characters is given in Table VI, below.

Table VI. Octal Conversion of IBM 1050 Characters

SERIES 200 Octal	IBM 1050	SERIES 200 Octal	IBM 1050	SERIES 200 Octal	IBM 1050
00	SPACE	30	6	60	3
01	-	31	0	61	L
02	@	32	W	62	T
03	&	33	F	63	C
04	8	34	UP-SHIFT	64	# also EOA
05	Q	35	BSKP	65	$
06	Y	36	EOB	66	,
07	H	37	DOWN-SHIFT	67	.
10	4	40	1	70	7
11	M	41	J	71	P
12	U	42	/	72	X
13	D	43	A	73	G
14	not used	44	9	74	EOT
15	RESTORE	45	R	75	IDLE
16	BYPASS	46	Z	76	PREFIX
17	not used	47	I	77	DELETE
20	2	50	5		
21	K	51	N		
22	S	52	V		
23	B	53	E		
24	Ø	54	RDR STOP		
25	not used	55	CR and LF		
26	not used	56	LF		
27	not used	57	TAB		

H. General Program Timing Considerations

The program must empty the Type 281-1E data buffer during the stop-bit time interval of 8.9 milliseconds. The program has a character time interval (68.18 milliseconds) to empty the data buffer of the Type 286 communication control associated with a Type 285-1E. If received data is not taken from the buffer of the Type 281-1E or Type 286 in the time specified, data is lost. In this event, the Type 281-1E Error switch

is set or an error indication is stored in the Type 286.

In the case of the Type 286/Type 285-1E, if a character is not sent by the central processor during the specified time, the last character transmitted is again sent by the Type 286, unless the program has issued a "Transmit Last Character" PDT instruction. For further details on Type 286/285-1E programming, see the reference bulletin, Type 286-1, -2 and -3, Section VI.

I. The LRC Character in the Type 281-1E

Transmitted and received LRC characters are the half-add sum of the data and parity bits of the message. The six data bits of the LRC character are supplied and checked by the program.

1. Transmission of the LRC Character

In transmission of the LRC character, the half-add sum of of the data bits is transferred to the Type 281-1E by means of a PDT instruction. If the message contains an odd number of characters, it requires no C3 control character. The message is transmitted with odd parity, which is correct. However, if the message contains an even number of characters, resulting in an even-parity LRC character, the PDT instruction to transmit the LRC character must have a C3 control character of octal 50.

2. Reception of the LRC Character

The LRC character is received as is any other data character, except that its parity may be odd or even, as described in Section VI,I,1, above. When the received message has an even number of characters but the parity error test shows odd parity, the received LRC character is in error. If the test for parity is satisfactory, the C-bit of the LRC character is correct, but the other six bits must be checked by the program.

J. Line Control Function of the IBM 1050 System

Line control is used by a central facility to control operation of a communication line servicing several stations. It is not required when only two stations are on a line; in this configuration, either station can initiate transmission. A Line Control switch within the cover at the rear of the IBM 1050 Control Unit regulates the function.

1. Operation With Line Control

The central facility puts all stations in the control mode by transmitting an End-of-Transmission (EOT) character identifying the next character as an address.

The address character conditions the selected terminal or terminals to receive the component-selection character. After the component-selection character is transmitted, the selected terminal responds with a positive answer if it is ready to receive a message, or with an End-of-Address (EOA) character if it is ready to transmit a message. A negative answer indicates that the terminal is not ready. No answer indicates the power is off at the addressed terminal. If the addressed terminal is ready to receive a message, the the central facility precedes its message with an EOA character.

The EOA character terminates the control mode for all stations and places the selected station in the data mode.

The EOA character is not included in the LRC character.

2. Operation Without Line Control

Without line control, either station initiates transmission by preceding a message with its prefix character, plus a component-recognition character. Both keyboard and reader are automatically recognized when an IBM 1050 terminal is reset.

The prefix and the component-recognition characters are included in the LRC character.

K. Series 200/Type 281-1E Interface Signals

1. Single-Character Transmission

The following paragraphs describe interface signals between the Type 281-1E and its Series 200 central processor for single-character transmissions.

a. Device Busy

The busy signal, when active, indicates to the program that a PDT instruction can not be be accepted by the control unit.

Busy is active whenever the read/write channel associated with a PDT instruction addressed to the control unit is busy, or the control unit is transmitting data to the line or receiving data from it.

b. Interrupt

The interrupt signal indicates to the program that the control unit is requesting service.

The Interrupt is set in response to the first "Set Allow" PCB instruction if the control unit is initialized. The

state of the output frame demand (OFD) or input frame demand (IFD) switch can not be guaranteed: either Input or Output Frame Demand can be present. If the IFD is present, a "Receive" PDT instruction is executed; if OFD is present, then the control unit is ready to accept a "Transmit" PDT instruction. Thereafter, the interrupt occurs whenever an OFD or IFD again becomes active.

The interrupt signal from the control unit is reset by one of the following: a PDT instruction to the control unit, a "Turn Off Interrupt" PCB instruction to the control unit, or initialization of the system.

c. Input Frame Demand (IFD) (Tested by a PCB instruction with C3 octal 61)

Input Frame Demand indicates to the program that a "Receive" PDT instruction is being requested by the control unit and must be issued to ensure proper operation.

The IFD signal becomes active when the control unit has assembled a character from the line and is ready to transfer it to the computer.

IFD is reset by the next PDT instruction to the control unit. If no PDT instruction is executed, the IFD signal is not reset.

d. Output Frame Demand (OFD) (Tested by a PCB instruction with C3 octal 60)

Output Frame Demand indicates to the program that the control unit is capable of accepting a "Transmit" PDT instruction.

The OFD signal is present when the control unit is not actively transmitting or receiving data or IFD is not active.

The OFD signal becomes active in the Transmit mode when the control unit is ready to transmit the next character. When receiving, OFD becomes active after one-half character time of inactivity on the line, provided that a PDT instruction has been executed to reset the IFD signal.

Output Frame Demand is reset by either a "Transmit" or a "Receive" PDT instruction or when the control unit senses a character on the line.

e. Timing Error (Tested by a PCB instruction with C3 octal 50)

This signal indicates that a data character has been lost in the control unit.

In the Receive mode, the timing error is set if a "Receive" PDT instruction is not issued in response to the IFD signal before the beginning of the next character is sensed on the line.

The timing error is reset by the next PDT instruction to the control unit.

f. Parity Even (Tested by a PCB instruction with C3 octal 40)

The parity even signal is associated with Receive mode only.

This signal is set if a character is sensed with even parity at the end of the character assembly time (when the IFD becomes active).

The signal is reset by the next PDT instruction to the control unit.

g. Turn Off Interrupt (Via a PCB instruction with C3 octal 74)

The "Turn Off Interrupt" PCB instruction allows the Resume Normal Mode (RNM) instruction to be effective without executing a PDT instruction to the control unit.

h. Reset Allow (Via a PCB instruction with C3 octal)

The "Reset Allow" PCB instruction prevents all future interrupts from the control unit. The present interrupt is not reset by this PCB instruction. Turn Off Interrupt or a PDT instruction is required before an RNM instruction is effective.

2. Single-Character Timing Considerations

a. Set Allow

The timing of the interrupt in response to the "Set Allow" PCB instruction is not predictable and should not be relied on for timing purposes.

b. Received Data

The data in response to a "Receive" PDT instruction is not guaranteed to be in main memory until 11 memory cycles after the end of the extraction of the instruction.

c. Transmitted Data

Data in main memory being transferred by a "Transmit" PDT instruction can not be changed until 14 main memory cycles are completed after the end of the extraction of the instruction.

NOTE

The read/write channel is busy until all data is transferred. The control unit is busy two main memory cycles longer than the read/write channel.

3. Message or Block Transmission

The following paragraphs describe the interface signals for message or block transmission between the Type 281-1E Communication Control and its Series 200 central processor.

a. Input Frame Demand (IFD)

The IFD signal becomes active when the control unit has assembled the first character of the message or block from the line and is ready to transfer it to the central processor.

The IFD signal is reset by the next PDT instruction and is not made active again by a character on the line until after the assigned read/write channel is released. This release may occur because of a record mark sensed in memory or because of a line inactivity time-out extending over approximately 30 seconds.

b. Output Frame Demand (OFD)

The OFD signal becomes active during transmission when the control unit is ready to transmit the next message or block.

When receiving, the OFD becomes active after one-half-character time of inactivity on the line, provided that the read/write channel has been released. If the read/write channel has not been released, an inactivity period of approximately 30 seconds is required before the release is effective; at this time, OFD becomes active.

c. Timing Error

When receiving, the timing error is also set if the read/write channel is released by the control unit after the 30-second inactivity time out.

L. The Type 285-1E/Type 286 "Special Strobe" PDT Instruction

The "Special Strobe" PDT instruction can be used by the program with a line in the Receive mode, causing the control unit to send a disconnect signal to the dataset. (For Type 285-1E programming, see the reference bulletin Type 286-1, -2 and -3, Section VI.)

VII. OPTIONAL FEATURES

A. Parity Check

Though odd parity checking and generation is standard in the Type 281-1E, no parity checking or generation is performed by the standard Type 285-1E. The odd parity check in the Type 285-1E/Type 286/IBM 1050 application is accomplished by installation of Feature 086 in the Type 286 communication control, in conjunction with programming (see the reference bulletin, Type 286-1, -2 and -3, Section VI,I).

B. Long Check

1. The Type 281-1E

Longitudinal check in the Type 281-1E/IBM 1050 application is accomplished by programming (Section VI,I).

2. The Type 285-1E

Longitudinal checking in the Type 285-1E/Type 286/IBM 1050 application is accomplished by installation of Long Check Feature 087 in the Type 286 Communication Control or by programming (see the reference bulletin, Type 286-1, -2 and -3, Section VI,H).

APPENDIX I

HONEYWELL/IBM 1050 APPLICATIONS

LINE	TERMINATION	HONEYWELL CONTROL UNIT
Voice-grade telephone	103A Data Set	Type 281-1E or 285-1E
Narrow-band line (i.e., TWX CE)	103A Data Set	Type 281-1E or 285-1E
Voice-grade telephone, private line	103F Data Set	Type 281-1J or 285-1J
Narrow-band line, private line (Bell-proposed 150-Baud)	EIA Termination	Type 281-1J or 285-1J
Narrow-band (WU 180 Baud)	WU Type 11725	Type 281-1K or 285-1K

NOTE

The following two categories of IBM 1050 applications are in use but will not be connected to Honeywell systems.

1) A Teletype-grade private line WU or Bell 75-baud service which is slower than the IBM 1050 capability.

2) Customer-owned lines using IBM-provided Model at both the computer and IBM 1050 stations.

APPENDIX II

REFERENCES FOR IBM 1050 SYSTEM AVAILABLE

AT

HONEYWELL EDP ENGINEERING

1. IBM Systems Reference Library
   IBM 1050 Data Communications System

   Introduction, Operating Features, Controls and Indicator lights, Special Features. (28 pages, 18 illustrations)

2. Original Equipment Manufacturer Information
   IBM 1050 Data Communications System

   General Description for OEM use, covers changes as of July 1963. (27 pages, 17 figures)

3. IBM Customer Engineering Maintenance Manual
   1050 Data Communications System

   General, Unpacking Instructions, Data Sets used, Cabling, Model 1 Home and Line Loop, Model II Line Only Data Channels, Switches, Control Keys, Codes, Correction Features, Line Control, Telegraph Grade Line Use, Customer and CE Aids, Diagnostic Tests, 1051 Latch and Trigger Descriptions. (124 pages, 20 illustrations)

4. IBM Customer Engineer Manual Of Instructions
   I/O Printer (Modified IBM Selectric)

   Printing, Character Selection, Operation-Control Mechanisms, Margin and Paper Control. (77 pages, 155 illustrations)

5. IBM Customer Engineering Reference Manual
   IBM Selectric Universal I/O Keyboard Printer

a.	Adjustments	44 pages	224 illustrations
b.	Removal	18 pages	61 illustrations
c.	Lubrication	11 pages	13 illustrations

   (73 pages, 298 illustrations)

6. IBM Customer Engineering Instructions - Maintenance
   1052 Keyboard Printer, 1053 Printer

   Introduction, Printing Controls and Indicator Lights, Adjustments. (34 pages, 50 illustrations)

7. IBM Customer Engineering Instructions - References

1057 Card Punch, 1058 Printing Card Punch Introduction, Punch, Printing and Non-Printing, EDB and LRC Operations, Interlock, Patch Panel. (22 pages, 13 illustrations)

8. IBM Customer Engineering Manual of Instruction
1056 Card Reader

Functional Units, Reader Operation, Wiring Diagrams.
(21 pages, 16 illustrations)

HONEYWELL EDP TECHNICAL PUBLICATIONS
USERS' REMARKS FORM

TITLE: Types 281-1E, 285-1E
Communication Units

DATED: October 27, 1965

FILE NO: 112.0005.1100.0-061

ERRORS NOTED:

Fold

SUGGESTIONS FOR IMPROVEMENT:

Fold

FROM: NAME _____ DATE _____

COMPANY _____

TITLE _____

ADDRESS _____

_____

Cut Along Line

FIRST CLASS
PERMIT NO. 39531
WELLESLEY HILLS
MASS.

BUSINESS REPLY MAIL

No postage stamp necessary if mailed in the United States

POSTAGE WILL BE PAID BY

HONEYWELL
ELECTRONIC DATA PROCESSING DIVISION
60 WALNUT STREET
WELLESLEY HILLS, MASS. 02181

ATT'N: PUBLICATIONS AND WRITING SERVICES DEPARTMENT

Cut along Line

Honeywell
ELECTRONIC DATA PROCESSING