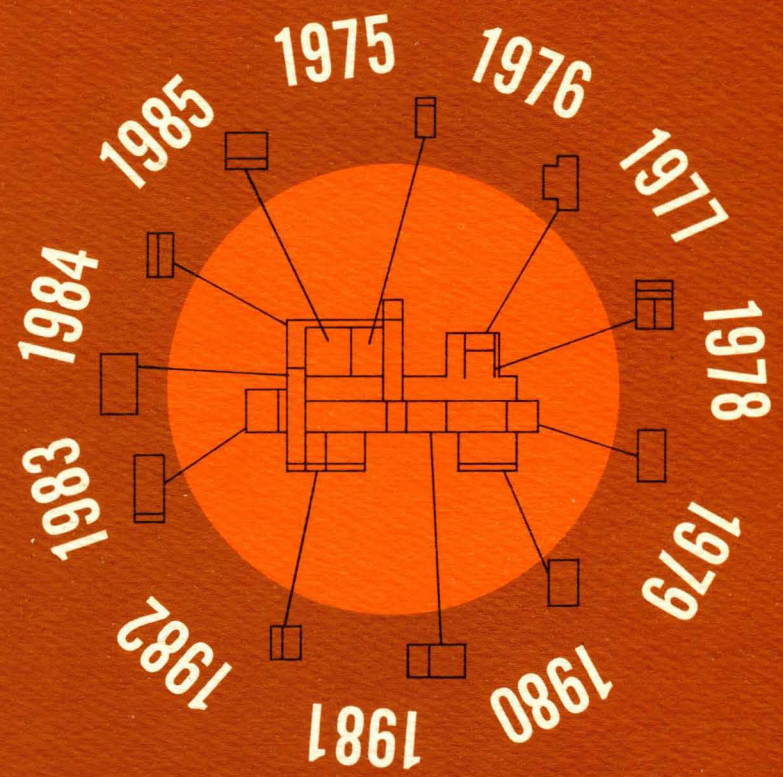# MILDATA

AN OPTIMIZING STUDY OF A MODULAR DIGITAL COMPUTER SYSTEM

Contract Number

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Final Report

Volume II

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MILDATA STUDY

Final Report

Volume II

12 August 1963 to 30 September 1964

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all aspects of data processing
applicable to CCIS in the time
frame 1975-1985.

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APPENDIX A

APPENDIX A

Applications

A.1. Introduction

The major delineations found in the applications area of MILDATA are dictated by Army doctrine and experience. The areas where some computer processing already exists are Logistics, Intelligence, Fire Control, and a grouping called Personnel and Administration. Superimposed upon these areas are Command and Control requirements which in some instances use these facilities and in some instances impose a totally new set of requirements on the loose system made up of the equipment applied to the foregoing areas.

The MILDATA system of the 1975-1985 era will very likely be an extension of this very general structure, but utilizing faster and radically more powerful equipment, communication facilities which are at the same time internal links in the system, and external links to the user, and operating in an environment that is at once global and local.

It is not inconceivable that the array of weaponry available to the combatants in this time era will be so formidable that actual use of all of them in combat would be unlikely and the utilization of military force for political gain will have ceased to be profitable in the cold war.

In such an environment the skill of analysis combined with the quickness of response will be the most effective weapon and the side which can demonstrate that it can use its weaponry and survive will win.

Attendant on such a theory, admittedly over-simplified, is the mounting need for centralization of information from an ever growing and expanding system of information gathering sensors. The function of information reduction and display will be central to the system design, and the system which can enrich the picture thus generated will be valuable to the man who must evaluate all the information and select a course of action.

Within this frame of reference the description of the application for future systems must be considered.

The computer system of the future (1975-1985) will likely lose its identity as a computer entity and emerge as an integral part of a larger system which is designed as a fast-reacting military shield with two purposes; to coerce the enemy from using his weaponry and to protect the United States and its allies from the effect of this weaponry if it is employed. Intrinsic to this system will be a wide and varying network of surveillance communications and countermeasures devices. A new aspect of this type of warfare will be the need to keep the enemy briefed on our capability in order to prevent a disastrous underestimate of our capability and our resolution to use it. Regular demonstrations of this strength on a global scale is one way to accomplish this, another way is to build a military system that is as quickly effective on a limited warfare basis as on an extended warfare basis. The enormous amounts of information available for analysis by a commander must be capable of utilization both in actual warfare and in the para military - political - economic half world in which the military operates today and will for the forseeable future.

The basic skills required to utilize the integrated system must be delineated and analyzed so that they may be taught to the various echelons of responsible rank within the Army organization. The system must be so designed that it supplements the basic skills found in each rank within the Army and at the same time enhances the fighting effectiveness of each occupant of these ranks. Only if these considerations are foremost throughout the design of the system can the system be properly integrated into the Army structure without causing a major disturbance of both structures. A quick integration of the system into the Army is desirable to prevent the debillitating effect of protracted phasing in and out of equipment in the traditional manner.

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A.2. Personnel and Administration

Under the category of work included in the Personnel and Administration Subsystem is found the Personnel Management and Control function, Financial, Medical, Discipline, and Special reporting (see Table A-1 (Personnel and Administration)). None of these work categories offer anything very new in the way of data processing requirements in that they are essentially information storage and retrieval problems, with file maintenance procedures of varying efficiencies the measure of effectual usage of the computer/data processor. Such work as this is a sustaining work factor in the system and, for purposes of the Mildata system, can form a segment called the backlog job area.

The backlog area is the sustaining job area in which resides the job pool from which the system draws when it has satisfied all priority processing requirements. When system processing power becomes available due to completion of high priority jobs, or a null period occurs in the real time demands upon the system, the System Control immediately takes account of which and how many systems components are available and then compares the contents of the backlog job pool against the available system components and processes the jobs for which components, files, and time are available. In the event that a job in the background pool becomes a priority job due to the passage of time, and the priority load on the systems is such that it can be handled on a priority basis, it will appear as though it were a new priority job just entering the system queue.

It can be seen that the system under these circumstances must be as powerful and efficient as possible. Moreover, the storage and retrieval of file items and the manipulation of blocks of data become high rate of occurance items in the system operation. It is also evident that to function in such an environment the Compile, Assembly, and Translate functions have to be held to a minimum general system requirement and to be monitored, maintained, updated or modified by a central group of people who have this responsibility exclusively. In short, a Systems Software Maintenance Group, enjoying a status as a high priority users group, will probably be a continuing requirement in the system. Each of the earlier distinguished job areas; i.e., Intelligence, Fire Control, Logistics, and Personnel and Administration must have representation in this group. This group's responsibility will be great but briefly stated is as follows: keep the compiler efficient and general, make the object programs as short and fast as possible and arrange them so as to lend

themselves easily to segmentation. The latter requirement is
to enable easy and fast system response to real time interrupt
requirements on the system.

   In addition to real time interrupt provision the type of
system being proposed in this report entails an adaptive response
capability. The Self adaptive aspect lies in the ability of the
system to react to an unprogrammed for demand in the system by
combining segments or pieces of programs and pieces of equipment
to service the requirement in an unanticipated manner. This is
possible only if the software array in the system is segmented
into meaningful programming units, meaningful not only to the
program of which it is a part, but also meaningful to an analytical
control program which is attempting to match system demand jobs to
system programming response.   A further potential gain here is
the possibility of the analytical control program being refined
to a point where it can choose between alternative software and
hardware configurations in responding to a request from the
regular job sources. It is easy to see the value of this power
in being able to initiate or continue critical processing even
though parts of the system are disabled or busy with other high
priority work. Such processing needs as are represented by
Personnel and Administration could essentially be serviced in
parallel with priority jobs, depending on the availability of
the system equipment segments to meet the job requirement; i.e.,
the right number and type of tape drive, the right tape reel on
the drive, the necessary memory space, etc.

A-5

System	Function	Input	Processing	Output	Files	Frequency
Personnel Manage-ment and Manpower Control	Personnel Record Keeping	Reports from all other P & A Sections	File Maintenance	Updated File, Hard Copy	Master Record	Daily
	Individual Replacement	Replacement Requests and Re-assignments to Duty	File Maintenance, Report Generation, Personnel Assignment	Updated File, Hard Copy Report	Master Record, Strength Accounting	On Demand
	Casualty Reporting	Admittance Report	File Maintenance, Report Generation Casualty Reporting	Updated File, Hard Copy Report	Master Record, Strength Accounting, Medical Accounting	Daily
	Rotation	Rotation Request	File Maintenance, Report Generation	Updated File, Hard Copy Report	Master Record, Strength Accounting	Cyclic Basis
	Graves Registration	Death Report	File Maintenance, Report Generation	Hard Copy Report, Updated File	Master Record, Strength Accounting	On Demand
	Personnel Locator Service	Personnel Locator Request	File Maintenance Report Generation Locating	Hard Copy Report, Updated File	Master Record, Strength Accounting, Locator	On Demand
	CBR Status Report	CBR Input from Field	File Maintenance Report Generation	Hard Copy Report, Updated File	Master Record, Strength Accounting, Medical Accounting	On Demand
	Manning Report	Report by Exception	File Maintenance	Updated File	Master Record, Strength Accounting	Daily
Financial Services	Military Pay	Data from Master File, Payroll Requests	Data Processing, File Maintenance	Hard Copy Report and Checks, Updated File	Master Record, Payroll	Cyclic Basis
	Funding	Expenditure and Fund Request Reports	Data Processing, File Maintenance	Hard Copy, Updated File	Funding	Cyclic Basis
Medical Services	Patient Accounting	Admittance and Discharge Reports	File Maintenance, Report Generation, Statistical	Hard Copy Report, Updated File	Master Record, Strength Accounting, Medical Accounting	Daily

TABLE A-1

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System	Function	Input	Processing	Output	Files	Frequency
Medical Services (continued)	Strength Accounting	Manpower Control Reports	File Maintenance, Report Generation, Statistical	Hard Copy Report, Updated File	Strength Accounting, Medical Accounting	Daily
	Medical Regulating Reports	Patient Accounting Reports, Evacuation Reports	File Maintenance, Report Generation	Hard Copy Report, Updated File	Medical Accounting, Strength Accounting	Daily
Discipline, Law and Order		Prisoner of War Records and Reports, Intelligence System File on Area	File Maintenance, Report Generation	Hard Copy Report, Updated File	POW File, Intelligence System Files	On Demand
Special Reports		Promotion Reports, AWOL Reports, Special Report Requests	File Maintenance, Report Generation, Data Processing	Hard Copy Report, Updated File	Master Record, Strength Accounting, Special Purpose	On Demand

In Figure A-1, entitled "System Expandibility Pattern" is a module entitled Minimum Associative Module. This is an operating computer module organized on an associated basis, much as described in the Third Quarterly Report (see Figure A-2). One of the main reasons for the presence of such a module in the MILDATA System will be to function in direct connection with the analytical control program cited above. This module should contain all of the necessary hardware and memory to implement the analytical control program; i.e., it will be associatively organized with all of the status registers and content addressable memory to permit the maintenance of a large descriptor matrix which can be quickly searched due to its content addressability and which will provide the necessary pointers to indicate applicable algorithms in the system and initiate the concatination of the algorithm subprograms or segments to generate the necessary object program for the job at hand. Good systems design should permit parallel processes here which will permit the execution of this process without interruption of processing on other modules. The increase in depth of knowledge of how to improve the primitive analytical control program, will permit the expansibility indicated in Figure A-1 cited above. Under this system design, background jobs (or sustaining jobs) could be serviced continuously up to the capacity of the system modules at hand.

It seems reasonable to assign the function of Personnel and Administration processing to the background job pool with the rough requirements that the processing requirement will be satisfied on a 24 hour basis. The estimated processing load in terms of Function, Input, Output, Files size and description and the frequency of reoccurrence of job, can be quickly inspected by looking at Table A-1. From this table, it can be seen that the natural segmentation of the processing load would be very convenient for processing as a background job.

Figure A-1. MILDATA Systems Expandability Pattern

A-8

Figure A-2

A-9
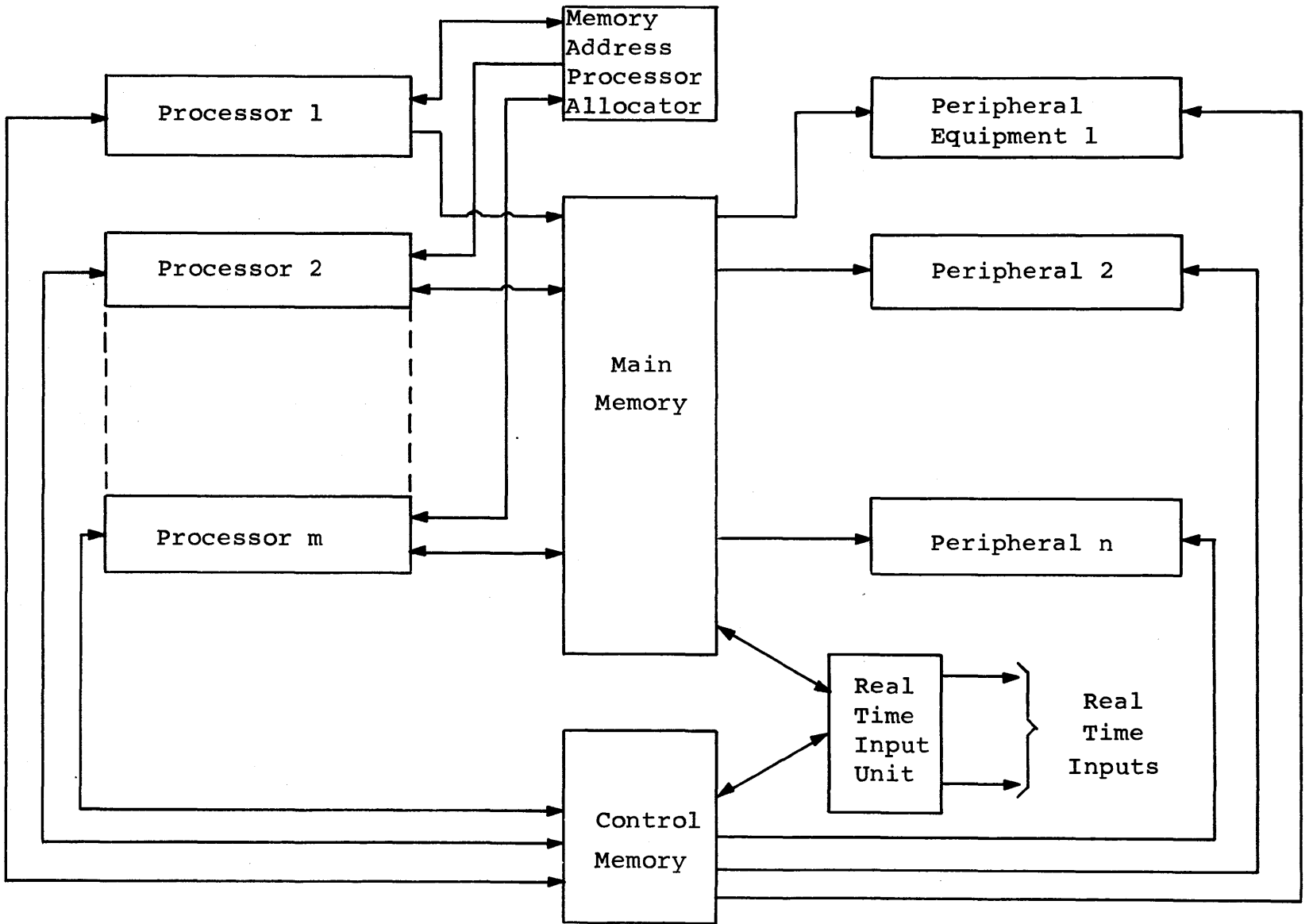
A.3. Logistics

Under the category of work in the Logistical Application is found Supply, Transportation, Evacuation and Hospitalization, Maintenance and Administration Planning (see Table A-2). In these areas are found good applications for the most advanced business type data processing techniques and equipments. Here is the area where a genuine increase in efficiency of the Army fighting machine can be realized. The files of parts, spares, food, clothing, ammunition are very large and diversified. They are also very active requiring almost constant updating, and processing. It will be very important to the Army Logistical Units of the future that the manner of use of the data processing equipment available to it be dictated by the strategic and tactical situation in which it must operate. The forcing of the Logistical Data Processing requirement into a mold designed for it by System planners, without regard for the quickly changing environment will negate the more obvious gains in efficiency and will ultimately lead to the acquisition of specialized equipments with low frequency of use and great weight in the scale of overhead and rear echelon loading. The system of 1975-1985 must accommodate the Logistical load along with the other sections of data processing and have the same efficiency as the others. A greatly increased strategic value is shown here when the extreme mobility of fighting units of the future is considered. On one hand a large array of weaponry and consequent fire power must be transported with the fighting man but his means of transport is likely to be airborne and therefore weight limited and somewhat vulnerable. He cannot be over or under supplied with the necessities of life and fighting power. As closely as is humanly possible he has to have at hand the right weapon for the tactical situation he faces, and an adequate supply to take, hold and/or destroy the objective depending on the situation with which he is faced. The enemy is apt to be of a type who is trained to seize his weapon and ammunition from a fallen enemy, likewise his food and clothing, where the situation permits. The creation of close-to-the-front supply depots generates an almost irresistable attraction not only for the undersupplied enemy soldier, but for the indigenous population who are theoretically on our side. Good logistics planning and solid machine support for this planning can eliminate the close in location of supply depots and deny the enemy this source of supply for his foragers. Further, it will increase the burden on

his own supply lines which are equally sensitive though not so exposed as ours.

Transportation is another important facet of logistic operations. The transport and support of an army fighting unit in the tactical situation of the future will be a highly integrated and coordinated operation whose success will depend on tremendously detailed timing and advanced simulation of the combat situation and the power (fire & man) needed to assure success. The enemy can out-man us numerically for the rest of this century so judicious use of superior technology, adapted to rigorous climactical environmental conditions, is the best tactic in the para-military combat of 1975-1985, and at the same time intrinsic to the Posture of the U. S. Army vis-a-vis, the more traditional military units confronting it in Europe.

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System	Function	Input	Processing	Output	Files	Frequency
Supply	Requisition Processing and Replenishment	Requisition Requests, Replenishment Report, Fire Support Requests	File Maintenance, Availability, Physical Inventory, Report Generation	Hard Copy Report, Updated File	Supply Inventory	On Demand
	Demand Analysis	Demand and Consumption Reports	Requirements Analysis Report Generation	Hard Copy Report	Supply Inventory	On Demand
	Physical Inventory	Request for Inventory of Specified Classes or Items	File Search, Report Generation Physical Inventory	Hard Copy Report	Supply Inventory	Cyclic Basis
	Fiscal Control and Audit	Audit Request, Fiscal Accounting Request, Construction Requests	Data Processing, File Search, Report Generation	Hard Copy Report	Supply Inventory	On Demand
Transportation	Intransit Accounting	Bills of Lading, Cargo and Freight Movement Reports	File Maintenance, Report Generation, Data Processing	Hard Copy Report, Updated File	Transportation, Supply Inventory	Daily
	Transportation Capability Forecast	Forecast Requests	File Search, Report Generation, Transportation Planning	Hard Copy Report	Transportation, Supply Inventory	Cyclic Basis
	Cargo and Freight Movements	Bills of Lading, Intransit, Accounting Reports	Report Generation, File Maintenance, Transportation Planning	Hard Copy Report, Updated File	Transportation, Supply Inventory	Daily
	Highway Traffic Regulation and Control	Road Reports	File Maintenance, Report Generation	Hard Copy Report, Updated File	Traffic	Cyclic Basis
	Integrated Movements and Supply	Supply Reports, Bills of Lading, Intransit Accounting Reports	File Maintenance, Report Generation,	Hard Copy Report, Updated File	Transportation, Supply Inventory	Daily

TABLE A-2

LOGISTICS
(Continued)

System	Function	Input	Processing	Output	Files	Frequency
Evacuation and Hospitalization	Accounting for Patients	Admittance and Discharge Reports	File Maintenance, Report Generation, Statistics	Hard Copy Report, Updated File	P&A Master Record, Medical Accounting, Patient Accounting	Daily
	Forecast of Patient Load	Patient Accounting Reports	File Search, Report Generation, Statistics	Hard Copy Report	Patient Accounting, Medical Accounting	Daily
	Bed Requirements and Availability	Patient Accounting Reports	File Maintenance, Availability, Report Generation, Statistical	Hard Copy Report Updated File	Supply Inventory, Medical Accounting, Patient Accounting	Daily
	Evacuation Requirements and Capability	Patient Accounting Reports, Transportation Capability Reports	File Maintenance, Report Generation, Transportation Planning	Hard Copy Report, Updated File	Medical Accounting, Patient Accounting, Supply Inventory	Daily
	Clinical and Diagnostic Records	Lab and Medical Reports, Patient Accounting	File Maintenance, Report Generation	Hard Copy Report, Updated File	Medical Accounting, Patient Accounting	Daily
Maintenance	Forecast of Requirements	Requirement Requests	File Search, Report Generation, Statistical	Hard Copy Report	Maintenance, Supply Inventory	Cyclic Basis
	Capability and Allocation of Units	Disable and Damage Reports, Damage Control Reports	File Maintenance, Report Generation, Data Processing	Hard Copy Report, Updated File	Maintenance, Supply Inventory	Cyclic Basis

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LOGISTICS
(Continued)

System	Function	Input	Processing	Output	Files	Frequency
Adminis-trative Planning	Administrative Orders and Estimates	Financial Reports, Equipment Reports, Manpower Reports	Report Generator, File Maintenance, Data Processing	Hard Copy Report, Updated File	Administrative, Master Record P&A	Daily
	Administrative Unit Distribution	Manpower Reports, Organization Changes	File Maintenance, Report Generator, Data Processing	Hard Copy Report, Updated File	Administrative, Master Record P&A	Daily
	Construction Requirements	Damage Control Reports Requests for Con-struction	File Maintenance, Report Generator	Hard Copy Report, Updated File	Supply Inventory Administrative	On Demand
	Damage Control	Disable and Damage Reports, Maintenance Reports	File Maintenance, Data Processing, Report Generation	Hard Copy Report, Updated File	Supply Inventory, Maintenance Administrative	On Demand

A-14

Underlying all of the above requirements for swift and dependable transport, quick and adquate supply, maintenance of a fabulously varied array of equipments, expenditure of money of heroic proportions to support these large endeavors is a continuing demand for positive control, positive knowledge of levels of supply, positive figures on necessary lead time for procurements, positive accountancy of supplied expended, where and by whom, for what purposes. The positive nature of the required information requires an integrated system of data processing equipment, communication equipment, transportation equipment and scheduling (see Table A-2), which goes far beyond anything accomplished by the military previously. Building such a system surely requires recognition of the details of the problem in depth. The growing science of army logistics can supply a great many of these details and the work load presented by logistics to the MILDATA system will be a sizable portion of the total load.

In the interest of keeping the problem manageable, it would seem to be worthwhile to adopt the most efficient File organizations found in the business world of the data processing. Army part numbering systems, the traditional numerical organization of part and number was efficient in the past but is no longer efficient and certainly not in the era under consideration. Any system which depends on human awareness to ferret out redundancies, repetitions, etc., cannot cope with the enormously expanding assemblage of items required by the fighting unit of the 1975-1985 time frame. Only a highly efficient combination of data processor, communication, data gathering and man-machine interfaces can cope with this problem and only highly imaginative, and, at the same time, technically sound system design can solve the problem.

At this point it will be assumed that we will now have the two major factors which combined will make up the "background" work load for the system processing load. Personnel and Administration plus Logistics will be the job source for all unassigned systems time plus sources of priority processing when the situation requires it.

A great deal of the intricate inter-relationship between transport management, Food, Fuel, Clothing and Ammunition Management, is easily handled on today's Data Processing systems. These items of work begin to acquire serious proportions of the work load only when their processing requirements clash with the pro-

cessing requirements of the other working areas; i.e., Fire Control or Intelligence. At the same time, future tactical situations may not permit delaying Logistic processing in the traditional manner. An advantage of the Expandibility design is the linking in of additional capacity on demand, via communications link, or even air dropping additional modules if the situation required. The important thing is to have the control program intact, on hand, and accurate figures as to equipment requirements for expanded processing capability.

FIRE SUPPORT SUBSYSTEM

	Input	Processing	Output	Files	Frequency
Ammo. Status	Battery	File Merge & Update	Hard-copy Listing Fire Planning	Logistics Ammunition file	at completion of each fire mission
Fire Unit Status	Battalion	File Merge & Update	Visual Display Fire Planning	Artillery Status file	Continuous
Artillery Fire Planning	Division Forward Observer	Data Analysis	Visual & Hard-copy	Artillery Status file	Daily
Artillery Survey	Battalion	Solution of Algebraic Equation	Visual Display	None	Continuous
Artillery Target Intelligence	Division	Information Retrieval	Hard copy & Target List	Intelligence O.B. files, weather & terrain files	Continuous
Fire Support Coordination	Division	Data Analysis	Visual Display	Artillery Status file	Continuous
Nuclear Target Analysis	Division Forward Observer	Statistical Analysis	Hard copy	Intelligence Weather & Terrain files	As required
Tactical Fire Control	Battery Forward Observer	Linear Program	Visual Display	Ammo. file Status file	Continuous
Technical Fire Control	Battalion	Solution of Differential Equation	Visual & Hard copy	None	Continuous

TABLE A-3

A.4. Fire Support (Control)

The third segment of the work areas of the MILDATA system is that of Fire Support (Control). (See Table A-3). Once again Army doctrine and experience have placed the responsibility for processing this area of work squarely on the functioning data processor center for the Army of 1975-1985 era.

The Army touch-stone of success in this time period will be mobility. Again the real power of the future Army will be its ability to get to the right place at the right time with as much coercive power as can be generated. By evidencing again and again the willingness and ability to use this mobile power anywhere on earth, the Army can eventually diminish the <u>rewards</u> accruing to any real or potential agressor. A succession of confrontations on a global basis, accompanied by the growing confidence of indigent peoples in the United States', willingness and ability to protect their young Democracies and prevent subversion of their Constitutional powers under the Aegis of the United Nations, or otherwise, will make the profit from military adventuring and subversion minimal, or even negative and further, a succession of defeats in these circumstances will damage the power image of the "agressor".

To accomplish this, there is a continuing demand for competent, fast, computational power to complement the complex weaponry of the Army and to direct it. Intrinsic to the complicated nature of the weapons is a demand for simpler methods of implacement and use. These weapons systems are potentially dangerous to the user as well as the target. Simple and safe methods for preparation and use of the weapon can be evolved with computer support. The simplicity thus achieved can be equally important in contributing to the mobility which is so valuable to the future Army.

Quick analysis of targets and quick computation of weapon requirements for the purpose at hand can have a direct effect upon the difficult job of logistical support for the fighting unit in what will consistently be an inconvenient geographical area. Victory in the encounter will depend on early and effective application of the weapons at hand to the targets of greatest strategic and tactical value. To achieve this a fast and extensive correlation of weapons, fire power, and range, target evaluation, intelligence estimates, logistic support and manpower availability will have to be accomplished. Some of this integration must be initiated before the undertaking

of the operation; however, the entry of the final variables
into the computation will often have to wait until the site for
the encounter is chosen and the enemy engaged.   This entry will
have to be easy to accomplish, and very likely will be via a
remote operation channel, generated by a surveillance sensor or
by a forward observer at the end of a very narrow information
transmission path (probably one way).

The net result of this sequence of operations should be
the exact targeting of the objective and a near perfect
coordination of the local effort with the overall plans and
policy of the area commander.

It follows, therefore, that the computational power re-
quirement is high and the communications facility extensive and
that they are both parts of one and the same system. The com-
puting equipment will be modular, permitting the coupling of a
number of modules to meet the exact requirements at the site,
it will be ruggedized at least to the same degree as the weaponry,
and it will have the ability to function with equal facility as a
communications controller and link allocator.   The commitment of
weapons, the use rate of ammunition, the kind of ammunition,
(high explosive or nuclear), the evaluation of target, the si-
tuation report and overall tactical summary of the action, ac-
complished and contemplated, will all be functions of the
integrated center and will represent peak processing require-
ments when they occur. In contrast to the Personnel and Adminis-
tration and Logistics processing requirements the Fire Control
requirements will be a high priority segment of the load and will
occur at irregular intervals-so cannot be a part of the background
job area but must be part of the priority processing load opera-
ting in a real time environment and responsive to both remote
usage and evaluation within the computer center.

Included in the main body of this report is a system
configurator which contains the elements of system composition
anticipated as adequate to the system demands of the future.
This configurator can be applied against the immediate needs of
the Fire Control site or against the integrated needs of a Field
Army Headquarters. It contains all of the possible combinations
of the different components available to meet a small computer or
a large System requirement. It further provides for utilizing
new developments when they are available in such areas as communi-
cation devices; i.e., voice input, or perhaps wall display output

for situation reporting. For the time in question in this study, all of the major systems components represented in this Configurator are considered to be available to the systems designer. Further, this array of System Components will permit the combination of components for new and unanticipated applications with the result of providing special purpose processes if required.

With the inclusion of the Fire Control processing load into the MILDATA system requirement, a new element in the system design emerges. This is the element of priority processing. For this requirement, provision must be made for computer availability under all circumstances. The inclusion of the computer as an integral part of the weapon system automatically generates a survivability and availability requirement at least equal to the weapons themselves. It is imperative that the arrangement of systems components be such as to assure a computation capability when only the smallest incremental unit of the system is operating. This requirement is equally applicable for both software and hardware components. It is from this perspective that Honeywell is proposing the Systems Expandability Pattern of system architecture.

INTELLIGENCE SUBSYSTEM

		Input	Processing	Output	Files	Freq.
Order of Battle	Infantry	Outpost Observa. Civilian Interroga. Spec. Recon.	File Update Queue Management File Search Prog. Library Maint. Exec. Prog. Cont. Matrix	Listing Routing, Visual Display	Numerical Order Admin. Order Geographic Order	Daily Weekly Monthly Annually
	Artillery	Same	Same	Visual Display, Plotter Display	Same	Same
	Mechanized	Same	Same	Listing Visual Display Plotter	Same	Same
PERSONALITY	Command Structure	Prisoner Interroga. Citizen Interroga. Intercept Observer-Recon.	Garble Eliminate Info. Corroboration File Update	Listing Report General. Visual Display	Administration Alphabetical-Name Skills	Demand
	Alphabetical	Same	Same	Same	Same	Demand
	Specialized by Function	Interrogation Observed Specialization	Same	Same	Skill File Special Training	Demand

TABLE A-4

	Input	Processing	Output	Files	Freq.
Recon Processing	Spec. Recon Infiltrators Air Surveillance	File Update File Search Rept Generator	Listings Visual Display/ Spec Rpts	Terrain Info Weather Info OB File Psy File	Periodic Demand
Weaponry Array Capability	Publications Parades Diplomatic Interrogation	File Update Rpt. Generator File Search Capability Computation	Analytical Reports	Weapons Certified Tested Estimated	Continuous
Psy Factor	Time under fire Intercept Logistics & Comfort health	Situation study Report generation	Reports Listings	OB Pers. Spec. functions	Periodic
Weather Terrain	Meteorological Terrain Study Photo Analysis	Weather Prediction Terrain Analysis	Same	Meteorlogical Terrain Profiles	Continuous
Counter Intelligence	Current Objectives Known Psy Factors	Resource File Estimation of Enemy knowledge Recommendation Computation	Reports Battle Plans	OB-Pers Terrain Weather Psy Factors	Demand

C O M B A T   I N T E L L

A-22

A.5. Intelligence

The value of Intelligence in a military operation is a function of its accuracy and timeliness. The instances when a particular military secret of the enemy suddenly becomes available to the Army - enabling victory in the immediate battle and ultimately leading to final victory, are very rare. Such secrets may be a revelation of some intrinsic weakness in the enemy defense posture or in his attack plan. In modern warfare, it would be inadvisable to assume any such weakness. It is much better to ascertain the enemies motivation, his strategic needs, his logistical system, and his morale. Information on the enemy in these areas is usally obtained by reducing a large mass of data to a manageable few reliable items of information.

The science of intelligence information generation is contained in the methodology of analysis, its completeness and the speed with which it can be applied. When data processing methodology is applied to intelligence generation (see Table A-4) Intelligence Subsystem) certain traditional similarities to more prosaic data processing requirements appear.

The first is the gathering together and ordering a large number of individual items. The relationship between these items may not be evident at first. In some cases the sheer number of items involved prevents immediate calculation and comparison, hence the relationship between the items is not immediately ascertained. An alternative approach is to set up an area of interest procedure in which general file categories are arbitrarily delineated and all incoming items are inspected for relevance to these categories. In some cases, an item may fall into all of the category files - same item but of interest in a different way to each of the files. In this manner a duplication of file items occurs but it is justified by the speed it permits in searching a particular file rather than using a cross referencing system to locate the item in question. So what we have seen here is a multistep process. The item in question must be identified for validity; for interest, and then inserted into the interested file according to the file organization.

Let us take an example - an item appears as follows - A _Russian_ national is identified as a _military_ person, belonging to a certain _artillery section_, of a certain _Artillary Army_, with

with a certain Order of Battle number. It is conceivable that in the above item five areas of interest are contained. If he is determined to be Russian – this is important, particularly if he happens to be in Vietnam, also if he belongs to an Artillery Section which is thought to have Atomic capability – this is of interest; also if his Artillery Army was thought to be in East Germany, that is of interest, and finally if all of the foregoing is true, then the order of battle of the Russian Military in East Germany may have to be reexamined. Thus we see that our very small item of interest involves five (5) items of high interest, ten (10) items of colation and checking, and implicit in this a relatively large amount of data processing. This very simple example should also serve to illustrate the importance of quick cross checking between such apparently un-related Files as Logistics and Fire Control to produce the secondary information implicit in the item once its primary information was extracted and incorporated into the concerned files. Thus we see the Order of Battles file, the Personality File, and the Combat Intelligence file primarily involved in processing with secondary involvment of Diplomatic Files, Artillery Geographical Files, Artillery Capabilities Files and possibly Atomic Weapons Files involved on a less immediate basis. To sum up – the method of analysis and the broad data base are the two main supports for successful production of Intelligence information.

The next requirement is timeliness. Very few things lose their value so quickly as Intelligence information. What is critically important and highly useful one day may be worthless clutter in your files the next day. It is, therefore, imperative that the end product (Intelligence) be produced as promptly as possible, in as complete a form as possible (i.e., having all secondary information brought out) and that duplicate and obsolete items be deleted from the various files as quickly as possible. The last is important because the size of the file is an important factor in the speed with which an item can be processed. It follows that the files should not only be kept of manageable size but as small as possible and still be complete. A secondary store, possibly off line, may sometimes be of great value in keeping a complete file of Active Items and a historical grouping at the same time. (The presence of a file of items, present for reason of historical interest is questionable in a field installation, but such a file should be present in the system somewhere, perhaps at the Army Headquarters)

A-24

From the foregoing, it can be seen that the principle method for producing Intelligence information is one of Information Storage and Retrieval plus effective analytical procedures. The MILDATA system of 1975-1985 must offer considerable improvement in both areas of processing.

A.6 Command and Control

The function of Command and Control is superimposed on the four functions discussed in this commentary on MILDATA applications. Fire Control, Intelligence, Logistics, etc. are committed to Data Processing in this system as the sustaining and continuing load.

It would seem that if the extreme mobility talked of for the 1975-1985 time period is to be used effectively, then the calculation and planning needed to support a choice of Strategy and an implementation of Tactics in support of the Strategy would require extensive computer support. This support can run the gauntlet from simple collation and comparison to the more sophisticated technique of gaming and trial decision analysis. The Commander's use of the information available to him from the data processing area is optional, and based upon his confidence in the information and the use to which he put it.

Intrinsic to such a common requirement is the idea of current situation reporting. For the time period of concern, situation reporting via sophisticated display devices is probable. Equally probable will be the ability of a computer to respond to commands entered by voice; more than the entry console with its typewriter keyboard, card reader, or tape reader. At the point in the system where the computer and Commander come into direct intercourse, voice communication response is desirable. The cognitive aid which the machine system can supply in this design can make the Commander more effective because with the aid of the system he can operate from a much broader data base. His analysis of the situation can be supplemented by the testing of various options to determine the best possible choice both for the immediate Military success and the longer range economic and political goals. Warfare in the era under question will be a narrowing down of more general economic and political forces and bringing to bear a focused combination of these pressures on points which offer likely targets for this kind of probing. The agressor forces have shown their willingness to use Military force to suppress revolutionary movements which threaten the regime in power. Tactics of the 1975-1985 era must provide a quick and effective countermove if desired. Fast exploitation of weakness will very likely require that the decision of how and when to exploit be left to the Area Commander who is on the ground and knows the situation. By broadening his data base via the computer, he can <u>know</u> a lot more and in the knowing possibly save lives but

at worst he can see to it that the objective for which the lives are expended is taken and retained. The Military Commander of this era must have a firm grasp of the Military situation as well as the political and economic situation facing him and must be able to make quick responses when the situation requires it. This response could range from calling two more tanks, to the other extreme of asking the President or the Director of the United Nations to intervene. It may require that he be briefed on some local anomaly of religion, or custom which can make his acceptance in the area peaceful, or otherwise.

The necessity for Command and Control functions is not of course limited to situation reporting requirements. Much of a Commander's communication capability will be run, controlled and modified by the computational set he possesses in this time period. Message routing and much of the clerical work found at the communication center such as Diarization, Header affixation, etc. will be accomplished by a subunit of the MILDATA computer system. The security of his communications may involve Encryption and Decryption under Computer Control. On line performance of such fundamental functions as these are already under study and experiment by many groups within the Armed forces and the U. S. Government. All of the aspects of the Command and Control system must be allocated to the Control aspect of the system. The Command aspect will be shaped by the echelon position of the user and by the situation confronting the user. It is certain that a simple Stimulus-Response arrangement will not serve in this time period. The Command aspect of the system will still be heavily influenced by the Command responsibilities of the user and any design for such a system must provide for both expansion and contraction of Command responsibility. It is because of this requirement, among others, that the system expandibility pattern of system design has been followed in this report. The broad catalogue of available modules called out earlier in this report is specifically designed to fit the Commander's needs at all levels of Command and Control. The Programming Software to use the modules must be tailored to operate on any and all combination of modules with an optimum efficiency, measured in thru-put time. The net effect of using the system must equate to an enhancement of the cognition of the using Commander and a contraction of his response time to a decision requirement in real time.

APPENDIX B

APPENDIX B.

Systems Analysis

B.1 Introduction

General system design approaches have been generated
for the MILDATA study as the result of several studies of
both large systems and families of equipment existant in
the field today. Also a concerted effort has been made to
determine the significance of reliability considerations on
initial system and equipment design. The results of these
studies have directed much of the effort of evolving the
MILDATA Systems Design presented in this report.

B.2 Discussion of Current Large Systems

B.2.1 Introduction

As the MILDATA Study progressed it became evident that
existing large computer systems could be studied with profit,
with the view of evaluating their effectiveness, methods of
system control and structure of system language. As represen-
tative large systems the Control Data Corporation 6600 and
the IBM 7950 systems were chosen. These systems are both
very large and powerful, with important differences in system
philosophy.

B.2.2 The IBM 7950 System

The IBM 7950 System (see Figure B-1) consists basic-
ally of a high performance general purpose computer (STRETCH)
which has been modified to include a powerful non-arithmetic
processor and is provided with a high performance tape system
and memories to maintain a balanced high speed of processing.

Programming control of the system resides in the
general purpose computer (7030) which executes conventional
instructions and directs all input/output activities, includ-
ing the high performance tape system (7955). The non- arith-
metic processor adds a set of powerful and flexible MACRO
INSTRUCTIONS to the general purpose list. These macro's are
useful in performing a wide variety of data editing, compar-
ison, searching, classification, and rearranging data activities.

B-1

The particular combination of macro's used to perform one of these functions is represented in the machine by, the configurations of the "Set Up" fields, a group of control fields directing and controlling these specific macro instructions. The "Set Up" fields are loaded into the Set Up registers by the basic program before processing begins. While a macro instruction is being executed the system is in "Set Up" mode. On the other hand, during execution of conventional instructions it is in arithmetic mode.

The major classes of operations carried out in the arithmetic mode are:

1. Integer arithmetic operation

2. Floating point arithmetic operations

3. Radix conversion operations

4. Connective operations

5. Index arithmetic operations

6. Branching operations

7. Transmission operation

8. I/O operation

9. Miscellaneous operation

The "Branch Enabled to Set Up" mode specifies that the next instruction is in "Set Up" mode or is a MACRO INSTRUCTION. It enables the interrupt mechanism and guarantees that all interrupt conditions generated during prior arithmetic mode operations are recognized and acted upon, leaving the interrupt mechanism cleared for "Set Up" mode responses.

The set up mode is entered by the above mentioned Branch and Enter instruction. Each MACRO is organized by the programmer.

B-2

MEDIUM SPEED MEMORIES
16,384 WORDS EACH

HIGH SPEED MEMORIES
1024 WORDS EACH

INPUT-OUTPUT
UNITS

MEMORY
BUS CONTROL

EXCHANGE

ARITHMETIC SECTION
(STRETCH)

SET-UP MODE SECTION
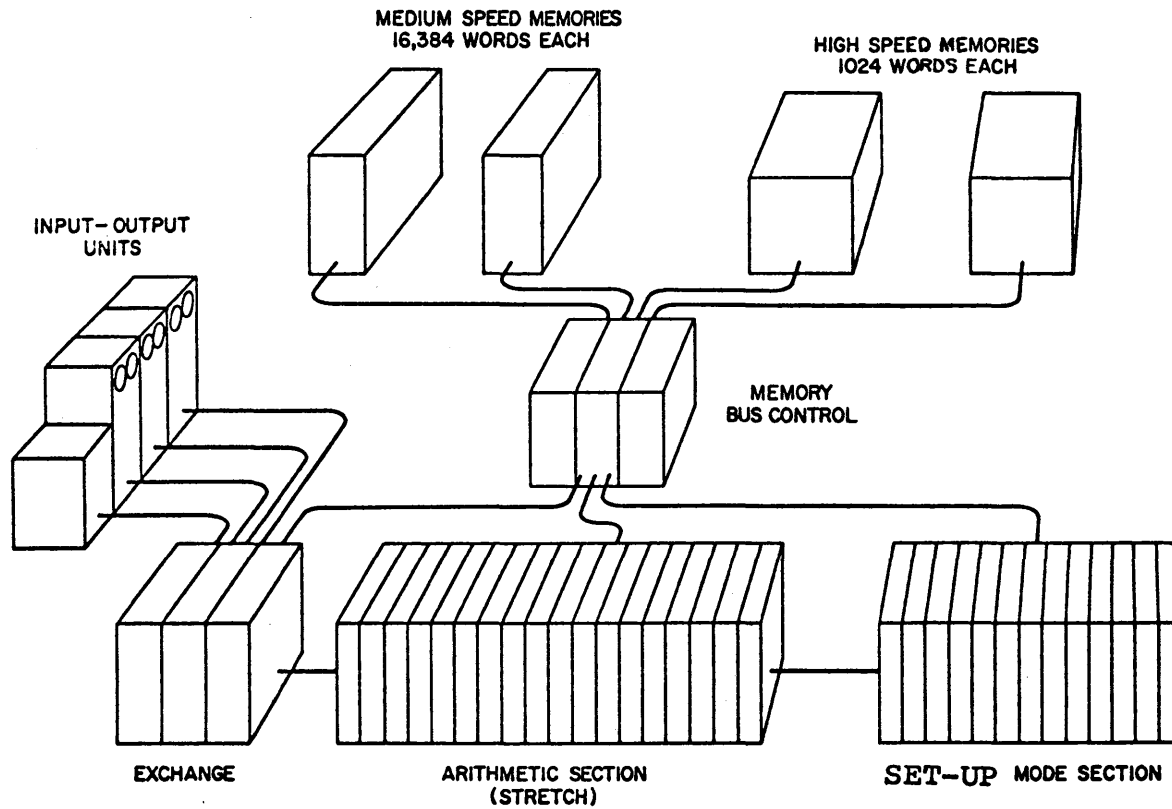
Fig. B-1   IBM-7950 Harvest System

The byte (8 bits) is the fundamental unit of information in the "Set Up" mode. Bytes are selected from memory by two special indexing units forming two sequences which can be combined by a class of logical or variable radix addition operations, or can be formed into "Look-up" addresses which are sent to memory to select ' and return a table entry. In either case, the result sequence can be sent back to memory by means of a third special indexing mechanism, or accumulated for statistical purposes. The path which the Byte follows is selected by the programmer, through the various logic junctions reflected by the bit configuration in the "Set Up" registers. The basic process can in turn be altered momentarily or permanently by a set of MICRO INSTRUCTIONS called Adjustments.

The special indexing mechanisms are unique in that the indexing is expressed directly in terms of the pattern of data selection. For the purpose of these indexing units the whole memory is treated as one long string of bits on which the pattern is imposed with no special notice taken of actual word boundaries. See Figure B-2.

To sum up, the basic non-arithmetic process, the data pathways, the set of MICRO INSTRUCTIONS and the indexing patterns are the major tools with which the programmer designs his MACRO INSTRUCTION, while these specification constitute the "Set Up".

B.2.3   Typical Application for a Non Arithmetic Mode
          Processor.

The non-arithmetic data processing, MACRO INSTRUCTION section of the 7950 offers an advanced capability primarily because of the powerful operation it can bring to bear on a train of data in one pass.

This segment processed data in the form of 8 bit Bytes in a continuous flow pattern and is designed to be applied in basic logical operations, counting, tablelook-ups, etc. The simple process of hunting for some particular piece of information in a mass of irrelevance can consume considerable machine time; moreover, if the mass of irrelevance is large enough, the pursuit of the gem of information may not be possible at all. The problem of too much data and too little information is found more and more often.
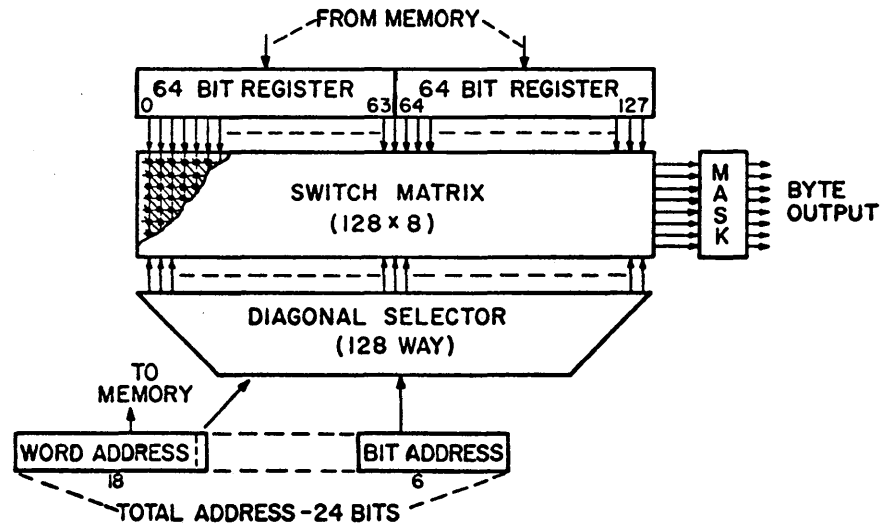
Fig. B-2 Byte Train Processor

To handle such a data searching problem conveniently, division of the data into subsets and generation of Statistical Characterization for each Subset is convenient. By studying the weightings of these statistics it is possible to determine cause and effect relationships by correlating events which look as though they may be related. In addition in most data processing systems a continuous effort is made to reduce the amount of data, to make significant data more accessible and to provide effective statistical characterization. Sorting of data is the first step in accomplishing this. Expensive storage must be used at maximum efficiency so sorting must be done with respect to the most important characteristic of the data. As new information enters it must be merged into the old.

Therefore, **FILE MAINTENANCE** becomes a very important function of the Data Processing system. A processor, with the facility for creating sources and sinks to generate and operate on long data sequences could be more effective than a conventional computer operating on a field at a time. For our purpose we can describe it as essentially processing sets of operand data from two sources to form a set of result data going to one data sink. The speed of this process should be determined entirely by the data flow rate into or out of memory, the data fetched and stored according to preset, but possibly very complex indexing patterns. In addition, while passing data through the processor we may wish to examine any or all of the three sets of data being processed to look for a particular piece of information; we may want to count the occurrance of various events in each set, relationships between subsets as well as the occurrence of the subsets themselves, react to these occurrances by altering the process and perhaps perform a sequence of table lookups with a means for terminating when desirable. Having initiated such a complicated process a means is needed to break out of this process and retain the state of the processing at the point of termination.

Further, an accumulation of statistics, may require that some action be taken to radically alter the indexing sequence or perhaps interrupt in response to an event occuring in the real time environment. To provide for maximum efficiency in such an application the 7950 system contains two units called a Table Address Generator (TAA) and a Table Extract Unit (TEU). These devices respond to circumstances within the Data Processor and send off addresses very rapidly, usually to a high speed

function. Loading of the system with jobs of various sizes
tend to make the short jobs wait for computation of the long
jobs, so many of the drawbacks of the batching techniques are
present here.

A symbolic language has been generated for the 6600
which is based on the multiple register design, of the instruc-
tion stack. By grouping the memory address register and the
operand registers the language can range effectively over the
central processor instruction and somewhat less efficiently
between the peripheral processors. In any event an object
program can be produced which effectively utilizes the register
combinations. The orientation of the software is for scientific
applications operating in FORTRAN. The principle of concurrency
of operation is predicated on finite, incremental calculations,
with a minimum of interdependency of results. In summary 10
independent calculations functions plus the central calculation
in the processor are possible. The management of the system
to accomplish this is as yet undemonstrated.

It may be said that the synchronous design of 7950 approx-
mately offsets the synchronous operation of 6600. System control,
hence ease of response to a functioning processor language are
simpler in 7950, but this is a result of the hardware design.
In the 6600, system controls are necessarily more complicated
because of the semi-autonomous nature of its system components.

For data processing purposes the 7950 enjoys the advan-
tages of "on the fly" indexing and processing, while it shows
only the "STRETCH" capacity in computational power. The 6600
clearly exceeds 7950 in arithmetic speed and capacity because
it is specifically designed for concurrent arithmetic operations.
The old dichotomy of scientific vs. data processing applications
still exists even in these very large systems hence the design
of these very large and powerful computational systems falls
short of the multi-application demands of the future systems.

B.2.4   Trends in Systems Control Philosophy

The description of 7950 and 6600 are intended to illus-
trate two trends in system control philosophy. In the 7950 a
great effort was made to produce hardware to execute some data
processing techniques normally found exclusively in the program-
ming part of the system. In the 6600 an effort is implemented
to eliminate these same bothersome control functions by providing

an array of processors, each capable of autonomous functioning
within limits and yet each executing a part of an integrated
program routine or sub-routine. By the multiple peripheral
processor FILE MAINTENANCE can be carried out in parallel with
arithmetic processing and/or communication link responses. In
this system the high speed indexing and file context notation
are not as easy to handle as in 7950, but true simultaneity of
processing is attained, while in 7950 the arithmetic processor
can only operate when the data processor is not operating and
large additions to the on-line tape file usually excludes any
parallel processing for that time interval.

We have in these two systems i.e. 7950 and 6600 two large
systems with great power, lowered cost per unit of computation,
extensive system programming and very little new development
in the area of adaptive organizational power, or ease of job
loading. We see two systems philosophies each trying to achieve
concurrency of problem solving, simultaneity of solution genera-
tion, and consequent reduction in thru-put time. Each accomp-
lishes these objectives, but both are difficult to program, and
have added to overall job processing time because of the program-
ming difficulties.

In the vital area of file maintenance the 7950 is
probably superior because of the large on line storage capacity
of the 7955 (Tractor) tape system. But the bookkeeping and
control effort required to keep records of the contents of this
file, affect to some degree the effectiveness of the system.
The set-up unit, with its adjustment reactions can provide high
speed modification to the indexing sequence, or initiate remedial
sub-routines, without interrupting the data processing. It can
also provide a limited pattern recognition, and language trans-
lation power that is hardware based and hence not programmed.

The 7950 is essentially an asynchronous machine system
with each major sub-unit operating at its own speed and synchron-
ous operations is not necessary. The memory bus design   is a
time quantized slot arrangement, with each time slot 300 usec
wide. All address generation (indexing) in the remainder of the
system can be at a rate which is some multiple of 300 nanosec.
In addition, a priority scheme is superimposed on the bus control

which says that the slowest system segment has first priority with second priority to next slowest system segment, etc. When a buss slot is gained and an address decoded and accepted by memory, a slot 7 x 300 nanosec. later is reserved for memory read out if it is an address within main memory range, or 4 buss slots later if the address falls within the H.S. memory range. This simply means that should a new address try to gain access to memory during the readout cycle slot time it would have to wait one additional slot time.

B.2.5 Conclusions

1. System design must not induce clutter in control.

2. The proportion of time devoted to getting ready to do work must be small in comparison to time expended in doing work.

3. Modularity of system design is better on a logical basis than a hardware basis.

4. Language development must be an aid in using the system not a constraint on the usefulness of the system.

5. The user must be accommodated as if he were very limited in his training to utilize such equipment (Idiot proof and fail safe).

6. A situation reporting method current to the last millisecond, and comprehensive enough to embrace a whole theatre of operations is intrinsic to the success of any large system.

B.3 Family Properties

Data processing systems or subsystems of the MILDATA family should have certain properties to junction effectively as a family.

The first family relationship is the sharing of common types of peripheral equipment. The critical design question is the planning of the interface or interface types of maximum value to the maximum number of different kinds of equipments.

It can be expected that compatibility with widely-available
military and commercial equipments of current and future
design will be as important as compatibility with equipments
designed especially for MILDATA. This will be important not
only for availability of emergency replacement of peripherals
-- which continue to increase in relative importance in cost,
bulk, and reliability -- but also for economy in non tactical
applications.

Such an interface design must minimize the variety of
modules required in forming the second type of family relation-
ship, the connection of similar-purpose elements by a variety
of interconnecting modules.

The second relationship requires that machines share a
similar internal data format to the point that there is a common
identical set of internal codes for data significance so that
there is effective bit by bit correspondence between data codes
stored internally. The recent promulgation of ASCII code gives
hope that this situation will be on its way to a final resolu-
tion by 1970 as far as input and output codes are concerned;
MILDATA can almost surely obtain speed, bulk, and cost advantages
if it can successfully avoid unnecessary proliferation of internal
codes for essentially identical purposes.

Note that the presence internally of a set of codes
possessing this property does not necessarily imply that some
processing modules do not have other data formats available to
them. For example, it is possible that a MILDATA family member
may require a set of data formats to be used for rapid calcula-
tions, as well as a standard MILDATA character-oriented format
probably required of all MILDATA processors to communicate with
external devices; there will also probably be optimal character-
oriented data formats required for compatibility with non-MILDATA
compatible devices still in extensive use in the 1970's, part-
icularly in communications areas. However, as fast arithmetic
or logical calculations are not of major importance in all
MILDATA applications, this fast-use internal format would not
be required in all systems, and the other applications would
perforce be planned to have data format compatibility as a
minimum.

B-10

The third relationship is a sharing of an internal instruction format with a common set of internal codes for instructions and addressing significance so that there is effective bit by bit correspondence between program instruction codes stored internally.

Thus, the members of the resulting family will possess the power of interpreting a common set of externally introduced instructions and data to produce identical results of identical data. In other words common compilers and other automatic programs will be available throughout the family.

B.4 Fundamental System Design Consideration For MILDATA Modules

B.4.1 Reliability Considerations

The continuing advance in component and interconnection reliability suggest that by the early 1970's it will be possible to field a simplex processor module of small size with a probability of failure of the order of 10^{-4} to 10^{-5}/hour. Such operational reliabilities have attractive military implications in terms of reduction of training and necessary availability of maintenance personnel, and in widening the range of tasks which may be entrusted to the processor system.

It must not be forgotten that the high speeds, relative infallibility within its limitations, and flexbility in principle, of electronic processing must be obtained under field conditions in the presence of such performance-degrading elements as extreme shock, natural or deliberate communication interference; fatigued, untrained or dazed personnel; constant requirements for motion; and other conditions inimical to optimum systems operation.

For these reasons, it seems appropriate to ask what techniques may be available in the MILDATA time frame for increasing substantially the reliability of entire systems which may include elements too unreliable in themselves to furnish the necessary assurance of operation since some of the necessary modules of the system--such as communications links, electromechanical input or output equipment, display equipment, etc. do not yet meet the most reasonable requirements for simple reliability in the intended application. Many of these considerations are, of course, substantially independent of the basic order of data structure or operating mode of the electronic processing modules, but lead to important suggestions for modification of these structures.

B.4.2 Reliability Requirements

B.4.2.1 Introduction

One of the most important considerations in providing highly reliable systems is that of ensuring continued effective operation even though part of the system be inoperable. It is customarily permissible that the capabilities of the system be somewhat reduced under these circumstances, but operation of the system must not cease completely; this is referred to as "graceful degradation" of system performance.

Another important consideration, especially important in military systems, is that system operation must not be permanently degraded or distorted by a temporary failure in performance of the system or any component thereof. This is sometimes referred to as "insensitivity to transient faults". The more complex the logic of a system is, the more difficult it is to provide this facility.

Both of the above considerations become important in the time interval where the probability of hardware failure becomes unacceptable for the required task. In practice this unacceptability level is usually conditioned by the assumed probability of failure of some other essential element of the system. While great strides continue to be made in the reliability of the electronic components and systems, it is probable that increasing use of processors in critical applications, the military value of operating processors in environments untenable to humans, and the high military value generally in reducing the need for maintenance personnel will result in a continuing demand for systems whose reliability must be higher than that attainable by a simplex system organization must be higher components available to the then-current state of the art. Systems substantially more reliable than the current reliability of their individual components seem to permit are here referred to as 'extremely high reliability' systems.

B.4.3. The Decentralized Control Concept

System organization can be made which permit automatic recovery from any single and many multiple faults, the recovery time being measured in small fractions of a second, with little or no risk that any real-time processing will have to be repeated. One such type of organization referred to is a "decentralized control" system.

The requirements for successful decentralized control may be reduced to the requirements that each processor independently be capable of

(1) Recognizing that any other processor-program combination is operating, or is not.

(2) If not operating, taking appropriate action; if operating

(3) Recognizing whether the operation is correct or not. If not correct, it is often convenient also to

(4) Recognize whether the incorrect operation is due to failure in the equipment (processor including essential connections to it) or to failure in the program.

(5) In the event of any incorrect action, it is necessary to take appropriate action.

Recognition: To recognize the existence of trouble each processor-program combination may transmit to every other processor-program at least the following information:

1. A frequently-updated "I am active" indication. One convenient such signal is the time from the master clock, passed by the program to a predetermined register of the common store. Whenever the time becomes out of date by more than the predetermined interval at which updating is expected, it is clear that the process is not correct, or that the equipment has failed. Similarly, if the time is found to be updated at more frequent intervals that the minimum permissible in the program, the processor-program combination has failed to execute part of its minimum permissible loop.

2. Any built-in hardware failure indicators available in the processor. Often internal parity errors, arithmetic errors, sequencing errors, etc., are indicated in the equipment's logic in such a manner that they can be turned on only if equipment has failed. It is relatively easy to arrange for such indicators to be monitored by all other processors and/or the common-access storage. The setting of any of the indicators then serves as an 'I am down' indication to all the other processors of the system.

3. Checking information in the program. This will be determined individually for each system and program of the system. These should in practice be checks, requiring relatively little processor time, for which complete information can be sent from one processor to another in little time. Two or more processors may conveniently "hash total" -- or "integerize" -- the same data independently. Each problem and system lend themselves individually to providing such identities.

Whenever failure of such an identity is found, both equipments -- that responsible for producing the data and that responsible for performing the check -- become suspect. In order to decide which equipment is to be bypassed, it is necessary that the various processors of the system perform the check independently and compare their results; this can easily be done with the use of the common store. A processor which finds that its own check agrees with that obtained by one processor and disagrees with the other will proceed to react as though the processor whose results do not check were not to be trusted and begin the appropriate corrective action from his point of view, as described below. A processor finding neither in error, or both in error, would be programmed to take other, but more cautious action. (In practice, this case should be expected to be less common, unless analysis of the system has shown that there is a third common element whose failure could be expected to produce this result.) The assumption is that but one new independently-generated failure is to be expected in a unit testing time, since the unit time is short and the system is physically designed to require multiple failures to provide indication of multiple faults.

Corrective action: One method provides a different set of programs for each combination of operative hardware and for the transition caused by the failure of each subsystem. Whenever these indicate a particular equipment at fault, each processor first tests the consensus of the trouble indications. If it finds the expected result--all processors currently active except the one at fault agree on the nature of the fault--it then alters its own program, by reading the appropriate new program from the common store, so that it will take over the role preassigned to it in the new-existing configuration of operative equipments. These changes are initiated by each processor independently--each initiation program itself, of

course, containing its own unique checks as to the satisfactory
progress of the initiation process. When all operating pro-
cessors have completed their individual independent reactions
to the new situation, the system will be in a state in which
the failed equipment or program is out of the operating sys-
tem, the work of the system is being carried on in the pre-
assigned manner appropriate for the available equipment, and
the human operator has been informed of the new state of affairs.

        The trend toward increased internal transfer speed
capability with decreased physical size of processors of a given
cost and logical complexity and trend toward increased speed
for a given cost, favors greater ease in implementing a decentral-
ized-control system in the future. The argument is that the
frequency with which tests need to be completed in order to
determine whether a given subsystem shall continue operation may
be expected to be fixed as a function of the nature of the task
to be accomplished, and in many cases to be determined by a
human 'inconvenience time' measured in a few seconds at most.
Since the human being's reaction times are not expected substan-
tially to change, and continued study of any given application
may be expected to unearth more efficient and effective tests to
be used the proportion of processor time needed for the control-
test portions of a decentralized-control system would seem to
decrease as faster processors become available. (The alterna-
tive, as usual, is that the proportion remains constant while
systems more demanding in reaction time are implemented.)
 Either of these alternatives suggests that it may often be
desirable for MILDATA processors to be interconnected and pro-
grammed as decentralized controls, and that the desired data for
such a connection are important to their system-organization
plan. Hence it is a great relief that the previous arguments
have suggested that decentralized control can be implemented
with little or no increase in hardware cost; the primary require-
ment is adequate attention to system properties of modules also
highly suitable for simplex operation. Finally, although the
system plan of Figure 4-11 was originally studied with the expec-
tation that the various processors would be within a relatively
small area, the inherent nature of a decentralized-control or
any other redundant-organization system does not require this.
Indeed, in some military applications in the MILDATA time frame,
it may be desirable that the alternate or checking processor
for each function be situated at a distance of many miles from
all processors and other equipment for which it is a monitor.
This implies, however, that broad-band communications links will
be required between the various systems, and, if current

communications plans do not include such links as a part of a subscriber system of radio-linked communications, consideration for such a system should be examined. If any of the systems are to be operated while in moving vehicles - as is believed likely - it is extremely important that proper attention be given to this requirement in preparing military communications requirements for the 1970 time period. The alternative is likely to be either that extremely high reliability systems can be operated only when all components are stationary, or that the modules to produce such systems must be physically shrunk still farther to permit their necessary operation in the vehicles.

The implementation of such a system requires appropriate provisions both in the hardware and in the programs of the system. The minimum hardware provisions are the following:

1. A substantial store for standby program configurations, which can be communicated with by all processors of the system, with a latency which is a very small fraction of the desired time of recovery from a system fault.

2. Means of continually passing information from any processor to any other processor regarding the status and progress of the processor itself and its program. The common access store of (1) is one such means.

3. Means of access to each non-processor (peripheral) device by at least two, and preferably three or more, independent paths to different processors, with provision for selecting the active path of instructions executed in any one of the processors connectable. Again, the common-access store of (1) may fulfill this function, providing the peripheral device has access to the store itself by alternate independent physical paths.

4. The common-access store referred to in (1) must of course itself be at least duplicated, and all duplications of equipment in the entire system must take into account the possibility of power, clocking, or mechanical failure, as well as of failure of the logical and/or storage media themselves.

Requirements in the programs include means for each processor's program continuously to transmit data to each of the other processors regarding the functioning of the processor and of the program, and means for each processors' program to recognize incorrect operation or non-operation of either the processor

or the program. There must also be means in the program for
each processor, acting independently, to take corrective action
when any one processor-program combination has been found
to have failed.

The programming requirements may also be implemented
about the common-access store, available to all processors of
the system. The storage should be physically divided so that
each processor has a part available which can be written into
only by its own program, and under no circumstances by the pro-
gram of any other processor. There may conveniently be pro-
vision for any processor's temporarily reserving for its own
writing use other portions of the common store, and there may
also be use for a common store segment which is unrestrictedly
available for writing by any processor. All processors have the
capability of reading any portion of the common store, irres-
pective of writing privileges. It is also convenient that the
common store include a system clock, advanced by unity at any
convenient interval (commonly in the range between fractions of
milliseconds and a few seconds depending on detailed system
requirements).

B.4.4 Implications

The following implications, based upon the foregoing
study, for MILDATA systems designs can be drawn:

1. (a) In operation, the decentralized control system
requires a substantial amount of input and output data transfer,
with fast service of each peripheral data transfer requested by
each processor. The processors thus require fairly high peak
input and output data rates. This is desirable for the MILDATA
family on the basis of data processing systems trends alone.

(b) The percentage of each processor's time taken by
the decentralized/control peripheral transfers should be small-
say under 20%. This permits peripheral-limited programs to pro-
ceed even under decentralized control.

(c) If the processor time required by decentralized-
controlled input and output data transfer times is more than a
very small percentage of total processor time, it is essential
that processor subsystems be available which are capable of
simultaneous processing and peripheral transfer. This property

is highly desirable for MILDATA units for other reasons --
namely, the probable frequent occurrence of problems which are
input-output limited. There is no present indication that per-
ipheral equipment breakthroughs will permit the (essentially
data processing) applications expected in 1970 from being peri-
pheral-device-limited in execution speed.

(d) If the decentralized-control peripheral transfer
times, including access times, are a very small percentage of
total processor time, processor modules can be used which cannot
compute and read or write simultaneously. Such modules are less
costly than those capable of simultaneous peripheral transfer
and computation by addition of another module. Again, such very
small modules deserve considerations in MILDATA for reason of
bulk, alone.

2. A real-time interrupt facility in each processor
module will undoubtedly be a substantial aid in implementing a
decentralized-control processor-program combination. This is
certainly expected to be required by many other MILDATA real-
time applications.

3. Based on current study, no system feature is _required_
for decentralized control which is not now present in some form
in the system design of one or more currently-available processors.
However, it is far too early to decide what details are most _de-_
sirable for implementing such a high-reliability system, expec-
ially if non-classical processing elements are to be included.

4. Trends appear to favor easy implementation of decentral-
ized control in the future.

5. The implementation of redundant, graceful degraded
decentralized-control systems, when desired, should be possible
in the MILDATA system with the same modules designed for applica-
tions requiring minimum-hardware non-redundant system organiza-
tion, with little or no change in the properties of the modules
themselves, provided they are designed with a moderate amount
of foresight.

6. If 1970 MILDATA field applications require decentral-ized-control system operation with subsystems at remote locations, wide-band communications will be required between subsystems.

7. It is not practically possible to provide very great mean-time to system failure by redundant use of relatively small numbers of subsystem modules unless the redundantly connected modules themselves have a mean-time to failure approaching or exceeding the desired system mean-time-to-failure. Hence, it is very important that MILDATA systems not included individual modules whose mean-time-to-failure does not equal or approach the desired interval between human attention in the most demand-ing application for that module, unless the module may easily be broken into sub-modules for interconnection when high relia-bility requirements must be met. This implies that the physical size of MILDATA modules will be influenced not only by the con-venient and practical physical size and cost of a replaceable unit and by the reliability of the physical unit, but also by the military use which is most demanding in terms of absence of maintenance personnel.

APPENDIX C

APPENDIX C

Software

C.1 Introduction

The general description of software system development
for MILDATA is found at various points in this report. A
general commentory on programming procedures and File
Organization is found in 4.3.3.6. This commentary traces
the organization of Data Files from primitive EAM oriented
systems to modern data file organizations and attempts to
justify why such developments took place.

What follows below is intended to bring the focus of
this report more explicity on the MILDATA system and its
development. The first section concerns itself with
Command and Control Programming for such a system and
with the characteristics which make if different from
scientific and business systems. Such items as develop-
ment and maintenance of the system are discussed, including
the support which presents an initial description of adaptive
use of the software in the field and examines management
problems and cost factors predictable for the time era
involved.

C.2 Characteristics of Command and Control Software

Computer programs for command and control systems tend
to be large, for example -- 200,000 machine language instructions
is very common for a set of programs and at least one set of
computer programs is being prepared consisting of about 3/4
of a million machine language instructions. Also the number
of pieces of data handled by the programming may be an order
of magnitude greater than the size of the programs.

Because of this size problem, program segmentation is
a characteristic of these systems. When the programs are
too large to completely store in core at one time, proper
segmentation is essential in the final system. The coor-
dination of activities within storage and the moving of
the programs and data base in and out of core storage is
very critical. Debugging of many pieces or segments at
one time is aided by the use of the proper segmentation
technique.

C-1

The necessity of handling input/output for many programs simultaneously with the necessary computations requires special techniques in writing co-existing programs. These techniques have been referred to as parallel processing; the fork and join technique; and simultaneous computing. Regardless of the terminology, the criteria must be that more than one program can be operating at one time, in the system, including input/output.

Queuing of processing loads must be planned when possible, even though processing peak loads may or may not be expected. The controlling programs must be able to handle unscheduled loads without substantially degrading the system, or lengthening the processing queue.

How often when one hears the term "system reliability", does one think of software? And yet, poorly planned software in this respect can negate any well-oriented reliable hardware system. Bugs in the system program <u>must</u> be found prior to software integration into the system. Validation of programs is seldom done on a planned basis. Intermediate validations will help build confidence in each step of developing the system. In particular, in a real-time system, the independent debugging or validation of the various necessary routines insures confidence at the packaging level. Here the system programmer is often uneasy due to the lack of knowledge of the extent of the testing of the segments of the package which he is trying to tie together. Some criteria must be established to determine whether the program is properly performing. In MILDATA a careful assembly of packages can relieve the Supervisory Programmer of much anxiety.

Equipment problems in a system such as MILDATA are many. Unavailability of the specific computer complex may delay program debugging. Compiling of the object program can be accomplished on a computer not even of the same class as the computer on which it will be executed. Here also, unreliable equipment may waste the programmer's time in verifying the correctness of a program or delay his testing, if it's often down for maintenance. A smooth transition from the existing system to the MILDATA system can be made by checking out MILDATA program on existing machine.

C-2

Another characteristic is the continuing change in
equipment design. These frequently require a change in
operational program design and may require reprogramming
of large segments. When equipment subsystems are developed
concurrently with the software, it is usually difficult to
get down-to-earth specifications of the developing system.
Non-current documentation frequently causes software problems
because the program design may result in incompatibility
with the hardware design. For example, accurate program
timing diagrams help a great deal here.

Unreliable programs supplied with the hardware for
purposes of diagnostic work are also frequently causes of
trouble. Substitute or engineering test computers supplied
for interim system check-out cause problems in the input/
output area. Results may no be either complete or realistic
and necessitate further testing when the operational hard-
ware is delivered. A well planned development program
should make certain that test machines accurately reflect
MILDATA specifications.

Command and control systems software changes continually.
The changes must be kept up-to-date, documentation must be
current, and the response to changes and requirements must
be as fast as possible.

Personnel changes are also a characteristic, which
must be planned for.

Although the frequency of occurance of the real-time
demand in MILDATA may be low in comparison to the information-
retrieval type request, where file-searching time is expected,
much emphasis must be placed upon the small fraction of work
in this area. Accommodation of real-time demands must be
a prime objective of System Interrupt design and system
control response.

The subsystems constituting the command and control
systems are so closely interrelated that it is difficult
to separate one from the other. The subsystems constituting
the Command and Control systems are so closely interrelated
that it is difficult to separate one from the other. The
figure below is intended to show the dependence of the com-
puter programs on the other subsystems and components within
the Command and Control system. Because of this inter-
dependence linkage of subsystems, programs, routines, sub-
routines, etc., is possible. It is also possible to link
in hardware diagnostics for use in systems components located

in remote areas.

Command And Control Problem Universe
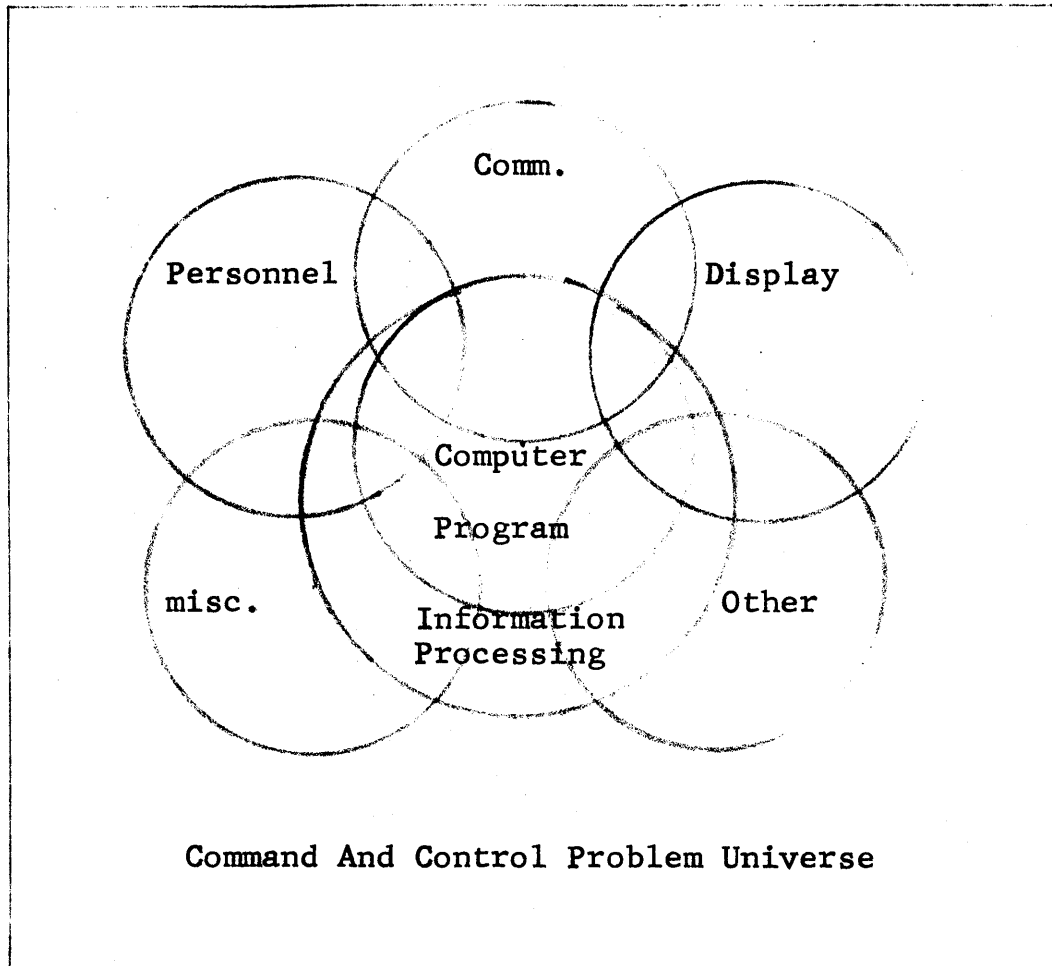
C.3 Development and Maintenace

The development of a Command and Control software
system is outlined below. This is an attempt to elicit
the major areas of work in the production of such a system
and then to tie these areas to particular aspects of the
system design which are calculated to make the work areas
achievable.

Requirements Analysis – This the first and most important step in the development phase of system design. Here a joining of the Army's System requirements, its Data Processing needs, the savvy and know-how of its experienced system analysts and system programmers can contribute substantially to the setting of reasonable targets for the MILDATA System. Even more important, deficiencies in the old system will not be repeated in the new system. Continuity of experience and confidence in the final design can result. The necessity for the program analysts to participate from the very beginning not only with help determine what cannot be done but also what can. All too frequently, assumptions are made in both directions by non-programming personnel, which would be invalid to a programmer. Often a task which looks impossible can readily be accomplished in software.

Operational Design – By this is meant designing the system and specifying how it must be tested. In designing the programming languages, the main objective is to make the task of programming as easily and quickly accomplished as possible. The programmers should be experienced and it should not be necessary to make allowances for inexperienced, "man-off-the-street" type of personnel. It has been shown that a small team of experienced people, armed with a concise language, can produce working systems in substantially less elapsed time and cost than a large staff with mixed experience in a FORTRAN, COBOL type language.

The system languages are those required to communicate with the system designers. Each area listed has its own terminology and will be better served if the terminology can be employed.

The other major language area is the input/output language. Obviously, in a Command and Control system, the need for on-line communication with the computer programs is essential. The means of communication must be simple, direct, and free of redundacies and format restrictions, i.e. errors must be allowed in spelling, etc.

Program Design – Under this category of development and maintenance the following areas of investigation are significant. These include the tasks of estimating and allocating computer storage required for both program and the data base, designing the executive and control system at each level of MILDATA, breaking out the required tasks into subprograms, planning data communication between programs, planning program testing and finally, documentation

C-5

criteria must be established.

Data base design and collection, i.e. designing the formats, structure and coding of all data to be used in the computing system.

Production - the actual writing of the programs to be tested.

Program Test - Testing the coded programs with simulated environment first, and then the actual (or as close as possible) conditions.

Operational testing - Installing the software in an operational system and testing it. This normally will be a different hardware setup than that used during Program Test. In this case the existing hardware system should serve.

Operation and Maintenance - Maintaining the software in an operational environment and providing retrofitting of the programs to correspond to changes in system requirements or system hardware.

The above activities will and should overlap in time. As listed, they are directed toward the operational system to be installed in the field. However, equal emphasis must be placed on the development of utility, library and other support software.

The tools which are to be used in developing the MILDATA system include both software and hardware components. The software to be used in the field should include a language with which the soldier can communicate with the computing system at the same time and in the same way that he normally communicates with his commander.

The computer oriented languages then break down into two areas:

    (a)   Off-line languages - those not used in the operating system but used to develop it.

    (b)   On-line languages - used in the operating system on a real-time basis.

As is evident, the higher the level of quality that the first area achieves, the easier it will be to implement the second. The "offline" languages necessary to implement MILDATA include programming languages (compiler, assembler, utility, library and debugging) and system languages, defined as a language which, although procedure-oriented intrinsically, can be understood by the particular subsystem user (Fire Control, Logistics, etc.). As in programming and maintaining any large scale computer system, a major area of difficulty is the communication link between the problem originators and the implementing team. The following approaches have developed to minimize the difficulties.

One approach is to use a system-oriented language (S Ø L) which both the originators and implementors can understand. This approach is good (a) if there is only one problem area, and (b) if the language is sufficiently well defined to make its implementation easy.

Where there are many problem areas, another approach is to use a general-purpose procedure-oriented language (PØ L) which may place the burden of learning the language upon the problem originators or else place the implementing team in the position of having to interpret the procedure-oriented language to the problem originators.

Where many problem areas exist, each with its unique terminology, it has been suggested that a system oriented language (SØL) be specified for each area. This eases the burden on the users, but increases many fold the load on a common programming team. Not only does the programmer have to know the SØL for each problem area, but a compiler must be provided to recognize each SØL. As is obvious, this increases greatly the elapsed time between system specification and system check out.

Compilers have been written which (theoretically) are capable of handling many languages by using different tables (internal) for each language. In practice, it is doubtful that any of these would actually work, as it is extremely difficult to control a programming team to the extent necessary to implement this type of compiler.

Even if it were possible to implement such a compiler successfully, the problem mentioned earlier still exists of the programming team needing to be familiar with each language (SOL).
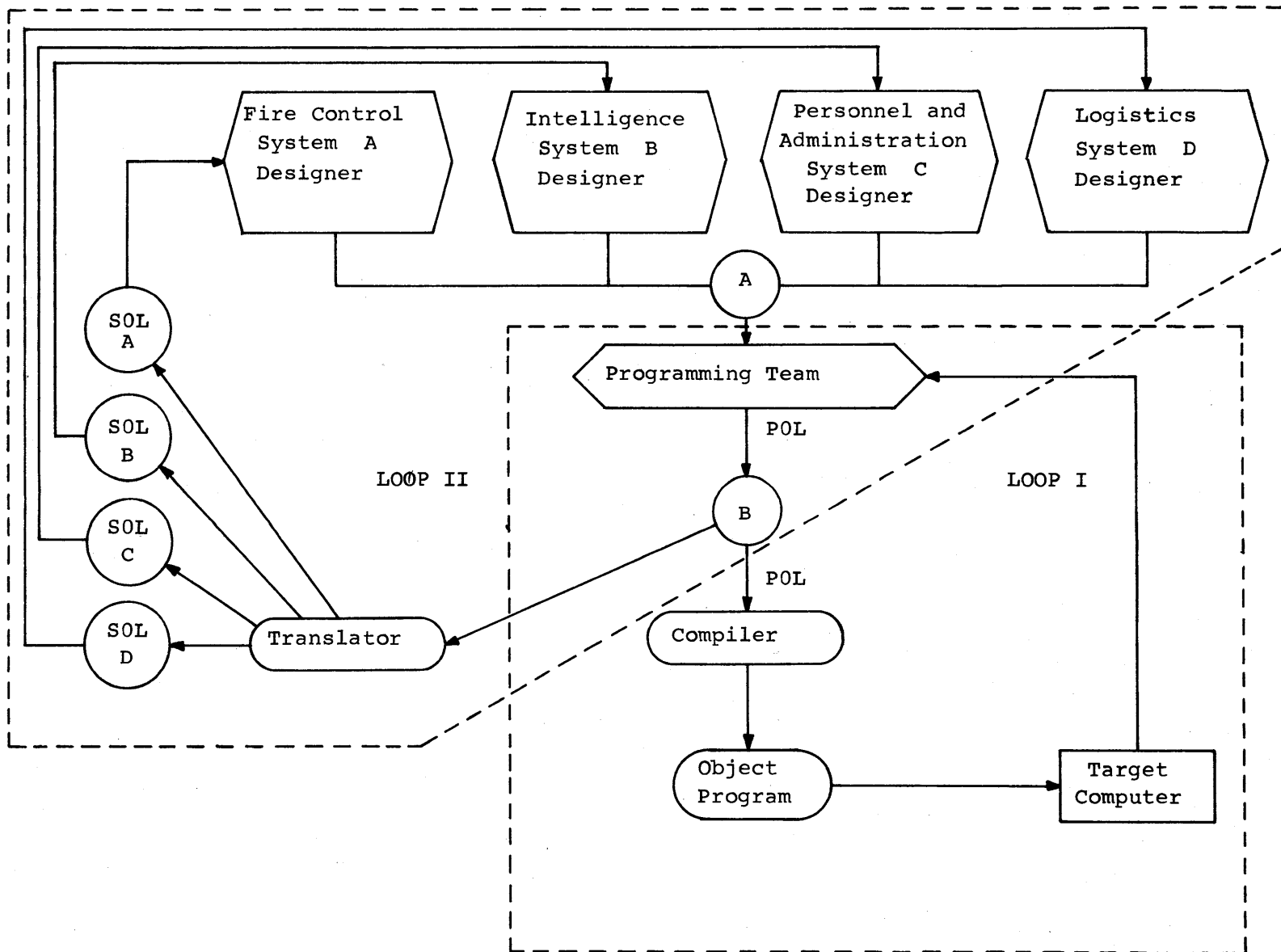
Figure C-1. Flow Chart

An alternate approach to this problem is outlined in
Figure C-1. When examining this approach, it must be
remembered that in a large-scale real-time system such as
MILDATA, it is mandatory that the programming be done by
experienced systems programmers, not users. Starting with
the premise of an experienced programming team using a
language designed to facilitate their work, what should
be done to expedite the system changed which are bound
to occur? Obviously, communication links must be
established in both directions between the programming
team and the specification team.

First, the specification team needs to know what has
been done in a language which is readily interpretable by
them.

Second, they need to be able to specify changes to
the programming team in relation to the existing programs.

Once these changes have been specified, they must be
easily incorporated into the existing programs and check
out.

Starting in the diagram at point A and following the
solid line with the systems specifications defined for each
area, (fire control, logistics, etc.) the programming
team writes the programs using the procedure-oriented
language, and submits them to the PØL compiler, (which
is not necessarily located in the object computer).
The compiler produces an object program which can be
tested in the target computer. The results of this test
are then analyzed by the programming team, changes made
(in the PØL) and the cycle continues.

At any point in time during this debugging cycle,
one of the systems designers may desire to determine if
the project is proceeding according to his design. At
that point any existing PØL program may be routed through
the translator (following the dotted lines now), which
will turn out a document in his particular system-oriented
language. This document will correspond line for line
with the PØL version, thus making it possible to alter
systems concepts and designs in the system language,
which then can readily be put into effect by the pro-
gramming team.

It should be apparent that there will be many more
cycles through Loop I than through Loop II. This is
inherent in any large system. Therefore, the need to

minimize the effort and elapsed time is great. This is the real justification for keeping the actual system programs in a high-level PØL, which has been proven to speed up checkout and changes.

The translator shown in Figure C-1 would be a single computer program written in the PØL, which would be capable of translating the PØL to anyone of the SØL's. No SØL would ever in any sense act as an input language to a computer or compiler. Instead, it would serve as a documentation of what was being done in the PØL in terminology easily interpretable by the user. The user then, with this document, can communicate with the programming team for purposes of revision, maintenance, clarification, etc.

Emphasis should be placed on the fact that we are talking about system specification, programming and maintenance, not system operation. Specifically, what advantages could be obtained from such a system?

1. The programmer-to-programmer communications are simplified with every one using a common non-machine-oriented language.

2. Programmer training is simplified.

3. Documentation of the current program is automatic and available in both user and programmer language.

4. The user-programmer communications are simplified without the necessity of learning several sets of terminology.

5. System checkout is speeded up because of the PØL.

6. Costs are substantially reduced.

C.4 Terminology

A list of definitions of the terms used in this commentary is included here.

Definition of Terms

Functional Specifications

Specify what must be done and the performance re-
quirements which must be met. Specified by the user.
Non-programming oriented, machine independent.

Programming Specifications

Defines the tasks in programmable terms. Translates
the Functional Specs into a technical, program-oriented
description.

System Flow Chart

An overall system description

User

Produces Functional Specifications, assists in preparing
programming specs.

System Analysts

Individuals able to understand the Functional Specs
and responsible for producing program specs. Also
responsible for maintaining contact with the User.

Programming Team

The team is responsible for producing the system from
the program specs. Varies in size throughout the
implementation, expected to be at a minimum after
checkout is finished and maintenance only is required.
Includes System Analysts.

System-Oriented Language (SØL)

The language (understandable to the User) used to
communicate between the User and the System Analysts.

Procedure-Oriented Language (PØL)

The machine-independent/language used by programmers
to implement the program specs.

Machine Language (ML)

The machine-dependent language.

Compiler

The computer programs which translate the PØL programs
to various ML programs.

Translator

The computer program which translates the current PØL
programs to SØL printed outputs.

C.5 Programming Support

These areas designated as Programming Support are:

1. Support Programs
2. Documentation
3. Coordination

The support programs for MILDATA would be:

Utility routines - Print, tape, tape dumps, trace,
load, etc.

Librarian routines - Routines to set up and maintain
library and the programs usually found in a system
library.

Functional routines - Sine, cosine, square root, etc.,
commonly found in a system.

Computer facility - A test bed for developing soft-
ware and checkout. Peripheral equipment should be
as similar as possible to final system hardware.

Documentation - This is all the necessary program
descriptors, flow charts, operator directions,
optional modes of running, etc., needed to keep
an up-to-date record of the program and its current
form within the computer. Provisions for updating
documents must be easy to use and frequently used.
As the program design changes the documentation
must change. Close control of these changes is
mandatory for successful system design.

Coordination – Under coordination is included the collection of information concerning operating conventions and procedures to facilitate understanding with the system user. The data collection, data base, etc., is also a function of coordination. The programmers who are using the system and the computer must have a group to whom they can bring their problems with equipment and program support software.

C.6 Adaptive Programming

As the MILDATA concept is a modular one, it must be recognized that the programs provided for such a system will also be modular in construction. In a time frame where the smallest computer may be carried on a soldier's back, or even in his helmet, the computer programs for this module will of necessity be semi-permanent, perhaps stored in a read-only memory. Input/output to this smallest computer could well be only by light-pen or some similar device.

However, at the higher levels of command, the computers will also be of a higher level, and will be more capable of performing more complex functions. One area that has been of concern in this study, has been the unexpected problem; the completely unanticipated requirement of a computer system to do that task for which it has no planned (programmed) action. For example, a commander in the logistics area is suddenly informed that a fire-control computer system is out of action. Every effort must be made to keep the fire-control function in action. In order to do so, the commander must be able to communicate to the computer system his problem, and to have every possible assistance in solving it. We have chosen to term the solution to this, "Adaptive Programming".

In order to explain the approach more readily, the normal compiler/loader action will be examined. If a programmer writes a statement in a compiler language which is syntactically correct, the result is a string of machine language instructions which will perform the specified action. If he uses the syntax incorrectly, the compiler will tell him so. In the same vein, after a program is compiled correctly, it must be loaded into the target computer for a program test. If the loader discovers that a routine has been called for that it does not have available to it (i.e., is not in its tables) it will issue a message indicating this, naming the routines which are unavailable. The programmer then either modifies his approach

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to the problem, eliminating the need for the missing routines, or in some way adding them to the system.

With the help of hardware which does not seem to be out of reach in the MILDATA time frame, the concept can be reasonably achieved. The hardware in question, in part would be an associative memory (content-addressable) or a similar device, which would allow fast searches through ordered trees. The trees would contain, as succinctly as possible, the available programs, subprograms, segments, and algorithms which made up the various systems already available. The characteristics of each, as well as the necessary inputs and outputs, would be retrievable.

With a convenient method of communicating with the executive system, the commander could then query the computer in much the same manner that a programmer would, receiving answers which would tell him whether this approach was achievable.

It should be emphasized that any forseeable situation should be already taken care of in the advance system programming. However, there will always be circumstances which cannot be forseen, and it is these situations for which adaptive programming is designed.

In non-field use, the same approach might be used to speed up programming and checkout of new equipment components. Bootstrapping a complete new system would be feasible providing all the components were there.

C.7 Management Problems and Cost Factors

In order to estimate the cost of developing large programming systems, it is necessary to look into three areas. These are the technical content, the environment and the resources. The technical content or requirements of the system are mostly beyond management control. However, managers can influence the impact on cost of the environment and resources. Some of the factors under the technical content area which will tend to increase the cost of program development are:

1. The number of command centers in the system and particularly the ones that will use automatic data processing techniques.

2. The number of different computers for which programs are prepared. In MILDATA this is held to a minimum.

3. The separation and remoteness of centers containing computers. (Separation from another and from the location of the developers.)

4. The number of input/output interfaces. (The variety of unique types of data input.)

5. The frequency of inputs and outputs to the command and control system.

6. The number of different program systems of the three general types, operation, utility and support.

7. The speed of the response necessary, the speed of the recovery for automatic data processing from malfunction or failure.

8. The number of equipment components that are being developed concurrently with program.

9. The number and diversity of the information processing functions.

10. The complexity and interdependence of the data processing functions.

11. The number of changes which are made.

12. The degree of innovation in the system, its components, and the data processing function.

The cost factors which can be controlled to some extent by management are environment and resources. To reduce program development cost, utilizing proper environment, a management plan should be developed that recognizes the relation of program development to system development, delineates the responsibility and authority among the component developers, specifies communication and decision making procedures and includes a mechanism for changing the plan. The management plan maintenance and monitoring will also effect the costs. The use of reasonable schedules are important. As previously noted, the development of the program by a small group of people rather than many hundreds affects both cost and schedules. Requirements must be stabilized during the production activities. Firm policies must be formulated and applied for documentation and quality control. The heavy emphasis in command and control systems on coordination and participation of many organizations and large numbers of people is very evident under the environment.

What about resources? The better the resources available to the software development, the cheaper it will be. The experience level of the personnel is extremely important, as is the availability of the computer; the proficiency of the computer operators; the experience level of the military personnel involved with coordination activities; the existence of various programs such as compilers, assemblers, utility programs, library routines, library handlers; the computer capability storage capacity, operating time and the power of its order code. The speed of response time for the computer facility in itself is a major factor in reducing costs.

APPENDIX D

APPENDIX D

D.1. Background and Implications of Changing Army Tactical
Doctrine

No single type of warfare can be postulated for future con-
flicts. In the future, hostilities may range from minimal assist-
ance to foreign forces, to unlimited nuclear war. In order of
increasing scope, the spectrum of military conflict may be delin-
eated as follows:

A. Military assistance programs

B. Committed U.S. force, non-nuclear combat

C. Full scale non-nuclear war

D. Limited nuclear war (tactical nuclear
weapons only)

E. Unlimited nuclear war (strategic ICBM
weapons)

Battlefield combat is of major significance in all but the
unlimited nuclear war. Limited nuclear war as defined, represents
the most severe and demanding tactical Army requirement. Forces
will be widely dispersed to reduce susceptibility to nuclear
weapons. Mobility is required to quickly concentrate forces for
an offensive strike and to disperse them immediately afterwards
in order to protect them from a nuclear counter-attack. As an
example, it has been estimated that the size of the battle area
will be substantially more than double that which was required for
engagement of an equal number of troops in World War II.

Even though U.S. Army forces must be prepared to engage in
nuclear combat, other types of warfare are still very much a part
of the picture. "Military Assistance Programs" is typical of the
present Viet Nam operations and frequently represents the guerilla
type combat. Extreme flexibility and mobility is paramount. Equip-
ment must be small and lightweight and be back carried or helicopter
transportable.

D-1

"Committed U.S. Forces, non-nuclear combat" and "Full scale non-nuclear war" are similar. Committed U.S. Forces is typical of the Korean War where large numbers of troops were engaged in support of a United Nations effort of limited scope. Full scale non-nuclear war is typical of the World War II fighting. In both these types the emphasis on mobility need not be as great as A and D and the battlefield sizes will be much smaller than D. This type of combat is what the current army communications equipment was designed for. Many advances now are possible even here, however.

These factors have their impact upon communication requirements. First, they increase the demands for communications equipment. There must be better radio communications at both higher and lower echelons to retain the necessary control of a highly mobile force in a rapidly changing combat situation. Every unit must have a means of quick communications extending over a broad area from headquarters to every outpost.

Second, they cause an increase in traffic beyond that experienced in past warfare. This greater volume demands greater capacity and at the same time complicates the problems of security. Increased traffic in an expanded combat area invites more possibilities for compromise in security, interception of messages and sabotage.

Third, they make mobility, flexibility, maintainability and survivability extremely important for all electronics gear. These factors are accompanied by a greatly compressed time factor. The tactical environment of modern warfare dictates the need for an all-weather, around-the-clock, mobile capability under all conditions. Darkness and inclement weather no longer provide the protection they once did. These factors drastically reduce the time margin for decision making.

Although communication advancements have been and are being made, tactical requirements for more communication have increased at a tremendous rate and, in many cases, have far exceeded the capability to provide it. The explosion in the use of electronics in warfare has placed a premium on the frequency spectrum as well as on the time that is available for use. The increasing reliance being placed on radio communications in tactical operations makes it necessary to find new techniques to:

A. exploit the frequency spectrum more fully

B. increase effective communication ranges, and

C. increase the mobility of communications equipment.

D.2. Communications Techniques

D.2.1 Introduction

The demands of Army communications for the period of 1965 through 1980 will, for the most part, be filled by equipments and techniques presently developed, under development or at least under study. For this reason, the discussion of this advanced period will consider the anticipated requirements and foreseen developments. Judging from the progress in the last ten years, in the field of tactical Army communications, it seems reasonable that technology, beyond the present thinking may be available for use late in the 1965 to 1980 period.

Generally speaking, future Army communications must show improvements in several areas. Perhaps the most critical of these is the more efficient use of the frequency spectrum. The wide dispersion of the modern battlefield, modern warfare concepts, new weapons systems and the automation of many functions, has placed and will continue to place, heavier demands on the communications system. Unfortunately, however, the usable frequency spectrum does not increase along with these demands. Unless the utilization of this spectrum is made considerably more efficient, saturation will be reached, and it will become the limiting factor in the entire communications system.

In addition to the more efficient use of the frequency spectrum, several other improvements will be necessary. Increased mobility, through a further reduction in size and weight, and new, long life, noiseless power sources are essential for the highly mobile army of the future. These new systems must provide simple and immediate user access, with decreased reaction time and greater routing flexibility. Also, decreased vulnerability to detection, and a simple and efficient method of providing both voice and data security are required.

D-3

Still further areas of desired improvement include battle-field IFF techniques, improved antenna systems, and real-time data links between aerial combat surveillance and ground stations. Also, instantaneous warning nets to warn combat elements against an impending nuclear burst, will be of great importance.

D.2.2 Random Access Discrete Address Systems (RADA)

Random Access Discrete Address System (RADA) now under development is designed to replace conventional radio and wire communications in the division area of operations. The system will provide a private"dial"connection with any other user in the RADA network whether on the move or at a fixed location. It will also provide for teletypewriter, facsimile, slow scan video and data transmission.

RADA is a wide-band, highly versatile communications system, which allows a very large number of subscribers to communicate on a common channel, without any form of traffic coordination.

RADA fulfills the requirements for simple immediate random access, fast reaction time and routing flexibility. It can also be used for both data and voice, simultaneously, and has a degree of inherent privacy in that it requires quite special receiving equipment. It has several additional advantages over conventional systems. It is non-synchronous, and therefore requires no central timing system.

Because of its use of a wide-band channel, no extreme frequency stability is required. Individual equipments are considerably cheaper than equivalent narrow-band equipments. Finally, the RADA has a "graceful degradation" as the system becomes overloaded.

D.2.3 Pulse Code Modulation (PCM)

At division and higher pulse code modulation (PCM) is becoming an important means of communication. This communications technique follows the philosophy of keeping voice the predominant mode of communications but does provide a rather natural secondary data transmission facility.

In PCM, voice is digitized and many channels are multi-plexed for transmission over either radio or cable. The rates at which the binary digits resulting from a single channel of digitized voice flow are of the order of 48 KC average. Such channels could be used in conjunction with special interface equipment to provide a reasonable data transmission capability wherever PCM service is provided.

2.4 Single Sideband and Frequency Modulation

Development, in the past several years, of SSB trans-mission techniques, has made considerable gains toward a more efficient use of the frequency spectrum. The SSB transmission of a signal can be confined to one-half of the bandwidth of a normal AM transmission of the same signal. Coupled with this bandwidth saving, however, is an increase in equipment complex-ity. Also, SSB makes no gains toward the problems of reaction time, immediate access or security. The single side-band technique of radio communications has now been successfully adapted to tactical requirements in the AN/GRC-106, a vehicle mounted set that will provide a voice and CW communications over a range of about 50 miles. In an advanced stage of devel-opment is the shelter mounted AN/GRC-108 which will have a range of about 100 miles.

Frequency modulation (FM), which has found wide use in the present field Army, is generally simpler than SSB equip-ment, but does not display the bandwidth nor range advantages. The other considerations for FM are about the same as for SSB. AN/VRC-12 and AN/PRC-25 radio sets presently in full scale pro-duction are members of a replacement family of FM tactical radio sets. Each is a transistorized modularized narrow band FM set designed to provide reliable radio communications between military vehicles, crew served weapons, and troops. The VRC-12 has a power output of 35 watts and a normal operat-ing range of about 20 miles. It replaces the old AN/GRC-3 through -8 series of sets. The PRC-25 is the Army's latest "walkie-talkie' with a power output of 1.5 watts and a normal range of about three to five miles; it replaces the old AN/PRC-8 through -10 series of sets.

The multitude of small, low power, VHF multi-channel FM equipments presently used by the Army will likely be quite ade-quate for the next several years. As the frequency spectrum be-comes more and more saturated, however, the swing to spectrum

saving techniques will tend to obsolete these equipments, and favor SSB and RADA techniques. One solution being approached is the addition of high power amplifiers to directional antennas for the VHF-UHF FM relays to take advantage of the longer range tropo-scatter transmission mode. This will reduce the number of relays required and probably extend the useful life of FM relay in the field.

Considering requirements for fast access and reaction times, SSB transmission may have to be coupled with new system techniques, in order to achieve a maximum of desired characteristics. Present configurations appear to have bandwidth advantages or access time advantages, but not both, which will be a must for the Army of the future.

2.5 Security Considerations

At present, crypo-security is used at the combat division and field army level; however, there are attendant problems that restrict its use. Currently, separate equipments are required for each channel, the equipments are not particularly small or lightweight, and physically secure areas must be maintained for their use.

The demand for secure communications has been expressed in recent years by lower and lower echelons, and in some cases it would be of advantage to have security at forward combat elements. The demand for decreased reaction times requires that all such techniques designed for the future be real-time, or so called "on-line". Security for voice as well as digital transmissions is desired.

Present information indicates that it is planned to secure all rear area digital communications. This implies that advancements in digital communications capability will be paced by not only the growth of transmission facilities but by the growth in crypto-security equipment capability. Studies are currently underway to reduce the burden of security equipment by using bulk multichannel encryption methods and appliques to permit one basic code generator to accommodate more than one channel. Rear area security equipments should be adaptable to both voice and date.

Forward area security represents a somewhat different set of requirements. Here it is possible that shorter-term security techniques may be adequate. For example, less elaborate coding

techniques which would provide 24 to 48 hour security may be acceptable. This reduced capability would, in turn, be traded for smaller and simpler equipments which would make use of security at front lines practical. Also to be considered, is the increased probability of capture and possible compromise of information until the next code change time. In general, the problems of front line security have not been solved. Such solutions will be slow to come about, and are not expected during the 1965 to 1980 period. The primary security advancements to be made in this period are in smaller, lighter weight equipment, and increased use of multichannel capability.

Although security considerations may prove to be a gating item on the development data transmission capability it is noteworthy that, in terms of use of the resulting facility, the security equipment appears to be transparent.

2.6 Error Control Considerations

The control of errors in a digital transmission system is approached in two ways:

1 Error detection

2 Error correction

Error detection must be accomplished through coding techniques such as simple parity and more complex redundant codes. Error correction similarly may be accomplished through the use of redundant codes and also by retransmission of erroneous data. Retransmission is the simplest and most practical method when conditions permit. It requires use of a full duplex data channel and data which is formatted into "blocks" for transmission. Sufficient redundant information is sent with each block to permit comprehensive error checks. If an error is detected, rather than try correction, the transmitter is notified that a particular block, usually the previous one, should be retransmitted. In general, where error rates are typically high, shorter transmission blocks are favored for greater efficiency.

Where full duplex is not practical, such as for remote front line inputs, addition of coding redundancy will be necessary not only to detect transmission errors but to enable error correction. Frequently, it is expected to be a matter of "correct the error" or "reject the data". Where information is at a premium it may be worthwhile to try correction. It is expected that single error correction will be the practical limit. Devices to perform error detection and/or correction will be the responsibility of the digital user rather than the field army communications unit.

3. Conclusions

The preceding discussions lead to the following conclusions:

1. The standard transmission code on all networks -- both store and forward, and circuit both rear area and forward area -- will be ASCll in the time period of interest.

2. Error rates will continue to be a major consideration, particularly at higher transmission rates. Some facilities will be available for intercomputer communication at rates approaching 100,000 bits per second. As these rates are used the error content of messages will increase and so that appropriate safeguards must be inherent in the data transmission schemes employed by all elements of the MILDATA system.

3. Every attempt must be made to maximize the communications facilities available to the MILDATA system. Only limited additional capacity is being added to the communication facility for data transmission purposes. It also follows that efforts should be stimulated to increase the data transmission capacity of the network to maximize the effectiveness of the MILDATA system.

APPENDIX E

APPENDIX E

HARDWARE

E.1   Introduction

E.1.1   General

A minimum hardware investigation commensurate with the
goals and objectives of the MILDATA effort was undertaken during
the early portion of the program effort. This investigation
was considered necessary since a total systems design requires
the integration not only of applications information and systems
design goals, but must also recognize hardware and software
availability and capability. The full results of that study
will be found in Reference E-29, and a summary of that has been
made a part of this appendix as attachments 1, 2, and 3.

Before being able to initiate a hardware oriented
investigation, a realistic examination of the overall MILDATA
Program was required. Thus, a time schedule which presents a
realistic approach to fielding the MILDATA computing system in
1975 was prepared and is shown in Figure E-1. In this figure,
production is indicated as being initiated on or about January 1,
1974. Production should be preceeded by the fabrication and
testing of five or more Service Test Models. Since this testing
could require as much as one year, the Field Service Test Model
must be available approximately 1 January 1973. This, in turn,
necessitates that the Field Service Test Models would have to
be contracted for, and initial construction begun, during the
first quarter of 1970. Further, the Service Test Model build
phase must be preceeded by feasibility studies and an overall
system design phase. Thus, the system design freeze, which
would result from the system design phases, will occur no later
than the last half of 1969.

From the preceeding schedule constraints, a target date
of 1971 was chosen against which to delineate the state-of-the-
art and operational characteristics of circuit components, memory
devices, peripheral devices, software techniques, etc., which
could be incorporated into the MILDATA System. This date has
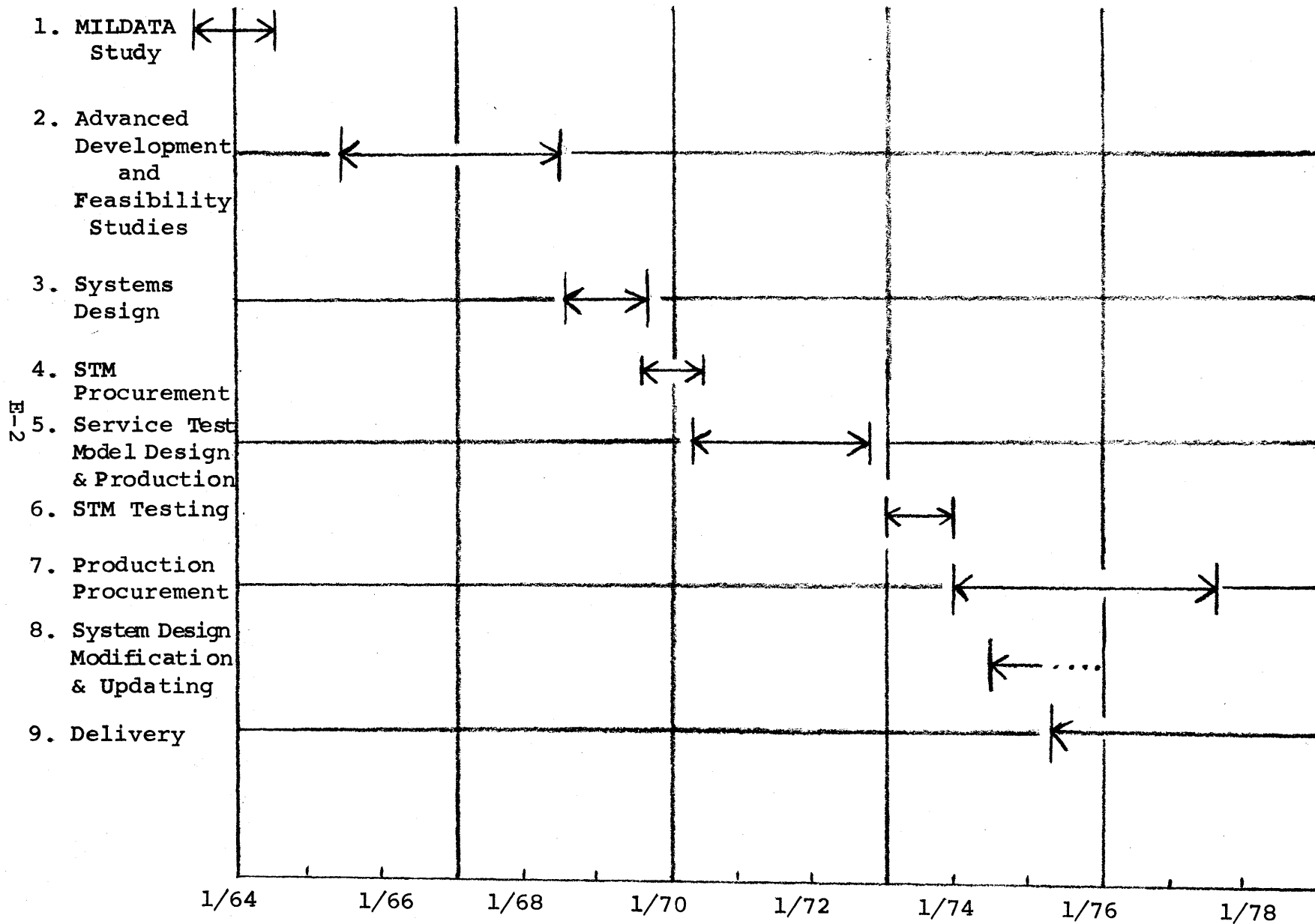been taken into account during all of the MILDATA hardware
examinations.

Figure E-1. MILDATA Time Schedule

E.1.2 Summary of Discussion

The remainder of this appendix is divided into eight sections. Section 2 treats circuitry and packaging, discussion in Section 3, followed by memory and memory techniques. Section 4 and 5 concern the input and output equipments which will be required, or are postulated, based upon overall system concepts. Peripheral storage is discussed in Section 6. Finally, Section 7 presents a brief resume of communications terminals and communications techniques as required. For a fuller discussion concerning communications the reader is directed to Appendix D of this volume. In conclusion, Section 8 presents a brief summary of the salient points presented.

E.2 Circuitry and Packaging

E.2.1 Historic Background

The rapid advances made during the past 20 years in the overall electronics area have been phenomenal, particularly within the computer art. The initial development of an electron tube computing mechanism in the late 1940's established a base-point from which continuous strides have since been made. The introduction of the transistor and the magnetic core during the mid 50's were principle factors towards major advances in the ability of computers to provide more and more computational capability. This increased speed capability was further enhanced by increased sophistication in computing systems design. Today, we are sitting on the edge of a major and multi-facited technological breakthrough. Specifically, the utilization of integrated electronics, only recently in the research laboratory stages, will become wide spread within the next few years. The first commercial step in that direction has already been announced by the International Business Machine Corporation in specifying the utilization of hybrid-integrated circuits in their System/360. Military utilization of integrated circuits is already well underway, with the MIT designed/Raytheon manufactured Apollo computer being a significant example.

As mentioned above, the simultaneous introduction of both transistors and ferrite magnetic cores lead to significant developments which would not have been obtainable if both had not occurred at approximately the same time. Similarly, the introduction of integrated electronics will require a new, parallel development in memories if the full potential of digital integrated circuits is to be realized. However, it must also be noted that overall gains are often accompanied by certain penalties. For example, the introduction of the transistor provided tremendous power savings and volumetric compression. However, an initial speed limitation was imposed. A similar situation may occur with the introduction of integrated electronics in the computer field, due to such inherent considerations as parasitic capacitances, distributed nature of large area components, and transmission line problems.

E.2.2 Discrete Component Technology

Fundamentally, three distinct and different technologies have been examined extensively during the past few years in attempting to design and develop logical elements or structures for use in ultra-high speed (100-1,000 MC) digital computer systems. These three areas or technologies are:

1. Semi-conductor
2. Cryogenic
3. Magnetic

E.2.2.1 Semi-conductor Technology

The semi-conductor approach to the design of logical elements for use in digital computers has become the generally accepted approach. Included under the general classification of semi-conductor logical elements are two sub-headings of prime interest: first, transistor or hybrid transistor structures; and secondly tunnel diode or modified tunnel diode circuitry. Between the two sub-headings, primary emphasis has been placed upon the utilization of the transistor elements in developing ultra-high speed circuits.

The utilization of conventional silicon transistor techniques to achieve ultra-high speed has been reported upon by various groups and individual investigators. One of the most promising efforts has been carried on by researchers at IBM (Reference E-2). This program has produced a small transistorized system which demonstrates a 2.2 ns (nanosecond) delay per level of logic under the worst case conditions. This particular investigation utilized more than 1,800 transistors in 424 individual circuit modules. In another report from IBM (Reference E-3), three distinct types of logic were operated in the range from 100-300 megacycles; the tests employed approximately 500 circuit modules in total.

Tunnel diode circuitry, although not presently utilized to any extent in existing systems, presents an interesting and possibly promising approach to the actual building of a computer whose main clock source may operate at gigacycle (10^9 cycle per second)rates. Much effort has been applied to the design of tunnel diode circuits by various groups toward this end. Of particular note have been the efforts at RCA (References E-4, E-5, and E-6) in the development of "simple" logical structures which operate between 250 and 450 megacycles. However, severe fabrication and interwiring limitations are noted to exist, due to the individual diodes switching at speeds greater than one nanosecond. One attempt to overcome the wiring limitations has been reported (Reference E-5) in which a three dimensional system has been utilized; two dimensions are empolyed for logical interconnection of modules and the third for power distribution. Another drawback to the tunnel diode stems from the fact that it possesses only two terminals presents an inherent design problem. Specifically, isolation between the input and output of a logical entity can only be obtained via complicated circuits which, in turn, require more components.

Several variations on the basic tunnel diode theme have also been reported. One of these variations utilizes a combination of tunnel diodes and "snap action" diodes. These circuits (References E-7 and E-8) permit the design of logical blocks which will operate at approximately 200 megacycles. An interesting aspect of this particular reference development is the utilization of strip lines for the distribution of clocking

signals and the use of open wire (unterminated) connections between logic modules where the lengths of these leads are less than two inches.

In addition to the conventional transistor and the tunnel diode approaches, a number of current research programs are directed toward the utilization of quantum effects or tunneling mechanisms for the development of very high speed switching devices (Reference E-9). These programs include the metal oxide semi-conductor triode (MOS) and the metal interface amplifier (MIA). Theoretical considerations indicate limitations in switching speeds far in excess of 1 nanosecond for devices which can satisfactorily employ the tunneling effect. Currently metal oxide semi-conductive triodes have been reported to be operating at 500 megacycles (Reference E-10). A particularly well written, general introduction to this area appeared in "SCP and SOLID STATE TECHNOLOGY", May 1964 (Reference E-10). These investigations appear to possess the greatest potential for the construction of very high speed digital computer systems in the distant future. Much work remains to be done; however, very close scrutiny of these developments is warranted and recommended.

E.2.2.2   Cryogenics

The second method of implementing ultra high speed logic has been through the utilization of cryogenic techniques. This approach appeared to have great potential until relatively recently (References E-11 and E-12). Individual elements demonstrating switching times of approximately 1 nanosecond or less have been reported in the literature. However, fundamental material problems appear to place an upper limit (Reference E-13) of approximately 100 megacycles upon the useful frequency for at least the relatively near future. Significant problems in the utilization and application of cryogenics have been reported upon concerning the thermal switching of the elements (Reference E-14). However, cryogenics does possess the extremely advantageous quality of permitting the design of very complex circuits. For example, logical functions could be embedded directly into memory structures in such a way as to permit the execution of complex operations either prior to or immediately following the acquisition of data from a particular memory cell. (References E-15 and E-16).

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E.2.2.3   Magnetics

The third approach to the design of very high speed
digital circuits utilizes magnetically switched materials.
Investigations in this area have been carried on concurrently
with efforts in the semi-conductor areas, although at a much
lower level in funding and personnel. During the past ten
years major strides have been made in the design and construc-
tion of ferrite core memories, and in the analysis and design
of thin magnetic film memories. Collateral to these develop-
ments have been investigations both at Stanford Research
Institute and at the Bell Telephone Laboratories (References
E-17, E-18, and E-19) toward the design of digital logic systems
composed exclusively of magnetic elements and interconnecting
wire. These investigations have not yet produced logical
structures which can operate at very high frequencies. However,
these investigations are continuing with at least one investigator
(Reference E-19) reporting sub-microsecond switching. The prob-
ability of developing logical modules based upon magnetic
techniques which would operate above 100 megacycles does not
at this time appear very promising although small inroads may
be made.

E.2.2.4   Summary of Discrete Circuit Investigations

Summarizing the foregoing introductory discussion, the
following points can be made:

1. The probability of the development of a magnetic
   or partial magnetic system, which would operate
   at very high frequencies and be applicable to
   the MILDATA System, appears to be very limited.

2. The utilization of cryogenics is similarly
   limited and possesses the further disadvantage
   of requiring a cryogenic environment. Although
   this difficulty could be overcome, the added
   maintenance, supply and support required for
   field operation mitigates against any further
   extensive examination of cryogenic techniques
   for the MILDATA program at this time.

3. The most promising approaches to the design of
   logical elements for the MILDATA time frame
   appears to be based upon the semi-conductor
   and/or the tunnel diode investigations currently
   underway.

The requirement outlined in the technical specification concerning the MILDATA Study Program specifies the utilization of integrated electronic circuits. This subject will be covered in the next section.

E.2.3   Integrated Electronic Circuitry

The early design of practical transistor switching circuits was based upon an equivalence to proven vacuum tube counterparts. As time progressed, however, transistor circuit design became a skill unto itself.

To some extent the same road is being followed today in the design of integrated electronic circuits. Happily, however, the transistor/integrated circuit technologies are more similar than was the vacuum tube/transistor relationship. Nonetheless, a significant discrepancy does exist between integrated circuit and transistor circuit technologies. Specifically, integrated circuits deposited upon a single chip must take into account the distributed nature of the elements as opposed to the discrete nature of the elements employed in designing transistor circuits. Techniques have recently been announced which attempt to avoid or minimize the distributed characteristics of specific deposited components on a single chip (Reference E-20) by the use of "isolation regions". However, many of the original researchers into integrated circuits, including those at the Westinghouse Corporation, have pointed out that for integrated electronics to come into their own, major steps in the analysis of integrated circuits based upon the inherent characterization of the technique will have to be developed and employed (Reference E-21). Until such analytical techniques emerge, though, the knowledge obtained in designing transistor circuits is a useful guide.

E.2.3.1   Definitions

During the past five years a series of definitions have emerged in order to describe the developments in the solid circuit/integrated electronics field. Of particular note is the report by C.R. Phipps, (Reference E-22) which is of major significance as a reference. The following set of definitions are a valid set for MILDATA consideration:

1. Hybrid - Discrete Component Circuits

   These circuits are composed of passive components
   deposited upon an inactive substrate; the tran-
   sistors and diodes necessary to produce a logical
   entity are soldered or welded onto the substrate.

2. Semi-Monolithic Integrated Circuits

   These circuits utilize several individual semi-
   conductor chips interconnected within a single
   housing to produce a total logical entity.

3. Monolithic Integrated Circuits

   In these circuits all components, both passive and
   active, are produced on a single semi-conductor
   substrate unit. These circuits are most easily
   exemplified by the Texas Instrument Series 51 and
   53 circuits as well as some of the developments
   of the Westinghouse Corporation.

4. Deposited Integrated Circuits

   These circuits are based upon the deposition of
   semi-conductive and non-conductive materials onto
   a passive substrate. Both active and passive
   elements are formed in such a way as to produce a
   total circuit, avoiding the various parasitic
   problems usually associated with monolithic
   circuitry, and it is possible to produce complex
   logical entities in and on a single inactive
   substrate.

   Although the definitions above delineate technologies
which are broadly exclusive of one another, they also represent
a time phasing as far as the implementation of various data
processing equipments and computers are concerned. The micro-
module, developed by RCA for the U.S. Army Signal Corps, is an
example of the first class of hybrid integrated electronics.
The second class of circuits have also been recently utilized,

to a lesser extent, by various computer manufacturers concerned primarily with the military market. The third classification, true monolithic integrated electronic circuits, has been offered currently and is being employed in Aerospace computers as well as in research and development environments. No system nor actual circuits of the Class 4 type are for sale as of this date.

By the time frame of MILDATA interest, in Class 3 true monolithic integrated electronic circuits will be widely employed in preference to both Class 1 and Class 2 circuits. It can be anticipated that Class 4 circuits may very well be reaching the research and development stage by the early 1970's. This assumption is speculative in nature; however, properly directed funding in this area could speed this program to the extent that MILDATA systems designers could take advantage of these circuits.

E.2.3.2 Circuit Selection Considerations

Due to the nature of the conclusions reached above, rigorous evaluations of currently available circuits do not appear to be warranted. However, generalized comparison of the circuits currently available can be made. Such comparisons must consider such circuit qualities as:

1. The noise rejection ratio;

2. The propagation delay for a logical structure;

3. The turn-on and turn-off time for a storage toggle element;

4. The fan-in and the fan-out of the same structure;

5. The practical limitation of logical function realization; and

6. The impedance matching qualities of the same circuits.

Various organizations within Honeywell have performed extensive investigations into circuitry as applied to militarized digital data processing and computing systems. These investigations took into account the various factors listed above. In

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addition, other parameters, such as the power dissipation per element, the average and temperature dependence of delay times, etc., were treated. The summation of all these investigations indicate that transistor-transistor logic (TTL) monolithic circuits provide the most advantageous approach as of this date. Whether the advantage of these circuits will carry over into the early 70's and beyond is open to some question.

Finally, the subjects of interconnection and minimum size of the individual circuit units must be discussed. The inherent problems of distributing very high frequency signals will be significant - if not paramount - in the design of systems using gigacycle range clocking frequencies. Jarvis (Reference E-24) has presented a rather thorough discussion concerning the subject (also see References E-7 and E-8). Fortunately, the reducing in size of the individual logic blocks tends to alleviate the signal transmission problem. Unfortunately, though, it introduces two new ones; namely heat dissipation and radiation susceptability. As the size of the basic element in an integrated electronic circuit becomes smaller, its susceptability to high energy cosmic rays becomes greater. Wallmark (Reference E-23) has calculated that an element's minimal size, taking into account both the heat dissipation and the radiation susceptability, will be limited to approximately 10 microns on an edge to provide a "reasonable" reliability within the individual component (reasonable in Wallmark's sense may not be adequate for MILDATA considerations). Thus, although the shrinking of elements is important, a critical size will be reached below which no practical advantages of further shrinkage can be anticipated.

E.2.3.3 Summary and Conclusions

All indications are that by the late 1960's and early 1970's the art of designing, building and utilizing monolithic integrated electronic circuits will have reached its peak. Further, the introduction of the deposition of both active and passive components upon inactive substrates may reach the state where utilization in military systems will be of advantage. Regardless of which technology is utilized in the design of the MILDATA computer systems both should provide maximum packing density consistant with other MILDATA requirements.

It also appears very likely, as of this date, that component clocking speeds in the range of 100 to 500 megacycles will be available at a reasonable cost. However, it should be emphasized that the size and speed advantages offered by integrated circuits may not be important unless such concomitant developments as memories, peripheral storage systems, and man-machine interfaces progress at the same speeds.

Finally, it is the opinion of this study group that, although the individual circuits may be available, the method of fabricating the individual circuits into a total system and the construction thereof may very well become a greater problem than the actual design, construction, and utilization of individual logical elements. Great stress must be placed upon this particular point.

E.3 Internal Processor Storage and Memory Systems

E.3.1 Introduction

The fundamental investigations into the MILDATA System carried on by the Honeywell MILDATA Study Team indicate that a variety of memories and memory implementations will be required. As is indicated in the recommended system, four distinct types of memory may be utilized in an expanded model of the final systems design. These are:

1. Very high speed executive memory
2. Read only fast memory
3. Main storage
4. Associative memories

Each of the four types of memory specified above will have their own operating characteristics. However, each of these must integrate with each of the others as well as the computational elements of the central processor to provide an integrated, well-balanced operational system. The fact that four distinct classes of memory have been defined is of major significance. Consider that currently most computers contain a single main memory or storage unit, and some contain as many as two. The utilization of multiple memory systems provides a very powerful method of permitting the implementation of a complete family of computers based upon a relatively simple set of building blocks or basic modules.

If any hardware development can be said to be fundamental to the development of the computer art, certainly the memory area ranks as that one development. Although circuitry developments have produced very high-speed circuits, the design of computers are, in general, limited by the availability of high-speed storage systems. These systems, in turn, are limited by the switching speeds of the storage media and the driving/sensing circuits employed in the memory. Most of the systems designed during the past ten to fifteen years have been limited by this constraint. A secondary constraint has been the conformity in the systems design to the principles established by John von Neumann in 1946 (Reference E-25).

Since the publication of the classic report by Burks, Goldstine, and von Neumann published in 1946, hundreds and possibly thousands of articles concerning the computer art and the logical design of computers have been published. In the area of memories and memory systems a proportionately large number of papers have been concerned with memory techniques and memory system designs. Several references of specific interest in this area are given in Reference E-26, E-27, E-28 and E-29.

Reference E-29 presents a set of extrapolations performed during the early stages of the MILDATA investigation which establish the trend lines which will, in all probability, be followed by the industry in the next few years. As was pointed out in that report, the introduction of a radically new technique or a so-called "breakthrough" does not appear to be likely. To substantiate this, recent evidence (References E-30, E-31, and E-32) concerning the most advanced research being performed in this country will be cited below.

Finally, for the sake of completeness, a brief discussion concerning potential future cryogenic memory developments are also discussed.

E.3.2   Status of Current Memory Developments

E.3.2.1   Active Register Storage

Based upon the technical discussions presented in Section E.2 above, it can be assumed that "live" storage flip-flops will be available in the time frame of interest which can

provide switching turn-over speeds in the order of one to several nanoseconds. Further, based upon extrapolations made by various investigators and management representatives in the semi-conductor field, the cost of integrated electronic elements (such as flip-flops) should be, by the time frame of interest, within the range of a few cents per bit stored (Reference E-33). This figure, of course, may vary by an order of magnitude. However, this would not be considered a major or serious problem, since the reliability of integrated electronics has been reported as being in the order of 1/10,000th of 1% per thousand hours (Reference E-34). Other sources indicate that these figures are attainable based upon many millions of hours of actual use of several types of militarized computers designed and developed utilizing currently available integrated electronic circuitry (Reference E-35).

With the cost approaching a few cents per bit and the reliability per circuit attaining 0.0001% per 1,000 hours, and the volumetric size permitting hundreds of bits per cubic inch, extensive use of active registers can and should be contemplated.

E.3.2.2 Magnetic Thin Film Memories

The results of current investigations into the design of thin magnetic film memories permits the assumption that sub-systems based upon this technology will be available in the near future. In addition, reliable estimates concerning the MILDATA time frame can be made. Table E-1 presents a summary of current endeavors in this area.

Examination of the table indicates that currently available developmental thin film memories have capacities of several thousand bits, or more, and can be operated in the 100 to 400 NS range. Of far greater significance is an observation made by Matcovich of UNIVAC, who indicates that the actual switching time of the individual magnetic film storage elements is in the order of 10 nanoseconds. He further shows that the speed of his memory (when reported, it operated at approximately 230 nanoseconds for a complete read-write cycle) was actually limited by the speed of the semi-conductive drivers and the sensing circuits employed. Other investigators have indicated the same limitations exist in their developments.

Table E-1
Current Thin Magnetic Film Memory Developments

Source	Storage Element	Capacity		Memory Cycle Time	First Date Operative	Reference
		Number of Bits	Number of Words			
BTL	Cylindrical "Twistor"	8,192	128	1 μs	?	E-36
NCR	Cylindrical "ROD"	240,000	20,000	800 ns	?	E-37
TI	Continuous Sheet	1,152	64	200 ns	?	E-38
ICT (England)	Continuous Sheet	?	4,096	1 μs	8/62	E-38
UNIVAC	Paired Rectangles	24,576	1,024	100 ns	8/62	E-38
UNIVAC	Circles	4,608	128	670 ns	?	E-38
IBM	Rectangles	18,432	256	100 ns	2/62	E-38
LL MIT	Rectangles	3,328	256	370 ns	2/62	E-38
Burroughs	Rectangles	3,072	128	200 ns	?	E-38
UNIVAC	Bicore Circles	159,744	6,656	3.0 μs	?	E-38
UNIVAC	Rectangles	16,384	512	250 ns	?	E-38

Of equal interest to the MILDATA effort are the prognostications made by some of the same individuals currently performing the advanced memory programs. These are shown in Table E-2.

E.3.2.3 Advanced Ferrite Memories

Although most of the current memory research has been concerned with thin magnetic films, several organizations have continued efforts in ferrites and ferrite devices. These studies can be broadly defined under two headings as:

1. Research in new materials for faster toroidal cores.

2. Research into methods of utilizing bulk ferrite material for storage arrays.

The former approach is best exemplified by the slow, though steady, increase in memory speeds which has occurred during the past few years. This fact can easily be seen by reviewing Table E-3, where a small representative set of machine memory cycle times have been tabulated. Extensive compilations and projections of memory cycle time, memory access time, capacity, etc., have been carried out and were reported in the MILDATA Second Quarterly (Reference E-29).

Investigations into the utilization of bulk ferrite material have been motivated by several factors; among the more significant are:

1. Desire for faster, larger memories, and

2. Desire to be able to mass produce memories at low cost per bit.

Brief descriptions of these efforts in this area are presented in Table E-4.

Table E-2
Prognostications Concerning Future Thin Magnetic Film Memories

Source	Capacity			Memory Cycle Time	Date Available	Comments
	Number of Bits	Number of Words	Bits/Word			
TI	10^6	8,000	128	$\curvearrowleft$ 100 ns	1969-1971	NDR Operation 5,000 Bits/Square Inch Packing Reference E-39
Fabritek	5×10^4	1,024	50	400 ns	1964-1965	Production Costs 1964 = 20-50 ¢/Bit 1965 = 5-10 ¢/Bit For Memory Plane Only
UNIVAC	2×10^5	4,000	50	200 ns	1965(?)	Reference E-38

Table E-3
Processor Main Memories

Company	Machine	First Date of Installation	Memory Cycle Time μs	Memory Capacity in Bits		C/M
				Minimum	Maximum	
				K Bits		
IBM	704	12/55	12	148	984	
RCA	501	11/59	15	96	1,572	
IBM	7090	6/60	2.2	1,152	-	
Honeywell	800	12/60	6.0	288	2,304	
UNIVAC	1107	9/62	4.0	576	2,304	
CDC	3600	4/63	1.5	1,536	12,288	
Honeywell	1800	11/63	2.0	384	3,072	
CDC	3200	5/64	1.25	96	768	
IBM	360/60	9/65	2.0	1,024	4,096	
IBM	360/70	9/65	1.0	2,048	8,192	

Table E-4

Bulk Ferrite Memory Efforts

Company	Name	Capacity	Memory Cycle Time	Comments	Reference
IBM	Molded Ferrite "FLUTE"	2K bits/sq. in. 5K bits/plane	250 ns	Bipolar read/write currents and Bipolar outputs	E-40
RCA	Laminated Ferrite	16,384 bits	100 ns	1. 100KW, 64 B/W 1-3 μs MCT Production estimated @ 1 ¢/bit 2. 10^6 bit memory by 1966 10^7 bit memory by 1968 10^8 bit memory by 1969-1970	E-41
BTL	"Waffle Iron"	8,092 bits	400 ns	Next program for 1KW, 32 B/W with 1 μs MCT	E-42
RCA	"Micro-aperature Ferrite Memory	32 bits	100 ns	1KW, 40 B/W 150 ns MCT next step	E-43
RCA	"Micro-ferrite" Memories	16W, 12 B/W	200 ns	Bipolar outputs yield $\pm$ 50 mv	E-44

E.3.2.4 Cryogenic Memories

Cryogenics presents a very interesting dilemma. On the one hand, cryogenics appears to be capable of providing very large (10^6 words or more) storage systems at moderate speeds as well as being amenable to the designing into the system of complex functions at relatively low cost. On the other hand, cryogenics presents the drawback of requiring a special environment. The latter consideration militates against the construction of the complete MILDATA System utilizing cryogenic technology. However, the use of cryogenics in selected portions may not be unreasonable, depending upon the cost-performance trade-off analyses yet to be performed.

The ability to incorporate complex logic in association with each bit storage position may far out weigh the disadvantages of providing and maintaining a cryogenic environment.

Note, however, that the provision of such a storage unit should, unless the cryogenic subsystem's reliability can be guaranteed, be capable of being simulated by the rest of the system in a reasonable and usable fashion.

In analyzing large cryogenic memories based upon a continuous sheet technique, magnetic core technology was considered the prime competition. Both technologies were projected to the 1970-1971 time period of interest. Figure E-5 presents the memory cycle time versus the capacity (in words) for three types of memory (Reference E-45):

1. Continuous sheet cryogenic memory.
2. Coincident current core memory.
3. Linear select core memory.

Further results of this study, the packing density/memory size and the cost per bit/memory size are shown in Figures E-6 and E-7. The data for all three figures refer to the use of cryogenics as a main store or memory system. In particular, the cost analysis was so oriented.
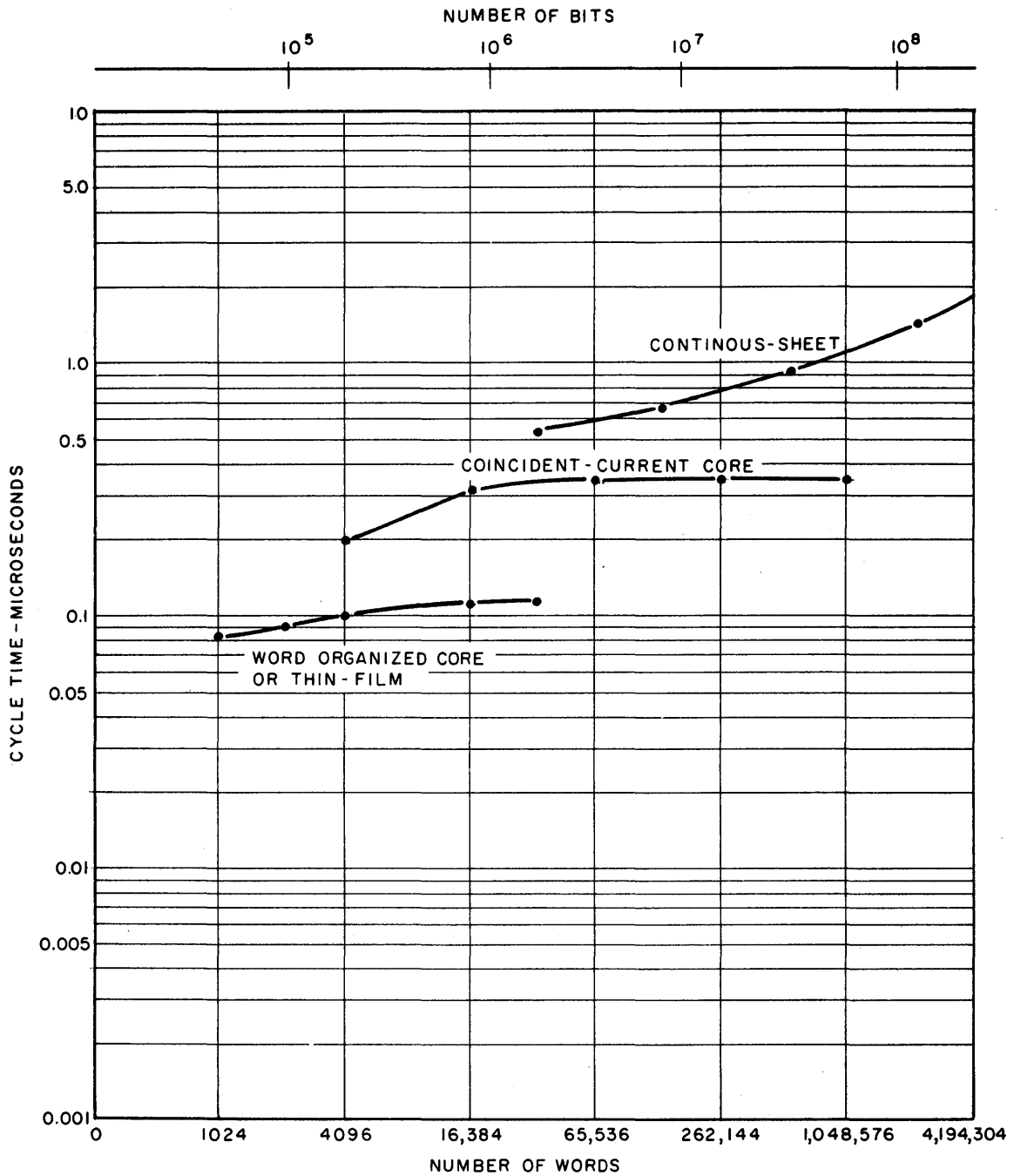
Figure E2. Large Random-Access Memories: Cycle Time
versus Capacity

NUMBER OF WORDS

4,096   16,384   65,536   262,144   1,048,576   4,194,304

10^8

CONTINUOUS SHEET

COINCIDENT-CURRENT MAGNETIC

WORD-ORGANIZED MAGNETIC

PACKING DENSITY - BITS PER CUBIC FOOT

10^7

10^6

10^5

10^4 10^5 10^6 10^7 10^8 10^9

NUMBER OF BITS
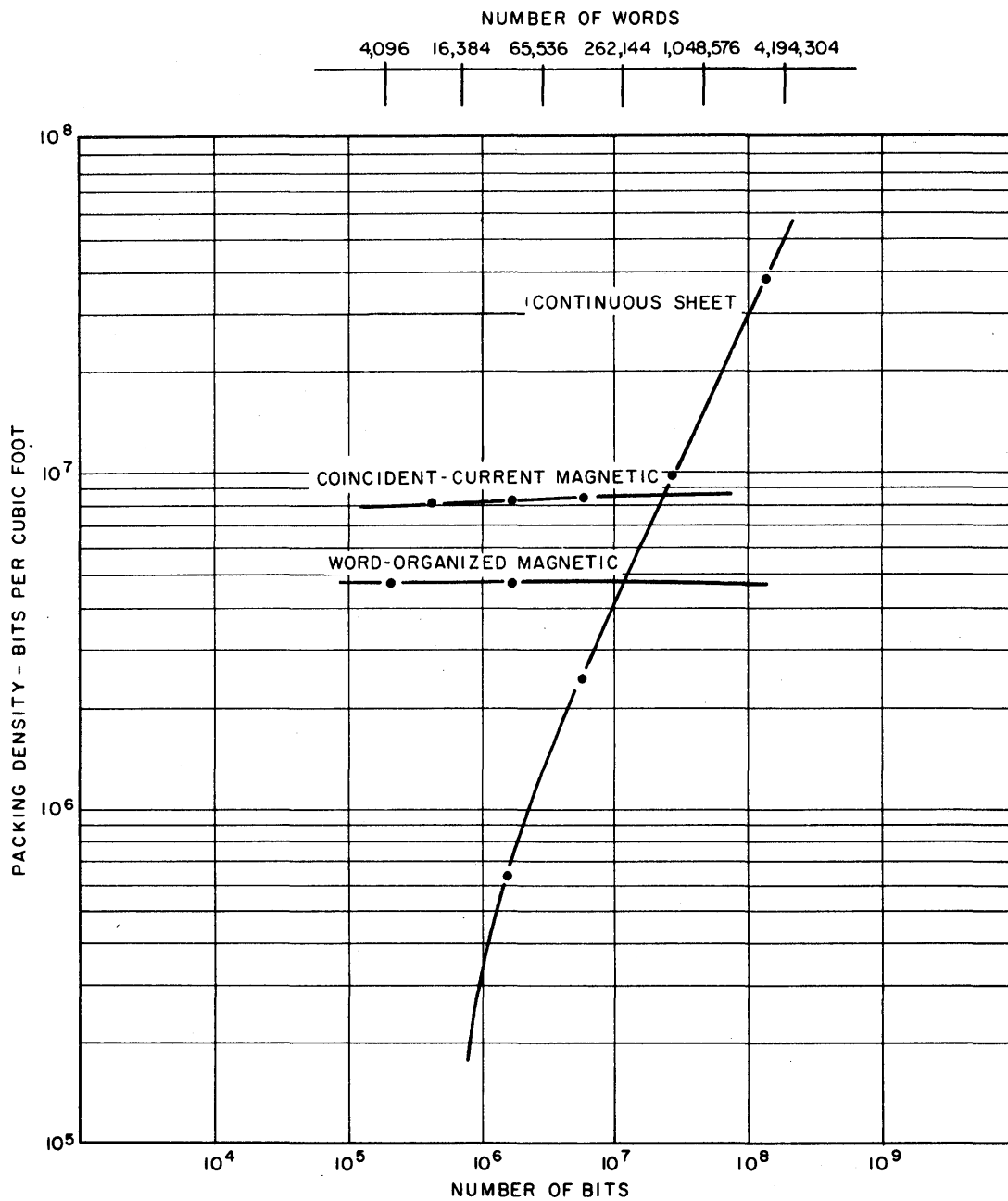
Figure E3.   Large Random-Access Memories: Packing
Density versus Capacity
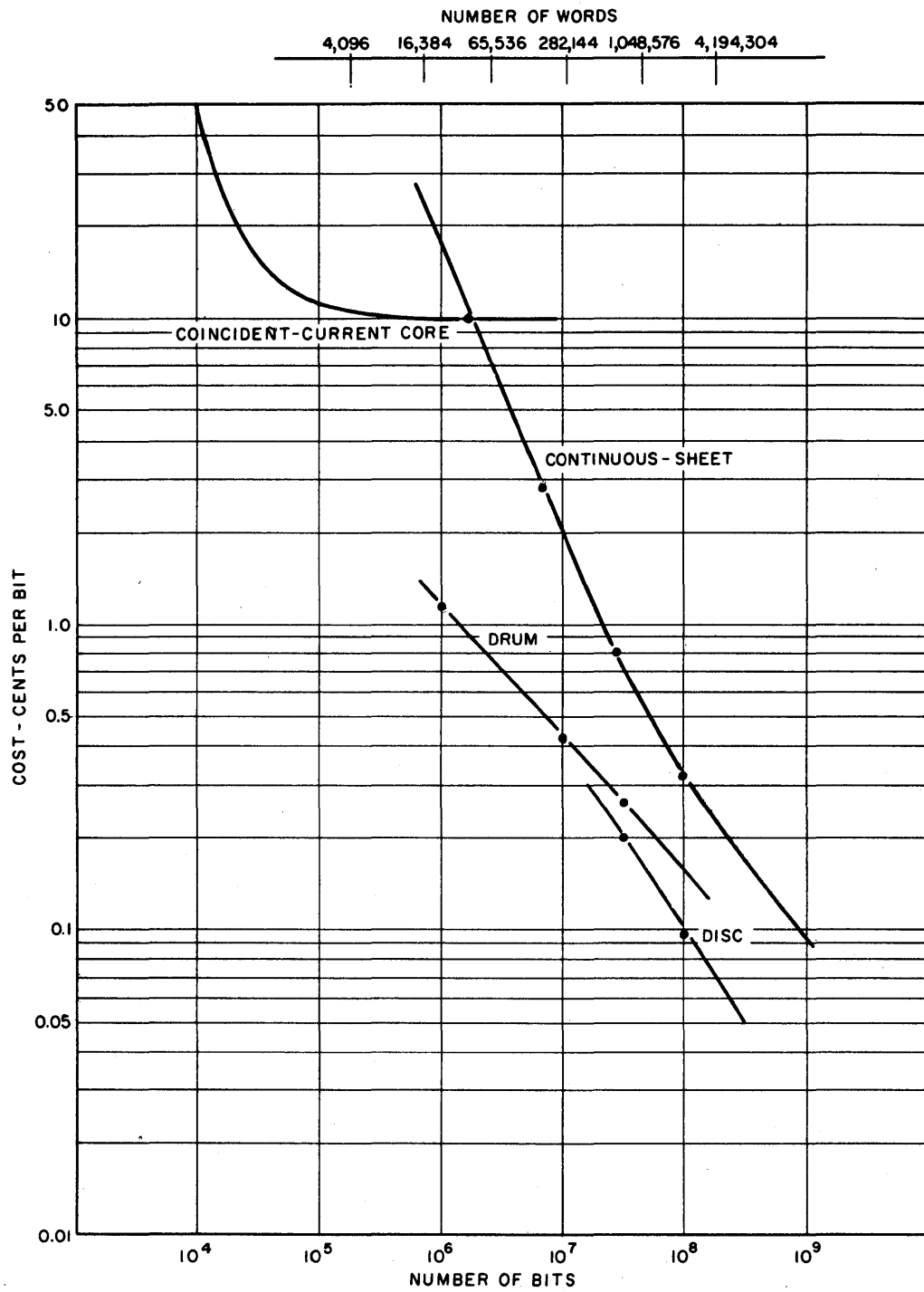
Figure E4. Large Random-Access Memories : Cost versus Capacity

E.3.3 Current Memory Design Trends

E.3.3.1 Introduction

The design and use of memory systems has, in the past
few years, begun to diversify. Various reasons and justifications
can be cited for this trend; however, the over-riding considera-
tion has been the fact that both system application requirements
and logic circuitry speeds have far outstripped the abilities of
the conventional memory system. Many different avenues of avoiding
this problem have been investigated, and certainly some of these
efforts were motivated by other, significant, requirements. The
SOLOMON project at Westinghouse was one such program. Another
was study performed at the National Cash Register Company and
reported at the "Gigacycle Computing Systems Conference"
(Reference E-46).

A third approach to solving this basic problem included
the segmentation of the main memory into N discrete modules; the
CDC 3600 and the Burroughs D825 are examples of this approach.
Yet another approach was the design and utilization of a very
high speed or scratch pad memory as an adjunct to the computer
control unit. This approach was employed by the designers of the
Burroughs 205 when they implemented the "quick access revolvers".
A variation of the scratch pad memory will be found in the
Honeywell H-800, where a small core control memory was employed.
In the H-800 the cycle time of the control memory was of the same
length (6 μsec.) as the main memory, but 180 degrees out of phase;
i.e., when one memory was reading the other was being written in-
to and vice-versa. More recent applications of this approach
can be seen in the UNIVAC 1107, the Burroughs D-825, and the
Honeywell H-200 and the H-300.

Finally, a slightly different method of improving the
overall system performance was, and is being, examined by various
groups. This approach permits the memory designers the greatest
latitude, in that the mode of operation and addressing are per-
mitted to vary. This approach to the memory or portions of the
memory has the greatest appeal to the system designer and portends
the greatest advances for the future.

A number of the more important developments with respect to this last mentioned avenue are discussed in the following sections of this appendix.

E.3.3.2   Read-Only Memories

As S.G. Campbell (Reference E-47) has pointed out, the term Read Only Memory (ROM) is relative. It could also be considered a write unchangeable memory (WUM) from the viewpoint of the originator; however, from the computer's view a ROM is a memory whose contents are unchangeable.

A further distinction must be made as to when (if at all) and how the contents of this type of memory can be modified. For example, a magnetic drum can be utilized in a computer system as a ROM if the write circuitry is not provided, once the desired programs have been placed upon the drum. This particular ROM implies that "loading system" is available at some location and at some time.

A second approach is the card capacitive ROM reported by Foglia, et.al., (Reference E-48) and developed at IBM. Cards are punched and then assembled to provide the memory subsystem. The cards can be physically replaced, but the computer cannot modify the contents of the ROM during the course of processing any program.

Other ROM's have been built employing magnetic material, in various forms, for example, the slug memory in the ATLAS computer designed and built by Ferrante in England.

A slight variation on the ROM is the write optional memory (WOM). This form of memory prefers to be read, since access times are very much shorter than a write time. Thus, the programmer is penalized each time he modifies the contents of a WOM cell. A WOM does have a certain attractiveness and has been investigated by several organizations. Most prominent examples of such memories thus far announced are based upon either the BIAX memory element (Reference E-49) or the UNIVAC BICORE development (Reference E-50). One proposal by Aeronautics (Reference E-51), has suggested the feasibility of designing a WOM which could read in 50 ns but would require 20 μs to write new information into the memory. This proposal was for a 4,000 word, 48 bits per word memory system.

In summary, it appears that ROM's and WOM's are reaching the stage in the development cycle where their use can be postulated and anticipated with confidence. Their first and most advantageous areas of use will be as:

1. Microprogramming mechanisms;

2. Common routine, subroutines, program and constant storage devices; and

3. Possibly, recovery and maintenance units.

E.3.3.3 Associative Memories

Associative memories have received a great deal of attention in the literature during the past few years (References E-52 thru E-57). Several investigators have even extended their study to the stage of postulating elemental computers utilizing associative memories as the heart of such systems (References E-58 thru E-62).

There is no doubt that associative memories will become a factor in the computer science at some point in the future. Neither this point in time nor the extent to which these memories will "revolutionize" the industry can be estimated with any assurance.

Currently small (256 to 4,000 words) associative memories are being constructed and tested. The usual mode of employing this subsystem is as a peripherally connected storage unit. These subsystems are, in general, self-contained; that is, they possess their own drive and sense circuitry as well as the logic and storage required to perform the desired functional comparisons,etc.

Two distinct component approaches have been proposed and examined - cryogenic and magnetic. The advantage of building a cryogenic associative memory would stem from the ability to incorporate and imbed logic at,or in close proximity to,each storage cell. Several studies are currently being carried on and their results should be examined and reviewed as they become available.

It should be noted that the cryogenic approach faces the same drawbacks, discussed in Section 2.2.2, that an all cryogenic computer would.

The second approach is based upon the use of magnetic components. This approach encompasses several different forms of implementation - each with unique advantages and disadvantages. Several of these are briefly noted in Table E-8.

When a relatively small associative memory is required, it is possible to realize such an element by a combination of a very small, very fast memory array in conjunction with a set of hard registers with comparison circuits built of conventional logical elements. If extremely high speed in the association is required, or if the memory is extremely small, hard registers may be used for the data storage also. In the MILDATA time frame, it is quite likely that microelectronic or tunnel-diode realizations of hard registers (Reference section E.3.2.1)may economically and reliably be used for such modules. The searched arguments are read to microelectronic or tunnel-diode comparison circuits, one per comparison per memory read time, in rapid succession; the association is accomplished rapidly enough to be of interest because of the small number of data words - 8 to 64, for example - which are read to each comparison circuit, and the high speed with which they are read. The comparison circuit itself is the same sort of fast adder - with or without carry, depending on the nature of the comparison desired - which is used in the fastest arithmetic circuits of the fastest processor.

Generally, the two principal hardware approaches to the implementation of associative memories, cryogenic and magnetic, in the time frame of interest can be compared as follows (Reference E-66):

1. Magnetic films and ferrite cores require relatively high driving power and have low signal-to-noise ratios.

2. Conventional ferrite cores are difficult to read non-destructively, and may present cross-talk problems between drive and sense lines.

Table E-5

Associative Memory Studies Utilizing Magnetic Techniques

Company	Basic Components	Capacity		Speed Compare (μs)	Reference	Comments
		Words	Bits/Word			
Goodyear	Multi-aperature Cores	256	30	5.0	E-54	Parallel by bit sensing is employed
Philco (Aero-nutronics)	BIAX	2,000	~40	5.0	E-63	Under development
SRI	Cores	1,100	281	7.0	E-63	Delivery in mid 1964 to RADC
IBM	Cores	?	36	~6.0	E-64	Early feasibility study
UNIVAC	Bicore	128	24	0.3	E-65	

3. Cryogenic refrigeration will require large amounts of power.

4. Cryogenic memories in general, and associative memories in particular will still require extensive semi-conductive circuitry at the refrigerator (physical) interface.

Finally, to assist in the future examination of associative memories and their evaluation, three further references should be noted. These references represent attempts by three distinct groups to evaluate associative memories in a broader than usual sense. The first report is Reference E-59, by R.H. Fuller, and was prepared while he was a graduate student at UCLA. In this thesis, Dr. Fuller examined "content-addressable memories" (CAM) as they might appear within a conventional computing system. He postulated a novel command set, and evaluated them via a simulation package as to their efficiency in a job program. Further, he examined applications for CAM's and, finally evaluated several different CAM implementations and variations.

The second, is a report by Hollander Associates (Reference E-67) in which a set of criteria are postulated and employed to measure the performance of many currently announced systems. Two applications are employed for the ultimate evaluation - a target correlator and a spelling correlator. This, as does Fuller's thesis, contains an extensive set of references.

Finally Reference E-68 is highly recommended due to the great similarities which generated the basic study. Due to these similarities the conclusions are quoted below (with minor deletions)*.

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*Reproduced here with the approval of the author.

"At the inception of the study program it has been decided to select three applications for which the use of an associative memory holds promise of improvements in computing time. The criteria for selecting the study problems have been that:

1. The problem be realistic and a solution is really needed.

2. Present techniques are inadequate for an efficient implementation.

3. An evaluation of the improvement in execution times be based on the time required for the entire process rather than portions of it that may favor the use of a hardware associative memory.

Accordingly, the three selected problems were:

1. A Pattern Recognition Process in Bubble Chamber Pictures.

2. An Automated Sea Surveillance System.

3. An Automated Threat Evaluation and Weapons Assignment System.

The studies of problems 1 and 2 have been completed and are summarized in this report. The study of problem 3 is now in progress. Algorithms for the computer implementation of the problem solutions were formulated in terms of flow charts. The times for the execution of these algorithms on an IBM 7094 has been compared with the execution times in a system in which a hardware associative memory would be combined with an IBM 7094. The reference to the IBM 7094 in the study was made as this computer is considered a typical large scale high-speed computer. The results should be applicable and similar if another large scale high-speed computer were used. The conclusions of the study to date may be summarized as follows:

1. A 256 to 512 word associative memory may
   speed-up the Data Association Process which
   is part of the Pattern Recognition of Bubble
   Chamber Pictures, and the Merging of Records of
   of Unidentified Ships which is part of the
   Automated Sea Surveillance problem, by approx-
   imately 30%. These two processes will
   potentially represent a large part of the
   work load in the respective systems. The
   cost of up to a 512 word associative memory
   is well justified by a 30% increase in speed
   on a computer of the size of the IBM 7094.

2. An associative memory of 4096 word capacity
   will speed-up the Sailing Plan Generation and
   Modification processes in the Automated Sea
   Surveillance system by 50%. However, these
   processes represent only a small fraction of
   the total work load of the system.

   Claims of improvements of an order of magnitude
   due to use of associative memories have been
   made in the literature and in various memoranda
   which have been examined in our study. We feel
   that our results are more realistic since:

   a. They incorporate a comparison of a hardware-
      type associative memory with an efficient
      simulated associative memory that is pro-
      grammed in a conventional addressable memory
      and

   b. The comparison is based on the entire pro-
      cess rather than on portions of the process
      where the gain due to the associative memory
      represents indeed an improvement of an order
      of magnitude.

"The associative memory has been used
primarily for retrieval by a combina-
tion of keys. We have realized that if
computational processes can be performed
in parallel within the associative memory
itself, much larger improvements may be
obtained. We believe that in this approach
we have developed a more advanced concept
of an associative memory that will be
employed in the study of Problem 3."

In line with the last paragraph of the above quote, two
brief application investigations were performed. These, due to
their nature, have been reproduced as attachments 3 and 4 to this
appendix.

E.4 Man Machine Input/Output Devices

E.4.1 Introduction

This section discusses peripheral devices used for man
machine communication. Historically, the first such device was
a simple typewriter, or, more explicitly, a typewriter-like key-
board and a single character-at-a-time basket construction
printer. This device was followed closely by the utilization
of punched card equipment and by the development and use of
punched tape equipment and high-speed impact printers. Even
today these devices remain as the standard computer input/output
peripherals on many computers.

The mid 1950's saw the initiation of considerable effort,
both analytical and developmental, towards advanced devices or
device concepts such as non-impact printers, direct character
recognition, visual displays and speech analysis. Two generalized
observations appear relevant to the MILDATA System interests.

1. Peripheral devices categorized as "standard", being
   essentially mechanical in nature, have not kept
   pace with central processor development; in almost
   all regards the peripheral equipment bulk, ruggedness,
   reliability, cost and, to a lesser extent, speed, have
   tended to remain constant over the past decade.

2. The progress made in the area of "advanced"
   input/output devices has been significant
   over the past decade. None the less, the
   level of development of most of those advanced
   devices is again not commensurate with central
   processor capabilities. The reason, however,
   is not one of stagnation but, rather, is due
   to the fact that in general these latter
   devices are on a considerably lower portion
   of the technological learning curve than are
   central processor and memory developments.

These two points indicate that the state-of-the-art of
mechanical input devices is reasonably predictable for the
MILDATA time frame of interest. Conversely, the state-of-the-
art of the newer, (and largely non-mechanical) devices is not
easily predictable. This situation is partly due to the current
steepness of the learning curve in most areas. Further, it also
stems from the fact that the level of interest shown and funding
provided by the military can very well channel research and
developmental activities into preferred input/output device
categories and, to a lesser extent, influence the time period
within which various devices may reach maturity.

E.4.2 Standard Input/Output Devices - Current Status

Standard input and output devices are considered to be:
keyboards, punched tape readers, punched card readers, tape
punches, card punches, character-at-a-time mechanical printers,
and high-speed impact printers. The following comments are
relevant to the utilization of these devices whthin the MILDATA
System.

E.4.2.1 Keyboards

The keyboard is considered an essential device for
entering small volumes of data into the system when that data
originates at or near the location of the central processor
itself. The per-character speed of the keyboard is limited by
human operator, to approximately 10 to 15 characters per second
as a maximum. Advances in keyboard entry rates are precluded
by its very nature. However, its effective rate can be increased
by the inclusion of specialized keys having particular and fre-
quently used control significance to the associated central
processor.

E.4.2.2   Paper Tape Equipment

        The Second MILDATA Quarterly (Reference E-29) notes
that over the last decade tape reading speed increased tenfold,
to 1,000 characters per second. Tape punching speeds showed no
such increase, however. Further, an examination of reading
speeds over the latter portions of the decade shows no significant
advances. Therefore, tape equipment seems to have plateaued. A
significant fact about punched paper tape should be noted; namely,
the initial preparation requires a keyboard, and final utiliza-
tion requires decoding on a printer. Thus, these devices can be
classified as intermediate storage. They are categorized as
input/output devices here because the preparation can be
accomplished in one step by a human operator (in contrast,
magnetic tape preparation requires at least two steps; the pre-
paration of a tape or card input followed by a run on the
computer to create the magnetic tape record). It is felt that
punched tape equipment will have a very useful place within the
MILDATA System. In particular, a hand punch requiring no external
power source might be very useful. For example, it would be a
simple way to record logistics data in combat area supply depots
for subsequent entry into a remote data processor.

E.4.2.3   Punched Card Equipment

        Cards, like punched paper tape, are but an intermediate
storage media requiring initial manual preparation. Reference
E-29 shows a six-fold increase in card reading speed over the
last decade, due mainly to the development of photoelectric
column-by-column readers. In contrast, only a 1.2 gain in card
punching speed is noted. The cards have these advantages over
tape as a storage media: off-line sorting, individual card
insertion, deletion or replacement, and unit record capability.
However, a significant drawback is to be noted; the card size
is fixed by tradition and is an inefficient storage media in
terms of the information contained per volume. This has not
been serious for the business world. For MILDATA, though, this
could present a serious logistics problem, requiring more bulk
than necessary both in cards and in card handling equipment.
The relative bulk of cards and of the associated handling equip-
ment, together with the fact that their functions can be per-
formed by the central processor (sorting), by tape equipment
(storage) and by direct character recognition devices (unit
record) makes their use questionable and undesirable in the
MILDATA time frame.

E.4.2.4 Character-at-a-time Printers

Here again, no speed progress is evident in character-
at-a-time printers over the last decade. Impact printers
typically operate at rates of 10-30 characters per second per
mechanism. Higher speeds impose severe mechanical stresses on
the impacting mechanisms causing fatigue and ultimate failure.
These rates are considered adequate for small volume outputs to
the system operator wherein message permanency is desired or
required. These rates are also generally associated with edge
printing on paper tapes or cards. The need for (and speed of)
character printers operating in the edge-print mode will be
very much a function of the utilization of paper tape and card
equipment within the MILDATA System.

E.4.2.5 High-Speed Impact Printers

High-speed impact printers matured early as a computer
peripheral device. In all cases the speed was realized due
more to quantity than to innovation. A 900 line per minute
printer, for example, prints at the rate of 15 characters per
second per print station. The high printing rate is realized
by a multiplicity of print stations, typically 60-120 identical
stations. Limitations of this type of printer, aside from the
sheer multiplicity of mechanisms, arise from the following: the
technical difficulties of handling large quantities of paper at
high speed, the logistics associated with maintaining the supply
of paper, and the problems associated with adjusting the print
quality as the number of carbon copies vary.

E.4.2.6 Non-Impact Printers

Although non-impact printers more properly belong in
the category of the advanced devices, there are nontheless many
similarities in the technical problems encountered to warrant
their discussion alongside mechanical impact printers. There
are many techniques available for non-impact printing. Broadly
they can be categorized as: electrostatic, electrochemical,
electroconductive, and cathode ray tube (CRT) display accompanied
by photography. The first three, although capable of rates far
in excess of mechanical impact, printers, nonetheless encounter
the same paper handling and paper logistics limitations
associated with mechanical impact printers. In fact, the paper

logistics problem is even more severe due to the need for specially prepared paper stock. The MILDATA First Quarterly (Reference E-69) analyzed the need for multiple copies and for hard copy in general. It concludes that the requirement for hard copy (such as for personnel pay checks) is sufficiently limited to be handled by present day print rates. It also notes that the requirements for multiple copy are both infrequent and variable. Note that all of the non-impact printing techniques produce but a single copy at a time. For the various electrical techniques, multiple copies could be manufactured by repeat computer transmissions; the CRT/photographic technique can utilize one negative to produce multiple copies, relieving the central processor, or the system, of repeated transmission requirements.

The preceeding discussion suggests that CRT display/ photographic techniques should be considered a prime candidate for implementating high-speed printers within the MILDATA System. In any event, it is felt that the military should give preference to non-impact printing methods, certainly for high-speed printing purposes and possibly for the lower speed character-at-a-time edit printers as well.

Reference E-70 contains a comprehensive treatment of the devices discussed in Section E.4.2. Although this reference was prepared in 1959, the general conclusions reached therein remain valid today.

E.4.3 Advanced Input/Output Devices

E.4.3.1 Character Readers

The advantages of direct character recognition are obvious; human intervention and the associated data transcription in correcting printed hard copy into machine sensable format are bypassed. Commercial character recognition devices have been operable for several years. Prime examples are bank checking accounts and gasoline service station credit cards. However, all existing character readers read but a single, pre-stylized alphabet. Successful efforts to read handwriting, or a multiplicity of alphabetical styles, with negligible or even tolerably low error rates appear to be beyond the MILDATA time frame. Reference E-71, E-72 and E-73 are representative of recent efforts

in this regard. However, an experiment is underway at MIT (to
be reported upon in the Fall Joint Computer Conference, October
1964) which shows great promise for accelerating the progress
of direct handwritten character recognition. In the method in
question the person who wishes to address the computer prepares
a sample of his handwriting (or hard printing) for insertion into
the computer. The computer, through software, develops a set of
rules for recognizing that particular individuals handwriting
only. The computer can display what it has recognized to the
individual doing the writing. In turn, the individual can revise
his method of executing the characters so as to increase the
computers capability for recognition. Once the computer has
developed the recognition criteria, the individual in question
may then proceed to feed messages to the computer. While the
software techniques for decoding an individuals writing might
be relatively slow such a technique would, nonetheless, prove
useful for field operation. Presumably, a library of
identification routines could be built up for those individuals
normally addressing the computer at frequent intervals. Thus,
the system would not be faced with the task of on-the-spot
development of rules every time a message was received. A
simple technique such as edge punching of each handwritten docu-
ment could be used to identify the originator of the document.
Only in those cases where the originator had not previously
addressed the computer would the rules for decoding the
individuals handwriting be developed on the spot.

E.4.3.2 Voice Recognition Devices

The advantage of voice recognition devices are even
greater than those of direct character recognition devices.
Not only is an intermediate operation eliminated, but the
technical problems of form handling and character registration
no longer exist. Much research is currently under way to
evaluate and understand the characteristics of speech. Present
successful efforts at the practical recognition of vocabulary
by machines are limited to vocabularies of single syllable
(see References E-74 and E-75 for recent reports, including
a comprehensive bibliography, of work in this field) sounds
(50-100 syllables) or to an even fewer number (10-20) of one
or two syllable words (such as the 10 numerals). Furthermore,

the recognition devices are generally tuned to a particular speaker's vocal characteristics. Recent projections are that by 1970 voice recognition devices will be available having a recognition vocabulary of from 500-2,000 words as spoken by 10-20 individual speakers. The vocabularies, in all probability will not be chosen for their word content; rather, they will be chosen in large measure for the phonetic dissimilarities between words in order to facilitate recognition by the machine. However, with vocabularies of several hundred words there should be sufficient leeway to permit a considerable number of useful vocal commands and queries to be delivered to the central processor instigating immediate system reaction thereby.

E.4.3.3 Direct Display Devices

Mechanical plotters, cathode ray tube displays, and various photographic-large screen display systems are available today (Reference E-76). Such devices are far more suitable for presentation of many forms of graphical and situation data than would be the case if the data were printed. Numerous CRT displays, capable of displaying alphanumeric and graphic data, are available (see Reference E-77) as well as a considerable number of slower mechanical plotters. The large screen photographic displays developed for military command and control in general utilize a CRT generated picture which is photographed and subsequently projected as a slide onto a screen. It is expected that CRT displays will be a necessary adjunct to MILDATA, both for graphic and printed presentations.

The CRT is entirely satisfactory for one-man displays and for most situations where a very small number of viewers are present. For large displays, used simultaneously by a large number of people, the present CRT/photoprojection technique will probably be replaced by more sophisticated devices in the MILDATA time frame. The most promising techniques today appear to be "light valves" and electroluminescent displays. The "light valve" is a technique wherein the functions both of electron beam writing and of image projection of the display are combined within one cathode ray tube. While "light valves" have been operated, they presently are limited by inefficient resolutions, low overall image brightness and poor display contrast between image and background. An electroluminescent display consists of a mosaic or matrix of individual electro-luminescent cells each stimulated by a coincidence of x-y

electrical signals. This latter display technique, being wholly solid state, offers inherent advantages in reliability, ruggedness and diminished equipment bulk. However, there are significant technical problems to overcome, not only with the individual electroluminescent cell itself but also with the large amount of equipment required to address such a display. Reference E-78 contains a good summary of the characteristics and limitations of large, multi-viewer display systems.

A particular advantage of direct displays should be noted. The displays, from an operator viewpoint, can be considered to be either eraseable, alterable, or permanent. Permanency is achieved, of course, through photography.

E.4.3.4 Light Pens

"Light pen" is a name given to a particular type of input device for use with CRT displays. The operator points the pen to a particular area on the display. As the CRT electron beam sweeps over the area in question, the pen is energized and the x-y coordinates of the spot are noted within the computer. The operator can then inform the computer what to do with the designated area (e.g., he could correct a character, ask for a modification of the area, etc.). The combination of CRT display, light pen, and specialized entry keyboard permit a degree of conversation between man and computer which is much more intimate than that previously achievable with more conventional input/output techniques. Reference E-79 describes a system of this sort (called SKETCHPAD) which is under development at MIT.

E.4.3.5 Audio Output

Of the more advanced devices under discussion, audio output is perhaps the easiest to realize. Typically, a vocabulary of preselected words is prestored in analog fashion on a multi-head drum (see Reference E-80). The computer can select combinations of words to make sentences. The drum outputs are then directed to an amplifier loudspeaker system which could be on-site or remotely located. It is not at all improbable that, within the MILDATA time frame of interest, complete audio conversations between commander and computer will be possible, at least in certain limited applications. For example, with properly preselected vocabularies, a commander might conceivably inquire verbally as to the ammunition or personnel status in the various sectors of a battle zone and receive an immediate verbal reply.

E.4.4 Usage Considerations

In the preceeding two sections the salient characteristics
of current and advanced input/output devices have briefly been
outlined. The ultimate selection for MILDATA usage (assuming
adequate availability) depends upon application criteria.
Several of the more significant usage criteria are discussed
below.

E.4.4.1 Environmental and Physical Factors

Rapid progress in the semi-conductor and other materials
fields has allowed for startling advances in the size, weight,
ruggedability, environmental non-susceptability, and reliability
of the central processor and main memory. These advances are
expected to continue through the utilization of integrated
circuits. In contrast, virtually no progress has been made in
these same regards for such mechanical input/output devices as
keyboards, impact printers, punched tape and punched card equip-
ment. The limitations of these devices, will probably also be
inherent in the paper handling portions of non-impact printers
and in the form handling portions of character recognition
devices. Many of the aforementioned input/output devices will
be essential to the MILDATA System. Therefore, every effort
should be made to minimize their use, by reducing the volume of
data to be handled by such devices.

The environmental and physical limitations of the
conventional input/output gear present powerful arguments
favoring the development and ultimate utilization of the more
advanced devices previously discussed. Not only are these
advanced equipments more subject to the reliability and com-
pactness of audio/optical/electronic devices, but they are also
in the early stages of development compared to the essentially
mechanical devices. Therefore, the normal evolution of these
devices is more susceptable to recognizing and reflecting the
requirements of military environments during the design and
development of second generation equipments.

E.4.4.2 System Response Time

Reaction times will vary considerably for the variety
of MILDATA applications. To meet troop payroll, for example,
present day input/output equipment response rates are more than
adequate. At the opposite pole, however, control over battle-
field troop movements and weapon assignments, etc., will require
instantaneous reaction. For the latter situation it is desirable
to bypass all intermediate steps of data preparation, trans-
cription and consumption, either by machine or human. These
latter considerations again tend to illustrate the advantages
of direct voice communications, CRT/light pen combinations,
specialized control keyboards, and character recognition
devices; that is to say, utilization of devices in these latter
categories is essential to improving response speed, in contrast
to increasing the data rates of existing mechanical devices.

E.4.4.3 Programming Considerations

An advantage of tape, card, keyboard and mechanical
printing devices is the relatively simple programming associated
with their use. In contrast, direct character recognition
devices, voice input/output, and CRT/light pen techniques will
require either relatively sophisticated programs and/or pro-
portionately larger volumes of storage. These more demanding
programs and storage requirements should not handicap the
MILDATA System. To the contrary, the speeds and storage cap-
abilities of the postulated MILDATA System can be put to good
advantage, servicing the particular requirements of the
sophisticated input/output devices by the proper implementation
of time-sharing techniques. In fact, if some of the more
sophisticated input/output devices postulated here do not
materialize, the MILDATA System may very well become input/
output limited and optimum utilization would not be obtained.

E.4.4.4 Formating Requirements

Proper utilization of any data handling system is, in
many instances, dependent upon pre-determined formating rules.
These rules include the selection of the vocabulary to be used
(both external and internal to the central processor) as well
as rules for positioning the characters and data into words,
fields, records, etc. This is standard procedure in the

utilization of keyboard commands, card and tape inputs, printer and tape outputs, CRT displays, etc. It is more than reasonable to expect that formating rules will be required for audio and direct character inputs, cathode ray tube/light pen conversational techniques, etc., to optimize the utilization of these devices. The development of rules and regulations, in coincidence with the development of peripheral hardware and software, may very well hold the key to practical utilization of direct character and voice inputs at an early date. Two examples that are immediately obvious are:

1. Utilization of a stylized alphabet cross hatched field and limitation of a character per block for handwritten inputs. This technique would simplify the problems of form handling associated with machine reading of the documents. Further, all information pertaining to a given situation could always appear in the same pre-ordered format. For example, a platoon commander, when reporting upon his particular platoon's situation, might always organize the report to begin with platoon, company, and battalion number followed by ammunition, personnel, and provision status, etc.

2. For other applications where voice input might be desirable such as the consumption and correlation of intelligence data, a limited vocabulary input device to the central processor may be of no advantage. However, for more routine and high volume situations, such as the insertion of hour-to-hour or day-to-day information on troop, ammunitions, and provision status, the advantages of a carefully chosen, limited vocabulary would seem considerable. In this instance, rules for formating the sequence of words might not be so important as rules for ennunciation of the syllables involved.

E.4.4.5 Training Requirements

Carefully chosen formating rules can minimize the required degrees of operator skill and associated training. Two problems arise with direct voice and handwritten character inputs: first, the input error rate is potentially high; second, each data originator is, effectively, a system operator. Present day systems place personnel in the data origination cycle, both to transcribe the data and to introduce error detecting (and sometimes correcting) measures. The use of additional personnel in this "feed forward" manner would defeat the concept of direct voice or character inputs. Therefore, the use of "feedback" principles is more applicable towards the effective utilization of the system operator towards controlling error rates to acceptable levels in the MILDATA System. The following technique is recommended: As each voice or handwritten message input is read into the central processor the CP could, in turn, display that message upon a cathode ray tube to an operator (called a "display attendant"). It would be the attendant's function to compare the handwritten or voice message just entered into the machine with the information presented on his display and, with a light pen and keyboard, to correct any significant errors appearing in the displayed information. After correction, or if no significant errors were initially present, the attendant can then allow the message into the central processor as valid data. This technique would be very useful during training in order to assist the potential machine communicators to improve both their handwritten and speaking vocabulary. Presumably, then, the initial field error rate when recognizing the vocabularies of trained operators would be low. Employing a monitor in the fashion recommended, namely in the feedback rather than the feedforward loop, could reduce the ultimate error rate to a negligible value. Utilization of a display attendant in this manner would also afford an additional measure of security; the attendant could filter out messages which are suspected as having originated with the enemy. Finally, the employment of feedback principles, both in training and in field operation, could make for an earlier utilization of handwritten character and direct voice inputs than might otherwise be possible.

E.4.5 Summary

The preceeding paragraphs have discussed generalized
considerations relevant to input/output equipments, both as
regards device characteristics and usage considerations. The
numbers and nature of input/output devices utilized within
the MILDATA System will be a function of the applications,
the data origination points, the data volume, and the data
destination. As such, a usefulness for all of the devices
discussed (except possibly punched card equipment) will exist.
However, the greatest payoff in MILDATA will be derived from
relatively new or presently non-existent devices; specifically,
cathode ray tube displays, cathode ray tube-to-print devices,
direct character recognition equipment, audio input/output
devices, and light pens and other special control devices.
The payoff from these devices will be realized not only in
terms of reduced reaction time, but also in reliability,
ruggedness, size reduction, and decreased paper logistics, etc.
However, the realization of the potential that exists will
require military funding. This requirement spans the gamut
from advanced research, in the case of audio input devices, to
the militarization and refinement of currently existing devices
such as CRT displays. Finally, it is recommended that an inte-
grated effort to develop software packages and useage criteria
simultaneously with the hardware investigations to produce
more useful "equipment systems" at an earlier date than would
otherwise be possible, be undertaken at the earliest possible
date for the greatest possible payoff.

E.5 Bulk - Peripheral Storage Systems

E.5.1 Introduction

In designing a system for the combat zone in the MILDATA
time frame, the two areas; input/output, and bulk storage systems,
present the most difficult goals for attainment. The question
of input/output devices has been discussed in the preceeding
section of this appendix. In this section, a brief discussion
concerning the requirements and possible methods of attainment
for bulk peripheral storage systems will be presented.

During the past ten years, the storage capacity require-
ments in data processing systems have generally increased at an
almost exponential rate with only moderate improvements in
access time. This trend will continue. The reader need only
consider the massive file structures required for the intelligence
application or the Tactical Operations Center to realize that as
the storage capabilities of the various devices increase, the
users desires can be expected to continue to surpass the properties
of currently available equipment. (Reference E-81)

A new factor is the radical decrease in access time
associated with recently announced electronic moderate capacity,
bulk storage systems; such as the SCREEN DOOR, BORAM, and large
scale film memories. Hobbs (Reference E-82) presented a very
lucid and clear discussion of the whole subject. His conclusions
appear to be generally valid except for one consideration. This
concerns the fact that he was concerned primarily with the
commercial application and utilization of mass bulk storage
systems. Necessary modifications to his conclusions must be
made within the MILDATA System and the battlefield environment.

E.5.2 Discussion

Bulk mass storage requirements for the various echelons
of the Field Army in the MILDATA time frame cannot be considered
without taking into account the types of communications
facilities which will also be available for use by the data
processing system. For example, if no communications adequate
for the use of mass transfer of information from one point to
another is available, bulk storage must be provided at each
site to the extent required by that site for the application
to be performed there. If, on the other hand, broad-band,
point to point, communications channels of reasonable reli-
ability, and adequate security can be expected; then the trans-
ference upwards to higher echelons of the bulk storage facility
for forward echelon units can be considered. Further, two
additional factors must be taken into account when discussing
this general question. First, is the physical displacement of
the various processing nodes, one from another, within the
overall system. This distance will impose a time of trans-
mission, effectively added to the storage system's access time
which would have to be taken into account. Secondly, the type

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of problem and its minimum acceptable response time and the
expected number of bulk storage accesses per unit time. For
example, the processing of a Logistics Program, could be
delayed for milliseconds or even (in extreme cases) seconds.
On the other hand, a Fire Support application, based upon a
real-time input, could not afford even a minimal delay.

Thus, the implementation of mass storage at each node
will differ, depending upon the communications facilities
available, the applications span required of the system at that
location, and (possibly) the nodes relative location to the
Forward Edge of the Battle Area.

In the event that no adequate communications facilities
are available, or the response times are too short; and the
current trend in the state-of-the-art continues at its present
rate, the following classes of peripheral bulk storage devices
will be required:

1. A few million characters. (Non mechanical
   storage system.) This device will be utilized
   at the lowest echelons to store data for
   immediate use on a day-to-day basis.
   Desirable characteristics would include the
   ability to have a storage dump capability
   for transmitting of information, via some
   media, to higher echelons for incorporation
   into the more extensive file systems which
   would be found at those locations.

2. Hundreds of millions of characters. (Preferably
   non mechanical - moving unit media acceptable.)
   These systems, based upon the concepts gene-
   rated by NCR, RCA, IBM, etc., (References E-83,
   E-84, and E-85) would be applicable in the
   intermediate range of applications and at the
   intermediate echelons of a Field Army.

3. Very large (10^9) characters or more. (Probably mechanical storage.) At the highest echelons (either at the Field Army or at the Corp level devices which will bear a striking resemblance to large disk systems will probably be employed in conjunction with magnetic tape systems of some form or other.

One development which was previously mentioned in Section E.3.3.2 may help in alleviating some of the bulk storage requirements. This development concerns the utilization of read only memories. For the large bulk mass storage system, the suggestion recently published by personnel from the Sylvania Electronic Systems Division (References E-86 and E-87) requires and warrants additional and deeper investigation. The concept of the solenoid array storage mechanism seems to provide a method of storing large tables of information and programs for utilization by the computer with a minimal amount of access time required. An alternate approach currently being examined by RCA (Reference E-88, E-89 and E-90) which would permit the updating and changing of information still is in the early stages of development and cannot be evaluated.

E.5.3   Summary

The providing of bulk mass storage will be one of the more critical considerations in the peripheral area for the MILDATA System. Compensation for a mass storage system at each computer site can be obtained for some applications, but not for others, by the utilization of broad-band communications in conjunction with the individual data processing systems. This point will require further, extensive study and evaluation.

However, regardless of the outcome of that investigation, funding support will be required to provide non-mechanical, large, fast peripheral storage mechanisms in the storage capacity levels required.

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E.88. Onyshkevych, L.S.; "Digital Computer Peripheral Memory",
Report #1, Contract No. DA36-039-AMC-03248(E), Sept. 1963,
39 pages.

E.89. Onyshkevych, L. S.; "Digital Computer Peripheral Memory"
Report #2, Contract No. DA36-039-AMC-03248(E), Dec.1963,
61 pages.

E.90. Onyshkevych, L.S.; Shahbender, R.A.; "Digital Computer
Peripheral Memory", Report #3, Contract No. DA-36-039-AMC-
03248(E), March 1964, 35 pages.

APPENDIX E

ATTACHMENT I

ATTACHMENT I

Mechanism for Computer Characteristic Extrapolations

1. General

An extrapolation software package was designed to be capable
of plotting any complex set of characteristics against any other
complex set while specifying boundary conditions. The objectives
of the program package can then be defined as follows:

1. Convert the collected data into a form easily used
   for manipulation by the computer.

2. Select data points for any set of X and Y variables,
   where either or both variables may be a single
   computer characteristic or combination of characteristics.

3. Plot the data with both X and Y variables shifted and
   scaled sufficiently to spread the data points over the
   full graph area, and to label the axes accordingly.

4. Fit curves, in a least squares manner, to the data
   points, or subsets of those points as required to
   obtain an envelope effect, and plot these curves and
   their descriptive constants.

In plotting the data the major problems were:

1. Putting meaningful labels on the axes.

2. Selection of the most appropriate extrapolation
   mechanism.

2. Program Description

The extrapolation package shown in Figure E-I-1 consists of
four programs which are described here in the order in which
they are normally used.

E-I-1

MILDATA COMPUTER CHARACTERISTIC
EXTRAPOLATION SYSTEM

FIGURE E.I.1

E.I.2
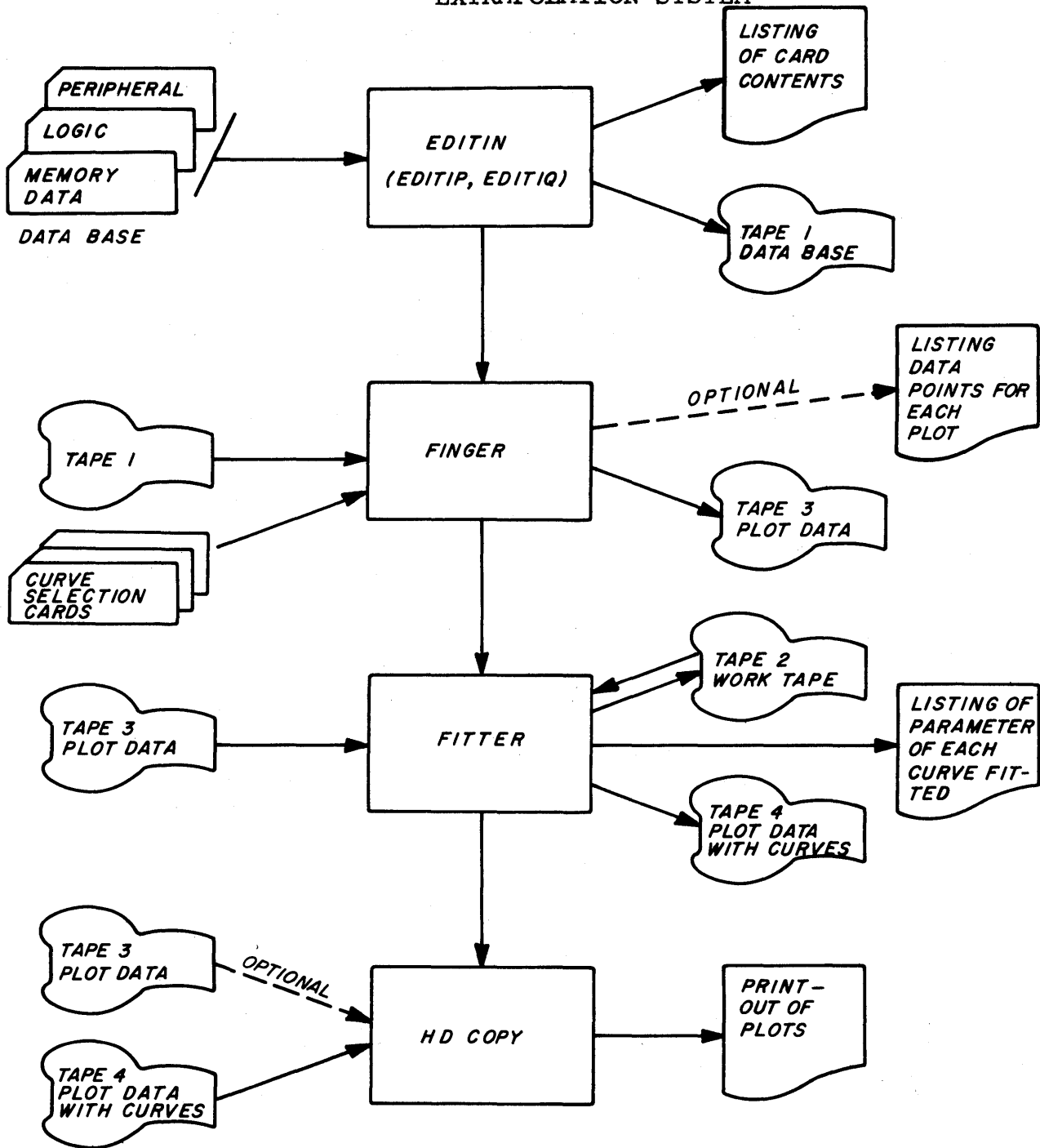
2.1 Data Transformation - EDITIN, EDITIP, EDITIQ

These three programs are essentially identical, being used to edit, respectively, memory data, logic data, and peripheral data. They will be discussed as one program.

This program reads the data from cards, one card per computer or device, and interprets it according to the format of that card type. Each card's contents is printed out to provide checking for card punch errors. The numeric fields are converted to logarithmic form, using a tree conversion.

All numbers here are given in the form in which the data appears after it has been logarithmically converted onto a scale of 24 units per Bell. The data is to be fitted onto a fixed scale 102 units on both X and Y axes. Thus, if memory access time varies from 100 nsec to 100 milliseconds it's converted values range from 72 to 216. Therefore, divide by 1.5 and then subtract 34 to give a final range of 2 to 96. (Note the base is 0.1 nsec., 100 ns is therefore up 3 Bells: 3 x 24 = 72, etc.)

A type 2 card must always accompany each pair of type 1 cards. This card indicates whether all available points are to be plotted or not. The type 2 card also supplies the actual characters to be printed on the printer for each data point. It specifies the character to print for a single point for two data points on the same spot, for three points, etc., up to five different characters may be specified. The converted numeric information and all non-numeric identification data is then stored on magnetic tape, with the numeric data being in signed fixed point decimal form.

2.2 Plot Selection - FINGER

The function of this program (Figure E-I-2) is to select all data needed for a particular plot. Its inputs are from the tape on which the base data has been stored by the previous program and a stack of punched cards which specify all parameters of each plot.

The functions of the program are best described by listing the functions and options involved with the various types of input cards.

E.I.4

READ CARD

INITIALIZE CHECK CARD TYPE

CARD I

SET OPERATOR TO "REPLACE"

SELECT FILE READ TAPE RECORDS INTO SAI SELECTING POINTS INTO SA2

COMBINE SA2 & SA3 INTO SA3 ACCORDING TO OPERATOR READ NEXT OPERATOR

NO NEW OPERATOR

DIVIDE DATE BY SCALE FACTOR & SUBTRACT SHIFT FACTOR. WAS THIS 1st. or 2nd. PASS ?

SET OPERATOR TO "ADD" OR "SUBTRACT"

FIRST PASS (X DATA)

SECOND PASS (Y PASS)

WRITE DATA ONTO TAPE 3 FOR TEMP. STORAGE

READ CARD TYPE 2

WRITE DATA ON TAPE (TAPE 3) INCLUDING CURVE SPECIFICATIONS AND PRINT PARAMETERS

TYPE I

TYPE 2

READ CARD

READ X DATA OFF TAPE 3 INTO SAI MERGE X & Y INTO ALTERNATING POS. IN SA2-SA3, ELIMINATING POINTS FOR WHICH X=0 or Y=0 PRINT OUT POINT LISTING

NO NEW PARAMETER

READ SELECTION PARAMETER

EXTRACT CURVE PARAMETERS

TYPE 4

SELECT FILE READ TAPE TO SAI. FOR EACH ITEM, COMPARE POINT TO SELECTION CONDITION SET CORRESPONDING PT. IN SA3 TO ZERO IF CONDITION NOT MET

WRITE Y LABEL ON TAPE 3 EDIT DATA INTO X AXIS LABEL READ CARDS UNTIL TYPE I FOUND WRITE X LABEL ON TAPE

EDIT DATA INTO Y AXIS COORDINATE LABEL READ CARDS UNTIL X AXIS CARD FOUND

LEGEND

SA — STORAGE AREA
CARD I — VARIABLE SELECTION
CARD 2 — PRINT CHAR., & 3 rd. PARAMETER FOR DATA SELECTION
CARD 3 — CURVE TYPE
CARD 4 — COORDINATE LABELS

FIGURE E.I.2

Card type 1 is used to specify the characteristics to be plotted on each axis. These cards always come in pairs; one each for the X and Y axes.

It is possible to plot several groups of points on the same graph, where each is specified by a pair of 1 cards and a 2 card. In this case, the type 2 cards would each give different print characters so that the groups could be distinguished and yet compared on the same chart.

A type 3 card specifies the nature of each curve to be fitted to the data points. One card is used for each curve, with a maximum of three curves allowed per plot. This card specifies the degree of the curve, with possible values ranging from 0 to 3. It also indicates that segment of the points to which the curve is to be fitted, namely all points, upper one-half, upper one-fourth, upper one-eighth.

A curve need not be restricted to being fitted on all points of a given plot. It can be fitted on a subset of these points according to the type 3 cards position in the deck of cards specifying that plot. A curve is fitted to all points in a plot which are specified before the type 3 card appears, but after the previous non-adjacent type 3 card.

Card type 4 is used to put labels along the two axes. A type 4 card signifies the end of a plot, with the next non-type 4 card to follow being taken as the first card of a new plot. There is no limit to the number of plots which can be specified in a given computer run.

The program which reads these cards produces an output tape which contains all the data, points and coordinate labels. For each pair of type 1 cards and accompanying 2 card, it searches the data base tape for the desired data, combines scales, and shifts the data as instructed, writes it on tape, and optionally prints it out. It edits type 3 cards into instructions on tape which will be operated upon by the curve-fitting program. Type 4 cards are edited into labels which are used directly by the plot printing program.

2.3 Curve Fitting - FITTER

The curve fitting program has a single input, the tape prepared by FINGER and a single output tape. This program copies the input tape onto the output tape up to the point where a curve must be fitted to the data. The curve-fitting routine actually consists of two routines, one which builds up an (N+1) (N+2) matrix for an N-degree curve, and one which solves the matrix for the curve equations (Figure E-I-3).

If the curve is to be fitted to the upper one-fourth of the data, then after fitting the curve, the program eliminates all data points which fall below the curve and then re-enters the fitting routine. Given the new curve it again eliminates points below that curve, and again re-enters the fitting routine, with the output this time being the final result.

Once the curve parameters are found, the program calculates the curve value for every Y value, and writes these on the output tape in such a form that they will be printed to give the curve.

The output of this program, then is a tape containing data points, curve points, and axis labels, with everything prepared for printing.

2.4 Printout - HDCOPY

Hardcopy prepares a full printed page image in memory by taking points as they come off tape and inserting the appropriate character in the correct image locations. When all data for a given plot has been read off tape, the labels are attached and the whole thing is printed out. No data modification is performed in this program except that all Y values are divided by two since there are only 53 available vertical, print positions as compared to more than 106 horizontal positions.

READ TAPE 3,
COPYING ONTO
OUTPUT TAPE (4)
UP THRU DATA

END
TAPE

EXIT

TAPE 4
NOW
PREPARED
FOR
PRINTING

COPY DATA FROM TAPE
3 TO TAPE 2 CON-
VERTING FROM FIXED
TO FLOATING DECIMAL

EXTRACT CURVE
SPECIFICATIONS

SET UP CURVE
DEGREE
POS. TAPE 2

LEAST SQUARES
FITTING
ROUTINE

REPOSITION
TAPE 2

PRINT CURVE
CONSTANTS

CURVE TO BE
FLOATED ?

FLOAT

COPY DATA AGAIN
TAPE 3 ⟶ TAPE 2

FIX TO FLOAT CONVER-
SION

COMPARE EACH POINT TO
CURVE VALUE, THROW-
ING OUT THOSE ABOVE
OR BELOW CURVE

ANOTHER
CURVE

COMPUTE CURVE FOR
PLOTTING
WRITE POINTS ON
TAPE 4
ANOTHER CURVE ?

NO FURTHER CURVE
FLOATING

MORE
DATA

MORE DATA
IN THIS
PLOT ?

LAST
CURVE

INITIALIZE
ALL
CONDITIONS

EDIT CURVE CONSTANTS
INTO X AXIS LABEL AS
TAPE 3 IS COPIED ONTO
TAPE 4 UP THROUGH
END OF PLOT DATA

E.I.7

FIGURE E.I.3

APPENDIX E

ATTACHMENT II

ATTACHMENT II

Analysis of Extrapolated Results

1. Projected State-of-the-Art

The curves presented in Attachment III, Extrapolation
Results, of Appendix E represent a selected portion of the
results obtained. For a complete and thorough discussion the
reader is referred to MILDATA Quarterly Report Number 2.*

The majority of the extrapolations were highly satisfying,
producing trends generally consistent with anticipated results.
Table E-II-1 shows the projected position of each characteristic
in 1971. The following comments are in order with respect to
this table.

1. Cycle time is a meaningless characteristic when
   considering drum and disc memories. Access time
   is a more meaningful parameter for all devices.
   Cycle time projections were therefore not tempered
   by the slow memory characteristics of the early
   (pre 1958) drum and disc machines whereas access
   time was. The cycle time figures, though con-
   sistent with anticipated speed in 1971, is not
   truly indicative of memory evolution, however,
   access time is (though somewhat slower than
   generally expected).

2. The projected transfer rate is sufficiently slow
   with respect to both access time and cycle time
   as to indicate that majority of computing systems
   will either not need what the state-of-the-art can
   provide or character oriented machines will become
   increasingly popular. This observation is
   strengthened by comparing add time (exclusive of
   memory access time) to access time. It appears
   that the industry will be at a point where logical
   hardware will be lagging.

_____

*See Reference E-29

Raw Projected Computer Characteristics - 1971

Characteristic	Highest Octant	Highest Quartile	Average	Lowest Quartile	Lowest Octant
A. Memory					
Access Time	50 ns	100 ns	300 ns	900 μs	10 ms
Cycle Time	30 ns	X	150 ns	460 ns	X
Transfer Rate	500×10^6 b/s	80×10^6 b/s	15×10^6 b/s	7.5×10^6 b/s	1.0×10^6 b/s
Max. Capacity	8×10^9 wds	2×10^7 wds	1.4×10^6 wds	4×10^5 wds	5×10^4 wds
Min. Capacity	5×10^9 wds	3.5×10^6 wds	2×10^5 wds	2×10^5 wds	X
Maximum Cost	$40 K	$50 K	$60 K	$80 K	$180 K
Minimum Cost	$2.5 K	$3.2 K	$6 K	$20 K	$45 K
Transfer Rate / Minimum Cost	X	250	100	30	X
Transfer Rate / Maximum Cost	X	X	20	15	9
Transfer Rate / System Cost	300	20	0.9	0.6	X
Min. Capacity / Minimum Cost	700	18	1.5	X	X
Max. Capacity / Maximum Cost	8	3	0.2	X	X

Raw Projected Computer Characteristics – 1971

Characteristics	Highest Octant	Highest Quartile	Average	Lowest Quartile	Lowest Octant
X Max. Capacity Transfer Rate	10^{13}	X	2.5×10^{12}	3×10^{10}	2×10^{10}
Max. Capacity Cycle Time	X	1.5×10^{12}	6×10^{11}	X	10^{11}
B. Logic					
Add Time	90 ns	300 ns	700 ns	2 μs	X
Multiply Time	12 μs	15 μs	45 μs	150 μs	400 μs
X Multiply Time Word Size	100×10^{-6}	200×10^{-6}	1.5×10^{-3}	2×10^{-3}	1.5×10^{-1}
Power (watts)	3.5	7	30	200	X
C. Peripheral					
Tape Transport Transfer Rate	X	X	4×10^{6} b/s	X	X
Tape Transport Packing Density	X	X	1200 b/in.	X	X
Tape Transport Linear Speed	X	X	200 in./sec.	X	X
Paper Tape Reader	X	X	30,000 b/sec.	X	X
Paper Tape Punch	X	X	3,000 b/sec.	X	X
Card Reader	X	X	20,000 b/sec.	X	X
Card Punch	X	X	400 b/sec.	X	X

2. Physical Limitations

The speed of light is finite, about a thousand feet per microsecond. The speed of light is an upper bound to the speed of signal propagation, without there being any assurance that in any particular case the upper bound will be achieved. Thus, if one wishes to diminish the time between the origination of a signal at one location and the response to it by a receiving device at another location, only three means need be considered, these are:

1. Improve the speed of reaction of the receiving device to a received signal.

2. Improve the signal path in order that the speed of propagation along it is more nearly equal to the speed of light.

3. Diminish the length of path that the signal must follow.

While these means are not at all mutually exclusive, neither are they independent of one another.

A systematic effort to bring signal sources closer to signal destinations entails all of the problems of what is usually called miniaturization with perhaps a few new ones as well. For example:

1. Scaling size downward without diminishing signal energy eventually reaches a point at which one cannot supply adequate means for removing the generated heat.

2. Signal energies may not be reduced to arbitrarily low levels since signals would become lost in ambient noise, and eventually in thermal noise.

3. Signal currents may not be reduced to arbitrarily low values while maintaining speed of signal propagation since inter-element capacitance will always be present.

4. Signal voltages may not be reduced to arbitrarily
   low values while maintaining speed of signal
   propagation, since signal propagation paths will
   always have some inductance.

5. Signal voltages may not be reduced below certain
   specific values without foregoing useful present
   techniques, such as depending on the two thirds
   volt threshold of a silicon junction to reject
   noise below that value.

3. Summary

Figure E-II-2 shows a conventional, word oriented,
von Neuman computer which, from projected characteristics,
should be readily available in 1971.

Consideration of history suggests that in the future as
well as in the past there will be monumental discoveries, per-
haps with as much significance as had the invention of the
vacuum tube. It likewise suggests that the state-of-the-art
will be fluid in the future as in the past, but it also
suggests that the fluid is highly viscous, and the effect of
a monumental discovery will be to change the pattern of
viscous flow rather than to replace suddenly a body of tech-
nology. Here nature has provided a barrier to advancement in
limiting the rate at which people can exchange information
and acquire new skills.

INTERNAL MEMORY

ACCESS TIME — 300ns

CAPACITY 1.4×10^6 WORDS

TRANSFER RATE $> 15 \times 10^6$ BITS / SEC.

ARITHMETIC & CONTROL

ADD TIME — 700ns
MULTIPLY TIME $- <12$ us
POWER CONSUMPTION —
30 WATTS

MAX.
TRANSFER
RATE

COMMUNICATIONS
CONVERTER

T_1

T_n

DATA RATES
FROM 75 BITS/SEC.
TO 38,400 BITS/SEC.
NUMBER OF
TERMINALS
VERTUALLY
UNLIMITED

I/O BUS

DYNAMIC MEMORY

CAPACITY 100×10^6 WDS

ACCESS TIME - 900 us

TRANSFER RATE —
7.5×10^6 BITS/SEC

TAPE TRANSPORTS
1-10 per I/O
CHANNEL
PACKING DENSITY
1200 BITS/IN.
LINEAR SPEED
200 IN./SEC
STRT. STOP TIME $\sim$ 5ms

CATHODE RAY DISPLAYS
PAPER TAPE & CARD
READERS & PUNCHES,
LINE PRINTERS, &
OPTICAL SCANNER ALL
WITH CHARACTERISTICS
COMPARABLE WITH
DEVICES AVAILABLE
TODAY, ETC

Postulated Simple Von Neuman Machine - 1971
Figure E-II-2

APPENDIX E

ATTACHMENT III

ATTACHMENT III

Extrapolation Results

1. Introduction

    Contained in this section are a sampling of the projections
listed below in the order in which they are cited.

    A. Memory Characteristics

        1. Access time

        2. Cycle time

        3. Transfer rate (all memories)

        4. Transfer rate (memories exceeding 1,000 words)

        5. Maximum capacity

        6. Minimum cost (leading trends)

        7. Minimum cost (lagging trends)

        8. Maximum cost (leading trends)

        9. Maximum cost (lagging trends)

       10. Maximum capacity/cycle time (leading trends)

       11. Maximum capacity/cycle time (lagging trends)

       12. Transfer rate/maximum cost

       13. Maximum capacity x Transfer rate (leading trends)

       14. Maximum capacity x Transfer rate (lagging trends)

       15. Minimum capacity/minimum cost (leading trends)

       16. Minimum capacity/minimum cost (lagging trends)

B. Logic Characteristics

    1. Add time (leading trends)

    2. Add time (lagging trends)

    3. Multiply time

    4. Move 10 characters

    5. Compare - 3 way branch

    6. Multiply time/word size

    7. Arithmetic and control unit composite weight

    8. Arithmetic and control unit composite power
       consumption

C. Peripheral Characteristics

    1. Tape transport linear speed

    2. Tape transport packing density

    3. Tape transport transfer rate

    4. Dynamic memory access time

    5. Communication devices data rate

    6. Paper tape reader data rate

    7. Paper tape punch data rate

    8. Card reader data rate

    9. Card punch data rate

2. Sample Extrapolation Plots

Figure E-III-1
E-III-3

DATE OF FIRST INSTALLATION

.Y=.073, -00.54,   -Y=+050, -00.36,   +Y=+045, -00.36,

Figure E-111-2
E-III-4

CYCLE TIME vs DATE OF FIRST INSTALLATION

•Y=+071• ■00.55•   ■Y=+051• ⁻00.34•   +Y=+049• ⁻00.42•
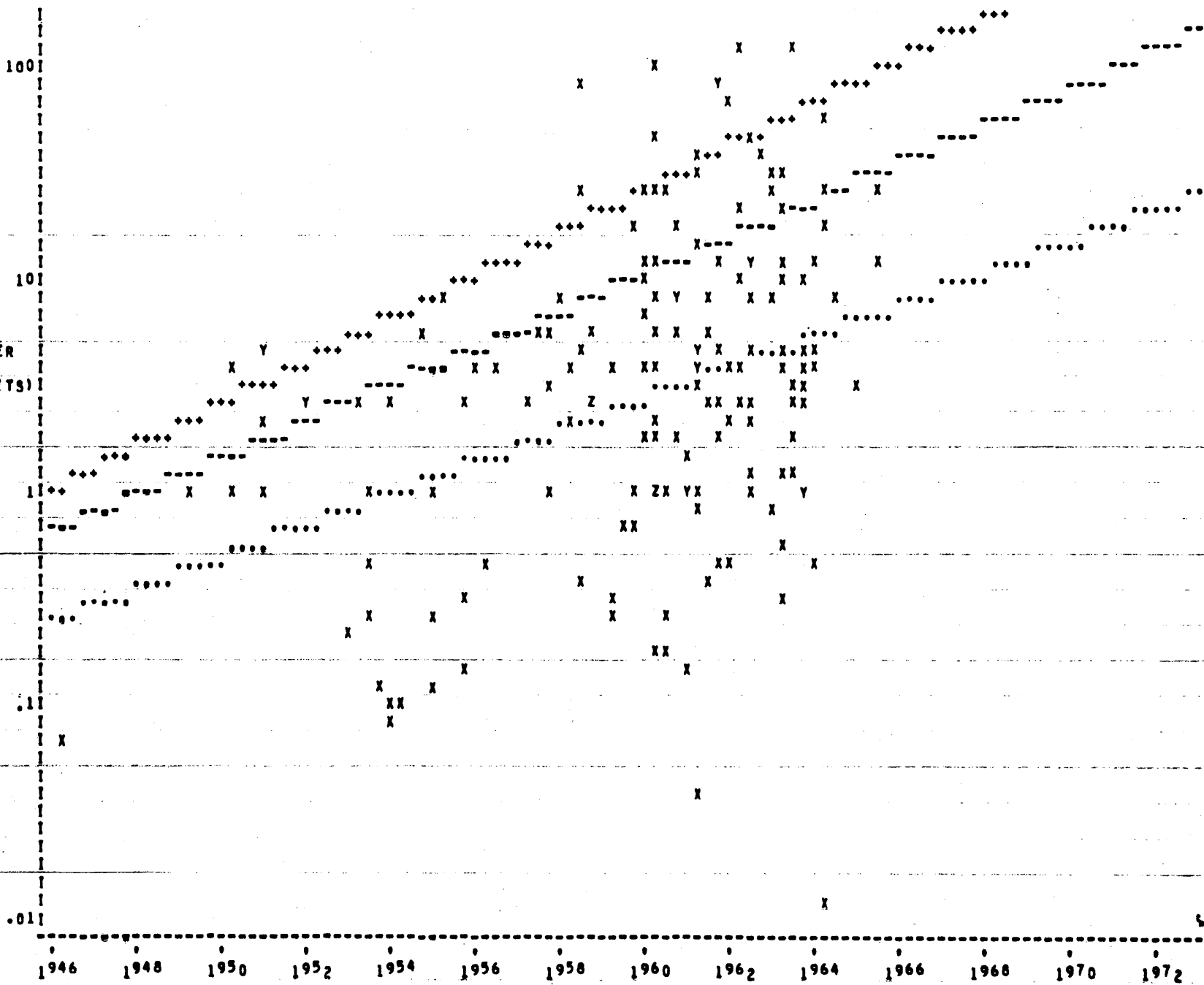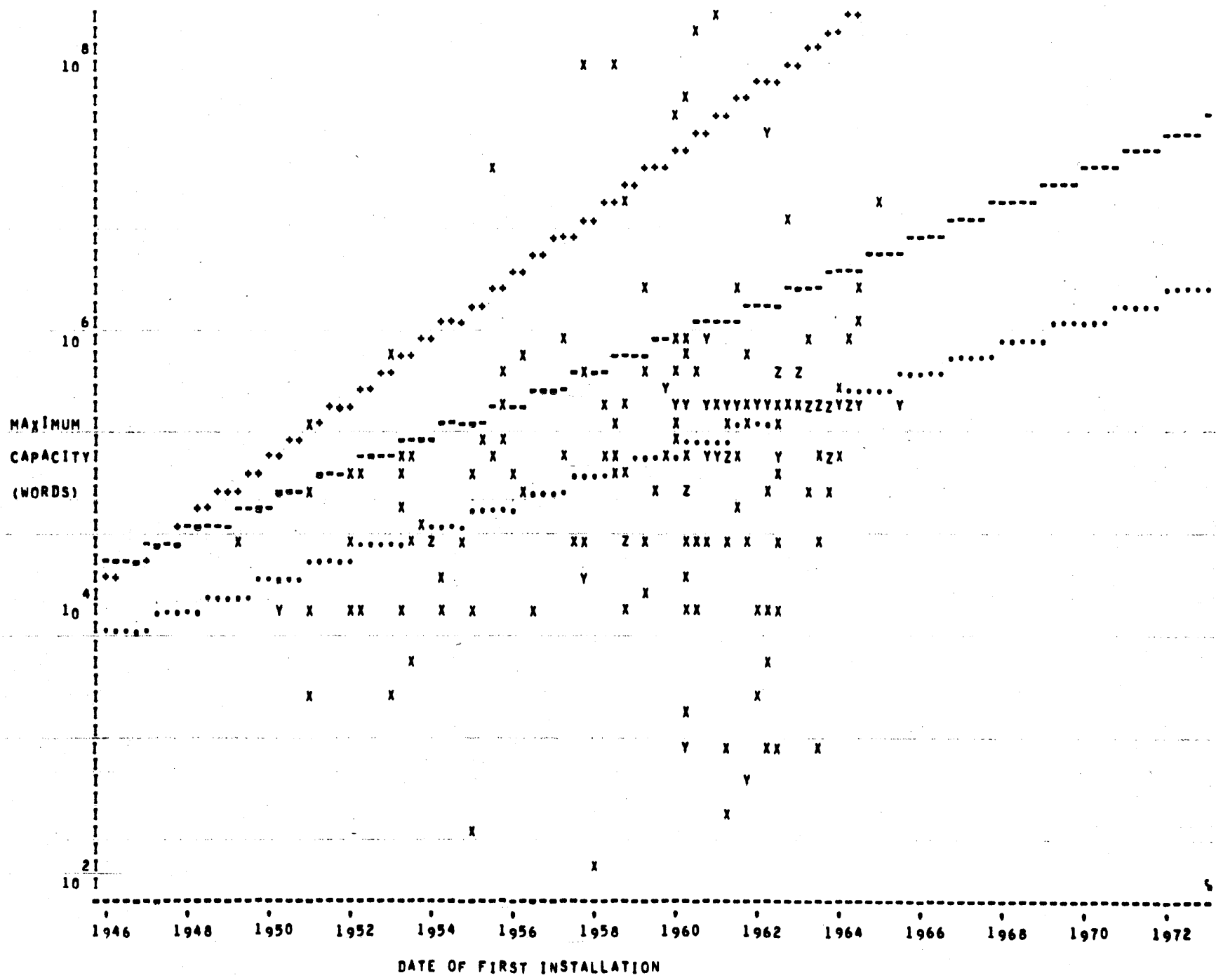
Figure E-III-3
E-III-5

Figure E-III-4
E-III-6

Figure E-III-5
E-III-7

Figure E-III-6
E-III-8

DATE OF FIRST INSTALLATION
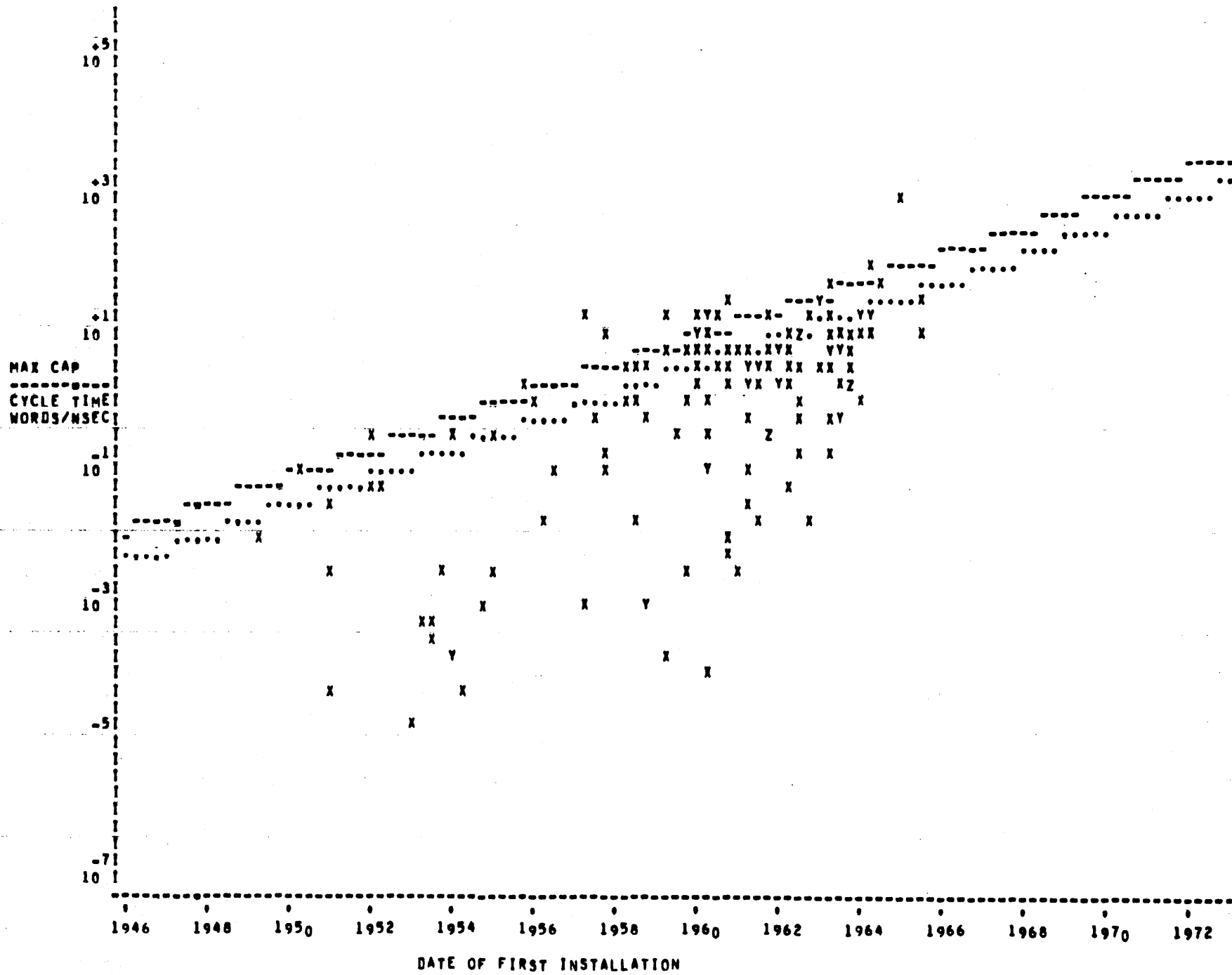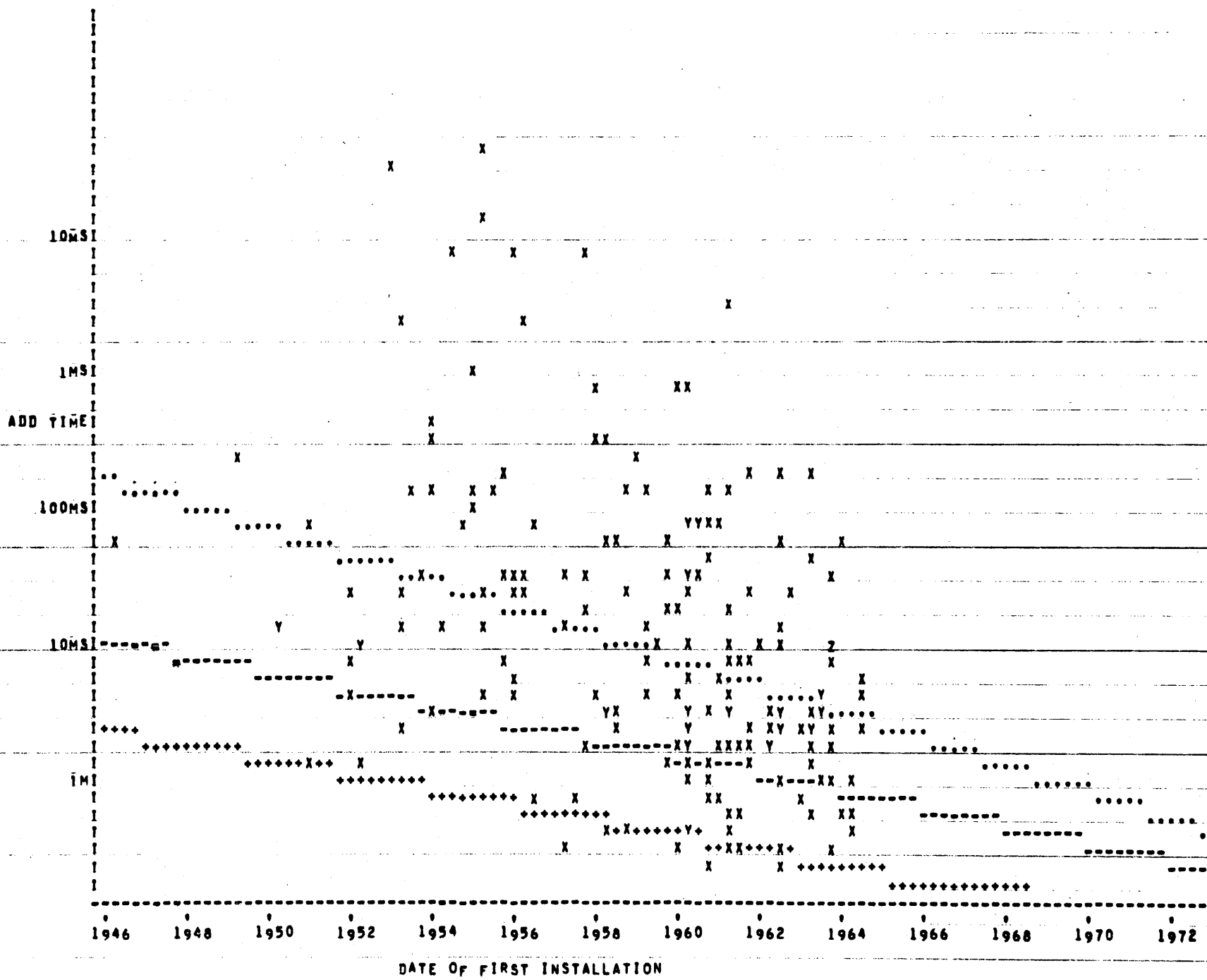
.Y=+048, -00.37,   -Y=+029, -00.24,   +Y=+018, -00.21,

Figure E-III-7
E-III-9

DATE OF FIRST INSTALLATION
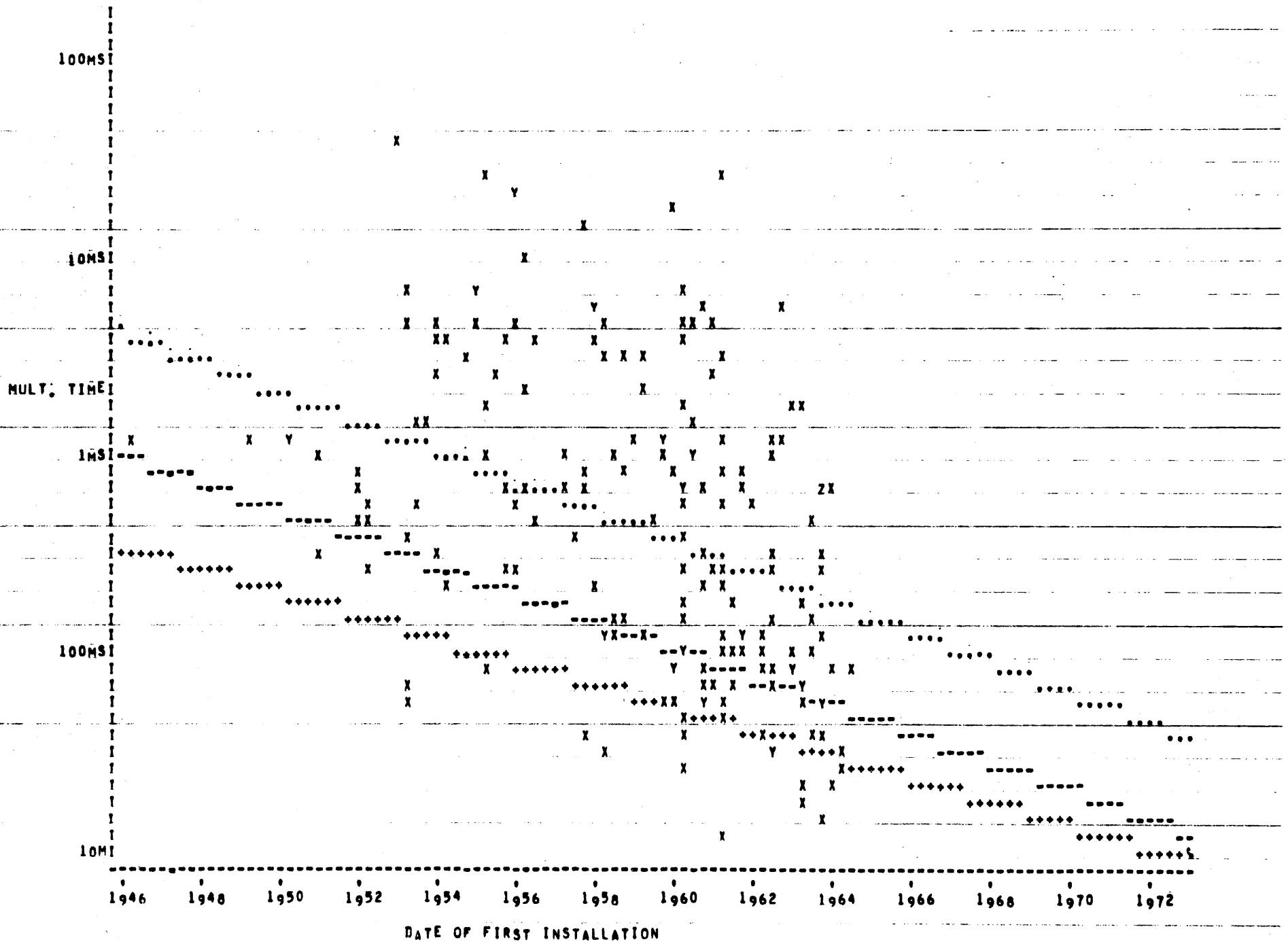
.Y=+064, -00.45,   -Y=+049, -00.41,   +Y=+037, -00.34,

100

POWER
(KW)
10

1

0.1

0.01

1946 1948 1950 1952 1954 1956 1958 1960 1962 1964 1966 1968 1970 1972

DATE OF FIRST INSTALLATION
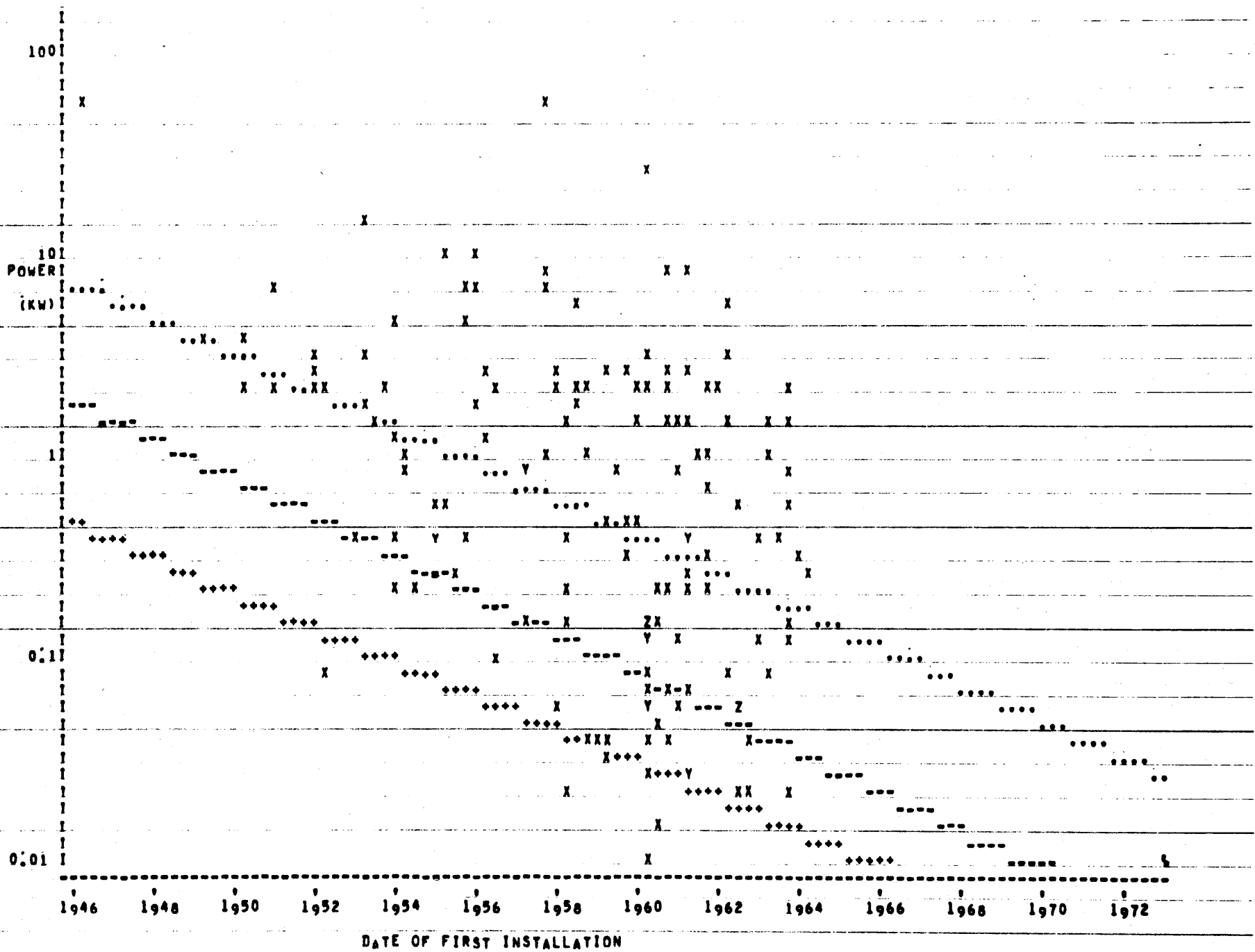
.Y=+069, -00.53,   -Y=+055, -00.57,   +Y=+040, -00.50,

APPENDIX E

ATTACHMENT IV

An Associative Processor for the Routing Problem

1. Introduction

The routing problem is encountered in a variety of systems including a store and forward communications system. In this case the best route (minimum delay, minimum cost, etc.) from a sending node to the receiving node in the network must be found. It is desirable that the routing problem be solvable in real time and that the computation be distributed throughout the network. That is, each node of network should have the capability of performing its own routing computation. Implications to the MILDATA problem of inter-nodal communications are obvious.

2. The Routine Algorithm

A routing algorithm called "distributed programming" has been proposed by Irv Cohen, Honeywell, St. Pete. This algorithm can best be described by an example using the network below.
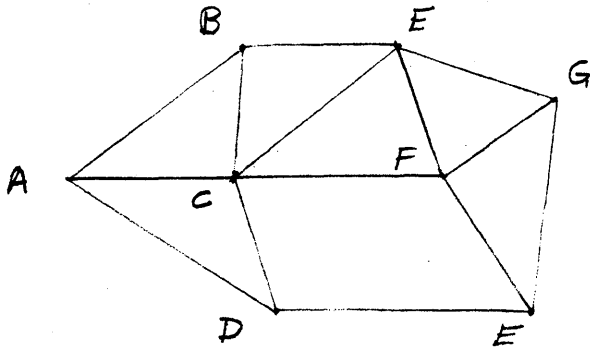
Assume for the moment that each of the nodes except A has determined its best path to every other node in the network, where the best path is the minimum delay path. Thus, each of these nodes has a routing table with an entry for every other node of the network. Included in each entry is the total delay from the node to each other node in the network. Assume also that the only delay information contained at node A is that along links AB,AC, and AD. However, by receiving the total delay portion of the routine table from each of its neighbors, B, C, and D, node A can compute its own minimum delay to each of the nodes of the network by using the equation

$$T_{Ak} = \min \quad t_{AB} + T_{Bk}, \quad t_{AC} + T_{Ck}, \quad t_{AD} + T_{Dk}$$

where t_{AB}, t_{AC}, t_{AD} = link delays from A to B, C and D, respectively

$T_{Ak}, T_{Bk}, T_{Ck}, T_{Dk}$ = minimum delay from A, B, C, and D, respectively, to node k

Node A can then identify the first link of the minimum delay path by noting which of its neighbors is part of the path.

In general terms the algorithm can be summarized as follows:

1. Each node receives a delay table from each of its neighbors. The delay table contains the minimum delay, T_{jk}, from that neighbor j to each node, k, of the network.

2. Using the T_{jk}'s received from its neighbors and its own link delays, t_{ij}, to each of its neighbors, each node i updates its own routing table by making the following computation:

$$T_{ik} = \min_{j} \quad t_{ij} + T_{jk}$$

The result of the computation is the minimum delay from the node i to the node k, T_{ik}, and the identity of the first link of the minimum delay path. With this information a given node will simply send an outgoing message to the proper nearest neighbor and let that neighbor route the message on to the destination.

3. The Associative Processor

The computation described above can be handled very effectively by using an associative processor, which is simply an associative memory with arithmetic capabilities. The organization of such a processor is illustrated in Figure E-IV-1.
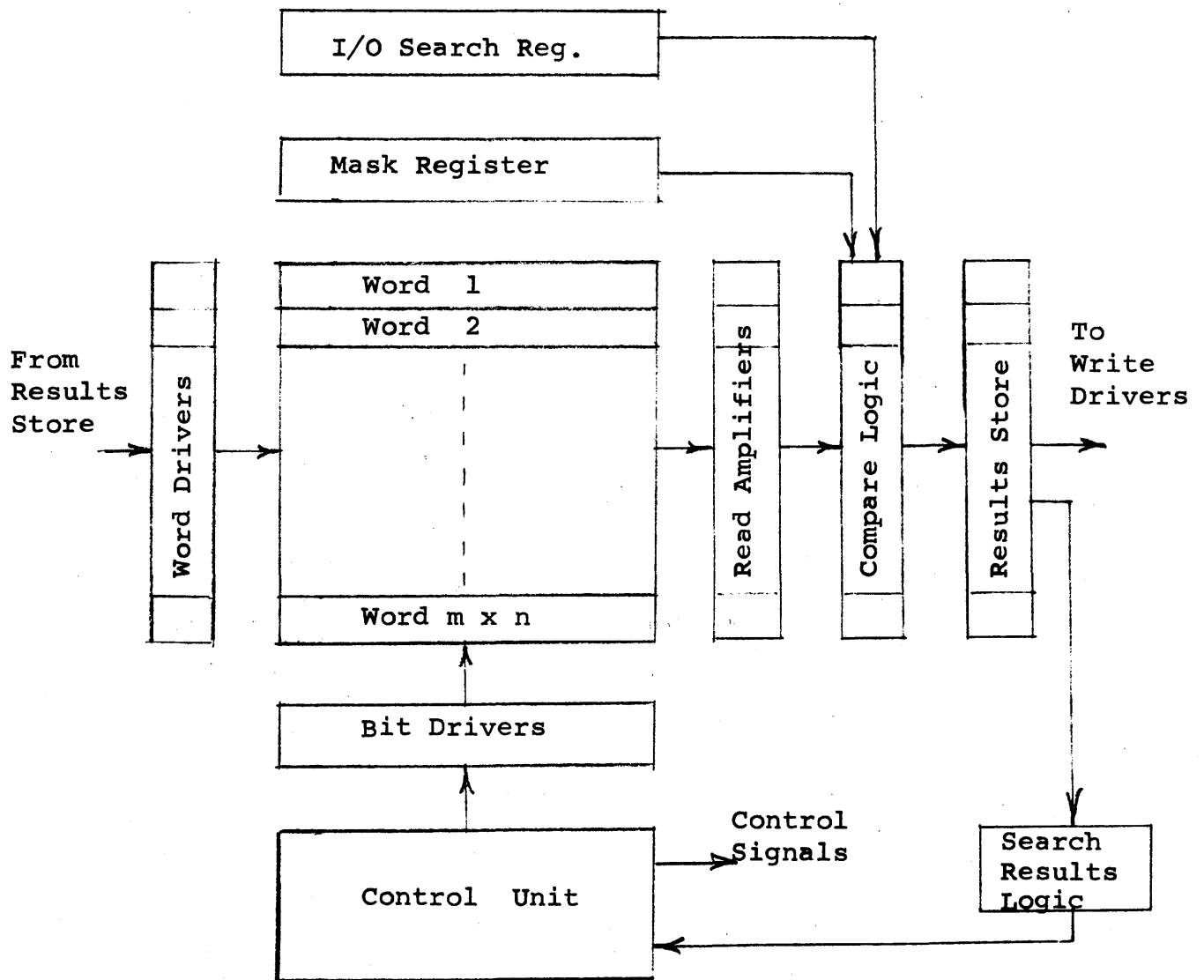
Figure E - IV - 1
Associative Memory With
Arithmetic Capability

The processor operates in a serial by bit, parallel by word mode for all operations. Readout of selected words of the memory is performed by energizing the bit drivers one bit at a time in whatever order desired. Writing is accomplished by again selecting a bit driver and by energizing word drivers depending on whether a 1 or a 0 is to be written in that word. In addition to the drivers, a read amplifier, compare logic, and search results store must be furnished for each word as indicated in Figure E-IV-1. Each compare logic will produce an output if the bit of the IO-Search register is the same as the bit being read out of that word.

Each associative processor must contain a number of words equal to the number of nodes in the network times the number of neighbors of that node;thus, if the network contains n nodes and each has m neighbors, m x n words or entries are required, each containing the following:

Identity of Neighbor, j	Identity of Destination, k	Minimum Delay to Destination, T_{jk}	Control Bits

The memory device normally used in an associative memory is a non-destructive readout type. This is necessary since the stored information is lost once it has been subjected to the compare operation (see Figure E-IV-1). A major disadvantage of present day non-destructive readout devices is the slow write time. This is particularly disturbing in this application since the arithmetic algorithm proposed uses a large amount of writing. While the clearest solution to this problem is a non-destructive readout device with a fast write time another solution is also available. This is to use a destructive read-out device in that portion of each word involved in the arith-metic operation, namely those parts used to store T_{jk} and the control bits. It turns out that for all the required operations on this portion of each entry, the information need not be saved after it is read out. Of course, the use of a destructive readout device in this manner will also require some memory development to find a destructive device and a non-destructive device with similar enough outputs that they can share the same sense amplifier. This solution also necessitates an additional signal from the word driver when the read operation is performed. This is an "inhibit read" signal for each word not involved in an arithmetic operation so that these words are not destroyed.

4. The Computational Procedure

Once the associative processor has been loaded, the computational procedure is as follows:

1. Do an __equality__ search on Identity of Neighbor of all entries to find those that came from neighbor 1.

2. Add t_{il}, the link delay from own node to neighbor 1, to T_{ik} of each of the entries tagged in step 1. Note that all add operations are performed in parallel.

3. Repeat steps 1 and 2 for each neighbor, then go to step 4.

4. To find the minimum delay path to a given node, do an __equality__ search on the Identity of Destination and a __minimum__ search on the Delay to Destination. The Identity of Neighbor of the selected entry identifies the first link of the minimum delay path.

5. To develop a complete routing table, perform step 4 for each node of the network and send the Identity of Destination and the Minimum Delay of Destination to each neighbor.

A summary of the procedure is as follows:

    m equality searches
    m add operations
    n combination equality - minimum searches

To obtain a rough estimate for the time required to accomplish the computation, assume a 200 nsec read time and 200 nsec write time. By using the algorithms described in Attachment V, the following operation times are determined:

    add time - 3.2 usec/bit
    equality search - 200 nsec/bit
    minimum search - 200 nsec/bit

By making further assumptions about word lengths and the size
of the network,

    n = 100 nodes
    m = 6 neighbors for each
    word length of T_{jk} = 10 bits
    word length of node identity = 7 bits

the following results are obtained

6 equality searches at 7 x 200 nsec	=	8.4	usec
6 add operations at 3.2 x 10 usec	=	192	usec
100 equality searches at 7 x 200 nsec	=	140	usec
100 minimum searches at 10 x 200 nsec	=	200	usec
total time		540.4	usec

This says that given the delay tables of each of its six neighbors
and given its own delays to each of these neighbors, a node can
determine the best route to each of the 100 other nodes in the
network in 540.4 usec.

Note that input/output operations have not been included in
the above estimate. It appears that the most convenient
organization of data for exchange of routing tables between the
nodes is as n-bit words containing the same bit of the delay to
the n nodes of the network. The search results store can then
be used for loading and unloading the memory, thereby reducing
the memory accesses required for these tasks and eliminating
extra drivers and read amplifiers required to load and unload
a word at a time.

5. Conclusions

The routing computation using the distributed programming
algorithm is an ideal application for an associative processor.
The associative capability is required to identify various sets
of entries in the memory and to find the minimum of other sets
of entries. The arithmetic requirement is such that an identical
operation is performed on a large number of operands, all of
which can be performed in parallel. While it is not clear at
this time that a requirement exists for this ultra-rapid routing
computation by itself, this application as one of many in a
distributed system such as MILDATA, highlights the advantages
of an associative systems capability.

APPENDIX E

ATTACHMENT V

ATTACHMENT V

An Associative Processor for Correlation Problems

1. Introduction

   A recent discussion has led to the examination of an
application of an associative processor to a correlation
problem. This problem is expected to be typical of a type
of problem present in military data processing systems, and
serves to show the value of an associative processor in the
MILDATA System currently being studied.

2. The Problem

   The problem is best described by the following equation,
which specifies logic operations within the parenthesis and
arithmetic operations between the parenthesis:

$$0_t = (W_1 \cap A_{t-199} \cup W_1' \cap A_{t-199}') + (W_2 \cap A_{t-198} \cup W_2' \cap A_{t-198}')$$

$$+ \text{-----} + (W_{200} \cap A_t \cup W_{200}' \cap A_t')$$

Where:

   0_t = the correlation coefficient

   $W_1,$ ---, W_{200} = weights which describe the reference
                    pattern (six bits each)

   A_t = present input (six bits)

   A_{t-1} = the input one time unit ago (six bits)

   A_{t-199} = the input 199 time units ago (six bits)

While the A's and W's are six bit numbers the logical operations
are bit - wise operations. Thus, the result of the logical
operation is a six bit number with "1's" in those bit positions

where A_i and W_i match and "0's" elsewhere. The arithmetic sum of these numbers, 0_t, is then an indication of the similarity between a 200 unit section of an incoming wave with a 200 segment reference. This will be compared with a threshold in order to determine when a certain waveform has been received.

The sampling rate of the incoming signal is 20 KC; that is, a new A_t is received every 50 usec.

3. Description of the Processor

An associative processor is defined here as an associative memory with certain additional features that give it the capability of doing arithmetic operations.

The associative processor capable of handling this problem is shown in Figure E-V-1. The processor is basically an associative memory of 200 words, 27 bits/word. The memory is organized in a bit serial, word parallel manner. For example, a read cycle would produce a selected bit of all words simultaneously. Thus, a 200 word, 27 bit/word associative memory organized this way is not unlike a 27 word, 200 bit/word random access memory. Writing is accomplished by selecting a bit driver corresponding to the bit to be written in all words. The information to be written in each word is furnished by the word driver as shown in Figure E-V-1. Also associated with each word of the memory is compare logic and a F/F. Each stage of compare logic will produce an output if the contents of F/F 1 (located directly above the compare logic in Figure E-V-1) is the same as the contents of the bit being read out of that word of the memory.

One significant difference between this application and more conventional applications of associative memories is the need for a large amount of writing. Thus, an element with a fast write capability is needed. For this reason a destructive readout memory element was given consideration. Thus, in those cases where the information is to be saved a write must follow each read. In this application the only time the information that is read out must be restored is in the case of the W's. One way of achieving this capability is to place a F/F between the read amplifier and the compare logic in Figure E-V-1 and

provide a path from each F/F to the corresponding write driver.
Note that the F/F must be inserted prior to the compare logic
because the information read out is lost at that point in an
equality search operation. Another approach is to use non-
destructive readout elements for storage of the W's since
writing into these positions is required only when the W's
change. This is the approach that has been chosen. Thus, in
the procedures that follow it is assumed that the W's are
stored in non-destructive readout memory elements and the
partial sums and control bits are stored in destructive read-
out elements.

Another somewhat special capability needed in this applica-
tion is the ability to select several bit drivers simultaneously
for writing. Since the information to be written is furnished
by the word driver, the effect is to write the same information
in several bits of each word. This capability is used to per-
form the logic in the addition equations discussed in the next
section.

4. Procedure

The associative processor is capable of performing the two
types of operations required in this problem - a bit-by-bit
equality comparison and an addition.

The equality comparison of A_t with each W is accomplished
by placing the ith bit of A in the F/F directly above the
compare logic in Figure E-V-1, and reading the ith bit of each
W stored in the memory. If the ith bit of W is the same as
the ith bit of A_t, a "1" will be placed in the corresponding
bit position of the Memory Register.

The addition can be performed by breaking it down to the
basic logic operations. Thus, $X + Y \rightarrow Z$ can be written as:

$$z_i = (x_i' \cap y_i' \cap c_i) \cup (x_i' \cap y_i \cap c_i') \cup (x_i \cap y_i' \cap c_i') \cup (x_i \cap y_i \cap c_i)$$

$$c_{i+1} = (c_i \cap x_i) \cup (c_i \cap y_i) \cup (x_i \cap y_i)$$

These equations are easier to perform if written in the
following form:

$$Z_i = \left[(X_i \cup Y_i \cup c_i')\underset{(1)}{\cap} (X_i \cup Y_i' \cup c_i)\underset{(2)}{\cap} (X_i' \cup Y_i \cup c_i)\underset{(3)}{\cap} (X_i' \cup Y_i' \cup c_i')\underset{(4)}{} \right]'$$

$$c_{i+1} = \left[(c_i' \cup x_i')\underset{(5)}{\cap} (c_i' \cup Y_i')\underset{(6)}{\cap} (x_i' \cup Y_i')\underset{(7)}{} \right]'$$

The number below each term in the equations above corresponds
to the control bit in the memory used to generate that term.
For instance, by storing the quantity X_i, Y_i, and C_i successively
in control bit 1, the term $X_i \cup Y_i \cup C_i$ is generated. Similarly
the other three terms in the Z equation are generated in
control bit 2, 3, and 4. The AND function of the four terms
of the Z equation is then generated by doing a search of control
bits 1, 2, 3, and 4 against 0000. This operation is effectively
an OR function of the complements; that is, if any of the four
is a 0, a 1 will be set in that position of the Memory Register.
The information in the Memory Register is then Z_i.

Given these two basic capabilities, the associative processor
can solve the correlation equation. Each word of the associative
processor will perform the bit-by-bit equality comparison of the
new input A_t with the weight stored in that word and will add
this result to the partial sum received from the word above.
The new partial sum is stored back into each word. Thus, the
contents of the partial sum portion of each word after each
computation cycle is:

word 1 - $(W_1 \cap A_t \cup W_1' \cap A_t')$

word 2 - $(W_1 \cap A_{t-1} \cup W_1' \cap A_{t-1}') + (W_2 \cap A_t \cup W_2' \cap A_t')$

word 200 - $(W_1 \cap A_{t-199} \cup W_1' \cap A_{t-199}') + (W_2 \cap A_{t-198} \cup W_2' \cap A_{t-198}')$

$+ \text{------} + (W_{200} \cap A_t \cup W_{200}' \cap A_t')$

Note that the quantity stored in word 200 is the desired result. It is read out to the output register during the next cycle.

The step-by-step procedure for $X + Y \longrightarrow Z$ is outlined below. Since A_t and the W's are six bit numbers, an X_i is generated only for the first six cycles. The addition must continue for eight more cycles, however, since the partial sum of 200 six bit numbers can grow to 14 bits. At the end of each cycle the carry C is left in the Memory Register for use during the next cycle. Thus, prior to the first cycle, the Memory Register must be cleared to give an initial carry-in of "0".

Procedure for Type A add cycle (First six cycles)

	No. of Reads	No. of Writes
1. Write C to control bits 2, 3		1
2. Complement		
3. Write C' to control bits 1, 4, 5, 6		1
4. Read Y_i	1	
5. Shift Memory Register down one		
6. Write Y_i to control bits 1, 3		1
7. Complement		
8. Write Y_i' to control bits 2, 4, 6, 7		1
9. Perform an equality comparison on the ith bit of A_t and the ith bit of W_{1_t} through W_{200}. Call the result X_i.	1	
10. Write X_i to control bits 1, 2		1
11. Complement		
12. Write X_i' to control bits 3, 4, 5, 7		1
13. Search control bits 1, 2, 3, 4	4	
14. Write Z_i		1
15. Search control bits 5, 6, 7	3	
totals	9	7

E-V-6

Procedure for type B add cycle (last eight cycles)

	No. of Reads	No. of Writes
1. Write C to control bits 2, 3		1
2. Complement		
3. Write C' to control bits 1, 4, 5, 6		1
4. Read Y_i	1	
5. Shift Memory Register down one		
6. Write Y_i to control bits 1, 3		1
7. Complement		
8. Write Y_i' to control bits 2, 4, 6, 7		1
9. Search control bits 1, 2, 3, 4	4	
10. Write Z_i		1
11. Search control bits 5, 6, 7	3	
totals	8	5

It can be seen that a Type B add cycle is the same as a Type A add cycle with steps 9, 10, 11, and 12 left out.

A time estimate for the add operation can now be made. Assuming that a read operation requires 200 nsec and a write operation requires 200 nsec, the following results can be obtained:

Time for a single Type A add cycle - 16 x 200 nsec = 3.2 usec
Time for a single Type B add cycle - 13 x 200 nsec = 2.6 usec
Time for 14 bit add
    6 type A add cycles - 6 x 3.2 = 19.2 usec
    8 type B add cycles - 8 x 2.6 = 20.8 usec
                                    40 usec

Since the input rate to the system is 20 KC, it can be seen that the speed requirement has been met.

5. Conclusions

The associative processor approach to this particular correlation problem can be recognized as a parallel-serial approach. Two hundred operations are performed in parallel, but each operation is performed in as serial a manner as possible to minimize the hardware. The other extreme in method of computation is a serial-parallel approach; that is, the two hundred operations are done sequencially but, each of these is done in as parallel a mode as possible to meet the speed requirement. There are, of course, combinations of these two approaches which would also be capable of meeting the requirements.

The significance of the approach described here is not that it is necessarily the best for this particular problem, but it shows that an associative memory, given certain characteristics, can be used effectively to perform arithmetic operations if the same operation is to be performed on a large number of operands.

An associative memory, in order that it be efficient for arithmetic operations must have:

1. A bit serial, word parallel organization; that is, read and write operations effect a selected bit of all words.

2. The ability to write the same information simultaneously in several bit positions of each word.

3. A fast write time since in such applications the number of writes required is about equal to the number of reads.

4. Local control to the extent that each word furnishes the information to be written in the selected bit position.

E-V-8
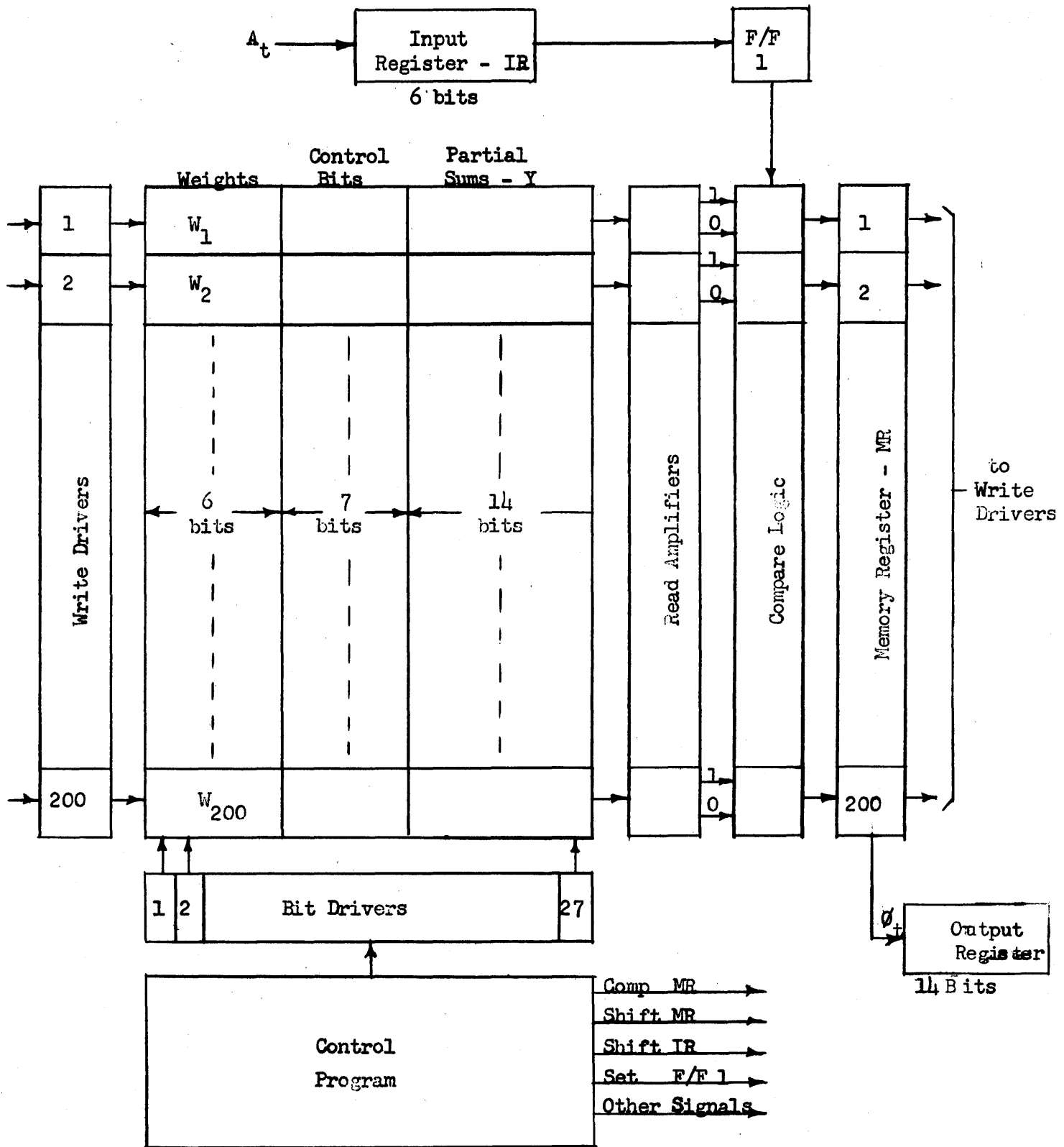
Figure E - V - 1

Associative Processor for the

Correlation Problem

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MILDATA Study by N. Nisenoff
Final Report   for 12 August - 30 September 1964
2v., incl. illus. and tables, April 15, 1965
(Contract No. DA 36-039-AMC-03275(E) Unclassified

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   Succintly, the proposed approach to the design of the MILDATA
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open-ended system; based upon the use of the most advanced
technology as extrapolated to the time frame of interest, in the
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Fundamentally the system's ability to provide the full range of
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interconnection of the MILDATA modules. These modules, which are
segmentable, perform the critical function of integrating and co-
ordinating the operation of the overall system. Once the Memory
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   This report serves to demonstrate the feasibility of this
approach. Recommendations concerning the implementation of this
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