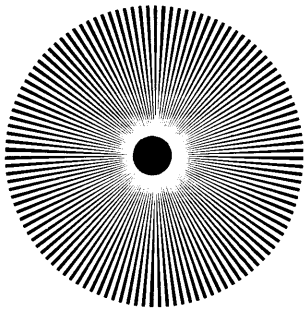

DATA-PAC

H 112 Series Instruction Manual

H 112 DIGITAL CONTROLLER

Central Processor Description

Volume I

Honeywell

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SECTION I
INTRODUCTION

The Honeywell H112 Digital Controller is a low cost processor which features high speed, efficient use of memory, and adaptability to a wide variety of on-line, real-time control, data collection, and data reduction applications. Honeywell has configured the H112 to meet the varied needs of control and systems engineers. It can be tailored to practically any application by the use of standard, off-the-shelf, plug-in modules. Memory is field expandable from 4K to 8K by use of a standard 4K plug-in module. The plug-in approach also allows a user to share one control panel among several H112 installations, by unplugging the panel once each unit is on-line.

SCOPE

This manual contains information which will enable maintenance personnel to troubleshoot and repair the H112 central processor. It is written with the assumption that the personnel are familiar with typical computer logic and state-of-the-art integrated circuit maintenance procedures. It makes no attempt to describe basic logic or circuit functions.

H112 CONTROLLER CHARACTERISTICS

Type – Parallel, binary, stored program

Addressing – Single-word addressing with single-level indirect addressing

Number System – Two's complement

Circuitry – Integrated, DTL

Instruction Complement – Five instruction types, making up 37 standard instructions; microprogrammable skip instructions

Word Length – 12 bits

Control Panel – Plug-in optional control panel, with facilities for display of A-, P-, or W-registers, as well as RUN/STOP, STORE, FETCH, START, and MASTER CLEAR functions, plus interlocks to prevent accidental entry

Input/Output Rate – One 12-bit word/3.39 μs, or 295K words/sec (Direct Data Channel Option)

Input/Output Bus – Party line with priority interrupt structure; optional bidirectional direct data channels (2)

Memory – Coincident current, random access, ferrite core, 12-bit word length; one or two 4K modules, field expandable to 8K

Memory cycle time – 1.69 μs

REFERENCES

Other publications which will assist maintenance personnel in servicing, installing, and operating the H112 Central Processor are listed below:

H112 Programmers Reference Manual, Doc. No. 70130072242, M-1164

H112 Interface and Installation Manual, Doc. No. 70130072243, M-1166

μ-PAC Integrated Circuit Modules, Vol. I, Doc. No. 130071369, M-135

H112 Central Processor Description, Vol. II, Doc. No. 70130072346, M-1421.

MACHINE INSTRUCTIONS

The various machine instructions used when programming the H112 are included in Table 1-1, following. Five groups of instructions make up the set, for a total of 37 words. All operation codes are in octal format.

ADDRESSING

Memory Organization

Each of the seven H112 memory reference instructions (LDA, STA, ADD, ANA, IRS, JMP, JST) contains a 7-bit address field. This allows 128 locations (0-177_8) to be directly referenced. As a

result, memory is divided into sectors of 128 words each. The sectors begin at addresses 0, 200_8, 400_8, 600_8, etc. A 4K H112 memory contains 32 sectors numbered 0-37_8; an 8K H112 memory contains 64 sectors numbered 0-77_8.

4K Memory Addressing

Each memory reference instruction contains a sector bit. This bit determines the sector in which the direct address is located. If the bit is ZERO, the direct address is located in a primary sector (sector 0 or 40_8); if the bit is ONE, the direct address is located in the same sector as the instruction.

Each memory reference instruction contains an indirect bit. If this bit is ZERO, the instruction operates on the contents of the direct address; i.e., the effective address equals the direct address. If the indirect bit is ONE, the instruction operates on the contents of the location specified by the direct address; i.e., the effective address equals the contents of the location specified by the direct address.

In a 4K machine, or when the bank bit in an 8K machine is ZERO, memory referencing occurs as shown in Table 1-2.

8K Memory Addressing

In an H112 with 8K memory, the bank bit is included in the calculation of the effective address. If the instruction is located in the lower 4K and the bank bit is ZERO, memory referencing occurs exactly as shown in Table 1-2. If the instruction is located in the upper 4K and the bank bit is ONE, memory referencing occurs in a manner similar to that shown in Table 1-2 except that 10000_8 (4096_{10}) is added to each address. For example, if the instruction location is 10204_8, the instruction address is 134_8, and the sector and indirect bits are both ONE (see example 3), then the effective address is all 12 bits at location 10334_8.

If the instruction is in the lower bank and the bank bit is ONE, all direct addresses are in the lower bank, but all indirect addresses are increased by 10000_8. Using example 3 under this condition, the instruction location is 204_8, the instruction address is 134_8, and the effective address is the contents of location 334_8 plus 10000_8. If 334_8 contains 1234_8, the effective address is 11234_8.

If the instruction is in the upper bank and the bank bit is ZERO, all direct addresses are in the upper bank, but all indirect addresses are in the lower bank. Again referring to example 3, the instruction location is 10204_8, the instruction address is 134_8, and the effective address is the contents of location 10334_8. If 10334_8 contains 1234_8, the effective address is 1234_8.

MAINTENANCE DRAWINGS

Maintenance drawings include Logic Block Diagrams (LBDs) and Flow and Timing Diagrams (FTDs). They are listed in Tables 1-3 and 1-4 respectively, and are given in Volume II of this manual.

TABLE 1-1.
MACHINE INSTRUCTIONS

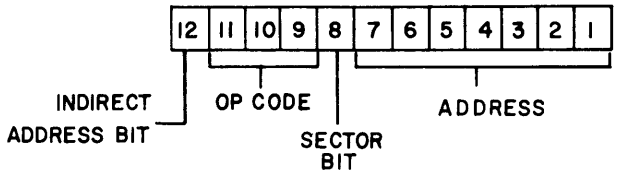
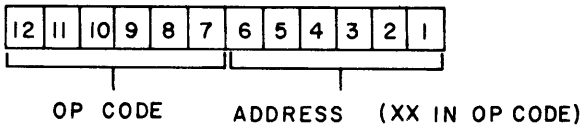
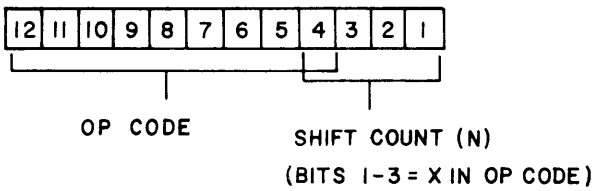
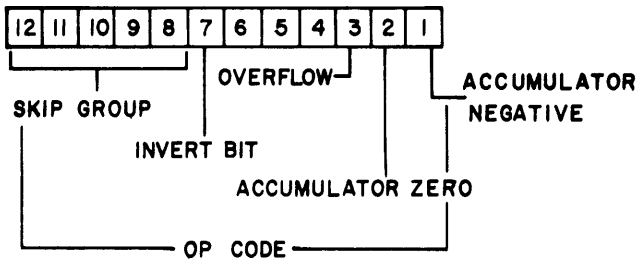
Op Code Octal	Mnemonic	Instruction	Execution Time (μs)
		Memory Reference Instruction:	
			
1	LDA	Load A (Direct)	3.39
	LDA*	Load A (Indirect)	5.09
2	STA	Store A (Direct)	3.39
	STA*	Store A (Indirect)	5.09
3	JMP	Jump (Direct)	3.39
	JMP*	Jump (Indirect)	5.09
4	ADD	Add (Direct)	7.63
	ADD*	Add (Indirect)	9.33
5	ANA	AND A (Direct)	7.63
	ANA*	AND A (Indirect)	9.33
6	IRS	Increment, Replace, and Skip (Direct)	9.33
	IRS*	Increment, Replace, and Skip (Indirect)	11.02
7	JST	Jump and Store P (Direct)	4.66
	JST*	Jump and Store P (Indirect)	6.36
		Input/Output Instructions:	
			
40XX	INA	Input Transfer to Accumulator	4.66
41XX	SKS	Skip if Set	4.66
42XX	OTA	Output Transfer from Accumulator	4.66
43XX	OCP	Output Control Pulse	4.66
4300 4301	SMK	Set Mask	4.66
		Shift Instructions:	
			
010X 011X	LGR	Logical Right Shift	3.4+N(0.424)

TABLE 1-1. (CONT)
MACHINE INSTRUCTIONS

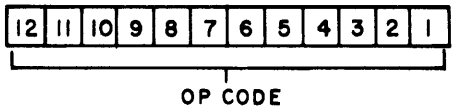
Op Code Octal	Mnemonic	Instruction	Execution Time (μs)
012X 013X	ARS	Arithmetic Right Shift	3.4+N(0.424)
014X 015X	RAR	Rotate A Right	3.4+N(0.424)

Skip Instructions:



0200	NOP	No Operation	3.39
0201	SMI	Skip if Accumulator is Minus	3.39
0202	SZE	Skip if Accumulator is ZERO	3.39
0203	SMZ	Skip if Minus or ZERO	3.39
0204	SOV	Skip if Overflow Flip-Flop is Set	3.39
0300	SKP	Skip Unconditionally	3.39
0301	SPL	Skip if Accumulator is Plus	3.39
0302	SNZ	Skip if Accumulator is Non-ZERO	3.39
0303	SPN	Skip if Positive and Non-ZERO	3.39
0304	SNO	Skip on no Overflow	3.39

Generic Instructions:



0000	HLT	Halt	2.54
0003	OCA	One's Complement Accumulator	7.63
0005	TCA	Two's Complement Accumulator	7.63
0021	STL	Stall On-Line	3.39+wait
0022	TBA	Transfer Bank Register to Accumulator	3.39
0024	ITS	Interrupt Save	3.39
0030	TOA	Transfer Overflow to Accumulator	3.39
0041	TAB	Transfer Accumulator to Bank Register	2.54
0042	ITR	Interrupt Return	2.54
0044	ENB	Enable Interrupts	2.54
0050	INH	Inhibit Interrupts	2.54
0060	CRA	Clear Accumulator	2.54

TABLE 1-2.
MEMORY REFERENCING IN 4K MODE

Example No.	Current Program Location$_8$	Address Assembled in Instruction$_8$ (7-bits)	[plus]	Sector Bit of:	[and]	Indirect Bit of:	[yields]	Effective Address$_8$ of:
1	204	134		1		0		334
2	204	134		0		0		134
3	204	134		1		1		(all 12 bits at location 334)
4	204	134		0		1		(all 12 bits at location 134)

TABLE 1-3.
LBD LIST

LBD No.	Title	Dwg. No.
12.00	Register Control	70 026 909
12.01	Register Bus Control (RB)	70 026 910
12.02	Timer (T)	70 026 911
12.03	Adder and Interrupt (AD,INT)	70 026 912
12.04	Shift Counter and Memory Load (C,L)	70 026 913
12.05	Decoder (D)	70 026 914
12.06	Program Counter (P)	70 026 915
12.07	Memory Address Register and Op Code Register (Y,F)	70 026 916
12.08	Working Register (W)	70 026 917
12.09	Accumulator (A)	70 026 918
12.10	Cable Data Bus and Register Transfer Bus (K,RB)	70 026 919
12.11	Cable Control Bus (K) and System Normalizer (N)	70 026 920
12.12	Expanded Address Option	70 026 921
12.13	CSM-160 Timing and Control	70 026 922
12.14	CSM-160 Timing and Control	70 026 923
12.15	CSM-160 Sense Amplifiers	70 026 924
12.16	CSM-160 Inhibit Drivers	70 026 925
12.17	CSM-160 X Selection Sinks and Switches	70 026 926
12.18	CSM-160 Y Selection Sinks and Switches	70 026 927
12.19	CSM-160 X and Y Selection Diode Matrix	70 026 928
12.20	Cable Chart	70 026 929
12.21	PAC Complement/Allocation	70 024 852
12.22	Control Panel Circuit Board A	70 026 930
12.23	Control Panel Circuit Board B	70 026 931

TABLE 1-4.
FTD LIST

FTD No.	Title	Dwg. No.
12.75	Fetch, Flow and Timing	70027847
12.76	Indirect Fetch, Panel Fetch/Store, Flow and Timing	70027848
12.77	LDA, STA, TOA, Flow and Timing	70027849
12.78	IRS, Flow and Timing	70027850
12.79	ADD and ANA, Flow and Timing	70027851
12.80	JMP, JST, Flow and Timing	70027852
12.81	OCA, TCA, RAR, LGR, ARS, Flow and Timing	70027853
12.82	INH, TAB, ITR, HLT, ENB, CRA, TBA, ITS, Flow and Timing	70027854
12.83	NOP, SMZ, SZE, SNZ, SMI, SPL, SOV, SNO, SKP, SPN, STL, Flow and Timing	70027855
12.84	INA, OTA, SKS, OCP, SMK, Flow and Timing	70027856
12.85	Load, Flow and Timing	70027857

SECTION II
BLOCK DIAGRAM DISCUSSION

The H112 Central Processor (CPU) contains a group of registers connected to a common register transfer bus and the control logic necessary to perform the required functions. The registers provide the temporary storage required to move data to and from the main memory storage, perform arithmetic operations on this data, control the program sequence, and control the execution of instructions.

Figure 2-1 contains a block diagram of the H112. This section of the manual will describe the functions of the major blocks and then provide a functional description of machine operation at the block diagram level.

TIMER (T)

The timer contains the master clock and time state generator which control CPU operations. The master clock is a free-running crystal-controlled oscillator that generates and distributes the clock pulses. The time state generator is essentially an 11-bit shift register that normally has only one flip-flop on at a time. Flip-flops 1 through 5 define the TF1 through TF5 times of the fetch cycle, and the remaining six flip-flops define the TE1 through TE6 times of the execute cycle. The time states and clock pulses are used with the various decoder outputs to generate the required control signals.

REGISTER TRANSFER BUS (RB)

The register transfer bus consists of 13 lines interconnecting the registers of the CPU. Capabilities for input transfers from the RB and output transfer to the RB are provided for both the accumulator and the working register. The shift counter, function register, and memory address register are capable of receiving data from the RB, while the program counter is capable of transferring data to the RB. The register bus control generates the transfer signals at the appropriate times to gate the data to the RB or into the appropriate register.

A typical example of a data transfer is as follows: the Register Bus From Program counter (RBFP) pulse gates the address stored in the program counter to the RB during TF1 time of a fetch cycle. Then the Register Bus To memorY address register Lower (RBTYL) gates bits 1 through 7 of the RB into bits 1 through 7 of the Y-register. The Register Bus To memorY address register Upper (RBTYU) gates bits 8 through 12 of the RB into bits 8 through 12 of the Y-register during TF1 time of a fetch cycle. Thus, the contents of the program counter have been transferred to the memory address register.

MEMORY (M)

The memory in the H112 is a 4096 x 12-bit, random-access, ferrite-core, coincident-current memory. Patterns are written into memory locations by using memory selection and inhibit drivers. Patterns are read from memory locations by using memory selection and sense amplifiers.

The address of the selected memory location is routed to the memory selection circuits from the Y-register. Data read from memory is loaded into the working register, and the data stored in the working register is written back into memory.

MEMORY ADDRESS REGISTER (Y)

The address register is a 12-bit (13 bits with the 8K memory option) parallel register that stores the address of the memory location to be accessed. The Y-register is loaded by a transfer from the register bus. Output lines from the Y-register are routed to the memory selection circuits and the program counter.

PROGRAM COUNTER (P)

The 12-bit (13 bits with the 8K memory option) program counter stores the address of the next

instruction to be executed. At the start of a fetch cycle, the address stored in the program counter is gated onto the register bus and transferred into the address register. Then, the program counter is incremented, conditioning it for the next instruction. The contents of the program counter are also changed by a transfer from the register bus through the Y-register. This occurs during JMP and JST instructions.

WORKING REGISTER (W)

The working register is a 12-bit parallel/serial shift register. Data words read from memory are loaded into the W-register, and data words to be written into memory are routed to memory via the W-register. The data on the register bus can be gated into the W-register, and data in the W-register can be gated onto the register bus. The W-register is also used to perform arithmetic operations on the stored data by shifting the data through the adder.

ACCUMULATOR (A)

The accumulator is a 12-bit parallel/serial shift register used as the primary arithmetic register of the CPU. Data stored in the accumulator is shifted into the adder with or without the W-register during arithmetic operations. The results of the arithmetic operations are returned to the accumulator. Gating logic associated with the accumulator allows data to be gated onto and off the register bus. The accumulator is also used to receive data from and route data to the I/O data bus via the register bus.

ADDER (AD)

The adder is a 1-bit element used in performing the arithmetic operation of the CPU. It performs the prescribed function on the bits shifted out of the A-register and/or the W-register and gates the results back into the A-register and/or the W-register. The following functions are performed by the adder: complementing numbers in the A-register, rotating numbers in the A-register, adding numbers in the A- and W-registers together, ANDing numbers in the A- and W-registers together, and incrementing numbers in the W-register.

In several of the preceding operations, a carry from the add of one bit position must be propagated and included in the add of the next bit position. This function is performed by the carry flip-flop (ADCRY). The carry flip-flop is set before an increment instruction (IRS or TCA), and reset before a rotate (RAR), complement (OCA), or logical add (ANA) instruction. This allows the overflow of an add operation to be tested (by an SOV instruction) or saved (by a TOA instruction) for multiple precision arithmetic.

SHIFT COUNTER (C)

The shift counter is a 4-bit counter used to count the number of shifts during a shift command and to control certain other operations (ADD, ANA, IRS, OCA, TCA, and Load Mode). During shifts the complement of the required number of right shifts is loaded into the shift counter via the register bus, and the counter is counted down. When the counter reaches all ZEROs, the instruction is terminated. When the counter is used for control of other functions, the appropriate count is detected.

FUNCTION REGISTER (F)

The function (Op Code) register is a 4-bit storage register which receives the Op Code portion of the instruction. During TF4 time of the fetch cycle, bits 9 through 12 of the instruction are gated onto the register bus and transferred into the F-register. The outputs from the F-register are routed to the decoder.

DECODER (D)

The decoder generates the various Op Codes depending upon the data stored in the F-register and/or the W-register. The Op Codes condition the various control gates which select the CPU operations.

BANK REGISTER (B)

The bank register is a 1-bit register used as the most significant bit of an indirect address word. It is also loaded with P13 during indirect JMP and indirect JST instructions. This register is supplied in the 8K version only.

Z-REGISTER (Z)

The Z-register is a 2-bit register used for intermediate storage during transfers between P13 and B01 and the accumulator. During an interrupt, Z is loaded with P13 and B01. During an interrupt return sequence, P13 and B01 are loaded from Z. This register is supplied in the 8K version only.

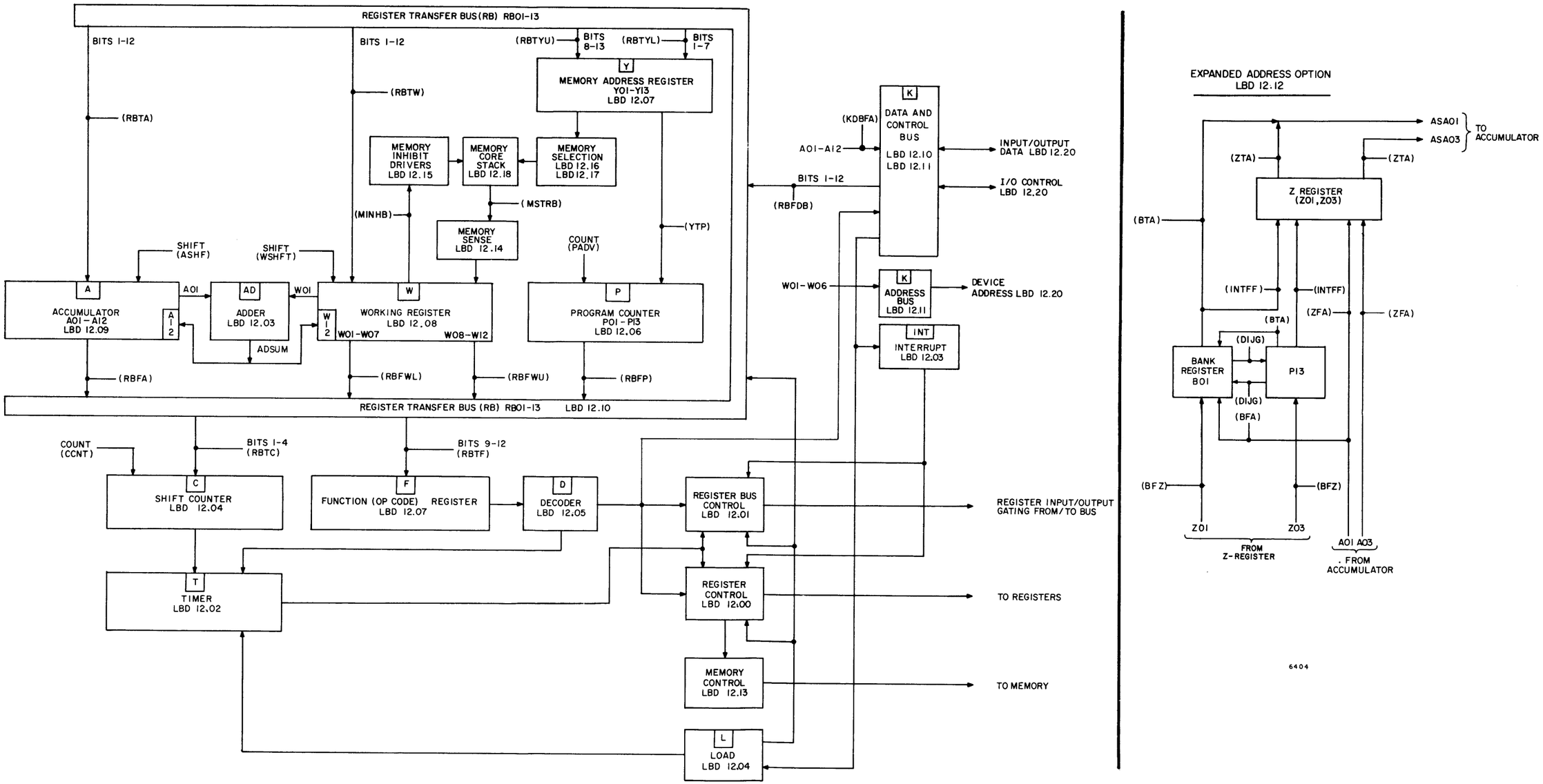


Figure 2-1. Block Diagram of Central Processor and Expanded Address Option

MACHINE OPERATION

From the time the CPU is started until it is stopped (by the STOP button or a HLT instruction), fetch and execute cycles are repeated one after another. During the fetch cycle, the instruction is read, the program counter is advanced by one, and the CPU is made ready to execute the instruction. At the end of the fetch cycle, the execute cycle is entered and the desired functions are performed. In this discussion, a typical machine operation is described, and operations during input/output instructions, interrupt conditions, and direct data channel operation are explained.

Instruction Fetch

A fetch cycle is performed to read the instruction out of memory. Each fetch cycle is divided into five time periods (TF1 through TF5) of 424 ns each. The fetch cycle is entered when the START switch on the panel is depressed or when the preceding instruction is completed. In TF1 time, the contents of the program counter (which identifies the address of the next instruction) are gated onto the register bus, and the data on the register bus are gated into the address (Y-) register. During TF2, the program counter is advanced by one and the memory cycle initiated. During TF3 time, the working register (W) is reset and the contents of the selected memory location are read and loaded into the W-register. Then the data in the W-register are used during the write portion of the memory cycle to restore the instruction in memory.

The contents of the W-register are gated onto the register bus during TF4 time. Bits 9 through 12 are gated into the function register (F), and the contents of the F-register are decoded to determine the function to be performed during the execute cycle.

During TF5, bits 1 through 7 of the W-register are gated into the Y-register via the register bus to identify the location addressed within the selected sector. Also in TF5 time, bit 8 of the W-register is sampled by the control logic to determine the selected sector. When bit 8 is a ONE, the selected sector is the same as the sector which was addressed during TF1. If bit 8 is a ZERO, the selected sector is a primary sector. Therefore, gating logic is enabled to gate all ZEROs into bits 8 through 12 of the Y-register.

The indirect address bit contained in bit 12 of the W-register is also sampled during TF5. The execute cycle is entered if bit 12 is a ZERO. The indirect addressing cycle is entered if bit 12 is a ONE and the instruction is a memory reference instruction.

Indirect Addressing

The indirect addressing cycle is enabled when a ONE is detected in bit 12 of the W-register during TF5 of the normal fetch cycle of a memory reference instruction. During the indirect cycle, a modified fetch cycle is performed. The fetch counter is started at TF2 time to prevent the reading of the P-counter into the Y-register. During TF2, the P advance pulse (PADV) is inhibited to prevent the incrementing of the P-counter. The address contained in the Y-register at the end of the normal fetch cycle is regarded as the address of a pointer. When the memory cycle is initiated during TF2 time, the data stored in this address are read into the W-register. The contents of bits 9 through 12 of the W-register are prevented from entering the F-register during TF4 time. During TF5 time, the contents of the W-register are gated onto the register bus and transferred into the Y-register. The new contents of the Y-register are used as the effective address during the following execute cycle. Single level indirect addressing only is provided. The indirect bit, therefore, is not examined again and an execute cycle will always follow the indirect cycle.

Instruction Execution

The operation prescribed by the contents of the F-register is performed during the execute cycle. The output signals from the decoder, along with the contents of the F-register and the timer outputs, generate the control signals required to perform the operations. During the execution of a non-memory reference instruction, the contents of the W-register along with the timer outputs are used to generate the required control signals.

Timing for the execute portion of an instruction is provided by a six-stage counter. The actual length of the execute cycle varies with the type of instruction under execution. An instruction requiring six execute timer pulses takes a total of 4.66 μs. Instructions which do not require the full six execute timer generate control signals that terminate the execute cycle in either TE1 or TE3 time and start the next fetch cycle. Some instructions require more than the 4.66 μs to perform

arithmetic operations. These instructions generate control signals which hold the execute counter in TE4 time and restart it at the proper time.

The following general operations are executed by the instructions: referencing memory, shifting through the adder for arithmetic and shift operations, changing the contents of the program counter to alter normal sequencing, transferring data between the accumulator and the I/O bus, performing control actions on registers, or operating condition flip-flops. Some instructions perform combinations of these basic operations to complete their required function.

Memory Reference (ADD, ANA, STA, LDA, IRS, JST).—Instructions which reference memory cause a memory read/restore or clear/write cycle to occur by enabling the Memory Cycle Initiate control function (MCI), and by setting or resetting the read control flip-flop (MREAD). The memory location accessed is determined by the Y-register which was loaded during the fetch cycle. The data is read into or written from the W-register. Therefore, the W-register must be loaded with the data to be written or cleared before receiving the read data.

The ADD, ANA, and LDA instructions cause a read cycle of memory. The STA and JST instructions cause a write cycle. The IRS instruction causes a read and then a write cycle to occur at the same memory address.

The JMP, while not a memory reference instruction, is usually included in this category because of the need to form a new effective address during the execution.

Arithmetic and Shift (ADD, ANA, IRS, ARS, LGR, RAR, OCA, TCA).—The arithmetic and shift instructions modify the accumulator (A) or a memory location by the prescribed action. In order to accomplish this function, the contents of the A-register or the W-register or the contents of both registers are shifted through the 1-bit adder. Bit 1 of each register feeds the adder, and the adder output feeds bit 12 of the A-register. (It also feeds the W-register during an IRS.)

Sequence Change (JMP, JST, SPL, SMI, SZE, SNZ, SOV, SNO, SPN, SMZ, SKP, IRS).—A sequence-changing instruction is executed to change the normal sequencing from one instruction to the next. This type of an instruction causes the program counter to be changed during the execute cycle.

The skip instructions (SPL, SMI, SZE, SNZ, SOV, SNO, SPN, SMZ, SKP, IRS) cause the program counter to be advanced by one if the indicated test condition is true (i.e., SPL skips the next instruction if the accumulator is plus). Otherwise, the program counter is not advanced.

During a jump instruction (JMP), the Y-register is loaded with the effective address to be accessed during the nex t fetch cycle. The program counter is then reset and the contents of the Y-register are gated into the program counter. The program continues from the new location.

During a jump and store instruction (JST), the Y-register is loaded with the effective address to be accessed during the next fetch cycle. When the execute cycle is started, the W-register is reset and the contents of the program counter are gated onto the register bus. The data on the register bus, which identify a memory location that is one greater than the location of the JST instruction, are gated into the W-register. The memory cycle is initiated and the contents of the W-register are stored in the memory location specified by the contents of the Y-register. The program counter is reset and the contents of the Y-register are gated into the program counter. The program counter is incremented by one, and the program continues from this new location.

I/O Control (OTA, INA, OCP, SKS, SMK).—The instructions in this group are used by the controller to communicate with peripheral devices. The address of the selected device, contained in bits 1 through 6 of the W-register, is routed to the peripheral devices via the address lines, and the I/O control signals are routed to the peripheral devices via the I/O control lines. Some instructions require the selected device to respond to the address and I/O control signals by a test signal from the device indicating that the device is ready. After the CPU detects the test signal (test line in the true condition) a strobe signal is routed to the device.

During an OTA instruction, the contents of the accumulator are gated onto the data bus and routed to the device. If the test line is true, the program counter is incremented by one to skip the next instruction, and a strobe signal is routed to

the device. The device uses the strobe signal to complete the transfer. If the test line is false during an OTA instruction, the program counter is not advanced and the next instruction is executed.

When an INA instruction is executed, the accumulator is cleared and the condition of the test line is checked. If the test line is true, the data on the data bus are gated into the accumulator via the register bus, the program counter is incremented by one, and the next instruction is skipped. The strobe signal then goes true, indicating that the data transfer is complete. If the test line is false during an INA, the A-register is cleared, the program counter is not advanced, and the next instruction is executed.

The SKS instruction is executed to check the condition of the test line from a specific device. If the test line is true, a pulse is issued on the strobe line and the program counter is incremented by one, causing the next instruction to be skipped.

During an OCP instruction, the address, control, and strobe signals are used to perform a function in the selected device irrespective of the condition of the test line. The program counter is not advanced by this instruction.

The SMK instruction is similar to an OCP instruction, except that the contents of the accumulator are used to set the interrupt mask flip-flops in the peripheral devices. Generally, one accumulator bit is assigned to each device. A ONE in an accumulator bit permits an interrupt, while a ZERO inhibits further interrupts and temporarily removes an interrupt request from a particular device. This instruction is not contingent upon the state of the test line and hence will never skip.

Run State Control (NOP, HLT, STL).—The NOP instruction performs no action. It is used to consume approximately 3.4 μs of time. Under some conditions, it is used as an instruction that is replaced by some other instruction.

The HLT instruction stops the CPU by resetting the run flip-flop in the timer. The START button must be depressed to restart the unit.

The STL instruction causes the CPU to stop performing instructions temporarily, until released from this condition by an external signal. The timer is held in state TE2 until the stall line (KSTAL) goes active (0V). The KSTAL line has no effect on processor operation until the STL instruction is executed.

Interrupt Control (ENB, INH).—The enable (ENB) and inhibit (INH) instructions set and reset, respectively, the interrupt control flip-flop. When an interrupt occurs, the interrupt control flip-flop is automatically reset. Therefore, an ENB instruction must be executed to re-enable the interrupt logic.

Accumulator Control (CRA, TOA).—The CRA instruction causes the accumulator to be cleared. When a TOA instruction is executed, the accumulator is cleared, the contents of the overflow flip-flop are transferred to bit 1 of the accumulator, and the overflow flip-flop is cleared (if in the set condition).

Expanded Address Option Instructions (TBA, TAB, ITS, ITR).—These instructions are used with the 8K memory option only and are treated as NOP or CRA instructions by the 4K version. During a TBA instruction, the accumulator is cleared, the contents of the bank register (B01) are transferred to bit 1 of the accumulator, and the contents of P13 are transferred to B01. The TAB instruction loads the contents of accumulator bit 1 into the bank register (B01).

When an interrupt occurs, the contents of the bank register are gated into Z01 and the contents of P13 into Z03. The ITS instruction will clear and transfer the contents of the Z-register into the accumulator. The contents of the accumulator can be stored to retain these conditions.

After the interrupt has been serviced, the contents of the bank register and P13 are restored. The previously saved data are loaded into the accumulator. The ITR instruction will clear and transfer the contents of the accumulator into the Z-register and precondition the interrupt return logic. During the next indirect JMP or indirect JST instruction, the contents of the Z-register will be transferred into P13 and the bank register.

Interrupts

An interrupt occurs when one of the devices on the I/O bus grounds the (KINTL) line. If interrupts have been enabled in the controller, the present instruction is completed and the instruction stored in dedicated location 00002 is then executed. Additional interrupts will be inhibited by this

action. This instruction must be a JST or indirect JST (JST*). The address of the next sequential instruction in the original program being run is stored in the memory cell at the effective address of the JST. The previous contents of the memory cell at this address are lost. In the 8K version the normal exchange of P13 and the bank register during an indirect JST is inhibited. Instead the contents of the bank register and P13 are transferred to the Z-register, and the bank register and P13 are cleared.

Direct Data Channel

When the DDC option makes a transfer request, instruction execution is temporarily suspended after the completion of the instruction in process. The Y-register is loaded with an address supplied by the direct data channel, and a memory cycle is initiated. An input or an output data transfer between memory and the channel takes place at this time, depending on the nature of the request. If a second request is made prior to the end of the present DDC cycle, another transfer occurs. If no request is waiting at the completion of the DDC cycle, instruction execution is resumed from the point of suspension with no alteration of programmable registers.

SECTION III
DETAILED THEORY OF OPERATION

This section describes the logic, timing, and functional operations of the H112. Each major functional block is described by use of the logic block diagrams (LBDs). The logic used to perform the fetch cycle is explained by use of both the LBDs and the flow and timing diagrams (FTDs). Instructions are grouped according to the operations performed during the execute cycle, and detailed descriptions of the different execute cycles are provided. In these descriptions, the term "passive" is used when a signal goes to +6V, and the term "active" is used when a signal goes to 0V. An assertion signal (e.g., TICYL+) is true if it is at +6V and false if it is at 0V, while a negation signal (e.g., TF5-) is true if it is at 0V and false if it is at +6V. Mnemonics are listed in Table 4-2.

REGISTER CONSTRUCTION

Five registers are used in the H112 processor, and the construction of each is discussed briefly in this section.

Memory Address Register (LBD 12.07)

The memory address (Y-) register in the basic H112 is a 12-bit parallel storage register with parallel transfer input gating. An additional bit is provided as Y13 (LBD 12.12) if the expanded address option is used. Data are transferred off the register bus and into the register in two parts. The information in bits 1 through 7 is transferred into the register by RBTYL+, and bits 8 through 13 are transferred into the register by RBTYU+, The dc set input of bit 2 (YSY02-) is used to select location 00002 during an interrupt routine.

Program Counter (LBD 12.06)

The program counter (P) is a 12-bit counter consisting of three CS-185 PACs. An additional bit is provided as P13 (LBD 12.12) if the expanded address option is used. The count stored in the counter is incremented by one each time PADV- goes true (0V), moving the counter to the next sequential address. The dc set inputs are used to load an address from the Y-register and change the normal counting sequence. The contents of P are available at the set outputs or can be gated onto the register bus via output gating logic enabled by RBFP-. P is cleared via the dc reset inputs of the flip-flops (PR-).

Accumulator (LBD 12.09)

The accumulator (A-register) is a 12-bit parallel/serial shift register consisting of two BR-320 Buffer Register PACs. The dc set inputs of the flip-flops are used for a parallel transfer of data from the register bus via input gating logic. Output gating logic is used to transfer the data at the set outputs of the flip-flops onto the register in a parallel fashion. Serial transfers are shift transfers, with new data from the adder (ADSUM) entering bit 12. Resetting the accumulator is accomplished via the dc reset inputs of the flip-flops (AR-).

Working Register (LBD 12.08)

The working (W-) register is a 12-bit parallel/serial shift register similar to the accumulator. The two BR-335 Buffer Register PACs and the control logic are connected to allow parallel input and output transfers via the register bus. The dc set inputs are also used to accept the data from the sense amplifiers of the memory during a memory read cycle. Output gating from the W-register is accomplished in two parts. Bits 8 through 12 are gated by RBFWU+, and bits 1 through 7 are gated by RBFWL+.

Function (Op Code) Register (LBD 12.07)

The function register (F) is a 4-bit parallel storage register which stores bits 9 through 12 of the instruction. Data on bits 9 through 12 of the register bus are transferred into the F-register at

the end of TF4 time and remain in the register until the fetch cycle of the next instruction. The contents of the F-register are directly taken from the outputs of the flip-flops and are used in the decoder. When data is loaded in the load mode, XLDSW- is applied to the dc set input of F10, generating an STA Op Code.

TIMER (LBD 12.02)

The time states required to control the CPU operations are generated in the timer. An 11-stage shift register and the necessary control logic generate 5 fetch times (TF1 through TF5) and 6 execute times (TE1 through TE6). Normally, only one time state is on at a time. The functions performed by the fetch time states are the same for all instructions, while the functions performed by the execute time states depend on which instruction was fetched.

The master clock PAC (A21A) generates and distributes the clock pulses (TCLK). TCLK+ remains active (0V) for 0.270 μs and passive (+6V) for 0.154 μs. The run logic receives signal XSRT+ from the START switch on the control panel, XXSRT+ from the START switch on the remote panel (if used), and a common line (XSRT-) from both switches. The level at A15C-25 goes passive (+6V) when one of the switches is depressed and active (0V) when the switch is released. Gates A23A and A23B are used to eliminate switch bounce. If the TRUN flip-flop is reset, the negative-going transition at A15C-25 enables the run condition by setting TRUN. TRUN- is inverted by A15G-29, enabling the set input of the TF1 flip-flop (A18A-26). The TF1 flip-flop is set when the next TCLK+ goes from the passive (+6V) to the active (0V) state and remains set for 0.424 μs. During this time, signals TF1+ and TF1- are used to condition CPU control logic (e.g., gate B34E on LBD 12.01). Gate B21K disables the set input to the TF1 flip-flop until the CPU is ready to enter the next fetch cycle (B21K-32 goes active – 0V). A23H and B26E form a flip-flop (TRUNS) which is used for synchronization on starting.

The TF1- signal is inverted by B15G-25, and the resultant signal conditions the set input to the TF2 flip-flop (the input to B15G-23 is explained in the indirect cycle discussion). Flip-flop TF2 is set by the trailing edge of the next TCLK+ pulse, and TF2 time is entered. Every 0.424 μs the fetch time is set and the previous fetch time reset until the end of TF4.

The contents of bits 9 through 12 of the W-register are checked for the memory reference indirect cycle (A17E and A15L). If the instruction uses indirect addressing, A15L-26 goes passive (+6V), conditioning the set input to the TICYL flip-flop and the input to A17D-3. When the TF5 flip-flop is set, A17D-11 goes active (0V), conditioning the set input to the TF2 flip-flop. At the same time, the output at B15C-13 goes active (0V), inhibiting the set input to the TE1 flip-flop. At the end of TF5 time, the TICYL flip-flop is set, the TF2 flip-flop is enabled, and the timer re-enters the fetch cycle at TF2.

During the first TF5 time if indirect addressing is not used, or during the second TF5 time if indirect addressing is used, the set input to the TE1 is conditioned. Then the next TCLK+ pulse following the appropriate TF5 time sets the TE1 flip-flop, and the execute cycle is entered. The length of the execute cycle depends on the type of instruction. It can be terminated at the end of TE1, TE3, or TE6 time. It can also be stalled in TE2 time or held in TE4 time.

The execute cycle is terminated and the next fetch cycle is started by the TSF1 signal. TSF1 can be generated in seven different ways, which will be explained later. To terminate the execute cycle at the end of TE1 time, TSF1- is used to inhibit the set input of the TE2 flip-flop, and TSF1+ is used to enable the set input of the TF1 flip-flop. Then the TCLK+ pulse at the end of TE1 time resets the TE1 flip-flop and sets the TF1 flip-flop. The execute cycle is terminated at the end of TE3 time in a similar manner, except that the TE4 flip-flop is inhibited.

Operations during a stall (STL) instruction are slightly different. During this instruction, the CPU is held in TE2 time until the STALN- signal goes active (0V). The output at A13G-25 prevents the setting of the TE3 flip-flop, and the output at A17H-26 prevents the resetting of the TE2 flip-flop. When STALN- goes active (0V), the set input to TE3 is enabled and the next TCLK+ pulse sets the TE3 flip-flop. The second TCLK+ pulse resets both TE2 and TE3 flip-flops, and the remainder of the operation is the same.

During instructions which require shifting operations, the CEE4+ signal goes active (0V), inhibiting the reset side of the TE4 flip-flop and the set sides of the TE5 and TF1 flip-flops. At the same time, the output from B17B-20 goes active, generating

TSF1-. After the required shift operations are performed, the CEE4+ signal goes passive (+6V), enabling the above listed flip-flop inputs. The next TCLK+ pulse resets the TE4 flip-flop and sets the TE5 and TF1 flip-flops. In this case, the next fetch instruction is started before the execute cycle is completed.

Instructions are performed in sequence until a halt (HLT) instruction is received, the STOP switch on either panel is depressed, or one of the various stop conditions is detected. Under these conditions the TSTOP- signal goes active, resetting the TRUN flip-flop. The remainder of the instruction is completed, but the output from A15G-29 goes active (0V), inhibiting the set input to the TF1 flip-flop. The timer remains in this condition until the START switch on either panel is depressed and operations are resumed.

INSTRUCTION FETCH (See Tables 3-3, 3-4)

Fetch With Direct Addressing (See FTD 12.75)

The fetch cycle is entered when the TF1 flip-flop in the timer is set. The Register Bus From P-counter (RBFP-) (LBD 12.01) goes active (0V) during TF1 if there is no interrupt waiting to be serviced (INTFF-A is passive: +6V). The output gates of the program counter (LBD 12.06) are enabled by RBFP-, and the address in P is gated onto the register bus. The data on the register bus are allowed to settle and the transfer gates of the Y-register (LBD 12.07) are conditioned. Near the end of the TF1 state, TCLK+B goes passive, generating the Register Bus To Y-register Upper and Lower signals (RBTYU+ and RBTYL+) (LBD 12.01). The trailing edge of RBTYU+ and RBTYL+ transfers the address on the register bus into the Y-register.

During TF2 time, memory control signals required for the read/regenerate mode are generated and routed to the memory (see LBD 12.00). When the TF2 flip-flop is set, MREAD+A goes passive (+6V), indicating that the memory location whose address is in the Y-register will be read. The address logic in memory is reset by MARP-A, which is active (0V) from the start of TF2 to the setting of the Memory Cycle Initiate (MCI) flip-flop. When MARP-A goes passive (+6V), the address in the Y-register is valid in the memory address logic.

At the start of TF2, MCILC+ goes passive (+6V), conditioning the set side of the MCI flip-flop. The leading edge of TCLK-, which occurs near the middle of TF2, sets the MCI flip-flop, initiating the memory cycle. The program counter is incremented by PADV-, which is generated by B22E (LBD 12.00).

The memory cycle continues during TF3 time, with the read cycle being performed first. WR-, which clears the W-register, goes active (0V) at the start of TF3 and passive (+6V) when TCLK- goes active (0V). The read cycle is completed, and the instruction in the addressed memory location is strobed onto the dc set lines (MSW01- through MSW12-) of the W-register (LBD 12.08). The contents of the W-register are used during a memory write cycle to restore the instruction in the addressed memory location.

At the start of TF4, bits 8 through 12 of the W-register are copied onto the register bus by the Register Bus From W-register Upper signal (RBFWU+) (LBD 12.01). After the lines are allowed to settle, the Op Code portion of the instruction (bits 9 through 12) is transferred into the F-register by the negative-going edge of the Register Bus To Function (Op Code) register signal (RBTF+) at the end of TE4.

The functions performed during TF5 depend on the mode of address and the condition of the sector bit (bit 8 in the W-register). Direct addressing is described in this section, indirect addressing in the next. The logic described is contained on LBD 12.01.

Irrespective of other conditions, bits 1 through 7 of the W-register are gated onto the register bus when TF5- goes active (0V), causing the Register Bus From W-register Lower signal (RBFWL+) to go passive (+6V). The contents of these 7 bits identify a location within a sector of memory. When TCLK+B goes passive (+6V), RBTYL+ is generated and its trailing edge transfers the address into bits 1 through 7 of the Y-register.

Bit 8 of the W-register is sampled to determine the sector of memory being addressed. If the primary sector (sector 0 or 32) is addressed, W08+ is active (0V), conditioning B24B-24. In this case, TCLK+B goes passive (+6V), which enables the gate and generates RBTYU+. Since bits 8 through 12 of the register bus contain ZEROs, the trailing edge of RBTYU+ transfers ZEROs into bits 8 through 12 of the Y-register. Under these conditions, the

addressed location is one of the 128 addresses in sector 0 or sector 32.

If the addressed location is in the same sector as the instruction, bits 8 through 12 of the Y-register must remain unchanged. To accomplish this function, W08+ must be passive (+6V), causing B24-16 to go active (0V). In this case, gate B24B is inhibited, RBTYU+ is not generated, and the upper 5 bits of the address remain the same.

At the end of TF5, the execute cycle is started if direct addressing is used, or the extended fetch cycle is entered if indirect addressing is used.

Fetch With Indirect Addressing (See FTD 12.76)

The indirect addressing mode is activated at the end of TF5 time if bit 12 of a memory reference instruction is set (LBD 12.02). Under these conditions, the set inputs to the TF2 and TICYL flip-flops are enabled, the set input to the TE1 flip-flop is disabled, and the reset input to the TF5 flip-flop is enabled. The trailing edge of TCLK+A resets the TF5 flip-flop and sets the TF2 flip-flop. When TF5+ goes false, the TICYL flip-flop is set, and the indirect fetch cycle is entered at TF2 time.

To prevent the incrementing of the program counter, TICYL- inhibits gate B22E (LBD 12.00) during TF2 of the indirect fetch cycle. MREAD+A and MARP-A are generated and used to condition the memory for a read/regenerate mode. The next TCLK- pulse sets the MCI flip-flop, and the memory read cycle is initiated. The address in the Y-register (loaded during the preceding TF5 time) is regarded as the address of a pointer. The W-register is cleared when TF3- goes true (0V). The contents of the addressed memory location are then read and strobed onto the dc set lines of the W-register.

The F-register, which contains the Op Code of the instruction, must not be changed during the indirect fetch cycle. Therefore, TICYL- disables gate C27C (LBD 12.01), inhibiting the generation of RBFWU+ and RBTF+ during TF4 of the indirect fetch cycle.

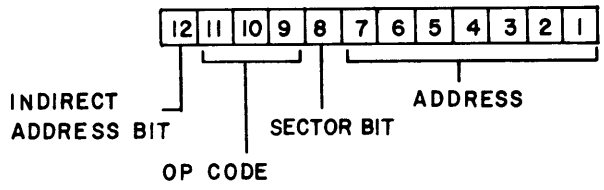
At this time, the W-register contains the address of the memory location to be referenced, and this data has to be transferred to the Y-register. To perform this function, TICYL+ conditions gate C32G. RBFWU+ and RBFWL+ are generated, gating the contents of the W-register onto the register bus while TF5+ is true (+6V). TICYL- causes B24A-16 to go passive (+6V), conditioning gate B24B. RBTYU+ and RBTYL+ are then generated by TCLK+B. When TCLK+B goes false (0V), the trailing edges of RBTYU+ and RBTYL+ transfer the data on the register bus into the Y-register. The new contents of the Y-register are used as the effective address during the execute cycle.

INSTRUCTION DECODING

The H112 instruction repertoire contains five basic instruction groups. Bit patterns of the instructions are decoded to obtain the control signals required to perform the desired functions. The major portion of the decoding logic is contained on LBD 12.05. Additional decoding appears on the other LBDs. The most efficient use of the decoding logic is obtained by decoding different bit combinations and using the decoded signals wherever they are applicable. Where this technique is impractical, the Op Code of a specific instruction is decoded (e.g., DIRS for an IRS instruction). Table 3-1 groups the instructions and lists the bit patterns used in decoding.

Memory Reference Group Decoding

The instruction word format for a memory reference instruction is as follows:



Bits 9 through 12 of the instruction are transferred into the F-register during TF4 time, and the contents of the F-register remain unchanged until TF4 time of the next instruction. An Op Code of three bits allows a maximum of seven instructions in the memory reference group plus an all-ZERO combination for all non-memory reference instructions. The decoding of these instructions is shown throughout the LBDs and will be explained in the discussion of the specific instructions.

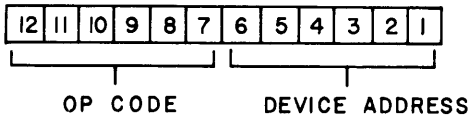
The JMP instruction, though not a true memory reference instruction, is included in this group for decoding convenience only. The indirect address bit, also contained in the F-register, is used to extend the fetch cycle during the execution of an indirect instruction in this group.

TABLE 3-1.
INSTRUCTION CODING

Group	Mnemonic	Instruction	12	11	10	9	8	7	6	5	4	3	2	1
Memory Reference	LDA	Load A	X	0	0	1	X	X	X	X	X	X	X	X
	STA	Store A	X	0	1	0	X	X	X	X	X	X	X	X
	JMP	Jump	X	0	1	1	X	X	X	X	X	X	X	X
	ADD	Add	X	1	0	0	X	X	X	X	X	X	X	X
	ANA	AND A	X	1	0	1	X	X	X	X	X	X	X	X
	IRS	Increment, Replace, and Skip	X	1	1	0	X	X	X	X	X	X	X	X
	JST	Jump and Store P	X	1	1	1	X	X	X	X	X	X	X	X
Input/Output	OTA	Output Transfer from A	1	0	0	0	1	0	X	X	X	X	X	X
	INA	Input Transfer to A	1	0	0	0	0	0	X	X	X	X	X	X
	SKS	Skip if Set	1	0	0	0	0	1	X	X	X	X	X	X
	OCP	Output Control Pulse	1	0	0	0	1	1	X	X	X	X	X	X
	SMK	Set Mask SMK00	1	0	0	0	1	1	0	0	0	0	0	0
	SMK	Set Mask SMK01	1	0	0	0	1	1	0	0	0	0	0	1
Shift	LGR	Logical Right Shift	0	0	0	0	0	1	0	0	X	X	X	X
	ARS	Arithmetic Right Shift	0	0	0	0	0	1	0	1	X	X	X	X
	RAR	Rotate A Right	0	0	0	0	0	1	1	0	X	X	X	X
Generic	CRA	Clear A	0	0	0	0	0	0	1	1	0	0	0	0
	OCA	One's Complement A	0	0	0	0	0	0	0	0	0	0	1	1
	TCA	Two's Complement A	0	0	0	0	0	0	0	0	0	1	0	1
	TOA	Transfer Overflow to A	0	0	0	0	0	0	0	1	1	0	0	0
	ENB	Enable Interrupt	0	0	0	0	0	0	1	0	0	1	0	0
	INH	Inhibit Interrupt	0	0	0	0	0	0	1	0	1	0	0	0
	STL	Stall On Line	0	0	0	0	0	0	0	1	0	0	0	1
	HLT	Halt	0	0	0	0	0	0	0	0	0	0	0	0
	TAB	Transfer A to Bank	0	0	0	0	0	0	1	0	0	0	0	1
	TBA	Transfer Bank to A	0	0	0	0	0	0	0	1	0	0	1	0
	ITS	Interrupt Save	0	0	0	0	0	0	0	1	0	1	0	0
	ITR	Interrupt Return	0	0	0	0	0	0	1	0	0	0	1	0
Skip	SPL	Skip if A is Positive	0	0	0	0	1	1	0	0	0	0	0	1
	SMI	Skip if A is Negative	0	0	0	0	1	0	0	0	0	0	0	1
	SZE	Skip if A is ZERO	0	0	0	0	1	0	0	0	0	0	1	0
	SNZ	Skip if A is Non-Zero	0	0	0	0	1	1	0	0	0	0	1	0
	SOV	Skip if Overflow Flip-Flop is Set	0	0	0	0	1	0	0	0	0	1	0	0
	SNO	Skip if Overflow Flip-Flop is Reset	0	0	0	0	1	1	0	0	0	1	0	0
	SPN	Skip if A is Positive and Non-ZERO	0	0	0	0	1	1	0	0	0	0	1	1
	SMZ	Skip if A is ZERO or Negative	0	0	0	0	1	0	0	0	0	0	1	1
	NOP	No Operation	0	0	0	0	1	0	0	0	0	0	0	0
	SKP	Skip Unconditionally	0	0	0	0	1	1	0	0	0	0	0	0

Input/Output Group Decoding

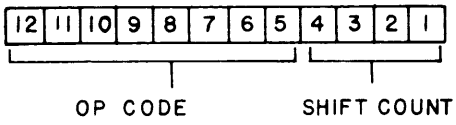
The format of the I/O group is as follows:



An instruction is identified as being in this group when bits 9 through 11 in the F-register are ZEROs and bit 12 is a ONE. Under these conditions, DGEN+ and F12+ are true (+6V), causing DIOG+ to go true (+6V) (LBD 12.05). Then, bits 7 and 8 of the W-register are decoded, generating the required I/O control signals. These are routed to the peripheral devices via the I/O bus. For example, DO78+ (LBD 12.05), which is true (+6V) when W07 and W08 both are ZEROs, causes the KINAL- line to go true (0V) (LBD 12.11). The signals decoded from the contents of the W- and F-registers are combined to generate CPU control signals. For example, DIOG+ and DO78+ generate DIAG+ (LBD 12.05), which allows RBFDB+ to go true (+6V) during TE4 time (LBD 12.01). Additional decoding is explained in the discussion of the instruction execution.

Shift Group Decoding

The shift group instruction format is as follows:



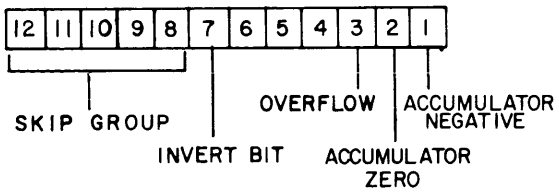
A shift instruction is identified when F09 through F12 and W08 are ZEROs and W07 is a ONE. Under these conditions, DSHFT- is 0V and DSHFT+ is +6V (LBD 12.05). Then, the DSHFT signals are combined with the contents of W05 or W06 to perform the required CPU functions. For example, DSHFT+ and W06- cause ADSUM- (LBD 12.03) to be false (+6V) during an LGR shift.

Generic Group Decoding

All 12 bits of this instruction group constitute the Op Code, and the contents of the F- and W-registers are used in the decoding. Bits 7 through 12 are all ZEROs and DG78Z+ is true (+6V) (LBD 12.05). A 2-out-of-6 decoding of bits 1 through 6 provides 15 possible combinations, 11 of which are used with this machine. A further breakdown is obtained by gating W05 and W06 with DG78Z+, which generates DGG5+ and DGG6+, respectively. These signals are used to generate the control signals for the instruction under execution. When W05 or W06 is not used, DG78Z+ is used along with the two selected bits to generate the required control signal (e.g., DG78Z+ • W02+ • W01+ generates DOCA- during an OCA instruction). A 12th generic instruction (HLT) is identified when all bits are ZEROs (e.g., on LBD 12.02, DG78Z+ and W01- through W06- are combined, generating TSTOP-).

Skip Group Decoding

The entire 12 bits of a skip instruction word constitute the Op Code, which is microprogrammed in the following manner:



This group is identified when bits 9 through 12 are ZEROs and W08 is a ONE, thus causing DSKP+ (LBD 12.05) to go true (+6V). Then, W01 through W04 are sampled by the skip logic on LBD 12.00, and the program counter is advanced if the conditions are met and the test is true.

SHIFT COUNTER OPERATIONS (LBD 12.04)

The 4-bit shift counter is used to control CPU operations during arithmetic type, shift type, and IRS instructions. The flip-flops in the counter are reset via the dc reset inputs during TF5, conditioning it for the execute cycle. The load mode also uses the counter.

During arithmetic instructions (ADD, ANA, OCA, TCA), 12 shift operations are required. In these cases, the shift counter is incremented twice (at the start of TE3 and TE4) before a shift operation is performed. After entering TE4, gate A13F causes CEE4+ to go false (0V), holding the timer in TE4. Each clock pulse causes one shift operation to be performed and increments the shift counter. Gate A13E looks for a count of 11, at which time 9 shift operations have been completed. When this count is reached, CEE4+ goes true (+6V), allowing the next clock pulse to restart the timer. This clock pulse also performs the 10th shift operation. The timer cycles through TE5 and TE6 while shifts 11 and 12 are completed.

A shift instruction (RAR, ARS, LGR) requires a different operation of the shift counter, because the required number of shifts is a variable. The ONE's complement of the desired number of shifts is loaded into the shift counter during TE1 via the dc set inputs. The shift counter is incremented at the start of TE3 and TE4 before a shift operation is performed. When TE4 time is entered, the set outputs of the counter flip-flops are gated onto a common line, causing CEE4+ to go false. This holds the timer in TE4. Each clock pulse shifts the contents of the A-register one place to the right and causes the shift counter to count. When one less than the desired number of shifts has been performed, the shift counter reaches all ZEROs and CEE4+ goes true. The next clock pulse performs the last shift operation and restarts the timer. The timer cycles through TE5 and TE6, but shifting operations are inhibited.

When an IRS instruction is executed, the shift counter must allow 12 shifts in TE4. After the timer enters TE3, CEE4+ goes false, conditioning the timer to be held in TE4. The shift counter is incremented at the start of TE3 and TE4 before shifting is started. Then the next clock pulse and

succeeding clock pulses shift the contents of the W-register one place to the right and increment the shift counter while the required logic operations are performed. Gate A13D looks for the count of 13, at which time 11 shifts have been completed. When that count is reached, CEE4+ goes true. The next clock pulse completes shift number 12 and restarts the timer. The timer cycles through TE5 and TE6, but shifting operations are inhibited.

ADDER OPERATIONS (LBD 12.03)

The 1-bit serial adder is used to perform the arithmetic operations of the CPU. It performs the prescribed function on the bits shifted out of the A- and/or W-registers and feeds the results back into the A- and/or W-registers. The following functions are performed by the adder: complementing numbers in the A-register; rotating numbers in the A-register; adding numbers in the A- and W-registers together; ANDing (ANA = add without carries) numbers in the A- and W-registers together; and incrementing numbers in the W-register.

Several of the preceding operations require the carry from the add of one bit position to be propagated and included in the add of the next bit position. The carry flip-flop (ADCRY), which is reset during TF5, is used to perform this function. During an ADD instruction, A01, W01, and ADCRY are combined. The ADCRY flip-flop is set if any two (or all three) of these signals are true (+6V). For all other combinations, the ADCRY flip-flop is reset. If a carry is generated by the high order position during an ADD instruction, the ADCRY flip-flop remains in the set condition. When this occurs, the adder overflow (ADOVF) flip-flop is set during TF4 of the instruction that follows the ADD instruction to save this condition. The ADOVF flip-flop is tested by an SOV (skip if set) or SNO (skip if reset) instruction. If the ADOVF flip-flop is set, it can be saved and used in a succeeding ADD instruction for multiple precision operation by transferring it into the A-register during a TOA instruction.

During the TCA and IRS instructions, the ADCRY flip-flop is used to increment by one (TCA = OCA+1).

When an instruction that does not require a carry is executed, the adder control logic maintains the ADCRY flip-flop in the reset condition and effectively removes it from the circuit. This occurs during shift operations, ANA instructions, and OCA instructions.

INSTRUCTION EXECUTION

At the end of the fetch cycle, the timer enters the execute cycle, during which the instruction is executed. The length of the execute cycle is variable, depending upon the instruction. In this section, the functions performed during the various execute cycles are explained. The logic that performs these functions is described by use of the LBDs as references. Each instruction is detailed, but instructions which perform similar operations are grouped under a common heading. In these descriptions, the term "passive" is used when a signal is at +6V, and the term "active" is used when a signal is at 0V. When an assertion signal (e.g., TCLK+) is true it is at +6V, and when it is false it is at 0V. When a negation signal (e.g., TCLK-) is true it is at 0V, and when it is false it is at +6V. The LBD number, which indicates where the referenced signals or gates may be found, is given in parentheses close to the point of reference.

STA and LDA Instructions (See FTD 12.77)

These instructions are used to exchange data between memory and the A-register. The effective memory location is identified by the contents of the Y-register established during the fetch cycle.

During the STA, data in the A-register are transferred to the W-register via the register bus, and a clear/write memory cycle is initiated to store the contents of the W-register. At the start of TE1, MARP-A goes true, resetting the memory address logic, and the output at B37E-24 goes passive (+6V) (LBD 12.00), causing the W-register Reset pulse (WR-) to go true (0V). With both F09+ and F11+ false (0V), DJSSA+ is true (+6V) and the input at C33P-4 (LBD 12.01) is active (0V). Thus, RBFA+ goes true (+6V), gating the contents o fthe A-register onto the register bus. Three of the inputs to C27D (LBD 12.01) are passive (+6V), and the gate is enabled when TCLK+B goes true (+6V). At this time RBTW- goes true (0V), resetting the MREAD flip-flop (LBD 12.00). With MREAD+A false (0V), the memory read cycle is inhibited. The RBTW+ signal also goes true (+6V), and gates the data on the register bus into the W-register.

At time TE1, MCILC+ is true (+6V), and

the leading edge of TCLK- sets the MCI flip-flop (LBD 12.00), which initiates the memory cycle. The memory cycle continues through TE2 and TE3. With MREAD+A false (0V), the effective memory location is cleared during the clear cycle. Then the write cycle is performed to transfer the contents of the W-register into memory.

At the start of TE3, A17G (LBD 12.02) goes active (0V), generating TSF1- (which inhibits the set input to the TE4 flip-flop) and TSF1+ (which conditions the set input to the TF1 flip-flop). Then the execute cycle is terminated and the next fetch cycle is started at the end of TE3.

The execute cycle of the LDA instruction initiates the read/regenerate cycle of the memory and clears both the W- and the A-registers. Data in the effective location is read and loaded into the W-register. Then the contents of the W-register are gated into the A-register.

At the start of TE1, the memory address logic is reset by MARP-A, and the W-register is reset by WR-. During the fetch cycle the decoded Op Code (LBD 12.05) has generated DLDA+, which causes DIAG+ to go true (+6V). During TE1, the A-register Reset pulse (AR-) is generated (LBD 12.00), resetting the A-register.

The MCILC+ signal has also gone true and the MCI flip-flop is set by TCLK-, initiating the memory cycle. The MREAD flip-flop is set during the fetch cycle (if reset by a previous instruction) and with MREAD+A true (+6V), the memory read cycle is performed. The contents of the effective memory location are loaded into the W-register during TE2. At the start of TE3, DLDA+ generates RBFWU+ and RBFWL+ (LBD 12.01), gating the contents of the W-register onto the register bus. Then, TCLK+B is ANDed with DLDA+ and TE3+A at B24H (LBD 12.01), generating RBTA+. The trailing edge of RBTA+ gates the data on the register bus into the A-register.

During TE3, the exit logic is conditioned as it was for the STA instruction. At the end of TE3, the execute cycle is terminated and the next fetch cycle starts.

ADD and ANA Instructions (See FTD 12.79)

During these instructions, the read/regenerate mode of the memory is enabled and the contents of the effective memory location are loaded into the W-register. Then the contents of the W-register and the A-register (loaded prior to this instruction) are shifted serially through the adder. The execute cycles of these instructions differ only with respect to the operation of the carry flip-flop (ADCRY) in the adder.

Since the control logic performs similar functions during both instructions, a general discussion of the control logic will be provided below. The differences in the operations performed by the adder during the two instructions will be described separately.

Upon entering TE1, MARP-A and WR- are generated (LBD 12.00), resetting the memory address logic and the W-register, respectively. Since MCILC+ is true during TE1 of these instructions, the MCI flip-flop is set by TCLK- (LBD 12.00), initiating the memory cycle. The memory cycle continues through TE2 and TE3, and the data read from memory are loaded into the W-register via its dc set inputs at the end of the read cycle. After regenerating the memory location the contents of the W- and A-registers are shifted through the adder in a serial fashion, and the shift counter is used to count the shift operations.

At the start of TE3, A13A (LBD 12.00) is enabled, generating CCNT-. The shift counter is incremented by the leading edge of CCNT-, but the data is not shifted. At the start of TE4 the leading edge of CCNT- increments the shift counter again. The contents of F10- and F11+ are ANDed in B21F (LBD 12.00), causing CTT+ to go true (+6V), and A13F is enabled by CTT+ (LBD 12.04), causing CEE4+ to go false. With CEE4+ false, the timer is held in TE4 (LBD 12.02). CTT+ also conditions the logic used to generate shift pulses (B21G for ASHF+, and B23H for WSHF, on LBD 12.00).

The contents of A01 and W01 are routed to the adder and combined in accordance with the instruction being executed. Complementary signals (ADSUM+ and ADSUM-) are routed from the adder to the set and reset controls of A12. (W12 also receives ADSUM, but the results in the W-register are not used.) When TCLK+B goes true, ASHF+ and WSHF+ are generated. Their trailing edges perform the first data transfer by shifting the results of ADSUM into the registers. At the same time, the shift counter is incremented for the third time.

Data are shifted and the shift counter is incremented by each clock pulse while A13E (LBD 12.04) looks for the count of 11. When the count of 11 is reached, the ninth shift operation has been performed. CEE4+ now goes true, conditioning the timer for restart. Then the next clock pulse sets the TE5 and TF1 flip-flops and completes the 10th shift operation. During the next two clock pulses, the last two shift operations are completed and the fetch cycle of the next instruction is started.

Adder Operation During ADD.—The adder logic appears on LBD 12.03. A simplified version of the logic used during an ADD instruction is shown in Figure 3-1. The truth table shows that the adder performs a binary add with carries.

When the ADCRY flip-flop is reset, gates C28A and C28D are inhibited. An OR circuit if formed by B26A and B25D such that either A01+ or W01+ being true (+6V) will cause ADSUM+ to be true (+6V) via C34A, C34B, and C33F. This causes a ONE to be transferred into A12 when a shift occurs. If neither A01+ nor W01+ is true (+6V), ADSUM+ will be false (0V). If both A01+ and W01+ are true (+6V), ADSUM+ will be false (0V) via gates C33D, B25C, B26B, C34B, and C33F. The set side of the ADCRY flip-flop is conditioned if both A01+ and W01+ are true (+6V). In this case A01- and W01- are both false (0V), causing the common output of C33D and B25C to be true (+6V) and thereby allowing the setting of the ADCRY flip-flop via C34C, C33G, and ASHF+.

When the ADCRY flip-flop is set, gate C34B is inhibited. The output of the OR circuit formed by B26A and B25D will generate ADSUM+ via path C34A, C33E, C28A, and C33F, which contains one more inverter than the previous path. Thus, either A01+ or W01+ being true (+6V) will cause ADSUM+ to be false (0V), which will cause a ZERO to be transferred into A12. If neither A01+ nor W01+ is true (+6V) ADSUM+ will be true (+6V). If both A01+ and W01+ are true (+6V) ADSUM+ will be true (+6V) via C33D, B25C, B26B, C33E, C28A, and C33F. If either A01+ or W01+ (or both) is true (+6V) the ADCRY flip-flop will remain set via B26A, B25D, C34A, C28D, C33G, and ASHF+. If neither A01+ or W01+ is true (+6V) the reset side of the ADCRY flip-flop is conditioned and the next ASHF+ will reset it.

If the ADCRY flip-flop is set after the add operation is complete, the ADOVF+ flip-flop will be set during the next TF4 time via C27A.

Adder Operation During ANA.—Figure 3-2 is a simplified diagram of the adder logic used during an ANA instruction. The truth table shows that the contents of W01 are logically ANDed with A01. If either A01+ or W01+ (or both) is false, the input to C28B is active (0V), ADSUM- is passive (+6V), and a ZERO is shifted into the A-register. If both A01+ and W01+ are true (+6V), the input to C28B is passive (+6V), ADSUM+ is passive (+6V), and a ONE is shifted into the A-register.

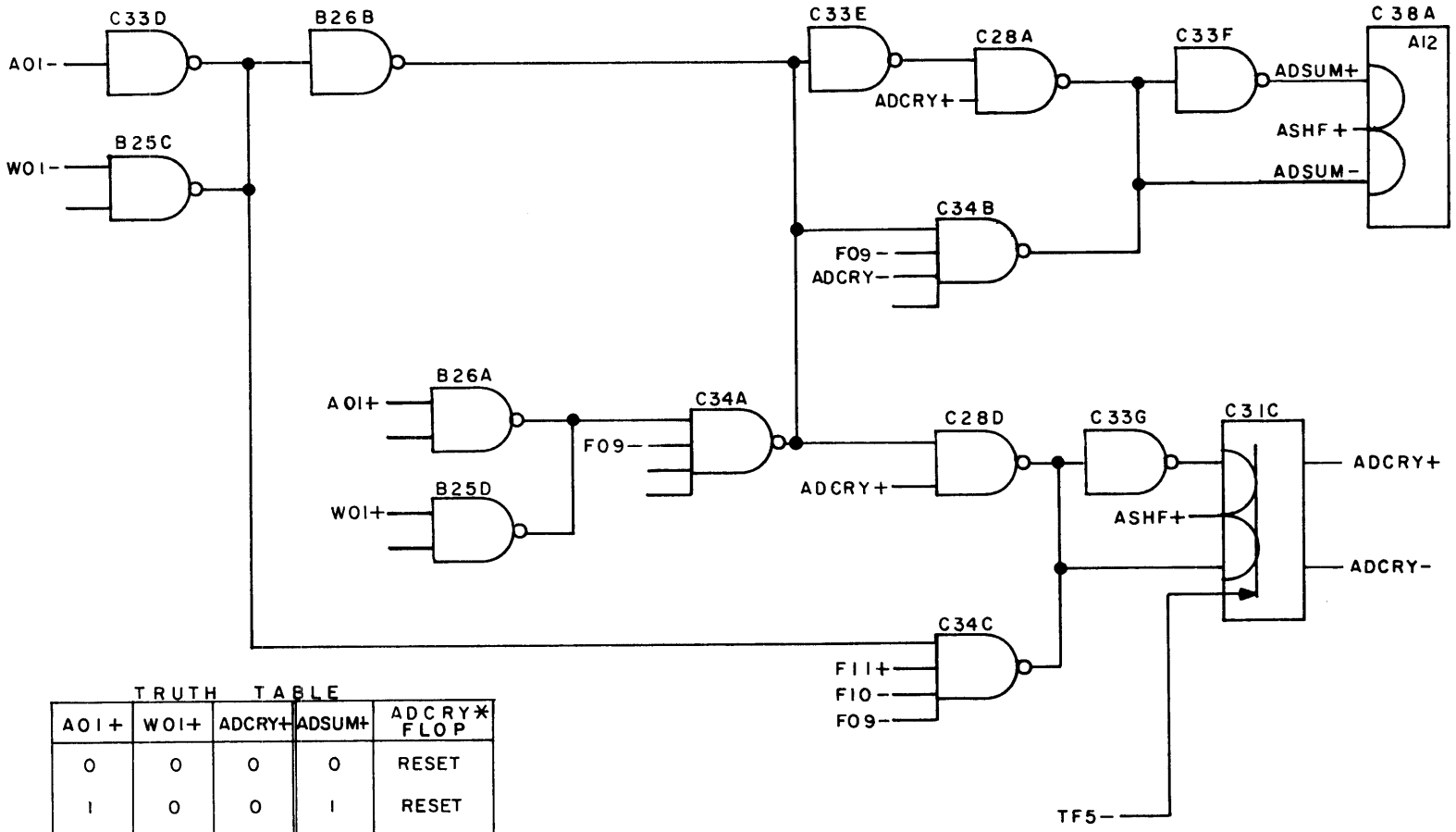
IRS Instruction (See FTD 12.78)

During the execute cycle of this instruction, the contents of the addressed memory location are loaded into the W-register and shifted through the adder, where they are incremented, and the results are returned to the addressed memory location. The results are then sampled. The program counter is advanced, causing the next instruction to be skipped if the results equal zero.

Since the operations performed during this instruction are similar to an ADD instruction, only the difference between the two instructions will be explained in detail in this section. At the start of TE1, MARP- is generated to reset the memory address logic, and WR- is generated to reset the W-register, as they were in ADD. During this instruction, the decoded IRS (DIRS) signal sets the ADCRY flip-flop via B26C (LBD 12.03) and causes CEE4+ to be false (LBD 12.04). The MCI flip-flop is set by the leading edge of TCLK-, initiating a read/regenerate memory cycle (LBD 12.00).

At the start of TE3, CCNT- goes true and the shift counter is incremented without shifting data. The memory cycle continues during TE3, and the contents of the addressed memory location are loaded into the W-register. The shift counter is incremented a second time without shifting data as TE4 is entered. With CEE4+ false, the timer is held in TE4, and each TCLK+B pulse generates WSHF+ (LBD 12.00). The trailing edge of WSHF+ clocks the ADCRY flip-flop (LBD 12.03) and shifts the data in the W-register (LBD 12.08).

The state of the bit loaded into the W-register depends on the output of the adder logic (ADSUM). Figure 3-3 is a simplified diagram of the adder logic used during this instruction. The truth table indicates the four possible conditions encountered.



TRUTH TABLE

A01+	W01+	ADCRY+	ADSUM+	ADCRY* FLOP
0	0	0	0	RESET
1	0	0	1	RESET
0	1	0	1	RESET
1	1	0	0	SET
0	0	1	1	RESET
1	0	1	0	SET
0	1	1	0	SET
1	1	1	1	SET

* AFTER SHIFT

6389

Figure 3-1. ADD Simplified Diagram

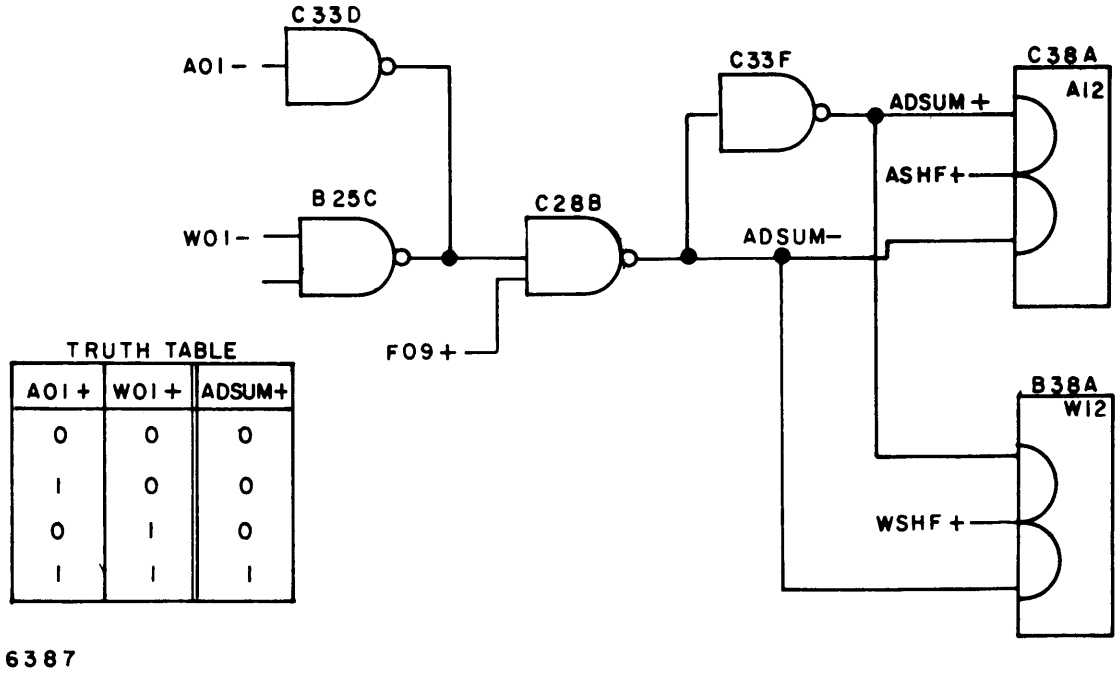


Figure 3-2. ANA Simplified Diagram

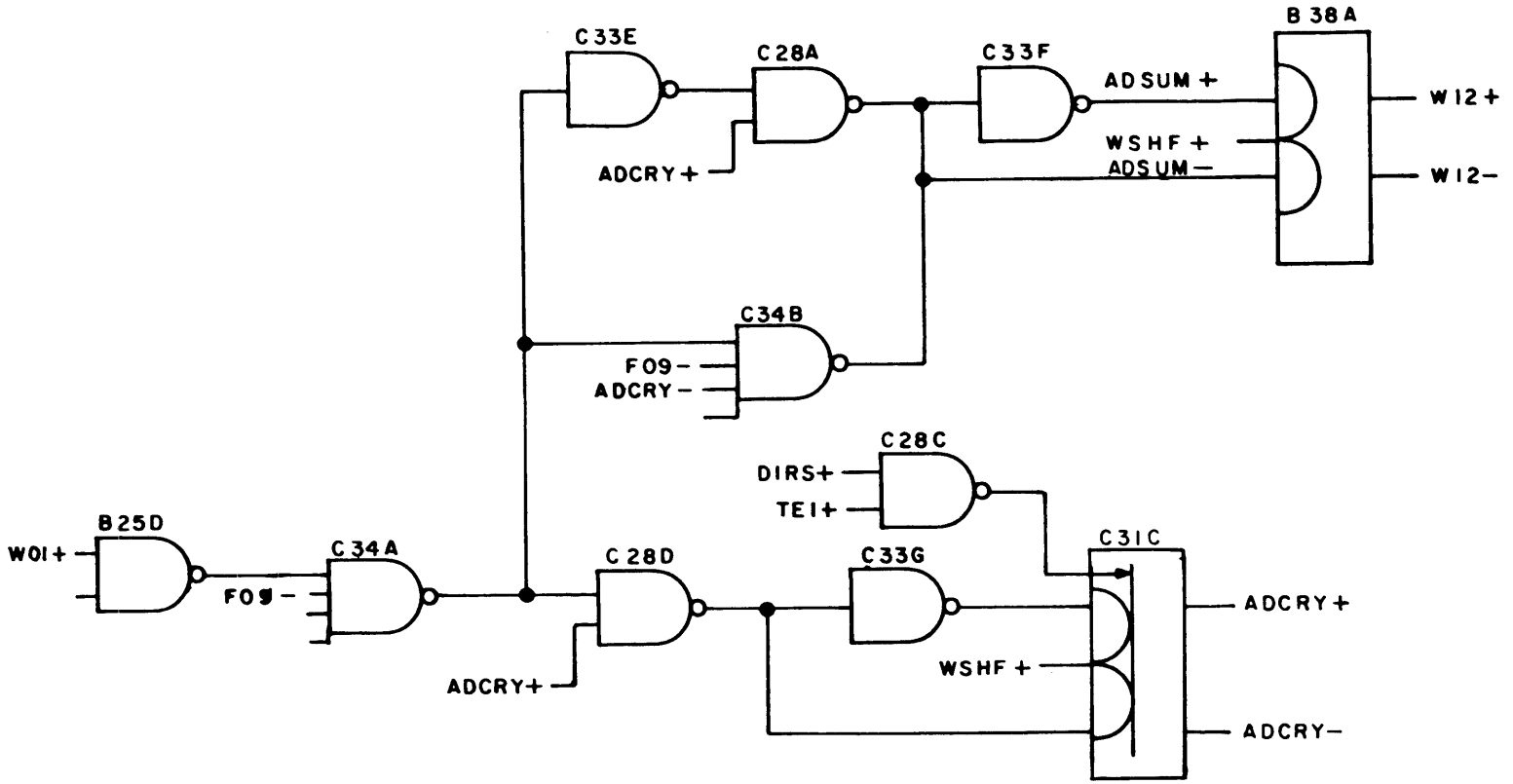
Before the first shift, ADCRY+ is always true because the ADCRY flip-flop was set during TE1. If W01+ is true at this time, the contents of W01 must be inverted and transferred into W12 while the ADCRY flip-flop remains set. To perform this function, the set input to the ADCRY flip-flop and the reset input to the W12 flip-flop are conditioned when the output of C34A goes passive (+6V). When the trailing edge of WSHF+ clocks the ADCRY flip-flop and shifts the W-register, the ADCRY flip-flop remains set, a ZERO is transferred into the W-register, and the data in the W-register are shifted 1 bit to the right.

As long as W01+ remains a ONE, this action is repeated for each shift. When a ZERO is shifted into W01, the output at C34A goes active (0V), conditioning the reset input of the ADCRY flip-flop and causing ADSUM+ to go true (+6V). The trailing edge of the next WSHF+ pulse resets the ADCRY flip-flop and shifts a ONE into the W-register. Once the ADCRY flip-flop is reset, it remains reset for the remainder of the shift operations. Under these conditions, C28A and C28D are effectively removed from the circuit and C34B is enabled. The remainder of the 12 bits are then shifted without inversion.

During the shifting operations, A13D (LBD 12.04) samples the outputs of the shift counter, looking for a count of 13. When this count is reached, 11 shifts have been completed and CEE4+ goes true, conditioning the timer for restart. During this instruction, B17B (LBD 12.02) in the timer prevents the next fetch cycle from starting during TE4.

Additional functions are performed following shift 11. The output from C27F (LBD 12.00) goes active (0V), resetting the MREAD flip-flop and causing MCILC+ to go true. Gate B22A (LBD 12.00) samples W01+ and ADCRY+. If either signal is false, the gate is disabled and effectively removed from the circuit. When both signals are true, shift 12 completes the loading of all ZEROs into the W-register, and a skip condition is indicated. PADV- is generated when MCILC+ goes true, advancing the program counter to the next instruction to be executed.

The next clock pulse restarts the timer in TE5, performs shift 12, and sets the MCI flip-flops which initiates a clear/write memory cycle. The memory cycle continues during TE5 and TE6, and the contents of the W-register are written into the



TRUTH TABLE

W01+	ADCRY+	ADSUM+	ADCRY* FLOP
0	0	0	RESET
1	0	1	RESET
0	1	1	RESET
1	1	0	SET

* AFTER SHIFT

Figure 3-3. IRS Simplified Diagram

addressed memory location. During TE6, B15B (LBD 12.02) generates TSF1+, and the following clock pulse starts the fetch cycle of the next instruction.

Shift Instructions (LGR, ARS, RAR) (See FTD 12.81)

During a shift instruction, the shift counter is loaded with the ONE's complement of the desired number of shifts. The contents of A01 are conditioned in the adder, the adder output is transferred into A12, and the contents of the A-register are shifted to the right. With the exception of what is transferred into A12, the three instructions are executed in an identical fashion. Therefore, overall operations will be discussed in a group while conditions for A12 transfers will be described separately. The data to be operated on must be in the A-register before the shift instruction is performed.

The decoded shift signal (DSHFT+) conditions gates C36K and A13C (LBD 12.01) at the start of The execute cycle, TE1+ goes true, enabling C36K and generating RBFWL+. The desired number of shifts is contained in the lower 4 bits of the W-register, and RBFWL+ gates this count onto the register bus. TCLK+B then conditions A13C to generate RBTC-, which loads the ONEs complement of of the count into the shift counter (LBD 12.04).

At the start of TE3, CCNT- goes true (0V) (LBD 12.00) and the shift counter is incremented for the first time. No shifting is done in TE3 time. The shift counter is incremented a second time (without shifting data) at the start of TE4. Upon entering TE4, the shift counter output gating logic is enabled, causing CEE4+ to go false (0V) (LBD 12.04). The timer is held in TE4 until CEE4+ goes true (+6V).

The contents of A01+ are routed to the adder logic (LBD 12.03), and the adder output (ADSUM) is conditioned according to the instruction under execution. Figure 3-4 is a simplified diagram of the adder logic used for the shift instruction.

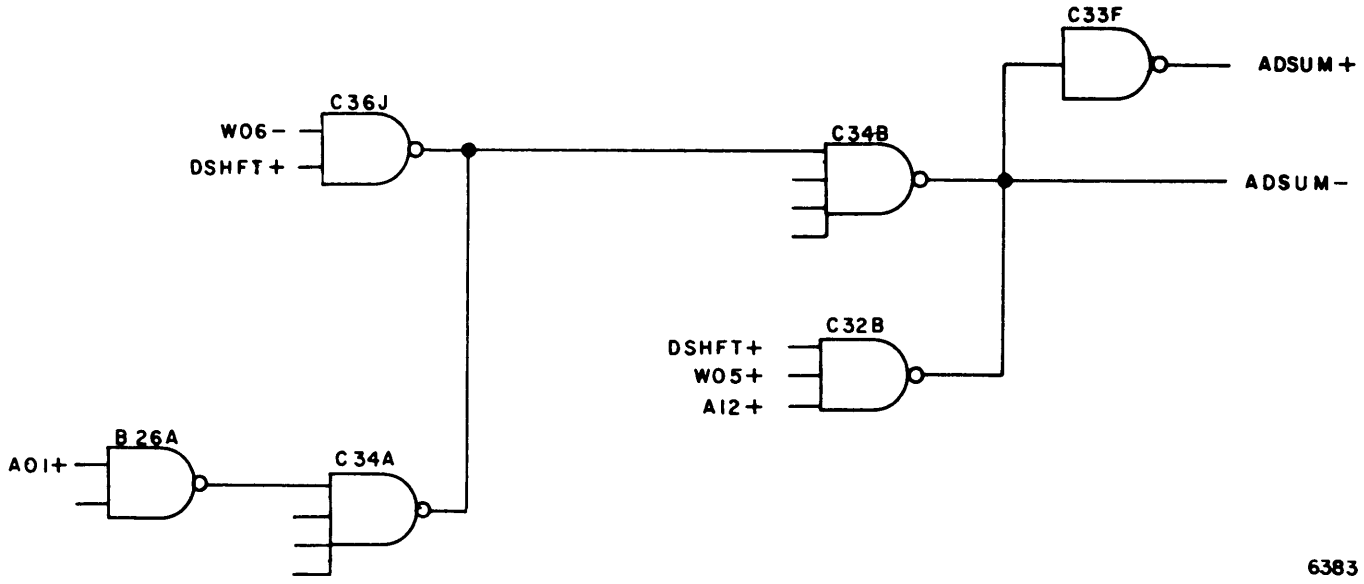


Figure 3-4. Simplified Shift Diagram

During an LGR instruction, the contents of the A-register are shifted to the right with ZEROs shifting in from the left. To perform this function, the output of C36J is active (0V), causing ADSUM+ to be false (0V), and a ZERO is loaded into A12 during a shift.

If an ARS instruction is executed, the contents of the A-register are shifted to the right and the sign bit (the original contents of A12) is shifted in from the left. To perform this function, the output of C32B is determined by the contents of A12. When A12 is a ONE, the output of C32B is active (0V), ADSUM+ is true (+6V), and a ONE is loaded into A12 during the shift.

During an RAR instruction, the contents of the A-register are shifted to the right and the contents

of A01 are shifted back into A12. To perform this function, W05+ and W06- are both active (0V) and C36J and C32B are effectively removed from the circuit. After four stages of inversion, ADSUM+ is the same as A01+ and the resultant signal is transferred into A12 during a shift.

The adder overflow (ADOVF) flip-flop is set when any ONE is shifted out of A01 during the LGR and ARS instructions. To perform this function, C34D (LBD 12.03) is conditioned to sample A01+ during the shift.

The first clock pulse after entering TE4 generates both CCNT- and ASHF+ (LBD 12.00). The shift counter is incremented for the third time by CCNT-, and the trailing edge of ASHF+ shifts the A-register for the first time. Each clock pulse that follows causes the shift counter to be incremented and a shift to take place. When the shift counter reaches all ZEROs, one less than the desired number of shifts has been performed and CEE4+ goes true, conditioning the timer for restart. The next clock pulse completes the last shift, restarts the timer in TE5, and starts the next fetch cycle. Shifting operations are inhibited when C36L (LBD 12.00) goes active, preventing the generation of ASHF+.

I/O Instructions (See FTD 12.84)

Data and control transfers between the CPU and external devices (or systems) are performed via the five I/O instructions. All I/O instructions use the full execute cycle (TE1 through TE6) and are executed in a similar manner. Therefore, a general discussion of an I/O instruction will be provided with the differences between the instructions pointed out.

A description of an I/O instruction begins with TF3 of the fetch cycle, when the instruction is loaded into the W-register. The address of the selected device is contained in W01 through W06, and these signals are routed to all devices via the common address bus (KAB01- through KAB06- on LBD 12.11).

All combinations of W07 and W08 are decoded (LBD 12.05), forming the four signals (D078+, D178+, D278+, and D378+) which identify the I/O instruction under execution. The signals generated are routed to drivers (LBD 12.11) whose outputs are connected to the control lines in the I/O bus.

During TF4, the contents of W09 through W12 are transferred as usual into the F-register. When an I/O instruction is being executed, the F-register contains a ONE in bit 12 and ZEROs in the other 3 bits.

Complementary DIOG signals are generated by decoding the contents of the F-register (LBD 12.05). DIOG+ enables the drivers, which cause the selected I/O control lines (KINAL-, KSKSL-, KOTAL-, KOCPL-) to go true (LBD 12.11).

If an OTA or SMK instruction is under execution, data stored in the A-register during a previous instruction are gated to the I/O devices via the common data bus (KDBXX). To perform this function, DIOG+ and W08+ are ANDed (LBD 12.10) to generate KDBFA+. The line drivers on two CS-517 PACs are enabled by KDBFA+, gating the data in the A-register onto the common data bus (KDB01- through KDB12-).

At this time, the address of the selected device is on the address lines, the selected I/O instruction line is true (0V), and the data are on the data bus if an OTA or SMK instruction is under execution. The selected device causes the test line (KTSTL-) to go true (0V) if it is ready for a transfer (INA or OTA instructions) or if a skip is to be performed (SKS instruction). The CPU timer continues to cycle through the fetch and execute cycles without performing additional functions if the test line does not go true (0V). The one exception to this is the INA instruction. During an INA instruction, the A-register is cleared to receive incoming data [whether or not the test line goes true (0V)]. To perform this function DIOG+ and D078+ are ANDed (LBD 12.05), generating DIAG+, which conditions C26N (LBD 12.00). Then TE1+B goes true at the start of TE1, generating AR-.

When the test line goes true (0V), the level is inverted and routed to the set input of the READY flip-flop as TSTLN+. Upon entering TE3 the READY flip-flop is set if TSTLN+ is true (+6V) (LBD 12.01). During an OTA, INA, or SKS instruction, B22F (LBD 12.00) is enabled at the start of TE4 if the READY flip-flop is set, which causes PADV- to go true (0V). Under these conditions, the program counter is advanced and the next instruction is skipped. If the READY flip-flop is not set, PADV- remains false, the transfer is not completed, and the next sequential instruction is executed. A program skip is never generated during an OCP or SMK instruction, because D378- is true (0V) and B22F is inhibited.

During execution of an INA instruction, the data on the data bus are gated into the A-register during TE4. To perform this transfer, the negation output of the READY flip-flop is gated to B15H in the decoder (LBD 12.05), allowing DINA+ to go true (+6V). Gate C25A (LBD 12.01) is conditioned by DINA+ and at the start of TE4, RBFDB+ goes true (+6V). Data on the I/O data bus (KDB01- through KDB12- on LBD 12.10) are gated onto the register bus by RBFDB+. TCLK+B then goes true (+6V), generating RBTA+ (LBD 12.01), which loads the data into the A-register.

At the start of TE5, the strobe flip-flop (B21J and B21H) is set (LBD 12.01), causing STRB+ to go true if an OCP instruction is being executed [D378- is true (0V)] or if an INA, OTA, or SKS instruction is being executed while the READY flip-flop is set [READY- is true (0V)]. If an SMK instruction is being executed, TZERO+ (W02 through W06 all ZEROs) and D378+ are true (+6V), generating SMK+. STRB+ is also generated during an SMK instruction, but it is considered redundant.

When STRB+ and SMK+ are generated, they are gated onto the control bus by DIOG+ (LBD 12.11), causing KSTRB- and KSMKL- lines to go true (0V), respectively. The KSTRB- line is routed to the external devices causing a data transfer to the device during an OTA and acknowledging a data transfer from the device during an INA. The next instruction will be skipped when the instructions are successfully completed. The OCP does not cause a skip condition. The KSMKL- line is true (0V) during the execution of an SMK00 or SMK01 instruction. This line, along with KAB01± and the appropriate data bus bit, is used to set or reset the mask flip-flop in the appropriate device.

During TE6 of all instructions, TSF1+ goes true. The next clock pulse starts the fetch cycle of the following instruction and resets the strobe flip-flop (LBD 12.02).

Generic Instructions (See Appropriate FTD)

All the generic instructions assigned to the H112 will be described individually in this section except for the OCA and TCA instructions. These two instructions have a similar execution cycle and will therefore be discussed together with the differences pointed out. Various decoded signals used in more than one instruction will be explained in detail the first time they are used and thereafter simply referenced.

CRA Instruction.—The A-register is cleared during the execution of this instruction, and the execute cycle is terminated at the end of TE1. To perform these functions, gate A23J in the timer (LBD 12.02) is conditioned by DGG6+ (generic group with W06+ a ONE) and A14E (LBD 12.05) is enabled by DGG5+ (generic group with W05+ a ONE) and W01-, causing DIAG+ to go true (+6V). At the start of TE1, DIAG+ and TE1+B generate AR- (LBD 12.00), which resets the A-register. Gate A23J is enabled by TE1+, which conditions the timer for an exit at the end of TE1. The trailing edge of the next clock pulse terminates the execute cycle and starts the next fetch (if the TRUN flip-flop is set).

OCA/TCA Instructions.—During these instructions, the contents of the A-register (loaded during a previous instruction) are shifted serially through the adder, and the results are returned to the A-register.

The shifting operations are similar to the shifting operations of the ADD and ANA instructions, except that only the contents of the A-register are shifted during the OCA and TCA instructions. At the start of TE3 and TE4, TCLK- generates CCNT- (LBD 12.00) and the shift counter is incremented twice before any data has been shifted. At the start of TE4, CTT+ is generated (LBD 12.00) and routed to the shift counter logic (LBD 12.04), causing CEE4+ to go false. With CEE4+ false, the timer is held in TE4 and each clock pulse generates CCNT- and ASHF+. A01 is routed through the adder. The adder output (ADSUM), whose level depends on the instruction under execution, is routed to the set and reset inputs of A12. The leading edge of CCNT- increments the shift counter, and the trailing edge of ASHF+ clocks the transfer into the A-register. The contents of the A-register are shifted to the right and ADSUM is transferred into A12.

Gate A13E in the shift counter logic (LBD 12.04) looks for the count of 11 from the shift counter. When the count of 11 has been reached, 9 shifts have been completed and CEE4+ goes true, conditioning the timer for restart. The next clock pulse completes shift 10, restarts the timer in TE5, and starts the next fetch cycle. Shifts 11 and 12 are completed at the end of TE5 and TE6, respectively, completing the shifting operations.

The adder logic used for the OCA and TCA instructions is shown in Figure 3-5. The ADCRY flip-flop is reset during TF5 and remains reset during the execution of an OCA. With the ADCRY flip-flop reset, C34B is conditioned and C28A is effectively removed from the circuit. A01- is gated through C34B, which inverts its polarity.

During a TCA instruction, the contents of the A-register are ONEs complemented and a ONE is added to the result as the bits are shifted through the adder. To perform these functions, the ADCRY flip-flop is set at the start of TE1 and reset for the remainder of the cycle when A01- goes true for the first time. While the ADCRY flip-flop is set, C28A is conditioned and C34B is effectively removed from the circuit. The contents of A01 are gated through C28A and each bit is shifted unchanged. When A01- goes true (the first ONE detected), the reset input of the ADCRY flip-flop is conditioned. Then the ADCRY flip-flop is reset during the next shift operation and remains reset for the remainder of the instruction. With the ADCRY flip-flop reset all remaining bits are inverted when shifted through the adder.

ENB/INH Instructions.—The ENB instruction enables the interrupt logic and permits interrupts after the next instruction is executed. To perform this function, the set input of the interrupt enable flip-flop (C31A on LBD 12.03) is conditioned by DGG6+ and W03+. At the start of TE1, the flip-flop is set, removing one of the two inhibits from the set input of the INTFF flip-flop.

The INH instruction is used to inhibit the interrupt logic. To perform this function, the reset inputs of the interrupt enable flip-flop and the INTFF flip-flop are conditioned by DGG6+ and W04+. At the start of TE1, both flip-flops are reset, disabling the interrupt logic.

During TE1 of both instructions, the timer is conditioned to terminate the execute cycle and start the next fetch cycle.

TOA Instruction.—This instruction is used to save the contents of the adder overflow (ADOVF) flip-flop. The A-register is reset by AR-, which is generated when DIAG+ and TE1+B are ANDed together (LBD 12.00). Gate C27B at the output of the ADOVF flip-flop (LBD 12.03) is conditioned by DGG5+ and W04+ and enabled at the start of TE2. If the ADOVF flip-flop is set, ASA01- goes true and A01 is set via the dc input.

Gate C32D, feeding the reset input of the ADOVF, is conditioned by DGG5+ and W04+ and is enabled at the start of TE3, thus resetting the flip-flop. During TE3 the timer is conditioned to terminate the execute cycle and start the next fetch cycle. These operations are completed at the end of TE3.

HLT Instruction.—All instruction bits are ZEROs during a HLT instruction. TSTOP- goes true (LBD 12.02), which resets the RUN flip-flop via the dc reset input. With the RUN flip-flop reset, the set input of TF1 is inhibited and all machine operations are terminated.

STL Instruction.—The operations performed during the execute cycle of this instruction are determined by the condition of the KSTAL- line of the control bus (LBD 12.11). The level on the line is inverted twice and the resultant signal, STALN-, is routed to A13G in the timer. Normally, this signal is false (+6V). When an STL instruction is decoded, the set input to the TE3 flip-flop and the reset input to the TE2 flip-flop are inhibited, which holds the timer in TE2.

When STALN- goes true (0V), the set input to TE3 is conditioned and the next clock pulse restarts the timer. Upon entering TE3, the reset input to TE2 is conditioned and the timer is conditioned to terminate the execute cycle (TSF1+ goes true) (+6V). The following clock pulse then resets both the TE2 and the TE3 flip-flops and starts the next fetch cycle.

If STALN- is true when the STL instruction is executed, the above actions do not occur and the instruction acts like an NOP.

Expanded Address Option Instructions.—These instructions operate with the expanded address option. If the expanded address option is not contained in the CPU, these instructions are treated as a NOP or CRA. The logic referenced in the following discussions is shown on LBD 12.12.

a. *TAB Instruction.*—The contents of A01 are transferred into the bank (B-) register during this instruction. At the start of TE1, the ANDing of W01+, DGG6+, and TE1+ enables A33C, which clears the B-register. The timer is conditioned to terminate the execute cycle at the end of TE1. The next clock pulse terminates the execute cycle and starts the following fetch cycle. When TF1+ goes true the contents of A01+ are gated into the B-register.

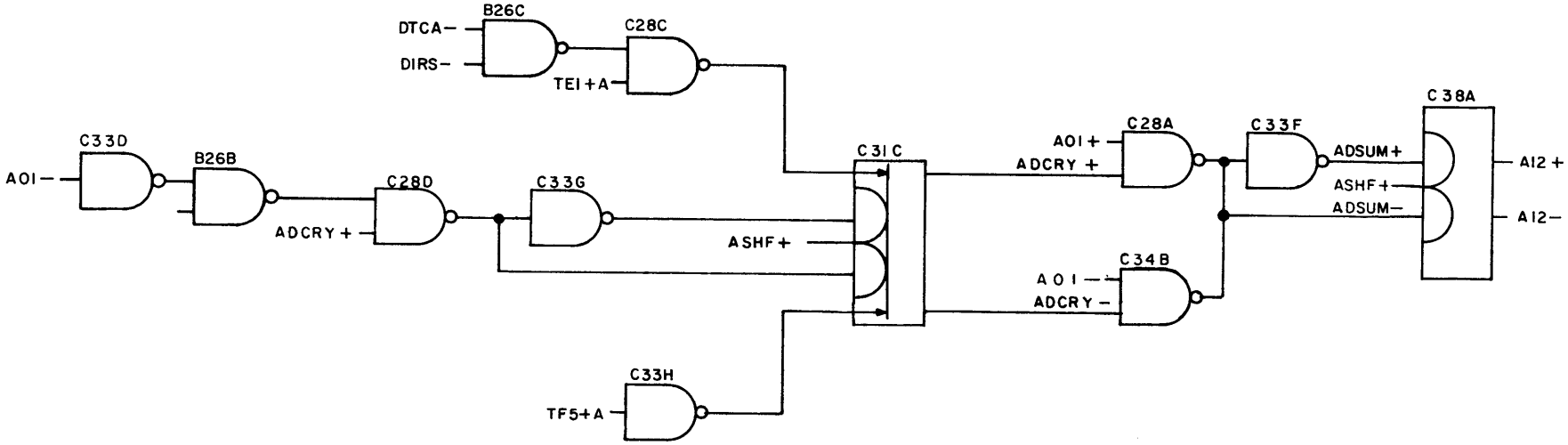


Figure 3-5. OCA and TCA Simplified Diagram

b. *ITR Instruction.*—This instruction is executed to transfer the contents of A01 and A03 to Z01 and Z03, respectively. At the start of TE1, the ANDing of W02+, DGG6+, and TE1+ enables A33H, which clears Z01 and Z03 via the dc reset inputs. The timer is conditioned to terminate the execute cycle at the end of TE1. The next clock pulse terminates the execute cycle and starts the next fetch cycle. When TF1 goes true, ZFA- and ZFA+ are generated. ZFA+ gates the contents of A01 and A03 into the Z-register. At the same time, ZFA- sets the ITRFF flip-flop, conditioning the logic for an indirect jump or indirect jump store instruction. When either instruction is performed, Z01 is gated into B01 and Z03 is gated into P13.

c. *TBA Instruction.*—During this instruction the contents of B01 are transferred to A01 and P13 is transferred to B01. DGG5+ and W01– are decoded, generating DIAG+ (LBD12.05). At the start of TE1, C26N is enabled, generating AR– and resetting the A-register (LBD 12.00). Then the ANDing of DGG5+, W02+, and TE3+a generates BTA+ and gates the contents of B01 into A01 (LBD 12.12) and P13 into B01.

d. *ITS Instruction.*—If the interrupt logic is enabled when an interrupt occurs, the contents of B01 are loaded into Z01 and the contents of P13 are loaded into Z03 by INTFF+. During this instruction, the contents of the Z-register are transferred to the A-register to save the data. The A-register is cleared at the start of TE1 when C26N is enabled and generates AR– (LBD 12.00). Then the ANDing of DGG5+, W03+, and TE3+A generates ZTA+, gating the contents of Z01 and Z03 into A01 and A03, respectively.

Skip Instructions.—These instructions are performed to test various CPU conditions. When a tested condition is true, the program counter is advanced and the next sequential instruction is skipped. The Op Code for these instructions can be microprogrammed to test more than one condition. If the invert bit (W07) is a ZERO when conditions are microprogrammed, the tested conditions are ORed and a skip is generated if any test condition is true. If the invert bit is a ONE when conditions are microprogrammed, the test conditions are ANDed and a skip is generated only if all test conditions are true.

A skip instruction is decoded and DSKP+ is generated when DGGG+ (bits 9 through 12 all ZERO) and W08+ are both true (LBD 12.05). The DSKP+ signal and the output of the skip logic enable B23B (LBD 12.00). PADV- then goes true at the start of TE1 if the skip is to be performed.

The operation of the skip logic is similar for all skip instructions. Three typical instructions have been selected as examples and the operation of the skip logic during these instructions will be described. The logic described is located on LBD 12.00.

a. *SPL Instruction.*—During this instruction, the program counter is advanced if the A-register is positive. Bit 7 is a ONE, making W07+ true and enabling B25E. If the A-register is positive, A12 is a ZERO and A12+ is false (0V). Gate B21A is disabled and its output goes passive (+6V). The level is inverted and applied to B25E-20, disabling the gate. Since B25M is disabled by W07-, the common output from B25E and B25M is passive (+6V) and B23B is conditioned. At the start of TE1, PADV- goes true (0V), incrementing the program counter.

b. *SOV Instruction.*—During this instruction the program counter is advanced if the adder overflow (ADOVF) flip-flop is set. W07+ is false (0V) and B25E is disabled. Gate B21C is conditioned by W03+ and enabled by ADOVF+ if the ADOVF flip-flop is set. The output at B21C-13 goes active (0V), disabling B25M. With both B25E and B25M disabled, their common output is passive (+6V). B23B is conditioned at the start of TE1, PADV- goes true, and the program counter is incremented.

c. *SKP Instruction.*—This instruction is executed to increment the program counter independently of any condition. Since no condition is being tested, the common line from the conditioned gates is passive (+6V) and B25E is disabled. W07- is a ZERO and B25M is disabled. With B25E and B25M disabled, their common output is passive (+6V) and PADV- goes true at the start of TE1.

JMP Instruction.—During the execute cycle of this instruction the effective address contained in the Y-register is transferred into the program counter to alter the normal program sequence. If the CPU contains the expanded address option and the instruction is indirectly addressed, additional functions will be performed in the execute cycle. Therefore, the execute cycle of a normal JMP instruction will be described below, and the additional functions which can be performed will then be discussed.

The outputs from F09+ and F10+ are decoded and the DJG signals go true (LBD 12.05) during the fetch cycle. DJG+ conditions B26J, which causes PR- to go true (0V) at the start of TE2 (LBD 12.00). The program counter is reset, which conditions it to receive a transfer from the Y-register. The contents of the Y-register are routed to the program counter input gating logic (LBD 12.06). B24D is conditioned by DJG+ and TE3+A during TE3, which causes YTP- to go true (0V) when TCLK+B goes true (+6V) (LBD 12.00). The program counter input gating logic is enabled by YTP-, which transfers the address in the Y-register to the program counter.

The timer is conditioned to terminate the execute cycle at the end of TE3 and start the next fetch cycle. The program continues from the new address in the program counter.

With the expanded address option the execution of an indirect jump (JMP*) causes the contents of B01 to be transferred to P13 and P13 to be transferred to B01, if this instruction does not follow an ITR instruction. During TF5 of the indirect cycle, B01+ is gated to the set input of Y13 and transferred into Y13 by the trailing edge of RBTYU+ (LBD 12.12). The ITRFF flip-flop is in the reset condition and A33E is enabled during TE1. At the end of TE1, the contents of P13 are transferred into the B-register. Then the contents of Y13, which were the contents of B01, are loaded into P13 via the dc set input during TE3 by YTP-.

When an indirect JMP instruction follows an ITR instruction, the operation is substantially modified. The contents of B01 and P13, which were stored when an interrupt was recognized, are returned to the Z-register during the ITR instruction. At the same time, the ITRFF flip-flop is set. These conditions prevail until TE1 of the indirect JMP instruction. At that time, P13 is reset by PR+ and B01 is reset by A33D. Then during TE3 BFZ is generated, which loads Z01 into B01 and Z03 into P13. The ITRFF flip-flop is cleared by BFZ and the interrupt return conditions are removed.

JST Instruction.—During a JST instruction the contents of the program counter are stored in the memory location identified by the effective address in the Y-register. Then the contents of the Y-register are loaded into the program counter and the program counter is incremented by one. The program continues from the new address in the program counter. If the instruction is indirectly addressed and the CPU contains the expanded address option, additional functions will be performed in the execute cycle. A description of the additional functions will be given below, following a description of the normal JST execute cycle.

At the start of TE1, MARP-A is generated to reset the memory address logic, and WR- is generated to reset the W-register (LBD 12.00). The contents of the program counter are gated onto the register bus by RBFP- via B34F (LBD 12.01). The output from B23D-11 goes passive (+6V), enabling B23E and allowing MCILC+ to go true (LBD 12.00). The next TCLK- pulse sets the MCI flip-flop, initiating a memory cycle. Gate C27D is conditioned (LBD 12.01) and the TCLK+B pulse generates RBTW- and RBTW+. The MREAD flip-flop is reset by RBTW- (LBD 12.00) and the clear/write memory mode is enabled. RBTW+ is routed to the W-register input gating logic, and the data on the register bus are loaded into the W-register via the dc set inputs (LBD 12.08). The memory cycle continues and the contents of the W-register (the instruction address plus one) are stored in the effective memory location.

The effective address in the Y-register is transferred to the program counter as follows: at the start of TE2, PR+ goes true (LBD 12.00), resetting the program counter. The contents of the Y-register are routed to the program counter input gating logic (LBD 12.06). DJG+ and TE3+A along with TCLK+B condition B24D (LBD 12.00), which generates YTP- and completes the transfer to the program counter.

The last function to be performed is the incrementing of the program counter. TE4+ and DJG+ condition B26K (LBD 12.00), which generates PADV-. The timer cycles through TE5 and TE6, after which the execute cycle is terminated and the next fetch cycle is started.

With the expanded address option the execution of an indirect JST causes the contents of B01 to be transferred to P13 and P13 to be transferred to B01 if this instruction does not follow an ITR instruction. The operations are performed in the same manner as the indirect JMP instruction.

The operations performed when an indirect JST instruction follows an ITR instruction are identical to the operations described in the indirect JMP instruction.

Interrupt Operation (See FTD 12.75)

General Operation.—The interrupt mode is initiated by the common interrupt input line, KINTL- (LBD 12.11). The signal is inverted to generate the external interrupt line signal, INTLC+, at C1401. Any device which generates an interrupt causes INTLC+ to go passive (+6V).

Interrupts may be either enabled by a previously programmed ENB instruction or inhibited by an INH instruction. These signals are decoded at the input of the ENB/INH flip-flop, C31A (LBD 12.03).

Timer pulse TE1+B sets the flip-flop during the decoded instruction. The active output at C31A-32 conditions one set input of the interrupt flip-flop, C31B-18. The reset input to the flip-flop is inhibited by the passive output of the ENB/INH flip-flop. An INH instruction is decoded at the ENB/INH flip-flop reset inputs (pins C31A-27 and -25) at time TE1+B. Interrupts are also inhibited upon generation of NCLR+, which is inverted at C26C-25 and applied to the dc reset input to the ENB/INH flip-flop. This flip-flop is also reset when the interrupt flip-flop is set by applying the active INTFF- signal to the dc reset input. INTFF-, therefore, inhibits new interrupts after an interrupt has been detected by the interrupt flip-flop. The program can reenable for new interrupts after the interrupt flip-flop has been reset by executing a new ENB instruction.

An interrupt may occur at any time and generate INTLC+. INTFF+, however, is generated at TF4 of a fetch cycle only if interrupts are enabled and it is not the first fetch of an indirectly addressed instruction. Execution of the present instruction continues unaltered until completion. At the next TF1 time, the RBFP- transfer is inhibited. Gate B34E-14 (LBD 12.01) normally generates the transfer strobe by gating a true (+6V) TF1+ signal and a false (+6V) INTFF-A signal. However, with INTFF-A in the true (0V) state, RBFP- is inhibited. TF1+ and TCLK+B are gated to produce an active (0V) signal at B34J-26, which generates active (+6V) RBTYU+ and RBTYL+ signals at the output of gates A35N-3 and A35P-2. With no data on the register bus, logical ZERO (reset state) is transferred into the Y-register (LBD 12.07). At TF2 time, gate C28-26, with active (+6V) TF2+ and INTFF+ inputs, goes active (0V) and generates YSY02- (LBD 12.03). YSY02- dc-sets bit Y02 of the Y-register. Thus, the address for the present fetch cycle is 00002, which is dedicated for entry to the interrupt program. The instruction at dedicated location 00002 must be either a direct or an indirect JST. INTFF is reset during TF4 of the actual interrupt cycle because the ENB/INH flip-flop (C31A) was reset by INTFF. This conditions the reset side of INTFF and allows resetting by the next TF4.

Interrupts With Expanded Address Option.—In processing interrupts with systems using the expanded (8K) memory option, it is necessary to save the bank bit and program counter bit P13 and to set the bank and P13 bits to zero. Saving these bits allows returning to the proper bank and program location of the next main program instruction after interrupt has been serviced. Resetting the bank bit and P13 enables the next fetch cycle to occur in dedicated location 00002 (lower bank) and all indirect references to be in the lower bank.

The Z-register stores the B-register bit and bit 13 of the P-counter for transfer into memory with ITS and STA instructions. INTFF and TF2 are gated at B14F-19, inverted by A26B-10, and applied to the clock inputs of the Z-register flip-flops (LBD 12.12). The B01± and P13± bits are applied to the set and reset inputs of Z-register flip-flops Z01 and Z03, respectively. Thus, the B-register bit (B01) is stored in Z01 and the program counter bit (P13) in Z03 during TF2 time. YSY02, in addition to its normal function of setting Y02, also resets Y13 because RBTYU transfer is blocked by B17D.

During TF3, B01 and P13 are reset by B14E and B14G, respectively.

Load Mode (See FTD 12.85)

Load mode transfers load 3-bit characters into the H112 controller for eventual storage in core as 12-bit packed words. Transfers occur over the programmed I/O bus under H112 hardware control, with no software program being executed. All load mode transfers are inputs to the controller.

Four transfers of 3-bit data characters are required to pack each location (the starting location is determined by the contents of the P-register when the function is initiated). Timing for transfers of data bits into the H112 is controlled by the transition of the KDB09- line from +6V to ground. This strobe signal from the input device may have a

period as short as 10 μs or as long as required by the sending device. The +6V to ground transition of KDB09- loads the three least significant bits of the I/O bus into the three most significant bits of the accumulator. The accumulator is then stored in the memory location determined by the P-register. On the next KDB09- ground-going transition, the following action occurs:

a. the accumulator (with the first character) is right-shifted three places;

b. the three least significant bits of the I/O bus are loaded into the three most significant bits of the accumulator;

c. the accumulator with both characters is stored in memory at the location determined by the P-register overwriting the previously stored character.

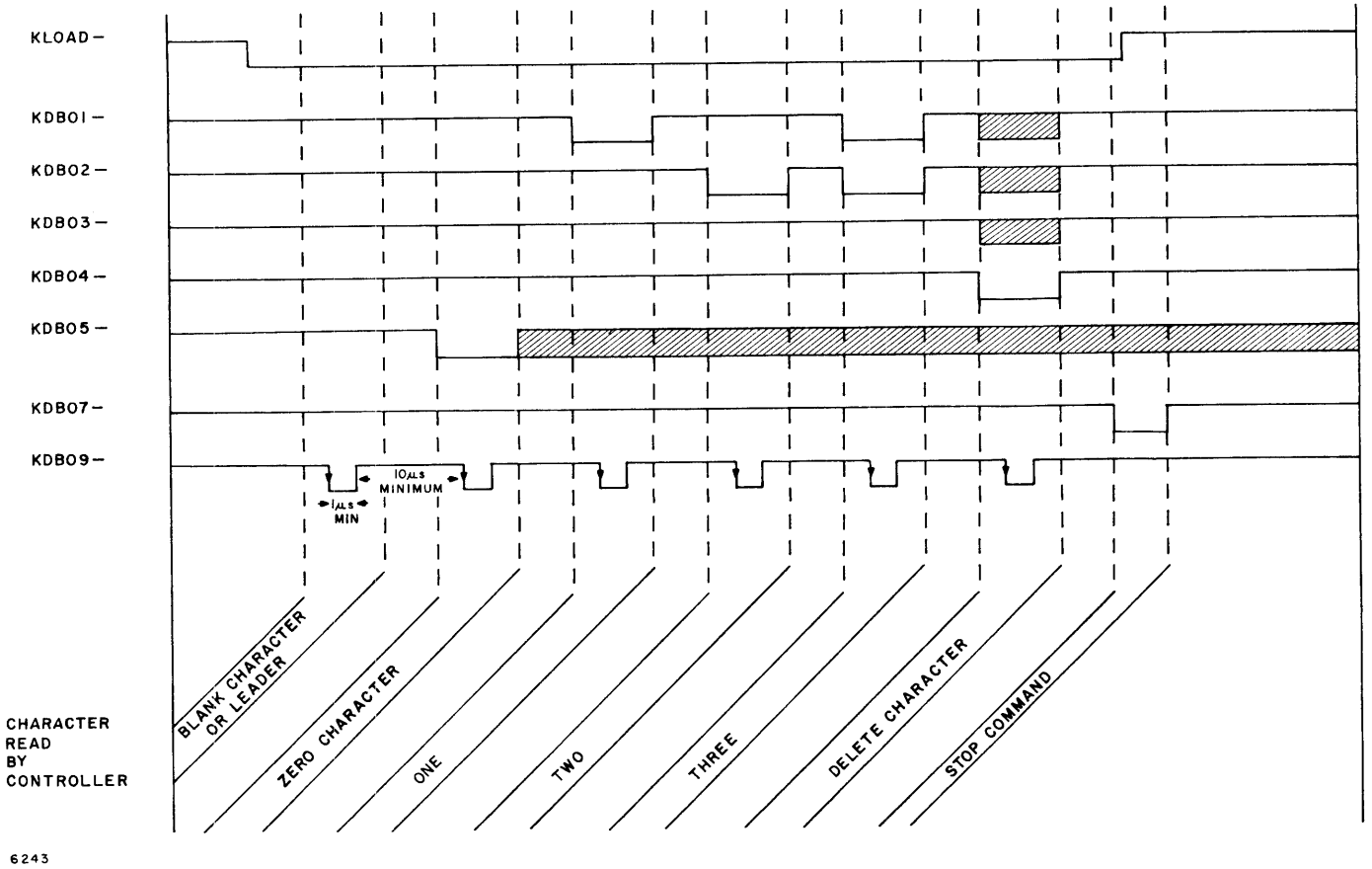
After four characters are stored in this memory location, the P-register is incremented and the next location is filled. Thus, to load a location with 4 3 2 1, the sequence of input characters must be 1 2 3 4. This sequence continues until a signal is recognized by the controller on KDB07-, which terminates the process. The remainder of the bit configuration included with the KDB07- signal is ignored.

Figure 3-6 shows the generation of data characters and control signals in their respective timing sequences.

Table 3-2 lists the load mode signal mnemonics, functions, and pin assignments. Data signals need be stable only during the KDB09- ground-going transition and 3 μs afterward. The states of KDB06, KDB08, KDB10, KDB11, and KDB12 are not important.

TABLE 3-2.
SIGNAL FUNCTIONS

Mnemonic	Function	Pin
KLOAD-	Load mode transfers. They are initiated by operation of the LOAD switch and START switch on the control panel or activation of the load line and start line from the machine control interface. When these conditions occur, the KLOAD- signal becomes active (ground) and remains active until the recognition of a stop command. After recognition of the stop signal, the KLOAD- line becomes passive (+6V). This output signal from the controller is to be used by the interface unit as a command to initiate transfers.	26
KDB01-	Least significant input bit of octal character. Passive (+6V) is defined as a ZERO, ground as a ONE. This signal must be passive during a blank character or leader.	1
KDB02-	Second most significant input bit of octal character. Passive (+6V) is defined as a ZERO, ground as a ONE. This signal must be passive during a blank character or leader.	2
KDB03-	Most significant input bit of octal character. Passive is defined as a ZERO, ground as a ONE. This signal must be passive during a blank character or leader.	3
KDB04-	When this input signal is active (ground) it is interpreted as a delete character signal, and causes the data character associated with it to be treated as a blank character or leader no matter what the character content.	4
KDB05-	This input signal must be passive (+6V) during a blank character or leader; when active (ground) it differentiates a ZERO character from a blank or leader.	5
KDB07-	When this input signal is made active (ground) it is interpreted as a stop command. It is not gated with the transition of KDB09- as is a data character. A pulse on this line at any time will stop the controller. This character cannot be deleted.	7
KDB09-	Transition from +6V to ground on this input line gates data character into the controller. This strobe pulse from the input device also causes shifting and storage of the accumulator and after every fourth shift, advancing of the program counter.	9



NOTE: OTHER OCTAL CHARACTERS NOT SHOWN IN THIS DIAGRAM REQUIRE THE CORRESPONDING BIT PATTERN ON LINES KDB01– THROUGH KDB03–; THE STATE OF KDB05– IS NOT IMPORTANT FOR OCTAL 1–7.

Figure 3-6. Timing for Load Mode

Since more than one device can be operated in the load mode and the controller does not select which device is to be read, each device must have a means by which the operator can select the desired device. The standard devices which can operate in the load mode are the input/output typewriter and the high-speed paper tape reader.

Load Mode Control Signals.—The load mode is initiated by activating the LOAD switch and the START switch on the control panel. The LOAD switch generates XLDSW-, which is inverted by C22N (LBD 12.04) to produce LLDSW+. LLDSW+ is gated with TRUN+ at B26G and then inverted by C22M to generate LLOAD+. TRUN is controlled by the timer start/stop logic, shown on LBD 12.02. The controller remains in the load mode as long as the LOAD switch is activated.

Data bus bits LDB01+ through LDB07+ are constantly monitored for the detection of delete, blank tape, or stop characters. Bit LDB09+ (the sprocket bit; LBD 12.04) is inverted and applied to the clock input of the sprocket stored flip-flop, A16B, to produce LSPKS±. LLDSW+ true (+6V) allows the flip-flop to set upon receipt of LDB09+. TF1- is applied to the dc reset input to clear the flip-flop once the fetch cycle has been initiated.

Blank tape (or leader) is detected by monitoring LDB01+ through LDB03+ and LDB05+ for false inputs. The signals are inverted and applied to AND gate B17C. If all signals are false, the gate output, LBLNK-, goes true (0V). LBLNK- also goes true when LDB04+ is true (+6V). A delete character (bit 4 = ONE) is thus treated as a blank character (bits 1, 2, 3, and 5 = ZERO). Channel 5 must always be a ONE to enable loading of a ZERO character. LBLNK- prevents loading data into the A-register, inhibits incrementing of the shift counter, inhibits the P-counter advance, and prevents shifting of the A-register data during that character.

LLOAD+ is inverted at C15-06 (LBD 12.11) to generate KLOAD-. This signal indicates activation of the load mode to the peripheral devices.

A stop (halt) code is detected when LDB07+ is true. With LLOAD+ and LDB07+ in the true (+6V) state, gate A23C (LBD 12.02) goes active (0V) and resets the TRUN flip-flop. With TRUN+ in the false (0V) state, LLOAD+ goes false (0V), thus terminating the load mode.

The simulated STA command is generated in the F-register (LBD 12.07) when XLDSW- dc-sets bit F10 of the F-register.

During TF1, TF2, and TF3, three ASHF± pulses are generated (LBD 12.00). These pulses shift the 3-bit data characters previously stored into the next lower 3 bits, thereby clearing bits 10-12 of the A-register for the transfer of the next character. ASHF- is generated by gating TF1- or TF2- or TF3- with LLOAD+, TCLK+B, and LBLNK- at B22C. LBLNK- prevents leader or blank spaces from entering memory.

Load Cycle Operations.—

a. *TF1.*—The transfer of the P-counter address to the Y-register is completed during TF1. TF1 generates RBFP- (LBD 12.01), which places the P-counter contents on the register bus. TF1 and TCLK generate RBTYU+ and RBTYL+, which transfer the P-register data from the register bus into the Y-register (LBD 12.07) at the end of TF1 time. TF1- is applied to the dc reset of the sprocket stored flip-flop, LSPKS (LBD 12.04). The flip-flop is reset, and LSPKS+ and LSPKS- go to their reset states. ASHF+ also shifts the A-register one place.

b. *TF2.*—During TF2, the A-register is again shifted one place, the read/write flip-flop (MREAD) is set to read, and the Memory Cycle Initiate (MCI) flip-flop is set. If the A-register contains four characters at the end of the loading of the present character, PADV is generated. TF2- sets the read/write flip-flop (LBD 12.00). The output of the flip-flop is inverted and applied to the memory as the MREAD+A signal. This signal is used for generating the memory strobe. TF2- is applied to gate B23-21, which generates MCILC+, thus conditioning the set input of the MCI flip-flop. The leading edge of TCLK- sets the MCI flip-flop, and MCI+ initiates the memory cycle. The program counter is incremented once every four input characters during the load mode. The shift counter (LBD 12.04) is used to count the number of characters that have been loaded into the A-register. PADV- is performed by gating shift counter bits C01+ and C02+ with time TF2+ at gate B22B (LBD 12.00).

c. *TF3.*—The shift counter (LBD 12.04) counts CCNT- pulses, which occur during each tape character input transfer. CCNT- is generated by gating

LLDSW+, the false state of LBLNK- (+6V), and TF3- at A13B (LBD 12.00). During TF3, the A-register is shifted one place, the W-register is cleared, and the shift counter is incremented one count. The W-register is reset by WR-. (B32B). WR- clears the W-register via the dc reset inputs (LBD 12.08).

d. *TF4.*—During TF4, the octal character on KDB01- through KDB03- is loaded into the A-register. KDB01- through KDB07- are inverted to produce LDB01+ through LDB07+ (LBD 12.10). Bits 01+ through 03+ are gated with LTB+ by B26M, N, and P (LBD 12.04) to register bus lines RB10- through RB12-. LTB+ is generated by gating LLDSW+ with TF4+ to produce LTB- at A14F (LBD 12.04). The signal is then inverted at C14-25 (LBD 12.11) to produce LTB+. RB10- through RB12- are inverted at B28K, B34C, and B34D (LBD 12.10) to produce RB10+ through RB12+. This data is gated with RBTA+ to load A-register bits 10 through 12. RBTA+ is generated by gating LLDSW+ and TF4+ with TCLK+B at B24F (LBD 12.01). The inverted signal at C26P is RBTA+.

e. *TE1 through TE3.*—The A-register data is stored in core memory by execution of a simulated STA instruction. XLDSW- is used to dc-set bit 10 of the F-register (LBD 12.07) to produce the STA Op Code. F-register bits 09 and 11 are decoded as ZEROs by gates B34G and B34H (LBD 12.05) to produce DJSSA+. This signal is gated with F-register bit F10+, TE1+B, and TCLK+B, and then inverted at C33N (LBD 12.01), to produce RBTW+. TE1+, DJSSA+, and F09-, which is in the false (+6V) state, are gated and then inverted to produce RBFA+ at C33P. With RBFA+ and RBTW+ true (+6V), the A-register contents are transferred to the W-register via the register bus. The simulated STA instruction execution exits in TE3, and the controller awaits a new character. A new load cycle is initiated by LSPKS as before.

Single Step Mode

The single step mode allows the operator to execute a program one instruction at a time and observe the contents of various registers at the end of each instruction. The operator initiates the fetch cycle of an instruction by pressing START. Upon completion of the execute cycle, the controller halts. The operator may then select particular registers for display and change their contents, if desired. The fetch cycle of the next instruction may then be initiated by pressing START again.

The single step mode is selected by first setting the RUN/STOP switch to the STOP position. The STOP position generates the XSS- signal and enables the remaining panel switches. XSS- is ORed with XXSS- (the remote panel RUN/STOP switch signal) and PSFLT- (the power supply failure signal) at A13H (LBD 12.02). The resulting signal is gated with XLDSW- (the load mode switch signal) at B15F, to generate TSS-. The signal is inverted at A15K to produce TSS+. This signal is gated with TSF1+ to generate the dc reset for the TRUN flip-flop (A23D).

The execution of a single step instruction is initiated by pressing START. The START switch generates XSRT± (XXSRT+ and XSRT- for remote panels), which activates the TRUN flip-flop. This enables the timer logic, which generates the instruction fetch and execute times.

During the final execute time, TSF1+ is generated. TSF1+ and TSS+ are then gated to produce the dc reset of the TRUN flip-flop, and the start of the next fetch is inhibited. The TRUN flip-flop then remains reset and inhibits the timer logic until the operator again presses START for a new instruction cycle.

Control Panel Functions

The control panel provides manual entry into the controller and allows registers to be displayed. A POWER ON/OFF function is also provided. Normal controller operation is enabled when the RUN/STOP switch is in the RUN position. Operation is then initiated by pressing START. All other control panel functions are disabled. The control panel is enabled by setting the RUN/STOP switch to STOP. All panel functions are then operative. The operation of each control and indicator is described below.

Panel Interface.—The control panel may be either permanently attached or portable. The two versions are identical in operation. LBDs 12.22 and 12.23 show all logic, controls, and indicators mounted on the control panel. Two cables connect the panel to the H112 mainframe: Panel connector A to A11, and Panel Connector B to B11. These connectors are shown on LBD 12.20. Connection of the portable panel is identical to that of the permanently mounted panel, except that the cable lengths are somewhat longer to allow convenient placement of the panel.

RUN/STOP Function.—The RUN/STOP switch selects normal (RUN) or single step (STOP) operation. When in the RUN position, XSS- goes false (+6V). As a result, A13H (LBD 12.02) goes true (all inputs +6V) and inhibits input B15F. The TSS- output (B15-20) goes false (+6V) and enables A17C. At this point, the timer operation is enabled and reentry into the fetch cycle is controlled by TSF1.

When the RUN/STOP switch is in the STOP position and the controller is stopped (as described under Single Stop Mode), single step operation is enabled. The timer operation is as previously discussed for this mode. In addition, this switch position enables the remaining panel switches. The power supply fault signal (PSFLT-), which is generated when the power supply detects a loss of primary ac power, may also stop the machine (A13H).

FETCH Function.—The FETCH switch, S10, generates XFTCH- when pressed. This switch is used to initiate a truncated fetch cycle of TF1 through TF4, which controls the memory read cycle. XFTCH- is ORed with XSTOR- at B15D (LBD 12.02). The resulting true signal is TFEST+, which is gated with TF4+ at A23E to produce TSTOP-. Enabling the fetch function includes first setting the RUN/STOP switch to STOP, depressing the FETCH switch, and initiating the fetch cycle by pressing START. The fetch cycle continues until TF4+ goes true (+6V). TF4+ and TFEST+ generate TSTOP-, which resets the TRUN flip-flop. TFEST+ is inverted at B18A, and the resulting ground signal inhibits the set input of the TF5 flip-flop. As a result, the fetch cycle terminates and the timer operation is inhibited by TRUN- false (+6V). The data is displayed in the W-register (LBD 12.08) and the P-register is incremented by B22E (LBD 12.00) as in a normal fetch.

STORE Function.—The STORE switch, S9, generates XSTOR- when pressed. This switch is used for loading the W-register data into a memory location specified by the P-register. Enabling of the store function includes setting the RUN/STOP switch to STOP and entering the address to be accessed in the P-register and data to be stored in the W-register. The transfer is initiated by depressing the STORE switch followed by the START switch. After the data is stored, the P-register is incremented as described under FETCH Function. STOR- is ORed with XFTCH- to generate TFEST+ at B15D (LBD 12.02). Operation of the timer logic and initiation of the memory cycle are identical to their counterparts in the fetch operation. However, the read cycle is inhibited by XSTOR-, which is applied to B17A (LBD 12.00). This causes MREAD+A at C26J to remain false for the duration of XSTOR-, which has the effect of clearing the addressed memory cell. XSTOR- also inhibits the W-register reset (B32B), allowing the data previously placed in it to be transferred to the addressed memory location.

MASTER CLEAR Function.—The MASTER CLEAR switch clears or presets all control, addressing, and I/O logic and all registers except the A- and W-registers. The switch is enabled by setting the RUN/STOP switch to the STOP position. The MASTER CLEAR switch (S7) is a momentary switch that generates XCLR- (LBD 12.22). XCLR- is applied to the system normalizer (C21-23) (LBD 12.11), which generates NCLR- (C21-31). The signal is inverted at C26K to produce NCLR+. NCLR+ is routed throughout the logic, as required, for proper initialization. NCLR+ is inverted at C15-22 to produce KXCLR- (LBD 12.11) for resetting external logic via the I/O bus.

Register Switches and Displays.—The control panel includes 13 data switches and 13 indicators, which are used for entering data into or reading data from the A-, P-, and W-registers. The switches are enabled by placing the RUN/STOP switch in the STOP position. The appropriate register is selected by depressing the A-, P-, or W-switches. The 13 data switches are used to enter ONEs into the selected register via XB01-XB13 (LBD 12.22 and 12.23). The CLEAR switch is used to clear the register. XB01- through XB12- are gated onto the register bus (LBD 12.10) as bits RB01+ through RB12+. These same signals are inverted to generate RB01-X through RB12-X for the panel display logic. XB13- is inverted twice to produce RB13- (LBD 12.12), for the expanded address option. RB13- is again inverted to produce RB13-X (A26-01) for the panel display logic.

The display logic gates and stores the RB01+X through RB13+X signals for the lamp display. The lamp display logic operates in both the run and the single step modes. During the run mode, the A-register will be displayed. In the single step mode, the selected register will be displayed.

Two control signals set and strobe the display register. XRGLD+ is the data strobe, which is true (+6V) only when RBTA-X and TRUN+X are present (LBD 12.23). When true (+6V), XRGLD+ conditions the data input gates, allowing register bus data to condition the data flip-flops. The flip-flops are preconditioned to the set state by XRGCL-. AR- is gated with TRUN+X to generate the XRGCL+ signal (LBD 12.22), which (after inversion) forces all the lamps to turn on. At this time, XRGLD+ is false (0V), effectively inhibiting entry of data into the display logic. After AR- returns to the passive (+6V) state, XRGCL- goes passive (+6V) and the lamps remain on. RBTA-X strobes data into the flip-flops. A logical ONE on the register bus (0V) does not cause a change of output state, and the lamp remains on. However, a logical ZERO on the register bus (+6V) resets the flip-flop and turns off the lamp.

In the stop mode, TRUN-X is false (+6V). This signal is inverted twice to produce XRGCL+. This inhibits the latching feature of the display flip-flops and allows the data on the register bus to drive the lamps. The register to be displayed is selected by the A-, P-, and W-switches.

The gating and display of bit 13 data are controlled by the RUN/STOP switch. ADOVF+ is always displayed when the switch is in the RUN position or when the A-register is being displayed (LBD 12.23). RB13+X is displayed when the switch is in the STOP position and the A-register is not being displayed. It is used for displaying P13 in an 8K system.

Register CLEAR Switch.—The CLEAR switch, a momentary contact type, is used for clearing registers when the controller is stopped. The RUN/STOP switch, when set to STOP, applies XSS- (0V) to the register CLEAR switch, S8. When pressed, the CLEAR switch supplies a ground signal to diode inputs CR1, CR2, and CR3. Diodes CR1 through CR3 gate the clear signal (0V) to REGISTER select switches A, P, and W. Depending upon which register is selected, the A-, P-, or W-switches generate AR-, XPR-, or WR- by grounding the appropriate signal line. AR- and WR- are applied directly to the dc reset inputs of the register flip-flops. XPR- is ORed at B23C (LBD 12.00) to generate PR+. PR+ is inverted at A27-11, A27-19, and A28-11 to produce dc resets for the P-register flip-flops (LBD 12.06).

REGISTER Select Switches A, P, and W.—These switches select the desired register for display and data entry (LBD 12.23). They are double-pole, double-throw types, with one section of each switch being used for the register clear function and the other section for the data gating function. Register display and manipulation (except A-register display) are possible only in the stop mode.

Depressing the A-register select switch, S13, generates XTABC-, which is ORed at C26P to generate RBTA+ and at C33P to generate RBFA+ (LBD 12.01). These signals place both the inputs and outputs of the A-register on the register bus. The register bus is displayed by the lamps when the machine is stopped.

Depressing the P-register select switch, S12, generates XTPBC-. This is inverted at B25J and applied to the logic to generate RBFP- (B25H) (LBD 12.01) and YTP- (B25K) (LBD 12.00). These signals gate the contents of the Y-register into the P-counter and the contents of the P-counter onto the register bus. The contents of the register bus are gated to the register by RBTYU+ and RBTYL+. These signals are generated continuously when the machine is stopped by C27E (LBD 12.01).

Depressing the W-register select switch, S11, generates XTWBC-. This is ORed at C33N to generate RBTW+, and at C32F and C32E to generate RBFWL+ and RBFWU+ (LBD 12.01). These signals gate the W-register data onto the register bus.

POWER Function.—The POWER circuit breaker applies primary power to the H112 dc power supply, fans, and convenience receptacle.

Remote Machine Control

Certain remote machine control functions may be supplied in normal system applications. These functions include START, RUN/STOP, LOAD, and MASTER CLEAR. A RUN indicator may be provided for displaying operational status. A POWER ON/OFF switch is also normally provided.

Remote control functions are applied to the H112 logic via Remote Panel Connector C11, shown on LBD 12.20. An example of how these functions could be supplied is shown in Figure 3-7. The functions shown are the same as those of the normal controls and functions previously dis-

cussed. Input signals are ORed with the normal control panel signals.

POWER DISTRIBUTION

AC primary power (115 Vac, 60 Hz) is applied to the H112 via the POWER circuit breaker on the control panel (see Figure 3-8). The circuit breaker outputs are routed to an ac convenience receptacle, the cooling fans, and the dc power supply input connections. For details of the dc power supply, see Appendix B.

MAJOR INSTRUCTION GROUP OPERATIONS

Tables 3-3 through 3-15 list the operations performed during the major instruction groups and identify the signal that performs these operations. The fetch cycle is common to all instructions and is performed before the execute cycle. Therefore, it is contained in a separate table and is not repeated. The indirect fetch cycle used during indirect addressing is also listed separately, in Table 3-4. Times do not include gate delays.

TABLE 3-3.
FETCH CYCLE OPERATIONS

Time	Operation	Signal Mnemonic	Origin (LBD)	Remarks
TF1	Transfer P to RB	RBFP	12.01	
	Transfer RB to Y	RBTYU	12.01	
		RBTYL	12.01	
TF2	Condition memory read	MREAD	12.00	
	Reset memory address	MARP	12.00	
	Initiate memory cycle	MCI	12.00	
	Increment P by one	PADV	12.00	
TF3	Reset W	WR	12.00	
	Transfer data from memory to W	MSW01-MSW12	12.08	Uses dc set inputs
TF4	Transfer Op Code to RB	RBFWU	12.01	
	Transfer RB to F	RBTF	12.01	
TF5	Transfer W-lower to RB	RBFWL	12.01	
	Transfer RB to Y-lower	RBTYL	12.01	
	Clear bits 8-12 of Y	RBTYU	12.01	Selects primary sector when W08 = ZERO
	Clear counter	CR	12.04	
	Set TICYL flip-flop	TF5	12.02	W12 = 1; W09-11 = 0
	Reset ADCRY flip-flop	TF5	12.02	

TABLE 3-4.
INDIRECT ADDRESSING OPERATIONS

Time	Operation	Signal Mnemonic	Origin (LBD)	Remarks
TF2	Condition memory read	MREAD	12.00	
	Reset memory address	MARP	12.00	
	Initiate memory cycle	MCI	12.00	
TF3	Reset W	WR	12.00	
	Transfer data from memory to W	MSW01-MSW12	12.08	Uses dc set inputs
TF5	Transfer W to RB	RBFWL	12.01	
		RBFWU	12.01	
	Transfer RB to Y and B01 to Y13	RBTYL	12.01	
		RBTYU	12.01	
	Clear counter	CR	12.04	

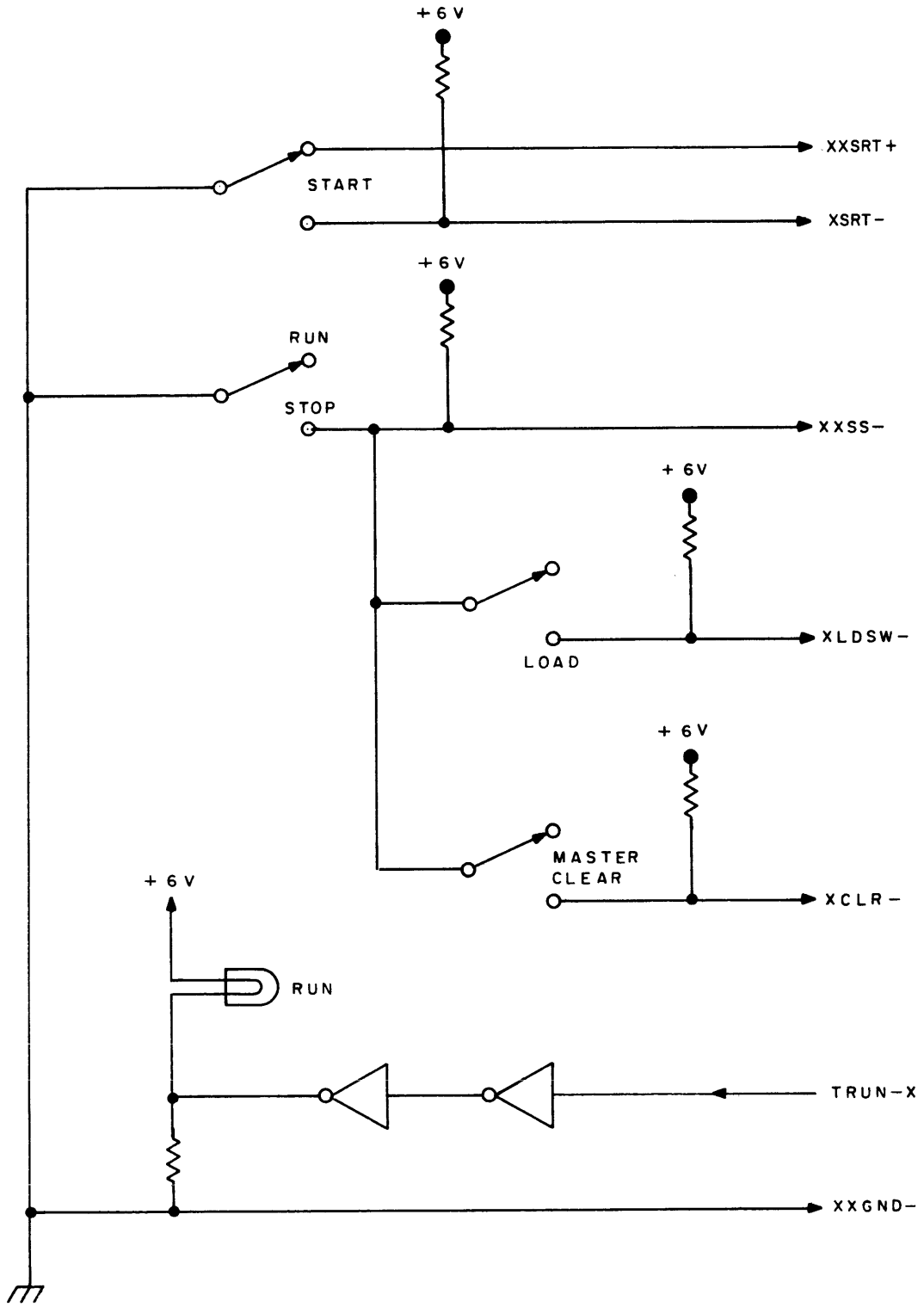


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Figure 3-7. Remote Control Functions

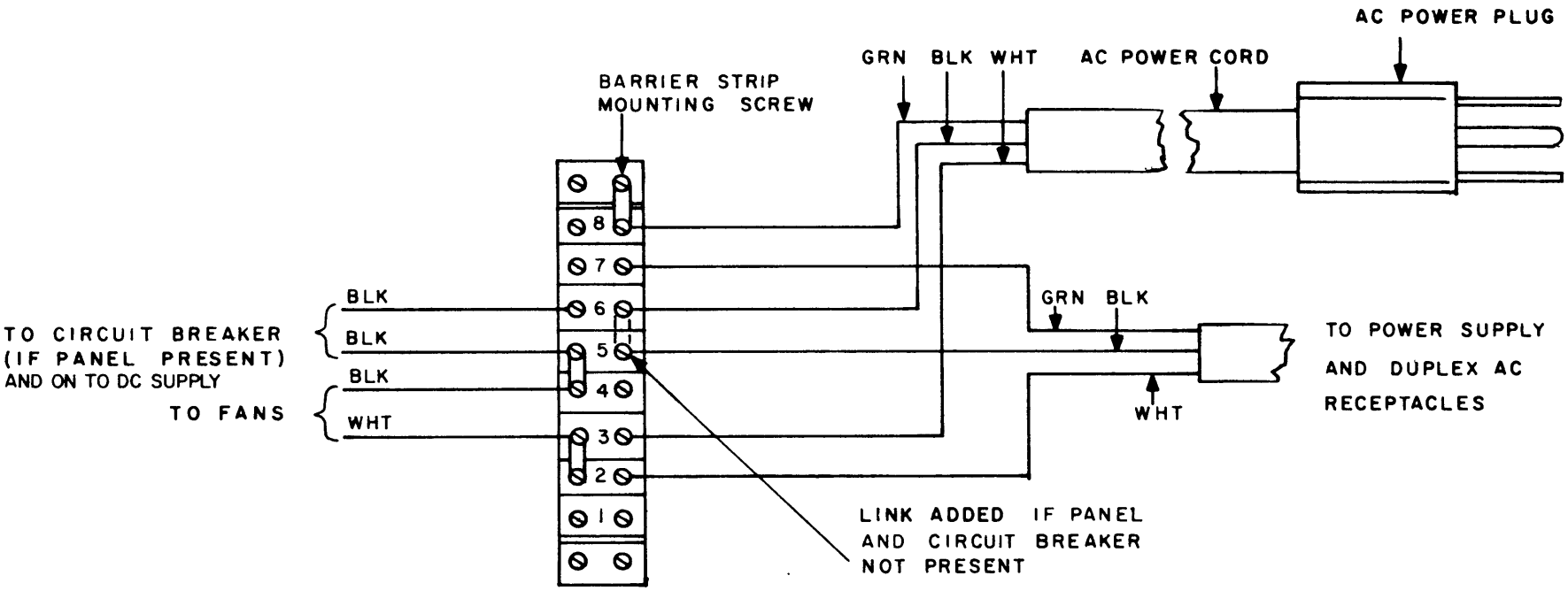


Figure 3-8. Primary Power Distribution

TABLE 3-5.
LDA OPERATIONS

Time	Operation	Signal Mnemonic	Origin (LBD)	Remarks
TE1	Reset memory address	MARP	12.00	
	Reset W	WR	12.00	
	Reset A	AR	12.00	
	Initiate memory cycle	MCI	12.00	
TE2	Transfer data from memory to W	MSW01-MSW12	12.08	Uses dc set inputs
TE3	Transfer W to RB	RBFWU	12.01	
		RBFWL	12.01	
	Transfer RB to A	RBTA	12.01	
	Exit execute cycle	TSF1	12.02	

TABLE 3-6.
STA OPERATIONS

Time	Operation	Signal Mnemonic	Origin (LBD)	Remarks
TE1	Reset W	WR	12.00	
	Reset memory address	MARP	12.00	
	Transfer A to RB	RBFA	12.01	
	Transfer RB to W	RBTW	12.01	
	Inhibit memory read	RBTW	12.01	Resets MREAD flip-flop
	Initiate memory cycle	MCI	12.00	
TE3	Exit execute cycle	TSF1	12.02	

TABLE 3-7.
JMP OPERATIONS

Time	Operation	Signal Mnemonic	Origin (LBD)	Remarks
TE1	Transfer P13 to B01	TE1+A	12.12	If it is indirect and does not follow an ITR
TE2	Reset program counter	PR	12.00	
TE3	Transfer Y to program counter	YTP	12.01	Inhibits Y13 to P13 if it is indirect and follows an ITR
	Transfer Z01 to B01 and Z03 to P13; reset ITRFF flip-flop	BFZ	12.12	If it is indirect and follows an ITR
	Exit execute cycle	TSF1	12.02	

TABLE 3-8.
ADD AND ANA OPERATIONS

Time	Operation	Signal Mnemonic	Origin (LBD)	Remarks
TE1	Reset memory address	MARP	12.00	
	Reset W	WR	12.00	
	Initiate memory cycle	MCI	12.00	
TE3	Increment shift counter	CCNT	12.00	
	Transfer data from memory to W	MSW01-MSW12	12.08	Uses dc set inputs
TE4	Shift A (A01 to A12)	ASHF	12.00	10 shifts are performed;
	Shift W (W01 to W12)	WSHF	12.00	ANA = ADD without carry
	Increment shift counter	CCNT	12.00	
	Inhibit reset input to TE4 flip-flop, set input to TE5 flip-flop, and set input to TF1 flip-flop	CEE4	12.04	Holds timer in TE4 time for 10 shifts
	Start next fetch cycle	TSF1 • CEE4	12.02	Timer starts after 10 shifts
TE5 & TF1	Shift A	ASHF	12.00	
	Shift W	WSHF	12.00	
TE6 & TF2	Shift A	ASHF	12.00	
	Shift W	WSHF	12.00	
TF4	Set ADOVF flip-flop		12.03	If ADCRY is set

TABLE 3-9.
IRS OPERATIONS

Time	Operation	Signal Mnemonic	Origin (LBD)	Remarks
TE1	Reset memory address	MARP	12.00	
	Set ADCRY flip-flop	TE1	12.03	Adds one to current value
	Reset W	WR	12.00	
	Initiate memory cycle	MCI	12.00	
TE2	Transfer data from memory to W	MSW01-MSW12	12.08	Uses dc set inputs
TE3	Inhibit reset input to TE4 flip-flop, set input to TE5 flip-flop, and set input to TF1 flip-flop	CEE4	12.04	Holds timer in TE4 for 12 shifts
	Increment shift counter	CCNT	12.00	
TE4	Shift W	WSHF	12.00	Perform 12 shifts
	Increment shift counter	CCNT	12.00	
	Increment program counter	PADV	12.00	Occurs only when ADCRY flip-flop is set and W01+ is true after 11 shifts
	Reset memory address	MARP	12.00	
	Inhibit memory read cycle	MREAD	12.00	
	Initiate memory cycle	MCI	12.00	
TE6	Exit execute cycle	TSF1	12.02	

TABLE 3-10.
I/O GROUP OPERATIONS

Time	Operation	Signal Mnemonic	Origin (LBD)	Remarks
	INA Instructions			
TF3	Address selected device	KABXX	12.11	
TF4	Enable INA line	D078•DIOG	12.05	
TE1	Reset accumulator	AR	12.00	
TE3	Set READY flip-flop	TSTLN•TE3	12.01	Occurs only when test line is true
TE4	Transfer data bus to RB	RBFDB	12.01	READY flip-flop must be set
	Transfer RB to accumulator	RBTA	12.01	
	Increment program counter	PADV	12.00	
TE5	Generate strobe	STRB	12.01	READY flip-flop must be set
TE6	Exit execute cycle	TSF1	12.02	
TF1	Reset strobe flip-flop	TF1	12.01	
TF2	Reset READY flip-flop	TF2	12.01	
TF3	Remove selected device address	WR	12.00	
	Disable INA line	WR	12.00	
	OTA Instructions			
TF3	Address selected device	KABXX	12.11	
TF4	Enable OTA line	D278	12.05	
	Transfer A to data bus	KDBFA	12.10	
TE3	Set READY flip-flop	TSTLN•TE3	12.01	Occurs only when test line is true
TE4	Increment program counter	PADV	12.00	READY flip-flop must be set
TE5	Generate strobe	STRB	12.01	READY flip-flop must be set
TE6	Exit execute cycle	TSF1	12.02	
TF1	Reset strobe flip-flop	TF1	12.01	
TF2	Reset READY flip-flop	TF2	12.01	
TF3	Remove selected device address	WR	12.00	
	Disable OTA line	WR	12.00	
	OCP and SMK Instructions			
TF3	Address selected device	KABXX	12.11	
TF4	Enable OCP line	D378	12.05	
	Transfer A to data bus	KDBFA	12.10	
TE5	Generate strobe	STRB	12.01	
	Generate SMK strobe	SMK	12.11	SMK only
TE6	Exit execute cycle	TSF1	12.02	
TF1	Reset strobe flip-flop and disable SMK line	TF1	12.01	
TF3	Remove selected device address	WR	12.00	
	Disable OCP line	WR	12.00	
	SKS Instructions			
TF3	Address selected device	KABXX	12.11	
TF4	Enable SKS line	D178	12.05	
TE3	Set READY flip-flop	TSTLN•TE3	12.01	Occurs only when test line is true
TE4	Increment program counter	PADV	12.00	READY flip-flop must be set
TE5	Generate strobe	STRB	12.01	READY flip-flop must be set
TE6	Exit execute cycle	TSF1	12.02	
TF1	Reset strobe flip-flop	TF1	12.01	
TF2	Reset READY flip-flop	TF2	12.01	
TF3	Remove selected device address	WR	12.00	
	Disable SKS line	WR	12.00	

TABLE 3-11.
GENERIC GROUP OPERATIONS

Time	Operation	Signal Mnemonic	Origin (LBD)	Remarks
	TAB Instructions			
TE1	Reset bank	TE1	12.12	
	Exit execute cycle	TSF1	12.02	
TF1	Transfer A01 to bank	BFA	12.12	
	ITR Instructions			
TE1	Reset Z	TE1	12.12	
	Exit execute cycle	TSF1	12.02	
TF1	Transfer A01 and A03 to Z	ZFA	12.12	
	Set ITRFF flip-flop	ZFA	12.12	
	ENB Instructions			
TE1	Exit execute cycle	TSF1	12.02	
	Set interrupt enable flip-flop	TE1	12.03	
	INH Instructions			
TE1	Exit execute cycle	TSF1	12.02	
	Reset interrupt enable flip-flop	TE1	12.03	
	Reset INTFF	NCLR-A	12.03	
	CRA Instructions			
TE1	Reset accumulator	AR	12.00	
	Exit execute cycle	TSF1	12.02	
	TBA Instructions			
TE1	Reset accumulator	AR	12.00	
TE3	Transfer bank to A01	BTA	12.12	Used dc sets
	Exit execute cycle	TSF1	12.02	
	Transfer P13 to Bank	TE3+A	12.12	
	ITS Instructions			
TE1	Reset accumulator	AR	12.00	
TE3	Transfer Z to A01 and A03	ZTA	12.12	Uses dc sets
	Exit execute cycle	TSF1	12.02	
	TOA Instructions			
TE1	Reset accumulator	AR	12.00	
TE2	Transfer overflow to A01	ASA01	12.03	
TE3	Reset overflow flip-flop	TE3+A	12.03	
	Exit execute cycle	TSF1	12.02	
	STL Instructions			
TE2	Inhibit set input to TE3 flip-flop	STALN	12.02	Remains in TE2 until STALN- goes true
	Inhibit reset input to TE2 flip-flop	TE3	12.02	Remains until end of TE3 time
TE3	Exit execute cycle	TSF1	12.02	
	HLT Instruction			
TE1	Reset run flip-flop	TSTOP	12.02	
	Exit execute cycle	TSF1	12.02	
	OCA/TCA Instructions			
TE1	Set ADCRY flip-flop	TE1	12.02	TCA only
TE3	Increment shift counter	CCNT	12.00	
TE4	Shift A (10 shifts performed)	ASHF	12.00	OCA—All bits inverted TCA—All bits following first ONE are inverted
	Increment shift counter	CCNT	12.00	
	Inhibit reset input to TE4 flip-flop, set input to TE5 flip-flop, and set input to TF1 flip-flop	CEE4	12.04	Holds timer in TE4 time for 10 shifts
	Start next fetch cycle	TSF1·CEE4	12.02	Timer starts after 10 shifts
TE5 & TF1	Shift A	ASHF	12.00	
TE6 & TF2	Shift A	ASHF	12.00	

TABLE 3-12.
SHIFT INSTRUCTION OPERATIONS

Time	Operation	Signal Mnemonic	Origin (LBD)	Remarks
TE1	Transfer W01-W07 to RB	RBFWL	12.01	
	Transfer RB01-RB04 to shift counter	RBTC	12.01	Loads the ONE's complement of the required number of shifts
TE3	Increment shift counter	CCNT	12.00	
TE4	Shift A	ASHF	12.00	LGR—A is shifted to right and ZEROs fill in from left RAR—A01 shifted into A12 ARS—A is shifted to right and sign bit is shifted in from left
	Increment shift counter	CCNT	12.00	
	Inhibit reset input to TE4 flip-flop, set input to TE5 flip-flop, and set input to TF1 flip-flop	CEE4	12.02	
	Start next fetch cycle	TSF1·CEE4	12.02	
TF1 & TE5	Inhibit shift	—	—	ASHF is inhibited
TF2 TE6	Inhibit shift	—	—	ASHF is inhibited

TABLE 3-13.
JST OPERATIONS

Time	Operation	Signal Mnemonic	Origin (LBD)	Remarks
TE1	Reset W	WR	12.00	
	Reset memory address	MARP	12.00	
	Transfer P13 to B01	TE1	12.12	If it is indirect and does not follow an ITR
	Transfer program counter to RB	RBFP	12.01	
	Transfer RB to W; reset MREAD flip-flop	RBTW	12.01	
	Initiate memory cycle	MCI	12.00	
TE2	Reset program counter	PR	12.00	
TE3	Transfer Y to program counter	YTP	12.01	Inhibits Y13 to P13 if it is indirect and follows an ITR
	Transfer Z01 to B01 and Z03 to P13; reset ITRFF flip-flop	BFZ	12.12	If it is indirect and follows an ITR
TE4	Increment program counter	PADV	12.00	
TE6	Exit execute cycle	TSF1	12.02	

TABLE 3-14.
LOAD MODE OPERATIONS

Time	Operation	Signal Mnemonic	Origin (LBD)	Remarks
TF1	Shift A right one place	ASHF	12.00	First shift
	Transfer P to RB	RBFP	12.01	
	Transfer RB to Y upper	RBTYU	12.01	
	Transfer RB to Y lower	RBTYL	12.01	
	Reset LSPKS flip-flop	TF1	12.02	
TF2	Shift A right one place	ASHF	12.00	Second shift
	Condition memory read	MREAD	12.00	
	Initiate memory cycle	MCI	12.00	
	Advance P every fourth character	(PADV)	12.00	PADV if C01 and C02 set
TF3	Shift A right one place	ASHF	12.00	Third shift
	Reset W	WR	12.00	
	Increment counter	CCNT	12.00	
TF4	Transfer RB to A	RBTA	12.01	
	Transfer LDB to RB	LTB	12.04	
	Inhibit RBTF and RBFWU	XLDSW-	12.01	
TE1	Reset W	WR	12.00	Simulated STA
	Transfer A to RB	RBFA	12.01	
	Transfer RB to W	RBTW	12.01	
	Inhibit memory read	RBTW	12.01	
	Initiate memory cycle	MCI	12.00	
TE3	Exit execute cycle	TSF1	12.02	

TABLE 3-15.
INTERRUPT OPERATIONS

Time	Operation	Signal Mnemonic	Origin (LBD)	Remarks
TF1	Register bus to Y upper	RBTYU	12.01	Clear Y upper
	Register bus to Y lower	RBTYL	12.01	Clear Y lower
TF2	Condition memory read	MREAD	12.00	
	Initiate memory cycle	MCI	12.00	
	Initialize Y	YSY02	12.03	Force Y to location 00002
	Transfer B01 to Z01 and P13 to Z03	TF2	12.12	Save B01 and P13
TF3	W-reset	WR	12.00	
	Reset B01 and P13	TF3	12.12	
TF4	Register bus from W upper	RBFWU	12.01	
	Register bus to F	RBTF	12.01	
	Reset INTFF	TF4	12.03	
TF5	Register bus from W lower	RBFWL	12.01	
	Register bus from W upper	RBFWU	12.01	
	Register bus to Y lower	RBTYL	12.01	
	Register bus to Y upper	RBTYU	12.01	
	Enter indirect JST fetch	TICLC	12.02	If indirect
	Clear counter	CR	12.04	

SECTION IV
SIGNAL MNEMONICS

The pertinent areas of the H112 have mnemonics chosen to have meaning to the user. The first one or two letters of the mnemonic indicate the primary area of the logic (the accumulator, the adder, the various registers, etc.) with which the function is associated. For example, the register bus control logic gates register data to and from the register bus. The mnemonics, therefore, are RBTX or RBFX; indicating Register Bus To and From register X, respectively.

The letters following the prefix letter (or letters) define the purpose of the function within its major area. For example, DIAG means Decoder, Input to Accumulator Group. Numbers following the prefix letter (or letters) indicate such things as the bit within a register or a bus or decoder bits. For example, A03 is bit 3 of the accumulator and DO78 is Decoder, bits 7 and 8 equal to octal zero. The plus (+) or minus (-) sign at the end of each mnemonic indicates the assertion or negation, respectively, of the function. The minus sign essentially inverts the meaning of the mnemonic. For example, TRUN+ is +6V when the machine is running, while TRUN- is +6V when the machine is stopped.

A letter sometimes follows the sign at the end of the mnemonic. This letter indicates that the function is repeated and that there are two or more driving sources for the same function. This technique is usually used when too many loads for a single driving source are encountered. For example, TE3+ and TE3+A both perform the same logic function, but TE3+A is a repeated or buffered TE3+ line.

A listing of the signal mnemonic prefixes and the definition of each are given in Table 4-1.

TABLE 4-1
SIGNAL MNEMONIC PREFIXES

Prefix	Definition
A	Accumulator (A-Register)
AD	Adder
B	Bank Register
C	Counter (Shift Counter)
D	Decoder
F	Function Register (Op Code)
H	High Speed Data Channel (Direct Data Channel)
INT	Interrupt
K	Cable Signals (I/O Bus)
L	Load Mode
M	Memory
P	Program Counter (P-Register)
RB	Register Bus
T	Timer
W	W-Register)
X	Panel Signals
Y	Memory Address Register (Y-Register)
Z	Z-Register

Table 4-2 shows the H112 mnemonics in alphanumeric order in the left column, the corresponding signal name in the center column, and the source of the signal associated with the mnemonic in the right column.

TABLE 4-2.
FUNCTION LIST

Mnemonic	Name	Origin (LBD)
A01–A12	Accumulator, bits 1 through 12	12.09
ADOVF	Adder, overflow flip-flop	12.03
ADCRY	Adder, carry flip-flop	12.03
ADSUM	Adder sum	12.03
AEZ	Accumulator equals zero	12.09
AR	Accumulator, reset	12.00,08,23
ASA01	Accumulator, set accumulator, bit 1	12.03,12
ASA03	Accumulator, set accumulator, bit 3	12.12
ASHF	Accumulator, shift signal	12.00,08
B01	Bank register, bit 1	12.12
BFA	Bank register from accumulator	12.12
BFZ	Bank register from Z-register	12.12
BTA	Bank register to accumulator	12.12
C01–C04	Counter, bits 1 through 4	12.00,04
CCNT	Counter, count signal	12.00
CEE4	Counter, exit, execute time 4	12.03,04
CTT	Counter to timer	12.00
D078	Decoder, bits 7 and 8 equal binary 0 (bit 8=ZERO, bit 7=ZERO)	12.05
D178	Decoder, bits 7 and 8 equal binary 1 (bit 8=ZERO, bit 7=ONE)	12.05
D278	Decoder, bits 7 and 8 equal binary 2 (bit 8=ONE, bit 7=ZERO)	12.05
D378	Decoder, bits 7 and 8 equal binary 3 (bit 8=ONE, bit 7=ONE)	12.05
DG78Z	Decoder, bits 7 through 12 are ZEROs	12.05
DGEN	Decoder, generic (non-memory reference) group	12.05
DGG5	Decoder, generic (non-memory reference) group with bit 5=ONE	12.05
DGG6	Decoder, generic (non-memory reference) group with bit 6=ONE	12.05
DGGG	Decoder, general generic group (excluding I/O instructions)	12.05
DIAG	Decoder, input to accumulator group	12.05
DIJG	Decoder, indirect jump group	12.05
DINA	Decoder, input to accumulator (INA)	12.05
DIOG	Decoder, input/output instruction group	12.05
DIRS	Decoder, increment, replace, and skip (IRS)	12.05
DJG	Decoder, jump group (JMP, JST)	12.05
DLDA	Decoder, load accumulator (LDA)	12.05
DOCA	Decoder, ONE's complement instruction (OCA)	12.05
DSHFT	Decoder, shift instructions	12.05
DSKP	Decoder, skip instructions	12.05
DTCA	Decoder, TWO's complement instruction (TCA)	12.05
F09–F12	Function (Op Code) register, bits 9 through 12	12.07
HAB01–HAB13	High speed, address, bits 1 through 13	12.25
HACKA	High speed acknowledge, subchannel A	12.24
HACKB	High speed acknowledge, subchannel B	12.24
HADST	High speed, address strobe	12.24
HCINP	High speed, cycle in process	12.24
HCRLA	High speed, cycle request, line A	12.24
HCRLB	High speed, cycle request, line B	12.24
HCYCL	High speed, data channel cycling	12.24
HDSTA	High speed, data strobe to subchannel A	12.24

TABLE 4-2. (CONT)
FUNCTION LIST

Mnemonic	Name	Origin (LBD)
HDSTB	High speed, data strobe to subchannel B	12.24
HEOPC	High speed, end of present cycle	12.24
HFSTC	High speed, first half cycle	12.24
H101A–H113A	High speed, I/O address, bits 1 through 13, subchannel A	12.24
H101B–H113B	High speed, I/O address, bits 1 through 13, subchannel B	12.24
HIDTA	High speed, input data time, subchannel A	12.24
HIDTB	High speed, input data time, subchannel B	12.24
HIDST	High speed, input data strobe	12.24
HINFC	High speed, input mode, first cycle	12.24
HINLA	High speed, input line, subchannel A	12.24
HINLB	High speed, input line, subchannel B	12.24
HINMD	High speed, input mode	12.24
HODT	High speed, output data time	12.24
HREQA	High speed, request storage, subchannel A	12.24
HREQB	High speed, request storage, subchannel B	12.24
INTFF	Interrupt flip-flop	12.03
INTLC	External interrupt line, conditioned	12.11
ITRFF	Interrupt return flip-flop	12.12
KAB01–KAB06	Cable, address bus, bits 1 through 6	12.11,20
KDBFA	Cable, data bus from accumulator	12.10
KDB01–KDB12	Cable, data bus, bits 1 through 12	12.10,20
KGND	Cable, ground	12.20
KINAL	Cable, input transfer to A line	12.11,20
KLOAD	Cable, load mode line	12.11,20
KOCPL	Cable, output control pulse line	12.11,20
KOTAL	Cable, output transfer from A line	12.11,20
KPWFL	Cable, power supply fault line	12.11,20
KSKSL	Cable, skip if set line	12.11,20
KSMKL	Cable, set mask line	12.11,20
KSTAL	Cable, stall line	12.11,20
KSTRB	Cable, strobe line	12.11,20
KXCLR	Cable, master clear line	12.11,20
KTSTL	Cable, test line	12.11,20
LBLNK	Load mode, blank tape (bits 1,2,3,5 are ZERO or bit 4=ZERO)	12.04
LDB01–LDB12	Load mode, bits from data bus to load logic	12.04,10
LLDSW	Load mode, load switch from panel	12.04
LLOAD	Load mode, load signal to device	12.04
LSPKS	Load mode, sprocket stored flip-flop	12.04
M6V	Memory, minus 6V	12.13
MARP	Memory, address reset pulse	12.00
MBSY	Memory, busy signal	12.13
MCI	Memory, cycle initiate	12.00
MCILC	Memory, cycle initiate flip-flop level control	12.00
MINHB	Memory, inhibit line	12.14
MREAD	Memory, read/write flip-flop	12.00
MRTDL	Memory, reset timing delay line	12.13
MRWSP	Memory, read/write pulse	12.13
MRZ01–MRZ12	Memory, inhibit winding terminator resistors	12.16
MSRWP	Memory, memory cycle read/write pulse	12.13
MSTRB	Memory, strobe core signal	12.13
MSW01–MSW12	Memory, set W-register bits 1 through 12	12.15

TABLE 4-2. (CONT)
FUNCTION LIST

Mnemonic	Name	Origin (LBD)
MUNSL	Memory, unit select	12.14
MWIHB	Memory, write inhibit	12.14
MWRIT	Memory, write enable	12.13
MXB01–MXB08	Memory, X-selection outputs, 1 through 8	12.17
MXC08	Memory, delay line tap C08	12.13
MXC24	Memory, delay line tap C24	12.13
MXC26	Memory, delay line tap C26	12.13
MXC28	Memory, delay line tap C28	12.13
MXC32	Memory, delay line tap C32	12.13
MXCSR	Memory, X-current source resistor	12.17
MXD01–MXD16	Memory, X-drive selection lines, 1 through 16	12.17
MXRSW	Memory, X-read switch signal	12.14
MXRWT	Memory, X-matrix selection strobe	12.13
MXWSW	Memory, X-write switch signal	12.14
MXYRE	Memory, X and Y, read enable	12.14
MXYWE	Memory, Y-read, X- and Y-write enable	12.14
MYB01–MYB08	Memory, Y-selection outputs, 1 through 8	12.18
MYCSR	Memory, Y-current source, resistor	12.18
MYD01–MYD16	Memory, Y-drive selection lines, 1 through 16	12.18
MYRWT	Memory, Y-matrix selection strobe	12.13
MZW01–MZW12	Memory, inhibit windings	12.16
NCLR	Normalizer, clear (from switch or system normalizer PAC)	12.11
P01–P12	Program counter, bits 1 through 12	12.06
PADV	Program counter, advance	12.00
PR	Program counter, reset	12.00
PSFLT	Power supply, fault signal	12.02
RB01–RB13	Register bus bits 1 through 13	12.04,06,08, 09,10,12
RBFA	Register bus from accumulator	12.01
RBFDB	Register bus from data bus	12.01
RBFP	Register bus from program counter	12.01
RBFWL	Register bus from W-lower (bits 1 through 7)	12.01
RBFWU	Register bus from W-upper (bits 8 through 12)	12.01
RBTA	Register bus to accumulator	12.01
RBTC	Register bus to counter	12.01
RBTF	Register bus to function register	12.01
RBTWU	Register bus to W-upper (bits 8 through 12)	12.01
RBTWL	Register bus to W-lower (bits 1 through 7)	12.01
RBTYH	Register bus to Y, halt	12.01
RBTYU	Register bus to Y-upper (bits 8 through 13)	12.01
RBTYL	Register bus to Y-lower (bits 1 through 7)	12.01
READY	Test line ready flip-flop	12.01
SMK	Set mask instruction decode	12.01
STALN	Stall line	12.02,11
STRB	Strobe for I/O instructions	12.01
TCLK	Timer, master clock	12.02
TE1–TE5	Timer, execute times 1 through 5	12.02
TF1–TF6	Timer, fetch times 1 through 6	12.02
TFEST	Timer, fetch and store	12.02
TICLC	Timer, indirect cycle flip-flop, level control	12.02
TICYL	Timer, indirect cycle flip-flop	12.02

TABLE 4-2. (CONT)
FUNCTION LIST

Mnemonic	Name	Origin (LBD)
TRUN	Timer, run flip-flop	12.02
TRUNS	Timer, run synchronized flip-flop	12.02
TSF1	Timer, start fetch time 1	12.02
TSFLT	Timer, power supply fault signal, repeated	12.02
TSS	Timer, single step	12.02
TSTLN	Test line	12.11
TSTOP	Timer, stop pulse	12.02
TZERO	Timer, bits 2 through 6 of W-register = ZERO	12.02
VOLT6	Plus six volts	12.20
W01–W12	Working register, bits 1 through 12	12.08
WR	Working register, reset	12.00,08,23
WSHF	Working register, shift signal	12.00,08
XB01–XB13	Control panel to register bus, bits 1 through 13	12.20,22,23
XCLR	Panel, clear	12.20,22
XFTCH	Panel, fetch	12.20,22
XGND	Panel, ground	12.20,22,23
XLDSW	Panel, load switch (control panel)	12.20,22
XLT7	Panel, panel lamp No. 7	12.20,22,23
XPR	Panel, program counter reset	12.20,23
XRGCL	Panel, display register clear	12.20,22,23
XRGLD	Panel, control panel register set	12.20,22,23
XSRT	Panel, start	12.20,22
XSS	Panel, single step	12.20,23
XSTOR	Panel, store	12.20,23
XTABC	Panel to accumulator bus control	12.20,23
XTPBC	Panel to program counter bus control	12.20,23
XTWBC	Panel to W-register bus control	12.20,23
XXGND	Remote panel, ground	12.20
XXSRT	Remote panel, start	12.20
XXSS	Remote panel, single step/stop	12.20
Y01–Y13	Y-register, bits 1 through 13	12.07,12
YSY02	Y-register, set Y-register, bit 2	12.03
YTP	Y-register to program counter	12.00,12
Z01,Z03	Z-register, bits 1 and 3	12.12
ZFA	Z-register from accumulator	12.12
ZTA	Z-register to accumulator	12.12

SECTION V
H112 MAGNETIC CORE MEMORY

This section contains instructions for proper operation and maintenance of the H112 4096-Word Magnetic Core Memory Module, and information on the installation of the expansion 4K memory.

DESCRIPTION

The H112 Magnetic Core Memory Module is a high-speed digital storage device capable of storing a maximum of 12 bits of information in 4096 locations, expandable to 8192 locations. Data is stored in an array of 30 mil ferrite cores. An address is selected by use of conventional four-wire coincident-current techniques. The switching time of the cores and the frequency characteristics of the driving and logic circuitry permit a full-cycle time of 1.69 μs and an access time of 0.53 μs. The memory does not contain a data register or a timing generator. Memory address signals are received from the address bus at the beginning of any memory operation. The appropriate timing signals are also received and the selection of a location is accomplished in the memory core array. During a memory load (clear/write) cycle, data is supplied to the memory from the computer and stored at the selected address. During a memory unload (read/regenerate) cycle, the data word at the selected location is first transferred to the computer and then regenerated (rewritten) into the core array.

System Layout

The system consists of a modular connector BLOC assembly, holding groups of μ-PACs. The solderless wrap connector assembly is a single piece of molded, glass-filled phenolic capable of holding eight μ-PACs. The memory module is contained in three connector assemblies arranged in a 1 x 3 connector plane.

The core stack is a plug-in unit requiring six μ-PAC connectors, three on each side (Figure 5-1). The stack assembly is made up of four glass epoxy boards, each containing four core mats of 4096 cores interconnected to make a stack of 12-bit words.

Specifications

Capacity

4K randomly addressable 12-bit words, expandable to 8K in a 4K increment.

Storage Mode

Coincident-current magnetic core array (3D, 4-wire)

X0 through X63	X-Drive Line
Y0 through Y63	Y-Drive Line

Cycle Time	*Access Time*	*Input/Output Levels*
1.69 μs	0.53 μs (max)	Passive: 3.5 to 6.3V Active: 0 to 0.5V

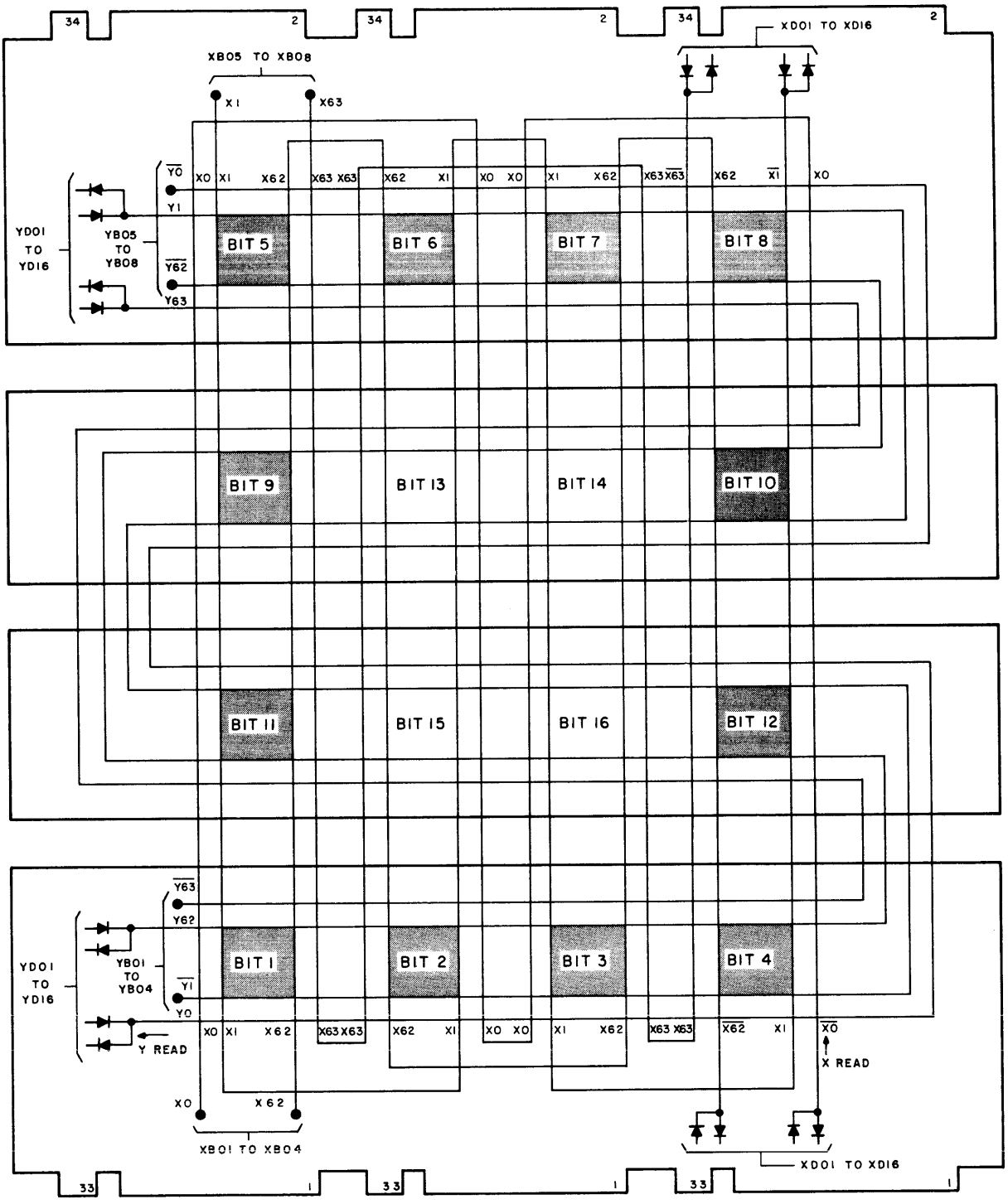
Memory Cycle Timing

For each cycle, the computer must provide the memory with an address and a read or write indication, and the timing circuits (located outside the memory) with a start signal. Once the cycle is initiated, another cycle cannot start until 1.69 μs has elapsed. During a read cycle, information is available no more than 0.53 μs (access time) after the cycle is initiated. If the memory is performing a write cycle, information must be made available to the memory within 0.7 μs after cycle initiate.

PRINCIPLES OF OPERATION

Principles of Magnetic Core Memories

Magnetic Core Storage.—The memory core stack, housed in the magnetic core unit, is a matrix configuration of individual ferrite cores (30-mil



NOTE: IN THE 12-BIT MEMORY STACK, CORE MATS 13 THROUGH 16 ARE NOT USED.

Figure 5-1. Stack Coding Diagram

OD, 18-mil ID). Basically, the ferrite core is a 1-bit storage element in the form of a ferrite ceramic ring that can be magnetically saturated to either positive or negative flux orientation. An important characteristic of the core is that the ferrite material retains a large part of the magnetic flux developed at the time the core is saturated. The time required to switch a core from one polarity to another depends primarily on the core material and size.

One similarity between the magnetic core and the flip-flop is that both provide storage for 1 bit of data. The two extremes of saturation in a magnetic core represent ZERO and ONE, as do the two stable states of a flip-flop. A core can be set to a ONE state by the application of a current pulse in a particular direction in a wire through the core and can be reset by a current pulse of similar magnitude in the opposite direction in the wire. Similarly, a flip-flop is set or reset by applying pulses to the appropriate inputs. Both the magnetic core and the flip-flop provide storage of the last state applied, but the core does so without requiring power to hold the state.

The ferrite core has a nearly rectangular hysteresis loop. The hysteresis loop is a graphical representation of the flux density produced in a magnetic material, plotted against the magnetizing force that produces it. Figure 5-2 is a simplified drawing showing the generation of a typical ferrite core hysteresis loop. Starting with an unmagnetized core, an increase in magnetizing current (H) increases the flux density (B) along the S-shaped curve (5-2A). The flux density levels off when the core is saturated, and any additional current applied does not appreciably increase the flux density, because the core material is supporting as much flux as it can. As the current is decreased and then made to flow in the opposite direction, the flux does not collapse along the same line (5-2B), and most of the flux remains even after the current has fallen to zero. The amount of flux actually remaining is a function of the retentivity of the magnetic material. As a magnetizing current is applied in the opposite direction, it has little effect on the flux level until the current reaches the knee of the hysteresis loop.

A slight increase in current beyond the knee of the curve switches the core rapidly to negative saturation (5-2C). The point on the curve representing the amount of current required to change the state of the core is termed the coercive current. When the negative magnetizing current is removed, most of the flux is retained as before (5-2D). Note that the original sweep from a magnetically neutral condition is never repeated (5-2E). A memory core in coincident-current use is never in a neutral condition, but is switched from one saturated state to the other. The core is thus an extremely useful binary component because it can exist in either of two stable states and can switch rapidly from one to the other.

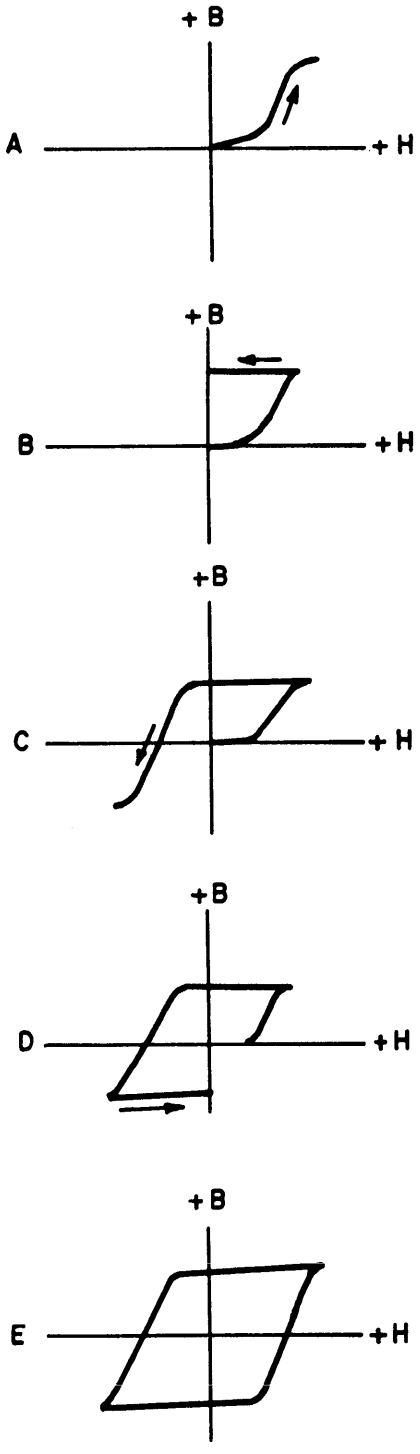
For any given toroidal magnetic core, the necessary magnetomotive force required to effect switching is a function of the product of the number of turns of wire and the current driven through those turns. It is not economically feasible to wind multiple turns of wire around the small toroidal cores used in core memories. Rather the number of turns is reduced to two, one in each of the perpendicular driving coordinates, and the current in these coordinate wires is of such a magnitude as to cause switching (rapid flux change) to occur.

In addition to the perpendicular (X and Y) coordinate selection lines, each core is threaded by two other wires, each of which passes through every core in a plane. One is the sense winding, which detects flux change due to switching of a core and thus provides a readout signal from the plane. The other is the inhibit winding, which as its name suggests, inhibits the writing of a ONE into the core, thereby causing ZERO to be stored. A single memory core, with its associated control windings, is illustrated in Figure 5-3.

A disadvantage of the memory core is that it does not provide a static indication of its state, as does a flip-flop. To obtain an indication of the condition of the flux in a memory core, the state of the core must be switched.

Information Sensing.—Sense lines allow the reading of information stored in the cores. One sense line (Figure 5-3) is threaded through all memory cores of each mat.

To read any of the words stored in memory, half-currents in the proper direction are generated in the selected X- and Y-lines (Figure 5-4). The read half-currents combine at the coincident junction of the X- and Y-lines to change the state of the affected core in each memory mat. If the affected core is storing a ONE at that instant, the effect of the read half-currents will change the state of the core to ZERO. If the core was



As Positive Current Increases Rising Flux Density is Limited by Core Saturation

Most of the Flux Remains after the Current is Removed.

As Negative Current Reaches the Switching Point, the Core is Driven to Negative Saturation

As with Positive Current, when Negative Current is Removed, Most of the Flux Remains

Thus, the Core is always Saturated in the Positive or Negative Direction

Figure 5-2. Ferrite Core Hysteresis Loop

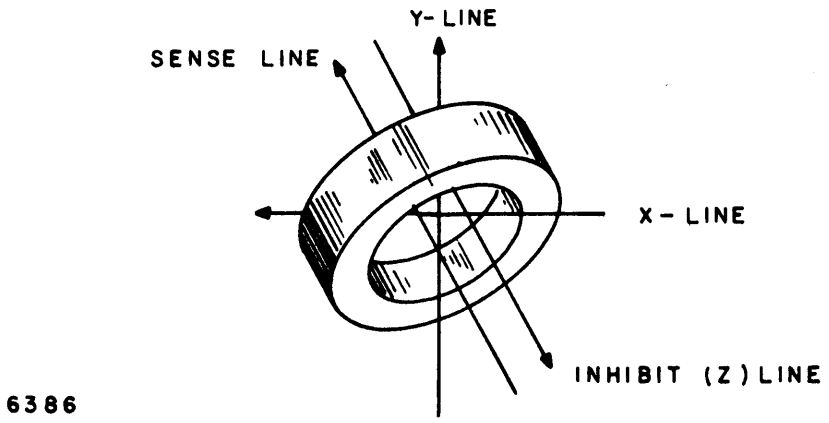


Figure 5-3. Core Control Windings

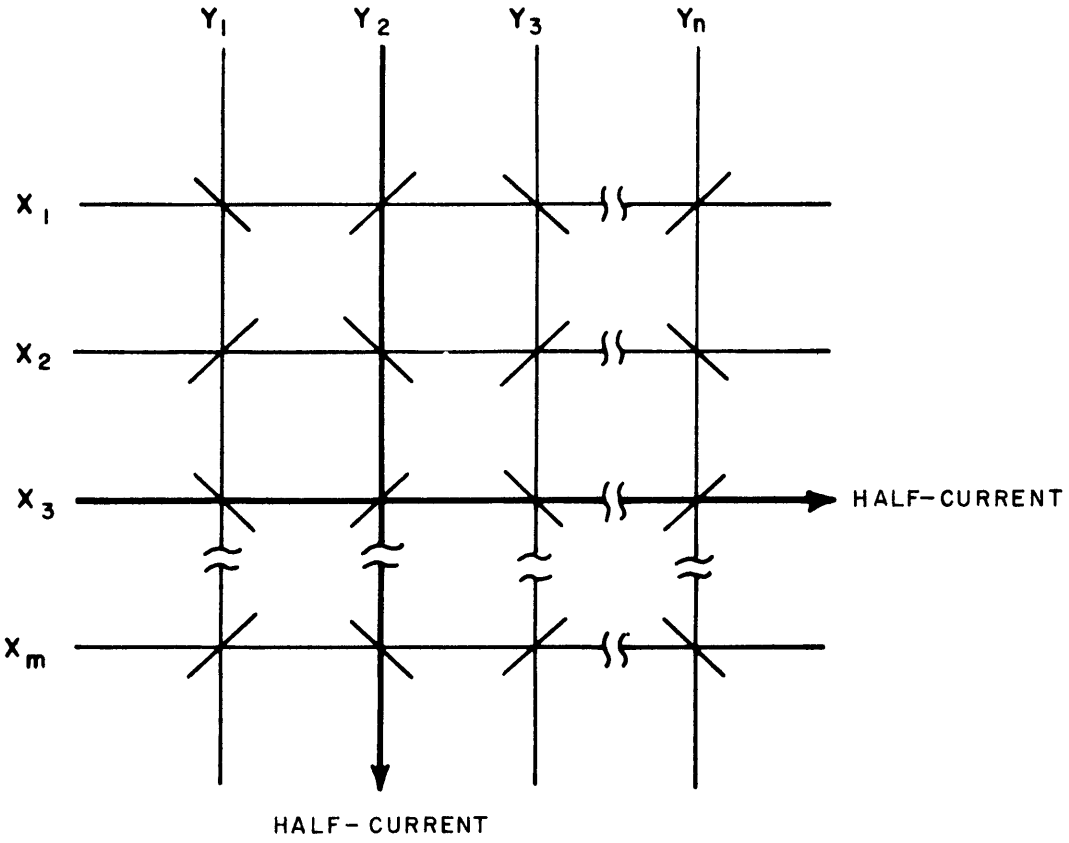


Figure 5-4. Coincident-Current Selection

previously in the ZERO state, the read half-currents will have no effect on the core. When the core is switched from the ONE to the ZERO state, the rapid change in flux from positive saturation to negative saturation induces a voltage pulse in the corresponding sense line. Therefore, the presence of a voltage pulse in the sense line during the read operation indicates that a ONE has been stored in the indicated core. If no voltage pulse occurs in a sense line during a read operation, a ZERO is indicated. The sense lines designated MWS01+ through MWS12+ in the memory core stack are connected to sense amplifiers. A ONE input to any of the sense amplifiers is amplified and applied to the W-register. Thus, output data is transferred from its storage location in the core stack to the W-register.

Addressing.—The complete core stack for a magnetic core unit consists of a number of individual matrices or mats. Each mat contains memory cores assembled in a rectangular configuration. The memory cores are threaded by X- and Y-lines in each mat so that one memory core is physically located at each junction of an X-line and Y-line.

As previously stated, pulses of current applied along the X- and Y-lines switch a memory core from one state to another. If one-half of the current required to switch a core is applied along the X-line, and one-half of the necessary current is applied along the Y-line, the core situated at the junction of the energized X- and Y-lines will receive the full switching current. This type of operation is termed coincident-current operation.

A coincident-current magnetic core memory depends upon the coincidence of two half-currents to read data from or to write data into the cores. Two additive half-current pulses will set the core to the ONE state, while two half-current pulses applied in the opposite direction will reset the core to the ZERO state. A half-current applied to one line without a similar half-current applied to the other line has no effect on the core.

Only one X-line and one Y-line of a mat are energized during a single cycle, and only that core situated at the junction of the activated X- and Y-lines will respond. Therefore, only one core in each mat will be affected during a single cycle. A simplified diagram of coincident-current selection of a memory core is illustrated in Figure 5-4.

In coincident-current memories, the X- and Y-lines are wired in series through all mats of the memory core array. Energizing one of the X-lines (designated X_1 through X_m in Figure 5-4) supplies a half-current pulse to the appropriate row of cores in every mat. Similarly, energizing one of the Y-lines (designated Y_1 through Y_n), supplies a half-current pulse to the appropriate column of cores in every plane. When pulses occur simultaneously on two lines (X and Y), they select the same core position in each of the planes. Therefore, the X- and Y-lines select a word in the memory core array and enable read or write operations.

Writing.—Inhibit lines enable a computer word or instruction to be written into memory at a selected address location. A single inhibit line is threaded through each memory core in a mat (Figure 5-3) and each mat of the magnetic core stack requires an individual inhibit line.

To write information into memory, half-current pulses in the direction opposite to those generated for read operation are applied to the selected X- and Y-coincident junction to switch the affected core in each memory plane.

Since all the cores at the selected address have been cleared to the ZERO state prior to the application of the write half-currents, these currents operate to switch all cores to the ONE state. If the incoming data dictates that a ZERO is to be written into a specific core, some means must be used to prevent the core from switching to the ONE state when the write currents are generated. This is accomplished by the inhibit (Z) lines, designated MZW01+ through MZW12+. An inhibit pulse, when transmitted through the inhibit line of the memory plane at the same time that the write half-currents are applied through the X- and Y-lines, prevents the writing of a ONE because the inhibit current subtracts from the X- and Y-write currents.

The inhibit pulse is of the same magnitude as, but opposite in polarity to, a write half-current pulse. Therefore, it directly cancels the effect of one write half-current pulse. Thus two write half-current pulses and one inhibit pulse are equivalent to a single write half-current pulse on the addressed core. This prevents the core from switching from the ZERO to the ONE state.

Information to be written into memory is stored in the W-register prior to being transferred to the memory core stack. During the transfer operation, a passive (+6V) signal from the register flip-flop

prevents the generation of an inhibit pulse, whereas an active (0V) signal from the register flip-flop allows an inhibit pulse to be generated. In this way information is rewritten (or new information is written) into the selected memory location exactly as it appears in the W-register.

Addressing and Selection

Addressing – Random Access.–The memory address buffer consists of cross-coupled power gates located on the CM-306 Selector μ-PAC. Data received from the 12 single-ended address input lines (Y01- through Y12-) will feed these power gates, and a reset pulse (MARP-A) will disable the gates under certain conditions. The outputs of the gates control the drive line selection circuits. Appendix A contains a detailed description of this μ-PAC.

Decoding and Selection.–Figure 5-5 is a simplified diagram of the address decoding and selection for a typical bit of a 4K memory. Three address bits are transferred to the X switches and three others to the X sinks. The X switches uniquely enable one of eight read/write line pairs going to the diode matrix. The X sinks select one of eight read/write buses. The selected bus enables one end of eight drive lines, each of which has its other end connected to an enabled diode matrix. Thus, only one of 64 X-lines has been selected. The Y-line selection is accomplished in a similar manner.

Figure 5-6 is a simplified schematic diagram of the X decoding and selection matrix. Two diodes per line isolate a single line when selected. Consider a read/regenerate cycle involving drive line X60. During the read portion of the cycle, X read switch (Q1) and X read sink (Q4) are selected by related address buffer outputs. These selection outputs are turned on when read timing pulses MXRSW- for the switch and MXYRE- for the sink go to 0V. Read current then flows in line X60 from +15.5V through R1, Q1, CR1, CR2, X60, and Q4 to ground. Read current ceases to flow when signals MXRSW- and MXYRE- return to +6V. During the write portion of the cycle the addresses do not change. Write timing pulses MXYSE- for the sinks and MXWSW- for the switches are generated. When these signals go to 0V, sink Q2 and switch Q3 are turned on. Write current then flows from +15.5V through R1, Q3, CR3, line X60, CR4, and Q2 to ground. Write current ceases when signals MXYWE- and MXWSW- return to +6V. At the end of the cycle the addresses will change, and in a similar manner, the remainder of the X-lines will be selected.

The Y-selection matrix is similar to the one described except that it is driven by the decoding of different addresses and command signals. For a detailed description of the CM-306 Selector μ-PAC, refer to Appendix A.

Timing and Control

See Volume II for the flow and timing diagrams and the logic block diagrams that illustrate the logical functions associated with the control and distribution of memory timing pulses and internal and interface timing.

Operating Modes

Read/Regenerate Mode.–The memory timing distribution (see Volume II, LBD 12.13) receives a cycle initiate command (MCI+), which is ANDed with the Memory Busy Signal (MSRWP-). If the memory is engaged in a cycle, the MBSY+ signal prevents the initiation of a new cycle. When MBSY+ is at 0V a flip-flop is set by MCI+, the reset side of which sends a negative pulse down a 400 ns delay line. Appropriate taps along this delay line are jumpered to power amplifier inputs to generate the timing pulses. A read command (MREAD+A) is received and ANDed with the MWRIT- signal and the appropriate delay line taps, to form a sense amplifier strobe signal (MSTRB-) during READ time. When the Selector μ-PAC control pulses (MXRSW- and MXYRE-) are generated, the sinks and switches are turned on (LBD 12.14). Stored data present in the addressed location is read out (Figure 5-7). The strobe (MSTRB-) samples the data. If a ONE was stored at that address, the sense amplifier associated with that bit produces an output, setting the data registers. The set side of the data registers (WXX+) is presented to the input of the inhibit drivers and disables it. If a ZERO was stored at that address, no output occurs. The data register remains reset and enables the inhibit drivers. When the read pulse reaches the end of the delay line, MRTDL- resets the timing distributor flip-flop, terminating the pulse train. The flip-flop is set once more by A35F (LBD 12.13), which sends a second negative pulse down the line to start the write cycle timing. The Selector μ-PAC control pulses (MXRSW- and MXYWE-) are generated, and X- and Y-line currents are once again established (LBD 12.14). When the inhibit pulse (MINHB+) is

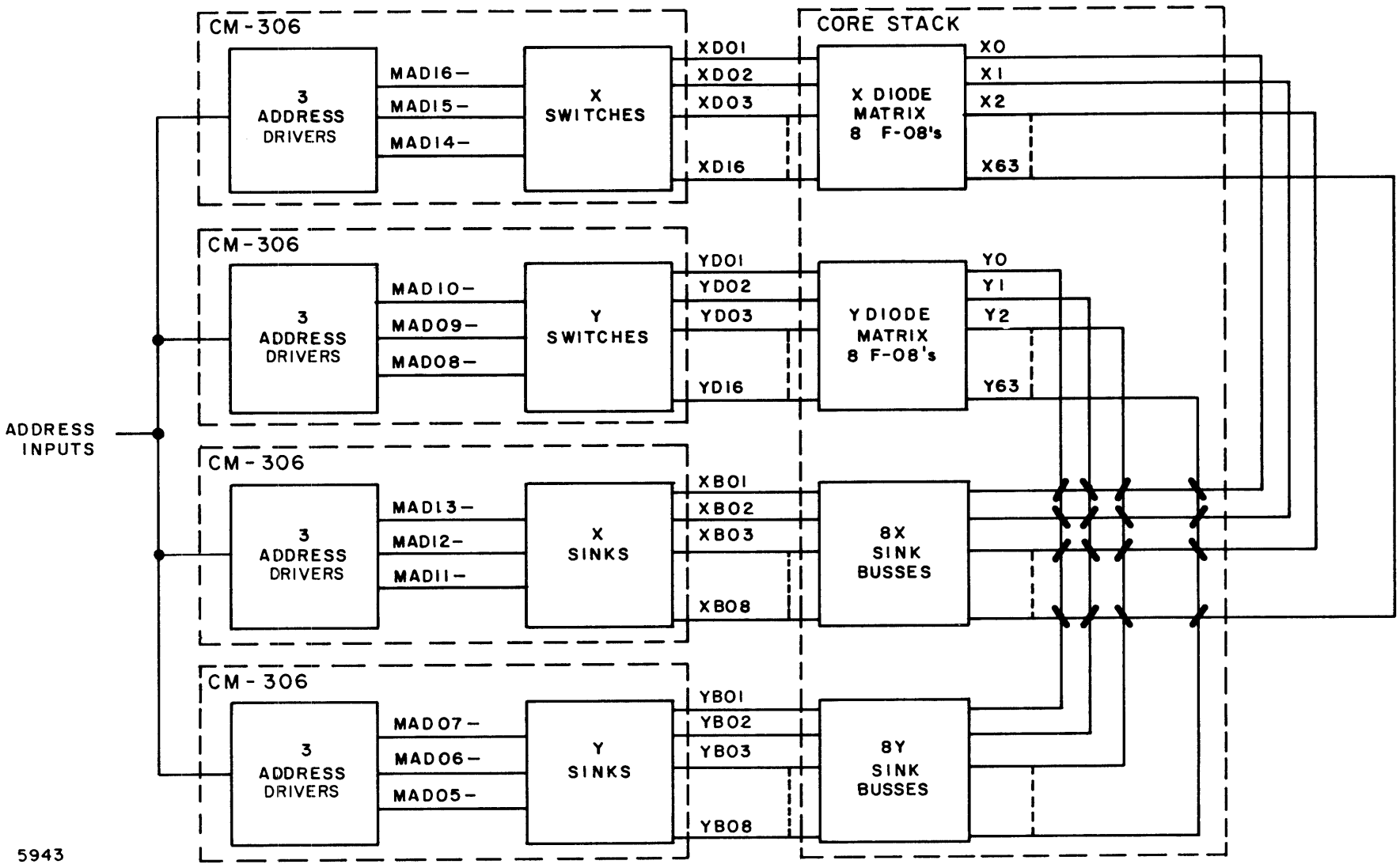


Figure 5-5. Simplified Block Diagram of Address Decoding and Selection

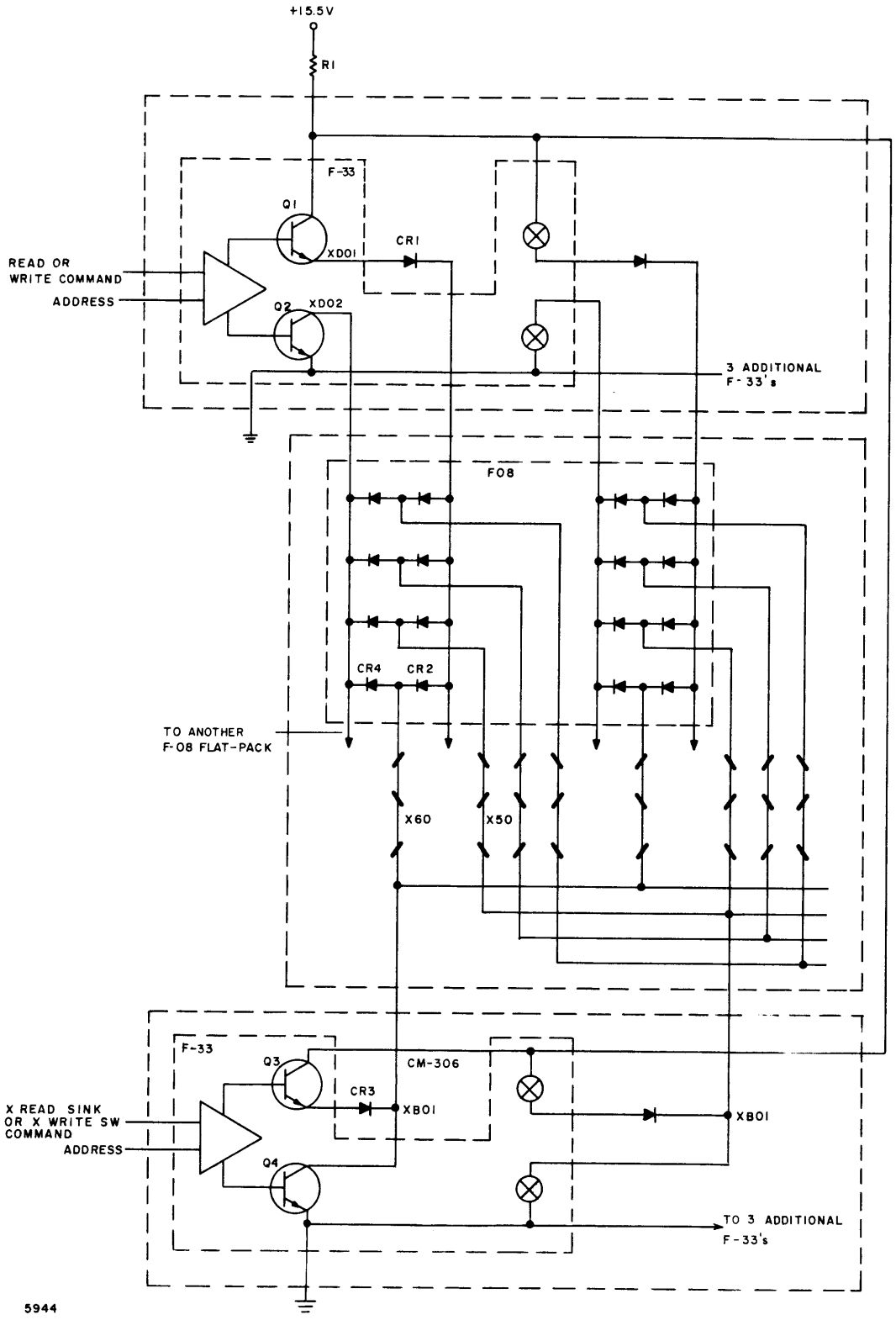


Figure 5-6. Simplified Schematic of Decoding and Selection Matrix

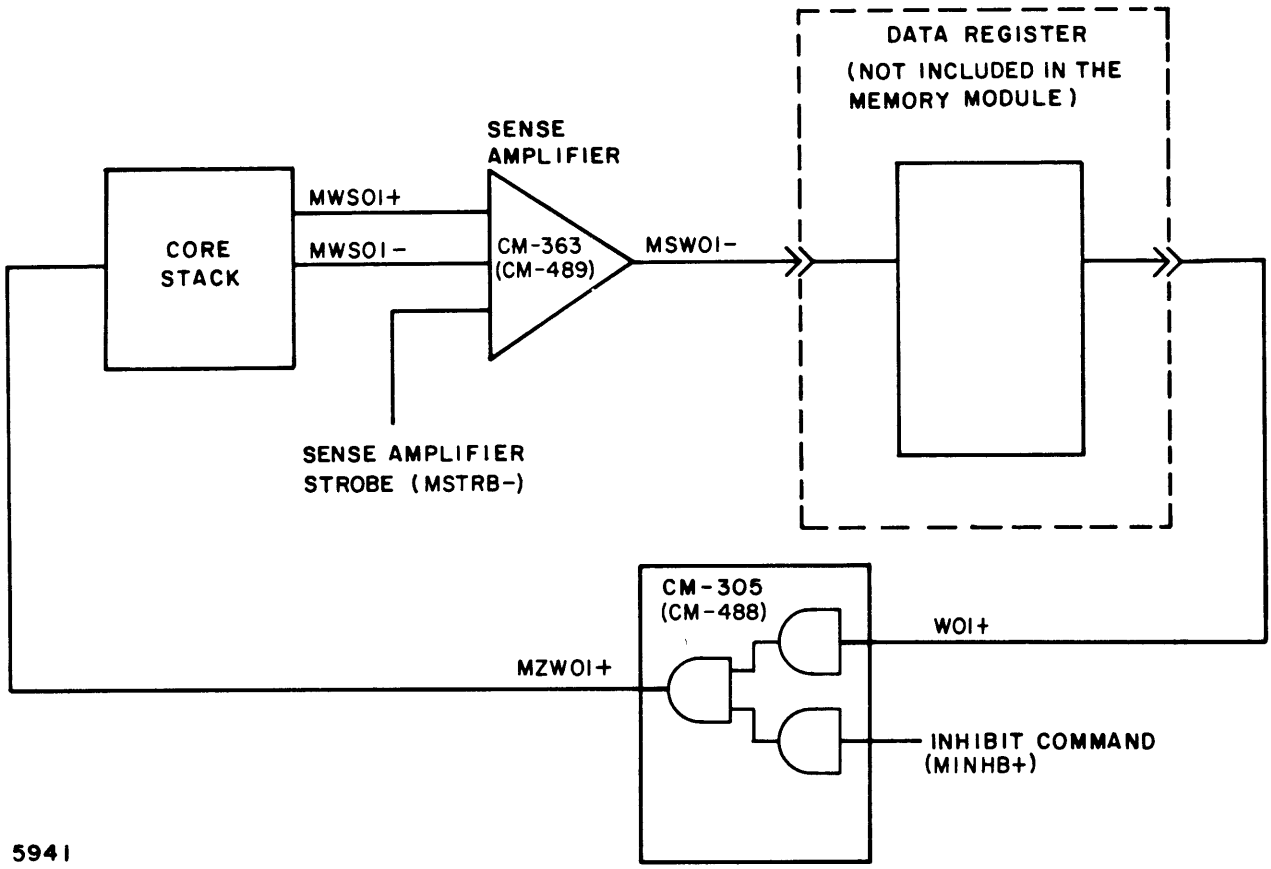


Figure 5-7. Simplified Diagram of Regeneration Loop

generated, a ONE is written in the stack if the inhibit drivers were disabled. A ZERO is written if the drivers were enabled.

Clear/Write Mode.—The clear/write mode operation is identical to the read/regenerate mode, except for the sense amplifier strobe. The read command is not enabled, and therefore the strobe signal is not generated. Without the sense amplifier strobe, data stored in a selected address is not loaded into the W-register. During the write portion of the cycle, new information stored in the W-register is written into the addressed location as was described in the discussion of the read/regenerate mode.

Interface Timing

The interface timing for the read/regenerate and clear/write modes is shown in Volume II. The timing distributor does not form an integral part of the memory system. Therefore, with the exception of signals MXYRE-, MXYWE-, MXRSW-, and MXWSW-, all signals, whether used internally or as commands, are classified as interface signals.

The MCI+ pulse starts a read/regenerate cycle or a clear/write cycle. The address inputs (Y01- through Y12-) must be present for all cycles at the leading edge of MCI+ inputs and remain stable for the duration shown on the interface timing diagram. The data lines (W01+ through W12+) must be stable for the duration of the MINHB+ pulse as defined on the timing diagram for a read/regenerate or clear/write cycle.

Voltage Sequencing

The turn-on sequencing of the main power supply is designed to allow the +15 voltage to remain off until the +6V and -6V logic supplies are stabilized. Similarly, the +15V supply is turned off before the logic supplies are turned off. This ensures that no current can flow during the power supply turn-on and turn-off transients which might change data previously stored in the core array.

INSTALLATION OF EXPANSION MEMORY

The 4K Expansion Memory Module, Model 112-03, contains the following items: a 1 x 3 memory module (including μ-PACs and stack); two ribbon jumper cables; wires for power distribution; screws for mounting; and five μ-PACs, to be added in the mainframe, which provide the optional instructions.

Physically, the 1 x 3 memory module mounts in locations A5, B5, and C5 (see Figure 5-8). The unit is secured with the mounting screws provided. Figure 5-9 shows module dimensions and Heyco connector locations.

The locations for plugging in the five optional μ-PACs and the electrical connections required are given in Tables 5-1 and 5-2.

TABLE 5-1.
LOCATION OF OPTIONAL μ-PACs

Optional μ-PAC	Location (LBD 12.21)
TG-320	A26
DI-320	A25
FA-320	A24
DF-320	A33
DF-320	B14

TABLE 5-2.
LOCATION OF ELECTRICAL CONNECTIONS

Ribbon Jumpers	Location (LBD 12.21)
1. Jumper μ-PAC A014998701	A52 → A47
2. Jumper μ-PAC A014998702	A51 → A48

NOTE

After installing the Expansion Memory, recalibrate the power supply according to the instruc- given in Appendix B.

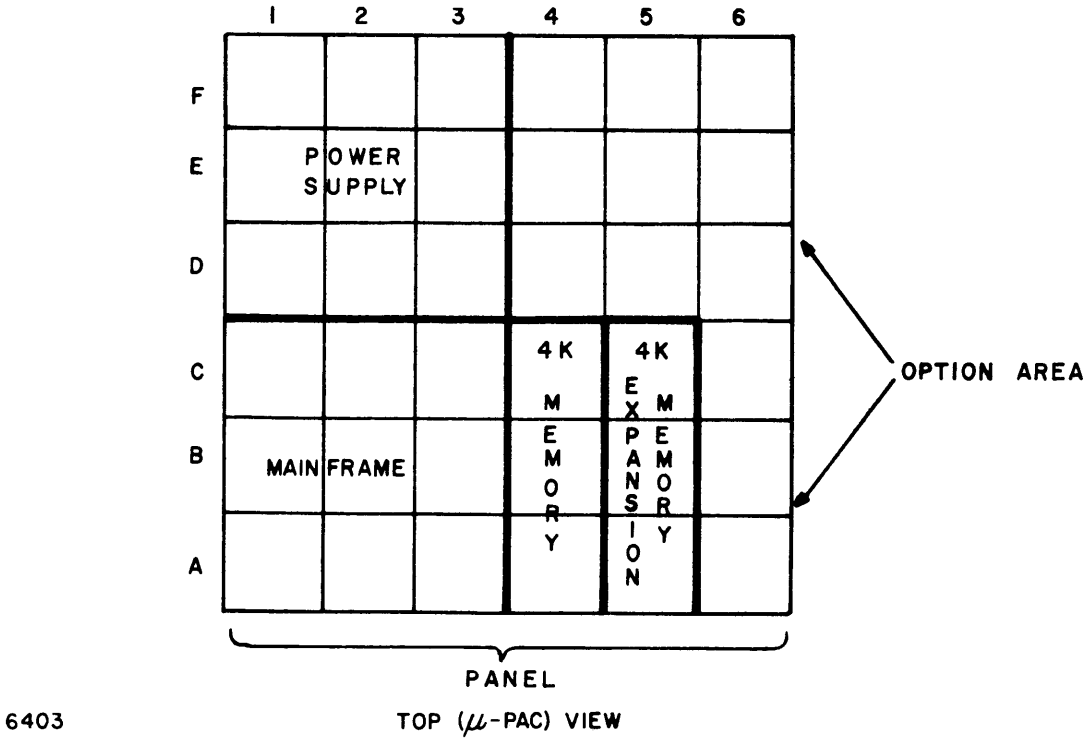


Figure 5-8. Module Locations

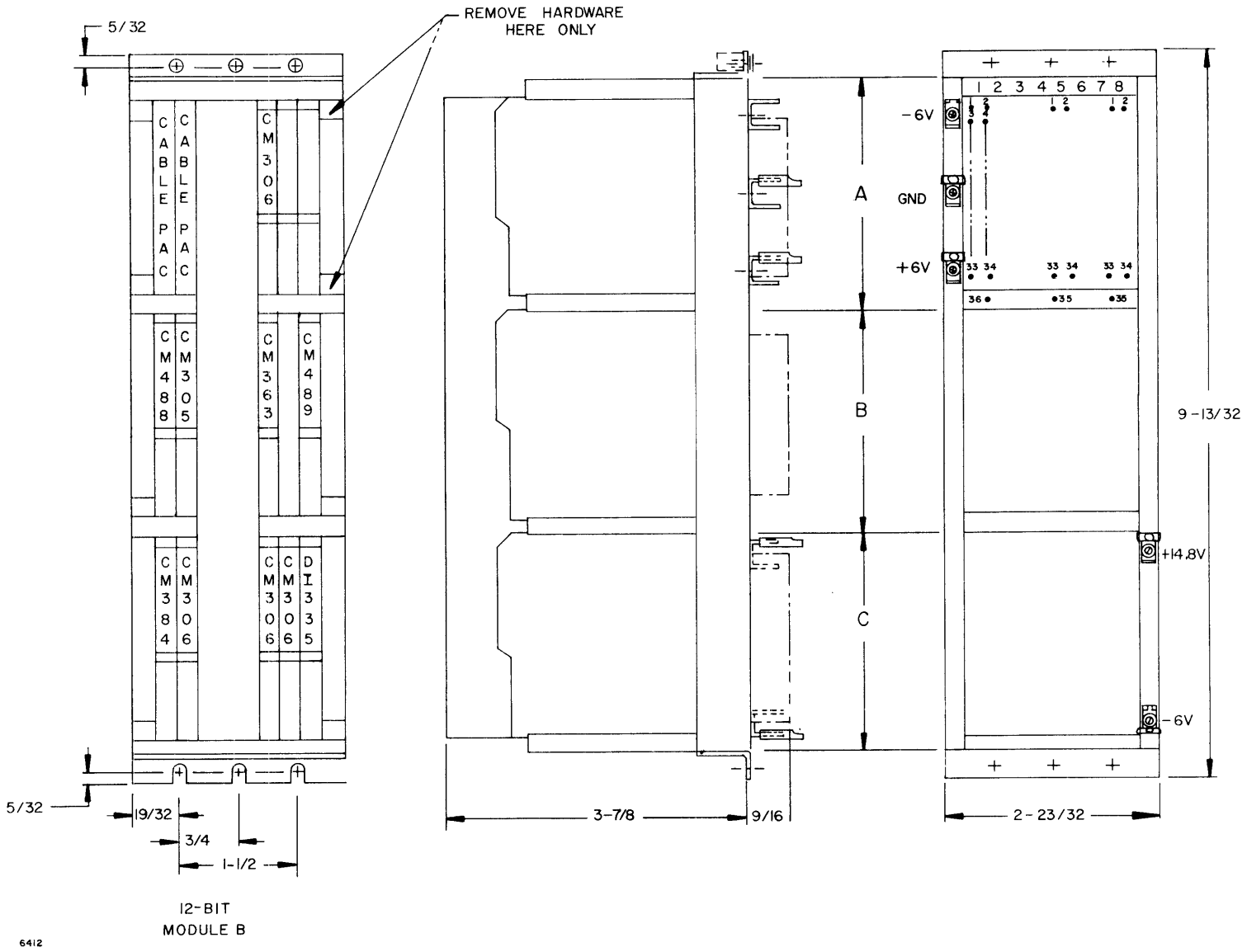


Figure 5-9. 4K Expansion Memory

SECTION VI
MAINTENANCE

This section contains data on preventive and corrective maintenance, service, and repair of the H112 Digital Controller.

μ-PAC COMPLEMENT, SPARE PARTS, AND EQUIPMENT

The basic μ-PAC complement and recommended number of spares for each μ-PAC type (including memory PACs) are listed in Table 6-1. Recommended spare parts (including memory) are listed in Table 6-2. Tools and test equipment to facilitate maintenance are listed in Table 6-3.

μ-PAC MAINTENANCE, EXTRACTION, AND REPAIR

The following discussion deals with preventive and corrective maintenance on the μ-PACs used in the controller, and with general procedures for μ-PAC service and repair.

Preventive Maintenance

Periodically, conduct a visual inspection of the controller. Watch for an accumulation of dust and dirt, for improperly seated μ-PACs, and for damaged or improperly dressed cable and signal leads. Check all connectors for secure mating.

Test the cooling fans for proper operation and maintain a schedule for cleaning fan filters. Do not, however, use an air hose to clean the memory core stack.

The memory is thoroughly tested at Honeywell Inc., Computer Control Division, prior to shipment. All planes are tested simultaneously under all ZEROs, all ONEs, and worst-pattern conditions. The drive currents and strobe timing are set so that optimum operating margins result. The memory may be tested periodically, as a preventive maintenance procedure, by use of a memory test program.

The test equipment listed in Table 6-3 includes that recommended for maintaining the memory. Detailed information on solderless-wrapping tools and procedures is contained in the *Instruction Manual for Solderless Wrapping of μ-PAC Digital Modules,* CCD Doc. No. 130071371.

TABLE 6-1.
BASIC H112 μ-PAC COMPLEMENT AND RECOMMENDED SPARES

μ-PAC Type	Qty	Spare
BR-320	4	1
TG-320	7	1
DI-320	8	1
DL-320	4	1
DK-320	6	1
DF-320	7	1
FA-320	7	1
BR-335	2	1
PA-336	1	1
DL-335	1	1
CM-490	1	1
CS-185	2	1
CS-517	2	1
CS-520	1	1
CS-521	3	1
CS-536	1	1
MC-335	1	1
Expanded Memory Option		
TG-320	1	1
DI-320	1	1
DF-320	2	1
FA-320	1	1
Memory μ-PAC Complement		
CM-305	1	1
CM-306	4	1
CM-363	1	1
CM-384	1	1
CM-488	1	1
CM-489	1	1
DI-335	1	1

TABLE 6-2.
RECOMMENDED SPARE PARTS

Description	Dwg No.	Qty
Axial Fans	70 964 001 002	1
Cable Assembly (μ-PAC to μ-PAC)	70 013 826 702	1
Cable μ-PAC	70 024 600 703	1
Deflector OMNI-BLOC	70 014 368 701	1
F-08 Flat Pack	70 950 100 008	1
Fuses		
1A	70 960 002 007	2
3A	70 960 002 010	2
4A	70 960 002 011	2
10A	70 960 002 015	2
Lamps	70 935 082 002	2
Memory Stack 4K*	70 023 577 702	–
OMNI-BLOC		
1x3	70 025 868 701	1
2x3	70 025 868 702	1
3x3	70 025 868 703	1
Power Supply–PB-421*	70 025 869 701	–
Ribbon Jumper		
Jumper μ-PAC	70 014 998 701	1
Jumper μ-PAC	70 014 998 702	1
Thermistor Assembly	70 025 871 701	1
Tantalum Capacitor (3.3 μF)	70 950 100 008	1

*Recommended as depot spares.

TABLE 6-3.
TOOLS AND TEST EQUIPMENT

Qty	Description	Type (or Equivalent)
1	Oscilloscope	Tektronix 585
1	Dual-Trace Preamplifier	Tektronix 82
1	Multimeter	Simpson 260
1	Card Extender μ-PAC	XP-330
1	μ-PAC Extractor Tool	B008428
1	AC Current Probe	Tektronix P6016 probe and passive termination (or type 131 amplifier)
1	Hand Wire-Unwrapping Tool	70 917 202 001 (Gardner-Denver 505084-LH)
1	Hand Wire-Wrapping Tool, Battery Operated	70 917 200 001 (Gardner-Denver No. 14R2)
1	Wire Stripper	70 917 250 001 (Ideal 45-179)
25 ft	No. 30 AWG Solid Wire	70 940 061 010
1	Quick Disconnect Terminal Crimper	T and B WT 145
25 ft	No. 30 AWG Twisted-Pair Solid Wire	70 940 402 002
1	Precision DC Voltmeter	Weston Model 930-1905003 30/7 5/3 volts, ±1/2%, 1000 ohms/volt

Inserting and Removing System μ-PACs

The μ-PAC connector is polarized to protect against incorrect μ-PAC insertion. To remove a μ-PAC from the controller, engage the two holes in the handles of the μ-PAC with the μ-PAC extractor tool. Do not remove or insert printed circuit cards without turning off the dc power to the unit. The pluggable core stack in the memory module should be removed and inserted with care to avoid damaging the flat back on the outside surface.

μ-PAC Troubleshooting

The Extender μ-PAC, Model XP-330, can be used to gain access to points on the μ-PACs. Signals on the pins of the μ-PACs may be found in the μ-PAC descriptions in Appendix A or from the μ-PAC manuals referenced in Section I (Introduction) and on page A-1.

Component Checking

Many μ-PACs contain several identical circuits. Components can be checked by resistance comparison with parts on other channels or μ-PACs, or identical μ-PAC types may be interchanged to determine the nature of the failure.

Component Replacement

When replacing defective components, use a low-wattage soldering iron and rosin-core 60/40 solder. Remove excess solder from the printed circuit board after unsoldering a component. Care should be taken when removing components to avoid lifting the etch.

Insert the leads of the new component through the drilled hole or eyelet, clip off excess wire, and solder the leads to the printed circuit etch.

A flat pack should be placed squarely on the etched area, using an insulator between it and the μ-PAC. The F33s on the pluggable core stack use insulgrease instead of an insulator. Cut the leads to proper length and solder them. Examine the μ-PAC carefully for excess solder. Remove rosin deposits with a commercial cleaning solvent and wipe the μ-PAC clean with a dry, lint-free cloth.

MEMORY TROUBLESHOOTING

Memory Drive and Inhibit Voltage Calibration

The memory drive line and inhibit line currents are determined by setting of the 15 Vdc supply and precision resistors mounted on the CM-384 resistor board. The 15V supply calibration should be periodically checked. Use a voltmeter with at least ±1% accuracy at the terminals of the memory system. The 15V supply can vary ±5% at room temperature from its nominal value (14.8 Vdc) without causing memory errors.

Memory Strobe Timing Calibration

The timing of the sense amplifier strobe pulse is set identically for each unit and should not be adjusted. If a change in timing is required to obtain proper memory operation, the associated μ-PACs should be checked (e.g., CM-306, CM-305) before a timing change is made. The CM-490 description in Appendix A should be referred to if a timing change is required. MSTRB- should be between 150 ns and 200 ns wide at the 1.5V points.

Corrective Maintenance Procedures

Memory system troubleshooting consists of determining the type of problem, predicting the μ-PAC at fault, and locating the faulty circuit. Test procedures to aid in troubleshooting are given in the following paragraphs.

CAUTION

Use oscilloscope probes carefully to avoid shorting the connector terminals and thus damaging the μ-PAC.

In some cases, spare μ-PACs may be used to isolate faulty circuits by interchanging identical μ-PACs and noting any shift in the faulty bits or addresses. All memory μ-PACs with the same designation are interchangeable.

Refer to μ-PAC schematic and assembly drawings in Appendix A to isolate the defective components on the printed circuit card. Replace defective components.

Memory failures are generally of the following types:

a. Operation failures, caused by faulty timing and control circuits.

b. Partial data word failures, caused by a faulty sense amplifier, data register flip-flop, or data regeneration circuits.

c. Address failures, caused by faulty address register or selection circuits.

Memory failures may be localized by the following procedures:

a. Load the test pattern into the memory.

b. Initiate a read operation at each address sequentially and check each readout data word for the following failures:

(1) *Operational failures:* No apparent response to commands applied to the memory, or faulty operation at all addresses (see Table 6-4).

(2) *Partial data word failures:* Failures of one bit or a series of two or more bits at all addresses (see Table 6-5).

(3) *Address failures:* Faulty memory operation at particular addresses only (see Table 6-6).

The normal waveforms at various test points and μ-PAC connector pins are shown in Figure 6-1.

TABLE 6-4.
OPERATIONAL FAILURES

Symptoms	Probable Fault
No apparent response to commands	1. DC voltage 2. Timing Distributor μ-PAC, CM-490 3. MBSY-, MCI+, MRTDL- signals
Unable to read from any address	1. Timing Distributor μ-PAC, CM-490 2. 15V supply 3. MSTRB- signal

TABLE 6-5.
PARTIAL DATA WORD FAILURES

Symptoms	Probable Fault
Failure of 1 bit (ZERO or ONE) at all addresses	1. Sense Amplifier μ-PAC, CM-363 2. Data register 3. Inhibit μ-PAC CM-305 4. Sense winding 5. Inhibit winding 6. Resistor μ-PAC, CM-384
Failure of 1 bit at particular addresses	1. Sense Amplifier μ-PAC, CM-363 2. X or Y switch or sink, Selector μ-PAC, CM-306 3. Sense winding 4. X- or Y-drive line 5. X- or Y-selection diode (F08)
Failure of 1 bit at one address	1. Sense Amplifier μ-PAC, CM-363 2. Marginal core

TABLE 6-6.
ADDRESS, DECODING, AND SELECTION FAILURES

Symptom	Probable Fault
All bits fail as a function of particular address bits	1. X or Y switch or sink, Selector μ-PAC, CM-306 2. Timing Distributor μ-PAC, CM-490 3. X- or Y-drive line 4. X- or Y-selection diode

Magnetic Core Stack Maintenance

Under normal operating conditions it is unlikely that troubles will occur within the magnetic core stack. However, continuity measurements of the sense and drive windings will enable maintenance personnel to check core stack wiring. Exercise caution in taking these measurements, to avoid damaging the matrix windings.

CAUTION

Multimeter current and voltage should be kept below 300 mA and 30V, respectively, to avoid damage to matrix windings and components.

Sense Windings.—The procedures for checking the sense windings are as follows:

a. Turn off memory power. Remove the Sense Amplifier μ-PAC (CM-363) associated with the sense windings to be checked.

b. Place the ohmmeter leads across the sense winding inputs (MWSXX+ and MWSXX-) to the Sense Amplifier μ-PAC, as determined from the logic diagrams of Volume II, and check for continuity. One sense winding links 4096 cores (Table 6-7).

TABLE 6-7.
SENSE WINDING CHECKLIST

Winding	Location	Winding	Location
MWS01+	BX0323	MWS07+	BX0314
MWS01-	BX0321	MWS07-	BX0316
MWS02+	BX0319	MWS08+	BX0310
MWS02-	BX0317	MWS08-	BX0312
MWS03+	BX0315	MWS09+	BX0114
MWS03-	BX0313	MWS09-	BX0116
MWS04+	BX0311	MWS10+	BX0110
MWS04-	BX0309	MWS10-	BX0112
MWS05+	BX0324	MWS11+	BX0124
MWS05-	BX0322	MWS11-	BX0122
MWS06+	BX0318	MWS12+	BX0118
MWS06-	BX0320	MWS12-	BX0120

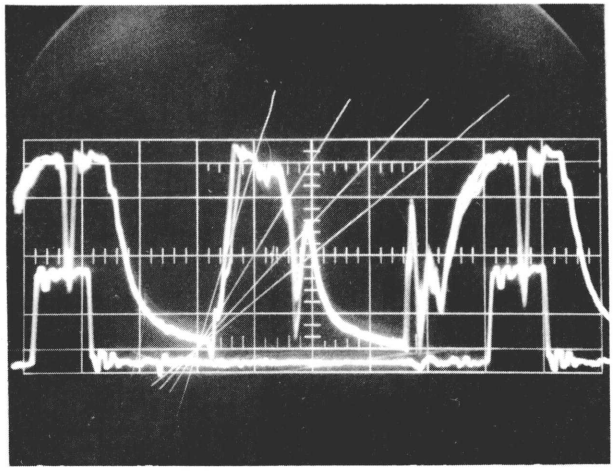
c. Resistance readings should be approximately 28 ohms for all sense windings. The resistance readings for all bits should agree within ±10%.

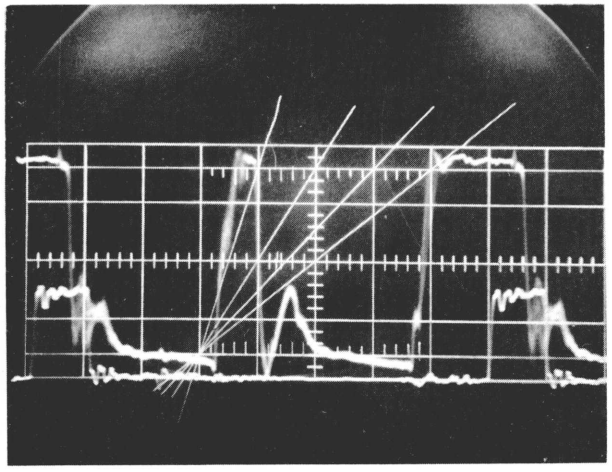
Drive Windings.—The procedures for checking the drive windings are as follows:

a. Turn off memory power. Remove the Selector μ-PAC (CM-306) associated with the X- and Y-drive line to be checked. This can be determined from the logic diagrams (Volume II), by relating the bad address to a sink and switch output for both the X- and Y-coordinates. The drive winding connections to the core stack are shown in Figure 5-1 (Section V).

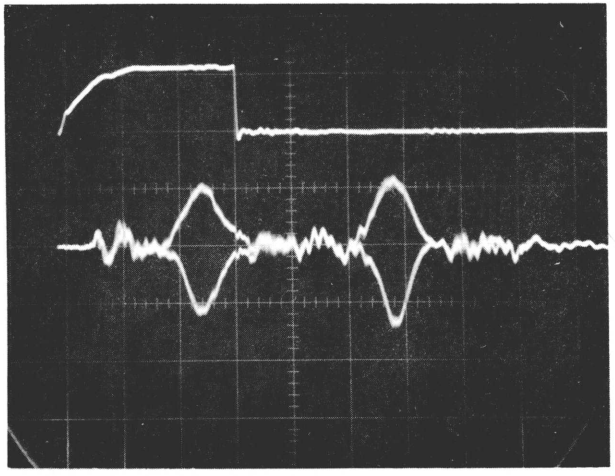
b. The actual drive line connections are located on the core stack printed circuit board. The selection switch outputs are isolated by a diode from each drive line so that the resistance reading between any diode bus (XDXX) and line bus (XBXX) will include a diode forward drop.

c. Measure continuity by referring to the simplified selection diagram, Figure 5-6 (Section V). For example, to check the continuity of drive line X60, put one ohmmeter probe on the corresponding sink output (collector output of transistor Q4) and the other ohmmeter probe on the proper switch output (collector of transistor Q2). A low resistance (one forward diode drop plus a drive line resistance of approximately 6 ohms) indicates continuity for both diodes and the drive line. It may be necessary to reverse the probes to obtain the correct polarity to forward-bias the selection diodes. The continuity of the current path for the opposite drive polarity should be similarly checked, by moving the probe from the collector of Q2 to the emitter of Q1 and reversing the polarity. In this mode of measuring, two diodes will be in the circuit. A high resistance reading in both drive current polarity paths indicates an open drive winding or drive bus. If a drive bus is open, the other drive lines connected to the same bus will

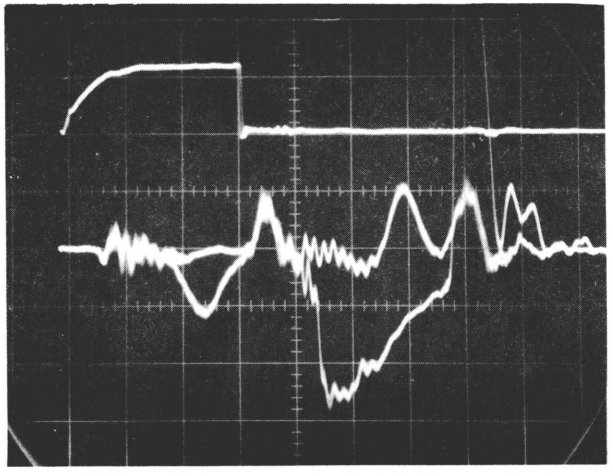




SCALE: 200ns / 5V / CM



SCALE: 50 MV / 200 ns / CM



SCALE: 50 MV/200 ns / CM

Figure 6-1. Normal Waveforms at Test Points and μ-PAC Connector Pins

also have a high resistance reading. A high resistance reading in only one of the read or write current paths indicates an open F08 Flat Pack diode.

Inhibit Windings.—The procedures for checking the inhibit windings are as follows:

a. Turn off memory power. Remove the Inhibit μ-PAC (CM-305) associated with the inhibit line to be checked.

b. Place the ohmmeter leads across the inhibit winding inputs (MZWXX+ and MZWXX-) to the Inhibit μ-PAC as determined from Table 6-8 and the logic diagram of Volume II.

c. Resistance readings should be approximately 11 ohms for all inhibit windings. The resistance windings for all bits should agree within ±10%.

TABLE 6-8.
INHIBIT WINDING CHECKLIST

Winding	Location	Winding	Location
ZW01+	CX06-03	ZW07+	BX04-01
ZW01-	CX06-01	ZW07-	BX04-02
ZW02+	BX06-32	ZW08+	AX04-30
ZW02-	BX06-31	ZW08-	AX04-32
ZW03+	BX06-01	ZW09+	CX04-06
ZW03-	BX06-02	ZW09-	CX04-08
ZW04+	AX06-31	ZW10+	AX04-26
ZW04-	AX06-29	ZW10-	AX04-28
ZW05+	CX04-02	ZW11+	CX06-07
ZW05-	CX04-04	ZW11-	CX06-05
ZW06+	BX04-32	ZW12+	AX06-27
ZW06-	BX04-31	ZW12-	AX06-25

SECTION VII
ILLUSTRATED PARTS BREAKDOWN (IPB)

INTRODUCTION

This section is an Illustrated Parts Breakdown (IPB) that lists, illustrates, and describes assemblies, subassemblies, and detail parts of the H112 Digital Controller mainframe. Major assemblies include the control panel, the main drawer assembly, and the logic and memory assembly.

This IPB consists of two major segments: the Introduction and the Group Assembly Parts List. Appendix B (Section 2) provides the breakdown of the power supply. Options are documented in their separate manuals.

Purpose

The IPB, illustrating the physical relationship of parts to one another, is meant to be used by logistics support personnel in procuring, storing, issuing, and identifying parts.

Equipment Coding

Coding drawings have been provided for use in further identifying CCD equipment.

Methods of Use

Locating a part in this IPB can be done in several ways. Two methods are outlined below, the method to be used depending upon the availability of information initially:

1. If you know the name of the assembly on which the part is located, proceed as follows:
   a. Find the assembly name in the figure/part cross-reference (Table 7-1).
   b. Refer to the page number indicated for the particular assembly.
2. If you know the location of the part, refer to Figure 7-1 in the Group Assembly Parts List and proceed as follows:
   a. Identify the equipment rack on the illustration, locate the unit within the rack, and note the number (the Index Number) at the end of the leader.
   b. Using this number, refer to the parts list immediately following the illustration.
   c. Read the information as it applies and turn to the referenced illustration (figure) for a detailed breakdown of the assembly.

Each parts list in this IPB provides information arranged in columns, as follows:

1. *Figure and Index Number*: This column gives the figure number (e.g., Figure 7-1) and the Index Number, previously mentioned. The Index Number keys the order in which the parts are identified in the parts list (the only exceptions to this procedure are the PAC parts lists, which are keyed in a different manner).
2. *Designation*: This column gives the CCD coding designation, explained in the coding drawings (which follow).
3. *CCD Part Number*: CCD part numbers are given in this column unless an asterisk indicates otherwise.
4. *Indenture*: The relationship of an item to its next higher assembly (NHA) is indicated in this column: the "B" level is an inherent part of the first preceding "A" level; the "C" level is an inherent part of the first preceding "B" level; etc.
5. *Description:* This column may contain the following:
   a. Data sufficient to identify parts for ordering purposes.
   b. Instructions for locating a more detailed illustration for breakdown, e.g., "(See Figure 7-3 for breakdown)."
   c. Instructions re-establishing how a particular figure was arrived at, e.g., "Refer to Figure 7-4-1 for NHA)."
   d. References to the coding drawings for a better understanding of the coding technique used, e.g., "(See Drawing Number 70026048, sheet 1, for coding drawing)."
6. *Quantity per Assembly*: Each new figure is considered an assembly and the quantity indicated

in the column is the unit quantity representing the total used common to that assembly. The appearance of "Ref" indicates that the quantity was stated at its first appearance (NHA).

Parts Procurement Guide

1. When ordering from this manual, always reference the model and serial number of the computer.
2. Find the location of the assembly where the part is used.
3. State the part number with the description given in this manual.
4. Direct all inquiries to the following address:

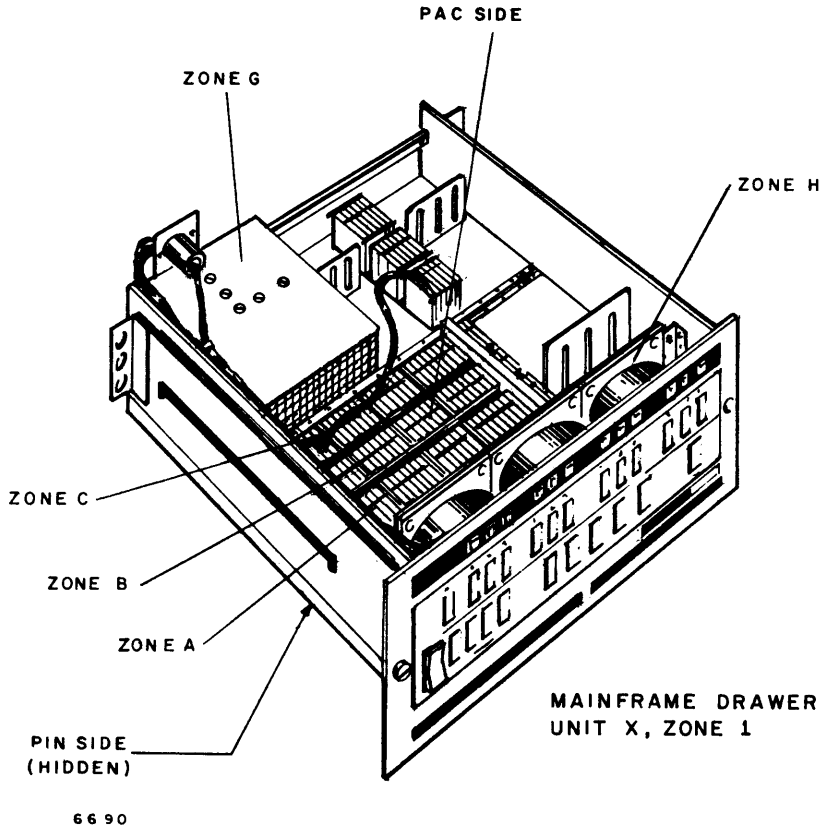
Honeywell Inc.
Computer Control Division
Old Connecticut Path
Framingham, Massachusetts 01701

Telephone: 617-879-2600
TWX: 710-380-6706

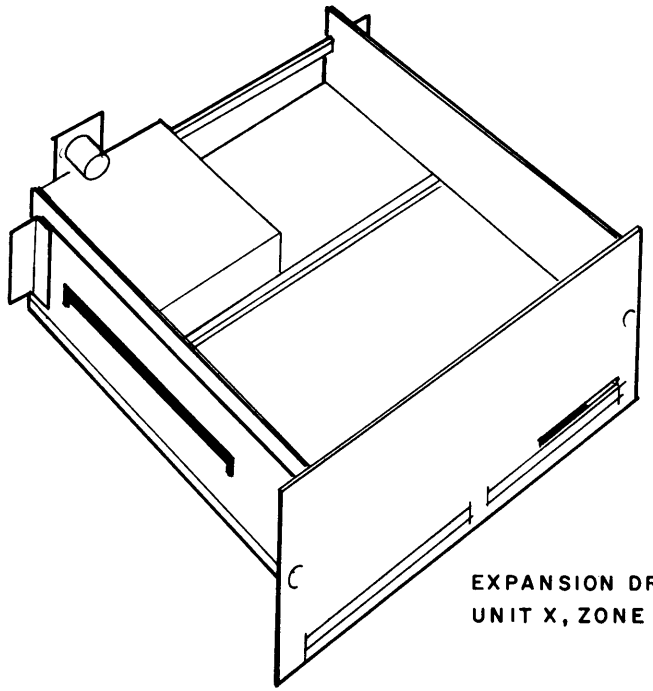
Important

The illustrations shown are representative of all Honeywell Inc., Computer Control Division, H112 Digital Controllers. Therefore, the illustrations used may not show minor differences between individual machines. If the differences are major, changes will be added to the illustration.

As changes are made in the equipment, this publication will be updated.

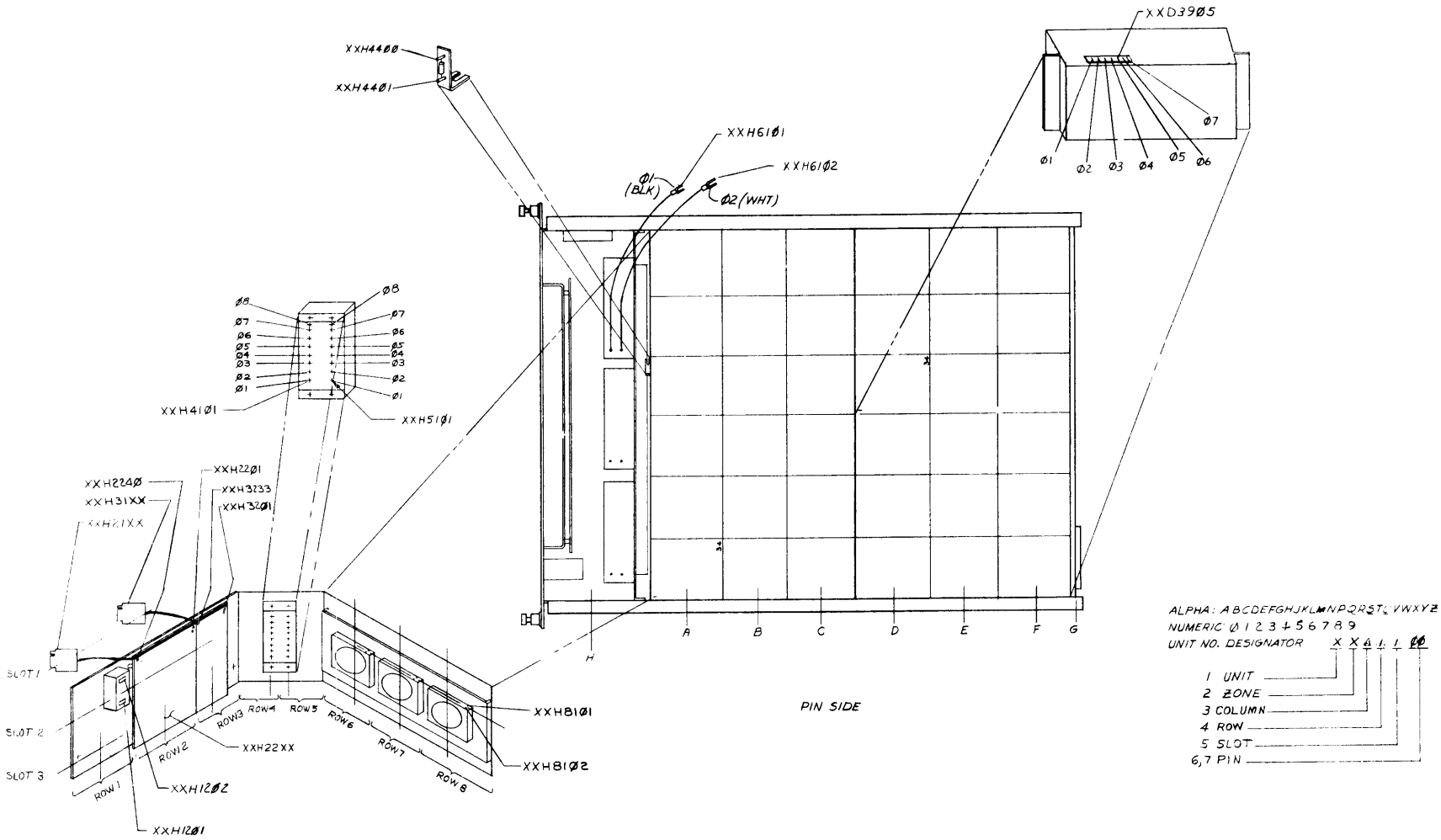


MAINFRAME DRAWER
UNIT X, ZONE 1

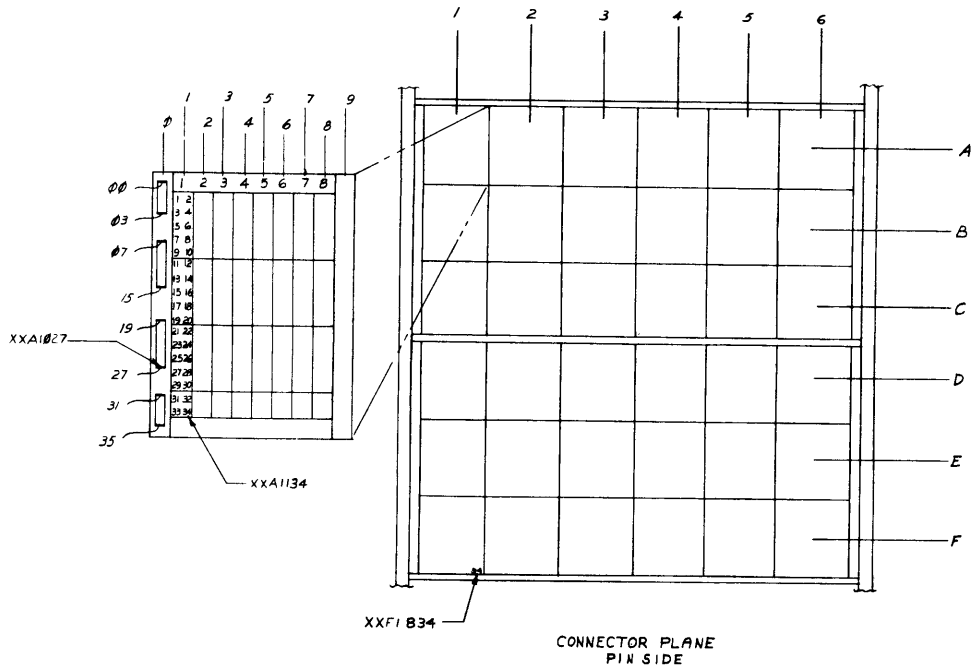


EXPANSION DRAWER
UNIT X, ZONE 2

Coding Drawing 70026048 (Sheet 1 of 3)



Coding Drawing 70026048 (Sheet 2 of 3)



ALPHA: A B C D E F G H J K L M N P Q R S T U V W X Y Z
NUMERIC: 0 1 2 3 4 5 6 7 8 9

UNIT NO. DESIGNATOR: A 3 B 2 1 34

1 UNIT
2 ZONE
3 COLUMN
4 ROW
5 SLOT
6,7 PIN

Coding Drawing 70026048 (Sheet 3 of 3)

GROUP ASSEMBLY PARTS LIST

Table 7-1 lists the figure and page numbers for use in locating the Group Assembly Parts List for a particular subassembly.

TABLE 7-1
CROSS REFERENCE FOR FIGURE AND PAGE NUMBER

Figure No.	Description	CCD Part No.	Page No.
7-1	H112-01 Digital Controller, Rack Mounted Model, 4K Basic Unit	70025866701	7-7
7-2	Panel Front Assembly	70025930701	7-8
7-3	Drawer Main Assembly	70025524701	7-9
7-4	Printed Circuit Board Assembly A	70025531701	7-10
7-5	Printed Circuit Board Assembly B	70025531702	7-12
7-6	Logic and Memory (4K) Assembly	70024852701	7-14
7-7	Logic PAC Layout	No Number	7-15
7-8	Core Memory Unit (4K)	70023577702	7-18
7-9	Cabling Block Diagram	No Number	7-20

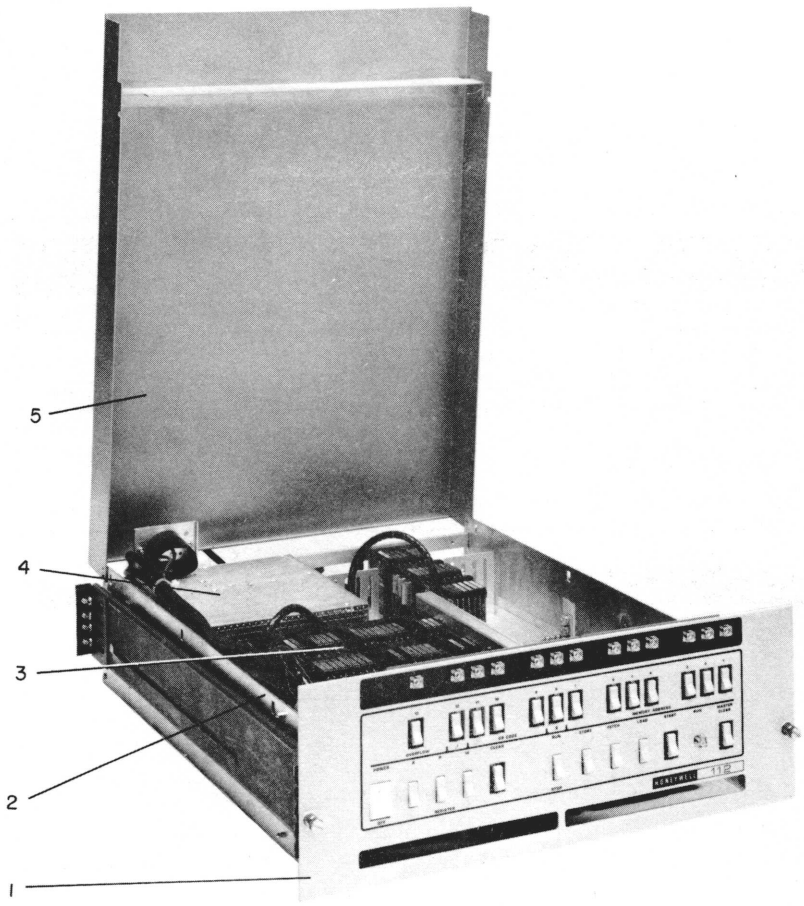


Figure 7-1. H112-01 Digital Controller

Fig. & Index No.	Designation	CCD Part No.	Indenture	Description	Qty. per Assy.
7-1	A1	70025866701	A	H112-01 DIGITAL CONTROLLER, RACK MOUNTED MODEL, 4K Basic Unit	
-1	A1	70025930701	B	PANEL FRONT ASSEMBLY (See Figure 7-2 for breakdown, and Dwg. No. 70026048 for coding drawings)	1
-2		70025524701	B	DRAWER MAIN ASSEMBLY (See Figure 7-3 for breakdown, and Dwg. No. 70026048 for coding drawings)	1
-3	A1ABC1 through A1ABC4	70024852701	B	LOGIC AND MEMORY (4K) ASSEMBLY (See Figure 7-6 for breakdown, and Dwg. No. 70026048 for coding drawings)	1
-4	A1DEF1 through A1DEF3	70025870701	B	POWER SUPPLY (See Appendix B for breakdown, and Dwg. No. 70026048 for coding drawings)	1
-5		70025568701	B	COVER, TOP ACCESS	1

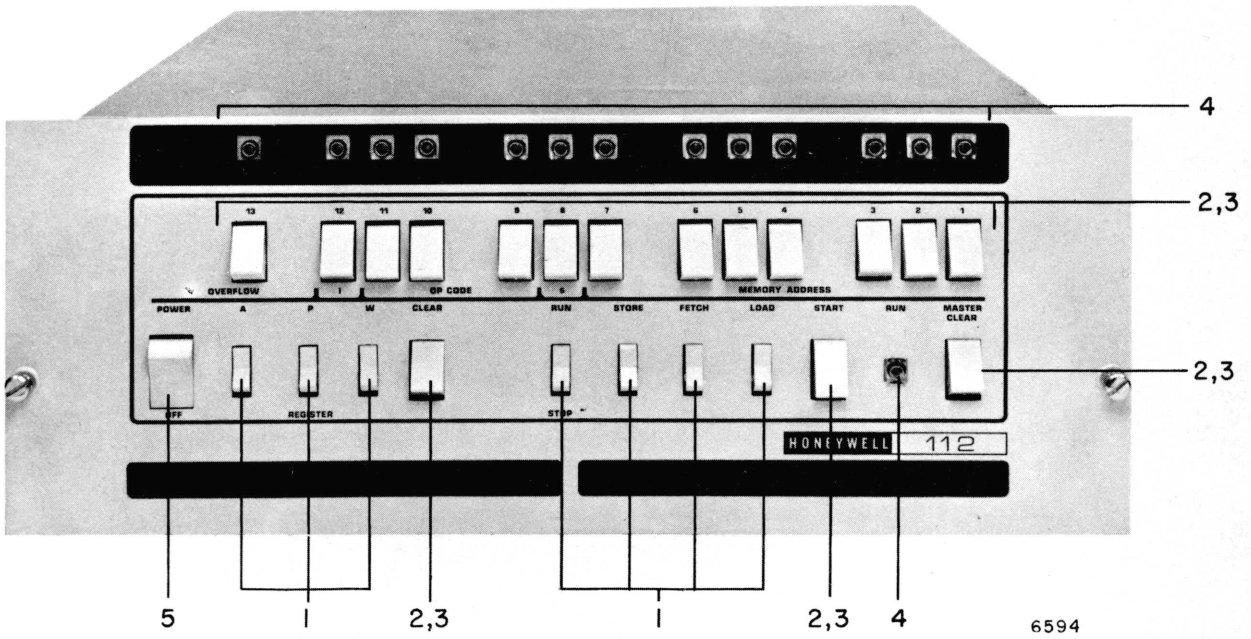


Figure 7-2. Panel Front Assembly

Fig. & Index No.	Designation	CCD Part No.	Indenture	Description	Qty. per Assy.
7-2	A1	70025930701	B	PANEL FRONT ASSEMBLY (Refer to Figure 7-1-1 for next higher assembly)	Ref
-1		70934279001	C	SWITCH, PUSH, DPDT – 3A at 125Vac; 1.5A at 250Vac; 0.5Adc	7
-2		70934277001	C	SWITCH, PUSH, SPDT – 6A at 125Vac; 3A at 250Vac; 1.0 Adc	16
-3		70023068001	C	BUTTON, CAP – white, molded plastic	16
-4		70935082002	C	LAMP, CARTRIDGE – 6.3Vac at 0.04A; clear lens	14
-5		70960057001	C	CIRCUIT BREAKER – single pole; 15A at 250Vac; time delay curve no. 3	1

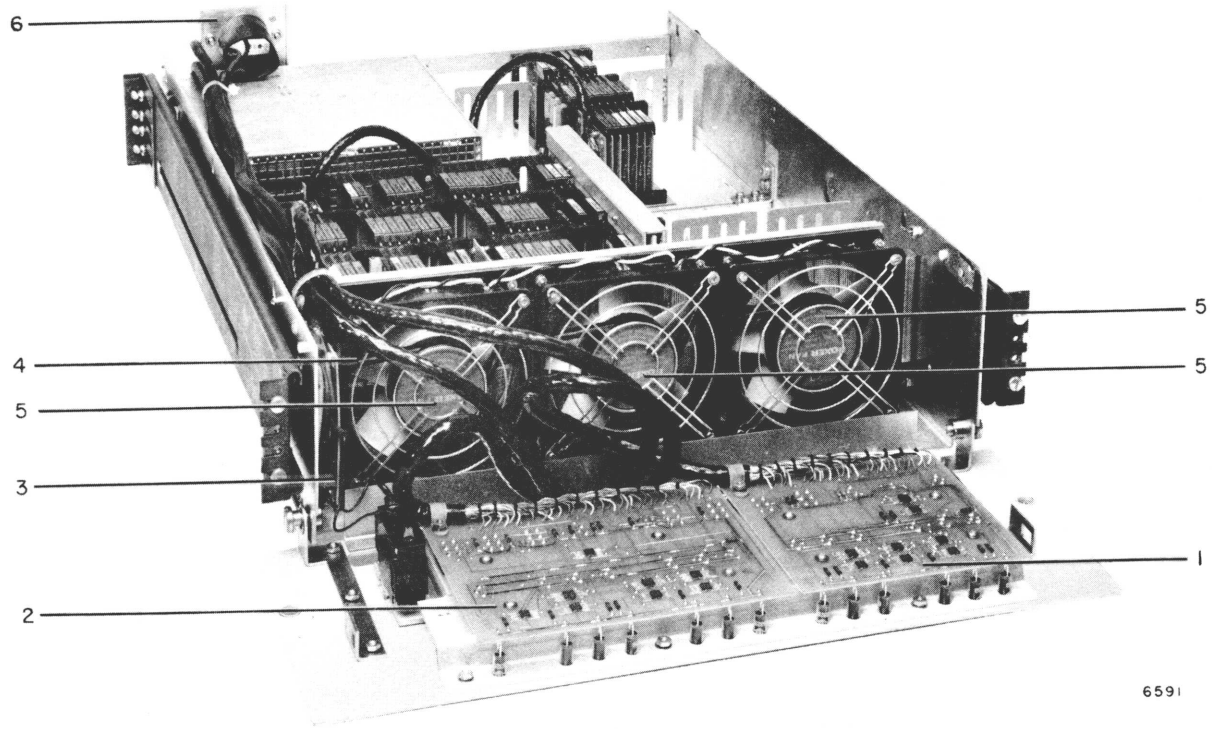


Figure 7-3. Drawer Main Assembly

Fig. & Index No.	Designation	CCD Part No.	Indenture	Description	Qty. per Assy.
7-3	A1G and H	70025524701	B	DRAWER MAIN ASSEMBLY (Refer to Figure 7-1-2 for next higher assembly)	Ref
-1		70025605701	C	PRINTED CIRCUIT BOARD ASSEMBLY A (See Figure 7-4 for breakdown)	1
-2		70025606702	C	PRINTED CIRCUIT BOARD ASSEMBLY B (See Figure 7-5 for breakdown)	1
-3		70937502008	C	TERMINAL BOARD – barrier type, 8 terminals	1
-4		70023929702	C	COOLING UNIT ASSEMBLY	1
-5		70964001002	C	FAN, AXIAL – 100 cfm, 105/120Vac, 50-60 Hz; 4-11/16 in. square by 1-1/2 in. thick	3
	(Hidden)	7091103010	C	FILTER, AIR – Multiple layers, crimped wire screen cloth, washable; 14-3/4 in. by 4-3/4 in. by 0.50 in. thick	1
-6		70941323001	C	CONNECTOR, RECEPTACLE, ELECTRICAL – 2 sections each with 2 female parallel-blade contacts and 1 ground pin contact	1

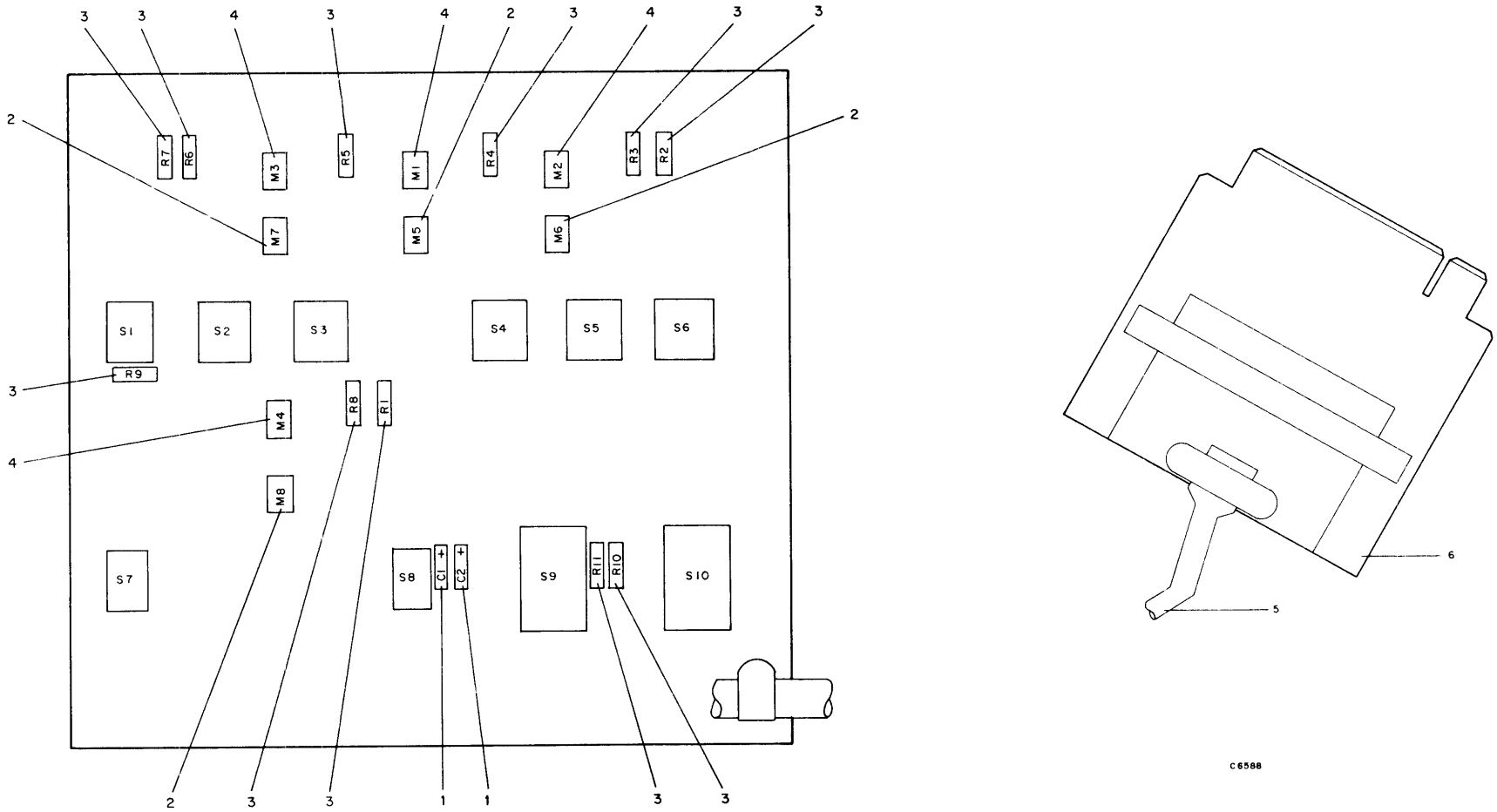


Figure 7-4. Printed Circuit Board Assembly A

Fig. & Index No.	Designation	CCD Part No.	Indenture	Description	Qty. per Assy.
7-4		70025531701	C	PRINTED CIRCUIT BOARD ASSEMBLY A (Refer to Figure 7-3-1 for next higher assembly)	Ref
-1	C1,C2	70930230011	C	CAPACITOR, FIXED, ELECTROLYTIC – 3.3 μF, ±20%, 10V	2
-2	M5 through M8	70950103002	D	MICROCIRCUIT – quad-two input NAND gate	4
-3	R1 through R11	70932007035	D	RESISTOR, FIXED, COMPOSITION – 270 ohms; 1/4W, ±5%	11
-4	M1 through M4	70950105008	D	MICROCIRCUIT – dual-four input NAND gate	4
-5		70940366001	D	CABLE, SPECIAL PURPOSE – 17 twisted-pair; 26 AWG size	1
-6	A1A11	70024600703	D	CABLE PAC ASSEMBLY	1

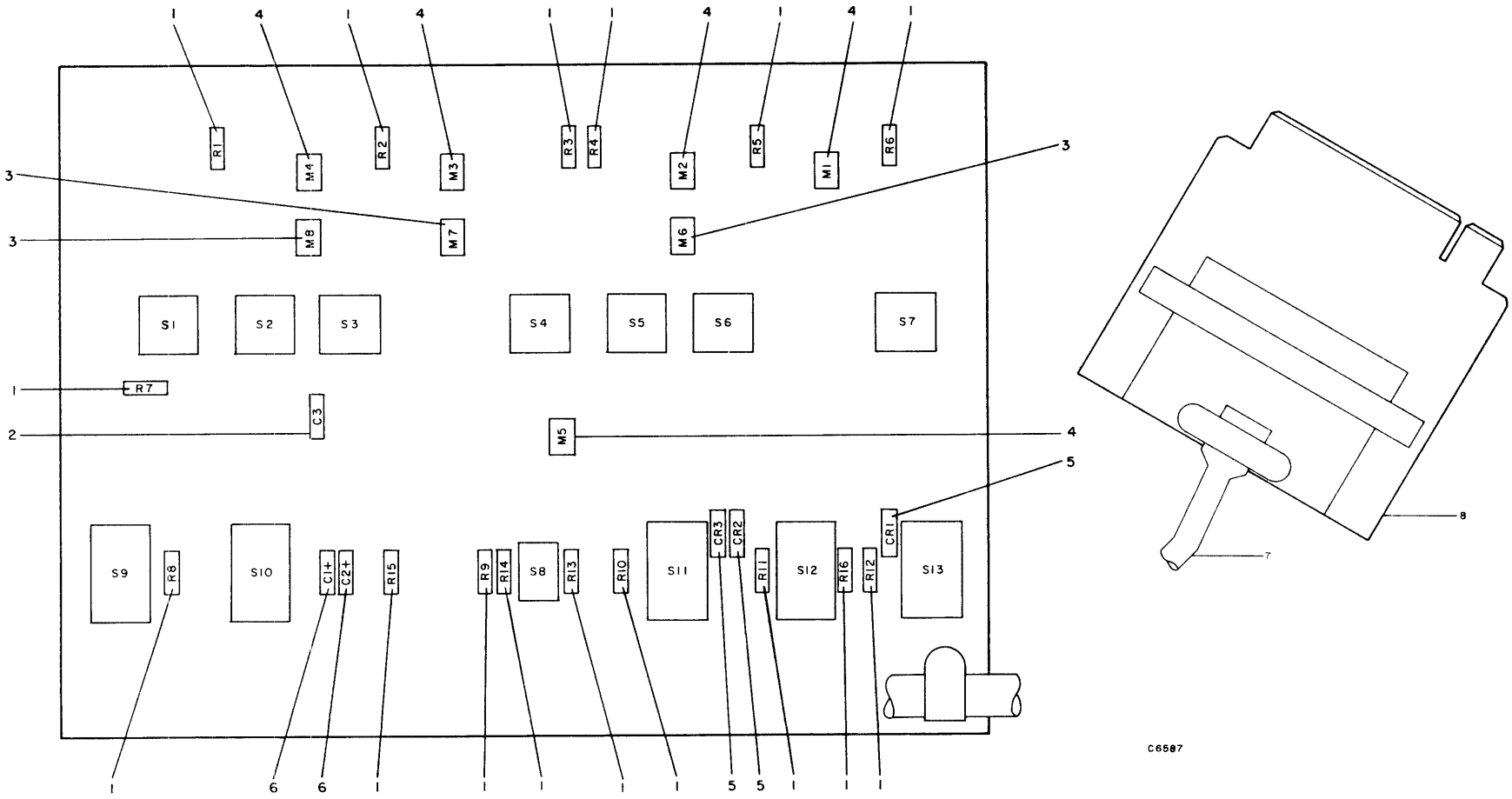


Figure 7-5. Printed Circuit Board Assembly B

Fig. & Index No.	Designation	CCD Part No.	Indenture	Description	Qty. per Assy.
7-5		70025531702	C	PRINTED CIRCUIT BOARD ASSEMBLY B (Refer to Figure 7-3-2 for next higher assembly)	Ref
-1	R1 through R16	70932007035	D	RESISTOR, FIXED, COMPOSITION – 270 ohms, 1/4W, ±5%	16
-2	C3	70930011127	D	CAPACITOR, FIXED, MICA – 100 pF, 100V ±5%	1
-3	M6 through M8	70950105002	D	MICROCIRCUIT – quad-two input NAND gate	3
-4	M1 through M5	70950105008	D	MICROCIRCUIT – dual-four input NAND gate	5
-5	CR1 through CR3	70943083002	D	SEMICONDUCTOR DEVICE, DIODE	3
-6	C1,C2	70930230011	D	CAPACITOR, FIXED, ELECTROLYTIC – 3.3 μF, 10V, ±20%	2
-7		70940366001	D	CABLE, SPECIAL PURPOSE – 17 twisted-pair; 26 AWG size	1
-8	A1B11	70024600703	D	CABLE PAC ASSEMBLY	1

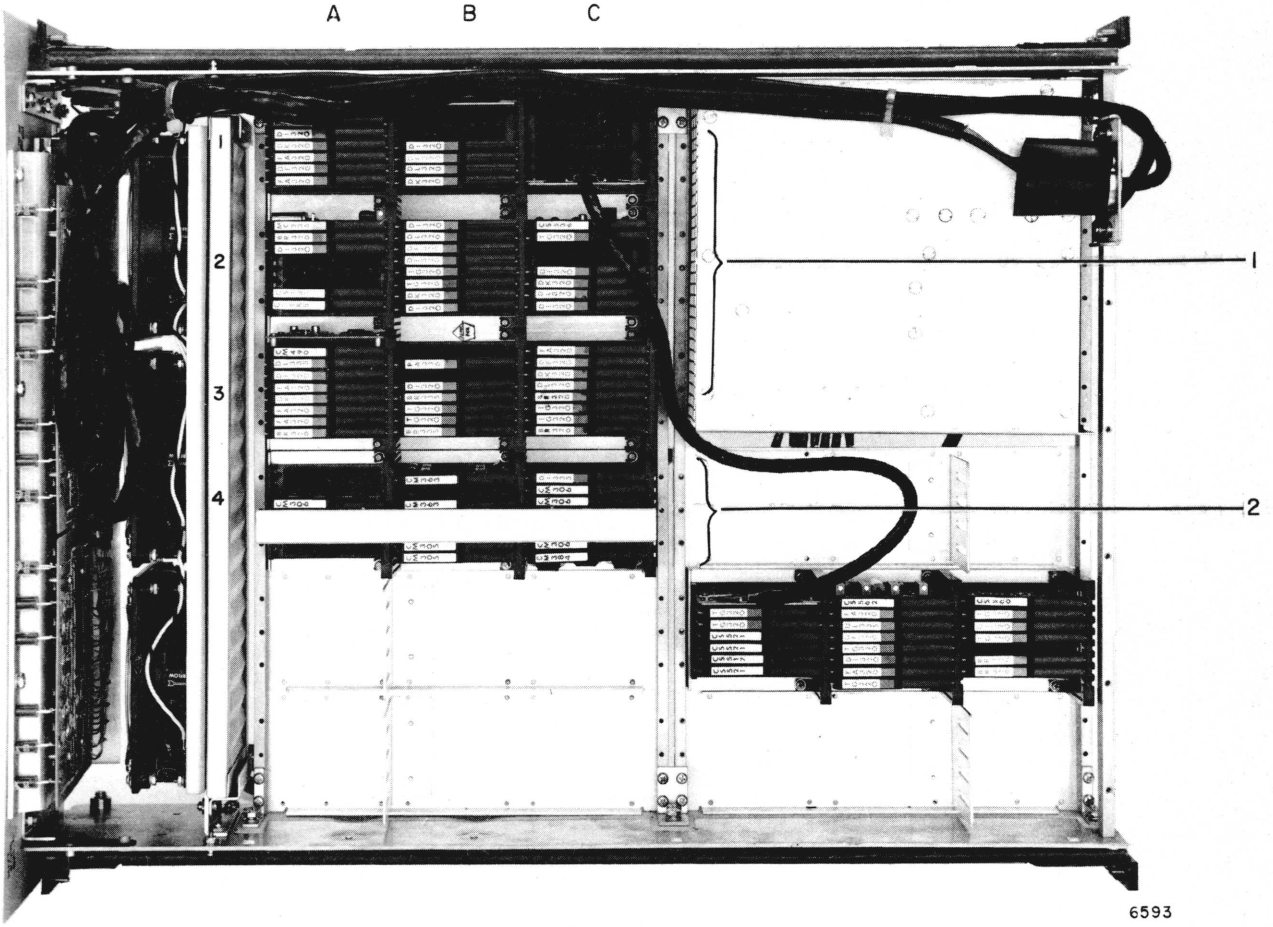


Figure 7-6. Logic and Memory (4K) Assembly

Fig. & Index No.	Designation	CCD Part No.	Indenture	Description	Qty. per Assy.
7-6	A1ABC1 through A1ABC4	70024852701	B	LOGIC AND MEMORY (4K) ASSEMBLY (Refer to Figure 7-1-3 for next higher assembly)	Ref
-1	A1ABC1 through A1ABC3	No number	C	LOGIC PAC LAYOUT (See Figure 7-7 for breakdown)	1
-2	A1ABC4	70023577702	C	CORE MEMORY UNIT (See Figure 7-8 for breakdown)	1

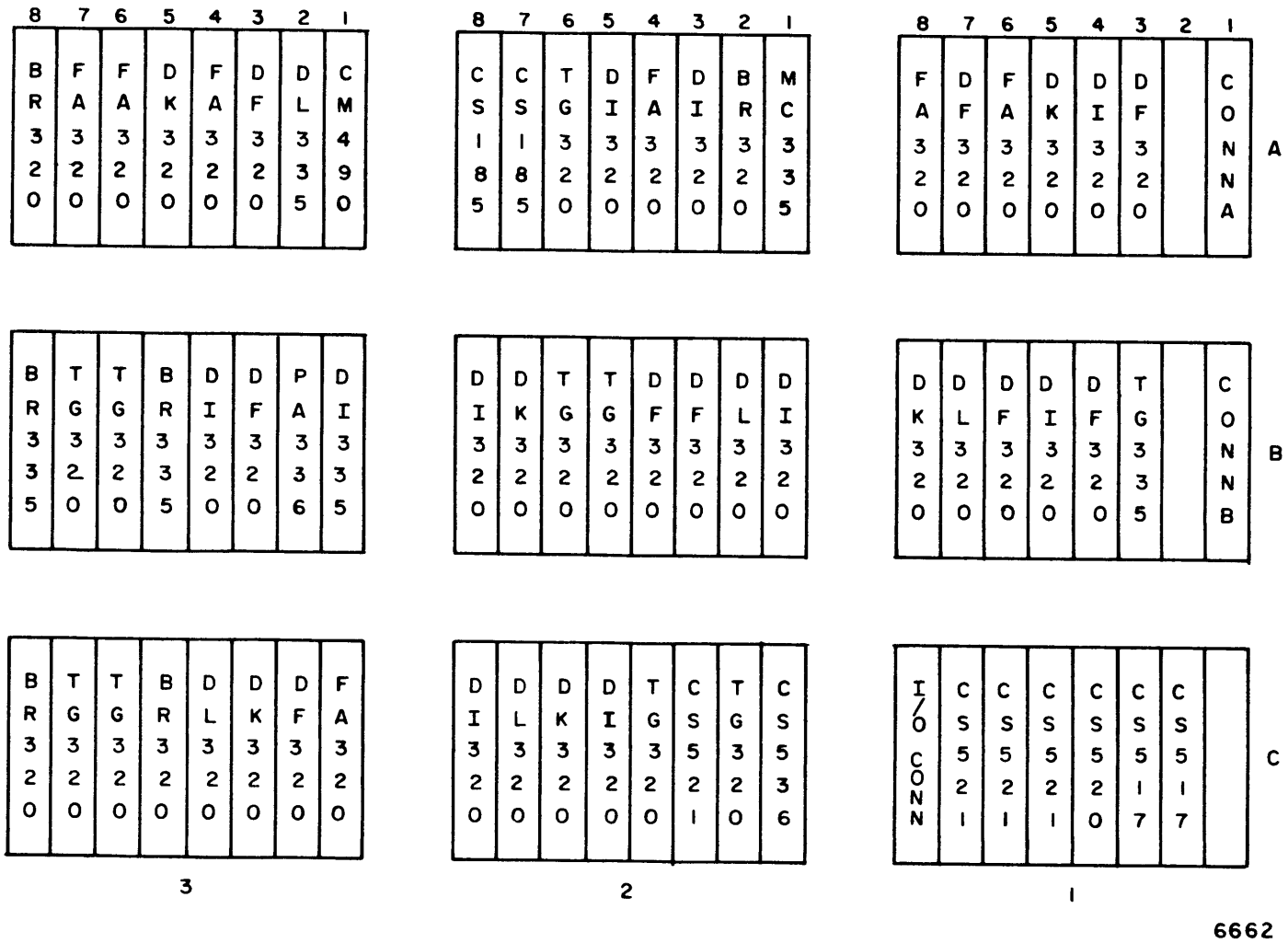


Figure 7-7. Logic PAC Layout

Fig. & Index No.	Designation	CCD Part No.	Indenture	Description	Qty. per Assy.
7-7	A1ABC1 through A1ABC3	No number	C	LOGIC PAC LAYOUT (Refer to Figure 7-6-1 for next higher assembly)	Ref
	A1A22,A38,C35, C38	BR-320	D	BUFFER REGISTER PAC (Refer to μ-PAC Instruction Manual, Doc. No. 130071369, Vol. I, Section 10, for parts breakdown)	4
	A1B35, B38	BR-335	D	BUFFER REGISTER PAC (Refer to μ-PAC Instruction Manual, Doc. No. 130071369, Vol. I, Section 2, for parts breakdown)	2
	A1A31	CM-490	D	TIMING DISTRIBUTOR PAC (Refer to Appendix A for parts breakdown)	1
	A1A27, A28	CS-185	D	8-BIT BINARY COUNTER PAC (Refer to Appendix A for parts breakdown)	2
	A1C12, C13	CS-517	D	DRIVER RECEIVER PAC (Refer to Appendix A for parts breakdown)	2
	A1C14	CS-520	D	RECEIVER PAC (Refer to Appendix A for parts breakdown)	1
	A1C15,C16,C17,	CS-521	D	DRIVER PAC (Refer to Appendix A for parts breakdown)	3
	A1C21	CS-536	D	SYSTEM NORMALIZER PAC (Refer to Appendix A for parts breakdown)	1
	A1A13,A17,A33*, B14, B16, B23, B24, B33, C32	DF-320	D	NAND TYPE 2 PAC (Refer to μ-PAC Instruction Manual, Doc. No. 130071369, Vol. I, Section 10, for parts breakdown)	9
	A1A14, A23,A25*, B15, B21, B28, B34, C25, C28	DI-320	D	NAND TYPE 1 PAC (Refer to μ-PAC Instruction Manual, Doc. No. 130071369, Vol. I, Section 10, for parts breakdown)	9
	A1A15,A35,B18, B27** , C26, C33	DK-320	D	INVERTER PAC (Refer to μ-PAC Instruction Manual, Doc. No. 130071369, Vol. I, Section 10, for parts breakdown)	6
	A1B17,B22,C27, C34	DL-320	D	NAND TYPE 2 PAC (Refer to μ-PAC Instruction Manual, Doc. No. 130071369, Vol. I, Section 10, for parts breakdown)	4
	A1A32	DL-335	D	NAND GATE PAC (Refer to μ-PAC Instruction Manual, Doc. No. 130071369, Vol. I, Section 4, for parts breakdown)	1
	A1A16,A18,A24*, A34, A36, A37, C31	FA-320	D	GATED FLIP-FLOP PAC (Refer to μ-PAC Instruction Manual, Doc. No. 130071369, Vol. I, Section 10, for parts breakdown)	7
	A1A21	MC-335	D	MASTER CLOCK PAC (Refer to μ-PAC Instruction Manual, Doc. No. 130071365, Vol. I, Section 5, for parts breakdown)	1

* Used for Expanded Addressing Option
** Used for Control Panel Option

Fig. & Index No.	Designation	CCD Part No.	Indenture	Description	Qty per Assy.
7-7	A1B32	PA-336	D	POWER AMPLIFIER PAC (Refer to μ-PAC Instruction Manual Doc. No. 130071369, Vol. I, Section 6, for parts breakdown)	1
	A1A26*, B25, B26, B36, B37, C22, C36, C37	TG-320	D	TRANSFER GATE PAC (Refer to μ-PAC Instruction Manual, Doc. No. 130071369, Vol. I, Section 10, for parts breakdown)	8

* Used for Expanded Addressing Option

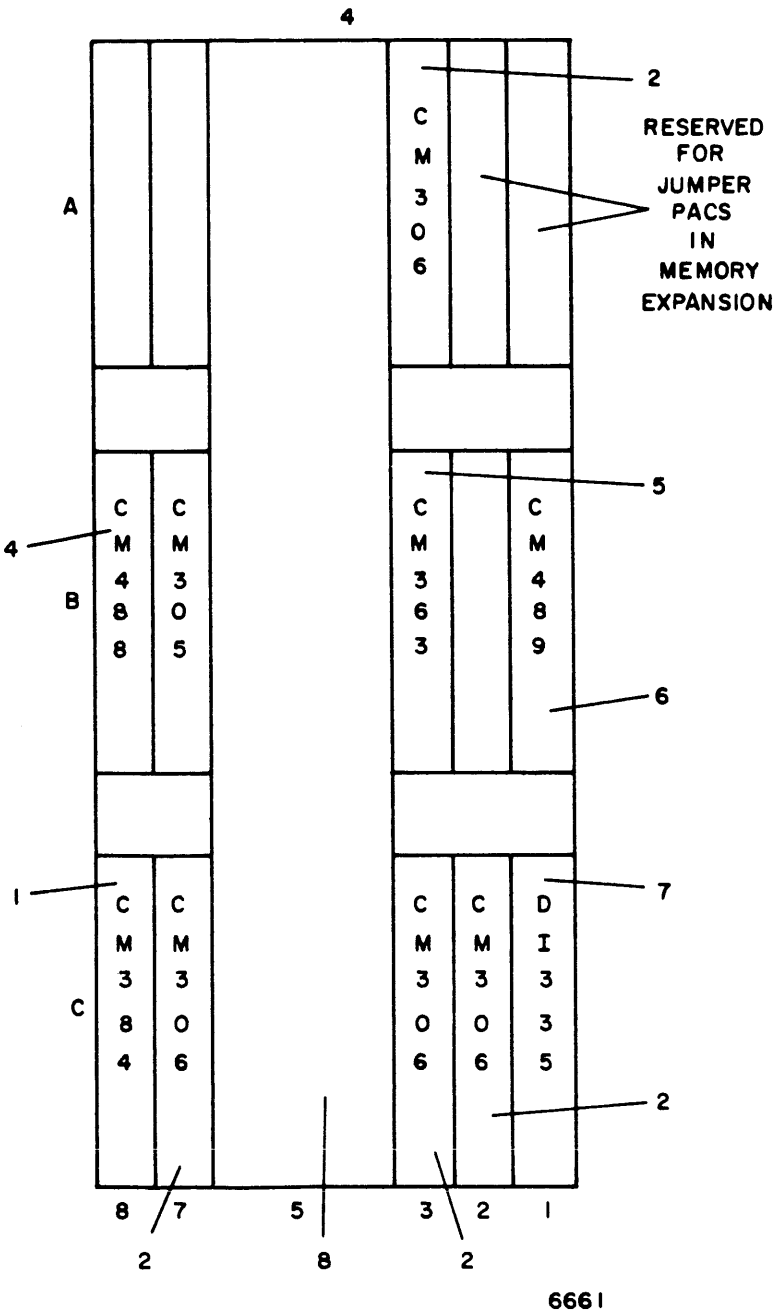


Figure 7-8. Core Memory Unit (4K)

Fig. & Index No.	Designation	CCD Part No.	Indenture	Description	Qty. per Assy.
7-8	A1ABC	700235702	C	CORE MEMORY UNIT (4K) (Refer to Figure 7-6-2 for next higher assembly)	Ref
-1	A1C48	CM-384	D	RESISTOR PAC (Refer to Appendix A for parts breakdown)	1
-2	A1C42,C42,C47, A43	CM-306	D	SELECTOR PAC (Refer to Appendix A for parts breakdown)	4
-3	A1B47	CM-305	D	INHIBIT PAC (Refer to Appendix A for parts breakdown)	1
-4	A1B48	CM-488	D	INHIBIT PAC (Refer to Appendix A for parts breakdown)	1
-5	A1B43	CM-363	D	SENSE AMPLIFIER PAC (Refer to Appendix A for parts breakdown)	1
-6	A1B41	CM-489	D	SENSE AMPLIFIER PAC (Refer to Appendix A for parts breakdown)	1
-7	A1C41	DI-335	D	NAND TYPE 1 PAC (Refer to μ-PAC Instruction Manual, Doc. No. 130071369, Vol. I, Section 3, for parts breakdown)	1
-8		70942507002	D	CORE STACK – 4096 words 16 bits per word	1

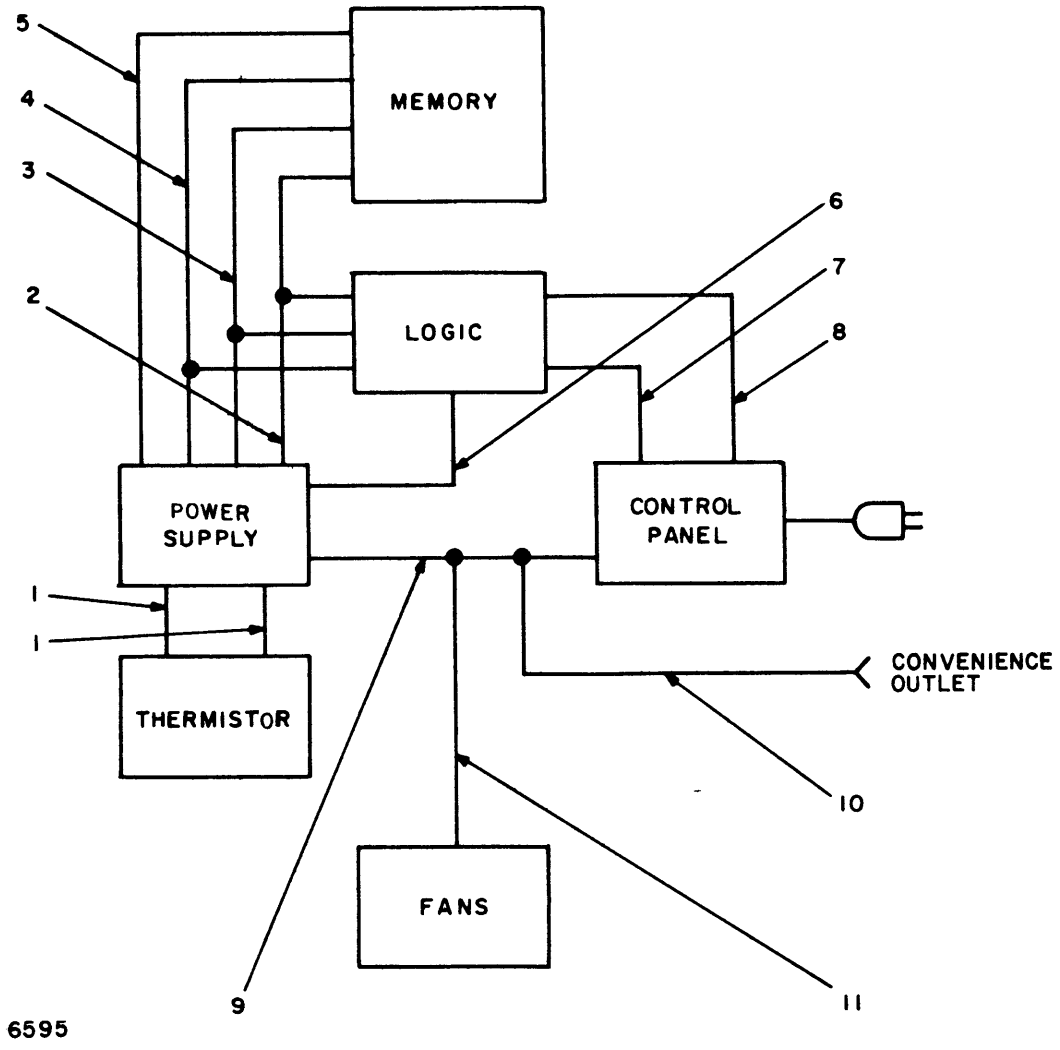


Figure 7-9. Cabling Block Diagram

Fig. & Index No.	Designation	CCD Part No.	Indenture	Description	Qty. per Assy.
7-9		No number	B	CABLING BLOCK DIAGRAM	Ref
-1			C	CABLE ASSEMBLY, SPECIAL PURPOSE – cable terminated one end with quick disconnect terminal; other end open; 18.5 in. o/a length; parts c/o:	2
		70937200001	D	TERMINAL, QUICK DISCONNECT – female, accommodating 1/4-in. wide by 0.032-in. thick blade male contact	4
		70940052806	D	WIRE, ELECTRICAL, INSULATED – blue, No. 16 AWG, 18.5 in. long	2
-2			C	CABLE ASSEMBLY, SPECIAL PURPOSE – cable terminated each end with quick disconnect terminals; 13 in. o/a length; parts c/o:	1
		70937200001	D	TERMINAL, QUICK DISCONNECT – female, accommodating 1/4-in. wide by 0.032-in. thick blade male contact	2
		70940052809	D	WIRE, ELECTRICAL, INSULATED – white, No. 16 AWG, 13 in. long	1
-3			C	CABLE ASSEMBLY, SPECIAL PURPOSE – cable terminated each end with quick disconnect terminals; 13 in. o/a length; parts c/o:	1
		70937200001	D	TERMINAL, QUICK DISCONNECT – female, accomodating 1/4-in. wide by 0.032-in. thick blade male contact	2
		70940052802	D	WIRE, ELECTRICAL, INSULATED – red, No. 16 AWG, 13 in. long	1
-4			C	CABLE ASSEMBLY, SPECIAL PURPOSE – cable terminated each end with quick disconnect terminals; 14 in. o/a length; parts c/o:	1
		70937200001	D	TERMINAL, QUICK DISCONNECT – female, accommodating 1/4-in.wide by 0.032-in. thick blade male contact	2
		70940052800	D	WIRE, ELECTRICAL, INSULATED – black, No. 16 AWG, 14 in. long	1
-5			C	CABLE ASSEMBLY, SPECIAL PURPOSE – cable terminated each end with quick disconnect terminals; 11 in. o/a length; parts c/o:	1
		70937200001	D	TERMINAL, QUICK DISCONNECT – female, accomodating 1/4-in. wide by 0.032-in. thick blade male contact	2
		70940052803	D	WIRE, ELECTRICAL, INSULATED – orange, No. 16 AWG, 11 in. long	1
-6			C	CABLE ASSEMBLY, SPECIAL PURPOSE – cable terminated each end with quick disconnect terminals; 17 in. o/a length; parts c/o:	1
		70937200001	D	TERMINAL, QUICK DISCONNECT – female; accommodating 1/4-in. wide by 0.032-in. thick blade male contact	2

Fig. & Index No.	Designation	CCD Part No.	Indenture	Description	Qty. per Assy.
7-9		70940052811	D	WIRE, ELECTRICAL, INSULATED – white with brown tracer color, No. 16 AWG, 17 in. long	
-7			C	CABLE ASSEMBLY, SPECIAL PURPOSE – part of Printed Circuit Board Assembly A (See Figure 7-4 for parts breakdown)	Ref
-8			C	CABLE ASSEMBLY, SPECIAL PURPOSE – part of Printed Circuit Board Assembly B (See Figure 7-5 for parts breakdown)	Ref
-9		70940251002	C	CABLE ASSEMBLY, POWER – 3-conductor cable; one end 3-contact male connector; other end open; o/a length 8 ft	1
-10			C	CABLE ASSEMBLY, POWER – 2-section connector; receptacle one end; other end open; parts c/o:	1
		70941323001	D	CONNECTOR, RECEPTACLE – 2-section, each with 2 female parallel blade contacts and 1 ground pin contact	1
		70940075001	D	CABLE, POWER – 3-conductor; No. 16 AWG, type SJ; rubber jacket	A/R
-11			C	CABLE ASSEMBLY, SPECIAL PURPOSE – twisted-pair wire; cable terminated one end with terminal lug; other end open; parts c/o:	1
		70937059001	D	TERMINAL LUG – flanged spade tongue; nylon-insulated ferrule accommodating No. 14 – No. 16 AWG wire; tongue accomodating no. 6 screw	2
		70940052700	D	WIRE, ELECTRICAL, INSULATED – black, No. 18 AWG, 7-strand	A/R
		70940052709	D	WIRE, ELECTRICAL, INSULATED – white, No. 18 AWG, 7-strand	A/R

APPENDIX A
DESCRIPTION OF SPECIAL μ-PACS*

This appendix describes the special μ-PACs used in the H112 Digital Controller (including memory). These are as follows:

CM-305	Inhibit PAC
CM-306	Selector PAC
CM-363	Sense Amplifier PAC
CM-384	Resistor PAC
CM-488	Inhibit PAC
CM-489	Sense Amplifier PAC
CM-490	Timing Distributor PAC
CS-185	Eight-Bit Binary Counter PAC
CS-517	Driver and Receiver PAC
CS-520	Receiver PAC
CS-521	Driver PAC
CS-536	System Normalizer PAC
CS-548	Line Receiver Assembly PAC

*Standard μ-PACs are described in the μ-PAC Manuals, CCD Doc. No. 130071369 and 130071853.

INHIBIT PAC, MODEL CM-305

The Inhibit PAC, Model CM-305 (Figures 1 and 2), contains two groups of four 425 mA transistor switches and one NAND gate. Each switch is controlled by a data input and strobed by a common line within each circuit.

An output switch is turned on (logic ZERO) when the corresponding data input is at logic ZERO, the timing input for circuits A, B, C and D is at logic ONE, and the timing input for circuits E, F, G, H is at logic ZERO.

The emitters of the output transistors are brought out to external pins 1 and 27. Optional capacitors C1, C2, and C3 are provided for filtering the +14V supply. Clamp diodes at each collector are used with inductive loads.

Specifications

Frequency of Operation

DC to 2 MHz

Input Loading

1 unit load each

Output Characteristics

Current:	425 mA (max)
Voltage:	30 V (max)
Power:	200 mW (max)

Current Requirements

+6V:	70 mA

Circuit Delay (425 mA Resistive Load)

Turn-on Delay (1.5V of input to 10% of current)	190 ns (max) 30 ns (min)
Turn-off Delay (1.5V of input to 90% of current)	190 ns (max) 30 ns (min)
Rise-fall Time (10%-90%)	35 ns (max)

Power Dissipation

2.2 W (max)

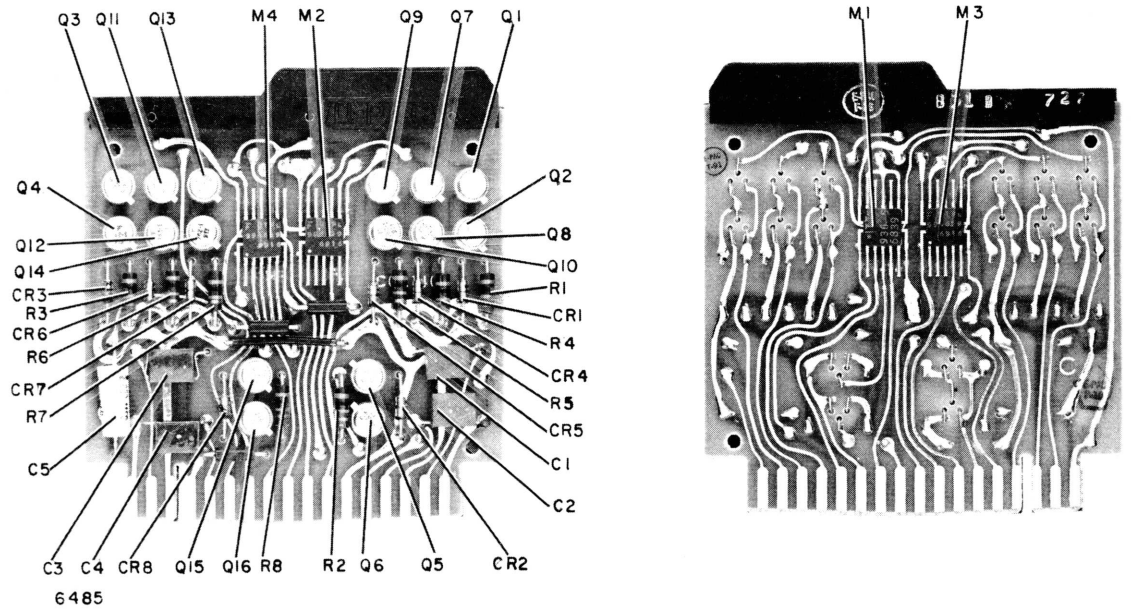
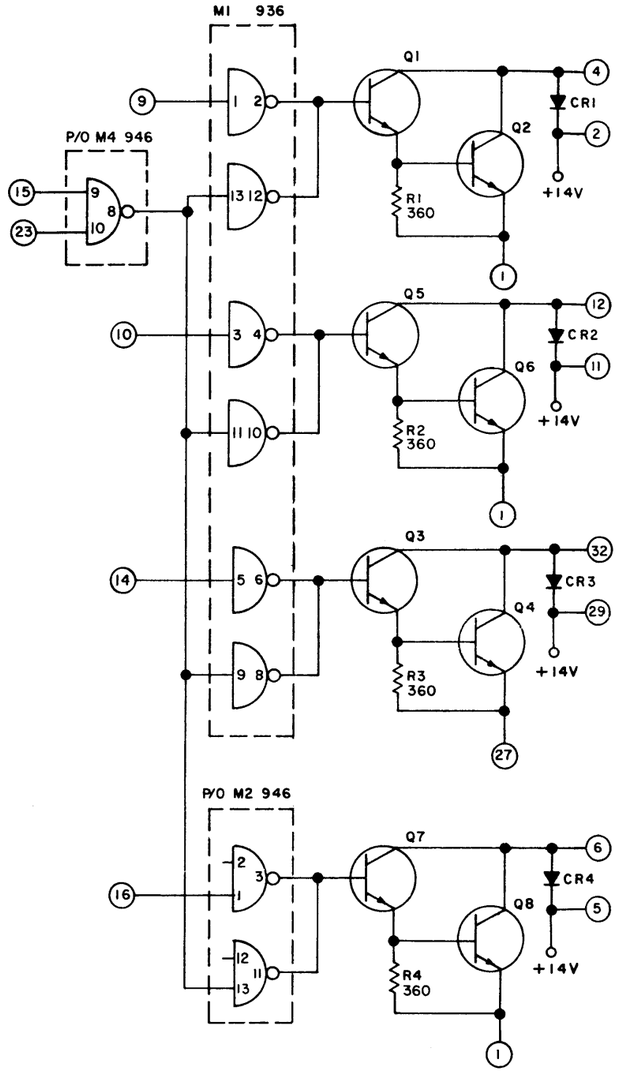
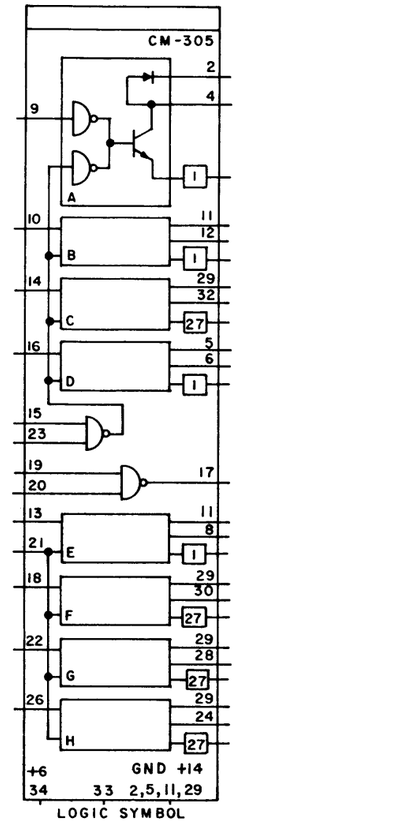


Figure 1. Inhibit PAC, Model CM-305, Parts Locations

ELECTRICAL PARTS LIST

Reference Designation	Description	CCD Part No.
C1-C4	CAPACITOR, FIXED, SOLID TANTALUM: 6.8 μF $\pm$5%, 20 Vdc	930 235 011
C5	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μF $\pm$5%, 20 Vdc	930 313 016
CR1-CR8	DIODE, SILICON	943 087 001
M1	MICROCIRCUIT: Type 936, hex single-input inverter integrated circuit	950 105 004
M2-M4	MICROCIRCUIT: Type 946, quad two-input NAND gate integrated circuit	950 105 002
Q1, Q3, Q5, Q7, Q9, Q11, Q13, Q15	TRANSISTOR	943 722 002
Q2,Q4, Q6, Q8, Q10, Q12, Q14, Q16	TRANSISTOR: Replacement Type 2N3647	943 762 001
R1-R8	RESISTOR, FIXED, COMPOSITION: 360 ohms $\pm$5%, ¼W	932 007 038





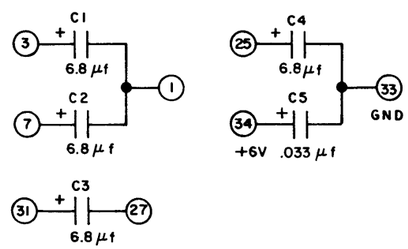


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Figure 2. Inhibit PAC, Model CM-305, Schematic Diagram and Logic Signal

SELECTOR PAC, MODEL CM-306

The Selector PAC, Model CM-306 (Figures 1 and 2) contains three registers, as well as decoding and drive circuitry for half of an 8 x 8 selection matrix. The outputs can sink or switch inductive loads of up to 400 mA with voltages up to +17V.

Registers

Three Type 932 power amplifier gates constitute the three register stages. Pin 6 is a common reset input to all three register stages. Pins 3, 14, and 20 are set inputs; pins 8, 9, and 17 are reset inputs; pins 10, 16, and 22 are set outputs.

Decoding and Drive Circuitry

Four F-13 flat packs decode the registers and sink or switch up to 400 mA of current into inductive loads. Input pin 24 at logic ONE enables the switch outputs. Pins 25 and 28 are inputs to a NAND gate whose output, at logic ONE, activates the sink outputs. Only one output (sink or switch) of an F-13 can be activated during a given cycle.

The expansion input, pin 4, must be at logic ONE to enable the CM-306 PAC.

Input and Output Signals

Table 1 lists logic levels on various pins and the resulting active outputs.

TABLE 1
INPUT/OUTPUT LOGIC SIGNALS

Pin 20 (A3+)	Pin 14 (A2+)	Pin 3 (A1+)	Pin 24 (Timing Switch)	Pins 25 & 28 (Timing Sink)	Active Output Pin No.
0	0	0	0	1	11
0	0	0	1	0	13
0	0	1	0	1	18
0	0	1	1	0	15
0	1	0	0	1	27
0	1	0	1	0	30
0	1	1	0	1	31
0	1	1	1	0	32
1	0	0	0	1	1
1	0	0	1	0	5
1	0	1	0	1	12
1	0	1	1	0	7
1	1	0	0	1	19
1	1	0	1	0	21
1	1	1	0	1	26
1	1	1	1	0	23

Specifications

Input Loading

Address Inputs	1 unit load
Reset Input	3 unit loads
Expansion Input	6 unit loads
Timing Inputs	1 unit load

Output Characteristics

Current (sink or switch)	400 mA (max)
Voltage (sink or switch)	17 V (max)
Power (sink or switch)	560 mW (max)
Collector-Emitter Saturation Voltage (sink or switch)	0.9V (max)
Register Set Output	4 unit loads

Circuit Delay (400 mA Resistance Load)

Turn-on Delay (1.5V of timing input to 10% of current)	Sink	80 ns
	Switch	50 ns
Turn-off Delay (2.2V of timing input to 10% of current)	Sink	200 ns
	Switch	80 ns
Rise-Fall Time	Sink	40 ns
	Switch	40 ns

Current Requirements

100 mA at +14V
45 mA at +6V

Power Dissipation

2.5W (max)

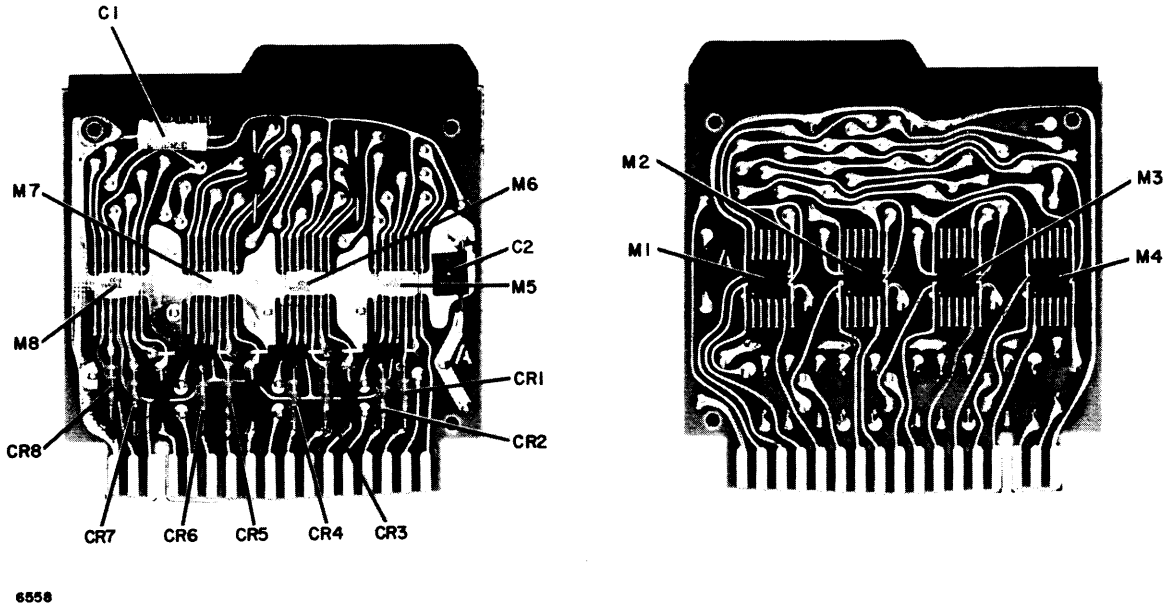


Figure 1. Selector PAC, Model CM-306, Parts Locations

ELECTRICAL PARTS LIST

Reference Designation	Description	CCD Part No.
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μF ±20%, 50 Vdc	930 313 016
C2	CAPACITOR, FIXED, SOLID TANTALUM: 6.8 μF ±20%, 10 Vdc	930 235 011
CR1-CR8	DIODE, SILICON	943 087 001
M1-M4	MICROCIRCUIT: Type 932, dual four-input current driver integrated circuit	950 105 005
M5-M8	MICROCIRCUIT: F-13, selection switch integrated circuit	950 100 013

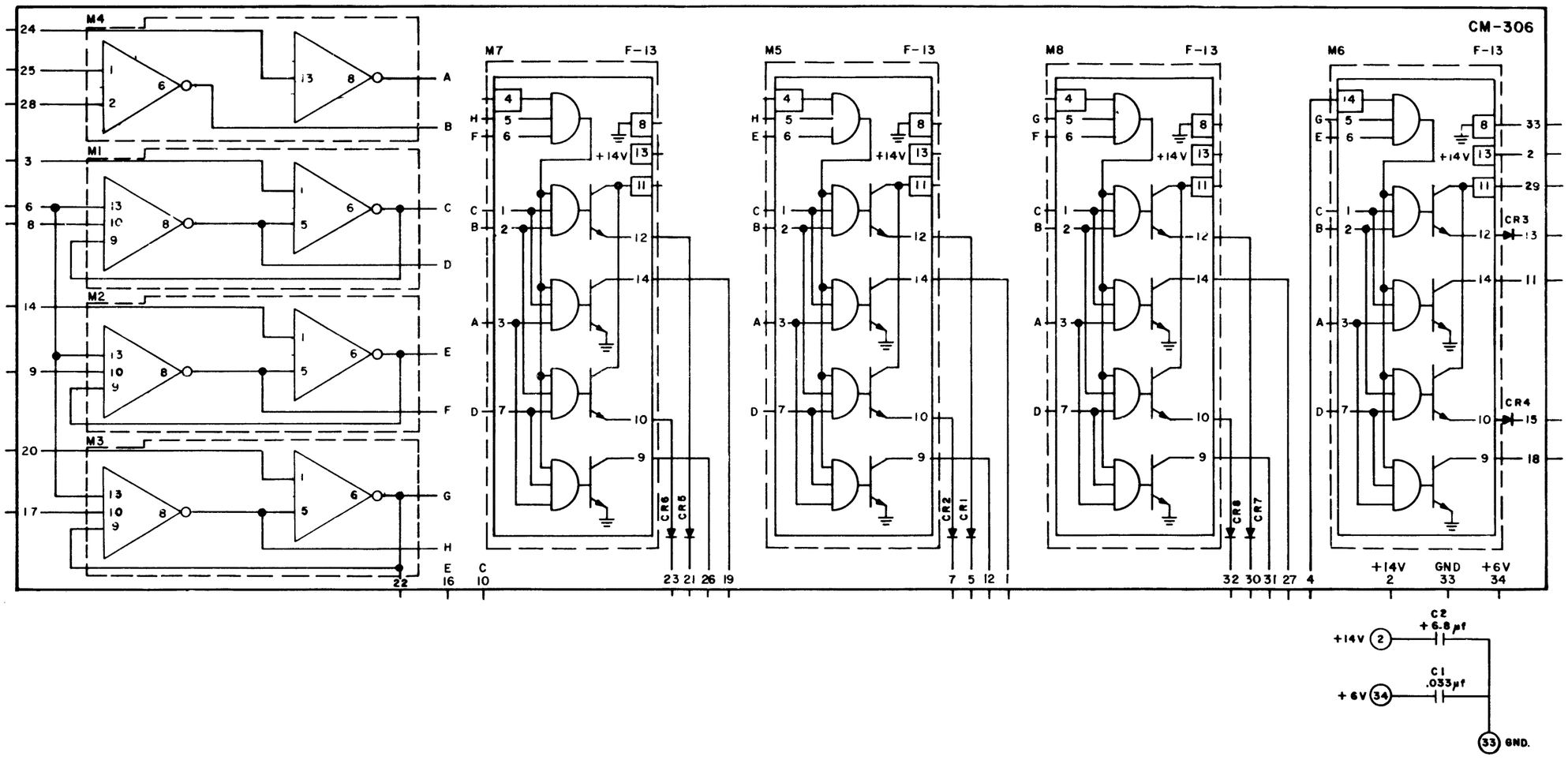


Figure 2. Selector PAC, Model CM-306, Schematic Diagram and Logic Symbol

SENSE AMPLIFIER PAC, MODEL CM-363

The Sense Amplifier PAC, Model CM-363 (Figure 1 and 2), contains four dual-in-line integrated circuit sense amplifiers, each of which contains two complete amplifier circuits capable of detecting and amplifying core signals. Each circuit has its own strobe input, all inputs being driven by the same buffer amplifier. A resistor divider network determines the threshold voltage for the eight circuits. Each amplifier output is connected to an inverter gate. The μ-PAC also contains the sense line termination resistors for each circuit.

Circuit Function

A differential signal which is greater than the threshold voltage will produce a positive sense amplifier output if the strobe circuit is enabled. A negative strobe signal applied to the strobe buffer amplifier will enable the strobe gate, and a positive signal will disable it. The sense amplifier output will be inverted, making a negative signal available to perform a logical OR function.

Specifications

Strobe Input

Input loading: 1.6 mA
Width: 180 ns $\pm$ 10 ns

Sense Inputs

Minimum Assertion signal: 37 mV
Maximum Negation signal: 10 mV

Current Requirements

+6V: 332 mA (max)
-6V: 80 mA (max)

Power Dissipation

2.5W (max)

Output

Delay from strobe input to PAC output
- Leading edge: 100 ns (max)
- Trailing edge: 120 ns (max)

Pulse width with 150 ns strobe input
- Pulse width: 150 ns (min)

Drive capability: 12.8 mA

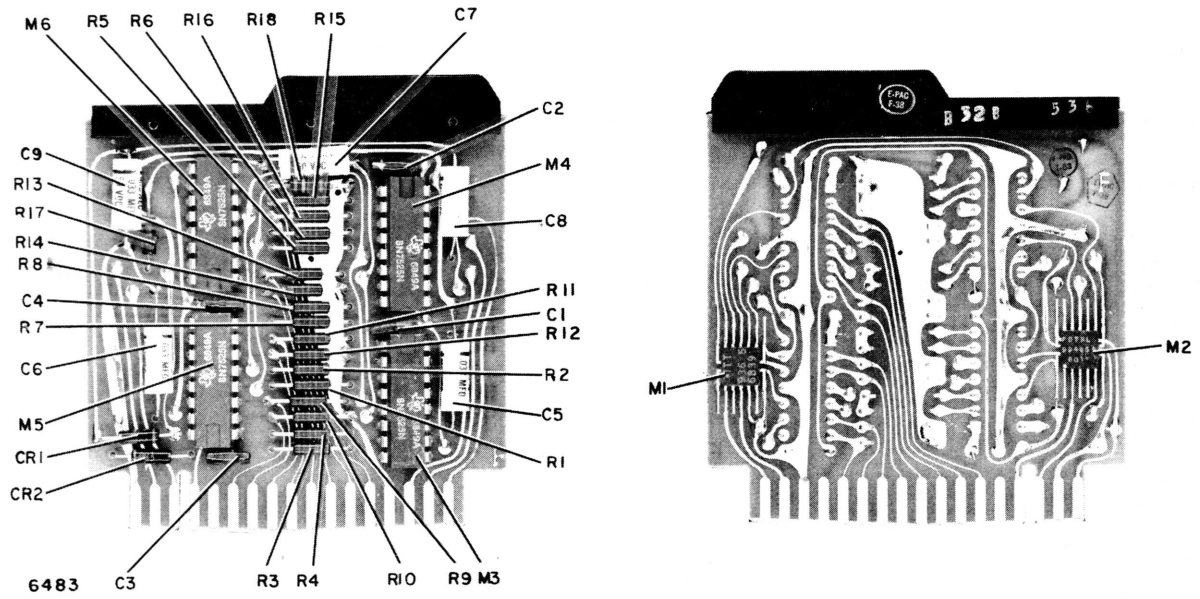
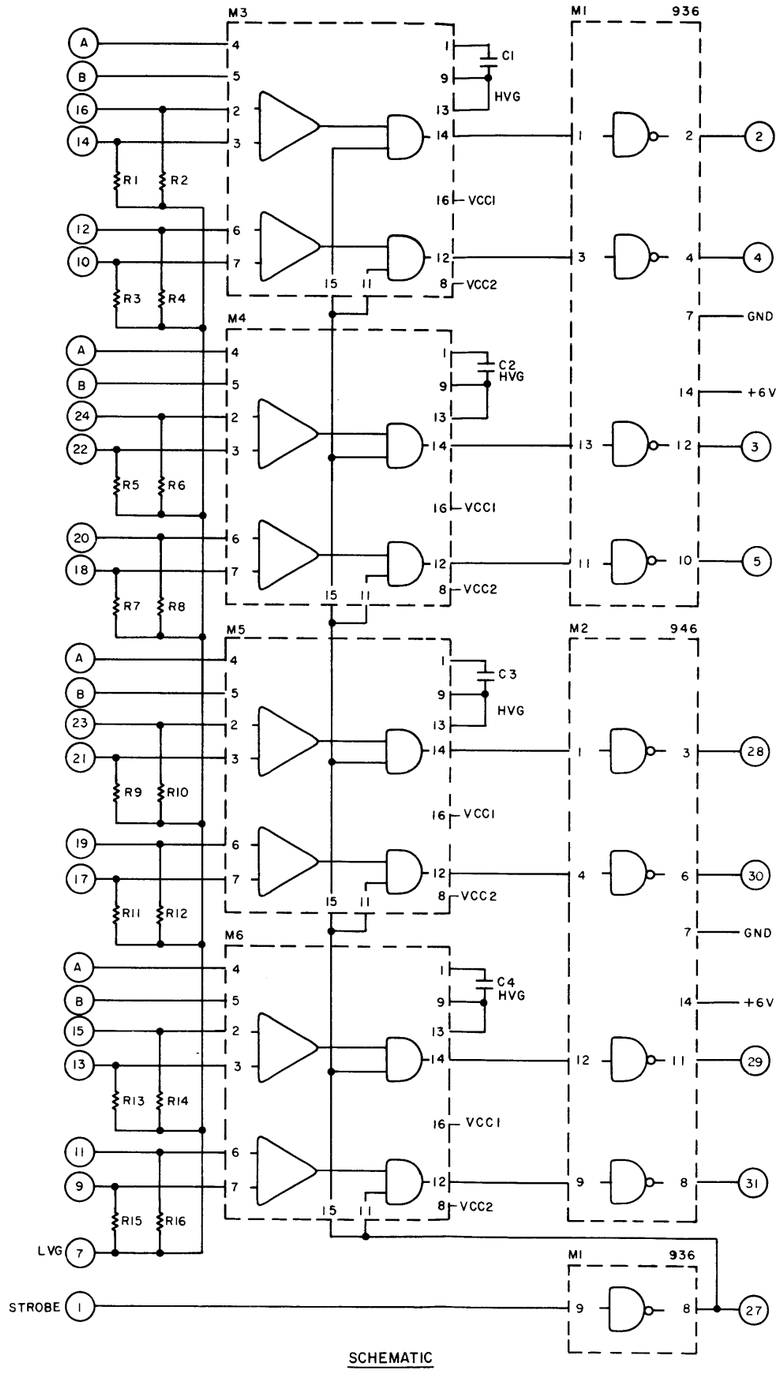


Figure 1. Sense Amplifier PAC, Model CM-363, Parts Locations

ELECTRICAL PARTS LIST

Reference Designation	Description	CCD Part No.
C1-C4	CAPACITOR, FIXED, MICA DIELECTRIC: 120 pF ±10%, 100 Vdc	70 930 004 019
C5-C9	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μF ±20%, 50 Vdc	70 930 313 021
CR1, CR2	DIODE, SILICON	70 943 083 001
M1	MICROCIRCUIT: Type 936, hex inverter integrated circuit	70 950 105 004
M2	MICROCIRCUIT: Type 946, quad two-input NAND gate integrated circuit	70 950 105 002
M3-M6	MICROCIRCUIT: Dual-in-line sense amplifier integrated circuit	70 950 100 034
R1-R16	RESISTOR, FIXED, FILM: 150 ohms ±2%, ¼W	70 932 114 029
R17	RESISTOR, FIXED, COMPOSITION: 9.1K ohms ±5%, ¼W	70 932 007 072
R18	RESISTOR, FIXED, COMPOSITION: 27 ohms ±5%, ¼W	70 932 007 011



SCHEMATIC

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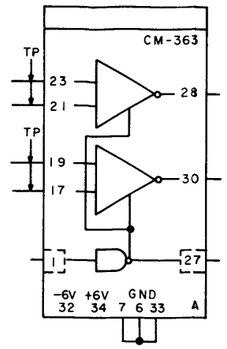
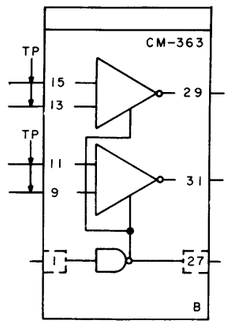
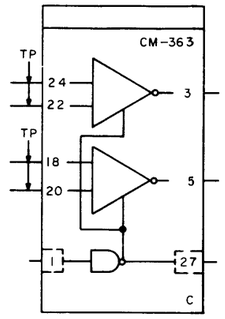
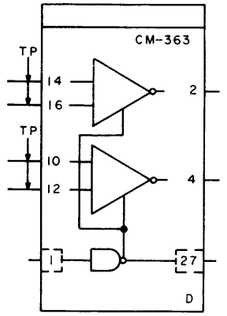
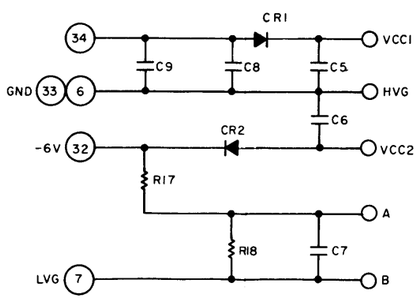








LOGIC SYMBOL



LEGEND

(1) PIN NUMBER OF PAC

⊣2 PIN NUMBER OF MICROCIRCUIT

M3 REFERENCE DESIGNATION OF MICROCIRCUIT

363 TYPE OF MICROCIRCUIT

Figure 2. Sense Amplifier PAC, Model CM-363, Schematic Diagram and Logic Symbol

RESISTOR PAC, MODEL CM-384

The Resistor PAC, Model CM-384 (Figures 1 and 2), contains twenty 3-watt, wire-wound resistors. Sixteen of these resistors (R1 through R16) are used as current limiting resistors for the inhibit drive lines. The four noninductive resistors form two groups of parallel pairs used as current-limiting resistors for the X- and Y-drive lines.

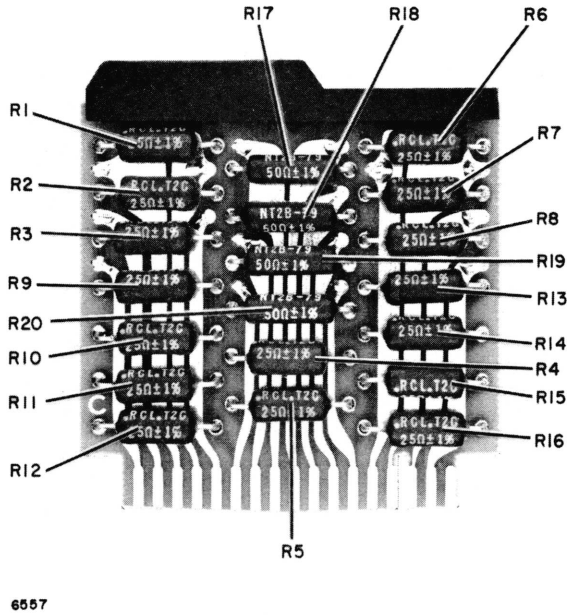
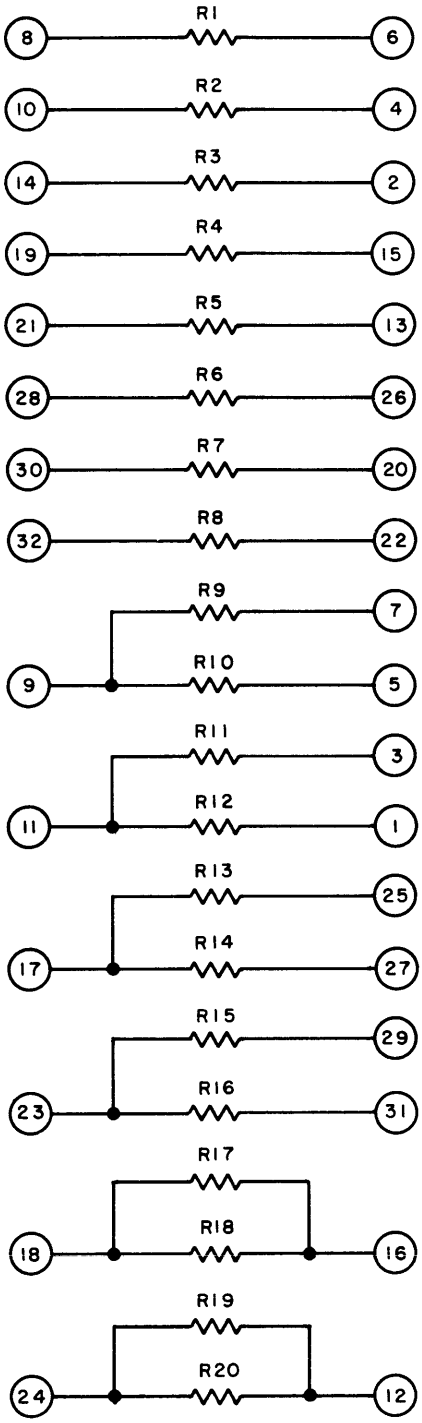


Figure 1. Resistor PAC, Model CM-384, Parts Locations

ELECTRICAL PARTS LIST

Reference Designation	Description	CCD Part No.
R1-R16	RESISTOR, FIXED, WIRE-WOUND: 25 ohms ±1%, 3W	70 932 206 408
R17-R20	RESISTOR, FIXED, WIRE-WOUND: 50 ohms ±1%, 3W, noninductive	70 932 223 122



5942

Figure 2. Resistor PAC, Model CM-384, Schematic Diagram

INHIBIT PAC, MODEL CM-488

The Inhibit PAC, Model CM-488 (Figures 1 and 2), contains a group of four 500 nsec transistor switches and one NAND gate. Each switch is controlled by a data input and strobed by a common line within each circuit.

An output switch is turned on (logic ZERO) when the corresponding data input is at logic ZERO, the timing input for circuits A, B, and C is at logic ONE, and the timing input for circuit D is at logic ZERO.

The emitters of the output transistors are brought out to external pins 1 and 27. Optional capacitors C1, C2, and C3 are provided for filtering the +14V supply. Clamp diodes at each collector are used with inductive loads.

Specifications

Frequency of Operation

DC to 2 MHz

Input Loading

1 unit load each

Output Characteristics

Current:	425 mA (max)
Voltage:	30 V (max)
Power:	200 mW (max)

Current Requirements

+6V:	70 mA

Circuit Delay (425 mA Resistive Load)

Turn-on Delay (1.5V of input to 10% of current)	190 ns (max) 30 ns (min)
Turn-off Delay (1.5V of input to 90% of current)	190 ns (max) 30 ns (min)
Rise-fall Time (10%-90%)	35 ns (max)

Power Dissipation

2.2 W (max)

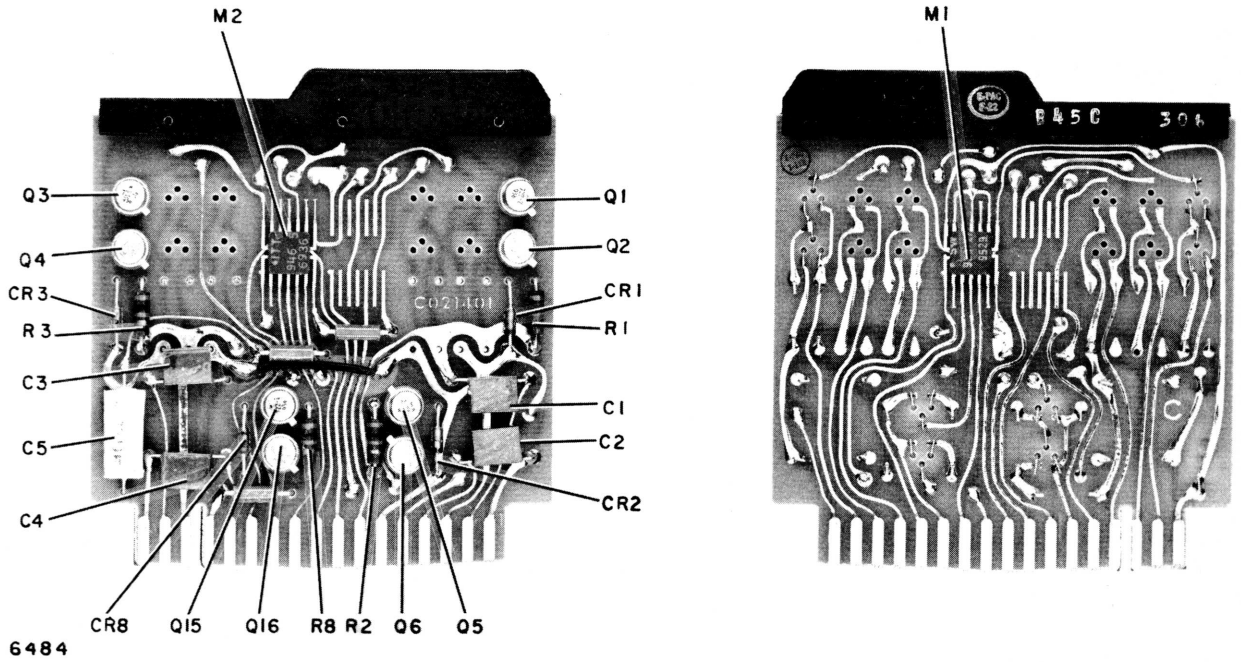


Figure 1. Inhibit PAC, Model CM-488, Parts Locations

ELECTRICAL PARTS LIST

Reference Designation	Description	CCD Part No.
C1-C4	CAPACITOR, FIXED, SOLID TANTALUM: 6.8 μF $\pm$5%, 20 Vdc	70 930 235 011
C5	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μF $\pm$5%, 20 Vdc	70 930 313 016
CR1-CR4	DIODE, SILICON	70 943 083 003
M1	MICROCIRCUIT: Type 936, hex single-input inverter integrated circuit	70 950 105 004
M2	MICROCIRCUIT: Type 946, quad two-input NAND gate integrated circuit	70 950 105 002
Q1, Q3, Q5, Q7	TRANSISTOR	70 943 722 002
Q2, Q4, Q6, Q8	TRANSISTOR: Replacement Type 2N3647	70 943 762 001
R1-R4	RESISTOR, FIXED, COMPOSITION: 100 ohms $\pm$5%, ¼W	70 932 007 025

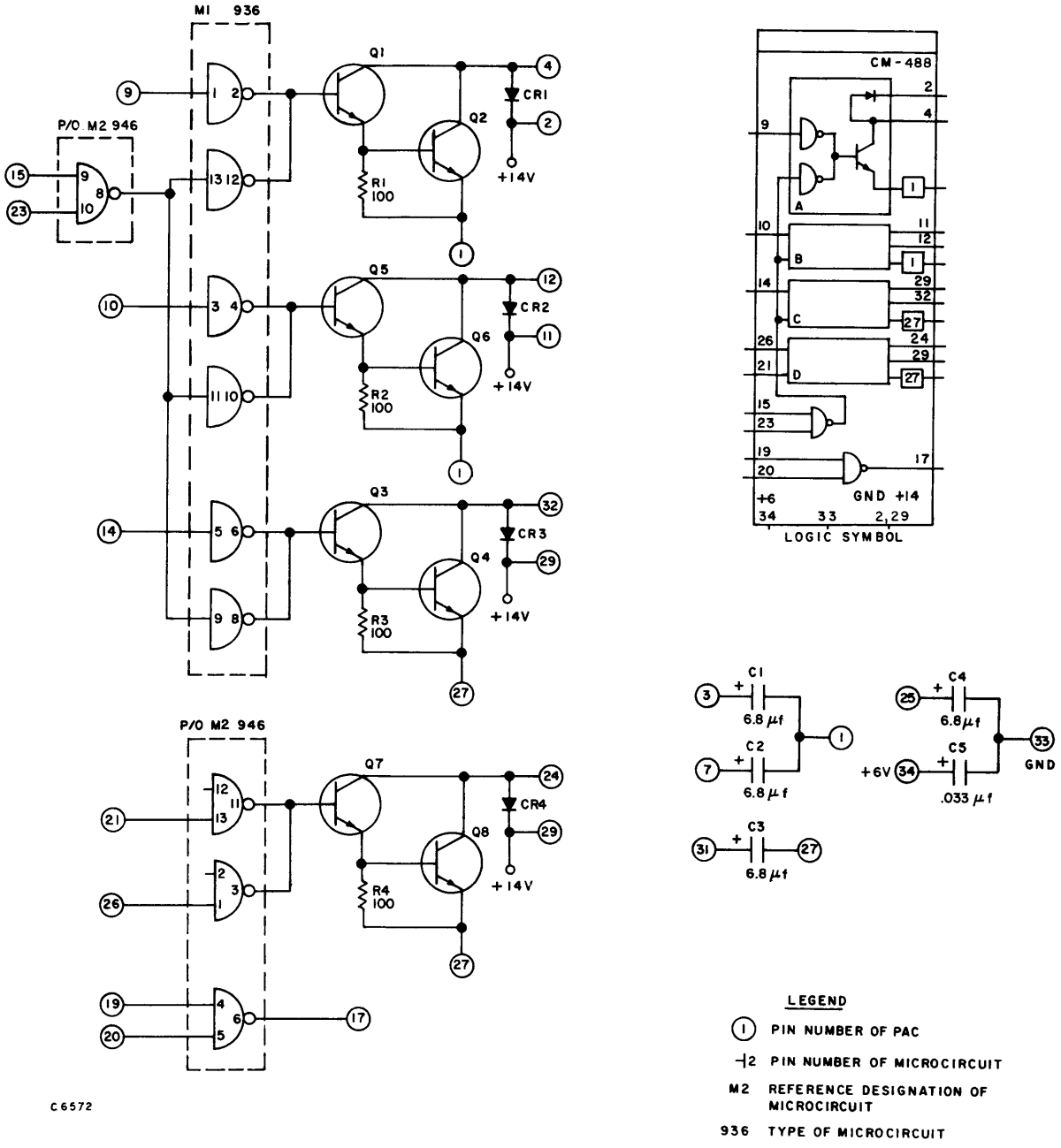


Figure 2. Inhibit PAC, Model CM-488, Schematic Diagram and Logic Symbol

SENSE AMPLIFIER PAC, MODEL CM-489

The Sense Amplifier PAC, Model CM-489, (Figures 1 and 2), contains two dual-in-line integrated circuit sense amplifiers, each of which contains two complete amplifier circuits capable of detecting and amplifying core signals. Each circuit has its own strobe input, all inputs being driven by the same buffer amplifier. A resistor divider network determines the threshold voltage for the four circuits. Each amplifier output is connected to an inverter gate. The μ-PAC also contains the sense line termination resistors for each circuit.

Circuit Function

A differential signal which is greater than the threshold voltage will produce a positive sense amplifier output if the strobe circuit is enabled. A negative strobe signal applied to the strobe buffer amplifier will enable the strobe gate, and a positive signal will disable it. The sense amplifier output will be inverted, making a negative signal available to perform a logical OR function.

Specifications

Strobe Input

Input loading: 1.6 mA
Width: 180 ns $\pm$ 10 ns

Sense Inputs

Minimum Assertion signal: 37 mV
Maximum Negation signal: 10 mV

Current Requirements

+6V: 332 mA (max)
-6V: 80 mA (max)

Power Dissipation

2.5W (max)

Output

Delay from strobe input to PAC output
- Leading edge: 100 ns (max)
- Trailing edge: 120 ns (max)

Pulse width with 150 ns strobe input
- Pulse width: 150 ns (min)

Drive capability: 12.8 mA

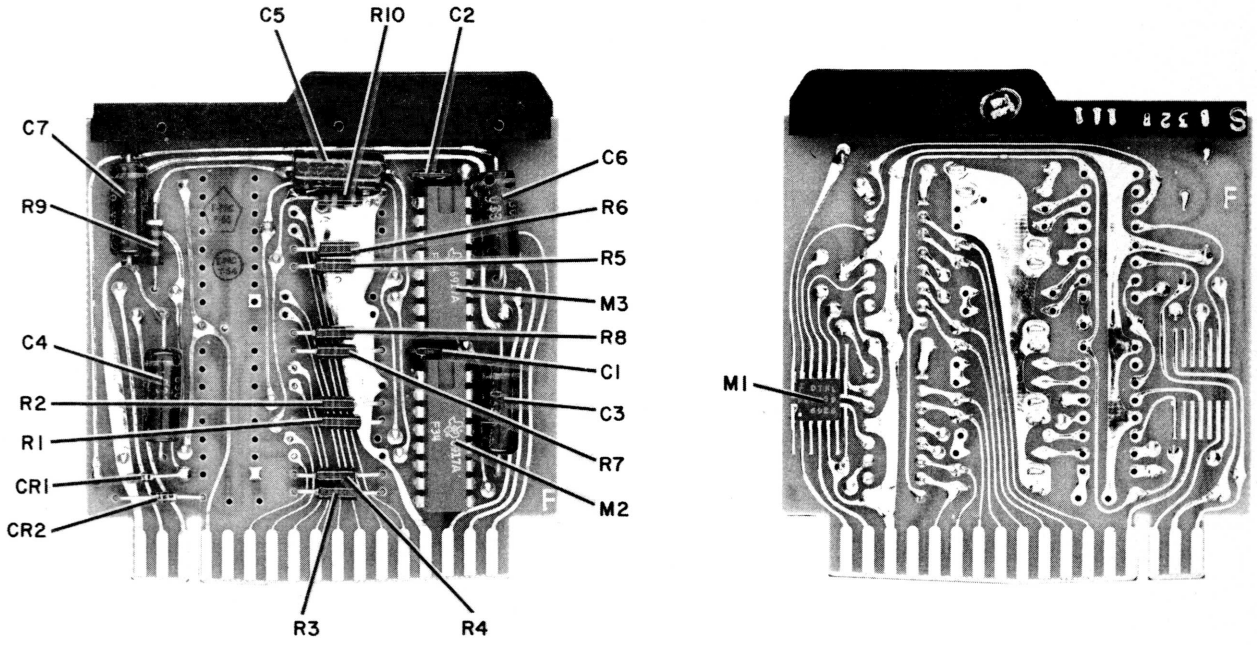
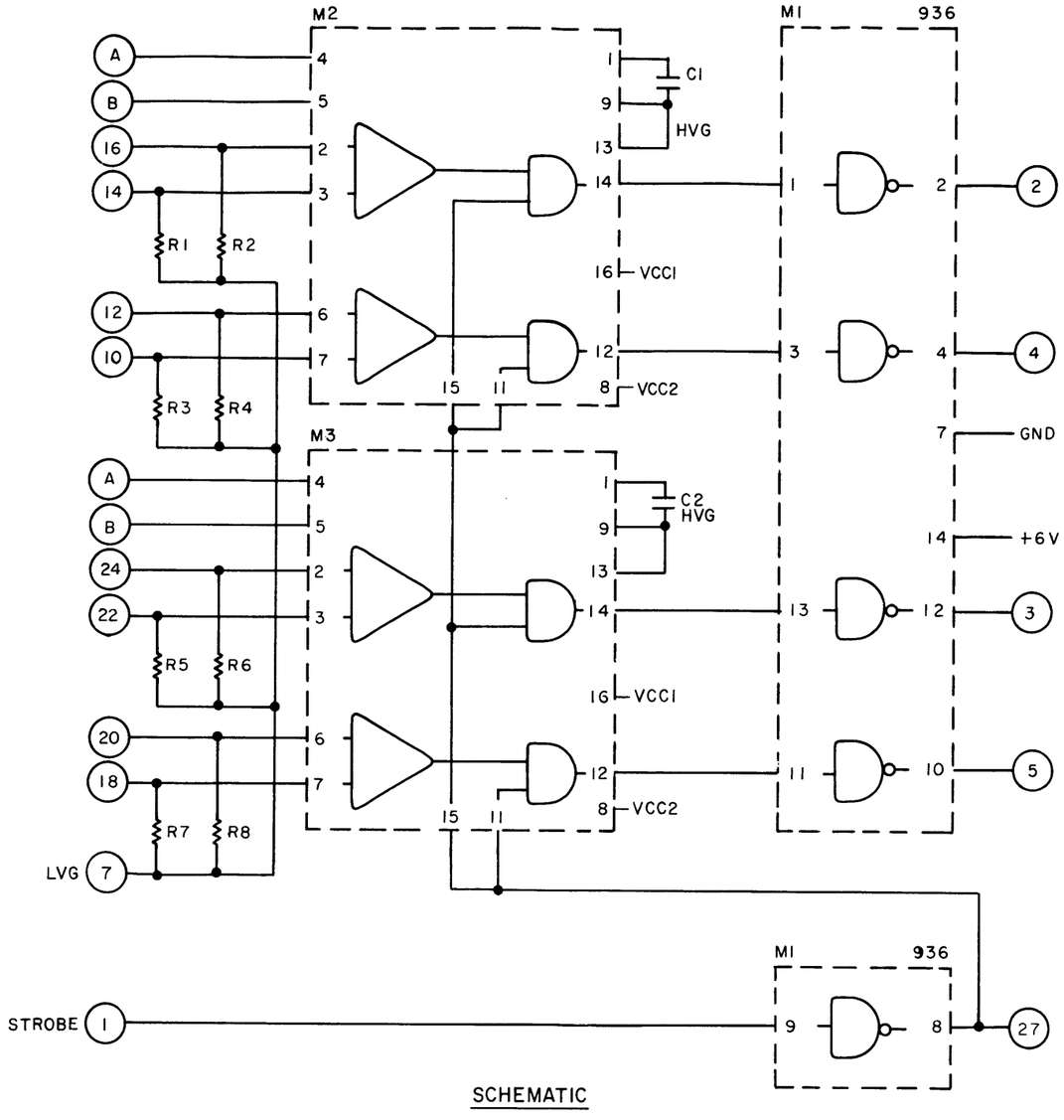


Figure 1. Sense Amplifier PAC, Model CM-489, Parts Locations

ELECTRICAL PARTS LIST

Reference Designation	Description	CCD Part No.
C1, C2	CAPACITOR, FIXED, MICA DIELECTRIC: 120 pF ±10%, 100 Vdc	70 930 016 030
C3-C7	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μF ±20%, 50 Vdc	70 930 313 021
CR1, CR2	DIODE, SILICON	70 943 083 001
M1	MICROCIRCUIT: Type 936, hex inverter integrated circuit	70 950 105 004
M2, M3	MICROCIRCUIT: Dual-in-line sense amplifier integrated circuit	70 950 100 034
R1-R8	RESISTOR, FIXED, FILM: 150 ohms ±2%, ¼W	70 932 114 029
R9	RESISTOR, FIXED, COMPOSITION: 9.1K ohms ±5%, ¼W	70 932 007 072
R10	RESISTOR, FIXED, COMPOSITION: 27 ohms ±5%, ¼W	70 932 007 011



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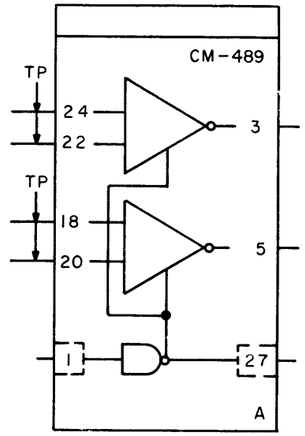
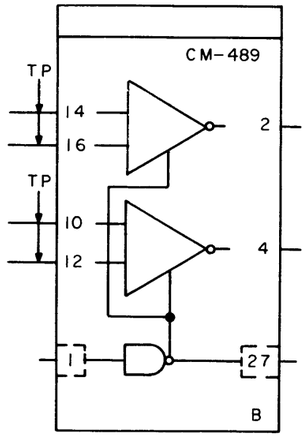
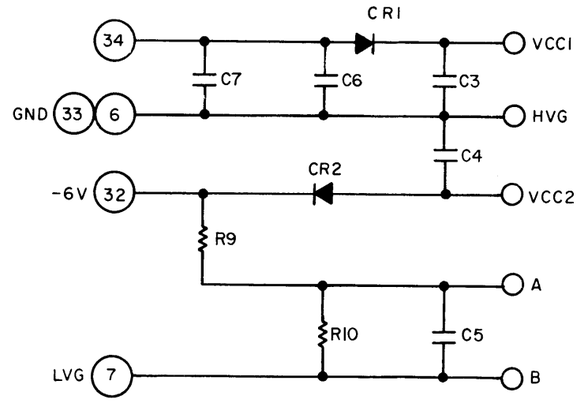




LOGIC SYMBOL



LEGEND

(1)	PIN NUMBER OF PAC
—|2	PIN NUMBER OF MICROCIRCUIT
M3	REFERENCE DESIGNATION OF MICROCIRCUIT
363	TYPE OF MICROCIRCUIT

C6568

Figure 2. Sense Amplifier PAC, Model CM-489, Schematic Diagram and Logic Symbol

TIMING DISTRIBUTOR PAC, MODEL CM-490

The Timing Distributor PAC, Model CM-490 (Figures 1 - 3), provides accurately timed pulse sequences for use in timing and control applications. The CM-490 contains one control flip-flop, a 300-ns-long delay line with 12-ns taps, a 50-ns-long vernier delay line with 6-ns taps, and nine inverting power amplifier output circuits.

The PAC consists of two double-sided printed circuit boards sandwiched together for ease of mounting in a μ-BLOC. Board A, which plugs into the connector, contains the four delay lines (DL1 through DL4) and five F-03 microcircuit power amplifiers. The delay lines are positioned between the two circuit boards to expose the etched side of board A for timing jumper adjustment.

Board B contains an F-04 microcircuit flip-flop, discrete drivers, and termination loads.

Note

The CM-490 PAC occupies two slots in a taper-pin BLOC and three slots in a solderless-wrap BLOC, or the end slot (position 1) in either.

Circuit Function

Delay lines DL1 through DL3 can be tapped and jumpered to the output power amplifiers and the vernier delay line, DL4, to provide accurately timed output pulses. Input connection points for each amplifier are located on the PAC to facilitate timing flexibility. Refer to Table 1 and Figure 3.

The dc reset of the flip-flop may also be tapped from any point along DL1 through DL3 to allow recirculation of the opposite driving edge, thereby establishing fixed pulse widths. An ac set, a dc reset, and the two outputs of the flip-flop are brought to the PAC connector.

Delay line DL4 and its associated output power amplifiers may be interconnected to provide pulses with a 6-ns delay resolution.

Specifications

Input Loading

Flip-flop dc reset:	2/3 unit load
Flip-flop ac set:	1 unit load
Power amplifiers:	2 unit loads each

Delay Line (DL1 through DL3)

Length:	300 ns $\pm$5%, 24 taps, each 12.5 $\pm$1 ns
Minimum pulse width:	85 ns
Maximum pulse width:	330 ns

Circuit Delay

Flip-flop:

Set input to set output or reset input to reset output

65 ns (typ); 80 ns (max)

Set input to reset output or reset input to set output

45 ns (typ); 60 ns (max)

Power amplifiers:

24 ns (typ); 30 ns (max) each

Delay to first tap (C1):

60 ns (typ); 80 ns (max)

Output Drive Capability

Flip-flop set:	8 unit loads
Flip-flop reset:	4 unit loads
Power amplifiers:	25 unit loads each

Vernier Delay Line (DL4)

Length: 50 ns $\pm$5%, 8 taps, each 6 $\pm$1 ns

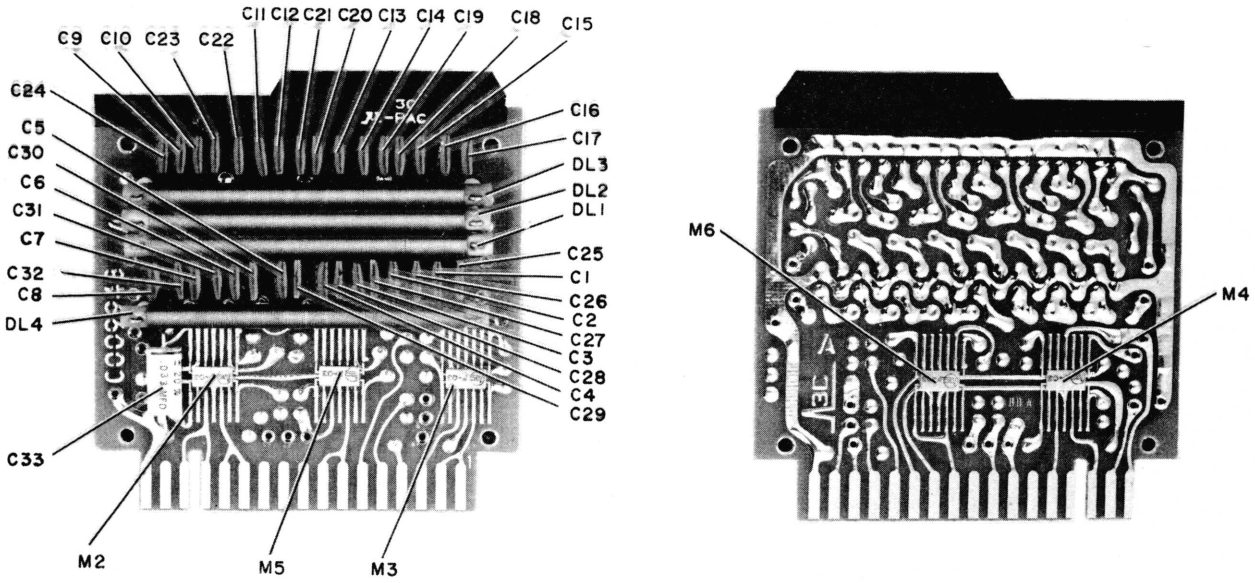
Current Requirements

+6V:	175 mA
-6V:	100 mA

Power Dissipation

1.10W (max)

Board A



Board B

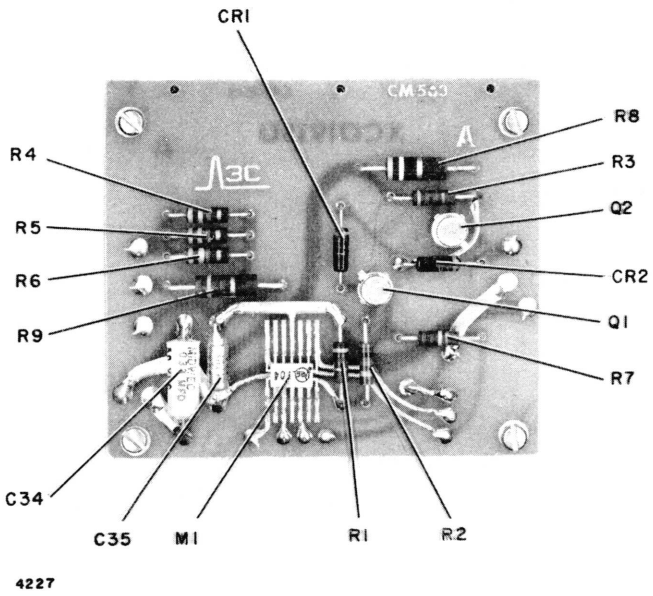
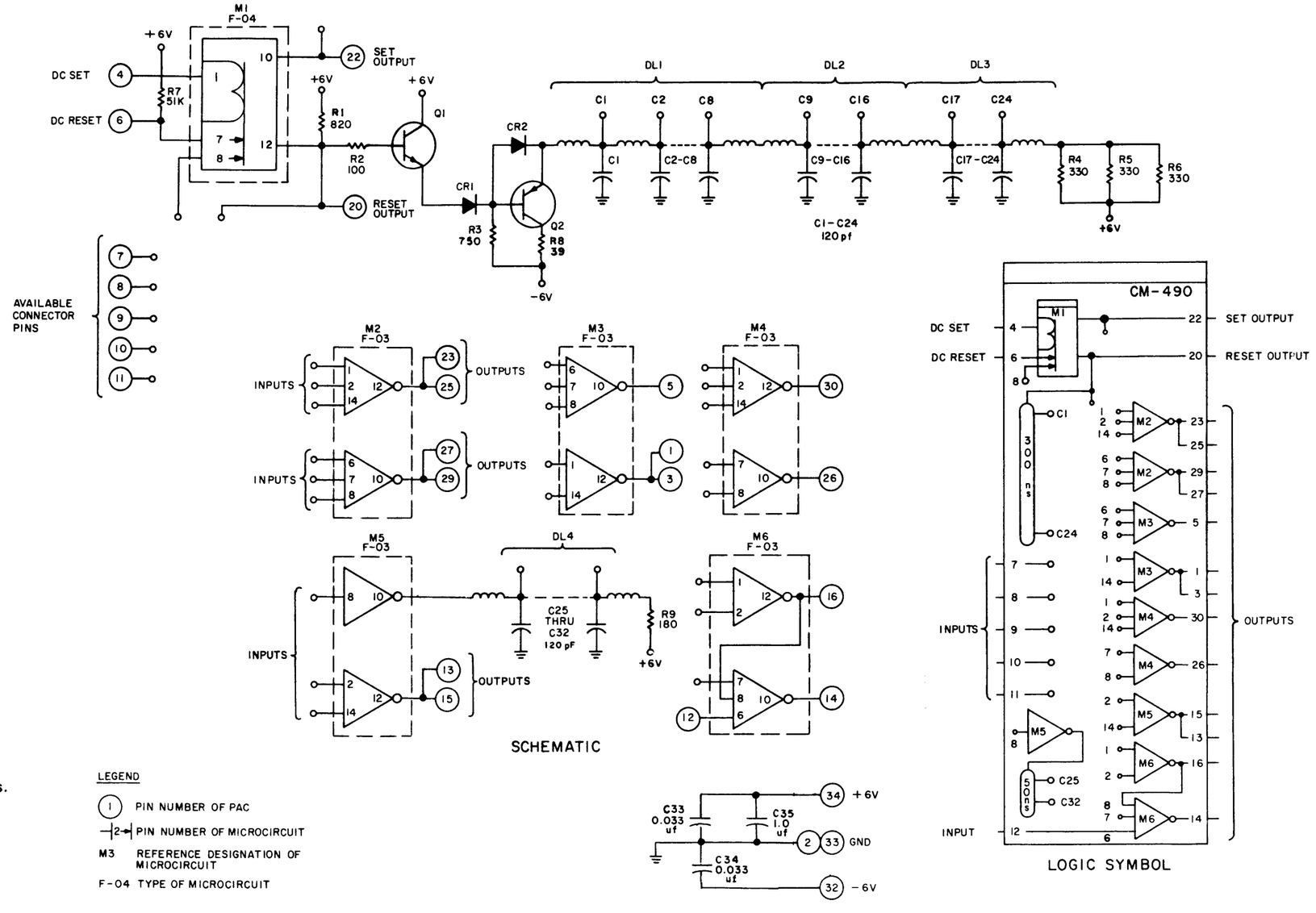


Figure 1. Timing Distributor PAC, Model CM-490, Parts Locations

ELECTRICAL PARTS LIST

Reference Designation	Description	CCD Part No.
C1-C32	CAPACITOR, FIXED, MICA DIELECTRIC: 120 pF ±2%, 100 Vdc	930 004 219
C33, C34	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μF ±20%, 50 Vdc	930 313 016
C35	CAPACITOR, FIXED, TANTALUM ELECTROLYTIC: 1.0 μF ±20%, 35 Vdc	930 217 015
CR1, CR2	DIODE	943 088 001
DL1-DL4	COIL, DELAY LINE	B000 206 703
M1	MICROCIRCUIT: F-04, flip-flop integrated circuit	950 100 004
M2-M6	MICROCIRCUIT: F-03, power amplifier integrated circuit	950 100 003
Q1	TRANSISTOR: Replacement Type 2N3011	943 722 002
Q2	TRANSISTOR: Replacement Type 2N3012	943 721 002
R1	RESISTOR, FIXED, COMPOSITION: 820 ohms ±5%, ¼W	932 007 047
R2	RESISTOR, FIXED, COMPOSITION: 100 ohms ±5%, ¼W	932 007 025
R3	RESISTOR, FIXED, COMPOSITION: 750 ohms ±5%, ¼W	932 007 046
R4-R6	RESISTOR, FIXED, COMPOSITION: 330 ohms ±5%, ¼W	932 007 037
R7	RESISTOR, FIXED, COMPOSITION: 51K ±5%, ¼W	932 007 090
R8	RESISTOR, FIXED, COMPOSITION: 39 ohms ±5%, ½W	932 004 015
R9	RESISTOR, FIXED, COMPOSITION: 180 ohms ±5%, ½W	932 004 031



NOTES

TAP DESIGNATIONS REFER TO CIRCUIT COMPONENTS.
EXAMPLE: C1 TO TAP AT C1; M3-8 TO TAP AT M-3, PIN 8, 10 TO TAP AT PIN 10 OF PAC.

REFER TO TABLE I FOR DELAY LINE DELAYS IN NANOSECONDS.

B6573

LEGEND

(1) PIN NUMBER OF PAC

—|2→ PIN NUMBER OF MICROCIRCUIT

M3 REFERENCE DESIGNATION OF MICROCIRCUIT

F-04 TYPE OF MICROCIRCUIT

Figure 2 Timing Distributor PAC, Model CM-490, Schematic Diagram and Logic Symbol

TABLE 1
DELAY LINE TAP POINTS WITH CORRESPONDING DELAY LINE DELAYS
(Refer to Figure 2)

Delay Line Jumper Connection	Delay Line Delay (ns)	Delay Line Jumper Connection	Delay Line Delay (ns)
C1	12	C19	228
C2	24	C20	240
C3	36	C21	252
C4	48	C22	264
C5	60	C23	276
C6	72	C24	288
C7	84		
C8	96		
C9	108		
C10	120		
C11	132	C25	6
C12	144	C26	12
C13	156	C27	18
C14	168	C28	24
C15	180	C29	30
C16	192	C30	36
C17	204	C31	42
C18	216	C32	48

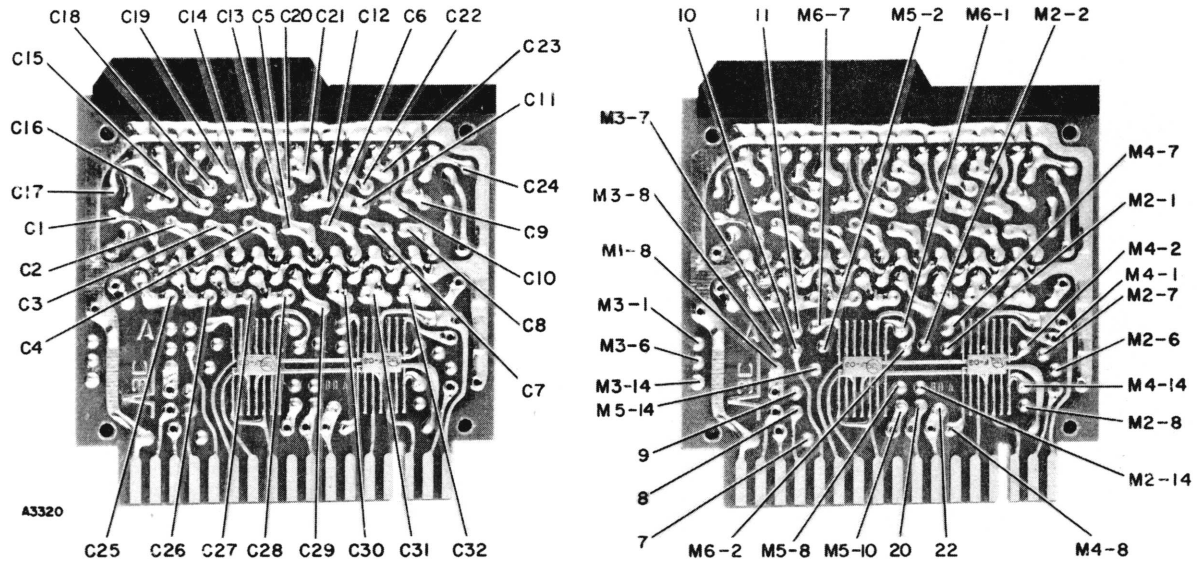


Figure 3. Timing Distributor PAC, Model CM-490, Test Points

EIGHT-BIT BINARY COUNTER PAC, MODEL CS-185

The Eight-Bit Binary Counter PAC, Model CS-185 (Figures 1 and 2), consists of two independent 4-bit binary counters. Set inputs for each stage are activated through individual inverters, strobed by a common input within each counter. A common reset, activated through an inverter, is contained in each 4-bit counter.

Each stage has a set output which may be used direct or inverted. Inverted outputs within each 4-bit counter are tied to a common strobe.

Specifications

Frequency of Operation (System)

DC to 2 MHz

Power Supply

+5V to +6V

Input Voltage

ZERO: 0.95V (max)
ONE: 2.0V (min)

Output Voltage

ZERO: 0.5V (max)
ONE: 4.3V (min for pins 4, 5, 14, 8, 18, 21, 30, 24)
2.5V (min for pins 6, 12, 16, 10, 22, 28, 32, 26)

Input Loading

Pins 17, 13, 11, 7, 1, 3, 9, 23, 15, 19, 25, 29, 27, 31:	1 unit load
Pins 2, 20:	2 unit loads

Output Drive Capability

Pins 8, 24:	10 unit loads
Pins 6, 4, 12, 5, 16, 14, 10, 8, 22, 18, 28, 21, 32, 30:	8 unit loads

Circuit Delay

Clock Input to Set Output:	45 ns to 120 ns
Clock Input to Strobed Inverted Output:	70 ns to 195 ns
DC Set/DC Common Reset to Set Output:	70 ns to 195 ns
DC Set/DC Common Reset to Strobed Inverted Output:	95 ns to 270 ns

Pulse Width

DC Set/DC Common Reset: 160 ns (min)

Clock Setup Time

80 ns (min)

Current Requirement

210 mA (max)

Power Dissipation

1.3W (max)

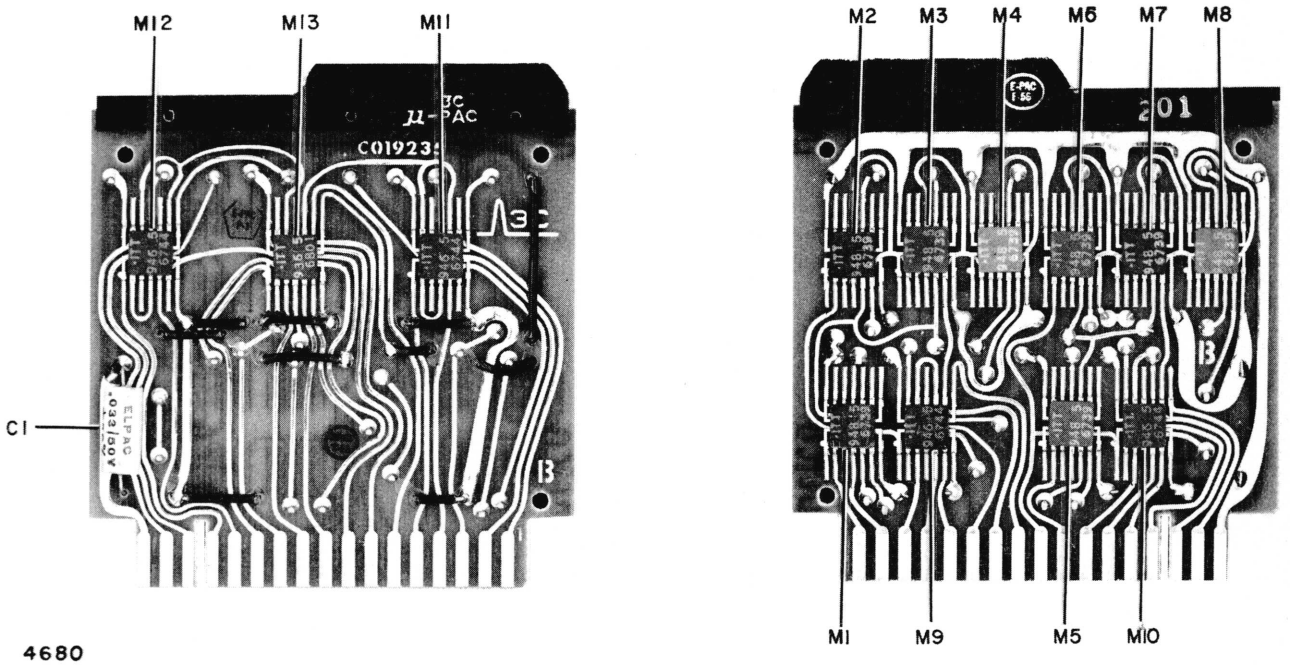
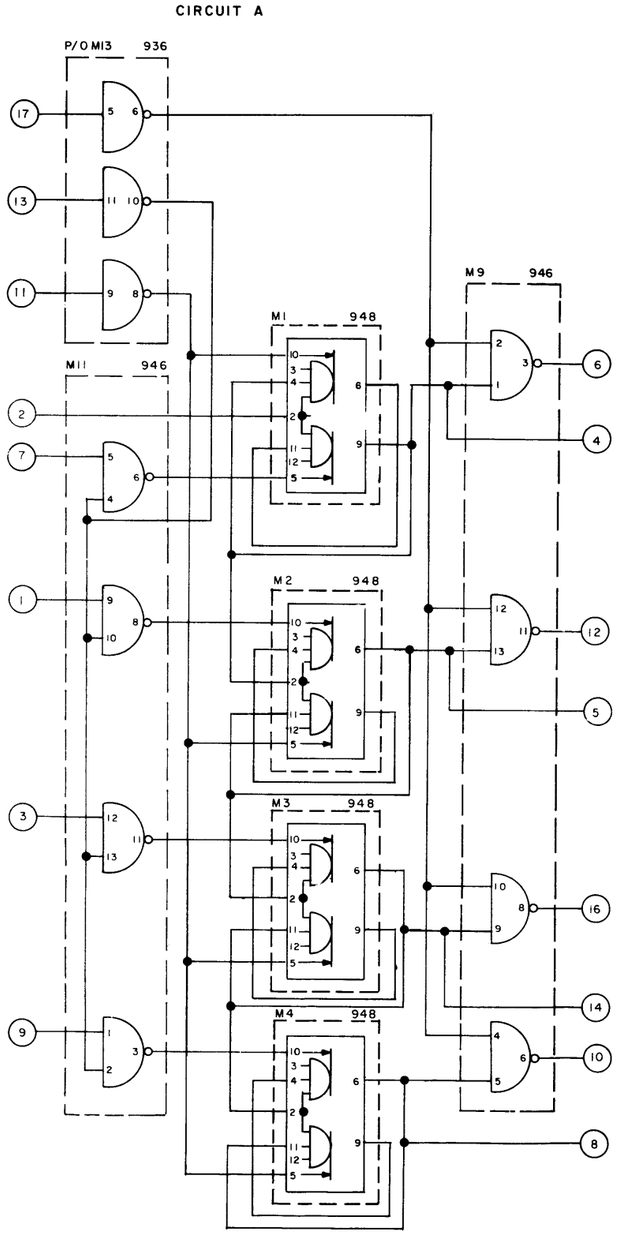
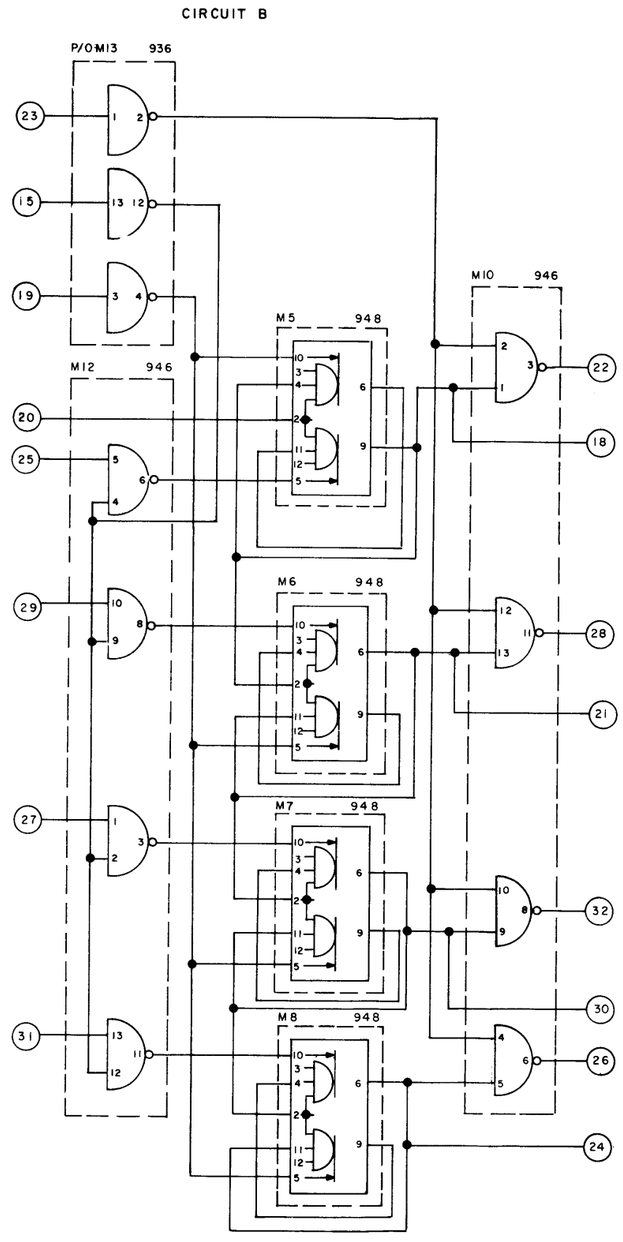


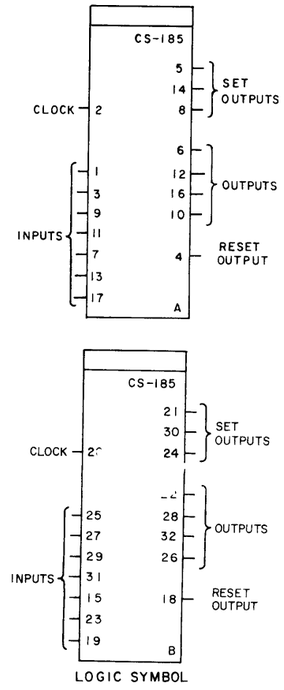
Figure 1. Eight-Bit Binary Counter PAC, Model CS-185, Parts Locations

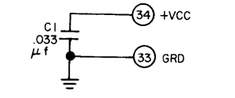
ELECTRICAL PARTS LIST

Reference Designation	Description	CCD Part No.
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μF ±20%, 50 Vdc	930 313 016
M1-M8	MICROCIRCUIT: Type 948, flip-flop integrated circuit	950 105 003
M9-M12	MICROCIRCUIT: Type 946, quad two-input NAND gate integrated circuit	950 105 002
M13	MICROCIRCUIT: Type 936, hex single-input inverter integrated circuit	950 105 004









LEGEND

(1)	PIN NUMBER OF PAC
2	PIN NUMBER OF MICROCIRCUIT
M2	REFERENCE DESIGNATION OF MICROCIRCUIT
948	TYPE OF MICROCIRCUIT

Figure 2. Eight-Bit Binary Counter PAC, Model CS-185, Schematic Diagram and Logic Symbol

DRIVER AND RECEIVER PAC, MODEL CS-517

The Driver and Receiver PAC, Model CS-517 (Figure 1), contains six line drivers and six line receivers for driving and receiving signals on the I/O bus. Driver rise and fall times are capacitor controlled. The six gated receiver outputs receive signals from the I/O bus. All circuits have built-in terminators for each signal. Pins 9 and 23 provide points for strobe signals.

Specifications

Receiver Section

Input Loading

1 unit load on pins 4, 6, 14, 16, 26, and 28

Output Drive Capacity

7 unit loads on pins 5, 1, 15, 11, 25, and 19

8 unit loads on pins 7, 3, 17, 13, 27, and 21

Circuit Delay (1.5V average over 2 stages)

75 ns

Current Requirements

+6V: 100 mA (max)

Driver Section

Input Loading

1 unit load on pins 10, 8, 22, 18, 29, and 30

Output Drive Capacity

20 loads on pins 4, 6, 14, 16, 26, and 28

Circuit Delay (1.5V average over 2 stages)

150 ns (max)

Rise and Fall Time

Rise time: 50 to 250 ns at 0 to +6V

Fall time: 50 to 100 ns at +6V to 0

Current Requirements

+6V: 100 mA (max)

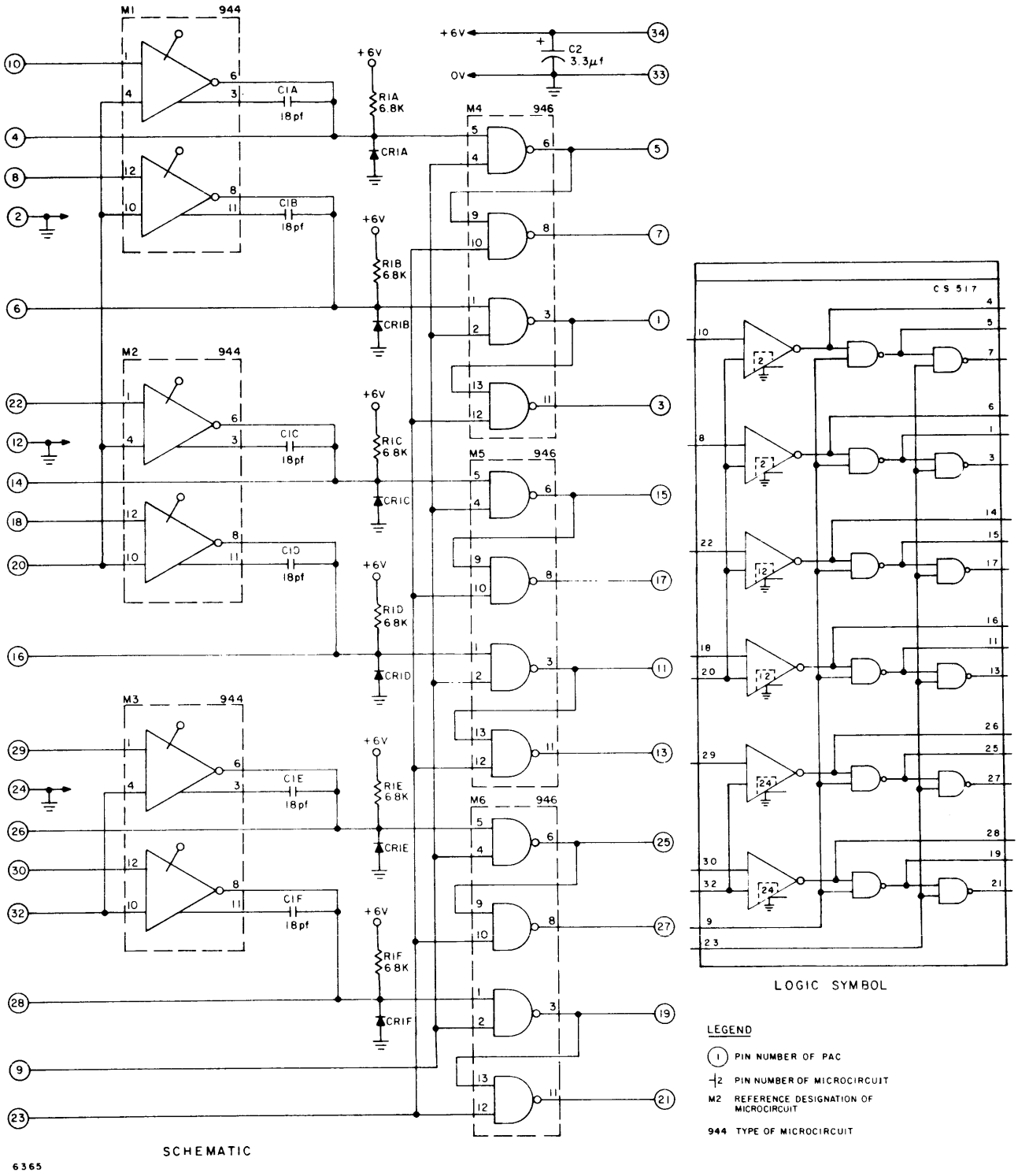


Figure 1. Driver and Receiver PAC, Model CS-517, Schematic Diagram and Logic Symbol

ELECTRICAL PARTS LIST

Reference Designation	Description	CCD Part No.
C1A-C1F	CAPACITOR, FIXED, CERAMIC, DIELECTRIC: 18 pF ±10%, 100 Vdc	70 930 173 206
C2	CAPACITOR, FIXED, ELECTROLYTIC:	70 930 230 011
CR1A-CR1F	DIODE, SILICON	70 943 083 001
R1A-R1F	RESISTOR, FIXED, FILM: 6.8K ±2%, ¼W	70 932 114 069
M1-M3	MICROCIRCUIT: Type 944, integrated circuit	70 950 105 008
M4-M6	MICROCIRCUIT: Type 946, quad NAND gate integrated circuit	70 950 105 002

RECEIVER PAC, MODEL CS-520

The Receiver PAC, Model CS-520 (Figure 1), is a line receiver with six gated outputs used to receive signals from the I/O bus on pins 4, 6, 14, 16, 26, and 28. The circuit has a built-in terminator for each signal.

Pins 9 and 23 provide points for strobe signals.

Specifications

Input Loading

1 unit load on each input pin

Output Drive Capacity

7 unit loads on pins 5, 1, 15, 11, 25, and 19
8 unit loads on pins 7, 3, 17, 13, 27, and 21

Circuit Delay

75 ns (at 1.5V average over two stages)

Current Requirements

+6V: 75 mA (max)

ELECTRICAL PARTS LIST

Reference Designation	Description	CCD Part No.
C1	CAPACITOR, FIXED, ELECTROLYTIC:	70 930 230 011
CR1A-CR1F	DIODE, SILICON	70 943 083 001
R1A-R1F	RESISTOR, FIXED, FILM: 6.8K ±2%, ¼W	70 932 114 069
M4, M5, M6	MICROCIRCUIT: Type 946, quad NAND gate integrated circuit	70 950 105 002

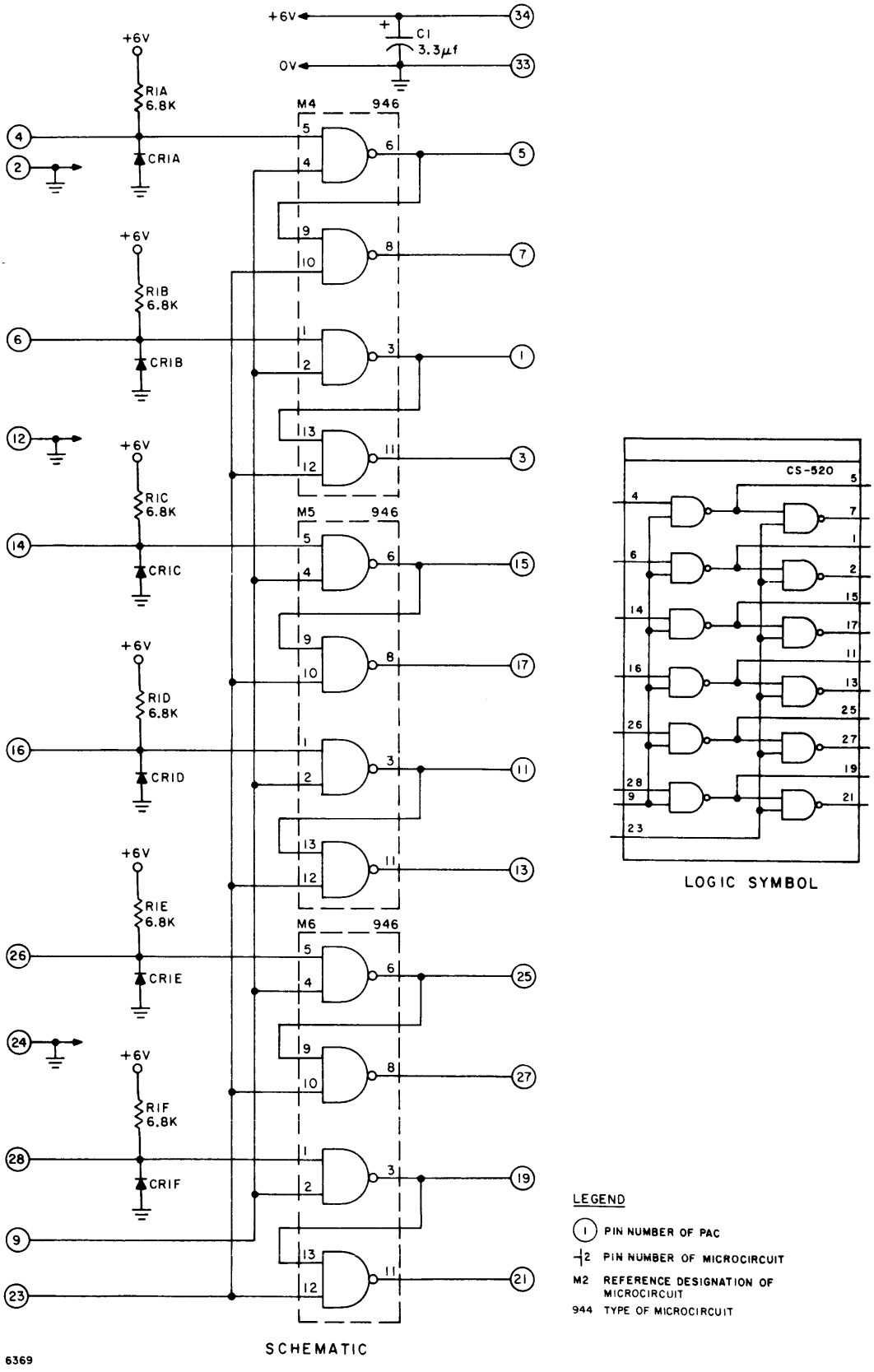


Figure 1. Receiver PAC, Model CS-520, Schematic Diagram and Logic Symbol

DRIVER PAC, MODEL CS-521

The Driver PAC, Model CS-521 (Figure 1), contains six line drivers used to drive the I/O bus. Rise and fall times are capacitor controlled and each signal has a built-in terminator.

Specifications

Input Loading

1 unit load on pins 10, 8, 22, 18, 29, and 30

Output Drive Capacity

20 loads on pins 4, 6, 14, 16, 26, and 28

Circuit Delay

150 ns (max)

Rise and Fall Times

Rise time: 50 to 250 ns at 0 to +6V
Fall time: 50 to 100 ns at +6V to 0

Current Requirements

+6V: 36 mA (max)

ELECTRICAL PARTS LIST

Reference Designation	Description	CCD Part No.
C1A-C1F	CAPACITOR, FIXED, CERAMIC DIELECTRIC: 18 pF ±10%, 100 Vdc	70 930 173 206
C2	CAPACITOR, FIXED, ELECTROLYTIC:	70 930 230 011
CR1A-CR1F	DIODE, SILICON	70 943 083 001
R1A-R1F	RESISTOR, FIXED, FILM: 6.8K ±2%, ¼W	70 932 114 069
M1-M3	MICROCIRCUIT: Type 944, integrated circuit	70 950 105 008

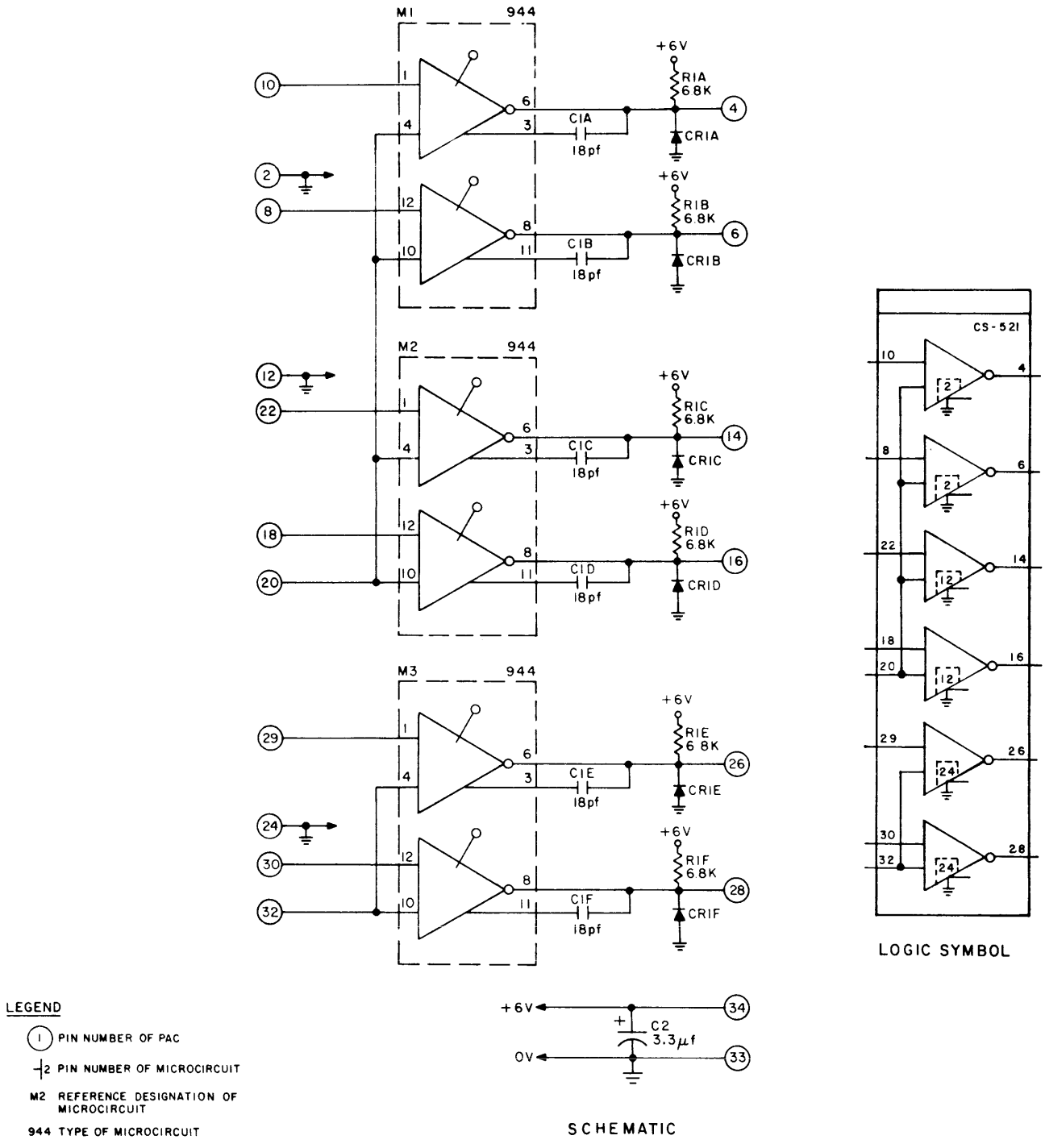


Figure 1. Driver PAC, Model CS-521, Schematic Diagram and Logic Symbol

SYSTEM NORMALIZER PAC, MODEL CS-536

The System Normalizer PAC, Model CS-536 (Figures 1 and 2), contains a time delay circuit which initially conditions system control flip-flops to the proper state (at power turn-on time).

Circuit Function

Initially the relay contacts are closed, coupling the outputs to ground. At a predetermined time after the system power supply is turned on and its voltages have stabilized, the relay contacts open and free the control flip-flops to the normal operating condition.

Specifications

Output Drive Capability

0.5A (max)
250V (max)
10W (max)

Power Dissipation

150 mW

Power Requirement

+6V: 25 mA

NOTE

The CS-536 PAC occupies two slots in a Solderless-Wrap BLOC and one slot in a Taper-Pin BLOC.

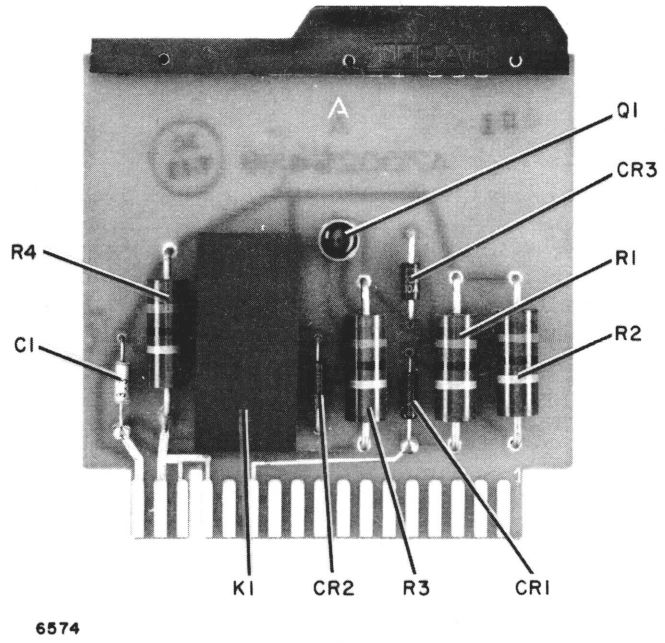
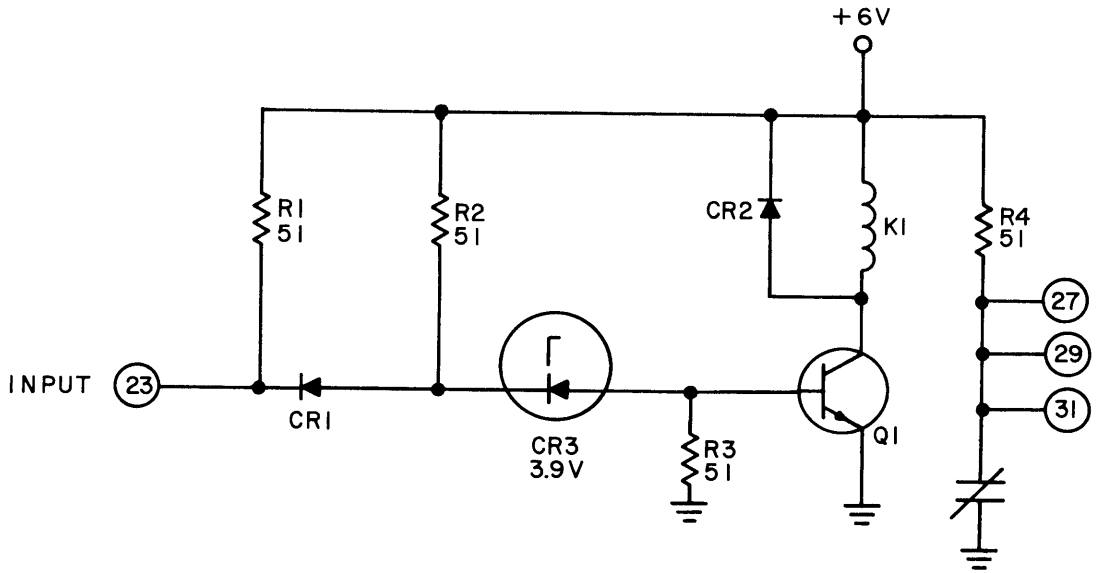
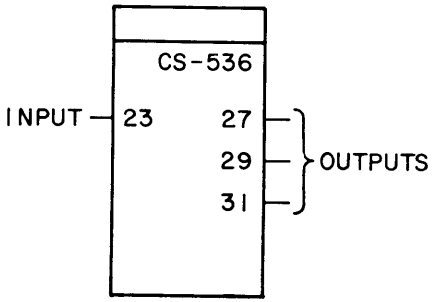


Figure 1. System Normalizer PAC, Model CS-536, Parts Locations

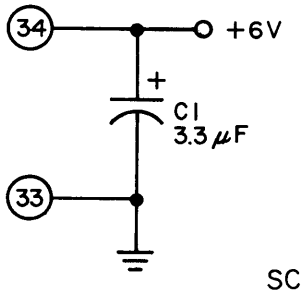
ELECTRICAL PARTS LIST

Reference Designation	Description	CCD Part No.
C1	CAPACITOR: 3.3 μF ±20%, 10V	70 930 230 011
CR1, CR2	DIODE, SILICON	70 943 083 002
CR3	DIODE, ZENER, 1N748A	70 943 110 003
K1	RELAY, REED FORM – B	70 963 034 004
Q1	TRANSISTOR: NPN	70 943 754 002
R1-R4	RESISTOR, FIXED, FILM: 51 ohms ±5%, 1W	70 932 005 018





LOGIC SYMBOL



SCHEMATIC

6576

Figure 2. System Normalizer PAC, Model CS-536, Schematic Diagram and Logic Symbol

LINE RECEIVER ASSEMBLY PAC, MODEL CS-548

The Line Receiver Assembly PAC, Model CS-548 (Figure 1), provides 14 gated outputs used to receive signals from an I/O bus.

Circuit Function

Signals are received on an I/O bus on pins 2, 6, 12, 16, 20, 26, 30, 31, 17, 21, 25, 11, 3, and 7. The Circuit has a built-in terminator for each signal. Pins 8, 22, 27, and 13 provide points for gating off-strobe signals.

Specifications

Input Loading

1 unit load on each input pin

Output Drive Capacity

8 units loads on pins 4, 10, 14, 18, 24, 28, 32, 29, 15, 19, 23, 9, 1, and 5

Circuit Delay

75 ns (at 1.5V average over two stages)

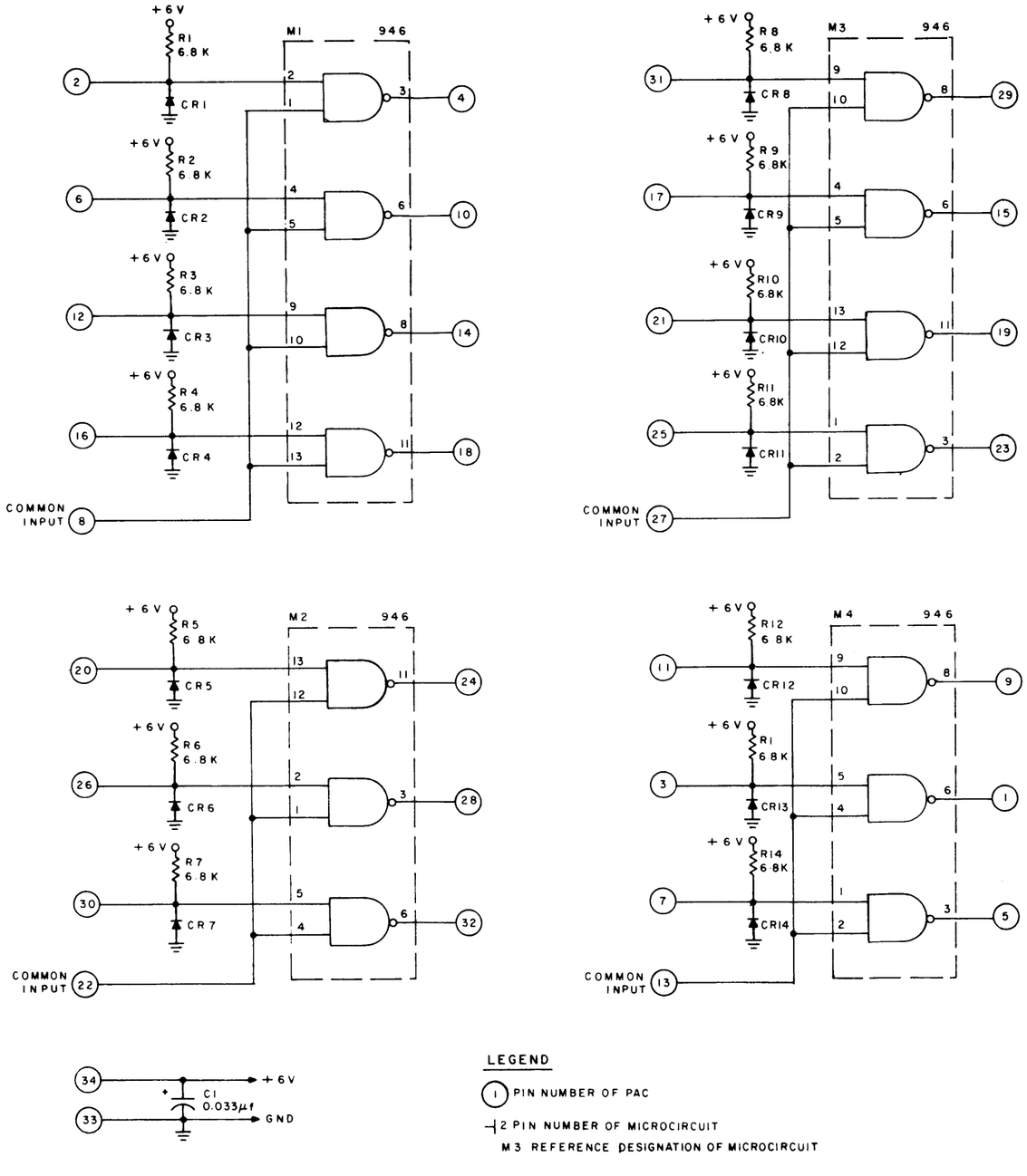
Current Requirements

+6V: 75 mA (max)

ELECTRICAL PARTS LIST

Reference Designation	Description	CCD Part No.
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μF $\pm$20%, 50V	70 930 313 016
R1-R14	RESISTOR, FIXED, FILM: 6.8K $\pm$2%, ¼W	70 932 114 069
CR1-CR14	DIODE, SILICON	70 943 083 002
M1-M4	MICROCIRCUIT: Type 946, quad input NAND gate integrated circuit	70 950 105 002

SCHEMATIC



LOGIC SYMBOL

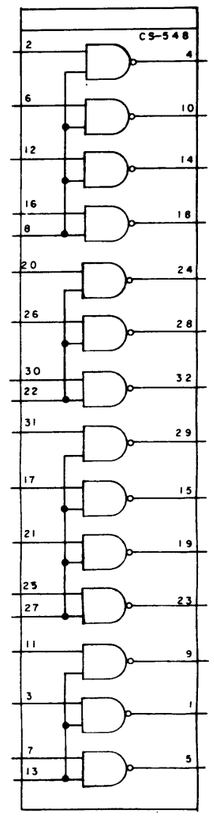


Figure 1. Line Receiver Assembly PAC, Model CS-548, Schematic Diagram and Logic Symbol

The +6V and -6V supplies are adjusted by monitoring the output voltage with a meter while turning the potentiometer. The 15 Vdc adjustment should be made with a 4.7 kilohm (±2%) resistor placed across the RT terminals. This resistor compensates for the thermistor. The output voltage should be set at 14.8 Vdc. The line sensing circuit is adjusted such that the FLT signal is 0V when the input line is at 95V or less and +6V when the input line is 100V or more.

The supply has six internal adjustments, which are factory set and normally do not need attention. Potentiometers R3, R30, and R45 control the +15V, +6V, and -6V overcurrent detectors, respectively. They are adjusted such that if the rated current is exceeded, the output voltage will decrease. Potentiometer R22 controls the +15V overvoltage detector. It is adjusted to crowbar the +15V supply when voltage exceeds +16 Vdc. Potentiometers R64 and R70 control the +6V and -6V undervoltage detectors, respectively, and are adjusted to crowbar the +15V supply when the absolute value of either voltage is 5V or less.

THEORY OF OPERATION

General Description

This power supply converts input ac power into three regulated outputs. A block diagram of the power supply is shown in Figure B-2.

Input ac power is supplied to a transformer in the input power converter. Secondaries of this transformer are rectified and filtered to provide bulk dc power for the three series regulators. These regulators provide the required dc outputs. Logic circuitry provides the required sequencing and line sensing. Overcurrent protection is included in the series regulators. Reverse diodes across each output prevent accidental reversal of polarity. Overvoltage crowbar circuits are provided for all outputs. See Figure B-3 for a detailed schematic of the power supply.

Input Power Converter

Input ac power is supplied to the primary of transformer T1 through plug P1. Thermostat S2 turns off the supply if unsafe temperatures are reached. The secondaries of T1 are rectified and filtered to provide bulk dc power and drive to the regulators.

Reference Voltages

The reference source supplies power required by the +15V turn-on delay circuit, the ±15V overvoltage circuit, and the ±6V and +15V regulators. The rectified voltage provided by CR22 and CR23 is filtered by R60 and C16. The voltage across C16 provides power to zener diode CR24, which provides the reference voltage.

+15V Series Regulator and Sequencing Circuit

Transistors Q25, Q26, and Q31 are the series pass transistors for the +15V supply. They are driven by Q3 and surrounding circuitry. Transistors Q4, Q5, and surrounding circuitry withhold base current from Q3 when either the +6V or -6V supply is below 5V.

Whenever Q5 is turned off, however, Q4 is also turned off. This removes the drive current for the +15V series regulator, which turns it off. It also turns Q6 off, which causes CR3 to conduct. This fires the crowbar SCR in the +15V overvoltage circuit, which shuts down the 15V output. (During initial turn-on of the supply, this circuit attempts to fire the crowbar SCR, which would prevent turn-on. However, since no output voltage is then present, the crowbar SCR cannot turn on.)

Series Regulator Operation

The output voltage appears across a voltage divider consisting of R17, R18, R19, R20, and an external temperature programming resistor. The wiper voltage of R19 is compared with the end reference at the emitter of Q2. R16 and CR5 provide temperature compensation. Q2 controls the series regulator by shunting a portion of the base drive current for Q3 (provided by R9) away from Q3. (It is assumed that the turn-on control circuitry has already indicated turn-on for this discussion.) Q3, in turn, controls the conductivity of Q26 and the pass transistors, Q25 and Q31, which provide the load current.

Current limiting is provided by the circuit consisting of R99, R3, R4, and Q1. The current level is sensed by R99. The voltage across R99 is compared with the fixed voltage across R3 by transistor Q1. Whenever the maximum allowed current is reached, the voltage across R99 exceeds the voltage across R3. This turns Q1 on, which shunts away a portion of the base drive current for Q3, thus reducing the load current.

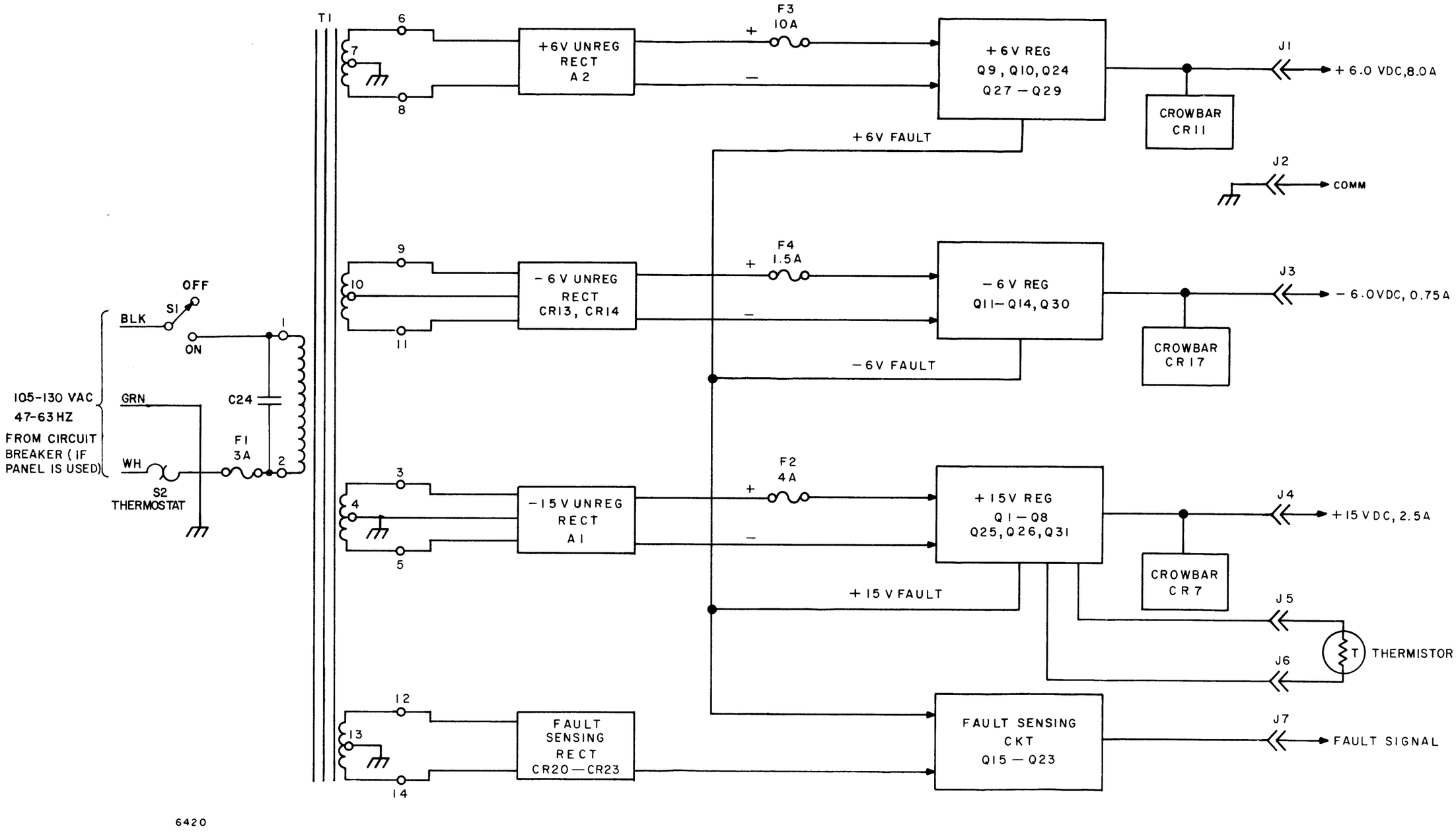
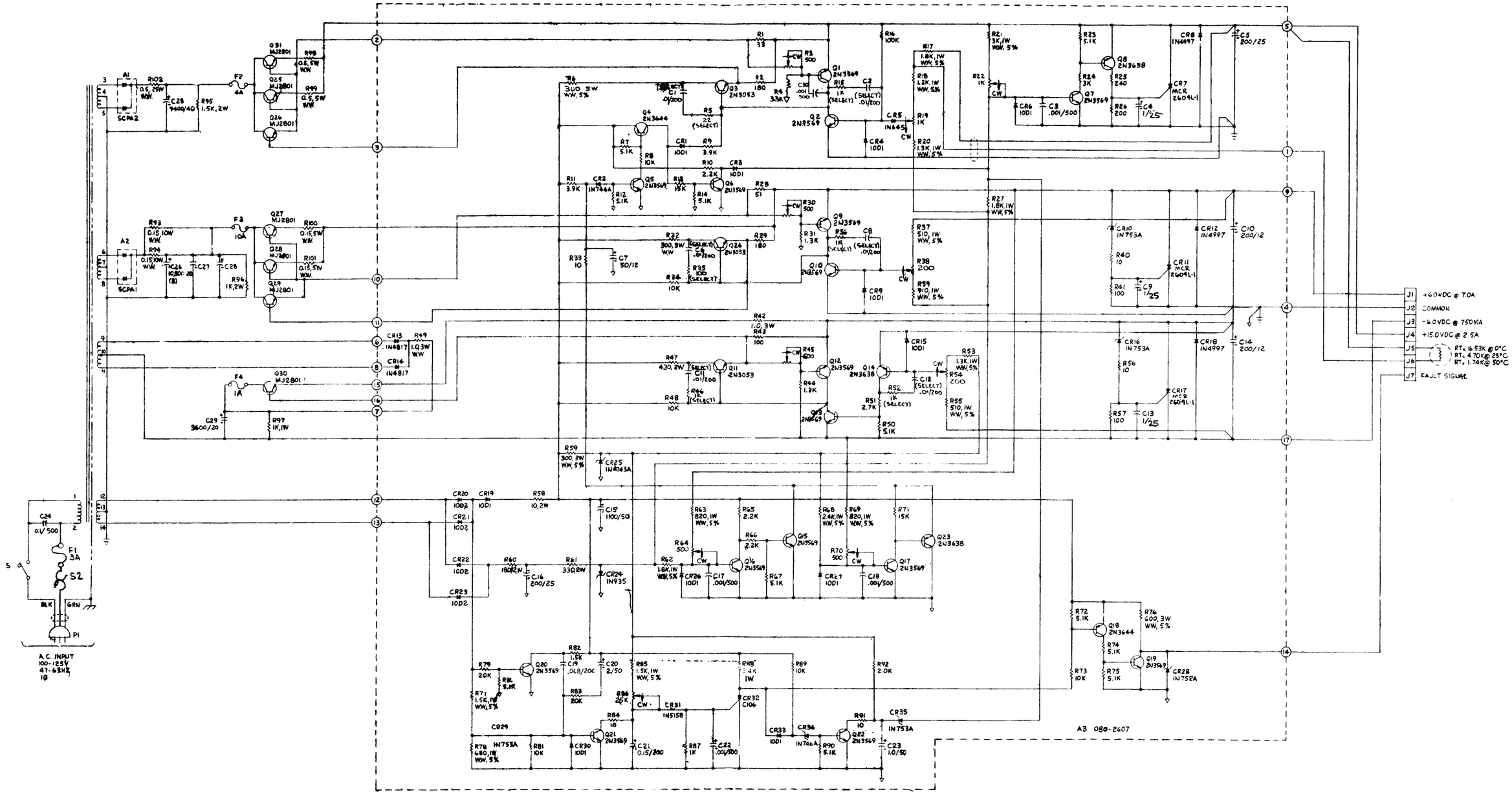


Figure B-2. Simplified Block Diagram of PB421 Power Supply



1 – ALL RESISTANCES ARE 1/2W IN OHMS & ALL CAPACITANCES ARE IN UF UNLESS OTHERWISE SPECIFIED.

Figure B-3. Schematic Diagram of PB421 Power Supply

+15V Turn-On Delay Circuit

The +15V turn-on delay circuit ensures that the +15V output is not allowed to turn on until the ±6V output voltages have both reached 83% of nominal.

The +6V output determines the current through resistors R63 and R64. This current is compared with the current through R62, which is determined by the -9V reference voltage. Whenever the +6V output reaches its minimum allowed level, the current through R63 and R64 exceeds the current through R62, which turns Q16 on. This clamps Q15 off, which allows zener diode CR2 to conduct.

Similarly, the -6V output determines the current through R69 and R70. This current is compared with the current through R68, which is determined by the +13V reference voltage. Whenever the -6V output reaches its minimum allowed level, the current through R69 and R70 exceeds the current through R68, which turns Q17 off. This turns Q23 off, which allows zener diode CR2 to conduct.

Whenever both the +6V and -6V outputs are above their minimum allowed levels, Q15 and Q23 are both off, and zener diode CR2 conducts. This provides a turn-on signal for the +15V regulator. However, if either the +6V or the -6V output is below its minimum allowed level, CR2 does not conduct. This removes the turn-on signal for the +15V regulator, which turns off the regulator and crowbars the +15V output. Capacitor C7 provides a delay which prevents ripple on ±6V from causing a false detection.

+15V Overvoltage Circuit

The +15V overvoltage circuit crowbars the +15V output via SCR CR7 whenever the +15V output exceeds its maximum allowed level or whenever a shutdown signal is received from the +15V regulator or the line sense circuit.

The +15V output determines the current through R21 and R22. This current is compared with the current through R27, which is determined by the -9V reference voltage. Whenever the +15V output exceeds its maximum allowed level, the current through R21 and R22 exceeds the current through R27. This turns Q7 on, which turns Q8 on. This fires crowbar SCR CR7, which clamps the +15V output voltage to a low level.

This circuit is also activated in the same manner whenever the +15V regulator or the line sense circuit provides a positive signal at the base of Q7.

+6V Series Regulator

The +6V output voltage is regulated by the series regulator, which controls the load current through pass transistors Q27 and Q28. They are controlled by Q9, which is in turn controlled by Q24.

The output voltage is sensed by a voltage divider consisting of R37, R38, and R39. The wiper voltage of R38 is compared with ground at the emitter of Q10. Q10 shunts away a portion of the base drive current for Q24 (supplied by R34) as required to regulate the +6V output voltage.

Overcurrent protection is provided by R101, R100, R30, R31, and Q9. R100 senses the load current. The voltage across R100 is compared with the fixed voltage across R30. As the load current tries to exceed the maximum allowed level, Q9 begins to conduct. This shunts away a portion of the base drive current of Q24, which reduces the load current.

-6V Series Regulator

The -6V output voltage is regulated by the series regulator, which controls the load current through pass transistor Q30, which is in turn controlled by Q11.

The output voltage is sensed by a voltage divider consisting of R53, R54, and R55. The wiper voltage of R54 is compared with ground at the emitter of Q14. Q14 shunts away a portion of the base drive current for Q11 (supplied by R48) as required to regulate the -6V output voltage.

Overcurrent protection is provided by R42, R45, R44, and Q12. R42 senses the load current. The voltage across R42 is compared with the fixed voltage across R45. As the load current tries to exceed the maximum allowed level, Q12 begins to conduct. This shunts away a portion of the base drive current of Q11, which reduces the load current.

+6V and -6V Overvoltage Circuitry

Overvoltage crowbar circuits are provided across each output. When the +6V output voltage exceeds the maximum allowed level, zener diode CR10

conducts. This fires SCR CR11, which shorts the +6V output to common until input ac power is removed. When the -6V output voltage exceeds the maximum allowed level, zener diode CR16 conducts. This fires SCR CR17, which shorts the -6V output to common until input ac power is removed.

Reverse Diodes

Diodes CR8, CR12, and CR18 are provided across the +15V, +6V, and -6V outputs, respectively, to prevent an output voltage reversal greater than 2V in the event of a component failure.

Line Sense Circuit

The line sense circuit initiates turn-off of the power supply if input ac power is lost.

Input ac power is sensed by the secondary of transformer T1. This secondary voltage is full-wave rectified by CR20 and CR21 to provide an unfiltered dc voltage across R77 and R78. R77 and R78 are chosen so that when input ac voltage reaches a predetermined peak, CR29 conducts, which turns Q21 on until the ac voltage drops below this level again.

At the beginning of each half-cycle, C21 begins to charge at a rate determined by C21, R85, R86, and the fixed reference voltage across zener diode CR25. Whenever C21 charges to a predetermined level, CR31 conducts, which fires SCR CR32. The charge rate is adjusted by R86 so that if input ac power is at low line or above, Q21 will be turned on (because of the line sense voltage) before C21 has charged to the level which causes CR31 to conduct. Transistor Q20 is held on by the full-wave rectified voltage at all times except for a short period as the input ac voltage passes through 0V. At this time, Q20 turns on, which discharges C21 to reset the line sense circuit.

Under normal ac input power conditions, Q21 clamps the gate of CR32 before it is fired. However, if ac power fails to reach low line for one half-cycle, CR32 is fired. This does the following:

1. Coupling resistor R73 turns Q18 on. This turns on Q19, causing the fault signal to drop to ground.

2. Coupling diode CR33 conducts, which shunts the current through R89 away from zener diode CR34. This turns CR34 off, which turns Q22 off. After a short delay, C23 charges sufficiently to cause zener diode CR35 to conduct. This fires crowbar SCR CR7 in the +15V overvoltage circuit.

In summary, whenever the input ac voltage fails to reach low line for a half cycle, the fault signal appears, and after a short delay, the +15V output is crowbarred.

TROUBLESHOOTING PROCEDURE

In the event of a malfunction, the supply should be visibly examined for broken, loose, or damaged parts or wire and for other foreign objects. Apparent power supply failures may be caused by improperly adjusted potentiometers. This should be kept in mind when troubleshooting the power supply per Table B-1.

TABLE B-1.
TROUBLESHOOTING GUIDE

Symptom	Possible Cause	Suggested Action
1. Power supply will not turn on (no dc outputs)	a. No input ac power	a. Check for input power
	b. Open input power switch S1	b. Check switch position
	c. Open thermostat S2	c. Check for proper cooling
	d. Blown fuse F1	d. Check fuse
2. No output on any output	a. Overvoltage circuit crowbarred	a. Check for faulty pass transistor, improper voltage adjustment, or faulty SCR
	b. Blown fuse	b. Check for blown fuse
	c. Shorted output	c. Check with no load applied
3. Low output voltage on any output	a. Improper adjustment	a. Check adjustment
	b. Overloaded output	b. Check with no load applied
4. Overvoltage occurs on any output	a. Shorted pass transistor	a. Check voltage adjustment

SECTION 2
ILLUSTRATED PARTS BREAKDOWN

This section contains the Illustrated Parts Breakdown (IPB) of the power supply for all models of the H112 Digital Controller.

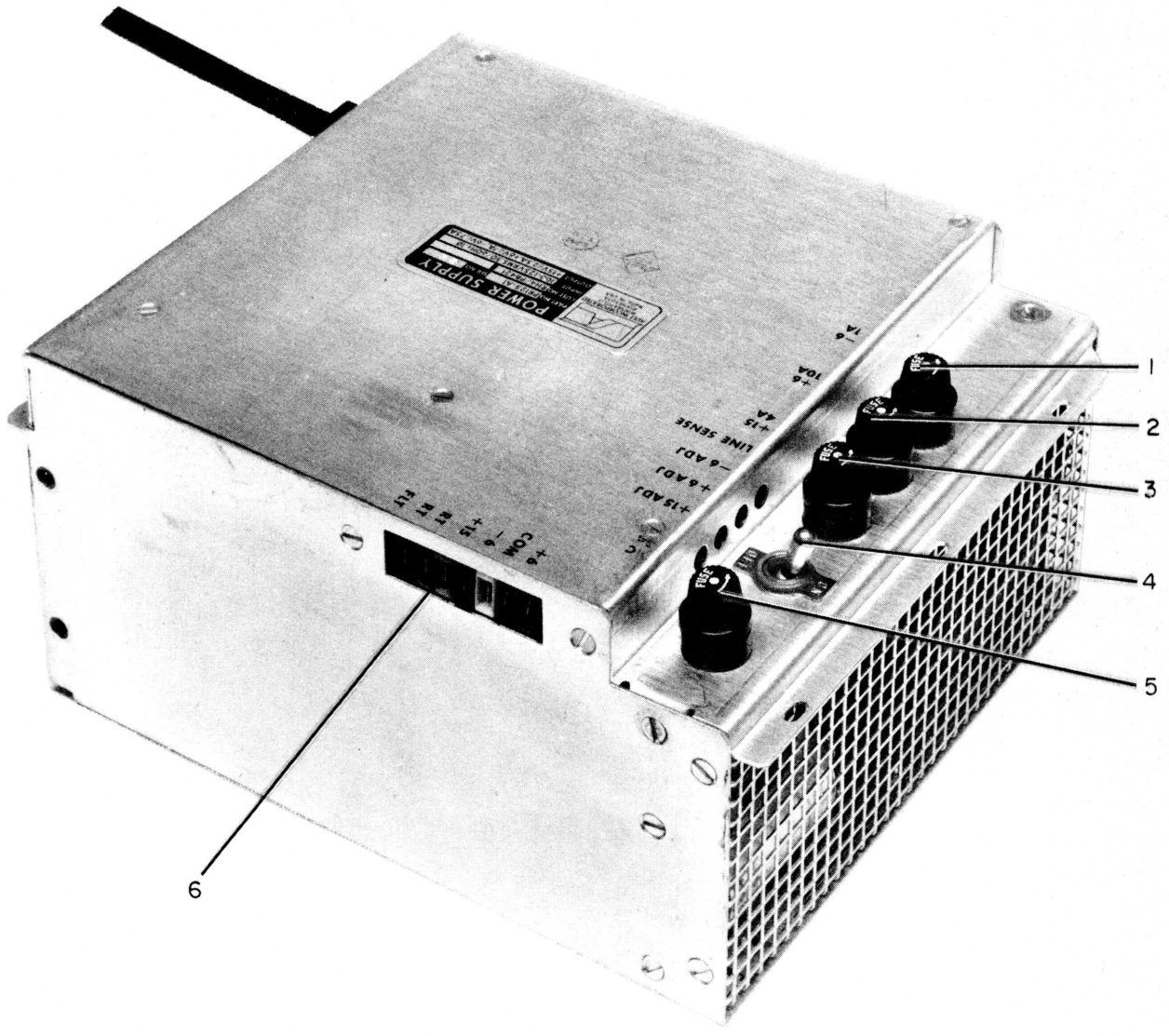


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Figure B-4. H112 Power Supply (Part 1 of 2)

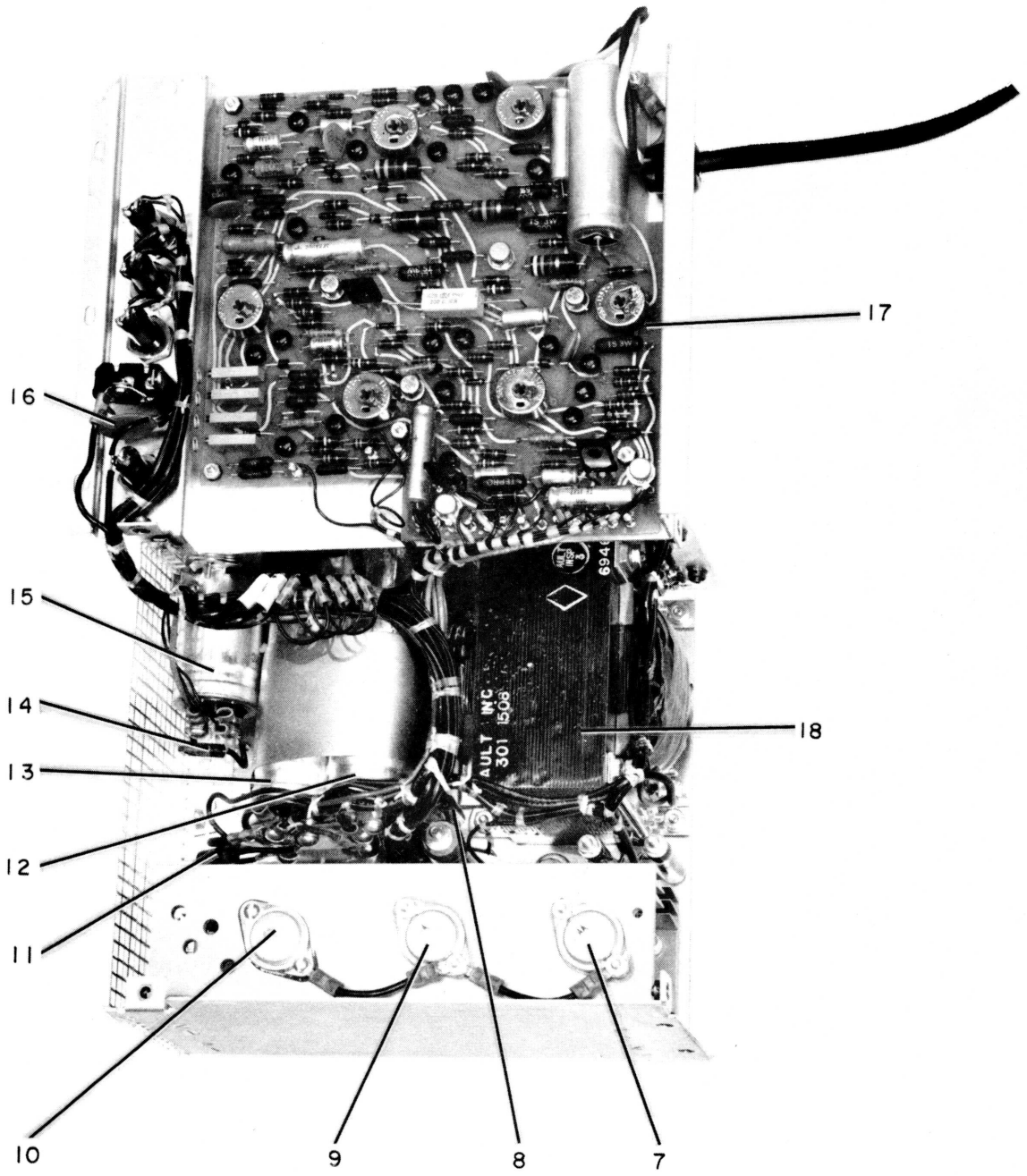

Figure B-4. H112 Power Supply (Part 2 of 2)

Fig. & Index No.	Designation	AULT Part No.	Indenture	Description	Qty. per Assy.
B-4-	DEF1 through DEF3	70950064001*	A	POWER SUPPLY: Ault, Inc., Part No. PR125-A1-2 (Refer to Figure 7-1-4)	A/R
-1	F4	6221084	B	FUSE, CARTRIDGE - 1A	1
-2	F3	6221088	B	FUSE, CARTRIDGE - 10A	1
-3	F2	6221097	B	FUSE, CARTRIDGE -4A	1
-4	S1	6261031	B	SWITCH, TOGGLE, SPST	1
-5	F1	6221082	B	FUSE, CARTRIDGE - 3A	1
-6	J1-J7		B	CONNECTOR, RECEPTACLE - c/o 7 Contacts, Heyco Type	1
-7	Q31	6011133	B	TRANSISTOR, Type MJ2801	7
-8	R95	5003097	B	RESISTOR, FIXED, COMPOSITION - 1.5K ohms, 10W, 5%	1
-9	Q25	6011133	B	Same as Q31	Ref
-10	Q26	6011133	B	Same as Q31	Ref
-11	R96	5003088	B	RESISTOR, FIXED, COMPOSITION - 1K ohm, 2W, 5%	1
-12	C27	4001416	B	CAPACITOR, ELECTROLYTIC - 10,800 μF, 20V	3
-13	C26	4001416	B	Same as C27	Ref
	C28 (Not shown)	4001416	B	Same as C27	Ref
-14	R97	5002088	B	RESISTOR, FIXED, COMPOSITION - 1K ohm, 1W, 5%	1
-15	C29	4001248	B	CAPACITOR, ELECTROLYTIC - 3600 μF, 20V	1
-16	C24	4061239	B	CAPACITOR - 0.01 μF, 500V	5
-17	A3	0802607	B	CIRCUIT CARD ASSEMBLY (see Figure B-5 for breakdown)	1
-18	T1	3011508	B	TRANSFORMER, POWER	1
	(The following are not shown)				
	A1	6661098-2	B	RECTIFIER ASSEMBLY	1
	A2	6061098-1	B	RECTIFIER ASSEMBLY	1
	C25	4001415	B	CAPACITOR - 9400 μF, 40V	1
	Q27	6011133	B	Same as Q31	Ref
	Q28	6011133	B	Same as Q31	Ref
	Q29	6011133	B	Same as Q31	Ref
	Q30	6011133	B	Same as Q31	Ref
	R93	5805361	B	RESISTOR, FIXED, WIREWOUND - 0.15 ohm, 10W, 5%	2
	R94	5805361	B	Same as R93	Ref
	R98	5804480-5	B	RESISTOR, FIXED, WIREWOUND - 0.50 ohm, 5W, 5%	2

* CCD part number.

Fig. & Index No.	Designation	AULT Part No.	Indenture	Description	Qty. per Assy.
B-4-	R99	5804480-5	B	Same as R98	Ref
	R100	5804480-3	B	RESISTOR, FIXED, WIREWOUND - 0.15 ohm, 5W, 5%	2
	R101	5804480-3	B	Same as R100	Ref
	R102	5806550-5	B	RESISTOR, FIXED, WIREWOUND - 0.5 ohm, 25W, 5%	1
	S2	Unavailable	B	THERMOSTAT	1

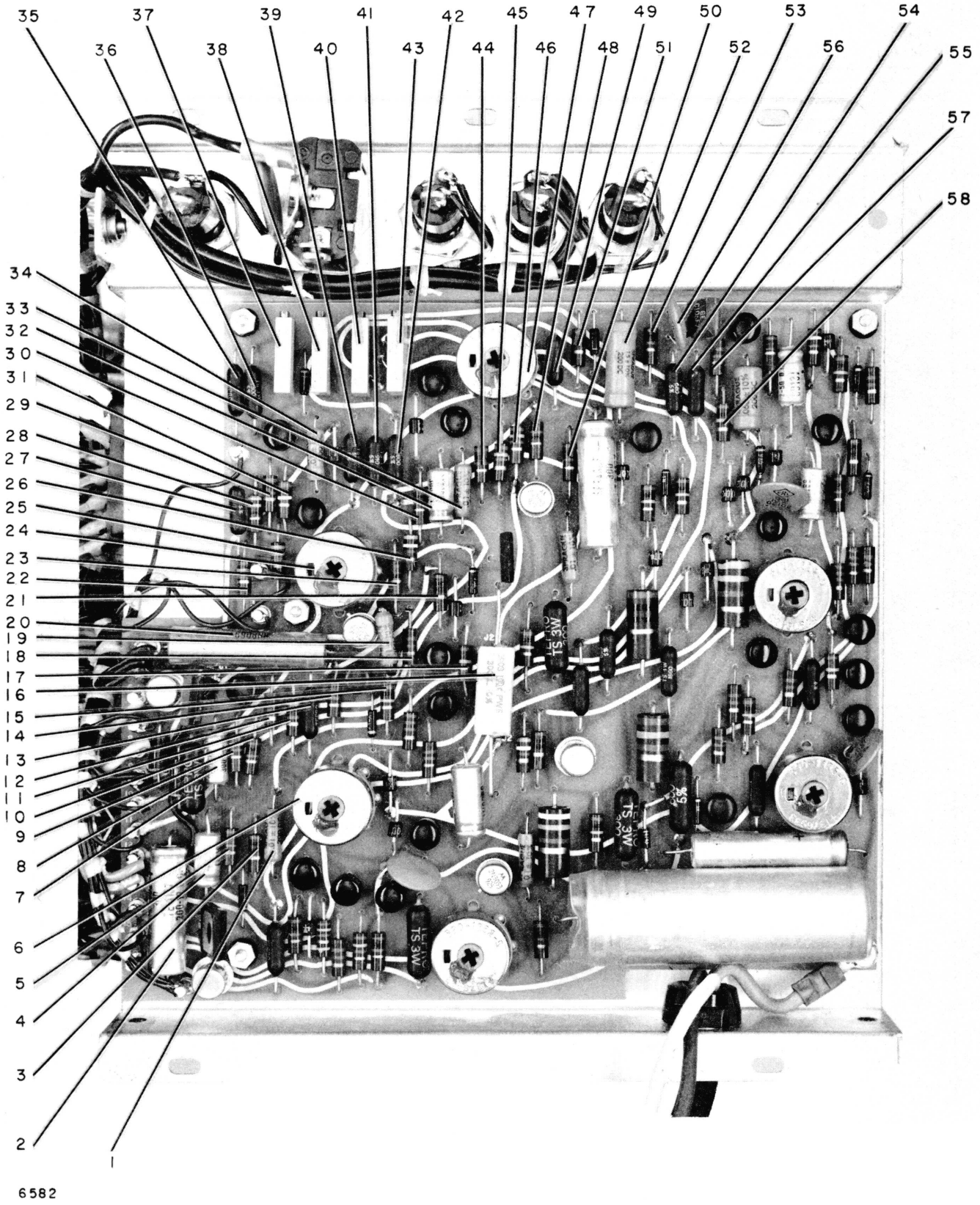

Figure B-5. Circuit Card Assembly (Part 1 of 3)

Fig. & Index No.	Designation	AULT Part No.	Indenture	Description	Qty. per Assy.
B-5-	A3	0802607	B	CIRCUIT CARD ASSEMBLY (Refer to Figure B-4-17 for next higher assembly)	Ref
-1	C12	4061133	C	CAPACITOR, SELECTED - 0.01 μF, 200V	5
-2	C14	4061100-3	C	CAPACITOR - 200 μF, 12V	2
-3	R56	5001040	C	RESISTOR, FIXED, COMPOSITION - 10 ohms, 1/2W, 5%	5
-4	C13	4001096	C	CAPACITOR - 1.0 μF, 25V	3
-5	R57	5001064	C	RESISTOR, FIXED, COMPOSITION - 100 ohms, 1/2W, 5%	3
-6	R22	5901351-4	C	RESISTOR, VARIABLE - 1K ohm	2
-7	R49	5802550-7	C	RESISTOR, FIXED, WIREWOUND - 1.0 ohm, 3W, 5%	2
-8	C4	4001096	C	Same as C13	Ref
-9	R25	5001073	C	RESISTOR, FIXED, COMPOSITION - 240 ohms, 1/2W, 5%	1
-10	R26	5001071	C	RESISTOR, FIXED, COMPOSITION - 200 ohms, 1/2W, 5%	1
-11	R24	5001099	C	RESISTOR, FIXED, COMPOSITION - 3K ohms, 1/2W, 5%	1
-12	R23	5001105	C	RESISTOR, FIXED, COMPOSITION - 5.1K ohms, 1/2W, 5%	11
-13	R21	5801207-108	C	RESISTOR, FIXED, WIREWOUND - 3K ohms, 1W, 5%	1
-14	R12	5001105	C	Same as R23	Ref
-15	R8	5001112	C	RESISTOR, FIXED, COMPOSITION - 10K ohms, 1/2W, 5%	6
-16	R6	5804480-25	C	RESISTOR, FIXED, WIREWOUND - 300 ohms, 5W, 5%	1
-17	R13	5001116	C	RESISTOR, FIXED, COMPOSITION - 15K ohms, 1/2W, 5%	2
-18	R7	5001105	C	Same as R23	Ref
-19	C1	4061133	C	Same as C12	Ref
-20	C5	4001098	C	CAPACITOR - 200 μF, 25V	2
-21	R40	5001040	C	Same as R56	Ref
-22	R2	5001070	C	RESISTOR, FIXED, COMPOSITION - 180 ohms, 1/2W, 5%	3
-23	R5	500XXXX	C	RESISTOR, FIXED, COMPOSITION, SELECTED - 1/2W, 5%	6
-24	R3	5901352-5	C	RESISTOR, VARIABLE - 500 ohms	5

Fig. & Index No.	Designation	AULT Part No.	Indenture	Description	Qty. per Assy.
B-5-25	R4	5001100	C	RESISTOR, FIXED, COMPOSITION - 3.3K ohms, 1/2W, 5%	1
-26	R9	5001102	C	RESISTOR, FIXED, COMPOSITION - 3.9K ohms, 1/2W, 5%	2
-27	R17	5801207-103	C	RESISTOR, FIXED, WIREWOUND - 1.8K ohms, 1W, 5%	3
-28	R1	5001052	C	RESISTOR, FIXED, COMPOSITION - 33 ohms, 1/2W, 5%	1
-29	R15	500XXXX	C	Same as R5	Ref
	C30 (Not shown)	Unavailable	C	CAPACITOR - 0.001 μF, 500V	1
-30	R41	5001064	C	Same as R57	Ref
-31	R16	5001136	C	RESISTOR, FIXED, COMPOSITION - 100K ohms, 1/2W, 5%	1
-32	C9	4001096	C	Same as C13	Ref
-33	C8	4061133	C	Same as C12	Ref
-34	C2	4061239	C	Same as C24	Ref
-35	R18	5801207-99	C	RESISTOR, FIXED, WIREWOUND - 1.2K ohms, 1W, 5%	1
-36	R20	5801207-100	C	RESISTOR, FIXED, WIREWOUND - 1.3K ohms, 1W, 5%	2
-37	R19	5901351-4	C	Same as R22	Ref
-38	R38	Unavailable	C	RESISTOR, VARIABLE - 200 ohms	2
-39	R37	5801207-90	C	RESISTOR, FIXED, WIREWOUND - 510 ohms, 1W, 5%	2
-40	R54	Unavailable	C	Same as R38	Ref
-41	R39	5801207-96	C	RESISTOR, FIXED, WIREWOUND - 910 ohms, 1W, 5%	1
-42	R27	5801207-103	C	Same as R17	Ref
-43	R86	5901351-9	C	RESISTOR, VARIABLE - 25K ohms	1
-44	R36	500XXXX	C	Same as R5	Ref
-45	R31	5001091	C	RESISTOR, FIXED, COMPOSITION - 1.3K ohms, 1/2W, 5%	2
-46	R29	5001070	C	Same as R2	Ref
-47	R30	5901352-5	C	Same as R3	Ref
-48	R28	5001057	C	RESISTOR, FIXED, COMPOSITION - 51 ohms, 1/2W, 5%	1
-49	R85	5801207-101	C	RESISTOR, FIXED, WIREWOUND - 1.5K ohms, 1W, 5%	2
-50	R35	500XXXX	C	Same as R5	Ref
-51	R84	5001040	C	Same as R56	Ref
-52	C21	4001148	C	CAPACITOR - 0.15 μF, 200V	1

Fig. & Index No.	Designation	AULT Part No.	Indenture	Description	Qty. per Assy.
B-5-53	R87	5001088	C	RESISTOR, FIXED, WIREWOUND - 1K ohm, 1/2W, 5%	1
-54	R78	5801207-93	C	RESISTOR, FIXED, WIREWOUND - 680 ohms, 1W, 5%	1
-55	R77	5801207-101	C	Same as R85	Ref
-56	C22	4061239	C	Same as C24	Ref
-57	R80	5001105	C	Same as R23	Ref
-58	R79	5001119	C	RESISTOR, FIXED, COMPOSITION - 20K ohms, 1/2W, 5%	2

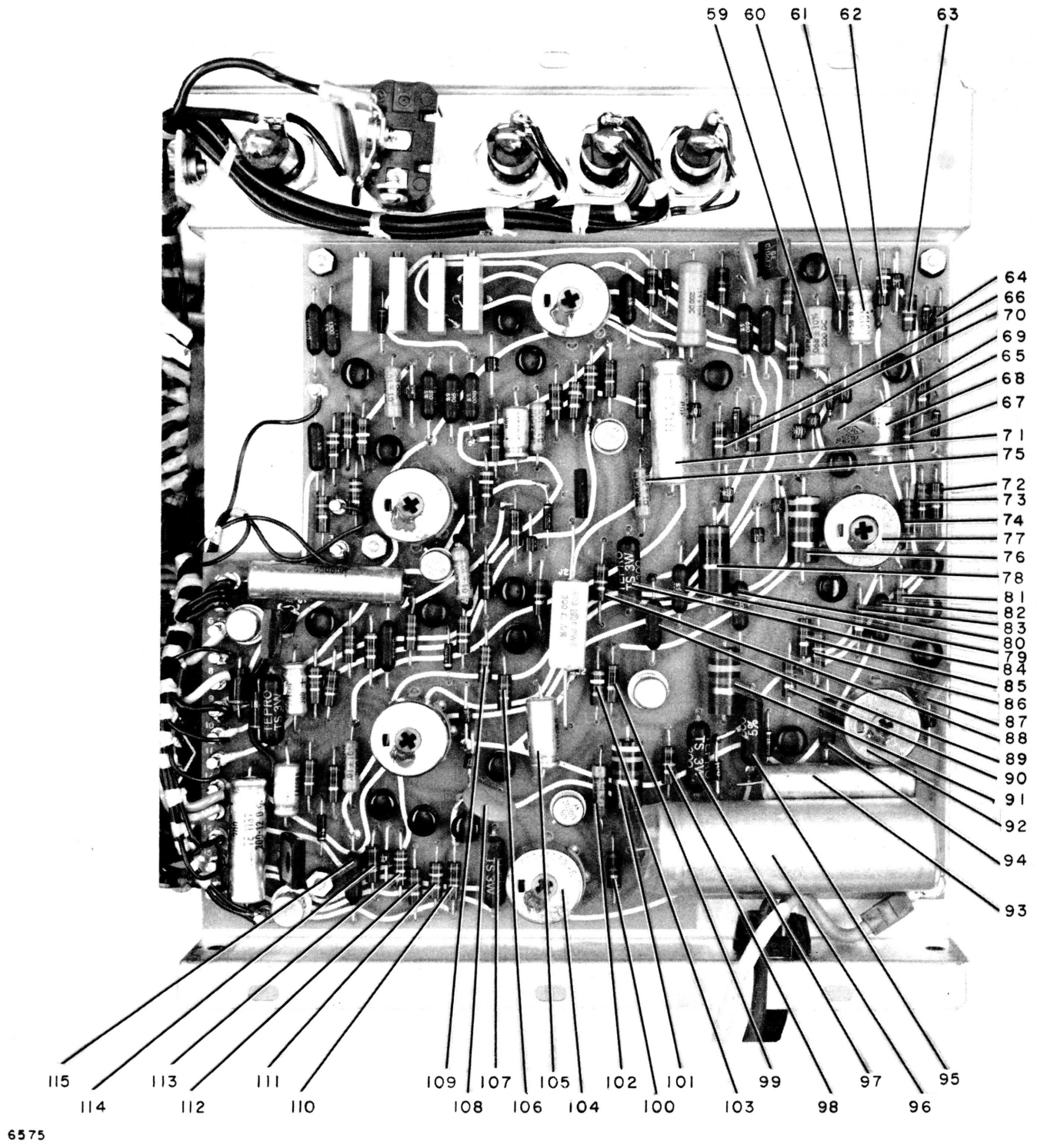

Figure B-5. Circuit Card Assembly (Part 2 of 3)

Fig. & Index No.	Designation	AULT Part No.	Indenture	Description	Qty. per Assy.
B-5 -59	C19	4061142	C	CAPACITOR - 0.068 μF, 200V	1
-60	R82	5001092	C	RESISTOR, FIXED, COMPOSITION - 1.5K ohm, 1/2W, 5%	1
-61	C20	4001069	C	CAPACITOR - 2 μF, 50V	1
-62	R88	5001097	C	RESISTOR, FIXED, COMPOSITION - 2.4K ohms, 1/2W, 5%	1
-63	R89	5001112	C	Same as R8	Ref
-64	R90	5001105	C	Same as R23	Ref
-65	R91	5001040	C	Same as R56	Ref
-66	R83	5001119	C	Same as R79	Ref
-67	R92	5001095	C	RESISTOR, FIXED, COMPOSITION - 2K ohms, 1/2W, 5%	
-68	C23	4001008	C	CAPACITOR - 1.0 μF, 50V	1
-69	C17	4061239	C	Same as C24	Ref
-70	R81	5001112	C	Same as R8	Ref
-71	C10	4001100-3	C	Same as C14	Ref
-72	R67	5001105	C	Same as R23	Ref
-73	R66	5001096	C	RESISTOR, FIXED, COMPOSITION - 2.2K ohm, 1/2W, 5%	3
-74	R65	5001096	C	Same as R66	Ref
-75	C6	4061133	C	Same as C12	Ref
-76	R61	5003076	C	RESISTOR, FIXED, COMPOSITION - 330 ohms, 2W, 5%	1
-77	R64	5901352-5	C	Same as R3	Ref
-78	R58	5003040	C	RESISTOR, FIXED, COMPOSITION - 10 ohms, 2W, 5%	1
-79	R63	5801207-95	C	RESISTOR, FIXED, WIREWOUND - 820 ohms, 1W, 5%	2
-80	R62	5801207-103	C	Same as R17	Ref
-81	R71	5001116	C	Same as R13	Ref
-82	R68	5801207-106	C	RESISTOR, FIXED, WIREWOUND - 2.4K ohms, 1W, 5%	1
-83	R72	5001105	C	Same as R23	Ref
-84	R32	5802550-25	C	RESISTOR, FIXED, WIREWOUND - 300 ohms, 3W, 5%	2
-85	R74	5001105	C	Same as R23	Ref
-86	R73	5001112	C	Same as R8	Ref
-87	C18	4061239	C	Same as C24	Ref
-88	R34	5001112	C	Same as R8	Ref
-89	R53	5801207-100	C	Same as R20	Ref
-90	R75	5001105	C	Same as R23	Ref

Fig. & Index No.	Designation	AULT Part No.	Indenture	Description	Qty. per Assy.
B-5					
-91	R60	5001070	C	Same as R2	Ref
-92	R70	5901352-5	C	Same as R3	Ref
-93	C16	4001098	C	Same as C5	Ref
-94	R69	5801207-95	C	Same as R63	Ref
-95	R76	5802550-29	C	RESISTOR, FIXED, WIREWOUND - 600 ohms, 3W, 5%	1
-96	C15	4001501	C	CAPACITOR - 1100 μF, 50V	1
-97	R59	5802550-25	C	Same as R32	Ref
-98	R48	5001112	C	Same as R8	Ref
-99	R33	5001040	C	Same as R56	Ref
-100	R46	500XXXX	C	Same as R5	Ref
-101	R47	5003079	C	RESISTOR, FIXED, COMPOSITION - 430 ohms, 2W, 5%	1
-102	C11	4061133	C	Same as C12	Ref
-103	R11	5001102	C	Same as R9	Ref
-104	R45	5901352-5	C	Same as R3	Ref
-105	C7	4001100-6	C	CAPACITOR - 50 μF, 12V	1
-106	R14	5001105	C	Same as R23	Ref
-107	R42	5802550-7	C	Same as R49	Ref
-108	C3	4001239	C	Same as C24	Ref
-109	R10	5001096	C	Same as R66	Ref
-110	R43	5001064	C	Same as R57	Ref
-111	R44	5001091	C	Same as R31	Ref
-112	R50	5001105	C	Same as R23	Ref
-113	R51	5001098	C	RESISTOR, FIXED, COMPOSITION - 2.7K ohms, 1/2W, 5%	1
-114	R52	500XXXX	C	Same as R5	Ref
-115	R55	5801207-90	C	Same as R37	Ref

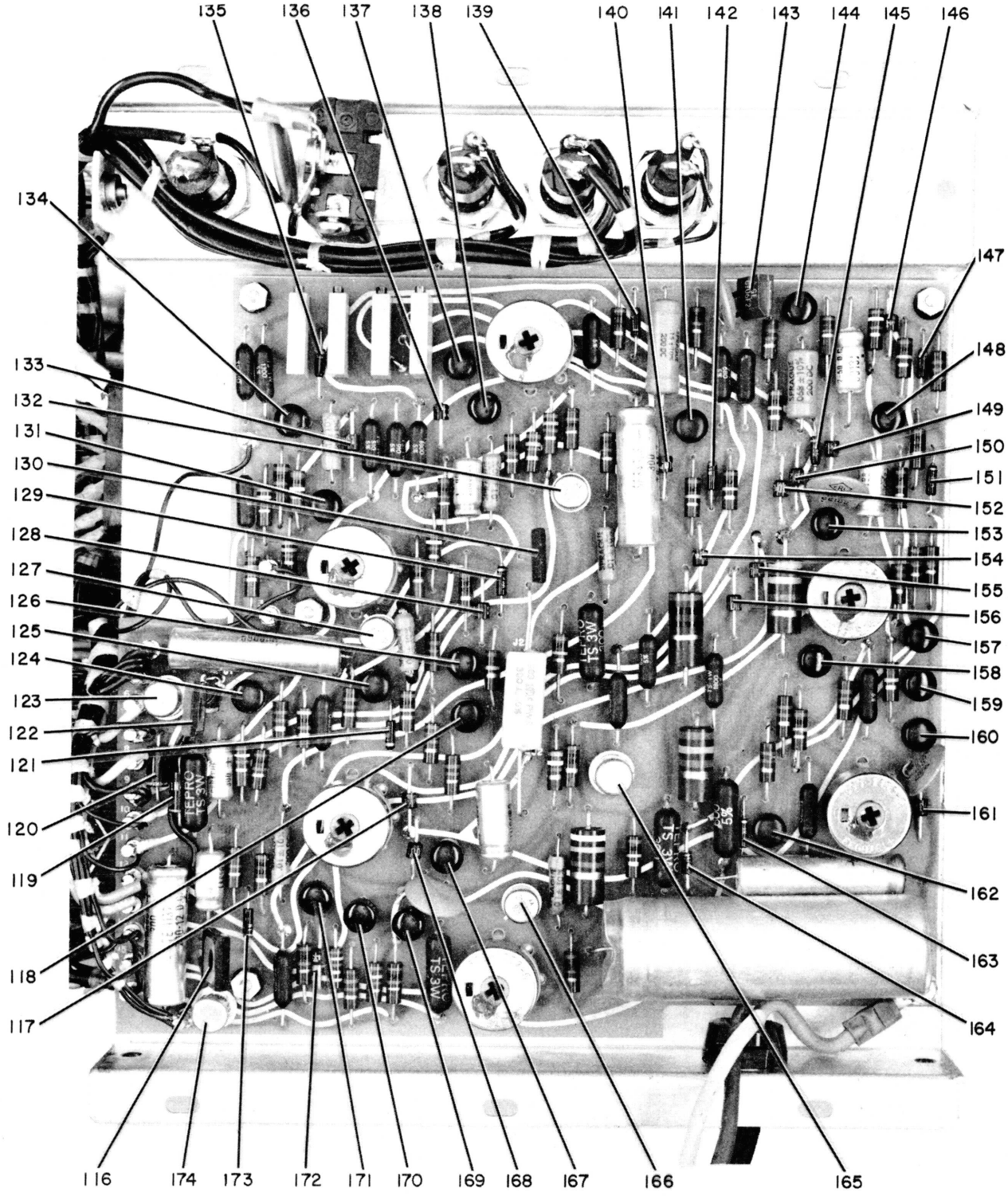

Figure B-5. Circuit Card Assembly (Part 3 of 3)

Fig. & Index No.	Designation	AULT Part No.	Indenture	Description	Qty. per Assy.
B-5					
-116	CR17	6001113	C	SEMICONDUCTOR DEVICE, DIODE	3
-117	CR3	6031220-1	C	SEMICONDUCTOR DEVICE, DIODE	11
-118	Q6	6011075	C	TRANSISTOR, Type 2N3509	17
-119	CR14	6031303	C	SEMICONDUCTOR DEVICE, DIODE	2
-120	CR13	6031303	C	Same as CR14	Ref
-121	CR2	6051100-30	C	SEMICONDUCTOR DEVICE, DIODE	2
-121	CR7	6001113	C	Same as CR17	Ref
-123	CR8	6031216	C	SEMICONDUCTOR DEVICE, DIODE	3
-124	Q8	6031151	C	TRANSISTOR, Type 2N3638	3
-125	Q5	6011075	C	Same as Q6	Ref
-126	Q4	6011153	C	TRANSISTOR, Type 2N3644	2
-127	Q3	6011073	C	TRANSISTOR, Type 2N3053	3
-128	CR1	6031220-1	C	Same as CR3	Ref
-129	CR10	6051100-2	C	SEMICONDUCTOR DEVICE, DIODE	4
-130	CR11	6001113	C	Same as CR17	Ref
-131	Q1	6011075	C	Same as Q6	Ref
-132	Q24	6011073	C	Same as Q3	Ref
-133	CR4	6031220-1	C	Same as CR3	Ref
-134	Q2	6011075	C	Same as Q6	Ref
-135	CR5	6031171	C	SEMICONDUCTOR DEVICE, DIODE	1
-136	CR9	6031220-1	C	Same as CR3	Ref
-137	Q9	6011075	C	Same as Q6	Ref
-138	Q10	6011075	C	Same as Q6	Ref
-139	CR31	6031264	C	SEMICONDUCTOR DEVICE, DIODE	1
-140	CR30	6031220-1	C	Same as CR3	Ref
-141	Q21	6011075	C	Same as Q6	Ref
-142	CR29	6051100-2	C	Same as CR10	Ref
-143	CR32	6001073	C	SEMICONDUCTOR DEVICE, DIODE	1
-144	Q20	6011075	C	Same as Q6	Ref
-145	CR24	6051190-1	C	SEMICONDUCTOR DEVICE, DIODE	1
-146	CR33	6031220-1	C	Same as CR3	Ref
-147	CR34	6051100-30	C	Same as CR2	Ref
-148	Q22	6011075	C	Same as Q6	Ref
-149	CR26	6031220-1	C	Same as CR3	Ref
-150	CR21	6031220-2	C	SEMICONDUCTOR DEVICE, DIODE	4
-151	CR35	6051100-2	C	Same as CR10	Ref
-152	CR20	6031220-2	C	Same as CR21	Ref
-153	Q16	6011075	C	Same as Q6	Ref
-154	CR19	6031220-1	C	Same as CR3	Ref
-155	CR23	6031220-2	C	Same as CR21	Ref
-156	CR22	6031220-2	C	Same as CR21	Ref

Fig. & Index No.	Designation	AULT Part No.	Indenture	Description	Qty.* per Assy.
B-5					
-157	Q15	6011075	C	Same as Q6	Ref
-158	Q18	6011153	C	Same as Q4	Ref
-159	Q23	6011151	C	Same as Q8	Ref
-160	Q17	6011075	C	Same as Q6	Ref
-161	CR27	6031220-1	C	Same as CR3	Ref
-162	Q19	6011075	C	Same as Q6	Ref
-163	CR28	6051100-20	C	SEMICONDUCTOR DEVICE, DIODE	1
-164	CR25	6051211	C	SEMICONDUCTOR DEVICE, DIODE	1
-165	CR12	6031216	C	Same as CR8	Ref
-166	Q11	6011073	C	Same as Q3	Ref
-167	Q7	6011075	C	Same as Q6	Ref
-168	CR6	6031220-1	C	Same as CR3	Ref
-169	Q12	6011075	C	Same as Q6	Ref
-170	Q13	6011075	C	Same as Q6	Ref
-171	Q14	6011151	C	Same as Q8	Ref
-172	CR15	6031220-1	C	Same as CR3	Ref
-173	CR16	6051100-2	C	Same as CR10	Ref
-174	CR18	6031216	C	Same as CR8	Ref

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