LARGE SYSTEMS PRODUCT GUIDE

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1. SCOPE AND PURPOSE

- The LARGE SYSTEMS PRODUCT GUIDE is a tool for sales-persons, promoters and Marketing Staff.

- This guide is intended as the basic reference document for large systems marketing information.

  Any document pertaining to the subject of Large Systems Marketing, published by the Large Systems Marketing Division at CII-HB headquarters, will be either an update/addendum to the product guide, or will be referenced in the documentation index which is part of the product guide.

- The Large Systems Product Guide is a living document, in that it will be completed and updated as the need arises, i.e. as information becomes available or evolves.

- Should the reader have any comment, correction, suggestion to make, please send them to :

W. KING-GILLIES
CII-HB (2L 067 E)

B.P. 33

75960 PARIS CEDEX 20

FRANCE

2. INTRODUCTION TO THE LARGE SYSTEMS OFFERING

2.1. GENERAL INTRODUCTION

2.2. CHARACTERISTICS OF LARGE SYSTEMS USERS

2.3. CONCERNS OF LARGE SYSTEMS USERS

2.4. THE LARGE SYSTEMS OFFERING

2.1. GENERAL INTRODUCTION

- The CII-HB Large Systems offering is based on hardware/software products as well as services, with the purpose of procuring revenue from :
  - new contracts : new systems
  - add-on contracts : add-on's to existing parc.
- Before going into the description of our products and services, it is useful to have a look at what our market is, in terms of characteristics and concerns of large systems users/prospects.

2.2. CHARACTERISTICS OF LARGE SYSTEMS USERS

There are three essential areas which provide characteristics :

a. Workload

- The workload achieved by large systems users sets the requirement for powerful central processors. We place the lower limit around 750 Kops (750 kilo operations per second).

  Note that our DPS 8 entry model, the 8/46, operates at roughly (770) 780 Kops.

- The workload of large systems users, hence the required throughput of the systems increases at annual rates between 20 % and 40 %.

b. Mode of operation

- The typical large system operates in a variety of modes simultaneously :
  - batch,
  - remote-batch,
  - transaction processing,
  - time-sharing
- The market we are looking at, today and into the 80's, is characterized by an ever stronger emphasis on interactive processing, which includes transaction processing, time-sharing and a variety of so-called "end-user facilities", such as forms query, procedural query with or without report generation, and even, in the longer-term, natural language query.

- The interactive orientation means distributing access to information and to the computer system's resources.

  This trend to distribution leads even further into distributing processing power, data bases and applications.

- The market analyses provide three interesting figures :

  - o By 1985, between 80 and 90 % of large systems users will have some form of distributed system ;
  - o By 1985, in large firms and organizations, 1 person out of 3 will be using a terminal ;
  - o The annual growth rate of terminal usage is between 16 and 35 %.

  It is for these reasons, among others, that CII-HB introduced DSE (the Distributed Systems Environment) in 1977 as a framework for its product developments, DSA (the Distributed Systems Architecture) in 1979 as an architecture and products which fit into the DSE, and the QUESTAR family of terminals in 1980.

c. Organization of data

- Large systems users process enormous quantities of information, and typically the information is organized in integrated data bases, simultaneously accessed by numbers of applications in the various modes of operation.
- On-line databases currently reach sizes in thousands of million characters.
- The annual growth rate of mass storage capacity varies between 50 and 60 %.

2.3. CONCERNS OF LARGE SYSTEMS USERS

Due to their characteristics, large systems users have a number of concerns We have chosen eight of them, and represented them with eight key-words, which also characterize highlights of our Large Systems offering (DPS 8, GCOS 8, DSA), so that we show that the concerns of large systems users were taken into account in our product developments and that our products provide satisfactory responses to the users needs.

Here are the eight key-words, followed by an explanation for each of them :

* PERFORMANCE
* GROWTH
* AVAILABILITY
* SECURITY
* NETWORKING
* EASE-OF-USE
* PRODUCTIVITY
* EVOLUTION

* PERFORMANCE

Because of their workload, large systems users require powerful central processors, high system throughput, low response-times.

Our response to this is the DPS 8 family with the GCOS 8 Operating System and the set of software which runs under it, such as the DM IV Transaction Processor.

The performance requirements are met not only by hardware, but by the efficient use which software makes of it.

* GROWTH

Users will not invest in a system if they cannot be guaranteed that it can grow in harmony with their workload.

The DPS 8 provides for growth, both vertical, with on-site performance upgrades, and horizontal, with the addition of CPU's, SCU's, IOM and of course memory.

The central system hardware raw performance spectrum, from the single-processor 8/46 to the quadruple processor 8/70, ranges from 1 to 8.

* AVAILABILITY

- o Particularly in an interactive/transactional mode of operation, availability of the system is a major requirement, because any down-time may have a dramatic business impact.

- o The DPS 8 systems technology, architecture, and software provide utility-grade availability, with features such as :
  - error detection and correction (EDAC),
  - fully redundant hardware configuration,
  - dynamic reconfiguration,
  - recovery-restart.

* SECURITY

- o In an environment where access to EDP resources is widely distributed, to numerous classes of users, with different degrees of technical knowledge, it is fundamental to grant each user a level of authorization such that only those applications and files which are relevant to his/her particular job can be accessed.

  The whole purpose of the security procedures is to preserve the integrity of information and protect it from accidental or wilful error or misuse.

- o It is also essential that programming errors do not result in corrupting or destroying areas of memory which are beyond the limits of the faulty program.

- o The DPS 8 /GCOS 8/DM IV system provides built-in mechanisms and tools to guarantee security at all levels.
  - hardware-controlled access to memory segments/domains,
  - schema/sub-schema mechanism for access to data-bases,
  - user identifications and passwords at various levels,
  - file access rights (read/write...)

* NETWORKING

- o Practically all large systems users, in the market where we compete, have a network, with some or all of the following elements :
  - front-end processors,
  - terminals,
  - remote-batch equipment,
  - concentrators,
  - message switching devices,
  - satellite systems.
- o Users are now looking at the possible use of public data networks.
- o Our response to the networking needs of large systems users is DSA (the Distributed Systems Architecture), which enables the construction of any form of network, from the simplest to the most complex.

  DSA and the associated products fit into the users current system and are open for future evolution, in the direction most suited to the users' organizational requirements.

  Furthermore, the GCOS 8 Operating System was designed to fit into the DSE framework : the basic concepts used in its design and its architecture make GCOS 8 an integral part of DSA.

* EASE-OF-USE AND PRODUCTIVITY

- o These two concerns really go together and are direct consequences of the following factors :
  - increasing salary costs,
  - wide distribution of access to EDP resources to end-users,
  - need to increase the number and range of applications,
  - need to make maximum and most efficient use of EDP resources.

- Ease-of-use is a requirement for all classes of users :
  - system operation managers,
  - data base/applications administrators,
  - system operators,
  - application developers/programmers,
  - end-users.

- The basic requirement is that people in the firm or organization spend their time on activities which are directly useful/ productive for the business, and not waste time on EDP "technicalities" which do not do anything for the business.

- Our response to ease-of-use and productivity requirements is comprehensive, in that it covers the whole range of users, with products available now or planned for future releases of our systems.

  In order to better specify the products, these are categorized according to the class of users they are intended for :

  - SMF : System Management Facilities

    This category includes all the tools and features which are intended for system operation, data base and application administration.

    For example :

    - Extended Job Control Language,
    - System status monitors,
    - System performance monitors,
    - Accounting/billing facilities,
    - Reconfiguration tools,
    - Data base and applications administration tools/utilities.

- ADF : Application Development Facilities

  This category includes all the tools available to the application developers and programmers, for example :

  - high-level languages,
  - interactive debugging facilities,
  - powerful text editors.

- EUF : End-User facilities

  This category is the broadest, since it includes all the tools available to the ever-expanding population of EDP users throughout firms and organizations.

  It includes, for example :

  - Time-Sharing facilities,
  - Procedural query with or without report generation,
  - Forms query,
  - Natural-language query.

* EVOLUTION

o This is a major preoccupation of large systems users : it translates into preservation of investments made in equipment, people, organizational structures and particularly applications.

  The key-word is COMPATIBILITY.

o Our response to this major requirement is extremely adequate and is demonstrated by past years of product evolution with compatibility, which has always been a key objective in all our developments and is unique with respect to other vendors.

- Our product offering today includes many novelties, which can be proposed to current customers without major disruption to their EDP system ; furthermore, evolution may be achieved in steps, with relative independence.

  The areas of evolution are the following :

  - central system,
  - peripherals,
  - network,
  - operating system,
  - applications.

  Examples of one-step evolution without impact on other areas are :

  - central system change,
  - installation of new peripherals,
  - migration of network to DSA, using a coexistence approach,
  - change of Operating System from GCOS III to GCOS 8,
  - change of applications, from the BCD to the DM IV environment, using the DDE (Dual Data Environment) facility.

- With a worldwide parc of over 1800 (1500) large systems, our company is as concerned about evolution and compatibility as our customers are.

2.4. THE LARGE SYSTEMS OFFERING

- Given the market characteristics and concerns of large systems users, which are also the highlights of our large systems products, we can be confident that we have an attractive and competitive offering.

- A new system offer typically consists of :
  - DPS 8 central system and peripherals,
  - DN 710X front-end processors,
  - GCOS III or GCOS 8 Operating System,
  - DM IV applications software,
  - Time-Sharing software,
  - DNS (telecomms software for DN 710X),
  - Distributed Customer Services (DCS),
  - Specialized applications software,
  - Courses

  All these items are covered in this Product Guide, but there are others which are not covered,but which nevertheless are part of the Large Systems Environment, in particular :
  - Mini-6 satellites or concentrators,
  - QUESTAR terminals,
  - Page-Printing System (PPS)

- With DPS 8, CII-HB introduced a new pricing structure, whereby products and services are fully unbundled, i.e. there is a price-tag on each item of our hardware, software and services catalogue.

- In effect, signing for a system involves two contracts :
  - a hardware contract,
  - a software contract.

- The software contract includes the list of all items to be used by the customer, with the corresponding licence fee (or in some specific cases, one-time fee), even if the item is "no-charge".

- The licence fee includes an associated service (described in (expanded 5.1. DCS). Actual support of the software, called "support service" (expanded support) is provided as an option, also included in the software contract.

- The "support service" option is not selective, in that it applies to either all items or none.

  Note that the "support service" option for the Operating System Executive or kernel (OSE) is a function of the central system hardware to which it applies, so that when a central processor performance upgrade or additional processor is ordered, the "support service" fee for the OSE has to be changed.

- The software contract also includes the so-called "designated system", on which the software is to operate. It is important in this context to properly understand and apply the definition of a "HARDWARE SYSTEM", not only for contractual, but also reporting and planning purpose :

  "A HARDWARE SYSTEM is a set of hardware equipment on which, at any given time, no more than ONE OPERATING SYSTEM EXECUTIVE is in operation."

  Note that a hardware system in the DPS 8 family is characterized by a Marketing Identifier of the form CPS82XX.

  So wherever a hardware configuration with one and only one CPS82XX is functioning, there must be one and only one GCOS executive in operation.

  As a consequence, for each CPS82XX in a hardware contract, a software contract for an operating system executive and relevant software items must also be established.

- The above definition and guidelines also apply to the DN 710X Front-end processors, where a hardware system is identified by the Marketing Identifier DCP710X.

  So for each DCP710X in a hardware contract, there must be a contract for DNS software.

3. HARDWARE

3.1. DPS 8 SYSTEMS DESCRIPTION AND CONFIGURATION RULES

3.2. SUMMARY CONFIGURATOR

3.3. PARC EVOLUTION

3.4. RECYCLED EQUIPMENT

3.5. SYSTEMS PERFORMANCE SUMMARY

3.1 DPS 8 SYSTEM DESCRIPTION AND CONFIGURATION RULES

3.1.1 CENTRAL SYSTEMS

3.1.2 POWER SUPPLIES

3.1.3 CONSOLES

3.1.4 MASS STORAGE SUBSYSTEMS

3.1.5 MAGNETIC TAPE SUBSYSTEMS

3.1.6 UNIT RECORD SUBSYSTEMS

3.1.7 PERIPHERAL SWITCHES

3.1.8 FRONT-END PROCESSORS

3.1.9 SUMMARY LIST AND DESCRIPTION OF ITEMS

3.1.1 CENTRAL SYSTEMS SUMMARY

Obtained from two hardware product architectures, the DPS 8 line is composed of the following five models.

DPS 8/~~47~~
DPS 8/49 84
DPS 8/~~52~~
DPS 8/~~62~~
DPS 8/70 74

- The two Entry Level models DPS 8/47 and DPS 8/49 are from the ELS system architecture.
- DPS 8/52, DPS 8/62 and DPS 8/70 are the already known DPS-E models.
- The five DPS 8 models operate under GCOS 8 operating system; GCOS III may also be used with DPS 8/52, DPS 8/62 and DPS 8/70.
- All models are fully compatible under GCOS 8 for customer applications, and support the same peripherals.
- On site upgrade is easy from DPS 8/47 to DPS 8/49 or from DPS 8/52 to 8/62 or 8/70 but not possible from ELS architecture DPS 8/47 or DPS 8/49 to DPS-E architecture DPS 8/52, 62, 70.
- DPS 8/47 is a single system only while DPS 8/49 configuration may reach up to 4 processors, 2 SCU, 2 IOM and 32 MB of memory.
- These two models are built in FAIRCHILD ADVANCED SCHOTTKY TTL (FAST TTL Technology).

3.1.1.1 BASIC E.L.S ARCHITECTURE CENTRAL SYSTEM

. The DPS 8 ELS architecture includes two basic central system models, named as follows.

DPS 8/47	MI	CPS 8139
DPS 8/49	MI	CPS 8141

A basic central system consists of the following elements:

- One central processor unit (CPU)
- One system control unit (SCU)
- One Input Output Multiplexer (IOM)
- Four million bytes (4MB) of central memory
- One 32 Kbytes cache memory
- One DPU included in the CPS.
- One 100 ms Ridethrough option per cabinet.

Both the DPS 8/47 and DPS 8/49 use the same CPU but with different performance levels.

DPS 8/47: 1 (approximately 720 KOPS)
DPS 8/49: 1.46 (approximately 1050 KOPS)

. DPS 8/47 is on site upgradable to DPS 8/49. DPS 8/49 may accept several CPUs, IOMs, SCUs.

Refer to 3.1.1.7 ELS Central System Upgrade.

PHYSICAL CHARACTERISTICS

DPS 8/47 and DPS 8/49 are located in two basic and fixed cabinets.

Total size of the two cabinets

Height	73.5 in	(186.7 cm)
Width	80.9 in	(205.5 cm)
Depth	32.7 in	(83.1 cm)

These cabinets provide room for

- CPU plus DPU
- IOM
- SCU plus up to 16MB of 64K bit chip memory
- Power supplies and cables

and optionally:

1 tape controller single channel

2 disk controllers (two single channels or one dual channel)

Room Layout

The first cabinet, CPU cabinet, includes:

- CPU plus DPU
- SCU plus up to 16 MB of memory

power supplies for the system

Plus one optional disk controller

The second cabinet (I/O cabinet) includes:

- IOM with 20 channel slots
- Room for cables

Optional:

- One single channel tape controller
- One disk controller

on DPS 8/49 the second CPU cabinet is a prerequisite for a second I/O cabinet.

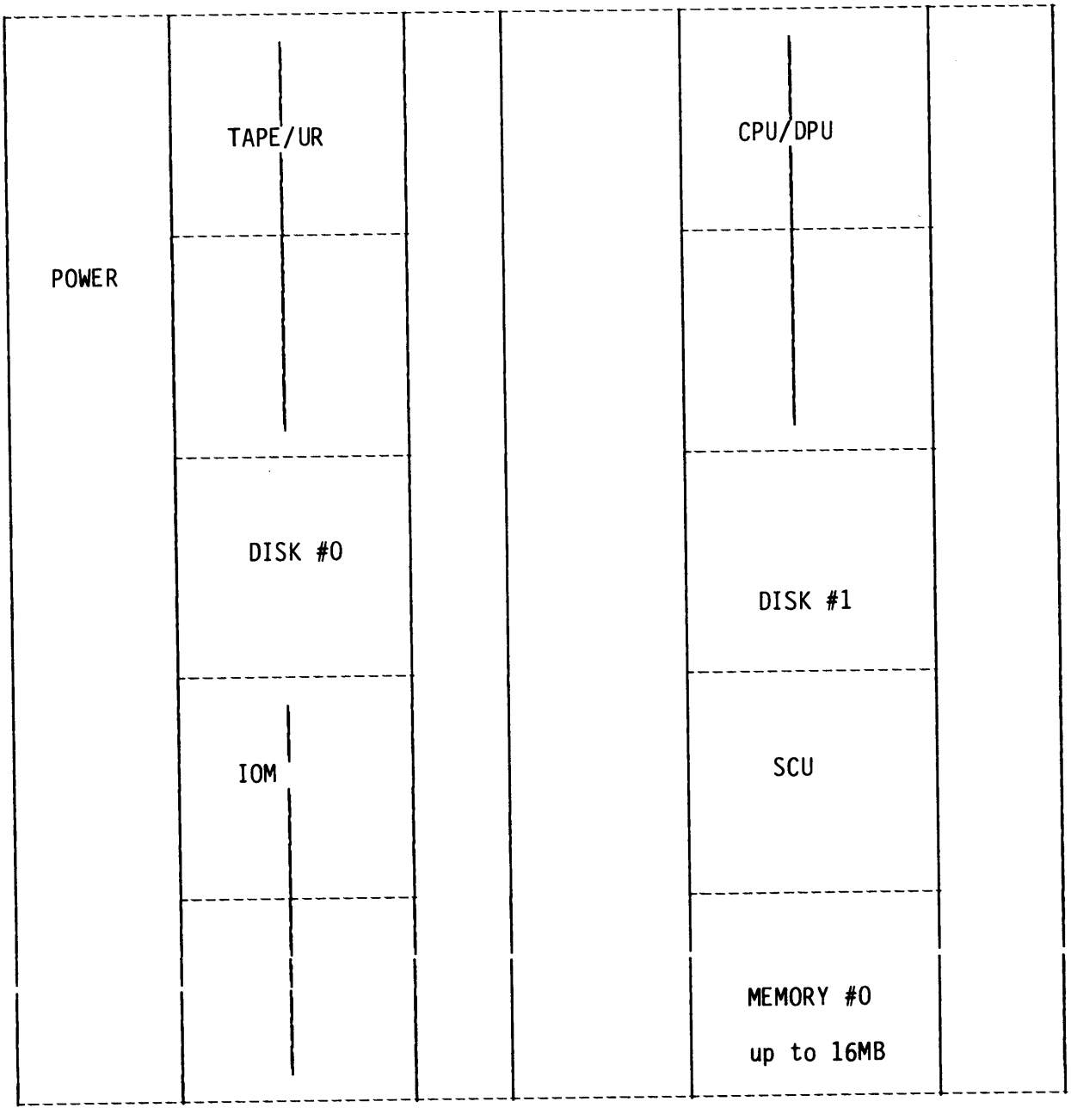


Figure A.2.1

3.1.1.1.2 C P U

The CPU is a microprogrammed central processor with an interior decor which is a superset of the L66/DPSE Processor using four-stage "pipelines" and microprocessors controlled by firmware.

Performs

- arithmetic and logic operations
- extended instructions (EIS)

Contains

* Hardware/Firmware used by GCOS 8 for:
  - dynamic memory management (Segmentation and paging)
  - domain protection
* 32 KB Cache Memory

Handles: address preparation

Controls faults and interrupts

Interface with memory

. The CPU has the hexadecimal floating point capability which gives the CPU a range of ± 10 to the 153rd power. This feature is used by Fortran 77.

3.1.1.1.3 S C U

. Located in the same cabinet as the CPU, the system control unit (SCU) has three main functions:

- to handle all data transfers to/from memory,
- to interface CPUs and IOMs,
- to memorize and manage all interrupts.

The basic SCU has five ports. It may be upgraded on site to 8 ports, if more than two CPU's are configured.

- Two SCUs may be configured on DPS 8/49; in this case, a second processor is a prerequisite.

3.1.1.1.4 I O M

. The Input Output Multiplexor (I O M) handles all data transfers to/from the peripherals and Front-End Processors.

. The I O M stores data into or retrieves data from central memory without interrupting the CPU. It is capable of translating segmented/paged addresses into absolute addresses without interrupting the CPU.

. The I O M has a memory of its own, called the "Scratch-pad" memory; using it, limits the number of accesses to central memory.

. Communications with the peripherals take place via an I/O bus, to which channels leading to/from the peripherals, are connected.

. Channel management, including the dialogue between I O M and peripherals, requires logic which is implemented on hardware boards, fitted into the so-called I O M "slots". In average, a channel requires three boards, i.e. three I O M slots.

  Since the I O M has 20 slots, the average number of suported channels is 6.

  One IOM only is authorized on DPS 8/47 (included in the CPS). However, two IOM's may be configured on DPS 8/49; in this case a second processor is a prerequisite.

3.1.1.1.5 D P U

. The Diagnostic Processor Unit (DPU) is a feature composed of two boards which reside in the CPU backpanel.

. The DPU interfaces with the CPU, IOM, and SCU of the system and serves the following purposes:

  - Maintenance panel functions (off-line testing),

  - Remote connection to a TTY or VIP terminal for DCS, (Distributed Customer Services).

. In addition, the DPU also provides a path from the low cost console to the dynamic maintenance panel interfaces of the IOM and SCU. These connections permit the local and remote access to these units via the dynamic panel interfaces in addition to the CPU.

. The DPU is included in the CPS Marketing identifier.

3.1.1.1.6 Memory

- The DPS 8/47, 49 central memory is implemented with VLSI MOS Technology Chips. Each VLSI MOS chip contains 64 K (65.536) bits and 16 connection pins.

- 64 K memory chips are assembled on hard copper boards along with the addressing logic. A board contains 1 MB of a 36 bit word.

- Boards are mounted into a bucket located in the CPU cabinet. The bucket may contain up to 16 boards, i.e. total of 16 MBytes.

- The controller manages the MOS memory and drives it at a speed of 750 nanoseconds; it also detects and corrects memory errors, by means of the EDAC feature (Error Detection and Correction).

- Memory size is limited to 16 MB per SCU.

3.1.1.1.7 CENTRAL SYSTEMS EXTENSIONS

. CPU performance upgrade and memory size extension are only allowed on DPS 8/47.

. CPS 8/49 may be extended up to 4 CPU's, 2 IOM's, 2 SCU's and 32 MB of memory.

Upgrades

DPS 8/47 may be upgraded from .65 to .95 by CPK 8337 which is the upgrade from CPS8139 to CPS8141.

. Memory upgrade up to 16 MB by increment of (2 Megabyte or 4 Megabyte Modules) CMM8002 or CMM8003.

(Up to 6 additional modules)

DPS 8/49

The extension may be done in two ways:

* Full redundancy option (CPF8132)

the option includes:

- One additional CPU
- One additional 5 Ports SCU
- One additional IOM

- 4 MB of memory
- crossbar features required to interconnect the basic elements of the central system, thus making it a redundant system.

Two additional processors CPU8131 may be added to the redundancy system. Then, *two MXK8009 options (SCU upgraded from 5 ports to 8 ports), are required.

With the redundancy option, one additional console CSU 6601 is required.

* Independent components

DPS 8/49 may also be upgraded by the addition of up to 3 additional processors CPU 8131, plus one additional IOM, MXU8003, and one additional SCU, MXC8003.

The second additional CPU requires an additional CSU6601.

- the first additional CPU is a prerequisite for the additional IOM and SCU.

The second additional CPU requires that the MXK8009 (8 port option) on each SCU is configured.

Required features to interconnect components are included in Marketing identifiers.

3.1.1.2.1 Basic DPS-E Central System

The current DPS 8 family includes three basic central system models, named as follows:

DPS 8/52	MI:	CPS 8257
DPS 8/62	MI:	CPS 8267
DPS 8/70	MI:	CPS 8277

A basic central system consists of the following elements:

- One central processor unit (CPU)
- One system control unit (SCU)
- One input/output multiplexor (IOM)
- Four million bytes (4MB) of central memory divided on two buckets
- One 32K byte cache memory.

A diagnostic processor unit, DPU, is mandatory on all DPS 8 systems listed above.

The DPU is company property and must not appear in the customer contract. However, it must appear on the equipment order for any of the above central systems, under one of the following identifiers:

DPU 9001 DPU with 60 Hz power capability

DPU 9001B DPU with 50 Hz power capability

The three DPS 8 models use the same CPU, but with different performance levels:

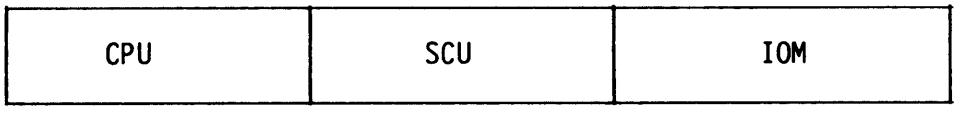
DPS 8/52:	(approximately 1045 KOPS)
DPS 8/62:	(approximately 1430 KOPS)
DPS 8/70:	(approximately 1870 KOPS)

For more information on performance level, refer to 3.5 systems performance summary.

DPS 8 systems are on site upgradable to the next performance level.

Refer to 3.1.1.7. Central system extensions.

The central system elements are grouped into independent cabinets of equal dimensions according to the following layout.



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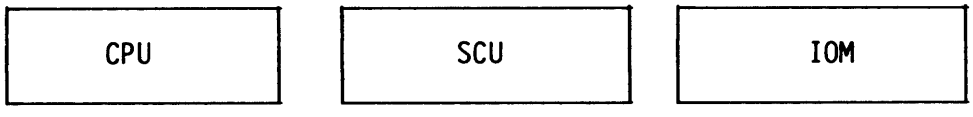
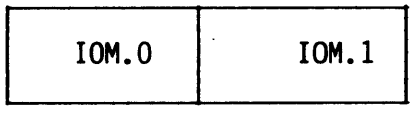


REDUNDANT SYSTEM CONFIGURATION



NOTE: EACH CABINET INCLUDES THE POWER SUPPLY

3.1.1.2.2 C P U

The DPS 8 CPU's include the following units:

- Operation unit (OU) where arithmetic and logic operations are performed.
- Decimal unit (DU) where the extended instruction set (EIS) operations are performed.
- Control unit (CU) which
  handles address preparation,
  controls faults and interrupts,
  interfaces with memory,
  contains the cache memory.
- Virtual unit (VU), which contains the hardware, used by GCOS 8, for:
  - dynamic memory management (segmentation and paging), domain protection

All DPS 8 models listed in 3.1.1.1 have the hexadecimal floating point capability, which gives the CPU a range of +10 to the 153rd power. This feature is used by FORTRAN 77.

3.1.1.2.3 S C U

The System Central Unit (SCU) has three main functions:

- to handle all data transfers to/from memory
- to interface CPUs and IOMs,
- to memorize and manage all interrupts.

An SCU can handle up to 64M bytes of central memory (TYPE MOS 64K), but this size is limited for marketing and security reasons to 16 MB.

The SCU can become a bottleneck in a large configuration, with multiple CPUs and IOMs, so it is also recommended to have multiple SCUs in such configurations.

Of course, multiple SCUs is a factor of security/availability.

Consult your F.E. specialist to determine the optimum number of SCUs in a given configuration and how to distribute the memory modules between the various SCUs.

3.1.1.2.4 I O M

The Input Output Multiplexor (I O M) handles all data transfers to/from the peripherals and Front-End Processors.

The I O M stores data into or retrieves data from central memory without interrupting the SCU. It is capable of translating segmented/paged addresses into absolute addresses without interrupting the CPU.

The IOM has a memory of its own, called the "Scratch-pad" memory; using it, limits the number of accesses to central memory.

Communications with the peripherals take place via an I/O bus, to which the peripheral channels are connected.

Channel management, including the dialogue between I O M and peripherals, requires logic, which is implemented on hardware boards fitted into the so-called I O M "slots". A channel requires, in average, three boards, i.e. three I O M slots.

Since the I O M has 35 slots, the average number of supported channels is 11.

However, the actual number of channels supported is dependent on the total throughput of the connected devices.

So, consult your F.E. specialist to determine the optimum number of I O Ms in a given configuration.

3.1.1.2.5 D P U

The Diagnostic Processor Unit (DPU) is a feature on all DPS 8 systems listed in 3.1.1.1.

The DPU interfaces with each CPU, IOM, and SCU in the systems and serves the following purposes:

- maintenance panel functions (off-line testing),
- remote connection to a TTY or VIP terminal for DCS (Distributed Customer Services)

In addition, the DPU is connected via the CSU6601 console channel to the IOM. It is thus possible to execute under GCOS on-line test and diagnostic programs submitted from the remote console connected to the DPU.

The DPU provides the capability to check and troubleshoot the CPU, IOM and SCU in an off-line mode,

The DPU is based on a Mini 6/43 computer, operating under MOD 400 software.

As mentioned in 3.1.1.1, the DPU must be ordered explicitely, using the identifier MPU 9001 (60 Hz) or MPU 9001B (50 Hz).

The DPU remains company property, and must not appear in the customer contract.

3.1.1.2.6 Memory

DPS 8 central memory is implemented with VLSI MOS Technology Chips. Each VLSI MOS chip contains 64K bits.

64K memory chips are assembled on hard copper boards, along with the addressing logic. A board contains 160 chips, the equivalent of 1 MB.

Boards are mounted into buckets, which also contain the actual memory controller. A bucket may contain up to 16 boards, so a total of 16M bytes.

The controller manages the MOS memory and drives it at a speed of 750 nanoseconds, it also detects and corrects memory errors, by means of the EDAC feature (Error Detection and Correction).

Buckets are loaded into the SCU cabinet. A cabinet contains up to two buckets.

When a SCU cabinet is full, i.e. 16M bytes, a second SCU is mandatory.

This rule is true for marketing and security reasons.

3.1.1.2.7 Central systems extensions

There are a number of extension options which apply to the DPS 8 basic central systems

* Full redundancy options

There are two such options, which apply respectively to the 8/52 and 8/62.

The options include:

- one additional CPU, with 32K byte cache
- one additional SCU
- one additional IOM
- 4M bytes additional memory divided on two buckets
- crossbar features required to interconnect the basic elements of the central system, thus making it a redundant system.

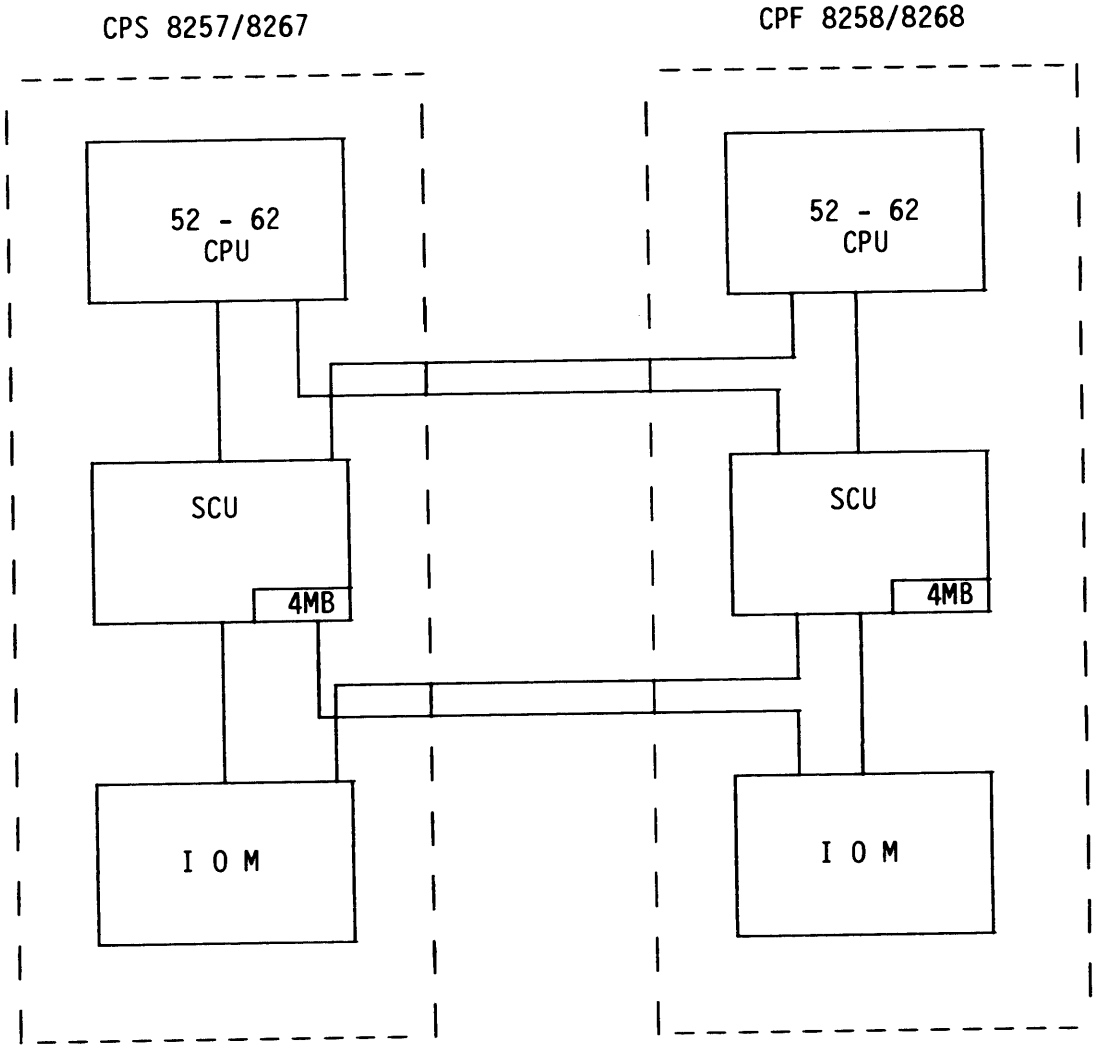
The two options have the following marketing identifiers:

CPF8258 Full redundancy option for DPS 8/52

CPF8268 Full redundancy option for DPS 8/62

Before being upgraded to a redundant system, the installed DPS 8/46 has to be transformed to a DPS 8/52

Redundant 8/52 and 62 central systems have the following layout:



* Additional 8/70 CPU: CPU 8189

Up to 3 CPUs may be added to the 8/70 basic central system.

* Additional SCU: MXC 8002

This item applies to the 8/52, 62 redundant systems and to the 8/70 mono or multi-processor systems. The maximum number of SCUs supported by redundant 8/52, 62 systems and by 8/70 systems is 4.

Additional SCUs are delivered with the features required to crossbar the various elements of the central system.

* Additional IOM: MXU 8002

This item applies to the 8/52, 62 redundant systems and to the 8/70 mono or multi-processor systems.

The maximum number of IOMs supported by redundant 8/52 and 62 systems and by 8/70 systems is 4.

Additional IOMs are delivered with the features required to crossbar the various elements of the central system.

* ADDITIONAL MEMORY

° There are three items available for memory increments:

CMM 8021 2 Mega bytes

CMM 8022 4 Mega bytes

CMM 8023 8 Mega bytes

° A maximum of one CMM 8022 item is allowed on each system.

° CMM 8023 is allowed to reach 16/32/48/64 M bytes.

° For technical reasons, total memory sizes must be: (4, 8, 16, 32, 48 or 64) M bytes.

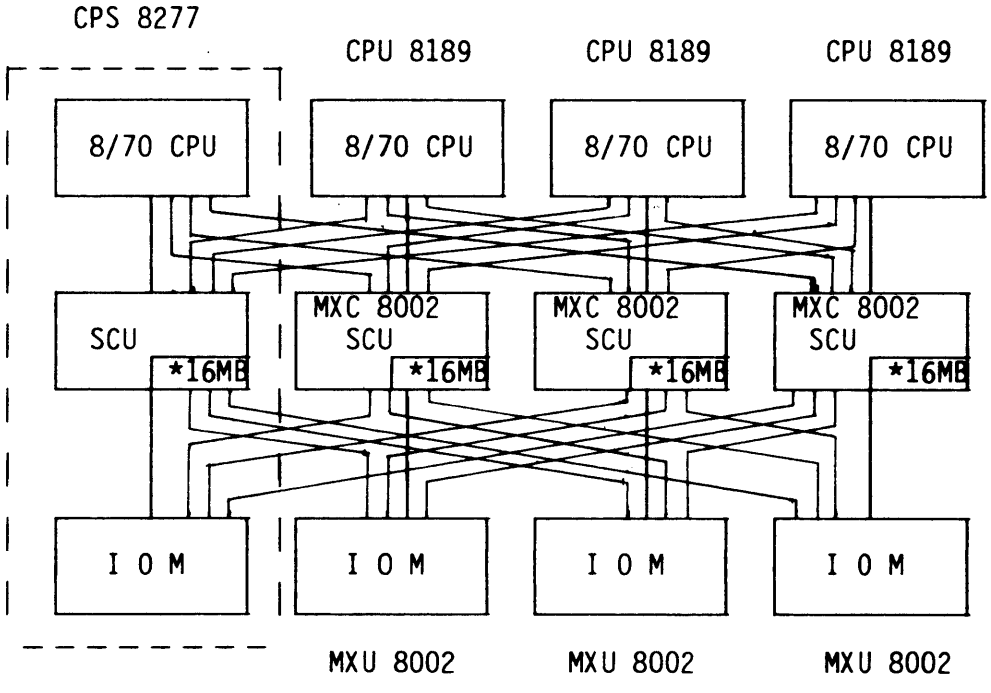
° Under GCOS III, total memory size is limited to 8M bytes.

° Under GCOS 8, total memory size on DPS 8 systems is limited to 64M bytes.

° The following tables summarizes the possible sizes.

SYSTEM MODEL	BASIC MEMORY SIZE	+ CMM8022	1 + 2 + 2 + 2
8/52 mono	4MB	8MB	16/32/48/64 MB
8/52 red.	8MB		16/32/48/64 MB
8/62 mono	4MB	8MB	16/32/48/64 MB
8/62 red.	8MB		16/32/48/64 MB
8/70 mono or multi CP	4MB	8MB	16/32/48/64 MB

The following diagram shows the layout of a maximum DPS 8/70 central system (not including the DPU).



* The total memory size of 64 MB is obtained by adding 60 MB to the 4 MB included in the basic central system. The 60 MB are ordered as CMM 8022 + 7 x CMM 8023.

Central system performance upgrades.

It is possible to upgrade a DPS 8 system on site to the next performance level.

The following items are the processor performance upgrade options:

CPK 8257	8/52	to	8/62	upgrade
CPK 8267	8/62	to	8/70	upgrade
CPK 8258	8/52	to	8/62	redundancy upgrade
CPK 8268	8/62	to	8/70	redundancy upgrade

FROM \ TO	8/49	8/62 MONO	8/62 REDUNDANT	8/70 MONO	8/70 REDUNDANT
8/47 mono	CPK 8337				
8/52 mono		CPK 8257			
8/52 red.			CPK 8257 + CPK 8258		
8/62 mono				CPK 8267	
8/62 red.					CPK 8267 + CPK 8268

3.1.2 POWER SUPPLIES

3.1.2.1 Rules

- All new DPS8 central units and peripheral controllers accept 50 Hz or 60 Hz 208 volts power. The hardware is the same for the two frequencies. The frequency is selected at installation time.

- Peripherals have to be ordered in 50 Hz 220 volts or 60 Hz 208 volts. Modification from one frequency to the other is not possible. For 50 Hz peripherals, letter B follows the 60 Hz marketing identifier - except CRU 0501 and MSU 0451 for which the 60 Hz MI is CRU 0501A and MSU 0451A and 50 Hz MI CRU 0501B and MSU 0451B.

- On the same site MIX of frequency is allowed between centrals and peripherals of different families.

- DPS 8 centrals and peripheral controllers must be protected against interruptions caused by short voltage dips.

- When two frequencies are used, isolation transformers must be installed to protect equipment against interferences.

3.1.2.2 * Protection agaist short voltage dips by:

Features provided by external suppliers

- fly wheel motor generator
- static convertor (UPS)

DPS 8 options:

- Ridethrough capacitor

Features provided by external suppliers:

Customers may use them in order to:

- protect system against short interruptions
- convert the frequency
- adjust the voltage.

Two different hardwares which are:

- flywheel motor generator
- static convertor.

Fly wheel motor generator

This feature has been removed from our DPS 8 catalog. This means that the customers are responsible for the purchase and installation of this feature.

. Since motor generators are very noisy, it is recommended to install them in the basement or at least in a room separated from the computer room.

  Installation of a control panel to control the motor generator from the computer room is mandatory.

Static convertor UPS

. This feature is preferable to a motor generator because it is less noisy and it permits frequency and voltage adjustments without modifications or change of hardware.

. Even if not recommended in some cases, DPS 8 systems may be supplied directly in 50 Hz. By the power distribution network for these installations the ride through option installation is mandatory on each CPU, IOM, SCU and peripheral controllers. These options protect hardware on which they are installed against interruptions caused by short voltage dips (up to 100 ms).

. In addition to the ride through option, hardware must be protected against network distribution interferences by isolation transformers providing 220 volts.

Options in our catalog:

PSS 8000 Capacitor ride through option, 1 required for each DPS-E CPU, IOM and SCU when MGS or UPS. are not used.

PSS 8001 Capacitor ride through option for MSP 0611/612 and MTP 0611 required when MGS or UPS are not used.

. In order to increase the system availability, it is possible to install (under SRPQ) the battery option on DPS 8 system SCU. This feature provides an additional 4 minutes of security for the memory. A warm boot is possible during this time.

3.1.3 CONSOLES

The CSU 6601 is the console available on DPS 8. With all its options, this console provides a large set of functionalities which fit all DPS 8 needs.

3.1.3.1 System console: CSU 6601

. At least one CSU 6601 must be configured with each DPS 8 system.

. The CSU 6601 provides functionality for:

- System Monitoring / operation
- Remote Maintenance

. The CSU 6601 is composed of:

- a VIP 7205 keyboard/display (12" screen)
- a TTU 1005 120 CPS serial printer used as a hard copy of the display.

Furthermore, the basic console includes the channel adaptor, a microprocessor, which fits into the IOM. This channel adaptor provides for connection of the keyboard/display, the printer and a Remote Console or Diagnostic Processor Unit (DPU).

. The following options may be added to the basic console:

* Console table: CSF 6601

. This is a "mandatory option", since it consists of:

- the table for the keyboard/display and printer
- the so-called "operator pod", which groups:
  . the processor speed indicators
  . Initialize, Boot and Emergency Power off buttons.

- Note that with the keyboard/display and printer on the table, there is very little room left for documents, listing, etc..., so we strongly recommend at least one additional pedestal, to choose from the following two options.

  * Pedestal for Serial Printer: CSF 6607
  * Pedestal for keyboard/display: DKF 7201
  * Auxiliary console: CSU 6602

    Includes:

    - a 120 cps serial printer with keyboard (TWU 1005)
    - the channel adaptor, which fits into the IOM, and provides for its connection.

    Note that this option does not include a table, so it is recommended to order an additional pedestal for serial printer (CSF 6607).

  * Keyboard/Display attachment: CSF 6602

    This option enables connection of an additional keyboard/display.

  * Additional keyboard/display: CSF 6603

    This option is a VIP 7205 keyboard and display (12" screen). A prerequisite is the CSF 6602. This additional keyboard/display enables display of the system status (VIDEO function).

  * 23" Monitor Display: CSF 6604

    . This option is a large screen, driven by the VIP 7205, which simply reproduces the information displayed on the CSU 6601 or CSF 6603 displays.

    . Up to 4 of these screens may be connected, in serial mode.

. A 305 m (1000 ft) cable supplies the video signal from the CSU 6601 or CSF 6603 display (modified VIP 7205).

* Extended system control feature: CSF 6606

. This option, which is a security/availability feature, is a switch, which can be applied between the basic console (CSU 6601) keyboard/display and:

- a remote console (terminal)
- an auxiliary console (CSU 6602)
- an additional keyboard/display (CSF 6603)

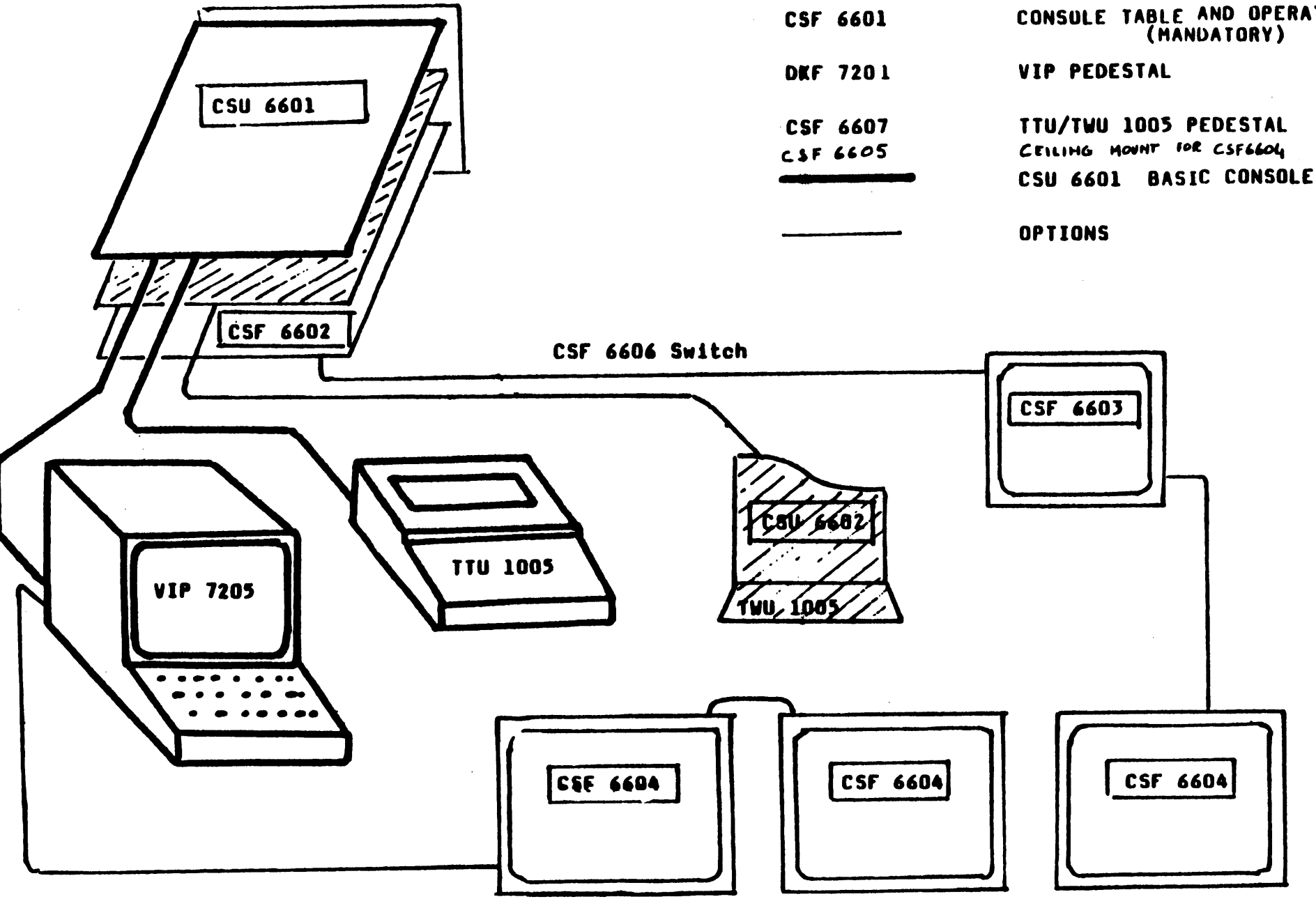
* Ceiling Mount: CSF 6605

Enables to hang a CSF 6604 from the ceiling.

As for the other peripherals to operate on 50 Hz the frequency must specified on the equipment order by adding the letter B to the MI, thus:

CSU 6601 becomes CSU 6601B.

The same is true for the additional keyboard CRT CSF 6603, additional CSU CSU 6602 and large screen monitor CSF 6604. These MI become CSF 6603B, CSU 6602B, and CSF 6604B.


CSF 6601
CONSULE TABLE AND OPERATOR POD (MANDATORY)
DKF 7201
VIP PEDESTAL
CSF 6607
TTU/TWU 1005 PEDESTAL
CSF 6605
CEILING MOUNT FOR CSF6604
CSU 6601 BASIC CONSOLE
OPTIONS
CSU 6601
CSF 6602
CSF 6606 Switch
CSF 6603
VIP 7205
TTU 1005
CSU 6602
TWU 1005
CSF 6604
CSF 6604
CSF 6604

3.1.4 MASS STORAGE SUBSYSTEM

3.1.4.1 Introduction

There are two types of mass storage controllers:

- integrated in central cabinet for ELS only;
- free standing for ELS and DPS-E, these units are replacing MSP0607/609

3.1.4.2 Free Standing Units

The new units provide improved cooling, reduced footprint and the ability to operate from any international power source in 50 or 60 Hz.

The new MSPs are available for connection to all models of DPS 8 LP (OS65) and MULTICS LP (OS86).

. The two models of MSP are:

MSP 0611	single channel
MSP 0612	dual simultaneous channel.

3.1.4.2.1 Product description

These two MSPs are packaged in LP cabinetry. They can co-exist with older type MSPs. Both the MSP 0611 and 0612 include a Device Adapter for controlling MSU 0500/ MSU 501 fixed disk drives and optional support of MSU 0451 removable disk drives.

. MSP 0611 is a single channel controller offering the same support as the MSP 0607. A maximum of sixteen spindles are supported in any mix of MSU 0451/0500/0501. The MSP 0611 provides an optional switched IOM channel, for MSP cross bar to another IOM, and an optional switched Datanet channel for use on systems running NPS.

  If MSU 04XX devices are connected, the MSP 0611 requires the MSU 04XX device adapter.

  The MSP 0611 can be on site upgraded to dual channel unit - MSP 0612.

. MSP 0612 provides a dual channel control for up to 32 spindles in the following combination:

16	x	MSU 04XX
	or	
15	x	MSU 050X
	or	
8	x	MSU 050X PLUS 16 x MSU04XX

  Both channels of the MSP 0612 are housed in the same cabinet, however, each channel has its own unique power supply.

By utilizing individual power supplies, a failure on one channel does not affect the other, thus allowing full access to the MSU via the working channel.

Each major channel is supported by a switched IOM channel allowing cross connection to other IOMs. Two switched FNP channels are provided by MSP 0611 allowing two NPS - FNPs to be supported. The two FNP channels are identified separately. In total, four switched channels may be configured on MSP 0612.

Like the MSP 0611, the MSP 0612 requires MSU 04XX device adapter if MSU 04XX devices are configured.

3.1.4.2.2 Physical description

Both MSPs are housed in a similar free standing cabinet, the dual channel MSP 0612 requiring one cabinet only.

	CABINET SIZE			WEIGHT	POWER SUPPLY			COOLING
	H	W	D		VOLTAGE	FREQ.	POWER	
MSP0611	73 in 185 cm	40.5 in 103 cm	32 in 83 cm	950 lbs 430 kg	120/208V 3 PH	50/50	1.6 KVA 1.3 KW	4500 BTU
MSP0612	73 in 185 cm	40.5 in 103 cm	32 in 83 cm	1100 lbs 499 kg	120/208V 3 PH	50/60	2.4 KVA 2.1 KW	7000 BTU

3.1.4.1.3 Marketing Identifiers

- Controllers

MSP 0611 Free-standing, single channel, Mass Storage Processor for use on DPS8 LP central system.
Includes adapter for controlling MSU 0500/501 devices.

MSP 0612 Free-standing, dual channel, Mass Storage Processor for use on DPS 8 LP central systems.
Includes adapter for controlling MSU 0500/501 devices.

MSU 04XX	15-16	13-14	11-12	9-10	7-8	5-6	3-4	1-2	0
	and	and	and	and	and	and	and	and	and
MSU 050X	0	1	2	3	4	5	6	7	8

- Options applicable to MSP0611, MSP8000, MSK8002

3.1.4.3 Integrated MSP (ELS only)

The integrated MSP located in the IOM cabinet permits the connection of 16 spindles. It supports:

- one link adapter for connection to the IOM from one to four device interface boards for connection of 1 - 16 spindles.
- One optional link adapter for connection to a front-end processor.

This processor can accommodate up to two controller adapters (CA):

- One in standard for the connection of MSU 0500/501
- The second optional for connection of MSU 0451.

This MSP may be upgraded to a dual simultaneous channel by adding of a second MSP into the CPU cabinet.

3.1.4.3.1 Marketing Identifiers

MSP 8000 Integrated Single Channel

MSP controller includes MSU 05XX adapter (ELS only).

MSK 8002

KIT TO UPGRADE MSP 08000 from single to dual simultaneous channel.

disk supported by single and dual channel MSP 8000.

MSU 04XX	15/16	13-14	11-12	9-10	7-8	5-6	3-4	1-2	0
MSU 050X	0	1	2	3	4	5	6	7	8

3.1.4.4 Marketing Identifiers - Options

- Options applicable to MSP 0611 only

MSK 0612 Upgrade kit from MSP 0611 to MSP 0612, maximum one.

This kit consists of all necessary logic cables/buckets/boards and power supplies for the second channel.

When the MSK 0612 is ordered for an MSP 0611, all options installed in this MSP must be ordered again with the MSK 0612.

- Options applicable to MSP 0611

MSF 1140 Device adapter for up to 16 MSU 04XX. Remember that the capacity limit of MSP 0611 is 16 spindles. So for configuration, the following table shows the configuration mix of MSU 050X and 4XX which must be followed.

MSA 1140 Single channel addressing capability for up to four MSU 04XX.

MSA 1141 Single channel addressing capability for up to two MSU 050X

- Options applicable to the MSP 0612 only

MSF 1141 Dual channel device adapter; allows the support of up to sixteen MSU 04XX. Provides adapters in both channels. Maximum one.

MSF 1142 Drive expansion adapter; allows connection of seven additional MSU 0500/501 units. Maximum one.

MSA 1142 Dual channel addressing feature to support up to four MSU 04XX. Provides addressing to both channels.

MSA 1143 Dual channel addressing feature to support up to two MSU 0500/501. Provides addressing to both channels.

- Options applicable to both MSP 0611, MSP 0612

MSF 1143 First non-simultaneous switched Datanet channel. Maximum one.

MSF 1150 Second non-simultaneous switched Datanet channel. Maximum one. Applicable on MSP 0612 only. MSF 1143 and MSF 1150 are used by NPS, FNPs only.

MSF 1144 Non-simultaneous switched IOM channel. Maximum one on MSP 0611 and MSP 8000 two on MSP 0612.

PSS 8001 Capacitor ride through option. As for central systems, the capacitor ride through option is mandatory in the case where the disk controller is operated on 50 Hz power and no MGS or UPS is used. Applicable on MSP 0611 and 612 only.

- Options applicable to MSP8000, MSK8002.

MSF8000 Device adapter for up to 16 MSU04XX.
Remember that the capacity limit of MSP 8000 is 16 spindles. So for configuration, the table showing the configuration mix of MSU050X and 4XX must be followed.

MSA8000 Single channel addressing capability for up to four MSU04XX.

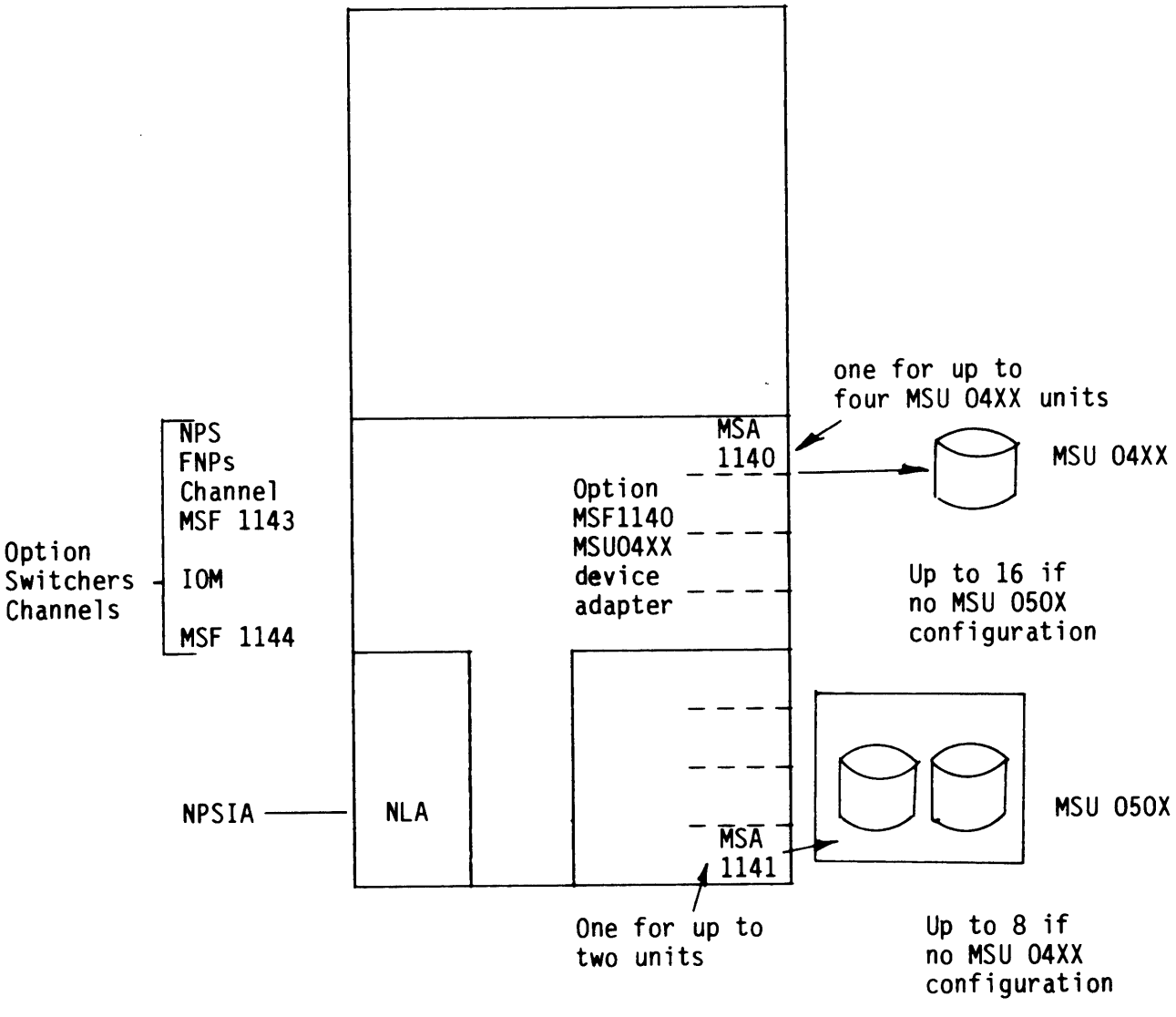
MSA8001 Single channel addressing capability for up to two MSU050X.

MSF8002 Non-simultaneous switched Datanet channel. Maximum one.

MSF8003 Non-simultaneous switched IOM channel.
Maximum one for each MSP8000.

3.1.4.1.4 Configurations

- MSP 0611



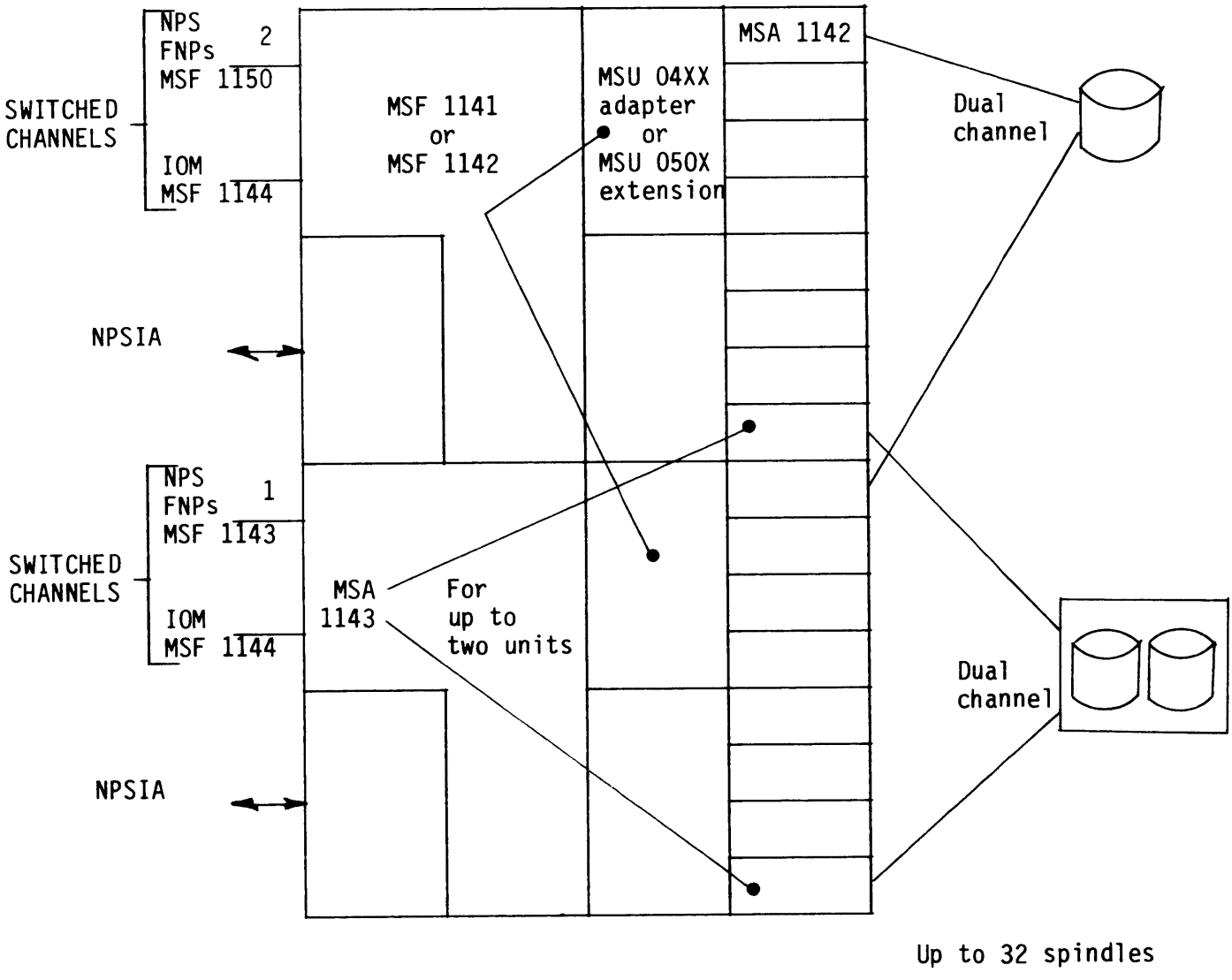
- MSU 0500/0501 Only

M S P 0 6 1 1			
MSU 050X	MSA 1141 Device Addressing	IOM Switched Channel	FNP SW Channel
1 - 2	1	MSF 1144	MSF 1143
3 - 4	2		
5 - 6	3		
7 - 8	4		

- Mix MSU 04XX and MSU 050X

MSP 0611 TOTAL NUMBER OF SPINDLES = 16						
MSU 0451A	MSU 050X X 2 spindles	MSF 1140 MSU 04XX adapter	MSA 1140 MSU 04XX addressing	MSA 1141 MSU 050X addressing	MSF 1144 IOM Switch Channel	MSF 1143 FNP Switch channel
1 - 4		1	1		U P T O 1 O P T I O N A L	U P T O 1 O P T I O N A L
5 - 8		1	2			
9 - 12		1	3			
13 - 16		1	4			
	1 - 2			1		
	3 - 4			2		
	5 - 6			3		
	7 - 8			4		

- MSP 0612


NPS
FNPs 2
MSF 1150
SWITCHED CHANNELS
IOM
MSF 1144
MSF 1141
or
MSF 1142
MSU 04XX
adapter
or
MSU 050X
extension
MSA 1142
Dual channel
NPSIA
NPS
FNPs 1
MSF 1143
SWITCHED CHANNELS
IOM
MSF 1144
MSA
1143
For
up to
two units
Dual channel
NPSIA
Up to 32 spindles

- MSP 0612

MSU 0500/MSU0501 only

MSU 050X	MSF 1142 MSU 050X Device Expansion	MSA 1143 MSU 050X Channel Addressing	MSF 1143 First NPS-FNPs SW Channel	MSF 1150 Second NPS-FNPs SW Channel	MSF 1144 Switch IOM Channel
1 - 2		1			
3 - 4		2	ONLY	ONLY	ONLY
5 - 6		3			
7 - 8		4	1	1	1
9 - 10	1	5	OPTIONAL	OPTIONAL	OPTIONAL
11 - 12	1	6			
13 - 14	1	7			
15 - 16	1	8			

Note: On each MSU 050X, the dual access (MSF 0011) is required.

- MSU 04XX ONLY

M S P 0 6 1 2					
MSU 04XX	MSF 1141 MSU 04XX Device Adpapter	MSA 1142 MSU 04XX Channel Addressing	MSF 1143 First NPS-FNPs SW Channel	MSF 1150 Second NPS-FNPs SW Channel	MSF 1144 Switch IOM Channel
1 - 4	1	1	Only	Only	Only
5 - 8	1	2	1	1	1
9 - 12	1	3	Optional	Optional	Optional
13 - 16		4			

Note: on each MSU 0451, the dual access (MSF 0006) is required.

- Mix MSU 04XX and MSU 05OX

MSP 0612										
MSU 0451	MSF 0006 MSU 0451 Dual Access	MSU 050X	MSF 0011 MSU 050X Dual Access	MSF 1141 MSU 04XX Channel Adapter	MSF 1142 MSU 050X Expansion Adapter	MSA 1142 add for MSU 04XX	MSA 1143 add for MSU 050X	MSF 1143	MSF 1150	MSF 1144
1 - 4	1 - 4	1 - 2	1 - 2	1		1	1			
		3 - 4	3 - 4	1		1	2			
		5 - 6	5 - 6	1		1	3			
		7 - 8	7 - 8	1		1	4			
5 - 8	5 - 8	1 - 2	1 - 2	1		2	1	UP	UP	UP
		3 - 4	3 - 4	1		2	2	TO	TO	TO
		5 - 6	5 - 6	1		2	3			
		7 - 8	7 - 8	1		2	4	ONE	ONE	TWO
9 - 12	9 - 12	1 - 2	1 - 2	1	1	3	1	OPTIONAL	OPTIONAL	
		3 - 4	3 - 4	1	1	3	2			
		5 - 6	5 - 6	1	1	3	3			
		7 - 8	7 - 8	1	1	3	4			
13 - 16	13 - 16	1 - 2	1 - 2	1	1	4	1			
		3 - 4	3 - 4	1	1	4	2			
		5 - 6	5 - 6	1	1	4	3			
		7 - 8	7 - 8	1	1	4	4			

3.1.4.2 Mass storage devices

. Our disk offering on DPS 8 systems consists of two disk types and three models.

- Removable disks: MSU0451A
- Fixed disks: MSU0500/MSU0501

. These devices can be connected to the MSP0611 or MSP 0612 controllers.

. If the disk drives are to be connected to an MSP0612 (dual-simultaneous channel controller), a dual access option must be configured for each device.

The MI's for these options are:

- MSF0006: dual access option for MSU0451A
- MSF0011: dual access option for MSU0500/501

. It is possible to upgrade on-site an MSU0500 to an MSU0501.

The option to be ordered for this purpose is:

- MSK0501: MSU0500 to MSU0501 upgrade

One option has to ordered for each device to upgrade.

. The following table provides the characteristics of the three disk models.

. If 50 Hz power supply is to be used, the following MI's must be used to order the disk devices from Cil/Angers.

- MSU0451B
- MSU0500B
- MSU0501B

	MSU0451A	MSU0500	MSU0501
Formatted capacity in millions of characters — 6-bit	235	940	1648
Formatted capacity in millions of characters — 8-bit	206	704	1236
Formatted capacity in millions of characters — 9-bit	157	626	1101
Transfer rate in thousand characters per second — 6-bit	1075	1597	1597
Transfer rate in thousand characters per second — 8-bit	806	1198	1198
Transfer rate in thousand characters per second — 9-bit	717	1064	1064
Access time in milli-seconds — Average seek time	30	25	25
Access time in milli-seconds — Average latency	8.5	8.3	8.3
Number of logical devices	1	4	4
Number of spindles per device	1	2	2
Number of recording surfaces per spindle	19	19	20
Number of tracks per recording surface	815	1630	1686
Number of read/write heads per surface	1	2	2
Number of sectors per track	40	40	8 physical to 64 physical
Logical sector size (36-bit words)	64	64	64
Physical sector size (36-bit words)	64	64	512
Density in BPI	4040	6436	6436
First supporting software release GCOS III	SR2H	SR4JS1	SR4JS2
First supporting software release GCOS 8	SR1000	SR1000	SR2000

3.1.5 MAGNETIC TAPE SUBSYSTEMS

3.1.5.1 Introduction

There are two types of Magnetic Tape processors:

- Integrated in the central cabinet (for ELS only)
- Free standing for ELS, DPS-E and DPS 88

These MTPs are based on the same logic and provide enhanced data recovery facilities.

It controls all existing handlers MTU 0400/0500/0600 and MTU 043X/53X family.

3.1.5.2 Product Description

MTPs, which are microprogrammed processors, have the capability to support:

9-track 6250/1600 bpi tapes

9-track 1600/800 bpi tapes

7-track 800/556 bpi tapes

. MTPs provide basic support of up to 8 tape units - in addition when equipped with the dual channel option, MTP 0611 supports up to 16 tape units in any mix.

The standard functions provided by the MTP 0611 are the following:

- support of up to 8 tape units
- automatic error recovery
- error logging
- standard end-of-file mark generation
- connection to the IOM high-speed PSIA channel.

To provide high level of data integrity, MTPs use various techniques for error detection and correction.

In NRZI, a system using cyclic redundancy checking is incorporated in densities up to 800 bpi to identify errors, which in PE (1600 bpi) mode dynamic detection and correction is provided to overcome all single bit errors. Error detection and correction techniques employed in GCR (6250 bpi) enable all single and double bit errors to be identified and corrected with no operator intervention.

Magnetic tape units utilizing either seven or nine track tapes cn be intermixed on the same MTP 0611, but only two 7 track units are supported.

When the dual simultaneous channel is installed in the MTP 0611, it is considered from a configuring point of view, as another MTP requiring its own set of addressing and functionality options. Whatever options being configured on the MTP must be duplicated on the dual simultaneous channel option.

3.1.5.1.1 Physical description

- The MTP 0611 is housed in the same LP designed cabinet as the DPS 8 central and MSP.

  The cabinet includes its own power supply.

	CABINET SIZE			WEIGHT	POWER SUPPLY			COOLING
	H	W	D		VOLTAGE	FREQ	POWER	
MTP0611	73 in 185 cm	40.5 in 103 cm	32.7 in 83 cm	1015 lb 461 kb	208/120 V 3 PH	60/50	2.3 KVA 2.1 KW	7580 BTU

- The integrated MTP 8001 is housed in the IOM ELS cabinet.

3.1.5.1.2 Marketing identifiers

MTP 0611 Magnetic tape processor with control adapter to support up to eight tape units

MTP 08001 Integrated Magnetic tape processor for ELS, only with control adapter to support up to eight tape units.

MTF 1151 Dual simultaneous channel for MSP 0611 only to support a second set of up to eight magnetic tape units. Maximum units connected when MTF 1151 is installed equals sixteen. With this option installed, the MTP 0611 becomes a dual-channel controller. It supports two high-speed PSIA channels, using crossbar links permitting the following simultaneities:

- Read/read
- Read/write
- Write/write

When the MTF 1151 is installed, all density options and following code translation options must be doubled.

It is recommended to order this at the same time as the MTP 0611, but if required, it may be installed on site.

In case of a problem with one of the channels, it may be invalidated by a DCAN command, and all tape units remain accessible through the other channel.

MTF 1159 Nine track NRZI/PE (800/1600 bpi) capability feature (one for each MTP 0611 and MTF 1151).

MTF 1160 Nine track PE/GCR (1600/6250 bpi) capability feature (one for each MTP 0611 and MTF 1151).

At least one feature MTF 1159, or MTF 1160 is mandatory.

MTF 1158 Seven track NRZI (556/800 bpi) capability feature (one for each MTP 0611 and MTF 1151). MTF 1159 is prerequisite.

MTF 1152 Non-simultaneous switched IOM channel. One for each MTP 0611 and MTF 1151.

MTA 1152 Magnetic tape addressing capability, supports up to four units.

MTF 1125 Series 200/2000 to level 66 tape compatibility feature (one for each MTP 0611 and MTF 1151).

MTF 1155 ASCII code translator
(One for each MTP 0611 and MTF 1151)

MTF 1156 EBCDIC code translator
(one for each MTP 0611 and MTF 1151)

MTF 1157 EBCDIC to ASCII code translator
(one for each MTP 0611 and MTF 1151)

PSS 8001 Capacitor ride through option for MSP 0611 only. As for central system and disk controllers, the capacitor ride through option (one per MTP 0611) is mandatory in the case where the tape controller is operated on 50 Hz power and no motor generator or UPS is used.

3.1.5.1.3 Configurations

Configuration of the MTPs are straight forward if the following plan is followed.

1 - Define type and quantity of units to be used (MTU 043X/53X/500/600).

2 - Configure dual channel on MTP 0611, if required and permitted (MTF 1151)

3 - Configure switched channel, if required
MTF 1152 maximum 1 for MTP 0611/8001
and 1 for MTF 1151.

4 - Configure magnetic tape unit addressing option MTA 1152 one for four MTU.

5 - Configure functionality options MTF 1158/59/60.

6 - configure translator options (MTF 1125/55/56/57).

7 - Recheck configuration.

3.1.5.1.4 Software support

MTP 0611/8001 are supported by the following software releases:

GCOS 3	4JS3
GCOS 8	SR2000
Multics	MR9

3.1.5.2 Magnetic tape units

. The following table provides a summary of the various tape units which may be ordered for a DPS 8 system to be connected to the MTP 0611 controller.

M.I.	NUMBER OF TRACKS	RECORDING MODES SUPPORTED	DENSITIES SUPPORTED	SPEED IN IPS	THROUGHPUT IN KBS
MTU0438	9	PE/GCR	1600/6250	75	468
MTU0538	9	PE/GCR	1600/6250	125	780

. If 50 Hz power supply is to be used, the following MI's must be used to order the tape drives from Cil/Angers:

MTU 0438B

MTU 0538B

. MTU0438

- 75 ips, 468 KBS tape unit
- This tape unit includes the features for support of GCR/6250 BPI and PE/1600 BPI tapes.
- The following options apply to the basic tape unit:

  MTK0442: 75 ips to 125 ips upgrade kit (MTU0436 to MTU0536)

  MTF0062: High altitude blower.

. MTU0538

- 125 ips, 780 KBS tape unit
- This tape unit includes the features for support of GCR/6250 BPI and PE/1600 BPI tapes.
- The following options applies to the basic tape unit:

  MTF0082: High altitude blower

3.1.6 UNIT RECORD SUBSYSTEM

UNIT RECORD CONTROLLER

3.1.6.1 Introduction

The Embedded URP (EURP) is the unique unit record controller available in our catalogue.

This controller, located, in the IOM of ELS or DPS-E, uses one or two IOM channel function slots and controls:

- New printers PRU 1101 or 1501 using PDSI (Serial Interface) PRU 1601, and card equipments using DA1 interface.

3.1.6.1.1 Product Description

EMBEDDED UNIT RECORD CONTROLLERS

This family is composed of three new controllers which provide support for the new printers and existing card readers, punches and printers.

The new controller consists of either two boards (mixed device types) or one board (single device type). These boards fit directly into the IOM with the device cables connecting to the free edge of the board.

This controller with one or two boards, provides the same fonctions as the old controller URP0600 which was composed of more than 10 boards; power supplies; control and maintenance panels, blowers, cabinets, plus three boards in the IOM.

The new controllers are essentially firmware driven microprocessors with the firmware installed in pluggable EPROM's. The new controllers also include a data buffer for temporary storage of data and command parameters together with the necessary IOM interface control logic.

A peripheral device serial interface (PDSI) is provided for the new printers and a device adapter interface (DAI) for existing card readers, punches and printers. These new controllers include all necessary addressing features for connection of the defined unit record devices.

URP8001 Supports a maximum of two PRU1101 or 1501 plus a maximum of two card devices from the following list:

CRU0501

CRU1050

PCU0120

URP8002 Supports a maximum of two card devices from the following list:

CRU0501

CRU1050

PCU0120

URP8004 Supports a maximum of two printers PRU1101 / 1501 or PRU 1200/160X/1042

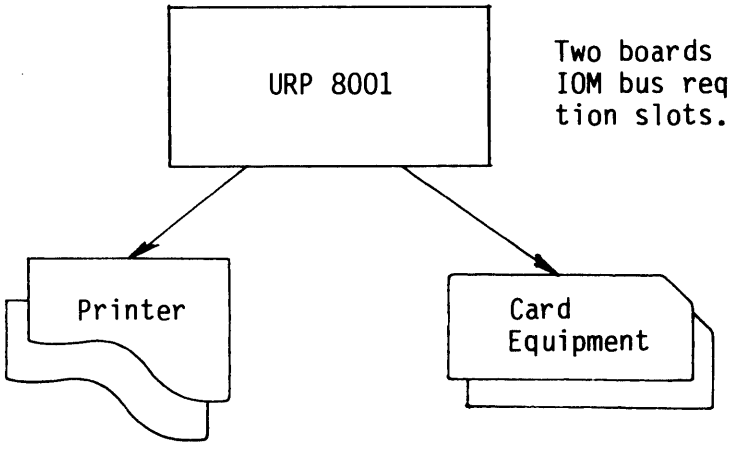
. The URP8001/2/4 do not require any addressets (URA) for peripheral connection.

3.1.6.1.3 Configuration

Configuration rules of the new controller are few and simple.

The new controllers (URP 8001/2/4) do not require addressing features as did the old style unit record processors and as mentioned above, no floor space has to be allocated to them.

URP 8001

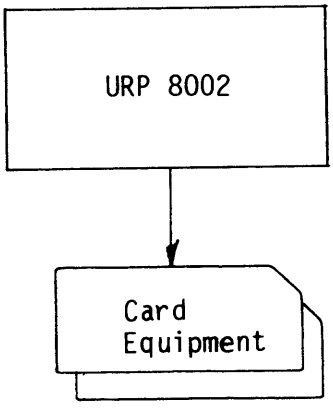


Two boards included in the IOM bus require two function slots.

Max of two any mix of PRU 1101/1501

Max of two any mix of CRU 0501/1050 or PCU 0120

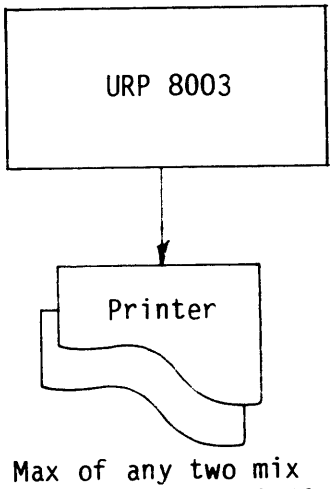
URP 8002



One board plugged in the IOM I/O bus

Max of any two mix of
CRU 0501/1050 or PCU0120

URP 8004



One board fitted in the IOM I/O bus

Max of any two mix
of PRU1101, PRU1501,
PRU1042, 1200 or 160X.

3.1.6.1.4 Software

. The URP 8001/8002/8004 are supported by the following software releases:

GCOS 3 release 4JS3

GCOS 8 release SR2000

MULTICS release MR10

3.1.6.2 Peripherals

Printers

Introduction

Printers available in the DPS 8 catalog are the two new printer models: PRU1101 and PRU1501.

3.1.6.2.1 Description

These PRU's are new design printers from CII-HB Belfort with rated speeds of 1180 and 1540 lines per minute using a 48 character belt. Should a 64 character belt be used, these rated speeds decrease to 900 and 1200 respectively. A 96 character belt reduces these speeds to 686 and 940 respectively.

The printers are supplied with a standard 136 column print positions. No optional 160 column print position options are available.

As the PR71, the new PRU's are belt printers. One belt is supplied free at the time of placing the printer order. It is necessary to specify the belt type required as "no charge" item.

Belts for these new printers are classified as consumable not being covered by the maintenance contract.

Replacement belts must be obtained from customer spares department.

The new printers use a 2 X 50 inch re-inkable replaceable ribbon. Each ribbon is scheduled to provide 40 million lines before replacement. Replacement ribbons and ink bottles are available from customer spares department.

A powered stacker is standard with both models of the new printer.

Device parameters such as number of lines per inch, vertical form positioning, slewing to top of page and specified intermediate form positions are programmable for automatic execution.

Checking features to ensure detection of both paper feed and data transfer errors are included in the new printers.

Clearly illustrated operating instructions next to all controls and indicators together with print test facilities make these printers extremely user friendly.

Note: Belts used on the PRU 1042/1200/1600/1601 cannot not be used on the new printers and vice-versa. This is a technical consideration, marketing restriction.

Belts used on the new PRU are OCR-B font style.

The PRU 1101/1501 ribbon is housed in a cartridge with integrated reinking. This cartridge is changeable and refillable by the operator.

The standard ribbon exchange kit includes:

1 cartridge
10 ribbons
10 ink bottles
20 gloves.

This kit is exclusively sold by CII-HB supply division (DIPI).

3.1.6.2.2 Physical specification

Both new printers have the same physical characteristics, the different performance level being an internal consideration.

	CABINET SIZE			WEIGHT	POWER SUPPLY			COOLING
	H	W	D		VOLTAGE	FREQ	POWER	
PRINTERS	39.5 (100 cm)	36.0 (92 cm)	26.0 (66 cm)	375 lbs 170 kg	220 Volt 208 Volt	50/60	0.5 KW	1.7 BTU
STACKERS	32 in 80 cm	29 in 73 cm	26 in 40 cm	86 lbs 39 kg				

3.1.6.2.4 Technical specification

PRINT SPEED

- BELT	PRU1101	PRU1501
- 48 char.	1180	1540
- 64 char.	900	1200
- 96 char.	686	940
PRINT POSITIONS	136	136
HORIZONTAL PITCH	10 char/inch	10 char/inch
VERTICAL PITCH	6 or 8 l/inch	6 or 8 l/inch
PAPER SKIP SPEED	26 inch/sec	44 inch/sec
PAPER STACKER	STANDARD	STANDARD
STATIC ELIMINATOR	OPTIONAL	OPTIONAL

STATIONARY: BOTH PRINTERS

NUMBER OF COPIES:	Original plus 5 carbons
SHEET LENGTH:	3 to 11 inches (7.7 to 28 cm)
SHEET WIDTH:	4 to 16 inches (10 to 40 cm)
WEIGHT (per m^2):	56 gr. to 160 gr.
THICKNESS:	Should not exceed 0.5 mm 0.020 inches

Note: Distance between left edge of paper and center line of column N°. 1 is 2.75" as a maximum (69.8 mm).

Distance between right edge of paper and center line of device col 136 is 3.75" as a maximum (95 mm).

3.1.6.2.5 Marketing identifiers

PRU1101 (1) Impact line printer, 1180 lpm with 48 chr belt, 900 lpm with 64 chr belt. Includes one belt (which must be specified at printer order time), one ribbon/ink mechanism and one paper stacker.

PRU1501 (1) High speed impact line printer, 1540 lpm with 48 chr belt, 1200 lpm with a 64 chr belt. Includes one belt (which must be specified at the printer order time), one ribbon/ink mechanism and one paper stacker.

(1) This MI must be completed with A or B depending on :

A = 60Hz, B = 50Hz.

. PRINTER OPTIONS

* PRK0901: Upgrade kit from PRU1101 to PRU1501

. PRINT BELTS

As mentioned above, the PRU1101 and PRU1501 include one print belt, to be chosen from the following list. Additional or replacement print belts are to be ordered as supplies, from your local supplies catalog.

PRB3500	63 char. code G, OCR-B
PRB3501	63 char. code I, OCR-B
PRB3503	63 char. code G, Spain, Mexico, Argentina, OCR-B
PRB3504	63 char. code G, Sweden, Finland, OCR-B
PRB3505	63 char. code G, Denmark, Norway, OCR-B
PRB3506	63 char. code I, Sweden, Finland, OCR-B
PRB3507	63 char. code I, Spain, Mexico, Argentina, OCR-B
PRB3508	63 char. code G, Brazil, Portugal, OCR-B
PRB3509	63 char. code I, Denmark, Norway, OCR-B
PRB3510	63 char. code Brazil, Portugal, OCR-B
PRB3513	63 char. standard ASCII, OCR-B
PRB3518	63 char. code DIN, Germany, OCR-B
PRB3521	63 char. code I, Germnay, OCR-B
PRB3524	63 char. numeric OCR-A, alpha OCR-B
PRB3546	63 char. Greece, OCR-B
PRB3559	63 char. GULF-specific (French), OCR-B
PRB3600	94 char. full ASCII U/L case, OCR-B
PRB3603	94 char. code DIN Germnay, OCR-B
PRB3746	73 char. code Greco-latin, OCR-B

3.1.6.2 Card readers

- The card readers available for DPS 8 systems is :

  CRU0501A: 500 cpm reader

- An addresset option must be ordered :

  URA0056: Addresset for CRU0501A

- The CRU0501 can be placed on a table, but a pedestal is available as an on option if this is preferred:

  CRF0008: Pedestal for CRU0501A

- The 50 Hz versions of the card readers must be ordered from Cil/Angers using the following MI :

  CRU0501B

3.1.7 PERIPHERAL SWITCHES

The PSU 8001 is contained in a standard Mini 6 Cabinet which will complement the overall appearance of the central system. In addition to the capability to switch peripheral processors, and peripheral processors between I/O processors, the new peripheral switch can switch Datanets between I/O processors.

The detailed description section lists the various hardware components and their functions. In addition some typical configurations are included to to assist you in configuring the new peripheral Switch Subsystems.

DETAILED DESCRIPTION

This section lists the various components and their functions.
The following is a list of manual peripheral switch subsystem marketing identifiers (MI) and their functions.

MI	Description	Remarks
PSU8001	Manual Peripheral Switch Console. Does not include an I/O channel. Includes one 8-line switch unit, switch control unit, power supply and cabinet.	The PSU 8001 manual switch Console can be configured with up to 3 additional 8-line switch units (PSF8000) for a maximum capability of 32 lines positions. PSU 8001 input voltage is 60 or 50 HZ Use suffix "B" to specify 50 HZ : PSU 8001 (60 HZ) PSU 8001 B (50 HZ)

The following interfaces are supported :

PSI - Peripheral Controllers to I/O Processor (2 lines)

DAI - Card devices and PRU 1200/1600 to controllers (2 lines/ device)

DLI - Disk and tape devices to controllers (2 lines/spindle or 4 lines/spindle dual access)

PDSI - PRU 1101/1501 to controllers (1 line/printer)

DIA - Datanets to I/O processor (3 lines/Datanet)

The PSI, DAI, and DLI interfaces each require 2 line positions of an 8-line switch unit. The PDSI interface requires 1 line position of an 8-line switch unit. The DIA interface requires 3 line positions of an 8-line switch unit.

MI	DESCRIPTION	REMARKS
PSF800(	Switch Capacity Expansion for PSU8001 Includes one 8-line switch unit maximum of 3 per PSU 8001	No additional power facilities required ; powered from switch control unit
PSF801:	PSI/DAI/DLI Peripheral Switch Adapter. Does not include I/O Channel	One adapter required per interface being switched. Adapter type must match interface type on each line. Consumes 2 line position
PSF801:	DIA Peripheral Switch Adapter. Does not include I/O Channel	One adapter required per interface being switched. Adapter type must match interface type on each line. Consumes 3 lines positions.
PSF801(	PDSI Peripheral Switch Adapter. Does not include I/O Channel	One adapter required per interface being switched. Adapter type must match interface type on each line. Consumes 1 line position.

FOR SWITCHING BETWEEN TWO PERIPHERAL CONTROLLERS

66/DPS or DPS8 Low Speed PSIA IOM	PSF8011 PLUS MXK 6005 are required
66/DPS or DPS8 high speed PSIA IOM	PSF8011 PLUS MXK 6006 are required
DPS88 CAU Peripheral sub syst attachment	PSQF8011 PLUS MXF 8801 are required if URP PSF 8011 PLUS MXF 8802 are required

FOR SWITCHING BETWEEN TWO DATANET

66/DPS or DPS8 IOM adapter	PSF8013 PLUS DCK 6005 are required
DPS88 CAU adapter	PSF8013 PLUS MXF 8803 are required

3.1.8 FRONT-END PROCESSORS

. This chapter is a duplication of part of Sales Aid N° 82.717/ DSA

. The chapter is in two parts:

- New orders DCP7121, DCP7122, DCP7123
- Add-ons on DCP7102, DCP7112, DCP7103, DCP7113

. There are three models of Front-End processors:

- Datanet: DCP 7121
- Datanet: DCP 7122
- Datanet: DCP 7123

. These Datanets are the standard front-end processor offering for the DPS 8 family.

DATANET 7102

MARKETING IDENTIFIER	DESCRIPTION	OBSERVATIONS
	BASIC SYSTEM	
DCP7121	- Process panel - Automatic control	- 24 line connector slots - Maximum 2 host couplers (same type)
	- 256K words of MOS EDAC memory - 1 30cps console - 1 512KB diskette	- Maximum memory size 512 Kwords - 1 cabinet - Maximum of 3 DCC 7103/7105/ 7106 or 1 of them plus 1 DCC 7104 (see Configurator User's Guide)
DCP7122	- Processor with full control panel - Automatic control	- 64 line connector slots - Maximum 2 host couplers (same type)
	- 256K words of MOS EDAC memory - 1 120 cps console - 1 512KB diskette	- Maximum memory size 768 Kwords - 1 cabinets - Maximum of 8 DCC 7103/7105 7106 or 4 DCC 7104 or a mix (see Configurator User's Guide)
DCP7123	- Processor with full control panel - Automatic control	- 128 line connector slots - Maximum 4 host couplers (same type)
	- 256K words of MOS EDAC memory - 1 120 cps console - 1 512 KB diskette	- 2 cabinets - Maximum of 14 DCC 7103/7105/ 7106 or 8 DCC 7104 or a mix (see Configurator User's Guide)

	OPTIONS	
	COUPLERS FOR CONNECTION TO HOST COMPUTER	
DCA 7103	- Coupler for DPS8 (66DPS-DPS8)	- Maximum of 2 per DATANET 7101/ 7102 - Maximum of 4 per DATANET 7103 - Excludes the DCA 7104
DCA 7104	- Coupler for DPS7 (64DPS-DPS7)	- Maximum of 2 per DATANET 7101/ 7102 - Maximum of 4 per DATANET 7103 - Excludes the DCA 7103
	COMMUNICATION LINE CONTROLLER	
DCC 7103	Multiline Controller	- Occupies 8 line connector slots - It can simultaneously support up to 4 line adapters for DCC7103 - Two of the following types of transmission procedure RCI, VIP, TMM, BSC, HDLC, Asynchronous, can be simultaneously installed on the line controller (see Configurator User's Guide)
DCC 7104	Asynchronous Multiline Controller (8 or 16 asyn. lines)	- Occupies 16 line connector slots - It can support up to two line adaptors for DCC 7104.
DCC 7105	Monoline Controller V35 HDLC up to 56Kbps with 30 feet cable TRANSPAC connector	- Occupies 8 line connector slots
DCC 7106	Monoline controller V35 HDLC up to 48Kbps with 30 feet cable INTERNATIONAL connector	- Occupies 8 line connector slots - It can be also used for TRANSPAC with DCK 7001.

	LINE ADAPTORS (for DCC 7103)	Maximum 4 per DCC 7103
DCF 7140	2 asynchronous line adapter up to 9600 bps, V24 with 30 feet cables	
DCF 7141	2 asynchronous line adapter up to 9600 bps, V24 with 50 feet cables	
DCF 7142	2 synchronous line adapter up to 9600 bps, V24 with 30 feet cables	
DCF 7143	2 synchronous line adapter up to 9600 bps, V24 with 50 feet cables	
DCF 7144	1 HDLC line adapter up to 19200 bps, V24 with 30 feet cable	
DCF 7145	1 HDLC line adapter up to 19200 bps, V24 with 50 feet cable	
DCF 7146	1 synchronous or HDLC X21 line adapter up to 9600 bps, with 30 feet cable.	
DCF 7147	2 asychronous lines current loop adapter up to 600 bps with 25 feet cables	
	LINE ADAPTERS (for DCC 7104)	Maximum 2 per DCC 7104
DCF 7123	8 asynchronous line V24 adapter up to 2400 bps with 30 feet cables	
DCF 7124	8 asynchronous line V24 adapter up to 2400 bps with 50 feet cables	
DCF 7125	8 asynchronous line V11 adapter up to 2400 bps with 50 feet cables.	

DCE 7105	Performance extension	- Enables increase of performance of DN 7102 to bring it up to the DN 7103 level. - Maximum number of lines remains the same (64 lines) - Implies STS7113 software in place of STS7112
DCE 7106	Attached Processor	- Increase the power of a DN 7102 with DCE 7105 or a DN 7103 in terms of throughput - Implies STU 7113 module in addition to STS7113.
DCF 7132	Remote DN 7100 automatic-loader (through HDLC line)	- Allows DATANET to be loaded remotely.
DDK 7106	Upgrade from single to dual diskette (double sided)	- Only on DCP 7122 and DCP 7123
	MEMORY EXTENSION	
DCM 7121	- 256 KWords additional memory	- Extension from 256K to 512K
DCM 7122	- 256 KWords additional memory (second)	- Extension from 512K to 768K for DN7102/DN7103

DCP 7121

PROCESSOR TYPE 1
MDC 30 CPS CONSOLE & 512 KB DISKETTE
HOST COUPLER = 2
HOST COUPLER = 1
MLCP = 3 or AMLC = 1
MLCP = 2
MLCP = 1
Automatic Control ° Remote Loading
256 KW ° 512 KW

°RESERVED FOR

UP TO 24 LINES

RFU
POWER EXTENSION

PERFORMANCES EXTENSION
PROCESSOR TYPE 1
MDC 120 CPS CONSOLE & 512 KB DISKETTE (°)
HOST COUPLER = 2
HOST COUPLER = 1
MLCP = 8 or AMCL = 1
7
6 or AMLC = 2
5
4 or AMLC = 3
3
2 or AMLC = 4
1
Automatic control ° Remote Loading
768 KW
256 KW ° 512 KW
RFU

° RESERVED FOR
(°) SECOND DISKETTE OPTIONAL

UP TO 64 LINES

RFU
POWER EXTENSION

PROCESSOR
MDC 120 CPS CONSOLE & 512 KB DISKETTE (°)
HOST COUPLER = 4
HOST COUPLER = 3
HOST COUPLER = 2
HOST COUPLER = 1
MLCP = 14 or AMCL = 1
MLCP 13 or AMLC = 2
MLCP 12
MLCP 11 or AMLC = 3
MLCP 10
MLCP 9 or AMLC = 4
MLCP 8
MLCP 7 or AMLC = 5
MLCP 6
////
MLCP 5 or AMLC = 6
MLCP 4
MLCP 3 or AMLC = 7
MLCP 2
MLCP 1 or AMLC = 8
Automatic control ° Remote Loading
768 KW
256 KW ° 512 KW
RFU
RFU

° RESERVED FOR
(°) SECOND DISKETTE OPTIONAL

UP TO 128 LINES

HARDWARE CATALOGUE

ADD - ONS

ADD-ONS

. DCP 7112 is now out of the Catalogue and replaced by DCP 7122.
. All Marketing Identifiers are new for DCP 7122.
. Old Marketing Identifiers for DCP 7102 or DCP 7112 ADD-ONS are STILL in the catalog.

. DCP 7113 is now out of the Catalogue and replaced by DCP 7123.
. All Marketing Identifies are new for DCP 7123.
. Old Marketing Identifiers for DCP 7103 or DCP 7113 ADD-ONS are STILL in the catalog.

DATANET 7102	DCP7102 DCP7112
DATANET 7103	DCP7103 DCP7113

MARKETING IDENTIFIER	DESCRIPTION	OBSERVATIONS
	MEMORY EXTENSIONS	
DCM 7110	- 32 Kwords additional memory	Mandatory for DN 7102/DCP7102
DCM 7111	- 64 KW additional memory (first extension of each 128 KW step)	- Maximum of 2 per system (one is yet included in DCP 7112) - Occupies 1 slot - Extension for upgrade: from 256 KW to 320 KW
DCM 7112	- 64 KW additional memory (second extension of each 128 KW step).	- Implies DCM 7111 - Extension for upgrade: from 192 KW to 256 KW from 320 KW to 384 KW

	OPTIONS	
	COUPLERS FOR CONNECTION TO HOST COMPUTER	
DCA 7101	- Coupler for Level 66 connection (66DPS-DPS8)	- Maximum of 2 per DCP 7102 or DCP 7112 Occupies 1 slot - Excludes the DCA 7102
DCA 7102	- Coupler for Level 64 connection (64DPS-DPS7)	- Maximum of 2 per DCP7102 or DCP 7112 - Occupies 1 slot - Excludes the DCA 7101

	EXTENSIONS	
DCE 7102	Extension of 4 slots on DATANET 7102	- With DCP 7112, the number of available slots become 9
DCE 7104	Performance extension on DATANET 7102	- Enables increase of performance on DN 7102 to bring it up to the DN 7103 level - Occupies 1 slot - Maximum number of lines remains the same (48 lines)
DCF 7130	DN 7102 automatic - loader from diskette and/or through host channel)	- Implies STU 7113 software
DCF 7131	Remote DN 7100 automatic-loader (through HDLC line)	- Implies STU 7112 software - Implies DCF 7130 hardware - Allows a Datanet to be loaded remotely

	COMMUNICATION LINE CONTROLLER	
DCC 7101	Multiline Controller	- Maximum of 9 DCC per DN 7102 (according to the number of options, lines and of DCC 7102) - Occupies 1 slot - It can simultaneously support several types of line adapters. - Two of the following types of transmission procedure: VIP, TMM, BSC, HDLC, Asychronous, can be simultaneously installed on the line controller. - For more than 5 DCC 7101 (or DCC 7102), if options or extensions are ordered, the number of available slots is to be verified. - A maximum of 4 DCF 710X adapters per controller.
DCC 7102	Asynchronous Multiline Controller (8 or 16 asyn. lines)	- Maximum of 6 DCC 7102 per DN 7102 (according to the number of options, lines and DCC 7101) - Occupies 1 slot - It supports only asynchronous adapters DCF 7121 and/or DCF 7122. - For more than 5 DCC 7101 (or DCC 7102), if options or extensions are ordered, the number of available slots is to be verified. - A maximum of 2 DCF 712X adapters per controller.

MARKETING IDENTIFIER	DESCRIPTION	OBSERVATIONS
	MEMORY EXTENSIONS	
DCM 7111	64 KW additional memory (first extension of each 128 KW step)	- Maximum of 2 per system Occupies 1 slot - Extension for upgrade: from 256 KW to 320 KW from 384 KW to 448 KW
DCM 7112	64 KW additional memory (second extension of each 128 KW step).	- Implies DCM 7111 - Extension for upgrade: from 320 KW to 384 KW from 448 KW to 512 KW

	OPTIONS	
	COUPLERS FOR CONNECTION TO HOST COMPUTERS	
DCA 7101	Coupler for connection to Level 66 (66DPS/DPS8)	- Maximum of 4 per DN 7103 - Occupies 1 slot - Excludes the DCA 7102
DCA 7102	Coupler for connection to Level 64 (64DPS/DPS7)	- Maximum of 4 per DN 7103 - Occupies 1 slot - Excludes the DCA 7101

	EXTENSIONS	
DCE 7103	Extension of 4 slots on DCP 7103	- only one per DN 7103/ DCP 7103 - With DCP7103, the number of available slots becomes 12.
DCE 7113	Extension of 9 slots on DCP 7113	- Maximum of 1 per system - With DCP 7113, the number of available slots becomes 23.
DCF 7131	Remote DN 7100 automatic-loader (Through HDLC line)	- Allows a Datanet to be loaded remotely.

	COMMUNICATION LINE CONTROLLER	
DCC 7101	Multiline Controller	- Maximum of 19 DCC 7101 per DN 7103 (according to the number of options, lines, and of DCC 7102) - It can simultaneously support several types of line adapters. - Two of the following transmission procedure: VIP, TMM, BSC, HDLC, Asynchronous, can be installed simultaneously on the line controller. - For more than 14 DCC 7101 (or DCC 7102), if options or extensions are ordered, the number of available slots is to be verified. - A maximum of 4 DCF 710X adapters per controller.
DCC 7102	Asynchronous Multiline Controller	- Maximum of 16 DCC 7102 per DN 7103 (according to the number of options, lines and of DCC 7101). - It supports only asynchronous adapters DCF 7121 and/or DCF 7122. - For more than 14 DCC 7101 (or DCC 7102), if options or extensions are ordered, the number of available slots is to be verified. - A maximum of 2 DCF 712X adapters per controller.

DCF 710X	LINE ADAPTERS (for DCC 7101)	
DCF 7101	2 asynchronous line adapter up to 9600 bps, V24	- Occupies a DCC 7101 position
DCF 7102	2 character synchronous line adapter up to 9600 bps, V24	- Occupies a DCC 7101 position
DCF 7104	1 HDLC line adapter up to 19200 bps, V24	- Occupies a DCC 7101 position
DCF 7105	1 HDLC line adapter up to 56000 bps, V35, French standard (1)	- Occupies 2 DCC 7101 position
DCF 7107	1 character synchronous line or HDLC X21 adapter up to 9600 bps	- Occupies a DCC 7101 position
DCF 7109	1 HDLC line adapter up to 56000 bps, V35, International Standard (1)	- Occupies 2 DCC 7101 position
DCF 7108	2 asynchronous lines current loop adapter up to 9600 bps	- Occupies a DCC 7101 position
DCF 712X	LINE ADAPTERS (for DCC 7102)	- Occupies a DCC 7102 position
DCF 7121	8 asynchronous lines V 24 adapter	- Occupies a DCC 7102 position
DCF 7122	8 asynchronous lines V 11 adapter	- Occupies a DCC 7102 position
	(1) REMARK: For FRANCE, two cases: - Access to TRANSPAC at 48 Kbps or to broad band lines: DCF 7105 - Use of SPECTRON Switch: DCF 7109 and, if it is necesary, a cable adapter from International standard to French standard.	

DDK 7102	Upgrade Kit from single to dual diskette (double sided)	- Implies DDS 7103
DDK 7103	Upgrade kit from single (single DDS 7101 of Rel.A) to single diskette (double sided)	
DDK 7104	Upgrade kit from single (single sided DDS 7101 of Rel. A) to dual diskette (double sided)	
DDK 7105	Upgrade kit from dual (single sided DDS 7102 to Rel. A) to dual diskette (double sided)	

3.1.9.1

CATEGORY	MARKETING IDENTIFIER	DESCRIPTION
ELS CENTRAL SYSTEMS	CPS8XYZ	DPS 8/MN BASIC CENTRAL SYSTEM, including 1 CPU with DPU, one 5 port SCU, one 20 channel function slot IOM, 4 mega bytes of memory and 32 kilo bytes of cache memory. DPS 8-ELS may be configured with up to 16 MB if single processor or 32 MB if dual processor.
	CPS8139	DPS 8/47 Basic Central System CPU performance = 1 (approx. 750 Kops)
	CPS8141	DPS 8/49 Basic Central System CPU performane = 1.46 (approx. 1050 Kops)
ELS CENTRAL SYSTEM REDUNDANCY OPTION	CPF 8132	DPS 8/49 full redundancy option applicable to the basic central system CPS8141. Includes 1 CPU with one DPU, 1 IOM, 1 SCU, 4 MB of central memory and crossbar features to interconnect the various elements of the central system, thus making it a fully redundant system.

CATEGORY	MARKETING IDENTIFIER	DESCRIPTION
ADDITIONAL CPU	CPU8131	Additional 8/49 CPU applicable on CPS8141. Up to 3 CPU8131 authorised.
ADDITIONAL SCU	MXC8003	Five port SCU. Applies to DPS 8/49 only (CPS8141). Up to 1 additional MXC8003 authorised.
ADDITIONAL IOM	MXU8003	20 channel function slot IOM. Applies to DPS 8/49 only (CPS8141). 1 additional MXU8003 authorised.
PERFORMANCE UPGRADE	CPK8337	Performance upgrade from DPS 8/47 to DPS 8/49 for the basic 8/47 central system (CPS8139).
PORT EXTENSION ON 5 PORTS SCU MXK8009	MXK8009	Upgrade 5 port SCU to 8 port SCU. This option is required to install on DPS 8/49 (CPS8141) a third CPU.
ADDITIONAL MEMORY	CMM8002	2 MB additional memory. Applies to DPS 8/47 and 8/49.
	CMM8003	4 MB additional memory. Applies to DPS 8/47 and 8/49.

3.1.9.2

CATEGORY	MARKETING IDENTIFIER	DESCRIPTION
DPS-E CENTRAL SYSTEMS	CPS 82XY	DPS 8/NM basic central system, including 1 CPU, 1 SCU, 1 IOM, 4 Mega bytes of central memory shared in two buckets and 32 Kilo bytes of cache memory. A DPS 8 system may be configured with up to 8 Mb of central memory under GCOS III and 64 Mb under GCOS 8. A Diagnostic Processor Unit (DPU) is delivered with each DPS 8 system, but remains the property of CII HONEYWELL BULL.
	CPS 8257	DPS 8/52 Basic Central System CPU performance = 1.46 (approx. 1045 KOPS)
	CPS 8267	DPS 8/52 Basic Central System CPU performance = 2.0 (approx. 1430 KOPS)
	CPS 8277	DPS 8/70 Basic Central System CPU performance = 2.6 (approx. 1870 KOPS)

CATEGORY	MARKETING IDENTIFIER	DESCRIPTION
DPS-E CENTRAL SYSTEM REDUNDANCY OPTIONS	CPF 82XZ	DPS 8/NM Full Redundancy option, applicable to the basic central systems, indluding 1 CPU, 1 SCU, 1 IOM, 4 MB of central memory shared in two buckets, 32 MB of cache memory, and crossbar features to interconnect the various elements of the central system, thus making it a fully redundant system.
	CPF 8258	DPS 8/52 Full Redundancy option. Applies to CPS 8257.
	CPF 8268	DPS 8/62 Full Redundancy option. Applies to CPS 8267.
ADDITIONAL CPU	CPU 8189	Additional 8/70 CPU. Applies to CPS 8277. Up to 3 CPU 8189 authorized.

CATEGORY	MARKETING IDENTIFIER	DESCRIPTION
ADDITIONAL SCU	MXU 8002	Additional SCU. Applies to redundant 8/52 and 8/62 systems as well as 8/70 systems. The above DPS 8 systems may be configured with up to 4 SCU's. Single-processor 8/52 and 62 systems are limited to 1 SCU (included in the CPS).
ADDITIONAL IOM	MXC 8002	Additional IOM. Applies to redundant 8/52 and 8/62 systems as well as to 8/70 systems. The above DPS 8 systems may be configured with up to 4 IOM's. Single-processor 8/52 and 8/62 systems are limited to 1 IOM (included in the CPS)
CENTRAL SYSTEM OPTION	PSS 8000	Capacitor Ride through option (1 per CPU, SCU, IOM).

CATEGORY	MARKETING IDENTIFIER	DESCRIPTION
ADDITIONAL MEMORY	CMM 8021	2 Mbytes additional memory. Applies to mono-processor 8/52, 62, 70 systems, and to multi-processor DPS 8 systems.
	CMM 8022	4 Mbytes additional memory. Applies to redundant 8/52, 62 systems and to 4 Mb 8/70 systems.
	CMM 8023	8 Mbytes additional memory. Applies to 8 Mbyte 8/52, 60 and 70 systems. Memory sizes above 8 Mb are supported under GCOS 8 only.

CATEGORY	MARKETING IDENTIFIER	DESCRIPTION
PERFORMANCE UPGRADES	CPK 8257	Performance upgrade from 8/52 to 8/62 Level for the basic 8/52 central system (CP 8257 or CPS 8245 + CPK 8245).
	CPK 8258	Performance upgrade from 8/52 to 8/62 level for the 8/52 redundancy option (CPF 8258 or CPF 8245 + CPK 8246).
	CPK 8267	Performance upgrade from 8/62 to 8/70 level for the basic 8/62 central system (CPS 8267 or CPS 8257 + CPK 8257) (or CPS 8245 + CPK 8245 + CPK 8257).
	CPK 8268	Performance upgrade from 8/62 to 8/70 level for the 8/62 redundancy option (CPF 8267 or CPF 8257 + CPK 8258 or CPF 8246 + CPK 8246 + CPK 8258).

CATEGORY	MARKETING IDENTIFIER	DESCRIPTION
SYSTEM CONSOLE	CSU 6601	Mandatory (at least 1) DPS 8 system console, including: - 1 Keyboard/display (12") - 1 120 CPS serial printer.
	CSF 6601	Mandatory table for CSU 6601, including the "operator pod", with Initialize/Boot/Emergency Power off buttons and the processor speed indicators.
	CSF 6607	Pedestal for serial printer, and keyboard/display.
	CSU 6602	Auxiliary console, i.e. additional 120 cps serial printer. CSF 6607 recommended.

CATEGORY	MARKETING IDENTIFIER	DESCRIPTION
SYSTEM CONSOLE	CSF 6602	Additional keyboard/display attachment.
	CSF 6603	Additional keyboard/display. CSF 6620 required. DKF 7201 recommended.
	CSF 6604	23" monitor display, which reproduces information appearing on the CSU 6601 or CSF 6603 displays.
	CSF 6605	Ceiling mount for 23" monitor display.
	CSF 6606	Extended System Control Feature, which is a security/availability feature i.e. a switch to be applied between the CSU 6601 and a remote terminal or a CSU 6602 or a CSF 6603.

CATEGORY	MARKETING IDENTIFIER	DESCRIPTION
FREE STANDING MASS STORAGE PROCESSORS	MSP 0611	Single channel disk controller; supports a maximum of 16 MSU 0451A or 8 MSU 00500/501 disk drives.
	MSP 0612	Dual-simultaneous channel disk controller; supports a maximum of 16 MSU 0451A or 15 MSU 0500/501 disk drives.
	MSK 0612	Upgrade from MSP 0611 to MSP 0612.
INTEGRATED MASS STORAGE PROCESSORS FOR ELS ONLY	MSP 8000	Single channel disk controller: Support a maximum of 16 MSU 0451 or 8 MSU 0500/ 500/501 disk drives.
	MSK 8002	Dual simultaneous channel for MSP 8000.
MASS STORAGE PROCESSOR FEATURES	MSF 1140	Device adapter required for support of MSU 0451A disk drives on MSP 0611.
	MSA 1140	Addresset for 4 MSU 0451A disk drives on MSP 0611.
	MSA 1141	Addresset for 2 MSU 0500/501 disk drives on MSP 0611.
	MSA 1144	Non-simultaneous switched channel between MSP 0611, or MSP 0612.

CATEGORY	MARKETING IDENTIFIER	DESCRIPTION
	MSF 1143	First non-simultaneous (switched) Datanet channel on MSP 0611, MSP 0612,
	MSF 1150	Second non-simultaneous (switched)Datanet channel on MSP 0612 only.
	MSF 8000	Device adapter for up to 16 MSU04XX for MSP8000 and MSK8002.
	MSA 8000	Addresset for 4 MSU04XX on MSP8000 and MSK8002.
	MSA 8001	Addresset for 2 MSU050X on MSP8000 and MSK8002.
	MSF 8002	Non simultaneous switched Datanet channel for MSP 8000 and MSK8002.
	MSK 8002	Non simultaneous switched IOM channel for MSP 8000 and MSK 8002.
	PSS 8001	Ride through option (one per free standing MSP).

CATEGORY	MARKETING IDENTIFIER	DESCRIPTION
MASS STORAGE PROCESSOR FEATURES	MSF 1141	Device adapter required to support MSU 0451 A disk drives on MSP 0612.
	MSF 1142	Device expansion feature, to support over 8 (and up to 15) MSU 0500/501 disk drives on MSP 0612. Excludes connection of MSU 0451A disk drives.
	MSA 1142	Addresset for 4 MSU 0451 A disk drives on MSP 0612.
	MSA 1143	Addresset for 2 MSU 0500/501 disk drives on MSP 0612.
	MSU 0451(1)	Removable disk drive. 157 Mbytes (formatted) on 1 spindle.
	MSU 0500(1)	Fixed disk drive. 626 Mbytes (formatted)

(1) This MI must be completed with A or B depending upon :
A = 60 Hz, B = 50 Hz.

CATEGORY	MARKETING IDENTIFIER	DESCRIPTION
DISK DRIVE OPTIONS	MSK 0501	Upgrade from MSU 0500 to MSU 0501.
	MSF 0006	Dual access option for MSU 0451A device. Applicable if device connected to MSP 0612.
	MSF 0011	Dual access option for MSU 0500/501 device. Applicable if device connected to MSP 0612.
FREE STANDING MAGNETIC TAPE CONTROLLER	MTP 0611	Magnetic tape controller; supports up to 8 tape units without dual-channel option and up to 16 tape units with the dual-channel option.
INTEGRATED MAGNETIC TAPE CONTROLLER ELS ONLY	MTP 8001	Magnetic tape controller supports up to 8 tape units.
MAGNETIC TAPE CONTROLLER OPTIONS	MTF 1151	Dual-simultaneous channel option for MTP 0611 only.
	MTF 1152	Second non-simultaneous channel option.

CATEGORY	MARKETING IDENTIFIER	DESCRIPTION
MAGNETIC TAPE CONTROLLER OPTIONS	MTF 1160	9-track, GCR/PE recording capability; 6250/1600 bpi density support.
	MTF 1159	9-track, PE/NRZI recording capability; 1600/800 bpi density support.
	MTF 1158	7-track, NRZI recording capability; 800/556 bpi density support.
	MTA 1152	Addresset for 4 tape units, ON MTP 611/MTF1151.
	MTF 1155	6-bit/ASCII code translator.
	MTF 1156	6-bit/EBCDIC code translator.
	MTF 1157	ASCII/EBCDIC code translator.
	MTF 1125	H200/H2000 tape interchange.
	PSS 8001	Ride through option (one per FREE STANDING MTP)
MAGNETIC TAPE DRIVES	MTU 0438(1)	9-track 1600/6250 bpi, 75 ips, 468 kb/s tape drive.
	MTU 0538(1)	9-track 1600/6250 bpi 125 ips, 780 kb/s tape drive.

(1) This MI must be completed with A or D depending on :
A = 60 Hz, B = 50 Hz.

CATEGORY	MARKETING IDENTIFIER	DESCRIPTION
UNIT RECORD PROCESSORS		
URP 0600 OPTIONS	URF 0040	Addresset extension. Provides for support of more than 4 and up to 7 peripherals on an URP 0600.
	URA 0057	Addresset for PRU 1042 printer.
	URA 0054	Addresset for PRU 1200 printer.
	URA 0055	Addresset for PRU 1600/1601 printer.
	URA 0052	Addresset for CRU 1050 card reader.
	URA 0056	Addresset for CRU 0501 card reader.
	URA 0050	Addresset for PCU 0120 card punch.
EMBEDDED UNIT RECORD PROCESSOR	URP 8001	Integrated URP; supports mix of up to two PRU 1101/1501 and two card devices.
	URP 8002	Integrated URP; supports up to two card devices.
	URP 8004	Integrated URP; supports up to two PRU 1101/1501/or PRU 1042/1200/1600.

3.2 CENTRAL SYTEM WITH MEMORY

CPS 8139

MAJOR UNIT DESCRIPTION

CENTRAL SYSTEM WITH MEMORY

INCLUDES:

- CENTRAL PROCESSOR INCLUDING VIRTUAL UNIT (for GCOS8 Operation) and 32 KByte cache memory
- I/O Multiplexor (IOM) with 20 channel function slots, IOM data rate expansion
- System Control Unit (SCU) with 5 ports
- 4 MB of main memory

REQUIRES:

- System console CSU6601 or CSU6601 B if 50 Hz

CONFIGURABILITY:

- Memory up to 16 MB 6, 8, 12, 16 MB
- Upgradable to the DPS 8/49 (CPS 8141) by CPK8337

MASS STORAGE PROCESSORS:

INTEGRATED	MSP8000 MSK8002
FREE STANDING	MSP0611, MSP0612

Units:	MSU0451A/500/501
of if 50 Hz:	MSU0451B/500B/501B

MAGNETIC TAPE PROCESSOR:

INTEGRATED	MTP8001
FREE STANDING	MTP0611

Units:	MTU0438/538
of if 50 Hz:	MTU0438B/538B

UNIT RECORD PROCESSORS: URP8001/URP8002/URP8004

Printers	PRU1101/1501
or if 50 Hz	PRU1101B/1501B

Cards	CRU 0501A
of if 50 Hz	CRU 0501B

FRONT END PROCESSORS:

DCP7121/7122/7123 or 7121B/7122B/7123B if 50 Hz.

CPS 8141

MAJOR UNIT DESCRIPTION

CENTRAL SYSTEM WITH MEMORY

INCLUDES:

- Central processor including virtual unit (for GCOS 8 operation) and 32 K Byte cache memory

- I/O Multiplexor (IOM) with 20 channel function slots, IOM data rate expansion

- System control unit (SCU) with 5 ports

- 4 MB of main memory

REQUIRES:

- System console CSU6601 or CSU6601 B if 50 Hz

CONFIGURABILITY: - DPS 8/49 is upgradable in two ways :
- Full redundancy option (CPF8132) plus additional CPUs (CPU8131)

- INDEPENDENT COMPONENTS

PROCESSORS	CPU 8131	Max 3
SCU	MXC 8003	Max 1
	CPU 8131 is a prerequisite	
IOM	MXU 8003	Max 1

- Memory sizes up to 32 MB (16 MB per SCU)

MASS STORAGE PROCESSORS:

INTEGRATED	MSP 8000 MSK 8002
FREE STANDING	MSP0611, MSP0612

Units: MSU0451A/500/501
of if 50 Hz: MSU0451B/500B/501B

MAGNETIC TAPE PROCESSOR:

INTEGRATED	MTP 8001
FREE STANDING	MTP0611

Units: MTU0438/0538
of if 50 Hz: MTU0438B/0538B

UNIT RECORD PROCESSORS: URP8001/URP8002/UPR8004

Printers PRU1101/1501
or if 50 Hz PRU1101B/1501B

Cards CRU 0501A
of if 50 Hz CRU 0501B

FRONT END PROCESSORS:

DCP7121/7122/7123 or 7121B/7122B/7123B if 50 H

Date: November 26, 1984

CPS 8257

MAJOR UNIT DESCRIPTION

CENTRAL SYSTEM WITH MEMORY

INCLUDES:

- Central processor including virtual unit (for GCOS 8 operation) and 32 K Byte cache memory
- Free-standing I/O Multiplexor (IOM) with 35 channel function slots, IOM data rate expansion
- Free-standing system control unit (SCU); supports up to 16 MB
- 4 MB of main memory shared in two buckets.

REQUIRES:

- System console CSU6601 or CSU6601 B if 50 Hz
- Protection against short voltage dips
- Diagnostic Processor Unit (DPU) MPU 9001 or MPU 9001B if 50 Hz

CONFIGURABILITY:

- Full redundancy option, includes all necessary addressing (crossbar) features.
- Memory sizes 4MB, 8MB and up to 64 MB under GCOS 8

MASS STORAGE PROCESSORS: MSP 0611, MSP 0612

Units: MSU0451A/500/501
of if 50 Hz: MSU0451B/500B/501B

MAGNETIC TAPE PROCESSOR: MTP0611

Units: MTU0438/0538
of if 50 Hz: MTU0438B/0538B

UNIT RECORD PROCESSORS: URP8001/URP8002/UPR8004

Printers PRU1101/1501
or if 50 Hz PRU1101B/1501B

Cards CRU 0501A
of if 50 Hz CRU 0501B

FRONT END PROCESSORS:

DCP7121/7122/7123 or 7121B/7122B/7123B if 50 Hz.

CPS 8267

MAJOR UNIT DESCRIPTION

CENTRAL SYSTEM WITH MEMORY

INCLUDES:

- Central processor including virtual unit (for GCOS 8 operation) and 32 K Byte cache memory
- Free-standing I/O Multiplexor (IOM) with 35 channel function slots, IOM data rate expansion
- Free-standing system control unit (SCU); supports up to 16 MB
- 4 MB of main memory shared in two buckets.

REQUIRES:

- System console CSU6601 or CSU6601 B if 50 Hz
- Protection against short voltage dips
- Diagnostic Processor Unit (DPU) MPU 9001 or MPU 9001B if 50 Hz

CONFIGURABILITY:

- Full redundancy option, includes all necessary addressing (crossbar) features.
- Memory sizes 4MB, 8MB and up to 64 MB under GCOS 8

MASS STORAGE PROCESSORS: MSP 0611, MSP 0612

Units: MSU0451A/500/501
of if 50 Hz: MSU0451B/500B/501B

MAGNETIC TAPE PROCESSOR: MTP0611

Units: MTU0438/0538
of if 50 Hz: MTU0438B/0538B

UNIT RECORD PROCESSORS: URP8001/URP8002/UPR8004

Printers PRU1101/1501
or if 50 Hz PRU1101B/1501B

Cards CRU 0501A
of if 50 Hz CRU 0501B

FRONT END PROCESSORS:

DCP7121/7122/7123 or 7121B/7122B/7123B if 50 Hz.

DPS 8 CONFIGURATOR SYMBOLS

P	Prerequisite
P ⟷ P	At least one is prerequisite
O	Optional
1/x	Optional from 1 to x
N	Number depends on the functionality required
M	Mandatory
M ⟷ M	At least one is mandatory
E	Excluded : option not applicable
R	Repeat : option must be duplicated

CONFIGURATOR DPS 8						
DESCRIPTION	REMARKS	CPS8245	CPS8255	CPS8265	CPS8275	
1. BASIC CENTRAL SYSTEM						
DPS 8/XX						
Each CPS model including :						
- one processor with 32 KB cache memory - one IOM with 35 channel slots function - one SCU - two megabytes of memory splitted into two buckets of 1 MB						
Each DPS 8 (single or multi CP) requires one Maintenance Processor Unit						
DPS 8/46	Power 1 (= .71 x 66/80)	1				
DPS 8/52	Power 1.34 (= .95 x 66/80)		1			
DPS 8/62	Power 1.83 (= 1.3 x 66/80)			1		
DPS 8/70	Power 2.19 (=1.7 x 66/80)				1	

CONFIGURATOR DPS 8

DESCRIPTION	REMARKS	CPK8245	CPK8255	CPK8265	CPK8275	CPK8245	CPK8255	CPK8265	CPF8246	CPF8256	CPF8266	CPK8246	CPK8256	CPK8266
- Upgrade kits for CPS														
From DPS 8/46 to DPS 8/52		P				1								
From DPS 8/52 to DPS 8/62			P				1							
From DPS 8/62 to DPS 8/70				P				1						
- Redundancy options														
Full redundancy option for 8/46	Each redundancy option includes : same features of CPS plus necessary links to interconnect central system.	P							1					
Full redundancy option for 8/52			P							1				
Full redundancy option for 8/62				P							1			
- Upgrade kits for CPF														
From DPS 8/46R to DPS 8/52R	Each upgrade option for CPF includes only the power pack for the second CPU. The corresponding power pack for first CPU has to be ordered in same time.	P				P			P			1		
From DPS 8/52R to DPS 8/62R			P				P			P			1	
From DPS 8/62R to DPS 8/70R				P				P			P			1

CONFIGURATOR DPS 8

DESCRIPTION	REMARKS	CPS8245	CPS8255	CPS8265	CPS8275	CPU8188	MXC8002	MXU8002	CMM8017	CMM8018	CMM8012
EXTENSIONS FOR DPS 8/70					P	1/3					
Additional CPU	Up to three CPU's 8188 may be connected to a CPS8275										
EXTENSIONS FOR DPS 8/70 AND ALL PARC REDUNDANT DPS 8/XX											
Additional SCU	Maximum configuration is : four modules				P		1/3				
Additional IOM	Each SCU or IOM includes necessary crossbar features.				P			1/3			
Additional memory	See memory repartition										
2 MB									X		
4 MB										X	
8 MB	Requires GCOS 8										X

CONFIGURATOR DPS 8						
DESCRIPTION	REMARKS	CPXXXX	MPU9001	MPU9001B	PS8000	
MAINTENANCE FEATURE						
Maintenance Processor Unit	Mandatory for each DPS 8 system, remains Company property MPU9001 MPU 60 HZ MPU9001B MPU 50 HZ	P	cf 1	1		
2. POWER EQUIPMENT						
Capacity ride through option	Required 1 for each CPU, SCU, IOM (3 per CPS or CPF) when MGS or UPS are not used 50 HZ frequency only	P			1	

CONFIGURATOR DPS 8

DESCRIPTION	REMARKS	CSU6601	CSU6601B	CSU6602	CSU6602B	CSF6601	CSF6602	CSF6602B	CSF6603	CSF6603B	CSF6604	CSF6604B	CSF6606	DKF7201	CSF6607	CSF6605
3. CONSOLES AND FEATURES																
o System Console Includes basic console channel, control firmware, TTU1005 120 cps serial printer, VIP 7205 with video connection support.	Mandatory for all DPS 8 systems	M	M													
Options for system console																
- Auxiliary console with keyboard, 120 cps printer.	TWU1005 = TTU1005 + Keyboard	P	P	O	O											
- Table for system console : includes processor display POD	This option should be ordered with each CSU6601. The POD supports the BOOT, INITIALIZE-EMERGENCY POWER-OFF buttons and the processor speedmeters.	P	P			M										
- Auxiliary KB/display attachment feature	IOM board	P	P			P	O	O								
- Additional keyboard/display (12")	Enables visualisation of the system status (video function)	P	P			P	P	P	O							
- Large Screen Monitor (23") and Monitor Drive option (includes up to 50" (15.25 m) of cable	Attached in serial mode to CSU6601 screen or CSF6603.	P	P			P			P	P	N					
- Extended Systems Control features. Necessary for the addition of a remote console and also for switching between master and auxiliary console.		P	P			P			P	P			O			
- Pedestal for 12" CRT		P	P						P	P				O		
- Pedestal for 120 cps printer		P	P				P	P							O	
- Celling mount for CSF6604											P	P				O

CONFIGURATOR DPS 8

DESCRIPTION	REMARKS	MSP0611	MSA1141	MSF1140	MSF1141	MSF1143	MSF1144
4. <u>MASS STORAGE SUBSYSTEM</u>							
4.1. <u>MASS STORAGE PROCESSORS</u>							
4.1.1. Single channel MSP including : adaptor for MSU0500/1	Supports up to 16 spindles - either 8 x MSU0500/1 or mixed combination of MSU500/1 and MSU451 <u>Note</u> : MSU0500/1 is considered as 2 spindles.	N					
- Options for single channel MSP							
• Addresset for MSU0500/1	Supports up to 2 x MSU0500/1. Maximum 2 or 4 if MSK0612 configured.	P	N				
. Device adaptor for MSU0451	Supports up to 16 x MSU0451	P		1			
. Addresset for MSU0451	1 required for every 4 x MSU0451	P		P	N		
. Non simultaneous (switched) datanet channel	Maximum 2. Requires MSU0451 (NPS operation)	P		P	P	N	
. Non simultaneous (switched) IOM channel	Maximum 3 without MSF1143. Only 1 if MSF1143.	P					N

CONFIGURATOR DPS 8									
DESCRIPTION	REMARKS	MSP0611	MSK0612	MSP0612	MSA1143	MSF1142	MSF1141		
. Upgrade from single to dual simultaneous channel	Upgrade from MSP0611 to MSP0612	P	1						
4.1.2. Dual simultaneous channel MSP including : Adaptor for MSU0500/1	Supports : 8 x MSU0500/1 16 x MSU0500/1 if device expansion configured 8 x MSU0500/1 + 16 MSU0451 if MSU0451 device adaptor configured.			N					
- Options for dual channel MSP									
. Dual addresset for MSU0500/1	1 required for every 2 x MSU0500 Maximum 2 or 4 if MSF1142 configured				N				
. Device expansion	Increases the MSP0612 capacity from 8 to 15 MSU0500/1					1			
. Device adaptor for up to 16 x MSU0451	This option is not compatible with MSF1142						1		

CONFIGURATOR DPS 8

DESCRIPTION	REMARKS	MSP0612	MSF1141	MSA1142	MSF1143	MSF1150	MSF1143	PPS8001
. Dual addresset for MSU0451	1 required for every 4 x MSU0451	P	P					
. Non simultaneous switched datanet channel	Maximum 4. Requires MSU0451 (NPS operation)	P	P	P	N			
. Non simultaneous switched second datanet channel	Maximum 2. Required MSU0451 (NPS operation)	P	P	P		N		
. Non simultaneous switched IOM channel	Maximum 6 without switched datanet channel. Otherwise up to 2.	P					N	
- Common option MSP0611/2								
. Capacitor ride through option	If the disk processor is operated on 50 HZ power and <u>no</u> MGS or UPS is used.							1

CONFIGURATOR DPS 8		MSU0451A	MSU0451B	MSF0006	MSU0500	MSU0500B	MSU0501	MSU0501B	MSF0011	MSK0501
DESCRIPTION	REMARKS									
4.2. MASS STORAGE DEVICES										
4.2.1. Removable disks										
157 MB disc unit	Includes RPS (Rotational Position Sensing) At least one MSU0451A required if NPS used. MSU0451A = 60 HZ MSU0451B = 60 HZ	N	N							
Features										
Dual access : one option per unit	Enables connection of one drive to two control adaptors. Mandatory when MSU0451A or B are connected to a MSP0612.	P		O						
4.2.2. Fixed disks										
626 MB disc unit	Two spindles. Includes RPS. MSU0500B = 50 HZ				N	N				
1100 MB disc unit	Two spindles. Includes RPQ MSU0501B = 50 HZ						N	N		
Feature for MSU0500/501 Dual access : one option per unit.	Enables connection of one drive to two control adaptors. Mandatory when MSU0500/501 are connected to a MSP0612.				P		P		O	
Upgrade kit for MSU500 only					P	P				O
Upgrade kit from MSU0500 to MSU0501 (626 MB to 1100 MB)	One kit per MSU0500 drive									

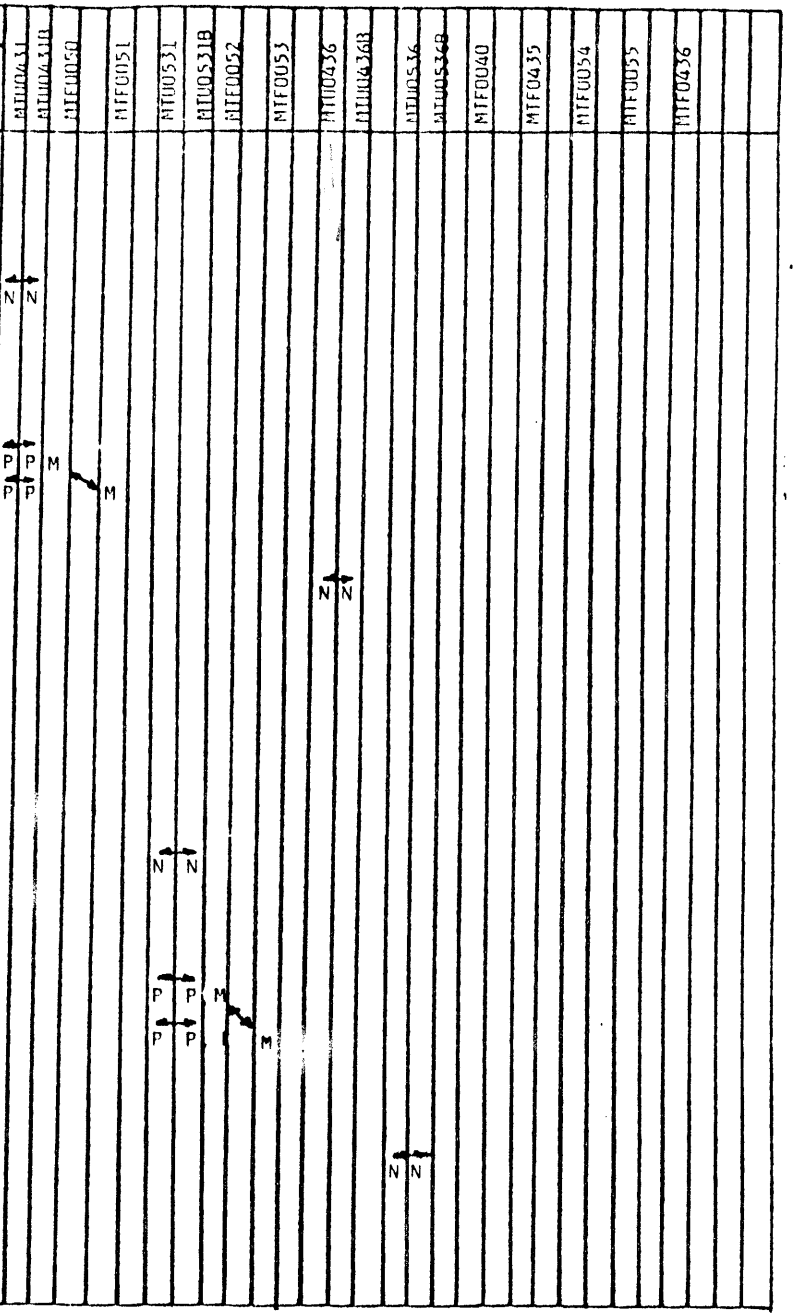
CONFIGURATOR DPS 8		MTP0611	MTF1151	MTF1160	MTF1159	MTF1158	MTF1155	MTF1156	MTF1157	MTF1125	MTA1152	MTF1152	PPS8001
DESCRIPTION	REMARKS												
5. MAGNETIC TAPE SUBSYSTEM													
5.1. MAGNETIC TAPE PROCESSOR Free-standing magnetic tape processor	Handles up to 8 tape units or up to 16 when the dual simultaneous channel is installed. Includes IOM physical channel. Requires at least one of the two recording mode options : GCR/PE or NRZI/PE.	N											
Features													
- Dual simultaneous channel	Permits connection of up to 16 tape units. With this feature, each unit can work simultaneously with any other unit.	P	O										
- Addresset for four tape units		P									M		
At least one of the following two options is mandatory													
. 9 track GCR/PE recording mode (1) (2)	Provides 6250 and 1600 bpi support	P	R	M									
. 9 track NRZI/PE recording mode (1, 2)	Provides 800 and 1600 bpi support	P	R		M								
. 7 track NRZI recording mode (1, 3)	Provides 556/800 bpi support, 9 track NRZI/PE option required	P	R		P	O							
. 6 bit/ASCII translation (1)		P	R				O						
. 6 bit/EBCDIC translation (1)		P	R					O					
. ASCII/EBCDIC translation (1)		P	R						O				
. S200/S6000 tape interchange (1)		P	R							O			
. Switched channel	Provides link between MTP0610 and IOM. Includes PSIA. Maximum 2 if MTF1151 is configured.											O	
Capacitor ride through option :	required if 50 HZ and no MGS or UPS used	P											O

(1) Two required if configuring a dual simultaneous channel MTP0610

(2) Either MTF1149 or MTF1160 are required

(3) MTF1158 use requires MTF1159

CONFIGURATOR DPS B	
DESCRIPTION	REMARKS
5.2 MAGNETIC TAPE UNITS	
5.2.1. 9 tracks, 75 ips drives	MTU0431B = 50 HZ
5.2.1.1. NRZI and PE capability, 120 KB/s	
o Basic magnetic tape unit (single deck)	Density option Mandatory
o Density option : - single density PE/1600 bpi - dual density NRZI/800 bpi	one option per tape unit
5.2.1.2. GCR and PE capability, 468 KB/s	
o Basic magnetic tape unit (single deck) includes density feature CGR/6250 bpi and PE/1600 bpi	MTU0436B = 50 HZ
5.2.2. 9 tracks, 125 ips drives	
5.2.2.1. PE and NRZI capability, 200 KB:s	
o Basic magnetic tape unit (single deck)	MTU0531B = 50 HZ Density option mandatory (not included)
o Density option	
- Single density PE/1600 bpi	one option per tape unit
- Dual density PE/1600 bpi and NRZI/800 bpi	
5.2.2.2. GCR and PE capability, 780 KB/s	
o Basic magnetic tape unit (single deck) includes density feature GCR/6250 bpi and PE/1600 bpi	MTU0536B = 50 HZ



CONFIGURATOR DPS 8

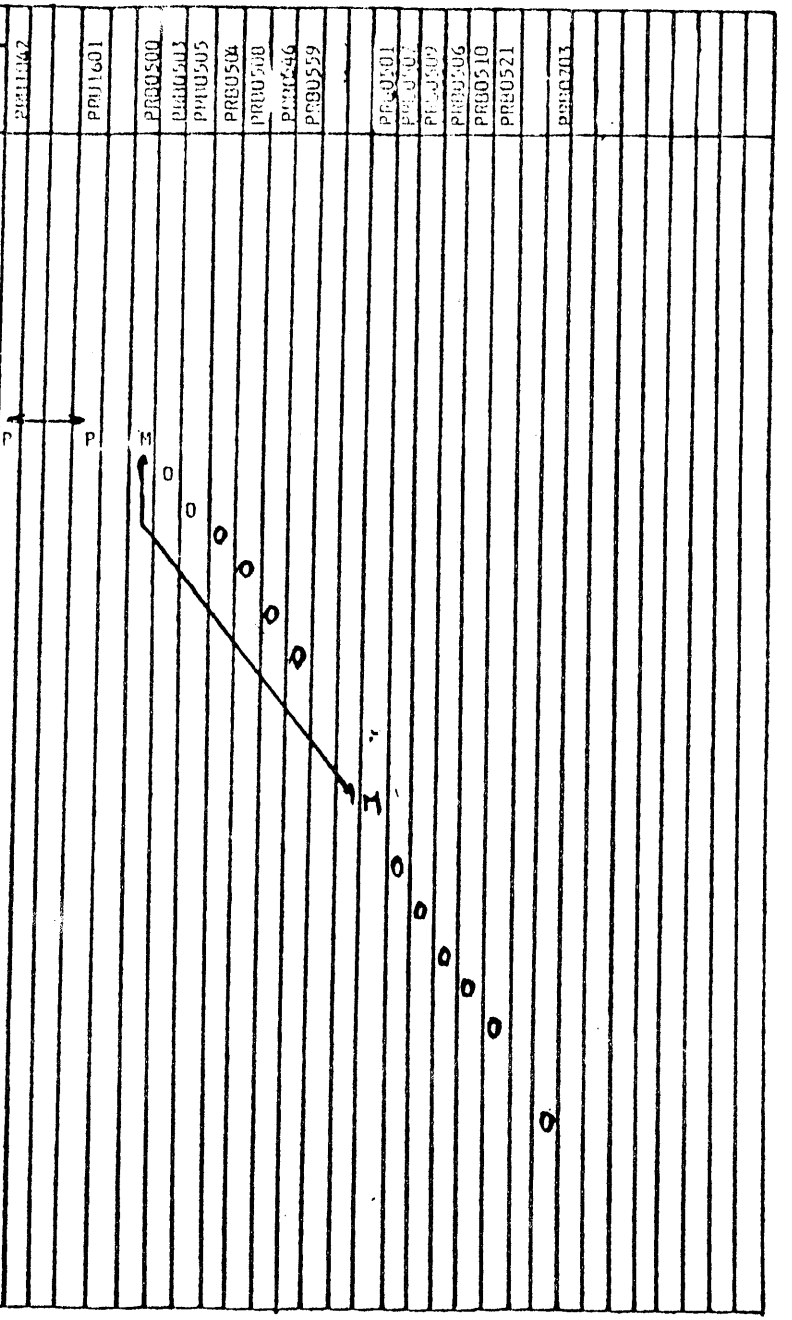
DESCRIPTION	REMARKS	MTU0431	MTU0410	MTF0050	MTF0051	MTU0531	MTU0531B	MTF0052	MTF0053	MTU0436	MTU0436B	MTU0536	MTU0536B	MTF0040	MTK0435	MTK0436
5.2. <u>MAGNETIC TAPE UNITS (continued)</u>																
Features for 75 and 125 ips drives																
High altitude blower		P	P			P	P			P	P	P	P	O		
Upgrade from 75 ips/PE to 125 ips/PE	These two options requires an RPQ	P	P												O	
Upgrade from 75 ips/GCR to 125 ips/ GCR										P	P					O

CONFIGURATOR DPS 8								
DESCRIPTION	REMARKS	URP8001	URP8002	URP8003	URP0600	URF0040		
6. UNIT RECORD SUBSYSTEMS								
6.1. Embedded URC								
Model for up to two card peripherals and up to two PRU1101/1501	Maximum 7 per IOM with a maximum of 8 card peripherals and 8 printers.	N						
Model for up to two card peripherals	Note : URP800 1/2 and 3 do not support PRU1200/1600 and PRU1601		N					
Model for up to two PRU1101/1501				N				
6.2. Free-standing URP	No 50 HZ capability							
Model for 1 to 4 peripherals	Does not support the PRU1101/1501				N			
Features (F.S. URP only)								
- Addresset expansion : up to 7 peripherals	Maximum 1 per URP				P	1		

CONFIGURATOR DPS 8

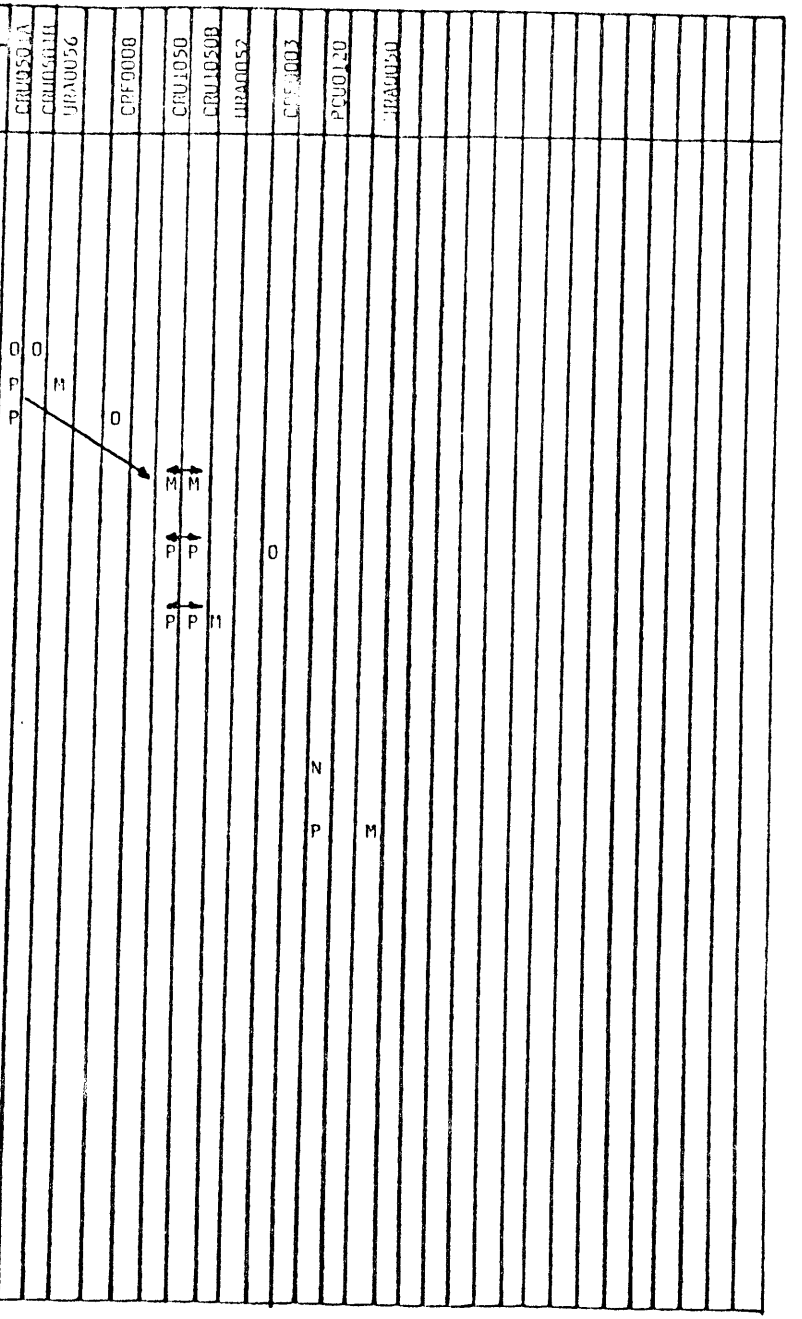
DESCRIPTION	REMARKS	URP8001	URP8002	URP8003			URP0600		PRU1101	PRU1101B	PRU1501	PRU1501B	PRU1042	URA0057		PRU1601	URA0055
6.3. Belt printers																	
1100 lpm belt printer 136 print positions, including 1 belt (see list in tariff)	Do not require addresset Connectable only on URP8001/3 Belts are considered as supplies	P		P					N	N							
1500 lpm belt printer 136 print positions, including 1 belt (see list in tariff)		P		P							N	N					
1000 lpm belt printer (1) 136 print positions, without belt	Addresset mandatory (URA0057)						P						N				
- Addresset for PRU1042	One per printer						P						P	1			
1600 lpm belt printer (1) 160 print position, without belt	Addresset mandatory (URA0055)						P									N	
- Addresset for PRU1601	One per printer (1) PRU1042 and PRU1601 are connectable only on URP0600. No 50 HZ capability.						P									P	1

CONFIGURATOR DPS 8	
DESCRIPTION	REMARKS
UNIT RECORD SUBSYSTEM (continued)	
6.4. Features for all belt printers (printing capabilities) (PRU1042 or PRU1601 only)	At least one belt per PRU. Each PRU must have at least one PRB0500 or PRB0501 (OCR-B, all countries)
PRT CAP for 64 char.	
- All countries OCR-B - SPAIN, ARGENTINA OCR-B - DENMARK, NORWAY OCR-B - SWEDEN, FINLAND OCR-B - PORTUGAL, BRAZIL OCR-B - GREECE - Latin OCR-B - Optimised for France	Same character set as Ex-BGE printers (Series 50, 100, 400, 600, 6000)
PRT CAP for 63 char. : all countries ASCII/OCR-B	
PRT CAP for 63 char.	
- All countries OCR-B - SPAIN, ARGENTINA OCR-B - DENMARK, NORWAY OCR-B - SWEDEN, FINLAND OCR-B - PORTUGAL, BRAZIL OCR-B - GERMANY OCR-B	
PRT CAP for 64 char. - All countries OCR-B	Same character set as ex-Honeywell



CONFIGURATOR DPS 8

DESCRIPTION	REMARKS
UNIT RECORD SUBSYSTEMS (continued)	
6.5. Card readers	
o 500 CPM card reader	Addresset mandatory for URP0600
- addresset for CRU0501 A/B	One for each CRU0501A (on URP0600)
- pedestal for CRU0501A or B	CRU0501B = 50 HZ
o 1050 CPM card reader	Addresset mandatory for URP0600
	connectable only on URP0600
- 51 column read option for CRU1050	One for each CRU1050
- Addresset for CRU1050	One for each CRU1050
	CRU1050B = 50 HZ
6.6. Card punch	
o card punch 120 CPM	Addresset mandatory (not included)
- Addresset for PCU0120	



CONFIGURATOR DPS 8							
DESCRIPTION	REMARKS	PSU0200	PSF0512	PSU0201	PSF0511		
7.0. PERIPHERAL SWITCHES	No 50 HZ power capability available						
7.1. Switching of a peripheral processor between two IOM's	No switching capability of embedded URP and PRU1100/1501						
- Manual peripheral switch (1) console	Cabinet including : - one peripheral switch and IOM channel (hardware required to switch one peripheral controller between two IOM's)	N					
	- Room for 15 additional switches						
- Manual unit switch includes (1) 1 IOM channel	Must be installed in switch console (cabinet) - Includes necessary hardware to switche one peripheral controller between two IOM's	P	O				
7.2. Switching of a peripheral between two peripheral processors							
- Manual peripheral switch (1) console	Cabinet including : - one peripheral switch (hardware required to switch one peripheral between two peripheral controllers, or one peripheral controller addresset between two peripherals.			N			
	- Room for 16 additional switches. Must be installed in switch console cabinet (PSU0200 or PSU0201).						
- Manual unit switch (1)	- Includes necessary hardware to switch one peripheral between two peripheral controller addresse between two peripherals.			P	O		

(1) Up to 15 PSF0511 and/or PSF0512 switches may be loaded in either PSU0200 or PSU0201 console

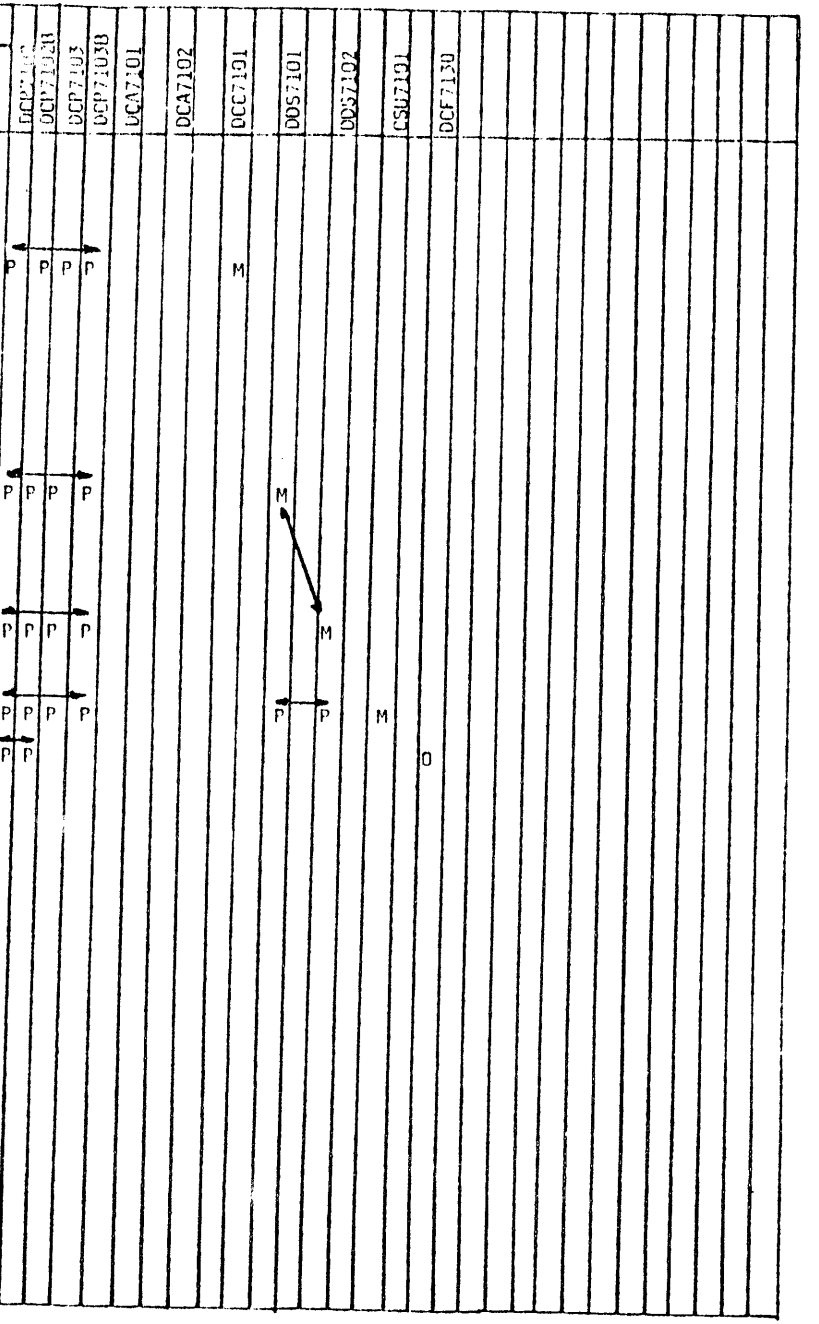
CONFIGURATOR DPS 8

DESCRIPTION	REMARKS
8.0 FRONT END PROCESSORS	
Datanet DCP7102 basic system including : - Processor - 96 Kwords memory, 16Kbits EDAC	Maximum number of lines 48 DCP7102B = 50 HZ Maximum thruput 20 messages of 256 c/s with DNS software.
Datanet DCP7103 basic system including : - Processor - 128 Kwords MOS memory, 16 Kbits EDAC - Remote batch	Maximum number of lines 128 Maximum thruput 80 messages of 256 c/s with DNS software. DCP7103B = 50 HZ
8.1. Options	
Direct channel controller to a DPS 8 or 66/DPS or 66 or 6000.	- Mandatory - 2 maximum excluding direct channel controller to a DPS 7 or 64/DPS or 64.
Direct channel controller to a DPS 7 or 64/DPS or 64.	1 maximum possible if one DCA7101 installed.

DCP7102	DCP7102B	DCP7103	DCP7103B	DCA7101	DCA7102	DCC7101	DDS7101	DDS7102	CSU7101	DKF7130
N	N									
		N	N							
P	P	P	P	M						
P	P	P	P		O					

CONFIGURATOR DPS 8

DESCRIPTION	REMARKS
8.2. Line controllers	
Line controller able to receive up to 4 line adaptors maximum.	-1 at least mandatory 8 DCC7101 maximum per DCC7102 Prerequisite DCC7102 if more than 4 DCC7101 are needed.
Subsystem including	
1 multi device controller	Mandatory if no DDS7102
1 diskette	Excluding DDS7101
Subsystem including	
1 multi device controller 1 dual diskette 2 x 256 KB	Mandatory if no DDS7101 Excluding DDS7001
Console 30 cps	Mandatory
Remote loading of DCP7102	



3.3 PARC EVOLUTION

3.3.1 GENERAL

3.3.2 600-6000 CENTRAL SYSTEMS EVOLUTION

3.3.3 66 "OLD" CENTRAL SYSTEMS EVOLUTION

3.3.4 66-P CENTRAL SYSTEMS EVOLUTION

3.3.5 66/DPS CENTRAL SYSTEMS EVOLUTION

3.3.6 DPS 8 HIGH PROFILE EVOLUTION

3.3.7 MEMORY EVOLUTION

3.3.8 PERIPHERALS EVOLUTION

3.3.9 NSA KIT FOR GCOS 8 SUPPORT

3.3.1 GENERAL

3.3.1.1 BASIC DESCRIPTION

- CII-HB's family of Large Systems was born with the 600, and included successively the 600, 6000, 66, 66-P and 66/DPS systems, leading to the current DPS 8 offering.

- Evolution from one product family to the other was in terms of logic, technology, packaging and configurability.

  But there have been two basic constants;

  - the overall architecture of the system,

  - the total software compatibility, with a common Operating System, GCOS III.

- The central systems could be packaged in two ways:

  - Integrated Control Units: ICU

  - Free-Standing: FS

ICU

In this mode of packaging, the SCU (System Control Unit) and IOM (Input-Output Multiplexor) are integrated in a single cabinet, sharing the power supply. This cabinet may also contain memory or some peripheral controllers.

F.S.

- In this mode of packaging, the SCU, IOM and peripheral controllers each have their own cabinet and power supply.

  In an FS system, some memory may be integrated in the SCU cabinet, but beyond certain limits, there are also separate cabinets for memory.

  Furthermore it is possible to integrate the Unit Record Processor (URP) in the IOM cabinet.

- With the introduction of the 66/DPS systems in 1978, all systems are free-standing (F.S).

- The following table shows the various models of the successive systems families, with their particular characteristics:

MODEL	PACKAGING TYPE	EIS OR NOT	TECH-NOLOGY TYPE	NUMBER OF CPU's POSSIBLE	NUMBER OF SCU's POSSIBLE	NUMBER OF IOM's POSSIBLE	PROCESSOR PERFORMANCE
6030	FS	-	A	4	4	4	-
6050	FS	-	A	4	4	4	-
6070	FS	-	A	4	4	4	-
6025	ICU	EIS	A	2	2	2	.25
6040	ICU/FS	EIS	A	2/4	2/4	2/4	.31
6060	ICU/FS	EIS	A	2/4	2/4	2/4	.52
6080	FS	EIS	A	4	4	4	.71
6610	ICU	EIS	A	2	2	2	.16
6620	ICU	EIS	A	2	2	2	.26
6640	ICU	EIS	A	2	2	2	.43
6660	ICU/FS	EIS	A	2/4	2/4	2/4	.71
6680	ICU/FS	EIS	A	2/4	2/4	2/4	1.0
6605	ICU	EIS	B'	2	2	2	.20
6610-P	ICU/FS	EIS	B'	2/4	2/4	2/4	.26
6620-P	ICU/FS	EIS	B'	2/4	2/4	2/4	.43
6640-P	ICU/FS	EIS	B'	2/4	2/4	2/4	.68
6660-P	ICU/FS	EIS	B'	2/4	2/4	2/4	.95
6680-P	FS	EIS	B'	4	4	4	1.15
66/DPS05	FS	EIS	B'	2	2	2	.71
66/DPS1	FS	EIS	B'	2	2	2	.89
66/DPS2	FS	EIS	B'	2	2	2	1.39
66/DPS3	FS	EIS	B'	2	2	2	1.86
66/DPS4	FS	EIS	B'	3	3	3	2.75
66/DPS5	FS	EIS	B'	4	4	4	3.6

A. 600 SYSTEM

- The 600 was built with discrete technology circuits. There are practically no 600 systems left in our parc.

B. 6000 SYSTEM

- Built with integrated circuits, the 6000 system was the successor of the 600.

  There is still today a fair number of 6000 systems in operation.

- The first models to be introduced were the 6030, 6050, 6070 - so-called "odd" models.

Later, addition of the Extended Instruction Set (EIS) enabled introduction of the so-called "even" models:

6040, 6060, 6080 and an entry model, the 6025.

The EIS instructions were implemented in a new unit of the CPU, called Decimal Unit (DU). The presence of the DU provides increased COBOL performance.

C. 66 SYSTEM

- The 66 system family was introduced as part of the Series 60, in 1974. Level 66, as it was called, was the successor of the 6000, although it had basically the same architecture, technology and functionality.

- The Level 66 family included five models: 6610, 6620, 6640, 6680.

  Later, new models were introduced, with a more attractive price/performance ratio, the 6610-P, 6620-P, 6680-P and a new entry model, the 6605.

  These five models made up the so-called "66-P" family, whereas the other models were referred to as "66-old".

- The difference between 66-P and 66-old is the CPU logic unit:

  66-old: "A" technology logic unit

  66-P: "B'" technolgy logic unit

  B'-technology units are wired in such a way that they may receive the "NSA" kit (New System Architecture) for support of the new Operating System, GCOS 8.

  When a B' logic unit is equipped with the NSA kit, it becomes a B-technology logic unit.

- The 6680-P is a 66-P equipped with a 32K-byte cache memory.

- The 66-P family also included three so-called "time sharing" models, the 6607, 6617 and 6627.

D. 66/DPS SYSTEM

- The 66/DPS is a family of systems with five models introduced in 1978: the 66/DPS 1, 66/DPS 2, 66/DPS 3, 66/DPS 4, 66/DPS 5.

  In 1979, a sixth model was introduced, the 66/DPS 05.

- All 66/DPS systems are free-standing and have B' technology logic units, so they are ready to receive the NSA-kit for support of GCOS 8.

- 66/DPS 1 to 3 are dual-processor systems with 2 CPU's sharing the same power supply cabinet, one SCU, one IOM.

- 66/DPS 4 is a triple processor system, with a 32K byte cache memory for each CPU.

- 66/DPS 5 is a quadruple-processor system, with a 32K byte cache memory for each CPU.

- The 66/DPS 1 to 5 systems may be configured with up to 4 SCU's and 4 IOM's.

- o 66/DPS 05 is a mono-processor system, one SCU, one IOM, 2 MB of memory and one URP integrated in the IOM.

  A redundancy option may be added to the basic system: this option includes one CPU, one SCU, one IOM, 2 MB of memory and one URP integrated in the IOM, as well as all crossbar features.

  Furthermore, a performance enhancement option is available to boost the 66/DPS 05 performance by 34%.

3.3.1.2 EVOLUTION STRATEGY

600/6000 SYSTEMS

No evolution from one model to another or on-site upgrade to a 66 system.

The strategy is to replace the complete system by a DPS 8 system.

66-OLD

No evolution from one model to another. It is possible to upgrade on site to 66-P, by exchanging logic units (A to B' technology), but in most cases, it is perferable to replace the complete system by a DPS 8 system.

66-P

Evolution from one model to another is possible, using the performance kits appearing in our hardware catalogue.

The installation of the NSA-kit is possible, for support of GCOS 8, but must be subject to an RPQ for technical verification (see chapter 3.3.8).

Evolution to DPS 8 line:

- Mono or dual 66/40-P - 60-P to mono or dual DPS 8/62 - 70 (under RPQ procedure).

66/DPS

o 66/DPS 1, 2, 3

- There are options in the hardware catalogue to evolve from one model to the other, and to add SCU's or IOM's.

Note: Extension to DPS 4 and 5 are second hand equipment only.

Evolution to DPS 8 line:

DPS 1 to fully redundant DPS 8/52

DPS 2 " " DPS 8/62

DPS 3 " " DPS 8/70

As far as the evolution of DPS 4 and 5 is concerned: RPQ procedure.

o 66/DPS 05

There are options in the catalogue to increase the basic system performance.

Evolution to DPS 8:

DPS 05 to DPS 8/62

DPS 05 + kit to DPS 8/70

Dual DPS 05 to dual DPS 8/62

Dual DPS 05 + kit to dual DPS 8/70

3.3.2 600/6000 CENTRAL SYSTEM EVOLUTION

- 600/6000 parc evolution is achieved by replacing the complete system with DPS 8 equipment.

3.3.3 66 "OLD" CENTRAL SYSTEM EVOLUTION

- Two possibilities, depending on where the financial and commercial advantage are:

  - replace by DPS 8 system,

  - evolution to 66-P.

- Evolution to 66-P concerns the CPU only and is achieved by changing the logic unit (A to B' technology). Note that the SCU and IOM technology status must be checked to determine whether the evolution is viable. Therefore a site inquiry form must be attached to any order of the following features, which apply to each CPU of the system.

  CPF6101: upgrade from 6610 (.16) to 6620-P (.43)

  CPF6201: upgrade from 6620 (.26) to 6640-P (.68)

  Any upgrade to 60-P performance level must be submitted under RPQ procedure (the installed memory may be removed).

  Note: CPFxxxx options are built with field returns equipments.

3.3.4 66-P CENTRAL SYSTEM EVOLUTION

3.3.4.1 PERFORMANCE EVOLUTION

The following kits are available for performance upgrade within the 66-P line.

a. Kits applicable to the system's 1st CPU:

CPK6030: Upgrade from 6605 (.20) to 6620-P (.43)

CPK6031: Upgrade from 6610-P (.26) to 6640-P (.68)

CPK6032: Upgrade from 6620-P (.43) to 6640-P (.68)

b. Kits applicable to the system's additional CPU's:

CPK6021: Upgrade from 6610-P to 6620-P additional CPU

CPK6022: Upgrade from 6620-P to 6640-P additional CPU

Note: Any evolution to 60-P and/or 80-P must to be submitted under R.P.Q. procedure:

For 60-P: installed memory is subject to replacement.

For 80-P: SCU's may be impacted.

3.3.4.2 FUNCTIONALITY EVOLUTION

It is possible to install the NSA kit on a 66-P system (one kit per CPU) for the support of GCOS 8. This evolution is subject to an RPQ.

See 3.3.8.

3.3.4.3 UPGRADE KITS TO THE DPS 8 LINE

HARDWARE

The following kits are based on the replacement of currently installed logic units with DPS 8 (i.e. DPS E processor) logic units.

These kits are on sales only.

Kit 6018: Upgrade kit from 66/40-P to DPS 8/62 performance level

Kit 6019: Upgrade kit from 66/60-P to DPS 8/70 performance level

Kit 6020: Upgrade kit from 66/40-P additional processor to DPS 8/62 performance level

Kit 6021: Upgrade kit from 66/60-P additional processor to DPS 8/70 performance level.

The new transformed central system must have the same content as a native DPS 8 system:

A single processor must have 2 MB of memory and be a free-standing one.

A dual processor must have 4 MB of memory and must be fully redundant.

The components of the central system must be at the same technical level as those of a native DPS 8.

For the above reasons the R.P.Q. procedure is mandatory. The R.P.Q. response will contain the list of equipment to be ordered from CIL. Angers.

In order to achieve:

full redundancy in the case of dual processor systems,

transformation of ICU systems into free standing systems,

replacemnt of those parts of the system which are incompatible with DPS-E processor and cannot be technically modified,

the following items may be included in the response list:

Kit 6022: 1 MB memory adjustment for adding DPS 8 capability

Kit 6023: 2 MB memory adjustment for adding DPS 8 capability

Kit 6024: Hardware cache clearing on SCU type 003/004

Kit 6001: Buckets for memory re-use

Kit 6006: Kit to add NSA compatibility to IOM type DC8134

Kit 6007: Direct Data Channel for IOM type DC8134,

plus standard items of the international tariff, such as MXC8001, MXU6002, etc...

SOFTWARE

The response to the R.P.Q. will also contain a software configuration using appropriate marketing identifiers, representing the minimum configuration to be contracted for, in order to achieve on the transformed system equivalent functionality with the software currently in use.

	GCOS 3	GCOS 8
Kit 6018	SES7102	SVS7102
Kit 6019	SES 7103	SVS7103
Kit 6020	SES7105	SVS7105
Kit 6021	SES7106	SVS7106

MONTHLY MAINTENANCE

There is no standard monthly maintenance price associated with these above kits. After transformation of his central system, the customer will be charged for it with a monthly fee to be determined locally.

MAINTENANCE TOOLS

As for all DPS 8 systems, a CSU6601 console with its feature CSF6601 and a diagnostic processor unit are mandatory for the implementation of D.C.S.

ADD-ONs

Add-ons to the transformed systems are the same as for a standard DPS 8 system, i.e. those included in the international tariff white pages, code OS 65.

3.3.5 66/DPS CENTRAL SYSTEM EVOLUTION

3.3.5.1 66/DPS 1 TO 3 UPGRADE KITS

3.3.5.1.1 UPGRADE KITS WITHIN THE 66/DPS LINE

CPK6654: 66/DPS 1 (.89 to 66/DPS 2 (1.39) performance upgrade

CPK6658: 66/DPS 2 (1.39 to 66/DPS 3 (1.86) performance upgrade

3.3.5.1.2 UPGRADE KITS TO THE DPS 8 LINE

HARDWARE

The following kits are based on the replacement of currently installed logic units with DPS 8 (i.e. DPS-E processor) logic units.

These kits are on sales only.

Kit 6015: upgrade kit from 66/DPS 1 to 8/52 performance level.

Kit 6016: upgrade kit from 66/DPS 2 to 8/62 performance level.

Kit 6017: upgrade kit from 66/DPS 3 to 8/70 performance level.

As far as 66 DPS 4 and 5 are concerned the respective upgrade kits will be processed entirely under RPQ procedure.

The new transformed central system must have the same content as a native DPS 8 system.

For the above reasons the R.P.Q. procedure is mandatory.

In order to achieve full redundancy in the case of dual processor systems, the following items may be added:

Kit 6022: 1 MB memory adjustment for adding DPS 8 capability

Kit 6023: 2 MB memory adjustment for adding DPS 8 capability

Kit 6024: Hardware cache clearing on SCU type 003/004

MXC8001: Additional F.S. SCU

MXU6602: Additional F.S. IOM

SOFTWARE

The response to the R.P.Q. will also contain a software configuation using appropriate marketing identifiers representing the minimum configuration to be contracted for, in order to achieve on the transformed system equivalent functionality with the software currently in use.

	GCOS 3	GCOS 8
Kit 6015	SES7102 and 7105	SVS7102 and 7105
Kit 6016	SES7102 and 7105	SVS7102 and 7105
Kit 6017	SES7103 and 7106	SVS7103 and 7105

MONTLY MAINTENANCE

There is no standard monthly maintenance price associated with these above kits. After transforamtion of his central system the customer will be charged for it with a monthly fee to be determined locally.

MAINTENANCE TOOLS

As for all DPS 8 systems a CSU6601 console with its feature CSF6601 and a diagnostic processor unit are mandatory for the implementation of D.C.S.

ADD-ONS

Add-ons to the transformed systems are the same as for a standard DPS 8 system, i.e. those included in the international tariff white pages, code OS 65.

3.3.5.2 66/DPS 05 UPGRADE KITS

3.3.5.2.1 UPGRADE KITS WITHIN THE DPS 05 LINE

CPF6642: Performance enhancement feature for 66/DPS 05 (.71 to .95).

CPF6643: Performance enhancement feature for redundant 66/DPS 05 (1.36 to 1.86).

3.3.5.2.2 UPGRADE KITS TO THE DPS 8 LINE

HARDWARE

The following kits are based on the replacement of currently installed logic units with DPS 8 (i.e. DPS 8-E processor) logic units.

These kits are on sales only.

CPK6656: Upgrade kit from DPS 05 mono to DPS 8/62 mono performance level

CPK6657: Upgrade kit from DPS 05 mono with performance enhancement to DPS 8/70 mono performance level

CPK6676: Upgrade kit from DPS 05 with redundancy to DPS 8/62 with redundancy performance level

CPK6677: Upgrade kit from DPS 05 with redundancy and performance enhancement to DPS 8/70 dual performance level.

The above kits are standard (R.P.Q. is not necessary).

SOFTWARE

The current software contract must be cancelled and replaced with the contract and conditions of the DCS policy applicable to DPS 8.

	GCOS 3	GCOS 8
CPK6656	SES7102	SVS7102
CPK6657	SES7103	SVS7103
CPK6676	SES7102 and 7105	SVS7102 and 7105
CPK6677	SES7103 and 7106	SVS7103 and 7106

MAINTENANCE TOOLS

As for all DPS 8 systems a CSU6601 console with its feature CSF6601 and a diagnostic processor unit are mandatory for the implementation of D.C.S.

3.3.6 DPS 8 HIGH PROFILE EVOLUTION

3.3.6.1 DPS 8 HP B-PRIME TECHNOLOGY

These systems have been delivered under the following marketing identifiers:

CPS8240	Central system 8/46
CPF8240	Redundancy option 8/46
CPS8250	Central system 8/52
CPF8250	Redundancy option 8/52

Technology is the same of 66 DPS 05:

- CPU type 66 DPS A (called also B prime technology) including in standard performance level .71 or .95, 8 KB cache memory and virtual memory option.

- Free Standing SCU with 2 MB of memory.

- Free Standing IOM with 35 channel slots function.

The following kits represent the upgrade path within the 66 DPS A technology:

CPK8240 First central processor upgrade kit from DPS 8/46 A to 8/52 A (CPS8240 to CPS8250)

CPK8241 Second central processor upgrade kit from DPS 8/46 A to DPS 8/52 A (CPF8241 to CPF8251).

The following kits represent the upgrade path from 8/52 A to DPS 8/62 E. These kits include the logic unit central processor swap.

After transformation, the central system has the same characteristics of native DPS 8 extended technology.

CPK8250 First central processor upgrade kit from DPS 8/52 A to DPS 8/62 E (CPS8250 to CPS8261)

CPK8251 Second central processor upgrade kit from DPS 8/52 A to DPS 8/62 (CPF8251 to CPF8262)

Note: Other upgrade kits to DPS 8/70 are the same as of DPS 8 high profile extended technology.

3.3.6.2 DPS 8 HP EXTENDED TECHNOLOGY

The following kits represent the upgrade path within the DPS 8 HP line extended technology.

CPK8242: First central processor upgrade kit from DPS 8/46 E to DPS 8/52 E (CPS8241 to CPS8251)

CPK8252: First central processor upgrade kit from DPS 8/82 E to DPS 8/62 E (CPS8251 to CPS8261)

CPK8262: First central processor upgrade kit from DPS 8/62 E to DPS 8/70 E (CPS8261 to CPS8270)

CPK8243: Second processor upgrade kit from DPS 8/46 E to DPS 8/52 E (CPF8242 to CPF8252)

CPK8253: Second processor upgrade kit from DPS 8/52 E to DPS 8/62 E (CPF8252 to CPF8262)

CPK8263: Second processor upgrade kit from DPS 8/62 E to DPS 8/70 E (CPF8262 to CPF8187).

3.3.7 MEMORY EVOLUTION

- Evolution of memory technology is very fast.

  In 1973, the MOS memories appeared and superseded core technology.

  Since then, MOS technology itself evolved in such a way that new models of memory were introduced almost every year, with dramatic volume and price reductions. With current MOS technology, 16 Mega-bytes of memory occupy the same volume as 1/4 mega-byte of CORE memory.

- The consequence of this evolution, combined with larger and larger memory requirements as customer applications grow and multiply, is the spectacular increase of memory add-ons.

- Because of the numerous changes in memory technology in the past years, adding-on memory to an installed system is not a straight-forward operation; it is indeed a complex problem.

  The following paragraphs present the main aspects of the problem and provide guidelines in order to avoid errors.

- MOS memory is composed of two basic parts:

  - memory boards,

  - memory buckets, which contain the boards, as well as a memory controller and the memory speed option (1400 or 750 nanoseconds).

- Memory is housed in cabinets, with two buckets per cabinet.

- There are four types of MOS memory boards in our parc:

  - 1K 16 pins

  - 4K 22 pins

  - 4K 16 pins

  - 16K 16 pins.

- Since each memory board type requires its own bucket, and since the type of bucket depends on whether it is insalled in a Free-standing or Integrated cabinet, and on whether it is in the top or bottom part of the cabinet, there are 16 different bucket types.

- Memory add-on requirements may be served by recycled memory or new built memory.

  Because new-built memory is 16K 16 pins (refer to 3.1.1.6), in some cases the whole installed memory has to be replaced.

- In all cases, a site inquiry form, which precisely describes the installed memory configuration and type, must be attached to orders for memory add-ons.

- The following items of our hardware catalogue may be used for memory add-ons:

  * CMM6042: 1 Mega-byte memory increment, 1400 ns speed.

    Applies to CPS61XX/62XX/64XX and generally speaking to all 66 systems under the 6660 or 6660-P.

    CMA6042 is a prerequisite.

  * CMA6042: Addresset for CMM6042.

    Includes features needed for installation of memory increment (cabinet, extended address option, etc...).

  * CMM6032: 1 Mega-byte memory increment, 750 ns speed.

    Applies to 6660, 6680, 6660-P and all 66/DPS systems.

    CMA6032 is a prerequisite.

  * CMA6032: Addresset for CMM6032.

    Includes features needed for installation of memory increment (cabinet, extended address option, etc...).

- The following items do not appear in the hardware catalogue, but they are in the cession price catalogue. Their purpose is to facilitate memory recycling. Their use is subject to validation by technically knowledgeable personnel.

  * KIT 6001: Memory bucket (all types)

  * KIT 6002: Memory cabinet

  * KIT 6003: Harness kit, for installation of bucket in cabinet.

  * KIT 6004: Memory speed-up option (1400 to 750 ns) for MOS memory types 4K 16 pins or 16K 16 pins.

  * KIT 6005: Extended address option for 6000 and 66A CPU's.

3.3.8 PERIPHERAL EVOLUTION

This chapter describes the peripheral families connected on 6000 - 66 - 66DPS lines (OS 19 - 66 and 33).

These peripherals may be classified according to:

A. The interface used for the connection to the system

- o Peripherals directly connected to the IOM through a CPI interface.
- o Peripherals connected through a peripheral controller.
- o Peripherals using a special interface.

B. The system on which these peripherals may be connected

- o Old peripherals for which the connection is authorized on DPS 8 systems;
- o New peripherals for which the connection is authorized on the 6000 - 66 and 66/DPS systems.

3.3.8.1 PERIPHERALS USING A CPI (Common Peripheral Interface)

Except for printers PRT 205, 207, 209, these products have been withdrawn from our catalogue and cannot be proposed anymore.

Connection of products using CPI interface is not authorized on DPS 8 systems.

- o Peripherals of this type that may be found in the parc are:

Printers	PRT205/207/209/300/301
Card punch	CPZ201
Card reader	CRZ201
Console	C08030/31

3.3.8.2 PERIPHREALS CONNECTED THROUGH A PERIPHERAL CONTROLLER

- Since 1971, all new peripherals are connected to the system through a peripheral controller, which takes care of peripheral amnagement, thus off-loading the central system.

  The consequence is of course increased system performance.

- The interface between peripheral controllers and the IOM is a PSIA (Peripheral Subsystem Interface Adapter) or for fast peripheral controllers, like MTP0610 or MSP driving MSU0500/501, a NPSIA (New Peripheral Subsystem Interface Adapter).

  The different types of peripheral controllers are:

  MSP for disk management

  MTP for tape management

  URP for card devices and printer management.

  Technically when a DPS 8 replaces a 6000 - 66 or 66/DPS system, installed controllers could be connected to the new system. This may be true for free-standing URP's but rarely for MSP or MTP because these controllers must be changed for the support of high performance tape or disk devices.

3.3.8.2.1 DISK SUBSYSTEMS

All MSP0600, MSP0601, MSP0603 and MSF6006 are second hand equipment only.

Available options (new built):

- MSP0601:

MSF1024	Under RPQ. Allows connection of up to 8 X MSU0500, if the option MSF1021 (dual simultaneous channel) is present; it will be necessary to dismount it. Note: MSF1024 applies to MSP model # WMSP450XX only.
MSF1045	Allows connection of MSU0501. MSU0500 and 501 may be mixed.
MSA 1031	Addresset for up to 4 X MSU0451's (maximum 4 or 8 if MSF1033 is configured).
MSA1030	Dual access addresset for up to 4 X MSU0451. used when MSF1021 or MSF1031 is configured.
MSA1033	Addresset for up to 2 X MSU0500/1's (maximum 4).

- MSP0603

MSF1035 Device adapter for MSU0451A. Provides for connection of up to 16 MSU0451A devices.

MSF1034 Drive expansion for MSU0500

Allows the connection of up to 7 additional MSU0500 devices.

Incompatible with MSF1035.

This option should only be used when the number of I/O per second on the drives is relatively low.

MSA1033 Addresset for MSU0500.

Allows connection of up to 2 MSU0500 devices.

Up to 4 MSA1033 options are allowed if MSF1034 not configured. Otherwise, with option MSF1034, up to 8 MSA1033 are allowed.

MSA1031 Addresset for MSU0451A. Allows connection of up to 4 MSU0451A devices.

Up to 4 MSA1031 allowed.

Requires MSF1035.

MSF1036 Dual crossbar option. Allows connection of all disk drives to 2 MSP's.

Requires on MSU0451A option MSF0006 and on MSU0500 option MSF0011.

MSF1026 Non-simultaneous switched channel. Provides the hardware needed for an additional non-simultaneous IOM channel.

MSF1027 Non-simultaneous switched datanet channel.

At least 1 is necessary for each datanet when NPS is used. MSU0451 required.

- MSP0606

MSF1035 Device adapter for MSU0451A. Provides connection capability of up to 16 MSU0451A.

MSF1034 Drive expansion for MSU0500. Allows the connection of up to 7 additional MSU0500.

MSA1032 Addresset for MSU0500. Allows connection of up to 2 X MSU0500. Maximum 4 X MSA1032. If MSF1034 configured, up to 8.

MSA1031 Addresset for MSU0451A. Allows connection of up to 4 MSU0451A. Up to 4 MSA1031 allowed.

MSF1026 Non-simultaneous switched channel. Provides the hardware needed for an additional non-simultaneous IOM channel.

MSF1027 Non-simultaneous switched datanet channel. At least 1 is necessary for each datanet when NPS is used. MSU0451 required.

MSF1045 Allows connection of MSU0501. MSU0500 and MSU501 may be mixed on same control adapter.

o DISK UNITS

- MSU0451A can be connected on MSP0601 and on MSP0603 or MSP0606 when the control adapter MSF1035 is installed.

- MSU0500 can be connected on MSP0603 or 606 and on MSP0601 model # WMSP450XXX under RPQ.

  On 66 and 66/DPS, it is possible to upgrade on site a MSU0500 to a MSU0501; the option to be ordered for this purpose is MSF0013, capacity enhancement for MSU0500.

  One option has to be ordered for each device upgrade and requires the MSF1045 option on the MSP.

  Chapter 3.1.4.2 includes a table providing characteristics of the three disk models.

3.3.8.2.2 MAGNETIC TAPE SUBSYSTEM

As the MTP0601 has been withdrawn from our catalogue the MTP0610 is the only tape controller available on 6000 - 66 and 66/DPS.

For description, see chapter 3.1.5.1.

A. On 6000 and 66 systems the following magnetic tape devices are available:

   MTU0431: 9-track, 800/1600 bpi, 75 ips, 120 Kbs

   MTU0531: 9-track, 800/1600 bpi, 125 ips, 200 Kbs

   MTU0436: 9-track, 1600/6250 bpi, 75 ips, 780 Kbs

   MTU0536: 9-track, 1600/6250 bpi, 125 ips, 780 Kbs

B. On 66/DPS in addition to the preceding handlers, there is also:

   MTU0601, MTU0531 — 9-track, 1600/6250 bpi, 200 ips, 1250 Kbs

Note

MTU0431/531 can be connected to the MTP0601

MTU0436/536 requires the MTP610.

MTU0400/500/600 can be connected to the MTP0610.

MTU431/531, MTU0400/500/600 and MTU0436/536/0610 can be mixed on same MTP0610; only restriction: MTU0431/531/610 cannot be mixed on same addresset with other tape handler.

3.3.8.2.3 UNIT RECORD SUBSYSTEM

- All unit record controllers (URP) and card or printer peripherals available for DPS 8 systems are available as add-ons to the non-DPS 8 parc.

- Installed unit record free standing model may be connected to current DPS 8 systems.

- See 3.1.6 for product descriptions.

3.3.9 NSA KIT FOR SUPPORT OF GCOS 8

- The new Operating System, GCOS 8, can be used on DPS 8, 66/DPS and 66-P systems. Operation of GCOS 8 uses new instructions and hardware features which are grouped in a new unit of the CPU, called VIRTUAL UNIT (VU). The corresponding hardware features are also referred to as the NEW SYSTEM ARCHITECTURE (NSA), hence the name "NSA-kit".

- The NSA-kit is standard on all DPS 8 systems.

  The kit may be installed on all 66/DPS systems and is to be ordered, using the following Marketing Identifier in our hardware catalogue: CPK6668 (one kit is necessary for each CPU), but it is recommended to check that the IOM and SCU conform to the requirements listed below for 66-P systems.

  Because of these requirements, in the case of 66-P systems, the order and installation of NSA-kits is subject to the RPQ procedure, for technical verification and definition of the actual system modifications required.

- Requirements for installation of the NSA-kit:

  a. CPU

  The NSA kit may be installed on the following CPU types:

  - WCPU66BX = 66-P CPU
  - 4WCP6600AAX + WNCU66BA/CA = 66 old transformed into 66-P by logic unit swap.

  b. IOM

  The IOM must be one of the following types:

  - 4WDC8634AA1
  - 4WDC8134AA1 + 4WPGE834AA1 *
  - 4WCSM601AA1
  - 4WCSM001AA1 + 4WPGE824BA1 *

  * Note that option 4WPGE834AA1 includes the IOM part of 1 datanet channel. For each other datanet installed, the following option must be ordered:

    4WDDC645BA1 or BA2

c. SCU

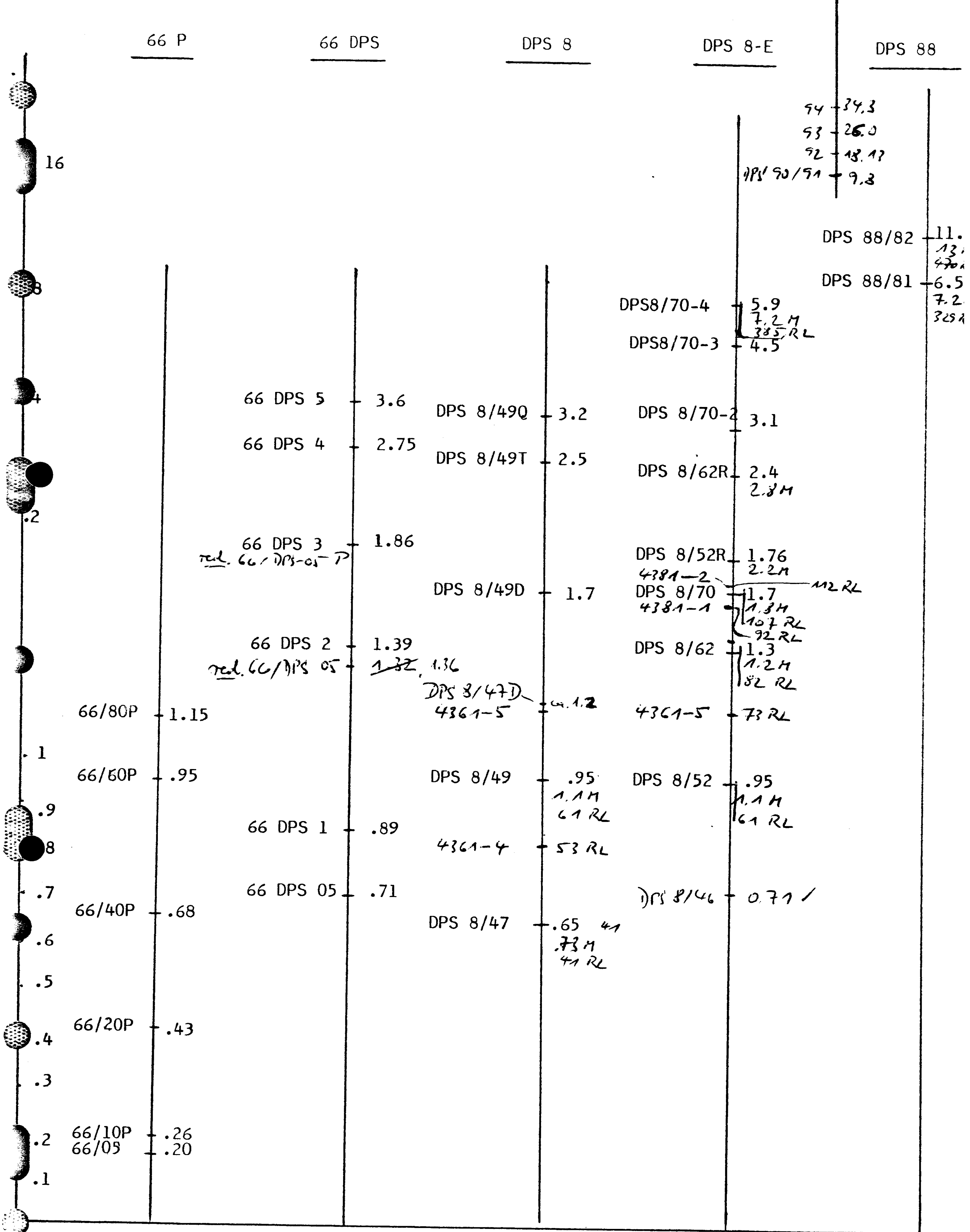
The SCU must be one of the following types:

- WSCU004A
- WSCU003A + WSCUNSAA
- WSCU001A + WSCUNSAA

- The complexity of the above paragraphs justifies the fact that an RPQ must be sent for installation of the NSA-kit on a 66-P CPU.

3.4. RECYCLED EQUIPMENT

3.5. SYSTEMS PERFORMANCE SUMMARY



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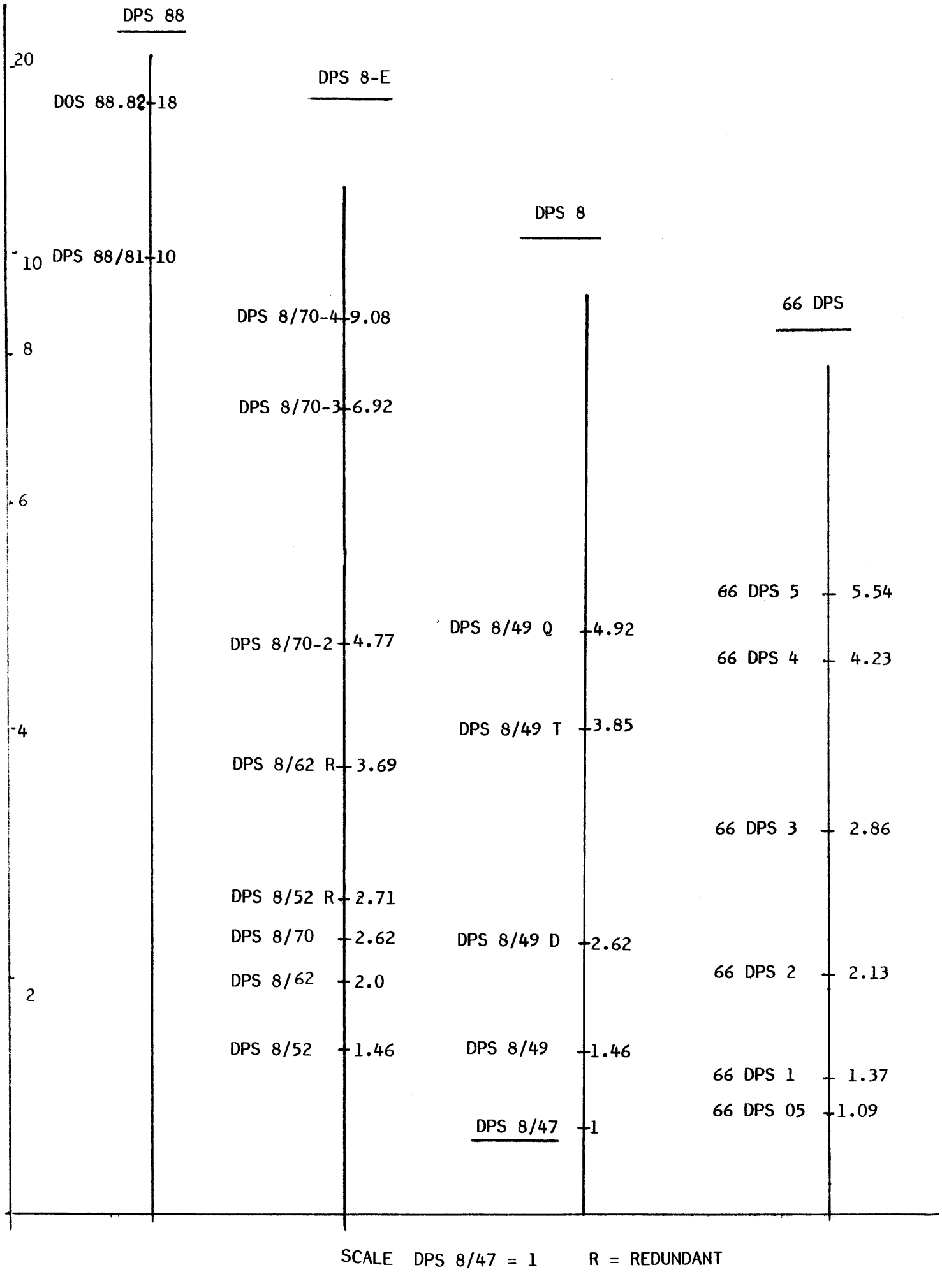
M = Mips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DOS 88.82 18
10
DPS 88/81 10
8
6
4
2
DPS 8-E
DPS 8/70-4 9.08
DPS 8/70-3 6.92
DPS 8/70-2 4.77
DPS 8/62 R 3.69
DPS 8/52 R 2.71
DPS 8/70 2.62
DPS 8/62 2.0
DPS 8/52 1.46
DPS 8
DPS 8/49 Q 4.92
DPS 8/49 T 3.85
DPS 8/49 D 2.62
DPS 8/49 1.46
DPS 8/47 1
66 DPS
66 DPS 5 5.54
66 DPS 4 4.23
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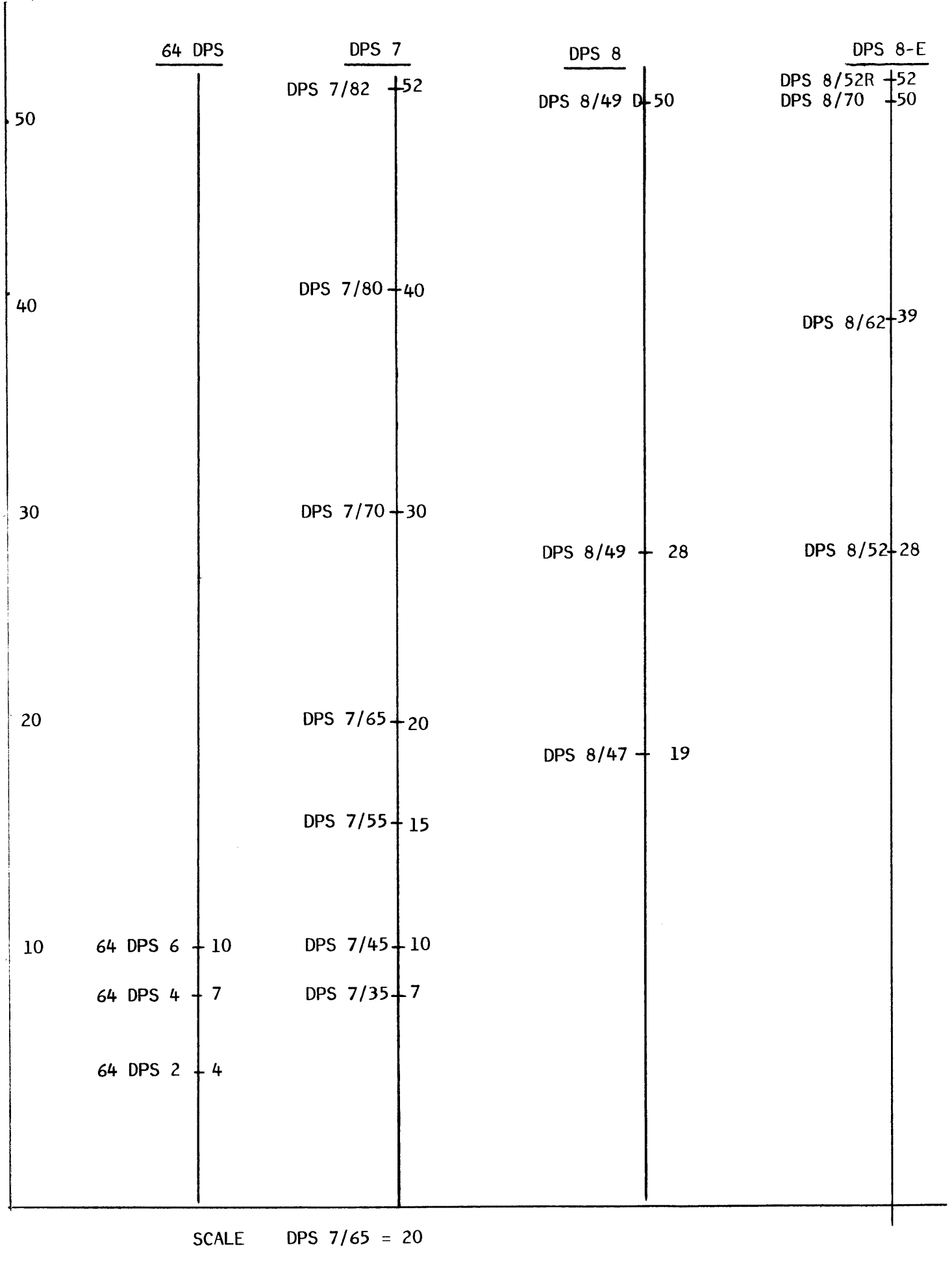
66 DPS 05 1.09
SCALE DPS 8/47 = 1
R = REDUNDANT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DPS 8
DPS 8-E
DPS 7/82 52
DPS 8/49 D 50
DPS 8/52R 52
DPS 8/70 50
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DPS 8/62 39
30
DPS 7/70 30
DPS 8/49 28
DPS 8/52 28
20
DPS 7/65 20
DPS 8/47 19
DPS 7/55 15
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DPS 7/45 10
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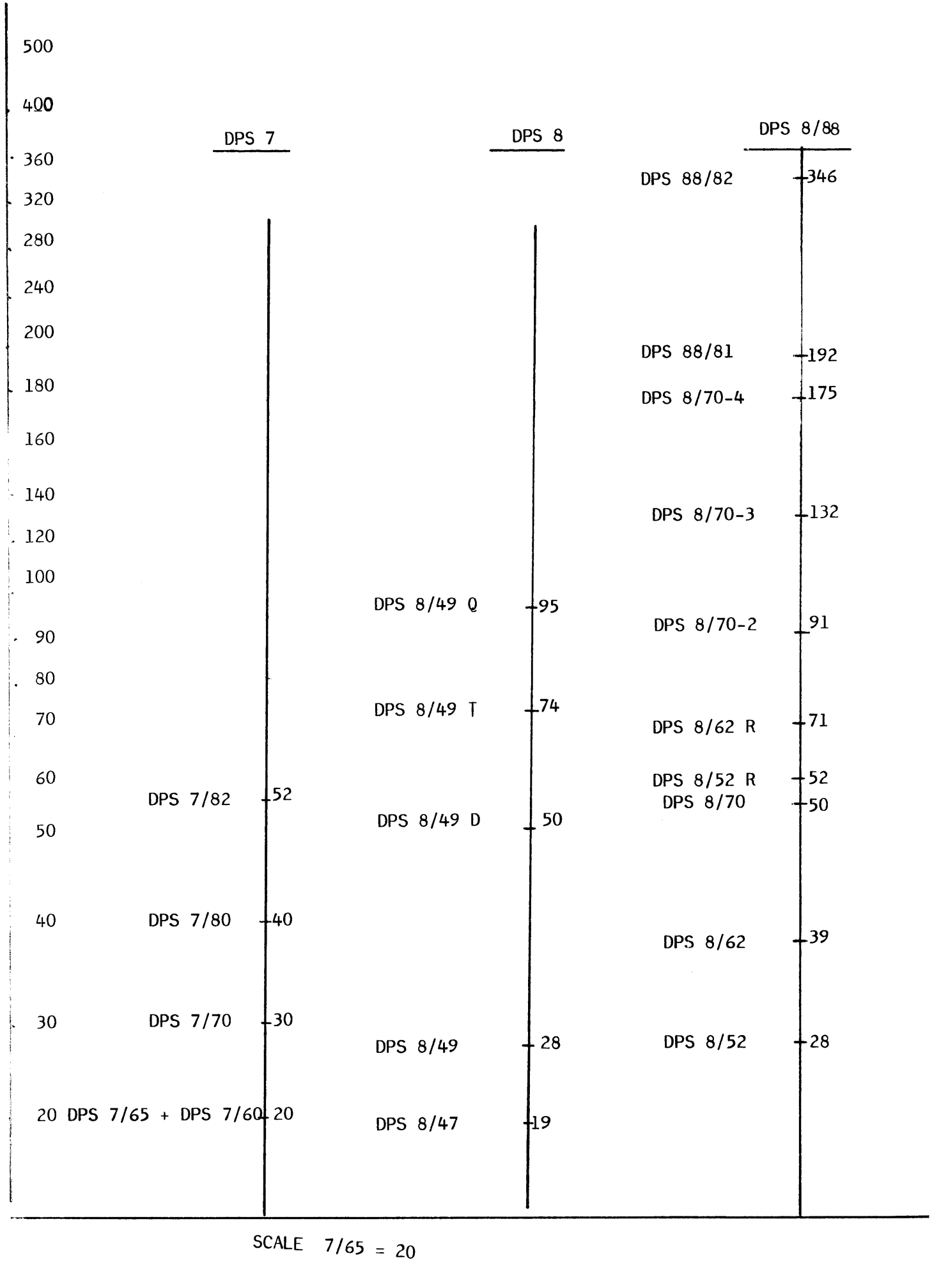
DPS 7/35 7
64 DPS 2 4
SCALE DPS 7/65 = 20


500
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DPS 7
DPS 7/82
52
DPS 7/80
40
DPS 7/70
30
DPS 7/65 + DPS 7/60
20
DPS 8
DPS 8/49 Q
95
DPS 8/49 T
74
DPS 8/49 D
50
DPS 8/49
28
DPS 8/47
19
DPS 8/88
DPS 88/82
346
DPS 88/81
192
DPS 8/70-4
175
DPS 8/70-3
132
DPS 8/70-2
91
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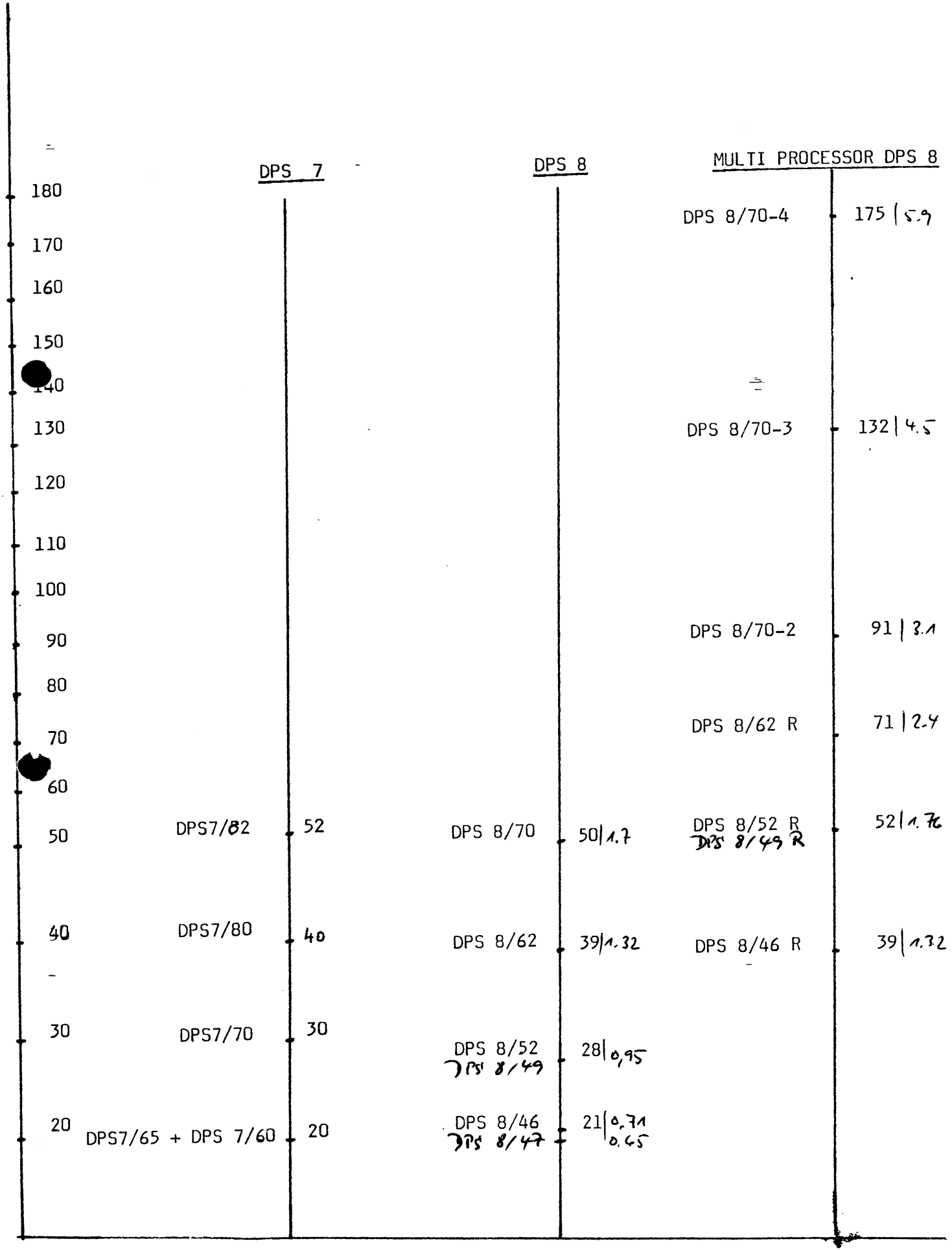
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DPS 8
MULTI PROCESSOR DPS 8
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170
160
150
140
130
120
110
100
90
80
70
60
50
40
30
20
DPS7/82
DPS7/80
DPS7/70
DPS7/65 + DPS 7/60
52
40
30
20
DPS 8/70
DPS 8/62
DPS 8/52
DPS 8/49
DPS 8/46
DPS 8/47
50 | 1.7
39 | 1.32
28 | 0,95
21 | 0.71
0.45
DPS 8/70-4
DPS 8/70-3
DPS 8/70-2
DPS 8/62 R
DPS 8/52 R
DPS 8/49 R
DPS 8/46 R
175 | 5.9
132 | 4.5
91 | 3.1
71 | 2.4
52 | 1.76
39 | 1.32

4. SOFTWARE

4.1 GCOS 8

4.2 GCOS III

4.3 DNS

4.4 APPLICATIONS

4.5 SRPQ ITEMS

LARGE SYSTEMS PRODUCT GUIDE

REMOVE THE SECTIONS :

4.2. GCOS III SOFTWARE

4.4. APPLICATIONS

4.5. SRPQ ITEMS

AND REPLACE THEM BY THE FOLLOWING UPDATE.

NOVEMBER 30, 1984

4.2 GCOS III

4.2.1 GCOS PACKAGING SUMMARY
4.2.2 GCOS SOFTWARE LISTING
4.2.3 GCOS SUMMARY CONFIGURATOR
4.2.4 SUPPORT MATRIX

4.2.1

GCOS PACKAGING SUMMARY

4.2.1 GCOS PACKAGING SUMMARY

By the end of 1981, DCS should have been totally applied to the parc. This section describes the packaging summary for the DCS version of the GCOS III catalog.

GCOS III

OPERATING SYSTEM KERNEL

SES6200	GCOS III OPERATING SYSTEM EXECUTIVE
SES7101	EXPANDED SUPPORT ON SES6200 1ST CP LEVEL 1
SES7104	EXPANDED SUPPORT ON SES6200 2ND CP LEVEL 1
SES7102	EXPANDED SUPPORT ON SES6200 1ST CP LEVEL 2
SES7105	EXPANDED SUPPORT ON SES6200 2ND CP LEVEL 2
SES7103	EXPANDED SUPPORT ON SES6200 1ST CP LEVEL 3
SES7106	EXPANDED SUPPORT ON SES6200 2ND CP LEVEL 3
SES7107	EXPANDED SUPPORT ON SES6200 3RD CP LEVEL 1, 2, 3
SES7108	EXPANDED SUPPORT ON SES6200 4TH CP LEVEL 1, 2, 3

UTILITIES

SES6208	PROGRAM NUMBER AS A RESOURCE OPTION
SEU6210	UTILITY/MAINTENANCE FACILITY
SEU6206	CAPSUL
SEU6213	PARS
SEU7201	SLAVE PROGRAM ACTIVITY MONITOR (SPM/II)

FILE SYSTEM

SEU6201	FILE GENERATION FACILITY
SFU6212	FILE MANAGEMENT SYSTEM UTILITIES
SEL7221	GENSYS - TAPE MANAGEMENT SYSTEM

LANGUAGES

SFL6201	COBOL-74 COMPILER AND RUNTIME FACILITY
SER6200	COBOL-74 RUNTIME FACILITY
SEP6203	COBOL-74 DEBUG SUPPORT OPTION
SEL6202	FORTRAN COMPILER AND RUNTIME FACILITY
SER6201	FORTRAN RUNTIME FACILITY
SEL6205	FORTRAN-77 COMPILER AND RUNTIME FACILITY
SER6203	FORTRAN-77 RUNTIME FACILITY
SEP6205	FORTRAN-77 DEBUG SUPPORT OPTION
SEL6206	FORTRAN-77 HEXADECIMAL OPTION
SEL6222	FORTRAN-66 COMPATIBILITY OPTION FOR FORTRAN-77
SFL6202	PL/1 COMPILER AND RUNTIME FACILITY
SER6202	PL/1 RUNTIME FACILITY
SEL6204	RPG-II FACILITY
SEU6212	DEBUG SUPPORT SYSTEM
SEL7202	APL INTERPRETER OPTION
SEL7212	LISP PROGRAMMING LANGUAGE
SEL7213	PASCAL COMPILER AND RUNTIME FACILITY
SEL7214	B-LANGUAGE FACILITY

TIME SHARING

SEP6201	TSS STANDARD FACILITY
SEU6208	TSS SORT OPTION
SEU6209	TSS ELECTRONIC MAIL OPTION
SEL6218	TSS TEXT PROCESSING OPTION (TEX)
SEL6219	TSS TEXT PROCESSING LIBRARY OPTION
SEL6203	TSS BASIC LANGUAGE OPTION
SEC6210	MULTI COPY TSS OPTION

DATABASE AND TRANSACTIONAL FACILITIES

SED6205	DMIV BASIC FACILITY
SEV6201	DMIV FORTRAN SUBSCHEMA TRANSLATOR
SED6206	DMIV/TP FACILITY
SED7015	DMIV/TP EXTENSIONS (DUAL)
SEU6211	DMIV/TP FORMS OPTION
SED6207	DMIV POLYGLOT QRP OPTION
SED6208	DMIV POLYGLOT PLP OPTION
SED6229	DATA DICTIONARY/DIRECTORY SYSTEM BASIC FACILITY
SED6230	DATA DICTIONARY/DIRECTORY SYSTEM ON-LINE OPTION

GCOS PACKAGING SUMMARY

COMMUNICATIONS

SFC6201	EXTENDED FNP SUPPORT FACILITY
SES7201	GRTS-I FACILITY
SES6201	GRTS-II FACILITY
SEC6204	NPS FACILITY
SEC6202	HOST FILE TRANSCEIVER FACILITY FOR MINI 6
SFC6212	HOST TO HOST FILE TRANSFER FACILITY VIA DN7100
SFU6210	GCOS NETWORK ADMINISTRATION UTILITIES FOR DN7100

PACKAGES

SED7008 DM-IV COMPREHENSIVE FACILITY

Includes:

SED6205	DMIV BASIC FACILITY
SED7206	DMIV/TP FACILITY
SED6207	DMIV POLYGLOT QRP OPTION
SED6208	DMIV POLYGLOT PLP OPTION
SFL6201	COBOL-74 COMPILER AND RUNTIME

SED7009 DM-IV STANDARD FACILITY

Includes:

SED6205	DMIV BASIC FACILITY
SED6206	DMIV/TP FACILITY
SFL6201	COBOL-74 COMPILER AND RUNTIME

SEL7203 FORTRAN-77 COMPREHENSIVE FACILITY

Includes:

SEL6205	FORTRAN-77 COMPILER AND RUNTIME
SEP6205	FORTRAN-77 DEBUG SUPPORT OPTION
SEL6222	FORTRAN-66 COMPATIBILITY

SEP7201 TSS COMPREHENSIVE FACILITY

Includes:

SEP6201	TSS STANDARD FACILITY
SEU6208	TSS SORT OPTION
SEU6209	TSS ELECTRONIC MAIL OPTION
SEL6218	TSS TEXT PROCESSING OPTION
SEL6219	TSS TEXT PROCESSING LIBRARY OPTION
SEL6203	TSS BASIC LANGUAGE OPTION

BCD SOFTWARE

SED6219	IDS/I FACILITY
SED6220	IDS/I DATA QUERY FACILITY
SEL6220	COBOL-68 COMPILER AND RUNTIME FACILITY (includes ISP)
SES6202	TPS FACILITY
SFS6201	TDS FACILITY
SFS7002	TDS DUAL PROCESSOR OPTION
SFP6202	MDQS/II FACILITY
SFP6204	MDQS/IV FACILITY

4.2.2

GCOS SOFTWARE LISTING

The following GCOS software listing is arranged by Marketing Identifier in alphanumeric sequence. The software products listed under prerequisites are those required to run the described product.

M.I.	DESCRIPTION	PREREQUISITES
SEC6202	HOST FILE TRANSCEIVER FACILITY FOR MINI 6 This is a program which provides a file exchange capability with a Mini-6. Interface to the Mini-6 Multifunction System is provided.	SES6200 SEU6210 (SEC6204 or SES6201 or SES7201)
SEC6204	NPS FACILITY This facility provides message switching and sophisticated control of remote I/O as well as facilities to allow nex terminal types to be more easily defined.	SES6200 SEU6210
SEC6210	MULTI-COPY TIME SHARING OPTION Multi-Copy Time Sharing Support Option enables up to 4 copies of the Time Sharing System (TSS) to execute simultaneously and can increase the number of time sharing users that can be supported. The total number supported is dependent on the hardware resources that are available, but can be in the range of 800 users with 4 copies of TSS.	SES6200 SEP6201 SEU6210 (SEC6204 or SES6201 or SES7201)
SED6205	DM-IV BASIC FACILITY GCOS DM-IV Basic System includes the Data Base Manager (I-D-S/II) and Interactive I-D-S/II. It is included in SED7008 and SED7009.	SES6200 SEU6210 (SFL6201 and SEL6209 or SEL6202 and SEV6201)
SED6206	DM-IV TRANSACTION PROCESSOR FACILITY GCOS DM-IV Transaction Processor is a communications oriented executive that can process a variety of transactions and provides support for large volume on-line traffic under control of GCOS and DM-IV software. Included in SED7008 and SED7009.	SES6200 SED6205 SFL6201 SEU6210 (SEC6204 or SES6201 or SES7201)

M.I.	DESCRIPTION	PREREQUISITES
SED6207	DM-IV POLYGLOT QRP OPTION GCOS DM-IV Query and Reporting processor is a subsystem of DM-IV which can access a data base controlled by Integrated Data Store/II and provide capabilities for retrieval, computation, sorting and output generation. Retrieval capabilities are provided for Non-DM-IV files with SR4JS3. Included in SED7008.	SES6200 SED6205 SEU6210 SEL6209 SEP6201 (SEC6204 or SES6201 or SES7201)
SED6208	DM-IV POLYGLOT PLP OPTION GCOS DM-IV Procedural Language Processor is a high level language that extends the capability of the Query and Reporting Processor (SED6207), a prerequisite for data retrieval, updating and processing. Included in SED7008	SES6200 SED6205 SED6207 SEU6210 SEL6209 SEP6201 (SEC6204 or SES6201 or SES7201)
SED6219	I-D-S/I FACILITY This facility provides an efficient data organization technique and a simplified means for record processing in the mass storage random access environment.	SES6200 SEL6220 SEU6210
SED6220	I-D-S/I DATA QUERY FACILITY The I-D-S/I Data Query System Option permits access to an I-D-S/I data base from a time sharing terminal without having to actually write a program.	SES6200 SED6219 SEU6210 SEP6201 (SEC6204 or SES6201 or SES7201)
SED6229	DATA DICTIONARY/DIRECTORY SYSTEM FACILITY This is a comprehensive set of software components used to manage and provide information about an organizaion's data resource. The sytem provides reporting capability, and a user interface to maintain the data base.	SES6200

M.I.	DESCRIPTION	PREREQUISITES
SED6230	DATA DICTIONARY/DIRECTORY SYSTEM ON-LINE OPTION This option supplies predefinded menu driven forms for populating, maintaining and querying the dictionary data base. It supports the full Data Dictionary maintenance capabilities.	SES6200 SED6229
SED7008	DM-IV COMPREHENSIVE FACILITY This package includes: SED6205 DM-IV BASIC FACILITY SFL6201 COBOL-74 COMPILER AND RUNTIME FACILITY SED6206 DM-IV/TP FACILITY SED6207 DM-IV POLYGLOT QRP OPTION SED6208 DM-IV POLYGLOT PLP OPTION	SES6200 SEV6210 SEP6201
SED7009	DM-IV STANDARD FACILITY This facility includes: SED6205 DM-IV BASIC FACILITY SFL6201 COBOL-74 COMPILER AND RUNTIME FACILITY SED6206 DM-IV/TP FACILITY	SES6200 SEU6210
SED7015	DM-IV/TP EXTENSIONS (DUAL) This option provides dual processor capability for DM-IV/TP. This enhances throughput in a dedicated environment.	SES6200 SED6206
SEL6202	FORTRAN COMPILER AND RUNTIME FACILITY This FORTRAN compiler includes verbs which allow access from batch mode programs to an I-D-S/II integrated or indexed data base. All features of "FORTRAN Y" are retained.	SES6200 SEU6210
SEL6203	TSS BASIC LANGUAGE OPTION The BASIC compiler allows a time sharing user to create programs interactively. The BASIC compiler implements the language originally defined at Dartmouth.	SES6200 SEU6210 SEP6201 (SEC6204 or SES6201 or SES7201)

M.I.	DESCRIPTION	PREREQUISITES
SEL6204	RPG-II FACILITY This RPG-II compiler operating under GCOS provides a subset of the IBM System 370 DOS/VS and System 3 RPG-II functionality. Subject to some conversion limitations, this provides a tool for converting former IBM RPG-II sites to GCOS III products.	SES6200 SEU6210
SEL6205	FORTRAN-77 COMPILER AND RUNTIME FACILITY This is an extended FORTRAN-66 Process encompassing the functionality of the ANSI standard (X 3.9 - 1978) and the CII-HB Series 60 FORTRAN standard, a superset of the 1978 ANSI standard. This item is composed of a batch compiler, runtime facility, a time sharing interface, and a call interface forroutines written PL/1 and COBOL-74 standard. It includes also the Data Manipulation Language (DML) interface to IDS/II, including support for the FORTRAN Subschema Translator.	SES6200 SEU6210
SEL6218	TSS TEXT (TEX) TEX is a programming language extension to the text editor. TEX consists of a word processing ocmpiler language that combines editing, computing and resource management.	SES6200 SEU6210 SEP6201 (SEC6204 or SES6201 or SES7201)
SEL6219	TSS TEXT PROCESSING LIBRARY (TEXLIB) TEX Library I is an optional limited library of programs available for TEX. It consists of procedures, functions and stored processes such as "screen" menus.	SES6200 SEL6218 SEU6210 SEP6201 (SEC6204 or SES6201 or SES7201)
SEL6220	COBOL-68 COMPILER AND ISP FACILITY This facility provides the ability to compile and execute COBOL-68 programs as well as a callable interface to support the Indexed Sequential file access method.	SES6200 SEU6210

M.I.	DESCRIPTION	PREREQUISITES
SEL6222	FORTRAN-66 COMPATIBILITY OPTION FOR FORTRAN-77 This option provides source level compatibility for FORTRAN-77 programs.	SES6200 SEU6210 (SEL6205 or SEL7203)
SEL7202	APL INTERPRETER APL is a language for science and engineering. It provides extended problem solving abilities under Time-Sharing without requiring a sophisticated knowledge of programming.	SES6200 SEU6210 SEP6201 (SEC6204 or SES6201 or SES7201)
SEL7203	FORTRAN-77 COMPREHENSIVE FACILITY This package includes: SEL6205 FORTRAN-77 COMPILER AND RUNTIME SEP6205 FORTRAN-77 DEBUG SUPPORT OPTION SEL6222 FORTRAN-66 COMPATIBILITY	SES6200 SEU6210
SEL7212	LISP LISP is an interpreter/compiler system designed to assist in the symbolic computations common to language translation, theorem proving, symbolic mathematics, and artificaial intelligence. It is a compatible superset of LISP 1.5. It has a set of built-in functions defined in "Standard LISP".	SES6200 SEP6201 SEU6210 (SEC6204 or SES6201 or SES7201)

M.I.	DESCRIPTION	PREREQUISITES
SEL7213	PASCAL Honeywell's PASCAL Compiler provides the user with a powerful and versatile language, a favorite language of computre sciences today. It has good control structures, has powerful data structuring abilities, and produces efficient object programs. The Honeywell compiler is an independent implementation of the language, and not related to PASCALL ocmpilers on other machines. This product may be run under time sharing. TSS Facility (SEP6201) and NPS Basic System (SEC6204) or GRTS II Basic System (SES6201) are required. The Utility/Maintenance Facility (SEU6210) is required to support the above.	SES6200
SEL7214	B-LANGUAGE FACILITY Honeywell's Compiler B is a compiler for a powerful language that operates under GCOS time sharing. The language includes a good set of control structures (if-then-else, case, do while, etc.), supports recursive programming and modular programming. It is compatible with "industry-wide" B compilers.	SES6200 SEP6201 SEU6210 (SEC6204 or SES6201 or SES7201)
SEL7221	GENSYS - TAPE MANAGEMENT SYSTEM This is a Generation Control System which handles the retention and, if necessary, cycling of multiple generations of serial tape files. It also provides extensive facilities for the tape librarian and a comprehensive set of hardware and software-oriented tape security features. RPQ only	SES6200 SEU6210

M.I.	DESCRIPTION	PREREQUISITES
SEP6201	TIME SHARING FACILITY This facility makes certain GCOS capabilities available from a terminal. The following are some of the capabilities that are provided: build, edit and save permanent files; submit and interrogate the status of batch jobs; register users; manage FMS resources and permissions; format files as determined by embedded control information; and compile and execute FORTRAN and COBOL-74 programs in the time sharing environment, provided the appropriate language processor is used.	SES6200 SEU6210 (SES6201 or SEC6204 or SES7201)
SEP6203	COBOL-74 DEBUG SUPPORT OPTION The COBOL-74 Debug Support Option provides the ability to use the Debug Support Sytem (SEU6212) for symbolic debugging of COBOL-74 programs. This option enhances the compiler so that it may produce the required schema for such symbolic debugging.	SES6200 SFL6201 SEU6212 SEU6210 SEP6201 (SEC6204 or SES6201 or SES7201)
SEP6205	FORTRAN-77 DEBUG SUPPORT OPTION This option provides the interface to the Debug Support System (SEU6212), allowing both symbolic and nonsymbolic debugging, tracing and modification through interactive sessions or file driven debug sequences.	SES6200 SEU6210 SEU6212 SEL6205
SEP7201	TSS COMPREHENSIVE FACILITY This package includes: SEP6201 Time Sharing Standard Facility SEU6208 TSS Sort Option SEU6209 TSS Electronic Mail Option SEL6218 TSS TEXT Processing Option SEL6219 TSS TEXT Processing Library Option SEL6203 TSS BASIC Language Option	SES6200 SEU6210

M.I.	DESCRIPTION	PREREQUISITES
SER6200	COBOL-74 RUNTIME FACILITY The COBOL-74 Runtime Facility is designed for satellite and satellite-like systems that require only program execution while the actual program development and maintenance is done at the central system.	SES6200 SEU6210
SER6201	FORTRAN RUNTIME FACILITY The FORTRAN runtime facility contains the library routine necessary to execute a FORTRAN application program. It is intended for satellite and satellite-like systems.	SES6200 SEU6210
SER6202	PL/1 RUNTIME FACILITY The PL/I Runtime Facility contains the library routines necessary to execute PL/I application programs on satellite and satellite-like systems.	SES6200 SEU6210
SER6203	FORTRAN-77 RUNTIME FACILITY The facility allows execution of programs compiled under the FORTRAN-77 compiler and runtime. The FORTRAN-77 runtime facility is identical to the runtime facility contained in the FORTRAN-77 compiler and runtime facility (SEL6205).	SES6200 SEU6210
SES6200	GCOS III OPERATING SYSTEM EXECUTIVE This package consists of the nucleus of GCOS III and is sufficient to cold start a system, create or restore a file system, and esxecute previously assembled programs.	None

M.I.	DESCRIPTION	PREREQUISITES
SES6201	GRTS-II FACILITY GRTS-II is a front-end network processor supervisor which provides connectability and throughput through the use of extended memory (i.e. greater than 64KB - 128KB maximum). Ease-of-use features such as a fast loader, formatted dump, and macro based addition of non-standard terminals are provided. Terminals user compatibility with GRTS-I is provided.	SES6200 SEU6210
SES6202	TRANSACTION PROCESSING SYSTEM (TPE) FACILITY This facility provides a subexecutive which controls user-supplied Transaction Processing Application Programs (TPAPs). The executive controls remote I/O, scheduling of TPAPs and communication between TPAPs.	SES6200 SEU6210 (SEL6202 or SEL6220 or SFL6201) (SEC6204 or SES6201 or SES7201)
SES6208	PROGRAM NUMBER AS A RESOURCE OPTION Program Number as a Resource Option is a GCOS extension of the standard number assignement techniques for use primarily on systems that have extreme production-load requirements and is not recommended for use in a normal load environment. The first software release supporting this product is SR4JS1.	SES6200 SEU6210
SES7101 SES7102 SES7103 SES7104 SES7105 SES7106 SES7107 SES7108	EXPANDED SUPPORT ON SES6200 Expanded optional software support for GCOS III Operating System Executive SES6200. 1. Monthly expanded support charge (ESC) varies according to model and performance level. 2. If expanded support is elected for GCOS III Exec. SES6200, or for any software product offering expanded support, the expanded support must be elected for all system software products.	SES6200

M.I.	DESCRIPTION	PREREQUISITES
SES7201	GRTS FACILITY The General Remote Terminal Supervisor is available for Datanet 355 and Datanet 6600 with memory sizes from 32 Kbytes to 64 Kbytes. It supports a variety of terminals and remote computer devices.	
SEU6201	FILE GENERATION FACILITY This software allows the user to maintain multiple, date-specific version of the same file and provides selective access aand/or updates the desired version. Both GFRC and UFAS files can be maintained. First availability is software release ADF2.	SES6200 SEU6210
SEU6206	COLLECTION AND PLOT OF SYSTEM USAGE LEVELS (CAPSUL) CAPSUL is a privileged program which collects data from GCOS tables and writes three records to the Statistical Collection File (SCF). This data is then extracted and reduced at a convenient time, usually once a day, and then plotted. The CAPSUL reports and plots provide the systems custodian and operations manager with an overview of utilization of selected hardware and software units.	SES6200 SEU6210
SEU6208	TSS SORT OPTION This option extends the SORT capability to the time sharing user by providing an easy-to-use interactive interface.	SES6200 SEU6210 SEP6201 (SEC6204 or SES6201 or SES7201)
SEU6209	TSS ELECTONIC MAIL OPTION This option provides a time sharing user the ability to send and receive messages to and from other users.	SES6200 SEU6210 SEP6201 (SEC6204 or SES6201 or SES7201)

M.I.	DESCRIPTION	PREREQUISITES
SEU6210	UTILITY/MAINTENANCE FACILITY This package contains BMC, Utility, UTL2, a facility for managing software library in source and object format (SRCLIB, OBJLIB, LODLIB, LODPCH), GMAP, 355MAP, 355SIM. Filedit, Sysedit, master mode dump analyzer, FMS catalog cache, password encryption, and the sort/merge facility.	SES6200
SEU6211	DM-IV TP FORMS OPTION This option provides DM-IV TP users a method for creating and managing forms information. The forms are initially created and maintained in the Time Sharing environment. The form information is maintained in a library and is available via the COBOL COPY statement.	SES6200 SED6206 SFL6201 SEU6210 SED6205 SEL6209 SEP6201 (SEC6204 or SES6201 or SES7201)
SEU6212	DEBUG SUPPORT SYSTEM The Debug Support System offers symbolic (for PL/1 and COBOL 74) and nonsymbolic debug capabilities for user programs using a schema produced by various language processors to allow for symbolic references to data and procedure. Additionally, debugging at slave address and register content level is supported for any btch language. Debugging may be done interactively, via Time Sharing or via file input of the debug commands for batch programs. Symbolic debugging of COBOL-74 programs requires the COBOL-74 Debug Support Option (SEP6203) which is available as of release CB4.&. Symbolic debugging of FORTRAN-77 programs requires the FORTRAN-77 Debug Support Option (SEP6205).	SES6200 SEU6210 SEP6201 (SFL6201 or SFL6202) (SEC6204 or SES6201 or SES7201) (SEP6203 or SEP6205)
SEU6213	PERFORMANCE ANALYSIS AND REPORTING SYSTEM-PARS PARS collects system performance statistics and provides summary reports on a weekly, monthly, and yearly basis.	SES6200 SEU6210

M.I.	DESCRIPTION	PREREQUISITES
SEU7201	SLAVE PROGRAM ACTIVITY MONITOR SYSTEM/II (SPM/II) SPM/II is a software tool for monitoring slave programs. It enables program developers and users to gather performance data about their programs without disruption program operation. SPM/II dynamically samples instruction addresses for any slave activity during execution. Sample data is collected at time intervals selected by the user.	
SEV6201	DM-IV FORTRAN SUB-SCHEMA TRANSLATOR This option permits DM-IV data base subsets to be defined for use with Fortran and Fortran-77 application programs.	SES6200 SED6205 SEU6210 (SEL6202 or SEL6205)
SFC6201	EXTENDED FNP SUPPORT FACILITY This facility increases connectability to support up to eight FNPs on a single system.	SES6200 SEU6210 (SEC6204 or SES6201 or SES7201)
SFL6201	HOST TO HOST FILE TRANSFER FACILITY FOR DN 7100 This facility enables two or more Level 66 or DPS 8 systems to exchange files across a DSA network. The package includes an executive supporting transfers up to five different hosts. Interface to and control of this executive is via a user program calling a subroutine provided with the facility.	
SFL6201	COBOL-74 COMPILER AND RUNTIME FACILITY The COBOL-74 compiler operates in the multiprogramming environment under GCOS. This compiler conforms to the American National Standards Institute COBOL-74 and supports the Data Manipulation Language as well as the communication verbs.	SES6200 SEU6210

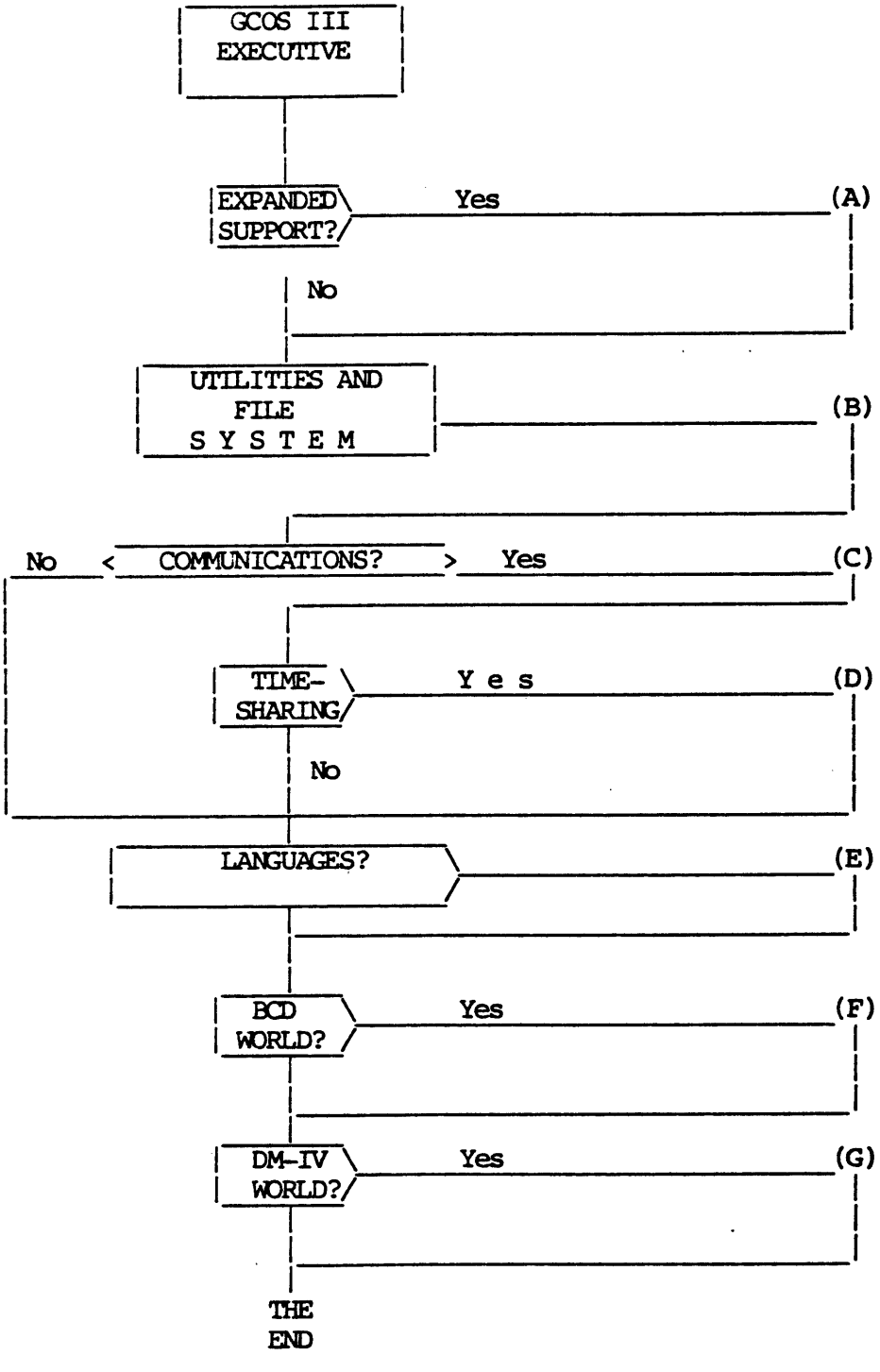
M.I.	DESCRIPTION	PREREQUISITES
SFL6202	PL/I COMPILER AND RUNTIME FACILITY The PL/I compiler is designed for commercial, scientific, and systems programming applications. GCOS PL/I conforms to the American National Standard PL/I.	SES6200 SEU6210
SFP6202	MANAGEMENT DATA QUERY SYSTEM/II (MDQS/II) MDQS/II provides the capability to extract and display data from GCOS III data files, with the exception of DM-IV files. It operates on sequential, index sequential (ISP), random, and itegrated data files (I-D-S/I) to retrieve data and perform report generation and computation.	SES6200 SED6219 SEU6210 SEP6201 (SEC6204 or SES6201 or SES7201)
SFP6204	MANAGEMENT DATA QUERY SYSTEM/IV (MDQS/IV)* MDQS/IV provides the capability to extract and display data files from GCOS III data files with the exception of DM-IV files. It operates on sequential, index sequential (ISP), random, and integrated data files to retieve data and perform report generation and computation (same as MDQS/II - SFP6202). Also it permits online file updating and procedural programming.	SES6200 SED6219 SEU6210 SEP6201 (SEC6204 or SES6201 or SES7201)
SFS6201	TRANSACTION DRIVEN SYSTEM (TDS) TDS is a multitasking, multiaccessing transaction processing subsystem that operates under GCOS, with the exception of the DM-IV environment. Included in SED6210.	SES6200 SED6219 SEL6220 SEU6210 (SEC6204 or SES6201 or SES7201)
SFS6202	TDS DUAL PROCESSOR OPTION The Dual Processor Option allows transaction processing tasks to utilize two processors at a time.	SES6200 SED6219 SEL6220 SEU6210 SFS6201 (SEC6204 or SES6201 or SES7201)

M.I.	DESCRIPTION	PREREQUISITES
SFU6210	GCOS III NETWORK ADMINISTRATION UTILITIES FOR DN 7100 This package includes the on-line utilities necessary to load and dump one or more DN 7100 front-end processors and to manage a network log file. Off-line utilities include a system generation verification program, a dump editor, a log editor and a network accounting package.	
SFU6212	FILE MANAGEMENT SYSTEM UTILITIES These utilities are intended to improve mass storage space managment and ultimately device and file space utilitization. This collection of utilities consists of: - Catalog Sort Utility, - System Master Catalog List Utility, - Statistics Report Generator Utility - Device Compactor Utility, - File Computer Utility.	

4.2.3

GCOS SUMMARY CONFIGURATOR

GCOS III CONFIGURATOR



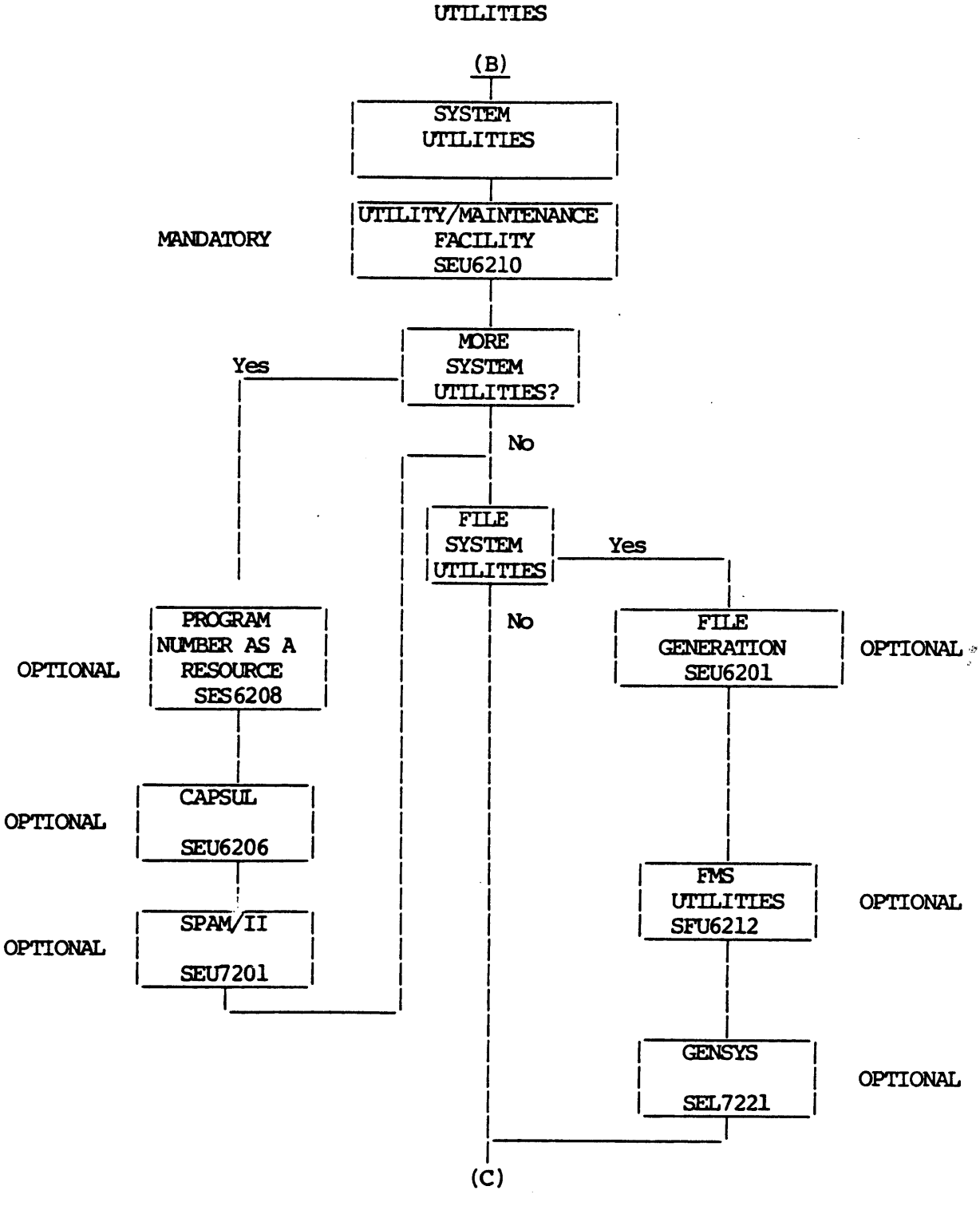
GCOS III CONFIGURATOR

EXPANDED SUPPORT

(A)

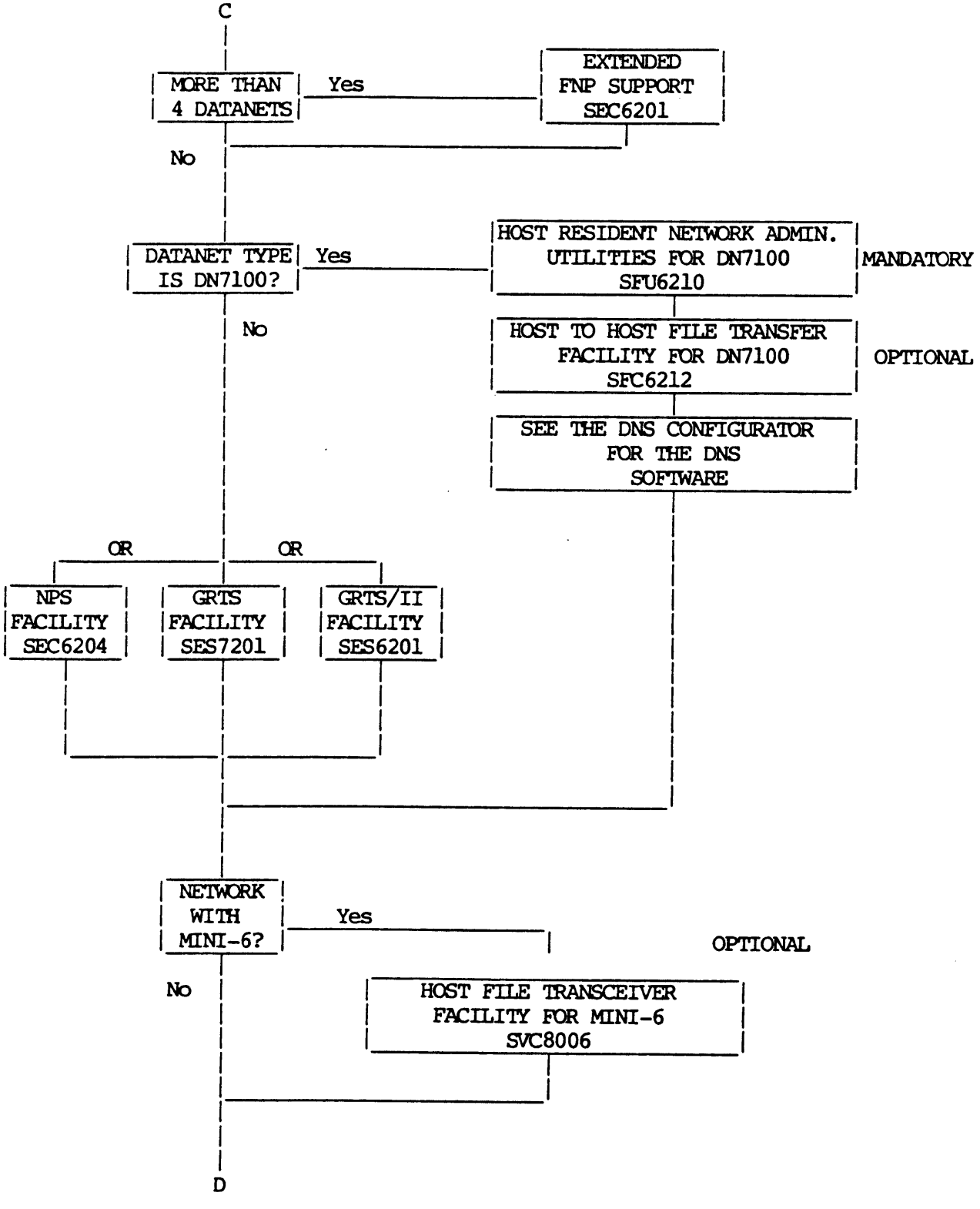
	PERFORMANCE CLASSIFICATION	EXPANDED SUPPORT
66/10, 66/20, 66/40, 66/60 66/07, 66/17, 66/27	LEVEL 1	SES7101 SES7104
3rd CP ON ABOVE LISTED SYSTEMS 4th CP ON ABOVE LISTED SYSTEMS	LEVEL 1, 2, 3	SES7107 SES7108
66/05, 66/10P, 66/20P, 66/40P	LEVEL 1	SES7101
2nd CP ON ABOVE LISTED SYSTEMS	LEVEL 1	SES7104
3rd CP ON ABOVE LISTED SYSTEMS 4th CP ON ABOVE LISTED SYSTEMS	LEVEL 1, 2, 3	SES7107 SES7108
66/60P, 66/80P	LEVEL 1	SES7102
2nd CP ON ABOVE LISTED SYSTEMS	LEVEL 2	SES7105
3rd CP ON ABOVE LISTED SYSTEMS 4th CP ON ABOVE LISTED SYSTEMS	LEVEL 1, 2, 3	SES7107 SES7108

GCOS III CONFIGURATOR

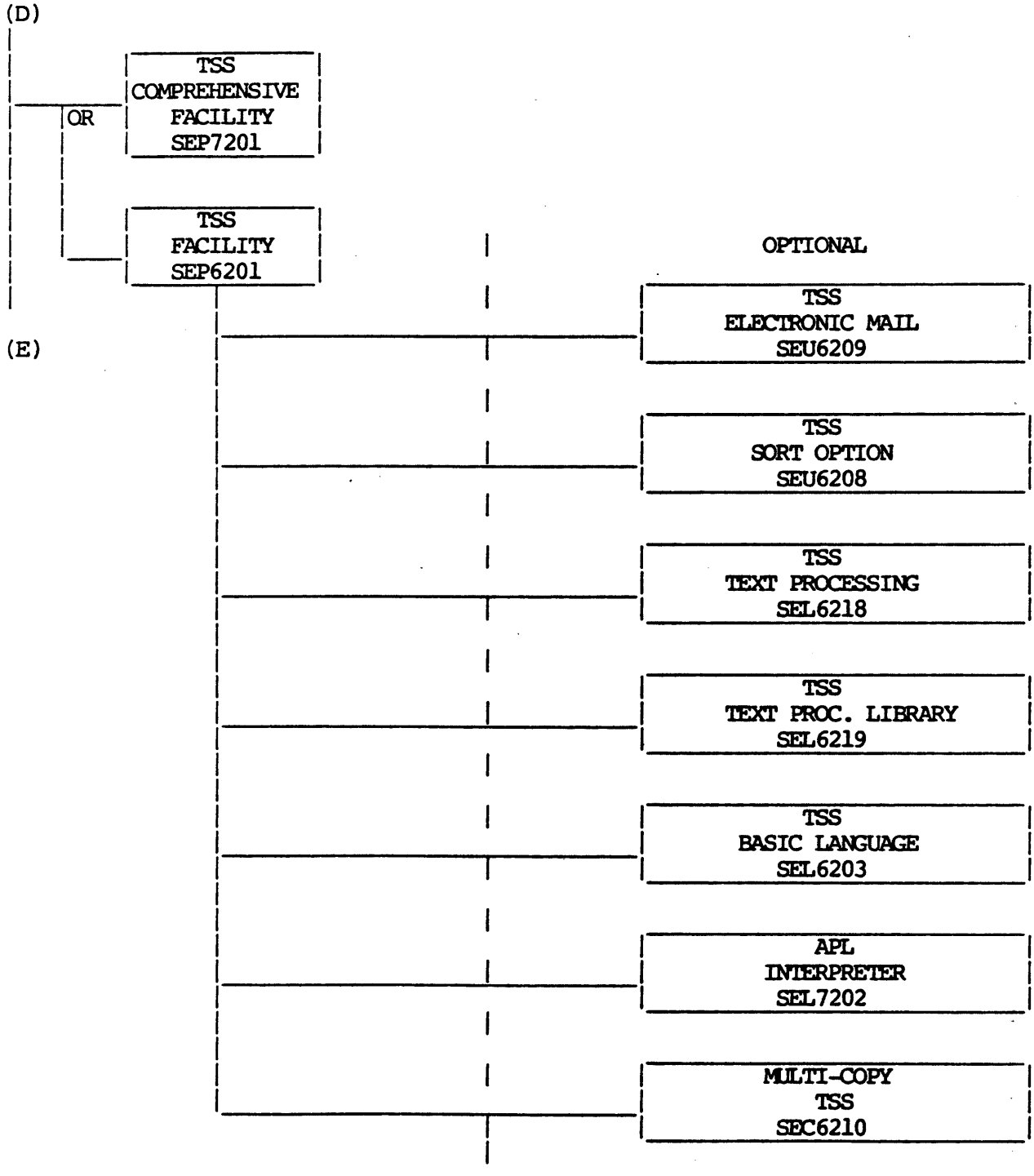


GCOS III CONFIGURATOR

COMMUNICATIONS

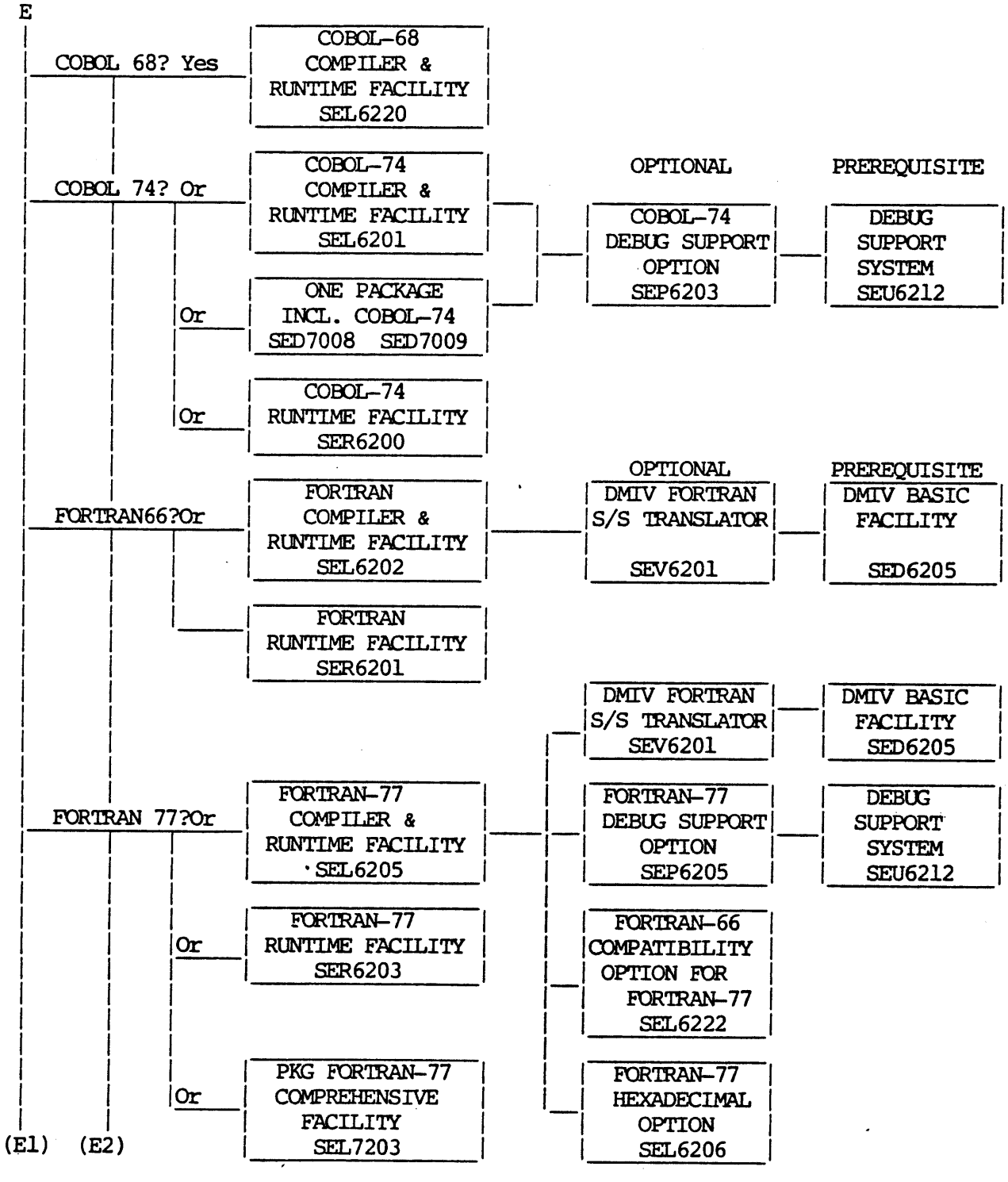


TIME-SHARING(TSS)



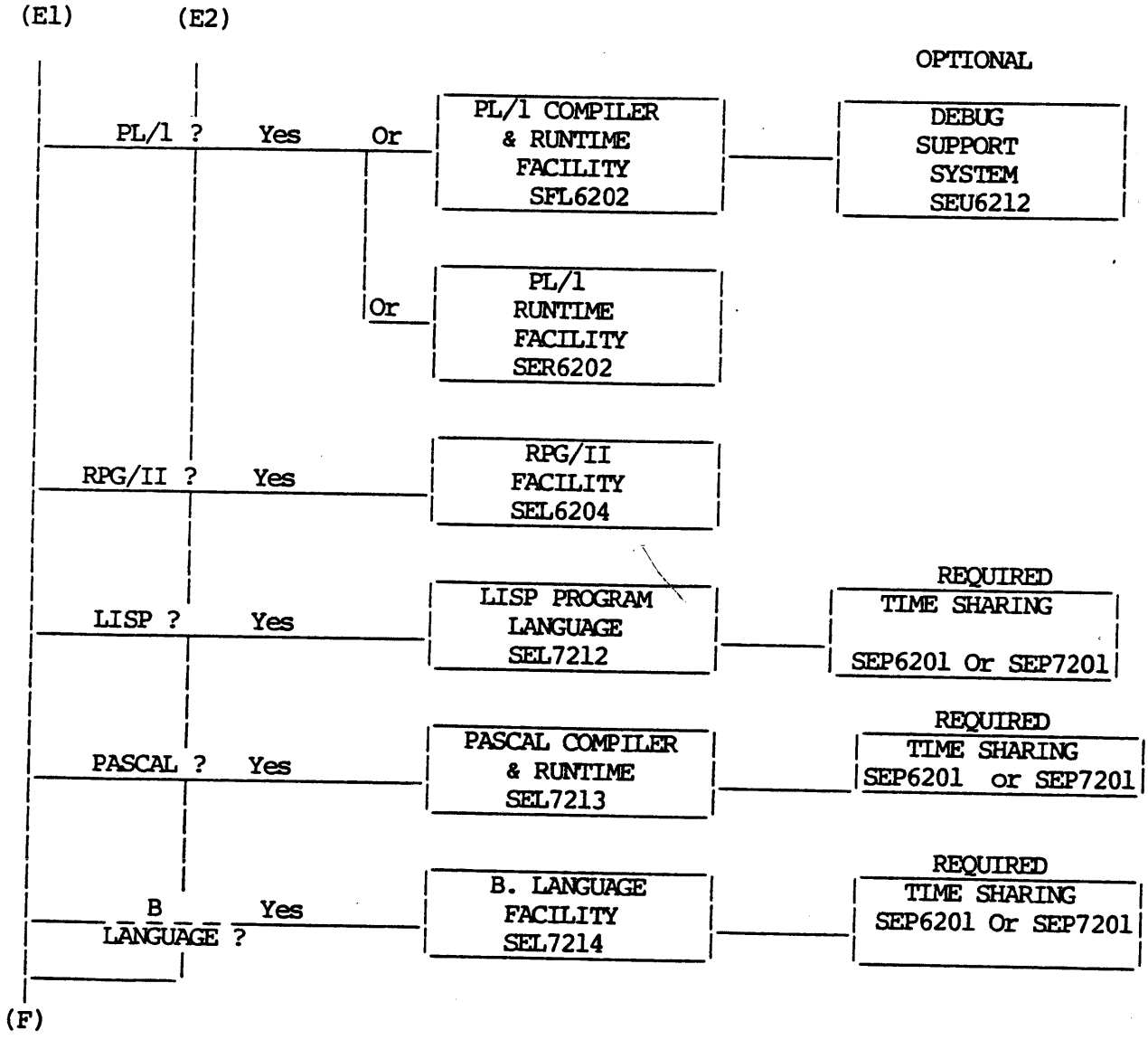
GCOS III CONFIGURATOR

LANGUAGES

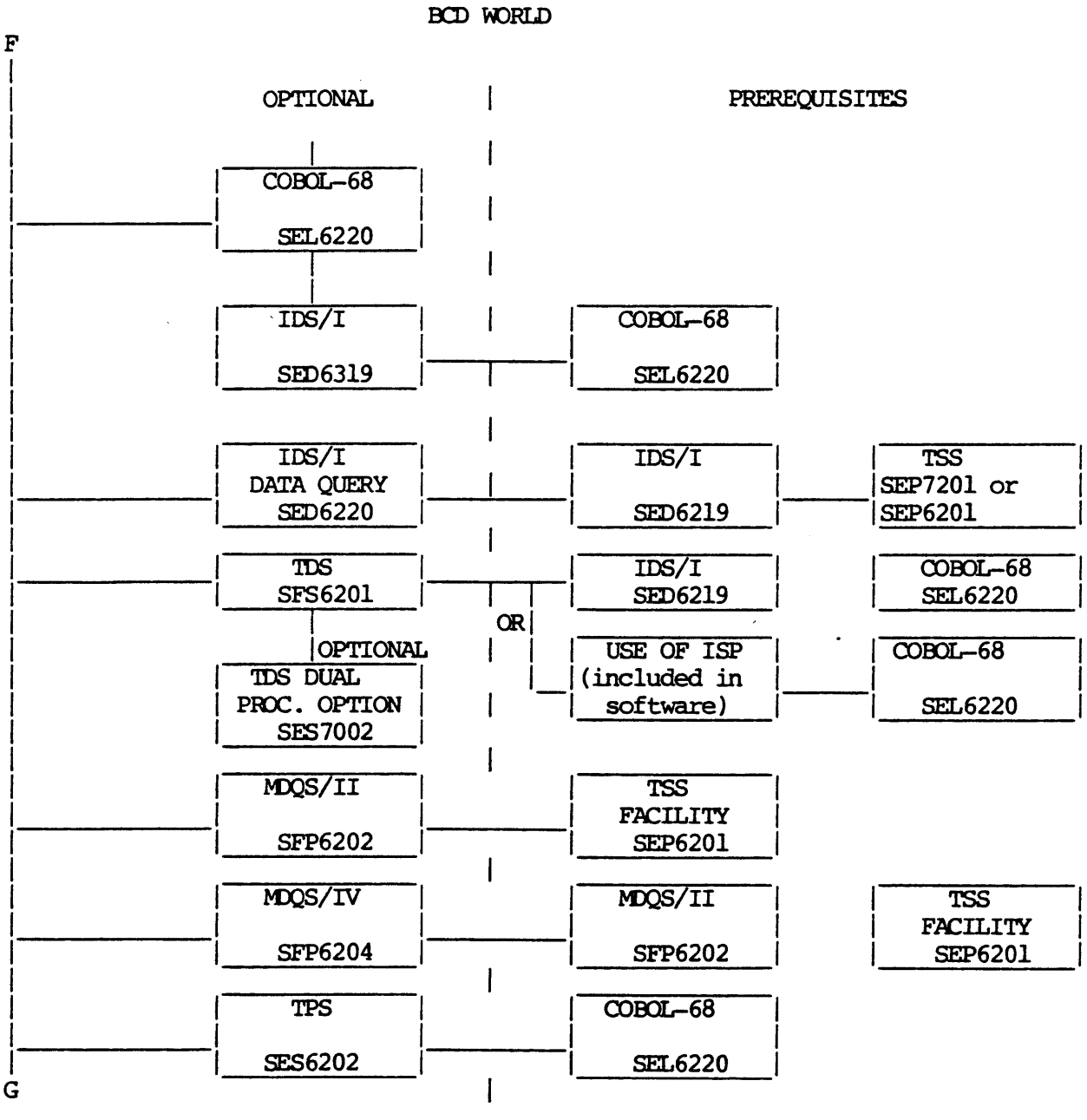


GCOS III CONFIGURATOR

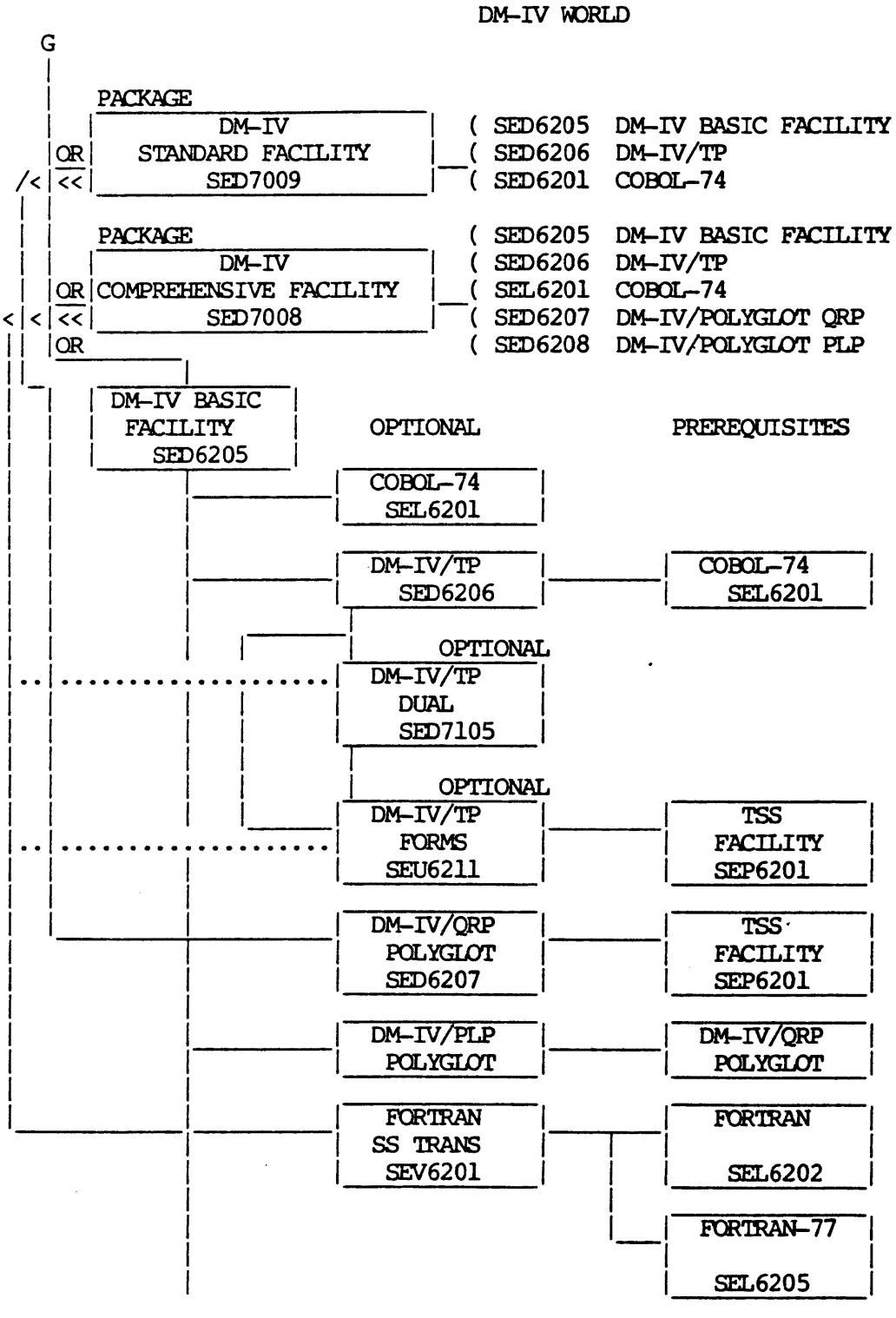
LANGUAGES(continued)



GCOS III CONFIGURATOR



GCOS III CONFIGURATOR



4.2.4

GCOS SUPPORT MATRIX

SOFTWARE SUPPORT MATRIX

MI	PRODUCT			4JS3
SFL6201	COBOL-74 Compiler + Runtime	CB3.1	CB4.0	CB4.1
SER6200	" Runtime	-	CR4.0	CR4.1
SEP6203	" Debug Option	-	CB4.0DS	CB4.IDS
SEL6220	COBOL-68 Compiler + Runtime		CZ1.0	CZ2.0
SEL6202	FORTRAN Compiler + Runtime	FT1.0	FT2.0	FT2.0
SER6201	" Runtime	-	FR2.0	
SEL6205	FORTRAN-77 Compiler + Runtime	-	-	FZ1.0
SER6203	" Runtime	-	-	FE1.0
SEP6205	" Debug Option	-	-	FZ1.0DS
SEL6206	" Hexadecimal	-	-	FZ1.0HEX
SEL6222	" Compatibility	-	-	FZ1.0FORTY
SLF6202	PL/1 Compiler + Runtime	PL3.0	PL3.1	PL3.1
SER6202	Runtime	-	PR3.1	PR3.1
SEU6212	DEBUG SUPPORT SYSTEM	DS1.0	DS2.0	DS2.1
SED6205	DM-IV Basic Facility	DB4.0	DB5.0	DB6.0
SEV6201	Fortran SS Translator	DB4.0FS	DB5.0FS	DB6.0FS
SED6206	DM-IB/TP	TA2.0	TA2.0	TA3.0
SED7015	Dual Processor	TA2.0DP	TA2.0DP	TA3.0DP
	Queued I/O	TA2.0QD	TA2.0QD	TA3.0QD
SEU6211	Forms	-	TA2.0F0	TA3.0F0
SED6207	DM-IV POLYGLOT QRP	MQ2.0	MQ2.1	MQ3.0
SED6208	PLP	MA2.0	MA2.1	MA3.0

SOFTWARE SUPPORT MATRIX

SFS6201	TDS	TD4.0	TD4.0	TD4.0
SFS7002	Dual Processor Option	TD4.0DP	TD4.0DP	TD4.0DP
SED6219	IDS/I Facility		ID1.0	ID2.0
SED6220	Data Query		ID1.0DQ	ID2.0DQ
SFP6202	MDQS/II	MT1.0	MT1.1	MT2.0
SFP6204	MDQS/IV	MF1.0	MF1.1	MF2.0
SES6202	TPE	TP1.0	TP1.0	TP2.0
SEU6201	File Generation	FG1.0	FG1.0	FG1.1
SFU6212	FMS Utility	-	-	FM1.0
SEU6210	Utility/Maintenance Facility		UM1.0	UM2.0
SEU6206	CAPSUL		CP3.0	CP3.2
SEP6201	TSS Facility		TZ1.0	TZ2.0
SEL6203	Basic Language		DT1.0	DT2.0
SEU6209	Electronic Mail	-	ML1.0	ML1.0
SEU6208	Sort		ST1.0	ST1.0
SEL6218	TEX	WP1.0	WP1.0	WP2.1
SEL6219	TEX Library	WL1.0	WL1.0	WL1.1
SES6201	GRTS-II	SG1.0	SG1.2	SG2.0
SEC6204	NPS	NT3.0	NT3.0	NT3.0
SED6229	Data Dictionary Basic Facility	-	-	DD1.0
SED6230	Data Dictionary Online Option			DD1.0DL

4.4.1

PACKAGING SUMMARY

SECTION 4.4.1
JUNE 1984
APPLICATIONS PACKAGING SUMMARY

PACKAGING SUMMARY

MANAGEMENT SCIENCES

AES0018 MATHEMATICAL PROGRAMMING SYSTEM - MPS

>Includes:
AES0015 MPS/BASIC SYSTEM
AES0016 MPS/MIXED INTEGER PROGRAMMING FEATURE
AES0017 MPS/GENERALIZED UPPER BOUND FEATURE
AES0004 MPS/COMMON FILE MANAGEMENT SYSTEM

AES0005 GENERAL PURPOSE SIMULATOR SYSTEM (GPSS)

AES0012 COORDINATE GEOMETRY - COGO

AES0013 ASTRA/II

AES0019 TIME-SHARING APPLICATION LIBRARY

AES0020 SIMSCRIPT

AES0026 STATPAC

AES7001 SIMULA COMPILER

MANUFACTURING

AVM0060 HMS - INVENTORY RECORD MANAGEMENT

AVM0061 HMS - MANUFACTURING DATA CONTROL

AVM0062 HMS - MATERIAL REQUIREMENT PLANNING

AVM0063 HMS - MASTER PRODUCTION SCHEDULING

AVM0064 HMS - STATISTICAL FORECASTING

AVM0065 HMS - CAPACITY REQUIREMENTS PLANNING

INFORMATION RETRIEVAL

AEP0020 MISTRAL BASIC SYSTEM

AEP0021 MISTRAL INTERACTIVE TEXT ENTRY

AEP0022 MISTRAL-SYMPHONIE DISTRIBUTED TEXT EXCHANGE FACILITY

AEP0023 MISTRAL IV (SIRIS 8) TO MISTRAL BASIC UPGRADE KIT

FINANCIAL ANALYSIS

AES9010	FCS BASIC SYSTEM INCLUDING STATISTICS
AES9012	HEIRARCHICAL CONSOLIDATION
AES9013	RISK ANALYSIS
AES9014	RENUMBERING

4.4.2

APPLICATIONS SOFTWARE LISTING

4.4.2 APPLICATIONS SOFTWARE LISTING

The following Applications Software Listing is arranged by Marketing Identifier in alphanumeric sequence. The software products listed under prerequisites are those required to run the described product.

M.I.	DESCRIPTION	PREREQUISITES
AEP0010	MISTRAL -IV MISTRAL is an information retrieval system which provides all the features needed to store, retrieve and distribute documents for people working in just about any field of activity.	SES6200
AES0004	MATHEMATICAL PROGRAMMING SYSTEM (MPS) - COMMON FILE MANAGEMENT SYSTEM (CFMS) A technique for optimizing a course of action subject to restrictions and constraints, for example: helping minimize cost of operating a refinery while meeting demand, supply and production capability restrictions. Provides matrix generation, report writing and database manipulation capabilities. For ease of use in entering data, interacting with an executing program, and on-line interrogation of results, the Time Sharing Facility (SEP6201 and GRTS-II Basic System (SES6201) or NPS Basic System (SEC6204) are desirable.	AES0015 (SEL6202 or SER6201) SES6200 SEU6210
AES0005	GENERAL PURPOSE SIMULATOR SYSTEM (GPSS) GPSS is used for modeling discrete activities of operations in industry and government. It can aid in design of systems, processes, manufacturing plans, and physical distribution activities. SEL6202 required if FORTRAN coded HELP routines are used. For ease of use in entering data, interacting with an executing program, and on-line interrogation of results, the Time sharing Facility (SEP6201) and GRTS II Basic System (SES6201) or NPS Basic System (SEC6204) are desirable.	(SEL6202 or SER6201) SES6200 SEU6210
AES0012	COORDINATE GEOMETRY (COGO) COGO is a double-precision FORTRAN program that solves civil engineering geometric problems such as horizontal alignments, vertical profiles, distance, areas, angles, coordinates of unknown points and traverses.	(SEL6202 or SER6201) SES6200 SEU6210 SEP6201 (SEC6204 or SES6201)

M.I.	DESCRIPTION	PREREQUISITES
AES0013	Automatic Scheduling with timed resource allocation (Astra II). ASTRA II provides automatic scheduling with timed resources allocation for project control in addition to PERT-like precedence relationships. It applies defined resources against identified requirements in a time-related sequence. ASTRA II provides additional capabilities in reporting and networking and resource capacity. For ease of use in entering data, interacting with an executing program, and on-line interrogation of results, the Time-Sharing Facility (SEP6201) and GRTS II Basic System (SES6201) or NPS Basic System (SEC6204) or DNS are desirable.	(SEL6202 or SER6201) SES6200 SEU6210
AES0015	MATHEMATICAL PROGRAMMING SYSTEM (MPS) - COMMON FILE MANAGEMENT SYSTEM (CFMS) A technique for optimizing a course of action subject to restrictions and constraints, for example: helping minimize cost of operating a refinery while meeting demand, supply and production capability restrictions. Provides matrix generation, report writing and database manipulation capabilities. For ease of use in entering data, interacting with an executing program, and on-line interrogation of results, the Time Sharing Facility (SEP6201) and GRTS-II Basic System (SES6201) or NPS Basic System (SEC6204) are desirable.	(SEL6202 or SER6201) SES6200 SEU6210

M.I.	DESCRIPTION	PREREQUISITES
AES0016	MATHEMATICAL PROGRAMMING SYSTEM (MPS) - MIXED INTEGER PROGRAMMING (MIP) FEATURE A technique for optimizing a course of action subject to restrictions and constraints, for example: helping minimize cost of operating a refinery while meeting demand, supply and production capability restrictions. Extends Basic System to handle problems where some variables are constrained to take on only integer values. For ease of use in entering data, interacting with an executing program, and on-line interrogation of results, the Time Sharing Facility (SEP6201) and GRTS-II Basic System (SES6201) or NPS Basic System (SEC6204) are desirable.	AES0015 (SEL6202 or SER6201) SES6200 SEU6210
AES0017	MATHEMATICAL PROGRAMMING SYSTEM (MPS) - GENERALIZED UPPER ROUND (GUB) SYSTEM A technique for optimizing a course of action subject to restrictions and constraints, for example: helping minimize cost of operating a refinery while meeting demand, supply and production capability restrictions. Extends Basic System to handle problems that can be formulated with GUB, or as transportation problems. For ease of use in entering data, interacting with an executing program, and on-line interrogation of results, the Time Sharing Facility (SEP6201) and GRTS-II Basic System (SES6201) or NPS Basic System (SEC6204) are desirable.	AES0015 (SEL6202 or SER6201) SES6200 SEU6210
AES0018	MATHEMATICAL PROGRAMMING SYSTEM Package including: AES0015 MPS/BASIC AES0016 MPS/MIP AES0017 MPS/GUB AES0004 MPS/CFMS	SES6200 SEU6210 (SEL6202 or SER6201)

M.I.	DESCRIPTION	PREREQUISITES
AES0019	TIME SHARING APPLICATION LIBRARY A collection of user-developed solution programs for applications in the time sharing environment. The programs are prepared and documented by four fields of use: mathematical, statistics, industry, and business/finanace.	SEL6202 SEL6203 SES6200 SEP6201 (SEC6204 or SES6201) SEU6210
AES0020	SIMSCRIPT A discrete simulation system used for modeling process operations in industry and government. It can aid in design and analysis of systems, processes, manufacturing plans, and physical distribution activities. For ease of use in entering data, interacting with an executing program, and on-line interrogation of results, the Time Sharing Facility (SEP6201) and GRTS-II Basic System (SES6201) or NPS Basic System (SEC6204) are desirable.	(SEL6202 or SER6201) SES6200 SEU6210
AES0026	STATPAC	
AES7001	SIMULA COMPILER The implementation of the SIMULA compiler is based on SIMULA 67, a general purpose programming language developed by the Norwegian Computing Center in Oslo. SIMULA is one of the most advanced simulation languages. It introduces the quasi-parallel execution and the class concept, which makes it equally suitable for simulation programs and for programs containing numerical calculations, symbol manipulations, list structures and text handling.	SES6200

M.I.	DESCRIPTION	PREREQUISITES
AVM0060	INVENTORY RECORD MANAGEMENT MODULE (HMS) Provides basic inventory accounting capability. It includes database initialization, material item maintenance, perpetual inventory record maintenance (issues, receipts, adjustments, on-order, etc.), stock status reporting, ABC Analysis, and cycle counting. To process transactions on-line, DMIV Transaction Processor (SED6206), DMIV TP Forms Option (SEU6211), Time Sharing Facility (SEP6201) and GRTS II Basic System (SES6201) are needed.	SFL6201 SEL6209 SES6200 SED6205 SEU6210
AVM0061	MANUFACTURING DATA CONTROL MODULE (HMS) Establishes and maintains product structures and production processes. The product structure function covers all material items from top level end items, through major assemblies, parts, and raw material. The production process function maintains material routing data, including the relationship of component material to operation, and work center operation information. Full Cost Implosion capability is also included. To process transactions on-line, DMIV Transaction Processor (SED6206), DMIV TP Forms Option (SEU6211), Time Sharing Facility (SEP6201) and GRTS II Basic System (SES6201) are needed.	AVM0060 SFL6201 SEL6209 SES6200 SED6205 SEU6210
AVM0062	MATERIAL REQUIREMENTS PLANNING MODULE (HMS) Provides for net change material requirements planning of selected material items. With this module new supply orders may be generated or existing orders may be identified for user rescheduling or cancellation as appropriate. It also provides demand entry, order release, feedback, and reporting. To process transactions on-line, DMIV Transaction Processor (SED6206), DMIV TP Forms Option (SEU6211), Time Sharing Facility (SEP6201) and GRTS II Basic System (SES6201) are needed.	AVM0060 AVM0061 SFL6201 SEL6209 SES6200 SER6205 SEU6210

M.I.	DESCRIPTION	PREREQUISITES
AVM0063	MASTER PRODUCTION SCHEDULING MODULE (HMS) Helps management establish a master schedule that plans production rates and material requirements to meet business objectives. This module provides the time-phased load on critical resources that corresponds to a specific master schedule. Once approved the master schedule is fully integrated with Material Requirements Planning.	AVM0060 AVM0061 AVM0062 SFL6201 SEL6209 SES6200 SED6205 SEU6210
AVM0064	STATISTICAL FORECASTING MODULE (HMS) Calculates a forecast of future demands. This module is designed to be used in conjunction with Material Requirements Planning and Master Production Scheduling modules, and based upon integrated information, uses exponential smoothing and an optional seasonal base to calculate the forecast. It includes a database maintenance feature to input available forecast data and an output report to show how the calculations were made and their results.	AVM0060 AVM0061 AVM0062 SFL6201 SEL6209 SES6200 SED6205 SEU6210
AVM0065	CAPACITY REQUIREMENTS PLANNING MODULE (HMS) Provides capacity requirements planning and shop floor control. Included in these functions are detailed operation scheduling of shop orders from preplanned or special routings, workcenter loading, shop order priority calculations and maintenance, and the monitoring of all phases of shop performance based upon actual shop feedback. To process transactions on-line, DMIV Transaction Processor (SED6206), DMIV TP Forms Option (SEU6211), Time Sharing Facility (SEP6201) and GRTS II Basic System (SES6201) are needed.	AVM0060 AVM0061 SFL6201 SEL6209 SES6200 SED6205 SEU6210

4.5

SRPQ ITEMS

4.5 SRPQ ITEMS

The following products are available only on SRPQ in order for the distribution of the products to be adequately controlled.

An SRPQ should be submitted for each customer requiring any of these proucts.

M.I. DESCRIPTION PREREQUISITES

4.5 SRPQ ITEMS

The following products are available only on SRPQ in order for the distribution of the products to be adequately controlled.

An SRPQ should be submitted for each customer requiring any of these proucts.

M.I.	DESCRIPTION	PREREQUISITES

PREREQUISITES

	GCOS	GCOS8
GCOS SEC6205 GCOS8 SVC8003		
NPS HDLC OPTION	SES6200 SEU6210 SEC6204	SVS8000 SVP8000 SVC8002 SVU8002
The NPS HDLC option allows connection of Mini 6, L6/06, and RNP707 (RN400) systems using LHDLC full duplex protocols. NPS HDLC is also available for NPS to NPS connections for system to system operations. . File to file transfer (program FTF 626). . Terminal to alternate host which allows a terminal connected to one NPS system to access a host system connected via a second NPS system.		
GCOS SEC6203 GCOS8 SVC8001		
GRTS II HDLC OPTIONS	SES6200 SEU6210 SES6201	SVS8000 SVP8000 SVC8000 SVU8002
The GRTS II HDLC option allows the connection of Mini-6/MFS system for file transfer, remote batch, and concentration using LHDLC line protocol		

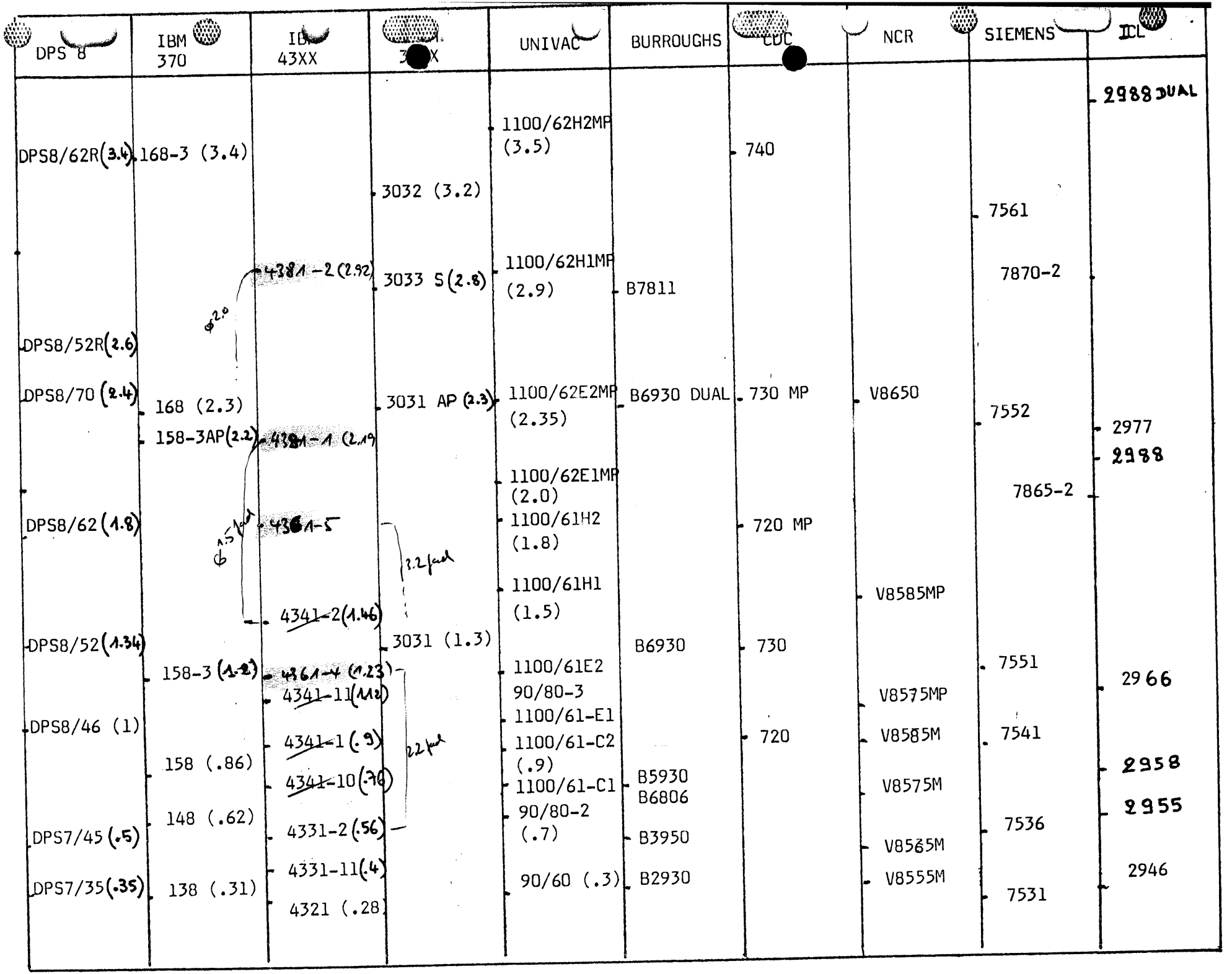
6. COMPETITIVE INFORMATION

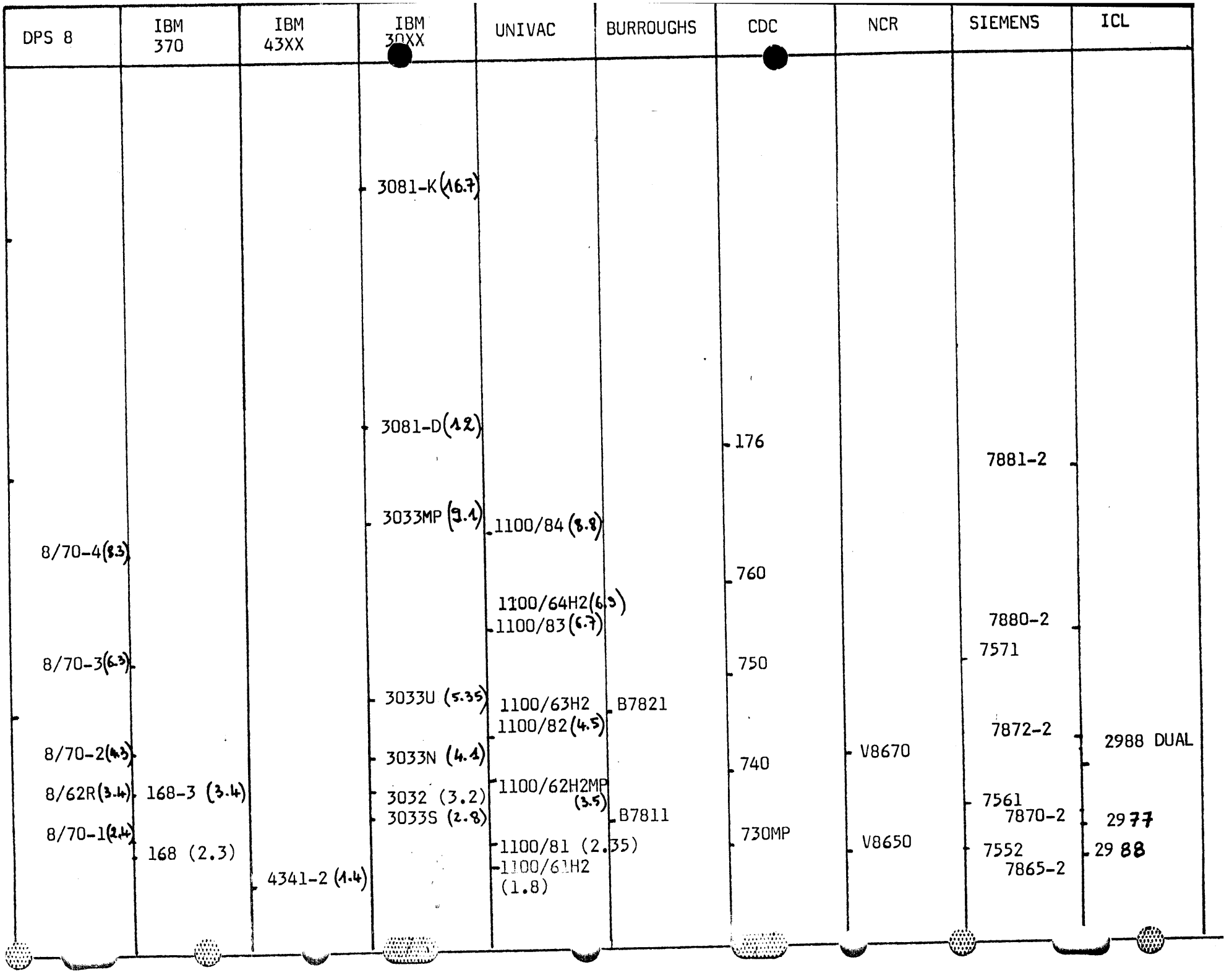
6.1. COMPARATIVE PERFORMANCE CHART

6.2. COMPETITION NEWS

6.3. CONVERSION AIDS

6.1. COMPARATIVE PERFORMANCE CHART


DPS 8
IBM 370
IBM 43XX
3XXX
UNIVAC
BURROUGHS
CDC
NCR
SIEMENS
ICL
2988 DUAL
1100/62H2MP (3.5)
DPS8/62R (3.4)
168-3 (3.4)
740
3032 (3.2)
7561
3
4381-2 (2.92)
3033 S (2.8)
1100/62H1MP (2.9)
B7811
7870-2
ϕ2.0
DPS8/52R (2.6)
DPS8/70 (2.4)
168 (2.3)
3031 AP (2.3)
1100/62E2MP (2.35)
B6930 DUAL
730 MP
V8650
7552
2977
158-3AP (2.2)
4381-1 (2.19)
2988
2
1100/62E1MP (2.0)
7865-2
DPS8/62 (1.8)
ϕ1.5 fuel
4361-5
1100/61H2 (1.8)
720 MP
2.2 fuel
1100/61H1 (1.5)
V8585MP
4341-2 (1.46)
DPS8/52 (1.34)
3031 (1.3)
B6930
730
158-3 (1.2)
4361-4 (1.23)
1100/61E2
7551
2966
4341-11 (1.12)
90/80-3
V8575MP
1
1100/61-E1
DPS8/46 (1)
4341-1 (.9)
1100/61-C2 (.9)
720
V8585M
7541
2.2 fuel
158 (.86)
2958
4341-10 (.76)
1100/61-C1
B5930
B6806
V8575M
148 (.62)
90/80-2 (.7)
2955
4331-2 (.56)
B3950
7536
DPS7/45 (.5)
V8565M
4331-11 (.4)
90/60 (.3)
B2930
2946
DPS7/35 (.35)
138 (.31)
V8555M
4321 (.28)
7531


DPS 8
IBM 370
IBM 43XX
IBM 30XX
UNIVAC
BURROUGHS
CDC
NCR
SIEMENS
ICL
15
10
5
3081-K (16.7)
3081-D (12)
3033MP (9.1)
1100/84 (8.8)
8/70-4 (8.3)
1100/64H2 (6.9)
1100/83 (6.7)
8/70-3 (6.3)
3033U (5.35)
1100/63H2
B7821
1100/82 (4.5)
8/70-2 (4.3)
3033N (4.1)
8/62R (3.4)
168-3 (3.4)
1100/62H2MP (3.5)
3032 (3.2)
3033S (2.8)
B7811
8/70-1 (2.4)
168 (2.3)
1100/81 (2.35)
4341-2 (1.4)
1100/61H2 (1.8)
176
760
750
740
730MP
V8670
V8650
7881-2
7880-2
7571
7872-2
7561
7870-2
7552
7865-2
2988 DUAL
2977
2988

Bull

< HP oberhalb

> HB oberhalb

H P 3000

DPS 8/47	<	3000-68
66/DPS 05	<	
DPS 8/49	>	

≈ 50 %	>	3000-48
≈ 70 %	>	3000-42
≈ 85 %	>	3000-39

Bull

≙ = e[illegible]
> = HB oberhalb
< = IBM oberhalb

I B M :

SERIE 43XX

DPS 8/47 S / DPS 05	≙	4361-4
DPS 8/49 + 52 S	≙	4361-5
DPS 8/62 S	≙	4381-1
DPS 8/70 S	≙	4381-2

SERIE 3083

DPS 8/70 Dual	<	3083-E
DPS 8/70 Q	>	3083-B
DPS 88/81	≙	3083-J

SERIE 3081 (neu)

DPS 88/81	<	3081-D
DPS 88/81	<	3081-G
DPS 88/82	≙	3081-K
DPS" 88/84 (Q) "	≙	3084

CII-HB	IBM4341	UNIVAC	BURROUGHS	NCR	CDC	ICL	SIEMENS
DPS8/62	4341-12	1100/71-H2	B6925 x 2		170/835		S7552
			B4955			2988	
		1100/71-H1					
	4341-2	1100/71-E2					
DPS8/52							
DPS8/49	4341-11	1100/71-E1	B6925	V8595-II	170/825		S7551
	4341-1	1100/71-C2				2966	
				V8585-II			
DPS8/47	4341-10	1100/71-C1			170/815		
			B5935			2958	S7541
	4341-09	1100/71-B1	B3955	V8575-II			
						2957	S7536
				V8565-II		2946	

CII-HB	IBM308X	UNIVAC	BURROUGHS	NCR	CDC	ICL	SIEMENS
		1100/93			170/875 DUAL		7890-L
	3081-K						
88/82		1100/92	B7900 K			ATLAS 15	7890-F
	3081-G				170/875		7890-E
			B7900 H				
	3083-J						7890-D
88/81		1100/91			170/865		7880-2
8/70-4							
	3083-B	1100/64-H2	B7900F		170/855		
8/70-3		1100/63-H2					
	3083-E		B7850				7875-2
8/70-2				V8670			
		1100/72-H2	B7830		170/835	2988 DUAL	7870-2
8/70-1				V8650			7865-2

N | Oktober 1982

Meldung

Leistungsbarometer

DPS 8/ 88 und der Mitbewerb

in MA geführt unter: 0 0 0 0 0 1 0 7 4 0 1

Scala	HB	IBM	Siemens	Univac	Amdahl	MAS
15						
14						
13						
12	DPS 88/84 28 MIPS	3084 22 MIPS				
11			7.890 S	1100/94		
10						
9						
8			7.890 L	1100/93	5880 22 MIPS	
7	DPS 88/82 15 MIPS					
6		3081 K (2P) 14,7 MIPS	7.890 F	1100/92	5870 22 MIPS	AS/9080 2P 20 MIPS
5		3081 G	7.890 E			
		3083 J (1P)				
4	DPS 88/81 8 MIPS	3033AP/MP		1100/91		
			7.890 D		5860 1P 13 MIPS	
3		3083 B (1P)				AS/9060 1P 11 MIPS
2	DPS 8/70D	3033U/3083E (1P)				
	DPS 8/62D	3033 N				
1	DPS 8/52D	4381-2 3033S				

Die noch nicht offiziell angekündigte 4-Proz.-Version der DPS 88 wird mit 28 MIPS das größte kommerziell einzusetzende System sein und knapp 1 MIPS über der IBM 3084 liegen.

Kaleidoskop der Nichtkompatiblen

Die Palette an Großrechnern, die nicht kompatibel zu IBM-Computern sind, ist ebensogroß, wie das Angebot an Systemen der IBM-Welt, inklusive der steckerkompatiblen Mitläufer (Online 9/83, Seite 26). Anbietern wie Burroughs, Control Data, Honeywell Bull, NCR und Sperry, aber auch den Miniproduzenten sagen amerikanische Marktforscher schwere Zeiten voraus, da der Marktführer mit neuen Rechnern der mittleren Leistungsklasse deren Kundenpotential knacken will.

Ende 1983 stellt sich der weltweite Großrechner-Markt, der in unserer Tabelle bei dem (Klein-)Rechner IBM 4321 beginnt, wie folgt dar: Rund 67% Anteil hält die IBM und etwa 17% halten die IBM-kompatiblen Anbieter. Also knapp 84% gehören der IBM-Welt an. Den Rest teilen sich Honeywell Bull (6%), Sperry (5%), Burroughs (1,5%), NCR (1%) und Control Data (3%). Die amerikanische Gartner Group »verteilt« den weltweiten Mainframe-Umsatz wie folgt: 1982, mit rund 50 Mrd. Dollar, 59% die IBM, 33% die Nichtkompatiblen und 8% die PCM. Bis 1987 gibt es nach ihren Aussagen eine Verschiebung: 56% des geschätzten Umsatzes von 110 Mrd. Dollar hält die IBM, 30% die Nichtkompatiblen und 14% die PCM-Industrie.

ÖVD/Online 1/84

Hersteller/ Modell	Relative Leistung nach IDC	Durchsatz (MIPS)	Hauptspeicher (MB)	Pufferspeicher (kB)	Känale
HB DPS 4/82	/	0,12–0,48	0,5–8	–	Busstruktur
HB System 6/54	12	0,2	0,2–1	–	Busstruktur
NCR V-8545	12	0,2	1–2	–	1–6
SP System 80-3	12	0,2	0,2–4	–	1–3
SP System 80-4	14	0,2	0,5–4	–	1–3
NCR V-8555	17	0,25	1–4	–	1–6
SP System 80-5	18	0,26	0,2–4	–	1–3
BUR B1955	19	0,27	0,5–2	8	4–15
HB System 6/74	20	0,3	0,5–2	8	Busstruktur
NCR V-8565	21	0,37	2–6	–	1–8
SP System 80-6	21	0,37	0,5–4	–	1–3
HB DPS 7/35	25	0,4	1–3	–	2–4
SP 1100/71-B1	30	0,54	2–32	–	5–28
BUR B 2925	31	0,55	1–2	–	5–16
HB DPS 7/45	31	0,55	2–4	–	2–6
NCR V-8575	34	0,6	4–6	–	1–6
BUR B 5920	34	0,6	3,1–6,2	–	5–20
CDC Cyber 170/185	/	0,7	0,2–1	–	12–24
HB DPS 8/47	41–72	0,7–1,2	2–32	32	20
SP System 80-8	42	0,7	1–8	–	1–8
NCR V-8585	42	0,7	4–6	–	1–6
HB System 6/76	45	0,75	0,5–2	8	Busstruktur
HB System 6/9x	45	0,75	1–16	8	Busstruktur
NCR V-8595	46	0,77	4–6	–	6
SP System 90/80-3	46	0,78	1–8	32	2–8
HB DPS 7/55	48	0,8	2–4	–	4–8
NCR V-8635	51	0,9	4–8	32	8
HB DPS 7/60	69	1,1	2–4	–	4–12
HB DPS 7/65	69	1,1	2–4	–	4–8
CDC Cyber 170/825	/	1,2	0,2–1	–	12–24
SP 1100/71-H1	70	1,2	2–32	32	5–28
BUR B 6925	76	1,2	3,1–6,2	–	6–64
HB DPS 7/60-P	78	1,3	2–4	–	4–12
HB DPS 7/70	80	1,6	2–4	–	4–12
HB DPS 8/49	61–208	1,6–6,4	2–32	32	20
HB DPS 8/52	61–220	1,8–3,6	2–32	32	20
NCR V-8645	96	1,9	4–16	128	8
NCR V-8655	100	1,9	8–16	64	16
HB DPS 7/80	120	2,1	3–4	–	4–20
BUR B 4955	120	2,1	5	142	8–64
SP 1100/72-H1	130	2,2	2–32	64	5–28
HB DPS 8/62	82–295	2,3–4,6	2–32	32	20
CDC Cyber 170/835	/	2,6	0,5–2	2–4	12–24
HB DPS 8/70	107–385	2,6–5,2	2–64	32	10–40
NCR V-8665	140	3	8–24	160	16
SP 1100/73-H1	150	3,4	2–32	96	10–42
NCR V-8675	180	4,1	8–32	256	16
SP 1100/74-H1	200	4,3	2–32	128	10–56
CDC Cyber 170/845	/	4,5	0,5–2	2–4	12–24
BUR B 7900-F	277	5,7	12–96	18	7–100
NCR V-8685	277	6	12–48	384	24
HB DPS 88/81	329	7,2	16–64	64	10–40
SP 1100/91	345	7,5	8–64	32	12–176
CDC Cyber 170/855	/	7,5	0,5–2	2–4	12–24
NCR V-8695	370	8	16–64	512	32
HB DPS 88/82	645	13	16–128	128	10–80
SP 1100/92	700	14	8–64	32	12–176
CDC Cyber 170/865	/	15	0,2–1	–	12–24
CDC Cyber 170/975	/	19	0,2–1	–	12–24
CDC Cyber 170/865-D	/	20	0,2–1	–	12–24
SP 1100/93	915	20	8–64	96	12–176
SP 1100/94	1150	25	8–64	128	12–176
CDC Cyber 170/875-D	/	30	0,2–1	–	12–24

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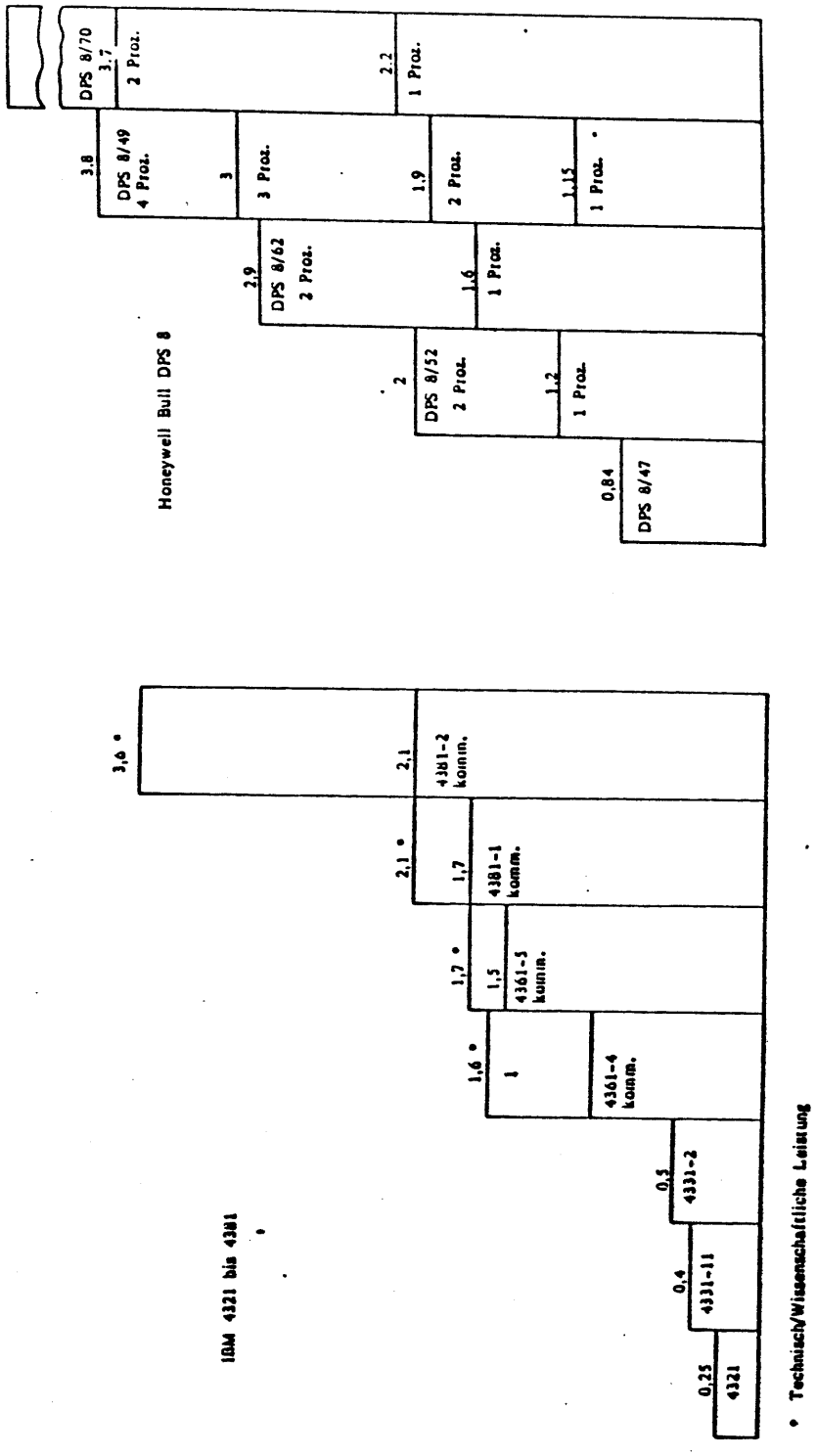
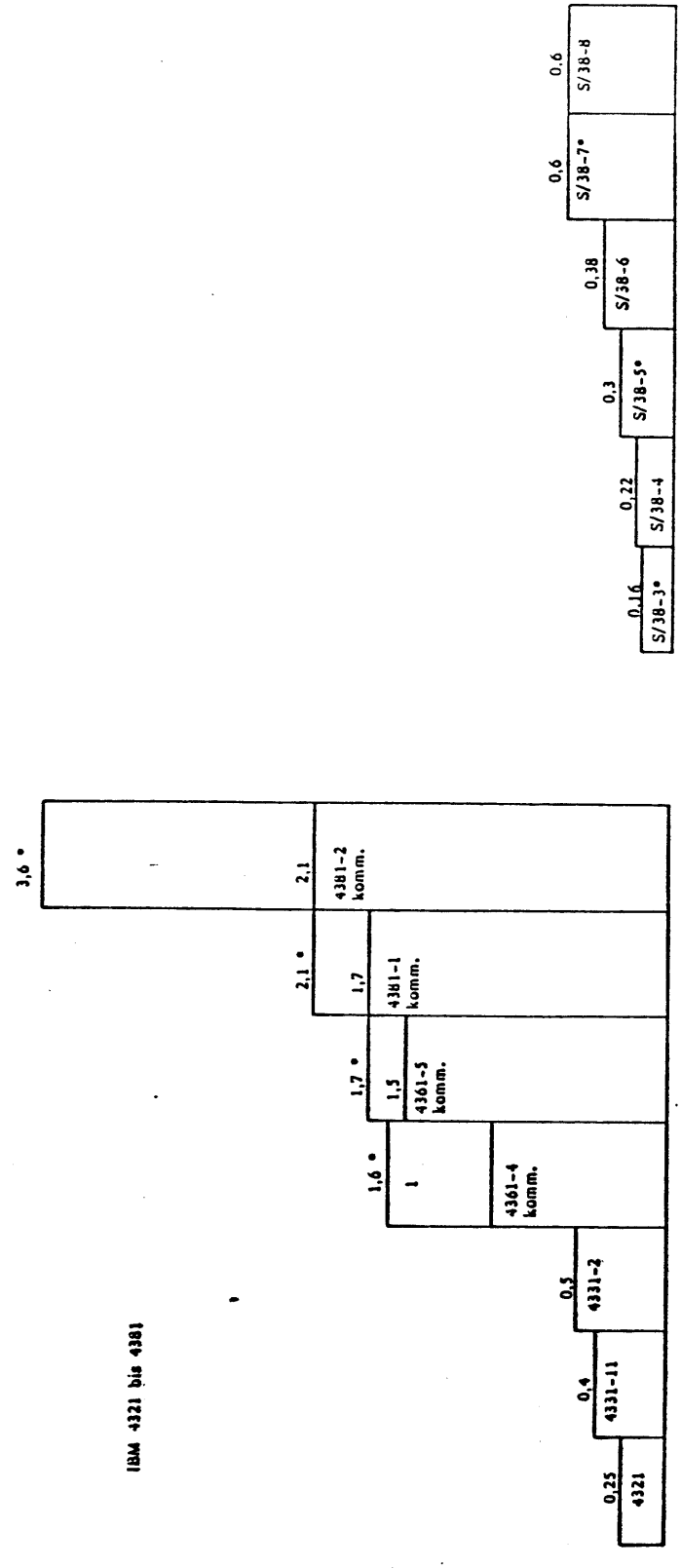
MIPS-LEISTUNGSEINORDNUNG IBM 4300 VS. HB DPS/8



IBM | 5/1984

MIPS-LEISTUNGSEINORDNUNG IBM 4300 VS. IBM S/38



6.2. COMPETITION NEWS

6.2.1. BURROUGHS

6.2.1.1. BURROUGH MEDIUM SYSTEM

The BURROUGHS medium systems are represented by three sub-series : the B 2900, the B 3900 and the 4900.

B2900

The B2900 series consists of two models : the entry-level model B2910, which was announced in June 1981, and the original model B2930 introduced in February 1979.

B3900

The B3900 series is composed of the B3955, a replacement of the previously announced B3950. The B3955 was introduced in September 1981.

B4900

The B4900 series includes the B 4955 which is the largest in the firm's range of B2000/3000/4000. This system was introduced in September 1982.

The B4955 has to be seen as a medium systems parc growth machine, permitting the medium system user to move from the B2900 to the B3900 and ultimately to the B4900's with only processor swaps.

In the B4955 performance range Burroughs would probably bid either the B5900 or B6900 to place the user in its large systems environment.

B2900/3900/4900

They provide substantialy better throughput capacity than the older B2800/3800/4800 and are object code compatible with the B3700/4700/2800/3800/4800.

- Burroughs B2900/B3900/B4900 employ an asynchronous pipelined architecture utilizing multiple independent processor modules which can operate concurrently, which is called by Burroughs "micro-modular concurrent" architecture.

- The input/output processor (IOP) initiates data transfers between memory and peripheral subsystems asynchronously and independently of the central processor.

  the IOP is interfaced to the peripheral subsystem through data link processor (DLP's). Each DLP is an independent microprocessor programmed to service a specific category of peripheral devices.

- The basic B2910 and B 2930 include 512 K bytes of main memory. Six DLP's are standard on the B 2910, while seven are standard on B2930. In addition they include console, a 1 x 8 disk controller and two diskette drives.

  The B2910 can be expanded to 1536 Kbytes of main memory and 16 DLP's while the B2930 can be expanded to 4864 Kbytes of main memory and 32 DLP's.

  the B2910 can be field-upgraded to a B2930, but B2900 cannot be field-upgraded to a B3955.

- The basic B3955 system includes 2048 Kbytes of main memory console, six DLP's, two disquette drives and a 2 x 8 disk controller. The system is expandable to 4864 Kbytes of main memory and 32 DLP's.

- The basic B4955 system includes 5 Million bytes of main memory and can perform up to 1.8 times faster than its predecessor, the B4800. A maximum of 64 DLP's can be configured with this model.

- In addition to the microprocessor configuration, the B2900/3900/4900 systems can be expanded with up to three additional processors to form a loosely coupled-multiprocessor system with shared mass storage, peripherals and communications system.

  With the addition of the shared system processor (SSP), the operating system, compilers utilities, program libraries and data files can also be shared by up to four central processors.

  Multiprocessor configurations can include B2800/3800/4800 series.

- Compared to the DPS 8 line and GCOS, Burroughs medium systems and the operating system (MCP) appears to be less efficient in multidimensional environment and especially in the interactive area.

TECHNICAL CHARACTERISTICS

MEDIUM SYTEMS

MODEL	ANNOUNCEMENT DATE	# CP	MAIN MEMORY MINI MAXI (MB)	DLP
B2910	06/81	1-4	0.5-1.5	6-16
B2930	09/79	1-4	0.5-5	7-32
B3955	09/79	1-4	2-5	7-32
B4955	09/82	1-4	5	8-64

FIELD UPGRADES ONLY = B2910 ⟶ B2930

6.2.1.1. BURROUGHS LARGE SYSTEMS

The BURROUGHS large and very large systems are now represented by three sub-series : the B5900, the B6900 and the B7900.

Entry level models of the B5900/6900 series are situated in the range of medium systems but place the user in a large systems environment. This situation is comparable to DPS 8 offer.

BURROUGHS B5900 SERIES

The original B5900 Model, the B5930 was introduced in September 1980. in september 1982, Burroughs replaced the B5930 with two new models: the B5920 and the B5935.

The B5920 is basically a B5930 re-implemented in newer technology and this re-implementation has yielded :

- higher performance (10 % more)
- a reduction of 69% in floor space requirements
- reduced power requirements
- a lower price (about 25 % less).

This sytem is Burroughs new name attack product in the large systems environment.

The B5935 looks just like the B5930.

The B5920 and B5935 Offer the same memory capacity and performance and differ only on I/O expansion cabinet required for a maximum B5900 configuration.

0 The principal architectural innovation of the B5900 is Burroughs multi-level function processor concept, in which major hardware function are assigned to separate programmable microprocessors.

The central processing unit includes the following processors : Micro Master Control Processor (MMCP), Program Controller, Data Processor, Memory Controller, Program Controller for instruction decoding, Message level Interface Port and Maintenance Processor.

The MMCP coordinates the activities of the other processors/ controllers and contains a microcoded implementation of the full instruction set of the large scale Burroughs computers.

0 From two to four B 5900 control processor can be interconnected via Burrough's global memory and operated in any of the three modes. Global memory capacity can range from 768 Kbytes to 3.1 megabytes, and each CPU can address a total of 6.2 megabytes of local memory plus global memory.

- in Multiprocessor (tightly coupled) mode, a single Master control Program (MCP) manages all the system's ressources

- in the Shared Resources (loosely coupled) Mode, each procesor operates under its own MCP but the processors can intercommunicate and share I/O and data communications ressources.

- in the Independent Systems (uncoupled) Mode, each processor operates with its own MCP, but communication between processors is prohibited. Global memory is used as an extension of each processor's local memory.

B 5900 can also be intermixed with B 6900 sytems in either the Shared Ressources Mode or the Independant Systems Mode.

0 Information is transferred to or from peripheral devices through additional function processors called data link processors (DLP).

A B5900 system can include up to 20 DLP's each controlling one peripheral device or a group of similar devices. Any DLP can be switched from one processor to another under MCP control.

Maximum aggregate I/O data rate is 2.3 million bytes per second.

0 Data communications controls functions are handled by specialized microprocessors called Network Support Processors (NSP's) and Line Support Processors (LSP's). Each NSP can controls up to 48 communication lines and a B 5900 sytem can support up to 3 NSP's. The NSP's and LSP's can be switched among processors when using multiprocessor systems.

0 The B5900 series run under the Master Control Program (MCP) which is available also for larger Burrough computers.

- When Burroughs users move to higher performance B6900's and B 7900's to accomplish growth, they have to swap their central processor, while the peripherals remains the same and all application programs, data base and system software can be executed without change.

- Note also that Burroughs large sytems are not compatible with any of the small systems or with any of the medium systems. And when users are in this case, it seems easier to change suppliers than to convert inside Burrough's lines.

BURROUGHS B6900 SERIES

The B6900 Series is the medium to large scale member of the new Burroughs "900" family of computers.

- The B6930 was announced in February 1980 as the first model. In October 1982 the B6925 was introduced and compared to the B6930, offers improvements in floor space in power and in air conditioning requirements.

  Through the B6930 is still being marketed, it is no longer in production, and so the B6925 appears to have removed the B6930 as an actively bid machine.

  The B6900 is code-compatible with its predecessors B5000, B6000 and B7000 including the B7900 announced in December 1982.

  The B6900 systems is similar to B5900 in design and functionality, but without possibility of upgrades.

- The B6925 central processing unit consists of a Data Processor that performs all arithmetic and logic functions, a memory control that permits the attachment of both local and global memory, a Message Level Interface Port (MLIP) that provides an interface between memory and the Input/Output data communications subsystem, and a Memory Tester that works in conjunction with the maintenance Diagnostic Processor.

  The MLIP provides an aggregate data transfer rate of 6.6. Million bytes per second for the input/output subystem.

  The input/output subystsem consists of a series of specialized microprocesors called Data link Processors (DLP's).

  These units perform peripheral-dependent functions and information transfer to and from memory via the Memory Level Interface (MLI).

  The B6900 I/O subsystem cabinet may be configured with up to four I/O base modules, each containing a Message Level Interface and up to eight DLP's on any type.

- The B6930 contains 3.1. million bytes of 16 K integrated Circuit (I.C.) main memory. In multiple-processor systems, the B6900 incorporates a memory hierarchy comprised of main memory that is local to each processor and memory that is global to all processors. GLOBAL memory is expandable from 768Kbytes to 3.1. Million bytes while local memory is expandable to 5.4 million bytes. Each processor is capable of addressing a total of 6.2. million bytes of local and Global memory, providing for up to 22 Million bytes of total memory in a four processor configuration.

- GLOBAL memory permits three different modes for multiprocessor environments : Multiprocessor Mode (tightly coupled), Shared Resources Mode (loosely coupled through Global memory), and Independent Systems Mode (uncoupled).

- The current B6800 systems may be intermixed with B6900 through Global memory in the shared resources or independent systems mode of operation.

BURROUGHS B7900 SERIES

In late December 1982, Burroughs announced their long awaited large systems follow-on product, the B7900. These product is intended to be the Burroughs answer to the IBM 308X Series.

Three models were announced : a single processor model B7900-F, a dual processor model B7900-H and a triple processor B7900-K.

- The B7900 central processor architecture is pattern after the B7800, utilizing four asynchronously operating units : program control, data reference, execution and memory access, each complemented with a fixed cache memory. An interesting and unique approach is the utilization of an auxiliary processor (AP), as standard, within each model. The AP is described as an enhanced 5900 processor designed to off-load the central processor. All the models include an AP in addition to the central processor or processors.

- The basic I/O subsystem is a processor called the host data unit (HDU).

  The HDU has three host-dependent ports, each containing two message level interface (MLI) ports, which in turn consists of I/O base modules. An I/O base module can contain up to eight data link processors (DLP). DLP handle peripherals and function as a channel controller.

- Each model is composed of the three processor types : central processor, auxiliary processor, and host data unit with maximum expansion and growth limited to a combination of eight of those processor types.

- The B7900 systems use the Master Control Program (MCP) operating system and are compatible with Burroughs's earlier B5000, B6000 and B7000 sytems.

BURROUGHS MODELS

	RELATIVE PERFORMANCE (x 66/80)	COMPETE WITH
MEDIUM SYTEM SERIES		
B2910	.2	DPS 7/35
B2930	.33	DPS 7/45
B3955	.4	DPS 7/45
B4955	1.6	DPS 8/62
LARGE SYSTEM SERIES		
B5920	.48	DPS 8/47
B5935	.48	DPS 8/47
B6925	.8	DPS 8/49
B6930	.8	DPS 8/49
B7900-F	5.5	DPS 88/81
B7900-H	10.0	DPS 88/82
B7900-K	14.0	DPS 88/82

TECHNICAL CHARACTERISTICS

LARGE SYSTEMS

MODEL	ANNOUNCEMENT DATE	# CP	MAIN MEMORY MINI-MAXI (MB)	(INCLUDING) GLOBAL MEMORY) (MB)	DLP
B5920	09/82	1-4	3.2-6.2	15.7	5-20
B5935	09/82	1-4	3.1-6.2	22.8	5-20
B6925	10/82	1-4	3.1-6.2	20	5-64
B6930	02/80	1-4	3.1-6.2	22.4	5-64
B7900-F	12/82	1	12-26	96	
B7900-H	12/82	2	24-96	96	
B7900-K	12/82	3	36-96	96	

6.2.3. IBM - INTERNATIONAL BUSINESS MACHINES CORPORATION

6.2.3.1. IBM 4300 SERIES

- The long-awaited "E Series" from IBM's Data Processing Division made its "debut" on January 30, 1979.

  Two new processors were introduced : the 4331-1 and the 4341-1.

  This series was completed with the announcement of the 4331 model group 2 in May 1980 and the 4341 model group 2 in September 1980.

  In November 1981, IBM gave a mid-life kicker to this line by announcing an entry-level CPU (4321), a mid-range addition to the 4331 line (4331-11) and two additions to the top-of-the-line 4341 (4341-10 and 4341-11).

- Within the 4300 family, there are two distinct lines, the 4331 and the 4341. Both of these lines present four models.

  The 4331 and the 4341 machines are distinctly different. There is no field upgradable path between them. Growth from a 4331 to a 4341 requires a processor swapout, and probably peripheral swapouts.

- The 4321/4331's are truly integrated systems with many of the peripherals adapters mounted in the processor cabinet. There are integrated adapter oriented computers and share this orientation with the so-called supermini computers.

  - On the original 4331-1, the Integrated Display/ Printer Adapter and a System Diskette Drive, which is used to load microcode, were the only standard I/O connections.

    One byte multiplexer channel and one block multiplexer channel were optional.

- The 4321 is a restricted 4331-1 from a connectability standpoint. It has no optional adapters, but in addition to those standard on the 4331-1 it has an integrated communication adapter, restricted to three lines, an integrated Direct Access Storage Device DADS adapter, restricted to 3310 disk only, and a 8809 magnetic tape adapter. It equals the performance of the 4331-1.

- The 4331-11 includes a high speed 4K cache buffer, an integrated DASD adapter, a byte multiplexer channel and a block multiplexer channel. Optionally, a five-line group is available.

  The 4331-2 offers twice the internal performance of the 4331-1. It includes a high speed 8K cache buffer, 131 Kbytes of reloadable control storage plus 12 Kbytes read only control storage. It presents more optional adapters, than the latest model 4331-11 : one byte multiplexer channel, two block multiplexer channels, one high speed block multiplexer channel and a second DASD (Direct Access Storage Device) adapter if the high speed multiplexer channel is not used.

  The available field upgrades for this line are :

  4321 ---> 4331-11 ---> 4331-2
  4331-1 ---> 4331-2

- The 4341 machine is a more traditional mainframe and looks like the 370 series.

  - The 4341-9 system is the new entry level model of the 4341 series. This system is available with one, two or four megabytes of central memory, a 2 Kbyte high speed buffer memory, and a group composed of one byte multiplexer channel and two block multiplexer channels (with a block transfer rate of up 3.0 million bytes per second).

    A second group of three additional channels is available as special feature and the aggregate data is 11 megabytes per second in this case.

    The 4341-9 systems can offers up to 70 % of the internal performance of the 4341-10 model.

  - The 4341-10 processor has similar memory and channels to the 4341-9 but offers a 4 Kbyte of high speed buffer memory. It is rated to 85 % of the internal performance of the 4341-1 in commercial environment (up to 95 % in scientific environment).

  - The IBM 4341-1 processor is similar to the 4341-10 except on the size of the high speed buffer memory (8 KB).

- The 4341-2 provides as standard equipment 16 Kbyte high speed buffer memory, one byte and five block multiplexer channels. The first two block multiplexer channels can transfer information at up to 3.0 Million bytes per second. The three remaining block multiplexer channels are each capable of transferring data up to 2.0 Million bytes per second. The aggregate data rate of the five block multiplexer channels is 12 megabytes per second. The main memory capacity ranges from 2 to 16 megabytes.

  The 4341-2 processor can provide internal operating speeds in the range of 1.5 to 1.8 times those of similarly configured model 4341-1 processor.

- The 4341-11 processor has similar channels to the 4341-2, a 8 K bytes high speed buffer memory, and the main memory capacity ranges from 2 to 8 megabytes.

  Internal performance for commercial/scientific environment is 125 % of a 4341-1.

0 An optional channel to channel adpater allows interconnection of two channels which may be on a 4341, system/360 or system/370.

0 The new processors can operate in a system 370 compatible mode or in an Extended Control Program (ECPS) mode which takes full advantage of the extensive micro-coding. They feature 64 Kbit memory chips and logic chips that contain up to 704 circuits each.

- The 4341-12 processor is similar to the 4341-2. The performance increase of this model is 15 % more in comparison of the 4341-2 processor.

0 The available field upgrades for this line are :

4341-9 ---> 4341-10 --->4341-11 --->4341-12

4341-1 ---> 4341-11 ---> 4341-12

4341-1 ---> 4341-2 ---> 4341-12

0 They include the following features : LSI technology, channels with virtual addressing, system/370 Universal Instruction Set, maintenance support functions including a support processor and remote support facility.

- o Instead of 3278-2A display console, the IBM 3279, color display and IBM 3287 color printer can be used as console devices with all 4341 processors.

- o With the introduction of the 4300 Series were introduced new fixed disk drives (IBM 3370) and a new disc controller (IBM 3880).

  - The IBM 3880 storage control provides two completely independant paths called a storage director and which are attached to the block multiplexer channels. Both storage directors can be attached to the same channel, to different channels on the same processor, or to channels on two separate processors.

    Now, five models of the IBM 3880 storage control are available on the 4341 line.

    Only two models the 3880-1 and the 3880-2 can be connected to the 4331-2.

  - The 3880-1 can attach on each storage director 33XX removable disk units and 3370/3375 fixed disk units.

  - The 3380-2 can attach on the first storage director 33XX removable disk units or 3370/3375 fixed disk units, and on the second director 3380 fixed disk units only.

  - The 3880-3 attaches 3380 fixed disk units only.

  - The 3880-11 incorporate 8 million characters of cache storage and is designed for paging and swapping applications from IBM 3350 disk drives.

  - The 3880-13 available with 4 or 8 million characters of cache storage supports IBM 3380 storage devices and is designated for application and non-paging system data.

- o The 4300 Series processors can utilize most of the system 370 mass storage devices in addition to the following new mass storage devices :

  - IBM 3310 : provides 64.5 Megabytes of disk storage for 4331 processor only, and are connected to 4341 via an integrated adapter.

- IBM 3370 : provides 571 Megabytes of disk storage per drive, 285 megabytes per actuator.

  The 3370 can be connected to an integrated adapter on the 4331 or to a 3880 storage control on the 4331-2 or 4341.

- IBM 3375 : provides 819 megabytes of disk storage per drive, 409 megabyte per actuator.

  The 3375 can be connected to a 3880 storage control on 4331-2/4341.

- IBM 3380 : provides 2520 megabytes of disk storage, 630 megabytes per actuator and a faster data transfer rate (3.0 MB/s).

  The 3380 can be used with the 4341 processors only.

  The 3375 and the 3380 use count-key data format employed in the 3350 and other IBM disk drives in contrast to the fixed 512 byte blocks used in the 3370 and 3310.

o Five operating systems are available for the 4300 series :

- DOS/VS extended is said to be a major expansion of DOS/VS. Unfortunately, DOS/VSE provides only limited multiprogramming capabilities unless the user acquires the DOS/VSE Advanced Function product, an independantly priced adjunct that allows the DOS/VSE user to employ up to 12 partitions and also makes it possible to incorporate many of the new programs products available with the system.

- Small System Executive (SSX/VSE) Operating System consist of a pre-generated system which contains DOS/VSE components tested together. Applicable to 4321 and 4331 only with at least 1 MB memory.

- OS/VS1 can run Extended Control program support mode with the ECPS/VS1 feature on either the 4331 or 4341 processor or in 370 mode.

- In spite of OS/VS1 has been improved in particular to support IBM 3880 storage control and the IBM 3375 disk units, it does not seem to be very attractive.

  Supports for IBM 3370 and IBM 3380 disk units are not available under OS/VS1.

- MVS support is provided on the 4341 through the extended control program support ECPS/MVS Option which includes new privileged instructions that enables the 4341 to utilize MVS/SP JES2 or JES 3. MVS/SP JES 2 and JES 3 present major extensions and enhancements to the MVS base control program plus JES 2 and JES 3 respectively.

- With VM/370, the 4300 user can operate in mixed-mode environment where CMS interactive computing is combined with a guest system control programming (DOS/VSE, OS/VS1 or MVS) on the 4300 processors.

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MODELS	CACHE MEMORY (KB)	MAIN MEMORY (MB)	RELATIVE SCALE (66/80 = 1)	COMPETE WITH
4321	-	1	.2	DPS 7/35
4331-1	-	0.5, 1	.2	DPS 7/35
4331-11	4	1, 2	.3	DPS 7/35
4331-2	8	1, 2, 3, 4	.4	DPS 7/45
4341-9	2	1, 2, 4	.48	DPS 8/47
4341-10	4	2, 4	.65	DPS 8/47
4341-1	8	2, 4	.8	DPS 8/49
4341-11	8	2, 4, 8	.94	DPS 8/49
4341-2	16	2, 4, 8, 12, 16	1.2	DPS 8/52
4341-12	16	2, 4, 8, 12, 16	1.45	DPS 8/62

6.2.3.2. IBM 303X SERIES

- The 303X Series was announced in 1977 ; three processors were introduced : the 3031, the 3032 and the 3033.

- In 1978, IBM announced a dual processor version of the model 3033 which provides up to 1.8 times the internal performance of the single-processor system.

  The same year IBM introduced the 3041 attached processor to fill the gap between the 3031 and the 3032. A 3031 can be upgraded to a 3031 attached processor (AP) complex for about half the cost of a second two megabyte 3031.

- In January 1979, IBM introduced its second attached processor : the 3042 AP. The 3033 attached processor complex combining a 3033 and a 3042 attached processing unit, is rated to be 1.6 to 1.8 times more powerful than the uniprocessor 3033.

  On November 1, 1979 a new member of the 303X family called IBM 3033 model group N processor was introduced. It is a downgrade version of the 3033 uniprocessor. The cache memory is reduced from 64 KB to 16 KB. In comparaison of a 3032 the performance can be evaluated to+30 % in a commercial batch environment and+80 % with a scientific processing workload .

  As computing needs expand, the 3033N can be upgraded to the more powerful 3033 uniprocessor, 3033 attached processor or 3033 dual processor.

- In 1980, IBM introduced the 3033S, a new entry system for the 3033 line. It is given to have from 2.1 to 2.4 times the performance of the 3031 processor with similar configurations and identical programs running under MVS.

This model can be configured with four or eight million bytes of main storage, and six or twelve channels.

It can be field upgraded to more powerful 3033 N/U/AP or MP models and explains, it has eclipsed the older 3032 model.

IBM has also announced significant enhancements to the 303X family which are :

- extended addressing capability for up to 32 megabytes for the 3033 MP multiprocessor.

- IBM 3042 attached processor model 2 which provides 6 channels standard and 6 optional channels and allows up to 28 channels on the 3033 attached processor complex which consists of a 3042 AP combined with a 3033 model A.

- Data streaming feature for 3033, 3032, 3031 and 3042 attached processor model 2.

  This feature modifies the first two block multiplexer channels of a channel group of these systems so that each can opprate at up to three megabytes per second data transfer rate in data streaming mode.

- IBM 3814 switching management system which is designed to aid in the management of complex EDP configurations by providing centralized control of control-unit switching. Up to 80 configurations can be stored in the system to simplify the operator actions involved in switching from one I/O configuration to another.

o A wide range of peripheral systems is available to 303X, in particular three high speed, high density direct access storage devices (DASD). The 3370, 3375 and 3380 DASD have 571, 819 and 2520 million bytes of storage capacity respectively. The 3370 uses fixed block architecture while the newer 3375 and 3380 both use the count-key-data format.

  The devices are all connected to 303X processors via the IBM 3880 storage controllers.

The IBM 3880 storage control provides two completely independant paths called a storage director and which are attached to the block multiplexer channels. Both storage directors can be attached to the same channel, to different channels on the same processor or to channels on two separate processors.

There are five models of the 3880 which can accomodate various combinations of 3330/3340/3350/3370/3375 and 3380.

- The 3880-1 can attach on each storage director 33XX removable disk units and 3370/3375 fixed disk units.

- The 3880-2 can attach on the first storage director 33XX removable disk units, and on the second storage director 3380 fixed disk units only.

- The 3880-3 attached 3380 fixed disk units only.

- The 3880-11 incorporates 8million characters of cache storage and is designed for paging and swapping applications from IBM 3350 disk drives.

- The 3880-13 available with 4 or 8 million characters of cache storage, supports IBM 3380 storage devices and is designated for application and non-paging systems data.

o The 303X/304X systems are supported by several different operating systems.

OS/VS 1 release 7 :

The current release of OS/VS1 operating system provides support for 303X processors in the system/370 Extended Control mode.

OS/VS 1 has been improved in particular to support the 3880 storage control and the 3375 fixed disk units.

Supports for IBM 3370 and IBM 3380 fixed disk units are not yet available under OS/VS1.

- DOS/VSE :

DOS/VSE is available on the 3033 S, as well as the 3033 models N and U, but is not recommended on the latter two systems.

IBM adds that a recommended maximum processor storage for DOS/VSE is 8 MB. Note also that IBM 3380 fixed disk units are not supported under DOS/VSE.

- Multiple Virtual System (MVS)

Operating system/virtual storage 2 (OS/VS2) is a significantly improved version of OS/Multiple Virtual Task, which was available for the system/370. IBM discontinued support for OS/MVT in 1976.

OS/VS 2 releases prior to release 2 are now known as OS/VS 2 single virtual systems (or SVS) while OS/VS 2 release 2 and above are known as OS/VS 2 multiple virtual systems (or MVS).

OS/VS2 (SVS) supports a maximum of 16 million bytes of virtual storage that is divided into 64 Kbytes segments and 4K byte pages (32 million bytes of space with the extended addressing feature in the 3033 systems) ; virtual storage support of TSO ; up to 63 protected batch user regions or 42 TSO user regions ; dynamic priority scheduling including I/O load balancing based upon I/O data rates ; etc...

OS/VS 2 (MVS) is a major functional enhancement over OS/VS 2 (SVS) that features support of multiprocessing for 3033 systems ; larger virtual storage with up to 16 million bytes of adressable space for each of up to 63 concurrent users ; job entry system 2 or 3 ; virtual telecommunications access method (VTAM) support of the 370X communications controllers in network control program mode.

MVS/System Extensions is a program product to improve certain characteristics of MVS. MVS/SE provides the following enhancements : reduced processor time to execute certain control program functions, faster address translation, improved AP and MP performance, improved system ressource utilization, etc...

MVS/System Product JES2/S

MVS/SP includes all the functions of MVS/SE plus the following : support for the 3375/3380 fixed disk units, support for the 3380 controllers, support for the 3081 models, and some improvements in system throughput and reliability activities.

MVS/Extended Architecture (MVS/XA)

MVS/XA consists of the two elements : the data facility product and the MVS/SP JES 2/3 VERSION 2, and provides extended addressing capabilities. Under MVS/XA, real and virtual storage addressing are expanded from 16 Million bytes to 2 gigabytes.

- Virtual Machine/System Product

VM/SP is an enhanced version of VM/370. VM is a system control program that manages a computing system's resources (CPU, storage and input/output devices) so that all are available to many users at the same time, and give them the functional equivalent of a real, dedicated computing system.

VM provides virtual machines and the ability to run multiple operating systems concurrently (DOS/VS, OS/VS1 or MVS) and a conversational time-sharing system (CMS).

VM/XA is a new program product to ease the conversion from MVS/SP to MVS/XA.

I B M 3 0 3 3

MODELS	CACHE MEMORY (KB)	MAIN MEMORY (MB)	RELATIVE SCALE 66/80 = 1	COMPETE WITH
3031	32	2/3/4/5/6/7/8	.9	DPS 8/52
3031 AP	2 x 32	2/3/4/5/6/7/8	1.6	DPS 8/70
3032	32	2/4/6/8	2.3	DPS 8/62 RED
3033 S	0.5	4/8	2.1	DPS 8/70
3033 N	16	4/8/12/16	2.9	DPS 8/70-2
3033 U	64	4/8/12/16	3.8	DPS 8/70-3
3033 AP	2 x 64	8/12/16/20/ 24/28/32	6.5	DPS 8/70-4
3033 MP	2 x 64	8/12/16/20/ 24/28/32	6.5	DPS 8/70-4

6.2.3.3. IBM 308X SERIES

- The 308X Series represents the top of IBM's large systems product line and the lower models are seen as the successors to IBM's 3033 line.

- The first model, the 3081 model group D, was announced in November 1980.

- In October 1981, IBM announced the 3081 model group K which offers 30 to 40 percent performance improvement over the model D.

- In March 1982, IBM announced three single processors : the 3083 model group E, model group B, model group J.

- In September 1982, IBM unveiled the new top-of-the-line computer the IBM 3084 which presents four central processing units.

  At the same time IBM introduced the 3081 model G which in fact replaces the 3081 model D.

o Performance

. The entry-level 3083-E has about 2.8 times the performance of the 4341-2, and is comparable in performance to the IBM 3033 Model U.

The 3083-B has 1.4 to 1.5 times the power of the 3083-E.

The 3083-J has 1.8 to 2.0 times the power of the 3083-E.

The 3083-K has 1.6 to 1.9 times the power of the 3083-J. (VM is given to 1.6, and MVS is in the range of 1.7 to 1.9).

The 3081-D has 1.8 to 2.1 times the power of the 3033 model U. (The lower end of the range concerns data base IMS environment, the upper end of the range concerns commercial batch and scientific).

The 3081-G's performance is slightly greater than that of the 3081-D. The internal instruction execution rate of the 3084 has been measured at up the 1.9 times that of the 3081-K.

Performance Inside IBM Series

MODEL	43XX	303X	3083	3081/3084
3083-E	2.8 x 4341-2	3033U		
3083-B	3.9-4.2 x 4341-2		1.4-1.5 x 3083-E	
3083-J	5.0-5.6 x 4341-2	3033-AP/MP	1.8-2.0 X 3083-E	
3081-D	6.1-7.6 x 4341-2	1.8-2.1 x 3033U		
3081-G				
3081-K	8.0-10.6 x 4341-2		1.6-1.9 x 3083-J	1.3-1.4 x 3081-D
3084				1.9 x 3081-K

o Description

. The 3083 system consists of :

- a 3083 processor unit with 8 megabytes of main memory which can be expanded up to 16 megabytes on the model E, and 16/24 megabytes on the models B, and J. The 3083 processor unit includes an integrated I/O processor containing 8 channels as basic. One set of 8 channels is available on E models, two on B and J.

- a 3082 processor controller to monitor and supervise all ongoing operational activity and available in three models corresponding to the number of channels : 8, 16, 24.

- a 3087 coolant distribution unit available in two versions. The model 1 uses the efficiency of water cooling and evacuates its heat to chilled water. The model 2 evacuates its heat to the air of the computer room.

- a 3089 power unit or other appropriate 400 Hz source of power.

- a 3278 display console model 2A as system console and one or more operator consoles (model 3277/3278/3279).

. The 3081 system consists of :

- a 3081 processor unit which is called by IBM a "dyadic processor" with two integrated central processors operating under a single operating system.

  Each processor has access to 16, 24, or 32 megabytes of shared storage and its own set of channels.

  The 3081 processor unit has 16 or 24 integrated channels organized into two logical sets, one per central processor. Up to 16 channels can be assigned to a set. Channel set switching permits one processor to continue all channel activity should the other processor experience a failure. Up to four channels may be byte multiplexer channels. Each block multiplexer channel is capable of up to a 3 megabyte/second data rate when operating in data streaming mode.

  The 3081 cannot, however, be split into two uniprocessors running simultaneously.

- a 3082 processor controller

  a 3087 coolant distribution unit

  a 3089 power unit or other appropriate 400 Hz source of power

  a 3278-2A console and one or more operator consoles

- Note that 3089 model 2 coolant distribution unit which evacuates its heat to the air of the computer room, supports only the 3083 and cannot be used for 3081 systems.

- Each model D or model G processor has a 32K byte high speed buffer while each model K processor has a 64K byte buffer. This leads to suppose that the cache buffer sizes on the models E, B, J are respectively 16, 32, 64 K bytes.

  For 3083/3081 systems processor cycle time is 26 nanoseconds, and the access time to control storage from a central processor is 312 NS with an 8 byte data path.

- Note: A dyadic processor does not have the capability that permits concurrent repair while a degraded configuration continues to function. A dyadic processor permits deferred repair only.

- The 3084 system consists of :

  - a 3084 system with four central processing units and offers 48 channels and up to 64 millions bytes of main memory. For flexibility it can be "partitioned" and used as two independant computers.

  - an expanded processor controller 3082-Q composed of two controllers. When operating in a multiprocessing configuration the 3082-Q employs 1 controller to manage the 3084 and a second for back-up. For partitioned operations the 3082-Q's two controllers each manage the operation of a dyadic configuration.

  - two 3087 coolant distribution

  - four 3278-2A consoles

  - two 3089 power unit or other appropriate 400 Hz source of power

MODEL	CACHE MEMORY (KB)	MAIN MEMORY (MB)	CHANNELS
3083-E	16	8/16	8/16
3083-B	32	8/16/24/32	8/16/24
3083-J	64	8/16/24/32	8/16/24
3081-D	2 x 32	16/24/32	16/24
3081-G	2 x 32	16/24/32	16/24
3081-K	2 x 64	16/24/32	16/24
3084	4 x 64	24/48/64	32/48

UPGRADABILITY: E ⟶ B ⟶ J ⟶ K ⟶ 3084

D ⟶ K ⟶ 3084

E ⟶ B ⟶ G ⟶ K ⟶ 3084

o Upgrades

. The upgrade paths are the following:

3083-E ⟶ 3083-B ⟶ 3083-J ⟶ 3081-K ⟶ 3084

3081-D ⟶ 3081-K ⟶ 3084

3083-E ⟶ 3083-B ⟶ 3081-G ⟶ 3081-K ⟶ 3084

. In particular if the 3083-J can be seen as half the 3082-K, the 3083-B cannot be presented as half the 3081-D. It is the new 3081-G that replaces the model D which is the dyadic version of the uniprocessor 3083 model B.

o Technology

. The 308X uses the Schottky TTL logic chip, similar to that used in IBMs 4300 Series. Up to 133 chips are sealed in a helium-filled unit called the thermal conduction module (TCM). Each CPU is made of eight TCMs, all mounted on a ceramic multi-layered board that contains all necessary connections.

o Software

- The 308X Series is supported by the MVS/SP (Multiple Virtual Storage/System Product) and VM/SP (Virtual Machine/System Product) operating systems.

- With the announcement of the model K, IBM extended the System/370 architecture by announcing MVS/XA which provides new addressing capabilities for large MVS applications. Under MVS/XA, real and virtual storage addressing are expanded from 24 bits (16 million bytes) to 31 bits (2 gigabytes). MVS/XA consists of two elements : MVS/SP Version 2 and the Data Facility Product (DFP).

- Bi-modal operations permits the concurrent execution of 24 bit and 31 bit programs.

- At the same time, IBM introduced a new program product VM/XA to ease the conversion from MVS/SP TO MVS/XA. The migration aids supports concurrently one MVS/SP Version 1 preferred virtual machine and one or more MVS/XA test machines.

- MVS/XA qnd VM/XA are expected to be available respectively in the first quarter and in the fourth quarter of 1983.

- IBM's Multiple Virtual Storage/Extended Architecture (MVS/XA) supports the 3084 processors when operating as four-way tightly coupled processors.

Performance Comparison

MODEL	TYPE	ANNOUNCEMENT DATE	SHIPMENT	PERFORMANCE 66/80=1	PERFORMANCE 8/64=1	COMPETITION WITH
3083-E	SINGLE	3/82	2Q83	3.7	5.2	DPS8/70-2
3083-B	SINGLE	3/82	1Q83	5.4	7.6	DPS8/70-4
3083-J	SINGLE	3/82	1Q83	7.1	10	DPS88/81
3081-D	DYADIC	11/80	4Q81	9.6	13.5	DPS88/82
3081-G	DYADIC	09/82	09/82	10.5	14.8	DPS 88/82
3081-K	DYADIC	10/81	2Q82	12.8	18	DPS88/82
3084	QUADRUPLE	09/82	4Q83	24.3	34.2	

6.2.7. SPERRY

6.2.7.1. SPERRY 1100/70 SERIES

On June 6, 1983 Sperry announced a new number of the 1100 family of systems : system 1100/70. The 1100/70 is essentially a re-packaged version of the 1100/60 ; it is an OS1100 system and is totally compatible with 1100/60, 1100/80 and 1100/90.

The announcement of June is composed of 7 single-processor and 8 multiple-processor models. The multiple-processor concerns only the 1100/70 models E1, E2, H1 and H2 and no more than two-processor models are offered.

So triple-processors and quadruple-processors 1100/60 models remain active offers.

Performance

The performance of the 1100/70 models should equate to the equivalent-model 1100/60s in commercial environment.

This can be different in scientific environment due to an "enhanced floating point performance" feature introduced with all the 1100/70s.

Description

The characteristics that distinguish the 1100/70 from the 1100/60 are the following :

- Memory packaging :

  the 64K chip memory is integrated within the 1100/70 basic cabinet, with the processor and input/output unit. This new memory technology allows to expand the integrated memory size from the 1100/60 maximum of 4 MB to an 1100/70 maximum of 16 MB per processor.

- Package pricing :

  all 1100/70 central system prices include the price of an entry-level Cache Disk Control per processor.

o FNP requirement :

the 1100/70 configuration must include one of the Sperry's data communications processors : DCP/10, DCP/20 or DCP/40. The hard-wired General communications Subsystem (GCS) is not available on 1100/70.

o Multiple Processor Variations :

the 1100/70 can accomodate a maximum of two processors in the integrated central system arrangement ; 3 and 4 processor configurations are not yet offered with 1100/70.

The dual processor 1100/70 can be offered with two complete central systems, each with processor, memory and IOU as on 1100/60 dual system, but can be offered also with only one IOU.

o Price level :

in comparison with the 1100/60 prices, the 1100/70 introduce some very significant price reductions. The most important cuts are in purchase prices. Prices reductions range from 20 % to 60 % depending on the models in the U.S.

Prices adjustments are also offered on central memory and decreases are up to 60 % in the U.S.

These pricing actions brings the large system 1100 more in line with the market prices.

o Upgrades :

the 1100/70 models can be field-upgraded from the entry-level model 1100/70-B1 up to the top model 1100/72-H2 MP, which corresponds to the two completely redundant central system cabinets cross-barred, or up to the top model 1100/72-H2 DP, with this version the second central system cabinet contains only one processor and memory.

For users equipped with 1100/60, Sperry offers to replace their 4 MB with 4 MB of 64 K bit chip integrated memory for $ 60 000, which authorizes then memory extensions up to 16 MB per processor.

SPERRY 1100/70

MODELS	# CP	# I/O	EXTENDED INSTRUCTION SET	CACHE MEMORY (KB)	CENTRAL MEMORY MINI-MAXI (MB)
1100/71-B1	1	1	N	N	2
1100/71-C1	1	1	N	N	2-16
1100/71-C2	1	1	Y	N	2-16
1100/71-E1	1	1	N	8	2-16
1100/71-E2	1	1	Y	8	2-16
1100/71-H1	1	1	N	32	2-16
1100/71-H2	1	1	Y	32	2-16
1100/70-E1 DP	2	1	N	2 x 8	2(2-16)
1100/70-E2 DP	2	1	Y	2 x 8	2(2-16)
1100/70-H1 DP	2	1	N	2 x 32	2(2-16)
1100/70-H2 DP	2	1	Y	2 x 32	2(2-16)
1100/72-E1 MP	2	2	N	2 x 8	2(2-16)
1100/72-E2 MP	2	2	Y	2 x 8	2(2-16)
1100/72-H1 MP	2	2	N	2 x 32	2(2-16)
1100/72-H2 MP	2	2	Y	2 x 32	2(2-16)

SPERRY 1100/70

MODELS	RELATIVE SCALE	COMPETE WITH
1100/71-B1	1	
1100/71-C1	1.2	DPS 8/47
1100/71-C2	1.6	DPS 8/47
1100/71-E1	1.8	DPS 8/49
1100/71-E2	2.2	DPS 8/49
1100/71-H1	2.8	DPS 8/52
1100/71-H2	3.3	DPS 8/62
1100/70-E1 DP	3.5	DPS 8/49 R
1100/70-E2 DP	4.2	DPS 8/49 R
1100/70-H1 DP	5.2	DPS 8/62 R
1100/70-H2 DP	6.4	DPS 8/70 R
1100/72-E1 MP	3.5	DPS 8/49 R
1100/72-E2 MP	4.2	DPS 8/49 R
1100/72-H1 MP	5.2	DPS 8/62 R
1100/72-H2 MP	6.4	DPS 8/70-2

6.2.7.2. SPERRY 1100/60 SERIES

- The 1100/Series was announced in June 1979, and included six models. The 1100/62 E1MP and 1100/62 E2MP were added in March 80 and the uniprocessor versions of its E1 and E2 appeared in September 80. The 1100/60 is aimed at replacing the 1100/10, 1100/20 AND 1100/40.

- The 1100/60 is based on multi-processor architecture. The arithmetic and logic portions of the 1100/60 employ sets of nine Motorola 10800 micro processors (4-bit slice), combined with ECL circuitry and multi-layer packaging.

- Memory in the 1100/60 is composed of 16K-bit dynamic MOS chips. Memory access time is 575 nano seconds with a 24 nano second refresh cycle. Univac intends to convert to 64K-bit chips when they become reliable enough.

- A new communication processor, the DCP/40 employing the same technology and multi-processor architecture as the 1100/60 is offered. This unit can handle from 16 to 256 communications lines and contains 32 K to 512 K 36-bit words of memory.

- A System Support Processor (SSP) provides partitioning, system control, maintenance and console management functions.

- The 1100/60 Series systems utilize the 1100 Operating Systems.

- In November 1981, Sperry UNIVAC announced the three-processor 1100/63 and the four-processor 1100/64. The 1100/63 and 1100/64 can be configured with model H1 or H2 processors only.

- The 1100/60 Series is available in 14 models which are differentiated with the number of processors (up to four), the size of the cache memory (2 or 8 Kwords), and the use of Extended Instruction Set (EIS)

SPERRY 1100/60 AVP

- In October 80, Sperry introduced the 1100/60 attached Virtual Processor (AVP) which integrates VS/9 capabilities. Application programs that run under VS/9 on the Series 90/60-70-80 can be executed on an 1100/60 AVP without modification.

- This processor shares the channels and the memory. The main storage capacity of an 1100/60 AVP ranges from 254 K TO 1048 Kwords.

- The Attached Processor Control Software (APCS) establishes the environment for VS/9 to operate as though it were running with its standard peripheral complement.

- The performance is given to be the same as 90/80-3 model (.9 MIPS).

- note that OS/1100 and VS/9 environments are strictly separated.

- First deliveries began in 4Q81.

MODELS		RELATIVE SCALE	COMPETE WITH
UNIPROCESSOR			
1100/61-B1	Base system	0.8	DPS 7/45
1100/61-C1	Base system	1	
1100/61-C2	C1 + EIS	1.25	DPS 8/47
1100/61-E1	C1 + CM (2 KW)	1.45	
1100/61-E2	C2 + CM (2 KW)	1.75	DPS 8/52
1100/61-H1	C1 + CM (8 KW)	2.2	
1100/61-H2	C2 + CM (8 KW)	2.6	DPS 8/62
MULTIPROCESSOR			
1100/62-E1MP	2 x E1 CM (2 KW)	2.8	DPS 8/49 R
1100/62-E2MP	2 x E2 CM (2 KW)	3.3	DPS 8/52 R
1100/62-H1MP	2 x H1 CM (8 KW)	4.1	DPS 8/62 R
1100/62-H2MP	2 x H2 CM (8 KW)	5	DPS 8/70 R
1100/63-H1MP	3 x H1 CM (8 KW)	6	
1100/63-H2MP	3 x H2 CM (8KW)	7.5	DPS 8/70-3
1100/64-H1MP	4 x H1 CM (8 KW)	8	
1100/64-H2MP	4 x H2 CM (8 KW)	9.5	DPS 8/70-4

6.2.7.2. SPERRY 1100/80 SERIES

- Introduced in November 1976, the 1100/80 systems are the largest and most powerful computers offered by Sperry Univac to date.

- When first announced, the 1100/80 systems were offered in mono-processor (1100/82) or dual processor (1100/82) configurations. In October 1977, Sperry announced three additions to the 1100 family, a low-end designated the 1100/80 and two multi-processor configurations designated the 1100/83 (3 CPU's) and 1100/84 (4 CPU's).

  The new main memory employs 16 K-bit MOS chips.

- The Sperry 1100/80 system is a limited configurability version of the 1100/81 that includes 4 Kwords (36 bits) of buffer storage and 524 K or 1048 Kwords of main memory, one byte multiplexer channel, one block multiplexer channel, four word channels, maintenance unit, system console and motor/alternator.

- The Sperry 1100/81 system consists of one central processor unit, one or two Input/Output Units, 524 K to 4194 Kwords of main memory, one storage interface unit with 8 K to 16 Kwords of buffer storage, one system transition unit, one system maintenance unit, one to any number of system consoles, and one motor/alternator.

- The 1100/84 consists of four CPU, four main storage units capable of controlling 2096 K to 4194 Kwords of main memory, 32 Kwords of buffer storage, two or four IOU each containing one byte multiplexer channels, one block multiplexer and four word channels, two system maintenance units, two or more alernator units.

- The 1100 Operating System, formerly called EXEC 8, is the standard Operating System for all the models.

MODELS	CP	BUFFER STORAGE (words)	COMPETE WITH
1100/80	1	4 K	DPS 8/52
1100/81	1	8 K to 16 K	DPS 8/70
1100/82	2	8 K to 32 K	DPS 8/70-2
1100/83	3	24 K to 32 K	DPS 8/70-3
1100/84	4	32 K	DPS 8/70-4

Sales Aid

Cii Honeywell Bull

DPS 8

Internal use only

Published by : LARGE SYSTEMS MARKETING DIVISION
Addressee :

Issue N° 129
Date : August 1st, 1983

Product :

COMPETITIVE BULLETIN

Please find hereafter a competitive bulletin on the mainframer Digital Equipment Corporation - DEC.

P. CHASTRES
Large Systems
Product Marketing

W. KING GILLIES
Manager
Large Systems
Marketing Division

June 24, 1983

SUBJECT: DIGITAL EQUIPMENT CORPORATION

The May 30th edition of Computerworld carried a front page article regarding Digital's mainframe business. The article stated that:

- The 10 MIP 36-bit mainframe follow-on product (JUPITER) has been terminated.
- Digital has discontinued all future large system models and will grow their users with the 32-bit VAX systems.
- The article also inferred that the mainframe users are very disappointed.

This announcement may be a result of a number of considerations, including:

1) Both the 32-bit VAX follow-on product (VENUS) and the JUPITER product have slipped significantly from their original schedule.
2) The cost of R&D for both products at a time when the corporation is making a significant commitment to strengthen their market share in personal computers, coupled with the threat to their minicomputer position by other vendors.
3) Their mainframe revenue as a percent of their total revenue has been declining.

However, Ken Olson, Digital's founder and CEO, had previously told the 36-bit mainframe users that they would not be abandoned. There are currently over 1,400 systems installed (Attachment 1 provides a detailed listing by model) and there are no tools or bridges to move those 36-bit users onto the 32-bit VAX systems. Also, many of those users are extended well past the VAX's performance level and are committed to a large central host system. The chart depicting the relative performance of Digital's systems versus DPS 8 is included as Attachment 2.

24 June 1983

Both the DECsystem 10 and 20 operating system software (TOPS10 and TOPS20 respectively) are designed for the interactive environment with concurrent batch/remote batch capability available. This is an area where Honeywell excels compared to Digital. (A more complete competitive assessment is included as Attachment 3.)

A follow-up article in Computerworld (June 20, 1983, p. 69) noted that the DEC users are accepting the "cluster concept" as a replacement for mainframe systems. We question whether the users of large DECsystem 10s and DECsystem 2060s are really accepting the cluster concept. These users have generally developed plans and installation growth direction utilizing a centralized host system concept, which does not lend itself to "clustering".

Interestingly, the article speculates that the real reason for the "cluster concept" is Digital's inability to develop a "state-of-the-art" mainframe such as Honeywell's DPS 88 within a comprehensive timeframe. Sam Fuller, Digital's senior manager of corporate research and architecture, admitted their inability to meet the demand for a viable follow-on mainframe system. He also stated "It became clear to us (that Jupiter) would be a non-competitive machine by the time it reached our customers. It doesn't make any sense to deliver a non-competitive machine."

A major portion of the complete "cluster concept" will be accomplished utilizing software that is not yet developed and it's completion presents a major challenge to Digital. Again quoting Sam Fuller, "The magnitude of that software development should not be underestimated. This is what we are in the process of doing now."

The money budgeted for the Jupiter project will now be applied to the development of mainframe-to-micro communications software.

Also of real interest were his comments regarding the much delayed follow-on VAX system, code name VENUS, rumored to be at 3 MIPS. He said, "that development has our highest priority, but I don't think putting more money or people into it will make it happen any faster." The delivery of such a system is "probably a year off." This in face of Data General's announcement of their MV/10000 and Hewlett-Packard's announcement of their HP3000/68, both significantly more powerful than the VAX system.

24 June 1983

Right now, while a significant percentage of Digital 36 bit mainframe users are still disappointed and frustrated is an excellent time for the Honeywell marketing representative to offer them an attractive alternative - DPS 8 and DSA. The Honeywell alternative is a success story of compatible systems growth, "state-of-the-art" large mainframes and a full range product offering - micros to mainframes.

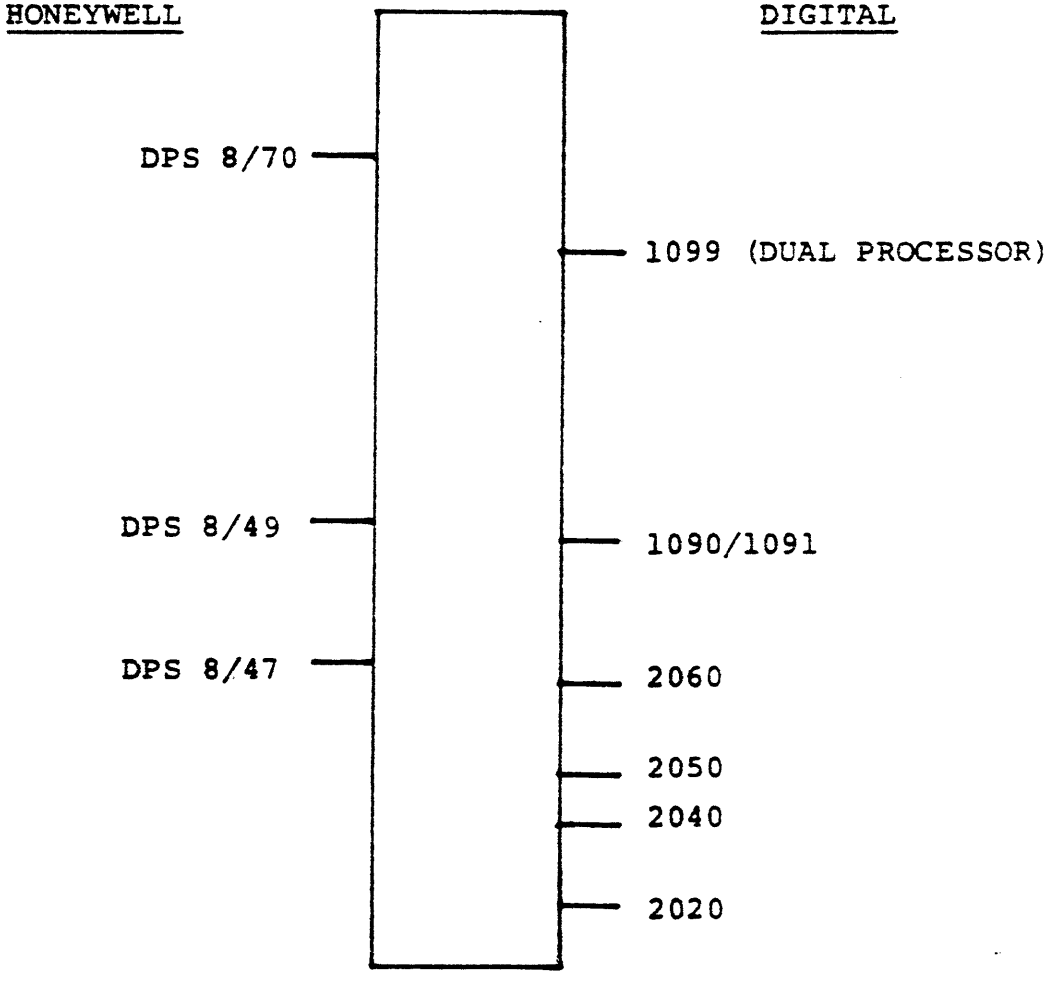
ATTACHMENT 1

DIGITAL EQUIPMENT CORPORATION
36-BIT MAINFRAME PARC

MODEL	FIRST CUSTOMER DELIVERY	NUMBER INSTALLED AS OF 1/1/82
2020	1977	365
2040	1977	172
2050	1975	
2060	1979	276
1040/50	1972	113
1060/70	Not Known	153
1080/90	1977	340
	TOTAL	1,419

ATTACHMENT 2

RELATIVE PERFORMANCE



ATTACHMENT 3
COMPETITIVE ASSESSMENT - DECsystems

HARDWARE

DECsystem 10 -

- First announced in 1971
  latest models 1090/1091 announced in 1977
- Symmetrical Multiprocessing (SMP) (tightly coupled) announced in 1979, with the model 1099.

DEC system 20

- First announced in 1976.
- Were marketing three models - 2020, 2040 and 2060.
- 2040 is upgradeable to 2060.
- No multiprocessing
- The ability to "cluster" systems (loosely couple) was announced in November, 1982.

HARDWARE SUMMARY

The hardware architecture is designed for scientific work rather than commercial work. However, the instruction set does include commercial type instructions.

Digital's hardware growth path is relatively limited; the 2020 cannot be upgraded. The 2040/2050 can be upgraded to the 2060. The 2060 cannot be upgraded. The DECsystem 20 also does not support multiple processor configurations, other than in a loosely coupled arrangement.

The DECsystem 10 is more powerful than the DECsystem 20, however, the design is also older. The DECsystem 10 tops out in the performance range of the DPS 8/70 single.

SOFTWARE

Operating systems are all interactively oriented -

- Patterned after MULTICS and CPV
- Everything in system considered to be time sharing, other dimensions are handled through sub-executives
- DECsystem 10s and DECsystem 20s have different operating system - TOPS10 and TOPS20 respectively

TOPS10

- Mainly a real memory system with virtual memory available as an option (VMSER).
- SMP version announced in 1979 to handle up to four processors.
- Batch work accomplished with a sub-executive (GALAXY-10)

TOPS20

- Virtual - demand paged system
- 256KW (36 bit word) program limit
- batch work handled through GALAXY-20
- 128 line limit - software limitation

SOFTWARE SUMMARY

Both DECsystems have a full complement of supporting software including a CODASYL compliant data base manager with it's complement of data manipulation and query software and excellent data communications and networking capability.

The software does not function as efficiently as Honeywell's in a full multidimensional environment. Digital also does not perform as well in the commercial environment with data base involvement.

ASSESSMENT CONCLUSION

Digital performs well in the interactive environment and the users are pleased with the system and are very loyal. However, they now have little or no growth path within the line.

The price/performance position of the Digital systems was never realigned following the announcement of the IBM 4300, which generally makes their systems more expensive in competitive situations.

Sales Aid

Cii Honeywell Bull

DPS 8

Internal use only

Published by : LARGE SYSTEMS MARKETING DIVISION Issue N° 128

Addressee : Date : August 1st, 1983

Product :

COMPETITIVE BULLETIN

Please find hereafter a Competitive Bulletin on the supplier of Large-scale Computer systems : CONTROL DATA CORPORATION - CDC.

P. CHASTRES
Large Systems
Product Marketing

W. KING GILLIES
Manager
Marketing Division

22 June 1983

SUBJECT: CONTROL DATA CORPORATION

Control Data - CDC - is a supplier of large-scale computer systems which have their major application in engineering/scientific environments. Honeywell has historically not offered systems targeted to the CDC marketplace, but CDC is attempting to expand its base into the commercial sector, introducing end-user facilities and ease-of-use products similar to those offered by Honeywell and other general-purpose vendors.

Corporate CDC includes, in addition to its computer business, ownership of Commercial Credit and the very large Service Bureau organization. It also has a majority holding in MPI (Magnetic Peripherals, Inc), the designer and producer of disk storage products. The balance of MPI is owned by Honeywell, Cii-HB and, most recently, Sperry. CDC's PLATO system, in conjunction with the computer business, has been in the forefront of computer aided instruction, although it has been somewhat troubled in terms of profitability.

Corporate revenues for 1982 were $4.29B, up 38% from 1981. Net income, however, was down by more than 9% for the period. There has been published speculation that CDC's computer business contributes a less profitable return than other corporate divisions, and that CDC may dispose of it. Ongoing product announcements, however, do not support such a conjecture.

Image/Marketing Strategy

Control Data's image as a large systems computer vendor is well established, and will remain unchanged so long as the CDC product line patterns remain unchanged. From the supercomputer CYBER 203 and CYBER 205 down through the more widely installed CYBER 170 machines, CDC's success and image are based on strengths in engineering/scientific computing. The 203 and 205 are in the computational ballpark with CRAY, some of the Japanese computers, the in-development TRILOGY, etc. Honeywell has no current product interest in that performance range.

The CDC scientific/engineering image persists in the more widely installed CYBER 170 series, and is supplemented by high performance in interactive processing. These systems have found wide acceptance in the university environment. In a 1982 proposal to an American university, CDC stated that 24% of CYBER's installed base is in the educational market. As a powerful timesharing vehicle, the CYBER system provides a good match for the needs of a student workload.

The CDC sales force is highly disciplined in prospect qualification, rarely entering a campaign with a "win" confidence level below 50%. Liberal discounts and trade-in allowances are offered in new-name situations and, like most vendors, CDC will submit very creative and attractive proposals to retain customers going out for new bids. If benchmarking is a consideration, CDC will often propose substituting an emulation process represented as satisfying the benchmark criteria.

CDC Large Systems

In 1979, CDC announced the CYBER 170 Series 700. The 700 provided upward compatibility with prior CYBER machines that were obsoleted by the price/performance characteristics of the 700 series. Then, in April of 1982, the 170/800 series was introduced with more than triple the maxiumum performance of the 170/700, and the 170/700 new build was discontinued. (The 170/700 may still be bid, at much reduced prices, if the situation does not prohibit proposal of used equipment.) As initially offered, the 800 series consisted of five models: the 825, 835, 855, 865 and 875. In February of 1983, an entry-level 815 was announced; in June, the mid-range 845 was released, with shipments scheduled for 4Q83. The seven models are available in nine mainframe configurations; the two top performers, the 865 and 875, offer a dual-processor option.

The CYBER 170/800 retains program compatibility with the CYBER 170 models and accommodates the same peripherals and front-end processors. Where the 170/700 was represented as field-upgradable within its model structure, that claim has not been observed for the 170/800. At announcement time, the entry machine was the 825, a machine with maximum memory of one megaword (64K chip) and a cooling requirement that could be satisfied with air conditioning. The next system above the 825 is the 835, a system with a two megaword memory limit using a 16K chip technology and requiring liquid cooling. The first upgrade from entry level

would require substantial hardware and site environment changes. In a subsequent action, CDC increased the 825 performance by 20% and introduced the 815 at about 60% of the 825 performance. That move brought the 800 series an entry-level machine that could be field upgraded. The performance range begins at about the level of an IBM 4341-2 and tops off well above the performance rating of IBM's 4-processor 3084. Using CDC's published MIPS ratings for the 170/800, these are the positionings:

170/815	1.1
170/825	1.7
170/835	3.5
170/845	5.4
170/855	8.0
170/865	11.0
170/865 Dual	19.3
170/875	19.0
170/875 Dual	32.0

These values are optimized around performance in a scientific/engineering batch application environment. There are benchmark reports of rated performances degrading by 40-50% in moving from pure batch to multidimensional processing.

The variations in rated performance are achieved by differences in memory cycle times, degrees of memory interlace, processor cache size options, instruction pipelining, and internal parallel processing.

Memory characteristics vary across the line, but word size is constant at 60 bits. CDC's internal decor is BCD, with various capacities expressed in terms of six-bit characters, e.g., the memory word has 10 characters. (There are operating system facilities for managing interfaces to ASCII and EBCDIC requirements.) Memory sizes are not notably large, with the maximum at 2048K words. Converting to bits, then to bytes, that maximum would translate to something under 16MB. Interestingly, the memory available with the two top 170/800 models (the 865 and 875) is limited to 1048K words. Even so, this capacity is four times that of the most powerful machines in the earlier 170/700 series. For the 170/865 and 170/875, an external Extended Semiconductor Memory is offered. Its capacity ranges up to 2048K words, and it has interfaces to the processor and to peripheral processing units. ESM is not

main memory -- instructions cannot be executed out of it -- but it serves as a disk cache and a high speed swapping device, with a transfer rate into main memory of 10 million words per second.

Price/Performance

The central system in a 170/800 contains a somewhat different complement of hardware functions than we include in the price of a DPS 8 mainframe. Recognizing some degree of error, it appears that DPS 8 and 170/800 are fairly close in price/performance at the CDC entry levels, where we would logically encounter the 170/800. An 8/49 and a 170/825 are very close in price/performance. In addition to the differences in hardware content for a mainframe price, CDC's performance ratings are biased heavily towards scientific/engineering batch processing. All things considered, DPS 8 and 170/800 are fairly close in the lower CDC performance ranges. At performance levels where DPS 8 has no product, CDC's price/performance ratio is very favorable:

CENTRAL SYSTEM	BATCH PERFORMANCE	PRICE/PERFORMANCE
DPS 8/49	.95	247K/MIP
170/825	1.70	220K/MIP
170/875	19.0	170K/MIP

Remember that Honeywell performance figures express a relationship to the performance of a 66/80; the .95 shown for the DPS 8/49 would be a somewhat higher figure when expressed, for example, in IBM MIPS. The 170/800 ratings are those expressed by CDC as "CDC MIPS". The vagaries of performance ratings, taken with the variations in hardware content per price, should qualify any price/performance analysis. And, as indicated, performance under NOS degrades significantly with the introduction of additional processing dimensions.

Software

The 170 series supervisor, NOS (Network Operating System), is an outgrowth of separate supervisors which were initially designed for either time sharing or batch emphasis. Announced

Data Communications

The 170/800 network processor is offered in two models; one (2551-1) supports up to 32 lines while the second (2551-2) can be expanded to accommodate 256 lines. Within its Network Communications System (NCS) CDC supports a selection of hosts, network processors, minicomputers, concentrators, intelligent workstations, interfaces to public data networks, and emulation of competitive interfaces (including Honeywell's HDLC).

Peripheral Subsystems

Disk Storage: CDC is currently new-building only fixed head-disk-assembly devices; these are the 885 series of devices, with characteristics much like those of our MSU0501. Within the series of 3 device models, one is available only to the 170/865 and 170/875, the two models accommodating Extended Semiconductor Memory, which functions as a disk cache. CDC offers disk drive access to up to 4 controllers; the controllers are available with up to 4 channels to peripheral processor units.

Magnetic Tape

The CYBER system magnetic tape devices are available in the conventional densities and transport speeds in 7 and 9 track configurations. NRZI, PE and GCR coding structures are offered (556/800 bpi, 800/1600 bpi, 1600/6250 bpi). Tape controls are offered in single and dual channel configurations.

Paper Media Subsystems

Card Reader:	1200 cpm
Card Punch:	250 cpm
Train Printer:	1200, 1600, 2000 lpm with 48-character set train

System Strengths

CDC's principal strength is its established reputation for fielding stable, very high performance mainframes. The CYBER systems continue to be very attractive to users with requirements for scientific/engineering performance or for single-dimension interactive power. Over a period of years a large body of applications software has accumulated for the classic CYBER environments. CDC can also offer Service Bureau

support for peak load periods or for backup. The PLATO Computer Aided Instruction system now runs as an application under NOS 2, which should make some contribution to 170/800 marketing. Having established the CYBER 170 series as the system of choice in specific technical application areas, CDC is continuing in its efforts to penetrate a wider market segment through introduction of easier-to-use software.

System Weaknesses

Some of the CYBER characteristics identified as strengths may work against CDC; its reputation for excellence in scientific, time sharing and educational markets may imply to some customers that it has limitations in the general commercial and business sectors. CDC is moving toward improvement of this position but there does not appear to be any customer ground swell outside CDC's traditional niches. Certain desirable features are not universally available in the CYBER machines, e.g., in the 800 series, only the top two of the seven models are offered in dual processor configurations. The operating system is not virtual, implying memory management overhead and program size constraints. There is also a need for the operating system to accommodate the differences between BCD and byte operations. We also note that the 800 series runs only on NOS 2 or NOS/BE, meaning that upgrades from some of the earlier models would require conversion to the new OS. The basic weakness of the 170 systems lies with their difficulty in managing the transitions between modes in processing a multidimensional workload.

Series 170/700 Installed Base

The CYBER 170/700 was introduced in 1979. By January 1, 1983, the census of installed systems, per IDC, was the following:

	U.S.	Outside the U.S.	Total
170/720	80	115	195
170/730	75	35	110
170/740	10	5	15
170/750	30	15	45
170/760	40	8	48
	235	178	413

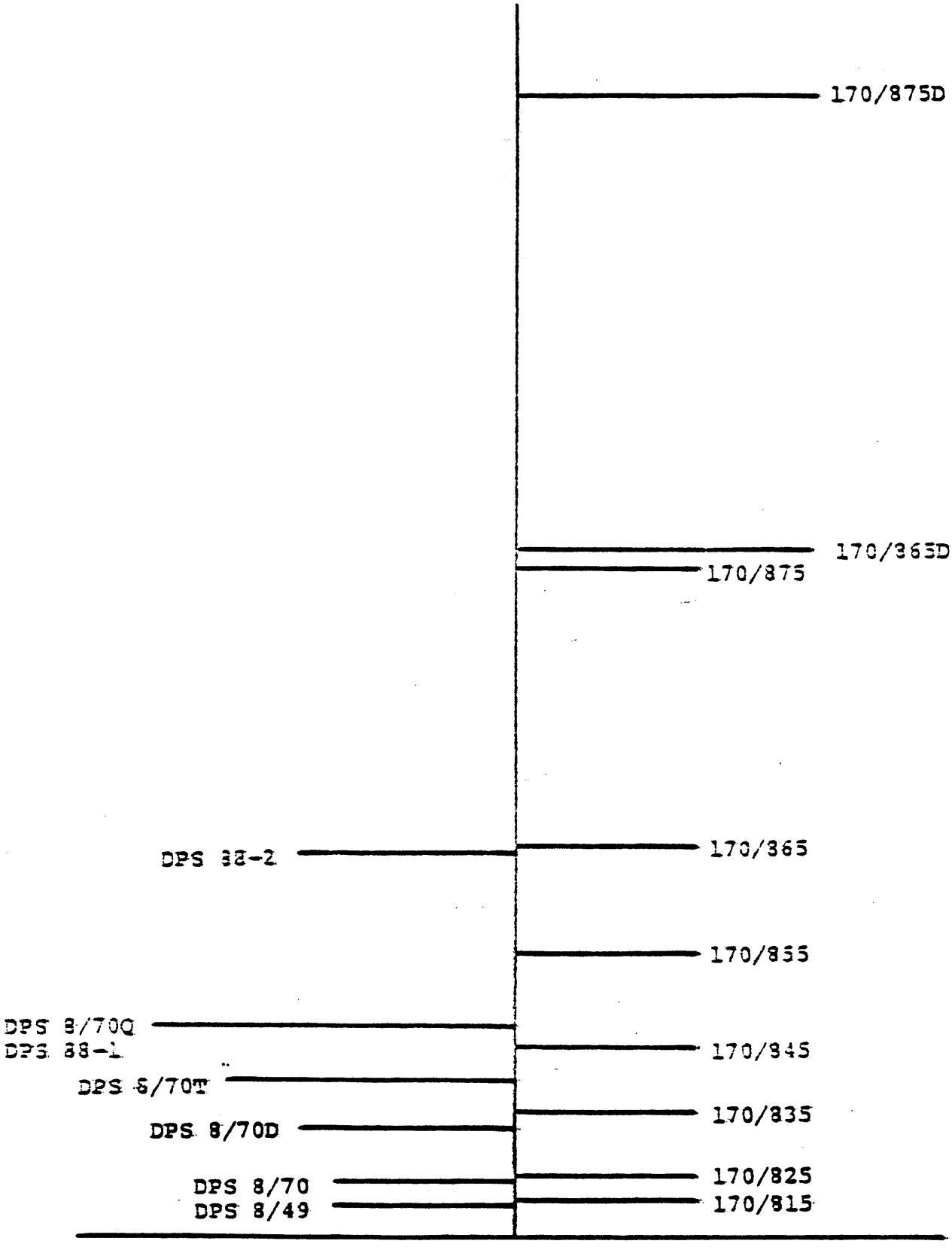
Series 170/800 data is not yet compiled.

22 June 1983

Batch Performance Ratings - Honeywell vs CDC

Attachment A presents the relative batch performance positioning of Honeywell DPS/8-DPS/88 and the CDC 170/800 family. Commercial transaction processing will tend to improve Honeywell's relative performance, but the degree of improvement is uncertain.

ATTACHMENT A



BATCH PERFORMANCE
DPS 8 - DPS 88 VS 170/8XX

with the 170/800, NOS Version 2 incorporates some features slanted towards the more commercial environments in which end users have come to expect ease-of-use facilities. NOS 2 is compatible with NOS/BE, a version of NOS incorporating Batch Extensions. NOS 2 also supports CDC's PLATO system running as a standard application alongside other applications; heretofore, PLATO has required a dedicated system. NOS 2 is not available to CYBERs other than the 170/800.

There is an extensive CDC library of scientific/engineering application programs available with the 170/800. System software includes:

- COBOL 5
- FORTRAN EXTENDED 4
- FORTRAN EXTENDED 5
- ALGOL 5
- APL 2
- BASIC 3
- COMPASS (Assembler)
- PL/1
- TOTAL
- IMF (Information Management Facility)*
- DMS-170 (CODASYL Compliant)

*IMF is an information base modeling tool that can be used as a production data base management system. It supports hierarchical and network structures, with interfaces to COBOL and FORTRAN.

Software Pricing

All software for the CYBER 170/800 is unbundled, including all NOS 2 modules. There are 4 classes of software, with assignment based on the degree of support commitment. There is another designation for each software product, based in this case on usage practice. Group A is a price category when the software is used on specific equipment, even when the equipment services other than the customer's internal users. Group B means that only the customer's internal processing can use the software. Group C is, in general, the category when non-profit educational institutions are using the software. Taking the above pricing considerations into account, CDC then charges differently for a given software product, depending upon which mainframe is in execution. BASIC, for example, rents for $174 on a 170/825, and for $684 on the 170/875. For all the variations, pricing schedules are available for:

- Paid-up License
- Initial Fee
- Monthly Right to Use
- Monthly Support

Sales Aid

Cii Honeywell Bull

DPS 8

Internal use only

Published by : LARGE SYSTEMS MARKETING DIVISION Issue N°130

Addressee :

Date : September 12, 1983

Product :

COMPETITIVE BULLETIN

Please find hereafter a very interesting analysis on the IBM Operating System MVS/XA. This analysis made by Honeywell is based on some views and opinions of Robert T. Fertig.

This analysis includes some subjects such as performance, conversion, cost and why MVS/XA for MVS/370 users. We can find also a comparison between IBM MVS/XA and GCOS 8.

P. CHASTRES
Large Systems Marketing Division

SUBJECT: IBM'S MVS/XA
A COMPETITIVE VIEW

WHAT IS MVS/XA?

MVS/System Product Version 2 Release 1 (MVS/SP 2.1) and MVS/XA Data Facility Product Release 1 (MVS/XA DFP1) are the official names for what are collectively referred to as MVS/XA. MVS/XA is then a generic name for a series of software releases. In a similar fashion MVS/370 is a generic name for the existing operating system officially entitled MVS/System Product Version 1 Release 3 (MVS/SP 1.3).

The terms MVS/XA, SP 2.1, and XA will be used interchangeably in this paper. Similarly the terms MVS/370, SP 1.3, and MVS will also be used interchangeably.

Included in the releases for MVS/XA are:

- Initial release - March 31, 1983 - MVS/SP 2.1.0 with MVS/XA DFP 1.0.
  FORTRAN and Assembler H languages - 31 bit mode. Statement of intent for 31 bit COBOL, PL/I and APL under TSO.
- June, 1983 release - MVS/SP 2.1.1 with MVS/XA DFP 1.1.
- CICS/OS/VS 1.6.1 - August, 1983
- RMF 3.2 - October, 1983 (Resource Measurement Facility).

- o 48MB support for 3081G's and K's - 4Q83
- o Support for IMS/VS data sharing and DBRC (Data Basic Recovery Control) - February, 1984
- o VM/XA Migration Aid - Promised 4Q83
- o Various other program products

XA is a new bimodal operating system. It is designed to handle as native programs that are written in both 24 bit mode (current MVS) and 31 bit mode (MVS/XA). MVS/XA requires 308X hardware. IBM has made no reference to retrofitting XA into the 303X series, although those machines can be used to "position" for MVS/XA migration and to do a sysgen for a 308X XA system.

No plans for XA have been announced for the 4341 family which can run MVS/370. There has been speculation in the trade press, specifically from the Gartner Group and EIS (Enterprise Information Systems), that IBM will announce a "bridge" machine for the 4341 family that will be compatible with existing 4341 and 308X models and have XA capability. In the opinion of Robert T. Fertig of EIS, it is unlikely that XA will be "downsized" for existing IBM models.

WHY IS IBM RELEASING MVS/XA?

According to EIS, current very large scale IBM MVS users are experiencing or anticipate serious production constraints. IBM confirms this in their XA announcements which speak of the removal of constraints. Among the constraints cited by R. J. Fertig in his article, "XA, THE VIEW FROM THE TRENCHES", in the May, 1983 issue of Datamation:

"

1. Limited address space of 16 megabytes stemming from the 24-bit address mode (25 bits with special 3033 SE feature)
2. Restricted number of channels, I/O bandwidth, and access flexibility
3. Maximum of two processors in a multiprocessor configuration
4. Lack of fault tolerance to meet the high reliability, availability, and serviceability (RAS) needs of the mid-'80s

5. Insufficient resource management facilities for large multiprocessor complexes."

Because of intrinsic limitations these constraints are not solvable under the current MVS architecture. Candle Corporation in its June 1, 1983 edition of Candle Computer Report states:

> "MVS/XA is designed to escape many of the 'large systems effects' which cause the throughput of an MVS system to saturate while some resources remain unused. Sequential searches and common queues, used widely in MVS, cause overhead to grow proportionately to workload."

Growth is the key element. In Fertig's analysis he comes to the conclusion that without XA, MVS cannot handle the anticipated growth of very large sites. According to a survey taken by EIS:

- 1982 average large IBM site had 11.4 MIPS of processor power. This will grow to a 23 MIPS average in 1985.

- Main storage (memory) growth will be from an average of 14MB in 1982 to 29MB in 1985. EIS makes some predictions that point out that their own survey is probably quite conservative. EIS predicts that there will be price erosion to the extent that 1MB of memory will cost $5K, and that this will stimulate sales to the extent that memory capacities will approach 100MB by the mid-80s. They further predict a ratio of 2MB/MIPS which would place the MIPS range at about 50.

  Real memory prices on a 308X class system have just declined from $25K/MB to $20K/MB. By 1985 it is likely that 308X class memory may decline to $10K/MB and that that would result in 60-70MB memories and 30-40 MIPS.

- DASD (Direct Access Storage Device - disk) capacity according to that survey will grow from 55.6GB in 1982 to 91.4GB in 1985.

  As the amount of disk capacity grows, the devices upon which it resides will gradually shift from 3350's to 3380's. Both 3350's and 3380's are fixed media devices. The amount of removable media capacity is expected to be rather insignificant.

As greater and greater disk capacities are kept on-line the problem of backup is compounded. It is likely then that the disk capacity buildup will result in the required presence of high-speed, high-capacity magnetic tape devices for the foreseeable future.

Disk buffering will also become critical by 1985. This fact coupled with dynamic I/O features of XA will force dependency on 3880 model 11 or 13 disk controllers and 3380 model AA4 disks. These disk controllers supply the hardware for the buffering and the disks supply the hardware for the dynamic connection capabilities of XA. These models of controllers and disks just happen to be the most expensive models in their respective families.

- In the area of communications, according to the survey, the average very large IBM site would grow from 65 lines and 537 terminals in 1982 to 91 lines and 880 terminals in 1985. EIS again differs from their survey predicting 2000 terminals requiring 50 MIPS by 1985.

- By survey, workloads are expected to grow by a combined CAGR of about 25%, but the various dimensions are growing at different speeds. Growth factors by 1985 would be as follows:

Batch	1.6 times
TP	1.9 times
TS	3.4 Times

The reason for the phenomenal growth of time sharing is said to be the presence of personal computers and graphics terminals, etc. This seems to differ from the Honeywell typical very large customer whose TP growth is greater and TS growth is slower. Perhaps some reasons for this are that IBM customers have not been into time sharing very actively in the past and because the greatest performance improvement promised by XA is in the time sharing (TSO) area.

TP work is becoming more complex. EIS quotes Dr. Glen Bacon of IBM as predicting that banking transactions would involve about 500,000 instructions per transaction giving one second response time. It would take about 25 MIPS to achieve a rate of about 50 transactions per second at such response time according to Dr. Bacon.

In a benchmark for a banking customer utilizing a DPS 8/70Q complex (about 6 MIPS) the system was able to sustain a rate in excess of 50 transactions per second.

In the IBM world, however, TS and TP work of this nature puts further strain on virtual storage address spaces and makes the move to XA the only solution for IBM.

VSPA (Virtual Storage Private Address) limit is what is forcing XA migration, according to Fertig. IBM calls this virtual storage constraint and its solution, VSCR (Virtual Storage Constraint Relief).

Under MVS each user in any dimension requires virtual storage address space and this space must be located in the first 16MB of virtual storage. According to the survey all very large scale MVS users are at or believe they will reach that limit by 1985.

Under XA, code and buffers are moved from space below 16MB to above it. Up to 2MB of virtual storage below 16MB will immediately be made available by a move to XA. This can be used for VSPA relief.

On the business and competitive side IBM also appears to have reasons for releasing MVS/XA. The PCM mainframers who are successful seem to be limited to the high end only. NAS and Amdahl do not seem to fear IBM and they expect strong 1983 shipments of their products. They have indicated their intent to support XA in the future. Perhaps IBM felt it could "beat them to the punch." That is questionable, however, since it was reported in a June, 1983 issue of Computerworld that Amdahl has announced XA support.

In an apparent attempt to forestall IBM's lead in implementation, the PCM's are pointing out difficulties of early conversion to XA according to the EDP Industry Report of April 15, 1983.

> "The PCMs are also quick to point out what can happen to conversion pioneers. MVS/XA contains an enormous amount of new code that has yet to be tested under diverse market conditions. Parallels to the difficulties in the early days of MVS/MVT/SVS are easily drawn, and since the VM migration aid won't be available until December, 1983, most users might be wise to wait and see for 1983."

XA is IBM's answer, though. It is implemented in an SCP over which they exercise complete control. The microcode will slow the PCM's and since initially 308X hardware is required it will boost sales. IBM's early action could very well "lock in customers", and it does answer their large uses needs for relief.

How good to make XA is a classic dilemma for IBM. According to the EDP Industry Report in the article, "IBM Releases MVS/XA Details, Conversion Battles Ready to Commence" in its April 15, 1983 issue, IBM could not afford to make too dramatic a change because they wanted to avoid a conversion rush which they could neither manage nor support. This point is also voiced by Fertig.

If MVS/SP2 performance were only equal to that of MVS/SP 1.3 many customers would delay a move to XA. If, however, MVS/SP2 performance represented a quantum leap of 25% or better, many (perhaps too many to manage) would rapidly move to XA; some might delay processor upgrades or actually downgrade hardware; residual values of 303X processors could be destroyed; IBM could actually help PCM's because their equipment could also show substantial performance improvement if they could support XA. To quote the EDP Industry Report, "The announced specifications reflect this timeworn juggling act".

WHO WILL MIGRATE TO MVS/XA?

If you ask IBM's largest users, as EIS did in their survey, the answer is, all of them, but EIS points out several facts and predicts that the migration might be less than the survey results indicate.

MVS/XA requires 308X hardware in place, and dedicated toward migration. XA requires the user to have implemented the "stepping stone" release of MVS/SP 1.3. According to IDC survey, only 17.4% of IBM users are running any level of MVS/SP (82.6% are not) and even of that 17.4% many of those are not at the SP 1.3 level. XA migration will be expensive and take time.

EIS predicts that 60-70% of IBM's very large scale users will have undertaken the migration to XA by 1985. The reasons why EIS predicts less of a migration to XA than their survey indicates include: IBM SE's are not fully trained; VM/XA Migration Aid will not really be ready for full use until 1984 since it will not be released until 4Q83; conversion/migration will take longer than the users expect; and no COBOL, PL/I or other 31 bit compilers except FORTRAN and Assembler H have been released.

The vast majority of IBM users will not migrate to MVS/XA. According to IDC survey 78.1% of IBM users are non-MVS. In the installed base, only 3% of the systems are 308X, the hardware requirement for XA. The 3083E is the entry level for 308X series. It has about 4 MIPS of power. There will be IBM users below 4 MIPS for the foreseeable future.

Also, IBM users have indicated in the past, a reluctance to migrate their operating system usage in the direction IBM would wish. For example, MVS was to become the only operating system. VM/370 was to be the "bridge" between DOS and MVS. IBM DOS users refused to move. The result was DOS/VSE and a viable VM/370. It is likely that some MVS users will move but not all, or even a majority, and IBM will have one more full-blown operating system to support.

WHAT IS IN IT FOR THE USER?

In his article, "XA, The View From the Trenches", Fertig says, regarding XA potential users:

> "Surprising and interesting is the fact that most users surveyed didn't know (or were unable to establish) what specific benefits they would gain from XA. Despite this they are undertaking the costly conversion/migration to XA."

These users apparently feel they must move. They are driven by the VSPA problem. XA promises them immediate and substantial relief, 1.3 - 2.4MB VSCR. They believe what IBM tells them and that XA's improved I/O capability will be translated into 30% improvement in I/O response time. They also look forward to a 10-30% reduction in software-caused IPL's (Initial Program Loads-Restarts) over MVS/SP 1.3.

In their view they can avoid redesigns of current applications to get around MVS problems by installing XA and with XA they can devote their development effort to exploit the 31 bit addressing capability. Thus they will be able to stave off possible future virtual storage size problems.

MVS/XA PERFORMANCE

In its announcement IBM presented performance figures. "For equal real storage, in unconstrained environments using a 32MB 3081K the user may anticipate MVS/XA performance vs MVS/SP 1.3 of +6% to -7%, the better (+6%) for a high-utilization TSO environment, and the poorer, (-7%), for a dedicated DB/DC environment. Batch performance falls within that range."

IBM adds, with a 16MB increment (to 48MB) it is estimated there could be 10% more TSO improvement.

It is interesting to note that all figures are based upon a 32MB 3081K. Are figures extrapolatable to other 308X models? MVS/SP 1.3 could use the top 16MB of a 32MB system for paging relief only. Does XA, which is said to locate part of itself in the upper 16MB, only give a maximum of 6% performance improvement? Also, if a 16MB increment can give a 10% TSO performance improvement, does it follow that 16MB less memory (a 16MB 3081K is marketed) would give a 10% degradation in TSO performance?

IBM also cites that with DPR (Dynamic Path Reconnect) a user can expect, with equivalent channel utilization, up to a 30% device response time improvement, or improved channel utilization with equivalent response time. This is probably quite true. It is, however, achievable only with the 3880 disk controller and 3380 model AA4 disks as heads of strings. Any other disks or disk models, such as 3380 model A4 or 3375 disks, would offer no relief.

CONVERSION

Of vital interest to users and potential users of XA is "How long will the conversion process take?". According to the previously cited EDP Review,

> "Conversion. It may be the ugliest word in the computer industry, upsetting the old order, forcing complex decisions, and tying up a user's best people in largely unproductive tasks. The bigger the system, the worse it gets."

Since MVS/XA involves the biggest sized systems, it must be pretty bad. According to the EIS Survey the positioning move to MVS/SP 1.3 should take from 7.8 to 14.2 man months and the move from SP 1.3 to MS/SP 2.1 (XA) from 17.5 to 32.4 man months. EIS and Fertig, once again, seem to differ with the opinions expressed in their own survey. They believe that the estimate of the positioning move is likely to be more accurate than the final move and that users tend to overestimate the final move. EIS seems to think that the move to SP 1.3 may well be more difficult than the move to XA. They do not seem

to dispute the total time for a user not yet at MVS/SP 1.3. Thirty-six man months seems to be the "magic" figure.

Converting to a basic MVS/XA is one thing, but exploitation of that which it provides could take many years. Old applications will have to be redesigned to take advantage of XA features. Eventually, all programs will have to be recompiled and relinked using new 31 bit compilers, and, of coure, everything will have to be tested.

WHAT WILL XA COST?

Using the previously described average of 36 man months and a loaded cost of $6,000 per man month we arrive at $216,000. EIS believes this to be a litle low considering increasing costs, etc. It looks for the gross cost to be in the neighborhood of a quarter of a million dollars and this is just the conversion/migration cost.

Besides this, there is, among other things, the direct cost of the software itself. EIS user's estimate an increase of an average of $4,582 during conversion and $8,917 after. EIS demurs and believes the costs during conversion will be much greater than those after. For one thing, there would be two sets of license fees, MVS and MVS/XA. They anticipate a minimum annual charge of $120,000 including Initial License Charges (ILC's) and maintenance, but excluding applications and other program products.

If history can be viewed as a guide, users can expect a 40-50% increase in software license charges over the budget years 1982-1985. IBM policies of allowing a two-month test allowance plus a three-month IIP (Installation Integration Program) waiver helps to soften the blow, but does not eliminate it. These test allowances and IIP's do not apply to the DSLO charges (Distributed System License Option) nor to the MVS production software which would continue to demand full charges.

PERSONNEL REQUIREMENTS

Staff to support an MVS/XA site is also expected to grow significantly. According to the EIS Survey, the IBM users expect their sites to grow from an average size of 150 people to a staff of 180 people by 4Q85 (20% CAGR). In terms of money that means a budget growth from $7.2 million to $12.5 million on average. The systems staff will also grow faster than other categories of personnel. It was reasoned by Fertig that this is likely to produce a "bubble effect", that is less resources for applications during the positioning and the actual conversion/migration while having an excess of systems people to support applications after the conversion/migration.

Fertig also makes another interesting observation. Burroughs, Univac and Honeywell sites generally have smaller staffs than IBM sites. He suggests that MVS sites have more staff beause they are generally more complex. One could wonder if it is the site or the operating system that is more complex. It is hard to imagine sites more complex and/or sophisticated than some of Honeywell very large ones.

CONCERNS OF IBM USERS

In the EIS survey IBM users expressed a number of concerns. These especially revolved around the relationship of XA and non-IBM developed software.

"o Most packages use assembler and reference MVS control blocks, will that delay my conversion?

o If IBM cuts back on mircofiche (or source code) will the software vendors have a hard time?

o How about compatibility and ease of conversion?

o Will the code run above the 16MB line?

o Timeliness and support for 31 bit addressing?

o Non-standard MVS interfaces, performance, software vendor cost justification in adjusting to XA.

o Will they work?"

The availability of source code and MVS/SP2 interface information appears to be the key issue. Fertig makes several salient points:

o It may not be in IBM's best interest to reveal these details, especially in view of the PCM position.

o To not reveal significant detail would hurt the marketability of some major independently-supplied software.

o Some of IBM's biggest and best customers are dependent on such software. IBM cannot ignore the concerns of these users. At the early support program (ESP) test sites few problems have been reported.

- o According to current IBM policy on the distribution of its license program source code and materials:
  - IBM will provide entries and exits for selected program products (not detailed specifications). This apparently applies to most XA program products
  - Source code will be available, but released only if IBM believes it necessary, and then only on a restricted basis.

COMPARISON TO HONEYWELL GCOS 8

In a limited sense MVS is to MS/XA as GCOS is to GCOS 8. MVS/XA evolved from MVS and GCOS 8 evolved from GCOS. In both cases, compatibility with the past is a dominent design goal. There the similarity ends, however. MVS/XA is designed for only the top of the line, the 308X series. This currently is composed of less than 3% of IBM mainframe type systems. GCOS 8, on the other hand, is applicable across the spectrum of large-scale products being offered today plus a large number of products not currently in production.

MVS/XA was created/evolved in order to solve a set of problems peculiar to MVS. It is a "state of the art" operating system, but it does not obsolete any other operating system: its own or its competitors. The problems solved by XA generally do not apply to GCOS or GCOS 8 since their design is radically different from that of MVS or MVS/XA.

In its press releases and announcements on XA, IBM properly and conveniently lists the highlights of each of the constituent parts of MVS/XA. It might be interesting to look at an inversion of those lists, since the inverse still applies to 97+% of IBM OS installations that are not XA and probably never will be. MVS/XA:

Highlight	Inverse
o Allows 24 channels on a uniprocessor	16 channels are maximum under MVS. GCOS 8 is only limited by the number of IOM/IOX's attached and could theoretically go to 96.

o Support of a 4 processor 3084 in a single image mode	Two tightly-coupled CP's are maximum under MVS. GCOS has supported up to six tightly-coupled CP's for years.
o Dynamic Channel reconnect	Fixed or dynamic channel options are available only under MVS or MVS/XA not any lower operating systems. To achieve any dynamic channeling, besides MVS or MVS/XA a 3880 disk controller and 3380 model AA4 disks are required. GCOS and GCOS 8 use a radial attachment scheme for disks and have at least as many paths to the data as there are disk devices regardless of the models of controllers or disks. This is inherently more flexible than dynamic path selection and/or dynamic path reconnect.
o Two billion bytes of virtual storage	MVS is actually restricted to 16MB. With 3033SE this is expanded to 32MB. The same limit applies to real memory. Then the top 16MB of a 32MB system is used to reduce paging. Relief with MVS/XA is dependent on moving things from the lowest 16MB to above the 16MB line. The virtual storage limit in GCOS 8 is over 8 trillion bytes. Real memory limitation is 128MB. There is no artificial 16MB line with GCOS 8.
o Up to 2.1MB of virtual storage relief	The need for VSPA space below 16MB has potential for problems, even with MVS/SA. GCOS 8 does not require private address space below 16MB line.

o Increased real storage capabilities	MVS/XA can now or will be able to handle 32MB, 48MB, (64MB?), (96MB?). MVS can handle 16MB (32MB with 3033SE). GCOS 8 can currently handle up to 128MB of real memory.
o Support for up to 4096 devices	2 to the 12th power = 4096. One gets the impression that 12 bits are now available to count devices. According to the MVS/ System Product Version 2 General Information Manual p. 2-7, "The maximum number of supported devices increases to 4096, however, the actual number of supported devices depends on the I/O configuration", and "changing the length of the unit control block (UCB) address from two bytes to three bytes enables UCBs to reside anywhere in the first 16 megabytes of storage". If the UCBs must still reside in the first 16MB of real storage, how does that grant any virtual storage constraint relief?

SUMMARY AND CONCLUSIONS

IBM is in a continuing process of releasing an evolved operating system for the high-end of its line. MVS/XA will start along the road to solution of several problems that beset MVS, for those who will install it. MVS, on the other hand, receives no promises of the retrofitting of XA features. MVS/XA does create a "showcase" platform for future operating system developments for its very large systems. It applies to a very small percentage of the IBM base.

MVS/XA represents a formidable technical challenge for IBM. For the first time in their history, IBM has released a tightly-coupled system with more than two CPs. For the first time IBM must support such a system through a new software offering.

MVS/XA may well do all that is claimed for it and be easy to install and operate, however, it offers no relief for the vast majority of IBM users; it creates another operating system for

IBM to support along with SSX/VSE, DOS/VSE, OS/VS1, OS/VS2 (MVS/SP 1.3), and VM/370; and it relies to a degree on VM/XA Migration Aid and SMP-E which have not been relesed yet.

MVS/XA costs more than what is being paid today, yet by IBM's own admission, in an unconstrained environment this represents a performance change of +6% to -7%. MVS/XA is clearly in IBM's best interest. The question to ask is "is it in the customer's best interest?".

Tech Aid

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GCOS-8 SR2300 MEMORY UTILIZATION

The attached report was prepared by H.I.S. MARKETING SOFTWARE DEVELOPMENT AND MIGRATION PLANNING PERSONNEL. It is intended to help you in preparing sites for the installation of GCOS-8 SR 2300.

This is a complement to the Tech Aid n° 134 (Aug.11, 1983) " GCOS-8 SR 2300 MEMORY UTILIZATION "

Prepared by

C. SOULIER

C. Soulier

Approved by

G. DER ANDREASSIAN

I. INTRODUCTION

The purpose of this paper is to provide general information on GCOS 8 SR2000 and SR2300 memory utilization compared to GCOS SR4JS3. Guidelines and examples are given to aid in the determination of how much, if any, additional memory should be installed before a site places GCOS 8 into production.

GCOS 8 is architecturally different from GCOS and manages memory differently. For instance, more memory can be configured with GCOS 8 than GCOS. GCOS 8 has greater functional capabilities and is a larger operating system. The focus of this paper is on presenting enough detail so that one can determine the amount of incremental memory necessary to support an existing GCOs site and that site's existing work load.

The following chart shows the major categories for which memory utilization guidelines were developed and the key factors that affect the amount of memory used. In some cases, the key factors affect GCOS 8 and GCOS memory utilization equally. In other cases, the factors have a different affect on GCOS 8. The guideline text in Section II attempts to describe each situation. There are also some sample comparisons following the guidelines.

GCOS 8 - MEMORY UTILIZATION CATEGORIES AND KEY FACTORS

CATEGORIES	DESCRIPTION	KEY FACTORS AFFECTING SIZE
HARD CORE MONITOR (HCM)	Basic OS that is "wired down" and resident whenever the OS is loaded	# of Program-Numbers Size of Trace Table Incore Available Space Table (IAST) System Size
SYSTEM PROGRAMS	Swapable Privileged Slave Programs such as Peripheral Allocator, SYSOUT, etc.	Amount and Type of Work Being Done Amount of Swapping That is Tolerable
TSS	Time Sharing Subsystem	# of Users and Subsystem Size Terminal Type Response Time Requirements Application Size Multiprogramming Depth
TP	DM-IV/TP	# of Control Tasks # of DB Buffers and Size # of MSG Buffers and Size # of MSG IDS TPR Area # of Subschemas
TDS	TDS	(Same as for TP Except # of Subschemas)
INTEGRATED SOFTWARE	GCOS 8 SHARED SOFTWARE	Use of UNPURGE # of Protected Files # Buffers Per Protected File Control Interval Size Use of AFTER Journal # of Jobs Using BEFORE Journals # Updated Control Intervals Per Commitment Unit
BATCH, TPE, OTHER	All Other Type Slave Jobs	Process Structure Space

II. GCOS 8 MEMORY GUIDELINES

1. HCM

Key Factors:
- # of Program-Numbers (PSUM)
- Size of Trace Table
- Incore Available Space Table (IAST)
- System Size

GCOS 8 allows for more program numbers than GCOS. The size of a number of internal tables depends on the number of program numbers established by a site.

GCOS 8 has a four word trace entry while GCOS uses two word entries. Thus additional GCOS 8 space is required to handle a like number of items.

The IAST memory consumption by GCOS 8 is comparable to that of GCOS. The size of the system represented by the amount of hardware, particularly peripherals, effects the size of the HCM, but in a manner analogous to GCOS.

GUIDELINE #1

The GCOS 8 SR2000 HCM requirement will range approximately 55K to 75K words more than the GCOS SR4JS3 HCM requirement, assuming the same amount of Program-Numbers (64), Trace Table size, and AST usage. GCOS 8 SR2300 will require approximately 5K words more than SR2000.

The following table shows the additional HCM requirements for selected PSUM values.

PSUM	(K WORDS)
65-164	2.4
165-264	4.7
265-364	5.9
365-464	7.1

2. SYSTEM PROGRAMS

Key Factors: Amount/Type of Work
Amount of Swapping

The amount of reasonable space for the system programs is the most subjective element in the memory comparisons. In general, the GCOS 8 System Programs are larger than those in GCOS and one should anticipate additional memory for their use. The amount of additional memory depends on how much work a system is doing (a function of its load and MIP rate) and the amount of swapping that will be done if insufficient space is provided.

The following programs were included in the category of System Programs for this comparison:

POPM
PALC
GEOT
SCHED
FSYS
HEAL
WIDEO

GUIDELINE #2

GCOS 8 SR2000 System Programs are a total of 42K words larger than they are in GCOS SR4JS3. GCOS 8 SR2300 System Programs are a total of 9K words larger than SR2000. Since all programs would not be memory resident simultaneously, a nominal additional memory requirement would be approximately 14K words.

3. TSS Key Factors: # of Users and Subsystem Size.
Terminal Type (VIPs vs. No-VIPs).
Application Size
Response Time Requirements

There is no GCOS 8 change affecting the subsystem size; it remains a function of the number of users and the types of subsystems required. GCOS 8 TSS is larger than GCOS TSS. The table below depicts the comparable sizes based on number of users and a no-VIPs and an all VIPs case. In actual practice the terminal types will be some mixture and the TSS size will be between the values shown.

Each active subsystem requires a logical work space (LWS) in which to execute. The number used is a function of the subsystem multiprogramming depth. 1K words of memory are required for each three LWS activated. The LWSs are used only while the subsystem is loading, swapping, or is in memory. A LWS is not required for each user logged into TSS. The numbers below provide LWS, ranging from 1K for the 5 terminal case to 6K for the 100 terminal case.

TSS Size (KWords) - Does Not Include Subsystems

# Of Users	No-VIPs GCOS/GCOS 8	All-VIPs GCOS/GCOS 8
5	29/42	33/47
10	30/44	37/51
25	34/54	51/69
50	40/62	74/90
100	52/83	122/137

GUIDELINE #3
13K to 31K additional TSS space is required with GCOS 8 SR2000 or SR2300. The increment depends on the number of users and terminal type.

4. TP and TDS

Key Factors: # of Control Tasks
# of DB Buffers and Size
# of MSG Buffers and Size
# of MSG IDs
TPR Area

TDS and DM-IV/TP are about 5K words larger on GCOS 8 for comparable parameters in the key factor area.

GUIDELINE #4
TDS and DM-IV/TP require 5K additional memory on GCOS 8 SR2000 or SR2300.

5. INTEGRATED SOFTWARE

Key Factors:
- Use of UNPURGE
- # of Protected Files
- Control Interval Size
- # of Buffers Per File
- # Jobs Using BEFORE Journals
- Use of AFTER Journals
- # of Updates Per Committment Unit

The amount of real memory (RSPACE) established by the site for executing integrated software can impact system performance. The size of real memory can be adjusted by a site by applying a patch in the Startup deck. A site will have to experiment to obtain the optimum memory size for the integrated software based on page faults and performance during production operation. An algorithm and detailed information for calculating the RSPACE value is provided in the GCOS 8 Software Release Bulletin (SRB) and the "GCOS 8 OS System Software Installation" manual (DH42).

GUIDELINE #5

The default value for RSPACE is 70K. The minimum allowable is 40K. If UNPURGE is the only usage, specify an RSPACE value of 50K. If Protected Files are used, the size can grow significantly. A practical minimum of 150-200K words is typical for many sites using Protected Files.

The Integrated Software memory contains a replacement for the FMS Protection Tables space in the HCM of GCOS, thereby eliminating the restriction of 300 entttries that prevails with the FMS Protection Tables.

6. BATCH, TPE, ALL OTHER

GCOS 8 requires 2-6K more words per job than does GCOS SR4JS3 for the operating system support associated with each job (Page Tables, SYSOUT, etc.,). This is what accounts for the 5K increase in the TDS and TP sizes shown earlier. Also, each process using protected files will use approximately 10K words more.

GUIDELINE #6
All active jobs require an additional 2-6K words of memory on GCOS 8.

The additional memory is part of the "process structure" and does not require the modification of any LIMITS.

7. OTHER CONSIDERATIONS

GCOS 8 provides some capabilities that are not available with GCOS III. Obviously, the selection and use of these options results in the use of additional memory. Examples of items in this category would be the specification of additional memory (Extended) for Time Sharing, TDS, or DM-IV/TP. A site can also choose to use more program numbers with GCOS 8 than are available on GCOS, resulting in an increase in the size of system tables and queues.

There is an SSA segment in GCOS 8 that resides in HCM, contributing to the HCM size. In GCOS, the SSA Cache is outside the 64K fence and is not considered as a part of the HCM.

GUIDELINES FOR MINIMUM MEMORY REQUIREMENTS (IN K WORDS)

	CATEGORY	GCOS	GCOS 8	GCOS 8 COMMENTS
A.	HCM	45	100	188 Largest Amount Observed on GCOS 8
B.	System Programs (PALC, GEOT, ETc.)	50	64	
C.	Time Sharing with 25 Terminals			
	Non-VIPS/VIPs	35/50	55/70	
	Subsystems (Mail, etc.)	40	40	
D.	DP (Assume 25K TPR Area)			
	No-DDE/DDE	95/100	100/105	Average Loading
E.	TDS (Assume 25K TPR Area)	90	95	
F.	Integrated Software (SHARD)	-	40K	Plus Protected File Requirements
G.	Batch, All Other GCOS 8 Increment		+2 to 6	Per Job

EXAMPLES OF WHAT COULD FIT IN TWO MEGABYTES (IN K WORDS)

	TSS/TP/BATCH	TSS/BATCH	TP/BATCH
NCP	125	125	125
System Programs	64	64	64
TSS w/25 Terminals	100		
TSS w/100 Terminals		200	
TP	100		200
Integrated Software (No Protected Files)	40	40	40
Batch	83	83	83
Totals	512	512	512

LARGE SYSTEMS

PRODUCT GUIDE

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PRODUCT GUIDE

A. CHRISTIANSEN
Large Systems Marketing Division