HONEYWELL

DATANET 66 SYSTEM & INSTALLATION MANUAL

CUSTOMER SERVICES

DATANET 66
SYSTEM AND INSTALLATION MANUAL

SUBJECT

Detailed Explanation of the Relationship of the Components within the DATANET System with Procedures for Installing, Testing, and Maintaining the System. A Parts Catalog is also included.

SPECIAL INSTRUCTIONS

This manual has been revised to the -400 level. It supersedes all previous issues.

Includes Update Pages Issued as Addendum A Dated November 1980, Addendum B Dated November 1981, Addendum C Dated May 1983, and Addendum D Dated December 1983.

The following notice is provided in accordance with the United States Federal Communications Commission's (FCC) regulations.

Warning: This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instruction manual, may cause interference to radio communications. The equipment manufactured after October 1, 1983 has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. As temporarily permitted by regulation the equipment manufactured prior to October 1, 1983 has not been tested for compliance. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

ORDER NUMBER FN01-03

DOCUMENT NUMBER 71010950-400

May 1980

Honeywell

RECORD OF REVISIONS (ROR)

REVISION	DATE	AUTHORITY	AFFECTED PAGES
-200	October 1977	BLCD87172	Entire Manual
-201	May 1978	BLCO80649	Front Cover, Title Page, ROR, 3-10, 3-11, 3-10, 3-27, and 3-30.
-300	February 1979	BLCO71472 BLCO80282 BLCO80326 BLCO80459 BLCO80652 BLCO80708 BLCO81672 BLCO81684	Entire Manual
-301	July 1979	BLCO81713 BLCO90181 BLCO90351 BLCO90420 BLCO90646 BLCO90939	Title Page, ROR, v, vi, vii, viii, 2-31, 3-9, 3-10, 3-11, 3-19, 3-26, 3-26.1/3-26.2, 3-29, 3-30.1/3-30.2, 3-33, 3-34, 3-42, 3-44, 3-47, 3-50, 3-54, 3-54.1/3-54.2, 3-55, 3-61, 3-68, 3-69, 3-70.1/3-70.2, 3-87/3-88, 4-2, 4-3, 4-4, 4-8.1/ 4-8.2, 4-13, and 4-22
-400	May 1980	BLCOA0451	Entire Manual
-401	November 1980	BLCOA1479	Title page and ROR
-402	November 1981	BLCO91739 BLCOA0020 BLCOA0021 BLCOA0250 BLCOA0353 BLCOA0446 BLCOA0481 BLCOA0559 BLCOA0842 BLCOA0943 BLCOA1237 BLCOA1405 BLCOB0460	See collating instructions

RECORD OF REVISIONS (ROR)

REVISION	DATE	AUTHORITY	AFFECTED PAGES
-403	October 1982	BLCOA0225 BLCOA0471 BLCOA0627 BLCOA0718 BLCOA0738 BLCOA0816 BLCOA1111 BLCOA1192 BLCOA1386 BLCOA1737 BLCOB0448 BLCOB0815 BLCOB1580 BLCOB1841 BLCOB7672 BLCOB7846 BLCOC0836 STARI14821 STARN21608	See collating instructions
-404	December 1983	BLCOD1884	See collating instructions

CONTENTS

CONTENTS

CONTENTS

CONTENTS

CONTENTS

ILLUSTRATIONS

ILLUSTRATIONS

ILLUSTRATIONS

ILLUSTRATIONS

TABLES

I
INTRODUCTION

1.1 SCOPE AND PURPOSE

This manual provides the Field Engineering Representative with an explanation of the relationship of the components within the DATANET system and with the procedures for installing, testing, and maintaining the system. A parts catalog is also included.

The DATANET system, hereafter referred to as the system, is designed to function as a Front-End Network Processor (FNP) for the L66 computer and comes in several configurations.

This manual consists of the following sections:

- Section I, Introduction
- Section II, System Description
- Section III, Installation
- Section IV, Fault Analysis
- Section V, System Parts Catalog

1.2 APPLICABLE DOCUMENTS

Documents are available that provide additional information on the system components. Each system is shipped with a complete set of microfiche (order number FX23) and with hard copies (order numbers AY34 and FN01).

Individual manuals can be ordered from the Publications Distribution Center by submitting a Publications Order Form.

Honeywell Information Systems Inc.
Publications/Computer Supplies
Distribution Center
47 Harvard Street
Westwood, Mass. 02090

1.2.1 Product Manuals on Microfiche

The following manuals are included as part of the DN66 product manual microfiche set (order number FX23). They are supplied as a complete set and cannot be ordered separately.

MICROFICHE ORDER NO.	TITLE	MANUAL ORDER NO.	DOCUMENT NUMBER
FX06	DCF6607 Channel Interface Base Controller	FX21	71010665
FX25	DN66 System and Installation Manual	FN01	71010950
FX26	Power System	FM90	71010291
FX27	Central Processor Unit	FN16	71010951
FX28	Input/Output Multiplexer	FN06	71010953
FX29	Direct Interface Adapter	FN10	71010955
FX30	Page Control Unit	FN14	71010985
FX31	Peripheral Interface Adapter	FN08	71010987
FX32	Cache Memory Unit	FN04	71010989
FX33	Double Word Fetch Main Memory	FN02	71010991
FX34	Single Word Fetch Main Memory	FP97	71010959
FX35	DCF6609 Channel Interface Base Controller (BSC Version)	FM56	71010435
FX37	System Support Channel	FM37	71010214
FX38	DCF6610 Asynchronous Current Loop Adapter	FK93	71010993
FX39	DCF6611/6618 Dual Synchronous Adapter	FN51	71010973

MICROFICHE ORDER NO.	TITLE	MANUAL ORDER NO.	DOCUMENT NUMBER
FX40	DCF6612 Dual Asynchronous Adapter	FN53	71010975
FX41	DCF6613 Dual Autocall Adapter	FN43	71010963
FX42	DCF6614 MIL-STD-188C Adapter	FN45	71010965
FX43	DCF6615 MIL-STD-188C Asynchronous Adapter	FQ59	71010453
FX44	DCF6616 MIL-STD-188C Broadband Adapter	FQ60	71010454
FX45	DCF6619 Synchronous Current Mode/DCF6621 Bisynchronous Communications Line Adapter	FN47	71010967
FX46	DCF6620 HDLC Adapter	FN41	71010961
FX47	DCF6627 Synchronous Balanced Line Adapter	FN49	71010969
FX48	SSC Console Adapter	FM73	71010244
FX50	SSC Diskette Adapter	FN26	71010246
FX51	DCF6622 HDLC Broadband Current Mode Adapter	FP98	71010447
FX52	DCF6623 HDLC Balanced Line Adapter	FP99	71010443
FX61	DCF6617 MIL-STD-188C HDLC Adapter	FQ84	71010269
FZ64	Single-/Double-Word Fetch Memory Controller	FY27	71010996
VA21	DCF6617/6620 HDLC Medium-Speed Controller	FY42	71010629
VA22	DCM6603/6604/6651 16K Expanded Memory	FZ38	71010763
N/A	HNP Equivalency Tables	N/A	N/A

1.2.2 Product Manuals Available Only in Hard Copy

The following manuals are not on microfiche but are available as hard copy (printed) manuals.

TITLE	MANUAL ORDER NO.
DN66 Network Processor Operation Manual	AY34
Remote Terminal Supervisor Manual	DD40
Network Processing Supervisor Manual	DD48
GRTS II Startup Procedures	DG14
DN66 Site Preparation Manual	DC79

1.2.3 Reference Manuals Available

The following system reference manuals are available. For information on each peripheral device, refer to the Outside Vendor Peripheral (OVP) device manual.

REFERENCE MANUAL	DOCUMENT NO.	ORDER NO.	BOARD LEVEL
Central Processor Unit (includes CPU PROM-PAC)	71010952 71010980	FN17 FP68	2.0 2.1
Main Memory (includes Memory-Pacs)	71010992 71010574 71010575 71010608	FN03 FP53 FP54 FP87	2.0 2.1 2.2 2.2
Cache Memory (includes Cache-Pac)	71010990	FN05	2.0
System Support Channel (includes SSC PROM-PAC)	71010216 71010979	FM62 FK89	2.0 2.1
SSC Diskette Adapter	71010247	FN27	2.0
SSC Console Adapter	71010245	FM74	2.1
Input/Output Multiplexer	71010954 71010567	FN07 FP47	2.0 2.1
Page Control Unit (includes PAT-PAC and PATN-PAC)	71010986	FN15	2.0
Peripheral Interface Adapter (includes PIA Interface-Pac)	71010988 71010617	FN09 FQ38	2.0 2.1

REFERENCE MANUAL	DOCUMENT NO.	ORDER NO.	BOARD LEVEL
Direct Interface Adapter (includes DIA Interface-Pac)	71010956 71010566	FN11 FP46	2.0 2.1
DCF6605 Channel Interface Base (HDLC) Controller	71010436	FM61	2.0
DCF6609 Channel Interface Base (BSC) Controller	71010590 71010572	FP70 FP71	2.0 2.1
DCF6610 Dual Asynchronous Current Loop Adapter	71010616	FP95	2.1
DCF6611/6618 Dual Synchronous/Bisynchronous Line Adapter	71010947 71010611 71010560	FN52 FP90 FP40	2.0 2.1 2.2
DCF6612 Dual Asynchronous Line Adapter	71010582 71010609	FP61 FP88	2.1 2.2
DCF6613 Dual Autocall Line Adapter	71010964 71010404	FN44 FN86	2.0 2.1
DCF6614 MIL-STD-188C Line Adapter	71010966	FN46	2.0
DCF6619/6621 Synchronous Current Mode Line Adapter	71010591	FP71	2.1
DCF6620 HDLC Control Adapter	71010962 71010406	FN42 FN88	2.0 2.1
DCF6622 HDLC Broadband Current Mode Line Adapter	71010451	FP17	2.0
DCF6623 HDLC Broadband Balanced Line Adapter	71010452	FP18	2.0
DCF6627 Synchronous Balanced Line Adapter	71010563	FP43	2.1

NOTE

The document number and the order number change as the board level changes.

1.3 SYSTEM COMPONENTS

The system is made up of the following components:

- CPU and Operator Control Panel
- Memory (24K words to 256K words of 18-bit EDAC)
- Page Control Unit - optional
- Cache Memory - optional
- Input/Output Multiplexer
- Direct Interface Adapter
- Peripheral Interface Adapter - optional
- Channel Interface Base - optional (HMLC)
- System Support Channel
- Power Supplies.

1.4 PHYSICAL DESCRIPTION

Figure 1-1 shows the basic system components. For detailed drawings of the system cabinets, refer to Section V.

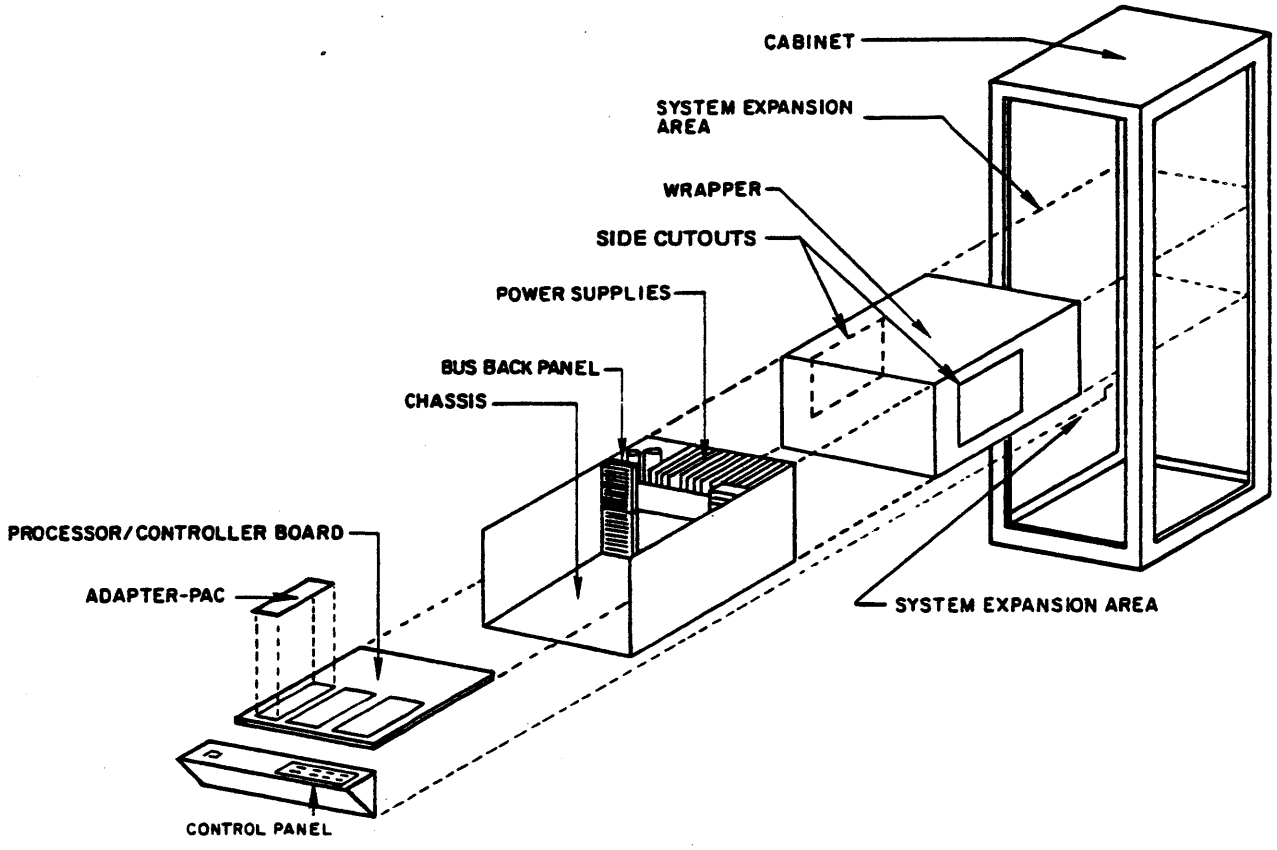


Figure 1-1 System Components

1.4.1 System Cabinet Configurations

Figure 1-2 shows the front view of the cabinet configurations that are used on the system. The dimensions of these rack-mountable cabinets are:

- Height: 62.0 in. (157.48 cm)
- Width : 27.0 in. (68.58 cm)
- Depth : 37.0 in. (93.98 cm)

The cabinets are capable of housing four 10.5-inch (26.67-cm) chassis, one Power Distribution Unit (PDU), a diskette, and a diskette power supply.

Cabinet BRCK181A is the original system cabinet and is capable of handling a maximum of 96 communications lines. It is no longer available for new installations and is replaced by BRCK183A, which accommodates a maximum of 64 communications lines with bulkhead cable connections in a stand-alone environment. When more than 64 communications lines are required, an expansion cabinet (BRCK012A) is bolted to the basic cabinet. The expansion cabinet contains the cable bulkheads and the basic cabinet contains the power supplies and logic assemblies.

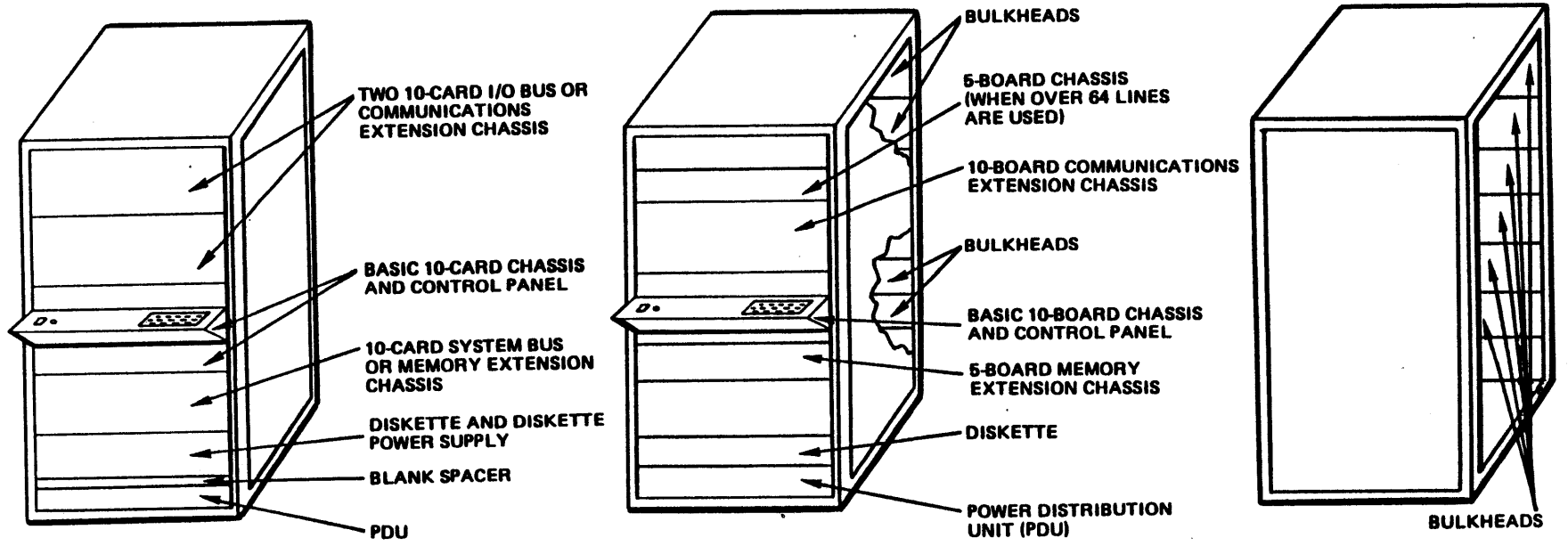
1.4.2 Chassis

The 10.5-inch (26.67-cm) basic or extension chassis holds the processor/controller boards that are specified by the configuration rules (refer to subsection 3.5.2). The basic system is housed in the basic split bus chassis; the upper half is the I/O bus, the lower half is the system bus (see Figure 1-3).

NOTE

The Input/Output Multiplexer (IOM), which is contained on two boards, is the only logic unit that plugs into both the I/O and the system bus (see Figure 1-3).

Extension chassis have only one bus (I/O or system bus), depending on their location in the cabinet. One extension is permissible in the lower cabinet (memory expansion) and two extension chassis are permissible at the top of the cabinet (communications expansion).



NOTE

IF 65 OR MORE LINES ARE REQUIRED, BOTH CABINETS BRCK183A AND BRCK012A ARE USED. ALL COMMUNICATIONS BULKHEADS ARE TO BE INSTALLED IN THE BRCK012A CABINET.

Figure 1-2 System Cabinet Configurations (Front View)

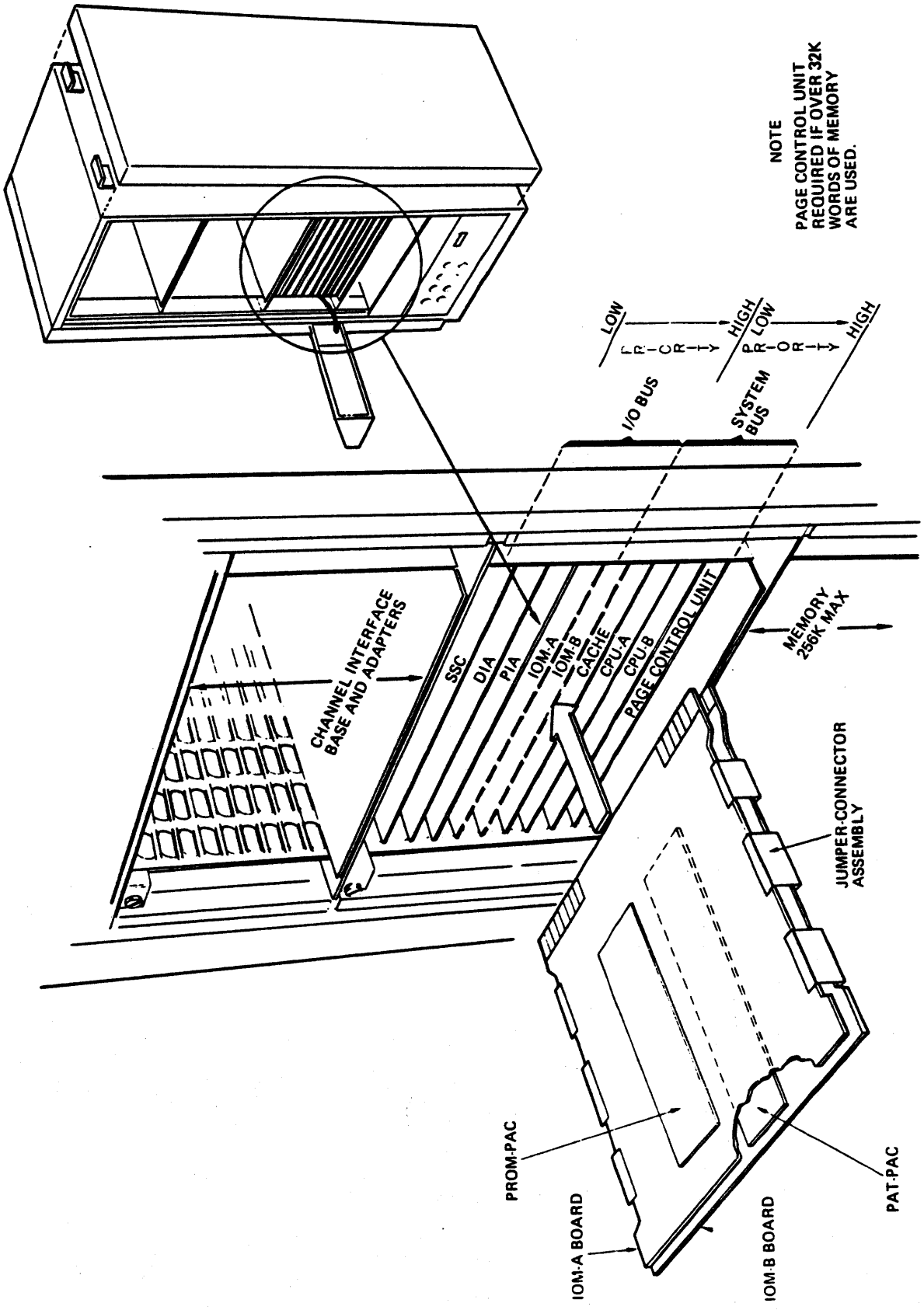


Figure 1-3 System Configuration

1.4.3 Wrapper

The wrapper, which is a sheet metal assembly, encloses the individual chassis assemblies. The wrapper has cutout areas to allow the installation of the interconnecting cables.

1.4.4 Processor/Controller Boards

The processer/controller boards are 15-inch (38.10-cm) by 16-inch (40.10-cm) printed wire assemblies designed to house an entire logic unit such as a memory controller or device controller. The boards plug into a bus that is the interface between the boards. A board is capable of supporting a maximum of four Adapter-Pacs, which are mounted piggyback style (see Figure 1-4).

Processor/controller boards can be paired to make a logic unit that is too large to fit on a single board. The system IOM is on a pair of boards; the CPU is also on a pair of boards. The pair of boards are interconnected by jumper connector assemblies, which connect to the side of the boards. These jumper connector assemblies (see Figure 1-5) serve to interconnect signals on the two boards. The CPU has four jumper connector assemblies (two on each side); the IOM has six jumper connector assemblies (three on each side). There is also a mechanical connection between the two boards in the form of spacers.

1.4.5 Adapter-Pacs/Option-Pacs

The Adapter-Pacs/Option-Pacs (see Figure 1-4) are small printed wire assemblies that plug into other boards. Their sizes are:

- 11.5 in. (29.21 cm) by 3.5 in. (8.89 cm)
- 11.5 in. (29.21 cm) by 7.0 in. (17.78 cm)
- 11.5 in. (29.21 cm) by 10.5 in. (26.67 cm)

Adapter-Pacs/Option-Pacs can be additional logic carriers or device interface modules, which provide cable ports to the various I/O devices.

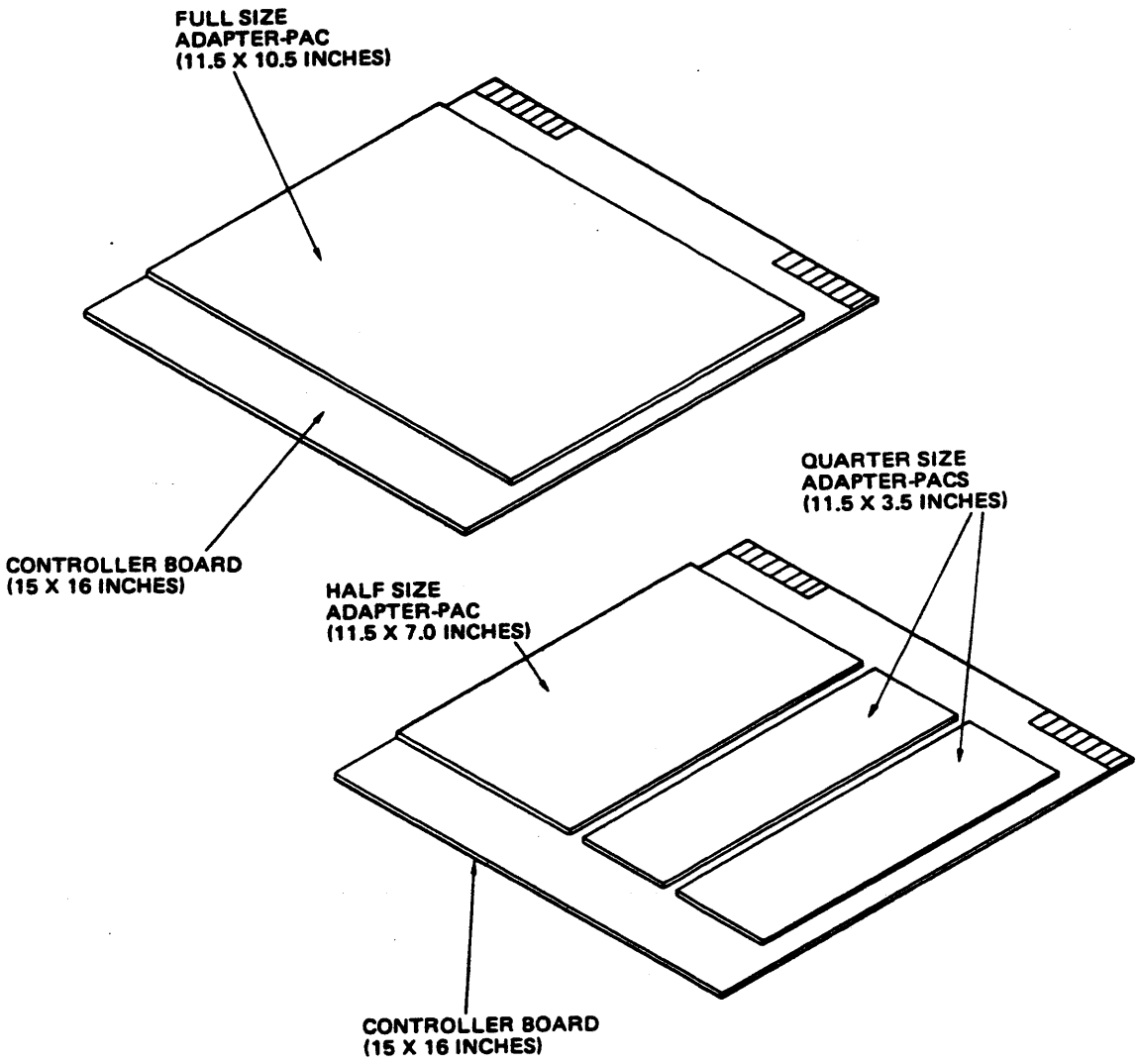


Figure 1-4 Controller Board to Adapter-Pacs Relationship

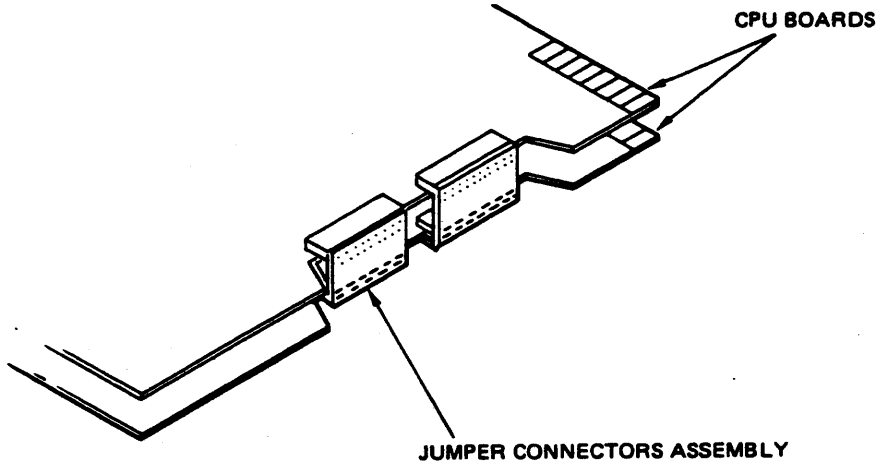


Figure 1-5 Board Jumper Connections

1.4.6 Operator Control Panel

Figure 1-6 shows the operator control panel. The control panel provides a means of initializing the system, starting and stopping the CPU, entering and displaying the registers and memory, single stepping a program, booting a program, master clearing the system, and indicating the CPU routines.

1.4.7 Power Supplies

1.4.7.1 System Power Supplies

The following information relates to the system power supplies:

- Input: 208 Vac at 60 Hz 3 Phase
- Output: +5 Vdc, +12 Vdc, -12 Vdc, and +18 Vdc
- Location: There are two power supplies for every 10-card chassis. The power supplies are at the rear of the chassis and are accessible from the rear of the cabinet.

1.4.7.2 Diskette Power Supply

The following information relates to the diskette power supply:

- Input: 120 Vac at 60 Hz or 220/240 Vac at 50 Hz
- Output: +24 Vdc, +5 Vdc, and -5 Vdc
- Location: The power supply is located at the rear of the diskette chassis and is accessible from the front of the cabinet.

1.4.8 Environmental Characteristics

The following information relates to the environmental conditions under which the system operates:

- Circuitry: TTL and STTL integrated circuits with liberal use of medium scale integration.
- Signal Levels:
  Active: Allowable high input 2.8 volts to 5.5 volts.
  Passive: Allowable low input -0.3 volt of 0.5 volt.
- Temperature: 0 to 50 degrees C ambient.
- Relative Humidity: 5 to 95 percent without condensation.

Figure 1-6 Operator Control Panel

1.5 PWA AND PROM IDENTIFICATION AND ORDERING GUIDE

Printed Wiring Assemblies (PWAs) and Programmable Read Only Memories (PROMs) used in this system are labeled with a code that identifies the item. This subsection provides the information necessary to use these codes.

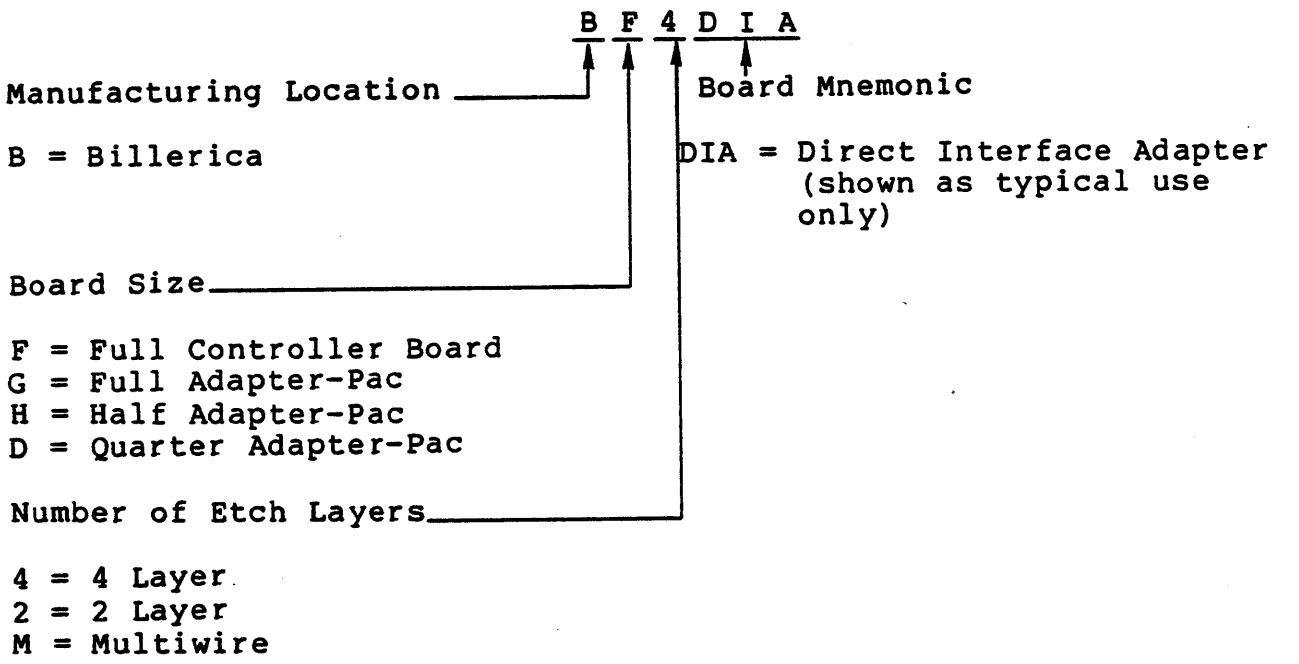
1.5.1 Board Identification

The boards used in this system are listed in Table 1-1. They are identified by the following:

- A 6-character board type identifier
- An 11-character Technical Identifier (TI)
- An 11-digit board assembly number.

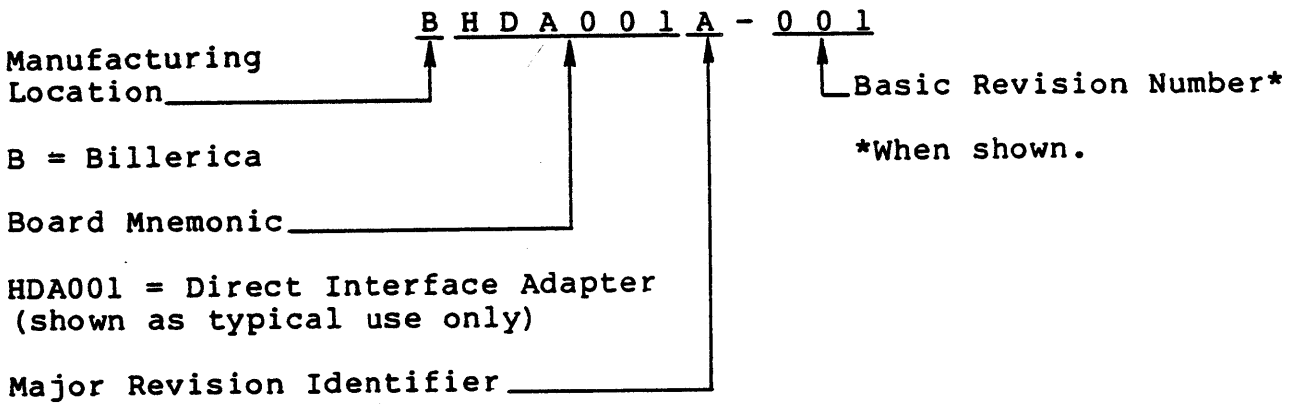
1.5.1.1 Six-Character Board Type Identifier

The board type is identified as follows:



1.5.1.2 Eleven-Character Technical Identifier

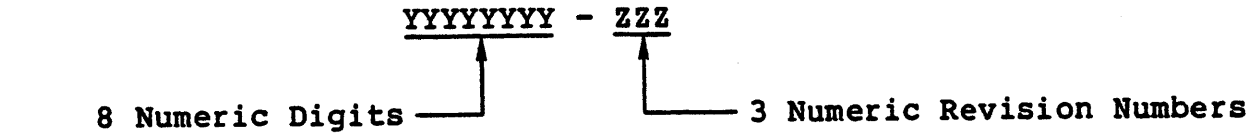
The 11-character Technical Identifier (TI) is used as follows:



The TI may also be referred to as the IPI (Internal Product Identifier) and is used when it is necessary to order a replacement board.

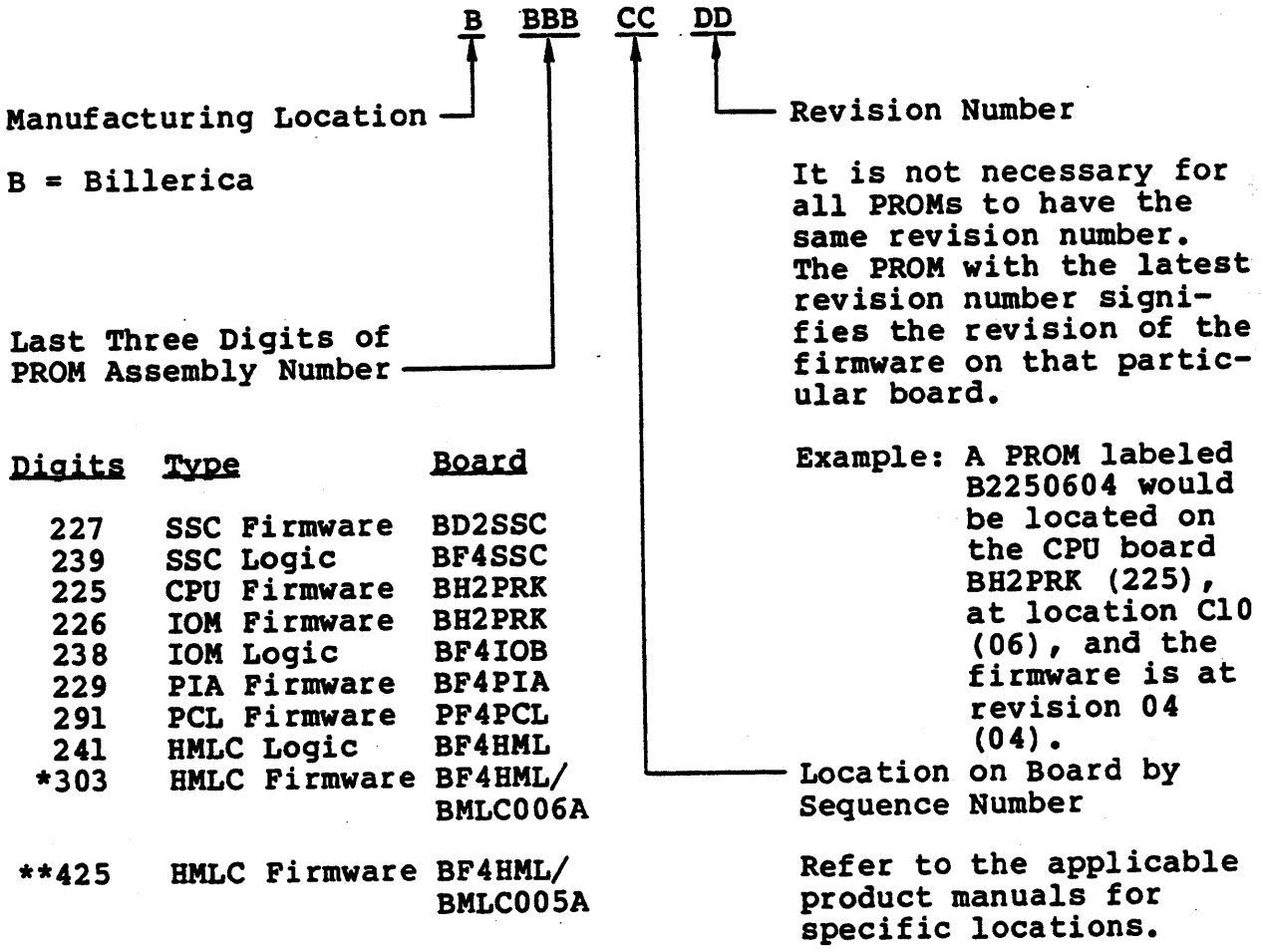
1.5.1.3 Eleven-Digit Board Assembly Number

The 11-digit board assembly number is different for each type of board and for every release of each board. Board releases are designated as 2.0, 2.1, etc., and correspond to assembly numbers, as shown in Table 1-1. The board assembly number is used as follows:



1.5.2 Programmable Read Only Memory Identification

PROM chips are used for logic functions and for firmware control. These PROMs are field replaceable items and are replaced in accordance with FCO updates. The 8-character type identification label on each PROM is used as follows:



Digits	Type	Board
227	SSC Firmware	BD2SSC
239	SSC Logic	BF4SSC
225	CPU Firmware	BH2PRK
226	IOM Firmware	BH2PRK
238	IOM Logic	BF4IOB
229	PIA Firmware	BF4PIA
291	PCL Firmware	PF4PCL
241	HMLC Logic	BF4HML
*303	HMLC Firmware	BF4HML/ BMLC006A
**425	HMLC Firmware	BF4HML/ BMLC005A

*Firmware 303 is for HMLC with HDLC capability.
**Firmware 425 is for HMLC with BSC and HDLC capabilities.

Table 1-1 System PWA Identification (Sheet 1 of 2)

ASSEMBLY	IPI NUMBER	BOARD TYPE NUMBER	ASSEMBLY NUMBER LEVEL 2.0	ASSEMBLY NUMBER LEVEL 2.1	ASSEMBLY NUMBER LEVEL 2.2	ASSEMBLY LEVEL NUMBER 2.3 & UP
Central Processor Unit	BCPA018A/B BCPB018A/B	BF418A BF418B	60127933 60127936	60130826 60130830	60133050 60133000	60133358 (2.3) 60139963 (2.3)
CPU PROM-PAC	BPRK001A	BH2PRK	60130285	60130806	60133198	—
Memory (Double Word Fetch)	BMMU021A	BF2MCE	—	60130766	60132544	—
Memory (Single Word Fetch)	BMMU011A	BF2MAE	—	60130768	60132550	—
Memory-Pac*	BCMM005A	BS2TC8 BD2T48	60130604 60127817	—	—	—
Cache Memory	BCHE001A	BF4CHE	60130665	—	—	—
Cache-Pac (4K)	BCHE04KA	BG4CHE	60130669	60135751	—	—
Memory Controller	BMMU031B	BF2MYE	60133096	60133341	60138544	—
Memory-Pac Memory DTR	BCMM048A	BS2SH8 BD2T48	60132666 60127818	60133233	—	—
Cache Controller	BCB15C1A	BF415C	—	60133289	60139507	—
Memory-Pac	BCMM038A	BS2TA8	60130603	—	—	—
System Support Channel	BSSC002A	BF4SSC	60130165	60130854	60133350	—
SSC PROM-PAC	BSSC001A	BD2SSC	60130161	60130697	—	—
SSC Console Adapter	BDCFCNSA	BD2CSL	60127819	60130145	—	60130513 (3.0)
SSC Diskette Adapter-Pac	BDCFDSKA	BH2FLD	60127867	—	—	60130678 (3.0)
Input/Output Multiplexer	BPDM002A	BF4IOA	60127939	60130790	60133054	60139238 (2.3) 60141412 (2.4)
	BPDM001B	BF4IOB	60127942	60130794	60133058	60139496 (2.3) 60141506 (2.4)
IOM PROM-PAC	BPRK002A	BH2PRK	60130285	60130806	60133198	—
Page Control Unit	BPAG001A	BF4PCL	—	60120626	60132953	60144610
PAT-PAC	BPAT001A	BD2PAT	60127948	60130979	60133370	—
PATN-PAC	BPAT002A	BD2PTN	60130168	60130355	—	—
Peripheral Interface Adapter	BHPA001A	BF4PIA BFMPIA	60130838 —	— 60132638	— 60133078	60138281 (2.3) —
PIA Interface-Pac	BHPA002A	BG4PID	60130842	60132966	60138856	—
Direct Interface Adapter	BHDA002A	BF4DIA	60130403	60130924	60135407	—
DIA Interface-Pac	BHDA001A	BG4DID	60130329	60130920	—	—
Channel Interface Base (DCF6607)**	BMLC005A BMLC006A	BF4HML	—	—	60132771	60133246 (2.3) 60135403 (2.4)
Channel Interface Base (DCF6609)	BMLC0B5A	BF4HML	60130343	60130779	—	—

*Board type BD2T48 (60127817) is interchangeable with BS2TC8.
**DCF6607 requires BMLC006A when shipped with the DCF6618 or DCF6621 options (special with 60143386 firmware).

Table 1-1 System PWA Identification (Sheet 2 of 2)

ASSEMBLY	IPI NUMBER	BOARD TYPE NUMBER	ASSEMBLY NUMBER LEVEL 2.0	ASSEMBLY NUMBER LEVEL 2.1	ASSEMBLY NUMBER LEVEL 2.2	ASSEMBLY LEVEL NUMBER 2.3 & UP
Dual Async Current Loop Adapter (DCF6610)	BMLFCLAA	BD2CLA	60130863	60132612	60135747	--
Dual Sync Line Adapter (DCF6611)	BMLF103A	BD2LAS	60127925	60130504	--	60133016 (3.0)
Dual Async Line Adapter (DCF6612)	BMLF101B	BD2ASC	60127918	60130510	--	60130798 (3.0) 60133012 (3.1)
Dual Autocall Line Adapter (DCF6613)	BMLFDACA	BD2DAC	60130567	60130987	--	--
MIL-STD-188C Sync Adapter (DCF6614)	BMLF188A	BD2188	60130413	60131019	--	--
MIL-STD-188C Async Adapter (DCF6615)	BMLFA88A	BD2A88	60132679	--	--	--
MIL-STD-188C Broadband Adapter (DCF6616)	BMLFB88B	BD2B88	60132869	60140115	--	--
MIL-STD-188C HDLC Adapter (DCF6617)	BMLFH88A	BD2H88	60133242	--	--	--
MIL-STD-188C Broadband Sync Adapter	BMLF616A	BD2B8D	60133490	--	--	--
HPIA-PSI Adapter	BHPA001A	BFMPIA	--	60132638	60133078	--
Control Panel Board	--	BX2CP7	60130198	60130741	60133406	--
HDLC MIL-STD-188C Adapter (DCF6628)	BMLFDL8A	BHMDL8	60140066	--	--	--
Dual Bisync Line Adapter (DCF6618)	BMLF61BA	BD2LAB	--	--	--	60138308 (3.0)
Sync Current Mode Adapter (DCF6619)	BMLF619A	BD2CMD	--	60133392	--	--
High Level Data Link (DCF6620)	BMLFDLCA	BD2DLC	60130591	60130991	60135477	--
Bisync Current Mode Adapter (DCF6621)	BMLF619A	BD2CMD	60133392	--	60133410	--
HDLC Broadband Current Mode Adapter (DCF6622)	BMLFDLDA	BH4DLD	60132712	60139327	--	--
HDLC Broadband Balanced Line Adapter (DCF6623)	BMLFDLEA	BH4DLE	60133111	60139428	--	--
Sync Balanced Line Adapter (DCF6627)	BMLF627A BMLFBLSB	BD2BLD* --	-- --	60133472 --	-- 60133442	-- --

*May be replaced by BMLFBLSB-001.

1.5.3 Guide to Locating Components on a Board

Locating a particular component on a board is made easier by following the letter and number system shown in Figures 1-7 and 1-8. The board area is divided into sections. For example, the location identified as K14 is the section where column K and row 14 intersect. The component that is mounted on a controller board at K14 is identified on Figure 1-7. The component mounted on an adapter board at D05 is identified on Figure 1-8. The other components mounted on a board can be located in a similar manner.

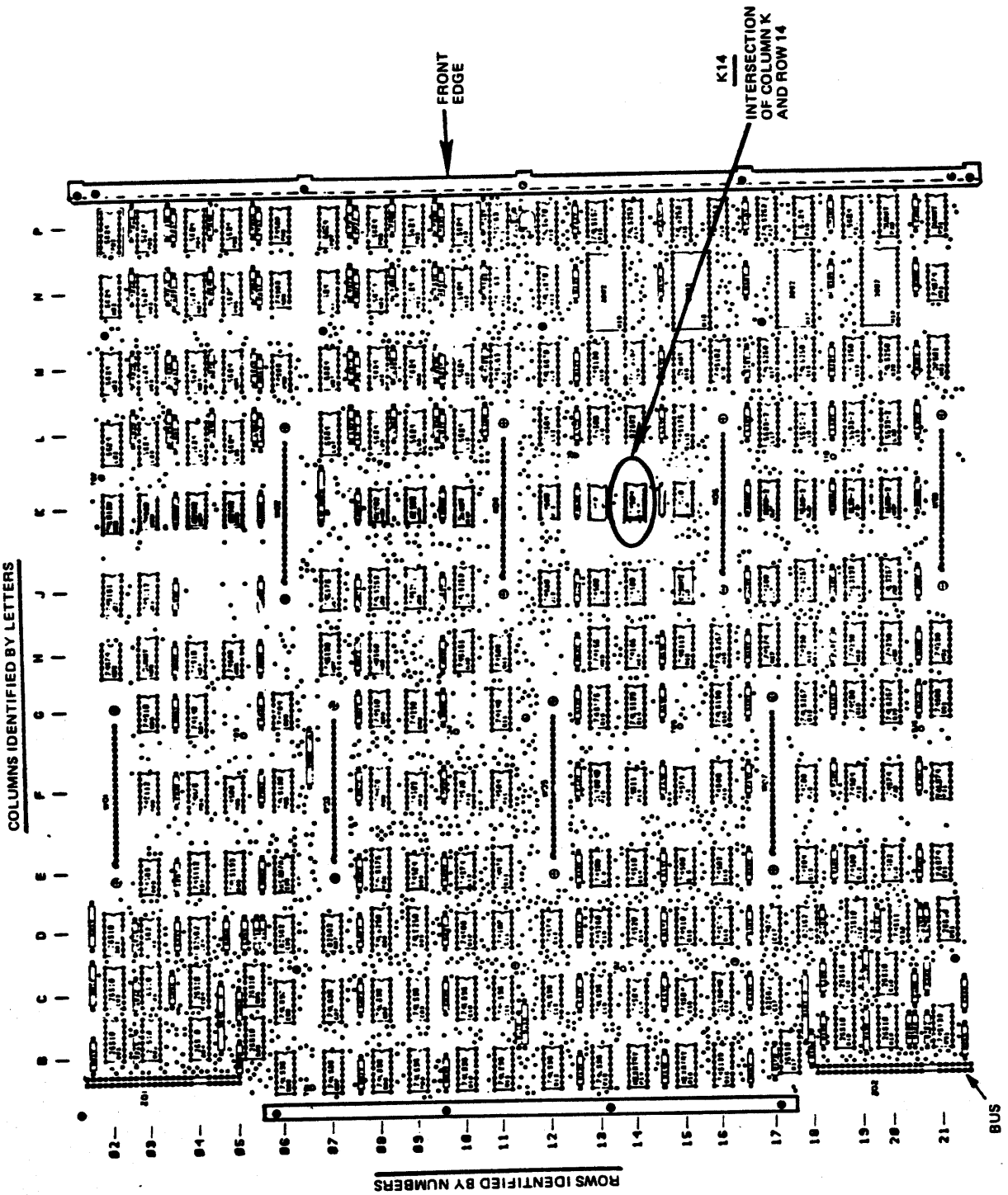


Figure 1-7 Typical Controller Board Component Layout

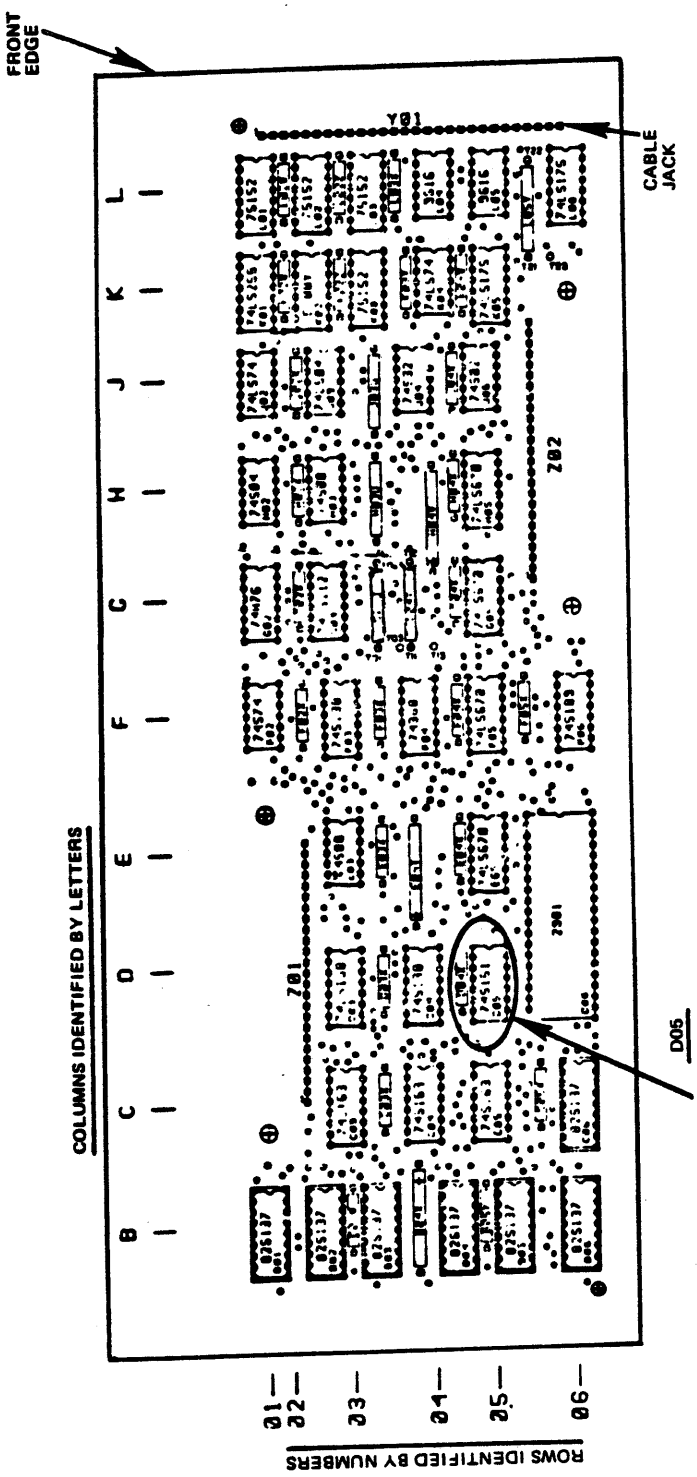


Figure 1-8 Typical Adapter Board Component Layout

FN01

II
SYSTEM DESCRIPTION

The DATANET system functions as a Front-End Network Processor (FNP) for the L66 computer and is available in several configurations. This section explains the basic operation of the system components and the relationship of the components to each other.

Features of the system include:

- Flexible Bus Structure
- Power Failure/Automatic Restart
- Error Detection and Correction Memory
- Processor Fault Sensing (Internal Interrupts)
- Program Interrupts (External Interrupts)
- Elapsed Time Clock
- Interval Timer.

This section also includes references to the software used with the system.

For further information on the individual components, refer to the manuals listed in subsection 1.2.

2.1 SYSTEM CONFIGURATION

2.1.1 Basic System Configuration

The basic system (see Figure 2-1) consists of:

- CPU and Operator Control Panel
- Memory
- Input/Output Multiplexer
- System Bus and I/O Bus
- System Support Channel
- Direct Interface Adapter.

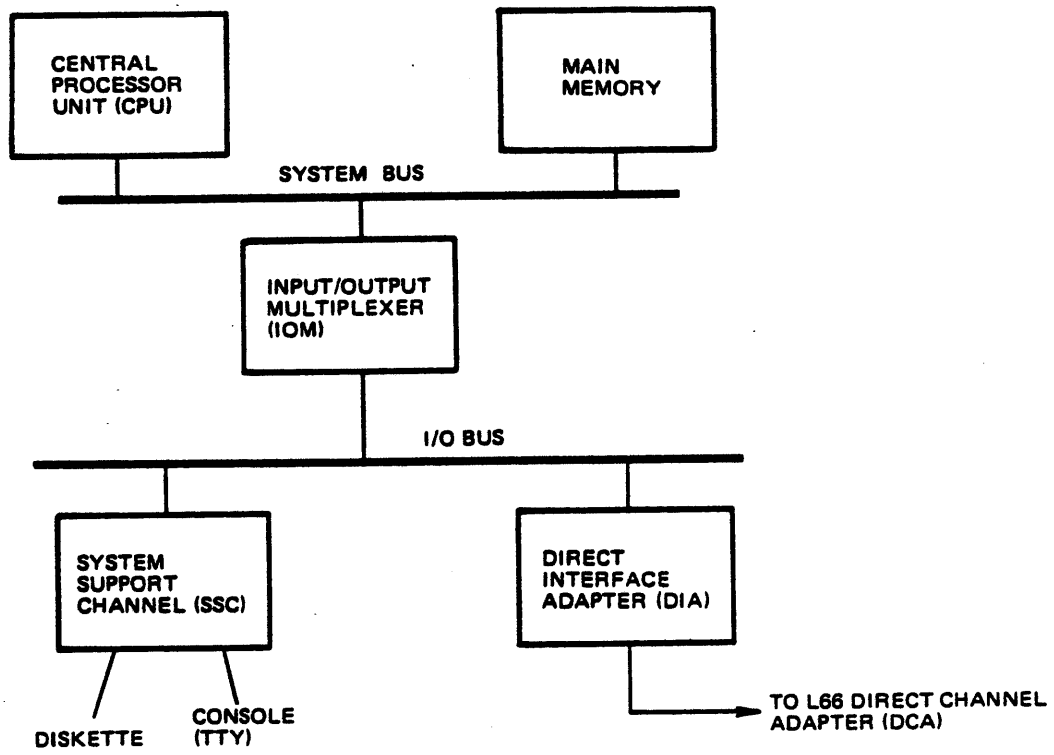


Figure 2-1 Basic System Block Diagram

2.1.1.1 Central Processor Unit

The Central Processor Unit (CPU) for the system is a processor that combines hardware and firmware, Read Only Store (ROS) memory, to execute the instruction set. The ROS memory consists of 2048 locations of microinstructions that perform the step-by-step tasks necessary to complete each software instruction. Each of the 2048 locations contains 40 bits of information, which are decoded to enable the necessary CPU operations for each software instruction.

The CPU hardware is centered about a parallel Arithmetic Logic Unit (ALU) and a Register File Unit (RFU) that contains most of the program-visible registers. The RFU and other hardware registers (some of which are program visible) have access to the ALU over lines that interface with that unit. The Bus Interface Unit (BIU) contains registers to interface with the system bus, and includes an optional Page Address Table Unit (PATU) and an optional interface to connect to the CPU cache.

Figure 2-2 is a block diagram of the CPU, illustrating the major areas within the CPU. For a detailed explanation of the CPU, refer to the system CPU manual (subsection 1.2 contains the manual order numbers).

2.1.1.2 Operator Control Panel

The system has a self-contained panel (see Figure 1-6). Two etched boards are mounted behind the panel. The control panel provides a means for initializing the system, starting/stopping the CPU, entering and displaying registers and memory, single stepping a program, booting a program, master clearing the system, and indicating the CPU routines. A ribbon cable connects the control panel to the CPU.

2.1.1.3 Memory

The system memory is a random access unit that is capable of performing all the storage functions without restrictions on address sequence, data patterns, or repetition rate. The memory is 24-bits wide, 18 data bits and 6 Error Detection and Correction (EDAC) bits, and is available as a fast double word fetch memory or a slow single word fetch memory. Memory can be addressed in a number of ways, as defined in the following:

- Banked or Single Word Pull: This is the normal memory addressing technique whereby locations are read sequentially through the memory Option-Pacs.

- Double Word Pull: The read cycle is maintained to allow reading of two consecutive memory locations at a time. In this memory addressing technique, the even numbered memory locations are on the Memory-Pac, while the odd numbered memory locations are on another Memory-Pac. Both Memory-Pacs must be on the same controller board. Information on the memory configuration and addressing is provided in subsection 3.5.3.3.

Additional features of the system memory are self-contained initialize and refresh logic.

Figure 2-3 is a block diagram of the memory. For a detailed description of the memory, refer to the memory manual (subsection 1.2 contains the manual order numbers).

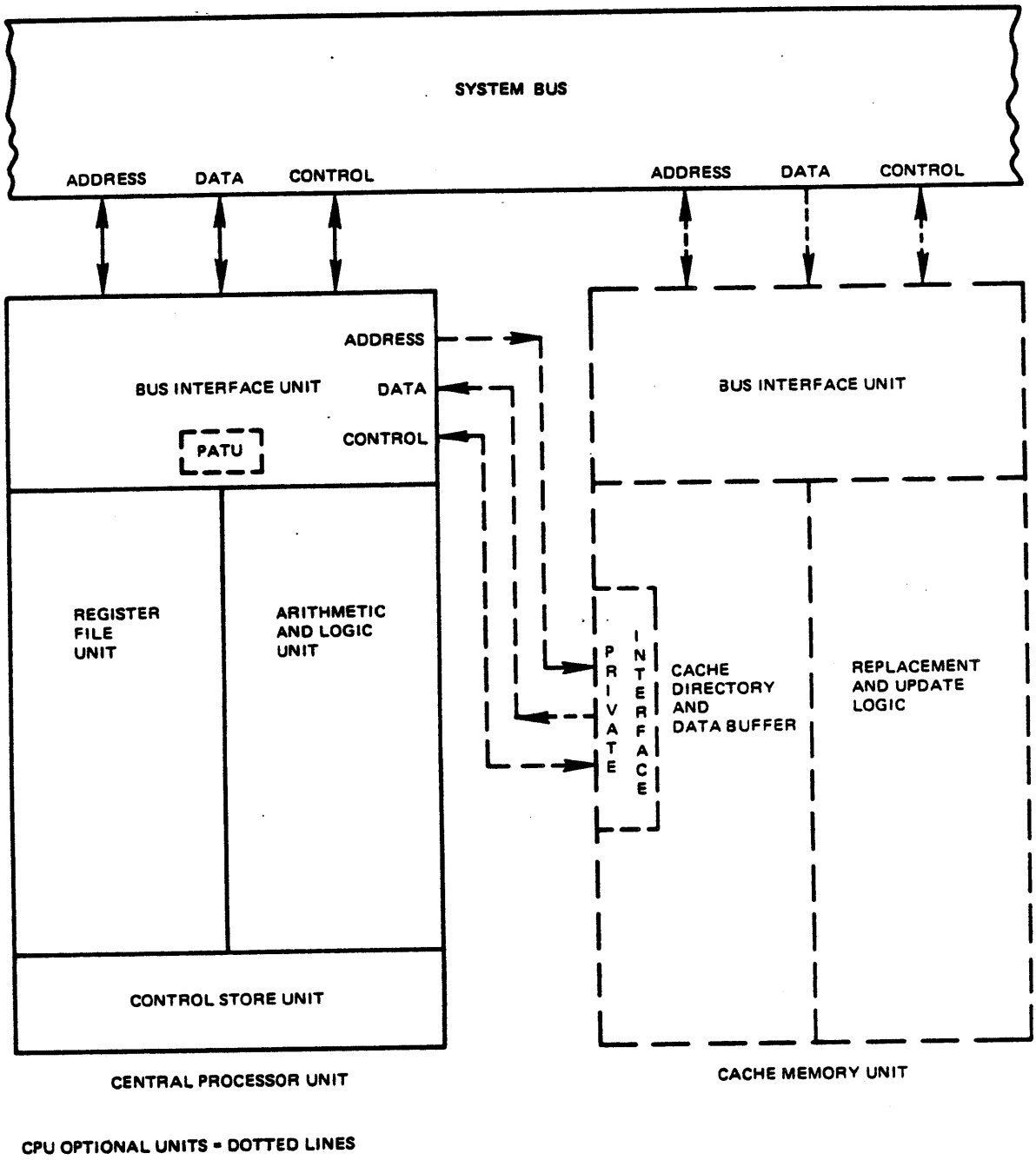


Figure 2-2 Central Processor Unit Block Diagram

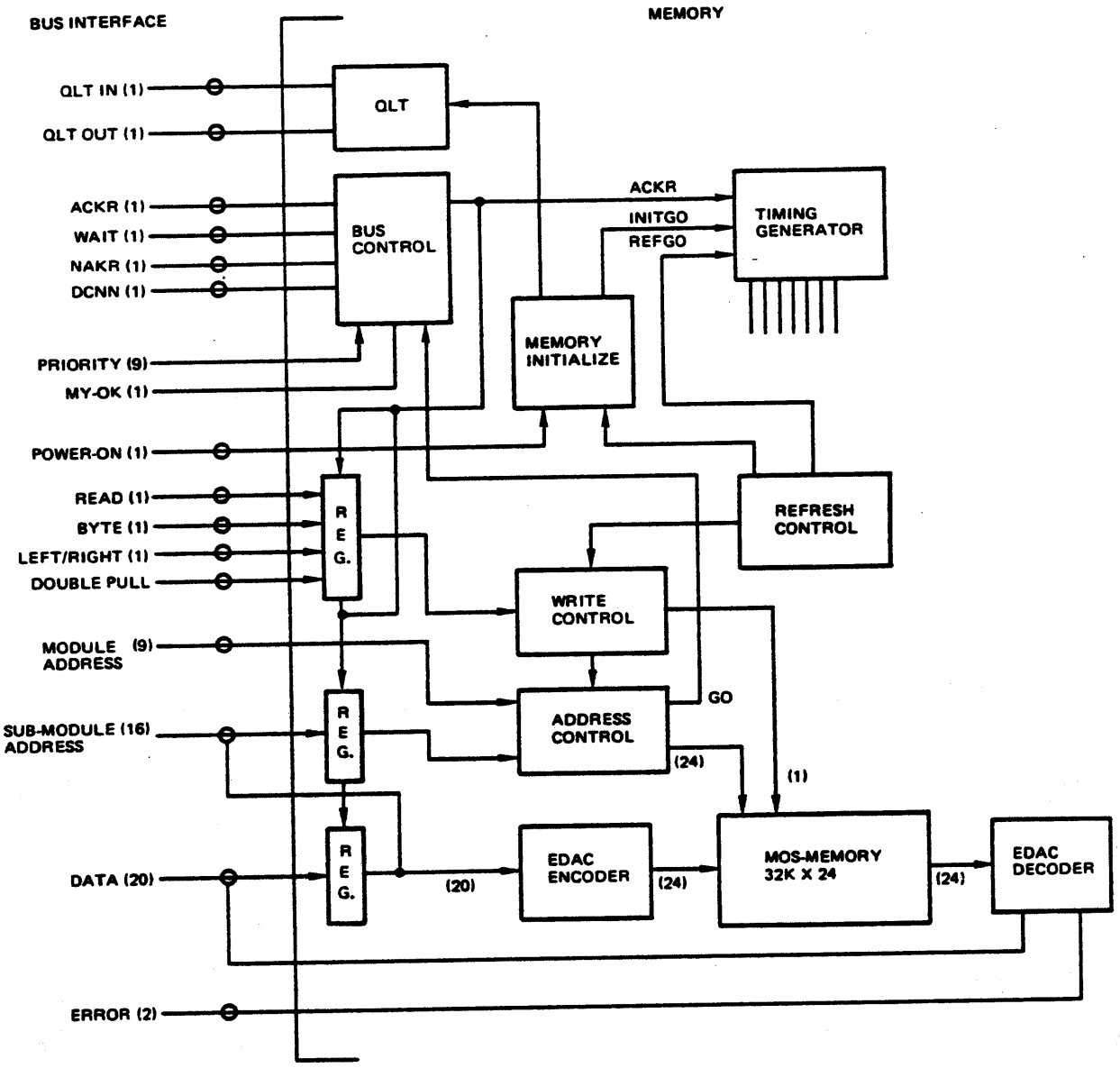


Figure 2-3 Main Memory Block Diagram

2.1.1.4 System and I/O Bus

An overview of the system and I/O bus is provided in subsection 2.2. Subsection 3.5.12 contains definitions of the interface signals.

2.1.1.5 Input/Output Multiplexer

The Input/Output Multiplexer (IOM) provides a path for data and control information between components attached to the system bus and the I/O controllers and their adapters on the I/O bus.

To facilitate these communications, the IOM:

- Provides compatibility with software I/O instructions by reformatting data for indirect data transfers
- Packs and unpacks various character or word sizes in memory on indirect data transfers
- Provides an Elapsed Time Clock (ETC) and an Interval Timer (IT)
- Manages interrupts (the primary method of communication between an I/O channel and a software program)
- Provides fault handling and reporting between components on different buses
- Supplies paged addresses for I/O controllers to be sent to the system page control logic unit, if installed
- Maintains a counter in memory locations 476 and 477 that indicates the number of corrected memory errors (EDAC).

The major components of the IOM (see Figure 2-4) operate asynchronously and are synchronized to each other through the internal bus.

The Input/Output Processor (IOP) controls the bus transfers and internal functions that are related to indirect data transfers and interrupt control instructions. Direct cycles to and from memory take place without activation of the IOP.

The IOP consists of a clock, a ROS unit, an ALU, and an RFU. The ROS unit provides storage for 1K of 36-bit wide functional microinstructions to determine the sequence that the IOP follows in response to bus activity that requires IOM intervention. The register file includes interrupt control registers that store indications of the level of interrupts that are pending for the CPU and the level of interrupts that are enabled.

Direct bus-to-bus transfers require only the use of the system bus interface, the I/O bus interface registers, the control logic, and the internal bus, permitting the IOM to accomodate direct transfers while the IOM IOP is busy. Direct bus cycle data flow is unidirectional, either I/O bus to system bus or system bus to I/O bus. I/O bus to system bus cycles are either memory write cycles or memory read request cycles; system bus to I/O bus cycles are second half memory read cycles that address a unit on the I/O bus.

All IOM operations other than direct transfers require the use of the IOM IOP. The IOP performs one operation at a time and waits for all bus cycles that require IOM IOP intervention until the current process runs to completion. IOP operations can be initiated by a bus cycle on the I/O bus, the system bus, or internal routines of the IOM. For a detailed description of the IOM, refer to the system IOM manual (subsection 1.2 contains the manual order numbers).

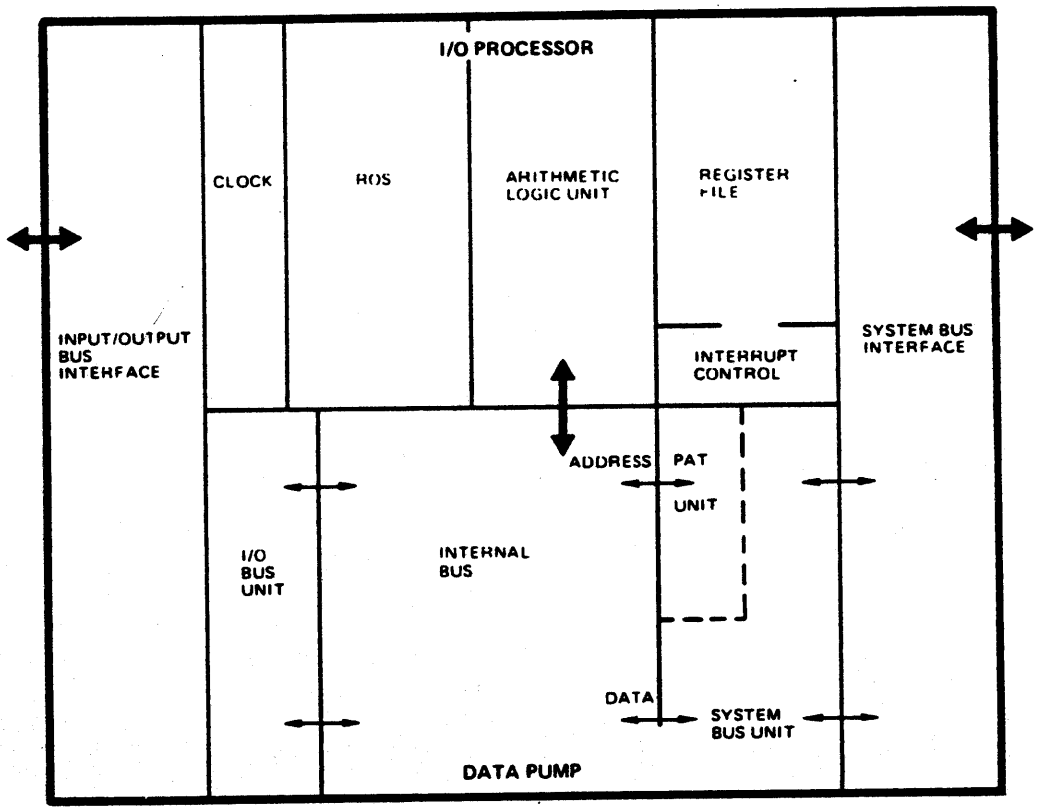


Figure 2-4 Input/Output Multiplexer

2.1.1.6 System Support Channel

The System Support Channel (SSC), along with configurable device adapters (Adapter-Pacs), is a peripheral controller, which attaches to the I/O bus. The SSC contains firmware and hardware common to the device adapters plus device-specific firmware. All the firmware associated with the SSC is located on a Control Store-Pac, which physically occupies one adapter position on the SSC board.

Information from the SSC is transferred to the adapters in byte form. The adapters supply information to the devices in bit serial form. The adapters assemble bit serial information from the devices into byte form for transfer to the SSC. The SSC provides control for the diskette that contains the offline T&Ds and for one of the following consoles:

- KSR-33 Teletype Console (DCF6608 Basic Console, used with GRTS)
- 120 CPS KBD Typewriter Console KSR (DCF6606 Heavy Duty Console, used with NPS).

Figure 2-5 is a major block diagram of the SSC. For a detailed description of the SSC, refer to the SSC manual (subsection 1.2 contains the manual order numbers).

2.1.1.7 Direct Interface Adapter

The system Direct Interface Adapter (DIA) provides a link between the IOM and the L66 IOM Direct Channel Adapter (DCA). Operations in the DIA are initiated by one of the following commands:

- Connect command from the system processor.
- Connect command from the L66 processor.

A Connect command from either the system or the L66 causes the DIA to:

- Transfer data from one system to the other
- Program interrupt either system
- Store status in the system.

Data is transferred between the DIA and the L66 DCA on a 36-bit bidirectional bus. The data transfer between the DIA and the IOM is in 18-bit or 36-bit direct transfer mode or 36-bit indirect transfer mode.

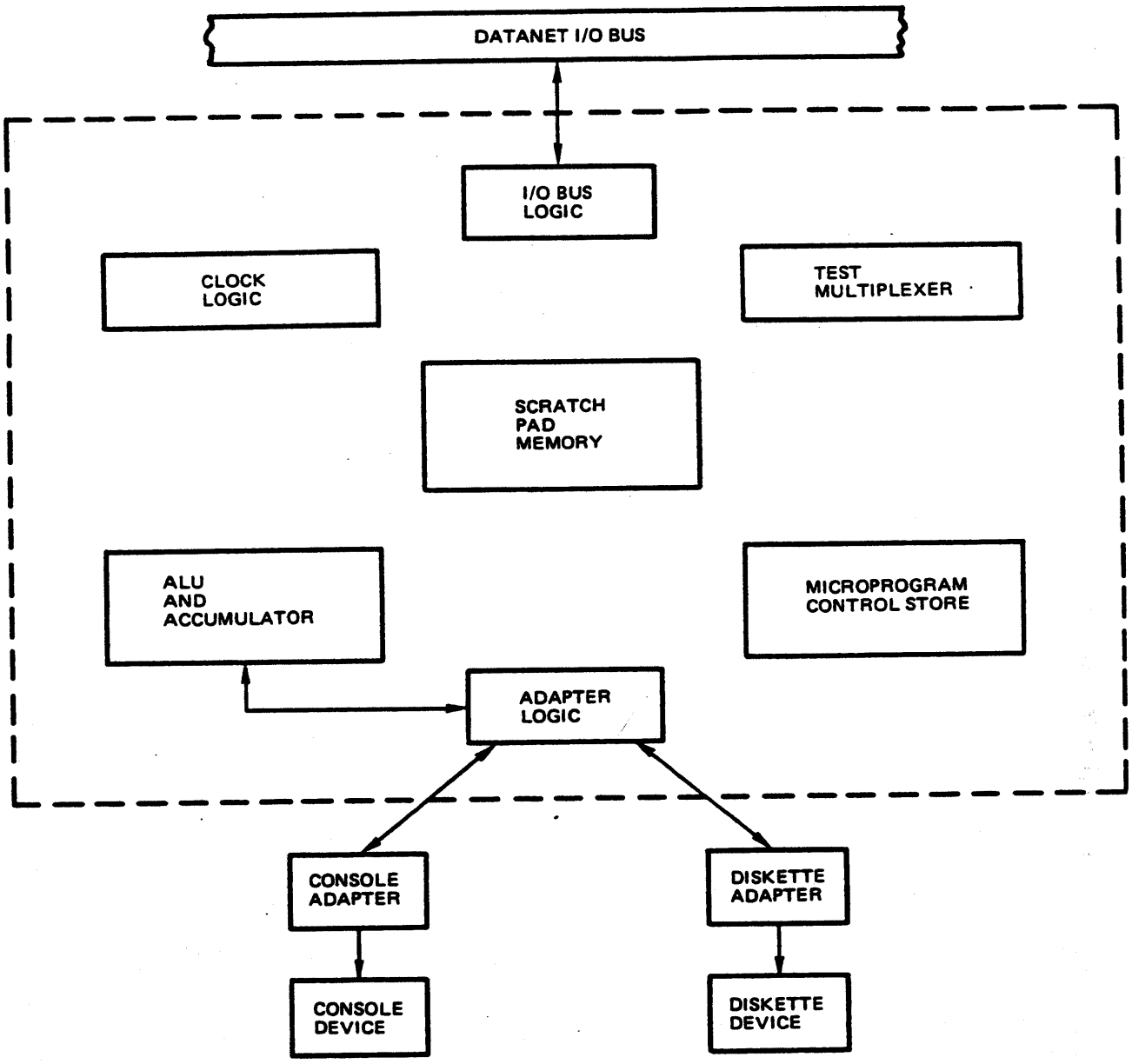


Figure 2-5 System Support Channel Major Block Diagram

The software in the system and the L66 central system determine the starting addresses for data transfers (blocks of data or single 36-bit words can be transferred). The DIA fetches these starting addresses from the system memory or the L66 memory; the DIA also fetches a count (tally) of the number of 36-bit words to be transferred. The DIA then transfers the data between the system and the L66 memories while controlling the addressing into each memory unit. The data transfer continues until all the data (as determined by the tally) is transferred from memory to memory.

Figure 2-6 is a block diagram of the DIA. For a more detailed description of the DIA, refer to the system DIA manual (subsection 1.2 contains the manual order numbers).

2.1.2 Expanded System Configurations

The expanded system consists of the basic components listed in subsection 2.1.1 and the following optional components, which are defined in the following subsections.

- Channel Interface Base
- Peripheral Interface Adapter
- Cache Memory
- Page Control Unit.

Figure 2-7 shows some possible expanded system configurations.

2.1.2.1 Channel Interface Base Controller

The system Channel Interface Base (CIB), or Honeywell Multiline Controller (HMLC), is a communications controller that interfaces with up to four Communication Line Adapters (CLAs), shown in Figure 2-8. The CIB contains the logic required to interface with the I/O bus of the system and to control up to eight communications lines by use of the appropriate CLAs (see Table 3-16). The CIB uses both hardware and firmware to perform its functions. All of the CIB hardware and firmware is housed on one board (BF4HML), which plugs into the I/O bus.

The CIB supports data transfer and data control for up to eight full duplex, low-speed (300 bits per second or less) and medium-speed (600 to 9600 bits per second) lines. The CIB accomodates high-speed lines as well, with reduced line connectability. Only one line up to 72KB full duplex may be attached per HMLC/CIB.

NOTE

The total maximum data transfer for all adapters attached to a CIB controller is 72KB full duplex or 144KB combined transmit and receive (see Table 3-16).

The CIB provides all the firmware and hardware that is common to all line adapters. Channel-specific logic is contained on interchangeable, pluggable line adapters and by firmware that is physically on the CIB board. Each CIA consists of either one-line or two-line interfaces, depending upon the complexity and circuit requirements of the particular CLA functions and the data set interface to be supported. Information is transmitted to/from the CLA and the CIB in parallel byte form. The CLA serializes byte information received from the CIB for transmission to the attached data set, and assembles serial data from the data set into byte form for transmission to the CIB.

Each line that operates with the CIB is a full duplex data path composed of two independently controlled channels either sending or receiving characters. The CIB uses indirect memory operations via Indirect Control Words (ICWs) to transfer characters between main memory and the communications lines.

The CIB is capable of handling both synchronous and asynchronous character-oriented messages. Character length may be five, six, seven, or eight bits for both synchronous or asynchronous messages. Appropriate software in the system allows the CIB to operate at various data transmission speeds with different:

- Bit Orders
- Bits per Character
- Information Codes
- Message Formats
- Data Communications Control Procedures.

The CIB is also capable of intermixing the various types of terminals and communications subsystems that can be connected to its communications lines.

There are two types of CIB controllers:

- Type DCF6609 Channel Interface Base Controller (BSC Version): Type DCF6609 accomodates all channel types except HDLC. (Refer to subsection 1.2 for manual order numbers.) This unit is obsolete and is replaced by the following type.

- Type DCF6607 Channel Interface Base Controller (Universal): Type DCF6607 accomodates all channel types and supports the switch-selected Direct Connect feature. (Refer to subsection 1.2 for manual order numbers.)

Table 3-16 lists the communications line adapters available with the CIB controller.

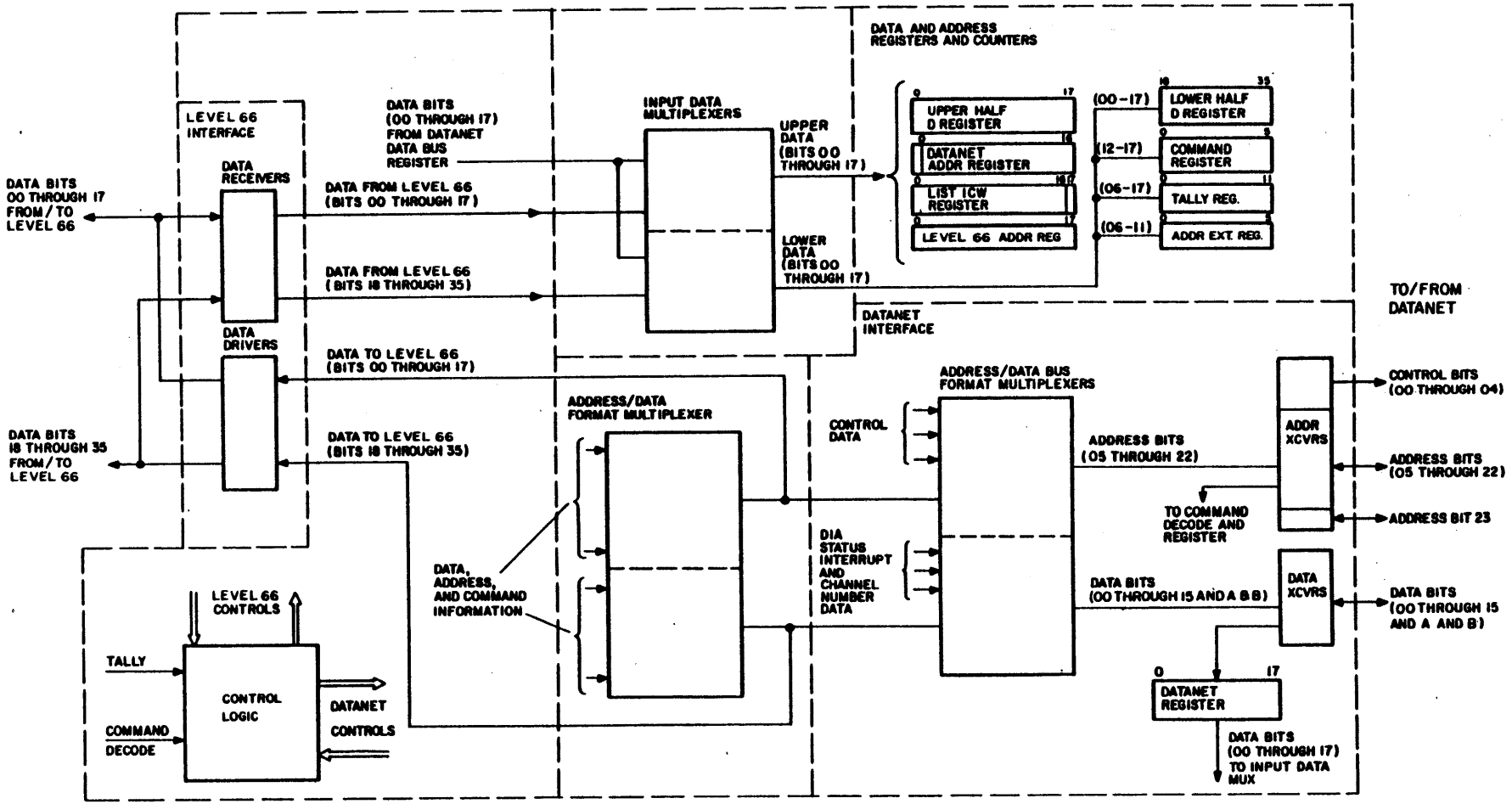


Figure 2-6 Direct Interface Adapter Major Block Diagram

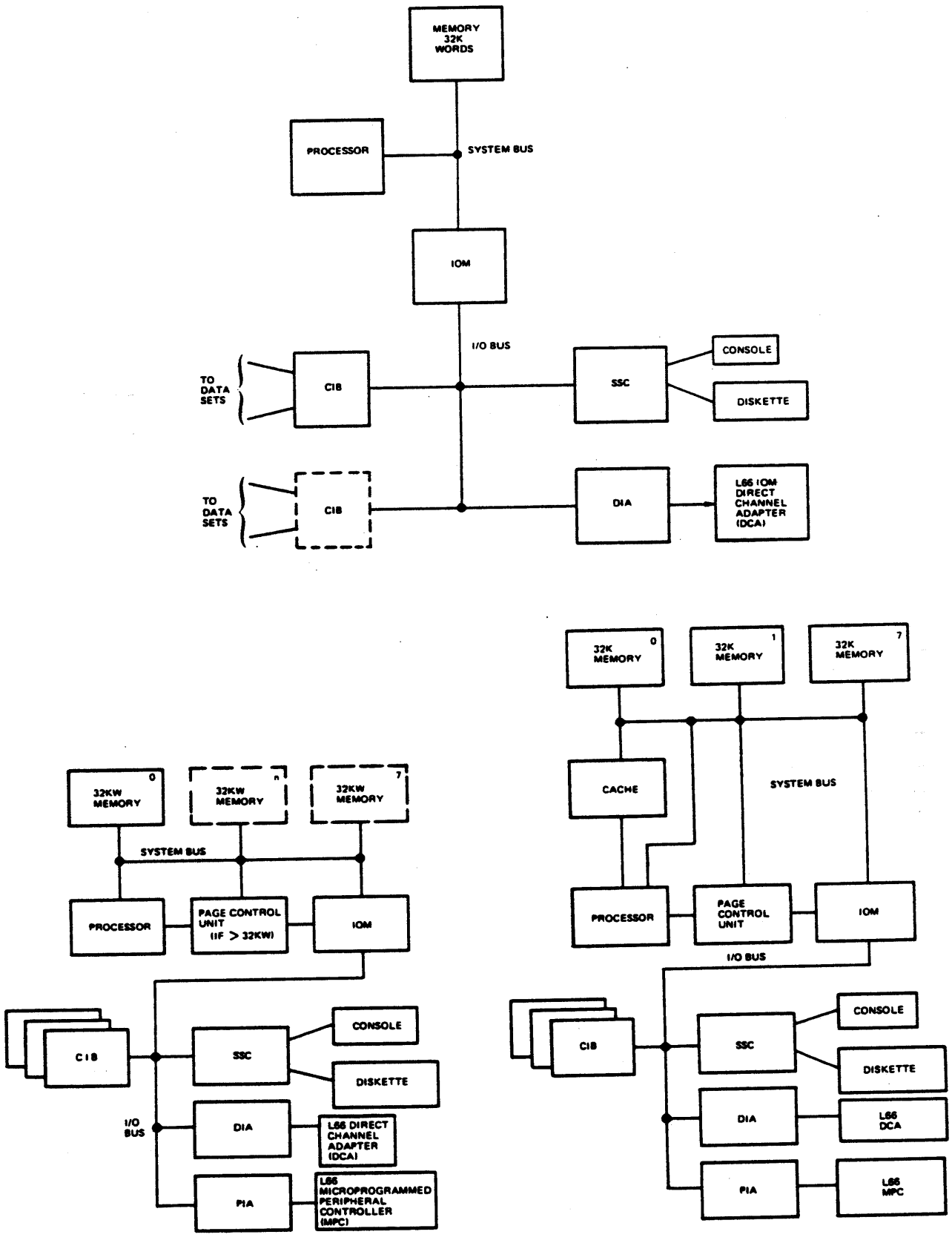
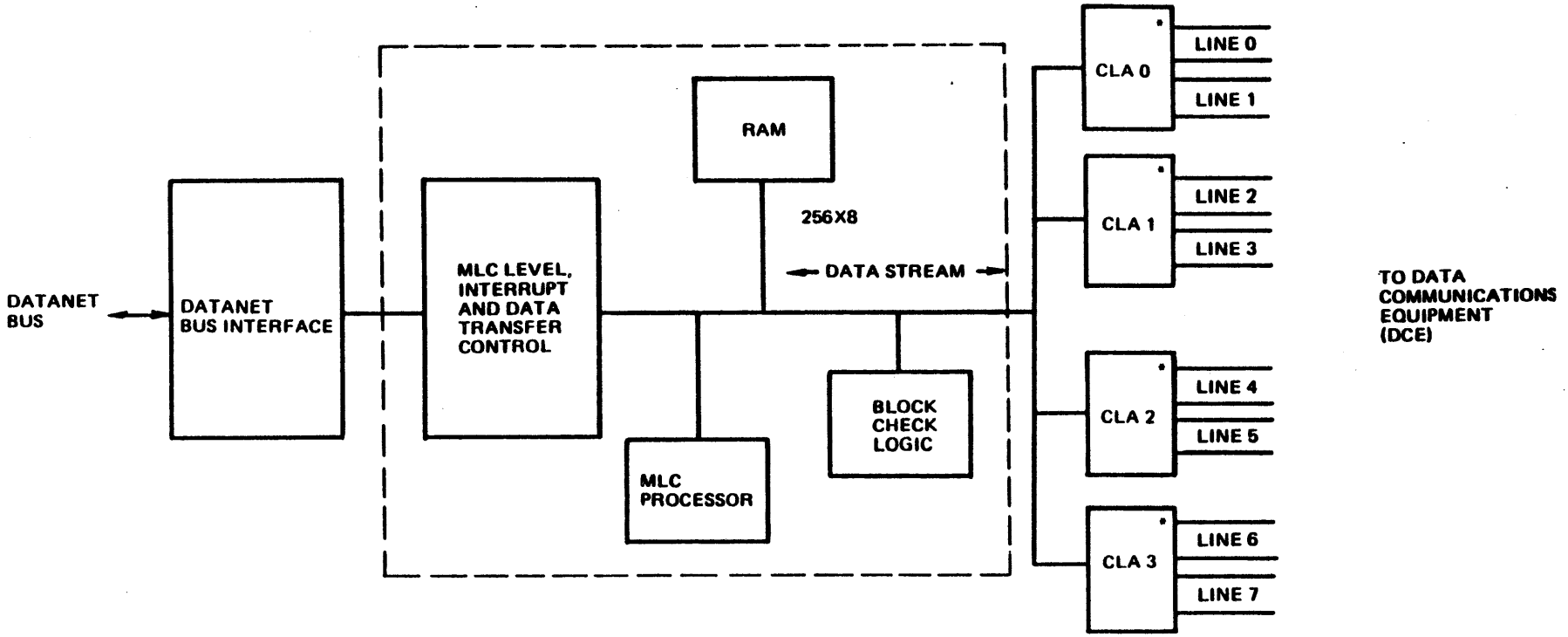


Figure 2-7 Expanded System Block Diagrams



*A CLA DESIGNED FOR HIGH LEVEL DATA LINK CONTROL (HDLC) PROCEDURES CAN INTERFACE WITH ONLY ONE LINE.

Figure 2-8 CIB Functional Block Diagram

2.1.2.2 Peripheral Interface Adapter

The system Peripheral Interface Adapter (PIA) provides the interface between the system IOM and the disk Microprogrammed Controller (MPC). A single PIA interfaces with one MPC (see Figure 2-9), which may control up to 16 disk packs.

Normal data transfer activities of the PIA are initiated by the system and are controlled by the MPC. The PIA basically responds only to the system Connect instruction. The Connect instruction causes the MPC to assume control for the data transfer to/from the disk. Data is transferred between the IOM and the PIA on the system I/O bus via direct 18-bit load/store cycles. Status is stored via the indirect 36-bit store cycle.

The overall data transaction is directed by the software in the system memory. The software sets up the mailbox region in memory and informs the PIA of the base address of that region. Then the software connects the PIA, instructing it to begin a specified routine on a specified logical channel, which is the access path to each virtual controller. Using the information provided with the Connect instruction, the PIA accesses the mailboxes necessary to initiate and complete the disk transaction.

The various microroutines are initiated by the MPC service codes. The exceptions are the Load External (LDEX) and Store External (STEX) commands, which are issued by the IOM. Each MPC service code initiates a specific routine that executes the service code function.

The PIA is a hard-fail device and is subject to transfer timing errors and aborts due to excessive transfer timing errors. For this reason, with the exception of the IOM, the PIA must have top priority on the system I/O bus.

NOTE

> The maximum data rate for PIA channels is 1 million bytes (8 bits) per second with the MPC, or 500K words (18-bits) per second in ASCII mode with the IOM.

Figure 2-10 shows the PIA major block diagram. For a more detailed description of the PIA, refer to the PIA manual (subsection 1.2 contains the manaul order numbers).

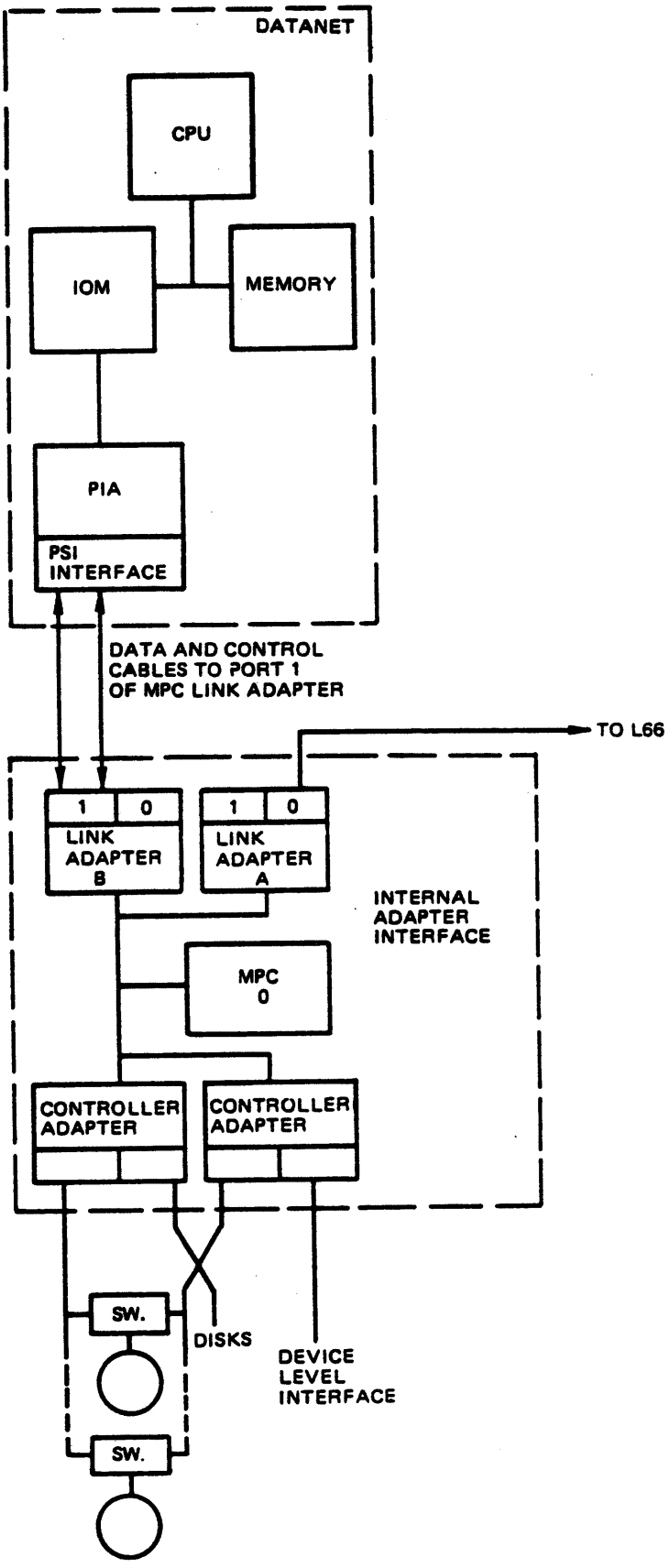


Figure 2-9 PIA/MPC Interface Block Diagram

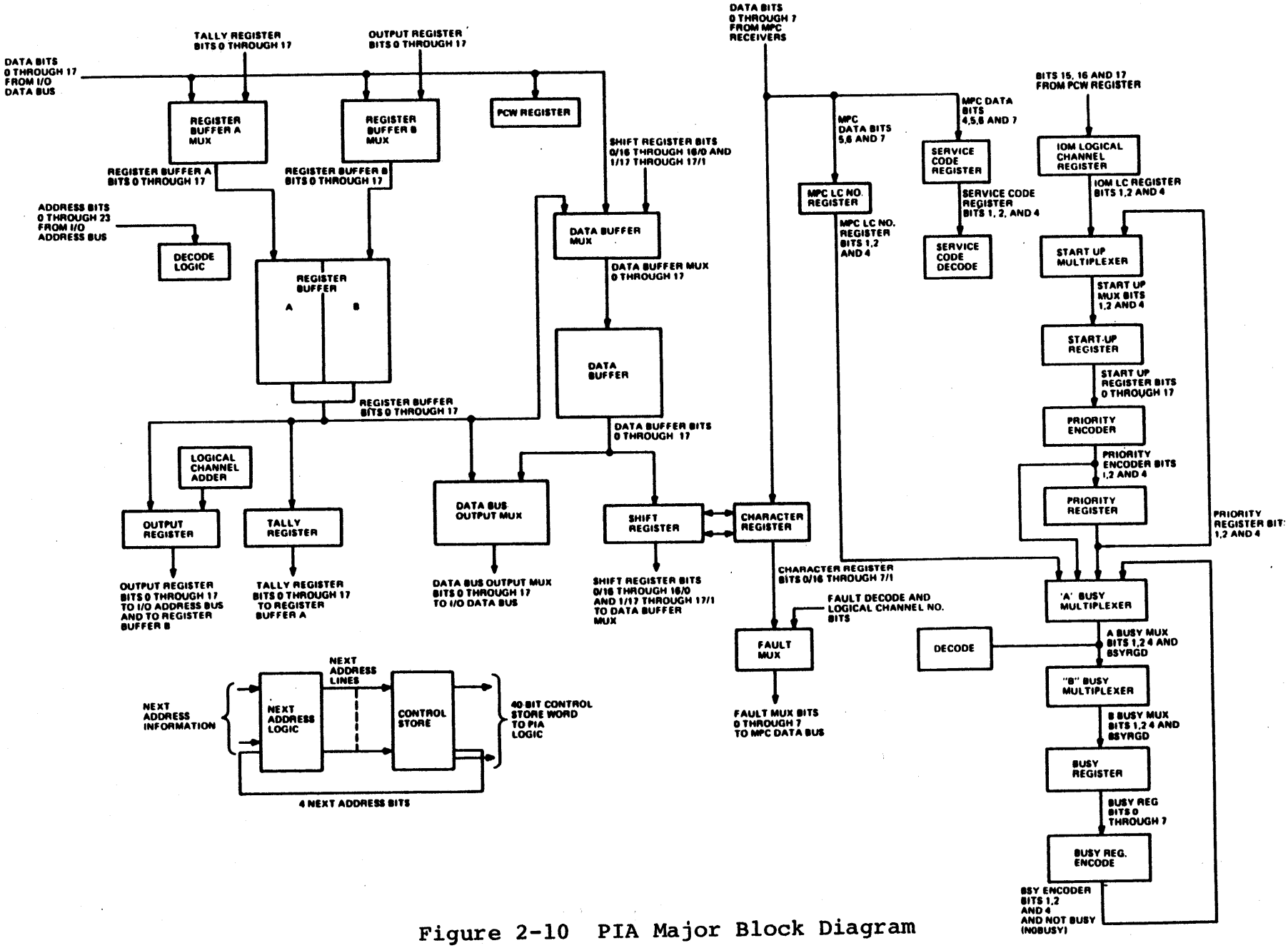


Figure 2-10 PIA Major Block Diagram

2.1.2.3 Cache Memory

Cache is defined as a secure temporary place of storage. The cache memory provides intermediate high-speed storage, which improves the performance of the CPU by decreasing the time required to receive (i.e., fetch) instructions and data from memory. This decrease in time is achieved both by anticipatory main memory reads and storage of previously used data and instructions for future repetitions of the currently executing program.

The cache memory contains copies of selected (recently referenced) memory locations. It has a system bus interface that allows it to make memory read references on behalf of the CPU and to monitor the system bus, copying main memory write data if it currently contains a copy of the location addressed. The cache memory also has a private interface that allows it to communicate with the CPU to which it is dedicated. It receives memory read requests across this interface, thereby becoming committed to locate the data for the CPU in its local cache array or in main memory. In either case, the requested data is delivered to the CPU for processing.

Figure 2-11 is the major block diagram for the cache memory (also see Figure 2-2). The major blocks on Figure 2-11 are:

- Cache Directory and Data Buffer Unit: This unit provides the associated logic required to determine whether the requested main memory word is present or not present in the cache directory and data buffer unit; i.e., Random Access Memory (RAM).

- Replacement and Update Logic Unit: This unit provides the hardware necessary to access main memory and to perform a monitor function. The monitor function checks and evaluates all main memory write references (i.e., from the CPU or the IOM) and replaces data in any currently active cache memory location with the data from the system bus.

- Bus Interface Unit: This unit connects the cache memory unit to the system bus, enabling the cache memory unit to access main memory and read out required CPU information.

- Private Cache/CPU Interface Unit: This unit connects the cache memory unit to the CPU, allowing main memory requests, addresses, and data to be communicated between the CPU and the cache memory unit.

For more detailed information, refer to cache memory manual (subsection 1.2 contains the manual order numbers).

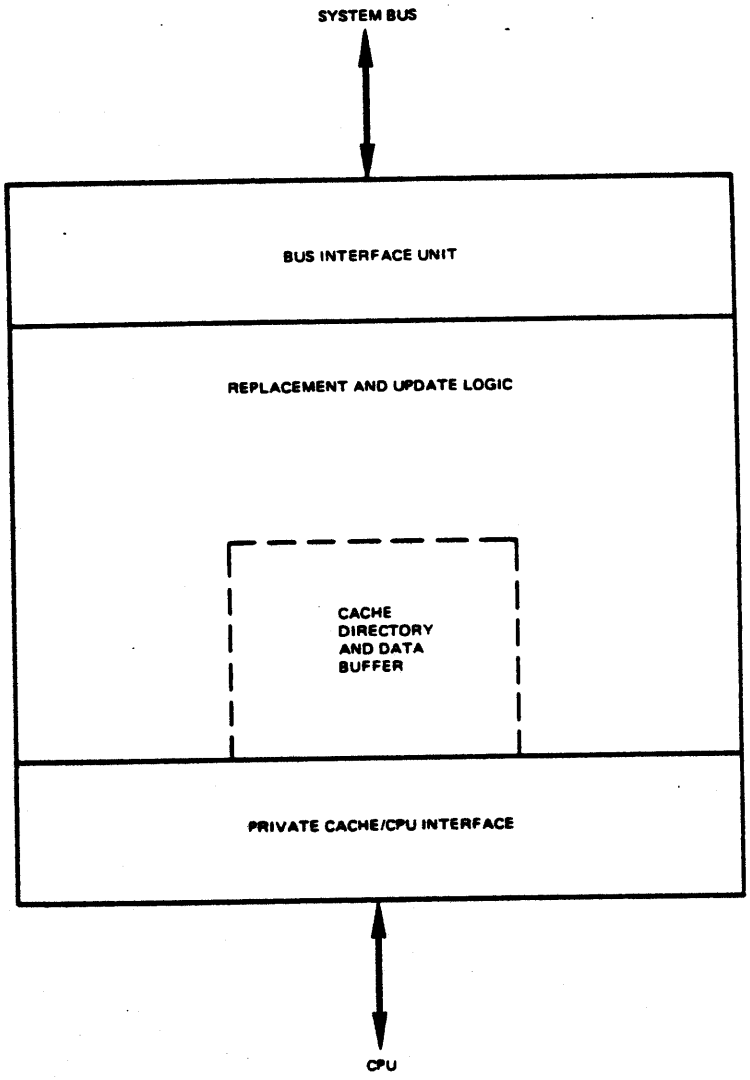


Figure 2-11 Cache Memory Major Logic Units

2.1.2.4 Page Control Unit (Pager)

The page control unit option enhances the system by providing a mechanism for memory protection and for accessing up to 256K of optional memory. It is required on all systems that are configured with more than 32K of memory. This option uses software-generated page address tables to expand a 15-bit (i.e., 32K) memory address into an 18-bit (i.e., 256K) absolute address (see Figure 2-12).

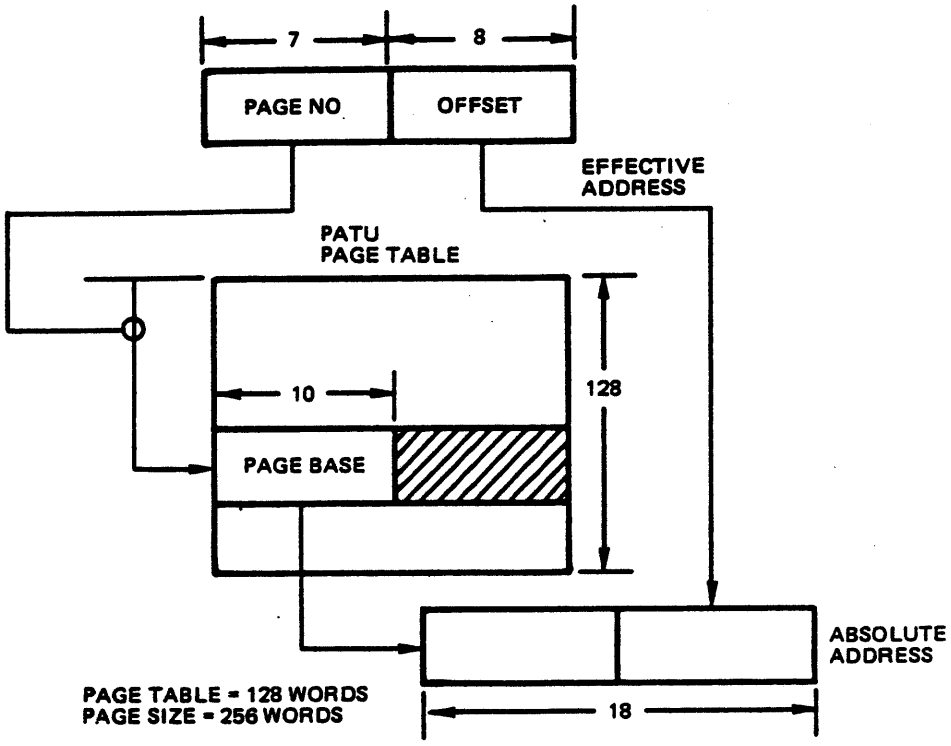


Figure 2-12 Page Address Expansion

The page control unit option consists of:

- Page Control Logic Unit: The Page Control Logic Unit (PCLU) is a full size, plug-in controller board on the system bus. It contains the logic that is required to constantly monitor the system bus for any changes to paging areas in main memory and to update the hardware Page Address Table Units (PATUs), when required.

- Page Address Table Unit: The Page Address Table Unit (PATU) is a 1/4-size Adapter-Pac. One PATU board attaches to the IOM board. The PATU stores copies of page tables that are associated with its processor. The PATU's primary purpose is to convert a virtual address supplied by its processor (i.e., CPU/IOM) into an absolute memory address. It also performs access right checks on the generated address.

Figure 2-13 shows the page control unit block diagram. For more detailed information, refer to the page control unit option manual (subsection 1.2 contains the manual order numbers).

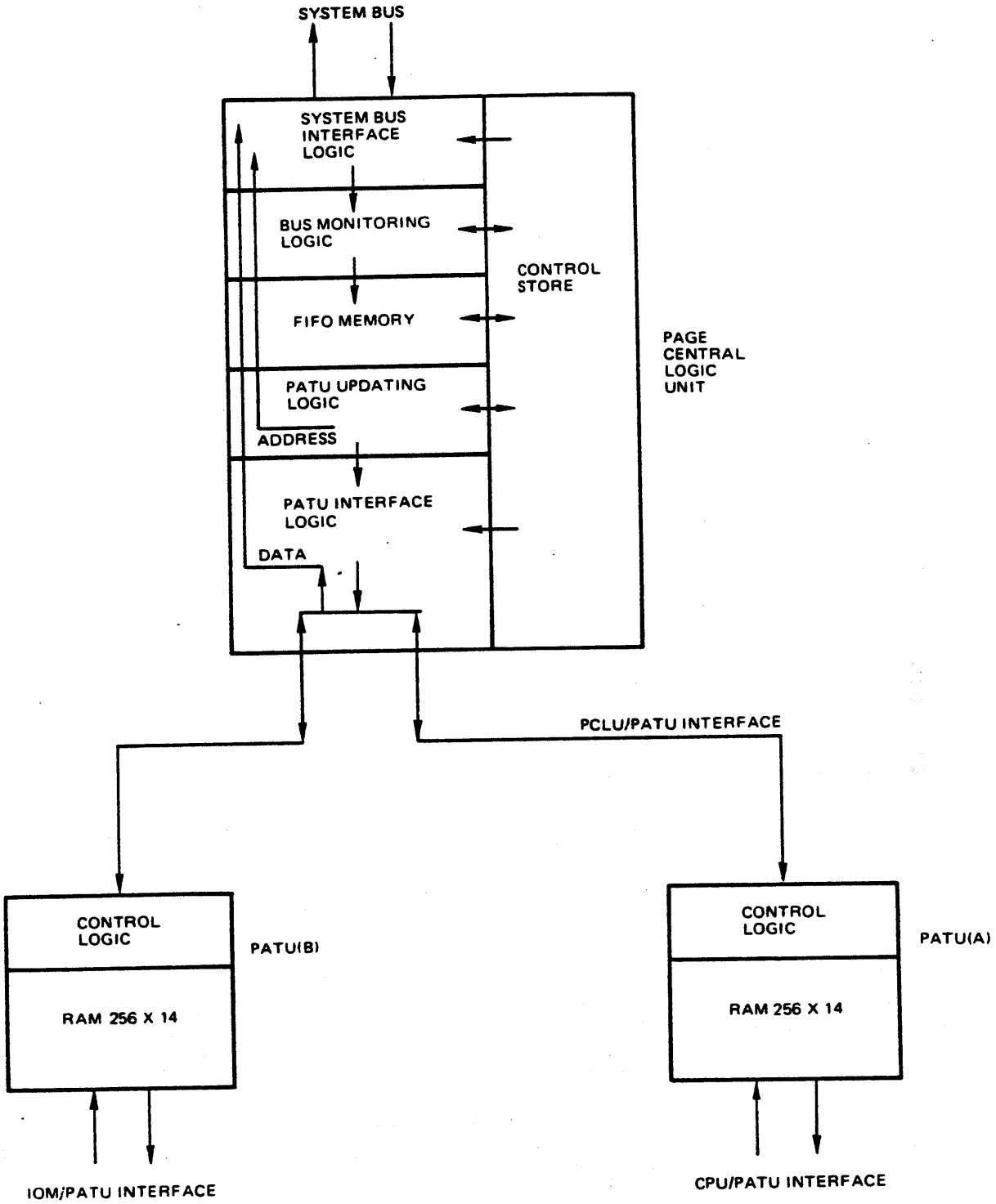


Figure 2-13 Page Control Unit Block Diagram

2.2 BUS FUNCTIONALITY

The bus provides a common communications path between units of the system. The bus is divided into the system bus and I/O bus. The system bus and the I/O bus are logically the same except that the system bus allows communications between the CPU, memory, and the IOM, while the I/O bus allows communications between the IOM and units beyond the IOM. For the sake of convenience, the system bus and the I/O bus are further subdivided into the address bus and the data bus, depending on whether reference is being made to the lines that carry the address and command information or the lines that carry data.

The bus is asynchronous in design, permitting units of varying speeds to operate efficiently on the same system. The design of the bus permits the following types of communications:

- Memory Transfers
- I/O Command Transfers
- Interrupts.

The granting of time on the bus is done on a priority basis. If two components on the bus simultaneously request time, the one with the highest priority is granted the time. The priority is established relative to the rate at which the components transfer and/or receive data. (Refer to subsection 3.5.2 for the rules applicable to the controller/processor board to chassis relationships.)

The transfer of information between units forms a master/slave relationship (i.e., the unit requesting and receiving access to the bus becomes the master unit; the unit being addressed by the master unit becomes the slave unit). If the communication requires a response, the responding slave unit assumes the role of master and the requesting unit (previous master) becomes the slave unit in a separate bus cycle.

All information transfers are from master to slave and each transfer is referred to as a bus cycle. This cycle is the period of time in which the requester (master) asks for use of the bus. If no other unit of a higher priority is making a bus cycle request, use of the bus is granted to the requester (master unit). The master unit then transmits this information to the slave unit and the slave unit acknowledges the communication.

Communication between a master unit and a slave unit requires an acknowledgment of the bus cycle from the slave unit when the slave unit is requested to transfer data (e.g., a memory read command). It this case, the request for information requires one bus cycle and the transmission of information back to the requester requires an additional bus cycle to complete the task.

2.3 SYSTEM SOFTWARE

Three software systems are available:

- General Remote Terminal Supervisor (GRTS I): GRTS I is an extension of the General Comprehensive Operating Supervisor (GCOS), which permits a variety of remote terminal devices, remote computer terminals, keyboard/display terminals, teleprinter terminals and others to communicate with the central system via this system. For more detailed information, refer to the Remote Terminal Supervisor Manual (subsection 1.2 contains the manual order numbers).

- General Remote Terminal Supervisor (GRTS II): GRTS II is an expanded software system with a maximum memory capacity of 64K words. For more detailed information, refer to the GRT II Startup Procedures Manual (subsection 1.2 contains the manual order numbers).

- Network Processing Supervisor (NPS): NPS is a software system developed to control the data communications sphere of an information network. It operates in the system and interfaces dynamically with the central system General Comprehensive Operating Supervisor (GCOS).

NOTE

To run under NPS, the PIA option must be installed; also required are CIB Type DCF6607 (if using HDLC devices) and Console Type DCF6606.

For more detailed information, refer to the Network Processing Supervisor Manual (subsection 1.2 contains the manual order numbers).

III
INSTALLATION

This section of the DATANET 66 manual provides the installation procedures for the system. It covers the initial installation along with procedures for expanding a system that has already been installed. System checkout procedures are also included.

NOTE

The installation procedures are based on the fact that all physical and electrical cable connections within the system cabinet were made at the factory prior to shipment of the equipment.

Site preparation information may be found in the Level 66 Site Preparation Manual (subsection 1.2 of this manual contains the manual order numbers).

3.1 EQUIPMENT ARRIVAL

When the equipment is delivered to the site, perform the following procedure:

1. Compare and check off all equipment and boxes with those listed on the shipping manifest.

2. Remove the shipping covers from the equipment and note any damaged or missing items before signing the shipping manifest.

3. Ensure that the documentation package includes a copy of FN01, FX23, and AY34. Check the manual titles with those listed on the Documentation Bill of Materials.

4. Check the system configuration against the locator card listing. The locator card is placed in the bottom of each chassis.

NOTE

T&D diskettes, the Level 66 IOM to DIA cables, and the ground cable are shipped from LISD in Phoenix.

3.2 EQUIPMENT PLACEMENT

To position the equipment, perform the following procedure:

1. Position the system cabinet (BRCK183A) in place (refer to the Level 66 Site Preparation Manual). Lower the leveling feet into position to hold the cabinet in place. (Leave sufficient space to allow access to the sides of the cabinet to install the system cables. A minimum of 3 feet is sufficient.)

2. Place a level on top of the cabinet. Using a 3/4-inch open-end wrench, adjust the leveling feet so that the cabinet is level (see Figure 3-1).

3. Install the KSR-33 console in accordance with subsection 3.5.9.6. The distance between the system cabinet and the KSR-33 console is limited by the length of the interconnecting cable. The two cabinets must be placed so that the 30-foot cable reaches the KSR-33 console with sufficient length available for routing into the cabinet and up to the console.

4. Swing open the top system cabinet dress panel by turning the captive screw at the middle left-hand side of the panel half a turn.

5. Remove the vertical and horizontal retaining bars and store them for future shipment.

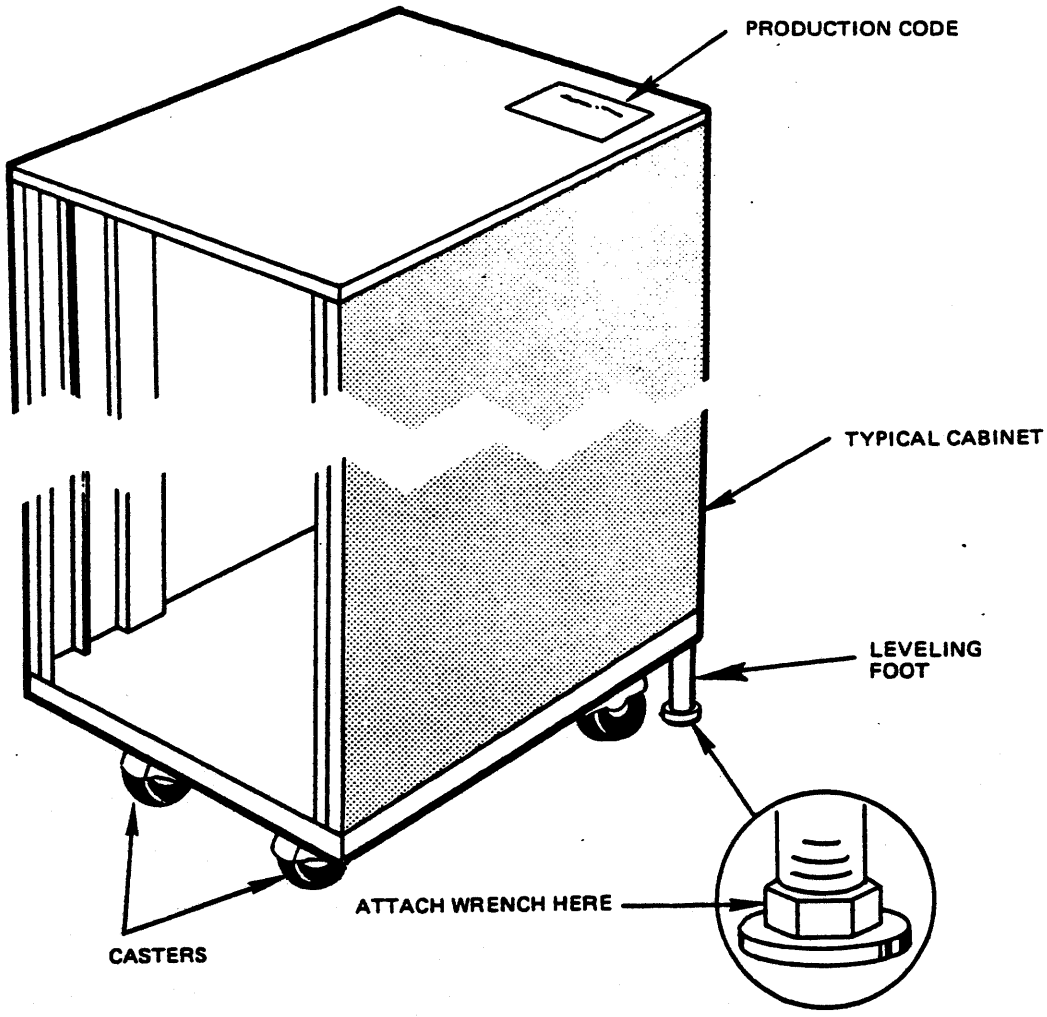


Figure 3-1 System Cabinet -- Adjustment of Leveling Feet

3.2.1 Cabinet and Control Panel Keys

The keys that unlock the rear door on the cabinet and the lock on the control panel are taped to the inside of the top dress panel.

3.2.2 Using the Computer Configuration Sheet

The Computer Configuration Sheet (CCS), a multipage document shipped with each system, provides:

- A list of the equipment ordered with the system
- Pertinent notes concerning the installation of the system
- An illustration of the layout of the mainframe cabinet
- A locator card that provides the locations of the controller and adapter boards within the system chassis
- Adapter-to-bulkhead locations for the internal cables
- Software channel assignments.

The size of the system configuration determines the number of sheets that make up the CCS. Figure 3-1.1 provides an example of how to use the CCS.

3.2.2a Code Clip Kit

If the system is shipped with a code clip kit, write the desired code on a paddle board label and on a code clip. Insert the code clip in a controller-board stiffener at the appropriate adapter-board position (Figure 3-22 provides an illustration). Repeat this procedure for each cable. Use code clip labels to identify the controller-board types by attaching a code clip at the left end of the board stiffener.

WARNING

To avoid bodily injury, set the POWER switch on the control panel to OFF before removing or installing a board. Ensure that the DC ON indicator on the control panel is extinguished. Set the PDU circuit breaker to OFF. Disconnect the ac power cable.

H O N E Y W E L L

COMPUTER CONFIGURATION SHEET

Technical Conf.-LAWRENCE

Model Type	Customer Name	Rev.
DN 66		A

System number	Configured by	Date
DZ7325-01	SEXTON	09/21/81

CABINET LAYOUT

1.75" F.P.
5.25" F.P.
1.75" F.P.
CAB013 *
1.75" F.P.
PNL010 CAB015
5.25" F.P.
7.0" F.P.
DSKT03
PDU063

ORDER TYPE
[X] System [ ] Exp.
[ ] Other

ITEM	TYPE NO.	QTY	REV
1	DNX0021	1	
2	DNX0022	1	
3	DNX0011	4	
4	DCF6612	8	
5	DCF6611	8	
6	DCF6606	1	

NOTES: SHEET 1 OF 2

1. Frequency 60 HZ [X] 50 Hz [ ] Volts

HOW MANY CAB013 EXPAN. CHASSIS FOR DN66	1
HOW MANY POWER SUPPLIES IN DN66 SYSTEM	3
HOW MANY POWER SUPPLIES IN MEM. EXPANSION	0

2. *1 POWER SUPPLY REQUIRED

VARIABLES

FW 42 10/16/81

DN 66 LOCATOR CARD SYSTEM NUMBER DZ7325-01

SHEET 2 OF 2 REV. A

SLOT NO / TERM	MEGABUS BOARD	[HEX ADDR]	TRAY CONFIGURATION 4	3	2	1
19						
18						
17						
16						
15						
14						
13	BX2RT3					
12	MLC005		MLF101	MLF101	MLF103	MLF103
11	MLC005		MLF107	MLF107	MLF103	MLF103
10	MLC005		MLF101	MLF101	MLF103	MLF103
9	MLC005		MLF101	MLF101	MLF103	MLF103
8	SSC002		DCPDSK DSKT03	DCPDSK	DCPCNS DCF6606	SSC001
7	HDA002					HDA001
6	PDM002					PRK002
5	PDM001					PAT002
4	CPA018					PAT002
3	CPB018					PRK003
2	MMU031					CMM048
TERM						
1	BX2RT4					

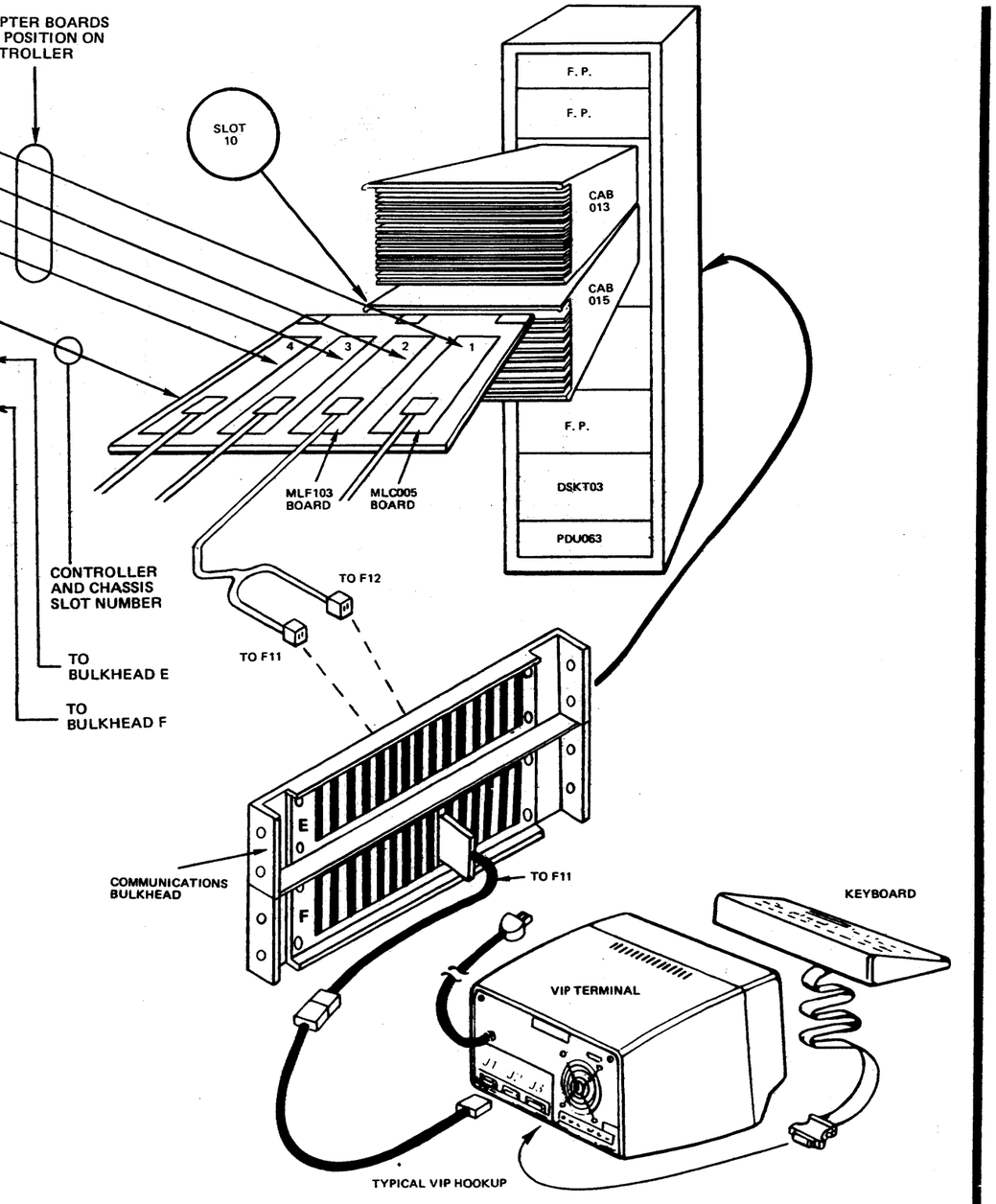


Figure 3-1.1 Using the Computer Configuration Sheet

3.2.3 Expansion (Bulkhead) Cabinet Attachment

This subsection contains the information necessary to attach an expansion (bulkhead) cabinet (BRCK012A) to the basic cabinet (BRCK183A). The use of the expansion cabinet is necessary if over 64 communications lines are to be used in the system. The expansion cabinet is used only to contain the connector bulkheads. No devices are installed in the expansion cabinet.

1. Refer to Figure 3-3 and position the basic and the expansion cabinets together.

2. Locate the 6 threaded tie rods, 12 nuts, 12 flat washers, and 12 lock washers (Table 3-1, items 3, 4, 5, and 6). This hardware is furnished with the expansion cabinet. Using this hardware, bolt the two cabinets together as shown.

NOTE

It may be necessary to remove temporarily some devices in the basic cabinet to gain access to the tie-rod mounting areas. If you cannot get at all of the tie rods, two (but no fewer than two) can be used.

3. Remove the fixing screw and washer (see Figure 3-3) from the cable door on the rear of the expansion cabinet. This hardware is used only to secure the cable door closed during shipment. Discard this hardware after removal.

4. Refer to Figures 3-3 and 3-4. The flat braid jumper (Table 3-1, item 7) must be connected between ground terminal E02 in the basic cabinet and ground terminal E01 in the expansion cabinet. The mounting hardware to be used is installed on the terminals. Ensure that the terminals are clean and that the mounting hardware is tightened.

NOTE

Although TB01 may be installed in the expansion cabinet, no connections have to be made to it.

5. Remove the lowest bulkhead from the shipping cage (see Figure 3-3) by removing the four bulkhead mounting screws (03010221-001). Carefully position the bulkhead on the lowest pair of bulkhead mounting brackets in the expansion cabinet, and secure it in place with the four mounting screws.

6. Repeat step 5 for the remaining bulkheads. Do not remove the shipping cage from the basic cabinet.

7. To install the connectors to the bulkheads, proceed as follows:

   a. Refer to the bulkhead locator card on the CSS (see Figure 3-1.1) and connect the connectors as shown. The locator card will be filled out prior to shipment of the system to indicate the location of subchannels 0 through 95. The number of the bulkhead location will be entered on the card in the appropriate location. An X marked on the card indicates that the communications cable used for that particular subchannel is not connected to the bulkhead; it connects directly from the CLA on the CIB. A # marked on the card denotes an unused channel.

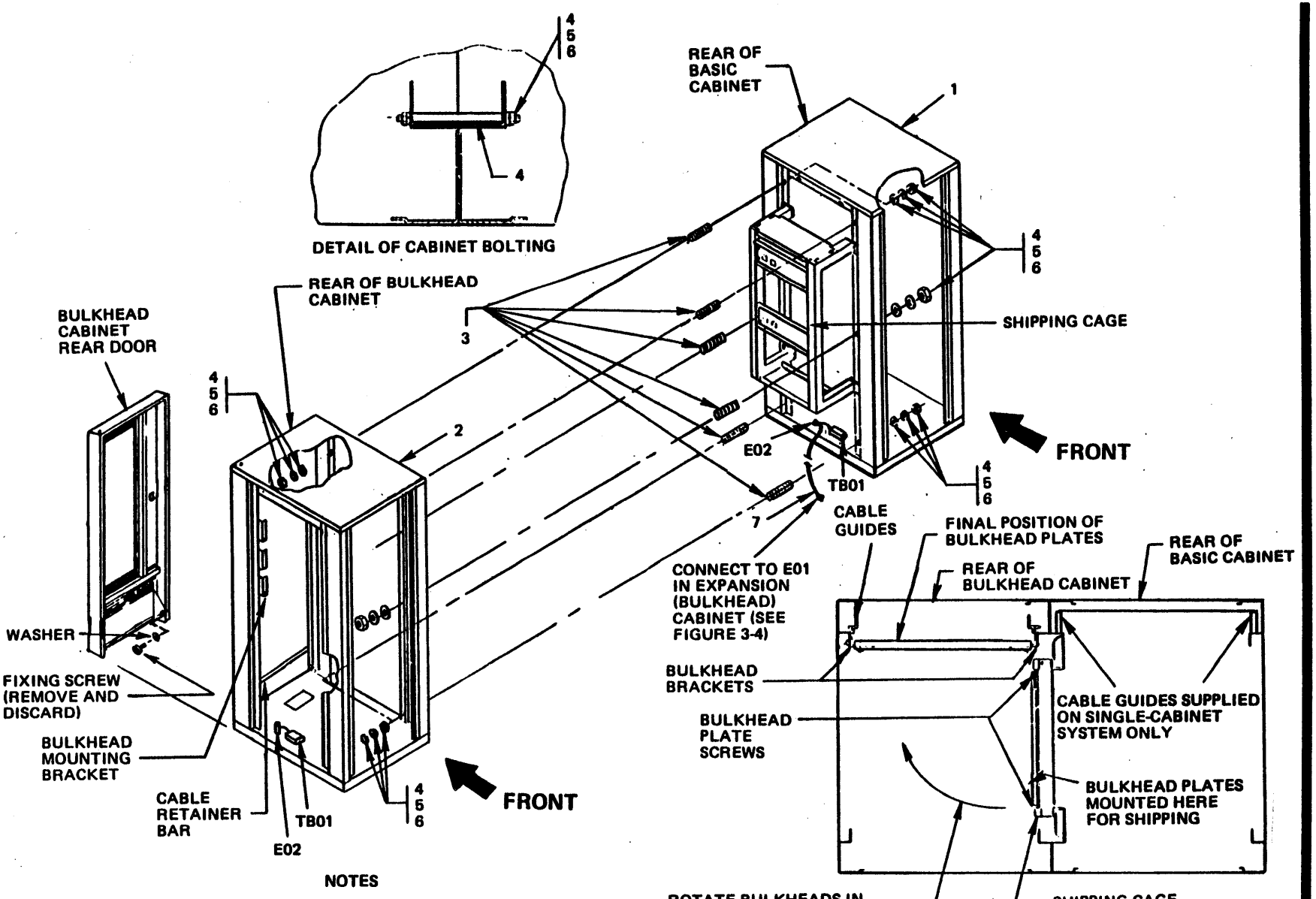
   b. Refer to Figure 3-6 for a typical connector to bulkhead attachment. Any mounting hardware that is not already installed is furnished as part of the bulkhead installation kit (60140740-006).

8. Connect any required external cables to the bulkheads in accordance with the cable locator card. Tighten the two mounting screws on the connectors. Table 3-16 lists the cables that may be used in the system. Dress the external cables around the cable guides, down the cabinet side posts, and between the cable retainer brackets near the bottom of the expansion cabinet. Install the cable retainer bar.

9. To attach an expansion cabinet to the opposite side of the basic cabinet, repeat steps 1 through 8. Note that the same hardware is used to attach the expansion cabinet to either side of the basic cabinet.

Table 3-1 Expansion (Bulkhead) Cabinet Installation Parts List (Refer to Figure 3-3)

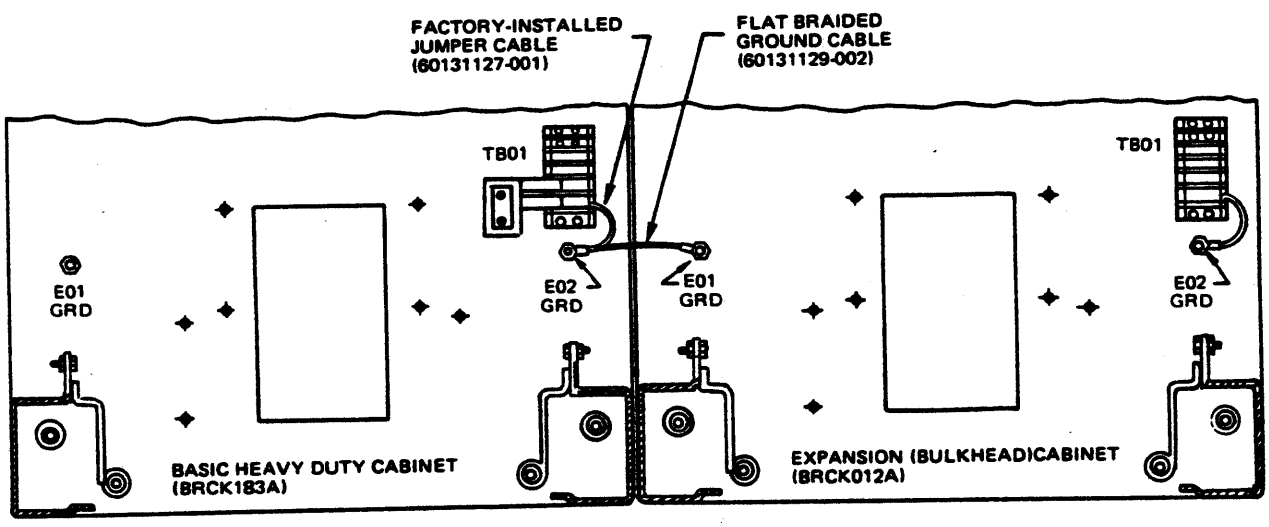
ITEM NUMBER	PART NUMBER	DESCRIPTION	QUANTITY
1	60135935-001	Basic Heavy Duty Cabinet, BRCK183A	1
2	60140760-001	Expansion (Bulkhead) Cabinet, BRCK012A	1
3	60135762-001	Tie Rod	6
4	03030001-012	Nut, Plain, Hex, 3/8	12
5	03020003-009	Lock Washer, HL-SPR, 3/8	12
6	03020045-008	Washer, Flat, 3/8	12
7	60131129-002	Jumper Assy, Flat Braid	1



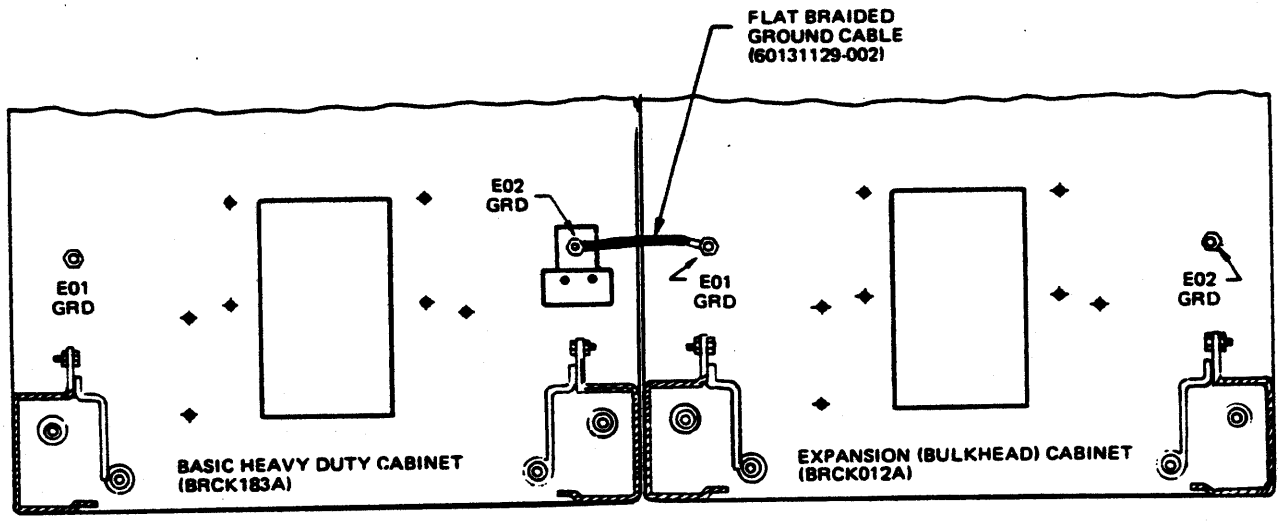
NOTES

1. BE SURE TO BOLT THE TWO CABINETS TOGETHER AT THE REAR LOCATIONS. ALSO BOLT AT FRONT WHEN POSSIBLE.
2. ON NON-BULKHEAD SYSTEMS, THERE IS NO BULKHEAD PLATE.

Figure 3-3 Expansion (Bulkhead) Cabinet Attachment



CABINETS WITH TB01



CABINETS WITHOUT TB01

Figure 3-4. System Grounding

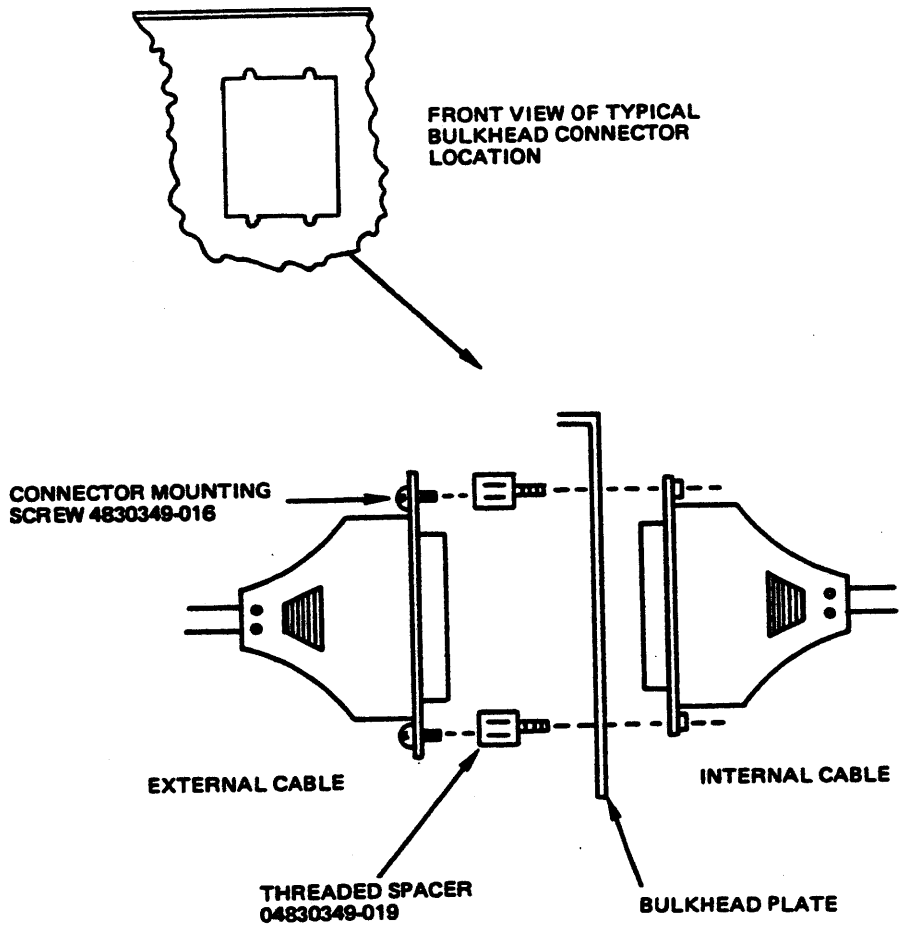


Figure 3-6 Cable Connector to Bulkhead Attachment

3.3 AC POWER AND GROUND CONNECTIONS

3.3.1 General Information

The system must be properly grounded and connected to a power source of the correct voltage and phase relationship to avoid bodily injury and damage to the equipment.

This subsection provides the information necessary to ensure that the system is safely grounded and that the input power is properly applied. Instructions are also included for making preliminary voltage measurements and adjustments.

3.3.2 Rules for Power Requirements -- Power Distribution Unit

1. UL requires that one and only one ac power cord be used to power all devices in a given rack.

2. All configurations require a Power Distribution Unit (PDU). This rule does not apply to an expansion (bulkhead) cabinet that is used to house bulkheads only.

3.3.3 Grounding System Installation

The grounding system within the cabinet is installed at the factory; however, the following steps should be performed to ensure proper installation:

1. Ensure that the following ground connections have been made for each 5-card chassis within the system (see Figure 3-6.1):

   a. The backplane bus bar at location A01-08BG1 should be connected via a braided cable to ground stud E01GD on the tray.

   b. Ground stud E02GD on the tray should be connected via a cable to ground stud E02GD on the wrapper.

2. Ensure that the following ground connections have been made for each 10-card chasis within the system (see Figure 3-6.1):

   a. The backplane bus bar at locations A01-08BG1 and A01-18BG1 should be connected via a braided cable to ground studs E01GD and E02GD on the tray.

   b. Ground stud E03GD on the tray should be connected via a cable to ground stud E03GD on the wrapper.

   c. The ground wire coming off the ac power cord of each power supply should be connected to the ac ground stud of the respective power supply.

d. The ac ground stud on both power supplies should be connected via a cable to ground studs E01GD (bottom supply) and E02GD (top supply) on the tray.

3. On the control panel, ensure that Q1AE02 is connected via a jumper cable to ground stud E02GD on the nearest five-card wrapper or to E03GD on the nearest ten-card wrapper (see Figure 3-6.2).

4. Ensure that ground stud E03GD on each 10-card tray and ground stud E02GD on each 5-card tray is connected via a jumper cable to E02 on the cabinet floor (see Figures 3-3 and 3-4).

5. If the system cabinet has a TB01, ensure that TB01 is connected via a jumper cable to ground stud E02, as shown in Figure 3-4.

NOTE

Although the expansion cabinet (if installed) may come with TB01, no connections have to be made to it.

6. Ensure that the PDU's ground connection, E01GD, is connected via a braided cable to ground stud E01 on the cabinet floor, as shown in Figure 3-7.

7. Ensure that the system is properly grounded to its L66 interface, as described in subsection 3.5.10.3 (step 3) and Figure 3-53.

8. If an expansion cabinet is attached to the system cabinet, ensure that the ground connection between the two cabinets has been properly made, as described in subsection 3.2.3 (step 4) and Figures 3-3 and 3-4.

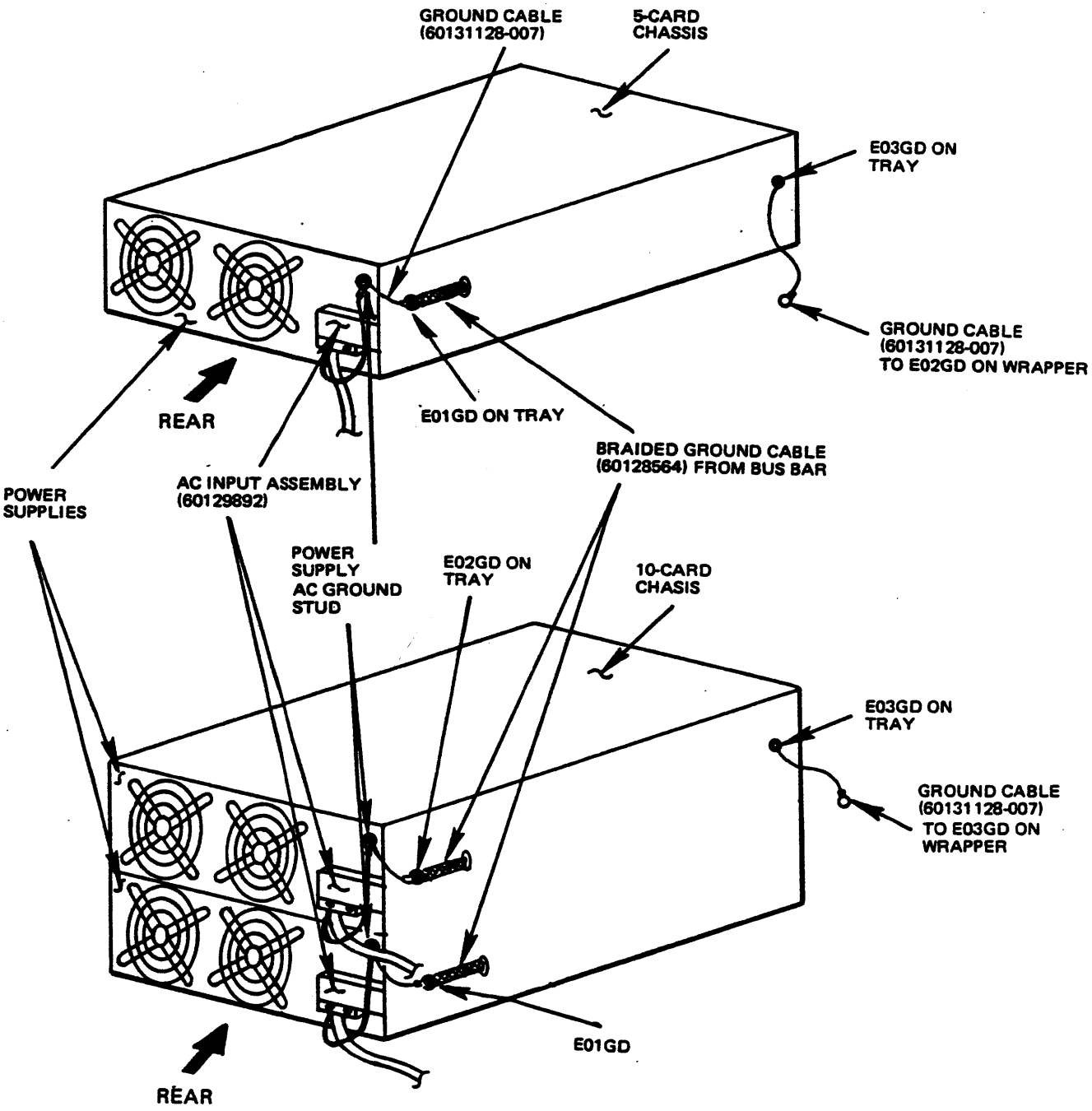


Figure 3-6.1 Card Chassis and Power Supply Grounds

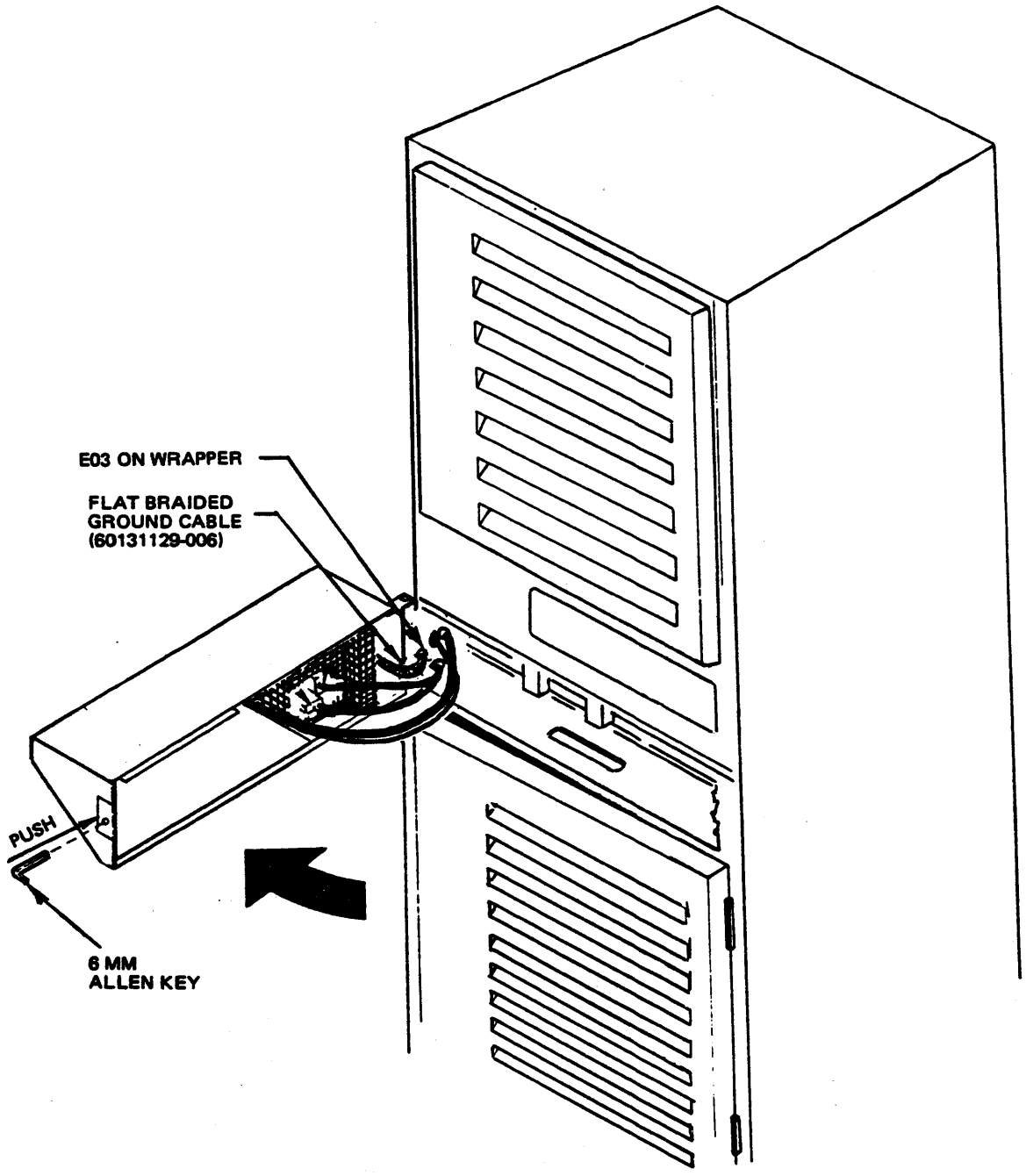


Figure 3-6.2 Control Panel Ground

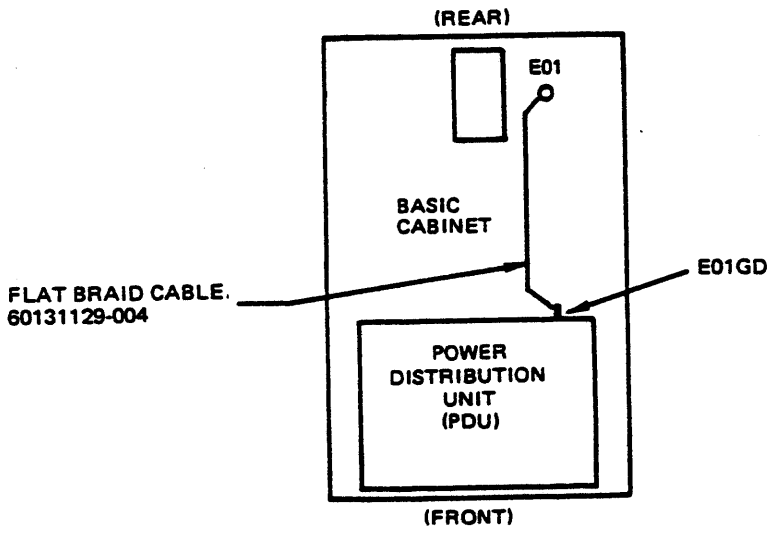


Figure 3-7 Grounding Within One-Cabinet System (Top View)

3.3.4 Connecting AC Power

Before connecting ac power to the system, read the following WARNING and CAUTION then connect the power according to Table 3-1.1 and Figure 3-8.

WARNING

To avoid bodily injury, all ac ON/OFF switches must be in the OFF position.

CAUTION

Before connecting any system components to ac power, verify that the ac electrical power service for the system is 120 Vac phase to neutral on all phases; otherwise, equipment damage may result (see Figure 3-8).

Table 3-1.1 U.S. and International Power Cable Color Codes

CONDUCTOR	U.S. COLORS	INTERNATIONAL COLORS
N - Neutral[a]	White	Blue
G - Ground[a]	Green or Green w/yellow stripe	Green w/yellow stripe
Phase A - (X)[a]	Black	Brown
Phase B - (Y)	Red	Black[b]
Phase C - (Z)	Blue	Black[b]

[a]Colors used in 3 wire (single phase) cord.

[b]Black wires may have color stripe to aid in identification.

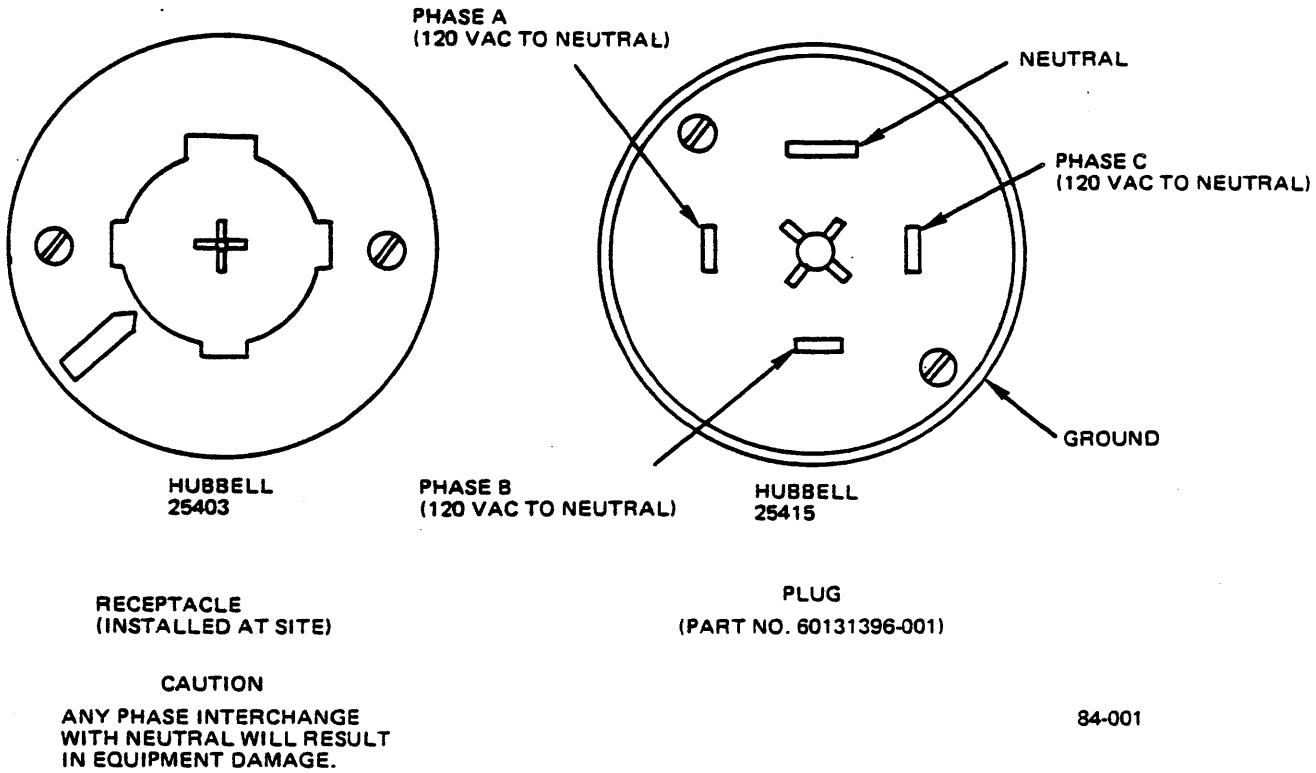


Figure 3-8 AC Power Cable Connections (Hubbell or Equivalent 5-Wire)

3.3.5 Power Distribution Unit

Refer to Figure 3-9, which shows the rear view of the Power Distribution Unit (PDU), and note the following:

1. The ac power cord from the diskette power supply must be plugged into receptacle J07.

2. The console ac power cord must also be plugged into receptacle J07.

3. The system power supplies are plugged into receptacles J02 through J06.

NOTE

The PDU has a total of 12 receptacles, four per phase. When plugging the system power supplies into the PDU, distribute the load evenly among the phases. For example, if six power supplies (including the diskette power supply) are to be plugged in, plug in two per phase.

Figure 3-10 is a block diagram of the PDU.

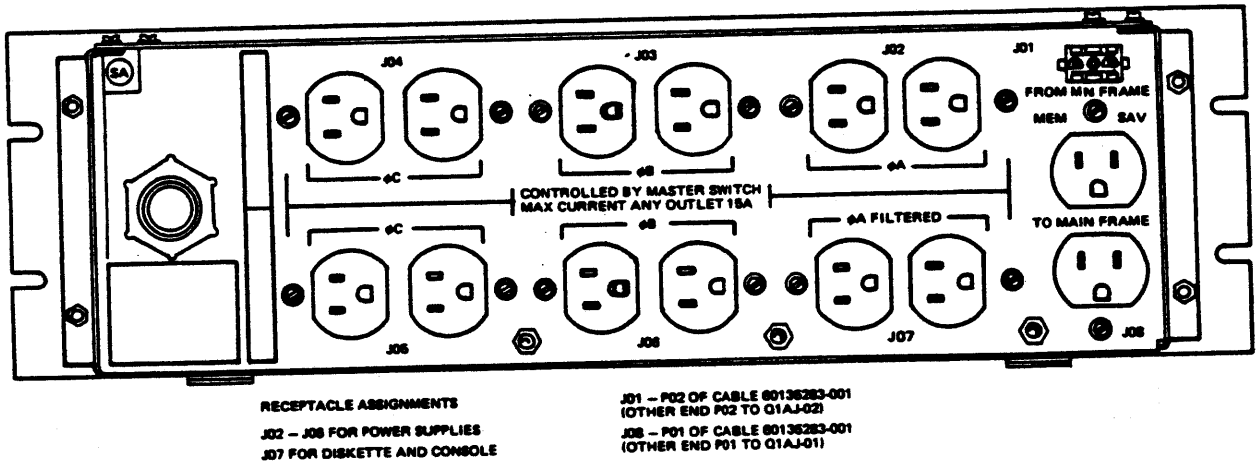


Figure 3-9 Power Distribution Unit, BPDU063B (Rear View)

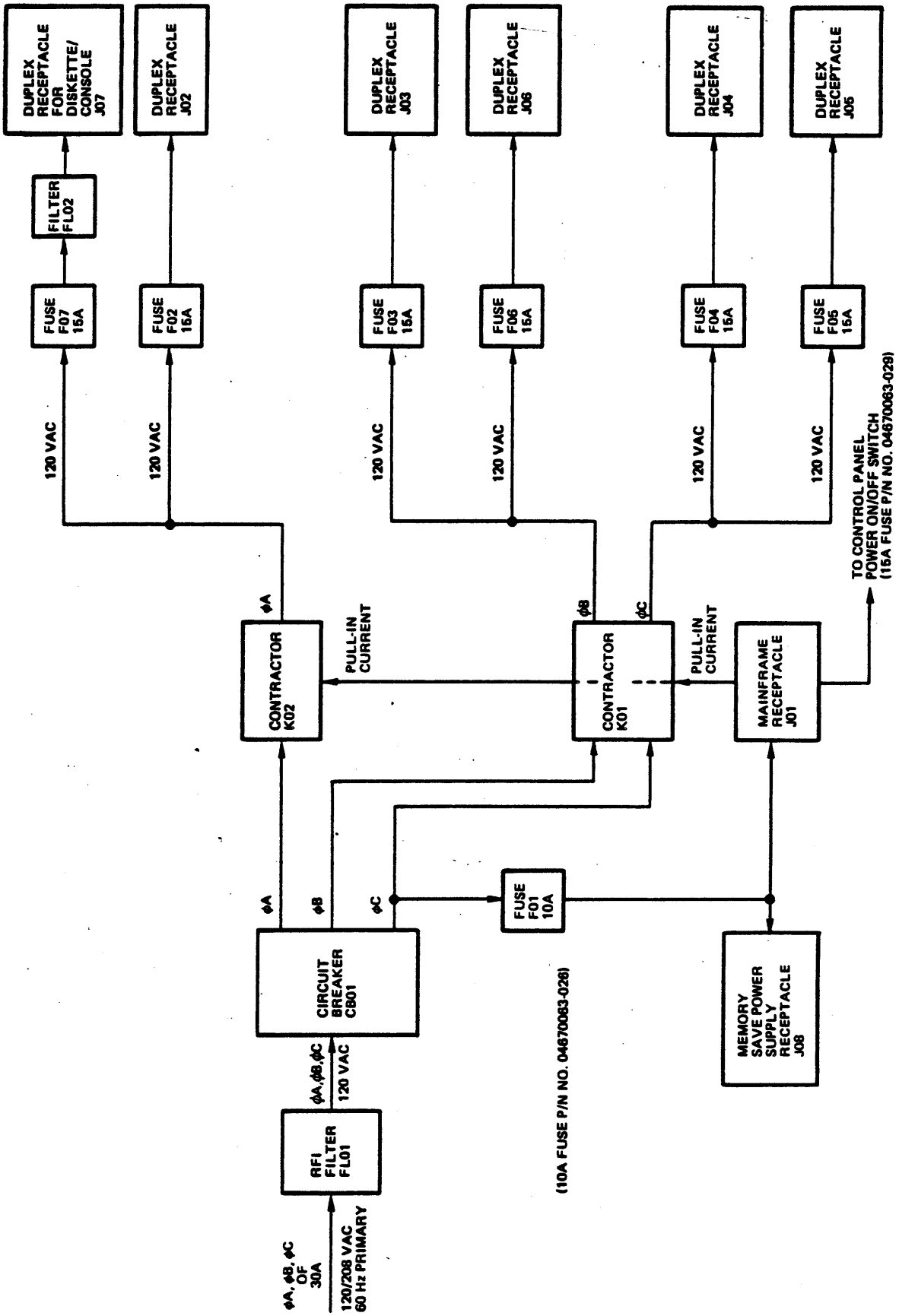


Figure 3-10 Power Distribution Unit Block Diagram

3.3.6 Power Supplies -- M150 (BPWU490A), M170 (BPWU500A), M176 (BPWU600A)

This subsection contains the power supply configuration rules, capabilities, and provides instructions for making preliminary power supply adjustments.

3.3.6.1 Power Supply Configuration Rules

The configuration rules are:

1. A 5-card segment is defined as the area powered by one power supply. A 10-card chassis contains two 5-card segments and is therefore powered by two power supplies.

2. Refer to Table 3-2 for the actual power calculations.

3. Special attention should be given to HDLC channel adapters because of very high power consumption.

Table 3-2 Current Rating (Amps) for System Boards (Sheet 1 of 2)

BOARDS	+5V	+12V	-12V
Diskette Adapter	1.2	-	-
SSC Controller	6.0	-	-
SSC PROM	2.7	-	-
Console Adapter	0.2	0.08	0.10
CPU-A	7.0	-	-
CPU-B	8.6	-	-
PROM	5.7	-	-
DIA Controller	3.8	-	-
DIA Interface-Pac	4.3	-	-
PIA Controller	6.5	-	-
PIA Interface-Pac	3.7	-	-
Cache Controller	5.1	-	-
Cache-Pac (4K)	8.3	-	-
Cache-Pac (2K)	4.4	-	-
IOM-A	9.8	-	-
IOM-B	8.6	-	-
PROM	3.3	-	-
Single Word Fetch Memory			
Actual	6.1	0.82	-
Standby	6.1	0.25	-
Double Word Fetch Memory			
Actual	6.5	0.91	-
Standby	6.5	0.25	-

Table 3-2 Current Rating (Amps) for System Boards (Sheet 2 of 2)

BOARDS	+5V	+12V	-12V
Page Control Unit (Pager)	8.7	-	-
PAT	2.6	-	-
PATN	-	-	-
Channel Interface Base	10.6	-	0.03
Dual Sync/Bisync Line Adapter	0.3	0.06	0.08
Dual Async Line Adapter	0.4	0.05	0.05
Sync/Bisync Current Mode Adapter	0.7	0.02	0.05
High Level Data Link Adapter	2.1	0.04	0.03
Balanced Line Broadband Adapter	0.5	0.02	0.13
Sync MIL-STD-188C Line Adapter	0.2	0.07	0.07
Autocall Line Adapter	0.2	0.06	0.05
Current Loop 20 mA	0.3	0.12	0.08
Dual Async MIL-STD-188C Line Adapter	0.2	0.11	0.09
Broadband Sync MIL-STD-188C Adapter	0.4	0.07	0.06
HDLC MIL-STD-188C Adapter	2.0	0.07	0.06
HDLC Broadband Balanced Line Adapter	4.4	0.04	0.12
HDLC Broadband Current Mode Adapter	4.5	0.04	0.02
Terminators	0.75	-	-
Terminator Dummy	-	-	-
Operator Control Panel	1.1	-	-

3.3.6.2 Power Supply Capabilities

M150 Power Supply (BPWU490A)

	Current	
Output Voltages	Maximum	Minimum
+5V	55.0*	10.0
+12V	3.0	0
-12V	3.0	0

*In configurations where the total 5-volt current is less than 55 amps, the difference can be traded for extra I (+12V) according to the equation:

$$I_{\pm 12V} = 4.0 + \frac{(55 - I_{+5V})}{4}$$ or maximum of 5.0 amps

M170 Power Supply (BPWU500A)

Output Voltages	Current Maximum	Current Minimum
+5V	70.0*	10.0
+12V	3.0	0
-12V	3.0	0

*In configurations where the total 5-volt current is less or greater than 70 amps, the difference can be traded for I (+12V) according to the equation:

$$I_{\pm 12V} - 4.0 + \frac{(70 - I_{+5V})}{4}$$ or maximum of 5.0 amps

M176 Power Supply (BPWU600A)

Output Voltages	Current Maximum	Current Minimum
+5V	70.02*	10.0
+12V	3.01	0
-12V	3.01	0
+18V	3.01	0

*In configurations where the total 5-volt current is less than 70 amps, the difference can be traded for extra I (+12V) according to the equation:

$$I_{\pm 12V} = 4.0 + \frac{(70 - I_{+5V})}{4}$$ or a maximum of 5.0 amps

3.3.6.3 Power Supply Adjustment (+5Vdc)

Figure 3-11 shows the rear view of a power supply. The location of the +5Vdc adjustment control is shown on the figure.

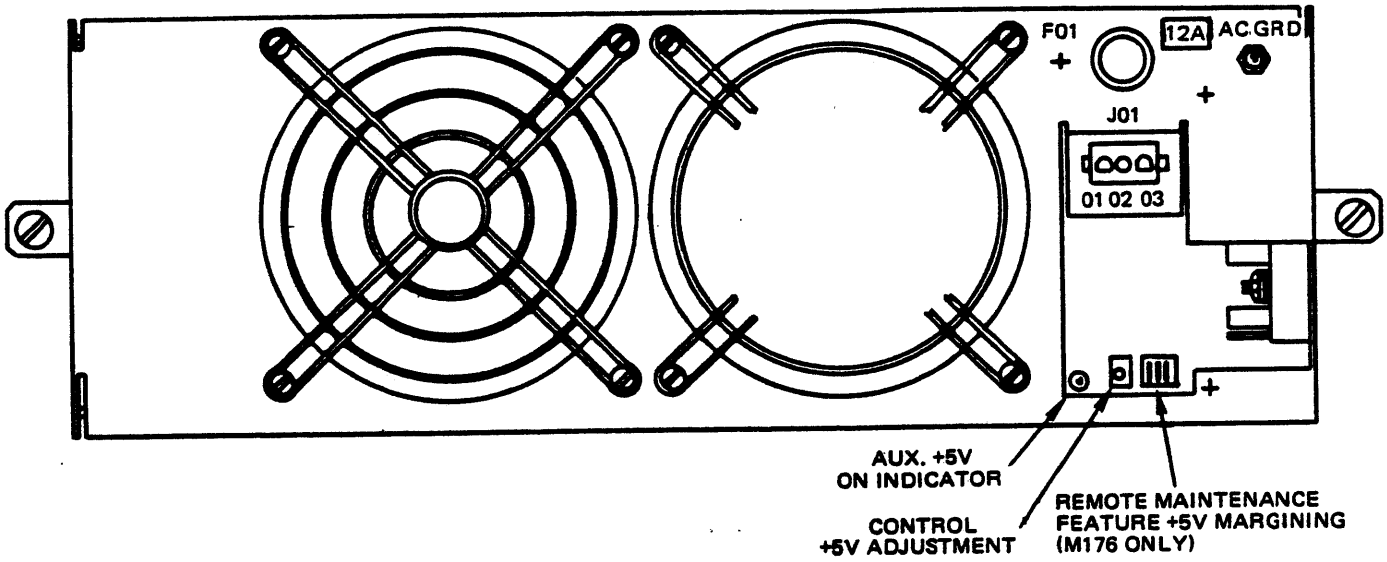


Figure 3-11 Power Supply (Rear View)

3.3.7 Power Requirements and Heat Load

3.3.7.1 Power Requirements

The power requirements for the system are as follows:

- AC Receptacle: Hubbell 25403 (mates with Hubbell 25415, see Figure 3-8)
- Circuit Breaker: 30 amp, 3%
- Number of Wires: 5 (#10 AWG)
- Phase Sensitive: No

3.3.7.2 Heat Load

The heat load of the system is as follows:

- KVA: 7.8
- Heat Gain: 16.6 KBTU

3.4 SYSTEM POWER UP, VOLTAGE CHECKS, AND ADJUSTMENTS

This subsection provides the information necessary to apply ac power to the system, make preliminary voltage checks, and run a system checkout test.

3.4.1 System Power Up

To power up the system, proceed as follows:

1. Connect the ac power cable from the system cabinet to the customer's 5-wire ac receptacle.

2. Set the circuit breaker on the PDU to the ON position.

3. Set the POWER switch on the operator control panel to the ON (up) position. Observe that the DC ON indicator is lit.

4. The system is now powered up.

5. The system voltage is preset at the factory and does not normally require any further adjustment. However, if it is necessary to check or readjust the voltage, proceed to step 6.

6. Verification of the proper voltage level on the system requires measuring the voltage on a maximum of four board types (configuration dependent). Measure at least one board for each 5-card slot. These boards are BF4IOA, BF4IOB, BF4HML, BF2MAE, BF2MCE and BF2MYE. One of these boards is in any given 5-card segment; thus, each power supply in the system is checked.

NOTE

A voltmeter with at least 0.01 volt accuracy must be used, such as a Fluke 8020A digital voltmeter or the equivalent. Do not connect the meter's ground lead to the chassis, the wrapper, or any other place except the ground side of the component indicated. Do not allow the meter's leads to contact adjacent terminals or the board frame.

The test points for each board are shown in Figure 3-12. Two levels of memory boards are shown; they have the following differences:

a. For BF2MAE and BF2MCE (Level 2.1, 60130768 and 60130766) memory boards, attach the meter probes across the capacitor shown in Figure 3-12. It may be necessary to remove the adapter board in order to access this point.

b. For BF2MAE and BF2MCE (Level 2.2, 60132550 and 60132544) memory boards, attach the meter probes to the test point shown in Figure 3-12.

c. For BF2MYE (Level 2.2, 60138544) memory boards, all voltage adjustments should be in reference to the CPU or PCL.

NOTE

The voltage at the above test points should measure between 4.95 volts and 5.05 volts. If the voltage is not within this range, adjust the 5-volt supply to 5.0 ±0.01 volts. Refer to Figure 3-11 for the location of the 5-volt adjustment control.

3.4.2 System Checkout

To check the system for proper operation, proceed as follows:

1. Run the Quality Logic Tests (QLTs) detailed in subsection 4.1.4.

2. Run the Extended Quality Logic Tests (E-QLTs) detailed in subsection 4.1.5.

3. Run the Test and Diagnostic (T&D) tests detailed in Section 3 of the DATANET Network Processor Operation Manual (subsection 1.2 contains the manual order number).

4. If a Peripheral Interface Adapter (PIA) is installed in the system, connect the PIA to the Microprogrammed Controller (MPC) as detailed in subsection 3.5.8.3.

5. Run T&D Test M2 detailed in Section 3 of the DATANET Network Processor Operation Manual.

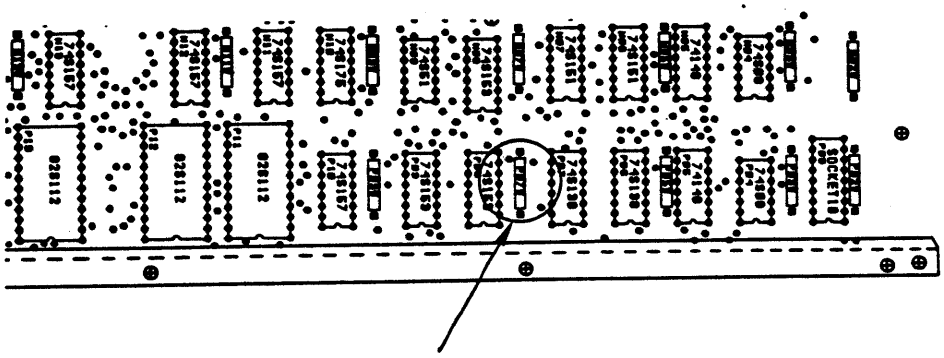
6. Install the Direct Interface Adapter (DIA) to the L66 Input Output Multiplexer (IOM), interconnecting the cables as detailed in subsection 3.5.10.3.

7. Run T&D Tests DA, DI, and POL detailed in Section 3 in the DATANET Network Processor Operation Manual.

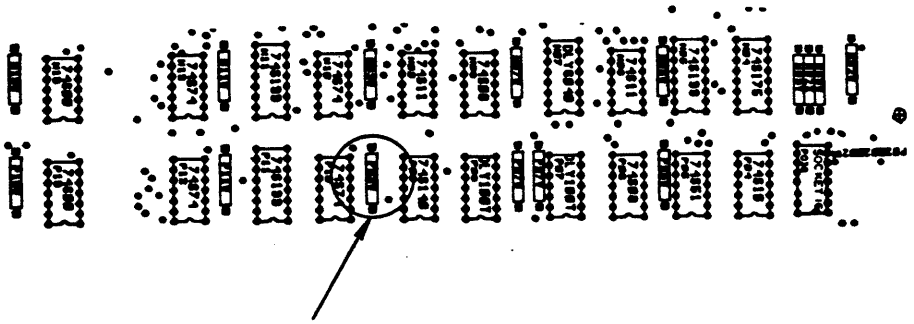
8. Install the Channel Interface Base (CIB)/Honeywell Multiline Controller (HMLC) subchannel, interconnecting the cables to the customer's communications devices as detailed in subsection 3.5.11.8.

9. The system installation and checkout is now completed.

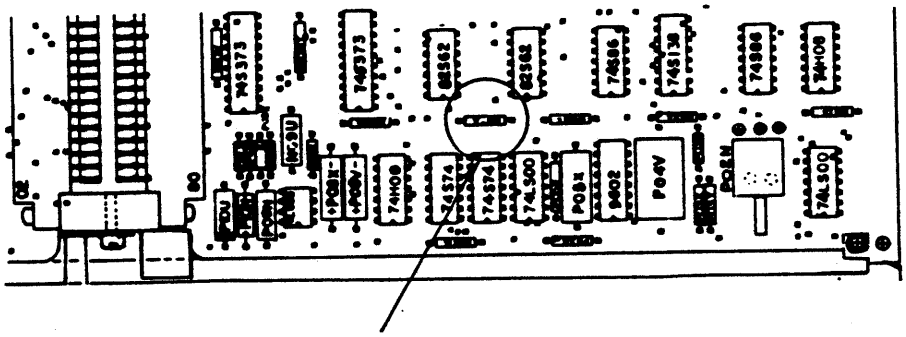
BF4IOA



BF4IOB



BF2MAE
(LEVEL 2.1)
(60130768)



BF2MCE
(LEVEL 2.1)
(60130766)

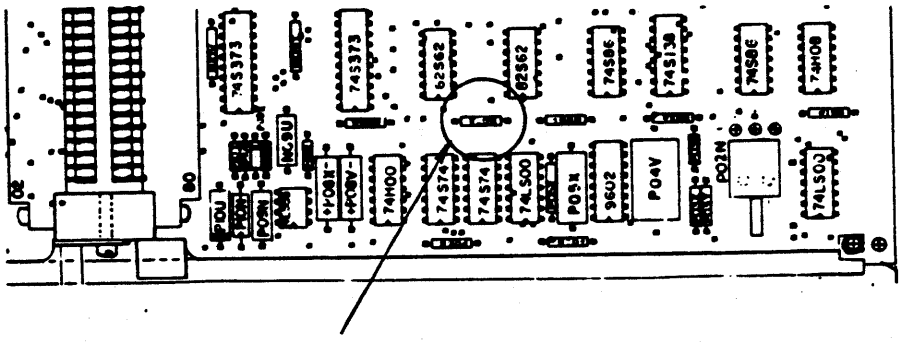
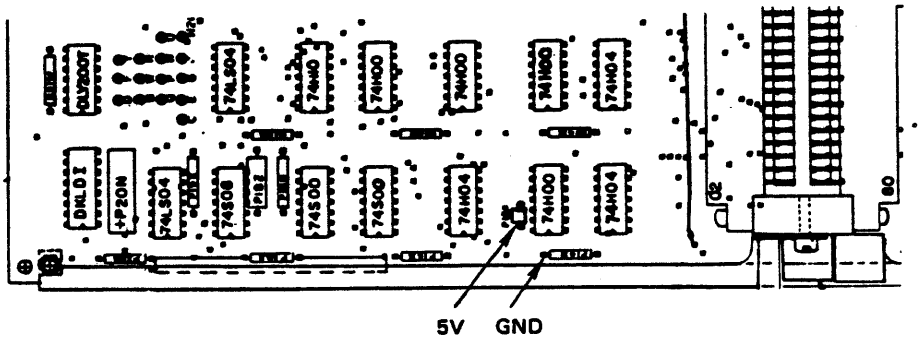
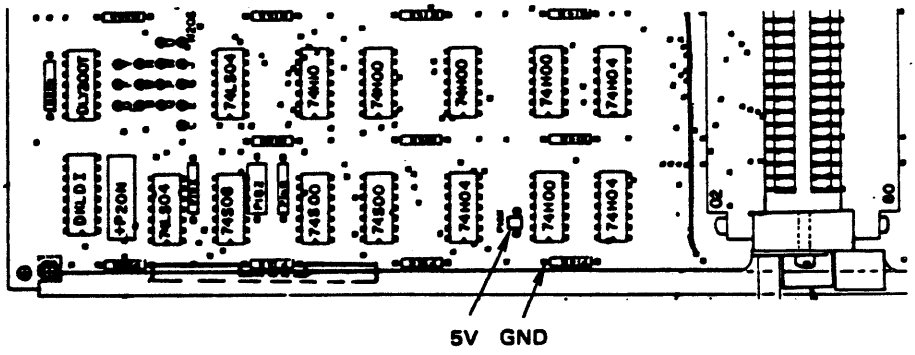


Figure 3-12 System Voltage Test Points (Sheet 1 of 2)

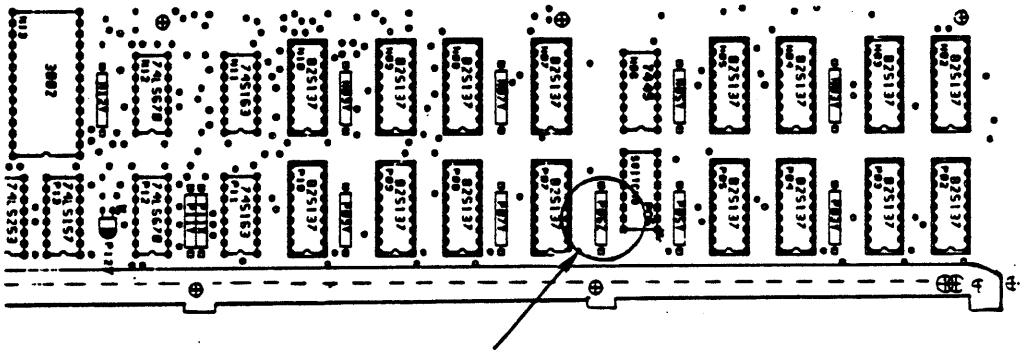
BF2MAE
(LEVEL 2.2)
(60132550)



BF2MCE
(LEVEL 2.2)
(60132544)



BF4HML



BF2MYE
(LEVEL 2.2)
(60138544)

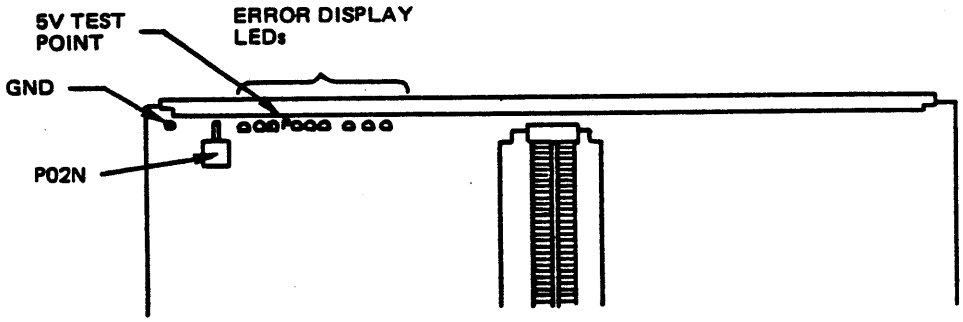


Figure 3-12 System Voltage Test Points (Sheet 2 of 2)

3.5 SYSTEM COMPONENTS

This subsection covers the configuration rules, component descriptions, installation instructions, cable connections, and the required switch settings for the components that are included in the system.

3.5.1 Rules for Chassis to Rack Relationships

The configuration rules for the chassis to rack relationships are as follows (see Figure 1-2):

1. The Power Distribution Unit (PDU) is always installed in the bottom position of the system cabinet.

2. The I/O bus extension chassis (60132152-001) are located above the basic 10-card chassis (60132152-002).

   a. There cannot be more than two extension chassis on the I/O bus (communications units area).

   b. Both extension chassis must have side cutouts.

3. The system bus (memory) extension chassis is located below the basic 10-card chassis.

4. The diskette is located immediately above the PDU.

5. When more than one chassis is required, two bus extender cables (60128386) must connect the lowest slot of the upper chassis with the highest slot of the lower chassis. Figure 3-13 shows the installation of the cables in the extension chassis. (The lowest slot in the upper chassis becomes unavailable for processor/controller board use.)

6. No blank spacer panels are required.

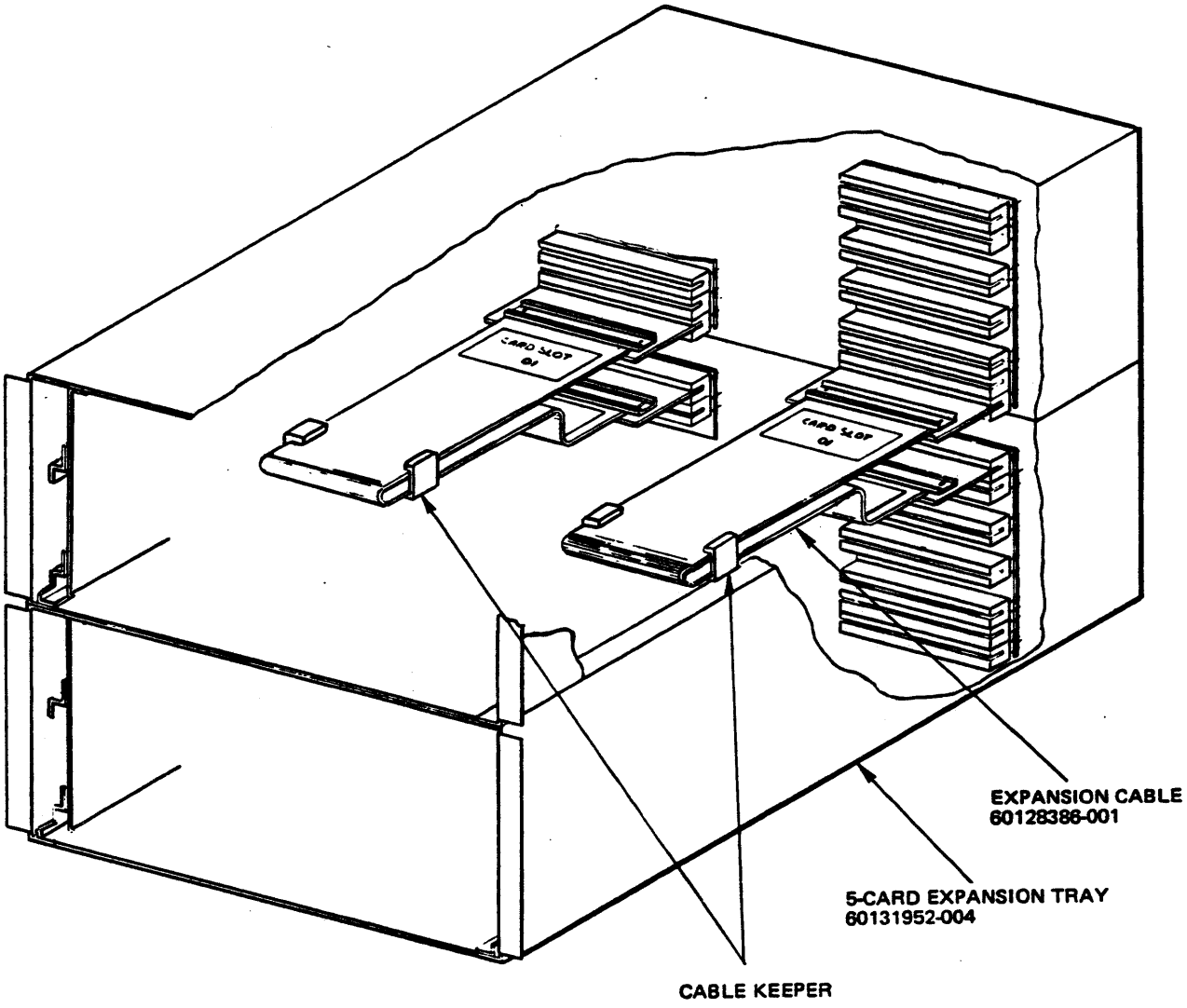


Figure 3-13 Bus Extension Chassis and Cables

3.5.2 Rules for Controller/Processor Board to Chassis Relationships

The rules for the controller/processor board to chassis relationships are as follows (see Figure 3-14):

1. General Rule: In the basic 10-board chassis, the IOM board pair occupies the center two controller board slots. The slot above the top IOM (IOM-A) board is occupied by a BX2RT4 terminator board. The slot between the two IOM boards is occupied by a BX2RT3 terminator board.

2. I/O Bus Rules: The ascending order from the IOM (decreasing priority) is as follows:

   a. PIA -- none required. Optional.

   b. DIA -- One DIA is required. A maximum of one more may be installed as an option.

   c. SSC -- One SSC is required.

   d. CIB -- Optional. A maximum of 12 CIBs per system is allowed.

3. System Bus Rules: The descending order from the IOM (increasing priority) is as follows:

   a. Cache -- optional.
   b. CPU board pair.
   c. Page control unit (pager) -- optional.
   d. Memory.

4. Extension Chassis Rules: The extension chassis rules are as follows:

   a. There must be no more than nine boards in a 10-card chassis.

   b. Any unused board slots falling between used slots must be filled by a dummy board (BX2RT5). Dummy boards are not required to fill up a chassis between the last board and the end of the chassis.

   c. Memory Extension Chassis (System Bus):

      (1) The pager is required if there is more than 32K of memory; it must be in the top slot of the extension chassis.

      (2) The 32K capacity per memory board (BF2MAE, BF2MCE) is limited to eight controller boards (256K memory).

(3) The 128K capacity per memory board (BF2MYE) is limited to two controller boards (256K memory).

(4) If there is a cache and 32K or less of memory, a BX2RT4 terminator is required immediately above the memory.

(5) If there is no cache and 32K or less of memory, a BX2RT4 terminator is required immediately below the memory.

(6) If there is 256K words of memory, a BX2RT4 terminator board must be installed immediately above the last memory board.

d. Communications Extension Chassis (I/O Bus):

(1) The first unused board slot after the last CIB or DIA must have a terminator. If the chassis is full, then the top slot in the chassis must have a terminator (BX2RT3).

(2) Two DIAs must be powered by separate power supplies to even the power load.

(3) When assigning CLAs to one CIB, the overriding rule is that the sum of the throughput factors (see Table 3-3) for all CLAs on the CIB must not exceed 100. Subject to this constraint, assignment is as follows:

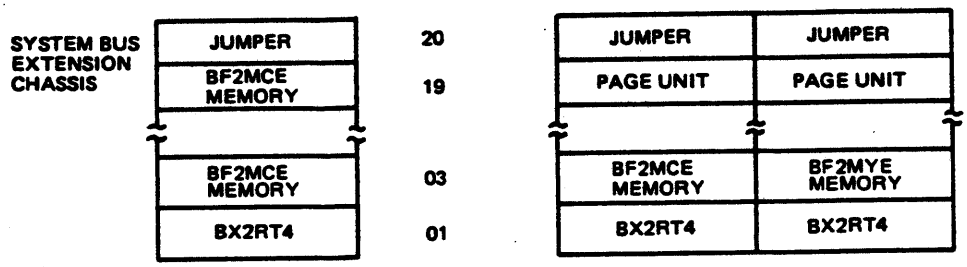
(a) Assign the class 7 CLAs, one per CIB, to the lowest priority position of the highest priority CIB.

(b) Assign class 5 and 6 CLAs, one per CIB, to the highest priority position of the next highest priority CIBs after those used for class 7. Throughput limitations prohibit class 7 on the same CIB as classes 5 and 6.

(c) Divide the medium speed synchronous CLAs, classes 1 through 4, as evenly as possible among the remaining CIBs with the highest speed in the highest priority position.

(d) Assign the remaining asynchronous CLAs to the available positions on the CIBs.

CARD SLOT NO.	WITHOUT CACHE			WITH CACHE		
	MEMORY < 128K	MEMORY < 32K	MEMORY > 32K	MEMORY < 32K	MEMORY > 32K	MEMORY > 128K
20	JUMPER TO EXTENSION IF NEEDED					
	I/O BUS					
12	TERMINATOR (BX2RT4)* High					
11	IOM (A)					
10	TERMINATOR (BX2RT3)** Low					
09	IOM (B)					
08						
07	CPU	CPU	CPU	CACHE	CACHE	CACHE
06						
05	CPU	CPU	CPU	CPU	CPU	CPU
04						
03	PAGE UNIT	BF2MAE MEMORY	PAGE UNIT	CPU	CPU	CPU
02	BX2RT4	BF2MCE MEMORY		BX2RT4		
01	BF2MYE MEMORY	BX2TR4	JUMPER	MEMORY	JUMPER	JUMPER



NOTE

ODD-NUMBERED SLOTS ARE BOARD SLOTS.
EVEN-NUMBERED SLOTS ARE EMPTY, WITH THE EXCEPTION OF TERMINATORS IN 2, 10, AND 12.

*BX2RT4 – HIGH PRIORITY TERMINATOR (60130115-001)
**BX2RT3 – LOW PRIORITY TERMINATOR (60127916-001)
BX2RT5 – DUMMY BOARD (60130177-001)

Figure 3-14 System Chassis to Board Relationship

Table 3-3 CLA Throughput Specifications

CLA CLASS	IPI	BOARD TYPE	MARKETING OPTION	THROUGHPUT FACTOR	BAUD RATE
1 & 2	BMLF101B	BD2ASC	DCF6612	4.5 or 8.2	9,600 HDX
1 & 2	BMLF103A	BD2LAS	DCF6611	4.5 or 8.2	9,600 HDX
1 & 2	BMLFCLAA	BD2CLA	DCF6610	4.5 or 8.2	9,600 HDX
1 & 2	BMLF188A	BD2188	DCF6614	4.5 or 8.2	9,600 HDX
1 & 2	BMLFA88A	BD2A88	DCF6615	4.5 or 8.2	9,600 HDX
3	BMLF618A	BD2LAB	DCF6618	10.1	9,600 HDX
4	BMLFH88A	BD2H88	DCF6617	8.8	9,600 FDX
4	BMLFDLCA	BD2DLC	DCF6620	8.8	9,600 FDX
5	BMLF619A	BD2CMD	DCF6619	55.0	56,000 FDX
5	BMLF627A	BD2BLB	DCF6627	55.0	56,000 FDX
5	BMLF616A	BD2B88	DCF6616	55.0	56,000 FDX
6	BMLF619A	BD2CMD	DCF6621	70.0	56,000 FDX
7	BMLFDLDA	BH4DLD	DCF6622	40.0	56,000 FDX
7	BMLFDLEA	BH4DLE	DCF6623	40.0	56,000 FDX
7	BMLFDL8A	BHMDL8	DCF6628	40.0	56,000 FDX

NOTES

1. Class 1 = CCT (Character Control Table) feature not used. Class 2 = CCT (Character Control Table) feature used. In the absence of specific information, assume class 2.

2. For classes 5, 6, and 7 the throughput factor is for broadband operation at 56,000 bits per second with CCT for 5. Class 5 without CCT throughput factor is 35.

3. For jumper component allocation, refer to subsection 3.5.11.7.

3.5.3 Memory Components

The system memory consists of a 32K word capacity for memory controller board configuration BF2MAE, BF2MCE or a 128K word capacity for memory controller board configuration BF2MYE. Up to eight controller boards can be used with the 32K word configuration and one or two controller boards can be used with the 128K word configuration. Figure 3-15 shows the layout of the memory boards with the Memory-Pacs mounted on the boards.

3.5.3.1 Memory Descriptions

This subsection provides a general description of the two memory configurations.

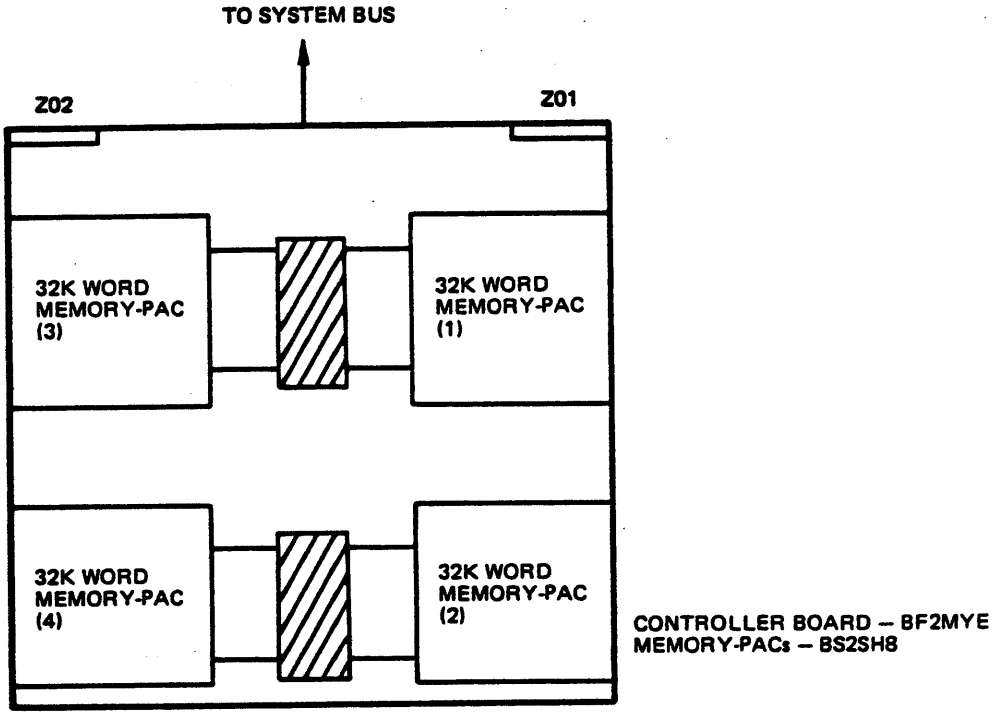
3.5.3.1.1 32K Word Memory Capacity (BF2MAE, BF2MCE)

The minimum to maximum storage capacity of the memory unit is 8K to 32K words. The minimum to maximum storage capacity allowed in any one system configuration is 8K to 256K words; hence, the minimum to maximum number of memory units allowed in any one system configuration is one to eight. Each memory unit in a system configuration must be installed sequentially, starting at the physical bottom (high priority) end of the bus (see Figure 1-3).

The memory unit consists of a memory controller and up to four memory modules, called memory boards. The memory boards are described in subsequent paragraphs. The memory controller consists of a single 15- by 16-inch two-layer logic board that contains the memory control logic, two 50-pin finger type connectors (Z01 and Z02), and four 80-pin female type connectors (W01 through W04). The two 50-pin connectors logically connect the memory controller into the bus, and the four 80-pin connectors logically connect and physically support up to four memory boards on a memory controller (see Figure 3-15). The type of main memory unit (i.e., single or double word fetch) is identified by a six-character mnemonic as shown in the following table. Included in the table is the associated memory board used with each memory unit.

MEMORY CONTROLLER		ASSOCIATED MEMORY BOARD	REMARKS
TYPE	MNEMONIC		
Single Word Fetch	BF2MAE	BS2TA8	-
Double Word Fetch	BF2MCE	BS2TA8 or BD2T48	EDAC Only

The memory controller also contains the facilities to set up a bus address and to disable or enable the EDAC feature. The facilities to set up a controller address consist of two rocker arm switch assemblies for the BF2MAE memory controller and five



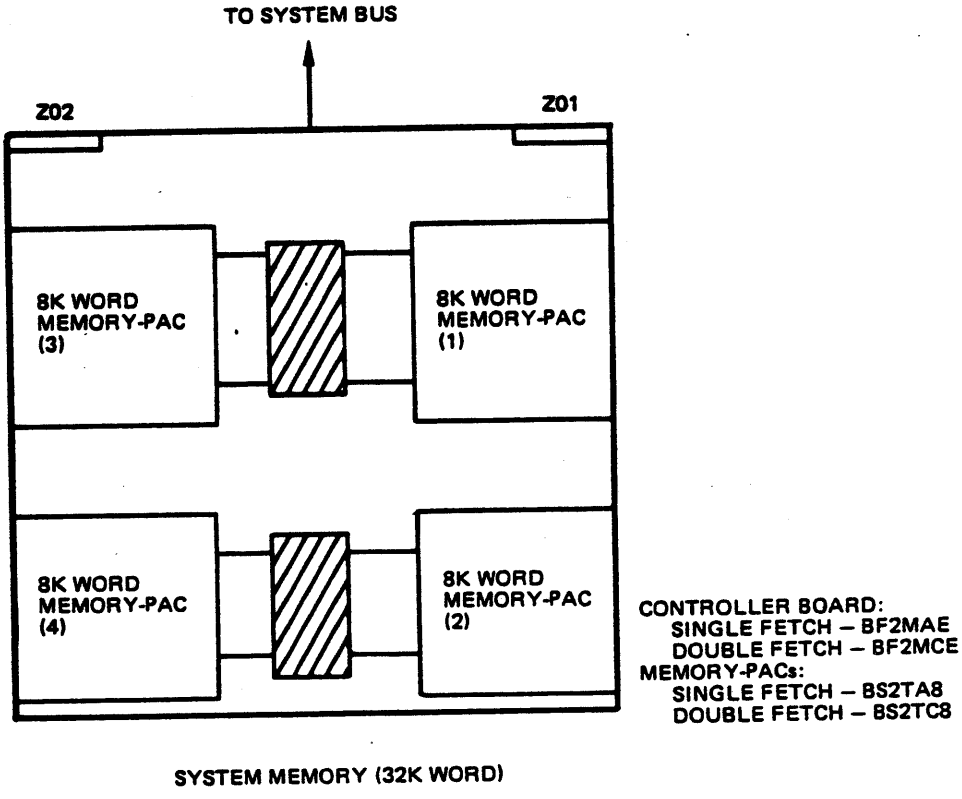


Figure 3-15 System Memory Configurations

rocker arm switch assemblies for the BF2MCE memory controller (see Figure 3-16 and subsection 3.5.3.2.1). The facility to disable or enable the EDAC feature consists of a single jumper between pins J05A and J05P. This feature must always be enabled; i.e., the jumper must be removed (see Figure 3-16 for jumper locations).

NOTE

The jumpers that enable or disable the single or double word fetch operation on a controller are included in the illustrations for verification purposes only.

The facilities to check data parity errors include a spring-loaded toggle switch that is used with the T&D to test the EDAC logic, or to test the data parity logic. The manner in which the parity check is accomplished is described in the T&D procedures.

A memory board is constructed on a single logic board (approximately 6.7 inches square) and uses 4K word Metal Oxide Semiconductor (MOS) RAM storage devices as the main storage medium to provide a fixed storage capacity of 8K words on a single memory board. Each 8K word memory board is physically supported by and logically connected onto the memory controller by one of four 80-pin connectors described earlier. This arrangement permits the installation of one to four memory boards for a minimum to maximum storage capacity of 8K to 32K words in a single word fetch memory unit. In a double word fetch memory unit, the storage capacity is either 16K or 32K words. When one or more memory boards are installed in a controller, they must be sequentially installed, beginning with the first connector (W01) on the controller. Also, in the case of a single word fetch memory controller, memory boards must be installed in 8K word increments (i.e., one memory board); in the case of a double word fetch memory controller, boards must be installed in 16K word increments (i.e., two memory boards).

3.5.3.1.2 128K Word Memory Capacity (BF2MYE)

Each memory controller board supports from one to four 32K word Memory-Pacs for a total of 128K words of memory. In single word pull applications, memory can be increased in 32K increments; in double word pull applications, memory must be increased in 64K increments.

A system may have one or two memory controller boards for a total of 256K words of memory. Memory (see Figure 1-3) occupies the high priority slots on the system bus.

The memory controller board (BF2MYE) is a 15-inch by 16-inch, two-layer etched board that contains all the logic needed to perform memory timing, refresh operations, address distribution and decoding, read/write functions, and bus interface operations.

The BF2MYE board is easily identified by nine LEDs and a toggle switch at one corner. The Internal Product Identifier (IPI) number for the memory controller is BMMU031A.

The Memory-Pacs are 6.5-inch by 6.5-inch etched boards (BS2SH8) that contain the Random Access Memory (RAM) chips for bit storage and a minimum amount of logic, such as, clock decoding and address and read/write buffers. The IPI number for the Memory-Pac is BCMM048B. Each Memory-Pac is connected to the memory controller via an 80-pin connector.

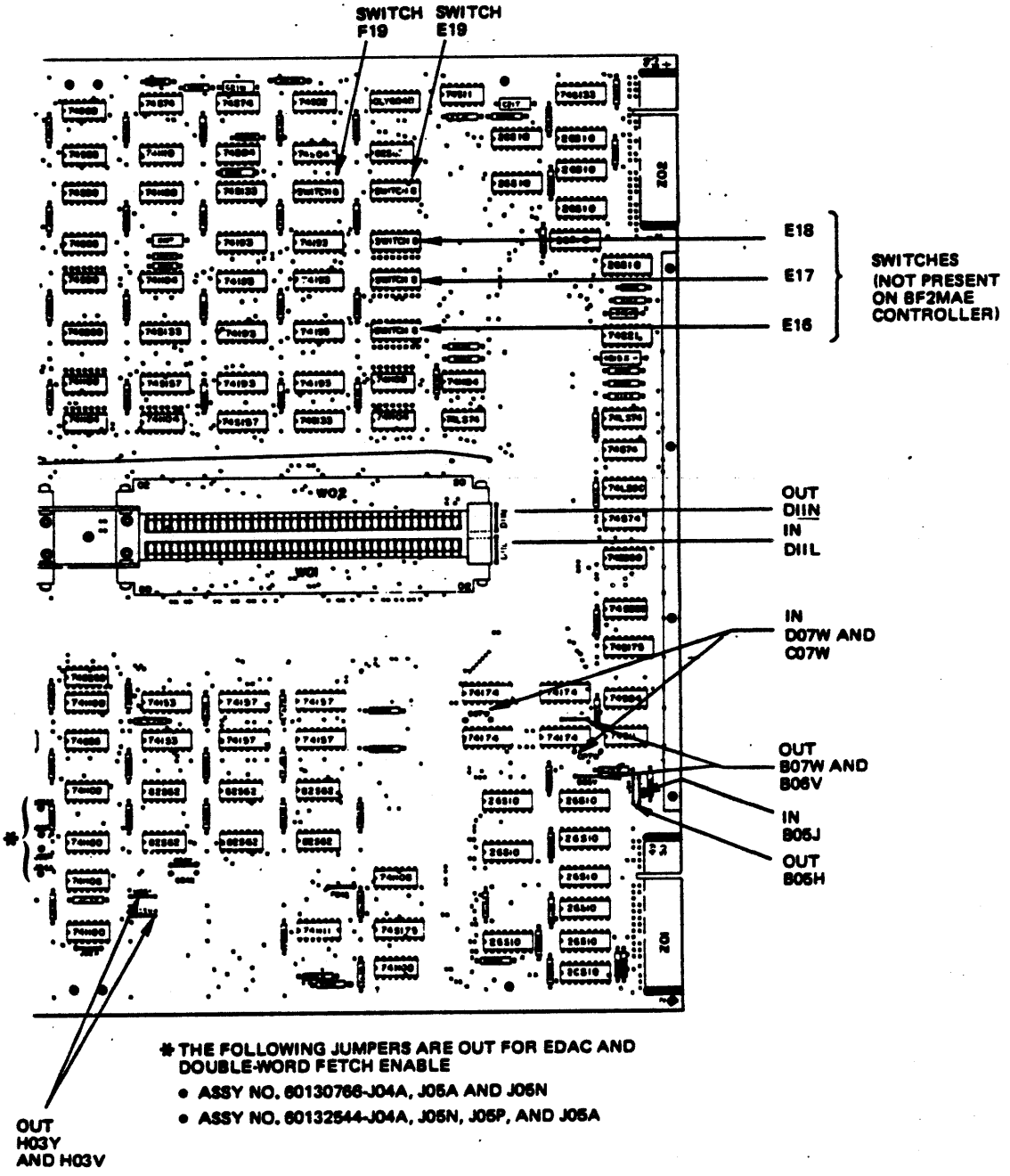


Figure 3-16 Switch and Jumper Locations (BF2MAE, BF2MCE)

3.5.3.2 Memory Address Switch Settings

The switches on the memory controller boards must be set according to the following subsections. Figure 3-16 shows the location of the switches and jumpers on the BF2MAE and BF2MCE boards. Figure 3-17 shows the location of the jumpers on the CPU PROM-PAC. Figure 3-18 shows the location of the switches on the BF2MYE board.

3.5.3.2.1 BF2MAE and BF2MCE Switch Settings

Set the switches on these boards according to the following charts:

BF2MAE & BF2MCE CONTROLLER BOARDS	SWITCH @ LOCATION F19 1 2 3 4 5 6 7 8	SWITCH @ LOCATION E19 1 2 3 4 5 6 7 8
1 (0 - 32K)	1 0 1 0 1 0 1 0	1 0 1 0 1 0 1 0
2 (32K - 64K)	0 1 1 0 1 0 1 0	1 0 1 0 1 0 1 0
3 (64K - 96K)	1 0 1 0 1 0 1 0	1 0 1 0 0 1 1 0
4 (96K - 128K)	0 1 1 0 1 0 1 0	1 0 1 0 0 1 1 0
5 (128K - 160K)	1 0 1 0 1 0 1 0	1 0 0 1 1 0 1 0
6 (160K - 192K)	0 1 1 0 1 0 1 0	1 0 0 1 1 0 1 0
7 (192K - 224K)	1 0 1 0 1 0 1 0	1 0 0 1 0 1 1 0
8 (224K - 256K)	0 1 1 0 1 0 1 0	1 0 0 1 0 1 1 0

BF2MCE CONTROLLER BOARD	SWITCH @ LOCATION E18 1 2 3 4 5 6 7 8	SWITCH @ LOCATION E17 1 2 3 4 5 6 7 8	SWITCH @ LOCATION E16 1 2 3 4 5 6 7 8
Double Word Pull (with Cache Memory)	1 0 0 0 0 1 0 1	0 1 0 1 0 1 0 0	1 0 1 0 1 0 0 1
Single Word Pull* (without Cache Memory)	1 0 0 1 0 0 1 0	0 1 0 1 0 0 0 1	1 0 1 0 1 0 0 1

*If the cache memory is not installed and one of the Memory-Pacs fails, resetting the switches as shown will limit memory loss to 8K words rather than 16K words, which would be a total loss for a double word fetch memory. (A 32K word memory becomes a 24K word memory.) If the cache memory is installed, configure for 16K words less memory. The cache memory functions only with double word fetch memory.

1. Ensure that the jumper installations on the boards are as shown in Figure 3-16.

2. If the BF2MCE board is used, jumper K09V on the CPU PROM-PAC (see Figure 3-17) must be installed. If the BF2MAE board is used, jumper K09V on the CPU PROM-PAC must not be installed.

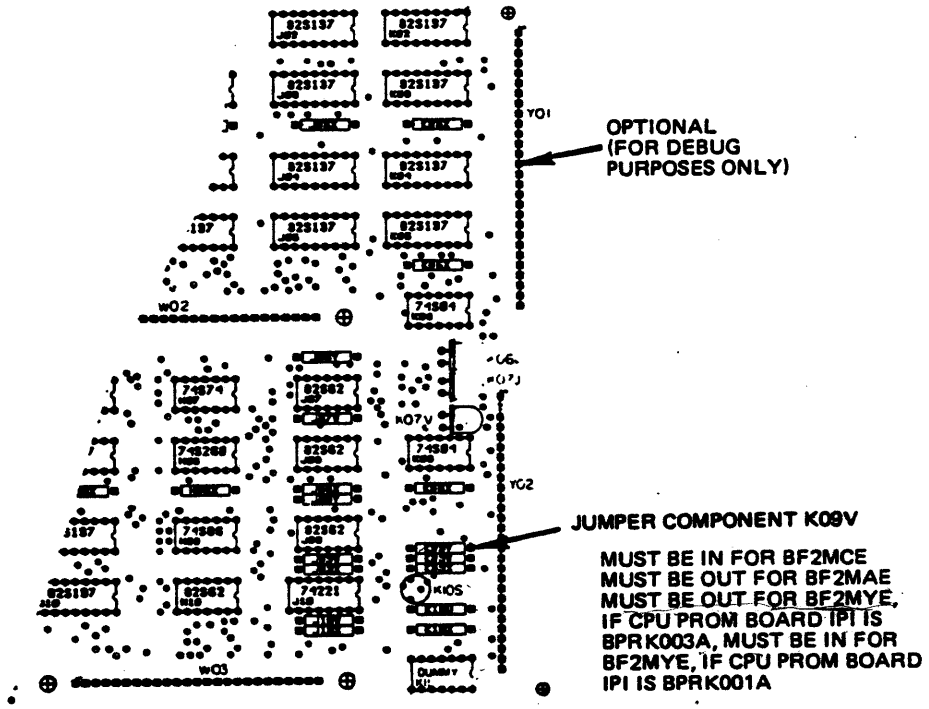


Figure 3-17 CPU PROM Board Jumper Locations (BH2PRK)

3.5.3.2.2 BF2MYE Switch Settings

Set the switches according to the following charts:

CAUTION

To avoid damaging the switches, be careful when making the switch settings. The use of a small non-metallic tool, such as a toothpick, is recommended.

BF2MYE CONTROLLER BOARD	SWITCH @ LOCATION F19 1 2 3 4 5 6 7 8
1 (0 through 128K) 2 (128K through 256K)	0 0 1 1 1 1 1 1 0 0 0 1 1 1 1 1

BF2MYE CONTROLLER BOARD	SWITCH @ LOCATION E16 1 2 3 4 5 6 7 8 9 10	SWITCH @ LOCATION E17 1 2 3 4 5 6 7 8 9 10
Single Word Pull Double Word Pull	0 1 0 1 1 1 0 0 0 1 0 1 0 1 1 1 0 0 0 0	0 0 0 1 1 0 0 0 0 0 1 0 0 0 0 0 0 0 1 0

BF2MYE CONTROLLER BOARD	SWITCH @ LOCATION E18 1 2 3 4 5 6 7 8 9 10	H04X F04S 1 2 1 2
Single Word Pull Double Word Pull	0 1 0 0 0 1 0 1 0 0 0 1 0 0 0 1 0 1 0 0	0 1 0 0 0 0 1 0

NOTE

When using a BF2MYE controller board and a CPU PROM-PAC with an IPI number of BPRK003A, make sure that jumper K09V on the CPU PROM-PAC is not installed (see Figure 3-17). When using a BF2MYE controller board and a CPU PROM-PAC with an IPI number of BPRK001A, make sure that jumper K09V on the CPU PROM-PAC is installed.

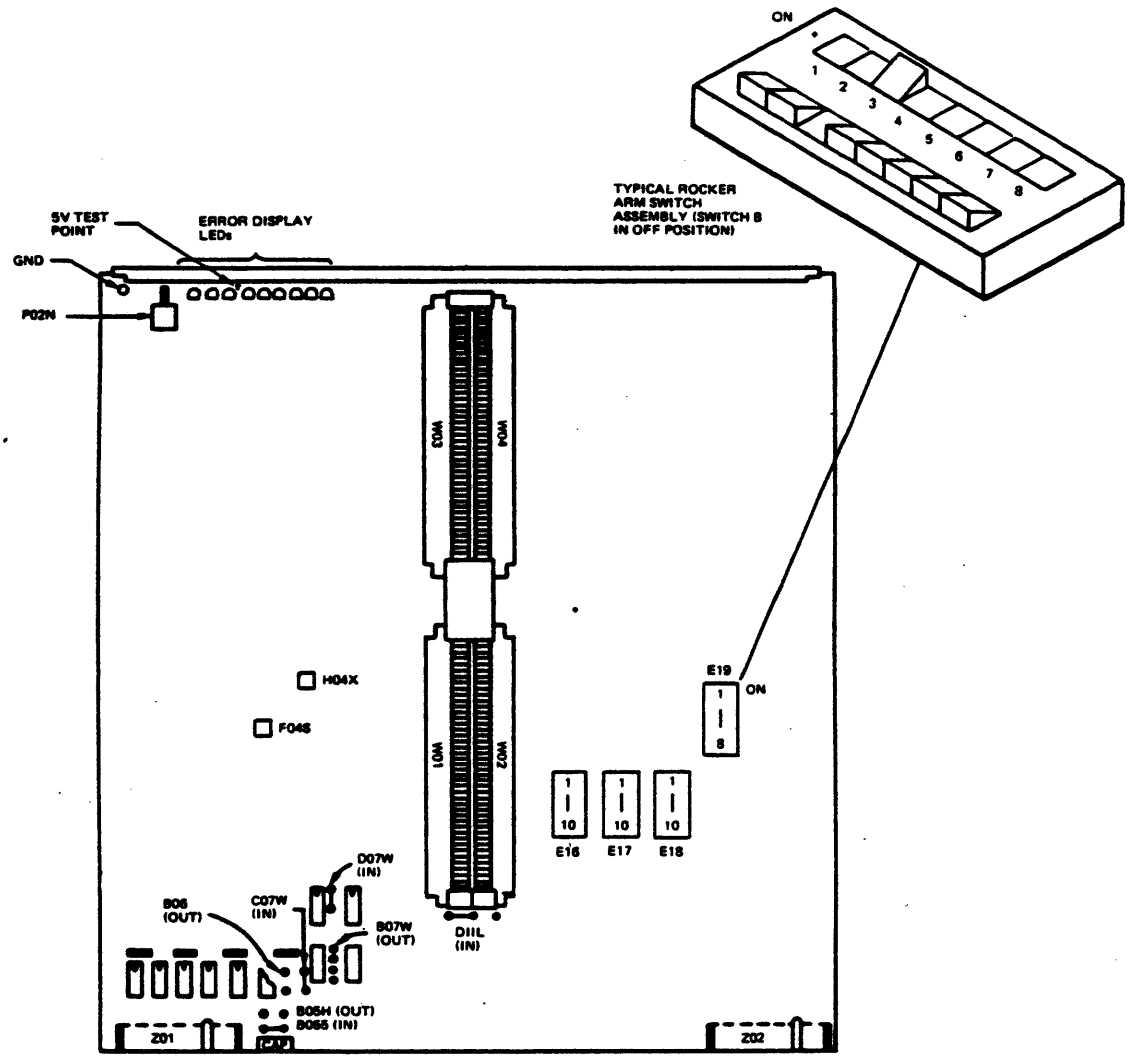


Figure 3-18 Switch and LED Indicator Locations (BF2MYE)

3.5.3.2.3 BF2MYE LED Indicators

Nine Light Emitting Diodes (LEDs) are located along the right-hand front edge of the BF2MYE board (see Figure 3-18). They are used to indicate a faulty Memory-Pac or a faulty memory chip on the Memory-Pac. The LEDs are divided into three groups (see Figure 3-19). They are designated D0, D1, and D2. Within the three groups, the LED on the left is the Most Significant Bit (MSB) and the LED on the right is the Least Significant Bit (LSB). The most significant group is D0 because it provides a binary indication of the faulty Memory-Pac. Groups D1 and D2 provide binary indications of faulty memory chips. Figure 3-20 provides the instructions necessary to locate a faulty component when the LEDs indicate a failure.

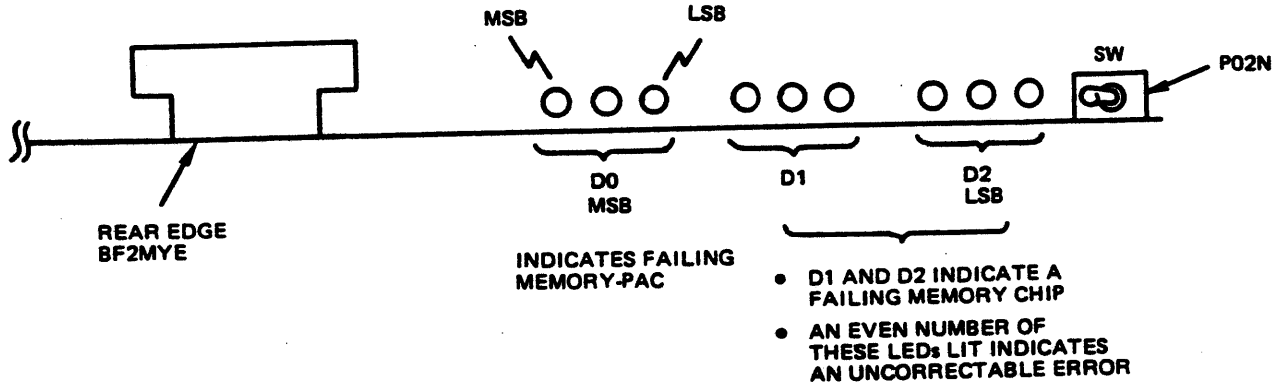


Figure 3-19 BF2MYE LED Indicator Identification

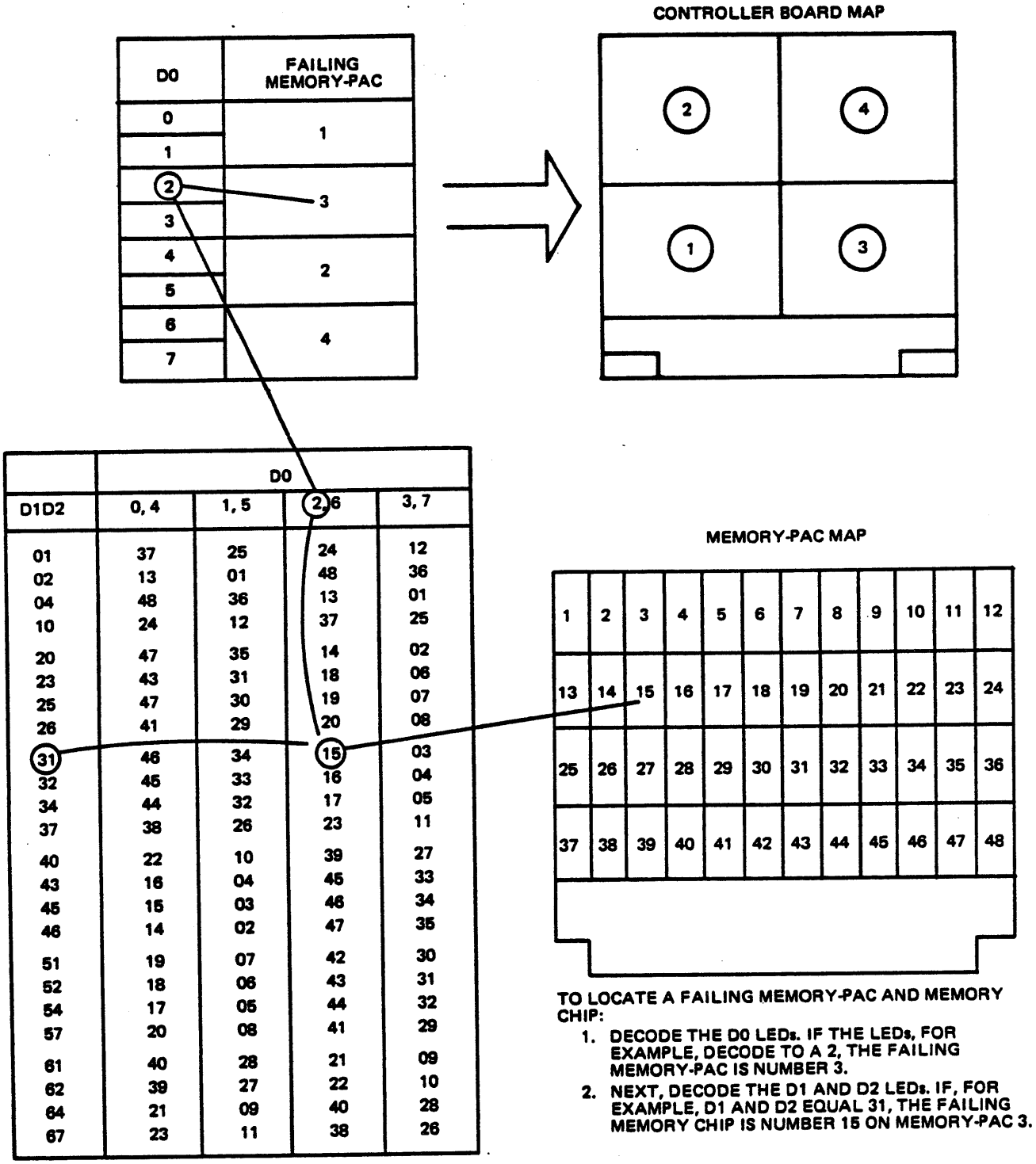


Figure 3-20 Locating Faulty Memory-Pac and Memory Chip (BF2MYE)

3.5.3.3 Rules for Memory Configuration

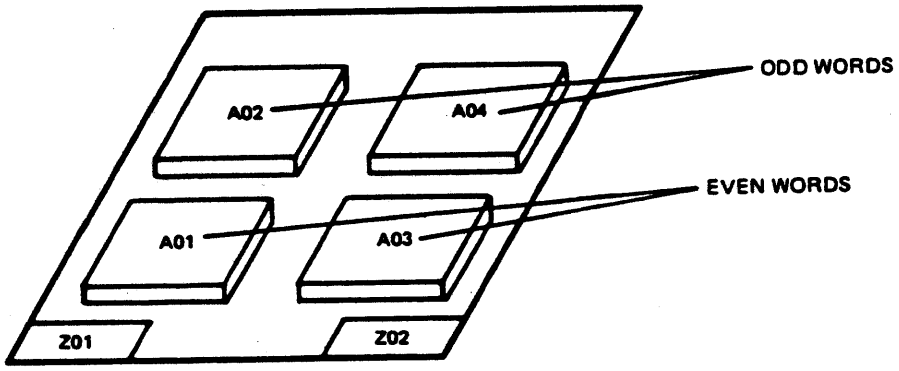
The memory configuration rules are:

1. The system memory can be configured as shown in Table 3-4.

Table 3-4 System Memory Configuration

CONTROLLER BOARDS	IPI	MEMORY-PAC	IPI	WORD CAPACITY PER BOARD
BF2MAE Single Word (slow)	BMMU011A	BS2TA8	BCMM038A	32K Words
BF2MCE Double Word (fast)	BMMU021A	BS2TC8	BCMM005A	32K Words
BF2MYE	BMMU031B	BS2SH8	BCMM048A	128K Words

2. Memory addressing is accomplishd by mounting the Memory-Pacs at specific locations on the memory controller boards (see Figure 3-21). The controller board/Memory-Pac combination must be as shown in Table 3-4. The units cannot be intermixed. If there are only two Memory-Pacs mounted on a controller board, one is the even address stack and the other is the odd address stack.



DOUBLE-WORD FETCH (BF2MCE)

A-01/A-02	ADDRESS LOCATIONS	0-16K
A-03/A-04	ADDRESS LOCATIONS	16K-32K

SINGLE-WORD FETCH (BF2MAE)

A-01	ADDRESS LOCATIONS	0-8K
A-02	ADDRESS LOCATIONS	8K-16K
A-03	ADDRESS LOCATIONS	16K-24K
A-04	ADDRESS LOCATIONS	24K-32K

Figure 3-21 Double and Single Word Fetch Memory Configuration

3.5.4 Page Control Unit (Pager)

The Page Control Unit (PCU) provides a mechanism for memory protection and for accessing up to 256K of optional memory. It is required on all systems that are configured with greater than 32K of memory.

3.5.4.1 PCU Description

The PCU option consists of a Page Control Logic Unit (PCLU) board, BF4PCL (IPI BPAG001A), and two Page Address Table Unit (PATU) boards, BD2PAT (IPI BPAT001A). One BD2PAT is installed on the CPU board (BF418A) and the other is on the IOM board (BF410B).

3.5.4.2 PCU Switch Settings

On the Level 2.1 (60132644) PCU, the hexadecimal rotary switch is set to 0 to enable the board and set to 4 to disable the board. For Level 2.2 (60132953) and above, the hexadecimal rotary switch is set to 0 and switch S01 is set to the left position to enable the pager and to the right position to disable the pager (see Figure 3-22).

3.5.4.3 PCU Installation and Cabling

Perform the following steps to install the PCU and the connecting cables:

WARNING

To avoid bodily injury, set the POWER switch on the control panel to the OFF (down) position. Ensure that the DC ON indicator on the control panel is not lit. Set the PDU circuit breaker to OFF. Disconnect the ac power cable from the system.

1. Install the PCU in the memory extension chassis according to the configuration rules in subsection 3.5.2 and Figure 3-14.

2. Disconnect the bus priority cable on CPU board B. Also disconnect the ribbon cable from the control panel on CPU board B.

3. Remove the CPU boards from the chassis as a pair. If cache is installed, remove the CPU/cache assembly.

4. Remove the PATN-PAC from CPU board A by loosening the connector screws.

5. Align the PAT-PAC with the connectors on the CPU board. Secure the PAT-PAC to the CPU board by tightening the connector screws.

6. Reinsert the CPU boards into the chassis.

7. Remove the IOM boards from the chassis.

8. Carefully remove the six side connectors on the two boards. Remove the screws at the corners of the boards that hold the boards together.

9. Remove the PATN-PAC from IOM board B.

10. Install a PAT-PAC on IOM board B.

11. Reassemble the IOM boards with the screws and standoffs at the corners of the boards. Reinsert the six side connectors.

12. Reinstall the IOM boards into the chassis.

13. Connect the bus priority cable from IOM board B to CPU board B. Connect the flat cable (60134476) from CPU board B to the control panel.

14. Connect two cables (60128601-003 and 60128601-004). One is from Y01 on the PCU to the PAT-PAC on the CPU (see Figure 3-22). Connect the other cable from Y02 on the PCU to the PAT-PAC on the IOM.

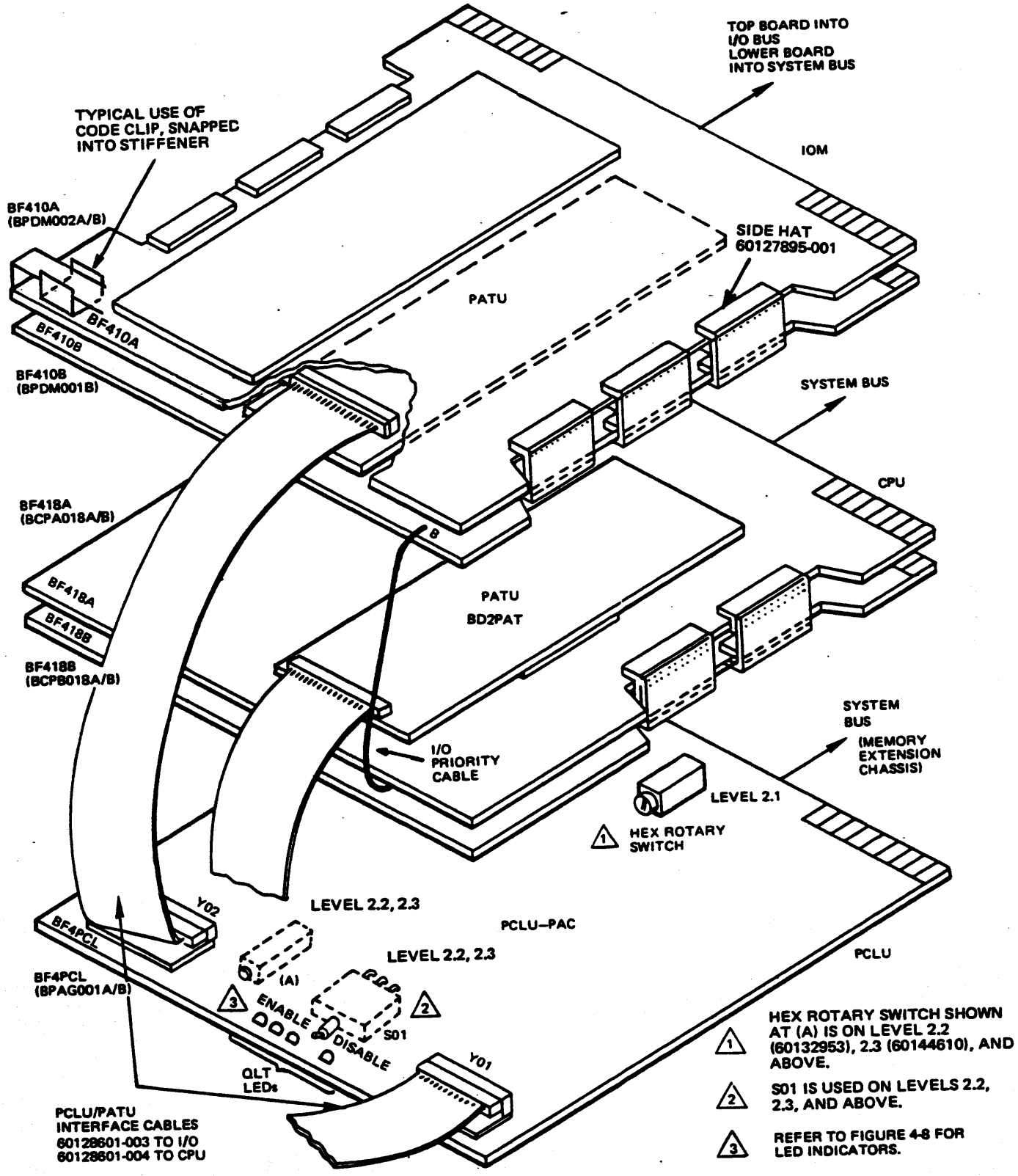


Figure 3-22 Page Control Unit Board Layouts

NOTES

3.5.5 Central Processor Unit

The Central Processor Unit (CPU) is a high-speed general purpose processor that operates in conjunction with other system units to meet a variety of communications applications, including front end processing.

3.5.5.1 CPU Description

The CPU is physically contained on a pair of full-size (15 by 16 inch) processor boards plus two smaller adapter boards that are attached to the processor boards (see Figure 3-23). The lower full-size processor board (BF418B), hereafter called the CPU-B board, has a half-size (7.5 by 11.5 inch) PROM adapter board (BH2PRK) attached to it. The upper full-size processor board (BF418A), hereafter called the CPU-A board, has one of two possible quarter-size (3.5 by 11.5 inch) adapter boards attached to it. If the system is configured with the paging option, a Page Address Table Unit (PATU) quarter-size adapter board (BD2PAT) is mounted on the CPU-A board. If the option is not configured into the system, a PATU NOT quarter-size adapter board (B2PATN) is installed on the CPU-A board instead.

3.5.5.2 Operator Control Panel

The system has a self-contained control panel (see Figure 1-6). Two etched boards are mounted behind the panel. The control panel provides a means for initializing the system, starting/stopping the CPU, entering and displaying registers and memory, single stepping a program, booting a program, master clearing the system, and indicating CPU routines. A ribbon cable connects the control panel to the CPU.

3.5.5.3 Operator Control Panel Installation and Cabling

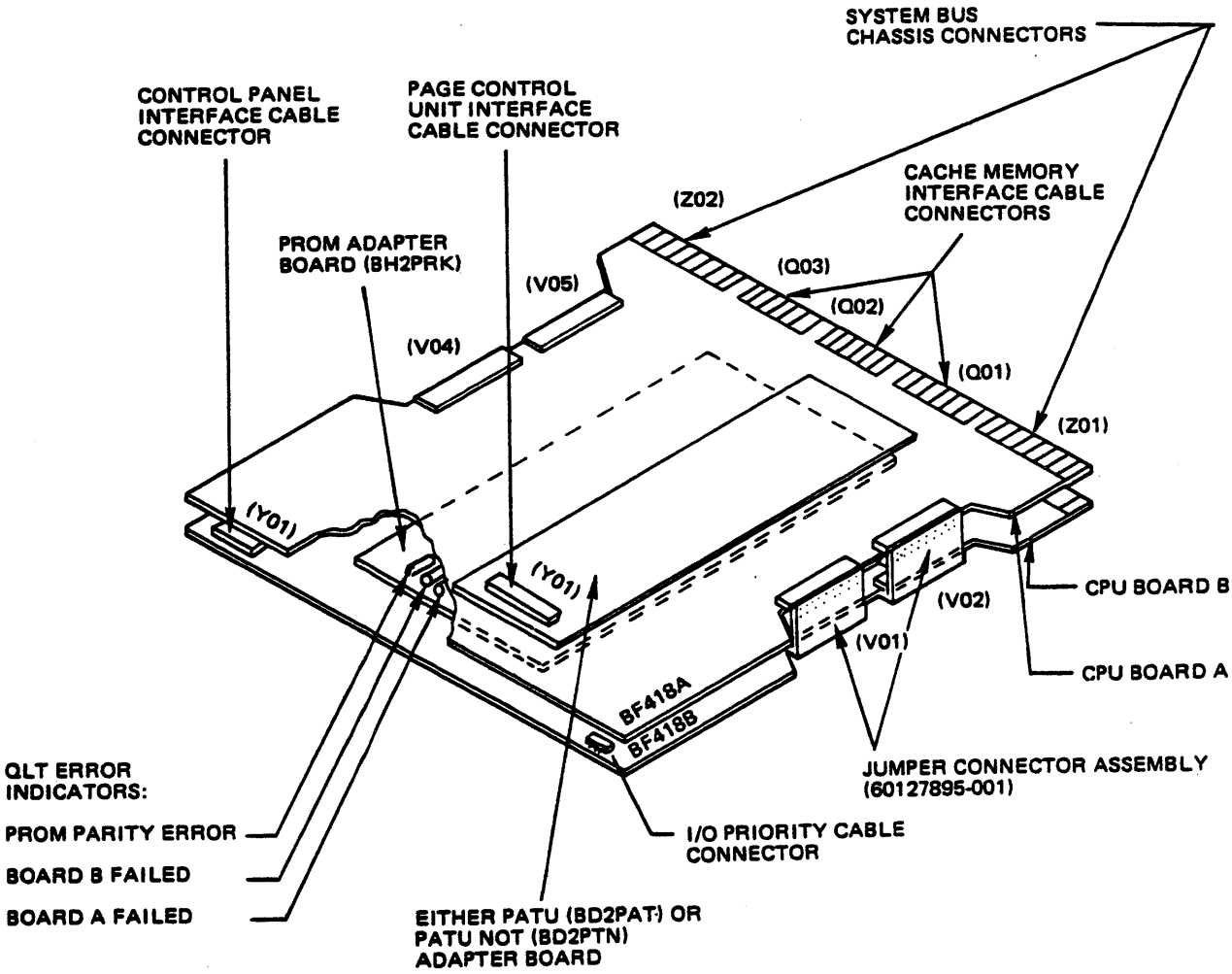
The control panel is installed and cabled at the factory. The following procedure for cabling the control panel is for reference only:

1. Open the control panel by inserting a 6-mm allen key into the key fitting on the latch and press inward (see Figure 3-24). The control panel release latch will disengage and the panel will open. Remove the allen key from the release latch and swing the panel away from the cabinet and to the left.

2. Connect the prefolded ribbon cable (60134476) from Y01 on the CPU-B board to Y01 and Y02 at the control panel board (see Figure 3-24). The cable has two connectors on one end, labelled A (Y02) and B (Y01).

3. Connect the three-pin and four-pin connectors from the system cabinet to connectors Q1AJ-01 and Q1AJ-02, respectively.

4. Route all cables through the tie-wraps and/or cable clamps inside the control panel.



- BF418A = IPI BCPA018A/B.
- BF418B = IPI BCPB018A/B.
- BH2PRK = IPI BPRK001A IF MEMORY TYPE IS BF2MCE, BF2MYE
  OR IPI BPRK003A IF MEMORY TYPE IS BF2MAE.
- BD2PAT = IPI BPAT001A IF PAGER IS INSTALLED
  OR IPI BPAT002A IF PAGER IS NOT INSTALLED.

Figure 3-23 CPU Board Layout

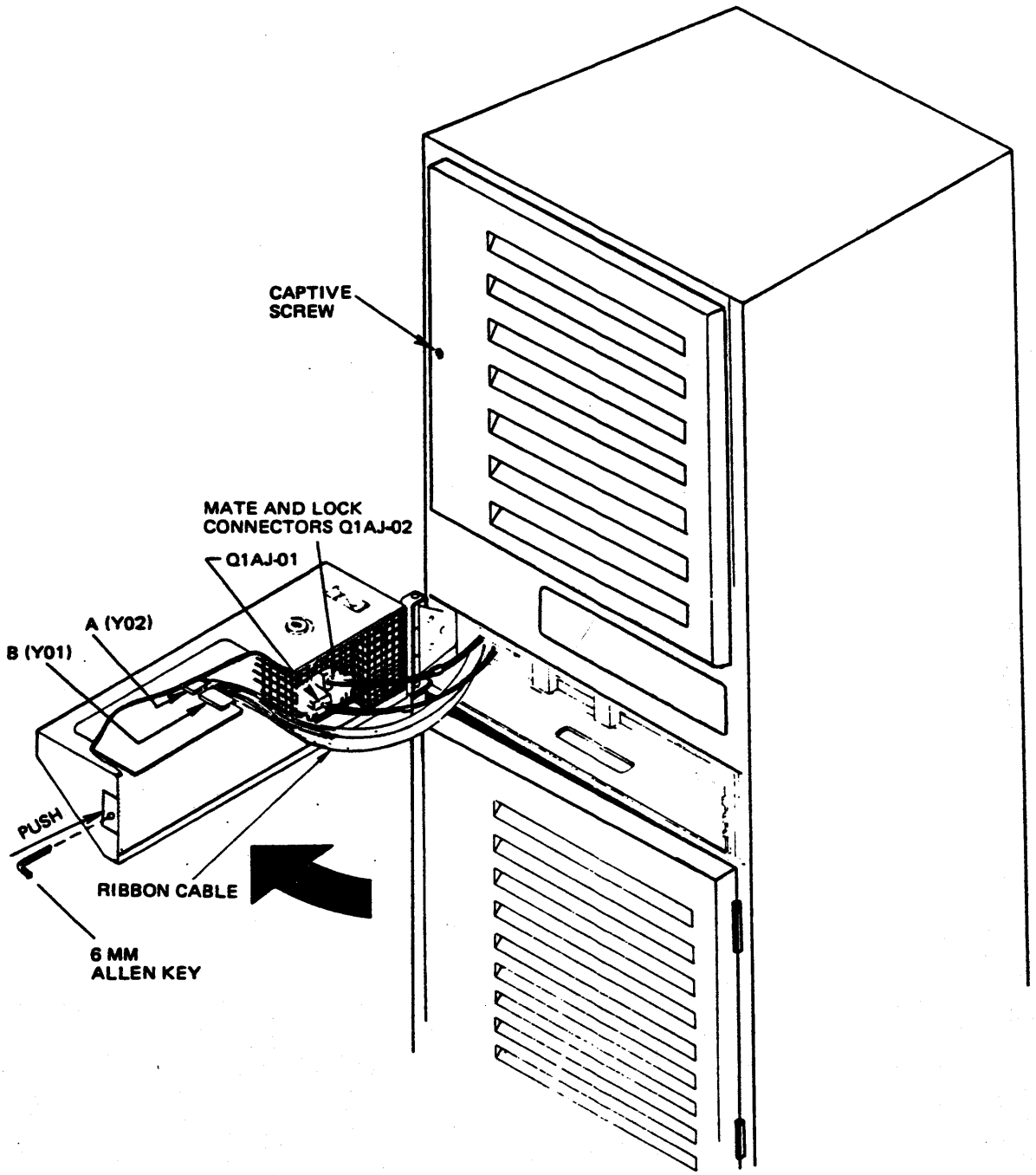


Figure 3-24 Operator Control Panel Installation

3.5.6 Cache Memory

The cache memory unit, hereafter referred to as the cache, enhances the system CPU performance by providing a hierarchical memory subsystem.

3.5.6.1 Cache Memory Description

The cache consists of a cache memory board (BG4CHE) that is physically mounted piggyback style on the cache control board (BF4CHE/BF415C) by four 25-pin stacking connectors (see Figure 3-25).

3.5.6.2 Cache Installation and Cabling

To install the cache, proceed as follows:

WARNING

To avoid bodily injury, set the POWER switch on the control panel to the OFF (down) position. Ensure that the DC ON indicator on the control panel is not lit. Set the PDU circuit breaker to OFF. Disconnect the ac power cable to the system.

1. The cache board is located above the CPU-A board in the system cabinet and is connected to the CPU by three cable assemblies.

2. Figure 3-25 shows the location of the three contact areas for the cache/CPU connection. Figure 3-26 shows one of the three cable assemblies (60128613) that connects the CPU and the cache. Figure 3-26 also shows how the boards are located in relation to each other.

CAUTION

When cabling the CPU and cache together, keep the the boards separated (e.g., with a piece of cardboard) so that the components on the CPU board do not damage the etch side of the cache.

3. When installing a CPU/cache assembly, the three boards must be carefully placed in the proper slots in the basic chassis and must be pushed into the chassis simultaneously.

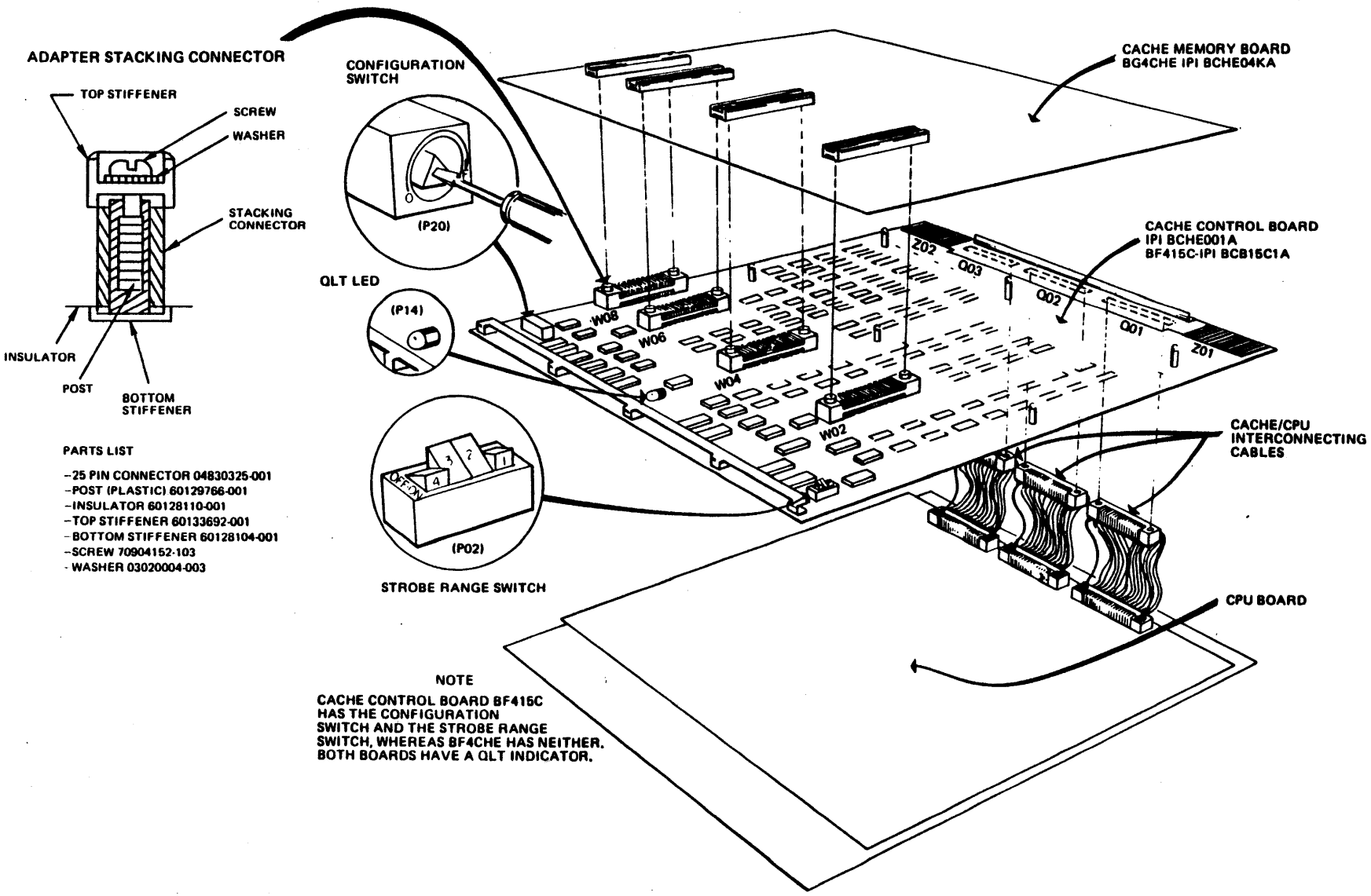


Figure 3-25 Cache Memory Unit Board Layout

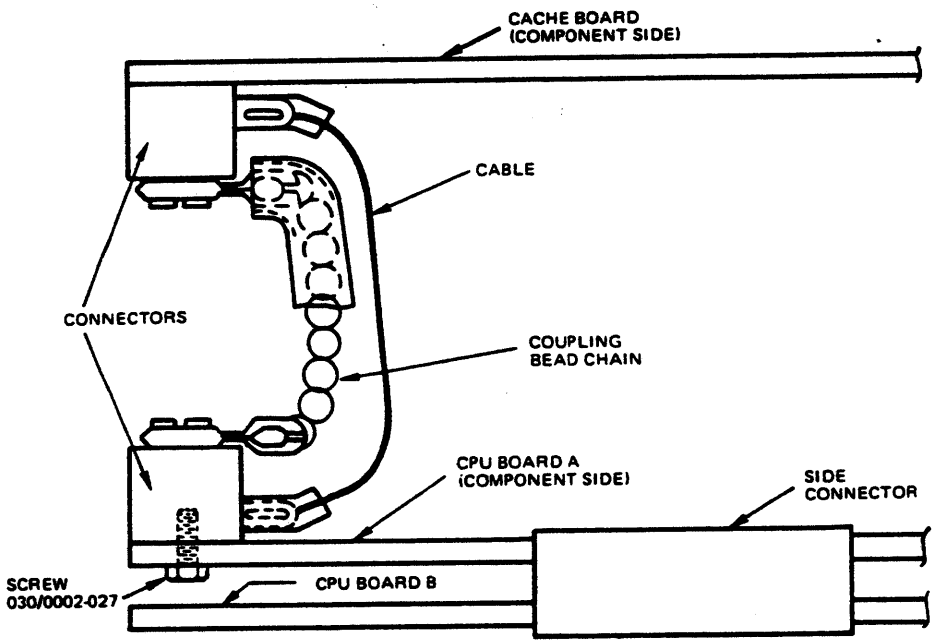


Figure 3-26 CPU/Cache Cable Assembly

3.5.6.3 Cache Switch Settings

The cache control board (BF415C) contains two switches, which are located as shown in Figure 3-25. The operation and settings of the switches are described in the following paragraphs.

Configuration Switch

The configuration switch is a 16-position rotary switch that defines the cache channel number. The configuration switch is normally in position hexadecimal 8 (channel ID 0080 hexadecimal).

Configuration Switch Settings

ROTARY SWITCH SETTING (HEX)	CACHE CHANNEL ID (HEX)
0 ↓ 7	Not Applicable
8 9 A	0080 00C0 0080 or 00C0
B ↓ F	Reserved for Future Use

Strobe Range Switch

The strobe range switch consists of four rocker arm switches and is provided for the adjustment of cache hits (cache data address compares). The strobe range switch must always have its section 4 (rocker arm) switch in the ON position, with a strobe range of 50 nanoseconds; sections 1 through 3 must always be in the OFF position.

3.5.7 Input/Output Multiplexer

The Input/Output Multiplexer (IOM) provides a path for data and control information between components attached to the system bus such as main storage units or CPUs and a wide variety of equipment, including peripherals, real-time devices, and other computers attached via I/O channels on the input/output bus.

3.5.7.1 IOM Description

The basic system is housed in a special (dual bus) 10.5-inch (10-board) chassis; the upper half is the I/O bus and the lower half is the system bus (see Figure 1-3). The two buses are connected through two full-size IOM printed circuit boards (IOM-A and IOM-B). The IOM-A board plugs into the I/O bus (card slot 11); the IOM-B board plugs into the system bus (card slot 9). The IOM is the only logic unit that plugs into both buses.

Physically, the IOM consists of the IOM-A board, the IOM-B board, a Page Address Table-Pac (PAT-PAC), a Programmable Read Only Memory (PROM-PAC), and six jumper-connector assemblies. The factory loaded PROM-PAC is mounted on the IOM-A board. A PAT-PAC (Page Address Table -- Optional) or a $\overline{\text{PAT}}$-PAC (Page Address Table -- Standard) is mounted on the IOM-B board. The PAT-PAC is used when the PAT option is installed; otherwise, the $\overline{\text{PAT}}$-PAC is used.

3.5.7.2 IOM Installation and Cabling

The IOM follows the same rules as the CPU with the exception that the PROM-PAC is mounted on the upper (IOM-A) board and the PAT-PAC or PATN-PAC is mounted on the lower (IOM-B) board (see Figure 3-27).

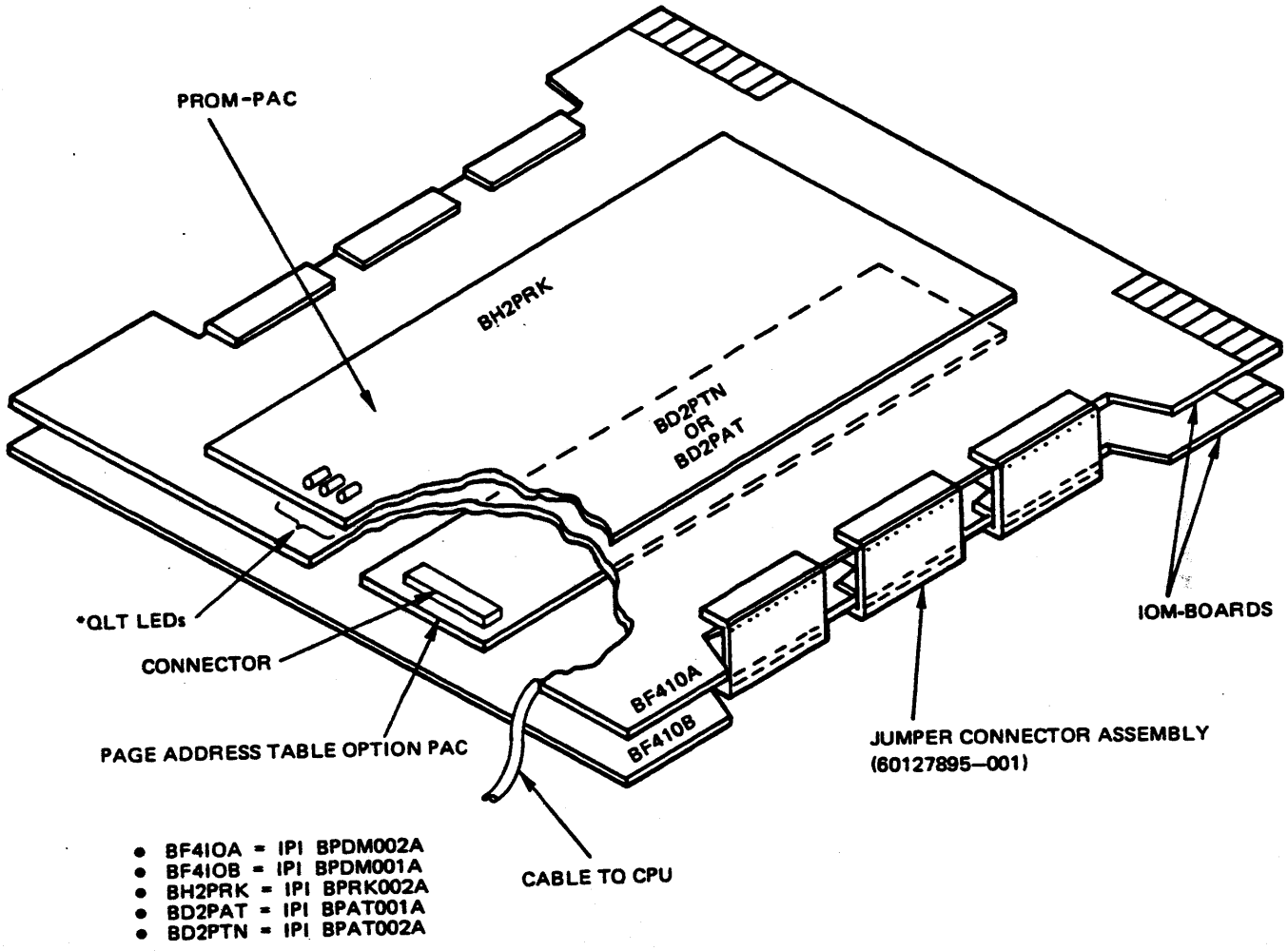


Figure 3-27 IOM Board Layout

3.5.8 Peripheral Interface Adapter

The Peripheral Interface Adapter (PIA) provides the interface between the system I/O Multiplexer (IOM) and the L66 Disk Micro-programmed Controller (MPC).

3.5.8.1 PIA Description

Each PIA consists of a 15-inch by 16-inch controller board (BF4PIA) to which a full-size PIA Interface-Pac (BG4PID) is attached by eight stacking connectors (see Figure 3-28).

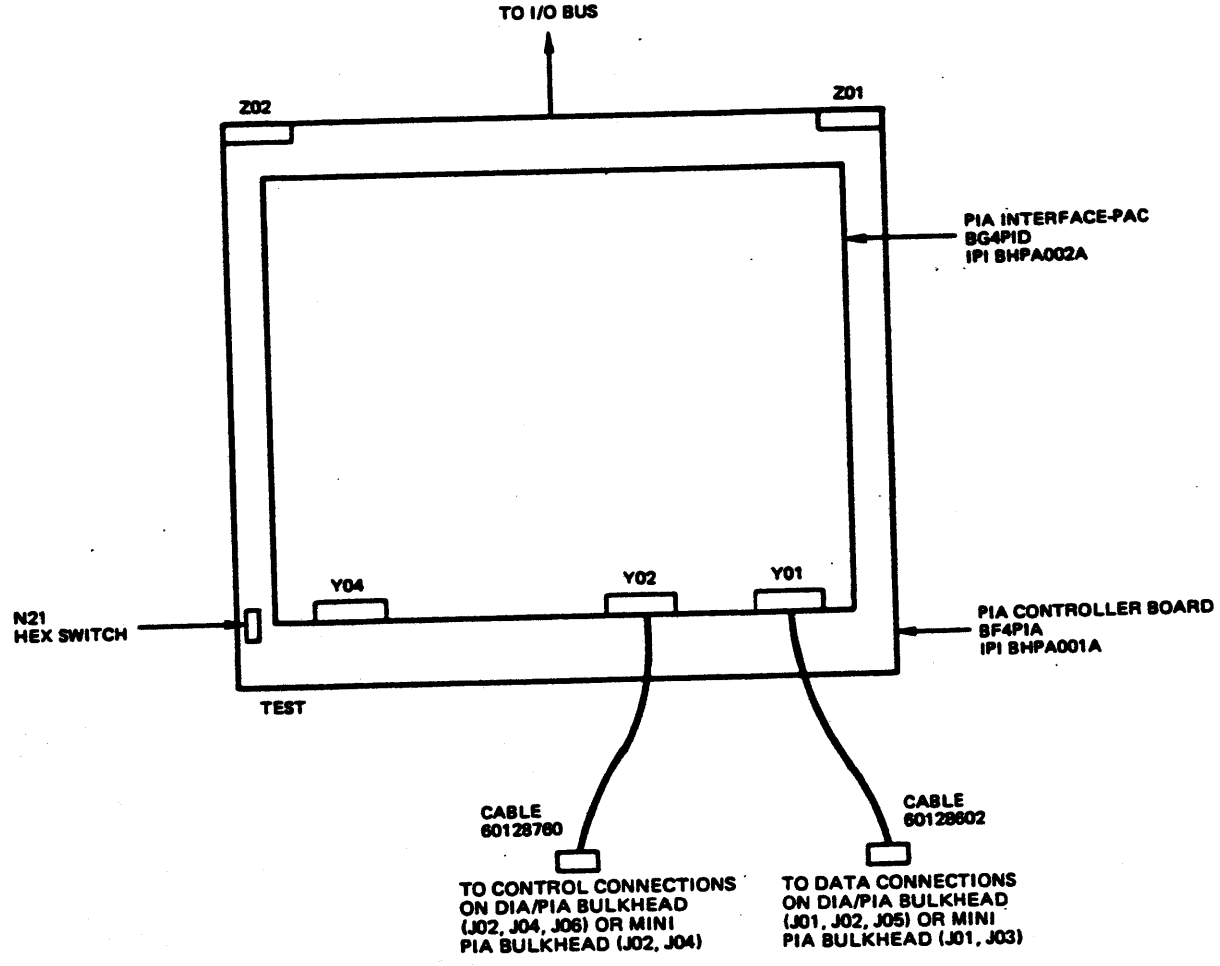


Figure 3-28 PIA Board Layout and Cable Connections

3.5.8.2 PIA Switch Settings

The hexadecimal rotary switch for the PIA is located at N21. The first PIA is usually set for channel number 03 and the second PIA is set for channel number 05.

3.5.8.3 PIA to L66 MPC Interface Panel

To connect the PIA to the L66 MPC interface panel, proceed as follows:

1. Run the two L66 MPC interface cables (43C240327) from the L66 MPC interface panel (see Figure 3-29) to the system cabinet. Pass the cables through the cutout at the bottom of the cabinet.

2. Connect the cable from J1A on the MPC interface panel to J02 on the DIA/PIA bulkhead or Mini PIA bulkhead (see Figures 3-30 and 3-31). Connect the other cable from J1B to J01.

NOTES

1. At the MPC, the PIA can be connected to one of four possible places (see Figure 3-29): LA0 port 0 or port 1 and LA1 port 0 or port 1, depending on the configuration. Each pair of plugs is labelled J1A and J1B, and J2A and J2B.

2. If the optional PIA is being installed, connect the cables as specified above, but use J03 and J04 on the DIA/PIA or Mini PIA bulkhead and one of the unused ports in Note 1.

3.5.8.4 PIA to L66 MPC Interface Lines

Figure 3-32 shows the PIA to L66 MPC interface signals.

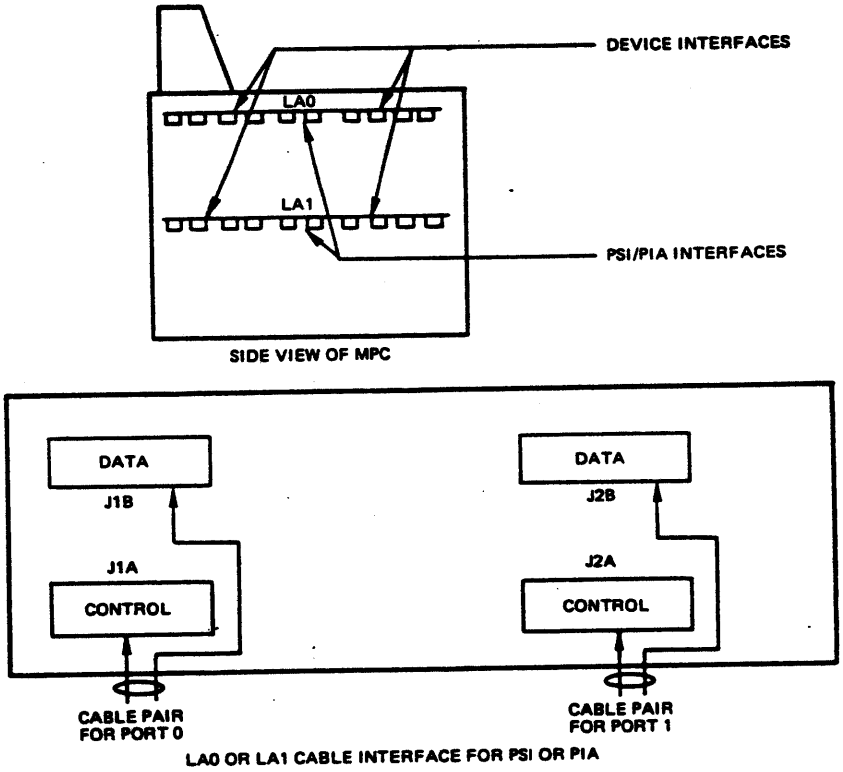


Figure 3-29 PIA/MPC Interface Panel

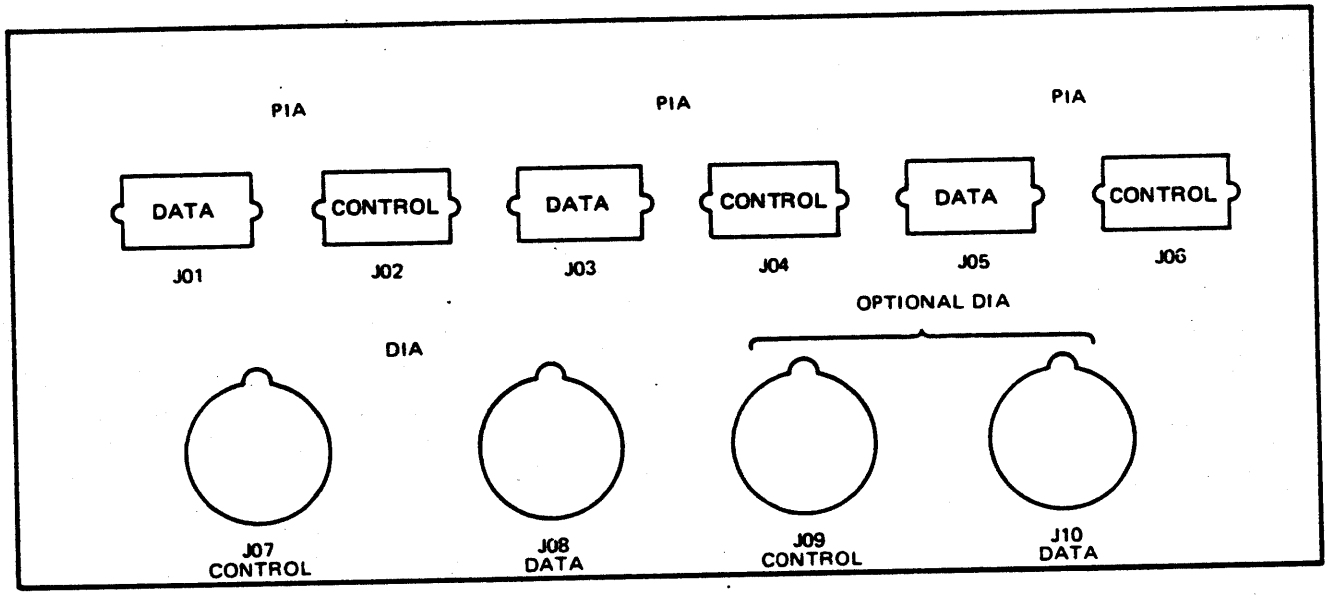


Figure 3-30 System DIA/PIA Bulkhead

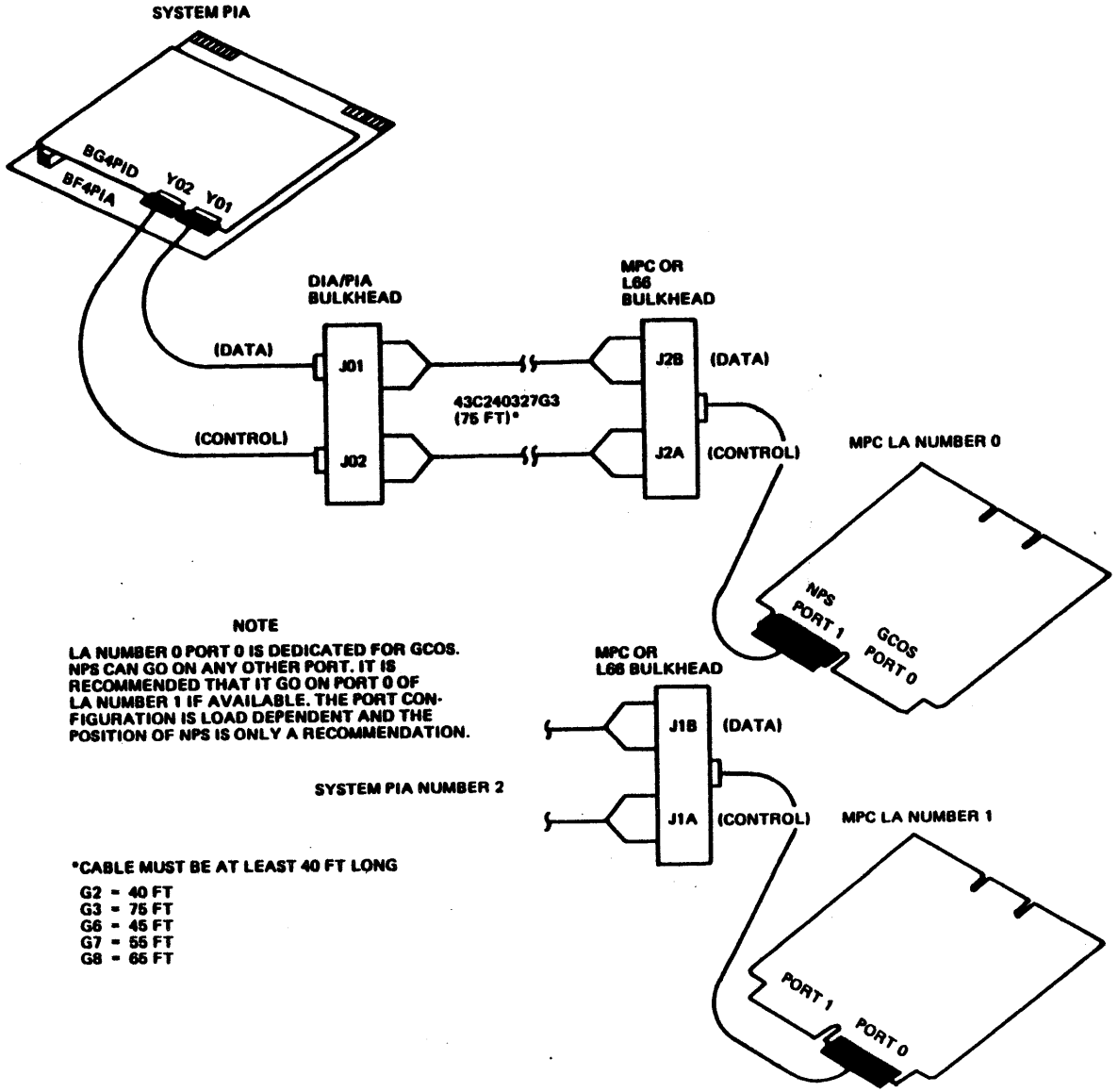


Figure 3-31 System PIA to MPC or L66 Cabling

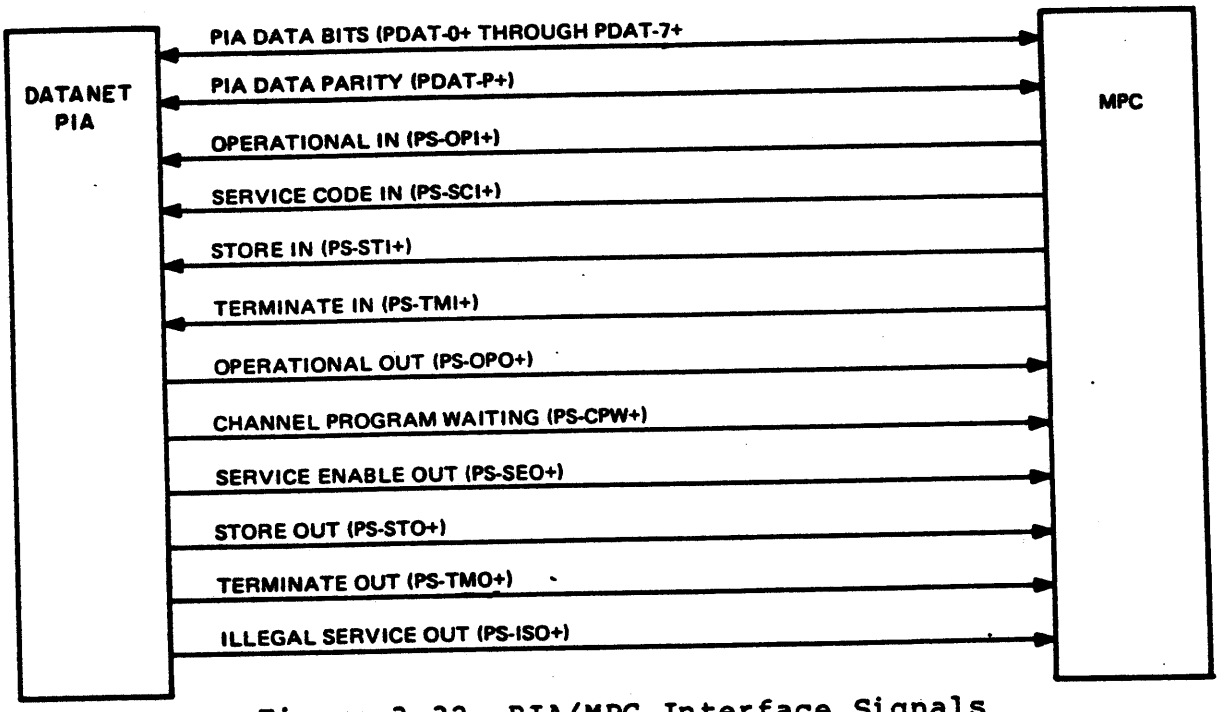


Figure 3-32 PIA/MPC Interface Signals

3.5.8.5 Definition of PIA/MPC Interface Lines

The PIA/MPC lines are:

1. PIA Data Bits (PDAT-0 through PDAT-7): These eight lines constitute an 8-bit byte of information transfer between the PIA and the MPC.

2. PIA Data Parity (PDAT-P): This is the parity signal for PIA/MPC transfers.

3. Operational In* (PS-OPI): When True, it indicates that the MPC is operational. If the MPC is not operational, OPI causes a power-off sequence.

4. Service Code In (PS-SCI): When True, it indicates that the MPC is requesting permission to issue a service code to the PIA.

5. Store In (PS-STI): When True, it indicates that data for the PIA is on the bus.

6. Terminate In (PS-TMI): When True, it indicates to the PIA that it received the last character of the transaction from the MPC.

7. Operational Out (PS-OPO): When True, it indicates to the MPC that the PIA is operational.

*In = from the MPC to the PIA.

8. Channel Program Waiting (PS-CPW): It notifies the MPC that the Connect I/O command was completed and MPC intervention is required for the next operation.

9. Service Enable Out (PS-SEO): When True, it indicates that the PIA acknowledged the service request by the MPC.

10. Store Out (PS-STO): When True, the PIA indicates to the MPC that it took the data from the bidirectional bus.

11. Terminate Out (PS-TMO): When True, it indicates that the PIA received the last character of a transaction.

12. Illegal Service Out (PS-ISO): When True, it indicates that the PIA is issuing a fault cycle request.

NOTE

For the various other interfaces between the controller boards and related Adapter-Pacs of the system, refer to the specific product manuals listed in subsection 1.2.

3.5.8.6 Cabling PIA to DIA/PIA Bulkhead or Mini PIA Bulkhead

To connect the PIA to the DIA/PIA bulkhead or Mini PIA bulkhead (see Figure 3-28), proceed as follows:

CAUTION

Ensure that the PIA interface cables are connected properly or damage to the PIA Interface-Pac will result. For the PIA cable signals, refer to Tables 3-5 and 3-6.

1. Connect the data cable (60128602) to Y01 on the PIA Interface-Pac. Dress the cable to the right of the cabinet and pass it between the cover and the chassis and connect the other end to J01 on the DIA/PIA or Mini PIA bulkhead.

2. Connect the control cable (60128760) to Y02 on the PIA Interface-Pac. Dress the cable to the left of the cabinet and pass it between the cover and the chassis and connect the other end to J02 on the DIA/PIA or Mini PIA bulkhead.

Table 3-5 PIA Data Cable Signals (60128602)

Y01 PINS	SIGNAL	J01 PINS
19	PDAT-0+	0A
11	PDAT-1+	0B
17	PDAT-2+	0C
09	PDAT-3+	0D
15	PDAT-4+	0E
07	PDAT-5+	0F
13	PDAT-6+	0H
05	PDAT-7+	0J
21	PDAT-P+	0K

Table 3-6 PIA Control Cable Signals (60128760)

Y01 PINS	SIGNAL	J02 PINS
09	PS-RSO+	0A
10	PS-OPI+	0H
11	PS-OPO+	0F
12	PS-SCI+	0J
13	PS-CPW+	0B
14	PS-STI+	0K
15	PS-SEO+	0L
16	PS-TMI+	0M
17	PS-TMO+	0E
18	PS-REI+	0R
19	PS-STO+	0D
21	PS-ISO+	0C
22	PS-MTO+	0N

3.5.9 System Support Channel

The System Support Channel, SSC (BF4SSC), contains the hardware common to all device adapters (Device-Pacs). The SSC and the device-specific firmware are on a Device-Pac (BD2SSC) called the SSC Microprogram Control Store (μPCS). The μPCS occupies one position on the SSC, which has three other adapter positions for device attachment. Device adapters consist of a single- or a double-size module. A single-size module (console adapter) occupies one adapter position. A double-size module (diskette adapter) occupies two adapter positions.

3.5.9.1 SSC Description

The SSC is a solid-state module that consists of Dual In-Line Packages (DIPs) mounted on a multilayer system controller. The SSC has eight 25-pin, in-line connectors for mounting the device adapters and two 50-pin connectors for connecting the SSC to the I/O bus. The SSC supports the three required Adapter-Pacs. They are the console, the diskette, and the PROM Adapter-Pacs (see Figure 3-33).

3.5.9.2 SSC Switch Settings

On the BF4SSC board, the switch at location G19 must be set to C and the switch at location G20 to 8. This generates addresses 00 for the console, 01 for the diskette, and 40 for the wraparound channel (see Figure 3-33). On the console adapter, the baud rate switch in location B02 is set to position 3 for 110 bps (DCF6608) or to position 9 for 1200 bps (DCF6606), see Table 3-7.

Table 3-7 Console Baud Rate Switch Position

HEXADECIMAL ROTARY SWITCH POSITION	BAUD RATE SELECTED	HEXADECIMAL ROTARY SWITCH POSITION	BAUD RATE SELECTED
0	Not Used	8	900
1	50	9**	1200
2	75	A	1800
3*	110	B	2400
4	134.5	C	3600
5	150	D	4800
6	300	E	7200
7	600	F	9600

*KSR-33 Teletype (DCF6608).
**Heavy-Duty 120 cps Typewriter (DCF6606).

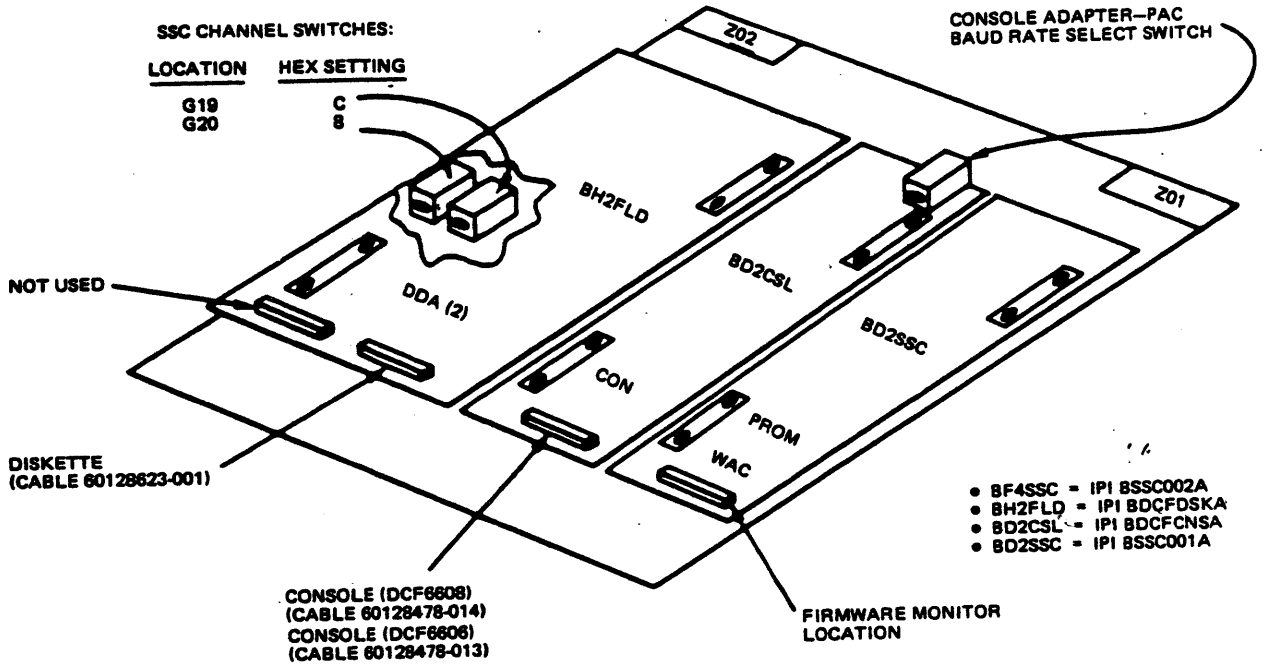


Figure 3-33 SSC Switch Settings

3.5.9.3 Diskette Installation and Cabling

The diskette unit is installed and cabled at the factory; therefore, the following is for information only.

NOTE

The ac power cord from the diskette power supply must always be plugged into the filtered receptacle (J07) of the power distribution unit (see Figure 3-9).

The unit is secured to the system cabinet by four screws on the diskette unit front panel and by four screws at the back of the diskette chassis. The diskette assembly and the rack-mounted tray assembly are shown in Figure 3-34. Table 3-8 lists the major components.

Cable 60138623-001 connects J02 on the diskette assembly with Y01 on the Diskette Adapter-Pac on the SSC board.

CAUTION

Remove the diskette from unit before powering down or its programs may be erased.

WARNING

To avoid bodily injury, set the ac power switch to OFF, set PDU circuit breaker to OFF, and disconnect the ac power source to the system before removing the diskette unit from the cabinet.

To connect or remove the cable from J02, remove all the screws at the front and back of the diskette and pull the unit forward.

NOTE

It may be necessary to loosen the screws on the blank spacer above the diskette unit to pull the diskette unit forward.

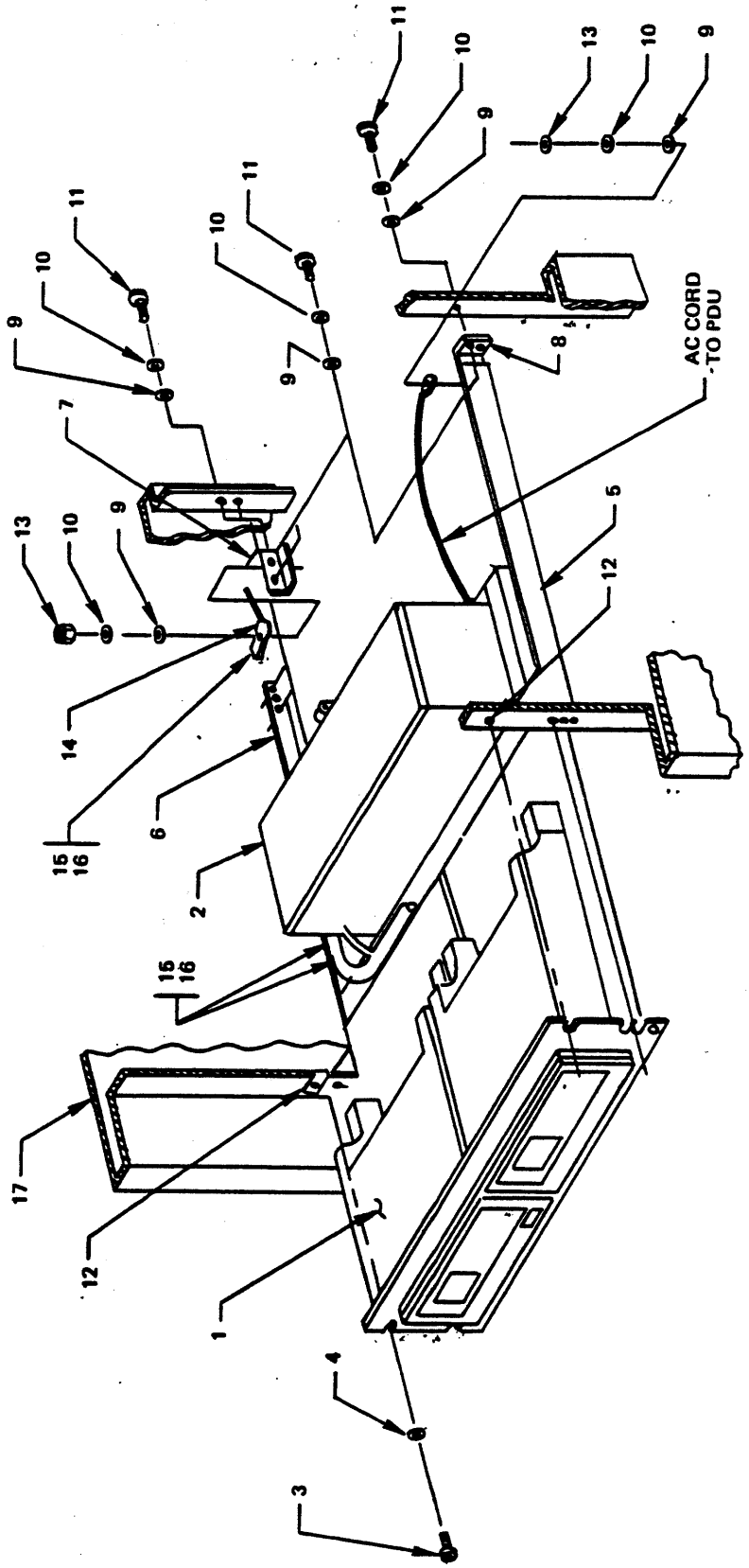


Figure 3-34 Diskette Tray Assembly (Refer to Table 3-8)

Table 3-8 Diskette Tray Assembly Parts List (See Figure 3-34)

ITEM NUMBER	PART NUMBER	TITLE	QUANTITY
1	60128287-024	Diskette Assy	Ref
2	60128259-003	Diskette Power Supply	Ref
3	03010155-026	Screw, Cap, Skt, Butn	4
4	03020038-005	Washer, Flat	4
5	60128307-001	Side Bracket Assy	1
6	60128307-002	Side Bracket Assy	1
7	60128301-001	Support Bracket	1
8	60128301-002	Support Bracket	1
9	03020001-051	Washer, Flat, 10	8
10	03020003-005	Washer, Lock, 10	8
11	03010002-059	Screw, PH, 10	8
12	70901402-001	Nut, Sheet Spring, Fltg	2
13	03030001-006	Nut, Plain, Hex, 10	2
14	03510002-004	Clamp, Copper	2
15	60128523-001	Device Cable, 6-ft	Ref
16	60128523-002	Device Cable, 12-ft	Ref
17	--	Cabinet Assy	Ref

3.5.9.4 Console Installation and Switch Settings

The system can have eiher a KSR-33 Teletype console (DCF6608) or a heavy-duty 120 characters-per-second typewriter console (DCF6606), required for NPS software. Subsections 3.5.9.6 and 3.5.9.7 provide modification procedures (where applicable) and cabling procedures for these devices.

3.5.9.5 SSC Formatted Console Dump

After the console installation is completed, it can be checked by performing the following steps:

1. Type in a ? (question mark) on the console.

2. Compare the printout with the SSC Formatted Console Dump, Figure 3-35.

3. The printer may be stopped before the normal completion of the console dump by pressing the BRK push button.

4. If an SSC Formatted Console Dump is not obtained, check the console, cable, console adapter board, the setting of the console baud rate switch, and boards BD2SSC and BF4SSC. No other boards in the system are used for this dump.

Figure 3-36 shows the Scratchpad Memory (SPM) map for the SSC dump format; Figure 3-37 shows the SSC SPM miscellaneous byte definitions.

ACU	000	BDR	000	000	000	000	000	ACU – ACCUMULATOR BDR – BUS DATA REGISTER
AD0	13F	11C	180	121				ADAPTER 0 (DATA, DEV ID, STA1, STA2)
AD1	10F	110	120	120				ADAPTER 1 (DATA, DEV ID, STA1, STA2)
AD2	10F	110	180	180				ADAPTER 2 (DATA, DEV ID, STA1, STA2)
AD3	1FF	1FF	1FF	1FF				ADAPTER 3 (DATA, DEV ID, STA1, STA2)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
00	000	011	033	000	000	080	000	000	066	002	040	062	002	040	060	000	CHANNEL 0 CON PORT 0
10	101	102	000	000	000	000	000	000	180	000	040	040	000	000	020	000	
20	000	000	000	000	000	000	11C	022	133	133	131	000	027	000	000	000	
30	042	000	028	000	000	000	033	070	102	100	001	181	000	000	13E	031	
40	000	000	033	000	000	080	000	000	06E	002	040	06A	002	040	000	000	NOT USED PORT 1
50	111	112	000	000	000	000	000	000	000	000	000	000	000	000	000	000	
60	000	000	000	000	000	000	110	022	000	000	000	000	000	000	000	000	
70	001	000	000	000	000	000	000	000	000	000	007	000	000	000	000	120	
80	000	000	033	000	000	080	000	000	06E	002	040	06A	002	040	000	000	DISKETTE PORT 2 CHANNEL
90	111	112	000	000	000	000	030	000	104	020	040	040	181	000	000	000	
A0	100	000	000	000	000	000	110	022	000	000	000	000	000	000	000	000	
B0	000	000	0ED	070	000	000	073	070	112	100	080	141	141	105	000	000	
C0	000	000	007	000	000	080	000	000	022	075	040	000	000	000	044	000	CHANNEL 10 WAC PORT 3
D0	1E2	1E1	161	162	09E	008	000	000	000	000	040	040	000	000	000	000	
E0	12E	053	000	000	000	000	1FF	022	026	075	040	000	000	000	000	000	
F0	0FC	0FC	1FF	077	000	000	007	078	1E2	100	077	06A	000	000	000	00F	

CHANNEL NUMBER EXAMPLE:
USING WAC SPM QUADRANT
LOCATION F7, F6 = 0XX HEX, 0XX HEX
[0111 1000] [0000 0111]
[7 4 0] [0 7]

CHANNEL NUMBERS:
7 00 = CON
7 01 = DDA, CRD, CASS
7 40 = WAC
7 41 = CASS

CHAN NO. OF CIOC | FC OF CIOC

DEVICE ID EXAMPLE:
USING DDA SPM QUADRANT
LOCATION A7 = 22 HEX SET BY SSC F/W
LOCATION A6 = 10 HEX

DEVICE IDs:
CONSOLE = 1C (LCSP) & 18 (KSR)
CARD READER = 08 HEX
CASSETTE = 28 HEX
WAC = FF HEX
DISKETTE = 10 HEX

Figure 3-35 SSC Formatted Console Dump

ACU – ACCUMULATOR BDR – BUS DATA REGISTER

AD0-3 – ADAPTERS 0–3 (DATA, DEV ID, STA1, STA2)

WILL BE IFF HEX IF NO DEVICE

0	1	2	3	4	5	6	7

8	9	A	B	C	D	E	F

CON

CWD 1	CWD 2	SFC 1	SFC 2	ILC 1	ILC 2	TSK 1*	TSK 2*	0
CNF 1*	CNF 2*	CNF 3*	CNF 4*	CNF 5*	CNF 6*	RFU	RFU	1
DTA 3	DTA 4	DTA 5	DTA 6	DTA 7	DTA 8	DID 1*	DID 2	2
EXW 1*	EXW 2*	PCW 1*	PCW 2*	PCW 3*	PCW 4*	CHN 1	CHN 2	3

ADR 1	ADR 2	ADR 3	STA 1	STA 2	STA 3	DMA 1	MON 1
STS 1*	STS 2*	ERR 1	ERR 2	STS 3*	STS 4*	DTA 1	DTA 2
ADR 4	ADR 5	ADR 6	–	RNG 3	RNG 4	CRC R	CRC W
IDF 1	IDF 2	WL 01	WL 02	WL 03	SV RT	TEMP	SIGN

*DEVICE SPECIFIC LOCATION (REFER TO APPROPRIATE MANUAL). FOR CONSOLE, REFER TO THE SCC CONSOLE ADAPTER MANUAL (ORDER NO. FM73, PAGE 3-4). REFER TO SUBSECTION 1.2 OF THIS MANUAL FOR ALL MANUAL ORDER NUMBERS.

DDA

								4
								5
								6
								7

DDA FOR DISKETTE, REFER TO THE SSC DISKETTE ADAPTER MANUAL (ORDER NO. FN26, PAGES 3-2 AND 3-3).

								8
								9
								A
								B

WAC FOR WRAPAROUND CHANNEL, REFER TO THE SYSTEM SUPPORT CHANNEL MANUAL (ORDER NO. FM47, SECTION IV).

								C
								D
								E
								F

FOR A DEFINITION OF TERMS AND DESCRIPTION OF SPM WORD, REFER TO THE SYSTEM SUPPORT CHANNEL MANUAL (ORDER NO. FM47, SECTION IV).

Figure 3-36 SPM Map for SSC Dump Format

ERR 1 & ERR2:

LOCATION 1A = LSB ERROR WORD
LOCATION 1B = MSB ERROR WORD

SYSTEM FAULT WORD:

ERR2* (SYSTEM BUS)

A	0	1	2	3	4	5	6	7
	UCER	ILLEGAL FC	DPEL	DPER	APE	ILLEGAL NAK	QLT ERROR	

ERR1* (I/O BUS)

B	0	1	2	3	4	5	6	7	
	ILLEGAL FC	DPEL	DPER	APE	NOT USED	QLT ERROR	1	0	CHANNEL DETECTED FAULT
							1	1	IOM DETECTED FAULT

*COMPARE IOM FAULT STATUS WORD

ADR1, ADR2, AND ADR3:

LOCATION 0A, 09, 08 = ADDRESS OF DATA ICW (MSB, MID, LSB)
CONSOLE = 463
DISKETTE = 467

STA1, STA2, & STA3:

LOCATION 0D, 0C, 0B = ADDRESS OF STATUS ICW (MSB, MID, LSB)
CONSOLE = 461
DISKETTE = 465

CNF1 & CNF2:

LOCATION 10 = CNF1 = SPECIAL INTERRUPT (CELL, LEVEL)
I.E., 101 = [1 0000 0001]
HNP = 1, NML = 0 — CELL 0 LVL1

LOCATION 11 = CNF2 = TERMINATE INTERRUPT (CELL, LEVEL)

EXW1 & EXW2:

LOCATION 31, 30 = LOCATION OF 18-BIT LDEX/STEX OPERAND (DATA) WORD
EXW2, EXW1

PCW1, PCW2, PCW3, & PCW4:

LOCATION 33, 32 = MSB, LSB OF SECOND HALF PCW WORD
LOCATION 35, 34 = MSB, LSB OF FIRST HALF PCW WORD

Figure 3-37 SSC SPM Miscellaneous Byte Definitions

3.5.9.6 KSR-33 Teletype Console (DCF6608)

NOTE

When performing KSR-33 modifications, refer to the following: the Teletype card entitled Instructions for Activating Set Options, the Teletype manual provided with the documentation package and the instructions in the following subsections.

3.5.9.6.1 Removing KSR-33 Cover

To remove the cover, proceed as follows (see Figure 3-38):

WARNING

To avoid bodily injury, the ac power cords to the unit must be disconnected prior to removing the Teletype cover.

1. Remove the control knob from the front lower right-hand side of the console.
2. Remove the nameplate from the front of the console by grasping the nameplate at the bottom and pulling down and out.
3. Remove or loosen the four screws at the front of the console and the three screws at the rear of the console.
4. Pull the platen knob off.
5. Grasp the cover and raise it straight upward.

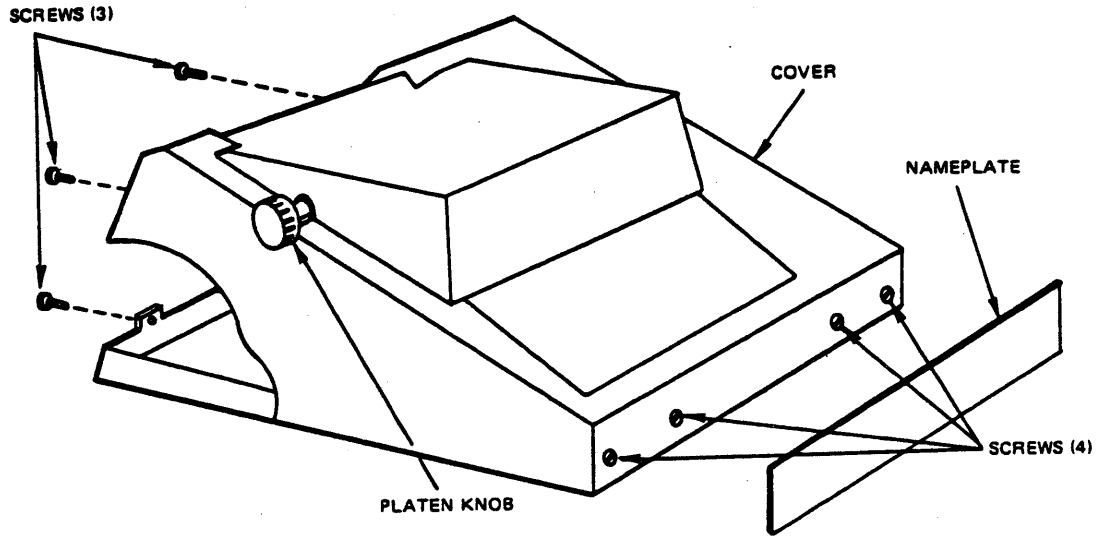


Figure 3-38 KSR-33 Cover Removal

3.5.9.6.2 Checking for Factory Incorporated Options

Check for the options as follows:

1. Keyboard Parity: The KSR-33 is wired for even parity. Refer to Teletype document 9334WD for odd parity operation.

2. Automatic Carriage Return: This option is disabled at the factory and must remain disabled (see Figure 3-39).

3. Answerback: The KSR can operate on local or remote answerback mode. To disable remote answerback, move the copper colored clip from the right front of the code bar basket to slot 15 at the right end of the code bar basket (see Figure 3-39).

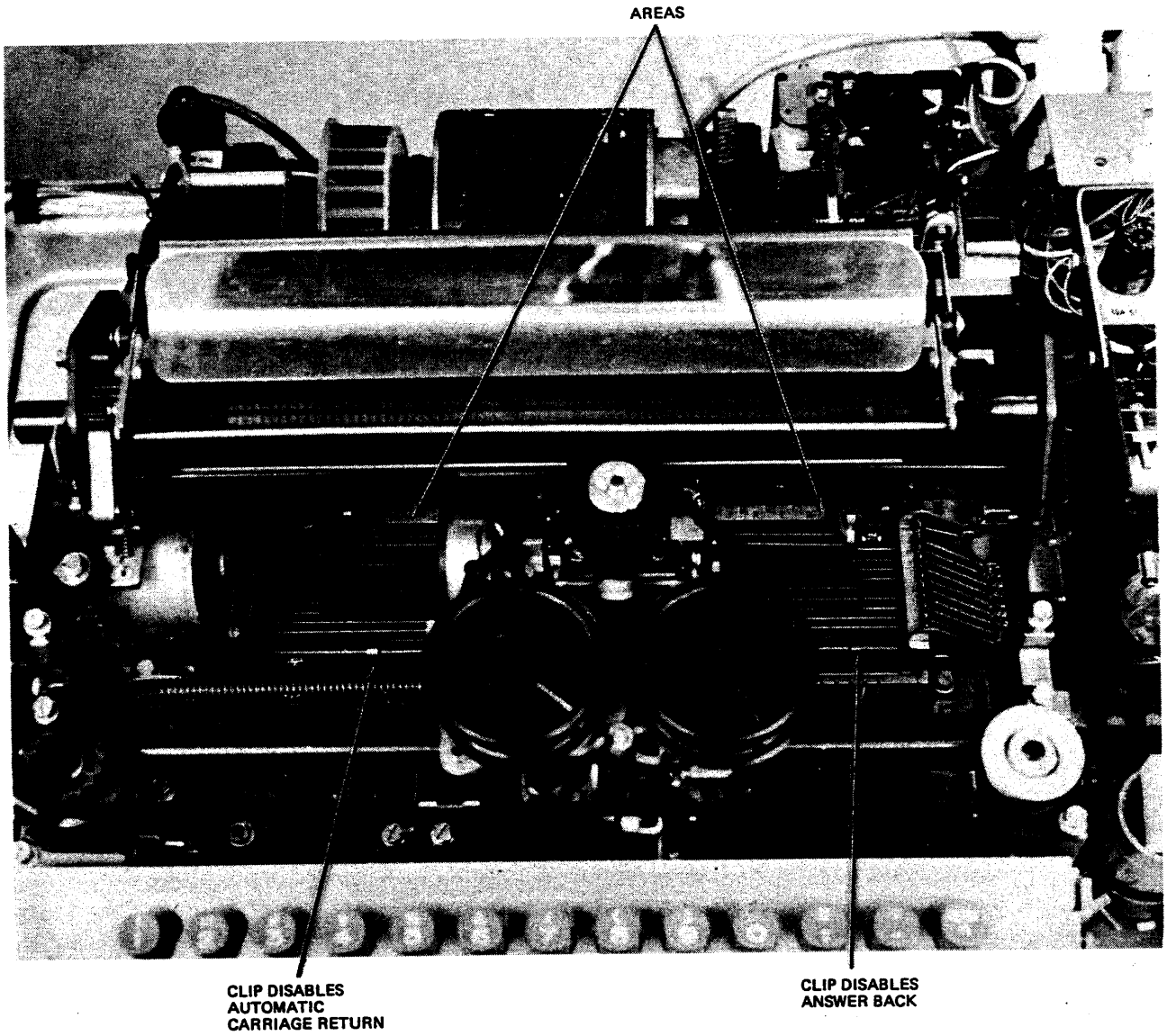


Figure 3-39 Disabling Answerback and Carriage Return

3.5.9.6.3 Full Duplex Option

To rework the KSR for full duplex operation, proceed as follows:

CAUTION

The KSR-33 must be in full duplex mode for proper operation on the system. If not in full duplex mode, the KSR will damage the SSC controller board.

1. Locate terminal board X under the mate-and-lock connectors at the left of the console, viewing the console from the rear (see Figure 3-40).

2. Remove the brown wire with the yellow stripe from terminal 3 of terminal board X.

3. Remove the white wire with the blue stripe from terminal 4 of terminal board X.

4. Connect these two wires (brown with yellow stripe and white with blue stripe) to terminal 5 of terminal board X (see Figure 3-41).

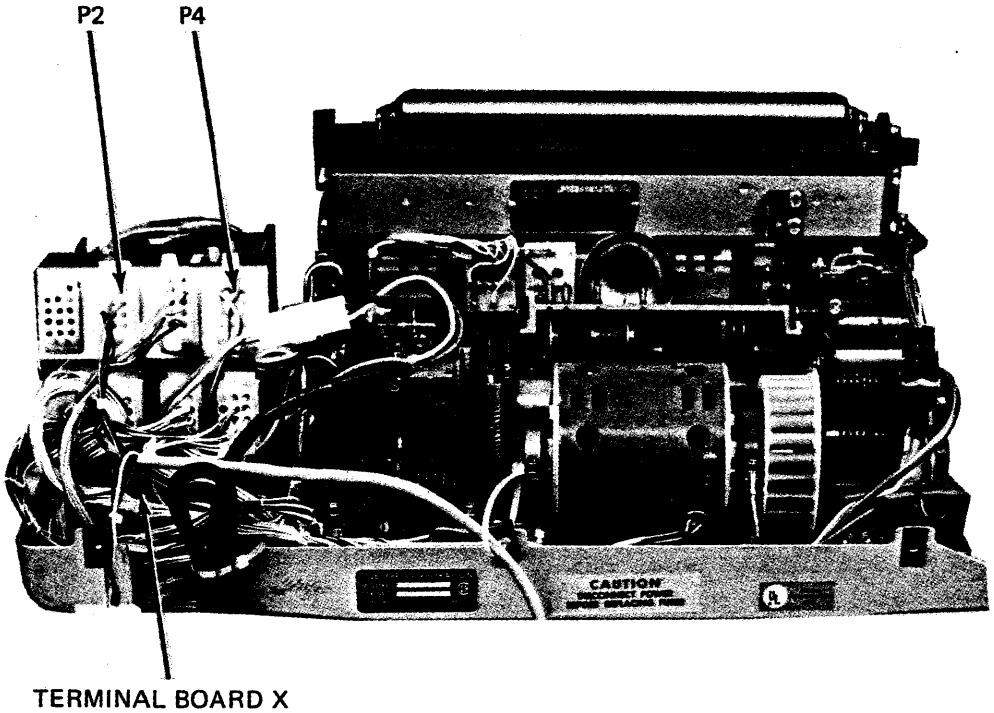


Figure 3-40 KSR-33 Terminal Board X

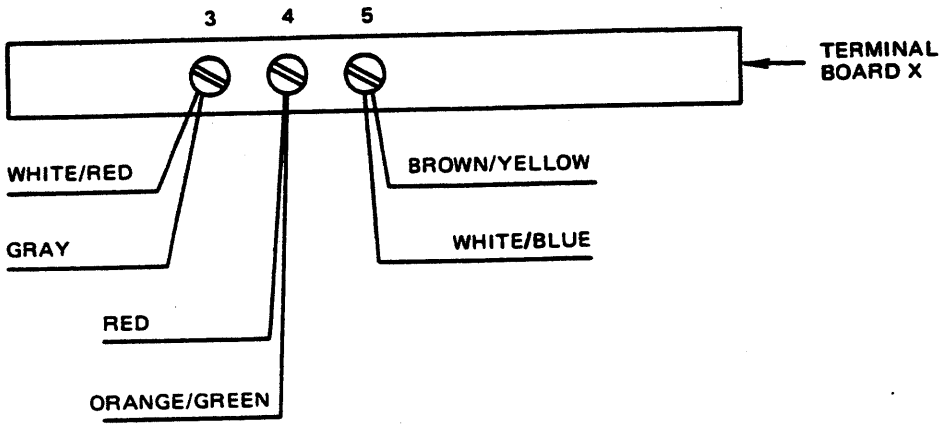


Figure 3-41 Full Duplex Wiring

3.5.9.6.4 Cabling KSR-33

When cabling a KSR-33 that does not have the Auto-Shutdown option installed, proceed as follows:

CAUTION

The KSR-33 must be wired for current mode operation; otherwise, controller boards in the system may be damaged.

The current mode console adapter cable (60128478-014) that plugs into P2 (see Figure 3-40) of the KSR is a 4-wire cable. To check if the KSR is equipped for current mode operation, look at P2. If P2 was altered (via an adapter, etc.) to accept a different connector, then the KSR is not wired for current mode and must not be used with the system.

CAUTION

The KSR-33 must be wired for 60-milliampere current mode operation; otherwise, damage to the equipment may result.

The 60-milliampere current mode operation is indicated by a purple wire on terminal 8 of terminal board X and a blue wire on terminal 3 of the power resistor (see Figure 3-42).

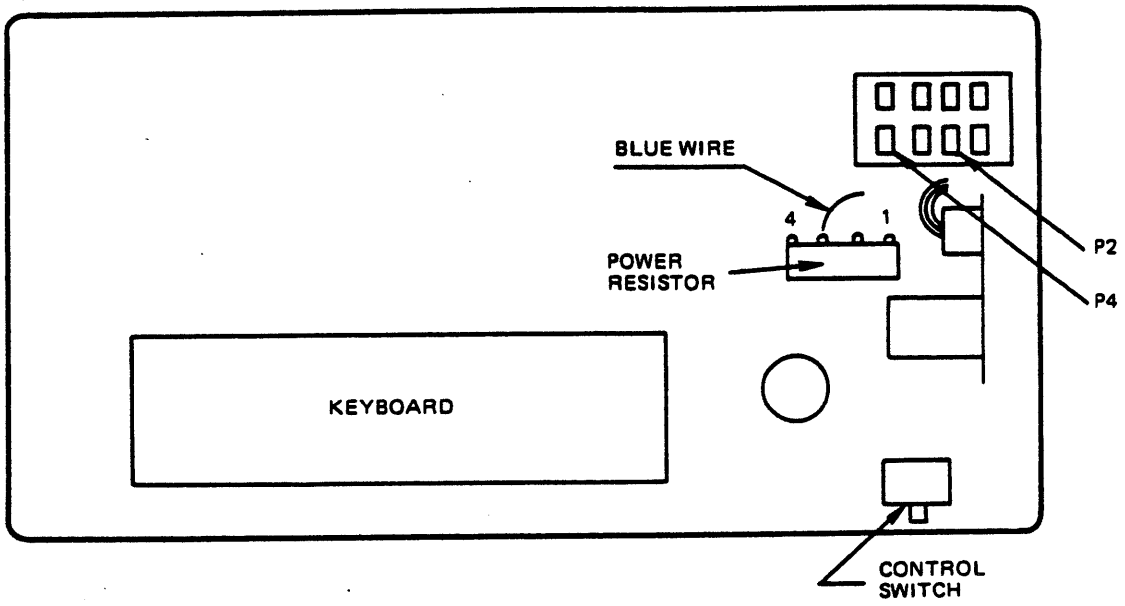


Figure 3-42 Locating Power Resistor in KSR-33

If these wires are not as described above, then:

1. Move the purple wire from terminal 9 to terminal 8 on terminal board X.

2. Move the blue wire from terminal 4 to terminal 3 on the power resistor.

Once the proper current mode operation of the KSR-33 is ensured:

1. Plug the console adapter cable (60128478-014) into P2 of KSR-33.

2. Route the cable through the cutout at the bottom of the system cabinet.

3. Locate the Console Adapter-Pac and plug the free end of the cable into the receptacle on the Adapter-Pac.

4. Verify that the console baud rate switch and the SSC channel switches are set correctly (see Figure 3-33).

5. Replace the cover on KSR-33. Tighten the screws shown in Figure 3-38. Replace the trimplate, control knob, and platen knob.

6. Plug the ac power cord into the ac receptacle at the PDU and connect the ac power to the system according to subsection 3.3.4.

3.5.9.6.5 Installation and Cabling of Auto-Shutdown Option

To install the Auto-Shutdown option, proceed as follows:

1. Remove the KSR-33 cover according to subsection 3.5.9.6.1.

2. Remove the back cover of the KSR-33 stand by removing the two screws in the upper corners of the stand.

3. Place the auto-shutdown box in the rear area of the KSR-33 stand (see Figure 3-43). Fasten the auto-shutdown box to the stand with the hardware supplied.

4. Connect one branch of the signal cable from the auto-shutdown box into the P2 receptacle of the KSR-33. Plug the other branch of this cable into the adapter cable (60128478-014). (See Figure 3-44 for the cable signal and wiring diagram.)

5. Unplug the TTY ac power cord connector from the P4 receptacle.

6. Using a Molex extractor tool (HT2038) or the equivalent, push out the white wire contact (pin 01) and the violet wire contact (pin 03) at P4.

7. Reconnect these two extracted wires (white and violet) into the new (supplied) 2-pin connector, ensuring that the white and violet wires mate with the black and white wires, respectively, of the MC300H motor ac power cord. After mating the new connector with the motor ac power connector, connect the green wire on the motor ac power cable to the KSR-33 chassis ground.

8. Plug the other end of the MC300H motor ac power cord into the auto-shutdown box at the receptacle that is labelled CONTROLLED.

9. Reconnect the TTY ac power cord into the P4 receptacle.

10. Plug the other end of the TTY ac power cord into the auto-shutdown box receptacle labelled CONVENIENCE.

11. Replace the rear cover of the KSR-33 stand, replace the console cover, and tighten the seven holding screws.

12. Replace the nameplate. Attach the WARNING labels supplied for the KSR-33 cover as shown in Figure 3-45. Replace the control knob and platen knob.

13. Ensure that the BYPASS switch on the auto-shutdown box is in the ENABLED (left) position.

14. Ensure that the system power switch is in the OFF position. Connect all the system ac power cords to the power source according to subsection 3.3.4.

15. Run Test and Diagnostic program CO to verify proper operation.

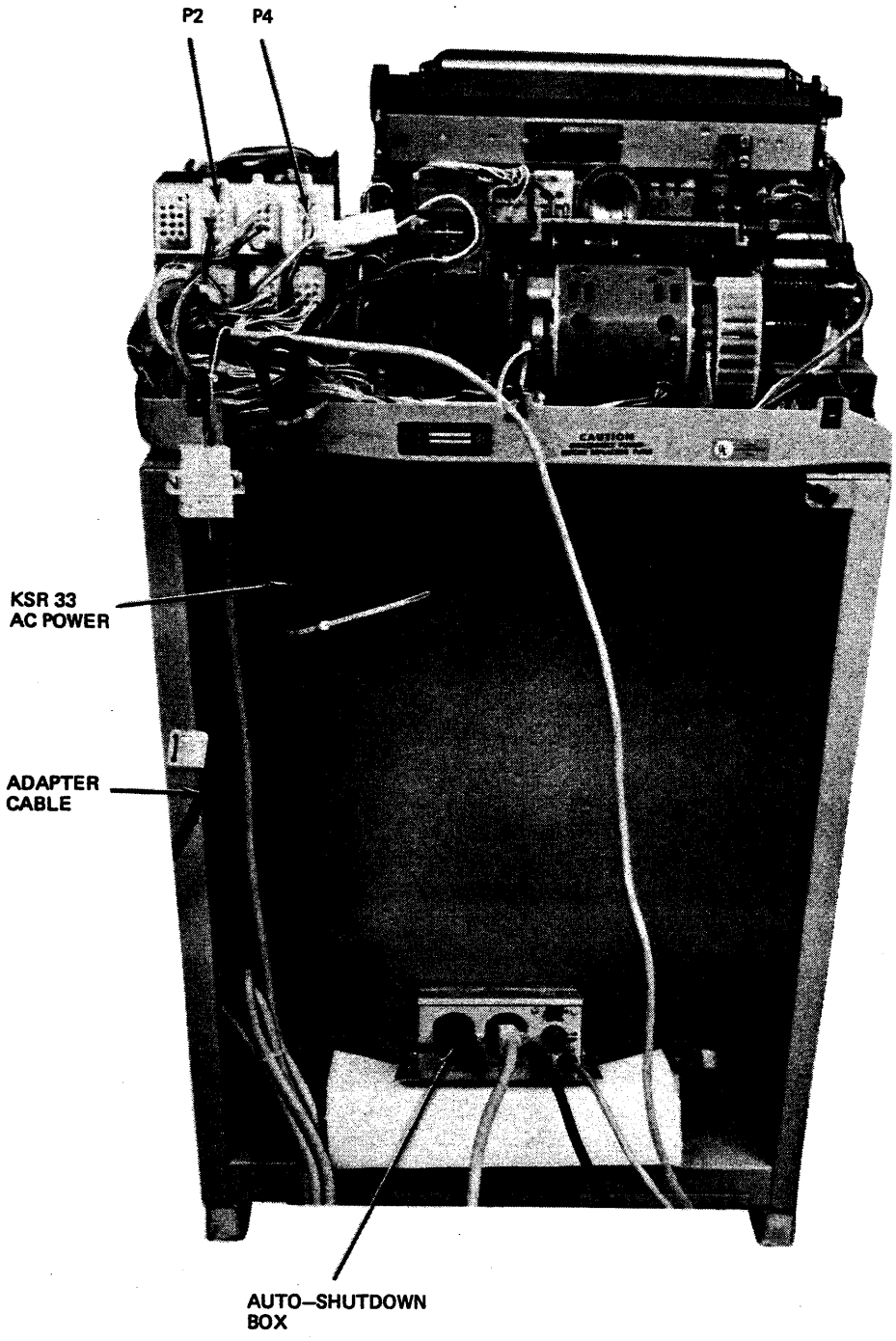


Figure 3-43 Auto-Shutdown Installation

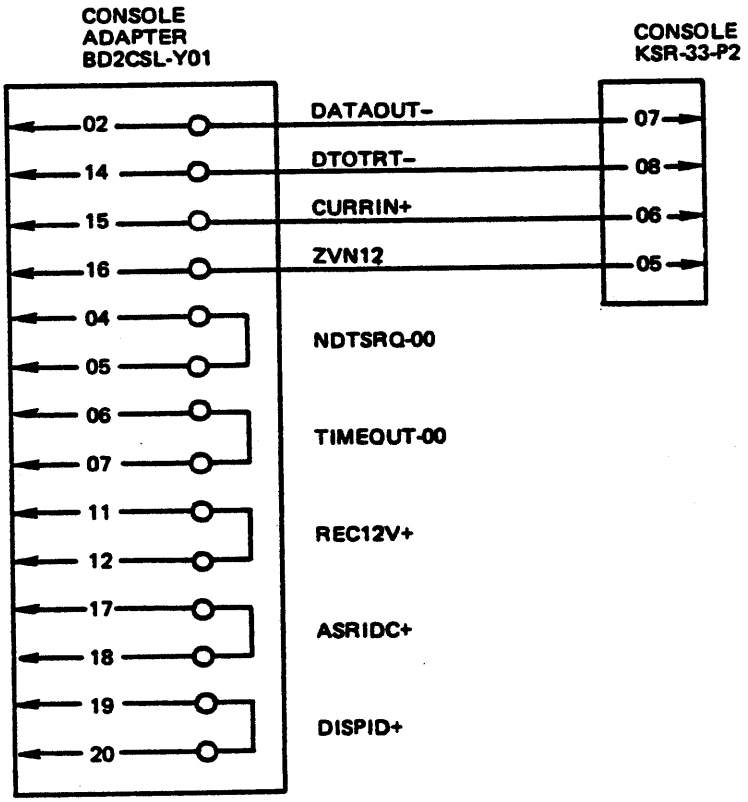


Figure 3-44 DCF6606 Console Cable (60128478-014) Signal and Wiring Diagram

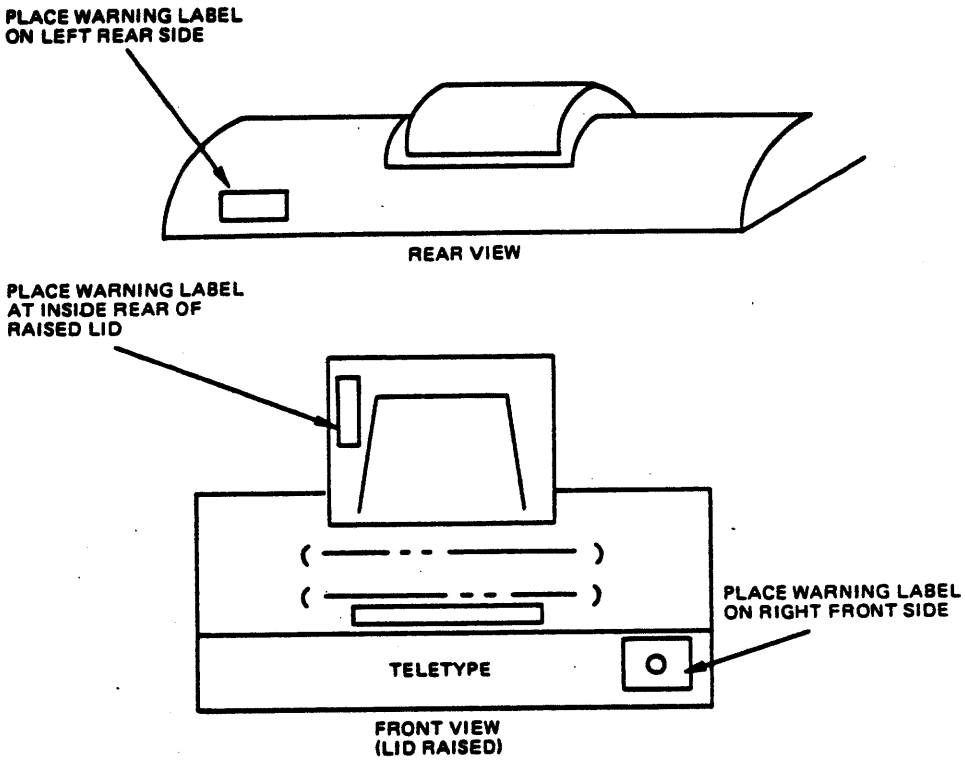


Figure 3-45 Auto-Shutdown WARNING Label Application

3.5.9.7 Installation of Heavy-Duty Typewriter Console (DCF6606)

The installation procedure for the heavy-duty typewriter console follows:

1. Ensure that the POWER switch on the system control panel is in the OFF (down) position (DC ON indicator must not be lit) and all ac power cords are disconnected.

2. Ensure that the console power ON/OFF switch at the rear of the console (Figure 3-46) is in the OFF position.

3. Locate the adapter cable (60128478-013) and plug it into the receptacle at the rear of the console. (See Figure 3-47 for the cable signal and wiring diagram.)

4. Connect the ground lead to the ground connection on the console.

5. Route the cable to the system cabinet and pass it through the cutout at the bottom of the cabinet.

6. Plug the free end of the cable into the Console Adapter-Pac.

7. Connect the ground lead to the ground connection on the chassis assembly.

8. Ensure that the system power switch is in the OFF position. Connect the console ac power cord (78200305-001) to the filtered receptacle (J07) on the PDU.

NOTES

1. Refer to subsection 3.5.9.2 for the switch configuration on the SSC and console adapter boards.

2. For the DCF6606 console operation, refer to Product Manual 71011334.

3. An optional stand is available for this device.

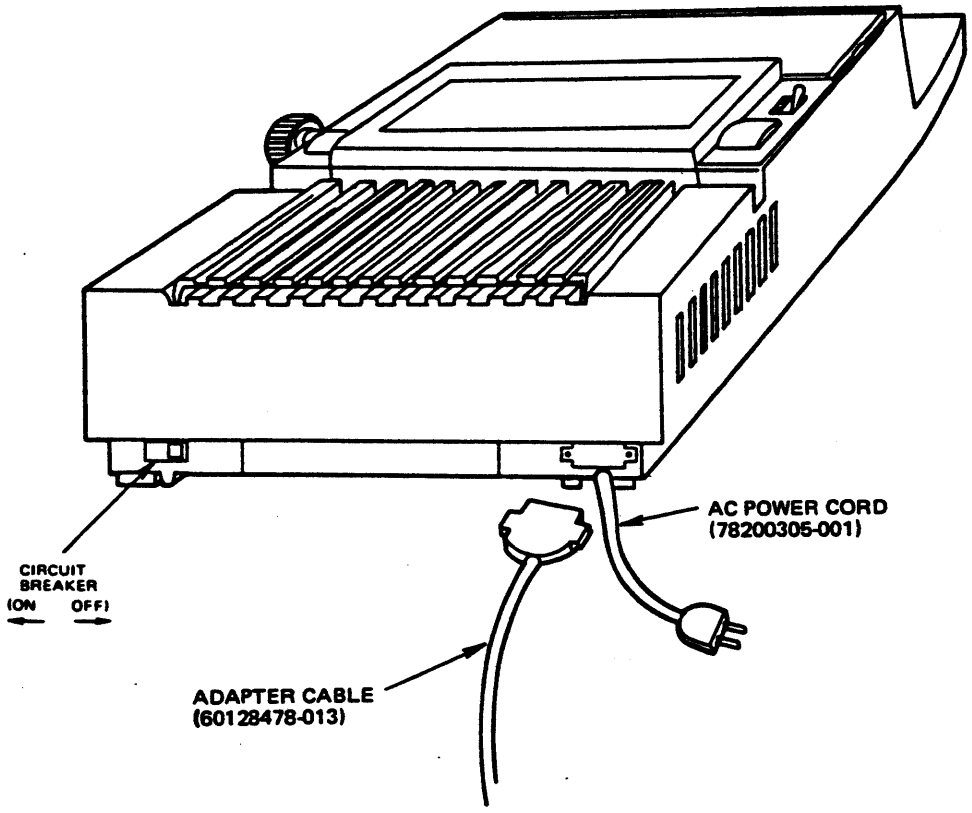


Figure 3-46 DCF6606 Console (Rear View)

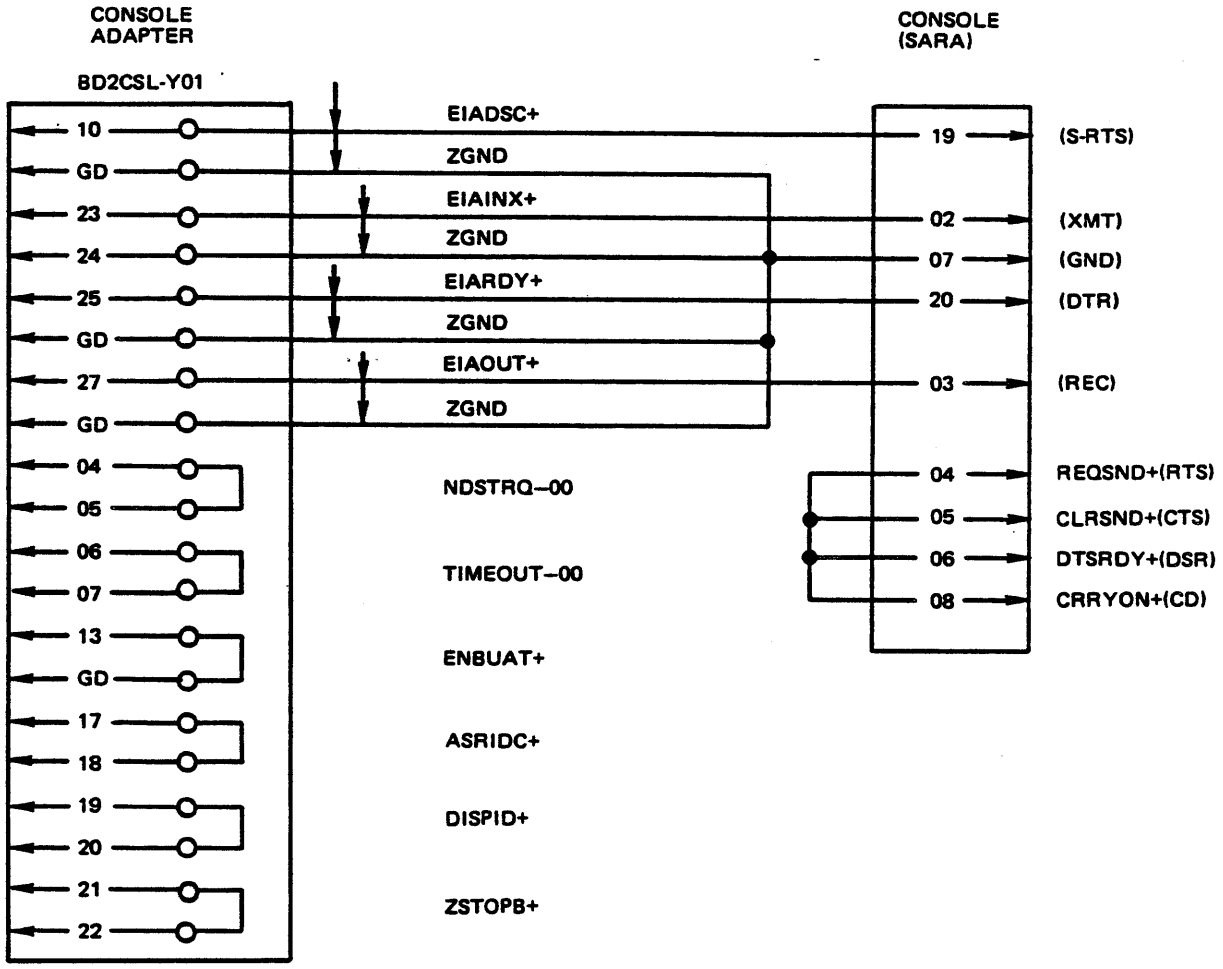


Figure 3-47 DCF6606 Console (SARA) Cable (60128478-013) Signal and Wiring Diagram

3.5.10 Direct Interface Adapter

The Direct Interface Adapter (DIA) is an I/O channel device that is used as a data and control link between the system and an L66 host central system.

3.5.10.1 DIA Description

Physically, the DIA consists of the DIA controller board (BF4DIA), DIA interface adapter (BG4DID), configuration panel, configuration panel cable, and the L66 cables. The DIA controller board (see Figure 3-48) plugs directly into the system I/O bus.

The BG4DID interface board is attached to the BF4DIA board by seven 25-pin stacking connectors. The interface board also has three 44-pin, rear-edge connectors. Two of these rear-edge connectors (Y01 and Y04) are connected to either the DIA/PIA bulkhead or the Mini PIA bulkhead at the back of the system cabinet by a cable, which allows the interface signals to be passed to the L66 Direct Channel Adapter (DCA). The third rear-edge connector (Y03) connects to the DIA configuration panel (see Figure 3-48).

The DIA circuit board contains a hexadecimal (HEX) rotary address switch at location B08.

The DIA configuration panel contains rocker switch assemblies that determine the mailbox addresses and interrupt levels used by the DIA (see Figure 3-49).

3.5.10.2 DIA Switch Settings

WARNING

To avoid bodily injury, extreme caution must be exercised when accessing the DIA configuration panel due to the presence of voltage within the exposed controller board chassis.

The switches are located within the system top dress panel and normally are set as shown in Figure 3-49. The first DIA usually is set to channel number 04.

NOTE

The DIA Interface-Pac may have to be removed to change the switch setting.

The second DIA (if installed) usually is set to channel number 14, hexadecimal C.

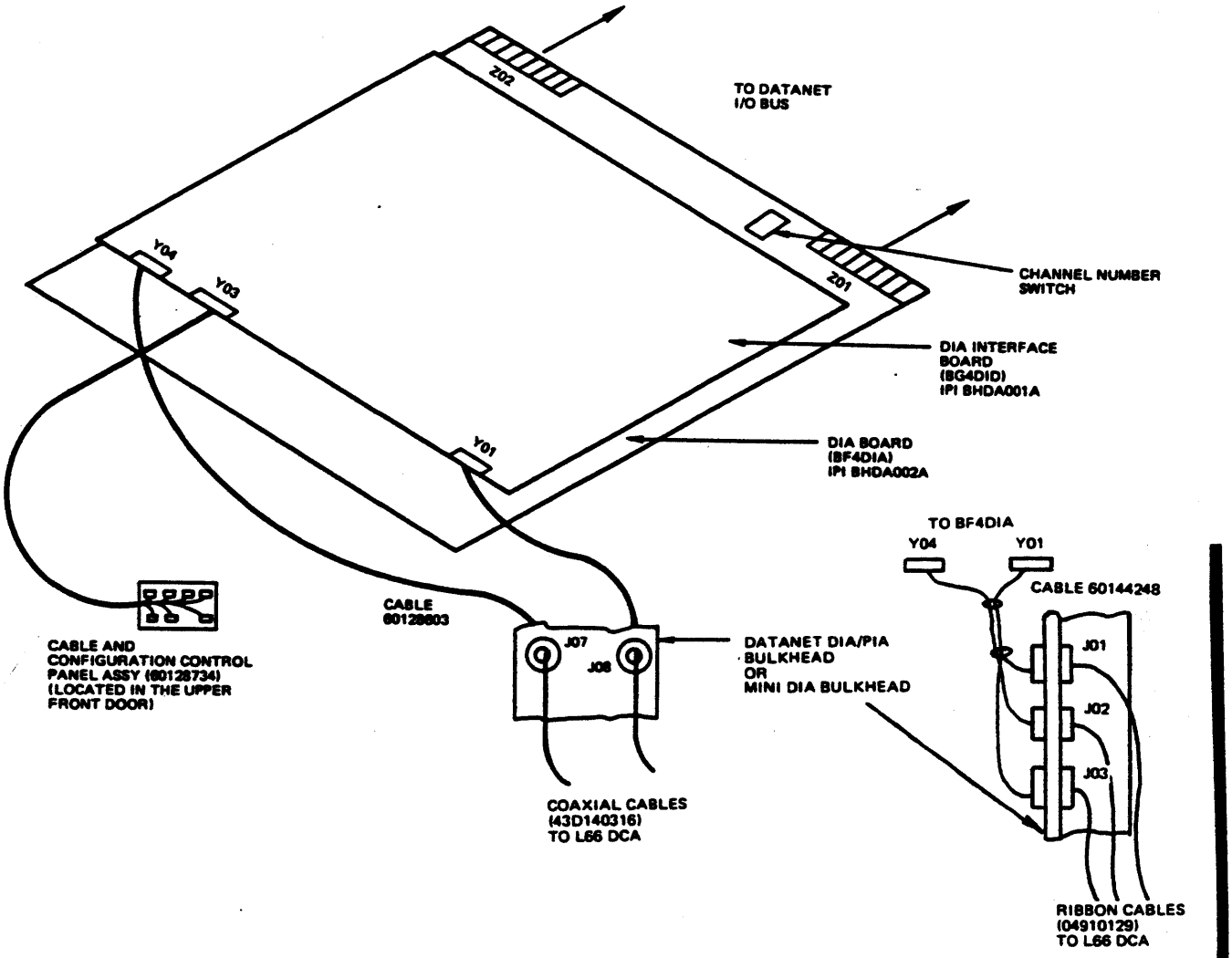


Figure 3-48 DIA Board Layout

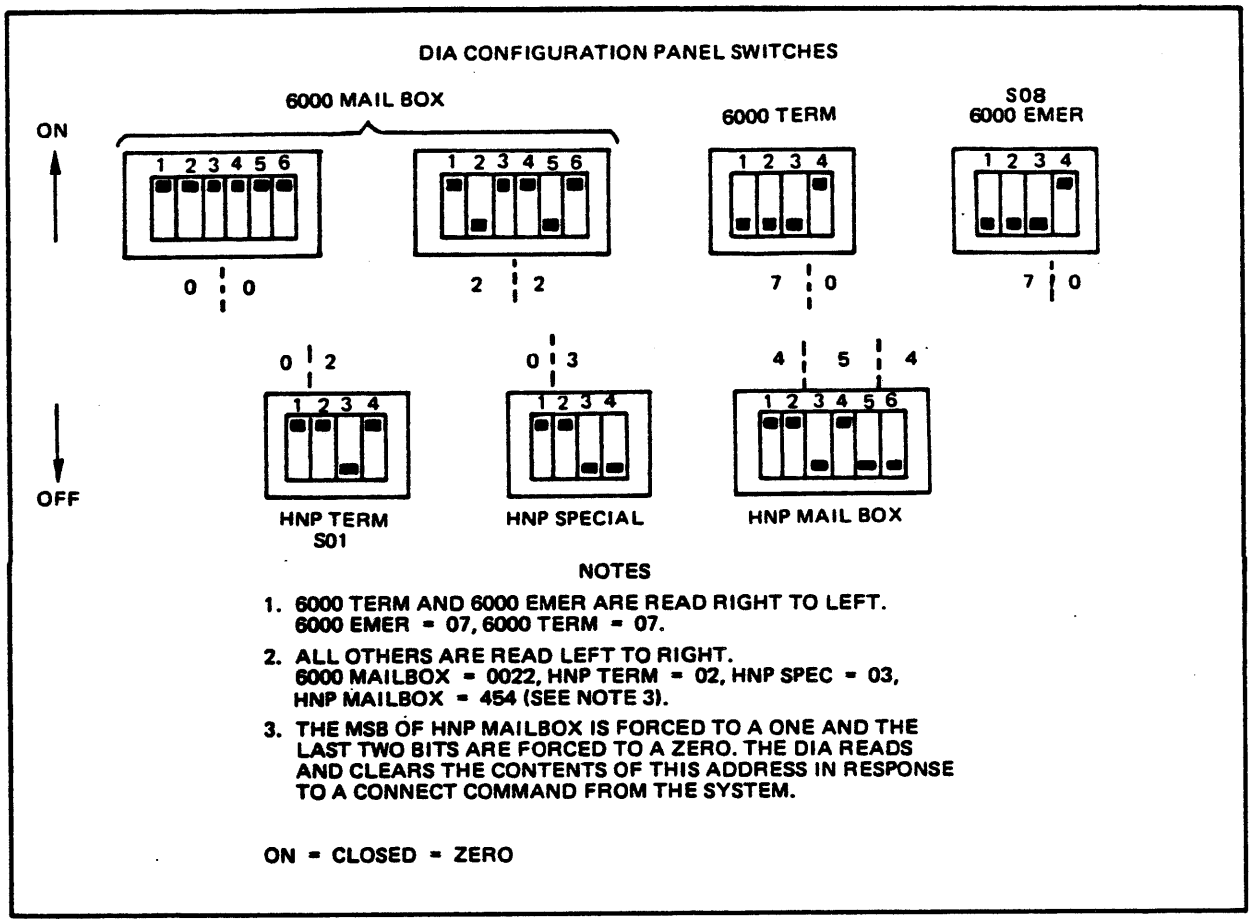


Figure 3-49 DIA Configuration Panel Switch Settings

3.5.10.3 System to L66 Cabling

The Direct Interface Adapter (DIA) provides the interface to the L66 system. The factory-installed internal cable connects the DIA Interface-Pac to a bulkhead panel (either cable 60128603 for the DIA/PIA bulkhead or cable 60144248 for the Mini DIA bulkhead). The bulkhead panel (see Figure 3-50) is accessible from the rear of the system cabinet. The configuration of the internal cable is such that the wires from Y01 and Y04 are both control and data lines (refer to Tables 3-9 and 3-9.1).

If it becomes necessary to remove or install the internal cable, note that:

1. The cable, because of its configuration, must be installed from the back of the cabinet.

2. J01 and J02 on cable 60128603 connect to J07 and J08, respectively, on the DIA/PIA bulkhead. J01, J02, and J03 on cable 60144248 connect to J01, J02, and J03, respectively, on the Mini DIA bulkhead.

3. The branch of the cable with the Y01 paddleboard is passed to the left of the system cabinet between the cover and the chassis that contains the DIA controller. The paddleboard is connected to Y01 on the DIA Interface-Pac.

4. The branch of the cable with the Y04 paddleboard is passed to the right of the system cabinet between the cover and the chassis that contains the DIA controller. The paddleboard is connected to Y04 on the DIA Interface-Pac.

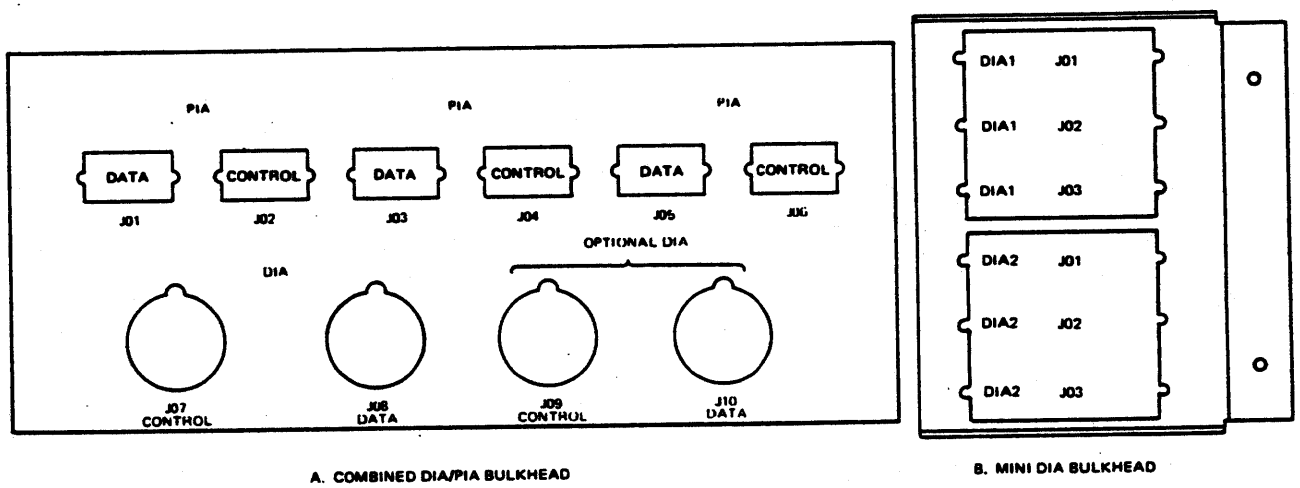


Figure 3-50 System DIA/PIA Bulkhead and Mini DIA Bulkhead

Table 3-9 DIA to Bulkhead Signals -- Cable 60128603

DIA		SIGNAL	BULKHEAD
Data	Y04-20	DATA00+	J02-01
Data	Y04-42	DATA01+	J02-02
Data	Y04-19	DATA02+	J02-03
Data	Y04-41	DATA03+	J02-04
Data	Y04-15	DATA04+	J02-05
Data	Y04-35	DATA05+	J02-06
Data	Y04-13	DATA06+	J02-07
Data	Y04-36	DATA07+	J02-08
Data	Y04-12	DATA08+	J02-09
Data	Y04-32	DATA09+	J02-10
Data	Y04-10	DATA10+	J02-11
Data	Y04-31	DATA11+	J02-12
Data	Y04-07	DATA12+	J02-13
Data	Y04-30	DATA13+	J02-14
Data	Y04-01	DATA14+	J02-15
Data	Y04-27	DATA15+	J02-16
Data	Y04-06	DATA16+	J02-17
Data	Y04-28	DATA17+	J02-18
Data	Y01-22	DATA18+	J02-19
Data	Y01-43	DATA19+	J02-20
Data	Y01-20	DATA20+	J02-21
Data	Y01-42	DATA21+	J02-22
Data	Y01-19	DATA22+	J02-23
Data	Y01-41	DATA23+	J02-24
Data	Y01-18	DATA24+	J02-25
Data	Y01-39	DATA25+	J02-26
Data	Y01-15	DATA26+	J02-27
Data	Y01-35	DATA27+	J02-28
Data	Y01-10	DATA28+	J02-29
Data	Y01-30	DATA29+	J02-30
Data	Y01-06	DATA30+	J02-31
Data	Y01-28	DATA31+	J02-32
Data	Y01-04	DATA32+	J02-33
Data	Y01-25	DATA33+	J02-34
Data	Y01-03	DATA34+	J02-35
Data	Y01-24	DATA35+	J02-36
Control	Y04-09	DAOPRL+	J01-01
Control	Y01-07	DATEST+	J01-02
Control	Y01-27	RSTCON+	J01-03
Control	Y01-09	DIADTA+	J01-04
Control	Y01-38	DTAENA+	J01-05
Control	Y01-16	REQEST+	J01-06
Control	Y04-25	DCOPRL+	J01-11
Control	Y04-04	DCTEST+	J01-12
Control	Y01-13	DCCNCT+	J01-13
Control	Y01-36	DCDATA+	J01-14
Control	Y01-12	DCINIT+	J01-15
Control	Y04-43	SYSFLT+	J01-16
Control	Y04-18	CMDPAR+	J01-17
Control	Y04-38	DTAERR+	J01-18
Control	Y04-39	IOMERR+	J01-19
Control	Y04-16	UBUSFT+	J01-20
Control	Y04-03	DATAPR+	J01-21
Control	Y04-22	BNDSER+	J01-22

Table 3-9.1 DIA to Bulkhead Signals -- Cable 60144248

DIA		SIGNAL	BULKHEAD
Data	Y04-20	DATA00+	J02-02
Data	Y04-42	DATA01+	J02-03
Data	Y04-19	DATA02+	J02-04
Data	Y04-41	DATA03+	J02-05
Data	Y04-15	DATA04+	J02-06
Data	Y04-35	DATA05+	J02-07
Data	Y04-13	DATA06+	J02-08
Data	Y04-36	DATA07+	J02-09
Data	Y04-12	DATA08+	J02-10
Data	Y04-32	DATA09+	J02-11
Data	Y04-10	DATA10+	J02-12
Data	Y04-31	DATA11+	J02-13
Data	Y04-07	DATA12+	J02-14
Data	Y04-30	DATA13+	J02-15
Data	Y04-01	DATA14+	J02-16
Data	Y04-27	DATA15+	J02-17
Data	Y04-06	DATA16+	J02-18
Data	Y04-28	DATA17+	J02-19
Data	Y01-22	DATA18+	J02-02
Data	Y01-43	DATA19+	J02-03
Data	Y01-20	DATA20+	J02-04
Data	Y01-42	DATA21+	J02-05
Data	Y01-19	DATA22+	J02-06
Data	Y01-41	DATA23+	J02-07
Data	Y01-18	DATA24+	J02-08
Data	Y01-39	DATA25+	J02-09
Data	Y01-15	DATA26+	J02-10
Data	Y01-35	DATA27+	J02-11
Data	Y01-10	DATA28+	J02-12
Data	Y01-30	DATA29+	J02-13
Data	Y01-06	DATA30+	J02-14
Data	Y01-28	DATA31+	J02-15
Data	Y01-04	DATA32+	J02-16
Data	Y01-25	DATA33+	J02-17
Data	Y01-03	DATA34+	J02-18
Data	Y01-24	DATA35+	J02-19
Control	Y04-09	DAOPRL+	J01-02
Control	Y01-07	DATEST+	J01-03
Control	Y01-27	RSTCON+	J01-04
Control	Y01-09	DIADTA+	J01-05
Control	Y01-38	DTAENA+	J01-06
Control	Y01-16	REQEST+	J01-07
Control	Y04-25	DCOPRL+	J01-08
Control	Y04-04	DCTEST+	J01-09
Control	Y01-13	DCCNCT+	J01-10
Control	Y01-36	DCDATA+	J01-11
Control	Y01-12	DCINIT+	J01-12
Control	Y04-43	SYSFLT+	J01-13
Control	Y04-18	CMDPAR+	J01-14
Control	Y04-38	DTAERR+	J01-15
Control	Y04-39	IOMERR+	J01-16
Control	Y04-16	UBUSFT+	J01-17
Control	Y04-03	DATAPR+	J01-18
Control	Y04-22	BNDSER+	J01-19

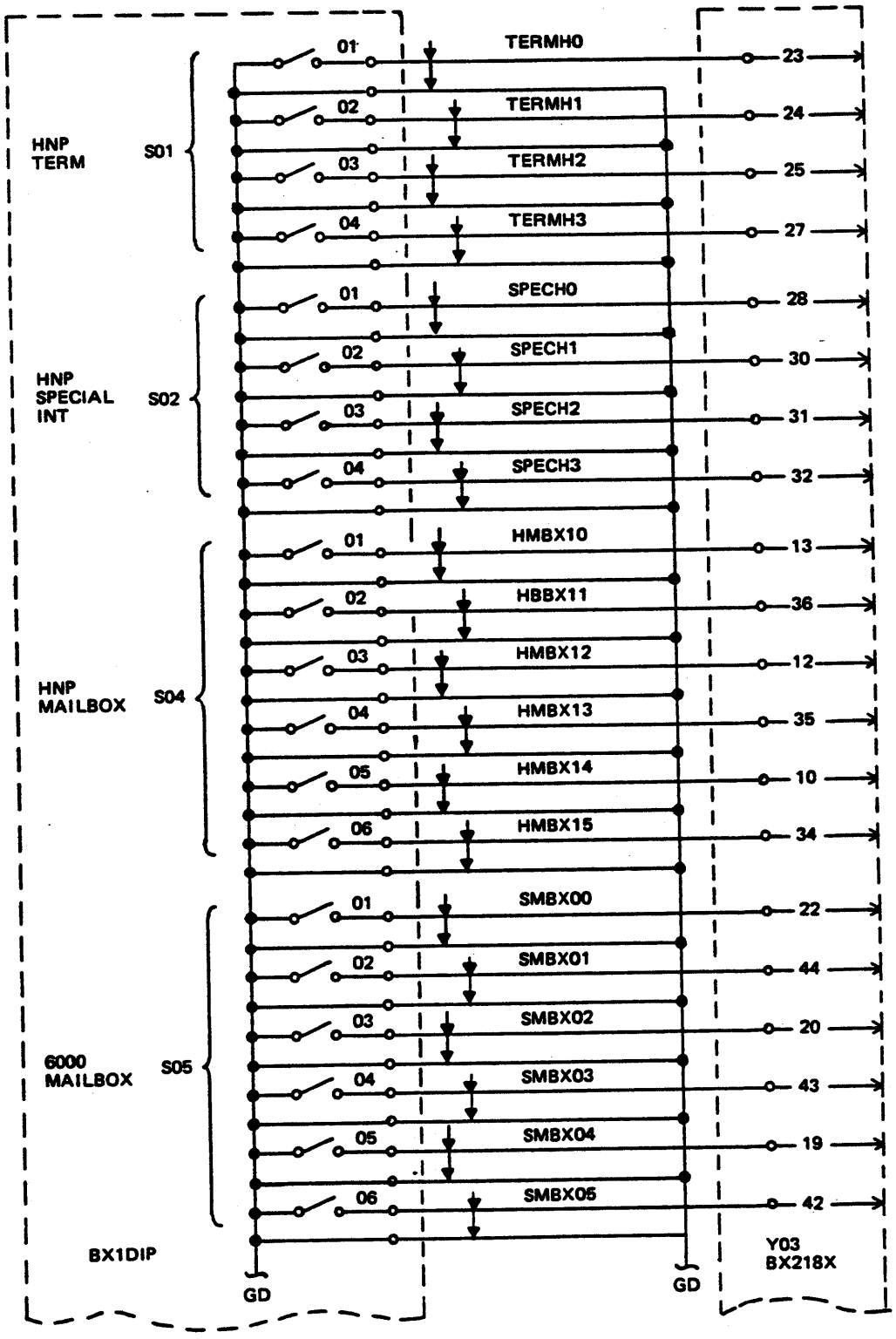


Figure 3-51 DIA Configuration Panel Cable (60128735) Wiring Diagram (Sheet 1 of 2)

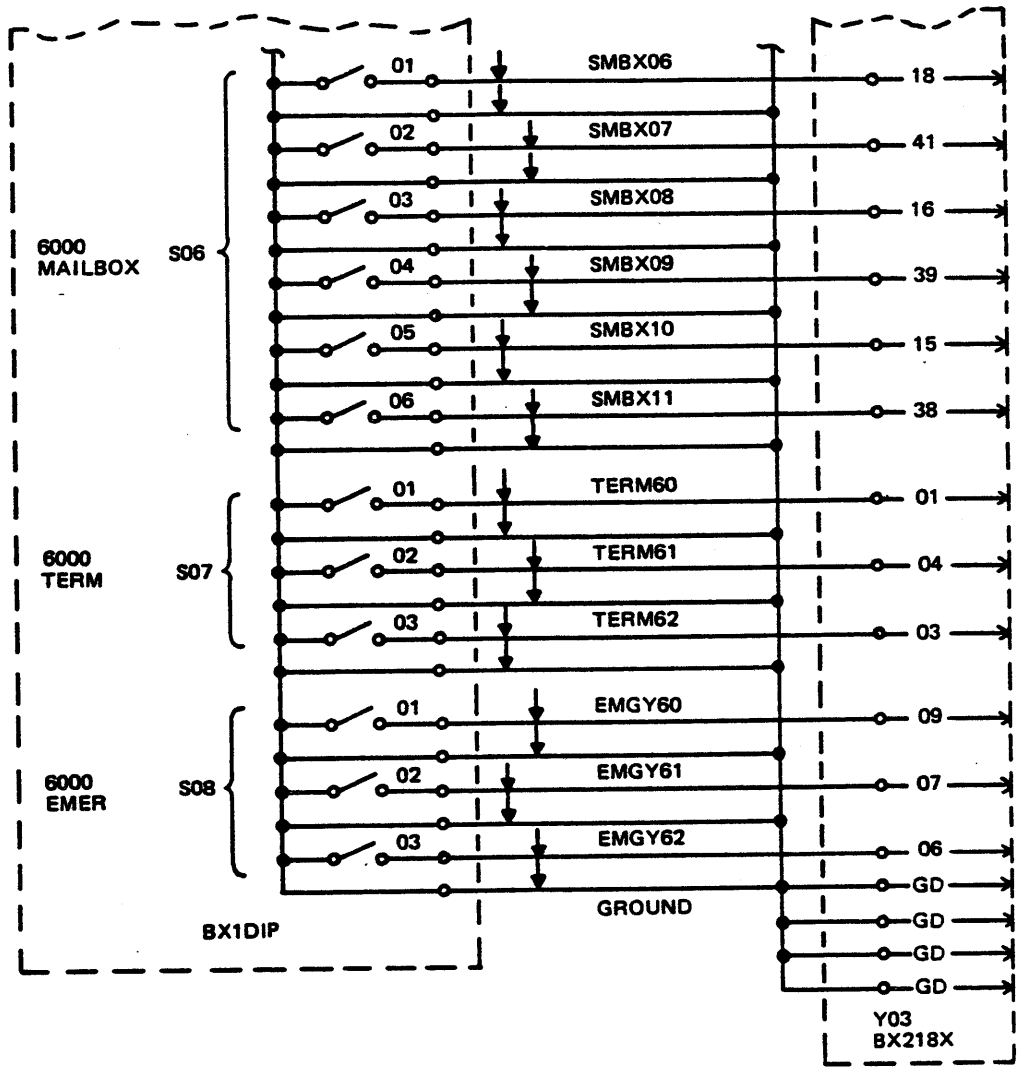


Figure 3-51 DIA Configuration Panel Cable (60128735) Wiring Diagram (Sheet 2 of 2)

The DIA configuration panel Cable (60128735) is factory installed and connects Y03 on the interface board to the DIA configuration control panel (see Figure 3-51). (The cable is soldered to the panel.) The configuration panel is attached to the inside of the top dress panel under a protective transparent shield, which is opened by turning two captive screws. The cable from the configuration panel is secured on the left side of the dress panel by a cable clamp. (Refer to sub- section 3.5.10.2 for the configuration panel switch settings.)

WARNING

To avoid bodily injury, extreme caution must be exercised when accessing the DIA configuration panel due to the presence of voltage within the exposed controller boards in the chassis.

CAUTION

Ensure the IOM cables are properly aligned during installation. Misalignment will damage the cables.

3.5.10.3.1 L66 Cabling Using a Mini DIA Bulkhead

To connect the Mini DIA bulkhead to the L66 IOM, proceed as follows:

1. Run the three 04910129 cables from the L66 IOM connector bulkhead through the cutout at the bottom of the cabinet.

2. Connect the cables from J1, J2, and J3 on the L66 IOM bulkhead to J01, J02, and J03 on the Mini DIA bulkhead.

3. If the system cabinet has a TB01, connect the ground cable (43B228514-75) from the L66 to TB01 in the bottom of the cabinet (see Figure 3-53). If the system cabinet doesn't have a TB01, connect the ground cable as shown in Figure 3-53.1.

NOTE

If the optional DIA has to be cabled, follow the procedure outlined in steps 1 and 2.

To connect the DIA/PIA bulkhead to the L66 IOM, proceed as follows:

1. Run the two 43D140316 cables from the L66 IOM connector bulkhead (see Figure 3-52) through the cutout at the bottom of the cabinet.

2. Connect the control/status cable from J1 on the L66 IOM bulkhead to J07 on the DIA/PIA bulkhead. Connect the data cable from J2 on the L66 IOM bulkhead to J08 on the DIA/PIA bulkhead.

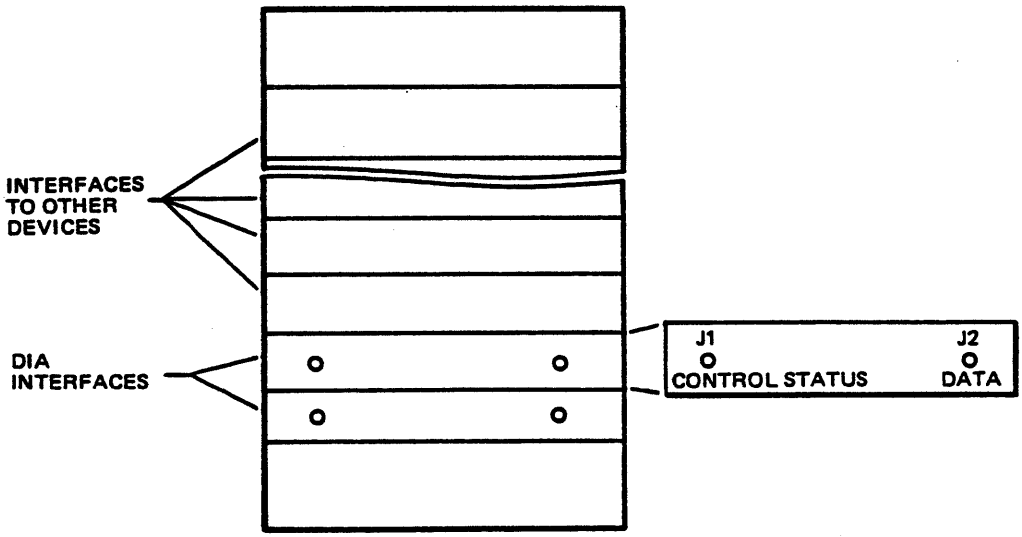


Figure 3-52 L66 IOM Connector Bulkhead

3. If the system cabinet has a TB01, connect the ground cable (43B228514-75) from the L66 to TB01 in the bottom of the cabinet (see Figure 3-53). If the system cabinet doesn't have a TB01, connect the ground cable as shown in Figure 3-53.1.

NOTE

If the optional DIA has to be cabled, follow the same procedure as above except use J09 (control) and J10 (data) on the DIA/PIA bulkhead. A second ground cable is not required.

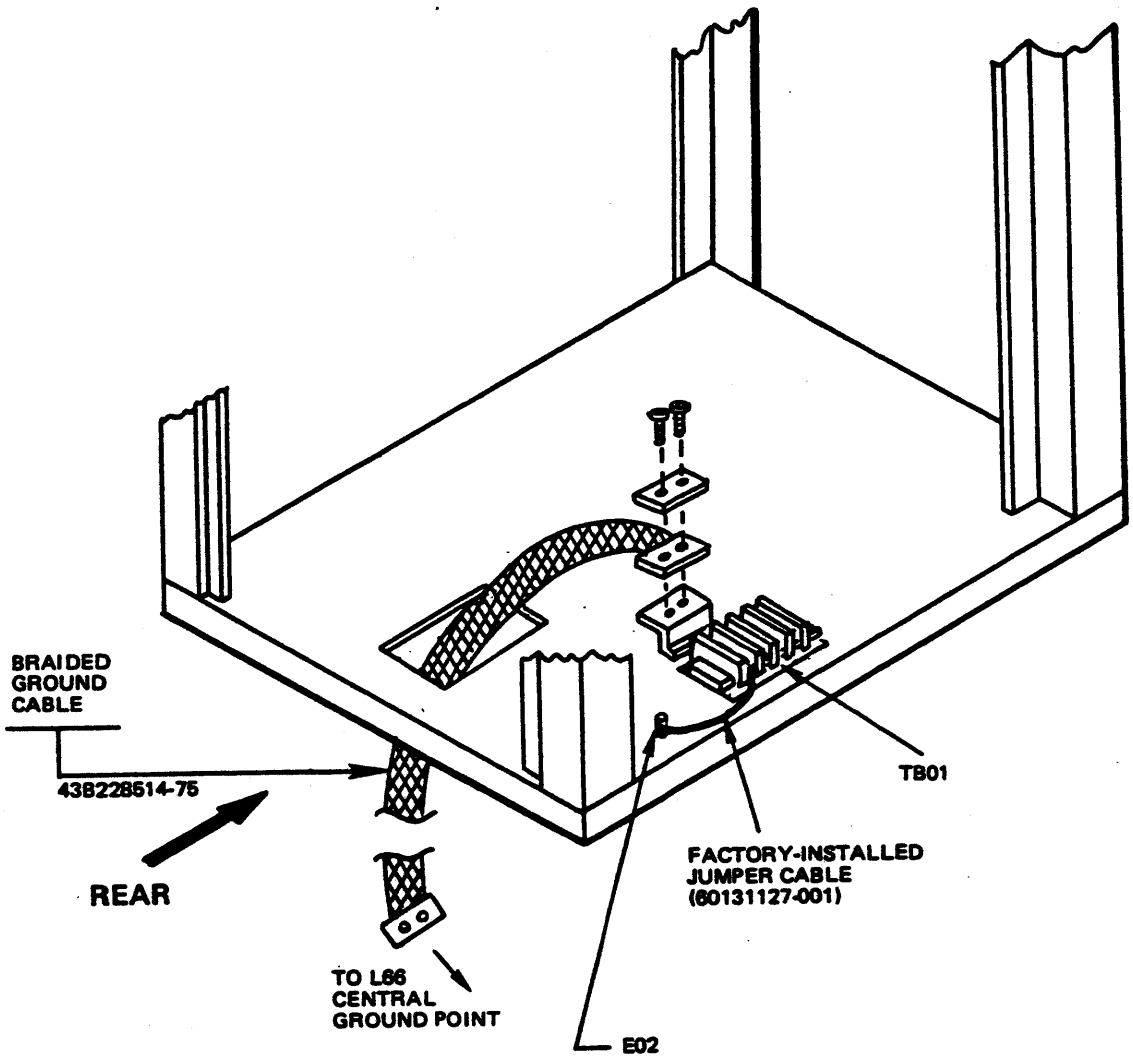


Figure 3-53 Ground Cable Installation -- L66 to System Cabinet TB01

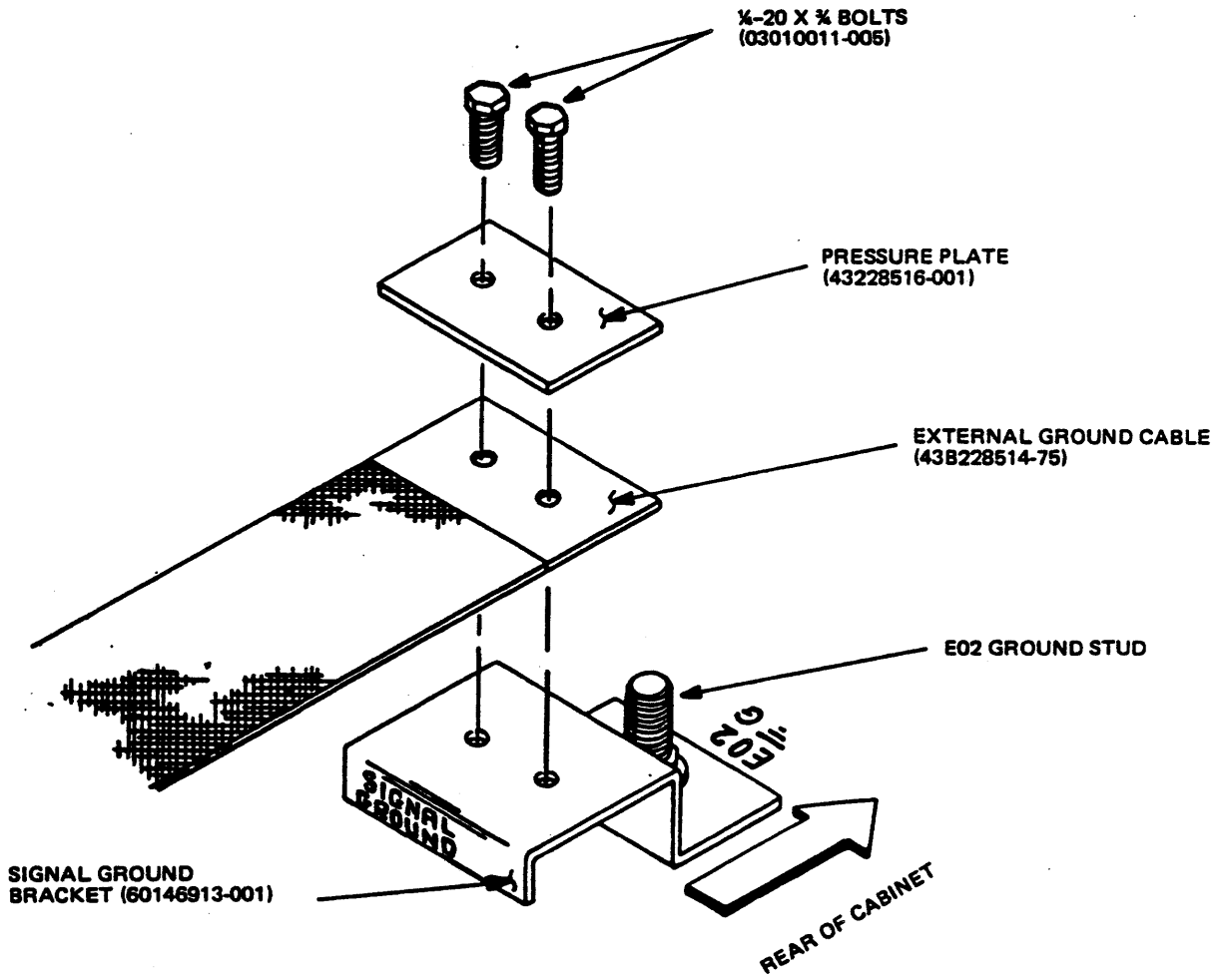


Figure 3-53.1 Ground Cable Installation -- L66 to System Cabinet E02

3.5.10.4 L66 I/O Bus

The DIA communicates with the L66 DCA via a bidirectional I/O bus. The interface signals between the DIA and L66 DCA are defined in subsection 3.5.10.5. (Refer to Table 3-9 for the wiring list.)

Figure 3-54 shows the DIA to L66 DCA interface lines.

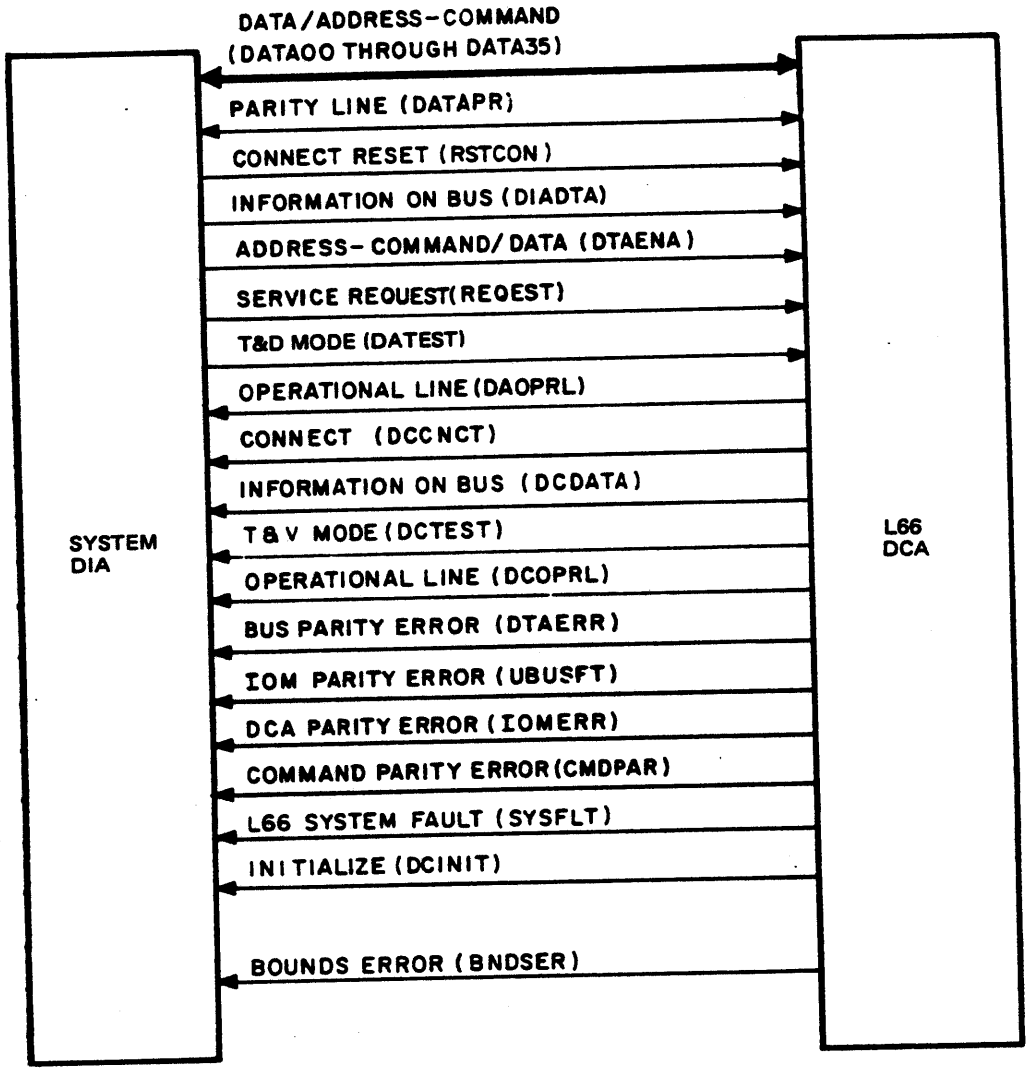


Figure 3-54 DIA/DCA Interface Lines

3.5.10.5 Definition of DIA/DCA Interface Lines

The interface lines are:

1. Data/Address -- Command Lines (DATA00 through DATA35): On these 36 lines, the DIA transfers data, address, and command information to the DCA. The DCA transfers data to the DIA.

2. Parity (DATAPR): The Parity line is used by the DIA and the DCA to make the 36 data lines. This Parity signal consists of an odd number of Ones.

3. Reset Connect (RSTCON): The Reset Connect line is used by the DIA to signal the DCA to reset the connect line. The DIA, having received the DCCNCT signal from the DCA, responds to the Connect.

4. DIA Data for DCA on Bus (DIADTA): The DIADTA line is used by the DIA to signal the DCA that data or control (command/address) information is on lines DATA00 through DATA35. This line is also used by DIA to acknowledge receipt of DCDATA information from the DCA.

5. Data/Address Enable (DTAENA): If the DTAENA line is set to a logic Zero, the DIA is indicating to the DCA that control information is on DATA00 through DATA35. If this line is at a logic One, then data is on the 36 data lines.

6. Service Request (REQEST): When True, REQEST signals the DCA to initiate an L66 IOM service request.

7. T&V Mode (DATEST): The DATEST line is forced True by the DIA when it is to enter the T&V mode involving the DCA. When the DIA is in functional data transfer mode, DATEST is False.

8. Operational Line (DAOPRL): When True, DAOPRL indicates that the DIA is ready to communicate with the DCA. When False, it indicates to the DCA that the DIA is in a test mode and will not respond to the Connect from the DCA.

9. DCA Connect (DCCNCT): When True, DCCNCT indicates a Connect from the L66 IOM.

10. DCA Data for DIA on Bus (DCDATA): The DCDATA line is used by the DCA to signal that data for the DIA is present on lines DATA00 through DATA35. This line is also used by the DCA to acknowledge receipt of DIADTA information from the DIA.

11. T&D Mode (DCTEST): When the DIA forces the DCTEST signal True, the DIA enters the T&V mode under control of the L66 IOM.

12. DCA Operational Line (DCOPRL): When True, the DCOPRL signal indicates that the DCA is ready to communicate with the DIA.

13. Bus Parity Error (DTAERR): When True, the DTAERR signal indicates that the L66 DCA detected a parity error on information received from the DIA.

14. IOM Parity Error (UBUSFT): When True, the UBUSFT signal indicates that the L66 DCA received a parity error signal for data transferred from the L66 IOM to the DCA.

15. DCA Parity Error (IOMERR): When True, the IOMERR signal indicates that the DCA detected a parity error on data transferred from the L66 DCA to the L66 IOM.

16. Command Parity Error (CMDPAR): When True, the CMDPAR signal indicates that the DCA detected a parity error in the command/address information received from the DIA.

17. L66 System Fault (SYSFLT): When True, the SYSFLT signal indicates that a system fault was detected while the L66 DCA was performing a service request to the L66 IOM.

18. DCA Initialize (DCINIT): When True, the DCINIT signal indicates that the L66 DCA received an Initialize signal from the L66 IOM.

19. Bounds Error (BNDSER): When True, the BNDSER signal indicates that the DCA detected an out-of-bounds address from the DIA.

3.5.11 Channel Interface Base Controller

The Channel Interface Base Controller (CIB) is a communications controller that interfaces with as many as four Communications Line Adapters (CLAs), as shown in Figure 3-55. CLAs interface with either one or two lines, depending upon the type of CLA. Also note that some CLAs are twice the physical size of others. Using oversize CLAs and/or CLAs with only one interface reduces the number of lines serviced by each CIB. The CIB uses both hardware and firmware to perform its functions. All of the CIB hardware and firmware is housed on one module board (BF4HML), which plugs into the I/O bus of the system.

3.5.11.1 CIB Description

Figure 3-55 shows the general layout of the CIB board (BF4HML) and the mounted CLAs. At the top of the board there are two 50-pin connectors (Z01 and Z02), which are used for the physical and electrical attachment of the board to the system I/O bus. Figure 3-55 also shows four 1/4-size CLAs attached to the component side of the CIB board. A maximum of four CLAs can be mounted and each CLA has one cable that interfaces with one or two data sets, depending on the CLA type.

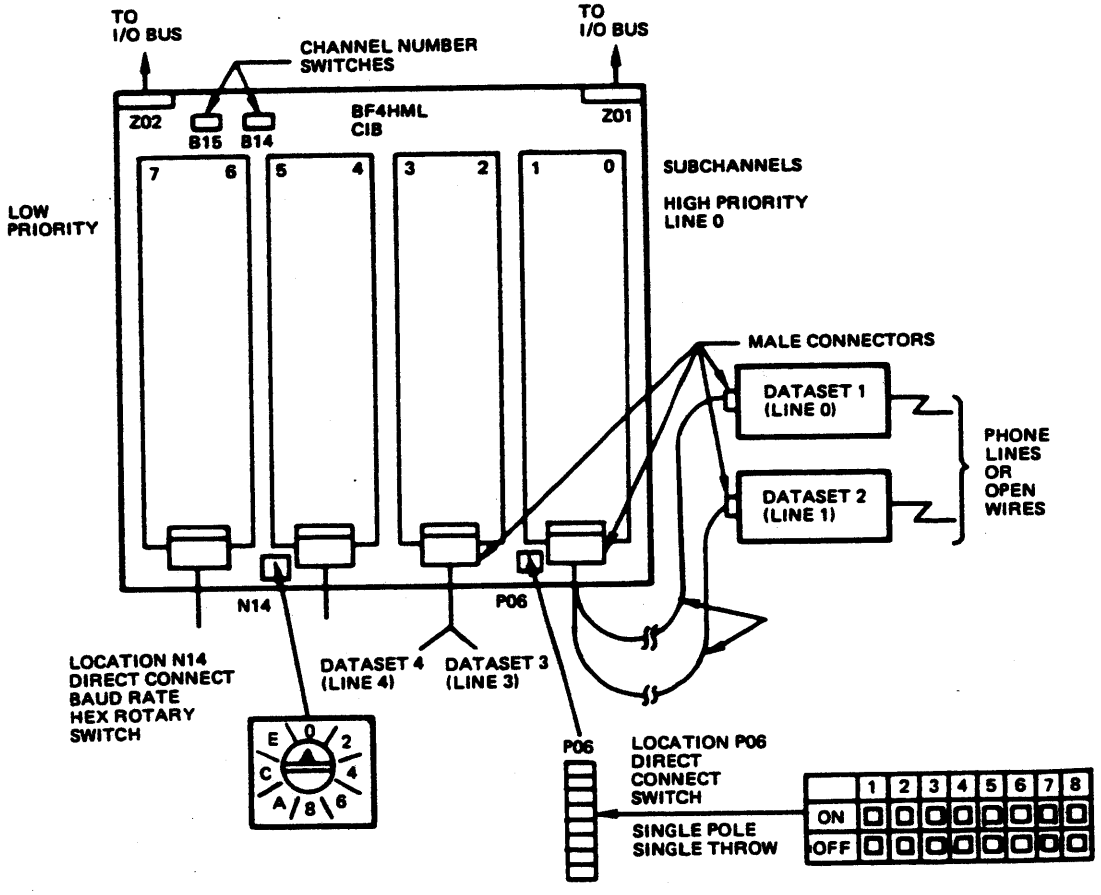


Figure 3-55 CIB Board Layout and Connections to Communications Devices

3.5.11.2 CIB Switch Settings

The CIB has two hexadecimal switches which are to be set as shown in Table 3-10.

Table 3-10 CIB Switch Settings

SWITCH LOCATION B14	B15	CIB NUMBER	TEST CHANNEL NUMBER (Octal)	SUBCHANNEL NUMBER (Octal)
4	0	0	06	0-07
4	2	1	06	10-17
4	4	2	06	20-27
4	6	3	06	30-37
4	8	0	07	0-07
4	A	1	07	10-17
4	C	2	07	20-27
4	E	3	07	30-37
5	0	0	10	0-07
5	2	1	10	10-17
5	4	2	10	20-27
5	6	3	10	30-37

The synchronous direct connect baud rate is set by a hexadecimal rotary switch in location N14 on the CIB board (refer to Table 3-11 for switch settings).

CAUTION

The direct connect switches on the CIB board at location P06 are used only with synchronous operations. If asynchronous operations are used, the appropriate direct connect switch at P06 must be in the OFF position.

Table 3-11 Direct Connect Baud Rate Switch Settings - 60135403 (BMLC005A Only)

SWITCH SETTING (N14)	BAUD RATE (Khz)
0	0.8
1	1.2
2	1.76
3	2.152
4	2.4
5	4.8
6*	9.6
7	19.2
8	28.8
9	32.0
A	38.4
B	57.6
C	76.8

*T&D setting.

NOTE

Direct connect is selected for an individual subchannel by the switch at location P06 of the CIB board. A switch being ON equals direct connect.

Switch 1 = subchannel 0.

Switch 2 = subchannel 1, etc.

3.5.11.3 CIB/HMLC Cabling Installation

The procedure for installing the CIB/HMLC cables follows:

NOTE

Refer to subsection 3.2.3 for the information required to install the bulkhead cabinet.

WARNING

To avoid bodily injury, before removing covers and installing cables, set the ac power switch to OFF and set the PDU circuit breaker to OFF.

1. Remove the side bulkhead (cabinet) covers by removing the screw at the bottom of the cover, using a cross-tip screwdriver. Lift the cover up and remove.

2. Remove the strain relief clamps on the side of the cabinet (see Figure 3-56).

3. Install the cable through the side cutouts, leaving sufficient cable length to connect to the adapter board. Dress the cable loosely through the cable clamps and strain relief areas.

NOTE

A cable that is to be connected to the left of the center of a processor/controller board must exit through the left side of the cabinet and vice versa.

4. When the cable is connected to the correct connector, remove the excess slack in the bulkhead area and reinstall the relief clamps. Tighten the cable clamps and the strain relief clamps.

5. Install the cabinet covers by aligning the pins inside the cover with the two brackets at the top of the cabinet. Insert and tighten the screw at the bottom of the cover.

NOTE

Side cutouts in both the cabinet and the chassis covers make it possible to install and remove system cables without removing the chassis from the cabinet.

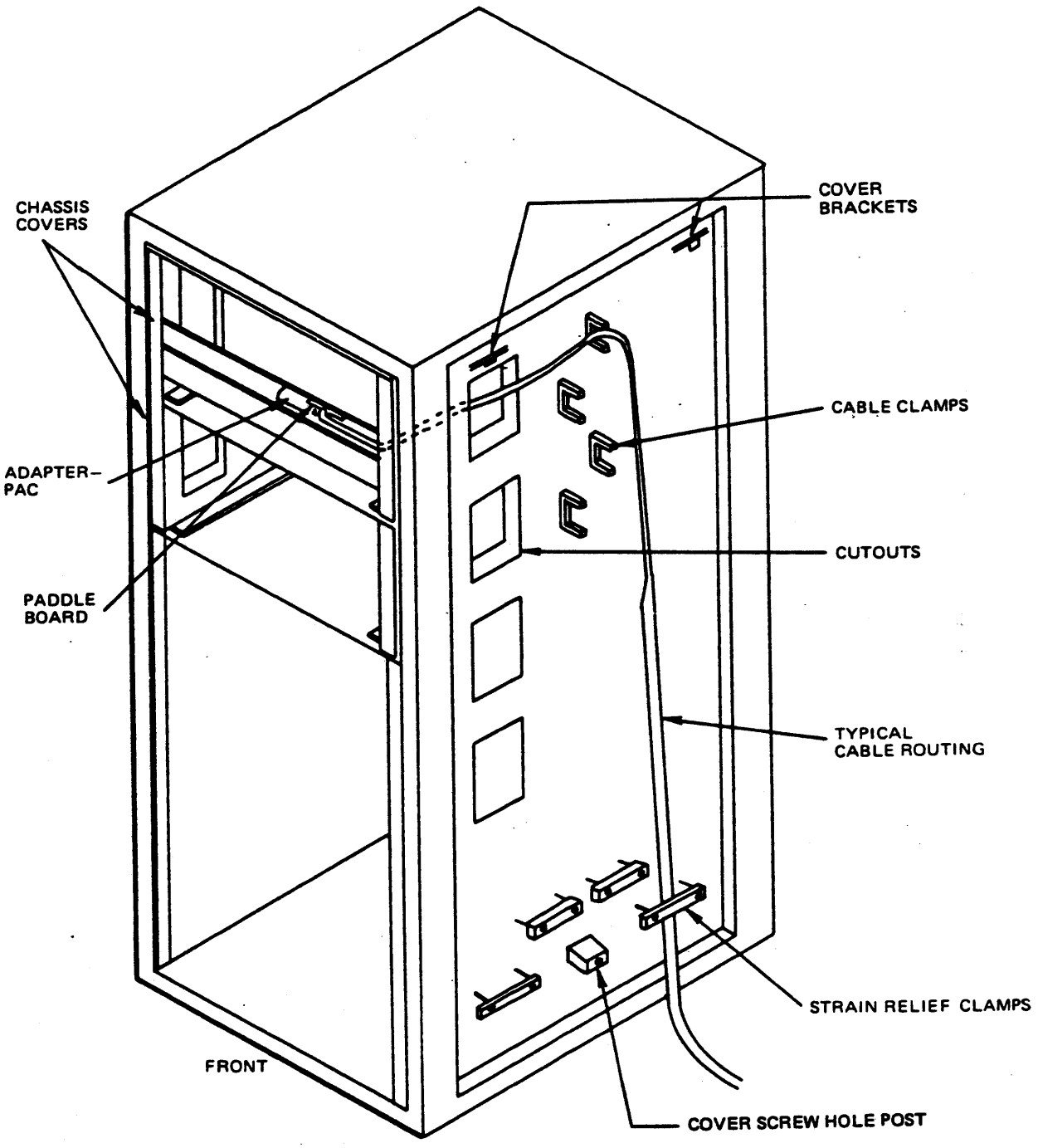


Figure 3-56 CIB and Console Cable Installation

3.5.11.4 DCF6613 Dual Autocall Adapter Switch Settings

The hexadecimal rotary switches for the dual autocall adapter are located at J02 and J03 (see Figure 3-57). Set the switches to correspond with the line numbers of the subchannels associated with the dual autocall adapter (see Table 3-12). Switch J02 is the lower number (higher priority). The use of the dual autocall adapter reduces line connectability by two. The adapter must be in the first or first and second board position on the HMLC.

Table 3-12 Dual Autocall Adapter Switch Settings

LINE NUMBER	SWITCH SETTING
0	1
1	3
2	5
3	7
4	9
5	B
6	D
7	F

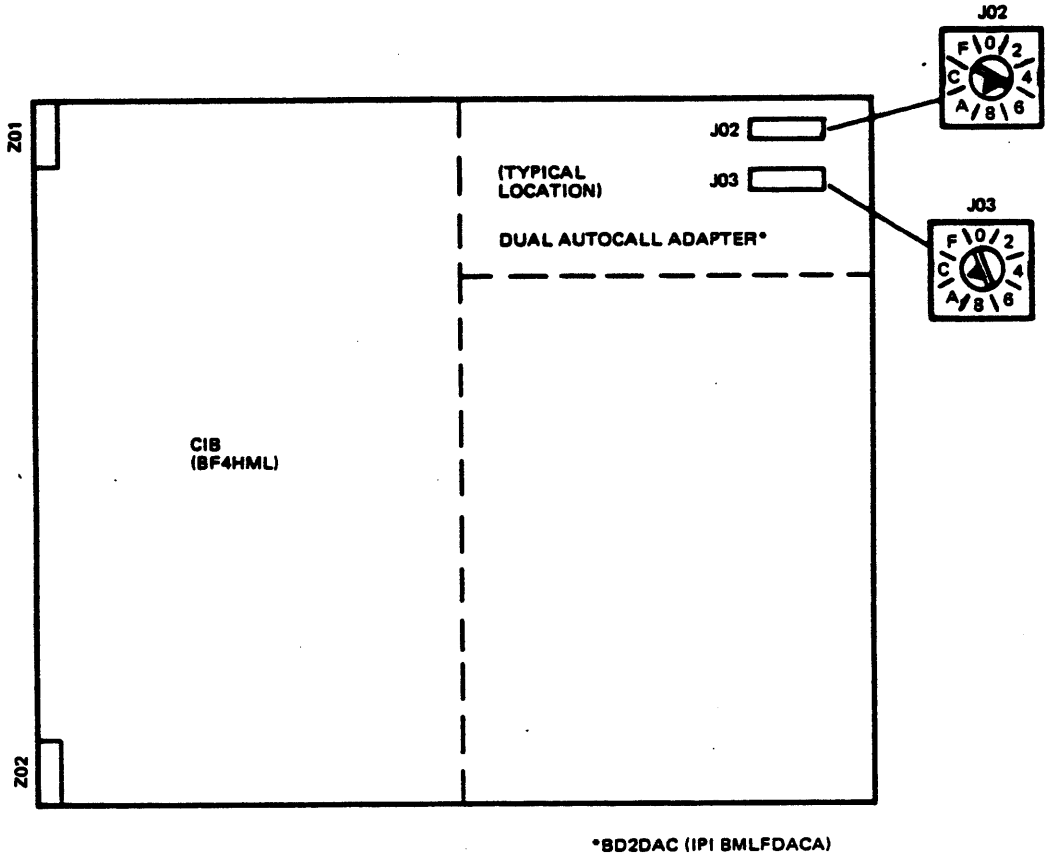


Figure 3-57 Dual Autocall Adapter Switch Locations

3.5.11.5 DCF6610 Dual Current Loop Adapter

The DCF6610 Dual Asynchronous Current Loop Adapter can be configured for 20 or 60 mA at 50 to 9,600 bps. It can be installed on the CIB in any position, subject to the configuration rules in subsection 3.5.2. Figure 3-58 shows the switch settings and IPI numbers. The 20-mA configuration should be used when possible. When the 60-mA configuration is required by the connected device, a maximum of six BD2CIAs (i.e., 12 lines) can be used in any five-card zone.

3.5.11.5.1 Cable Installation in Nonbulkhead System

Cable 60132380 is a 30-foot cable that plugs into the CLA and separates into two EIA connectors (see Figure 3-71 for cable list). Cable 60132385-00X is an extension cable (X indicates the number of 10-foot increments up to 97, 970 feet). Cable 60134581 is also used (refer to Table 3-16 for application).

3.5.11.5.2 Cable Installation in Bulkhead System

Cable 60135450 in the internal cable (refer to Figure 3-75 for the cabling). Cable 60135449 is the external cable (refer to Figure 3-76 for the cabling).

3.5.11.6 MIL-STD-188C Adapter Operation, Capacitor Location, and Selection

This subsection describes the operation, capacitor location, and selection (if required) for the line adapters (CommunicationPacs) designed to operate at levels specified by MIL-STD-188C. The line adapters are:

- DCF6614 Single Synchronous Line Adapter - BD2188 (IPI BMLF188A)
- DCF6615 Dual Asynchronous Line Adapter - BD2A88 (IPI BMLFA88A)
- DCF6616 Broadband Synchronous Line Adapter - BD2B88 (IPI BMLFB88A)
- DCF6617 High-Level Data Link (HDLC) Line Adapter - BD2H88 (IPI BMLFH88A).
- DCF6628 High-Level Data Link (HDLC) MIL-STD-188C Line Adapter - BHMLD8 (IPI BMLFDL8A)

3.5.11.6.1 DCF6614 Line Adapter

The DCF6614 Line Adapter provides an interface for one MIL-STD-188C synchronous full duplex data communications line. Figure 3-59 shows the general layout of the DCF6614, mounted on the CIB. Up to four line adapters can be used with the CIB.

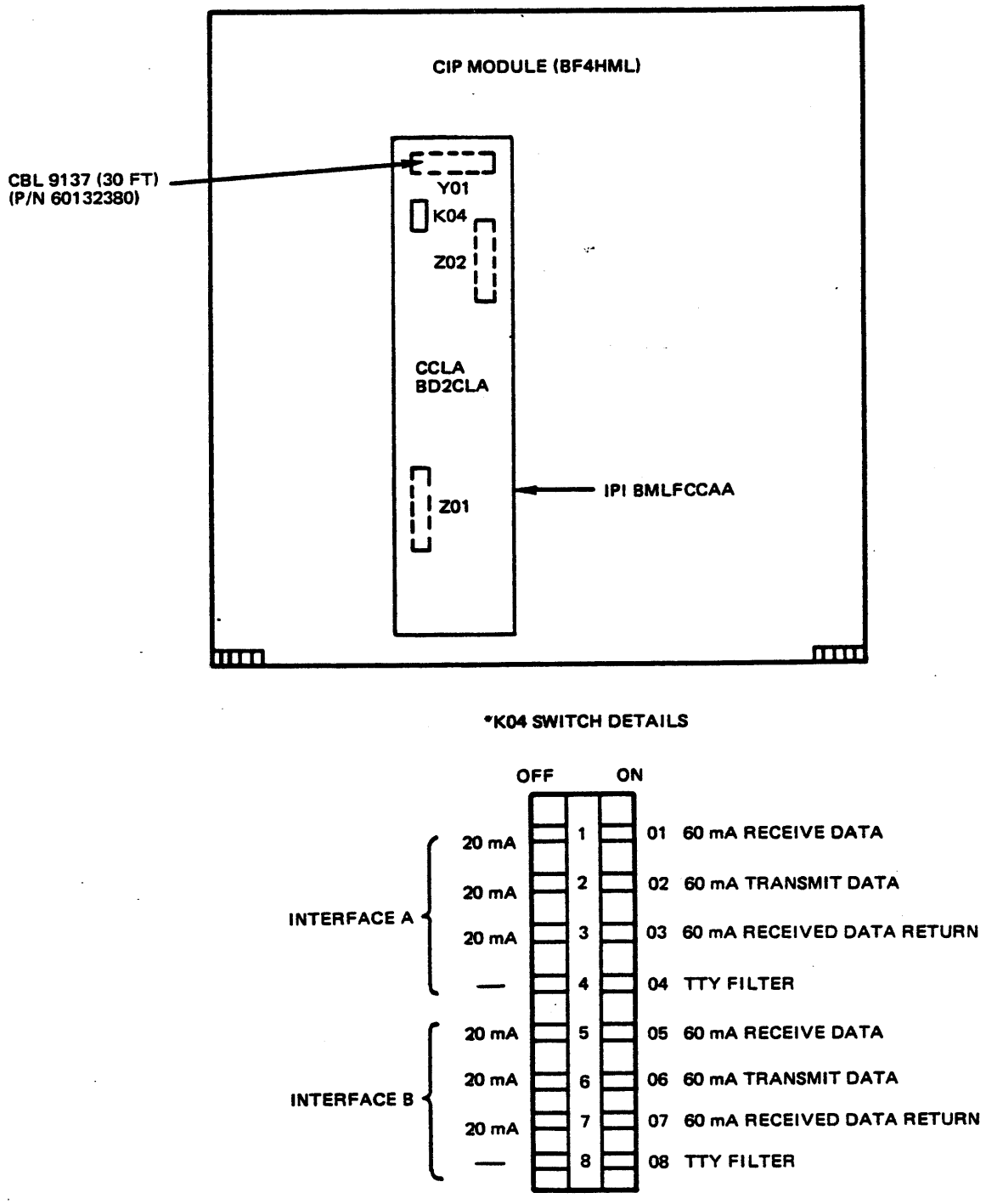
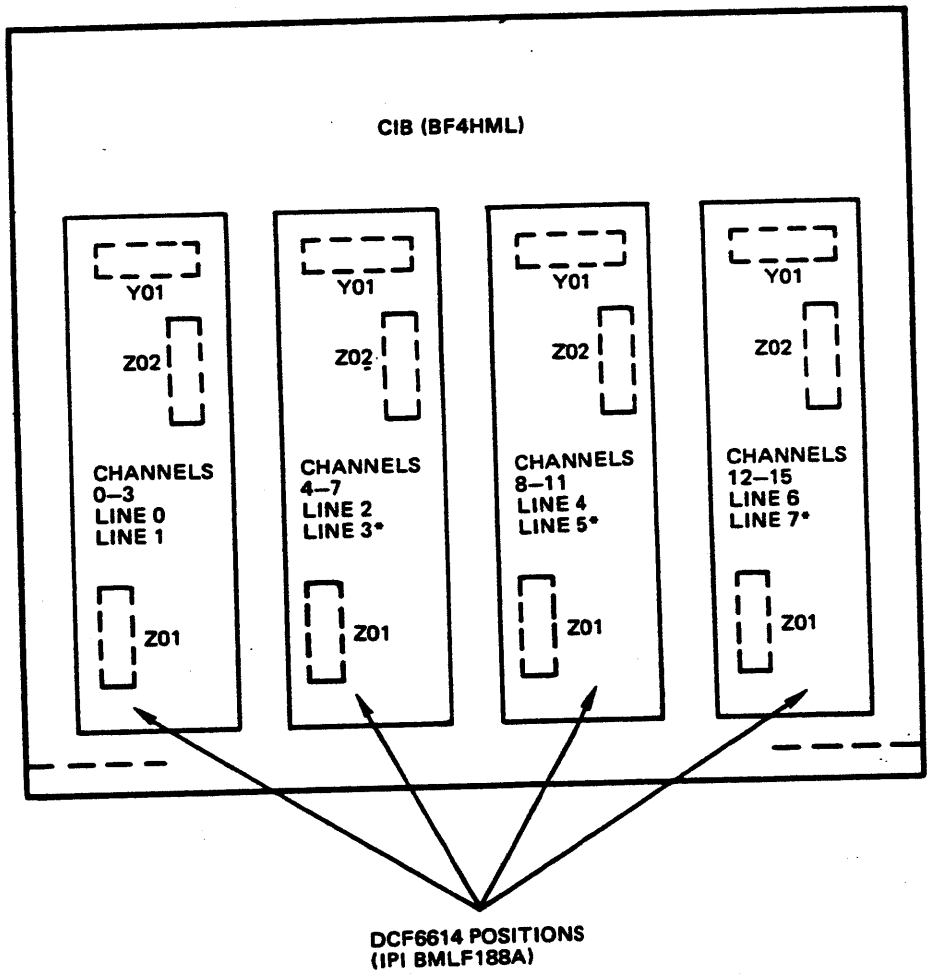


Figure 3-58 Dual CLA Switch and Connector Locations



*IF SINGLE SCLA, SUBCHANNELS 1, 3, 5, AND 7 DO NOT EXIST.

Figure 3-59 DCF6614 Line Adapter, Typical Installation

3.5.11.6.2 DCF6615 Line Adapter

The DCF6615 Line Adapter provides an interface for two MIL-STD-188C full duplex (4-wire) asynchronous communications lines. Figure 3-60 shows the general layout of the DCF6615 Line Adapter, mounted on the CIB. Up to four line adapters can be used with the CIB. Figure 3-60 also shows the location of the capacitors that must be installed on the line adapter for the proper configuration. The value of the capacitors varies in accordance with the Data Communications Equipment (DCE) baud rate. Note the following and select the capacitors:

1. The required capacitor size for output data lines DATXDA- and DATXDB- varies with the baud rates as listed in Table 3-13.

2. Each output control line requires a 0.56 microfarad capacitor regardless of the baud rate.

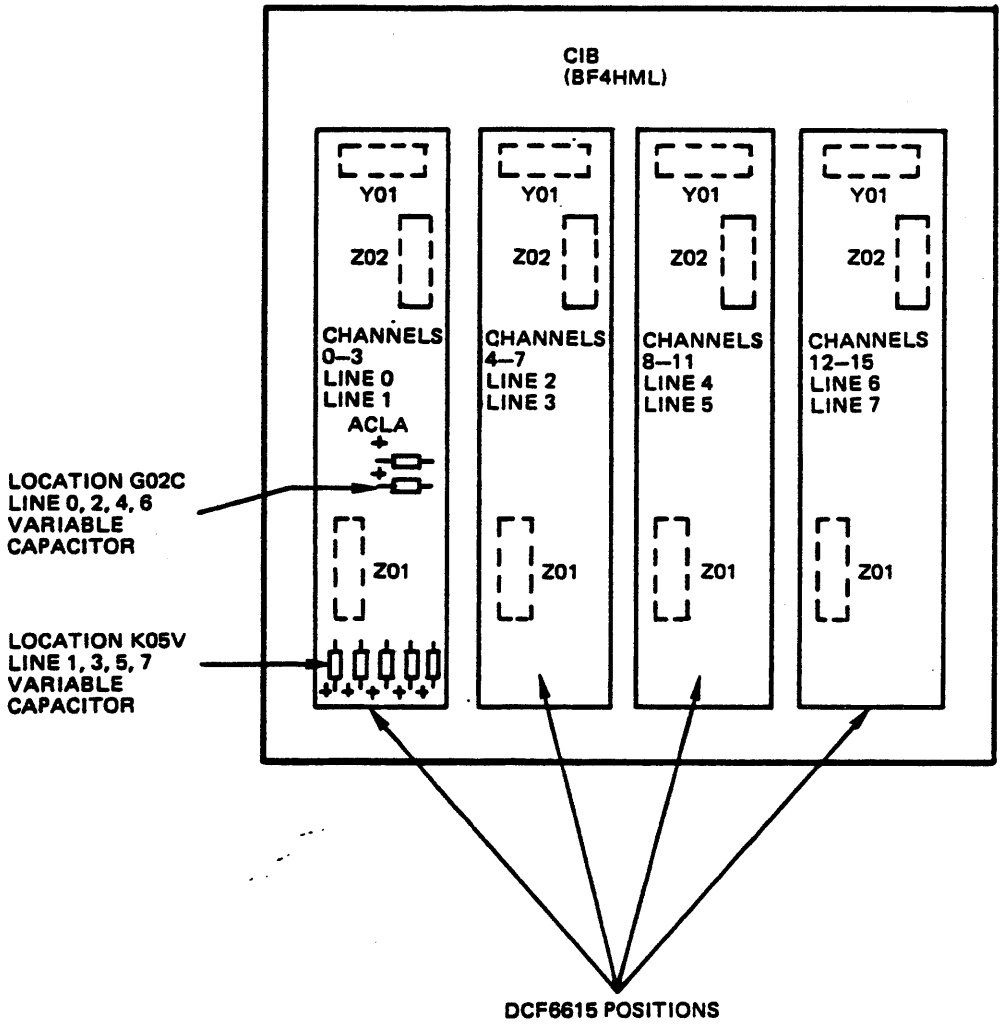


Figure 3-60 DCF6615 Line Adapter, Typical Installation

Table 3-13 Output Data Line* (DATXDA-** and DATXDB-***) Capacitor Selections (DCF6615)

BAUD RATE	CAPACITOR SELECTION	
	VALUE IN MICROFARADS	PART NUMBER
50	4.1	70930246-240
75	2.7	04350031-012
110	2.2	04350031-011
134.5	1.5	04350031-008
150	1.5	04350031-008
200	1.0	04350031-006
300	0.68	04350031-004
600	0.33	04350031-001
1050	0.22	04350016-013
1200	0.18	04350016-012
1800	0.12	04350016-010
2400	0.082	04350016-008
4800	0.047	70930301-114
9600	0.022	04330011-022

*Both output control lines require a 0.56-microfarad capacitor, part number 04350031-003 or 04350023-004, regardless of the baud rate.

**The capacitor for DATXDA- (line 0) is at location G02C (see Figure 3-60).

***The capacitor for DATXDB- (line 1) is at location K05V (see Figure 3-60).

3.5.11.6.3 DCF6616 Line Adapter

The DCF6616 Line Adapter provides an interface for one MIL-STD-188C synchronous full duplex data communications line. Figure 3-61 shows the general layout of the DCF6616, mounted on the CIB. Only one line adapter can be used on a CIB because of its high throughput requirements. It is placed on subchannel 0, which has the highest priority on the CIB. Figure 3-61 also shows the location of the three capacitors that must be installed on the line adapter for the proper configuration. The value of capacitors varies in accordance with the DCE baud rate. Note the following and select the capacitors:

1. Both control signals TRDYDA+ and RQSDDA+ require a 0.56-microfarad capacitor (part number 04350023-004 or 04350031-003) regardless of the mode or baud rate.

2. Both clock signals NSYNDA+ and SPSLDA+, in nondirect connect mode, require a 0.56-microfarad capacitor (part number 04350023-004 and 04350031-003) regardless of the baud rate. In direct connect mode, the capacitor requirements vary according to the baud rates listed in Table 3-14.

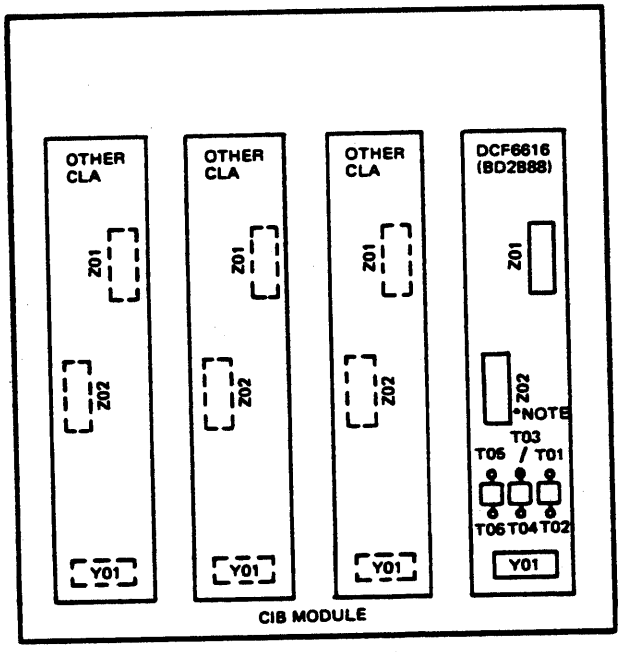
3. Data signal DATXDA+ capacitor values vary according to the baud rates listed in Table 3-14. The baud rate is either a clock signal provided by the DCE or the test clock signal (CLKSYN-) provided by the CIB.

4. Note that the capacitor for DATXDA+ is installed between T01 and T02 (see Figure 3-61), for NSYNDA+ it is installed between T03 and T04, and for SPSLDA+ between T05 and T06.

Table 3-14 Output Signal Capacitor Selection (DCF6616)

BAUD RATE	DATXDA+ (Data to Line)		NSYNDA+ AND SPSLDA+ (Clocks)*	
	CAPACITOR VALUE (microfarad)	PART NUMBER	CAPACITOR VALUE (microfarad)	PART NUMBER
300	0.68	04350031-004	0.082	04350016-008
600	0.33	04350031-001	0.082	04350016-008
1050	0.22	04350016-013	0.082	04350016-008
1200	0.18	04350016-012	0.082	04350016-008
1800	0.12	04350016-010	0.056	04350016-006
2400	0.082	04350016-008	0.047	70930301-114
4800	0.047	70930301-114	0.022	04330011-022
9600	0.022	04330011-022	0.010	76952149-117
19200	0.010	76952149-117	0.0056	76952149-147
40800	0.0056	76952149-147	0.0027	70930702-030
56000	0.0039	76952149-145	0.0018	76952149-141
72000	0.0027	70930702-030	0.0015	04330011-014
	(Between T01 and T02, see Figure 3-61)		(Between both T03 and T04 and T05 and T06, see Figure 3-61)	

*Applies in direct connect mode when NSYNDA+ and SPSLDA+ are used as clock signals from the CIB to the DCE. In nondirect connect mode, a 0.56-microfarad capacitor (part number 04350023-004 or 04350031-003) is required for all baud rates.



NOTE
VALUE OF CAPACITORS VARY DEPENDING UPON BAUD RATE OF LINE.

Figure 3-61 DCF6616 Line Adapter, Typical Installation

3.5.11.6.4 DCF6617 Line Adapter

The DCF6617 Line Adapter provides the following communications line specific functions:

1. Controls the communications line interface dialogs
2. Generates the various types of control sequences for transmission
3. Recognizes various types of control sequences when received
4. Supplies and deletes zeros, as necessary, to provide data field transparency
5. Supplies data and status information to the CIB
6. Provides for data to be wrapped from the CIB to the communications line interface and back to the CIB for test purposes.

Figure 3-62 shows the general layout of the DCF6617, mounted on the CIB. Up to four line adapters can be used with the CIB. Figure 3-62 also shows the location of the three capacitors that must be installed on the line adapter for the proper configuration. The value of the capacitors varies in accordance with the DCE baud rate. Note the following and select the capacitors:

1. Both control signals DCEDTR+ and DCERTS+ require a 0.18-microfarad capacitor (part number 04350016-012) regardless of the mode or baud rate.
2. Direct connect clock signals DCENSZ+ and DCESSZ+ capacitor requirements vary according to the baud rates listed in Table 3-15.
3. Data signal DCETDZ+ capacitor requirements vary according to the baud rates listed in Table 3-15.
4. The baud rates listed in Table 3-15 are determined by the normal clock input from the DCE or the test clock (CLKSYN+) input from the CIB when the direct connect feature is used.

3.5.11.6.5 DCF6628 Line Adapter

The DCF6628 Line Adapter provides an interface for one High-Level Data Link (HDLC) MIL-STD-188C synchronous full duplex data communications line. Figure 3-61.1 shows the general layout of the DCF6628, mounted on the CIB. Only one line adapter can be used on a CIB, because of its high throughput requirements. It is placed on subchannel 0, which has the highest priority on the CIB.

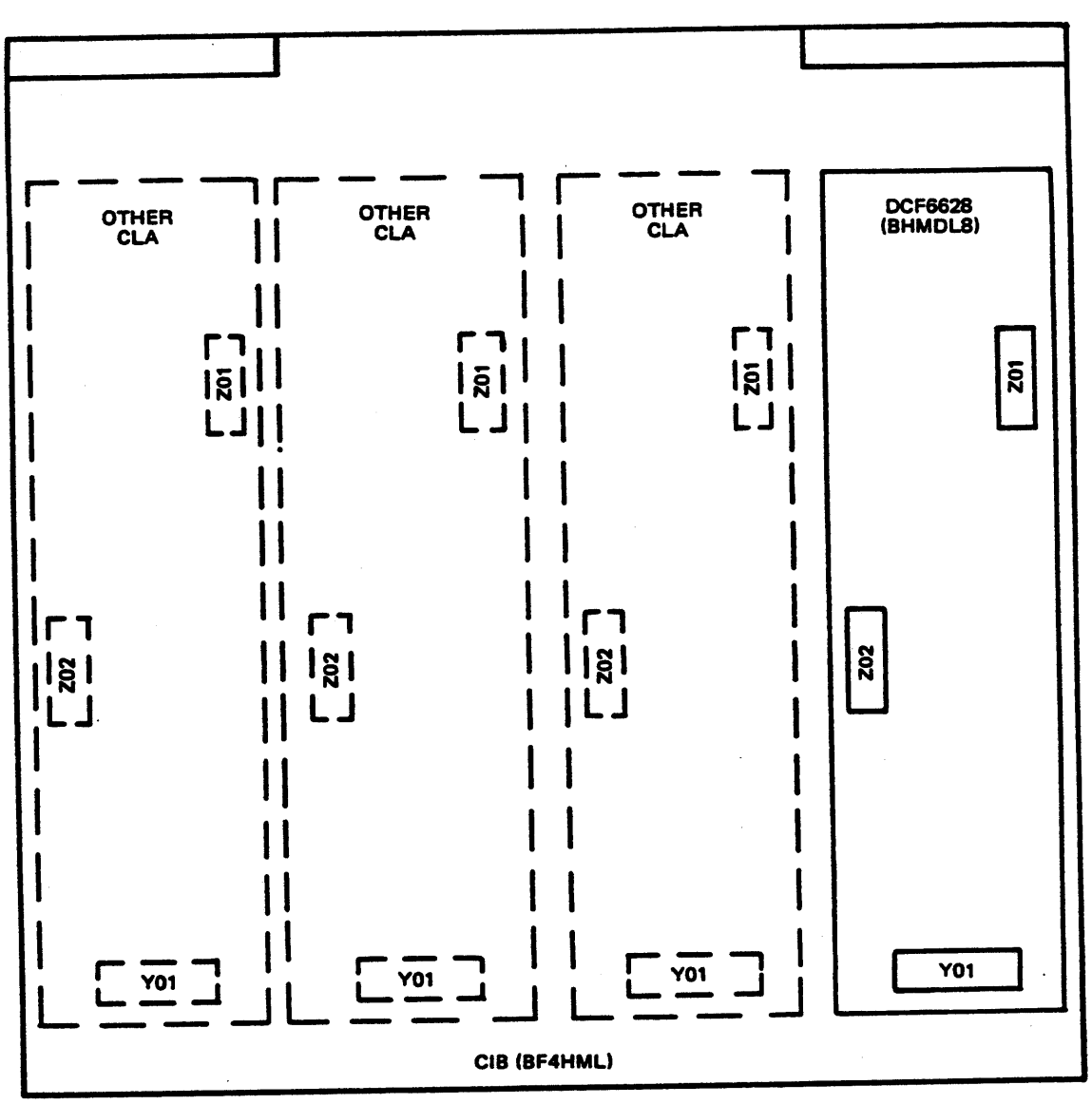


Figure 3-61.1 DCF6628 Line Adapter, Typical Installation

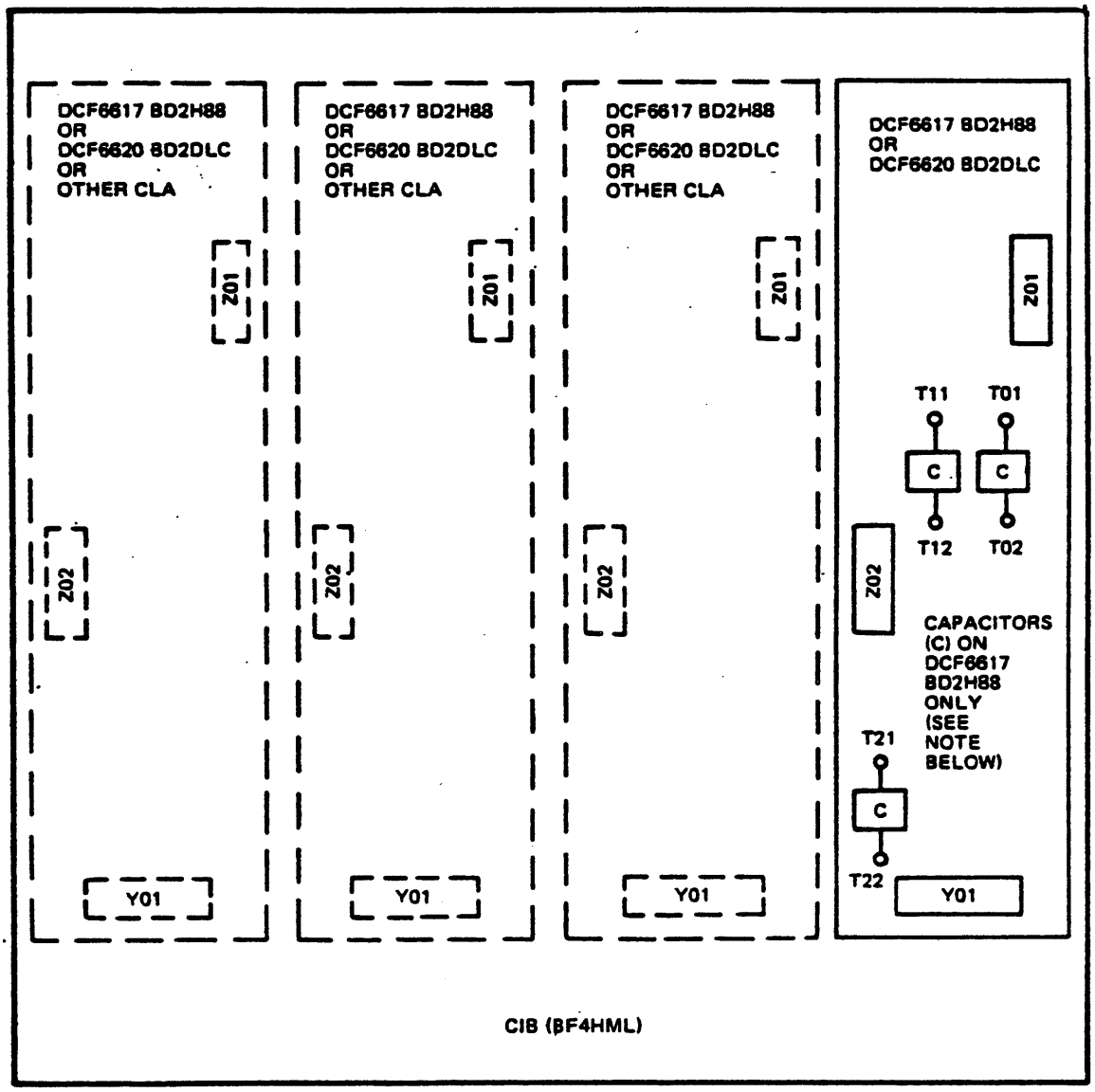
Table 3-15 Output Signal Capacitor Selection (DCF6617)

BAUD RATE	DCETDZ+ (Date to Line)		DCENSZ+ AND DCESSZ+ (Clocks)*	
	CAPACITOR VALUE (microfarad)	PART NUMBER	CAPACITOR VALUE (microfarad)	PART NUMBER
300	0.68	04350031-004	0.082	04350016-008
600	0.33	04350031-001	0.082	04350016-008
1050	0.22	04350016-013	0.082	04350016-008
1200	0.18	04350016-012	0.082	04350016-008
1800	0.12	04350016-010	0.056	04350016-006
2400	0.082	04350016-008	0.047	70930301-114
4800	0.047	70930301-114	0.022	04330011-022
9600	0.022	04330011-022	0.010	76952149-117
	(Installed between T21 and T22, see Figure 3-62)		(Installed between both T01 and T02 and T11 and T12, see Figure 3-62)	

*Applies in direct connect mode when DCENSZ+ and DCESSZ+ are used as clock signals from the adapter to the DCE. In non-direct connect mode, a 0.18-microfarad capacitor (part number 04350016-012) is required.

NOTE

The capacitor for DCETDZ+ is installed between T21 and T22 (see Figure 3-62), for DCENSZ+ it is installed between T11 and T12, and for DCESSZ+ between T02 and T03.



NOTE

THE VALUES OF THESE CAPACITORS VARY WITH THE BAUD RATE OF THE LINE.

Figure 3-62 DCF6617 Line Adapter, Typical Installation

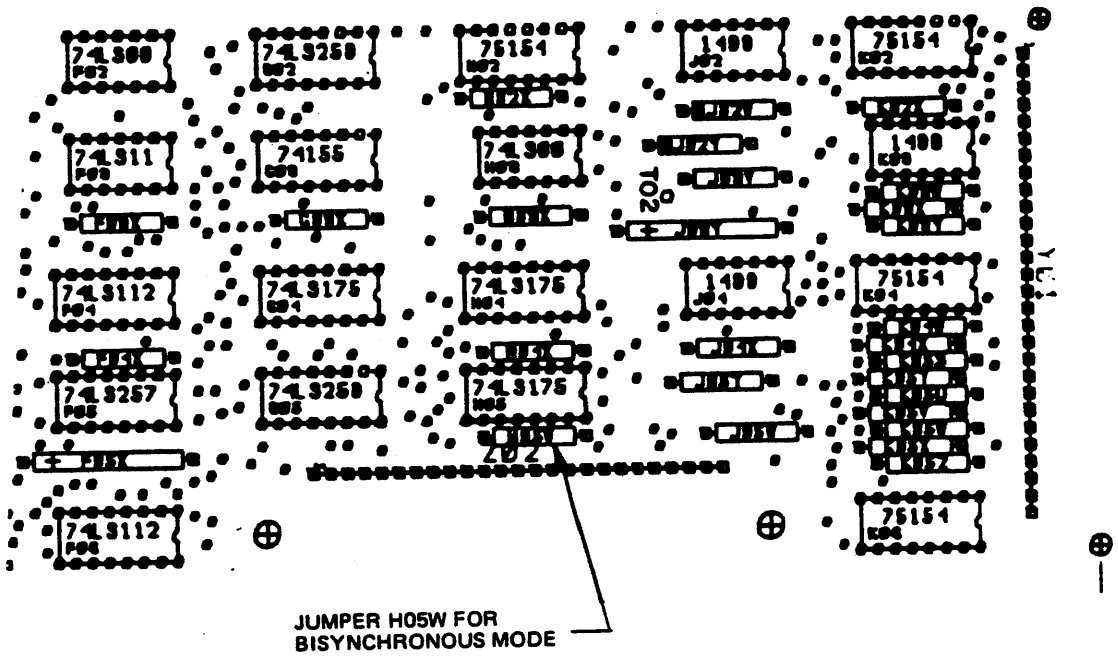
3.5.11.7 CLA/Current Mode Adapter Configuration

The rules for CLA/Current Mode Adapters are as follows:

1. Synchronous dual channel line adapter BD2LAS (IPI BMLF103A) is configured as a bisynchronous dual channel line adapter by a jumper component in loction H05W (see Figure 3-63). The IPI now becomes BMLF618A.

2. The Level 2.1 synchronous broadband channel (current mode) adapter is configured as a bisynchronous broadband channel adapter by a jumper component in location G04W (see Figure 3-64).

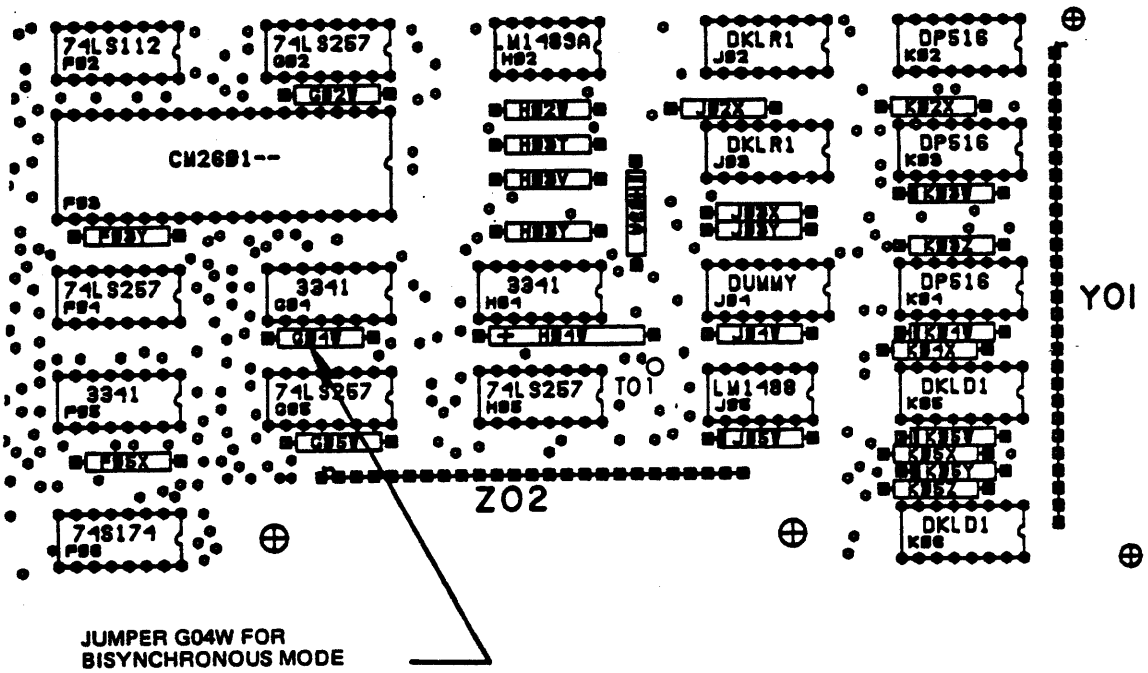
3. The Level 2.2 synchronous broadband channel (current mode) adapter is configured as a bisynchronous broadband channel adapter by a switch in location B03X (see Figure 3-65).



NOTE

JUMPER IS IN FOR OPTION DCF6618 (IPI BMLF618A) BISYNC;
JUMPER IS OUT FOR OPTION DCF6611 (IPI BMLF103A) SYNC.

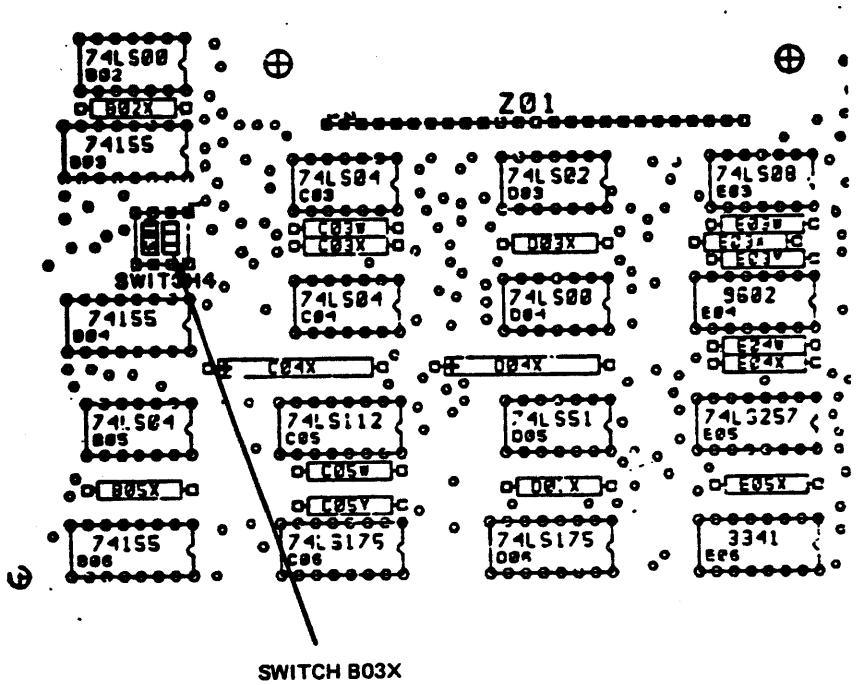
Figure 3-63 BD2LAS Board Jumper Locations



NOTE

JUMPER IS IN FOR OPTION DCF6621 (IPI BMLF619A) BISYNC;
JUMPER IS OUT FOR OPTION DCF6619 (IPI BMLF619A) SYNC.

Figure 3-64 BD2CMD Board (Level 2.1, 60133392) Jumper Locations



NOTE

SWITCH 1 IS OFF, SWITCH 2 IS ON FOR OPTION DCF6619(IPI BMLF619A) SYNC;
SWITCH 1 IS ON, SWITCH 2 IS OFF FOR OPTION DCF6621 (IPI BMLF619A) BISYNC.

Figure 3-65 BD2CMD Board (Level 2.2, 60133410) Jumper Locations

3.5.11.8 DCF6627 Balanced Line Broadband Adapter

The DCF6627 Balanced Line Adapter contains the logic for data handling, control, and interfacing between the CIB and the Bell Digital Data Systems Data Terminal (CCITT-V35) or the equivalent.

Figure 3-66 shows the general layout of the DCF6627 adapter, mounted on the CIB. Up to four line adapters can be used with the CIB.

Set the switches shown on Figure 3-66 as follows:

- 1 = OFF
- 2 = ON
- 3 = OFF } These switch sections
- 4 = OFF } are not connected.

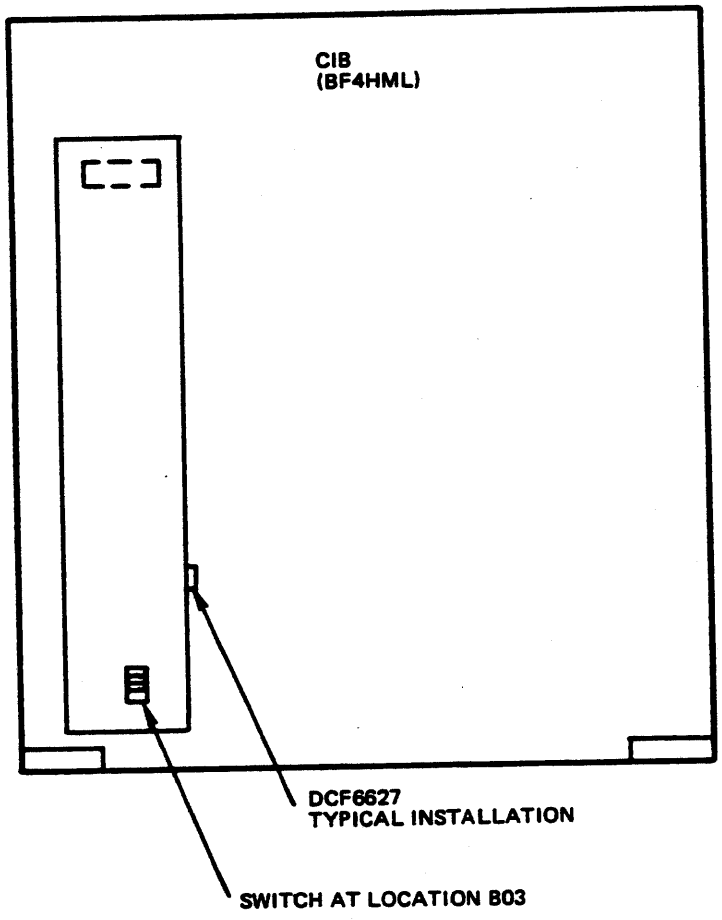


Figure 3-66 DCF6627 Balanced Line Broadband Adapter, Typical Installation and Switch Location

3.5.11.9 Cabling for Communications Devices

After the CIB controllers are installed according to subsection 3.5.2, connect the device cables between the CLAs and the communications devices. Refer to subsection 3.5.11.3 for the proper method of installing the cables.

Figure 3-55 shows the typical communications device to CIB connections. Figure 3-67 shows the direct connect connections. Table 3-16 provides a list of cables, CIB Adapter-Pacs, CLA/DCE, and baud rates. Table 3-17 provides a list of the system configurations. Figure 3-68 shows the wiring of the alternate asynchronous direct connect cable (43C239754G8). The wiring for the cables listed in Table 3-16 is detailed in Figures 3-69 through 3-80 and Tables 3-18 through 3-25.

Table 3-16 CIB Cable Numbers, CLA/DCE, and Baud Rate List (Sheet 1 of 2)

CLA TYPE	COMMUNICATIONS LINE ADAPTER	ORIGINAL CABLE	EXPANDED (BULKHEAD) SYSTEM				LINES SERVICED	ASSOCIATED DCE	BAUD RATE
			INTERNAL CABLE	QTY	EXTERNAL CABLE	QTY			
DCF6610	Dual Async Current Loop Adapter	60132380 & 60132385* 60134581*	60135450-001	1	60135449-001	2	2	Terminal Display Equipment	9,600
DCF6611	Dual Sync Line Adapter	60128704	60140527-001	1	04910129-003	2	2	Bell System 201, 203, or 208 modem	10,800
DCF6612	Dual Async Line Adapter	60128704	60140527-001	1	04910129-003	2	2	Bell System 103, 112, 113, or 202 modem	9,600
DCF6613	Dual Autocall Unit	60128738	60140528-001	1	04910129-003	2	2	Bell System 801A, 801C Autocall Units	10
DCF6614	MIL-STD-188C Sync Line Adapter	60128629	60140527-001	1	04910129-003	1	1	DCE with MIL-STD-188C Interface	10,800
DCF6615	MIL-STD-188C Async Line Adapter	60128704	60140527-001	1	04910129-003	2	2	MIL-STD-188C Data Set or Terminal	9,600
DCF6616	MIL-STD-188C Broad-band Adapter	60128629	60140527-001	1	04910129-003	1	1	MIL-STD-188C Data Set or Terminal	72,000
DCF6617	MIL-STD-188C HDLC Adapter	60128629	60140527-001	1	04910129-002	1	1	DCE with RS-232-C Function-ality with MIL-STD-188C	10,800
DCF6618	Dual Bisync Line Adapter	60128704	60140527-001	1	04910129-003	2	2	Bell System 201, 203, or 208 modem	10,800
DCF6619	Sync Current Mode Adapter	60128596	60135766-001	1	60135767-002	1	1	Bell System 301 or 303 modem	72,000
DCF6620	HDLC Adapter	60128629	60140527-001	1	04910129-003	1	1	Bell System 201, 203, or 208 modem	10,800
DCF6621	Bisync Current Mode Adapter	60128596	60135766-001	1	60135767-002	1	1	Bell System 301 or 303 modem	72,000

Table 3-16 CIB Cable Numbers, CLA/DCE, and Baud Rate List (Sheet 2 of 2)

CLA TYPE	COMMUNICATIONS LINE ADAPTER	ORIGINAL CABLE	EXPANDED (BULKHEAD) SYSTEM				LINES SERVICED	ASSOCIATED DCE	BAUD RATE
			INTERNAL CABLE	QTY	EXTERNAL CABLE	QTY			
DCF6622	HDLC Current Mode Broadband Adapter	60128596	60135766-001	1	60135767-002	1	1	Bell System 301 or 303 modem	72,000
DCF6623	HDLC Broadband Balanced Line Adapter	60128744	60135457-001	1	60135458-002	1	1	Bell System DDS Terminal CCITT-V35 Interface, 72KB or below	72,000
DCF6624	Async Direct Connect FE-MA **Async Direct Connect FE-FE	59413148(W13) 60135146-001	-	-	-	-	-	-	-
DCF6625	Sync Direct Connect FE-MA ***Sync Direct Connect FE-FE	60128767-001 (W17) 60128766(W18)	-	-	-	-	-	-	
DCF6627	Balanced Line Broadband Adapter (CCITT-V35)	60128744	60135457-001	1	60135458-002	1	1	Bell System DDS Terminal CCITT-V35 Interface, 72KB or below	10,800
DCF6628	MIL-STD-188C HDLC Broadband Balanced Line Adapter	-	60140527-001	1	04910129-002	1	1	MIL-STD-188C Data Set or Terminal 72KB or below	72,000

*These are extension cables.
**43C239754G8 is a direct substitute and includes reverse channel capability. If a reverse channel is not required, 59400546 (W8) can be used.
***If the system is not the clock source, the async cables can be used provided a clock is on pins 15 and 17 (RS-232-C).

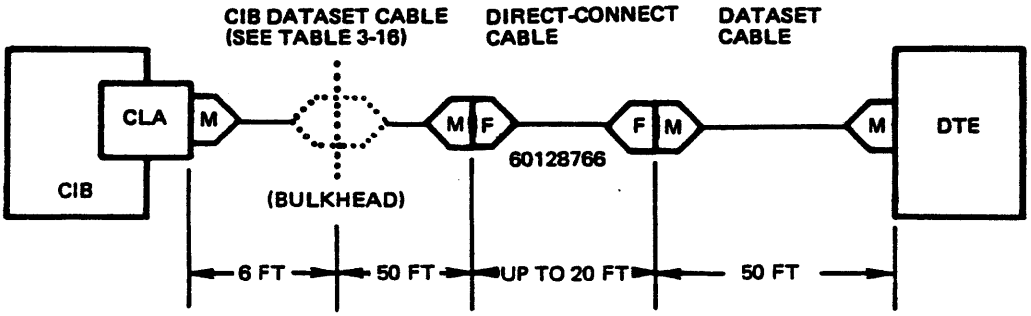
Table 3-17 System Configuration Chart

MKT. OPTION NO. FOR:	MKT. OPTION NO. FOR:	IPI NUMBER	BOARD TYPE	BOARD SIZE	ID CODE*	NUMBER OF CHANNELS	ASYNC/ SYNC	BAUD RATE	COMMENTS
CPS6050	DCP6616	-	-	-	-	-	-	-	-
CPS6058	DCP6624	-	-	-	-	-	-	-	-
CPS8802	DCP6632	-	-	-	-	-	-	-	-
DCU6641	-	-	-	-	-	-	-	-	-
DCU6651	-	-	-	-	-	-	-	-	-
DCP6678	-	-	-	-	-	-	-	-	-
DCU6661	-	-	-	-	-	-	-	-	-
DCF6610	DCF6011	BMLFCLAA	B2DCLA	1/4	02	2	Async	9,600	20/60 mA
DCF6611	DCF6013,6014,6060	BMLF103A	BD2LAS	1/4	13	2	Sync	10,800	EIA
DCF6612	DCF6010	BMLF101B	BD2ASC	1/4	03	2	Async	9,600	EIA
DCF6613	DCF6014,6062	BMLFDACA	BD2DAC	1/4	04	2	-	10	ACU
DCF6614	DCF6012,6053	BMLF188A	BD2188	1/4	14	1	Sync	10,800	MIL-STD-188C
DCF6615	DCF6039	BMLFA88A	BD2A88	1/4	00	2	Async	9,600	MIL-STD-188C
DCF6616	DCF6048	BMLF616A	BD2B8D	1/4	11	1	Sync	72,000	MIL-STD-188C Broadband
DCF6616	-	BMLFB88B	BD2B88	Replaced by BLMFB88A		-	-	-	-
DCF6617	DCF6050	BMLFH88A	BD2H88	1/4	-	1	Sync	10,800	MIL-STD-188C HDLC
DCF6618	-	BMLF103A	BD2LAS	Replaced by BMLF618A		-	-	-	-
DCF6618	DCF6015,6062	BMLF618A	BD2LAS	1/4	12	2	Sync	10,800	BSC
DCF6619/21	DCF6016,6055	BMLF619A	BD2CMD	1/4	7/6	1	Sync	72,000	Current Mode/BSC
DCF6619/21	-	BMLFCMSA	BD2CMS	Replaced by BMLF619A		-	-	-	-
DCF6620	DCF6019,6053	BMLFDLCA	BD2DLC	1/4	10	1	Sync	10,800	EIA HDLC
DCF6622	DCF6054	BMLFDLDA	BH4DLD	1/2	366***	1	Sync	72,000	EIA HDLC Broadband
DCF6623	DCF6058	BMLFDLEA	BH4DLE	1/2	367***	1	Sync	72,000	CCITT-V35 HDLC
DCF6627	-	BMLFBLSA	BD2BLS	Replaced by BMLF627A		-	-	-	-
DCF6627**	DCF6060	BMLF627A	BD2BLD	1/4	15	2	Sync	10,800	CCITT-V35 Broadband
DCF6628	-	BMLFDL8A	BHMDL8	1/4	370***	1	Sync	72,000	MIL-STD-188C HDLC Broadband

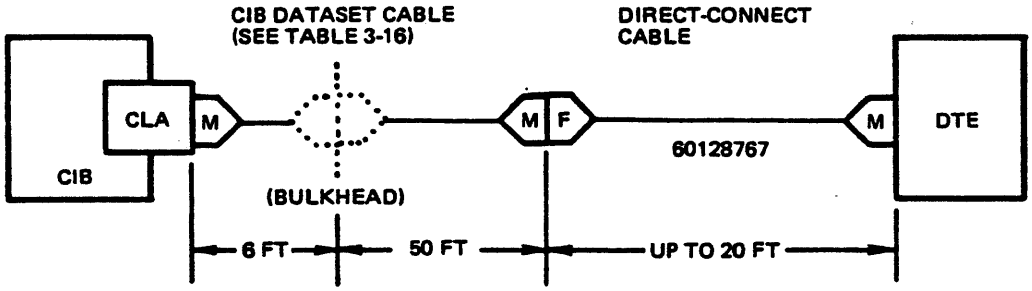
*The configuration status stored in memory has an octal 40 added to the ID to signify the HMLC connection and an octal 20 added if connected to an ACU.

**DCF6627 can be replaced by BMLFBLSB.

***Extended IDs. LR0 Bit 2 of the Configuration Status Byte = 1.



A. DIRECT CONNECT CABLING CONFIGURATION (FEMALE/FEMALE)



B. DIRECT CONNECT CABLING CONFIGURATION (FEMALE/MALE)

Figure 3-67 Typical CIB Sync or Async Direct Connections to Terminal

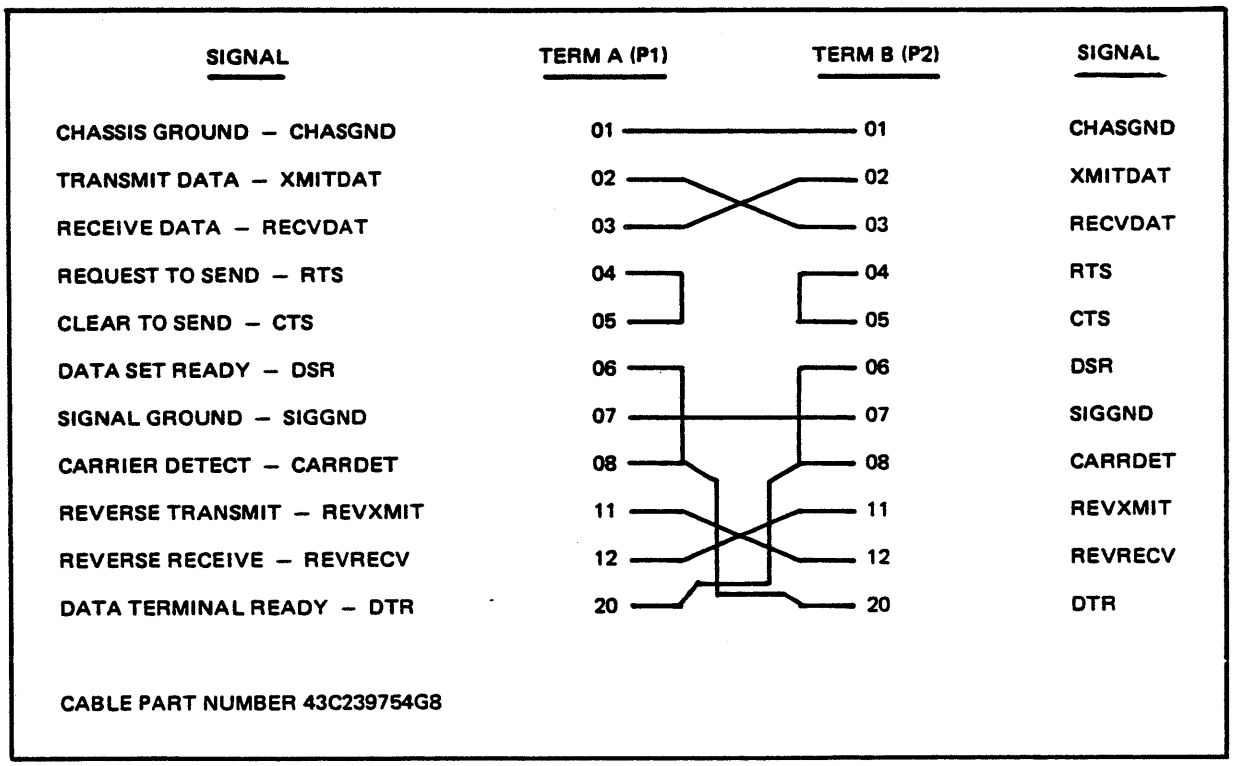


Figure 3-68 Wiring of Alternate Async Direct Connect Cable

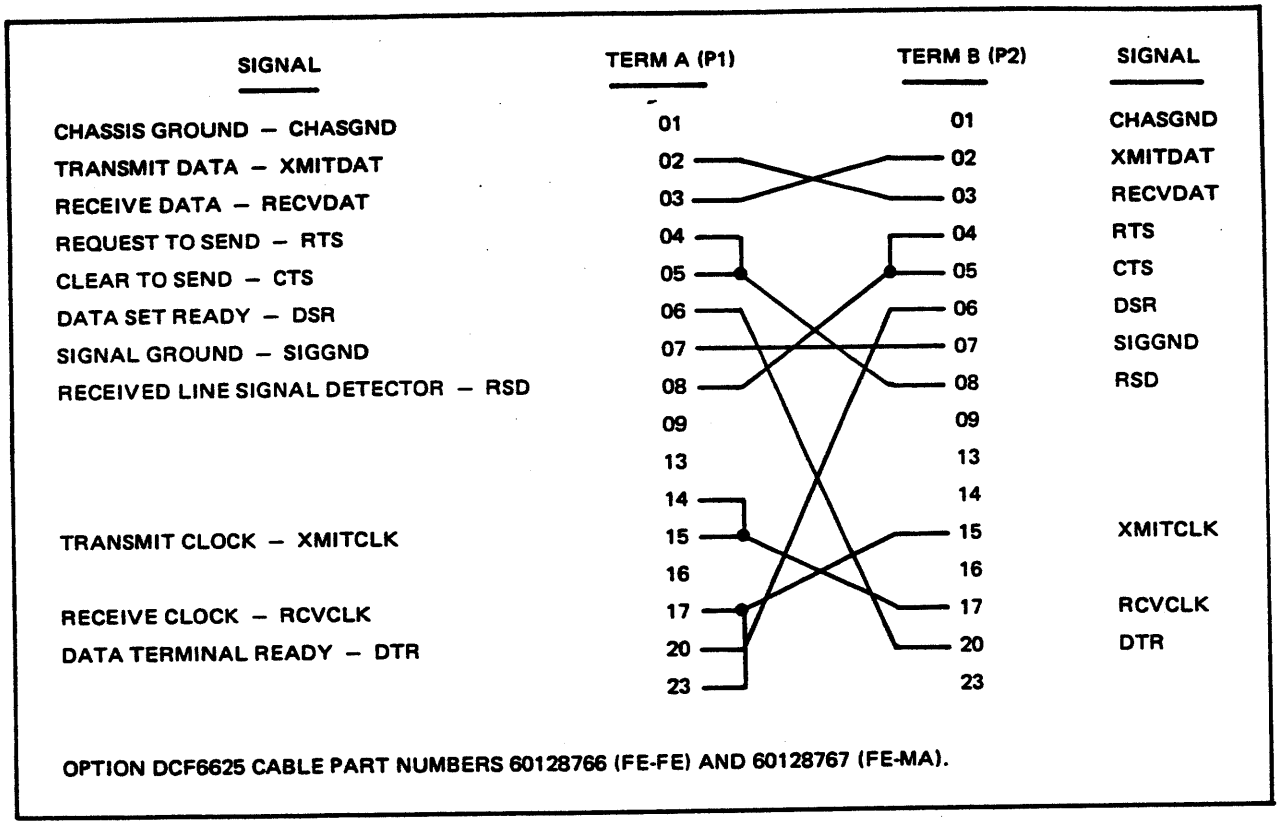


Figure 3-69 Wiring of Sync Direct Connect Cables

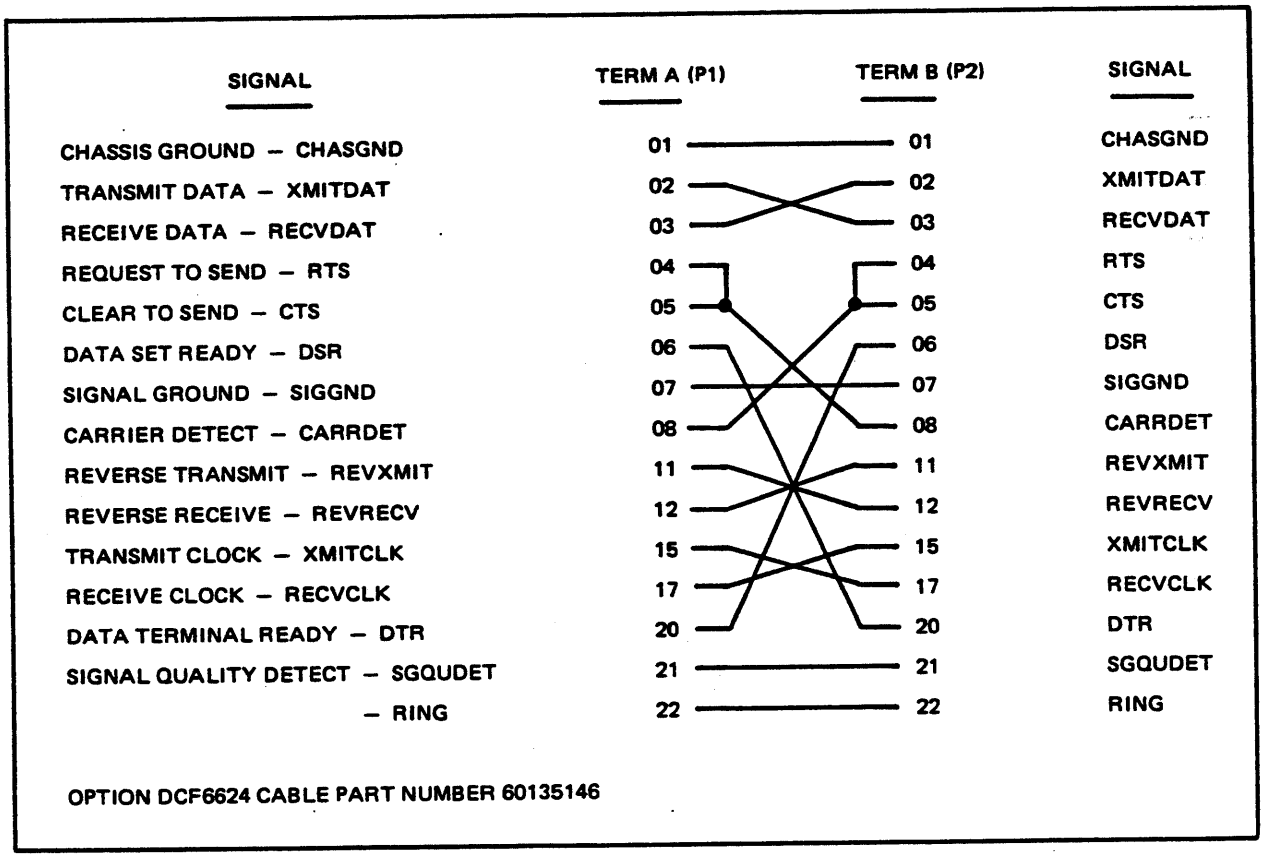


Figure 3-70 Wiring of Async Direct Connect Cables

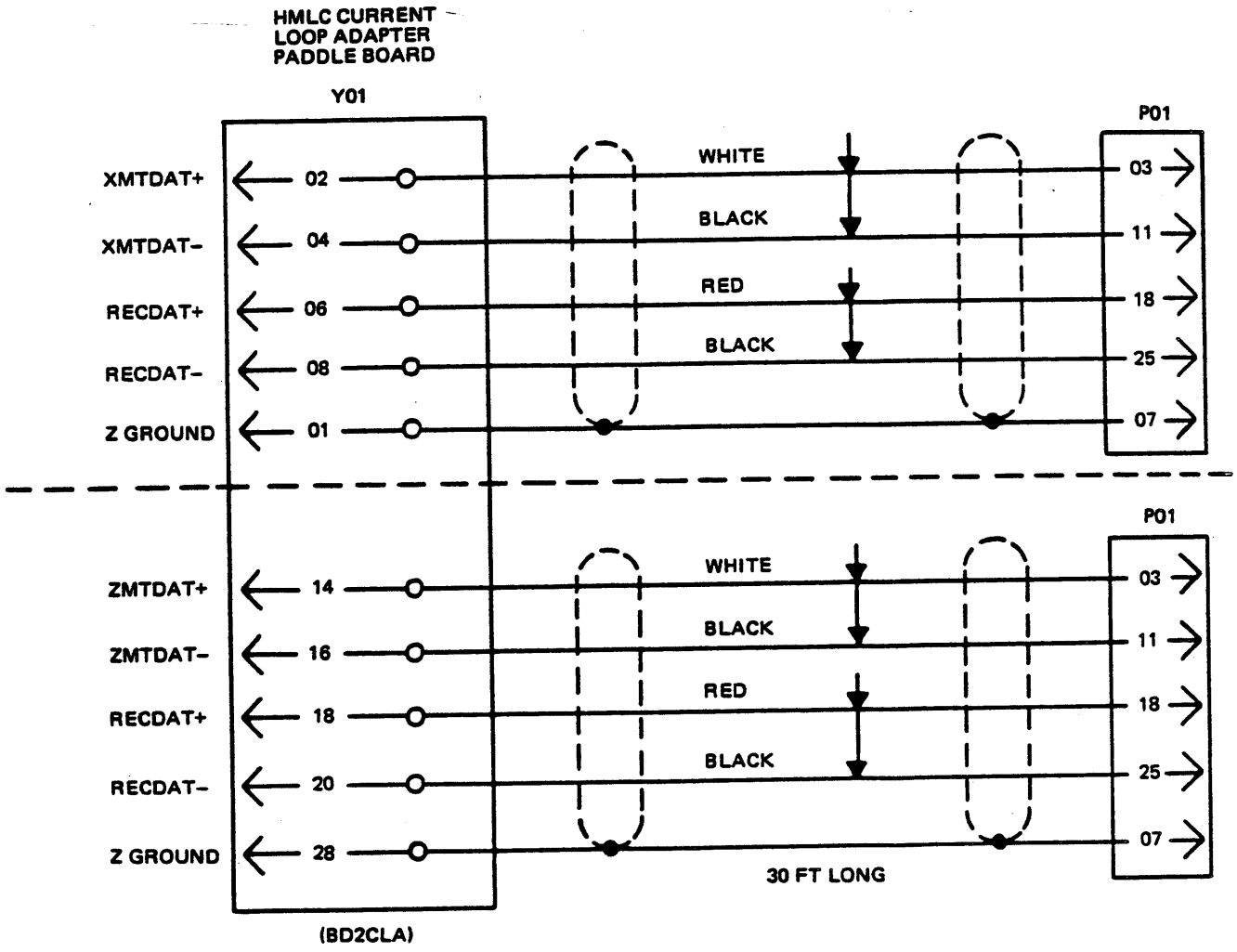


Figure 3-71 Wiring of Current Loop Adapter Cable (60132380-001)

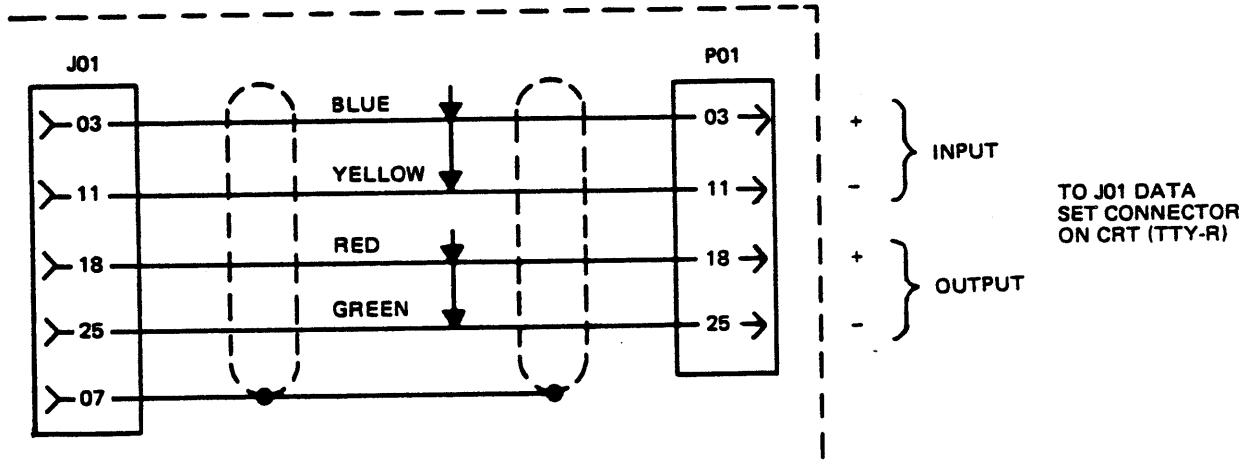


Figure 3-72 Wiring of Current Loop Extension Cable (60132385-001 to 097)

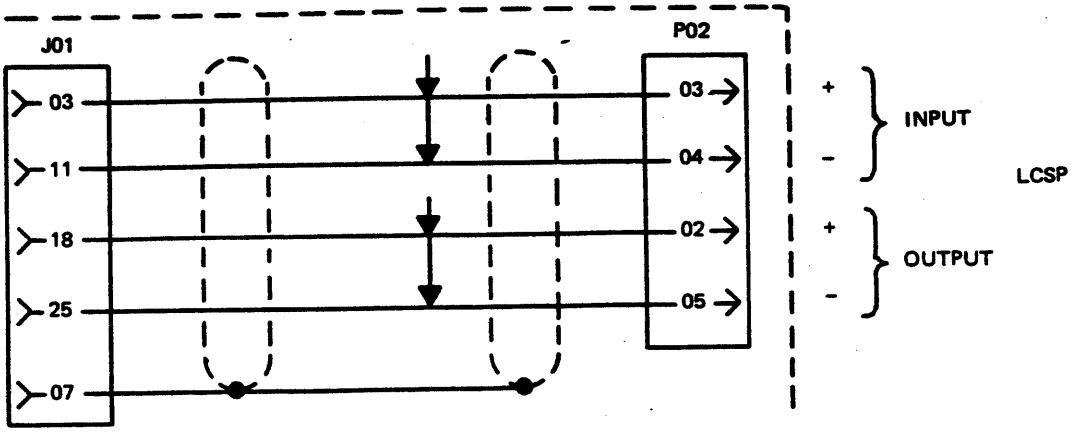


Figure 3-73 Wiring of Current Loop Extension Cable (60134581-001 to -097)

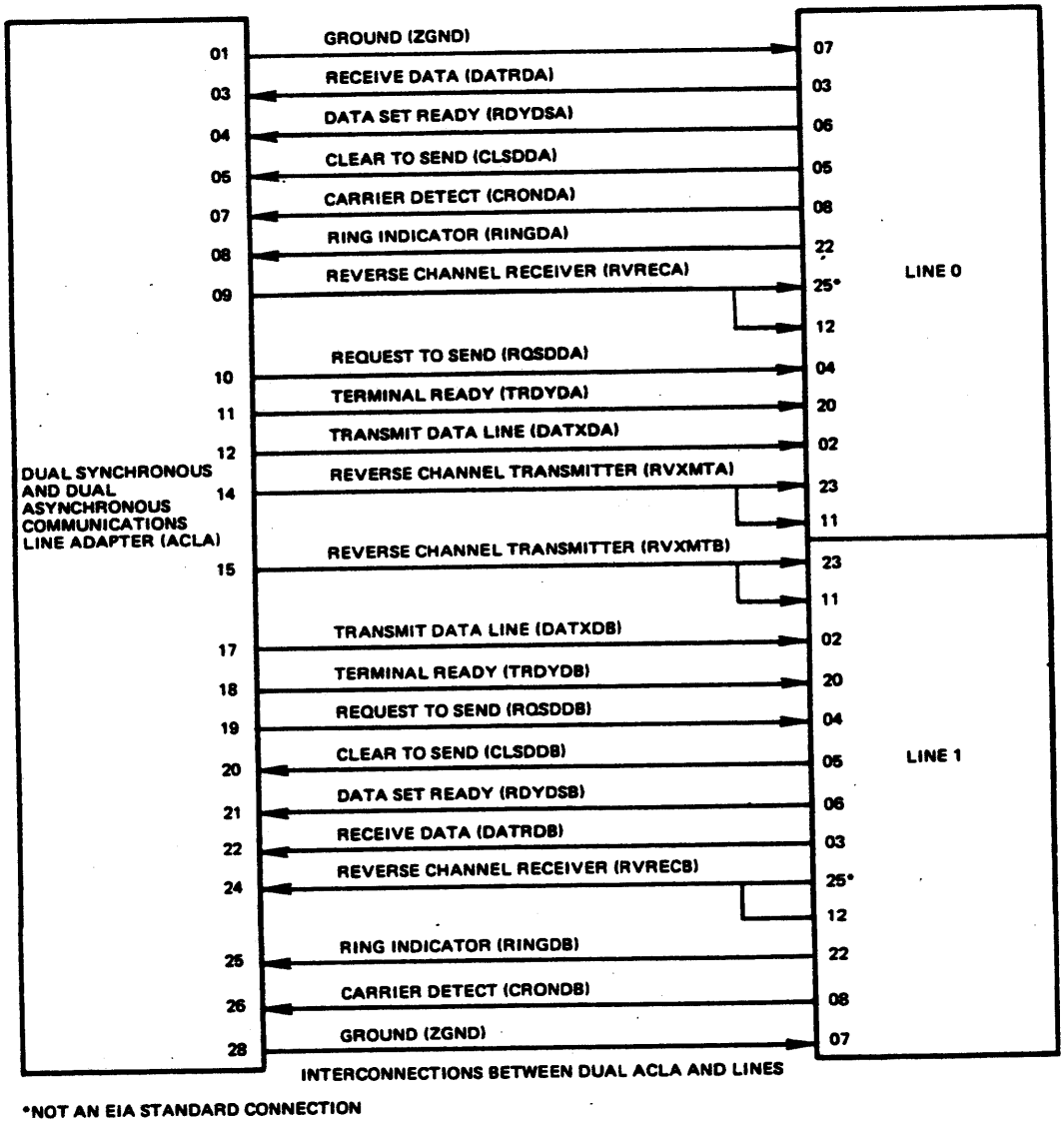


Figure 3-74 Wiring of Dual Sync Line Adapter Cable (60128704)

Table 3-18 Wiring of Dual Autocall Cable (60128738-002)

TERMINAL A	TERMINAL B	ATT-A	ATT-B	FUNCTION
A-02	D-02	-	-	ACDPRA+
A-01	D-07	X07A	X10A	GND
A-03	D-03	-	-	ACACRA+
A-01	D-07	X07A	X10A	GND
A-04	D-04	-	-	ACCRQA+
A-01	D-07	X07A	X10A	GND
A-05	D-05	-	-	ACPNDA+
A-01	D-07	X07A	X10A	GND
A-06	D-06	-	-	ACPWIA+
A-01	D-07	X07A	X10A	GND
A-07	D-13	-	-	ACCOSA+
A-01	D-07	X07A	X10A	GND
A-09	D-14	-	-	ACNB1A-
A-01	D-07	X07A	X10A	GND
A-10	D-15	-	-	ACNB2A-
A-01	D-07	X07A	X10A	GND
A-11	D-16	-	-	ACNB4A-
A-01	D-07	X07A	X10A	GND
A-12	D-17	-	-	ACNB8A-
A-01	D-07	X07A	X10A	GND
A-13	D-22	-	-	ACDLOA+
A-01	D-07	X07A	X10A	GND
A-16	F-22	-	-	ACDLOB+
A-28	F-07	X07B	X10B	GND
A-17	F-17	-	-	ACNB8B-
A-28	F-07	X07B	X10B	GND
A-18	F-16	-	-	ACNB4B-
A-28	F-07	X07B	X10B	GND
A-19	F-15	-	-	ACNB2B-
A-28	F-07	X07B	X10B	GND
A-20	F-14	-	-	ACNB1B-
A-28	F-07	X07B	X10B	GND
A-22	F-13	-	-	ACCOSB+
A-28	F-07	X07B	X10B	GND
A-23	F-06	-	-	ACPWIB+
A-28	F-07	X07B	X10B	GND
A-24	F-05	-	-	ACPNDB+
A-28	F-07	X07B	X10B	GND
A-25	F-04	-	-	ACCRQB+
A-28	F-07	X07B	X10B	GND
A-26	F-03	-	-	ACACRB+
A-28	F-07	X07B	X10B	GND
A-27	F-02	-	-	ACDPRA+
A-28	F-07	X07B	X10B	GND
A-01	SHLD-TAP	-	X07A	GND
A-28	SHLD-TAP	-	X07B	GND
D-07	SHLD-TAP	-	X10A	GND
F-07	SHLD-TAP	-	X10B	GND

Table 3-19 Wiring of MIL-STD-188C Sync Cable (60128629-001)

TERMINAL A	TERMINAL B	FUNCTION
A-02	B-17	RECCLK
A-01	B-07	GRD
A-03	B-03	RECDATA
A-01	B-07	GRD
A-04	B-06	DSRDY
A-01	B-07	GRD
A-05	B-05	CLSEND
A-01	B-07	GRD
A-06	B-15	XMTCLK
A-01	B-07	GRD
A-07	B-08	CARRON
A-01	B-07	GRD
A-08	B-22	RING
A-01	B-07	GRD
A-09	B-25	STANDBY
A-01	B-07	GRD
A-10	B-04	REQSEND
A-01	B-07	GRD
A-11	B-20	TERRDY
A-01	B-07	GRD
A-12	B-02	XMTDATA
A-01	B-07	GRD
A-13	B-14	NEWSYNC
A-01	B-07	GRD
A-14	B-23	SPEEDSL
A-01	B-07	GRD
A-01	B-01	-

Table 3-20 Wiring of Sync Current Mode Adapter Cable (60128596)

TERMINAL A	TERMINAL B	FUNCTION
A-06	B-EX	DATXMT-
A-01	B-EY	-
A-14	B-KX	DATREC+
A-28	B-KY	-
A-22	B-DX	RQSEND+
A-28	B-DY	-
A-25	B-CX	CLSEND+
A-28	B-CY	-
A-26	B-FX	SETRDY+
A-24	B-FY	RINGDA+
A-27	B-MX	CARDET+
A-20	B-MY	TRDYDA+
A-02	B-JX	CLKXMT+
A-01	B-JY	-
A-08	B-BX	SPARE
A-01	B-BY	-
A-10	B-LX	CLKREC+
A-01	B-LY	-
A-16	B-GX	LOCTST+
A-28	B-GY	-
A-04	B-HX	CLKEXT+
A-12	B-HY	CLKEXT-

Table 3-21 Wiring of Broadband Line Adapter (60128744)

TERMINAL A	TERMINAL B	FUNCTION
A-27	B-0C	RQSEND+
A-GD	B-0B	GND
A-21	B-0D	CCSEND+
A-GD	B-0B	GND
A-23	B-0F	CARDET+
A-GD	B-0B	GND
A-22	B-0E	SETRDY+
A-GD	B-0B	GND
A-18	B-05	DATXMT+
A-19	B-0P	DATXMT-
A-14	B-0R	DATRBL+
A-16	B-0T	DATRBL-
A-10	B-0V	CLKRBL+
A-12	B-0X	CLKRBL-
A-02	B-0Y	CLKXBL+
A-04	B-AA	CLKXBL-
A-06	B-0U	XMTCLK+
A-08	B-0W	XMTCLK-
A-26	B-0H	TRDYDA+
A-GD	B-0B	GND
A-20	B-0J	RINGDA+
A-GD	B-0B	GND

FN01

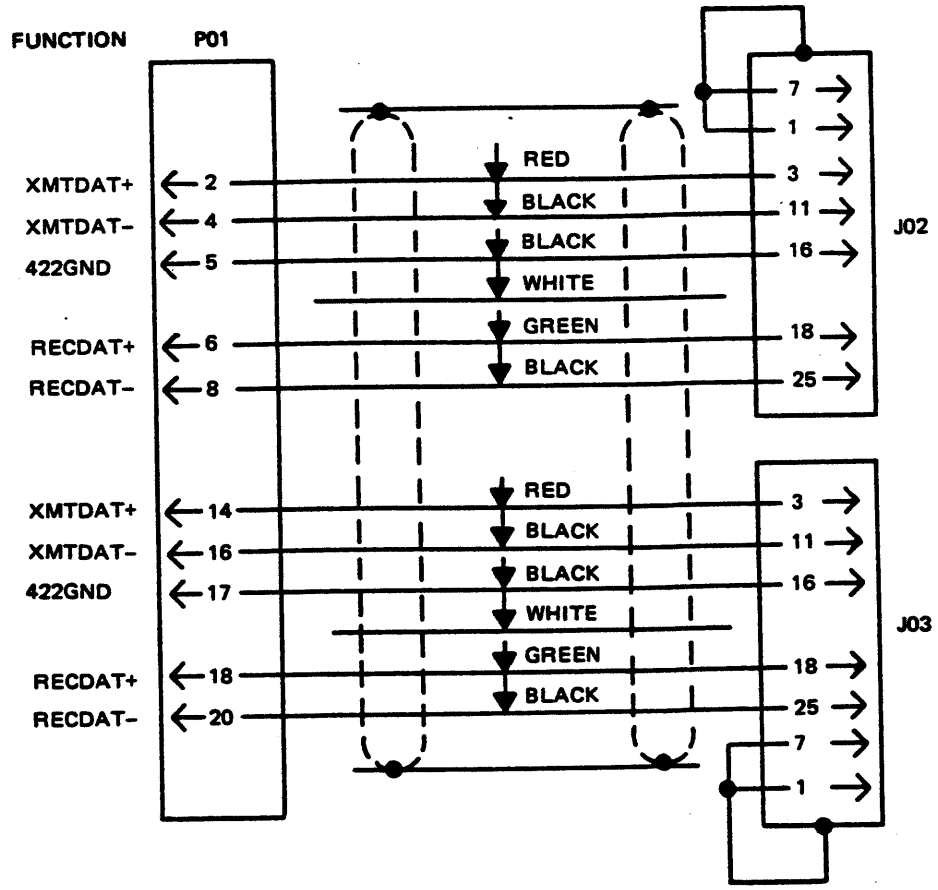


Figure 3-75 Wiring of Dual Current Loop Internal Cable (60135450)

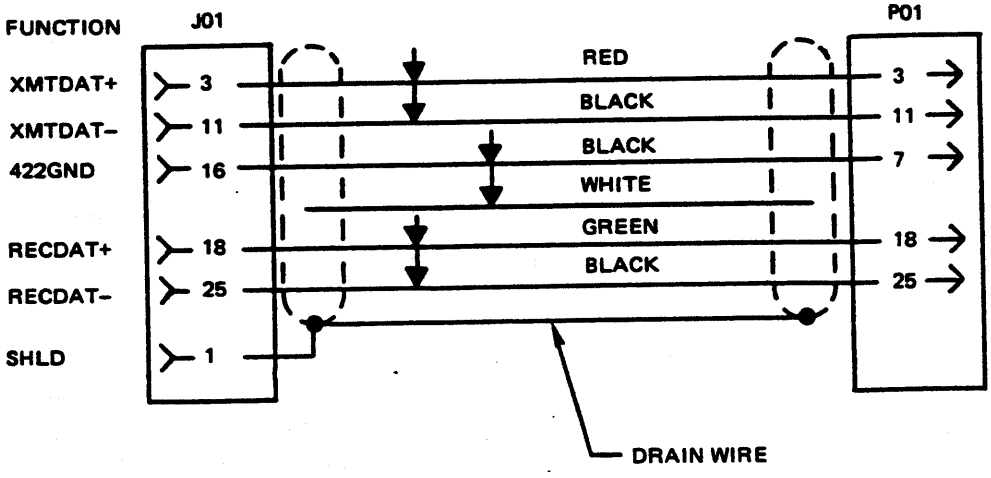


Figure 3-76 Wiring of Dual Current External Cable (60135449)

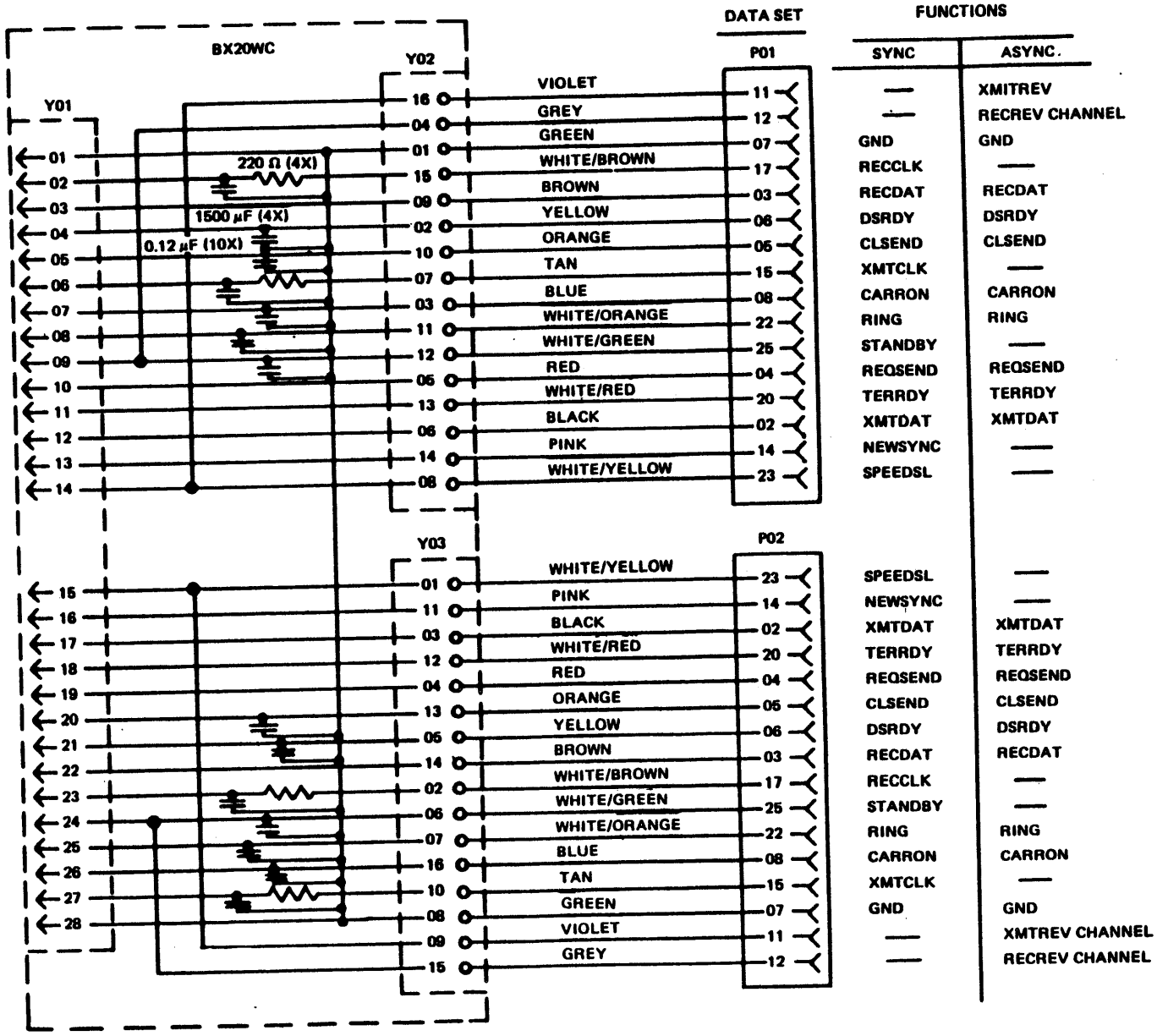


Figure 3-77 Wiring of Sync and Async Internal Cable (60140527)

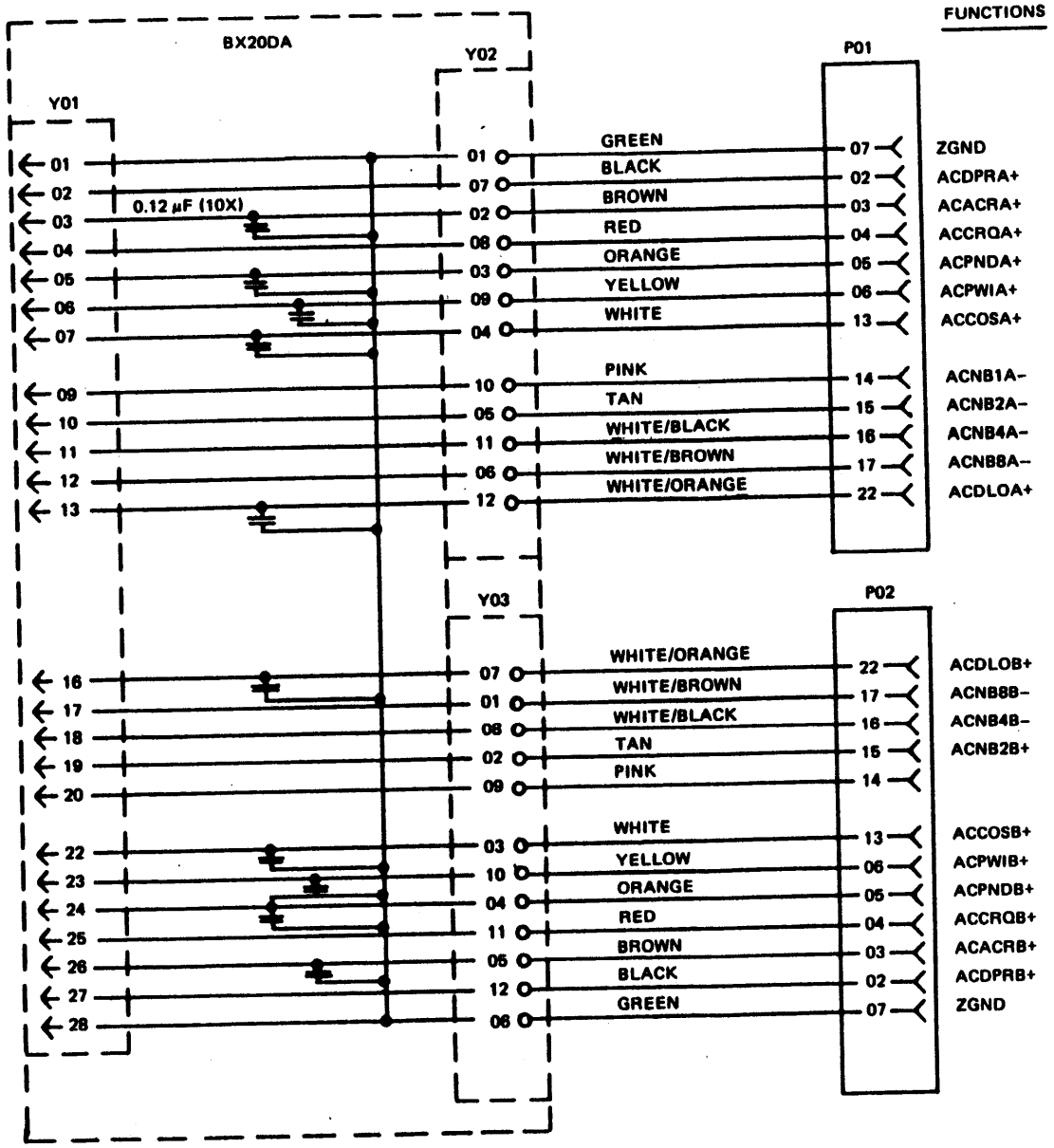


Figure 3-78 Wiring of Dual Autocall Internal Cable (60140528)

Table 3-22 Wiring of Sync Current Mode Adapter Internal Cable (60135766)

TERMINAL A	TERMINAL B	FUNCTION
A-06	J-0101	DATXMT-
A-01	J-0102	GND
A-14	J-0103	DATREC+
A-28	J-0104	GND
A-22	J-0105	RQSEND+
A-28	J-0106	GND
A-25	J-0107	CLSEND+
A-28	J-0108	GND
A-26	J-0109	SETRDY+
A-24	J-0110	RINGDA+
A-27	J-0111	CARDET+
A-20	J-0112	TRDYDA+
A-02	J-0113	CLKXMT+
A-01	J-0114	GND
A-08	J-0115	SPARE
A-01	J-0116	GND
A-10	J-0117	CLKPEC+
A-01	J-0118	GND
A-16	J-0119	LOCTST+
A-28	J-0120	GND
A-04	J-0121	CLKEXT+
A-12	J-0112	CLKEXT-

Table 3-23 Wiring of HDLC V35/DDS Internal Cable (60135457)

TERMINAL A	TERMINAL B	FUNCTION
A-27	J-0101	RQSEND+
A-01	J-0102	GND
A-21	J-0103	CCSEND+
A-01	J-0104	GND
A-23	J-0105	CARDET+
A-01	J-0106	GND
A-22	J-0107	SETRDY+
A-01	J-0108	GND
A-18	J-0109	DATXMT+
A-19	J-0110	DATXMT-
A-14	J-0111	DATRBL+
A-16	J-0112	DATRBL-
A-10	J-0113	CLKRBL+
A-12	J-0114	CLKRBL-
A-02	J-0115	CLKXBL+
A-04	J-0116	CLKXBL-
A-06	J-0117	XMTCLK+
A-08	J-0118	XMTCLK-
A-26	J-0119	TRDYDA+
A-01	J-0120	GND
A-20	J-0121	RINGDA+
A-01	J-0122	GND

FN01

Table 3-24 Wiring of HDLC Current Mode External Cable (60135767)

TERMINAL A	TERMINAL B	FUNCTION
P-0101	B-EX	DATXMT-
P-0102	B-EY	GND
P-0103	B-KX	DATREC+
P-0104	B-KY	GND
P-0105	B-DX	RQSEND+
P-0106	B-DY	GND
P-0107	B-CX	CLSEND+
P-0108	B-CY	GND
P-0109	B-FX	SETRDY+
P-0110	B-FY	RINGDA+
P-0111	B-MX	CARDET+
P-0112	B-MY	TRDYDA+
P-0113	B-JX	CLKXMT+
P-0114	B-JY	GND
P-0115	B-BX	SPARE
P-0116	B-BY	GND
P-0117	B-LX	CLKPEC+
P-0118	B-LY	GND
P-0119	B-GX	LOCTST+
P-0120	B-GY	GND
P-0121	B-HX	CLKEXT+
P-0122	B-HY	CLKEXT-

Table 3-25 Wiring of HDLC V35/DDS External Cable (60135458)

TERMINAL A	TERMINAL B	FUNCTION
P-0101	B-0C	RQSEND+
P-0102	B-0B	GND
P-0103	B-0D	CCSEND+
P-0104	B-0B	GND
P-0105	B-0F	CARDET+
P-0106	B-0B	GND
P-0107	B-0E	SETRDY+
P-0108	B-0B	GND
P-0109	B-0S	DATXMY+
P-0110	B-0P	DATXMT-
P-0111	B-0R	DATRBL+
P-0112	B-0T	DATRBL-
P-0113	B-0V	CLKRBL+
P-0114	B-0X	CLKRBL-
P-0115	B-0Y	CLKXBL+
P-0116	B-AA	CLKXBL-
P-0117	B-0U	XMTCLK+
P-0118	B-0W	XMTCLK-
P-0119	B-0H	TRDYDA+
P-0120	B-0B	GND
P-0121	B-0J	RINGDA+
P-0122	B-0B	GND

FN01

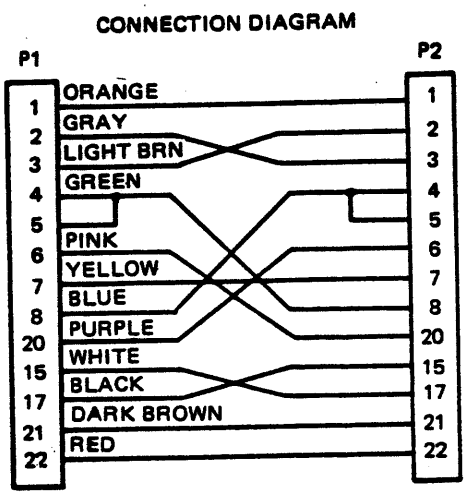


Figure 3-79 Wiring of Async Direct Connect Cable (59413148)

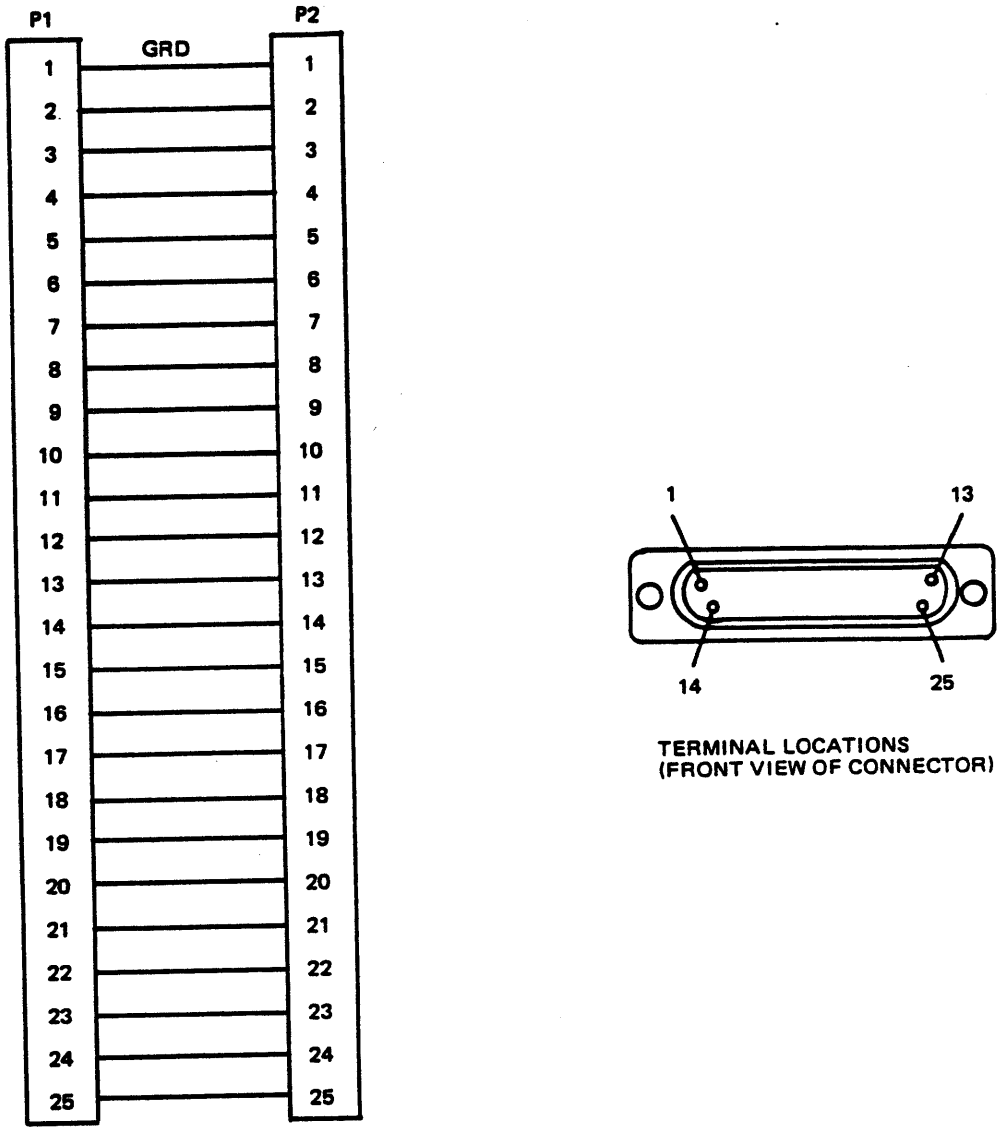
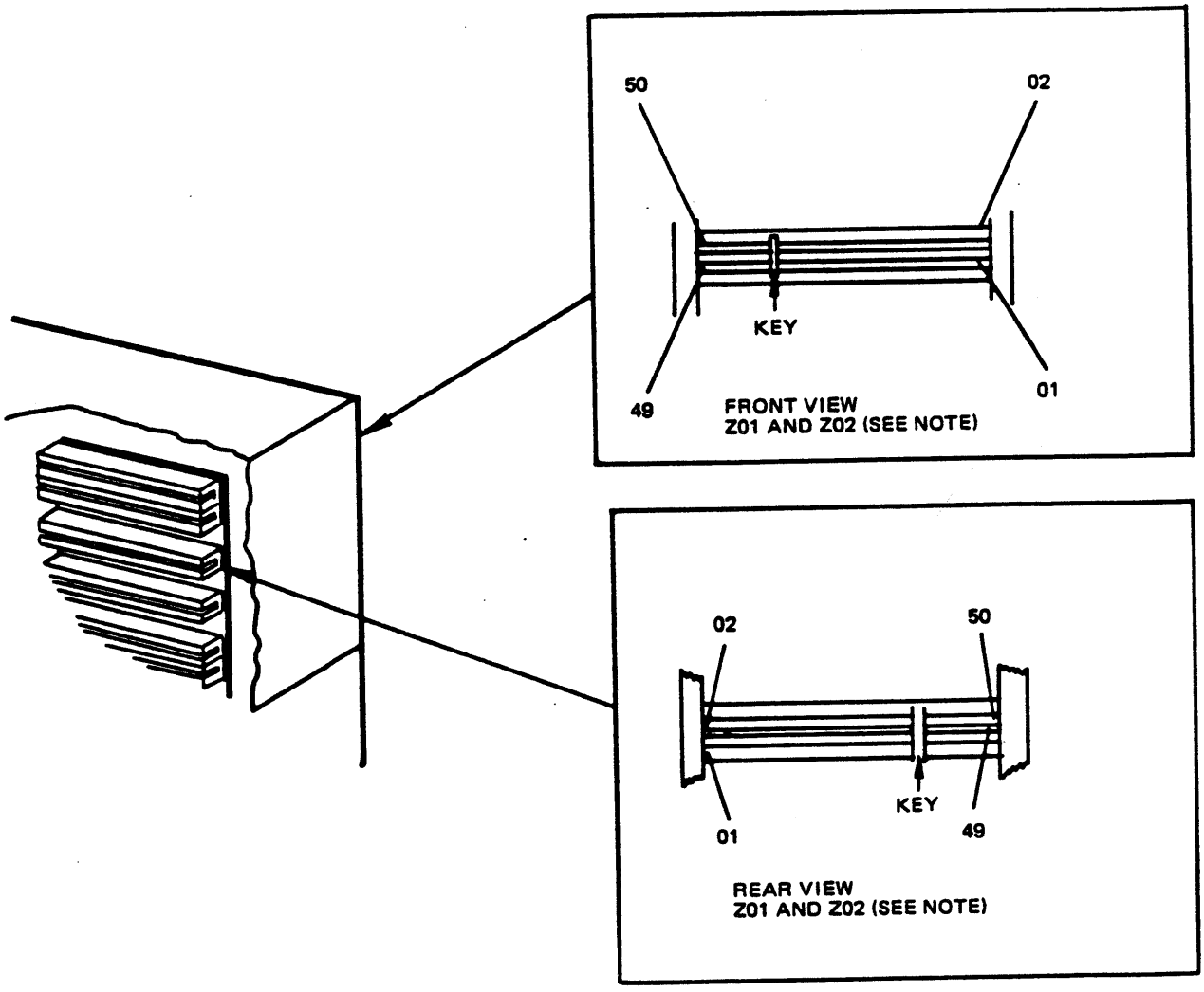


Figure 3-80 Wiring of External Cable (04910129)

3.5.12 System I/O Bus

Figure 3-81 shows the terminal locations of a typical bus connector. Table 3-26 lists the bus signals and the connector terminals on which the signals appear. The bus signals are shared by both the I/O bus and system bus. The signals are also defined in this subsection.



NOTE

AS VIEWED FROM THE FRONT OF THE CABINET, Z01 IS ON THE RIGHT AND Z02 IS ON THE LEFT.
AS VIEWED FROM THE REAR OF THE CABINET, Z01 IS ON THE LEFT AND Z02 IS ON THE RIGHT.

Figure 3-81 Typical Bus Connector Terminal Locations

Table 3-26 System Bus Interface Lines (Sheet 1 of 2)

CLASS	FUNCTION		MNEMONIC	LOCATION CONN.	LOCATION PIN
Timing	Bus Request		BSREQT-	Z01	13
	Data Cycle Now		BSDCNN-	Z02	27
	ACK		BSACKR-	Z02	31
	NAK		BSNAKR-	Z01	31
	WAIT		BSWAIT-	Z01	42
Information	Data Bit	0	BSDT0A-	Z01	43
		1	BSDT00-	Z01	41
		2	BSDT01-	Z01	39
		3	BSDT02-	Z01	36
		4	BSDT03-	Z01	34
		5	BSDT04-	Z01	33
		6	BSDT05-	Z01	32
		7	BSDT06-	Z01	30
		8	BSDT07-	Z01	26
		9	BSDT0B-	Z01	24
		10	BSDT08-	Z01	23
		11	BSDT09-	Z01	22
		12	BSDT10-	Z01	21
		13	BSDT11-	Z01	19
		14	BSDT12-	Z01	18
		15	BSDT13-	Z01	17
		16	BSDT14-	Z01	16
		17	BSDT15-	Z01	15
	Address Bit	0	BSAD00-	-	-
		1	BSAD01-	Z02	32
		2	BSAD02-	Z02	30
		3	BSAD03-	Z02	26
		4	BSAD04-	Z02	25
		5	BSAD05-	Z02	24
		6	BSAD06-	Z02	23
		7	BSAD07-	Z02	21
		8	BSAD08-	Z02	18
		9	BSAD09-	Z02	17
		10	BSAD10-	Z02	16
		11	BSAD11-	Z02	15
		12	BSAD12-	Z02	14
		13	BSAD13-	Z02	13
		14	BSAD14-	Z02	12
		15	BSAD15-	Z02	10
		16	BSAD16-	Z02	09
		17	BSAD17-	Z02	08
		18	BSAD18-	Z02	07
		19	BSAD19-	Z02	06
		20	BSAD20-	Z02	05
		21	BSAD21-	Z02	04
		22	BSAD22-	Z02	03
		23	BSAD23-	Z01	48

Table 3-26 System Bus Interface Lines (Sheet 2 of 2)

CLASS	FUNCTION	MNEMONIC	LOCATION CONN.	PIN
Control Accompanying Transfer	Memory Reference	BSMREF-	Z01	44
	Bus Byte	BSBYTE-	Z01	45
	Bus Write	BSWRIT-	Z01	09
	Second Half Bus Cycle	BSSHBC-	Z01	12
	Double Pull	BSDBPL-	-	-
	Lock	BSLOCK-	Z01	10
Integrity Accompanying Transfer	Red	BSREDD-	Z01	46
	Yellow	BSYELO-	Z01	47
	Data Parity Left	BSDP00-	Z01	25
	Data Parity Right	BSDP08-	Z01	14
	Address Parity	BSAP00-	Z02	19
Static Integrity	Logic Test Out	BSQLTO-	Z01	28
	Logic Test In	BSQLTI-	Z01	27
	Logic Test Active	BSQLTA-	Z02	34
Miscellaneous Control	Master Clear	BSMCLR-	Z01	07
	Power On	BSPWON+	Z02	35
	Resume Interrupting	BSRINT-	Z01	06
Tie-Breaking Network	-	BSAUOK+	Z02	39
	-	BSBUOK+	Z02	42
	-	BSCUOK+	Z02	41
	-	BSDUOK+	Z02	44
	-	BSEUOK+	Z02	43
	-	BSFUOK+	Z02	46
	-	BSGUOK+	Z02	45
	-	BSHUOK+	Z02	48
	-	BSIUOK+	Z02	47
	-	BSMYOK+	Z02	36

Timing Signals

The following five signals accomplish the handshaking function on the bus:

1. Bus Request (BSREQT-): When True, this signal indicates that one or more units on the bus requested a bus cycle. When false, there are no pending bus requests.

2. Data Cycle Now (BSDCNN-): When True, this signal indicates that a specific source (master unit) is making a bus transfer and placed information on the bus for use by some specific destination (slave unit). When False, the bus is idle or between bus cycles.

3. ACK (BSACKR-): When True, this signal indicates to the master unit that the slave unit is accepting this transfer.

4. NAK (BSNAKR-): When True, this signal indicates to the master unit that the slave unit is refusing this transfer.

5. WAIT (BSWAIT-): When True, this signal indicates to the master unit that the slave unit is busy and cannot accept the transfer at this time.

Information Signals

The following 42 signals are transferred as the information content of each bus cycle. These 42 signals are each valid for use by the destination (slave) on the leading edge of the strobe signal (delayed 60 nanoseconds from BSDCNN-).

1. Data Lines (BSDT0A- through BSDT15-): These 18 lines constitute an 18-bit word of information transfer. This information can be in the form of true main memory data, address information (source identification), control information, register information, or status information.

2. Address Lines (BSAD00- through BSAD23-): These 24 address lines have either of two interpretations, depending on control line Memory Reference (BSMREF-).

Control Accompanying Transfer

The following signals for each bus cycle control the information signals:

1. Memory Reference (BSMREF-): When True, this signal indicates that the address leads contain a memory address. When False, this signal indicates that the address leads contain a channel address and a function code.

2. Bus Byte (BSBYTE-): When True, this signal indicates that the current transfer is a byte transfer rather than a word transfer.

3. Bus Write (BSWRIT-): When True, this signal indicates that a master unit is requesting a slave unit to execute a write cycle.

4. Second Half Bus Cycle (BSSHBC-): This signal is used by the master unit to indicate to the slave unit that this is the information previously requested. From the time a pair of units on the bus started a read operation until the second cycle occurs to complete the transfer, both units are busy to all other units on the bus.

5. Bus Lock (BSLOCK-): This signal is used by the master unit to reference memory in the read modify write or double word mode and locks out any other unit that is trying to break into the operation. If a test and set memory (BSLOCK- low, BSSHBC- high) is being performed and the lock is already set, the memory sends a NAK to master unit. If the lock is not set, it is set and the memory sends an ACK to the master unit. If a reset memory (BSLOCK- low, BSSHBS- low) is performed, memory responds to the master unit with an ACK.

6. Bus Double Pull (BSDPBL-): When True, this signal indicates that the master is requesting a double word operand from the slave. During the first second half bus cycle, BSDBPL- is redelivered to the requesting unit, indicating that another word follows.

NOTE

If a single word fetch memory is installed on the system, BSDBPL- is not redelivered during the second half bus cycle, notifying the requesting unit that only single word operations can be performed.

Integrity Accompanying Transfer

The following signals accompany transferred information for verification and to indicate any corrections performed:

1. Red (BSREDD-): When True, this signal indicates that the accompanying transferred information is in error. On memory read responses, it indicates an uncorrectable error in the data. In a controller, the result is to set a status bit.

2. Yellow (BSYELO-): When True, this signal indicates that the accompanying transferred information is correct, but a correction operation was performed. It designates that a single bit error and maintenance action should be performed if occurrence is frequent and in multiple locations. On a memory read response, it indicates that an error was found and successfully corrected. In a controller, the result is to set a status bit.

3. Data Parity Left Byte (BSDP00-): This signal contains odd parity for bits 0 through 8 of the data bus.

4. Data Parity Right Byte (BSDP08-): This signal contains odd parity for bits 9 through 17 of the data bus.

5. Address Parity (BSAP00-): This signal contains odd parity for bits 0 through 7 of the address bus.

Static Integrity

The following signals verify the continuity of the bus and provide a path to indicate successful completion of resident logic tests:

1. Logic Test Out (BSQLTO-): This signal travels the entire length of the bus, passing through each and every connector, cable, and terminator in the system, and if continuous, indicates that the bus has no vacant slots nor missing connectors. This signal also indicates that each unit successfully completed its resident logic test.

2. Logic Test In (BSQLTI-): This signal performs the same function as the Logic Test Out (BSQLTO-) signal.

3. Quality Logic Test Action (BSQLTA-): When True, this signal indicates that at least one unit on the bus did not successfully complete its logic test or that there is a break in continuity on the bus (i.e., a unit is not installed). MSQLTA+ is also True, momentarily, for the Master Clear signal.

Miscellaneous Control

The following signals perform control functions on the bus, but are completely asynchronous to the bus cycle:

1. Master Clear (BSMCLR-): This signal is normally False and becomes True when the Master Clear (CLR) push button on the CPU control panel is pressed. When signal BSMCLR- is True, the units on the bus initialize. In addition, units capable of doing so, run a logic test. Successful completion of the logic test is indicated by passing on the input signal BSQLTI- to the next unit as BSQLTO-. To be recognized by units on the bus, Bus Clear must be True for at least 500 nanoseconds and have clean edges.

2. Power On (BSPWON+): This signal is True when all power supplies in the system are operating correctly.

3. Resume Interrupting (BSRINT-): This signal is a 200-nanosecond pulse, which is issued by the CPU whenever it completes a level change. When this signal is received, each destination that was previously interrupted and refused (NAK from CPU) reissues the interrupt.

Tie-Breaking Network

The tie-breaking network signals are:

1. Tie-Breaking Networks (BSAUOK+ through BSIUOK+): All potential master units look at these lines to determine if units of higher priority requested the system bus. If these signals are all high, the requesting master unit receives the system bus and can send BSDCNN-.

2. Tie-Breaking Network (BSMYOK+): This signal indicates that a master unit's request flip-flop was not set, 20 nanoseconds elapsed, and units of a higher priority on the system bus did not want the cycle.

For additional information on the system I/O and system bus, refer to the system CPU manual (subsection 1.2 contains the manual order numbers).

3.6 SYSTEM EXPANSION

System modification can involve the addition of optional controllers and related equipment, and the expansion of memory. All controller boards, adapters, and Memory-Pacs for a fully expanded system are contained within the basic cabinet.

This subsection provides the required instructions for the addition of communications or memory extension chassis, controller boards, and related equipment.

WARNING

To avoid bodily injury, before starting the following procedures ensure that the Power ON/OFF switch, located on the control panel housing, is placed in the OFF position, the PDU circuit breaker is placed in the OFF position, and that all ac power cords to the system are disconnected from their source of power.

3.6.1 Extension Chassis Installation

Chassis expansion can include the addition of up to two communications extension chassis on the I/O bus, and one memory extension chassis on the system bus. The extension chassis can be either a 5- or 10-card chassis, depending on the system configuration. Refer to the configuraton rules for chassis to rack relationships (subsection 3.5.1) before starting the following procedure.

To install a 5- or 10-card extension chassis in the basic cabinet, proceed as follows:

WARNING

To avoid bodily injury, before starting the following procedure ensure that the Power ON/OFF switch, located on the control panel housing, is placed in the OFF position, the PDU circuit breaker is placed in the OFF position, and that all ac power cords to the system are disconnected from their source of power.

1. Set the Power ON/OFF switch on the system control panel housing to the OFF position (ensure that the DC ON indicator is extinguished on the system control panel).

2. Set the PDU circuit breaker (on the PDU front panel) to the OFF position.

3. Disconnect all ac power cords to the system from their source of power.

4. Open the front upper and lower doors, and rear door of the basic cabinet.

5. If applicable, remove the basic cabinet right-side panel; otherwise, with the expansion (bulkhead) cabinet already attached to the basic cabinet, open the front and rear doors of the expansion (bulkhead) cabinet.

6. Remove the filler panel from the designated area of the basic cabinet, where the new extension chassis is to be installed.

7. Temporarily remove any bulkheads interfering with the installation of the extension chassis, saving the hardware for reinstallation later.

8. Open the carton containing the extension chassis and installation kit. Check that the contents of the kit match the itemized parts list and that none of the items are missing or damaged.

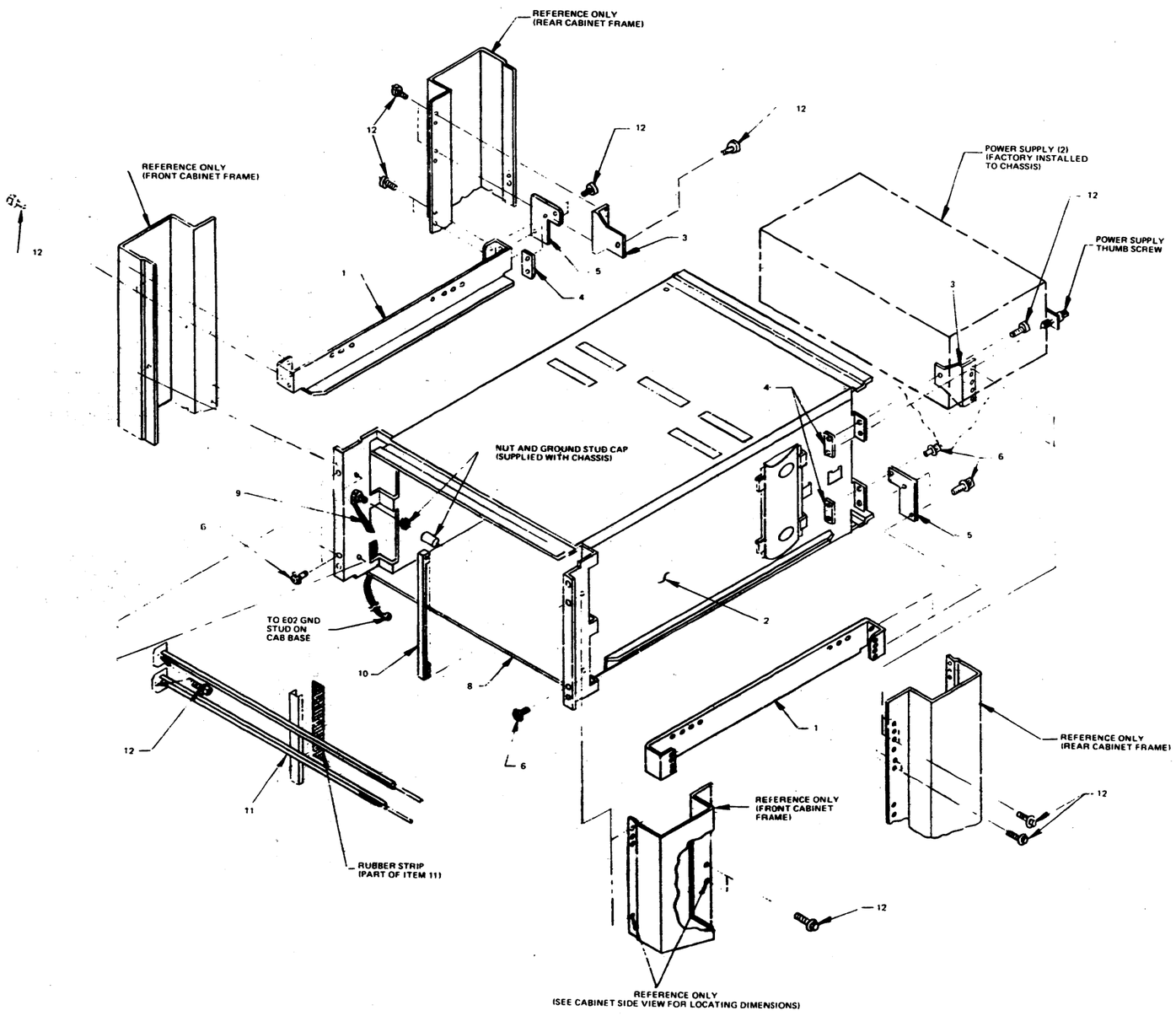
9. Refer to the illustration and parts list in Figure 3-82 and install the extension chassis in the cabinet as follows:

NOTE

Proper placement of the card chassis in the cabinet requires that the slide tray supports be installed to the cabinet frame at the appropriate locations as shown in Figure 3-82. A clearance of approximately 1/8-inch (0.32 cm) between the chassis after installation is normal, and is dependent upon the location of the slide tray supports.

a. Align the slide tray support (item 1) to the cabinet side frame mounting holes, so that the bottom holes of the slide tray supports are exactly aligned as shown in the cabinet side view of Figure 3-82. Install four TORX screws (item 12) through the top and bottom holes of the slide tray support and fasten securely to the cabinet side frames.

b. Repeat step a. for the opposite slide tray support (item 1).



PARTS LIST

ITEM NO.	IDENTIFICATION NO.	DRAWING TITLE	QUANTITY
1	60141447-001	SLIDE TRAY SUPPORT	2
2	60143928-003	EXTENSION CHASSIS (10-CARD)	X
3	60141670-001	UPPER TRAY SUPPORT	2
4	60141567-001	NUT PLATE	4
5	60141671-001	SUPPORT PLATE	2
6	03010228-001	TORX-HD SCREW 5/16	4
7	60128386-001	BUS EXTENDER CABLE	X
8	60128379-001	CABLE KEEPER	X
9	60131128-010	GROUND CABLE	-
10	60133618-001	DAMPENING STRIP	1
11	60150030-001	RETAINING BAR	1
12	03010231-003	TORX-HD SCREW 8-32	20

Figure 3-82 Ten-Card Chassis Installation (Sheet 1 of 2)

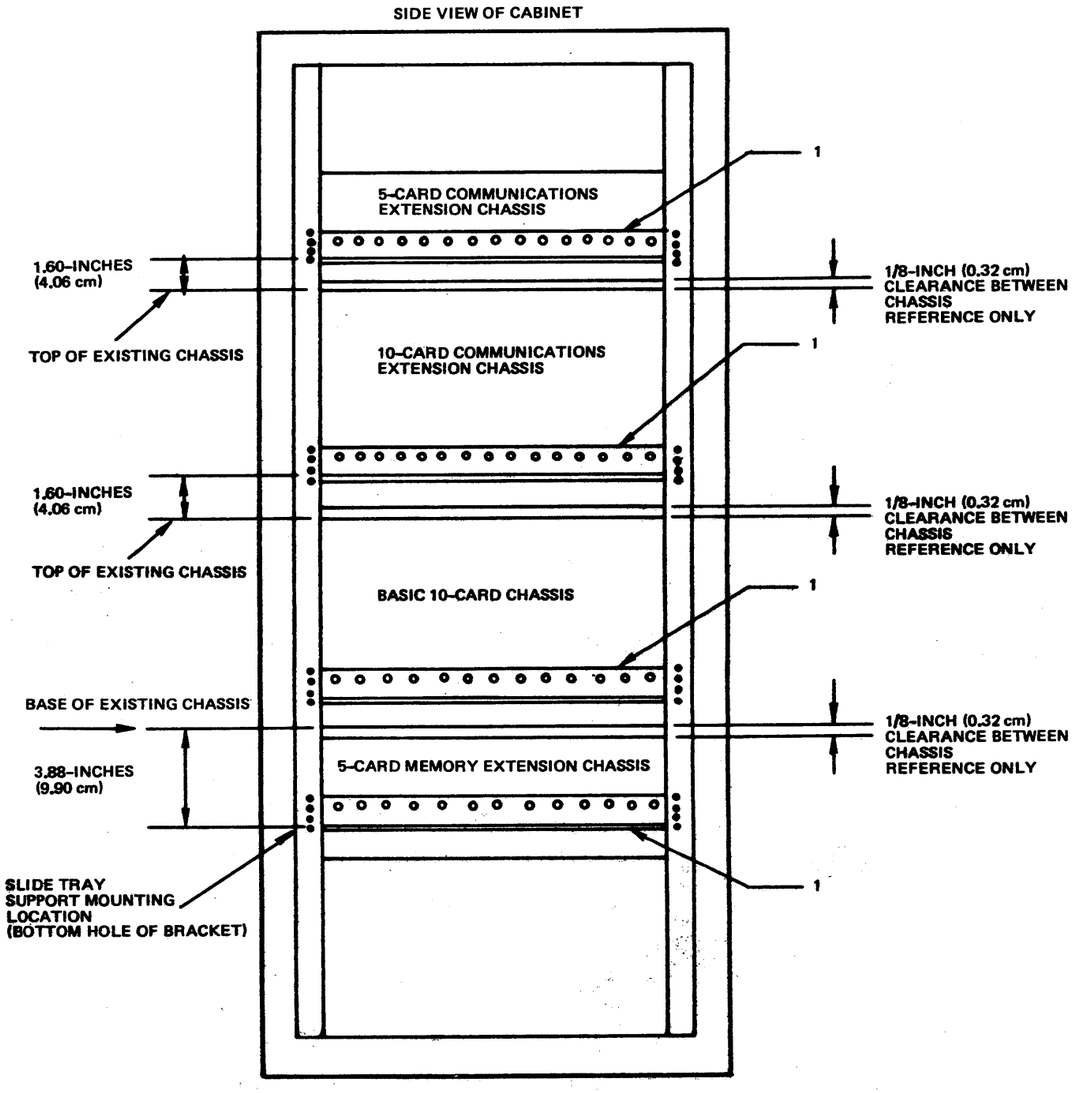


Figure 3-82 Ten-Card Chassis Installation (Sheet 2 of 2)

WARNING

The extension chassis is shipped with the power supplies installed at the rear of the device. Two persons are required when lifting the chassis.

c. With another person assisting, place the extension chassis (item 2) onto the left and right slide tray supports (item 1) and slide it in from the front of the cabinet to the rear. Check the space between the new and existing chassis. It should be approximately 1/8-inch (0.32 cm), as shown in Figure 3-82.

d. Attach two upper tray supports (item 3) to the nut plates (item 4) at the rear of the chassis (next to the top power supply thumb screws), using two screws (item 12).

e. Fasten each upper tray support (item 3) to the cabinet frame with two screws (item 12).

f. Attach two support plates (item 5) to the nut plates (item 4) at the rear of the chassis (next to the bottom power supply thumb screws), using two screws (item 12).

g. Fasten each support plate (item 5) to the slide tray supports (item 1) using two screws (item 12).

h. Fasten the front of the extension chassis to the frame with four screws (item 6).

i. Connect the ground cable (item 9) from the extension chassis ground stud (E05), to the ground stud (E02) at the base of the cabinet.

j. Dress and secure the ac power cords from the extension chassis power supplies to the cable clamps provided on the cabinet sides, and connect the male plugs to the PDU receptacles located at the base of the cabinet (Refer to subsection 3.3.5 for proper load distribution for the PDU).

k. Install the bus extender ribbon cables between the extension chassis and existing chassis (refer to subsection 3.6.2).

3.6.2 Chassis to Chassis Bus Connection

After installing the extension chassis in the system cabinet, the bus segments (Both I/O and System bus) must be connected in order for the bus segments to have continuity. To perform this operation, refer to Figure 3-82 and proceed as follows:

NOTE

The segments of the bus within each chassis must be connected in order for the bus to have continuity between chassis.

1. Using a 6mm ALLEN-head key (see Figure 3-6.2), unlock and swing open the system control panel.

2. Remove the two TORX-head screws securing the retaining bar to the left side of the basic 10-card chassis and remove the retaining bar. Remove the dampening strip securing the boards to the chassis and set the items aside for reinstallation later.

3. If the system bus is to be extended, remove the memory board at the bottom of the basic chassis. If the I/O bus is to be extended, remove the terminator or controller board at the top of the basic chassis.

4. Plug one end of a bus extender ribbon cable (item 7) into the bottom connector of the upper chassis (see Figure 3-82).

5. Slide the free end of the cable through the cutout in the bottom of the upper chassis, through the cutouts in the lower chassis, and plug the cable into the top connector of the lower chassis.

6. Repeat the previous two steps for the bus segments on the other side of the chassis and then attach a cable keeper (item 8) onto each cable.

7. Proceed in a similar manner for each newly installed extension chassis.

8. After installing the bus extender cables, install or reconfigure the controllers or memory boards as described in subsection 3.6.3.

3.6.3 Reconfiguration

When expanding a system, it may be necessary to install additional boards into the basic or extension chassis, and in some cases, to relocate the boards in order to establish the correct priority allocation. In all cases, refer to rules for controller to chassis relationships (subsection 3.5.2), prior to performing the following procedure.

To install or relocate the boards in the basic or extension chassis, proceed as follows:

1. Refer to the new Computer Configuration Sheets (CCS), shipped with the installation kit, and determine the board allocation for the new system configuration.

NOTES

1. If any controller boards have to be moved from the basic 10-card chassis to the new extension chassis, the device cables must be disconnected from all adapter boards. Make sure that the cable labels are clearly marked for easy reconnection.

2. Device cables are routed along the sides of the basic 10-card chassis or along the sides of the new extension chassis, depending on the adapters into which they plug. Ensure that they are fed on the correct side. This is important because the cables are designed to plug into adapters on one side only.

3. Whenever additional boards are added to the system, it may be necessary to readjust the system power supplies (+5Vdc). Subsection 3.3.6 provides instructions for power supply adjustments.

4. If the system expansion requires the addition of adapters/memory-pacs, ensure that the adapter stacking connectors are installed correctly (refer to subsection 3.6.4).

2. Identify and label any cables that are to be moved. Route the cables to the new location in the extension chassis.

NOTE

Ensure that the hexadecimal rotary switches and jumpers on the memory and controller boards are set correctly (refer to subsection 3.5 for switch and jumper locations for the system boards).

3. With reference to the new CCS, insert the boards into the correct slots of the appropriate chassis.

4. Connect the device cables to the correct adapter boards. The cables should be labeled for easy installation.

5. Replace any bulkheads that were temporarily removed.

6. Connect the other end of the new device cables to the system bulkhead locations according to the new CCS.

7. Install the dampening strip (item 10) to the extension chassis by firmly pressing it over the front of the chassis boards.

8. Install and secure the retaining bar (item 11) to the new extension chassis, using two TORX-head screws (item 12).

9. Replace the dampening strip and retaining bar that were removed from the basic 10-card chassis, and then close and secure the system control panel.

10. Replace any cabinet side panels that were temporarily removed.

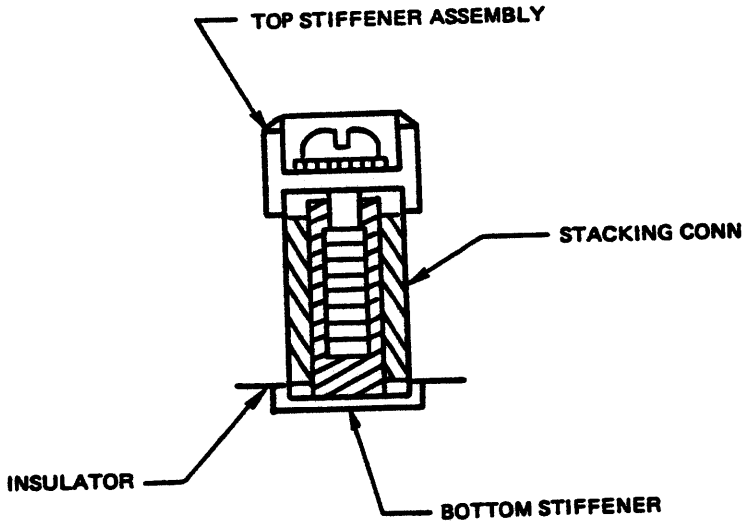
11. Reconnect all ac power cords to their power source.

12. Close the cabinet front and rear doors.

13. Power up the system and verify satisfactory system operation by performing the system checkout as described in subsection 3.4

3.6.4 Adapter Stacking Connector

Figure 3-83 illustrates the adapter stacking connector and the part numbers associated with the connector.



DESCRIPTION	PART NUMBER
STACKING CONNECTOR	04830325-001
TOP STIFFNER ASSEMBLY	60133844-001
BOTTOM STIFFNER	60128104-001
INSULATOR	60128110-001

Figure 3-83 Adapter Stacking Connector

IV
FAULT ANALYSIS

This section of the manual provides fault analysis information to help diagnose system malfunctions. Subsection 4.1 contains a step-by-step test procedure that checks all the system assemblies and isolates faulty units. Subsection 4.2 contains general reference information on the system operation and assemblies. Included are interrupt vectors, fault handling data, control words, indirect control words, word formats, and instruction sets.

4.1 SYSTEM FAULT ANALYSIS

The procedures contained in this subsection test the system in a logical sequence that follows the Fault Analysis Flow Chart (see Figure 4-1). This subsection contains the following:

- Fault Analysis Flow Chart
- Initial Fault Analysis
- Quality Logic Tests (QLTs)
- Extended Quality Logic Tests (E-QLTs)
- Test and Diagnostic Procedures (T&Ds).

4.1.1 Fault Analysis Flow Chart

The Fault Analysis Flow Chart provides a step-by-step procedure for determining faults within the system and is a guide to this section.

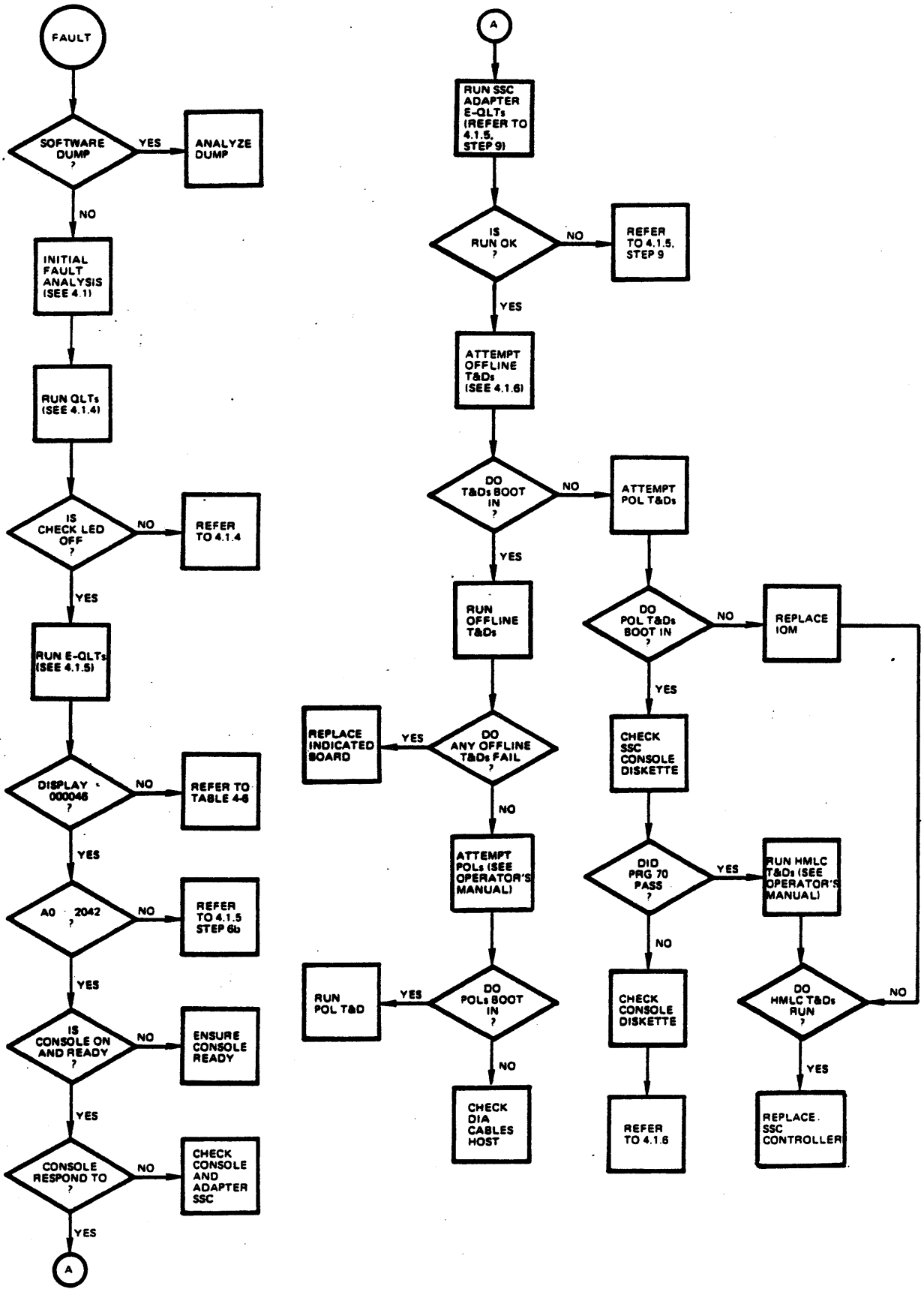


Figure 4-1 Fault Analysis Flow Chart

4.1.2 Initial Fault Analysis

When a failure occurs and a software dump cannot be obtained, the first step is to determine the possible cause and the state of the system by using the operator control panel. Figure 4-2 shows the control panel and Table 4-1 summarizes the operator control panel operations.

NOTE

If at any time the LED indicator marked INT remains ON after pressing the EXECUTE push button, the CPU is either hung up or in a non-interruptable fault state. Press the CLEAR push button. Display and record A0 and the type of instuction at and before that location.

If a software dump can be obtained and the software is rebooted without problems, then the dump should be analyzed to determine the associated hardware that may have caused the problem or to determine if it is a software problem.

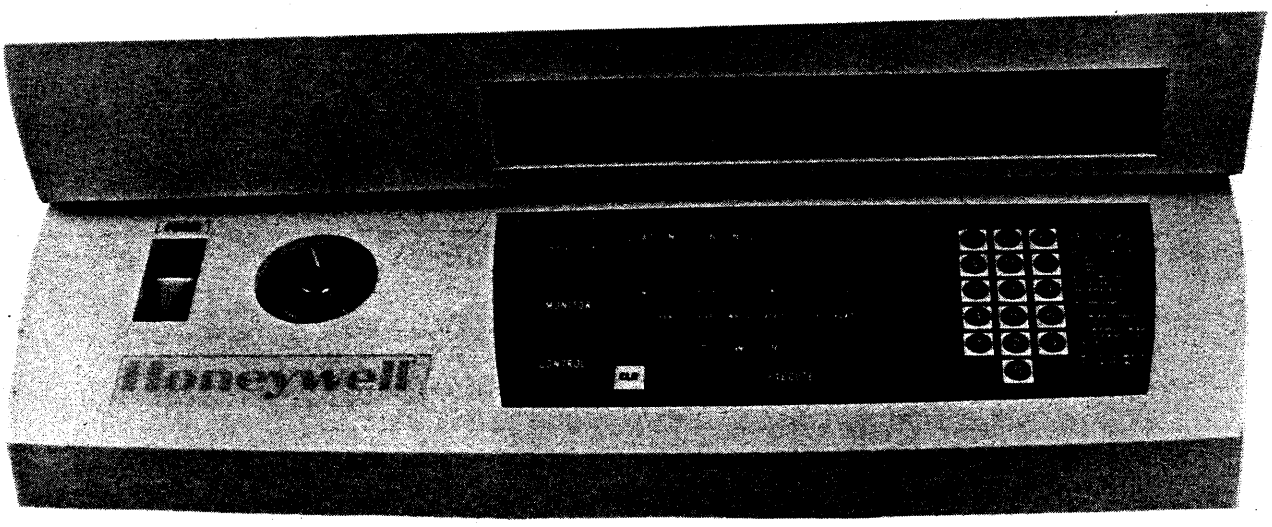


Figure 4-2 Operator Control Panel

Table 4-1 Summary of Operator Control Panel Operations

MODE	REGISTER (HEX)	(OCTAL)	OPERATION
Stop	B	0	Bootstrap with Timer ON
		1	Bootstrap with Timer OFF
	B Not	-	If Stop, Step Mode
		-	If Stop Not, Stop Mode
Run	-		Run Mode
Read	A	0	Read Instruction Counter
		1	Read Index Register 1
		2	Read Index Register 2
		3	Read Index Register 3
		4	Read Accumulator
		5	Read Quotient Register
		6	Read Indicator/Select Register
		7	Display Memory Fault Address
	C	0	Read AOR Unpaged
		1	Read Main Memory
		2	Read MM Unpaged AOR + 1
		3	Read MM Unpaged AOR - 1
		4	Read AOR Paged
		5	Read MM Paged
		6	Read MM Paged AOR + 1
		7	Read MM Paged AOR - 1
Write	A	0	Write Instruction Counter
		1	Write Index Register 1
		2	Write Index Register 2
		3	Write Index Register 3
		4	Write Accumulator
		5	Write Quotient Register
		6	Write Indicator/Select Register
	C	0	Write AOR Unpaged
		1	Write MM Unpaged
		2	Write MM Unpaged AOR + 1
		3	Write MM Unpaged AOR - 1
		4	Write AOR Paged
		5	Write MM Paged
		6	Write MM Paged AOR + 1
		7	Write MM Paged AOR - 1
	D	0	Turn Timer ON
		1	Turn Timer OFF
		2	Run Extended QLTs
		3	Turn Cache OFF
Trap	-		Trap Mode

Using the operator control panel, perform initial fault analysis as follows:

1. Check the DC ON indicator on the control panel. If the indicator is not ON, refer to subsection 4.1.3 entitled Power Fault Analysis.

2. Check that the control panel is operational.

3. Check that the elapsed timer is running:

   a. Unless the timer was turned OFF either by the operator control panel (select D1, WRITE, EXECUTE) or the Extended QLTs were run, the elapsed timer (memory location 451) should be incrementing by one every millisecond.

   b. If the timer is not running and was not turned OFF (assuming the panel is operational), the IOM is either hung or a breakdown in communications between the IOM and CPU occurred since the last Master Clear.

   C. To determine if the IOM is hung, attempt to turn the timer ON twice from the control panel (select D0, WRITE, EXECUTE, EXECUTE). If the INT indicator does not remain ON after the second EXECUTE, the IOM is not hung.

4. Display and record the contents of the following registers:

   - Instruction Counter (A0)
   - Index Register 1 (A1)
   - Index Register 2 (A2)
   - Index Register 3 (A3)
   - A-Register (A4)
   - Q-Register (A5)
   - Indicator Register (A6).

5. Display the level zero interrupt location (000400) from the operator control panel and take the appropriate action:

   a. If the location equals 000000, go to step 6.

   b. If the location is not equal to 000000, display and record the channel fault status words in locations 000420 through 000437.

6. Perform a memory dump and have the results analyzed by the appropriate personnel. If memory parity errors are indicated in the memory dump, run the Memory Scan Test as follows:

a. Select A7.
b. Press R (READ).
c. Press E (EXECUTE).

At the end of the test, the location in memory where the fault occurred is displayed on the control panel. The cause of the fault is written into memory location 0, using the format of the channel fault word (see Table 4-9). This test involves memory only, not the pager or cache.

NOTE

The Memory Scan Test is also used to confirm the number of memory controller boards in the system. The IOM reads each sequential memory location until a fault, normally a No Bus Response, is detected. A No Bus Response indicates the first nonexistent memory location (i.e., the end of memory). This location is displayed on the control panel. If memory is 256K words, the contol panel will read 000000. This test involves memory only, not the pager or cache.

7. Run the Quality Logic Tests (QLTs) detailed in subsection 4.1.4.

4.1.3 Power Fault Analysis

If the DC ON indicator on the operator control panel is not ON, proceed as follows:

1. Open the rear door on the cabinet and check that the AUX V ON LED located at the rear of each power supply is ON. If the LED on each power supply is ON, proceed to step 2. If the LED on one or more power supplies is OFF, proceed to step 3.

2. Check the setting of the 5-volt adjustment control on each power supply in accordance with subsection 3.3.6.3. Disconnect one power supply at a time from the ac supply by disconnecting the ac cord from the back of the power supply (see Figure 4-3), and disconnecting the white plastic plug on the power supply, located behind the ac cord assembly. Proceed to step 4.

3. Check that 115 Vac is available at the outlet on the Power Distribution Unit (PDU). If 115 Vac is available at the outlet, replace the power supply. If 115 Vac is not available at the outlet, the PDU is faulty. Refer to the Power System Manual (Order Number FM90).

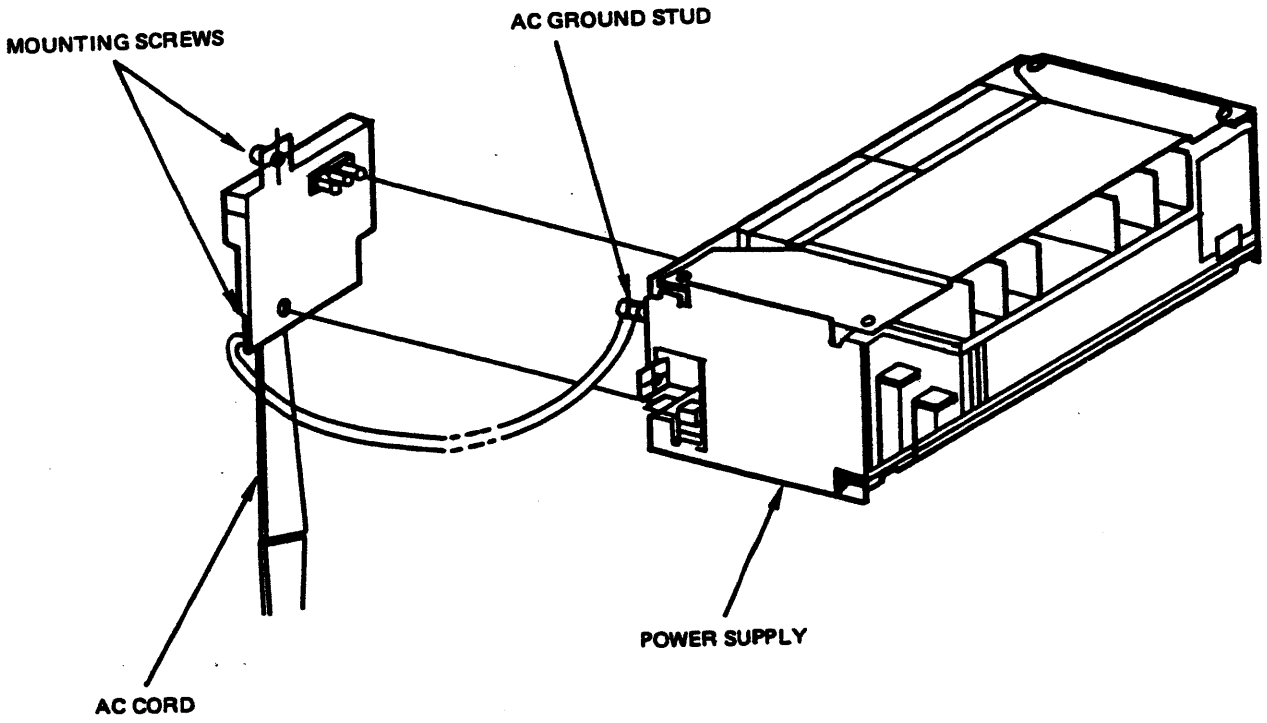


Figure 4-3 Power Supply AC Cord Connection

4. The Power Valid signal (BSPWON+) is on the bus at connector 202, terminal 35. Figure 4-4 shows the flow of the Power Valid signal from the power supplies to the LED indicator on the operator control panel. The boards, connectors, and terminals are labeled on Figure 4-4.

5. After replacing the faulty device, reconnect the ac cord to the power supplies.

4.1.4 Quality Logic Tests

General Description

After the initial fault analysis (subsection 4.1.2), the QLTs must be run. The QLTs are firmware-resident test programs that reside on all the boards in the system, except memory and the DIA. QLTs are initiated on each board by the receipt of a Master Clear signal (BSMCLR-) from the bus. The Master Clear signal can be initiated from the operator control panel via the CLR (Clear) push button, from the host system via the DIA, or from the Power Valid signal (BSPWON+) sent by the system power supplies to the operator control panel (see Figure 4-4). Figure 4-5 is a flow chart that shows the master clear initiation flow.

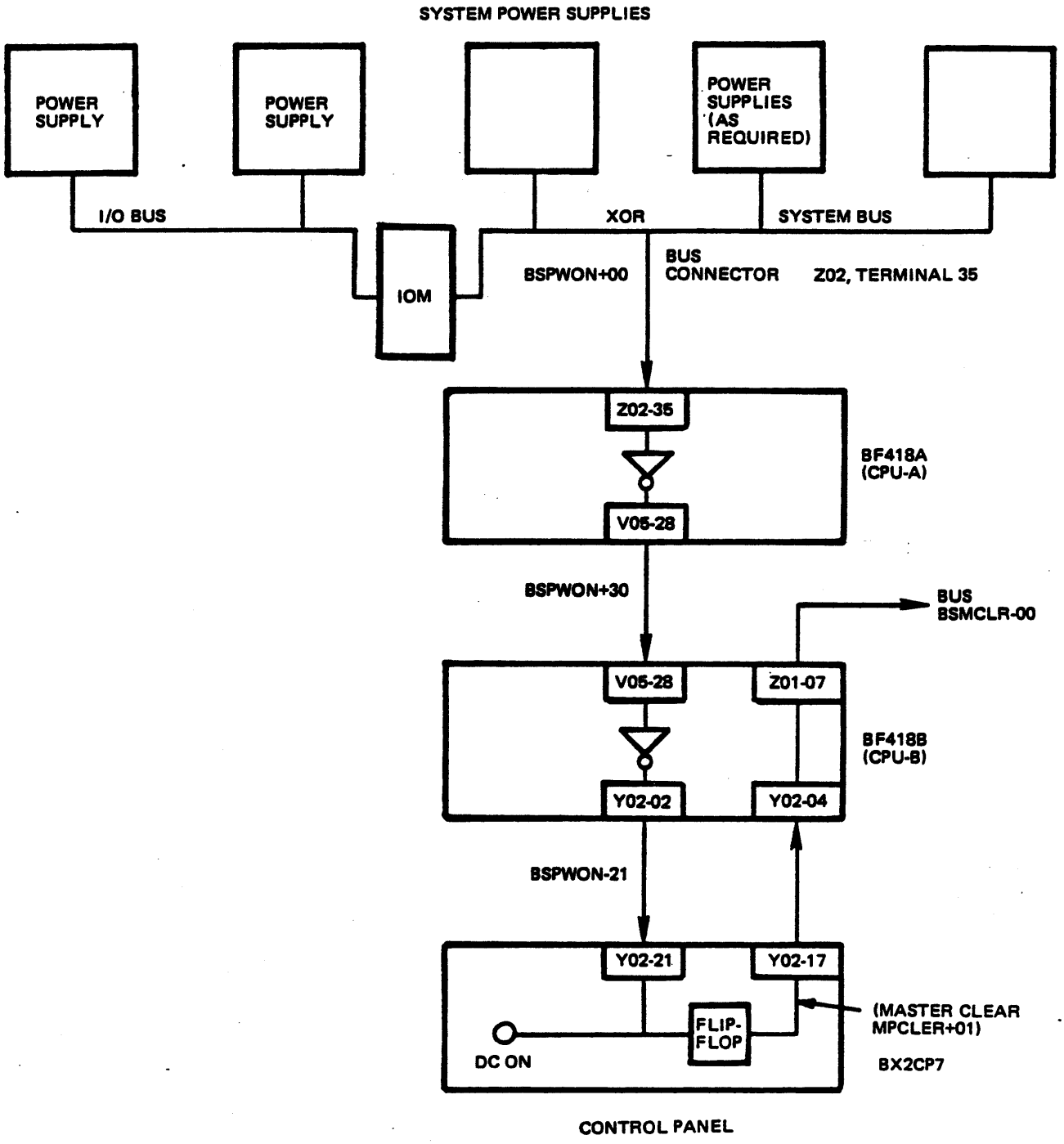


Figure 4-4 Power Valid Signal Flow Chart

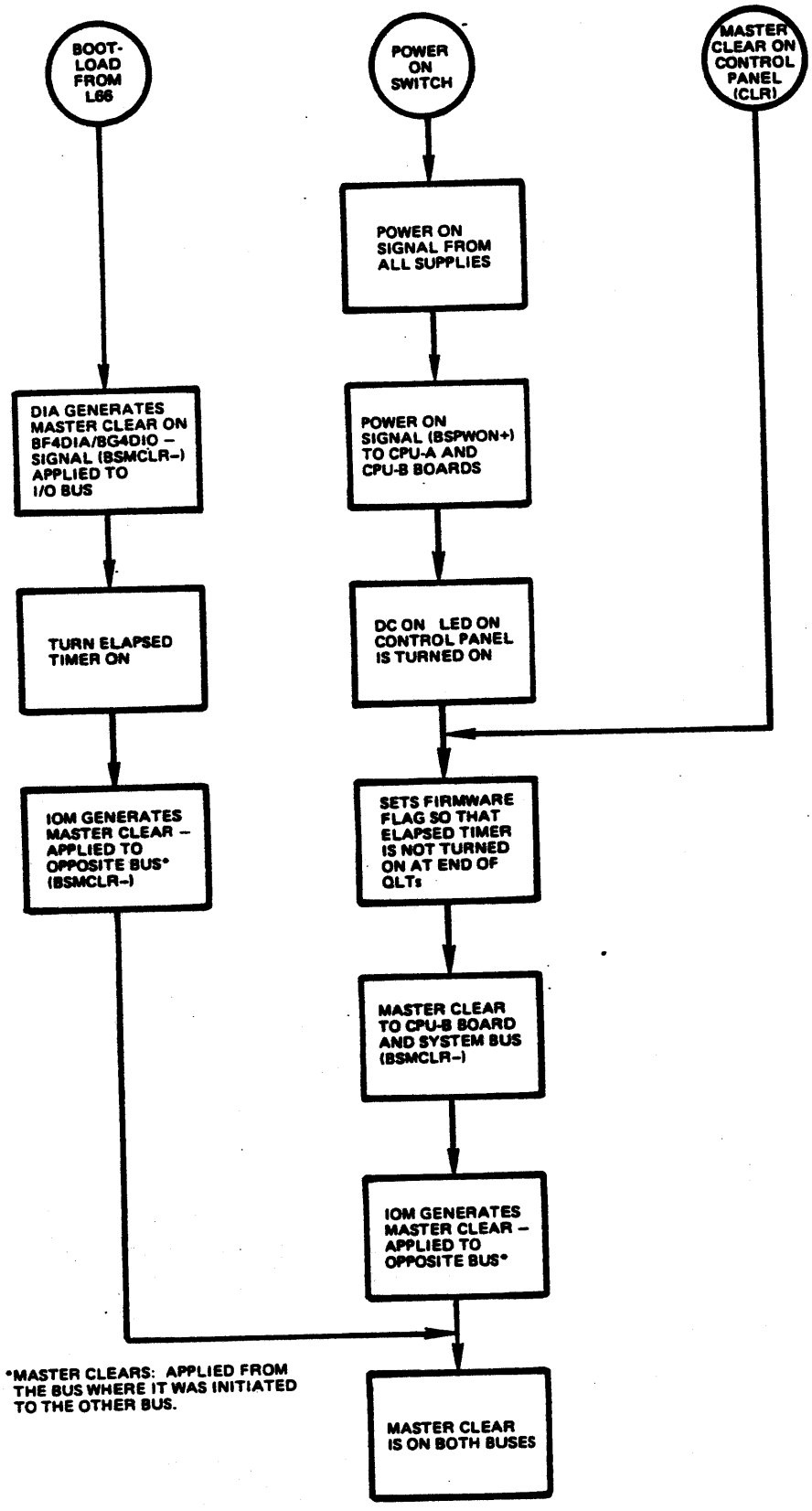


Figure 4-5 Master Clear Initiation Flow Chart

When initiated, the QLTs light one or more of the red LEDs that are positioned along the edge of most of the boards in the system, and also light the LED marked CHECK on the operator control panel. Figures 4-6 through 4-10 show the QLT and parity error LED indicator locations on the boards and Tables 4-2 through 4-5 list the QLT error light combinations. Master Clear or the QLTs do not affect software or operator visible registers other than the Interrupt Enable Register. Master Clear affects every controller board, causing each one to start its QLT cycle. When the QLT cycle is successfully completed, the QLT LED goes OFF and a QLT Done signal (BSQLTO-) is placed on the bus. If the QLT cycle is not successfully completed, the QLT LED remains ON, the QLT Done signal (BSQLTO-) is not placed on the bus, and the control panel LED marked CHECK remains ON.

NOTES

1. Memory controller boards BF2MCE and BF2MAE, and the DIA controller board BF4DIA do not have QLT LEDs. They simulate a QLT cycle by placing a QLT Done signal on the bus.

2. An open bus slot causes the control panel LED marked CHECK to remain ON. QLTs, E-QLTs, and offline T&Ds run, but communications from the host to the system are not allowed.

3. The Master Clear signal from the control panel turns the timer OFF. A Boot Load turns the timer ON.

4. An open bus slot causes the control panel CHECK LED to remain ON even if all boards successfully completed their QLTs. Offline T&Ds can be executed, but host communications cannot be executed.

Operating Procedures

The QLT operating procedures are as follows:

1. Press the CLR (Master Clear) push button. When the QLT indicators on all applicable boards are lit, the QLTs are running.

2. After approximately 10 to 20 seconds, all QLT LEDs and the LED marked CHECK go OFF.

3. The contents of the instruction counter (A0) are displayed on the control panel.

4. Verify that the LED on the operator control panel marked DC ON is ON. If it is not, check the system power supplies.

5. If it appears that an excessive number of QLT LEDs are ON, check the 5-volt power supply adjustments (refer to subsection 3.3.6.3).

6. If the CHECK LED remains ON, no QLT LEDs are ON, and there are no open bus slots, check the seating of all boards into the socket cables and the IOM/CPU side hat connections.

4.1.4.1 Input/Output Multiplexer QLTs

The QLTs indicate faulty IOM boards in accordance with Figure 4-6 and Tables 4-2 and 4-3.

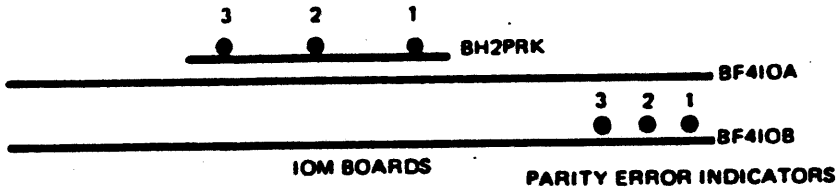


Figure 4-6 IOM Boards QLT Parity Error Indicator Locations

Table 4-2 IOM Error Light Combinations

BOARD	DEFINITIONS	ERROR LIGHTS 3	2	1
BH2PRK	QLT Successful	0	0	0
	BH2PRK Fault	1	0	0
	BF4IOA Fault	0	0	1
	BF4IOB Fault	0	1	0
	IOM Failure (cannot identify specific board or cable)	0	1	1

Table 4-3 Memory Write Parity Error Light Combinations

BOARD	DEFINITIONS	ERROR LIGHTS 3	2	1
BF4IOB	Address Parity on I/O Bus	*	*	1
	Data Parity Byte 0 on I/O Bus	*	1	*
	Data Parity Byte 1 on I/O Bus	1	*	*

*Indication is irrelevant.

The error lights shown in Table 4-3 indicate that an error was detected from the I/O bus unit during a direct memory write, but the faulty board cannot be identified.

4.1.4.2 Central Processor Unit QLTs

The QLTs indicate faulty CPU boards in accordance with Figure 4-7 and Table 4-4.

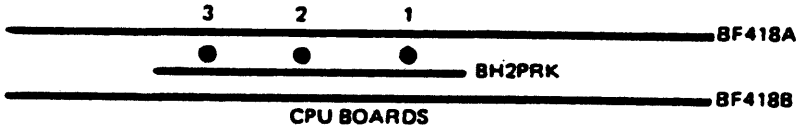


Figure 4-7 CPU Boards QLT Parity Error Indicator Locations

Table 4-4 CPU Error Light Combinations

BOARD	DEFINITIONS	ERROR LIGHTS 3	2	1
BH2PRK	QLT Successful	0	0	0
	BH2PRK Fault (ROS PROM)	1	0	0
	BF418A Fault	0	0	1
	BF418B Fault (may be memory)	0	1	0
	CPU Failure (cannot identify specific board, cable, or panel)	0	1	1

4.1.4.3 Page Control Logic Unit QLTs

The QLTs indicate a faulty PCLU board in accordance with Figure 4-8 and Table 4-5.

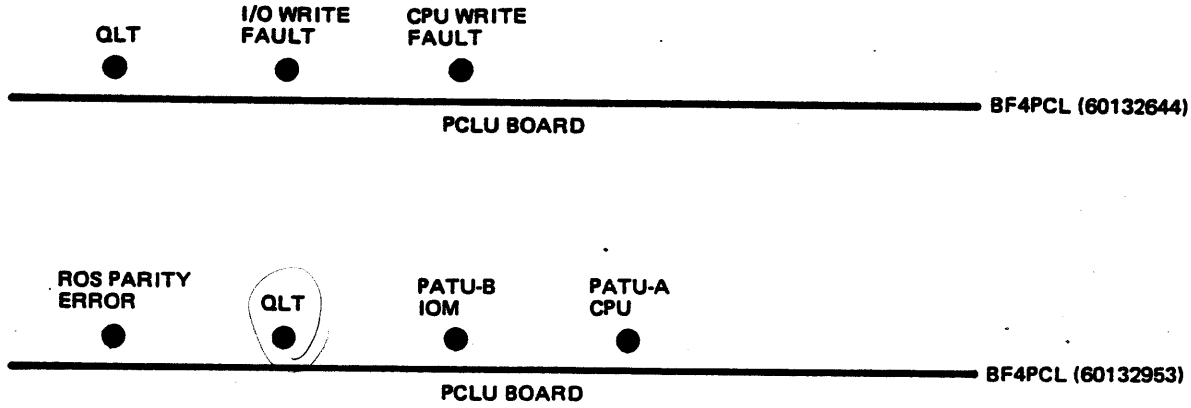


Figure 4-8 PCLU Boards QLT Error Indicator Locations

Table 4-5 PCLU Error Light Combinations

BOARD	DEFINITIONS	ERROR LIGHTS			ROS PARITY
		PATU-(BD2PAT)			
		B-IOM	A-CPU	QLT	
BF4PCL	No Errors	0	0	0	0
	CPU Fault	0	0	1	0
	IOM Fault	0	0	0	1
	BF4PCL	0	0	1	1
	QLT Failed	0	0	1	0
	PATU-B	1	0	0	0
	PATU-A	0	1	0	0
	BF4PCL Fault	1	1	1	0
	BF4PCL ROS Parity	*	*	*	1

*Indication is irrelevant.

PATU-A or PATU-B QLT failures may cause the CPU or the IOM to fail the QLTs, requiring the following to be performed:

1. If a fault is indicated for either PATU-A or PATU-B, replace the faulty PATU and rerun the QLT. If the fault persists, replace the BF4PCL board. It should be noted that the power supply can cause a cache failure. Check the voltages for ripple with an oscilloscope.

2. If the QLT indicators are ON for more than one board on the system bus, proceed as follows:

CAUTION

When removing boards from the system, the power must be OFF to avoid loss of memory contents.

   a. Remove the cache from the bus and rerun the QLTs. If the problem no longer exists, the cache is at fault. If the problem remains, reinstall the cache.

   b. If more than one memory controller board is installed, remove memory controller board number 1. Then, remove all other memory boards except one. (If additional information is necessary to identify board 1, refer to subsection 3.5.3.3.) Set the remaining memory board to 1 and rerun the QLTs. Treat the problem as in step a above.

   c. Turn the pager off as follows: on assembly number 60132644, set the hex rotary switch to 4; on assembly number 60132953, set the toggle switch to the right. Rerun the QLTs. If the problem remains, replace the pager and rerun the QLTs. Treat the problem as in step a above.

d. Replace the CPU board pair and rerun QLTs. Treat the the problem as in step a above.

4.1.4.4. System Support Channel QLTs

The QLTs indicate a faulty SSC board in accordance with Figure 4-9. When the SSC board is in Step mode and the test of a function is True, the Clear Microprocessor Instruction Register (CLEAR μPIR) LED is ON. When the QLT LED is ON, a faulty BF4SSC/ BD2SSC is indicated.

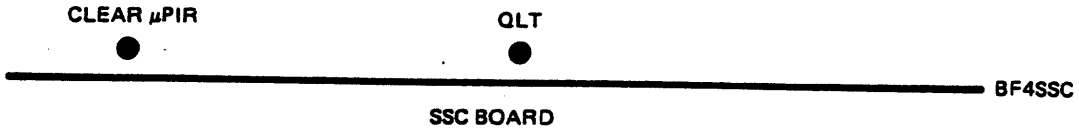


Figure 4-9 SSC Board QLT Parity Error Indicator Locations

4.1.4.5 Channel Interface Base QLTs

The QLTs indicate a faulty CIB board in accordance with Figure 4-10. When the QLT LED is ON, it indicates that a ROM scan test failed and that BF4HML is faulty.

Figure 4-10 CIB Board QLT Parity Error Indicator Location

4.1.5 Extended QLTs

General Description

The Extended QLTs (E-QLTs) are capable of detecting a high percentage of those failures that cannot be caught by the QLTs (bus or dialog-oriented logic), but which might preclude bootloading. The minimum units involved are: memory (first 16K words), CPU, IOM, and the SSC wraparound channel.

CAUTION

The E-QLTs destroy the memory and register contents.

The E-QLTs diagnose the various system components by performing the following tests in the order listed:

- Tests the CPU internal logic.
- Tests the first 16K words of memory, using the CPU
- Tests the first 16K words of memory, using the IOM
- Tests the CPU/IOM interfaces and dialog
- Tests the I/O bus
- Tests the I/O units' bus response logic
- Writes a print buffer that contains the channel number of each unit on the I/O bus in the order of priority
- Writes a software program into memory
- Executes the program in three parts:

  CPU internal

  Outputs print buffer on the system console

  Executes I/O and data wraparound tests with the CPU/IOM/SSC.

Operating Procedures

The operating procedures for the Extended QLTs are as follows:

NOTE

When running the system software, a memory dump from the host console should be performed prior to running the E-QLTs. The memory dump is an aid used to determine hardware and software faults.

1. Press the CLR (Clear) push button and wait for the CP indicator to go OFF.
2. Press the S (Select) push button.
3. Key in D2.
4. Press the W (Write) push button.
5. Press the E (Execute) push button and wait approximately 30 seconds:

   a. The panel displays the current E-QLT test number 1 to 46.

b. A message is printed on the console.

c. The CP indicator comes ON for approximately 15 more seconds and then goes OFF.

NOTE

If these three (a, b, and c) are not true, proceed to step 8.

6. When the CP indicator is OFF, display register A0:

NOTE

If register A0 is not equal to 2042, refer to b or c below.

a. If register A0 equals 2042, the E-QLTs ran successfully. The message on the console is a list of all the units on the I/O bus in their order of priority. The actual entries are derived from the units' channel number switch settings. There are two types of entries:

(1) CIB - four characters:

CONSOLE PRINTOUT	MEANING
0006	Channel 6, Subchannels 0 - 7 (HMLC 0)
0106	Channel 6, Subchannels 8 - 15 (HMLC 1)
0206	Channel 6, Subchannels 16 - 23 (HMLC 2)
0306	Channel 6, Subchannels 24 - 31 (HMLC 3)
0007	Channel 7, Subchannels 0 - 7 (HMLC 0)
	List continues in this sequence to:
0310	Channel 10, Subchannels 24 - 31

(2) Others - two characters:

CONSOLE PRINTOUT	MEANING
00	SSC (Console on No. 0, Diskette on No. 1)
01*	PIA on Channel 5
03	Unit on Channel 3
04	DIA on Channel 4

*PIAs (etc.) return only the two low-order bits of their channel number.

NOTE

The operator must check the system configuration against this printout and the locator card.

b. If register A0 equals 2056, an IOM or SSC interrupt problem is indicated. Run the Partial Online (POL) T&Ds (refer to manual order number AY34). If the POL T&Ds execute, an SSC problem is indicated (refer to subsection 4.1.4.4 of this manual). If the POL T&Ds do not execute, an IOM problem is indicated.

c. If register A0 equals 1772, a CPU, an IOM, or an SSC problem is indicated (refer to subsection 4.1.5.3 of this manual).

7. If the panel display is 000046 but there is no printout, check the console for:

a. POWER ON
b. PAPER
c. READY.

If the console was not ready, make the necessary corrections and rerun the test. If the console was ready, verify that the console is properly installed (refer to subsection 3.5.9.4 of this manual). Console operation may be rapidly checked by typing a ? (question mark). The console should print out the contents of the SSC scratchpad memory (see Figure 4-11 and the SSC E-QLTs).

NOTE

If the console is not ready, the E-QLTs run to completion as long as there are no other faults (A0 through 2042).

- Register A0 equal to 1772 without a printout indicates a CPU problem.

- Register A0 equal to 1772 with a printout is usually an SSC problem; if not, then it is an IOM or CPU problem.

8. If the panel display is not 000046 (i.e., XX00YY), the E-QLTs detected a problem (XX = Fault Message, YY = Test Number). Refer to Table 4-6.

```
ACU 000  BDR 000  000  000  000  000
AD0 13F  11C 180  121
AD1 1F0  110 120  120
AD2 1F0  110 100  100
AD3 1FF  1FF 1FF  1FF

00  000  011  033  000  000  080  000  000    066  002  040  062  002  040  020  000
10  101  102  000  000  000  000  000  000    000  000  000  000  000  000  000  000
20  000  000  000  000  000  000  11C  022    132  133  131  000  027  000  000  000
30  001  000  000  000  000  000  000  000    000  000  001  080  11C  000  13E  021

40  000  000  033  000  000  080  000  000    06E  002  040  06A  002  040  000  000
50  111  112  000  000  000  000  040  000    000  000  000  000  000  000  000  000
60  000  000  000  000  000  000  110  022    000  000  000  000  000  000  000  000
70  001  000  000  000  000  000  000  000    000  000  007  04F  000  000  000  007

80  000  000  033  000  000  080  000  000    06E  002  040  06A  002  040  000  010
90  111  112  000  000  000  000  040  000    000  000  000  000  182  000  000  000
A0  000  000  000  000  000  000  110  022    000  000  000  000  000  000  000  000
B0  001  000  000  000  000  000  000  000    000  000  007  000  000  000  000  007

C0  000  000  007  000  000  080  000  000    000  000  000  000  000  000  000  000
D0  000  000  000  000  000  000  000  000    000  000  000  000  000  000  000  000
E0  000  000  000  000  000  000  1FF  022    000  000  000  000  000  000  000  000
F0  000  000  000  000  000  000  000  000    000  000  000  000  000  000  000  007
```

Figure 4-11 Typical Scratchpad Memory Printout

Table 4-6 E-QLT Faults

YY = Test	MOST LIKELY UNIT 1	2	3	COMMENTS
0	CPU	-	-	Check operator control panel
1	CPU	MM	Cache	Check system bus
2	CPU	MM	Cache	Check system bus
3	CPU	MM	Cache	Check system bus
4	CPU	MM	Cache	Check system bus
5-11	-	-	-	Refer to subsection 4.1.5.1
12	IOM	-	-	-
13-32	CPU	IOM	-	-
33	IOM	CPU	-	Check CPU PAT-PAC
34	IOM	CPU	-	Eliminate pager and cache
35	-	-	-	Refer to subsection 4.1.5.2
36*	CPU	IOM	MM	-
37	CPU	IOM	-	-
40-45	CPU	MM	-	-
46	CPU	IOM	SSC	Refer to subsection 4.1.5.3 for E-QLT software description
XX = Fault	1	2	3	COMMENTS
00	IOM	CPU	System Bus	-
10	IOM	-	-	-
20	MM	-	-	-
40	CPU	-	-	-
50	CPU	IOM	-	-
60	CPU	MM	-	-
70	MM	CPU	IOM	-
14	IOM	Any I/O Bus Unit		-

*If Test 36 hangs, press CLR (Master Clear) and display register A3:

- If A3 bits 8 through 11 are equal to 1010, there is a possible main memory or cache parity problem.
- If A3 bits 8 through 11 are not equal to 1010, there is a CPU or I/O problem.

NOTE

The panel format is XX00YY.

9. The E-QLTs for the SSC and its associated adapters are as follows:

   a. If the SSC PROM board (BD2SSC) is BSSC001B-001 or higher, the SSC contains special E-QLTs to aid in the isolation of malfunctions to the console channel or the diskette channel. The E-QLTs are not related to the operator control panel (D2) E-QLTs. The only devices involved in the SSC E-QLTs are the console, the diskette, the SSC and its adapters, and the power supply with its interconnecting cables.

   b. To execute the SSC E-QLTs, enter an * (asterisk) at the console after first verifying that the console and diskette devices are in the ready condition. Any type of floppy disk may be inserted into the diskette.

   c. If the console is ready, two lines of all printable characters are printed (see TEST RESULTS below step e).

   d. If the diskette is loaded and ready, a test steps the head and checks the index pulses. After successful completion of these two tests, the device ready logic indicates a normal device ready status.

   e. Upon successful completion of steps c and d, an END OF TEST message is printed.

TEST RESULTS

```
 !"#$%&'()*+,-./0123456789:;<=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz{|}~
 !"#$%&'()*+,-./0123456789:;<=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz{|}~
END OF  SSC EXT QLTS
```

   f. If the SSC E-QLTs do not run to completion, an examination of the E-QLT error byte (QLTB) aids in isolating the malfunction. To access the E-QLT error byte, enter the following program into memory by using the operator control panel:

MEMORY ADDRESS	MACHINE CODE	OPERATION
5000	073000	Select Channel 00
5001	233100	NOP
5002	004004	LDAQ
5003	533300	CCQ
5004	433100	DIS
5005	071773	TRA-5
5006	000705	FC, Channel No.,
5007	000000	& SPM Address

g. Select D1 and Write/Execute to turn OFF the elapsed timer.

h. Start the instruction counter at 5000 (A0 = 5000) and step through address 5005 until A0 wraps back to 5001.

i. Read register A5 as follows:

A5	PROBLEM AREA
0 0 0 0 0 0 1 0 0 0 0 0 0 2 0 0 0 0	Console Channel Diskette Channel

NOTE

If the console prints the contents of the SPM in response to typing a ?, the QLTB is at hexadecimal location 5. The format (in hexadecimal) is:

```
                0 1 2 3  4 5 6 7
Bits 0 0 0 0 0 0 0 0  0 0 0 0
                  |     └──→ If = 1, diskette channel problem.
                  └────────→ If = 1, console channel problem.
```

NOTES

1. Changing the last two octal characters in location 5006 of the preceding program allows the reading of any two locations of the SPM quadrant that are addressed. Although the two character addresses may be odd, the SSC treats it as the next lower even address.

2. Changing the channel number selected in location 5000 of the preceeding program changes the SPM quadrant selected:

   SEL 00 = Channel No. 0, Console, SPM Quadrant No. 0.

   SEL 01 = Channel No. 1, Diskette, SPM Quadrant No. 2.

   SEL 40 = Channel No. 40, WAC, SPM Quadrant No. 3.

   SPM quadrant no. 1 is not used at this time. Refer to the product manuals listed in subsection 1.2 for a definition and description of the associated SPM locations.

3. The relationship of SPM data to register A5 data is shown in Figure 4-12.

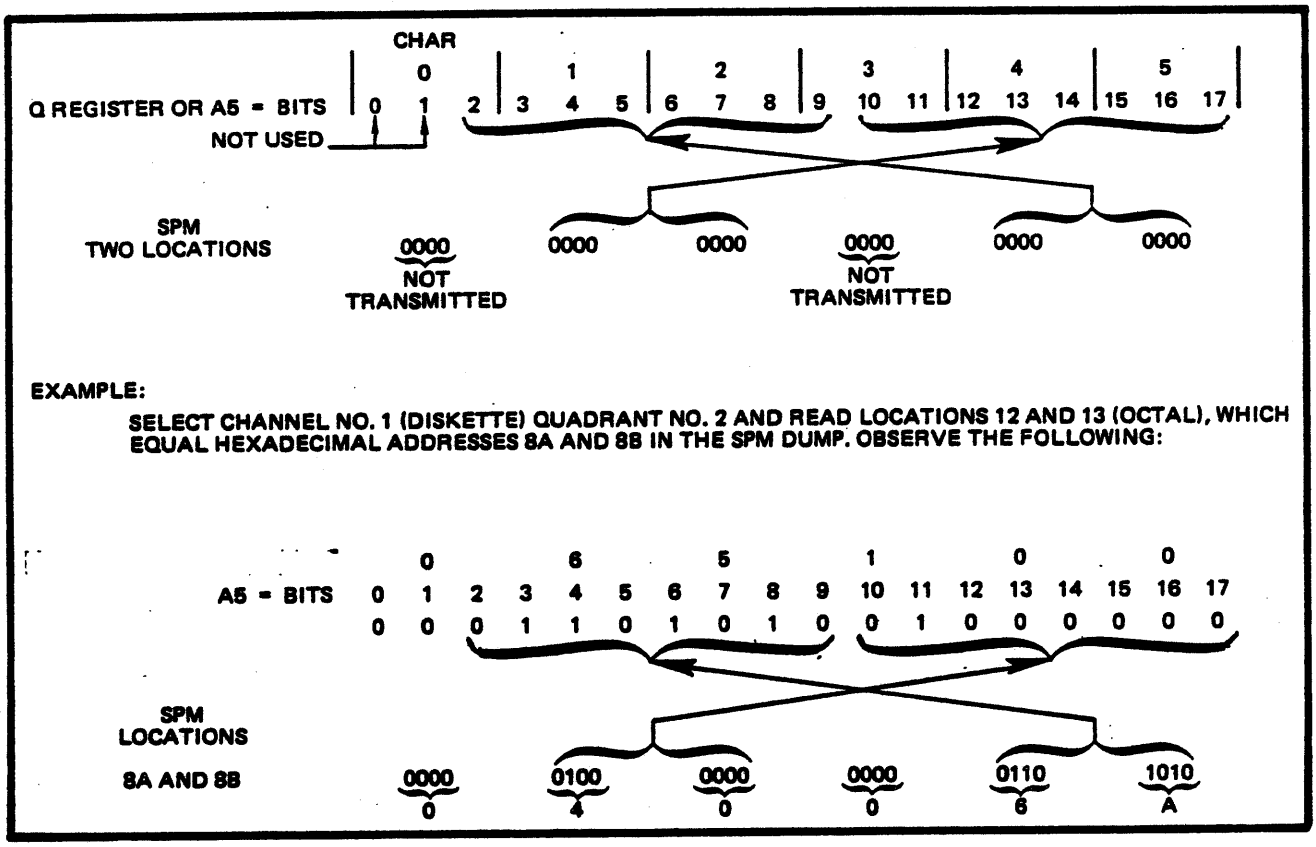


Figure 4-12 Relationship of SPM Data to Register A5 Data

4.1.5.1 E-QLT Memory Tests 5, 6, 7, 10, and 11

The E-QLT memory tests are:

- Test 5: The CPU writes and reads all data patterns in memory location 0.
- Test 6: The CPU writes and reads all data patterns in memory location 1.
- Test 7: The CPU writes 16K words of memory.
- Test 10: The CPU reads back and checks the 16K words of memory written in Test 7.
- Test 11: The IOM performs tests 5, 6, 7, and 10, and tells the CPU that they passed or which test failed.

If the CPU fails in one of tests 5, 6, 7, or 10, it stops. The operator control panel displays the failing test, and the IOM performs the test. The CPU results and the IOM results are used to determine the failing unit. The results are the XX bits in Table 4-6 and are shown on the operator control panel.

NOTES

1. Eliminate the cache if the CPU is indicated by the XX bits.

2. Eliminate the pager if memory is indicated by the XX bits.

3. PAT-PACs may cause address test failures on respective units.

For tests 5, 6, 7, 10 (if they fail) or for test 11, the contents of register A3 represent the status of the IOM and are as follows:

- 000010: I/O passed the memory test.
- 000011: I/O failed data test location 0.
- 000012: I/O failed data test location 1.
- 000014: I/O failed main memory address test.
- 740000: I/O failed main memory function code wraparound test.

4.1.5.2 E-QLT Test 35

Refer to subsection 4.1.5.3 for general information related to E-QLT 35. Refer to subsection 4.1.5.4 (subdivisions 4.1.5.4.1 through 4.1.5.4.6) for explanations of E-QLT subtests 00 through 05.

To perform E-QLT 35, proceed as follows:

1. When the panel displays XX0035, press the CLR (Clear) push button. The panel displays 140035.

2. Read register A3 as follows:

   a. When register A3 is 0, 1, or 2, proceed as follows:

CAUTION

When removing boards from the system, the power must be OFF.

(1) Remove all units from the I/O bus except the IOM.

(2) Rerun the E-QLTs.

(3) When the panel displays the XX0035, press the CLR (Clear) push button. The panel displays 140035.

(4) Read register A3 as follows:

(a) When register A3 is 0, 1, or 2, replace the IOM.

(b) When register A3 is 3, reinsert one I/O unit and rerun the E-QLTs. Observe the panel display as above. Continue this process until A3 is 0, 1, or 2. At this point, the last unit reinserted is the failing unit.

b. When register A3 is 3, proceed as follows:

(1) Remove all units from the I/O bus except the IOM and the SSC.

(2) Rerun the E-QLTs.

(a) If the E-QLTs fail, reinsert all units on the bus and attempt to run the Partial Online (POL) T&Ds. If the POL T&Ds boot and run, replace the SSC; if POL T&Ds do not boot, replace the IOM.

(b) If the E-QLTs pass, reinsert one unit at a time and run the E-QLTs until A3 is 3. At this point, the last unit reinserted is the failing unit.

c. When register A3 is 4 or 5, proceed as in item b above, but do not remove all the units at once. Remove them one at a time, starting at the top of the I/O bus until the faulty unit is found.

4.1.5.3 E-QLT Test 35 General/Print Buffer Information

GENERAL INFORMATION

Channel Number Table

004777 -- Number of ACKs received from the census sending.
005000 -- First channel that ACKed (or HMLC that waited).
005001 -- Second channel that ACKed.
005002 -- Third channel that ACKed.
005003 -- etc.

Interpreting Channel Number Table

The channel numbers in the preceding table are in a formatted form with the HMLCs first then the non-HMLCs, each in ascending channel number order.

HMLC Channel Numbers

020000-- 6 0
020400-- 6 1
021000-- 6 2
021400-- 6 3
022000-- 7 0
022400-- 7 1
023000-- 7 2
023400-- 7 3
024000--10 0
024400--10 1
025000--10 2
025400--10 3

Non-HMLCs

034000--00
034040--01
034100--02
034140--03
034200--04
etc.

Fault Table

004770 -- Contents of register 1, usually fault.
004771 -- Contents of register 4, usually should-be data.
004772 -- Contents of register 3, usually data bits wrong.

Console ICW

```
000462    2060XX    Buffer at 6000.
000463    0000Y0    Tally (count of second half BC = Y).
```

- Set the buffer word to 206000 before printing.
- To dump the print buffer contents, write the following into memory:

```
000462---206000     9 bit, buffer at 6000

002000---073000     Select Channel 00
002001---060003     CIOC
002002---433100     DIS
002003---071777     TRA-1
002004---000000     PCW-1
002005---000044     PCW-2

000002---002001     Interrupt Vector
```

- Set register A0 to 002000, then press the RUN (R) and EXECUTE (E) push buttons.

PRINT BUFFER INFORMATION

The print buffer is located at 6000.

- Each print line is eight (10 octal) characters long.
- Each word contains two 9-bit print characters.

```
240--ASCII SPACE
260--ASCII ZERO
261--ASCII ONE
262--ASCII TWO
   etc.
267--ASCII SEVEN
215--ASCII CARRIAGE RETURN
212--ASCII LINE FEED
377--ASCII RUBOUT (FILL CHARACTER)
```

On the printed line, the HMLCs are four characters.

- The first two characters are the subchannel.
- The second two characters are the channel.

```
0006--- Channel 6, Subchannel 00
0207--- Channel 7, Subchannel 02
```

Non-HMLCs are preceded by two spaces, then the two-character channel number.

```
  00-- Channel 0
  04-- Channel 4
```

NOTE

The PIAs return only the two low-order bits of the channel number field; therefore, a PIA at channel 5 reports as being on channel 1.

4.1.5.4 E-QLT Test 35, Subtests 00 through 05

4.1.5.4.1 Subtest 00, I/O Data Bus Test

General Information

This test places all of the possible data patterns on the I/O bus, ACKs them, reads them back into the IOM, tests for faults (parity, etc.), and then compares the data. The first data pattern is all zeros and increments to all ones.

Failures

- Location 4770 contains channel fault status (if any).
- Location 4771 contains the should-be data.
- Location 4772 contains what the data was if there was a fault or the bits in error if there was no fault.

NOTE

If no data was stored, the values are:

Location 4770 = 073247.
Location 4771 = 073246.
Location 4772 = 073245.

- Unsolicited bus cycles from any unit on the I/O bus can cause this test to fail.
- Do not press the Break key during the E-QLTs.
- Do not touch the MPC during the E-QLTs.

Failure Procedure

If this test fails, proceed as follows:

1. Read locations 4770 through 4772 and retry the test.
2. Read memory locations 4770 through 4772 again to see if the failure is consistent.
3. Remove all units from the I/O bus (merely pulling the units out of bus 2 inches is sufficient) and retry the test.

4. If the test passes, reinsert each board one at a time; retry the test after each board insertion until one board causes the test to fail.

NOTE

If the test fails, replace the IOM, both of the terminators, or the backplane until the test passes.

4.1.5.4.2 Subtest 01, I/O Address Bus Test

General Information

This test places all of the possible data patterns on I/O bus address signal bits 5 through 22, reads them back into the IOM, tests for parity errors (etc.), and then compares the data out to the data received. The first data pattern tried is all zeros incremented to all ones.

Although the IOM is the only unit involved directly in this test, any unit on the bus can be causing the problem.

Failures

The failure procedures are the same as for subtest 00, entitled I/O Data Bus Test (refer to subsection 4.1.5.4.1).

4.1.5.4.3 Subtest 02, High-Order Address Bit Test

General Information

This test tests all the patterns of bits 0 through 3 of the I/O address bus, starting with F and ending with 0. The test uses the PIAC register in the IOM for the first time. These bits are used for all indirect bus cycles and/or for storage. Bit 3 can affect direct bus cycles. Although no other units are involved in this test, extraneous bus cycles can cause it to fail.

Failures

The failure procedures are the same as for subtest 00, entitled I/O Data Bus Test (refer to subsection 4.1.5.4.1).

4.1.5.4.4 Subtest 03, Firmware Starting Address Test

General Information

This test wraps around the I/O bus to test the starting address generation logic for the I/O bus, internal to the IOM. It is necessary first, however, to receive an STEX second half bus cycle from the WAC channel. If the WAC (SSC) is not present or does not respond, the CPU hangs in this test. Once the second half bus cycle is received, no other unit on the bus affects this test; however, extraneous bus cycles can cause it to fail.

Failures

- Location 4771 contains the vector sent out.
- Location 4772 contains the vector received.

The failure procedures are the same as for subtest 01 (refer to subsection 4.1.5.4.2) except that for this and for subsequent tests, the SSC cannot be removed.

VECTORS	CYCLE TYPE DESCRIPTION
0	OR to Storage
1	Indirect Store Single
2	Indirect Store Double
3	Indirect Load
4	Channel Fault

4.1.5.4.5 Subtest 04, Census Taker Test

General Information

This test sends STEXs to all HMLC controller boards, and then to all channel numbers between 00 and 40 octal. If it receives a Wait signal while sending to the HMLCs, it includes that channel number in the Channel Number Table (refer to subsection 4.1.5.3). A Wait from an HMLC is an error, but will be caught later; the print buffer will be available.

NOTE

Every channel number that neither NAKs nor Waits is written into the Channel Number Table.

Location 4777 contains the number of ACKs received. Locations 5000 and up contain the formatted channel numbers of the units on the bus. The HMLCs are first in ascending channel and subchannel order, then the non-HMLCs are in ascending order of the lowest channel number on a controller board.

During the second half of the test, as each channel responds with a second half bus cycle, it does so in the order of priority. Since each channel has a different CPU channel number to answer, the channel number of the responder can be deduced.

As each response is received, the console ICW in memory locations 462 and 463 is updated and a print buffer at memory location 6000- is loaded. If this test and subsequent tests are successful, the buffer contents will be printed on the console.

At the end of this test (7 milliseconds after the last second half bus cycle), the number of responses is compared to the number of ACKs received in the first (sending) part of the test. If they are not equal, the test fails.

These numbers are available to the operator in memory locations 4777 (ACKs received) and 0463 (second half bus cycles) shifted left three bits. Note that further information is available in the Channel Number Table (5000-) and the print buffer (6000-).

Possible Causes of Failure

- ACKs not equal to second half bus cycle

  --HMLC waited (responding to two channel numbers).

  --Two units on same channel number (dump the print buffer and compare to the configuration).

  --Some unit did not respond (Which one is not present in the print buffer).

  --Priority network problem (look for the Logical Or of the channel numbers).

- Other response

  --First unit not in the buffer is probably in error.

NOTE

With the exception of the IOM and SSC, remove the boards one at a time until the test does not fail.

Fault Analysis Procedure

Read memory location 4777 (ACKs received, 0000XX) and location 0463 (second half bus cycles, 000YY0). Check that they are equal to each other and to the number of boards on the I/O bus. If not, check that:

1. YY is less than XX and XX equals the number of boards on the I/O bus. Check the print buffer, starting in location 6000, to determine the missing channel number and replace that board.

2. XX is greater than the number of boards on the I/O bus. Check the Channel Number Table (subsection 4.1.5.3), starting at memory location 5000, to determine which channel number, reported in memory, does not exist in the system. If the channel number corresponds to a CIB channel, the problem is most likely caused by another CIB.

3. XX is less than the number of boards on the I/O bus. Check the print buffer to determine the missing channel number. Possibly two boards are using the same channel.

4.1.5.4.6 Subtest 05, Priority Network Tester

General Information

This test uses the listing of channel numbers in the table in subsection 4.1.5.3 (4777-) to have each possible pair of controller boards compete against each other on the priority network. This test is run only if the number of ACKs received in the previous test (4777) is greater than one. During this test, the unit whose channel number is contained in memory location 5000 is sent an STEX; the unit whose channel number is contained in memory location 5001 is also sent an STEX. When the IOM becomes not busy, only two second half bus cycles should be received. If only two are received, 5000 competes against 5002, 5003, and on up. Then 5001 against 5002, 5003, 5004, then 5002 against 5003, 5004, and so on until all of the possibilities of two are exhausted.

If more than two second half bus cycles are received, the number received is written into location 4770. The offset address from 5000 of the two units competing against each other is written into locations 4771 and 4772.

Figure 4-13 shows the logic diagram for the priority network.

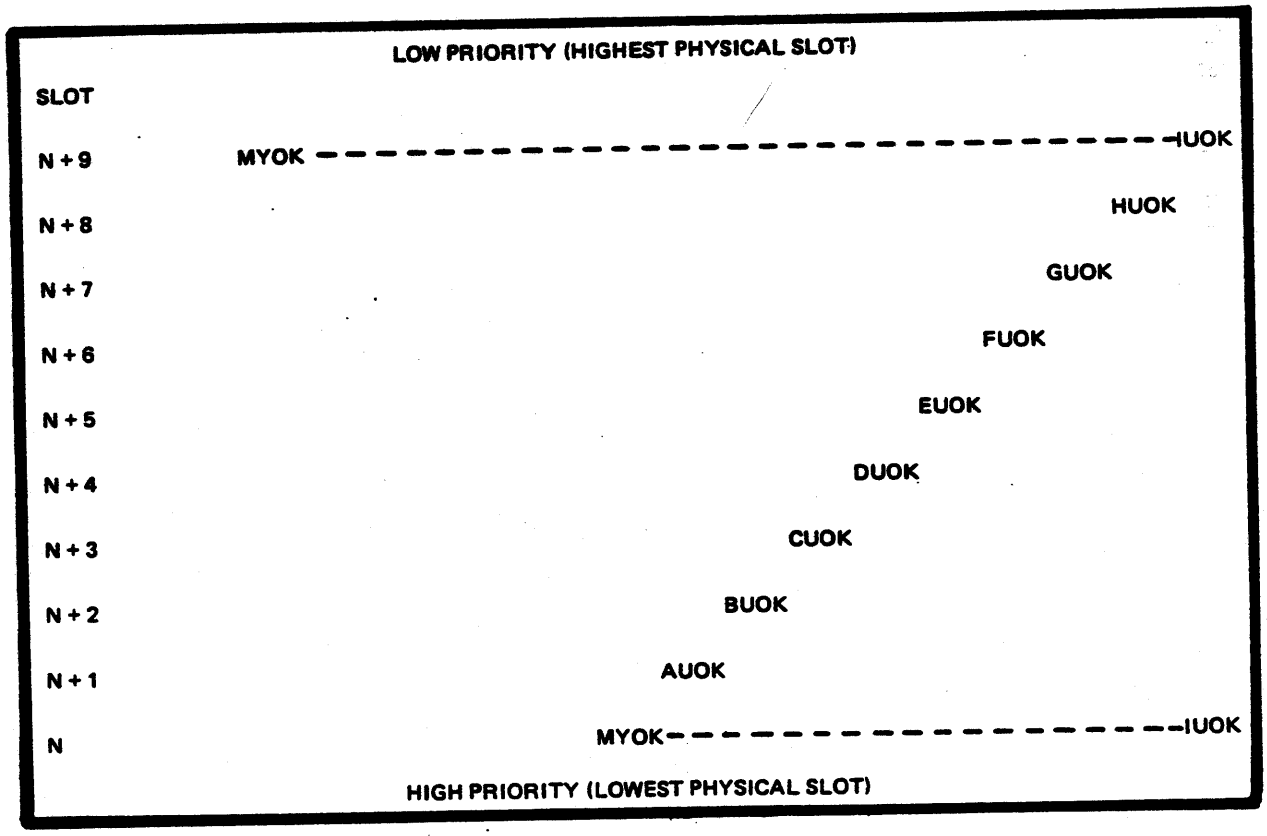


Figure 4-13 Priority Network Logic Diagram

If the priority network test fails, proceed as follows:

1. Press the CLR (Master Clear) push button.

2. Dump the printer buffer contents and compare to the system configuration.

3. Read memory locations 4770, 4771, and 4772:

   a. Location 4770 is the number of second half bus cycles and should be two.

   b. Location 4771 contains the pointer to the first board.

   c. Location 4772 contains the pointer to the second board.

4. If locations 4771 and 4772 are two, read location 5002. If they are three, read location 5003, etc. for the channel number; one of these two boards is probably at fault.

The priority network tester tests the ability of each board's MYOK signal to prevent each and every other board from getting on the bus at the same time.

The normal failure mode is that memory location 4770 equals 1 when the test fails. This means that only one second half bus cycle was received after sending out two STEXs to two channels, each of which previously acknowledged (and responded to) an STEX. The assumption is that both bus cycles were sent, but occurred on the bus at the same time because the priority network on one of the boards (or the bus) is defective.

- If a board's MYOK signal does not work, it will fail against all boards of lower priority.

- If a board's XUOK input signal does not work, it will fail against the MYOK signals of any board(s) that come from that slot.

- If the bus is malfunctioning (open), all boards in those slots always fail.

This test assumes that each channel number appears in the system only once. If this is not the case, the test fails and the indication is that memory location 4770 equals 3. This could also indicate that some channel is responding to a channel number other than its own.

If this test passes, the print buffer contents appear at the console. The operator must verify that the order of the channel numbers agrees with the actual configuration.

Fault Analysis Procedure

Perform fault analysis as follows:

1. Starting at the physical bottom of the I/O bus, check that all the boards are seated properly and have no empty slots between them.

2. Read and record memory locations 4770, 4771, and 4772:

   a. Location 4770 is the number of second half bus cycles and should be two.

   b. Location 4771 contains the memory location (refer to the Channel Number Table in subsection 4.1.5.3).

   c. Location 4772 contains the memory location (refer to the Channel Number Table in subsection 4.1.5.3).

3. Read and record the memory locations pointed to in locations 4771 and 4772, e.g.:

   a. If 4771 contains 000002, read memory location 5002.
   b. If 4772 contains 000005, read memory location 5005.

NOTES

1. The contents of locations 5002 and 5005 are unit channel numbers and one of these units is probably at fault.

2. If the number in location 4770 is greater than two, multiple units are responding to one of these two channel numbers.

4.1.5.5 E-QLT Software Test 46

Test 000046 of the E-QLTs writes a program into memory and then executes it. The program consists of three parts:

1. CPU internal (fault vector checking)

2. Printing a previously prepared print buffer on the console and interrupting

3. An I/O data check that involves the CPU, the IOM, and the SSC, using the LDEX and STEX T&D instructions.

The CPU is in the DIS state (register A0 equals 2056) during step 2 until it receives an interrupt. The interrupt vector is at memory location 0002 and points to 002050.

This test makes QR and (IND) equal to 000000. It also loads the ICR to the beginning of the program and starts the program running. It should end with 002042.

Initial Conditions

A0-- 002000
A1-- 002053
A2-- 002006
A3-- 002032
A5-- 000000
A6-- 000000

Program Listing

```
002     002050   -     Console Termination Interrupt Vector

440     001770   -              ---
        001770   -              ---
442     001770   -              ---
        001775   -     Illegal Op-Code Vector
444     001772   -     Overflow Fault Vector
        001770   -              ---
446     001770   -              ---
        001770   -              ---
460     104000   -     Status ICW for Console
        010000   -     Status ICW for Console
462     206000   -     Data ICW for Console
        000XXX   -     Data ICW for Console
                       XXX = Number of Characters in Print Buffer
1771    433100   DIS   Normal Error Stop
        XXXXXX   -     Address When Overflow Occurs
        006777   ADA   A4 = 413466
1774    055031   TOV   Transfer on Overflow          (T)
        XXXXXX   -     Address When Illegal Op-Code
1776    006777   ADA   Add to A
        071022   TRA   A4 = 152031, A5 = 004007
2000    673000   ILA   A4 = 000000                   Program Start
        074004   TZE   Transfer on Zero              (T)
2002    000000   -     Illegal Op-Code
        075777   TMI   Transfer on Minus             (F)
2004    065007   TPL   Transfer on Plus              (T)
        064775   TNZ   Transfer on Not Zero          (F)
2006    773003   IAA   A4 = 000003
        074773   TZE   Transfer on Zero              (F)
2010    464001   TNZ   Indirect TNZ                  (T)
        002003   -              ---
2012    000000   -              ---
        015775   ADAQ  A4 = 464004, A5 = 002003
2014    065776   TPL   Transfer on Plus              (F)
        075002   TMI   Transfer on Minus             (T)
2016    000000   -              ---
        233401   LLR   Long Left Rotate
2020    000000   -     Illegal Op-Code on Purpose
                 -     A4 = 150010, A5 = 004007
        055777   TOV   Transfer on Overflow          (F)
```

Program Listing (Cont'd)

```
2022    157773  STQ             ---
        206040  ADA   A4 = 156040, A5 = 004007
2024    006773  ADA   A4 = 411441, Generate an Overflow
        327012  CMPA  Compare Result
2026    064743  TNZ   Transfer on Not Equal          (F)
        071023  TRA   Branch to I/O Program
2030    073040  SEL   Select WAC Channel
        030011  LDEX  Send Data to SSC
2032    070013  STEX  Receive Data from SSC
        007007  LDA   A4 = Data Sent
2034    027011  CMPA  Compare Data Sent and Received
        064734  TNZ   Branch If Not Equal
2036    773001  IAA   Increment the Data Sent by 1
        017003  STA             ---
2040    045770  TNC   Test End of Test
        433100  DIS   Normal Termination
                      Wait for Console Interrupt
2042    000000   -    Data Sent to SSC
        004000   -    Overflow Inhibit
2044    413466   -    Expected Result
        XXXXXX   -    Data Received from SSC
2046    XXXXXX   -    A5 Stored from STQ (2022)
        ------   -    Unused Location
2050    XXXXXX   -    Should Contain 2056 After Test
        071757  TRA   I/O Interrupt Return (via 002)
2052    044771  LDI   Set Overflow Fault Inhibit
        073000  SEL   Select Console Channel
2054    060002  CIOC  Print Buffer on Console
        433100  DIS   Wait for I/O Interrupt
2056    000000   -    Peripheral Control Word
        000044   -    PCW, Write Command for Console
```

The following information shows the correct sequence of execution of the program. To restart the program, ensure the following:

1. Register A0 equals 002000.
2. Register A5 equals 000000.
3. Register A6 equals 000000.
4. Main memory location 462 equals 206000.
5. Main memory location 463 indicates the number of characters in the printer buffer.

NOTE

Ensure that main memory locations 400 and 402 are Zero.

The sequence of execution of the program follows. The asterisks indicate the addresses that are visible on the operator control panel while single stepping.

```
* 2000  ILA
* 2001  TZE  (T)
  2005  TNZ  (F)
  2006  IAA
* 2007  TZE  (F)
  2010  TNZ  (T)  Indirect
  2003  TMI  (F)
  2004  TPL  (T)
  2013  ADAQ
* 2014  TPL  (F)
  2015  TMI  (T)
  2017  LLR
* 2020  Illegal Op-Code
  1776  ADA
* 1777  TRA
  2021  TOV  (F)
  2022  STQ  Index A1
* 2023  ADA  Index A2
* 2024  ADA  Generate an Overflow
  1773  ADA
* 1774  TOV  (T)
  2025  CMPA Index A3
* 2026  TNZ  (F)
  2027  TRA
  2052  LDI
  2053  SEL
+ 2054  CIOC
  2055  DIS  When single stepping, the DIS is not executed
  2051  TRA
  2030  SEL
* 2031  LDEX
* 2032  STEX
* 2033  LDA
* 2034  CMPA   This loop is executed 256,000 times
* 2035  TNZ
  2036  IAA
* 2037  STA
* 2040  TNC
  2041  DIS
```

4.1.6 Test and Diagnostic Procedures

This subsection contains the procedures for running the T&Ds. The bootload sequence and bootload fault analysis are also described.

4.1.6.1 Running the T&Ds

To run the T&Ds, proceed as follows:

1. Mount the T&D diskette that is to be run.
2. Press the CLR (Clear) push button on the control panel (see Figure 4-2).
3. Select register B0 from the control panel.
4. Press the E (Execute) push button on the control panel.
5. The diskette executes some basic tests on the CPU and on the memory. After approximately 5 seconds, the diskette stops and a message is printed out on the console. The T&D Executive is now loaded and ready to execute the T&Ds.
6. For information on specific T&Ds, refer to the Network Processor Operation Manual (Order Number AY34).

4.1.6.2 Bootload Sequence

The bootload sequence of events follows:

1. Select register B0 and press the E (Execute) push button.
2. The CPU:
   a. Clears the first 600 (octal) memory locations to 0.
   b. Lights the RUN indicator.
   c. Writes Indirect Control Words (ICWs) into locations 464 through 467 (initial setting 101000, 010001, 400000, 000000).
   d. Places the control panel in Select mode.
   e. Issues a Connect to the diskette through the IOM.
3. The SSC reads a record from the diskette (audible click).
4. The CPU places the control panel into A0 mode (from B0), goes to the Disconnect (DIS) state, and the CP indicator goes OFF.

5. The SSC loads memory through the IOM, using the ICW in 464 through 467.

6. The CPU:

   a. Causes the CP panel indicator to blink 5 or 6 times and then stay ON for approximately 10 seconds.

   b. Executes the Primitive Function Tests (PFTs).

   c. Issues a Connect to the diskette.

7. The SSC reads T&D Executive from the diskette (audible click).

8. The printout appears on the console.

4.1.6.3 Bootload Fault Analysis

The bootload fault analysis is described as follows:

1. If the CP LED on the operator control panel does not blink on and off 5 or 6 times, proceed as follows:

   a. Run the SSC E-QLTs in accordance with subsection 4.1.5, step 9.

   b. Try different T&D diskettes.

   c. Press the CLR push button and listen for an audible click from the diskette.

   d. Verify that the diskette power is ON.

   e. Verify that the diskette is connected correctly (refer to subsection 3.5.9.3).

NOTE

If operating problems persist, the most likely trouble areas are the BH2FLD board, the diskette, the interconnecting cables, and the T&D diskette.

2. If the CP LED on the control panel blinks on and off 5 or 6 times but a message is not printed out on the console, proceed as follows:

   a. Verify that the console is connected to the ac power and is online/ready with the paper correctly installed.

   b. Verify that the console is cabled correctly (refer to subsection 3.5.9.4).

c. Verify that the console prints out the contents of the SPM when a ? (question mark) is typed on the control panel. If the SPM printout does not occur, check the console, the console cabling, and the BD2CSL board.

d. Run the SSC E-QLTs in accordance with subsection 4.1.5, step 9.

3. If the console, the diskette, and the SSC appear to be operating correctly, proceed as follows:

   a. Disable the cache. This can be done by performing either one of the following steps:

      (1) Press CLR, D3, Write, Execute, B0, Read, Execute (bootload).

      (2) Power down (remove the diskette first) and pull the cache out of the bus; note that the cache is attached to the CPU and cannot be pulled completely out. Power up and reboot the T&Ds.

NOTE

When the cache is turned OFF, the cache LED will be ON and the CHECK indicator will be ON. To turn the cache back ON, press the CLR push button.

   b. Disable the pager by performing either one of the following steps:

      (1) On assembly 60132644 (level 2.1), set the hexadecimal rotary switch to position 4.

      (2) On assembly 60132953 (level 2.2), set the toggle switch to the right (refer to subsection 3.5.4 for detailed information).

4. If the bootloading T&Ds do not operate properly and if the E-QLTs do operate properly, the most likely trouble areas are the first 16K of memory, the CPU, the IOM, or the power supplies.

4.2 FAULT ANALYSIS REFERENCE INFORMATION

This subsection supplements the information contained in subsection 4.1 and includes general system data such as interrupt vectors, fault vector data, direct control words, indirect control words, word formats, and instruction sets.

4.2.1 Memory

This subsection contains a general memory map of the interrupt vectors and the I/O communications region.

General Memory Map

MEMORY ADDRESS (Octal)	FUNCTION
00 000 00 377	Interrupt Vectors
00 400	Interrupt Cells (Refer to Table 4-7)
00 417 00 420	IOM Detected Channel Fault Status - Stored Here (Refer to Table 4-8)
00 437 00 440	Processor Detected Fault Vectors (Refer to Table 4-10)
00 447 00 450	I/O Communications Region (Refer to Table 4-11)
00 777 01 000	I/O Communications Region Channel 6 (HMLC 0-3) (Optional Program Area)
01 777 02 000	I/O Communications Region Channel 7 (HMLC 4-7) (Optional Program Area)
02 777 03 000	I/O Communications Region Channel 10 (HMLC 8-11) (Optional Program Area)
03 777 04 000	
37 777 (16K) or 77 777 (32K)	Program Area

4.2.1.1 Interrupts

There are 256 interrupt cells that are divided into 16 levels with 16 cells each. The levels correspond to the words in memory, with the cells being equivalent to bit positions 0 through 15 within the level. Levels 0 through 15 are located in octals 400 through 417, respectively.

Masking is by level only. Interrupt service (answering) priority is by cells within a level, then by level (level 0 is the highest). The interrupt vector location corresponding to any cell (bit) within a level is found as follows:

(Interrupt Vector)
(Address, Octal) = Bit Position x 20, Octal) + (Level, Octal)

Conversely, if an interrupt vector location is known, the corresponding level is equal to the four least significant bits of the vector address, and the bit position (cell) is equal to the next four bits of the address.

Interrupt service is acomplished by the hardware forced (processor) execution of a TSY instruction (indirectly to the interrupt vector) upon hardware detection of an Interrupt Present signal. Visibility and control of interrupts is program controllable through the use of Processor Interrupt Control instructions. Table 4-7 shows the division of the interrupt cells.

4.2.1.2 Program Interrupt Vectors

Program interrupt vectors are 256 software-maintained memory addresses used to service external program interrupts. They reside in dedicated memory locations 00000 through 00377 (octal). Each location is associated with one of the 256 possible external interrupts to which the CPU can react. Each location stores the software address to which the CPU branches when it services the associated external interrupt. The level and cell number supplied by the IOM specifies which external interrupt is to be serviced and is used by the CPU to extract the associated program interrupt vector when the CPU processes an IOM external interrupt.

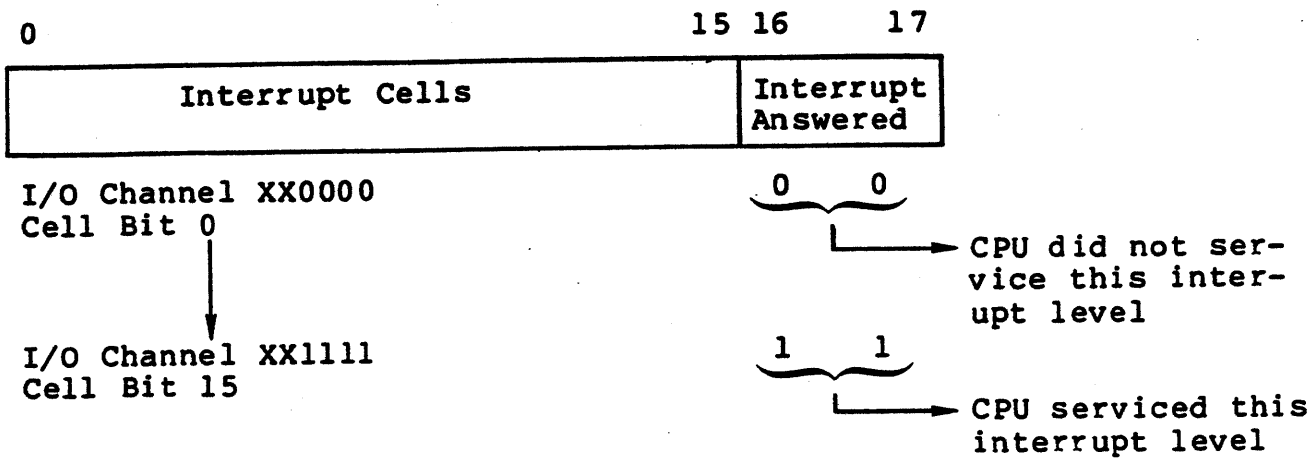
Table 4-7 Interrupt Cells

Level	Bit Position/Sublevel 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15	16**17**
0 (400)*	IOM Detected Channel Faults	
1 (401)	Miscellaneous Channel Specials & LSLA, Active	
2 (402)	Miscellaneous Channel Terminates & LSLA, Configuration	
3 (403)	ICA Specials (via SXC Command)	
4 (404)	Channel No. 6 HMLCs 0-3 — Active, Subchannels 0-15	
5 (405)		
6 (406)	Configuration, Subchannels 0-15	NOT
7 (407)	Configuration, Subchannels 16-31	
8 (410)	Channel No. 7 — Active, Subchannels 0-15	USED
9 (411)	Active, Subchannels 16-31	
10 (412)	Configuration, Subchannels 0-15	
11 (413)	Configuration, Subchannels 16-31	
12 (414)	Channel No. 8 — Active, Subchannels 0-15	
13 (415)	Active, Subchannels 16-31	
14 (416)	Configuration, Subchannels 0-15	
15 (417)	Configuration, Subchannels 16-31	

*Absolute memory addresses are in parenthesis.
**Bits 16 and 17 are set to One once an interrupt is serviced on a particular level.

4.2.1.3 Interrupt Level Words

Interrupt level words are the 16 dedicated main memory locations 00400 through 00417 (octal) that store IOM controlled interrupts pending information. Each of the 16 locations corresponds to the 16 I/O interrupt levels in the system and each location contains 16 interrupt cell bits which correspond to the 16 possible I/O interrupts that can be generated at each level as determined by the four low-order bits of the associated I/O channel address. This makes a total of 256 interrupt cell bits arranged in a 16-level by 16-bits-per-level priority array. If any interrupt cell bit is set, an external interrupt is pending from the corresponding I/O channel. Bits 16 and 17 of each interrupt level word specify if the CPU answered the interrupt at that level. The format for an interrupt level word is as follows:



The IOM controls information stored in these dedicated locations. The IOM sets the corresponding interrupt cell bit in the appropriate level word when it receives an interrupt from an I/O channel. In response to the set cell, the IOM sends an interrupt signal to the CPU. When the CPU answers the interrupt, the IOM scans the interrupt level words and sends the highest enabled priority level and cell number to the CPU, resets the associated cell bit, and sets the answer interrupt bits in the corresponding level word. Software resets the answer interrupt bits during interrupt processing.

For diagnostic purposes, any interrupt cell bit can be set and cause the IOM to generate the corresponding external interrupt by execution of a Set Interrupt Cell (SIC) instruction. The SIC instruction is used only to set cell bits for test and verification operations.

4.2.1.4 Fault Handling

The IOM detected faults result in a Fault Status Word (FSW) being sent to either the CPU or the I/O channel, depending upon the operation being performed. If the IOM is performing a CPU function when a fault is detected, the IOM stores the status word in memory location 437 (octal) and sets the CPU interrupt. If the IOM is performing an indirect data transfer when a fault is detected, the IOM sends the status word and tally counts to either the I/O channel performing the function (indirect load) or to the universal channel number (indirect store).

4.2.1.5 IOM Detected Channel Faults

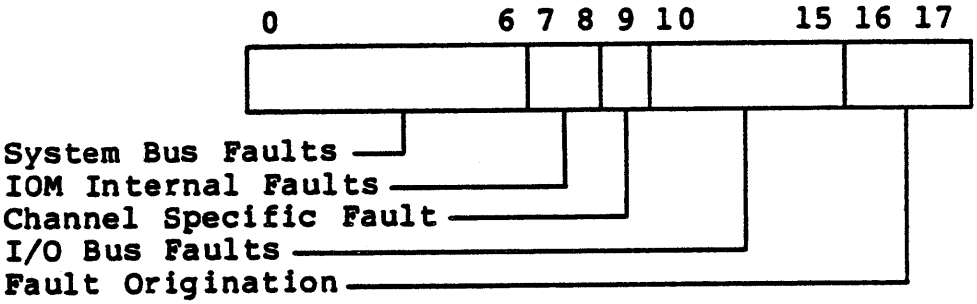
Memory locations 420 through 437 (octal) are reserved for storage of IOM detected fault information (see Table 4-8). The occurrence of an IOM detected fault results in the storage of the fault information, followed by a level zero (fault) interrupt.

Table 4-8 IOM Detected Channel Faults

HNP STORED ADDRESS (Octal)	FAULT INFORMATION STORED FOR I/O CHANNEL NUMBER & FUNCTION	CORRESPONDING INTERRUPT VECTOR LOCATION (All Level 0 Interrupts)
00 420	Channel 0 (Console)	00 000
421	1 (Diskette)	00 420
422	2 (*)	*
423	3 (HPIA)	00 060
424	4 (HDIA)	00 100
425	5 (HPIA)	00 120
426	6 (HMLC 0-3)	00 140
427	7 (HMLC 4-7)	00 160
430	10 (HMLC 8-11)	00 200
	(*)	*
00 437	Channel 17 (Timer/IOM-CPU Fault)	00 360

*Nonstandard configuration or not supported on the system.

The format and significance of the FSW is as follows:



System Bus Faults

Bit 0: When One, the IOM detected an uncorrectable error indication (red) from the system main memory unit.

Bit 1: When One, the IOM received an illegal function code from a component on the system bus.

Bit 2: When One, the IOM detected a parity error on data bus lines A and 0 through 7 (left byte).

Bit 3: When One, the IOM detected a parity error on data bus lines B and 8 through 15 (right byte).

Bit 4: When One, the IOM detected a parity error on the address bus lines.

Bit 5: When One, the IOM performed a Dead Man Timeout on the system bus.

Bit 6: When One, the IOM detected a bus logic test error or a bus continuity error on the system bus. This condition will never initiate the fault reporting sequence but will be set only as a system status indication.

IOM Internal Faults

Bit 7: When One, the IOM detected a Read Only Storage (ROS) parity error. Any ROS parity error detected while attempting to report any fault halts the I/O processor.

Bit 8: When One, the IOM page table unit indicated a fault.

Channel Specific Fault

Bit 9: Is not used.

I/O Bus Faults

Bit 10: When One, the IOM received an illegal function code from a channel on the I/O bus.

Bit 11: When One, the IOM detected a parity error on data bus lines A and 0 through 7 (left byte).

Bit 12: When One, the IOM detected a parity error on data bus lines B and 8 through 15 (right byte).

Bit 13: When One, the IOM detected a parity error on the address bus bits (0 through 7) signal lines.

Bit 14: When One, the IOM received an illegal NAK response on the I/O bus.

Bit 15: When One, the I/O bus failed the bus logic test or the IOM detected an I/O bus continuity error. This condition will never initiate the fault reporting sequence but will be set only as a system status indication.

Fault Origination

Bits 16 and 17: When One, the IOM detected the fault and originated this FSW.

4.2.1.6 Channel Fault Status Word

For interpretation of the various bits that make up the channel fault status word, refer to Table 4-9.

Table 4-9 Channel Fault Status Bit Definitions

BIT	SYSTEM BUS FAULTS
0	Red from Main Memory
1	Illegal Function Code
2	Upper Data Bus Parity
3	Lower Data Bus Parity
4	Parity Error Address Bits 5 through 7
5	Illegal NAK on System Bus (Dead Man Timeout)
6	Bus Continuity Error
7	Read Only Storage Parity
8	Page Address Table Error
9	Channel Specific Channel Fault
BIT	**I/O BUS FAULTS**
10	Illegal Function Code
11	Upper Data Bus Parity
12	Lower Data Bus Parity
13	Parity Error Address Bits 0 through 7
14	Illegal NAK (DMTO)
15	Bus Continuity Error
16-17	11 = IOM Detected the Fault and Originated Status Word 10 = Channel Detected the Fault

If the I/O fault status word location is 426, 427, or 430 and if the channel detected the fault, the meaning of bits 0 through 8 is (for BMLC0B5A-005/BMLC005A-002 or higher):

Channel No. 6 -- Y01000XX0
Channel No. 7 -- Y01001XX0
Channel No. 10 -- Y01010XX0

where:

Y = Memory Red Indicator.
XX = MLC/CIB Board Number.

If the I/O fault status word corresponds to the DIA (normally location 424 if the DIA is on channel 4), then the format is as follows:

000 000 00U XY0 00Z 100

where:

DIA Detected Fault
- U = OR to Storage.
- X = OR to Storage OR Write to Storage.
- Y = Red from Main Memory.
- Z = Error Damage Report (IOM Detected Fault).

4.2.1.7 Processor Detected Faults

Faults (internal interrupts) are included in the processor to provide for program intervention when certain system errors or other events occur by automatic hardware forced transfer (TSY) to fixed storage locations called vectors (see Table 4-10). An indirect address is contained in the vector; it points to a software fault handling routine.

4.2.1.8 Processor Faults

A list of the processor faults follows:

1. Power Shutdown Beginning Fault (PF): This fault is triggered by an external signal to the computer, indicating impending power OFF. *

2. Power ON Restart Fault (PO): This fault is triggered by an external signal to the computer, indicating that power ON occurred. The computer initializes and transfers to the fault vector location. *

3. Memory Parity Error Fault (MP): This fault is triggered when a parity error occurs during a read from memory by the processor. This fault can be program inhibited by setting the Parity Fault Inhibit bit on the LDI instruction. System bus parity includes: an error in data parity, data transferred between the CPU and memory, data received from the cache memory unit or data received from the IOM, or the page unit detected bad parity on a bus write to memory.

4. Illegal Operation Code (OP): This fault occurs when the processor detects an illegal op-code. All codes not listed in subsections 4.2.4.2 through 4.2.10 are illegal.

Table 4-10 Processor Detected Faults

FAULT VECTOR LOCATION*	FAULT NAME	PRIORITY	UNCONDITIONAL ABORT	FAULT INHIBIT
00 440	Power Shutdown Beginning (PF)	1	No	-
00 441	Power ON Restart (PO)	7	Yes	-
00 442	Memory Parity Error (MP)	2	Yes on instruction and indirect cycle; No on operand cycle	By program control
00 443	Illegal Operation Code (OP)	4	Yes	-
00 444	Overflow (OV)	5	No	By program control
00 445	Illegal Memory Operation (IM)	3	Yes	-
00 446	Divide Check (DC)	6	No	-
00 447	Illegal Program Interrupt (II)	8	No	-
-	IOM Channel Detected Fault (CF)	9	-	-
-	Operator Induced Abort at Console (CN)	-	-	-
-	Extraneous Interrupt (XI)	-	-	-

*The last character of the fault vector is also the fault number.

5. Overflow Fault (OV): This fault is generated when an overflow occurs during an arithmetic operation. This fault can be program inhibited by setting the Overflow Fault Inhibit bit in the indicator register with the LDI instruction.

6. Illegal Memory Operation Fault (IM): This fault is generated for the following reasons:

   a. Memory controller timeout (hardware error)

   b. Illegal command to memory controller (hardware error)

   c. Out of bounds address

   d. Illegal character code (7 is the only illegal character, position code 1 acts like 0)

   e. Any attempt to alter storage in a protected area (paging only)

   f. A parity error in a Page Address Table Unit (PATU) entry when accessed during address formation.

   g. Page Control Unit (Pager) detects a Memory Parity (MP) error fault.

7. Divide Check Fault (DC): This fault is generated when a division cannot be carried out by a Divide instruction for any of the reasons indicated.

8. Illegal Program Interrupt Fault (II): The illegal program interrupt can be generated in two ways:

   a. The processor attempted to answer an interrupt when there was no interrupt present.

   b. The processor answered a valid interrupt; however, the contents of the word in storage containing the interrupt sublevels were all zeros. This can happen if the processor or the IOM stores a zero in one of the interrupt sublevel locations after an interrupt was set.

   This fault is detected by the IOM and is reported as an I/O interrupt to the CPU. When the CPU requests the interrupt vector address, the IOM returns the address of the CPU interrupt vector for this fault.

4.2.1.9 I/O Communications Region

Table 4-11 provides information that defines the I/O communications region (refer to subsections 4.2.1.9.1 through 4.2.1.9.3 for supplementary information).

Table 4-11 I/O Communications Region

FUNCTION	MEMORY ADDRESS ABSOLUTE OCTAL
Internal Timer	450
Elapsed Timer	451
Reserved for Software and T&D	452-453
HDIA Peripheral Control Word (PCW)	454-455
HDIA Status Indirect Control Word (ICW)	456-457
Console -- Status ICW	460-461
-- Data ICW	462-463
Diskette -- Status ICW	464-465
Data ICW	466-467
Data ICW (Alternate)	470-471
Reserved for Software and T&D	472-473
Page Table Pointers (PTP) -- IOM	474
-- CPU	475
Memory Yellow Counter -- EDAC*	476-477
(Not Used)	500-517
Control Panel Storage Area**	634
CPU Fault Status***	635
(Not Used)	636-637
Software Operator Interface	640-677

*Subsection 4.2.1.9.1
**Subsection 4.2.1.9.2
***Subsection 4.2.1.9.3

4.2.1.9.1 Memory Yellow Counter - EDAC

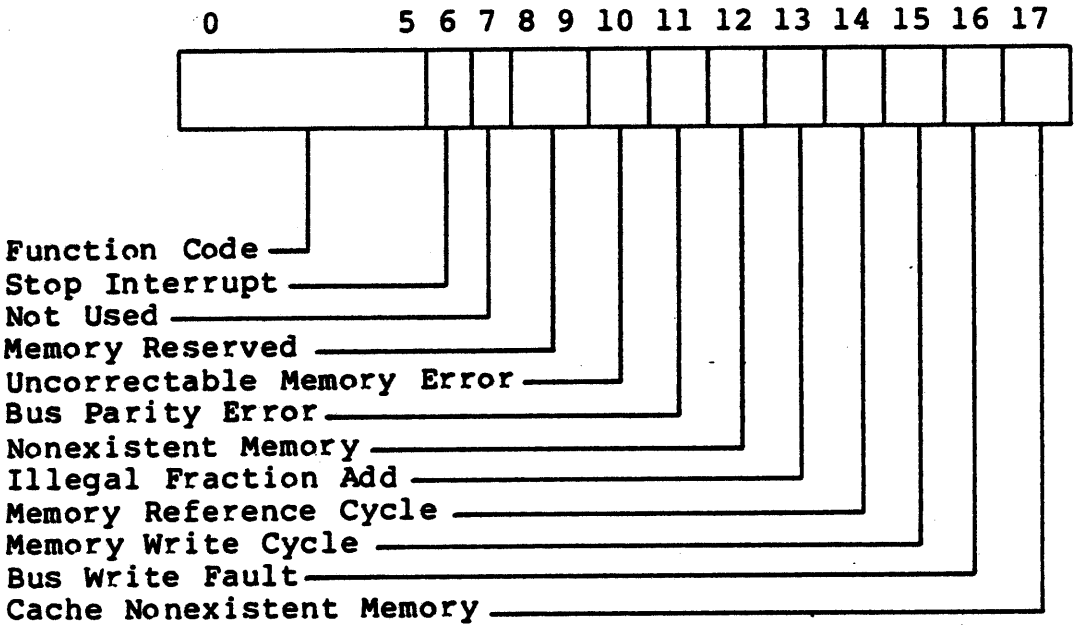
The IOM maintains two words in the IOM communications region at octal locations 476 and 477 as a count of the corrected memory errors, serving as a maintenance aid. The IOM increments the contents of these locations when main memory indicates that a word that was accessed had error correction applied to it by setting the Yellow indication on the bus. No interrupt is generated on an overflow of these words. The Yellow counter location is reset to Zero at power up or upon bootload.

4.2.1.9.2 Control Panel Address Buffer (Storage Area)

The control panel address buffer location is a CPU hardware controlled dedicated memory loction (00634 octal). It always contains the last address used to access memory on behalf of the control panel. The CPU firmware controls the information stored in this location. When a C0 Write is performed from the control panel, the CPU firmware loads the control panel data contents into this register. This address is then used by the CPU for subsequent panel accesses to memory.

4.2.1.9.3 CPU Fault Status (Applies to BF418A, Level 2.4)

The CPU fault status register is dedicated memory location 00635 (octal). It is used to store a CPU status word that defines the type of CPU fault when a parity error or an illegal store condition is detected. This location is controlled by the CPU firmware. It is cleared to all Zeros when the Initialize signal is received, and then loaded with the status word if either a Storage Parity Fault or an Illegal Operation Store Fault is detected. The format for the CPU fault status word is as follows:



Bits 0 through 5: These bits store the last function code received by the CPU.

Bit 6: This bit is a One if a Stop Interrupt is stored in the CPU when the error is detected.

Bit 7: Bit 7 is not used.

Bits 8 and 9: These bits indicate the condition to which the CPU has set the main memory Lock function during double-word and read-modify-write operations. These bits specify the following:

Bits 8, 9

1 0 = Lock, memory lock set by the CPU.
0 1 = Unlock, memory released from CPU use.
0 0 = Memory Lock function not used.
1 1 = Lock maintained, Memory Lock unchanged.

Bit 10: This bit is a One if main memory detects an uncorrectable (Red) read error during a CPU memory reference.

Bit 11: This bit is a One if the CPU detects a parity error on data received over the system bus.

Bit 12: This bit is a One if there is no response to a CPU generated memory reference bus cycle.

Bit 13: This bit is a One if during CPU address generation an attempt was made to modify a byte address by a character or word address stored in an index register or vice versa.

Bit 14: This bit is a One if the last system bus cycle generated by the CPU was a memory reference cycle.

Bit 15: This bit is a One if the last CPU generated system bus cycle was a memory write cycle.

Bit 16: This bit is a One if the page control unit detected illegal parity on the last memory write performed on the system bus by any unit.

Bit 17: This bit is set if cache memory attempts to access a nonexistent memory location.

4.2.2 Control Console Adapter

This subsection contains interrupt vectors, ICWs, control words, and op-codes for the Control Console Adapter (CCA).

IOM Channel Number: The channel number is 0.

Interrupt Vectors (Octal):

00000 = IOM detected fault.

00001 = Special, caused by a line break (no status store).

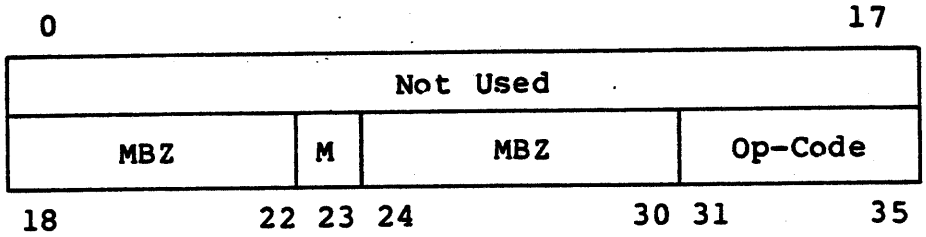
00002 = Terminate, caused by ICW, TY1, or TY0, Carriage Return (015) Control-X (030), X-off (023), or 30-second timer (preceded by a normal Status Store).

ICWs (Indirect 9):

Status = 460, 461
Data = 462, 463

Control Words:

Peripheral Control Word (PCW):



Bits 0 through 17: Not used.
Bits 18 through 22: Must be Zero.
Bit 23, Mask Bit (M): This must be a One to mask.
Bits 24 through 30: Must be Zero.
Bits 31 through 35: Op-Code.

Op-Codes

CODE	FUNCTION
00	Status Request
44	Write Mode
50	Read Mode
54	Wraparound Mode

Special (with STEX Y Instruction):

C (Y00-08) = Must be Zero.
C (Y09-14) = Contents of CCA Command Register.
C (Y15) = CCA Busy Bit.
C (Y16) = CCA Ready Bit.
C (Y17) = Mask.

Status (Normal - Stored Indirect - 9):

BIT	INDICATION (IF = 1)
0	Ready (DSR and CTS both up)
1	30-second timer runout occurred
2	Tally runout (TY0) occurred
3	Pre-tally runout (TY1) occurred
4	Data transfer timing error occurred
5	Control character detected
6	Illegal instruction sequence (CIOC while BSY)
7	Illegal instruction
8	Parity error (immediate interrupt not generated)

4.2.3 Diskette Adapter

This subsection contains interrupt vectors, ICWs, and control words for the diskette adapter.

IOM Channel Number: The channel number is 1.

Interrupt Vectors (Octal):

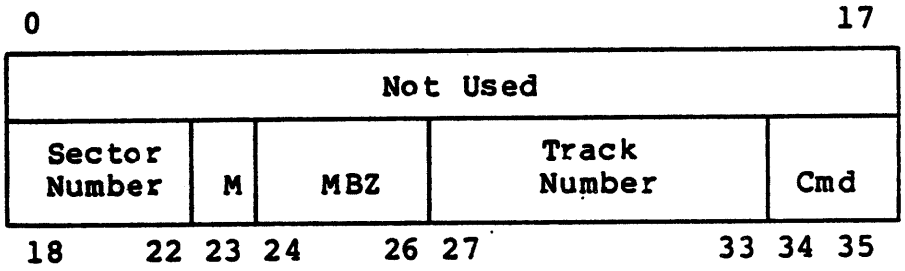
00020 = IOM detected fault.
00021 = Special interrupt.
00022 = Terminate interrupt, caused by PCW op-code of 00, track error, CRC error, TRO, or PTRO.

ICWs (Indirect - 18):

Status = 464, 465
Data = 466, 467
Data = 470, 471 (alternate)

Control Words:

Peripheral Control Word (PCW):



Bits 0 through 17: Not used.

Bits 18 through 22: These are the Sector Number bits:

BIT	SECTOR NUMBER (BCD Value)
18	16
19	8
20	4
21	2
22	1

Bit 23, Mask Bit (M): This must be a One to mask.

Bits 24 through 26: Must be Zero.

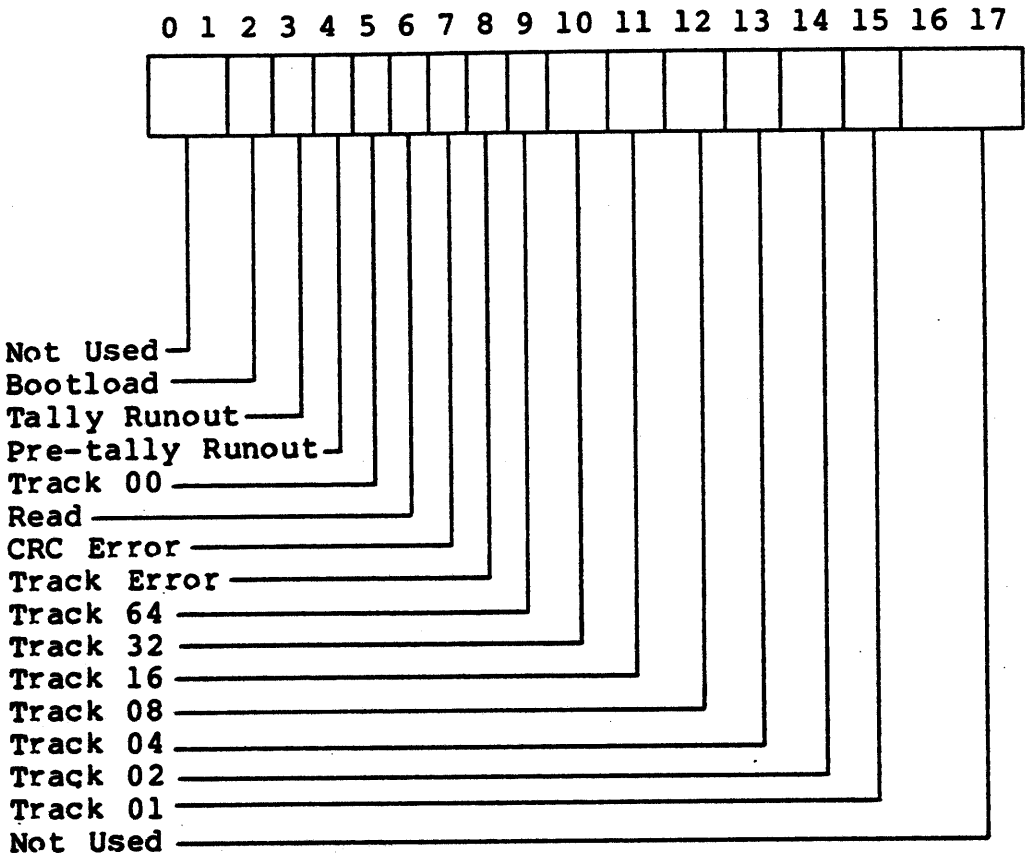
Bits 27 through 33: These are the Track Number bits:

BIT	TRACK NUMBER
27	64
28	32
29	16
30	8
31	4
32	2
33	1

Bits 34 and 35: These are the Command bits:

CODE	FUNCTION
00	Store Status
01	Read

Status (Normal - Stored Indirect - 18):



4.2.4 Peripheral Interface Adapter

This subsection contains interrupt vectors, ICWs, and control words for the Peripheral Interface Adapter (PIA). It also includes address data, Data Control Word (DCW) information, MPC commands, and PIA-MPC interface line data.

IOM Channel Number: The channel number is octal 03 or 05.

Interrupt Vectors:

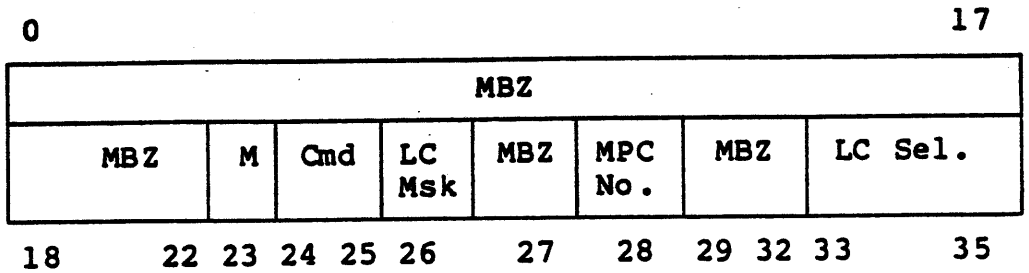
Level 1 (Special): Channel 3 = 61, Channel 5 = 121.
Level 2 (Terminate Marker): Channel 3 = 62, Channel 5 = 122.

ICWs:

Status = Software specified.
Data = Software specified.

Control Words:

Connect PCW (Operational Mode):



Bits 0 through 22: Must be Zero (used only for T&D mode).

Bit 23: Physical channel mask.

Bits 24 and 25: Physical channel command.

Channel Command Bits 23, 24, 25

BITS 23	24	25	DESCRIPTION
1	0	0	Mask PIA
0	0	0	Normal startup of LC
0	1	1	T&D PCW
1	1	1	Reset MPC and mask all LCs

Bit 26: Logical channel mask.

Bit 27: Must be Zero.

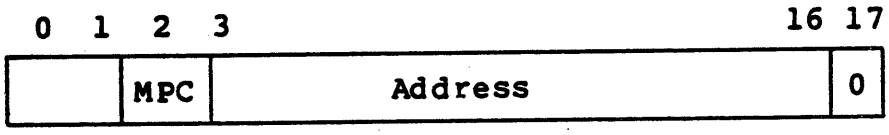
Bit 28: MPC select: Zero = MPC No. 1; One MPC No. 2.

Bit 29: Must be Zero.

Bits 33 through 35: Logical channel select.

4.2.4.1 Base Address Word

This subsection contains the starting address word format of the PIA mailbox. There must be a separate mailbox for each MPC. This function must be loaded by an LDEX instruction prior to issuing Connect. The format is as follows:



Bit 2 is the MPC select bit:

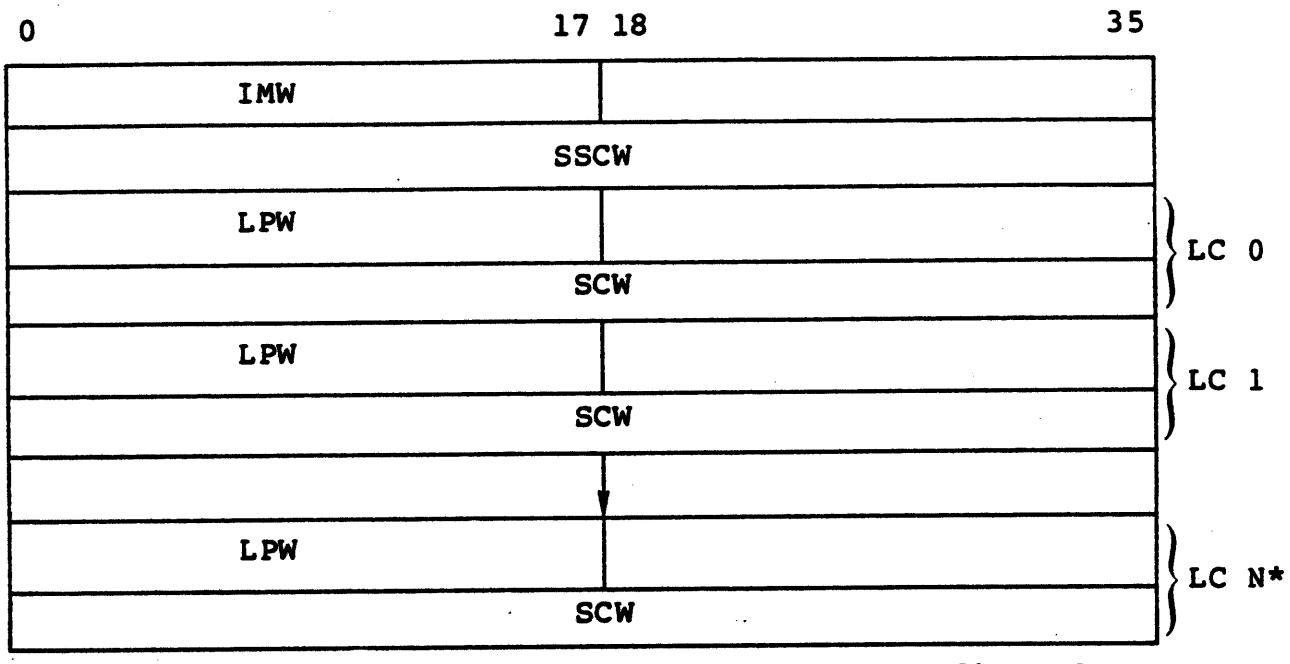
- When bit 2 is set to Zero, MPC 1 is selected.
- When bit 2 is set to One, MPC 2 is selected.

4.2.4.2 Mailbox

The mailbox format is as follows:

NOTE

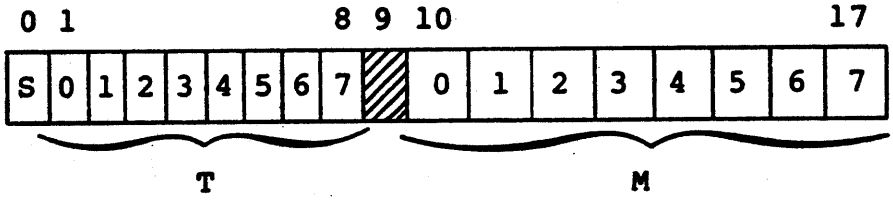
The address in the base address register points to the starting location of the mailbox area.



*A maximum of eight logical channels may be configured.

4.2.4.3 Interrupt Multiplex Word

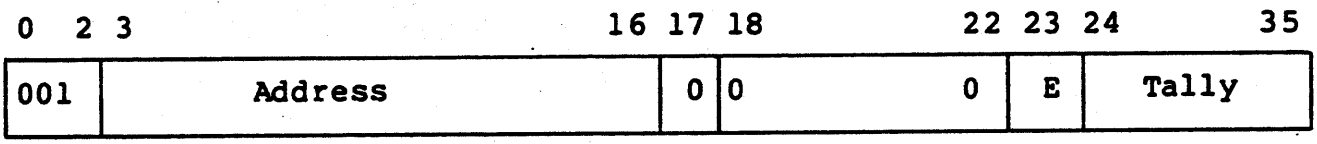
The Interrupt Multiplex Word (IMW) format is as follows:



Bit 0 (S): When set to One, a special interrupt occurs.
T Field: Terminate interrupt by the logical channel.
M Field: Marker interrupt by the logical channel.

4.2.4.4 Special Status Control Word/Status Control Word

The SSCW and SCW word formats are as follows:

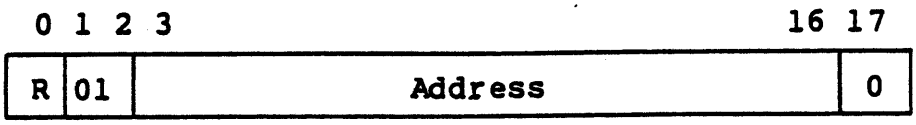


SSCW: Special Status Control Word (status is stored in ASCII format).

SCW: Status Control Word.

4.2.4.5 List Pointer Word

The List Pointer Word (LPW) format is as follows:



Bit 0, R (Restricted). When set to One, bit 0 restricts the DCW list services to one IDCW.

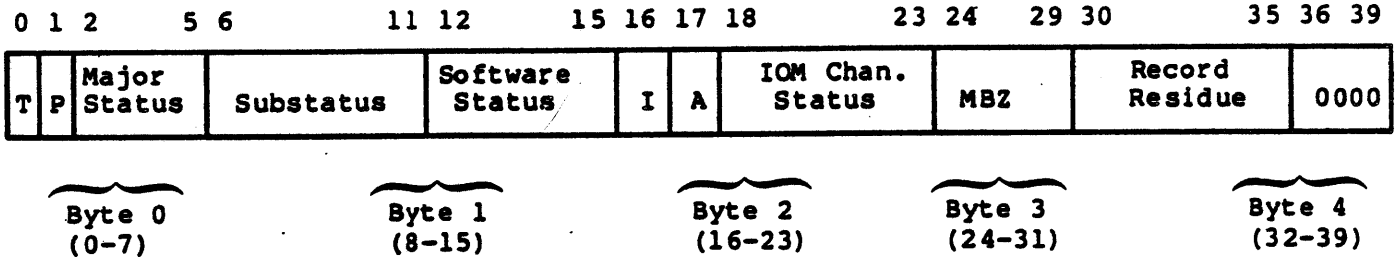
4.2.4.6 Status Words Formats

These formats are:

- Terminate/marker status, first word (5 bytes from MPC)
- Terminate/marker status, second word (36 bits from PIA).

Terminate/Marker Status, First Word

The format is:



Bit 0: This bit is set by the MPC when status is stored (software flag).

Bit 1, Power Bit: Bit 1 is set to One when the MPC power is OFF.

Bits 2 through 5: These bits show the MPC major status.

Bits 6 through 11: These bits show the MPC substatus.

NOTE

Refer to subsection 4.2.4.13 for the definitions of MPC Major Status/Substatus.

Bits 12 through 15: These are the software status bits and are stored as Zeros by the MPC. They can be used by the software to indicate software detected errors to the Slave program after the hardware has stored status word.

Bit 16, Initiate Interrupt: Bit 16 shows the status stored during an interrupt sequence (no data transfer).

Bit 17, Abort Bit: Bit 17 is stored as Zero by the MPC; it is set to One by the software if this transaction caused the program to abort.

Bits 18 through 23, IOM/Channel Status: These bits are divided into two independent 3-bit segments:

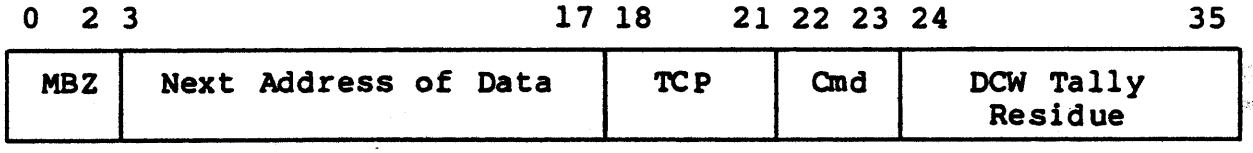
- Bits 18 through 20: Channel detected user faults.
- Bits 21 through 23: IOM detected user faults reported to the PSA.

Bits 24 through 29: Must be Zero.

Bits 30 through 35, Residue Record Count: These bits are illegal for the disk subsystem and are always stored as Zeros.

Terminate/Marker Status, Second Word

The format is:



Bits 0 through 2: Must be Zero.

Bits 3 through 17: These bits show the contents of the DCW register.

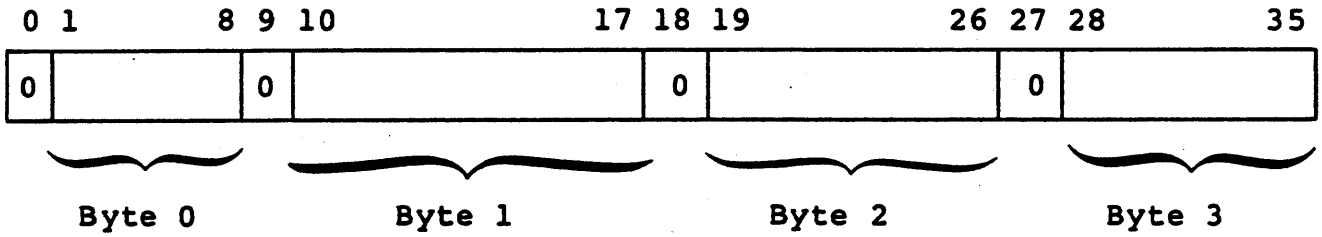
Bits 18 through 21: These bits contain the terminate character position code.

Bits 22 and 23: These bits are the DCW command.

Bits 24 through 25: These bits show the contents of the tally register.

Special Status (ASCII Format)

The format is:



Bits 1 through 8 (Byte 0): The MPC sends this character all Zeros.

Bits 10 through 17 (Byte 1): This is the MPC device number (MPC controller is device number 0).

NOTE

Bits 19 through 26 and 28 through 35 represent types of special interrupts.

Bits 19 through 26 (Byte 2): These bits indicate pack change (to all).

Bits 28 through 35 (Byte 3): These bits indicate device released (to unit of original request).

NOTE

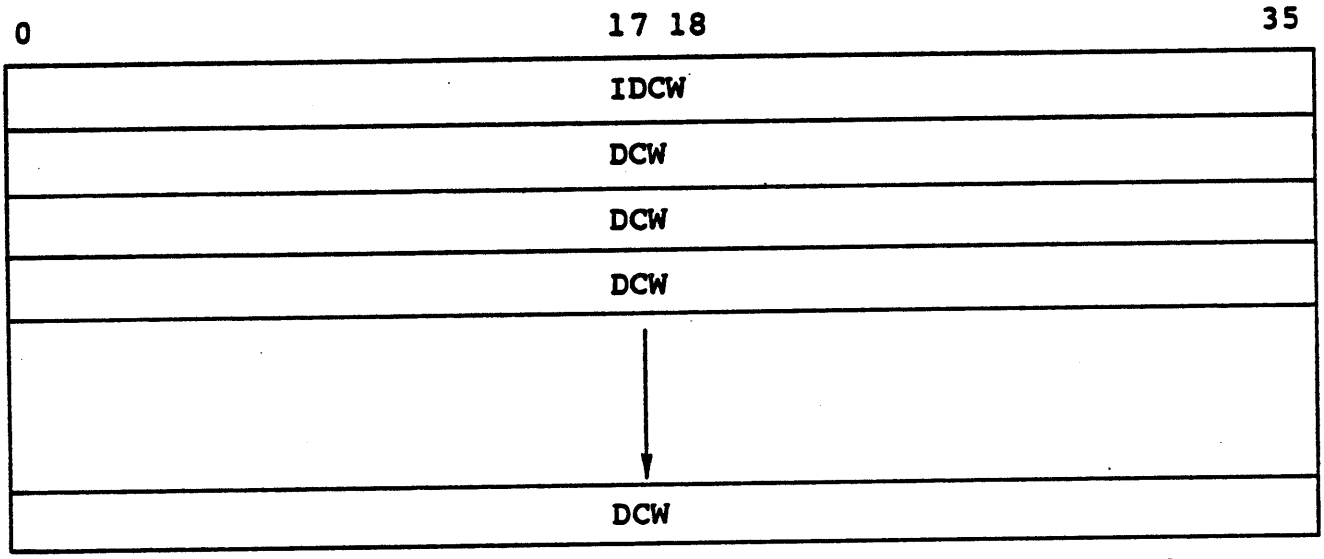
The Special Status Store is followed by a Special Interrupt (Level 1).

4.2.4.7 Logical Channel DCW List

The logical channel DCW list format is as follows:

NOTE

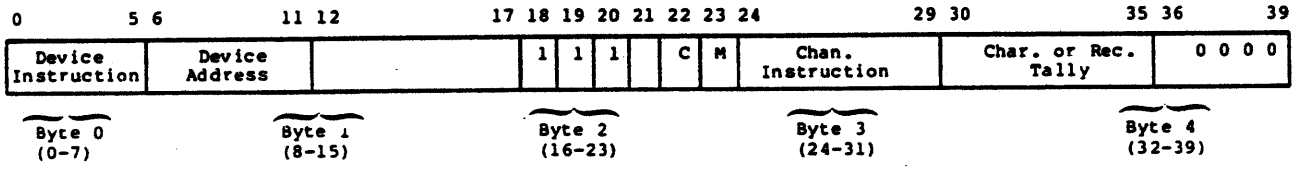
There are separate DCW lists for each logical channel configured.



The logical channel LPW in the PSA mailbox points to the starting address of the DCW List.

Instruction Data Control Word

The IDCW format is:



Bits 0 through 5: These bits are the MPC system command.

Bits 6 through 11: These bits are the device code.

NOTE

The first IDCW establishes the device code; subsequent IDCW device codes are ignored. This makes it impossible for a program to switch devices within a list.

Bits 12 through 17: These bits are ignored.

Bits 18 through 20: These bits must be ON (this distinguishes a DCW from an IDCW).

Bit 21: This bit is ignored.

Bit 22, Continue: This bit indicates this is not the last IDCW in the list. On completion of this IDCW, a Move Pointer Service Code is issued to obtain a new IDCW.

Bit 23, Marker Bit: This bit is ignored if bit 22 is not ON. On completion of the IDCW, the MPC issues service codes to Store Marker Status and Set Marker Interrupt. The MPC then issues a Move Pointer Service Code to obtain a new IDCW.

Bits 24 through 29, Channel Instruction: These bits must be one of the following:

- 00 - Unit Record Transfer.
- 02 - Peripheral Action (no data transfer; e.g., Request Status, Release, Restore).
- 2(X) - Command Extension Modifiers.
- 4(X) - Special Controller Commands.

If 2(X):

- 21 - Inhibit Automatic Retry.
- 22 - Inhibit Alternate Track Logic and EDAC logic.

- 23 - Special Permission Execution:

  Read Override RPS Queue.
  Write Override RPS Queue.

- 24 - EDAC Override (190); Check Character Override (181).

- 25 - Read and perform error corrections on data before transferring data to EUS (PSA).

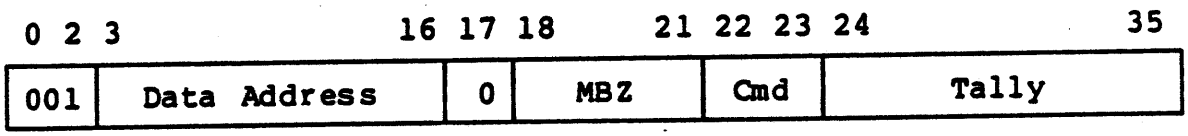
If 4(X):

- 40 - Special Controller Command (device address fields, bits 6 through 11, must be Zero).

Bits 30 through 35, Record Tally or Character: These bits contain the number of times the device instruction is to be reissued to the controller (channel instruction 02).

Data Control Word:

The DCW format is:



Bits 22, 23: These bits identify the type of DCW.

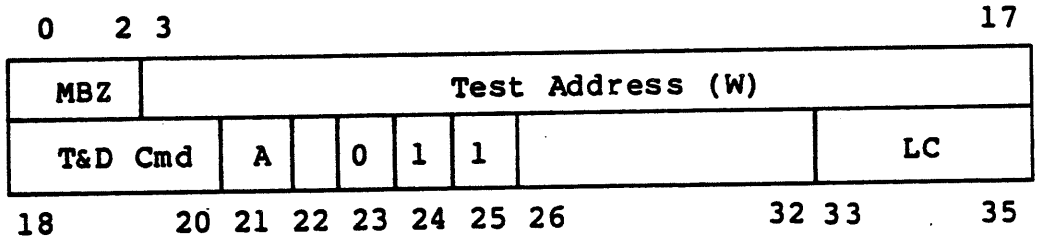
0	0 = I/O Transfer and Disconnect (IOTD).
0	1 = I/O Transfer and Proceed (IOTP).
1	0 = Transfer DCW (TDCW).
1	1 = I/O Nontransfer and Proceed (IONTP).

NOTE

For the DCW, note the following: (1) pseudo read/write operation (2) write uses one location of memory, and (3) no update occurs for the DCW.

4.2.4.8 Test and Diagnostic Mode

The T&D PCW word format is:



FN01

T&D COMMAND (Octal)	COMMAND DESCRIPTION	TEST ADDRESS (W)	LOGICAL CHANNEL (LC)	ASCII (A)
0	Data Wraparound (Four 36-bit words) From 0-7 to 10-16	Must be Zero	Used to generate a location for storing LPW Register (Stored in LPW +1 location)	Specifies ASCII or binary transfer 1 = ASCII
1*	Load LPW, PLPW, DCW, and BAW Registers	Address of data to be loaded	Specified which LPW Register to be loaded	Not Used
2	Add Logical Channel to BAW and Store	Address of stored result of test command	Used with BAW Register to generate data to be stored	Not Used
3	Increment PLPW and Store	Address of stored result of test command	Not Used	Not Used
4	Store PLPW Register	Address of stored result of test command	Not Used	Not Used
5	Increment DCW Register and Store	Address of stored result of test command	Not Used	Not Used
6	Data Transfer-PLPW to LPW Register	Not Used	Specifies which LPW Register to be loaded	Not Used
7	Logical Channel No. ORed into Test Address; Set Level 2 Interrupt	Not Used	Specify bit to be ORed	Not Used

*Store word in all four registers.

4.2.4.9 PIA Error Summary

The PIA error summary chart follows:

PIA Error Summary Chart

FAULTS	ACTION	FAULT BYTE SENT TO MPC*							
		0	1	2	3	4	5	6	7	Meaning
Data parity error, internal PSIC	Terminate later if data service Terminate now if not data service	1	0	0	1	0	0	0	0	Terminate
Connect while busy (unexpected PCW)	Terminate when LC is active	1	0	0	0	1	0	0	0	
Data parity error, PSI	Terminate later	1	0	1	1	0	0	0	0	
Parity error, IOM to or from PSIC treated as IOM detected fault	---									
Illegal Service Code	Terminate now	0	1	0	0	0	0	0	0	
Parity error during service code sequence	Terminate now	0	1	0	0	0	0	0	0	
Illegal DCW	Terminate now	1	0	0	1	1	0	0	0	Terminate
Service code for not busy or masked logical channel	Terminate now	1	1	0	0	0	0	0	0	Abort
(PSIC is masked for these conditions)										
IOM detected fault	Terminate now	1	1	0	0	0	0	0	0	
Masking PCW	Terminate when LC number is active	1	1	0	0	0	0	0	0	Abort
Tally runout with terminate from MPC	Termination in process	0	0	0	0	0	0	0	0	PSIC tally runout

*Fault Byte - Bits 0 and 1:

00 = Special IOM instruction.
01 = PSA detected illegal SVC or PE (MPC should retry three times).
10 = Status store and terminate cycle should follow.
11 = Logical channel masked, abort (no status and termination cycle).

4.2.4.10 Service Codes - MPC to PIA

The meaning, data bits, and hexadecimal equivalents of the MPC to PIA service codes appear in the following chart.

MPC to PIA Service Codes Chart

MEANING	DATA BITS 0123 4567	HEXADECIMAL
Initiate New Channel Program	0000 0001	1
Move Pointer and Initiate Command Transfer	0000 0010	2
Backup Pointer and Initiate Command Transfer	0000 0011	3
Data Transfer, Read Binary	0000 0100	4
Data Transfer, Read ASCII	0000 0101	5
Data Transfer, Write Binary	0000 0110	6
Data Transfer, Write ASCII	0000 0111	7
Store Special Status	0000 1000	8
Store Terminate Status	0000 1001	9
Set Terminate Interrupt*	0000 1101	D
Set Marker Interrupt*	0000 1110	E
Set Special Interrupt	0000 1111	F

*Refer to subsection 4.2.4.3, Interrupt Multiplex Word.

NOTE

All other codes are illegal.

4.2.4.11 Service Codes - PIA to MPC

The PIA to MPC service codes are:

- Connect = 0010 0000 (one byte PIA to MPC)
- Disconnect = 0001 0000

4.2.4.12 MPC Commands

The description, octal, and hexadecimal equivalents of the MPC commands appear in the following chart.

NOTE

These commands are sent to the MPC in bits 0 through 5 of the IDCW.

OCTAL	HEXADECIMAL	DESCRIPTION
00	00	Request Status
04	04	Read Nonstandard
10	08	Boot C/S
11	09	Boot ITR
16	0E	Write Control Register
17	0F	Format
21	11	Read EDAC
22	12	Read Status Register
23	13	Read ASCII
25	15	Read
26	16	Read Control Register
27	17	Read Header
30	18	Execute DLI
31	19	Write
32	1A	Write ASCII
33	1B	Write and Compare
34	1C	Seek
36	1E	Special Seek
37	1F	Preseek
40	20	Reset Status
42	22	Restore
72	3A	Set Standby
76	3E	Release
77	3F	Reserve

The special controller commands appear in the following chart.

Special Controller Commands

OCTAL	DESCRIPTION
00	Suspend
02	Read Memory ASCII
04	Read Lock
06	Initiate Read
12	Write Memory ASCII
14	Write Lock
16	Initiate Write
20	Release
22	Read Memory Binary
32	Write Memory Binary
34	Conditional Write Lock

4.2.4.13 MPC Device Status

The major status and substatus field of the first status word are listed in the following chart.

MDC Device Status Chart (Sheet 1 of 2)

MAJOR STATUS		SUBSTATUS	
BITS 2 3 4 5	MEANING	BITS 6 7 8 9 10 11	MEANING
0 0 0 0	Ready	0 0 0 0 0 0	No Substatus
		0 0 0 0 X X[a]	Retries
		0 0 1 0 X X[a]	Device in T&D
0 0 0 1	Busy	0 0 0 0 0 0	Positioning
		1 0 0 0 0 0	Alternate Channel
0 0 1 0	Attention	0 0 0 0 0 1	Write Inhibit
		0 0 0 0 1 0	Seek Incomplete
		0 0 1 0 0 0	Device Fault
		0 1 0 0 0 0	Device in Standby
		1 0 0 0 0 0	Device Offline
0 0 1 1	Data Alert	0 0 0 0 0 1	Transfer Timing
		0 0 0 0 1 0	Parity
		0 0 0 1 0 0	Invalid Seek Address
		0 X 1 0 0 0	Header Verification
		X 1 X 0 0 0	Cyclic Check
		1 X 0 0 0 0	Compare Alert
0 1 0 0	End of File	0 0 0 0 0 0	Good Track
		0 0 0 0 X 1	Last Consecutive Block
		0 0 0 0 1 X	Block Count Limit
		0 0 0 1 0 0	Defective Track, Alternate Assignment
		0 0 1 0 0 0	Defective Track, No Alternate
		0 1 0 0 0 0	Alternate Track Detected
0 1 0 1	Instruction Reject	0 0 0 0 0 1	Invalid Op-Code
		0 0 0 0 1 0	Invalid Device Code
		0 0 0 1 0 0	IDCW Parity
		0 0 1 0 0 0	Invalid Instruction Sequence
1 0 1 0	MPC Device Attention	0 0 0 0 0 1	Configuration Error
		0 0 0 0 1 0	Multiple Device
		0 0 0 0 1 1	Device Number Error
		0 0 1 1 0 0	Alert EN-1
		0 0 1 1 0 1	CA EN-1 Error
		0 0 1 1 1 0	CA Alert (No EN-1)

MDC Device Status Chart (Sheet 2 of 2)

MAJOR STATUS		SUBSTATUS	
BITS 2 3 4 5	MEANING	BITS 6 7 8 9 10 11	MEANING
1 0 1 1	MPC Device Data Alert	0 0 0 0 0 1	Transmission Parity
		0 0 0 0 1 0	Inconsistent Command
		0 0 0 0 1 1	Sum Check Error
		0 0 0 1 0 0	Byte Lockout
		0 0 1 1 1 0	EDAC Parity
		0 1 0 0 0 1	Sector Size Error
		0 1 0 0 1 0	Nonstandard Sector Size
		0 1 0 0 1 1	Search Alert (First)
		0 1 0 1 0 0	Cyclic Code (# First)
		0 1 0 1 0 1	Search Alert (# First)
		0 1 0 1 1 0	Sync Byte # Hex 19
		0 1 1 0 1 0	EDAC Correction (# Last Sector)
		0 1 1 0 1 1	EDAC Correction, BCL
		0 1 1 1 0 0	EDAC Uncorrected
1 1 0 1	Command Reject	0 0 0 0 0 1	Illegal Procedure
		0 0 0 0 1 0	Illegal LC Number
		0 0 0 0 1 1	Illegal Suspend
		0 0 0 1 0 0	Continue Bit Not Set

[a] xx = Retry count

The Software Flag (T) and Power (P) bits (bits 0 and 1 of the first status word) are listed in the following chart.

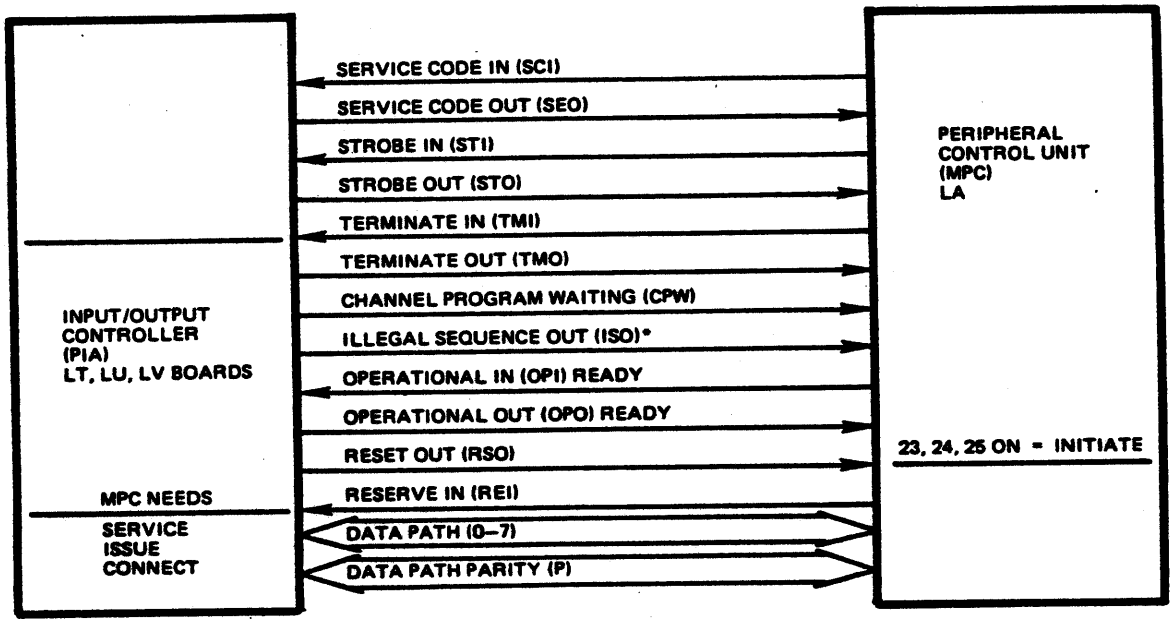
Bit	Meaning
0	Status Stored by MPC Hardware (Reset when status processed by software)
1	MPC Power Off/OPI Down

The IOM channel status (bits 18 through 23 of the first status word) is listed in the following chart.

BITS 18 19 20	MEANING	BITS 21 22 23	MEANING
0 0 1	Connect While Busy	0 0 0	Not Used
0 1 0	PSA Internal PE		
0 1 1	Illegal DCW		
1 1 0	Transmission PE		

4.2.4.14 PIA/MPC Interface Lines

Figure 4-14 shows the PIA/MPC interface signals.



*FORCE DUMMY SERVICE CODE FOLLOWED BY ONE BYTE OF FAULT CODE OR NORMALLY AFTER CPU TO START CONNECT.

DATA MPC → PIA

STI = SEND DATA MPC – PIA
STO = DATA TRANSFER DONE PIA – MPC
TMI = REPLACE STI ON LAST BYTE TRANSFER
STO = STILL RESPONDS TO TMI OR STI

DATA PIA → MPC

STO = DATA TRANSFER PIA – MPC
STI = DATA RECEIVED AT MPC
TMO = REPLACE STO ON LAST TRANSFER
STI = RESPONDS TO TMO OR STO

Figure 4-14 PIA/MPC Interface Lines

4.2.5 Direct Interface Adapter

This subsection contains interrupt vectors, ICWs, and control words for the Direct Interface Adapter (DIA). It also includes HDIA status information, the connect flow chart, and the bootload (72) flow.

IOM Channel Number: The channel number is usually 4.

Interrupt Vectors (Octal):

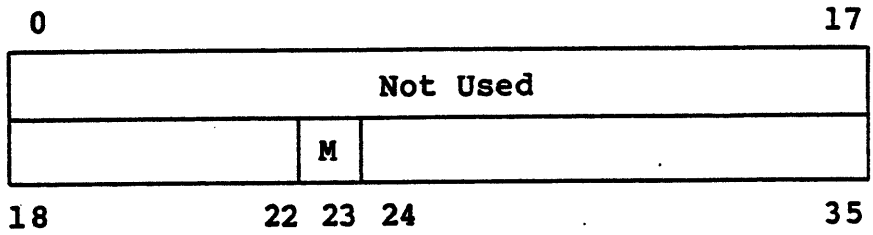
00100 = IOM Detected Fault
00103 = Special
00102 = Terminate

ICWs:

Status = 456, 457
Mailbox = 454, 455

Control Words:

Peripheral Control Word (PCW):



Bit 23 (M) is the Mask bit and must be set to One to mask.

4.2.5.1 HDIA Status - Terminate Status Report

The HDIA status, configuration status report data, and word format are as follows.

HDIA Status Format

The HDIA status format appears as follows:

BIT	EVENT INDICATED
00-14	Must be Zero
15	System Bus Parity
16	Must Be Zero
17	Ready Line: One = Cables, Zero = L66 Not Connected
18-19	Must be Zero
20	Illegal Connect from System
21	Illegal Op-Code from System
22	List ICW Tally Runout
23-26	Zero (Not Used)
27	L66 Test Command While Busy
28	Illegal Op-Code from L66
29	No Answer from L66
30	Zero
31	Parity Error Detected by DIA on L66 IOM
32	IOM or Command Parity Error Detected by L66 IOM
33[a]	Data Parity Error Detected by L66 IOM
34[a]	Bus Parity Error Detected by L66 IOM
35	System Fault Detected by L66 IOM

[a]Status bits 33 and 34 on together indicate an address out of bounds error detected by L66 IOM.

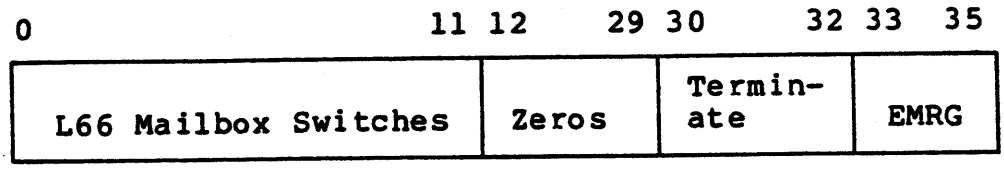
Configuration Status Report (Octal 74)

Four 36-bit words of configuration data are stored.

W16, 17 (L66 Address Bits)

0 0 Zeros

0 1 L66 Mailbox and Interrupt Cell Switches



1 0 Zeros

1 1 Zeros

4.2.5.2 System Connect Flow

Figure 4-15 shows the system connect flow and lists the op-codes:

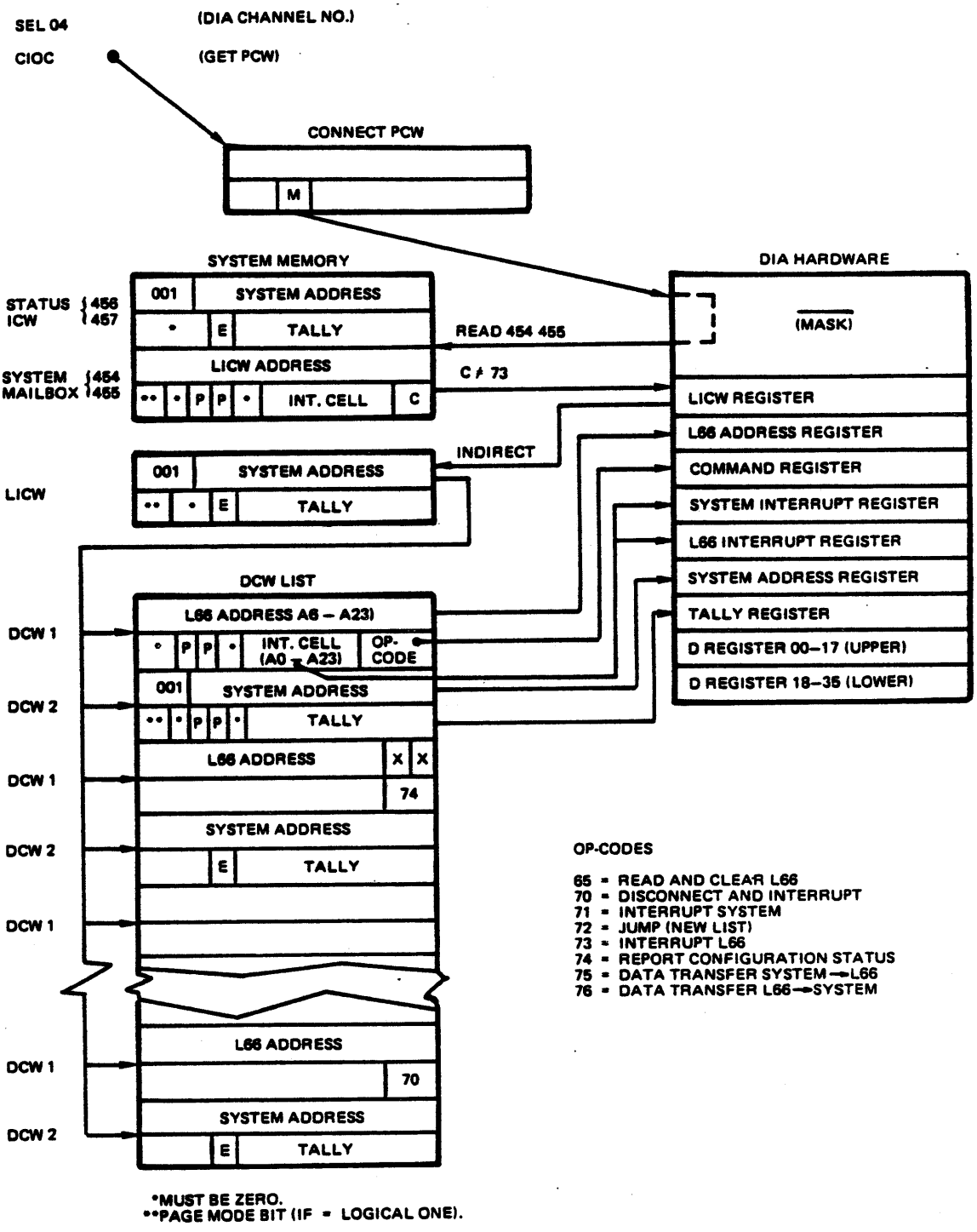


Figure 4-15 System Connect Flow

4.2.5.3 L66 to System for Bootload (72) Flow

Figure 4-16 shows the bootload (72) flow between the system DIA and the L66 DCA.

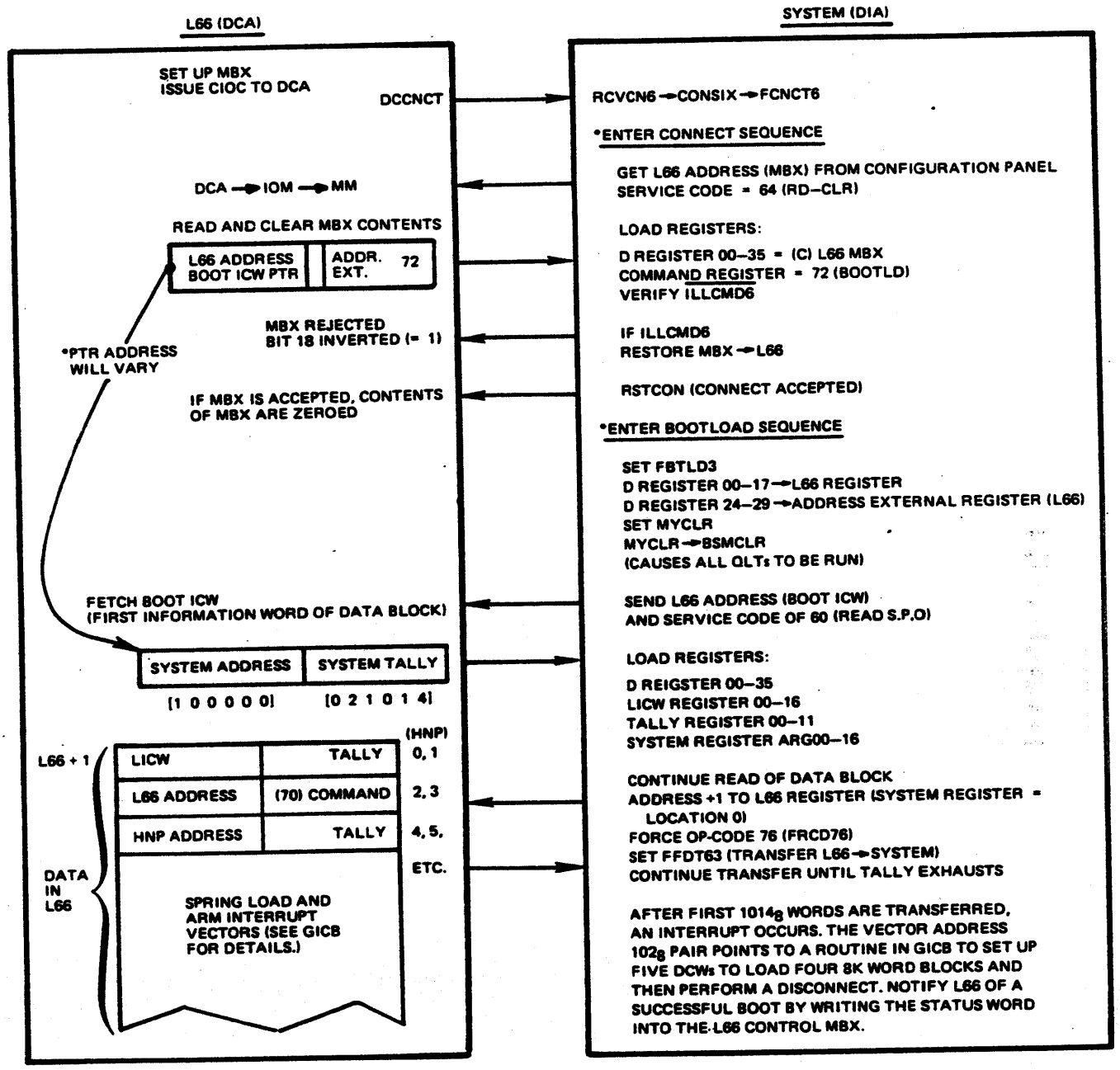


Figure 4-16 L66 DCA to System DIA Bootload (72) Flow

4.2.6 HMLC/CIB

This subsection contains interrupt vectors, status words, CLA identification, PCW formats and active/configuration interrupt vectors for the HMLC/CIB.

IOM Channel Numbers: The channel numbers are 6, 7, and 10.

Interrupt Vectors (Octal):

IOM Detected Channel Fault: 140 (Channel 6), 160 (Channel 7), 200 (channel 10).

Special Interrupt: Not applicable.

Terminal Interrupt: Not applicable.

Interrupts are by subchannel and consist of two types:

- Active
- Configuration.

The active interrupt occurs as a result of a status lead changing on the communications interface or as a result of a PCW 0 or PCW 1 with an op-code of 01 or 02 (Status Request). Either activity causes the active status to be stored in memory and then an interrupt occurs through the active interrupt vector.

The configuration interrupt occurs as a result of a PCW 0 or PCW 1 with an op-code of 03 (Status Request, Configuration). This causes the configuration status to be stored and then an interrupt occurs through the configuration interrupt vector.

Refer to Tables 4-12 through 4-15 for the HMLC/CIB status words, CLA identification, PCW formats, and the active/configuration interrupt vectors.

Table 4-12 HMLC/CIB Status Words

BIT	ACTIVE STATUS	CONFIGURATION STATUS	BSC CONFIGURATION	HDLC CONFIGURATION AND FUNCTION	CODED BAUD RATE (Bits 28–31)
0	0 = Send; 1 = Receive	= 1	= 1	= 1	–
1	Receive Only, Normal Marker Received	0 = Async; 1 = Sync	1 = Sync	1 = Sync	–
2	Receive Only, Delayed Marker Received	2	–	–	–
3	Receive Only, Terminate Character Received	3	–	–	–
4	Alternate Buffer Active	4	–	–	–
5	Buffers will be Switched after Status Store	5	–	–	–
6	TY0 (Tally Zero)	6	–	–	–
7	TY1 (Tally One)	7	–	–	–
8	Receive Only, Lateral Parity Error	8	–	–	–
9	Receive Only, Command to Inactive S/C When MSK	Spare	–	–	–
10	Receive Only, Dataset Status Change	Spare	–	–	–
11	MBZ, Spare	Spare	–	–	–
12	Transfer Timing Error	Check Lateral Receive Parity	–	–	–
13	HDLC, FCS Error	Generate Lateral Send Parity (7 + 1 Codes Only) ASCII	–	–	–
14	MBZ, Spare	1 = Odd; 0 = Even Lateral Parity	–	–	–
15	No Stop Bit Received (Async Only)	0 = One; 1 = Two Send ICWs Used	–	0 = One; 1 = Two Send ICWs Used	–
16	ACU – DLO – Data Line Occupied	Use BAW	–	–	–
17	ACU – PWI – Power On Indicator	Spare (MBZ)	–	–	–
18	Data Set Ready	Spare (MBZ)	–	–	–
19	Clear to Send	Spare (MBZ)	–	–	–
20	Carrier Detect	5-Bit Character Length (Async Only)	–	–	–
21	Supervisor Received	6-Bit Character Length	–	–	–
22	ACU – ACR – Abandon Call and Retry	7-Bit Character Length	–	–	–
23	Data Set Status Lead Up – ACU	8-Bit Character Length	–	–	–
24	Ring Indicator – Call	Two Stop Bits (Async Only)	1 = CRC 16 Polynomial 0 = CCITT Polynomial	–	–
25	Line Break Received – Complete	Spare	–	Idle Detect	–
26	HDLC/BSC Terminate Character Received	Spare	–	Buffer Switch Enabled	
27	Receive Mode	Spare	1 = EBCDIC Code 0 = ASCII Code	1 = Transmit Flag Byte If Idle 0 = Transmit Marks If Idle	
28	Send Mode	110 (Async Bit Rates) Or Bit 8	1 = Transparency 0 = Nontransparency	Extended Control Field One Byte	
29	Wraparound Mode	134.5 (Async Bit Rates) Or Bit 7	Timer Enable	Extended Address Mode (Zero = CLA Assumes Only One Address Field Byte)	
30	Data Terminal Ready	150 (Async Bit Rates) Or Bit 6	–		
31	Request To Send	300 (Async Bit Rates) Or Bit 5 (Sync)	–		
32	Make Busy	1050 (Async Bit Rates) Or Bit 4	–		
33	Supervisory Transmit/BSC – CRC Error	1200 (Async Bit Rates) Or Bit 3 (Char)	–		
34	Call Request (ACU)	1800 (Async Bit Rates) Or Bit 2			
35	Spare	See Note (Async Bit Rates) Or Bit 1			

SEND BYTE SIZE

30	31	32	SEND BYTE SIZE FIELD
1	0	1	5 bits per byte
1	1	0	6 bits per byte
1	1	1	7 bits per byte
0	0	0	8 bits per byte

RECEIVE BYTE

33	34	35	RECEIVE BYTE SIZE FIELD
1	0	1	5 bits per byte
1	1	0	6 bits per byte
1	1	1	7 bits per byte
0	0	0	8 bits per byte

BIT 35 = 1 PCW 2 AND CONFIGURATION STATUS

28	29	30	31	BAUD RATE
0	0	0	0	50*
0	0	0	1	75
0	0	1	0	110
0	0	1	1	134.5*
0	1	0	0	150*
0	1	0	1	200*
0	1	1	0	300*
0	1	1	1	600*
1	0	0	0	1050
1	0	0	1	1200*
1	0	1	0	1800
1	0	1	1	2000
1	1	0	0	2400
1	1	0	1	4800
1	1	1	0	9600
1	1	1	1	Not Specified

*Considered European Baud Rate

NOTE: If bit 35 = 1, then bits 32 through 40 = 0 and bits 28 through 31 are decoded in the last column of this table.

Table 4-13 CLA Identification

TYPE CLA	BOARD NUMBER	CLA ID HEX (OCTAL)	CLA DESCRIPTION	BITS 2-5 OF CONFIGURATION STATUS WORD (OCTAL)	
				WITHOUT ACU	WITH ACU
DCF6615	BD2A88	0 (0)	MIL-STD-188C Async Line Adapter	40	60
		1 (1)	Not used		
DCF6610	BD2CLA	2 (2)	Dual Async Current Loop Adapter	42	62
DCF6612	BD2ASC	3 (3)	Dual Async Line Adapter	43	63
DCF6613	BD2DAC	4 (4)	Dual Autocall Unit Adapter	-	64
		5 (5)	Not used	-	-
DCF6621	BD2CMS	6 (6)	Bisync Current Mode Broadband Adapter	46	66
DCF6619	BD2CMS	7 (7)	Sync Current Mode Broadband Adapter	47	67
DCF6620	BD2DLC	8 (10)	HDLC Adapter	50	70
DCF6616	BD2B88	9 (11)	MIL-STD-188C Broadband Adapter	51	71
DCF6618	BD2LAS	A (12)	Dual Bisync Line Adapter	52	72
DCF6611	BD2LAS	B (13)	Dual Sync Line Adapter	53	73
DCF6614	BD218P	C (14)	MIL-STD-188C Sync Line Adapter	54	74
DCF6627	BD2BLS	D (15)	Sync Balanced Line Broadband Adapter	55	75
DCF6617	BD2H88	E (16)	MIL-STD-188C HDLC Adapter	56	76
DCF6622	BH4DLD	F6 (366)	Broadband HDLC Current Mode Adapter	146	166
DCF6623	BH4DLE	F7 (367)	Broadband HDLC Balanced Line Adapter	147	167

Table 4-14 HMLC PCW Formats

PCW BITS	PCW 0 ACTIVE	PCW 1 ACTIVE BROADSIDE	PCW 2 CONFIGURATION (ASYNC)	PCW 3 CONFIGURATION (SYNC)	PCW 3 BSC (SYNC)
0, 1	00	01	10	11	11
2-5	Active Command (Octal): 00 = No Command (Used with PCW 1 Broadside) 01 = Status Request – S/C Receive 02 = Status Request – S/C Send 03 = Status Request – S/C Configuration 04 = S/C Mask Bit – Set 05 = S/C Mask Bit – Reset 06 = Switch S/C Data Buffer – Receive 07 = Switch S/C Data Buffer – Send 10 = Initialize HMLC 11 = Store Mask Register 14 = Resynchronize 15 = Transmit Line Break (600 msec) Others = Not Used (0 or 1)		Configuration Command (Octal): 14 = 5-Bit Character (Async) 15 = 6-Bit Character 16 = 7-Bit Character 17 = 8-Bit Character Others = Not Used	Configuration Command (Octal): Bits 2 through 5 MBZ on the HDLC	Character length is ignored by BSC **NOTE** The subchannel is hardwired for 8 bits per character.
6	Not Used by HMLC			(2 or 3)	
7-11	Subchannel Number		(00 – 31)		–
12	Not Used		LPR (Latitudinal Parity Receive)	Bits 12 through 14 MBZ on the HDLC	LPR
13	Not Used		LPS (Latitudinal Parity Send)		LPS
14	Not Used		LPO (Latitudinal Parity Odd)		LPO
15	Not Used		ACW (Alternate Control Word) (Two Send ICWs)	Not Used	ACW
16	Buffer Switch Enable (HDLC Only)	Not Used	TFE (Table Function Enable) CCT (Enable)	Bits 16 through 22 MBZ on the HDLC	TFE – CCC
17	Send TR0 Enable (HDLC Only)	Not Used	Spare		Spare
18	Not Used	Not Used	Not Used		Not Used
19	Not Used	Not Used	Not Used		Not Used
20	Not Used	Not Used	Not Used		
21	Not Used	Not Used			
22	Not Used	Not Used			
23	Initialize (Mask Subchannels)				
24	Not Used	Not Used	Two Stop Bits If = 1	MBZ on HDLC	If = One, CRC-16 Polynomial If = Zero, CCITT Polynomial
25	Not Used	Not Used	Not Used	Idle Enable – One = If Idle State Entered During Frame (HDLC Only)	–
26	Not Used	Not Used	Not Used	Buffer Switch Enable (HDLC Only)	–
27	Not Used	Set Receive Mode	Not Used	Transmit Fill – One = Transmit Fills When Idle (HDLC Only)	If = One, EBCDIC Code If = Zero, ASCII
28	Not Used	Set Send Mode	110 Baud	Extended Control Field (HDLC Only)	If = One, Transparent Data If = Zero, Nontransparent Data
29	Not Used	Set Wraparound Mode	134.5 Baud	Extended Address Field (HDLC Only)	If = One, Timer Enabled
30	Not Used	Set Data Terminal Ready	150 Baud	Bits 30–32 Send Byte Size* (HDLC Only)	
31	Not Used	Set Request to Send	300 Baud		
32	Not Used	Send Logic Bypass (BSC Only)	1080 Baud		–
33	Not Used	Set Supervisor Send	1200 Baud	Bits 33–35 Receive Byte Size** (HDLC Only)	
34	Not Used	Set Call Request	1800 Baud		
35	Not Used	Receive Logic Bypass (BSC Only)	Coded Bit Gate Selected***		

*Byte Size Decode

BIT 30	BIT 31	BIT 32	SEND BYTE SIZE
1	0	1	5 Bits/Byte
1	1	0	6 Bits/Byte
1	1	1	7 Bits/Byte
0	0	0	8 Bits/Byte
0	1	0	Size in Text Control Byte (TCB)

**Byte Size Decode

BIT 33	BIT 34	BIT 35	RECEIVE BYTE SIZE
1	0	1	5 Bits/Byte
1	1	0	6 Bits /Byte
1	1	1	7 Bits/Byte
0	0	0	8 Bits/Byte
0	1	0	Size in Text Control Byte (TCB)

***Coded Baud Rates

BIT PCW 2 28	29	30	31	BAUD RATE
0	0	0	0	50
0	0	0	1	75
0	0	1	0	110
0	0	1	1	134.5
0	1	0	0	150
0	1	0	1	200
0	1	1	0	300
0	1	1	1	600
1	0	0	0	1050
1	0	0	1	1200
1	0	1	0	1800
1	0	1	1	2000
1	1	0	0	2400
1	1	0	1	4800
1	1	1	0	9600

Table 4-15 HMLC Subchannel Control Word Memory Map

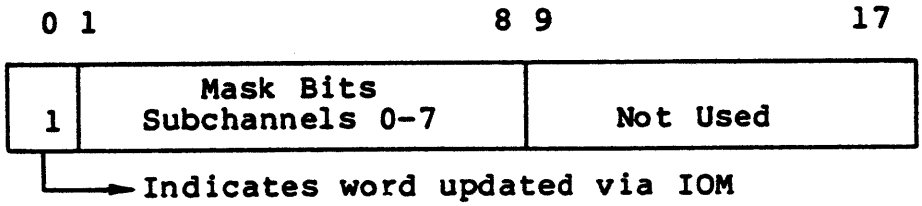
ICW ADDRESS	SUBCHANNEL NUMBER		CHANNEL 6 INTERRUPT VECTOR LOCATION		CHANNEL 7 INTERRUPT VECTOR LOCATION		CHANNEL 10 INTERRUPT VECTOR LOCATION	
(Octal)	(Decimal)	(Octal)	(Active)	(Configuration)	(Active)	(Configuration)	(Active)	(Configuration)
01000-01017	0	1	00004	00006	10	0012	0014	0016
01020-01037	1	1	00024	00026	30	0032	0034	0036
01040-01057	2	2	00044	00046	50	0052	0054	0056
01060-01077	3	3	00064	00066	70	0072	0074	0076
01100-01117	4	4	00104	00106	110	0112	0114	0116
01120-01137	5	5	00124	00126	130	0132	0134	0136
01140-01157	6	6	00144	00146	150	0152	0154	0156
01160-01177	7	7	00164	00166	170	0172	0174	0176
01200-01217	8	10	00204	00206	210	0212	0214	0216
01220-01237	9	11	00224	00226	230	0232	0234	0236
01240-01257	10	12	00244	00246	250	0252	0254	0256
01260-01277	11	13	00264	00266	270	0272	0274	0276
01300-01317	12	14	00304	00306	310	0312	0314	0316
01320-01337	13	15	00324	00326	330	0332	0334	0336
01340-01357	14	16	00344	00346	350	0352	0354	0356
01360-01377	15	17	00364	00366	370	0372	0374	0376
01400-01417	16	20	00005	00007	11	0013	0015	0017
01420-01437	17	21	00025	00027	31	0033	0035	0037
01440-01457	18	22	00045	00047	51	0053	0055	0057
01460-01477	19	23	00065	00067	71	0073	0075	0077
01500-01517	20	24	00105	00107	111	0113	0115	0117
01520-01537	21	25	00125	00127	131	0133	0135	0137
01540-01557	22	26	00145	00147	151	0153	0155	0157
01560-01577	23	27	00165	00167	171	0173	0175	0177
01600-01617	24	30	00205	00207	211	0213	0215	0217
01620-01637	25	31	00225	00227	231	0233	0235	0237
01640-01657	26	32	00245	00247	251	0253	0255	0257
01660-01677	27	33	00265	00267	271	0273	0275	0277
01700-01717	28	34	00305	00307	311	0313	0315	0317
01720-01737	29	35	00325	00327	331	0333	0335	0337
01740-01757	30	36	00345	00347	351	0353	0355	0357
01760-01777	31	37	00365	00367	371	0373	0375	0377

4.2.6.1 HMLC Subchannel Control Words

The HMLC subchannel control word data follows (also refer to Figure 4-17, next page).

RELATIVE ADDRESS (MODULO 20 OCTAL PER SUBCHANNEL)	FUNCTION
0-1	ICW Active - Receive No. 1
2-3	ICW Active - Receive No. 2 (Alternate)
4-5	ICW Active - Send No. 1
6-7	ICW Active - Send No. 2 (Alternate)
10-11	BAW (10) and Spare (11)
12-13	Mask Register (stored direct - 36)
14-16	ICW Active - Status (stored indirect - 36)
16-17	Configuration Status (stored direct - 36)

The Mask Status Word format follows:



NOTE

The subchannel mask status is stored into the first CLA communications region of each HMLC (if a One = Masked Off).

CHANNEL NUMBER	HMLC NO.	MEMORY LOCATION
06	0	1012
06	1	1212
06	2	1412
06	3	1612
07	0	2012
07	1	2212
07	2	2412
07	3	2612
10	0	3012
10	1	3212
10	2	3412
10	3	3612

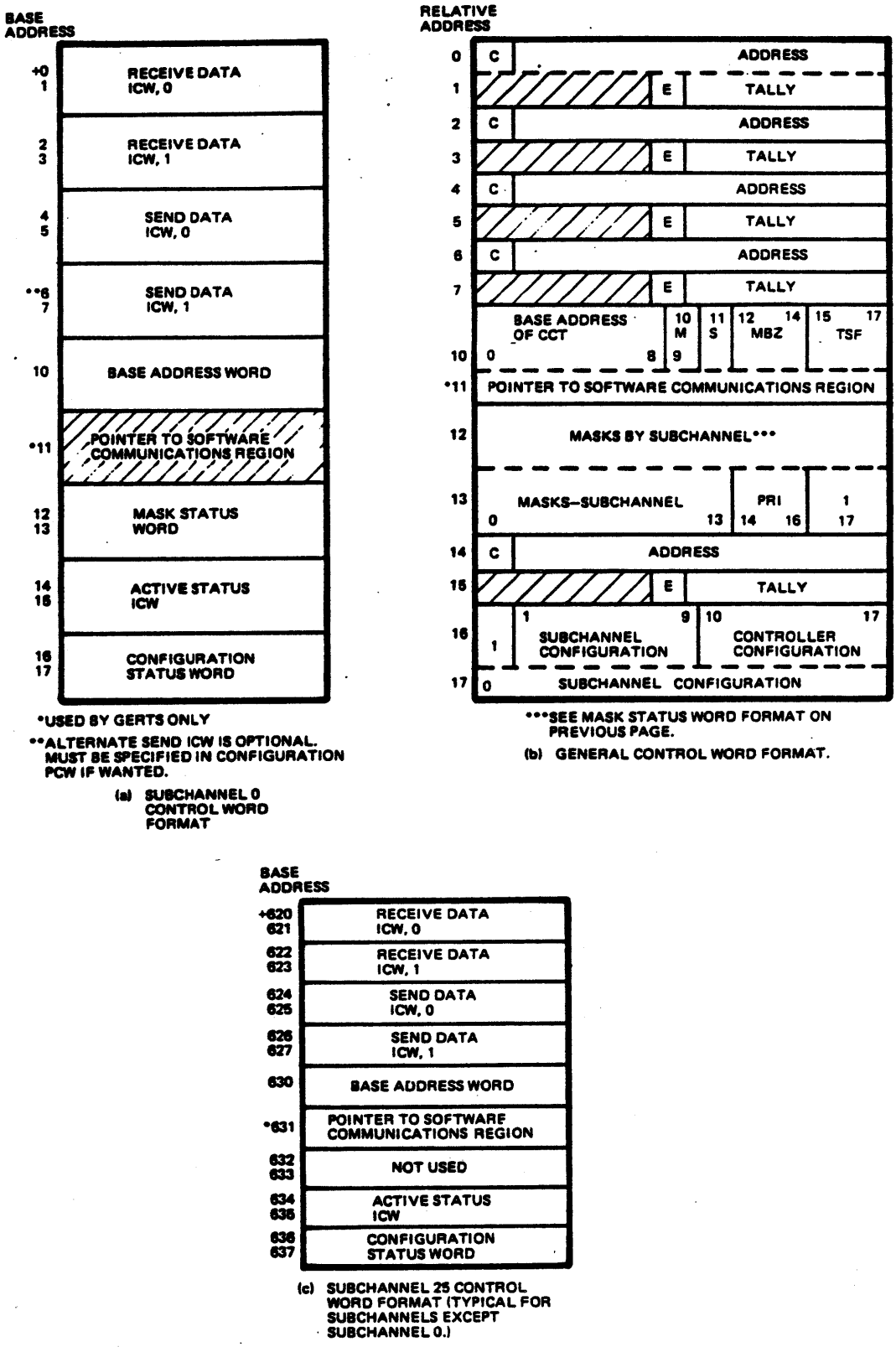


Figure 4-17 HMLC Subchannel Control Word Data

4.2.6.2 Character Control - General Information

Figure 4-18 shows the CCW function data flow.

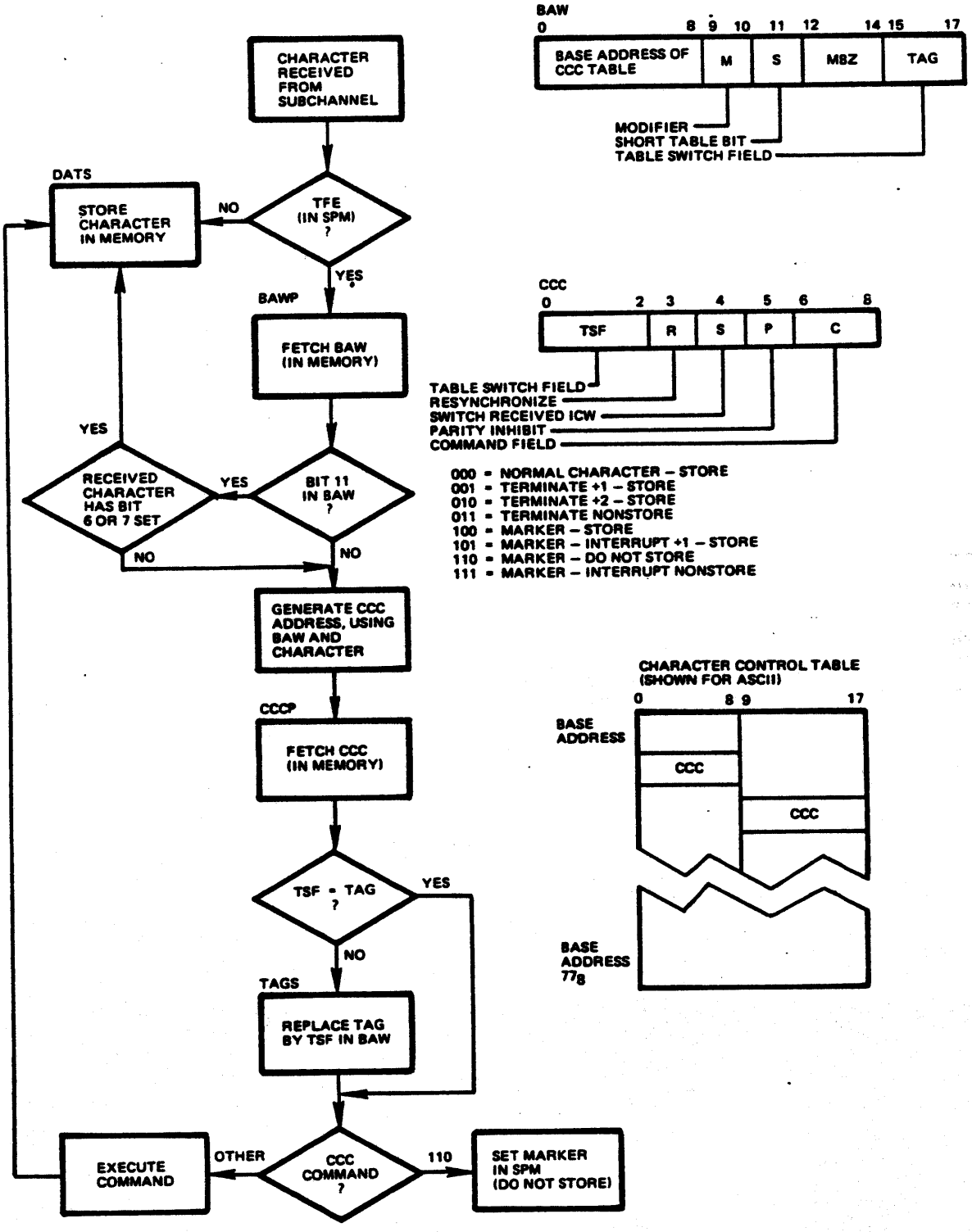


Figure 4-18 CCW Function Data Flow

FN01

4.2.6.3 Fault Conditions and HMLC Responses

The system fault conditions and the appropriate HMLC responses appear in the following chart.

FAULT	RESPONSE
An instruction other than a CIOC or an STEX is received (no parity errors).	The instruction is ignored.
A bus parity error (data left, right, or address) or Red occurs when an instruction (any) is received.	The HMLC that is addressed performs a fault status transfer to the IOM. The other three HMLCs ignore the instructions even if a PCW (CIOC) with bit 23 (set mask/initialize) set. A timeout occurs if an unimplemented HMLC is addressed.
An NAK is received when the HMLC performs an STEX response.	A fault status transfer and interrupt occurs (continue normal operation).
The first (or only) cycle of an HMLC initiated operation (direct load of BAW on CCC; direct store of BAW on configuration status; indirect store of data or active status) is NAKed.	The HMLC masks (initializes) the subchannel (continue normal operation).
The second (response) cycle of an HMLC initiated operation (direct load of a BAW or CCC; indirect load of data; indirect store of active status or data) has a parity error (Red or Yellow ?) or fault status.	The HMLC masks (initializes) the subchannel. A fault status transfer and interrupt is made (continue normal operation on the other subchannels). NOTE The fault status word must specify which parity error (Red or Yellow), an improper NAK, etc.
An NAK was received in response to a fault status report.	Set up a new status word (include previous status) and retry. Note that this may result in a loop.

4.2.7 Timer Channel - General Information

This subsection contains interrupt vectors, PCWs, and mailbox information for the timer channel.

IOM Channel Number (Octal): The channel number is 17.

CIOC to Channel 77: Interrupt Timer.

Interrupt Vectors (Octal):

IOM Detected Channel Fault = 360
Interval Timer Runout = 361
Elapsed Timer Rollover = 362

Peripheral Control Word:

The PCW affects only the interval timer. When the mask bit is set to One, turn the interval timer OFF.

Mailboxes (Octal):

Interval Timer = 450
Elapsed Timer = 451

Status: None reported.

4.2.8 Wraparound Channel T&D Testing

This subsection contains the channel number data, word format, and the indicator register format for the Wraparound Channel (WAC).

CHANNEL NO.	DEFINITION
70	Command Register
71	Address Register
72	Data Lower Register
73	Data Upper Register
74	Connect Sequence
75	Indicator Register
76	Program Aid Register (355 AB1 only)

LDEX can be made only to:

- Channel 70
- Channel 71
- Channel 72
- Channel 73
- Channel 76.

Connect can be made only to Channel 74.

STEX can be made only to:

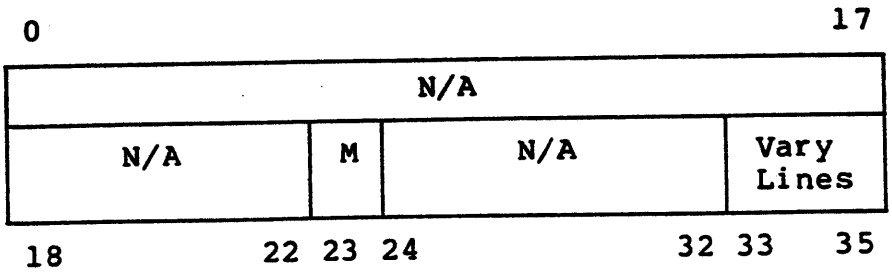
- Channel 72
- Channel 73
- Channel 75
- Channel 70
- Channel 76.

Vary Request Lines:

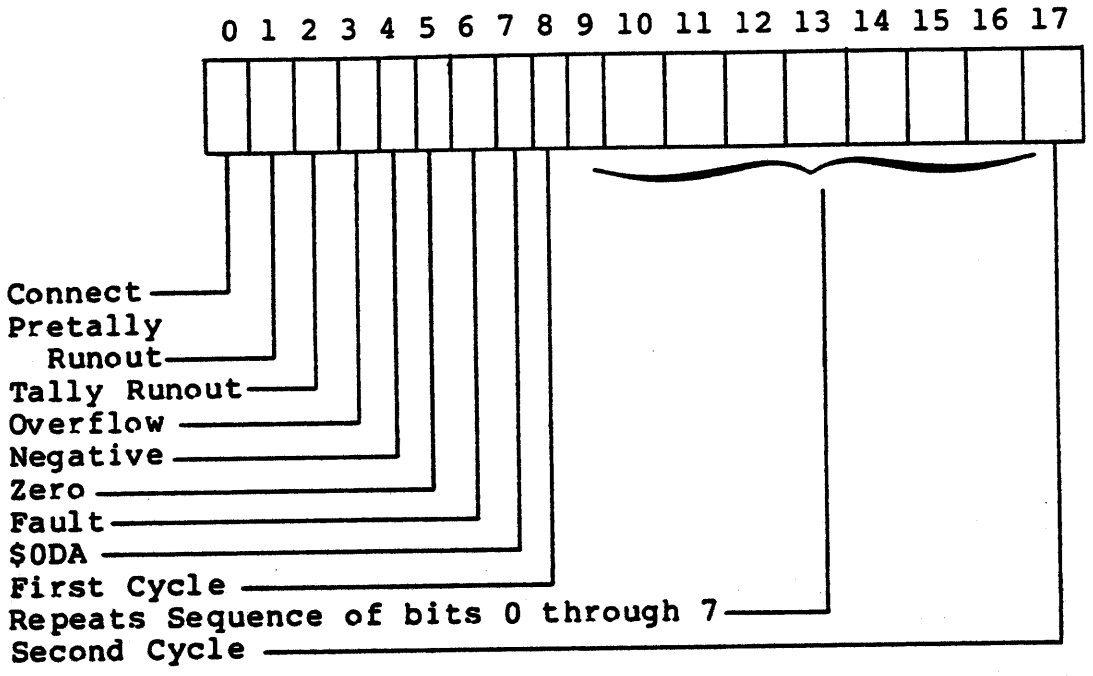
PCW Bits

33	34	35	
0	0	0	One = Request
0	0	1	One = Request, short delay, second request
0	1	0	One = Request, long delay, second request
1	0	0	One = Request, long delay, second request

PCW Format:



WAC Indicator Register Format:



4.2.9 Processor Word Formats and Instruction Information

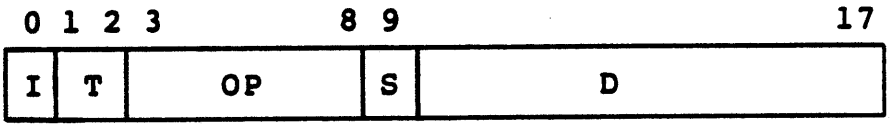
This subsection contains word formats and instruction information for the processor. This information includes:

- Instructions
- Processor Instruction Set
- Processor Instructions - Numerical Order
- Processor Instructions by Function
- Character Address Addition (see Table 4-16)
- Processor Indicator Register
- Processor Index Register
- Indirect Words
- Instruction Counter
- Operands.

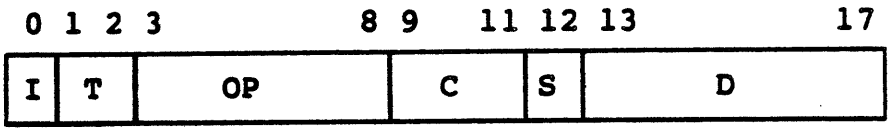
4.2.9.1 Instructions

The processor instruction formats are:

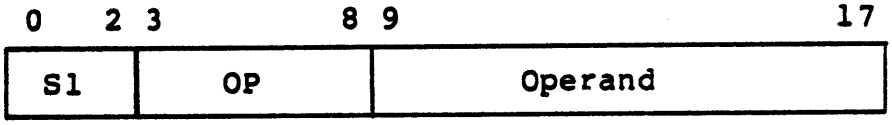
Memory Reference, Word Addressing:



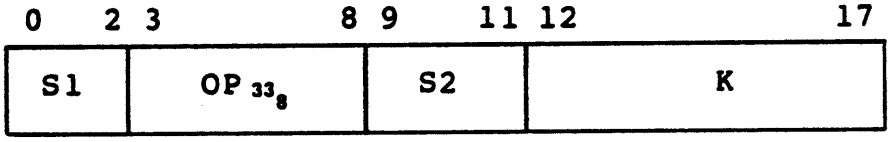
Memory Reference, Character Addressing:



Nonmemory Reference Group 1:



Nonmemory Reference Group 2:



OP = 6-Bit Operation Code
T = Modification - Bits 1 and 2
00 = IC 02 = X2
01 = X1 03 = X3
I = Indirect bit
K = Operand (for shift counts, ect.)
S1 = Suboperation Field 1
S2 = Suboperation Field 2
D = Displacement Field ($-256 \leq D \leq +255$)
S = Sign Bit

4.2.9.2 Processor Instruction Set

The processor instruction set appears in the following chart.

Processor Instruction Set (Sheet 1 of 2)

OP-CODE	MEMORY REFERENCE INSTRUCTIONS	
07	LDA	Load A
47	LDQ	Load Q
04	LDAQ	Load AQ
43, 03, 41	LDXN	Load XN = 1, 2, 3
44	LDI	Load Index Register
17	STA	Store A
57	STQ	Store Q
14	STAQ	Store AQ
53, 13, 50	STXN	Store XN = 1, 2, 3
54	STI	Store Index Register
56	STZ	Store Zeros
06	ADA	Add to A
46	ADQ	Add to Q
15	ADAQ	Add to AQ
42, 02, 40	ADCXN	Add Character Address to XN
16	ASA	Add Stored to A
76	AOS	Add One to Storage
26	SBA	Subtract from A
66	SBQ	Subtract from Q
24	SBAQ	Subtract from AQ
36	SSA	Subtract Stored from A
01	MPF	Multiply Fraction
21	DVF	Divide Fraction
34	ANA	And to A
32	ANSA	And to Storage A
37	ORA	OR to A
72	ORSA	OR to Storage A
35	ERA	Exclusive OR to A
62	ERSA	Exclusive OR to Storage A
27	CMPA	Compare with A
67	CMPQ	Compare with Q
63, 23, 61	CMPXN	Compare with XN
20	SZN	Set Zero & Negative Indicator from Memory
31	CANA	Comparative And with A
71	TRA	Transfer Unconditionally
10	TSY	Transfer And Store in Y
74	TZE	Transfer on Zero
64	TNZ	Transfer on Not Zero
75	TMI	Transfer on Minus
65	TPL	Transfer on Plus
45	TNC	Transfer on No Carry
55	TOV	Transfer on Overflow
60	CIOC	Connect I/O Channel
30	LDEX	Load External
70	STEX	Store External

Processor Instruction Set (Sheet 2 of 2)

OP-CODE	GROUP 1: NONMEMORY REFERENCE INSTRUCTIONS	
773	IAA	Immediate Add to A
573	IAQ	Immediate Add to Q
173, 273, 373	IACXN	Immediate Add Character Address to XN
673	ILA	Immediate Load A
473	ILQ	Immediate Load Q
073	SEL	Select I/O Channel
012	RIER	Read/Interrupt Enable Register
412	RIA	Read/Interrupt Address
052	SIER	Set Interrupt Enable Register
452	SIC	Set Interrupt Cell
022	IANA	Immediate And to A
122	IORA	Immediate OR to A
322	IERA	Immediate Exclusive OR to A
422	ICMPA	Immediate Compare A
222	ICANA	Immediate Comparative And with A

OP-CODE	GROUP 2: NONMEMORY REFERENCE INSTRUCTIONS	
7333	CQA	Copy Q Register into A Register
6333	CAQ	Copy A Register into Q Register
4332, 0332		
4333	CAXN	Copy A Register into XN Register
2332, 3332		
3333	CXNA	Copy XN Register into A Register
3331	INH	Interrupt Inhibit Mode On
7331	ENI	Enable Interrupt Mode
4331	DIS	Delay Until Interrupt
2331	NOP	No Operation
0337	ARS	A Right Shift
4337	QRS	Q Right Shift
0335	LRS	Long Right Shift
0336	ALS	A Left Shift
4336	QLS	Q Left Shift
0334	LLS	Long Left Shift
2337	ARL	A Right Logical
6337	QRL	Q Right Logical
2335	LRL	Long Right Logical
2336	ALR	A Left Rotate
3336	ALP	A Left Parity Rotate
6336	QLR	Q Left Rotate
7336	QLP	Q Left Parity Rotate
2334	LLR	Long Left Rotate
1336	NRM	Normalize
1334	NRML	Normalize Long

4.2.9.3 Processor Instruction Set - Numerical Order

The numerical order listing for the instruction set follows:

00	-	26	SBA	54	STI
01	MPF	27	CMPA	55	TOV
02	ADCX2	30	LDEX	56	STZ
03	LDX2	31	CANA	57	STQ
04	LDAQ	32	ANSA	60	CIOC
05	-	33	(Group 2)	61	CMPX3
06	ADA	34	ANA	62	ERSA
07	LDA	35	ERA	63	CMPX1
10	TSY	36	SSA	64	TNZ
11	-	37	ORA	65	TPL
12	(Group 3)	40	ADCX3	66	SBQ
13	STX2	41	LDX3	67	CMPQ
14	STAQ	42	ADCX1	70	STEX
15	ADAQ	43	LDX1	71	TRA
16	ASA	44	LDI	72	ORSA
17	STA	45	TNC	73	(Group 1)
20	SZN	46	ADQ	74	TZE
21	DVF	47	LDQ	75	TMI
22	(Group 5)	50	STX3	76	AOS
23	CMPX2	51	-	77	-
24	SBAQ	52	(Group 4)		
25	-	53	STX1		

Group 1:

073	SEL
173	IACX1
273	IACX2
373	IACX3
473	ILQ
573	IAQ
673	ILA
773	IAA

Group 2:

0330	-
0331	-
0332	CAX2
0333	-
0334	LLS
0335	LRS
0336	ALS
0337	ARS
1330	-
1331	-
1332	-

Group 2:

1333	-
1334	NRML
1335	-
1336	NRM
1337	-
2330	-
2331	NOP
2332	CX1A
2333	-
2334	LLR
2335	LRL

Group 2:

2336	ALR
2337	ARL
3330	-
3331	INH
3332	CX2A
3333	CX3A
3334	-
3335	-
3336	ALP
3337	-

Group 2:

4331	DIS
4333	CAX3
4336	QLS
4337	QRS
6333	CAQ
6336	QLR
6337	QRL
7331	ENI
7333	CQA
7336	QLP

Group 3:

012	RIER
112	-
212	-
312	-
412	RIA
512	-
612	-
712	-

Group 4:

052	SIER
152	-
252	-
352	-
452	SIC
552	-
652	-
752	-

Group 5:

022	IANA
122	IORA
222	ICANA
322	IERA
422	ICMPA
522	-
622	-
722	-

4.2.9.4 Processor Instructions by Function

The processor instructions listed by function are as follows:

LOADS

LDA	07
LDQ	47
LDAQ	04
LDX1	43
LDX2	03
LDX3	41
LDI	44
SZN	20

STORES

STA	17
STQ	57
STAQ	14
STX1	53
STX2	13
STX3	50
STI	54
STZ	56

TRANSFERS

TRA	71
TSY	10
TZE	74
TNZ	64
TMI	75
TPL	65
TNC	45
TOV	55

COMPARES

CMPA	27
CMPQ	67
CMPX1	63
CMPX2	23
CMPX3	61
CANA	31

ADDS

ADA	06
ADQ	46
ADAQ	15
ADCX1	42
ADCX2	02
ADCX3	40
ASA	16
AOS	76

SUBTRACTS

SBA	26
SBQ	66
SBAQ	24
SSA	36

MULTIPLIES & DIVIDES

MPF	01
DVF	21

BOOLEAN

ANA	34
ANSA	32
ORA	37
ORSA	72
ERA	35
ERSA	62

IMMEDIATES

IAA	773
ILA	673
IAQ	573
ILQ	473
IACX1	173
IACX2	273
IACX3	373
IANA	022
IORA	122
IERA	322
ICMPA	422
ICANA	222

COPIES

CAQ	6333
CQA	7333
CAX1	4332
CAX2	0332
CAX3	4333
CX1A	2332
CX2A	3332
CX3A	3333

SHIFTS

ARS	0337
QRS	4337
ALS	0336
QLS	4336
LRS	0335
LLS	0334
ARL	2337
QRL	6337
LRL	2335
ALR	2336
QLR	6336
ALP	3336
QLP	7336
LLR	2334
NRM	1336
NRML	1334

INPUT/OUTPUT

SEL	073
CIOC	60
LDEX	30
STEX	70

INTERRUPT CONTROL

INH	3331
ENI	7331
SIER	052
RIER	012
SIC	452
RIA	412
DIS	4331

MISC.

NOP	2331

4.2.9.5 Character Address Addition

Figure 4-19 illustrates character address addition.

X REGISTER C FIELD		WORD	DOUBLE WORD	0/2 BYTE	1/2 BYTE	0/3 BCD	1/3 BCD	2/3 BCD	ILLEGAL
FRACTIONAL	OCTAL	0	1	2	3	4	5	6	7
WORD	0	0	7	7	7	7	7	7	7
DOUBLE WORD	1	7	7	7	7	7	7	7	7
0/2	2	7	7	0/2	1/2	7	7	7	7
1/2	3	7	7	1/2	0/2 *	7	7	7	7
0/3	4	7	7	7	7	0/3	1/3	2/3	7
1/3	5	7	7	7	7	1/3	2/3	0/3 *	7
2/3	6	7	7	7	7	2/3	0/3 *	1/3 *	7
ILLEGAL	7	7	7	7	7	7	7	7	7

*+CARRY – INCREMENTS THE ADDRESS DISPLACEMENT FIELD OF THE ORIGINAL WORD.

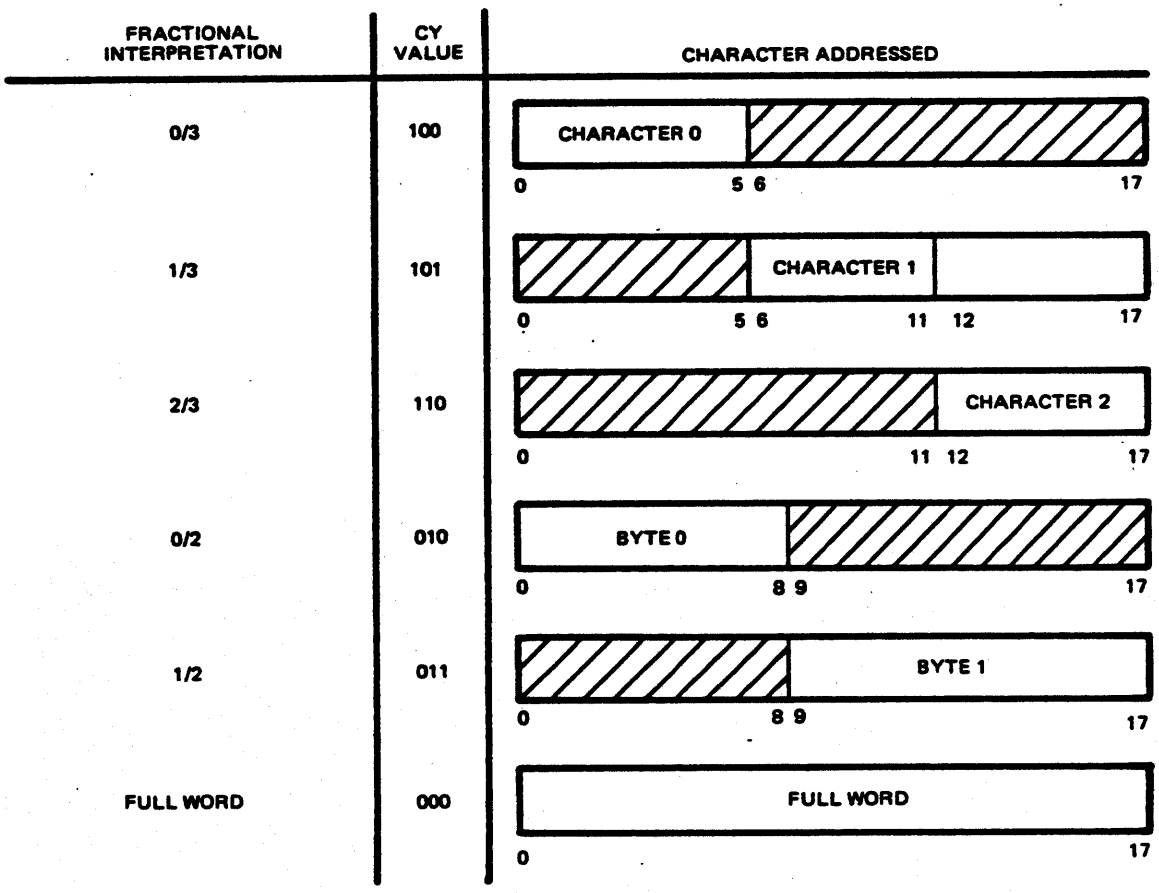
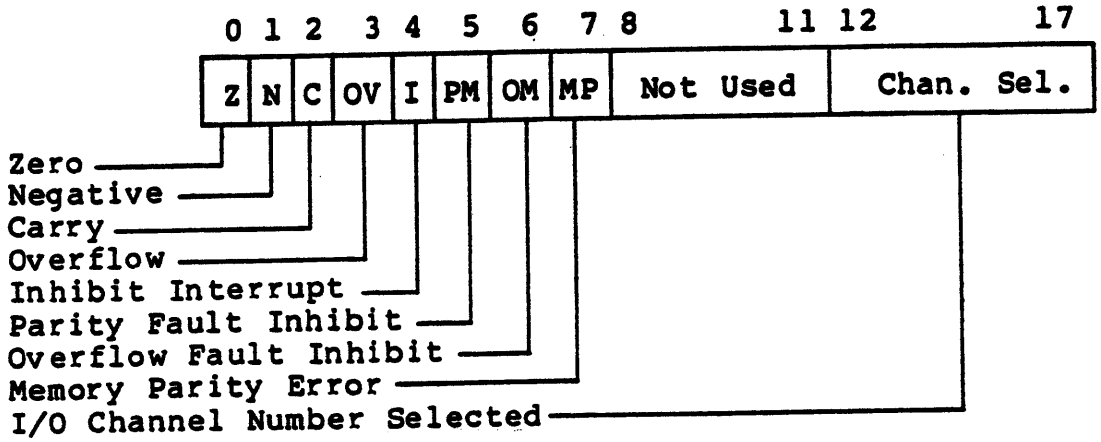


Figure 4-19 Character Address Addition

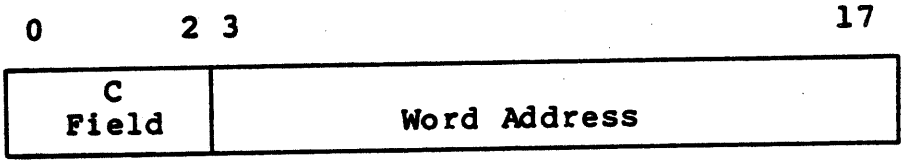
4.2.9.6 Processor Indicator Register

The processor indicator register word format follows:



4.2.9.7 Processor Index Register

The processor index register word format follows:



If X register modification is specified (i.e., the T field of the instruction word equals 1, 2, or 3), then the legal values of the X register C field are:

0 = Single precision word
1 = Double precision word
2 = Byte 0, bits 0 through 8
3 = Byte 1, bits 9 through 17
4 = Character 0, bits 0 through 5
5 = Character 1, bits 6 through 11
6 = Character 2, bits 12 through 17

If the C field equals 7, an IM fault occurs. If the X register C field equals byte or character addressing, then the field of the original word must also specify the same type of addressing or an IM fault will occur, for example:

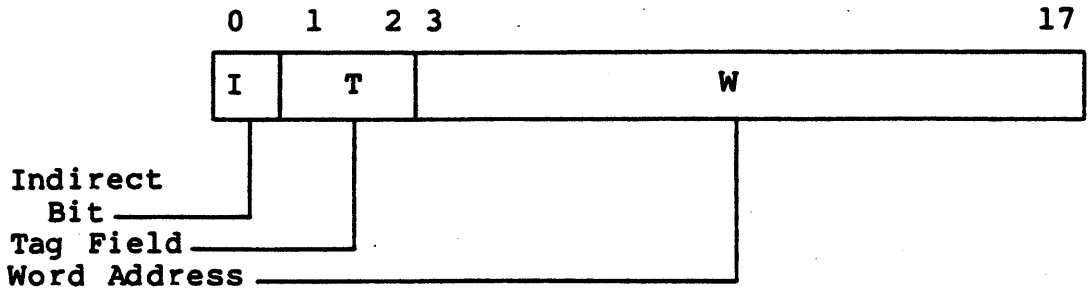
X Register C Field		Instruction Cy Field
2 or 3 byte	=	2 or 3
4,5, or 6 character	=	4, 5, or 6

Refer to subsection 4.2.9.5 to determine the results of byte/character addressing.

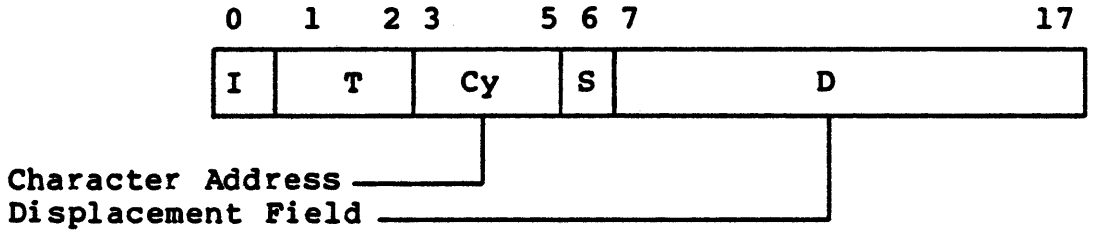
4.2.9.8 Indirect Words

The indirect word addressing and character addressing word formats follow:

Word Addressing:

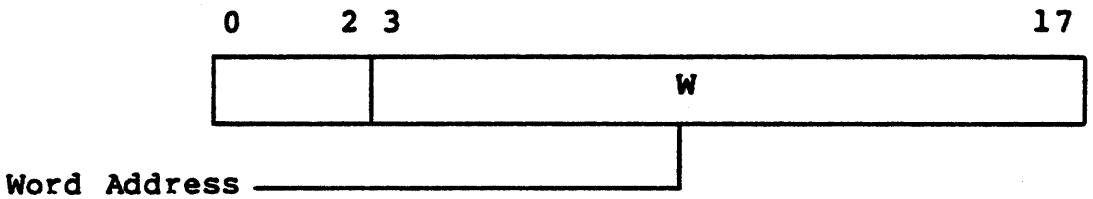


Character Addressing:



4.2.9.9 Instruction Counter

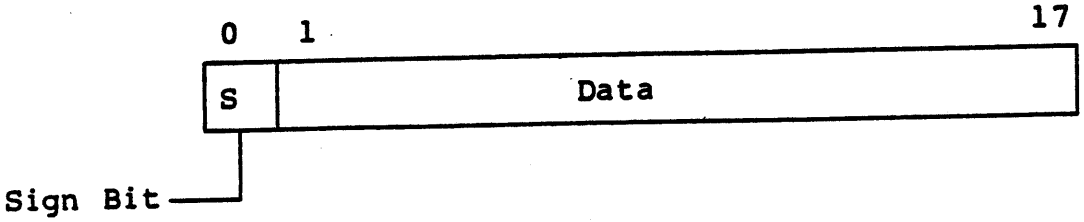
The instruction counter word format follows:



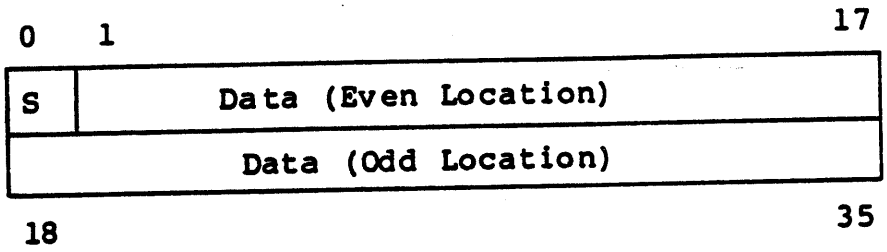
4.2.9.10 Operands

The word formats for the operands are as follows:

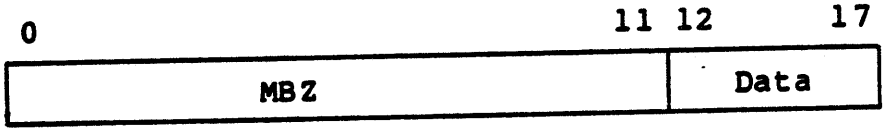
Single Precision Word:



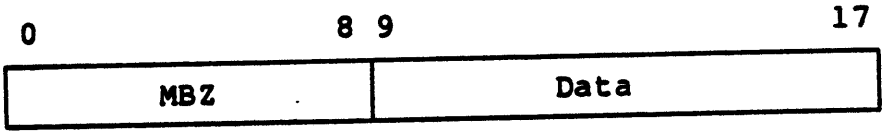
Double Precision Word:



6-Bit Character:



9-Bit Character:



NOTE

The character position in storage is determined by the character address.

4.2.10 System T&D Instructions

Special Test and Diagnostic (T&D) versions of standard system instructions are provided in this subsection to aid in resolving failures in the processor or in other system components. The instructions are:

- CRA: Copy Register to A (Octal 7332XX)
- CAR: Copy A to Register (Octal 1332XX)
- CAQC: Copy AQ to Channel (Octal 533200)
- CCQ: Copy Channel to Q (Octal 533300)

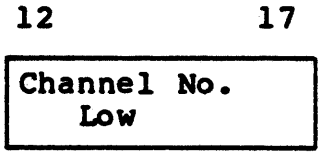
The CACQ and CCQ instructions allow T&D access to registers and control in system components that are completely external to the processor (e.g., the IOM, PCLU, I/O channels). The definitions of these T&D instructions are contained in the appropriate component specification manuals (refer to subsection 1.2 of this manual for the order numbers).

CACQ: Copy Accumulator and Quotient to Channel (Octal 533200)

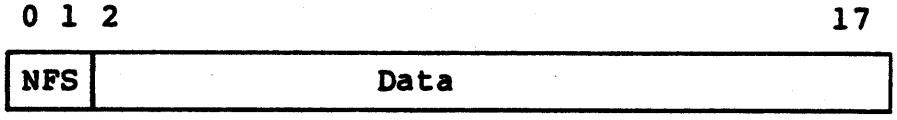
Summary:

Data and control information are delivered to the controller, which is connected to the channel specified by the SEL register and bits 8 through 11 of the A register. The software visible format is as follows:

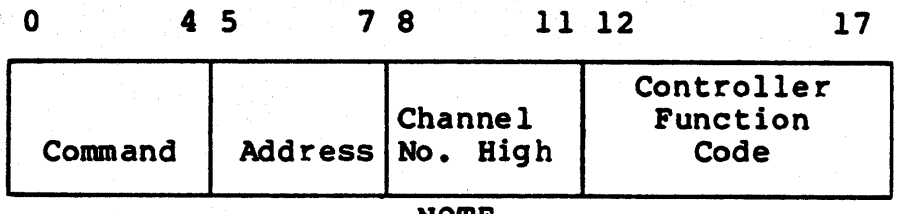
SEL Register:



Q Register:



A Register:



NOTE

The K field (Y_{12-17}) must be octal 00.

Indicators:

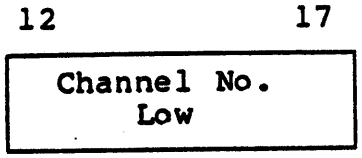
The indicators are not affected.

CCQ: Copy Channel to Quotient (Octal 533300)

Summary:

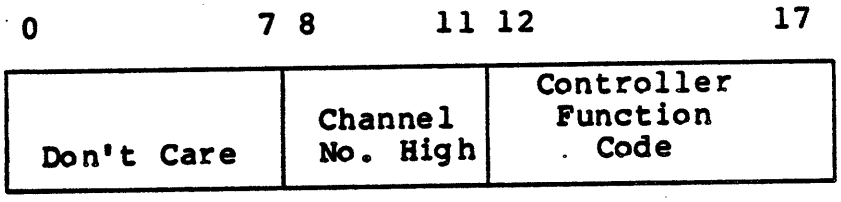
Control information is delivered from the accumulator to the controller, which is connected to the channel specified by the SEL register and bits 8 through 11 of the Accumulator. Then, 16 bits of data are returned to the Quotient register. The software visible formats before and after the instructions are as follows:

SEL Register:



Before

A Register:

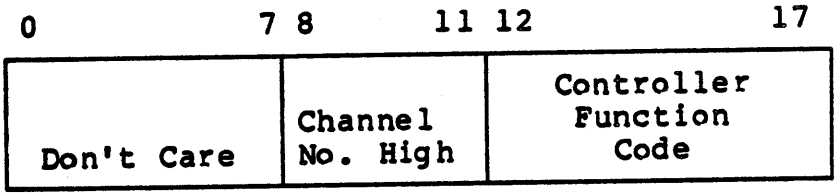


Q Register:

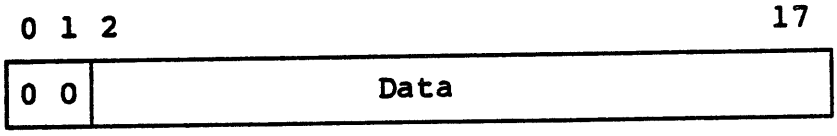
Don't Care

After

A Register:



Q Register:



NOTE

The K field (Y_{12-17}) must be octal 00.

Indicators:

The indicators are not affected.

CRA: Copy Register to A (Octal 7332XX)
CAR: Copy A to Register (Octal 1332XX)

Summary:

The CRA and CAR instructions allow T&D access to registers and control associated with the CPU, including the PATU and the cache memory unit. The K field of the instruction word (i.e., the six low-order bits) specifies the register or function. The K field values are assigned as follows:

- Octal 0XXXXX: CPU
- Octal 10XXXX: PATU
- Octal 11XXXX: Cache Memory Unit.

The PATU and cache CRA/CAR orders (i.e., K field assignments) are defined in the specific option manuals (refer to subsection 1.2 of this manual for the order numbers).

The CPU CRA/CAR instructions (i.e., K field assignments) are defined in the following charts:

Copy Register to A Instruction Chart

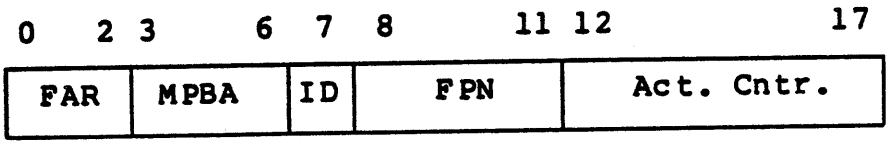
CRA K FIELD (Octal)	REGISTER/FUNCTION
00	Processor Number, A Register = CPU's ID (bit 7)
01	Panel Register, A Register = Panel Data
02	Hardware Q Register, A Register = (Q Register) Live
03	Hardware IC Register, A Register = (IC Register) Live
04	Combination Register*, A Register = Contents of Combination Register
05	Read System Bus, A Register = Address Bus & Q Register = Read Data Bus, LSB of Function Code = Zero
06-57	Reserved for Future Use
60	Load Cache
61	Store Cache

*The layout of the Combination Register appears after the CAR Instruction Chart.

Copy A to Register Instruction Chart

CAR K FIELD (Octal)	REGISTER/FUNCTION
00	Reserved for Future Use
01	Panel Register, A Register = Panel Data
02	Places CPU in Stop Mode
03	Panel Register Data to A Register and Stop
04	Write System Bus, A Register = Address Bus & Q Register = Write Data Bus, LSB of Function Code = One
05-57	Reserved for Future Use
60	Initialize Cache (Leaves Cache in Offline Mode)
61	Cache Off
62	Cache On
63	Set Hit Fault Mode
64	Reset Hit Fault Mode
65	Reserved for Future Use
66	Disable Timers
67	Enable Timers

The layout of the Combination Register is as follows:



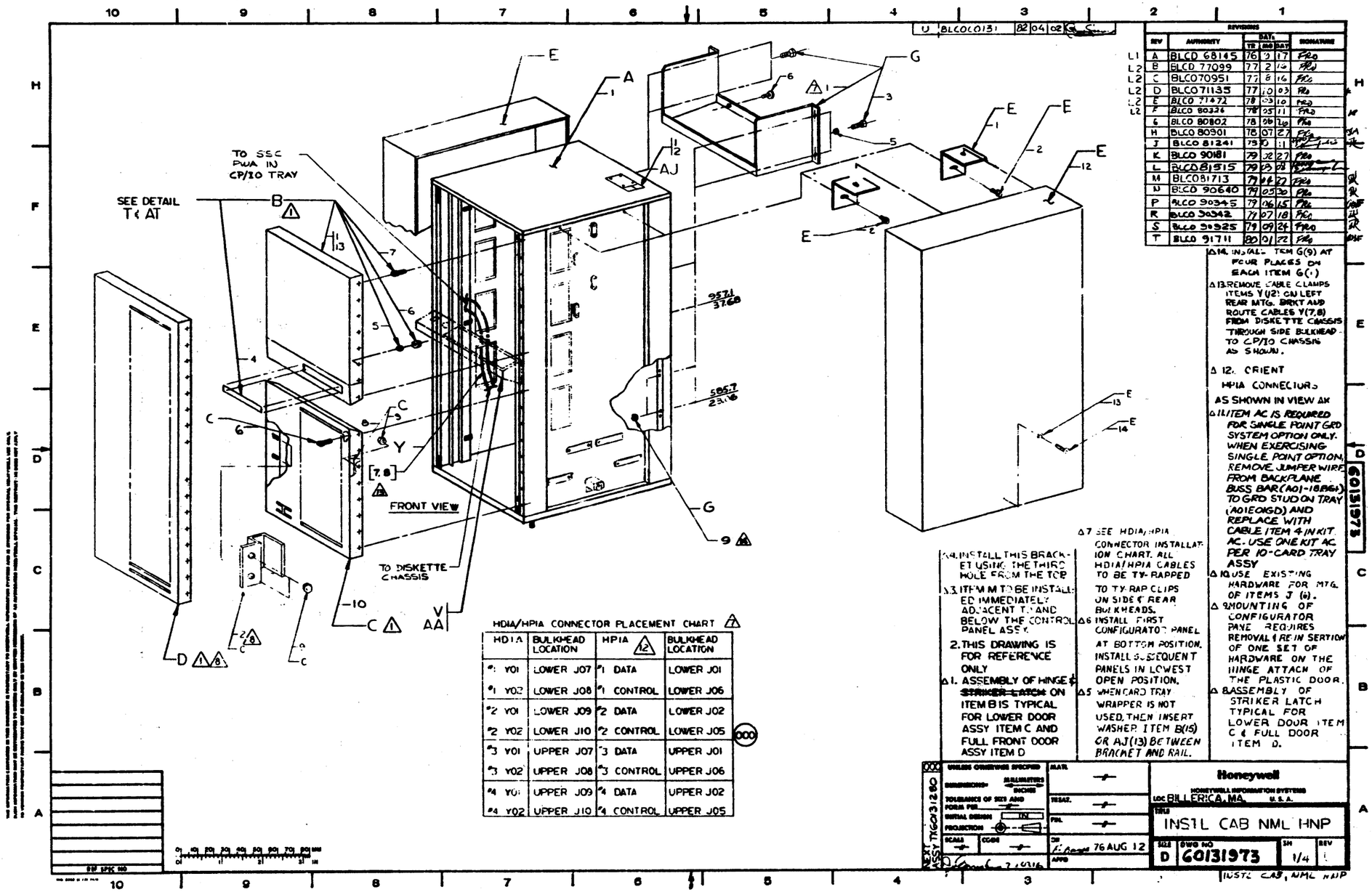
where:

FAR = Fractional Address Register
MPBA = Microprogram Branch Analysis
ID = Processor Identification
FPN = Fault Priority Network
Act. Cntr. = Activity Counter

V
SYSTEM PARTS CATALOG

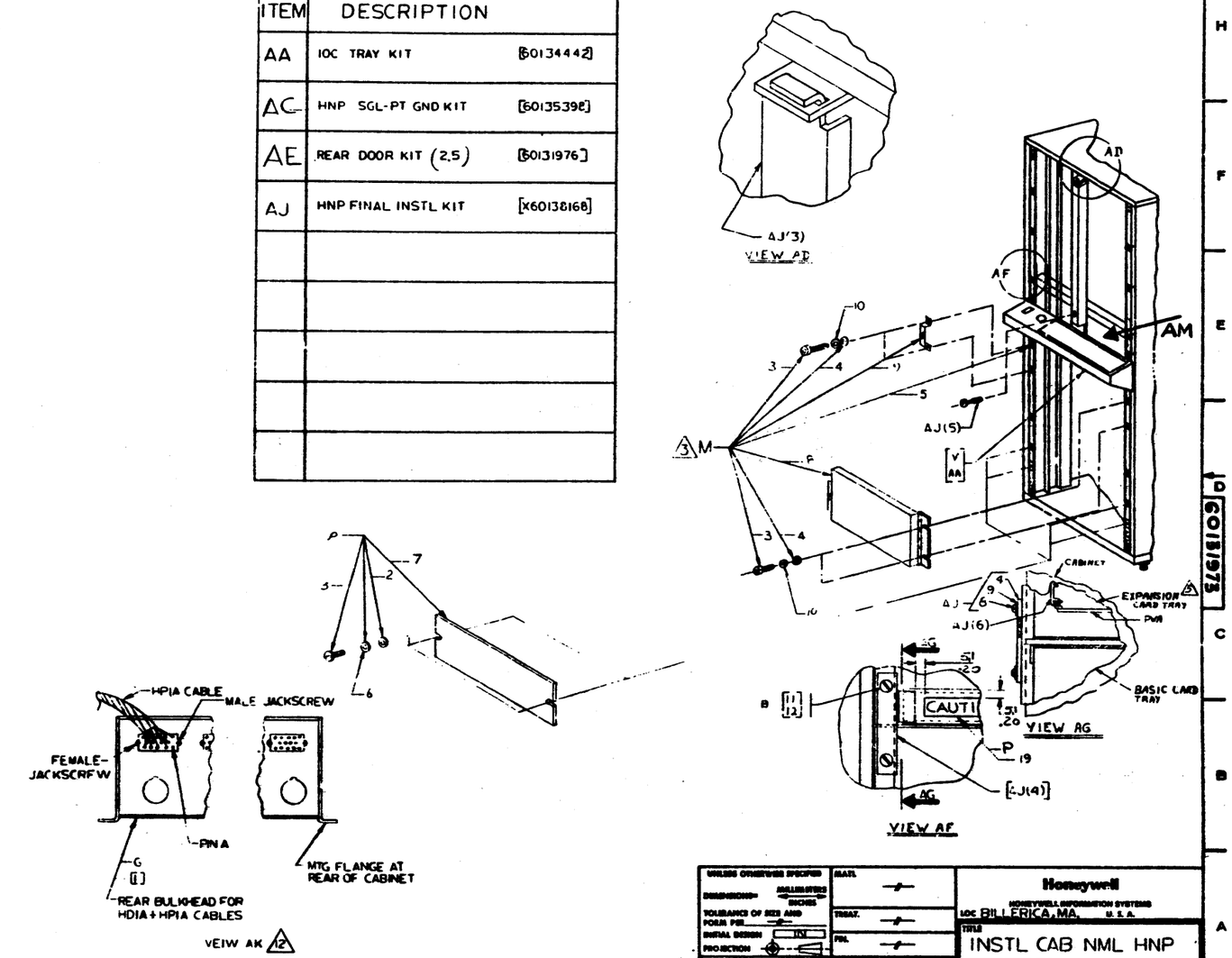
This section contains the parts lists and engineering drawings for the different components of the DATANET system. They are arranged in the following order:

- BRCK181A Cabinet Installation
- BRCK183A Cabinet Installation
- Ten-Card Tray Assembly
- Ten-Card Tray Installation
- Ten-Card Tray Installation Kit
- Keyboard Assembly
- Diskette Installation
- Diskette Installation Kit
- PDU Installation Kit
- Configuration Panel Kit
- Communications Bulkhead Installation
- Communications Bulkhead Installation Kit
- Mini Bulkhead Installation
- Mini DIA Bulkhead Installation Kit
- Mini PIA Bulkhead Installation Kit.



ITEM	DESCRIPTION
A	NML SYSTEM CAB ASSY(HNP) [E60131972]
B	UPPER FRONT DOOR KIT [X60131280]
C	LOWER FRONT DOOR KIT [X60129721]
D	FULL FRONT DOOR KIT [X60129722]
E	BULKHEAD COVER KIT [X...]
F	~~RIGHT SKIN KIT [X60129724]~~
G	BULKHEAD KIT REAR [X60132116]
H	~~LEFT SKIN KIT [X60129723]~~
J	CONFIGURATOR PANEL KIT [X60132081]
L	~~5 CARD TRAY INSTL [E60129830]~~
M	...STD PNL KIT [X60134014]
N	
P	DUMMY PANEL KIT [X60132082]
R	REAR DOOR KIT [X60129881]
S	PDU INSTL KIT [X60133613]
Y	...SETTE INSTL KIT [X60128543]
V	10 CARD TRAY INSTL KIT [X60132034]

ITEM	DESCRIPTION	
AA	IOC TRAY KIT	[60134442]
AC	HNP SGL-PT GND KIT	[60135392]
AE	REAR DOOR KIT (2.5)	[60131976]
AJ	HNP FINAL INSTL KIT	[X60138168]



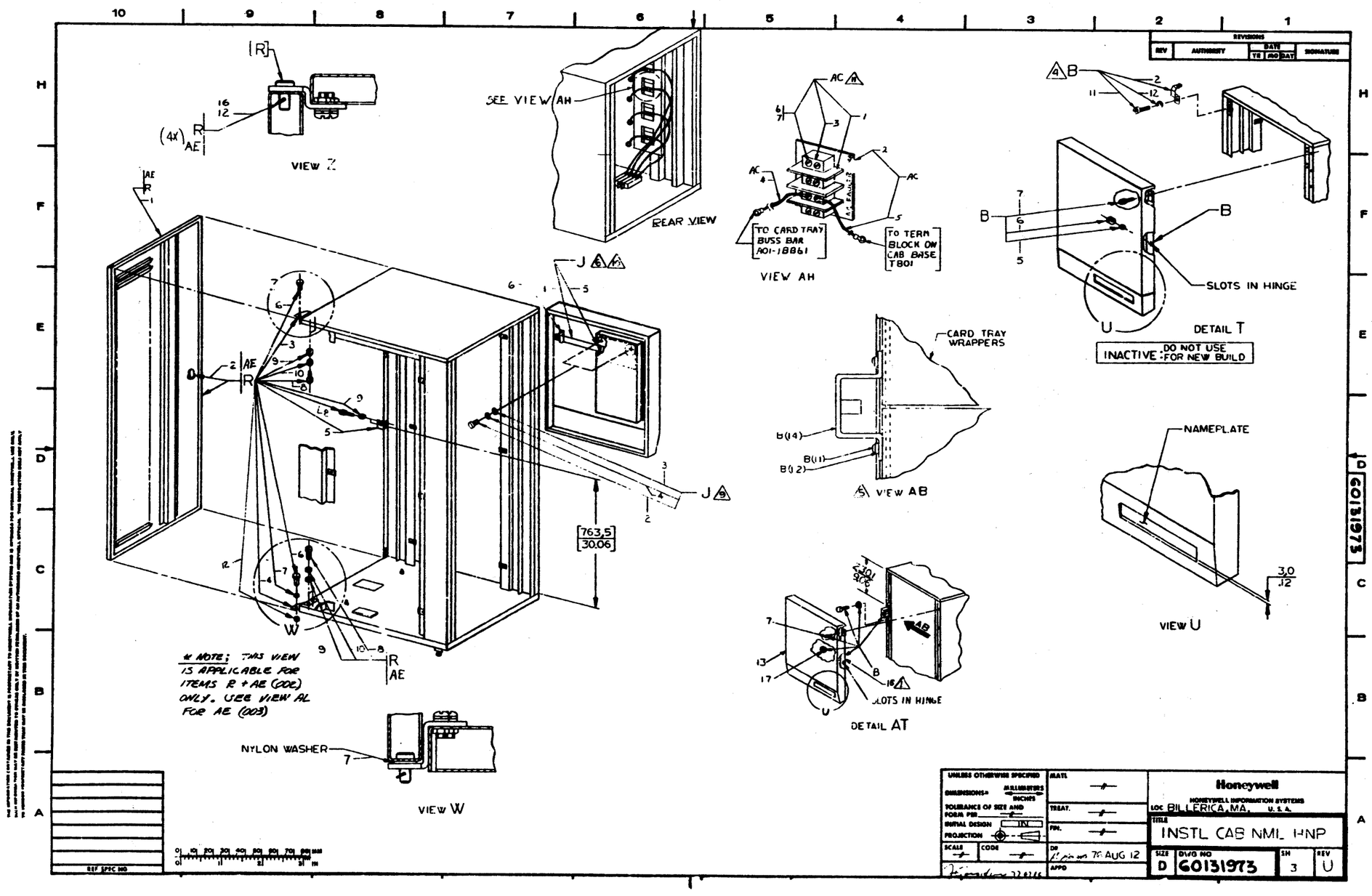
REVISIONS				
REV	AUTHORITY	DATE YR	MO	DAY

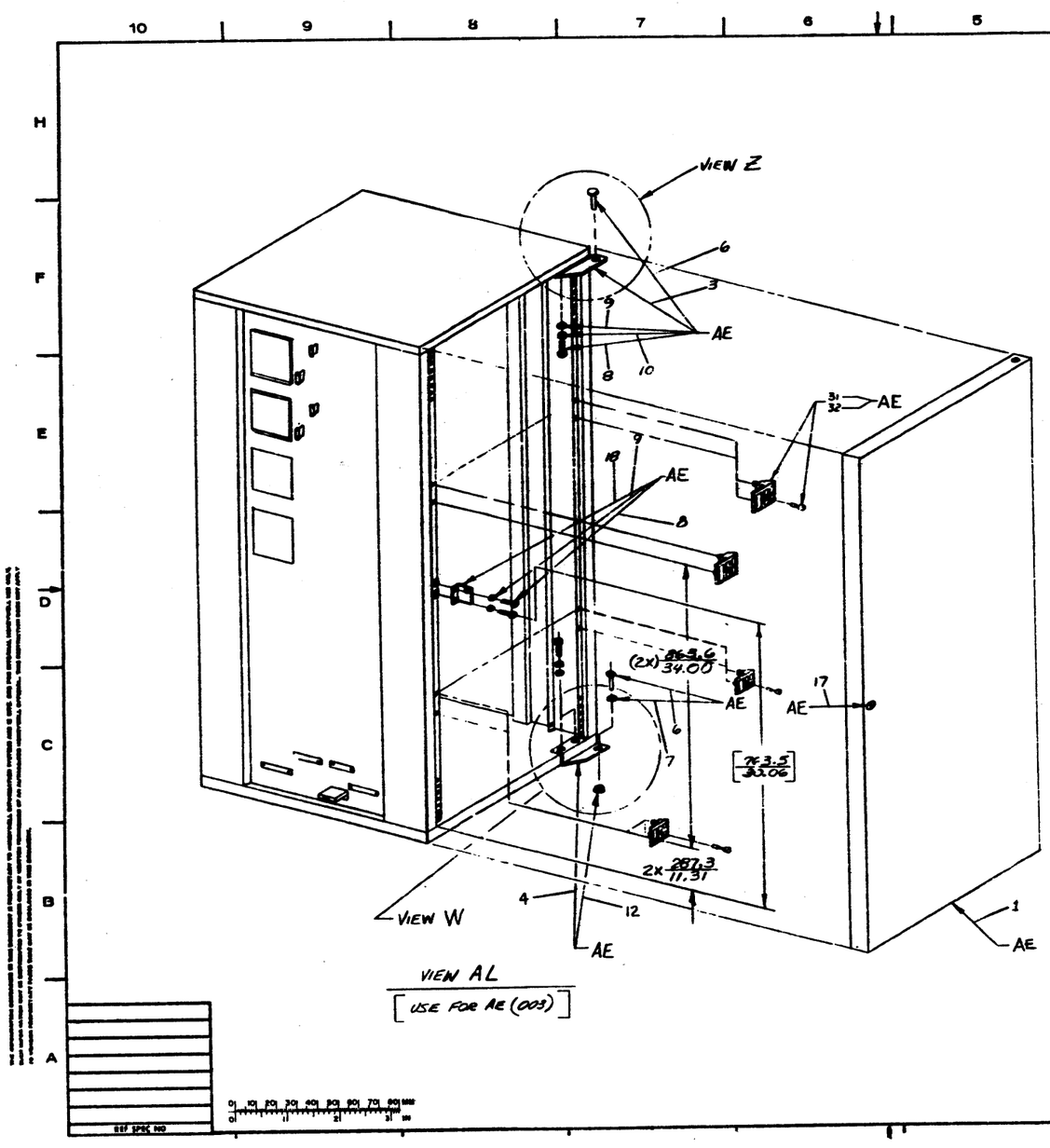
UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES; TOLERANCE OF SIZE AND FORM PER; INITIAL DESIGN; PROJECTION; SCALE; CODE; MATL; TREAT; FINI; DR 76 AUG 12; APPD

Honeywell
HONEYWELL INFORMATION SYSTEMS
LOC BILLERICA, MA. U.S.A.

TITLE: INSTL CAB NML HNP

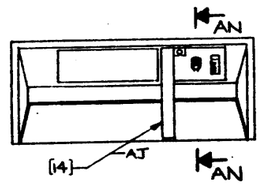
SIZE	DWG NO	SH.	REV
D	60131973	2	S


VIEW Z
SEE VIEW AH
REAR VIEW
VIEW AH
TO CARD TRAY BUSS BAR A01-18861
TO TERM BLOCK ON CAB BASE TB01
DETAIL T
INACTIVE: DO NOT USE FOR NEW BUILD
SLOTS IN HINGE
CARD TRAY WRAPPERS
VIEW AB
NAMEPLATE
VIEW U
763,5
30,06
* NOTE; THIS VIEW IS APPLICABLE FOR ITEMS R + AE (002) ONLY. USE VIEW AL FOR AE (003)
NYLON WASHER
VIEW W
DETAIL AT
SLOTS IN HINGE
REVISIONS
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN MILLIMETERS / INCHES
TOLERANCE OF SIZE AND FORM PER
INITIAL DESIGN
PROJECTION
SCALE
CODE
MATL
TREAT.
FIN.
APPD
Honeywell
HONEYWELL INFORMATION SYSTEMS
LOC BILLERICA, MA. U.S.A.
TITLE
INSTL CAB NML HNP
SIZE D
DWG NO 60131973
SH 3
REV U
REF SPEC NO
60131973

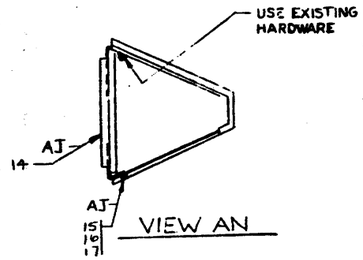


VIEW AL

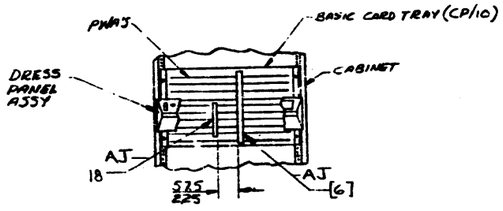
[USE FOR AE (003)]



VIEW AM



VIEW AN



VIEW AP

[FRONT OF CABINET]

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN MILLIMETERS / INCHES; TOLERANCE OF SIZE AND FORM PER —; INITIAL DESIGN —; PROJECTION —; SCALE —; CODE —	MATL —	Honeywell; HONEYWELL INFORMATION SYSTEMS; LOC BILLERICA, MA. U.S.A.	
	TREAT. —	TITLE: INSTL CAB NML HNP	
	FIN. —	SIZE D; DWG NO 60131973; SH 4F; REV U	
	DR. 79-2-12		
	APPD		

REF SPEC NO

60131973 D

ITEM	DESCRIPTION	
A	HNP SYS CAB ASSY	[X60143377]
B	UPPER FRONT DOOR KIT	[X60131280]
C	LOWER FRONT DOOR KIT	[X60129721]
D	LEFT SIDE SKIN KIT	[X60129726]
E	BULKHEAD KIT REAR	[X60132116]
F	CONFIGURATOR PANEL KIT	[X60132081]
G	VENTED PNL KIT-7CD	[X60143458-103]
H	COMM BLKHD KIT	[X60140740]
J	PDU INSTL KIT	[X60133610]
K	DISKETTE INSTL KIT	[X60128343]
L	IOC TRAY KIT	[X 60134442]
M	HNP SGL-PT GND KIT	[X 60135338]
N	HNP/UNCP REAR DOOR KIT	[X60140683]
P	HNP FINAL INSTL KIT	[X60138168]
Q	RIGHT SIDE SKIN KIT	[X60129724]
R	KIT MINI BLKHD	[X60143839]
S	KIT BLKHD MINI PIA	[X60146658]

H DIA/HPIA CONNECTOR PLACEMENT CHART

HDIA	BULKHEAD LOCATION	HPIA	BULKHEAD LOCATION
#1 Y01	LOWER J07	#1 DATA	LOWER J01
#1 Y02	LOWER J08	#1 CONTROL	LOWER J06
#2 Y01	LOWER J09	#2 DATA	LOWER J02
#2 Y02	LOWER J10	#2 CONTROL	LOWER J05
#3 Y01	UPPER J07	#3 DATA	UPPER J01
#3 Y02	UPPER J08	#3 CONTROL	UPPER J06
#4 Y01	UPPER J09	#4 DATA	UPPER J02
#4 Y02	UPPER J10	#4 CONTROL	UPPER J05

△15. UTILIZE ALL POS. OF DIA "FIRST BLKHD" BEFORE ADDING "SECOND BLKHD" TO SYSTEM. START WITH LOWER DIA. POS #1 (J01-J03) THEN ON TO DIA. POS #2 (J01-J03)

△14. THIS CHART APPLIES TO ITEM E BLKHD KIT (60132116) ONLY.

△13. ORIENT HPIA CONNECTORS AS SHOWN IN VIEW AK

△12. INSTALL ITEM 3(E) AT FOUR PLACES ON EACH ITEM 1(E)

△11. ROUTE CABLES ITEMS 7+8 (K) FROM DISKETTE CHASSIS TO SIDE AND UP TO CP/IO CHASSIS AS SHOWN.

△10. ITEM M IS REQUIRED FOR SINGLE POINT GRD SYSTEM OPTION ONLY. WHEN EXERCISING SINGLE POINT OPTION REMOVE JUMPER WIRE FROM BACKPLANE BUSSBAR (A01-18BG) TO GRD STUD ON TRAY (A01E01GD) AND REPLACE WITH CABLE ITEM 4 IN KIT M USE ONE KIT M PER IO CARD TRAY ASSY

△9. USE EXISTING HARDWARE FOR MOUNTING ITEMS 6 (F)

△8. MOUNTING OF CONFIGURATOR PANEL REQUIRES REMOVAL & RE-INSERTION OF ONE SET OF HARDWARE ON THE HINGE ATTACH AREA OF THE PLASTIC DOOR.

△7. ASSEMBLY OF STRIKER LATCH TYPICAL FOR LOWER DOOR ITEM C

△6. SEE HDIA/HPIA CONNECTOR INSTALLATION CHART. ALL HDIA/HPIA CABLES TO BE TY-RAPPED TO TY-RAP CLIPS ON SIDE & REAR BULKHEADS.

△5. INSTALL FIRST CONFIGURATOR PANEL AT BOTTOM POSITION. INSTALL SUBSEQUENT PNLS IN LOWEST OPEN POSITION.

△4. WHEN CARD TRAY WRAPPER IS NOT USED, INSERT WASHER ITEM 15 BETWEEN BRACKET & RAIL.

△3. ITEM G TO BE INSTALLED IMMEDIATELY ADJACENT TO AND BELOW THE CONTROL PANEL ASSY.

2. THIS DRAWING IS FOR REFERENCE ONLY.

△1. ASSEMBLY OF HINGE ON ITEM B IS TYPICAL FOR LOWER DOOR ASSY ITEM C.

△16. UTILIZE ALL POS OF PIA "FIRST BLKHD" BEFORE ADDING "SECOND BLKHD" TO SYSTEM. START WITH LOWER PIA POS. (J01, J02) THEN ON TO UPPER PIA. POS. (J03, J04).

REVISIONS					
REV	AUTHORITY	DATE YR	DATE MO	DATE DAY	SIGNATURE
L2 C	BLCOA0288	80	3	11	
D	BLCOB0815	81	11	19	
E	BLCOC0131	82	04	02	

60140769

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN MILLIMETERS / INCHES; TOLERANCE OF SIZES AND FORMS PER ---; MATERIAL ---; TREAT. ---; FINISH ---; NEXT ASSY

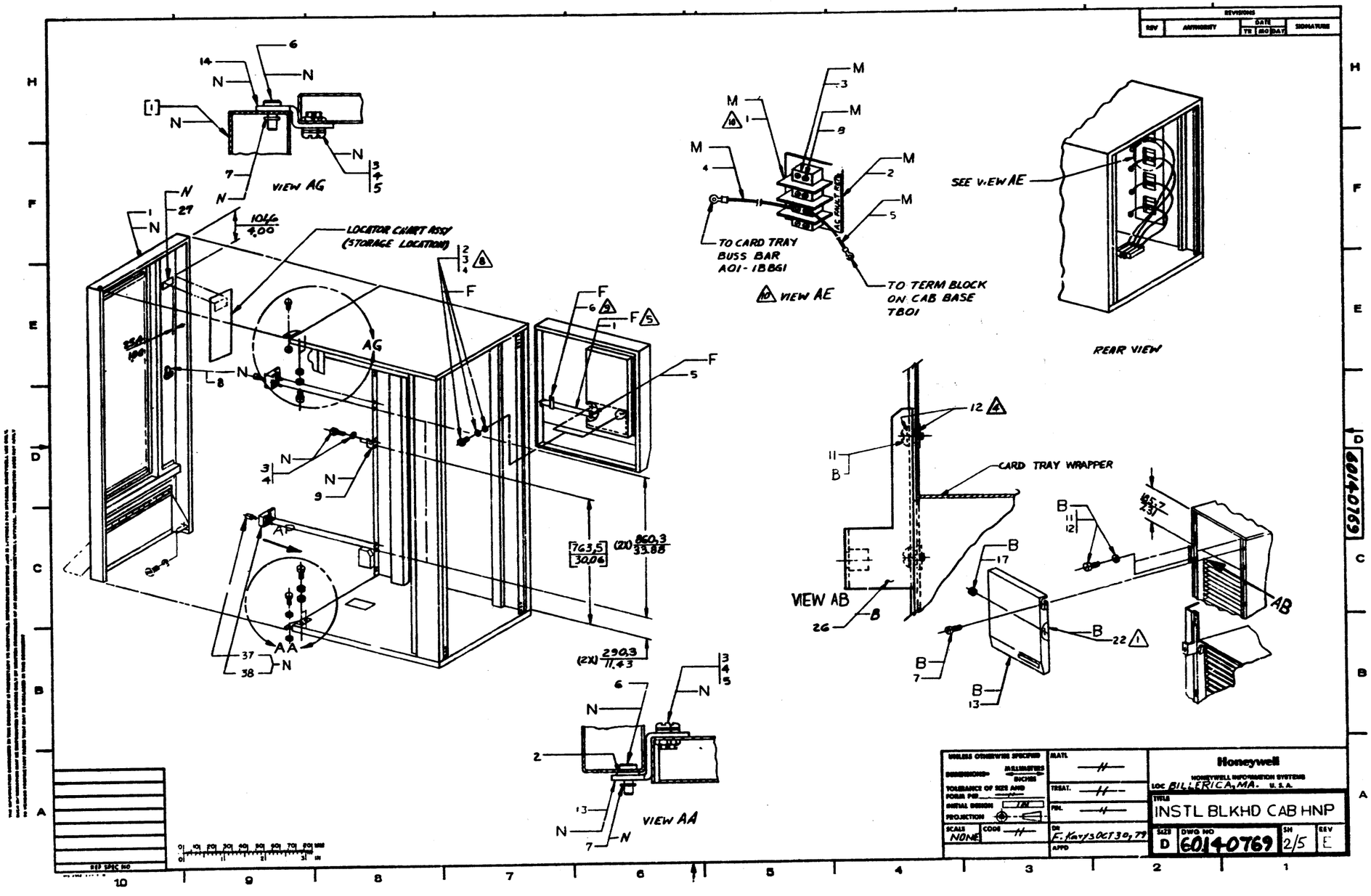
Honeywell
HONEYWELL INFORMATION SYSTEMS
BILLERICA, MA. U.S.A.

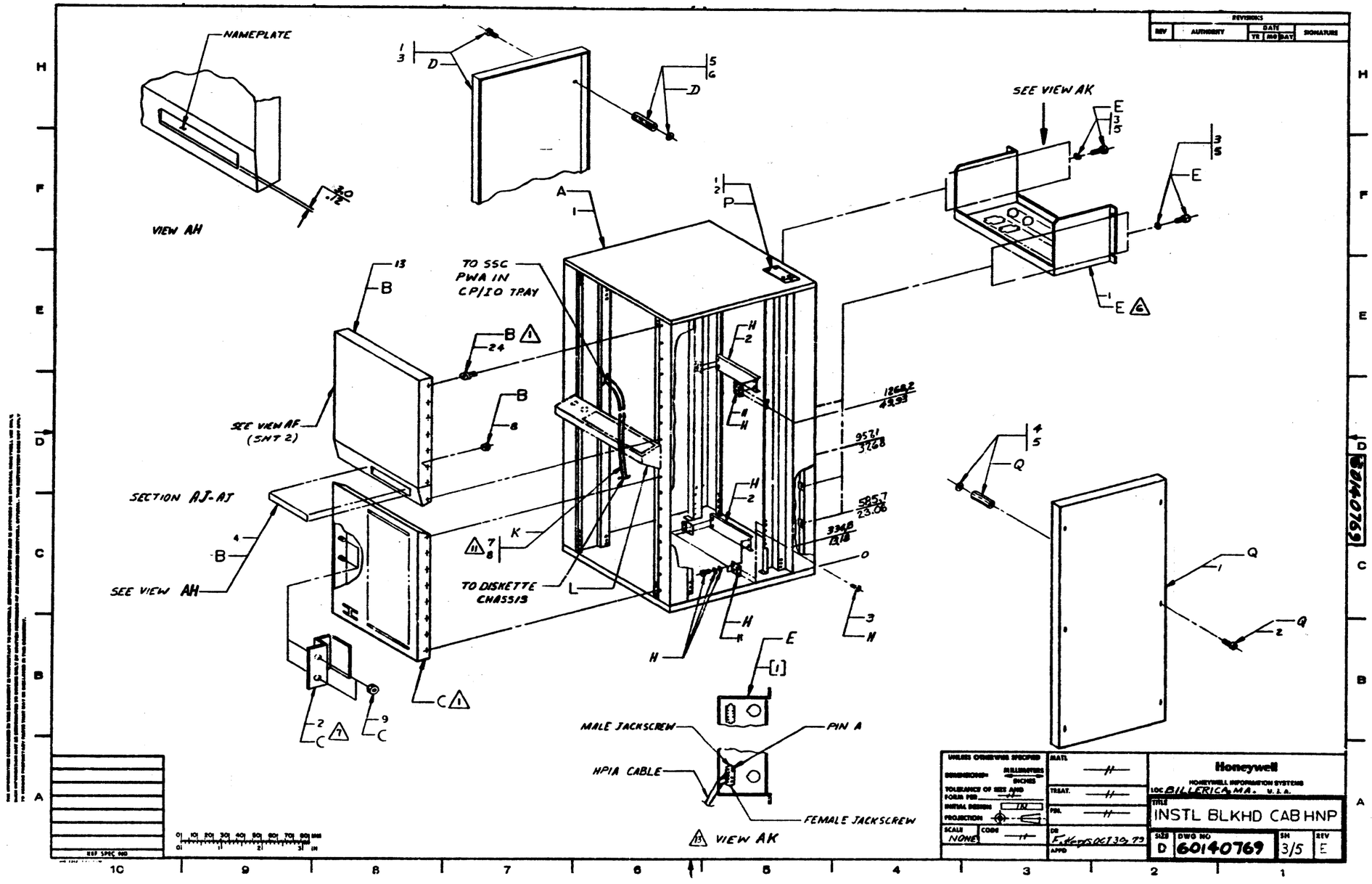
TITLE: INSTL BLKHD CAB HNP

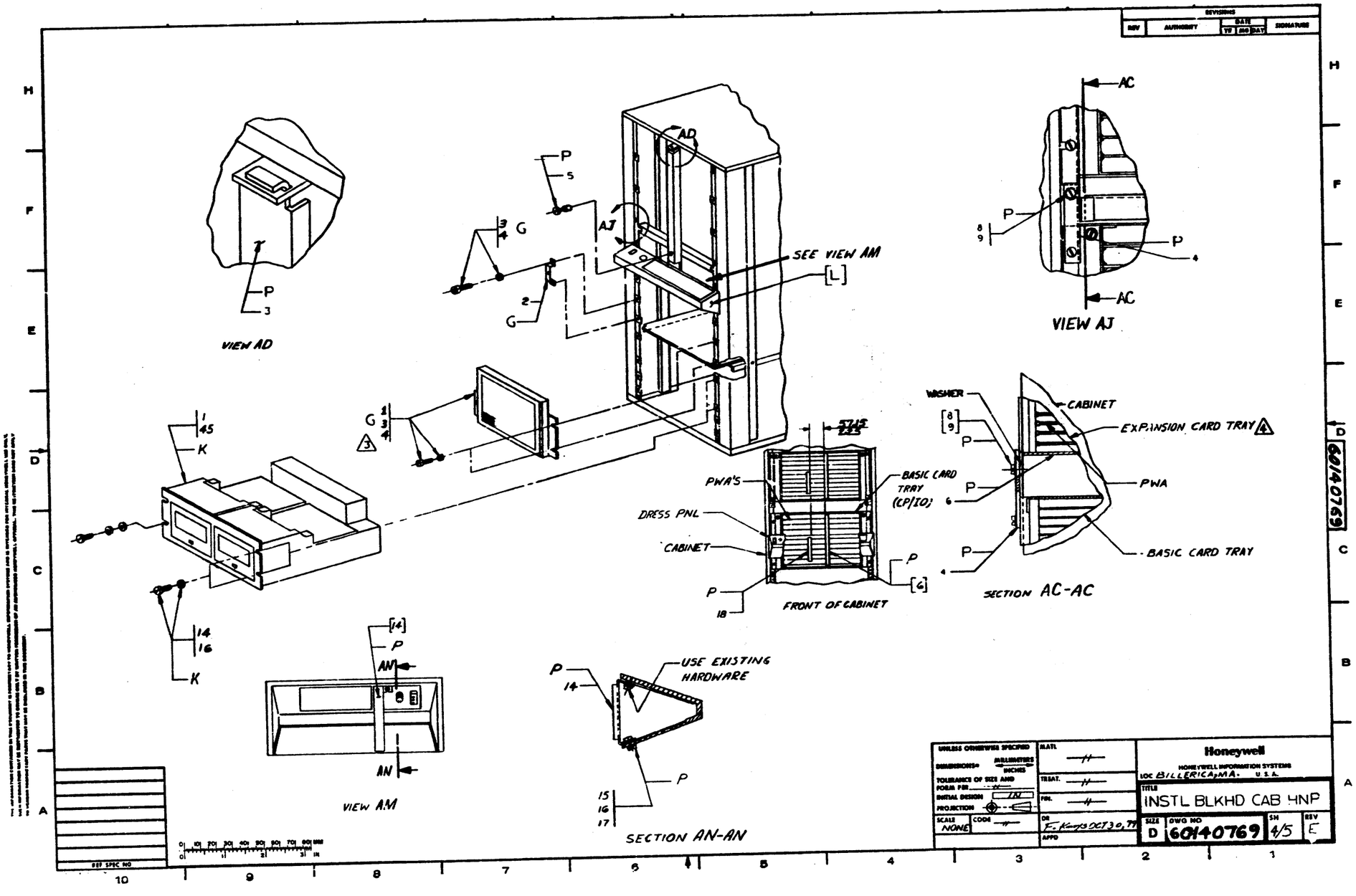
SCALE: NONE | CODE | DR: E. Kevis OCT 30 '82 | APPD

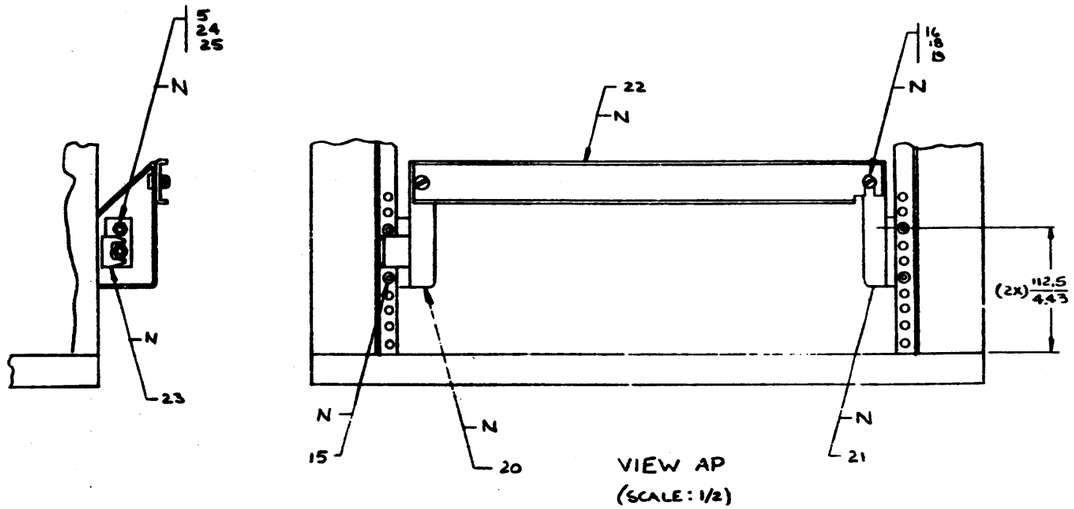
SIZE: D | DWG NO: 60140769 | SH: 1/5 | REV: E

REF SPEC NO




NAMEPLATE
VIEW AH
SEE VIEW AK
TO SSC PWA IN CP/IO TRAY
SEE VIEW AF (SHT 2)
SECTION AJ-AJ
SEE VIEW AH
TO DISKETTE CHASSIS
MALE JACKSCREW
PIN A
HPIA CABLE
FEMALE JACKSCREW
VIEW AK
REVISIONS
REV
AUTHORITY
DATE
SIGNATURE
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN MILLIMETERS / INCHES
TOLERANCE OF SIZES AND FORMS PER
INITIAL DESIGN
PROJECTION
SCALE NONE
CODE
MATL
TREAT.
FINISH
DO
APPD
Honeywell
HONEYWELL INFORMATION SYSTEMS
LOC BILLERICA, MA. U.S.A.
TITLE
INSTL BLKHD CAB HNP
SIZE D
DWG NO 60140769
SH 3/5
REV E





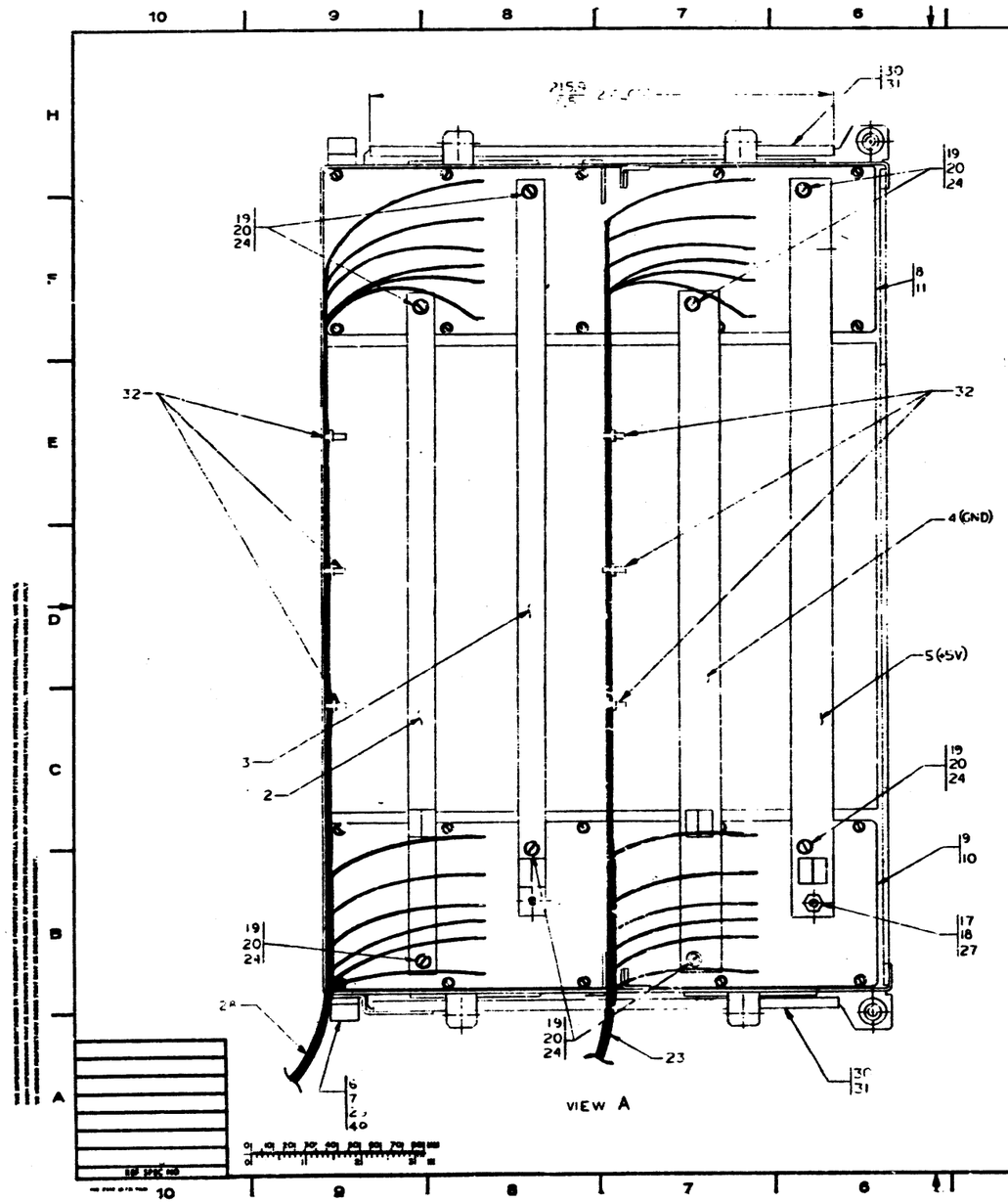
REVISIONS

REV	AUTHORITY	DATE	SIGNATURE
		YR MO DAY	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MILLIMETERS / INCHES; TOLERANCE OF SIZE AND FORM PER; INITIAL DESIGN; PROJECTION	MATL	Honeywell — HONEYWELL INFORMATION SYSTEMS — LOC BILLERICA, MA. U.S.A.	
	TREAT.	TITLE: INSTL BLKHD CAB HNP	
SCALE NONE CODE	FOL.	SIZE D	DWG NO 60140769
	DR E. Kaplan 12/3/79	SH 5F	REV E
	APPD		

REF SPEC NO

60140769



REVISIONS					
REV	AUTHORITY	DATE YR	MO	DAY	SIGNATURE
A	BLCO SN273	76	10	21	
B	BLCO 8715	77	01	10	
C	BLCO 71104				
D	BLCO 71243	77			
E	BLCO 71001	78	02	03	
F	BLCO 71332	78	03	07	
G	BLCO 80148	78	03	31	
H	BLCO 80135	78	07	14	
J	BLCO 81743	79	03	21	
K	BLCO 90691	79	07	26	
L	BLCO 82888	79	10	09	
M	BLCO 81159	79			
N	BLCO 91161	80	03	21	
P	BLCO A02235	80	08	20	
R	BLCO A05627	80	09	18	

L2

Δ 3-FIXTURES REQUIRED TO LOCATE I/O BACKPLANE CONN KEYS RELATIVE TO FORMED CARD GUIDES OF ITEM 1.

Δ 2-CENTERLINE OF CONNECTOR CARD SLOT.

Δ 1-KEYWAY

002001

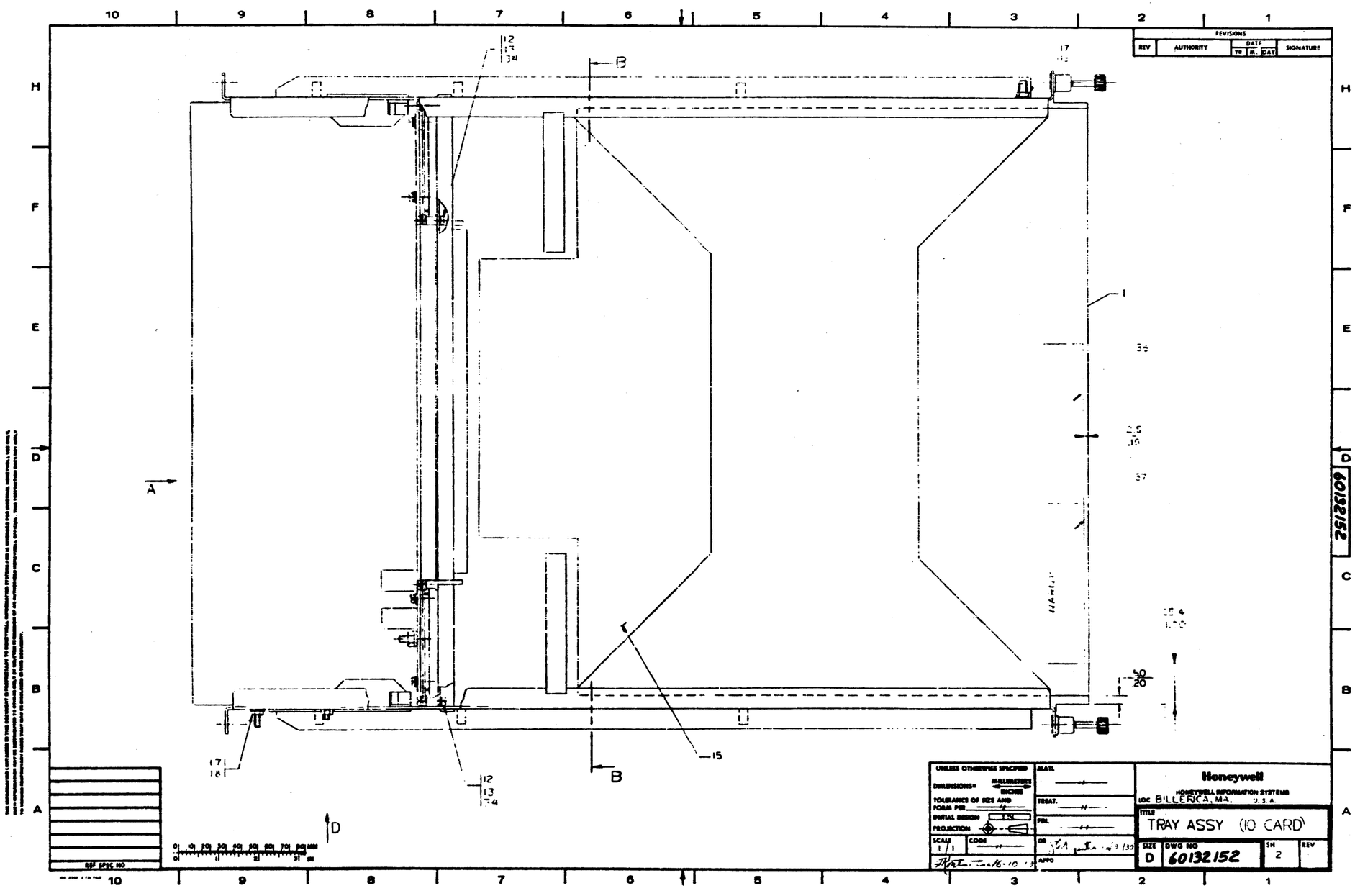
UNLESS OTHERWISE SPECIFIED DIMENSIONS: MILLIMETERS / INCHES
TOLERANCE OF REF ANGS FOR A PER ITEM 4
MATRIAL DESIGN
PROJECTION
SCALE 1/1
CODE
MAT'L
BASIC
TREAT.
FINISH
DR
APPD

Honeywell
HONEYWELL INFORMATION SYSTEMS
LOC: LEXICA, MA. U.S.A.

TITLE: TRAY ASSY (10 CARD)

SIZE D | DWG NO 60132152 | SH 1/3 | REV R

25126109


REVISIONS
REV
AUTHORITY
DATE
YR
M.
DAY
SIGNATURE
B
A
D
12
13
14
17
18
15
1
Honeywell
HONEYWELL INFORMATION SYSTEMS
LOC BILLERICA, MA. U.S.A.
TRAY ASSY (10 CARD)
SIZE
D
DWG NO
60132152
SH
2
REV
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN
MILLIMETERS
INCHES
TOLERANCE OF SIZE AND FORM PER
INITIAL DESIGN
PROJECTION
SCALE
1/1
CODE
MATL
TREAT.
FIN.
APPD
60132152

REVISIONS			
REV	AUTHORITY	DATE YR MO DAY	SIGNATURE

304,80 ± 0,13
12.000 ±.005

24,26 ±0,25
.955 ±.010

1,12 ±0,1
.044 ±.005

SECTION B B

SECTION E-E (-X)

VIEW D

A01E02GD

A01E01GD

UNLESS OTHERWISE SPECIFIED	MATL
DIMENSIONS= MILLIMETERS / INCHES	
TOLERANCE OF SIZE AND FORM PER	TREAT.
INITIAL DESIGN	FIN
PROJECTION	
SCALE 1/1	CODE
	DR.
	APPD.

Honeywell
HONEYWELL INFORMATION SYSTEMS
LOC HILLERICA, MA U.S.A.

TITLE: TRAY ASSY (10 CARD)

SIZE	DWG NO	SH	REV
D	60132152	3F	

REF SPEC NO

60132152 D

•	ITEM NO	P C	IDENTIFICATION NO.	S C	DRAWING TITLE	ASSEMBLY/QUANTITY 001	002							U M
	1	TE	60132003-001	A	TRAY FAB 10 CD	INTCH	INTCH							EA
	1	TE	60132003-002	A	TRAY FAB 10 CD	1	1							EA
	2	TC	60131215-002	A	BUS BAR ASSY	1	1							EA
	3	TC	60131215-001	A	BUS BAR ASSY	1	1							EA
	4	TC	60132151-001	A	BUS BAR ASSY	1	1							EA
	5	TC	60132151-002	A	BUS BAR ASSY	1	1							EA
	6	TD	60129865-001	V	RAIL TRAY	2	2							EA
	7	A	03010002-012	V	SCREW PNS 632 1/2	8	8							EA
	8	TD	60128300-005	A	BUS ASSY TYP I/O B/P	INTCH	-							EA
	8	TD	60130278-001	A	BUS ASSY I/O 10 CD	1	-							EA
	9	TD	60128300-006	A	BUS ASSY TYP I/O B/P	INTCH	-							EA
	9	TD	60130278-002	A	BUS ASSY I/O 10 CD	1	-							EA
	10	TD	60128300-007	A	BUS ASSY TYP I/O B/P	-	INTCH							EA
	10	TD	60130278-003	A	BUS ASSY I/O 10 CD	-	1							EA
	11	TD	60128300-008	A	BUS ASSY TYP I/O B/P	-	INTCH							EA
	11	TD	60130278-004	A	BUS ASSY I/O 10 CD	-	1							EA

Honeywell
HONEYWELL INFORMATION SYSTEMS
LOC. BILLERICA, MASSACHUSETTS, USA.

UM = UNIT OF MEASURE
EA = EACH, IN = INCHES, CM = CENTIMETER, OZ = OUNCE, G = GRAMS

•=ITEMS CHANGED SINCE REV N

TITLE: TRAY ASSY (10 CARD)

SIZE	P.L. NO.	SHEET	REV.
TD	60132152	1/3	R

DOES A DOCUMENT REVISION STATUS SHEET EXIST? NO

S = SUBSTITUTE PARTS

•	ITEM NO.	P C	IDENTIFICATION NO.	S C	DRAWING TITLE	ASSEMBLY/QUANTITY 001	002							U M
	12	A	03010006-006	V	SCREW PNS 440 1/4	16	16							EA
	13	A	70902055-001	V	WASH FLAT CRES 12	16	16							EA
	14	A	13010007-000	D	MFG TOLERANCES	X	X							
	15	A	02060085-001	M	PLSTC S MY .007	1	1							IN
	16	TB	60131122-001	P	RETAINER CBL DC	1	1							EA
	17	A	03030001-005	V	NUT HEX STL 832	4	4							EA
	18	A	03020004-004	V	WASH LCK EX-TTH 8	4	4							EA
	19	A	76951117-564	V	SCREW PNS 4X0.7 X12	8	8							EA
	19	A	76951117-566	V	SCREW PNS 4X0.7 X16	8	8							EA
	20	A	76951126-550	V	WASH FLAT STEEL 4	8	8							EA
	21	C	60128729-001	D	SCHEM PWR DC 10 CC	X	X							--
	23	TK	60128730-001	A	JL PWR CBL 10 CC	1	1							EA
	24	A	76951134-550	V	WASH LCK HL-SPR 4	8	8							EA
	25	A	03030001-004	V	NUT HEX STL 632	1	1							EA
	26	A	03020004-003	V	WASH LCK EX-TTH 6	1	1							EA
	27	A	03020001-010	V	WASH FLAT STEEL 6	1	1							EA

Honeywell
HONEYWELL INFORMATION SYSTEMS
LOC. BILLERICA, MASSACHUSETTS, USA.

UM = UNIT OF MEASURE
EA = EACH, IN = INCHES, CM = CENTIMETER, OZ = OUNCE, G = GRAMS

•=ITEMS CHANGED SINCE REV N

TITLE: TRAY ASSY (10 CARD)

SIZE	P.L. NO.	SHEET	REV.
TD	60132152	2	R

DOES A DOCUMENT REVISION STATUS SHEET EXIST? NO

S = SUBSTITUTE PARTS

890729

SIZE	P.L. NO.	SHEET	REV.
TD	60132152	3	R

•	ITEM NO.	P C	IDENTIFICATION NO.	S C	DRAWING TITLE	ASSEMBLY/QUANTITY 001	002							U M
	28	TK	60128728-001	A	JL PWR CBL 5 CC	1	1							EA
•	29	A	03020003-004	V	WASH LCK 8	8	8							EA
	30	A	02630001-001	M	CHAN RBR 5/32	AR	AR							IN
	31	A	02710004-001	M	ADHES RAPID CURING	AR	AR							OZ
	32	A	70906156-001	V	CLAMP CBL 3/8	7	7							EA
	33	A	03510002-002	V	CLAMP LOOP 1/8 ID	1	1							EA
	34	A	03020003-002	V	WASH LCK 4	16	16							EA
	35	TK	60128564-002	A	CA GND MULTI-PT	X	X							EA
	36	TK	60131564-002	A	KIT TB FAULT GND	X	X							EA
	37	A	03910263-001	V	LABEL CAUT PS U/L	1	1							EA
	38	A	03910263-002	V	LABEL CAUT PS CSA	1	1							EA
	39	A	02760164-001	M	PLSTC EXTR WHT	11.0	11.0							IN
	40	A	03020065-003	V	WASH FLAT STEEL 6	8	8							EA
•	41	TK	60128564-001	A	CA GND MULTI-PT	X	X							EA

Honeywell
HONEYWELL INFORMATION SYSTEMS
LOC. BILLERICA, MASSACHUSETTS, USA.

UM = UNIT OF MEASURE
EA = EACH, IN = INCHES, CM = CENTIMETER, OZ = OUNCE, G = GRAMS

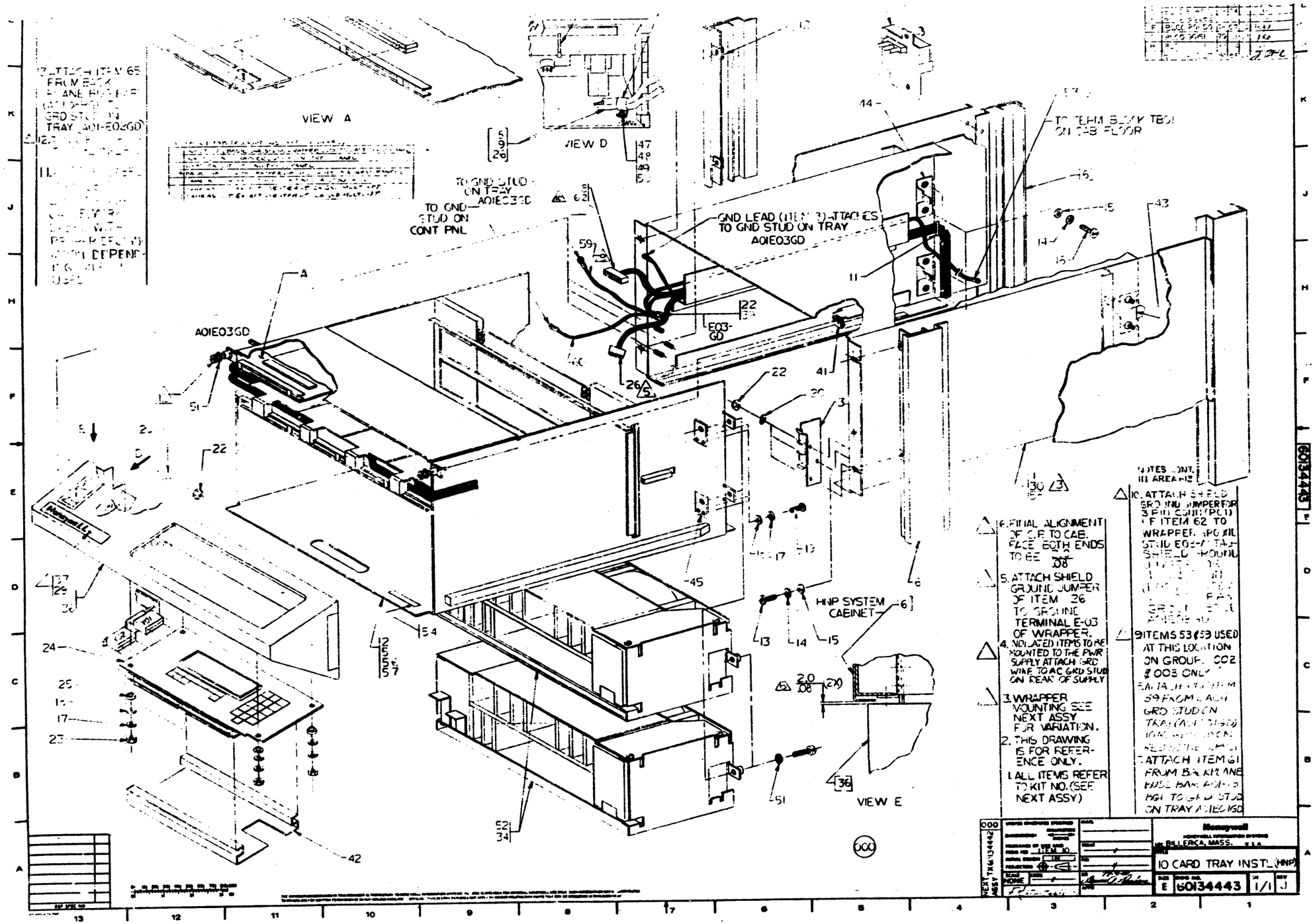
•=ITEMS CHANGED SINCE REV N

TITLE: TRAY ASSY (10 CARD)

SIZE	P.L. NO.	SHEET	REV.
TD	60132152	3F	R

DOES A DOCUMENT REVISION STATUS SHEET EXIST? NO

S = SUBSTITUTE PARTS



•	ITEM NO.	P C	IDENTIFICATION NO.	S C	DRAWING TITLE	ASSEMBLY QUANTITY 001	002	003	004	005	006	007	008	U M
	1	TE	60128212-002	A	WRPR PAB 10 CD	X	X	-	-	-	-	-	-	EA
	2	TD	60128308-007		TRAY ASST INA	X	-	-	-	-	-	-	-	EA
	3	TJ	60131882-001	A	LATCH ASSY	INTCH	-	-	INTCH	INTCH	-	INTCH	-	EA
	3	T8	60130802-001	A	LATCH ASSY PADDED	1	-	-	1	1	-	1	-	EA
	5	TD	60128308-005	A	TRAY ASSY INA	-	X	-	-	-	-	-	-	EA
	6	TE	60131972-002	A	CAB ASSY MNP SYS	X	X	X	X	X	X	X	-	EA
	7	TD	60134476-001	A	RBN CBL FOLDING ASSY	X	-	-	X	X	-	X	-	EA
	8	TK	60128679-003	A	CA AC CORD 60HZ	X	-	-	X	-	-	-	-	EA
•	10	A	13010007-000	D	MFG TOLERANCES	X	X	X	X	X	X	X	X	--
•	11	A	03510004-001	V	LOOP SL 7-5/16	AR	AR	AR	AR	AR	AR	AR	AR	EA
•	12	A	70901402-001	V	NUT FLC THD TYPE T	X	X	X	X	X	X	X	X	EA
•	13	A	03010140-088	V	SCREW PNS 1032 5/8	4	4	4	4	4	4	4	4	EA
	14	A	03020039-005	V	WASH LCK STEEL 10	12	12	12	12	12	12	12	-	EA
	15	A	03020038-005	V	WASH FLAT STEEL 10	12	12	12	12	12	12	12	-	EA
	16	A	03010002-050	V	SCREW PNS 1024 1/2	8	8	8	8	8	8	8	-	EA
	17	A	03020003-003	V	WASH LCK HELSPG 6	12	12	12	12	12	12	12	-	EA

Honeywell
HONEYWELL INFORMATION SYSTEMS
LOC. BILLERICA, MASSACHUSETTS, USA.

UM = UNIT OF MEASURE
EA = EACH IN = INCHES
CM = CENTIMETER OZ = OUNCE
G = GRAMS

**ITEMS CHANGED SINCE REV U

TITLE: KIT 10 CU TRAY INSTL

SIZE TX | P.L. NO. 60134442 | SHEET 1/9 | REV. V

DOES A DOCUMENT REVISION STATUS SHEET EXIST? NO

S = SUBSTITUTE PARTS

•	ITEM NO.	P C	IDENTIFICATION NO.	S C	DRAWING TITLE	ASSEMBLY QUANTITY 001	002	003	004	005	006	007	008	U M
	18	A	03020045-003	V	WASH FLAT STEEL 6	12	12	12	12	12	12	12	-	EA
•	19	A	03010066-024	V	SCREW PNS 632 1/2	8	8	8	8	8	8	8	8	EA
	20	A	03020001-050	V	WASH FLAT STEEL 8	6	-	-	6	6	-	6	-	EA
	21	E	60134443-000	D	10 CARD TRAY INSTL	X	X	X	X	X	X	X	-	--
•	22	A	03030002-004	V	NUT LCK HEX 832	7	1	1	7	7	1	7	1	EA
	23	A	03030001-004	V	NUT HEX STL 832	4	-	-	4	4	-	4	-	EA
	24	TD	60129993-001		KEYBOARD ASSY MNP	X	-	-	X	X	-	X	-	EA
	25	A	03020010-001	V	WASH SHOR FIBER 6	4	-	-	4	4	-	4	-	EA
	26	TK	60128790-001	A	CA PDU CONTROL	1	-	-	1	-	-	-	-	EA
•	27	C	60128157-009	A	INPUT ASSY AC	INTCH	INTCH	INTCH	INTCH	INTCH	INTCH	INTCH	INTCH	EA
•	27	TC	60129892-010	A	INPUT ASSY AC	X	X	X	X	X	X	X	X	EA
•	28	C	60128157-004	A	INPUT ASSY AC	INTCH	INTCH	INTCH	INTCH	INTCH	INTCH	INTCH	INTCH	EA
•	28	TC	60129892-003	A	INPUT ASSY AC	X	X	X	X	X	X	X	X	EA
	29	C	60134551-001	P	PLATE LOGO HONEYWELL	-	-	-	X	X	-	X	-	EA
•	30	TE	60128212-004	A	WRPR PAB 10 CD	-	-	X	-	-	X	-	X	EA
•	34	TD	60130010-005	A	PS ASSY 4150 50HZ	X	X	X	X	X	X	X	X	EA

Honeywell
HONEYWELL INFORMATION SYSTEMS
LOC. BILLERICA, MASSACHUSETTS, USA.

UM = UNIT OF MEASURE
EA = EACH IN = INCHES
CM = CENTIMETER OZ = OUNCE
G = GRAMS

**ITEMS CHANGED SINCE REV U

TITLE: KIT 10 CU TRAY INSTL

SIZE TX | P.L. NO. 60134442 | SHEET 2 | REV. V

DOES A DOCUMENT REVISION STATUS SHEET EXIST? NO

S = SUBSTITUTE PARTS

•	ITEM NO.	P C	IDENTIFICATION NO.	S C	DRAWING TITLE	ASSEMBLY QUANTITY 001	002	003	004	005	006	007	008	U M
	36	TD	60129856-006	A	PNL ASSY DRESS	X	-	-	INTCH	INTCH	-	INTCH	-	EA
	36	TD	60129856-008	A	PNL ASSY DRESS	-	-	-	INTCH	INTCH	-	INTCH	-	EA
	36	TD	60132337-002	A	PNL ASSY DRESS	-	-	-	1	1	-	1	-	EA
	37	TC	60134372-001	P	LABEL CII BULL	-	-	-	X	X	-	X	-	EA
•	39	A	03020045-004	V	WASH FLAT STEEL 8	1	1	1	1	1	1	1	1	EA
	41	A	03030012-001	V	NUT SPR STL 1044	2	2	-	-	-	-	-	-	EA
•	41	A	03030012-005	V	NUT SPR STL 1044	-	-	2	2	2	2	2	2	EA
	42	C	60133936-001	V	COVER KYBD LOGIC BD	1	-	-	1	1	-	1	-	EA
•	43	C	60134286-001	P	BRKT TIE	2	2	2	2	2	2	2	2	EA
•	44	C	60134286-002	P	BRKT TIE	2	2	2	2	2	2	2	2	EA
•	45	B	60134287-001	V	NUT PLATE	4	4	4	4	4	4	4	4	EA
	46	A	03510002-007	V	CLAMP LOOP 5/8 ID	1	-	-	1	1	-	1	-	EA
	47	A	03010002-010	V	SCREW PNS 632 5/8	1	-	-	1	1	-	1	-	EA
	48	A	03020045-003	V	WASH FLAT STEEL 6	1	-	-	1	1	-	1	-	EA
	49	A	03020003-003	V	WASH LCK HELSPG 6	1	-	-	1	1	-	1	-	EA
	50	A	03030001-004	V	NUT HEX STL 632	1	-	-	1	1	-	1	-	EA

Honeywell
HONEYWELL INFORMATION SYSTEMS
LOC. BILLERICA, MASSACHUSETTS, USA.

UM = UNIT OF MEASURE
EA = EACH IN = INCHES
CM = CENTIMETER OZ = OUNCE
G = GRAMS

**ITEMS CHANGED SINCE REV U

TITLE: KIT 10 CU TRAY INSTL

SIZE TX | P.L. NO. 60134442 | SHEET 5 | REV. V

DOES A DOCUMENT REVISION STATUS SHEET EXIST? NO

S = SUBSTITUTE PARTS

•	ITEM NO.	P C	IDENTIFICATION NO.	S C	DRAWING TITLE	ASSEMBLY QUANTITY 001	002	003	004	005	006	007	008	U M
•	51	A	03020004-005	V	WASH LCK EX-TTH 10	X	X	X	X	X	X	X	42	EA
•	52	TJ	60130011-005	A	PS ASSY M150 60HZ	X	X	X	X	X	X	X	X	EA
•	53	T8	60131128-009	A	JMPR ASSY 10 AWG	-	1	1	-	-	1	-	1	EA
•	54	A	60126281-XXX	A	TECH ID TAG MARKING	X	X	X	X	X	X	X	X	EA
	56	TD	60132152-002	A	TRAY ASSY (10 CARD)	-	-	-	X	X	-	X	-	EA
•	57	TD	60132152-001	A	TRAY ASSY (10 CARD)	-	-	X	-	-	X	-	X	EA
	58	TE	60128212-006	A	WRPR PAB 10 CD	-	-	-	X	X	-	X	-	EA
•	59	T8	60131128-007	A	JMPR ASSY 10 AWG	2	3	3	2	2	3	2	3	EA
	60	T9	60131129-006	A	JMPR ASSY FLAT BRAID	1	-	-	1	1	-	1	-	EA
•	61	TK	60128564-002	A	CA GND MULTI-PT	1	1	1	1	1	1	1	1	EA
	62	TK	60135276-001	A	CA 15/30A 60HZ IN/UT	-	-	-	-	X	-	X	-	EA
•	63	A	70982152-003	V	CABLE MARKER 2 INCH	4	6	4	4	4	4	4	4	EA
•	65	TK	60128564-001	A	CA GND MULTI-PT	-	-	-	-	-	1	1	1	EA
•	66	A	03010227-030	V	SCREWTPNT 1032 5/8	-	-	-	-	-	-	-	8	EA
•	67	E	60135645	D	10 CARD TRAY INSTL	-	-	-	-	-	-	-	X	EA
•	68	A	02740164-001	M	PLSTC EXTN ANT	-	-	-	-	-	-	-	40	IN

Honeywell
HONEYWELL INFORMATION SYSTEMS
LOC. BILLERICA, MASSACHUSETTS, USA.

UM = UNIT OF MEASURE
EA = EACH IN = INCHES
CM = CENTIMETER OZ = OUNCE
G = GRAMS

**ITEMS CHANGED SINCE REV U

TITLE: KIT 10 CU TRAY INSTL

SIZE TX | P.L. NO. 60134442 | SHEET 6 | REV. V

DOES A DOCUMENT REVISION STATUS SHEET EXIST? NO

S = SUBSTITUTE PARTS

*	ITEM NO	P C	IDENTIFICATION NO	S C	DRAWING TITLE	ASSEMBLY QUANTITY 001	002	003	004	005	006	007	008	U M
*	69	J	60140769-000	C	INSTL BLKHD CAB MNP	-	-	-	-	-	-	-	X	EA
*	70		60143377-XXX	A	MNP SYS CAB ASSY	-	-	-	-	-	-	-	X	EA
*	71	A	03020089-005	V	WASH LCK EX-TTH 110	-	-	-	-	-	-	-	4	EA

Honeywell
HONEYWELL INFORMATION SYSTEMS
LOC. BILLERICA, MASSACHUSETTS, USA.

UM = UNIT OF MEASURE
EA = EACH IN = INCHES
CM = CENTIMETER OZ = OUNCE
G = GRAMS
*=ITEMS CHANGED SINCE REV U

TITLE: KIT 10 CD TRAY INSTL
SIZE: TX | P.L. NO.: 60136462 | SHEET: 5 | REV.: V

DOES A DOCUMENT REVISION STATUS SHEET EXIST? YU

S = SUBSTITUTE PARTS

*	ITEM NO	P C	IDENTIFICATION NO.	C	DRAWING TITLE	009	U M
*	3	TD	60131882-001	A	LATCH ASSY	INTCH	EA
*	3	TB	60138802-001	A	LATCH ASSY PADDED	1	EA
*	7	TD	60134476-001	A	RSW CBL FOLDING ASSY	X	EA
*	10	A	13010007-000	D	MFG TOLERANCES	X	--
*	11	A	03510004-001	V	LOOP SL 7-5/16	AR	EA
*	12	A	70901402-001	V	NUT FLC THD TYPE T	X	EA
*	13	A	03010140-088	V	SCREW PNS 1032 5/8	4	EA
*	17	A	03020003-003	V	WASH LCK HELSPR 6	4	EA
*	18	A	03020045-003	V	WASH FLAT STEEL 6	4	EA
*	19	A	03010006-024	V	SCREW FHS 632 1/2	8	EA
*	20	A	03020001-050	V	WASH FLAT STEEL 8	6	EA
*	22	A	03030002-004	V	NUT LCK HEX 832	7	EA
*	23	A	03030001-004	V	NUT HEX STL 632	4	EA
*	24	TD	60129993-001		KEYBOARD ASSY MNP	X	EA
*	25	A	03020010-001	V	WASH SHDR FIBER 6	4	EA
*	27	C	60128157-009	A	INPUT ASSY AC	INTCH	EA

Honeywell
HONEYWELL INFORMATION SYSTEMS
LOC. BILLERICA, MASSACHUSETTS, USA.

UM = UNIT OF MEASURE
EA = EACH IN = INCHES
CM = CENTIMETER OZ = OUNCE
G = GRAMS
*=ITEMS CHANGED SINCE REV U

TITLE: KIT 10 CD TRAY INSTL
SIZE: TX | P.L. NO.: 60136462 | SHEET: 6 | REV.: V

DOES A DOCUMENT REVISION STATUS SHEET EXIST? YU

S = SUBSTITUTE PARTS

801120

SIZE: TX | P.L. NO.: 60136462 | SHEET: 7 | REV.: V

*	ITEM NO.	P C	IDENTIFICATION NO.	S C	DRAWING TITLE	ASSEMBLY/QUANTITY 009	U M
*	27	TC	60129892-010	A	INPUT ASSY AC	X	EA
*	28	C	60128157-004	A	INPUT ASSY AC	INTCH	EA
*	28	TC	60129892-003	A	INPUT ASSY AC	1	EA
*	29	C	60136551-001	P	PLATE LOGO HONEYWELL	X	EA
*	34	TD	60130010-005	A	PS ASSY 4150 50HZ	X	EA
*	36	TD	60129856-006	A	PNL ASSY DRESS	INTCH	EA
*	36	TD	60129856-008	A	PNL ASSY DRESS	INTCH	EA
*	36	TD	60132537-002	A	PNL ASSY DRESS	1	EA
*	37	TC	60136372-001	P	LABEL CII BULL	X	EA
*	39	A	03020045-004	V	WASH FLAT STEEL 8	1	EA
*	41	A	03030012-005	V	NUT SPR STL 1024	2	EA
*	42	C	60133936-001	V	COVER KYBD LOGIC BD	1	EA
*	43	C	60136288-001	P	BRKT TIE	2	EA
*	44	C	60136288-002	P	BRKT TIE	2	EA
*	45	B	60134287-001	V	NUT PLATE	4	EA
*	46	A	03510002-007	V	CLAMP LOOP 5/8 ID	1	EA

Honeywell
HONEYWELL INFORMATION SYSTEMS
LOC. BILLERICA, MASSACHUSETTS, USA.

UM = UNIT OF MEASURE
EA = EACH IN = INCHES
CM = CENTIMETER OZ = OUNCE
G = GRAMS
*=ITEMS CHANGED SINCE REV U

TITLE: KIT 10 CD TRAY INSTL
SIZE: TX | P.L. NO.: 60136462 | SHEET: 7 | REV.: V

DOES A DOCUMENT REVISION STATUS SHEET EXIST? YU

S = SUBSTITUTE PARTS

801120

SIZE TX | 60134442 | SHEET 8 | REV. V

*	ITEM NO.	PC	IDENTIFICATION NO.	SC	DRAWING TITLE	ASSEMBLY/QUANTITY 009								UM
*	47	A	03010002-010	V	SCREW PNS 632 3/8	1								EA
*	48	A	03020045-003	V	WASH FLAT STEEL 6	1								EA
*	49	A	03020005-003	V	WASH LCK HELSPG 6	1								EA
*	50	A	03030001-004	V	NUT HEX STL 632	1								EA
*	51	A	03020004-005	V	WASH LCK EX-TTH 10	22								EA
*	52	TD	60130011-005	A	PS ASSY 4150 60HZ	X								EA
*	54	A	60126281-XXX	A	TECH ID TAG MARKING	X								EA
*	56	TD	60132152-002	A	TRAY ASSY (10 CARD)	X								EA
*	58	TC	60128212-006	A	WRPR FAB 10 CD	X								EA
*	59	TB	60131128-007	A	JMPR ASSY 10 AWG	2								EA
*	60	TB	60131129-006	A	JMPR ASSY FLAT BRAID	1								EA
*	61	TK	60128564-002	A	CA GND MULTI-PT	1								EA
*	62	TK	60135276-001	A	CA 15/30A 60HZ IN/OUT	X								EA
*	63	A	7098215-003	V	CABLE MARKER 2 INCH	4								EA
*	65	TK	60128564-001	A	CA GND MULTI-PT	1								EA
*	66	A	03010220-030	V	SCHEMTPNT 1032 5/8	8								EA

Honeywell
HONEYWELL INFORMATION SYSTEMS
LGC. BILLERICA, MASSACHUSETTS, USA.

UM = UNIT OF MEASURE
EA = EACH IN = INCHES
CM = CENTIMETER OZ = OUNCE
G = GRAMS

**ITEMS CHANGED SINCE REV U

TITLE: KIT 10 CU TRAY INSTL

SIZE TX | P.L. NO. 60134442 | SHEET 8 | REV. V

DOES A DOCUMENT REVISION STATUS SHEET EXIST? NO

S = SUBSTITUTE PARTS

HONEYWELL CONFIDENTIAL & PROPRIETARY

801120

SIZE TX | 60134442 | SHEET 9 | REV. V

*	ITEM NO.	PC	IDENTIFICATION NO.	SC	DRAWING TITLE	ASSEMBLY/QUANTITY 009								UM
*	67	E	60135045	D	10 CARD TRAY INSTL	X								EA
*	68	A	02740164-001	M	PLSTC EXTR AMT	20								IN
*	69	D	60140769-000	D	INSTL BLKHD CAB HNP	X								EA
*	70		60143377-XXX	A	HNP SYS CAB ASSY	X								EA
*	71	A	03020089-005	V	WASH LCK EX-TTH 310	4								EA

Honeywell
HONEYWELL INFORMATION SYSTEMS
LGC. BILLERICA, MASSACHUSETTS, USA.

UM = UNIT OF MEASURE
EA = EACH IN = INCHES
CM = CENTIMETER OZ = OUNCE
G = GRAMS

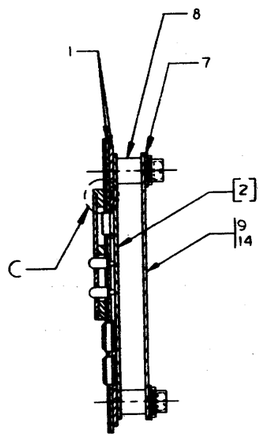
**ITEMS CHANGED SINCE REV U

TITLE: KIT 10 CU TRAY INSTL

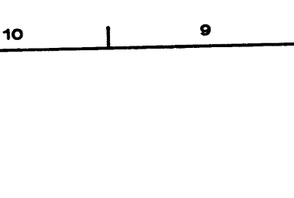
SIZE TX | P.L. NO. 60134442 | SHEET 9F | REV. V

DOES A DOCUMENT REVISION STATUS SHEET EXIST? NO

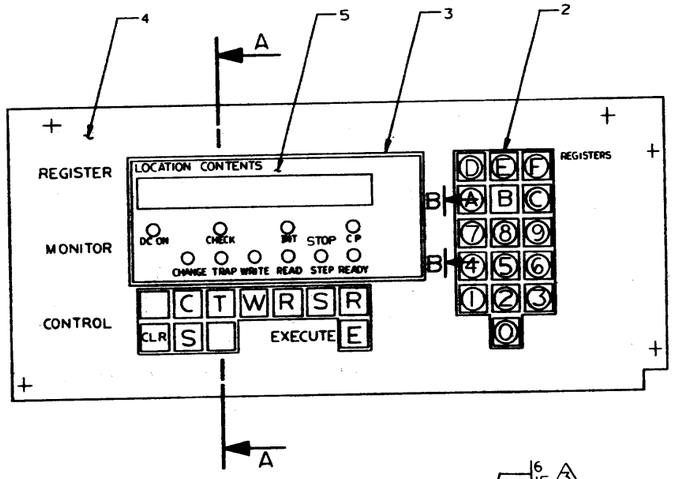
S = SUBSTITUTE PARTS

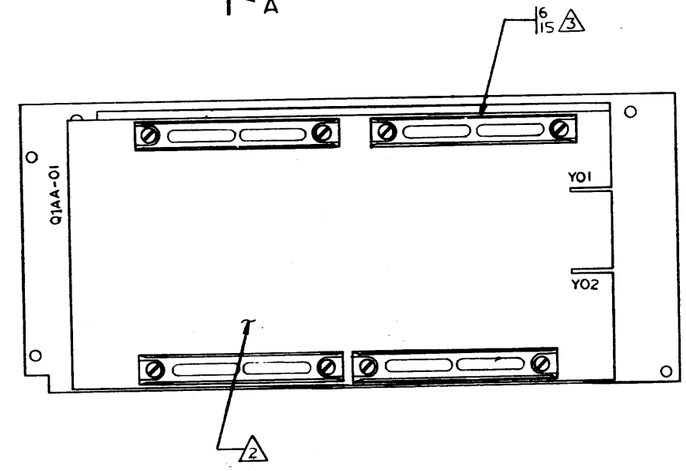


SECTION A-A

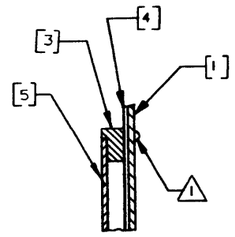


SECTION B-B
(SCALE 2/1)





REAR VIEW



VIEW C
(SCALE 2/1)

REVISIONS						
	REV	AUTHORITY	DATE YR	DATE MO	DATE DAY	SIGNATURE
L1	A	BLCD 67266	76	3	5	FRo
L2	B	BLCD 67296	76	3	12	FRo
L2	C	BLCO 60918	76	11		FRo
L2	D	BLCO 61391	77	1	28	FRo
L2	E	BLCO 61577	77	4	12	FRo
L2	F	BLCO 61339	77	5	27	T. Soares
L2	G	BLC070310	77	9	7	
L2	H	BLC070831	77	10	21	
	J	BLC081178				

△3. TO INSTALL ITEM 6 OR 15 TORQUE SCREWS TO 4±1 INCH/LBS.
△2. COMPONENT SIDE
△1. THERMAL SWAGE ITEM (10 PLACES)

004 003 002 001

NEXT ASSY

UNLESS OTHERWISE SPECIFIED
DIMENSIONS= MILLIMETERS / INCHES
TOLERANCE OF SIZE AND FORM PER
INITIAL DESIGN IN
PROJECTION
SCALE 1/1
CODE
MATL
TREAT.
FIN.
DR L Mango 75 DEC 24
APPD

Honeywell
HONEYWELL INFORMATION SYSTEMS
LOC BILLERICA, MASS. U.S.A.
TITLE KEYBOARD ASSY HNP
SIZE D
DWG NO 60129993
SH 1/1
REV J

60129993

REF SPEC NO

790105

SIZE TD | 60129993 | SHEET 1/ | REV. J

•	ITEM NO.	PC	IDENTIFICATION NO	SC	DRAWING TITLE	ASSEMBLY/QUANTITY 001	002	003	004					UM
	1	TD	60128360-001	A	BEZEL KEYBOARD ASSY	1	1	1	1					EA
	2	C	60129995-001	-	KEYBOARD CONFIG HNP	1	1	1	1					EA
	3	TD	60129845-001	P	FRAME	1	1	1	1					EA
	4	D	60129838-003	A	KEYBD PNL OVERLAY	1	1	1	1					EA
	5	C	60129994-001	-	BACKLIT PANEL HNP	1	1	1	1					EA
•	6	T	60133844-001	A	TOP-STIFF-ASSY	4	4	4	-					EA
	7	T	60128110-001	P	INSULATOR	4	4	4	-					EA
	8	NA	04830325-001	V	CONN PWB 25 PIN	4	4	4	4					EA
	9	T	60130198-002C	A	BX2CP7 ASSY (2.0)	NOINT	-	-	-					EA
	9	T	60130741-001A	A	BX2CP7 ASSY	1	1	-	-					EA
	9	T	60130198-003D	A	BX2CP7 ASSY	-	INTCH	INTCH	INTCH					EA
	10	TB	60128230-001	P	SPACER	1	1	1	1					EA
	11	A	03020003-004	V	WASH LCK HL-SPR 8	1	1	1	1					EA
	12	A	03030001-005	V	NUT PLN HEX 8	1	1	1	1					EA
	13	A	03020001-050	V	WASH FLAT STEEL 8	1	1	1	1					EA
•	14	T	60130741-0028	A	BX2CP7-ASSY	-	-	1	INTCH					Y

Honeywell
HONEYWELL INFORMATION SYSTEMS
LOC. BILLERICA. MASSACHUSETTS. USA.

UM = UNIT OF MEASURE
EA = EACH — IN = INCHES
CM = CENTIMETER — OZ = OUNCE
G = GRAMS

• ITEMS REVISED SINCE REV. H

TITLE: KEYBOARD ASSY HNP

SIZE TD | P.N. NO. 60129993 | SHEET 1/2 | REV. J

DOES A DOCUMENT REVISION STATUS SHEET EXIST? NO

S = SUBSTITUTE PARTS

790105

SIZE TD | 60129993 | SHEET 2 | REV. J

•	ITEM NO.	PC	IDENTIFICATION NO.	SC	DRAWING TITLE	ASSEMBLY/QUANTITY 001	002	003	004					UM
•	14	T	60133406-0018	A	BX2CP7 ASSY	-	-	-	1					EA
	15	T	60133844-001	A	TOP-STIFF-ASSY	-	-	-	4					EA

Honeywell
HONEYWELL INFORMATION SYSTEMS
LOC. BILLERICA. MASSACHUSETTS. USA.

UM = UNIT OF MEASURE
EA = EACH — IN = INCHES
CM = CENTIMETER — OZ = OUNCE
G = GRAMS

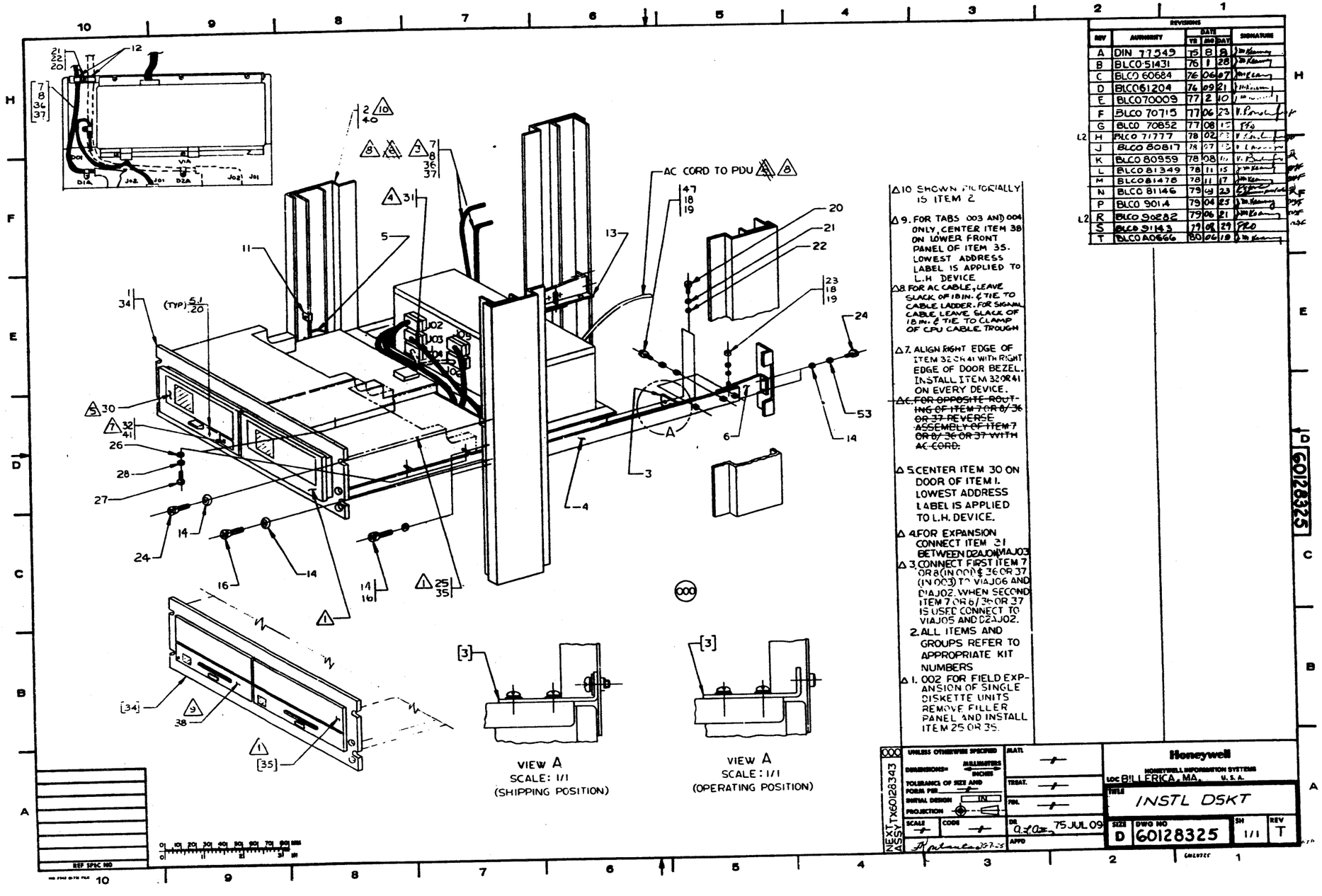
• ITEMS REVISED SINCE REV. H

TITLE: KEYBOARD ASSY HNP

SIZE TD | P.N. NO. 60129993 | SHEET 2F | REV. J

DOES A DOCUMENT REVISION STATUS SHEET EXIST? NO

S = SUBSTITUTE PARTS



REVISIONS					
REV	AUTHORITY	DATE YR	DATE MO	DATE DAY	SIGNATURE
A	DIN 77545	75	8	8	
B	BLCO 51431	76	1	28	
C	BLCO 60684	76	06	07	
D	BLCO 61204	76	09	21	
E	BLCO 70009	77	2	10	
F	BLCO 70715	77	06	23	
G	BLCO 70852	77	08	15	
L2 H	BLCO 71777	78	02		
J	BLCO 80817	78	07		
K	BLCO 80959	78	08		
L	BLCO 81349	78	11	15	
M	BLCO 81478	78	11	17	
N	BLCO 81146	79	03	23	
P	BLCO 90142	79	04	25	
L2 R	BLCO 90282	79	06	21	
S	BLCO 91143	79	08	29	
T	BLCO A0666	80	06	18	

△10 SHOWN PICTORIALLY IS ITEM 2.

△9. FOR TABS 003 AND 004 ONLY, CENTER ITEM 38 ON LOWER FRONT PANEL OF ITEM 35. LOWEST ADDRESS LABEL IS APPLIED TO L.H. DEVICE.

△8 FOR AC CABLE, LEAVE SLACK OF 18 IN. & TIE TO CABLE LADDER. FOR SIGNAL CABLE, LEAVE SLACK OF 18 IN. & TIE TO CLAMP OF CPU CABLE TROUGH

△7. ALIGN RIGHT EDGE OF ITEM 32 OR 41 WITH RIGHT EDGE OF DOOR BEZEL. INSTALL ITEM 32 OR 41 ON EVERY DEVICE.

~~△6. FOR OPPOSITE ROUTING OF ITEM 7 OR 8/36 OR 37 REVERSE ASSEMBLY OF ITEM 7 OR 8/36 OR 37 WITH AC CORD.~~

△5 CENTER ITEM 30 ON DOOR OF ITEM 1. LOWEST ADDRESS LABEL IS APPLIED TO L.H. DEVICE.

△4 FOR EXPANSION CONNECT ITEM 31 BETWEEN D2AJ04 VIAJ03

△3 CONNECT FIRST ITEM 7 OR 8 (IN 001) & 36 OR 37 (IN 003) TO VIAJ06 AND D1AJ02. WHEN SECOND ITEM 7 OR 8/36 OR 37 IS USED CONNECT TO VIAJ05 AND D2AJ02.

2. ALL ITEMS AND GROUPS REFER TO APPROPRIATE KIT NUMBERS

△1. 002 FOR FIELD EXPANSION OF SINGLE DISKETTE UNITS REMOVE FILLER PANEL AND INSTALL ITEM 25 OR 35.

UNLESS OTHERWISE SPECIFIED	MATL	Honeywell	
DIMENSIONS= MILLIMETERS / INCHES	TREAT.	HONEYWELL INFORMATION SYSTEMS LOC BILLERICA, MA. U.S.A.	
TOLERANCE OF SIZE AND FORM PER	FIN.	TITLE INSTL DSKT	
INITIAL DESIGN IN		SIZE D	DWG NO 60128325
PROJECTION		SCALE	CODE
DR 75 JUL 09		SH 1/1	REV T
APPD			

NEXT ASSY TX60128343

60128325

05/83
FN01-03C

HONEYWELL CONFIDENTIAL & PROPRIETARY

801118 | SIZE TX | 60128343 | SHEET 1/3 | REV. X

•	ITEM NO.	PC	IDENTIFICATION NO.	SC	DRAWING TITLE	ASSEMBLY/QUANTITY 001	002	003	004	005	006			UM
	1	TD	60126287-XXX	A	DSKT ASSY	X	-	-	-	X	-			EA
	2	TE	60128315-XXX	A	CAB ASSY NML SYS	X	-	X	-	-	-			EA
	3	TB	60128320-001	V	BRKT SHPNG DSKT	2	-	2	-	2	-			EA
	4	TD	60128307-001	A	BRKT FAB SIDE	1	-	1	-	-	-			EA
	5	TD	60128307-002	A	BRKT FAB SIDE	1	-	1	-	-	-			EA
	6	TC	60128301-002	P	BRKT SPRT	1	-	1	-	-	-			EA
	7	TK	60128523-001	A	CA DSKT 6 FT	X	X	-	-	X	X			EA
	8	TK	60128523-002	A	CA DSKT 12 FT	X	X	-	-	X	X			EA
	11	A	70901402-001	V	NUT FLC THD TYPE T	2	-	2	-	-	-			EA
	12	A	03510002-004	V	CLAMP LOOP 3/8 ID	2	-	2	-	-	-			EA
	13	TC	60128301-001	P	BRKT SPRT	1	-	1	-	-	-			EA
	14	A	03020038-005	V	WASH FLAT STEEL 10	12	-	12	-	8	-			EA
	16	A	03010140-069	V	SCREW PNS 1024 5/8	6	-	6	-	6	-			EA
	18	A	03020003-005	V	WASH LCK HELSPG 10	8	-	8	-	-	-			EA
	19	A	03020001-051	V	WASH FLAT STEEL 10	8	-	8	-	-	-			EA
	20	A	03010002-051	V	SCREW PNS 832 1/2	5	-	5	-	4	-			EA

Honeywell
HONEYWELL INFORMATION SYSTEMS
LOC. BILLERICA, MASSACHUSETTS, USA.

UM = UNIT OF MEASURE
EA = EACH, IN = INCHES, CM = CENTIMETER, OZ = OUNCE, G = GRAMS

**ITEMS CHANGED SINCE REV M

TITLE: KIT DSKT INSTL
SIZE TX | P.L. NO. 60128343 | SHEET 1/3 | REV. X

DOES A DOCUMENT REVISION STATUS SHEET EXIST? YES

S = SUBSTITUTE PARTS

HONEYWELL CONFIDENTIAL & PROPRIETARY

801118 | SIZE TX | 60128343 | SHEET 2 | REV. X

•	ITEM NO.	PC	IDENTIFICATION NO.	SC	DRAWING TITLE	ASSEMBLY/QUANTITY 001	002	003	004	005	006			UM
	21	A	03020003-004	V	WASH LCK HELSPG 8	5	-	5	-	4	-			EA
	22	A	03020001-050	V	WASH FLAT STEEL 8	5	-	5	-	4	-			EA
	23	A	03030001-006	V	NUT HEX STL 1024	2	-	2	-	2	-			EA
	24	A	03010140-088	V	SCREW PNS 1032 5/8	6	-	6	-	2	-			EA
	25		47217760-XXX	V	DISKETTE DRIVE	-	X	-	-	-	X			EA
	26	A	03020001-048	V	WASH FLAT STEEL 6	-	6	-	6	-	6			EA
	27	A	03010002-041	V	SCREW PNS 440 1/2	-	6	-	6	-	6			EA
	28	A	03020003-002	V	WASH LCK HELSPG 6	-	6	-	6	-	6			EA
	29	D	60128325-000	D	INSTL DSKT	X	X	X	X	-	-			--
	30		03910236-XXX	V	LABEL DISKETTE	X	X	-	-	X	X			EA
	31	TK	60128522-XXX	A	CA DISKETTE PWR	-	1	-	1	-	1			--
	32	A	03910250-001	V	LABEL CAUT PS UB	X	X	-	-	X	X			EA
	34	TD	60135350-XXX	A	DSKT ASSY	-	-	X	-	-	-			EA
	35	A	60135348-XXX	D	DISKETTE DRIVE D.S.	-	-	-	X	-	-			--
	36	TK	60136926-001	A	CA DSKT LOG-PDR	-	-	X	X	-	-			EA
	37	TK	60136926-002	A	CA DSKT LOG-PDR	-	-	X	X	-	-			EA

Honeywell
HONEYWELL INFORMATION SYSTEMS
LOC. BILLERICA, MASSACHUSETTS, USA.

UM = UNIT OF MEASURE
EA = EACH, IN = INCHES, CM = CENTIMETER, OZ = OUNCE, G = GRAMS

**ITEMS CHANGED SINCE REV M

TITLE: KIT DSKT INSTL
SIZE TX | P.L. NO. 60128343 | SHEET 2 | REV. X

DOES A DOCUMENT REVISION STATUS SHEET EXIST? YES

S = SUBSTITUTE PARTS

HONEYWELL CONFIDENTIAL & PROPRIETARY

801118 | SIZE TX | 60128343 | SHEET 3F | REV. X

•	ITEM NO.	PC	IDENTIFICATION NO.	SC	DRAWING TITLE	ASSEMBLY/QUANTITY 001	002	003	004	005	006			UM
	38	A	03910273-XXX	V	NAMEPLATE DBL DISK	-	-	X	X	-	-			EA
	39	D	60135932-000	D	INSTL CAB HD NML	X	-	X	-	-	-			--
	40	TD	60135778-XXX	A	CAB ASSY HD SYS	X	-	X	-	-	-			EA
	41	A	03910250-002	V	LABEL CAUT PS FR	X	X	-	-	X	X			EA
	42	D	60139775-000	D	INSTL CAB INTMD HNP	-	-	-	-	-	X			EA
	43	TD	60139678-001	A	BRKT FAB DSKT	-	-	-	-	1	-			EA
	44	TD	60139678-002	A	BRKT FAB DSKT	-	-	-	-	1	-			EA
	45	D	60139773-000	D	INSTL DSKT HNP	-	-	-	-	X	X			EA
	46	A	03510004-006	V	LOOP SL 5=1/2	-	-	-	-	1	-			EA
	47	A	03010002-059	V	SCREW PNS 1024 1/2	6	-	6	-	-	-			EA
	49	A	03010220-030	V	SCHEMTPNT 1032 5/8	-	-	-	-	4	-			EA
	50	A	03020004-005	V	WASH LCK EX-TTH 10	-	-	-	-	6	-			EA
	51	A	03020004-002	V	WASH LCK EX-TTH 6	-	-	-	-	6	-			EA
	52	D	60140769-000	D	INSTL BLKHD CAB HNP	-	-	-	-	X	-			EA
	53	A	03020039-005	V	WASH LCK STEEL 10	4	-	4	-	-	-			EA
•	54	A	02740164-001	M	PLSTC EXTR AMT	-	-	-	-	36	36			IN

Honeywell
HONEYWELL INFORMATION SYSTEMS
LOC. BILLERICA, MASSACHUSETTS, USA.

UM = UNIT OF MEASURE
EA = EACH, IN = INCHES, CM = CENTIMETER, OZ = OUNCE, G = GRAMS

**ITEMS CHANGED SINCE REV M

TITLE: KIT DSKT INSTL
SIZE TX | P.L. NO. 60128343 | SHEET 3F | REV. X

DOES A DOCUMENT REVISION STATUS SHEET EXIST? YES

S = SUBSTITUTE PARTS

*	ITEM NO	P C	IDENTIFICATION NO.	S C	DRAWING TITLE	ASSEMBLY/QUANTITY 001	002	003	004	005	006	007	008	U M
	1	TJ	60132031-007	A	PDU ASSY 50HZ	-	-	-	-	-	-	X	-	EA
	1	TJ	60132031-XXX	A	PDU ASSY NML 50 HZ	X	-	-	-	-	-	-	-	EA
	2	TJ	60132032-XXX	D	NML 50HZ PDU ASSY	X	-	-	-	-	-	-	-	EA
	3	TJ	60131567-009	A	PDU ASSY 50HZ	-	-	X	-	-	-	-	-	EA
	5	TJ	60131907-XXX	A	PDU ASSY 60 HZ	-	X	-	-	-	-	-	-	EA
*	4	TJ	60131907-010	A	PDU ASSY 60HZ	-	-	-	X	-	-	-	-	EA
	5	TK	60131902-003	A	KIT PLD	-	-	-	-	X	-	-	-	EA
	5	TJ	60131902-004		PDU ASSY 50HZ	-	-	-	-	X	-	-	-	EA
	5	TJ	60131902-XXX	A	PDU ASSY 50 HZ	-	X	-	-	-	-	-	-	EA
	6	TJ	60131905-005	A	PDU ASSY 60HZ	-	-	-	-	-	X	-	-	EA
	6	TJ	60131905-XXX	A	PDU ASSY 30A 60 HZ	-	X	-	-	-	-	-	-	EA
	7	TE	60128315-XXX	A	CAB ASSY NML SYS	-	X	-	-	-	-	-	-	EA
	8	A	70901002-001	V	NUT FLC THD 1032	X	X	8	8	8	8	8	X	EA
	9	A	03010015-023	V	SCREW CAX 1032 3/8	2	-	2	-	-	-	2	2	EA
	10	A	03020001-051	V	WASH FLAT STEEL 10	-	-	-	-	-	-	2	-	EA
	11	A	03020039-005	V	WASH LCK HELSPG 10	-	-	-	-	-	-	2	-	EA

Honeywell
HONEYWELL INFORMATION SYSTEMS
LOC. BILLERICA, MASSACHUSETTS, USA.

UM = UNIT OF MEASURE
EA = EACH IN = INCHES
CM = CENTIMETER OZ = OUNCE
G = GRAMS

*=ITEMS CHANGED SINCE REV V

TITLE: KIT PDU
SIZE: TX | P.L.NO.: 60133610 | SHEET: 1/6 | REV.: A

DOES A DOCUMENT REVISION STATUS SHEET EXIST? YES

S = SUBSTITUTE PARTS

*	ITEM NO.	P C	IDENTIFICATION NO.	S C	DRAWING TITLE	ASSEMBLY/QUANTITY 001	002	003	004	005	006	007	008	U M
	11	A	03020039-005	V	WASH LCK STEEL 10	2	-	-	-	-	-	-	2	EA
	12	A	03020038-005	V	WASH FLAT STEEL 10	6	6	6	6	6	6	6	6	EA
	13	T3	60141129-007	A	JMPR ASSY FLAT BRAID	-	-	-	-	-	1	-	-	EA
	14	A	03010140-088	V	SCREW PNS 1032 5/8	4	4	-	-	-	-	-	4	EA
	16	A	03010155-026	V	SCREW PHX 1032 1/2	-	-	4	4	4	4	4	-	EA
	15	D	60133611-000	D	INSTL PDU NML	X	X	X	X	X	X	X	X	--
	16	T3	60131129-004	A	JMPR ASSY FLAT BRAID	-	1	-	-	-	-	1	1	EA
	17	T3	60131129-009	A	JMPR ASSY FLAT BRAID	1	-	-	1	1	-	-	-	EA
	18	TE	60128315-001	A	CAB ASSY NML SYS	-	X	X	-	X	-	-	-	EA
	19	TE	60128315-003	A	CAB ASSY NML SYS	-	X	X	-	X	-	-	-	EA
	20	TE	60128315-004	A	CAB ASSY NML SYS	-	X	X	X	X	-	-	-	EA
	21	TD	60132459-XXX	D	HNP 60HZ PDU ASSY	-	-	-	-	-	-	-	X	EA
	22	D	60131973-000	D	INSTL CAB NML HNP	-	-	-	-	-	-	-	X	--
	23	TE	60128315-005	A	CAB ASSY NML SYS	X	X	X	X	X	-	-	-	EA
	24	TK	60128679-003	A	CA PWR AC CORD 60HZ	-	X	-	-	-	-	-	X	EA
	25	TK	60128681-002	A	CA AC CORD 50HZ	X	X	-	-	-	-	-	X	EA

Honeywell
HONEYWELL INFORMATION SYSTEMS
LOC. BILLERICA, MASSACHUSETTS, USA.

UM = UNIT OF MEASURE
EA = EACH IN = INCHES
CM = CENTIMETER OZ = OUNCE
G = GRAMS

*=ITEMS CHANGED SINCE REV V

TITLE: KIT PDU
SIZE: TX | P.L. NO.: 60133610 | SHEET: 2 | REV.: A

DOES A DOCUMENT REVISION STATUS SHEET EXIST? YES

S = SUBSTITUTE PARTS

HONEYWELL CONFIDENTIAL & PROPRIETARY

SIZE: TX | 60133610 | SHEET: 3 | REV.: A

*	ITEM NO	P C	IDENTIFICATION NO.	S C	DRAWING TITLE	ASSEMBLY/QUANTITY 001	002	003	004	005	006	007	008	U M
	26		60135028-XXX	D	RATING TAG MARKING	1	1	-	-	-	-	-	1	--
	27	A	03070036-001	V	PIN RDHM 2 .250	4	4	-	-	-	-	-	4	EA
	28	A	60126281-XXX	A	TECH IO TAG MARKING	1	1	-	-	-	-	-	-	EA
	29	A	60135401-001	V	WARNING TAG	-	-	-	-	-	-	-	2	EA
	30	A	03510004-002	V	FASNR NYLON 3-5/8	-	-	-	-	-	-	-	4	EA
	31	TE	60131972-003	A	CAB ASSY HNP SYS	-	-	-	-	-	-	-	X	EA
	32	T4	60131129-001	A	JMPR ASSY FLAT BRAID	-	-	1	-	-	-	-	1	EA
	33	TD	60135778-001	A	CAB ASSY HD SYS	-	X	-	-	-	-	-	-	EA
	34	D	60135982-000	D	INSTL HD CAB NML	-	X	-	-	-	-	-	-	--
	35	TD	60135778-003	A	CAB ASSY HD SYS	-	X	-	-	-	-	-	-	EA
	36	D	60135778-002	A	CAB ASSY HD SYS	-	X	-	-	-	-	-	-	EA
	37	TD	60135778-004	A	CAB ASSY HD SYS	-	X	-	-	-	-	-	-	EA
*	49	D	60143405	D	INSTL PKG SYS 60°	-	X	X	X	-	X	-	-	--
*	50	TD	60143537-XXX	A	CAB ASSY NO 2	-	X	X	X	-	X	-	-	EA
*	51	TD	60143536-XXX	A	CAB ASSY NO 1	-	X	X	X	-	X	-	-	EA
*	52	TD	60143538-XXX	A	CAB ASSY NO 3	-	X	X	X	-	X	-	-	EA

Honeywell
HONEYWELL INFORMATION SYSTEMS
LOC. BILLERICA, MASSACHUSETTS, USA.

UM = UNIT OF MEASURE
EA = EACH IN = INCHES
CM = CENTIMETER OZ = OUNCE
G = GRAMS

*=ITEMS CHANGED SINCE REV V

TITLE: KIT PDU
SIZE: TX | P.L. NO.: 60133610 | SHEET: 3 | REV.: A

DOES A DOCUMENT REVISION STATUS SHEET EXIST? YES

S = SUBSTITUTE PARTS

HONEYWELL CONFIDENTIAL & PROPRIETARY

SIZE: TX | 60133610 | SHEET: 4 | REV.: A

*	ITEM NO.	P C	IDENTIFICATION NO.	S C	DRAWING TITLE	ASSEMBLY/QUANTITY 009	010	011						U M
	1	TJ	60132031-XXX	A	PDU ASSY NML 50 HZ	X	X	-						EA
	2	TJ	60132032-XXX	D	NML 50HZ PDU ASSY	X	X	-						EA
	8	A	70901002-001	V	NUT FLC THD 1032	X	X	X						EA
*	9	A	03010015-023	V	SCREW CAX 1032 3/8	2	-	-						EA
	11	A	03020039-005	V	WASH LCK STEEL 10	2	2	2						EA
	12	A	03020038-005	V	WASH FLAT STEEL 10	6	6	6						EA
	14	A	03010140-088	V	SCREW PNS 1032 5/8	4	4	4						EA
	15	D	60133611-000	D	INSTL PDU NML	X	X	X						--
	16	T3	60131129-004	A	JMPR ASSY FLAT BRAID	1	1	1						EA
	21	TD	60132459-XXX	D	HNP 60HZ PDU ASSY	-	-	X						EA
	24	TK	60128679-003	A	CA PWR AC CORD 60HZ	X	X	X						EA
	25	TK	60128681-002	A	CA AC CORD 50HZ	X	X	X						EA
	26		60135028-XXX	D	RATING TAG MARKING	1	1	1						--
	27	A	03070036-001	V	PIN RDHM 2 .250	4	4	4						EA
	28	A	60126281-XXX	A	TECH IO TAG MARKING	1	1	-						EA
	29	A	60135401-001	V	WARNING TAG	-	-	2						EA

Honeywell
HONEYWELL INFORMATION SYSTEMS
LOC. BILLERICA, MASSACHUSETTS, USA.

UM = UNIT OF MEASURE
EA = EACH IN = INCHES
CM = CENTIMETER OZ = OUNCE
G = GRAMS

*=ITEMS CHANGED SINCE REV V

TITLE: KIT PDU
SIZE: TX | P.L. NO.: 60133610 | SHEET: 4 | REV.: A

DOES A DOCUMENT REVISION STATUS SHEET EXIST? YES

S = SUBSTITUTE PARTS

810714

SIZE		SHEET	REV.
TX	60133610	5	A

*	ITEM NO.	P C	IDENTIFICATION NO.	S C	DRAWING TITLE	ASSEMBLY/QUANTITY 009	010	011						U M
	30	A	03510004-002	V	FASNR NYLON 3-5/8	-	-	4						EA
	32	TJ	60131129-001	A	JMPR ASSY FLAT BRAID	-	-	1						EA
	33	TJ	60135778-001	A	CAB ASSY MD SYS	X	-	-						EA
	34	D	60135932-000	D	INSTL MD CAB NML	X	X	-						--
	35	TJ	60135778-003	A	CAB ASSY MD SYS	-	X	-						EA
	36	A	03010220-030	V	SCREWTPNT 1032 5/8	-	2	2						EA
	37	D	60139775-000	D	INSTL CAB INTMD MNP	-	-	X						EA
	38	D	60135778-002	A	CAB ASSY MD SYS	X	-	-						EA
	39	D	60139774-001	A	INT MNP SYS CAB ASSY	-	-	X						EA
	40	TJ	60135778-004	A	CAB ASSY MD SYS	-	X	-						EA
	41		60143377-XXX	A	MNP SYS CAB ASSY	-	-	X						EA
	42	D	60140769-000	D	INSTL BLKMD CAB MNP	-	-	X						EA
	43	TJ	60140968-XXX	A	PDU ASSY DUAL CSS 50	X	X	-						EA
	44	TJ	60140465-XXX	A	PDU ASSY DUAL CSS 60	X	X	-						EA
	45	TJ	60137087-XXX	A	PDU ASSY NML 60HZ	X	X	-						EA
	46	TJ	60137088-XXX	A	PDU ASSY NML 50HZ	X	X	-						EA

Honeywell
HONEYWELL INFORMATION SYSTEMS
LOC. BILLERICA, MASSACHUSETTS, USA.

UM - UNIT OF MEASURE
EA - EACH IN - INCHES
CM - CENTIMETER OZ - OUNCE
G - GRAMS

**ITEMS CHANGED SINCE REV V

TITLE: KIT PDU

SIZE	P.L. NO.	SHEET	REV.
TX	60133610	5	A

DOES A DOCUMENT REVISION STATUS SHEET EXIST? YES

S = SUBSTITUTE PARTS

HONEYWELL CONFIDENTIAL & PROPRIETARY

810714

SIZE		SHEET	REV.
TX	60133610	6F	A

*	ITEM NO	P C	IDENTIFICATION NO	S C	DRAWING TITLE	ASSEMBLY/QUANTITY 009	010	011						U M
	47	TD	60143740	A	CAB ASSY 6/36	-	X	-						EA
	48	D	60143508	D	INSTL PKG SYS 30"	-	X	-						--
*	49	D	60143405	D	INSTL PKG SYS 60"	X	X	X						--
*	50	TD	60143537-XXX	A	CAB ASSY MD 2	X	X	X						EA
*	51	TD	60143536-XXX	A	CAB ASSY MD 1	X	X	X						EA
*	52	TD	60143538-XXX	A	CAB ASSY MD 3	X	X	X						EA

Honeywell
HONEYWELL INFORMATION SYSTEMS
LOC. BILLERICA, MASSACHUSETTS, USA.

UM - UNIT OF MEASURE
EA - EACH IN - INCHES
CM - CENTIMETER OZ - OUNCE
G - GRAMS

**ITEMS CHANGED SINCE REV V

TITLE: KIT PDU

SIZE	P.L. NO.	SHEET	REV.
TX	60133610	6F	A

DOES A DOCUMENT REVISION STATUS SHEET EXIST? YES

S = SUBSTITUTE PARTS

780616

SIZE		SHEET	REV.
TX	60132081	1/F	C

•	ITEM NO.	P C	IDENTIFICATION NO.	S C	DRAWING TITLE	ASSEMBLY/QUANTITY 001	U M
	1	TK	60128735-001	A	CA CONFIGURATOR PNL	X	EA
•	2	A	03010002-039	V	SCREW PH 4	3	EA
•	3	P	03020045-002	V	WASHER FLAT 4	3	EA
•	4	P	03020003-002	V	WASHER LOCK 4 STL	3	EA
	5	P	03510004-001	V	LOOP STRAP FASTENER	1	EA
	6	P	03510002-006	V	CLAMP LOOP	1	EA
	10	D	60131973-000	D	NML CAB INSTL HNP	X	--

Honeywell

HONEYWELL INFORMATION SYSTEMS
LOC. BILLERICA, MASSACHUSETTS, USA.

UM = UNIT OF MEASURE
EA = EACH — IN = INCHES
CM = CENTIMETER — OZ = OUNCE
G = GRAMS

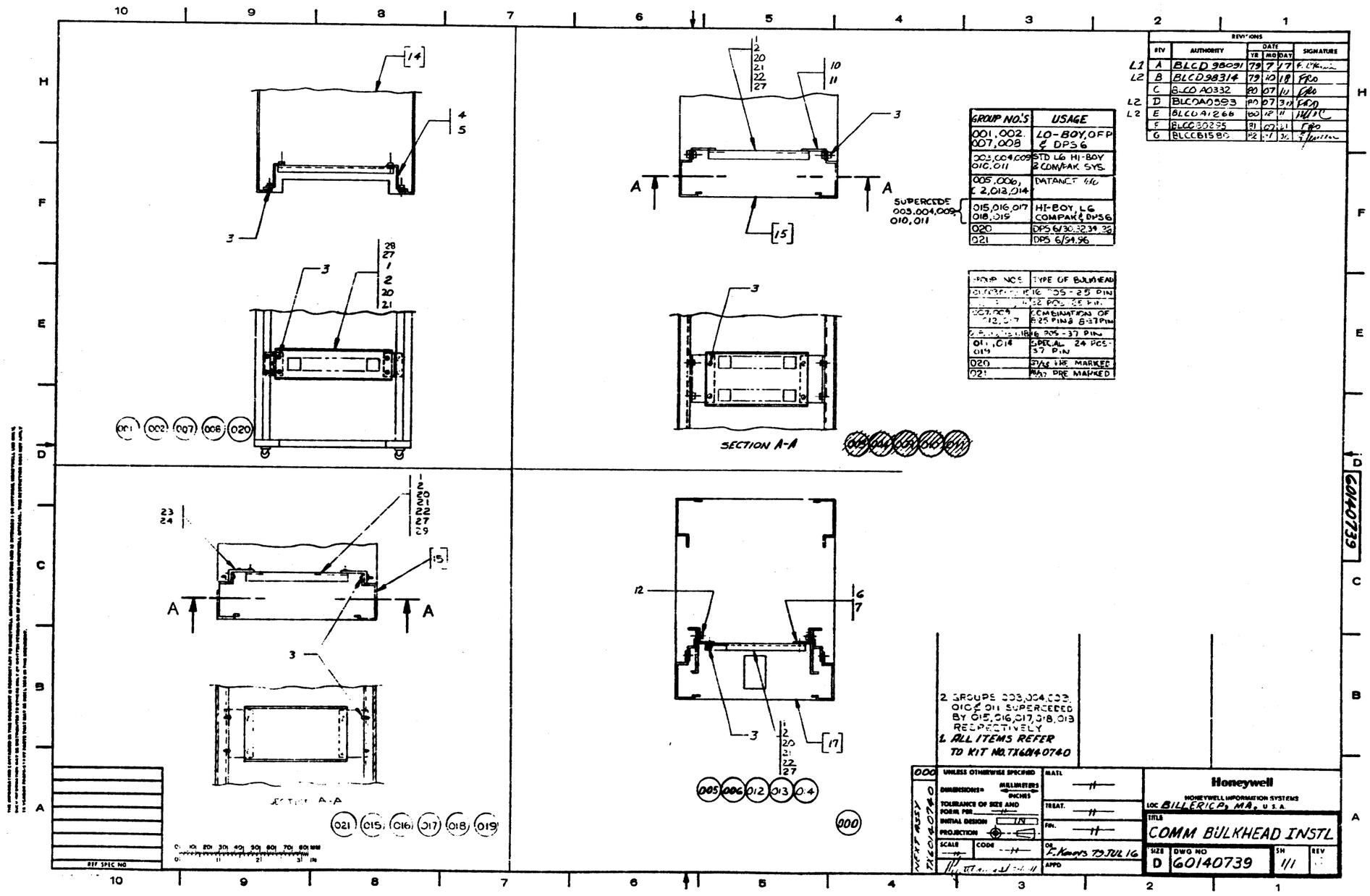
• ITEMS REVISED SINCE REV. B

TITLE: CONFIGURATOR PNL KIT

SIZE	P.L. NO.	SHEET	REV.
TX	60132081	1F	C

DOES A DOCUMENT REVISION STATUS SHEET EXIST? YES

S = SUBSTITUTE PARTS



GROUP NO.'S	USAGE
001, 002, 007, 008	LO-BOY, OFP & DPS 6
003, 004, 009, 010, 011	STD LG HI-BOY & COMPAK SYS
005, 006, & 2, 013, 014	DATANET 6/6
015, 016, 017, 018, 015	HI-BOY, LG COMPAK & DPS 6
020	DPS 6/30, 32, 34, 36
021	DPS 6/34.96

SUPERCEDE 003, 004, 009, 010, 011

GROUP NOS	TYPE OF BULKHEAD
[illegible]	16 PCS - 25 PIN
[illegible]	32 PCS - 25 PIN
007, 009 & 012, 017	COMBINATION OF 8-25 PINS & 8-37 PIN
[illegible]	16 PCS - 37 PIN
013, 014 & 019	SPECIAL 24 PCS - 37 PIN
020	STAR HF MARKED
021	STAR PRE MARKED

REVISIONS					
	REV	AUTHORITY	DATE YR	MO	DAY	SIGNATURE
L1	A	BLCD 98091	79	7	17	[illegible]
L2	B	BLCD98314	79	10	18	FRO
	C	B-CO A0332	80	07	11	FRO
L2	D	BLCOA0593	80	07	30	FRO
L2	E	BLCO A1268	80	12	11	[illegible]
	F	BLCC30295	81	07	31	FRO
	G	BLCCB1580	82	7	30	[illegible]

HONEYWELL CONFIDENTIAL & PROPRIETARY

810708 | SIZE TX 60140740 | SHEET 1/4 | REV. G

•	ITEM NO.	P C	IDENTIFICATION NO.	S C	DRAWING TITLE	ASSEMBLY/QUANTITY 001	002	003	004	005	006	007	008	U M
	1	D	60140737-001	P	SINGLE BLKHD	1	-	1	-	1	-	-	-	EA
	2	D	60140738-001	P	DUAL BLKHD	-	1	-	1	-	1	-	-	EA
	3	A	03010221-001	V	SC/WA THP 1032 1/2	8	8	8	8	4	4	8	8	EA
	4	TC	60140684-001	A	OFP BLKHD BRKT ASSY	2	-	-	-	-	-	2	2	EA
	5	TC	60140684-002	A	OFP BLKHD BRKT ASSY	-	2	-	-	-	-	-	-	EA
	6	TC	60140685-001	A	DN66 BLKHD BRKT ASSY	-	-	-	-	2	-	-	-	EA
	7	TC	60140685-002	A	DN66 BLKHD BRKT ASSY	-	-	-	-	-	2	-	-	EA
	10	TC	60140695-001	A	L6 BLKHD BRKT ASSY	-	-	2	-	-	-	-	-	EA
	11	TC	60140695-002	A	L6 BLKHD BRKT ASSY	-	-	-	2	-	-	-	-	EA
	12	A	03010220-030	V	SCREWTPNT 1032 5/8	-	-	-	-	4	8	-	-	EA
	14	D	60135955	D	INSTL CAB OFP EQUIP	X	X	-	-	-	-	X	X	EA
	15	D	60135932	D	INSTL MD CAB NML	-	-	X	X	-	-	-	-	--
	17	D	60140769	D	INSTL BLKHD CAB HNP	-	-	-	-	X	X	-	-	EA
	18	D	60140739	D	COMM BULKHEAD INSTL	X	X	X	X	X	X	X	X	EA
	19	D	60140063	D	INSTL SHPNG CAGE	-	-	X	X	X	X	-	-	--
	20	D	60142029-001	P	PLATE BLKHD 37/25	-	-	-	-	-	-	1	-	EA

Honeywell
HONEYWELL INFORMATION SYSTEMS
LOC. BILLERICA, MASSACHUSETTS, USA.

UM = UNIT OF MEASURE
EA = EACH IN = INCHES
CM = CENTIMETER OZ = OUNCE
G = GRAMS

**=ITEMS CHANGED SINCE REV F

TITLE: INSTL BLKHD COMM

SIZE TX | P.L. NO. 60140740 | SHEET 1/4 | REV. G

DOES A DOCUMENT REVISION STATUS SHEET EXIST? YES

S = SUBSTITUTE PARTS

HONEYWELL CONFIDENTIAL & PROPRIETARY

810708 | SIZE TX 60140740 | SHEET 2 | REV. G

•	ITEM NO.	P C	IDENTIFICATION NO.	S C	DRAWING TITLE	ASSEMBLY/QUANTITY 001	002	003	004	005	006	007	008	U M
	21	D	60142030-001	P	PLATE BLKHD 37	-	-	-	-	-	-	-	1	EA
	25	TC	60143315-001	A	GUIDE FAB	-	-	-	-	-	4	-	-	EA
	26	A	03020004-005	V	WASH LCK EX-TTH 10	-	-	-	-	-	8	-	-	EA
	27	A	04830369-019	V	CONN LCK FEM W/O HDW	32	64	-	-	32	64	32	32	EA

Honeywell
HONEYWELL INFORMATION SYSTEMS
LOC. BILLERICA, MASSACHUSETTS, USA.

UM = UNIT OF MEASURE
EA = EACH IN = INCHES
CM = CENTIMETER OZ = OUNCE
G = GRAMS

**=ITEMS CHANGED SINCE REV F

TITLE: INSTL BLKHD COMM

SIZE TX | P.L. NO. 60140740 | SHEET 2 | REV. G

DOES A DOCUMENT REVISION STATUS SHEET EXIST? YES

S = SUBSTITUTE PARTS

HONEYWELL CONFIDENTIAL & PROPRIETARY

810708 | SIZE TX 60140740 | SHEET 3 | REV. G

•	ITEM NO.	P C	IDENTIFICATION NO.	S C	DRAWING TITLE	ASSEMBLY/QUANTITY 009	010	011	012	013	014	015	016	U M
	1	D	60140737-001	P	SINGLE BLKHD	-	-	-	-	-	-	1	-	EA
	2	D	60140738-001	P	DUAL BLKHD	-	-	-	-	-	-	-	1	EA
	3	A	03010221-001	V	SC/WA THP 1032 1/2	8	8	8	4	4	4	8	8	EA
	6	TC	60140685-001	A	DN66 BLKHD BRKT ASSY	-	-	-	2	2	2	-	-	EA
	10	TC	60140695-001	A	L6 BLKHD BRKT ASSY	2	2	2	-	-	-	-	-	EA
	12	A	03010220-030	V	SCREWTPNT 1032 5/8	-	-	-	4	4	4	-	-	EA
	15	D	60135932	D	INSTL MD CAB NML	X	X	X	-	-	-	X	X	--
	17	D	60140769	D	INSTL BLKHD CAB HNP	-	-	-	X	X	X	-	-	EA
	18	D	60140739	D	COMM BULKHEAD INSTL	X	X	X	X	X	X	X	X	EA
	19	D	60140063	D	INSTL SHPNG CAGE	X	X	X	X	X	X	X	X	--
	20	D	60142029-001	P	PLATE BLKHD 37/25	1	-	-	1	-	-	-	-	EA
	21	D	60142030-001	P	PLATE BLKHD 37	-	1	-	-	1	-	-	-	EA
	22	D	60143455-001	P	BLKHD PERIPH 24	-	-	1	-	-	1	-	-	EA
	23	TC	60143534-001	A	BRKT FAB BLKHD L6	-	-	-	-	-	-	2	-	EA
	24	TC	60143534-002	A	BRKT FAB BLKHD L6	-	-	-	-	-	-	-	2	EA
	27	A	04830369-019	V	CONN LCK FEM W/O HDW	-	-	-	32	32	48	32	64	EA

Honeywell
HONEYWELL INFORMATION SYSTEMS
LOC. BILLERICA, MASSACHUSETTS, USA.

UM = UNIT OF MEASURE
EA = EACH IN = INCHES
CM = CENTIMETER OZ = OUNCE
G = GRAMS

**=ITEMS CHANGED SINCE REV F

TITLE: INSTL BLKHD COMM

SIZE TX | P.L. NO. 60140740 | SHEET 3 | REV. G

DOES A DOCUMENT REVISION STATUS SHEET EXIST? YES

S = SUBSTITUTE PARTS

HONEYWELL CONFIDENTIAL & PROPRIETARY

810708 | SIZE TX 60140740 | SHEET 4F | REV. G

•	ITEM NO.	P C	IDENTIFICATION NO.	S C	DRAWING TITLE	ASSEMBLY/QUANTITY 017	018	019	020	021				U M
**	3	A	03010221-001	V	SC/WA THP 1032 1/2	8	8	8	8	8				EA
**	4	TC	60140684-001	A	OFP BLKHD BRKT ASSY	-	-	-	2	-				EA
	15	D	60135932	D	INSTL MD CAB NML	X	X	X	-	-				--
**	18	D	60140739	D	COMM BULKHEAD INSTL	X	X	X	X	X				EA
**	19	D	60140063	D	INSTL SHPNG CAGE	X	X	X	-	X				--
	20	D	60142029-001	P	PLATE BLKHD 37/25	1	-	-	-	-				EA
	21	D	60142030-001	P	PLATE BLKHD 37	-	1	-	-	-				EA
	22	D	60143455-001	P	BLKHD PERIPH 24	-	-	1	-	-				EA
**	23	TC	60143534-001	A	BRKT FAB BLKHD L6	2	2	2	-	2				EA
**	27	A	04830369-019	V	CONN LCK FEM W/O HDW	32	32	48	32	32				EA
**	28	D	60142029-002	P	PLATE BLKHD 37/25	-	-	-	1	-				EA
**	29	D	60142030-002	P	PLATE BLKHD 37	-	-	-	-	1				EA

Honeywell
HONEYWELL INFORMATION SYSTEMS
LOC. BILLERICA, MASSACHUSETTS, USA.

UM = UNIT OF MEASURE
EA = EACH IN = INCHES
CM = CENTIMETER OZ = OUNCE
G = GRAMS

**=ITEMS CHANGED SINCE REV F

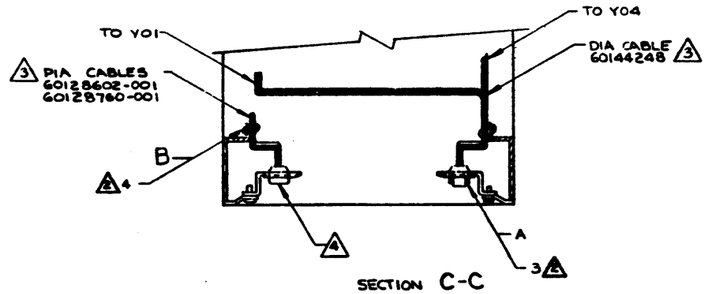
TITLE: INSTL BLKHD COMM

SIZE TX | P.L. NO. 60140740 | SHEET 4F | REV. G

DOES A DOCUMENT REVISION STATUS SHEET EXIST? YES

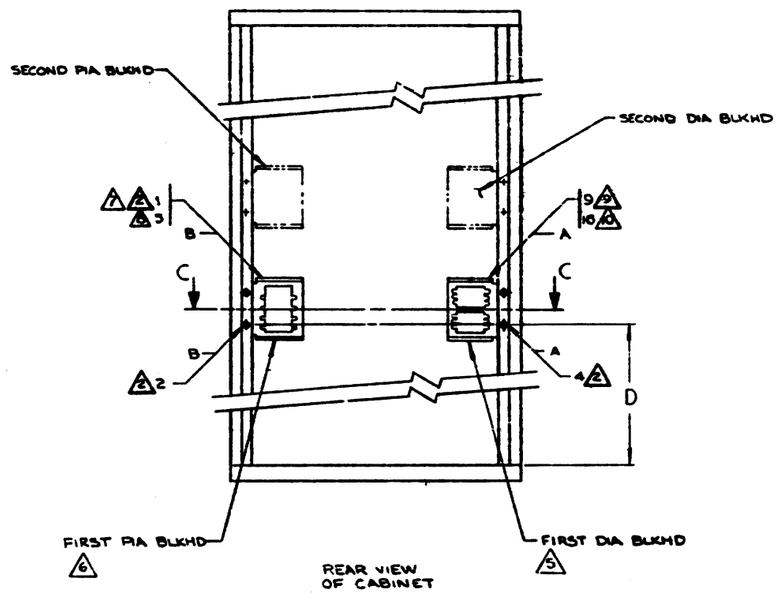
S = SUBSTITUTE PARTS

REVISIONS						
	REV	AUTHORITY	DATE YR	DATE MO	DATE DAY	SIGNATURE
L1.9	A	BLCDB7672	81	06	10	
L2.0	B	BLCDB7846	81	09	11	
L2.0	C	BLCC0836	82	06	25	



ITEM	DESCRIPTION	KIT NO.	INSTL DWG
A	KIT MINI BLKHD	TX 60143839-005/011	C 60146675
B	KIT BLKHD MINI PIA	TX 60146658-001/002	C 60146675

2



DIM	FIRST BLKHD	SECOND BLKHD
D	579.4 22.81	950.7 37.43

Δ 5. UTILIZE ALL POS. OF DIA FIRST BLKHD BEFORE ADDING SECOND BLKHD TO SYSTEM. START WITH LWR DIA, POS # 1 (J01-J03) THAN ON TO DIA, POS # 2 (J01-J05)

Δ 4. INSERT CONNECTORS THRU CUTOUT & MOUNT ON FRONT OF PLATE USING SWELL HARDWARE

Δ 3. SECURE CABLES TO SIDE RAILS AS REQUIRED

Δ 2. FOR ITEM CALLOUTS SEE KIT NO. 60143839-005 &CHG 60146658-001&002 (REFER TO CHART ABOVE)

1. THIS DWG IS FOR REFERANCE ONLY

10. TX60143839-011 MINI BLKHD 6-37(38-DEEP) PIA
9. TX60143839-005 MINI BLKHD 6-37. DIA
8. TX60146658-002 MINI BLKHD 6-37(38-DEEP) PIA
7. TX60146658-001 MINI BLKHD 6-37 PIA
Δ 6. UTILIZE ALL POS. OF PIA FIRST BLKHD BEFORE ADDING SECOND BLKHD TO SYSTEM. START WITH LWR PIA POS. (J01, J02) THAN ON TO UPPER PIA POS. (J03, J04)

NEXT ASSY TX 60146659

UNLESS OTHERWISE SPECIFIED: DIMENSIONS — MILLIMETERS / INCHES; TOLERANCE OF SIZE AND FORM PER ITEM; INITIAL DESIGN PROJECTION; SCALE NONE; CONT

MATL | TREAT. | FIN. | DR. J. Millett 6-23-81 | APP'D

Honeywell
HONEYWELL INFORMATION SYSTEMS
LOC BILLERICA, MA. U.S.A.

TITLE: INSTL BLKHD DN 66

SIZE D | DWG NO. 60146675 | SH 1/1 | REV C

60146675

820716

SIZE		SHEET	REV.
TX	60143839	1/2	D

•	ITEM NO	P C	IDENTIFICATION NO	S C	DRAWING TITLE	ASSEMBLY/QUANTITY 001	002	003	004	005	006	007	008	U M
	1	TC	60143836-001	A	BLKHD MINI 2-37	1	-	-	-	-	-	-	-	EA
	2	TC	60143837-001	A	BLKHD FAB MINI 6-37	-	1	-	-	-	-	-	-	EA
*	3	A	04830349-019	V	CONN LCK FEM W/O HDW	4	10	12	12	12	4	4	12	EA
*	4	A	03010221-001	V	SC/MA THP 1032 1/2	2	2	2	2	2	2	2	2	EA
*	5	C	60143838	D	INSTL MINI BLKHD	X	X	X	-	X	X	X	X	--
	6	A	03910299-004	V	LABEL BLKHD DEV DBK	-	1	-	-	-	-	-	-	EA
	7	TC	60143837-002	A	BLKHD FAB MINI 6-37	-	-	1	-	-	-	-	-	EA
	8	TC	60143837-003	A	BLKHD FAB MINI 6-37	-	-	-	1	-	-	-	-	EA
	9	TC	60143837-004	A	BLKHD FAB MINI 6-37	-	-	-	-	1	-	-	-	EA
*	10	C	60144249	D	INSTL BLKHD 234E	-	-	-	X	-	-	X	-	--
*	11	TD	60146881-001	A	BLKHD FAB MINI 2-37	-	-	-	-	-	1	-	-	EA
*	12	TD	60146881-002	A	BLKHD FAB MINI 2-37	-	-	-	-	-	-	1	-	EA
*	13	TC	60146880-001	A	BLKHD FAB MINI 6-37	-	-	-	-	-	-	-	1	EA
*	17	D	60146675	D	INSTL BLKHD DN 66	-	-	-	-	X	-	-	-	--
*	18	C	60146687	D	INSTL BLKHD DN8	-	-	-	-	X	-	-	-	EA

Honeywell
HONEYWELL INFORMATION SYSTEMS
LOC. BILLERICA, MASSACHUSETTS, USA.

UM = UNIT OF MEASURE
EA = EACH, CM = CENTIMETER, G = GRAMS, IN = INCHES, OZ = OUNCE, M = METER

*=ITEMS CHANGED SINCE REV C

TITLE: KIT MINI BLKHD

SIZE	P.L. NO.	SHEET	REV.
TX	60143839	1/2	D

DOES A DOCUMENT REVISION STATUS SHEET EXIST? YES

S = SUBSTITUTE PARTS

HONEYWELL CONFIDENTIAL & PROPRIETARY

820716

SIZE		SHEET	REV.
TX	60143839	2P	D

•	ITEM NO	P C	IDENTIFICATION NO	S C	DRAWING TITLE	ASSEMBLY/QUANTITY 009	010	011	U M
*	3	A	04830349-019	V	CONN LCK FEM W/O HDW	12	12	12	EA
*	4	A	03010221-001	V	SC/MA THP 1032 1/2	2	2	2	EA
*	5	C	60143838	D	INSTL MINI BLKHD	X	-	X	--
*	10	C	60144249	D	INSTL BLKHD 234E	-	X	-	--
*	14	TD	60146880-002	A	BLKHD FAB MINI 6-37	1	-	-	EA
*	15	TD	60146880-003	A	BLKHD FAB MINI 6-37	-	1	-	EA
*	16	TD	60146880-004	A	BLKHD FAB MINI 6-37	-	-	1	EA
*	17	D	60146675	D	INSTL BLKHD DN 66	-	-	X	--
*	18	C	60146687	D	INSTL BLKHD DN8	-	-	X	EA

Honeywell
HONEYWELL INFORMATION SYSTEMS
LOC. BILLERICA, MASSACHUSETTS, USA.

UM = UNIT OF MEASURE
EA = EACH, CM = CENTIMETER, G = GRAMS, IN = INCHES, OZ = OUNCE, M = METER

*=ITEMS CHANGED SINCE REV C

TITLE: KIT MINI BLKHD

SIZE	P.L. NO.	SHEET	REV.
TX	60143839	2P	D

DOES A DOCUMENT REVISION STATUS SHEET EXIST? YES

S = SUBSTITUTE PARTS

820716

SIZE		SHEET	REV.
TX	60146658	1/F	C

•	ITEM NO.	P C	IDENTIFICATION NO.	S C	DRAWING TITLE	ASSEMBLY/QUANTITY 001	002							U M
	1	TD	60146674-001	A	BLKHD FAB MINI PIA	1	-							EA
•	2	A	03010221-001	V	SC/MA THP 1032 1/2	2	2							EA
•	3	D	60146675	D	INSTL BLKHD ON 66	X	X							--
•	4	A	03510004-003	V	CLAMP CBL TIE 4	AR	AR							EA
•	5	TD	60146679-001	A	BLKHD FAB MINI PIA	-	1							EA

Honeywell
HONEYWELL INFORMATION SYSTEMS
LOC. BILLERICA, MASSACHUSETTS, USA.

UM = UNIT OF MEASURE
EA = EACH — IN = INCHES
CM = CENTIMETER — OZ = OUNCE
G = GRAMS — M = METER

•=ITEMS CHANGED SINCE REV B

TITLE: KIT BLKHD MINI PIA

SIZE	P.L. NO.	SHEET	REV.
TX	60146658	1F	C

DOES A DOCUMENT REVISION STATUS SHEET EXIST? YES

S = SUBSTITUTE PARTS

Honeywell

COLOR CODES FOR THE DATANET 8, DATANET 8C, AND DATANET 66 PDU POWER CORDS

The U.S. and international power cable color codes for the DATANET Power Distribution Units are as listed:

Conductor	U.S. Colors	International Colors
N – Neutral[a]	White	Blue
G — Ground[a]	Green or green w/yellow stripe	Green w/yellow stripe
Phase A – (X)[a]	Black	Brown
Phase B – (Y)	Red	Black[b]
Phase C – (Z)	Blue	Black[b]

[a]Colors used in 3-wire (single phase) code.

[b]Black wires have color stripe to aid in identification.

For further information contact: Honeywell Information Systems Inc., P.O. Box 6000, Phoenix, AZ 85005.

Order Number
VG93-00

Document Number
71017972-100

File No.: 2F<3

February 1984

SSTD HARDWARE PUBLICATIONS
USER COMMENTS FORM

DOCUMENT TITLE: _____

PART NO.: _____

ORDER NO.: _____

ERRORS:

HOW DO YOU USE THIS DOCUMENT?

THEORY ☐

MAINTENANCE ☐

TROUBLESHOOTING ☐

OTHER: _____

_____

DOES THIS MANUAL SATISFY YOUR REQUIREMENTS?

YES ☐ NO ☐

IF NOT, PLEASE EXPLAIN _____

_____

_____

FROM: NAME _____ DATE _____

TITLE _____

COMPANY _____

ADDRESS _____

PLEASE FOLD AND TAPE—
NOTE: U. S. Postal Service will not deliver stapled forms

NO POSTAGE
NECESSARY
IF MAILED
IN THE
UNITED STATES

BUSINESS REPLY MAIL
FIRST CLASS PERMIT NO. 39531 WALTHAM, MA02154

POSTAGE WILL BE PAID BY ADDRESSEE

HONEYWELL INFORMATION SYSTEMS
200 SMITH STREET
WALTHAM, MA 02154

ATTN: PUBLICATIONS, MS872A

CUT ALONG LINE

FOLD ALONG LINE

FOLD ALONG LINE

Honeywell

Together, we can find the answers.

Honeywell

Honeywell Information Systems
U.S.A.: 200 Smith St., MS 486, Waltham, MA 02154
Canada: 155 Gordon Baker Rd., Willowdale, ON M2H 3N7
U.K.: Great West Rd., Brentford, Middlesex TW8 9DH **Italy**: 32 Via Pirelli, 20124 Milano
Mexico: Avenida Nuevo Leon 250, Mexico 11, D.F. **Japan**: 2-2 Kanda Jimbo-cho Chiyoda-ku, Tokyo
Australia: 124 Walker St., North Sydney, N.S.W. 2060 **S.E. Asia**: Mandarin Plaza, Tsimshatsui East, H.K.

Printed in U.S.A.

FN01-03
(+A,B,C & D)