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DK512 Winchester Disk Drive OEM Manual

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DK512
WINCHESTER DISK DRIVE

K 6600074	SHEET No. 2/	REV NO 1
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REVISION RECORD

CODE
AD: Addition, CH: Change, CR: Correction, DL: Deletion

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		NOTICE	Copyright	AD
		REVISION	Copyright	DL
	2-1	2.1 Modle	85.7→86.1 120.0→120.6	CR
			171.4→172.4	CR
1→2		Operating Brief		DL
2→3	2-4	Acess Time	25ms→23	CH
	2-5	SEEK ERR RATE	$10^6 \rightarrow 10^7$	CR
	4-1	Fig 4-1	20sec→25sec	CR
	5-3	Fig 5-2	AM FOUND-N	CR
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	5-7	Fig 5-4	$T_2>30 \rightarrow T_2>20$	CH
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L I S T O F F I G U R E S

L I S T O F T A B L E S

1. INTRODUCTION

1.1 Purpose

This manual is intended to familiarize Original Equipment Manufacturers (OEMs) with the Hitachi DK512 Winchester disk drives, and to enable OEMs to integrate the drives into their computer-based systems. The manual provides technical information needed by system designers, engineers, purchasing agents and quality-control personnel. A separate Service Manual describes installation, strapping, spare parts, and troubleshooting.

1.2 Manufacturer

The DK512 series disk drives are manufactured at the Odawara Works, a member of the Hitachi Computer Division. The Odawara Works also produces large disk drives, magnetic tape drives, diskpacks, optical character readers, mass storage units, and data entry systems. Its first Winchester drives were delivered in 1976.

1.3 Quality Control

Production of the DK512 drives is highly automated, using robots and the latest technological advancements. The drives benefit from total vertical integration: heads, platters and electronics are all designed, manufactured and tested at the same facility, providing assurance of component compatibility. An elaborate quality control system assures that each drive satisfies all specifications.

1.4 Related Documents

The following documents are also applicable.

- Service Manual
- Schematic Diagrams
- Hitachi Technical Report on DK512

2. PRODUCT DESCRIPTION

The Hitachi DK512 series disk drives are high-capacity 5.25-inch Winchester disk drives with an Enhanced Small Device Interface (ESDI). The drives support the serial mode.

The mechanics and electronics are similar to DK511 series disk drives, which are already being marketed, but these new drives feature larger storage capacities, and higher transfer and access speeds.

2.1 Models

The series includes three models, differing in the number of disks mounted on the spindle:

Model	Disks	Capacity (MBytes) (Unformatted)
DK512-8	3	86.1
DK512-12	4	120.6
DK512-17	6	172.3

The unit is housed in an aluminum casting (see Figure 2-1). One casting accommodates all models.

2.2 Components

The DK512 disk drive includes the assemblies below and is delivered with the following documents attached. Sections 3.7 and 3.8 list the connectors and cables which the customer should prepare.

2.2.1 DK512 Disk Drive Unit

Figure 2-1 shows the DK512 disk drive unit.

The unit consists of:

- Head and Disk Assembly (HDA)
- Mounting Frame and Shock Mounts
- Printed Circuit (PC) boards. These are mounted in the frame

2.2.2 OEM Manual, Service Manual and Schematic Diagrams

One set of these transparencies is delivered with the first lot of drives. When any modification is maken, the corresponding transparency will be provided.

2.2.3 Test Report and Defect List

One set of the Test Report and the Defect List will be provided with each drive.

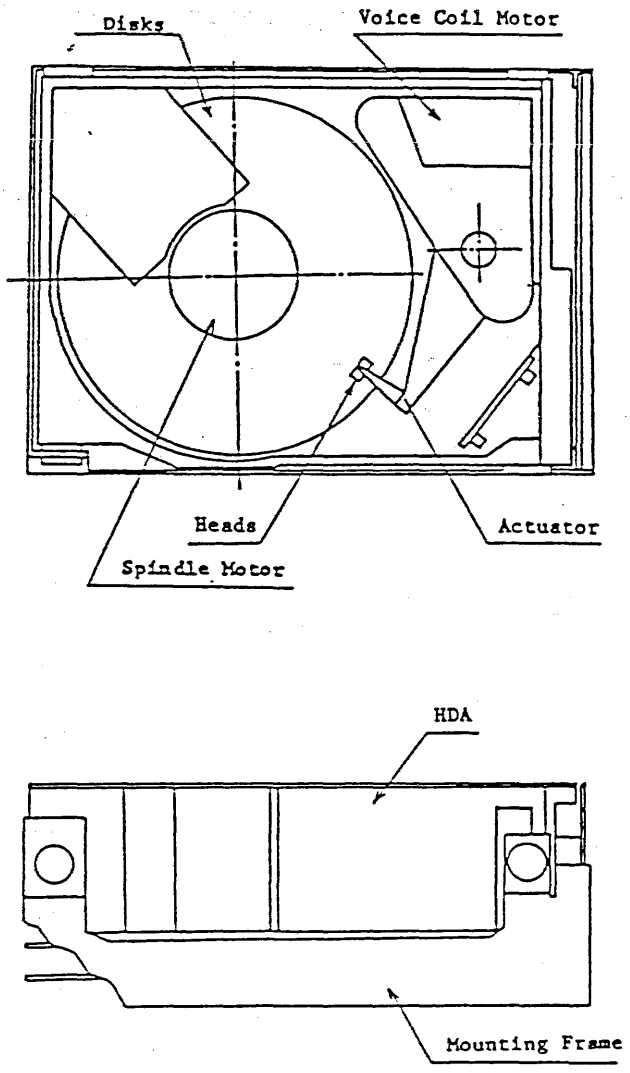


Figure 2-1 Structure of DK512

2.3 Options

- Controller Board

  The optional controller board enables a drive to operate with the SCSI interface.

2.4 Features

Hitachi drives are designed and manufactured for exceptional performance and high reliability. Each drive is given a lengthy burn-in, then tested at marginal conditions.

The principal features of the drives are summarized below:

- Large Capacity, Fast Data Transfer

  This is really a high performance disk drive with an exceptional maximum 171 Mbytes of capacity per drive and a fast 1.2 Mbytes/sec data transfer rate.

- Compact

  It took Hitachi to put all of this capacity in a body the same size as a minifloppy disk drive.

- High-Speed Access

  The DK512 offers 23 millisecond average access time thanks to positioning to heads by a microprocessor-controlled rotary voice-coil actuator.

- Superior Reliability

  In-house manufacturing of all heads, disks and custom LSIs, plus strict testing throughout guarantees the highest drive reliability.

- Industry Standard Interface

  The ESDI industry standard interface provides easy integration with a wide range of systems.

2.5 Specifications

Table 2-1 lists the complete specifications for DK512 models.

Table 2-1 Specifications

Model			DK512 -8	DK512 -12	DK512 -17
Total Capacity		(unformatted)	86.1 Mbytes	120.6 Mbytes	172.3 Mbytes
		(formatted)*	67.4 Mbytes	94.4 Mbytes	134.8 Mbytes
Capacity	per Track (unformatted)		20,944 bytes		
	per Track (formatted)*		16,384 bytes		
	per Sector (formatted)*		256 bytes		
Number of Sectors/Track			Selectable in one-byte increments		
Number of Disks			3	4	6
Number of Heads		Data Head	5	7	10
		Servo Head	1	1	1
Number of Cylinders			823		
Access Time (nominal)		Average	23 ms		
		Maximum	45 ms		
		Minimum	6 ms		
		Average Latency	8.6 ms		
Disk Speed			3,482 rpm ± 1%		
Data Transfer Rate			1,215 kbytes/sec		
Maximum Recording Density			18,500 bpi/925 tpi		
Recording Method			RLL 2-7		
Data Transfer Method with Controller			NRZ		
Startup Time			Approx. 25 seconds		
Power Requirements			+12V±5% 5.0 A (max.) 2.5 A (average) +5V±5% 2.8 A		
Dimensions		Height	82.5mm (3.25 in)		
		Width	146 mm (5.75 in)		
		Length	203 mm (8.00 in)		
Weight			Approx. 3.4Kg (7.5 lbs)		

(Cont'd)

*64 sectors/track

Table 2-1 Specifications (cont'd)

Model		DK512 -8	DK512 -12	DK512 -17
Interface	Type	ESDI		
	Configurations	Daisy-Chain or Radial		
Acoustic noise		Max 50 dBA, except when start-up, stop and seek.		
Reliability	MTBF	20,000 POH, typical usage		
	Preventive Maintenance	Not required		
	MTTR	0.5 hrs		
	Start/Stop Operations	Up to 10,000		
	Component Design Life	5 years or 20,000 POH		
Error Rate (within 10 retrials)	Recoverable (soft)	1 per 10^{10} bits read		
	Unrecoverable (hard)	1 per 10^{13} bits read		
Seek Error Rate		1 per 10^{6} seeks		
Ambient	Altitude Operating Nonoperating	 3,000 m (10,000 ft) max. 12,000 m (40,000 ft) max.		
	Temperature Operating Nonoperating Transporting/ storing Maximum Gradient	 5° - 45°C (41° - 113°F) -20° - 50°C (-4° - 122°F) -40° - 60°C (-40°- 140°F) 10°C/hr. (18°F/hr.)		
	Relative Humidity Operating Nonoperating	 8 - 80% (no condensation) 8 - 90% (no condensation)		
	Vibration Operating Nonoperating	 0.25G max. 0.5G max.		
	Shock Operating Nonoperating	 2G max. (10 msec,half sine wave) 20G max. (10 msec,half sine wave)		
	Air Cleanliness	No corrosive gas, salt, or metallic particulates.		
Media defects	Maximum number of defects per device	86	120	172
	Maximum number of defects per surface	40	40	40
	Defect Free Areas	Heads 0 and 1 on Cylinder 0		
	Logging	Each defect is identified in a written test report, and on the disk itself.		

2.6 Standards Observed

The DK512 drives will comply with the following standards:

UL 478
CSA 22.2-154
FCC Part 15, Class A (when mounted in a standard cabinet)

2.7 Mechanical Construction

A durable casting provides a stable mounting for the spindle motor and supports the voice coil motor. The voice coil motor pivots on precision bearings, moving between the poles of a permanent magnet. The motor carries 6-11 heads (depending on the model), which are mounted in pairs on adjustable cast aluminum truss arms. The monolithic flying heads are housed in light-weight frames which have been computer-adjusted for optimum tension against the disks. Hall sensors measure the speed of the spindle motor.

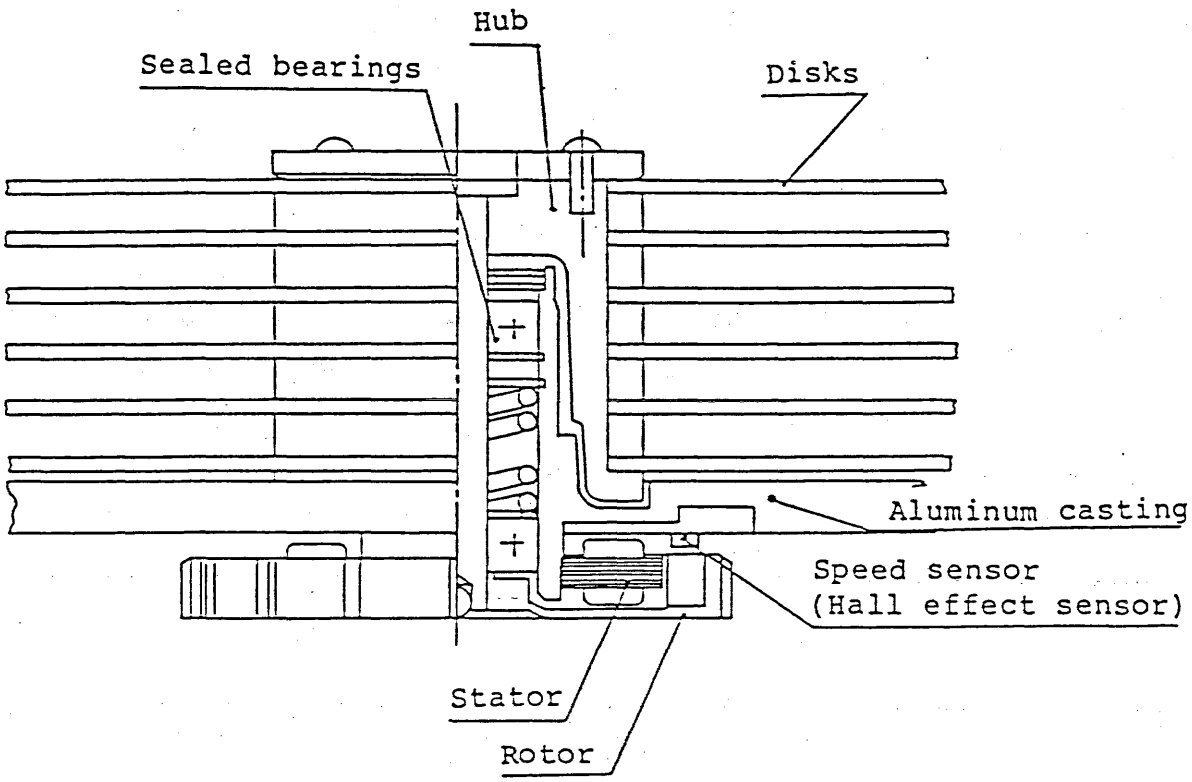


Figure 2-2 Spindle Motor

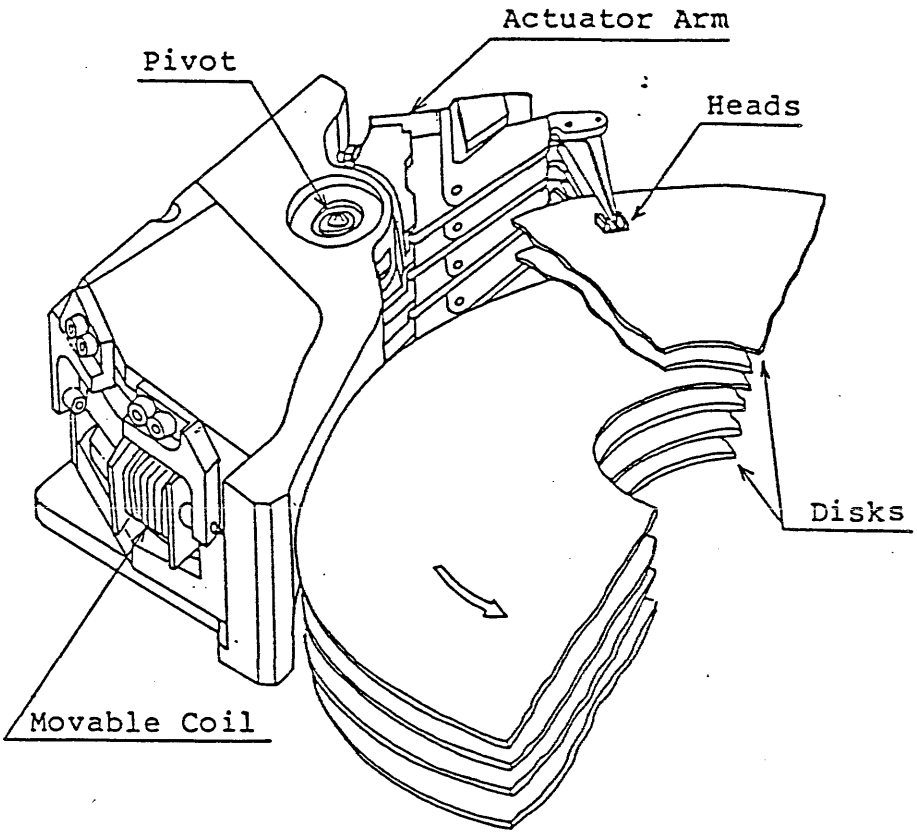


Figure 2-3 Actuator Arm Assembly

The disk platters are made with the aluminum substrates, which are turned with diamond tools to mirror finishes and parallel surfaces. Proprietary processes then produce uniform magnetic coatings. Every platter is tested and inspected at each step of production.

2.11 Disk Basics

The spindle rotates at 3,482 rpm, creating air films over the surfaces of the disks, which balance the pressure of the flying heads and prevent the heads from touching the surfaces. When the disks stop, as when power is turned off, the heads come to rest in a safe area near the center of the disk. Close head-to-disk spacing requires that the disks be sealed in a clean environment.

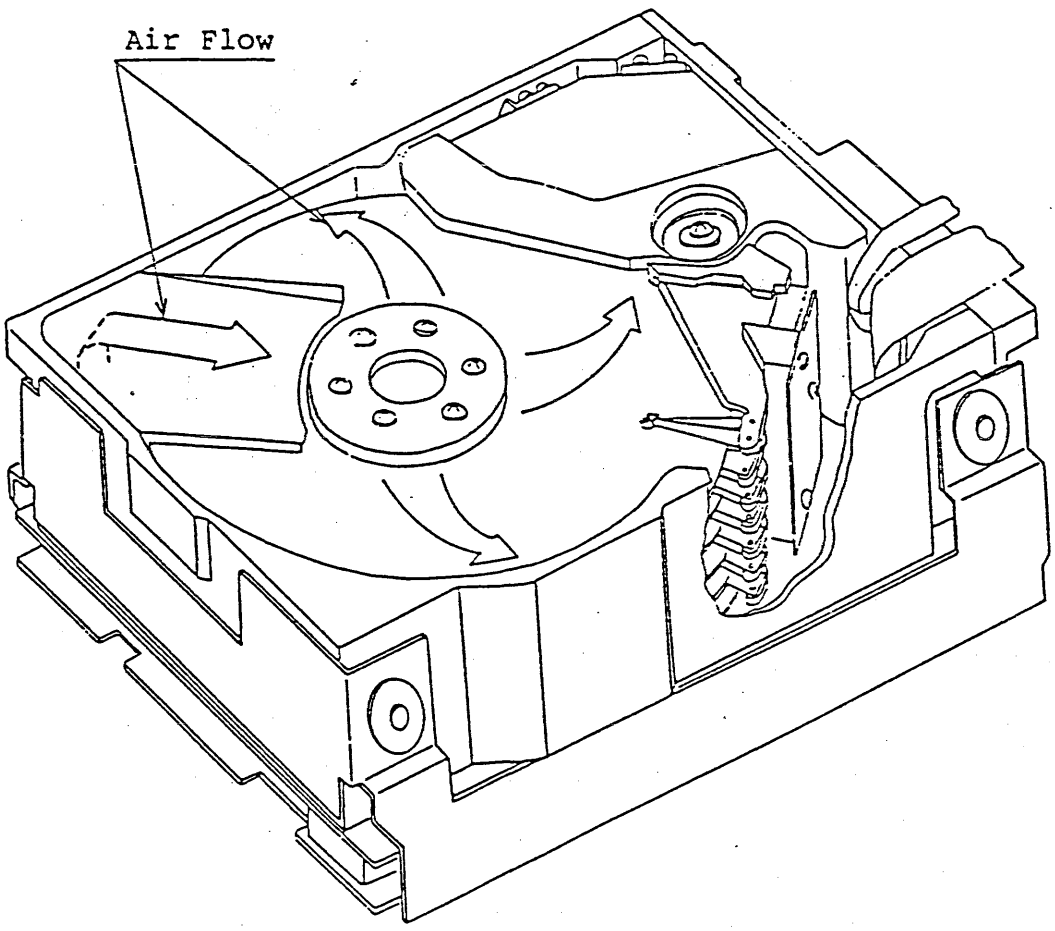


Figure 2-4 Air Circulation Inside Head and Disk Assembly

A positioning system for the voice coil motor moves the head assembly rapidly and accurately to the addressed cylinder. Since all heads are mechanically fastened together, they are positioned to the same cylinder, that is, to the same track on each surface. Cylinders are numbered from 0 at the periphery to 822 at the center.

Absolute cylinder position is established by the servo tracks, which are recorded at the factory on a dedicated surface, located at the top of the stack.
An elaborate feedback system centers the servo head in it's track.

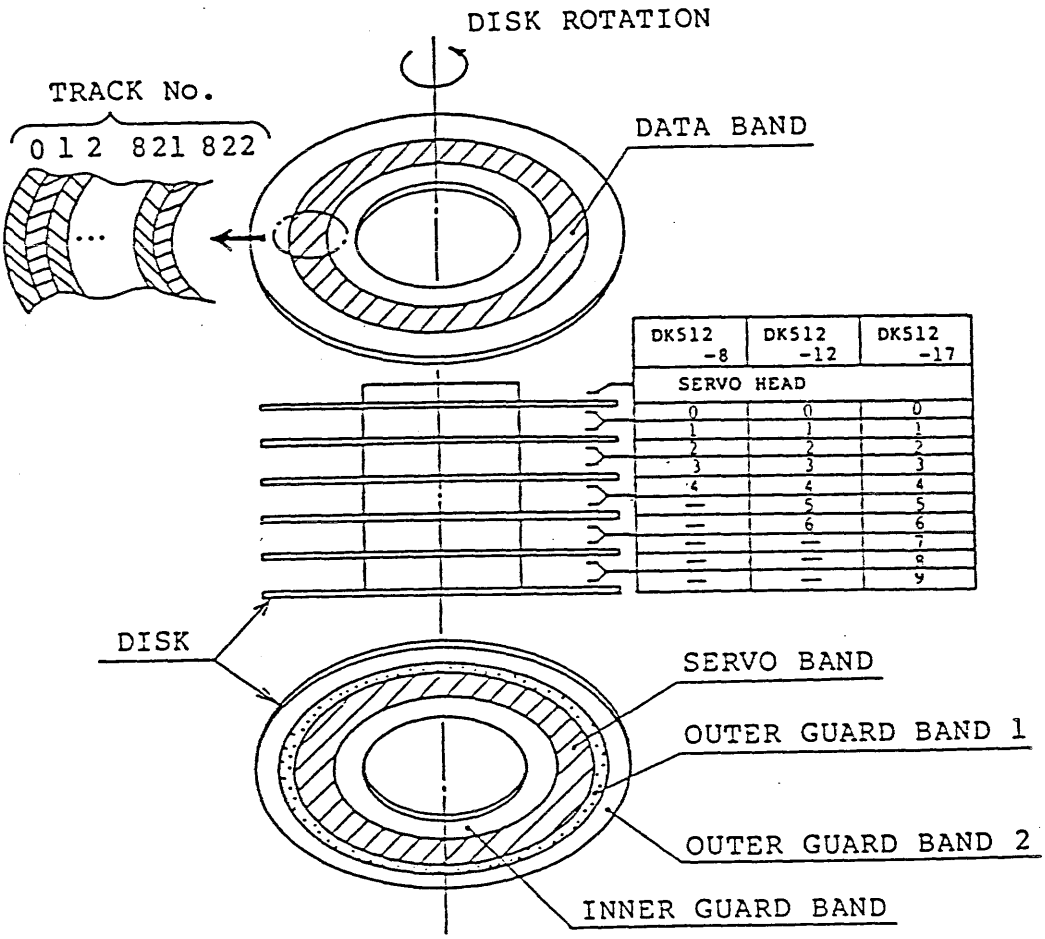


Figure 2-5 Head and Cylinder Address

An index signal and a precision clock are derived from the servo information. The index signal marks the beginning of a track or cylinder. The clock, a Phase Locked Oscillator (PLO), is a precision reference for writing data to the disk, and enables data to be formatted with shorter gaps between fields.

Disks are formatted by the OEM, depending on the intended application. Recommendations for a fixed sector format are provided in Chapter 6.

2.12 Power Supply

The drive requires +12 V DC and +5 V DC input.
Figure 2-6 shows the derived voltages and representative circuits operated by each voltage.

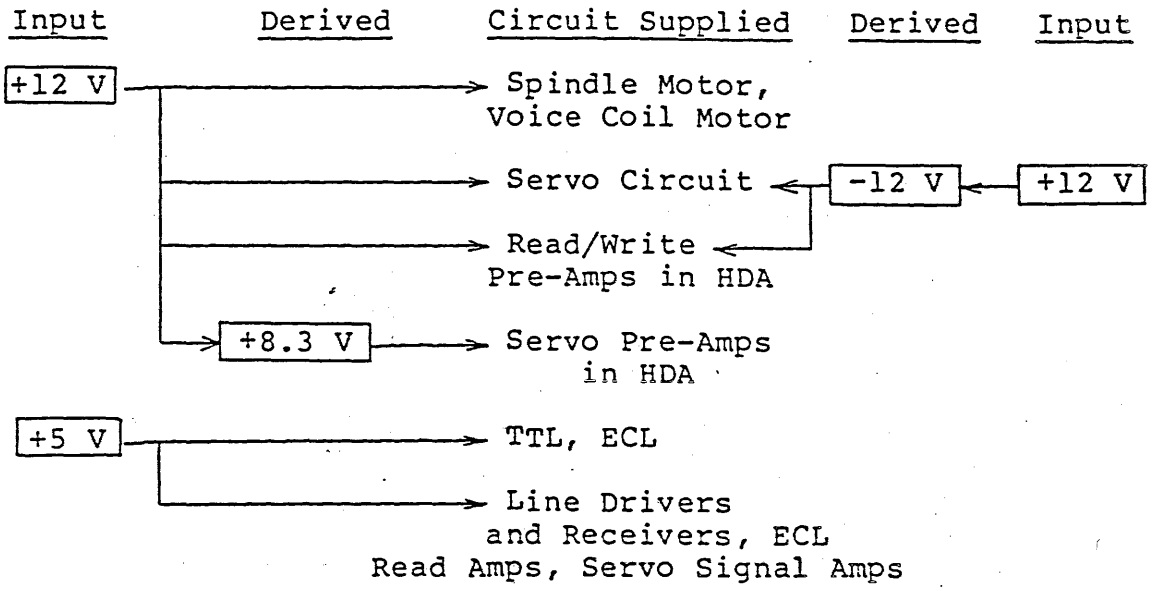


Figure 2-6 Voltage Utilization

2.13 SZ118 Read/Write PC Board

This PC board controls the drive's read and write operations. Mounted on this board are:

- Write driver
- READY and SELECTED Lamp(LED)
- Head select circuit
- Write fault sensor
- Read signal amplifier and AGC (Automatic Gain Control)
- Read signal equalizer amplifier

2.14 SZ123 Digital PC Board

This board controls digital operations such as interface control, seek control, servo control and read/write logic. Mounted on this board are:

- Line drivers and receivers
- One-chip microprocesser
- Head velocity digital-to-analog converter
- Address mark detector
- Low-voltage detector and power-on reset
- R/W gate control
- Cylinder address register
- STATUS circuit
- PLO (Phase-Locked Oscillator) for master clock
- VFO (Variable Frequency Oscillator) for READ DATA
- Read peak sense logic
- Write precompensation
- RLL 2-7 encoding and decoding (for writing to the disk)
- Servo logic
- Servo signal amplifier
- Position signal generator
- Sync pulse generator

2.15 SZ117 Analog PC Board

This board controls analog operations such as motor control, servo control and power supply. Mounted on this board are:

- Head positioning control
  - On-track signal sensor
  - Track crossing pulse generator
  - Absolute velocity signal generator
  - Velocity error signal generator
- Voice coil motor driver
- Voltage regulator (+2 V)
- DC-DC converter (-12 V)
- DC spindle motor control

2.16 Microprocessor

A high-speed 64-pin CMOS one-chip microcomputer is employed. This has reduced remarkably the size of circuits. Its main functions are:

- Motor power-on sequence
- Positioning the heads at the addressed cylinder, using a fast seek algorithm
- Returning the heads to the zero cylinder during power-up and recalibration (RTZ)
- Command protocol control
- Spindle motor speed checking

3. PHYSICAL INTERFACE

3.1 Physical Description

The DK512 5.25-inch disk drive is shown in the frontispiece and in Figure 3-1. Three cables (control, data, and power) plug in at one end of the DK512 PC assembly; connectors for cables to the Head and Disk Assembly (HDA) are at the other end where the Read/Write PC Board is attached, i.e., on the Front Panel side. The Read/Write PC Board is screwed to a heavy cover used as a heat sink; it is connected with two plug-in cables. The HDA is sealed in a contaminant-free atmosphere in its casting and is never to be opened in the field.

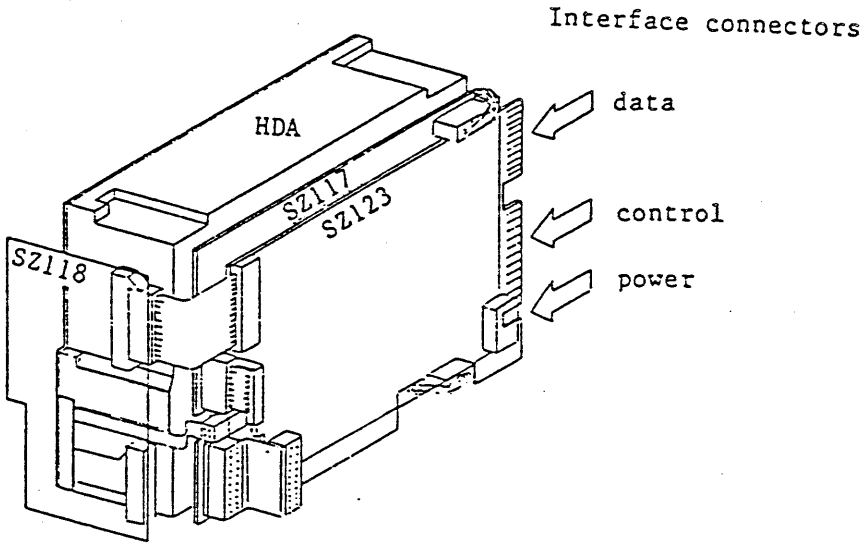
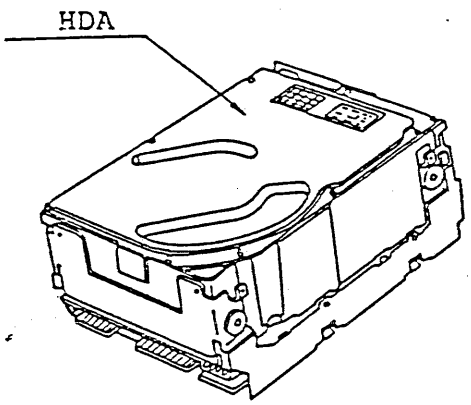
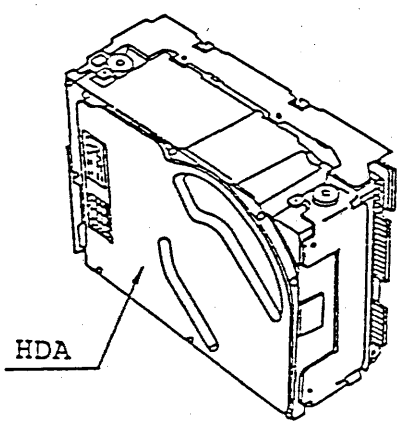


Figure 3-1 DK512 PC Boards and Interface Connectors

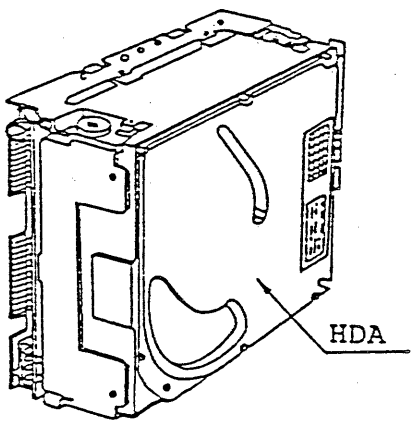
Figure 3-2 shows how the drive may be mounted either horizontally or vertically. Forced or natural air cooling may be used. When the drive is installed in a cabinet or box, forced air cooling is required. When no fan is used, the drive should be mounted so that the internal heat is conducted out completely and no outside heat affects the drive.



(a) Horizontal mounting



b) Vertical mounting-1



c) Vertical mounting-2

Figure 3-2 Mounting Positions

3.2 Mounting Requirements

The drive has 8 threaded holes for the mounting screws. Four screws are used, whether the drive is mounted horizontally or vertically. Be careful not to insert the mounting screws more than 5 mm (0.2 inch) into the drive. Figure 3-3 shows the DK512 mounting dimensions.

The guidelines in Section 3.2 should be observed by those responsible for mounting the DK512 in a system.

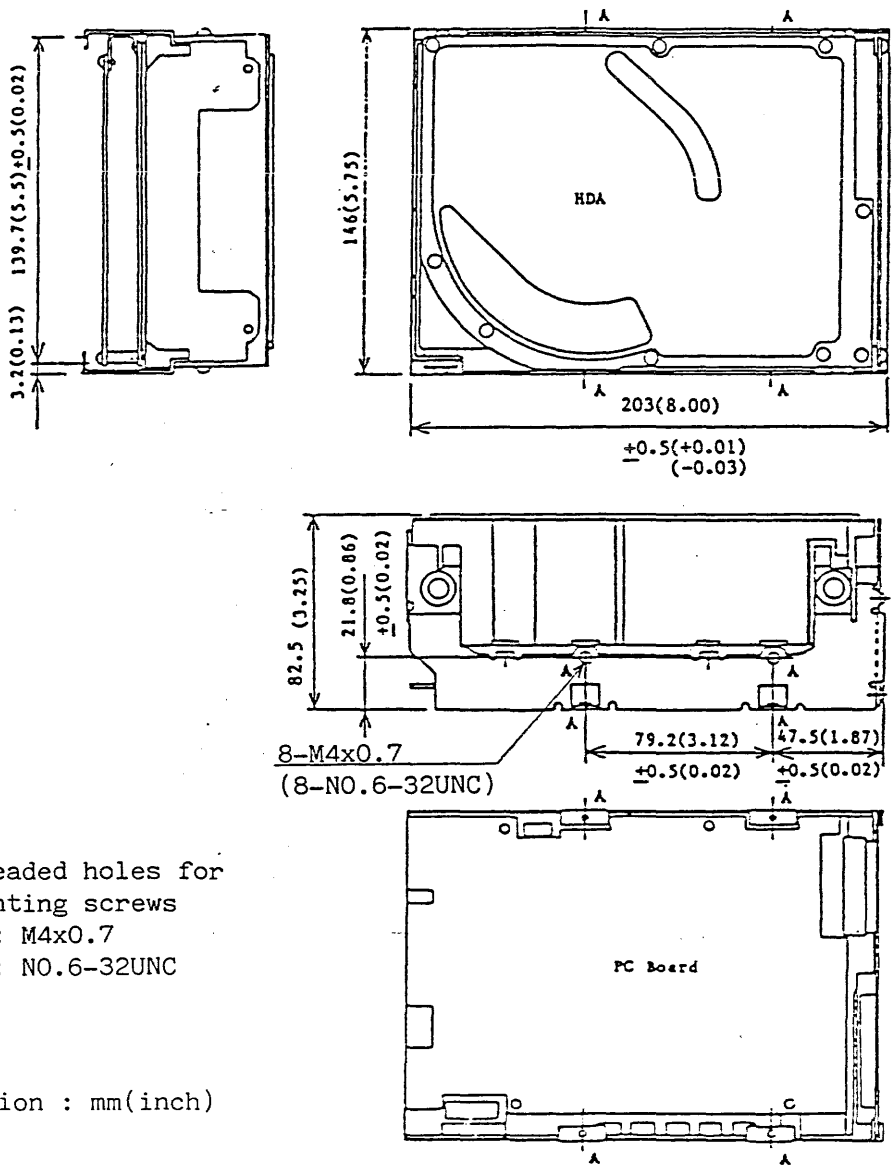


Figure 3-3 DK512 Mounting Dimensions: Side and Top Views

3.2.1 Shock Mounts and Handling

Special precautions must be taken so that the drive is not jarred or bumped while it is off its shock mounts. When removed from the system, it must be placed on a urethane foam cushion. The drive should be installed in an accessible position for convenient removal and maintenance.

3.2.2 Metric Screws

Only metric screw threads and screws are used on the DK512. They are specified as:

M4x.7x8, where
- M = Metric
- 4 = basic major diameter, mm. Thus, a clearance hole would be approximately 4/25.4 = 0.157 inch.
- 7 = distance between threads, mm. Thus, this screw has 25.4/0.7 = 36.3 threads per inch.
- 8 = length, mm.

Metric screws must be used. There are no U.S. Standard screws, even in unusual sizes, that are interchangeable.

3.2.3 Air Flow

The DK512 disk drives are more reliable as the ambient temperature lowers. Air must pass over all sides of the HDA and between the boards. Select natural or forced cooling depending on its mounting conditions.

3.2.3.1 Forced Cooling

When the drive is mounted in a cabinet or box, a fan must be installed on the cabinet or box to force heated air out and take outside air in. Keep the internal temperature as close to the room temperature as possible. Figure 3-4 shows the forced air flow.

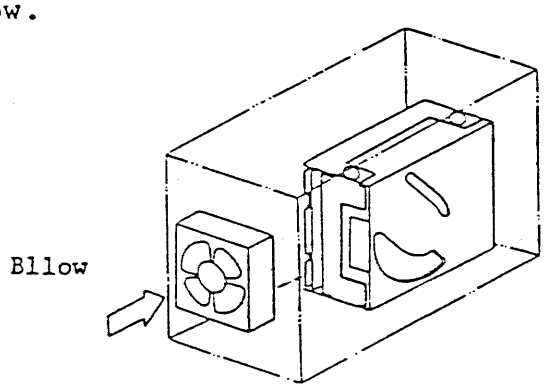


Figure 3-4 An Example of Forced Cooling

3.2.3.2 Natural Cooling

Natural cooling means that the drive is mounted so that no heated air remains anywhere in the devices, and that no outside heat affects the drive.

3.4 Interface Connectors

Control cable B, data cable C, and DC power cable A from the controller are connected to the drive at the following connectors:

- J1 for Control Cable B (P1)
- J2 for Data Cable C (P2)
- J3 for DC Power Cable A (P3)
- J4 for Ground Cable D (P4)

Figure 3-5 shows the locations of these four connectors.
Figure 3-6 shows the DC power cable A connector J3 pinout.
Figure 3-7 shows the ground cable D connector J4 pinout.

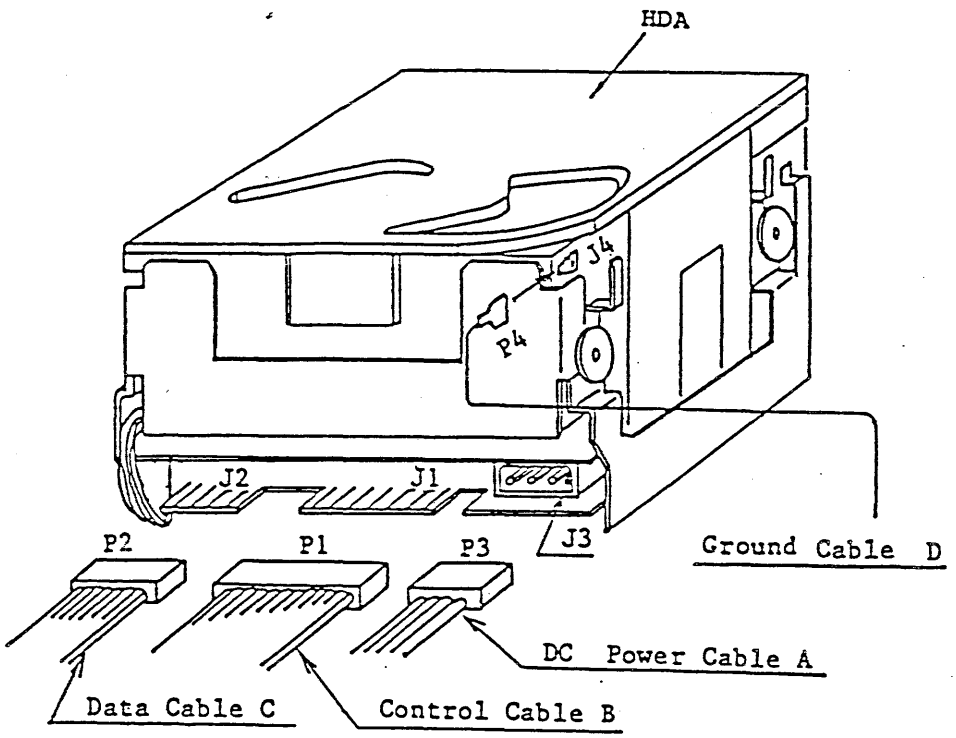
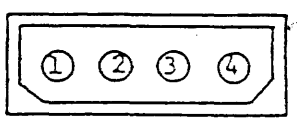


Figure 3-5 Cable Connector Locations



1 : +12V DC
2 : +12V return (GND)
3 : +5V return (GND)
4 : +5V DC

Figure 3-6 DC Power Cable A Connector J3

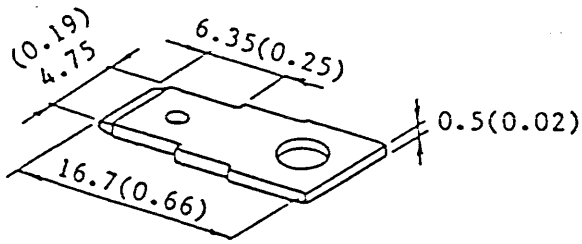


Figure 3-7 Ground Cable D Connector J4

3.5 Control Cable B Pinout

Figure 3-8 shows the dimensions of control cable B connector J1.

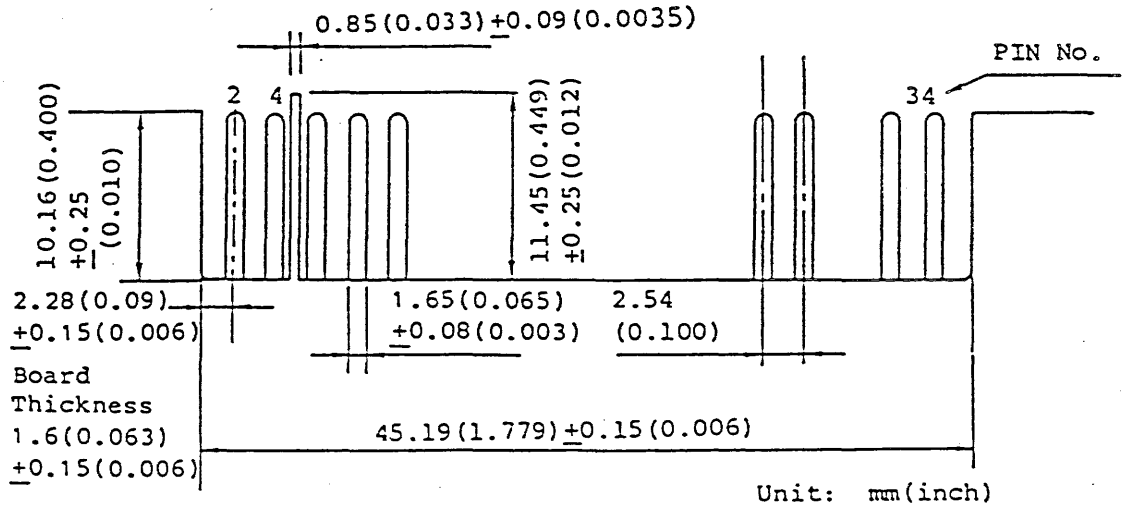


Figure 3-8 Control Cable B Connector J1

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		'86·2·25

3.6 Data Cable C Pinout

Figure 3-9 shows the data cable C connector J2.

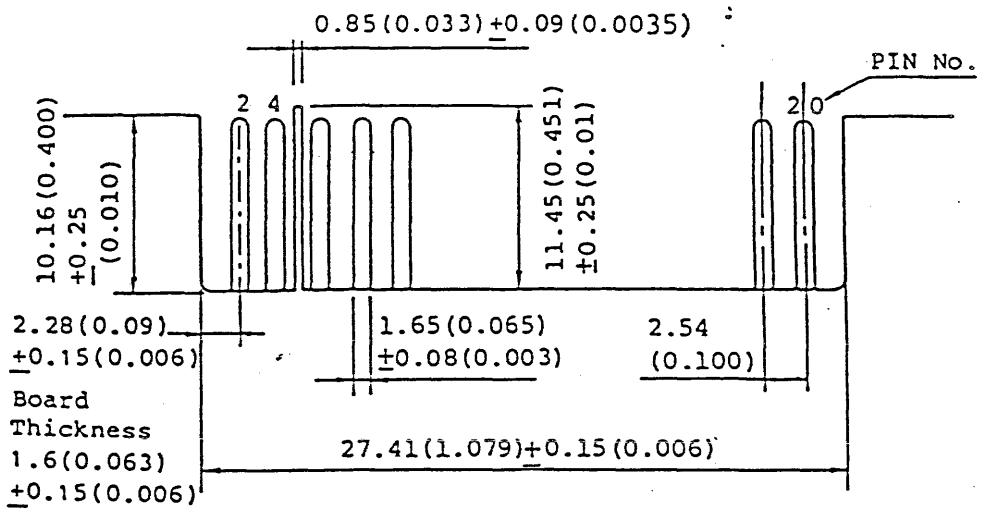


Figure 3-9 Data Cable C Connector J2

3.7 Connector Specifications for Cable Plugs

Table 3-1 lists connector specifications for cable plugs.

Table 3-1 Connector Specifications for Cable Plugs

Cable	Item	Mfr.	Manufacturer's Part Number	Qty.
B Control	P1 Connector	AMP	88373-3	1
C Data	P2 Connector	AMP	88373-6	1
A DC Power	P3 Connector Pin Housing	 AMP AMP	 61314-4 1-480424-0	 4 1
D Ground	P4 Plug	AMP	62187-1 or 60711-1 or 170038-2	1

3.8 Cable Specifications

Table 3-2 lists cable specifications.

Table 3-2 Cable Specifications

Cable	Item	Length
B Control	Flat ribbon or twisted pair	3 m max., cumulative
C Data	Flat ribbon or twisted pair	3 m max., each cable
A DC Power	20 AWG	3 m max., each cable
D Ground	Braid or equivalent, 20 AWG	3 m max., each cable

*To reduce noise, braid the cable in such cases as the cable goes out of the system cabinet.

3.9 Crimping Tools

Table 3-3 Crimping Tools

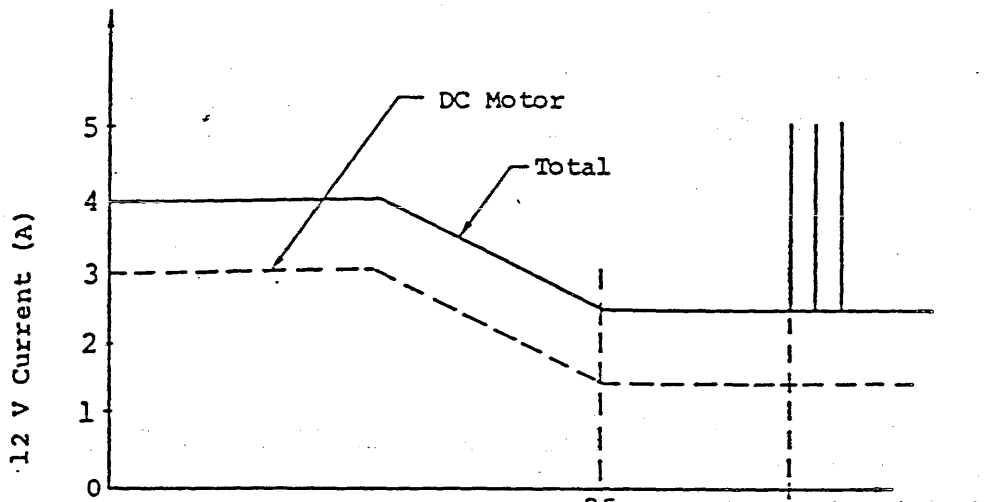
Cable	Crimping tool
B Control	Air pressure type: AMP91112-2 Manual type (bench type): AMP91085-2 Manual type: AMP91128-1
C Data	
A DC power	Manual type: AMP90123-2
D Ground	—

4. ELECTRICAL INTERFACE

4.1 DC Power Requirements

Figure 4-1 gives the +12 V DC requirements. The DC brushless motor requires a maximum current of 5.0 A at startup and has short peak current requirements during seek operations.

The drive requires also +5 V DC power of 2.8 A.



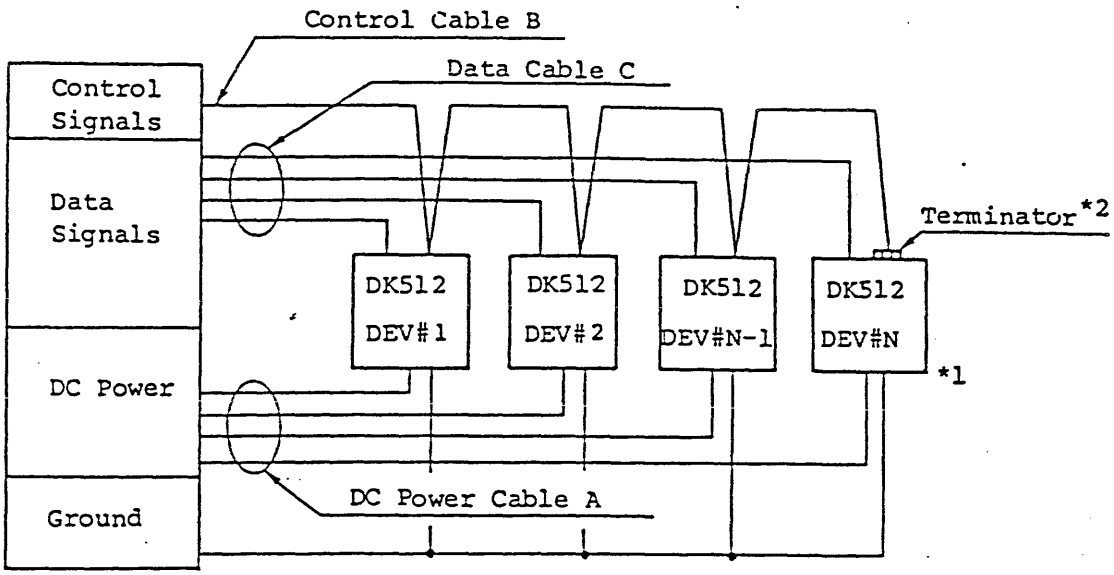
+12 V Power		(average)	
DC Motor	3.0 A max.	1.5 A	-
Other Equip.	1.0 A	1.0 A	-
Total	4.0 A max.	2.5 A	5.0 A max.

Figure 4-1 +12 V DC Power Requirements

Note that starting up two or more motors simultaneously results in a large current flow. To avoid this, wait at least 20 seconds before turning on the +12 V DC power for the second motor. All the devices become ready when the last device enters the READY state.

4.2 Daisy-Chain Connection

Figure 4-2 shows the daisy-chain connection.



Notes

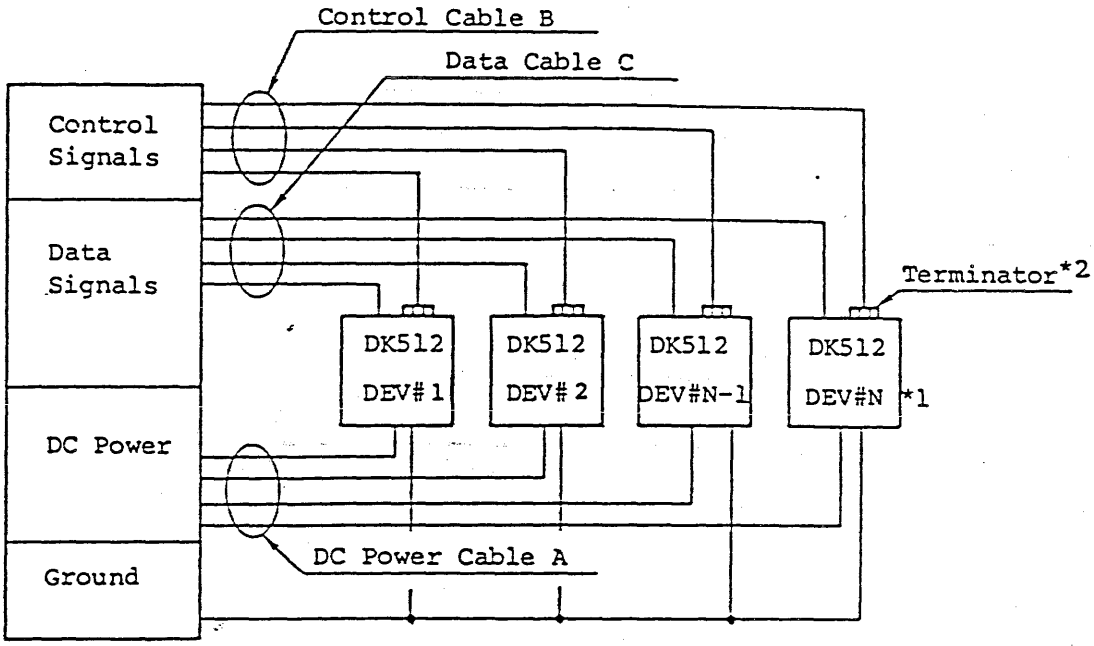
*1. N=7 for SERIAL mode.

*2. The last device (only) in the daisy-chain must have terminator on cable B. Remove the other terminators that are provided with each drive. Refer to Service Manual for the locations and other necessary information.

Figure 4-2 Daisy-Chain Connection

4.3 Star Connection

Figure 4-3 shows the star connection.



Notes

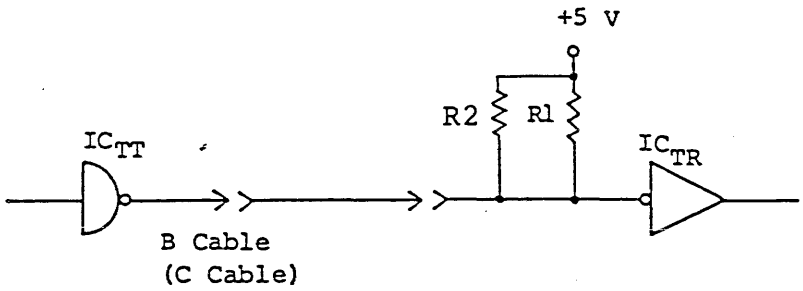
*1. N=7 for SERIAL mode.

*2. Each control cable is terminated at its drive. Plug-in terminators are provided with each drive.

Figure 4-3 Star Connection

4.4 Control Signal Transmitter and Receiver Circuits

Figure 4-4 shows a single signal line in simplified form. The transmitter is a 7438 or equivalent integrated circuit line driver which outputs TTL signals. The receiver is a 7414 or equivalent integrated circuit line receiver. This TTL interface circuit is used for all the DK512 signals except WRITE CLOCK, READ/REFERENCE CLOCK, NRZ WRITE DATA and NRZ READ DATA.



IC_{TT}: 7438
IC_{TR}: 74LS14/7414/74LS240

R1 : 220Ω ±5%
R2 : 330Ω ±5%

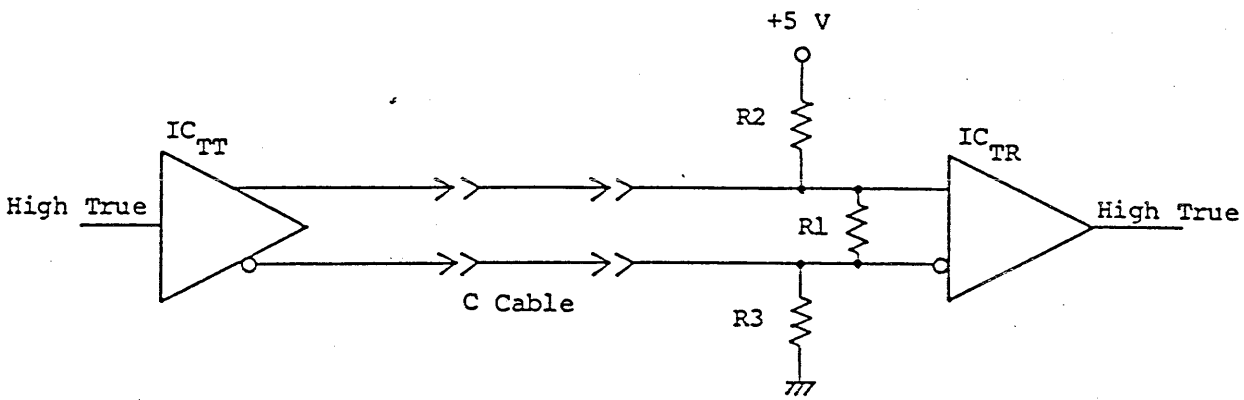
Figure 4-4 TTL Interface Circuit

The TTL interface signal transmitter and reciever circuits have the following characteristics. Note that values are those at 25°C (77°F).

- Input signal:
  - High false "0": +2.5 V - +5.0 V
  - Low true "1" : 0 V - +0.5 V
  - Rise/Fall time: 30 ns max.
- Output signal:
  - High false "0": Open collector output
  - Low true "1" : 0.4 V max.
  - Rise/Fall time: 30 ns max.

4.5 Data Signal Transmitter and Receiver Circuits

Figure 4-5 shows a simplified schematic of the data cable signal circuits. The transmitter is a 75172 or equivalent integrated circuit line driver with a three-state differential output. The receiver is a 75173 or equivalent integrated circuit. This interface circuit is used for data signals on cable C: WRITE CLOCK, READ/REFERENCE CLOCK, NRZ WRITE DATA and NRZ READ DATA.



IC_{TT} : 26LS31/75172
IC_{TR} : 26LS32/75173

R1 : 100Ω ±5%
R2,R3: 4.7 kΩ ±10%

Figure 4-5 Data Interface Circuits

Resistors R2 and R3 shown in this figure prevent the line receiver from oscillating when the differential line enters a high impedance state.

The data signal transmitter and receiver circuits have these characteristics. Note that values are those at 25°C (77°F).

- Input signal: High false "0", Low true "1"

$$| V_H - V_L | > 200 \text{ mV}$$

- Output signal: High false "0", Low true "1"

$$| V_H - V_L | > 2 \text{ V}$$

Signal names with -P suffix represent high true "1" signals, while those with -N suffix are low true "1" signals.

5. INTERFACE SIGNALS -- SERIAL MODE

This chapter describes the interface signals and timing requirements for the ESDI interface SERIAL mode implementation. Signal timing specifications are those measured at the connector pins in the drive.

Figure 5-1 shows the DK512 block diagram for SERIAL mode implementation. First, the drive is selected, then the cylinder, finally the head. The desired sector is obtained by reading the sector addresses passing under the head. Each track has sync patterns and intersector gaps. WRITE GATE is asserted and negated in designated places in these fields, producing write splices. The servo information keeps the heads on cylinder, and develops the clock for encoding and decoding the data.

Table 5-1 lists the pinout for control cable B and Table 5-2 the pinout for data cable C.

Section 5.1 covers the control signals and Section 5.2 the data signals.

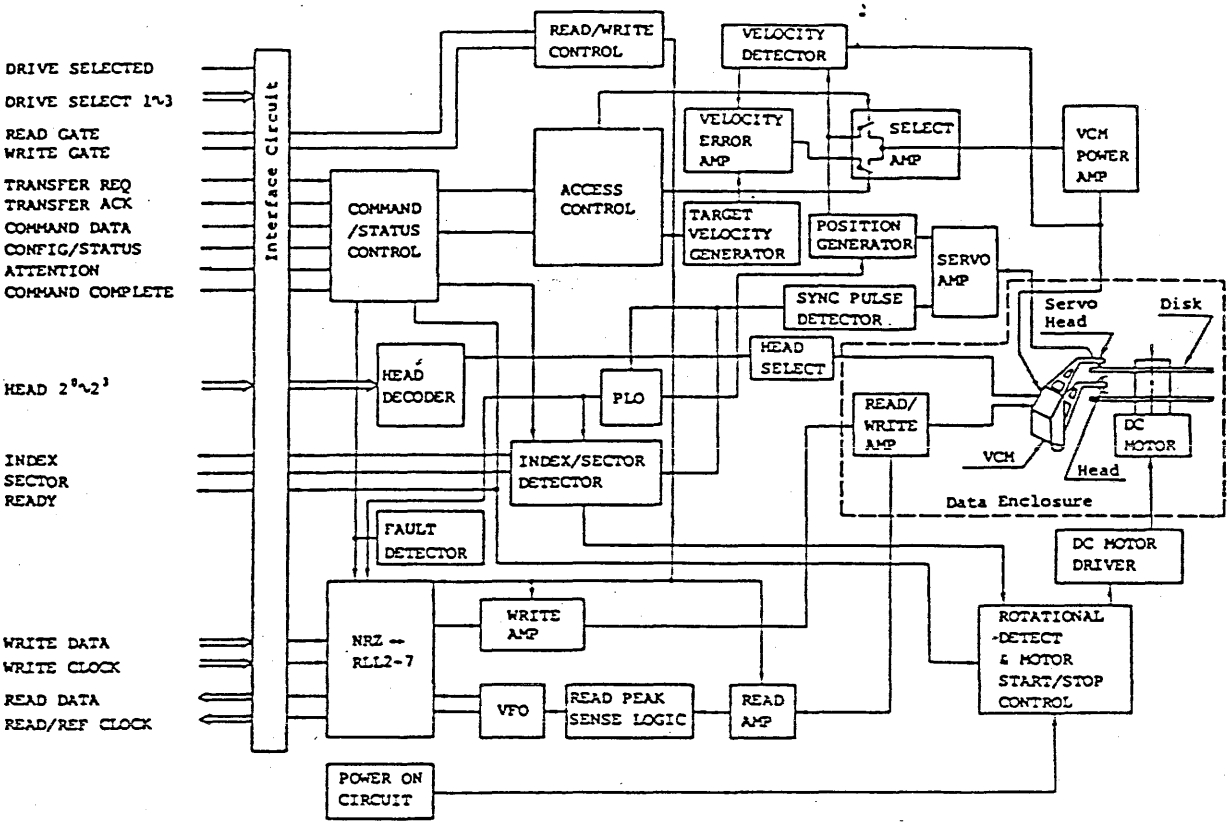


Figure 5-1 SERIAL Mode Block Diagram

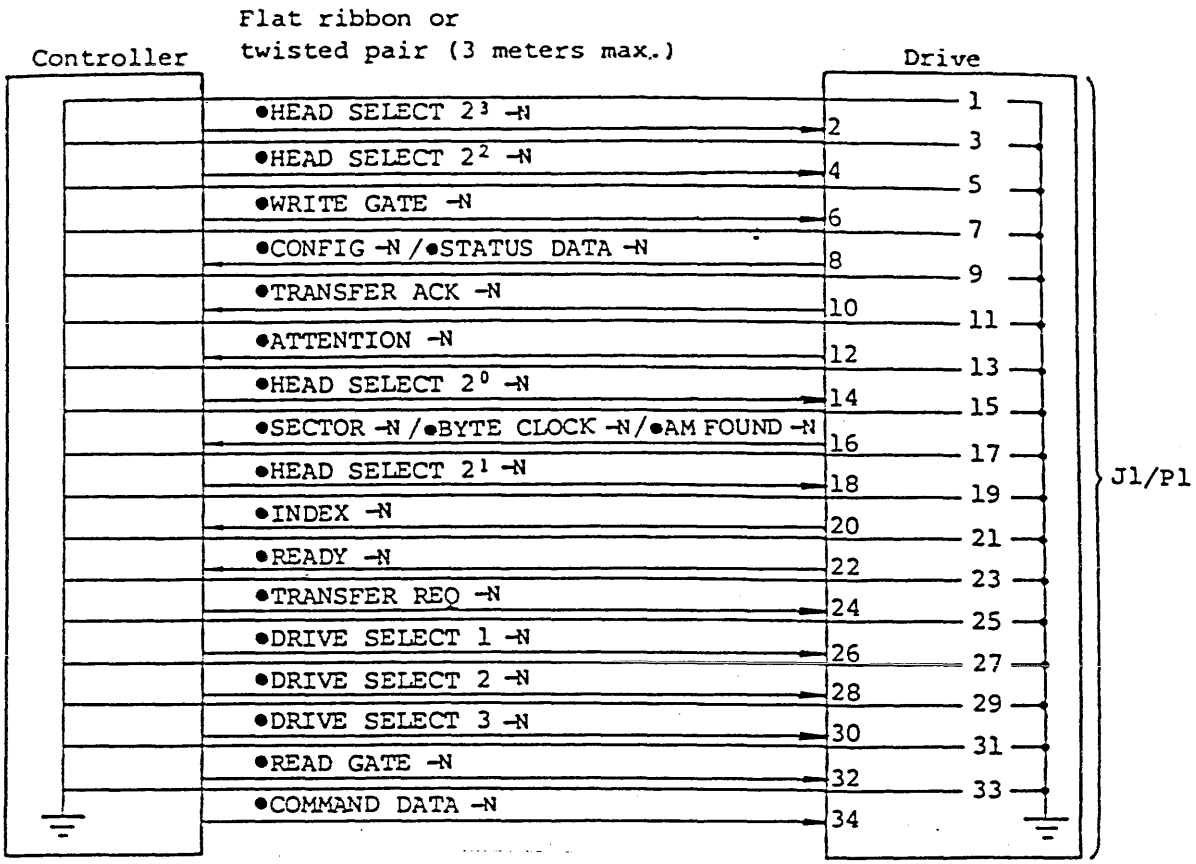


Figure 5-2 Control Cable B Signals

Table 5-1 Pinout for Control Cable B

Hitachi Signal Name	Source	Signal Pin	Ground Pin
HEAD SELECT 2^3-N	CU	2	1
HEAD SELECT 2^2-N	CU	4	3
WRITE GATE-N	CU	6	5
CONFIG-N/STATUS DATA-N	Drive	8	7
TRANSFER ACK-N	Drive	10	9
ATTENTION-N	Drive	12	11
HEAD SELECT 2^0-N	CU	14	13
SECTOR-N/BYTE CLOCK-N/ ADDRESS MARK FOUND-N	Drive	16	15
HEAD SELECT 2^1-N	CU	18	17
INDEX-N	Drive	20	19
READY-N	Drive	22	21
TRANSFER REQ-N	CU	24	23
DRIVE SELECT 1-N	CU	26	25
DRIVE SELECT 2-N	CU	28	27
DRIVE SELECT 3-N	CU	30	29
READ GATE-N	CU	32	31
COMMAND DATA-N	CU	34	33

Notes
CU: Control Unit
-N: Low true (logical "1") signal

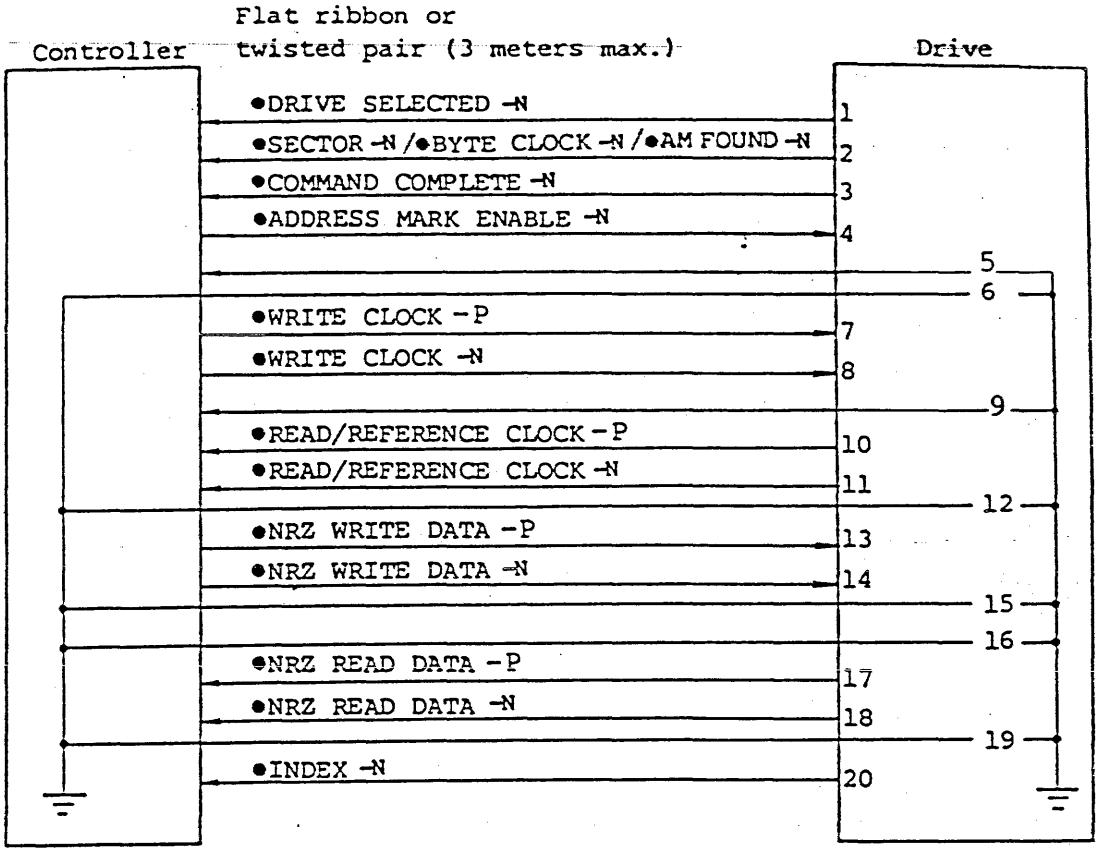


Figure 5-3 Data Cable C Signals

Table 5-2 Pinout for Data Cable C

Hitachi Signal Name	Source	Signal Pin	Ground Pin
DRIVE SELECTED-N	Drive	1	-
SECTOR-N/BYTE CLOCK-N/ ADDRESS MARK FOUND-N	Drive	2	-
COMMAND COMPLETE-N	Drive	3	-
ADDRESS MARK ENABLE-N	CU	4	5/6
WRITE CLOCK-P/N	CU	7/8	-
READ/REF CLOCK-P/N	Drive	10/11	12
NRZ WRITE DATA-P/N	CU	13/14	15/16
NRZ READ DATA-P/N	Drive	17/18	19
INDEX-N	Drive	20	-

Notes
CU: Control Unit
-N: Low true (logical "1") signal
-P/N: Differential line signal
*1: Head at a "0" level

5.1 Control Signal Descriptions

This section describes the control signals transferred between the drive and the controller. One group's source is at the controller and used to control the drive's operation, i.e., input signals. The other's source is at the drive and reports its status to the controller, i.e., output signals. Control cable B transmits all the control input signals and all the control output signals except DRIVE SELECTED and COMMAND COMPLETE which are placed on data cable C. INDEX and SECTOR signals are found on both cables.

5.1.1 Control Input Signals

The control input signals are of two types: those to be multiplexed in a multiple drive system and those intended to do the multiplexing. The control input signals to be multiplexed are WRITE GATE, READ GATE, HEAD SELECT 2^0, HEAD SELECT 2^1, HEAD SELECT 2^2, HEAD SELECT 2^3, TRANSFER REQ and COMMAND DATA. The signals to do the multiplexing are DRIVE SELECT 1, DRIVE SELECT 2, and DRIVE SELECT 3.
ADDRESS MARK ENABLE is a control input in the radial cable. It is not multiplexed.
NOTE: Any lines not used should be terminated.

5.1.1.1 DRIVE SELECT 1, 2, 3 -N

To select a drive, the controller places the address on these three lines in a binary form. DRIVE SELECT 1 is the least significant line and DRIVE SELECT 3 is the most significant line. Seven drives can be selected at maximum.

Table 5-3 lists the combinations of DRIVE SELECT 1, 2 and 3 lines and the drives selected. Figure 5-13 shows the DRIVE SELECT timing with other control signals.

DRIVE SELECT must be low when SEEK, WRITE GATE, READ GATE or STATUS CHECK command is issued.

Table 5-3 DRIVE SELECT Lines and Selected Drives

DRIVE SELECT Lines			Selected Drive Number
3	2	1	
H	H	H	NONE
H	H	L	1
H	L	H	2
H	L	L	3
L	H	H	4
L	H	L	5
L	L	H	6
L	L	L	7

Notes

H: High level, "0"
L: Low level, "1"

5.1.1.2 HEAD SELECT 2^0 2^1 2^2 2^3 -N

To select a head, the controller places the head number in a binary form on these four lines. HEAD SELECT must be low when READ GATE or WRITE GATE is activated.

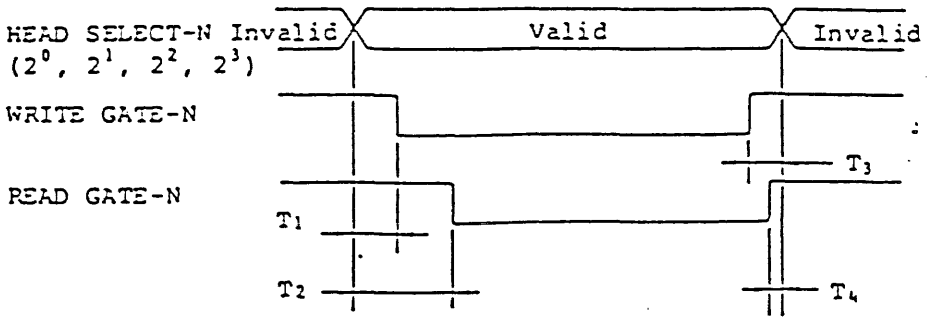
Table 5-4 lists the combinations of HEAD SELECT lines and the heads selected. Figure 5-4 shows the HEAD SELECT timing with WRITE GATE and READ GATE.

Table 5-4 HEAD SELECT Lines and Selected Heads

HEAD SELECT Lines				Selected Head Number		
2^3	2^2	2^1	2^0	DK512-8	DK512-12	DK512-17
H	H	H	H	0	0	0
H	H	H	L	1	1	1
H	H	L	H	2	2	2
H	H	L	L	3	3	3
H	L	H	H	4	4	4
H	L	H	L	-	5	5
H	L	L	H	-	6	6
H	L	L	L	-	-	7
L	H	H	H	-	-	8
L	H	H	L	-	-	9

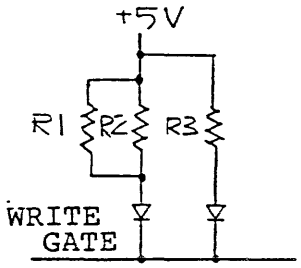
Notes

H: High level
L: Low level
-: No head.



T_1>1 μs, T_2>20 μs, T_3>1 μs, T_4>0 μs

Figure 5-4 HEAD SELECT Timing with WRITE GATE and READ GATE



R1:220Ω ± 5%
R2:330Ω ± 5%
R3:3.9KΩ± 5%
Diode:A35DHD
or Equivalent

Figure 5-5A
WRITE GATE TERMINATION

5.1.1.3 WRITE GATE-N

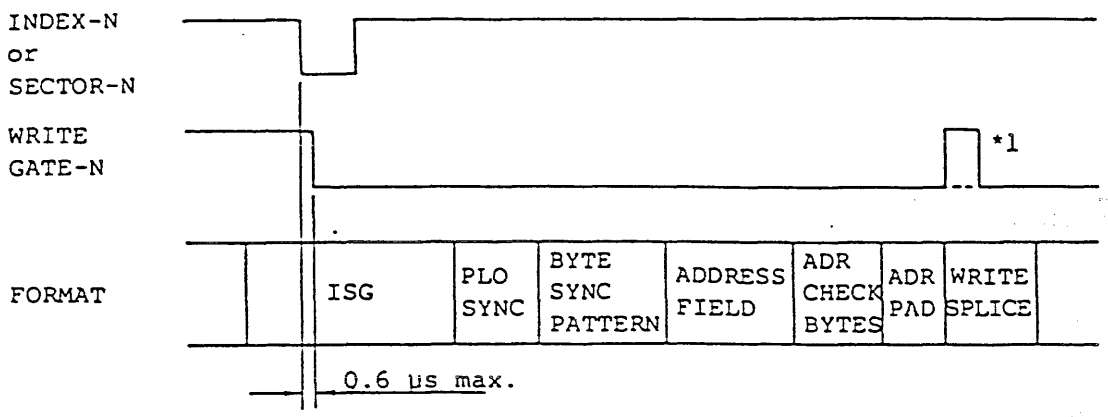
This signal, when low, causes the serialized data on the data line to be written on the disk.

If the drive responds to the controller with WRITE FAULT while WRITE GATE remains active, the entire sector being written may be invalid. The data will be lost, and must be rewritten after the fault has been cleared.

When WRITE GATE goes inactive upon detection of WRITE FAULT, try to rewrite the same data if READY, SEEK COMPLETE, WRITE FAULT or HEAD SELECT is normal.

The following timing restrictions apply to WRITE GATE (see Figures 5-5 through 5-8):

- When writing after reading, WRITE GATE must not be activated for at least 300 ns after READ GATE is inactivated.
- During succesive writes, as when formatting, WRITE GATE must be inactivated for at least one microsecond between activations.
- After WRITE GATE is inactivated, READ GATE must not be activated for at least 20 microseconds.
- After the desired data is written to the disk, one byte of dummy data must be written.



*1. WRITE GATE may remain active for the portion indicated by "...".

Figure 5-5 WRITE GATE Timing When Formatting

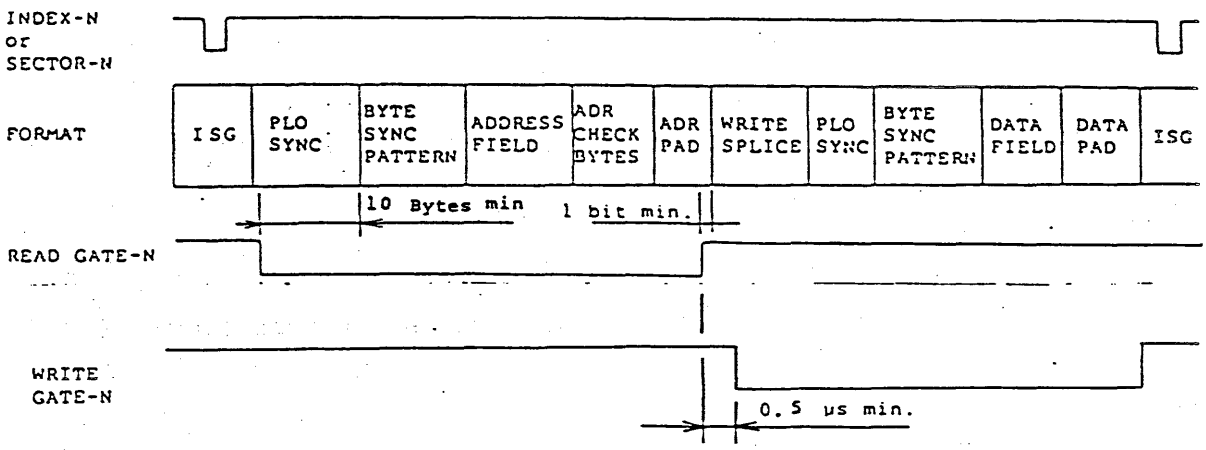


Figure 5-6 WRITE GATE Timing When Writing Data

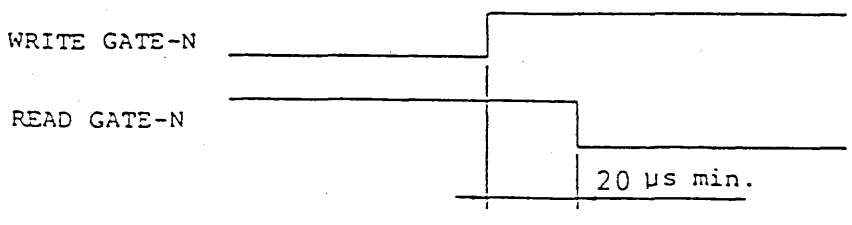


Figure 5-7 WRITE GATE Timing with READ GATE

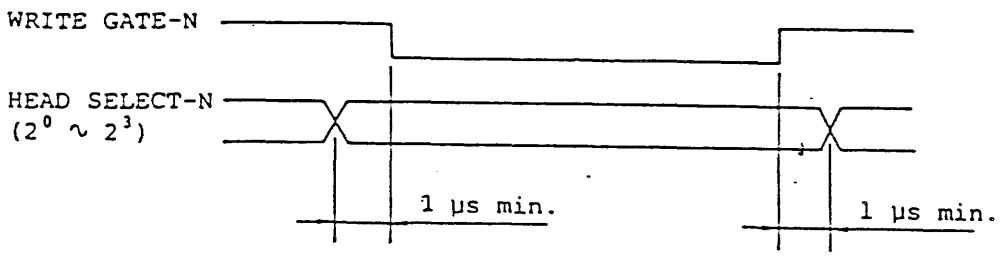


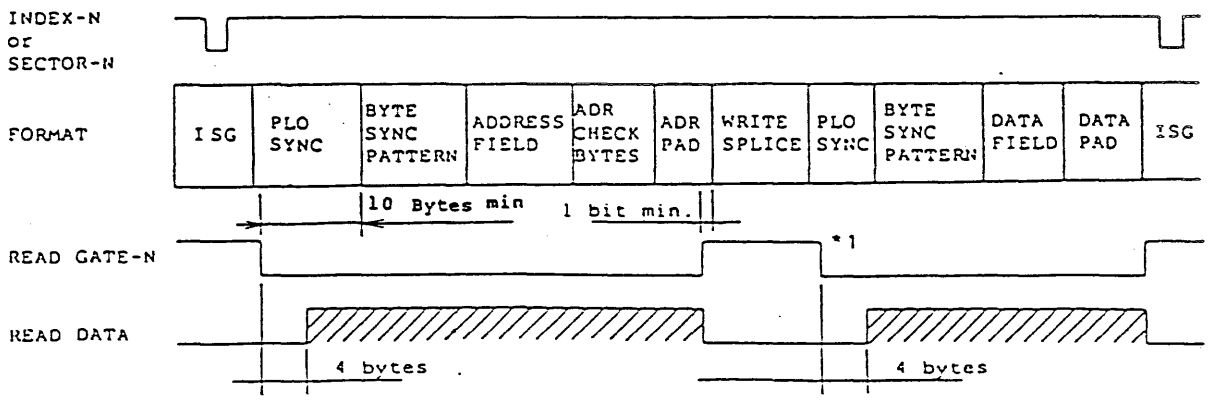
Figure 5-8 WRITE GATE Timing with HEAD SELECT

5.1.1.4 READ GATE-N

When low, READ GATE enables the read circuitry to decode the RLL 2-7 data written on the disk. The data is converted to the NRZ format and, synchronized with READ CLOCK signals, transferred bit by bit to the READ DATA line, which carries it to the controller.

These timing restrictions apply to READ GATE. Figure 5-9 shows the READ GATE timing.

- The characteristics of the drive circuit require a delay when changing heads. Data can be read without error 20 microseconds after the selection of the new head. Ignore the data for about 4 bytes after READ GATE is activated. See Figure 5-4.
- READ GATE must not be activated for 20 microseconds after WRITE GATE is inactivated. See Figure 5-7.



*1. READ GATE must be activated at least 10 bytes prior to SYNC PATTERN after WRITE SPLICE.

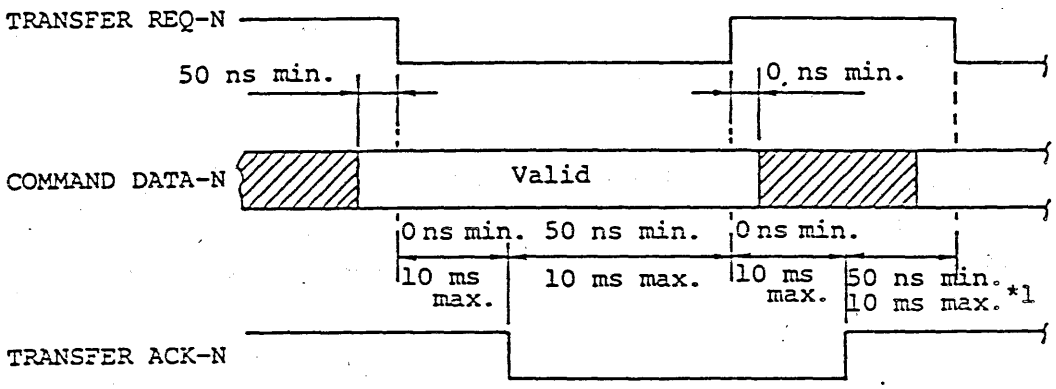
Figure 5-9 READ DATA Timing

5.1.1.5 COMMAND DATA-N

To issue a command, the controller must send out 16-bit serial data, MSB first, and a parity bit onto this line. Transfer of this serial data is controlled by the handshake protocol with TRANSFER REQ and TRANSFER ACK. Upon receiving this serial data, the drive executes a function as specified by the bit configuration. Figure 5-10 shows the COMMAND DATA transfer timing with TRANSFER REQ and TRANSFER ACK. Figure 5-11 shows the COMMAND DATA bit configuration. Table 5-5 lists the COMMAND FUNCTION definitions. The following paragraphs describe each of the command functions.

While COMMAND COMPLETE is high, the controller must not send out data.

COMMAND DATA must be high when not in use.



*1. Except for the last bit.

Figure 5-10 COMMAND DATA Transfer Timing with TRANSFER REQ and TRANSFER ACK

Most Significant Bit

Least Significant Bit

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	P
CMD FUNCTION				CMD MODIFIER				ALL ZEROS								P
CMD FUNCTION				CMD PARAMETER												P

Bit P: Parity (odd)

Figure 5-11 Command Data Word Structure

Table 5-5 COMMAND DATA Definitions

CMD FUNCTION BITS				CMD FUNCTION DEFINITION	CMD MODIFIER Bits 11-8	CMD PARAMETER Bits 11-0	STATUS/CONFIGURATION DATA
15	14	13	12				
0	0	0	0	SEEK	x	o	x
0	0	0	1	RECALIBRATE	x	x	x
0	0	1	0	REQUEST STATUS	o	x	o
0	0	1	1	REQUEST CONFIGURATION	o	x	o
0	1	0	0	UNIMPLEMENTED	-	-	-
0	1	0	1	CONTROL	o	x	x
0	1	1	0	UNIMPLEMENTED	-	-	-
0	1	1	1	TRACK OFFSET	o	x	x
1	0	0	0	UNIMPLEMENTED	-	-	-
1	0	0	1	SET BYTES PER SECTOR	x	o	x
1	0	1	0	RESERVED	-	-	-
1	1	0	0	RESERVED	-	-	-
1	1	0	1	RESERVED	-	-	-
1	1	1	0	RESERVED	-	-	-
1	1	1	1	RESERVED	-	-	-

o: Applicable x: Not applicable

Notes

1. All unused or not applicable lower order bits must be zero.

2. When receiving any "RESERVED" commad, the drive will process it as an unimplemented command.

Definitions of COMMAND DATA Bits 15, 14, 13, 12

(1) SEEK (0000)

This command causes the drive to seek to the cylinder specified with bits 0 through 11. A SEEK command restores the track offset to zero.

(2) RECALIBRATE (0001)

This command causes the head to return to cylinder 0000. A RECALIBRATE command restores the track offset to zero.

(3) REQUEST STATUS (0010)

This command requests the drive to report a 16-bit standard or vendor unique status information to the controller as specified by the command modifier bits.

- REQUEST STANDARD STATUS

  When the command modifier bits 11-8 of the REQUEST STATUS command is 0000, the drive reports the standard status to the controller. Bits 15-12 of this status do not cause ATTENTION to be asserted. Bits 11-0 cause ATTENTION to be asserted when a fault condition or change of status is set.

  Tables 5-9 through 5-11 list the response protocol and status response formats from the drive.

- REQUEST VENDER UNIQUE STATUS

  When the command modifier bits 11-8 are 0001, the drive reports a fault status as the vender unique status to the controller. When the command modifier bits 11-8 of the REQUEST STATUS command is any of 0002-1111, the drive treats that command as an unimplemented command.

(4) REQUEST CONFIGURATION (0011)

This command causes the drive to report its configuration to the controller. The configuration is defined by bits 11-8. Table 5-6 lists the combinations of COMMAND MODIFIER bits that define the drive's configuration.

Table 5-6 CONFIGURATION Definitions

COMMAND MODIFIER BITS				FUNCTION
11	10	9	8	
0	0	0	0	GENERAL CONFIGURATION OF DRIVE AND FORMAT
0	0	0	1	NUMBER OF CYLINDERS,FIXED
0	0	1	0	—
0	0	1	1	NUMBER OF HEADS
0	1	0	0	MINIMUM UNFORMATTED BYTES PER TRACK
0	1	0	1	UNFORMATTED BYTES PER SECTOR
0	1	1	0	SECTORS PER TRACK
0	1	1	1	MINIMUM BYTES IN ISG FIELD
1	0	0	0	MINIMUM BYTES PER PLO SYNC FIELD
1	0	0	1	NUMBER OF WORDS OF VENDOR UNIQUE STATUS AVAILABLE
1	0	1	0	RESERVED
		S		
1	1	1	0	VENDER IDENTIFICATION
1	1	1	1	

(5) CONTROL (0101)

This command causes the drive to perform a control operation as specified by bits 11-8. Table 5-7 lists the combinations of COMMAND MODIFIER bits that define the control functions.

Table 5-7 CONTROL Definitions

COMMAND MODIFIER BITS				FUNCTION
11	10	9	8	
0	0	0	0	RESET INTERFACE ATTENTION AND STANDARD STATUS (BITS 0-11) *1
0	0	0	1	RESERVED
0	0	1	0	STOP SPINDLE MOTOR (OPTIONAL) *2
0	0	1	1	START SPINDLE MOTOR (OPTIONAL) *2
0	1	0	0	RESERVED
0	1	0	1	RESERVED
0	1	1	0	RESERVED
0	1	1	1	RESERVED
1	x	x	x	RESERVED

*1. This reset function becomes effective provided the fault condition has been cleared. The VENDOR UNIQUE STATUS (bits 0-5) is also reset if the faule condition has been cleared.

*2. Selectable with option set jumper switch. If the jumper switch is set to select motor start/stop option, the spindle motor starts rotating by the command. If the jumper switch is set not to select the option, the spindle motor starts rotating by the power on.

(6) TRACK OFFSET (0111)

This command causes the drive to perform a track offset in the amount specified by bits 11-8. Table 5-8 lists the combinations of COMMAND MODIFIER bits that define the TRACK OFFSET functions.

Table 5-8 TRACK OFFSET Definitions

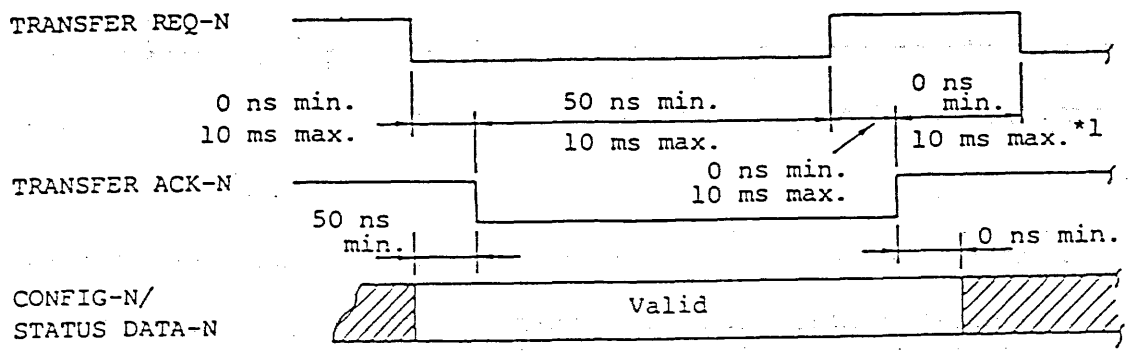
COMMAND MODIFIER BITS				FUNCTION
11	10	9	8	
0	0	0	0	RESTORE OFFSET TO 0
0	0	0	1	RESTORE OFFSET TO 0
0	0	1	0	POSITIVE OFFSET 1
0	0	1	1	NEGATIVE OFFSET 1
0	1	0	0	POSITIVE OFFSET 2
0	1	0	1	NEGATIVE OFFSET 2
0	1	1	0	POSITIVE OFFSET 3
0	1	1	1	NEGATIVE OFFSET 3
1	x	x	x	RESERVED

(7) SET UNFORMATTED BYTES PER SECTOR (1001)

This command requests the drive to set the number of unformatted bytes per sector indicated in bit 11-0. This command is valid only if the drive is configured to be in the drive hard sector mode. Bytes per sector function is able to be excuted by jumper switch on PC board. This command has priority to the jumper switch.

5.1.1.6 TRANSFER REQUEST-N

This signal, in conjunction with the TRANSFER ACK signal, controls the handshake protocol for transferring commands and configuration/status information. Figure 5-12 shows the handshake timing.



*1. Except on last bit.

Figure 5-12 TRANSFER REQUEST and TRANSFER ACKNOWLEDGE Timing

5.1.2 Control Output Signals

These signals' source is at the drive and sent to the controller to report the drive's status.

5.1.2.1 DRIVE SELECTED-N

This ungated signal goes low when the drive is selected. The controller must not send any control signal for at least 250 ns after receiving this signal, and must inactivate the control at least 250 ns before inactivating DRIVE SELECT. Figure 5-13 shows the DRIVE SELECTED timing with DRIVE SELECT and control signals.

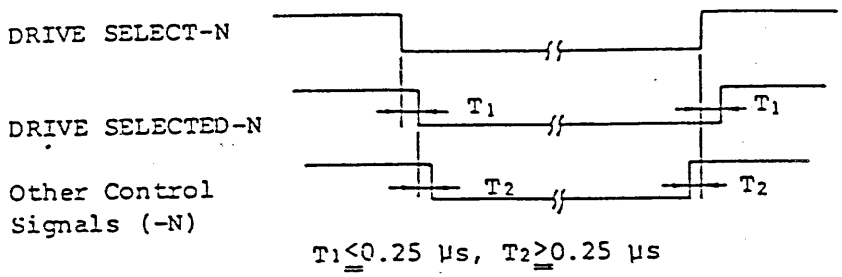


Figure 5-13 DRIVE SELECTED Timing with DRIVE SELECT and Control Signals

5.1.2.2 READY-N

This signal, when low, indicates that the drive is selected and that the disks are up to speed. When both READY and COMMAND COMPLETE are low, the drive is ready for read, write and seek operations. When READY is high, the controller must not command the drive to seek, write or read.

Within 30 seconds of power on, READY goes low. This signal stays low while the drive is performing a seek or changing heads, as long as the drive is selected. When disk rotation is abnormal in the drive, READY goes high. When this signal is high, the drive does not seek or write. Figure 5-14 shows the READY timing.

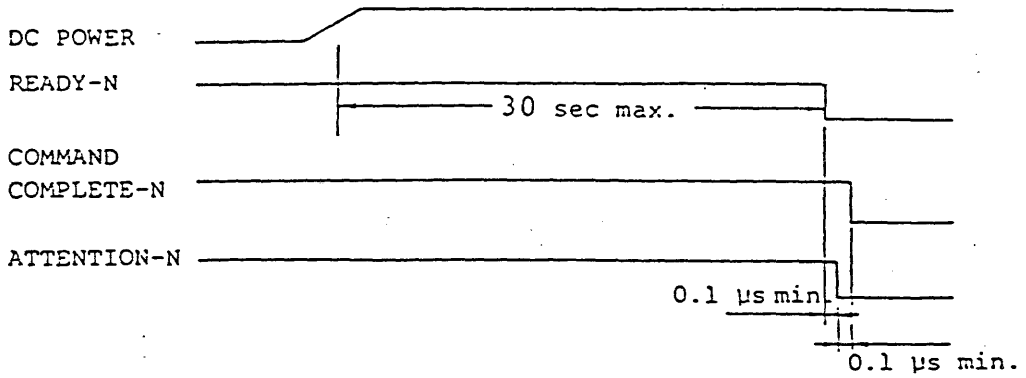


Figure 5-14 READY Timing

5.1.2.3 CONFIGURATION/STATUS DATA-N

When requested from the controller, the drive places 16-bit serial data and a parity bit on this line to report its configuration or status to the controller. Transfer of CONFIGURATION/STATUS data is controlled by the handshake protocol with TRANSFER REQ and TRANSFER ACK signals. MSB is transferred first.

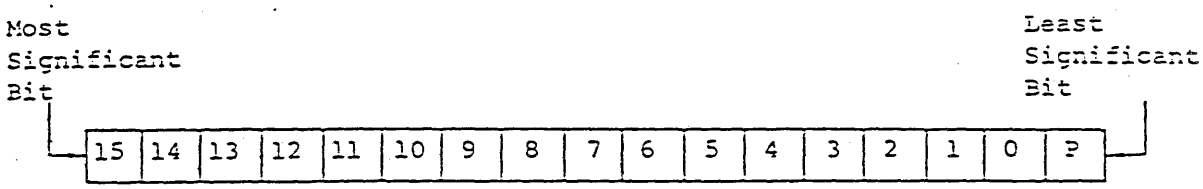


Figure 5-15 CONFIGURATION/STATUS DATA Configuration

(1) CONFIGURATION RESPONSE Bits

In response to the REQUEST CONFIGURATION command, the drive sends a 16-bit data of configuration information to the controller.

When bits 11-8 of the COMMAND MODIFIER are 0000, the drive sends the status information of General Configuration shown in Table 5-9. Otherwise the drive sends a configuration information as specified by the COMMAND MODIFIER bits as shown in Table 5-10.

Table 5-9 General Configuration Response Bits

BIT POSITION	FUNCTION	BIT VALUE
15	TAPE DRIVE	0
14	FORMAT SPEED TOLERANCE GAP REQUIRED	0
13	TRACK OFFSET OPTION AVAILABLE	1
12	DATA STROBE OFFSET OPTION AVAILABLE	0
11	RESERVED ROTATIONAL SPEED TOLERANCE IS > 0.5%	0
10	TRANSFER RATE > 10 MHz	0
9	TRANSFER RATE > 5 MHz < 10 MHz	1
8	TRANSFER RATE < 5 MHz	0
7	REMOVABLE CARTRIDGE DRIVE	0
6	FIXED DRIVE	1
5	Spindle Motor Control Option Implemented	*1
4	HEAD SWITCH TIME > 15 μs	0
3	RLL ENCODED (NOT MFM)	1
2	CONTROLLER SOFT SECTORED (ADR MARK)	*1
1	DRIVE HARD SECTORED (SECTOR PULSES)	*1
0	CONTROLLER HARD SECTORED (BYTE CLOCK)	*1

*1 Selectable with Option SEL jumper switches

Table 5-10 Specific Configuration Response Bits

COMMAND MODIFIER BITS				CONFIGURATION RESPONSE	BIT VALUE(HEX)		
					DK512 -8	DK512 -12	DK512 -17
11	10	9	8				
0	0	0	1	NUMBER OF CYLINDERS, FIXED	0337	0337	0337
0	0	1	0	NUMBER OF CYLINDERS, REMOVABLE	0000	0000	0000
0	0	1	1	NUMBER OF HEADS BITS 15-8: REMOVABLE DRIVE HEADS BITS 7-0 : FIXED HEADS	 00 05	 00 07	 00 0A
0	1	0	0	MINIMUM UNFORMATTED BYTES PER TRACK	51D0	51D0	51D0
0	1	0	1	UNFORMATTED BYTES PER SECTOR (HEAD SECTOR ONLY)	*1	*1	*1
0	1	1	0	SECTORS PER TRACK (DRIVE HARD SECTOR ONLY) BITS 15-8: SPARE BITS 7-0 : SECTORS PER TRACK	 00 *1	 00 *1	 00 *1
0	1	1	1	MINIMUM BYTES IN ISG FIELD BITS 15-8: ISG BYTES AFTER INDEX BITS 7-0 : BYTES PER ISG	 0C 1D	 0C 1D	 0C 1D
1	0	0	0	MINIMUM BYTES PER PLO SYNC FIELD BITS 15-8: SPARE BITS 7-0 : BYTES PER PLO SYNC FIELD	 00 0B	 00 0B	 00 0B
1	0	0	1	NUMBER OF WORDS OF VENDER UNIQUE STATUS AVAILABLE BITS 15-4: SPARE BITS 3-0 : NUMBER OF VENDOR UNIQUE STATUS WORDS	 00 01	 00 01	 00 01
1	0	1	0	RESERVED	—	—	—
5							
1	1	1	0				
1	1	1	1	VENDER IDENTIFICATION	0500	0500	0500

*1. Selectable with jumper switches or set unformatted bytes per sector command.

(2) STATUS RESPONSE Bits

In response to the REQUEST STATUS command, the drive sends 16-bit data of status information to the controller. When the COMMAND MODIFIER bits 11-8 are 0000, the drive sends the standard status information shown in Table 5-11. When they are 0001, the drive reports a fault status shown in Table 5-12 and activates ATTENTION signal.

Table 5-11 Standard Status Response Bits

BIT POSITION	FUNCTION	ATT.
15	RESERVED*2	-
14	REMOVABLE MEDIA NOT PRESENT*2	0
13	WRITE PROTECTED, REMOVABLE MEDIA*2	0
12	WRITE PROTECTED, FIXED MEDIA	0
11	RESERVED*2	-
10	RESERVED*2	-
9	1=Spindle Motor Stopped by Stop command	0
	1=Spindle Motor Stopped for other	1
8	POWER ON RESET CONDITIONS EXIST (RECONFIGURATION OR START SPINDLE MOTOR COMMAND MAY BE REQUIRED)	1
7	COMMAND DATA PARITY FAULT	1
6	INTERFACE FAULT	1
5	INVALID OR UNIMPLEMENTED COMMAND FAULT	1
4	SEEK FAULT	1
3	WRITE GATE WITH TRACK OFFSET FAULT	1
2	VENDOR UNIQUE STATUS AVAILABLE	-
1	WRITE FAULT*1	1
0	REMOVABLE MEDIA CHANGED*2	1

Notes

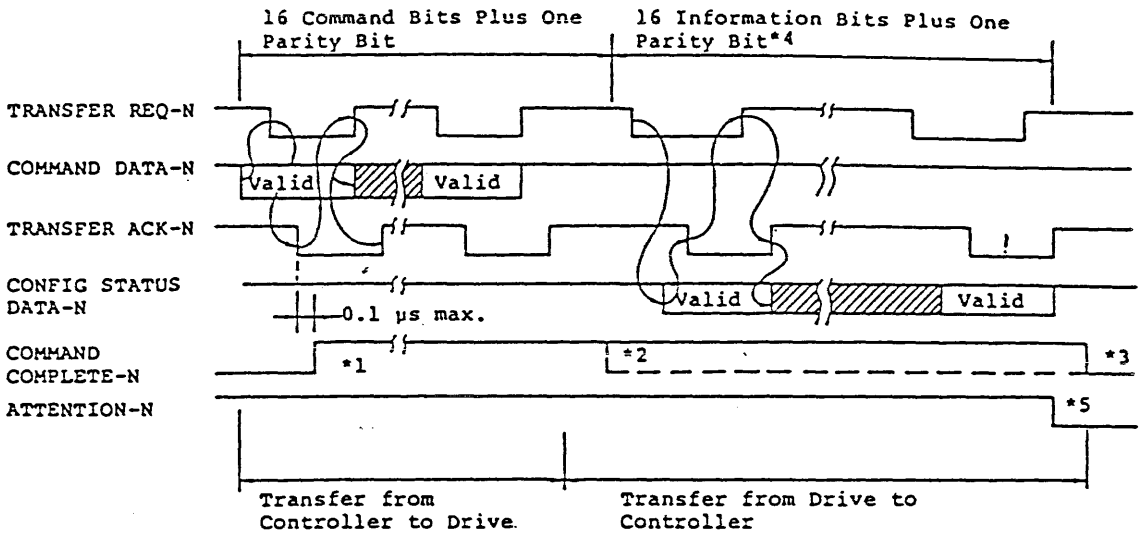
*1. WRITE FAULT goes true when:

a) No head selected or multiple heads selected while WRITE GATE is activated.
b) Wrtie current does not flow or bit inversion does not occur while WRITE GATE is activated.
c) Write current flows or bit inversion occurs when WRITE GATE is inactive.
d) WRITE GATE and READ GATE are activated simultaneously.
e) The head is off the track during a write.

*2 The DK512 drive respond with "0" to the controller.

Table 5-12 Specific Status Response Bits

BITS POSITION	FUNCTION	DEFINITION
15	RESERVED	-
14	RESERVED	-
13	RESERVED	-
12	RESERVED	-
11	RESERVED	-
10	RESERVED	-
9	RESERVED	-
8	RESERVED	-
7	RESERVED	-
6	RESERVED	-
5	RESERVED	-
4	WRITE ERROR 3	WRITE GATE activated while write protected.
3	WRITE ERROR 2	. Write current does not flow or bit inversion does not occur while WRITE GATE is activated.
2	WRITE ERROR 1	. WRITE GATE received when two or more heads are selected simultaneously. . Abnomal index pattern detected. . Position signal abnormal during a write. . READ GATE and WRITE GATE are activated simultaneously.
1	STATUS ERROR 2	WRITE GATE is activated during a seek.
0	STATUS ERROR 1	The drive is commanded to read, write or seek when not ready.



Notes

*1. COMMAND COMPLETE goes high for all commands to the drive.

*2. COMMAND COMPLETE goes low upon completion of a command execution.

*3. COMMAND COMPLETE goes low upon completion of a CONFIGURATION/STATUS data transfer.

*4. Applicable for all REQUEST STATUS/CONFIGURATION commands.

*5. If an error is detected during a command execution, ATTENTION goes low at least 100 ns before COMMAND COMPLETE goes low.

Figure 5-16 Typical Serial Operations

5.1.2.4 TRANSFER ACKNOWLEDGE-N

This signal, in conjunction with TRANSFER REQUEST, controls the handshake protocol during command and configuration status transfers. See Figure 5-12.

5.1.2.5 ATTENTION-N

This signal is activated when a fault condition or change of status occurs. When ATTENTION is low, the drive is inhibited from writing. ATTENTION can be reset with the RESET INTERFACE ATTENTION command provided the fault condition has been cleared.

5.1.2.6 INDEX-N

This signal is a timing pulse which goes low once each revolution to indicate the beginning of a data track. The leading edge or high to low transition of this signal is the start of a track. This pulse is available on both control (J1) and data (J2) cables. On J1 cable, INDEX is gated by DRIVE SELECT, while on J2 cable, it is not gated.

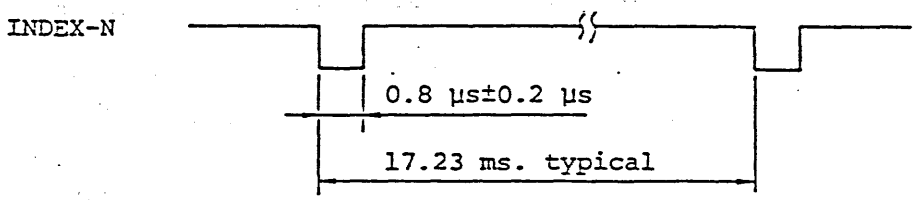


Figure 5-17 INDEX Timing

5.1.2.7 SECTOR-N/BYTE CLOCK-N/AM FOUND-N

There tree signals are mutually exclusive and therefore may share this line. The signal that is used is determined by NRZ data trausfer control implementation. These signals are available on both control J1 (gated) and data J2 (ungated).

1. SECTER-N (Drive Hard Sector)

This signal is a timing pulse which goes low at the beginning of each sector except sector 0 which is indicated by the INDEX pulse. The leading edge of this signal is the start of a sector. The number of data bytes per sector is selectable in 1-byte increments by setting jumper switches on the drive. Figure 5-18-a shows SECTOR Timing.

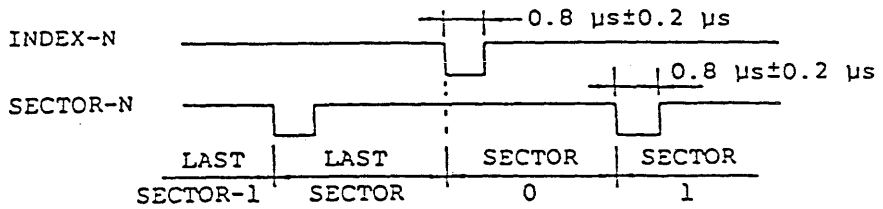
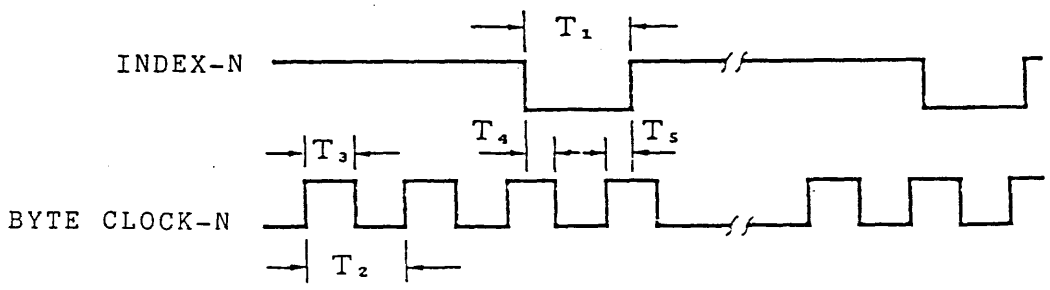


Figure 5-18-a SECTOR Timing with INDEX

2. BYTE CLOCK-N (Controller Hard Sector)

This signal occurs once per every eight Reference clock periods. This signal is provided for the controller to count desired number of Byte clocks to determine the secter sige and beginning sector locations. This clock does not have fixed phase relationship to the recorded data. Figure 5-18-b shows BYTE CLOCK Timig.

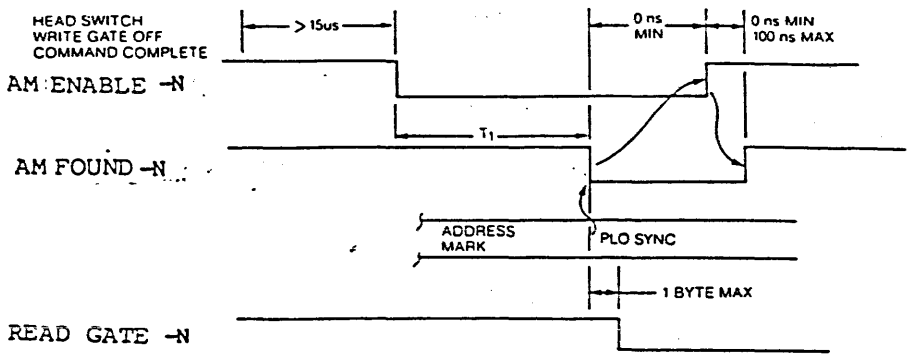


$T_1 = 0.8 \pm 0.2\mu s$
$T_2 = T_1$
$T_3 = T_1/2$
$T_4 = T_5 = T_{3/2}$

Figure 5-18-b BYTE CLOCK Timing

3. ADDRESS MARK FOUND-N (Controller Soft Secter)

This signal indicates the detection of the end of an address mark. Figure 5-18-c shows ADDRESS MARK FOUND Timing.



T1=24 BIT TIMES MINIMUM

Figure 5-18-C

5.1.2.8 COMMAND COMPLETE-N

This ungated status signal goes high in either of these cases:

- During initial recalibration sequence at power on.
- During command sequence after reception of the first bit of a command data. COMMAND COMPLETE stays false during the entire command sequence.

Figure 5-16 shows the timing.

5.2 Data Signal Descriptions

Data and clock signals are transferred over differential pairs. These signals are provided at J2/P2 connectors on all drives. There are four differential pairs: NRZ WRITE DATA, NRZ READ DATA, WRITE CLOCK and READ/REFERENCE CLOCK.

5.2.1 Data Input Signals

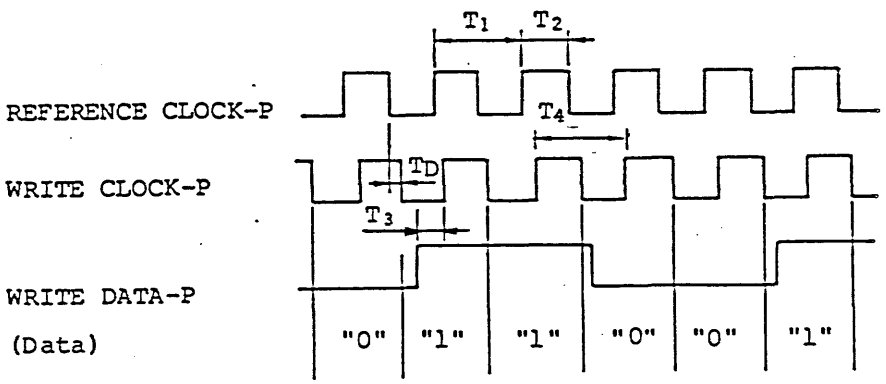
5.2.1.1 NRZ WRITE DATA

The controller places NRZ data on this differential pair that transmits it to the drive for recording on the disk. The data is generated in the controller in an NRZ format and sent out to the drive, synchronized with WRITE CLOCK pulses. Drive circuits convert it from NRZ format and write it on the disk in RLL 2-7 format.

5.2.1.2 WRITE CLOCK

The controller must transmit this timing pulse at the bit data rate for synchronization of WRITE DATA. The signal is derived from the REFERENCE CLOCK and its timing is controlled by the controller. The controller must initiate its transmission at least 250 ns before activating WRITE GATE.

Figure 5-19 shows REFERENCE CLOCK and WRITE CLOCK signals.



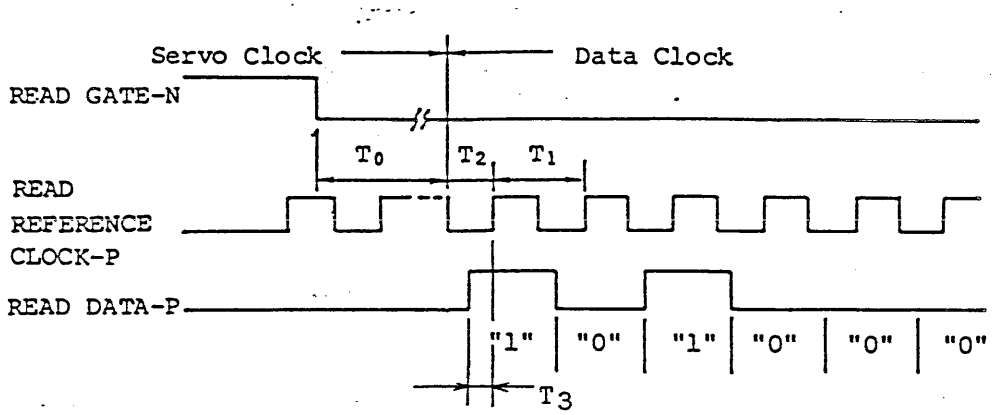
T_1 = 102.8 ns ± 8 ns
T_2 = $T_1/2$
T_3 = $T_4/2$ ± 20 ns
T_D = $2T_1$
T_4 = 102.8 ± 8 ns

Figure 5-19 WRITE DATA and Clock Timing

5.2.2 Data Output Signals

5.2.2.1 NRZ READ DATA

The drive places NRZ data on this differential pair for transmission to the controller. The data written on the disk in RLL 2-7 format is decoded into NRZ format through the Variable Frequency Oscillator (VFO) and Data Separator circuits and clocked by the READ CLOCK signal for transmission. Data transfer is initiated after the VFO circuit is stabilized, so the controller must ignore the data for 4 bytes after activating READ GATE.



T_0 = 4 bytes
T_1 = 102.8 ns $\pm$ 10 ns
T_2 = T1/2 $\pm$ 10 ns
T_3 = T1/2 $\pm$ 15 ns

Figure 5-20 READ DATA and Clock Timing

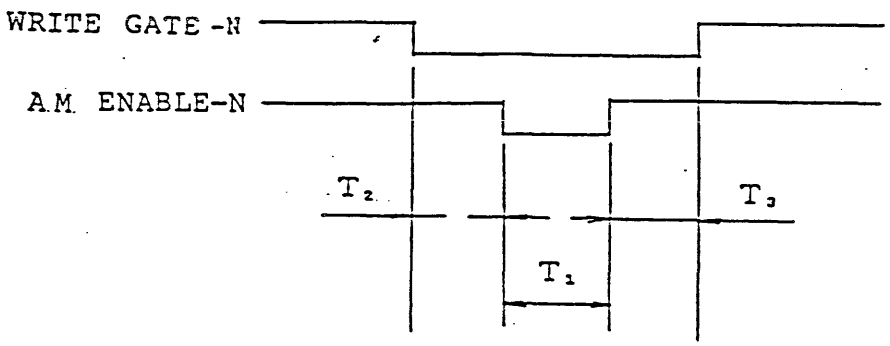
5.2.2.2 READ/REFERENCE CLOCK

The drive transmits this timing pulse continuously for the controller to discriminate read data. When READ GATE is active, this signal is supplied by the Variable Frequency Oscillator (VFO) circuit synchronized with a read data. When READ GATE is inactive, it is a servo clock or REFERENCE CLOCK. The transition from servo clock to data clock is completed in 4 bytes after READ GATE goes low.

Figure 5-20 above shows the timing.

2.2.3 ADDRESS MARK ENABLE-N

This optional signal, when actie with WRITE GATE, Causes an Address Marks to be written. ADDRESS MARK ENABLE shall be active for 24 bit times.
ADDRESS MARK ENABLE, when active without WRITE GATE or READ GATE, causes a search for Address Marks.



T_1 = 24 Bit times
$T_2 = T_3$ = 100ns min

Figure 5-18-c WRITE ADDRESS MARK Timing

6. FORMAT

This section provides a recommended track format to be used when integrating the DK512 into a system. The number of data bytes per sector is selectable in 1-byte increments by jumper switches. See Paragraph 5.1.2.7, "SECTION-N."

Each sector consists of three functional areas; Intersector Gap, Address and Data. Intersector gap and address areas, which must be set aside for write splices and synchronization, are kept to a minimum for higher track efficiency.

There are 20,944 bytes per track. To ensure high drive reliability, an Error Correcting Code (ECC) should be used as the error check code in data fields. The ECC requires seven bytes to prevent correction error. Paragragh 6.2.3.5 gives a suitable polynomial.

6.1 Fixed Sector Format

Figure 6-1 shows a sample fixed sector format. Note the minimum number of synchronization bytes stated in the figure. They are required to synchronize the Phase Locked Oscillator (PLO) with the data. The overhead (non-data bytes) shown in Figure 6-1 is 71 per sector. Given the desired data-bytes/sector, the following calculation can be made:

$$\text{Number of sectors} = \frac{\text{Total bytes/track}}{\text{bytes/sector}} = \frac{20{,}944}{\text{bytes/sector}}$$

For example, 256 data-bytes/sector requires

$$\frac{20{,}944}{256+71} = 64 \text{ sectors/track}$$

The efficiency of the scheme is $\frac{256 \times 64}{20{,}944} = 78.2\%$

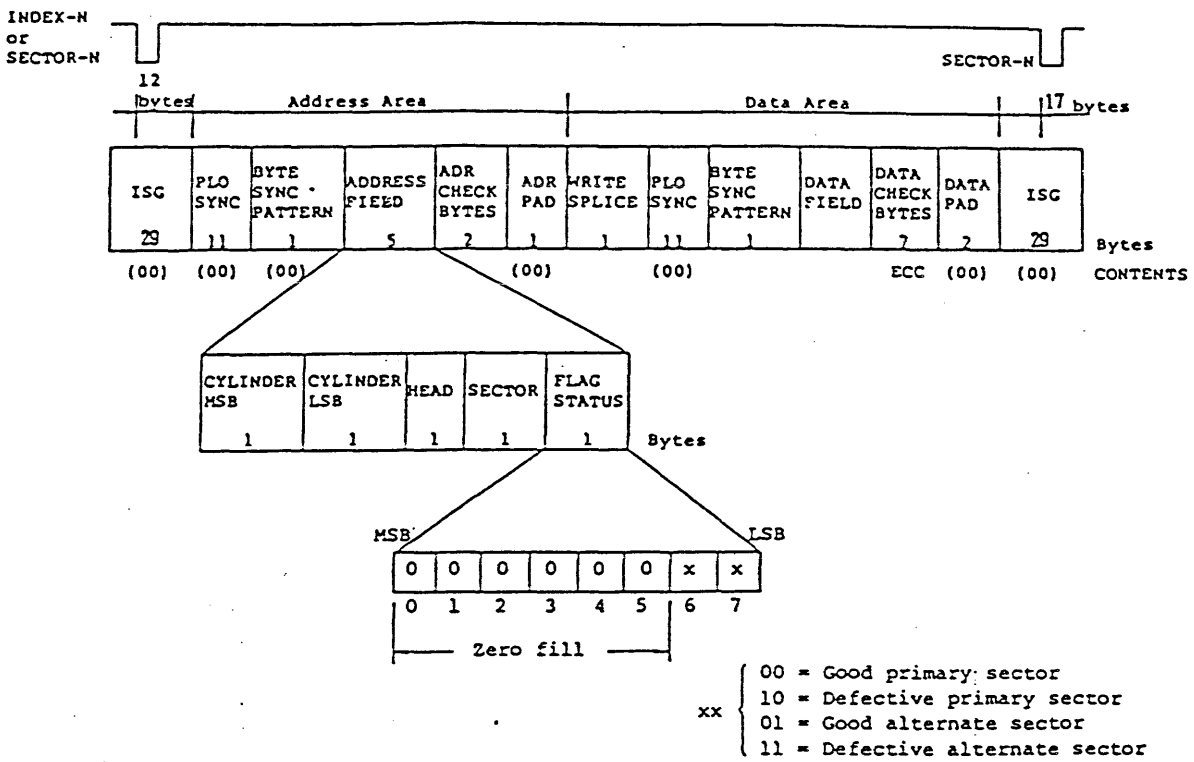


Figure 6-1 Fixed Sector Format

6.2 Track Field Descriptions

The following provides additional information on the field lengths and field contents defined in Figure 6-1.

6.2.1 INTERSECTOR GAP (ISG)

This is an area required by the drive to switch the heads from write to read, i.e., write-to-read recovery period. The size is determined from the configuration data.

6.2.2 Address Area

The address area defines the track and sector locations. The following fields are required.

6.2.2.1 PLO SYNC

This field requires at least 11 bytes for the drive to stabilize the variable frequency oscillator (VFO) circuit. In this area, read data is synchronized with the VFO.

If the ID field has a media defect, it is recommended that 64 bytes of 00_{16} be added to the PLO SYNC field, and that the physical (primary) sector be abandoned. The logical (alternate) sector may be on one of the reserved tracks. The controller must keep track of the relationship between physical and logical addresses.

6.2.2.2 BYTE SYNC PATTERN

The field is filled with 1 bits to mark the beginning of an address or data area.

6.2.2.3 ADDRESS FIELD

This field consists of the following five bytes. High-order bits unused in CYLINDER MSB, CYLINDER LSB, HEAD and SECTOR bytes are filled with 0s.

(1) CYLINDER MSB

Most significant byte of a cylinder number.

(2) CYLINDER LSB

Least significant byte of a cylinder number.

(3) HEAD

Head number.

(4) SECTOR

Sector number.

(5) FLAG STATUS

Sector data field condition.

6.2.2.4 ADDRESS CHECK BYTE

A 2-byte CRC polinomial X16 + X12 + X5 + 1 is used, where the initial value is FF.

6.2.2.5 ADDRESS PAD.

This 2-byte additional area is required by the drive for proper recording and recovery of the address area.

6.2.3 Data Area

The data area consists of the following fields:

6.2.3.1 WRITE SPLICE

This area must be at least one-byte long so that the write driver can reach to the recording amplitude sufficient to ensure data recovery.

6.2.3.2 PLO SYNC

See 6.2.2.1 above.

6.2.3.3 BYTE SYNC PATTERN

See 6.2.2.2 above.

6.2.3.4 DATA FIELD

In this area the user can record his data.

6.2.3.5 DATA CHECK BYTES

The following 7-byte ECC polynomial is recommended to improve the error correcting capability.

$$(X22 + 1)\ (X11 + X9 + X7 + X6 + X5 + X + 1)$$
$$(X12 + X11 + X10 + X9 + X8 + X7 + X6 + X5 + X4 + X3 + X2 + X + 1)$$

6.2.3.6 DATA PAD

This 2-byte additional area is required for proper recording and recovery of the data area.

6.3 Bytes/Sector and Sectors/Track Selection

Selection is made with jumper plugs on the DK512 PC assembly. Table 6-1 lists jumper plugs used for setting the number of bytes per sector. Each plug represents a power of 2, from 2^0 (or 1) to 2^{13} (or 8192) bytes/sector, representing 2-byte increments. The Service Manual has detailed instructions.

Table 6-1 Bytes/Sector Jumper Plugs

Jumper Plug	No. of Bytes	Jumper Plug	No. of Bytes
JP22-1	1	JP22-8	128
JP22-2	2	JP32-11	256
JP22-3	4	JP32-10	512
JP22-4	8	JP32-9	1024
JP22-5	16	JP32-8	2048
JP22-6	32	JP32-7	4096
JP22-7	64	JP32-6	8192

The number of sectors is determined in either of the following ways:

(a) Given the number of bytes/sector:

Example: 583 bytes/sector are required:

$$\text{Number of sectors} = \frac{\text{Total bytes/track}}{\text{bytes/sector}} = \frac{20{,}944}{583}$$

$$= 35 \text{ sectors/track,}$$
rounded to the next higher integer

Each track will consist of 35 sectors of 583 bytes each and one sector of 539 bytes.

Install the following plugs:

JP32-10 JP22-7 JP22-3 JP22-2
512 + 64 + 4 + 2 = 582

An extra count is added when the byte counter resets, giving the required 583 bytes/sector.

(b) Given the number of sectors/track:

Example: 32 sectors/track are required:

$$\text{Bytes/sector} = \frac{\text{Total bytes/track}}{\text{sectors/track}} = \frac{20,944}{32}$$

$$= 654 \text{ bytes}$$

Install the following plugs:

JP32-10		JP22-8		JP22-4		JP22-3		JP22-1	
512	+	128	+	8	+	4		1	= 653

An extra count is added when the byte counter resets, giving the required 651 bytes/sector.

6.4 Media Defects and Logging

This section defines defects precisely, and gives the factory formats used to record them. Table 2-1 shows the allowable number of defects for each model.

Media defects are logged at the factory during a lengthy test which includes operation at low and high temperatures, low and high voltages, and worst-case seek algorithms. Media defects lengths and positions are written on the disk in a format that can be read with either fixed sector or variable sector controllers. In addition, a flaw map is included on the test data sheet shipped with each drive. For each defect, the flaw map lists the cylinder number, head number, number of bytes from index, and bit length.

Difect information for DK512 unit is recorded in sector 0 of the maximum cylinder and repeated on maximum cylinder minus 8 (ESDI Defect List) and 0 cylinder (Option Controller Defect List) at shipment.

6.4.1 Defect List Format

1. ESDI Defect List

Figure 6-2 shows the Defect List Format. The defect list resides on Sector 0 of the maximum cylinder and is repeated on the maximum cylinder minus 8 for redundancy against possible errors on the maximum cylinder. Sector 0 of each surface contains the defects list for that surface.

The data field of this sector has the format shown with 2 bytes of CRC ($X^{16} + X^{12} + X^5 + 1$):

- Defect locations are 5 bytes long: Cylinder MSB, Cylinder LSB, Byte Count MSB, Byte Count LSB and Error Length in bits.
- The start of the actual defect is off by up to 7 bits due to the one-byte resolution.
- The end of the defect list for each surface is indicated by 5 bytes of 1s in the defect location field or the end of the sector.
- The CRC Check bytes are used.
- Byte count is the number of bytes from INDEX.

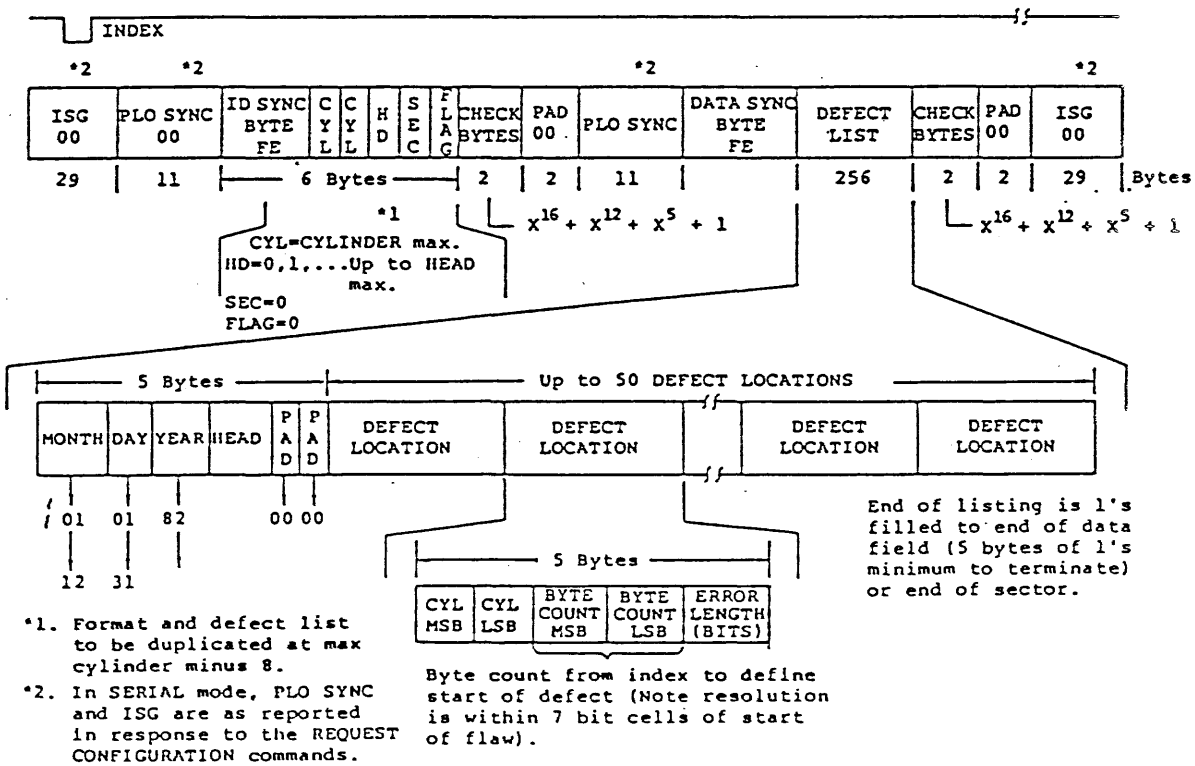


Figure 6-2 ESDI Defect List Format

2. Option Controller Defect List

Bad spot (defect) information for DK512 unit is recorded in all tracks of cylinder #0 at shipment. In order to perform initialization of disk units easily and with less manual operations, it is possible to utilize the prewritten bad spot information and to manage bad spots. Recording format of bad spot information is as follows:

(1) Sector #0 to #5 of each track in cylinder #0 contains identical bad spot information.

(2) Data format is same as previous section 1 and bad spot information is written into its data fields.

(3) Model name "DK512-XX" is written in byte address #0 to #7 of sector #0 and next to this, unit serial number is written in byte address #8 to #14. These are written by using ASCII code. Byte address #15 is "00".

(4) Byte address #16 to #23 shows number of total bad spots for the unit.

(5) Bad spot information is written as 8 bytes data per each bad spot in the area starting byte address #24 of sector #0.

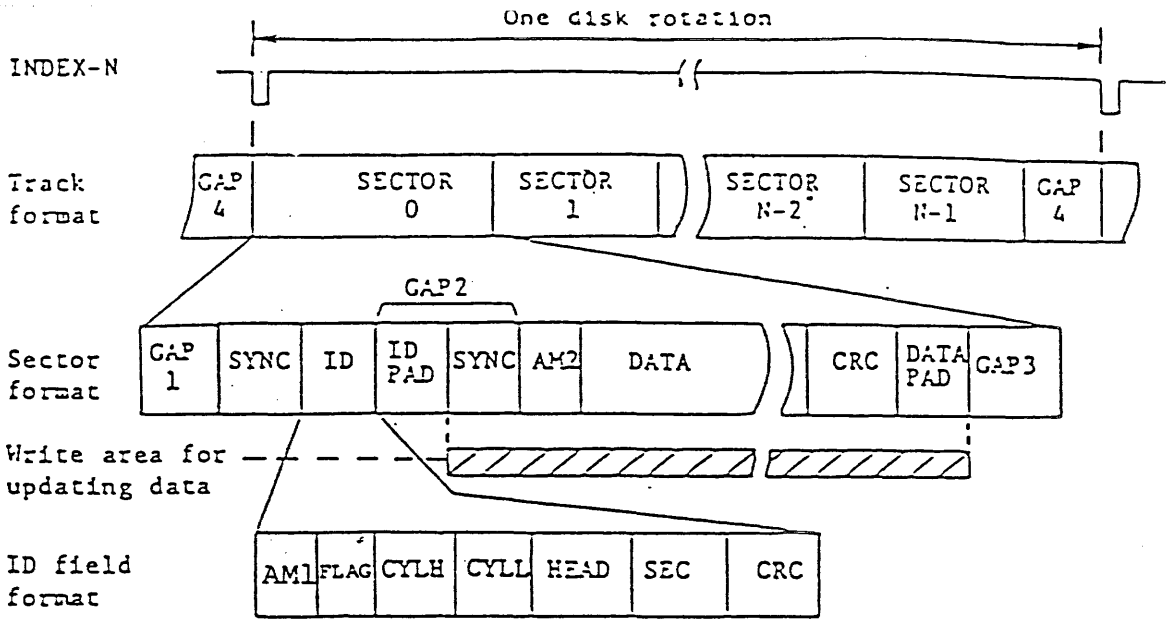
(6) Contents of 8 bytes data for bad spot information are as follows;

- Cylinder Address#; 2 bytes length (former byte indicates more than #256)
- Head Address#; 1 byte length
- Sector Address#; 1 byte length
- Position; 2 bytes length, indicates the leading position of bad spot from Index measured by bytes length. The first byte just after Index is defined as "1" byte. Tolerance of position determination is within $\pm$16 bytes.
- Length ; 1 byte length, indicated by bits length. Tolerance is within $\pm$1 bit.
- Gap ; 1 byte length of "00".

(7) Residual space area with no bad spot information is filled in "FF". Detecting "FFFF" of read back data may be used to recognize the end of bad spot information.

(8) Error check code in this format is CRC applied to both ID field and Data field and the CRC objective range of ID field is from FLAG to SEC. The rang of data field not cantains AM2.

CRC polynomial : $X^{16}+X^{12}+X^{5}+1$
Initial value : "00"



Each area has the following contents and number of bytes.

Area		Contents	Number of bytes 256 bytes/sector (65 sectors/track)	
GAP1		"00"	12	
SYNC		"00"	11	
ID	AM1	"19"	1	
	FLAG	"00"	1	
	CYL HL	"**"	2	
	HEAD	"**"	1	
	SEC	"**"	1	
	CRC	"****"	2	322
GAP2	ID PAD	"00"	2	
	SYNC	"00"	11	
AM2		"19"	1	
DATA			256	
CRC		"****"	2	
DATA PAD		"00"	2	
GAP3		"00"	17	
GAP4		"00"	14 Typ.	

Initialized write area (Contents of a data field are undefined.)

Write area for updating data

Note: Each content is indicated by the hexadecimal notation using bit 0 as MSB. Nominal track capacity is 20,944bytes.

Each area has the following meaning.

Area	Meaning
GAP1	Provides a time for head switching.
SYNC	Placed before an ID or data field AM. Used for synchronizing PLL in the decoder circuit.
AM1	One-byte "19" pattern to indicate the beginning of an ID field.
CYLH	ID field recognition pattern following AM1. CYLH has the following contents and also indicates high-order digit of a cylinder address.
CYLL	Indicates low-order digit of a cylinder address.
HEAD	(1) Bit 0 (MSB) indicates a sector flag. When bit 0 is set to 1, that sector is of no use. (2) Bits 5 to 7 indicate a head address.
SEC	Indicates a sector address.
CRC	CRC polynomial: $X^{16} + X^{12} + X^5 + 1$; Initial value: "00" Generation of this code ranges from FLAG to SEC
ID PAD	Additional area to correctly read and write an ID field.
AM2	"19" pattern to indicate the beginning of a data field.
DATA	User area for writing data
CRC	Bytes to check an error in the data field. This code is generated for the area not containning AM2. Polynomial and initial value are the same as for ID field.
DATA PAD	Additional area to correctly read and write a data field.
GAP3	Gap to allow spindle rotation speed fluctuations during reading/writing in a data field of each sector.
GAP4	Gap to allow displacement of a write position due to spindle speed fluctuations for a full track.

CYLH	Cylinder address
"FE"	$(0)_{10}$ - $(255)_{10}$
"FF"	$(256)_{10}$ - $(511)_{10}$
"FC"	$(512)_{10}$ - $(767)_{10}$
"FD"	$(768)_{10}$ - $(1023)_{10}$

Example of Recording Format of Defect List
(Written in 65 Sectors per Track)

Sect. Addr.	Byte Addr. in Data Field (Decimal)	Contents in Each 8 bytes (HEX) 0	1	2	3	4	5	6	7	Description
0	0 ~ 7	44 (D)	4B (K)	35 (5)	31 (1)	32 (2)	2D (-)	31 (1)	37 (7)	Model Name (DK512-17)
	8 ~ 15	30	31	30	31	30	30	31	00	Serial Number (0101001)
		← (S/N 0101001) →								
	16 ~ 23	00	00	00	00	00	00	13	00	No. of Total Defects
		← (19 Defects) →								
	24 ~ 31	00	1A	00	11	16	80	01	00	--1st Defect
		Cyl.#		HD#	Sect.#		Pos. (From Index)	Length		
	23 ~ 39	00	B6	05	00	00	FE	03	00	--2nd Defect
	40 ~ 47	01	C0	02	09	0C	78	01	00	--3rd Defect
	48 ~ 55	01	00	01	03	04	00	02	00	--4th Defect
										Cyl#(256)$_{10}$ HD#1, Sect#3, Location of (1024)$_{10}$ bytes from Index, Defect Length 2bits.
	168 ~ 175	03	02	06	1E	26	74	01	00	--Last Defect
	176 ~ 183	FF	FF	FF	FF	FF	FF	FF	FF	No more Defect
0	248 ~ 255	FF	FF	FF	FF	FF	FF	FF	FF	
1	0 ~ 7	FF	FF	FF	FF	FF	FF	FF	FF	
5	248 ~ 255	FF	FF	FF	FF	FF	FF	FF	FF	

6.5 Data Control Timing

(a) Read Initialization Time

To initiate a read operation with a new head, a 20-microsecond delay is required: 5 microseconds for head change, 15 microseconds to stabilize the read amplifier.

(b) Write-to-Read Recovery Time

The transition from inactivating WRITE GATE to activating READ GATE requires at least 20 microseconds.

(c) Read-to-Write Recovery Time

The transition from inactivating READ GATE to activating WRITE GATE requires at least 0.5 microseconds.

(d) Write Gate Off Time

The controller must send at least one byte of dummy data following a correct write data(ID or DATA CHECH BYTE) before inactivating WRITE GATE.

(e) Write Driver Turn On Time

The write driver requires 0.8 microseconds or one-byte time to become enabled. The period is provided as a write splice.

7. HANDLING AND SHIPPING

7.1 Receiving

When shipped from the factory, the DK512 is double-packed in inner and outer cartons made of strong, two-ply corrugated cardboard. The drives and their inner cartons are cushioned on all sides by approximately two and one-half inches of urethane foam. This careful packaging protects the drive against shocks and vibrations during shipping.

Keep the original cartons for shipping individual drives that are not mounted in a cabinet. For storage, seal the drive in a heavy plastic bag with a desiccant, and keep it in the inner carton.

When a drive is brought from a cold warehouse or truck into a warmer area, let it warm up slowly so that water vapor does not condense in the HDA. Open the outer carton and remove it. Leave the drive in the inner carton for the length of time shown below so it can warm up to typical room temperature (to 77°F with 50% relative humidity).

Warehouse temperature	+32°F	+14°F	-4°F
Warm-up time	6 hrs	9 hrs	11 hrs

7.2 Handling

Before removing a drive from its inner carton or from its shock-resistant mounting, prepare a cushioned area to set the drive on. Use two or three inches of urethane foam covered with cardboard, such as the top cushion of the inner carton. This is especially important if the drive will be moved around on a cart. Lift the drive by both ends, and set it gently on the cushion.

Keep each test data report with its own drive, and make sure the serial number on the report matches the nameplate on the drive. Do not separate PC boards from their drives -- the factory has installed the correct assemblies for each model.

Before testing a drive, changing any jumper plugs, or formatting, make a back-up copy of the track defect data which has been written by the factory on each surface. When the data has been backed up, the jumper plugs may be reset, as described in the Service Manual.

7.3 Shipping

Drives can be shipped in the cabinets if the drives are securely installed on their shock-absorbing mounts. If cabinets with the drives mounted will be shipped by motor freight, the cabinets should be carefully packed in cushioned packages. Drives can also be shipped separately if they are packed in their original shipping cartons.

The following procedures should be taken:

1. Clean the drive.

2. Seal the drive in a heavy plastic bag with a desiccant, otherwise water vapor might condense.

3. Double pack the drive in the original inner and outer cartons, or equivalent ones that can protect the drive from shocks of 5G or more during shipment.

4. Put a "This Side Up" mark and a "Handle with Care" indication on the outer carton surfaces.

7.4 Cautions

- Do not apply any force to the plug-in parts during packing, unpacking, or shipping.
- Take care not to vibrate or shock the drive while handling it.

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DK515 Winchester Disk Drive

Service Manual

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6. Adjustment

6.1 Adjustment of SZ931 PCB

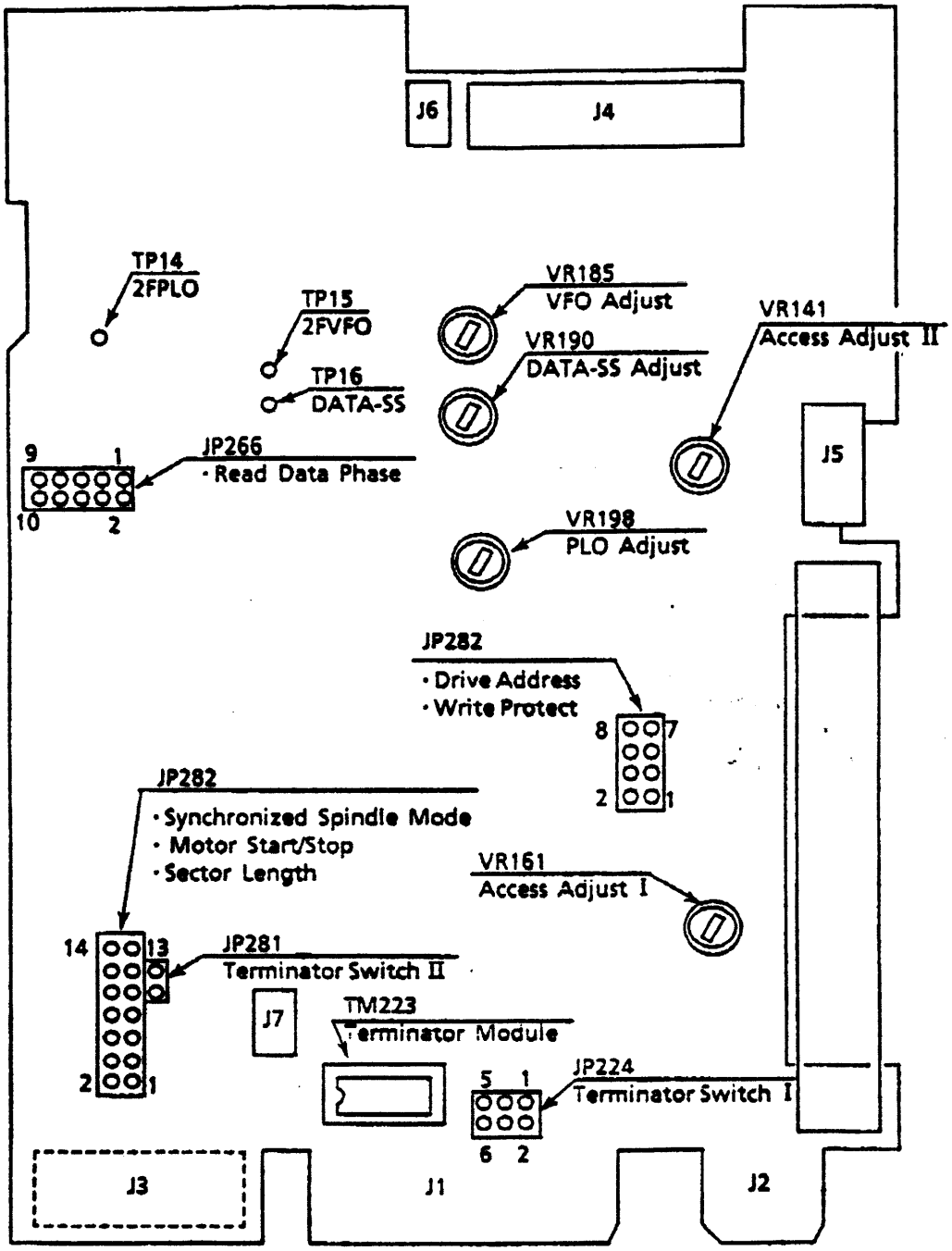


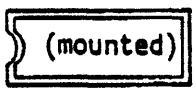
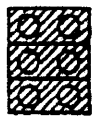
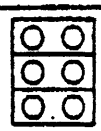
Fig. 6-1 SZ931 PCB Layout

6.1.1 Setting of Terminator Module and Terminator Switches

(1) Control Signal

Each drive in Radial connection of cable B and the last end of the drives in Daisy Chain connection of cable B should be terminated. Since a terminator module (TM223) and Terminator Switch I (JP224) are provided to all drives as shipped, remove both of them except the last drive's ones in case of Daisy Chain connection.

Table 6-1 Terminator Module and Terminator Switch I

Configuration	Terminator Module (TM223)	Terminator Switch I (JP224, pin 1-6)
• Single drive on cable B • All drive in Radial connection • The last drive in Daisy Chain		
• All drives except the last one in Daisy Chain		

* At the time of shipment, Terminator Module and Terminator Switch I are mounted on Terminator socket.

(2) Synchronized Spindle Signal

Synchronized Spindle Signal is terminated via JP281 to terminator register on the PCB. When the synchronized spindle option is used, JP281 shall be removed except the last drive's one in Daisy Chain of Synchronized Spindle Signal.

Table 6-2 Terminator Switch II

Configuration	Terminator Switch II (JP281)
The last Slave drive	
All drivs except the last Slave drive	

* A drive as shipped is mounted with Terminator Switch II

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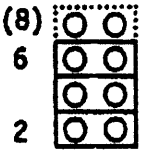
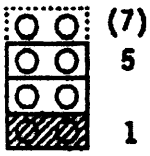
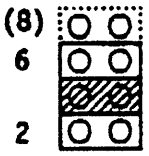
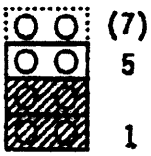
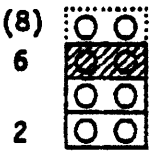
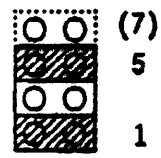
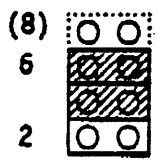
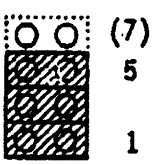
6.1.2 Setting of Jumper Switches

(1) Drive Address Jumper (JP213, Pin 1-6)

Drive address can be selected by using the jumper switch (JP213) the jumper setting and the selected Drive address is shown in table 6-3. Drive No. 0 is not used.

Table 6-3 Jumpr Setting for Drive Address

Drive No.	None	#1 *	#2	#3
JP213 (pin1-6)				

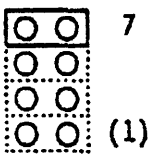
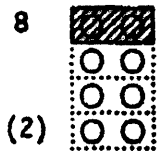
Drive No.	#4	#5	#6	#7
JP213 (pin1-6)				

* At the time of shipment, Drive #1 is selected.

(2) Write Protect Jumper (JP213, Pin 7-8)

Write operation of a drive is inhibited by setting a jumper on JP213, pin 7-8 (Write Protect mode), which condition will generate ATTENTION status upon receiving of WRITE GATE-N signal.

Table 6-4 Jumper setting for Write Protect

JP213 (pin 7-8)		
Function	Write Enable*	Write Protect

* At the time of shipment, "Write Enable" mode is selectd.

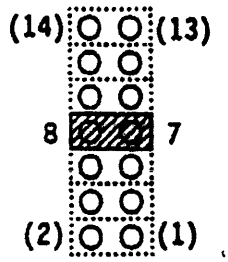
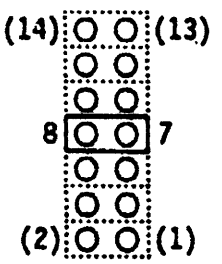
(3) Hard Sector / Soft Sector Selection Jumper

Soft Sector mode is not supported to this PCB.

(4) Motor Start/Stop Jumper (JP282, Pin 7-8)

When the "Start/Stop Spindle Motor" option, set the jumper as "Supported" before DC power on.

Table 6-5 Jumper Setting for Motor Start/Stop

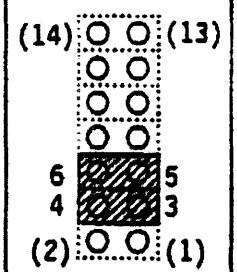
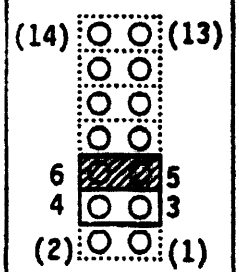
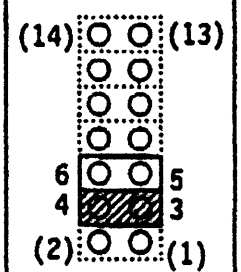
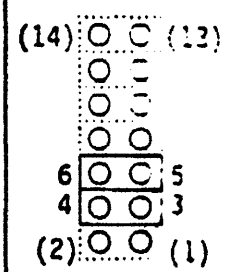
JP282 (Pin 7~8)		
Function	Not Supported *	Supported

* At the time of shipment, "Not Supported" mode is selected.

(5) Synchronized Spindle Mode Jumper (JP282, pin3-6)

Synchronized spindle mode can be selected by using the jumper switch (JP282, pin 3-6). This Jumper Setting will be aborted by the following Set Configuration command. Set the jumpers, before turn on the DC power. For the detail, refer "DK51X Winchester Disk Drive Synchronized Spindle Feature Specification ".

Table 6-6 Jumper Setting for Synchronized Spindle Mode

JP282 (Pin 3~6)				
Function	Off Line *	Slave	Master	Reserved

* At the time of shipment, "Off Line" mode is selected.

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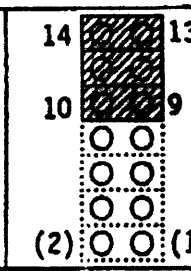
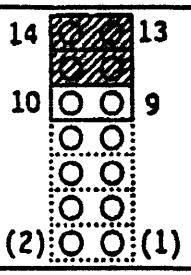
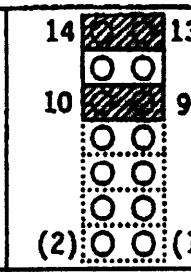
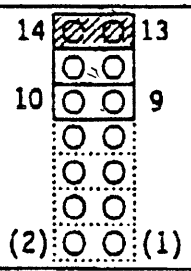
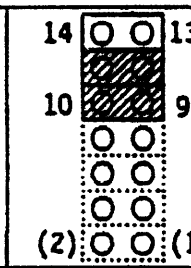
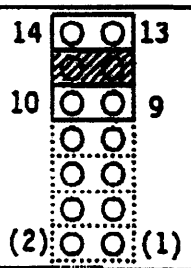
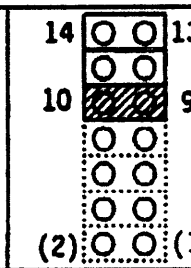
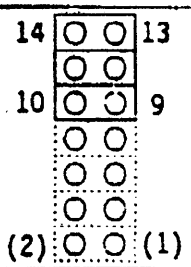
(6) Sector Length Jumper (JP282, Pin9-14)

This Jumper Setting function is effective with Hard Sector mode. This Jumper Setting will be aborted by the following "SET BYTES PER SECTOR" command. All the applicable configurations of Bytes/Sector or Sector/Track are listed in Table 6-4. Set the jumper(s) before on the DC power.

Table 6-7 Jumper Setting for Sector Length

JP282 (Pin 9-14)				
Bytes Per Sector	335	338	593	602 *
Sectors Per Track	122	121	69	68
Data Langth	256	256	512	512

JP282 (Pin 9-14)				
Bytes Per Sector	Adjust Mode	1107	Not Used	
Sectors Per		37		
Data Langth		1024		

* At the time of shipment, 122 sectors per track is selected.
* Refer to Section 6.1.3 (5) as for Adjust Mode.

Eprom 14C-9255T-C

6.1.3 Adjust of Variable

(1) PLO Frequency Adjusting

This variable resistor shall be re-adjusted for setting the frequency of the servo
synchronous clock after altering PLO circuit.

Sequence

a) Connect J3 connector and turn on the DC Power-supply on the condition that J5 connector is disconnected.

b) Adjust the frequency of 2F PLO-P signal (observed at TP14) to 41.5 ± 0.4MHz by using VR198.

Table 6-8 Adjustmentt of PLO Frequency

Instrument	Location
Test Pin	TP14
Variable Resistor	VR198

c) Turn off the Power and install the PCB as it was before.
As for the installation, refer to section 5.4 (1)

d) Turn on the Power again and confirm that it can be read normally by using the system program or a tester.

(Note) When adjusting the Variable Resistor, use the adjustable screw driver (-: minus type) and turn it carefully.

(2) VFO Frequency Adjusting

This variable resistor shall be re-adjusted for setting the frequency of the read signal synchronous clock after altering VFO circuit.

Sequence

a) Turn on the DC power-supply on the condition that J1 and J2 cable are disconnected.

b) Adjust the frequency of 2F VFO-P signal (observed at TP15) to 39.3 ± 0.4MHz by using VR185.

Table 6-9 Adjustment of VFO Frequency

Instrument	Location
Test Pin	TP15
Variable Resistor	VR185

c) Turn off the Power and install J1 and J2 cable as it was before.

d) Turn on the Power again and confirm that it can be read normally by using the system program or a tester.

(Note) When adjusting the Variable Resister, use the adjustable screw driver (-: minus type) and turn it carefully.

(3) DATA-SS Pulse Width Adjusting

This variable resistor shall be re-adjusted for gaining a enough VFO capture range after altering Data SS circuit.

Sequence

a) Access the data writtn track on condition that DK515 is interface with the host system or a tester.

b) Adjust the pulse width of DATA-SS-N signal (observed at TP16) to 17.5 ± 1ns by using VR190.

Table 6-9 Adjustment of DATA-SS Pulse Width

Instrument	Location
Test Pin	TP16
Variable Resistor	VR190

c) Turn on the Power and confirm that it can be read normally by using the system program or a tester.

(Note) When adjusting the Variable Resistor, use the adjustable screw driver (-: minus type) and turn it carefully.

(4) Read Data Phase Adjusting

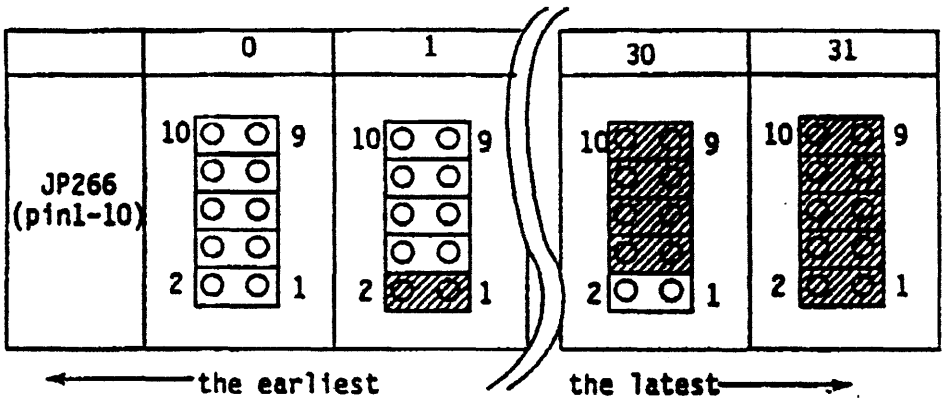
This Jumper switch shall be re-adjusted after altering READ DATA circuit or the combination of PCB and HDA.

Sequence

a) Interface with the host system or a tester, and read the randam data in an inner cylinder continuously.

b) Adjust with the jumper switch (JP266) and find out the read boundary (the earliest and the latest) with no read error.

Table 6-11 Adjustment of Read Data Phase



c) Set JP266 to the average value of the earlist and the latest.

d) Turn on the Power again confirm that it can be read normally by using the system program or a tester.

(Remarks) To confirm without retry for the read error.

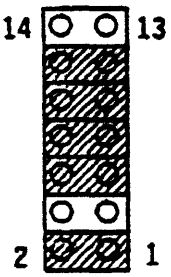
(5) Access Adjusting (VR161, VR141)

This variable resistor shall be re-adjusted with an exerciser program in DK515 after altering the combination of PCB and HDA.

Sequence

a) Set the jumper switch (JP282) on the PCB shown as Table 6-12, and turn on the DC Power Supply. Adjust the DC Power Voltage to 12V ± 1% and 5V ± 1% at the DC Power Supply Connector. The irregular DC Power Voltage may cause an irregular adjustment.

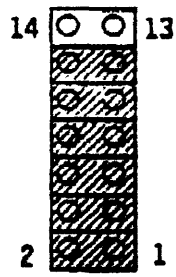
Table 6-12 Access adjust-I

JP282 (pin1-14)	
Variable Resistor	VR161

b) The DK515 will go to the Access Adjust-I with indication that the LED on the front panel is flushing, within 30sec after the DC Power turns on. In the state, adjust VR161 by turning carefully right or left to the adjusted state with indication that the LED is "ON". The closer the adjusting of VR161 is, the shorter the interval of the LED flushing.

c) After the completion of Access Adjust-I, set the jumper (JP282) on the PCB shown as Table 6-13.

Table 6-13 Access Adjust-II

JP282 (pin1-14)	
Variable Resister	VR141

d) DK515 will go to the Access Adjust-II with indication that LED on the front panel is flushing. In the state adjust VR141 by turning carefully right or left to the adjusted state with indication that the LED is "ON". The closer the adjusting of VR141 is, the shorter the interval of the LED flushing.

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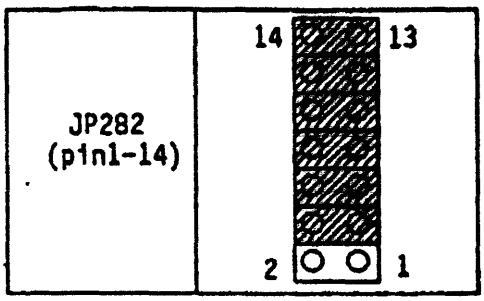
e) After the completion of Access Adjust-II, set the jumper (JP282) on the PCB shown as Table 6-14.

Table Completion of Access Adjust



f) Confirm the Ready condition within 10 seconds after the setting as above.

g) After the confirmation of correct adjustment, re-configurate JP282 as it was, and turn off and on the DC power so as to inifialze the drive.