HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

APPLICATION NOTE HM004

STATIC MEMORY SYSTEMS UTILIZING THE HM-6100

INTRODUCTION

In the design of a microprocessor based memory system, the designer must direct considerable attention to a minimum package count. Minimum system package count results in minimum system cost. Care should be taken, however, by the designer when evaluating various microprocessors, to select a device which will function with standard memory components. Many microprocessors require dedicated memory components to achieve minimum system package count, and since these special memory components may not be multiple sourced, the dedicated system cannot benefit from the high volume production associated with standard components.

In designing the HM-6100 CMOS microprocessor, considerable care was taken to minimize the number of external packages required thereby reducing the overall cost and complexity of many system configurations. All the control signals to interface directly with standard memory components, input-output devices, a switch register and a control panel, without the need for any external gating, are provided.

This note describes four memory systems utilizing the HM-6100.

- Low Power 256 x 12 CMOS RAM, 2K x 12 Bipolar PROM System
- 1K x 12 Static NMOS RAM System
- 256 x 12 CMOS RAM, 1K x 12 CMOS ROM System
- 4K x 12 Nonvolatile CMOS RAM System

Since the 4K x 12 Nonvolatile CMOS RAM System is a part of the 6900 Prototyping System, which includes, additionally, a CPUTTY Interface Board and a Control Panel Board, special attention is given to it.

HM-6100 MEMORY SYSTEM INTERFACE SIGNALS

Prior to discussing the memory systems described herein, a brief review of the HM-6100 signals used to interface with the memory components is in order.

DX (0-11) — Memory/Peripheral device address, data-in and data-out are time multiplexed on the DataX (DX) lines.

LXMAR (H) — When a valid address is present on the DX lines, the Load External Address Register (LXMAR) is pulsed high. LXMAR, the clock input to a register, is used to externally latch the address information. If the memory device has internal address latches, as is the case with Harris CMOS RAMs and 4K dynamic NMOS RAMs, LXMAR serves as an address strobe.

MEMSEL (L) — The HM-6100 activates the Memory Select (MEMSEL) line to "low" enabling memory devices to perform read and write operations.

XTC — XTC distinguishes the read portion of the CPU cycle from that of the write. XTC is high for read's and low for write's. MEMSEL serves as the standard Chip Select (CS) signal and XTC as the Read (H)/Write (L) ($\overline{R/W}$ or $\overline{WE}$) control for memory devices.

XTA (H) and XTB (H) — The external timing signals XTA and XTB specify the flow of information on the DX lines. XTA is valid for data-in transfers

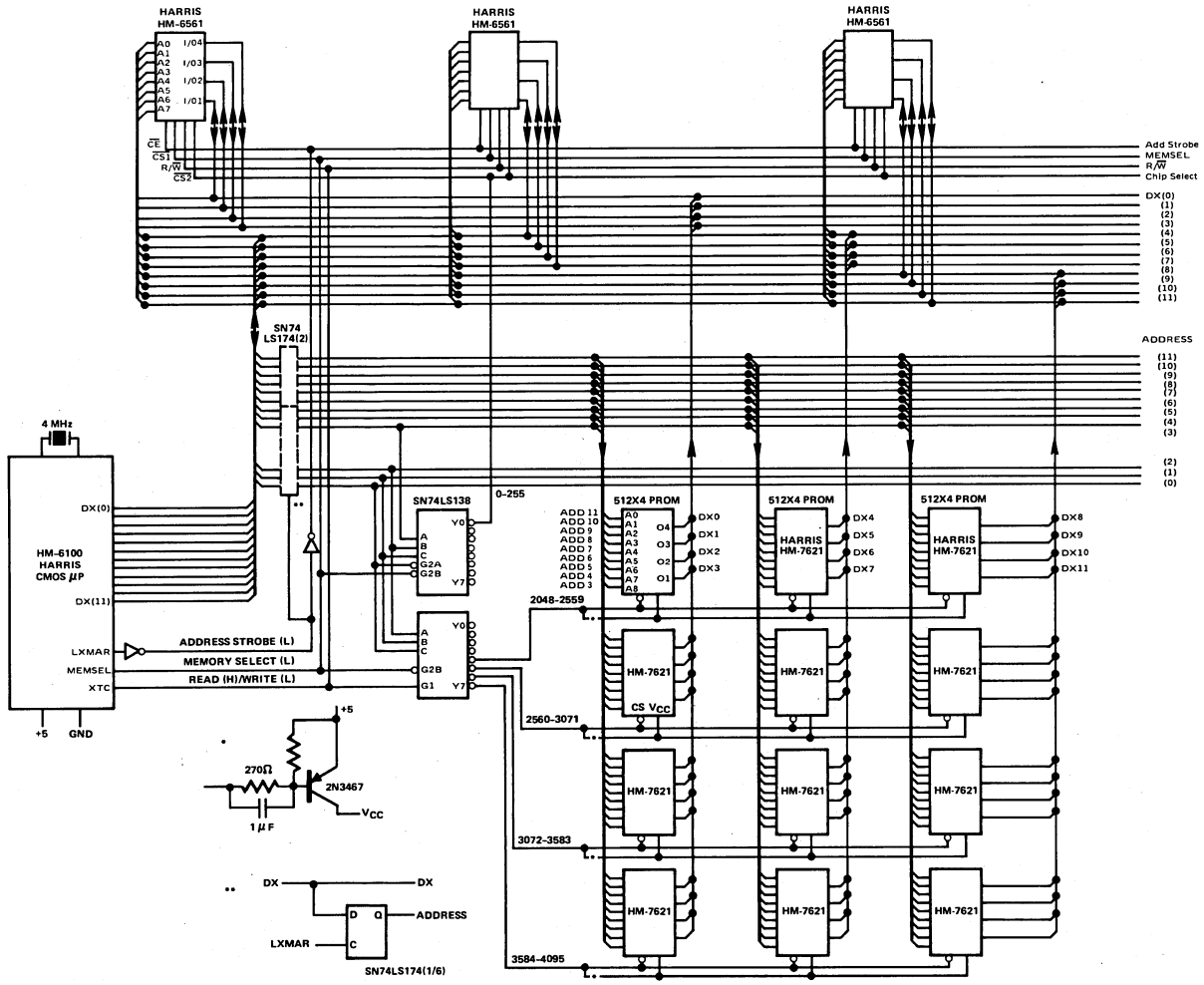

Figure 1

Table 1
POWER DISSIPATION CALCULATION

TYPE	QTY	EXPLANATION	SYSTEM P_D(AV)(mW)
HM-6561	3	Each device dissipates 15mW at 1MHz. The minimum cycle time of the HM-6100 is 2.5μs. Therefore, the RAMs are accessed, best case, every 2.5μs or 400kHz. Each RAM will effectively dissipate 6.0mW.	18
HM-7621	12	Each device dissipates 500mW. Due to power strobing only three devices are on at any time. Devices are operating at a 20% duty cycle.	300
MEMORY SYSTEM DISSIPATION			318

to the HM-6100; XTB is valid for data-out transfers from the CPU. All HM-6100 signals are TTL compatible at 5 volts. Each output can sink 2mA at 0.4 volts. This provides for one standard TTL device or 10 low Power Schottky devices. If the drive capacity on the DX lines is exceeded in a system, the DX lines must be buffered by tristate driver/receiver (transceiver) pairs. XTA and XTB provide the steering control for the transceivers.

WAIT (L) The HM-6100 expects a memory system access time of 600 ns for full speed operation at 5 volts with a 4 MHz crystal. However, the CPU can pause for an external data transfer in steps of 250 ns to interface with slow memory or peripheral devices. The WAIT signal is sampled at T2C and T6C of the cycles that involve data transfers. The microprocessor resumes operation when the WAIT signal returns to high. The HM-6100 is in the lowest power state when it is paused since only the internal oscillator circuit consumes power in the wait state and the rest of the circuits require only p-n leakage current to maintain microprocessor state information indefinitely.

Most of the currently available microprocessors require 400-500 ns memory system access for full speed operation, and the CPU can wait only in 500 ns steps. Since the memory system accounts for a significant portion of the system cost, the requirements for a faster and, hence, more expensive memory increases the cost of the system.

LOW POWER 256 x 12 CMOS RAM, 2K x 12 PROM SYSTEM (FIGURE 1)

Power supplies and cooling requirements add considerably to the cost and reliability of microprocessor systems. The power dissipation of ROMs and PROMs can be substantially reduced by "power strobing." That is, read only memory devices are powered up only when they are selected for reading. Extremely low standby power dissipation makes CMOS RAMs particularly suitable for low power applications. Harris CMOS RAMs consume power only when addresses change and their quiescent power dissipation is in the microwatt range.

The following is a detailed description of a low power memory system ideally suited for microprocessor system prototyping. The memory system uses a single power supply of +5V. A 2K x 12 PROM, 256 x 12 RAM organization is chosen for the illustration since it seems to be adequate for most microprocessor based applications. However, provisions are made in the system to expand the RAM/PROM capacity to 4K words. The memory system is organized such that Pages 00_8-01_8 (locations 0000-0377_8/0000-0255_{10}) have RAM and Pages 20_8-37_8 (locations 4000-7777_8/2048-4095_{10}) have PROM.

The addresses are latched in two hex DFF's (SN 74LS174). The control signals are buffered with hex buffers. Octal decoders (SN74LS138) are used to decode RAM packages in 256 word "pages" and PROMs in 512 "pages". The address inputs for the RAMs are not latches since the CMOS RAMs provide for internal latches. LXMAR strobes the addresses into the CMOS devices.

The PROMs (HM-7621) are power switched using PNP transistor. In the organization shown, only three PROMs, in the selected row, will consume power. MEMSEL is used to turn the entire PROM memory on and off. The series transistor switch adds about 30 ns to the PROM access time. Since the PROMs have a typical access time of 50 ns, the added delay of 30 ns will not affect the system operation. The V_{CE} drop across the transistor reduces the power supply margin of the PROMs. With properly selected parameters for the switch and the power supply, the PROMs will operate reliably with the PNP power switch.

In microprocessor systems, main memory utilization is only 20 to 30%. That is, on the average, the memory is accessed 20 to 30% of the CPU active time. There are technological reasons for this sparse memory reference pattern. The microprogrammed control structure of microprocessors implies that the CPUs execute 2-4 nonmemory cycles for every memory cycle. Since the microprocessors and memory devices are implemented with the same technology, any improvements in the technology that would reduce the CPU cycle time, should also reduce the memory access/cycle time. The memory read duty cycle of the HM-6100 for a typical program is approximately 20% and about 50% of the CPU cycles involve memory references. Using these two factors, the average power dissipation of the memory system can be calculated as shown in Table 1.

1K x 12 STATIC NMOS SYSTEM (Figure 2)

If low power dissipation and nonvolitility are not important, the 1K x 1 NMOS Static RAM is a cost effective memory device for microporcessor applications. The HM-6100 microprocessor interfaces directly with these standard RAMs. The memory address information must be stored externally. Since the 1K x 1 NMOS RAMs do not tristate the outputs during Write's, the RAMs require tristate output buffers, even if one does not require the additional drive capability, in systems with common data inputs and outputs.

CMOS 256 x 12 RAM–1K x 12 ROM SYSTEM (Figure 3)

Since the standard CMOS RAMs and ROMs manufactured by Harris have tristate outputs and internal edge triggered address latches, address, data-in and data-out can be time multiplexed on the same lines. Considerable reduction in the total number of lines to be bussed without any degradation in performance, or without adding any additional devices for buffering and latching, will be realized.

The HM-6561 is a standard 256 x 4 CMOS RAM with multiplexed data-in and data-out. The HM-6312 is a 1K x 12 CMOS ROM for microprocessor applications with address and data-out multiplexed on the same pins. In the HM-6312, address is loaded into the on-chip register at the falling edge of LXMAR. DX (0) and DX (2) are latched chip enables during the address strobe time. They are programmed internally so that up to 4 ROM packages can be in the system without any external decoding. RSEL output defines an area in the 4096 word addressing space dedicated to RAM. It can be programmed to any latched logical NAND function of the variable DX(0), DX(1), DX(2) and DX(3) during the address strobe time. This output eliminates a four bit register and decoder for the high order address bits to select RAM in RAM-ROM systems. When RSEL is active in a ROM package, its outputs are tristated.

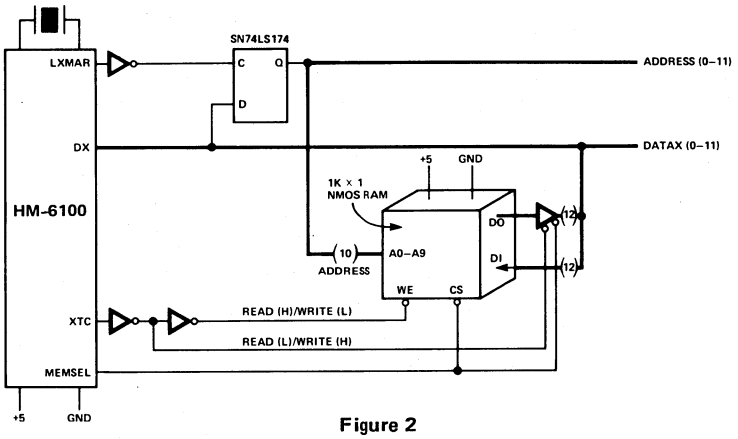

Figure 2

HM-6100 – STATIC NMOS RAM INTERFACE

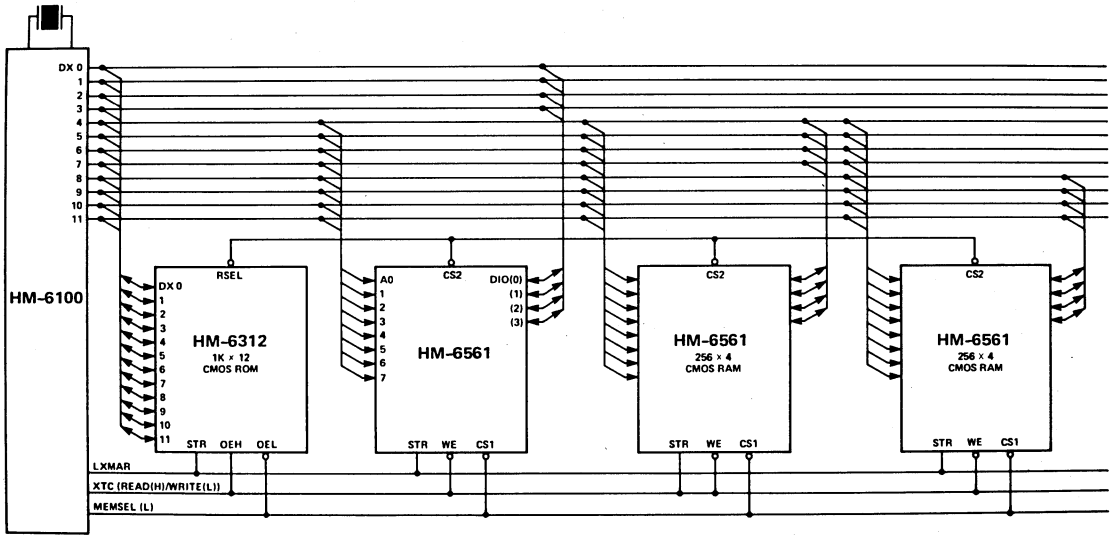

Figure 3

CMOS 256 x 12 RAM – 1K x 12 ROM SYSTEM

4K x 12 NONVOLATILE CMOS RAM SYSTEM

A portable nonvolatile CMOS memory system has distinct performance, functional and cost advantages over Bipolar Programmable ROMs (PROMs) and MOS Erasable ROMs (EROMs) as a microprocessor system development tool. Currently available CMOS RAMs have access times of < 100 ns at 10 volts. CMOS RAMs provide performance similar to bipolar PROMs in addition to being reprogrammable. MOS EROMs may be erased and reprogrammed. However, erasure is nonselective, that is, all locations are erased at the same time. Locations in CMOS RAMs can be selectively modified with the conventional WRITE operation while EROMs require special equipments for programming and erasing. Since CMOS RAMs are considerably faster than EROMs (100 ns vs. 500 ns), the system performance need not be degraded in the prototype stage when CMOS RAMs are used. The following sections describe the specific implementation of a TTL compatible 4K x 12 portable nonvolatile memory plane, utilizing Harris' 1K x 1 CMOS RAMs (HM-6508), Figure 4.

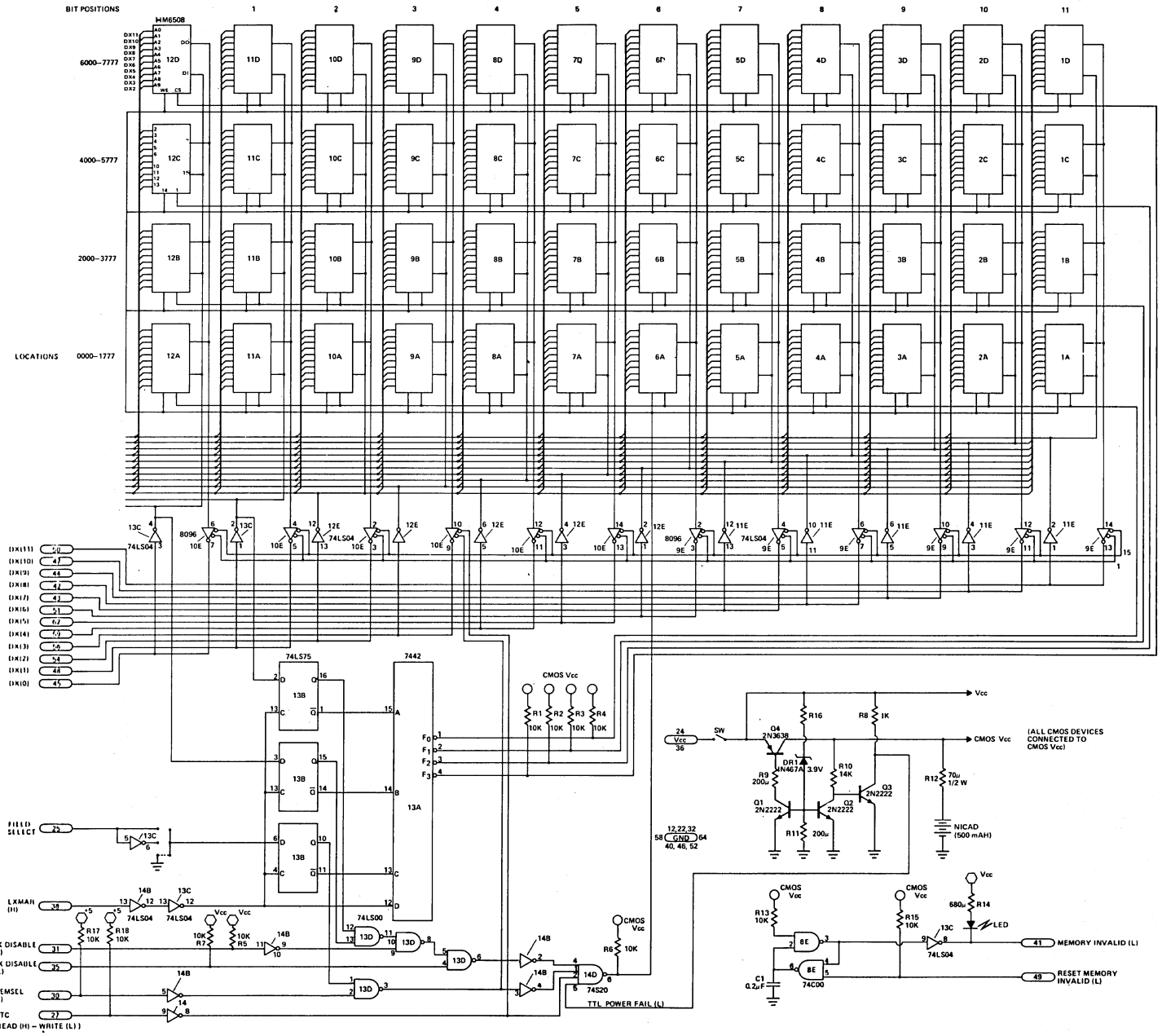

Figure 4

AUTOMATIC BATTERY BACKUP

Memory systems require peripheral circuits for buffering and decoding. If 54/74C or 4000 series CMOS devices are used for the peripheral logic in a CMOS memory system, the system performance is significantly degraded. A more efficient approach would be to use bipolar devices for buffering, decoding and to provide battery backup to the CMOS devices as shown in Figure 5. When the power supply is interrupted, only the CMOS RAMs will draw power from the battery and, hence, the standby characteristics of the system is not affected by using bipolar peripheral circuits.

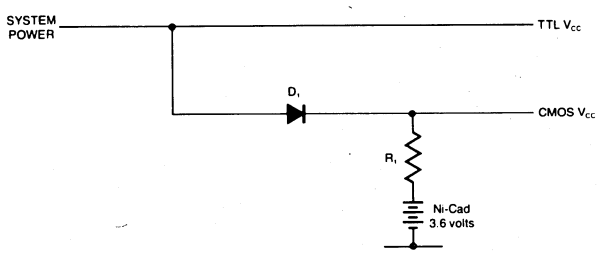

Figure 5

When the system is supplying power, the diode D_1 will be forward biased, and the CMOS V_{CC} will be one diode drop, 0.6 volts, below the TTL V_{CC}. If the power supply fails, the battery will supply power to the CMOS devices, and the diode D_1 will isolate the TTL devices. Note also, that when the system power is on, the battery is constantly being charged through the resistor R_1.

This arrangement, though extremely simple, has certain drawbacks due to special characteristics of CMOS devices. Since TTL V_{CC} is more positive than CMOS V_{CC}, there is the possibility of a TTL totem-pole output to a CMOS device becoming more positive than the CMOS V_{CC}. There are 4 layer (P-N-P-N) parasitic devices associated with CMOS device structures. These parasitic devices can latchup due to SCRing if any input to the device is more positive than V_{CC}. If, open collector bipolar devices are used for interfacing with the pullup resistors going to the CMOS V_{CC}, CMOS devices can be protected against positive spikes as shown in Figure 6. This approach

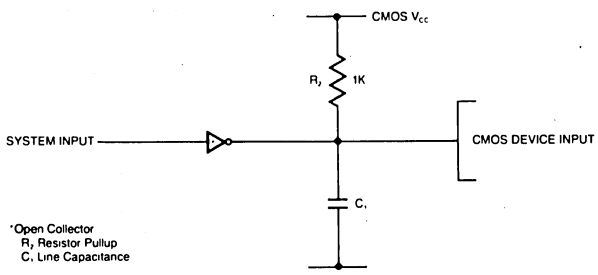

Figure 6

adds an RC time constant to the delay of the gates. In a 4K x 12 memory system, the total capacitive loading on an address line can be approximately 200 pF.

If the pullup resistors is 1K ohms, the time constant will be 200 ns. There is also DC power dissipation when the gate outputs go to logic ZERO. However, the pullup resistors guarantee against the inputs to the CMOS devices being floated when the system power is off. If inputs to CMOS devices are allowed to float, the inputs could be at marginal logic levels, causing both the P and N channel transistors of input inverters to be active simultaneously. The worst case power dissipation, due to marginal input levels, can easily increase standby power dissipation of CMOS devices by a factor of 10.

POWER FAIL INDICATOR

The Diode D_1 in Figure 5 can be replaced by a PNP transistor, T_1 as in Figure 7 which is on when the system is supplying power and off when memory is on battery backup. The POWER FAIL (L) signal is used to turn off the PNP transistor. This signal also provides a logic flag to the system when the memory devices are on battery backup. Read/Write functions to the memory are disabled when the system is on battery backup.

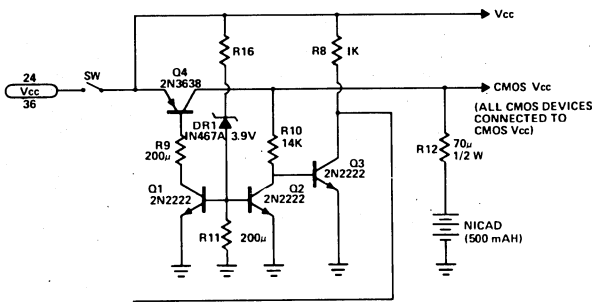

Figure 7

Since the V_{CE} drop of a PNP transistor being approximately 0.2 volts less than that of a diode, there is more margin against SCR actions being triggered by positive spikes at the inputs. The open collector TTL devices can now be replaced by TTL devices with active pullups thereby improving system performance due to reduced RC time constants on input lines. With conventional bipolar devices, resistor pullups to CMOS V_{CC} are still required to ensure against CMOS inputs floating when power supply to bipolar devices are interrupted. Low power Schottky devices (54/74 LS) have the interesting property that when their V_{CC} is at GND, the outputs will be at GND also. Thus, resistor pullups can be avoided if 54/74 LS devices are used for line buffering. Certain control lines to the CMOS devices, Chip Selects and Write Enable, must be held high so that the devices are not

accidentally written in when the memory devices are on battery backup. 54/74 LS devices should not be used to buffer these control lines.

DATA INVALID INDICATOR

A nonvolatile memory system must provide a DATA INVALID flag as shown in Figure 8 to inform the system if the power to the memory devices has gone below, even momentarily, the level required to guarantee data retention in CMOS devices (typically 3 volts). The flag once set, must be reset only by a positive action from the system or the user. The capacitance loading in the output of the CMOS gates that make up the latch guarantee that the CMOS latch circuit will come up with a DATA INVALID flag if the CMOS latch is disrupted even momentarily or if the CMOS V_{CC} has dropped below the voltage to maintain the state of the CMOS latch. If the data is invalid, the LED indicator illuminates as the system power comes back up.

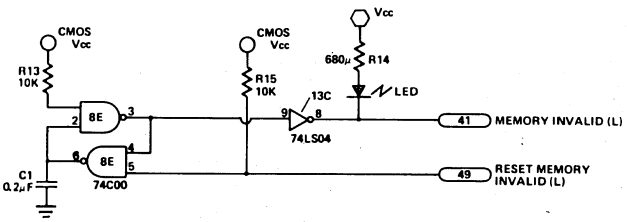

Figure 8

PROTECTION AGAINST STRAY CONTACT SIGNALS

A switch in series with the power supply is used to protect the memory against stray contact signals when plugging or unplugging the module from a "live" system.

WRITE PROTECT CONTROLS

The entire 4K memory can be write protected with the Write Protect 4K signal. There is also an option of write protecting only the upper 3K of memory with the Write Protect 3K signal. The user can simulate 4K RAM, 4K ROM, or 1K RAM-3K ROM combinations with these two signals.

STANDBY DATA RETENTION

The maximum standby current drain of the 4K x 12 memory plane at 25°C is 500 μA. The data retention is time dependent on the battery rating and the storage temperature. For example, if 500 mAH rechargeable Nickel-Cadium cells are used, the standby data retention at 25°C will be 1000 hours (40 days).

FUNCTIONAL DESCRIPTION

The detailed circuit diagram of the 4K x 12 nonvolatile CMOS memory system is shown in Figure 4. The system makes provision for expansion with FIELD SELECT input. The addresses (A_0 - A_{14}) need be valid only for a short duration when the LXMAR pulse makes a negative transition. The HM-6508 latches the addresses internally. Since the HM-6508 address strobe and chip select functions are provided on a single pin ($\overline{CE}$) , the address strobes are sent to devices through a decimal decoder (7442). All chip selects are high when the LXMAR goes high. If the memory board is selected, then the chip select to a specific row of HM-6508's will be enabled low when LXMAR goes low. The timing requirements are such that the Address, Data-In and Data-Out can be time-shared on the same lines without any degradation in the memory system performance.

DC Characteristics

I_{CC} at 3.6V, 25°C	**500 μA (max)**
Standby data retention at 25°C	**40 days**

AC Characteristics

The memory system timing specification follows closely that of the **HM-6508/18**

AC characteristics V_{CC} = 5.0V T_A = 25°C

	MIN (ns)	MAX (ns)
Access time from Address Strobe (T_{AL})		390
Address set-up time (T_{AS})	50	
Address hold time (T_{AH})	115	
Address strobe pulse width positive (T_L)	235	
Address strobe pulse width negative ($T_{\overline{L}}$)	390	
Write pulse width (T_{WP})	235	
Input data set-up time (T_{DS})	235	
Input data hold time (T_{DH})	0	
Output disable time (T_{DIS})	10	50
Output enable time (T_{EN})	10	50
I_{CC} 250 KHz (4 MHz for CPU)	400 mA (max)	

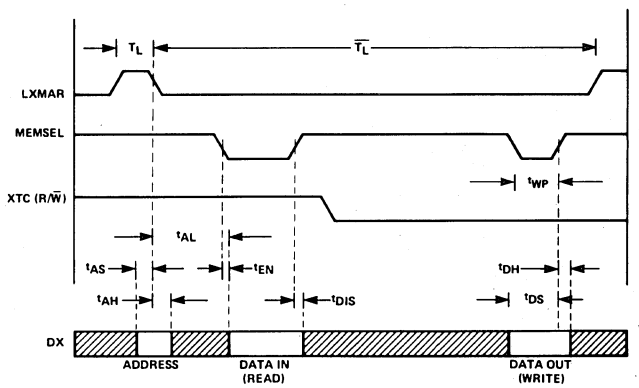

Figure 9

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