HARRIS CORPORATION
COMPUTER SYSTEMS DIVISION

High Performance Super-Minicomputers

CPUs

Harris CPUs: The Key to Performance

The Computer Systems Division of Harris Corporation produces the finest high performance super-minicomputers available today. These machines are used in industry, government and universities, with special prominence in engineering and scientific applications.

Harris computers have been distinguished for their technical superiority since the founding of the Computer Systems Division more than 10 years ago. This superiority continues today, maintained by research and development spending well above the average for the electronics industry.

Outstanding Performance

Harris machines typically offer outstanding price/performance. The HARRIS 800 is the most powerful virtual memory super-minicomputer available today, as measured by the Whetstone benchmark. This benchmark is the industry standard for evaluating processor power in scientific and engineering environments.

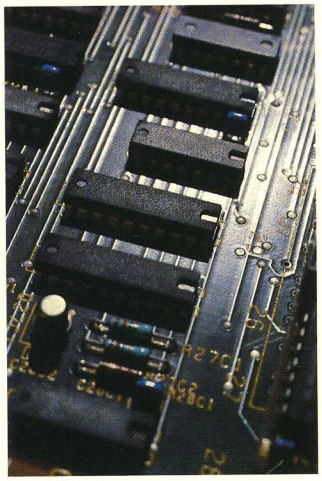
Another performance factor is seen in an exceptionally high I/O throughput rate. This is common to all Harris computers from the HARRIS 80 to the HARRIS 800. For example, the HARRIS 800 combines this high I/O rate with the raw processing power of pipeline architecture and with large virtual and physical memory capabilities. This combination makes the HARRIS 800 the most powerful computer in the Harris line.

Benchmarks have proven conclusively that Harris computers outperform other machines in their price range, especially in FORTRAN processing. Harris computers are also efficient in other high-level languages used in the educational and scientific world, such as Pascal and APL.

Unsurpassed Compatibility

Compatibility, from system to system, is characteristic of all Harris computers manufactured since the inception of the company. Today's HARRIS 800 will run the same software that is used on Harris computers manufactured nearly ten years ago. All system and application software remains fully compatible, from the smallest to the largest system.

Most of the I/O channels, peripheral controllers and peripherals themselves are likewise compatible over a wide range of Harris computers, thus guaranteeing the security and long-term growth path for Harris users.



Unlimited Flexibility

In addition to the benefits of compatibility, Harris offers its users the ability to perform concurrently in all three major processing modes:

- Interactive
- Batch
- Real-time

Each of these modes is available separately from any terminal and simultaneously throughout the system. A distinctive Harris characteristic is that the entire line performs equally well in any of these environments. Either directly connected or via communication lines, Harris remote users have access to all three forms of processing and can select the exact processing mode through any terminal.

Harris Systems' Architecture: A Proven Foundation

Resource sharing, an important user benefit, is only part of the Harris story. Field-proven and fully-tested hardware, plus multiple, unique hardware features, are additional characteristics which make Harris super-minis outstanding systems.

Fast and Efficient Bus Structures

All Harris computers have a separate 48-bit data bus, plus an additional address bus, both of which serve to increase system throughput. The data bus asynchronously connects major system elements, including the CPU, input/output channels, data communications processor and main memory.

The 19 megabytes-per-second system data bus bandwidth handles the most demanding applications. Large amounts of input/output data can be simultaneously transferred along with program instructions to the central processing unit.

System efficiency and performance are greatly increased through the parallel transmission of the address and data paths over separate busses.

Pipeline Processing

Pipeline processing provides extremely fast program execution by beginning the decoding of an instruction before the decoding of the previous instruction is completed. This is one of the ways in which the HARRIS 800 achieves its high performance.

The Harris pipeline can simultaneously hold seven instructions at various stages of execution, completing an instruction at the exceptionally high rate of 180 nanoseconds. Floating point numbers in the pipeline have 39-bit signed mantissas and 8-bit signed exponents, accuracy equivalent to eleven decimal digits. This is sufficient to define a point on the circumference of the earth to within one millimeter and enough precision to meet demanding user requirements.

The HARRIS 800 includes three concurrent processes:

- Instruction prefetch
- Instruction decode
- Instruction execution

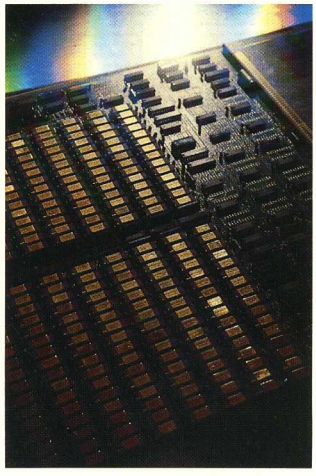
In addition, this system provides a prefetch feature unique among minicomputers: the prefetch unit will fetch both branches of a conditional branch and build a queue for instructions from both branches. Then when the instruction is executed and the branch selected, the queue required is already prefetched and available so that no time is lost in flushing and reloading the queue, as would occur with other super-minicomputers.

Floating Point Processor

The Harris scientific arithmetic unit (SAU), a high-speed floating point processor, is available on non-pipeline Harris computers. The SAU processes floating point numbers with 39-bit signed mantissas and 8-bit signed exponents.

Because arithmetic operations for such large numbers are iterative and time consuming, sophisticated algorithms are implemented in the SAU to perform these operations quickly.

To further increase system performance, the SAU operates asynchronously with the CPU, allowing the units to work in parallel.



Harris Memory: Extremely Flexible

The Harris memory implementation is the key to much of the performance of Harris machines. With state-of-the-art high density memory and hardware-implemented virtual memory, Harris computers again outstep other machines.

Harris offers memory in two versions: standard and high density. Standard memory, with 192 kilobytes of memory per board, is constructed with a timing and control circuit on each board. This construction technique provides a high degree of redundancy and reliability.

Not only is standard memory reliable, but it is also very fast, even without the use of cache memory. With a read access time of 290 nanoseconds and a cycle time of 400 nanoseconds, the Harris memory implementation is the fastest available on any superminicomputer.

Harris high density memory is offered in the largest configuration available in the minicomputer industry today — with 1.5 megabytes per board. This memory uses a single timing and control circuit with one or more memory boards. These boards utilize the 64K-bit RAM chip; Harris was one of the first vendors to utilize this high density device.

Lower cost, increased flexibility, space economy and lower power consumption are major benefits of high density memory.

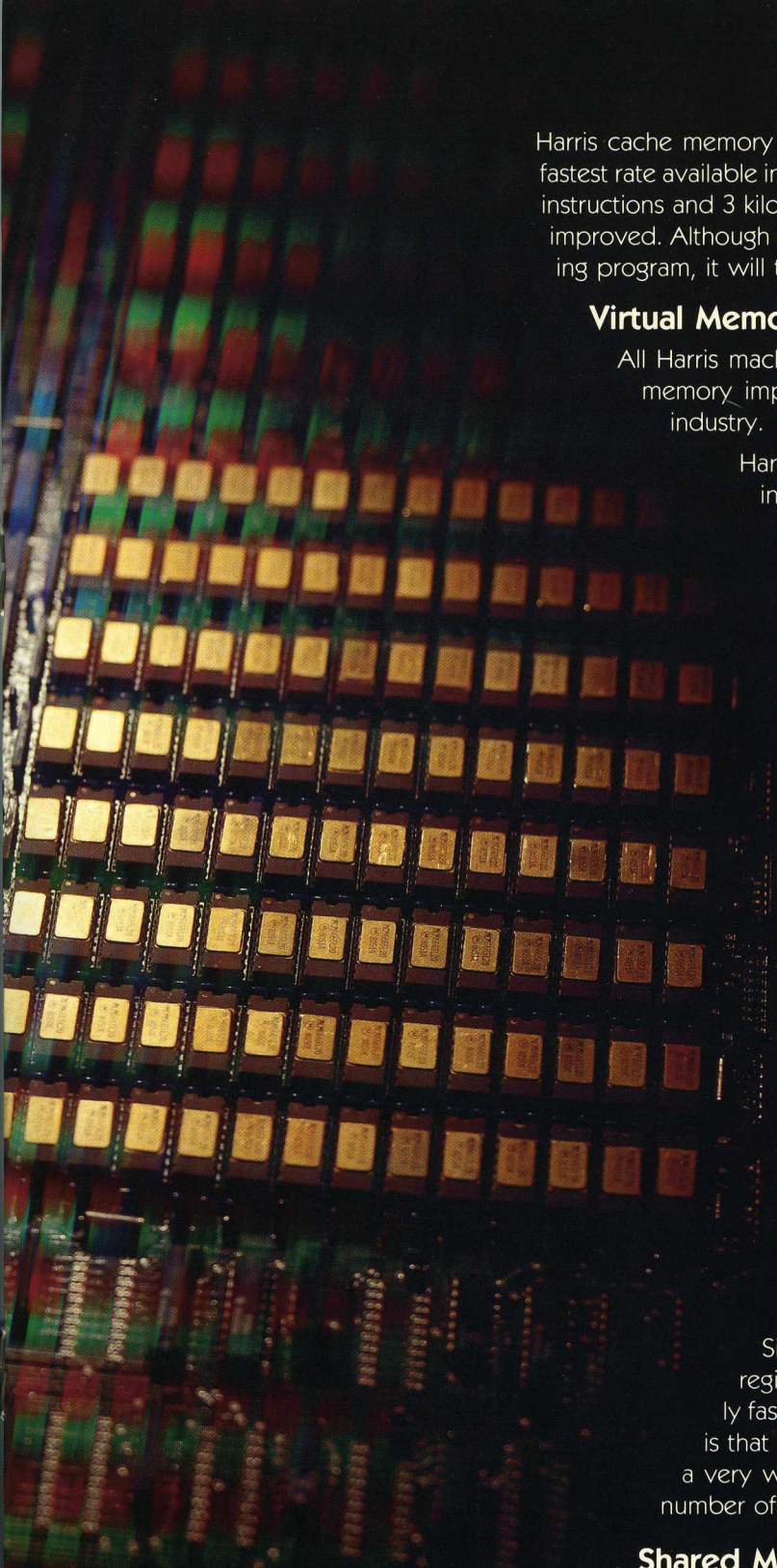
Harris memories can also be interleaved in various ways, providing total throughput of up to 19 megabytes per second. This is the highest total throughput generally available in the industry today.

Cache Memory

In addition to main memory, the HARRIS 500 and 800 each include 6 kilobytes of high-speed cache memory. Cache memory enhances the apparent speed of main memory, effectively creating an extremely high-speed memory without the cost of actually doing so.

Harris cache memory includes several unique features, including write through to main memory and automatic purge of "stale" information. This space management assures that high priority tasks remain in cache memory.

Speed is the primary benefit of cache. Recently fetched instructions and data are kept in the cache memory, which has a much shorter access time than main memory. Each time the contents requested from a memory location are obtained from cache memory (rather than main memory), a cache "hit" occurs and significant access time is saved.



Harris cache memory has an access time of only 70 nanoseconds. . . the fastest rate available in the industry. Uniquely segmented into 3 kilobytes of instructions and 3 kilobytes of operands, the cache hit rate is dramatically improved. Although the hit rate is dependent on the nature of the executing program, it will typically be 90 percent or better.

Virtual Memory

All Harris machines are virtual memory systems. The Harris virtual memory implementation is totally unique in the minicomputer industry.

Harris built the first virtual memory super-minicomputer in the early 70s and has continued to develop and refine the concept since that time. One of the especially efficient features of the Harris virtual memory system is its hardware and software implementation. This unique feature greatly minimizes demands on the operating system.

Harris virtual memory is addressed through a series of hardware registers known as "virtual address registers." These addressing units operate at register speed to provide extremely high-speed access.

The HARRIS 80 and 100 both have over 2000 virtual address registers, while the other machines have over 4000 virtual address registers. Because of the high speed and extremely large number of virtual address registers, memory can be utilized both extensively and efficiently.

Each unit of memory can be addressed in very small increments by a virtual address register. The pages of an individual program can be scattered throughout real memory and still addressed at register speeds. This prevents memory fragmentation and is a very effective use of memory, especially in heavy program loading situations.

Since an individual memory page can be addressed at register speed, the virtual memory translation is extremely fast. The benefit of this implementation to the customer is that Harris systems maintain their high performance over a very wide range of loads and can support a much larger number of terminals than competitive machines.

Shared Memory

In addition, a shared memory system is available on the HARRIS 300, 500 and 800 computers for multiple processor configurations requiring rapid access to common data. The shared memory system supports six ports, permitting as many as six processors to be linked through shared memory. This technique is especially useful in real-time or simulation applications, where multi-processor configurations are often encountered.

Harris I/O: Complete Versatility

The speed and versatility of the Harris I/O structure offer important user benefits. These features, incorporated into the design of all Harris computers, permit different types of I/O channels to be mixed together to meet user I/O requirements. In addition, a variety of channels are available for transferring data between the CPU (or main memory) and external devices via the high-speed system data bus.

An Industry First: Communications Network Processor

One of the unique features of the Harris CPU is its high performance communications front-end processor. The communications network processor (CNP) is essentially a microprocessor-based front-end computer with a high degree of intelligence. Multiple CNPs can be used in any Harris system to support a wide selection of communications options.

Each CNP is capable of supporting the following:

- Network Processing (utilizing the X.25 protocol)
- RJE (with a large number of mainframe protocols either as a terminal or as a host)
- Interactive Communications (including ASCII and Teletype)

An individual CNP can support up to 16 communications ports. Each of these ports can support a different protocol at different speeds. Speeds range from 110 cps for low-speed devices to a maximum of 1.54 megabits per second for network processing.

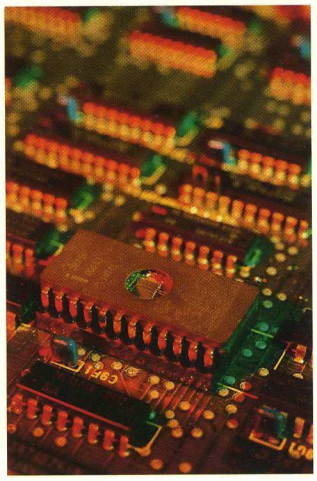
Each port can be individually loaded with its appropriate communications protocol by the addition of daughterboard ports to the main front-end processor.

Within the super-minicomputer industry, the CNP is a unique device, offering unusual flexibility, performance and extendibility. No other vendor offers such a high performance and flexible front-end processor to support all communications modes. Only Harris offers synchronous, asynchronous and network processing on a single, instantly reconfigurable board.

In addition to the CNP, Harris provides a wide variety of channels and controllers including the following:

Buffered Block Channel (BBC)

This channel is central to the Harris system and is used for both disks and tapes. The BBC offers a 48-byte buffer as well as dual priority busses to maximize system bus utilization. It is extremely



flexible and can be reconfigured for a wide variety of high performance devices. For example, Harris BBCs have been modified to support parallel graphic devices, real-time devices and a variety of analog-to-digital converters. Only Harris offers the extremely flexible BBC to support various devices through direct memory access at high throughput rates (up to 2.7 megabytes per second).

Universal Block Channel (UBC)

The universal block mode channel is a high-speed direct memory access channel for use with high-speed peripheral controllers. Using a single UBC in scan mode, two concurrent input/output operations can be supported, providing the user with the capabilities of two separate I/O channels. The maximum transfer rate of the UBC is 3.2 megabytes per second, input; 2.5 megabytes per second, output.

External Block Channel (XBC)

The external block channel is a specialized direct memory access channel for user-developed controllers and devices which are independently timed and controlled. The XBC provides the user with the flexibility to interface special, custom-made devices to Harris computers.

Programmed Input/Output Channel (PIOC)

This channel is used to interface up to four low-speed device controllers to the CPU. It functions under program control to transfer data between a CPU register and the channel. Typically, the PIOC is used for the operator's console, low- and high-speed printers and a small number of terminals. A PIOC is included with every Harris CPU.

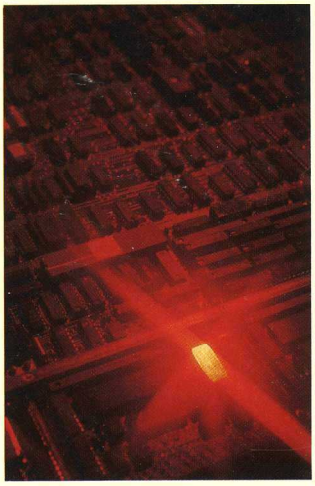
Communications Multiplexer (COMM MUX)

This multiport I/O channel is useful for low-speed interactive devices, especially communications devices using the RS232 protocols. The COMM MUX provides an economical alternative for the user while offering capabilities consistent with low-end requirements.

Harris Software: Extensive Offerings

While the hardware provides the necessary foundation for the performance, compatibility and flexibility of all Harris computers, the software adds to this capability in a manner unmatched by any other vendor. Harris has a strong reputation for the effectiveness of its language processors and, in fact, was one of the first minicomputer vendors to have both FORTRAN and COBOL fully validated by the U.S. government.

Harris also provides a wide selection of software for data management, report writing, financial modeling and an enormous selection of application programs in the engineering, technical, scientific and financial areas. Many of these programs have been developed by Harris users and development firms, leaders in their respective fields. These programs are available on Harris machines through license with these vendors.



With efficient archit[illegible] flexible memory implementations and a versatile I/O structure, Harris computers excel in the most demanding environments. These features, coupled with extensive software offerings and superior support services, provide Harris users with the tools to solve today's most challenging computing problems. Whether in benchmark situations or in the field, Harris computers offer unparalleled price/performance for scientific, engineering, educational and related applications.

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