BIPOLAR
DIGITAL DATA BOOK

Part of the Harris Spectrum
of Integrated Circuits

HARRIS

$5.00

1984 Harris Bipolar Digital Data Book

Harris Semiconductor Bipolar Digital Products represent state-of-the-art production in density and performance. HARRIS expertise in design and processing offers the user leadership in quality and reliability of products in a wide choice of formats, options, and package types. With continuing research and development and the introduction of new products, Harris will provide its customers with the most advanced technology.

This book describes Harris Semiconductor Digital Products Division's complete line of bipolar memory and programmable logic products, including a complete set of product specifications and data sheets. Also included are sections on reliability, programming, packaging, and custom/semi-custom capabilities.

Please fill out the request for information/action card at the back of this book and return it to us so we may keep you informed of our latest new product developments over the next year.

If you need more information on these and other HARRIS products, please contact the nearest HARRIS sales office listed in the back of this data book.

Harris Semiconductor's products are sold by description only. HARRIS reserves the right to make changes in circuit design, specifications and other information at any time without prior notice. Accordingly, the reader is cautioned to verify that data sheets and other information in this publication are current before placing orders. Information contained in application notes is intended soley for general guidance; use of the information for user's specific application is at user's risk. Reference to products of other manufacturers are solely for convenience of comparison and do not imply total equivalence of design, performance, or otherwise.

Printed in USA

BIPOLAR 1984 Digital Data Book

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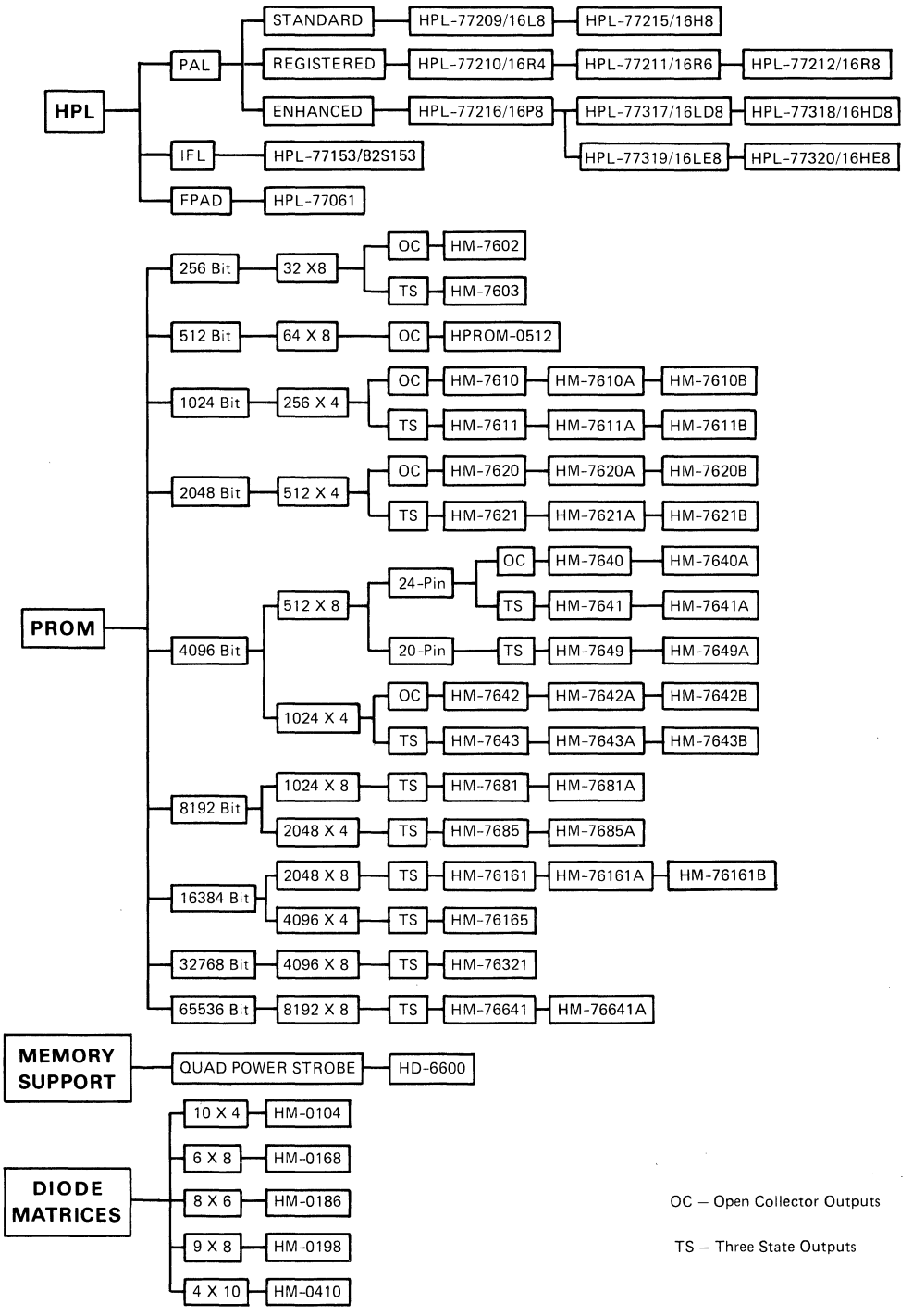
Bipolar Alpha-Numeric Index

Bipolar Family Tree



OC – Open Collector Outputs

TS – Three State Outputs

Bipolar PROM Cross-Reference

AMD PART NUMBER	ORGANIZATION AND OUTPUT	HARRIS PIN-FOR-PIN REPLACEMENT
27S18 27S18A	32 X 8 OC	HM-7602
27S19 27S19A	32 X 8 TS	HM-7603
27S20 27S20A	256 X 4 OC	HM-7610 HM-7610A HM-7610B
27S21 27S21A	256 X 4 TS	HM-7611 HM-7611A HM-7611B
27S12 27S12A	512 X 4 OC	HM-7620 HM-7620A HM-7620B
27S13 27S13A	512 X 4 TS	HM-7621 HM-7621A HM-7621B
27S30 27S30A	512 X 8 OC	HM-7640 HM-7640A
27S31 27S31A	512 X 8 TS	HM-7641 HM-7641A
27S29 27S29A	512 X 8 TS	HM-7649 HM-7649A
27S32 27S32A	1024 X 4 OC	HM-7642 HM-7642A HM-7642B
27S33 27S33A	1024 X 4 TS	HM-7643 HM-7643A HM-7643B
27S181 27S181A	1024 X 8 TS	HM-7681 HM-7681A
27S185 27S185A	2048 X 4 TS	HM-7685 HM-7685A
27S191 27S191A	2048 X 8 TS	HM-76161 HM-76161A HM-76161B
27S41 27S41A	4096 X 4 TS	HM-76165
27S43 27S43A	4096 X 8 TS	HM-76321

FAIRCHILD PART NUMBER	ORGANIZATION AND OUTPUT	HARRIS PIN-FOR-PIN REPLACEMENT
93417	256 X 4 OC	HM-7610 HM-7610A HM-7610B
93427	256 X 4 TS	HM-7611 HM-7611A HM-7611B
93436	512 X 4 OC	HM-7620 HM-7620A HM-7620B
93446	512 X 4 TS	HM-7621 HM-7621A HM-7621B
93438	512 X 8 OC	HM-7640 HM-7640A
93448	512 X 8 TS	HM-7641 HM-7641A
93452	1024 X 4 OC	HM-7642 HM-7642A HM-7642B
93453	1024 X 4 TS	HM-7643 HM-7643A HM-7643B
93451 93Z451	1024 X 8 TS	HM-7681 HM-7681A
93Z511	2048 X 8 TS	HM-76161 HM-76161A HM-76161B
93515	4096 X 4 TS	HM-76165
93Z565 93Z565A	8192 X 8 TS	HM-76641 HM-76641A

Bipolar PROM Cross-Reference (Continued)

FUJITSU PART NUMBER	ORGANIZATION AND OUTPUT	HARRIS PIN-FOR-PIN REPLACEMENT
MB7124E MB7124H	512 X 8 TS	HM-7649 HM-7649A
MB7121E MB7121H	1024 X 4 OC	HM-7642 HM-7642A HM-7642B
MB7122E MB7122H	1024 X 4 TS	HM-7643 HM-7643A HM-7643B
MB7132E MB7132H	1024 X 8 TS	HM-7681 HM-7681A
MB7128E MB7128H	2048 X 4 TS	HM-7685 HM-7685A
MB7138E MB7138H	2048 X 8 TS	HM-76161 HM-76161A HM-76161B
MB7134E MB7134H	4096 X 4 TS	HM-76165
MB7142E MB7142H	4096 X 8 TS	HM-76321
MB7144E MB7144H	8192 X 8 TS	HM-76641 HM-76641A

HITACHI PART NUMBER	ORGANIZATION AND OUTPUT	HARRIS PIN-FOR-PIN REPLACEMENT
HN25089 HN25089S	1024 X 8 TS	HM-7681 HM-7681A
HN25085 HN25085S	2048 X 4 TS	HM-7685 HM-7685A
HN25169 HN25169S	2048 X 8 TS	HM-76161 HM-76161A HM-76161B

INTEL PART NUMBER	ORGANIZATION AND OUTPUT	HARRIS PIN-FOR-PIN REPLACEMENT
3601 3601-1	256 X 4 OC	HM-7610 HM-7610A HM-7610B
3621 3621-1	256 X 4 TS	HM-7611 HM-7611A HM-7611B
3602 3602A 3602A-2	512 X 4 OC	HM-7620 HM-7620A HM-7620B
3622 3622A 3622A-2	512 X 4 TS	HM-7621 HM-7621A HM-7621B
3604-4 3604 3604A 3604A-2	512 X 8 OC	HM-7640 HM-7640A
3624-4 3624 3624A 3624A-2	512 X 8 TS	HM-7641 HM-7641A
3605 3605-2	1024 X 4 OC	HM-7642 HM-7642A HM-7642B
3625 3625-2	1024 X 4 TS	HM-7643 HM-7643A HM-7643B
3628A-4 3628A-3 3628A-1	1024 X 8 TS	HM-7681 HM-7681A
3636B 3636B-2 3636B-1	2048 X 8 TS	HM-76161 HM-76161A HM-76161B
3632 3632-1	4096 X 8 TS	HM-76321

Bipolar PROM Cross-Reference (Continued)

NEC PART NUMBER	ORGANIZATION AND OUTPUT	HARRIS PIN-FOR-PIN REPLACEMENT
μPB403	256 X 4 OC	HM-7610 HM-7610A HM-7610B
μPB423	256 X 4 TS	HM-7611 HM-7611A HM-7611B
μPB405	512 X 8 OC	HM-7640 HM-7640A
μPB425	512 X 8 TS	HM-7641 HM-7641A
μPB406	1024 X 4 OC	HM-7642 HM-7642A HM-7642B
μPB426	1024 X 4 TS	HM-7643 HM-7643A HM-7643B
μPB428	1024 X 8 TS	HM-7681 HM-7681A
μPB429	2048 X 8 TS	HM-76161 HM-76161A HM-76161B

INTERSIL PART NUMBER	ORGANIZATION AND OUTPUT	HARRIS PIN-FOR-PIN REPLACEMENT
IM5600	32 X 8 OC	HM-7602
IM5610	32 X 8 TS	HM-7603
IM5603	256 X 4 OC	HM-7610 HM-7610A HM-7610B
IM5623	256 X 4 TS	HM-7611 HM-7611A HM-7611B
IM5604	512 X 4 OC	HM-7620 HM-7620A HM-7620B
IM5624	512 X 4 TS	HM-7621 HM-7621A HM-7621B
IM5605	512 X 8 OC	HM-7640 HM-7640A
IM5625	512 X 8 TS	HM-7641 HM-7641A

Bipolar PROM Cross-Reference (Continued)

MMI PART NUMBER	ORGANIZATION AND OUTPUT	HARRIS PIN-FOR-PIN REPLACEMENT
6330-1	32 X 8 OC	HM-7602
6331-1	32 X 8 TS	HM-7603
6300-1 63S140	256 X 4 OC	HM-7610 HM-7610A HM-7610B
6301-1 63S141	256 X 4 TS	HM-7611 HM-7611A HM-7611B
6305-1 63S240	512 X 4 OC	HM-7620 HM-7620A HM-7620B
6306-1 63S241	512 X 4 TS	HM-7621 HM-7621A HM-7621B
6340-1 6340-2	512 X 8 OC	HM-7640 HM-7640A
6341-1 6341-2	512 X 8 TS	HM-7641 HM-7641A
6349-1 6349-2	512 X 8 TS	HM-7649 HM-7649A
6352-1	1024 X 4 OC	HM-7642 HM-7642A HM-7642B
6353-1	1024 X 4 TS	HM-7643 HM-7643A HM-7643B
6381-1 6381-2	1024 X 8 TS	HM-7681 HM-7681A
6389-1 6389-2	2048 X 4 TS	HM-7685 HM-7685A
63S1681	2048 X 8 TS	HM-76161 HM-76161A HM-76161B
63S1641	4096 X 4 TS	HM-76165
63S3281	4096 X 8 TS	HM-76321

MOTOROLA PART NUMBER	ORGANIZATION AND OUTPUT	HARRIS PIN-FOR-PIN REPLACEMENT
MCM7620	512 X 4 OC	HM-7620 HM-7620A HM-7620B
MCM7621	512 X 4 TS	HM-7621 HM-7621A HM-7621B
MCM7640	512 X 8 OC	HM-7640 HM-7640A
MCM7641	512 X 8 TS	HM-7641 HM-7641A
MCM7642	1024 X 4 OC	HM-7642 HM-7642A HM-7642B
MCM7643	1024 X 4 TS	HM-7643 HM-7643A HM-7643B
MCM7681	1024 X 8 TS	HM-7681 HM-7681A
MCM7685	2048 X 4 TS	HM-7685 HM-7685A
MCM76161	2048 X 8 TS	HM-76161 HM-76161A HM-76161B

Bipolar PROM Cross-Reference (Continued)

NATIONAL PART NUMBER	ORGANIZATION AND OUTPUT	HARRIS PIN-FOR-PIN REPLACEMENT
74S188 87S188	32 X 8 OC	HM-7602
74S288 87S288	32 X 8 TS	HM-7603
74S387	256 X 4 OC	HM-7610 HM-7610A HM-7610B
74S287	256 X 4 TS	HM-7611 HM-7611A HM-7611B
74S570 74S570A	512 X 4 OC	HM-7620 HM-7620A HM-7620B
74S571 74S571A	512 X 4 TS	HM-7621 HM-7621A HM-7621B
74S475 74S475A	512 X 8 OC	HM-7640 HM-7640A
74S474 74S474A 74S474B	512 X 8 TS	HM-7641 HM-7641A
74S472 74S472A 74S472B	512 X 8 TS	HM-7649 HM-7649A
74S572 74S572A	1024 X 4 OC	HM-7642 HM-7642A HM-7642B
74S573 74S573A 74S573B	1024 X 4 TS	HM-7643 HM-7643A HM-7643B
87S181 87S181A	1024 X 8 TS	HM-7681 HM-7681A
87S185 87S185A	2048 X 4 TS	HM-7685 HM-7685A
87S191 87S191A	2048 X 8 TS	HM-76161 HM-76161A HM-76161B

RAYTHEON PART NUMBER	ORGANIZATION AND OUTPUT	HARRIS PIN-FOR-PIN REPLACEMENT
29660	256 X 4 OC	HM-7610 HM-7610A HM-7610B
29661	256 X 4 TS	HM-7611 HM-7611A HM-7611B
29610	512 X 4 OC	HM-7620 HM-7620A HM-7620B
29611	512 X 4 TS	HM-7621 HM-7621A HM-7621B
29624	512 X 8 OC	HM-7640 HM-7640A
29625	512 X 8 TS	HM-7641 HM-7641A
29621 29621A	512 X 8 TS	HM-7649 HM-7649A
29635	1024 X 8 TS	HM-7681 HM-7681A
29651 29651A	2048 X 4 TS	HM-7685 HM-7685A
29681 29681A	2048 X 8 TS	HM-76161 HM-76161A HM-76161B
29641 29641A	4096 X 4 TS	HM-76165
29671 29671A	4096 X 8 TS	HM-76321

Bipolar PROM Cross-Reference (Continued)

SIGNETICS PART NUMBER	ORGANIZATION AND OUTPUT	HARRIS PIN-FOR-PIN REPLACEMENT
82S23	32 X 8 OC	HM-7602
82S123	32 X 8 TS	HM-7603
82S126	256 X 4 OC	HM-7610 HM-7610A HM-7610B
82S129	256 X 4 TS	HM-7611 HM-7611A HM-7611B
82S130	512 X 4 OC	HM-7620 HM-7620A HM-7620B
82S131	512 X 4 TS	HM-7621 HM-7621A HM-7621B
82S140	512 X 8 OC	HM-7640 HM-7640A
82S141	512 X 8 TS	HM-7641 HM-7641A
82S147 82HS147	512 X 8 TS	HM-7649 HM-7649A
82S136	1024 X 4 OC	HM-7642 HM-7642A HM-7642B
82S137 82S137A 82S137B	1024 X 4 TS	HM-7643 HM-7643A HM-7643B
82S181 82S181A 82S181B	1024 X 8 TS	HM-7681 HM-7681A
82S185 82S185A 82S185B	2048 X 4 TS	HM-7685 HM-7685A
82S191 82HS191	2048 X 8 TS	HM-76161 HM-76161A HM-76161B
82S195 82HS195	4096 X 4 TS	HM-76165
82S321	4096 X 8 TS	HM-76321

T. I. PART NUMBER	ORGANIZATION AND OUTPUT	HARRIS PIN-FOR-PIN REPLACEMENT
SN74S188 TBP18SA030	32 X 8 OC	HM-7602
SN74S288 TBP18S030	32 X 8 TS	HM-7603
SN74S387 TBP14SA10 TBP24SA10	256 X 4 OC	HM-7610 HM-7610A HM-7610B
SN74S287 TBP14S10 TBP24S10	256 X 4 TS	HM-7611 HM-7611A HM-7611B
SN74S475 TBP18SA46 TBP28SA46	512 X 8 OC	HM-7640 HM-7640A
SN74SA74 TBP18S46 TBP28S46	512 X 8 TS	HM-7641 HM-7641A
SN74S472 TBP18S42 TBP28S42	512 X 8 TS	HM-7649 HM-7649A
SN74S477 TBP24SA41	1024 X 4 OC	HM-7642 HM-7642A HM-7642B
SN74S476 TBP24S41	1024 X 4 TS	HM-7643 HM-7643A HM-7643B
SN74S478 TBP28S86	1024 X 8 TS	HM-7681 HM-7681A
SN74S454 TBP24S81	2048 X 4 TS	HM-7685 HM-7685A
TBP28S166	2048 X 8 TS	HM-76161 HM-76161A HM-76161B

Bipolar HPL Cross-Reference

AMD PART NUMBER	ARRAY INPUTS	MATRIX ARCHITECTURE	LOGIC	HARRIS PART NUMBER
AmPAL16L8	Ten Dedicated Six Bidirectional	Programmable AND-Fixed OR	Eight 7-Wide AND-OR-INVERT (Active Low Outputs)	HPL-77209 /16L8
AmPAL16H8	Ten Dedicated Six Bidirectional	Programmable AND-Fixed OR	Eight 7-Wide AND-OR (Active High Outputs)	HPL-77215 /16H8
AmPAL16LD8	Ten Dedicated Six Feedback	Programmable AND-Fixed OR	Eight 8-Wide AND-OR-INVERT (Active Low Outputs)	HPL-77317 /16LD8
AmPAL16HD8	Ten Dedicated Six Feedback	Programmable AND-Fixed OR	Eight 8-Wide AND-OR (Active High Outputs)	HPL-77318 /16HD8
AmPAL16R4	Eight Dedicated Four Feedback Four Bidirectional	Programmable AND-Fixed OR	Four 8-Wide AND-OR Four 7-Wide AND-OR-INVERT	HPL-77210 /16R4
AmPAL16R6	Eight Dedicated Six Feedback Two Bidirectional	Programmable AND-Fixed OR	Six 8-Wide AND-OR Two 7-Wide AND-OR-INVERT	HPL-77211 /16R6
AmPAL16R8	Eight Dedicated Eight Feedback	Programmable AND-Fixed OR	Eight 8-Wide AND-OR	HPL-77212 /16R8

MMI PART NUMBER	ARRAY INPUTS	MATRIX ARCHITECTURE	LOGIC	HARRIS PART NUMBER
PAL16L8	Ten Dedicated Six Bidirectional	Programmable AND-Fixed OR	Eight 7-Wide AND-OR-INVERT (Active Low Outputs)	HPL-77209 /16L8
PAL16H8	Ten Dedicated Six Bidirectional	Programmable AND-Fixed OR	Eight 7-Wide AND-OR (Active High Outputs)	HPL-77215 /16H8
PAL16R4	Eight Dedicated Four Feedback Four Bidirectional	Programmable AND-Fixed OR	Four 8-Wide AND-OR Four 7-Wide AND-OR-INVERT	HPL-77210 /16R4
PAL16R6	Eight Dedicated Six Feedback Two Bidirectional	Programmable AND-Fixed OR	Six 8-Wide AND-OR Two 7-Wide AND-OR-INVERT	HPL-77211 /16R6
PAL16R8	Eight Dedicated Eight Feedback	Programmable AND-Fixed OR	Eight 8-Wide AND-OR	HPL-77212 /16R8

Bipolar HPL Cross-Reference (Continued)

NATIONAL PART NUMBER	ARRAY INPUTS	MATRIX ARCHITECTURE	LOGIC	HARRIS PART NUMBER
PAL16L8	Ten Dedicated Six Bidirectional	Programmable AND-Fixed OR	Eight 7-Wide AND-OR-INVERT (Active Low Outputs)	HPL-77209 /16L8
PAL16R4	Eight Dedicated Four Feedback Four Bidirectional	Programmable AND-Fixed OR	Four 8-Wide AND-OR Four 7-Wide AND-OR-INVERT	HPL-77210 /16R4
PAL16R6	Eight Dedicated Six Feedback Two Bidirectional	Programmable AND-Fixed OR	Six 8-Wide AND-OR Two 7-Wide AND-OR-INVERT	HPL-77211 /16R6
PAL16R8	Eight Dedicated Eight Feedback	Programmable AND-Fixed OR	Eight 8-Wide AND-OR	HPL-77212 /16R8

T. I. PART NUMBER	ARRAY INPUTS	MATRIX ARCHITECTURE	LOGIC	HARRIS PART NUMBER
FP74ALS16L8	Ten Dedicated Six Bidirectional	Programmable AND-Fixed OR	Eight 7-Wide AND-OR-INVERT (Active Low Outputs)	HPL-77209 /16L8
FP74ALS16R4	Eight Dedicated Four Feedback Four Bidirectional	Programmable AND-Fixed OR	Four 8-Wide AND-OR Four 7-Wide AND-OR-INVERT	HPL-77210 /16R4
FP74ALS16R6	Eight Dedicated Six Feedback Two Bidirectional	Programmable AND-Fixed OR	Six 8-Wide AND-OR Two 7-Wide AND-OR-INVERT	HPL-77211 /16R6
FP74ALS16R8	Eight Dedicated Eight Feedback	Programmable AND-Fixed OR	Eight 8-Wide AND-OR	HPL-77212 /16R8

SIGNETICS PART NUMBER	ARRAY INPUTS	MATRIX ARCHITECTURE	LOGIC	HARRIS PART NUMBER
82S153	Eight Dedicated Ten Bidirectional	Programmable AND-Prog. OR	Ten 32-Wide AND-OR (Programmable Output Polarity)	HPL-77153 /82S153

PROM Functional Index and Selection Guide

PART NUMBER	ORGANIZATION	OUTPUT	NUMBER OF PINS	T_{AA} COMMERCIAL/ MILITARY (ns MAX)	I_{CC} (mA MAX)	(1) PACKAGE AVAILABILITY	PAGE
HM-7602	32 x 8	OC	16	50/60	130	D, P	4-13
HM-7603	32 x 8	TS	16	50/60	130	D, P	4-13
JAN-0512	64 x 8	OC	24	140/140	100	D, F	4-51
HM-7610 HM-7610A HM-7610B	256 x 4	OC	16	60/75 45/65 35/50	130 110 110	D, P, F	4-16
HM-7611 HM-7611A HM-7611B	256 x 4	TS	16	60/75 45/65 35/50	130 110 110	D, P, F	4-16
HM-7620 HM-7620A HM-7620B	512 x 4	OC	16	70/85 50/70 40/55	130 120 120	D, P, F	4-19
HM-7621 HM-7621A HM-7621B	512 x 4	TS	16	70/85 50/70 40/55	130 120 120	D, P, F	4-19
HM-7640 HM-7640A	512 x 8	OC	24	70/85 50/65	170 170	D, P, F, SD	4-22
HM-7641 HM-7641A	512 x 8	TS	24	70/85 45/60	170 170	D, P, F, SD	4-22
HM-7649 HM-7649A	512 x 8	TS	20	60/80 45/60	170 170	D, P, F	4-28
HM-7642 HM-7642A HM-7642B	1024 x 4	OC	18	60/85 50/70 45/55	140 140 140	D, P, F	4-25
HM-7643 HM-7643A HM-7643B	1024 x 4	TS	18	60/85 50/70 45/55	140 140 140	D, P, F	4-25
HM-7681 HM-7681A	1024 x 8	TS	24	70/90 50/—	170 170	D, P, L, F, SD	4-31
HM-7685 HM-7685A	2048 x 4	TS	18	70/90 50/60	170 170	D, P	4-34
HM-76161 HM-76161A HM-76161B	2048 x 8	TS	24	60/80 50/— 35/—	180 180 180	D, P, L, F, SD	4-37 4-37 4-40
HM-76165	4096 x 4	TS	20	60/80	170	D	4-41
HM-76321	4096 x 8	TS	24	65/85	190	D, L	4-44
HM-76641 HM-76641A	8192 x 8	TS	24	85/100 50/—	190 190	D, L	4-47 4-50

(1) D = Ceramic DIP; P = Plastic DIP; L = Leadless Chip Carrier; F = Flatpack; SD = Slimline Ceramic DIP

HPL Functional Index and Selection Guide

PART NUMBER	ARRAY INPUTS	MATRIX ARCHITECTURE	LOGIC	OUTPUT ENABLE	OUTPUTS	PROPAGATION DELAY 0°C to +75°C	REGISTER SETUP TIME 0°C to +75°C	CLOCK TO OUTPUT TIME 0°C to +75°C	PAGE
HPL-77061	Twelve Dedicated Six Bidirectional	Programmable AND-Fixed OR	Ten 2-Wide AND-OR (Programmable Output Polarity)	Programmable	Six Bidirectional Four Dedicated	25 nsec	–	–	5-4
HPL-77153 /82S153	Eight Dedicated Ten Bidirectional	Programmable AND-Prog. OR	Ten 32-Wide AND-OR (Programmable Output Polarity)	Programmable	Ten Bidirectional	40 nsec	–	–	5-6
HPL-77209 /16L8	Ten Dedicated Six Bidirectional	Programmable AND-Fixed OR	Eight 7-Wide AND-OR-INVERT (Active Low Outputs)	Programmable	Six Bidirectional Two Dedicated	35 nsec	–	–	5-15
HPL-77210 /16R4	Eight Dedicated Four Feedback Four Bidirectional	Programmable AND-Fixed OR	Four 8-Wide AND-OR Four 7-Wide AND-OR-INVERT	Dedicated Programmable	Four Registered Four Bidirectional	35 nsec	35 nsec	25 nsec	5-42
HPL-77211 /16R6	Eight Dedicated Six Feedback Two Bidirectional	Programmable AND-Fixed OR	Six 8-Wide AND-OR Two 7-Wide AND-OR-INVERT	Dedicated Programmable	Six Registered Two Bidirectional	35 nsec	35 nsec	25 nsec	5-42
HPL-77212 /16R8	Eight Dedicated Eight Feedback	Programmable AND-Fixed OR	Eight 8-Wide AND-OR	Dedicated	Eight Registered	–	35 nsec	25 nsec	5-42
HPL-77215 /16H8	Ten Dedicated Six Bidirectional	Programmable AND-Fixed OR	Eight 7-Wide AND-OR (Active High Outputs)	Programmable	Six Bidirectional Two Dedicated	35 nsec	–	–	5-15
HPL-77216 /16P8	Ten Dedicated Six Bidirectional	Programmable AND-Fixed OR	Eight 7-Wide AND-OR (Programmable Output Polarity)	Programmable	Six Bidirectional Two Dedicated	35 nsec	–	–	5-15
HPL-77317 /16LD8	Ten Dedicated Six Feedback	Programmable AND-Fixed OR	Eight 8-Wide AND-OR-INVERT (Active Low Outputs)	–	Eight Dedicated	35 nsec	–	–	5-24
HPL-77318 /16HD8	Ten Dedicated Six Feedback	Programmable AND-Fixed OR	Eight 8-Wide AND-OR (Active High Outputs)	–	Eight Dedicated	35 nsec	–	–	5-24
HPL-77319 /16LE8	Ten Dedicated Six Fuse Selectable	Programmable AND-Fixed OR	Eight 8-Wide AND-OR-INVERT (Active Low Outputs)	Six Single-Fuse Programmable	Six Fuse Selectable Two Dedicated	35 nsec	–	–	5-33
HPL-77320 /16HE8	Ten Dedicated Six Fuse Selectable	Programmable AND-Fixed OR	Eight 8-Wide AND-OR (Active High Outputs)	Six Single-Fuse Programmable	Six Fuse Selectable Two Dedicated	35 nsec	–	–	5-33

NOTE: All HPL products are available in Ceramic and Plastic DIPs. Please see section 9 (Packaging) of this Data Book.

Harris Semiconductor
Sector Overview

Harris Semiconductor is one of the five management groups of Harris Corporation, a producer of high-technology communication and information processing systems sold in over 160 countries. Four main operations of Harris Semiconductor produce standard and custom semiconductor devices. These operations are:

ANALOG PRODUCTS DIVISION

Harris is a major force in analog integrated circuitry, offering a broad line of products including: analog-to-digital converters, digital-to-analog converters, switches, multiplexers, voltage references, operational amplifiers, speech processing products, telecommunications filters, and Subscriber Loop Interface Circuits (SLIC).

DIGITAL PRODUCTS DIVISION

Harris introduced the industry's first bipolar programmable read only memory (PROM) in 1970, and has continued as a leader in the field of bipolar PROMs. Harris offers a complete spectrum of bipolar PROMs from 256 bits to 64K bits. In 1982, Harris became the first supplier of a new family of programmable logic (HPL) featuring patented on-chip testability. The Harris line includes both programmable array logic and integrated fuse logic architectures.

Harris is a pioneer in developing and producing digital CMOS products including: CMOS RAMs, CMOS PROMs, CMOS microprocessors, CMOS peripherals, CMOS data communications products; and introduced a full line of 80CXX products and peripherals in 1983.

CUSTOM INTEGRATED CIRCUITS DIVISION

Harris designs, develops and manufactures custom analog, digital bipolar, radiation-hardened, and CMOS circuits for specialized military and commercial applications.

MICROWAVE SEMICONDUCTOR, INC.

Harris Microwave Semiconductor, Inc., develops and manufactures gallium arsenide transistors, integrated circuits and microwave amplifiers.

Classification of Literature

CLASSIFICATION	PRODUCT STAGE	DISCLAIMERS
Preview DATA SHEET	Formative or Design	This document contains the design specifications for product under development. Specifications may be changed in any manner without notice.
Advance Information DATA SHEET	Sampling or Pre-Production	This is advanced information, and specifications are subject to change without notice.
Preliminary DATA SHEET	First Production	Supplementary data may be published at a later date. Harris reserves the right to make changes at any-time without notice, in order to improve design and supply the best product possible.

I. C. Handling Procedures

Harris IC processes produce circuits more rugged than similar ones. However, no semiconductor is immune from damage resulting from the sudden application of many thousands of volts of static electricity. While the phenomenon of catastrophic failure of devices containing MOS transistors or capacitors is well known, even bipolar circuits can be damaged by static discharge, with altered electrical properties, and diminished reliability with resulting latent problems in the field. None of the common IC internal protection networks operates quickly enough to positively prevent damage.

It is therefore recommended that semiconductor integrated circuits be handled, tested, and installed using standard static control handling procedures consisting of the proper grounding of personnel, work area, and equipment. Parts and sub-assemblies should never be in contact with untreated (i.e., not-antistatic) plastic bags or wrapping materials. Especially high impedance IC inputs wired to a P.C. connector should have a path to ground on the card; placing conductive shunting bars across the PC connector is standard practice.

Specific Handling Rules

Since the introduction of integrated circuits with MOS structures and high quality (bipolar) junctions, a safe and effective means of handling integrated circuits has been of primary importance. If electrostatic discharge occurs at sufficient magnitude (2kV or more), some damage or degradation will usually occur. It has been found that handling equipment and personnel can generate static potentials well in excess of 10kV in a low humidity environment; thus, it becomes necessary for additional measures to be implemented to eliminate static. It is evident, therefore, that proper handling procedures or rules should be adopted.

To establish a static controlled environment when handling integrated circuits, the following procedures must be implemented:

- Do not remove product from its protective Faraday cage static shielding bags

(transparent or opaque) unless located at a static controlled work station with the person handling the product always grounded by a static controlled wrist strap. Remember that anti-static shipping tubes do not provide protection against electrostatic fields!

- The static controlled work station must consist of: (a) grounded dissipative covering $10^5 - 10^9$ ohms/square (never use metal as this will cause sudden discharge and a "zap" effect); (b) absence of any plastic objects (e.g., plastic bags, foam coffee cups, polystyrene "snow", etc.) on the bench; if the use of plastic containers and other similar objects is unavoidable, an ionized airblower must be used to neutralize the objects to eliminate the static field generated by these objects; (c) all equipment must be grounded.

- Ground all personnel handling the product with a static controlled wrist strap which includes a one megohm safety resistor. The latter is required to prevent electroshock injury. Insure that the wrist strap always makes contact to the bare skin (check with an ohmmeter), and if dry skin creates a contact problem, apply a hand lotion to the wrist. Since the wrist strap is the first line of defense against ESD damage, a daily check of the wrist strap is necessary.

- To avoid transient personnel (e.g., visiting supervisor) from inducing damaging electrostatic fields, the presence of an ionized airblower is essential. Transient personnel must never touch product unless also grounded by a wrist strap.

- Wear a conductive jacket/coat consisting of, e.g., 65% polyester, 34% cotton, and 1% stainless steel thread. The latter is essential to block out the electrostatic field generated by the clothing worn underneath. Grounding by means of the wrist strap will not help since clothing does not conduct, and therefore, will not bleed off the static charge.

- Use a static charge meter to insure that work stations and personnel do not generate/carry static charge.

- Keep dual in-line and LCC devices in their anti-static shipping tubes (or conductive foam protected containers if other package styles are used) as long as possible.

- Despite being grounded via the wrist strap, avoid directly touching the leads of the device.

- Always transport product inside a static shielding or non-transparent conductive bag.

- In dealing with automated handling equipment, the belt, chutes or other surfaces should be made of (or covered with) conducting material. If this is not possible, ionized airblowers or nuclear ionized bars may be a good alternative. Definite verification of any of these fixes will always be required.

For further detailed points, please consult Technical Brief # 52, which is available through Harris distribution.

Definition of Terms

This section will aid in explaining symbols (i.e., acronyms and data sheet parameters) which may be found throughout this data book. Please consult individual data sheets for specific test conditions.

Acronyms

a-d	Analog to Digital
ALS	Advanced Low-Power Schottky
ALU	Arithmetic/Logic Unit
AOI	AND/OR Invert
ASCII	American National Standard Code for Information Intercharge
ATE	Automatic Test Equipment
CAD	Computer-Aided Design
d-a	Digital to Analog
DI	Dielectric Isolation
DIP	Dual In-Line Package
EBCDIC	Extended Binary Coded-Decimal Interchange Code
ECL	Emitter-Coupled Logic
EEPROM	Electrically Erasable PROM
EFL	Emitter-Follower Logic
EPROM	Erasable Programmable Read Only Memory
ESD	Electrostatic Discharge
FET	Field-Effect Transistor
FPAD	Field Programmable Address Decoder
FPLA	Field Programmable Logic Array
FPGA	Field Programmable Gate Array
FPLS	Field Programmable Logic Sequencer
HELP	Harris Enhanced Language for Programmable Logic
HPL	Harris Programmable Logic
IC	Integrated Circuit
IFL	Integrated Fuse Logic
I/O	Input/Output
IPOS	Inverted Product of Sums
ISOP	Inverted Sum of Products
JAN	Joint Army Navy
JFET	Junction Field Effect Transistor
JI	Junction Isolation
LCC	Leadless Chip Carrier
LSI	Large Scale Integration
LSTTL	Low Power Schottky Transistor-Transistor Logic
MOS	Metal Oxide Semiconductor
μP	Microprocessor
MPU	Microprocessor Unit
MSI	Medium Scale Integration
MTBF	Mean Time Between Failure
MTTF	Mean Time to Failure
NAND	Inverted AND Gate
NiCr	Nickel-Chromium
OE	Open Emitter
OC	Open Collector
PAL™	Programmable Array Logic
PLA	Programmable Logic Array
PLL	Phase Locked Loop
POS	Product of Sums
PPFY	Post Programming Functional Yield
PROM	Programmable Read Only Memory
PT	Product Term
QPL	Qualified Product Line
ROM	Read Only Memory
R/W	Read/Write
SOP	Sum of Products
SSI	Small Scale Integration
STL	Schottky Transistor Logic
TS	Three-State
TTL	Transistor-Transistor Logic
VLSI	Very Large Scale Integration
XOR	Exclusive OR Gate

Data Sheet Parameters

PROMs and PROGRAMMABLE LOGIC

Defined below are the symbols for parameters which apply to PROMs and PROGRAMMABLE LOGIC.

I_{IH} – **High-level input current.** The current into * an input when a high-level voltage is applied to that input.

I_{IL} – **Low-level input current.** The current into * an input when a low-level voltage is applied to that input.

V_{IH} – **High-level input voltage.** An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables.
NOTE: A minimum is specified that is the least positive value of high-level voltage for which operation of the logic element within specification limits is guaranteed.

V_{IL} – **Low-level input voltage.** An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables.
NOTE: A maximum is specified that is the most positive value of low-level input voltage for which operation of the logic

* Current out of a terminal is given as a negative value.

TM PAL is a trademark of Monolithic Memories Incorporated

element within specification limits is guaranteed.

I_{OH} – **High-level output current.** The current into * an output with input conditions applied that according to the product specification will establish a high level at the output.

I_{OL} – **Low-level output current.** The current into * an output with input conditions applied that according to the product specification will establish a low level at the output.

V_{OH} – **High-level output voltage.** The voltage at an output terminal with input conditions applied that according to the product specification will establish a high level at the output.

V_{OL} – **Low-level output voltage.** The voltage at an output terminal with input conditions applied that according to the product specification will establish a low level at the output.

I_{OHE} – **Output disable current (High).** The current into * an output (with a logical high voltage level applied to the output) when the input conditions are such that, according to the product specification, the output is in the high impedance state.

I_{OLE} – **Output disable current (Low).** The current into * an output (with a logical low voltage level applied to that output) when the input conditions are such that, according to the product specification, the output is in the high impedance state.

V_{CL} – **Input clamp voltage.** An input voltage in a region of relatively low differential resistance that serves to limit the input voltage swing.

I_{OS} – **Short-circuit output current.** The current into * an output when that output is short-circuited to ground (or other specified potential) with input conditions applied to establish the output logic level farthest from ground potential (or other specified potenial).

I_{CC} – **Supply Current.** The current into * the V_{CC} supply terminal of an integrated circuit.

PROMs

Defined below are symbols for parameters which apply to PROMs ONLY.

T_{AA} – is the address (to output) access time of memory devices.

T_{EA} – is the output enable access time of memory devices.

T_{DA} – is the output disable (enable recovery) time of memory devices.

C_{INA} – **Input Capacitance, Address Input.** The capacitance between an address input and ground.

C_{INCE} – **Input Capacitance, Output Enable Input.** The capacitance between an output enable input and ground.

C_{OUT} – **Output Capacitance.** The capacitance between an output pin and ground.

Programmable Logic

Defined below are the symbols for parameters which apply to PROGRAMMABLE LOGIC ONLY.

I_{FZH} – **Output Current, High-Z State.** The current into * an output pin when it is the high impedance state and a high-level voltage is applied to that pin.

I_{FZL} – **Output Current, High-Z State.** The current into * an output pin when it is the high impedance state and a low-level voltage is applied to that pin.

I_{BZH} – **Bidirectional Pin Current, High-Z State.** The current into * a bidirectional pin when a high-level voltage is applied to that pin.

I_{BZL} – **Bidirectional Pin Current, High-Z State.** The current into * a bidirectional pin when a low-level voltage is applied to that pin.

C_I – **Input Capacitance.** The capacitance between an input pin and ground.

C_B – **Bidirectional Pin Capacitance.** The capacitance between a bidirectional pin and ground.

C_F – **Output Capacitance.** The capacitance between an output pin and ground.

* Current out of a terminal is given as a negative value.

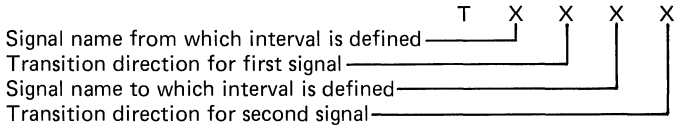
Timing Symbols for Harris Programmable Logic (HPL)

This data book utilizes a new set of timing specification nomenclature applicable to Harris Programmable Logic (HPL). This new format is derived from an IEEE and JEDEC supported standard for semiconductor memories. It is intended to clarify the symbols, abbreviations

and definitions, and to make all memory data sheets consistent. We believe that once acclimated, you will find this standard format easy to read and use.

Timing Parameter Abbreviations

All timing abbreviations use upper case characters with no subscripts. The initial character is always T and is followed by four descriptors. ** These characters specify two signal points arranged in a "from to" sequence that defines a timing interval. The two descriptors for each signal point specify the signal name and the signal transitions. Thus, the format is:

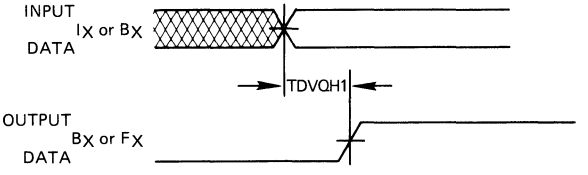


Signal Definitions:	Transition Definitions:
A = Address	H = Transition to High
D = Data In	L = Transition to Low
Q = Data Out	V = Transition to Valid
E = Chip Enable	X = Transition to Invalid or Don't Care
S = Chip Select	Z = Transition to Off (High Impedance)
G = Output Enable	

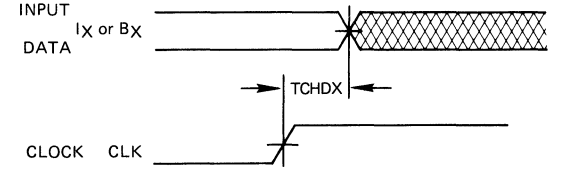
** NOTE: It is possible that four descriptors may not exclusively define all possible timing parameters. In this case, it is acceptable to add an extra descriptor (i.e., 1 or 2) to the end of the symbol.

Examples:

A) TDVQH1 – Propagation Delay – Input or I/O to Active High Output



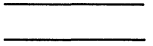
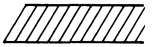
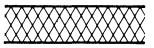
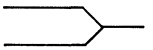
B) TCHDX – Data Hold Time



Timing Limits

The table of timing values on each data sheet shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address set up time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

Waveforms

WAVEFORM SYMBOL	INPUT	OUTPUT
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	—	HIGH IMPEDANCE

Quad Power Strobe (HD-6600)

Defined below are the symbols for parameters which apply to the QUAD POWER STROBE ONLY.

I_{IR} – **High-level input current.** The current into * an input when a high-level voltage is applied to that input.

I_{IF} – **Low-level input current.** The current into * an input when a low-level voltage is applied to that input.

t_{on} – **Turn On Delay.**

t_{off} – **Turn Off Delay.**

t_r – **Rise Time.**

t_f – **Fall Time.**

* Current out of a terminal is given as a negative value.

Monolithic Diode Matrices (HM-0XXX)

Defined below are the symbols for parameters which apply to the MONOLITHIC DIODE MATRICES ONLY.

V_F – **Foward Voltage.**

BV_R – **Reverse Breakdown Voltage.**

t_{rr} – **Reverse Recovery Time.**

C_C – **Crosspoint Capacitance.**

BIPOLAR

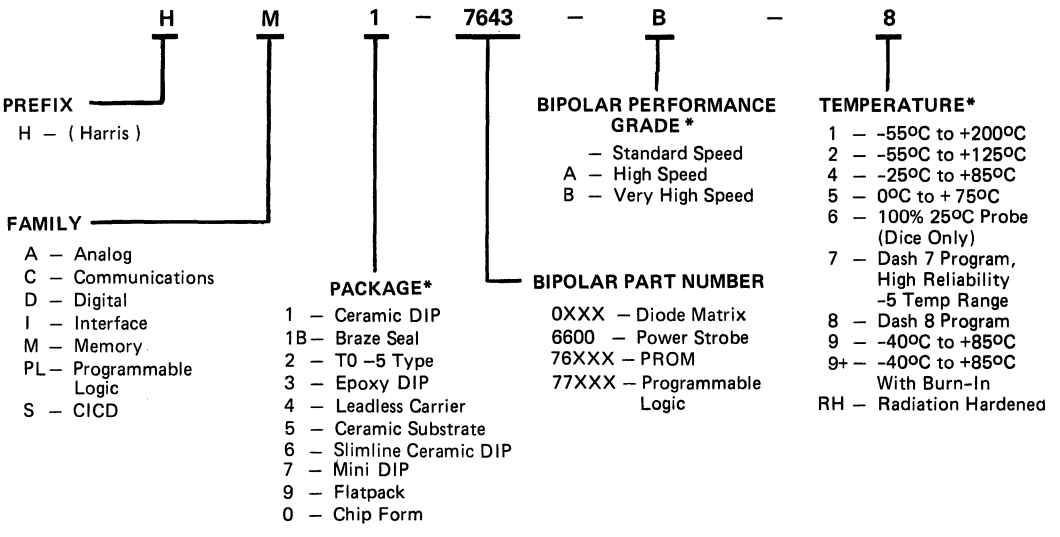
Ordering Information

2

Bipolar Alpha-Numeric Index

PART NUMBER	DESCRIPTION
HD-6600	Quad Power Strobe
HM-0104	10 x 4 Diode Matrix
HM-0168	6 x 8 Diode Matrix
HM-0186	8 x 6 Diode Matrix
HM-0198	9 x 8 Diode Matrix
HM-0410	4 x 10 Diode Matrix
HM-7602/03	32 x 8 Bit Generic PROM
HM-7610/11	256 x 4 Bit Generic PROM
HM-7610A/11A	256 x 4 Bit High Speed Generic PROM
HM-7610B/11B	256 x 4 Bit Very High Speed Generic PROM
HM-7620/21	512 x 4 Bit Generic PROM
HM-7620A/21A	512 x 4 Bit High Speed Generic PROM
HM-7620B/21B	512 x 4 Bit Very High Speed Generic PROM
HM-7640/41	512 x 8 Bit Generic PROM (24-Pin)
HM-7640A/41A	512 x 8 Bit High Speed Generic PROM (24-Pin)
HM-7649	512 x 8 Bit Generic PROM (20-Pin)
HM-7649A	512 x 8 Bit High Speed Generic PROM (20-Pin)
HM-7642/43	1024 x 4 Bit Generic PROM
HM-7642A/43A	1024 x 4 Bit High Speed Generic PROM
HM-7642B/43B	1024 x 4 Bit Very High Speed Generic PROM
HM-7681	1024 x 8 Bit Generic PROM
HM-7681A	1024 x 8 Bit High Speed Generic PROM
HM-7685	2048 x 4 Bit Generic PROM
HM-7685A	2048 x 4 Bit High Speed Generic PROM
HM-76161	2048 x 8 Bit Generic PROM
HM-76161A	2048 x 8 Bit High Speed Generic PROM
HM-76161B	2048 x 8 Bit Very High Speed Generic PROM
HM-76165	4096 x 4 Bit Generic PROM
HM-76321	4096 x 8 Bit Generic PROM
HM-76641	8192 x 8 Bit Generic PROM
HM-76641A	8192 x 8 Bit High Speed Generic PROM
JAN-0512	64 x 8 HPROM
HPL-77061	24-Pin Field Programmable Address Decoder
HPL-77153/82S153	20-Pin Field Programmable Logic Array
HPL-77209/16L8	20-Pin Field Programmable Array Logic (Active Low Outputs)
HPL-77210/16R4	20-Pin Field Programmable Array Logic (Four Registered Outputs)
HPL-77211/16R6	20-Pin Field Programmable Array Logic (Six Registered Outputs)
HPL-77212/16R8	20-Pin Field Programmable Array Logic (Eight Registered Outputs)
HPL-77215/16H8	20-Pin Field Programmable Array Logic (Active High Outputs)
HPL-77216/16P8	20-Pin Field Programmable Array Logic (Programmable Output Polarity)
HPL-77317/16LD8	20-Pin Field Programmable Array Logic (Active Low Dedicated Outputs)
HPL-77318/16HD8	20-Pin Field Programmable Array Logic (Active High Dedicated Outputs)
HPL-77319/16LE8	20-Pin Field Programmable Array Logic (Enhanced HPL-77317/16LD8)
HPL-77320/16HE8	20-Pin Field Programmable Array Logic (Enhanced HPL-77318/16HD8)
M38510/20701BEB	32 x 8 Open Collector QPL1 PROM
M38510/20702BEB	32 x 8 Three State QPL1 PROM
M38510/20101BJB	64 x 8 Open Collector QPL1 PROM
M38510/20301BEB	256 x 4 Open Collector QPL1 PROM
M38510/20302BEB	256 x 4 Three State QPL1 PROM
M38510/20401BEB	512 x 4 Open Collector QPL1 PROM
M38510/20402BEB	512 x 4 Three State QPL1 PROM
M38510/20801BJB	512 x 8 Open Collector QPL1 PROM
M38510/20802BJB	512 x 8 Three State QPL1 PROM
M38510/20601BVB	1024 x 4 Open Collector QPL1 PROM
M38510/20602BVB	1024 x 4 Three State QPL1 PROM
M38510/20904BJB	1024 x 8 Three State QPL1 PROM
M38510/20902BVB	2048 x 4 Three State QPL1 PROM
M38510/21002BJB	2048 x 8 Three State QPL1 PROM

Product Code



* All products may not be available in all package, performance grade, and temperature options. Please consult the factory or your local Harris representative.

HARRIS DASH 8 PROGRAM

The Harris Dash 8 Program is designed to provide products screened to meet the needs of high rel users. The Dash 8 Program provides users with a cost savings by using a standard processing flow and allows for "off the shelf" delivery. Harris Dash 8 products are available worldwide from authorized distributors. For additional information on the Dash 8 processing flow, see Section 7 of this catalog, Hi-Rel.

JAN QUALIFIED PRODUCTS

JAN qualified products offer high rel users the highest level of quality and reliability available in a standard product. All Harris JAN qualified products are manufactured and tested in a government certified facility to MIL-M-38510, and applicable device slash sheet specifications. Quality conformance testing per Method 5005 for Group A, B, C and D, is completed on JAN qualified products prior to shipment. The use of a standard process flow in place of a custom flow, allows for cost savings and "off the shelf" delivery. The Harris nomenclature for JAN qualified devices is the same as the slash sheet number; e.g., MIL-M38510/20602BVB, is Harris Part Number 20602BVB. JAN qualified devices are available from authorized distributors.

SPECIAL ORDERS

Should a user need additional electrical or reliability screening not available in the standard products, Dash 8 program, or JAN qualified products, a special order may be requested. A request for quotation and a complete device specification or Source Control Drawing should be submitted through the local Harris sales office or sales representative.

Harris reserves the right to decline a quote or to request modification to special screening requirements.

BIPOLAR Quality and Reliability 3

Harris Quality & Reliability

Introduction

The Product Assurance Department at Harris Semiconductor Products Group is responsible for assuring that the quality and reliability of all products shipped to customers meet their requirements. During all phases of product fabrication, there are many independent visual and electrical checks performed by Product Assurance personnel.

Prior to shipment, a final inspection is performed at Quality Assurance Plant Clearance to insure that all requirements of the purchase order and customer specifications are met.

The following military documents provide the foundation for HARRIS Product Assurance Program.

MIL-M-38510D	"General Specification of Microcircuits"
MIL-Q-9858A	"Quality Program Requirements"
MIL-STD-883B	"Test Methods and Procedures for Microelectronics"
NASA Publication 200-3	"Inspection System Provisions"
MIL-C-45662A	"Calibration System Requirements"
MIL-I-4508A	"Inspection System Requirements"

The Harris Semiconductor Reliability and Quality Manual, which is available upon request, describes the total function and policies of the organization to assure product reliability and quality. All customers are encouraged to visit the Harris Semiconductor facilities and survey the deployment of the Product Assurance function.

Quality Control

The Quality Control Department consists of Process Control with Chemical Mix as an available supporting service.

Process Quality Control is responsible for quality engineering and controls in the wafer processing modules, assembly, mask and materials production areas, and electrical wafer probe.

The primary responsibilities of Process Quality Control are:

a. To establish and maintain effective controls for monitoring manufacturing processes and equipment;

b. to provide rapid feedback of information concerning the state of control;

c. to initiate, design, and develop statistically controlled experiments to further improve product reliability and quality levels.

Statistical control charts on processes and operating procedures are used in the manufacturing areas and in the evaluation of process and product parameters utilized to qualify new processes.

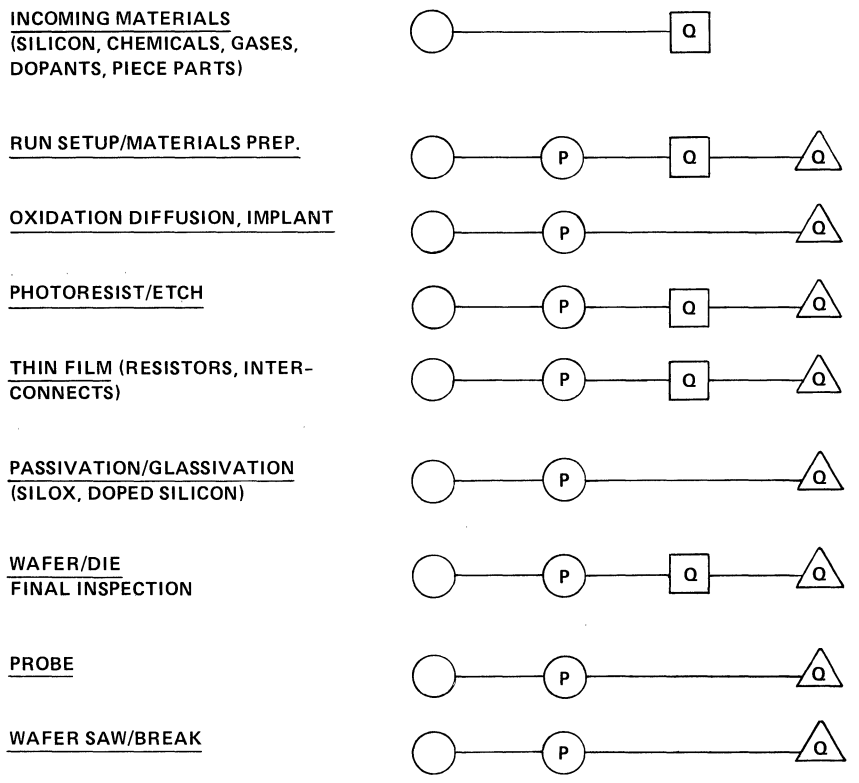
When necessary, fixed gate inspections are permanently employed to assure specified quality levels.

On a regular basis, process audits are performed to verify conformance to operating procedures.

Statistical control charts are maintained on processes and workmanship for all phases of assembly and environmental testing.

PROCESS CONTROL

WAFER FABRICATION - GENERAL PROCESS FLOW



Quality Assurance

The primary responsibility of the Quality Assurance Department is to assure that all delivered products meet the rigid standard of reliability and quality of Harris Semiconductor Products Group. The Quality Assurance department is responsible for process control and product quality from product test to shipment. Random sampling of products at specified points and intervals is used to ensure quality. This includes performance and analysis of sample electrical testing (Group A) and environmental and life testing (Groups B, C and D). In addition, mechanical and visual inspections specified by the Quality Assurance Test Plans, as well as customer and military specifications are performed. The random selection and distribution of samples, the routing of devices through specified testing and adherence to inspection programs are controlled and implemented by Quality Assurance.

All packaged microcircuits are marked by a code indicating the date the lot was sealed. This code provides product traceability and meets customer date coding requirements. Traceability is maintained through lot acceptance, testing and shipment to the customer.

Reliability

The primary responsibility of the Reliability Department is to assure that high and consistent reliability prevails among product produced. The Reliability Department establishes, defines and maintains evaluation programs to determine both product and process reliability, to monitor failure rates and to maintain them within specified limits.

The Reliability Department assists Research and Development and Product Engineering as each new product type is designed, developed, and transferred to manufacturing. Formal and progressive concept, design, and layout reviews are held at scheduled dates during product development.

Throughout the process, reliability based ground rules are invoked to ensure that guidelines for a reliable product are met.

During product development, the Reliability Department defines critical processes requiring stand-alone new technology qualification. Formal transfer of new products from preproduction to manufacturing cannot be authorized until all Quality Control procedures are written, critical processes defined and evaluated, and preliminary product qualifications performed by Reliability. This is required as an essential input to each new product internal specification.

Product reliability standards are established by the evaluation of all products through life tests, stress tests, and process capability studies. Comparisons of test results with general industry performance, requirements of the marketplace and product concept goals form the baseline for product reliability.

The evaluation of new products and the resultant reliability estimates begin in the new product development cycle. All products are evaluated for process compatibility in the initial design stages. Test pattern drop-ins, expanded contact devices and actual devices are produced and evaluated through a series of accelerated stress tests. Results for known processes and accepted standards are compared to specific data for the new product.

In the Failure Analysis Laboratory, failures are analyzed and identified failure modes are utilized to precipitate corrective action.

All products are subjected to elevated temperature operation life tests. Based on the review of these results with appropriate engineering groups, recommendations are made to:

a. take corrective action in design, processing or screening, verify that the implemented corrective action has solved the problem;

b. authorize the transfer of product to Manufacturing.

The completion of new product development and the initiation of volume production does not take place until the Reliability Department has granted full qualification. This is done only on the successful completion of life test of devices from a standard production flow. This results in the identification of critical screens and process controls to ensure consistent high product performance capable of meeting the specified reliability objectives.

It is the responsibility of the Reliability Department to initiate continuing evaluations of reliability (add-on) during the volume production phase. These tests are performed to verify the conclusions reached during product development, to provide additional reliability data and to recommend process improvements to further improve product reliability.

RELIABILITY PROCEDURES

Harris Semiconductor Products Group employs a comprehensive approach to reliability evaluation to ensure that reliability is designed and built into all products. This approach is referred to as the Reliability Evaluation Procedures and outlines the basic guidelines for evaluation of the total inherent reliability capability of all products types. The Reliability Evaluation Procedures are applied as an overlay during the early product development phase, subsequent prove-in via preproduction and final maturity in the manufacturing of all new product types. They also provide guidelines for evaluation of new process technologies deployed in all applicable products. The Reliability Evaluation Procedures also encompass a package qualification procedure, and the "Add-on" program which is a quarterly reliability monitor of all process groups. These documents are available upon request. The following test matrix (Table 1) outlines the minimum requirements necessary for product qualification.

TABLE I. TEST MATRIX

	DESIGN PACKAGE PROCESS		NEW NEW NEW	NEW NEW EST.	NEW EXIST NEW	NEW EXIST EST.	EXIST NEW NEW	EXIST NEW EST.	EXIST EXIST NEW	EXIST EXIST EST.
Abuse Tests	20 Units		X	X	X	X	X		X	X
Max. Ratings	20 Units	No failures	X		X	X	X		X	X
85/85 or Autoclave	50 Units	No failures	X	X	X		X	X	X	
Constr. Analysis	5 Units	No failures	X	X	X	X	X	X	X	X
Centrifuge	50 Units	No failures	X	X			X	X		
Elec. Characteristics	20 Units	No failures	X	X	X	X	X		X	X
ESD Immunity	20 Units	No failures	X	X	X	X	X		X	X
Figure Test	20 Units	No failures	X	X	X	X	X		X	
HTOL Sample Groups			200 (min)	200 (min)	200 (min)	200 (min)	200 (min)	200 (min)	200 (min)	200 (min)
Latch-up	20 Units	No failures	X	X	X	X	X			
Lead Integrity	20 Units	No failures	X	X			X	X	X	X
Mech. Characteristics	20 Units	No failures	X	X			X	X		
Mechanical Shock	50 Units	No failures	X	X			X	X		
Moisture Resist	50 Units	No failures	X	X			X	X		
$\theta ja/\theta jc$	20 Units		X	X			X	X		
Solvent Resistance	4 Units	No failures	X	X			X	X		
Solderability	20 Units	No failures	X	X			X	X		
Temperature Cycling	50 Units	No failures	X	X			X	X		
Thermal Shock	50 Units	No failures	X	X			X	X		
Vibration	50 Units	No failures	X	X			X	X		

The Harris bipolar product line has had a continual evolution of new and enhanced processes based on junction isolation (JI) technology. From the gold doped process that produced the industry's first bipolar PROM (the HPROM-0512), to the current shallow diffused, dual-level metal JI process which utilized advanced ground rules, there has been an on-going effort to increase performance, density and reliability. Table II is a summary of recent reliability data taken on the various bipolar processes. Table III lists the activation energies of the most common defects associated with bipolar products. Table IV gives a breakdown of field returns by failure mechanism.

At Harris, accelerated life tests are utilized to estimate the field failure rate of our product. A typical life test consists of 200 devices tested at +125°C to +150°C ambient, dynamic or static operation, 5.5V to 6.5V, for 1000 hours. All failures are carefully analyzed to determine the failure mechanism and associated activation energy (E_A) utilizing the Arrehnius equation derating factors back to +55°C ambient, 5.5 volts of operation are determined.

$$\text{Derating factor} = \text{D. F.} = e^{-\left(\frac{E_A}{K}\right)\left(\frac{1}{T_2} - \frac{1}{T_1}\right)}$$ where E_A = Activation Energy, K = Boltzman's Constant, T_2 = Life Test Junction Temp., T_1 = Junction Temp. at +55°C Ambient

Projected field failure rates are calculated at 60% and 95% confidence levels. This means that either 60% or 95% of the product will meet or exceed the reliability demonstrated in the test. We also ensure that the failure rate is decreasing with time to prevent any wear-out mechanism from reaching our customers.

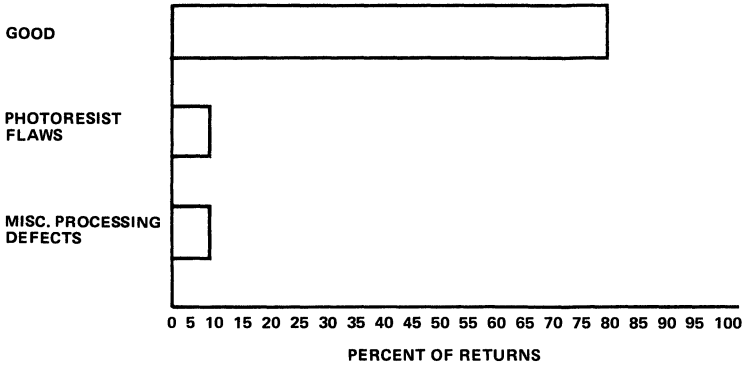
TABLE II. SUMMARY OF BIPOLAR RELIABILITY DATA

PROCESS TYPE	NO. OF DEVICES	DEVICE HOURS (+125°C)	NO. OF FAILURES	E_A (eV)	FAILURE RATE (%/K HOURS) T_A = 55°C		
					OBSERVED	60% CONFIDENCE	95% CONFIDENCE
PROM							
Gold Doped Junction Isolation	616	616,000	2	0.7	0.0078	0.0115	0.234
Junction Isolation, Schottky Diode, Deep Diffused, Single Level Metal	2,740	2,740,000	2 2	0.7 0.8	0.0037	0.005	0.0012
Junction Isolated, Schottky Diode, Shallow Diffused, Double Level Metal	2,785	11,242,220	5 2 5	0.5 0.7 0.8	0.0051	0.0064	0.0113
Junction Isolated, Schottky Diode, Shallow Diffused, Double Level Metal, Adv. Ground Rules	546	16,178,780	2 1 5	0.5 0.6 0.8	0.0177	0.0261	0.0544
PROGRAMMABLE LOGIC							
Junction Isolated, Shallow Diffused, Double Level Metal	273	1,987,509	3	0.5	0.0120	0.0170	0.0320
POWER STROBE & DIODE MATRICES							
Dielectric Isolation	150	105,745	0		N/A	0.0061	0.020

TABLE III. BIPOLAR PRODUCTS - ACTIVATION ENERGY

FAILURE MECHANISM	ACTIVATION ENERGY E_A
Oxide Defects	0.5eV
Defective Apertures	0.6eV
Photoresist Flaws	0.7eV
Assembly Defects	0.8eV

TABLE IV. FIELD RETURNS BY FAILURE MECHANISM



NOTE: Returned units are less than 1% of the total shipped.

AQL/AOQ Terminology

AQL SAMPLING PLAN: An AQL (Acceptable Quality Level) Sampling Plan is determined by knowing the lot size and specifying the AQL (expressed as percent defective and typically considered as an acceptable process average). A unique sample size and accept number is determined by these facts. Given a lot size and sampling to an AQL of 0.4%, for example, means that over time, lots 0.4% defective will be accepted "95%" of the time. (The quotes denote that this number varies around 95%). Relating this to confidence levels means that a producer has a 95% confidence level that lots 0.4% defective or better will be accepted.

Note that sampling to a 0.4% AQL does not guarantee any percent defective in a lot. A 5,000 piece lot sampled to a 0.4% AQL (ss = 200, accept # = 2) could contain 1,000 rejects (percent defective = 20) and still theoretically pass the sampling. An AQL sampling does not guarantee any specified lot acceptance rate - this is totally determined by the lot quality.

PRODUCER'S RISK (α): This is the probability that a lot with an acceptable quality level (AQL) will be rejected. In our above example, 0.4% defective material has a "95%" probability of acceptance; therefore, a "5%" probability of rejection. The "5%" is the producer's risk.

LTPD SAMPLING PLAN: An LTPD (Lot Tolerance Percent Defective) Sampling Plan assumes a statistically large lot size and is determined by specifying an LTPD (expressed as percent defective), and and accept number. A given LTPD requires an increasing sample size as the accept number increases. The LTPD, for example 2.0%, means that a lot sampled to this LTPD (specify accept number to get unique sample size), will be accepted only 10% of the time if the lot quality is 2.0% defective. The LTPD is sometimes referred to as the unacceptable quality level. Once again, sampling to a specified LTPD does not quarantee any specified lot acceptance rate - this is determined by the lot quality.

CONSUMER'S RISK (β): This is the probability that a lot with an unacceptable quality level (LTPD) would be accepted. In our above example, the consumer's risk is 10% because a product 2% defective (considered bad) has a 10% chance of passing the LTPD sampling plan.

AQL & LTPD are obviously related. A specified sampling plan (sample size & accept #) defines an AQL & LTPD if we set these values at 95% and 10% probability of acceptance. You cannot identify an AQL sampling plan & force it through a specified LTPD. The AQL sampling plan mathematically gives an LTPD.

AOQ: AOQ (Average Outgoing Quality) is expressed as a percent, or more commonly, parts per million (ppm, 1% = 10,000 ppm).

AOQ calculations assume that rejected lots are 100% screened with defective units replaced by good units; thus improving AOQ.

Because of the above procedure, the lowest AOQ is obtained when lots are perfect or totally defective (because of 100% screening and replacing bad with good). An AOQ curve lists incoming quality on the X-axis and AOQ on the Y-axis. The curve starts at 0% AOQ for 0% incoming quality and ends at 0% AOQ for 100% defective incoming quality.

The statistical calculations for AOQ involve lot size, sample size and the percent defective incoming. This will yield an AOQ point on the above mentioned curve. It should, therefore, be noted that by specifying sampling plan and knowing the incoming percent defective, an AOQ is determined.

However, because of some slight deviations to the rescreening procedure and to simplify calculations, many companies have elected to determine AOQ merely by investigating lot history. The total percent defective in all samples is multiplied by the percent of lots accepted.

AOQL: AOQL (Average Outgoing Quality Limit) is the maximum (worse or limit) of the AOQ's determined from our sampling plan. It is the maximum point on our AOQ curve. Sampling plans can be based on AOQL. Sampling to a 0.8% AOQL means that the AOQ will be no greater than 0.8% defective.

Specifying the AQL sampling plan or an LTPD sampling plan (sample size and accept #) will mathematically yield the AOQL.

Fusing Mechanism of Nickel-Chromium Thin Film Links

Nickel-chromium fusible link programmable read-only memories, (PROMs) have been developed and utilized since their inception during the early 1970's[1] . The physical mechanism of fusing these links has been generally described as melting[2], but only with the advent of a successful transmission electron microscopy technique[3], has detailed information on the structure of the programmed fuse gap become available. These observations, coupled with electrical and thermodynamic characterization of the fusing event, have led to a clearer understanding of this phenomenon with concurrent definition of programming conditions for reliable operation of programmed PROMs.

SOME RELEVANT GENERAL PROPERTIES OF NICKEL-CHROMIUM

Fundamental to the mechanism of NiCr fusing are those physical properties that make it an excellent resistor material from processing, design and applications perspective. It is no accident of history that NiCr is widely used for resistors on solid state devices.

To begin with, NiCr is a resistive material comprised of two transition metals-nickel and chromium. In transition metals, the outer electron shells contain only one or two electrons and some of the conduction electrons must come from inner shells. The inner shell conduction electrons are shielded by the outer shell resulting in a high scattering and trapping site density. Thus, transition metals are inherently less conductive than normal metals[4]. In the case of NiCr, an alloy effect[4] occurs to further enhance electron scattering. The result is that the resistance of the alloy is much higher than the arithmetic average of its two components[5] as illustrated in Figure 1**.

The resistivity of NiCr makes it well suited for small geometry thin film resistors that are size compatible with high density fuse design requirements. Due to its high resistivity the thickness of NiCr that is necessary to achieve a typical fuse resistance of 200 ohms is an advantageous property for a fuse, as will be described later. There is also the elimination of step coverage problems where the metallization (aluminum) contacts the NiCr.

A consequence of the extensive electron scattering in NiCr is a short mean free path of the conduction electrons. For example, the mean free path in gold is 380Å[6] compared to an estimated 40Å for NiCr. As a consequence, films greater than 100Å thick have bulk resistivity properties (i.e., surface effects are not dominant). As Figure 2 shows, surface scattering effects which reduce conduction are absent by the time the resistor film is greater than 100Å[7] in thickness. The practical ramification of this property is reproducibility in the fabrication process. Because there is no dependence on surface effects to achieve the desired sheet resistivity, thin film resistors may be produced with excellent tolerance and stability[8].

The short mean free path is also relevant to describing the fusing mechanism, discussed in the Mass Transport Models section.

NiCr is a material that forms a self-limiting oxide skin. That is, the oxide of NiCr is known to be a coherent spinel[9,10], see Figure 3. It is postulated that in the course of processing NiCr resistors, this thin spinel sheath will form around the NiCr to a thickness of Δ 20Å. This sheath serves to stabilize the resistors and is partly responsible for the excellent thermal stability of NiCr 11. This spinel may also be a factor in the fusing phenomenon.

MICROSTRUCTURE OF A PROGRAMMED NICKEL-CHROMIUM FUSE

The technique of using transmission electron microscopy (TEM) to examine programmed fuse gaps was developed by Dr. Kinsey Jones at C.S. Draper Labs[3,12]. It is the only technique which mutually satisfies the requirements of sufficient resolution to analyze the gap and not destroy in sample preparation the structure to be analyzed. It is this latter point that has severely limited the utility of the scanning electron microscope (SEM) in endeavors to analyze programmed NiCr fuses. In depassivating devices, necessary with the SEM, microstructural details of the fuse gap are destroyed. Many interpretations of the fusing phenomenon based on SEM results have been erroneous or misleading because what was seen was an artifact of sample preparation.

Figure 4 illustrates schematically the utilization of transmission electron microscopy for fuse gap analysis. Of course, besides direct structure observation, composition of various phases may be ascertained by electron probing.

The microstructure of a programmed fuse gap in a PROM circuit via TEM is shown in Figure 5. The relevance of those programming conditions will be discussed further in following sections, but Figure 5 is representative of the gap created in a NiCr fuse under programming power conditions specified[13] for PROMs.

The TEM micro photograph indicates the elemental distribution found by microprobing. The following observations are made:

a. The visual appearance indicates that the neck of the fuse was in the molten state during programming.

b. Mass transport of the nickel and chromium from the gap region has occurred.

c. There is asymmetry to the melted NiCr distribution. That is, there is more densified Nickel-chromium on what was the cathode (negative) side of the fuse which suggests the molten NiCr moved in a direction opposite to electron flow during programming.

d. The gray phase (region C) of the gap which comprises the insulative separation of the two sides of the fuse is devoid of nickel and composed of oxides of silicon and chromium[14]. The typical separation is 0.6-1.0 microns. The resistance across the gap is > 10 megohms and it will not break down, electrically or structurally to voltages in excess of 100 volts.

e. The white spots, dark spots and filaments are described by the fluid dynamics of a disintegrating liquid sheet[12]. Briefly, that model describes how minute discontinuities in a liquid sheet perturbate into larger holes, and finally into droplets and filaments because of surface tension effects. The structure looks similar to a "frozen splash".

MASS TRANSPORT MODELS

In the previous section, it has been demonstrated that programmed NiCr fuses melt and that mass transport takes place. But what is the mechanism, the driving force for mass transport ? Table 1 lists the possibilities.

Table 1

(1) Electromigration (Huntington & Grone[15]): Mass flux occurs under the influence of high current flow because electron collisions with atoms of the conducting medium provide a net motion vector in the direction of electron flow.

(2) Thermal gradient (Soret[16]): In the presence of a thermal differential, material will diffuse from the high temperature to the low temperature region.

(3) Concentration gradient (Fick[17]): In an imbalanced distribution of concentration, mass will diffuse from regions of higher concentration to lower concentration.

(4) Field enhanced ionic mobility (Eyring and Jost[18]): Molten metals will ionize, lose electrons and become cations. In the presence of an electric field, they will be driven towards the cathode.

Considering each possible mechanism in turn:

(1) Electromigration — On the surface, this seems a most logical explanation for programming. It is known that the current densities in a fuse neck at programming are very high ($\sim 5 \times 10^7$ amps/cm^2), and it could be postulated that this electron flux sweeps the nickel and chromium from the gap. But empirical data and theoretical considerations show this not to be the case.

a. TEM of the fuse gap indicates the molten NiCr has moved in a direction opposite to electron flow.

b. Theoretical calculations of the kinetic energy of conduction electrons in NiCr demonstrate that because the mean free path is short and the lattice binding energy is high (transition metals typically have high melting points), the electrons have insufficient energy to impart the mobility to the nickel and chromium atoms necessary for electromigration in the direction of electron flow.

However, general treatments of electromigration theory[15, 24] identify two forces acting on atoms of the conducting medium. One is the aforementioned electron momentum ("electron wind") in the direction of electron flow. The other is the electrostatic force from the applied electric field that causes ions of the conducting material to move opposite to the direction of electron flow. See mechanism (4).

Obviously, the joule heating that leads to melting the fuse is coming from electron interaction with the NiCr film. There is no incongruity with the fact that this is not leading to electromigration such as observed in aluminum. Because the mean free path is short, the energy exchanged per collision is small. But because electron scattering is a dominant factor in resistive materials, the frequency of collisions is high. Thus, thermal energy (lattice vibration) is added to the metal atoms. The electron collisions increase the amplitude of the atomic vibration and increase the temperature. This is why NiCr is an efficient material for converting electrical energy into thermal energy (toaster effect).

(2) Thermal Gradient — From an analysis of heat flow in a fuse, it has been shown (see the Transient Heat Flow Analysis section), Figure 6, that the temperature profile across a fuse neck is flat. The gradient occurs at the neck-to-fuse body interface. But the programmed gap occurs in a region where there is no temperature gradient. Further, this model would predict a symmetric distribution of mass, post-programming which is not observed. Temperature gradient does not cause the mass transport.

(3) Concentration Gradient — It has been shown in unprogrammed fuses that no concentration gradient exists. Laterally in the fuse film this is borne out by the TEM/probe analysis. That is, no nickel or chromium concentration variations are observed across an unprogrammed fuse. Vertically (distribution of nickel, chromium through a cross section of the resistor) it has been shown[20], from sputter etching Auger analysis that the nickel and chromium are distributed uniformly through the film (no concentration layering effects).

Because there is no concentration gradient initially, this is ruled out as a starting mechanism for fusing.

(4) Field Enhanced Ionic Mobility — Eyring and Jost[18] have observed that liquids have a fixed ratio between their energy as a liquid and the energy required for vaporization; see Figure 7. Stated simply, the principal is, the more cohesive the liquid, the more energy is required to transform it to the gaseous phase, and the ratio is a constant. This rule held for all types of liquids (gases, solvents, organics, etc.) except metals. But by accounting for ionization of molten metals and the subsequent reduction in atomic radii, see Table II, they found that metals obeyed the liquid:gas constant energy ratio. In other words, molten metals are ionic.

It follows then that these positive ions (they have given up outer shell electrons) will move in the presence of an electric field (from the programming pulse) toward the negative terminal, opposite to the direction of electron flow. This is consistent with the TEM observations and with some investigations of electromigration. For example, Wever[25] observed in copper above 950°C, that mass flux was toward the cathode.

In summary, NiCr fuses program as follows: **A programming pulse of sufficient power is applied across the fuse. Power dissipation in the fuse neck heats this region into the molten state and the nickel and chromium atoms become ionized. They move toward the negative side of the fuse and the liquid film begins to disintegrate. The film becomes electrically discontinuous and rapidly returns to the solid state, the final structure resembling a frozen splash described by fluid dynamics. The fuse gap consists of insulative oxides of silicon and chrome, with resistance >10 megohms.**

Footnote: Arguments have also been advanced that oxidation is the mechanism of fusing [19]. If this were so, the probe data, which discerns elemental presence, would not show nickel and chromium depletion in the gap region, i. e., mass transport, per se, would not have occurred. Because the TEM data clearly indicates mass transport, attention is focused here on identifying the driving force for that mass transport.

TRANSIENT HEAT FLOW ANALYSIS

The previous discussions dealt with the fusing event postfacto, describing the microscopic material structure created by programming. The dynamics of the fusing event can also be characterized. By modeling the fuse structure and its environment in terms of classical heat flow, the connection between electrical and material behavior of fuses can be established.

A computer thermal analysis program called "THEROS"[21] was used to calculate the dynamic temperature effects in a PROM-fuse structure as a function of applied power density.

This computer program can thermally model a multicomponent structure and calculate the temperature as a function of time for given power dissipation conditions. The program takes into account temperature dependent thermal properties of the various materials and models a 2-dimensional multimaterial, multigeometrical structure into a RC circuit network that can be analyzed by sophisticated transient circuit analysis programs. This approach is convenient because the differential equations that describe heat flow problems have the same form as differential equations for RC circuit networks. For example, specific heat is analogous to capacitance, thermal conductivity is analogous to the inverse of resistance, temperature is analogous to voltage and heat flow is analogous to current. By way of the "THEROS" heat flow to electrical analog program, the sophistication available with present circuit analysis programs can be utilized to solve complex heat flow problems without consuming hours of computer time and without the errors prevalent in more simplified calculations. For the heat flow model to be truly representative of the actual device, the immediate environment of the fuse must be completely accounted for. For example, the passivating oxide layer on top of the fuse will affect the heat flow and the subsequent structure of the programmed fuse. Programming a fuse without the passivating oxide[22] will result in a different structure than occurs in an actual PROM circuit.

The term "power density" is defined as the amount of power that is dissipated in the fuse neck region divided by the area of the fuse neck ($mW/\mu 2$), see Figure 8. The concept of defining power density as power per unit surface area is applicable to thin film heat flow problems where the heat is dissipated through a surface. (The concept is analogous to defining current density as current per cross sectional area). Figure 9 shows a plot of the computer results giving the temperature in the center of the NiCr fuse that would be achieved if a constant power were applied for a time t. The curves show that the fuse can easily reach the melt temperature of NiCr 23 within 10 microseconds for power densities > $5mW/\mu 2$.

Figure 10 is a plot of the intercept of the time to reach the melt temperature (1450°C) vs. the power density. This theoretical prediction of the power density versus time to reach the melt temperatures compares well with experimental data on time to fuse. The data in Figure 10 was taken from test vehicle fuses, processed identically to circuit fuses, but free of interfacing circuitry. This allowed precise characterization of fuse-pulse interactions. The data matches for long fusing time but deviates for short fusing time. This difference can be accounted for by considering the definition of "time to fuse". The experimental data points represent total time to fuse which includes rise time of the programming pulse, time for the fuse to heat to sufficient temperature, and time of the actual fusing event. For example, Figure 11 shows a typical current trace for a fuse programmed under constant voltage conditions. The trace shows a fixed rise time, t_r (about 100 nanoseconds for this data), a response time, t_m, for the NiCr to reach the melt temperature, and a time for the fuse neck to enter the melt phase and program, t_f. Plotting the time defined as t_m shows excellent correlation with the theoretical prediction of the time to reach melt temperature. The difference between the theoretical prediction to reach melt and the actual time to fuse agrees with the measured values of $t_r + t_f$. Figure 10, therefore, shows that fusing follows a heat flow dependence that requires the NiCr to achieve melt. Proper PROM design necessitates taking into account thermal factors that affect the heat flow conditions in the neighborhood of the fuse. Concentrating power by optimum fuse geometry and ensuring sufficient power to the fuse will achieve fast, uniform programming.

For power density conditions below the programming threshold level, the fuse temperature as a function of power density into a fuse for a sustained pulse ($t \longrightarrow \infty$) is shown in Figure 12. There is good agreement of the computer model with experimental data. The experimental data was derived from measuring the fuse resistance (at reduced current, avoiding I^2R heating) of an externally heated fuse and comparing that to the power necessary to generate the same resistance at an ambient temperature of 25°C. The agreement between model and experimental data is a further indication that the heat flow analysis is correctly projecting the temperature in the fuse.

It is also relevant to note the low power density on a fuse in the read mode, 10% of the threshold power density to melt the NiCr fuse. Test vehicle fuses were stressed at $1.2mW/\mu^2$ which is 60% of the fusing threshold level and equivalent to a fuse temperature of 800°C. No failure occurred after 4000 hours of continuous operation. Thus, the designed power density for PROM operation in the read mode avoids the occurrence of unprogrammed fuses becoming open.

In summary, the power density versus time to program curve, Figure 10, agrees with the heat flow model and implies a single mechanism, heat transfer for both fast and slow fusing. High power fusing (fast blow) approaches adiabatic heating conditions, and therefore gives a large melted region and a wide gap due to the large electric field present during programming. Restricted power programming (slow blow) allows much of the heat to diffuse away, taking longer for the fuse to reach the melt temperature and produces a smaller melted region with a narrower gap due to the smaller electric field present.

MARGINALLY PROGRAMMED FUSE

By grossly violating recommended programming procedures for fuses, it is possible to create a marginal fuse gap that may be subject to reverting state ("growback"). This anomaly was induced in a test vehicle fuse by restricting the power input to a value on the $t \longrightarrow \infty$ asymptote ($\sim 2mW/\mu^2$) of the power density versus time to fuse curve (Reference previous section, Figure 10). Under these conditions, a fuse was induced to program, become electrically discontinuous, after 5 minutes of sustained power. This effect, programming under an anomalously reduced power, was not found to be reproducible. Many fuses at this power would not program after days.

This deliberately improperly programmed fuse was subsequently subjected to a slowly applied DC voltage ramp under current limited conditions (10MΩ resistor in series). At 12 volts, the fuse resistance dropped to $\sim$ 5000 ohms. The TEM photograph of this fuse is shown in Figure 13. It is obvious from this photograph that the reduced power condition has resulted in a fuse that has marginally programmed. That is, the gap created after programming is very narrow (approximately a few hundred angstroms) and subject to a voltage breakdown effect.

Fuses programmed per the recommended power levels will program rapidly with a wide gap as illustrated in the Mass Transport Models section. These fuses can be subjected to more that 100 volts and will undergo no change in electrical or physical condition.

As indicated in Figure 13, if a restricted amount of power is applied to a fuse, it is possible to create a very narrow gap. Under the presence of high voltage and extreme current limiting, it is then possible to force a voltage breakdown across the gap. It is postulated that this voltage discharge results in the establishment of a low conductivity relink at one or a few points of closest approach in the marginally blown gap. This specific structure could not be confirmed with the TEM study because even the TEM did not have resolution to examine microstructure at < 300 angstroms.

This mechanism of marginal programming is precluded from occurring in an actual PROM circuit because the programming specification; specifically, the power and pulse widths have been established to only generate well blown, wide gap fuses. That is, if the power actually reaching a fuse is lower than that required to blow the fuse properly, the fuse will not program in the time allotted for the programming pulse. The device, therefore, becomes a programming reject (won't program) and is scrapped.

In summary, the observation that a NiCr fuse can be marginally programmed has no connection with the reliability of the PROM circuit. Recall, to generate this anomaly, a power density four times less than the designed value and a program time $\sim 10^8$ times longer than the maximum specified programming time was required. Further, a voltage $\sim$10 times higher than the maximum that would be seen in an actual PROM, (with current limiting) was required to cause the relink.

Obviously, these observations and conclusions are based on NiCr fuses, PROM design, and control procedures as deployed by Harris. Contentions by others that a specific fuse material, NiCr or something else, is more or less reliable must be interpreted in perspective of the manufacturer's technology and not necessarily be construed as being generally representative.

SUMMARY

(1) Conduction electrons in NiCr have a short mean-free path. This maximizes I^2R heating and precludes electromigration in the direction of electron flow as a fusing mechanism.

(2) Transmission electron microscopy is the only effective analytical tool to characterize the programmed fuse gap structure.

(3) NiCr fuses program by molten metal (nickel, chrome), ions moving in the presence of an electric field. The final structure resembles a frozen splash and is described by fluid dynamics.

(4) Thermal analysis coupled with empirical programmed fuse data indicate a threshold power density for fusing. If this power density is exceeded, which can be assured if the programming time utilized is as specified, the fuse gap will be wide and reliable. If this power density threshold is only matched, it is possible to create a marginal fuse.

(5) Life test results indicate programmed PROM reliability is equivalent to devices of the same complexity that do not utilize fusible links.

(NOTE: This paper originally appeared in the Proceedings of the IEEE International Reliability Physics Symposium, 1976. It has since been revised to reflect current Harris circuit geometries and other details. The original intent of the paper is unchanged.)

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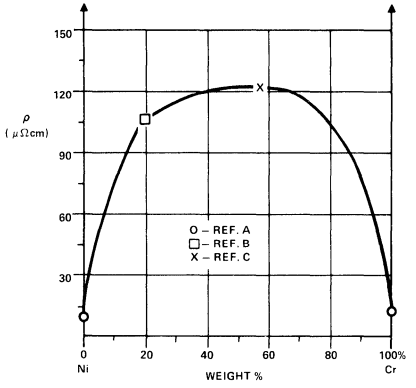
CONDUCTION PROPERTIES OF NiCr

- NICKEL AND CHROMIUM ARE TRANSITION METALS.
- INNER SHELL ELECTRONS CONDUCT, OUTER SHELL SHIELDS. HIGHER RESISTANCE.
- ALLOY EFFECT ENHANCES SHIELDING/RESISTIVITY.

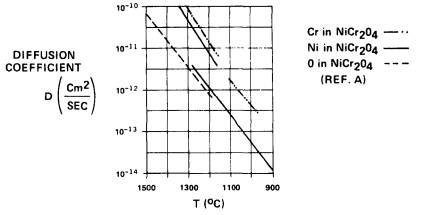


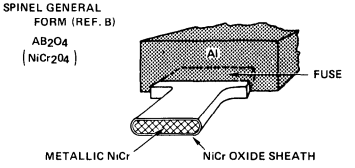
A – Handbook of Chemistry and Physics.
B – Thin Film Technology, R. W. Berry, et. al.
C – Japanese Metal Material Handbook, Y. Yamamoto, et al.

Figure 1

OXIDATION OF NiCr

- NiCr FORMS SELF LIMITING SKIN OXIDE
- SPINEL THICKNESS ≃ 20 Å
- PROMOTES RESISTOR STABILITY



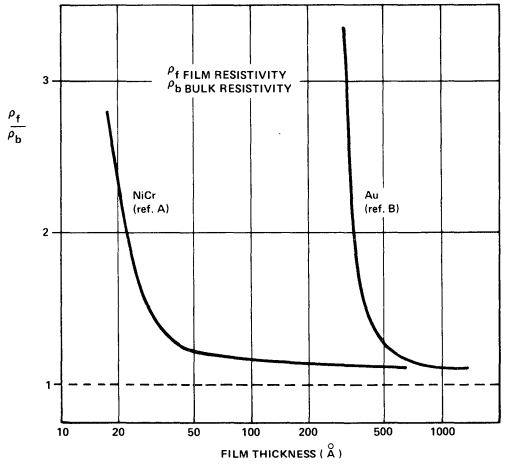


Ref. A – "Mass Transport in Oxides," NBS Publ. 296, (1968).
Ref. B – A. F. Wells, "Structural Inorganic Chemistry", Oxford Press (1950).

Figure 3

FILM VS. BULK PROPERTIES

- SHORT MEAN FREE PATH LENGTH OF ELECTRONS
- BULK RESISTIVITY IN THIN FILM
- GOOD FILM REPRODUCIBILITY



A – M. Nagata, et. al., Proc. Elec. Comp. Conf., 1969.
B – K. L. Chopra, Thin Film Phenomena, McGraw–Hill, 1969.

Figure 2

SCANNING TRANSMISSION ELECTRON MICROSCOPY ANALYSIS OF FUSES

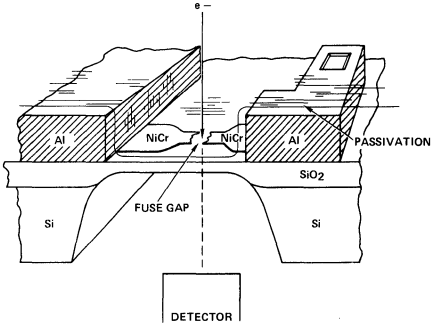
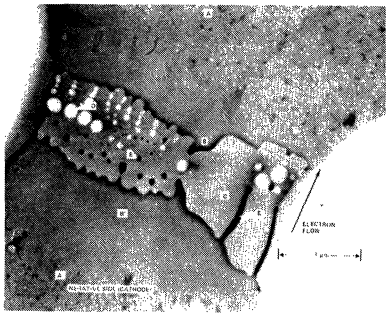


Figure 4

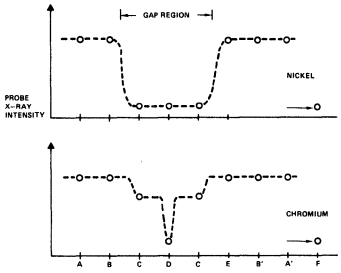
STEM PROGRAMMED FUSE

PROGRAMMING CONDITIONS:
POWER = 150 mW.
TIME TO FUSE = 2 μSEC.



POINT MICROPROBE ANALYSIS

A – NiCr
B – MELTED NiCr
C – SiO_2, CHROMIUM OXIDE
D – SiO_2
E – DENSIFIED NiCr
F – FIELD OXIDE (SiO_2)



NOTE: (A) "FROZEN SPLASH" EFFECT PROGRAMMING HAS MELTED NiCr IN GAP REGION.
(B) MASS TRANSPORT IN GAP.
(C) MASS ASYMMETRY TO NEGATIVE TERMINAL.

Figure 5

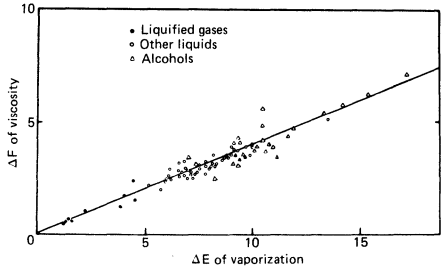


Fig. 11-24. Empirical relation between free energy of activation in liquids, ΔF, and energy of evaporation, ΔE, Rosevaere, Powell and Eyring.

TABLE II

Corrected ratio of energy of vaporization and activation for viscous flow

Metal	Average temp. °C.	ΔE_{vap} kcal.	ΔE_{vis} kcal.	$\frac{\Delta E_{vap}}{\Delta E_{vis}}$	$\frac{\Delta E_{vap}}{\Delta E_{vis}}\left(\frac{r_{ion}}{r_{atom}}\right)^3$
Na	500	23.4	1.45	16.1	2.52
K	480	19.0	1.13	16.7	3.41
Ag	1400	60.7	4.82	12.5	3.79
Zn	850	26.5	3.09	8.6	2.10
Cd	750	22.5	1.65	13.5	3.96
Ga	800	34.1	1.13	30.3	2.53
Pb	700	42.6	2.80	15.9	4.97
Hg	250	13.6	0.65	20.8	2.37
Hg	600	12.3	0.55	22.2	3.54
Sn	600	15.3	1.44	10.6	4.07
Sn	1000	14.5	1.70	8.6	3.30

From "Diffusion in Solids, Liquids, Gases", W. Jost.

Figure 7

TEMPERATURE PROFILE IN FUSE NECK FROM HEAT FLOW MODEL

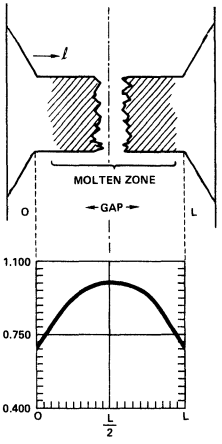
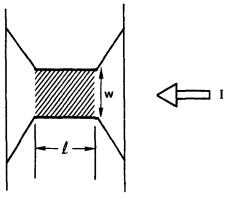


Figure 6

POWER DENSITY IN FUSE NECK REGION



$$\text{POWER DENSITY} = \frac{I^2(\rho_s \ell/w)}{(\ell \cdot w)}$$

$\rho_s \ell/w$ = RESISTANCE OF THE FUSE NECK (OHMS)

ρ_s = SHEET RESISTIVITY OF NICHROME (OHMS/SQ)

$\ell \cdot w$ = AREA OF FUSE NECK (MIL.^{2})

ℓ = LENGTH OF FUSE NECK

w = WIDTH OF FUSE NECK

I = PROGRAMMING CURRENT ($I = V_F/R_F$)

Figure 8

DYNAMIC HEATING OF NiCr FUSE VS. POWER DENSITY

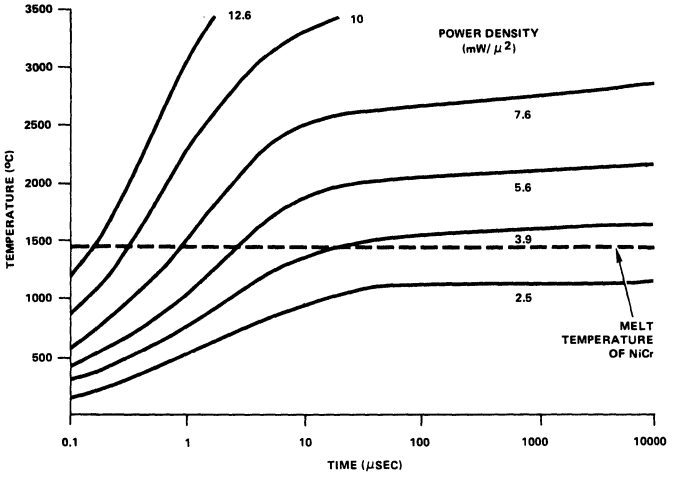


Figure 9

POWER DENSITY VS. TIME TO FUSE

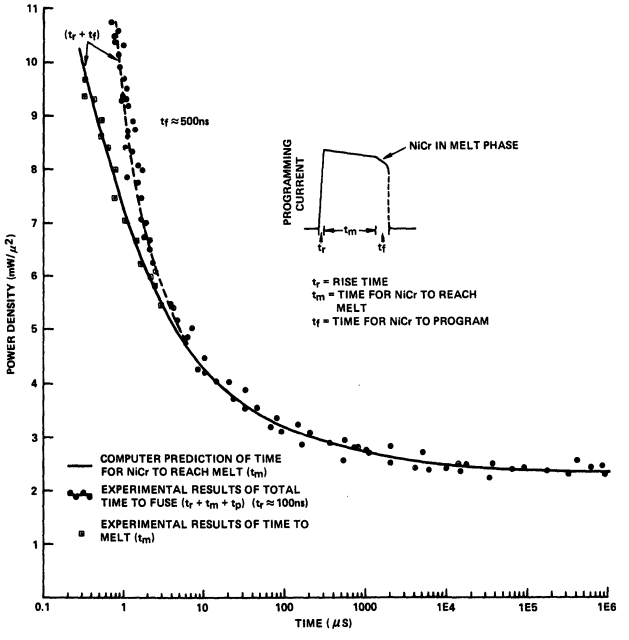
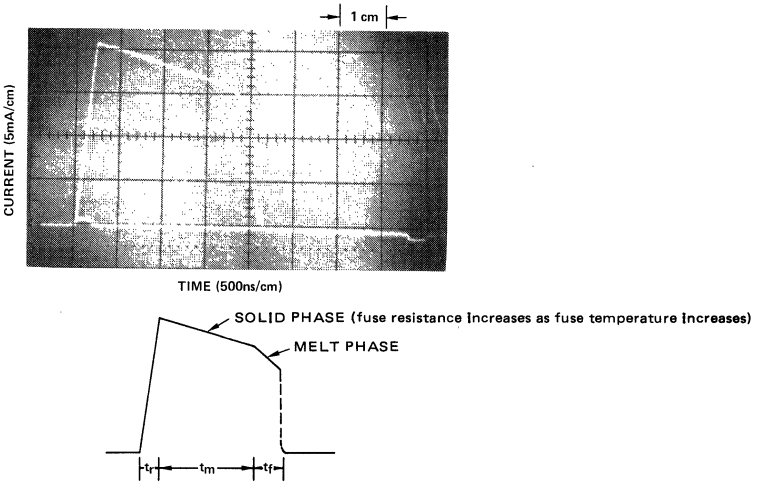


Figure 10

PROGRAMMING PULSE CHARACTERISTICS



t_r = RISE TIME OF PROGRAMMING PULSE

t_m = TIME FOR NiCr TO REACH MELT

t_f = TIME OF THE FUSING EVENT (IONIC MASS TRANSPORT)

Figure 11

MAXIMUM FUSE TEMPERATURE VS. POWER DENSITY

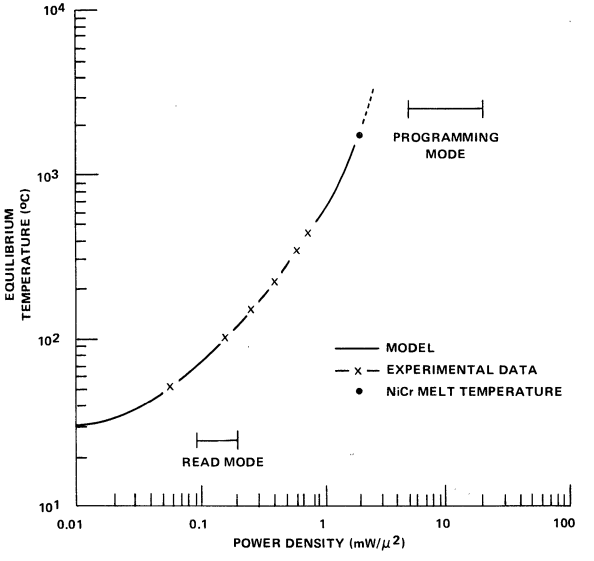
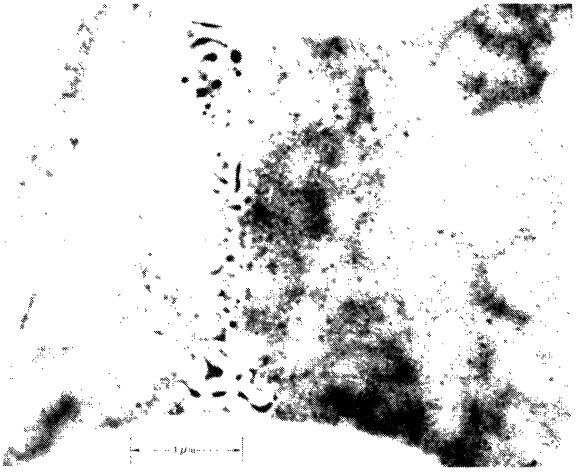


Figure 12

MARGINALLY PROGRAMMED TEST VEHICLE FUSE

PROGRAMMING CONDITIONS:
POWER DENSITY = 1.5 WATTS/MIL^2
TIME TO FUSE = 300 SEC.



FORCED RELINK OF MARGINALLY PROGRAMMED TEST FUSE

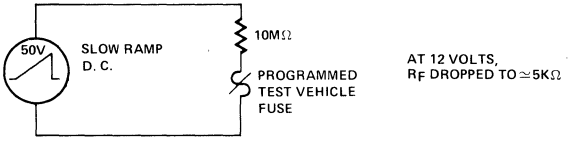


Figure 13

Microscopic Observations of Fuses

Beauty is in the eye of the beholder. When the eye is attached to a microscope, beauty can take strange forms. Nowhere is this more evident than when the realm of blown fuses in PROMs is entered. This paper will "shed some light" on the misinformation which has been generated regarding the nature of NiCr fuse gaps as viewed by different microscopic techniques.

WHAT YOU SEE OPTICALLY

Using a light microscope to examine fuse structures is a futile exercise because the wavelength of visible light is within an order of magnitude of the total fuse dimensions. The microstructure of the fusing process reaction zone contains formations that are smaller than a wavelength of light. In addition, the overlying passivation acts like an aberrant lens and distorts the image which is visible. The most that can be reliably ascertained regarding the nature of a fuse with optical microscopy is whether the fuse is physically present or absent.

Photo 1* illustrates this physical phenomenon. The photograph is of photoresist after exposure to ultraviolet light and normal developing solutions. The ridges in the vertical portion of the photoresist are produced by the standing wave that is present due to reflection of the U.V. light from the oxidized silicon during resist exposure. As can be seen, the ridge pattern has a wavelength λ of the incident light (λ = 3650nm), the index of refraction of the photoresist is n = 1.58; thus, for visible light on the order of λ= 5000nm, less than ten wavelengths are needed to span the fuse neck region.

WHAT THE SCANNING ELECTRON MICROSCOPE SHOWS

The SEM is a useful analytical tool for many applications. This is amply demonstrated by Photo 1 that showed us the standing wave pattern in photoresist.

The SEM does have limitations in observing fuses, however. For one, it cannot "see" through the passivation layer on top of the fuse. This necessitates the removal of the glassivation and hence, physical and chemical alteration of the fuse gap microstructure. In addition, the results after depassivation are misleading. A SEM of a depassivated typical programmed NiCr fuse is shown in Photo 2. Photo 3 is a typical programmed polysilicon fuse as deployed in the CMOS PROM.

Previous observers have never reached satisfactory explanations for the fusing phenomena based on SEM photographic evidence. The important facts to consider here are that for both fuses, an electrical discontinuity has been achieved through programming. In both cases, the observer is hard pressed to determine how this was achieved, for his eyes tell him that both fuses appear physically connected in various areas. Electrically, we know this is not the case.

This brings us to the crucial observation that the SEM cannot distinguish between electrical conductors and electrical insulators. This is readily confirmed by observing the lack of differentiation afforded in the SEM view of the adjacent aluminum interconnect (an excellent conductor) and the underlying silicon dioxide (an excellent insulator). Since both of the above fuses are electrically discontinuous, some portion of their makeup is insulative, but the Scanning Electron Microscope gives us no clues as to the integrity of the insulator.

*Photos found on pages 7-25 thru 7-27.

TRANSMISSION ELECTRON MICROSCOPY ANALYSIS OF FUSES

A fresh approach in fuse analysis has been developed to view a fuse without disturbing the conditions present at the time of programming. Basically, the technique uses a thinned specimen PROM with the fuses sandwiched between the two normal glass sheets found on the PROM (the passivation above and thermal oxide below) with the underlying silicon substrate etched away as shown in **Photo 4**. Now standard high resolution bright and dark field TEM (Transmission Electron Microscopy) analytical techniques are available.

Photo 4 is a TEM photograph of a typical programmed NiCr fuse. Now we can see which regions of the blown fuse are conductive metal and which are not. The well-defined darkened regions are metallic while the overlying gray, which is all that was seen by SEM, has proven by electron diffraction analysis to be a stable insulating oxide compound with crystalline order that resembles a $NiCr_2O_4$ spinel. The surrounding region of high transmission are characteristic of the undisturbed passivation and underlying thermal SiO_2.

Therefore, Transmission Electron Microscopy has the capability of determining the true chemistry of programmed NiCr fuses.

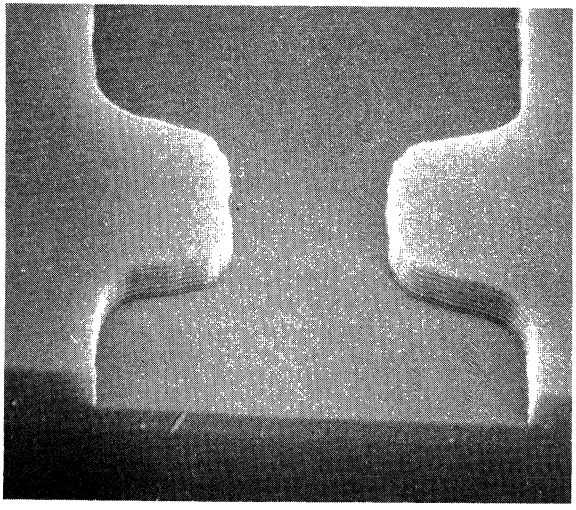


PHOTO 1A

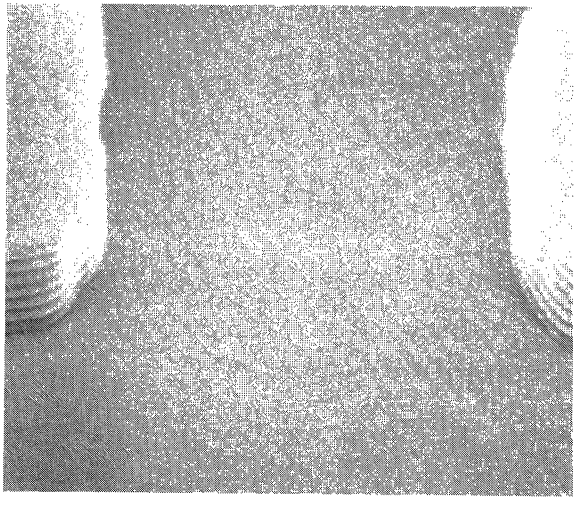


PHOTO 1B

SEM Photographs of Programmed Fuses

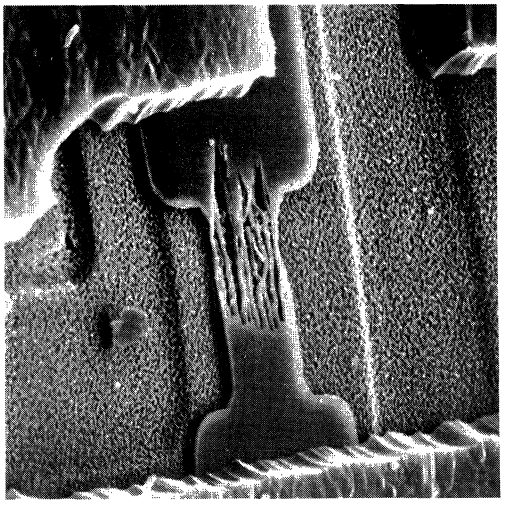


PHOTO 2A

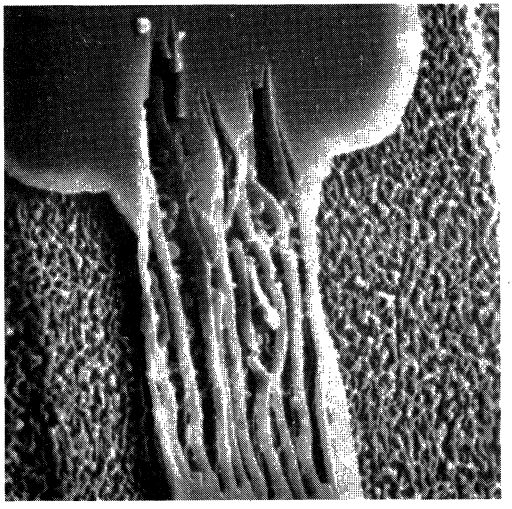


PHOTO 2B

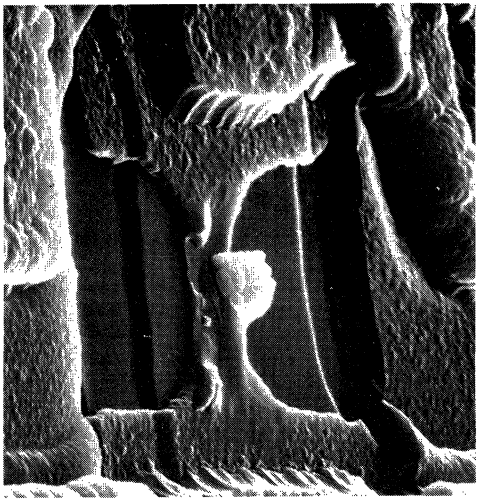


PHOTO 3A

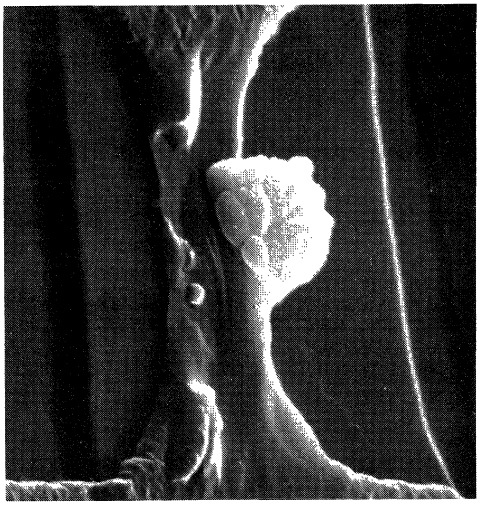


PHOTO 3B

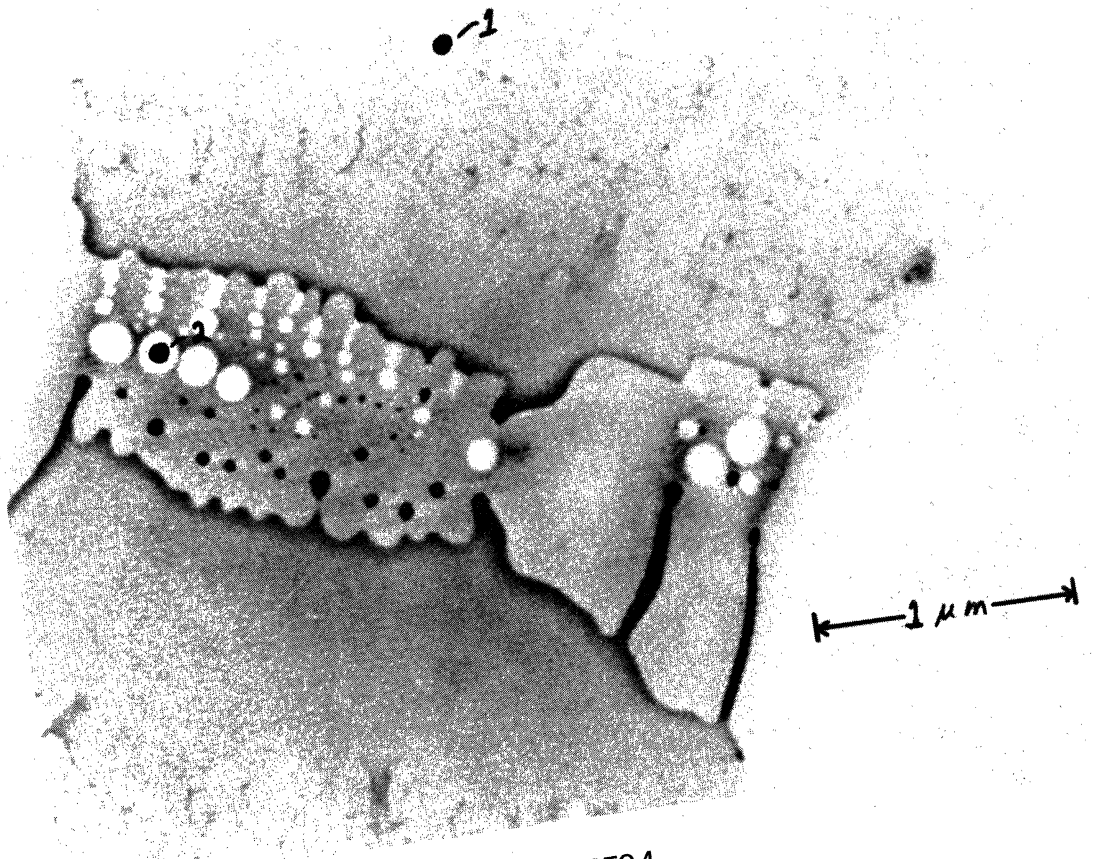


PHOTO 4

Burn-In Circuit Diagrams

MIL-STD-883B, method 1015.2, paragraph 1 states, "The Burn-In test is performed for the purpose of screening or eliminating marginal devices, those with inherent defects, or defects resulting from manufacturing aberrations which cause time and stress dependent failures.". In the absence of Burn-In, these defective devices would be expected to result in infant mortality or early lifetime failures under use conditions. Therefore, it is the intent of this screen to stress microcircuits at or above maximum rated operating conditions or to apply equivalent screening conditions which will reveal time and stress dependent failure modes with equal or greater sensitivity without impairing long term reliability of the Burn-In surviving microciruits.

Typically a dynamic type of Burn-In is preferred at Harris because of its worst case conditions. Static Burn-In is applied only where there is a specific customer requirement.

Capability exists for +125°C through +150°C Burn-In, usually at Harris option. This enables higher throughput of devices by performing, for example, a +150°C, 80-hour Burn-In which is equivalent to the standard +125°C, 160-hour cycle.

Actual Burn-In circuits are available on request through Harris field sales office and may include a variety of schematics, due to the differences in Burn-In oven systems, all of which are functionally equivalent with regard to the Burn-In objectives.

BIPOLAR

Bipolar Memory

4

PROM Functional Index and Selection Guide

PART NUMBER	ORGANIZATION	OUTPUT	NUMBER OF PINS	T_{AA} COMMERCIAL/ MILITARY (ns MAX)	I_{CC} (mA MAX)	(1) PACKAGE AVAILABILITY	PAGE
HM-7602	32 x 8	OC	16	50/60	130	D, P	4-13
HM-7603	32 x 8	TS	16	50/60	130	D, P	4-13
JAN-0512	64 x 8	OC	24	140/140	100	D, F	4-51
HM-7610 HM-7610A HM-7610B	256 x 4	OC	16	60/75 45/65 35/50	130 110 110	D, P, F	4-16
HM-7611 HM-7611A HM-7611B	256 x 4	TS	16	60/75 45/65 35/50	130 110 110	D, P, F	4-16
HM-7620 HM-7620A HM-7620B	512 x 4	OC	16	70/85 50/70 40/55	130 120 120	D, P, F	4-19
HM-7621 HM-7621A HM-7621B	512 x 4	TS	16	70/85 50/70 40/55	130 120 120	D, P, F	4-19
HM-7640 HM-7640A	512 x 8	OC	24	70/85 50/65	170 170	D, P, F, SD	4-22
HM-7641 HM-7641A	512 x 8	TS	24	70/85 45/60	170 170	D, P, F, SD	4-22
HM-7649 HM-7649A	512 x 8	TS	20	60/80 45/60	170 170	D, P, F	4-28
HM-7642 HM-7642A HM-7642B	1024 x 4	OC	18	60/85 50/70 45/55	140 140 140	D, P, F	4-25
HM-7643 HM-7643A HM-7643B	1024 x 4	TS	18	60/85 50/70 45/55	140 140 140	D, P, F	4-25
HM-7681 HM-7681A	1024 x 8	TS	24	70/90 50/–	170 170	D, P, L, F, SD	4-31
HM-7685 HM-7685A	2048 x 4	TS	18	70/90 50/60	170 170	D, P	4-34
HM-76161 HM-76161A HM-76161B	2048 x 8	TS	24	60/80 50/– 35/–	180 180 180	D, P, L, F, SD	4-37 4-37 4-40
HM-76165	4096 x 4	TS	20	60/80	170	D	4-41
HM-76321	4096 x 8	TS	24	65/85	190	D, L	4-44
HM-76641 HM-76641A	8192 x 8	TS	24	85/100 50/–	190 190	D, L	4-47 4-50

(1) D = Ceramic DIP; P = Plastic DIP; L = Leadless Chip Carrier; F = Flatpack; SD = Slimline Ceramic DIP

Harris Generic Programmable Read Only Memories

In 1970, Harris offered the industry's first bipolar Programmable Read Only Memory, and has been a leader in the field of bipolar PROMs from 1970 to date. Harris PROMs are manufactured using the bipolar Junction Isolation process with reliability proven nickel chromium fusible links. Harris has had experience with nickel chromium since 1964 when it was first used for high reliability military circuits because of its high stability characteristics. Harris has been manufacturing nickel chromium fuse links since 1970 when the first PROM was manufactured, and this technology has since developed into the industry's most extensive Programmable Read Only Memory concept. This history has been a factor in giving Harris PROMs their high programming yield and a proven level of quality and reliability.

We now employ a shallow diffused self-aligned emitter aperture process combined with two level aluminum interconnect. This state-of-the-art process technology has been deployed to produce large format devices with the high speed and versatility required by the industry.

Today Harris offers a family of Programmable Read Only Memories which we call the Generic PROMs. They have the following characteristics:

- Coherent part numbering scheme, the 76xxx series.
- Identical programming procedure for all Generic PROMs.
- All parameters are guaranteed over full temperature and voltage.
- The family comprises a complete range of formats.

TESTABILITY

Bipolar memory products from Harris Semiconductor receive extensive testing prior to shipment to the customer. The following is an overview of the testing done on all memory products, as well as a brief description of the test conditions.

D.C. specifications found in this data book and on separate data sheets are tested at wafer probe and at each temperature during package test. These specifications are tested on each device using the loading conditions specified in the data book. All D.C. specifications can be tested, including zero state conditions, through the use of internal test circuitry.

Fusibility is tested at wafer probe by fusing one fuse in each row and column on every device. The inclusion of additional test rows and columns allows this, and the nature of the fusing pattern insures the functionality of the device.

On-board circuitry allows A.C. testing of unprogrammed devices prior to shipment. Characterization has shown that results obtained using this circuitry correlates with the observed performance of patterned devices. This testing allows Harris to guarantee the performance of each device to its corresponding data book specification.

As part of an on-going effort to improve quality and to monitor outgoing fusibility, Quality Assurance statistically samples all product lines, and programs lot samples to a 50% pattern.

This combination of testing procedures and the fact that all devices are tested at each temperature, allows Harris to guarantee each product's specifications over the entire temperature range.

JAN QUALIFIED PROMs

The Harris Semiconductor Bipolar manufacturing line has received certification for processing JAN products. There are fourteen QPL I qualified PROMs. Additional HARRIS PROMs are at various stages of qualification and the status of each at press time is listed below. As the status of these products will change rapidly, we suggest that you contact the nearest Harris Representative or Harris Sales Office for current status.

HARRIS MIL-GRADE BIPOLAR PROMs

SLASH NUMBER	PART NUMBER	NUMBER OF BITS	ORGANIZATION	DESCRIPTION	NUMBER OF PINS
20101BJB	JAN-0512	512	64 x 8	Open-Collector Output	24
20701BEB	HM-7602	256	32 x 8	Open-Collector Output	16
20702BEB	HM-7603	256	32 x 8	Three-State Output	16
20301BEB	HM-7610	1024	256 x 4	Open-Collector Output	16
20302BEB	HM-7611	1024	256 x 4	Three-State Output	16
20401BEB	HM-7620	2048	512 x 4	Open-Collector Output	16
20402BEB	HM-7621	2048	512 x 4	Three-State Output	16
20801BJB	HM-7640	4096	512 x 8	Open-Collector Output	24
20802BJB	HM-7641	4096	512 x 8	Three-State Output	24
20601BVB	HM-7642	4096	1K x 4	Open-Collector Output	18
20602BVB	HM-7643	4096	1K x 4	Three-State Output	18
20904BJB	HM-7681	8192	1K x 8	Three-State Output	24
20902BVB	HM-7685	8192	2K x 4	Three-State Output	18
21002BJB	HM-76161	16384	2K x 8	Three-State Output	24
21102BJB	HM-76321*	32768	4K x 8	Three-State Output	24
21202BJB	HM-76641*	65536	8K x 8	Three-State Output	24

* Qualification to be scheduled upon release of finalized issue of applicable 38510 Slash Sheet.

HARRIS

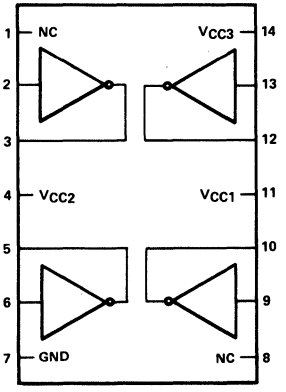
HD-6600

QUAD POWER STROBE

Features

- HIGH DRIVE CURRENT—150mA
- HIGH SPEED 50ns TYPICAL
- TTL COMPATIBLE INPUTS
- DIELECTRIC ISOLATION
- QUAD MONOLITHIC CONSTRUCTION
- POWER SUPPLY FLEXIBILITY
- LOW POWER:
  - STANDBY—30mW/CIRCUIT
  - ACTIVE—95mW/CIRCUIT

Logic Diagram

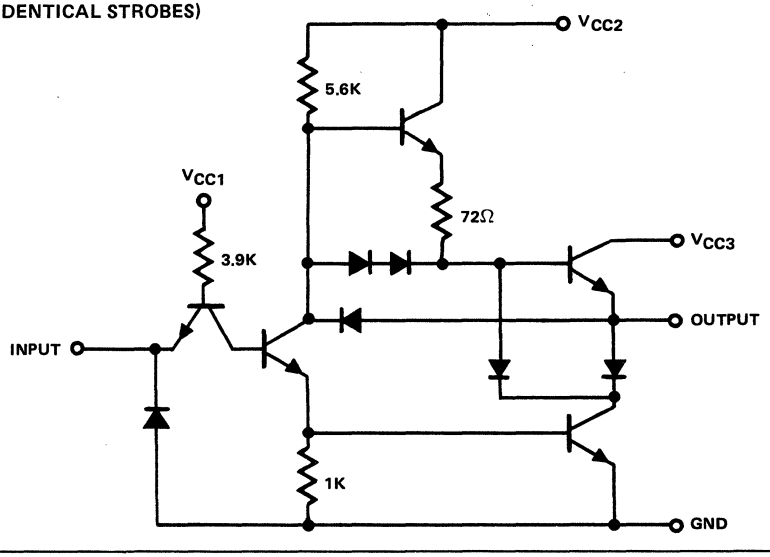


Description

The HD-6600 Quad Power Strobe is constructed with Harris Dielectric Isolation Bipolar Monolithic Process. The design incorporates power supply flexibility with TTL compatible inputs and high current outputs. This circuit is intended for use in power switched PROM arrays.

Circuit Diagram

(ONE OF FOUR IDENTICAL STROBES)



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	V_{CC1}	+8 VDC
	V_{CC2}	+18 VDC
	V_{CC3}	+18 VDC
Input Voltage V_{IN}		-0.5 VDC to +5.5 VDC
Storage Temperature T_{STG}		-65°C to +150°C
Output Current I_L		-200mA
Power Dissipation at 25°C		1000mW
		(Derate 9mW/°C Above 60°C)

RECOMMENDED OPERATING CONDITIONS

Power Supplies:	V_{CC1}	5 VDC ± 10%
	V_{CC2}	12 VDC ± 15%
	V_{CC3}	5 VDC ± 20%

ELECTRICAL CHARACTERISTICS

T_A = -55°C to +125°C HD1-6600-2 V_{CC2} = 12.0 VDC
T_A = 0°C to +75°C HD1-6600-5 V_{CC3} = 5.0 VDC

D.C.

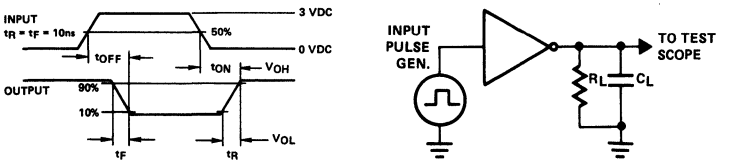
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
I_{IR} I_{IF}	Input Current			60 -1.6	µA mA	V_{IN} = 2.4 VDC V_{IN} = 0.4 VDC — V_{CC1} = 5.5 VDC
V_{IH} V_{IL}	Input Threshold Voltage (Note 1)	2.0		 0.8	V V	V_{CC1} = 4.5 VDC
V_{OH}	Output Voltage (Note 2)	4.75	4.85		V	V_{CC1} = 5.0 VDC V_{IN} = 0.4 VDC — I_L = -150mA DC
V_{OL}				1.0	V	V_{CC1} = 5.0 VDC — I_L = 500µA DC
I_{CC1}	Supply Current (Note 3)		4	6.0	mA	V_{CC1} = 5.5 VDC — V_{IN} = 2.4 VDC
I_{CC2}			40	70	mA	V_{CC1} = 5.5 VDC V_{IN} = 0.4 VDC — I_L = -150mA DC
I_{CC2}	Supply Current (Note 4)		8	15	mA	V_{CC1} = 5.5 VDC V_{IN} = 2.4 VDC — I_L = 0

A.C.

SYMBOL	PARAMETER	TYP.	MAX.	UNITS	CONDITIONS T_A = 25°C
tON	Turn On Delay	50	75	ns	V_{CC1} = 5.0 VDC
tOFF	Turn Off Delay	50	75	ns	V_{CC2} = 12 VDC
					V_{CC3} = 5.0 VDC
tR	Rise Time	40	65	ns	R_L = 33Ω
tF	Fall Time	40	65	ns	C_L = 620 pF

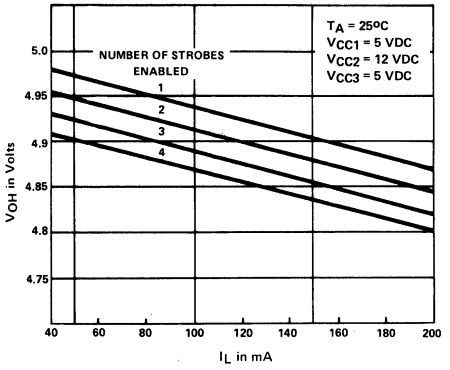
NOTE (1) These are absolute voltages with respect to ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
(2) One strobe enabled.
(3) All strobes enabled.
(4) All strobes disabled.

Switching Time Definitions

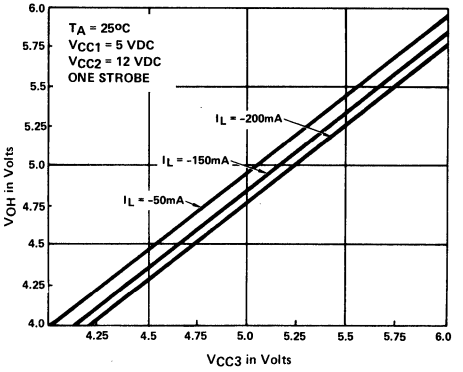


Typical Characteristics

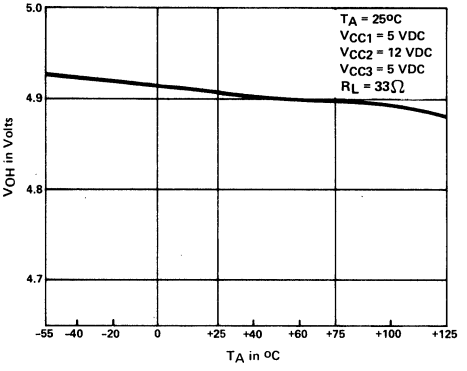
TYPICAL OUTPUT VOLTAGE vs.
LOAD CURRENT AND NUMBER OF STROBES ENABLED



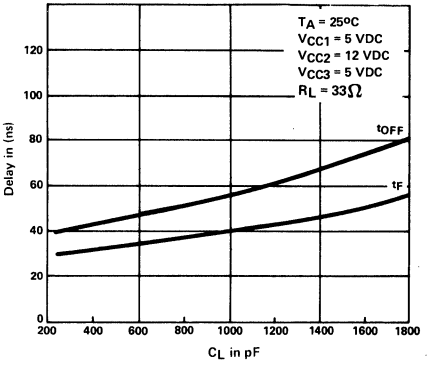
TYPICAL OUTPUT VOLTAGE vs.
V_{CC3} SUPPLY VOLTAGE



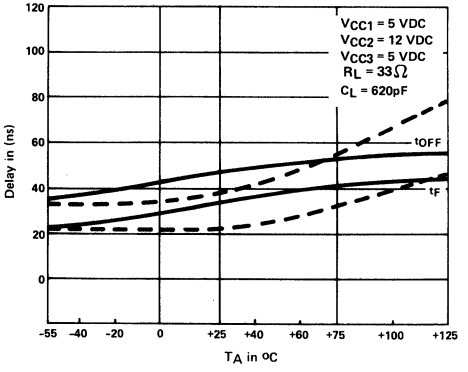
TYPICAL OUTPUT VOLTAGE vs.
AMBIENT TEMPERATURE



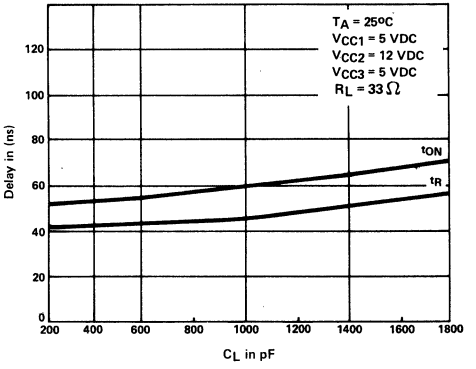
TYPICAL DELAY t_{OFF} AND t_F vs.
LOAD CAPACITANCE



TYPICAL DELAY vs.
AMBIENT TEMPERATURE



TYPICAL DELAY t_{ON} AND t_R vs.
LOAD CAPACITANCE



HARRIS

Not Recommended For New Designs

MONOLITHIC DIODE MATRICES

Features

- FIELD PROGRAMMABLE
- CMOS COMPATIBLE
- ZERO POWER DISSIPATION
- FAST SWITCHING
- FIVE POPULAR ORGANIZATIONS

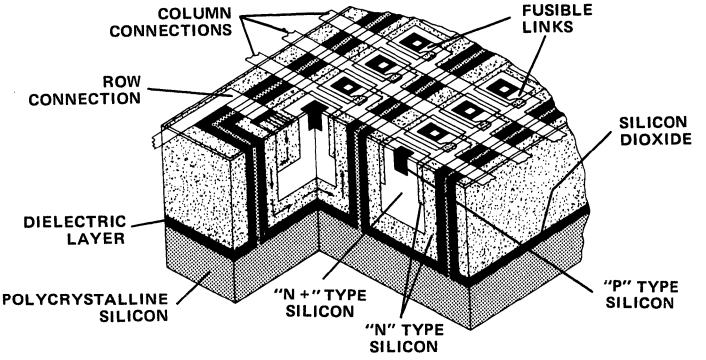
Description

Designed with the CMOS circuit engineer in mind, these versatile diode matrices allow the application of logically powerful programmable solutions to low power CMOS system applications.

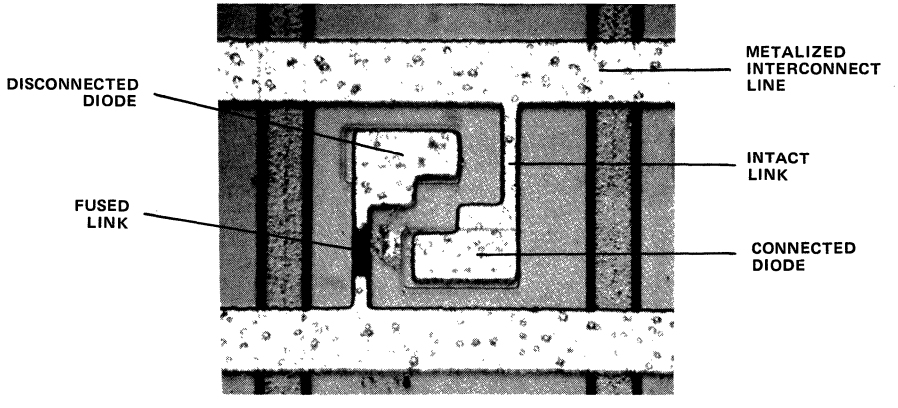
These devices incorporate an advanced dielectric isolation process to eliminate the need for power supply pins and allow parasitic free operation.

Programming is accomplished by cleanly vaporizing a fusible link by application of a brief high voltage pulse to a selected array element. This operation open circuits a row to column orring diode eliminating their former interaction.

Monolithic Structure



Fusible Link System



Monolithic Diode Matrices

HM-0168 6 x 8 DIODE MATRICES

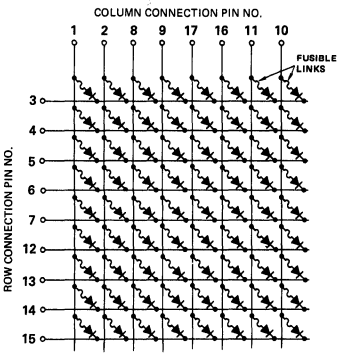
HM-0186 8 x 6 DIODE MATRICES

HM-0410 4 x 10 DIODE MATRICES

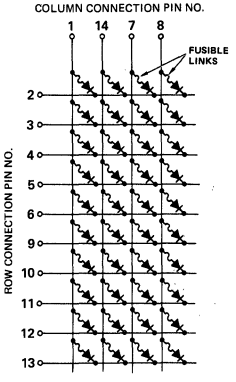
HM-0104 10 x 4 DIODE MATRICES

HM-0198 9 x 8 DIODE MATRICES

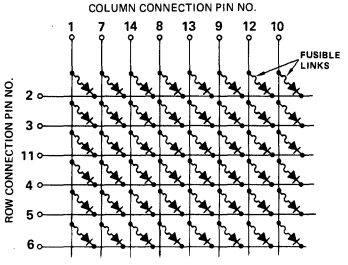
HM-0198



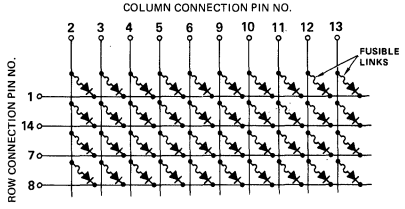
HM-0104



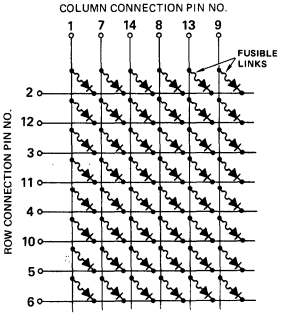
HM-0168



HM-0410



HM-0186



CUSTOM PATTERNS

When ordering a matrix with a custom pattern: Send a paper tape, or copy a matrix pattern and circle out those diodes to be removed from the matrix. Another method to clearly identify a pattern is to call out respective anode and cathode for each diode to be removed, by package pin number.

ABSOLUTE MAXIMUM RATINGS

Forward Current	100mA
Surge Current (100 μs Max.)	200mA
Total Ckt. Dissipation (Still Air)	450mW
Storage Temperature (Ambient)	-65°C to +150°C

Maximum Ratings are limiting values above which permanent damage may occur.

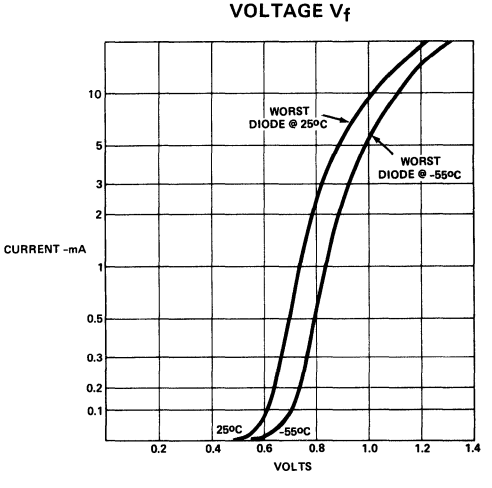
ELECTRICAL CHARACTERISTICS

		HM-0XXX-5		HM-0XXX-2 HM-0XXX-8			
	T_A	0°C to +75°C		-55°C to +125°C			
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS	CONDITIONS
V_F	Forward Voltage		1.5 0.9		1.5 .9	V V	I_F = 20mA I_F = 1mA
BV_R	Reverse Breakdown Voltage	20		30		V	I_{BV} = 100μA
		25°C		25°C			
t_{rr}	Reverse Recovery Time		100		50	ns	I_F = 10mA to I_R = 10mA Recovery to 1mA
C_C	Crosspoint Capacitance (1)				8	pF	V_R = 5V; f = 1MHz (2)

(1) Guaranteed but not 100% tested.

(2) $C_C \propto \frac{1}{V_{BIAS}}$

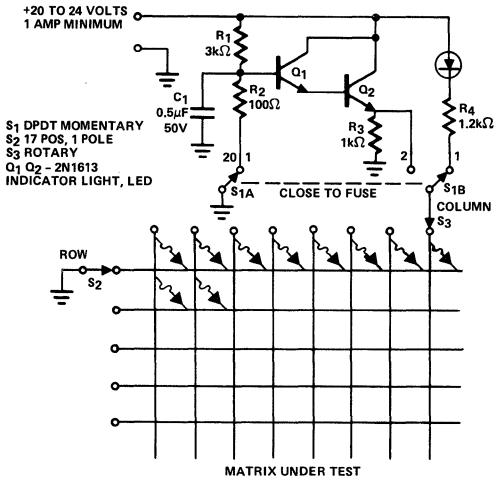
TYPICAL PERFORMANCE CURVES



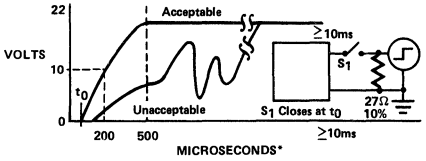
Use a simple supply capable of driving a 27 ohm resistor (carbon) with a clean transition from 0 to 20-24 volts in less than 500μs, for at least 10ms. The diode to be disconnected is selected by setting the row and column switches S2 and S3 respectively as required. When switch S1 is depressed, programming current is provided to column contacts in the matrix. This current opens the fusible link, in series with the selected diode. The peak fusing current required to open a fusible link is approximately 750 milliamperes. As the temperature of the fuse is raised, the aluminum begins to melt. This melting continues until the fuse link separates. The cohesive forces of the melting aluminum retracts the remaining portions of the metal, thereby preventing formation of loose aluminum residues. The melting temperature of aluminum (approximately 650°C) will not affect the passivating layer of silicon dioxide, whose melting temperature is about 1350°C. Test verification is obtained by an indicator lamp or LED placed in series with the column and row switches through the verify contacts of S1 to give electrical indication of the condition of each diode in the matrix before and after fusing.

Caution: Programming is limited to one fuse at a time.

SIMPLE PROGRAMMER



PROGRAMMER TEST CONFIGURATION



* Typ T_{RISE} = 200 μsec to 10V Reference

NOTE: The 27 ohm resistor is only used for oscilloscope measurements of the Power Supply Characteristics becaues it represents a typical unprogrammed fuse/diode.

HM-7602/03

32 x 8 PROM

HM-7602 — Open Collector Outputs
HM-7603 — "Three State" Outputs

Features

- 50ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OUTPUTS WITH ONE ACTIVE LOW CHIP ENABLE
- FAST ACCESS TIME – GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES
- INDUSTRY STANDARD 0.300 INCH 16 PIN PACKAGE
- PRODUCED ON MIL-M-38510 QUALIFIED WAFER FAB LINE
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE – ONE PULSE/BIT TYPICALLY ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY

Description

The HM-7602/03 is a fully decoded high speed Schottky TTL 256/Bit Field Programmable ROM in a 32 word by 8 bit/word format with open collector (HM-7602) or "Three State" (HM-7603) outputs. These PROMs are available in a 16 pin D.I.P. (ceramic or power plastic).

All bits are manufactured storing a logical "1" (Positive Logic) and can be selectively programmed for a logical "0" in any one bit position.

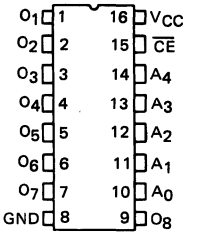
Nickel-chromium fuse technology is used on this and all other Harris Bipolar PROMs.

The HM-7602/03 contains test rows which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows are blown prior to shipment.

There is one chip enable input on the HM-7602/03. $\overline{CE}$ low enables the chip.

Pinout

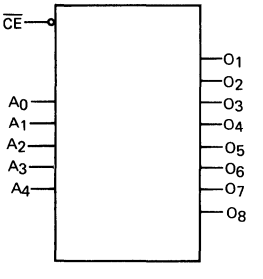
TOP VIEW – DIP



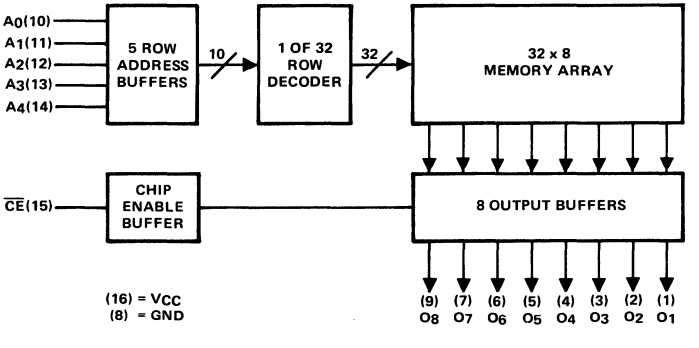
PIN NAMES

$A_0 - A_4$	Address Inputs
$O_1 - O_8$	Data Outputs
$\overline{CE}$	Chip Enable Input

Logic Symbol



Functional Diagram



4 BIPOLAR MEMORY

ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7602/03-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-7602/03-2/-8 (V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V
NOTE: Positive current defined as into device terminals.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/Enable "1" Input Current "0"	– –	– -50.0	+40 -250	µA µA	V_{IH} = V_{CC} Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0* –	1.5 1.5	– 0.8*	V V	V_{CC} = V_{CC} Min V_{CC} = V_{CC} Max.
V_{OH} V_{OL}	Output Voltage "1" "0"	2.4** –	3.2** 0.35	– 0.45	V V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min. I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0"	– –	– –	+100 -100	µA µA	V_{OH}, V_{CC} = V_{CC} Max. V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15**	–	-100**	mA	V_{CC} = V_{CC} Max., V_{OUT} = 0.0V One Output Only for a Max. of 1 Second.
I_{CC}	Power Supply Current	–	90	130	mA	V_{CC} = V_{CC} Max. All Inputs Grounded

* These are absolute voltages with respect to ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
** "Three-State" only.

A.C. ELECTRICAL CHARACTERISTICS (Operating)

Typical measurements are at T_A = +25°C, V_{CC} = +5V

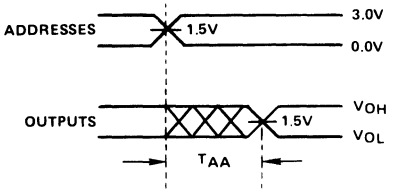
		HM-7602/03-5 5V ±5% 0°C to +75°C		HM-7602/03-2/-8 5V ±10% -55°C to +125°C		
SYMBOL	PARAMETER	TYPICAL	MAXIMUM*	TYPICAL	MAXIMUM*	UNITS
T_{AA}	Address Access Time	30	50	–	60	ns
T_{EA}	Chip Enable Access Time	20	35	–	50	ns

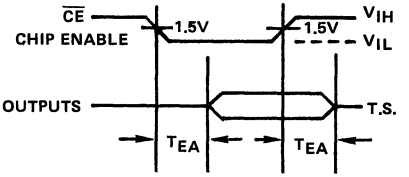
*A.C. limits guaranteed for worst case N^2 sequencing with maximum test frequency of 5MHz.

CAPACITANCE: T_A = 25°C

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	12	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	12	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

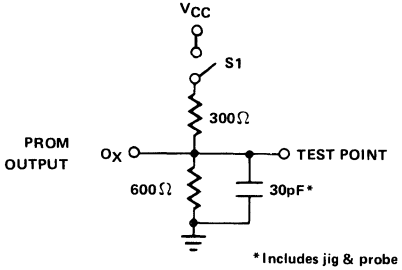
HM-7602/03 SWITCHING TIME DEFINITIONS





NOTE: As is common to all memory devices, output levels can be undefined during the address access period (T_{AA}); however, the outputs are guaranteed to reach stable levels by T_{AA}. It is not recommended that outputs from this class of devices be used to drive edge triggered inputs on subsequent devices (counters, flip-flops, etc.) without proper intermediate synchronization.

A.C. TEST LOAD



This is the A.C. Test Load which Harris Semiconductor uses in its automatic test equipment, and it is recommended that users of Harris bipolar devices use the same or an equivalent load in performing A.C. testing.

HM-7610/11

HIGH SPEED 256 x 4 PROM

HM-7610 - Open Collector Outputs
HM-7611 - "Three State" Outputs

Features

- FAST ADDRESS ACCESS TIME
  - HM-7610/11 . . . . . 60 ns MAXIMUM
  - HM-7610A/11A . . . . . 45 ns MAXIMUM
  - HM-7610B/11B . . . . . 35 ns MAXIMUM
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS AND TWO CHIP ENABLE INPUTS
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE-ONE PULSE/BIT ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- INPUTS AND OUTPUTS TTL COMPATIBLE
- FAST ACCESS TIME – GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- PIN COMPATIBLE WITH INDUSTRY STANDARD 1K PROMs.

Description

The HM-7610/11 are fully decoded high speed Schottky TTL 1024 bit Field Programmable ROM's in a 256 word by 4 bit/word format with open collector (HM-7610) or "three state" (HM-7611) outputs. The PROMs are available in 16 pin D.I.P. (ceramic or power plastic).

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

The HM-7610/11 contain test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

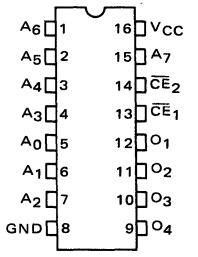
This PROM is intended for use in state of the art high speed logic systems.

Nickel-chromium fuse technology is used on these and all other Harris Bipolar PROMs.

There are two chip enable inputs on the HM-7610/11 where $\overline{CE}_1$ and $\overline{CE}_2$ low enables the chip.

Pinouts

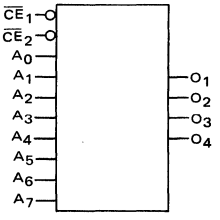
TOP VIEW–DIP



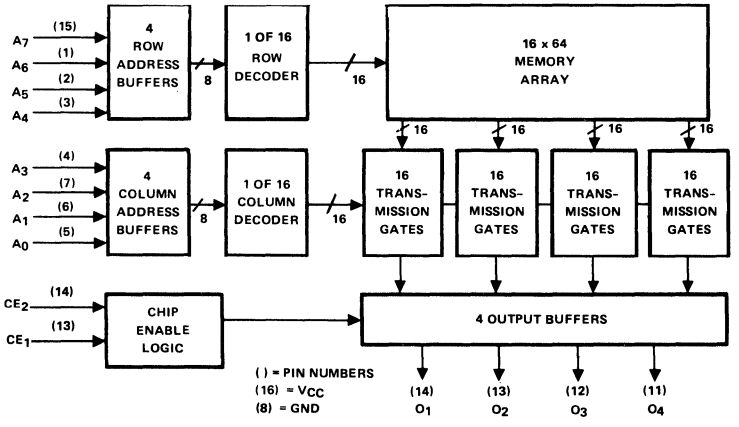
PIN NAMES

$A_0 - A_7$ Address Inputs
$O_1 - O_4$ Data Outputs
$\overline{CE}_1, \overline{CE}_2$ Chip Enable Inputs

Logic Symbol



Functional Diagram



ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7610/11-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-7610/11-2/-8 (V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V.
NOTE: Multiple entries refer to parameter values for "A", "B"/Std.
Positive current defined as into device terminals.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/Enable "1" Input Current "0"	– –	– –	+40 -100/-250	µA µA	V_{IH} = V_{CC} Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0* –	1.5 1.5	– 0.8*	V V	V_{CC} = V_{CC} Min. V_{CC} = V_{CC} Max.
V_{OH} V_{OL}	Output "1" Voltage "0"	2.4** –	3.2** 0.35	– 0.50	V V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min. I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0"	– –	– –	+40/+100 -40/-100**	µA µA	V_{OH}, V_{CC} = V_{CC} Max. V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15**	–	-100**	mA	V_{CC} = V_{CC} Max. V_{OUT} = 0.0V One Output Only for a Max. of 1 Second
I_{CC}	Power Supply Current	–	90	110/130	mA	V_{CC} = V_{CC} Max. All Inputs Grounded

* These are absolute voltages with respect to ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
** "Three-State" only.

A.C. ELECTRICAL CHARACTERISTICS (Operating)

Typical measurements are at T_A = 25°C, V_{CC} = +5V.

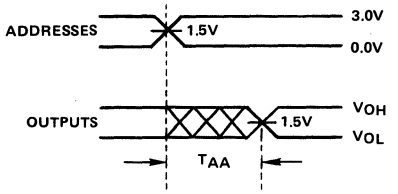
		HM-7610/11-5 5V ±5% 0°C to +75°C						HM-7610/11-2/-8 5V ±10% -55°C to +125°C						
		"B"		"A"		STD		"B"		"A"		STD		
SYMBOL	PARAMETER	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	UNITS
T_{AA}	Address Access Time	25	35	35	45	40	60	–	50	–	65	–	75	ns
T_{EA}	Chip Enable Access Time	–	25	–	25	–	25	–	30	–	30	–	30	ns
T_{DA}	Chip Disable Access Time	–	25	–	25	–	25	–	30	–	30	–	30	

A.C. limits guaranteed for worst case N2 sequencing with maximum test frequency of 5MHz.

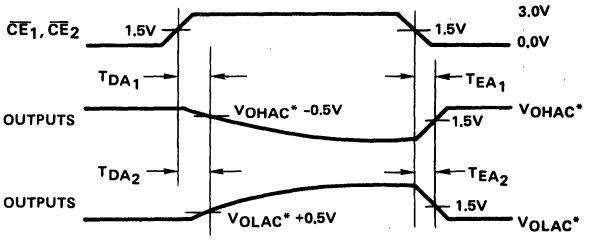
CAPACITANCE: T_A = 25°C

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

HM-7610/11 SWITCHING TIME DEFINITIONS



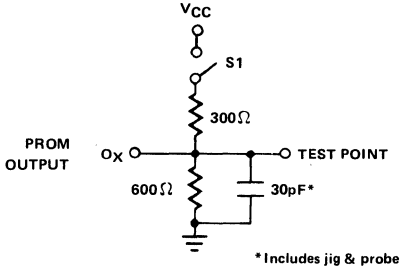
NOTE: As is common to all memory devices, output levels can be undefined during the address access period (T_{AA}); however, the outputs are guaranteed to reach stable levels by T_{AA}. It is not recommended that outputs from this class of devices be used to drive edge triggered inputs on subsequent devices (counters, flip-flops, etc.) without proper intermediate synchronization.



tr, tf < 5ns

*VOLAC AND VOHAC ARE THE MEASURED OUTPUT VOLTAGE LEVELS WHILE ENABLED.

A.C. TEST LOAD



*Includes jig & probe total capacitance

This is the A.C. Test Load which Harris Semiconductor uses in its automatic test equipment, and it is recommended that users of Harris bipolar devices use the same or an equivalent load in performing A.C. testing.

SYMBOL	PARAMETER	S1
T_{AA}	Address Access Time	Closed
*T_{EA_1}	Chip Enable Access Time from "Three State" to V_{OH}	Open
T_{EA_2}	Chip Enable Access Time to V_{OL}	Closed
*T_{DA_1}	Chip Disable Access Time from V_{OH} to "Three State"	Open
T_{DA_2}	Chip Disable Access Time from V_{OL}	Closed

* Applies to "Three-State" only.

HM-7620/21

HIGH SPEED 512 x 4 PROM

HM-7620- Open Collector Outputs
HM-7621 - "Three State" Outputs

Features

- FAST ADDRESS ACCESS TIME
  - HM-7620/21 . . . . . 70 ns MAXIMUM
  - HM-7620A/21A . . . . . 50 ns MAXIMUM
  - HM-7620B/21B . . . . . 40 ns MAXIMUM
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS AND A SINGLE CHIP ENABLE INPUT
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE-ONE PULSE/BIT ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- INPUTS AND OUTPUTS TTL COMPATIBLE
- FAST ACCESS TIME–GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- PIN COMPATIBLE WITH INDUSTRY STANDARD 2K PROMs.

Description

The HM-7620/21 are fully decoded high speed Schottky TTL 2048 bit Field Programmable ROM's in a 512 word by 4 bit/word format with open collector (HM-7620) or "three state" (HM-7621) outputs. These PROMs are available in 16 pin D.I.P. (ceramic or power plastic).

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

The HM-7620/21 contain test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A. C. performance. The fuses in these test rows and columns are blown prior to shipment.

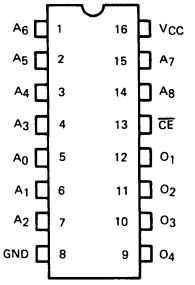
This PROM is intended for use in state of the art high speed logic systems.

Nickel-chromium fuse technology is used on these and all other Harris Bipolar PROMs.

There is a single chip enable input on the HM-7620/21 where $\overline{CE}$ low enables the chip.

Pinout

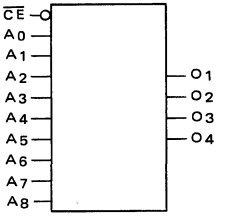
TOP VIEW - DIP



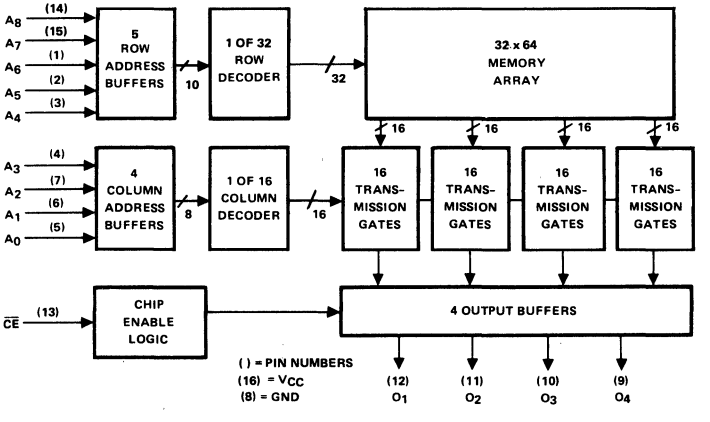
PIN NAMES

$A_0 - A_8$	Address Inputs
$\overline{CE}$	Chip Enable Input
$O_1 - O_4$	Data Outputs

Logic Symbol



Functional Diagram



4 BIPOLAR MEMORY

ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7620/21-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-7620/21-2/-8 (V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V.
NOTE: Multiple entries refer to parameter values for "A", "B"/Std.
Positive current defined as into device terminals.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/enable "1" Input Current "0"	– –	– –	+40 -100/-250	µA µA	V_{IH} = V_{CC} Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0* –	– –	– 0.8*	V V	V_{CC} = V_{CC} Min. V_{CC} = V_{CC} Max.
V_{OH} V_{OL}	Output "1" Voltage "0"	2.4 ** –	3.2** 0.35	– 0.50	V V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min. I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0"	– –	– –	+40/+100 -40/-100**	µA µA	V_{OH}, V_{CC} = V_{CC} Max. V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15**	–	-100**	mA	V_{CC} = V_{CC} Max. V_{OUT} = 0.0V One Output Only for a Max. of 1 Second
I_{CC}	Power Supply Current	–	90	120/130	mA	V_{CC} = V_{CC} Max. All Inputs Grounded

* These are absolute voltages with respect to ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
** "Three-State" only.

A.C. ELECTRICAL CHARACTERISTICS (Operating)

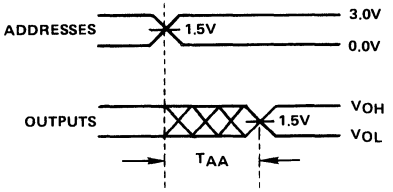
Typical Measurements are at T_A = 25°C, V_{CC} = +5V.

		HM-7620/21 - 5 5V ±5% 0°C to +75°C						HM-7620/21-2/8 5V ±10% –55°C to +125°C						
		"B"		"A"		STD		"B"		"A"		STD		
SYMBOL	PARAMETER	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	UNITS
T_{AA}	Address Access Time	30	40	40	50	50	70	–	55	–	70	–	85	ns
T_{EA}	Chip Enable Access Time	–	25	–	25	–	25	–	30	–	30	–	30	ns
T_{DA}	Chip Disable Access Time	–	25	–	25	–	25	–	30	–	30	–	30	ns

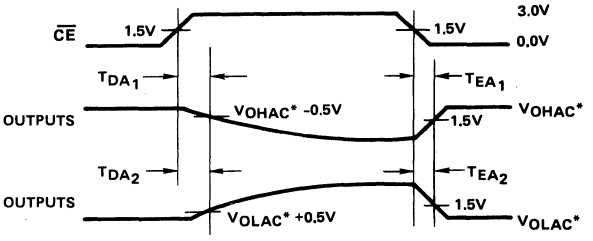
A.C. limits guaranteed for worst case N2 sequencing with maximum test frequency of 5MHz.

CAPACITANCE: T_A = 25°C

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz



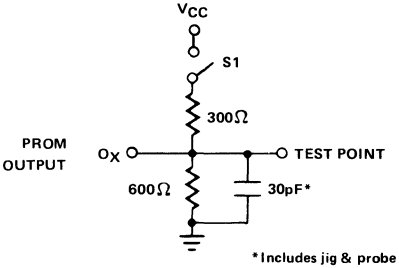
NOTE: As is common to all memory devices, output levels can be undefined during the address access period (T_{AA}); however, the outputs are guaranteed to reach stable levels by T_{AA}. It is not recommended that outputs from this class of devices be used to drive edge triggered inputs on subsequent devices (counters, flip-flops, etc.) without proper intermediate synchronization.



tr, tf < 5ns

*V_{OLAC} AND V_{OHAC} ARE THE MEASURED OUTPUT VOLTAGE LEVELS WHILE ENABLED.

A.C. TEST LOAD



*Includes jig & probe total capacitance

This is the A.C. Test Load which Harris Semiconductor uses in its automatic test equipment, and it is recommended that users of Harris bipolar devices use the same or an equivalent load in performing A.C. testing.

SYMBOL	PARAMETER	S1
T_{AA}	Address Access Time	Closed
*T_{EA1}	Chip Enable Access Time from "Three State" to V_{OH}	Open
T_{EA2}	Chip Enable Access Time to V_{OL}	Closed
*T_{DA1}	Chip Disable Access Time from V_{OH} to "Three State"	Open
T_{DA2}	Chip Disable Access Time from V_{OL}	Closed

*Applies to "Three-State" only.

HM-7640/41

HIGH SPEED 512 x 8 PROM

HM-7640 - Open Collector Outputs
HM-7641 - "Three State" Outputs

Features

- FAST ADDRESS ACCESS TIME
  - HM-7640/41 . . . . . 70 ns MAXIMUM
  - HM-7640A/41A . . . . . 45 ns MAXIMUM
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS AND FOUR CHIP ENABLE INPUTS.
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE — ONE PULSE/BIT ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME – GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- PIN COMPATIBLE WITH INDUSTRY STANDARD 4K PROMs.

Description

The HM-7640/41 are fully decoded high speed Schottky TTL 4096 bit Field Programmable ROMs in a 512 word by 8 bit/word format with open collector (HM-7640) or "three-state" (HM-7641) outputs. These PROMs are available in a 24 pin DIP (ceramic or power plastic).

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

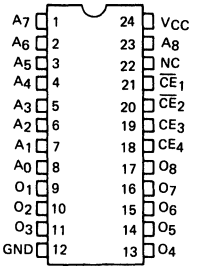
Nickel-chromium fuse technology is used on this and all other Harris Bipolar PROMs.

The HM-7640/41 contain test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

There are four chip enable inputs on the HM-7640/41 where $\overline{CE}_1$ and $\overline{CE}_2$ low and CE_3 and CE_4 high enables the chip.

Pinouts

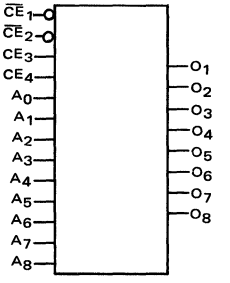
TOP VIEW – DIP



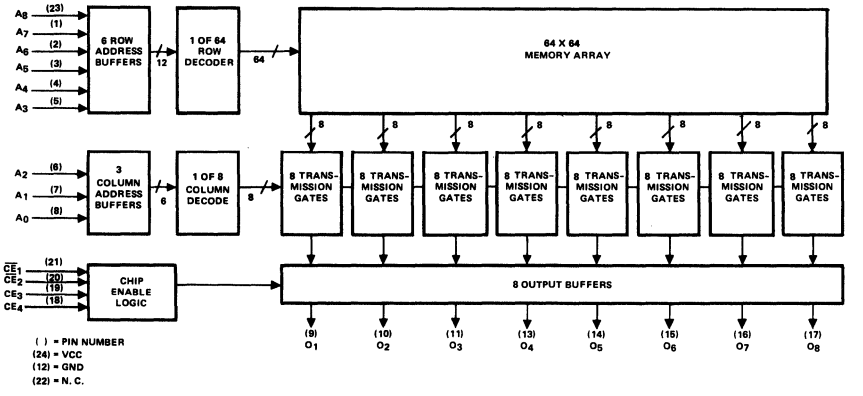
PIN NAMES

$A_0 - A_8$	Address Inputs
$O_1 - O_8$	Data Outputs
$\overline{CE}_1, \overline{CE}_2, CE_3, CE_4$	Chip Enable Inputs

Logic Symbol



Functional Diagram



ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7640/41-5 (V_{CC} = 5.0V ± 5%, T_A = 0°C to +75°C)
HM-7640/41-2/-8 (V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V.
NOTE: Multiple entries refer to parameter values for "A"/Std.
Positive current defined as into device terminals.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/Enable "1" Input Current "0"	– –	– –	+40 -100/-250	µA µA	V_{IH} = V_{CC} Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0* –	– –	– 0.8*	V V	V_{CC} = V_{CC} Min. V_{CC} = V_{CC} Max.
V_{OH} V_{OL}	Output "1" Voltage "0"	2.4** –	3.2** 0.35	– 0.50	V V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min. I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0"	– –	– –	+40/+100 -40/-100**	µA µA	V_{OH}, V_{CC} = V_{CC} Max. V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15**	–	-100*	mA	V_{CC} = V_{CC} Max. V_{OUT} = 0.0V One Output at a Time for Max. of 1 Second
I_{CC}	Power Supply Current	–	125	170	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.

* These are absolute voltages with respect to ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
** "Three-State" only.

A.C. ELECTRICAL CHARACTERISTICS (Operating)

Typical Measurements are at T_A = 25°C, V_{CC} = +5V.

		HM-7640/41-5 5V ±5% 0°C to +75°C				HM-7640/41-2/-8 5V ±10% -55°C to +125°C				
		"A"		STD		"A"		STD		
SYMBOL	PARAMETER	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	UNITS
T_{AA}	Address Access Time	35	45*	50	70	–	60*	–	85	ns
T_{EA}	Chip Enable Access Time	–	35	–	40	–	45	–	50	ns
T_{DA}	Chip Disable Access Time	–	35	–	40	–	45	–	50	ns

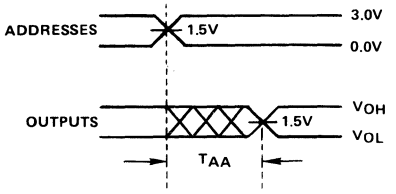
A.C. limits guaranteed for worst case N2 sequencing with maximum test frequency of 5MHz.

*T_{AA} is 50ns for HM-7640A-5 and 65ns for HM-7640A-2/-8

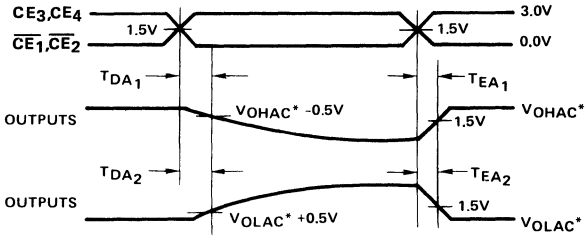
CAPACITANCE: T_A = 25°C

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
CINA, CINCE	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
COUT	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

HM-7640/41 SWITCHING TIME DEFINITIONS



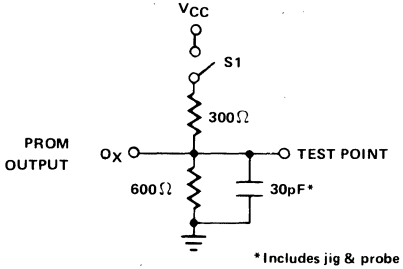
NOTE: As is common to all memory devices, output levels can be undefined during the address access period (T_{AA}); however, the outputs are guaranteed to reach stable levels by T_{AA}. It is not recommended that outputs from this class of devices be used to drive edge triggered inputs on subsequent devices (counters, flip-flops, etc.) without proper intermediate synchronization.



tr, tf < 5ns

*VOLAC AND VOHAC ARE THE MEASURED OUTPUT VOLTAGE LEVELS WHILE ENABLED.

A.C. TEST LOAD



*Includes jig & probe total capacitance

This is the A.C. Test Load which Harris Semiconductor uses in its automatic test equipment, and it is recommended that users of Harris bipolar devices use the same or an equivalent load in performing A.C. testing.

SYMBOL	PARAMETER	S1
T_{AA}	Address Access Time	Closed
*T_{EA_1}	Chip Enable Access Time from "Three State" to V_{OH}	Open
T_{EA_2}	Chip Enable Access Time to V_{OL}	Closed
*T_{DA_1}	Chip Disable Access Time from V_{OH} to "Three State"	Open
T_{DA_2}	Chip Disable Access Time from V_{OL}	Closed

*Applies to "Three-State" only.

HM-7642/43

HIGH SPEED 1K x 4 PROM

HM-7642 - Open Collector Outputs
HM-7643 - "Three State" Outputs

Features

- FAST ADDRESS ACCESS TIME
  - HM-7642/43 . . . . . 60ns MAXIMUM
  - HM-7642A/43A . . . . . 50ns MAXIMUM
  - HM-7642B/43B . . . . . 45ns MAXIMUM
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS AND TWO CHIP ENABLE INPUTS
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE - ONE PULSE/BIT ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME - GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- PIN COMPATIBLE WITH INDUSTRY STANDARD 4K PROMs.

Description

The HM-7642/43 are fully decoded high speed Schottky TTL 4096 bit Field Programmable ROMs in a 1K word by 4 bit/word format with open collector (HM-7642) or "three state" (HM-7643) outputs. These PROM's are available in an 18 pin DIP (ceramic or power plastic).

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

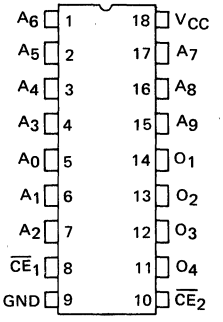
Nickel-Chromium fuse technology is used on these and all other Harris Bipolar PROMs.

The HM-7642/43 contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametrics and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

There are two chip enable inputs on the HM-7642/43. $\overline{CE}_1$ and $\overline{CE}_2$ low enables the chip.

Pinout

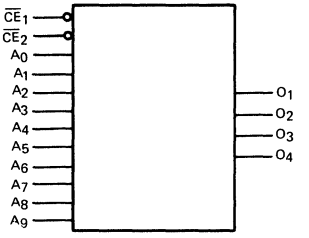
TOP VIEW—DIP



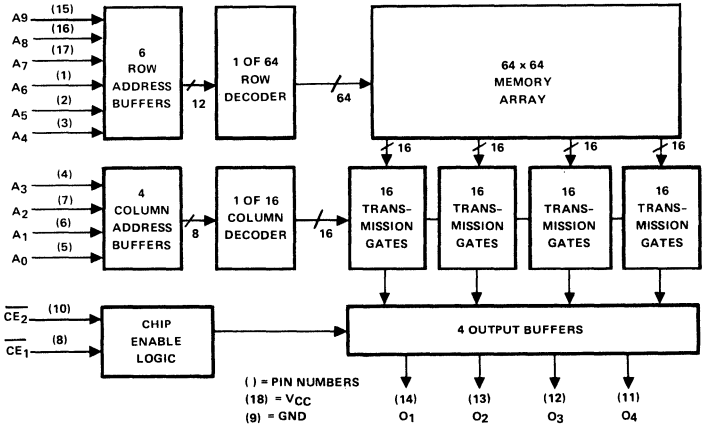
PIN NAMES

$A_0 - A_9$	ADDRESS INPUTS
$O_1 - O_4$	DATA OUTPUTS
$\overline{CE}_1, \overline{CE}_2$	CHIP ENABLE INPUTS

Logic Symbol



Functional Diagram



ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7642/43-5 (V_{CC} = 5.0V ± 5%, T_A = 0°C to +75°C)
HM-742/43-2/-8 (V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V.
NOTE: Multiple entries refer to parameter values for "B"/"A"/Std.
Positive current defined as into device terminals.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/Enable "1" Input Current "0"	– –	– –	+40 -100/-250/-250	μA μA	$V_{IH} = V_{CC}$ Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0* –	– –	– 0.8*	V V	$V_{CC} = V_{CC}$ Min. $V_{CC} = V_{CC}$ Max.
V_{OH} V_{OL}	Output "1" Voltage "0"	2.4** –	3.2** 0.35	– 0.50	V V	I_{OH} = -2.0mA, V_{CC} = VCC Min. I_{OL} = +16mA, $V_{CC} = V_{CC}$ Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0"	– –	– –	+40/+40/+100 -40/-40/-100**	μA μA	V_{OH}, $V_{CC} = V_{CC}$ Max. V_{OL} = 0.3V, $V_{CC} = V_{CC}$ Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15**	–	-100**	mA	$V_{CC} = V_{CC}$ Max. V_{OUT} = 0.0V, One Output at a Time for a Max. of 1 Second
I_{CC}	Power Supply Current	–	100	140	mA	$V_{CC} = V_{CC}$ Max., All Inputs Grounded.

* These are absolute voltages with respect to ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

** "Three-State" only.

A.C. ELECTRICAL CHARACTERISTICS (Operating)

Typical Measurements are at T_A = 25°C, V_{CC} = +5V.

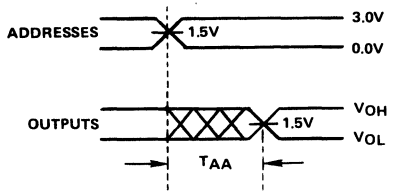
		HM-7642/43-5 5V ±5% 0°C to +75°C						HM-7642/43-2/-8 5V ±10% –55°C to +125°C						
		"B"		"A"		STD		"B"		"A"		STD		
SYMBOL	PARAMETER	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	UNITS
T_{AA}	Address Access Time	35	45	40	50	45	60	–	55	–	70	–	85	ns
T_{EA}	Chip Enable Access Time	–	25	–	25	–	25	–	30	–	30	–	30	ns
T_{DA}	Chip Disable Access Time	–	25	–	25	–	25	–	30	–	30	–	30	ns

A.C. limits guaranteed for worst case N2 sequencing with maximum test frequency of 5MHz.

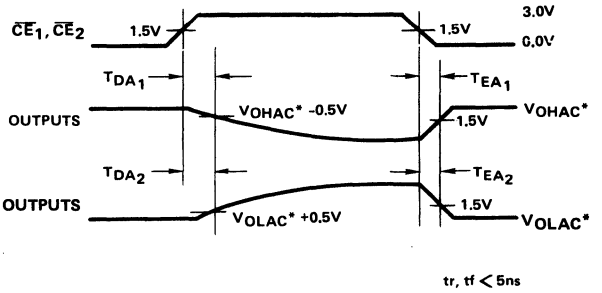
CAPACITANCE: T_A = 25°C

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
CINA, CINCE	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
COUT	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

HM-7642/43 SWITCHING TIME DEFINITIONS

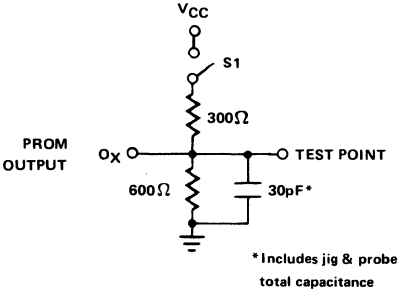


NOTE: As is common to all memory devices, output levels can be undefined during the address access period (T_{AA}); however, the outputs are guaranteed to reach stable levels by T_{AA}. It is not recommended that outputs from this class of devices be used to drive edge triggered inputs on subsequent devices (counters, flip-flops, etc.) without proper intermediate synchronization.



*V_{OLAC} AND V_{OHAC} ARE THE MEASURED OUTPUT VOLTAGE LEVELS WHILE ENABLED.

A.C. TEST LOAD



This is the A.C. Test Load which Harris Semiconductor uses in its automatic test equipment, and it is recommended that users of Harris bipolar devices use the same or an equivalent load in performing A.C. testing.

SYMBOL	PARAMETER	S1
T_{AA}	Address Access Time	Closed
*T_{EA1}	Chip Enable Access Time from "Three State" to V_{OH}	Open
T_{EA2}	Chip Enable Access Time to V_{OL}	Closed
*T_{DA1}	Chip Disable Access Time from V_{OH} to "Three State"	Open
T_{DA2}	Chip Disable Access Time from V_{OL}	Closed

*Applies to "Three-State" only.

HARRIS

HM-7649

HIGH SPEED 512 x 8 PROM

Features

- FAST ADDRESS ACCESS TIME
  - HM-7649 . . . . . 60 ns MAXIMUM
  - HM-7649A . . . . . 45 ns MAXIMUM
- "THREE STATE" OUTPUTS AND A SINGLE CHIP ENABLE INPUT
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE - ONE PULSE/BIT ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME - GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- PIN COMPATIBLE WITH THE 74S473
- LOW INPUT LOADING

Description

The HM-7949 is a fully decoded high speed Schottky TTL 4096 bit Field Programmable ROM in a 512 word by 8 bit/word format with "Three-State" outputs. This PROM is available in a 20 pin DIP (ceramic or power plastic).

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

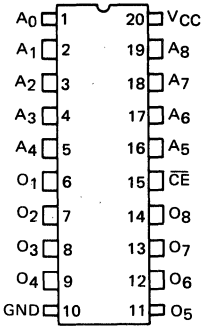
Nickel Chromium fuse technology is used on this and all other Harris Bipolar PROMs.

The pinout is identical to the 74S473 PROM.

The HM-7649 contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

There is a chip enable input on the HM-7649 where $\overline{CE}$ low enables the device.

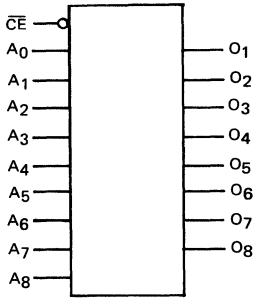
Pinout



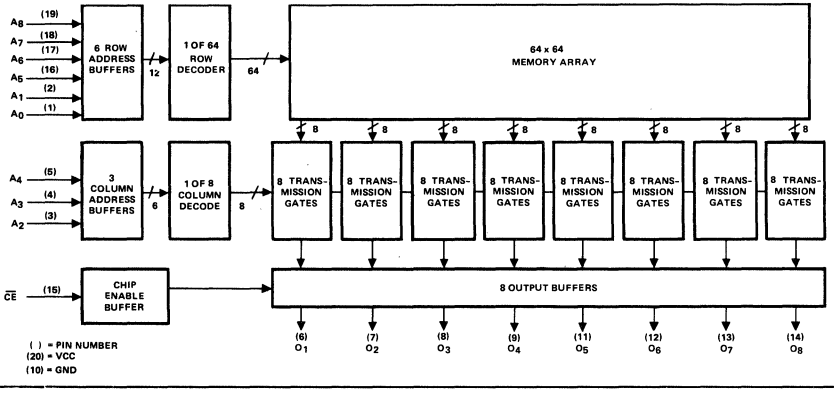
TOP VIEW - D.I.P.

PIN NAMES	
A_0-A_8	Address Inputs
O_1-O_8	Data Outputs
$\overline{CE}$	Chip Enable Input

Logic Symbol



Functional Diagram



ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7649-5 (V_{CC} = 5.0V ± 5%, T_A = 0°C to +75°C)
HM-7649-2/-8 (V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V.
NOTE: Multiple entries refer to parameter values for "A"/Std.
Positive current defined as into device terminals.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/Enable "1" Input Current "0"	– –	– –	+25 -100/-250	µA µA	V_{IH} = V_{CC} Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0* –	– –	– 0.80*	V V	V_{CC} = V_{CC} Min. V_{CC} = V_{CC} Max.
V_{OH} V_{OL}	Output "1" Voltage "0"	2.4 –	3.2 0.35	– 0.50	V V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min. I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0"	– –	– –	+40 -40	µA µA	V_{OH}, V_{CC} = V_{CC} Max. V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-20	–	-100	mA	V_{CC}=V_{CC} Max. V_{OUT}=0.0V, One Output Only for a Max. of 1 Second
I_{CC}	Power Supply Current	–	120	170	mA	V_{CC} = V_{CC} Max. All Inputs Grounded

* These are absolute voltages with respect to ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

A.C. ELECTRICAL CHARACTERISTICS (Operating)

Typical Measurements are at T_A = 25°C, V_{CC} = +5V.

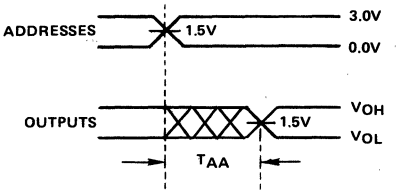
		HM-7649-5 5V ±5% 0°C to +75°C				HM-7649-2/-8 5V ±10% -55°C to +125°C				
		"A"		STD		"A"		STD		
SYMBOL	PARAMETER	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	UNITS
T_{AA}	Address Access Time	35	45	40	60	–	60	–	80	ns
T_{EA}	Chip Enable Access Time	–	35	–	40	–	45	–	50	ns
T_{DA}	Chip Disable Access Time	–	35	–	40	–	45	–	50	ns

A.C. limits guaranteed for worst case N2 sequencing with maximum test frequency of 5MHz.

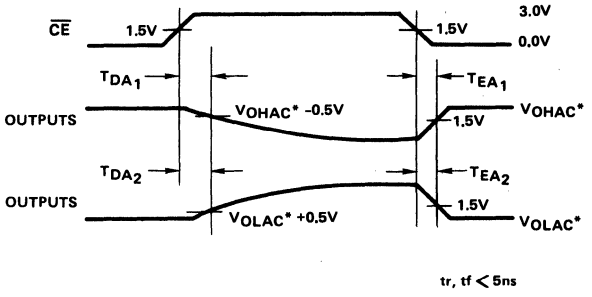
CAPACITANCE: T_A = 25°C

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

HM-7649 SWITCHING TIME DEFINITIONS



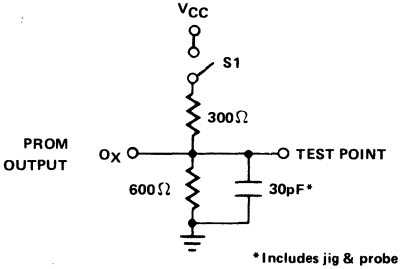
NOTE: As is common to all memory devices, output levels can be undefined during the address access period (T_{AA}); however, the outputs are guaranteed to reach stable levels by T_{AA}. It is not recommended that outputs from this class of devices be used to drive edge triggered inputs on subsequent devices (counters, flip-flops, etc.) without proper intermediate synchronization.



tr, tf < 5ns

*V_{OLAC} AND V_{OHAC} ARE THE MEASURED OUTPUT VOLTAGE LEVELS WHILE ENABLED.

A.C. TEST LOAD



*Includes jig & probe total capacitance

This is the A.C. Test Load which Harris Semiconductor uses in its automatic test equipment, and it is recommended that users of Harris bipolar devices use the same or an equivalent load in performing A.C. testing.

SYMBOL	PARAMETER	S1
T_{AA}	Address Access Time	Closed
T_{EA_1}	Chip Enable Access Time from "Three State" to V_{OH}	Open
T_{EA_2}	Chip Enable Access Time from "Three State" to V_{OL}	Closed
T_{DA_1}	Chip Disable Access Time from V_{OH} to "Three State"	Open
T_{DA_2}	Chip Disable Access Time from V_{OL} to "Three State"	Closed

Features

- **FAST ADDRESS ACCESS TIME**
  - **HM-7681 . . . . . 70 ns MAXIMUM**
  - **HM-7681A . . . . . 50 ns MAXIMUM**
- **"THREE STATE" OUTPUTS AND FOUR CHIP ENABLE INPUTS**
- **SIMPLE HIGH SPEED PROGRAMMING PROCEDURE-ONE PULSE/BIT ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY**
- **FAST ACCESS TIME - GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES**
- **PIN COMPATIBLE WITH INDUSTRY STANDARD 8K PROMs**

Description

The HM-7681 is a fully decoded high speed Schottky TTL 8192 bit Field Programmable ROM in a 1K word by 8 bit/word format with "Three State" outputs. This PROM is available in a 24 pin D.I.P. (ceramic or power plastic).

All bits are manufactured storing a logic "1" (Positive Logic) and can be selectively programmed for a logical "0" in any one bit position.

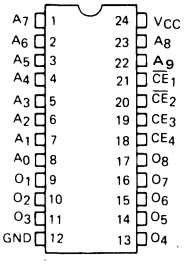
Nickel-chromium fuse technology is used on this and all other HARRIS Bipolar PROMs.

The HM-7681 contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

There are four chip enable inputs on the HM-7681. $\overline{CE}_1$, $\overline{CE}_2$ low, and CE_3, CE_4 high enables the chip.

Pinouts

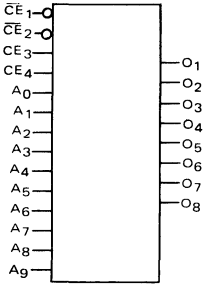
TOP VIEW – DIP



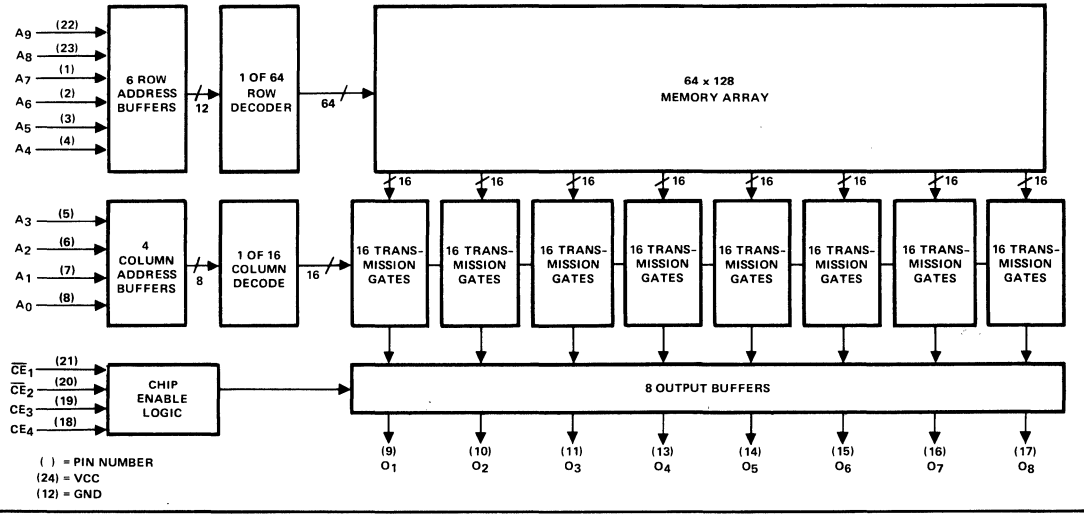
PIN NAMES

A_0 - A_9 Address Inputs
O_1 - O_8 Data Outputs
$\overline{CE}_1$, $\overline{CE}_2$, CE_3, CE_4 Chip Enable Inputs

Logic Symbol



Functional Diagram



ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	0°C to + 75°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7681-5 (V_{CC} = 5.0V ± 5%, T_A = 0°C to +75°C)
HM-7681-2/-8 (V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V.
NOTE: Multiple entries refer to parameter values for "A"/Std.
Positive current defined as into device terminals.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/enable "1" Input Current "0"	– –	– –	+40 -100/-250	µA µA	V_{IH} = V_{CC} Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0* –	– –	– 0.8*	V V	V_{CC} = V_{CC} Min. V_{CC} = V_{CC} Max.
V_{OH} V_{OL}	Output "1" Voltage "0"	2.4 –	3.2 0.35	– 0.50	V V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min. I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0"	– –	– –	+40 -40	µA µA	V_{OH}, V_{CC} = V_{CC} Max. V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15	–	-100	mA	V_{CC} = V_{CC} Max., V_{OUT} = 0.0V One Output Only for a Max. of 1 Second
I_{CC}	Power Supply Current	–	130	170	mA	V_{CC} = V_{CC} Max. All Inputs Grounded

* These are absolute voltages with respect to ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

A.C. ELECTRICAL CHARACTERISTICS (Operating)

Typical Measurements are at T_A = 25°C, V_{CC} = +5V.

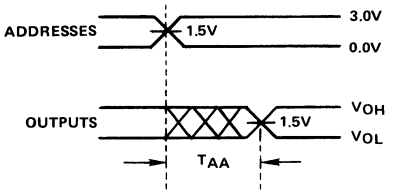
		HM-7681-5 5V ±5% 0°C to +75°C				HM-7681-2/8 5V ±10% –55°C to +125°C		
		"A"		STD		STD		
SYMBOL	PARAMETER	TYP	MAX	TYP	MAX	TYP	MAX	UNITS
T_{AA}	Address Access Time	40	50	50	70	–	90	ns
T_{EA}	Chip Enable Access Time	–	35	–	40	–	50	ns
T_{DA}	Chip Disable Access Time	–	35	–	40	–	50	ns

A.C. Limits guaranteed for worst case N^2 sequencing with maximum test frequency of 5MHz.

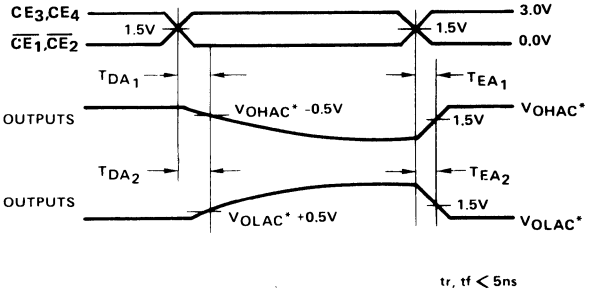
CAPACITANCE : T_A = 25°C

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

HM-7681 SWITCHING TIME DEFINITIONS

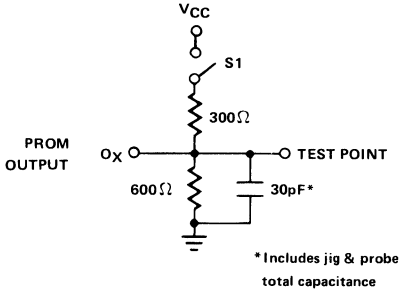


NOTE: As is common to all memory devices, output levels can be undefined during the address access period (T_{AA}); however, the outputs are guaranteed to reach stable levels by T_{AA}. It is not recommended that outputs from this class of devices be used to drive edge triggered inputs on subsequent devices (counters, flip-flops, etc.) without proper intermediate synchronization.



*V_{OLAC} AND V_{OHAC} ARE THE MEASURED OUTPUT VOLTAGE LEVELS WHILE ENABLED.

A.C. TEST LOAD



This is the A.C. Test Load which Harris Semiconductor uses in its automatic test equipment, and it is recommended that users of Harris bipolar devices use the same or an equivalent load in performing A.C. testing.

SYMBOL	PARAMETER	S1
T_{AA}	Address Access Time	Closed
T_{EA_1}	Chip Enable Access Time from "Three State" to V_{OH}	Open
T_{EA_2}	Chip Enable Access Time from "Three State" to V_{OL}	Closed
T_{DA_1}	Chip Disable Access Time from V_{OH} to "Three State"	Open
T_{DA_2}	Chip Disable Access Time from V_{OL} to "Three State"	Closed

HARRIS

HM-7685

HIGH SPEED 2K x 4 PROM

Features

- FAST ADDRESS ACCESS TIME
  - HM-7685 . . . . . 70ns MAXIMUM
  - HM-7685A . . . . . 50ns MAXIMUM
- "THREE STATE" OUTPUTS AND A SINGLE CHIP ENABLE INPUT
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE - ONE PULSE/BIT ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY
- FAST ACCESS TIME - GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES
- PIN COMPATIBLE WITH INDUSTRY STANDARD 8K PROMs

Description

The HM-7685 is a fully decoded high speed Schottky TTL 8192- bit Field Programmable ROM in a 2K word by a 4 bit/word format with "Three State" outputs. This PROM is available in an 18 pin DIP (ceramic or power plastic).

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

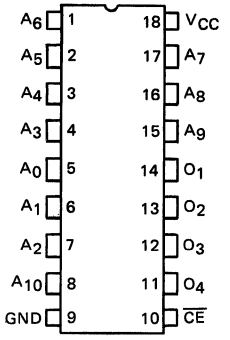
Nickel-chromium fuse technology is used on this and all other Harris Bipolar PROMs.

The HM-7685 contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametrics and A. C. performance. The fuses in these test rows and columns are blown prior to shipment.

There is a chip enable on the HM-7685. $\overline{CE}$ low enables the chip.

Pinouts

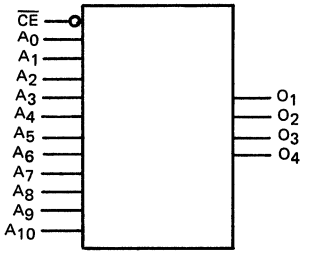
TOP VIEW - DIP



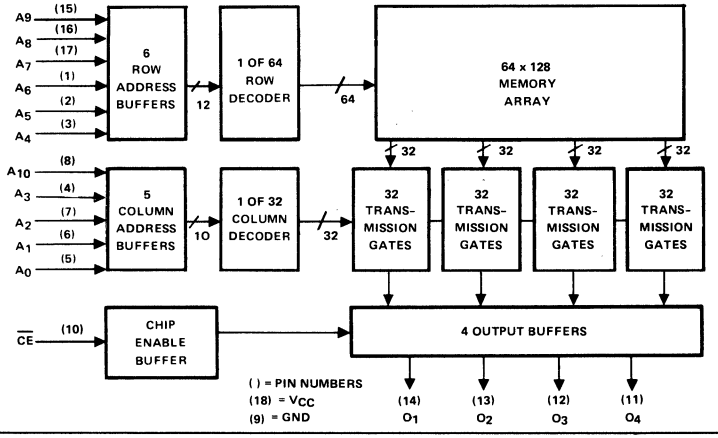
PIN NAMES

$A_0 - A_{10}$ Address Inputs
$O_1 - O_4$ Data Outputs
$\overline{CE}$ Chip Enable Input

Logic Symbol



Functional Diagram



ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7685-5 (V_{CC} = 5.0V ± 5%, T_A = 0°C to +75°C)
HM-7685-2/-8 (V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V
NOTE: Multiple entries refer to parameter values of "A"/Std.
Positive current defined as into device terminals.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH}	Address/Enable "1"	–	–	+40	µA	V_{IH} = V_{CC} Max.
I_{IL}	Input Current "0"	–	–	-100/-250	µA	V_{IL} = 0.45V
V_{IH}	Input Threshold "1"	2.0*	–	–	V	V_{CC} = V_{CC} Min.
V_{IL}	Voltage "0"	–	–	0.8*	V	V_{CC} = V_{CC} Max.
V_{OH}	Output "1"	2.4	3.2	–	V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min.
V_{OL}	Voltage "0"	–	0.35	0.50	V	I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE}	Output Disable "1"	–	–	+40	µA	V_{OH}, V_{CC} = V_{CC} Max.
I_{OLE}	Current "0"	–	–	-40	µA	V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15	–	-100	mA	V_{CC}=V_{CC} Max. V_{OUT}=0.0V, One Output at a Time for a Max. of 1 Second
I_{CC}	Power Supply Current	–	120	170	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.

* These are absolute voltages with respect to ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

A.C. ELECTRICAL CHARACTERISTICS (Operating)

Typical measurements are at T_A = 25°C, V_{CC} = +5V.

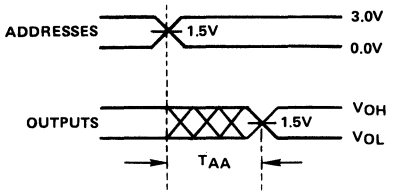
		HM-7685-5 5V ±5% 0°C to +75°C				HM-7685-2/-8 5V ±10% –55°C to +125°C				
		"A"		STD		"A"		STD		
SYMBOL	PARAMETER	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	UNITS
T_{AA}	Address Access Time	40	50	50	70	–	60	–	90	ns
T_{EA}	Chip Enable Access Time	–	30	–	40	–	35	–	50	ns
T_{DA}	Chip Disable Access Time	–	30	–	40	–	35	–	50	ns

A.C. limits guaranteed for worst case N2 sequencing with maximum test frequency of 5MHz.

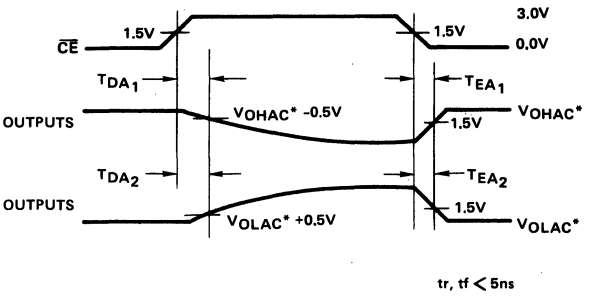
CAPACITANCE: T_A = 25°C

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
CINA, CINCE	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
COUT	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

HM-7685 SWITCHING TIME DEFINITIONS

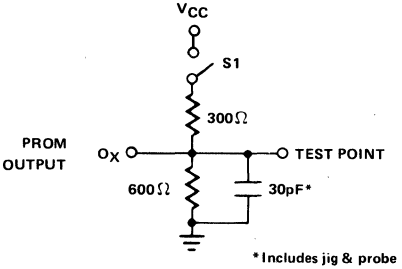


NOTE: As is common to all memory devices, output levels can be undefined during the address access period (T_{AA}); however, the outputs are guaranteed to reach stable levels by T_{AA}. It is not recommended that outputs from this class of devices be used to drive edge triggered inputs on subsequent devices (counters, flip-flops, etc.) without proper intermediate synchronization.



*V_{OLAC} AND V_{OHAC} ARE THE MEASURED OUTPUT VOLTAGE LEVELS WHILE ENABLED.

A.C. TEST LOAD



This is the A.C. Test Load which Harris Semiconductor uses in its automatic test equipment, and it is recommended that users of Harris bipolar devices use the same or an equivalent load in performing A.C. testing.

SYMBOL	PARAMETER	S1
T_{AA}	Address Access Time	Closed
T_{EA_1}	Chip Enable Access Time from "Three State" to V_{OH}	Open
T_{EA_2}	Chip Enable Access Time from "Three State" to V_{OL}	Closed
T_{DA_1}	Chip Disable Access Time from V_{OH} to "Three State"	Open
T_{DA_2}	Chip Disable Access Time from V_{OL} to "Three State"	Closed

HM-76161

HIGH SPEED 2K x 8 PROM

Features

- FAST ADDRESS ACCESS TIME
  - HM-76161 . . . . . 60ns MAXIMUM
  - HM-76161A . . . . . 50ns MAXIMUM
- "THREE STATE" OUTPUTS AND THREE CHIP ENABLE INPUTS
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE - ONE PULSE/BIT ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY
- FAST ACCESS TIME - GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES
- PIN COMPATIBLE WITH INDUSTRY STANDARD 16K PROMs

Description

The HM-76161 is a fully decoded high speed Schottky TTL 16,384 bit Field Programmable ROM in a 2K word by 8 bit/word format with "Three State" outputs. This PROM is available in a 24 pin DIP (ceramic or power plastic).

All bits are manufactured storing a logical "1" (Positive Logic) and can be selectively programmed for a logical "0" in any bit position.

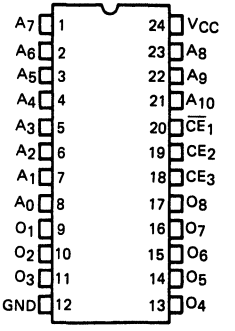
The nickel-chromium fuse technology used is the same as all other Harris Bipolar PROMs and the JAN approved MIL-M-38510 PROMs.

The HM-76161 contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametrics and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

There are three chip enable inputs on the HM-76161. $\overline{CE}_1$ low, CE_2 high, and CE_3 high enables the device.

Pinout

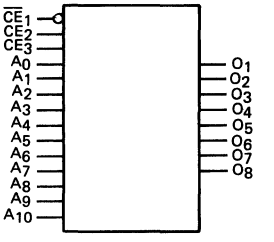
TOP VIEW - D I P



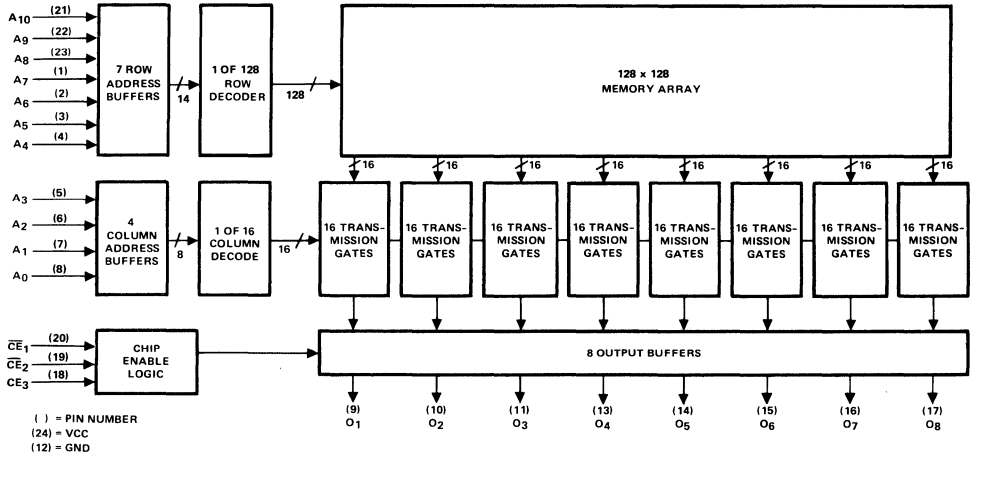
PIN NAMES

$A_0 - A_{10}$	Address Inputs
$O_1 - O_8$	Data Outputs
$\overline{CE}_1, CE_2, CE_3$	Chip Enable Inputs

Logic Symbol



Functional Diagram



4 BIPOLAR MEMORY

ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-76161-5 (V_{CC} = 5.0V ± 5%, T_A = 0°C to +75°C)
HM-76161-2/-8 (V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V.
NOTE: Positive current defined as into device terminals.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/Enable "1" Input Current "0"	– –	– –	+40 -100	µA µA	V_{IH} = V_{CC} Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0* –	– –	– 0.8*	V V	V_{CC} = V_{CC} Min. V_{CC} = V_{CC} Max.
V_{OH} V_{OL}	Output "1" Voltage "0"	2.4 –	3.2 0.35	– 0.50	V V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min. I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0"	– –	– –	+40 -40	µA µA	V_{OH}, V_{CC} = V_{CC} Max. V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15	–	-100	mA	V_{CC} = V_{CC} Max. V_{OUT} = 0.0V One Output at a Time for Max. of 1 Second
I_{CC}	Power Supply Current	–	130	180	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.

* These are absolute voltages with respect to ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

A.C. ELECTRICAL CHARACTERISTICS (Operating)

Typical measurements are at T_A = 25°C, V_{CC} = +5V

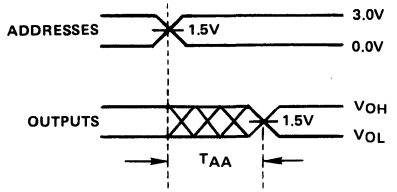
		HM-76161-5 5V ±5% 0°C to +75°C				HM-76161-2/-8 5V ±10% –55°C to +125°C		
		"A"		STD		STD		
SYMBOL	PARAMETER	TYP	MAX	TYP	MAX	TYP	MAX	UNITS
T_{AA}	Address Access Time	40	50	45	60	–	80	ns
T_{EA}	Chip Enable Access Time	–	40	–	40	–	50	ns
T_{DA}	Chip Disable Access Time	–	40	–	40	–	50	ns

A.C. limits guaranteed for worst case N^2 sequencing with maximum test frequency of 5MHz

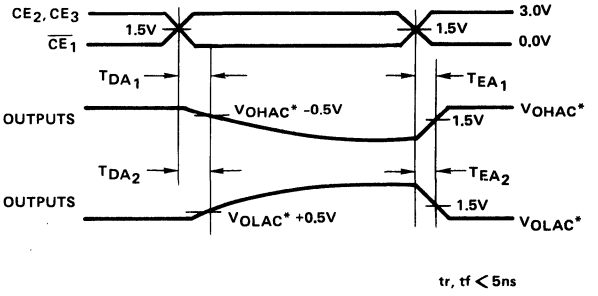
CAPACITANCE: T_A = 25°C

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

HM-76161 SWITCHING TIME DEFINITIONS



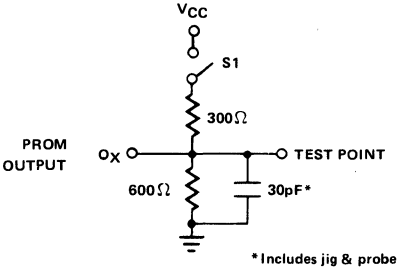
NOTE: As is common to all memory devices, output levels can be undefined during the address access period (T_{AA}); however, the outputs are guaranteed to reach stable levels by T_{AA}. It is not recommended that outputs from this class of devices be used to drive edge triggered inputs on subsequent devices (counters, flip-flops, etc.) without proper intermediate synchronization.



tr, tf < 5ns

*V_{OLAC} AND V_{OHAC} ARE THE MEASURED OUTPUT VOLTAGE LEVELS WHILE ENABLED.

A.C. TEST LOAD



*Includes jig & probe total capacitance

This is the A.C. Test Load which Harris Semiconductor uses in its automatic test equipment, and it is recommended that users of Harris bipolar devices use the same or an equivalent load in performing A.C. testing.

SYMBOL	PARAMETER	S1
T_{AA}	Address Access Time	Closed
T_{EA_1}	Chip Enable Access Time from "Three State" to V_{OH}	Open
T_{EA_2}	Chip Enable Access Time from "Three State" to V_{OL}	Closed
T_{DA_1}	Chip Disable Access Time from V_{OH} to "Three State"	Open
T_{DA_2}	Chip Disable Access Time from V_{OL} to "Three State"	Closed

HARRIS

HM-76161B

HIGH SPEED 2K x 8 PROM

Preview

Features

- 35 nsec MAXIMUM ADDRESS ACCESS TIME (0°C TO +75°C)
- "THREE STATE" OUTPUTS AND THREE CHIP ENABLE INPUTS
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE – ONE PULSE/BIT ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME – GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES
- PIN COMPATIBLE WITH INDUSTRY STANDARD 16K PROMs.

Description

The HM-76161 is a fully decoded high speed Schottky TTL 16,384 bit Field Programmable ROM in a 2K word by 8 bit/word format with "Three State" outputs. This PROM is available in a 24 pin DIP (ceramic or power plastic).

All bits are manufactured storing a logical "1" (Positive Logic) and can be selectively programmed for a logical "0" in any bit position.

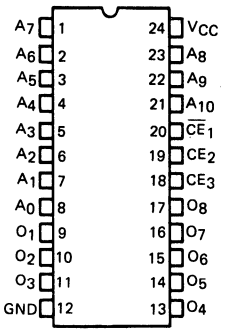
The nickel-chromium fuse technology used is the same as all other Harris Bipolar PROMs and the JAN approved MIL-M-38510 PROMs.

The HM-76161 contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametrics and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

There are three chip enable inputs on the HM-76161. $\overline{CE}_1$ low, CE_2 high, and CE_3 high enables the device.

Pinout

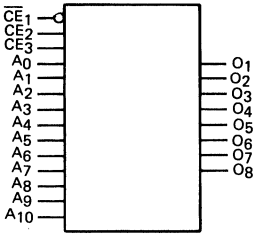
TOP VIEW - D I P



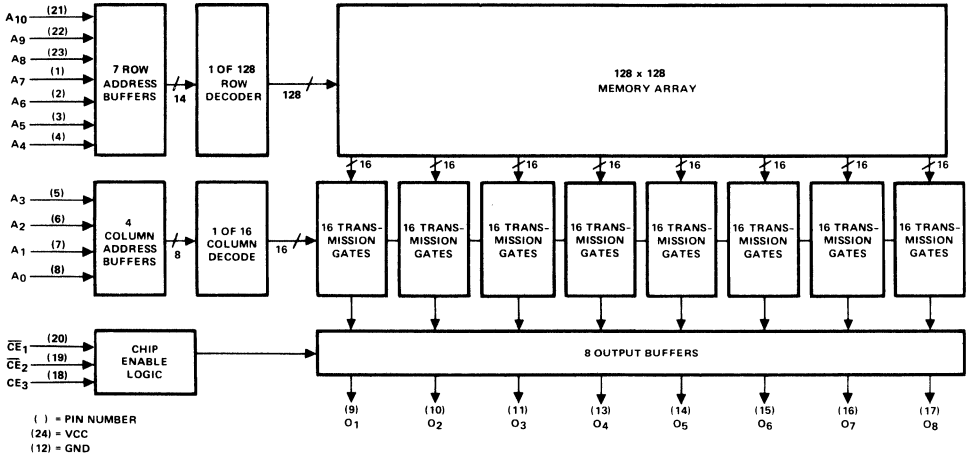
PIN NAMES

$A_0 - A_{10}$	Address Inputs
$O_1 - O_8$	Data Outputs
$\overline{CE}_1, CE_2, CE_3$	Chip Enable Inputs

Logic Symbol



Functional Diagram



HM-76165

4K x 4 PROM

Features

- 60ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OUTPUTS WITH TWO ACTIVE LOW CHIP ENABLES
- FAST ACCESS TIME - GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES
- INDUSTRY STANDARD 0.300 INCH 20 PIN PACKAGE
- PRODUCED ON MIL-M-38510 QUALIFIED WAFER FAB LINE
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE - ONE PULSE/BIT TYPICALLY ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY

Description

The HM-76165 PROM is a fully decoded Schottky TTL 16,384 bit field programmable ROM in a 4K word by 4 bit/word format with "Three State" outputs. This PROM is available in a 20 pin 0.300 inch wide DIP.

All bits are manufactured storing a logical "1" and can be selectively programmed for a logical "0" in any bit position.

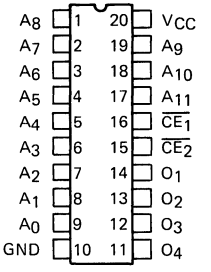
MIL-M-38510 qualified NiCr technology is used on the HM-76165 and all other HARRIS bipolar PROMs.

The HM-76165 contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametrics and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

The HM-76165 utilizes two chip enables where $\overline{CE_1}$ low and $\overline{CE_2}$ low enables the device.

Pinout

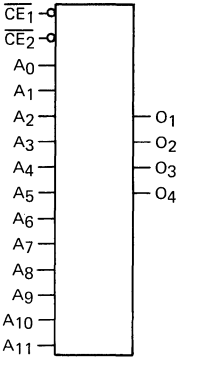
TOP VIEW – DIP



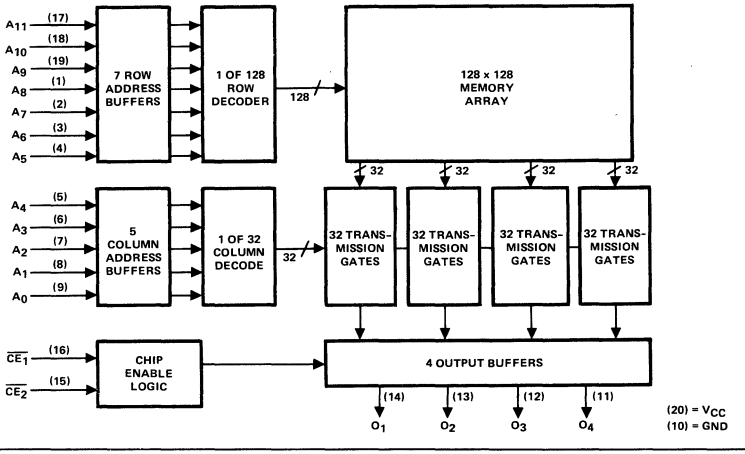
PIN NAMES

$A_0 - A_{11}$	Address Inputs
$O_1 - O_4$	Data Outputs
$\overline{CE_1}, \overline{CE_2}$	Chip Enable Inputs

Logic Symbol



Functional Diagram



ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-76165-5 (V_{CC} = 5.0V ± 5%, T_A = 0°C to +75°C)
HM-76165-2/-8 (V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V.
NOTE: Positive current defined as into device terminals.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/Enable "1" Input Current "0"	– –	– -50.0	+40 -100	μA μA	V_{IH} = V_{CC} Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0* –	1.5 1.5	– 0.8*	V V	V_{CC} = V_{CC} Min. V_{CC} = V_{CC} Max.
V_{OH} V_{OL}	Output "1" Voltage "0"	2.4 –	3.2 0.35	– 0.50	V V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min. I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0"	– –	– –	+40** -40	μA μA	V_{OH}, V_{CC} = V_{CC} Max. V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15	–	-100	mA	V_{OUT} = 0.0V, One Output at a Time for a Max. of 1 Second
I_{CC}	Power Supply Current	–	120	170	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.

* These are absolute voltages with respect to ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
** I_{OHE} = +60 μA for -2 and -8.

A.C. ELECTRICAL CHARACTERISTICS (Operating)

Typical Measurements are at T_A = +125°C, V_{CC} = +5V

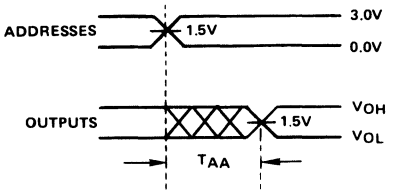
		HM-76165-5 5V ±5% 0°C to +75°C		HM-76165-2/-8 5V ±10% -55°C to +125°C		
SYMBOL	PARAMETER	TYPICAL	MAXIMUM	TYPICAL	MAXIMUM	UNITS
T_{AA}	Address Access Time	45	60	50	80	ns
T_{EA}	Chip Enable Access Time	25	35	30	40	ns
T_{DA}	Chip Disable Access Time	25	35	30	40	ns

A.C. limits guaranteed for worst case N^2 sequencing with maximum test frequency of 5MHz.

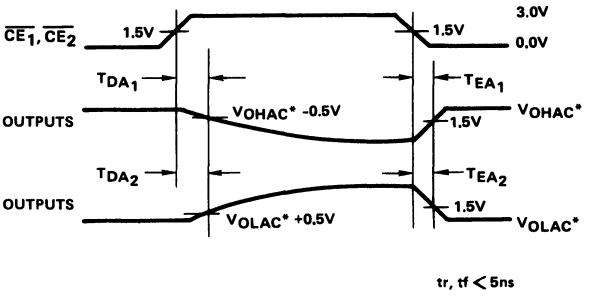
CAPACITANCE: T_A = 25°C

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
CINA, CINCE	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
COUT	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

HM-76165 SWITCHING TIME DEFINITIONS



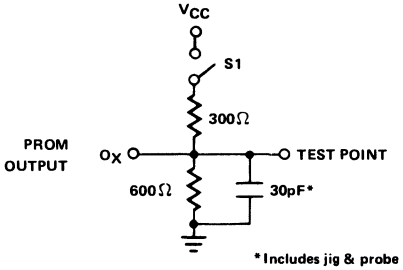
NOTE: As is common to all memory devices, output levels can be undefined during the address access period (T_{AA}); however, the outputs are guaranteed to reach stable levels by T_{AA}. It is not recommended that outputs from this class of devices be used to drive edge triggered inputs on subsequent devices (counters, flip-flops, etc.) without proper intermediate synchronization.



tr, tf < 5ns

*V_{OLAC} AND V_{OHAC} ARE THE MEASURED OUTPUT VOLTAGE LEVELS WHILE ENABLED.

A.C. TEST LOAD



*Includes jig & probe total capacitance

This is the A.C. Test Load which Harris Semiconductor uses in its automatic test equipment, and it is recommended that users of Harris bipolar devices use the same or an equivalent load in performing A.C. testing.

SYMBOL	PARAMETER	S1
T_{AA}	Address Access Time	Closed
T_{EA_1}	Chip Enable Access Time from "Three State" to V_{OH}	Open
T_{EA_2}	Chip Enable Access Time from "Three State" to V_{OL}	Closed
T_{DA_1}	Chip Disable Access Time from V_{OH} to "Three State"	Open
T_{DA_2}	Chip Disable Access Time from V_{OL} to "Three State"	Closed

HARRIS

HM-76321

4K x 8 PROM

Features

- 65ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OUTPUTS AND TWO CHIP ENABLE CONTROLS
- SIMPLE HIGH SPEED PROGRAMMING - ONE PULSE/BIT TYPICAL
- FAST ACCESS TIME - GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE
- PRODUCED ON MIL-M-38510 QUALIFIED WAFER FAB LINE
- INDUSTRY STANDARD 24 PIN PACKAGE

Description

The HM-76321 is a fully decoded Schottky TTL 32,768 bit field programmable ROM in a 4K word by 8 bit/word format with "Three State" outputs. This PROM is available in a 24 pin DIP.

All bits are manufactured storing a logical "1" (Positive Logic) and can be selectively programmed for a logical "0" in any bit position.

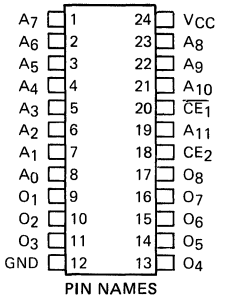
MIL-M-38510 qualified NiCr technology is used on the HM-76321 and all other HARRIS Bipolar PROMs.

The HM-76321 contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametrics and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

The HM-76321 utilizes two chip enable controls, where $\overline{CE_1}$ low and CE_2 high enables the device.

Pinout

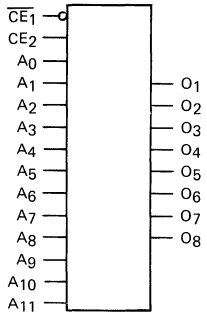
TOP VIEW – DIP



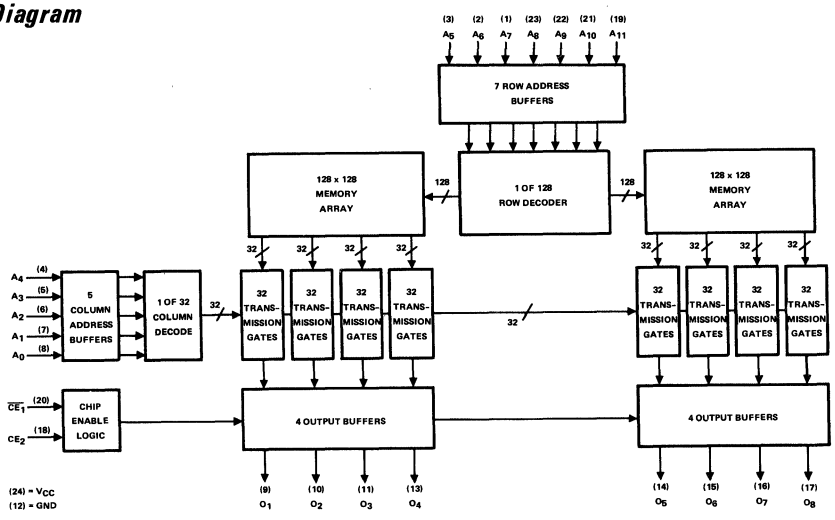
PIN NAMES

$A_0 - A_{11}$	Address Inputs
$O_1 - O_8$	Data Outputs
$\overline{CE_1}, CE_2$	Chip Enable Inputs

Logic Symbol



Functional Diagram



ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-76321-5 (V_{CC} = 5.0V ± 5%, T_A = 0°C to +75°C)
HM-76321-2/-8 (V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V.
NOTE: Positive current defined as into device terminals.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH}	Address/Enable "1"	–	–	+40	μA	V_{IH} = V_{CC} Max.
I_{IL}	Input Current "0"	–	-50.0	-100	μA	V_{IL} = 0.45V
V_{IH}	Input Threshold "1"	2.0*	1.5	–	V	V_{CC} = V_{CC} Min.
V_{IL}	Voltage "0"	–	1.5	0.8*	V	V_{CC} = V_{CC} Max.
V_{OH}	Output "1"	2.4	3.2	–	V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min.
V_{OL}	Voltage "0"	–	0.35	0.50	V	I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE}	Output Disable "1"	–	–	+40**	μA	V_{OH}, V_{CC} = V_{CC} Max.
I_{OLE}	Current "0"	–	–	-40	μA	V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15	–	-100	mA	V_{OUT} = 0.0V, One Output at a Time for a Max. of 1 Second
I_{CC}	Power Supply Current	–	–	190	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.

* These are absolute voltages with respect to ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
** I_{OHE} = +100 μA for -2 and -8.

A.C. ELECTRICAL CHARACTERISTICS (Operating)

Typical measurements are at T_A = +25°C, V_{CC} = +5V

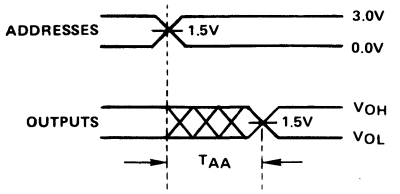
		HM-76321-5 5V ±5% 0°C to +75°C		HM-76321-2/-8 5V ±10% -55°C to +125°C		
SYMBOL	PARAMETER	TYPICAL	MAXIMUM	TYPICAL	MAXIMUM	UNITS
T_{AA}	Address Access Time	45	65	–	85	ns
T_{EA}	Chip Enable Access Time	25	35	–	40	ns
T_{DA}	Chip Disable Access Time	25	35	–	40	ns

A.C. limits guaranteed for worst case N^2 sequencing with maximum test frequency of 5MHz.

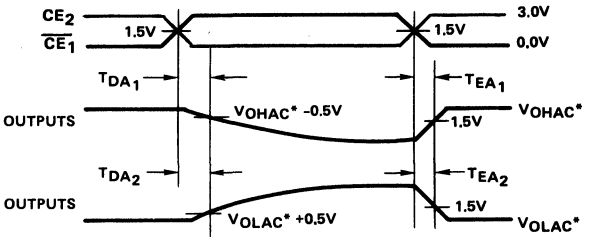
CAPACITANCE: T_A = 25°C

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

HM-76321 SWITCHING TIME DEFINITIONS



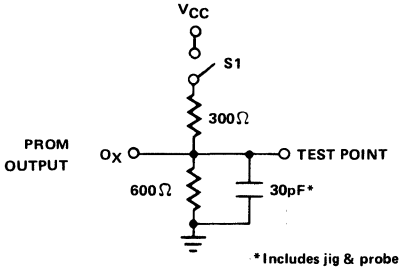
NOTE: As is common to all memory devices, output levels can be undefined during the address access period (T_{AA}); however, the outputs are guaranteed to reach stable levels by T_{AA}. It is not recommended that outputs from this class of devices be used to drive edge triggered inputs on subsequent devices (counters, flip-flops, etc.) without proper intermediate synchronization.



tr, tf < 5ns

*VOLAC AND VOHAC ARE THE MEASURED OUTPUT VOLTAGE LEVELS WHILE ENABLED.

A.C. TEST LOAD



SYMBOL	PARAMETER	S1
T_{AA}	Address Access Time	Closed
T_{EA_1}	Chip Enable Access Time from "Three State" to V_{OH}	Open
T_{EA_2}	Chip Enable Access Time from "Three State" to V_{OL}	Closed
T_{DA_1}	Chip Disable Access Time from V_{OH} to "Three State"	Open
T_{DA_2}	Chip Disable Access Time from V_{OL} to "Three State"	Closed

HARRIS

HM-76641

8K x 8 PROM

Features

- 85ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OUTPUTS
- ACTIVE LOW CHIP ENABLE CONTROL
- HIGHEST DENSITY AVAILABLE IN THE INDUSTRY
- FOUR FOLD INCREASE IN DENSITY OVER CURRENTLY AVAILABLE 16K PROMs WITH 1/4 POWER DISSIPATION PER BIT
- INDUSTRY STANDARD 24 PIN PACKAGE
- SIMPLE HIGH SPEED PROGRAMMING - ONE PULSE/BIT TYPICAL
- FAST ACCESS TIME - GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE
- PRODUCED ON MIL-M-38510 QUALIFIED WAFER FAB LINE

Description

The HM-76641 is a fully decoded Schottky TTL 65,536 bit field programmable ROM in an 8K word by 8 bit/word format with "Three State" outputs. This PROM is available in a 24 pin DIP.

All bits are manufactured storing a logical "1" (Positive Logic) and can be selectively programmed for a logical "0" in any bit position.

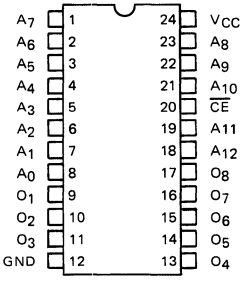
MIL-M-38510 qualified NiCr technology is used on the HM-76641 and all other HARRIS bipolar PROMs.

The HM-76641 contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametrics and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

The HM-76641 utilizes a single chip enable, $\overline{CE}$, which when low enables the device.

Pinout

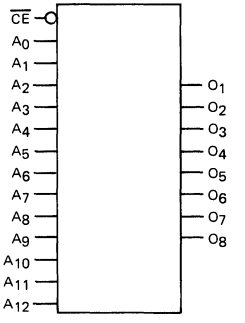
TOP VIEW – DIP



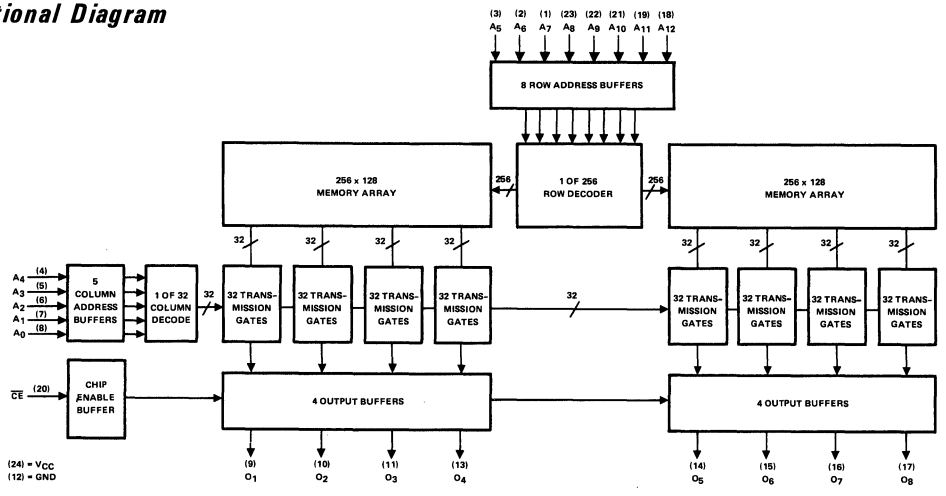
PIN NAMES

$A_0 - A_{12}$	Address Inputs
$O_1 - O_8$	Data Outputs
$\overline{CE}$	Chip Enable Inputs

Logic Symbol



Functional Diagram



ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-76641-5 (V_{CC} = 5.0V ± 5%, T_A = 0°C to +75°C)
HM-76641-2/-8 (V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V.
NOTE: Positive current defined as into device terminals.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH}	Address/Enable "1"	–	–	+40	μA	V_{IH} = V_{CC} Max.
I_{IL}	Input Current "0"	–	-50.0	-100	μA	V_{IL} = 0.45V
V_{IH}	Input Threshold "1"	2.0*	1.5	–	V	V_{CC} = V_{CC} Min.
V_{IL}	Voltage "0"	–	1.5	0.8*	V	V_{CC} = V_{CC} Max.
V_{OH}	Output "1"	2.4	3.2	–	V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min.
V_{OL}	Voltage "0"	–	0.35	0.50	V	I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE}	Output Disable "1"	–	–	+40**	μA	V_{OH}, V_{CC} = V_{CC} Max.
I_{OLE}	Current "0"	–	–	-40	μA	V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15	–	-100	mA	V_{OUT} = 0.0V, One Output at a Time for a Max. of 1 Second
I_{CC}	Power Supply Current	–	–	190	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.

* These are absolute voltages with respect to ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
** I_{OHE} = +100 μA for -2 and -8.

A.C. ELECTRICAL CHARACTERISTICS (Operating)

Typical Measurements are at T_A = +25°C, V_{CC} = +5V

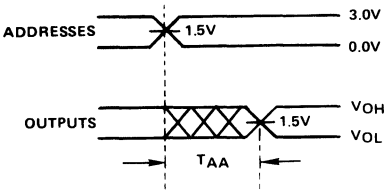
		HM-76641-5 5V ±5% 0°C to +75°C		HM-76641-2/-8 5V ±10% -55°C to +125°C		
SYMBOL	PARAMETER	TYPICAL	MAXIMUM	TYPICAL	MAXIMUM	UNITS
T_{AA}	Address Access Time	50	85	–	100	ns
T_{EA}	Chip Enable Access Time	30	40	–	45	ns
T_{DA}	Chip Disable Access Time	30	40	–	45	ns

A.C. limits guaranteed for worst case N^2 sequencing with maximum test frequency of 5MHz.

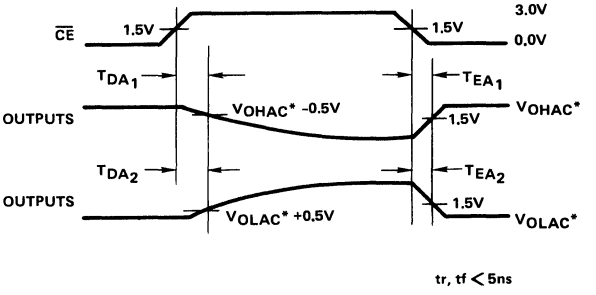
CAPACITANCE: T_A = 25°C

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

HM-76641 SWITCHING TIME DEFINITIONS



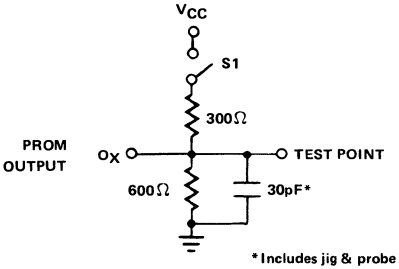
NOTE: As is common to all memory devices, output levels can be undefined during the address access period (T_{AA}); however, the outputs are guaranteed to reach stable levels by T_{AA}. It is not recommended that outputs from this class of devices be used to drive edge triggered inputs on subsequent devices (counters, flip-flops, etc.) without proper intermediate synchronization.



tr, tf < 5ns

*V_{OLAC} AND V_{OHAC} ARE THE MEASURED OUTPUT VOLTAGE LEVELS WHILE ENABLED.

A.C. TEST LOAD



*Includes jig & probe total capacitance

This is the A.C. Test Load which Harris Semiconductor uses in its automatic test equipment, and it is recommended that users of Harris bipolar devices use the same or an equivalent load in performing A.C. testing.

SYMBOL	PARAMETER	S1
T_{AA}	Address Access Time	Closed
T_{EA_1}	Chip Enable Access Time from "Three State" to V_{OH}	Open
T_{EA_2}	Chip Enable Access Time from "Three State" to V_{OL}	Closed
T_{DA_1}	Chip Disable Access Time from V_{OH} to "Three State"	Open
T_{DA_2}	Chip Disable Access Time from V_{OL} to "Three State"	Closed

HARRIS

HM-76641A

8K x 8 PROM

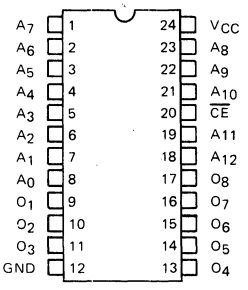
Preview

Features

- 50ns MAXIMUM ADDRESS ACCESS TIME (0°C TO +75°C)
- "THREE STATE" OUTPUTS
- ACTIVE LOW CHIP ENABLE CONTROL
- HIGHEST DENSITY AVAILABLE IN THE INDUSTRY
- FOUR FOLD INCREASE IN DENSITY OVER CURRENTLY AVAILABLE 16K PROMs WITH 1/4 POWER DISSIPATION PER BIT
- INDUSTRY STANDARD 24 PIN PACKAGE
- SIMPLE HIGH SPEED PROGRAMMING - ONE PULSE/BIT TYPICAL
- FAST ACCESS TIME - GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE

Pinout

TOP VIEW – DIP



PIN NAMES

$A_0 - A_{12}$	Address Inputs
$O_1 - O_8$	Data Outputs
$\overline{CE}$	Chip Enable Inputs

Description

The HM-76641 is a fully decoded Schottky TTL 65,536 bit field programmable ROM in an 8K word by 8 bit/word format with "Three State" outputs. This PROM is available in a 24 pin DIP.

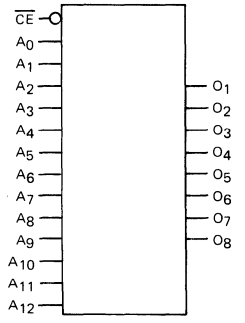
All bits are manufactured storing a logical "1" (Positive Logic) and can be selectively programmed for a logical "0" in any bit position.

MIL-M-38510 qualified NiCr technology is used on the HM-76641 and all other HARRIS bipolar PROMs.

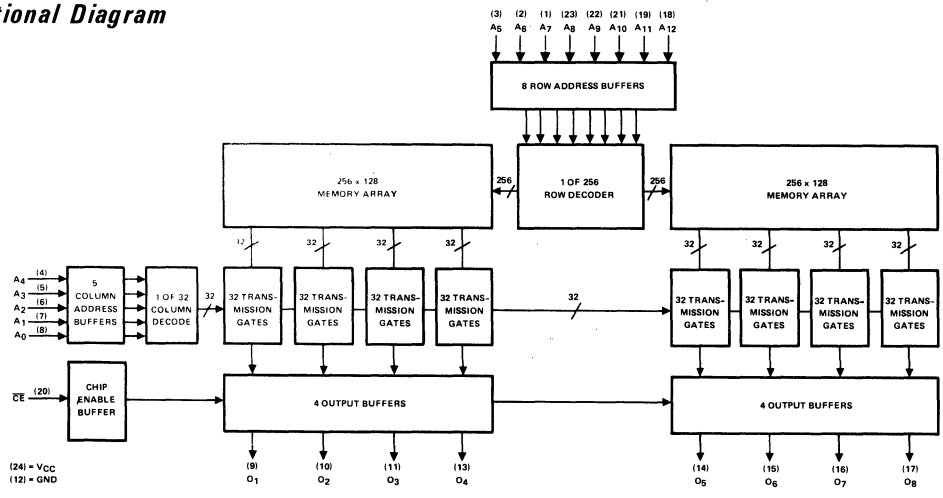
The HM-76641 contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametrics and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

The HM-76641 utilizes a single chip enable, $\overline{CE}$, which when low enables the device.

Logic Symbol



Functional Diagram



JAN-0512

512 BIT, BIPOLAR PROM
MIL/M38510/20101

Features

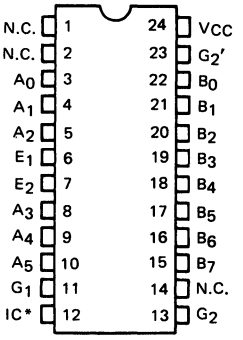
- FIELD PROGRAMMABLE
- 64 WORDS/8 BITS PER WORD
- FULLY DECODED
- DTL/TTL COMPATIBLE
- 140ns ACCESS TIME

Description

The JAN-0512 is a field programmable 64 word by 8 bit PROM. In an unprogrammed memory, all "Memory Elements" are short circuits so that logical "zeros" appear at each output bit position for any address input. "Electronic Programming" involves the alteration of specific "Memory Elements" to create logical "ones" in selected bit positions. This alteration is irreversible and cannot be accomplished under normal operating conditions.

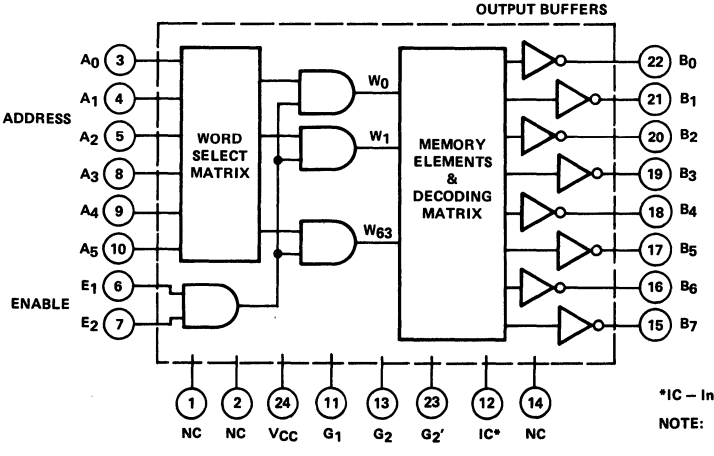
Pinout

TOP VIEW – D.I.P.



*Must be left open circuit

Block Diagram



*IC – Internal Connection must be left open

NOTE: For operational condition, return pins 11, 13, and 23 to system ground.

4 BIPOLAR MEMORY

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range	-0.5 V_{DC} to 7.0 V_{DC}
Input Voltage Range	-1.5 V_{DC} at -12mA to 5.5V_{DC}
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering 10 Seconds)	300°C
Thermal Resistance, Junction-to-Case	JC' Case J = 30°C/w
Output Supply Voltage	-0.5V_{DC} to 7.0V_{DC}
Output Sink Current	+30mA
Maximum Power Dissipation, P_D	575mWdc
Maximum Junction Temperature, T_J	175°C

RECOMMENDED OPERATING CONDITIONS

Supply Voltage	4.75 V_{DC} Min. to 5.25V_{DC} Maximum
Minimum High Level Input Voltage	2.0V_{DC}
Maximum Low Level Input Voltage	0.8V_{DC}
Normalized Fanout (Each Output)	6 Maximum (10mA)
Ambient Operating Temperature Range	-55°C to +125°C

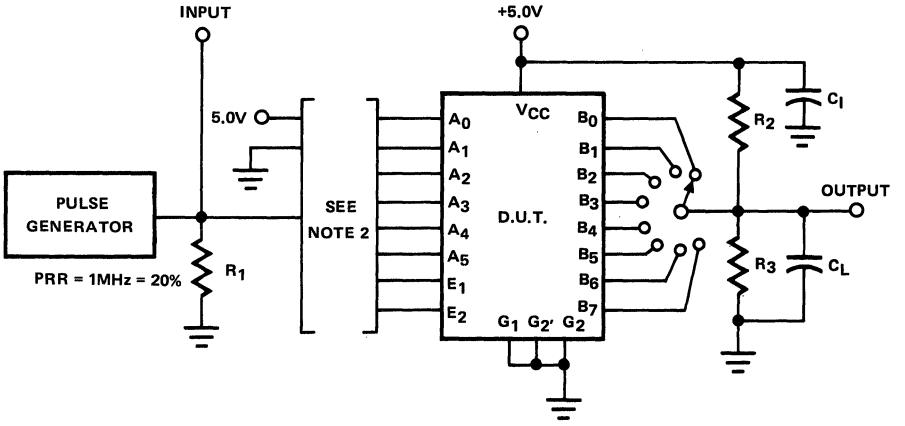
ELECTRICAL CHARACTERISTICS

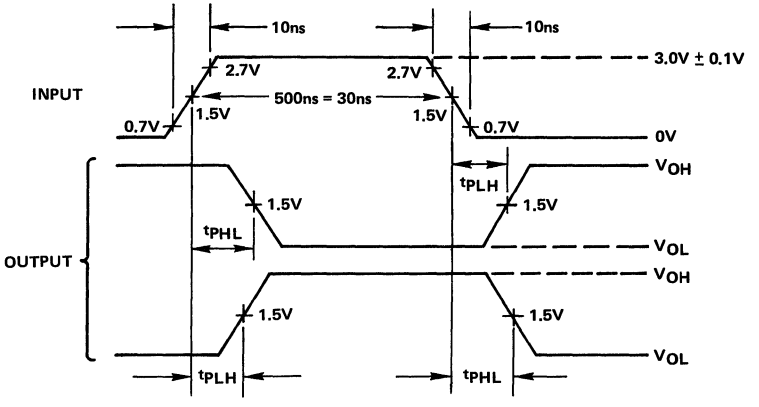
The electrical characteristics are as specified in the table and apply over the full recommended ambient operating temperature range, unless otherwise specified.

SYMBOL	TEST	LIMITS MIN	LIMITS MAX	UNITS	TEST CONDITIONS
V_{OL}	Low Level Output Voltage		0.45	Volts	V_{CC} = 4.75V V_{IN} = 2.0V I_{OL} = 10mA
V_{IC}	Input Clamp Voltage		-1.5	Volts	V_{CC} = 4.75V I_{IN} = -12mA T_A = 25°C
I_{CEX1}	Maximum Collector Cut-Off Current		100	μA	V_{CC} = 5.25V V_{OH} = 2.8V V_{IN} = 0.8V
I_{CEX2}			200	μA	V_{CC} = 5.25V V_{OH} = 5.25V V_{IN} = 0.8V
I_{IH1}	High Level Input Current		60	μA	V_{CC} = 5.25V V_{IN} = 2.4V;
I_{IH2}			100	μA	V_{CC} = 5.25V V_{IN} = 5.25; ①
I_{IL}	Low Level Input Current	-0.2	-1.6	mA	V_{CC} = 5.25V V_{IN} = 0.4V; ②
I_{CC}	Supply Current		100	mA	V_{CC} = 5.25V V_{IN} = 0
t_{PHL}	Propagation Delay Time High-to-Low Level Logic	85	140	ns	V_{CC} = 5.0V C_L = 30pF Min. R_1 = 470 Ω ±5%
t_{PLH}	Propagation Delay Time Low-to-High Level Logic	85	140	ns	

NOTES: 1. When testing one E input, apply 5.25V to the other.
2. When testing one E input, apply GND to the other.

Switching Time Test Circuits



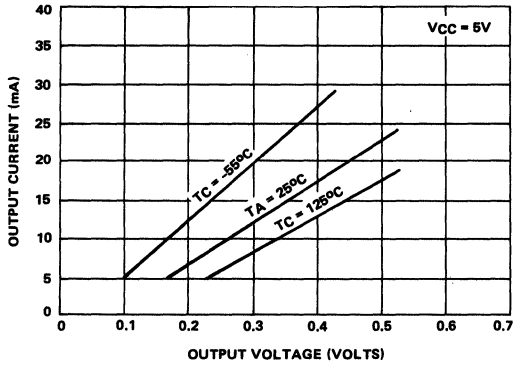


NOTES:

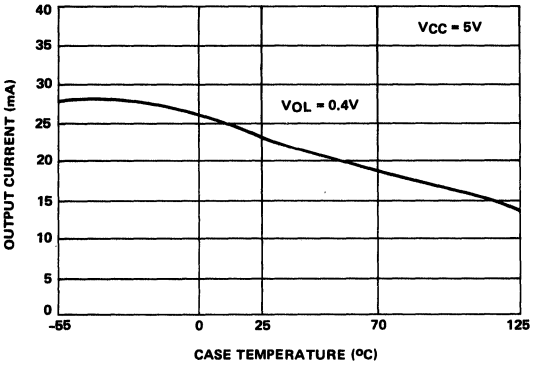
1. Pins 12 and 14 shall be left open.
2. The applicable test table should be selected from the altered item drawing.
3. $C_1 = 0.5\mu F \pm 10\%$; $R_1 = 50\Omega \pm 5\%$; $R_2 = 470\Omega \pm 5\%$; $R_3 = 1k\Omega \pm 5\%$; $C_L = 30pF$ including jig and probe capacitance.

Characteristic Curves

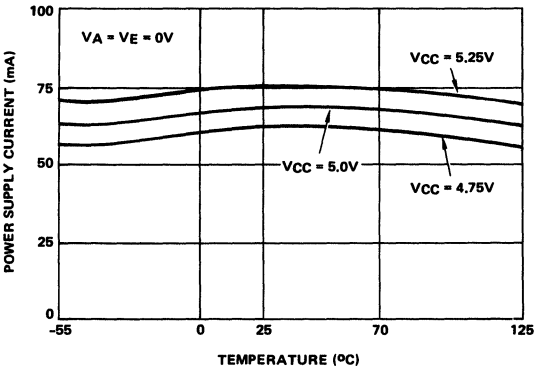
OUTPUT CHARACTERISTICS



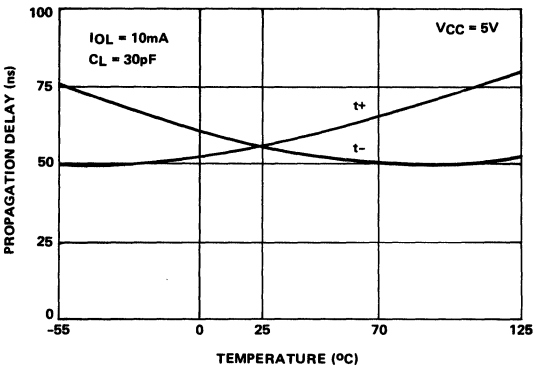
OUTPUT CURRENT vs. TEMPERATURE



POWER SUPPLY CURRENT vs. TEMPERATURE



PROPAGATION DELAY vs. TEMPERATURE



PROGRAMMING SPECIFICATIONS

PARAMETER	VALUE
Address Input Voltage	
High Logic Level	Open Circuit ①
Low Logic Level	-5.0V
Power Supply Voltage	+5.0V +5%, -0%
G1 Voltage ②	-5.0V
G2 Voltage	0V
G2' Voltage	
For Device Type 01 Circuit A	Open
Maximum Programming Voltage	-7.0V
Maximum Programming Current	100mA
Maximum Number or Attempts to Program a Given Bit	2
Maximum Case Temperature During Programming	75°C

1. Open collector TTL gates meet this requirement.
2. G1 must be connected to -5.0V prior to applying V_{CC} or programming voltage.

PROGRAMMING PROCEDURES

Using the test conditions of the table, the following procedures shall be used for programming the device:

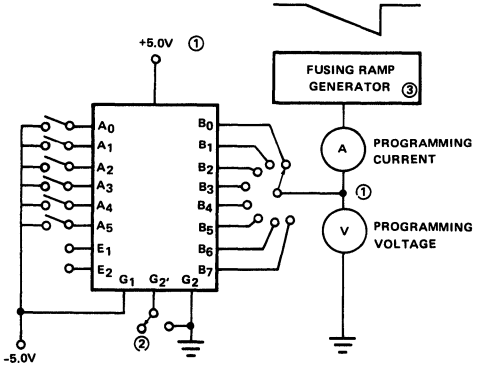
(a) Connect the device as shown in Figure 1, using the fusing generator of Figure 1 or the alternate circuit of Figure 2. The circuit shown in Figure 2 can be used in more automated programming systems. This circuit generates a current pulse which is at the proper voltage and current levels for fast reliable programming. The input programming pulse width shall be 750ms ±50ms. The number of attempts to program a given bit shall be as specified in the table.

(b) To address a particular word in the memory, set the input switches to the binary equivalent of that word, where a logical low level is -5.0V and a logical high level is an open circuit. (Do not return to supply). All output bits (B_0, B_1, . . . B_7) of this word are available for programming.

(c) With the output current limited (as specified in the table), apply a negative going current pulse to the pin associated with the first bit to be changed from a logical low level to a logical high level. This is most easily accomplished by connecting the negative terminal of a variable power supply to the proper output pin and manually increasing the voltage to approximately 6.0V.

(d) Skipping any bit which is to remain a logical low level, repeat step (c) for each logical low level in the word being addressed. Not more than one bit shall be programmed at a time.

(e) Set the next input address and repeat steps (c) and (d). This procedure is repeated for each input address for which a specific output word pattern is desired. Note that all addresses do not have to be programmed at the same time, nor do all output bits for a given address. A logical low level can always be changed to a logical high level, simply by repeating steps (b) and (c). A logical low level, once programmed to a logical high level, cannot be reprogrammed.



NOTES:
1. Connect -5.0V to G1 before applying VCC or programming voltage.
2. For device type 01, G2' shall be open.
3. Generator characterisitics are defined in Programming Procedures.

FIGURE 1
PROGRAMMING CONNECTIONS

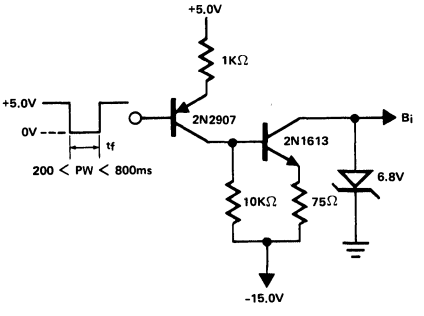


FIGURE 2
PROGRAMMING CIRCUIT

Generic PROM Programming

All 76xxx series devices utilize the same programming method which is one of the characteristics that lends to the term "Generic" PROM.

Harris Generic PROMs have the industry's highest programming yield and exhibit an extremely high level of reliability in the field; however, this level of device quality can only be obtained if the PROM has been properly programmed to the data sheet specifications. Outlined below are the key points which deserve attention to assure that programming has been optimally performed.

- Be certain that you are following the latest revision status of programming specifications.
- If you are utilizing a commercial programmer, be sure that the module for Harris Generic PROMs is certified for the most recent revision level.
- Have the Programmer calibrated at routine intervals to assure that the electrical and mechanical characteristics are acceptable. This would include such things as:
  - ► Making certain that the socket which the device is placed into is clean, free of corrosion and is mechanically sound.
  - ► Check ribbon cable connectors for good continuity.
  - ► Making sure that all voltage levels conform to the programming specifications.
  - ► Assuring that all pulses are clean of distortion and exhibit the correct timing characteristics.
- The typical programming failure mode of Harris Generic PROMs should be underprogrammed (won't blow a fuse or fuses). This is usually due to the pyrotechnic nature of PROMs. You won't know for sure whether any given fuse will program until you try. Overprogramming (undesired fuses program) is an extremly low incidence problem, and any measurable percentage of overprogramming is a glaring indication of programming equipment malfunction. PROMs that fail at the same location also indicates a problem with the programmer as untestable flaws in PROMs are random in nature.

If there is any problem in determining how to follow any of the guidelines, contact a local Harris office for assistance.

PROGRAMMING PROCEDURE

The following is a generic programming procedure which is used for all Harris Generic 76xxx PROMs.

The HM-76xxx PROMs are manufactured with all bits storing a logical "1" (output high). Any desired bit can be programmed to a logical "0" (output low) by following the simple procedure shown below. One may build his own programmer to satisfy the specifications described in the table, or use any of the commercially available programmers which meet these specifications. These PROMs can be programmed automatically or by the manual procedure shown on the next page.

Programming the HM-76xxx PROMs

The HM-76xxx PROMs are manufactured with all bits storing a logical "1" (output high). Any desired bit can be programmed to a logical "0" (output low) by following the simple procedure shown below. One may build his own programmer to satisfy the specifications described in the table, or use any of the commercially available programmers which can meet these specifications.

PROGRAMMING SPECIFICATIONS

SYMBOL	PARAMETER	MINIMUM	RECOMMENDED OR TYPICAL	MAXIMUM	UNITS
V_{IH} V_{IL}	Address Input Voltage (1)	2.4 0.0	5.0 0.4	5.0 0.5	V V
V_{PH} (2) V_{PL} (3)	Programming/Verify Voltage to V_{CC}	12.0 4.5	12.0 4.5	12.5 5.5	V V
I_{ILP}	Programming Input Low Current at V_{PH}	–	-300	-600	μA
t_r t_f	Programming (V_{CC}) Voltage Rise and Fall Time	1.0 1.0	1.0 1.0	10.0 10.0	μs μs
t_d	Programming Delay	10	10	100	μs
t_p	Programming Pulse Width (4)	90	100	110	us
P.D.C.	Programming Duty Cycle (5)	–	50	60	%
V_{OPE} V_{OPD}	Output Voltage Enable (6) Output Voltage Disable	10.5 0.0	10.5 5.0	11.0 5.5	V V
T_a	Ambient Temperature	–	25	30	°C

During programming the chip must be disabled for proper operation.

NOTES:
1. No inputs should be left open for V_{IH}.
2. V_{PH} source must be capable of supplying one ampere.
3. It is recommended that dual verification be made at V_{PL} min and V_{PL} max.
4. Note step 9 in programming procedure.
5. Programming Duty Cycle applies to DIPs only.
6. V_{OPE} source must be capable of supplying 10mA minimum.

PROGRAMMING PROCEDURE

1. Address the PROM with the binary address of the word to be programmed. Address inputs are TTL compatible. An open circuit should not be used to address the PROM.

2. Bring the $\overline{CE}_X$ input(s) high and the CE_X input(s) low to disable the device. The disabling of the device during programming is an essential step in correctly programming all HARRIS PROMs. The chip enables are TTL compatible. An open circuit should not be used to disable the device.

3. Disable the programming circuitry by applying a voltage of V_{OPD} to the outputs of the PROM.

4. Raise V_{CC} to V_{PH} with rise time less than or equal to t_r.

5. After a delay equal to or greater than t_d apply a pulse with amplitude of V_{OPE} and duration of t_p to the output selected for programming. Note that the PROM is supplied with fuses intact, which generates an output high. Programming a fuse will cause the output to go low.

6. Other bits in the same word may be programmed while the V_{CC} input is raised to V_{PH} by applying output enable pulses to each output which is to be programmed. The output enable pulses must be separated by a minimum interval of t_d.

7. Lower V_{CC} to 4.5 volts following a delay of t_d from last programming enable pulse applied to an output.

8. Enable the PROM for verification by applying V_{IL} to $\overline{CE}_X$ and V_{IH} to CE_X.

9. Repeat verification (step 8) at V_{CC} = 5.5 volts.

10. If any bit does not verify as programmed, repeat steps 2 through 9 until the bit has received a total of 1ms of programming time. Bits which do not program within 1ms are programming rejects. No further attempt to program these parts should be made.

11. Repeat steps 1 through 10 for all other bits to be programmed in the PROM.

12. Programming rejects returned to the factory must be accompanied by data giving address, desired data, and actual output data of the location in which a programming failure has occurred.

TYPICAL PROGRAMMING CIRCUIT

The circuit and timing diagrams shown in Figures 1 and 2 will establish the proper programming conditions for the output enable pulses. This allows the use of standard TTL parts for all logic inputs to the PROM. Note the gate which senses the output must withstand inputs up to 11.0 volts during programming.

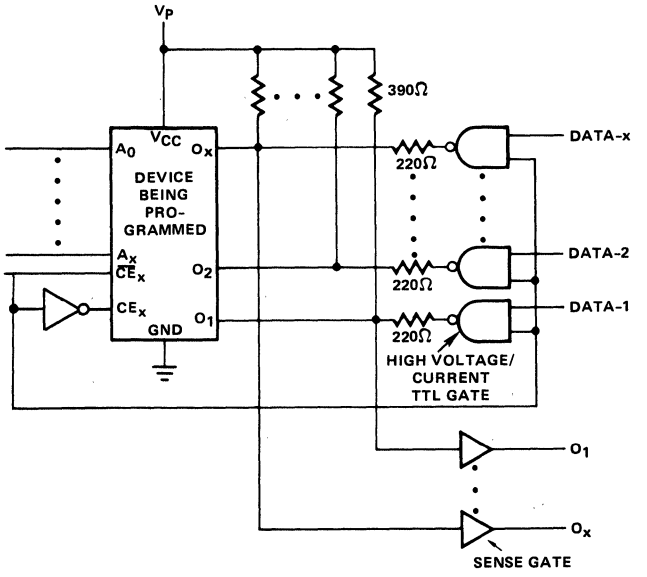


FIGURE 1

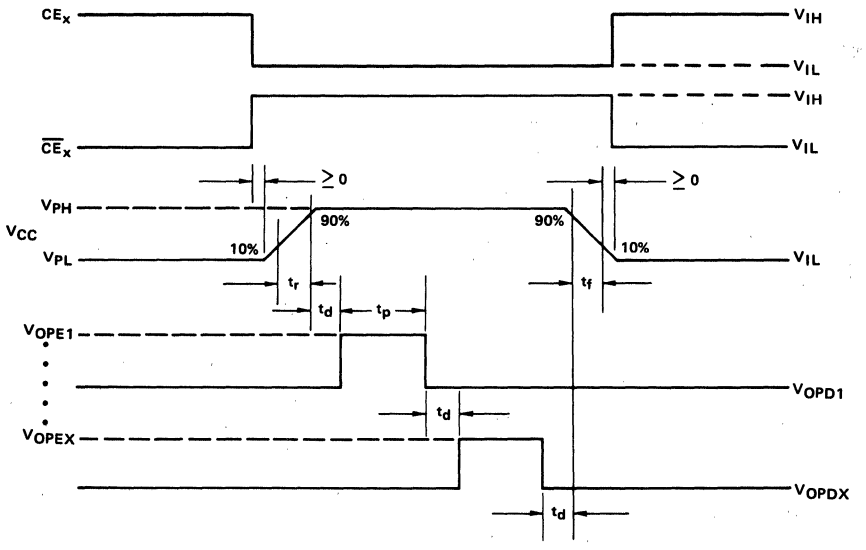


FIGURE 2

Waveforms Applied to the Device Pins During Programming

Programmer Evaluation

Programmer equipment manufacturers identified in the accompanying list have previously produced equipment determined to be capable of properly programming Harris Semiconductor PROMs. This list is provided only as a convenience to purchasers of HARRIS PROMs to identify programmer manufacturers potentially suitable for programming the PROMs. It is neither intended to be a representation or warranty by Harris of the capability of all listed manufacturers models nor an indication of unsuitability of other manufacturers not contained in the list. PROM purchasers are advised to adhere to the programming requirements specified in HARRIS current data sheets applicable to the PROMs to be programmed and to the programming equipment manufacturer's specifications. Responsibility for programming equipment performance lies solely with the equipment manufacturer. The programmer user is cautioned to verify operation and performance according to the manufacturer's instructions and specifications prior to each use, and to determine that the programming complies with the applicable HARRIS PROM data sheet. Harris accepts no responsibility for PROMs which have been subjected to incorrect or faulty programming.

PROM Programmer Manufacturers

DIGILEC USA
Suite 103
7335 E. Acoma Dr.
Scottsdale, AZ 85260
Phone: 602-991-7268

INTERNATIONAL
MICROSYSTEMS, INC.
11554 C Avenue
Auburn, CA 95603
Phone: 916-885-7262

KONTRON
ELECTRONICS
630 Price Avenue
Redwood City, CA 94063
Phone: 415-361-1012

PRO-LOG
2411A Garden Rd.
Monterey, CA 93940
Phone: 408-372-4593

STAG
MICROSYSTEMS, INC.
528-5 Weddell Drive
Sunnyvale, CA 94086
Phone: 408-745-1991

SUNRISE ELECTRONICS
524 South Vermont Avenue
Glendora, CA 91740
Phone: 213-963-8775

DATA I/O
10525 Willows Road N.E.
C46
Redmond, WA 98052
Phone: 206-881-6444

STOLZ AG
Tafernstrasse 15
5405 Braden-Dattwil
Switzerland
Phone: 056840151

NOTE: Programmer manufacturers are changing from modules or card sets to a universal type of programming system. Contact the programmer manufacturer for their latest updates of hardware and software.

Data Entry Formats for Harris Custom Programming*

For Harris to custom program to a user data pattern specification, the user must supply the data in one of the following formats:

1. Master PROM of same organization and pinout as device ordered. Two pieces required, three preferred.
2. Paper tape in Binary or ASCII BPNF.

* BINARY PAPER TAPE FORMAT

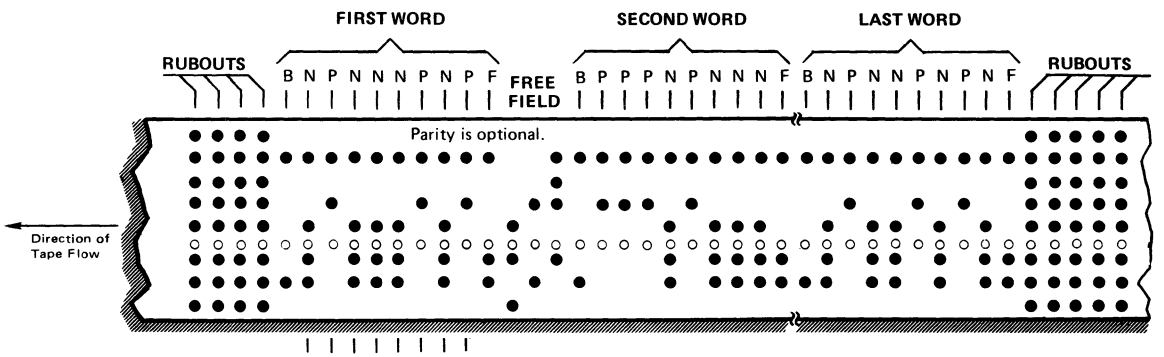
- A minimum of six inches of leader.
- A rubout (all eight locations punched).
- Data words beginning with the first word (word "0"), proceeding sequentially, ending with the last word (word "N"), with no interruptions or extraneous characters of any kind.
- Specify whether a punched hole is a VOH = "1" = logic high or is a VOL = "0" = logic low.
- A minimum trailer of six inches of tape.

* ASCII BPNF FORMAT

- A minimum leader of twenty rubouts (all eight locations punched).
- Any characters desired (none necessary) except "B".
- Data words beginning with the first word (word "0"), proceeding sequentially, ending with the last word (word "N").
- Data words consist of:
    1. The character "B" denoting the beginning of a data word.
    2. A sequence of characters, only "P" or "N", one character for each bit in the word.
    3. The character "F" denoting the finish of the data word.
- No extraneous characters of any kind may appear within a data word (between any "B" and the next "F").
- Errors may be deleted by rubouts superimposed over the entire word including the "B", and beginning the word again with a new "B".
- Any text of any kind (except the character "B") is allowed between data words (between any "F" and the next "B"), including carriage return and line feed.
- A minimum trailer of twenty-five rubouts.
- Specify whether a "P" is a "1" = VOH = logic high or is a "0" = VOL = logic low.
- The use of even or odd parity is optional.

* *Harris can not assume responsibility for PROMs programmed to data tapes or masters which contain errors. The user must insure the accuracy of the data provided to Harris. Harris guarantees that the programmed PROMs will contain the information provided if either of the following formats are followed.*

ASCII BPNF PAPER TAPE EXAMPLE



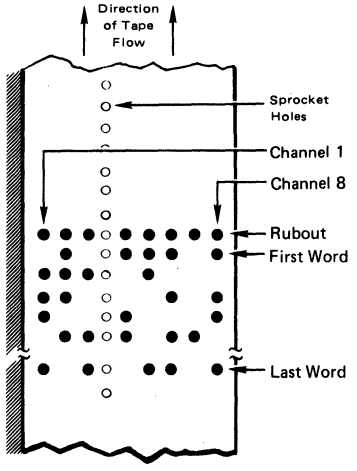
EXAMPLE	PACKAGE TYPE	DEVICE OUTPUT PINS
HM-7611	16 Pin Pkg.	12 11 10 9
HM-7649	20 Pin Pkg.	14 13 1211 9 8 7 6

Truth Table
Character "D" = "1" = VOH = Logic High
Character "V" = "0" = VOL = Logic Low

Word				PROM Outputs Data ①							
AX ···· A2	A1	A0		O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1
0 ····· 0	0	0	First	0	1	0	0	0	1	0	1
0 ····· 0	0	1	Second	1	1	1	0	1	0	0	0
1 ····· 0	1	0	Last	0	1	0	0	1	0	1	0

NOTES:
① In the ASCII BPNF format, MSB data is punched after "B". On devices with 8 outputs, O_8 (Output 8) data is punched after "B". On devices with 4 outputs, O_4 (Output 4) data is punched after "B"

BINARY PAPER TAPE EXAMPLE



Punched Hole = "0" = VOL = Logic Low

Word					PROM Output Data ①							
AX ··· A2	A1	A0		Channel Output	8 O_8	7 O_7	6 O_6	5 O_5	4 O_4	3 O_3	2 O_2	1 O_1
0 ···· 0	0	0	First		0	1	0	0	0	1	0	1
0 ···· 0	0	1	Second		1	1	1	0	1	0	0	0
0 ···· 0	1	0	Third		0	1	0	1	1	1	0	0
0 ···· 0	1	1	Fourth		0	1	1	1	0	1	1	0
0 ···· 1	0	0	Fifth		1	0	0	1	0	0	0	1
1 ···· 1	1	1	Last		0	1	0	0	1	0	1	0

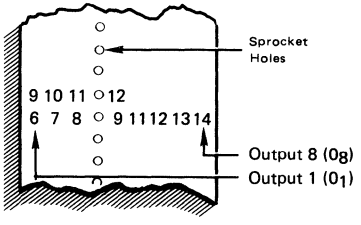
NOTES:

① PROMs with 4 bit wide data outputs require punching only first 4 channels on tape (Channels 1 thru 4).

② On HARRIS PROMs O_X (Example: O_1) designates a respective output pin on the device. O_1 (Output 1) is always LSB.

DEVICE OUTPUT PACKAGE PINS

EXAMPLE:



Package	Device Type
16-Pin	HM-7611
20-Pin	HM-7649

BIPOLAR

Harris Programmable Logic

5

PART NUMBER	ARRAY INPUTS	MATRIX ARCHITECTURE	LOGIC	OUTPUT ENABLE	OUTPUTS	PROPAGATION DELAY 0°C to +75°C	REGISTER SETUP TIME 0°C to +75°C	CLOCK TO OUTPUT TIME 0°C to +75°C	PAGE
HPL-77061	Twelve Dedicated Six Bidirectional	Programmable AND-Fixed OR	Ten 2-Wide AND-OR (Programmable Output Polarity)	Programmable	Six Bidirectional Four Dedicated	25 nsec	–	–	5-4
HPL-77153 /82S153	Eight Dedicated Ten Bidirectional	Programmable AND-Prog. OR	Ten 32-Wide AND-OR (Programmable Output Polarity)	Programmable	Ten Bidirectional	40 nsec	–	–	5-6
HPL-77209 /16L8	Ten Dedicated Six Bidirectional	Programmable AND-Fixed OR	Eight 7-Wide AND-OR-INVERT (Active Low Outputs)	Programmable	Six Bidirectional Two Dedicated	35 nsec	–	–	5-15
HPL-77210 /16R4	Eight Dedicated Four Feedback Four Bidirectional	Programmable AND-Fixed OR	Four 8-Wide AND-OR Four 7-Wide AND-OR-INVERT	Dedicated Programmable	Four Registered Four Bidirectional	35 nsec	35 nsec	25 nsec	5-42
HPL-77211 /16R6	Eight Dedicated Six Feedback Two Bidirectional	Programmable AND-Fixed OR	Six 8-Wide AND-OR Two 7-Wide AND-OR-INVERT	Dedicated Programmable	Six Registered Two Bidirectional	35 nsec	35 nsec	25 nsec	5-42
HPL-77212 /16R8	Eight Dedicated Eight Feedback	Programmable AND-Fixed OR	Eight 8-Wide AND-OR	Dedicated	Eight Registered	–	35 nsec	25 nsec	5-42
HPL-77215 /16H8	Ten Dedicated Six Bidirectional	Programmable AND-Fixed OR	Eight 7-Wide AND-OR (Active High Outputs)	Programmable	Six Bidirectional Two Dedicated	35 nsec	–	–	5-15
HPL-77216 /16P8	Ten Dedicated Six Bidirectional	Programmable AND-Fixed OR	Eight 7-Wide AND-OR (Programmable Output Polarity)	Programmable	Six Bidirectional Two Dedicated	35 nsec	–	–	5-15
HPL-77317 /16LD8	Ten Dedicated Six Feedback	Programmable AND-Fixed OR	Eight 8-Wide AND-OR-INVERT (Active Low Outputs)	–	Eight Dedicated	35 nsec	–	–	5-24
HPL-77318 /16HD8	Ten Dedicated Six Feedback	Programmable AND-Fixed OR	Eight 8-Wide AND-OR (Active High Outputs)	–	Eight Dedicated	35 nsec	–	–	5-24
HPL-77319 /16LE8	Ten Dedicated Six Fuse Selectable	Programmable AND-Fixed OR	Eight 8-Wide AND-OR-INVERT (Active Low Outputs)	Six Single-Fuse Programmable	Six Fuse Selectable Two Dedicated	35 nsec	–	–	5-33
HPL-77320 /16HE8	Ten Dedicated Six Fuse Selectable	Programmable AND-Fixed OR	Eight 8-Wide AND-OR (Active High Outputs)	Six Single-Fuse Programmable	Six Fuse Selectable Two Dedicated	35 nsec	–	–	5-33

NOTE: All HPL products are available in Ceramic and Plastic DIPs. Please see section 9 (Packaging) of this Data Book.

Harris Programmable Logic

Introduction

Harris Programmable Logic (HPL) is a family of user configurable logic elements designed to be space and power saving replacements for random logic designs implemented in TTL or LSTTL. HPL products are a natural progression for Harris Semiconductor, already a major PROM supplier with over ten years experience in the field of nickel-chromium fuse programmable devices. The HPL family contains devices which are functional and pinout replacements for existing industry standard devices, and also includes new devices with enhanced architectural features designed for applications which are not served by existing devices.

Family

The HPL family is divided into three architecturally distinct groups, each with its own advantages and areas of application. The three HPL groups are: IFL™, PAL® and PROM, and are all similar in that they contain two logic arrays. The first array is an AND array which is used to form PRODUCT terms from combinations of feedback and/or input variables. The second array is an OR array which is used to form SUM terms from combinations of product terms generated by the first array. The difference between the three architectural groups results from various combinations of user configurable and fixed arrays.

The PAL type devices have a programmable first array (AND) and a fixed second array (OR). The PROM type devices have this configuration reversed; they have a fixed first array (AND) and a programmable second array (OR).

The IFL™ architectural group is different again, with both its first (AND) and second (OR) logic arrays being programmable.The various combinations of fixed and programmable arrays are shown graphically in Figure 1 below. No one architectural group is the optimum solution for all designs, and for this reason Harris offers a wide range of devices to suit almost any design requirement.

Quality

One of the fundamental requirements for high quality is the ability to perform testing on unprogrammed devices as they are manufactured. It was only after the appearance on the market of early Programmable Array Logic devices that both manufacturers and users became aware of the inherent non-testability of those devices. The reasons for this difficulty is testing blank devices stemmed from architectural differences between programmable logic and programmable memory.

In a programmable memory device, such as a PROM, the same circuitry that is used at manufacture to verify the existence of fuses is used during the normal operation of the device. Therefore, if a PROM passes a fuse array verification test, then the logic paths from input to output are automatically tested for functionality. This simplicity of testing is not, however, present in programmable logic devices because the fuse array is verified using totally separate circuitry to that which is used to carry logic signals during normal device operation. Consequently, verification of the fuse array at manufacture does not guarantee correct operation of the logic paths, and because of this, fuse pattern verification by the user does not guarantee correct device functionality. It is apparent that, unlike a PROM, there are two components of FUNCTIONAL YIELD in a Programmable Logic device: FUSING YIELD and LOGIC PATH YIELD. The FUSING YIELD of a programmable logic device is similar to a PROM and is close to 100%. However, the LOGIC PATH YIELD is an unknown quantity and varies from device to device. The components of FUNCTIONAL YIELD for a programmable logic and programmable memory device are shown below.

FUNCTIONAL YIELD (PROM) = FUSING YIELD

FUNCTIONAL YIELD (PROGRAMMABLE LOGIC) = FUSING YIELD x LOGIC PATH YIELD

Responding to customer requirements for high quality devices, Harris developed unique on-chip test circuitry, patent pending, which is enabled at the time of manufacture to allow complete testing of all logic paths, eliminating the uncertain factor of LOGIC PATH YIELD. One of the benefits of this test circuitry is that the user receives a completely tested device which, providing the fuse array programs correctly, is guaranteed to be functional, eliminating the problem of devices that verify on the programmer but fail in the circuit board. A second benefit of on-chip test circuitry is the ability to perform AC/DC parametric testing at the time of manufacture. This allows Harris to ship devices which are TESTED AND GUARANTEED, and not simply GUARANTEED.

HPL PRODUCT LINE

The HPL product range includes devices from all three of the possible programmable logic architectures, in recognition of the fact that no one architecture is the optimum solution for all designs.

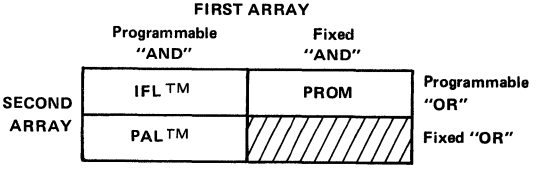


Figure 1

HPL is a Trademark of Harris Corporation
IFL is a Trademark of Signetics Corporation
PAL is a Registered Trademark of MMI

HARRIS

HPL-77061

Product Preview

HPL™ Harris Programmable Logic

The HPL-77061 is a proprietary device designed by Harris Semiconductor. It is a 24 pin device with 12 input pins, 6 bi-directional pins, and 4 output pins. The architecture consists of a programmable AND array, followed by a fixed OR array, followed by a programmable INVERTER. This configuration generates a device that implements logic expressions in either SUM OF PRODUCTS (SOP) or INVERTED SUM OF PRODUCTS (ISOP) form. Two fuses associated with each output and bi-directional pin allow their three state buffers to be configured as permanently active, permanently inactive, or under the control of a common CHIP SELECT(CS) signal. When under the control of the CS signal, they may be configured to be active when CS is high and inactive when low, or active when CS is low and inactive when high.

The HPL-77061 is intended to be used as an address decoder in 8, 16 or 32 bit microprocessor systems, and is known as a FIELD PROGRAMMABLE ADDRESS DECODER (FPAD). When used as an address decoder, it is possible to contiguously concatenate the address spaces of large and small system components. This allows more efficient use to be made of available memory space, as well as making the memory decoder design easier. The HPL-77061 may also be used to replace several TTL packages in many random logic designs. In both the above applications, a significant reduction in board space, power consumption, package count, and an increase in reliability may be realized. The HPL-77061 incorporates Harris designed test circuitry which allows complete parametric and logical testing of unprogrammed devices at the time of manufacture. The benefits for the user of this exhaustive testing are very high POST PROGRAMMING FUNCTIONAL YIELD (95% guaranteed; 97% typically) and pretested AC and DC parametrics.

The HPL-77061 uses the standard HPL programming algorithm which is also used for all Harris Programmable Logic parts. Special test fuses are included in the HPL-77061. These are selectively programmed during post manufacturing testing. This allows all the programming circuitry to be tested for correct operation.

The Harris policy is to ship pretested devices, removing the test burden from the small user and assuring the large user the highest possible quality.

• PROPAGATION DELAY	25ns MAX COMMERCIAL
• SUPPLY CURRENT	140mA MAX COMMERCIAL
• PACKAGE	24 PIN SLIMLINE (POWER PLASTIC & CERAMIC)
• TEMPERATURE OPTIONS	COMMERCIAL, MILITARY & 883B
• AC/DC SPECS	PRETESTED
• FUNCTIONALITY	PRETESTED
• PROGRAMMING	GENERIC
• TTL COMPATIBLE	
• SUPPORTED BY HELP™ SOFTWARE	

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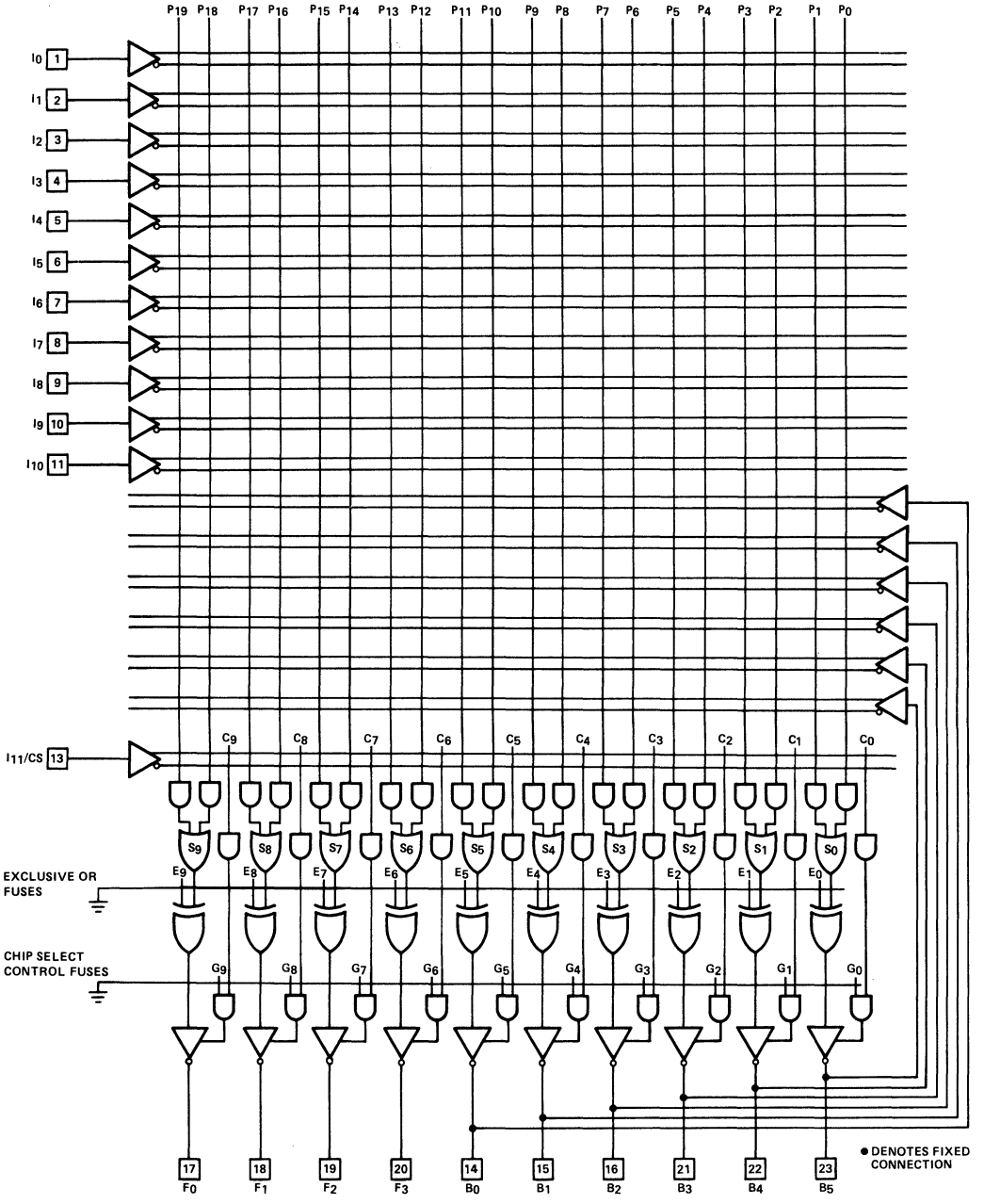
HELP is a trademark of Harris Corporation

Functional Diagram HPL-77061



HARRIS HPL-77153/82S153

HPL™ Harris Programmable Logic

Features

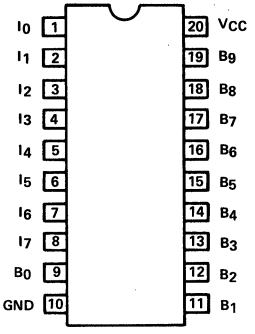
- LOGIC PATHS TESTED TO ENSURE FUNCTIONALITY
- FAST ACCESS (INPUT TO OUTPUT). . . . . 40nsec MAX
- LOW ICC. . . . . .155mA MAX
- ALLOWS SIGNIFICANT PACKAGE COUNT SAVINGS
- FUNCTIONALLY IDENTICAL TO EXISTING 82S153
- 20 PIN SLIMLINE DIP
- HIGH SPEED PROGRAMMING PROCEDURE – ONE PULSE/BIT ASSURES SUPERIOR RELIABILITY
- SUPPORTED BY HELP™ SOFTWARE
- PROGRAMMABLE SUBSTITUTE FOR TTL SSI/MSI LOGIC CIRCUITS
- REDUCTION OF IC INVENTORIES
- EASE OF PROTOTYPING AND BOARD LAYOUT
- TTL COMPATIBLE INPUTS AND OUTPUTS
- "THREE STATE" OUTPUTS
- PROGRAMMABLE OUTPUT POLARITY
- HARRIS RELIABLE NICKEL-CHROMIUM FUSE TECHNOLOGY

Applications

- RANDOM LOGIC REPLACEMENT
- CODE CONVERTORS
- ADDRESS DECODING
- FAULT DETECTORS
- BOOLEAN FUNCTION GENERATORS
- DIGITAL MULTIPLEXERS
- PARITY GENERATORS
- PATTERN RECOGNITION
- ROM PATCHING

Pinout

HPL-77153/82S153



Description

The HPL-77153/82S153 is a programmable logic device designed to be cost effective and space saving replacement for discrete logic designs. This device is a two-level logic element, consisting of 32 product terms (AND) and 10 sum terms (OR) with fusible links for programming I/O polarity and direction.

All product terms can be linked to 8 inputs (I) and 10 bidirectional I/O lines (B) allowing variable I/O configurations using the 10 direction control gates (D), ranging from 17 inputs and 1 output to 8 inputs and 10 outputs.

On chip T/C buffers allow either True (I,B) and/or Complement ($\overline{I}$,$\overline{B}$) signals to be linked to any of the product terms, the outputs of which may be used as inputs to any or all of the sum terms. The output polarity of the sum terms is individually programmable by means of a fuse link controlled EX-OR gate to allow implemention of Sum Of Products (SOP) or Inverted Sum Of Products (ISOP) expressions.

The HPL-77153/82S153 is field programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

Nickel-chromium fuse technology is used on these and all other HARRIS HPL-77XXX programmable logic devices. The HPL-77153/82S153 is available in 20 pin slimline DIP packages with a pinout identical to the 82S153.

The HPL-77153/82S153 contains unique test circuitry developed by HARRIS which is enabled at the time of manufacture to allow complete AC and DC testing.

CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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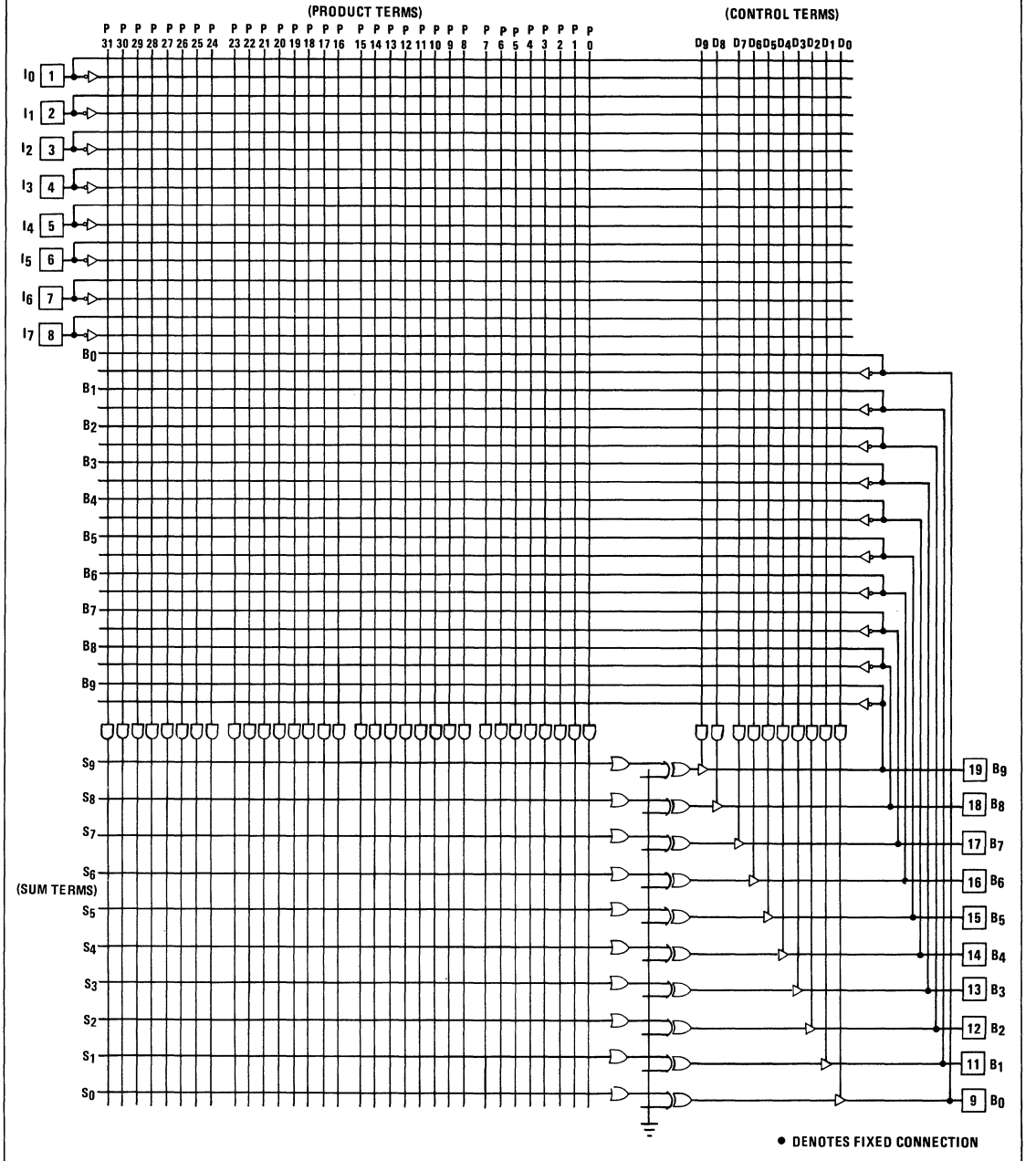
HELP is a trademark of Harris Corporation.

Functional Diagram HPL-77153/82S153



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+7V	Storage Temperature	-65°C to +150°C
Input Voltage	+5.5V	Operating Temperature (Ambient)	
Output Voltage	+5.5V	Commercial	0°C to 75°C
Input Current	-20mA	Military	-55°C to +125°C
Output Sink Current	+100mA	Maximum Junction Temperature	
		Commercial	+150°C
		Military	+175°C

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, following the programming specifications.)

D. C. ELECTRICAL CHARACTERISTICS (Operating)

HPL-77153/82S153-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HPL-77153/82S153-2/-8 (V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER		MIN	MAX	UNITS	TEST CONDITIONS	
I_{IH}	Input Current	"1"	–	+40	μA	$V_{IH} = V_{CC}$ MAX	
I_{IL}	Dedicated Input	"0"	–	-100	μA	V_{IL} = 0.4V	$V_{CC} = V_{CC}$ MAX
I_{BZH}	Input Current Bidirectional Pin Current	"1"	–	+40	μA	$V_{BH} = V_{CC}$ MAX	$V_{CC} = V_{CC}$ MAX
I_{BZL}	Hi-Z State	"0"	–	-100	μA	V_{BL} = 0.4V	
V_{IH}	Input Threshold Voltage (NOTE)	"1"	2.0	–	V	$V_{CC} = V_{CC}$ MAX	
V_{IL}		"0"	–	0.8	V	$V_{CC} = V_{CC}$ MIN	
V_{OH}	High-Level Output Voltage		2.4	–	V	$V_{CC} = V_{CC}$ MIN, V_{IL} = 0.8V, V_{IH} = 2.0V	I_{OH} = -2.0mA
V_{OL}	Low-Level Output Voltage		–	0.5	V		I_{OL} = +16mA
V_{CL}	Input Clamp Voltage		–	-1.2	V	I_{IN} = -18mA, V_{CC} = 0V	
I_{OS}	Output Short Circuit Current		-20(C) -15(M)	-70(C) -85(M)	mA mA	V_{CC} = 5.0V, V_{OUT} = 0V One output for MAX of One Sec.	
I_{CC}	Power Supply Current		– –	155(C) 165(M)	mA mA	$V_{CC} = V_{CC}$ MAX	

C = Commercial (-5) M = Military (-2/-8)

NOTE: These are absolute voltages with respect to ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

A. C. SWITCHING CHARACTERISTICS (Operating)

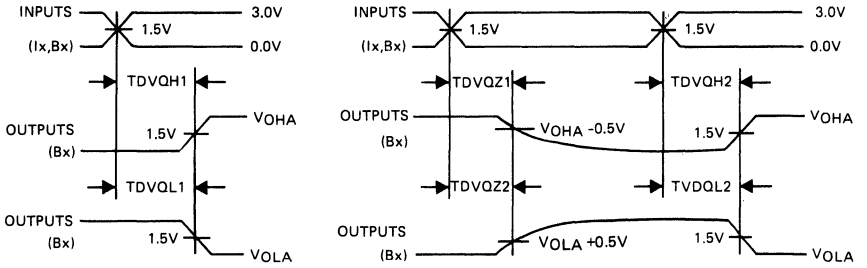
SYMBOL			HPL-77153/82S153-5 5V ± 5% 0°C to +75°C		HPL-77153/82S153-2/-8 5V ± 10% -55°C to +125°C		
JEDEC STANDARD	OLD SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS
TDVQH1	T_{PD}	Propagation Delay-Input or I/O to Active High Output	–	40	–	55	ns
TDVQL1	T_{PD}	Propagation Delay-Input or I/O to Active Low Output	–	40	–	55	ns
TDVQH2	T_{OE}	Enable Access Time to Active High Output	–	35	–	45	ns
TDVQL2	T_{OE}	Enable Access Time to Active Low Output	–	35	–	45	ns
TDVQZ1	T_{OD}	Disable Access Time from Active High Output	–	30	–	45	ns
TDVQZ2	T_{OD}	Disable Access Time from Active Low Output	–	30	–	45	ns

NOTE: Maximum test frequency is 5MHz with a 50% duty cycle.

CAPACITANCE: $T_A = 25^oC$ (NOTE: Sampled and guaranteed – but not 100% tested)

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_I	Input Capacitance	12	pF	$V_{CC} = 5.0V, V_I = 2.0V, f = 1MHz$
C_B	Bidirectional Pin Cap	15	pF	$V_{CC} = 5.0V, V_B = 2.0V, f = 1MHz$

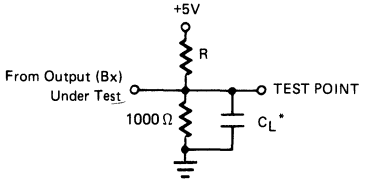
SWITCHING TIME DEFINITIONS



INPUT CONDITIONS: t_r, t_f = 5ns (10% to 90%)

NOTE: Disable access time is the time taken for the output to reach a high impedance state when the director control product term drives the output inactive. The high impedance state is defined as a point on the output waveform equal to a ΔV of 0.5 from V_{OHA} or V_{OLA}, the active output level.

AC TEST LOAD



*C_L Includes Jig and Probe Total Capacitance

This simulates the A.C. Test Load which Harris Semiconductor uses in its automatic test equipment, and it is recommended that users of Harris bipolar devices use the same or an equivalent load in performing A.C. testing.

SYMBOL	PARAMETER	R (Ω)	C_L (pF)
TDVQH1	Propagation Delay from Input or I/O to Active High Output	470	30
TDVQL1	Propagation Delay from Input or I/O to Active Low Output	470	30
TDVQH2	Enable Access Time to Active High Output	∞	30
TDVQL2	Enable Access Time to Active Low Output	470	30
TDVQZ1	Disable Access Time from Active High Output	∞	5
TDVQZ2	Disable Access Time from Active Low Output	470	5

Following is the programming procedure which is used for the Harris Bipolar HPL-77153/82S153. This device is manufactured with all fuses intact. Any desired fuse can be programmed by following the simple procedure shown below. One may build a programmer to satisfy the specifications described in the table, or use any of the commercially available programmers which meets these specifications.

PROGRAMMING SPECIFICATIONS

TABLE 1

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
V_{CCP}	V_{CC} Supply During Programming[1]		8.25	8.5	8.75	V
I_{CCP}	I_{CC} Limit During Programming		550	–	1000	mA
V_{IH}	Input Voltage (High)		2.4	–	5.5	V
V_{IL}	Input Voltage (Low)		0.0	–	0.8	V
I_{IHP}	Input Current (High) During Prog.	V_{IH} = +5.5V	–	–	50	μA
I_{ILP}	Input Current (Low) During Prog.	V_{IL} = 0V	–	–	-500	μA
V_{OPF}	Forced Output Voltage [2]	Transient or Steady State	17.0	17.5	18.0	V
I_{OPF}	Forced Output Current		–	100	325	mA
PW_V	Verify Pulse Width		1	5	50	μS
PW_P	Programming Pulse Width		90	100	110	μS
T_D	Pulse Sequence Delay		1	5	50	μS
tr_2	Forced Output Voltage Rise Time	10% to 90%	4	14	40	μS
tr1	V_{CC} Supply Rise Time	10% to 90%	2	7	20	μS
tf_2	Forced output Voltage Fall Time	90% to 10%	2	7	20	μS
t_{f1}	V_{CC} Supply Fall Time	90% to 10%	1	4	10	μS
T_{PP}	Programming Period		100	160	350	μS
F_L	Fusing Attempts per Link		–	1	2	Cycle
V_S	Verify Threshold[3]		1.4	1.5	1.6	V

NOTES:

1. Bypass V_{CC} to GND with a 0.01μf capacitor to reduce voltage spikes. The V_{CC} power supply must be capable of handling 1 Ampere maximum.
2. Care should be taken to ensure that the voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.
3. V_S is the sensing threshold of the device output voltage for a programmed link. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.

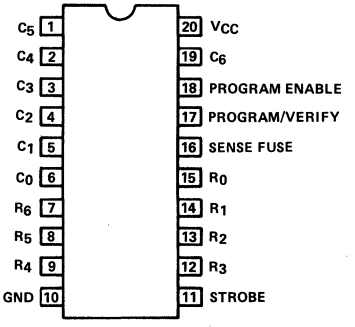


Figure 1
EDIT MODE PINOUT
HPL-77153/82S153

NOTE: While programming the HPL-77153/82S153, no pins should be left floating. Pin 16 (Sense Fuse) appears as an open collector output during programming. It should be tied to V_{CC} through a 10K ohm resistor.

PROGRAMMING PROCEDURE

1. **Set-Up:**
   a. During programming, no pins should be left floating. Pin 16 should be terminated with a 10k ohm resistor to V_{CC}.
   b. Set GND (Pin 10) to 0V.
2. **Select the EDIT Mode:**
   a. Apply 0V to Pin 20.
   b. Apply V_{IL} to Pin 18.
   c. Apply V_{IH} to Pin 11.
   d. Apply V_{IL} to Pin 17.
3. **Select the Fuse to be Programmed:**
   a. Wait T_D and select a ROW by specifying the appropriate binary ROW address according to TABLE 2.
   b. Select a COLUMN by specifying the appropriate binary COLUMN address according to TABLE 3.
4. **Program the Fuse:**
   a. Wait T_D and raise Pin 20 to V_{CCP}.
   b. Wait T_D and raise Pin 17 to V_{IH}.
   c. Wait T_D and raise Pin 18 to V_{OPF}.
   d. Wait T_D and pulse Pin 11 to V_{IL} for a duration of PW_P.
   e. Return Pin 11 to V_{IH}.
   f. Wait T_D and lower Pin 18 to V_{IL}.
   g. Wait T_D and lower Pin 17 to V_{IL}.
5. **Verify Programmed Fuse:**
   a. Wait T_D and lower Pin 11 to V_{IL}.
   b. At the end of PW_V, monitor Pin 16 for a level of V_{OH}.
   c. Return Pin 11 to V_{IH}.
   d. Wait T_D and lower Pin 20 to 0V.
   e. If Pin 16 has indicated a V_{OL}, return to step 4 and repeat so that the fuse receives a maximum of two (2) fusing attempts.
6. **Repeat Steps 3 Through 5 for All Fuses to be Blown.**

PROGRAMMING WAVEFORMS

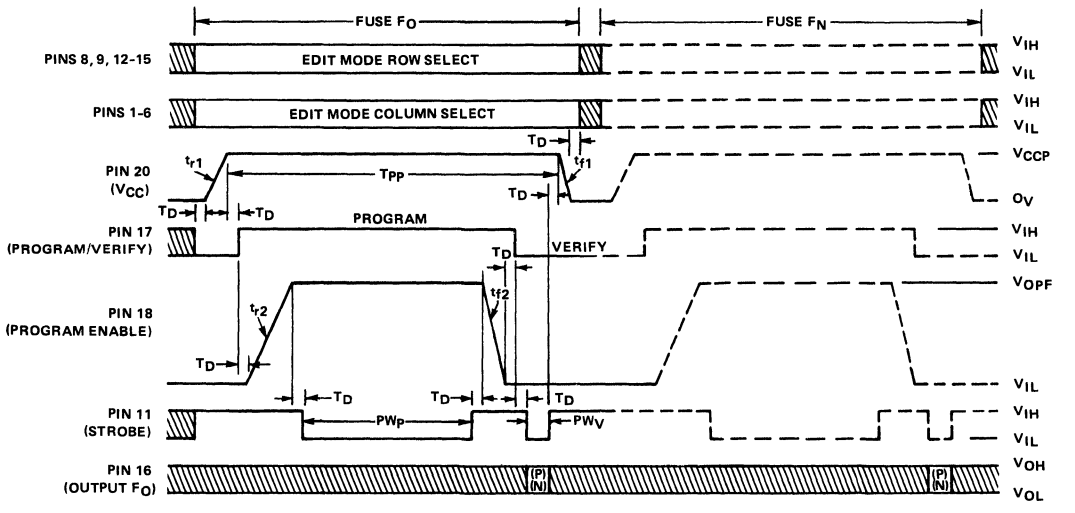


Figure 2

TABLE 2
EDIT MODE ROW SELECT

R5	R4	R3	R2	R1	R0	SELECTED ROW	
Pin 8	Pin 9	Pin 12	Pin 13	Pin 14	Pin 15		
L	L	L	L	L	L	I0	AND ARRAY
L	L	L	L	L	H	$\overline{I0}$	
L	L	L	L	H	L	I1	
L	L	L	L	H	H	$\overline{I1}$	
L	L	L	H	L	L	I2	
L	L	L	H	L	H	$\overline{I2}$	
L	L	L	H	H	L	I3	
L	L	L	H	H	H	$\overline{I3}$	
L	L	L	L	L	L	I4	
L	L	L	L	L	H	$\overline{I4}$	
L	L	L	L	H	L	I5	
L	L	L	L	H	H	$\overline{I5}$	
L	L	L	H	L	L	I6	
L	L	L	H	L	H	$\overline{I6}$	
L	L	L	H	H	L	I7	
L	L	L	H	H	H	$\overline{I7}$	
L	L	H	L	L	L	B9	
L	L	H	L	L	H	$\overline{B9}$	
L	L	H	L	H	L	B8	
L	L	H	L	H	H	$\overline{B8}$	
L	L	H	H	L	L	B7	
L	L	H	H	L	H	$\overline{B7}$	
L	L	H	H	H	L	B6	
L	L	H	H	H	H	$\overline{B6}$	
L	H	L	L	L	L	B5	
L	H	L	L	L	H	$\overline{B5}$	
L	H	L	L	H	L	B4	
L	H	L	L	H	H	$\overline{B4}$	
L	H	L	H	L	L	B3	
L	H	L	H	L	H	$\overline{B3}$	
L	H	L	H	H	L	B2	
L	H	L	H	H	H	$\overline{B2}$	
L	H	H	L	L	L	B1	
L	H	H	L	L	H	$\overline{B1}$	
L	H	H	L	H	L	B0	
L	H	H	L	H	H	$\overline{B0}$	
H	L	L	L	L	L	B9	OR ARRAY
H	L	L	L	L	H	B8	
H	L	L	L	H	L	B7	
H	L	L	L	H	H	B6	
H	L	L	H	L	L	B5	
H	L	L	H	L	H	B4	
H	L	L	H	H	L	B3	
H	L	L	H	H	H	B2	
H	L	H	L	L	L	B1	
H	L	H	L	L	H	B0	
H	H	H	L	H	L	OUTPUT POLARITY ENABLE	

TABLE 3
EDIT MODE COLUMN SELECT

C5	C4	C3	C2	C1	C0	SELECTED COLUMN	
Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6		
L	L	L	L	L	L	0	PRODUCT TERMS
L	L	L	L	L	H	1	
L	L	L	L	H	L	2	
L	L	L	L	H	H	3	
L	L	L	H	L	L	4	
L	L	L	H	L	H	5	
L	L	L	H	H	L	6	
L	L	L	H	H	H	7	
L	L	H	L	L	L	8	
L	L	H	L	L	H	9	
L	L	H	L	H	L	10	
L	L	H	L	H	H	11	
L	L	H	H	L	L	12	
L	L	H	H	L	H	13	
L	L	H	H	H	L	14	
L	L	H	H	H	H	15	
L	H	L	L	L	L	16	
L	H	L	L	L	H	17	
L	H	L	L	H	L	18	
L	H	L	L	H	H	19	
L	H	L	H	L	L	20	
L	H	L	H	L	H	21	
L	H	L	H	H	L	22	
L	H	L	H	H	H	23	
L	H	H	L	L	L	24	
L	H	H	L	L	H	25	
L	H	H	L	H	L	26	
L	H	H	L	H	H	27	
L	H	H	H	L	L	28	
L	H	H	H	L	H	29	
L	H	H	H	H	L	30	
L	H	H	H	H	H	31	
H	L	L	L	L	L	D0	CONTROL TERMS
H	L	L	L	L	H	D1	
H	L	L	L	H	L	D2	
H	L	L	L	H	H	D3	
H	L	L	H	L	L	D4	
H	L	L	H	L	H	D5	
H	L	L	H	H	L	D6	
H	L	L	H	H	H	D7	
H	L	H	L	L	L	D8	
H	L	H	L	L	H	D9	
H	L	H	L	H	L	B0	POLARITY TERMS
H	L	H	L	H	H	B1	
H	L	H	H	L	L	B2	
H	L	H	H	L	H	B3	
H	L	H	H	H	L	B4	
H	L	H	H	H	H	B5	
H	H	L	L	L	L	B6	
H	H	L	L	L	H	B7	
H	H	L	L	H	L	B8	
H	H	L	L	H	H	B9	

NOTES: 1) Pin 7 (R6) and Pin 19 (C6) are used for programming other HPL devices and should be held at or less than V_{IL} during programming.

2) $0V \leq L \leq V_{IL}$
$V_{IH} \leq H \leq 5V$

PROGRAM TABLE ENTRIES:

I, B(I) (AND)

INACTIVE	O
I, B	H
I, B	L
Don't Care	—

B(O) (OR)

ACTIVE	A
INACTIVE	•

B(O) (POL)

HIGH	H
LOW	L

NOTES
1. The FPLA is shipped with all links intact. Thus a background of entries corresponding to states of virgin links exists in the table, shown BLANK for clarity.
2. Unused I and B bits in the AND array are normally programmed Don't Care (—).
3. Unused product terms can be left blank.

TERM	AND I 7	6	5	4	3	2	1	0	AND B(I) 9	8	7	6	5	4	3	2	1	0	POLARITY OR B(O) 9	8	7	6	5	4	3	2	1	0
0																												
1																												
2																												
3																												
4																												
5																												
6																												
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D6																												
D5																												
D4																												
D3																												
D2																												
D1																												
D0																												
PIN	8	7	6	5	4	3	2	1	19	18	17	16	15	14	13	12	11	9										

Figure 3

USE OF THE PROGRAMMING FORM

The programming form for the HPL-77153 is shown in Figure 3. This device has ten bi-directional pins (B0-B9) which may be used as outputs or inputs. Any pin used as an output can have from 1 to 32 product terms (AND) summed (OR'D) to it. Each product term can have from one to eighteen variables. In addition, each bi-directional pin has an extra product term (CONTROL TERM) which may be used to drive those pins into a high impedance state. This allows the ten bi-directional pins to be used as inputs if desired.

The HPL-77153 has the capability for its output polarity to be user determined. Output polarity selection is made possible by the addition of 10 extra fuses associated with the ten bi-directional pins. The HPL-77153 is supplied with the polarity fuses intact, causing the outputs to be non-inverting. If a particular polarity fuse is blown, then the output associated with that fuse will be inverting. Referring to the programming form (Figure 3), it can be seen that the product term and control term numbers are listed at the left hand side. Across the top, the input variables are listed. In order to include an input variable in a product term, an "L" or "H" should be placed in the box at the intersection of the input variable and the product term. An "L" causes the inverted form of an input variable to be included, and an "H", the true form. If it is not desired to include either form for an input variable in a product term, a dash (—) should be placed in the box. Notice that for every product term, a "0" in any single box or any combination of boxes will cause that product term to be unconditionally disabled (A./A=0), and will not contribute to any output. If it is desired not to use a product term, then all its boxes may be left blank. This has the same effect as including a "0".

Exactly the same procedure is used for the control terms. But in this case, the bi-directional pins may have dynamic three-state control by including "H's" and "L's", or may be forced permanently three-stated by including one or more "0's", or by leaving the control term blank. The bi-directional pins may also be forced permanently active by placing dashes in all the boxes of the associated control term. At the right hand side of the programming form, the sum terms (OR) are shown. Placing an "A" in a box at the intersection of a product term and a bi-directional pin will cause the product term to be summed to that output. Because the product terms are not dedicated to any specific output, any product term may be summed to any of the ten outputs. In this way, product terms may be shared thereby reducing the total number of product terms required for a given application. If it is not desired to sum a product term to an output, a dot (.) should be placed at the intersection of the product term and the output. Any unused product terms (which contribute a logical "0") should be summed to all outputs by placing an "A" at all product term and output intersections. This preserves maximum flexibility for future modifications since product terms which are no longer required may be disconnected in the OR array and unused product terms may be substituted. This capability for "logical surgery" is unique to the FPLA architecture because product terms in an unprogrammed part are not committed to any specific output pin.

The HPL-77153 experiences propagation delay variations as a function of the pattern used in the OR arrray. Although all devices are pre-tested and guaranteed to meet the AC switching characteristics with a worst case pattern, it is possible to minimize propagation delays by disconnecting unused product terms. This can be done by placing dots in all the product term and output intersections. Harris Semiconductor does not specify or guarantee a particular decrease in propagation delay; it is left to customers to measure this for themselves.

Care should be taken when using a signal from an output pin as input variable for the same output pin, as this may cause a latched or oscillatory condition to occur if a positive or negative feedback loop is formed.

HPL devices are supplied with all fuses intact and undesired fuses or connections must be blown. For information concerning the entry of fuse data from the programming form into a suitable HPL programmer, refer to the operating guide for that programmer. If it is desired that device programming should be performed by Harris, programming information may be supplied in one or more of the following forms:

1. Master devices (Harris or other).
2. Boolean equations.
3. Paper tapes.
4. Programming form.
5. Marked up logic diagrams (a substantial charge may be made for this entry format).

HARRIS

HPL-77215/16H8
HPL-77216/16P8
HPL-77209/16L8

HPL™ Harris Programmable Logic

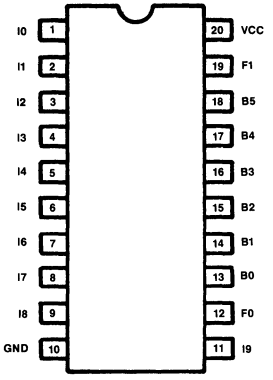
Features

- LOGIC PATHS TESTED TO ENSURE FUNCTIONALITY
- FAST ACCESS (INPUT TO OUTPUT) 35nsec MAX
- LOW ICC 155mA MAX
- ALLOWS SIGNIFICANT PACKAGE COUNT SAVINGS
- INDUSTRY STANDARD AND PROPRIETARY PARTS
- 20 PIN SLIMLINE DIP
- HIGH SPEED PROGRAMMING PROCEDURE - ONE PULSE/FUSE ASSURES SUPERIOR RELIABILITY
- PROGRAMMABLE SUBSTITUTE FOR TTL SSI/MSI LOGIC CIRCUITS
- REDUCTION OF IC INVENTORIES
- EASE OF PROTOTYPING AND BOARD LAYOUT
- TTL COMPATIBLE INPUTS AND OUTPUTS
- "THREE STATE" OUTPUTS
- PROGRAMMABLE OUTPUT POLARITY
- THE HARRIS RELIABLE NICKEL-CHROMIUM FUSE TECHNOLOGY
- SUPPORTED BY HELP™ SOFTWARE

Applications

- RANDOM LOGIC REPLACEMENT
- CODE CONVERTORS
- ADDRESS DECODING
- FAULT DETECTORS
- BOOLEAN FUNCTION GENERATORS
- DIGITAL MULTIPLEXERS
- PARITY GENERATORS
- PATTERN RECOGNITION
- ROM PATCHING

Pinout
HPL-77215/216/209



5
HPL

Description

The HPL-77215/216/209 are programmable logic devices designed to be cost effective and space saving replacements for discrete logic designs. These devices are two-level logic elements consisting of 7 product terms (AND) summed (OR) together to generate each of the 8 outputs. An eighth product term associated with each output can drive it to a high impedance state allowing 6 (B0-B5) of the 8 outputs to be used as inputs, either permanently or dynamically.

The HPL-77209 is functionally identical to the industry standard 16L8, and implements logic expressions of the Inverted Sum Of Products (ISOP) form.

The HPL-77215 is a similar device to the 16L8 but does not include the associated output inversion. It implements logic expressions of the Sum Of Products (SOP) form.

The HPL-77216 is a more flexible device, it includes 8 EX-OR gates in each output path, controlled by 8 extra fuses, allowing the polarity of each output to be user configured. This device can implement a combination of SOP and ISOP expressions.

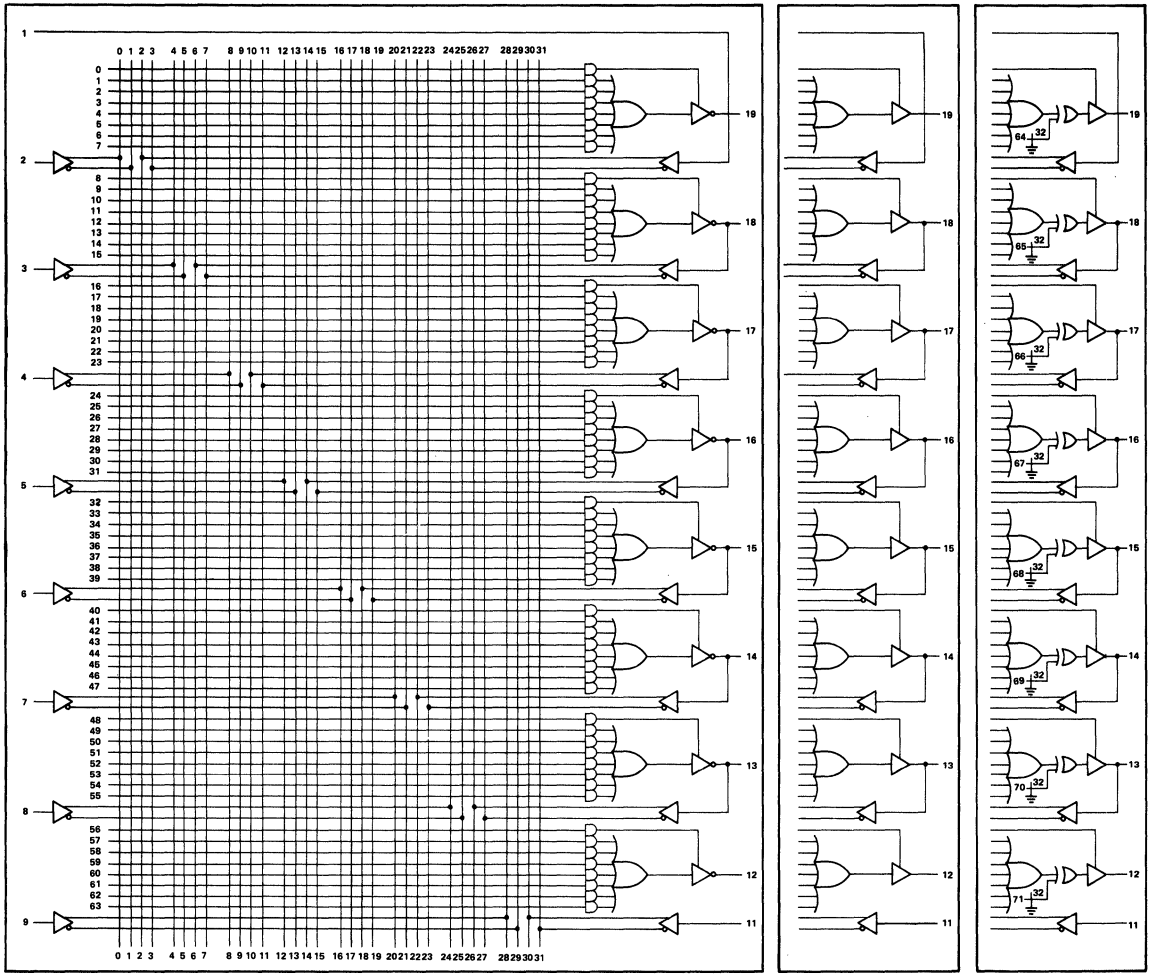
The HPL-77215/216/209 are field programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

Nickel-chromium fuse technology is used on these and all other HARRIS HPL-77XXX programmable logic devices. The HPL-77215/216/209 are available in 20 pin slimline DIP packages with pinouts identical to the 16L8.

The HPL-77215/216/209 contain unique test circuitry developed by HARRIS which is enabled at the time of manufacture to allow complete AC and DC testing.

CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
HPL is a trademark of Harris Corporation.
HELP is a trademark of Harris Corporation.

HPL-77209/16L8 **HPL-77215/16H8** **HPL-77216/16P8**



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+7V	Storage Temperature	−65°C to +150°C
Input Voltage	+5.5V	Operating Temperature (Ambient)	
Output Voltage	+5.5V	Commercial	0°C to +75°C
Input Current	−20mA	Military	−55°C to +125°C
Output Sink Current	+100mA	Maximum Junction Temperature	
		Commercial	+150°C
		Military	+175°C

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, following the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HPL-77215/216/209 −5 (V_{CC} = 5.0V±5%, T_A = 0°C to +75°C)
HPL-77215/216/209 −2/−8 (V_{CC} = 5.0V±10%, T_A = −55°C to +125°C)

SYMBOL	PARAMETER		MIN	MAX	UNITS	TEST CONDITIONS	
I_{IH}	Input Current	"1"	—	+25	µA	V_{IH} = V_{CC} MAX	
I_{IL}	Dedicated Input	"0"	—	−100	µA	V_{IL} = 0.4 V	V_{CC} = V_{CC} MAX
I_{FZH}		"1"	—	+40	µA	V_{FH} = V_{CC} MAX	
	Output Current						V_{CC} = V_{CC} MAX
I_{FZL}	HI-Z State	"0"	—	−40	µA	V_{FL} = 0.4V	
I_{BZH}		"1"	—	+40	µA	V_{BH} = V_{CC} MAX	
	Bidirectional Pin Current						V_{CC} = V_{CC} MAX
I_{BZL}	Hi-Z State	"0"	—	−100	µA	V_{BL} = 0.4V	
V_{IH}		"1"	2.0	—	V	V_{CC} = V_{CC} MAX	
	Input Threshold (1)						
V_{IL}	Voltage	"0"	—	0.8	V	V_{CC} = V_{CC} MIN	
V_{OH}	High-Level Output Voltage (2)		2.4	—	V	V_{CC} = V_{CC} MIN	I_{OH} = −2.0mA (M) I_{OH} = −3.2mA (C)
V_{OL}	Low-Level Output Voltage (2)		—	0.5	V	V_{IL} = 0.8V V_{IH} = 2.0V	I_{OL} = +16mA (M) I_{OL} = +24mA (C) (3)
V_{CL}	Input Clamp Voltage (1)		—	−1.2	V	I_{IN} = −18mA, V_{CC} = OV	
I_{OS}	Output Short Circuit Current (2)		−30	−130	mA	V_{CC} = 5.0V, V_{OUT} = OV One Output for MAX of One Sec.	
I_{CC}	Power Supply Current		—	155 (C)	mA	V_{CC} = V_{CC} MAX	
			—	165 (M)	mA		

C = Commercial (-5) M = Military (-2/-8)

(1) These specifications apply to both Input (I) & Bi-Directional (B) pins. These are absolute voltages with respect to ground pin & include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

(2) These specifications apply to both Output (F) and Bi-Directional (B) pins.

(3) One output at a time, otherwise 16mA.

A. C. SWITCHING CHARACTERISTICS (Operating)

SYMBOL			HPL-77215−5 HPL-77216−5 HPL-77209−5 5V±5% 0°C to +75°C		HPL-77215−2/−8 HPL-77216−2/−8 HPL-77209−2/−8 5V±10% −55°C to +125°C		
JEDEC STANDARD	OLD SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS
TDVQH1	T_{PD}	Propagation Delay – Input or I/O to Active High Output	—	35	—	45	ns
TDVQL1	T_{PD}	Propagation Delay – Input or I/O to Active Low Output	—	35	—	45	ns
TDVQH2	T_{PZX}	Enable Access Time to Active High Output (1)	TDVQZ1	35	TDVQZ1	45	ns
TDVQL2	T_{PZX}	Enable Access Time to Active Low Output (1)	TDVQZ2	35	TDVQZ2	45	ns
TDVQZ1	T_{PXZ}	Disable Access Time from Active High Output	—	30	—	35	ns
TDVQZ2	T_{PXZ}	Disable Access Time from Active Low Output	—	30	—	35	ns

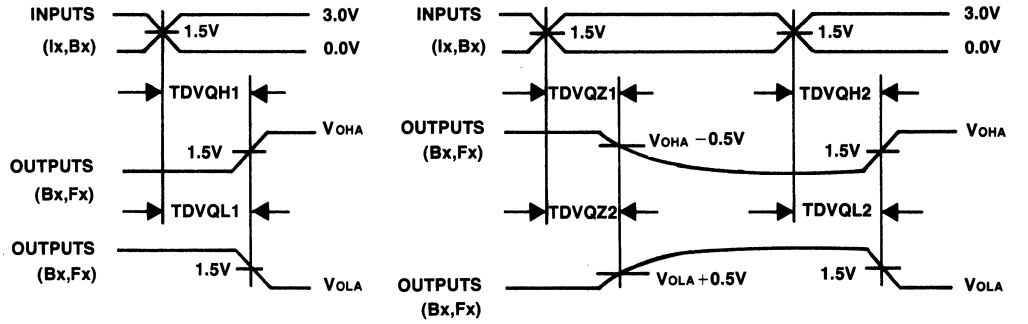
(1) Enable Access Time is guaranteed greater than Disable Access Time to avoid device contention.

NOTE: Maximum test frequency is 5MHz with a 50% duty cycle.

CAPACITANCE: T_A = 25°C (NOTE: Sampled and guaranteed – but not 100% tested.)

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_I	Input Capacitance	12	pF	V_{CC} = 5.0V, V_I = 2.0V, f = 1 MHz
C_F	Output Capacitance	15	pF	V_{CC} = 5.0V, V_F = 2.0V, f = 1 MHz
C_B	Bidirectional Pin Cap.	15	pF	V_{CC} = 5.0V, V_B = 2.0V, f = 1 MHz

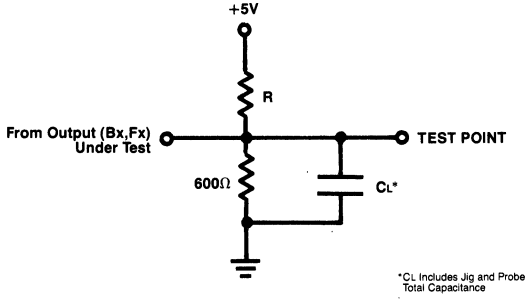
SWITCHING TIME DEFINITIONS



INPUT CONDITIONS: t_r, t_f = 5ns (10% to 90%)

NOTE: Disable access time is the time taken for the output to reach a high impedance state when the three-state product term drives the output inactive. The high impedance state is defined as a point on the output waveform equal to a ΔV of 0.5 from VOHA or VOLA, the active output level.

AC TEST LOAD



This simulates the A.C. Test Load which Harris Semiconductor uses in its automatic test equipment, and it is recommended that users of Harris bipolar devices use the same or an equivalent load in performing A.C. testing.

SYMBOL	PARAMETER	R(Ω)	C_L (pF)
TDVQH1	Propagation Delay from Input or I/O to Active High Output	300	50
TDVQL1	Propagation Delay from Input or I/O to Active Low Output	300	50
TDVQH2	Enable Access Time to Active High Output	∞	50
TDVQL2	Enable Access Time to Active Low Output	300	50
TDVQZ1	Disable Access Time from Active High Output	∞	5
TDVQZ2	Disable Access Time from Active Low Output	300	5

Following is the programming procedure which is used for the HPL-77216/215/209 devices. These devices are manufactured with all fuses intact. Any desired fuse can be programmed by following the simple procedure shown on the following page. One may build a programmer to satisfy the specifications described in the table, or use any of the commercially available programmers which meet these specifications.

PROGRAMMING SPECIFICATIONS
TABLE 1

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
V_{CCP}	Vcc Supply During Programming[1]		8.25	8.5	8.75	V
I_{CCP}	Icc Limit During Programming		550	—	1000	mA
V_{IH}	Input Voltage (High)		2.4	—	5.5	V
V_{IL}	Input Voltage (Low)		0.0	—	0.8	V
I_{IHP}	Input Current (High) During Prog.	V_{IH} = +5.5V	—	—	50	μA
I_{ILP}	Input Current (Low) During Prog.	V_{IL} = 0V	—	—	−500	μA
V_{OPF}	Forced Output Voltage[2]	Transient or Steady State	16.0	16.5	18.0	V
I_{OPF}	Forced Output Current		275	300	325	mA
PW_V	Verify Pulse Width		1	5	50	μS
PW_P	Programming Pulse Width		90	100	110	μS
T_D	Pulse Sequence Delay		1	5	50	μS
t_{r2}	Forced Output Voltage Rise Time	10% to 90%	4	14	40	μS
t_{r1}	Vcc Supply Rise Time	10% to 90%	2	7	20	μS
t_{f2}	Forced Output Voltage Fall Time	90% to 10%	2	7	20	μS
t_{f1}	Vcc Supply Fall Time	90% to 10%	1	4	10	μS
T_{PP}	Programming Period		100	160	350	μS
F_L	Fusing Attempts per Link		—	1	2	Cycle
V_S	Verify Threshold[3]		1.4	1.5	1.6	V

NOTES:

1. Bypass VCC to GND with a 0.01 μF capacitor to reduce voltage spikes. The VCC power supply must be capable of handling 1 Ampere maximum.
2. Care should be taken to ensure that the voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.
3. VS is the sensing threshold of the device output voltage for a programmed link. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.

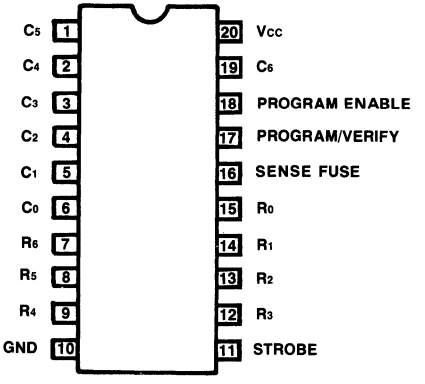


Figure 1
EDIT MODE PINOUT
HPL-77216/215/209

NOTE: While programming the HPL-77216/215/209 no pins should be left floating. Pin 16 (SENSE FUSE) appears as an open collector output during programming. It should be tied to VCC through a 10K ohm resistor.

PROGRAMMING PROCEDURE

1. Set-Up:
   a. During programming, no pins should be left floating. Pin 16 should be terminated with a 10k ohm resistor to V_{CC}.
   b. Set GND (Pin 10) to OV.
2. Select the EDIT Mode:
   a. Apply OV to Pin 20.
   b. Apply V_{IL} to Pin 18.
   c. Apply V_{IH} to Pin 11.
   d. Apply V_{IL} to Pin 17.
3. Select the Fuse to be Programmed:
   a. Wait T_D and select a ROW by specifying the appropriate binary ROW address according to Table 2.
   b. Select a COLUMN by specifying the appropriate binary COLUMN address according to Table 3.
4. Program the Fuse:
   a. Wait T_D and raise Pin 20 to V_{CCP}.
   b. Wait T_D and raise Pin 17 to V_{IH}.
   c. Wait T_D and raise Pin 18 to V_{OPF}.
   d. Wait T_D and pulse Pin 11 to V_{IL} for a duration of PWp.
   e. Return Pin 11 to V_{IH}.
   f. Wait T_D and lower Pin 18 to V_{IL}.
   g. Wait T_D and lower Pin 17 to V_{IL}.
5. Verify Programmed Fuse:
   a. Wait T_D and lower Pin 11 to V_{IL}.
   b. At the end of PWv, monitor Pin 16 for a level of Vs.
   c. Return Pin 11 to V_{IH}.
   d. Wait T_D and lower Pin 20 to OV.
   e. If Pin 16 has indicated a V_{OL}, return to step 4 and repeat so that the fuse receives a maximum of two (2) fusing attempts.
6. Repeat Steps 3 Through 5 for All Fuses to be Blown.

PROGRAMMING WAVEFORMS

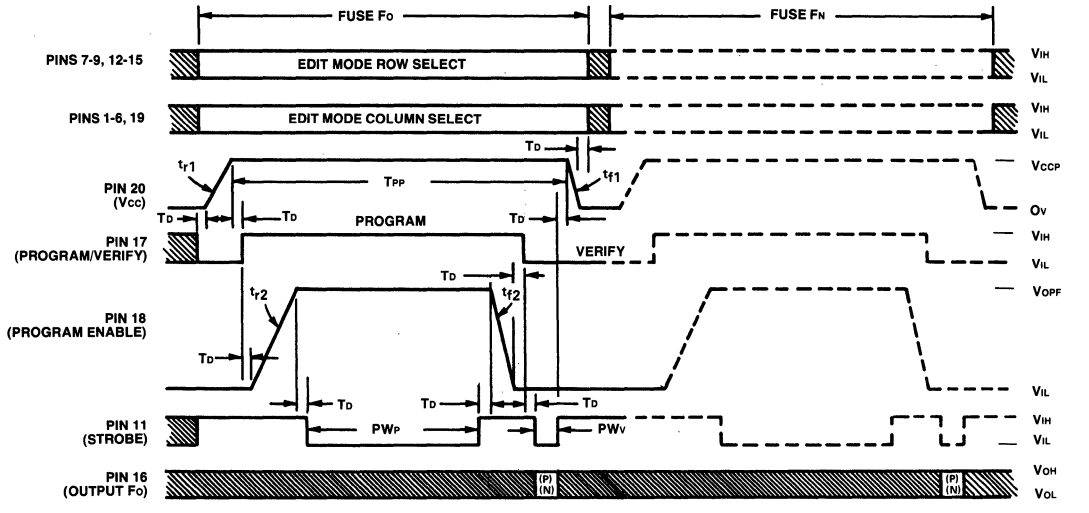


Figure 2

TABLE 2
EDIT MODE ROW SELECT

ROW NUMBER	R5 Pin 8	R4 Pin 9	R3 Pin 12	R2 Pin 13	R1 Pin 14	R0 Pin 15	VARIABLE
0	L	L	L	L	L	L	I1 $\overline{I1}$
1	L	L	L	L	L	H	
2	L	L	L	L	H	L	I0 $\overline{I0}$
3	L	L	L	L	H	H	
4	L	L	L	H	L	L	I2 $\overline{I2}$
5	L	L	L	H	L	H	
6	L	L	L	H	H	L	B5 $\overline{B5}$
7	L	L	L	H	H	H	
8	L	L	H	L	L	L	I3 $\overline{I3}$
9	L	L	H	L	L	H	
10	L	L	H	L	H	L	B4 $\overline{B4}$
11	L	L	H	L	H	H	
12	L	L	H	H	L	L	I4 $\overline{I4}$
13	L	L	H	H	L	H	
14	L	L	H	H	H	L	B3 $\overline{B3}$
15	L	L	H	H	H	H	
16	L	H	L	L	L	L	I5 $\overline{I5}$
17	L	H	L	L	L	H	
18	L	H	L	L	H	L	B2 $\overline{B2}$
19	L	H	L	L	H	H	
20	L	H	L	H	L	L	I6 $\overline{I6}$
21	L	H	L	H	L	H	
22	L	H	L	H	H	L	B1 $\overline{B1}$
23	L	H	L	H	H	H	
24	L	H	H	L	L	L	I7 $\overline{I7}$
25	L	H	H	L	L	H	
26	L	H	H	L	H	L	B0 $\overline{B0}$
27	L	H	H	L	H	H	
28	L	H	H	H	L	L	I8 $\overline{I8}$
29	L	H	H	H	L	H	
30	L	H	H	H	H	L	I9 $\overline{I9}$
31	L	H	H	H	H	H	
32	H	L	L	L	L	L	EX-OR SELECT

NOTES:

(1) Row number 32 should only be selected when programming the HPL-77216/16P8.

(2) Pin 7 (R6) is used for programming other HPL devices and should be held at or less than VIL during programming.

(3) $0V \leq L \leq V_{IL}$
$V_{IH} \leq H \leq 5v$

TABLE 3
EDIT MODE COLUMN SELECT

COLUMN NUMBER	C6 Pin 19	C5 Pin 1	C4 Pin 2	C3 Pin 3	C2 Pin 4	C1 Pin 5	C0 Pin 6	PART NUMBER
0	L	L	L	L	L	L	L	
1	L	L	L	L	L	L	H	
2	L	L	L	L	L	H	L	
3	L	L	L	L	L	H	H	
4	L	L	L	L	H	L	L	
5	L	L	L	L	H	L	H	
6	L	L	L	L	H	H	L	
7	L	L	L	L	H	H	H	
8	L	L	L	H	L	L	L	
9	L	L	L	H	L	L	H	
10	L	L	L	H	L	H	L	
11	L	L	L	H	L	H	H	
12	L	L	L	H	H	L	L	
13	L	L	L	H	H	L	H	
14	L	L	L	H	H	H	L	
15	L	L	L	H	H	H	H	
16	L	L	H	L	L	L	L	
17	L	L	H	L	L	L	H	
18	L	L	H	L	L	H	L	
19	L	L	H	L	L	H	H	
20	L	L	H	L	H	L	L	HPL77215
21	L	L	H	L	H	L	H	
22	L	L	H	L	H	H	L	HPL77216
23	L	L	H	L	H	H	H	
24	L	L	H	H	L	L	L	HPL77209
25	L	L	H	H	L	L	H	
26	L	L	H	H	L	H	L	
27	L	L	H	H	L	H	H	
28	L	L	H	H	H	L	L	
29	L	L	H	H	H	L	H	
30	L	L	H	H	H	H	L	
31	L	L	H	H	H	H	H	
32	L	H	L	L	L	L	L	
33	L	H	L	L	L	L	H	
34	L	H	L	L	L	H	L	
35	L	H	L	L	L	H	H	
36	L	H	L	L	H	L	L	
37	L	H	L	L	H	L	H	
38	L	H	L	L	H	H	L	
39	L	H	L	L	H	H	H	
40	L	H	L	H	L	L	L	
41	L	H	L	H	L	L	H	
42	L	H	L	H	L	H	L	
43	L	H	L	H	L	H	H	
44	L	H	L	H	H	L	L	
45	L	H	L	H	H	L	H	
46	L	H	L	H	H	H	L	
47	L	H	L	H	H	H	H	
48	L	H	H	L	L	L	L	
49	L	H	H	L	L	L	H	
50	L	H	H	L	L	H	L	
51	L	H	H	L	L	H	H	
52	L	H	H	L	H	L	L	
53	L	H	H	L	H	L	H	
54	L	H	H	L	H	H	L	
55	L	H	H	L	H	H	H	
56	L	H	H	H	L	L	L	
57	L	H	H	H	L	L	H	
58	L	H	H	H	L	H	L	
59	L	H	H	H	L	H	H	
60	L	H	H	H	H	L	L	
61	L	H	H	H	H	L	H	
62	L	H	H	H	H	H	L	
63	L	H	H	H	H	H	H	
64	H	L	L	L	L	L	L	
65	H	L	L	L	L	L	H	
66	H	L	L	L	L	H	L	HPL77216 ONLY
67	H	L	L	L	L	H	H	
68	H	L	L	L	H	L	L	ROW 32 ONLY
69	H	L	L	L	H	L	H	
70	H	L	L	L	H	H	L	
71	H	L	L	L	H	H	H	

ROW NUMBER	02	03	00	01	04	05	08	09	12	13	16	17	20	21	24	25	28	29	30	31	26	27	22	23	18	19	14	15	10	11	06	07	32	
INPUT NAME	I0	$\overline{I0}$	I1	$\overline{I1}$	I2	$\overline{I2}$	I3	$\overline{I3}$	I4	$\overline{I4}$	I5	$\overline{I5}$	I6	$\overline{I6}$	I7	$\overline{I7}$	I8	$\overline{I8}$	I9	$\overline{I9}$	B0	$\overline{B0}$	B1	$\overline{B1}$	B2	$\overline{B2}$	B3	$\overline{B3}$	B4	$\overline{B4}$	B5	$\overline{B5}$	⏚	
COL NUMBER																																		OUTPUT NAME
3 STATE 00																																		
01																																		
02																																		
03																																		
04																																		F1
05																																		
06																																		
07																																		
INVERT 64																																		
3 STATE 08																																		
09																																		
10																																		
11																																		
12																																		B5
13																																		
14																																		
15																																		
INVERT 65																																		
3 STATE 16																																		
17																																		
18																																		
19																																		
20																																		B4
21																																		
22																																		
23																																		
INVERT 66																																		
3 STATE 24																																		
25																																		
26																																		
27																																		
28																																		B3
29																																		
30																																		
31																																		
INVERT 67																																		
3 STATE 32																																		
33																																		
34																																		
35																																		
36																																		B2
37																																		
38																																		
39																																		
INVERT 68																																		
3 STATE 40																																		
41																																		
42																																		
43																																		
44																																		B1
45																																		
46																																		
47																																		
INVERT 69																																		
3 STATE 48																																		
49																																		
50																																		
51																																		
52																																		B0
53																																		
54																																		
55																																		
INVERT 70																																		
3 STATE 56																																		
57																																		
58																																		
59																																		
60																																		F0
61																																		
62																																		
63																																		
INVERT 71																																		

Figure 3

USE OF THE PROGRAMMING FORM

The programming form for the HPL-77215/216/209 is shown in Figure 3. All three devices have two output pins (F0-F1), and six bi-directional pins (B0-B5) which may be used as outputs or inputs. Any pin used as an output can have from one to seven product terms (AND) summed (OR'D) to it. Each product term can have from one to sixteen variables. In addition, each output and bi-directional pin has an extra product term which may be used to drive those pins into a high impedance state. This allows the six bi-directional pins to be used as inputs if desired. The HPL-77209/16L8 has inverting outputs; the HPL-77215/16H8 has non-inverting outputs, and the HPL-77216/16P8 has the capability for its output polarity to be user determined. Output polarity selection is made possible by the addition of eight extra fuses associated with the eight output/bi-directional pins. The HPL-77216/16P8 is supplied with the polarity fuses intact, causing the outputs to be non-inverting. If a particular polarity fuse is blown, then the output associated with that fuse will be inverting.

Referring to the programming form (Figure 3), it can be seen that the column numbers or product term numbers are listed at the left hand side. Across the top, the row numbers or input variables are listed. In order to include an input variable in a product term, a "1" should be placed in the box at the intersection of the input variable and the product term. Notice that for every product term, if any input variable has both its true and complement forms included, then the entire product term will be unconditionally disabled (A./A=0), and will not contribute to the associated output. If it is desired not to use a product term, then all boxes for that column number should be left blank. Notice that row 32 has the input symbol $\frac{1}{\pm}$, this indicates that this row is at ground potential or logical "0". If a "1" is placed in a box at an intersection of row 32 and an INVERT product term, then the associated output will be non-inverting, if a "0" is used, then the output will be inverting. The polarity of each output can be defined independently of all other outputs.

Each of the six bi-directional pins (B0-B5) has a gray area shown on the programming form at the intersection of their product terms and feedback variables. These gray areas may be used, but a latched or oscillatory condition could occur if a positive or negative feedback loop is formed.

The programming form is shown with all boxes blank which is equivalent to all fuses being blown. HPL devices are supplied with all fuses intact and undesired fuses or connections must be blown.

For information concerning the entry of fuse data from the programming form into a suitable HPL programmer, refer to the operating guide for that programmer.

If it is desired that device programming should be performed by Harris, programming information may be supplied in one or more of the following forms:

1. Master devices (Harris or other)
2. Boolean equations
3. Paper tapes
4. Programming form
5. Marked up logic diagrams (A charge may be made for this entry format)

HARRIS

HPL-77317/16LD8
HPL-77318/16HD8

Preliminary

HPL™ Harris Programmable Logic

Features

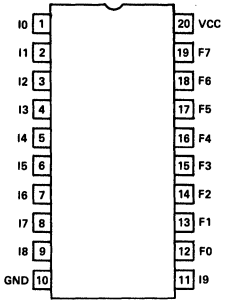
- LOGIC PATHS TESTED TO INSURE FUNCTIONALITY
- FAST ACCESS (INPUT TO OUTPUT) 35 nsec MAX
- LOW ICC 155mA MAX
- ALLOWS SIGNIFICANT PACKAGE COUNT SAVINGS
- 8 PRODUCT TERMS PER OUTPUT
- 20 PIN SLIMLINE DIP
- HIGH SPEED PROGRAMMING PROCEDURE – ONE PULSE/FUSE ASSURES SUPERIOR RELIABILITY
- PROGRAMMABLE SUBSTITUTE FOR TTL SSI/MSI LOGIC CIRCUITS
- REDUCTION OF IC INVENTORIES
- EASE OF PROTOTYPING AND BOARD LAYOUT
- TTL COMPATIBLE INPUTS AND OUTPUTS
- "THREE STATE" OUTPUTS
- THE HARRIS RELIABLE NICKEL-CHROMIUM FUSE TECHNOLOGY
- SUPPORTED BY HELP™ SOFTWARE

Applications

- RANDOM LOGIC REPLACEMENT
- CODE CONVERTERS
- ADDRESS DECODING
- FAULT DETECTORS
- BOOLEAN FUNCTION GENERATORS
- DIGITAL MULTIPLEXERS
- PARITY GENERATORS
- PATTERN RECOGNITION
- ROM PATCHING

Pinout

HPL-77317/318



Description

The HPL-77317/318 are programmable logic devices designed to be cost effective and space saving replacements for discrete logic designs. These devices are two-level logic elements consisting of 8 product terms (AND) summed (OR) together to generate each of the 8 outputs. To achieve 8 product terms per output, the ability to force the outputs to a high impedance state has not been included. All eight outputs are permanently active.

The HPL-77317 is similar to the industry standard 16L8, and implements logic expressions of the Inverted Sum Of Products (ISOP) form.

The HPL-77318 is a similar device to the HPL-77317, but does not include the associated output inversion. It implements logic expressions of the Sum Of Products (SOP) form.

Six of the 8 outputs feature feedback into the fuse matrix, allowing output functions to be utilized for other output functions.

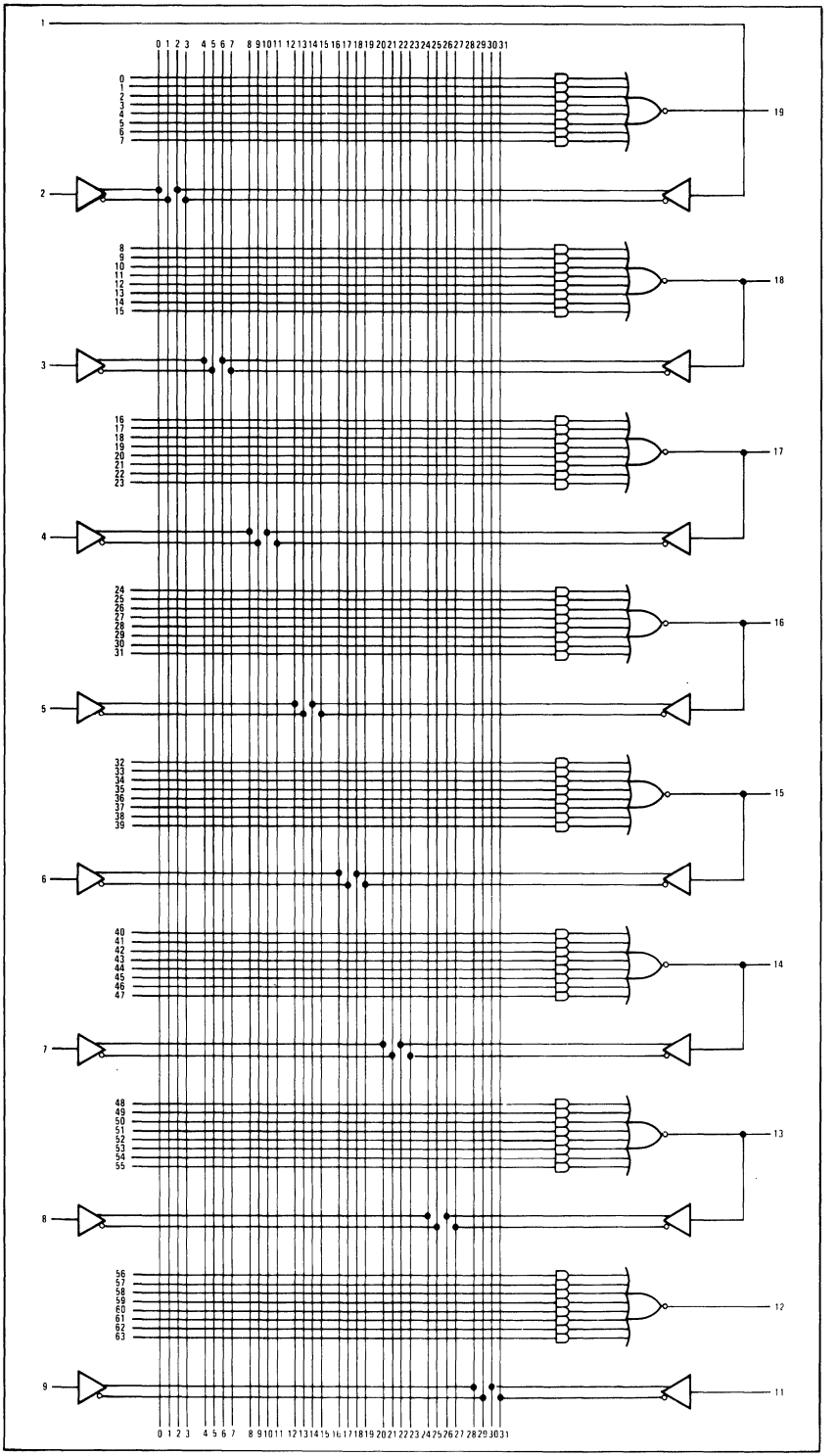
The HPL-77317/318 are field programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

Nickel-chromium fuse technology is used on these and all other HARRIS HPL-77XXX programmable logic devices. The HPL-77317/318 are available in 20 pin slimline DIP packages with pinouts similar to the 16L8.

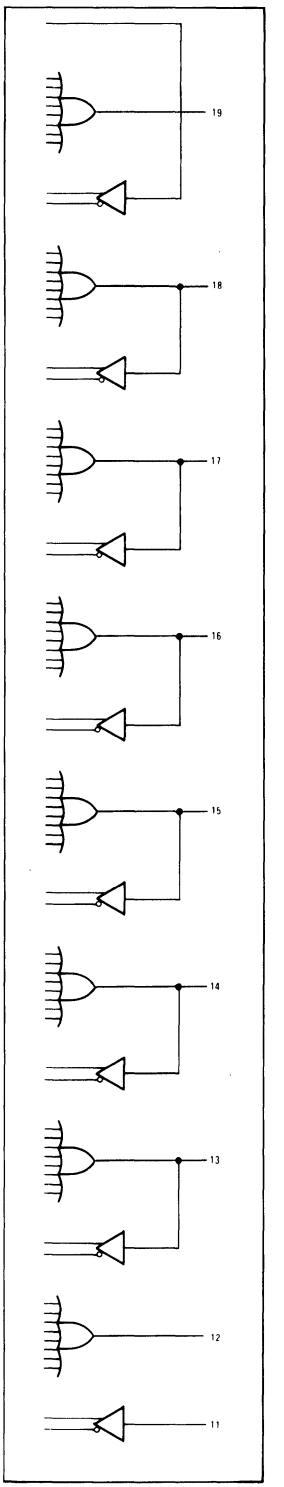
The HPL-77317/318 contain unique test circuitry developed by HARRIS, which is enabled at the time of manufacture to allow complete AC, DC and functional testing.

CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
HPL is a trademark of Harris Corporation.
HELP is a trademark of Harris Corporation.

HPL-77317/16LD8



HPL-77318/16HD8



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+7V	Storage Temperature	−65°C to +150°C
Input Voltage	+5.5V	Operating Temperature (Ambient)	
Output Voltage	+5.5V	Commercial	0°C to +75°C
Input Current	−20mA	Military	−55°C to +125°C
Output Sink Current	+100mA	Maximum Junction Temperature	
		Commercial	+150°C
		Military	+175°C

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, following the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HPL-77317/318 -5 (V_{CC} = 5.0V+5%, T_A = 0°C to +75°C)
HPL-77317/318 -2/-8 (V_{CC} = 5.0V+10%, T_A = -55°c to +125°C)

SYMBOL	PARAMETER		MIN	MAX	UNITS	TEST CONDITIONS	
I_{IH} I_{IL}	Input Current Dedicated Input	"1" "0"	— —	+25 −100	μA μA	V_{IH} = V_{CC} MAX V_{IL} 0.4 V	V_{CC} = V_{CC} MAX
V_{IH} V_{IL}	Input Threshold Voltage (1)	"1" "0"	2.0 —	— 0.8	V V	V_{CC} = V_{CC} MAX V_{CC} = V_{CC} MIN	
V_{OH}	High-Level Output Voltage		2.4	—	V	V_{CC} = V_{CC} MIN	I_{OH} = −2.0mA (M) I_{OH} = −3.2mA (C)
V_{OL}	Low-Level Output Voltage		—	0.5	V	V_{IL} = 0.8V V_{IH} = 2.0V	I_{OL} = +16mA (M) I_{OL} = +24mA (C) (1)
V_{CL}	Input Clamp Voltage (2)		—	−1.2	V	I_{IN} = −18mA, V_{CC} = OV	
I_{OS}	Output Short Circuit Current		−30	−130	mA	V_{CC} = 5.0V, V_{OUT} = OV One Output for MAX of One Sec.	
I_{CC}	Power Supply Current		— —	155 (C) 165 (M)	mA mA	V_{CC} = V_{CC} MAX	

C = Commercial (-5) M = Military (-2/-8)

(1) These specifications apply to both Input (I) & Bi-directional (B) pins. These are absolute voltages with respect to ground pin & include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

(2) One output at a time, otherwise 16mA.

A. C. SWITCHING CHARACTERISTICS (Operating)

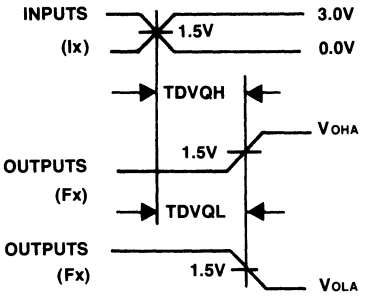
SYMBOL			HPL-77317−5 HPL-77318−5 5V±5% 0°C to +75°C		HPL-77317−2/−8 HPL-77318−2/−8 5V±10% −55°C to +125°C		
JEDEC STANDARD	OLD SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS
TDVQH	T_{PD}	Propagation Delay – Input to Active High Output	—	35	—	45	ns
TDVQL	T_{PD}	Propagation Delay – Input to Active Low Output	—	35	—	45	ns

NOTE: Maximum test frequency is 5MHz with a 50% duty cycle.

CAPACITANCE: T_A = 25°C (NOTE: Sampled and guaranteed – but not 100% tested.)

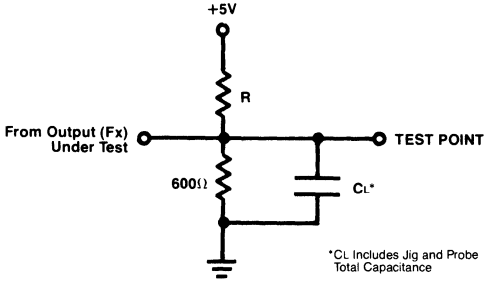
SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_I	Input Capacitance	12	pF	V_{CC} = 5.0V, V_I = 2.0V, f = 1 MHz
C_F	Output Capacitance	15	pF	V_{CC} = 5.0V, V_F = V_{OL} or V_{OH}, f = 1 MHz

SWITCHING TIME DEFINITIONS



INPUT CONDITIONS: t_r, t_f = 5ns (10% to 90%)

AC TEST LOAD



This simulates the A.C. Test Load which Harris Semiconductor uses in its automatic test equipment, and it is recommended that users of Harris bipolar devices use the same or an equivalent load in performing A.C. testing.

SYMBOL	PARAMETER	R(Ω)	C_L (pF)
TDVQH	Propagation Delay from Input to Active High Output	300	50
TDVQL	Propagation Delay from Input to Active Low Output	300	50

Following is the programming procedure which is used for the HPL-77317/318 devices. These devices are manufactured with all fuses intact. Any desired fuse can be programmed by following the simple procedure shown on the following page. One may build a programmer to satisfy the specifications described in the table, or use any of the commercially available programmers which meet these specifications.

PROGRAMMING SPECIFICATIONS

TABLE 1

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
V_{CCP}	Vcc Supply During Programming[1]		8.25	8.5	8.75	V
I_{CCP}	Icc Limit During Programming		550	—	1000	mA
V_{IH}	Input Voltage (High)		2.4	—	5.5	V
V_{IL}	Input Voltage (Low)		0.0	—	0.8	V
I_{IHP}	Input Current (High) During Prog.	V_{IH} = +5.5V	—	—	50	μA
I_{ILP}	Input Current (Low) During Prog.	V_{IL} = 0V	—	—	−500	μA
V_{OPF}	Forced Output Voltage[2]	Transient or Steady State	16.0	16.5	18.0	V
I_{OPF}	Forced Output Current		—	100	325	mA
PW_V	Verify Pulse Width		1	5	50	μS
PW_P	Programming Pulse Width		90	100	110	μS
T_D	Pulse Sequence Delay		1	5	50	μS
t_{r2}	Forced Output Voltage Rise Time	10% to 90%	4	14	40	μS
t_{r1}	Vcc Supply Rise Time	10% to 90%	2	7	20	μS
t_{f2}	Forced Output Voltage Fall Time	90% to 10%	2	7	20	μS
t_{f1}	Vcc Supply Fall Time	90% to 10%	1	4	10	μS
T_{PP}	Programming Period		100	160	350	μS
F_L	Fusing Attempts per Link		—	1	2	Cycle
V_S	Verify Threshold[3]		1.4	1.5	1.6	V

NOTES:

1. Bypass VCC to GND with a 0.01 μF capacitor to reduce voltage spikes. The VCC power supply must be capable of handling 1 Ampere maximum.
2. Care should be taken to ensure that the voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.
3. VS is the sensing threshold of the device output voltage for a programmed link. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.

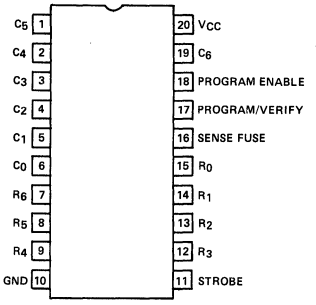


Figure 1
EDIT MODE PINOUT
HPL-77317/318

NOTE: While programming the HPL-77317/318 no pins should be left floating. Pin 16 (SENSE FUSE) appears as an open collector output during programming. It should be tied to VCC through a 10K ohm resistor.

PROGRAMMING PROCEDURE

1. Set-Up:
   a. During programming, no pins should be left floating. Pin 16 should be terminated with a 10k ohm resistor to V_{CC}.
   b. Set GND (Pin 10) to OV.
2. Select the EDIT Mode:
   a. Apply OV to Pin 20.
   b. Apply V_{IL} to Pin 18.
   c. Apply V_{IH} to Pin 11.
   d. Apply V_{IL} to Pin 17.
3. Select the Fuse to be Programmed:
   a. Wait T_D and select a ROW by specifying the appropriate binary ROW address according to Table 2.
   b. Select a COLUMN by specifying the appropriate binary COLUMN address according to Table 3.
4. Program the Fuse:
   a. Wait T_D and raise Pin 20 to V_{CCP}.
   b. Wait T_D and raise Pin 17 to V_{IH}.
   c. Wait T_D and raise Pin 18 to V_{OPF}.
   d. Wait T_D and pulse Pin 11 to V_{IL} for a duration of PWp.
   e. Return Pin 11 to V_{IH}.
   f. Wait T_D and lower Pin 18 to V_{IL}.
   g. Wait T_D and lower Pin 17 to V_{IL}.
5. Verify Programmed Fuse:
   a. Wait T_D and lower Pin 11 to V_{IL}.
   b. At the end of PW_V, monitor Pin 16 for a level of V_S.
   c. Return Pin 11 to V_{IH}.
   d. Wait T_D and lower Pin 20 to OV.
   e. If Pin 16 has indicated a V_{OL}, return to step 4 and repeat so that the fuse receives a maximum of two (2) fusing attempts.
6. Repeat Steps 3 Through 5 for All Fuses to be Blown.

PROGRAMMING WAVEFORMS

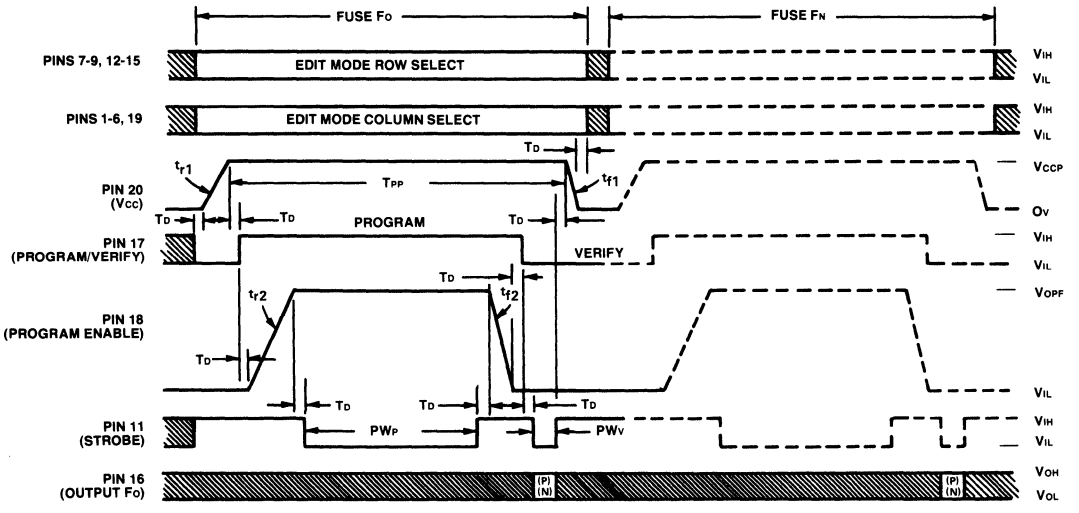


Figure 2

TABLE 2
EDIT MODE ROW SELECT

ROW NUMBER	R5 Pin 8	R4 Pin 9	R3 Pin 12	R2 Pin 13	R1 Pin 14	R0 Pin 15	VARIABLE
0	L	L	L	L	L	L	I1
1	L	L	L	L	L	H	$\overline{I1}$
2	L	L	L	L	H	L	I0
3	L	L	L	L	H	H	$\overline{I0}$
4	L	L	L	H	L	L	I2
5	L	L	L	H	L	H	$\overline{I2}$
6	L	L	L	H	H	L	F6
7	L	L	L	H	H	H	$\overline{F6}$
8	L	L	H	L	L	L	I3
9	L	L	H	L	L	H	$\overline{I3}$
10	L	L	H	L	H	L	F5
11	L	L	H	L	H	H	$\overline{F5}$
12	L	L	H	H	L	L	I4
13	L	L	H	H	L	H	$\overline{I4}$
14	L	L	H	H	H	L	F4
15	L	L	H	H	H	H	$\overline{F4}$
16	L	H	L	L	L	L	I5
17	L	H	L	L	L	H	$\overline{I5}$
18	L	H	L	L	H	L	F3
19	L	H	L	L	H	H	$\overline{F3}$
20	L	H	L	H	L	L	I6
21	L	H	L	H	L	H	$\overline{I6}$
22	L	H	L	H	H	L	F2
23	L	H	L	H	H	H	$\overline{F2}$
24	L	H	H	L	L	L	I7
25	L	H	H	L	L	H	$\overline{I7}$
26	L	H	H	L	H	L	F1
27	L	H	H	L	H	H	$\overline{F1}$
28	L	H	H	H	L	L	I8
29	L	H	H	H	L	H	$\overline{I8}$
30	L	H	H	H	H	L	I9
31	L	H	H	H	H	H	$\overline{I9}$

NOTES:
(1) Pin 7 (R6) is used for programming other HPL devices and should be held at or less than VIL during programming.
(2) $0V \leq L \leq V_{IL}$
$V_{IH} \leq H \leq 5v$

TABLE 3
EDIT MODE COLUMN SELECT

COLUMN NUMBER	C6 Pin 19	C5 Pin 1	C4 Pin 2	C3 Pin 3	C2 Pin 4	C1 Pin 5	C0 Pin 6	PART NUMBER
0	L	L	L	L	L	L	L	
1	L	L	L	L	L	L	H	
2	L	L	L	L	L	H	L	
3	L	L	L	L	L	H	H	
4	L	L	L	L	H	L	L	
5	L	L	L	L	H	L	H	
6	L	L	L	L	H	H	L	
7	L	L	L	L	H	H	H	
8	L	L	L	H	L	L	L	
9	L	L	L	H	L	L	H	
10	L	L	L	H	L	H	L	
11	L	L	L	H	L	H	H	
12	L	L	L	H	H	L	L	
13	L	L	L	H	H	L	H	
14	L	L	L	H	H	H	L	
15	L	L	L	H	H	H	H	
16	L	L	H	L	L	L	L	
17	L	L	H	L	L	L	H	
18	L	L	H	L	L	H	L	
19	L	L	H	L	L	H	H	
20	L	L	H	L	H	L	L	
21	L	L	H	L	H	L	H	HPL-77317
22	L	L	H	L	H	H	L	HPL-77318
23	L	L	H	L	H	H	H	
24	L	L	H	H	L	L	L	
25	L	L	H	H	L	L	H	
26	L	L	H	H	L	H	L	
27	L	L	H	H	L	H	H	
28	L	L	H	H	H	L	L	
29	L	L	H	H	H	L	H	
30	L	L	H	H	H	H	L	
31	L	L	H	H	H	H	H	
32	L	H	L	L	L	L	L	
33	L	H	L	L	L	L	H	
34	L	H	L	L	L	H	L	
35	L	H	L	L	L	H	H	
36	L	H	L	L	H	L	L	
37	L	H	L	L	H	L	H	
38	L	H	L	L	H	H	L	
39	L	H	L	L	H	H	H	
40	L	H	L	H	L	L	L	
41	L	H	L	H	L	L	H	
42	L	H	L	H	L	H	L	
43	L	H	L	H	L	H	H	
44	L	H	L	H	H	L	L	
45	L	H	L	H	H	L	H	
46	L	H	L	H	H	H	L	
47	L	H	L	H	H	H	H	
48	L	H	H	L	L	L	L	
49	L	H	H	L	L	L	H	
50	L	H	H	L	L	H	L	
51	L	H	H	L	L	H	H	
52	L	H	H	L	H	L	L	
53	L	H	H	L	H	L	H	
54	L	H	H	L	H	H	L	
55	L	H	H	L	H	H	H	
56	L	H	H	H	L	L	L	
57	L	H	H	H	L	L	H	
58	L	H	H	H	L	H	L	
59	L	H	H	H	L	H	H	
60	L	H	H	H	H	L	L	
61	L	H	H	H	H	L	H	
62	L	H	H	H	H	H	L	
63	L	H	H	H	H	H	H	

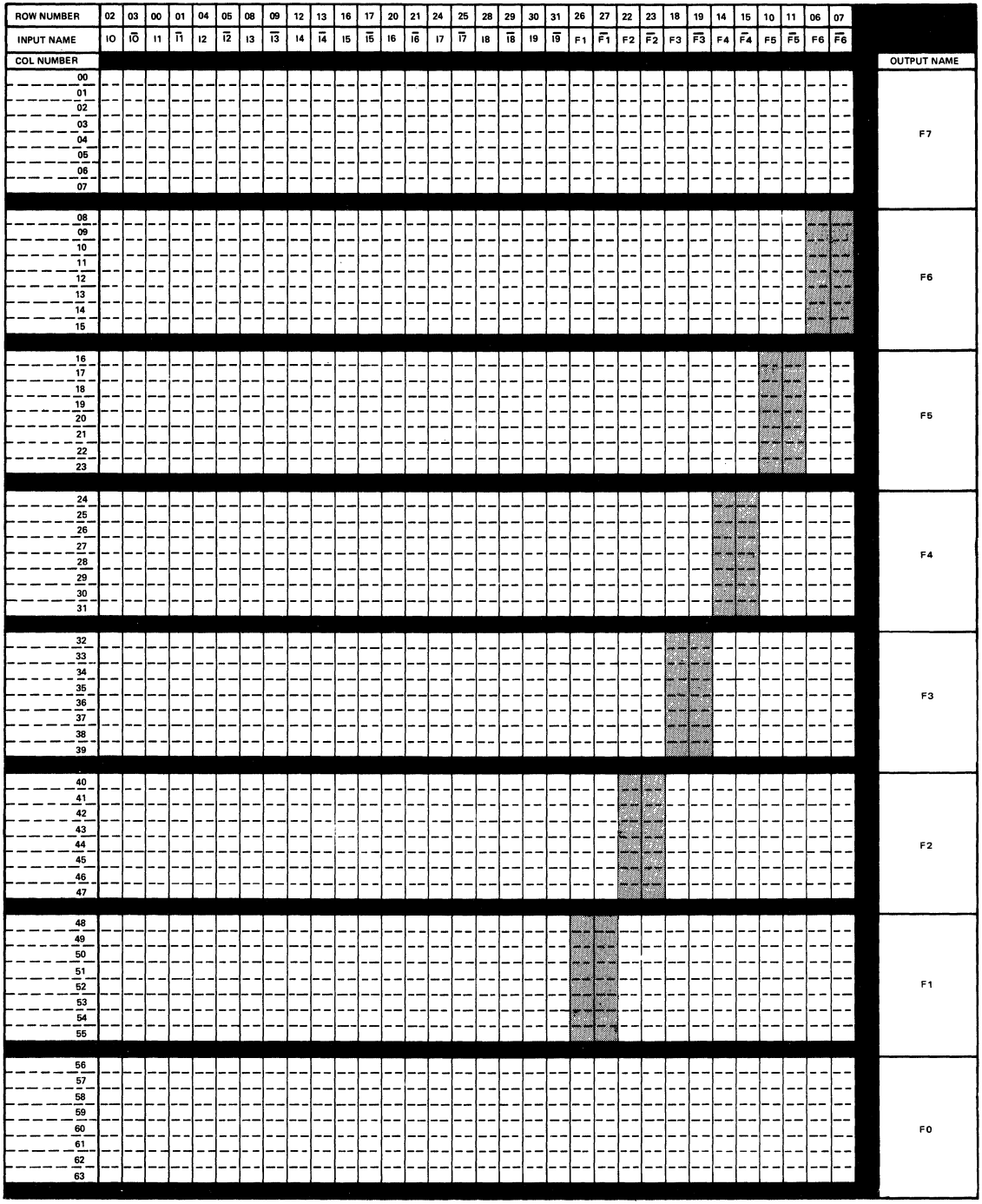

ROW NUMBER
02 03 00 01 04 05 08 09 12 13 16 17 20 21 24 25 28 29 30 31 26 27 22 23 18 19 14 15 10 11 06 07
INPUT NAME
I0 Ī0 I1 Ī1 I2 Ī2 I3 Ī3 I4 Ī4 I5 Ī5 I6 Ī6 I7 Ī7 I8 Ī8 I9 Ī9 F1 F̄1 F2 F̄2 F3 F̄3 F4 F̄4 F5 F̄5 F6 F̄6
COL NUMBER
OUTPUT NAME
00 01 02 03 04 05 06 07
F7
08 09 10 11 12 13 14 15
F6
16 17 18 19 20 21 22 23
F5
24 25 26 27 28 29 30 31
F4
32 33 34 35 36 37 38 39
F3
40 41 42 43 44 45 46 47
F2
48 49 50 51 52 53 54 55
F1
56 57 58 59 60 61 62 63
F0

Figure 3

USE OF THE PROGRAMMING FORM

The programming form for the HPL-77317/318 is shown in Figure 3. Both devices have eight output pins (F0-F7). Any output can have from one to eight product terms (AND) summed (OR'D) to it. Each product term can have from one to sixteen variables. The HPL-77317/16LD8 has inverting outputs; the HPL-77318/16HD8 has non-inverting outputs.

Referring to the programming form (Figure 3), it can be seen that the column numbers or product term numbers are listed at the left hand side. Across the top, the row numbers or input variables are listed. In order to include an input variable in a product term, a "1" should be placed in the box at the intersection of the input variable and the product term. Notice that for every product term, if any input variable has both its true and complement forms included, then the entire product term will be unconditionally disabled (A./A=0), and will not contribute to the associated output. If it is desired not to use a product term, then all boxes for that column number should be left blank.

Six of the eight output pins (F1-F6) have a gray area shown on the programming form at the intersection of their product terms and feedback variables. These gray areas may be used, but a latched or oscillatory condition could occur if a positive or negative feedback loop is formed.

The programming form is shown with all boxes blank which is equivalent to all fuses being blown. HPL devices are supplied with all fuses intact and undesired fuses or connections must be blown.

For information concerning the entry of fuse data from the programming form into a suitable HPL programmer, refer to the operating guide for that programmer.

If it is desired that device programming should be performed by Harris, programming information may be supplied in one of more of the following forms:

1. Master devices (Harris or other)
2. Boolean equations
3. Paper tapes
4. Programming form
5. Marked up logic diagrams (A substantial charge may be made for this entry format)

HARRIS

HPL-77319/16LE8
HPL-77320/16HE8

Preliminary

HPL™ Harris Programmable Logic

Features

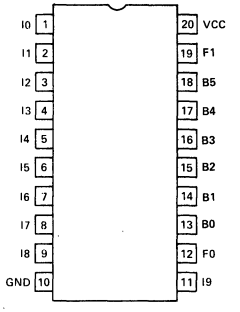
- LOGIC PATHS TESTED TO ENSURE FUNCTIONALITY
- FAST ACCESS (INPUT TO OUTPUT) 35 nsec MAX
- LOW ICC 155mA MAX
- ALLOWS SIGNIFICANT PACKAGE COUNT SAVINGS
- 8 PRODUCT TERMS PER OUTPUT
- 20 PIN SLIMLINE DIP
- HIGH SPEED PROGRAMMING PROCEDURE-ONE PULSE/FUSE ASSURES SUPERIOR RELIABILITY
- ENHANCED VERSIONS OF HPL77317/16LD8 AND HPL77318/16HD8
- PROGRAMMABLE SUBSTITUTE FOR TTL SSI MSI LOGIC CIRCUITS
- REDUCTION OF IC INVENTORIES
- EASE OF PROTOTYPING AND BOARD LAYOUT
- TTL COMPATIBLE INPUTS AND OUTPUTS
- "THREE STATE" OUTPUTS
- PROGRAMMABLE OUTPUT POLARITY
- THE HARRIS RELIABLE NICKEL-CHROMIUM FUSE TECHNOLOGY
- SUPPORTED BY HELP™ SOFTWARE

Applications

- RANDOM LOGIC REPLACEMENT
- CODE CONVERTERS
- ADDRESS DECODING
- FAULT DETECTORS
- BOOLEAN FUNCTION GENERATORS
- DIGITAL MULTIPLEXERS
- PARITY GENERATORS
- PATTERN RECOGNITION
- ROM PATCHING

Pinout

HPL-77319/320



Description

The HPL-77319/320 are programmable logic devices designed to be cost effective and space saving replacements for discrete logic designs. These devices are two-level logic elements consisting of 8 product terms (AND) summed (OR) together to generate each of the 8 outputs. An extra fuse associated with each bi-directional pin can drive it to a high impedance state allowing 6 (B0-B5) of the 8 outputs to be used as inputs.

An extra fuse associated with each output pin can be used to control output polarity which is active high on an unprogrammed part.

The HPL-77319 is similar to the industry standard 16L8, and implements logic expressions of the Inverted Sum of Products (ISOP) form.

The HPL-77320 is a similar device to the HPL-77319 but does not include the associated output inversion. It implements logic expressions of the Sum of Products (SOP) form.

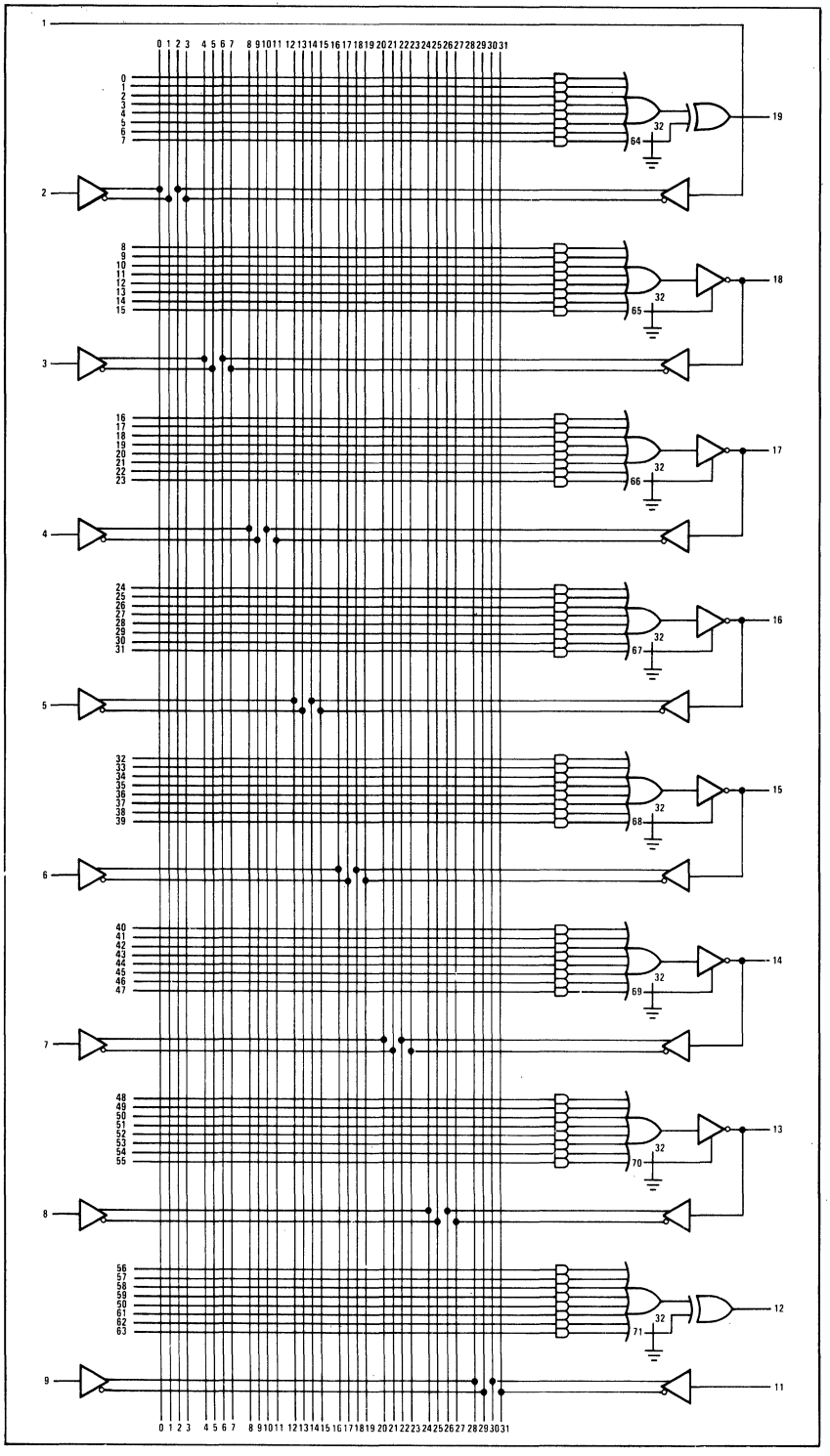
The HPL-77319/320 are field programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

Nickel-chromium fuse technology is used on these and all other HARRIS HPL-77XXX programmable logic devices. The HPL-77319/320 are available in 20 pin slimline DIP packages with pinouts identical to 16L8.

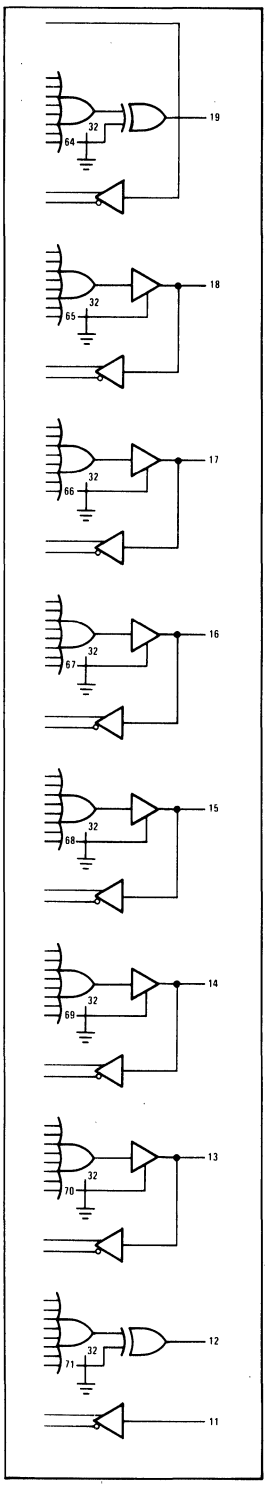
The HPL-77319/320 contain unique test circuitry developed by HARRIS which is enabled at the time of manufacture to allow complete AC, DC and functional testing.

CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I. C. handling procedures should be followed.
HPL is a trademark of Harris Corporation
HELP is a trademark of Harris Corporation.

HPL-77319/16LE8



HPL-77320/16HE8



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+7V	Storage Temperature	−65°C to +150°C
Input Voltage	+5.5V	Operating Temperature (Ambient)	
Output Voltage	+5.5V	Commercial	0°C to +75°C
Input Current	−20mA	Military	−55°C to +125°C
Output Sink Current	+100mA	Maximum Junction Temperature	
		Commercial	+150°C
		Military	+175°C

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, following the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HPL-77319/320-5 (V_{CC} = 5.0V±5%, T_A = 0°C to +75°C)
HPL-77319/320-2/-8 (V_{CC} = 5.0V±10%, T_A = −55°C to +125°C)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS	
I_{IH}	Input Current "1"	—	+25	µA	V_{IH} = V_{CC} MAX	
I_{IL}	Dedicated Input "0"	—	−100	µA	V_{IL} = 0.4 V	V_{CC} = V_{CC} MAX
I_{BZH}	"1"	—	+40	µA	V_{BH} = V_{CC} MAX	
	Bidirectional Pin Current					V_{CC} = V_{CC} MAX
I_{BZL}	Hi-Z State "0"	—	−100	µA	V_{BL} = 0.4V	
V_{IH}	"1"	2.0	—	V	V_{CC} = V_{CC} MAX	
	Input Threshold (1)					
V_{IL}	Voltage "0"	—	0.8	V	V_{CC} = V_{CC} MIN	
V_{OH}	High-Level Output Voltage (2)	2.4	—	V	V_{CC} = V_{CC} MIN	I_{OH} = −2.0mA (M) I_{OH} = −3.2mA (C)
V_{OL}	Low-Level Output Voltage (2)	—	0.5	V	V_{IL} = 0.8V V_{IH} = 2.0V	I_{OL} = +16mA (M) I_{OL} = +24mA (C) (3)
V_{CL}	Input Clamp Voltage (1)	—	−1.2	V	I_{IN} = −18mA, V_{CC} = OV	
I_{OS}	Output Short Circuit Current (2)	−30	−130	mA	V_{CC} = 5.0V, V_{OUT} = OV One Output for MAX of One Sec.	
I_{CC}	Power Supply Current	—	155 (C)	mA	V_{CC} = V_{CC} MAX	
		—	165 (M)	mA		

C = Commercial (-5) M = Military (-2/-8)

(1) These specifications apply to both input (I) and Bi-directional (B) pins.These are absolute voltages with respect to ground pin & include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

(2) These specifications apply to both Output (F) and Bi-directional (B) pins.

(3) One output at a time, otherwise 16mA.

A. C. SWITCHING CHARACTERISTICS (Operating)

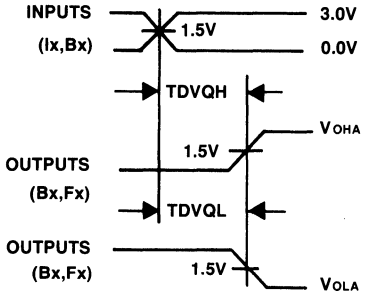
			HPL-77319-5 HPL-77320-5 5V±5% 0°C to +75°C		HPL-77319-2/-8 HPL-77320-2/-8 5V±10% −55°C to +125°C		
SYMBOL							
JEDEC STANDARD	OLD SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS
TDVQH	T_{PD}	Propagation Delay – Input or I/O to Active High Output	—	35	—	45	ns
TDVQL	T_{PD}	Propagation Delay – Input or I/O to Active Low Output	—	35	—	45	ns

NOTE: Maximum test frequency is 5MHz with a 50% duty cycle.

CAPACITANCE: T_A = 25°C (NOTE: Sampled and guaranteed – but not 100% tested.)

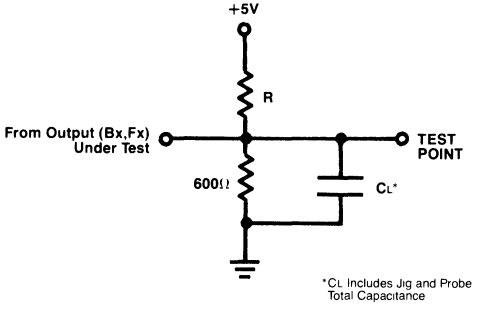
SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_I	Input Capacitance	12	pF	V_{CC} = 5.0V, V_I = 2.0V, f = 1 MHz
C_F	Output Capacitance	15	pF	V_{CC} = 5.0V, V_F = V_{OL} or V_{OH}, f = 1 MHz
C_B	Bidirectional Pin Cap.	15	pF	V_{CC} = 5.0V, V_B = 2.0V, f = 1 MHz

SWITCHING TIME DEFINITIONS



INPUT CONDITIONS: t_r, t_f = 5ns (10% to 90%)

AC TEST LOAD



This simulates the A.C. Test Load which Harris Semiconductor uses in its automatic test equipment, and it is recommended that users of Harris bipolar devices use the same or an equivalent load in performing A.C. testing.

SYMBOL	PARAMETER	R(Ω)	C_L (pF)
TDVQH	Propagation Delay from Input or I/O to Active High Output	300	50
TDVQL	Propagation Delay from Input or I/O to Active Low Output	300	50

Following is the programming procedure which is used for the HPL-77319/320 devices. These devices are manufactured with all fuses intact. Any desired fuse can be programmed by following the simple procedure shown on the following page. One may build a programmer to satisfy the specifications described in the table, or use any of the commercially available programmers which meet these specifications.

PROGRAMMING SPECIFICATIONS

TABLE 1

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
V_{CCP}	Vcc Supply During Programming[1]		8.25	8.5	8.75	V
I_{CCP}	Icc Limit During Programming		550	—	1000	mA
V_{IH}	Input Voltage (High)		2.4	—	5.5	V
V_{IL}	Input Voltage (Low)		0.0	—	0.8	V
I_{IHP}	Input Current (High) During Prog.	V_{IH} = +5.5V	—	—	50	μA
I_{ILP}	Input Current (Low) During Prog.	V_{IL} = 0V	—	—	−500	μA
V_{OPF}	Forced Output Voltage[2]	Transient or Steady State	16.0	16.5	18.0	V
I_{OPF}	Forced Output Current		—	100	325	mA
PWv	Verify Pulse Width		1	5	50	μS
PWp	Programming Pulse Width		90	100	110	μS
TD	Pulse Sequence Delay		1	5	50	μS
t_{r2}	Forced Output Voltage Rise Time	10% to 90%	4	14	40	μS
t_{r1}	Vcc Supply Rise Time	10% to 90%	2	7	20	μS
t_{f2}	Forced Output Voltage Fall Time	90% to 10%	2	7	20	μS
t_{f1}	Vcc Supply Fall Time	90% to 10%	1	4	10	μS
TPP	Programming Period		100	160	350	μS
FL	Fusing Attempts per Link		—	1	2	Cycle
Vs	Verify Threshold[3]		1.4	1.5	1.6	V

NOTES:

1. Bypass VCC to GND with a 0.01 μF capacitor to reduce voltage spikes. The VCC power supply must be capable of handling 1 Ampere maximum.
2. Care should be taken to ensure that the voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.
3. VS is the sensing threshold of the device output voltage for a programmed link. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.

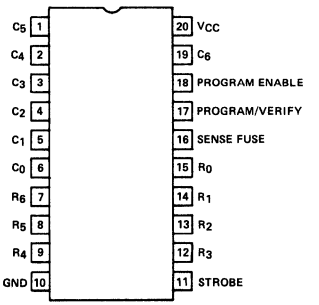


Figure 1
EDIT MODE PINOUT
HPL-77319/320

NOTE: While programming the HPL-77319/320 no pins should be left floating. Pin 16 (SENSE FUSE) appears as an open collector output during programming. It should be tied to VCC through 10K ohm resistor.

PROGRAMMING PROCEDURE

1. Set-Up:
   a. During programming, no pins should be left floating. Pin 16 should be terminated with a 10k ohm resistor to V_{CC}.
   b. Set GND (Pin 10) to OV.
2. Select the EDIT Mode:
   a. Apply OV to Pin 20.
   b. Apply V_{IL} to Pin 18.
   c. Apply V_{IH} to Pin 11.
   d. Apply V_{IL} to Pin 17.
3. Select the Fuse to be Programmed:
   a. Wait T_D and select a ROW by specifying the appropriate binary ROW address according to Table 2.
   b. Select a COLUMN by specifying the appropriate binary COLUMN address according to Table 3.
4. Program the Fuse:
   a. Wait T_D and raise Pin 20 to V_{CCP}.
   b. Wait T_D and raise Pin 17 to V_{IH}.
   c. Wait T_D and raise Pin 18 to V_{OPF}.
   d. Wait T_D and pulse Pin 11 to V_{IL} for a duration of PWp.
   e. Return Pin 11 to V_{IH}.
   f. Wait T_D and lower Pin 18 to V_{IL}.
   g. Wait T_D and lower Pin 17 to V_{IL}.
5. Verify Programmed Fuse:
   a. Wait T_D and lower Pin 11 to V_{IL}.
   b. At the end of PW_V, monitor Pin 16 for a level of Vs.
   c. Return Pin 11 to V_{IH}.
   d. Wait T_D and lower Pin 20 to OV.
   e. If Pin 16 has indicated a V_{OL}, return to step 4 and repeat so that the fuse receives a maximum of two (2) fusing attempts.
6. Repeat Steps 3 Through 5 for All Fuses to be Blown.

PROGRAMMING WAVEFORMS

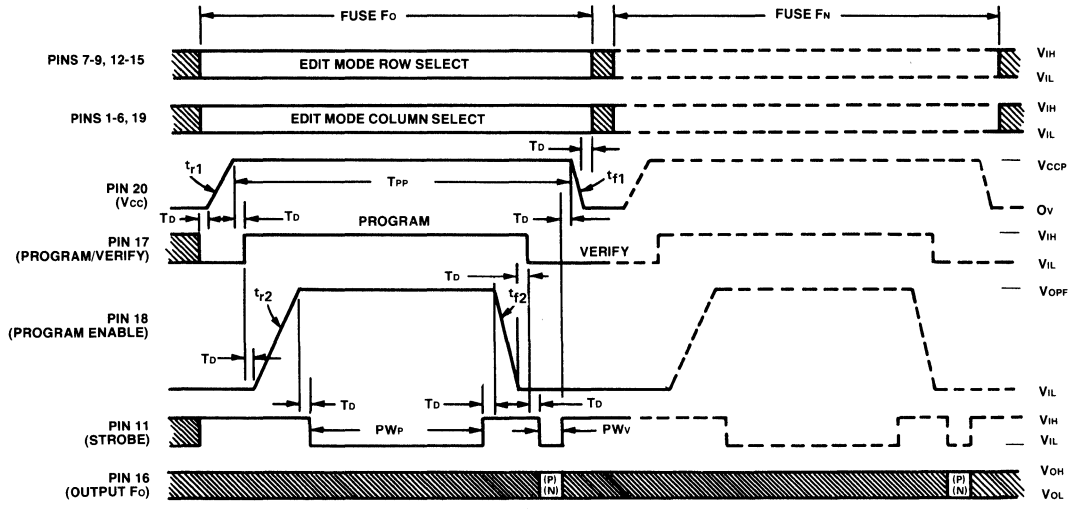


Figure 2

TABLE 2
EDIT MODE ROW SELECT

ROW NUMBER	R5 Pin 8	R4 Pin 9	R3 Pin 12	R2 Pin 13	R1 Pin 14	R0 Pin 15	VARIABLE
0	L	L	L	L	L	L	I1
1	L	L	L	L	L	H	$\overline{I1}$
2	L	L	L	L	H	L	I0
3	L	L	L	L	H	H	$\overline{I0}$
4	L	L	L	H	L	L	I2
5	L	L	L	H	L	H	$\overline{I2}$
6	L	L	L	H	H	L	B5
7	L	L	L	H	H	H	$\overline{B5}$
8	L	L	H	L	L	L	I3
9	L	L	H	L	L	H	$\overline{I3}$
10	L	L	H	L	H	L	B4
11	L	L	H	L	H	H	$\overline{B4}$
12	L	L	H	H	L	L	I4
13	L	L	H	H	L	H	$\overline{I4}$
14	L	L	H	H	H	L	B3
15	L	L	H	H	H	H	$\overline{B3}$
16	L	H	L	L	L	L	I5
17	L	H	L	L	L	H	$\overline{I5}$
18	L	H	L	L	H	L	B2
19	L	H	L	L	H	H	$\overline{B2}$
20	L	H	L	H	L	L	I6
21	L	H	L	H	L	H	$\overline{I6}$
22	L	H	L	H	H	L	B1
23	L	H	L	H	H	H	$\overline{B1}$
24	L	H	H	L	L	L	I7
25	L	H	H	L	L	H	$\overline{I7}$
26	L	H	H	L	H	L	B0
27	L	H	H	L	H	H	$\overline{B0}$
28	L	H	H	H	L	L	I8
29	L	H	H	H	L	H	$\overline{I8}$
30	L	H	H	H	H	L	I9
31	L	H	H	H	H	H	$\overline{I9}$
32	H	L	L	L	L	L	CONFIGURE

NOTES:

(1) Row number 32 should only be selected when programming the **configuration fuses.**

(2) Pin 7 (R6) is used for programming other HPL devices and should be held at or less than VIL during programming.

(3) $0V \leq L \leq V_{IL}$
$V_{IH} \leq H \leq 5v$

TABLE 3
EDIT MODE COLUMN SELECT

COLUMN NUMBER	C6 Pin 19	C5 Pin 1	C4 Pin 2	C3 Pin 3	C2 Pin 4	C1 Pin 5	C0 Pin 6	PART NUMBER
0	L	L	L	L	L	L	L	
1	L	L	L	L	L	L	H	
2	L	L	L	L	L	H	L	
3	L	L	L	L	L	H	H	
4	L	L	L	L	H	L	L	
5	L	L	L	L	H	L	H	
6	L	L	L	L	H	H	L	
7	L	L	L	L	H	H	H	
8	L	L	L	H	L	L	L	
9	L	L	L	H	L	L	H	
10	L	L	L	H	L	H	L	
11	L	L	L	H	L	H	H	
12	L	L	L	H	H	L	L	
13	L	L	L	H	H	L	H	
14	L	L	L	H	H	H	L	
15	L	L	L	H	H	H	H	
16	L	L	H	L	L	L	L	
17	L	L	H	L	L	L	H	
18	L	L	H	L	L	H	L	
19	L	L	H	L	L	H	H	
20	L	L	H	L	H	L	L	
21	L	L	H	L	H	L	H	HPL77319
22	L	L	H	L	H	H	L	HPL77320
23	L	L	H	L	H	H	H	
24	L	L	H	H	L	L	L	
25	L	L	H	H	L	L	H	
26	L	L	H	H	L	H	L	
27	L	L	H	H	L	H	H	
28	L	L	H	H	H	L	L	
29	L	L	H	H	H	L	H	
30	L	L	H	H	H	H	L	
31	L	L	H	H	H	H	H	
32	L	H	L	L	L	L	L	
33	L	H	L	L	L	L	H	
34	L	H	L	L	L	H	L	
35	L	H	L	L	L	H	H	
36	L	H	L	L	H	L	L	
37	L	H	L	L	H	L	H	
38	L	H	L	L	H	H	L	
39	L	H	L	L	H	H	H	
40	L	H	L	H	L	L	L	
41	L	H	L	H	L	L	H	
42	L	H	L	H	L	H	L	
43	L	H	L	H	L	H	H	
44	L	H	L	H	H	L	L	
45	L	H	L	H	H	L	H	
46	L	H	L	H	H	H	L	
47	L	H	L	H	H	H	H	
48	L	H	H	L	L	L	L	
49	L	H	H	L	L	L	H	
50	L	H	H	L	L	H	L	
51	L	H	H	L	L	H	H	
52	L	H	H	L	H	L	L	
53	L	H	H	L	H	L	H	
54	L	H	H	L	H	H	L	
55	L	H	H	L	H	H	H	
56	L	H	H	H	L	L	L	
57	L	H	H	H	L	L	H	
58	L	H	H	H	L	H	L	
59	L	H	H	H	L	H	H	
60	L	H	H	H	H	L	L	
61	L	H	H	H	H	L	H	
62	L	H	H	H	H	H	L	
63	L	H	H	H	H	H	H	
64	H	L	L	L	L	L	L	
65	H	L	L	L	L	L	H	
66	H	L	L	L	L	H	L	
67	H	L	L	L	L	H	H	
68	H	L	L	L	H	L	L	ROW 32 ONLY
69	H	L	L	L	H	L	H	
70	H	L	L	L	H	H	L	
71	H	L	L	L	H	H	H	

Programming Form HPL-77319/320

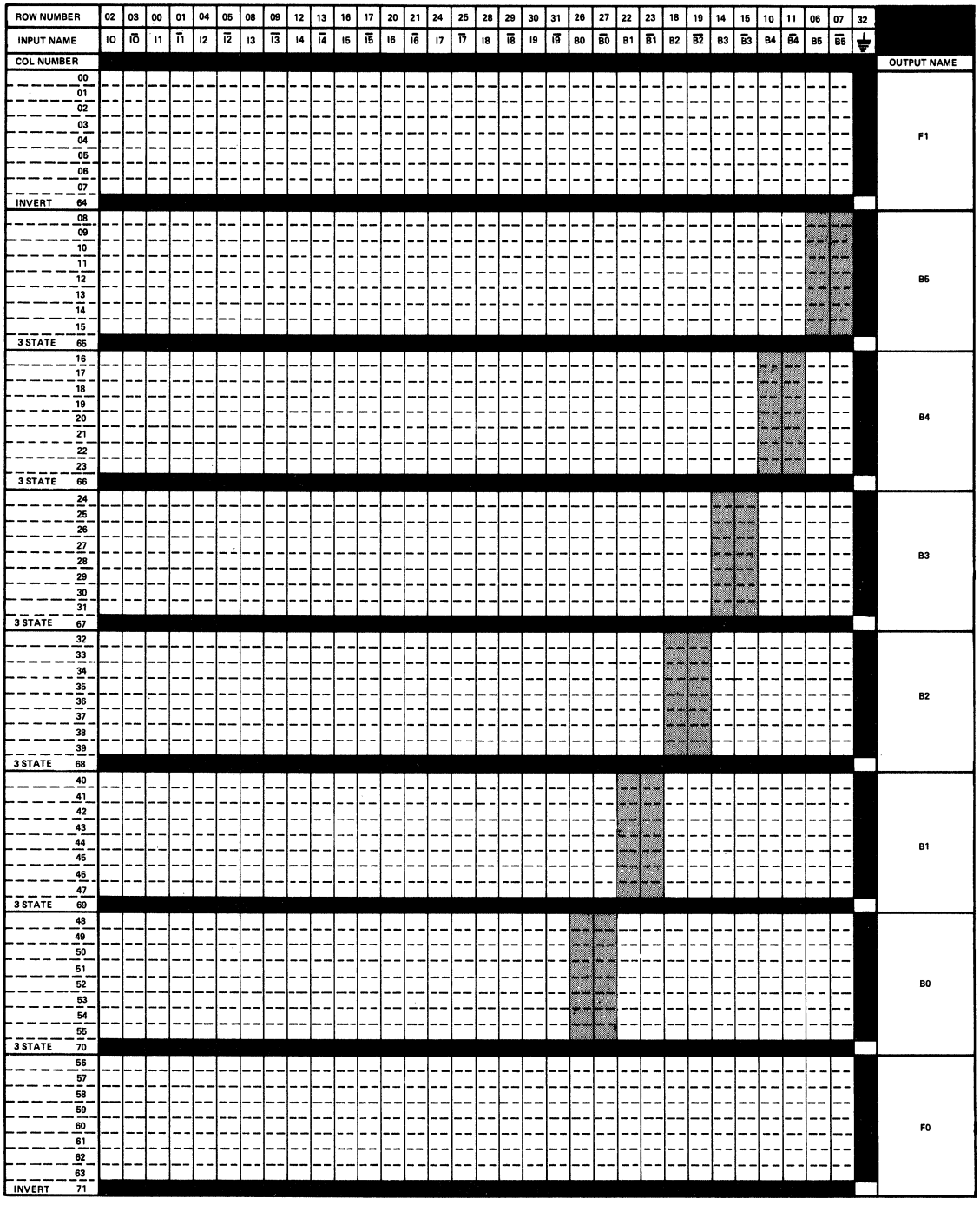


Figure 3

USE OF THE PROGRAMMING FORM

The programming form for the HPL-77319/320 is shown in Figure 3. Both devices have two output pins (F0-F1), and six bi-directional pins (B0-B5) which may be used as outputs or inputs. Any pin used as an output can have from one to eight product terms (AND) summed (OR'D) to it. Each product term can have from one to sixteen variables. In addition, each output and bi-directional pin has an extra configuration fuse which may be used to drive the bi-directional pins into a high impedance state allowing them to be used as inputs if desired, and to invert the polarity of the output pins. The HPL-77318/16LE8 has six inverting bi-directionals; the HPL-77320/16HE8 has six non-inverting bi-directionals.

Referring to the programming form (Figure 3), it can be seen that the column numbers or product term numbers are listed at the left hand side. Across the top, the row number or input variables are listed. In order to include an input variable in a product term, a "1" should be placed in the box at the intersection of the input variable and the product term. Notice that for every product term, if any input variable has both its true and complement forms included, then the entire product term will be unconditionally disabled (A./A=0), and will not contribute to the associated output. If it is desired not to use a product term, then all boxes for that column number should be left blank, notice that row 32 has the input symbol ⏚ ; this indicates that this row is at ground potential or logical "0". If a "1" is placed in a box at the intersection of Row 32 and an INVERT product term, then the associated output will be non-inverting; if a "0" is used, then the output will be inverting.

If a "1" is placed in a box at the intersection of Row 32 and a Three-State product term, then the associated bi-directional pin will be active (output). If a "0" is used, then it will be inactive (input). In this way the device's I/O ratio may be varied.

Each of the six bi-directional pins (B0-B5) has a gray area shown on the programming form at the intersection of their product terms and feedback variables. These gray areas may be be used, but a latched or oscillatory condition could occur if a positive or negative feedback loop is formed.

The programming form is shown with all boxes blank which is equivalent to all fuses being blown. HPL devices are supplied with all fuses intact and undesired fuses or connections must be blown.

For information concerning the entry of fuse data from the programming form into a suitable HPL programmer, refer the operating guide for that programmer.

If it is desired that device programming should be performed by Harris, programming information may be supplied in one or more of the following forms:

1. Master devices (Harris or other)
2. Boolean equations
3. Paper tapes
4. Programming form
5. Marked up logic diagrams (A substantial charge may be made for this entry format)

HARRIS

HPL-77210/16R4
HPL-77211/16R6
HPL-77212/16R8

Product Preview

HPL™ Harris Programmable Logic

Features

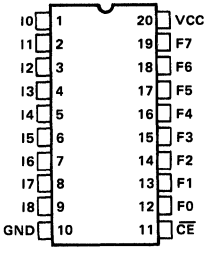
- LOGIC PATHS TESTED TO ENSURE FUNCTIONALITY
- FAST ACCESS (INPUT TO OUTPUT) . . . . . 35nsec MAX
  (CLOCK TO OUTPUT) . . . . . 25nsec MAX
- LOW ICC . . . . . 180mA MAX
- ALLOWS SIGNIFICANT PACKAGE COUNT SAVINGS
- ENHANCED INDUSTRY STANDARD PARTS
- 20 PIN SLIMLINE DIP
- HIGH SPEED PROGRAMMING PROCEDURE - ONE PULSE/ FUSE ASSURES SUPERIOR RELIABILITY
- REDUCTION OF IC INVENTORIES
- PROGRAMMABLE SUBSTITUTE FOR TTL SSI/MSI LOGIC CIRCUITS
- EASE OF PROTOTYPING AND BOARD LAYOUT
- TTL COMPATIBLE INPUTS AND OUTPUTS
- "THREE STATE" OUTPUTS
- THE HARRIS RELIABLE NICKEL-CHROMIUM FUSE TECHNOLOGY
- COMBINATORIAL AND/OR REGISTERED OUTPUTS
- SUPPORTED BY HELP™ SOFTWARE

Applications

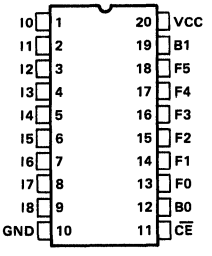
- RANDOM LOGIC REPLACEMENT
- CODE CONVERTORS
- STATE MACHINES
- ENCODERS/DECODERS
- BOOLEAN FUNCTION GENERATORS
- DIGITAL MULTIPLEXERS
- SHIFT REGISTERS
- COMPARATORS

Pinouts

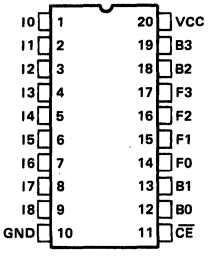
HPL-77212/16R8



HPL-77211/16R6



HPL-77210/16R4



Description

The HPL-77210/211/212 are programmable logic devices designed to be cost effective and space saving replacements for discrete logic designs. These devices are two level logic elements with either four registered and four combinatorial outputs (HPL-77210), six registered and two combinatorial outputs (HPL-77211), or eight registered outputs (HPL-77212).

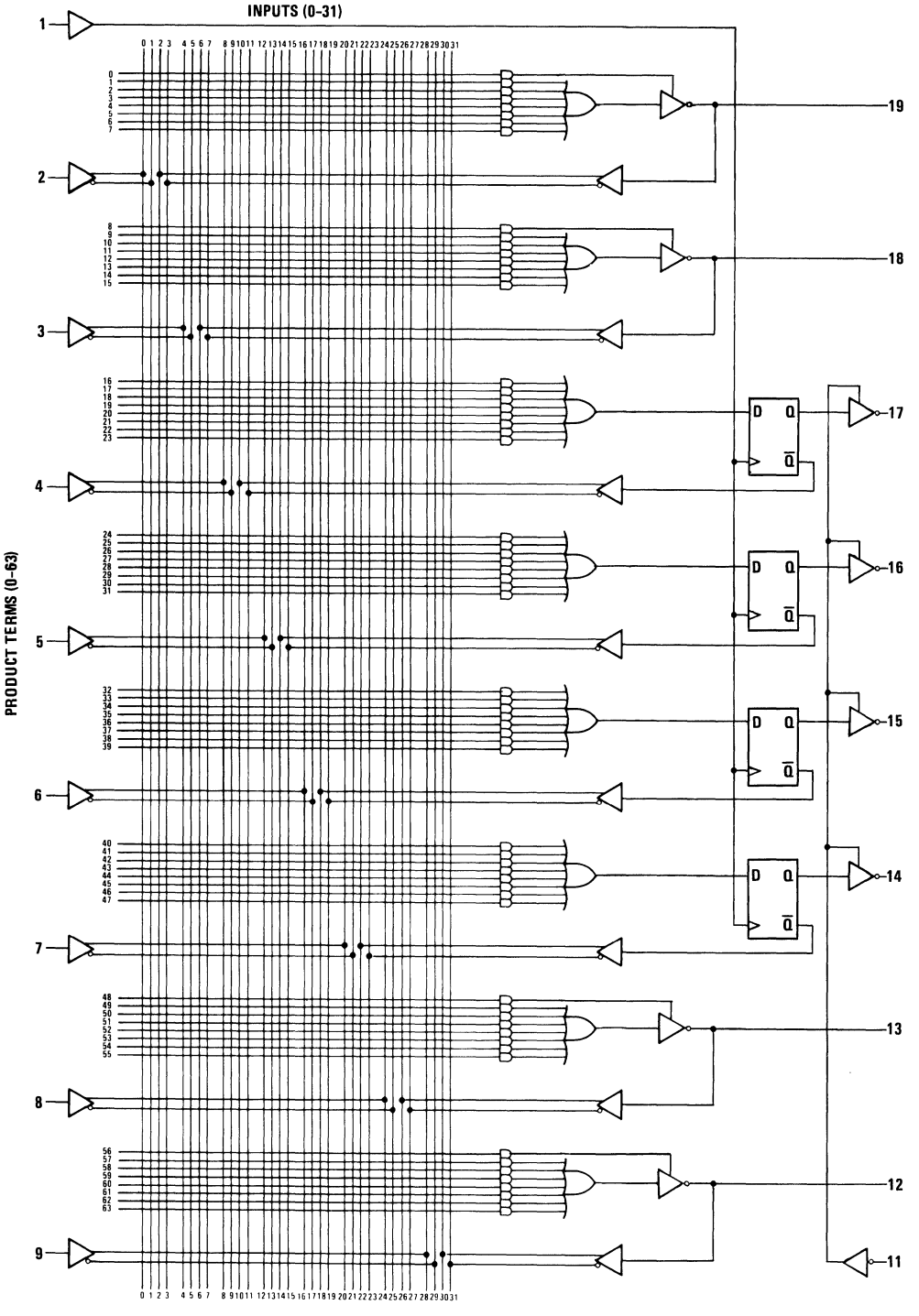
Each combinatorial output consists of seven product terms (AND) summed (RO) together to generate the familiar Sum of Products (SOP) form of Boolean expression. An eighth product term associated with each conbinatorial output can drive it into a high impedance state allowing that output to be used as an input, either permanently or dynamically. Each registered output is controlled by a dedicated output enable pin (Pin 11). Registered outputs also provide feedback to the matrix, allowing state machines to be implemented.

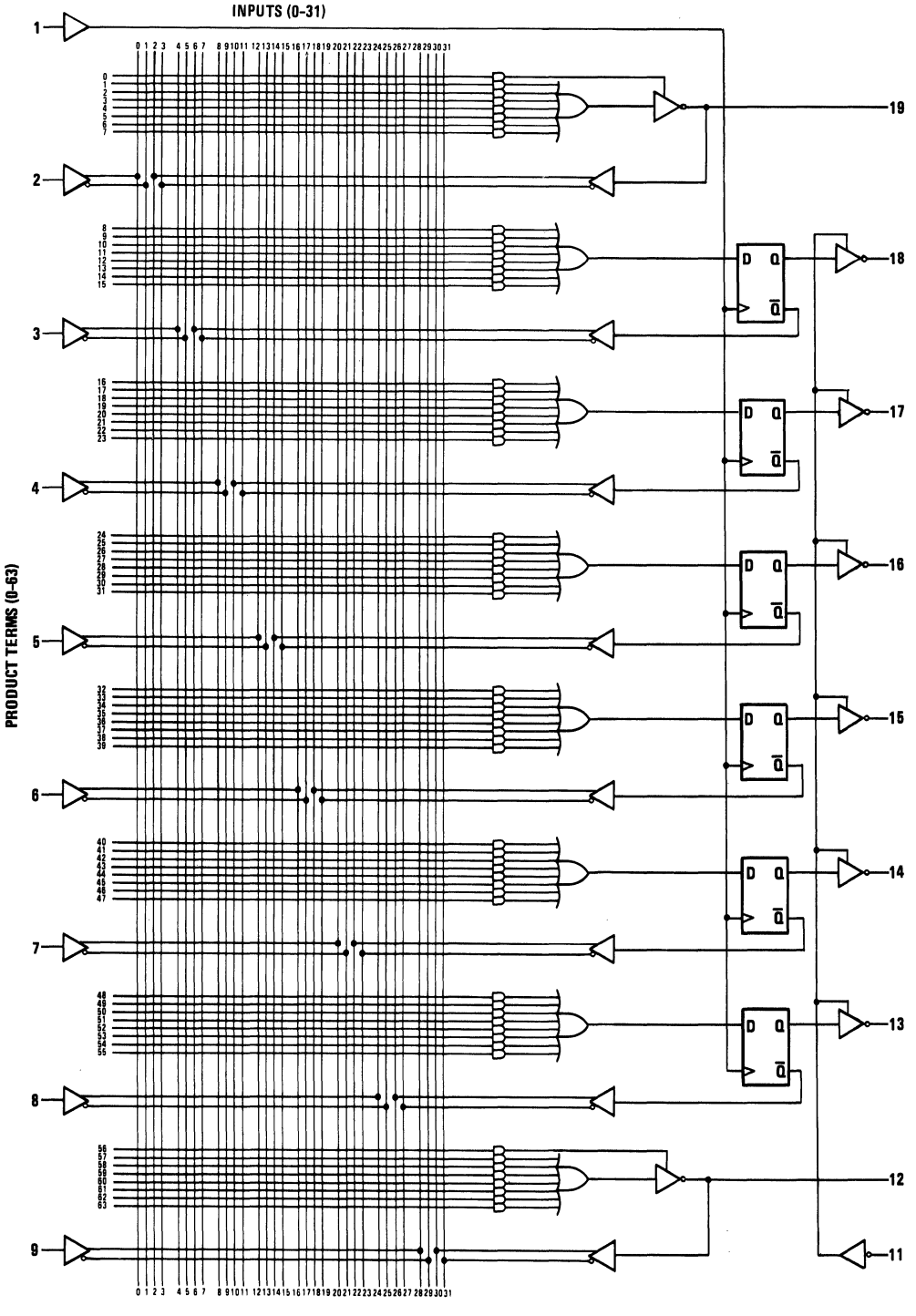
The HPL-77210/211/212 are field programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

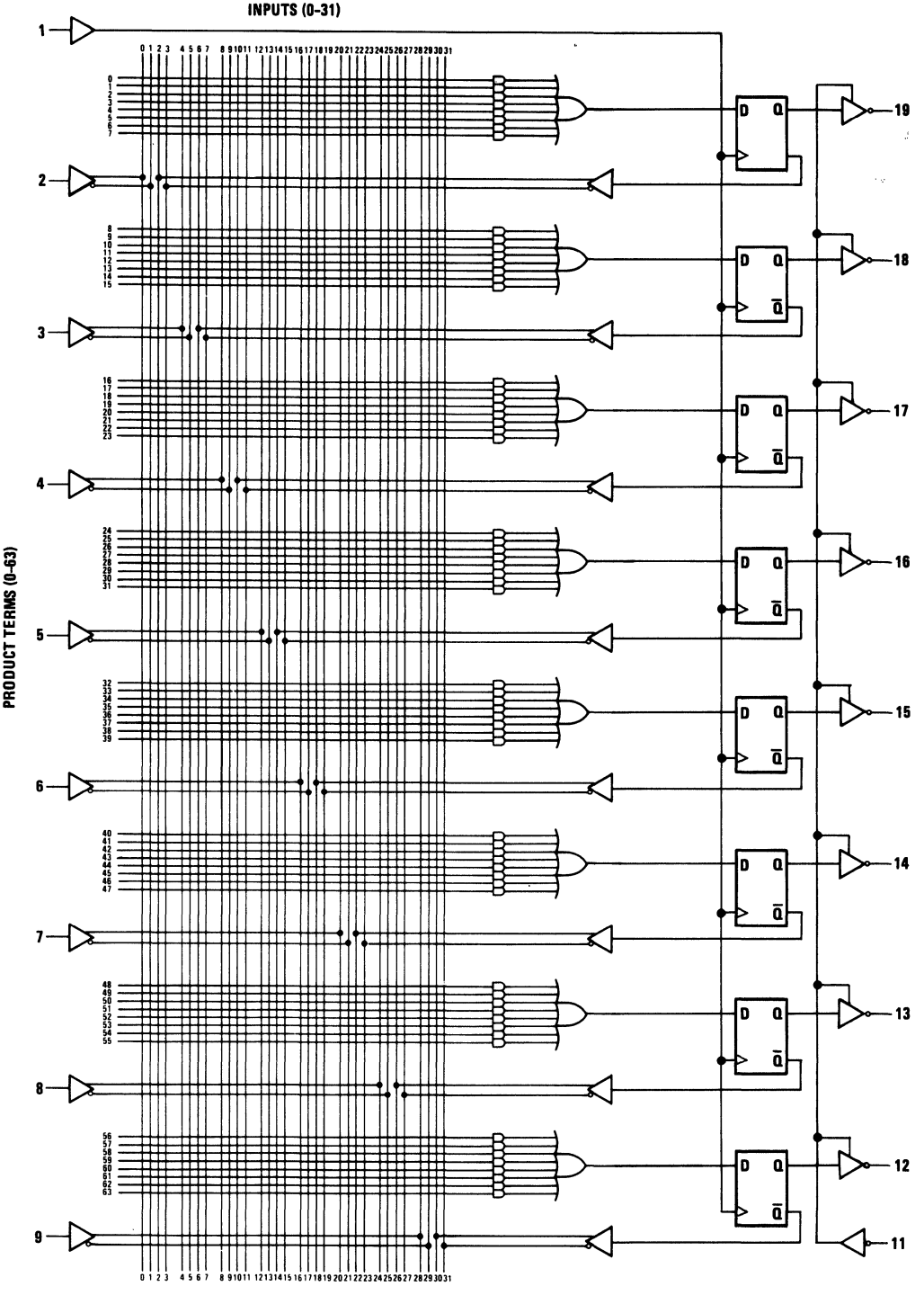
Nickel-chromium fuse technology is used on these and all other Harris HPL-77xxx programmable logic devices. The HPL-77210/211/212 are available in 20 pin slimline DIP packages with pinouts identical to the 16R4/R6/R8.

The HPL-77210/211/212 contains unique test circuitry developed by Harris which is enabled at the time of manufacture to allow complete AC and DC testing.

CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
HPL is a trademark of Harris Corporation.
HELP is a trademark of Harris Corporation.


INPUTS (0-31)
PRODUCT TERMS (0-63)
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
1
2
3
4
5
6
7
8
9
19
18
17
16
15
14
13
12
11
D
Q
Q̄


INPUTS (0-31)
PRODUCT TERMS (0-63)
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
1
2
3
4
5
6
7
8
9
19
18
17
16
15
14
13
12
11
D
Q
Q̄


INPUTS (0-31)
PRODUCT TERMS (0-63)
1
2
3
4
5
6
7
8
9
D
Q
19
18
17
16
15
14
13
12
11

HPL Programming Philosophy

Harris Semiconductor is the only vendor who manufactures both IFL and PAL type devices, and all HPL products (IFLs and PALs) program generically on any conventional programmer fitted with the appropriate Harris Programming/Testing Adaptor.

The HPL generic programming method employs a simple programming algorithm which does not require stress-inducing high voltages for individual fuse addressing; instead, program mode fuse addressing is done using TTL logic level signals. By using low voltages during programming, functional yield and in-circuit device reliability are maximized.

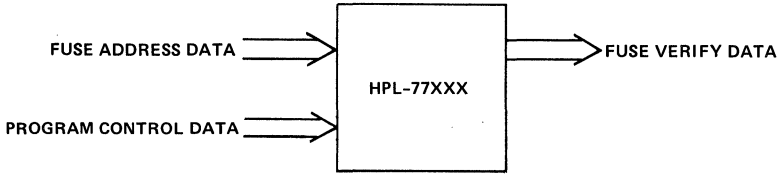
Another advantage of family wide generic programming is a reduction in the number of programmer adaptors required to program a wide range of devices, and therefore a reduction in the time required for familiarization by the operator. The HPL generic programming philosophy will be used on all future products, helping to ensure nonobsolescence of programming equipment.

All HPL products feature three distinct modes of operation. Two modes are always available to the user: the PROGRAMMING MODE (MODE 2) and the FUNCTIONAL MODE (MODE 3). The TEST MODE (MODE 1) is not generally available to the user because of its proprietary nature. For further information on MODES 1 and 3, please contact Harris Semiconductor, or consult Module 5, on page 6-32 (Section 6 – Applications) of this data book.

In MODE 2 (PROGRAMMING MODE), the integrity of the fuse matrix is verifiable; in other words, it is possible to verify that all the fuses in an unprogrammed device are intact. Also, individual fuses are capable of being selectively programmed in order to generate the overall logical functionality required by the user. Lastly, it is possible to verify that programmed fuses have programmed correctly, and that fuses desired not to be programmed are still intact. In summary, the basic features of the programming mode are:

1. The ability to selectively read all fuses to determine whether they are intact or programmed. This feature is functional both before and after programming.

2. The ability to selectively program individual fuses without erroneously programming nonselected fuses, or electrically or thermally overstressing or damaging the device.



PROGRAM MODE BLOCK DIAGRAM

Complete information on the programming and subsequent verification of HPL parts can be found in the individual device data sheets. The HPL programming mode pinout and programming algorithm is generic to all HPL products to this date; however, in accord with the Harris policy of supplying the customer with the highest possible quality, future products may include enhancements to the basic programming scheme.

HPL Programmer Evaluation

Programmer equipment manufacturers identified in the accompanying list have previously produced equipment determined to be capable of properly programming Harris Semiconductor Programmable Logic (HPL). This list is provided only as a convenience to purchasers of HPLs to identify programmer manufacturers potentially suitable for programming the HPLs. It is neither intended to be a representation or warranty by Harris of the capability of all listed manufacturer's models nor an indication of unsuitability of other manufacturers not contained in the list. HPL purchasers are advised to adhere to the programming requirements specified in HARRIS current data sheets applicable to the HPLs to be programmed and to the programming equipment manufacturer's specifications. Responsibility for programming equipment performance lies solely with the equipment manufacturer. The programmer user is cautioned to verify operation and performance according to the manufacturer's instructions and specifications prior to each use, and to determine that the programming complies with the applicable HPL data sheet. Harris accepts no responsibility for HPLs which have been subjected to incorrect or faulty programming.

HPL Programmer Manufacturers

DATA I/O
10525 Willows Road N. E.
C46
Redmond, WA 09052
Phone: 206-881-6444

STAG MICROSYSTEMS, INC.
528-5 Weddell Drive
Sunnyvale, CA 94086
Phone: 408-745-1991

DIGILEC USA *
Suite 103
7335 East Acoma Drive
Scottsdale, AZ 85260
Phone: 602-991-7268

* In approval process at present time.

NOTE: Programmer manufacturers are changing from modular or card sets to a universal type of programming system. Contact the programmer manufacturer for their latest updates of hardware and software.

BIPOLAR

Applications 6

Applications Index

INTRODUCTION TO HARRIS PROGRAMMABLE LOGIC.

Introduction

Harris Programmable Logic (HPL) is a family of user configurable logic elements designed to be space and power saving replacements for random logic designs implemented in TTL or LSTTL. HPL products are a natural progression for Harris Semiconductor, already a major PROM supplier with over ten years experience in the field of nichrome fuse programmable devices. The HPL family contains devices which are functional and pinout replacements for existing industry standard devices, and also includes new devices with enhanced architectural features designed for applications which are not served by existing devices.

Family

The HPL family is divided into three architecturally distinct groups, each with its own advantages and areas of application. The three HPL groups are: IFL™, PAL® and PROM, and are all similar in that they contain two logic arrays. The first array is an AND array which is used to form PRODUCT terms from combinations of feedback and/or input variables. The second array is an OR array which is used to form SUM terms from combinations of product terms generated by the first array. The difference between the three architectural groups results from various combinations of user configurable and fixed arrays.

The PAL type devices have a programmable first array (AND) and a fixed second array (OR). The PROM type devices have this configuration reversed; they have a fixed first array (AND) and a programmable second array (OR).

The IFL architectural group is different again, with both its first (AND) and second (OR) logic arrays being programmable. The various combinations of fixed and programmable arrays are shown graphically in FIG 2 on the following page. No one architectural group is the optimum solution for all designs, and for this reason Harris offers a wide range of devices to suit almost any design requirement.

Programming

All HPL devices, with the exception of the high speed PROM group, program generically on any conventional programmer fitted with the appropriate adaptor. The HPL generic programming method employs a simple programming algorithm which does not require stress-inducing high voltages for individual fuse addressing; instead, program mode fuse addressing is done using TTL logic level signals. By using low voltages during programming, functional yield and in-circuit device reliability are maximized. Another advantage of family wide generic programming is a reduction in the number of programmer adaptors required to program a wide range of devices, and therefore a reduction in the time required for familiarization by the operator. The HPL generic programming philosophy will be used on all future products, helping to ensure non-obsolescence of programming equipment.

Quality

One of the fundamental requirements for high quality is the ability to perform testing on unprogrammed devices as they are manufactured. It was only after the appearance on the market of early Programmable Array Logic devices that both manufacturers and users became aware of the inherent non-testability of those devices. The reasons for this difficulty in testing blank devices stemmed from architectural differences between programmable logic and programmable memory.

In a programmable memory device, such as a PROM, the same circuitry that is used at manufacture to verify the existence of fuses is used during the normal operation of the device. Therefore, if a PROM passes a fuse array verification test, then the logic paths from input to output are automatically tested for functionality. This simplicity of testing is not, however, present in programmable logic devices because the fuse array is verified using totally separate circuitry to that which is used to carry logic signals during normal device operation. Consequently, verification of the fuse array at manufacture does not guarantee correct operation of the logic paths, and because of this, fuse pattern verification by the user does not guarantee correct device functionality. It is apparent that, unlike a PROM, there are two components of FUNCTIONAL YIELD in a Programmable Logic device: FUSING YIELD and LOGIC PATH YIELD. The FUSING YIELD of a programmable logic device is similar to a PROM and is close to 100%. However, the LOGIC PATH YIELD is an unknown quantity and varies from device to device. The components of FUNCTIONAL YIELD for a programmable logic and programmable memory device are shown in FIG 1.

FUNCTIONAL YIELD (PROM) = FUSING YIELD

FUNCTIONAL YIELD (PROGRAMMABLE LOGIC) = FUSING YIELD × LOGIC PATH YIELD

FIG. 1

Responding to customer requirements for high quality devices, Harris developed unique on-chip test circuitry, which is enabled at the time of manufacture to allow complete testing of all logic paths, eliminating the uncertain factor of LOGIC PATH YIELD. One of the benefits of this test circuitry is that the user receives a completely tested device which, providing the fuse array programs correctly, is guaranteed to be functional, eliminating the problem of devices that verify on the programmer but fail in the circuit board. A second benefit of on-chip test circuitry is the ability to perform AC/DC parametric testing at the time of manufacture. This allows Harris to ship devices which are TESTED AND GUARANTEED, and not simply GUARANTEED.

Family Features and Characteristics

- Broad range of device types
- Generic "Low Voltage" programming
- Industry standard and proprietary devices
- Quality "TESTED AND GUARANTEED" devices
- MIL-M-38510 approved NiCr fuse technology
- Slimline packages including "Power Plastic"

HPL is a Trademark of Harris Corporation
IFL is a Trademark of Signetics Corporation
PAL is a Trademark of MMI

HPL PRODUCT LINE

The HPL product range includes devices from all three of the possible programmable logic architectures, in recognition of the fact that no one architecture is the optimum solution for all designs.

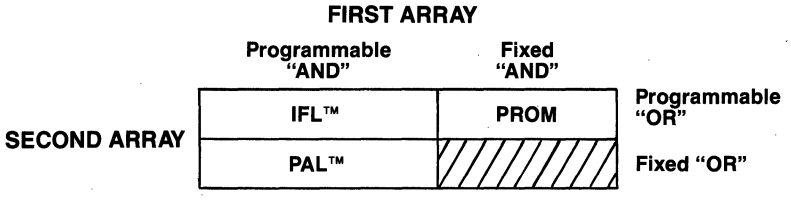


FIG 2

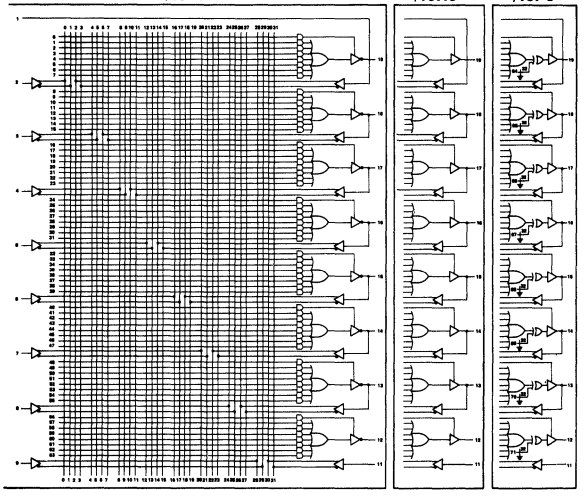
PART NUMBER	ALTERNATIVE PART NUMBER	ARCHITECTURE	SPEED	AVAILABILITY
HPL-77153	82S153	FPLA	40 nS	NOW
HPL-77209	16L8	PAL	35 nS	NOW
HPL-77210	16R4	PAL	17 MHz	CY84
HPL-77211	16R6	PAL	17 MHz	CY84
HPL-77212	16R8	PAL	17 MHz	CY84
HPL-77215	*16H8	PAL	35 nS	NOW
HPL-77216	*16P8	PAL	35 nS	NOW
HPL-77317	16LD8	PAL	35 nS	CY84
HPL-77318	16HD8	PAL	35 nS	CY84
HPL-77319	*16LE8	PAL	35 nS	CY84
HPL-77320	*16HE8	PAL	35 nS	CY84
HPL-77209B	——	PAL	15 nS	CY85
HPL-77215B	——	PAL	15 nS	CY85
HPL-77216B	——	PAL	15 nS	CY85
HPL-77210B	——	PAL	40 MHz	CY85
HPL-77211B	——	PAL	40 MHz	CY85
HPL-77212B	——	PAL	40 MHz	CY85
HPL-77061	*——	FPAD	25 nS	CY84
HPL-77209A	16L8A	PAL	25 nS	CY84
HPL-77215A	16H8A	PAL	25 nS	CY84
HPL-77216A	*16P8A	PAL	25 nS	CY84
HPL-77210A	16R4A	PAL	25 MHz	CY84
HPL-77211A	16R6A	PAL	25 MHz	CY84
HPL-77212A	16R8A	PAL	25 MHz	CY84

NOTE: SPECIFICATIONS FOR THOSE PARTS NOT IN PRODUCTION MAY BE CHANGED WITHOUT NOTICE. PLEASE CONTACT FACTORY FOR UPDATED AVAILIBILITY.
** ARCHITECTURE DEFINED BY HARRIS.*

HPL-77209/16L8 HPL-77215/16H8 HPL-77216/16P8

Functional Diagrams

HPL-77209 /16L8 HPL-77215 /16H8 HPL-77216 /16P8



D.C. ELECTRICAL CHARACTERISTICS (Operating)

HPL-77215/216/209 −5 (V_{CC} = 5.0V±5%, T_A = 0°C to +75°C)
HPL-77215/216/209 −2/−8 (V_{CC} = 5.0V±10%, T_A = −55°C to +125°C)

SYMBOL	PARAMETER		MIN	MAX	UNITS	TEST CONDITIONS	
I_{IH}	Input Current	"1"	—	+25	µA	V_{IH} = V_{CC} MAX	
I_{IL}	Dedicated Input	"0"	—	−100	µA	V_{IL} = 0.4 V	V_{CC} = V_{CC} MAX
I_{IZH}	Output Current	"1"	—	+40	µA	V_{IH} = V_{CC} MAX	V_{CC} = V_{CC} MAX
I_{IZL}	Hi-Z State	"0"	—	−40	µA	V_{IL} = 0.4V	
I_{BZH}	Bidirectional Pin Current	"1"	—	+40	µA	V_{BH} = V_{CC} MAX	V_{CC} = V_{CC} MAX
I_{BZL}	Hi-Z State	"0"	—	−100	µA	V_{BL} = 0.4V	
V_{IH}	Input Threshold (1)	"1"	2.0	—	V	V_{CC} = V_{CC} MAX	
V_{IL}	Voltage	"0"	—	0.8	V	V_{CC} = V_{CC} MIN	
V_{OH}	High-Level Output Voltage (2)		2.4	—	V	V_{CC} = V_{CC} MIN	I_{OH} = −2.0mA (M) I_{OH} = −3.2mA (C)
V_{OL}	Low-Level Output Voltage (2)		—	0.5	V	V_{IL} = 0.8V V_{IH} = 2.0V	I_{OL} = +16mA (M) I_{OL} = +24mA (C) (3)
V_{CL}	Input Clamp Voltage (1)		—	−1.2	V	I_{IN} = −18mA, V_{CC} = 0V	
I_{OS}	Output Short Circuit Current (2)		−30	−130	mA	V_{CC} = 5.0V, V_{OUT} = 0V One Output for MAX of One Sec.	
I_{CC}	Power Supply Current		—	155 (C)	mA	V_{CC} = V_{CC} MAX	
			—	165 (M)	mA		

C - Commercial (−5) M - Military (−2/−8)
(1) These specifications apply to both Input (I) and Bidirectional (B) pins
(2) These specifications apply to both Output (F) and Bidirectional (B) pins
(3) One output at a time, otherwise 16mA

A. C. SWITCHING CHARACTERISTICS (Operating)

SYMBOL			HPL-77215-5 HPL-77216-5 HPL-77209-5 5V±5% 0°C to +75°C		HPL-77215-2/-8 HPL-77216-2/-8 HPL-77209-2/-8 5V±10% −55°C to +125°C		
JEDEC STANDARD	OLD SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS
TDVQH1	T_{PD}	Propagation Delay - Input or I/O to Active High Output	—	35	—	45	ns
TDVQL1	T_{PD}	Propagation Delay - Input or I/O to Active Low Output	—	35	—	45	ns
TDVQH2	T_{PZX}	Enable Access Time to Active High Output (1)	TDVQZ1	35	TDVQZ1	45	ns
TDVQL2	T_{PZX}	Enable Access Time to Active Low Output (1)	TDVQZ2	35	TDVQZ2	45	ns
TDVQZ1	T_{PXZ}	Disable Access Time from Active High Output	—	30	—	35	ns
TDVQZ2	T_{PXZ}	Disable Access Time from Active Low Output	—	30	—	35	ns

(1) Enable Access Time is guaranteed greater than Disable Access Time to avoid device contention
NOTE: Maximum test frequency is 5MHz with a 50% duty cycle

Description

The HPL-77215/216/209 are programmable logic devices designed to be cost effective and space saving replacements for discrete logic designs. These devices are two-level logic elements consisting of 7 product terms (AND) summed (OR) together to generate each of the 8 outputs. An eighth product term associated with each output can drive it to a high impedance state allowing 6 (B0-B5) of the 8 outputs to be used as inputs, either permanently or dynamically.

The HPL-77209 is functionally identical to the industry standard 16L8, and implements logic expressions of the Inverted Sum Of Products (ISOP) form.

The HPL-77215 is a similar device to the 16L8 but does not include the associated output inversion, it implements logic expressions of the Sum Of Products (SOP) form.

The HPL-77216 is a more flexible device, it includes 8 EX-OR gates in each output path, controlled by 8 extra fuses, allowing the polarity of each output to be user configured. This device can implement a combination of SOP and ISOP expressions.

The HPL-77215/216/209 are field programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

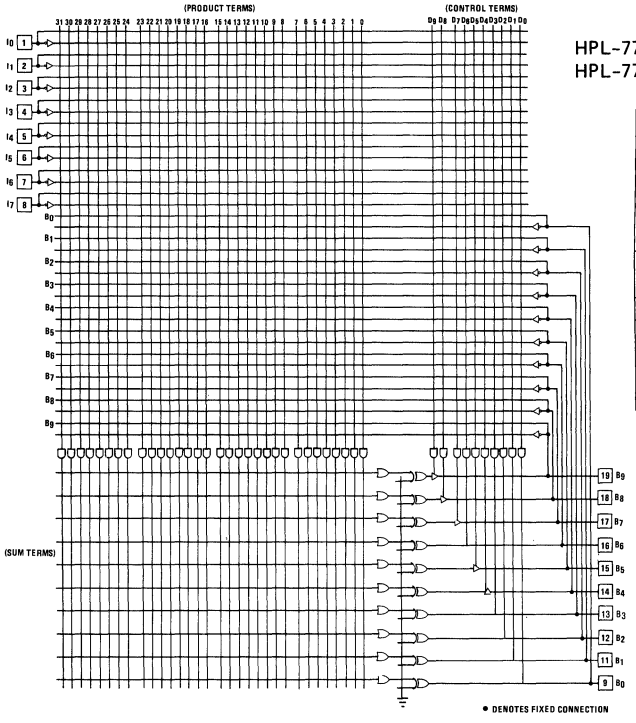
Nickel-chromium fuse technology is used on these and all other HARRIS HPL-77XXX programmable logic devices. The HPL-77215/216/209 are available in 20 pin slimline DIP packages with pinouts identical to the 16L8.

The HPL-77215/216/209 contain unique test circuitry developed by HARRIS which is enabled at the time of manufacture to allow complete AC and DC testing.

Functional Diagram

HPL-77153/82S153

HPL-77153/82S153



D.C. ELECTRICAL CHARACTERISTICS (Operating)

HPL-77153/82S153 -5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HPL-77153/82S153 -2/-8 (V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER		MIN	MAX	UNITS	TEST CONDITIONS	
I_{IH}	Input Current	"1"	–	+40	A	$V_{IH} = V_{CC}$ MAX	
I_{IL}	Dedicated Input	"0"	–	-100	A	V_{IL} = 0.4V	$V_{CC} = V_{CC}$ MAX
I_{BZH}	Input Current Bidirectional Pin Current	"1"	–	+40	A	$V_{BH} = V_{CC}$ MAX	
I_{BZL}	Hi-Z State	"0"	–	-100	A	V_{BL} = 0.4V	$V_{CC} = V_{CC}$ MAX
V_{IH}	Input Threshold Voltage	"1"	2.0	–	V	$V_{CC} = V_{CC}$ MAX	
V_{IL}		"0"	–	0.8	V	$V_{CC} = V_{CC}$ MIN	
V_{OH}	High-Level Output Voltage		2.4	–	V	$V_{CC} = V_{CC}$ MIN, V_{IL} = 0.8V, V_{IH} = 2.0V	I_{OH} = -2.0mA
V_{OL}	Low-Level Output Voltage		–	0.5	V		I_{OL} = +16mA
V_{CL}	Input Clamp Voltage		–	-1.2	V	I_{IN} = -18mA, V_{CC} = 0V	
I_{OS}	Output Short Circuit Current*	C	-20	-70	mA	V_{CC} = 5.0V, V_{OUT} = 0V	
		M	-15	-85	mA	One output for MAX of One Sec.	
I_{CC}	Power Supply Current	C	–	155	mA	$V_{CC} = V_{CC}$ MAX	
		M	–	165	mA		

C = Commercial (-5) M = Military (-2/-8)

A. C. SWITCHING CHARACTERISTICS (Operating)

SYMBOL		PARAMETER	HPL-77153/82S153-5 5V ± 5% 0°C to +75°C		HPL-77153/82S153-2/-8 5V ± 10% -55°C to +125°C		UNITS
JEDEC STANDARD	OLD SYMBOL		MIN	MAX	MIN	MAX	
TDVQH1	T_{PD}	Propagation Delay-Input or I/O to Active High Output	–	40	–	55	ns
TDVQL1	T_{PD}	Propagation Delay-Input or I/O to Active Low Output	–	40	–	55	ns
TDVQH2	T_{OE}	Enable Access Time to Active High Output	–	35	–	45	ns
TDVQL2	T_{OE}	Enable Access Time to Active Low Output	–	35	–	45	ns
TDVQZ1	T_{OD}	Disable Access Time from Active High Output	–	30	–	45	ns
TDVQZ2	T_{OD}	Disable Access Time from Active Low Output	–	30	–	45	ns

NOTE: Maximum test frequency is 5MHz with a 50% duty cycle.

Description

The HPL-77153/82S153 is a programmable logic device designed to be cost effective and space saving replacement for discrete logic designs. This device is a two-level logic element, consisting of 32 product terms (AND) and 10 sum terms (OR) with fusible links for programming I/O polarity and direction.

All product terms can be linked to 8 inputs (I) and 10 bidirectional I/O lines (B) allowing variable I/O configurations using the 10 direction control gates (C), ranging from 17 inputs and 1 output to 8 inputs and 10 outputs.

On chip T/C buffers allow either True (I, B) and/or Complement (I, B) signals to be linked to any of the product terms, the outputs of which may be used as inputs to any or all of the sum terms. The output polarity of the sum terms is individually programmable by means of a fuse-link controlled EX-OR gate to allow implementation of Sum Of Products (SOP) or inverted Sum Of Products (ISOP) expressions.

The HPL-77153/82S153 is field programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

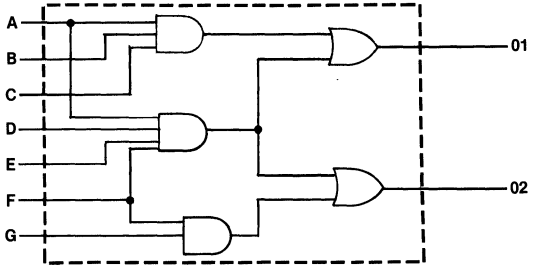
Nickel-chromium fuse technology is used on these and all other HARRIS HPL-77XXX programmable logic devices. The HPL-77153/82S153 is available in a 20 pin slimline ceramic DIP with a pinout identical to the 82S153. NOTE: The HPL-77152/82S152 (open collector outputs) can also be made available.

The HPL-77153/82S153 contains unique test circuitry developed by HARRIS which is enabled at the time of manufacture to allow complete AC and DC testing.

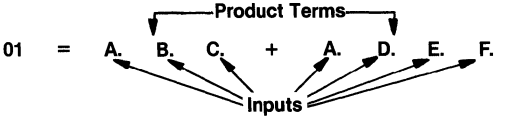
CHOOSING AND USING PROGRAMMABLE LOGIC

Because of the wide range of HPL products available, some method of selecting the right device for a given application is necessary. The method offered below is one way of selecting a device based on input, output and product term usage. This is only one method; other selection criteria, such as speed or power, may require a different selection procedure and will be different from user to user. However, the method shown is a good first approach. Decisions based on other criteria can be made after a device is initially selected.

FOUR CRITERIA ARE IMPORTANT

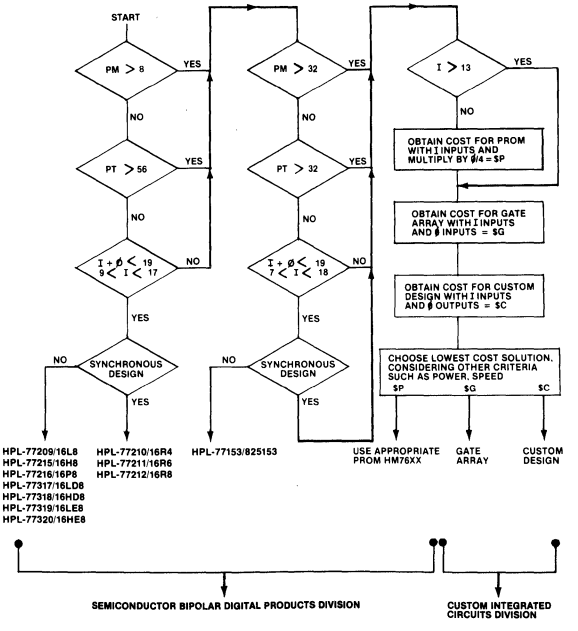


1. DRAW BOX AROUND SECTION OF CIRCUIT TO BE REPLACED, COUNT NUMBER OF INPUTS = I
2. COUNT NUMBER OF OUTPUTS = Ø
3. DERIVE LOGIC EQUATIONS FOR EACH OUTPUT e.g.:



COUNT NUMBER OF PRODUCT TERMS FOR ALL OUTPUTS = PT

4. HOW MANY PRODUCT TERMS ARE USED ON THE OUTPUT WITH MOST PRODUCT TERMS = PM



Module 1

Introduction to the HPL Family

By Steven Bennett – HPL Product Marketing

1.1 THE HPL FAMILY IS THE ANSWER!

In the 1970's, the microprocessor, after some reticence by engineers, was hailed as the panacea for many logic circuit design problems which previously had been the domain of large arrays of discrete logic.

The microprocessor could offer many advantages over discrete logic arrays, including reduced system power, much reduced package count, improved reliability, the ability to implement logic functions not available in discrete packages, and the flexibility to reprogram the emulated logic function by simple software changes.

These advantages were quickly realized by engineers working in many different application areas, and were partly responsible for the astonishing success enjoyed by the microprocessor.

Useful though the microprocessor is, it does suffer from one important disadvantage – speed. Any emulation of a discrete logic array cannot, with today's technology, hope to even approach the speed of the discrete design.

Speed may not be an important consideration in some designs, but in many others it certainly is. For this class of applications, a new product line is available: the HPL family of programmable logic.

The HPL family consists of many products for implementing large or small, synchronous or asynchronous logic arrays, that could only be emulated in real time by a microprocessor running at several hundred megahertz, which is not possible with today's technology.

The use of HPL products, because they are easily understood by a hardware engineer, can allow him to exercise more control over a project. In the last decade, this control has become more and more the domain of software engineers who have required increasingly large amounts of time and resources to accomplish their task.

In conclusion, there exists a class of applications where HPL devices can be used to produce a cheaper, faster, lower power, fewer parts solution to logic design problems.

1.2 WHAT ARE HPL DEVICES?

HPL devices are a "black box" solution to logic design problems. All the devices in the family are characterized by having a set of inputs and a set of outputs; the logical relationship between any output and the set of all other inputs and outputs is determined by the way an array of fuses inside the device is programmed (the fuse array is similar to a PROM). The method used for generating the pattern for programming HPL devices may vary according to how the designer views the device.

For those designers who are more familiar with discrete logic design, the HPL device may be viewed as a highly integrated form of discrete logic. Indeed, examination of an HPL device data sheet will reveal a schematic of the internal logic of the device in terms of AND, OR and INVERTOR gates, LATCHES, REGISTERS, and other devices, with which such designers will be familiar.

For those designers who are familiar with Boolean Algebra, and take a "black box" approach to systems design, they need only generate the appropriate Boolean logic equations for each device output.

Whichever approach is taken to generate the programming pattern, it is a simple task to use almost any PROM programmer (with a suitable adapter) to program devices with the required pattern.

The ease of programming HPL devices can solve a common problem for designers using discrete logic, which is:

> "How do I tell my boss that my design needs a minor modification, which will cause a six week production delay until new printed circuit boards are obtained?"

The programmability of HPL devices can eliminate this problem, as a "minor modification" can be implemented in minutes by programming a new device, or with some HPL devices performing "logical surgery" on a programmed part.

Having covered some areas of application and the advantage of using HPL devices, the following sections will deal with some of the decisions that must be made before choosing an HPL device.

**HPL is a Trademark of Harris Corporation*

1.3 PROM OR HPL, THAT IS THE QUESTION!

Programmable read only memories (PROM) have traditionally been used not only for the storage of computer programs, but also to emulate asynchronous random logic arrays.

The emulation of random logic by PROMs is attractive because it allows a significant reduction in package count, but it is not an optimum solution for the following reasons:

Any random logic array is characterized by having a number of inputs (X) and a number of outputs (Y). To replace a random logic array with a PROM requires the use of a PROM with X inputs, which translates to 2^X bytes. For a small number of inputs, say 5, one can use a 2^5 or 32 byte PROM which is a low cost solution; however, suppose the input field is 13 bits wide, one must now use an 8K byte PROM which is an expensive solution.

The high cost involved in replacing random logic arrays with a large number of inputs, with PROMs is mainly due to the inefficient architecture of PROMs when used in this manner. One useful definition of architectural efficiency is:

$$\text{EFFICIENCY} = \frac{\text{NUMBER OF DISCRETE OUTPUT CODES USED}}{\text{TOTAL NUMBER OF OUTPUT CODES POSSIBLE}} \times 100\%$$

Let us now use this definition to compare the efficiency of PROMs versus HPL programmable logic arrays.

Suppose a random logic array exists, having an input field width of ten bits, an output field width of eight bits, and five unique output codes associated with the input field. One solution would be to use a 1K × 8 PROM which would have the following efficiency:

$$\text{1K} \times 8 \text{ PROM EFFICIENCY} = \frac{5 \times 100}{1024} = 0.48\%$$

A better solution would be to use an HPL77209/16L8 Programmable Logic Array, which would have the following improved efficiency:

$$\text{HPL77209/16L8 EFFICIENCY} = \frac{5 \times 100}{7} = 71.42\%$$

NOTE: In the calculation used to evaluate the HPL77209/16L8 efficiency, it is assumed that the seven internal product terms available to each output are used to generate seven unique output codes in a similar manner to a PROM. Although this approach cannot be representative of all applications, it is a useful approximation.

The large difference in device efficiency is reflected in the higher cost of the PROM solution. This is not to say that all PROM applications are inefficient; for example, an ASCII to EBCDIC code convertor using a PROM would have a high efficiency, and in fact, could not be implemented using an HPL device.

The secret is to choose the correct device for one's application, and for the majority of random logic replacement applications, an HPL device should be preferred.

Having shown that HPL devices are far more efficient than PROMs for replacing most random logic arrays, the following is a more detailed explanation of how that efficiency is achieved.

HPLs are programmable AND arrays followed by either a fixed or a programmable OR array, according to the type. PROMs are fixed AND arrays followed by a programmable OR array. Figures 1-1 and 1-2 depict the basic difference.

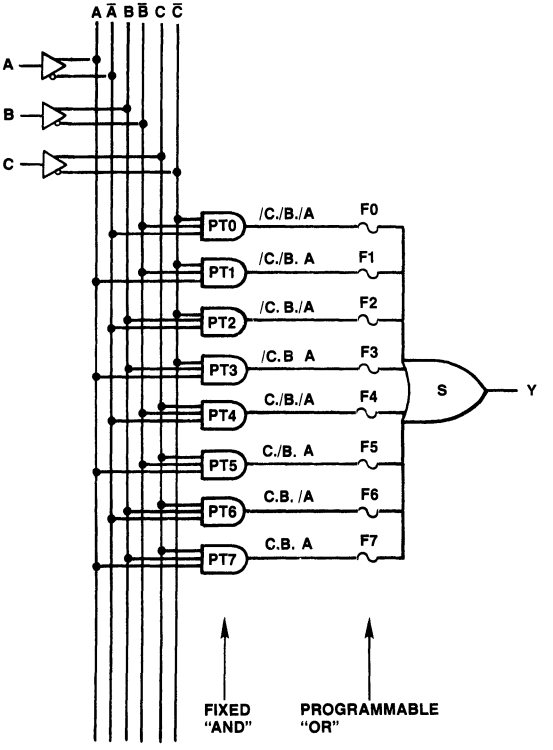


Figure 1-1 – Elementary PROM

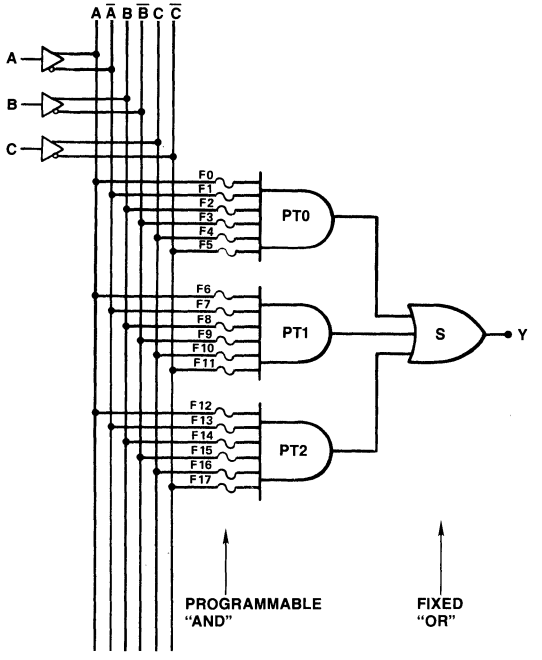


Figure 1-2 – Elementary HPL

The PROM structure decodes all input combinations using a fixed AND decoder as shown in Fig. 1-1. Because the PROM illustrated has three inputs, the AND decoder must consist of $2^3 = 8$ AND gates. Each gate uniquely defines a product term (PT) which is fuse-linked to the input of the OR matrix as shown. The presence or absence of the fuse determines the programmed function. For example, to program the function

YO = /C./B./A + /C.B.A + C./B./A + C./B.A
(PTO) (PT3) (PT4) (PT5)

One would retain fuses for PTO, PT3, PT4, PT5 and blow all others. Note that a blown fuse represents a logical zero to the OR matrix.

NOTES: Symbology used in equations + = OR
• = AND
/ = NOT (INVERT)

Now suppose the following function were desired instead:

Y1 = A + B.C + /B./C

The first term, A, is implemented in the PROM by selecting PT1, PT3, PT5, and PT7. Product terms PT1, PT3, PT5, and PT7 can be reduced using Boolean Algebra as follows:

A = /C./B.A + /C.B.A + C./B.A + C.B.A
A = /C.A + C.A = A. (/C+C)
A = A

Similarly, the second term, B.C is generated by selecting PT6 and PT7 and the last term, /B./C by selecting PT0 and PT1. The ORing of all product terms implements Y1 in the PROM as follows:

Y1 = /C./B./A + /C./B.A + /C.B.A
+ C./B.A + C.B./A + C.B.A

Note that the original equation for Y1 contained only three product terms while the PROM implementation required that six product terms be involved. This demonstrates the inefficiency of using a PROM to replace random logic.

A more effective architecture for implementing logic is shown in Fig. 1-2. Y1 can be directly implemented using this structure by simply programming fuses to generate the three product terms as follows:

Y1 = A + B.C + /C./B
FO F8, F10 F17, F15

This would involve blowing all fuses except F0, F8, F10, F15, and F17.

Typically, logic designs involve a relatively high number of input variables but do not require that all 2^n possible input combinations be completely decoded as in the PROM; for example, a 10 variable logic expression as shown below would require a $2^{10} = 1024$ location PROM.

Y2 = A./B./C.D.E./F.G.H.I./J
+ /A./B./C.D.E.F.G.H./I.J

However, the same function can easily be implemented in the basic HPL shown in Fig. 1-3. The HPL structure offers several potential advantages over the PROM, such as:

- GREATER THAN 4 TO 1 REDUCTION IN BOARD SPACE
- LOWER COSTS
- FASTER PROGRAMMING
- INCREASED SPEED
- USER DEFINABLE PINOUT
- EFFICIENT PRODUCT TERM COMPRESSION
- SMALLER FUSE ARRAY
- LOWER POWER
- ADVANCED ARCHITECTURE FEATURES

In addition, the price paid for additional input capability when using a PROM as a logic element is usually too high. As an example, consider adding another input variable to the previous 10-input logic expression. The extra input variable would require a $2^{11} = 2048$ location PROM, doubling the fuse matrix size required. On the other hand, adding an extra input to the HPL structure of Fig. 1-3 would only increase the fuse matrix size from 120 to 132 fuses, only a 10% increase in size.

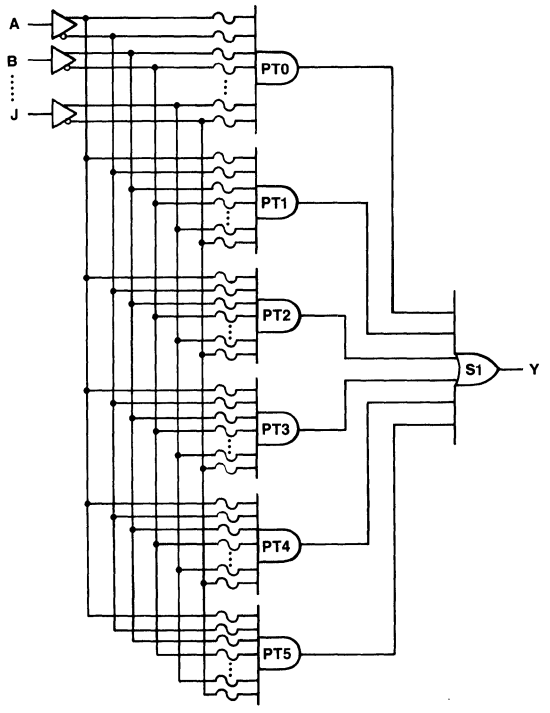


Figure 1-3 – Basic HPL Logic Structure

As a function of the number of inputs (X), the PROMs' fuse matrix size increases geometrically ($\propto 2^X$), whereas the HPLs' array size increases arithmetically ($\propto 2X$).

Harris programmable logic devices exhibit other features which make their use more desirable than PROMs. One such feature is the minimization of output glitches during input transitions. It is not often recognized that the logical output condition of a PROM is undefined for the duration of the device's access time, which means that for tens of nanoseconds after an address line changes, the device outputs may exhibit an undesired state. If the output from such a PROM is then used to drive a synchronous device such as a counter, erroneous counts may be registered. This situation rarely occurs with HPL devices, which can make the design engineers task easier, leading to fewer production problems.

So far, only an elementary form of HPL has been discussed. More complex devices are found in the HPL family, including:

Devices with programmable AND structures and programmable OR structures, which allow the implementation of larger and more powerful logic equations.

Devices with programmable output polarity (using EX-OR gates) allowing outputs to implement the true or inverted form of a logic expression.

Devices with latches and internal feedback allowing the implementation of sophisticated synchronous state machines of the Mealy or Moore type.

These and many other powerful features are dealt with more completely in the following modules.

1.4 THE HARRIS PROGRAMMABLE LOGIC FAMILY

The Harris Programmable Logic family consists of many different parts, some of which are enhanced versions of industry standard parts, while others are powerful propriety parts developed to satisfy a specific area of applications.

The HPL family is available in an advanced Bipolar technology, allowing high speed and low power devices to be fabricated.

Some of the features to be found in the HPL family are:

- SPACE SAVINGS PACKAGES
- HIGH SPEED AND LOW POWER
- ON-CHIP FUNCTIONAL TEST CIRCUITS
- VARIABLE I/0 PIN RATIO
- PROGRAMMABLE THREE STATE OUTPUTS
- BI-DIRECTIONAL PINS
- REGISTERS WITH FEEDBACK
- PROGRAMMABLE LATCHES
- PROGRAMMABLE OUTPUT POLARITY
- ARITHMETIC CAPABILITIES
- USER DEFINABLE PIN-OUT

Harris programmable logic devices can be programmed and verified using most standard PROM Programmers, with the addition of a suitable personality card.

A user can expect a very high programming yield because special test circuitry, built on chip, is enabled at the time of manufacture, allowing the parts to be exercised and tested for logical functionality and compliance with the published static (DC) and switching (AC) parameters. The ability to test parts at the time of manufacture eliminates a major problem associated with other industry parts; namely, the inability to guarantee the units as fully functional after programming, even though the fuse matrix had "verified".

Built in testability is just one of many unique enhancements included in the HPL family. All the enhancements included in the HPL family were designed in with the intention of providing the user with improved programming yield, superior and more reliable parts.

HARRIS

HPL™ The Logical Solution

Module 2

Introduction to Boolean Algebra

By Steven Bennett – HPL Product Marketing

2.1 INTRODUCTION TO LOGIC

It is ironic to reflect that the foundation of modern logic theory has lain dormant for many years before being utilized in practice. The basis of logic as we know it was set down in the nineteenth century by Boole, DeMorgan and others. Many generations were to pass before technologists began to realize the implications of these theories, and even longer before fabrication techniques for the construction of "logical" devices were perfected.

In this introduction to Boolean Algebra, the following Boolean operators are used:

=	Logical Equality
/	Negate (Not, invert)
+	OR (Sum)
•	AND (Product)
:+:	Exclusive OR
:*:	Exclusive NOR

In addition, a number of logic theorems and laws will be used to manipulate and reduce logical equations; these theorems and laws are as follows:

THEOREM 1	A + 0 = A
THEOREM 2	A•0 = 0
THEOREM 3	A + 1 = 1
THEOREM 4	A•1 = A
THEOREM 5	A + A = A
THEOREM 6	A•A = A
THEOREM 7	A + /A = 1
THEOREM 8	A•/A = 0

COMMUTATIVE LAW

A + B = B + A
A•B = B•A

ASSOCIATIVE LAW

A + B + C = (A + B) + C = A + (B + C)
A•B•C = (A•B)•C = A•(B•C)

DISTRIBUTIVE LAW

A + (B•C•D) = (A + B)•(A + C)•(A + D)
A•(B + C + D) = A•B + A•C + A•D

DeMORGAN'S THEOREM

/(A + B + C) = /A•/B•/C
/(A•B•C) = /A + /B + /C

DeMorgan's theorem is one of the most powerful tools for engineering applications and is very useful for designing with HPL programmable logic devices because it provides a quick and simple conversion method between PRODUCT OF SUMS and SUM OF PRODUCTS expressions.

Any logic expression can be reduced to a two level form and expressed as either a SUM OF PRODUCTS (SOP) or PRODUCT OF SUMS (POS). The two basic forms are explained below.

SUM OF PRODUCTS (SOP)

F = (A•B) + (C•D) + (E•F•G) EQ 2.0

The above is an example of a SOP logic expression. The reason for the name becomes apparent if one refers to the table of Boolean operators.

PRODUCT OF SUMS (POS)

F = (A + B)•(C + D)•(E + F + G) EQ 2.1

The above is an example of a POS logic expression. Again the reason for the name becomes apparent if one refers to the table of Boolean operators.

2.2 REVIEW OF BOOLEAN ALGEBRA

Boolean Algebra is probably the simplest form of Algebra because variables can have only one of two values, either a logical one or logical zero. For example, the Boolean function shown below has at the most four possible solutions since it is a function of two variables and each variable can have one of two states (0 or 1).

F(X, Y) = X•Y + Y•Y EQ 2.2

The four possible solutions are:

F(0, 0) = 0•0 + 0•0 = 0
F(0, 1) = 0•1 + 1•1 = 1
F(1, 0) = 1•0 + 0•0 = 0
F(1, 1) = 1•1 + 1•1 = 1

These solutions can also be written as a "truth table":

X	Y	F(X, Y)
0	0	0
0	1	1
1	0	0
1	1	1

Because a binary variable can assume only one of two states, it is possible to perform a logical reduction by inspection. The equation (EQ 2.2) can be reduced by using the theorems shown earlier, as follows:

F(X, Y = X•Y + Y•Y	
F(X•Y) = X•Y + Y	(Theorem 6)
F(X•Y) = Y•(X + 1)	(Distributive Law)
F(X•Y) = Y•(1)	(Theorem 3)
F(X•Y) = Y	(Theorem 4)

So, F(X, Y) has been reduced to a function of a single variable F(Y) = Y. Contrast this process with conventional linear algebra where:

F(X•Y) = X•Y + Y•Y

can only be factored, not simplified, to:

F(X•Y) = Y•(X + Y)

Another binary function which can be reduced by inspection is shown below.

F = /A + A•B + /C•D + C•D	EQ 2.3
F = [(/A + A)•(/A + B)] + /C•D + C•D	(Distributive Law)
F = [1•(/A + B)] + /C•D + C•D	(Theorem 7)
F = /A + B + /C•D + C•D	(Theorem 4)
F = /A + B + D•(/C + C)	(Distributive Law)
F = /A + B + D•(1)	(Theorem 7)
F = /A + B + D	EQ 2.4

In terms of logical representation, see Fig 2-1a for the implementation of EQ 2.3 in its original form, and compare it to the reduced version Fig. 2-1b (EQ 2.4).

The use of logical theorems and laws is not only useful for the reduction of the number of gates needed to implement a function, but can also reduce or eliminate "race hazards" which occur if the propagation delays from all inputs to an output are not identical. Obviously, the more complex a logic circuit, and the more redundant paths included, the more chance there is for "race hazards" to occur. "Race hazards" manifest themselves as logical glitches at the network output.

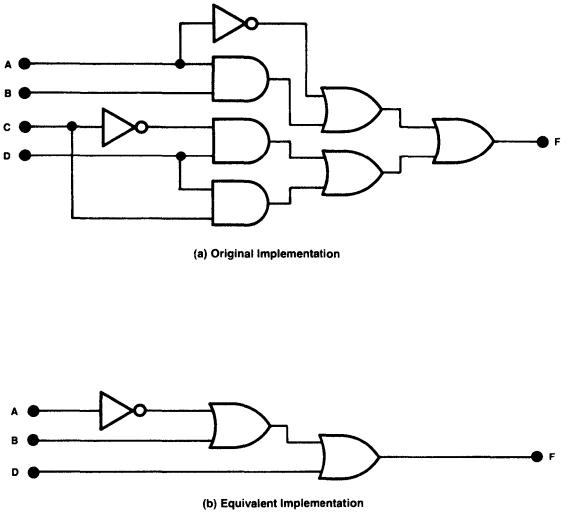


FIGURE 2-1. IMPLEMENTATION OF THE SAME LOGIC FUNCTION

As you can see there are several ways to implement the same function. Figure 2-1(a) and (b) are only two realizations for F. Although the circuit in (b) is a minimum gate realization, it is not the only one.

Figure 2-2 shows yet another implementation for F. The transposition of Figure 2-1(b) to Figure 2-2 is made possible by DeMorgan's theorem as follows:

F = /A + B + D	EQ 2.5
/F = /(/A + B + D)	(Negate Both Sides)
/F = A•/B•/D	(DeMorgan's Theorem)
F = /(A•/B•/D)	EQ 2.6

As can be seen EQ 2.5 is in a SUM form, whereas EQ 2.6 is in a PRODUCT form. Both equations are logically identical. In a discrete design, the decision as to which form to use may depend on such factors as the relative speed performance, or even the types of gates left over from other areas of a larger design.

When implementing such logic equations in HPL devices, the preferred form is that which "fits" the device architecture most efficiently, and as can be seen, the reversible transposition from one form to another is a relatively simple procedure.

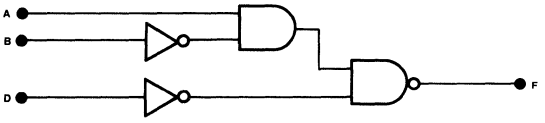


FIGURE 2-2.ANOTHER IMPLEMENTATION FOR FUNCTION F

By direct substitution of the equivalent representation for ANDs, NORs, NANDs and ORs, a multitude of different circuits can be formulated to implement the same function. When designing with 7400 series gates, the designer tailors his circuits to utilize the minimum number of packages. When a logic design requires an extra two input OR gate, but only inverters and AND gates are left, an extra package can be saved by implementing the OR equivalent using three inverters and an AND gate (if the additional propagation delays are permitted). It's no wonder that logic designs take on so many forms. Simple gate equivalent due to DeMorgan is shown in Fig. 2-3.

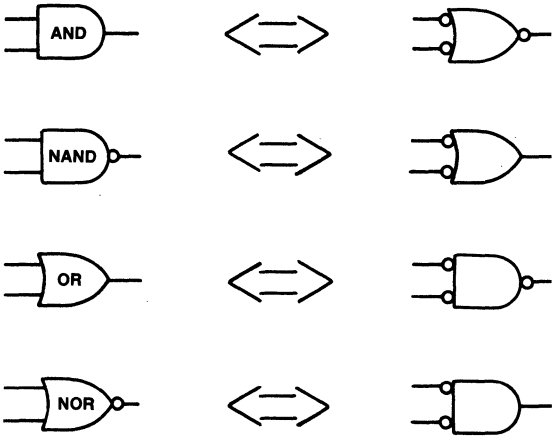


FIGURE 2-3.GATE EQUIVALENCY

What is the common denominator in random logic design? All Boolean equations and their logic representations can be expressed in either of two forms: PRODUCT OF SUMS (POS) or a SUM OF PRODUCTS (SOP). All HPL Programmable logic devices internally implement the SOP form but, certain devices have fixed or programmable output invertors that allows them to generate INVERTED SUM OF PRODUCTS (ISOP) expressions. ISOP expressions can be considered equivalent to POS expressions, demonstrating how output invertors allow SOP devices to implement POS expressions.

2.2.1 SUM OF PRODUCTS EXPRESSIONS

A SOP expression is of the form:
F = A•B•C + A•/B•/C + D•E + F•G

This expression represents the sum of four product terms. Each product term can consist of one or more variables AND'ed together. The logic circuit for this SOP expression is shown as an AND-OR representation in Figure 2-4.

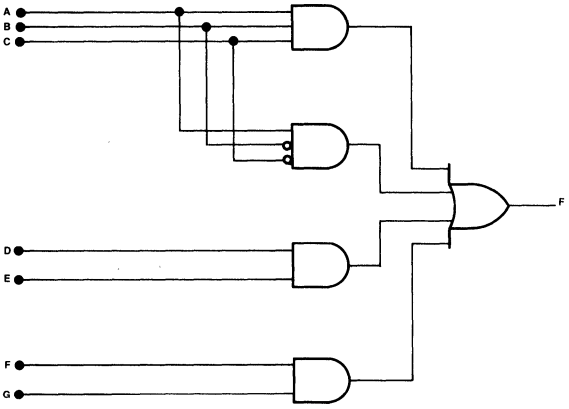


FIGURE 2-4. GENERAL AND-OR SOP IMPLEMENTATION

Any logic expression can be written in SOP notation. For instance, consider expressing the following in SOP form:

F = (A•B•C + D)•(B + D) + A•/C•(B + D)
Expanding, we have:

F = A•B•C + B•D + A•B•C•D + D + A•/C•B + A•/C•D
EQ 2.7 (SOP)

This six product term expression is in SOP form, but is not a minimum SOP. That is, by using Boolean Algebra, F can be simplified to a minimum SOP as shown below:

F = A•B•C•(1 + D) + D•(B + 1)
+ A•/C•B + A•/C•D (Distributive Law)

F = A•B•C + D + A•/C•B + A•/C•D (Theorem 3)

F = A•B•(C + /C) + D•(1 + A•/C) (Distributive Law)

F = A•B + D EQ 2.8
(Theorem 7)

The minimum SOP expression can now be implemented as the simple AND-OR logic circuit as shown in Figure 2-5.

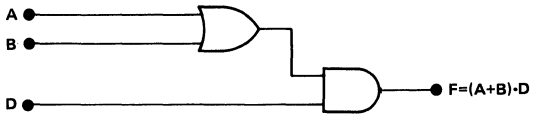


FIGURE 2-5. MINIMUM SOP IMPLEMENTATION

Instead of using Boolean Algebra to reduce the number of product terms, Karnaugh mapping can be used. For example, consider the mapping of the previous function F onto the Karnaugh map of Figure 2-6. Karnaugh maps are a two dimensional representation of a two level logic expression. Normally Karnaugh maps are used to represent expressions involving from two to five variables, although more variables can be handled with increased difficulty. In the example shown in Figure 2-6 a map accomodating four variables is used to represent the four variable expression of EQ 2.7. Note how the six product terms involved are mapped by the intersections of variables, denoted here by ones.

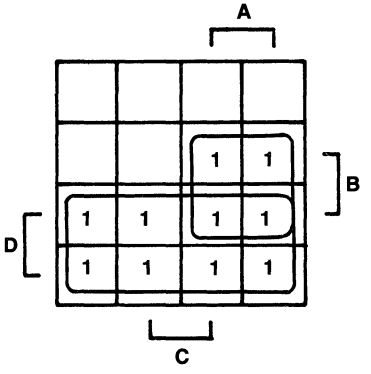


FIGURE 2-6. KARNAUGH MAP OF EQUATION

All six product terms are represented on the above Karnaugh map. The minimization of large logic equations, by the use of Karnaugh maps, is done by grouping adjacent pairs of cells containing ones. The grouping of pairs of cells can be extended to include other pairs of cells.

Figure 2-6 shows how the set of ones which represent EQ 2.7 can be regrouped into the two sets shown, which represent EQ 2.8, the reduced form.

There are many techniques for grouping cells not demonstrated here. For a more complete description, the reader should refer to any comprehensive book covering logic and Boolean Algebra.*

When choosing an HPL device to implement the reduced expression shown in EQ 2.8, it is important to select one that can implement SOP expressions, i.e., either one that has true (not inverted) outputs, or one that has programmable output polarity which can be programmed for true outputs. Otherwise, the user may have to add invertors at the device outputs, which will necessitate the use of another package. Alternately the SOP expression can be converted to the ISOP form as shown in section 2.2.3.1, in which case an inverted output HPL device can be used.

* DIGITAL COMPUTER DESIGN – RAYMOND M. KLINE – PRENTICE HALL INC.

2.2.2 PRODUCT OF SUMS EXPRESSIONS

$$F = (A + /B + C)\cdot(D + E)\cdot(/C + /A)\cdot(/D + /E) \quad \text{EQ 2.9}$$

The above POS expression consists of the product of four SUM terms. Each SUM term can consist of one or more variables OR'ed together. The logic circuit for this POS expression is shown as an OR-AND representation in FIG 2-7.

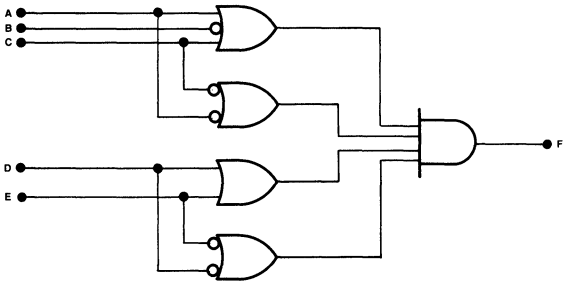


FIGURE 2-7. GENERAL OR-AND POS IMPLEMENTATION

Any logic expression can be written in POS notation. For instance, consider expressing the following in POS form.

$$F = A\cdot/B\cdot/D\cdot(/C + C) + /A\cdot/B\cdot/D\cdot(C + /C) \quad \text{EQ 2.10}$$

Expanding, we have:

$$F = A\cdot/B\cdot/C\cdot/D + A\cdot/B\cdot C\cdot/D + /A\cdot/B\cdot C\cdot/D + /A\cdot/B\cdot/C\cdot/D \quad \text{EQ 2.11}$$

The expression EQ 2.11 is now in the SOP form. DeMorgan's theorem may now be used to convert this expression to the INVERTED PRODUCTS OF SUMS (IPOS) form in EQ 2.12. IPOS is the negated form of POS, in the same way that ISOP is the negated form of SOP.

$$F = /[(/A + B + C + D)\cdot(/A + B + /C + D)\cdot(A + B + /C + D)\cdot(A + B + C + D)] \quad \text{EQ 2.12}$$

This four sum term expression is in IPOS form but is not a minimum IPOS form. That is, by using Boolean Algebra, or Karnaugh mapping, EQ 2.12 can be reduced to a minimized form. Generally it is easier to reduce SOP expressions by Karnaugh mapping. Figure 2-8 shows how EQ 2.11, the SOP version of EQ 2.12, can be reduced using a Karnaugh map.

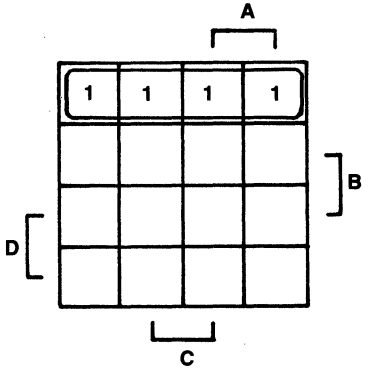


FIGURE 2-8.KARNAUGH MAP OF EQUATION 2.11

All four product terms are represented on the above map. The cell grouping is done using the same methods described in the earlier section on SOP expressions.

As can be seen in Fig 2-8, the cells containing ones can be grouped to represent the reduced function.

F = /B•/D EQ 2.13 (POS)

Notice that because of the simplicity of the actual reduced logic function, the SOP expression of EQ 2.11 appears to reduce on the Karnaugh map to the POS expression of EQ 2.13; this would not normally happen with more complex equations. The complete expression of EQ 2.13 is shown below, and can be seen to have a SOP form.

F = /B•/D + 0 EQ 2.14 (SOP)

Having found the minimum SOP form, DeMorgan's theorem can be used to regenerate the minimum IPOS form as follows:

F = //(/B•/D + 0)	Double Negation
F = /(B + D)•1	DeMorgan's Theorem
F = /(B + D)	Theorem 4
F = /(B + D)	EQ 2.15 (IPOS)

The circuit implementation of the minimum IPOS expression of EQ 2.15 is shown in Figure 2-9.

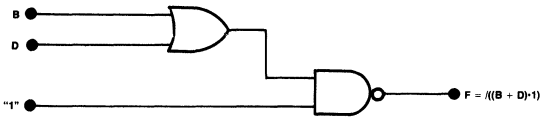


FIGURE 2-9. MINIMUM POS IMPLEMENTATION

Notice that in practice the NAND gate is not required to implement the simple function shown; it is included only to demonstrate that EQ 2.15 is a POS expression, even though one of the SUM terms is invariant ("1").

2.2.3 POS and SOP Equivalence; What Does It Mean?

2.2.3.0 All HPL devices consist of a programmable AND array followed by a fixed or programmable OR array, which may or may not be followed by a stage of inversion (in some HPL devices the outputs are programmable to provide either the true form or the negated form of a function).

Because of the internal structure, all HPL devices implement positive logic functions in either a SUM OF PRODUCTS (SOP) form, or an INVERTED SUM OF PRODUCTS (ISOP) form. Two typical equations demonstrating both forms are shown below:

F = A•B + C•D	SOP
F = /(A•B + C•D)	ISOP

Any logic expression can be expanded to a two level expression; either an AND array followed by an OR array, or an OR array followed by an AND array. An expanded two level expression can have one of four possible forms:

1) SUM OF PRODUCTS	SOP
2) INVERTED SUM OF PRODUCTS	ISOP
3) PRODUCT OF SUMS	POS
4) INVERTED PRODUCT OF SUMS	IPOS

Four typical logic expressions demonstrating the four forms are shown below:

F = A•B + C•D	SOP
F = /(A•B + C•D)	ISOP
F = (A + B)•(C + D)	POS
F = /[(A + B)•(C + D)]	IPOS

FIGURE 2-10.

The logic expression for any discrete random logic circuit (TTL,

CMOS, etc.) can be expanded to one of the four forms shown in Fig 2-10.

Any one of the four forms of expression can be converted to any of the other three forms by the application of the logic laws and theorems described earlier.

Because HPL devices implement SOP or ISOP forms of logic expressions, the most useful conversions to understand are:

SOP ——→ ISOP
ISOP ——→ SOP
POS ——→ ISOP
POS ——→ SOP
IPOS ——→ ISOP
IPOS ——→ SOP

In order to demonstrate the techniques used to perform these six conversions, actual examples are shown in the following sections.

2.2.3.1 SOP → ISOP

F = /B•/D + B•/C	SOP
F = //(/B•/D + B•/C)	Double Inversion
F = /[(B + D)•(/B + C)]	DeMorgan's Theorem
F = /[B•/B + B•C + /B•D + C•D]	Expand
F = /[B•C + /B•D + C•D]	Eliminate Zero Terms
F = /[B•C•D + B•C•/D + /B•C•D + /B•/C•D + B•C•D + /B•C•D]	Expand to Canonical Form*
F = /[B•C•D + B•C•/D + /B•C•D + /B•C•/D]	Combine Common Terms
F = /[B•C + /B•D]	Combine Terms Containing True and Complement Variables Using Distributive Law and Theorem 7
F = /[B•C + /B•D]	ISOP

* CANONICAL FORM IS A FULLY EXPANDED EXPRESSION CONTAINING ALL INPUT VARIABLES.

2.2.3.2 ISOP → SOP

F = /(B•C + /B•D)	ISOP
F = (/B + /C)•(B + /D)	DeMorgan's Theorem
F = /B•B + /B•/D + B•/C + /C•/D	Expand
F = /B•/D + B•/C + /C•/D	Eliminate Zero Terms
F = /B•C•/D + /B•/C•/D + B•/C•D + B•/C•/D + B•/C•/D + /B•/C•/D	Expand to Canonical Form
F = /B•C•/D + B•/C•D + /B•/C•D + B•/C•/D	Combine Common Terms
F = /B•/D + B•/C	Combine Terms Containing True and Complement Variables
F = /B•/D + B•/C	SOP

2.2.3.3 POS → ISOP

F = (/B +/C)•(B + /D)	POS
F = //[(/B + /C)•(B + /D)]	Double Invert
F = /[B•C + /B•D]	DeMorgan's Theorem
F = /[B•C + /B•D]	ISOP

2.2.3.4 POS → SOP

F = (/B + /C)•(B + /D)	POS
F = /B•B + /B•/D + B•/C + /C•/D	Expand
F = /B•/D + B•/C + /C•/D	Eliminate Zero Terms
F = /B•C•/D + /B•/C•/D + B•/C•D + B•/C•/D + B•/C•/D + /B•/C•/D	Expand to Canonical Form
F = /B•C•/D + B•/C•D + /B•/C•/D + B•/C•/D	Combine Common Terms
F = /B•/D + B•/C	Combine Terms Containing True and Complement Variables
F = /B•/D + B•/C	SOP

2.2.3.5 IPOS → ISOP

F = /[(/B + /C)•(B + /D)]	IPOS
F = /[/B•B + /B•/D + B•/C + /C•/D]	Expand
F = /[/B•/D + B•/C + /C•/D]	Eliminate Zero Terms
F = /[/B•C•/D + /B•/C•/D + B•/C•D + B•/C•/D + B•/C•/D + /B•/C•/D]	Expand to Canonical Form
F = /[/B•C•/D + B•/C•D + /B•/C•/D + B•/C•/D]	Combine Common Terms
F = /[/B•/D + B•/C]	Combine Terms Containing True and Complement Variables
F = /[/B•/D + B•/C]	ISOP

2.2.3.6 IPOS → SOP

F = /[(/B + /C)•(B + /D)] IPOS
F = B•C + /B•D DeMorgan's Theorem
F = B•C + /B•D SOP

2.2.3.7 The six conversions described in Sections 2.2.3.1 - 6 will allow the user to convert the logic expression for his random logic circuit to either a SOP or ISOP expression, depending on the type of HPL device to be used.

So for example, if the user, after generating an expanded expression for his random logic circuit,finds that he has an IPOS expression, and he has chosen an HPL device which has inverted outputs (ISOP), he should refer to Section 2.2.3.4 (IPOS → ISOP) for the appropriate method of conversion.

It should be noted from the earlier sections on format conversion that two conversions, POS → ISOP and IPOS → SOP, can be performed by a simple application of DeMorgan's theorem. Two of the other conversions, SOP → ISOP and ISOP → SOP can also be performed simply by using a Karnaugh map technique as follows.

Suppose the following SOP expression is to be converted to the equivalent ISOP form.

F = /B•/D + B•/C SOP

First, the function F is plotted on a three variable Karnaugh map as shown in Fig 2-11.

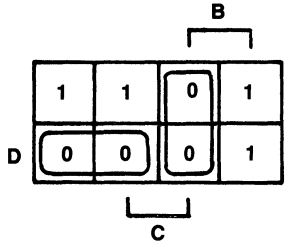


FIGURE 2-11.

If the "0"s or blank cells, which represent /F are grouped, the following expression results:

/F = B•C + /B•D
F = /[B•C + /B•D] ISOP

This result can be seen to be identical to that obtained by the algebraic method shown in Section 2.2.3.1.

An identical technique is used for the ISOP → SOP conversion.

The Karnaugh map can be used for expressions with up to five variables, but above this number it becomes difficult to use, as it becomes increasingly hard for the human eye to identify cell groupings.

2.2.4 Product Term Minimization is Painless

All HPL devices have a maximum number of product terms that are, or can be, assigned to the output OR array.

The maximum number can vary from as little as one to as many as thirty-two product terms (future HPL devices will have more).

The user, after converting his initial logic expression to either a SOP or ISOP form, may find that the HPL device chosen does not have a sufficient number of product terms to implement his expression.

He may then wish to consider product term minimization (PTM) as a possible solution to this problem.

PTM consists of converting a logic expression from the SOP→ISOP, or from ISOP→SOP; inspection of the two forms will then reveal which requires fewer product terms.

If the user already has his expression in both SOP and ISOP form, he needs only to inspect these directly.

Two examples of product term minimization are shown below. The first is an extreme example intended to demonstrate a dramatic reduction of product terms; the second is a more general case.

It is not a general rule that either the SOP or ISOP form of an expression will require fewer product terms (in some cases both require the same), but both forms should be inspected if one desires, or is required, to minimize the number used.

2.2.4.1 Extreme Case

Suppose one must implement the following function in an HPL device with only seven product terms per output:

F = A + B + C + D + E + F + G + H + I EQ 2.16

This equation clearly requires nine product terms, which may deter the user from a seven product term device. But there is a way, a simple application of DeMorgan's theorem will reduce the number of product terms to one!

F = A + B + C + D + E + F + G + H + I	
F = //(A + B + C + D + E + F + G + H + I)	Double Invert
F = /(/A•/B•/C•/D•/E•/F•/G•/H•/I)	DeMorgan's Theorem
F = /[(/A•/B•/C•/D•/E•/F•/G•/H•/I) + 0]	Theorem 1
F = /(/A•/B•/C•/D•/E•/F•/G•/H•/I)	EQ 2.17

The minimized form of F (EQ 2.17) shows that only one product term is required; this is because the original form (EQ 2.16) was a SOP form, and the minimized form is ISOP. This is an extreme case, and such a saving in product terms should not be expected in all cases.

Note that the final equation is in ISOP, and can be implemented in one of three ways.

1) A true output device followed by an external invertor. (Poor solution)
2) A negated output device. (Good solution)
3) A programmable polarity output device with the appropriate output programmed for inversion. (Good solution)

2.2.4.2 General Case

Suppose one must implement the following three product term function, but use the minimum number of product terms.

F = /A•/B + /C + /D EQ 2.18

First, one must convert this SOP expression to the equivalent ISOP form:

F = //(/A•/B + /C + /D)	Double Invert
F = /[(A + B)•(C)•(D)]	DeMorgan's Theorem
F = /[A•C•D + B•C•D]	Expand
F = /[A•B•C•D + A•/B•C•D + A•B•C•D + /A•B•C•D]	Canonical Form
F = /[A•B•C•D + A•/B•C•D + /A•B•C•D]	Combine Common Terms
F = /[A•C•D + /A•B•C•D]	Combine Terms Containing True and Complement Variables
F = /[C•D•(A + /A•B)]	Distributive Law
F = /[A•C•D + B•C•D]	EQ 2.19

Inspection of EQ 2.18 (SOP) and EQ 2.19 (ISOP) shows that the ISOP form requires one less product term than the SOP form.

Again this ISOP form can be implemented in any of the three ways detailed in the previous example.

Notice that EQ 2.19 appears in the third step of the conversion procedure, this will sometimes happen with simple expressions, but the complete rigorous procedure should always be performed to ensure that the correct result is obtained.

A second method for minimizing product terms for expressions containing five or fewer variables is to use a Karnaugh map technique.

The original equation (EQ 2.18) is shown in Karnaugh map form in Fig 2-12.

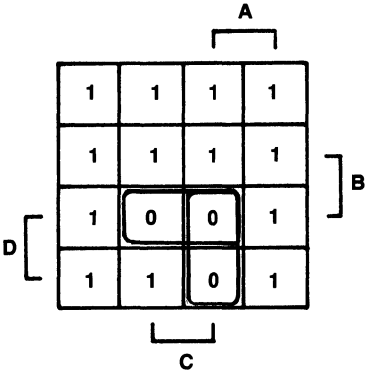


FIGURE 2-12.

The three groupings corresponding to /A•/B or /C or /D are shown on the Karnaugh map of Fig 2-12, but compare these with the minimum grouping of the "0"s; only two groups include all the zeros.

Because the zeros on a Karnaugh map represent /F, we have:

/F = A•C•D + B•C•D
F = /[A•C•D + B•C•D] EQ 2.20

Compare EQ 2.19 and EQ 2.20; they are identical. Karnaugh map PTM is a simple and quick method for reducing product terms because this visual representation helps one to see minimal groupings which are not obvious in an algebraic representation.

HARRIS

HPL™ The Logical Solution
Module 3
HPL-77215/16H8, HPL-77216/16P8
HPL-77209/16L8 Applications

Steven Bennett—HPL Product Marketing

THE HPL™-77209/215/216 are PAL® type devices designed by Harris Semiconductor. The HPL-77209 is a functional equivalent for the 16L8, and features inverting outputs. The HPL-77215 is a proprietary device similar to the 16L8, but features non-inverting outputs. The HPL-77216 is also a proprietary device similar to the 16L8, but includes extra circuitry to allow user configurable output polarity.

The HPL-77209/215/216 parts have been designed to satisfy two requirements. First, they can be used as very effective space saving replacements for existing designs implemented in TTL or LS TTL. Secondly, they are powerful and flexible devices for new designs. They can save the designer from having to think in terms of gates having a fixed number of inputs (74XX Series). This is because full advantage can be taken of their flexible architectures. This contrasts with a 74XX design, where one is often constrained to use parts with more inputs and outputs than are actually needed to implement a particular function. This can be seen if one examines any TTL design; many device inputs are held at a fixed logic level, and some device outputs are not used.

The HPL-77209/215/216 architecture consists of a programmable AND array, followed by a fixed OR array. In addition the HPL-77216 has a programmable invertor included on each output. These configurations implement logic expressions in either SUM OF PRODUCTS (SOP) or INVERTED SUM OF PRODUCTS (ISOP) form. Logic expressions in any other form can be converted to one of the above forms (see Module 2: An Introduction to Boolean Algebra). SOP or ISOP expressions contain by definition two levels of logic. Two level logic expressions are desirable in any logic design because they minimize input to output propagation delay, and also the propagation delays from any input to any output are equal. This not only maximizes throughput, but also helps to eliminate race hazards and other timing problems, making the task of generating timing diagrams much easier. These desirable features are implicit in the architecture of the HPL-77209/215/216, and because they are monolithic devices, the propagation delays from any input pin to any output pin are equal and track well with temperature and supply voltage variations.

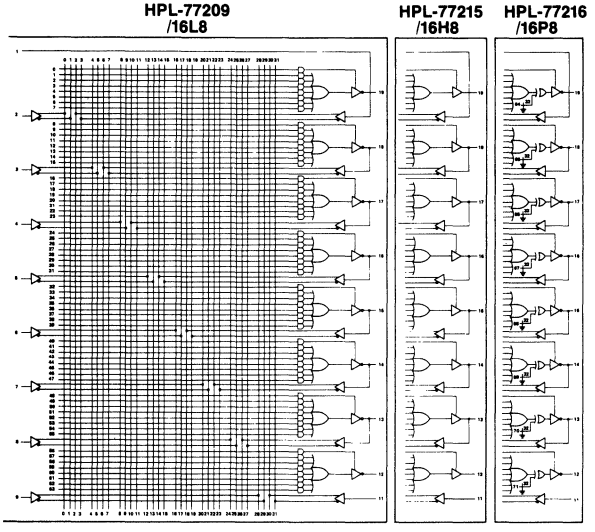
All three devices contain several unique circuit enhancements which allow complete parametric and logical testing of unprogrammed devices at the time of manufacture. This unique on-chip test circuitry (patent pending) known as VOCAL™ (Verification of On Chip Array Logic) allows Harris to perform extensive AC and DC parametric testing over temperature, and also to verify that all the internal logic paths work correctly and according to the published functional diagram. This test circuitry is made use of at wafer probe to identify working devices, and very importantly, it is used again at final package test to ensure that no damage has occurred during the assembly operation. The benefits for the user of this exhaustive testing are very high POST PROGRAMMING FUNCTIONAL YIELD (98%) and pre-tested AC and DC parametrics. The standard HPL programming algorithm is used for all Harris Programmable Logic parts. Special test fuses are included, which are selectively programmed during post manufacturing testing, allowing all the programming circuitry to be tested for correct operation. In addition, this test circuitry allows every fuse in the device to be verified as intact.

Most programmable logic manufacturers guarantee replacement of faulty or out-of-spec devices, but this places the burden of testing functionality and parametrics on the user. Harris' policy is to ship pre-tested devices, removing the test burden from the small user and assuring the large user the highest possible quality.

The following sections of this module cover the design and implementation of a TEN LINE TO BCD/GRAY CODE PRIORITY ENCODER WITH MICROPROCESSOR INTERFACE. This was conceived as a new design and not as a replacement for an existing TTL circuit. The HPL-77216 is used for this design because a mixture of ACTIVE HIGH and ACTIVE LOW outputs is required; however, the design principles shown apply equally well to the HPL-77209 and HPL-77215 parts.

HPL-77209/16L8 HPL-77215/16H8 HPL-77216/16P8

Functional Diagrams



Description

The HPL-77215/216/209 are programmable logic devices designed to be cost effective and space saving replacements for discrete logic designs. These devices are two-level logic elements consisting of 7 product terms (AND) summed (OR) together to generate each of the 8 outputs. An eighth product term associated with each output can drive it to a high impedance state allowing 6 (B0-B5) of the 8 outputs to be used as inputs, either permanently or dynamically.

The HPL-77209 is functionally identical to the industry standard 16L8, and implements logic expressions of the Inverted Sum Of Products (ISOP) form.

THE HPL-77215 is a similar device to the 16L8 but does not include the associated output inversion; it implements logic expressions of the Sum Of Products (SOP) form.

The HPL-77216 is a more flexible device; it includes 8 EX-OR gates in each output path, controlled by 8 extra fuses, allowing the polarity of each output to be user configured. This device can implement a combination of SOP and ISOP expressions.

The HPL-77215/216/209 are field programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

Nickel-chromium fuse technology is used on these and all other HARRIS HPL-77XXX programmable logic devices. The HPL-77215/216/209 are available in 20 pin slimline DIP packages with pinouts identical to the 16L8.

The HPL-77215/216/209 contain unique test circuitry developed by HARRIS which is enabled at the time for manufacture to allow complete AC and DC testing.

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HPL-77215/216/209 -5
(Vcc = 5.0V±5%, T_A = 0°C to +75°C)
HPL-77215/216/209 -2/-8
(Vcc = 5.0V±10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER		MIN	MAX	UNITS	TEST CONDITIONS		
I_{IH}	Input Current	1	—	· 25	µA	V_{IH} Vcc MAX		
I_{IL}	Dedicated Input	0	—	100	µA	V_{IL} 0 4 V	Vcc	Vcc MAX
I_{IFZH}	Output Current	1	—	· 40	µA	V_{FH} Vcc MAX	Vcc	Vcc MAX
I_{IFZL}	Hi-Z State	0	—	40	µA	V_{FL} 0 4V		
I_{IBZH}	Bidirectional Pin Current	1	—	· 40	µA	V_{BH} Vcc MAX	Vcc	Vcc MAX
I_{IBZL}	Hi-Z State	0	—	100	µA	V_{BL} 0 4V		
V_{IH}	Input Threshold (1)	1	2 0	—	V	Vcc Vcc MAX		
V_{IL}	Voltage	0	—	0 8	V	Vcc Vcc MIN		
V_{OH}	High-Level Output Voltage (2)		2 4	—	V	Vcc Vcc MIN	I_{OH}	2 0mA (M) 3 2mA (C)
V_{OL}	Low-Level Output Voltage (2)		—	0 5	V	V_{IL} 0 8V V_{IH} 2 0V	I_{OL}	· 16mA (M) · 24mA (C) (3)
V_{CL}	Input Clamp Voltage (1)		—	1 2	V	I_{IN} 18mA Vcc 0V		
I_{OS}	Output Short Circuit Current (2)		30	130	mA	Vcc 5 0V V_{OUT} 0V One Output for MAX of One Sec		
I_{CC}	Power Supply Current		—	155 (C)	mA	Vcc Vcc MAX		
			—	165 (M)	mA			

C Commercial (5) M Military (2 8)
(1) These specifications apply to both Input (I) and Bidirectional (B) pins
(2) These specifications apply to both Output (F) and Bidirectional (B) pins
(3) One output at a time otherwise 16mA

A.C. SWITCHING CHARACTERISTICS (Operating)

			HPL-77215 5 HPL-77216 5 HPL-77209 5 5V · 5% 0 C to · 75 C		HPL-77215 2/ 8 HPL-77216 2/ 8 HPL-77209 2/ 8 5V · 10% 55 C to · 125 C		
SYMBOL JEDEC STANDARD	SYMBOL OLD SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS
TDVQH1	T_{PD}	Propagation Delay – Input or I/O to Active High Output	—	35	—	45	ns
TDVQL1	T_{PD}	Propagation Delay – Input or I/O to Active Low Output	—	35	—	45	ns
TDVQH2	T_{PZX}	Enable Access Time to Active High Output (1)	TDVQZ1	35	TDVQZ1	45	ns
TDVQL2	T_{PZX}	Enable Access Time to Active Low Output (1)	TDVQZ2	35	TDVQZ2	45	ns
TDVQZ1	T_{PXZ}	Disable Access Time from Active High Output	—	30	—	35	ns
TDVQZ2	T_{PXZ}	Disable Access Time from Active Low Output	—	30	—	35	ns

(1) Enable Access Time is guaranteed greater than Disable Access Time to avoid device contention
NOTE Maximum test frequency is 5MHz with a 50% duty cycle

TEN LINE TO BCD/GRAY CODE PRIORITY ENCODER WITH MICROPROCESSOR INTERFACE

This section covers the design and implementation of a ten line priority encoder with user selectable BCD or GRAY code outputs. Also included are all the necessary control signals to allow direct interface with most microprocessor systems. The final implementation of this design uses the HPL-77216, and has been designed to demonstrate many of the features and flexibilities of this device. The HPL-77216 is basically an asynchronous two level logic array (a programmable AND array followed by a fixed OR array) with feedback. Because the device includes six bi-directional lines, a user may choose to expand the number of inputs from the 10 fixed inputs provided. In this particular design, which calls for 13 inputs, three of the bi-directional pins are used as inputs.

This priority encoder has three main functions, which are:

1. The prioritization and encoding of ten active low inputs. The generated code can be selected to be either BCD or GRAY code. This is determined by logic level applied to the CODE SELECT input pin.

2. The provision of a three stateable output port and associated active low CHIP SELECT input pin suitable for direct interface to most microprocessors.

3. The generation of an active high FLAG output to indicate that one or more of the input pins has been taken to a low logic level. The FLAG output may only become active if the device ENABLE pin is taken to a high logic level.

The features of this priority encoder are as follows. Ten active low inputs are provided for direct connection to either a ten switch keyboard or some other electronic system. When one or more of the 10 inputs is taken to a low logic level, the input with the highest priority (I9 has the highest priority; I0 has the lowest) is encoded to either BCD or GRAY code according to whether the CODE SELECT input is high or low. Table 1 shows the relationship between the various inputs and the code generated. Note that in order to simplify the table, both the BCD and GRAY codes are shown separated by a slash (/) as are the logic levels of the CODE SELECT pin.

BCD/GRAY	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0	D	C	B	A	FLAG
1/0	1	1	1	1	1	1	1	1	1	1	0/0	0/0	0/0	0/0	0
1/0	1	1	1	1	1	1	1	1	1	0	0/0	0/0	0/0	0/0	1
1/0	1	1	1	1	1	1	1	1	0	X	0/0	0/0	0/0	1/1	1
1/0	1	1	1	1	1	1	1	0	X	X	0/0	0/0	1/1	0/1	1
1/0	1	1	1	1	1	1	0	X	X	X	0/0	0/0	1/1	1/0	1
1/0	1	1	1	1	1	0	X	X	X	X	0/0	1/1	0/1	0/0	1
1/0	1	1	1	1	0	X	X	X	X	X	0/0	1/1	0/1	1/1	1
1/0	1	1	1	0	X	X	X	X	X	X	0/0	1/1	1/0	0/1	1
1/0	1	1	0	X	X	X	X	X	X	X	0/0	1/1	1/0	1/0	1
1/0	1	0	X	X	X	X	X	X	X	X	1/1	0/1	0/0	0/0	1
1/0	0	X	X	X	X	X	X	X	X	X	1/1	0/1	0/0	1/1	1

TABLE 1

The four bit code generated by the priority encoder appears at the four bit output port whenever the CHIP SLECT pin is taken to a low logic level; otherwise the port is in a high impedance state. The four bit output port would normally be connected to the least significant nibble of the microprocessor's 8 or 16 bit data bus. The CHIP SELECT pin would normally be connected to the microprocessor's active low READ signal.

An ENABLE input pin is provided to allow the priority encoder to be disabled or enabled under control of the microprocessor. This input pin would normally be connected to a single bit of an output port. When this signal is taken to a low logic level, the four bit output port is forced unconditionally to a high impedance state, and the FLAG output is inhibited. The flag output may be connected to an edge sensitive microprocessor interrupt for fast response, or may be connected to a bit of an input port and polled as desired. Table 2 shows the relationship between the various control signals.

CHIP SELECT	ENABLE	BCD/GRAY	INPUTS	OUTPUTS	FLAG
0	0	X	X	HI-Z	0
0	1	X	X	ACTIVE	ACTIVE
1	0	X	X	HI-Z	0
1	1	X	X	HI-Z	ACTIVE

TABLE 2

The functional block diagram for the priority encoder is shown in Figure 1. An equivalent TTL version for this function would require at least five packages with their attendant increased board space requirement, assembly cost, power consumption, and reduced reliability.

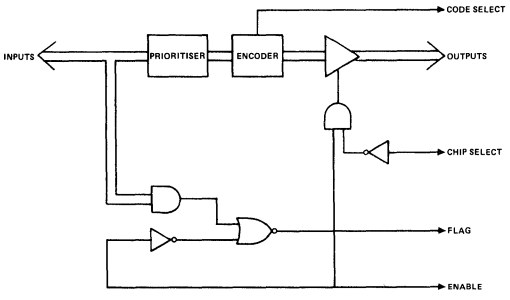


FIGURE 1

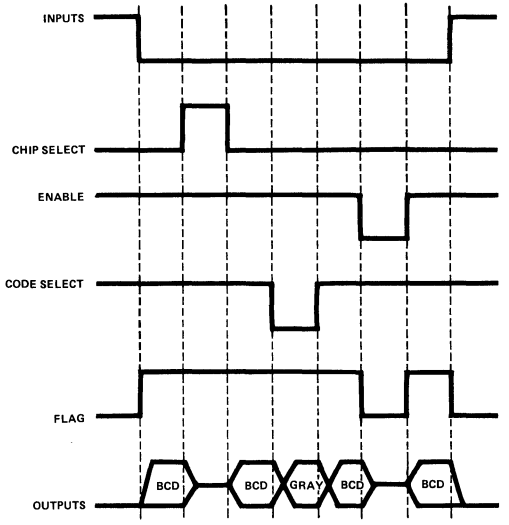


FIGURE 2

The waveform diagram showing the various relationships between the input, output, and control signals is shown in Figure 2. Table 3 shows the pin number, pin name, attributed function, and signal flow for the HPL-77216 used in this application.

PIN NO.	PIN NAME	ATTRIBUTED FUNCTION	SIGNAL FLOW
1	I0	INPUT ZERO	INPUT
2	I1	INPUT ONE	INPUT
3	I2	INPUT TWO	INPUT
4	I3	INPUT THREE	INPUT
5	I4	INPUT FOUR	INPUT
6	I5	INPUT FIVE	INPUT
7	I6	INPUT SIX	INPUT
8	I7	INPUT SEVEN	INPUT
9	I8	INPUT EIGHT	INPUT
11	I9	INPUT NINE	INPUT
12	F0	OUTPUT A	OUTPUT
13	B0	OUTPUT B	OUTPUT
14	B1	OUTPUT C	OUTPUT
15	B2	OUTPUT D	OUTPUT
16	B3	CODE SELECT	INPUT
17	B4	CHIP SELECT	INPUT
18	B5	ENABLE	INPUT
19	F1	FLAG	OUTPUT

TABLE 3

Now that the waveform diagram has been generated (Figure 2), and all the input and output pins have been assigned their desired function, one can now start to develop the various Boolean equations necessary to implement this design. The HPL-77216 is divided into two basic sections. The first section consists of banks of seven product terms; each product term can AND together various combinations of the 10 dedicated inputs and the six bi-directional feedbacks. The second section consists of eight SUM terms, each of which OR together seven product terms in each of the eight banks (refer to an HPL-77216 data sheet).

Referring to the waveform diagram of Figure 2 and the functional diagram of Figure 1, it is now possible to extract the logic equations necessary to implement the four code outputs: A, B, C, and D. As mentioned earlier, the logic levels for both the BCD and GRAY codes are listed adjacent to one another separated by a slash(/). In this application, we shall develop logic equations for those input conditions which cause logical "1s" to appear at the output port, as this requires the least number of product terms. This is not always the case however, so one should always examine both options. Note that whenever a bit of the output port is a logical "1" for both the BCD and GRAY code, one need only generate one product term since the logical condition of the CODE SELECT pin is a "don't care" condition. The logical reduction process is shown below for bit "A" when I1 is taken to a low logic level.

A = /I1.I2.I3.I4.I5.I6.I7.I8.I9.CODE SELECT
+/I1.I2.I3.I4.I5.I6.I7.I8.I9./CODE SELECT

A = /I1.I2.I3.I4.I5.I6.I7.I8.I9.(CODE SELECT + /CODE SELECT)

A = /I1.I2.I3.I4.I5.I6.I7.I8.I9. (1)

A = /I1.I2.I3.I4.I5.I6.I7.I8.I9

The above reduction allows one to use only one product term for both the BCD and GRAY codes. Now one can develop all the equations for each output bit; these are listed in Table 4. Shown below as an example are the equations for bit "D" of the output port. Notice from Table 1 that bit "A" requires seven product terms, bit "B" requires six, bit "C" also requires six, and bit "D" requires only two.

D = /I8.I9 + /I9

Now that the Boolean equations have been developed for the logical prioritization and encoding of the input signals, we can now turn our attention to developing the equations that control the four three state buffers associated with the four bit output port. These control expressions

are designated by the letter "Z", followed by the bit label in parentheses. Referring to the functional block diagram (Figure 1), one can see that the signal required to force the three state buffer to a driving condition is the logical product of the ENABLE signal and the inverted form of the CHIP SELECT signal. As an example, the three state buffer control equation for bit A is shown below. All four are listed in table 4.

Z(A) = ENABLE./CHIP SELECT

Finally, one must now develop the Boolean equations for the FLAG output. Referring again to the functional block diagram (Figure 1), it can be seen that FLAG is the inverted SUM (NOR) of two internal signals, which are the inverted form of the ENABLE signal and an active low signal produced whenever one or more of the inputs is taken to a low logic level. The Boolean equation for the FLAG output is shown below.

FLAG = /[I0.I1.I2.I3.I4.I5.I6.I7.I8.I9. + /ENABLE]

The FLAG output, unlike the four bit output port, is never forced to a high impedance state (Figure 1). The three state buffers of the HPL-77216 require their control product terms to be at a logic high level in order to become active. A logic low forces them to a high impedance condition; therefore, the control equation for the FLAG output is simply a permanent logic one. The equation is shown below.

Z(FLAG) = 1

In a similar way, the control equations for those bi-directional pins used as inputs should be an unconditional logical zero. The control equations for the CODE SELECT, CHIP SELECT, and ENABLE input pins are shown in Table 4.

A = /I1.I2.I3.I4.I5.I6.I7.I8.I9 + /I2.I3.I4.I5.I6.I7.I8.I9.
/CODE SELECT + /I3.I4.I5.I6.I7.I8.I9.CODE SELECT
+ /I5.I6.I7.I8.I9 + /I6.I7.I8.I9./CODE SELECT
+ /I7.I8.I9.CODE SELECT + /I9

B = /I2.I3.I4.I5.I6.I7.I8.I9 + /I3.I4.I5.I6.I7.I8.I9
+/I4.I5.I6.I7.I8.I9./CODE SELECT + /I5.I6.I7.I8.I9.
/CODE SELECT + /I6.I7.I8.I9.CODE SELECT
+ /I7.I8.I9.CODE SELECT

C = /I4.I5.I6.I7.I8.I9 + /I5.I6.I7.I8.I9 + /I6.I7.I8.I9
+ /I7.I8.I9 + /I8.I9./CODE SELECT + /I9./CODE
SELECT

D = /I8.I9 + /I9

FLAG = /[I0.I1.I2.I3.I4.I5.I6.I7.I8.I9 + /ENABLE]

Z(A) = ENABLE./CHIP SELECT

Z(B) = ENABLE./CHIP SELECT

Z(C) = ENABLE./CHIP SELECT

Z(D) = ENABLE./CHIP SELECT

Z(FLAG) = 1

Z(CODE SELECT) = 0

Z(CHIP SELECT) = 0

Z(ENABLE) = 0

TABLE 4

A complete listing of all the equations necessary to implement this design can be found in Table 4. Notice that the FLAG output is inverted whereas the other four outputs are not. This requirement is possible using the HPL-77216 because, although it is functionally identical to the PAL 16L8, it includes eight extra fuses which allow the polarity of the eight outputs to be user selected. Harris Semiconductor also manufactures the HPL-77209, which is a functional equivalent for the active low PAL 16L8, and the HPL-77215, which is an active high version of the HPL-77209. In this way, one of these parts will satisfy any combination of true and inverted outputs.

Now that all the Boolean equations have been derived, the only thing left to do is to program a part and insert it into one's system. However, before a part can be programmed, the Boolean equations must be converted into a form that is acceptable to a programmer. One way to do this is to process the equations using the HELP software support package. (Please contact the factory or your sales office for further information.) Another way to convert the equations is to transpose them onto a standard HPL-77216 programming form. A completed form for this particular design is shown in Figure 3. A blank form can be found inside any HPL-77216 data sheet.

Referring to the programming form (Figure 3), the various input and feedback variables are listed across the top of the form. The outputs are listed down the right hand side of the form. Any input or feedback variable included in a product term is represented by a "1" in the box at the

intersection of the variable and the product term. For example, the FLAG output (F1) uses two product terms (product terms 01 and 02), although any two of the seven product terms associated with the FLAG output (F1) could have been used. Notice that there is a direct correspondence between the variables appearing in the Boolean equations for FLAG (Table 4), and the "1 s" on the programming form. The FLAG output is unconditionally active; therefore, the control term (product term 00) should have all its fuses blown which will force it to an unconditional logic high level. In a similar way, the control terms for ENABLE (B5), CHIP SELECT (B4), and CODE SELECT (B3) should have all their fuses intact forcing the control product terms 08, 16, and 24 to a logic low level. The product terms and control terms used for OUTPUT A (F0), OUTPUT B (B0), OUTPUT C (B1), and OUTPUT D (B2) are completed in a similar manner. Any unused product terms can either be left completely blank or should contain all ones. Also note that the FLAG output is inverted. This is not a problem when using the HPL-77216 as the output polarity is programmable. One simply places a "0" in the box at the intersection of Row 32 and the appropriate output. Those outputs which are required to be noninverting or not specifically inverting should have a "1" placed in their boxes.

After transposing one's expressions onto the programming form, data can be read from the programming form and entered directly into a suitable programmer. The exact procedure for reading off the data from the programming form will vary according to the selected programmer. One should consult the programmer manufacturer for complete information on this procedure.

In conclusion, the author hopes that this module will serve as a worked example of a design using the HPL-77216, and also as a starting point for a user's own designs. The design procedures outlined in this module are equally applicable to other products in the HPL family, including such similar parts as the HPL-77209 and HPL-77215. It should be apparent from this design that the HPL-77216 is eminently suitable for complex and highly integrated new designs, as well as its more traditional role as a replacement for existing random logic designs. Devices of this type are often much more efficient if one uses them to implement new designs and functions, rather than attempting to squeeze old designs into them.

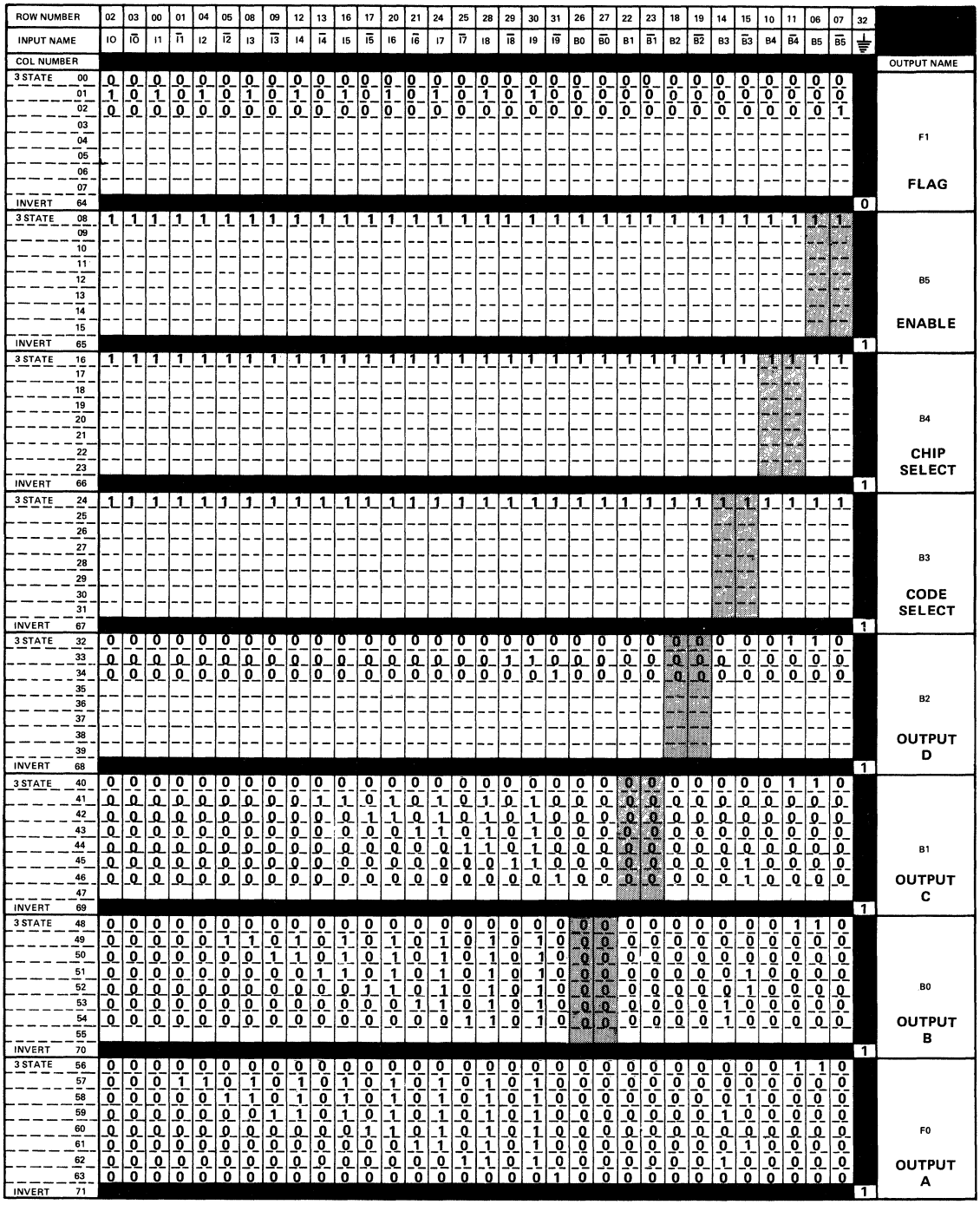

ROW NUMBER
02 03 00 01 04 05 08 09 12 13 16 17 20 21 24 25 28 29 30 31 26 27 22 23 18 19 14 15 10 11 06 07 32
INPUT NAME
I0 Ī0 I1 Ī1 I2 Ī2 I3 Ī3 I4 Ī4 I5 Ī5 I6 Ī6 I7 Ī7 I8 Ī8 I9 Ī9 B0 B̄0 B1 B̄1 B2 B̄2 B3 B̄3 B4 B̄4 B5 B̄5
COL NUMBER
OUTPUT NAME
3 STATE 00
01
02
03
04
05
06
07
INVERT 64
F1
FLAG
3 STATE 08
09
10
11
12
13
14
15
INVERT 65
B5
ENABLE
3 STATE 16
17
18
19
20
21
22
23
INVERT 66
B4
CHIP SELECT
3 STATE 24
25
26
27
28
29
30
31
INVERT 67
B3
CODE SELECT
3 STATE 32
33
34
35
36
37
38
39
INVERT 68
B2
OUTPUT D
3 STATE 40
41
42
43
44
45
46
47
INVERT 69
B1
OUTPUT C
3 STATE 48
49
50
51
52
53
54
55
INVERT 70
B0
OUTPUT B
3 STATE 56
57
58
59
60
61
62
63
INVERT 71
F0
OUTPUT A

FIGURE 3

HPL-77153/82S153 FPLA Applications

Steven Bennett – HPL Product Marketing

The HPL™-77153 has been designed to be a functional and pinout replacement for the SIGNETICS 82S153. The HPL-77153 contains several unique circuit enhancements which allow complete parametric and logical testing of unprogrammed devices at the time of manufacture. The benefits for the user of this exhaustive testing are very high programming functional yield (98%) and tested AC and DC parametrics. Most programmable logic manufacturers guarantee replacement of faulty or out-of-spec devices, but this places the burden of testing functionality and parametrics on the user. Harris' policy is to ship pre-tested devices, removing the test burden from the small user and assuring the large user the highest possible quality.

The HPL-77153 architecture has been designed to satisfy two requirements. First, it can be used as a very effective space saving replacement for existing designs implemented in TTL or LS TTL. Secondly, it is a powerful and flexible piece of hardware for new designs. It avoids the encumbrance of having to think in terms of gates having a fixed number of inputs (74XX Series). As with any programmable device, such as a microprocessor, the HPL-77153 exhibits greatest efficiency in terms of gates replaced when it is used for new designs rather than emulating existing ones. This is because full advantage can be taken of the device flexibility, whereas in a 74XX design, one is often constrained to use parts with more inputs and outputs than are actually needed to implement a particular function. This can be seen if one examines any TTL design; many device inputs are held at a fixed logic level and some device outputs are not used.

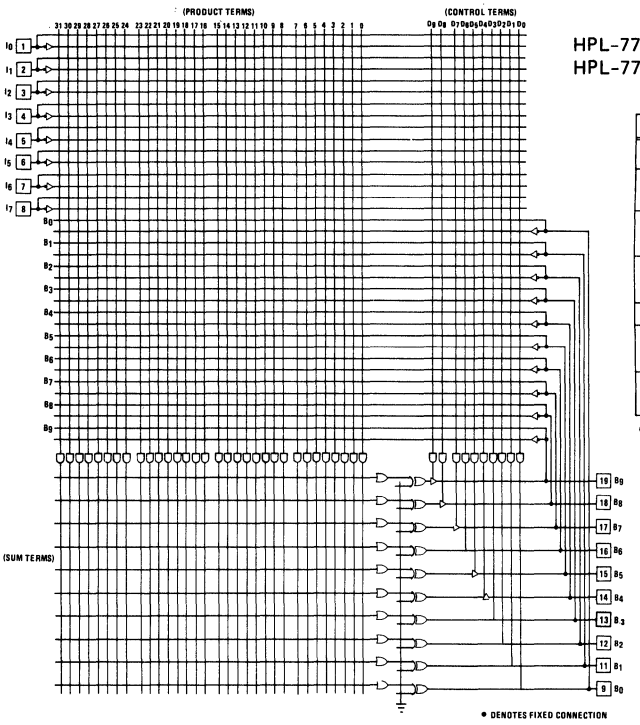
The HPL-77153 architecture consists of two programmable arrays: an AND array followed by an OR array. This configuration generates a device that implements logic expressions in either SUM OF PRODUCTS (SOP) or INVERTED SUM OF PRODUCTS (ISOP) form. Logic expressions in any other form can be converted to one of the above forms (see Module 2: An Introduction to Boolean Algebra). SOP or ISOP expressions contain by definition two levels of logic. Two level logic expressions are desirable in any logic design because they minimize input to output propagation delay, and also the propagation delays from any input to any output are equal. This not only maximizes throughput but also helps to eliminate race hazards and other timing problems, making the task of generating timing diagrams much easier. These desirable features are implicit in the architecture of the HPL-77153 since the propagation delays from any input pin to any ouput pin are equal and track well with temperature and supply voltage changes.

The HPL-77153 uses the same programming algorithm as the 82S153.Special test fuses are included in the HPL-77153.These are selectively programmed during post manufacturing testing. This allows all the programming circuitry to be tested for correct operation. In addition, this test circuitry allows every fuse in the device to be verified as intact. In this way, the user can be assured of very high (98%) fusing yield, and as explained earlier, all functional logic paths are fully tested (100%), allowing a final POST PROGRAMMING FUNCTIONAL YIELD which is virtually identical to the fusing yield (98%). Extensive on-chip test circuits assure the user that the yield and performance of the HPL-77153 will not be subject to the random fluctuations of the manufacturing process. Only Harris Semiconductor's HPL series of programmable logic parts incorporate this unique on-chip test circuitry.

The following sections of this module cover the design and implementation of a high speed data processor for ASCII characters. This was conceived as a new design and not as a replacement for an existing TTL circuit. It is hoped that the efficient use of the HPL-77153 in this design is apparent if compared to a typical random logic replacement application.

Functional Diagram

HPL-77153/82S153



D.C. ELECTRICAL CHARACTERISTICS (Operating)

HPL-77153/82S153 -5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HPL-77153/82S153 -2/-8 (V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER		MIN	MAX	UNITS	TEST CONDITIONS	
I_{IH}	Input Current	"1"	–	+40	A	$V_{IH} = V_{CC}$ MAX	
I_{IL}	Dedicated Input	"0"	–	-100	A	V_{IL} = 0.4V	$V_{CC} = V_{CC}$ MAX
I_{BZH}	Input Current Bidirectional Pin Current Hi-Z State	"1"	–	+40	A	$V_{BH} = V_{CC}$ MAX	$V_{CC} = V_{CC}$ MAX
I_{BZL}		"0"	–	-100	A	V_{BL} = 0.4V	
V_{IH}	Input Threshold Voltage	"1"	2.0	–	V	$V_{CC} = V_{CC}$ MAX	
V_{IL}		"0"	–	0.8	V	$V_{CC} = V_{CC}$ MIN	
V_{OH}	High-Level Output Voltage		2.4	–	V	$V_{CC} = V_{CC}$ MIN V_{IL} = 0.8V V_{IH} = 2.0V	I_{OH} = -2.0mA
V_{OL}	Low-Level Output Voltage		–	0.5	V		I_{OL} = +16mA
V_{CL}	Input Clamp Voltage		–	-1.2	V	I_{IN} = -18mA, V_{CC} = 0V	
I_{OS}	Output Short Circuit Current*	C	-20	-70	mA	V_{CC} = 5.0V, V_{OUT} = 0V	
		M	-15	-85	mA	One output for MAX of One Sec.	
I_{CC}	Power Supply Current	C	–	155	mA	$V_{CC} = V_{CC}$ MAX	
		M	–	165	mA		

C = Commercial (-5) M = Military (-2/-8)

A. C. SWITCHING CHARACTERISTICS (Operating)

SYMBOL JEDEC STANDARD	SYMBOL OLD SYMBOL	PARAMETER	HPL-77153/82S153-5 5V ± 5% 0°C to +75°C MIN	HPL-77153/82S153-5 5V ± 5% 0°C to +75°C MAX	HPL-77153/82S153-2/-8 5V ± 10% -55°C to +125°C MIN	HPL-77153/82S153-2/-8 5V ± 10% -55°C to +125°C MAX	UNITS
TDVQH1	T_{PD}	Propagation Delay-Input or I/O to Active High Output	–	40	–	55	ns
TDVQL1	T_{PD}	Propagation Delay-Input or I/O to Active Low Output	–	40	–	55	ns
TDVQH2	T_{OE}	Enable Access Time to Active High Output	–	35	–	45	ns
TDVQL2	T_{OE}	Enable Access Time to Active Low Output	–	35	–	45	ns
TDVQZ1	T_{OD}	Disable Access Time from Active High Output	–	30	–	45	ns
TDVQZ2	T_{OD}	Disable Access Time from Active Low Output	–	30	–	45	ns

NOTE: Maximum test frequency is 5MHz with a 50% duty cycle.

Description

The HPL-77153/82S153 is a programmable logic device designed to be cost effective and space saving replacement for discrete logic designs. This device is a two-level logic element, consisting of 32 product terms (AND) and 10 sum terms (OR) with fusible links for programming I/O polarity and direction.

All product terms can be linked to 8 inputs (I) and 10 bidirectional I/O lines (B) allowing variable I/O configurations using the 10 direction control gates (C), ranging from 17 inputs and 1 output to 8 inputs and 10 outputs.

On chip T/C buffers allow either True (I, B) and/or Complement (I, B) signals to be linked to any of the product terms, the outputs of which may be used as inputs to any or all of the sum terms. The output polarity of the sum terms is individually programmable by means of a fuse-link controlled EX-OR gate to allow implementation of Sum Of Products (SOP) or inverted Sum Of Products (ISOP) expressions.

The HPL-77153/82S153 is field programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

Nickel-chromium fuse technology is used on these and all other HARRIS HPL-77XXX programmable logic devices. The HPL-77153/82S153 is available in a 20 pin slimline ceramic DIP with a pinout identical to the 82S153. NOTE: The HPL-77152/82S152 (open collector outputs) can also be made available.

The HPL-77153/82S153 contains unique test circuitry developed by HARRIS which is enabled at the time of manufacture to allow complete AC and DC testing.

HIGH SPEED DATA PROCESSOR FOR PARALLEL ASCII CHARACTERS

This application note covers the design and implementation of a multi-function, high speed processing unit for parallel ASCII characters. The final implementation of this design uses the HPL-77153 Field Programmable Logic Array, and has been designed to demonstrate many of the features and flexibilities of this device. The HPL-77153 is basically an asynchronous, two level logic array with feedback; however, careful use of the feedback paths can allow more complex functions, such as latches and flip flops to be implemented. This particular design includes both asynchronous logic and an R.S. flip flop, the designs of which will be shown from first principles.

This ASCII processing unit has three main functions, which are:

1. The detection and flagging of 18 popular ASCII control codes (more could be included if desired).
2. The detection and flagging of two specific control codes. Also, storage of the last control code detected. The two control codes chosen for this particular application are: START OF TEXT (STX) and END OF TEXT (ETX).
3. Removal of the 18 detected control codes from the parallel character stream and their replacement by NULL (NUL) control codes.

The features of this ASCII processing unit are as follows. A seven bit input data bus with an associated input strobe line is used to move ASCII characters into the unit. A seven bit output data bus is used to move the processed ASCII characters out of the unit. This data bus is normally held in a three-state condition, but becomes active whenever a valid character stream is detected, allowing the bussing of more than one device. A valid data output is provided which goes high when the STX control code is detected, and remains high until the ETX control code clears this signal (because two outputs have to be used to implement this R.S. flip flop function, the inverted form of the valid data signal is also available).

The input character stream consists of back to back seven bit characters in parallel form. An associated active low strobe signal is centered in the middle of the character period as shown in FIG. 1.

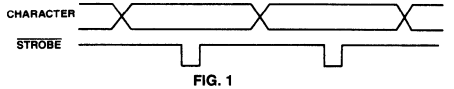


FIG. 1

The strobe signal is used to enable a control code detection flip flop and to indicate when the characters are stable.

The 18 control codes detected by this unit are a subset of the 32 possible control codes included in the ASCII character set. The chosen control codes could be changed for other applications if desired, or more or less could be included. However, because of limitations of the HPL-77153 all 32 cannot be included, although two devices could be paralleled to achieve this. The chosen control codes together with their hexadecimal and binary equivalents are shown in Table 1.

HEX	ASCII CONTROL CODE	BINARY EQUIVALENT I6	I5	I4	I3	I2	I1	I0	CONTROL CODE
02	STX	0	0	0	0	0	1	0	1
03	ETX	0	0	0	0	0	1	1	1
04	EOT	0	0	0	0	1	0	0	1
05	ENQ	0	0	0	0	1	0	1	1
06	ACK	0	0	0	0	1	1	0	1
07	BEL	0	0	0	0	1	1	1	1
08	BS	0	0	0	1	0	0	0	1
09	HT	0	0	0	1	0	0	1	1
0A	LF	0	0	0	1	0	1	0	1
0C	FF	0	0	0	1	1	0	0	1
0D	CR	0	0	0	1	1	0	1	1
10	DLE	0	0	1	0	0	0	0	1
11	DC1	0	0	1	0	0	0	1	1
12	DC2	0	0	1	0	0	1	0	1
13	DC3	0	0	1	0	0	1	1	1
14	DC4	0	0	1	0	1	0	0	1
15	NAK	0	0	1	0	1	0	1	1
1B	ESC	0	0	1	1	0	1	1	1
—	—	ALL OTHER CODES							0

TABLE 1

The block diagram for this design is shown in FIG. 2 and the associated timing diagram in FIG. 3. Having now defined the design, the individual inputs and outputs must be allocated in order implement the block diagram. With reference to the functional diagram of the HPL-77153, Table 2 lists the device pins and their attributed functionality.

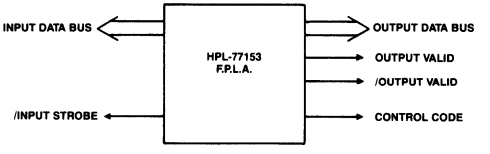


FIG. 2

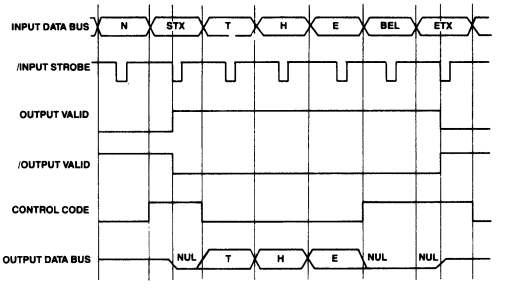


FIG. 3

PIN NO.	PIN NAME	ATTRIBUTED FUNCTION	SIGNAL FLOW
1	I0	INPUT DATA BUS 0	INPUT
2	I1	INPUT DATA BUS 1	INPUT
3	I2	INPUT DATA BUS 2	INPUT
4	I3	INPUT DATA BUS 3	INPUT
5	I4	INPUT DATA BUS 4	INPUT
6	I5	INPUT DATA BUS 5	INPUT
7	I6	INPUT DATA BUS 6	INPUT
8	I7	/INPUT STROBE	INPUT
9	B0	OUTPUT DATA BUS 0	OUTPUT
11	B1	OUTPUT DATA BUS 1	OUTPUT
12	B2	OUTPUT DATA BUS 2	OUTPUT
13	B3	OUTPUT DATA BUS 3	OUTPUT
14	B4	OUTPUT DATA BUS 4	OUTPUT
15	B5	OUTPUT DATA BUS 5	OUTPUT
16	B6	OUTPUT DATA BUS 6	OUTPUT
17	B7	OUTPUT VALID	OUTPUT
18	B8	/OUTPUT VALID	OUTPUT
19	B9	CONTROL CODE	OUTPUT

TABLE 2

Now that the timing diagram FIG. 3 has been generated, and all the input and output pins have been assigned their desired function, one can now start to develop the various Boolean expressions necessary to implement this design. The HPL-77153 FPLA is divided into two basic sections. The first section consists of 32 product terms; each product term can AND together various combinations of the 8 dedicated inputs and the 10 bi-directional feedbacks. The second section consists of 10 SUM terms, each of which can OR together various combinations of the 32 product terms (see functional diagram).

Because the HPL-77153 is divided into two separate sections, they can be dealt with separately. The first section to be dealt with should be the PRODUCT term array, followed by the SUM term array. Referring to the timing diagram FIG. 3, we shall now develop the logic equations necessary to implement the output signal called CONTROL CODE. Table 1 lists the 18 ASCII control codes to be detected; it can be seen that each control code can be detected using just one product term. For example, let us assign product term 0 (P0) to detect the STX control code. The necessary Boolean expressions can be extracted directly from the binary equivalent code shown.

P0 = /I0 •I1•/I2•/I3•/I4•/I5•/I6 STX

Whenever a 1 appears in the binary equivalent code, it is replaced by the true value of the input signal and whenever a 0 appears, it is replaced by the complemented value. In a similar way, P1 to P17 can be allocated to the other 17 control codes.

The signal CONTROL CODE should go high whenever any of the 18 control codes are detected; therefore, it should be the logical SUM of the 18 product terms P0 to P17.

B9 = P0+P1+P2+P3+P4+P5+P6+P7+P8+P9+P10
+P11+P12+P13+P14+P15+P16+P17

Note how the flexibility to assign a variable number of product terms to each SUM term allows this design to be implemented. This would not be possible with other devices which have fixed number of product terms per output.

Having developed the expressions for CONTROL CODE, we can now turn our attention to the output signal called OUTPUT VALID and its complement. These signals are the two outputs from an R.S. flip flop implemented internally using the feedback features found in the HPL-77153. Before we can generate the Boolean expressions, we must first go back to basics and develop the logic circuit necessary to implement this flip flop using simple gates, as shown in FIG. 4.

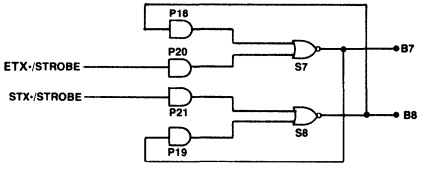


FIG. 4

From FIG. 3, it can be seen that OUTPUT VALID should go high whenever an STX control code is detected and the input strobe goes low; this will be implemented using P21. Also, whenever the ETX control code is detected and the input strobe goes low, then OUTPUT VALID should return low. This is implemented using P20. From FIG. 4, the following Boolean expressions can be extracted:

P18 = B8 R.S. FLIP FLOP FEEDBACK
P19 = B7 R.S. FLIP FLOP FEEDBACK
P20 = I0•I1•/I2•/I3•/I4
•/I5•/I6•/I7 ETX•/STROBE
P21 = /I0•I1•/I2•/I3•/I4
•/I5•/I6•/I7 STX•/STROBE

B7 = /(P18 + P20) OUTPUT VALID
B8 = /(P19 + P21) /OUTPUT VALID

The above expressions will implement the R.S. flip flop shown in FIG. 4. Note that because there is no direct feedback from the bi-directional pins to the SUM array, two product terms, P18 and P19, have to be used for this function. When using feedback paths to implement flip flops, two stages of propagation delay are incurred; therefore, in order to change the state of the flip flop, the minimum length of the INPUT STROBE signal should be equal to or greater than twice the device propagation delay specified in the data sheet.

Referring again to FIG. 3, the last output for which Boolean expressions must be generated are the seven outputs used to form the OUTPUT DATA BUS (B0-B6). One of the functions of this design is to replace the 18 detected control codes by NUL codes (all outputs low). All normal data characters are passed straight through the device. The signal used to force a NUL character onto the OUTPUT DATA BUS is CONTROL CODE. Therefore, each OUTPUT

DATA BUS line should consist of the appropriate INPUT DATA BUS line logically AND'd with the complement of the CONTROL CODE signal. As an example, the Boolean expressions for OUTPUT DATA BUS 0 are shown below.

P22 = I 0•/B9 INPUT DATA BUS 0
•/CONTROL CODE
B0 = P22 OUTPUT DATA BUS 0

In a similar way, the other six sets of expressions for B1-B6 can be developed.

The last function that must be implemented for this design is the three-state control of the OUTPUT DATA BUS. Whenever OUTPUT VALID is active, then the OUTPUT DATA BUS is also active; otherwise, it is held in a three-state condition. It can be seen from the functional diagram of the HPL-77153 that there are 10 control terms (D0-D9) which are used to disable the output drivers on the 10 bi-directional lines (B0-B9). Because we want all seven lines of the OUTPUT DATA BUS (B0-B6) to be active or three-state at the same time, the Boolean expressions for each associated control term will be identical. For example, the expression for the three-state control product term for OUTPUT DATA BUS 0 is shown below:

D0 = B7 B0 THREE-STATE CONTROL

Lastly, note that 10 EXCLUSIVE OR gates, controlled by 10 fuses, are included in the HPL-77153. This allows the user to invert the polarity of any or all of the outputs. In this example, the only outputs which are required to be inverted are B7 and B8. How the condition of these fuses is specified will be dealt with later, in the section covering conversions of Boolean expressions to the final programming table. Table 3 is a complete listing of all expressions developed so far.

Now that all the Boolean expressions have been derived, the only thing left to do is to program a part and plug into one's system. However, before a part can be programmed, the Boolean expressions must be converted into a form that is acceptable to a programmer. One way to do this is to process the expressions using the H.E.L.P. software support package. H.E.L.P. is a large and sophisticated software support package available on-line from Harris Semiconductor's Melbourne facility. (Please contact the factory or your local sales office for further information.) The final output from H.E.L.P. can be used to generate a paper tape or can be fed directly into a suitable programmer via a communications link. Another way to convert the expressions is to transpose them onto a standard HPL-77153 programming form. A completed form for this particular design is shown in FIG. 5. The transposition is fairly simple, and its execution should become apparent if one compares the expressions listed in Table 3 with the completed programming form.

After transposing one's expressions onto the programming form, data can be read from the programming form and entered directly into a suitable programmer. The exact procedure for reading off the data from the programming form will vary according to the selected programmer. One should consult the manufacturer of one's programmer for complete information on this procedure.

In conclusion, the author hopes that this module will serve as a worked example of a design using the HPL-77153, and also as a starting point for a user's own designs. It should be apparent from this design that the HPL-77153 is eminently suitable for complex and highly integrated new designs , as well as its more traditional role as a replacement for existing random logic designs. Devices of this type are often much more efficient if one uses them to implement new designs and functions, rather than attempting to squeeze old designs into them.

PRODUCT TERMS

P0 = /I0•I1•/I2•/I3•/I4•/I5•/I6	STX
P1 = I0•I1•/I2•/I3•/I4•/I5•/I6	ETX
P2 = /I0•/I1•I2•/I3•/I4•/I5•/I6	EOT
P3 = I0•/I1•I2•/I3•/I4•/I5•/I6	ENQ
P4 = /I0•I1•I2•/I3•/I4•/I5•/I6	ACK
P5 = I0•I1•I2•/I3•/I4•/I5•/I6	BEL
P6 = /I0•/I1•/I2•I3•/I4•/I5•/I6	BS
P7 = I0•/I1•/I2•I3•/I4•/I5•/I6	HT
P8 = /I0•I1•/I2•I3•/I4•/I5•/I6	LF
P9 = /I0•/I1•I2•I3•/I4•/I5•/I6	FF
P10 = I0•/I1•I2•I3•/I4•/I5•/I6	CR
P11 = /I0•/I1•/I2•/I3•I4•/I5•/I6	DLE
P12 = I0•/I1•/I2•/I3•I4•/I5•/I6	DC1
P13 = /I0•I1•/I2•/I3•I4•/I5•/I6	DC2
P14 = I0•I1•/I2•/I3•I4•/I5•/I6	DC3
P15 = /I0•/I1•I2•/I3•I4•/I5•/I6	DC4
P16 = I0•/I1•I2•/I3•I4•/I5•/I6	NAK
P17 = I0•I1•/I2•I3•I4•/I5•/I6	ESC
P18 = B8	R.S. FLIP FLOP FEEDBACK
P19 = B7	R.S. FLIP FLOP FEEDBACK
P20 = I0•I1•/I2•/I3•/I4•/I5•/I6•/I7	ETX•/STROBE
P21 = /I0•I1•/I2•/I3•/I4•/I5•/I6•/I7	STX•/STROBE
P22 = I0•/B9	INPUT DATA BUS 0•/CONTROL CODE
P23 = I1•/B9	INPUT DATA BUS 1•/CONTROL CODE
P24 = I2•/B9	INPUT DATA BUS 2•/CONTROL CODE
P25 = I3•/B9	INPUT DATA BUS 3•/CONTROL CODE
P26 = I4•/B9	INPUT DATA BUS 4•/CONTROL CODE
P27 = I5•/B9	INPUT DATA BUS 5•/CONTROL CODE
P28 = I6•/B9	INPUT DATA BUS 6•/CONTROL CODE
P29 = NOT USED	
P30 = NOT USED	
P31 = NOT USED	

SUM TERMS

B0 = P22	OUTPUT DATA BUS 0
B1 = P23	OUTPUT DATA BUS 1
B2 = P24	OUTPUT DATA BUS 2
B3 = P25	OUTPUT DATA BUS 3
B4 = P26	OUTPUT DATA BUS 4
B5 = P27	OUTPUT DATA BUS 5
B6 = P28	OUTPUT DATA BUS 6
B7 = /(P18 + P20)	OUTPUT VALID
B8 = /(P19 + P21)	/OUTPUT VALID
B9 = P0+P1+P2+P3+P4+P5+P6+P7+P8+P9 +P10+P11+P12+P13+P14+P15+P16+P17	

CONTROL TERMS

D0 = B7	B0 THREE-STATE CONTROL
D1 = B7	B1 THREE-STATE CONTROL
D2 = B7	B2 THREE-STATE CONTROL
D3 = B7	B3 THREE-STATE CONTROL
D4 = B7	B4 THREE-STATE CONTROL
D5 = B7	B5 THREE-STATE CONTROL
D6 = B7	B6 THREE-STATE CONTROL
D7 = 1	UNCONDITIONALLY ACTIVE
D8 = 1	UNCONDITIONALLY ACTIVE
D9 = 1	UNCONDITIONALLY ACTIVE

EXCLUSIVE OR FUSES

B0 = INTACT	NON-INVERTING
B1 = INTACT	NON-INVERTING
B2 = INTACT	NON-INVERTING
B3 = INTACT	NON-INVERTING
B4 = INTACT	NON-INVERTING
B5 = INTACT	NON-INVERTING
B6 = INTACT	NON-INVERTING
B7 = PROGRAMMED	INVERTING
B8 = PROGRAMMED	INVERTING
B9 = INTACT	NON-INVERTING

TABLE 3

HPL-77153 FPLA PROGRAMMING FORM

PROGRAM TABLE ENTRIES:

I, B(I) (AND)

INACTIVE	O
I, B	H
I, B	L
Don't Care	—

B(O) (OR)

ACTIVE	A
INACTIVE	•

B(O) (POL)

HIGH	H
LOW	L

NOTES
1. The FPLA is shipped with all links intact. Thus a background of entries corresponding to states of virgin links exists in the table, shown BLANK for clarity.
2. Unused I and B bits in the AND array are normally programmed Don't Care (—).
3. Unused product terms can be left blank.

																					POLARITY	H	L	L	H	H	H	H	H	H	H
TERM	AND I								AND B(I)												OR B(O)												
	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0
0	—	L	L	L	L	L	H	L	—	—	—	—	—	—	—	—	—	—	A	•	•	•	•	•	•	•	•	•
1	—	L	L	L	L	L	H	H	—	—	—	—	—	—	—	—	—	—	A	•	•	•	•	•	•	•	•	•
2	—	L	L	L	L	H	L	L	—	—	—	—	—	—	—	—	—	—	A	•	•	•	•	•	•	•	•	•
3	—	L	L	L	L	H	L	H	—	—	—	—	—	—	—	—	—	—	A	•	•	•	•	•	•	•	•	•
4	—	L	L	L	L	H	H	L	—	—	—	—	—	—	—	—	—	—	A	•	•	•	•	•	•	•	•	•
5	—	L	L	L	L	H	H	H	—	—	—	—	—	—	—	—	—	—	A	•	•	•	•	•	•	•	•	•
6	—	L	L	L	H	L	L	L	—	—	—	—	—	—	—	—	—	—	A	•	•	•	•	•	•	•	•	•
7	—	L	L	L	H	L	L	H	—	—	—	—	—	—	—	—	—	—	A	•	•	•	•	•	•	•	•	•
8	—	L	L	L	H	L	H	L	—	—	—	—	—	—	—	—	—	—	A	•	•	•	•	•	•	•	•	•
9	—	L	L	L	H	H	L	L	—	—	—	—	—	—	—	—	—	—	A	•	•	•	•	•	•	•	•	•
10	—	L	L	L	H	H	L	H	—	—	—	—	—	—	—	—	—	—	A	•	•	•	•	•	•	•	•	•
11	—	L	L	H	L	L	L	L	—	—	—	—	—	—	—	—	—	—	A	•	•	•	•	•	•	•	•	•
12	—	L	L	H	L	L	L	H	—	—	—	—	—	—	—	—	—	—	A	•	•	•	•	•	•	•	•	•
13	—	L	L	H	L	L	H	L	—	—	—	—	—	—	—	—	—	—	A	•	•	•	•	•	•	•	•	•
14	—	L	L	H	L	L	H	H	—	—	—	—	—	—	—	—	—	—	A	•	•	•	•	•	•	•	•	•
15	—	L	L	H	L	H	L	L	—	—	—	—	—	—	—	—	—	—	A	•	•	•	•	•	•	•	•	•
16	—	L	L	H	L	H	L	H	—	—	—	—	—	—	—	—	—	—	A	•	•	•	•	•	•	•	•	•
17	—	L	L	H	H	L	H	H	—	—	—	—	—	—	—	—	—	—	A	•	•	•	•	•	•	•	•	•
18	—	—	—	—	—	—	—	—	—	H	—	—	—	—	—	—	—	—	•	•	A	•	•	•	•	•	•	•
19	—	—	—	—	—	—	—	—	—	—	H	—	—	—	—	—	—	—	•	A	•	•	•	•	•	•	•	•
20	L	L	L	L	L	L	H	L	—	—	—	—	—	—	—	—	—	—	•	•	A	•	•	•	•	•	•	•
21	L	L	L	L	L	L	H	H	—	—	—	—	—	—	—	—	—	—	•	A	•	•	•	•	•	•	•	•
22	—	—	—	—	—	—	H	L	—	—	—	—	—	—	—	—	—	—	•	•	•	•	•	•	•	•	•	A
23	—	—	—	—	—	—	H	—	L	—	—	—	—	—	—	—	—	—	•	•	•	•	•	•	•	•	A	•
24	—	—	—	—	—	H	—	—	L	—	—	—	—	—	—	—	—	—	•	•	•	•	•	•	•	A	•	•
25	—	—	—	—	H	—	—	—	L	—	—	—	—	—	—	—	—	—	•	•	•	•	•	•	A	•	•	•
26	—	—	—	H	—	—	—	—	L	—	—	—	—	—	—	—	—	—	•	•	•	•	•	A	•	•	•	•
27	—	—	H	—	—	—	—	—	L	—	—	—	—	—	—	—	—	—	•	•	•	•	A	•	•	•	•	•
28	—	H	—	—	—	—	—	—	L	—	—	—	—	—	—	—	—	—	•	•	•	A	•	•	•	•	•	•
29	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	A	A	A	A	A	A	A	A	A	A
30	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	A	A	A	A	A	A	A	A	A	A
31	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	A	A	A	A	A	A	A	A	A	A
D9	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—										
D8	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—										
D7	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—										
D6	—	—	—	—	—	—	—	—	—	—	H	—	—	—	—	—	—	—										
D5	—	—	—	—	—	—	—	—	—	—	H	—	—	—	—	—	—	—										
D4	—	—	—	—	—	—	—	—	—	—	H	—	—	—	—	—	—	—										
D3	—	—	—	—	—	—	—	—	—	—	H	—	—	—	—	—	—	—										
D2	—	—	—	—	—	—	—	—	—	—	H	—	—	—	—	—	—	—										
D1	—	—	—	—	—	—	—	—	—	—	H	—	—	—	—	—	—	—										
D0	—	—	—	—	—	—	—	—	—	—	H	—	—	—	—	—	—	—										
PIN	8	7	6	5	4	3	2	1	19	18	17	16	15	14	13	12	11	9										

FIG. 5

Module 5

Testability For Programmable Logic

By Steven Bennett—HPL Product Marketing

WHY TEST SEMICONDUCTOR DEVICES?

The obvious answer to this question is, "to be sure that they work", but what do we mean by "work"? A generally accepted description of a working part is one which will perform correctly in any system that does not violate the part's published specifications. Specifications for digital integrated circuits can be divided into three easily identifiable sections as shown below.

1. FUNCTIONAL SPECIFICATION: Describes precisely the way in which the device operates. Input stimuli (if any) and subsequent output response are presented in a rigorous and generally understood format. The functional specification is generally independent of the technology employed; for example, an "AND" gate is an "AND" gate whether it is implemented using Schottky TTL or relays.

2. STATIC ELECTRICAL (DC) SPECIFICATIONS: Describe precisely what input voltages are required to guarantee particular logic levels, what output voltages are used to represent particular logic levels, what currents flow at device inputs, what drive current capability the outputs have, what supply current is consumed, and several other less important specifications. In contrast to the functional specification, the DC specifications depend to a greater extent on the technology employed. For example, one would expect the supply current of a CMOS part to be much less than an equivalent BIPOLAR part, although the output drive capability could be similar.

3. DYNAMIC SWITCHING (AC) SPECIFICATIONS: Describe precisely what maximum (and in some cases minimum) propagation delay can be expected at an output in response to some external or internal stimulus, what input timing requirements must be met to insure correct operation, such as set up and hold times, pulse widths and others. In contrast to the functional specification, the AC specifications are almost totally dependent on the technology employed.

Every integrated circuit, whether it is a complex microprocessor or a simple logic gate, should have an associated data sheet showing the FUNCTIONAL, STATIC, and DYNAMIC specifications. Semiconductor manufacturers may at their discretion TEST, GUARANTEE, or TEST AND GUARANTEE the various specifications. TEST means that a specification is actually tested at the time of manufacture; GUARANTEE means that a specification is not tested, but the manufacturer will take back any part not meeting that specification. TEST AND GUARANTEE means that a specification is not only tested at the time of manufacture, but the manufacturer will take back any part not meeting that specification (an unlikely event). Manufacturers TEST AND GUARANTEE most specifications with a few exceptions, such as input and output capacitances, which are difficult to measure in a manufacturing environment, and normally do not fluctuate to any great degree. Such specifications are normally only GUARANTEED.

All specifications discussed so far have been boundary specifications (minimum or maximum). Some manufacturers show "TYPICAL" specifications, which are of little use to anyone but the most casual designer, because generally these specifications are not only untested but are not even guaranteed. Designing a system using the typical specifications of integrated circuits could cause a system to fail permanently or intermittently with variations of temperature or power supply.

PROGRAMMABLE LOGIC IS NO EXCEPTION

Since the first integrated circuit was developed, FUNCTIONAL and PARAMETRIC testing was a relatively simple matter because the devices performed the same function at the time of manufacture as they did when they were in the customer's equipment; therefore, they could be exhaustively tested. A hint that this utopian state of affairs was not to last came with the invention of the non-erasable PROM. This was the first device where the customer had control over the final function. The FUSIBLE LINK had arrived and offered customers tremendous flexibility to generate their own proprietary designs, but at the same time generated increased testing difficulties for the manufacturer. Ingenious schemes were devised to allow predictions of FUSING YIELD, such as the inclusion of extra fuses not available to the user, which could be programmed and verified at manufacture. Additional schemes allowed measurement of DC and AC parameters. A simple form of test circuitry had been invented and, because PROMs were simple repetitive structures, it worked reliably and efficiently.

The floodgates were finally flung open with the invention of PROGRAMMABLE LOGIC devices. The first manufacturers of these devices made a fundamental error by only including the same type of simple test circuitry that was used for PROMs; such devices are called FIRST GENERATION. A programmable logic device can be considered as an array of LOGICAL ELEMENTS, the function of which is controlled by an EMBEDDED PROM. The manufacturers of first generation devices incorporated all the test circuitry necessary to test the EMBEDDED PROM,

but unfortunately, they did not include any circuitry to test the integrity, functionality and specifications of the LOGICAL ELEMENTS. As a result, the early manufacturers could predict the FUSING YIELD of their parts, but had absolutely no information to indicate whether the part would function correctly after programming. These difficulties were compounded by the inclusion on almost all devices of a new feature called USER CONFIGURABLE DYNAMIC THREE-STATE. This facility allowed the user to decide when the outputs should be active, and when they should not. Unfortunately, one of the results of this feature was that all the outputs of an unprogrammed part were unconditionally in a HIGH IMPEDANCE condition. This prevented many important device parameters from being measured, and resulted in virtually untested parts being shipped. The only parameters which could be measured on a FIRST GENERATION device were INPUT CURRENT, OUTPUT LEAKAGE and SUPPLY CURRENT. Vitally important specifications, such as INPUT THRESHOLDS, OUTPUT VOLTAGES and CURRENTS, DYNAMIC (AC), and FUNCTIONALITY were not being tested. One manufacturer of programmable logic devices recognized some of the problems, and attempted a correction on some of their later parts. They did this by including test circuitry which could be used to activate the THREE-STATE output buffers, allowing some STATIC (DC) parametric testing to be done at WAFER PROBE. This testing could only be performed at WAFER PROBE because the signals that activated the test circuitry were connected to extra BOND PADs on the DIE which were not bonded out at PACKAGE ASSEMBLY.

The result was that packaged devices could still not be tested, so it was not possible to measure parameters over temperature.

The testability of FIRST GENERATION programmable logic devices was to remain in this primitive state for a number of years; indeed, such parts are still being manufactured today. This lack of testability has been responsible for much user frustration with marginally and non-working parts. However, this did not deter the use of such parts because, even with all their limitations, programmable logic gave the customer some very valuable and cost-effective features.

HPL GENERIC TESTABILITY IS THE ANSWER

It was only with the emergence of HPL (Harris Programmable Logic) from Harris Semiconductor in 1982 that the problems of functional and parametric testing were finally addressed in a complete and rational way. HPL is an advanced SECOND GENERATION range of products which feature complete FUNCTIONAL and PARAMETRIC testing OVER TEMPERATURE in PACKAGED FORM on UNPROGRAMMED DEVICES. The implementation of this test philosophy is so novel that at this date a patent is pending. The HPL test philosophy is known as VOCAL™ (Verification of On Chip Array Logic), and is incorporated in all HPL products, including PAL®, IFL™, and Harris proprietary parts.

All non-erasable programmable devices, including PROMs and programmable logic, should exhibit three distinct modes of operation. The three modes have been defined as shown below:

MODE 1 TEST MODE (Parametric and Functional)

MODE 2 PROGRAMMING MODE (Fuse Program and Verify)

MODE 3 FUNCTIONAL MODE (Normal Operational Mode)

A PROM is not normally equipped for MODE 1 operation because its architecture allows parametric and functional testing to be performed in MODE 3, before it is programmed. Test fusing can be performed in MODE 2. However, this is not the case with programmable logic parts, since unlike a PROM they will not operate in MODE 3 until they have been programmed. So, in order to effectively test programmable logic, MODE 1 is essential; and as was implied earlier, most programmable logic parts, with the exception of HPL, do not exhibit MODE 1 operation. This is why HPL devices are said to have TRI-MODE ™ functionality. If a part does not have MODE 1 capability, how can it be tested? The answer is it cannot be tested until it has been programmed either by the user or the manufacturer. This involves the writing of a special test program for each different pattern, an expensive process. The VOCAL test scheme allows the user to achieve in excess of 98% PPFY (POST PROGRAMMING FUNCTIONAL YIELD – those parts meeting AC, DC, and functional specifications after programming) without performing exhaustive POST PROGRAMMING VECTOR TESTING. MODE 1 operation allows parts not meeting specification to be eliminated during the manufacturing process. Faulty parts without MODE 1 operation cannot be detected until they reach the customer. Therefore, a user of parts without MODE 1 operation will experience a fluctuating PPFY within the range 0% to 95% (average approximately 50% to 80%). HPL devices offer the user virtually the maximum theoretical PPFY attainable today.

HPL FEATURES TRI-MODE™ OPERATION

All HPL products feature three distinct modes of operation, as explained earlier. Two modes are always available to the user: the PROGRAMMING MODE (MODE 2) and the FUNCTIONAL MODE (MODE 3). The TEST MODE (MODE 1) is not generally available to the user because of its proprietary nature; please contact Harris Semiconductor for further information. A complete explanation of the three operational modes follows:

MODE 1 (TEST MODE)

In this mode, the FUNCTIONAL MODE parametrics, both dynamic (A.C.) and static (D.C.), can be measured and verified as being within the published data sheet specifications. The logical functionality can also be verified; in other words, it is possible to verify logically correct operation of all the internal data paths, logic gates, input and output buffers, and miscellaneous circuitry. Note that in this

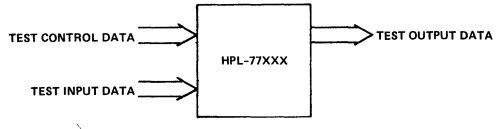
mode, the integrity of the fuse matrix is not checked as this function is reserved for Mode 2. In summary, the basic features of the test mode are:

1. The ability to verify functional DC voltage and current specifications.

2. The ability to verify functional AC switching specifications.

3. The ability to verify logical continuity and functionality of internal data paths and circuit elements.

The TEST MODE is enabled by the correct manipulation of special TEST MODE control pins. TEST MODE control pins are heirarchical functions of the normal FUNCTIONAL MODE pinout. The TEST MODE block diagram for HPL products is shown below.



TEST MODE BLOCK DIAGRAM

The various TEST MODE control signals (when activated) cause specific functional modifications to occur within the device. Various combinations of control signal activation allow many different tests to be performed on unprogrammed parts. The test flow for both wafer and package level devices is shown below. Each test performed actually consists of many sub-tests, as a large number of input/output configurations must be examined.

PACKAGED TEST PERFORMED	HARRIS HPLs	OTHERS	MODE USED
V_{CL}	YES	–	N/A
I_{CC}	YES	–	3 (FUNCTIONAL)
I_{IL}, I_{BZL}, I_{FZL}	YES	–	3 (FUNCTIONAL)
I_{IH}, I_{BZH}, I_{FZH}	YES	–	3 (FUNCTIONAL)
V_{OL}	YES	–	1 (TEST)
V_{OH}	YES	–	1 (TEST)
I_{OS}	YES	–	1 (TEST)
OUTPUT LOGIC FUNCTIONAL	YES	–	1 (TEST)
INPUT BUFFERS FUNCTIONAL	YES	–	1 (TEST)
COLUMN DECODE FUNCTIONAL	YES	–	2 (PROGRAM)
ROW DECODE FUNCTIONAL	YES	–	2 (PROGRAM)
TEST ROW FUSIBILITY	YES	–	2 (PROGRAM)
TEST COLUMN FUSIBILITY	YES	–	2 (PROGRAM)
FUSE MATRIX INTEGRITY	YES	–	2 (PROGRAM)
V_{IH}, V_{IL}	YES	–	1 (TEST)
DYNAMIC (AC) TEST	YES	–	1 (TEST)

PACKAGE DEVICE TESTS PERFORMED AT MANUFACTURE

The above table shows the tests performed on all HPL parts at the time of manufacture. A blank column has been left so the reader may check off any tests performed by other manufacturers for comparison. Note that all these tests are performed on packaged devices; some manufacturers can do some of these tests on unpackaged die, but this is no guarantee that the final packaged parts will work.

Most of the above tests are self-explanatory, with the possible exception of "OUTPUT LOGIC FUNCTIONAL". Some HPL products include user configurable output logic, or output conditioning, such as EX-OR GATES, THREE-STATE BUFFERS and others, which are controlled by configuration fuses. It is this logic which is verified as working correctly during the "OUTPUT LOGIC FUNCTIONAL" test.

POST PROGRAMMING TEST CAPABILITY

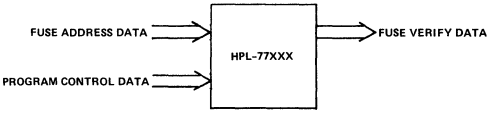
The TEST MODE capability is retained even after device programming, allowing detailed non-invasive analysis of any parts returned to Harris Semiconductor as non-functional or programming failures. This ability to take an electronic "X-RAY" of returned parts allows Harris to advise the customer of the exact nature of the fault.

MODE 2 (PROGRAMMING MODE)

In this mode, the integrity of the fuse matrix is verifiable; in other words, it is possible to verify that all the fuses in an unprogrammed device are intact. Also, individual fuses are capable of being selectively programmed in order to generate the overall logical functionality required by the user. Lastly, it is possible to verify that programmed fuses have programmed correctly, and that fuses desired not to be programmed are still intact. In summary, the basic features of the programming mode are:

1. The ability to selectively read all fuses to determine whether they are intact or programmed. This feature is functional both before and after programming.

2. The ability to selectively program individual fuses without erroneously programming non-selected fuses, or electrically or thermally overstressing or damaging the device.



PROGRAM MODE BLOCK DIAGRAM

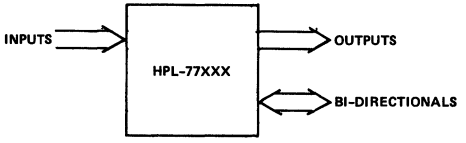
Complete information on the programming and subsequent verification of HPL parts can be found in the individual device data sheets. The HPL programming mode pinout and programming algorithm is generic to all HPL products to this date; however, in accord with Harris' policy of supplying the customer with the highest possible quality, future products may include enhancements to the basic programming scheme. The programming scheme has been designed to minimize stresses to the device being programmed; this is another difference between FIRST and SECOND GENERATION parts.

MODE 3 (FUNCTIONAL MODE)

In this mode, the device functions and meets all the AC and DC parametrics shown in the published data sheet. It will also exhibit the logical functionality which the user creates by selectively progamming fuses. In summary, the basic

features of the functional mode are:

1. Exhibition of correct AC and DC and logical functionality.



FUNCTIONAL MODE BLOCK DIAGRAM

Complete information on the functional mode operation of HPL parts can be found in the individual device data sheets. In this mode, non-proprietary HPL parts are functionally equivalent to the industry standard architectures from which they were developed. All HPL products are designed by Harris Semiconductor and feature many enhancements over earlier products.

SUMMARY

It is hoped that this module has identified the problems associated with the testing of programmable logic devices, and explained in some detail the very comprehensive approach taken by Harris Semiconductor to alleviate these problems. Future Harris products will continue to make use of the VOCAL test philosophy. Enhancements and improvements will be made which will be functionally compatible with existing products using VOCAL.

For further information on this or related subjects, contact ADVANCED PRODUCTS GROUP of SEMICONDUCTOR BIPOLAR DIGITAL PRODUCTS DIVISION.

HARRIS

Harris Programmable Logic (HPL™) Application Note 106

HAZARD FREE LOGIC DESIGN

By Steven Bennett, Senior Marketing Engineer

INTRODUCTION

One of the more insidious pitfalls of logic design is the unwitting inclusion of static* (race) hazards into a circuit. Static hazards can cause undesirable glitches (transitory incorrect logic levels) to occur at the output of a logical network under certain input transition conditions. Static hazard is a somewhat inappropriate name for an effect which is only present as a consequence of an input signal transition. Such hazards are caused by unequal propagation delays in different parts of a logical network. This may result from unequal numbers of logical elements in different paths, or using logical elements with different propagation delays, or simply using devices which exhibit propagation delay variation due to transition direction sensitivity (most logical devices). No matter how carefully the various paths are matched within a network, changes in supply voltage, temperature, and node loading will conspire to unbalance them.

Having static hazards present in logical networks is not always undesirable; for example, any network outputs driving other devices not adversely affected by glitches would not be a cause for concern. Devices not sensitive to glitches are LEDs, filament lamps, solenoids, and other level activated components. However, many devices are sensitive to glitches, and these are mainly edge triggered or level sampling digital components, such as latches, registers, flip flops, and counters, to name but a few. Driving edge sensitive inputs on these types of components with the output of network containing static hazards can cause permanent or intermittent system failures.

Static hazards can be a problem, but are they avoidable? Fortunately yes; static hazards can be eliminated by employing well established techniques of Boolean Algebra in one or more of its diverse forms. The following sections show various solutions to this problem, with application to discrete logic, PROM, or programmable logic designs.

* Static hazards in the context of this paper are defined as logical abnormalities in a digital system, and should not be confused with electrostatic discharge induced damage in semiconductor devices.

KARNAUGH MAP EXAMPLE

Consider the simple Boolean expression shown below:

F = /A.C + B./C

It is not immediately obvious that a minimum network implementation of this function would suffer from a static hazard. However, inspection of the Karnaugh Map representation of this function (Figure 1) can make this clear.

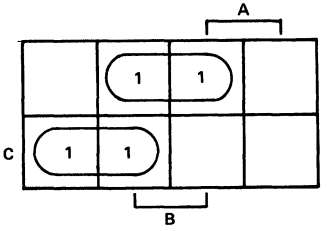


FIGURE 1

The technique for identifying a possible stacic hazard is to search for any adjacent (not diagonally adjacent) cells not grouped together? As can be seen from Figure 1, two cells satisfy this criteria. They are identified by the coordinates /A.B./C and /A.B.C. The gate implementation of Function F is shown in Figure 2.

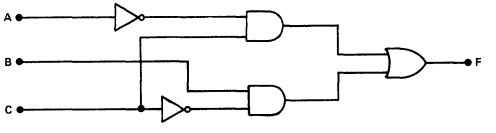


FIGURE 2

The input variable which is different between the two cells, /A.B./C and /A.B.C, is obviously C. Therefore, this is the input variable which could give rise to a static hazard. The waveform diagram generated by holding

A at a low level, B at a high level, and changing C is shown in Figure 3.

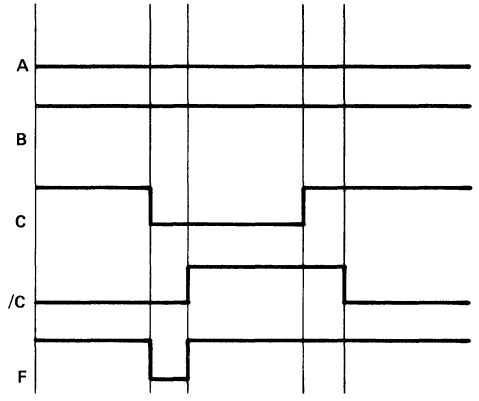


FIGURE 3

Notice how the delay introduced by the C invertor causes a glitch to occur each time C is taken low. The duration of the glitch is approximately equal to the propagation delay of the invertor. Having identified the cause of the glitch, what steps can one take to eleminate it? The solution is elegantly simple: one simply needs to group the two cells, /A.B./C and /A.B.C. This is shown in Figure 4.

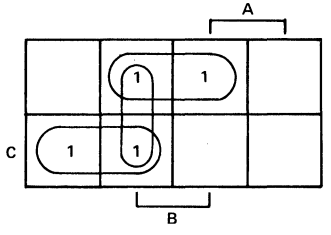


FIGURE 4

Now, the glitch detection criterion mentioned earlier is no longer satisfied. There are now no adjacent cells not grouped together. What implication does this have for the gate level implementation of this function? The new expression for F is shown below:

F' = /A.C + B./C + /A.B

Notice that a new product (AND) term has been generated: /A.B. In terms of gates, one more AND gate, and a three rather than two input OR gate are required. The gate implementation of the new expression for F is shown in Figure 5.

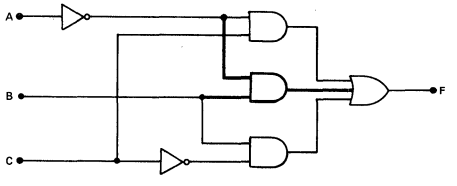


FIGURE 5

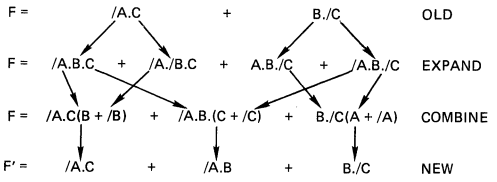
It is left to the reader to show that the circuit of Figure 5 is not prone to glitches caused by changing the state of input C, nor for that matter, A or B. The Karnaugh Map technique shown works well for logic network with up to four or five input variables, but above this number, it becomes increasingly difficult to visualize the cell interrelationships. The next section demonstrates an algebraic method leading up to a more general solution applicable to multi-input programmable logic devices.

ALGEBRAIC EXAMPLE

Examine the function F, from the previous example, shown below.

F = /A.C + B./C

What clue lies locked in this expression that would suggest a possible static hazard? First, the two product terms contain variables that are not mutually exclusive, A and B, and secondly, they contain the true and complement forms of a third variable, C. These two conditions set the stage for a possible static hazard as demonstrated in the previous section. What procedure can we employ to eliminate this problem? Consider the approach taken when using a Karnaugh Map, which is to generate and include a product term to overlay any two product terms contributing to glitch generation. It is possible to use the same approach for the algebraic method as shown below:



The first step is to expand the old expression (F) to its cannonical form. This means expand each product term to include all combinations of "don't care" input variables. For example, B is a "don't care" variable in the product /A.C., and similarly, A is a "don't care" variable in the product B./C. The cannonical form not only would require more gates to implement but would also be prone to glitch generation. The reader may verify this by drawing a Karaugh Map of the cannonical expression; three sets of adjacent cells will be found. The second step is to develop a new product term which overlays the original two product terms. This new product term should be selected from cannonical product terms which differ only by the state of the glitch producing variable, in this case C. This new product term, /A.B, overlays the two original product terms. The cannonical expression can now be reduced with the inclusion of the new product term, /A.B, to the new expression, F'.

This algebraic method is applicable to any Boolean expression, and particularly so for expressions containing five or more input variables. The next section shows how algebraic glitch elimination techniques can be ap-

plied to a real world design using an HPL™ programmable logic device.

PROGRAMMABLE LOGIC EXAMPLE

This example is based around the HPL-77215/16H8, which is a proprietary device designed by Harris Semicondutor. The HPL-77215 is functionally similar to the 16L8, but features active high outputs. It contains two logical arrays: a programmable AND array followed by a fixed OR array. It has 10 fixed inputs, 2 fixed outputs, and 6 bi-directionals. Each output (and bi-directional) has seven product terms OR'd to it. Refer to the HPL-77215 data sheet for further information. The "black box" diagram for the HPL-77215 used in this example is shown in Figure 6.

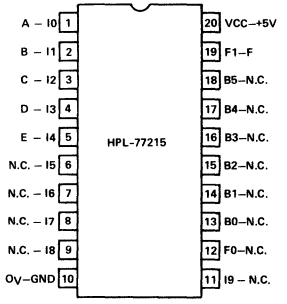
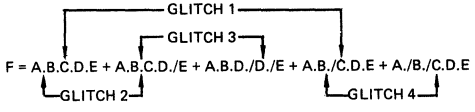


FIGURE 6

Suppose one wishes to implement the expression shown below:

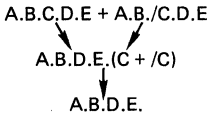
F = A.B.C.D.E + A.B.C./E + A./C.D./E

Function F is intended to drive the clock input of a binary counter. We must therefore check this expression for possible glitch generation and eliminate that possibility if necessary. The first step is to expand F to its cannonical form which is shown below:

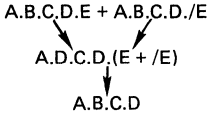


Notice that the cannonical form has four possible glitch generating transitions; however, Glitch 3 and Glitch 4 have been artifically introduced as a result of the expansion process as described earlier. They will disappear when the product terms are recombined and can be ignored. Glitch 1 and 2 are, by contrast, permanent and implicit in the original expression for F. They must be eliminated by developing overlaying product terms as shown below.

GLITCH 1



GLITCH 2



The cannonical form of F may now be reduced to its original form, and the two overlay product terms, A.B.D.E and A.B.C.D, appended as shown below.

F'=A.B.C.D.E + A.B.C./E + A./C.D.E + A.B.D.E + A.B.C.D

Notice that the new expression, F', contains five product terms, whereas the original expression F had only three. This can be accommodated in the HPL-77215 as each output has 7 product terms available.

Now F' can safely be used to drive a binary counter since glitch free operation has been assured by means of two overlay terms. The same procedure can be applied to expressions using more variables which in the case of the HPL-77215 could be up to 16.

CONCLUSION

It is hoped that this application note will prove useful to experienced and inexperienced logic designers alike. The essential theme throughout this paper is that any logic network driving or incorporating edge sensitive devices should be analyzed for possible static hazards. Remember that any such design involving discrete gates, PROMs, or HPL products should be investigated for this possibility. This is particularly important for man-rated applications such as avionics — GOOD HUNTING!

HARRIS

Harris Programmable Logic (HPL™) Application Note 107

SPEED OPTIMIZATION FOR THE HPL-77153 FIELD PROGRAMMABLE LOGIC ARRAY (FPLA) AND OTHER PROGRAMMABLE LOGIC ARCHITECTURES

By Steven Bennett, Senior Marketing Engineer
and Barbara J. Fisher, Design Engineer

INTRODUCTION

This application note explains how to minimize input to output propagation delay when using the HPL-77153 (FPLA). The techniques described are applicable to other devices with similar architectures. Any reduction in propagation delay achieved by these methods is not specified or guaranteed by Harris Semiconductor. These techniques should only be used by customers who have the equipment necessary to perform accurate post-programming propagation delay measurements on every part to be so used. Customers without this equipment should design their systems to tolerate the maximum propagation delay specified in the device data sheet, or contact Harris Semiconductor for information on in house programming and speed optimization.

The HPL-77153 FPLA is a programmable logic device designed by Harris Semiconductor. It is intended to be a highly integrated replacement for designs implemented in low power Schottky TTL. It can also be used to generate totally new designs. The HPL-77153 incorporates the VOCAL™ (Verification of On Chip Array Logic) test system (patent pending). This on-chip test system allows Harris to measure all dynamic (AC) and static (DC) parameters, and to perform functional testing on unprogrammed parts at the time of manufacture.

The HPL-77153 has two main sections. The first section is a fuse programmable AND array where input and feedback variables can be linked to any of 32 PRODUCT terms. The second section is a fuse programmable OR array where PRODUCT terms can be linked to any of 10 SUM terms. Other logical components, such as PROGRAMMABLE OUTPUT INVERTORS, INPUT INVERTORS, and THREE-STATE BUFFERS support these two main sections, but will not be discussed further as they are not relevant to this application note. A symbolic representation of a small part of the HPL-77153 is shown in Figure 1.

The symbols used in Figure 1 are now a standard for representing the internal logic of programmable logic parts. The HPL-77153 operates as follows: true and inverted versions of the input variables, in this case A and B, are generated internally and are available for linking to any of the product terms. A fuse is included at each intersection of an INPUT VARIABLE and a PRODUCT term. This causes each product term, in this example, to be a four input AND gate. In a similar manner, a fuse is included at each PRODUCT term and SUM term intersection, causing each SUM term to be a two input OR gate. At any intersection where it is not desired to make a connection, the fuse at that intersection must be programmed. Unprogrammed fuses may be represented by an X symbol at the intersections.

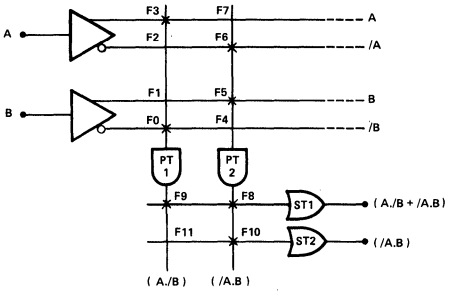


FIGURE 1.

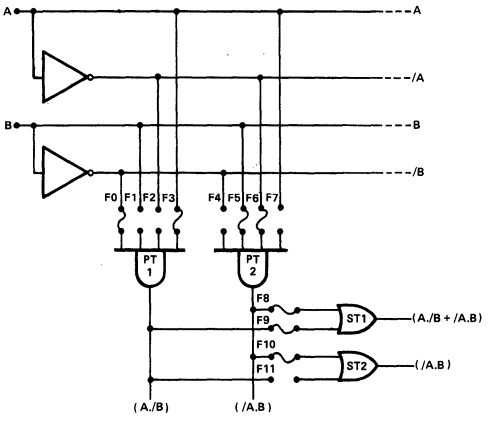


FIGURE 2.

HPL and VOCAL are trademarks of Harris Corporation.

The pattern of fuses shown in Figure 1 generates two different logical expressions and demonstrates the inherent flexibility of the device architecture. An equivalent representation using discrete gates is shown in Figure 2, and has been configured to generate the same logical expressions as Figure 1, to allow the reader to make a direct comparison.

WHY ARE FPLAs PATTERN SENSITIVE

After comparing Figures 1 and 2, it should be obvious that when different fuse patterns are used to generate different output expressions, the load seen by each gate varies. This load is complex and consists of resistive and capacitive components which can significantly affect propagation delays. An analogous situation exists in a discrete TTL design where propagation delays increase as more gates are driven from a particular logical node. For example, in Figures 1 and 2, PRODUCT term 2 (PT2) drives both SUM terms 1 and 2 (ST1 and ST2), whereas PRODUCT term 1 (PT1) only drives ST1. Therefore, it is reasonable to assume that an input condition causing PT1 to become active would propagate to ST1 more quickly than an input condition causing PT2 to become active. It is this effect which forms the basis for the delay minimization examples in the following sections.

OPTIMIZATION IS POSSIBLE

Four basic rules can be deduced which if followed will allow minimization of propagation delays. These four rules are concerned mainly with the programmable OR array of the HPL-77153. Speed optimization by manipulating the programmable AND array is not discussed in this application note because the highly interactive nature of this array makes optimization very complex. Also, improvements that can be made in the AND array are not significant compared to those that can be made in the OR array.

The following sections explain in detail the four basic rules for minimization, and give practical examples using Boolean expressions.

RULE 1

ANY PRODUCT TERM SHOULD NOT BE ALLOWED TO DRIVE NON-FUNCTIONING OUTPUTS (BI-DIRECTIONALS USED AS INPUTS).

When an HPL-77153 is unprogrammed, all PRODUCT terms are connected to all outputs. Fuses may be programmed to selectively disconnect PRODUCT terms from outputs; however, any outputs which are not active, such as bi-directional pins used as inputs, may or may not be connected to PRODUCT terms. Figure 3 shows a simple set of Boolean expressions with 5 outputs and 5 inputs. Notice that the 3 PRODUCT TERMS drive all 5 bi-directional pins used as inputs.

```
B0 (INPUT)    = PT0  + PT1  + PT31
B1 (OUTPUT)   =        PT1  + PT31
B2 (OUTPUT)   = PT0  + PT1
B3 (INPUT)    = PT0  + PT1  + PT31
B4 (OUTPUT)   = PT0  + PT1  + PT31
B5 (INPUT)    = PT0  + PT1  + PT31
B6 (OUTPUT)   = PT0  +         PT31
B7 (INPUT)    = PT0  + PT1  + PT31
B8 (INPUT)    = PT0  + PT1  + PT31
B9 (OUTPUT)   = PT0
```

FIGURE 3.

As it is of no logical consequence whether a non-functional output (input) is driven by PRODUCT terms or not, it may safely be disconnected from all PRODUCT terms to minimize propagation delays. Figure 4 shows how PT0, PT1, and PT31 may be disconnected from those outputs not requiring their contribution.

```
B0 (INPUT)    =
B1 (OUTPUT)   =         PT1  + PT31
B2 (OUTPUT)   = PT0  + PT1
B3 (INPUT)    =
B4 (OUTPUT)   = PT0  + PT1  + PT31
B5 (INPUT)    =
B6 (OUTPUT)   = PT0  +         PT31
B7 (INPUT)    =
B8 (INPUT)    =
B9 (OUTPUT)   = PT0
```

FIGURE 4.

This rule should be observed at all times since it does not call for any extra circuitry to be committed, which is not the case with all the speed optimization rules.

RULE 2

ANY UNUSED PRODUCT TERMS SHOULD BE DISCONNECTED FROM ALL THE SUM TERMS.

Unused PRODUCT terms normally contribute a logical "0" to the SUM array, and are normally left connected so they can be used for new PRODUCT terms, or to replace undesired PRODUCT terms at a later date Figure 5 shows a set of Boolean expressions where PT2 and PT3 are unused. All PRODUCT terms have been disconnected from the bi-directional pins used as inputs, according to RULE 1.

```
B0 (INPUT)    =
B1 (OUTPUT)   =          PT1  + PT2  + PT3  + PT31
B2 (OUTPUT)   = PT0   + PT1  + PT2  + PT3  +
B3 (INPUT)    =
B4 (OUTPUT)   = PT0   + PT1  + PT2  + PT3  + PT31
B5 (INPUT)    =
B6 (OUTPUT)   = PT0   +        PT2  + PT3  + PT31
B7 (INPUT)    =
B8 (INPUT)    =
B9 (OUTPUT)   = PT0            PT2  + PT3
```

FIGURE 5.

The unused PRODUCT terms, PT2 and PT3, will load the SUM terms of those pins used as outputs and should be disconnected. This results in a new set of expressions as shown in Figure 6.

```
B0 (INPUT)    =
B1 (OUTPUT)   =          PT1  +          PT31
B2 (OUTPUT)   = PT0   + PT1
B3 (INPUT)    =
B4 (OUTPUT)   = PT0   + PT1  +          PT31
B5 (INPUT)    =
B6 (OUTPUT)   = PT0   +                 PT31
B7 (INPUT)    =
B8 (INPUT)    =
B9 (OUTPUT)   = PT0
```

FIGURE 6.

The user should note that while disconnecting PRODUCT TERMS will enhance speed, some of the flexibility for performing "LOGICAL SURGERY" (replacing incorrectly programmed PRODUCT TERMS by new ones) will be lost.

RULE 3

ANY PRODUCT TERMS DRIVING A PARTICULAR OUTPUT SHOULD NOT BE USED TO DRIVE ANY OTHER OUTPUTS (NO PRODUCT TERM SHARING).

If a PRODUCT term is used to drive more than one output (2-10 for the HPL-77153), it must drive the large capacitive loads associated with the SUM term interconnect metallization. Each extra SUM term driven adds more load capacitance and results in longer propagation delays. Consider the expressions shown in Figure 7. Three product terms are generated from six input variables; two outputs are constructed from combinations of the three product terms.

```
PT0   = A.B
PT1   = C.D
PT2   = E.F

B0 (OUTPUT) = PT0  + PT1
B1 (OUTPUT) = PT1  + PT2
```

FIGURE 7.

Notice that PT1 is shared between B0 and B1. This is good practice for minimizing the number of PRODUCT terms used, but will not minimize the propagation delay. A better solution would be to use an extra PRODUCT term. so that each PRODUCT term only drives one output as shown in Figure 8.

```
PT0   = A.B
PT1   = C.D
PT2   = C.D
PT3   = E.F

B0 (OUTPUT) = PT0  + PT1
B1 (OUTPUT) = PT2  + PT3
```

FIGURE 8.

An easy way to identify shared PRODUCT terms is to examine the SUM term expressions and search for any PRODUCT terms that appear in more than one SUM term. Such shared PRODUCT terms should be replaced by duplicated PRODUCT terms as shown above. This procedure may be repeated until no shared PRODUCT terms are left, or until all spare PRODUCT terms are used up.

RULE 4

IF SPARE PRODUCT TERMS ARE AVAILABLE, USE THEM TO DUPLICATE FUNCTIONING PRODUCT TERMS IN CRITICAL PATHS.

Every PRODUCT term driving an output has to contend with the capacitance of the associated SUM term. If spare PRODUCT terms are available, they can be used to drive the SUM terms in parallel, effectively multiplying the available drive to the SUM terms by the number of duplicated PRODUCT terms.

```
PT0   = A.B

B0 (OUTPUT) = PT0
```

FIGURE 9.

Figure 9 shows an example of an output being driven by one PRODUCT term, and Figure 10 shows the same output being driven by four PRODUCT terms. Both Figures 9 and 10 exhibit the same logical functionality, but the implementation of Figure 10 will usually have a lower propagation delay.

```
PT0   = A.B
PT1   = A.B
PT2   = A.B
PT3   = A.B

B0 (OUTPUT) = PT0  + PT1  + PT2  + PT3
```

FIGURE 10.

This procedure may be extended to include more PRODUCT terms, but importantly, the user should be aware that as more PRODUCT terms are duplicated, the loading imposed on the input buffers will cause delays in the AND array which will increasingly negate any speed improvement in the OR array. The extra loading on the input buffers may also be reflected in extra delays for outputs not associated with the output being optimized. For any given logical function there will be an optimum value for the number of duplicated PRODUCT terms. It is left to the user to determine empirically the optimum number of PRODUCT terms duplicated.

CONCLUSION

As mentioned earlier, Harris Semiconductor does not guarantee that any specific speed improvement will be brought about by employing any of the techniques shown in this application paper. However, characterization data generated from best case and worse case patterned parts suggests that an improvement of several nano-seconds may be expected.

Generally, when minimizing device propagation delays, RULES 1, 2, 3, and 4 should be exercised in that order although specific user requirements may dictate otherwise.

The four rules shown in this application note are applicable to devices having two programmable arrays (AND and OR); however, RULE 4 is applicable to devices having only one programmable array (AND), such as PAL® type and proprietary devices manufactured by Harris Semiconductor.

Applications assistance is available from Harris Semiconductor with regard to speed optimization.

THE VOCAL TEST CIRCUITRY INCORPORATED IN THE HPL-77153 (AND ALL OTHER HPL PRODUCTS) IS USED AT THE TIME OF MANUFACTURE TO FORCE THE FPLA INTO A WORST CASE PATTERN CONFIGURATION FOR THE PURPOSE OF PERFORMING DYNAMIC (AC) TESTING. ONLY THE HARRIS FPLA IS GUARANTEED TO MEET THE DYNAMIC (AC) AND STATIC (DC) SPECIFICATIONS OVER TEMPERATURE AND WITH A WORST CASE PATTERN.

PAL is a registered trademark of MMI.

HARRIS

Bipolar Application Note 201

POWER STROBING LARGE MEMORY ARRAYS

by D.R. Burge

INTRODUCTION

As system designs become more complex, software flexibility often demands denser memory arrays. Consequently, memory IC vendors are designing and manufacturing denser memory chips. However, regardless of the density of the memory IC, one memory chip will seldom do the job.

In extremely memory-intensive systems, power consumption can be a critical design factor. Every accomplished designer realizes, however, that reducing power often leads to slower access times. The challenge is to reduce power without significantly affecting access time.

Bipolar PROMs are high-speed, non volatile memories whose matrix contents are not adversely affected by the proper removal of power. In certain applications where access to the memory matrix is required for only a small percentage of time, overall power consumption can be significantly reduced by power strobing.

OPTIONS

There are, in general terms, three distinct methods of power strobing that are available to designers today. Each method is best suited for only a subset of all applications. The methods are:

1) Using ICs with the power strobe function integrated on-chip
2) External power strobing with discrete components
3) External power strobing with an IC designed specifically for that purpose

The use of Bipolar PROMs with the power strobe function integrated on-chip can be very enticing. These devices are best suited for applications in which only a few PROMs are needed, as there are few vendors supplying these parts, and they can be very expensive. In addition, use of these parts will typically permit power reduction of only approximately 65% to 75%.

Power strobing PROMs with discrete components is another option which is best suited for small volume applications. Using this method can be very space- and time-consuming due to the number of components required. A commonly used discrete power strobing circuit consists of a high-speed, low $V_{CE(sat)}$, PNP transistor with the appropriate bias circuitry as shown in Figure 1. More elaborate discrete power strobing circuits have been used, often at the expense of slower turn-on and turn-off times.

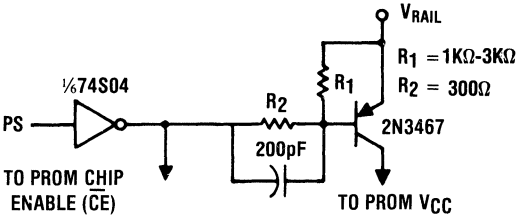


FIGURE 1. Discrete Power Strobe Circuit

For large memory arrays, it is often most desirable to choose an integrated circuit specifically designed to reduce overall power consumption. Harris Semiconductor manufactures a device designed to meet that need—the HD-6600 Quad Power Strobe. Each 14-pin dual in-line package contains four identical monolithic power strobes. The circuit diagram for each strobe is shown in Figure 2.

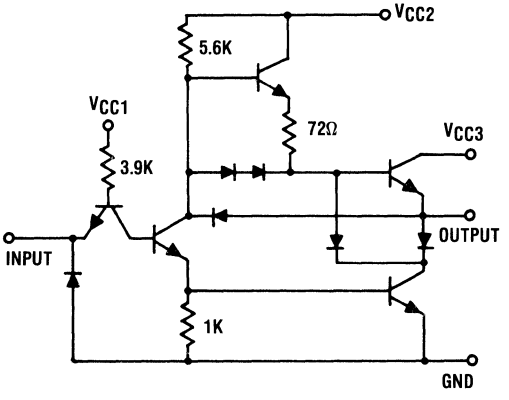


FIGURE 2. Circuit Diagram for HD-6600 (One of Four Identical Strobes)

Typical turn-on and turn-off delay for the HD-6600 is 50 ns. Power requirements for the device are as follows:

I_{CC1} = 6mA Max
I_{CC2} = 70mA Max (all strobes enabled, I_L = −150mA)
I_{CC2} = 15mA Max (all strobes disabled, I_L = 0)

Please consult the HD-6600 Data Sheet for more detailed specifications.

Using nominal power supplies of V_{CC1} = +5V, V_{CC2} = +12V, and V_{CC3} = +5V, and simplifying the power calculations by approximating that:

$$P_D = V_{CC1} I_{CC1} + V_{CC2} I_{CC2} + V_{CE(sat)} I_{CC3},$$

then,

P_D = (5V)(6mA) + (12V)(15mA) = 30mW + 180mW
= 210mW

for an HD-6600 with no strobes enabled. In this example, in which four PROMs with power supply currents of 150mA each are utilized, the power is reduced from 3 Watts (all four PROMs powered up) to 210mW, a staggering 93%. The absolute power reduction will be even more extreme with larger memory arrays as shown in the example below.

APPLICATION

In this example, four HD-6600s are utilized to strobe power for a 16K x 16 memory array which consists of sixteen 4K x 4 PROMs (See Figure 3). This application stresses the fact that access is required to only ¼ of the array at any specific instant in time; therefore, the other ¾ of the array may be powered-down.

The 74S139 One-of-Four-Decoder is required in this application to select the portion of the array to which access is required. Adding the four HD-6600 Quad Power Strobes in this design provides for significant power reduction, as shown below.

POWER REQUIREMENTS FOR 16K x 16 ARRAY WITH NO POWER STROBES

P_D = (90mA)(5V) + (170mA)(5V)(16)
= 0.45W + 13.6W
= 14.05 Watts

POWER REQUIREMENTS FOR 16K x 16 ARRAY WITH POWER STROBES

¼ of Array Enabled

P_D = (90mA)(5V) + (170mA)(5V)(4) + (6mA)(5V)(4)
+ (¼)(70mA)(12V)(4) + (¾)(15mA)(12V)(4)
= 0.45W + 3.4W + 0.12W + 0.84W + 0.54W
= 5.35 Watts

All of Array Disabled (A_{14} High)

P_D = (90mA)(5V) + (6mA)(5V)(4) + (15mA)(12V)(4)
= 0.45W + 0.12W + 0.72W
= 1.29 Watts

Note that in using A_{14} to disable the entire array, power has been reduced to approximately 9% of what would be required if the HD-6600s had not been used in the design. Remember that it is absolutely essential to properly decouple the power supplies. Decoupling capacitors should be placed as close as possible to the power strobe.

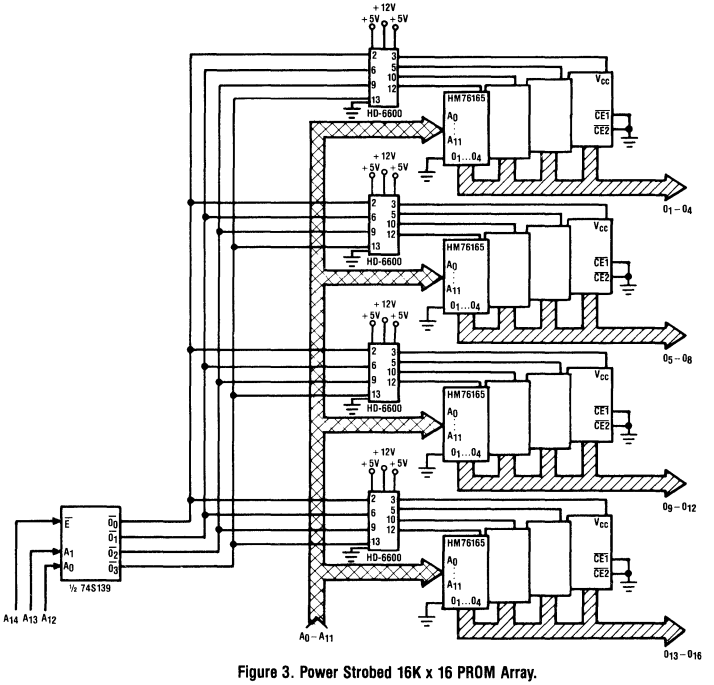


Figure 3. Power Strobed 16K x 16 PROM Array.

CONCLUSION

The purpose of this paper is to simply suggest possible methods for reducing the power requirements of Bipolar PROMs. The information contained herein is intended solely for general guidance. Recognizing that there is no single optimum solution for all applications, a method has been presented utilizing the HD-6600 Quad Power Strobe manufactured by Harris Semiconductor Bipolar Digital Products Division. It is hoped that this paper will inspire creative new ideas in the design of large memory arrays.

BIPOLAR

Hi-Rel

7

Introduction

Harris Semiconductor Bipolar Products Division offers three standard levels of military device screening to coincide with the three industry levels of quality assurance for military products. This provides the most cost-effective product in relation to its overall quality and reliability.

The three standard levels of processing include: Harris Standard Class B, JM38510 Class B, and Harris Standard Class S. The Harris Standard Class B flow also includes the DESC part drawings for the 32K and 64K PROMs.

However, Harris Bipolar offers total flexibility in test condition/stress level selection, within the three standard processing levels. This allows Harris to meet individual screening requirements, where standard processing and standard electricals are not permissible by individual contract requirements.

The Division also offers a broad line of packaging for each device:

(a) Ceramic Dual In-line Package
(b) Bottom Braze Metal Flatpack
(c) Ceramic Flatpack
(d) Leadless Chip Carrier

With this packaging variety, Harris can supply to the full spectrum of program requirements.

Harris Bipolar Military Cross-Reference Chart

ORGANIZATION	HARRIS	SIGNETICS	MMI	AMD	FAIRCHILD	NATIONAL	TI
64 X 8	HPROM 0512-8 JM38510/20101						
32 X 8 (OC)	HM-7602-8 JM38510/20701	82S23 JM38510/20701	5330	27S18		54S188	TBP18SA030J
32 X 8 (TS)	HM-7603-8 JM38510/20702	82S123 JM38510/20702	5331	27S19		54S288	TBP18S030J
256 X 4 (OC)	HM-7610-8 JM38510/20301	82S126 JM38510/20301	5300	27S20	93417	54S387	TBP24SA10J
256 X 4 (TS)	HM-7611-8 JM38510/20302	82S129 JM38510/20302	5301 JM38510/ 20302	27S21	93427	54S287	TBP24S10J
512 X 4 (OC)	HM-7620-8 JM38510/20401	82S130 JM38510/20401	5305	27S12	93436	54S570	
512 X 4 (TS)	HM-7621-8 JM38510/20402	82S131 JM38510/20402	5306	27S13	93446	54S571	
512 X 8 (OC)	HM-7640-8 JM38510/20801		5340	27S30	93439	54S475	TBP28SA46J
512 X 8 (TS)	HM-7641-8 JM38510/20802	82S141 JM38510/20802	5341	27S31	93448	54S474	TBP28S46J
1024 X 4 (OC)	HM-7642-8 JM38510/20601		5352	27S32	93452	54S572	TBP24A41J
1024 X 4 (TS)	HM-7643-8 JM38510/20602	82S137 JM38510/20602	5353	27S33	93453	54S573	TBP24S41J
512 X 8 (TS)	HM-7649-8	82HS147	5349	27S29		54S472	TBP28S42J
1024 X 8 (TS)	HM-7681-8 JM38510/20904	82S181 JM38510/20904	5381	27S181 JM38510/ 20904	93451	77S181	TBP28S86J
2048 X 4 (TS)	HM-7685-8 JM38510/20902	82S185 JM38510/20902	5389	27S185		77S185	TBP24S81J
2048 X 8 (TS)	HM-76161-8 JM38510/21002	82S191 JM38510/21002		27S191	93511 JM38510/ 21002	77S191	TBP28S166J
4096 X 4 (TS)	HM-76165-8	82S195	27S41			77S195	
4096 X 8 (TS)	HM-76321-8	82S321	27S43			77S321	
8192 X 8 (TS)	HM-76641-8	82S641			93Z565		
FPLA	HPL77153	82S153					
PAL	HPL77209		PAL16L8	AMPAL16L8			
PAL	HPL77215		PAL16H8	AMPAL16H8			
PAL	HPL77216		PAL16P8				

JAN PROMs

HARRIS MIL-GRADE BIPOLAR PROMS

SLASH NUMBER	PART NUMBER	NUMBER OF BITS	ORGANI-ZATION	DESCRIPTION	NUMBER OF PINS
20101BJB	JAN-0512	512	64 x 8	Open-Collector Output	24
20701BEB	HM-7602	256	32 x 8	Open-Collector Output	16
20702BEB	HM-7603	256	32 x 8	Three-State Output	16
20301BEB	HM-7610	1024	256 x 4	Open-Collector Output	16
20302BEB	HM-7611	1024	256 x 4	Three-State Output	16
20401BEB	HM-7620	2048	512 x 4	Open-Collector Output	16
20402BEB	HM-7621	2048	512 x 4	Three-State Output	16
20801BJB	HM-7640	4096	512 x 8	Open-Collector Output	24
20802BJB	HM-7641	4096	512 x 8	Three-State Output	24
20601BVB	HM-7642	4096	1K x 4	Open-Collector Output	18
20602BVB	HM-7643	4096	1K x 4	Three-State Output	18
20904BJB	HM-7681	8192	1K x 8	Three-State Output	24
20902BVB	HM-7685	8192	2K x 4	Three-State Output	18
21002BJB	HM-76161	16384	2K x 8	Three-State Output	24
21102BJB	HM-76321 *	32768	4K x 8	Three-State Output	24
21202BJB	HM-76641 *	65536	8K x 8	Three-State Output	24

* Qualification to be scheduled upon release of finalized issue of applicable 38510 Slash Sheet.

Harris Bipolar Flows and Screening Procedures

Screen	Commercial		Harris Standard Class B		JAN Class B		Harris Standard Class S	
	Plastic	DIP	Method	Requirement	Method	Requirement	Method	Requirement
Wafer Acceptance	Harris Standard	Harris Standard	Harris Standard	Harris Standard	Per JM 38510	Per JM 38510	Mod. 5007	
Internal Visual (Precap)	Harris Standard	Harris Standard	2010 Cond. B	100%	2010 Cond. B and 38510	100%	1008 24 Hrs. (min) Cond. A	100%
Stabilization Bake		As Required	1008 24 Hrs. (min) Cond. C	100%	1008 24 Hrs. (min) Cond. C	100%	1008 24 Hrs. (min) Cond. C	100%
Temperature Cycling		1010 Cond. C 10 Cycles	1010 Cond. C 10 Cycles	100%	1010 Cond. C (min) in Y_1 Plane	100%	1010 Cond. C	100%
Constant Acceleration		2001 Cond. E (min) in Y_1 Plane	2001 Cond. E (min) in Y_1 Plane	100%	2001 Cond. E (min) in Y_1 Plane	100%	2001 Cond. E (min) in Y_1 Axis	100%
Pind Testing							2020	100%
Seal Fine and Gross		Harris Standard	1014	100%	1014	100%	1014	100%
Interim Electrical	Harris Standard Published Electricals	Harris Standard Published Electricals	Harris Standard Published Electricals	100%	JAN Slash Sheet Elec. Specifications	As Applicable	Harris Standard Electrical Specifications Serialization R & R Variable Data Note 1	100%
Burn-In Test		As Required	1015 125°C (min) PDA = 5%	100%	1015 125°C (min) PDA = 5%	100%	1015 125°C (min 240 Hrs) PDA = 5%	100%

Harris Bipolar Flows and Screening Procedures (Continued)

Screen	Commercial		Harris Standard Class B		JAN Class B		Harris Standard Class S	
	Plastic	DIP	Method	Requirement	Method	Requirement	Method	Requirement
Final Electrical Tests Static Tests (1) 25°C (Subgroup 1, Table 1, 5005) (2) Max and Min Rated Operating Temperature Dynamic Tests and Switching Tests 25°C (Subgroup 9 Table 1, 5005)	Harris Standard	Harris Standard	Harris Standard Published Electricals	100%	JAN Slash Sheet Electrical Specifications	100%	Harris Standard Electrical Specifications Read and Record 25°C	100%
Functional Tests 25°C (Subgroup 7, Table 1, 5005) Quality Conformance Inspection: Group A Static (1) 25°C (Subgroup 1) (2) Temperature (Subgroup 2 and 3) Switching (1) 25°C (Subgroup 1) (2) Temperature (Subgroup 10 and 11) Functional (1) 25°C (Subgroup 7)	Harris Standard	Harris Standard	5005 Class B	LTPD Per 5005 Class B		LTPD Per MIL-STD-883	25°C,-55°C 125°C 5005 Class S	LTPD 3% 5% 5% 3%
Radio Graphic							2012	100%
Group B			5005 Class B	6 weeks	5005 Class B	Inspection Lot	5005 Class S	Inspection Lot
Group C			5005 Class B	13 Weeks	5005 Class B	13 Weeks Production		
Group D			5005 Class B	6 Months	5005 Class B	6 Months Pkg. Production	5005 Class S	Generic or Inspection Lot
External Visual	Harris Standard	Harris Standard	2009	100%	2009	100%	2009	100%

Military Products Packaging

PROMS

Part Number	PACKAGE AVAILABLE					QPL Status (DIP Only)
	Plastic DIP (Commercial Only)	Ceramic DIP	Flat Pack	LCC	Slim Line DIP	
HM-7602 (1/4K)	●	●				QPL1
HM-7603 (1/4K)	●	●				QPL1
HM-7610 (1K)	●	●	●			QPL1
HM-7611 (1K)	●	●	●			QPL1
HM-7620 (2K)	●	●	●			QPL1
HM-7621 (2K)	●	●	●			QPL1
HM-7640 (4K)	●	●	●		●	QPL1
HM-7641 (4K)	●	●	●		●	QPL1
HM-7642 (4K)	●	●	●			QPL1
HM-7643 (4K)	●	●	●			QPL1
HM-7649 (4K)	●	●	●			Planned
HM-7681 (8K)	●	●	●	●	●	QPL1
HM-7685 (8K)	●	●				QPL1
HM-76161 (16K)	●	●	●	●	●	QPL1
HM-76165 (16K)		●				Planned
HM-76321 (32K)		●		●		Planned
HM-76641 (64K)		●		●		Planned
JAN 0512 (1/2K)		●	●			QPL1

PROGRAMMABLE LOGIC

HPL-77153	●	●		●		Planned
HPL-77209	●	●		●		Planned
HPL-77215	●	●		●		Planned
HPL-77216	●	●		●		Planned
HPL-77317	●	●		●		Planned
HPL-77318	●	●		●		Planned
HPL-77319	●	●		●		Planned
HPL-77320	●	●		●		Planned

DIODE MATRICES

HM-0104	●	●	●			
HM-0168	●	●	●			
HM-0186	●	●	●			
HM-0198	●	●	●			
HM-0410	●	●	●			

NOTE: This table is intended to provide a general guide to the packaging options available for Harris Bipolar products. Please note that other packaging options may be available. Contact your local Harris sales office regarding your requirements.

Mechanical Information

LEAD FINISHES

A – Kovar or Alloy 42, with hot solder dip
B – Kovar or Alloy 42, with matte tin plate
C – Kovar or Alloy 42, with gold plate
X – Any of above, for ordering purposes only

Note: Matte tin is reflowed for JM 38510 products.

CASE OUTLINES

Letter	Appendix C Designation	Description
A	F-1	14-lead FP (1/4" X 1/4")
B	F-3	14-lead FP (3/16" X 1/4")
C	D-1	14-lead DIP (1/4" X 3/4")
D	F-2	14-lead FP (1/4" X 3/8")
E	D-2	16-lead DIP (1/4" X 7/8")
F	F-5	16 lead FP (1/4" X 1-1/4")
G	A-1	8-lead can
H	F-4	10-lead FP (1/4" X 1/4")
I	A-2	10-lead can
J	D-3	24-lead DIP (1/4" X 1-1/4")
K	F-6	24-lead FP (3/8" X 5/8")
L	NONE	NONE
M	A-3	12-lead can
N	NONE	NONE
P	D-4	8-lead DIP (1/4" X 3/8")
Q	D-5	40-lead DIP (9/16" X 2-1/16")
R	D-8	20-lead DIP (1/4" X 1-1/16")
S	NONE	NONE
T	NONE	NONE
U	NONE	NONE
V	D-6	18-lead DIP (.300" X 1")
W	D-7	22-lead DIP (.400" X 1.1")
X	Dual in-line packages not listed above	
Y	Flat packages not listed above	
Z	All other configurations not listed above	

LCC OUTLINES

LCC	Available	Dimensions (in.)
C-2	20-Terminal	.350 x .350
C-4	28 -Terminal	.450 X .450
C-5	44-Terminal	.650 X .650
C-11	28-Terminal	.350 X .350
C-12	32-Terminal	.450 X .450

SLIM LINE DIP

Available	Dimensions (in)
24-Lead	1.250 X .288

NOTE: The information contained on this page has been reprinted from MIL-M-38510 and is provided for reference only. It is not intended to be a representation of the packaging capabilities of Harris Semiconductor Bipolar Digital Products Division.

Standard Harris Programs

Harris offers four standard levels of device screening (including the Harris commercial flow) to coincide with the four industry levels of quality assurance—providing you with the most cost-effective product in relation to its overall quality and reliability.

Total flexibility in test condition/stress level selection assures you of screening tailored to your individual requirements.

Please note: specification of high screening levels may result in unnecessary costs, while limited screening could endanger product reliability requirements. Harris can help you determine the correct screening level for your particular application.

For general hi-rel applications, Class B levels should be considered.

Contact Harris for additional information for specialized requirements.

How to Order

MIL-M-38510 JAN-QUALIFIED PRODUCTS

J	M38510	/001	04	B	C	B
Indicates a Qualified Device	Military Designator	Detail Specification Number	Device Type Within Detail Specification	Class B (Refer to MIL-M-38510 for explanation)	Case Outline	Lead Finish

STANDARD PRODUCTS

H	M	1	—	7620	—	8
PREFIX: H (Harris)	FAMILY: D – Digital; M – Memory; PL – Programmable Logic	PACKAGE: 1 – Ceramic DIP; 3 – Epoxy DIP; 4 – Leadless Carriers; 6 – Slim Line DIP; 7 – Mini DIP; 9 – Flat Pack (Consult Factory); 0 – Chip Form		PART NUMBER *		TEMPERATURE: 2 – -55°C to +125°C; 5 – 0°C to +75°C; 6 – 100% 25°C Probe (Dice Only); 8 – Dash 8 Program

* Alpha suffix defined in individual data sheets.

Custom Integrated Circuits Division

8

The Custom Integrated Circuits Division

Custom Integrated Circuits Division is an independent division, fully facilitated and staffed, dedicated to the development and production of Custom/Semi-Custom and specialized integrated circuits. CICD employs high performance CMOS and Bipolar technologies to meet the needs of the marketplace.

During the 1970's, technologies and innovative processes developed in custom circuit work were transferred into diverse standard products for broad-based commercial applications. This successful technology transfer helped make Harris Semiconductor one of the nation's leading IC suppliers.

Custom and Semi-Custom circuit fabrication has continued to thrive in the independent, full-function Custom Integrated Circuits Division (CICD), one of the five major business units within the Harris Semiconductor Sector — Analog Products, Bipolar Digital Products, CMOS Digital Products, Microwave and CICD. Major markets include the military, information systems, communications, industrial and medical equipment areas.

The Custom Integrated Circuits Division has achieved greater than a 20 percent compounded growth rate and has continued strong growth projections through the 1980's.

Organization and Resources

Compared to standard product lines marketed to multiple customers by the other divisions, CICD products are customized in Melbourne to serve unique user requirements. In addition to performing special functions in critical environments, custom chips can perform multiple functions at higher speed with lower power requirements, providing the means to reduce equipment size and cost while increasing performance. As a major supplier to such critical systems as Trident, Peacekeeper, B-1B, and Heart Pacemaker Programs, performance and reliability are of paramount concern.

Because no two customer orders are alike, CICD is oriented to engineering and manufacturing specific customer capabilities. A high level of quality assurance is imperative and technological advantages are emphasized in all customer involvements. The division is also one of the few custom product makers in the IC industry with its own dedicated manufacturing operation and engineering, product assurance, sales and marketing organizations.

The division's marketing program emphasizes the capability to meet specific customer requirements with state of the art products that compare with the best in the IC industry.

Future growth in broader commercial and industrial application areas is assured by expanding engineering and manufacturing facilities and by new capabilities in Semi-Custom Circuitry.

Bipolar Digital Design Techniques

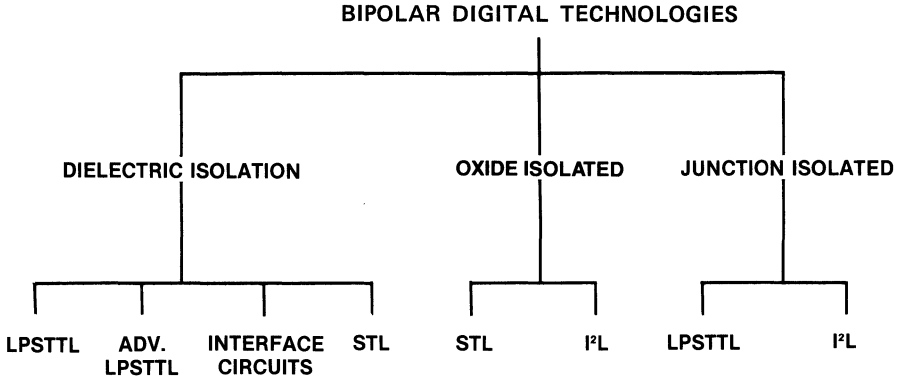
Harris CICD Bipolar Digital Design capabilities cover a wide range of custom/semi custom applications. Many fabrication processes are available to best fit the application. These processes can best be classified by the type of isolation process used.

Dielectric Isolation gives total device sidewall and substrate oxide isolation. This isolation process is used for strategic radiation hardened applications such as Trident and Peacekeeper. This isolation process also allows fabrication of many types of devices on one chip. High breakdown NPN and PNP devices are often combined with lower resistivity, high switching speed digital NPN devices in interface applications where linear and digital functions are to be combined on one chip.

Oxide Isolated processes utilize passive oxide sidewall isolation with junction substrate isolation. These processes are used in high performance/high packing density commercial/ industrial applications.

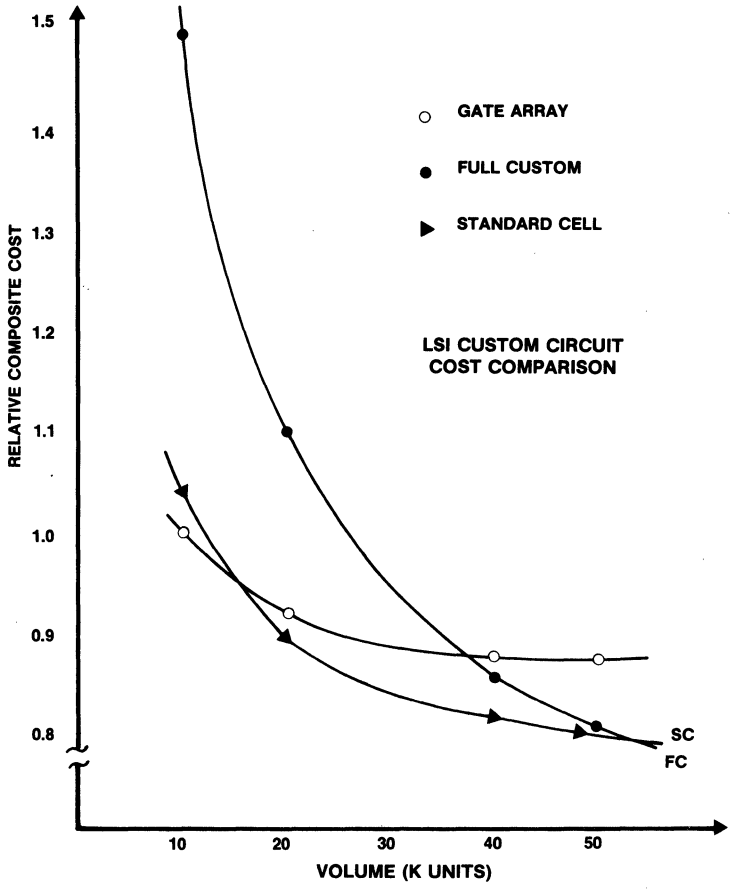
Junction Isolation, in which both the sidewall and substrate is junction isolated is used for medium performance, low cost applications.

In the following pages an overview of the major technologies, their electrical characteristics and design examples will be presented.



LPSTTL = LOW POWER SCHOTTKY T^2L
STL = SCHOTTKY TRANSISTOR LOGIC
I^2L = INTEGRATED INJECTION LOGIC

LSI Custom Circuit Cost Comparison



Bipolar LSI/VLSI Design Options

DESIGN TECHNIQUE	DESCRIPTION	ADVANTAGES/ DISADVANTAGES
FULL CUSTOM	Every device is custom designed in the layout for a specific application.	• Lowest Production Cost • Smallest Chip Size • High Development Cost • Requires Long Design Cycle
GATE ARRAY	Two or three masking levels are designed to create a new custom circuit	• Fast Design Cycle • Low Risk, Low Design Cost • High Production Cost • Not all circuits may fit on a given Array.
MARCO CELL DESIGN	A marco cell family is created as a full custom design. All circuits in the program are designed from this macro family.	• Good compromise between – Schedule – Cost – Performance – Risk

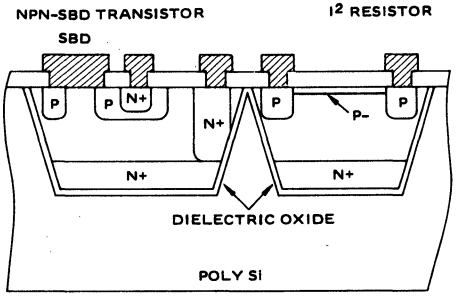
Bipolar Digital Technologies

Most RAD-Hard designs are implemented in the advanced LPSTTL technology for 5 V only operation or DI STL when 5 V and 1.8 V are available.

Most High-Speed Nonhardened designs are implemented in the Oxide-Isolated STL technology.

Harris can also process wafers using a customer's mask set and process parameters.

DI-Low Power Schottky



LOW POWER SCHOTTKY CROSS-SECTION

PROCESS DESCRIPTION

- DIELECTRIC ISOLATION
- NINE MASKING STEPS
- ION IMPLANTED RESISTORS
- Pt-Si SBD'S
- Ti-W PLUS ALUMINUM INTERCONNECTIONS

COMPATIBILITY

- PACKING DENSITY = 25 GATES/mm²
- MAX COMPLEXITY = 400 GATES/CHIP
- TYPICAL SPEED = 6nS/GATE
- TYPICAL POWER = 10mW/GATE
- POWER SUPPLY VOLTAGE = 5V
- OUTPUT DRIVE = 4mA

DEVICE PARAMETERS

- NPN BETA≅100
- I² RESISTOR SHEET = 1000Ω/□
- BREAKDOWN VOLTAGE = 10V
- HARDENED TO STRATEGIC RADIATION LEVELS

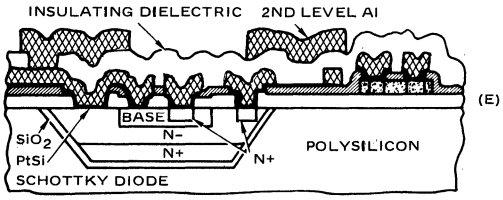
PRODUCT TYPES

PRESENTLY USED FOR PEACEKEEPER

- GATES
- MSI FUNCTIONS
- MEMORIES

12 PART TYPES IN PRODUCTION

DI-Advanced LPSTTL (ALPS)



PROCESS DESCRIPTION

- DIELECTRIC ISOLATION
- ELEVEN MASKING STEPS
- POLYSILICON THIN FILM RESISTORS
- Pt-Si SBD'S
- TWO LAYERS OF INTERCONNECT

COMPATIBILITY

- PACKING DENSITY = 50 GATE/mm^2
- RAM CELL AREA = 10 SQ MILS
- MAX COMPLEXITY = 1000 GATES/CHIP
- TYPICAL SPEED = 5 ns/GATE
- TYPICAL POWER = 1 mW/GATE
- POWER SUPPLY VOLTAGE = 5 VOLTS
- OUTPUT DRIVE = 8 mA

DEVICE PARAMETERS

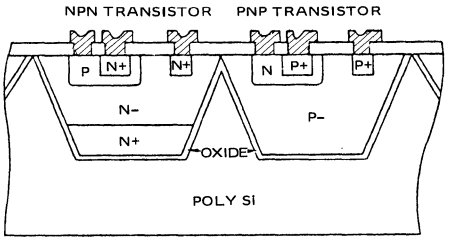
- NPN BETA ≅ 100
- POLY RESISTOR SHEET = 1000Ω/□
- BREAKDOWN VOLTAGE = 8 V
- HARDENED TO STRATEGIC RADIATION LEVELS

PRODUCT TYPES—STRATEGIC HARDNESS

- 90 ns MAX 256 x 4 STATIC RAM
- 120 CGA WITH 14 I/O
- 312 CGA WITH 46 I/O
- 918 CGA WITH 76 I/O

NOTE: SEE RADIATION-HARDENED PRODUCTS OR THE GATE ARRAY SECTION FOR MORE INFORMATION ON THE ALPS ARRAYS

Interface Circuit Technology – DI



DI COMPLEMENTARY TECHNOLOGY CROSS-SECTION

PROCESS DESCRIPTION

- DIELECTRIC ISOLATION
- TEN TO TWELVE MASKING STEPS
- COMPLEMENTARY NPN AND PNP TRANSISTORS
- DEEP COLLECTOR CONTACTS CAN BE USED TO ALLOW HIGH DRIVE CURRENTS

CAPABILITY

THIS TECHNOLOGY IS AIMED TOWARD INPUT AND OUTPUT BUFFERS AND IS CAPABLE OF:

- HIGH OUTPUT DRIVE=100mA
- POWER SUPPLY VOLTAGES = ± 15V TO ± 30V
- EMP PROTECTION

DEVICE PARAMETERS

- NPN BETA≅200
- PNP BETA≅100
- BREAKDOWN VOLTAGES=30V – 60V
- HARDENED TO MAN RATED RADIATION LEVELS.

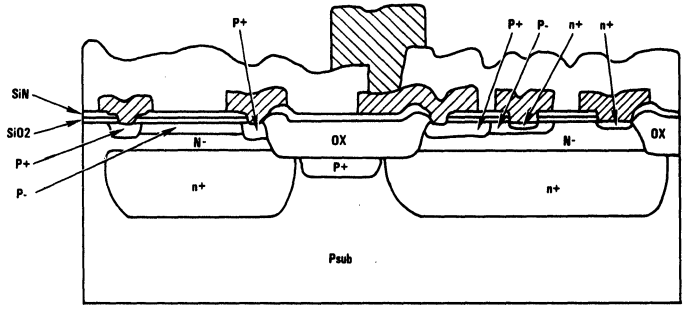
PRODUCT TYPES

- ARINC-429 DRIVER
- B-1 RECEIVERS/DRIVERS – 5 CIRCUITS

PACKAGES

- NO PACKAGE LIMITATIONS

Advanced Schottky Transistor Logic — ASTL



ASTL CROSS-SECTION

PROCESS DESCRIPTION	COMPATIBILITY
• OXIDE ISOLATION • THIRTEEN MASK STEPS • TWO LEVELS OF INTERCONNECT • THREE MICRON GROUNDRULES • TiW OUTPUT SBD's • PtSi CLAMP SBD's	• MAX SPEED = 0.75 ns • POWER AT MAX SPEED = 0.26 mW • MAX COMPLEXITY = 3000 GATES/CHIP • LOGIC POWER SUPPLY = 2.0 V • T^2L BUFFER POWER SUPPLY = 5 V
DEVICE PARAMETERS	**PRODUCT TYPES**
• NPN BETA $\cong$ 80 • ft $\geqslant$ 3 GHz • $BV_{CEO} \sim$ 8.0V • 125 AND 1000Ω/□ RESISTORS	• GATE ARRAYS • CUSTOM LOGIC CIRCUITS

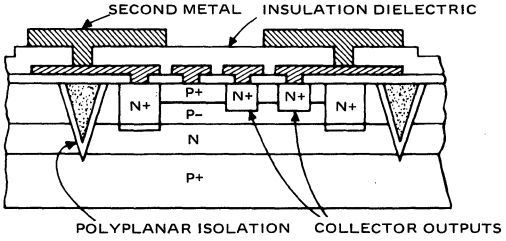
Oxide Isolated Schottky Transistor Logic (STL)

STL is a low power Bipolar technology capable of high speeds and amiable to gate Array, Macro Cell and full custom designs.

- Basic gate is single input-multiple output
- Requires a 2V V_{BB} power supply
- Designs have T^2L compatible input and three state output buffers using a 5V power supply
- Can operate over the full military temperature range
- Can use standard packages, DIP's, Flat Packs, LCC's
- 1500 Gate CGA now being characterized
- 2500 Gate CGA in design

Integrated Injection Logic (I^2L)

- I^2L is a Bipolar technology which uses merged NPN and PNP transistors to form the basic gate operating from 0.7 Volt.
- Designs have T^2L compatible input and open collector output buffers using a 5 Volts power supply.
- The primary application for this technology is in radiation-hardened military systems with low power requirements.
- Requires a separate constant current power supply.



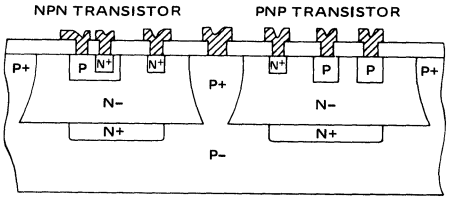
SUBSTRATE FED I^2L CROSS-SECTION

PROCESS DESCRIPTION	COMPATIBILITY
• POLYPLANAR ISOLATION • NINE MASKING STEPS • DOUBLE EPI SUBSTRATE FED PROCESS • TWO LEVELS OF INTERCONNECT • ISOLATED POLYPLANAR RESISTORS.	• PACKING DENSITY =100 GATES/mm² • MAX COMPLEXITY=4000 GATES/CHIP • MAX SPEED = 12nS/GATE • POWER AT MAX SPEED = .07mW/GATE • I^2L POWER SUPPLY = 0.7 VOLTS • T^2L INPUT AND OUTPUT BUFFER POWER SUPPLY = 5 VOLTS • OPEN COLLECTOR OUTPUT CURRENT = 4mA.
DEVICE PARAMETERS	**PRODUCT TYPE**
• NPN BETA≅100 • T^2L DEVICE BV=6 VOLTS • I^2L DEVICE BV=2 VOLTS • HARDENED TO STRATEGIC RADIATION LEVELS	• GATE ARRAYS 1680 CGA • CUSTOM RANDOM LOGIC CIRCUITS 8 X 8 MULTIPLIER

PACKAGES

- SUBSTRATE FED I^2L REQUIRES AN INJECTOR CONTACT THROUGH THE BOTTOM OF THE PACKAGE
  — GOLD DIE ATTACH REQUIRED

Junction Isolated Bipolar



JI BIPOLAR CROSS-SECTION

PROCESS DESCRIPTION

- JUNCTION ISOLATION
- SEVEN TO TEN MASKING STEPS
- PROCESS FLEXIBILITY CAN INCLUDE
  - — ALUMINUM SBD'S
  - — ION IMPLANTED RESISTORS
  - — MULTILEVEL INTERCONNECTS
  - — POLYPLANAR SIDEWALL ISOLATION

COMPATIBILITY

- PACKING DENSITY = 25 GATES/mm²
- MAX COMPLEXITY = 300 GATES/CHIP
- TYPICAL SPEED = 10nS/GATE
- TYPICAL POWER = 15mW/GATE
- POWER SUPPLY VOLTAGE = 5 TO 30 VOLTS
- OUTPUT DRIVE = 16mA

DEVICE PARAMETERS

- NPN BETA≅100
- PNP BETA≅15
- BREAKDOWN VOLTAGE = 8-30 VOLTS
- NOT NORMALLY RAD-HARD

PRODUCT TYPES

- MEMORIES
- SPECIAL MSI FUNCTIONS

PACKAGES

- NO PACKAGE LIMITATIONS

Advanced Low Power Schottky Gate Array Radiation-Hardened for Strategic Systems

Arrays Available Now

- 120 gate GCA with 14 I/O pins for MSI 14-16 pin applications
- 312 gate GCA with 46 I/O for multiple MSI replacement
- 918 gate CGA with 76 I/O for LSI application

Strategically Hardened Against

- Total gamma dose
- Logic upset due to total dose rate
- Prompt dose rate latchup/burnout
- Neutron radiation fluence

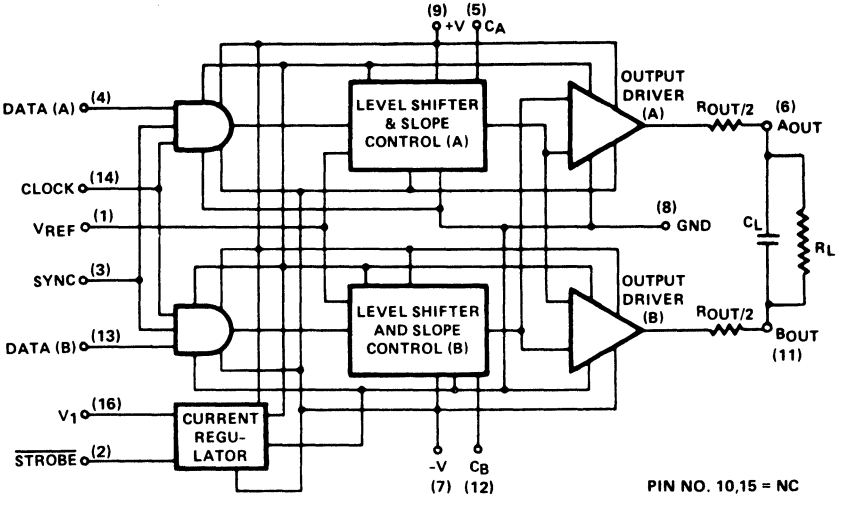
Array Features

- 5 Volts ± 10% only supply requirement
- -55° to 125°C operation
- No input buffers required, all array gates T^2L compatible
- Output buffer typically 10ns/15mW with 8mA Iol
- Internal gate typically 5ns/0.8mW
- Three custom layers; both metal levels and interlevel Via's
- Unused gates and buffers not powered

HS-3182 ARINC Driver Circuit Feature

- Bipolar differential line driver
- Inputs T^2L and CMOS compatible
- Adjustable rise and fall times controlled by 2 external capacitors
- Differential output voltage range programmed via the voltage reference input (V_{REF})
- Outputs are short circuit proof and over voltage protected
- Operates up to a 100K BPS data rate
- Full military temperature range

HS-3182 ARINC Driver Circuit Block Diagram



B-1B Circuits Part Description

PART NUMBER	PART NAME	CHANNELS PER PACKAGE	POWER SUPPLY VOLTAGES	PACKAGE TYPE	PART NUMBER
HS-3194	NIOB Non-Isolated Output Buffer	4	+12.6V +5.25V	14 Lead DIP	The NIOB converts a fast rise/fall input signal to a slow rise/fall output signal. IOL = 10mA. inputs are TTL.
HS-3195	SCIB Switch Closure Input Buffer	4	±30V +5.25V	18 Lead DIP	The SCIB provides a differential constant current at the input to detect an open or closed switch. Outputs are TTL.
HS-3196	DIB Discrete Input Buffer	4	±30V +5.25V	18 Lead DIP	The DIB accepts differential input voltages with ΔVin<2V⇒"0" at output and ΔVin>2.5V⇒"1" at output. Outputs are TTL.
HS-3197	SDOB Serial Digital Output Buffer	2	±15.6V	14 Lead DIP	The SDOB accepts an Open Collector TTL input and produces a differential ±5V output centered around ground. The output provides 5V across 35Ω.
HS-3198	SDIB Serial Digital Input Buffer	2	±20V +5.25V	16 Lead DIP	The SDIB produces differential logic "1" and "0" outputs from a differential input. Input voltages must be >2.25V apart or both outputs are "0".

NOTE: The outputs of all Output Buffers and inputs to all Input Buffers are protected against EMP.

Peacekeeper Digital Integrated Circuits (All IC's use DI, I^2 Resistors, P_T-S_i SBD's, and T_i-W-A_l Interconnect)

All Parts are Presently in Production

PART DESCRIPTION	PEACEKEEPER NUMBER 477-	NEAREST COMMERCIAL EQUIVALENT	HARRIS PART NUMBER
Quad 2 NAND	1269	SN54LS00	3114
Dual 4 NAND	1270	SN54LS20	3112
Dual JK Flip-Flop	1271	SN54LS112	3113
Dual 4-1 MUX	1272	SN54LS253	3115
Dual 2-4 DEMUX	1273	SN54LS155	3116
ALU	1274	SN54LS181	3118
4-Bit Counter	1276	SN54LS193	3120
4-Bit Shift Register	1277	SN54LS194	3121
4 x 4 Register File	1284	SN54LS670	3117
High Drive MUX	1789	NONE	3128
256 x 4 PROM	1786	HM-7611	3148

Future of Bipolar Digital IC's

- Advanced low power Schottky II Process development under way for Radiation-Hardened 4K RAM and 2000 Gate Array (5V only) applications.
- The first of a family of Dielectrically Isolated Rad-Hard STL Gate Arrays has completed development and prototype parts are being characterized. Requests for proposals on both a 936 gate CGA and 1950 gate CGA are now being accepted. By March 1984 an autoroute 1856 CGA will be developed which will allow up to 1000 gate personalizations.
- ASTL devices being characterized for full custom design applications.

Custom Integrated Circuits Division

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011-447-5334666
Telex: 848174 Harris G

Note: Custom Integrated Circuits Division maintains its own sales force.

BIPOLAR

Packaging 9

Package Availability

PART NUMBER		1* CERDIP	3* PLASTIC DIP	4* LEADLESS CARRIER	9* FLATPACK**
BIPOLAR MEMORY					
ORGANIZATION	**MARKETING PART #**				
Quad Power Strobe	HD-6600	4D	–	–	–
32 x 8 OC PROM	HM-7602	4Z	7H	–	–
32 x 8 TS PROM	HM-7603	4Z	7H	–	–
64 x 8 OC PROM	JAN-0512	4K	–	–	8F
256 x 4 OC PROM	HM-7610	4Z	7H	–	8B
256 x 4 TS PROM	HM-7611	4Z	7H	–	8B
256 x 4 OC PROM	HM-7610A	4Z	7H	–	8B
256 x 4 TS PROM	HM-7611A	4Z	7H	–	8B
256 x 4 OC PROM	HM-7610B	4Z	7H	–	8B
256 x 4 TS PROM	HM-7611B	4Z	7H	–	8B
512 x 4 OC PROM	HM-7620	4Z	7H	–	8B
512 x 4 TS PROM	HM-7621	4Z	7H	–	8B
512 x 4 OC PROM	HM-7620A	4Z	7H	–	8B
512 x 4 TS PROM	HM-7621A	4Z	7H	–	8B
512 x 4 OC PROM	HM-7620B	4Z	7H	–	8B
512 x 4 TS PROM	HM-7621B	4Z	7H	–	8B
512 x 8 OC PROM	HM-7640	4K, DC [1]	7C	–	8F
512 x 8 TS PROM	HM-7641	4K, DC [1]	7C	–	8F
512 x 8 OC PROM	HM-7640A	4K, DC [1]	7C	–	8F
512 x 8 TS PROM	HM-7641A	4K, DC [1]	7C	–	8F
512 x 8 TS PROM	HM-7649	5Z	7M	–	8D
512 x 8 TS PROM	HM-7649A	5Z	7M	–	8D
1024 x 4 OC PROM	HM-7642	4N	7V	–	8C
1024 x 4 TS PROM	HM-7643	4N	7V	–	8C
1024 x 4 OC PROM	HM-7642A	4N	7V	–	8C
1024 x 4 TS PROM	HM-7643A	4N	7V	–	8C
1024 x 4 OC PROM	HM-7642B	4N	7V	–	8C
1024 x 4 TS PROM	HM-7643B	4N	7V	–	8C
1024 x 8 TS PROM	HM-7681	4K, DC [1]	GA	LR	8F
1024 x 8 TS PROM	HM-7681A	4K, DC [1]	GA	LR	8F
2048 x 4 TS PROM	HM-7685	5E	7V	–	–
2048 x 4 TS PROM	HM-7685A	5E	7V	–	–
2048 x 8 TS PROM	HM-76161	5J, DC [1]	GA	LZ	8L
2048 x 8 TS PROM	HM-76161A	5J, DC [1]	GA	LZ	8L
4096 x 4 TS PROM	HM-76165	5M	–	–	–
4096 x 8 TS PROM	HM-76321	DA [2]	–	LV	–
8192 x 8 TS PROM	HM-76641	DA [2]	–	LV	–
DIODE MATRICES					
ORGANIZATION	**MARKETING PART #**				
6 x 8	HM-0168	4U	GC	–	9H
8 x 6	HM-0186	4U	GC	–	9H
4 x 10	HM-0410	4U	GC	–	9H
10 x 4	HM-0104	4U	GC	–	9H
9 x 8	HM-0198	4N	7W	–	–
PROGRAMMABLE LOGIC					
ARCHITECTURE	**MARKETING PART #**				
20-Pin IFL	HPL-77153/82S153	5Z	7J	–	–
20-Pin PAL	HPL-77216/16P8	5Z	7J	–	–
20-Pin PAL	HPL-77209/16L8	5Z	7J	–	–
20-Pin PAL	HPL-77215/16H8	5Z	7J	–	–
24-Pin FPAD	HPL-77061	5Z	7J	–	–

* These package numbers should be used in the product code when ordering. Other numbers shown in this table and in the Package Dimensions portion of this section are internal numbers to be used only to match the package code of a specific product with the package outline. Please note that other packaging options may be available. Contact your local Harris sales office regarding your requirements.

**Not Recommended For New Designs. Consult Factory.

NOTES: [1] Slimline CERDIP.
[2] Side-Brazed CERDIP.

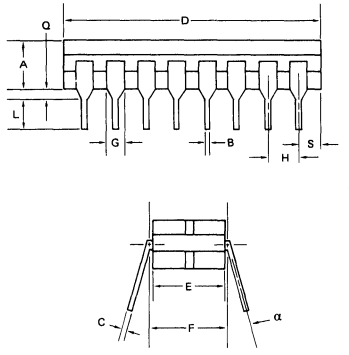
This table is provided as a quick reference for the approximate dimensions of all flatpacks available from Harris Semiconductor's Bipolar Digital Products Division. For more detailed information, see the package dimension diagrams, pages 9-5 through 9-7.

PACKAGE	LEAD COUNT	DEVICE	APPROXIMATE PACKAGE DIMENSIONS (INCHES)
CERPACKS			
9H	14	Diode Matrices (HM-0XXX)	.250 x .250
8F	24	1/2K (JAN-0512)	.375 x .375
8B	16	1K (HM-7611)	.375 x .375
8B	16	2K (HM-7621)	.375 x .375
8C	18	4K (HM-7643)	.375 x .375
8F	24	4K (HM-7641)	.375 x .375
8D	20	4K (HM-7649)	.375 x .375
8F	24	8K (HM-7681)	.375 x .375
8L	24	16K (HM-76161)	.500 x .375
LEADLESS CHIP CARRIERS			
LR	28	8K (HM-7681)	.450 x .450
LZ	28	16K (HM-76161)	.450 x .450
LV	28	32K (HM-76321)	.450 x .450
LV	28	64K (HM-76641)	.450 x .450

Package Dimensions

4D, 4U, 4Z, 4N, 5E, 5Z, 5M, DC

CERDIP .300

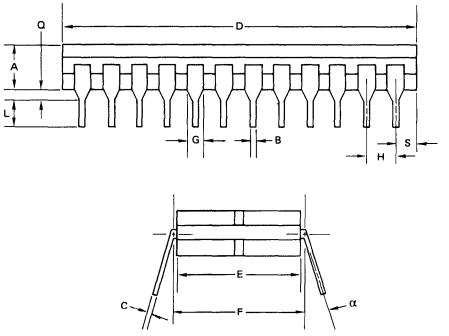


PKG. TYPE	LEAD COUNT	DIM. A	DIM. B	DIM. C	DIM. D	DIM. E	DIM. F	DIM. G	DIM. H	DIM. L	DIM. Q	DIM. S	DIM. α
4D	14 MSI	.140/.170	.016/.018	.008/.012	.760/.785	.265/.285	.290/.310	.050/.070	.090/.110	.125/.180	.020/.040	.070/.100	0°/15°
4U	14 SSI	.140/.170	.016/.018	.008/.012	.760/.785	.245/.265	.290/.310	.050/.070	.090/.110	.125/.180	.020/.040	.070/.100	0°/15°
4Z	16 MSI	.140/.170	.016/.018	.008/.012	.760/.790	.265/.285	.290/.310	.050/.070	.090/.110	.125/.150	.020/.040	.025/.045	0°/15°
4N 5E	18 LSI	.140/.170	.016/.018	.008/.012	.885/.915	.285/.305	.300/.320	.050/.070	.090/.110	.125/.180	.020/.040	.040/.060	0°/15°
5Z 5M	20 LSI	.140/.170	.016/.018	.008/.012	.940/.970	.285/.305	.300/.320	.050/.070	.090/.110	.125/.180	.020/.040	.020/.040	0°/15°
DC	24 SLIM	.150/.180	.016/.018	.008/.012	1.240/1.270	.285/.305	.300/.320	.050/.070	.090/.110	.125/.180	.020/.040	.060/.090	0°/15°

NOTE: 1) Dimensions are: MIN./MAX.
2) All Dimensions in inches

5J, 4K

CERDIP .600

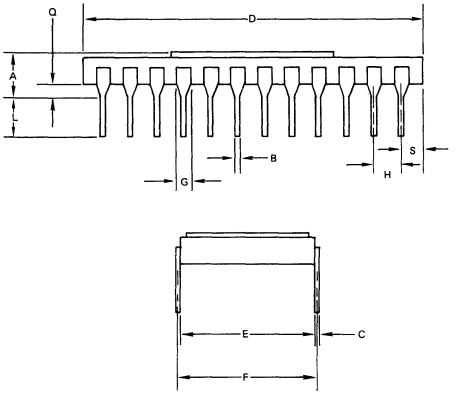


PKG. TYPE	LEAD COUNT	DIM. A	DIM. B	DIM. C	DIM. D	DIM. E	DIM. F	DIM. G	DIM. H	DIM. L	DIM. Q	DIM. S	DIM. α
5J 4K	24 MSI	.150/.180	.016/.018	.008/.012	1.24/1.27	.515/.535	.595/.615	.050/.070	.090/.110	.125/.180	.020/.045	.060/.090	0°/15°

NOTE: 1) Dimensions are: MIN./MAX.
2) All Dimensions in inches

DA

SIDE BRAZED



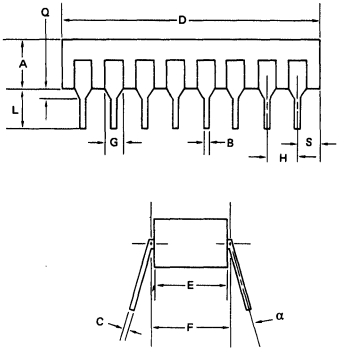
PKG. TYPE	LEAD COUNT	DIM. A	DIM. B	DIM. C	DIM. D	DIM. E	DIM. F	DIM. G	DIM. H	DIM. L	DIM. Q	DIM. S
DA	24	.122/.158	.016/.020	.009/.012	1.188/1.212	.587/.603	.588/.612	.040/.054	.100 BSC	.125/.180	.040/.060	.040/.060

NOTE: 1) Dimensions are: MIN./MAX.
2) All Dimensions in inches

Package Dimensions

GC, 7H, 7W, 7V, 7M, 7J

PLASTIC .300

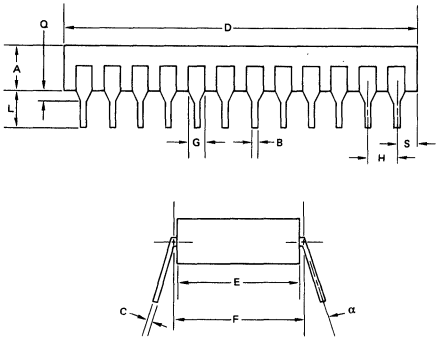


PKG. TYPE	LEAD COUNT	DIM. A	DIM. B	DIM. C	DIM. D	DIM. E	DIM. F	DIM. G	DIM. H	DIM. L	DIM. Q	DIM. S	DIM. α
GC	14	.125/.140	.016/.020	.008/.012	.750/.770	.245/.265	.290/.310	.050/.070	.090/.110	.150/.170	.020/.040	.030/.050	0°/15°
7H	16	.125/.140	.016/.020	.008/.012	.750/.770	.245/.265	.290/.310	.050/.070	.090/.110	.150/.170	.020/.040	.025/.035	0°/15°
7W 7V	18	.125/.140	.016/.020	.008/.012	.900/.920	.245/.265	.290/.310	.050/.070	.090/.110	.150/.170	.020/.040	.040/.060	0°/15°
7M 7J	20	.130/.145	.016/.020	.008/.012	1.030/1.050	.250/.270	.290/.310	.050/.070	.090/.110	.150/.170	.020/.040	.060/.080	0°/15°

NOTE: 1) Dimensions are: MIN./MAX.
2) All Dimensions in inches

7C, GA

PLASTIC .600

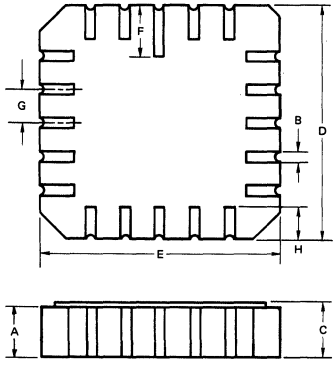


PKG. TYPE	LEAD COUNT	DIM. A	DIM. B	DIM. C	DIM. D	DIM. E	DIM. F	DIM. G	DIM. H	DIM. L	DIM. Q	DIM. S	DIM. α
7C GA	24	.145/.155	.016/.020	.008/.012	1.24/1.26	.540/.560	.590/.610	.050/.070	.090/.110	.150/.170	.020/.040	.065/.085	0°/15°

NOTE: 1) Dimensions are: MIN./MAX.
2) All Dimensions in inches

LZ, LR, LV

LEADLESS CHIP CARRIER

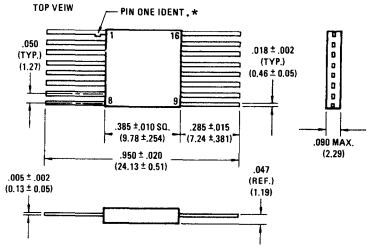


PKG. TYPE	LEAD COUNT	DIM. A	DIM. B	DIM. C	DIM. D	DIM. E	DIM. F	DIM. G	DIM. H
LZ, LR, LV	28 .450 sq.	.050/.078	.020/.030	.060/.090	.442/.458	.442/.458	.060/.095	.050 BSC	.040/.065

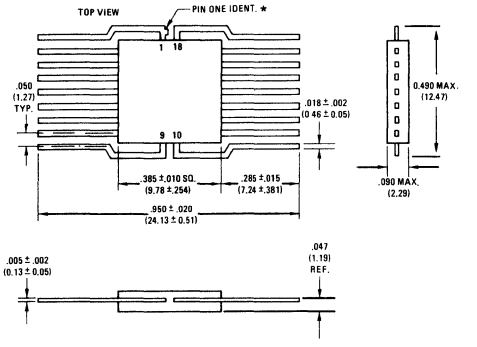
NOTE: 1) Dimensions are: MIN./MAX.
2) All Dimensions in inches

Package Dimensions

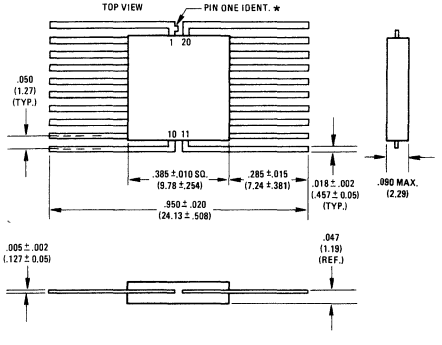
8B 16 LEAD CERPACK



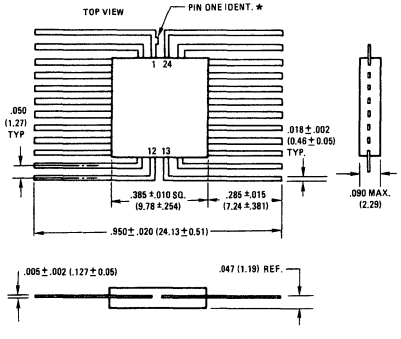
8C 18 LEAD CERPACK



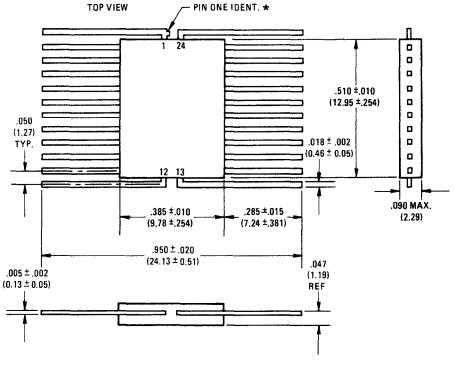
8D 20 LEAD CERPACK



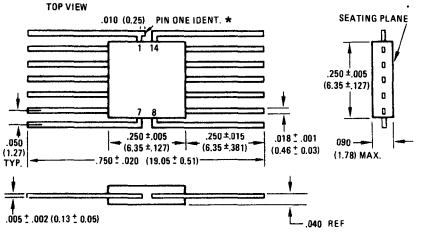
8F 24 LEAD CERPACK



8L 24 LEAD CERPACK



9H 14 LEAD FLATPACK



* Pin One Identification for Harris Semiconductor Products Packaged in Flatpacks is accomplished in one of three ways:

1) Shortened Pin One Lead
2) Tab on Pin One Lead
3) Branded Dot

For the sake of clarity, tabs are used here on all diagrams.

Thermal Resistance Measurements

The thermal resistance of a device/package system is defined as:

$$\theta_{JA} = \frac{T_J - T_A}{P} \quad \text{or} \quad \theta_{JC} = \frac{T_J - T_C}{P}$$

where T_J is the junction temperature when operated at power P. T_A is the temperature of the surrounding ambient, and T_C is the case temperature. θ_{JA} is dependent on the device fixturing and is generally measured with the device in a socket, in still air. θ_{JC} is measured with the case temperature controlled by immersion in a temperature controlled liquid or through other heat sinking.

The junction temperature is measured by calibrating the forward bias voltage of a junction on the device being tested. Generally, a junction of an output transistor is used. The junction is calibrated by immersion in liquid baths of known temperatures. The voltage generated by a 100μA current is measured, and a straight line fitted to the voltage/temperature values.

The thermal resistance is measured using the basic system shown in Figure 1. The VCC of the device under test (DUT) is switched off when the junction temperature is being measured. The switching circuitry is designed to pull VCC to zero volts within three μsecs. VCC is kept off for a period of 50 μsecs. The signal to the sample and hold triggers a sample period of 14 μsecs starting when VCC is switched off. This cycle is repeated every 20 msecs giving a power on duty cycle of greater than 99%. The overall period, VCC off time and sample time, are adjustable.

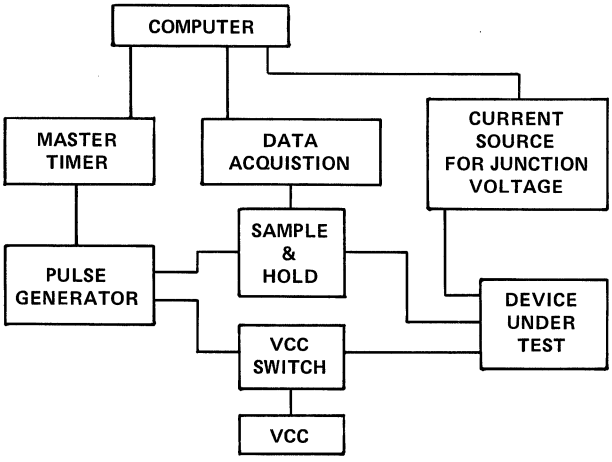


Figure 1.

The case temperature is measured by a thermocouple centered under the die and between the case and socket. This configuration allows for the determination of the true case temperature of the device/package under test. The temperature measured by this thermocouple is used to determine the case temperature used to calculate θ_{JC}.

Measurements are done using a computer controlled system to record the data, calculate the temperature calibration, the thermal resistance, and to switch the VCC, 100μA current and measuring system to one of a series of devices being measured. Presently, capacity is limited to 10 devices at a time. The capability to obtain measurements as a function of air velocity will be available in the near future.

The table below summarizes the results of measurements made on the most popular bipolar devices using this automated thermal resistance test system. Please note that the values quoted are typical values and, as such, are provided for general guidance only.

For further information on thermal resistance, contact the factory.

		CERAMIC		PLASTIC	
		θ_{JA}	θ_{JC}	θ_{JA}	θ_{JC}
PRODUCT	PACKAGE	°C/WATT	°C/WATT	°C/WATT	°C/WATT
HM-7602/03	16 PIN DIP	75.7	16.7	87.5	28.2
JAN-0512	24 PIN DIP	51.0	15.0	NA	NA
HM-7610/11 (A,B)	16 PIN DIP	74.2	14.5	85.0	25.0
HM-7620/21 (A,B)	16 PIN DIP	70.0	13.0	81.7	22.4
HM-7649 (A)	20 PIN DIP	66.4	13.5	68.0	20.0
HM-7640/41 (A)	24 PIN DIP	48.1	13.9	46.5	25.6
HM-7642/43 (A,B)	18 PIN DIP	69.8	17.8	76.1	28.9
HM-7681 (A)	24 PIN DIP	51.8	13.9	55.7	23.1
HM-7685 (A)	18 PIN DIP	65.1	12.9	78.3	21.7
HM-76161 (A)	24 PIN DIP	45.5	13.0	48.9	17.8
HM-76165	20 PIN DIP	59.1	8.9	NA	NA
HM-76321	24 PIN DIP	49.2*	12.2*	NA	NA
HM-76641	24 PIN DIP	49.4*	13.4*	NA	NA
HPL-77153	20 PIN DIP	54.8	7.8	60.9	20.3
HPL-77209/215/216	20 PIN DIP	60.9	8.4	58.9	20.6
HM-7681 (A)	28 PAD LCC	67.6	18.8	NA	NA
HM-76161 (A)	28 PAD LCC	64.1	17.9	NA	NA
HM-76321	28 PAD LCC	65.2	17.0	NA	NA
HM-76641	28 PAD LCC	61.0	15.8	NA	NA

*Side-Brazed DIP

NOTE: For more details on package configurations, see pages 9-5 through 9-7.

Bipolar Memory Products General Chip Information

Bipolar memory chips offer reliability and performance comparable to that of the Harris established high standards for packaged parts.

This information describes the following items:

- Product Assurance at Harris
- Standard Chip Processing
- Product Testing
- Mechanical Information
- Passivation
- Storage
- Shipping
- Recommended Handling and Die Attachment
- Recommended Bonding Procedures
- Ordering Information
- Options Available/Special Orders
- Return Policy
- Dice Layout & Geometric Information

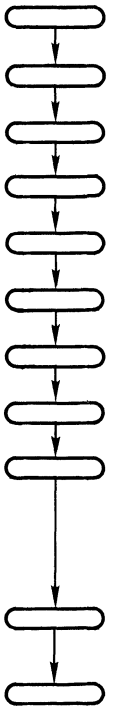
Product Assurance at Harris

Our Product Assurance Department strives to insure that the dice shipped to our customers are reliable, of a high quality level, and consistent with customer requirements. During product processing, there are several independent visual and electrical checks performed by Quality Assurance personnel based on various process and control documents. This insures that the dice meet the specifications controlling fabrication and workmanship, thus enhancing the quality and reliability of the product.

A final inspection prior to shipment is performed at Quality Assurance Plant Clearance to insure that all requirements of the purchase order and customer specifications are met. The systems procedures implemented are based on Military Standards.

Standard Chip Processing

Harris maintains the same processing and control requirements for chips destined for dice sales as for those assembled in packages. This insures the continued reliability and high performance of Harris chips. The following diagram shows the processing steps for chips once the wafer has been processed.



Wafer Processing

100% Wafer Probe for DC/AC characteristics

In-Process Sample Inspection

Scribe and Break

Die Sort

Die Clean

100% Visual

Dice to Q.A. for acceptance

Q.A. Sample Inspection
- Acceptance Visual Test to LTPD of 5%
- Physical Quantity
- Confirmation of Product
- Documentation

Q.A. Plant Clearance – Final inspection of packaging, quantity, marking per customer requirements

Shipping

Product Testing

All chips offered in the data book are 100% visual screened to meet the criteria of Method 2010, Test Condition B. This is the standard visual test for all chips available from the data book.

Most of the chips provided by Harris are available in both commercial (-6) and military (-2) grade. Consult the specific data sheet to determine which grades are available for a particular chip. Bipolar programmable memory devices are supplied unpatterned. If patterned devices are required, consult the factory for special options. The following electrical tests are applicable:

1. Chips are 100% probe tested at 25°C for commercial product (-6) and military grade (-2).

2. The DC and AC data sheet characteristics will be guaranteed or 100% tested as follows:

   a. Guaranteed not tested: V_{IH}/V_{IL}
      Input/Output Capacitance

   b. Tested; I_{IH}, V_{CL}, I_{IL}, I_{OS}, V_{OH}, I_{CC}, V_{OL}, T_{AA}, I_{OHE}, T_{EA}, I_{OLE}

3. Commercial product (-6) chips are 100% probe tested to guarantee the max/min characteristics listed in the data sheets over the temperature range from 0°C to +75°C.

These DC and AC characteristics are guaranteed to the following LTPDs at 25°C.

a. LTPD of 10/1 for DC characteristics
b. LTPD of 10/1 for AC characteristics

4. Military grade (-2) chips are 100% probe tested at +25°C to guarantee the max/min characteristics listed in the data sheets over the temperature range from -55°C to +125°C. These DC and AC characteristics are guaranteed to the following LTPDs:

   a. LTPD of 10/1 for DC characteristics at +25°C.
   b. LTPD of 15/2 for DC characteristics at +125°C.
   c. LTPD of 15/2 for DC characteristics at -55°C.
   d. LTPD of 10/1 for AC characteristics at +25°C.

To assure that the DC and AC characteristics are being consistently met, the chips are sampled systematically by Quality Assurance. The dice are assembled in standard packages and tested at the appropriate temperatures to the LTPDs stated above.

Lot acceptance send ahead testing for DC and AC specifications is available as an option at an additional charge when ordering chips. Sample dice are assembled in a standard package and tested to the indicated LTPDs. Consult the factory when placing an order requiring lot acceptance send ahead test data.

Quality Assurance also systematically samples wafer lots using a Scanning Electron Microscope (SEM) for inspection of the metallization. This test is available as an option at an additional charge for most orders. Please consult the factory for additional information.

Mechanical Information

Dimensions: All chips dimensions given in the layouts in the data sheet section are nominal with a tolerance of ±.003 inches (±.08mm). Die thickness is nominally .020 inches ±.002 inches.

Bonding Pads: Minimum bonding pad size is .004 x .004 inches (.10mm x .10mm).

Passivation

All Harris dice are passivated with a layer of protective material to guard against deterioration of the dice. Passivation is applied to all areas of the die except the bonding pads and scribe lines.

Storage

Harris stores its dice in a dry nitrogen atmosphere and recommends that the customer do the same. If dice are exposed to air, the aluminum metallization will slowly oxidize at the bonding pads. The aluminum oxide will make bonding more difficult, especially if thermal compression gold ball bonding is used.

The humidity should be kept as low as possible with a relative humidity of no more than 50%.

Shipping

Dice are placed in conductive waffle carriers and covered with layer of bibilious paper and with a layer of mylar. The waffle pack is then sealed and labeled. The label contains the

part number of the chips, the quantity, and the lot number. The waffle pack is placed in a polyethylene bag along with a humidity indicating desiccant. The bag is then heat sealed and packaged in a suitable shipping container.

Recommended Handling

It is suggested that all dice be handled, tested, and installed using standard MOS handling techniques. This includes the use of conductive carriers and grounding of equipment and personnel. It has been found that handling equipment and personnel can generate static potentials in excess of 10kV in a low humidity environment. Therefore, proper handling procedures must be adopted to reduce static charge. Harris recommends using the following procedures when handling dice:

1. Use conductive work stations. Metallic or conductive plastic* tops on work benches connected to ground help eliminate static build-up.

2. Ground all handling equipment. To prevent scratches, it is recommended that a vacuum pick-up with protected tip be used for handling the dice. If tweezers are used, the dice should be gripped only on its sides.

3. Ground all handling personnel with a conductive bracelet through a 1M ohm resistor to ground. The resistor will prevent electroshock to personnel.

4. Smocks, clothing, and especially shoes of certain insulating materials (notably nylon) should not be worn in areas when devices are handled. These materials, highly dielectric in nature, will hold or aid in the generation of a static charge. Instead, natural materials such as cotton should be used to minimize charge generation.

5. Ionized air blowers reduce charge build-up in areas where grounding is not possible or desirable.

6. Devices should be in conductive carriers during all phases of transport.

*Supplier 3M Company "Velostat"

Recommended Die Attachment

Harris uses gold eutectic die-attach for its packaged circuits and recommends this procedure for use with its chips. The die-attach area of the package should be gold plated. Gold preforms are usually not required. The recommended temperature for die-attachment is 420°C ±10°C, and should remain constant throughout the procedure. To prevent oxidation, a laminar flow of approximately 30 liters/hour of nitrogen should be provided over the chip surface.

The package should be placed on the heater block and allowed to arrive at a uniform temperature. With tweezers, the die should be picked up and placed on the package. Using an orbital motion, the die should be rubbed on the package until eutectic melt is visible along the entire periphery of the die. There should be no evidence of balling or flaking of die-attach material. The die should be level with respect to the package and the die-attach material should be no higher than the top edges of the die.

Although Harris recommends using gold eutectic die-attach, conductive epoxy die-attach may also be used. Specific directions depend upon the epoxy used.

Recommended Bonding Procedures

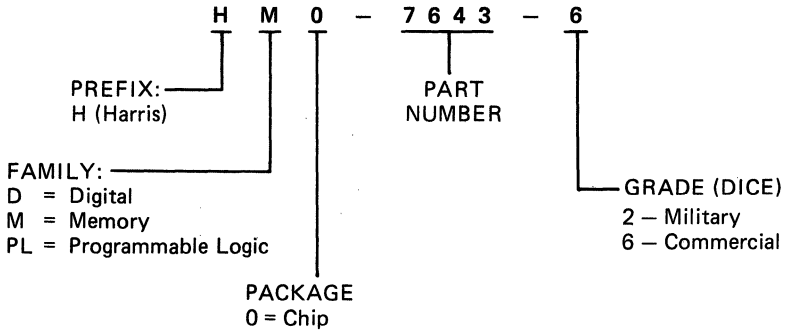
Harris uses ultrasonic aluminum wire bonding and recommends this procedure be used by

our customers for best results. Harris uses an aluminum-silicon alloy wire, 99% aluminum and 1% silicon. The diameter is 0.00125 inches, tensile strength is 22±2g, and elongation is 1.0 to 4.5%. Harris recommends similar wire be used by the customer. Actual bonding procedure will be governed by the manufacturers' instructions for the particular bonding equipment being used. A minimum bond pull strength of 3g is recommended to assure mechanical bond quality.

Ordering Information

Harris chips are designated by a product code. When ordering standard chips from this data book, please refer to the chips by the full product code. Harris chip codes will always begin with an H. Specific device numbers will always be isolated by hyphens.

Chip Code Example



Chips are generally available on new Harris ICs at the time of introduction. Consult a salesman, representative of the factory regarding availablity, specifications, and minimum order requirements.

BIPOLAR

Sales Locations

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Alpha-Numeric Product Index

Analog

PRODUCT	DESCRIPTION
HA-1608	+10V Adjustable Voltage Reference
HA-2400/04/05	PRAM, Four Channel Operational Amplifiers
HA-2420/25	Fast Sample and Hold Operational Amplifiers
HA-2420/02/05	Precision High Slew Rate Operational Amplifiers
HA-2500/02/05	Precision High Slew Rate Operational Amplifiers
HA-2510/12/15	High Slew Rate Operational Amplifiers
HA-2520/22/25	Uncompensated High Slew Rate Operational Amplifiers
HA-2539	Super High Slew Rate Wideband Operational Amplifiers
HA-2540	Ultra High Slew Rate Operational Amplifiers
HA-2600/02/05	Wideband, High Impedance Operational Amplifiers
HA-2620/22/25	Very Wideband, Uncompensated Operational Amplifiers
HA-2630/35	High Performance Current Booster
HA-2640/45	High Voltage Operational Amplifiers
HA-2650/55	Dual High Performance Operational Amplifiers
HA-2720/25	Wide Range Programmable Operational Amplifiers
HA-2730/35	Wide Range Dual Programmable Operational Amplifiers
HA-2740	Quad Programmable Operational Amplifiers
HA-4156	High Performance Quad Operational Amplifiers
HA-4600/02/05	High Performance Quad Operational Amplifiers
HA-4620/22/25	Wideband, High Performance Quad Operational Amplifiers
HA-4741	Quad Operational Amplifier
HA-4900/0205	Precision Quad Comparators
HA-5033	High-Speed Current Buffer
HA-5062	Dual Low Power, JFET Input Operational Amplifier
HA-5064	Low Power, JFET Input Quad Operational Amplifier
HA-5082	Dul JFET Input Operational Amplifer
HA-5084	JFET Input Quad Operational Amplifier
HA-5100/05	Wideband, JFET Input Operational Amplifiers
HA-5110/15	Wideband, JFET Input, Uncompensated Operational Amplifiers
HA-5130/35	Precision Operational Amplifiers
HA-5141/42/44	Power Operational Amplifier, Single, Dual & Quad
HA-5160/62	Wideband, JFET Input, High Slew Rate, Uncompensated Operational Amplifiers
HA-5170	Precision JFET Input Operational Amplifiers
HA-5180/5180A	Ultra Low I_{BIAS} JFET Input Precision Operational Amplifier
HA-5190/95	Wideband, Fast Settling Operational Amplifiers
HA-5320	High Speed Precision Monolithic Sample and Hold Amplifier
HC-5116A/5156A	Monolithic CODECS (Preliminary)
HC-5502	SLIC-LC Subscriber Line Interface Circuit (PBX)
HC-5504	SLIC-LC Subscriber Line Interface Circuit (PBX)
HC-5510/5511	Monolithic CODECs (Preliminary)
HC-5512/5512A	PCM Monolithic Filter
HC-55536	Decode Digital Continuously Variable Slope Delta Modulator (CVSD)
HC-55564	Encode and Decode all Digtal Continuously Variable Slope Delta Modulator (CVSD)

Analog (Continued)

PRODUCT	DESCRIPTION
HD-0165	Keyboard Encoder
HI-200	Dual SPST CMOS Analog Switch
HI-201	Quad SPST CMOS Analog Switch
HI-201HS	High Speed Quad SPST CMOS Analog Switch
HI-300	Dual SPST CMOS Analog Switch
HI-301	SPDT CMOS Analog Switch
HI-302	Dual DPST CMOS Analog Switch
HI-303	Dual SPDT CMOS Analog Switch
HI-304	Dual SPST CMOS Analog Switch
HI-305	SPDT CMOS Analog Switch
HI-306	Dual DPST CMOS Analog Switch
HI-307	Dual SPDT CMOS Analog Switch
HI-381	Dual SPST CMOS Analog Switch
HI-384	Dual DPST CMOS Analog Switch
HI-387	SPDT CMOS Analog Switch
HI-390	Dual SPDT CMOS Analog Switch
HI-506/507	Single 16/Differential 8 Channel CMOS Analog Multiplexers
HI-506A/507A	16 Channel CMOS Analog Multiplexers with Overvoltage Protection
HI-506L/507L	Latched, 16/8 Channel Analog Multiplexer
HI-508/509	Single 8/Differential 4 Channel CMOS Analog Multiplexers
HI-508A/509A	8 Channel CMOS Analog Multiplexers with Overvoltage Protection
HI-508L/509L	Latched, 8/4 Channel Analog Multiplexer
HI-516	16 Channel/Differential 8 Channel CMOS High Speed Analog Multiplexer
HI-518	8 Channel/Differential 4 Channel CMOS High Speed Analog Multiplexer
HI-524	4 Channel Video Multiplexer
HI-539	Monolithic, Four Channel, Low Level, Differential Multiplexer
HI-562A	12 Bit High Speed Monolithic Digital-to-Analog Converter
HI-565A	High Speed Monolithic Digital-to-Analog Converter with Reference
HI-574A	Fast, Complete 12 Bit A-to-D Converter with P Interface
HI-674A	High Speed, Complete 12-Bit A-to-D Converter with P Interface
HI-1818A/1828A	Low Resistance 8 Channel CMOS Analog Multiplexer
HI-5040	Low Resistance SPST Switch
HI-5041	Low Resistance Dual SPST Switch
HI-5042	Low Resistance SPDT Switch
HI-5043	Low Resistance Dual SPDT Switch
HI-5044	Low Resistance DPST Switch
HI-5045	Low Resistance Dual DPST Switch
HI-5046	Low Resistance DPDT Switch
HI-5046A	Low Resistance DPDT Switch
HI-5047	Low Resistance 4PST Switch
HI-5047A	Low Resistance 4PST Switch
HI-5048	Low Resistance Dual SPST Switch
HI-5049	Low Resistance Dual DPST Switch
HI-5050	Low Resistance SPDT Switch
HI-5051	Low Resistance Dual SPDT Switch
HI-5610	10 Bit High Speed Monolithic Digital-to-Analog Converter

Analog (Continued)

PRODUCT	DESCRIPTION
HI-5618A/18B	8 Bit High Speed Digital-to-Analog Converters
HI-5660	High Speed Monolithic D-to-A Converter
HI-5680	12 Bit Low Cost Monolithic D-to-A Converter
HI-5685	High Performance Monolithic 12 Bit D-to-A Converter
HI-5687	Wide Temperature Range Monolithic 12 Bit D-to-A Converter
HI-5712/12A	High Performance 12 Bit Analog-to-Digital Converters
HI-5900	Analog Data Acquisition Signal Processor
HI-5901	Analog Data Acquisition Signal Processor
HI-7541	12 Bit Multiplying Monolithic Digital-to-Analog Converter
HI-DAC801	12 Bit High Speed Monolithic Digital-to-Analog Converter
HI-DAC16B/C	16 Bit D-to-A Converter
HV-1000/1000A	Single-Phase Induction Motor Energy Saver
LF347	Wideband Quad JFET Input Operational Amplifiers
LF353	Wideband Dual JFET Input Operational Amplifier
LF355 Series	Monolithic JFET Input Operational Amplifiers
LF356 Series	Wideband Monolithic JFET Input OPerational Amplifiers
LF357 Series	Decompensated Wideband Monolithic JFET Input Operational Amplifiers
LM118/318	Operational Amplifiers
LM143/343	High Voltage Operational Amplifiers

Bipolar

PART NUMBER	DESCRIPTION
HD-6600	Quad Power Strobe
HM-0104	10 x 4 Diode Matrix
HM-0168	6 x 8 Diode Matrix
HM-0186	8 x 6 Diode Matrix
HM-0198	9 x 8 Diode Matrix
HM-0410	4 x 10 Diode Matrix
HM-7602/03	32 x 8 Bit Generic PROM
HM-7610/11	256 x 4 Bit Generic PROM
HM-7610A/11A	256 x 4 Bit High Speed Generic PROM
HM-7610B/11B	256 x 4 Bit Very High Speed Generic PROM
HM-7620/21	512 x 4 Bit Generic PROM
HM-7620A/21A	512 x 4 Bit High Speed Generic PROM
HM-7620B/21B	512 x 4 Bit Very High Speed Generic PROM
HM-7640/41	512 x 8 Bit Generic PROM (24-Pin)
HM-7640A/41A	512 x 8 Bit High Speed Generic PROM (24-Pin)
HM-7649	512 x 8 Bit Generic PROM (20-Pin)
HM-7649A	512 x 8 Bit High Speed Generic PROM (20-Pin)
HM-7642/43	1024 x 4 Bit Generic PROM
HM-7642A/43A	1024 x 4 Bit High Speed Generic PROM
HM-7642B/43B	1024 x 4 Bit Very High Speed Generic PROM
HM-7681	1024 x 8 Bit Generic PROM
HM-7681A	1024 x 8 Bit High Speed Generic PROM
HM-7685	2048 x 4 Bit Generic PROM
HM-7685A	2048 x 4 Bit High Speed Generic PROM
HM-76161	2048 x 8 Bit Generic PROM
HM-76161A	2048 x 8 Bit High Speed Generic PROM
HM-76161B	2048 x 8 Bit Very High Speed Generic PROM
HM-76165	4096 x 4 Bit Generic PROM
HM-76321	4096 x 8 Bit Generic PROM
HM-76641	8192 x 8 Bit Generic PROM
HM-76641A	8192 x 8 Bit High Speed Generic PROM
JAN-0512	64 x 8 HPROM
HPL-77061	24-Pin Field Programmable Address Decoder
HPL-77153/82S153	20-Pin Field Programmable Logic Array
HPL-77209/16L8	20-Pin Field Programmable Array Logic (Active Low Outputs)
HPL-77210/16R4	20-Pin Field Programmable Array Logic (Four Registered Outputs)
HPL-77211/16R6	20-Pin Field Programmable Array Logic (Six Registered Outputs)
HPL-77212/16R8	20-Pin Field Programmable Array Logic (Eight Registered Outputs)
HPL-77215/16H8	20-Pin Field Programmable Array Logic (Active High Outputs)
HPL-77216/16P8	20-Pin Field Programmable Array Logic (Programmable Output Polarity)
HPL-77317/16LD8	20-Pin Field Programmable Array Logic (Active Low Dedicated Outputs)
HPL-77318/16HD8	20-Pin Field Programmable Array Logic (Active High Dedicated Outputs)
HPL-77319/16LE8	20-Pin Field Programmable Array Logic (Enhanced HPL-77317/16LD8)
HPL-77320/16HE8	20-Pin Field Programmable Array Logic (Enhanced HPL-77318/16HD8)
M38510/20701BEB	32 x 8 Open Collector QPL1 PROM
M38510/20702BEB	32 x 8 Three State QPL1 PROM
M38510/20101BJB	64 x 8 Open Collector QPL1 PROM
M38510/20301BEB	256 x 4 Open Collector QPL1 PROM
M38510/20302BEB	256 x 4 Three State QPL1 PROM
M38510/20401BEB	512 x 4 Open Collector QPL1 PROM
M38510/20402BEB	512 x 4 Three State QPL1 PROM
M38510/20801BJB	512 x 8 Open Collector QPL1 PROM
M38510/20802BJB	512 x 8 Three State QPL1 PROM
M38510/20601BVB	1024 x 4 Open Collector QPL1 PROM
M38510/20602BVB	1024 x 4 Three State QPL1 PROM
M38510/20904BJB	1024 x 8 Three State QPL1 PROM
M38510/20902BVB	2048 x 4 Three State QPL1 PROM
M38510/21002BJB	2048 x 8 Three State QPL1 PROM

CMOS

PRODUCT	DESCRIPTION
HD-15530	Manchester Encoder-Decoder
HD-15531	Manchester Encoder-Decoder
HD-4702	Programmable Bit Rate Generator
HD-6101	Parallel Interface Element
HD-6120	12 Bit High Performance Microprocessor
HD-6121	I/O Controller
HD-6402	LSI Universal Asynchronous Receiver Transmitter
HD-6406	Programmable Asynchronous Communication Interface
HD-6408	Asynchronous Manchester Adapter
HD-6409	Manchester Encoder-Decoder
HD-6431	Hex Latching Bus Driver
HD-6432	Hex Bi-directional Bus Driver
HD-6433	Quad Bus Separator/Driver
HD-6434	Octal Resettable Latch
HD-6436	Octal Bus Buffer/Driver
HD-6440	Latch Decoder/Driver
HD-6495	Hex Bus Driver
HM-6100	12 Bit Static Microprocessor
HM-6504	4K X 1 Synchronous RAM
HM-6508	1K X 1 Synchronous RAM
HM-6514	1K X 4 Synchronous RAM
HM-6516	2K X 8 Synchronous RAM
HM-65162	2K X 8 Asynchronous RAM
HM-65172	2K X 8 Asynchronous RAM
HM-6518	1K X 1 Synchronous RAM
HM-65262	16K X 1 Asynchronous RAM
HM-6551	256 X 4 Synchronous RAM
HM-6561	256 X 4 Synchronous RAM
HM-6564	64K Synchronous RAM Module
HM-6616	2K X 8 Fuse Link PROM
HM-6641	512 X 8 PROM
HM-6664	8K X 8 Fuse Link PROM
HM-92560	256K Synchronous RAM Module
HM-92570	256K Synchronous RAM Module - Buffered
HPL- 16LC8	Programmable Logic
HPL-16RC4	Programmable Logic
HPL-16RC6	Programmable Logic
HPL-16RC8	Programmable Logic
80C86	16 Bit Microprocessor
80C88	8 Bit Microprocessor
82C37A	High Performance Programmable DMA Controller
82C52	Serial Controller Interface
82C54	Programmable Interval Timer
82C55A	Programmable Peripheral Interface
82C59A	Priority Interrupt Controller
82C82	Octal Latch
82C83	Octal Latching Inverting Bus Driver
82C84A	Clock Generator/Driver
82C86	Octal Bus Transceiver
82C87	Octal Inverting Bus Transceiver
82C88	Bus Controller
82C89	Bus Arbiter

Harris Sales Locations

OEM Sales

EASTERN REGION

Suite 215
3890 West Commercial Blvd.
Ft. Lauderdale, FL 33309
(305) 739-0016

Suite 400
875 Johnson Ferry Road
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(404) 256-4000

Suite 308
1 Burlington Woods Drive
Burlington, MA 01803
(617) 273-5942

P. O. Box 31747
Raleigh, NC 27622

Suite 1101
996 Old Eagle School Road
Wayne, PA 19087
(215) 687-6680

Suite 273
555 Broadhollow Road
Melville, L. I., NY 11747
(516) 249-4500

CENTRAL REGION

Suite 300
6400 Shafer Court
Rosemont, IL 60018
(312) 692-4960

Suite 101
1717 East 116th Street
Carmel, IN 46032
(317) 844-8011

Suite 703
2850 Metro Drive
Minneapolis, MN 55420
(612) 854-3558

Suite 110
17120 Dallas Parkway
Dallas, TX 75248
(214) 248-3237

WESTERN REGION

Suite 250
1717 E Morten Avenue
Phoenix, AZ 85020
(602) 870-0080

Suite 320
1503 South Coast Drive
Costa Mesa, CA 92626
(714) 540-2176

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883 Stierlin Road
Mt. View, CA 94043
(415) 964-6443

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6400 Canoga Avenue
Woodland Hills, CA 91367
(213) 992-0686

33919 9th Avenue South
Federal Way, WA 98003
(206) 838-4878

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153 Farnham Road
Slough SL1 4XD
Int'l. Tel.: 44-753-34666
TWX: 848174

ITALY

Harris Italiana, Inc.
20092 Cinisello Balsamo (Milano)
Via Fratelli Cracchi 48
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TWX: 5-213-866

Harris/Matra-Harris Semiconductor
Walsroderstrasse 71
D-3012 Langenhagen 1
Tel: 49-511-737037
TWX: 9 230 474 HM HH D

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AUSTRIA

Transistor Vetriebsgesellschaft
mbH & Co. KG.
Auhofstr. 41A
A-1130 Wien
Tel: 43-0222-82-94-01
TWX: 133738 TVGWN

BELGIUM

Betea S.A
755 Chaussee de Louvain
B-1140 Brussels
Tel: 32-2-7368050
TWX 23188

DENMARK

Ditz Schweitzer A. S.
Vallensbaekvej 41
DK-2600 Glostrup
Tel: 45-2-453044
TWX: 33257

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Yleiselektronikka OY
Atomitie 5 B (P.O. Box 33)
SF-00370 Helsinki 37
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6 Av Charles de Gaulle
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Matra Harris Semiconductor
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Postfach 1240
D-2085 Quickborn
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TWX:213590

Jermyn GmbH
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Postfach 1180
D-6277 Camberg-Wuerges
Tel: 49-6434-231
TWX: 4884426

Kontrol Halbleiter GmbH
Breslauer Str. 2
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TWX 522122

SASCO GmbH
Hermann-Oberth-Strasse 16
D-8011
Putzbrunn
Tel: 49-89-4611-1

Spoerle Electronic KG
Max-Planck-Str. 1-3
D-6072 Dreieich Bei
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Tel: 49-6103-30-40

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MRBD Industries Ltd.
P.O. Box 1717
54 Jabotinsky street
Ramat-Gan 52117
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722-367
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3S SPA
Viale Elvezia 18
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TWX: 331612

Lasi Elettronica
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TWX: 337612

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Tel.: 472-64-49-70
TELEX 71265 nen

REPUBLIC OF S. AFRICA

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P.O. Box 6090
Dunswart, 1508
Boksburg East Trasvaal
Tel.: 27-11-892-1001
TWX: 4-25559

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Torre de Madrid
Planta 12 Officina 9
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Tel: 34-242-5204
TWX 22596

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Macro Marketing Ltd.
396 Bath Road
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TWX: 847945

Radio Resistor Co. Ltd.
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Cambridge Road
Bedford MK 42 OLF
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TWX: 837508

SDP
(Semi Ltd.)
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Hartlepool, Cleveland TS26 90U
Int'l. Tel.: 44-429-33721
TWX: 587650 Sempro

Thame Components Ltd.
Thame Park Ind. Estate
Thame, Oxon OX9 3RS
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TWX 837508

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TWX: 777404

Ireland Representative

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Trim
County Meath
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Tel.: 353-46-36263
TWX: 90342

Far East

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TWX: 326525

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AUSTRALIA

VSI Electronics
35-37 Dickson Avenue
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Tel.: 61-439-4655
TWX A22846

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Enterprex Int'l Corp.
3900 E. Whiteside Street
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Fegu Incorporated
Electronics Division
2584 Wyandotte St.
Mountain View, CA 94043
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TWX: 176-572

Zenith Electronics
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Nariman Point
Bombay

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Argentina
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TWX: CABINA PUBLICA N9

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Rua da Consolacao 867 - Conj. 22
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Tel: (PABX): 9-011-55-11-255-1733

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P. O. Box 883
Melbourne, FL 32902
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TWX: 510-959-6259

SEMICONDUCTOR DIGITAL PRODUCTS DIVISION

Harris Semiconductor Spectrum of Products:

Analog

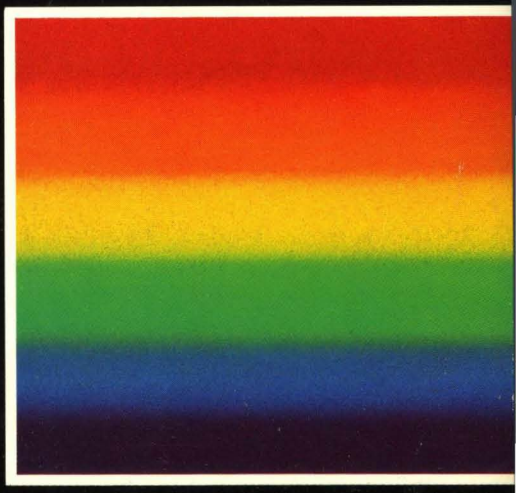
Bipolar Digital

CMOS Digital

Gallium Arsenide

Semicustom

Custom



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... Your Competitive Edge

HARRIS