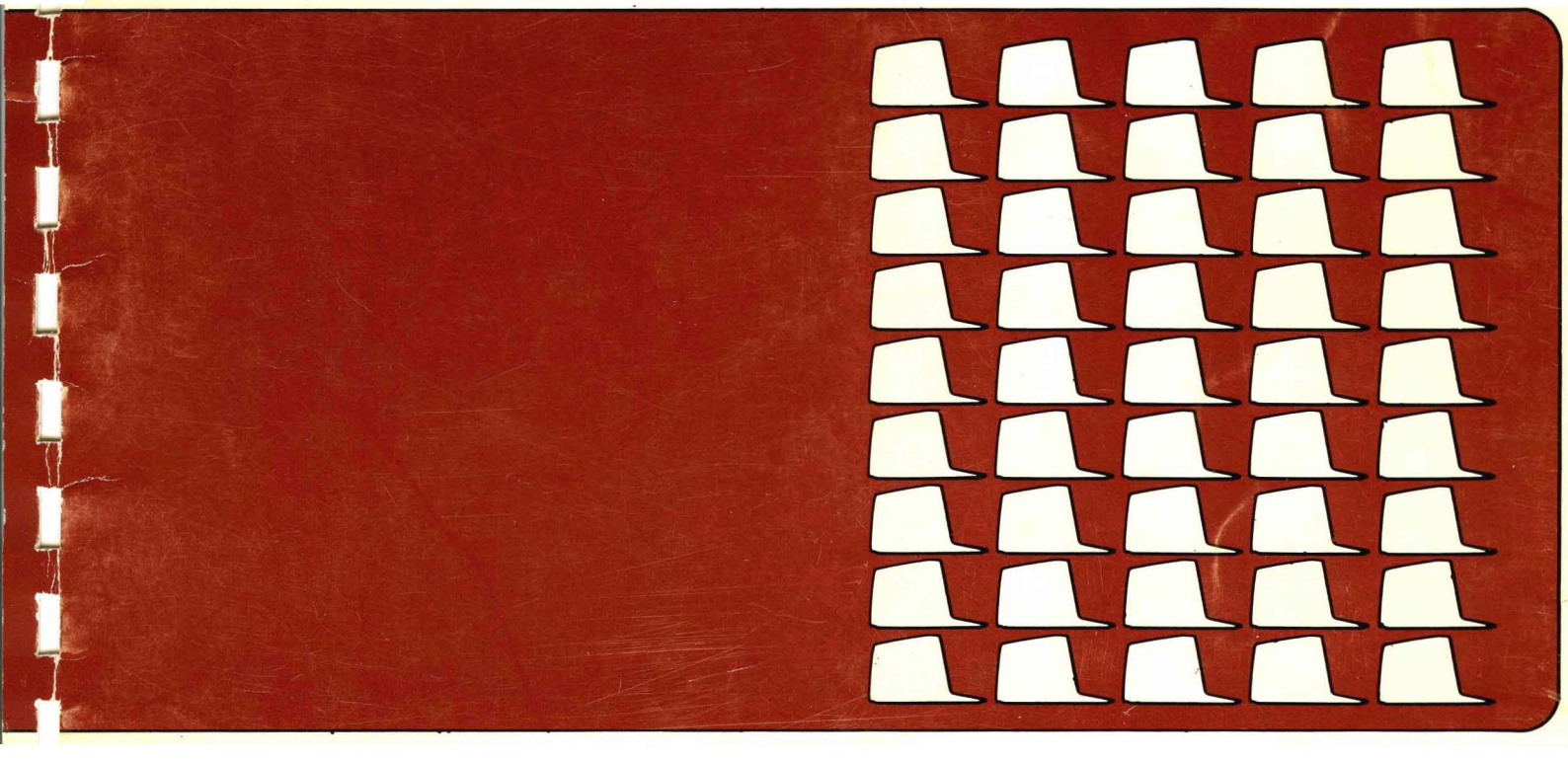
GTC

MAINTENANCE INSTRUCTIONS

MODEL GT400

General Terminal Corporation



PRICE $35.00

General Terminal Corporation

MAINTENANCE INSTRUCTIONS

MODEL GT400

This document is issued for information only. Specifications, data, and information may change after the date of printing. Latest specifications, data, and information are available upon request and will be the subject of subsequent releases issued from time to time.

ORDER NO. 05007 **FEB/1980**

TABLE OF CONTENTS

TABLE OF CONTENTS — Continued

LIST OF FIGURES

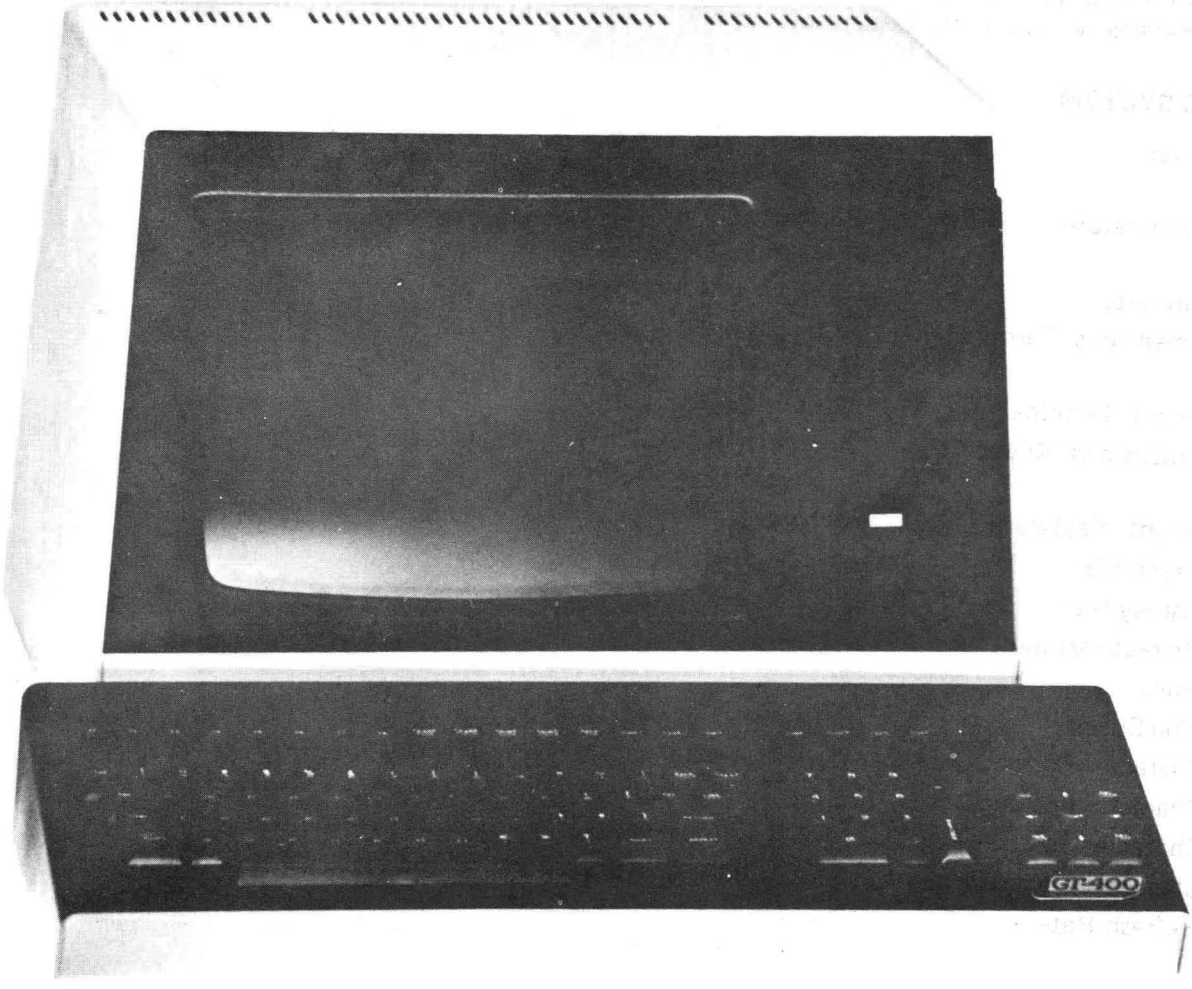


Figure 1 General Terminal Corporation Model 400

1. SPECIFICATIONS

The General Terminal Corporation 400 is a stand-alone alphanumeric display terminal for use in data entry and retrieval systems where a highly flexible interaction between man and machine is desired. The 400 utilizes micro-computer architecture to include as standard features; Full/Half Intensity, Reverse Video, Blink, Underscore, and Area Attributes.

1.1 BASIC SYSTEM

Power	Domestic: 120 watts, 105-130 volts; 60 Hz Export: 120 watts; 105-130, 210-260 volts; 50 Hz
Temperature	Operating: 5° to 40°C Storage: −30° to 70°C
Humidity	5% to 85% non-condensing
Dimensions, Terminal	13 inches high, 17 inches wide, 16 inches deep (33 cm X 43 cm X 41 cm)
Weight, Terminal	35 pounds (15.8 Kg)
Dimensions, Keyboard	3 inches high, 20 inches wide, 8 inches deep (7 cm X 51 cm X 20 cm)
Weight, Keyboard	10 pounds (4.4 Kg)
Screen Size	12 inch diagonal (30 cm)
Display Size	8-1/2 inches wide, 6 inches high (21 cm X 15 cm)
Characters/Line	80
Lines	25
Line Spacing	0.45 character height (11 mm)
Character Format	9 X 9 dot matrix
Character Spacing	0.4 character width
Character Size	0.08 X 0.19 inch nominal (2 mm X 5 mm)
Character Repertoire	64 ASCII Standard, 95 ASCII Optional
Refresh Rate	Domestic: 60 times a second Export: 50/60 times a second } ±0.5 Hz, Line Synchronized
Cursor	Non-destructive blinking underscore
Transmit Data	Character by character as entered by the keyboard, or block transmission.

1.2 STANDARD INTERFACE

The Asynchronous Serial Interface is a multi-purpose serial data interface which provides maximum flexibility in operator switch selectable data rates, and operation modes that can be applied to allow operation under a wide variety of serial data input and output situations. A panel at the rear of the display contains switches and connectors that allow the operator to match both the standard EIA RS232C voltage interface and the teletype-writer compatible 20/60 mA current loop interface for serial communications and computer interfaces.

The operator selectable functions include the following:

1. Sixteen data rates – 50, 75, 110, 134.5, 150, 200, 300, 600, 1,200, 1,800, 2,400, 3,600, 4,800, 7,200, 9,600, 19,200 bits per second
2. An external TTL-clock input
3. Local Copy
4. Ten or eleven bit code selection (one or two stop bits)
5. Odd, Even, Mark or Space Parity
6. Normal or strapped Request-to-Send
7. Normal or Reversed Video
8. 20 and 60 Ma teletypewriter compatible current loop interface
9. EIA RS 232 C Interface
10. Secondary Channel enable
11. Secondary Channel Inversion
12. Character Mode reset request-to-send on EOT or CR
13. Message Last Character of EOT or ETX
14. Area Last Character of EOT or ETX

GT400

BITS 4, 3, 2, 1	BITS 7, 6, 5 000	001	010	011	100	101	110	111
0000	NULL	DLE	SPACE	0	@	p		p
0001	SOH	DC1	!	1	A	Q	a	q
0010	STX	DC2	"	2	B	R	b	r
0011	ETX	DC3	#	3	C	S	c	s
0100	EOT	DC4	$	4	D	T	d	t
0101	ENQ	NAK	%	5	E	U	e	u
0110	ACK	SYN	&	6	F	V	f	v
0111	BELL	ETB	/	7	G	W	g	w
1000	BSP	CAN	(	8	H	X	h	x
1001	HZ. TAB	EM	)	9	I	Y	i	y
1010	LINE FEED	SUB	*	:	J	Z	j	z
1011	V.TAB	ESC	+	;	K	[	k	⦚
1100	ERASE SCRN	FS	,	<	L	\	l	⦚
1101	CARR. RET.	GS	–	=	M	]	m	⦚
1110	SO	RS	•	>	N	↑	n	~
1111	SI	US	/	?	O	←	o	RUB OUT

THE AREA ENCLOSED BY DASHED LINES REPRESENT LOWER CASE CODES WHICH ARE DISPLAYED AS UPPER CASE CHARACTERS WHEN THE LOWER CASE OPTION IS NOT INSTALLED.

Figure 2 ASCII Character Set

1.3 OPTIONS

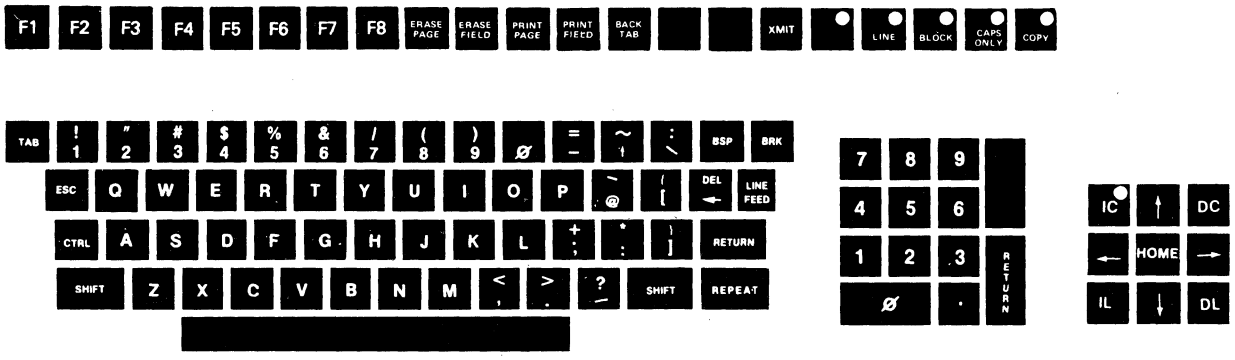
- Upper/Lower case keyboard with 8 Function keys, or Upper/Lower case keyboard with 24 Function keys
- Serial unbuffered Printer option
- Fully buffered Printer Interface
- Polling
- Synchronous Communications Interface
- National Character Sets
- Paging (2 or 3 pages)
- Time Sharing Option (TSO)
- Hazeltine 2000 Emulation (HZ2000)

2. OPERATING INSTRUCTIONS

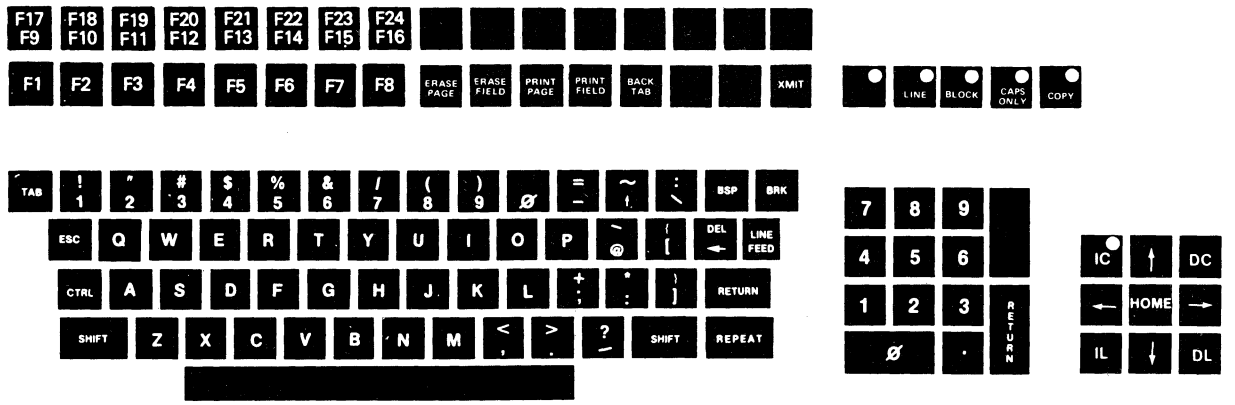
Before using your Model 400 terminal On Line, we suggest that this section be read and understood.

2.1 OPERATOR CONTROLS, FRONT

Operator controls and indicators which are located on the front of the terminal and on the keyboard assemblies are shown in Figure 3 and described below.



Model 400/4 STANDARD KEYBOARD WITH 8 FUNCTION KEYS



Model 400/5 OPTIONAL KEYBOARD WITH 24 FUNCTION KEYS

Figure 3 Model 400 Keyboard Layouts

- POWER — In the ON position, the terminal is in the operating state and an indicator contained within the switch is illuminated. In the OFF position, power is removed from the terminal. After the switch is turned ON, a 30 second warm-up period is required before operating the terminal.

- LINE/LOCAL – Selects either local or on line mode of operation. In LOCAL, data and control are provided by the keyboard. The unit is automatically configured in the LOCAL COPY mode and no data is transmitted to the interface. In ON LINE, data flow to and from the terminal is permitted. The integral LED is illuminated to indicate the ON LINE position.

2.2 KEYBOARD AND CODE SET

The 400 terminal is controlled by a 7-bit ASCII code set, Figure 2, generated by the two keyboards shown in Figure 3, or received over the data line.

The 64 ASCII codes from 040_8 through 137_8 are entered into memory when received from the data line or from the keyboard (Local Copy). With the exception of the space code (040_8); all of these codes result in the display of a character on the screen.

The 31 ASCII codes from 140_8 through 176_8 (lower case), are stored in memory when received and are displayed as upper case characters when the lower case option is not installed.

LINE FEED	LINE FEED - (from data line or from keyboard) – The LINE FEED command causes the cursor to move down one line.
RETURN	RETURN - (from data line or from keyboard) – The carriage RETURN key places the cursor at the beginning of the line, (left margin).
DEL	DELETE - (from keyboard) – The DELETE key causes a rubout code (all ones) to be transmitted, no cursor movements occur and no character enters memory. Rubout codes received from the data line are ignored.
REPT	REPEAT - (from keyboard) – The REPEAT key, when held down while any other key is depressed, causes that character or function to be repeated at a rate of 10 characters per second.
BRK	BREAK - (from keyboard) – Depressing the BREAK key forces a "space" condition on the data line as long as the key is depressed.
SHIFT	SHIFT - (from keyboard) – The SHIFT key enables keyboard generation of symbolic characters (!, &, etc.). Lower case alphabetic characters will be generated by this keyboard when CAPS LOCK is not enabled.
CTRL	CONTROL - (from keyboard) – Depression of the CONTROL key allows the control code to be generated by the keyboard.
ESC	ESCape - (from keyboard) – The ESCape key generates the ASCII code 023_8. It is used as an introducing character for special functions defined in Section 2.6.
F1	Function keys transmit the code sequence defined in Section 2.6. These codes have no effect when received by the terminal.

°BLOCK

The BLOCK key switches the terminal transmit mode between character by character transmission and block transmission.

°CAPS ONLY

CAPS ONLY prevents the keyboard from generating lower case alphabetic characters only. All other functions are normal including the use of the shift key. CAPS ONLY mode is indicated by the illumination of an LED.

TAB

The TAB key causes the cursor to advance, in Block Mode, to the beginning of the next unprotected field. If protected data is not present on the screen, the cursor will advance to the first position of the next line. When the terminal is on line in Character Mode and the TAB key is pressed a control I will be transmitted.

BACK TAB

In Block Mode the BACK TAB Key causes the cursor to back to the beginning of the previous unprotected field. If no protected data is present on the screen, the cursor will return to the beginning of the previous line. In Character Mode CSI Z will be transmitted. See Transmit Code, Section 2.6.

ERASE FIELD

In Block Mode the ERASE FIELD key will erase that portion of the field where the cursor is resident. If EF was used to modify the ERASE FIELD extent, then the entire field will be erased. If EF was not used, then only that portion from the cursor position to the end of the field will be erased. When protected data is not present on the screen, then that portion of the current line defined by EF will be erased. In Character Mode CSI N will be transmitted when the ERASE FIELD key is pressed. See Section 2.6.

ERASE PAGE

In Block Mode the ERASE PAGE Key will erase that portion of the screen specified by the ED function (Section 2.6). If ED was previously used, the ERASE PAGE will clear the entire screen, otherwise only the area from the cursor through the end of the screen will be erased. In Character Mode, CSI J will be transmitted when the ERASE PAGE Key is pressed.

BSP

In Block Mode the BSP key will backspace the cursor one position except when this would place the cursor in a protected area. In this event, the cursor will not be moved. In Character Mode the BSP key will transmit a control H.

XMIT

In Block Mode will either transmit the screen as defined by DAQ or if modified by SM, it will transmit a transmit header. In Character Mode pressing the XMIT key will result in transmission of the screen of data as above unless SM modified the XMIT function in which case CSI h will be sent. See Section 2.6.

IC°

In Block Mode the IC key enables the insert Character Mode. When a displayable character key is pressed, data to the right of the cursor position is moved to the right one position and the new character is inserted at the cursor position. The number of characters to the right and below the cursor which will be moved by Insert Character are determined by the SEM function (Section 2.6). Striking the IC key again disables the mode. In character Mode the IC key transmits CSI 4 h.

DC

In Block Mode the Delete Character key will erase the character at the cursor position and move the data to the right and below the cursor one position to the left. SEM (Section 2.6) again determines how many characters will move for this operation. In Character Mode the DC key transmits CSI P.

IL

In Block Mode the Insert Line key causes the data on the line specified by the cursor to move down one line. In addition, lines below the cursor also move down limited by the SEM function (Section 2.6). The last line of this area will be lost. In Character Mode, CSI L will be transmitted when the IL key is pressed.

DL

The Delete Line key has the opposite effect as the IL key including the limitations posed by the SEM function except that the data on the line which contains the cursor is lost. In Character Mode CSI M will be transmitted.

CURSOR KEYS

The following 5 cursor keys act to place the cursor in an incremental manner. Should this action place the cursor in a protected area, AUTOTAB will immediately move the cursor to the right and down to the first unprotected space encountered.

HOME

In Block Mode the HOME key places the cursor in the first position on the top line. In Character Mode the HOME key transmits CSI H.

↑

In Block Mode the ↑ key moves the cursor one line above its previous location. In Character Mode, the ↑ key transmits CSI A.

↓

In Block Mode the ↓ key moves the cursor one line below its previous location. In Character Mode this key transmits CSI B.

→

In Block Mode the → key moves the cursor one character to the right of its previous location. In Character Mode this key transmits CSI C.

←

In Block Mode the ← key moves the cursor one character to the left of its previous position. In Character Mode this key transmits CSI D.

The above 4 keys (↑, ↓, →, ←) will move beyond the edges of the screen, i.e., cursor right on the 80th position of the First line will place the cursor on the position of the Second line. In Character Mode cursor down on the bottom line will cause the screen to roll up one line leaving the cursor on the bottom line rather than placing the cursor on the top line as it would in Block Mode.

2.3 TV MONITOR CONTROLS

The two operator controls which affect the TV monitor presentation are located on the underside of the front left corner of the terminal assembly as shown in Figure 4.

2.3.1 Intensity

Allows adjustment of the brightness of the characters displayed.

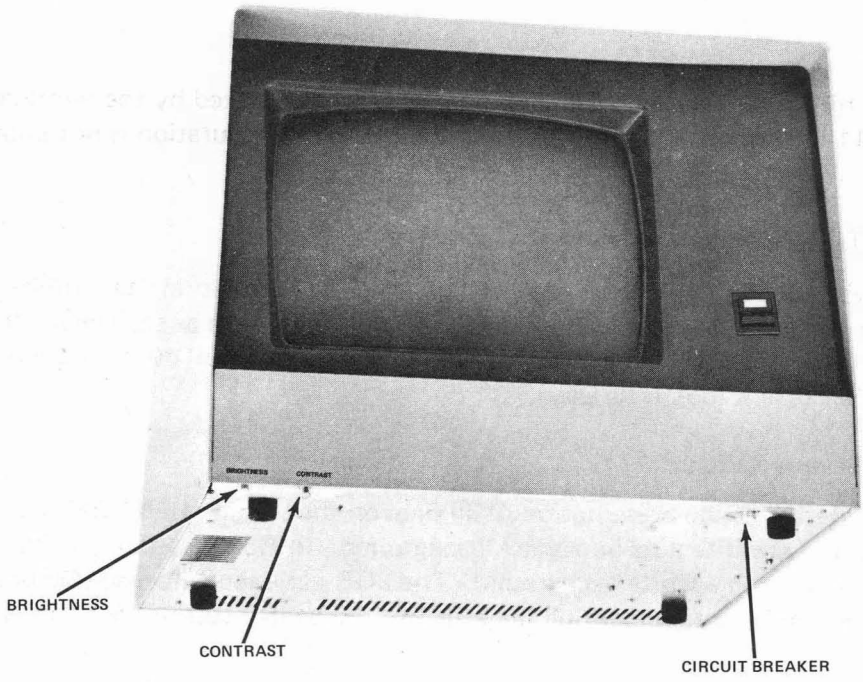


Figure 4 Model 400 TV Monitor Controls

2.3.2 Contrast

Allows adjustment of the contrast to provide image density control.

2.4 REAR PANEL CONTROLS

Interface controls, located on the rear of the terminal, provide for customer interface connection and determination of related functions (data rate, parity, etc.), for the serial asynchronous EIA or current loop interface.

2.4.1 Speed Select

These four switches select one of the sixteen asynchronous data rates from 50 to 19,200 baud.

2.4.2 Parity

The parity switches determine both the transmit and the receive parity. In the EVEN position, the transmit character parity bit is selected to make the number of marking bits in the character even. The switch also configures the receive parity checking logic to check for EVEN parity. In ODD parity the transmitter transmits ODD parity and the receiver checks for ODD character parity. In MARK parity the transmitter always sends a marking bit for parity and the receiver does not check for parity. In Space parity the transmitter always sends a spacing bit for parity and again the receiver does not check for parity.

2.4.3 Local Copy

The local copy switch when on routes transmitted data back to the receiver in addition to sending it to the CPU. In the off position the transmitted data will appear on the screen ONLY when the CPU echoes it back. The OFF POSITION should be used for Block Mode.

6.1 MNEMONICS LIST

Mnemonics	Definitions	PCB	Sheet	Schematic Location	PCB Chip Location
ABØ	ADDRESS BUS (TRI STATE)	CONT	4	C6	K4
AS2Ø	POLLING ADDRESS SWITCH 2 BIT Ø	CONT	4	A2	A2
BELL	RING BELL	CONT	4	A3	J5
BELLF	BELL FREQUENCY	CONT	7	A7	E10
BLANK	FIELD BLANK FUNCTION	CONT	3	B6	F6
BLINKF	BLINK FUNCTION	CONT	3	B6	F6
BMS	BUFFER MEMORY SELECT (SCRATCH PAD)	CONT	6	A3	H5
BR	BAUD RATE (ASYNCHRONOUS)	CONT	2	C3	J9
BRK	RECEIVED BREAK DETECTED	CONT	2	C1	H12
BRKS	BREAK SENSED	CONT	2	A8	J12
BUSAK	REQUESTING DEVICE NOW HAS μP BUS	CONT	4	D7	J7
BUSRQ	ADDRESS BUS REQ. FROM EXT. DEVICE	OPT	4	D8	J4
CAPLOCK	KBD CAPS LOCK KEY	KBD	2	C5	J2
CCOMP	CURSOR COMPARE	CONT	4	C2	C6
CD	CARRIER DETECT (TTL)	CONT	2	D6	L10
CLEAR TO SEND	EIA CLEAR TO SEND	CONT	2	C6	J1
CLOCK	12.012 MHz CLOCK	CONT	7	D7	A10
COMPB	COMPOSITE BLANKING	CONT	7	B6	E8
COPYE	LOCAL COPY SWITCH	CONT	2	B4	K9
CPLKEN	KBD CAPS LOCK ENABLE	CONT	2	C5	J2
CPLK LED	KBD CAPS LOCK LED	CONT	2	C5	J2
CP2	DOT TIME CLOCK	CONT	7	D6	A9
CT1	CURSOR BLINK TIME 1	CONT	7	A7	E10
CTS	CLEAR TO SEND (TTL)	CONT	2	C6	K12
CURUB	CURSOR UNDERBAR	CONT	3	C7	E6
DATA TERMINAL READY	EIA DATA TERM. READY	CONT	2	B6	L11
DATA SET READY	EIA DATA SET READY	CONT	2	C6	J1
DBØ	DATA BUS, BIDIRECTIONAL, TRISTATE	CONT	4	C6	M5
DCCD	DAISY CHAIN CARRIER DETECT	CONT	2	D6	K12
DCCTS	DAISY CHAIN CLEAR TO SEND	CONT	2	C6	K12
DCDSR	DAISY CHAIN DATA SET READY	CONT	2	C6	K12
DCDTR	DAISY CHAIN DATA TERM. READY	CONT	2	B6	J3
DCLKC	DOT CLOCK	CONT	7	C6	A12
DCRD	DAISY CHAIN EIA RECEIVED DATA	CONT	2	D6	K12
DCRTS	DAISY CHAIN REQUEST TO SEND	CONT	2	B6	J3
DCSCTS	DAISY CHAIN SEC. CLEAR TO SEND	CONT	2	A7	M12
DCSRC	DAISY CHAIN SYNC. REC. CLOCK	CONT	2	C7	M12
DCSRTS	DAISY CHAIN SEC. REQ. TO SEND	CONT	2	A6	J3
DCSXC	DAISY CHAIN SYNC. XMIT CLOCK	CONT	2	C7	M12
DCTXD	DAISY CHAIN XMIT DATA	CONT	2	B8	J3

2.4.4 Stop Bits

The 1/2 stop bit switch determines the number of bits transmitted by the terminal to be either 10 or 11 (1 stop bit, or 2 stop bits). If the correct configuration is not known select 2 stop bits.

2.4.5 Request-To-Send

The R-T-S switch allows the Request-to-Send signal generated within the terminal and used on the EIA interface to be permanently on (RTS ON) or to cycle as each character is transmitted (RTS Normal). RTS On position is used primarily on a full duplex network and when using the current loop interface.

2.4.6 Normal/Reversed Video

This switch determines the presentation of all data on the screen. In NORM position all characters appear as white dots on a black background. In REV position all characters appear as black dots on a white background. The SGR code sequence (see Section 2.6) alters this selection by complimenting the effect of this switch setting each time it is received.

2.4.7 Secondary Channel ON/OFF

This switch when on causes a transmitted BREAK to be sent on the secondary channel and causes the receiver to monitor the secondary channel for a received BREAK. When off BREAK information is communicated on the primary channel.

2.4.8 Secondary Channel NOR/INV

This switch determines the polarity of the BREAK signal when the secondary channel is used. In NOR position BREAK carries the same polarity as any other EIA control signal. In INV position BREAK has the same polarity as EIA data signals.

2.4.9 INT. CLK./EXT. CLK

This switch in the INT. CLK. position allows one of the sixteen data rates to be selected. In EXT. CLK. position the interface will operate at the data rate determined by the external TTL clock supplied. The external clock operates at 16 times the rate desired, and has a maximum data rate of 20,000 baud.

2.4.10 EOT/CR-EOT

This switch determines the point at which the Request-to-Send signal is reset while transmitting the character mode. The RTS signal will be reset after transmitting either the Carriage Return Code or the EOT Code typed, or only when the EOT code is typed.

2.4.11 EOT/ETX (Field)

This switch determines which character (EOT or ETX) will be transmitted at the end of a Field. If the switch is on, an EOT will be sent. This operation occurs only in Block Mode.

2.4.12 EOT/ETX (Page)

This switch determines which character (EOT or ETX) will be transmitted at the end of the Page. If the switch is on an EOT will be sent. This operation occurs only in Block Mode. When the end of a field and the end of a page coincide, only one EOT or ETX will be sent and it is determined by this switch.

2.4.13 EIA

The molex connector (Figure 7) provides the I/O termination for use with a General Terminal Corporation supplied optional cable. The cable is designed to be attached to a modem, however it may be used directly with a computer modem interface. The 400 EIA interface specifications comply with EIA RS 232C and CCITT V24 standards.

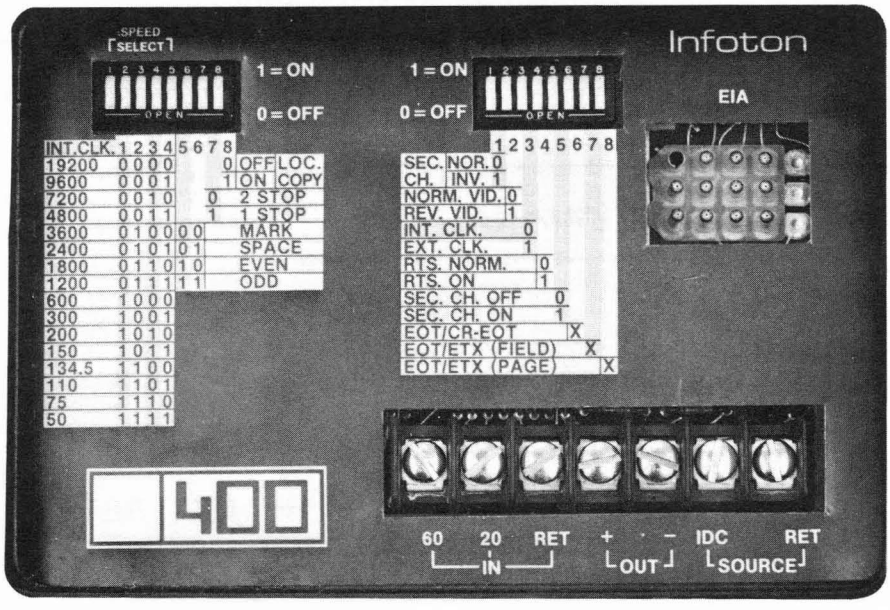


Figure 5 Rear Panel Controls

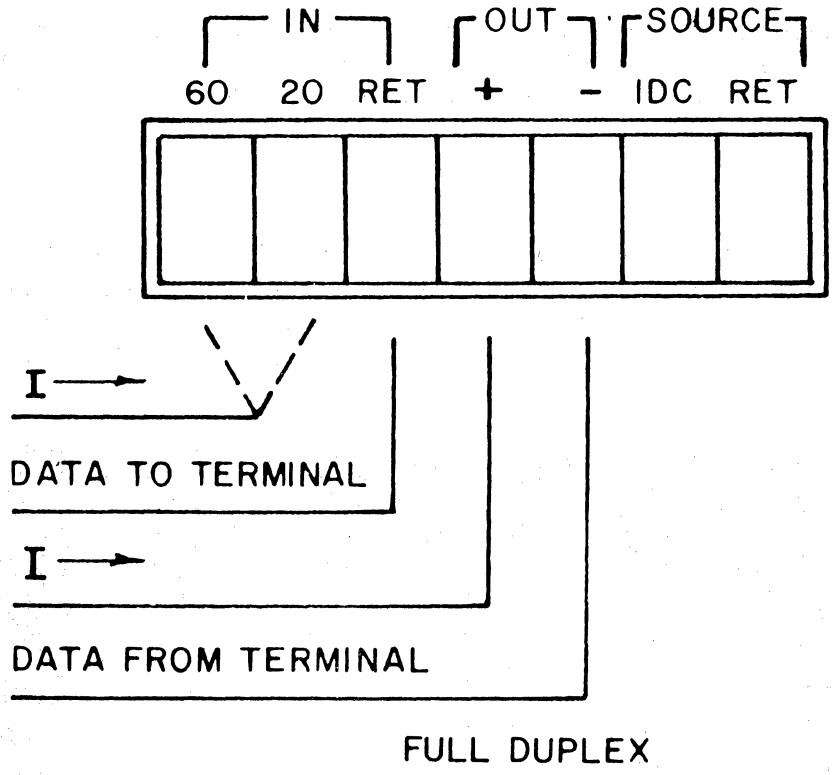
2.4.14 Current Loop Terminal Strip

A 7 pin barrier terminal strip is provided to interconnect with the current loop interface. Either Full or Half Duplex operation may be used at either 20 or 60 Ma. The source of the current is external to the 400. Figure 6 illustrates both Full and Half Duplex connections.

2.5 INITIAL SETUP

At the start of any operating period, we recommend that you follow these procedures before turning the terminal on line.

- Set the LINE/LOCAL switch to LOCAL, POWER switch to ON. The Power switch will then illuminate and approximately 30 seconds later a blinking cursor will appear on the screen.



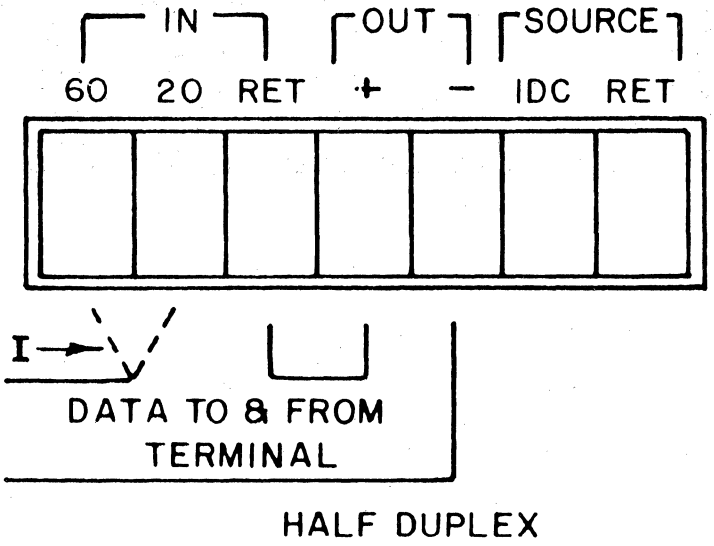


Figure 6 Model 400 Current Loop Connection

EIA RS-232C Name	CCITT V-24 Name	Description	Printer EIA Pin No.*	Modem EIA Pin No.**	MOLEX Pin No.	Comments
BA	103	Data transmitted from terminal	–	2	1	Logical "1" = OFF = –12V Logical "0" = ON = +12V 300-ohm source impedance.
CA	105	Request to send signal from terminal	–	4	2	Goes high (+12V) when the terminal is ready to transmit.
CB	106	Clear to send signal to terminal	–	5	3	Must be high to allow terminal to send; is supplied by a modem.
BB	104	Data transmitted to terminal	–	3	4	Logical "1" = OFF = –5V to –25V Logical "0" = ON = +5V to +25V 6.8K ohm load impedance
CF	109	Carrier present signal to terminal	–	8	5	Must be high to allow terminal to receive; is supplied by a modem.
CD	108.2	Data terminal ready signal from terminal	–	20	8	Goes high (+12V) when terminal is on LINE; is low when terminal is in LOCAL mode.
		External clock input at TTL logic level	–	–	10	For use with RECEIVE RATE selector switch in EXT position.
AB	102	Signal ground	7	7	12	
CC	107	Data set ready	–	6	7	Must be high to allow terminal to operate; is supplied by a modem.
SCF	122	Secondary channel Carrier Present		12	6	Received Break when Secondary Channel is enabled.
SCA	120	Secondary Channel Request to Send		19	9	Transmitted Break when Secondary Channel is enabled.
BB*	104	Data to printer	3	–	11	Copy Mode Output (Print Data)
CB*	106	Clear to send	5	–	–	These signals are connected to the printer's data terminal ready signal.
CC*	107	Data set ready	6	–	–	
CF*	109	Carrier present	8	–	–	
CD*	108.2	Data terminal ready	20	–	–	

*Optional Cable assembly 03157-G02

**Optional Cable assembly 00692-G02

Figure 7 EIA RS-232 Signals and Connector Pins

- Check front and rear panel switches for proper position (data rate, parity, etc.).
- Type a message and see that it is correctly written on the screen. Exercise all functional keys to insure correct operation.
- Adjust INTENSITY and CONTRAST controls for your viewing comfort.

2.6 SPECIAL FUNCTION CODES

2.6.1 CRT Functions on Receive of Control Sequences

The following code sequences make use of the following multicode mnemonics.

APC =	ESC ←	APPLICATIONS PROGRAM COMMAND
CSI =	ESC [	CONTROL SEQUENCE INTRODUCER
DCS =	ESC P	DEVICE CONTROL STRING
ST =	ESC \	STRING TERMINATOR
Pn =		NUMERIC VALUE FROM COLUMN 3 (Ø THROUGH ?) WHEN NOT USED, DEFAULT VALUE OF Ø IS USED WHERE Ø ≡ 1
Ps =		NUMERIC VALUE FROM COLUMN 3 (Ø THROUGH ?) WHEN NOT USED, DEFAULT VALUE OF Ø IS USED

NOTE: SPACES SHOWN ARE FOR CLARITY ONLY – THE SEQUENCE DOES NOT CONTAIN SPACE CODES.

Cursor Controls

CUP	HOME	CSI H	
CUU	CURSOR UP	CSI Pn A	UP Pn LINES
CUD	CURSOR DOWN	CSI Pn B	DOWN Pn LINES
CUF	CURSOR RIGHT	CSI Pn C	RIGHT Pn SPACES
CUB	CURSOR LEFT	CSI Pn D	LEFT Pn SPACES
BS	BACK SPACE	CONTROL H	LEFT ONE SPACE
CNL	CURSOR NEW LINE	CSI Pn E	TO LEFT MARGIN DOWN Pn LINES
CPL	CURSOR PREVIOUS NEW LINE	CSI Pn F	TO LEFT MARGIN UP Pn LINES
CR	CARRIAGE RETURN	CONTROL M	TO LEFT MARGIN CURRENT LINE
LF	LINE FEED	CONTROL J	DOWN ONE LINE OR DOWN ONE LINE AND TO LEFT MARGIN (SEE SET MODE)
CUP	DIRECT CURSOR ADDRESS (CURRENT PAGE)	CSI Y;XH	WHERE Y IS IN THE RANGE OF 1 TO 24 LINES X IS IN THE RANGE OF 1 TO 80 CHARACTERS
	DIRECT CURSOR ADDRESS (MULTI-PAGE UNIT)	CSI Y;Xf	WHERE Y IS IN THE RANGE OF 1 TO 50 OR 75 X IS IN THE RANGE OF 1 TO 80 CHARACTERS
	SCROLL UP	CSI Pn S	
	SCROLL DOWN (MULTI-PAGE UNITS)	CSI Pn T	
	NEXT PAGE (MULTI-PAGE UNITS)	CSI Pn U	
	PREVIOUS PAGE (MULTI-PAGE UNITS)	CSI Pn V	

Tab

CHT	HORIZONTAL TAB	CSI Pn I	FORWARD TAB Pn TAB STOPS
HT	HORIZONTAL TAB	CONTROL I	FORWARD TAB ONE FIELD OR LINE
CT	COLUMNAR TAB	ESC I	SET COLUMNAR TAB STOP (10 MAXIMUM)
CBT	BACK TAB	CSI Pn Z	BACK TAB Pn FIELDS OR LINES
RCT	RESET COLUMNAR TABS	CSI 3 g	RESETS ALL COLUMNAR TAB STOPS

NOTE: IF PROTECTED DATA IS NOT PRESENT, TAB FUNCTIONS ARE PERFORMED ON A LINE BASIS.

Erase Functions

EF	ERASE FIELD OR LINE	CSI Ps N	Ps = Ø ERASE FROM CURSOR TO END Ps = 2 ERASE ENTIRE FIELD OR LINE
ED	ERASE SCREEN	CONTROL L OR CSI Ps J	Ps = Ø ERASE FROM CURSOR TO END Ps = 2 ERASE ENTIRE SCREEN

NOTE: SEE SET MODE/RESET MODE FOR MODIFICATION TO ABOVE. IF SET MODE ERASE PROTECTED DATA PRECEDES THE ABOVE PROTECTED DATA WILL BE ERASED.

Edit

	INSERT CHARACTER MODE		SEE SET MODE
DCH	DELETE CHARACTER	CSI Pn P	DELETE Pn CHARACTERS
DL	DELETE LINE	CSI Pn M	DELETE Pn LINES
IL	INSERT LINE	CSI Pn L	INSERT Pn LINES

NOTE: THE END OF THE AREA AFFECTED BY THE ABOVE EDIT FUNCTIONS IS DETERMINED BY SET EDIT EXTENT.

SEM	SET EDIT EXTENT	CSI Ps Q	Ps = Ø EDIT IN PAGE Ps = 2 EDIT IN FIELD OR LINE

Display

SGR	SELECT GRAPHIC MODE	CSI Ps m	Ps = Ø NORMAL Ps = 4 UNDERLINE Ps = 5 BLINK Ps = 7 REVERSE THE MEANING OF THE REVERSE VIDEO SWITCH Ps = 8 SECURITY FIELD (NOT DISPLAYED)

Display (Continued)

DAQ	DEFINE AREA QUALITIES (DAQ will reset any SGR values previously set at the cursor location)	CSI Ps o	Ps = Ø NORMAL Ps = 1 NON-TRANSMITTED PROTECT Ps = 3 NUMERIC ONLY Ps = 8 TRANSMITTABLE PROTECT

Mode Control

The set mode sequence (CSI Ps h) selects the following modes and the reset sequence (CSI Ps) resets the mode.

Ps = 2	LOCK THE KEYBOARD AND DISABLE AUTO TAB
Ps = 3	ENTER CONTROL REPRESENTATION MODE (RESET REQUIRES ESC CSI 3)
Ps = 4	INSERT REPLACE MODE
Ps = 5	STATUS REPORTING MODE
Ps = 6	MODIFY ERASE FUNCTION TO ERASE PROTECTED DATA (ERASURE MODE)
Ps = 12	CHARACTER MODE
Ps = 15	MULTIPLE AREA TRANSMIT MODE
Ps = 16	TRANSMIT TERMINATION MODE
Ps = 17	SELECTED AREA TRANSMIT* MODE
Ps = 19	EDIT IN MEMORY (PAGED UNITS ONLY)
Ps = 20	NEW LINE MODE
Ps =	CARRIAGE RETURN (CR) NEW LINE MODE
Ps = =	XMIT REQUEST MODE
Ps =	PRINT COPY MODE
Ps = ?	TEXT EDIT MODE. When a Carriage Return code is received in TEXT EDIT MODE it is stored in memory, performed, and the remainder of line is erased. If Insert Character is then performed data is shifted to the right until the CR code reached position 80 when data on subsequent lines will be shifted.

*To reset all selected field bits CSI p is required.

Transmit Control

DSR	DEFINE STATUS REQUEST	CSI Ps n	Ps = 5 SEND DEVICE STATUS Ps = 6 SEND CURSOR ADDRESS

FOR XMIT FORMATS SEE TRANSMIT SEQUENCES

STOP TRANSMITTER	CONTROL S
RESTART TRANSMITTER	CONTROL Q

2.6.2 Transmit Sequences

The following functions are transmitted in block or character mode.

KEY OR FUNCTION	SEQUENCES
F1	APC A ST EOT
F2	APC B ST EOT
.	
.	
.	
F24	APC X ST EOT
CURSOR LOCATION	CSI Y;XR
XMIT STATUS	DCS Pa ; Pb ST EOT
Pa = Ø NORMAL	Pb = Ø PRINTER AND TERMINAL NOT BUSY
2 PRINTER ERROR	1 CRT BUSY
	2 PRINTER BUSY
	3 CRT AND PRINTER BUSY
	8 COMMUNICATIONS ERROR

Block Mode Only

KEY OR FUNCTION	SEQUENCE
REQUEST XMIT	APC Z ST EOT (RECEIPT OF ESC S EOT WILL START THE TRANSMITTER)

Character Mode Only

KEY OR FUNCTION	SEQUENCE	REMARKS
ALPHAS	ASCII ALPHA CODE	
NUMERICS	ASCII NUMERIC CODE	
PUNCTUATION & SYMBOLS	ASCII CODE	
RETURN	CONTROL M	
LINE FEED	CONTROL J	
ESC	CONTROL [	
BACKSPACE	CONTROL H	
TAB	CONTROL I	
BACK TAB	CSI Z	
ERASE PAGE	CSI J	
ERASE FIELD	CSI N	
INS CHAR	CSI 4 h	
INS LINE	CSI L	
DEL CHAR	CSI P	
DEL LINE	CSI M	
HOME	CSI H	
↑	CSI A	
↓	CSI B	
→	CSI C	
←	CSI D	
XMIT	CSI > h or XMIT	CSI > h IF SET MODE ENABLED REQUEST XMIT. IF NOT, THE SCREEN OF DATA WILL BE TRANSMITTED.
BLOCK	CSI 12ℓ	

Printer Option Commands

PRINT PAGE	CSI r
PRINT FIELD	CSI q
FILL PRINT BUFFER	CSI P P ESC\DATA EOT

2.7 POLLING OPTION

Address Definition

The device address may take three forms; single address character, repeated single character address, or two character address. In all cases the address character(s) must range in value between 21_{16} to $7E_{16}$ (041_8 to 176_8) (1 to ~). Address 20_{16} (040_8) (SPACE) is reserved for BROADCAST POLL. All terminals on the same data line must use the same address form (single, repeated single, or two character address).

The switch bank located at A2 is used to set the first character address (7 bits, switch 1 is LSB) and to determine the number of address characters (switch 8 on for repeated single character address, switch 8 off for one or two character address). The switch bank located at A3 is used for the second address character. If A3 is set to all ones or all zeros single character address is implied.

Switch bank A2 can also be used as a test function by setting its switches to all ones or all zeros. This places the terminal in a monitor mode where it will receive and display all messages independent of address. In this mode the terminal will not transmit nor will it respond to any polls.

NOTE: Each time any address switch is changed the line/local switch must be cycled from line to local and back to line.

Broadcast Poll

If the host substitutes a space code (20_{16}, 040_8) for an address character then the terminals described below will receive the message but will not respond to the poll. On single address terminals and on repeated single address terminals (if the host sends two spaces) the broadcast text will be received and displayed. On terminals using two character address all will receive and display the broadcast text provided the host uses two space characters for address. If the host substitutes only one character with a space code then only some of the terminals will receive the data as described in the following example.

HOST ADDRESS CHARACTERS	RECEIVING TERMINAL
SPACE A	ALL TERMINALS WHICH USE A AS THE SECOND ADDRESS CHARACTER
A SPACE	ALL TERMINALS WHICH USE A AS THE FIRST ADDRESS CHARACTER
SPACE SPACE	ALL TERMINALS WHICH USE TWO CHARACTER ADDRESS

Polling Address with Printer Option

When the printer option is installed in a polled terminal an additional address character can be appended, following normal address character(s), to allow data to be directed to the CRT only, the PRINTER only, or to both. If the appended character is 1 (31_{16} or 061_8) or not present the data will be received by the CRT only. If the character is 2 then the PRINTER only receives the data. If the character is 3 then both the CRT and the PRINTER will receive the data.

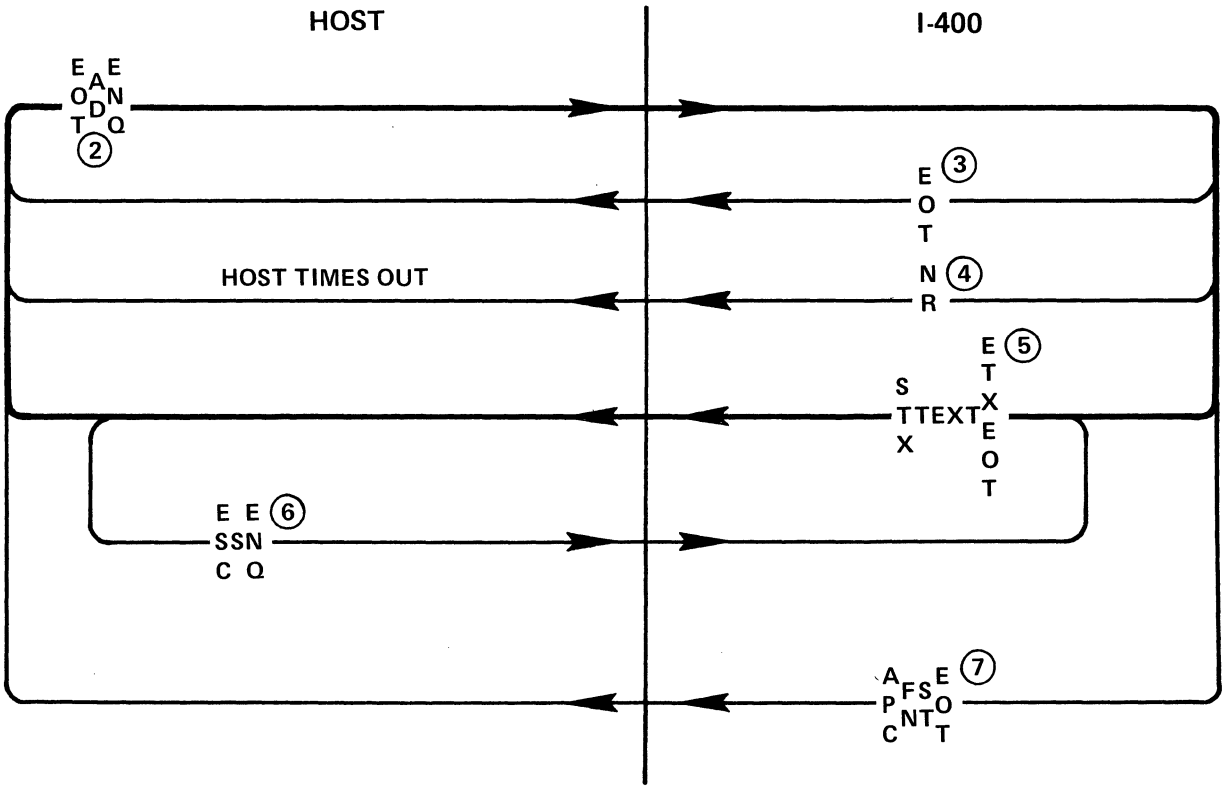


Figure 8 Poll Sequence ①

1. Assumes single text block and TRM reset
2. See Section 2.7 for address definitions
3. If nothing to transmit
4. Illegal Parameter, Parity Error in Poll or terminal not on-line
5. ETX or EOT depends upon setting of I-400 rear panel switches
6. Error recovery path
7. APC key (function key) struck

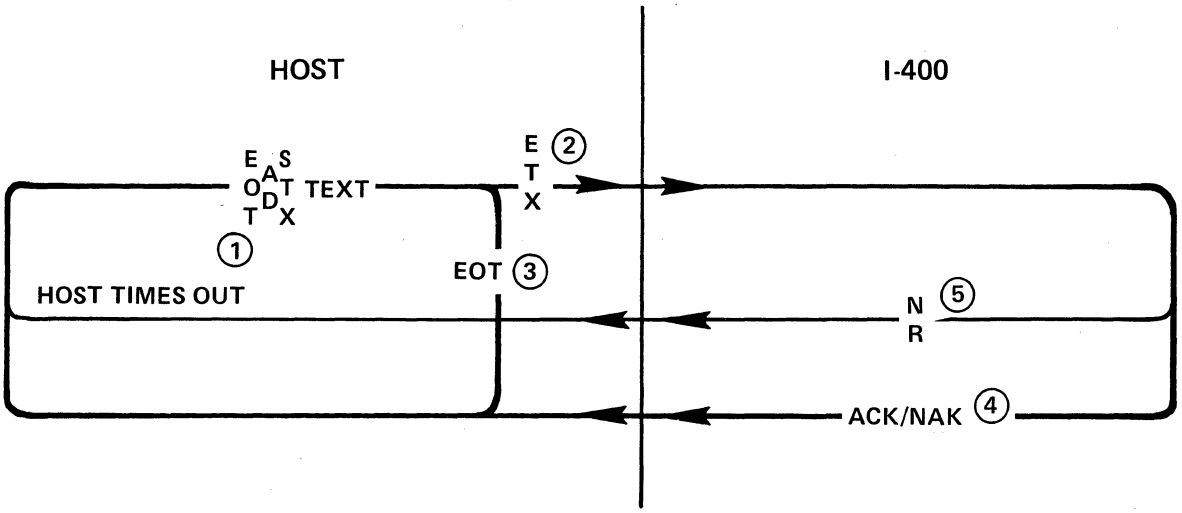


Figure 9 Fast Select Sequence

1. See Section 2.7 for address definitions.
2. End with ETX if ACK/NAK reply wanted. If status or cursor position report wanted, then end with ENQ.
3. End with EOT if no reply wanted.
4. The link is not broken after reply is sent. To resend data or xmit new data, simply xmit an STX followed by an ETX (or an EOT if reply to last block of data is not wanted).
5. No response if Broadcast. If reply expected, Error in addressing, missed ETX due to error or terminal not on-line.

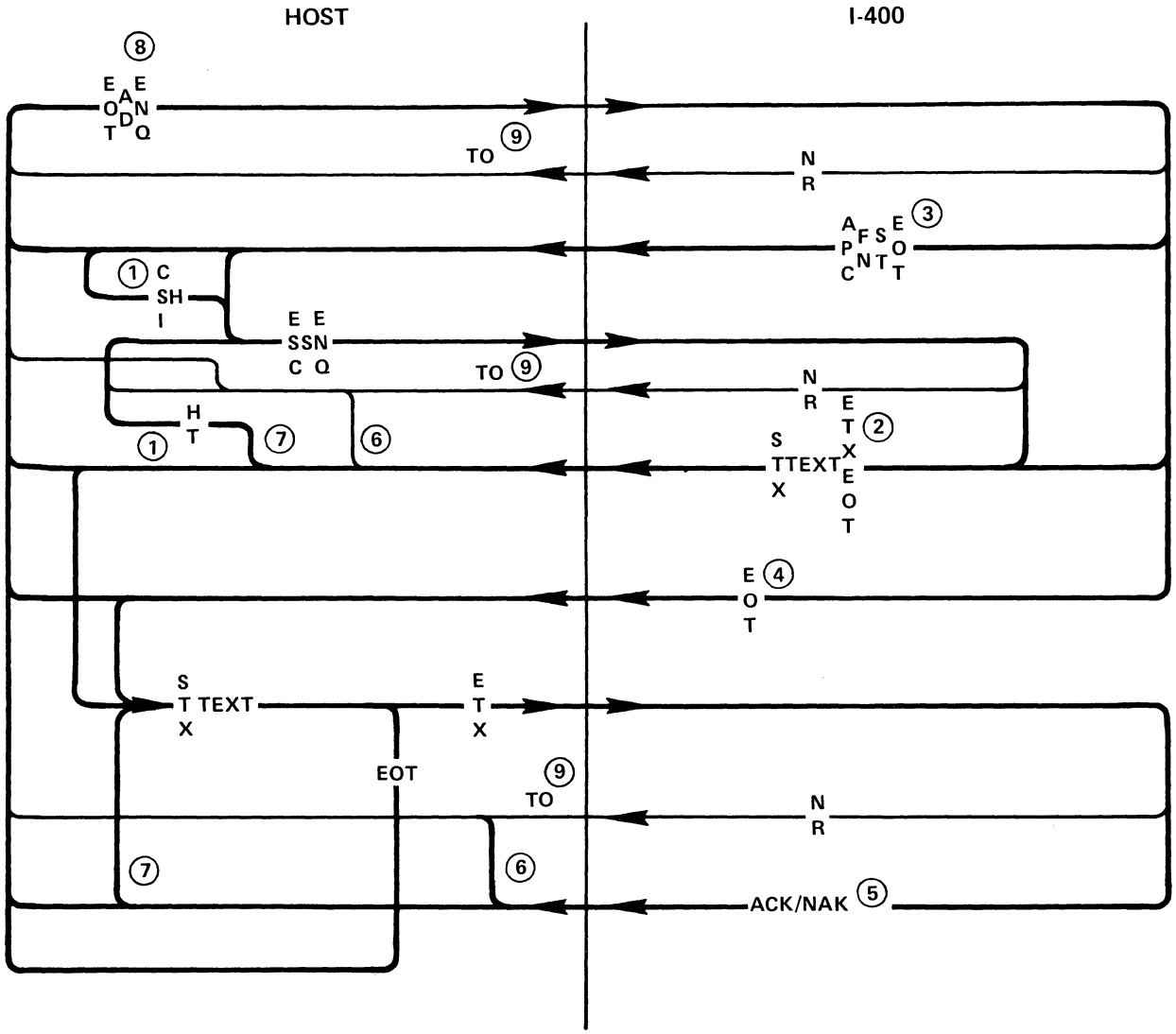


Figure 10 Poll-Select Sequence

1. Can be any cursor positioning sequence
2. ETX or EOT determined by switch setting
3. APC key struck or if TRM set and XMIT key struck Fn = z
4. If nothing to transmit
5. See Note 4 on Fast Select Sequence Page
6. Error recovery path
7. Multiple text block path
8. See Section 2.7 for address definition
9. Host system times out

3. THEORY OF OPERATION

As an aid in maintenance of your Model 400 this section is provided to give the reader a basic feel for how their terminal functions. It is only intended as an aid in location of a problem to the subassembly level. Repair of subassemblies is not covered in this manual. This section is broken up into three parts; Keyboard Electronics, Logic Board Assembly, and TV Monitor.

The physical configuration consists of three major groups:

- TV Monitor
- Keyboard Switch Assembly
- Logic Board Assembly (Figures 12 and 13)
  1. Micro Processor
  2. Memory
  3. Video Logic
  4. EIA Drivers and Receivers
  5. Current Loop Drivers and Receivers

3.1 KEYBOARD ASSEMBLY

The keyboard assembly uses a fully encoded Capacitive Scan technique. Eight bit ASCII codes are created with each key stroke without the use of switch contacts of any kind. Rollover features are incorporated which allow proper generation of codes as keys are struck even though one or more other keys are held depressed. Documentation on the keyboard will be found in the appendix.

3.2 CONTROL LOGIC PRINTED CIRCUIT ASSEMBLY (Figures 12 and 13)

The Control Logic PCB contains most of the components comprising the terminal.

3.2.1 Power Supply Portion

The Model 400 power supplies are contained on the Control Logic PCB and consist of four +5V supplies, a +12V supply, a −12V supply, and a +15V supply. Each supply except for the +15V supply has been implemented using 3 pin monolithic regulators. The +15V supply uses a conventional pass transistor in addition to the 3 pin monolithic regulator in order to provide sufficient power for the separate sync. TV monitor. Figure 13 indicates the test points for each supply output.

3.2.2 Interface Electronics Portion

The interface electronics provides a 20/60 mA teletypewriter compatible current loop interface and an EIA RS232C compatible interface. Both operate in an asynchronous serial mode. EIA RS232C connector pin assignments and signal levels are defined in Figure 7. Both full and half duplex modes of operation are available. In addition, Mark, Space, Even, or Odd parity, the eighth bit, can be selected by the operator. Data rates are operator selectable. Eleven or ten bit code length at all data rates is also switch selectable.

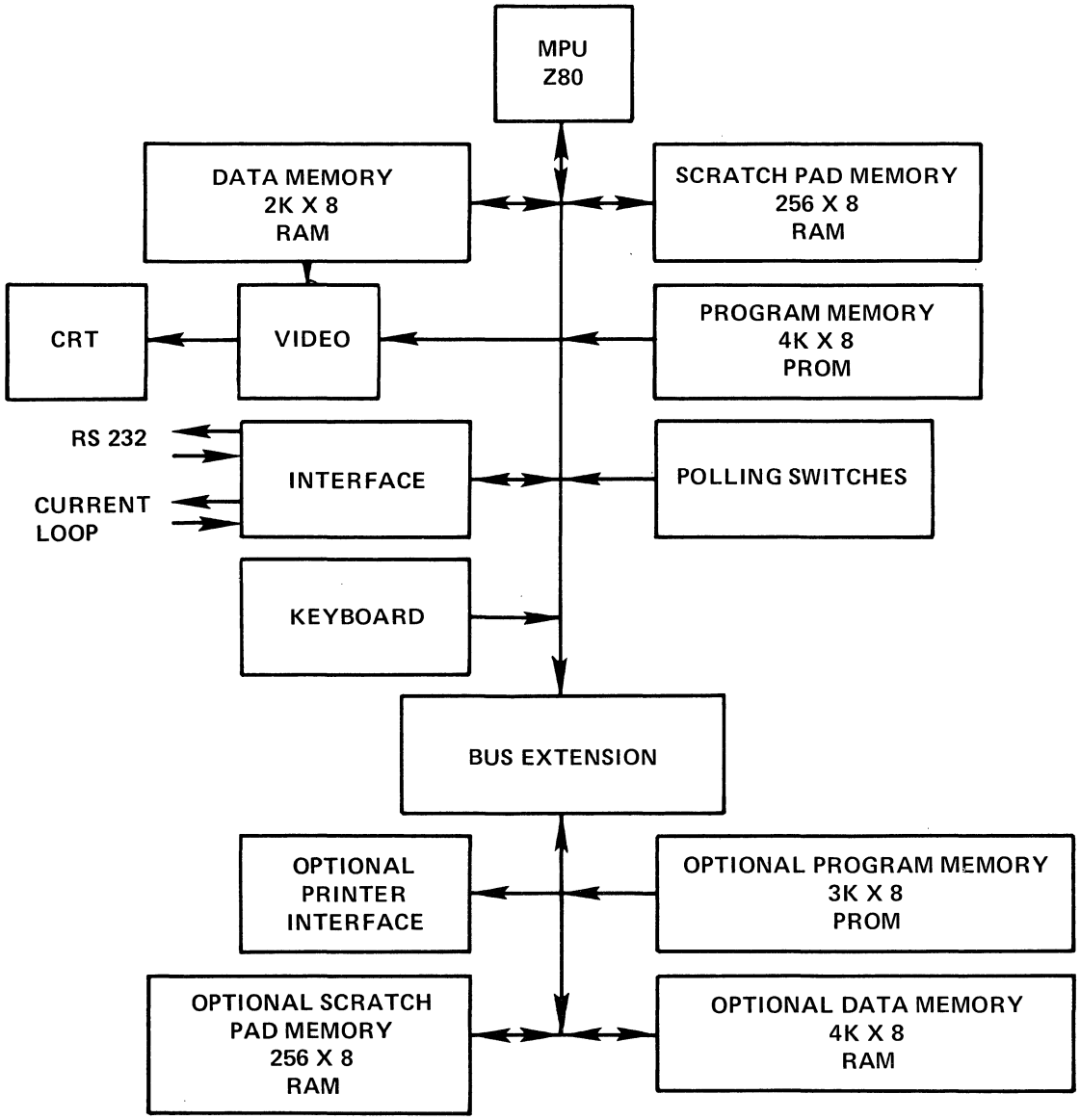


Figure 11 Display Block Diagram

The asynchronous serial interface consists of a transmitter (parallel to serial converter) and a receiver (serial to parallel converter), (see Figure 14). Parallel data generated by the keyboard is converted by the transmitter to a serial bit stream. The bit stream is appended with a start bit, parity bit, and either one or two stop bits (10 or 11 unit code) prior to presentation at the transmit output.

Serial data at the receive input is stripped of start and stop bits, after which the parity bit is checked against the character parity and the status of the parity selection switch. The receiver converts the seven bit serial code to parallel, and forwards the character to memory.

Schematic diagrams of the I/O electronics and keyboard electronics are contained in the Appendix.

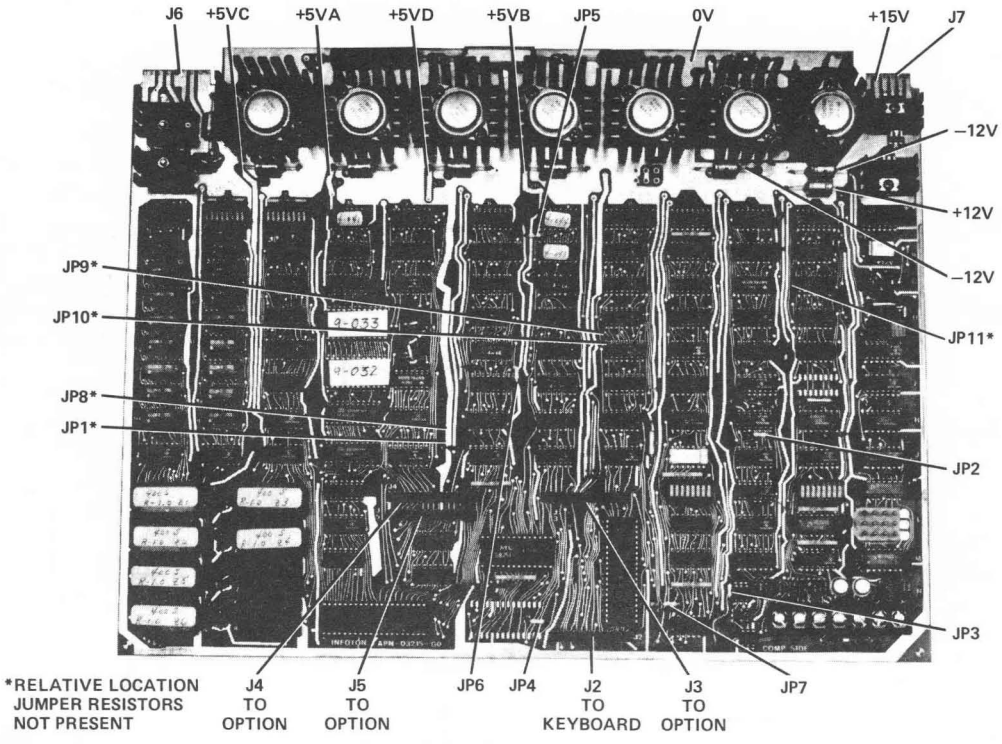


Figure 12 Control Logic PCB

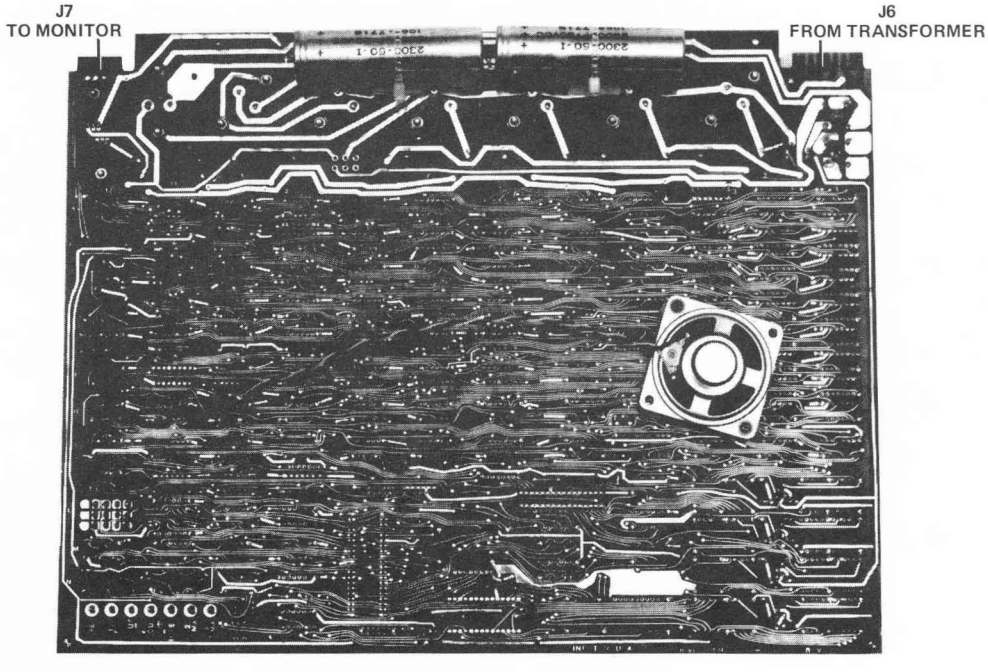


Figure 13 Power Supply Test Points

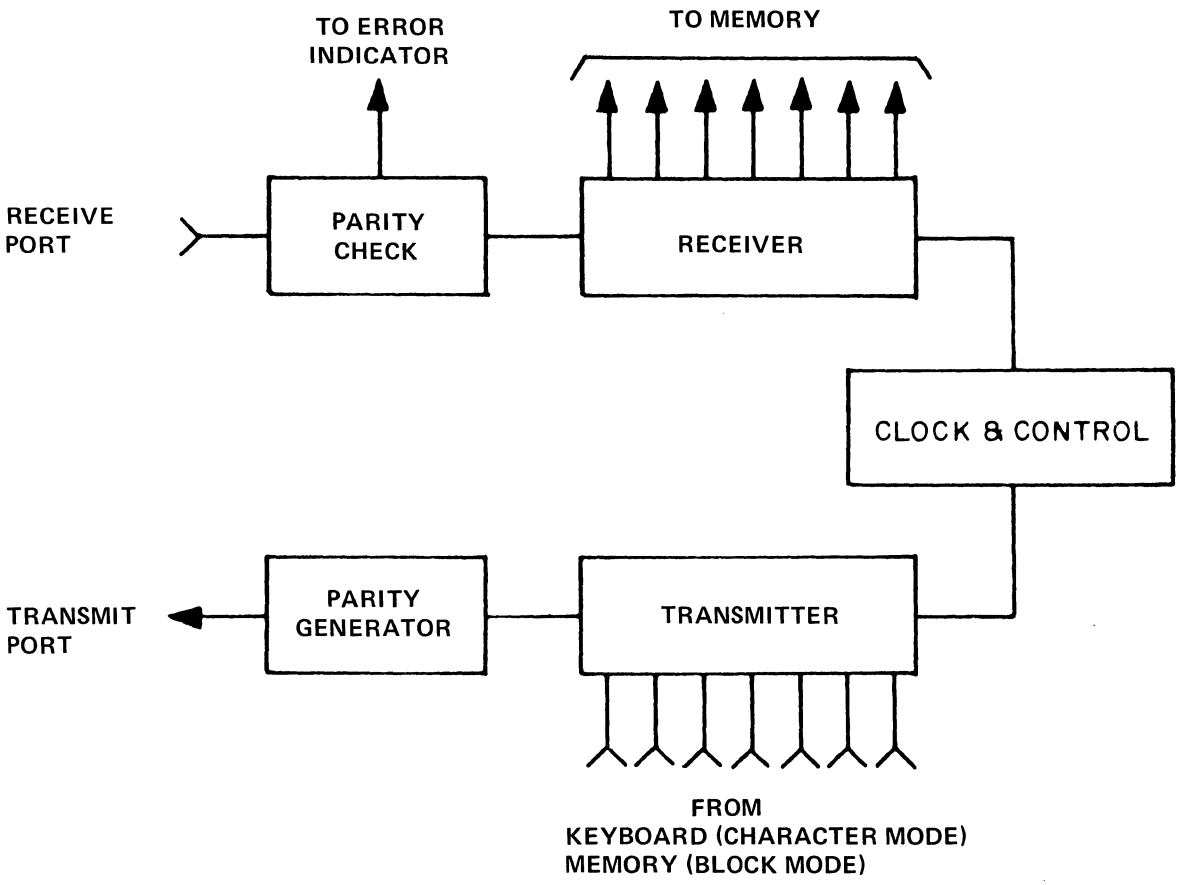


Figure 14 Serial Interface Block Diagram

3.2.3 Timing and Control Electronics

The timing and control logic provides complete timing for the display. The basic clock (24.024 MHz crystal oscillator) is used to provide the character dots to the video monitor. A divide by fourteen counter converts the basic clock to character clock. This clock is divided by 106 to form the character time (106 characters per line). The character is then divided by 10 for 10 slices per character line. Last in the chain is a divide by 25 for 25 lines per screen. The character and line portions are used as memory address while refreshing the screen. In addition, other timing signals are derived from the basic clock to drive the read only memory (ROM) timing, vertical and horizontal sync for the monitor, and form the data rates used in the serial interface.

3.2.4 Memory

Memory in the standard Model 400 terminal consists of Program Memory (PROM), Data Memory (RAM), and Scratch Pad Memory (RAM). Optionally, these memories may be expanded individually through the use of an option board, see Figure 11. In all cases these memory elements are attached to the microprocessor's bus and are addressed by the microprocessor. Figure 15 illustrates the address assignments for each of these elements.

ITEM	HEX ADDRESS	OCTAL ADDRESS	DECIMAL ADDRESS
Program Memory	0 to 0FFF	0 to 7777	0 to 4095
Scratch Pad Memory	3200 to 32FF	31,000 to 31,400	12,800 to 13,055
RAM*	3800 to 3FFF	34,000 to 37,777	14,366 to 16,383
*Portion used for Display Memory	3830 to 3FFF	34,060 to 37,777	14,384 to 16,383
Optional Data Memory	4000 to 4FFF	40,000 to 47,777	16,384 to 20,479
Opticnal Program Memory	5000 to 5BFF	50,000 to 50,600	20,480 to 23,551
Optional Scratch Pad	5F00 to 5FFF	57,234 to 57,634	24,320 to 24,575

Figure 15 Memory Addressing

3.2.5 Microprocessor

The microprocessor used to control all operations of the terminal is implemented using the Z80 CPU chip, the PIO (Parallel Input-Output) chip, and the CTC (Counter Timer) chip. Functional descriptions including specifications and the instruction set is included in the Appendix.

3.2.6 Video Logic

The line counter and the character counter from the Main timing chain provide alternate addressing to the display memory RAM. Video access to the display memory is allowed at all times except when the microprocessor updates the display memory.

Data is retrieved from memory for display, character by character at the video rate. The low order 5 bits from memory address the character generator PROMS. Bits 5 and 6 are decoded to enable either the upper case or the lower case character generator.

Field attribute characters (bit 7 = 1) are fully decoded to enable Half Intensity, Blink, Reverse Video, Underscore, and Blanking (Security Fields).

The output of the character generator PROMS consist of 5 dots and a control bit. The dots are presented to a serial shift register while the control bit is used to determine the shift mode of the shift register. If the control bit is a zero the dots associated with it are shifted out to the monitor ½ bit time earlier causing the presentation of those dots to be shifted to the left of their normal position. The presentation is thereby enhanced and produces effectively a 9 X 9 Matrix rather than a 5 X 9 Matrix.

3.3 AUXILIARY DEVICES

The Model 400 is equipped with an Infotone which sounds an audible tone when a bell code is received.

3.4 VIDEO MONITOR

The separate sync video signals generated on the control PCB are channeled to the video monitor. Detailed information on the video monitor is contained in the monitor manufacturer's maintenance manual.

3.5 PRINTER COPY MODE OUTPUT

Through the use of the optional EIA Cable Assy. PN 03157-G01 an EIA output is provided for printer operation. In Line Mode, Local Copy OFF, and Character Mode, receive data is sent to the printer at EIA levels and at the data rate of the receiver. Keyboard data arrives at the printer by virtue of the host system echoing the data.

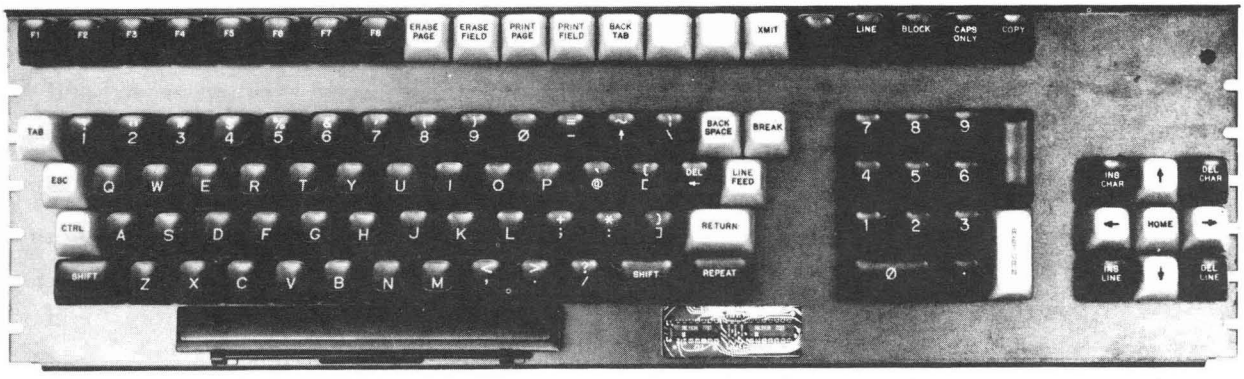
In Line Mode, Local Copy ON, and Character Mode, keyboard and receive data are both sent to the printer at EIA levels and at the same rate as the receiver.

In Line Mode, Local Copy ON, and Block Mode, both received data and transmitted data are sent to the printer.

In Line Mode, Local Copy OFF, and Block Mode, only received data is sent to the printer.

In Local Mode data is inhibited from being sent to the printer.

The Copy Mode function is enabled and disabled by use of the Set Mode and Reset Mode function commands, see Section 2.6.1.



Model 400/4 Keyboard

Model 400/5 Keyboard

Figure 16 Keyboard Assemblies

3.6 OPTIONAL BUFFERED PRINTER OPTION

Two optional printer interfaces are available for the Model 400. Assembly 03278-GO1 provides serial output at EIA Levels and data rates independent of the receiver data rate. Assembly 03278-GO2 provides a parallel output which is slaved to the printer busy signal. Both printer interfaces allow print page and print field functions. If either interface is installed in a polled terminal they may be addressed separately as defined in Section 2.7. The Print Page and Print Field function commands are shown in Section 2.6.1.

3.7 PAGING OPTION

Two versions of the Paging Option are available on the Model 400. One version provides one additional page of memory; the other version provides two additional pages of memory for a maximum of three pages. The additional commands offered with the Paging Option are as follows:

Scroll Up	Moves contents of memory up a specified number of lines.
Scroll Down	Moves contents of memory down a specified number of lines.
Next Page	Moves contents of memory to the next page(s) and places cursor on the first unprotected position of the next page.
Previous Page	Moves contents of memory to the previous page(s) and places cursor in HOME or the first unprotected position of the page.
Form Feed	Moves contents of memory to the next page, erases page, and places cursor in HOME position.

An additional feature of this option is Edit Boundary Mode (EBM). EBM enables the user to edit through line and page boundaries when editing in entire memory is required.

3.8 TIME SHARING OPERATION (TSO)

The TSO Option features the following characteristics:

In Character Mode operation the terminal is in the receive state until a key is struck. The terminal leaves the transmit state when an ETX code or optionally, a CR-ETX code is entered from the keyboard. No automatic turnaround from receive to transmit is supported. The terminal display is always in roll mode.

All Block Mode transmissions will be prefixed by an STX or optionally, no prefix. All Block Mode transmissions will be terminated with an ETX or optionally, a Carriage Return. All transmit requests will be serviced immediately.

3.9 HAZELTINE 2000 EMULATION (HZ-2000)*

The I-400 HZ-2000 Emulation emulates the HZ-2000 command character set and functionality. An additional feature is, while handling data transmissions which include part or all of the bottom (25th) line, the terminal will roll the screen if the transmit symbol is on the bottom line or optionally, will leave the cursor under the transmit symbol.

NOTE: HZ-2000 is a registered trademark of the Hazeltine Corporation.

4. SERVICE

The Model 400 terminal is a modular system that has been designed for ease in service. In addition to a high MTBF, the terminal has a maximum time to repair of 30 minutes. Typically fault location and replacement takes 10 minutes. This section is intended to aid the service man in module replacement. Section 5 of this manual is devoted to troubleshooting and fault location.

4.1 MECHANICAL ACCESS TO THE UNIT

4.1.1 Removal of Cover (Figure 17)

a. Remove two flat head screws from each side of cover
b. Disconnect all interface cables
c. Lift cover straight up and off.

4.1.2 Removal of the Control Logic PCB (Figure 18)

a. Disconnect the two connectors from the top of the PCB
b. Remove keyboard cable connector
c. Remove internal printer cable from option board if present
d. Remove the PCB

4.2 VIDEO MONITOR ADJUSTMENTS

With a screen full of H's, vertical size, vertical linearity, horizontal size, horizontal linearity brightness, contrast, and focus adjustments can readily be made. Consult the appropriate supplement contained in Section 7 for the location of these controls. Best linearity can be achieved when the block of 1920 characters form a rectangle of from 7.5 to 8.5 inches wide (19-21 cm) and 5.5 to 6.0 inches high (14-15 cm).

4.3 POWER SUPPLY ADJUSTMENTS

The 400 is equipped with a general purpose power supply incorporating overvoltage protection and current foldback protection. Power Supply input is selectable as follows.

By Frequency

JP 5 is installed for 60 Hz, removed for 50 Hz.

By Voltage

Figure 19 details the jumper connections for AC Input range selection. This terminal strip is located adjacent to the transformer.

The proper tap is the highest voltage range which contains the value of the nominal line voltage.

The TV monitor receives its power from the +15 volt power supply. As a result there are no changes within the monitor due to line voltage or frequency changes.

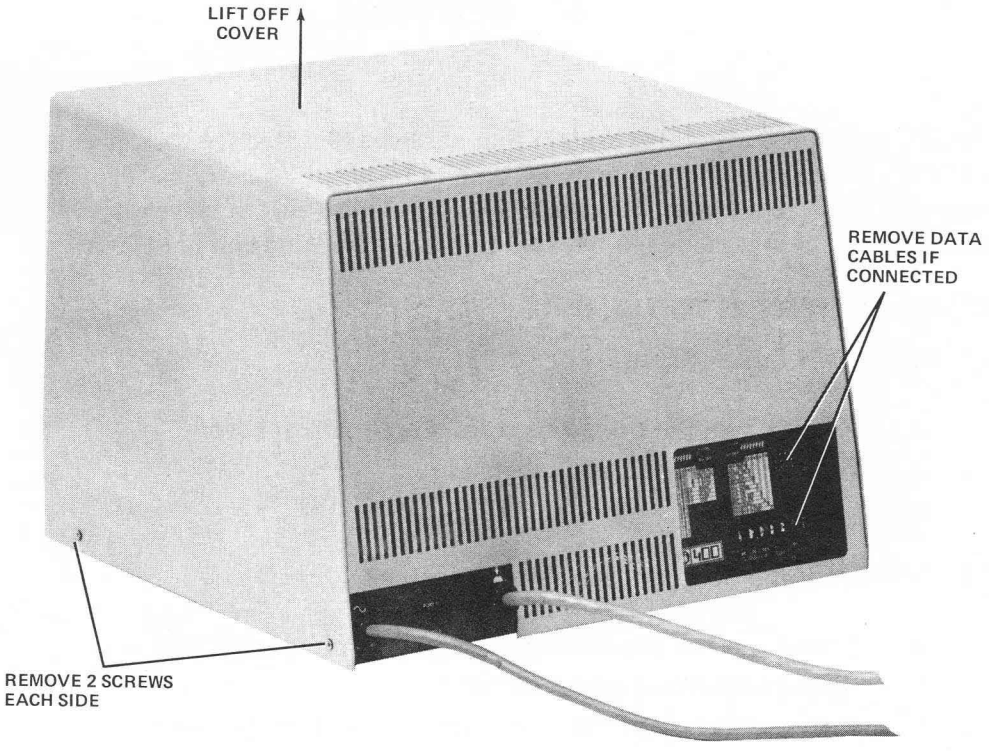


Figure 17 Cover Removal

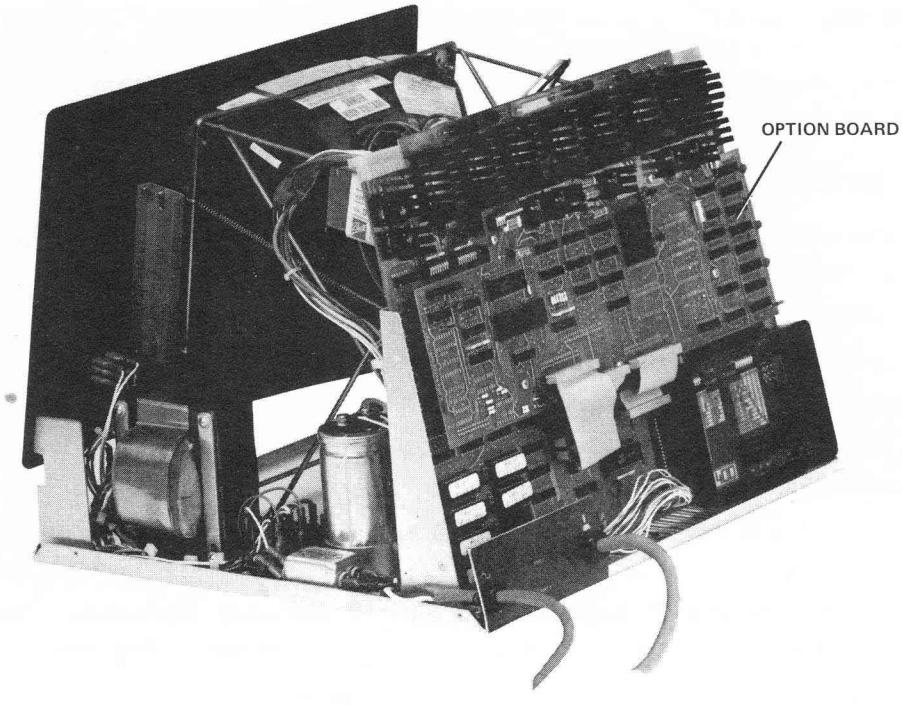


Figure 18 PCB Mounting

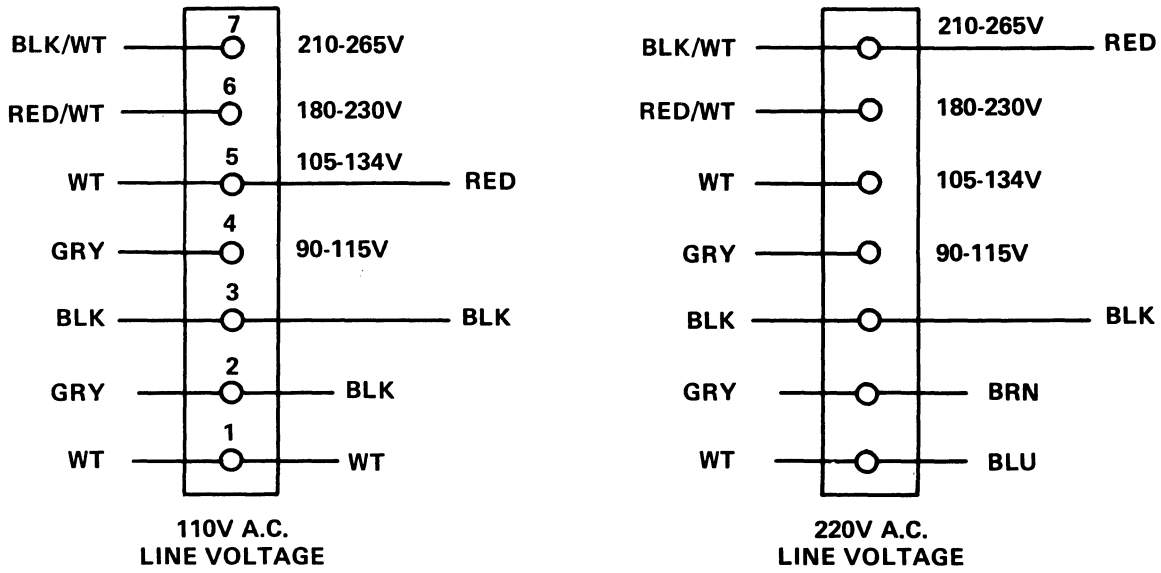


Figure 19 AC Input Selection

4.4 OPTIONAL JUMPERS

The following chart details the use of all jumpers contained on the 400 Control Board Assembly. Jumpers are 10 ohm resistors in the locations shown in Figure 12.

Jumper	Functionality When Installed	Functionality When Removed
JP1	Normal	V3 Emulation
JP2	Asynchronous Interface	Synchronous Interface
JP3	Normal Keyboard installed	Special Keyboard installed
JP4	CTC chip not installed	CTC chip installed
JP5	60 Hz	50 Hz
JP6	Control Code Display enabled	Control Code Display disabled
JP7	Keyboard Caps Lock enabled	Keyboard Caps Lock disabled
JP8	V3 Emulation	Normal
JP9	V3 Emulation	Normal
JP10	Normal	V3 Emulation
JP11	Line Sync	Free Running Sync

The following chart details the use of all jumpers located on the 400 Option Board Assembly. Jumpers are 10 ohm resistors in the locations shown in Figure 20.

Jumper Option	Functionality When Installed	Functionality When Removed
JP1 Parallel Printer	Low True Acknowledge	High True Acknowledge
JP2 Parallel Printer	High True Busy	Low True Busy
JP3 Parallel Printer	High True Paper Empty	Low True Paper Empty
JP4 Parallel Printer	Low True Output Strobe	High True Output Strobe
JP5 Parallel Printer	High True Output Data	Low True Output Data
JP6 Serial Printer	Odd or Space Parity	Even or Mark Parity
JP7 Serial Printer	Odd or Even Parity	Mark or Space Parity
JP8 Serial Printer	10 Bits/Character	11 Bits/Character
JP9 Both Printers	CR After Data	LF, CR After Data
JP10 Both Printers	Form Feed enabled	Form Feed disabled
JP11 Both Printers	Parallel Printer	Serial Printer
JP12 Serial Printer		
JP13 Serial Printer	Determines the number of Null codes sent after	
JP14 Serial Printer	Carriage Return, Line Feed, Vertical Tab, and Form Feed	
JP15 Parallel Printer	High True Printer Select	Low True Printer Select

Printer Delay

CHARACTER	JP14	JP13	JP12	
CR and LF	20	10	5	(Removing JP 14, 13, and 12 equals 35 Nulls)
VT and FF	40	20	10	

A 4 position DIP switch located at U29 selects the Serial Printer Interface Data Rate. The position of each switch is defined in Figure 5.

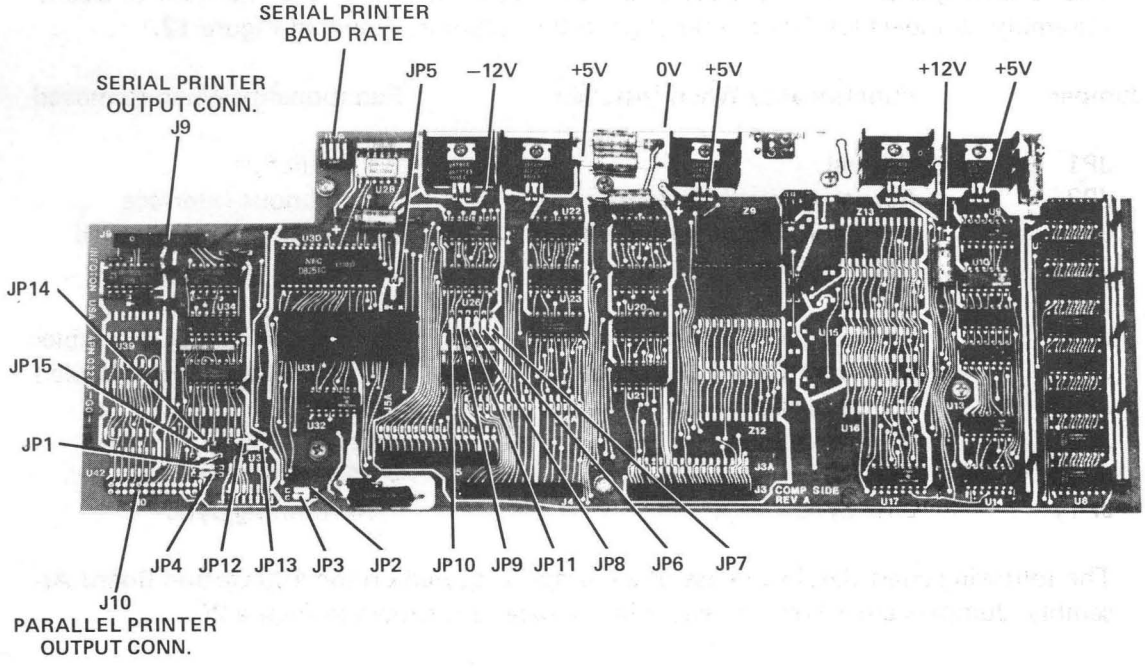


Figure 20 Option Board

4.5 CABLE ASSIGNMENTS

Connector	Function	Destination
J1 (Control Board)	EIA Interface	Modem
J2 (Control Board)	Keyboard Data	Keyboard
J3 (Control Board)	I/O Bus	Option Board J3
J4 (Control Board)	I/O Bus	Option Board J4
J5 (Control Board)	I/O Bus	Option Board J5
J6 (Control Board)	AC Input (Low Voltage)	Transformer Assy.
J7 (Control Board)	Video	TV Monitor
J8 (Control Board)	DC Power	Option Board P8
J9 (Option Board)	Serial Printer I/O	Terminal Rear Panel Connector (Printer, Port 1)
J10 (Option Board)	Parallel Printer I/O	Terminal Rear Panel Connector (Printer, Port 1)

4.6 ORDERING REPLACEMENT AND SPARE PARTS

After determining the failure mode of the unit (see Section 5), a replacement part may be ordered by performing the following steps:

- Identify the terminal by name and serial number (see Figure 21). The serial number name tag is located on the bottom of your Model 400 terminal.

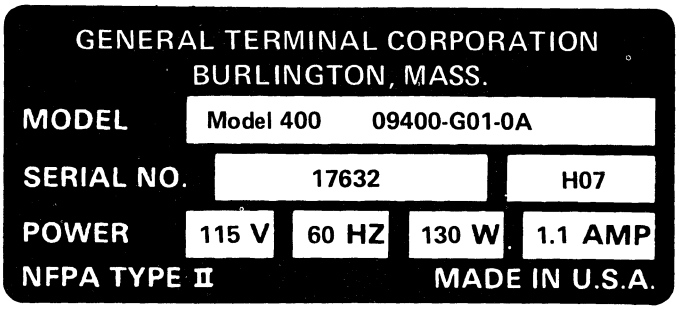


Figure 21 Model 400 Series Name Plate

- Identify the module by name and assembly part number (APN).
- Refer to the spare parts manual in Section 7 to find the proper part number when ordering parts.

If a question arises as to what is the correct part to order, write or call the Manager of Field Service, General Terminal Corporation, Second Avenue, Burlington, Massachusetts 01803; Phone: (617) 272-6660. Be sure to supply the terminal serial number as shown in Figure 16.

General Terminal Corporation maintains a complete product log of each unit in the field. The log is intended to aid the customer in acquiring proper service for his terminal. All factory authorized changes that are applied to a terminal in the field are entered in the product log. If a customer would like General Terminal Corporation to keep a record of authorized factory changes that he may apply to his terminal, he may do so by notifying the Manager of Field Service, General Terminal Corporation, in writing. Be sure to supply detailed information of the changes applied and the display serial number.

5. TROUBLESHOOTING AND FAULT LOCATION

5.1 TERMINAL SELF CHECK

A feature of the terminal is that it is capable of almost a complete self check when placed in the local mode of operation, all subassemblies of the terminal are exercised. Only the serial interface is not fully exercised. The serial interface can be tested by operating the on line with a turn-around plug, (APN 99999-022) Section 7, plugged into the EIA cable.

5.2 SUBASSEMBLY FUNCTIONS

Troubleshooting at the customer's site shall be limited to isolating the fault to one of the system's subassemblies. These subassemblies and their functional role in the system are described in the following paragraphs.

5.2.1 Keyboard Assembly (Figure 13)

- Capacitive switches and encoding logic producing parallel TTL codes
- Line/Local switch

5.2.2 Control PCB (Figure 9)

- Asynchronous Serial Interface
  1. Receives serial input data and converts it to parallel for presentation to memory.
  2. Receives parallel data from keyboard electronics and converts it to serial for data presentation to current loop and EIA output.
  3. Generates I/O direction and request signals.
  4. Contains interface clock source.
  5. Converts received EIA and current loop information to TTL logic levels.
  6. Converts transmit TTL information to EIA and current loop levels.
  7. Provides data rate, bits per character, FDX/HDX, and parity selection information.
- Timing Generator
  1. Clock Source
  2. Raster Generator
  3. Sync Generator
  4. Timing Signal Generator
  5. Memory Timing
- Control Logic
- Video Generation
  1. Read Only Memory (Character Generators)
  2. Parallel to Serial Converter
  3. Video Drivers

- Memory
  1. PROM Program Memory
  2. RAM Scratch Pad Memory
  3. RAM Display Memory
- Power Supply
  1. Power Supply Active Components

5.2.3 Video Monitor

Combines horizontal sync., vertical sync. and serial video information for presentation on the CRT screen.

5.3 TROUBLESHOOTING

Because of the modular construction of the terminal and its built-in self-test capability, troubleshooting is a relatively simple procedure. Most troubleshooting can be accomplished by viewing the CRT while exercising the terminal in local mode. The following additional equipment may be useful when troubleshooting the terminal, especially when the trouble is associated with the particular system configuration in the on-line mode.

- General Purpose Multimeter
- Cross Coupler APN 99999-015
- Turn-around Connector APN 99999-022
- A second terminal
- Oscilloscope Tektronix 465 or equivalent
- ASR 33 Teletype
- Spare set of Replacement Modules

5.3.1 System Test, Off Line (terminal in local mode)

Exercise the terminal from the keyboard, being sure to test all of its functions. Make sure data is loaded onto every line of the display, and that the top and bottom line is filled completely. The turn-around connector may be used by placing the terminal on-line, thereby exercising the entire transmitter and receiver.

5.3.2 System Test, On Line

Repeat steps outlined in 5.3.1 including all control codes recognized by the computer.

5.3.3 Additional Test Features

By entering Transparent Mode (see Section 2.6.1) all incoming characters including control codes and control sequences are displayed instead of being acted upon. This feature is invaluable in determining whether expected control sequences are in fact being received.

On terminals equipped with polling the first address character switch can be set to all ones or zeros instead of an address. This action places the polling function in a monitor mode where all data on the line (this terminal's and any other terminal's on the same data line) is received and displayed. This function is helpful in determining CRT versus CPU or Data Line problems. All control characters, including polling dialog characters, will be displayed in this mode.

5.3.4 Power Supply Testing

Because of over-voltage and over-current protection of the power supply, the symptom of power supply failure may be caused by problems listed below:

- Over-voltage crowbar. Turn unit off, then on again. The power supply should recover from this failure mode.
- Over-current protection causes the power supply to reduce output voltage when the current capacity of the supply is exceeded. This can be caused by a short within any module. To isolate this type of failure, simply unplug each module until the supply recovers. If all modules are removed and the failure still exists, check the PCB for contaminants bridging etched circuits. Replace the control PCB assembly if failure persists.

5.4 FAULT LOCATION

Since there is inherently some interaction between the modules within the terminal, it becomes difficult to pinpoint the defective module for all possible symptoms. In the following table typical failure symptoms, probable sources of trouble, and recommended repairs are listed.

Fault	Probable Source of Trouble	Recommended Repair
Pilot lamp not on; unit inoperable.	Unit not plugged in.	Plug unit in.
	Circuit breaker – Underside left front of unit tripped.	Reset circuit breaker.
	Faulty on/off switch.	Replace switch.
Pilot lamp on but no raster.	Brightness turned full off.	Turn up brightness control.
	Monitor fuse open.	Repair or replace fuse. See the TV Monitor Manual.
	Monitor not plugged in.	Check monitor cord in rear of monitor.
	One or more monitor connectors not connected.	Check connections. TV Monitor Manual.
	Terminal power supply defective.	Repair terminal power supply. See Section 4.
Raster but no sync.	Defective control module.	Replace control module.
	Defective video monitor.	Repair or replace video monitor.
Sync but no video pattern.	Defective control module.	Replace control module.
	Defective video monitor.	Repair or replace video monitor.
Noise on screen; sync poor or nonexistent.	Defective control module.	Replace control module.
	Defective power supply.	Replace control module.

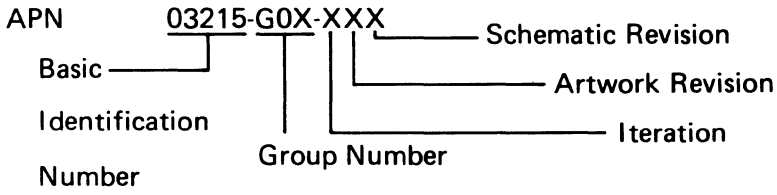
Figure 22 Fault Location

Fault	Probable Source of Trouble	Recommended Repair
Sync and video random characters; cursor may not be present.	Unit not initialized.	Turn unit off, wait 5 seconds, turn unit on.
	Defective control module.	Replace control module.
Characters broken or unintelligible.	Defective control module.	Replace control module.
Cursor but no cursor movement and no characters.	Defective control module.	Replace control module.
	Defective keyboard.	Repair or replace keyboard. Could be stuck key for a control character.
Cursor and characters but no cursor movement.	Defective control module.	Replace control module.
Cursor movement but no characters in system.	Defective keyboard.	Repair or replace keyboard. Could be stuck key.
Enters incorrect characters.	Defective control module.	Replace control module.
	Defective asynchronous serial interface drivers/receivers.	Replace control module.
	Defective keyboard.	Repair or replace keyboard. Character errors not bit-oriented.
Enters single character for all keys.	Defective keyboard.	Stuck key usually on key of character entered on the screen.
	Defective control module.	Replace control module.
Operable off line (local); not operable on line.	Defective asynchronous serial interface	Replace control module
	Defective control module.	Replace control module.

Figure 22 Fault Location (Continued)

6. DRAWINGS

The following drawings relate to the terminal. Figure 23 shows the relationship between the module assembly numbers (APN 03215-G01-XXX) and the schematics.



The X's denote various generations of the basic module.

6.1 MNEMONICS LIST

6.2 SCHEMATIC MAIN LOGIC INCLUDING POWER SUPPLY (7 Sheets)

6.3 OPTION SCHEMATICS (5 Sheets)

6.4 KEYBOARD SCHEMATICS (7 Sheets)

Title	Assembly Part Number	Schematic
Control Board and Power Supply	APN 03215-G01-XXX	03213
Serial Printer Option	APN 03278-G01-XXX	03277
Parallel Printer Option	APN 03278-G02-XXX	03277
Extended Firmware	APN 03278-G03-XXX	03277
Extended Data Memory	APN 03278-G04-XXX	03277
Serial Printer and Data Memory	APN 03278-G05-XXX	03277
Parallel Printer and Data Memory	APN 03278-G06-XXX	03277
Keyboard 400/4 (E20)	APN 03189-003	1768 (KTC)
Keyboard 400/5 (E30)	APN 03191-001	1667 (KTC)

Figure 19 Assembly to Schematic Reference Table

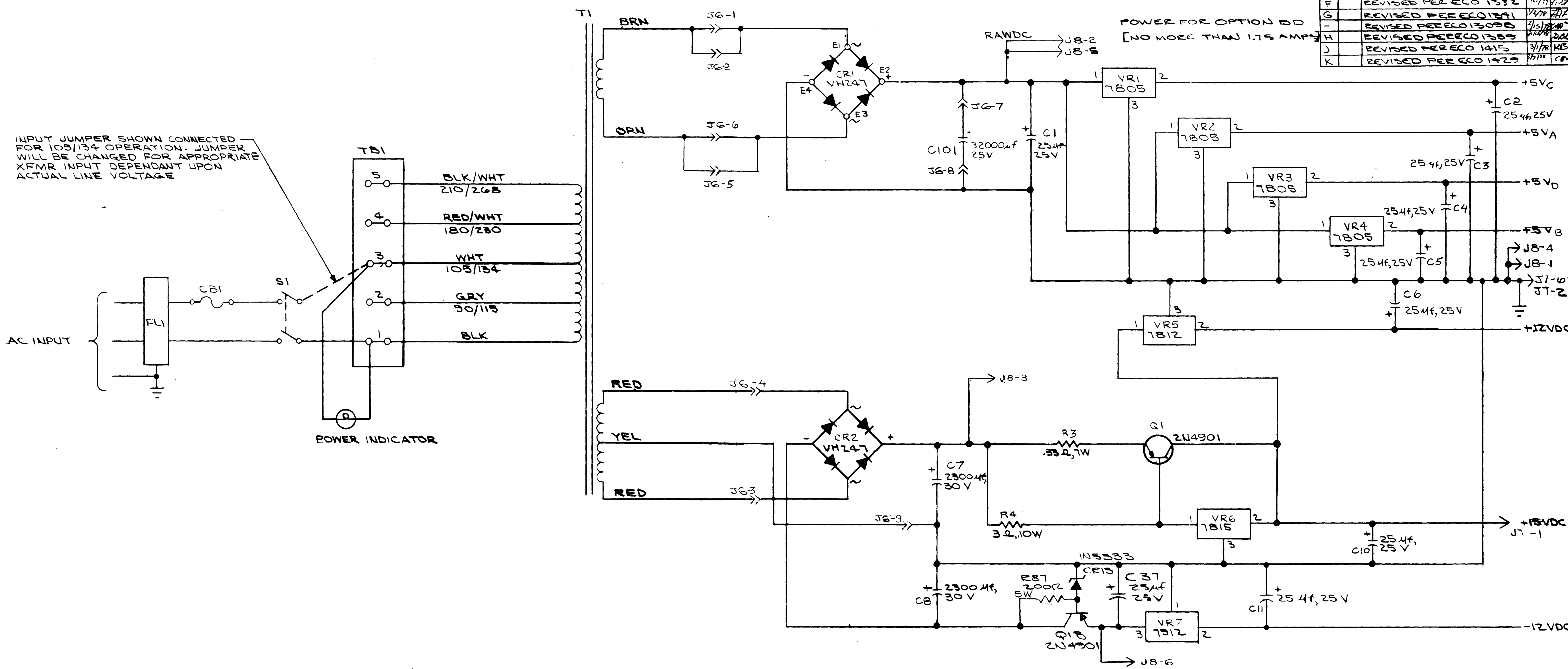
Mnemonics	Definitions	PCB	Sheet	Schematic Location	PCB Chip Location
DRCLK	DATA RATE CLOCK	CONT	7	D8	A11
DRH	DATA RATE MSB SWITCH	CONT	2	C4	K9
DSR	TTL DATA SET READY	CONT	2	C6	K12
DTR	TTL DATA TERMINAL READY	CONT	4	B5	M6
ELC	END OF LINE COUNT (SLICE 9)	CONT	7	C4	F8
ERLC	END RASTER LINE COUNT (LAST SLICE ON SCREEN)	CONT	7	B2	E11
ESCT	ENABLE SLICE COUNT TIME	CONT	7	C5	C9
FBUFFED	FIRMWARE BUFFERED (TO BLOCK LED)	CONT	4	A4	L9
FCLK	FAST CLOCK (24.024 MHz)	CONT	7	D7	B11
FDOT	FORCE DOTS	CONT	3	B5	C6
HBLNK	HORIZONTAL BLANKING	CONT	7	C6	C9
HDRIVE	HORIZONTAL DRIVE TO MONITOR	CONT	7	A4	E11
HDRIVES	HORIZONTAL DRIVE	CONT	7	C6	C9
HLFIN	HALF INTENSITY	CONT	7	A8	D7
HLFINE	HALF INTENSITY FUNCTION	CONT	3	B6	F6
ICF	INSERT CHARACTER FLOP	CONT	4	A4	L9
IDC	20 MA CURRENT SOURCE	CONT	3	B3	TB1
IM1	OPCODE FETCH CYCLE FLAG TO EXTERNAL DEVICE	CONT	4	C5	J6
INRET	CURRENT LOOP INPUT RETURN	CONT	3	C4	TB1
INT	INTERRUPT TO μP	CONT	2	C1	E12
IORZ	μP I/O REQUEST	CONT	4	C8	P4
I/ORQ	DATA I/O REQUEST	CONT	4	D5	J6
KBØ	KBD BIT Ø	KBD	2	C5	J2
KBRK	KBD BREAK KEY	KBD	2	D5	J2
KBSTB	KBD KEY STROBE	KBD	2	D5	J2
KBUFFED	KBD BLOCK KEY	KBD	2	D5	J2
KLINE	KBD LINE KEY	KBD	2	D5	J2
KLINE LED	KBD LINE KEY LED	KBD	2	D5	J2
KSPARE	KBD SPARE KEY	KBD	2	D5	J2
KSPARE LED	KBD SPARE KEY LED	KBD	2	D5	J2
LINE	ON LINE FUNCTION	CONT	2	D4	M10
LRVID	LOGICAL REVERSE VIDEO	CONT	3	B5	C6
LVIDE	LOGICAL VIDEO ENABLE	CONT	3	A5	H8
M1	μP OPCODE FETCH CYCLE IN PROCESS	CONT	4	C7	P4
MBØ	DATA MEMORY OUTPUT BIT Ø	CONT	6	C7	U9
MEMRQ	DATA MEMORY REQUEST	CONT	4	D5	J6
MREQ	μP MEMORY ADDRESS BUS REQUEST	CONT	4	C7	P4
NMI	NON MASKED INTERRUPT EXTERNAL INPUT	CONT	4	C7	P4
ODD	ODD PARITY SWITCH	CONT	2	B4	K9
OUT	CURRENT LOOP OUTPUT	CONT	3	B2	TB1

Mnemonics	Definitions	PCB	Sheet	Schematic Location	PCB Chip Location
PAGE	KBD PAGE KEY	KBD	2	D5	J2
PARITY	PARITY SWITCH	CONT	2	B4	K9
PC2	PROCESSOR CLOCK BIT2	CONT	7	A2	F10
PCP1	PRINT COPY	CONT	4	A5	L9
PCP2	PRINT PAGE	CONT	4	A5	L9
PCLOCK	PROCESSOR CLOCK (3.003 MHz)	CONT	7	A1	F9
PIE	PARALLEL I/O INTERRUPT OUTPUT (DAISY CHAIN)	CONT	4	A5	L9
PLFP	POWER LINE FRAME PULSE	CONT	1	C4	R1
PLSP	POWER LINE SYNC PULSE	CONT	7	C6	C10
PSØ	PROGRAM PROM SELECT Ø	CONT	6	A3	H5
PSD	PRINTER SERIAL DATA (UNBUFFERED)	CONT	2	C3	C11
PVI	PRIORITY VIDEO INTERRUPT	CONT	6	A3	D6
RAMØ	BUFFERED DATA MEMORY OUTPUT BIT Ø	CONT	6	C1	E3
RAWDC	UNREGULATED +5 VOLTS	CONT	1	D3	CR1
RCLOCK	RECEIVE CLOCK	CONT	2	A4	J11
RCVD	RECEIVED DATA (TTL)	CONT	2	D7	K10
RD	MEMORY OR I/O READ TO μP	CONT	3	C7	P4
READ	PROGRAM OR DATA MEMORY READ ENABLE	CONT	4	D5	J6
RECV DATA	EIA RECEIVED DATA	CONT	2	D6	J1
REQ TO SEND	EIA REQ. TO SEND	CONT	2	B6	L11
RESET	INITIALIZE RESET OR EXTERNAL RESET	CONT	4	D2	J8
RET	20 MA CURRENT SOURCE RETURN (GND)	CONT	3	A2	TB1
RFRSH	RFSH FUNCTION TO EXT. DEVICE OR MEMORY	CONT	4	C5	J6
RFSH	REFRESH PORTION OF μP PROGRAM MEMORY READ/REFRESH CYCLE	CONT	4	C7	P4
RSI	RESET SERIAL INTERRUPT	CONT	4	A3	J5
RSTSW	EXTERNAL RESET (INITIALIZE) SWITCH	CONT	4	D3	J3
RTS	TTL REQ. TO SEND	CONT	4	B5	M6
RTSSW	REQ. TO SEND SWITCH	CONT	2	B4	K11
RVID	REVERSE VIDEO SWITCH	CONT	2	B4	K11
RXD	RECEIVE & XMIT DATA	CONT	2	A3	J10
RXR	RECEIVE READY	CONT	4	C5	M6
RXRE	RECEIVE READY ENABLE	CONT	4	A4	L9
ACE	SECONDARY CHANNEL ENABLE SWITCH	CONT	2	B4	K11
SCI	SEC. CHANNEL INVERT	CONT	2	B4	K11
SCIC	SELECT CONTROL TIMER CHIP	CONT	4	A3	J5
SCLKØ	SLICE CLOCK BIT Ø	CONT	7	D4	F8
SCRTS	SEC. CHANNEL REQUEST TO SEND	CONT	4	A5	L9
SEC. CH CTS	SEC. CHANNEL CLEAR TO SEND	CONT	2	A6	J1
SEC. CH RTS	SEC. CHANNEL REQ TO SEND	CONT	2	A6	L11

Mnemonics	Definitions	PCB	Sheet	Schematic Location	PCB Chip Location
SPIO	SELECT PARALLEL I/O CHIP	CONT	4	A3	J5
SRC	TTL SYNC. RECEIVE CLOCK	CONT	2	C7	M12
SS6	CR/EOT SWITCH	CONT	2	B4	K11
SS7	FIELD EOT/ETX SWITCH	CONT	2	B4	K11
SS8	PAGE EOT/ETX SWITCH	CONT	2	B4	K11
SSB	STOP BIT SWITCH	CONT	2	B4	K9
SSIO	SELECT SERIAL I/O (USART)	CONT	4	A3	J5
SSMX1	SELECT STATUS MUX	CONT	4	A2	F5
SSMX2	SELECT MUX 2 (POLLING ADDRESS SWITCHES)	CONT	4	A2	F5
SXC	TTL SYNC. XMIT CLOCK	CONT	2	C7	M12
SYNCH RCV CLK	EIA SYNC. RECEIVE CLOCK	CONT	2	C7	J1
SYNCH XMIT CLOCK	EIA SYNC. XMIT CLOCK	CONT	2	C7	J1
TCLOCK	TRANSMIT CLOCK	CONT	2	A4	J11
VBLNK	VERTICAL BLANKING	CONT	7	C2	A8
VCCØ	VIDEO CHARACTER COUNTER BIT Ø	CONT	7	D6	C8
VDRIVE	VERTICAL DRIVE	CONT	7	C2	A8
VIDE	VIDEO ENABLE	CONT	3	D7	E6
VIDEO	VIDEO OUTPUT TO MONITOR	CONT	7	A3	Q17
VLCØ	VIDEO LINE COUNTER BIT Ø	CONT	7	C2	B8
VMA1Ø	VIDEO MEMORY (REFRESH) ADDRESS BIT 1Ø	CONT	6	A5	H7
VMR	VIDEO MEMORY READ	CONT	6	A2	H7
VMS	VIDEO MEMORY STROBE	CONT	6	A3	H5
VSRIØ	VIDEO SHIFT REGISTER INPUT BIT Ø	CONT	3	D5	E4
VSRR	VIDEO SHIFT REGISTER RESET	CONT	3	D7	E6
WAIT	EXTERNAL INPUT TO STALL μP	CONT	4	C7	J5
WCCC	WRITE TO CURSOR CHARACTER COUNTER	CONT	4	A3	J5
WCLC	WRITE TO CURSOR LINE COUNTER	CONT	4	A3	J5
WR	μP WRITE DATA	CONT	4	C7	P4
WRITE	DATA MEMORY WRITE ENABLE	CONT	4	D5	J6
XCLK	EXTERNAL TTL CLOCK INPUT	CONT	2	A5	J1
XCLKE	EXTERNAL CLOCK ENABLE SWITCH	CONT	2	B4	K11
XIE	EXTERNAL INTERRUPT ENB (INT. DAISY CHAIN)	CONT	4	C2	J8
XRESET	EXTERNAL RESET (INITIALIZE) OUTPUT	CONT	4	D2	J8
20 MA	20 MA CURRENT LOOP INPUT	CONT	3	C5	TB1
60 MA	60 MA CURRENT LOOP INPUT	CONT	3	C5	TB1

SYM	ZONE	DESCRIPTION	DATE	APPD
L		REVISED PER ECO 1448A	6/22/78	F.D.F.
M		REVISED PER. ECO 1469A	6/22/78	F.D.F.
N		REVISED PER ECO 1485	7/18/78	BBB

SYM	ZONE	DESCRIPTION	DATE	APPD
A		RELEASED		
B		REVISED PER ECO 1276	9/20/77	BBB
C		REVISED PER ECO 1300	10/7/77	KB
D		REVISED PER ECO 1309	10/7/77	KB
E		REVISED PER ECO 1319	10/17/77	KB
F		REVISED PER ECO 1332	10/21/77	F.D.F.
G		REVISED PER ECO 1341	1/2/78	F.D.F.
–		REVISED PER ECO 1309B	2/15/78	
H		REVISED PER ECO 1389	2/15/78	BBB
J		REVISED PER ECO 1415	3/1/78	KB
K		REVISED PER ECO 1429	3/7/78	CBV



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. RESISTORS ARE 1/4W, 5%
2. VR1, VR2, VR3, VR4, VR6 + Q1 ARE MOUNTED ON THERMALLOY HEAT SINKS, PART NO. [illegible]-169.
3. CR1 AND CR2 ARE MOUNTED ON THERMALLOY HEAT SINK, PART NO. 999[illegible]-122.
4. VR5 + VR7 ARE MOUNTED ON THERMALLOY HEAT SINKS, PART NO. [illegible]3-122.
5. Q18 IS MOUNTED ON THERMALLOY HEAT SINK PART NO. 99999-182.
6. P10 USE FAIRCHILD IL-1 ONLY

QTY PER DASH NO.	PART OR IDENTIFYING NO.	INFOTON PART NO.	NOMENCLATURE OR DESCRIPTION	ITEM NO.

PARTS LIST

MATERIAL

DR H. L. Barnes
CHK C. D[illegible] 7/28/77
APPD K. Ba[illegible] 7/28/77
APPD [illegible] 7/28/77

SCHEMATIC
MODEL GT400
POWER SUPPLY

SIZE D | 03213 | REV N

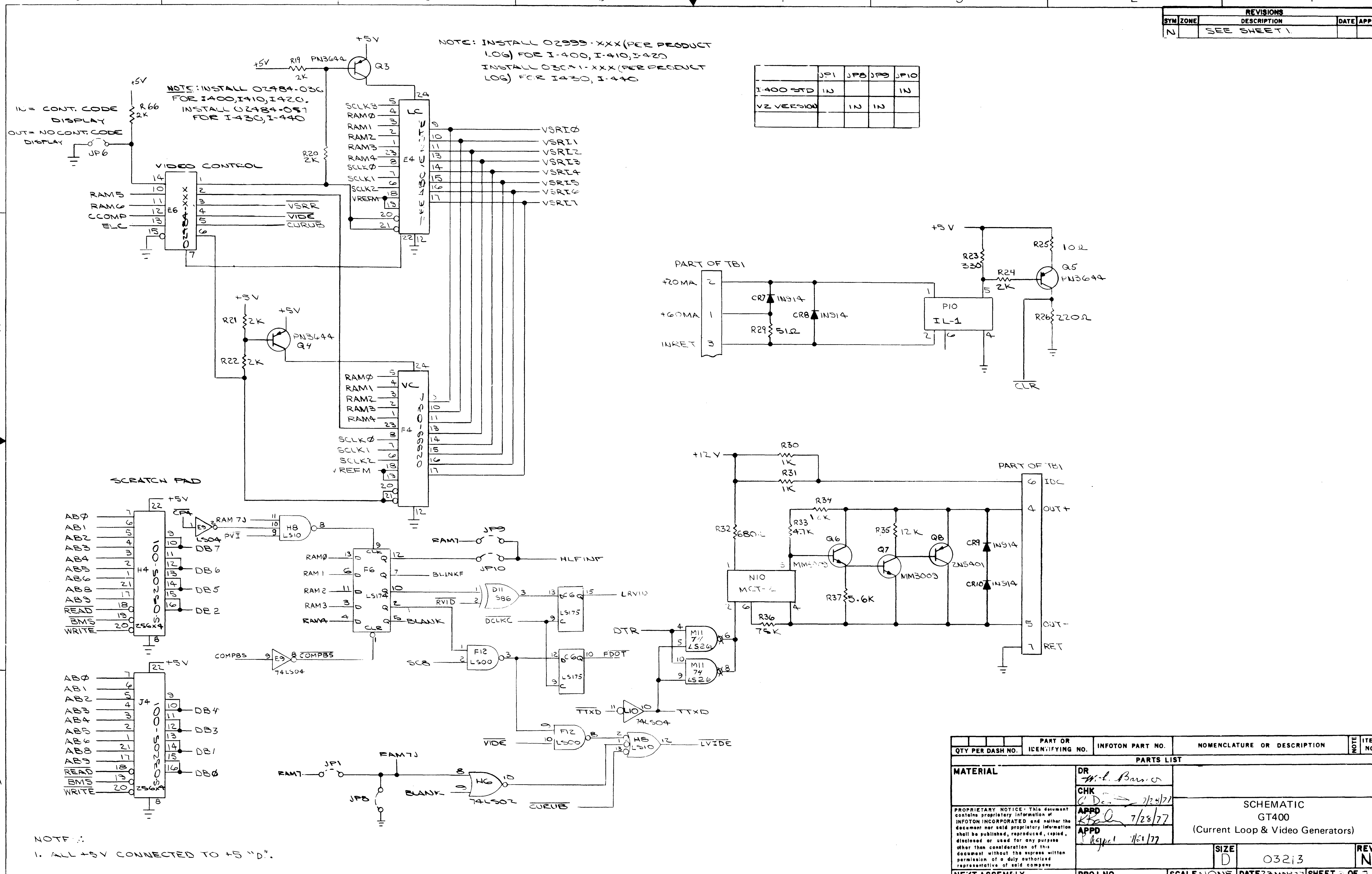
NEXT ASSEMBLY | PROJ. NO. | SCALE NONE | DATE 17 FEB 77 | SHEET 1 OF 1

REVISIONS				
SYM	ZONE	DESCRIPTION	DATE	APPD
N		SEE SHEET 1		

NOTE:
1. ALL +5V TO BE CONNECTED TO "D" REGULATOR EXCEPT CHIPS MARKED **

QTY PER DASH NO.	PART OR IDENTIFYING NO.	INFOTON PART NO.	NOMENCLATURE OR DESCRIPTION	NOTE	ITEM NO.
			PARTS LIST		

MATERIAL	DR W. L. Barnes		
PROPRIETARY NOTICE - This document contains proprietary information of INFOTON INCORPORATED and neither the document nor said proprietary information shall be published, reproduced, copied, disclosed or used for any purpose other than consideration of this document without the express written permission of a duly authorized representative of said company	CHK C. Davis 7/28/77	SCHEMATIC GT400 EIA INTERFACE	
	APPD K. Klein 7/28/77		
	APPD J. Kapel 7/28/77	SIZE D	03213 REV N
NEXT ASSEMBLY	PROJ. NO.	SCALE NONE	DATE 14 MAR 77 SHEET 2 OF 7



	JP1	JP8	JP9	JP10
I-400 STD	IN			IN
V2 VERSION		IN	IN	

REVISIONS

SYM	ZONE	DESCRIPTION	DATE	APPD
N		SEE SHEET 1		

QTY PER DASH NO.	PART OR IDENTIFYING NO.	INFOTON PART NO.	NOMENCLATURE OR DESCRIPTION	NOTE	ITEM NO.

PARTS LIST

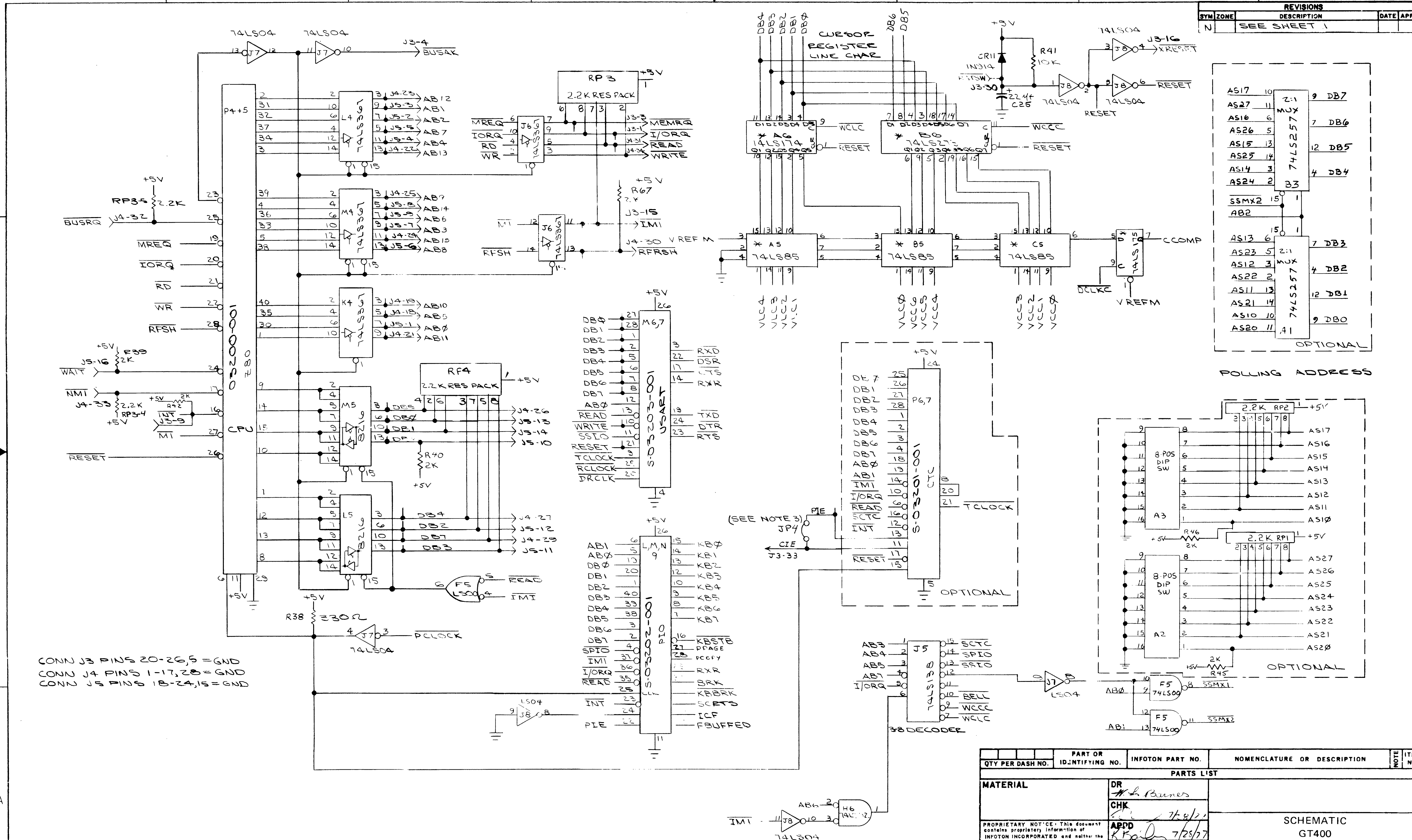
MATERIAL

DR W. L. Barr
CHK C. D. 7/28/77
APPD K Bal 7/28/77
APPD 8/1/77

SCHEMATIC
GT400
(Current Loop & Video Generators)

SIZE D — 03213 — REV N

NEXT ASSEMBLY | PROJ. NO. | SCALE NONE | DATE 23MAR77 | SHEET 3 OF 7



REVISIONS

SYM	ZONE	DESCRIPTION	DATE	APPD
N		SEE SHEET 1		

NOTES:
1. ALL CHIPS MARKED * CONNECTED TO "D" REGULATOR.
2. ALL OTHER +5V CONNECTED TO "C" REGULATOR.
3. JP4 INSTALLED IF Z80 CTC (P6,7) NOT INSTALLED.

QTY PER DASH NO.	PART OR IDENTIFYING NO.	INFOTON PART NO.	NOMENCLATURE OR DESCRIPTION	NOTE	ITEM NO.

PARTS LIST

MATERIAL

DR W. L. Barnes
CHK 7/8/77
APPD 7/25/77
APPD 11/28/77

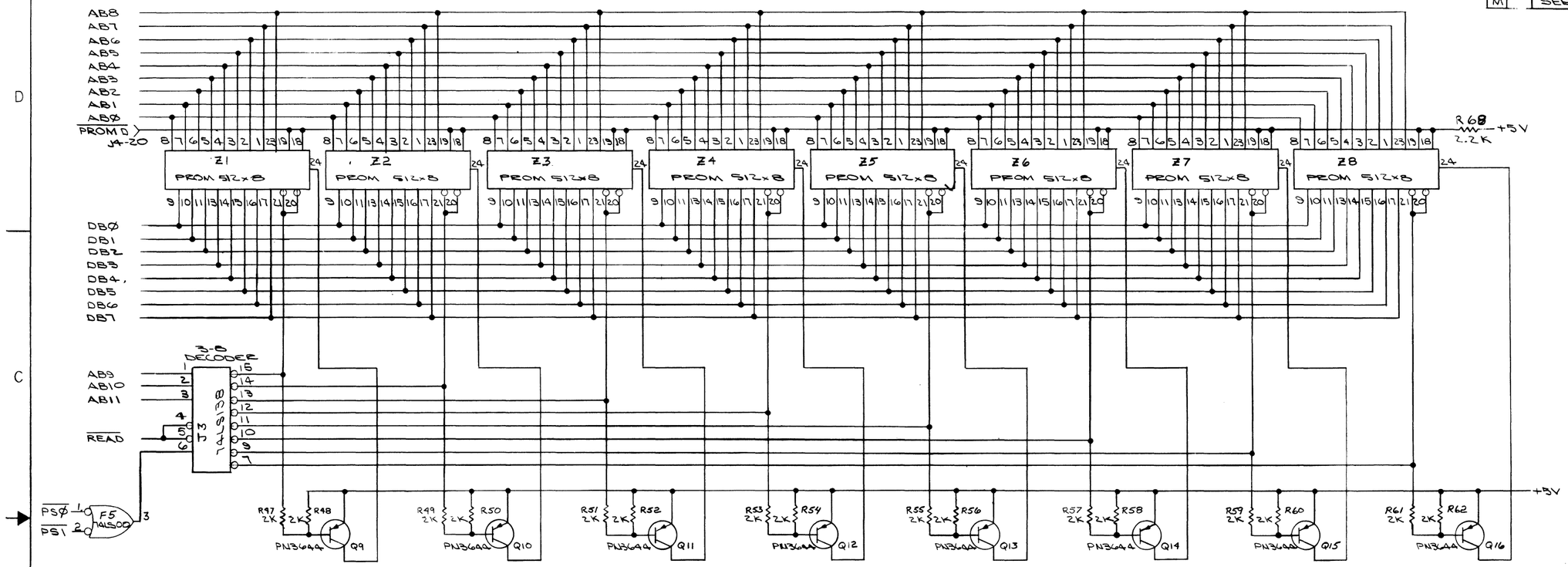
PROPRIETARY NOTICE: This document contains proprietary information of INFOTON INCORPORATED and neither the document nor said proprietary information shall be published, reproduced, copied, disclosed or used for any purpose other than consideration of this document without the express written permission of a duly authorized representative of said company.

SCHEMATIC
GT400
MICROPROCESSOR

SIZE D 03213 REV N

NEXT ASSEMBLY | PROJ NO. | SCALE NONE | DATE 11 MAR 77 | SHEET 4 OF 7

REVISIONS				
SYM	ZONE	DESCRIPTION	DATE	APPD
M		SEE SHEET 1		



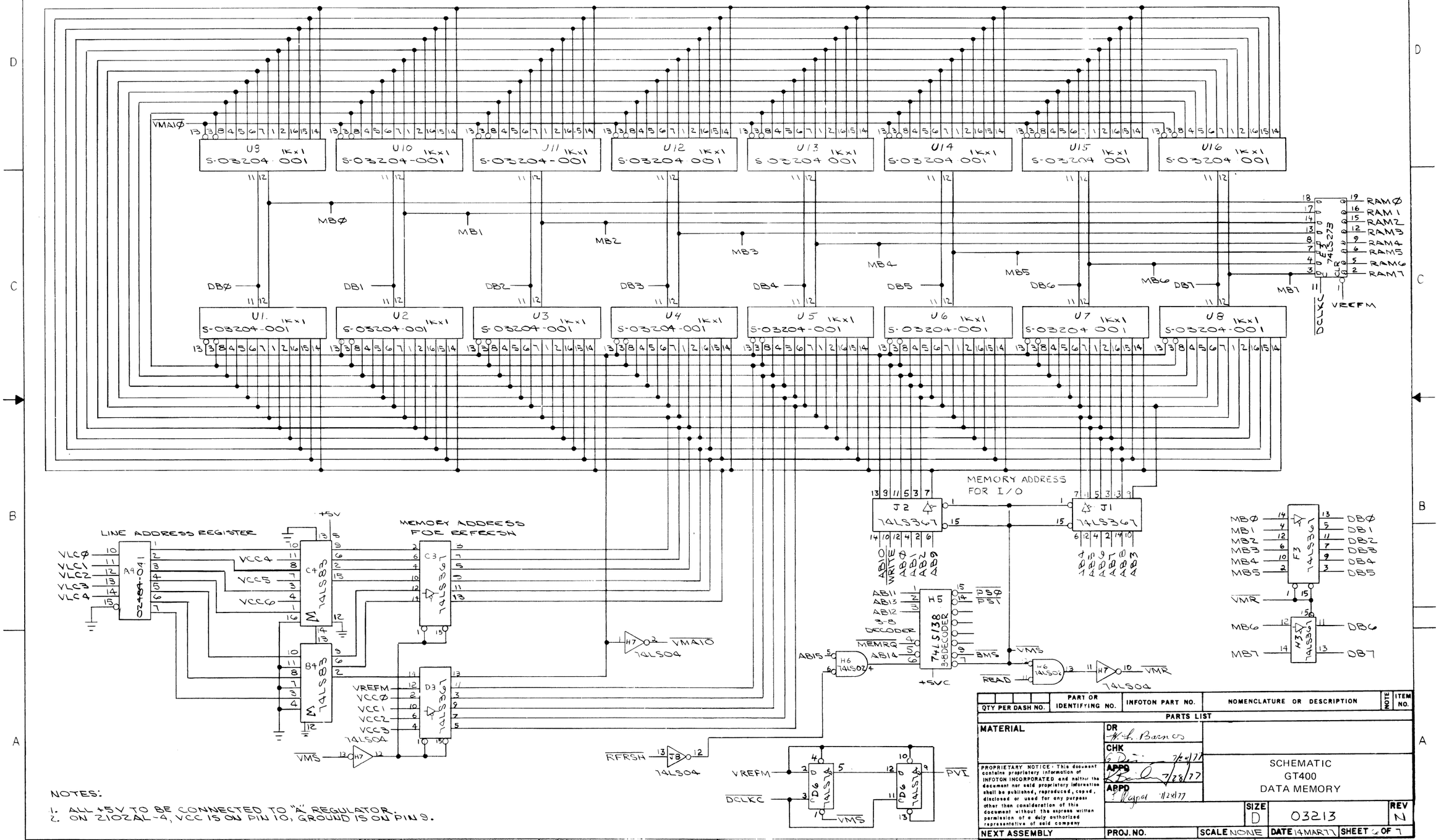
NOTES:

1. ALL +5V TO BE CONNECTED TO "C" REGULATOR.

QTY PER DASH NO.	PART OR IDENTIFYING NO.	INFOTON PART NO.	NOMENCLATURE OR DESCRIPTION	NOTE	ITEM NO.
PARTS LIST					

MATERIAL	DR W. F. Barnes	
	CHK 7/28/77	
PROPRIETARY NOTICE: This document contains proprietary information of INFOTON INCORPORATED and neither the document nor said proprietary information shall be published, reproduced, copied, disclosed or used for any purpose other than consideration of this document without the express written permission of a duly authorized representative of said company	APPD 7/28/77	SCHEMATIC GT400 PROGRAM MEMORY
	APPD P. Rappl 7/28/77	
		SIZE D — 03213 — REV N
NEXT ASSEMBLY	PROJ. NO.	SCALE NONE — DATE 30 DEC 76 — SHEET 5 OF 7

REVISIONS				
SYM	ZONE	DESCRIPTION	DATE	APPD
N		SEE SHEET 1		



NOTES:

1. ALL +5V TO BE CONNECTED TO "A" REGULATOR.
2. ON 2102AL-4, VCC IS ON PIN 10, GROUND IS ON PIN 9.

QTY PER DASH NO.	PART OR IDENTIFYING NO.	INFOTON PART NO.	NOMENCLATURE OR DESCRIPTION	NOTE	ITEM NO.
PARTS LIST					

MATERIAL

DR W. L. Barnes 7/4/77
CHK 7/4/77
APPD 7/28/77
APPD 11/24/77

SCHEMATIC
GT400
DATA MEMORY

NEXT ASSEMBLY	PROJ. NO.	SCALE NONE	SIZE D	03213	REV N
			DATE 14MAR77	SHEET 6 OF 7	

REVISIONS				
SYM	ZONE	DESCRIPTION	DATE	APPD
N		SEE SHEET 1		

XTAL FREQ	MAINS FREQ	FROM C7	FROM F7	FROM A7	FROM B7
24.024	60HZ	4-042	4-051	N/A	4-059
24.024	50HZ	4-029	4-051	4-056	N/A
24.576	50 OR 60HZ	4-042	4-051	4-056	4-059

QTY PER	DASH NO.	PART OR IDENTIFYING NO.	INFOTON PART NO.	NOMENCLATURE OR DESCRIPTION	NOTE	ITEM NO.

PARTS LIST

MATERIAL

DR W.A. Burnes 7/28/77

CHK 7/28/77

APPD 7/28/77

APPD 7/28/77

PROPRIETARY NOTICE: This document contains proprietary information of INFOTON INCORPORATED and neither the document nor said proprietary information shall be published, reproduced, copied, disclosed or used for any purpose other than consideration of this document without the express written permission of a duly authorized representative of said company

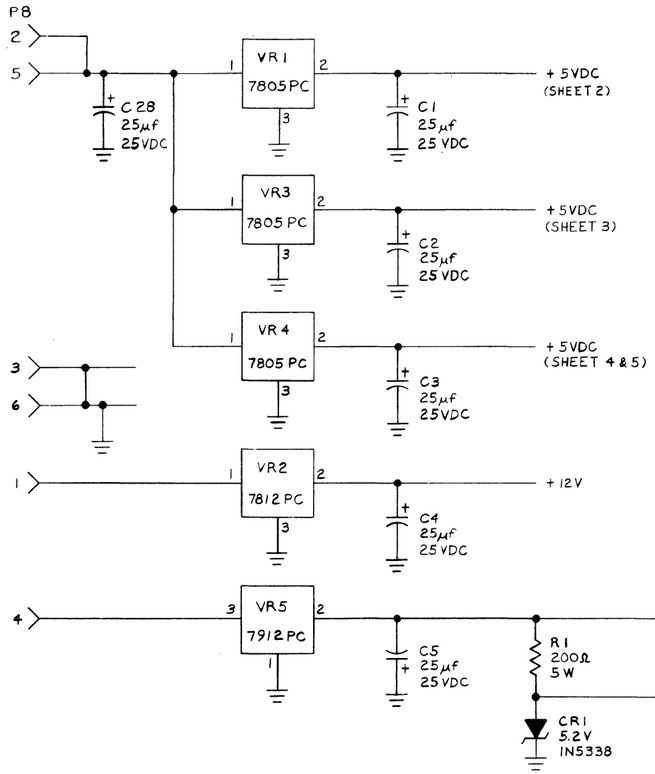
SCHEMATIC
GT400

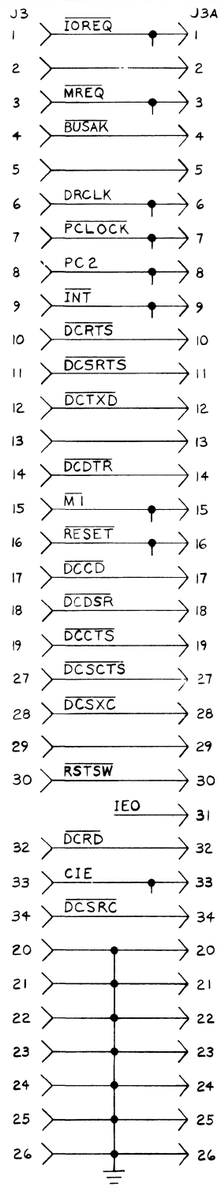
SIZE D | 03213 | REV N

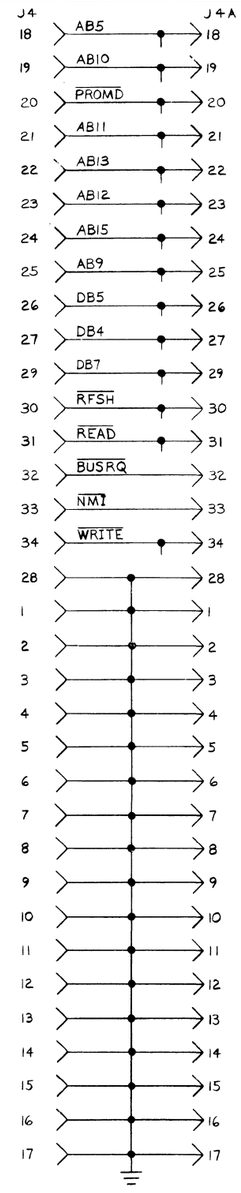
NEXT ASSEMBLY | PROJ. NO. | SCALE NONE | DATE 22 MAR 77 | SHEET 1 OF 1

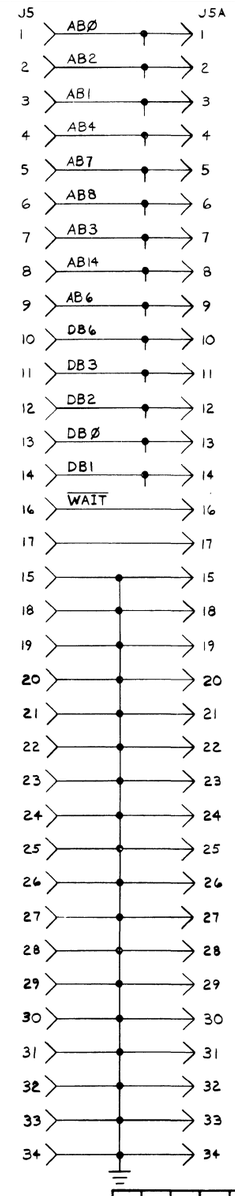
NOTES:
1. * INDICATES IC IN SAME PACK
2. ALL +5 V TO BE CONNECTED TO "B" REGULATOR.
3. CUT JP1 TO INHIBIT BLINK; CUT JP2 FOR HALF INTENSITY.

IN = 60 CYCLE
OUT = 50 CYCLE









REVISIONS				
SYM	ZONE	DESCRIPTION	DATE	APPD
B		REVISED PER ECO 1328	8/4/77	JDE
C		REVISED PER ECO 1339	8/17/77	JDE
D		REVISED PER ECO 1350A	9/15/77	JDE
E		REVISED PER ECO 1417	3/1/78	KB

QTY PER DASH NO.	PART OR IDENTIFYING NO.	INFOTON PART NO.	NOMENCLATURE OR DESCRIPTION	NOTE	ITEM NO.

PARTS LIST

MATERIAL

DR J. L. Eldridge

CHK 8/22/77

APPD 9/30/77

APPD

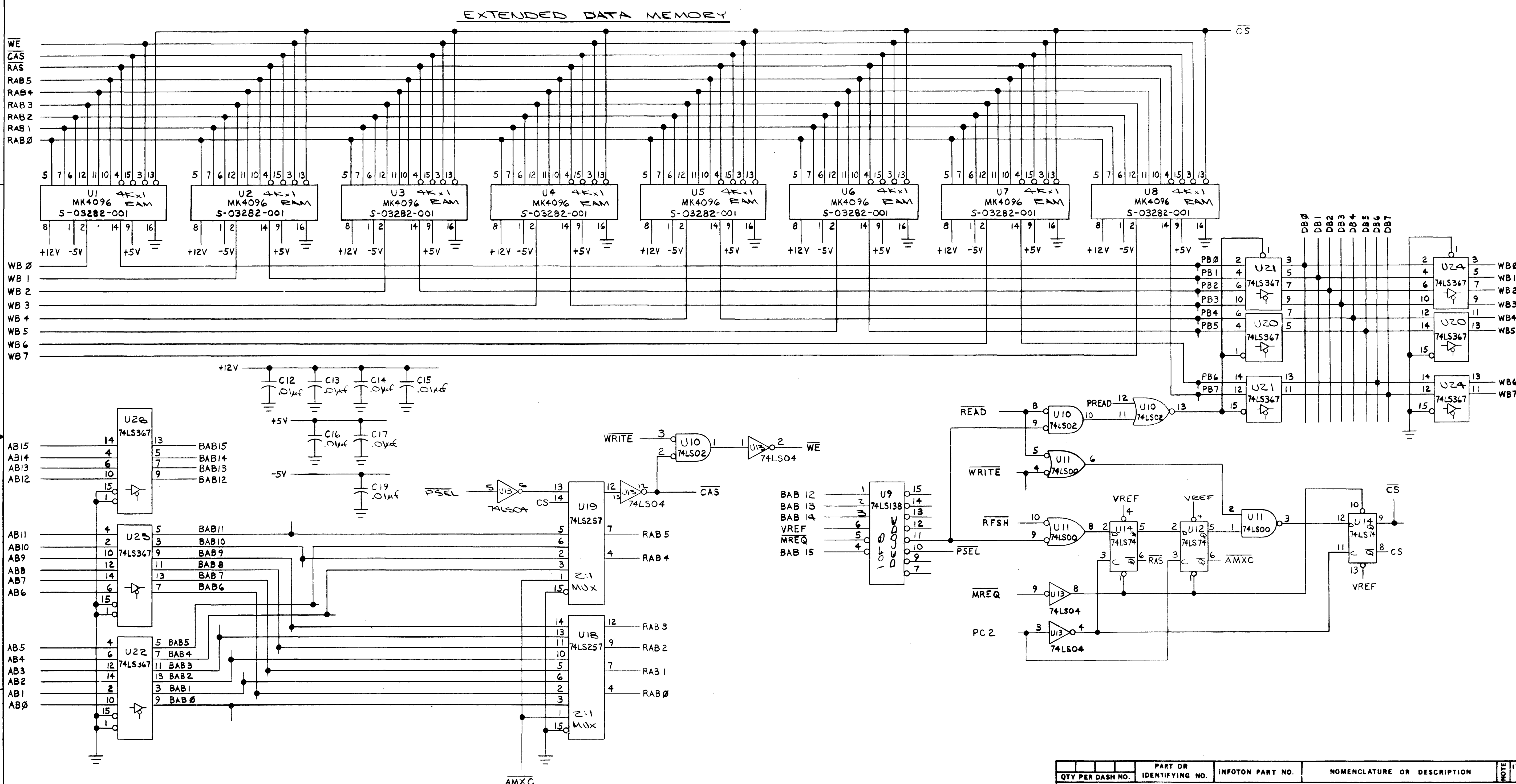
BUFFERED I/O PORT AND EXTENDED MEMORY OPTION
GT400

SIZE D | 03277 | REV E

NEXT ASSEMBLY | PROJ. NO. | SCALE NONE | DATE 23 AUG 77 | SHEET 1 OF 5

REVISIONS

SYM	ZONE	DESCRIPTION	DATE	APPD
		SEE SHT 1		



NOTES:

1. FILTER CAPS IN THE RAM ARRAY ARE LOCATED AS FOLLOWS:
   - +12 - EVERY CHIP
   - +5 - EVERY OTHER CHIP
   - -5 - EVERY CHIP WITHOUT A +5 FILTER CAP.

QTY PER DASH NO.	PART OR IDENTIFYING NO.	INFOTON PART NO.	NOMENCLATURE OR DESCRIPTION	NOTE	ITEM NO.

PARTS LIST

MATERIAL

DR L.L. Eldridge
CHK
APPD R. Bailey 9/30/77
APPD

BUFFERED I/O PORT AND EXTENDED MEMORY OPTION GT400

SIZE D | 03277 | REV E

NEXT ASSEMBLY | PROJ. NO. | SCALE NONE | DATE 26 AUG 77 | SHEET 2 OF 5

REVISIONS				
SYM	ZONE	DESCRIPTION	DATE	APPD
		SEE SHT 1		

EXTENDED PROGRAM MEMORY

EXTENDED SCRATCH PAD MEMORY

READ
WRITE
BAB 8
BAB 7
BAB 6
BAB 5
BAB 4
BAB 3
BAB 2
BAB 1
BAB Ø
PROM D

Z9 512x8 3624-4 PROM
Z10 512x8 3624-4 PROM
Z11 512x8 3624-4 PROM
Z12 512x8 3624-4 PROM
Z13 512x8 3624-4 PROM
Z14 512x8 3624-4 PROM
U15 256x4 2101 RAM
U16 256x4 2101 RAM

RP1,8

RP5 2.2K RES PACK

+5V

R30 2K

PBØ
1
2
3
4
5
6
7
WBØ
WB1
WB2
WB3
WB4
WB5
WB6
WB7
+5V

BAB 9
BAB 10
BAB 11
PSEL
VREF

U17 10F8 DECODE 74LS138

R29 2K Ω
+5V

R2 2K R3 2K — Q1 PN3644
R4 2K R5 2K — Q2 PN3644
R6 2K R7 2K — Q3 PN3644
R8 2K R9 2K — Q4 PN3644
R10 2K R11 2K — Q5 PN3644
R12 2K R13 2K — Q6 PN3644

READ
PSEL
U10 74LS02
PREAD

NOTES:
1. ALL +5V TO BE CONNECTED TO "C" REGULATOR.

QTY PER DASH NO.	PART OR IDENTIFYING NO.	INFOTON PART NO.	NOMENCLATURE OR DESCRIPTION	NOTE	ITEM NO.
			PARTS LIST		

MATERIAL

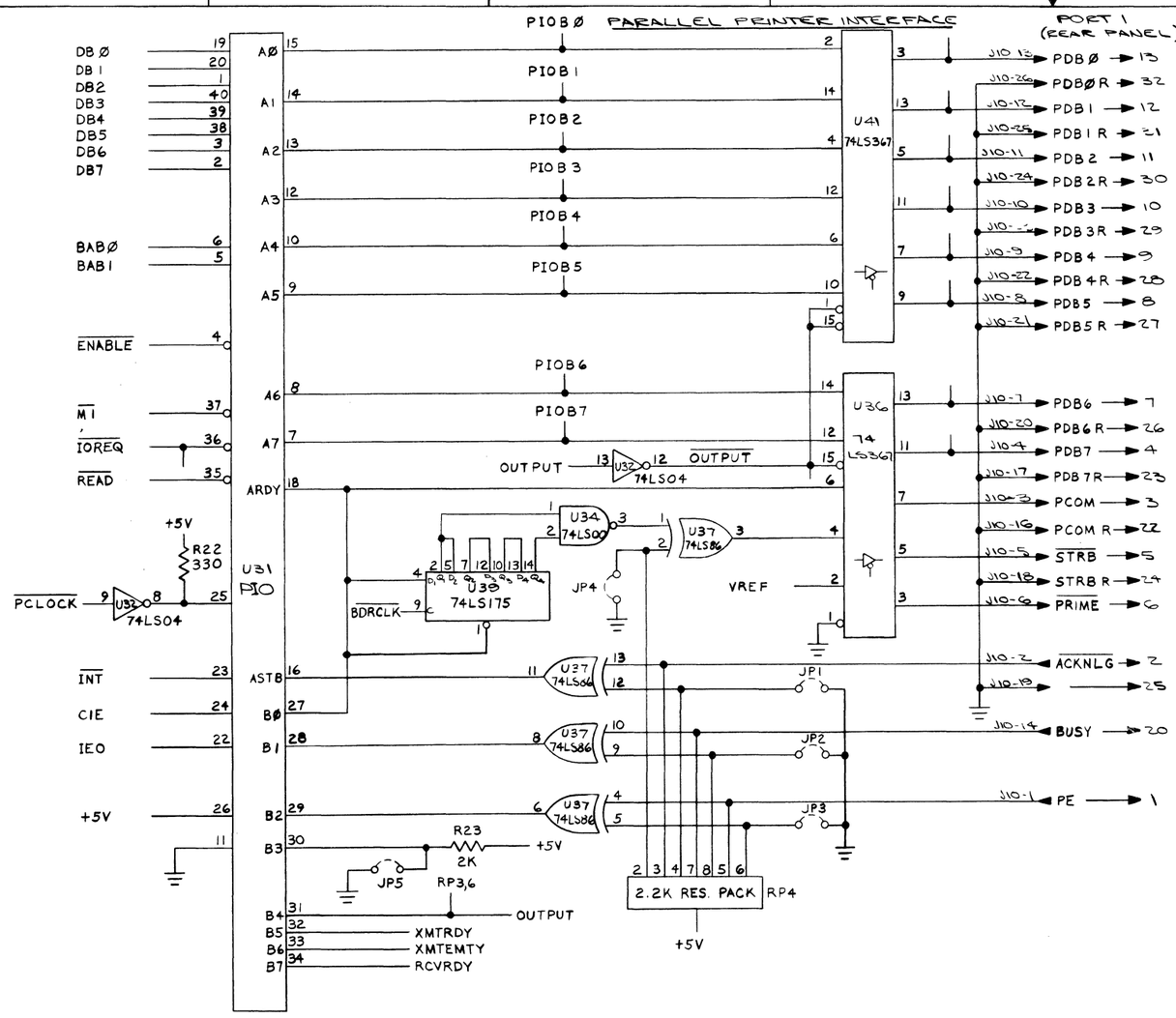
DR J. F. Eldridge
CHK [illegible] 9/30/77
APPD [illegible] 9/30/77
APPD

BUFFERED I/O PORT AND EXTENDED MEMORY OPTION GT400

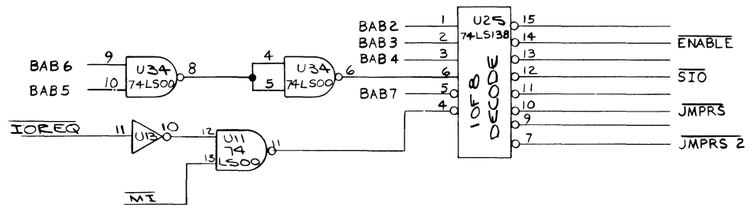
NEXT ASSEMBLY	PROJ. NO.	SCALE NONE	SIZE D	03277	REV E
			DATE 19 AUG 77	SHEET 3 OF 5	

PARALLEL PRINTER INTERFACE

REVISIONS			
SYM	ZONE	DESCRIPTION	DATE APPD
		SEE SHT 1	



	IN	OUT
JP1	LOW TRUE ACK. PULSE	HIGH TRUE ACK. PULSE
JP2	HIGH TRUE BUSY	LOW TRUE BUSY
JP3	HIGH TRUE PAPER EMPTY	LOW TRUE PAPER EMPTY
JP4	LOW TRUE OUTPUT STROBE	HIGH TRUE OUTPUT STROBE
JP5	NORMAL OUTPUT DATA	INVERTED OUTPUT DATA



QTY PER DASH NO.	PART OR IDENTIFYING NO.	INFOTON PART NO.	NOMENCLATURE OR DESCRIPTION	NOTE	ITEM NO.
PARTS LIST					

MATERIAL

DR J. L. Eldridge

CHK 7/6/77

APPD R.B. 7/30/77

APPD

BUFFERED I/O PORT AND EXTENDED MEMORY OPTION
GT400

NEXT ASSEMBLY | PROJ. NO. | SCALE NONE | SIZE D | 03277 | REV E | DATE 29 AUG 77 | SHEET 4 OF 5

REVISIONS			
SYM	ZONE	DESCRIPTION	DATE APPD
		SEE SHT 1	

SERIAL PRINTER INTERFACE

DB Ø
DB 1
DB 2
DB 3
DB 4
DB 5
DB 6
DB 7

READ
WRITE
SIO
BAB Ø
BDRCLK

RESET — U32 74LS04

U30 8251 USART

+5V
+12V
-12V

CR2 IN914
CR3 IN914

PORT 1 (REAR PANEL) CONN

U33 1488

J9-16 TXD → 22
J9-14 DTR → 20
J9-15 RTS → 21
J9-25 → 25

C6 330pf
C7 330pf
C8 330pf

U38 1489

J9-26 CTS → 32
J9-23 DSR → 29
J9-24 RXD → 30

R18 4.7K
R19 4.7K
R20 4.7K

C9 22pf
C10 22pf
C11 22pf

RCVRDY
XMTRDY
XMTEMTY

2.2K RES PACK RP1

JP6
JP7
JP8
JP9
JP10
JP11

U27 74LS367

DB5
DB4
DB7
DB1
DB2
DB0

JMPRS

	IN	OUT
JP 6	ODD/SPACE	EVEN/MARK
JP 7	GEN./CHECK PARITY	MARK/SPACE PARITY
JP 8	10 BIT	11 BIT
JP 9	CR ONLY AFTER DATA	LF&CR ALLOWED AFTER DATA
JP10	FF AT END OF PG/FLD	NO FF AT END OF PG/FLD
JP11	PARALLEL PRINTER	SERIAL PRINTER

PRINTER DELAY	JP14	JP13	JP12
CR&LF	20MILLS	10MILLS	5MILLS
VT & FF	40MILLS	20MILLS	10MILLS

EFFECT OF JP14 AND JP13 AND JP12 IS CUMULATIVE.

+5V — 2.2K RP3

JP12
JP13
JP14

U35 367

DB0
DB1
DB2
DB3

JMPS2

RP3,2 — R21 2K

J10-15 → 21 SELECT (USED FOR PARALLEL PRINTER)

U42 74LS86

JP15

+5V — RP2 2.2K RES. PACK

U29

BAUD RATE GEN U28 03171-001

+12V — C18 1µf

U32 74LS04

DRCLK

U34 74LS00

BDRCLK

QTY PER DASH NO.	PART OR IDENTIFYING NO.	INFOTON PART NO.	NOMENCLATURE OR DESCRIPTION	NOTE	ITEM NO.
PARTS LIST					

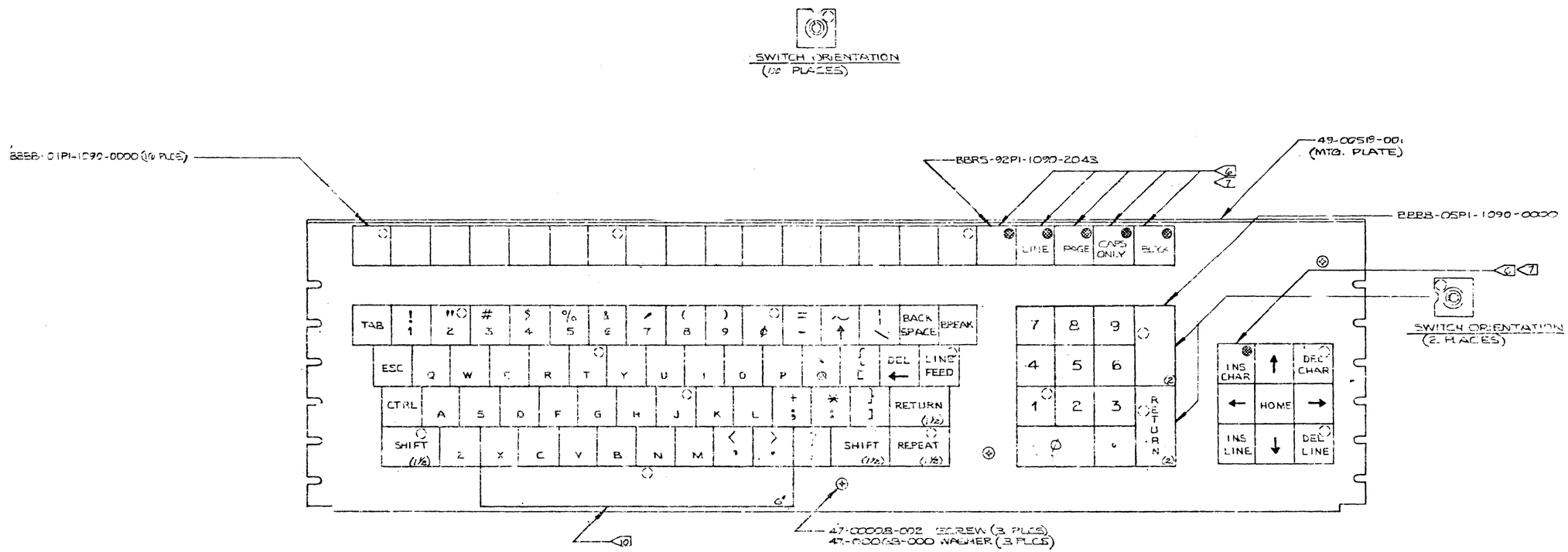
MATERIAL

DR J. L. Eldridge
CHK
APPD
APPD

BUFFERED I/O PORT AND EXTENDED MEMORY OPTION GT400

NEXT ASSEMBLY	PROJ. NO.	SCALE NONE	SIZE D	03277	REV E
			DATE 24 AUG 77	SHEET 5 OF 5	

OCT 0 6 1977



-003 MECH. ASSY & 66-01666-003 KEYTOP SET

(SEE SHEET 1 FOR ELECT. ASSY.)

NOTES:

10. 6 INCH SPACE BAR BBBB-12P1-1090-0000 WITH MECHANISM P/N'S 44-00176-000 (2 PL), 44-00074-000 (2 PL), & 44-00075-000
9. USE 47-00132-000 SCREW (16 PLACES) TO MOUNT PCB TO SWITCHES.
8. ALL SPRINGS ARE 45-00021-020 Z Ø/E.
7. INSTALL 42-00227-002 LIGHT SHIELD BETWEEN SWITCH & MOUNTING PLATE.
6. USE 21-00006-00 (6 PLACES) AS INDICATED.
5. ALL SWITCHES ARE (UNLESS NOTED) EXCEPT AS NOTED IN 6.
4. ALL SWITCHES ARE CENTERED.
3. KEYBOARD IS A 101 POSITION STEPPED.
2. APPLY APPROPRIATE DASH NO. AFTER KTC PART NUMBER.
1. APPLY DATE SEAL NO PRESSURE ADHESIVE TAG TO COMPONENT SIDE OF PCB.

ITEM	PART NO.	DESCRIPTION	QTY
CAGE	TITLE		

EFF.	REV.	ECO	BY	DESCRIPTION	APP.	DATE
—	—	—	DEJ	PROTO RELEASE		
—	—	—	RJB	PROD. REL.		

OCT 07 1977

ITEM	PART NO.	DESCRIPTION	QTY.

NOTICE OF PROPRIETARY INFORMATION
"INFORMATION CONTAINED HEREIN IS PROPRIETARY AND IS TRANSMITTED IN KEY TRONIC CORPORATION CONFIDENCE AND SHALL NOT BE REPRODUCED, THE RECIPIENT SHALL USE IT SOLELY TO EVALUATE THE PROPOSAL HEREBY FURNISHED OR AS OTHERWISE AUTHORIZED IN WRITING BY KEY TRONIC CORPORATION. ANY USE OF SUCH INFORMATION FOR PURPOSES OF INSPECTION, INSTALLATION, OR MAINTENANCE, OF THE EQUIPMENT SUPPLIED TO A SUPPLIER, IT SHALL BE LIMITED SOLELY TO THE PERFORMANCE OF WORK CONTRACTED FOR BY THIS COMPANY.
THIS INFORMATION SHALL NOT BE USED OR DISCLOSED BY THE RECIPIENT FOR ANY OTHER PURPOSE WHATSOEVER."

MANUFACTURE PARTS AND/OR ASSY'S PER K.T.C. DOCUMENT: FTP 36-790

UNLESS OTHERWISE NOTED ALL DIMENSIONS ARE IN INCHES
XXX DIMENSION NOT TO SCALE

TOL. EXCEPT AS NOTED
HOLE DIA.
FRACT. ± 1/64"
XX ± .01"
XXX ± .005"
ANG. ± 1°

USED ON: INFOTON 220

	RELEASED	
APD		
CH.		
DR.		7-11-77

SCALE —

TITLE: SCHEMATIC

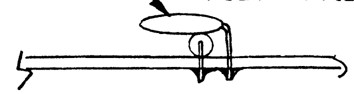
key tronic corporation
SPOKANE, WASH., U.S.A.

DWG. NO. 35-01763

SHEET 1 OF 1

EFF	REV	REC	ECO	BY	DESCRIPTION	APP	DATE
—	—	—	—	RJB	PROTO REL.		8/5/7
—	—	—	—	RJB	PROD. REL.		7/21/
—	A	—	3914 3979	DB	SEE ECO'S		10/5/7

INSTALL C9-C15 BY LAYING OVER R12-R18 WITH NON-PREPTED LONG LEADS AS SHOWN.

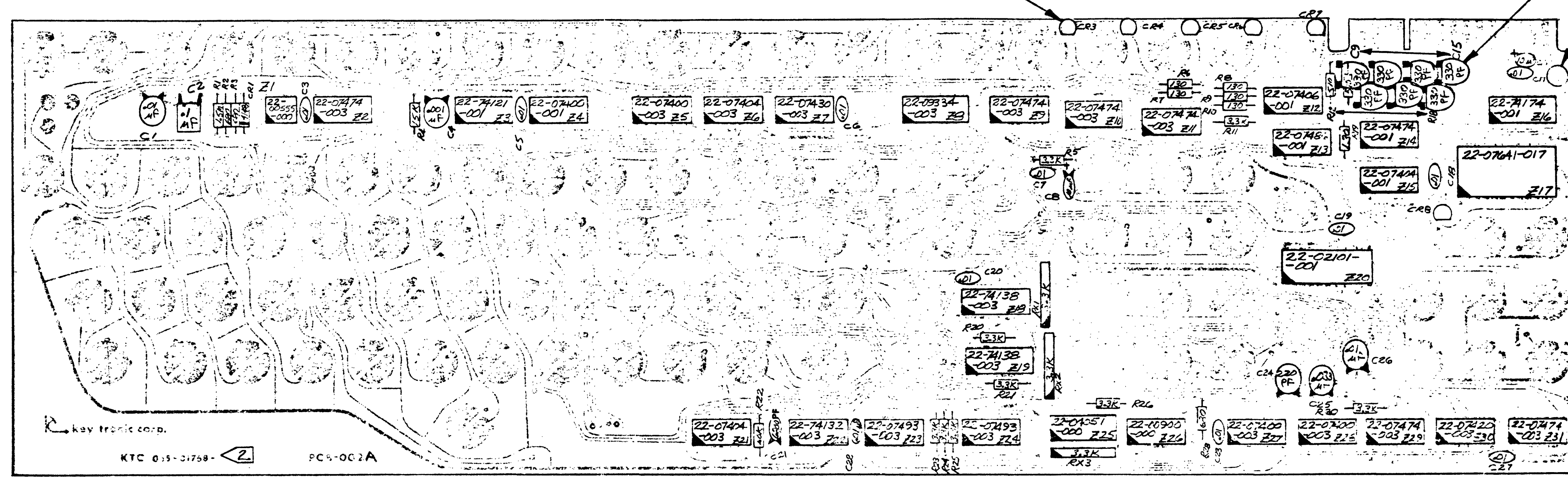


DETAIL I
(NO SCALE)

DO NOT INSTALL CR3 ON -003 ASSY
DO NOT INSTALL CR3 CR7 & CR8 ON -004 ASSY

47-00181-000
STANDOFF

SEE DETAIL I



-001, -003 & -004 ASSY
SEE SHEET 3 FOR MECH. & KEYTOPS

OCT 12 1977

4. APPLY APPROPRIATE DASH & REV. NUMBER AFTER CUSTOMERS P/N ON CIRCUIT SIDE OF PCB.
3. CAPACITOR VALUES ARE IN µF.
2. APPLY APPROPRIATE DASH NUMBER AFTER ... PART NUMBER.
1. APPLY DATE-SERIAL NO. PRESSURE ADHESIVE TAG TO COMPONENT SIDE OF PCB.

NOTES:

INFOTON

RJB 8-3-77

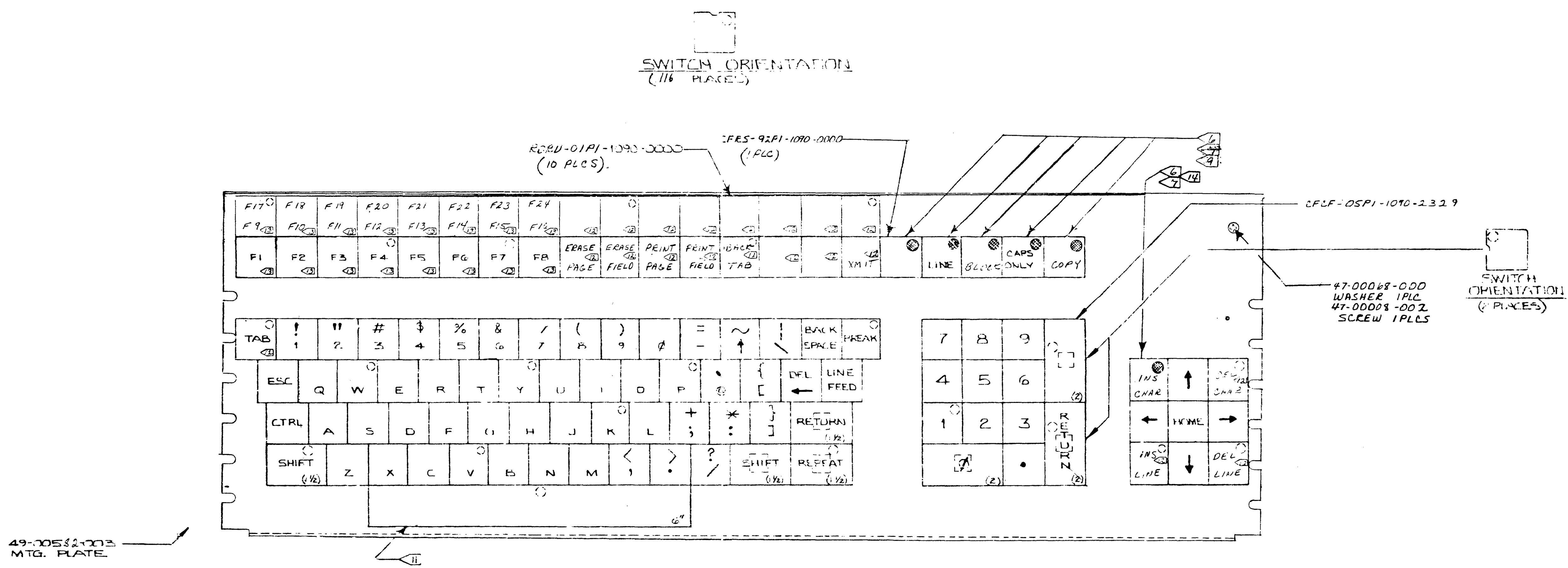
KEY BOARD ASSY.

key tronic corporation

65-01768

C

EFF.	REV.	ECO	BY	DESCRIPTION	APP.	DATE
—	—	—	R.B.	PROTO REL.		



-003 MECH. ASSY & 66-01767-003 KEYTOP SET

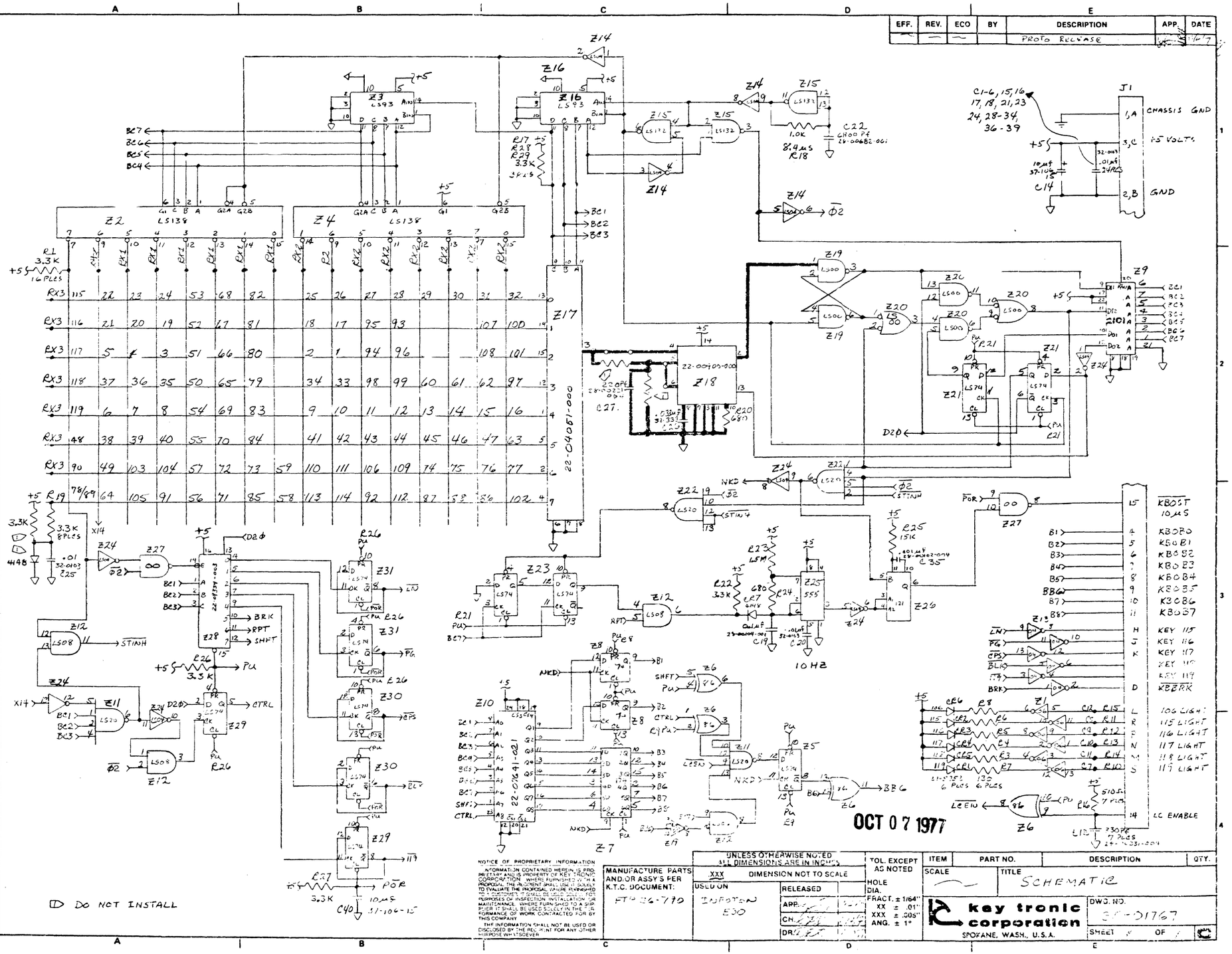
SEE SHEET 1 FOR ELECT. ASSY

14 USE 45-00024-060 60Z SPRING (1 PLC)
13 45-00021-040 40Z SPRING (17-PLACES).
12 45-00021-060 60Z SPRING (20 PLCS)
11 6 INCH SPACE BAR CFCF-12P1-1090-0000 WITH MECHANISM P/N'S 44-00076-000 LEG(2 PLCS), 44-00075-000 PLT, & 44-00074-000 MNT (2 PLCS).
10. USE 47-00192-000 SCREW (22 PLCS) TO MOUNT PCB. TO SWITCHES.
9 USE 45-00024-040 40Z (5 PLCS) IN LIGHTED KEY POSITIONS.
8 ALL SPRINGS ARE 45-00021-020 20Z EXCEPT AS NOTED IN 9 12 13 (76 PLCS)
7 INSTALL 48-00227-004 LIGHT SHIELD BETWEEN SWITCH & MOUNTING PLATE (6 PLCS).
6 USE 61-04005-001 SW (6 PLCS) IN LIGHTED KEY POSITIONS.
5 ALL SWITCHES ARE 61-04001-001 EXCEPT AS NOTED IN 6 (112 PLACES).
4. ALL SWITCHES ARE CENTERED.
3. KEYBOARD IS A LOW PROFILE STEPPED.
2. APPLY APPROPRIATE DASH NO. AFTER KTC PART NUMBER.
1. APPLY DATE-SERIAL NO. PRESSURE ADHESIVE TAG TO COMPONENT SIDE OF PCB.

MANUFACTURE PARTS AND/OR ASSY'S PER K.T.C. DOCUMENT	UNLESS OTHERWISE NOTED ALL DIMENSIONS ARE IN INCHES	TOL. EXCEPT AS NOTED	TITLE
M006, M007, M011	XXX DIMENSION NOT TO SCALE; USED ON: INFOTON	HOLE DIA. FRACT. ± 1/64"; XX ± .01"; XXX ± .005"; ANG ± 1°	KEYBOARD ASSY MECH. & KEYTOPS
	RELEASED; APP.; CH. JB; DR. R.B. 8/31	SCALE: ~	DWG NO 65-01767; SHEET OF; C

key tronic corporation
SPOKANE, WASH., U.S.A.

EFF.	REV.	ECO	BY	DESCRIPTION	APP.	DATE
—	—	—		PROTO RELEASE		10-7-77



MANUFACTURE PARTS AND/OR ASSYS PER K.T.C. DOCUMENT: FTP 26-770

USED ON: INFOTRON 530

UNLESS OTHERWISE NOTED ALL DIMENSIONS ARE IN INCHES
XXX DIMENSION NOT TO SCALE

RELEASED
APP.
CH.
DR.

TOL. EXCEPT AS NOTED
HOLE DIA.
FRACT. ± 1/64"
XX ± .01"
XXX ± .005"
ANG. ± 1°

ITEM	PART NO.	DESCRIPTION	QTY.

SCALE —

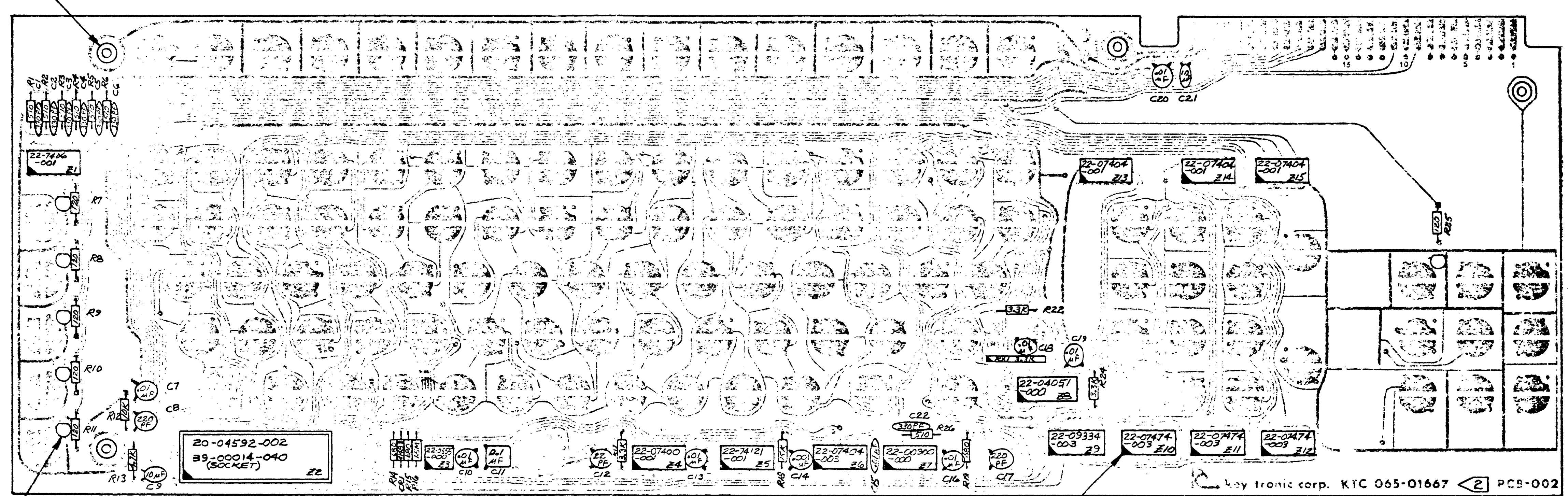
TITLE SCHEMATIC

key tronic corporation
SPOKANE, WASH., U.S.A.

DWG. NO. 37-01767

SHEET OF

EFF.	REV.	REC	ECO	BY	DESCRIPTION	APP	DAT
—	—	—	—	RJB	PROTO REL		4/1/77



-001 ASSY

(SEE SHEET 3 FOR MECH. & KEYTOP)

OCT 1 1977

NOTES:
1. APPLY APPROPRIATE DASH NUMBER AFTER KTC PART NUMBER.
2. APPLY DATE-SERIAL NO. PRESSURE ADHESIVE TAG TO COMPONENT SIDE OF PCB.

INFOTON INC.

M007

DR RJB 4-13-77

KEY BOARD ASSY. (ELECT. ASSY.)

key tronic corporation

SPOKANE, WASH. U.S.A.

65-01667

SHEET 1 OF

C

7. PARTS LIST

P.L03215-G01 REV. 3.HS1 USED ON: MODEL 400

SHT. 1 OF 6 TITLE: P.C. BOARD ASSY NEXT ASSY: 09400-G01

	BY	DATE	REV.	ECO	DATE	REV.	ECO	DATE	REV.	ECO	DATE	KITTING INFO.
DRAWN	[illegible]	6/24/77	A	—	—	E	1276	9/8/77	J	1314	10/17/77 KB	LOT NO.
CHECK	[illegible]	7/28/77	B	—	—	F	1292	9/8/77	K	1319	10/17/77 KB	QUAN. TO MAKE
APPD.	KB	7/28/77	C	—	—	G	1300	10/17/77 KB	1E	1325	10/17/77 KB	
RELEASE	[illegible]	7/28/77	D	REL	8/8/77	H	1309	10/17/77 KB	2E	1326	10/17/77 KB	QUANTITY

LINE	SIZE	PART NO.	REV.	DESCRIPTION	U/M	QUAN	KIT	ISU'D	SHOR
1	D	03215-000	3	P.C. BOARD ASSY		REF			
2	D	03213-000	S	SCHEMATIC		REF			
3									
4									
5									
6	D	03214-001	H	P.C. BOARD		1			
7									
8	P	01000-036		I.C. 1488 C11,L11		2			
9	"	-056		74S74 A10,A12,F9		3			
10		-059		74S04 B11		1			
11		-060		74S288		6*			
12		-067		1489 K12,M12		2			
13		-103		74LS74 D6,		5			
14				D7,E11, H9,H12					
15		-104		74LS157 J11		1			
16		-105		74LS163 A9,		5			
17				A11,B9,C8,F10					
18		-107		74LS174 A6,		3			
19				F6,F8					
20		-108		74LS175 C6,		3			
21				C9,E8					
22		-115		74LS257 L9,		4			
23				A1,B3,M9					
24		-116		9602 H11		1			
25		-117		74LS367 C3,		10			
26				D3,F3,H3,J1,J2,J6,					
27				K4,L4,M4					
28		-118		74LS00 C10,		4			
29				F5,F12,K10					
30		-119		74LS04 B8,		7			
31	"	"		E9,H7,J7,J8,J10,L10					
	P	01000-120		I.C. 74LS10 D10,H8		2			

PL03215-G01 REV. 3HS3 USED ON: MODEL 400

SHT. 2 OF 6 TITLE: P.C. BOARD ASSY NEXT ASSY: _____

	BY	DATE	REV.	ECO	DATE	REV.	ECO	DATE	REV.	ECO	DATE	KITTING INFO.
DRAWN	[illegible]	6/26/77	ZEE	1327	10/31/77	-	1309C	2/13/78	ZEJ	1415	3/1/78 KB	LOT NO.
CHECK	LAD	7/28/77	4EF	1332	12/5/77	6EG	1360A		1FK	1429	3/7/78	QUAN. TO MAKE
APPD.	KB	7/28/77	5EG	1341	1/3/78	7EG	1385		2FL	1448A	6/23/78	
RELEASE	[illegible]	7/28/77	—	1309B	2/15/78	8EW	1353	2/16/78	3FM	1469A	6/23/78	QUANTITY

LINE	SIZE	PART NO.	REV.	DESCRIPTION	U/M	QUAN	KIT	ISU'D	SHOR
1	P	01000-124		IC 74LS26 M11		1			
2	P	01000-122		IC 74LS51 J12,P9		2			
3	↑	-025		7426 E12		1			
4		-126		74LS02 D8,		3			
5				H6, H10					
6		-132		74LS86 M10		1			
7		-135		74LS393 E10		1			
8		-042		74166 E7		1			
9		-137		74LS83 B4, C4		2			
10		-139		74LS85 A5,		3			
11				B5, C5					
12		-140		74LS273 A8,		3			
13				B6, E3					
14		-141		74LS138 H5,		3			
15				J3, J5					
16	↓	-153		8216 L5, M5		2			
17	P	01000-113		I.C. 74S86 D11		1			
18		01000-085		IC. 74S00 D9		1			
19	↑								
20									
21		01006-008		TRANS MM3009 Q6,Q7		2			
22		-012		VOLTAGE REG 7812 VR5		1			
23		-014		VOLTAGE REG 7912 VR7		1			
24		-019		TRANS 2N4901 Q1, Q18		2			
25		-020		VOLTAGE REG 7805 VR1,		4			
26				VR2, VR3, VR4					
27		-021		VOLTAGE REG 7815 VR6		1			
28		-022		TRANS PN3643 Q2,		2			
29				Q17,					
30		-023		TRANS PN3644 Q3, Q4,		11			
31	↓			Q5, Q9 THRU Q16					
32	P	01006-024		TRANS 2N5401 Q8		1			

PL03215-G01 REV. 3HS USED ON: MODEL 400

SHT. 3 OF 6 TITLE: P.C. BOARD ASSY NEXT ASSY: _____

	BY	DATE	REV.	ECO	DATE	REV.	ECO	DATE	REV.	ECO	DATE	KITTING INFO.
DRAWN	WLB	6/27/79	AFN	1485A	7/11/79 WLB	IGS	1538	2-6-79	3HS	1695	8-1-79	LOT NO.
CHECK	CAD	7/24/79	SFP	1503	11/1/78 WLB	2GS	1564	2-7-79				QUAN. TO MAKE
APPD.	KB	7/24/79	GFB	1514A	11/1/78 WLB	3FS	1695	8-1-79				
RELEASE	SN	7/24/79	TFS	1525	11/1/78 WLB	3GS	1695	8-1-79				QUANTITY

LINE	SIZE	PART NO.	REV.	DESCRIPTION	U/M	QUAN	KIT	ISU'D	SHOR
1	P	01007-008		DIODE IN914 | CR3,		11			
2	↑	↑		CR4, CR5, CR6, CR7,		↑			
3				CR8, CR9, CR10, CR11,					
4		↓		CR15, CR14					
5		01007-010		DIODE IN5353 | CR13		1			
6									
7									
8		01008-011		CAP. 22 Mf | C23, C25, C36		3			
9		↑ -072		↑ 22 Pf | C12, C13,		6			
10				C14, C15, C21, C22					
11		-073		1 Mf | C41, C35 C39, C40,		4			
12		-074		10 Pf C24, C26, C34		3			
13		-096		2300 Mf, 30V | C7,		2			
14				C8					
15		-083		25 Mf, 25V | C1, C2,		9			
16				C3, C4, C5, C6,					
17		↓		↓ C10, C11, C37					
18									
19		01008-090		CAP. 330 Pf | C16, C17,		6			
20				C18, C19, C20, C30					
21									
22									
23		01009-034		RES PACK 2.2K | RP1		9			
24				THRU RP9					
25		01009-040		RES. 3Ω, 10W | R4		1			
26		01009-028		RES. .33Ω, 7W | R3		1			
27									
28									
29		01017-026		SWITCH 8 POS | K9, K11		2			
30		01017-026		SWITCH 8 POS | A2, A3		2	**		
31	↓								
32	P	01009-065		RES. 390Ω | R80		1			

PL03215-G01 REV. 3HS USED ON: MODEL 400

SHT. 4 OF 6 TITLE: P.C. BOARD ASSY NEXT ASSY: _____

	BY	DATE	REV.	ECO	DATE	REV.	ECO	DATE	REV.	ECO	DATE	KITTING INFO.
DRAWN	WJB	6/27/77										LOT NO.
CHECK	[illegible]	7/28/77										QUAN. TO MAKE
APPD.	KB	7/28/77										
RELEASE	SM	7/28/77										QUANTITY

LINE	SIZE	PART NO.	REV.	DESCRIPTION	U/M	QUAN	KIT	ISU'D	SHORT
1	P	01021-007		CONN 12 PIN WAFERCON		1			
2	↓	↓ -077		CONN 30 PIN HEADER		1			
3		↓ -078		CONN 34 PIN HEADER		3			
4		01021-086		CONN 6 PIN WAFERCON		1			
5		01029-015		SOCKET 28 PIN | M6&7		1			
6		01029-004		SOCKET 24 PIN | Z1-Z8 D4, F4		10			
7		01029-013		SOCKET 16 PIN | K9, K11 A2, A3		4			
8		01029-010		SOCKET 40 PIN | LM, N9 & P4 & P5		2			
9		01030-009		CRYSTAL 24.0408 MHZ | Y1		1			
10		01029-006		SOCKET 14 PIN | J9		1			
11		01034-015		BRIDGE RECT. VH247 | CR1		2			
12				CR2					
13		01035-005		WASHER, FIBER		2			
14		01035-013		STAND OFF		2			
15		01035-018		CRADLE MOUNT		2			
16		01038-001		I.C. MCT-2 | P10		2	***		
17				N10					
18	↓	01042-006		CABLE TIE		2			
19	P	01048-001		SPEAKER		1			
20									
21	S	03200-001		Z80 CPU | P4 & P5		1			
22	↓	03202-001		Z80 PIO | L, M, N9		1			
23		03203-001		USART | M6 & 7		1			
24		03204-001		1K x 1 RAM | U1 THRU U16		16			
25	↓	03205-001		256 x 4 RAM | H4, J4		2			
26	S	03171-001		I.C. · BAUD RATE		1			
27				GEN | J9					
28									
29	P	99999-122		HEAT SINK		4			
30	↓	↓ -144		TERMINAL BLOCK		1			
31	↓	↓ -169		HEAT SINK		6			
32	P	99999-182		HEAT SINK		1			

PL03215-G01 REV. 3HS USED ON: MODEL 400

SHT. 5 OF 6 TITLE: P.C. BOARD ASSY NEXT ASSY: _____

	BY	DATE	REV.	ECO	DATE	REV.	ECO	DATE	REV.	ECO	DATE	KITTING INFO.
DRAWN	WHB	6/27/77										LOT NO.
CHECK	CAD	7/28/77										QUAN. TO MAKE
APPD.	KB	7/28/77										
RELEASE	SR	7/28/77										QUANTITY

LINE	SIZE	PART NO.	REV.	DESCRIPTION	U/M	QUAN	KIT	ISU'D	SHORT
1	P	01009-096		RES. 68K R11		1			
2									
3		-080		4.7K R5, R6, R7,		8			
4				R33, R8, R9, R13, R64					
5									
6		-064		330Ω R23		4			
7				R38, R63, R79					
8		-087		10K R41,		1			
9									
10		-070		1K R89 R30,		5			
11				R31, R90 R81					
12		-062		220Ω R26		1			
13		-091		22K R12		1			
14		-088		12K R35, R34		2			
15		-094		39K R10		1			
16		-058		120Ω R78		1			
17		-056		75Ω R82		1			
18		-082		5.6K R37		1			
19		01009-074		RES 2K R14 THRU R15,		34			
20				R19 THRU R22, R39, R40, R42,					
21				R91, R24, R45 THRU R62, R66					
22				THRU R68, R83, R88					
23		01009-041		RES 200Ω 5W R87		1			
24	P	01009-112		RES 10Ω JP1 THRU JP7,		10			
25				R25 R18, JP10					
26	P	01009-068		RES. 680Ω R32, R76		2			
27	P	01009-053		RES 51 R29		1			
28	D	03211-001		REAR BEZEL		1			
29	D	03222-001		DECAL		1			
30	P	01035-016		STAND OFF		2			
31	P	01009-097		RES 75K R36		1			
2	P	01009-066		RES 470 R77		1			

PL03215-G01 REV. 3HS USED ON: MODEL 400

SHT. 6 OF 6 TITLE: P.C. BOARD ASSY NEXT ASSY:

	BY	DATE	REV.	ECO	DATE	REV.	ECO	DATE	REV.	ECO	DATE	KITTING INFO.
DRAWN	WHB	6/27/77										LOT NO.
CHECK	CAD	7/20/77										QUAN. TO MAKE
APPD.	KB	7/28/77										
RELEASE	[illegible]	7/28/77										QUANTITY

LINE	SIZE	PART NO.	REV.	DESCRIPTION	U/M	QUAN	KIT	ISU'D	SHORT
1	S	02971-000		PROM (512 x 8) Z1 THRU Z8		8			
2	|	02999-032		9 x 9 U.C. CHAR GEN F4		1			
3	|	02999-XXX		9 x 9 L.C. CHAR GEN E4		1	***		
4	|	02484-042		VID CHAR CONT (60 Hz) C7		1*			
5	|	02484-051		VIDEO SLICE CNTR F7		1*			
6	|	02484-054		VIDEO LINE COUNTER		1*			
7	|			(60 HZ) B7					
8	|	02484-056		VIDEO LINE COUNTER		1*			
9	|			(50 HZ) A7					
10	|	02484-041		LAR A4		1*			
11	S	02484-036A		VIDEO CONTROL E6		1*			
12									
13									
14									
15									
16									
17									
18									
19									
20		NOTE:							
21	1.	* ITEM'S 4, 5, 6, 8, 10, 11 OF THIS			SHEET		TO BE PURCHASE		
22		AS BLANK PROM'S PER ITEM			11	OF	SHT 1.		
23									
24	2.	** REFER TO CONFIGUEATION DRAWING FOR							
25		PROPER ASSEMBLY LEVEL PER THE							
26		PRODUCT LOG.							
27	3.	*** P1Ø USE FAIRCHILD IL-1 ONLY							
28	4.	**** REFER TO PRODUCT LOG FOR							
29		PROM CONFIGURATION							
30									
31									
32									

APPENDIX

E10, E20, E30 KEYBOARD GENERATED CODES

Bits	Bits 7654															
3210	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1110
0000	c@ (C,CS)	cP (C,CS)	SPACE	Ø ØNP (NS,C) (ALL)	@	P	`	p	K1 (ALL)	K7 (ALL)		Ø (S,CS)	K17 (NS,C)	K17 (S,CS)		
0001	cA (C,CS)	cQ (C,CS)	!	1	A	Q	a	q	K2 (ALL)		INS CHAR (ALL)		K18 (NS,C)	K18 (S,CS)		
0010	cB (C,CS)	cR (C,CS)	"	2	B	R	b	r	K3 (ALL)		DEL CHAR (ALL)		K19 (NS,C)	K19 (S,CS)		
0011	cC (C,CS)	cS (C,CS)	#	3	C	S	c	s	K4 (ALL)	K16 (ALL)	INS LINE (ALL)		K20 (NS,C)	K20 (S,CS)		
0100	cD (C,CS)	cT (C,CS)	$	4	D	T	d	t	K5 (ALL)		DEL LINE (ALL)		K21 (NS,C)	K21 (S,CS)		
0101	cE (C,CS)	cU (C,CS)	%	5	E	U	e	u		K8 (ALL)			K22 (NS,C)	K22 (S,CS)		
0110	cF (C,CS)	cV (C,CS)	&	6	F	V	f	v	K6 (ALL)	K9 (ALL)			K23 (NS,C)	K23 (S,CS)		
0111	cG (C,CS)	cW (C,CS)	'	7	G	W	g	w					K24 (NS,C)	K24 (S,CS)		
1000	cH (C,CS)	cX (C,CS)	(	8	H	X	h	x	K109 BSP ← (ALL) (ALL)	K10 (ALL)	K93 (ALL)		K25 (NS,C)	K25 (S,CS)		
1001	cI TAB (C,CS) (ALL)	cY (C,CS)	)	9	I	Y	i	y		→ (ALL)			K26 (NS,C)	K26 (S,CS)		
1010	cJ LF (C,CS) (ALL)	cZ (C,CS)	. (S)	: (NS)	J	Z	j	z		HOME (ALL)	* (CS)	: (C)	K27 (NS,C)	K27 (S,CS)		
1011	cK (C,CS)	c[(C,CS)	+ (S)	; (NS)	K	[	k	{	K13 (ALL)	ESC (ALL)	+ (CS)	; (C)	K28 (NS,C)	K28 (S,CS)		
1100	cL (C,CS)	c\ (C,CS)	(NS)	< (S)	L	\	l	|		↑ (ALL)	, (C)	< (CS)	K29 (NS,C)	K29 (S,CS)		
1101	cM CR (C,CS) (ALL)	c] (C,CS)	–	=	M	]	m	}	K92 RETURN (ALL)	↓ (ALL)			K30 (NS,C)	K30 (S,CS)		
1110	cN (C,CS)	c↑ (C,CS)	. (NS)	> (S)	N	↑	n	~	K14 (NS,C)	K11 (ALL)	. (C)	> (CS)	K31 (NS,C)	K31 (S,CS)	K14 (S,CS)	
1111	cO (C,CS)	c← (C,CS)	/ (NS)	? (S)	O	←	o	DEL	K15 (NS,C)	K12 (ALL)	/ (C)	? (CS)	K32 (NS,C)	K32 (S,CS)	K15 (S,CS)	

ns = non shift
s = shift
c = control
cs = control shift
all = all of the above four modes
bit 7 = indicates a general code to be converted by the keyboard translator prom

This page intentionally left blank

256 BIT PROM P.N. 02484-030

MNEMONIC	ERLC	SCLK3	SCLK2	SCLK1	SCLK0			ELC							
PIN	14	13	12	11	10	15		9	7	6	5	4	3	2	1
INPUT							OUTPUT								
BIT	A4	A3	A2	A1	A0	ENB	Word	B7	B6	B5	B4	B3	B2	B1	B0
	0	0	0	0	0	0	0	0			0	0	0	0	1
	0	0	0	0	1	0	1	0			0	0	0	1	0
	0	0	0	1	0	0	2	0			0	0	0	1	1
	0	0	0	1	1	0	3	0			0	0	1	0	0
	0	0	1	0	0	0	4	0			0	0	1	0	1
	0	0	1	0	1	0	5	0			0	0	1	1	0
	0	0	1	1	0	0	6	0			0	0	1	1	1
	0	0	1	1	1	0	7	0			1	0	0	0	0
	0	1	0	0	0	0	8	1			0	1	0	0	1
	0	1	0	0	1	0	9	0			0	0	0	0	0
	0	1	0	1	0	0	10	0			0	0	0	0	0
	0	1	0	1	1	0	11	0			0	0	0	0	0
	0	1	1	0	0	0	12	0			0	0	0	0	0
	0	1	1	0	1	0	13	0			0	0	0	0	0
	0	1	1	1	0	0	14	0			0	0	0	0	0
	0	1	1	1	1	0	15	0			0	0	0	0	0
	1	0	0	0	0	0	16	0			0	0	0	0	1
	1	0	0	0	1	0	17	0			0	0	0	1	0
	1	0	0	1	0	0	18	0			0	0	0	1	1
	1	0	0	1	1	0	19	0			0	0	1	0	0
	1	0	1	0	0	0	20	0			0	0	1	0	1
	1	0	1	0	1	0	21	0			0	0	1	1	0
	1	0	1	1	0	0	22	0			0	0	1	1	1
	1	0	1	1	1	0	23	0			0	1	0	0	0
	1	1	0	0	0	0	24	0			0	1	0	0	1
	1	1	0	0	1	0	25	0			0	1	0	1	0
	1	1	0	1	0	0	26	0			0	1	0	1	1
	1	1	0	1	1	0	27	0			0	1	1	0	0
	1	1	1	0	0	0	28	0			0	1	1	0	1
	1	1	1	0	1	0	29	0			0	1	1	1	0
	1	1	1	1	0	0	30	1			0	1	1	1	1
	1	1	1	1	1	0	31	0			0	0	0	0	0
	X	X	X	X	X	1	ALL								

GT400 Video Slice Counter
GT400 Location F7

256 BIT PROM P.N. 02484-036A

	MNEMONIC CONT. CODE	ELC	CCOMP	RAM6	RAM5						$\overline{\text{UCE}}$	$\overline{\text{CURUB}}$	$\overline{\text{VIDE}}$	$\overline{\text{VSRR}}$	USK3	$\overline{\text{LCE}}$
PIN	14	13	12	11	10	15		9	7		6	5	4	3	2	1
INPUT							OUTPUT									
BIT	A4	A3	A2	A1	A0	ENB	Word	B7	B6		B5	B4	B3	B2	B1	B0
	0	0	0	0	0	0	0	0	0		0	1	0	1	0	1
	0	0	0	0	1	0	1	0	0		0	1	0	1	1	1
	0	0	0	1	0	0	2	0	0		0	1	0	1	0	1
	0	0	0	1	1	0	3	0	0		1	1	0	1	0	0
	0	0	1	0	0	0	4	0	0		0	1	0	1	0	1
	0	0	1	0	1	0	5	0	0		0	1	0	1	1	1
	0	0	1	1	0	0	6	0	0		0	1	0	1	0	1
	0	0	1	1	1	0	7	0	0		1	1	0	1	0	0
	0	1	0	0	0	0	8	0	0		1	1	0	0	0	1
	0	1	0	0	1	0	9	0	0		1	1	1	0	1	1
	0	1	0	1	0	0	10	0	0		1	1	1	0	0	1
	0	1	0	1	1	0	11	0	0		1	1	0	1	0	0
	0	1	1	0	0	0	12	0	0		1	0	1	0	0	1
	0	1	1	0	1	0	13	0	0		1	0	1	0	1	1
	0	1	1	1	0	0	14	0	0		1	0	1	0	0	1
	0	1	1	1	1	0	15	0	0		1	0	1	0	0	1
	1	0	0	0	0	0	16	0	0		1	1	1	1	0	1
	1	0	0	0	1	0	17	0	0		0	1	0	1	1	1
	1	0	0	1	0	0	18	0	0		0	1	0	1	0	1
	1	0	0	1	1	0	19	0	0		1	1	0	1	0	0
	1	0	1	0	0	0	20	0	0		1	1	1	1	0	1
	1	0	1	0	1	0	21	0	0		0	1	0	1	1	1
	1	0	1	1	0	0	22	0	0		0	1	0	1	0	1
	1	0	1	1	1	0	23	0	0		1	1	0	1	0	0
	1	1	0	0	0	0	24	0	0		1	1	1	0	0	1
	1	1	0	0	1	0	25	0	0		1	1	1	0	1	1
	1	1	0	1	0	0	26	0	0		1	1	1	0	0	1
	1	1	0	1	1	0	27	0	0		1	1	0	1	0	0
	1	1	1	0	0	0	28	0	0		1	0	1	0	0	1
	1	1	1	0	1	0	29	0	0		1	0	1	0	1	1
	1	1	1	1	0	0	30	0	0		1	0	1	0	0	1
	1	1	1	1	1	0	31	0	0		1	0	1	0	0	1
	X	X	X	X	X	1	ALL									

GT400 Video Control
GT400 Location E6

256 BIT PROM P.N. 02484-041

	MNEMONIC	VLC4	VLC3	VLC2	VLC1	VLC0									
PIN		14	13	12	11	10	15		9	7	6	5	4	3	2	1
	INPUT							OUTPUT								
BIT		A4	A3	A2	A1	A0	ENB	Word	B7	B6	B5	B4	B3	B2	B1	B0
		0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
		0	0	0	0	1	0	1	0	0	0	0	1	0	0	0
		0	0	0	1	0	0	2	0	0	0	0	1	1	0	1
		0	0	0	1	1	0	3	0	0	0	1	0	1	1	0
		0	0	1	0	0	0	4	0	0	0	1	0	1	1	1
		0	0	1	0	1	0	5	0	0	0	1	1	0	0	0
		0	0	1	1	0	0	6	0	0	1	0	0	1	0	1
		0	0	1	1	1	0	7	0	0	1	0	0	0	1	0
		0	1	0	0	0	0	8	0	0	1	0	1	0	1	1
		0	1	0	0	1	0	9	0	0	1	1	0	1	0	0
		0	1	0	1	0	0	10	0	0	1	1	0	0	0	1
		0	1	0	1	1	0	11	0	0	1	1	1	1	1	0
		0	1	1	0	0	0	12	0	0	1	1	1	1	1	1
		0	1	1	0	1	0	13	0	1	0	0	0	0	0	0
		0	1	1	1	0	0	14	0	1	0	0	1	1	0	1
		0	1	1	1	1	0	15	0	1	0	0	1	0	1	0
		1	0	0	0	0	0	16	0	1	0	1	0	0	1	1
		1	0	0	0	1	0	17	0	1	0	1	1	1	0	0
		1	0	0	1	0	0	18	0	1	0	1	1	0	0	1
		1	0	0	1	1	0	19	0	1	1	0	0	1	1	0
		1	0	1	0	0	0	20	0	1	1	0	0	1	1	1
		1	0	1	0	1	0	21	0	1	1	0	1	0	0	0
		1	0	1	1	0	0	22	0	1	1	1	0	1	0	1
		1	0	1	1	1	0	23	0	1	1	1	0	0	1	0
		1	1	0	0	0	0	24	0	1	1	1	1	0	1	1
		1	1	0	0	1	0	25	0	0	0	0	0	0	0	0
		1	1	0	1	0	0	26	0	0	0	0	0	0	0	0
		1	1	0	1	1	0	27	0	0	0	0	0	0	0	0
		1	1	1	0	0	0	28	0	0	0	0	0	0	0	0
		1	1	1	0	1	0	29	0	0	0	0	0	0	0	0
		1	1	1	1	0	0	30	0	0	0	0	0	0	0	0
		1	1	1	1	1	0	31	0	0	0	0	0	0	0	0
		X	X	X	X	X	1	ALL								

GT400 Line Address Register
GT400 Location A4

256 BIT PROM P.N. 02484-042

	MNEMONIC	VCC5	VCC4	VCC3	VCC2	VCC1	$\overline{VCC6}$						$\overline{HSYNC}$	$\overline{HDRIVE}$	$\overline{HBLANK}$	$\overline{VC79}$	$\overline{EOL}$	
PIN		14	13	12	11	10	15		9	7	6	5	4	3	2	1		
	INPUT							OUTPUT										
BIT		A4	A3	A2	A1	A0	ENB	Word	B7	B6	B5	B4	B3	B2	B1	B0	Character	
		0	0	0	0	0	0	0				1	1	1	1	1	64	
		0	0	0	0	1	0	1				1	1	1	1	1	66	
		0	0	0	1	0	0	2				1	1	1	1	1	68	
		0	0	0	1	1	0	3				1	1	1	1	1	70	
		0	0	1	0	0	0	4				1	1	1	1	1	72	
		0	0	1	0	1	0	5				1	1	1	1	1	74	
		0	0	1	1	0	0	6				1	1	1	1	1	76	
		0	0	1	1	1	0	7				1	1	1	0	1	78	
		0	1	0	0	0	0	8				1	1	0	1	1	80	
		0	1	0	0	1	0	9				1	1	0	1	1	82	
		0	1	0	1	0	0	10				1	0	0	1	1	84	
		0	1	0	1	1	0	11				1	0	0	1	1	86	
		0	1	1	0	0	0	12				0	0	0	1	1	88	
		0	1	1	0	1	0	13				0	0	0	1	1	90	
		0	1	1	1	0	0	14				0	0	0	1	1	92	
		0	1	1	1	1	0	15				0	0	0	1	1	94	
		1	0	0	0	0	0	16				0	0	0	1	1	96	
		1	0	0	0	1	0	17				1	0	0	1	1	98	
		1	0	0	1	0	0	18				1	0	0	1	1	100	
		1	0	0	1	1	0	19				1	0	0	1	1	102	
		1	0	1	0	0	0	20				1	0	0	1	0	104	
		1	0	1	0	1	0	21				1	0	0	1	0	106	
		1	0	1	1	0	0	22				1	0	0	1	0	108	
		1	0	1	1	1	0	23				1	0	0	1	0		
		1	1	0	0	0	0	24				1	0	0	1	0		
		1	1	0	0	1	0	25				1	0	0	1	0		
		1	1	0	1	0	0	26				1	0	0	1	0		
		1	1	0	1	1	0	27				1	0	0	1	0		
		1	1	1	0	0	0	28				1	0	0	1	0		
		1	1	1	0	1	0	29				1	0	0	1	0		
		1	1	1	1	0	0	30				1	0	0	1	0		
		1	1	1	1	1	0	31										
		X	X	X	X	X	1	ALL										

GT400 Video Character Counter
GT400 Location C7

256 BIT PROM P.N. 02484-043

MNEMONIC								ERLC	$\overline{\text{VBLANK}}$	$\overline{\text{VDRIVE}}$	$\overline{\text{NL4}}$	$\overline{\text{NL3}}$	$\overline{\text{NL2}}$	$\overline{\text{NL1}}$	$\overline{\text{NL0}}$
PIN	14	13	12	11	10	15		9	7	6	5	4	3	2	1
INPUT							OUTPUT								
BIT	A4	A3	A2	A1	A0	ENB	Word	B7	B6	B5	B4	B3	B2	B1	B0
	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0
	0	0	0	0	1	0	1	0	1	1	1	1	1	0	1
	0	0	0	1	0	0	2	0	1	1	1	1	1	0	0
	0	0	0	1	1	0	3	0	1	1	1	1	0	1	1
	0	0	1	0	0	0	4	0	1	1	1	1	0	1	0
	0	0	1	0	1	0	5	0	1	1	1	1	0	0	1
	0	0	1	1	0	0	6	0	1	1	1	1	0	0	0
	0	0	1	1	1	0	7	0	1	1	1	0	1	1	1
	0	1	0	0	0	0	8	0	1	1	1	0	1	1	0
	0	1	0	0	1	0	9	0	1	1	1	0	1	0	1
	0	1	0	1	0	0	10	0	1	1	1	0	1	0	0
	0	1	0	1	1	0	11	0	1	1	1	0	0	1	1
	0	1	1	0	0	0	12	0	1	1	1	0	0	1	0
	0	1	1	0	1	0	13	0	1	1	1	0	0	0	1
	0	1	1	1	0	0	14	0	1	1	1	0	0	0	0
	0	1	1	1	1	0	15	0	1	1	0	1	1	1	1
	1	0	0	0	0	0	16	0	1	1	0	1	1	1	0
	1	0	0	0	1	0	17	0	1	1	0	1	1	0	1
	1	0	0	1	0	0	18	0	1	1	0	1	1	0	0
	1	0	0	1	1	0	19	0	1	1	0	1	0	1	1
	1	0	1	0	0	0	20	0	1	1	0	1	0	1	0
	1	0	1	0	1	0	21	0	1	1	0	1	0	0	1
	1	0	1	1	0	0	22	0	1	1	0	1	0	0	0
	1	0	1	1	1	0	23	0	1	1	0	0	1	1	1
	1	1	0	0	0	0	24	0	0	1	0	0	1	1	0
	1	1	0	0	1	0	25	0	0	1	0	0	1	1	0
	1	1	0	1	0	0	26	0	0	1	0	0	1	1	0
	1	1	0	1	1	0	27	0	0	1	0	0	1	1	0
	1	1	1	0	0	0	28	0	0	1	0	0	1	1	0
	1	1	1	0	1	0	29	0	0	1	0	0	1	1	0
	1	1	1	1	0	0	30	0	0	1	0	0	1	1	0
	1	1	1	1	1	0	31	1	1	1	1	1	1	1	1
	X	X	X	X	X	1	ALL								

GT400 60 Hz Video Line Counter
GT400 Location B7

256 BIT PROM P.N. 02484-044

	MNEMONIC	VLC4	VLC3	VLC2	VLC1	VLC0			ERLC	$\overline{\text{VBLANK}}$	$\overline{\text{VDRIVE}}$	$\overline{\text{NL4}}$	$\overline{\text{NL3}}$	$\overline{\text{NL2}}$	$\overline{\text{NL1}}$	$\overline{\text{NL0}}$
PIN		14	13	12	11	10	15		9	7	6	5	4	3	2	1
INPUT								OUTPUT								
BIT		A4	A3	A2	A1	A0	ENB	Word	B7	B6	B5	B4	B3	B2	B1	B0
		0	0	0	0	0	0	0	0	1	1	1	1	1	1	0
		0	0	0	0	1	0	1	0	1	1	1	1	1	0	1
		0	0	0	1	0	0	2	0	1	1	1	1	1	0	0
		0	0	0	1	1	0	3	0	1	1	1	1	0	1	1
		0	0	1	0	0	0	4	0	1	1	1	1	0	1	0
		0	0	1	0	1	0	5	0	1	1	1	1	0	0	1
		0	0	1	1	0	0	6	0	1	1	1	1	0	0	0
		0	0	1	1	1	0	7	0	1	1	1	0	1	1	1
		0	1	0	0	0	0	8	0	1	1	1	0	1	1	0
		0	1	0	0	1	0	9	0	1	1	1	0	1	0	1
		0	1	0	1	0	0	10	0	1	1	1	0	1	0	0
		0	1	0	1	1	0	11	0	1	1	1	0	0	1	1
		0	1	1	0	0	0	12	0	1	1	1	0	0	1	0
		0	1	1	0	1	0	13	0	1	1	1	0	0	0	1
		0	1	1	1	0	0	14	0	1	1	1	0	0	0	0
		0	1	1	1	1	0	15	0	1	1	0	1	1	1	1
		1	0	0	0	0	0	16	0	1	1	0	1	1	1	0
		1	0	0	0	1	0	17	0	1	1	0	1	1	0	1
		1	0	0	1	0	0	18	0	1	1	0	1	1	0	0
		1	0	0	1	1	0	19	0	1	1	0	1	0	1	1
		1	0	1	0	0	0	20	0	1	1	0	1	0	1	0
		1	0	1	0	1	0	21	0	1	1	0	1	0	0	1
		1	0	1	1	0	0	22	0	1	1	0	1	0	0	0
		1	0	1	1	1	0	23	0	1	1	0	0	1	1	1
		1	1	0	0	0	0	24	0	0	1	0	0	1	1	0
		1	1	0	0	1	0	25	0	0	1	0	0	1	1	0
		1	1	0	1	0	0	26	0	0	1	0	0	1	1	0
		1	1	0	1	1	0	27	0	0	1	0	0	1	1	0
		1	1	1	0	0	0	28	0	0	1	0	0	1	1	0
		1	1	1	0	1	0	29	1	1	1	1	1	1	1	0
		1	1	1	1	0	0	30	0	0	1	0	0	0	1	0
		1	1	1	1	1	0	31	0	0	1	0	0	0	0	1
		X	X	X	X	X	1	ALL								

GT400 50 Hz Video Line Counter
GT400 Location A7

SPEC. #02999-032 REVISION: 000

TITLE: GT200/GT400 9 x 9 U.C. CHAR. GEN.

ADD.	--DATA-- 87654321	ADD.	--DATA-- 87654321	ADD.	--DATA-- 87654321	ADD.	--DATA-- 87654321
001	11111111	129	11111111	257	11111111	385	11111111
002	11[illegible]111	130	1[illegible]111	258	11111111	386	11[illegible]111
003	1[illegible]111	131	1[illegible]111	259	11111111	387	1[illegible]111
004	1[illegible]111	132	1[illegible]111	260	11111111	388	1[illegible]111
005	1[illegible]111	133	1[illegible]111	261	11111111	389	1[illegible]111
006	1[illegible]111	134	11111111	262	11111111	390	1[illegible]111
007	11111111	135	11111111	263	11111111	391	1[illegible]111
008	1[illegible]111	136	11111111	264	11111111	392	11[illegible]111
009	11111111	137	11111111	265	11111111	393	11111111
010	1[illegible]111	138	1[illegible]111	266	1[illegible]1111	394	1[illegible]1111
011	1[illegible]1010	139	1[illegible]111	267	1[illegible]0110	395	1[illegible]1111
012	1[illegible]111	140	1[illegible]111	268	1[illegible]0110	396	1[illegible]1111
013	1[illegible]111	141	1[illegible]111	269	1[illegible]1111	397	1[illegible]1111
014	1[illegible]111	142	1[illegible]111	270	1[illegible]1111	398	1[illegible]1111
015	1[illegible]111	143	1[illegible]1010	271	11111111	399	1[illegible]1111
016	1[illegible]111	144	1[illegible]111	272	1[illegible]1111	400	1[illegible]1111
017	11111111	145	11111111	273	11111111	401	11111111
018	1[illegible]1010	146	1[illegible]111	274	1[illegible]111	402	1[illegible]111
019	1[illegible]111	147	1[illegible]111	275	1[illegible]111	403	1[illegible]111
020	1[illegible]111	148	1[illegible]111	276	1[illegible]1010	404	1[illegible]111
021	1[illegible]111	149	1[illegible]111	277	11111111	405	1[illegible]111
022	1[illegible]111	150	1[illegible]1111	278	11111111	406	1[illegible]1110
023	1[illegible]111	151	1[illegible]1111	279	11111111	407	1[illegible]1110
024	1[illegible]1010	152	1[illegible]111	280	11111111	408	1[illegible]111
025	11111111	153	11111111	281	11111111	409	11111111
026	1[illegible]111	154	1[illegible]111	282	11111111	410	1[illegible]111
027	1[illegible]111	155	1[illegible]111	283	1[illegible]1111	411	1[illegible]111
028	11111111	156	1[illegible]1110	284	1[illegible]111	412	1[illegible]111
029	11111111	157	1[illegible]0110	285	1[illegible]1111	413	1[illegible]111
030	11111111	158	11111010	286	1[illegible]1111	414	1[illegible]111
031	1[illegible]111	159	1[illegible]111	287	1[illegible]111	415	1[illegible]111
032	1[illegible]111	160	1[illegible]111	288	1[illegible]1111	416	1[illegible]111
033	11111111	161	11111111	289	11111111	417	11111111
034	1[illegible]1010	162	1[illegible]111	290	1[illegible]1111	418	1[illegible]111
035	1[illegible]111	163	1[illegible]1111	291	1[illegible]1010	419	1[illegible]111
036	1[illegible]111	164	1[illegible]1111	292	1[illegible]1111	420	1[illegible]1111
037	1[illegible]111	165	1[illegible]1111	293	1[illegible]1010	421	1[illegible]1111
038	1[illegible]111	166	1[illegible]1111	294	1[illegible]111	422	1[illegible]111
039	1[illegible]111	167	1[illegible]1111	295	1[illegible]1010	423	1[illegible]1111
040	1[illegible]1010	168	1[illegible]1111	296	1[illegible]1111	424	1[illegible]1111
041	11111111	169	11111111	297	11111111	425	11111111
042	1[illegible]111	170	1[illegible]111	298	1[illegible]111	426	1[illegible]111
043	1[illegible]1111	171	1[illegible]111	299	1[illegible]111	427	1[illegible]1111
044	1[illegible]1111	172	1[illegible]1111	300	1[illegible]1111	428	1[illegible]1111
045	1[illegible]1111	173	1[illegible]1111	301	1[illegible]1111	429	1[illegible]1111
046	1[illegible]1111	174	1[illegible]1111	302	1[illegible]1111	430	1[illegible]1111
047	1[illegible]1111	175	1[illegible]1111	303	1[illegible]1111	431	1[illegible]1111
048	1[illegible]111	176	1[illegible]1010	304	1[illegible]1111	432	1[illegible]1010

SPEC. #02999-032 REVISION: 000

TITLE: GT200/GT400 9 x 9 U.C. CHAR. GEN.

ADD.	--DATA-- 87654321	ADD.	--DATA-- 87654321	ADD.	--DATA-- 87654321	ADD.	--DATA-- 87654321
049	11111111	177	11111111	305	11111111	433	11111111
050	10000011	178	10111011	306	11001110	434	11000010
051	10111111	179	10111011	307	11011110	435	11011110
052	10111111	180	10111011	308	11011111	436	10111111
053	10001111	181	11011010	309	11111111	437	10000111
054	10111111	182	11000111	310	10111011	438	10111011
055	10111111	183	11110110	311	11011110	439	10111011
056	10111111	184	11101111	312	11001010	440	11000111
057	11111111	185	11111111	313	11111111	441	11111111
058	11000111	186	10111011	314	11101111	442	10000011
059	10111011	187	10111011	315	11101110	443	11111010
060	10111111	188	10111011	316	11011111	444	11110111
061	10111111	189	10111011	317	11111111	445	11101111
062	10111011	190	10111011	318	11111111	446	11011111
063	10111011	191	10111011	319	11111111	447	11011110
064	11000011	192	11011111	320	11111111	448	10111111
065	11111111	193	11111111	321	11111111	449	11111111
066	10111011	194	10111011	322	11110110	450	11000111
067	10111011	195	11011010	323	11101111	451	11011010
068	10111011	196	11000111	324	11101110	452	11011010
069	10000011	197	11101111	325	11101110	453	11000111
070	10111011	198	11000111	326	11101110	454	10111011
071	10111011	199	11011010	327	11101111	455	10111011
072	10111011	200	10111011	328	11110110	456	11000111
073	11111111	201	11111111	329	11111111	457	11111111
074	11000111	202	10111011	330	11101110	458	11000111
075	11101111	203	11011010	331	11101111	459	10111011
076	11101111	204	11000111	332	11110110	460	10111011
077	11101111	205	11101111	333	11110110	461	11000011
078	11101111	206	11101111	334	11110110	462	11111011
079	11101111	207	11101111	335	11101111	463	11111010
080	11000111	208	11101111	336	11101110	464	11000110
081	11111111	209	11111111	337	11111111	465	11111111
082	11111011	210	10000011	338	11111111	466	11111111
083	11111011	211	11111011	339	11011010	467	11101111
084	11111011	212	11110111	340	11110110	468	11101111
085	11111011	213	11101111	341	10000011	469	11111111
086	10111011	214	11011111	342	11110110	470	11101111
087	10111011	215	10111111	343	11011010	471	11101111
088	11000010	216	10000011	344	11111111	472	11111111
089	11111111	217	11111111	345	11111111	473	11111111
090	10111011	218	11000111	346	11111111	474	11111111
091	10111111	219	11011111	347	11101111	475	11101111
092	10111111	220	11011111	348	11101111	476	11101111
093	10111111	221	11011111	349	10000011	477	11111111
094	10111111	222	11011111	350	11101111	478	11101111
095	10111111	223	11011111	351	11101111	479	11101110
096	10111111	224	11000111	352	11111111	480	11011111

SPEC. #02999-032 REVISION: 000

TITLE: GT200/GT400 9 x 9 U.C. CHAR. GEN.

ADD.	--DATA-- 87654321	ADD.	--DATA-- 87654321	ADD.	--DATA-- 87654321	ADD.	--DATA-- 87654321
097	11111111	225	11111111	353	11111111	481	11111111
098	11111111	226	11011110	354	11111111	482	11111111
099	11111111	227	11111111	355	11111111	483	11110111
100	11111111	228	11101110	356	11111111	484	11101111
101	11111111	229	11101111	357	11111111	485	11011111
102	11111111	230	11110110	358	11001111	486	11101111
103	11111111	231	11110111	359	11101110	487	11110111
104	11000011	232	11111010	360	11011111	488	11111111
105	11111111	233	11111111	361	11111111	489	11111111
106	11111011	234	11000111	362	11111111	490	11111111
107	11101011	235	11110111	363	11111111	491	11111111
108	11101011	236	11110111	364	11111111	492	10000011
109	11101011	237	11110111	365	10000011	493	11111111
110	11111011	238	11110111	366	11111111	494	10000011
111	11111011	239	11110111	367	11111111	495	11111111
112	11111011	240	11000111	368	11111111	496	11111111
113	11111111	241	11111111	369	11111111	497	11111111
114	11111011	242	11101111	370	11111111	498	11111111
115	11111011	243	11110111	371	11111111	499	11011111
116	11101011	244	11101011	372	11111111	500	11101111
117	11101011	245	11101111	373	11111111	501	11110111
118	11111011	246	11101111	374	11111111	502	11101111
119	11111011	247	11101111	375	11001111	503	11011111
120	11111011	248	11101111	376	11001111	504	11111111
121	11111111	249	11111111	377	11111111	505	11111111
122	11000010	250	11111111	378	11111010	506	11000111
123	11111011	251	11101111	379	11110111	507	11111011
124	11111011	252	11011111	380	11110110	508	11110111
125	11111011	253	11000011	381	11101111	509	11101111
126	11111011	254	11011111	382	11101110	510	11101111
127	11111011	255	11101111	383	11011111	511	11111111
128	11000010	256	11111111	384	11011110	512	11101111

SPEC #02939-003 REVISION: 000

TITLE: **GT200/GT400 9 x 9 LOWER CASE CHAR. GEN.**

ADD.	--DATA-- 87654321	ADD.	--DATA-- 87654321	ADD.	--DATA-- 87654321	ADD.	--DATA-- 87654321
001	11111111	129	11111111	257	11111111	385	11111111
002	11111111	130	11111111	258	11111111	386	11111111
003	11111111	131	11111111	259	11111111	387	11111111
004	11111111	132	11111111	260	11111111	388	11111111
005	11111111	133	11111111	261	11111111	389	11111111
006	11111111	134	11111111	262	11111111	390	11111111
007	11111111	135	11111111	263	11111111	391	11111111
008	11111111	136	11111111	264	11111111	392	11111111
009	11111111	137	11111111	265	11111111	393	11111111
010	11111111	138	11111111	266	11111111	394	11111111
011	11111111	139	11111111	267	11111111	395	11111111
012	11111111	140	11111111	268	11111111	396	11111111
013	11111111	141	11111111	269	11111111	397	11111111
014	11111111	142	11111111	270	11111111	398	11111111
015	11111111	143	11111111	271	11111111	399	11111111
016	11111111	144	11111111	272	11111111	400	11111111
017	11111111	145	11111111	273	11111111	401	11111111
018	11111111	146	11111111	274	11111111	402	11111111
019	11111111	147	11111111	275	11111111	403	11111111
020	11111111	148	11111111	276	11111111	404	11111111
021	11111111	149	11111111	277	11111111	405	11111111
022	11111111	150	11111111	278	11111111	406	11111111
023	11111111	151	11111111	279	11111111	407	11111111
024	11111111	152	11111111	280	11111111	408	11111111
025	11111111	153	11111111	281	11111111	409	11111111
026	11111111	154	11111111	282	11111111	410	11111111
027	11111111	155	11111111	283	11111111	411	11111111
028	11111111	156	11111111	284	11111111	412	11111111
029	11111111	157	11111111	285	11111111	413	11111111
030	11111111	158	11111111	286	11111111	414	11111111
031	11111111	159	11111111	287	11111111	415	11111111
032	11111111	160	11111111	288	11111111	416	11111111
033	11111111	161	11111111	289	11111111	417	11111111
034	11111111	162	11111111	290	11111111	418	11111111
035	11111111	163	11111111	291	11111111	419	11111111
036	11111111	164	11111111	292	11111111	420	11111111
037	11111111	165	11111111	293	11111111	421	11111111
038	11111111	166	11111111	294	11111111	422	11111111
039	11111111	167	11111111	295	11111111	423	11111111
040	11111111	168	11111111	296	11111111	424	11111111
041	11111111	169	11111111	297	11111111	425	11111111
042	11111111	170	11111111	298	11111111	426	11111111
043	11111111	171	11111111	299	11111111	427	11111111
044	11111111	172	11111111	300	11111111	428	11111111
045	11111111	173	11111111	301	11111111	429	11111111
046	11111111	174	11111111	302	11111111	430	11111111
047	11111111	175	11111111	303	11111111	431	11111111
048	11111111	176	11111111	304	11111111	432	11111111

SPEC. #02999-033 REVISION: 000

TITLE: **GT200/GT400 9 x 9 LOWER CASE CHAR. GEN.**

ADD.	--DATA-- 87654321	ADD.	--DATA-- 87654321	ADD.	--DATA-- 87654321	ADD.	--DATA-- 87654321
049	11111111	177	11111111	305	11111111	433	11111111
050	11111111	178	11111111	306	11111111	434	11111011
051	11111111	179	11111111	307	11111111	435	11110110
052	11111111	180	11111111	308	11000010	436	11101111
053	11011010	181	11101111	309	11111111	437	11101110
054	11111111	182	11101111	310	11000010	438	11101111
055	11011010	183	11101111	311	11111011	439	11110110
056	11111111	184	11111011	312	11000010	440	11110011
057	11111111	185	11111111	313	11111111	441	11111111
058	11111111	186	11111111	314	11111111	442	11111111
059	11111111	187	11111111	315	11111111	443	11111111
060	11111111	188	11111111	316	11111111	444	11111111
061	11111111	189	11111111	317	11111111	445	11111111
062	11111111	190	11111111	318	11111111	446	11111111
063	11111111	191	11111111	319	11111111	447	11111111
064	11111111	192	11111111	320	11111111	448	11111111
065	11111111	193	11111111	321	11111111	449	11111111
066	11111011	194	11101111	322	11101111	450	11101111
067	11111011	195	11101111	323	11101111	451	11101111
068	11111011	196	11101111	324	11100011	452	11101111
069	11110011	197	11101111	325	11101111	453	11111111
070	11011011	198	11101111	326	11101111	454	11101111
071	11011011	199	11101111	327	11101111	455	11101111
072	11011011	200	11100111	328	11110010	456	11101111
073	11111111	201	11111111	329	11111111	457	11111111
074	11111111	202	11111111	330	11111111	458	11111111
075	11111111	203	11111111	331	11111111	459	11111111
076	11111111	204	11111111	332	11111111	460	11111111
077	11111111	205	11111111	333	11111111	461	11111111
078	11111111	206	11111111	334	11111111	462	11111111
079	11111111	207	11111111	335	11111111	463	11111111
080	11111111	208	11111111	336	11111111	464	11111111
081	11111111	209	11111111	337	11111111	465	11111111
082	11111111	210	11111111	338	11111111	466	10011111
083	11111111	211	11111111	339	11111111	467	11101110
084	11011011	212	11011011	340	10111011	468	11101111
085	11011010	213	10111011	341	10111011	469	11110010
086	11011011	214	10111011	342	10111011	470	11101111
087	11011110	215	10111011	343	10110011	471	11101110
088	11100010	216	10111011	344	11101011	472	10011111
089	11111111	217	11111111	345	11111111	473	11111111
090	11111111	218	11111111	346	11111111	474	11111111
091	11111111	219	11111111	347	11111111	475	11111111
092	11111111	220	11111111	348	11111111	476	11111111
093	11111111	221	11111111	349	11111111	477	11111111
094	11111111	222	11111111	350	11111111	478	11111111
095	11111111	223	11111111	351	11111111	479	11111111
096	11111111	224	11111111	352	11111111	480	11111111

SPEC. #02999-033 REVISION: 000

TITLE: GT200/GT400 9 x 9 LOWER CASE CHAR. GEN.

ADD.	--DATA-- 87654321	ADD.	--DATA-- 87654321	ADD.	--DATA-- 87654321	ADD.	--DATA-- 87654321
097	11111111	225	11111111	353	11111111	481	11111111
098	11[illegible]010	226	11111111	354	11111111	482	11[illegible]1110
099	11[illegible]1111	227	11111111	355	11111111	483	10[illegible]011
100	1[illegible]111	228	1[illegible]111	356	10111011	484	11110010
101	11[illegible]1111	229	10[illegible]011	357	11011010	485	11111111
102	11[illegible]1111	230	10[illegible]011	358	11[illegible]111	486	11111111
103	11[illegible]1111	231	10[illegible]011	359	11[illegible]0110	487	11111111
104	11[illegible]1111	232	10[illegible]011	360	11[illegible]1111	488	11111111
105	11111111	233	11111111	361	11111111	489	11111111
106	11111111	234	11111111	362	11111111	490	11111111
107	11111111	235	11111111	363	11111111	491	11111111
108	11111111	236	11111111	364	11111111	492	11111111
109	11111111	237	11111111	365	11111111	493	11111111
110	11111111	238	11111111	366	11111111	494	11111111
111	11111111	239	11111111	367	11111111	495	11111111
112	11111111	240	11111111	368	11111111	496	11111111
113	11111111	241	11111111	369	11111111	497	11111111
114	11111111	242	11111111	370	11111111	498	1[illegible]11
115	11111111	243	11111111	371	11111111	499	1[illegible]11
116	11[illegible]011	244	11[illegible]111	372	10111011	500	1[illegible]11
117	10[illegible]011	245	11011010	373	10111011	501	1[illegible]11
118	10[illegible]011	246	10111011	374	10[illegible]011	502	1[illegible]11
119	10[illegible]011	247	11011010	375	10[illegible]011	503	1[illegible]11
120	11[illegible]011	248	11[illegible]111	376	11[illegible]1111	504	1[illegible]11
121	11111011	249	11111111	377	11111111	505	11111111
122	11[illegible]111	250	11111111	378	11111111	506	11111111
123	11111111	251	11111111	379	11111111	507	11111111
124	11111111	252	11111111	380	11111111	508	11111111
125	11111111	253	11111111	381	11111111	509	11111111
126	11111111	254	11111111	382	11111111	510	11111111
127	11111111	255	11111111	383	11111111	511	11111111
128	11111111	256	11111111	384	11111111	512	11111111

Z80™-CPU
Z80A™-CPU

Zilog

Product Specification

The Zilog Z80 product line is a complete set of microcomputer components, development systems and support software. The Z80 microcomputer component set includes all of the circuits necessary to build high-performance microcomputer systems with virtually no other logic and a minimum number of low cost standard memory elements.

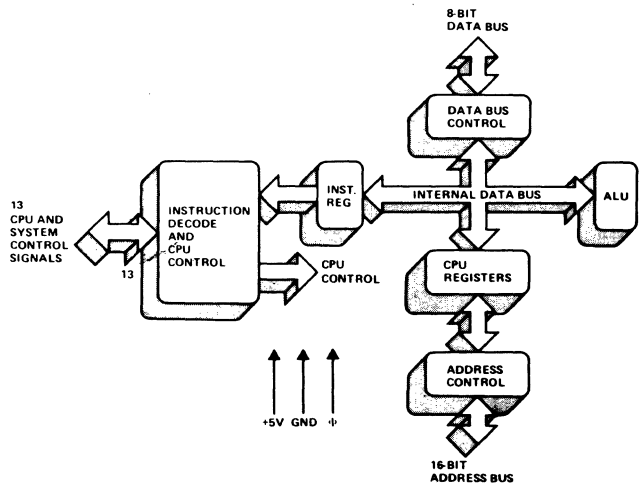
The Z80 and Z80A CPU's are third generation single chip microprocessors with unrivaled computational power. This increased computational power results in higher system through-put and more efficient memory utilization when compared to second generation microprocessors. In addition, the Z80 and Z80A CPU's are very easy to implement into a system because of their single voltage requirement plus all output signals are fully decoded and timed to control standard memory or peripheral circuits. The circuit is implemented using an N-channel, ion implanted, silicon gate MOS process.

Figure 1 is a block diagram of the CPU, Figure 2 details the internal register configuration which contains 208 bits of Read/Write memory that are accessible to the programmer. The registers include two sets of six general purpose registers that may be used individually as 8-bit registers or as 16-bit register pairs. There are also two sets of accumulator and flag registers. The programmer has access to either set of main or alternate registers through a group of exchange instructions. This alternate set allows foreground/background mode of operation or may be reserved for very fast Interrupt response. Each CPU also contains a 16-bit stack pointer which permits simple implementation of multiple level interrupts, unlimited subroutine nesting and simplification of many types of data handling.

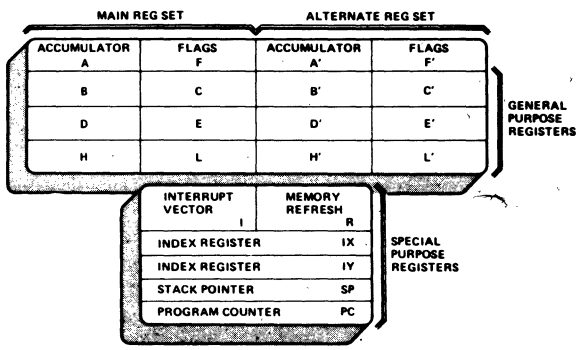
The two 16-bit index registers allow tabular data manipulation and easy implementation of relocatable code. The Refresh register provides for automatic, totally transparent refresh of external dynamic memories. The I register is used in a powerful interrupt response mode to form the upper 8 bits of a pointer to a interrupt service address table, while the interrupting device supplies the lower 8 bits of the pointer. An indirect call is then made to this service address.

FEATURES

- Single chip, N-channel Silicon Gate CPU.
- 158 instructions–includes all 78 of the 8080A instructions with total software compatibility. New instructions include 4-, 8- and 16-bit operations with more useful addressing modes such as indexed, bit and relative.
- 17 internal registers.
- Three modes of fast interrupt response plus a non-maskable interrupt.
- Directly interfaces standard speed static or dynamic memories with virtually no external logic.
- 1.0 μs instruction execution speed.
- Single 5 VDC supply and single-phase 5 volt Clock.
- Out-performs any other single chip microcomputer in 4-, 8-, or 16-bit applications.
- All pins TTL Compatible
- Built-in dynamic RAM refresh circuitry.



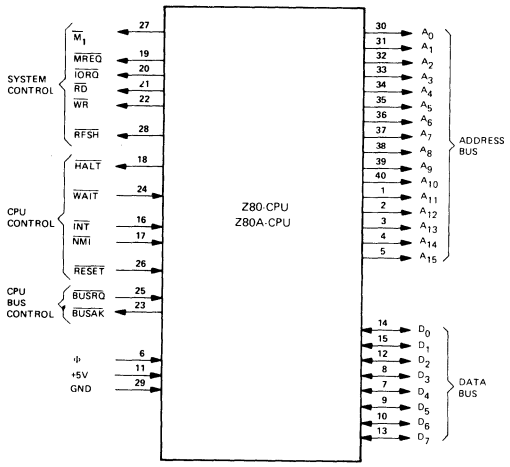
Z80, Z80A CPU BLOCK DIAGRAM



Z80, Z80A CPU REGISTERS

TM: Z80 is a trademark of Zilog, Inc.

Z80, Z80A-CPU Pin Description



Z80, Z80A CPU PIN CONFIGURATION

A_0-A_{15} (Address Bus)
Tri-state output, active high. A_0-A_{15} constitute a 16-bit address bus. The address bus provides the address for memory (up to 64K bytes) data exchanges and for I/O device data exchanges.

D_0-D_7 (Data Bus)
Tri-state input/output, active high. D_0-D_7 constitute an 8-bit bidirectional data bus. The data bus is used for data exchanges with memory and I/O devices.

$\overline{M_1}$ (Machine Cycle one)
Output, active low. $\overline{M_1}$ indicates that the current machine cycle is the OP code fetch cycle of an instruction execution.

$\overline{MREQ}$ (Memory Request)
Tri-state output, active low. The memory request signal indicates that the address bus holds a valid address for a memory read or memory write operation.

$\overline{IORQ}$ (Input/ Output Request)
Tri-state output, active low. The $\overline{IORQ}$ signal indicates that the lower half of the address bus holds a valid I/O address for a I/O read or write operation. An $\overline{IORQ}$ signal is also generated when an interrupt is being acknowledged to indicate that an interrupt response vector can be placed on the data bus.

$\overline{RD}$ (Memory Read)
Tri-state output, active low. $\overline{RD}$ indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O device or memory should use this signal to gate data onto the CPU data bus.

$\overline{WR}$ (Memory Write)
Tri-state output, active low. $\overline{WR}$ indicates that the CPU data bus holds valid data to be stored in the addressed memory or I/O device.

$\overline{RFSH}$ (Refresh)
Output, active low. $\overline{RFSH}$ indicates that the lower 7 bits of the address bus contain a refresh address for dynamic memories and the current $\overline{MREQ}$ signal should be used to do a refresh read to all dynamic memories.

$\overline{HALT}$ (Halt state)
Output, active low. $\overline{HALT}$ indicates that the CPU has executed a HALT software instruction and is awaiting either a non-maskable or a maskable interrupt (with the mask enabled) before operation can resume. While halted, the CPU executes NOP's to maintain memory refresh activity.

$\overline{WAIT}$ (Wait)
Input, active low. $\overline{WAIT}$ indicates to the Z-80 CPU that the addressed memory or I/O devices are not ready for a data transfer. The CPU continues to enter wait states for as long as this signal is active.

$\overline{INT}$ (Interrupt Request)
Input, active low. The Interrupt Request signal is generated by I/O devices. A request will be honored at the end of the current instruction if the internal software controlled interrupt enable flip-flop (IFF) is enabled.

$\overline{NMI}$ (Non Maskable Interrupt)
Input, active low. The non-maskable interrupt request line has a higher priority than $\overline{INT}$ and is always recognized at the end of the current instruction, independent of the status of the interrupt enable flip-flop. $\overline{NMI}$ automatically forces the Z-80 CPU to restart to location 0066_H.

$\overline{RESET}$
Input, active low. $\overline{RESET}$ initializes the CPU as follows: reset interrupt enable flip-flop, clear PC and registers I and R and set interrupt to 8080A mode. During reset time, the address and data bus go to a high impedance state and all control output signals go to the inactive state.

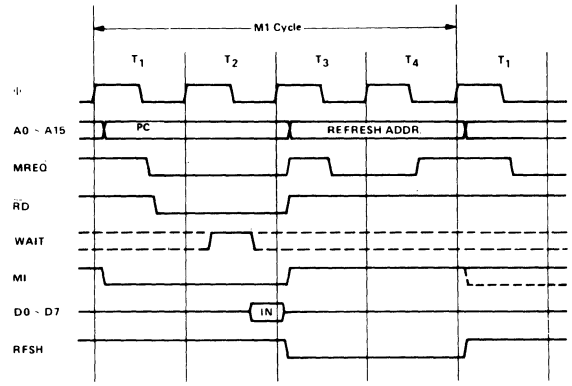
$\overline{BUSRQ}$ (Bus Request)
Input, active low. The bus request signal has a higher priority than $\overline{NMI}$ and is always recognized at the end of the current machine cycle and is used to request the CPU address bus, data bus and tri-state output control signals to go to a high impedance state so that other devices can control these busses.

$\overline{BUSAK}$ (Bus Acknowledge)
Output, active low. Bus acknowledge is used to indicate to the requesting device that the CPU address bus, data bus and tri-state control bus signals have been set to their high impedance state and the external device can now control these signals.

Timing Waveforms

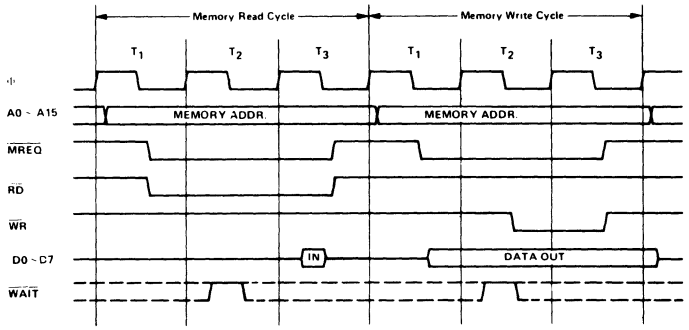
INSTRUCTION OP CODE FETCH

The program counter content (PC) is placed on the address bus immediately at the start of the cycle. One half clock time later $\overline{MREQ}$ goes active. The falling edge of $\overline{MREQ}$ can be used directly as a chip enable to dynamic memories. $\overline{RD}$ when active indicates that the memory data should be enabled onto the CPU data bus. The CPU samples data with the rising edge of the clock state T_3. Clock states T_3 and T_4 of a fetch cycle are used to refresh dynamic memories while the CPU is internally decoding and executing the instruction. The refresh control signal $\overline{RFSH}$ indicates that a refresh read of all dynamic memories should be accomplished.



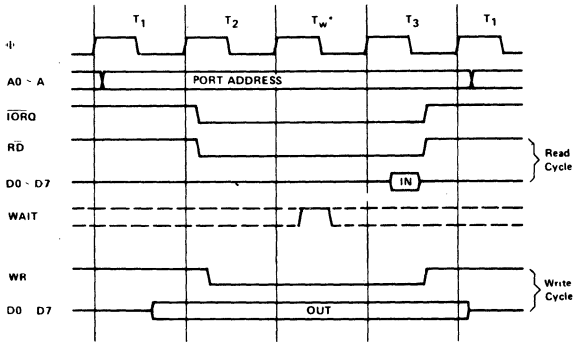
MEMORY READ OR WRITE CYCLES

Illustrated here is the timing of memory read or write cycles other than an OP code fetch (M_1 cycle). The $\overline{MREQ}$ and $\overline{RD}$ signals are used exactly as in the fetch cycle. In the case of a memory write cycle, the $\overline{MREQ}$ also becomes active when the address bus is stable so that it can be used directly as a chip enable for dynamic memories. The $\overline{WR}$ line is active when data on the data bus is stable so that it can be used directly as a R/W pulse to virtually any type of semiconductor memory.



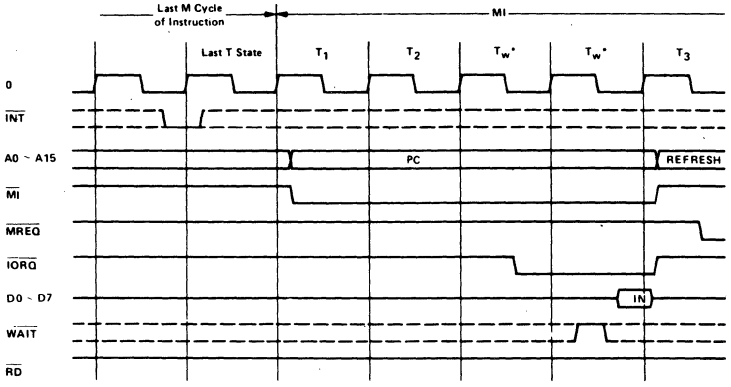
INPUT OR OUTPUT CYCLES

Illustrated here is the timing for an I/O read or I/O write operation. Notice that during I/O operations a single wait state is automatically inserted (Tw*). The reason for this is that during I/O operations this extra state allows sufficient time for an I/O port to decode its address and activate the $\overline{WAIT}$ line if a wait is required.



INTERRUPT REQUEST/ACKNOWLEDGE CYCLE

The interrupt signal is sampled by the CPU with the rising edge of the last clock at the end of any instruction. When an interrupt is accepted, a special M_1 cycle is generated. During this M_1 cycle, the $\overline{IORQ}$ signal becomes active (instead of $\overline{MREQ}$) to indicate that the interrupting device can place an 8-bit vector on the data bus. Two wait states (Tw*) are automatically added to this cycle so that a ripple priority interrupt scheme, such as the one used in the Z80 peripheral controllers, can be easily implemented.



Z80, Z80A Instruction Set

The following is a summary of the Z80, Z80A instruction set showing the assembly language mnemonic and the symbolic operation performed by the instruction. A more detailed listing appears in the Z80-CPU technical manual, and assembly language programming manual. The instructions are divided into the following categories:

- 8-bit loads
- 16-bit loads
- Exchanges
- Memory Block Moves
- Memory Block Searches
- 8-bit arithmetic and logic
- 16-bit arithmetic
- General purpose Accumulator & Flag Operations
- Miscellaneous Group
- Rotates and Shifts
- Bit Set, Reset and Test
- Input and Output
- Jumps
- Calls
- Restarts
- Returns

In the table the following terminology is used.

- b ≡ a bit number in any 8-bit register or memory location
- cc ≡ flag condition code
  - NZ ≡ non zero
  - Z ≡ zero
  - NC ≡ non carry
  - C ≡ carry
  - PO ≡ Parity odd or no over flow
  - PE ≡ Parity even or over flow
  - P ≡ Positive
  - M ≡ Negative (minus)
- d ≡ any 8-bit destination register or memory location
- dd ≡ any 16-bit destination register or memory location
- e ≡ 8-bit signed 2's complement displacement used in relative jumps and indexed addressing
- L ≡ 8 special call locations in page zero. In decimal notation these are 0, 8, 16, 24, 32, 40, 48 and 56
- n ≡ any 8-bit binary number
- nn ≡ any 16-bit binary number
- r ≡ any 8-bit general purpose register (A, B, C, D, E, H, or L)
- s ≡ any 8-bit source register or memory location
- s_b ≡ a bit in a specific 8-bit register or memory location
- ss ≡ any 16-bit source register or memory location
- subscript "L" ≡ the low order 8 bits of a 16-bit register
- subscript "H" ≡ the high order 8 bits of a 16-bit register
- ( ) ≡ the contents within the ( ) are to be used as a pointer to a memory location or I/O port number

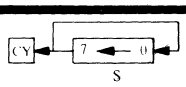
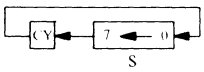
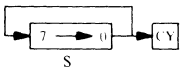
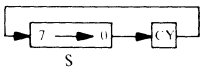
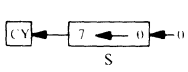
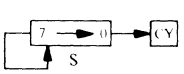
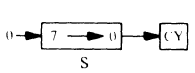
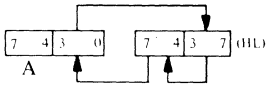
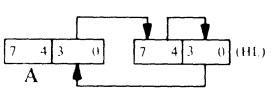
8-bit registers are A, B, C, D, E, H, L, I and R
16-bit register pairs are AF, BC, DE and HL
16-bit registers are SP, PC, IX and IY

Addressing Modes implemented include combinations of the following:

- Immediate
- Immediate extended
- Modified Page Zero
- Relative
- Extended
- Indexed
- Register
- Implied
- Register Indirect
- Bit

	Mnemonic	Symbolic Operation	Comments
8-BIT LOADS	LD r, s	r ← s	s ≡ r, n, (HL), (IX+e), (IY+e)
	LD d, r	d ← r	d ≡ (HL), r (IX+e), (IY+e)
	LD d, n	d ← n	d ≡ (HL), (IX+e), (IY+e)
	LD A, s	A ← s	s ≡ (BC), (DE), (nn), I, R
	LD d, A	d ← A	d ≡ (BC), (DE), (nn), I, R
16-BIT LOADS	LD dd, nn	dd ← nn	dd ≡ BC, DE, HL, SP, IX, IY
	LD dd, (nn)	dd ← (nn)	dd ≡ BC, DE, HL, SP, IX, IY
	LD (nn), ss	(nn) ← ss	ss ≡ BC, DE, HL, SP, IX, IY
	LD SP, ss	SP ← ss	ss = HL, IX, IY
	PUSH ss	$(SP-1) \leftarrow ss_H$; $(SP-2) \leftarrow ss_L$	ss = BC, DE, HL, AF, IX, IY
	POP dd	$dd_L \leftarrow (SP)$; $dd_H \leftarrow (SP+1)$	dd = BC, DE, HL, AF, IX, IY
EXCHANGES	EX DE, HL	DE ↔ HL	
	EX AF, AF'	AF ↔ AF'	
	EXX	$\begin{pmatrix} BC \\ DE \\ HL \end{pmatrix} \leftrightarrow \begin{pmatrix} BC' \\ DE' \\ HL' \end{pmatrix}$	
	EX (SP), ss	$(SP) \cdot\cdot ss_L$, $(SP+1) \cdot\cdot ss_H$	ss ≡ HL, IX, IY

	Mnemonic	Symbolic Operation	Comments
MEMORY BLOCK MOVES	LDI	(DE) ← (HL), DE ← DE+1 HL ← HL+1, BC ← BC-1	
	LDIR	(DE) ← (HL), DE ← DE+1 HL ← HL+1, BC ← BC-1 Repeat until BC = 0	
	LDD	(DE) ← (HL), DE ← DE-1 HL ← HL-1, BC ← BC-1	
	LDDR	(DE) ← (HL), DE ← DE-1 HL ← HL-1, BC ← BC-1 Repeat until BC = 0	
MEMORY BLOCK SEARCHES	CPI	A-(HL), HL ← HL+1 BC ← BC-1	
	CPIR	A-(HL), HL ← HL+1 BC ← BC-1, Repeat until BC = 0 or A = (HL)	A-(HL) sets the flags only. A is not affected
	CPD	A-(HL), HL ← HL-1 BC ← BC-1	
	CPDR	A-(HL), HL ← HL-1 BC ← BC-1, Repeat until BC = 0 or A = (HL)	
8-BIT ALU	ADD s	A ← A + s	
	ADC s	A ← A + s + CY	CY is the carry flag
	SUB s	A ← A - s	
	SBC s	A ← A - s - CY	s ≡ r, n, (HL) (IX+e), (IY+e)
	AND s	A ← A ∧ s	
	OR s	A ← A ∨ s	
	XOR s	A ← A ⊕ s	

	Mnemonic	Symbolic Operation	Comments
8 ALU	CP s	A - s	s = r, n (HL) (IX+e), (IY+e)
	INC d	d ← d + 1	d = r, (HL) (IX+e), (IY+e)
	DEC d	d ← d - 1	
16-BIT ARITHMETIC	ADD HL, ss	HL ← HL + ss	ss ≡ BC, DE HL, SP
	ADC HL, ss	HL ← HL + ss + CY	
	SBC HL, ss	HL ← HL - ss - CY	
	ADD IX, ss	IX ← IX + ss	ss ≡ BC, DE IX, SP
	ADD IY, ss	IY ← IY + ss	ss ≡ BC, DE, IY, SP
	INC dd	dd ← dd + 1	dd ≡ BC, DE, HL, SP, IX, IY
	DEC dd	dd ← dd - 1	dd ≡ BC, DE, HL, SP, IX, IY
GP ACC. & FLAG	DAA	Converts A contents into packed BCD following add or subtract.	Operands must be in packed BCD format
	CPL	$A \leftarrow \overline{A}$	
	NEG	A ← 00 – A	
	CCF	$CY \leftarrow \overline{CY}$	
	SCF	CY ← 1	
MISCELLANEOU	NOP	No operation	
	HALT	Halt CPU	
	DI	Disable Interrupts	
	EI	Enable Interrupts	
	IM 0	Set interrupt mode 0	8080A mode
	IM 1	Set interrupt mode 1	Call to 0038_H
	IM 2	Set interrupt mode 2	Indirect Call
ROTATES AND SHIFTS	RLC s		s ≡ r, (HL) (IX+e), (IY+e)
	RL s		
	RRC s		
	RR s		
	SLA s		
	SRA s		
	SRL s		
	RLD		
	RRD		

	Mnemonic	Symbolic Operation	Comments
BIT S, R, & T	BIT b, s	$Z \leftarrow \overline{s_b}$	Z is zero flag
	SET b, s	$s_b \leftarrow 1$	s ≡ r, (HL) (IX+e), (IY+e)
	RES b, s	$s_b \leftarrow 0$	
INPUT AND OUTPUT	IN A, (n)	A ← (n)	
	IN r, (C)	r ← (C)	Set flags
	INI	(HL) ← (C), HL ← HL + 1 B ← B - 1	
	INIR	(HL) ← (C), HL ← HL + 1 B ← B - 1 Repeat until B = 0	
	IND	(HL) ← (C), HL ← HL - 1 B ← B - 1	
	INDR	(HL) ← (C), HL ← HL - 1 B ← B - 1 Repeat until B = 0	
	OUT(n), A	(n) ← A	
	OUT(C), r	(C) ← r	
	OUTI	(C) ← (HL), HL ← HL + 1 B ← B - 1	
	OTIR	(C) ← (HL), HL ← HL + 1 B ← B - 1 Repeat until B = 0	
	OUTD	(C) ← (HL), HL ← HL - 1 B ← B - 1	
	OTDR	(C) ← (HL), HL ← HL - 1 B ← B - 1 Repeat until B = 0	
JUMPS	JP nn	PC ← nn	cc ≡ NZ PO, Z PE, NC P, C M
	JP cc, nn	If condition cc is true PC ← nn, else continue	
	JR e	PC ← PC + e	
	JR kk, e	If condition kk is true PC ← PC + e, else continue	kk ≡ NZ NC, Z C
	JP (ss)	PC ← ss	ss = HL, IX, IY
	DJNZ e	B ← B - 1, if B = 0 continue, else PC ← PC + e	
CALLS	CALL nn	$(SP-1) \leftarrow PC_H$ $(SP-2) \leftarrow PC_L$, PC ← nn	cc ≡ NZ PO, Z PE, NC P, C M
	CALL cc, nn	If condition cc is false continue, else same as CALL nn	
RESTARTS	RST L	$(SP-1) \leftarrow PC_H$ $(SP-2) \leftarrow PC_L$, $PC_H \leftarrow 0$ $PC_L \leftarrow L$	
RETURNS	RET	$PC_L \leftarrow (SP)$, $PC_H \leftarrow (SP+1)$	cc ≡ NZ PO, Z PE, NC P, C M
	RET cc	If condition cc is false continue, else same as RET	
	RETI	Return from interrupt, same as RET	
	RETN	Return from non-maskable interrupt	

T_A = 0°C to 70°C, Vcc = +5V ± 5%, Unless Otherwise Noted.

Signal	Symbol	Parameter	Min	Max	Unit	Test Condition
Φ	t_c	Clock Period	.4	[12]	μsec	
	$t_{w(\Phi H)}$	Clock Pulse Width, Clock High	180	[E]	nsec	
	$t_{w(\Phi L)}$	Clock Pulse Width, Clock Low	180	2000	nsec	
	$t_{r,f}$	Clock Rise and Fall Time		30	nsec	
A_{0-15}	$t_{D(AD)}$	Address Output Delay		145	nsec	C_L = 50pF
	$t_{F(AD)}$	Delay to Float		110	nsec	
	t_{acm}	Address Stable Prior to $\overline{MREQ}$ (Memory Cycle)	[1]		nsec	
	t_{aci}	Address Stable Prior to $\overline{IORQ}$, $\overline{RD}$ or $\overline{WR}$ (I/O Cycle)	[2]		nsec	
	t_{ca}	Address Stable from $\overline{RD}$ or $\overline{WR}$	[3]		nsec	
	t_{caf}	Address Stable From $\overline{RD}$ or $\overline{WR}$ During Float	[4]		nsec	
D_{0-7}	$t_{D(D)}$	Data Output Delay		260	nsec	C_L = 200pF
	$t_{F(D)}$	Delay to Float During Write Cycle		90	nsec	
	$t_{S\Phi(D)}$	Data Setup Time to Rising Edge of Clock During M1 Cycle	50		nsec	
	$t_{S\overline{\Phi}(D)}$	Data Setup Time to Falling Edge of Clock During M2 to M5	60		nsec	
	t_{dcm}	Data Stable Prior to $\overline{WR}$ (Memory Cycle)	[5]		nsec	
	t_{dci}	Data Stable Prior to $\overline{WR}$ (I/O Cycle)	[6]		nsec	
	t_{cdf}	Data Stable From $\overline{WR}$	[7]			
	t_H	Any Hold Time for Setup Time	0		nsec	
$\overline{MREQ}$	$t_{DL\overline{\Phi}(MR)}$	$\overline{MREQ}$ Delay From Falling Edge of Clock, $\overline{MREQ}$ Low		100	nsec	C_L = 50pF
	$t_{DH\Phi(MR)}$	$\overline{MREQ}$ Delay From Rising Edge of Clock, $\overline{MREQ}$ High		100	nsec	
	$t_{DH\overline{\Phi}(MR)}$	$\overline{MREQ}$ Delay From Falling Edge of Clock, $\overline{MREQ}$ High		100	nsec	
	$t_{w(\overline{MRL})}$	Pulse Width, $\overline{MREQ}$ Low	[8]		nsec	
	$t_{w(\overline{MRH})}$	Pulse Width, $\overline{MREQ}$ High	[9]		nsec	
$\overline{IORQ}$	$t_{DL\Phi(IR)}$	$\overline{IORQ}$ Delay From Rising Edge of Clock, $\overline{IORQ}$ Low		90	nsec	C_L = 50pF
	$t_{DL\overline{\Phi}(IR)}$	$\overline{IORQ}$ Delay From Falling Edge of Clock, $\overline{IORQ}$ Low		110	nsec	
	$t_{DH\Phi(IR)}$	$\overline{IORQ}$ Delay From Rising Edge of Clock, $\overline{IORQ}$ High		100	nsec	
	$t_{DH\overline{\Phi}(IR)}$	$\overline{IORQ}$ Delay From Falling Edge of Clock, $\overline{IORQ}$ High		110	nsec	
$\overline{RD}$	$t_{DL\Phi(RD)}$	$\overline{RD}$ Delay From Rising Edge of Clock, $\overline{RD}$ Low		100	nsec	C_L = 50pF
	$t_{DL\overline{\Phi}(RD)}$	$\overline{RD}$ Delay From Falling Edge of Clock, $\overline{RD}$ Low		130	nsec	
	$t_{DH\Phi(RD)}$	$\overline{RD}$ Delay From Rising Edge of Clock, $\overline{RD}$ High		100	nsec	
	$t_{DH\overline{\Phi}(RD)}$	$\overline{RD}$ Delay From Falling Edge of Clock, $\overline{RD}$ High		110	nsec	
$\overline{WR}$	$t_{DL\Phi(WR)}$	$\overline{WR}$ Delay From Rising Edge of Clock, $\overline{WR}$ Low		80	nsec	C_L = 50pF
	$t_{DL\overline{\Phi}(WR)}$	$\overline{WR}$ Delay From Falling Edge of Clock, $\overline{WR}$ Low		90	nsec	
	$t_{DH\Phi(WR)}$	$\overline{WR}$ Delay From Falling Edge of Clock, $\overline{WR}$ High		100	nsec	
	$t_{w(\overline{WRL})}$	Pulse Width, $\overline{WR}$ Low	[10]		nsec	
$\overline{M1}$	$t_{DL(M1)}$	$\overline{M1}$ Delay From Rising Edge of Clock, $\overline{M1}$ Low		130	nsec	C_L = 30pF
	$t_{DH(M1)}$	$\overline{M1}$ Delay From Rising Edge of Clock, $\overline{M1}$ High		130	nsec	
$\overline{RFSH}$	$t_{DL(RF)}$	$\overline{RFSH}$ Delay From Rising Edge of Clock, $\overline{RFSH}$ Low		180	nsec	C_L = 30pF
	$t_{DH(RF)}$	$\overline{RFSH}$ Delay From Rising Edge of Clock, $\overline{RFSH}$ High		150	nsec	
$\overline{WAIT}$	$t_{s(WT)}$	$\overline{WAIT}$ Setup Time to Falling Edge of Clock	70		nsec	
$\overline{HALT}$	$t_{D(HT)}$	$\overline{HALT}$ Delay Time From Falling Edge of Clock		300	nsec	C_L = 50pF
$\overline{INT}$	$t_{s(IT)}$	$\overline{INT}$ Setup Time to Rising Edge of Clock	80		nsec	
$\overline{NMI}$	$t_{w(\overline{NML})}$	Pulse Width, $\overline{NMI}$ Low	80		nsec	
$\overline{BUSRQ}$	$t_{s(BQ)}$	$\overline{BUSRQ}$ Setup Time to Rising Edge of Clock	80		nsec	
$\overline{BUSAK}$	$t_{DL(BA)}$	$\overline{BUSAK}$ Delay From Rising Edge of Clock, $\overline{BUSAK}$ Low		120	nsec	C_L = 50pF
	$t_{DH(BA)}$	$\overline{BUSAK}$ Delay From Falling Edge of Clock, $\overline{BUSAK}$ High		110	nsec	
$\overline{RESET}$	$t_{s(RS)}$	$\overline{RESET}$ Setup Time to Rising Edge of Clock	90		nsec	
	$t_{F(C)}$	Delay to Float ($\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$ and $\overline{WR}$)		100	nsec	
	t_{mr}	$\overline{M1}$ Stable Prior to $\overline{IORQ}$ (Interrupt Ack.)	[11]		nsec	

[12] $t_c = t_{w(\Phi H)} + t_{w(\Phi L)} + t_r + t_f$

[1] $t_{acm} = t_{w(\Phi H)} + t_f - 75$

[2] $t_{aci} = t_c - 80$

[3] $t_{ca} = t_{w(\Phi L)} + t_r - 40$

[4] $t_{caf} = t_{w(\Phi L)} + t_r - 60$

[5] $t_{dcm} = t_c - 180$

[6] $t_{dci} = t_{w(\Phi L)} + t_r - 180$

[7] $t_{cdf} = t_{w(\Phi L)} + t_r - 50$

[8] $t_{w(MRL)} = t_c - 40$

[9] $t_{w(MRH)} = t_{w(\Phi H)} + t_f - 30$

[10] $t_{w(WR)} = t_c - 40$

[11] $t_{mr} = 2t_c + t_{w(\Phi H)} + t_f - 80$

NOTES:

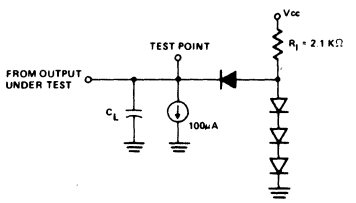
A. Data should be enabled onto the CPU data bus when $\overline{RD}$ is active. During interrupt acknowledge data should be enabled when $\overline{M1}$ and $\overline{IORQ}$ are both active.

B. All control signals are internally synchronized, so they may be totally asynchronous with respect to the clock.

C. The $\overline{RESET}$ signal must be active for a minimum of 3 clock cycles.

D. Output Delay vs. Loaded Capacitance
TA = 70°C Vcc = +5V ±5%
(1) ΔC_L = +100pF ($A_\phi - A_{15}$ and Control Signals), add 30 ns to timing shown.

E. Although static by design, testing guarantees $t_{w(\Phi H)}$ of 200 μsec maximum

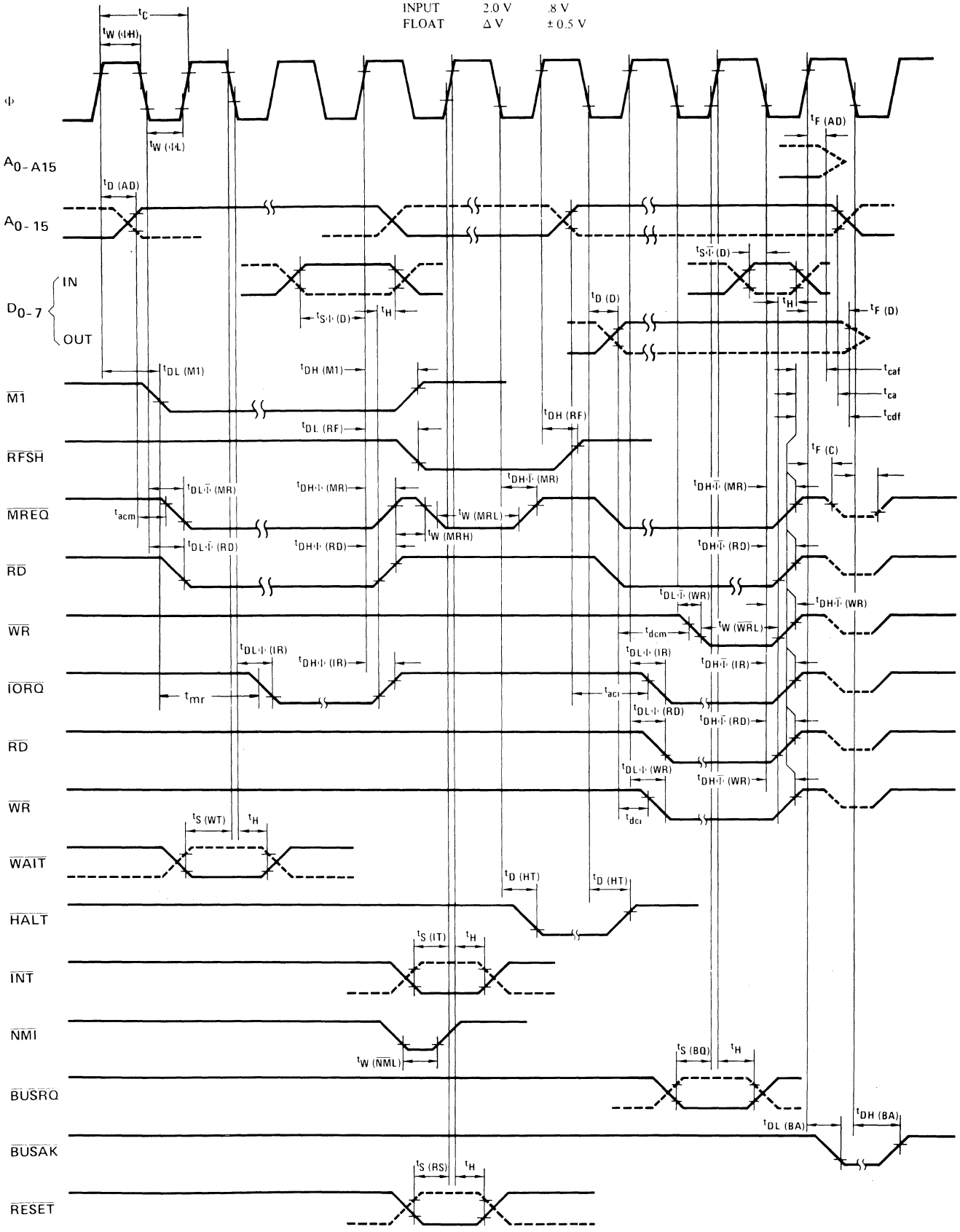


Load circuit for Output

A.C. Timing Diagram

Timing measurements are made at the following voltages, unless otherwise specified:

	"1"	"0"
CLOCK	4.2 V	.8 V
OUTPUT	2.0 V	.8 V
INPUT	2.0 V	.8 V
FLOAT	Δ V	± 0.5 V



Absolute Maximum Ratings

Temperature Under Bias	Specified operating range.
Storage Temperature	-65°C to +150°C
Voltage On Any Pin with Respect to Ground	-0.3V to +7V
Power Dissipation	1.5W

*Comment

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: For Z80-CPU all AC and DC characteristics remain the same for the military grade parts except I_{cc}.

I_{cc} = 200 mA

Z80-CPU D.C. Characteristics

T_A = 0°C to 70°C, V_{cc} = 5V ± 5% unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
V_{ILC}	Clock Input Low Voltage	-0.3		0.45	V	
V_{IHC}	Clock Input High Voltage	V_{cc} -.2 [1]		V_{cc}	V	
V_{IL}	Input Low Voltage	-0.3		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{cc}	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL}=1.8mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -250μA
I_{CC}	Power Supply Current			150	mA	t_c= 400nsec
I_{LI}	Input Leakage Current			10	μA	V_{IN}=0 to V_{cc}
I_{LOH}	Tri-State Output Leakage Current in Float			10	μA	V_{OUT}=2.4 to V_{cc}
I_{LOL}	Tri-State Output Leakage Current in Float			-10	μA	V_{OUT}=0.4V
I_{LD}	Data Bus Leakage Current in Input Mode			±10	μA	$0 \leq V_{IN} \leq V_{cc}$

Capacitance

T_A = 25°C, f = 1 MHz,
unmeasured pins returned to ground

Symbol	Parameter	Max.	Unit
C_Φ	Clock Capacitance	35	pF
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	10	pF

Z80-CPU Ordering Information

C – Ceramic
P – Plastic
S – Standard 5V ±5% 0° to 70°C
E – Extended 5V ±5% -40° to 85°C
M – Military 5V ±10% -55° to 125°C

Z80A-CPU D.C. Characteristics

T_A = 0°C to 70°C, V_{cc} = 5V ± 5% unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
V_{ILC}	Clock Input Low Voltage	-0.3		0.45	V	
V_{IHC}	Clock Input High Voltage	V_{cc} -.2		V_{cc}	V	
V_{IL}	Input Low Voltage	-0.3		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{cc}	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL}=1.8mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -250μA
I_{CC}	Power Supply Current		90	200	mA	t_c= 250nsec
I_{LI}	Input Leakage Current			10	μA	V_{IN}=0 to V_{cc}
I_{LOH}	Tri-State Output Leakage Current in Float			10	μA	V_{OUT}=2.4 to V_{cc}
I_{LOL}	Tri-State Output Leakage Current in Float			-10	μA	V_{OUT}=0.4V
I_{LD}	Data Bus Leakage Current in Input Mode			±10	μA	$0 \leq V_{IN} \leq V_{cc}$

Capacitance

T_A = 25°C, f = 1 MHz,
unmeasured pins returned to ground

Symbol	Parameter	Max.	Unit
C_Φ	Clock Capacitance	35	pF
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	10	pF

Z80A-CPU Ordering Information

C – Ceramic
P – Plastic
S – Standard 5V ±5% 0° to 70°C

T_A = O°C to 70°C, Vcc = +5V ± 5%, Unless Otherwise Noted.

Signal	Symbol	Parameter	Min	Max	Unit	Test Condition
Φ	t_c	Clock Period	.25	[12]	μsec	
	$t_{w(\Phi H)}$	Clock Pulse Width, Clock High	110	[E]	nsec	
	$t_{w(\Phi L)}$	Clock Pulse Width, Clock Low	110	2000	nsec	
	t_r, t_f	Clock Rise and Fall Time		30	nsec	
A_{0-15}	$t_{D(AD)}$	Address Output Delay		110	nsec	C_L = 50pF
	$t_{F(AD)}$	Delay to Float		90	nsec	
	t_{acm}	Address Stable Prior to $\overline{MREQ}$ (Memory Cycle)	[1]		nsec	
	t_{aci}	Address Stable Prior to $\overline{IORQ}$, $\overline{RD}$ or $\overline{WR}$ (I/O Cycle)	[2]		nsec	
	t_{ca}	Address Stable from $\overline{RD}$ or $\overline{WR}$	[3]		nsec	
	t_{caf}	Address Stable From $\overline{RD}$ or $\overline{WR}$ During Float	[4]		nsec	
D_{0-7}	$t_{D(D)}$	Data Output Delay		180	nsec	C_L = 200pF
	$t_{F(D)}$	Delay to Float During Write Cycle			nsec	
	$t_{S\Phi(D)}$	Data Setup Time to Rising Edge of Clock During M1 Cycle	35		nsec	
	$t_{S\overline{\Phi}(D)}$	Data Setup Time to Falling Edge of Clock During M2 to M5	50		nsec	
	t_{dcm}	Data Stable Prior to $\overline{WR}$ (Memory Cycle)	[5]		nsec	
	t_{dci}	Data Stable Prior to $\overline{WR}$ (I/O Cycle)	[6]		nsec	
	t_{cdf}	Data Stable From $\overline{WR}$	[7]			
	t_H	Any Hold Time for Setup Time		0	nsec	
$\overline{MREQ}$	$t_{DL\overline{\Phi}(MR)}$	$\overline{MREQ}$ Delay From Falling Edge of Clock, $\overline{MREQ}$ Low		75	nsec	C_L = 50pF
	$t_{DH\Phi(MR)}$	$\overline{MREQ}$ Delay From Rising Edge of Clock, $\overline{MREQ}$ High		75	nsec	
	$t_{DH\overline{\Phi}(MR)}$	$\overline{MREQ}$ Delay From Falling Edge of Clock, $\overline{MREQ}$ High		75	nsec	
	$t_{w(\overline{MRL})}$	Pulse Width, $\overline{MREQ}$ Low	[8]		nsec	
	$t_{w(\overline{MRH})}$	Pulse Width, $\overline{MREQ}$ High	[9]		nsec	
$\overline{IORQ}$	$t_{DL\Phi(IR)}$	$\overline{IORQ}$ Delay From Rising Edge of Clock, $\overline{IORQ}$ Low		75	nsec	C_L = 50pF
	$t_{DL\overline{\Phi}(IR)}$	$\overline{IORQ}$ Delay From Falling Edge of Clock, $\overline{IORQ}$ Low		80	nsec	
	$t_{DH\Phi(IR)}$	$\overline{IORQ}$ Delay From Rising Edge of Clock, $\overline{IORQ}$ High		80	nsec	
	$t_{DH\overline{\Phi}(IR)}$	$\overline{IORQ}$ Delay From Falling Edge of Clock, $\overline{IORQ}$ High		80	nsec	
$\overline{RD}$	$t_{DL\Phi(RD)}$	$\overline{RD}$ Delay From Rising Edge of Clock, $\overline{RD}$ Low		75	nsec	C_L = 50pF
	$t_{DL\overline{\Phi}(RD)}$	$\overline{RD}$ Delay From Falling Edge of Clock, $\overline{RD}$ Low		95	nsec	
	$t_{DH\Phi(RD)}$	$\overline{RD}$ Delay From Rising Edge of Clock, $\overline{RD}$ High		75	nsec	
	$t_{DH\overline{\Phi}(RD)}$	$\overline{RD}$ Delay From Falling Edge of Clock, $\overline{RD}$ High		80	nsec	
$\overline{WR}$	$t_{DL\Phi(WR)}$	$\overline{WR}$ Delay From Rising Edge of Clock, $\overline{WR}$ Low		60	nsec	C_L = 50pF
	$t_{DL\overline{\Phi}(WR)}$	$\overline{WR}$ Delay From Falling Edge of Clock, $\overline{WR}$ Low		80	nsec	
	$t_{DH\Phi(WR)}$	$\overline{WR}$ Delay From Falling Edge of Clock, $\overline{WR}$ High		80	nsec	
	$t_{w(\overline{WRL})}$	Pulse Width, $\overline{WR}$ Low	[10]		nsec	
$\overline{M1}$	$t_{DL(M1)}$	$\overline{M1}$ Delay From Rising Edge of Clock, $\overline{M1}$ Low		100	nsec	C_L = 30pF
	$t_{DH(M1)}$	$\overline{M1}$ Delay From Rising Edge of Clock, $\overline{M1}$ High		100	nsec	
$\overline{RFSH}$	$t_{DL(RF)}$	$\overline{RFSH}$ Delay From Rising Edge of Clock, $\overline{RFSH}$ Low		130	nsec	C_L = 30pF
	$t_{DH(RF)}$	$\overline{RFSH}$ Delay From Rising Edge of Clock, $\overline{RFSH}$ High		120	nsec	
$\overline{WAIT}$	$t_{s(WT)}$	$\overline{WAIT}$ Setup Time to Falling Edge of Clock	70		nsec	
$\overline{HALT}$	$t_{D(HT)}$	$\overline{HALT}$ Delay Time From Falling Edge of Clock		200	nsec	C_L = 50pF
$\overline{INT}$	$t_{s(IT)}$	$\overline{INT}$ Setup Time to Rising Edge of Clock	80		nsec	
$\overline{NMI}$	$t_{w(\overline{NML})}$	Pulse Width, $\overline{NMI}$ Low	80		nsec	
$\overline{BUSRQ}$	$t_{s(BQ)}$	$\overline{BUSRQ}$ Setup Time to Rising Edge of Clock	50		nsec	
$\overline{BUSAK}$	$t_{DL(BA)}$	$\overline{BUSAK}$ Delay From Rising Edge of Clock, $\overline{BUSAK}$ Low		100	nsec	C_L = 50pF
	$t_{DH(BA)}$	$\overline{BUSAK}$ Delay From Falling Edge of Clock, $\overline{BUSAK}$ High		100	nsec	
$\overline{RESET}$	$t_{s(RS)}$	$\overline{RESET}$ Setup Time to Rising Edge of Clock	60		nsec	
	$t_{F(C)}$	Delay to Float ($\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$ and $\overline{WR}$)		80	nsec	
	t_{mr}	M1 Stable Prior to IORQ (Interrupt Ack.)	[11]		nsec	

[12] $t_c = t_{w(\Phi H)} + t_{w(\Phi L)} + t_r + t_f$

[1] $t_{acm} = t_{w(\Phi H)} + t_f - 65$

[2] $t_{aci} = t_c - 70$

[3] $t_{ca} = t_{w(\Phi L)} + t_r - 30$

[4] $t_{caf} = t_{w(\Phi L)} + t_r - 45$

[5] $t_{dcm} = t_c - 140$

[6] $t_{dci} = t_{w(\Phi L)} + t_r - 140$

[7] $t_{cdf} = t_{w(\Phi L)} + t_r - 40$

[8] $t_{w(\overline{MRL})} = t_c - 30$

[9] $t_{w(\overline{MRH})} = t_{w(\Phi H)} + t_f - 20$

[10] $t_{w(WR)} = t_c - 30$

[11] $t_{mr} = 2t_c + t_{w(\Phi H)} + t_f - 65$

NOTES:

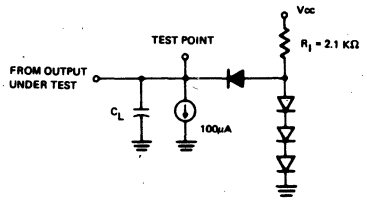
A. Data should be enabled onto the CPU data bus when $\overline{RD}$ is active. During interrupt acknowledge data should be enabled when $\overline{M1}$ and $\overline{IORQ}$ are both active.

B. All control signals are internally synchronized, so they may be totally asynchronous with respect to the clock.

C. The $\overline{RESET}$ signal must be active for a minimum of 3 clock cycles.

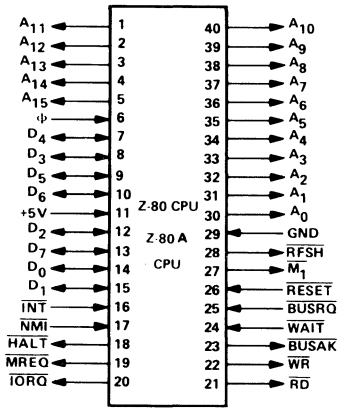
D. Output Delay vs. Loaded Capacitance
TA = 70°C Vcc = +5V ±5%
(a) ΔC_L = +100pF ($A_0 - A_{15}$ and Control Signals), add 30 ns to timing shown.

E. Although static by design, testing guarantees $t_{w(\Phi H)}$ of 200 μsec maximum

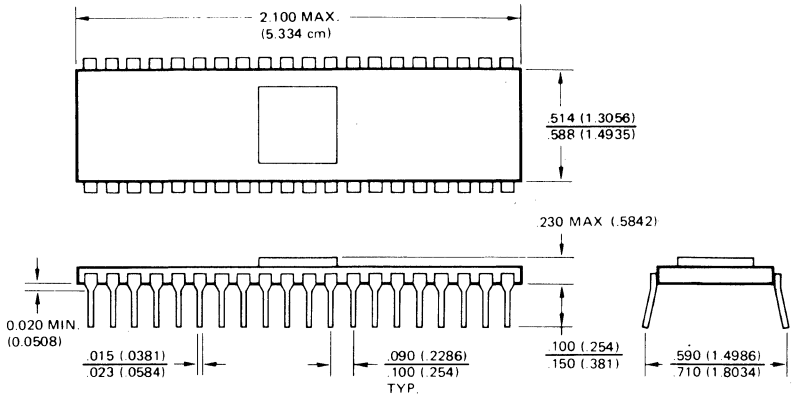


Load circuit for Output

Package Configuration



Package Outline



*Dimensions for metric system are in parentheses

Further Ordering Information

EASTERN REGION
Zilog, Inc.
400-1 Totten Pond Road
Waltham, MA 02154
TEL: (617) 890-0640
TWX: 710 324-1974

MIDWESTERN REGION
Zilog, Inc.
1701 Woodfield Place
Suite 417
Schaumburg, IL 60195
TEL: (312) 885-8080
TWX: 910 291-1064

WESTERN REGION
Zilog, Inc.
1815 Via el Prado
Redondo Beach, CA 90277
TEL: (213) 540-7749

Zilog

10460 Bubb Road, Cupertino, California 95014 ■ Telephone: (408) 446-4666 TWX: 910-338-7621

Printed in U.S.A.

Z80™-PIO
Z80™A-PIO

Zilog

Product Specification

The Zilog Z-80 product line is a complete set of microcomputer components, development systems and support software. The Z-80 microcomputer component set includes all of the circuits necessary to build high-performance microcomputer systems with virtually no other logic and a minimum number of low cost standard memory elements.

The Z-80 Parallel I/O (PIO) Interface Controller is a programmable, two port device which provides TTL compatible interfacing between peripheral devices and the Z80-CPU. The Z80-CPU configures the Z80-PIO to interface with standard peripheral devices such as tape punches, printers, keyboards, etc.

Structure

- N-Channel Silicon Gate Depletion Load technology
- 40 Pin DIP
- Single 5 volt supply
- Single phase 5 volt clock
- Two independent 8-bit bidirectional peripheral interface ports with "handshake" data transfer control

Features

- Interrupt driven "handshake" for fast response
- Any one of the following modes of operation may be selected for either port:
  - Byte output
  - Byte input
  - Byte bidirectional bus (available on Port A only)
  - Bit Mode
- Programmable interrupts on peripheral status conditions.
- Daisy chain priority interrupt logic included to provide for automatic interrupt vectoring without external logic.
- Eight outputs are capable of driving Darlington transistors.
- All inputs and outputs fully TTL compatible.

PIO Architecture

A block diagram of the Z80-PIO is shown in figure 1. The internal structure of the Z80-PIO consists of a Z80-CPU bus interface, internal control logic, Port A I/O logic, Port B I/O logic, and interrupt control logic. A typical application might use Port A as the data transfer channel and Port B for the status and control monitoring.

The Port I/O logic is composed of 6 registers with "handshake" control logic as shown in figure 2. The registers include: an 8-bit input register, an 8-bit output register, a 2-bit mode control register, an 8-bit mask register, an 8-bit input/output select register, and a 2-bit mask control register. The last three registers are used only when the port has been programmed to operate in the bit mode.

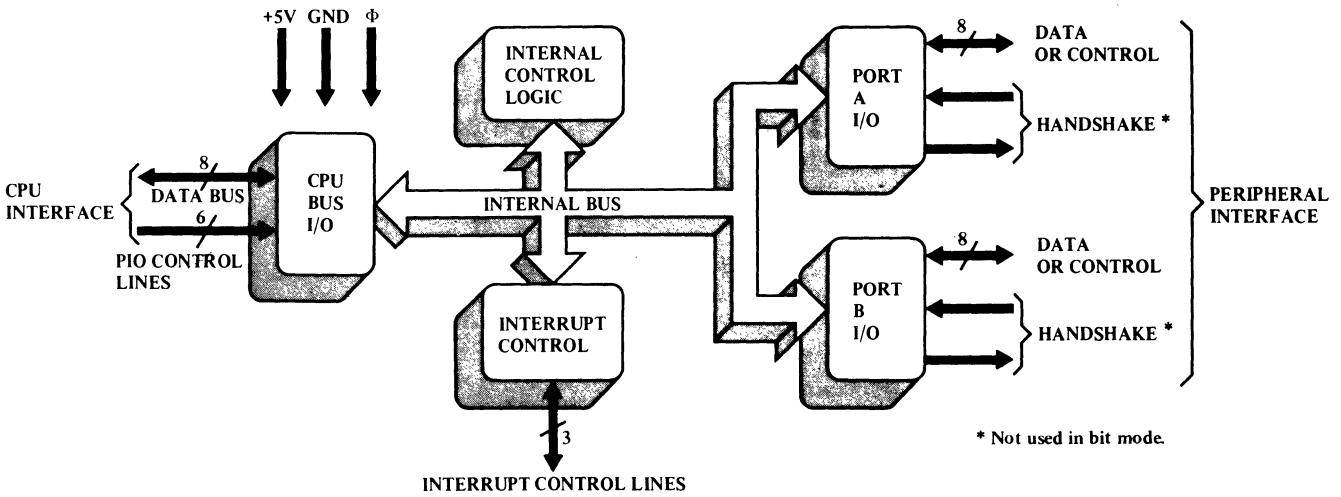


FIGURE 1
PIO BLOCK DIAGRAM

TM: Z80 is a registered trademark of Zilog, Inc.

Register Description

Mode Control Register–2 bits, loaded by CPU to select the operating mode: byte output, byte input, byte bidirectional bus or bit mode.

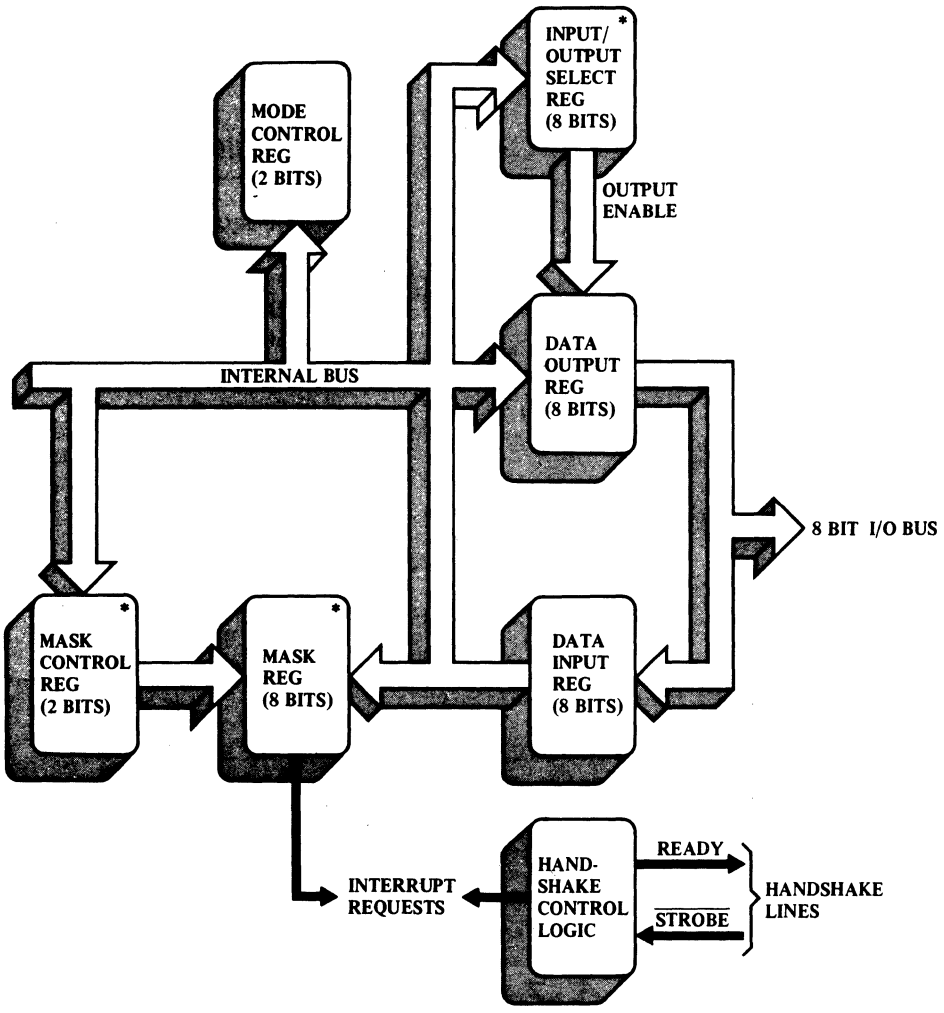
Data Output Register–8 bits, permits data to be transferred from the CPU to the peripheral.

Data Input Register–8 bits, accepts data from the peripheral for transfer to the CPU.

Mask Control Register–2 bits, loaded by the CPU to specify the active state (high or low) of any peripheral device interface pins that are to be monitored and, if an interrupt should be generated when all unmasked pins are active (AND condition) or, when any unmasked pin is active (OR condition).

Mask Register–8 bits, loaded by the CPU to determine which peripheral device interface pins are to be monitored for the specified status condition.

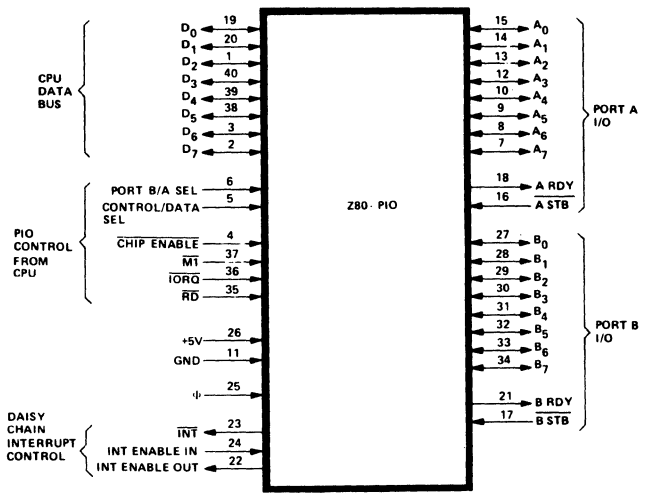
Input/Output Select Register–8 bits, loaded by the CPU to allow any pin to be an output or an input during bit mode operation.



* Used in the bit mode only to allow generation of an interrupt if the peripheral I/O pins go to the specified state.

FIGURE 2
A TYPICAL PORT I/O BLOCK DIAGRAM

Z80-PIO Pin Description

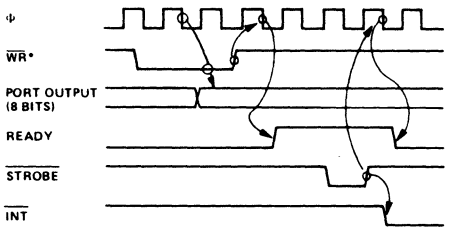


D_7-D_0	Z80-CPU Data Bus (bidirectional, tristate)
B/A Sel	Port B or A Select (input, active high)
C/D Sel	Control or Data Select (input, active high)
$\overline{CE}$	Chip Enable (input, active low)
Φ	System Clock (input)
$\overline{M1}$	Machine Cycle One Signal from CPU (input, active low)
$\overline{IORQ}$	Input/Output Request from Z80-CPU (input, active low)
$\overline{RD}$	Read Cycle Status from the Z80-CPU (input, active low)
IEI	Interrupt Enable In (input, active high)
IEO	Interrupt Enable Out (output, active high). IEI and IEO form a daisy chain connection for priority interrupt control.
$\overline{INT}$	Interrupt Request (output, open drain, active low)
A_0-A_7	Port A Bus (bidirectional, tristate)
$\overline{A\ STB}$	Port A Strobe Pulse from Peripheral Device (input, active low)
A RDY	Register A Ready (output, active high)
B_0-B_7	Port B Bus (bidirectional, tristate)
$\overline{B\ STB}$	Port B Strobe Pulse from Peripheral Device (input, active low)
B RDY	Register B Ready (output, active high)

Timing Waveforms

OUTPUT MODE

An output cycle is always started by the execution of an output instruction by the CPU. The $\overline{WR}$ pulse from the CPU latches the data from the CPU data bus into the selected port's output register. The write pulse sets the ready flag after a low going edge of Φ, indicating data is available. Ready stays active until the positive edge of the strobe line is received indicating that data was taken by the peripheral. The positive edge of the strobe pulse generates an $\overline{INT}$ if the interrupt enable flip flop has been set and if this device has the highest priority.

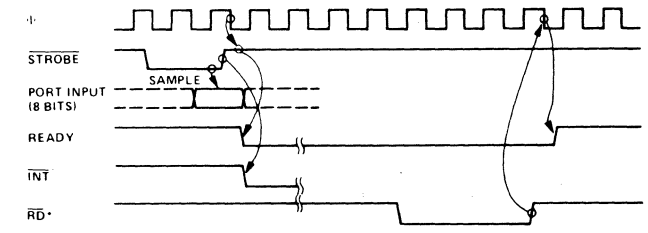


MODE 0 (OUTPUT) TIMING

$\overline{WR}^* = \overline{RD} \cdot CE \cdot \overline{C/D} \cdot \overline{IORQ}$

INPUT MODE

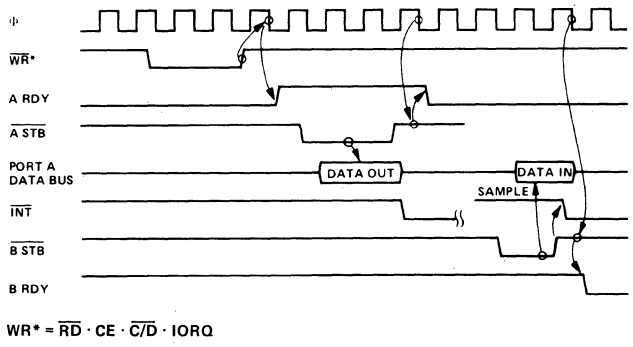
When $\overline{STROBE}$ goes low data is loaded into the selected port input register. The next rising edge of strobe activates $\overline{INT}$ if interrupt enable is set and this is the highest priority requesting device. The following falling edge of Φ resets Ready to an inactive state, indicating that the input register is full and cannot accept any more data until the CPU completes a read. When a read is complete the positive edge of $\overline{RD}$ will set Ready at the next low going transition of Φ. At this time new data can be loaded into the PIO.



$\overline{RD}^* = \overline{RD} \cdot CE \cdot \overline{C/D} \cdot \overline{IORQ}$ MODE 1 (INPUT) TIMING

BIDIRECTIONAL MODE

This is a combination of modes 0 and 1 using all four handshake lines and the 8 Port A I/O lines. Port B must be set to the Bit Mode. The Port A handshake lines are used for output control and the Port B lines are used for input control. Data is allowed out onto the Port A bus only when $\overline{A\ STB}$ is low. The rising edge of this strobe can be used to latch the data into the peripheral.

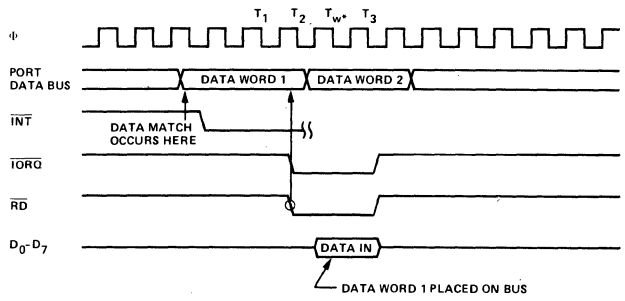


$WR^* = \overline{RD} \cdot CE \cdot \overline{C/D} \cdot IORQ$

BIT MODE

The bit mode does not utilize the handshake signals and a normal port write or port read can be executed at any time. When writing, the data will be latched into the output registers with the same timing as the output mode.

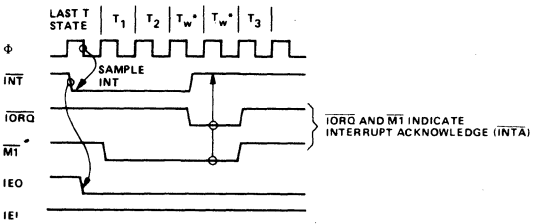
When reading the PIO, the data returned to the CPU will be composed of output register data from those port data lines assigned as outputs and input register data from those port data lines assigned as inputs. The input register will contain data which was present immediately prior to the falling edge of $\overline{RD}$. An interrupt will be generated if interrupts from the port are enabled and the data on the port data lines satisfy the logical equation defined by the 8-bit mask and 2-bit mask control registers.



* Timing Diagram Refers to Bit Mode Read.

INTERRUPT ACKNOWLEDGE

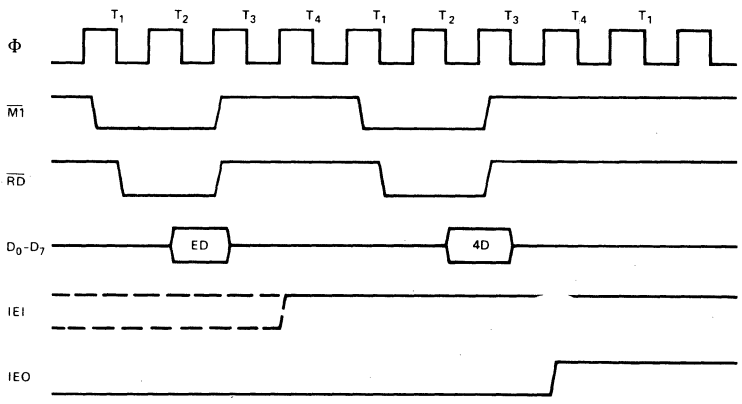
During $\overline{MI}$ time, peripheral controllers are inhibited from changing their interrupt enable status, permitting the $\overline{INT}$ Enable signal to ripple through the daisy chain. The peripheral with IEI high and IEO low during $\overline{INTA}$ will place a preprogrammed 8-bit interrupt vector on the data bus at this time. IEO is held low until a return from interrupt (RETI) instruction is executed by the CPU while IEI is high. The 2-byte RETI instruction is decoded internally by the PIO for this purpose.



RETURN FROM INTERRUPT CYCLE

If a Z80 peripheral device has no interrupt pending and is not under service, then its IEO=IEI. If it has an interrupt under service (i.e., it has already interrupted and received an interrupt acknowledge) then its IEO is always low, inhibiting lower priority chips from interrupting. If it has an interrupt pending which has not yet been acknowledged, IEO will be low unless an "ED" is decoded as the first byte of a two byte opcode. In this case, IEO will go high until the next opcode byte is decoded, whereupon it will again go low. If the second byte of the opcode was a "4D" then the opcode was an RETI instruction.

After an "ED" opcode is decoded, only the peripheral device which has interrupted and is currently under service will have its IEI high and its IEO low. This device is the highest priority device in the daisy chain which has received an interrupt acknowledge. All other peripherals have IEI=IEO. If the next opcode byte decoded is "4D", this peripheral device will reset its "interrupt under service" condition.



LOAD INTERRUPT VECTOR

The Z80-CPU requires an 8-bit interrupt vector be supplied by the interrupting device. The CPU forms the address for the interrupt service routine of the port using this vector. During an interrupt acknowledge cycle the vector is placed on the Z-80 data bus by the highest priority device requesting service at that time. The desired interrupt vector is loaded into the PIO by writing a control word to the desired port of the PIO with the following format.

D7	D6	D5	D4	D3	D2	D1	D0
V7	V6	V5	V4	V3	V2	V1	0

signifies this control word is an interrupt vector

SELECTING AN OPERATING MODE

When selecting an operating mode, the 2-bit mode control register is set to one of four values. These two bits are the most significant bits of the register, bits 7 and 6; bits 5 and 4 are not used while bits 3 through 0 are all set to 1111 to indicate "set mode."

D7	D6	D5	D4	D3	D2	D1	D0
M1	M0	X	X	1	1	1	1

mode word — signifies mode word to be set

X=unused bit

Mode	M_1	M_0
Output	0	0
Input	0	1
Bidirectional	1	0
Bit	1	1

MODE 0 active indicates that data is to be written from the CPU to the peripheral.

MODE 1 active indicates that data is to be read from the peripheral to the CPU.

MODE 2 allows data to be written to or read from the peripheral device.

MODE 3 is intended for status and control applications. When selected, the next control word must set the I/O Register to indicate which lines are to be input and which lines are to be output.

I/O = 1 sets bit to input.
I/O = 0 sets bit to output.

D7	D6	D5	D4	D3	D2	D1	D0
I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0

INTERRUPT CONTROL

Bit 7 = 1 — interrupt enable is set—allowing interrupt to be generated.

Bit 7 = 0 — indicates the enable flag is reset and interrupts may not be generated.

Bits 6,5,4 — are used in the bit mode interrupt operations; otherwise they are disregarded.

Bits 3,2,1,0 — signify that this command word is an interrupt control word.

D7	D6	D5	D4	D3	D2	D1	D0
Enable Interrupt	AND/ OR	High/ Low	Mask follows	0	1	1	1

used in Mode 3 only — signifies interrupt control word

If the "mask follows" bit is high (D4 = 1), the next control word written to the port must be the mask.

D7	D6	D5	D4	D3	D2	D1	D0
MB_7	MB_6	MB_5	MB_4	MB_3	MB_2	MB_1	MB_0

Only those port lines whose mask bit is a 0 will be monitored for generating an interrupt.

The interrupt enable flip-flop of a port may be set or reset without modifying the rest of the interrupt control word by the following command.

D7	D6	D5	D4	D3	D2	D1	D0
Int Enable	X	X	X	0	0	1	1

TA = 0° C to 70° C, Vcc = +5 V ± 5%, unless otherwise noted

SIGNAL	SYMBOL	PARAMETER	MIN	MAX	UNIT	COMMENTS
Φ	t_c	Clock Period	400	[1]	nsec	
	$t_{W(\Phi H)}$	Clock Pulse Width, Clock High	170	2000	nsec	
	$t_{W(\Phi L)}$	Clock Pulse Width, Clock Low	170	2000	nsec	
	t_r, t_f	Clock Rise and Fall Times		30	nsec	
	t_h	Any Hold Time for Specified Set-Up Time	0		nsec	
CS, $\overline{CE}$ ETC.	$t_{S\Phi(CS)}$	Control Signal Set-Up Time to Rising Edge of Φ During Read or Write Cycle	280		nsec	
D_0-D_7	$t_{DR(D)}$	Data Output Delay from Falling Edge of $\overline{RD}$		430	nsec	[2]
	$t_{S\Phi(D)}$	Data Set-Up Time to Rising Edge of ΦDuring Write or $\overline{M1}$ Cycle	50		nsec	C_L = 50 pf
	$t_{DI(D)}$	Data Output Delay from Falling Edge of $\overline{IORQ}$ During INTA Cycle.		340	nsec	[3]
	$t_{F(D)}$	Delay to Floating Bus (Output Buffer Disable Time)		160	nsec	
IEI	$t_{S(IEI)}$	IEI Set-Up Time to Falling Edge of $\overline{IORQ}$ During INTA Cycle	140		nsec	
IEO	$t_{DH(IO)}$	IEO Delay Time from Rising Edge of IEI		210	nsec	[5]
	$t_{DL(IO)}$	IEO Delay Time from Falling Edge of IEI		190	nsec	[5] C_L = 50 pf
	$t_{DM(IO)}$	IEO Delay from Falling Edge of $\overline{M1}$ (Interrupt Occurring Just Prior to $\overline{M1}$) See Note A.		300	nsec	[5]
$\overline{IORQ}$	$t_{S\Phi(IR)}$	$\overline{IORQ}$ Set-Up Time to Rising Edge of Φ During Read or Write Cycle	250		nsec	
$\overline{M1}$	$t_{S\Phi(M1)}$	$\overline{M1}$ Set-Up Time to Rising Edge of Φ During INTA or $\overline{M1}$ Cycle. See Note B.	210		nsec	
$\overline{RD}$	$t_{S\Phi(RD)}$	$\overline{RD}$ Set-Up Time to Rising Edge of Φ During Read or $\overline{M1}$ Cycle	240		nsec	
A_0-A_7, B_0-B_7	$t_{S(PD)}$	Port Data Set-Up Time to Rising Edge of $\overline{STROBE}$ (Mode 1)	260		nsec	
	*$t_{DS(PD)}$	Port Data Output Delay from Falling Edge of $\overline{STROBE}$ (Mode 2)		230	nsec	[5]
	$t_{F(PD)}$	Delay to Floating Port Data Bus from Rising Edge of $\overline{STROBE}$ (Mode 2)		200	nsec	C_L = 50 pf
	$t_{DI(PD)}$	Port Data Stable from Rising Edge of $\overline{IORQ}$ During WR Cycle (Mode 0)		200	nsec	[5]
$\overline{ASTB}$, $\overline{BSTB}$	$t_{W(ST)}$	Pulse Width, $\overline{STROBE}$	150		nsec	
			[4]		nsec	
$\overline{INT}$	$t_{D(IT)}$	$\overline{INT}$ Delay Time from Rising Edge of $\overline{STROBE}$		490	nsec	
	$t_{D(IT3)}$	$\overline{INT}$ Delay Time from Data Match During Mode 3 Operation		420	nsec	
ARDY, BRDY	$t_{DH(RY)}$	Ready Response Time from Rising Edge of $\overline{IORQ}$		t_c+ 460	nsec	[5] C_L = 50 pf
	$t_{DL(RY)}$	Ready Response Time from Rising Edge of $\overline{STROBE}$		t_c+ 400	nsec	[5]

A. 2.5 t_c > (N-2) $t_{DL(IO)}$ + $t_{DM(IO)}$ + $t_{S(IEI)}$ + TTL Buffer Delay, if any

B. $\overline{M1}$ must be active for a minimum of 2 clock periods to reset the PIO.

[1] $t_c = t_{W(\Phi H)} + t_{W(\Phi L)} + t_r + t_f$

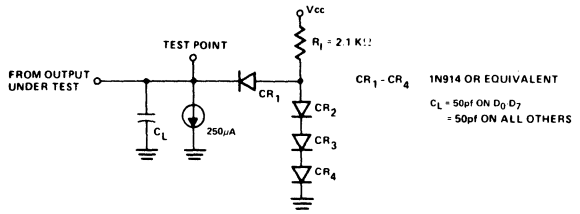
[2] Increase $t_{DR(D)}$ by 10 nsec for each 50 pf increase in loading up to 200 pf max.

[3] Increase $t_{DI(D)}$ by 10 nsec for each 50 pf increase in loading up to 200 pf max.

[4] For Mode 2: $t_{W(ST)} > t_{S(PD)}$

[5] Increase these values by 2 nsec for each 10 pf increase in loading up to 100 pf max.

Output load circuit.



Capacitance

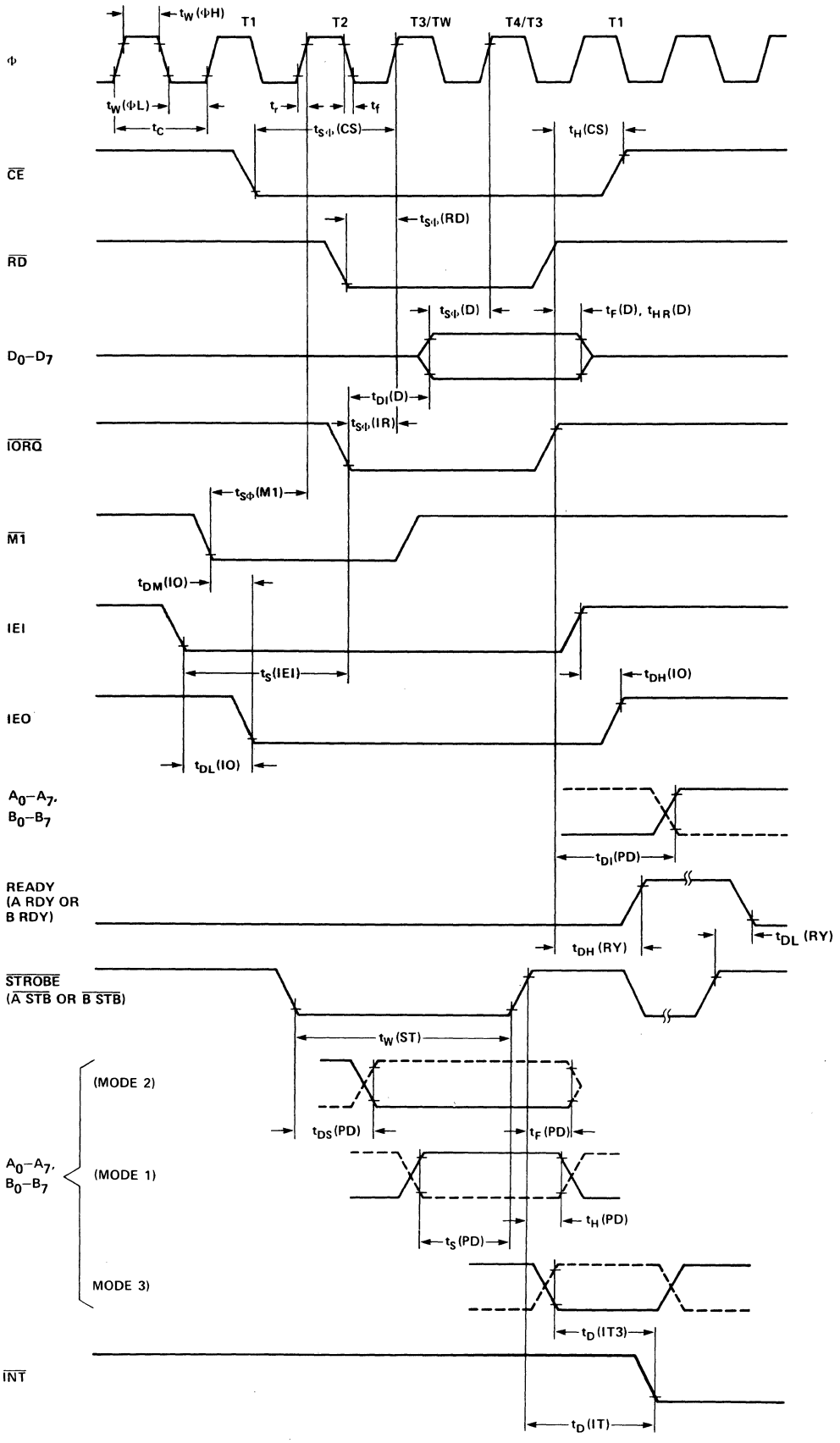
TA = 25° C, f = 1 MHz

Symbol	Parameter	Max.	Unit	Test Condition
C_Φ	Clock Capacitance	10	pF	Unmeasured Pins
C_{IN}	Input Capacitance	5	pF	Returned to Ground
C_{OUT}	Output Capacitance	10	pF	

A.C. Timing Diagram

Timing measurements are made at the following voltages, unless otherwise specified:

	"1"	"0"
CLOCK	4.2V	0.8V
OUTPUT	2.0V	0.8V
INPUT	2.0V	0.8V
FLOAT	ΔV	= +0.5V



Absolute Maximum Ratings

Temperature Under Bias	Specified operating range.
Storage Temperature	-65° C to +150° C
Voltage On Any Pin With Respect To Ground	-0.3 V to +7 V
Power Dissipation	.6 W

***Comment**

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: All AC and DC characteristics remain the same for the military grade parts except I_{CC}.

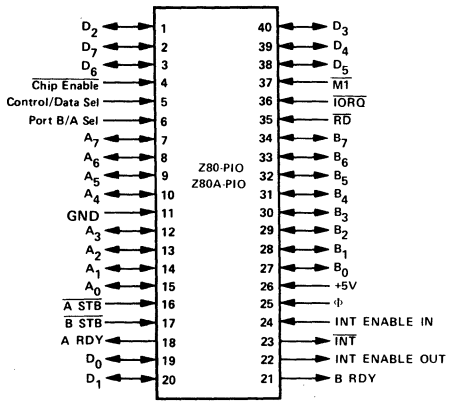
I_{CC} = 130 mA.

Z80-PIO and Z80A-PIO D.C. Characteristics

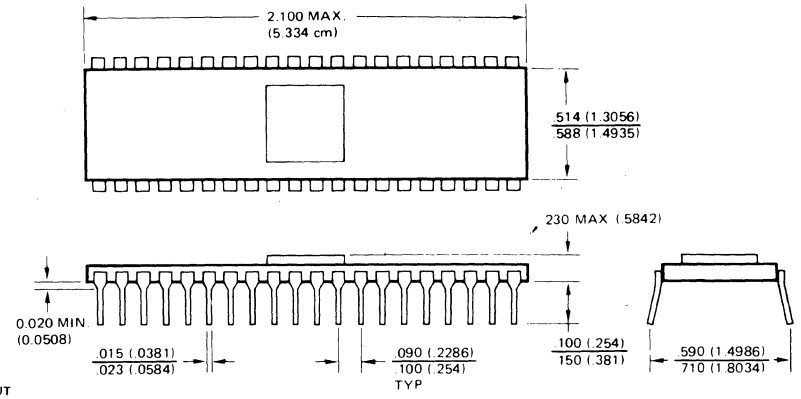
TA = 0° C to 70° C, Vcc = 5 V ± 5% unless otherwise specified

Symbol	Parameter	Min.	Max.	Unit	Test Condition
V_{ILC}	Clock Input Low Voltage	-0.3	.45	V	
V_{IHC}	Clock Input High Voltage	Vcc-.6	Vcc+.3	V	
V_{IL}	Input Low Voltage	-0.3	0.8	V	
V_{IH}	Input High Voltage	2.0	Vcc	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2.0 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} - 250 μA
I_{CC}	Power Supply Current		70	mA	
I_{LI}	Input Leakage Current		10	μA	V_{IN} = 0 to Vcc
I_{LOH}	Tri-State Output Leakage Current in Float		10	μA	V_{OUT} = 2.4 to Vcc
I_{LOL}	Tri-State Output Leakage Current in Float		-10	μA	V_{OUT} = 0.4 V
I_{LD}	Data Bus Leakage Current in Input Mode		±10	μA	$0 \leqslant V_{IN} \leqslant$ Vcc
I_{OHD}	Darlington Drive Current	-1.5		mA	V_{OH} = 1.5 V Port B Only

Package Configuration



Package Outline



*Dimensions for metric system are in parentheses

TA = 0° C to 70° C, Vcc = +5 V ± 5%, unless otherwise noted

SIGNAL	SYMBOL	PARAMETER	MIN	MAX	UNIT	COMMENTS
Φ	t_c	Clock Period	250	[1]	nsec	
	$t_{W(\Phi H)}$	Clock Pulse Width, Clock High	105	2000	nsec	
	$t_{W(\Phi L)}$	Clock Pulse Width, Clock Low	105	2000	nsec	
	t_r, t_f	Clock Rise and Fall Times		30	nsec	
	t_h	Any Hold Time for Specified Set-Up Time	0		nsec	
CS, $\overline{CE}$ ETC.	$t_{S\Phi}$ (CS)	Control Signal Set-Up Time to Rising Edge of Φ During Read or Write Cycle	145		nsec	
D_0-D_7	t_{DR} (D)	Data Output Delay From Falling Edge of $\overline{RD}$		380	nsec	[2]
	$t_{S\Phi}$ (D)	Data Set-Up Time to Rising Edge of Φ During Write or $\overline{M1}$ Cycle	50		nsec	C_L = 50 pf
	t_{DI} (D)	Data Output Delay from Falling Edge of $\overline{IORQ}$ During INTA Cycle		250	nsec	[3]
	t_F (D)	Delay to Floating Bus (Output Buffer Disable Time)		110	nsec	
IEI	t_S (IEI)	IEI Set-Up Time to Falling edge of $\overline{IORQ}$ During INTA Cycle	140		nsec	
IEO	t_{DH} (IO)	IEO Delay Time from Rising Edge of IEI		160	nsec	[5]
	t_{DL} (IO)	IEO Delay Time from Falling Edge of IEI		130	nsec	[5] C_L = 50 pf
	t_{DM} (IO)	IEO Delay from Falling Edge of $\overline{M1}$ (Interrupt Occurring Just Prior to $\overline{M1}$) See Note A.		190	nsec	[5]
$\overline{IORQ}$	$t_{S\Phi}$ (IR)	$\overline{IORQ}$ Set-Up Time to Rising Edge of Φ During Read or Write Cycle.	115		nsec	
$\overline{M1}$	$t_{S\Phi}$ (M1)	$\overline{M1}$ Set-Up Time to Rising Edge of Φ During INTA or $\overline{M1}$ Cycle See Note B	90		nsec	
$\overline{RD}$	$t_{S\Phi}$ (RD)	$\overline{RD}$ Set-Up Time to Rising Edge of Φ During Read or $\overline{M1}$ Cycle	115		nsec	
A_0-A_7, B_0-B_7	t_S (PD)	Port Data Set-Up Time to Rising Edge of $\overline{STROBE}$ (Mode 1)	230		nsec	
	t_{DS} (PD)	Port Data Ourput Delay from Falling Edge of $\overline{STROBE}$ (Mode 2)		210	nsec	[5]
	t_F (PD)	Delay to Floating Port Data Bus from Rising Edge of $\overline{STROBE}$ (Mode 2)		180	nsec	C_L = 50 pf
	t_{DI} (PD)	Port Data Stable from Rising Edge of $\overline{IORQ}$ During WR Cycle (Mode 0)		180	nsec	[5]
$\overline{ASTB}$, $\overline{BSTB}$	t_W (ST)	Pulse Width, $\overline{STROBE}$	150 [4]		nsec nsec	
$\overline{INT}$	t_D (IT)	$\overline{INT}$ Delay time from Rising Edge of $\overline{STROBE}$		440	nsec	
	t_D (IT3)	$\overline{INT}$ Delay Time from Data Match During Mode 3 Operation		380	nsec	
ARDY, BRDY	t_{DH} (RY)	Ready Response Time from Rising Edge of $\overline{IORQ}$		t_c+ 410	nsec	[5] C_L = 50 pf
	t_{DL} (RY)	Ready Response Time from Rising Edge of $\overline{STROBE}$		t_c+ 360	nsec	[5]

A. $2.5\,t_c > (N-2)\,t_{DL}$ (IO) + t_{DM} (IO) + t_S (IEI) + TTL Buffer Delay, if any

B. $\overline{M1}$ must be active for a minimum of 2 clock periods to reset the PIO.

[1] $t_c = t_{W(\Phi H)} + t_{W(\Phi L)} + t_r + t_f$

[2] Increase t_{DR} (D) by 10 nsec for each 50 pf increase in loading up to 200 pf max.

[3] Increase t_{DI} (D) by 10 nsec for each 50 pf increase in loading up to 200 pf max.

[4] For Mode 2: t_W (ST) > t_S (PD)

[5] Increase these values by 2 nsec for each 10 pf increase in loading up to 100 pf max.

This page intentionally left blank.

Z80™-CTC
Z80A™-CTC

Zilog

Product Specification

The Zilog Z80 product line is a complete set of microcomputer components, development systems and support software. The Z80 microcomputer component set includes all of the circuits necessary to build high-performance microcomputer systems with virtually no other logic and a minimum number of low cost standard memory elements.

The Z80-Counter Timer Circuit (CTC) is a programmable, four channel device that provides counting and timing functions for the Z80-CPU. The Z80-CPU configures the Z80-CTC's four independent channels to operate under various modes and conditions as required.

Structure

- N-Channel Silicon Gate Depletion Load Technology
- 28 Pin DIP
- Single 5 volt supply
- Single phase 5 volt clock
- Four independent programmable 8-bit counter/16-bit timer channels

Features

- Each channel may be selected to operate in either a counter mode or timer mode.
- Programmable interrupts on counter or timer states.
- A time constant register automatically reloads the down counter at zero and the cycle is repeated.
- Readable down counter indicates number of counts-to-go until zero.
- Selectable 16 or 256 clock prescaler for each timer channel.
- Selectable positive or negative trigger may initiate timer operation.
- Three channels have zero count/timeout outputs capable of driving Darlington transistors.
- Daisy chain priority interrupt logic included to provide for automatic interrupt vectoring without external logic.
- All inputs and outputs fully TTL compatible.

CTC Architecture

A block diagram of the Z80-CTC is shown in figure 1. The internal structure of the Z80-CTC consists of a Z80-CPU bus interface, internal control logic, four counter channels, and interrupt control logic. Each channel has an interrupt vector for automatic interrupt vectoring, and interrupt priority is determined by channel number with channel Ø having the highest priority.

The channel logic is composed of 2 registers, 2 counters and control logic as shown in figure 2. The registers include an 8-bit time constant register and an 8-bit channel control register. The counters include an 8-bit readable down counter and an 8-bit prescaler. The prescaler may be programmed to divide the system clock by either 16 or 256.

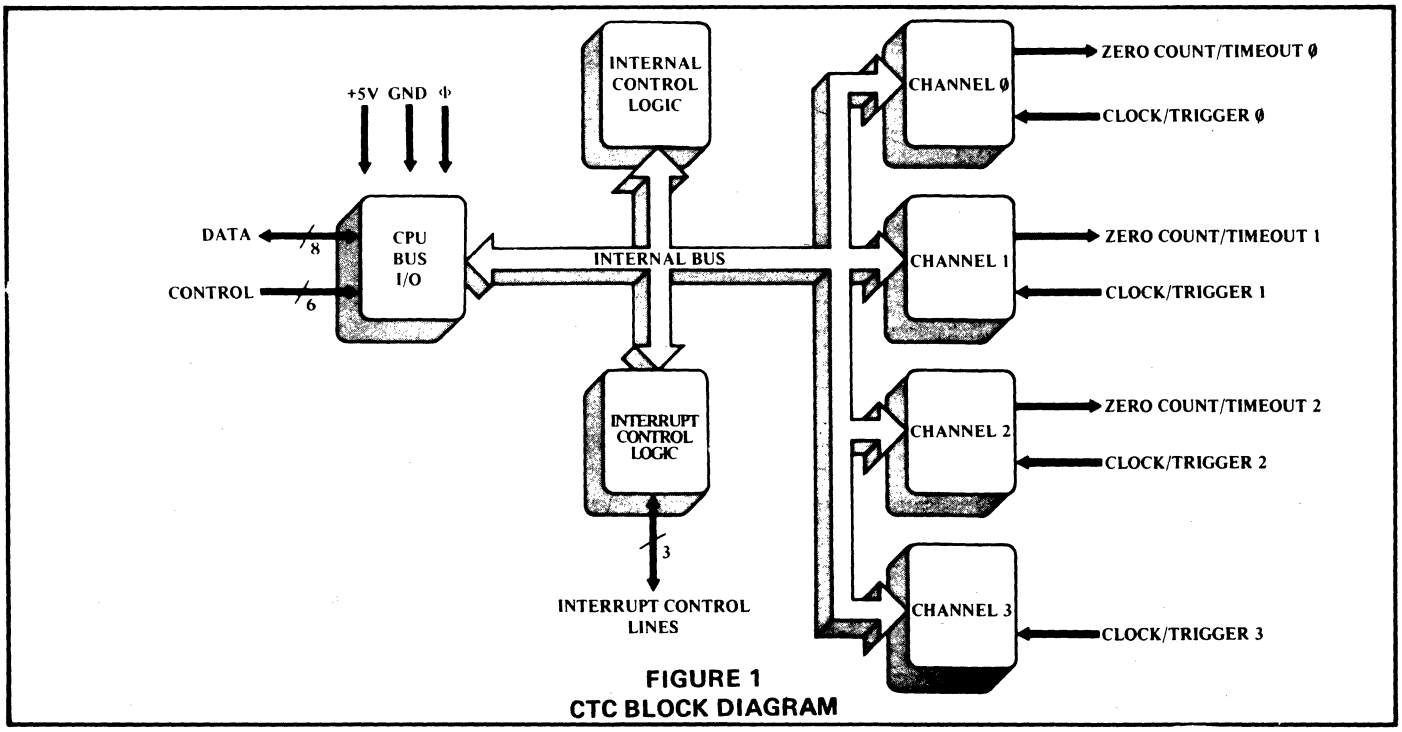


FIGURE 1
CTC BLOCK DIAGRAM

TM: Z80 is a trademark of Zilog, Inc.

Time Constant Register – 8 bits, loaded by the CPU to initialize and re-load Down Counter at a count of zero.

Channel Control Register – 8 bits, loaded by the CPU to select the mode and conditions of channel operation.

Down Counter – 8 bits, loaded by the Time Constant Register under program control and automatically at a count of zero. At any time, the CPU can read the number of counts-to-go until a zero count. This counter is decremented by the prescaler in timer mode and CLK/TRIG in counter mode.

Prescaler – 8 bit counter, divides system clock by 16 or 256 for decrementing Down Counter. It is used in timer mode only.

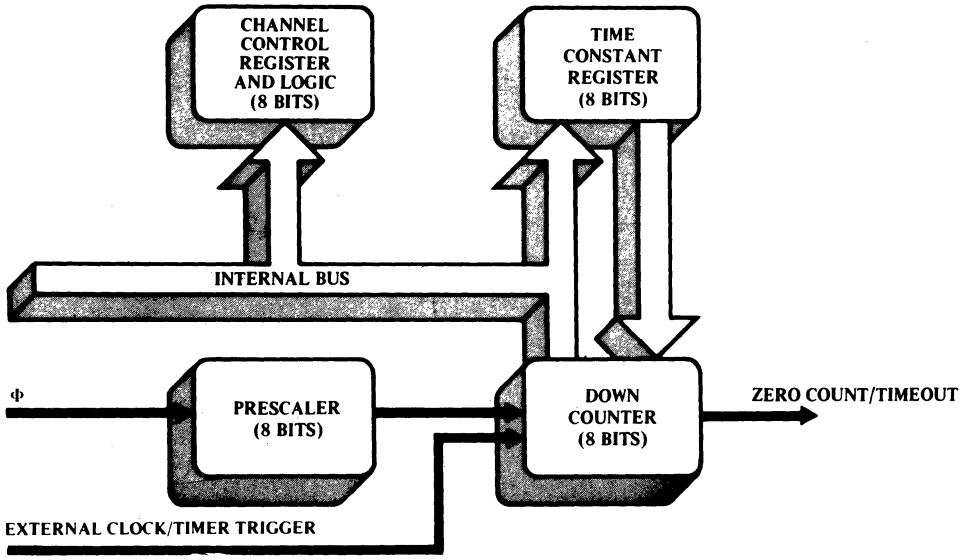
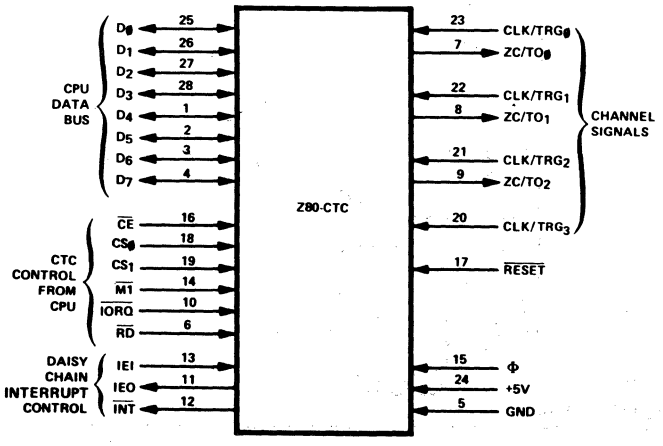


FIGURE 2
CHANNEL BLOCK DIAGRAM

Z80-CTC Pin Description



CLK/TRGϕ	Channel ϕ External Clock or Timer Trigger (Input)
CLK/TRG1	Channel 1 External Clock or Timer Trigger (Input)
CLK/TRG2	Channel 2 External Clock or Timer Trigger (Input)
CLK/TRG3	Channel 3 External Clock or Timer Trigger (Input)
ZC/TOϕ	Channel ϕ Zero Count or Timeout (output, active high)

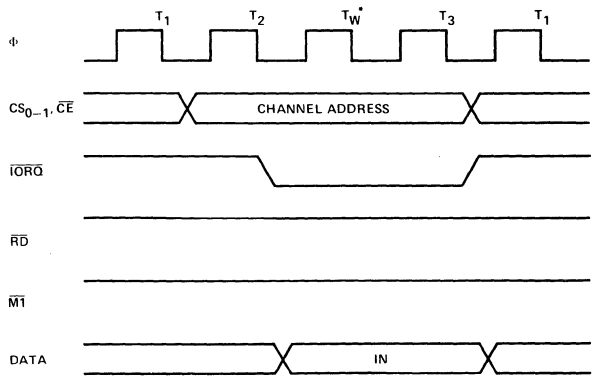
Z80-CTC Pin Description (continued)

ZC/TO_1	Channel 1 Zero Count or Timeout (output, active high)
ZC/TO_2	Channel 2 Zero Count or Timeout (output, active high)
$CS_1 - CS_\emptyset$	Channel Select (input, active high). These form a 2-bit binary address of the channel to be accessed.
$D7 - D_\emptyset$	Z80-CPU Data Bus (bidirectional, tristate)
$\overline{CE}$	Chip Enable (input, active low)
Φ	System Clock (input)
$\overline{M1}$	Machine Cycle One Signal from Z80-CPU (input, active low)
$\overline{IORQ}$	Input/Output Request from Z80-CPU (input, active low)
$\overline{RD}$	Read Cycle Status from the Z80-CPU (input, active low)
IEI	Interrupt Enable In (input, active high)
IEO	Interrupt Enable Out (output, active high). IEI and IEO form a daisy chain connection for priority interrupt control
$\overline{INT}$	Interrupt Request (output, open drain, active low)
$\overline{RESET}$	RESET stops all channels from counting and resets channel interrupt enable bits in all control registers. During reset time $ZC/TO_{\emptyset-2}$ and $\overline{INT}$ go to the inactive states, IEO reflects the state of IEI, and the data bus output drive go to the high impedance state (input, active low)

Timing Waveforms

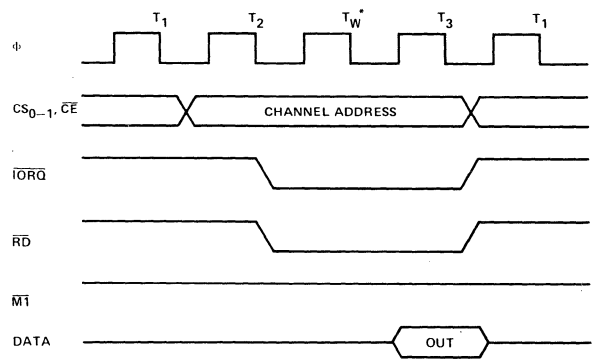
CTC WRITE CYCLE

Illustrated here is the timing for loading a channel control word, time constant and interrupt vector. No wait states are allowed for writing to the CTC other than the automatically inserted (T_W*). Since the CTC does not receive a specific write signal, it internally generates its own from the lack of an $\overline{RD}$ signal.



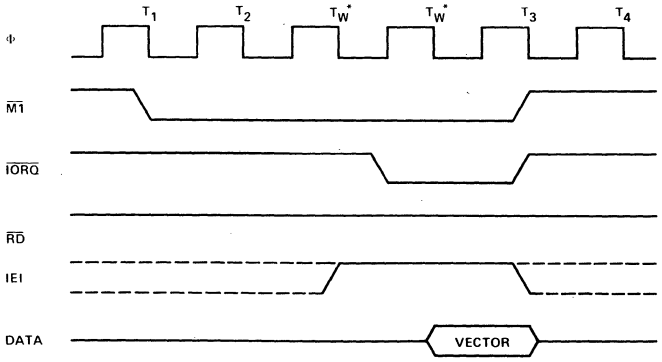
CTC READ CYCLE

Illustrated here is the timing for reading a channel's Down Counter when in Counter Mode. The value read onto the data bus reflects the number of external clock's rising edges prior to the rising edge of cycle (T_2). No wait states are allowed for reading the CTC other than the automatically inserted (T_W*).



INTERRUPT ACKNOWLEDGE CYCLE

Some time after an interrupt is requested by the CTC, the CPU will send out an interrupt acknowledge ($\overline{M1}$ and $\overline{IORQ}$). During this time the interrupt logic of the CTC will determine the highest priority channel which is requesting an interrupt. To insure that the daisy chain enable lines stabilize, channels are inhibited from changing their interrupt request status when $\overline{M1}$ is active. If the CTC Interrupt Enable Input (IEI) is active, then the highest priority interrupting channel places the contents of its interrupt vector register onto the Data Bus when $\overline{IORQ}$ goes active. Additional wait cycles are allowed.



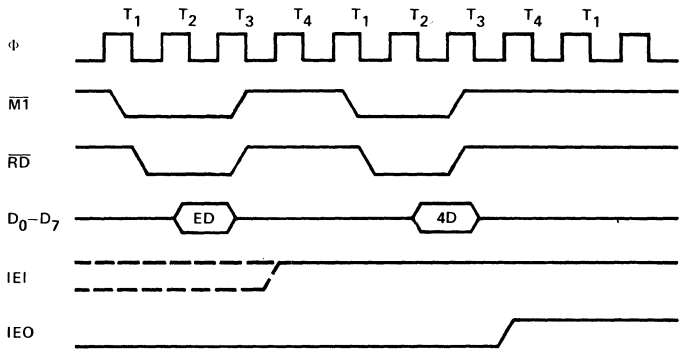
Timing Waveforms (continued)

RETURN FROM INTERRUPT CYCLE

If a Z80 peripheral device has no interrupt pending and is not under service, then its IEO = IEI. If it has an interrupt under service (i.e. it has already interrupted and received an interrupt acknowledge) then its IEO is always low, inhibiting lower priority chips from interrupting. If it has an interrupt pending which has not yet been acknowledged, IEO will be low unless an "ED" is decoded as the first byte of a two byte opcode. In this case, IEO will go high until the next opcode byte is decoded, whereupon it will again go low. If the second byte of the opcode was a "4D" then the opcode was an RETI instruction.

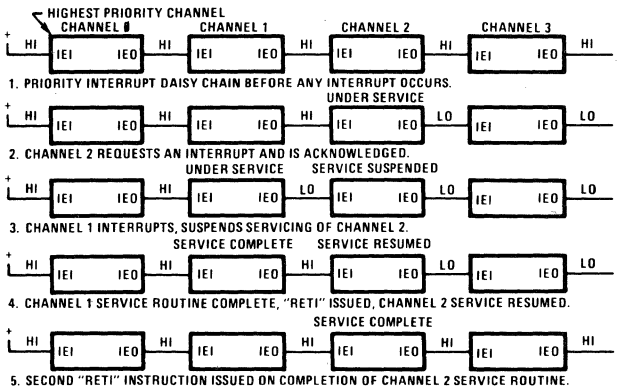
After an "ED" opcode is decoded, only the peripheral device which has interrupted and is currently under service will have its IEI high and its IEO low. This device is the highest priority device in the daisy chain which has received an interrupt acknowledge. All other peripherals have IEI = IEO. If the next opcode byte decoded is "4D", this peripheral device will reset its "interrupt under service" condition.

Wait cycles are allowed in the $\overline{M1}$ cycles.



DAISY CHAIN INTERRUPT SERVICING

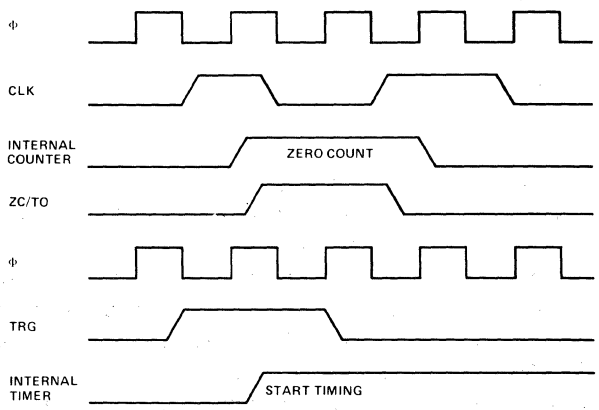
Illustrated at right is a typical nested interrupt sequence which may occur in the CTC. In this sequence channel 2 interrupts and is granted service. While this channel is being serviced, higher priority channel 1 interrupts and is granted service. The service routine for the higher priority channel is completed and a RETI instruction is executed to indicate to the channel that its routine is complete. At this time the service routine of lower priority channel 2 is completed.



CTC COUNTING AND TIMING

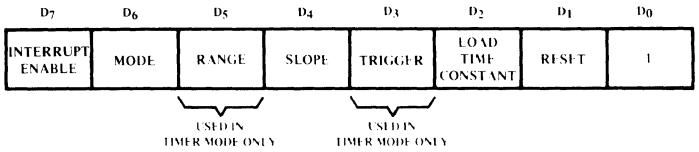
In the counter mode the rising or falling edge of the CLK input causes the counter to be decremented. The edge is detected totally asynchronously and must have a minimum CLK pulse width. However, the counter is synchronous with Φ therefore a setup time must be met when it is desired to have the counter decremented by the next rising edge of Φ.

In the timer mode the prescaler may be enabled by a rising or falling edge on the TRG input. As in the counter mode, the edge is detected totally asynchronously and must have a minimum TRG pulse width. However, when timing is to start with respect to the next rising edge of Φ a setup time must be met. The prescaler counts rising edges of Φ.



SELECTING AN OPERATING MODE

When selecting a channel's operating mode, bit Ø is set to 1 to indicate this word is to be stored in the channel control register.



Bit 7 = Ø — Channel interrupts disabled.

Bit 7 = 1 — Channel interrupts enabled to occur every time Down Counter reaches a count of zero. Setting Bit 7 does not let a preceding count of zero cause an interrupt.

Bit 6 = Ø — Timer Mode – Down counter is clocked by the prescaler. The period of the counter is:
$t_C \bullet P \bullet TC$
t_C = system clock period
P = prescale of 16 or 256
TC = 8 bit binary programmable time constant (256 max)

Bit 6 = 1 — Counter Mode – Down Counter is clocked by external clock. The prescaler is not used.

Bit 5 = Ø — Timer Mode Only–System clock Φ is divided by 16 in prescaler.

Bit 5 = 1 — Timer Mode Only–System clock Φ is divided by 256 in prescaler.

Bit 4 = Ø — Timer Mode – negative edge trigger starts timer operation.
Counter Mode – negative edge decrements the down counter.

Bit 4 = 1 — Timer Mode – positive edge trigger starts timer operation.
Counter Mode – positive edge decrements the down counter.

Bit 3 = Ø — Timer Mode Only – Timer begins operation on the rising edge of T_2 of the machine cycle following the one that loads the time constant.

Bit 3 = 1 — Timer Mode Only – External trigger is valid for starting timer operation after rising edge of T_2 of the machine cycle following the one that loads the time constant. The Prescaler is decremented 2 clock cycles later if the setup time is met, otherwise 3 clock cycles.

Bit 2 = Ø — No time constant will follow the channel control word. One time constant must be written to the channel to initiate operation.

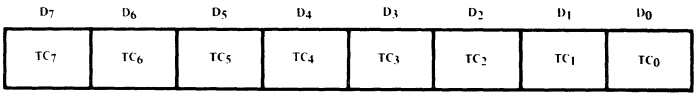
Bit 2 = 1 — The time constant for the Down Counter will be the next word written to the selected channel. If a time constant is loaded while a channel is counting, the present count will be completed before the new time constant is loaded into the Down Counter.

Bit 1 = Ø — Channel continues counting.

Bit 1 = 1 — Stop operation. If Bit 2 = 1 channel will resume operation after loading a time constant, otherwise a new control word must be loaded.

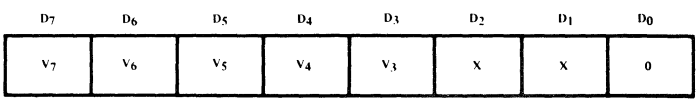
LOADING A TIME CONSTANT

An 8-bit time constant is loaded into the Time Constant register following a channel control word with bit 2 set. All zeros indicate a time constant of 256.



LOADING AN INTERRUPT VECTOR

The Z80-CPU requires that an 8-bit interrupt vector be supplied by the interrupting channel. The CPU forms the address for the interrupt service routine of the channel using this vector. During an interrupt acknowledge cycle the vector is placed on the Z80 Data Bus by the highest priority channel requesting service at that time. The desired interrupt vector is loaded into the CTC by writing into channel Ø with a zero in DØ. D7-D3 contain the stored interrupt vector, D_2 and D_1 are not used in loading the vector. When the CTC responds to an interrupt acknowledge, these two bits contain the binary code of the highest priority channel which requested the interrupt and DØ contains a zero since the address of the interrupt service routine starts at an even byte. Channel Ø is the highest priority channel.

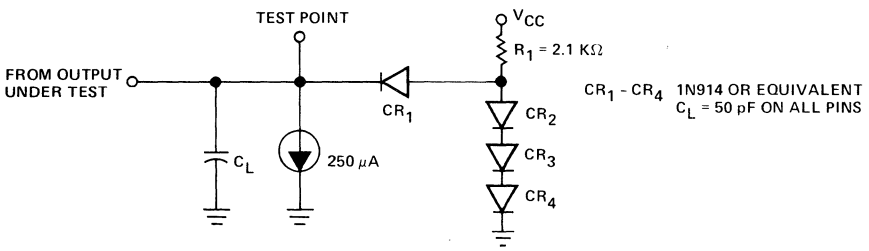


TA = 0° C to 70° C, Vcc = +5 V ± 5%, unless otherwise noted

Signal	Symbol	Parameter	Min	Max	Unit	Comments
Φ	t_C	Clock Period	400	[1]	ns	
	$t_W(\Phi H)$	Clock Pulse Width, Clock High	170	2000	ns	
	$t_W(\Phi L)$	Clock Pulse Width, Clock Low	170	2000	ns	
	t_r, t_f	Clock Rise and Fall Times		30	ns	
	t_H	Any Hold Time for Specified Setup Time	0		ns	
CS, $\overline{CE}$, etc.	$t_{S\Phi}(CS)$	Control Signal Setup Time to Rising Edge of Φ During Read or Write Cycle	160		ns	
D_0–D_7	$t_{DR}(D)$	Data Output Delay from Rising Edge of $\overline{RD}$ During Read Cycle		480	ns	[2]
	$t_{S\Phi}(D)$	Data Setup Time to Rising Edge of Φ During Write or M1 Cycle	60		ns	
	$t_{DI}(D)$	Data Output Delay from Falling Edge of IORQ During INTA Cycle		340	ns	[2]
	$t_F(D)$	Delay to Floating Bus (Output Buffer Disable Time)		230	ns	
IEI	$t_S(IEI)$	IEI Setup Time to Falling Edge of $\overline{IORQ}$ During INTA Cycle	200		ns	
IEO	$t_{DH}(IO)$	IEO Delay Time from Rising Edge of IEI		220	ns	[3]
	$t_{DL}(IO)$	IEO Delay Time from Falling Edge of IEI		190	ns	[3]
	$t_{DM}(IO)$	IEO Delay from Falling Edge of $\overline{M1}$ (Interrupt Occurring just Prior to $\overline{M1}$)		300	ns	[3]
$\overline{IORQ}$	$t_{S\Phi}(IR)$	$\overline{IORQ}$ Setup Time to Rising Edge of Φ During Read or Write Cycle	250		ns	
$\overline{M1}$	$t_{S\Phi}(M1)$	$\overline{M1}$ Setup Time to Rising Edge of Φ During INTA or M1 Cycle	210		ns	
$\overline{RD}$	$t_{S\Phi}(RD)$	$\overline{RD}$ Setup Time to Rising Edge of Φ During Read or M1 Cycle	240		ns	
$\overline{INT}$	$t_{DCK}(IT)$	$\overline{INT}$ Delay Time from Rising Edge of CLK/TRG		$2t_C(\Phi)$ + 200		Counter Mode
	$t_{D\Phi}(IT)$	$\overline{INT}$ Delay Time from Rising Edge of Φ		$t_C(\Phi)$ + 200		Timer Mode
CLK/TRG_{0-3}	$t_C(CK)$	Clock Period	$2t_C(\Phi)$			Counter Mode
	t_r, t_f	Clock and Trigger Rise and Fall Times		50		
	$t_S(CK)$	Clock Setup Time to Rising Edge of Φ for Immediate Count	210			Counter Mode
	$t_S(TR)$	Trigger Setup Time to Rising Edge of Φ for Enabling of Prescaler on Following Rising Edge of Φ	210			Timer Mode
	$t_W(CTH)$	Clock and Trigger High Pulse Width	200			Counter and Timer Modes
	$t_W(CTL)$	Clock and Trigger Low Pulse Width	200			Counter and Timer Modes
ZC/TO_{0-2}	$t_{DH}(ZC)$	ZC/TO Delay Time from Rising Edge of Φ, ZC/TO High		190		Counter and Timer Modes
	$t_{DL}(ZC)$	ZC/TO Delay Time from Falling Edge of Φ, ZC/TO Low		190		Counter and Timer Modes

Notes: [1] $t_C = t_W(\Phi H) + t_W(\Phi L) + t_r + t_f$.
[2] Increase delay by 10 nsec for each 50 pF increase in loading, 200 pF maximum for data lines and 100 pF for control lines.
[3] Increase delay by 2 nsec for each 10 pF increase in loading, 100 pF maximum
[4] $\overline{RESET}$ must be active for a minimum of 3 clock cycles.

OUTPUT LOAD CIRCUIT

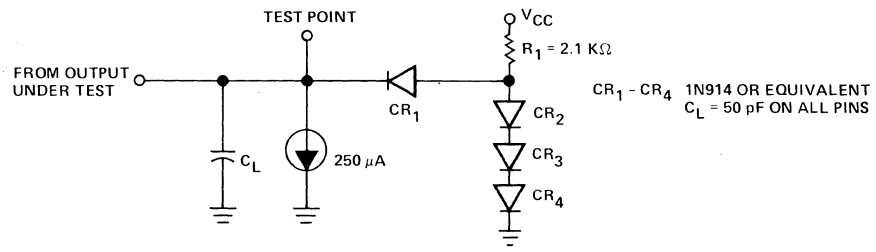


TA = 0° C to 70° C, Vcc = +5 V ± 5%, unless otherwise noted

Signal	Symbol	Parameter	Min	Max	Unit	Comments
Φ	t_C	Clock Period	250	[1]	ns	
	$t_W(\Phi H)$	Clock Pulse Width, Clock High	105	2000	ns	
	$t_W(\Phi L)$	Clock Pulse Width, Clock Low	105	2000	ns	
	t_r, t_f	Clock Rise and Fall Times		30	ns	
	t_H	Any Hold Time for Specified Setup Time	0		ns	
CS, $\overline{CE}$, etc	$t_{S\Phi}(CS)$	Control Signal Setup Time to Rising Edge of Φ During Read or Write Cycle	60		ns	
D_0–D_7	$t_{DR}(D)$	Data Output Delay from Falling Edge of $\overline{RD}$ During Read Cycle		380	ns	[2]
	$t_{S\Phi}(D)$	Data Setup Time to Rising Edge of Φ During Write or M1 Cycle	50		ns	
	$t_{DI}(D)$	Data Output Delay from Falling Edge of IORG During INTA Cycle		160	ns	[2]
	$t_F(D)$	Delay to Floating Bus (Output Buffer Disable Time)		110	ns	
IEI	$t_S(IEI)$	IEI Setup Time to Falling Edge of $\overline{IORQ}$ During INTA Cycle	140		ns	
IEO	$t_{DH}(IO)$	IEO Delay Time from Rising Edge of IEI		160	ns	[3]
	$t_{DL}(IO)$	IEO Delay Time from Falling Edge of IEI		130	ns	[3]
	$t_{DM}(IO)$	IEO Delay from Falling Edge of $\overline{M1}$ (Interrupt Occurring just Prior to $\overline{M1}$)		190	ns	[3]
$\overline{IORQ}$	$t_{S\Phi}(IR)$	$\overline{IORQ}$ Setup Time to Rising Edge of Φ During Read or Write Cycle	115		ns	
$\overline{M1}$	$t_{S\Phi}(M1)$	$\overline{M1}$ Setup Time to Rising Edge of Φ During INTA or M1 Cycle	90		ns	
$\overline{RD}$	$t_{S\Phi}(RD)$	$\overline{RD}$ Setup Time to Rising Edge of Φ During Read or M1 Cycle	115		ns	
$\overline{INT}$	$t_{DCK}(IT)$	$\overline{INT}$ Delay Time from Rising Edge of CLK/TRG		$2t_C(\Phi) + 140$		Counter Mode
	$t_{D\Phi}(IT)$	$\overline{INT}$ Delay Time from Rising Edge of Φ		$t_C(\Phi) + 140$		Timer Mode
CLK/TRG_{0-3}	$t_C(CK)$	Clock Period	$2t_C(\Phi)$			Counter Mode
	t_r, t_f	Clock and Trigger Rise and Fall Times		30		
	$t_S(CK)$	Clock Setup Time to Rising Edge of Φ for Immediate Count	130			Counter Mode
	$t_S(TR)$	Trigger Setup Time to Rising Edge of Φ for enabling of Prescaler on Following Rising Edge of Φ	130			Timer Mode
	$t_W(CTH)$	Clock and Trigger High Pulse Width	120			Counter and Timer Modes
	$t_W(CTL)$	Clock and Trigger Low Pulse Width	120			Counter and Timer Modes
ZC/TO_{0-2}	$t_{DH}(ZC)$	ZC/TO Delay Time from Rising Edge of Φ, ZC/TO High		120		Counter and Timer Modes
	$t_{DL}(ZC)$	ZC/TO Delay Time from Rising Edge of Φ, ZC/TO Low		120		Counter and Timer Modes

Notes: [1] $t_C = t_W(\Phi H) + t_W(\Phi L) + t_r + t_f$.
[2] Increase delay by 10 nsec for each 50 pF increase in loading, 200 pF maximum for data lines and 100 pF for control lines.
[3] Increase delay by 2 nsec for each 10 pF increase in loading, 100 pF maximum.
[4] $\overline{RESET}$ must be active for a minimum of 3 clock cycles.

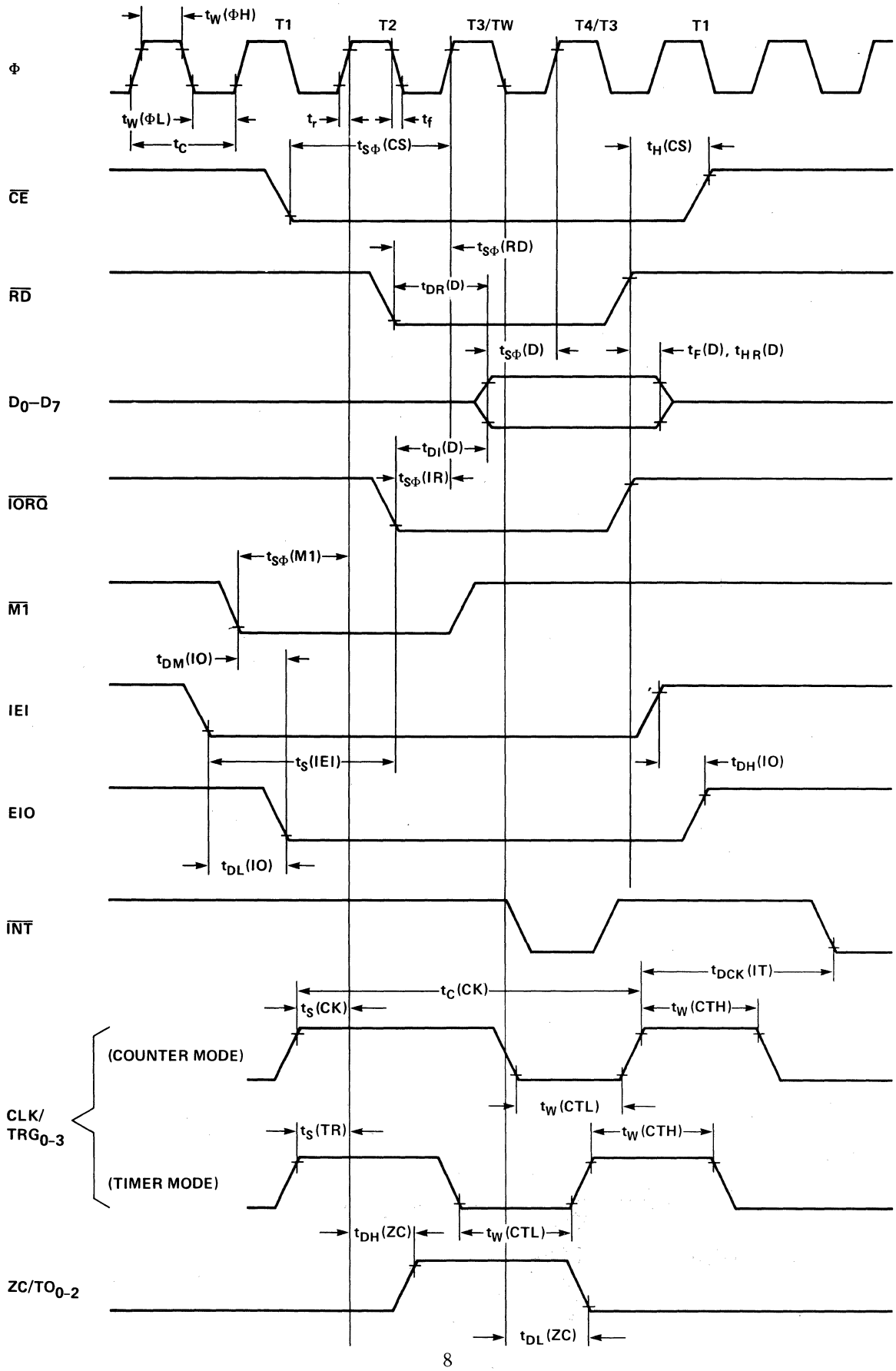
OUTPUT LOAD CIRCUIT



A.C. Timing Diagram

Timing measurements are made at the following voltages, unless otherwise specified:

	"1"	"0"
CLOCK	V_{CC} - .6V	.45V
OUTPUT	2.0V	.8V
INPUT	2.0V	.8V
FLOAT	ΔV	±0.5V



Absolute Maximum Ratings

Temperature Under Bias	0° C to 70° C
Storage Temperature	-65° C to +150° C
Voltage On Any Pin With Respect To Ground	-0.3 V to +7 V
Power Dissipation	0.8W

***Comment**

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

TA = 0° C to 70° C, Vcc = 5 V ± 5% unless otherwise specified

Z80-CTC

Symbol	Parameter	Min	Max	Unit	Test Condition
V_{ILC}	Clock Input Low Voltage	-0.3	.45	V	
V_{IHC}	Clock Input High Voltage [1]	V_{CC} - .6	V_{CC} + .3	V	
V_{IL}	Input Low Voltage	-0.3	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -250 μA
I_{CC}	Power Supply Current		120	mA	T_C = 400 nsec
I_{LI}	Input Leakage Current		10	μA	V_{IN} = 0 to V_{CC}
I_{LOH}	Tri-State Output Leakage Current in Float		10	μA	V_{OUT} = 2.4 to V_{CC}
I_{LOL}	Tri-State Output Leakage Current in Float		-10	μA	V_{OUT} = 0.4V
I_{OHD}	Darlington Drive Current	-1.5		mA	V_{OH} = 1.5V R_{EXT} = 390Ω

Z80A-CTC

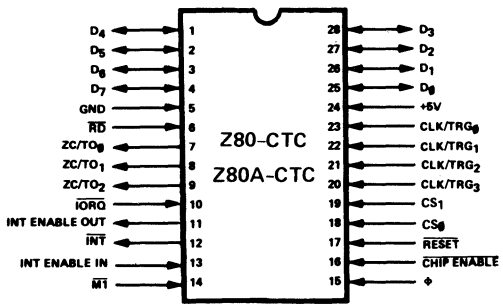
Symbol	Parameter	Min	Max	Unit	Test Condition
V_{ILC}	Clock Input Low Voltage	-0.3	.45	V	
V_{IHC}	Clock Input High Voltage [1]	V_{CC} - .6	V_{CC} + .3	V	
V_{IL}	Input Low Voltage	-0.3	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -250 μA
I_{CC}	Power Supply Current		120	mA	T_C = 250 nsec
I_{LI}	Input Leakage Current		10	μA	V_{IN} = 0 to V_{CC}
I_{LOH}	Tri-State Output Leakage Current in Float		10	μA	V_{OUT} = 2.4 to V_{CC}
I_{LOL}	Tri-State Output Leakage Current in Float		-10	μA	V_{OUT} = 0.4V
I_{OHD}	Darlington Drive Current	-1.5		mA	V_{OH} = 1.5V R_{EXT} = 390Ω

Capacitance

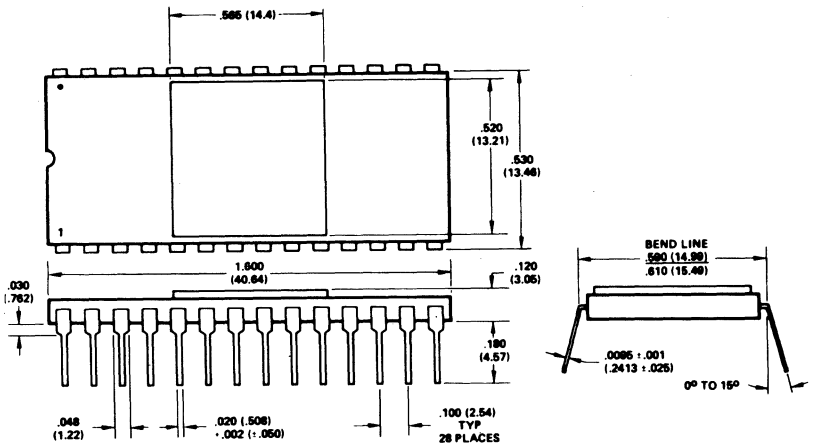
TA = 25° C, f = 1 MHz

Symbol	Parameter	Max.	Unit	Test Condition
C_Φ	Clock Capacitance	20	pF	Unmeasured Pins Returned to Ground
C_{IN}	Input Capacitance	5	pF	
C_{OUT}	Output Capacitance	10	pF	

Package Configuration



Package Outline



* DIMENSIONS FOR METRIC SYSTEM IN PARENTHESES (mm)

ZILOG SALES OFFICES

EASTERN REGION
Zilog, Inc.
400-1 Totten Pond Road
Waltham, MA 02154
TEL 617 890-0640
TWX 710 324 1974

MIDWESTERN REGION
Zilog, Inc.
1701 Woodfield Place
Suite 417
Schaumburg, IL 60195
TEL 312 885-8080
TWX 910 291 1064

WESTERN REGION
Zilog, Inc.
1815 Via el Prado
Redondo Beach, CA 90277
TEL 213 540-7749

ZILOG EUROPEAN HEADQUARTERS
Zilog (UK) Ltd.
Nicholson House
Maidenhead
Berks
England
TEL (0628) 36131/2/3
TWX 848-609

ZILOG U.S. DISTRIBUTORS

Western Region

Intermark Electronics
1802 E. Carnegie Avenue
Santa Ana, CA 92705
TEL 714 540 1322
TWX 910 595 1583

Intermark Electronics
4040 Sorrento Valley Blvd.
San Diego, CA 92121
TEL 714 279 5200
714 453 9005
TWX 910 335 1515

Intermark Electronics
1020 Stewart Drive
Sunnyvale, CA 94086
TEL 408 738 1111
TWX 910 339 9312

R.V. Weatherford Co.
6921 San Fernando Road
Glendale, CA 91201
TEL 213 849 3451
TWX 910 498 2223

R.V. Weatherford Co.
1550 Babbitt Avenue
Anaheim, CA 92805
TEL 714 634 9600
TWX 910 593 1334

R.V. Weatherford Co.
3240 Hillview Avenue
Stanford Industrial Park
Palo Alto, CA 94304
TEL 415 493 5373

Sterling Electronics
5608 6th Avenue South
Seattle, WA 98108
TEL 206 762 9100
TLX 32 9652

R.V. Weatherford Co.
1095 East Third Street
Pamona, CA 91766
TEL 714 623 1261
TWX 910 581 3811

R.V. Weatherford Co.
3311 W. Earll Drive
Phoenix, AZ 85017
TEL 602 272 7144
TWX 910 951 0636

Mountain

Century Electronics
121 Elizabeth, N.E.
Albuquerque, NM 87123
TEL 505 292 2700
TWX 910 989 0625

Century Electronics
2150 South 300 West
Salt Lake City, UT 84115
TEL 801 972 6969
TWX 910 925 5686

Century Electronics
8155 West 48th Avenue
Wheatridge, CO 80033
TEL 303 424 1985
TWX 910 938 0393

R.V. Weatherford Co.
3905 South Mariposa
Englewood, CO 80110
TEL 303 761 5432
TWX 910 933 0173

Eastern

Hallmark Electronics
4739 Commercial Drive
Huntsville, AL 35805
TEL 205 837 8700
TWX 810 726 2187

Hallmark Electronics
1302 West McNab Road
Fort Lauderdale, FL 33309
TEL 305 971 9280
TWX 510 956 9720

Hallmark Electronics
7233 Lake Ellenor Drive
Orlando, FL 32809
TEL 305 855 4020
TWX 810 850 0183

Hallmark Electronics
3355 Amberton Drive
Baltimore, MD 21227
TEL 301 796 9300
TWX 710 862 1942

Hallmark Electronics
1208 Front Street
Building K
Raleigh, NC 27609
TEL 919 832 4465
TWX 510 928 1831

Hallmark Electronics
Pike Industrial Park
Huntington Valley, PA
TEL 215 355 7300
TWX 510 667 1750

Summit
916 Main Street
Buffalo, NY 14202
TEL 716 884 3450

Midwestern

Hallmark Electronics
180 Grossen Avenue
Elk Grove Village, IL 60076
TEL 312 437 8800
TWX 910 223 3645

Hallmark Electronics
11870 West 91st Street
Congleton Industrial Park
Shawnee Mission, KS 66214
TEL 913 888 4747
TWX 910 749 6620

Hallmark Electronics
9201 Penn Avenue South
Suite 10
Bloomington, MN 55431
TEL 612 884 9056
TWX 910 576 3187

Hallmark Electronics
13789 Rider Trail
Earth City, MO 63045
TEL 314 291 5350
TWX 910 760 0671

Hallmark Electronics
6969 Worthington-Galena Road
Worthington, OH 43085
TEL 614 846 1882

Hallmark Electronics
4846 S. 83rd Road E. Avenue
Tulsa, OK 74145
TEL 918 835 8458
TWX 910 845 2290

Hallmark Electronics
3100-A Industrial Terrace
Austin, TX 78758
TEL 713 837 2814
TWX 910 874 2031

Hallmark Electronics
9333 Forest Lane
Dallas, TX 75231
TEL 214 231 5101
TWX 910 867 4721

Hallmark Electronics
8000 W. Glenn
Houston, TX 77063
TEL 713 781 6100
TWX 910 881 2711

Hallmark Electronics
237 South Curtis
West Allis, WI 53214
TEL 414 476 1270
TWX 910 262 3186

Zilog

03-0031-00

10460 Bubb Road, Cupertino, California 95014 ■ Telephone: (408) 446-4666 TWX: 910-338-7621

Printed in U.S.A.

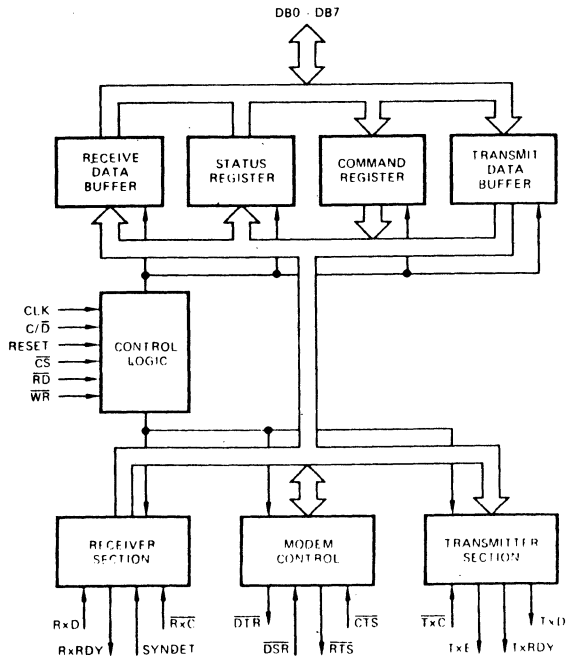
PURCHASE SPECIFICATIONS

PROGRAMMABLE COMMUNICATIONS

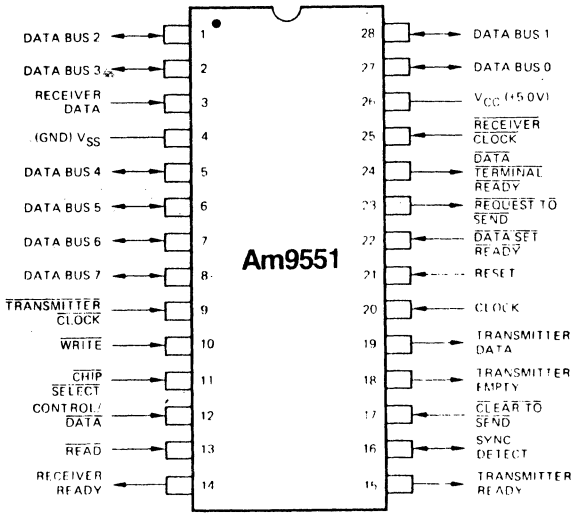
INTERFACE (USART)

REV.	ECO	DATE	REV.	ECO	DATE	ORIGINATED BY GAD Jr. 6/10/77	GENERAL TERMINAL CORPORATION SECOND AVENUE, BURLINGTON, MASS.	
						CHECKED KB 6/10/77	PURCHASE SPECIFICATIONS PROGRAMMABLE COMMUNICATIONS INTERFACE (USART)	
						APPROVED 6/10/77	A/SPEC 03203 SHT. 1 OF 15	REV.

BLOCK DIAGRAM



CONNECTION DIAGRAM
Top View



Pin 1 is marked for orientation.

REV.	ECO	DATE	REV.	ECO	DATE	ORIGINATED BY	GENERAL TERMINAL CORPORATION SECOND AVENUE, BURLINGTON, MASS.	
						CHECKED	PURCHASE SPECIFICATIONS PROGRAMMABLE COMMUNICATIONS INTERFACE (USART)	
						APPROVED	A/SPEC 03203 SHT. 2 OF 15	REV.

INTERFACE SIGNAL DESCRIPTION

Data Bus

The Am9551 uses an 8 bit bi-directional data bus to exchange information with an associated processor. Internally, data is routed between the data bus buffers and the transmitter section or receiver section as selected by the Read ($\overline{RD}$) or Write ($\overline{WR}$) control inputs.

Chip Select ($\overline{CS}$)

The active low Chip Select input allows the Am9551 to be individually selected from other devices within its address range. When Chip Select is high, reading or writing is inhibited, and the data bus output is in it's high impedance state.

Reset

The Am9551 will assume an idle state when a high level is applied to the Reset input. When the Reset is returned Low, the Am9551 will remain in the idle state until it receives a new mode control instruction.

Read ($\overline{RD}$)

The active low Read input enables data to be transferred from the Am9551 to the processor.

Write ($\overline{WR}$)

The active low Write input enables data to be transferred from the processor to the Am9551.

Control/Data (C/$\overline{D}$)

During a Read operation, if this input is at a high level the status byte will be read, and if it is at a low level the receive data will be read by the processor. When a Write operation is being performed, this input will indicate to the Am9551 that the bus information being written is a command if C/$\overline{D}$ is high and data if C/$\overline{D}$ is low.

C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	0	1	0	Am9551 DATA → DATA BUS
0	1	0	0	DATA BUS → Am9551 DATA
1	0	1	0	Am9551 STATUS → DATA BUS
1	1	0	0	DATA BUS → Am9551 COMMAND
X	X	X	1	DATA BUS → 3-STATE

Clock (CLK)

This input is used for internal timing within the Am9551. It does not control the transmit or receive rate. However, it should be at least 30 times the receive or transmit rate in the synchronous mode and 4.5 times the receive or transmit rate in the asynchronous mode. The CLK frequency is also restricted by both an upper and a lower bound. This input is often connected to a clock from the associated processor.

Receiver Data (RxD)

Serial data is received from the communication line on this input.

Receiver Clock ($\overline{RxC}$)

The serial data on input RxD is clocked into the Am9551 by the $\overline{RxC}$ clock signal. In the synchronous mode, $\overline{RxC}$ is determined by the baud rate and supplied by the modem. In the asynchronous mode, $\overline{RxC}$ is 1, 16, or 64 times the baud rate as selected in the mode control instruction. Data is sampled by the Am9551 on the rising edge of $\overline{RxC}$.

Receiver Ready (RxRDY)

The RxRDY output signal indicates to the processor that data has been shifted into the receiver buffer from the receiver section and may be read. The signal is active high and will be re-

set when the buffer is read by the processor. RxRDY can be activated only if the receiver enable (RxE) has been set in the command register, even though the receiver may be running. If the processor does not read the receiver buffer before the next character is shifted from the receiver section then an overrun error will be indicated in the status buffer.

Sync Detect (SYNDET)

This signal is used only in the synchronous mode. It can be either an output or input depending on whether the program is set for internal or external synchronization. As an output, a high level indicates when the sync character has been detected in the received data stream after the Internal Synchronization mode has been programmed. If the Am9551 is programmed to utilize two sync characters, then SYNDET will go to a high level when the last bit of the second sync character is received. SYNDET is reset when the status buffer is read or when a Reset signal is activated. SYNDET will perform as an input when the External Synchronization mode is programmed. External logic can supply a positive-going signal to indicate to the Am9551 that synchronization has been attained. This will cause it to initialize the assembly of characters on the next falling edge of $\overline{RxC}$. To successfully achieve synchronization the SYNDET signal should be maintained in a high condition for at least one full period of $\overline{RxC}$.

Transmit Data (TxD)

Serial data is transmitted to the communication line on this output.

Transmitter Clock ($\overline{TxC}$)

The serial data on TxD is clocked out with the $\overline{TxC}$ signal. The relationship between clock rate and baud rate is similar to that for $\overline{RxC}$. Data is shifted out of the Am9551 on the falling edge of $\overline{TxC}$.

Transmitter Ready (TxRDY)

The TxRDY output signal goes high when data in the Transmit Data Buffer has been shifted into the transmitter section allowing the Transmit Data Buffer to accept the next byte from the processor. TxRDY will be reset when information is written into the Transmit Data Buffer. Loading command register also resets TxRDY. TxRDY will be available on this output pin only when the Am9551 is enable to transmit (CTS = 0, TxEN = 1). However, the TxRDY bit in the status Buffer will always be set when the Transmit Data Buffer is empty regardless of the state of TxEN and $\overline{CTS}$.

Transmitter Empty (TxE)

The TxE output signal goes high when the Transmitter section has transmitted its data and is empty. The signal will remain high until a new data byte is shifted from the Transmit Data Buffer to the Transmitter section. In the synchronous mode if the processor does not load a new byte into the buffer in time, TxE will, independent of the status of the TxEN bit in the command register, momentarily go to a high level as SYNC characters are loaded into the Transmitter Section.

Data Terminal Ready ($\overline{DTR}$)

This signal is a general purpose output which reflects the state of bit 1 in the Command instruction. It is commonly connected to an associated modem to indicate that the Am9551 is ready.

Data Set Ready ($\overline{DSR}$)

This is a general purpose input signal and forms part of the status byte that may be read by the processor. $\overline{DSR}$ is generally used as a response to $\overline{DTR}$, by the Modem, to indicate that it is ready. The signal acts only as a flag and does not control any internal logic.

INTERFACE SIGNAL DESCRIPTION (Cont.)

Request to Send ($\overline{RTS}$)

This is a general purpose output, similar to $\overline{DTR}$, and reflects the state of bit 5 in Command Instruction. It is normally used to initiate a data transmission by requesting the modem to prepare to send.

Clear to Send ($\overline{CTS}$)

This is a general purpose input signal used to enable the 8251/9551 to transmit data if the TxEN bit in the Command byte is a one. $\overline{CTS}$ is generally used as a response to $\overline{RTS}$ by a modem to indicate that transmission may begin. Designers not using $\overline{CTS}$ in their systems should remember to tie it low so that 8251/9551 data transmission will not be disabled.

OPERATION AND PROGRAMMING

The microcomputer program controlling the Am9551 performs these tasks:

- Outputs control codes
- Inputs status
- Outputs data to be transmitted
- Inputs data which have been received

Control codes determine the mode in which the Am9551 will operate and are used to set or reset control signals output by the Am9551.

The Status register contents will be read by the program monitoring this device's operation in order to determine error conditions, when and how to read data, write data or output control codes. Program logic may be based on reading status bit levels, or control signals may be used to request interrupts.

INITIALIZING THE Am9551

The Am9551 may be initialized following a system reset or prior to starting a new serial I/O sequence. The USART must be reset following power up and subsequently may be reset at any time following completion of one activity and preceeding a new set of operations. Following a reset, the Am9551 enters an idle state in which it can neither transmit nor receive data.

The Am9551 is initialized with two, three or four control words from the processor. Figure 1 shows the sequence of control words needed to initialize the Am9551, for synchronous or for asynchronous operation. Note that in asynchronous operation a mode control is output to the device followed by a command. For synchronous operation, the mode control is followed by one or two SYNC characters, and then a command.

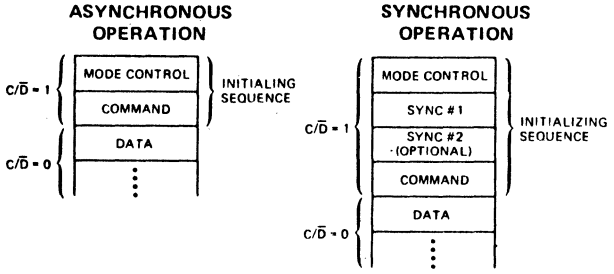


Figure 1. Control Word Sequence for Initialization.

Only a single address is set aside for mode control bytes, command bytes and SYNC character bytes. For this to be possible, logic internal to the chip directs control information to its proper destination based on the sequence in which it is received. Following a reset, the first control code output is interpreted as a mode control. If the mode control specifies synchronous operation, then the next one or two bytes (as determined by the mode byte) output as control codes will be interpreted as SYNC characters. For either asynchronous or synchronous operation, the next byte output as a control code is interpreted as a command. All subsequent bytes output as control codes are interpreted as commands. There are two ways in which control logic may return to anticipating a mode control input; following an external Reset signal or following an internal Reset command.

MODE CONTROL CODES

The Am9551 interprets mode control codes as illustrated in Figures 2 and 3.

Control code bits 0 and 1 determine whether synchronous or asynchronous operation is specified. A non-zero value in bits 0 and 1 specifies asynchronous operation and defines the relationship between data transfer baud rate and receiver or transmitter clock rate. Asynchronous serial data may be received or transmitted on every clock pulse, on every 16th clock pulse, or on every 64th clock pulse. A zero in both bits 0 and 1 defines the mode of operation as synchronous.

For synchronous and asynchronous modes, control bits 2 and 3 determine the number of data bits which will be present in each data character.

For synchronous and asynchronous modes, bits 4 and 5 determine whether there will be a parity bit in each character, and if so, whether odd or even parity will be adopted. Thus in synchronous mode a character will consist of five, six, seven or

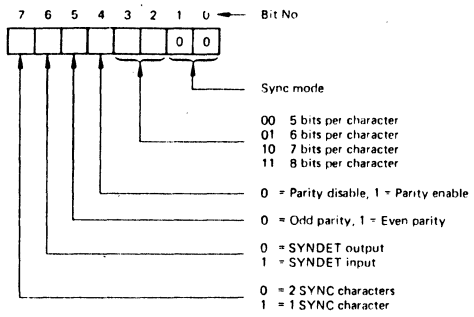


Figure 2. Synchronous Mode Control Code.

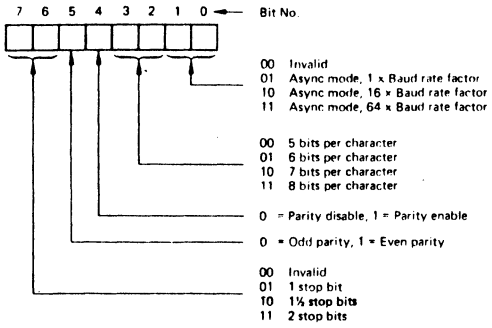


Figure 3. Asynchronous Mode Control Code.

OPERATION AND PROGRAMMING (Cont.)

eight data bits, plus an optional parity bit. In asynchronous mode, the data unit will consist of five, six, seven or eight data bits, an optional parity bit, a preceeding start bit, plus 1, 1½, or 2 trailing stop bits. Interpretation of subsequent bits differs for synchronous or asynchronous modes.

Control code bits 6 and 7 in asynchronous mode determine how many stop bits will trail each data unit. 1½ stop bits can only be specified with a 16x or 64x baud rate factor. In these two cases, the half stop bit will be equivalent to 8 or 32 clock pulses, respectively.

In synchronous mode, control bits 6 and 7 determine how character synchronization will be achieved. When SYNDET is an output, internal synchronization is specified; one or two SYNC characters, as specified by control bit 7, must be detected at the head of a data stream in order to establish synchronization.

COMMAND WORDS

Command words are used to initiate specific functions within the Am9551 such as, "reset all error flags" or "start searching for sync". Consequently, Command Words may be issued by the microprocessor to the Am9551 at any time during the execution of a program in which specific functions are to be initiated within the communication circuit.

Figure 4 shows the format for the Command Word.

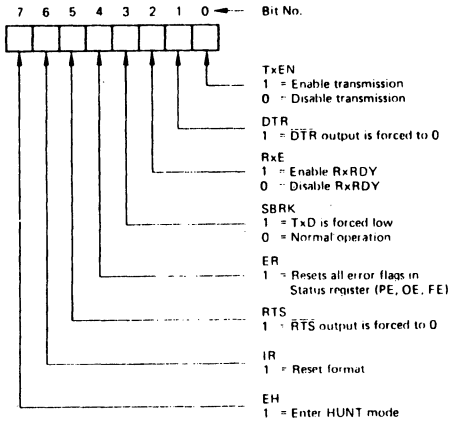


Figure 4. Am9551 Control Command.

Bit 0 of the Command Word is the Transmit Enable bit (TxEN). Data transmission from the Am9551 cannot take place unless TxEN is set in the command register. Figure 5 defines the way in which TxEN, TxE and TxRDY combine to control transmitter operations.

Bit 1 is the Data Terminal Ready (DTR) bit. When the DTR command bit is set, the DTR output connection is active (low). DTR is used to advise a modem that the data terminal is prepared to accept or transmit data.

Bit 2 is the Receiver Enable Command bit (RxE). RxE is used to enable the RxRDY output signal. RxE prevents the RxRDY signal from being generated to notify the processor that a complete character is framed in the Receive Character Buffer. It does not inhibit the assembly of data characters at the input, however. Consequently, if communication circuits are active,

characters will be assembled by the receiver and transferred to the Receiver Character Buffer. If RxE is disabled, the overrun error (OE) will probably be set; to insure proper operation, the overrun error is usually reset with the same command that enables RxE.

TxEN	TxE	TxRDY	
1	1	1	Transmit Output Regsiter and Transmit Character Buffer empty. TxD continues to mark if Am9551 is in the asynchronous mode. TxD will send Sync pattern if Am9551 is in the Synchronous Mode. Data can be entered into Buffer.
1	0	1	Transmit Output Register is shifting a character. Transmit Character Buffer is available to receive a new byte from the processor.
1	1	0	Transmit Register has finished sending. A new character is waiting for transmission. This is a transient condition.
1	0	0	Transmit Register is currently sending and an additional character is stored in the Transmit Character Buffer for transmission.
0	0/1	0/1	Transmitter is disabled.

Figure 5. Operation of the Transmitter Section as a Function of TxE, TxRDY and TxEN.

Bit 3 is the Send Break Command bit (SBRK). When SBRK is set, the transmitter output (TxD) is interrupted and a continuous binary "0" level, (spacing) is applied to the TxD output signal. The break will continue until a subsequent Command Word is sent to the Am9551 to remove SBRK.

Bit 4 is the Error Reset bit (ER). When a Command Word is transmitted with the ER bit set, all three error flags in the Status Register are reset. Error Reset occurs when the Command Word is loaded into the Am9551. No latch is provided in the Command Register to save the ER command bit.

Bit 5, the Request To Send Command bit (RTS), sets a latch to reflect the RTS signal level. The output of this latch is created independently of other signals in the Am9551. As a result, data transfers may be made by the microprocessor to the Transmit Register, and data may be actively transmitted to the communication line through TxD regardless of the status of RTS.

Bit 6, the Internal Reset (IR), causes the Am9551 to return to the Idle mode. All functions within the Am9551 cease and no new operation can be resumed until the circuit is reinitialized. If the operating mode is to be altered during the execution of a microprocessor program, the Am9551 must first be reset. Either the external reset connection can be activated, or the Internal Reset Command can be sent to the Am9551. Internal Reset is a momentary function performed only when the command is issued.

Bit 7 is the Enter Hunt command bit (EH). The Enter Hunt mode command is only effective for the Am9551 when it is operating in the Synchronous mode. EH causes the receiver to stop assembling characters at the RxD input and start searching for the prescribed sync pattern. Once the "Enter Hunt" mode has been initiated, the search for the sync pattern will

OPERATION AND PROGRAMMING (Cont.)

continue indefinitely until EH is reset when a subsequent Command Word is sent, when the IR command is sent to the Am9551, or when SYNC characters are recognized.

STATUS REGISTER

The Status Register maintains information about the current operational status of the Am9551. Figure 6 shows the format of the Status Register.

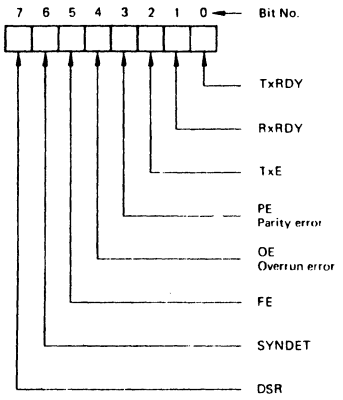


Figure 6. The Am9551 Status Register.

TxRDY signals the processor that the Transmit Character Buffer is empty and that the Am9551 can accept a new character for transmission.

RxRDY signals the processor that a completed character is holding in the Receive Character Buffer Register for transfer to the processor.

TxE signals the processor that the Transmit Register is empty.

PE is the Parity Error signal indicating to the CPU that the character stored in the Receive Character Buffer was received with an incorrect number of binary "1" bits.

OE is the receiver Overrun Error. OE is set whenever a byte stored in the Receiver Character Register is overwritten with a new byte before being transferred to the processor.

FE is the character framing error which indicates that the asynchronous mode byte stored in the Receiver Character Buffer was received with incorrect character bit format, as specified by the current mode.
SYNDET is the synchronous mode status bit associated with internal sync detection.

DSR is the status bit set by the external Data Set Ready signal to indicate that the communication Data Set is operational. All status bits are set by the functions described for them. SYNDET is reset whenever the processor reads the Status Register. OE, FE, PE are reset only by command.

MAXIMUM RATINGS Above which the useful life may be impaired

Storage Temperature	−65°C to +150°C
Ambient Temperature Under Bias	−55°C to +125°C
V_{CC} with Respect to V_{SS}	−0.5V to +7.0V
All Signal Voltages with Respect to V_{SS}	−0.5V to +7.0V
Power Dissipation	1.0W

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested, nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

ELECTRICAL CHARACTERISTICS Over Operating Range (Note 1)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
V_{OH}	Output HIGH Voltage	$I_{OH} = -200\mu A$	2.4			Volts
		$I_{OH} = -100\mu A$				
V_{OL}	Output LOW Voltage	$I_{OL} = 3.2mA$			0.4	Volts
		$I_{OL} = 1.6mA$				
V_{IH}	Input HIGH Voltage		2.0		V_{CC}	Volts
V_{IL}	Input LOW Voltage		-0.5		0.8	Volts
I_{LI}	Input Load Current	$V_{SS} \leq V_{IN} \leq V_{CC}$			10	μA
I_{DL}	Data Bus Leakage	$V_{OUT} = 0.45V$			-50	μA
		$V_{OUT} = V_{CC}$			10	
I_{CC}	V_{CC} Supply Current	$T_A = +25°C$		45		mA
		$T_A = 0°C$			80	
		$T_A = -55°C$			120	
C_O	Output Capacitance				15	pF
C_I	Input Capacitance				10	pF
$C_{I/O}$	I/O Capacitance	fc = 1.0MHz, Inputs = 0V			20	pF

SWITCHING CHARACTERISTICS OVER OPERATING RANGE (Note 2)

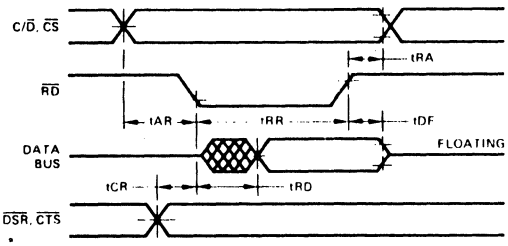
Parameters	Description		C8251 Min.	C8251 Max.	Am9551DM Am9551DC Min.	Am9551DM Am9551DC Max.	Am9551-4DC Min.	Am9551-4DC Max.	Units
t_{AR}	$\overline{CS}$, C/$\overline{D}$ Stable to $\overline{READ}$ Low Set-up Time		50		50		50		ns
t_{AW}	$\overline{CS}$, C/$\overline{D}$ Stable to $\overline{WRITE}$ Low Set-up Time		20		20		20		ns
t_{CR}	$\overline{DSR}$, $\overline{CTS}$ to $\overline{READ}$ Low Set-up Time			16		16		16	tCY
t_{CY}	Clock Period		420	1.35	380	1.35	380	1.35	µs
t_{DF}	$\overline{READ}$ High to Data Bus Off Delay		25	200	25	200	25	200	ns
t_{DTx}	TxC Low to TxD Delay			1.0		1.0		1.0	µs
t_{DW}	Data to $\overline{WRITE}$ High Set-up Time		200		150		100		ns
t_{ES}	External SYNDET to RxC Low Set-up Time			16		16		16	tCY
t_{HRx}	Sampling Pulse to Rx Data Hold Time		2.0		2.0		2.0		µs
t_{IS}	Data Bit (Center) to Internal SYNDET Delay			25		25		25	tCY
$t_{\phi W}$	Clock Pulse Width		220	0.7tCY	175	0.7tCY	175	0.7tCY	ns
t_R, t_F	Clock Rise & Fall Time		0	50	0	50	0	50	ns
t_{RA}	$\overline{READ}$ High to $\overline{CS}$, C/D Hold Time		5.0		5.0 ✓		5.0		ns
t_{RD}	$\overline{READ}$ Low to Data Bus On Delay			350		250		180	ns
t_{RPD}	Receiver Clock High Time	1x Baud Rate	15		15		15		tCY
		16x & 64x Baud Rate	3.0		3.0		3.0		
t_{RPW}	Receiver Clock Low Time	1x Baud Rate	12		12		12		tCY
		16x & 64x Baud Rate	1.0		1.0		1.0		
t_{RR}	$\overline{READ}$ Pulse Width		430		380		250		ns
t_{RV}	Time Between $\overline{WRITE}$ Pulses During Initialization (Note 3)		6.0		6.0		6.0		tCY
t_{Rx}	Data Bit (Center) to RxRDY Delay			20		20		20	tCY
t_{SRx}	Rx Data to Sampling Pulse Set-up Time		2.0		2.0		2.0		µs
t_{TPD}	Transmitter Clock High Time	1x Baud Rate	15		15		15		tCY
		16x & 64x Baud Rate	3.0		3.0		3.0		
t_{TPW}	Transmitter Clock Low Time	1x Baud Rate	12		12		12		tCY
		16x & 64x Baud Rate	1.0		1.0		1.0		
t_{Tx}	Data Bit (Center) to TxRDY Delay			16		16		16	tCY
t_{TxE}	Data Bit (Center) to Tx EMPTY Delay			16		16		16	tCY
t_{WA}	$\overline{WRITE}$ High to $\overline{CS}$, C/D Hold Time		20		20		20		ns
t_{WC}	$\overline{WRITE}$ High to TxE, $\overline{DTR}$, $\overline{RTS}$ Delay			16		16		16	tCY
t_{WD}	$\overline{WRITE}$ High to Data Hold Time		65		65		65		ns
t_{WW}	$\overline{WRITE}$ Pulse Width		400		380		250		ns
f_{Rx}	Receiver Clock Frequency	1x Baud Rate	DC	56	DC	56	DC	56	kHz
		16x & 64x Baud Rate	DC	520	DC	520	DC	520	
f_{Tx}	Transmitter Clock Frequency	1x Baud Rate	DC	56	DC	56	DC	56	kHz
		16x & 64x Baud Rate	DC	520	DC	520	DC	520	

NOTES:

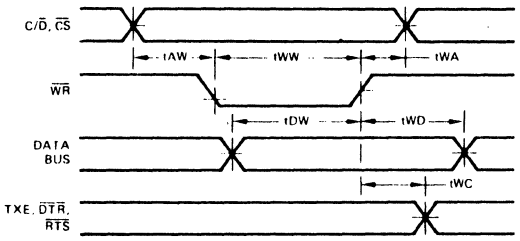
1. Typical values are for T_A = 25°C, nominal supply voltage and nominal processing parameters.
2. Test conditions include: transition times ≤ 20nS, output loading of 1TTL gate plus 100pF, input and output timing reference levels of 0.8V and 2.0V.
3. This time period between write pulses is specified for initialization purposes only; when MODE, SYNC 1, SYNC 2, COMMAND and first DATA BYTE are written into the Am9551. Subsequent writing of both COMMAND and DATA are only allowed when TxRDY = 1.
4. Reset Pulse Width = 6tCY min.
5. Switching Characteristic parameters are listed in alphabetical order.

SWITCHING WAVEFORMS

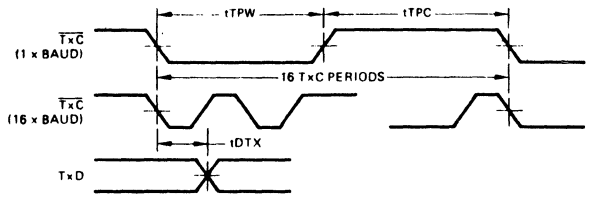
READ OPERATION



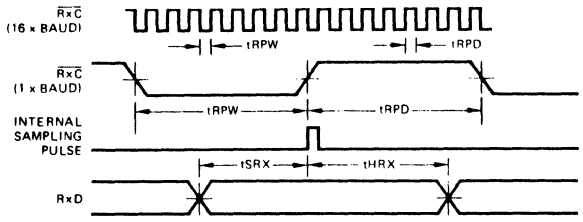
WRITE OPERATION



TRANSMITTER CLOCK AND DATA

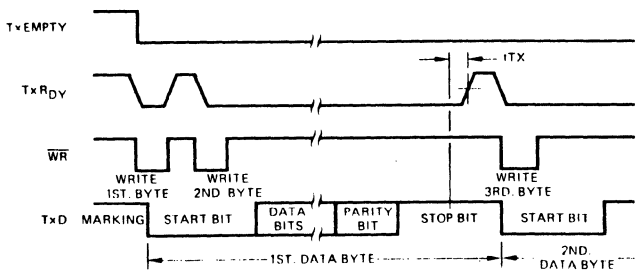


RECEIVER CLOCK AND DATA

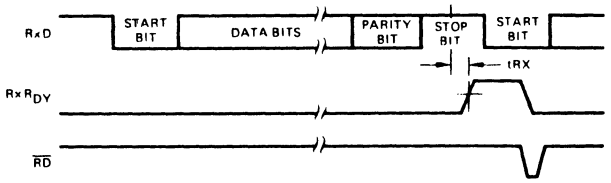


REV.	ECO	DATE	REV.	ECO	DATE	ORIGINATED BY	GENERAL TERMINAL CORPORATION SECOND AVENUE, BURLINGTON, MASS.	
						CHECKED	PURCHASE SPECIFICATION PROGRAMMABLE COMMUNICATION INTERFACE (USART)	
						APPROVED	A/SPEC 03203 SHT. 12 OF. 15	REV.

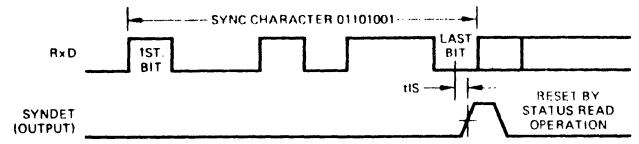
TxRDY TIMING (ASYNC MODE)



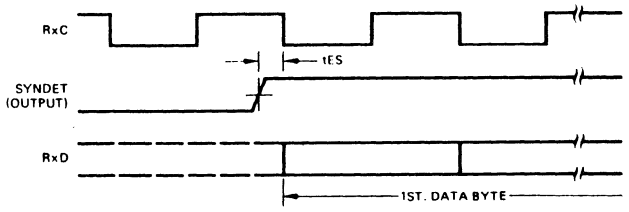
RxRDY TIMING (ASYNC MODE)



INTERNAL SYNC DETECT (SYNC MODE ONLY)

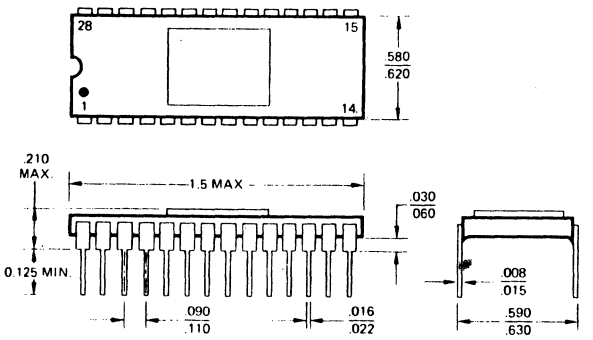


EXTERNAL SYNC DETECT (SYNC MODE ONLY)



REV.	ECO	DATE	REV.	ECO	DATE	ORIGINATED BY	GENERAL TERMINAL CORPORATION SECOND AVENUE, BURLINGTON, MASS.	
						CHECKED	PURCHASE SPECIFICATION PROGRAMMABLE COMMUNICATION INTERFACE (USART)	
						APPROVED	A/SPEC 03203 SHT. 13 OF. 15	REV.

PHYSICAL DIMENSIONS
28-Pin Hermetic DIP



REV.	ECO	DATE	REV.	ECO	DATE	ORIGINATED BY	GENERAL TERMINAL CORPORATION SECOND AVENUE, BURLINGTON, MASS.		
						CHECKED	PURCHASE SPECIFICATION PROGRAMMABLE COMMUNICATION INTERFACE (USART)		
						APPROVED	A/SPEC 03203	SHT. 14 OF. 15	REV.

APPROVED VENDORS

VENDOR	VENDOR PART NO.	INFOTON PART NO.
		03203
NEC	MPD8251C	
Intel	P8251	

REV.	ECO	DATE	REV.	ECO	DATE

ORIGINATED BY AD 5/10/77

CHECKED KB 6/16/77

APPROVED 6/10/77

GENERAL TERMINAL CORPORATION
SECOND AVENUE, BURLINGTON, MASS.

PURCHASE SPECIFICATION PROGRAMMABLE COMMUNICATION INTERFACE (USART)

A/SPEC | 03203 | SHT. 15 OF. 15 | REV.

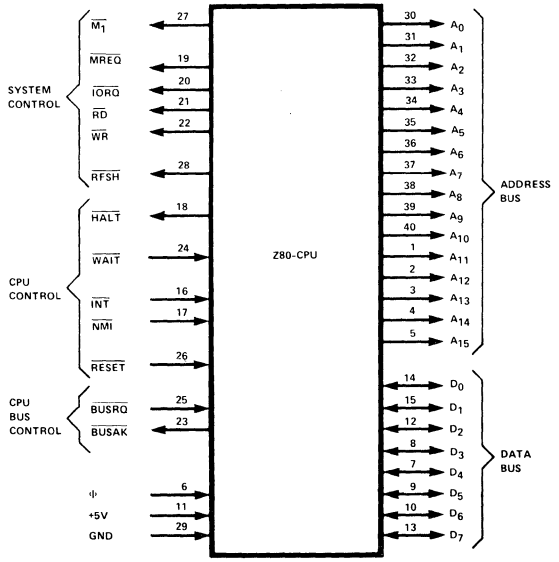
This page intentionally left blank.

ZILOG Z80-CPU
Programming Reference Card

MAIN REG SET		ALTERNATE REG SET		
ACCUMULATOR A	FLAGS F	ACCUMULATOR A′	FLAGS F′	
B	C	B′	C′	GENERAL PURPOSE REGISTERS
D	E	D′	E′	
H	L	H′	L′	

INTERRUPT VECTOR I	MEMORY REFRESH R	SPECIAL PURPOSE REGISTERS
INDEX REGISTER IX		
INDEX REGISTER IY		
STACK POINTER SP		
PROGRAM COUNTER PC		

Z80-CPU REGISTER CONFIGURATION



CPU PIN-OUTS

Z80 Peripheral Family

Z80-PIO **Z80-DMA**
Z80-CTC **Z80-SIO**

INSTRUCTION	C	Z	P/V	S	N	H	COMMENTS
ADD A, s; ADC A, s	↕	↕	V	↕	0	↕	8-bit add or add with carry
SUB s; SBC A, s, CP s, NEG	↕	↕	V	↕	1	↕	8-bit subtract, subtract with carry, compare and negate accumulator
AND s	0	↕	P	↕	0	1	Logical operations
OR s; XOR s	0	↕	P	↕	0	0	And sets different flags
INC s	•	↕	V	↕	0	↕	8-bit increment
DEC m	•	↕	V	↕	1	↕	8-bit decrement
ADD DD, ss	↕	•	•	•	0	X	16-bit add
ADC HL, ss	↕	↕	V	↕	0	X	16-bit add with carry
SBC HL, ss	↕	↕	V	↕	1	X	16-bit subtract with carry
RLA; RLCA, RRA, RRCA	↕	•	•	•	0	0	Rotate accumulator
RL m; RLC m; RR m; RRC m SLA m; SRA m; SRL m	↕	↕	P	↕	0	0	Rotate and shift location s
RLD, RRD	•	↕	P	↕	0	0	Rotate digit left and right
DAA	↕	↕	P	↕	•	↕	Decimal adjust accumulator
CPL	•	•	•	•	1	1	Complement accumulator
SCF	1	•	•	•	0	0	Set carry
CCF	↕	•	•	•	0	X	Complement carry
IN r, (C)	•	↕	P	↕	0	0	Input register indirect
INI; IND; OUTI; OUTD	•	↕	X	X	1	X	Block input and output
INIR; INDR; OTIR; OTDR	•	1	X	X	1	X	Z = 0 if B ≠ 0 otherwise Z = 1
LDI, LDD	•	X	↕	X	0	0	Block transfer instructions
LDIR, LDDR	•	X	0	X	0	0	P/V = 1 if BC ≠ 0, otherwise P/V = 0
CPI, CPIR, CPD, CPDR	•	↕	↕	X	1	X	Block search instructions Z = 1 if A = (HL), otherwise Z = 0 P/V = 1 if BC ≠ 0, otherwise P/V = 0
LD A, I; LD A, R	•	↕	IFF	↕	0	0	The content of the interrupt enable flip-flop (IFF) is copied into the P/V flag
BIT b, s	•	↕	X	X	0	1	The complement of bit b of location is copied into the Z flag
NEG	↕	↕	V	↕	1	↕	Negate accumulator

The following notation is used in this table:

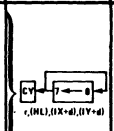
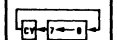
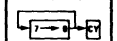
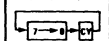
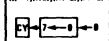
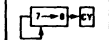
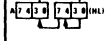
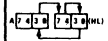
SYMBOL	OPERATION
C	Carry/link flag. C=1 if the operation produced a carry from the MSB of the operand or result.
Z	Zero flag. Z=1 if the result of the operation is zero.
S	Sign flag. S=1 if the MSB of the result is one.
P/V	Parity or overflow flag. Parity (P) and overflow (V) share the same flag. Logical operations affect this flag with the parity of the result while arithmetic operations affect this flag with the overflow of the result. If P/V holds parity, P/V=1 if the result of the operation is even, P/V=0 if result is odd. If P/V holds overflow, P/V=1 if the result of the operation produced an overflow.
H	Half-carry flag. H=1 if the add or subtract operation produced a carry into or borrow from bit 4 of the accumulator.
N	Add/Subtract flag. N=1 if the previous operation was a subtract.
	H and N flags are used in conjunction with the decimal adjust instruction (DAA) to properly correct the result into packed BCD format following addition or subtraction using operands with packed BCD format.
↕	The flag is affected according to the result of the operation.
•	The flag is unchanged by the operation.
0	The flag is reset by the operation.
1	The flag is set by the operation.
X	The flag is a "don't care."
V	P/V flag affected according to the overflow result of the operation.
P	P/V flag affected according to the parity result of the operation.
r	Any one of the CPU registers A, B, C, D, E, H, L.
s	Any 8-bit location for all the addressing modes allowed for the particular instruction.
ss	Any 16-bit location for all the addressing modes allowed for that instruction.
ii	Any one of the two index registers IX or IY.
R	Refresh counter.
n	8-bit value in range <0, 255>.
nn	16-bit value in range <0, 65535>.
m	Any 8-bit location for all the addressing modes allowed for the particular instruction.

SUMMARY OF FLAG OPERATION

MNEMONIC	SYMBOLIC OPERATION	FLAGS C	P/V	S	N	H	OP-CODE 76 543 210	NO. OF T CYCLES	COMMENTS
LD r, r′	r ← r′	•	•	•	•	•	01 r r	4	r, r′ Reg.
LD r, n	r ← n	•	•	•	•	•	00 r 110	7	000 B
							← n →		001 C
LD r, (HL)	r ← (HL)	•	•	•	•	•	01 r 110	7	010 D
LD r, (IX+d)	r ← (IX+d)	•	•	•	•	•	11 011 101	19	011 E
							01 r 110		100 H
							← d →		101 L
LD r, (IY+d)	r ← (IY+d)	•	•	•	•	•	11 111 101	19	111 A
							01 r 110		
							← d →		
LD (HL), r	(HL) ← r	•	•	•	•	•	01 110 r	7	
LD (IX+d), r	(IX+d) ← r	•	•	•	•	•	11 011 101	19	
							01 110 r		
							← d →		
LD (IY+d), r	(IY+d) ← r	•	•	•	•	•	11 111 101	19	
							01 110 r		
							← d →		
LD (HL), n	(HL) ← n	•	•	•	•	•	00 110 110	10	
							← n →		
LD (IX+d), n	(IX+d) ← n	•	•	•	•	•	11 011 101	19	
							00 110 110		
							← d →		
							← n →		
LD (IY+d), n	(IY+d) ← n	•	•	•	•	•	11 111 101	19	
							00 110 110		
							← d →		
							← n →		
LD A, (BC)	A ← (BC)	•	•	•	•	•	00 001 010	7	
LD A, (DE)	A ← (DE)	•	•	•	•	•	00 011 010	7	
LD A, (nn)	A ← (nn)	•	•	•	•	•	00 111 010	13	
							← n →		
							← n →		
LD (BC), A	(BC) ← A	•	•	•	•	•	00 000 010	7	
LD (DE), A	(DE) ← A	•	•	•	•	•	00 010 010	7	
LD (nn), A	(nn) ← A	•	•	•	•	•	00 110 010	13	
							← n →		
							← n →		
LD A, I	A ← I	•	↕	IFF	↕	0	0	11 101 101	9
							01 010 111		
LD A, R	A ← R	•	↕	IFF	↕	0	0	11 101 101	9
							01 011 111		
LD I, A	I ← A	•	•	•	•	•	11 101 101	9	
							01 000 111		
LD R, A	R ← A	•	•	•	•	•	11 101 101	9	
							01 001 111		
LD dd, nn	dd ← nn	•	•	•	•	•	00 dd0 001	10	dd Pair
							← n →		00 BC
							← n →		01 DE
LD IX, nn	IX ← nn	•	•	•	•	•	11 011 101	14	10 HL
							00 100 001		11 SP
							← n →		
							← n →		
LD IY, nn	IY ← nn	•	•	•	•	•	11 111 101	14	
							00 100 001		
							← n →		
							← n →		
LD HL, (nn)	H ← (nn+1) L ← (nn)	•	•	•	•	•	00 101 010	16	
							← n →		
							← n →		
LD dd, (nn)	dd_H ← (nn+1) dd_L ← (nn)	•	•	•	•	•	11 101 101	20	
							01 dd1 011		
							← n →		
							← n →		
LD IX, (nn)	IX_H ← (nn+1) IX_L ← (nn)	•	•	•	•	•	11 011 101	20	
							00 101 010		
							← n →		
							← n →		
LD IY, (nn)	IY_H ← (nn+1) IY_L ← (nn)	•	•	•	•	•	11 111 101	20	
							00 101 010		
							← n →		
							← n →		
LD (nn), HL	(nn+1) ← H (nn) ← L	•	•	•	•	•	00 100 010	16	
							← n →		
							← n →		

MNEMONIC	SYMBOLIC OPERATION	FLAGS C	Z	P/V	S	N	H	OP-CODE 76 543 210	NO. OF T CYCLES	COMMENTS
LD (nn), dd	(nn+1) ← dd_H (nn) ← dd_L	•	•	•	•	•	•	11 101 101 01 dd0 011 ← n → ← n →	20	
LD (nn), IX	(nn+1) ← IX_H (nn) ← IX_L	•	•	•	•	•	•	11 011 101 00 100 010 ← n → ← n →	20	
LD (nn), IY	(nn+1) ← IY_H (nn) ← IY_L	•	•	•	•	•	•	11 111 101 00 100 010 ← n → ← n →	20	
LD SP, HL	SP ← HL	•	•	•	•	•	•	11 111 001	6	
LD SP, IX	SP ← IX	•	•	•	•	•	•	11 011 101 11 111 001	10	
LD SP, IY	SP ← IY	•	•	•	•	•	•	11 111 101 11 111 001	10	
PUSH qq	(SP-2) ← qq_L (SP-1) ← qq_H	•	•	•	•	•	•	11 qq0 101	11	qq | Pair 00 | BC 01 | DE 10 | HL 11 | AF
PUSH IX	(SP-2) ← IX_L (SP-1) ← IX_H	•	•	•	•	•	•	11 011 101 11 100 101	15	
PUSH IY	(SP-2) ← IY_L (SP-1) ← IY_H	•	•	•	•	•	•	11 111 101 11 100 101	15	
POP qq	qq_H ← (SP+1) qq_L ← (SP)	•	•	•	•	•	•	11 qq0 001	10	
POP IX	IX_H ← (SP+1) IX_L ← (SP)	•	•	•	•	•	•	11 011 101 11 100 001	14	
POP IY	IY_H ← (SP+1) IY_L ← (SP)	•	•	•	•	•	•	11 111 101 11 100 001	14	
EX DE, HL	DE ↔ HL	•	•	•	•	•	•	11 101 011	4	
EX AF, AF′	AF ↔ AF′	•	•	•	•	•	•	00 001 000	4	
EXX	BC ↔ BC′ DE ↔ DE′ HL ↔ HL′	•	•	•	•	•	•	11 011 001	4	Register bank and auxiliary register bank exchange
EX (SP), HL	H ↔ (SP+1) L ↔ (SP)	•	•	•	•	•	•	11 100 011	19	
EX (SP), IX	IX_H ↔ (SP+1) IX_L ↔ (SP)	•	•	•	•	•	•	11 011 101 11 100 011	23	
EX (SP), IY	IY_H ↔ (SP+1) IY_L ↔ (SP)	•	•	•	•	•	•	11 111 101 11 100 011	23	
LDI	(DE) ← (HL) DE ← DE+1 HL ← HL+1 BC ← BC-1	•	•	① ↕	•	0	0	11 101 101 10 100 000	16	Load (HL) into (DE), increment the pointers and decrement the byte counter (BC)
LDIR	(DE) ← (HL) DE ← DE+1 HL ← HL+1 BC ← BC-1 Repeat until BC = 0	•	•	0	•	0	0	11 101 101 10 110 000	21 16	If BC ≠ 0 If BC = 0
LDD	(DE) ← (HL) DE ← DE-1 HL ← HL-1 BC ← BC-1	•	•	① ↕	•	0	0	11 101 101 10 101 000	16	
LDDR	(DE) ← (HL) DE ← DE-1 HL ← HL-1 BC ← BC-1 Repeat until BC = 0	•	•	0	•	0	0	11 101 101 10 111 000	21 16	If BC ≠ 0 If BC = 0
CPI	A - (HL) HL ← HL+1 BC ← BC-1	•	↕	② ↕	↕	1	↕	11 101 101 10 100 001	16	
CPIR	A - (HL) HL ← HL+1 BC ← BC-1 Repeat until A = (HL) or BC = 0	•	↕	② ↕	↕	1	↕	11 101 101 10 110 001	21 16	If BC ≠ 0 and A ≠ (HL) If BC = 0 or A = (HL)
CPD	A - (HL) HL ← HL-1 BC ← BC-1	•	↕	② ↕	↕	1	↕	11 101 101 10 101 001	16	

MNEMONIC	SYMBOLIC OPERATION	FLAGS C	Z	P/V	S	N	H	OP-CODE 76 543 210	NO. OF T CYCLES	COMMENTS
CPDR	A - (HL) HL ← HL-1 BC ← BC-1 Repeat until A = (HL) or BC = 0	•	② ↕	① ↕	↕	1	↕	11 101 101 10 111 001	21 16	If BC ≠ 0 and A ≠ (HL) If BC = 0 or A = (HL)
ADD A, r	A ← A + r	↕	↕	V	↕	0	↕	10 000 r	4	r | Reg. 000 | B 001 | C 010 | D 011 | E 100 | H 101 | L 111 | A
ADD A, n	A ← A + n	↕	↕	V	↕	0	↕	11 000 110 ← n →	7	
ADD A, (HL)	A ← A + (HL)	↕	↕	V	↕	0	↕	10 000 110	7	
ADD A, (IX+d)	A ← A + (IX+d)	↕	↕	V	↕	0	↕	11 011 101 10 000 110 ← d →	19	
ADD A, (IY+d)	A ← A+(IY+d)	↕	↕	V	↕	0	↕	11 111 101 10 000 110 ← d →	19	
ADC A,s SUB s SBC A,s AND s OR s XOR s CP s	A ← A + s + CY A ← A - s A ← A - s - CY A ← A ∧ s A ← A ∨ s A ← A s A - s	↕	↕	V	↕	0	↕	001 010 011 100 110 101 111		s is any of r, n, (HL), (IX+d), (IY+d) as shown for ADD instruction The indicated bits replace the 000 in the ADD set above.
INC r	r ← r + 1	•	↕	V	↕	0	↕	00 r 100	4	
INC (HL)	(HL) ← (HL)+1	•	↕	V	↕	0	↕	00 110 100	11	
INC (IX+d)	(IX+d) ← (IX+d)+1	•	↕	V	↕	0	↕	11 011 101 00 110 100 ← d →	23	
INC (IY+d)	(IY+d)← (IY+d)+1	•	↕	V	↕	0	↕	11 111 101 00 110 100 ← d →	23	
DEC m	m ← m-1	•	↕	V	↕	1	↕	101		m is any of r, (HL), m (IX+d), (IY+d) as shown for INC. Same format and states as INC. Replace 100 with 101 in OP code.
ADD HL, ss	HL ← HL+ss	↕	•	•	•	0	X	00 ss1 001	11	ss | Reg. 00 | BC 01 | DE 10 | HL 11 | SP
ADC HL, ss	HL←HL+ss+CY	↕	↕	V	↕	0	X	11 101 101 01 ss1 010	15	
SBC HL, ss	HL←HL-ss-CY	↕	↕	V	↕	1	X	11 101 101 01 ss0 010	15	
ADD IX, pp	IX ← IX + pp	↕	•	•	•	0	X	11 011 101 00 pp1 001	15	pp | Reg. 00 | BC 01 | DE 10 | IX 11 | SP
ADD IY, rr	IY← IY+rr	↕	•	•	•	0	X	11 111 101 00 rr1 001	15	rr | Reg. 00 | BC 01 | DE 10 | IY 11 | SP
INC ss	ss ← ss + 1	•	•	•	•	•	•	00 ss0 011	6	
INC IX	IX ← IX + 1	•	•	•	•	•	•	11 011 101 00 100 011	10	
INC IY	IY ← IY + 1	•	•	•	•	•	•	11 111 101 00 100 011	10	
DEC ss	ss ← ss -1	•	•	•	•	•	•	00 ss1 011	6	
DEC IX	IX ← IX -1	•	•	•	•	•	•	11 011 101 00 101 011	10	
DEC IY	IY ← IY -1	•	•	•	•	•	•	11 111 101 00 101 011	10	
RLCA		↕	•	•	•	0	0	00 000 111	4	Rotate left circular accumulator
RLA		↕	•	•	•	0	0	00 010 111	4	Rotate left accumulator
RRCA		↕	•	•	•	0	0	00 001 111	4	Rotate right circular accumulator
RRA		↕	•	•	•	0	0	00 011 111	4	Rotate right accumulator

MNEMONIC	SYMBOLIC OPERATION	FLAGS C	Z	P/V	S	N	H	OP-CODE 76 543 210	NO. OF T CYCLES	COMMENTS
RLC r		↕	↕	P	↕	0	0	11 001 011 00 000 r	8	Rotate left circular register r r | Reg. 000 | B 001 | C 010 | D 011 | E 100 | H 101 | L 111 | A
RLC (HL)		↕	↕	P	↕	0	0	11 001 011 00 000 110	15	
RLC (IX+d)		↕	↕	P	↕	0	0	11 011 101 11 001 011 ← d → 00 000 110	23	
RLC (IY+d)		↕	↕	P	↕	0	0	11 111 101 11 001 011 ← d → 00 000 110	23	
RL m		↕	↕	P	↕	0	0	010		Instruction format and states are as shown for RLC,s. To form new OP-code replace 000 of RLC,s with shown code
RRC m		↕	↕	P	↕	0	0	001		
RR m		↕	↕	P	↕	0	0	011		
SLA m		↕	↕	P	↕	0	0	100		
SRA m		↕	↕	P	↕	0	0	101		
SRL m		↕	↕	P	↕	0	0	111		
RLD		•	↕	P	↕	0	0	11 101 101 01 101 111	18	Rotate digit left and right between the accumulator and location (HL). The content of the upper half of the accumulator is unaffected.
RRD		•	↕	P	↕	0	0	11 101 101 01 100 111	18	
DAA	Converts acc. content into packed BCD following add or subtract with packed BCD operands	↕	↕	P	↕	•	↕	00 100 111	4	Decimal adjust accumulator.
CPL	A ← $\overline{A}$	•	•	•	•	1	1	00 101 111	4	Complement accumulator (one's complement)
NEG	A ← o-A	↕	↕	V	↕	1	↕	11 101 101 01 000 100	8	Negate acc. (two's complement)
CCF	CY ← $\overline{CY}$	↕	•	•	•	0	X	00 111 111	4	Complement carry flag
SCF	CY ← 1	1	•	•	•	0	0	00 110 111	4	Set carry flag
NOP	No operation	•	•	•	•	•	•	00 000 000	4	
HALT	CPU halted	•	•	•	•	•	•	01 110 110	4	
DI	IFF ← 0	•	•	•	•	•	•	11 110 011	4	
EI	IFF ← 1	•	•	•	•	•	•	11 111 011	4	
IM 0	Set interrupt mode 0	•	•	•	•	•	•	11 101 101 01 000 110	8	
IM 1	Set interrupt mode 1	•	•	•	•	•	•	11 101 101 01 010 110	8	
IM 2	Set interrupt mode 2	•	•	•	•	•	•	11 101 101 01 011 110	8	
BIT b, r	Z ← $\overline{r_b}$	•	↕	X	X	0	1	11 001 011 01 b r	8	r | Reg. 000 | B 001 | C 010 | D 011 | E 100 | H 101 | L 111 | A
BIT b, (HL)	Z ← $\overline{(HL)_b}$	•	↕	X	X	0	1	11 001 011 01 b 110	12	
BIT b, (IX+d)	Z ← $\overline{(IX+d)_b}$	•	↕	X	X	0	1	11 011 101 11 001 011 ← d → 01 b 110	20	
BIT b, (IY+d)	Z ← $\overline{(IY+d)_b}$	•	↕	X	X	0	1	11 111 101 11 001 011 ← d → 01 b 110	20	b | Bit Tested 000 | 0 001 | 1 010 | 2 011 | 3 100 | 4 101 | 5 110 | 6 111 | 7

MNEMONIC	SYMBOLIC OPERATION	FLAGS C	Z	P/V	S	N	H	OP-CODE 76 543 210	NO. OF T CYCLES	COMMENTS
SET b, r	$r_b \leftarrow 1$	•	•	•	•	•	•	11 001 011 11 b r	8	
SET b, (HL)	$(HL)_b \leftarrow 1$	•	•	•	•	•	•	11 001 011 11 b 110	15	
SET b, (IX+d)	$(IX+d)_b \leftarrow 1$	•	•	•	•	•	•	11 011 101 11 001 011 ← d → 11 b 110	23	
SET b, (IY+d)	$(IY+d)_b \leftarrow 1$	•	•	•	•	•	•	11 111 101 11 001 011 ← d → 11 b 110	23	
RES b, m	$s_b \leftarrow 0$ m ≡ r, (HL), (IX+d), (IY+d)							10	•	To form new OP-code replace 11 of SET b, s with 10 . Flags and time states for SET instruction
JP nn	PC ← nn	•	•	•	•	•	•	11 000 011 ← n → ← n →	10	
JP cc, nn	If condition is true PC ← nn, otherwise continue	•	•	•	•	•	•	11 cc 010 ← n → ← n →	10	cc | Condition 000 | NZ non zero 001 | Z zero 010 | NC non carry 011 | C carry 100 | PO parity odd 101 | PE parity even 110 | P sign positive 111 | M sign negative
JR e	PC ← PC + e	•	•	•	•	•	•	00 011 000 ← e-2 →	12	
JR C, e	If C = 0, continue	•	•	•	•	•	•	00 111 000 ← e-2 →	7	If condition not met
	If C = 1, PC ← PC + e								12	If condition is met
JR NC , e	If C = 1, continue	•	•	•	•	•	•	00 110 000 ← e-2 →	7	If condition not met
	If C = 0, PC ← PC + e								12	If condition is met
JR Z, e	If Z = 0 continue	•	•	•	•	•	•	00 101 000 ← e-2 →	7	If condition not met
	If Z = 1, PC ← PC + e								12	If condition is met
JR NZ, e	If Z = 1, continue	•	•	•	•	•	•	00 100 000 ← e-2 →	7	If condition not met
	If Z = 0, PC ← PC + e								12	If condition met
JP (HL)	PC ← HL	•	•	•	•	•	•	11 101 001	4	
JP (IX)	PC ← IX	•	•	•	•	•	•	11 011 101 11 101 001	8	
JP (IY)	PC ← IY	•	•	•	•	•	•	11 111 101 11 101 001	8	
DJNZ e	B ← B-1 If B = 0, continue	•	•	•	•	•	•	00 010 000 ← e-2 →	8	If B = 0
	If B ≠ 0, PC ← PC + e								13	If B ≠ 0
CALL nn	(SP-1) ← PC_H (SP-2) ← PC_L PC ← nn	•	•	•	•	•	•	11 001 101 ← n → ← n →	17	
CALL cc, nn	If condition cc is false continue, otherwise same as CALL nn	•	•	•	•	•	•	11 cc 100 ← n → ← n →	10	If cc is false
									17	If cc is true
RET	$PC_L \leftarrow$ (SP) $PC_H \leftarrow$ (SP+1)	•	•	•	•	•	•	11 001 001	10	
RET cc	If condition cc is false continue, otherwise same as RET	•	•	•	•	•	•	11 cc 000	5	If cc is false
									11	If cc is true cc | Condition 000 | NZ non zero 001 | Z zero 010 | NC non carry 011 | C carry 100 | PO parity odd 101 | PE parity even 110 | P sign positive 111 | M sign negative
RETI	Return from interrupt	•	•	•	•	•	•	11 101 101 01 001 101	14	
RETN	Return from non maskable interrupt	•	•	•	•	•	•	11 101 101 01 000 101	14	

MNEMONIC	SYMBOLIC OPERATION	FLAGS C	Z	P/V	S	N	H	OP-CODE 76 543 210	NO. OF T CYCLES	COMMENTS
RST p	(SP-1) ← PC_H (SP-2) ← PC_L $PC_H \leftarrow 0$ $PC_L \leftarrow$ P	•	•	•	•	•	•	11 t 111	11	
IN A, (n)	A ← (n)	•	•	•	•	•	•	11 011 011 ← n →	11	n to $A_0 \sim A_7$ Acc to $A_8 \sim A_{15}$
IN r, (C)	r ← (C) If r = 110 only the flags will be affected	•	‡	P	‡	0	‡	11 101 101 01 r 000	12	C to $A_0 \sim A_7$ B to $A_8 \sim A_{15}$
INI	(HL) ← (C) B ← B-1 HL ← HL + 1	•	‡ ③	X	X	1	X	11 101 101 10 100 010	16	C to $A_0 \sim A_7$ B to $A_8 \sim A_{15}$
INIR	(HL) ← (C) B ← B-1 HL ← HL + 1 Repeat until B = 0	•	1 ③	X	X	1	X	11 101 101 10 110 010	21 16	C to $A_0 \sim A_7$ B to $A_8 \sim A_{15}$
IND	(HL) ← (C) B ← B-1 HL ← HL-1	•	‡ ③	X	X	1	X	11 101 101 10 101 010	16	C to $A_0 \sim A_7$ B to $A_8 \sim A_{15}$
INDR	(HL) ← (C) B ← B-1 HL ← HL-1 Repeat until B = 0	•	1	X	X	1	X	11 101 101 10 111 010	21 16	C to $A_0 \sim A_7$ B to $A_8 \sim A_{15}$
OUT (n), A	(n) ← A	•	•	•	•	•	•	11 010 011 ← n →	11	n to $A_0 \sim A_7$ Acc to $A_8 \sim A_{15}$
OUT (C), r	(C) ← r	•	•	•	•	•	•	11 101 101 01 r 001	12	C to $A_0 \sim A_7$ B to $A_8 \sim A_{15}$
OUTI	(C) ← (HL) B ← B-1 HL ← HL + 1	•	‡ ③	X	X	1	X	11 101 101 10 100 011	16	C to $A_0 \sim A_7$ B to $A_8 \sim A_{15}$
OTIR	(C) ← (HL) B ← B-1 HL ← HL + 1 Repeat until B = 0	•	1 ③	X	X	1	X	11 101 101 10 110 011	21 16	C to $A_0 \sim A_7$ B to $A_8 \sim A_{15}$
OUTD	(C) ← (HL) B ← B-1 HL ← HL-1	•	‡ ③	X	X	1	X	11 101 101 10 101 011	16	C to $A_0 \sim A_7$ B to $A_8 \sim A_{15}$
OTDR	(C) ← (HL) B ← B-1 HL ← HL-1 Repeat until B = 0	•	1	X	X	1	X	11 101 101 10 111 011	21 16	C to $A_0 \sim A_7$ B to $A_8 \sim A_{15}$

Notes: r, r′ means any of the registers A, B, C, D, E, H, L
ss is any of the register pairs BC, DE, HL, SP
rr is any of the register pairs BC, DE, IY, SP
① P/V flag is 0 if the result of BC-1 = 0, otherwise P/V = 1
② Z flag is 1 if A = (HL), otherwise Z = 0
③ If the result of B−1 = 0, the Z flag is set, otherwise it is reset.
e represents the extension in the relative addressing mode
e is a signed two's complement number in the range < -126, 129 >
e-2 in the op-code provides an effective address of pc+e as PC is incremented by 2 prior to the addition of e.
The notation s_b indicates bit b (0 to 7) of location s.

Flag Notation: • = flag not affected, 0 = flag reset, 1 = flag set, X = flag is unknown
‡ = flag is affected according to the result of the operation.

ASCII CHARACTER SET (7-BIT CODE)

LSD \ MSD	0 000	1 001	2 010	3 011	4 100	5 101	6 110	7 111
0 0000	NUL	DLE	SP	0	@	P	`	p
1 0001	SOH	DC1	!	1	A	Q	a	q
2 0010	STX	DC2	"	2	B	R	b	r
3 0011	ETX	DC3	=	3	C	S	c	s
4 0100	EOT	DC4	$	4	D	T	d	t
5 0101	ENG	NAK	%	5	E	U	e	u
6 0110	ACK	SYN	&	6	F	V	f	v
7 0111	BEL	ETB	'	7	G	W	g	w
8 1000	BS	CAN	(	8	H	X	h	x
9 1001	HT	EM	)	9	I	Y	i	y
A 1010	LF	SUB	*	:	J	Z	j	z
B 1011	VT	ESC	+	;	K	[	k	{
C 1100	FF	FS	,	<	L	\	l	|
D 1101	CR	GS	-	=	M	]	m	}
E 1110	SO	RS	.	>	N	↑	n	~
F 1111	SI	VS	/	?	O	←	o	DEL

HEXADECIMAL COLUMNS

6 HEX = DEC	5 HEX = DEC	4 HEX = DEC	3 HEX = DEC	2 HEX = DEC	1 HEX = DEC
0 0	0 0	0 0	0 0	0 0	0 0
1 1,048,576	1 65,536	1 4,096	1 256	1 16	1 1
2 2,097,152	2 131,072	2 8,192	2 512	2 32	2 2
3 3,145,728	3 196,608	3 12,288	3 768	3 48	3 3
4 4,194,304	4 262,144	4 16,384	4 1,024	4 64	4 4
5 5,242,880	5 327,680	5 20,480	5 1,280	5 80	5 5
6 6,291,456	6 393,216	6 24,576	6 1,536	6 96	6 6
7 7,340,032	7 458,752	7 28,672	7 1,792	7 112	7 7
8 8,388,608	8 524,288	8 32,768	8 2,048	8 128	8 8
9 9,437,184	9 589,824	9 36,864	9 2,304	9 144	9 9
A 10,485,760	A 655,360	A 40,960	A 2,560	A 160	A 10
B 11,534,336	B 720,896	B 45,056	B 2,816	B 176	B 11
C 12,582,912	C 786,432	C 49,152	C 3,072	C 192	C 12
D 13,631,488	D 851,968	D 53,248	D 3,328	D 208	D 13
E 14,680,064	E 917,504	E 57,344	E 3,584	E 224	E 14
F 15,728,640	F 983,040	F 61,440	F 3,840	F 240	F 15
0123	4567	0123	4567	0123	4567
BYTE		BYTE		BYTE	

POWERS OF 2

2^n	n
256	8
512	9
1 024	10
2 048	11
4 096	12
8 192	13
16 384	14
32 768	15
65 536	16
131 072	17
262 144	18
524 288	19
1 048 576	20
2 097 152	21
4 194 304	22
8 388 608	23
16 777 216	24

$2^0 = 16^0$	
$2^4 = 16^1$	
$2^8 = 16^2$	
$2^{12} = 16^3$	
$2^{16} = 16^4$	
$2^{20} = 16^5$	
$2^{24} = 16^6$	
$2^{28} = 16^7$	
$2^{32} = 16^8$	
$2^{36} = 16^9$	
$2^{40} = 16^{10}$	
$2^{44} = 16^{11}$	
$2^{48} = 16^{12}$	
$2^{52} = 16^{13}$	
$2^{56} = 16^{14}$	
$2^{60} = 16^{15}$	

POWERS OF 16

16^n	n
1	0
16	1
256	2
4 096	3
65 536	4
1 048 576	5
16 777 216	6
268 435 456	7
4 294 967 296	8
68 719 476 736	9
1 099 511 627 776	10
17 592 186 044 416	11
281 474 976 710 656	12
4 503 599 627 370 496	13
72 057 594 037 927 936	14
1 152 921 504 606 846 976	15

Z80–CPU INSTRUCTION SET

OBJ CODE	SOURCE STATEMENT		OPERATION
8E	ADC	A,(HL)	Add with Carry Operand to Acc.
DD8E05	ADC	A,(IX+d)	
FD8E05	ADC	A,(IY+d)	
8F	ADC	A,A	
88	ADC	A,B	
89	ADC	A,C	
8A	ADC	A,D	
8B	ADC	A,E	
8C	ADC	A,H	
8D	ADC	A,L	
CE20	ADC	A,n	
ED4A	ADC	HL,BC	Add with Carry Reg. Pair to HL
ED5A	ADC	HL,DE	
ED6A	ADC	HL,HL	
ED7A	ADC	HL,SP	
86	ADD	A,(HL)	Add Operand to Acc.
DD8605	ADD	A,(IX+d)	
FD8605	ADD	A,(IY+d)	
87	ADD	A,A	
80	ADD	A,B	
81	ADD	A,C	
82	ADD	A,D	
83	ADD	A,E	
84	ADD	A,H	
85	ADD	A,L	
C620	ADD	A,n	
09	ADD	HL,BC	Add Reg. Pair to HL
19	ADD	HL,DE	
29	ADD	HL,HL	
39	ADD	HL,SP	
DD09	ADD	IX,BC	Add Reg. Pair to IX
DD19	ADD	IX,DE	
DD29	ADD	IX,IX	
DD39	ADD	IX,SP	
FD09	ADD	IY,BC	Add Reg. Pair to IY
FD19	ADD	IY,DE	
FD29	ADD	IY,IY	
FD39	ADD	IY,SP	
A6	AND	(HL)	Logical 'AND' of Operand and Acc.
DDA605	AND	(IX+d)	
FDA605	AND	(IY+d)	
A7	AND	A	
A0	AND	B	
A1	AND	C	
A2	AND	D	
A3	AND	E	
A4	AND	H	
A5	AND	L	
E620	AND	n	
CB46	BIT	0,(HL)	Test Bit b of Location or Reg.
DDCB0546	BIT	0,(IX+d)	
FDCB0546	BIT	0,(IY+d)	
CB47	BIT	0,A	
CB40	BIT	0,B	
CB41	BIT	0,C	
CB42	BIT	0,D	
CB43	BIT	0,E	
CB44	BIT	0,H	

OBJ CODE	SOURCE STATEMENT		OPERATION
CB45	BIT	0,L	Test Bit b of Location or Reg.
CB4E	BIT	1,(HL)	
DDCB054E	BIT	1,(IX+d)	
FDCB054E	BIT	1,(IY+d)	
CB4F	BIT	1,A	
CB48	BIT	1,B	
CB49	BIT	1,C	
CB4A	BIT	1,D	
CB4B	BIT	1,E	
CB4C	BIT	1,H	
CB4D	BIT	1,L	
CB56	BIT	2,(HL)	
DDCB0556	BIT	2,(IX+d)	
FDCB0556	BIT	2,(IY+d)	
CB57	BIT	2,A	
CB50	BIT	2,B	
CB51	BIT	2,C	
CB52	BIT	2,D	
CB53	BIT	2,E	
CB54	BIT	2,H	
CB55	BIT	2,L	
CB5E	BIT	3,(HL)	
DDCB055E	BIT	3,(IX+d)	
FDCB055E	BIT	3,(IY+d)	
CB5F	BIT	3,A	
CB58	BIT	3,B	
CB59	BIT	3,C	
CB5A	BIT	3,D	
CB5B	BIT	3,E	
CB5C	BIT	3,H	
CB5D	BIT	3,L	
CB66	BIT	4,(HL)	
DDCB0566	BIT	4,(IX+d)	
FDCB0566	BIT	4,(IY+d)	
CB67	BIT	4,A	
CB60	BIT	4,B	
CB61	BIT	4,C	
CB62	BIT	4,D	
CB63	BIT	4,E	
CB64	BIT	4,H	
CB65	BIT	4,L	
CB6E	BIT	5,(HL)	
DDCB056E	BIT	5,(IX+d)	
FDCB056E	BIT	5,(IY+d)	
CB6F	BIT	5,A	
CB68	BIT	5,B	
CB69	BIT	5,C	
C86A	BIT	5,D	
CB6B	BIT	5,E	
CB6C	BIT	5,H	
CB6D	BIT	5,L	
CB76	BIT	6,(HL)	
DDCB0576	BIT	6,(IX+d)	
FDCB0576	BIT	6,(IY+d)	
CB77	BIT	6,A	
CB70	BIT	6,B	
CB71	BIT	6,C	
CB72	BIT	6,D	
CB73	BIT	6,E	
CB74	BIT	6,H	
CB75	BIT	6,L	
CB7E	BIT	7,(HL)	
DDCB057E	BIT	7,(IX+d)	

OBJ CODE	SOURCE STATEMENT		OPERATION
FDCB057E	BIT	7,(IY+d)	Test Bit b Location or Reg.
CB7F	BIT	7,A	
CB78	BIT	7,B	
CB79	BIT	7,C	
CB7A	BIT	7,D	
CB7B	BIT	7,E	
CB7C	BIT	7,H	
CB7D	BIT	7,L	
DC8405	CALL	C,nn	Call Subroutine at Location nn if Condition True
FC8405	CALL	M,nn	
D48405	CALL	NC,nn	
C48405	CALL	NZ,nn	
F48405	CALL	P,nn	
EC8405	CALL	PE,nn	
E48405	CALL	PO,nn	
CC8405	CALL	Z,nn	
CD8405	CALL	nn	Unconditional Call to Subroutine at nn
3F	CCF		Complement Carry Flag
BE	CP	(HL)	Compare Operand with Acc.
DDBE05	CP	(IX+d)	
FDBE05	CP	(IY+d)	
BF	CP	A	
B8	CP	B	
B9	CP	C	
BA	CP	D	
BB	CP	E	
BC	CP	H	
BD	CP	L	
FE20	CP	n	
EDA9	CPD		Compare Location (HL) and Acc. Decrement HL and BC
EDB9	CPDR		Compare Location (HL) and Acc. Decrement HL and BC, Repeat until BC = 0
EDA1	CPI		Compare Location (HL) and Acc., Increment HL and Decrement BC
EDB1	CPIR		Compare Location (HL) and Acc. Increment HL, Decrement BC, Repeat until BC = 0
2F	CPL		Complement Acc. (1's Comp)
27	DAA		Decimal Adjust Acc.
35	DEC	(HL)	Decrement Operand
DD3505	DEC	(IX+d)	
FD3505	DEC	(IY+d)	
3D	DEC	A	
05	DEC	B	
0B	DEC	BC	
0D	DEC	C	
15	DEC	D	
1B	DEC	DE	

OBJ CODE	SOURCE STATEMENT		OPERATION
1D	DEC	E	Decrement Operand
25	DEC	H	
2B	DEC	HL	
DD2B	DEC	IX	
FD2B	DEC	IY	
2D	DEC	L	
3B	DEC	SP	
F3	DI		Disable Interrupts
102E	DJNZ	e	Decrement B and Jump Relative if B = 0
FB	EI		Enable Interrupts
E3	EX	(SP),HL	Exchange Location and (SP)
DDE3	EX	(SP),IX	
FDE3	EX	(SP),IY	
08	EX	AF,AF'	Exchange the Contents of AF and AF'
EB	EX	DE,HL	Exchange the Contents of DE and HL
D9	EXX		Exchange the Contents of BC,DE,HL with Contents of BC',DE',HL' Respectively
76	HALT		HALT (Wait for Interrupt or Reset)
ED46	IM	0	Set Interrupt Mode
ED56	IM	1	
ED5E	IM	2	
ED78	IN	A,(C)	Load Reg. with Input from Device (C)
ED40	IN	B,(C)	
ED48	IN	C,(C)	
ED50	IN	D,(C)	
ED58	IN	E,(C)	
ED60	IN	H,(C)	
ED68	IN	L,(C)	
34	INC	(HL)	Increment Operand
DD3405	INC	(IX+d)	
FD3405	INC	(IY+d)	
3C	INC	A	
04	INC	B	
03	INC	BC	
0C	INC	C	
14	INC	D	
13	INC	DE	
1C	INC	E	
24	INC	H	
23	INC	HL	
DD23	INC	IX	
FD23	INC	IY	
2C	INC	L	
33	INC	SP	
DB20	IN	A,(n)	Load Acc. with Input from Device n
EDAA	IND		Load Location (HL) with Input from Port (C), Decrement HL and B

OBJ CODE	SOURCE STATEMENT		OPRRTION
EDBA	INDR		Load Location (HL) with Input from Port (C), Decrement HL and Decrement B, Repeat until B = 0
EDA2	INI		Load Location (HL) with Input from Port (C); Increment HL and Decrement B
EDB2	INIR		Load Location (HL) with Input from Port (C), Increment HL and Decrement B, Repeat until B = 0
E9	JP	(HL)	Unconditional Jump to Location
DDE9	JP	(IX)	
C38405	JP	nn	
FDE9	JP	(IY)	
DA8405	JP	C,nn	Jump to Location if Condition True
FA8405	JP	M,nn	
D28405	JP	NC,nn	
C28405	JP	NZ,nn	
F28405	JP	P,nn	
EA8405	JP	PE,nn	
E28405	JP	PO,nn	
CA8405	JP	Z,nn	
382E	JR	C,e	Jump Relative to PC+e if Condition True
302E	JR	NC,e	
202E	JR	NZ,e	
282E	JR	Z,e	
182E	JR	e	Unconditional Jump Relative to PC+e
02	LD	(BC),A	Load Source to Destination
12	LD	(DE),A	
77	LD	(HL),A	
70	LD	(HL),B	
71	LD	(HL),C	
72	LD	(HL),D	
73	LD	(HL),E	
74	LD	(HL),H	
75	LD	(HL),L	
3620	LD	(HL),n	
DD7705	LD	(IX+d),A	
DD7005	LD	(IX+d),B	
DD7105	LD	(IX+d),C	
DD7205	LD	(IX+d),D	
DD7305	LD	(IX+d),E	
DD7405	LD	(IX+d),H	
DD7505	LD	(IX+d),L	
DD360520	LD	(IX+d),n	
FD7705	LD	(IY+d),A	
FD7005	LD	(IY+d),B	
FD7105	LD	(IY+d),C	
FD7205	LD	(IY+d),D	
FD7305	LD	(IY+d),E	
FD7405	LD	(IY+d),H	
FD7505	LD	(IY+d),L	
FD360520	LD	(IY+d),n	
328405	LD	(nn),A	
ED438405	LD	(nn),BC	

OBJ CODE	SOURCE STATEMENT		OPERATION
ED538405	LD	(nn),DE	Load Source to Destination
228405	LD	(nn),HL	
DD228405	LD	(nn),IX	
FD228405	LD	(nn),IY	
ED738405	LD	(nn),SP	
0A	LD	A,(BC)	
1A	LD	A,(DE)	
7E	LD	A,(HL)	
DD7E05	LD	A,(IX+d)	
FD7E05	LD	A,(IY+d)	
3A8405	LD	A,(nn)	
7F	LD	A,A	
78	LD	A,B	
79	LD	A,C	
7A	LD	A,D	
7B	LD	A,E	
7C	LD	A,H	
ED57	LD	A,I	
7D	LD	A,L	
3E20	LD	A,n	
ED5F	LD	A,R	
46	LD	B,(HL)	
DD4605	LD	B,(IX+d)	
FD4605	LD	B,(IY+d)	
47	LD	B,A	
40	LD	B,B	
41	LD	B,C	
42	LD	B,D	
43	LD	B,E	
44	LD	B,H	
45	LD	B,L	
0620	LD	B,n	
ED4B8405	LD	BC,(nn)	
018405	LD	BC,nn	
4E	LD	C,(HL)	
DD4E05	LD	C,(IX+d)	
FD4E05	LD	C,(IY+d)	
4F	LD	C,A	
48	LD	C,B	
49	LD	C,C	
4A	LD	C,D	
4B	LD	C,E	
4C	LD	C,H	
4D	LD	C,L	
0E20	LD	C,n	
56	LD	D,(HL)	
DD5605	LD	D,(IX+d)	
FD5605	LD	D,(IY+d)	
57	LD	D,A	
50	LD	D,B	
51	LD	D,C	
52	LD	D,D	
53	LD	D,E	
54	LD	D,H	
55	LD	D,L	
1620	LD	D,n	
ED5B8405	LD	DE,(nn)	
118405	LD	DE,nn	
5E	LD	E,(HL)	
DD5E05	LD	E,(IX+d)	
FD5E05	LD	E,(IY+d)	
5F	LD	E,A	
58	LD	E,B	
59	LD	E,C	

OBJ CODE	SOURCE STATEMENT		OPERATION
5A	LD	E,D	Load Source to Destination
5B	LD	E,E	
5C	LD	E,H	
5D	LD	E,L	
1E20	LD	E,n	
66	LD	H,(HL)	
DD6605	LD	H,(IX+d)	
FD6605	LD	H,(IY+d)	
67	LD	H,A	
60	LD	H,B	
61	LD	H,C	
62	LD	H,D	
63	LD	H,E	
64	LD	H,H	
65	LD	H,L	
2620	LD	H,n	
2A8405	LD	HL,(nn)	
218405	LD	HL,nn	
ED47	LD	I,A	
DD2A8405	LD	IX,(nn)	
DD218405	LD	IX,nn	
FD2A8405	LD	IY,(nn)	
FD218405	LD	IY,nn	
6E	LD	L,(HL)	
DD6E05	LD	L,(IX+d)	
FD6E05	LD	L,(IY+d)	
6F	LD	L,A	
68	LD	L,B	
69	LD	L,C	
6A	LD	L,D	
6B	LD	L,E	
6C	LD	L,H	
6D	LD	L,L	
2E20	LD	L,n	
ED4F		LD R,A	
ED7B8405	LD	SP,(nn)	
F9	LD	SP,HL	
DDF9	LD	SP,IX	
FDF9	LD	SP,IY	
318405	LD	SP,nn	
EDA8	LDD		Load Location (DE) with Location (HL), Decrement DE,HL and BC
EDB8	LDDR		Load Location (DE) with Location (HL), Repeat until BC = 0
EDA0	LDI		Load Location (DE) with Location (HL), Increment DE,HL, Decrement BC
EDB0	LDIR		Load Location (DE) with Location (HL), Increment DE,HL, Decrement BC and Repeat until BC = 0
ED44	NEG		Negate Acc. (2's Complement)
00	NOP		No Operation
B6	OR	(HL)	Logical "OR" of Operand and Acc.
DDB605	OR	(IX+d)	
FDB605	OR	(IY+d)	
B7	OR	A	
B0	OR	B	
B1	OR	C	
B2	OR	D	
B3	OR	E	
B4	OR	H	
B5	OR	L	
F620	OR	n	
ED8B	OTDR		Load Output Port (C) with Location (HL) Decrement HL and B, Repeat until B = 0
EDB3	OTIR		Load Output Port (C) with Location (HL), Increment HL, Decrement B, Repeat until B = 0
ED79	OUT	(C),A	Load Output Port (C) with Reg.
ED41	OUT	(C),B	
ED49	OUT	(C),C	
ED51	OUT	(C),D	
ED59	OUT	(C),E	
ED61	OUT	(C),H	
ED69	OUT	(C),L	
D320	OUT	(n),A	Load Output Port (n) with Acc.
EDAB	OUTD		Load Output Port (C) with Location (HL), Decrement HL and B
EDA3	OUTI		Load Output Port (C) with Location (HL), Increment HL and Decrement B
F1	POP	AF	Load Destination with Top of Stack
C1	POP	BC	
D1	POP	DE	
E1	POP	HL	
DDE1	POP	IX	
FDE1	POP	IY	
F5	PUSH	AF	Load Source to Stack
C5	PUSH	BC	
D5	PUSH	DE	
E5	PUSH	HL	
DDE5	PUSH	IX	
FDE5	PUSH	IY	
CB86	RES	0,(HL)	Reset Bit b of Operand
DDCB0586	RES	0,(IX+d)	
FDCB0586	RES	0,(IY+d)	
CB87	RES	0,A	
CB80	RES	0,B	
CB81	RES	0,C	
CB82	RES	0,D	
CB83	RES	0,E	
CB84	RES	0,H	
CB85	RES	0,L	
CB8E	RES	1,(HL)	
DDCB058E	RES	1,(IX+d)	
FDCB058E	RES	1,(IY+d)	
CB8F	RES	1,A	
CB88	RES	1,B	Reset Bit b of Operand
CB89	RES	1,C	
CB8A	RES	1,D	
CB8B	RES	1,E	
CB8C	RES	1,H	
CB8D	RES	1,L	
CB96	RES	2,(HL)	
DDCB0596	RES	2,(IX+d)	
FDCB0596	RES	2,(IY+d)	
CB97	RES	2,A	
CB90	RES	2,B	
CB91	RES	2,C	
CB92	RES	2,D	
CB93	RES	2,E	
CB94	RES	2,H	
CB95	RES	2,L	
CB9E	RES	3,(HL)	
DDCB059E	RES	3,(IX+d)	
FDCB059E	RES	3,(IY+d)	
CB9F	RES	3,A	
CB98	RES	3,B	
CB99	RES	3,C	
CB9A	RES	3,D	
CB9B	RES	3,E	
CB9C	RES	3,H	
CB9D	RES	3,L	
CBA6	RES	4,(HL)	
DDCB05A6	RES	4,(IX+d)	
FDCB05A6	RES	4,(IY+d)	
CBA7	RES	4,A	
CBA0	RES	4,B	
CBA1	RES	4,C	
CBA2	RES	4,D	
DBA3	RES	4,E	
CBA4	RES	4,H	
CBA5	RES	4,L	
CBAE	RES	5,(HL)	
DDCB05AE	RES	5,(IX+d)	
FDCB05AE	RES	5,(IY+d)	
CBAF	RES	5,A	
CBA8	RES	5,B	
CBA9	RES	5,C	
CBAA	RES	5,D	
CBAB	RES	5,E	
CBAC	RES	5,H	
CBAD	RES	5,L	
CBB6	RES	6,(HL)	
DDCB05B6	RES	6,(IX+d)	
FDCB05B6	RES	6,(IY+d)	
CBB7	RES	6,A	
CBB0	RES	6,B	
CBB1	RES	6,C	
CBB2	RES	6,D	
CBB3	RES	6,E	
CBB4	RES	6,H	
CBB5	RES	6,L	
CBBE	RES	7,(HL)	
DDCB05BE	RES	7,(IX+d)	
FDCB05BE	RES	7,(IY+d)	
CBBF	RES	7,A	
CBB8	RES	7,B	
CBB9	RES	7,C	
CBBA	RES	7,D	

OBJ CODE	SOURCE STATEMENT		OPERATION
CBBB	RES	7,E	Reset Bit b of Operand
CBBC	RES	7,H	
CBBD	RES	7,L	
C9	RET		Return from Subroutine
D8	RET	C	Return from Subroutine if Condition True
F8	RET	M	
D0	RET	NC	
C0	RET	NZ	
F0	RET	P	
E8	RET	PE	
E0	RET	P0	
C8	RET	Z	
ED4D	RETI		Return from Interrupt
ED45	RETN		Return from Non-Maskable Interrupt
CB16	RL	(HL)	Rotate Left Through Carry
DDCB0516	RL	(IX+d)	
FDCB0516	RL	(IY+d)	
CB17	RL	A	
CB10	RL	B	
CB11	RL	C	
CB12	RL	D	
CB13	RL	E	
CB14	RL	H	
CB15	RL	L	
17	RLA		Rotate Left Acc. Through Carry
CB06	RLC	(HL)	Rotate Left Circular
DDCB0506	RLC	(IX+d)	
FDCB0506	RLC	(IY+d)	
CB07	RLC	A	
CB00	RLC	B	
CB01	RLC	C	
CB02	RLC	D	
CB03	RLC	E	
CB04	RLC	H	
CB05	RLC	L	
07	RLCA		Rotate Left Circular Acc.
ED6F	RLD		Rotate Digit Left and Right between Acc. and and Location (HL)
CB1E	RR	(HL)	Rotate Right Through Carry
DDCB051E	RR	(IX+d)	
FDCB051E	RR	(IY+d)	
CB1F	RR	A	
CB18	RR	B	
CB19	RR	C	
CB1A	RR	D	
CB1B	RR	E	
CB1C	RR	H	
CB1D	RR	L	
1F	RRA		Rotate Right Acc. Through Carry
CB0E	RRC	(HL)	Rotate Right Circular
DDCB050E	RRC	(IX+d)	
FDCB050E	RRC	(IY+d)	
CB0F	RRC	A	

OBJ CODE	SOURCE STATEMENT		OPERATION
CB08	RRC	B	Rotate Right Circular
CB09	RRC	C	
CB0A	RRC	D	
CB0B	RRC	E	
CB0C	RRC	H	
CB0D	RRC	L	
OF	RRCA		Rotate Right Circular Acc.
ED67	RRD		Rotate Digit Right and Left Between Acc. and Location (HL)
C7	RST	00H	Restart to Location
CF	RST	08H	
D7	RST	10H	
DF	RST	18H	
E7	RST	20H	
EF	RST	28H	
F7	RST	30H	
FF	RST	38H	
9E	SBC	A,(HL)	Subtract Operand from Acc. with Carry
DD9E05	SBC	A,(IX+d)	
FD9E05	SBC	A,(IY+d)	
9F	SBC	A,A	
98	SBC	A,B	
99	SBC	A,C	
9A	SBC	A,D	
9B	SBC	A,E	
9C	SBC	A,H	
9D	SBC	A,L	
DE20	SBC	A,n	
ED42	SBC	HL,BC	
ED52	SBC	HL,DE	
ED62	SBC	HL,HL	
ED72	SBC	HL,SP	
37	SCF		Set Carry Flag (C = 1)
CBC6	SET	0,(HL)	Set Bit b of Location
DDCB05C6	SET	0,(IX+d)	
FDCB05C6	SET	0,(IY+d)	
CBC7	SET	0,A	
CBC0	SET	0,B	
CBC1	SET	0,C	
CBC2	SET	0,D	
CBC3	SET	0,E	
CBC4	SET	0,H	
CBC5	SET	0,L	
CBCE	SET	1,(HL)	
DDCB05CE	SET	1,(IX+d)	
FDCB05CE	SET	1,(IY+d)	
CBCF	SET	1,A	
CBC8	SET	1,B	
CBC9	SET	1,C	
CBCA	SET	1,D	
CBCB	SET	1,E	
CBCC	SET	1,H	
CBCD	SET	1,L	
CBD6	SET	2,(HL)	
DDCB05D6	SET	2,(IX+d)	
FDCB05D6	SET	2,(IY+d)	
CBD7	SET	2,A	
CBD0	SET	2,B	
CBD1	SET	2,C	
CBD2	SET	2,D	

OBJ CODE	SOURCE STATEMENT		OPERATION
CBD3	SET	2,E	Set Bit b of Location
CBD4	SET	2,H	
CBD5	SET	2,L	
CBD8	SET	3,B	
CBDE	SET	3,(HL)	
DDCB05DE	SET	3,(IX+d)	
FDCB05DE	SET	3,(IY+d)	
CBDF	SET	3,A	
CBD9	SET	3,C	
CBDA	SET	3,D	
CBDB	SET	3,E	
CBDC	SET	3,H	
CBDD	SET	3,L	
CBE6	SET	4,(HL)	
DDCB05E6	SET	4,(IX+d)	
FDCB05E6	SET	4,(IY+d)	
CBE7	SET	4,A	
CBE0	SET	4,B	
CBE1	SET	4,C	
CBE2	SET	4,D	
CBE3	SET	4,E	
CBE4	SET	4,H	
CBE5	SET	4,L	
CBEE	SET	5,(HL)	
DDCB05EE	SET	5,(IX+d)	
FDCB05EE	SET	5,(IY+d)	
CBEF	SET	5,A	
CBE8	SET	5,B	
CBE9	SET	5,C	
CBEA	SET	5,D	
CBEB	SET	5,E	
CBEC	SET	5,H	
CBED	SET	5,L	
CBF6	SET	6,(HL)	
DDCB05F6	SET	6,(IX+d)	
FDCB05F6	SET	6,(IY+d)	
CBF7	SET	6,A	
CBF0	SET	6,B	
CBF1	SET	6,C	
CBF2	SET	6,D	
CBF3	SET	6,E	
CBF4	SET	6,H	
CBF5	SET	6,L	
CBFE	SET	7,(HL)	
DDCB05FE	SET	7,(IX+d)	
FDCB05FE	SET	7,(IY+d)	
CBFF	SET	7,A	
CBF8	SET	7,B	
CBF9	SET	7,C	
CBFA	SET	7,D	
CBFB	SET	7,E	
CBFC	SET	7,H	
CBFD	SET	7,L	
CB26	SLA	(HL)	Shift Operand Left Arithmetic
DDCB0526	SLA	(IX+d)	
FDCB0526	SLA	(IY+d)	
CB27	SLA	A	
CB20	SLA	B	
CB21	SLA	C	
CB22	SLA	D	
CB23	SLA	E	
CB24	SLA	H	
CB25	SLA	L	

OBJ CODE	SOURCE STATEMENT		OPERATION
CB2E	SRA	(HL)	Shift Operand Right
DDCB052E	SRA	(IX+d)	Arithmetic
FDCB052E	SRA	(IY+d)	
CB2F	SRA	A	
CB28	SRA	B	
CB29	SRA	C	
CB2A	SRA	D	
CB2B	SRA	E	
CB2C	SRA	H	
CB2D	SRA	L	
CB3E	SRL	(HL)	Shift Operand Right
DDCB053E	SRL	(IX+d)	Logical
FDCB053E	SRL	(IY+d)	
CB3F	SRL	A	
CB38	SRL	B	
CB39	SRL	C	
CB3A	SRL	D	
CB3B	SRL	E	
CB3C	SRL	H	
CB3D	SRL	L	
96	SUB	(HL)	Subtract Operand
DD9605	SUB	(IX+d)	from Acc.
FD9605	SUB	(IY+d)	
97	SUB	A	
90	SUB	B	
91	SUB	C	
92	SUB	D	
93	SUB	E	
94	SUB	H	
95	SUB	L	
D620	SUB	n	
AE	XOR	(HL)	Exclusive "OR"
DDAE05	XOR	(IX+d)	Operand and Acc.
FDAE05	XOR	(IY+d)	
AF	XOR	A	
A8	XOR	B	
A9	XOR	C	
AA	XOR	D	
AB	XOR	E	
AC	XOR	H	
AD	XOR	L	
EE20	XOR	n	

Example Values

nn	EQU	584H
d	EQU	5
n	EQU	20H
e		30H

RIO

RIO I/O REQUEST VECTOR							
LOGICAL UNIT	REQUEST	DATA TRANSFER ADDRESS	DATA LENGTH	COMPLETION RETURN ADDRESS	ERROR RETURN ADDRESS	COMPLETION CODE	SUPPLEMENTAL PARAMETER VECTOR ADDRESS
0	1	2-3	4-5	6-7	8-9	A	B-C

SUPPLEMENTAL PARAMETER VECTOR			
TYPE OPEN OR ASSIGN	DRIVE SPECIFIER	LENGTH OF NAME	NAME
0	1	2	3 . . . .

I/O REQUEST CODE (RETURN WHEN COMPLETE)		I/O REQUEST CODE (RETURN WHEN COMPLETE)	
0	INITIALIZE	1A	ERASE FILE
2	ASSIGN	1C	READ AND DELETE
4	OPEN	1E	READ CURRENT RECORD
6	CLOSE	20	READ CURRENT RECORD
8	REWIND	22	READ PREVIOUS RECORD
A	READ BINARY	24	SKIP FORWARD
C	READ ASCII	26	SKIP BACKWARD
E	WRITE BINARY	28	SKIP TO END
10	WRITE ASCII	2A	RENAME
12	WRITE CURRENT RECORD	2C	UPDATE
14	WRITE DIRECT	2E	SET ATTRIBUTES
16	DELETE	30	QUERY ATTRIBUTES
18	DELETE REMAINING		

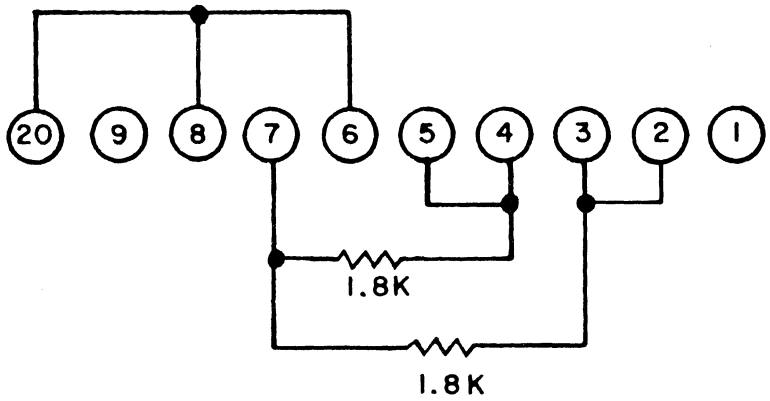
COMPLETION CODE	MEANING	COMPLETION CODE	MEANING
40	INVALID DRIVE NAME	C6	DATA TRANSFER ERROR
41	INVALID OR INACTIVE DEVICE	C7	FILE NOT FOUND
42	INVALID UNIT	C9	END OF FILE ERROR
43	MEMORY PROTECT VIOLATION	CA	POINTER CHECK ERROR
44	MISSING OR INVALID OPERAND(S)	CB	FILE NOT OPEN
45	SYSTEM ERROR	CC	UNIT ALREADY ACTIVE (OPEN)
46	ILLEGAL FILE NAME	CD	ASSIGN BUFFER FULL
47	NON-EXISTENT COMMAND	CE	INVALID DRIVE SPECIFICATION
48	ILLEGAL FILE TYPE	CF	LOGICAL UNIT TABLE FULL (>16 OPEN)
49	PROGRAM ABORT		
4A	INSUFFICIENT MEMORY		
4B	MISSING OR INVALID FILE PROPERTIES	D0	DUPLICATE FILE
		D1	DISKETTE ID ERROR
80	OPERATION COMPLETE	D2	INVALID ATTRIBUTES
81	DIRECTORY FORMAT ERROR	D3	DISK IS FULL
82	SCRATCH FILE CREATED	D4	FILE NOT IN PROPER DIRECTORY RECORD
83	FILE NAME TRUNCATED		
84	ATTRIBUTE LIST TRUNCATED	D5	BEGINNING OF FILE ERROR
		D6	FILE ALREADY OPEN ON OTHER UNIT
C1	INVALID OPERATION (REQUEST)	D7	INVALID RENAME TO SCRATCH FILE
C2	DEVICE IS NOT READY	D8	FILE LOCKED (ATTEMPT TO CHANGE ATTRIBUTES)
C3	WRITE PROTECTION		
C4	SECTOR ADDRESS ERROR	D9	INVALID OPEN REQUEST
C5	SEEK ERROR		

ZDOS RETURN CODES

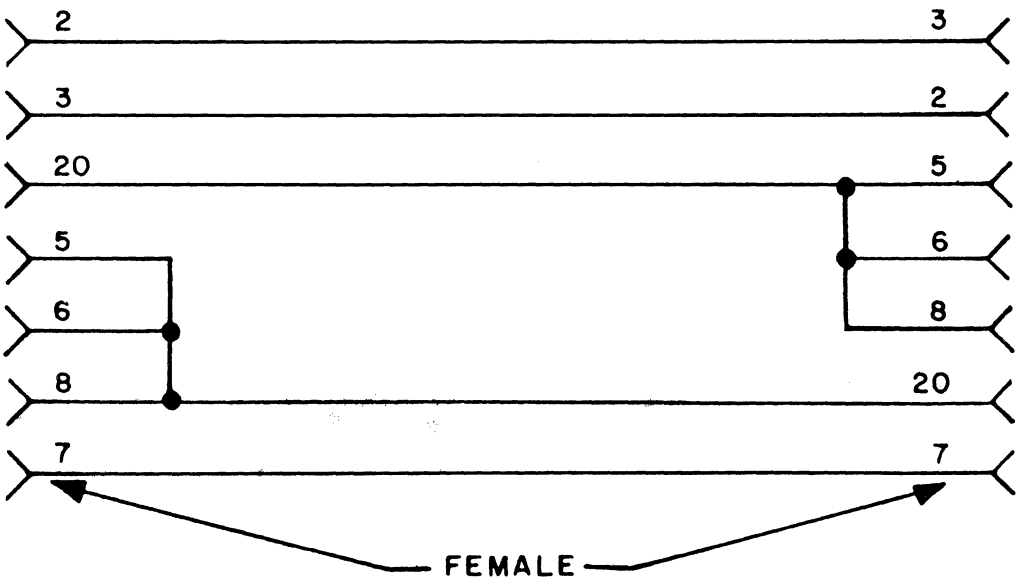
DATA LOST	DISK ERROR	
C 1	8 1	INVALID OPERATION
C 2	8 2	DUPLICATE FILE
C 3	8 3	ACTIVE FILE TABLE FULL
C 4	8 4	FILE NOT FOUND
C 5	8 5	DIRECTORY FULL
C 6	8 6	SYSTEM ERROR
C 8	8 8	FILE NOT OPEN
C 9	8 9	END OF FILE
C A	8 A	DISK ERROR
C B	8 B	DISK FULL
C C	8 C	POINTER ERROR
C D	8 D	BEGINNING OF FILE
C E	8 E	FILE ALREADY OPEN
C F	8 F	DISK NOT READY
D 0	9 0	WRONG DISK
D 1	9 1	NONEXISTENT DISK

ZDOS REQUEST CODES								
REQUEST	03	BUFFER ADDR	NOT USED	# RECORDS	fn	ft	UNIT	ERROR CODE
0	1	2-3	4-5	6	7-12	13	14	15

REQUEST CODE	OPERATION
08	INITIALIZE
0C	OPEN
0E	CREATE
10	CLOSE
12	ERASE
14	RENAME
16	REWIND
18	READ n RECORDS
1A	READ CURRENT RECORD
1C	READ PREVIOUS RECORD
1E	SKIP n RECORDS
20	BACK n RECORDS
22	REWRITE CURRENT RECORD
24	INSERT n RECORDS
26	DELETE n RECORDS



TURN AROUND PLUG
25 PIN CINCH CONNECTOR (FEMALE)
APN 99999-022



CROSS COUPLER
25 PIN CINCH CONNECTOR (FEMALE)
APN 99999-015

This page intentionally left blank.

General Terminal Corporation

Technical publications remarks form

Title : _____

Reference no. : _____ Dated : _____

ERRORS IN PUBLICATION

SUGGESTIONS FOR IMPROVEMENT TO PUBLICATION PLEASE FEEL FREE TO COMMENT ON THE EQUIPMENT, ALSO.

Your comments will be promptly investigated by qualified technical personnel and action will be taken as required

If you require a written reply, check here and furnish complete mailing address below. ☐

FROM : **NAME** _____ **DATE** _____

TITLE _____

COMPANY _____

ADDRESS _____

_____

CUT ALONG LINE

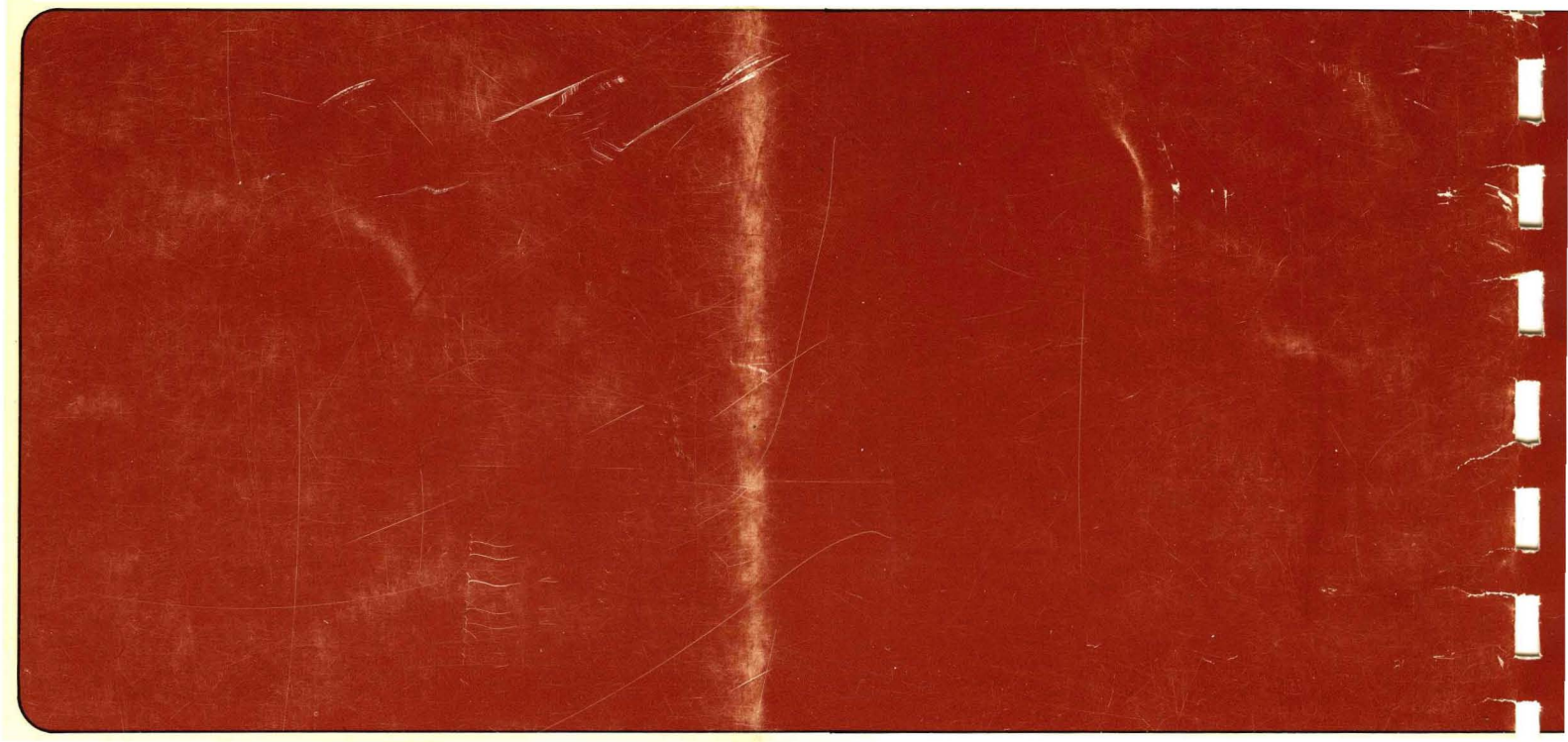
Please give this technical publications remarks form to your GTC representative.

General Terminal Corporation

or mail to :

General Terminal Corporation

GTC Incorporated
14831 Franklin Avenue
Tustin, California 92680
ATT: Marketing Support Publications



GTC®

General Terminal Corporation

14831 Franklin Avenue
Tustin, California 92680
(800) 854-6925

Part Number
05007-001