6800-6809 MOTHER BOARD

INTRODUCTION

The GIMIX GHOST MOTHER BOARD provides bus interconnections and physical support for the other boards in the GIMIX GHOST computer. It has 15 slots for full-sized (SS-50) boards, and 8 slots for I/O-sized (SS-30) boards, plus a special 10 pin slot for the baud rate generator. The board has many features which make it very versatile and easy to use in a variety of applications and configurations.

FEATURES

* Fully compatible with the SS-50 (6800) and SS-50C (6809) buses.
* Gold bus connectors
* 4, 8, or 16 decoded addresses per I/O slot
* Extended address decoding for the I/O section
* The I/O block is DIP-switch addressable to any 32, 64, or 128 byte boundary (depending on the selected number of addresses per slot).
* Baud rate generator (75 to 38,400 baud)
* All data, address, and control lines are terminated and separatd by noise reducing ground lines.

HARDWARE CONFIGURATION

I/O SLOT SIZE

There are two ways to change the I/O slot size depending on the users needs. The board is normally supplied with one 74LS244 IC. installed at location U-5 and DIP-switch S2-3 ON (CLOSED). This selects 16 decoded addresses per I/O slot which is normal for 6809 systems. To select either 4 or 8 addresses per slot move the 74LS244 to location U-3 (4 addresses) or U-4 (8 addresses) and set the corresponding section of S-2 ON (S2-1 for 4 and S2-2 for 8).

If you wish to be able to change I/O slot size by DIP-switch alone without moving the 74LS244 you can install additional 74LS244s at locations U-3 and U-4 and turn on the proper switch section for the desired slot size. NOTE: BE SURE ONLY THE DIP-SWITCH SECTION CORRESPONDING TO THE DESIRED SLOT SIZE IS ON, THE OTHER 2 OF THE 3 SECTIONS (S2-1,2,3,) THAT CONTROL SLOT SIZE MUST BE OFF.

Regardless of the method selected for determining I/O slot size, when using 8 addresses per slot, S2-4 (A5) MUST BE OFF (OPEN) for correct address decoding. When using 16 addresses per slot, S2-4 (A5) and S2-5 (A6) MUST BE IN THE OFF (OPEN) POSITION for correct decoding.

I/O BLOCK ADDRESSING

The entire I/O block is enabled or disabled by S1, section 1. The base address of the I/O block is set by DIP-switch S1; sections 2, 3, 4, and 5 ; and S2, sections 3, 4, 5, 6, 7, 8, 9, and 10. Extended address decoding for the I/O block is enabled or disabled by S1; section 6, and set by S1; sections 7, 8, 9, and 10.

If S1-1 is ON (CLOSED) the entire I/O block is disabled and does not appear in the address space. S1-1 should be set OFF (OPEN) to enable the I/O section.

S1; sections 2 through 5, correspond to address bits A12 through A15 respectivly and S2; sections 4 through 10 correspond to A5 through A11. These switches should be set to match the bit pattern for the desired base address. A switch set ON (CLOSED) corrresponds to a 1 in that bit position and a switch set OFF (OPEN) corresponds to a 0.

If S1-6 is OFF (OPEN) extended address decoding is disabled and the board only decodes the regular 16 address lines. If S1-6 is ON (CLOSED) the I/O block responds to both the regular 16 address lines and the 4 SS-50C extended address lines. When extended address decoding is enabled, the desired extended address is set using S1; sections 7 through 10, which correspond to address lines A16 through A19. A switch set ON (CLOSED) corresponds to a 1 in that bit position and a switch set OFF (OPEN) corresponds to a 0.

ADDRESSING EXAMPLE

STANDARD ADDRESS CONFIGURATION FOR 6809 SYSTEMS USING GMXBUG-09 AND GIMIX FLEX™

S2				S1		
SECTION	SETTING			SECTION	SETTING	
1	OFF	4	16 ADDR.	1	OFF	I/O ENABLE
2	OFF	8	PER SLOT	2	OFF	A12 = 0
3	ON	16		3	ON	A13 = 1
4	OFF	A5	MUST BE	4	ON	A14 = 1
5	OFF	A6	OFF	5	ON	A15 = 1
6	OFF	A7	= 0	6	OFF	EXT ADD OFF
7	OFF	A8	= 0	7	X	DON'T CARE
8	OFF	A9	= 0	8	X	DON'T CARE
9	OFF	A10	= 0	9	X	DON'T CARE
10	OFF	A11	= 0	10	X	DON'T CARE

THE ABOVE EXAMPLE SHOWS THE BOARD SET FOR 16 ADDRESS PER I/O SLOT, I/O BOCK ENABLED AT $E000, AND EXTENDED ADDRESSING DISABLED. NOTE: S2,4 and 5 must be off when using 16 addresses per slot.

JUMPER OPTIONS

BAUD RATE OPTION JUMPER (JA-1)

JA-1 is used to connect the baud rate lines from the 30 pin I/O bus to the corresponding lines on the 50 pin bus. This jumper area consists of 2 rows of 5 pins which can be strapped as required using wire-wrap or standard 0.1" jumper blocks. Do not install jumpers if the extended address lines are being used. Figure A, of the switch and jumper options drawing shows the pinouts for JA-1.

INTERRUPT OPTION * UD-1 UD-2 JUMPER (JA-2)

JA-2 is used to connect either the NMI line or the 6809 FIRQ line from the 50 pin bus to the FIRQ/NMI line of the 30 pin bus. Figures C and D of the switch and jumper options drawing show the proper jumper position for connecting either interrupt to the 30 pin bus. This jumper area also provides external connection points for the SS-50 user defined lines: UD-1 and UD-2. Figure B shows the pinouts of JA-2.

SLOW I/O OPTION JUMPER (JA-3)

The motherboard includes a slow I/O circuit for use with 6809 systems. When enabled the circuit generates a pulse on te 6809 MRDY line each time an I/O port is accessed by the processor. This allows slower I/O devices, such as disk controllers, to be used in systems with 1.5 or 2 MHz. clock speeds. Figures E, F, and G of the switch and jumper options drawings show the pinout of JA-3 and the proper jumper positions for slow I/O ON and OFF.

PIO DISK OPTION * UD-3 UD-4 JUMPER

When using 30 pin PIO (programmed I/O) disk controllers such as the GIMIX 5/8 or DOUBLE DENSITY PIO controllers at 4 addresses per I/O slot, a jumper is required to connect the I/O select line from I/O port #5 to the RS-2 (UD-3) line of the 30 pin bus. JA-4 provides this jumper option. Figures H, I, and J show the pinouts and jumper positions for JA-4. This jumper area also provides external connection points for the user defined lines UD-3 and UD-4 in 6800 applications.

TERMINATION OPTIONS JA-5

JA-5 provides two options for terminating the SS-50C MRDY / SS-50 MRST and the SS-50C BUSY / SS-50 NMI bus lines. These lines are normally pulled-up to the +5V supply with the jumpers shown in figure L of the switch and jumper option drawing. By changing the jumpers these lines can be connected to passive terminating networks, instead of the pull-ups, for special applications. Figure K shows the pinouts of JA-5

EXTERNAL CONNECTIONS

POWER SUPPLY CONNECTIONS

Power connections to the board are provided by solder pads located near the center of the board. The 8V bus is split into two separate sections to allow greater current capacity. The board is normally supplied with wires attached to the pads, for connection to the power supply. These wires are color coded as follows:

BLACK ----- COMMON GROUND RETURN
TAN ------- + 8V DC (First 9 50 pin slots)
RED ------- + 8V DC (Last 6 50 pin slots + I/O section)
YELLOW ---- + 16 V DC
BLUE ------ - 16 V DC

The 8 Volt output of the GIMIX power supply is split into two separate sections with separate fuses. The two fuses can be selected to provide the required current to each of the two motherboard sections. The combined total current rating of the two fuses must not exceed the 30 Amp. maximum capacity of the power supply. Systems are normally supplied with two 15 Amp. fuses installed. The maximum fuse size is limited to 25 Amps. by the fuse clip rating. Fuses rated for 32 Volts should be used to limit voltage drop across the fuse. If 125 or 250 Volt fuses are used the drop at higher current will be excessive.

6800 MASTER RESET CONNECTOR CA-1

The front panel reset switch on GIMIX systems is provided with a 5 pin connector. A matching connector, CA-1, on the motherboard is used to connect the switch to the 6800 reset line MRST. In 6800 systems the reset switch should be connected to the motherboard at CA-1. In 6809 systems the reset switch connects directly to a matching connector on the GIMIX 6809 CPU board and CA-1 is not used. The connectors are polarized to prevent improper installation. Figure o of the switch and jumper drawing shows the pinouts for CA-1

PILOT LIGHT CONNECTOR CA-2

CA-2 provides power and ground connections for the LED power indicator on the front panel of GIMIX systems. Figure P of the switch and jumper drawing shows the pinouts of CA-2.

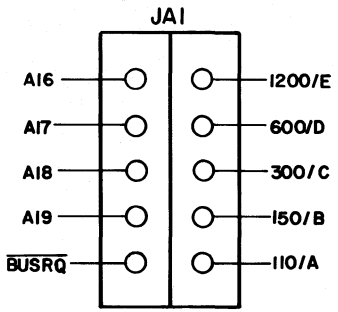
SS-50 BUS DESIGNATIONS

SS-50	GIMIX	SS-50C
D0	D0	D0
D1	D1	D1
D2	D2	D2
D3	D3	D3
D4	D4	D4
D5	D5	D5
D6	D6	D6
D7	D7	D7
A15	A15	A15
A14	A14	A14
A13	A13	A13
A12	A12	A12
A11	A11	A11
A10	A10	A10
A9	A9	A9
A8	A8	A8
A7	A7	A7
A6	A6	A6
A5	A5	A5
A4	A4	A4
A3	A3	A3
A2	A2	A2
A1	A1	A1
A0	A0	A0
GND	GND	GND
GND	GND	GND
GND	GND	GND
+8V	+8V	+8V
+8V	+8V	+8V
+8V	+8V	+8V
-12	-16	-16
+12	+16	+16
INDEX	INDEX	INDEX
MRST	MRDY	MRDY
NMI	NMI/BUSY	BUSY
IRQ	IRQ	IRQ
UD2	FIRQ	FIRQ
UD1	Q	Q
02	E	E
VMA	VMA	VMA
R/W	R/W	R/W
RESET	RESET	RESET
BA	BA	BA
01	BS	BS
HALT	HALT	HALT
110b	BUSRQ	BUSRQ or 110b
150b	S3/A19	9600b or S3
300b	S2/A18	300b or S2
600b	S1/A17	4800b or S1
1200b	S0/A16	1200b or S0

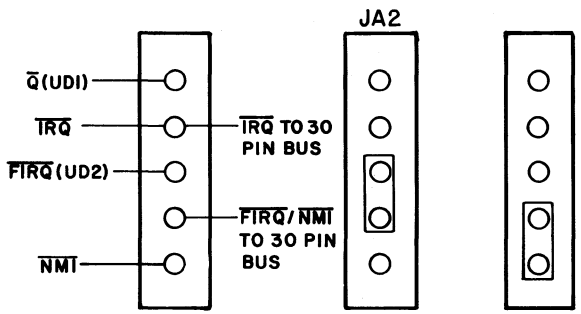
SS-30	GIMIX	SS-30C
UD3	RS2	RS2
UD4	RS3	RS3
-12	-16	-16
+12	+16	+16
GND	GND	GND
GND	GND	GND
INDEX	INDEX	INDEX
NMI	FIRQ/NMI	FIRQ
IRQ	IRQ	IRQ
RS0	RS0	RS0
RS1	RS1	RS1
D0	D0	D0
D1	D1	D1
D2	D2	D2
D3	D3	D3
D4	D4	D4
D5	D5	D5
D6	D6	D6
D7	D7	D7
02	E	E
R/W	R/W	R/W
+8V	+8V	+8V
+8V	+8V	+8V
1200b	1200b/E	1200b
600b	600b/D	4800b
300b	300b/C	300b
150b	150b/B	9600b
110b	110b/A	110b
RESET	RESET	RESET
I/O SEL	CS	I/O SEL

NOTE: THIS CHART DOES NOT INDICATE THE POLARITY OF THE SIGNALS. IT IS ONLY A COMPARISON OF THEIR NAMES.

THE NAMES IN THE "GIMIX" COLUMN REFLECT THE DESIGNATIONS THAT APPEAR ON THE MOTHER BOARD ITSELF AND IN THE DOCUMENTATION. THE ACTUAL SIGNALS AT SOME OF THE PINS DEPENDS ON THE JUMPER CONFIGURATION OF THE BOARD AND THE PARTICULAR CPU CARD INSTALLED.



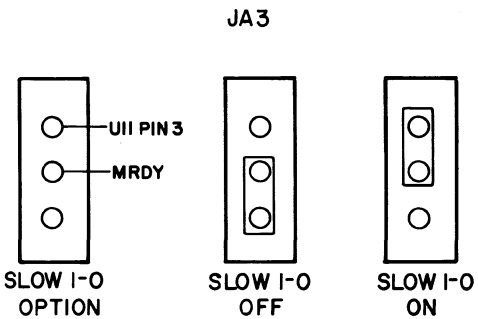
50 PIN TO 30 PIN BUS
BAUD RATE OPTION
FIG. A



INTERUPT OPTION
UDI/UD2 CONNECTIONS
FIG. B

FIRQ TO 30 PIN BUS
FIG. C

NMI TO 30 PIN BUS
FIG. D

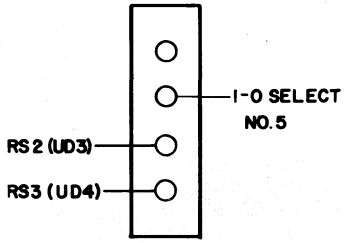


SLOW I-O OPTION
FIG. E

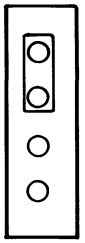
SLOW I-O OFF
FIG. F

SLOW I-O ON
FIG. G

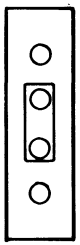
JA 5



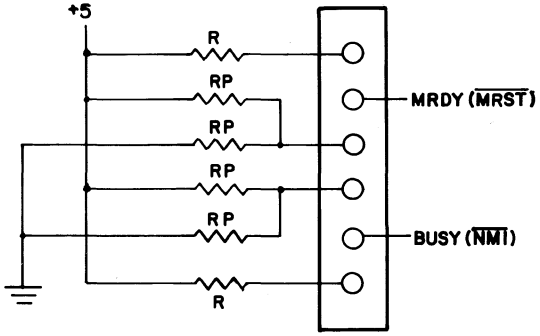
PIO DISC OPTION
UD3/UD4 CONNECTIONS
FIG. H



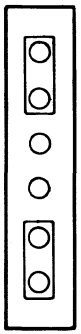
PIO DISC DISABLED
(ONLY REQUIRED WHEN USING 4 ADDRESSES PER I-O SLOT)
FIG. I



PIO DISC ENABLED
FIG. J



TERMINATION OPTIONS
FIG. K



NORMAL FOR GIMIX
6800/6809 CPU BOARDS
FIG. L

DIP SWITCHES

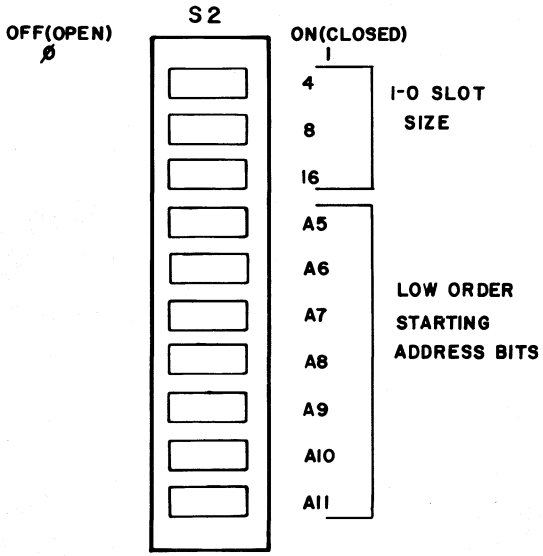


FIG. M

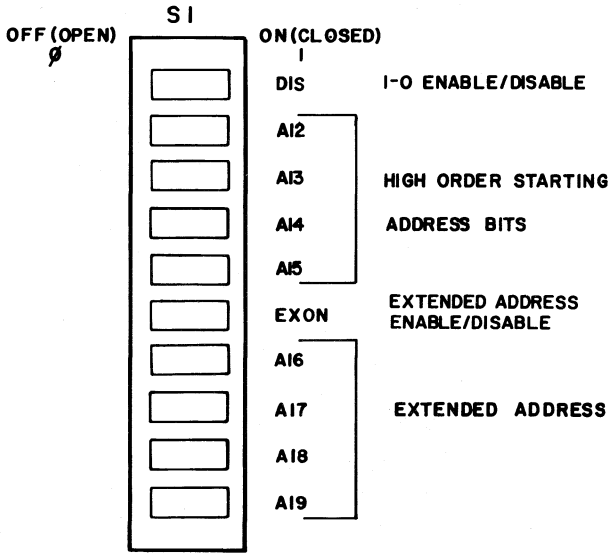
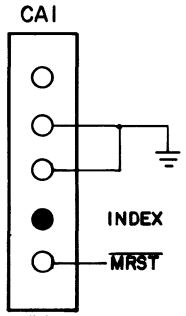
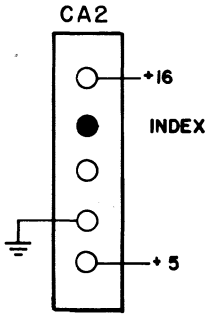


FIG. N



MASTER RESET
CONNECTOR FOR 6800
FIG. O



PILOT LIGHT
CONNECTOR
FIG. P

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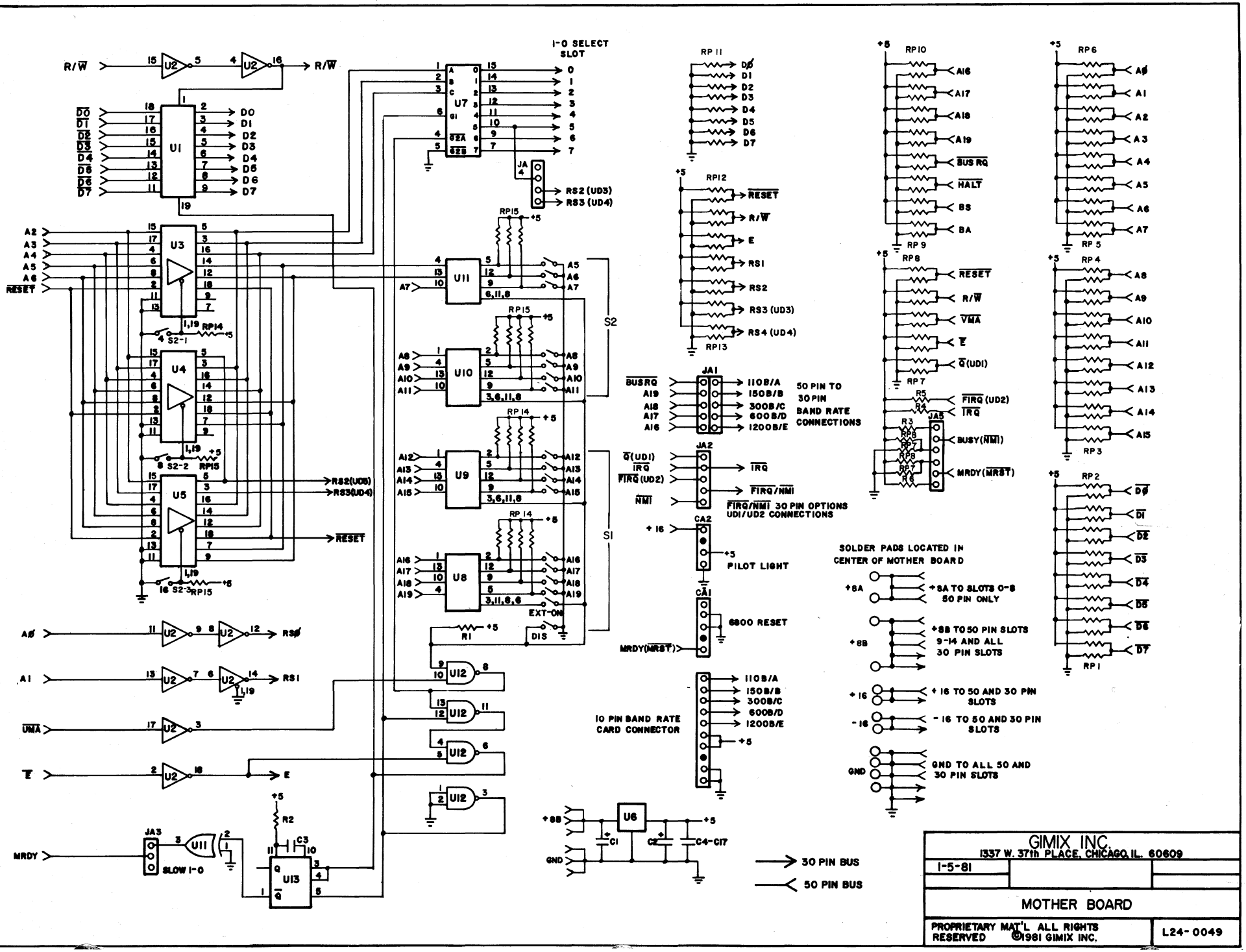
JUMPER OPTIONS & DIP SWITCHES		C24-0049


I-O SELECT SLOT
R/W
U1
U2
U3
U4
U5
U7
U8
U9
U10
U11
U12
U13
RESET
E
VMA
MRDY
SLOW I-O
RS2(UD3)
RS3(UD4)
S2
S1
EXT-ON
DIS
JA1
JA2
JA3
JA4
JA5
50 PIN TO 30 PIN BAUD RATE CONNECTIONS
110B/A
150B/B
300B/C
600B/D
1200B/E
FIRQ/NMI 30 PIN OPTIONS UDI/UD2 CONNECTIONS
PILOT LIGHT
6800 RESET
10 PIN BAND RATE CARD CONNECTOR
SOLDER PADS LOCATED IN CENTER OF MOTHER BOARD
+8A TO SLOTS 0-8 50 PIN ONLY
+8B TO 50 PIN SLOTS 9-14 AND ALL 30 PIN SLOTS
+16 TO 50 AND 30 PIN SLOTS
-16 TO 50 AND 30 PIN SLOTS
GND TO ALL 50 AND 30 PIN SLOTS
30 PIN BUS
50 PIN BUS
GIMIX INC.
1337 W. 37th PLACE, CHICAGO IL. 60609
1-5-81
MOTHER BOARD
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GIMIX BAUD RATE GENERATOR BOARD

This board is a companion board to the GIMIX 6800/6809 mother board. It plugs into a special 10 pin slot on the motherboard to provide Baud rate clocks for serial I/O interfaces. It can also be adapted for use in other systems that need a baud rate generator.

FEATURES

* 11 standard baud rates from 75 to 38.4K
* Easy jumper selection of baud rates
* Fully buffered output
* Provisions for software baud rate select controlled by the output of an external parallel port

JUMPER OPTIONS

BAUD RATE GROUP SELECT JA-1

The MC14411 can be programmed to provide one of four groups of output frequencys by applying the proper voltage levels to its RATE SELECT (A) and RATE SELECT (B) inputs.. Jumper area JA-1 is used to program the MC14411 for the desired group. The RATE SELECT (B) input is normally tied HIGH (1) by a PC board trace and jumper blocks are used to tie RATE SELECT INPUT (A) either LOW (0) or HIGH (1) to select either the LOW GROUP or the HIGH GROUP . See the MC14411 data sheet for more information. The following table shows the baud rates available at the BAUD RATE SELECT JUMPERS when either group is selected.

JUMPER POSITION	LOW GROUP	HIGH GROUP
X	*	*
75	75	300
110	110	440
150	150	600
300	300	1200
600	600	2400
1200	1200	4800
2400	2400	9600
4800	4800	19.2K
9600	9600	38.4K

* The baud rate on this line is determined by the software select option.

NOTE: All references to baud rates assume a serial interface that requires a 16X baud rate clock. The actual clock frequency generated is 16 times the figure shown for baud rate.

To select the LOW GROUP jumper pad (A) to (G) at JA-1. To select the HIGH GROUP jumper (A) to (+5).

BAUD RATE SELECT JUMPERS

Five double rows of jumper pins are used to connect the desired baud rate to the baud rate lines of the bus. These strips; labeled A, B, C, D, and E, correspond to the 110, 150, 300, 600, and 1200 baud lines on the bus respectively. The following example illustrates some sample jumper connections:

	A	B	C	D	E
X	***	. .	. .	. .	. .
75	. .	. .	. .	. .	. .
110	. .	. .	. .	. .	. .
150	. .	. .	. .	. .	. .
300	. .	. .	***	. .	. .
600	. .	. .	. .	. .	. .
1200	. .	. .	. .	. .	***
2400	. .	. .	. .	. .	. .
4800	. .	. .	. .	. .	. .
9600	. .	***	. .	. .	. .

*** = jumper installed

In the above example the following baud rates are selected; assuming the LOW GROUP is selected at JA-1. If the HIGH GROUP is selected the baud rates shown below are multiplied by 4; 9600 baud becomes 38.4K etc.

BUS LINE	BAUD RATE
110(A)	SOFTWARE SELECT
150(B)	9600
300(C)	300
600(D)	NONE
1200(E)	1200

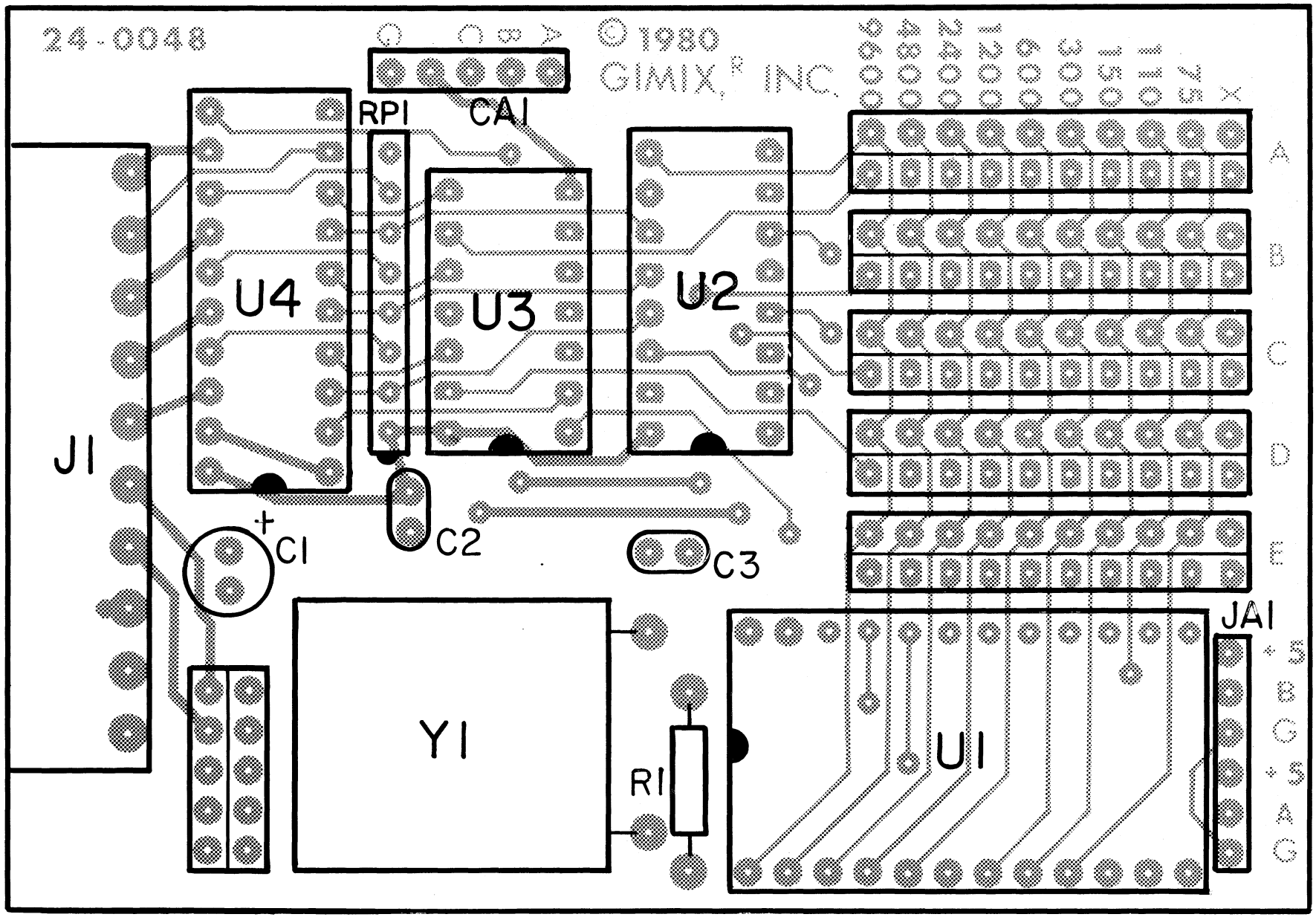
SOFTWARE BAUD RATE SELECT

The board can be connected to the output of an external parallel port to permit software selection of baud rates. The software selected rate is available at the jumpers labeled X and can be connected to any of the baud rate lines on the bus.

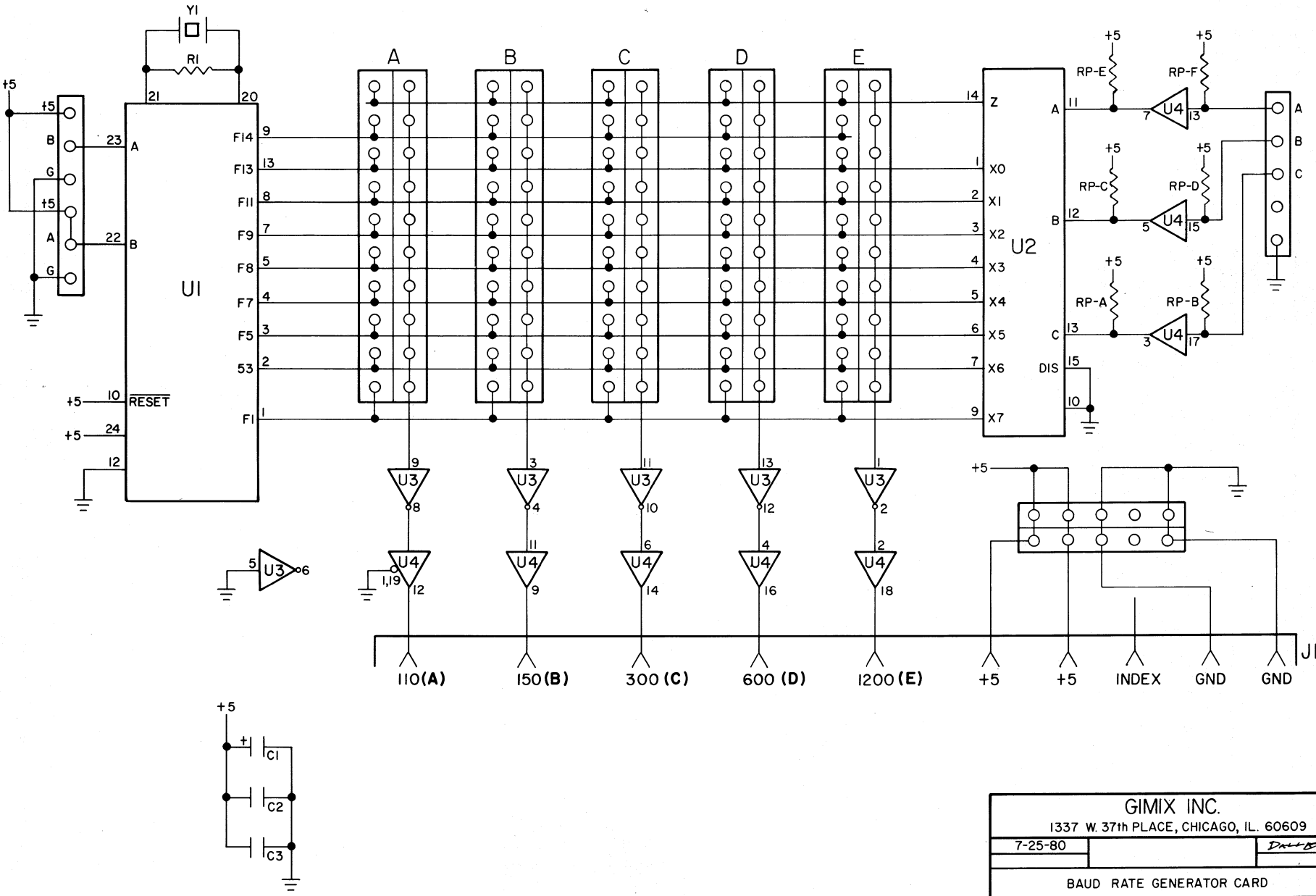
The 3 input lines for software selection are available at the connector CA-1. These are LS TTL inputs and the binary data placed on the lines selects 1 of 8 possible baud rates. The line labeled "A" is the least significant, and "C" is the most significant bit.

Any of the 8 fastest baud rates, 110 through 9600 if the LOW GROUP or 440 through 38.4K if the HIGH GROUP is selected, can be software selected. The baud rates are selected sequentially with "000" on the select inputs selecting the slowest rate and "111" selecting the fastest.

The select inputs do not latch the input data. Any time the input data changes the baud rate will change.



COMPONENT LAYOUT



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7-25-80		
BAUD RATE GENERATOR CARD		
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GIMIX MISSING-CYCLE DETECTOR BOARD

The GIMIX MISSING-CYCLE DETECTOR is designed to monitor the AC power line and generate and interrupt when a power failure occurs. It can be used in conjunction with battery back-up RAM memory, such as the GIMIX 64K byte CMOS STATIC RAM BOARD W/BATTERY BACK-UP and the battery back-up scratchpad RAM option on the GIMIX 6809 PLUS CPU BOARD, in systems where data loss due to power failure cannot be tolerated.

FEATURES

* Input connects directly to the 115 V. AC line
* High voltage input/output isolation (7500 V.)
* Open collector output drives bus interrupt lines directly
* Totem-pole output drives standard TTL loads
* On board voltage regulation (requires +8 VDC from system)

INSTALLATION

The board can be installed in any convenient location in the system using the double-face tape provided. The suggested location for GIMIX mainframes is just in front of the power transfomer and bridge rectifier, with the input side (orange leads) facing the right side of the cabinet. Remove the protective backing from the tape and carefully press the board into place at the chosen location.

CONNECTIONS

AC CONNECTIONS

For most applications the board should be connected in parallel with the power transformer primary so that interrupt/powerfail outputs will be generated whenever the system is turned off or the AC power fails. The AC input leads (orange) are provided with ¼" QC (quick connect) terminals and "Y" adapters for connection to the primary of the GIMIX power transformer. Before making any connections to the AC input BE SURE THAT THE COMPUTER POWER CORD IS UNPLUGED, either at the back of the cabinet or at the wall outlet, to prevent shock hazard and possible damage to the computer.

Carefully disconnect the QC terminals from the power transformer, and install one of the "Y" adapters on each of the transformer terminals. Reconnect the two wires from the cabinet wiring harness, one to each of the "Y" adapters, and connect the AC leads (orange) from the missing cycle detector to the remaining terminals of the "Y" adapters. Be sure that the QC terminals and "Y" adapters do not touch each other or the cabinet.

DC CONNECTIONS

The DC input to the board (red lead) should be connected to the same +8VDC source that powers rest of the system. In GIMIX mainframes and systems the red lead should be connected to one of the red +8VDC terminals of the barrier block on the power supply filter board.

The DC/signal ground (black lead) should be connected to the system ground at a point as close as practical to the point(s) on the circuit board, usually the motherboard or an I/O board, where the signal output (gray and/or violet) leads are connected. In many applications this lead will be soldered directly to the circuit board. Consult the documentation for the board chosen to determine the location of a convenient ground point.

SIGNAL OUTPUT

The board has two separate outputs leads, violet and gray. The violet lead is an open collector output that can be connected directly to any one of the 50 or 30 pin bus interrupt lines; NMI, IRQ, or FIRQ. See the motherboard documentation for the locations of external connection points for these bus lines. The gray lead is a totem-pole output that will drive a standard "TTL" logic input. This output, if used, would normally be be connected to the input of a parallel interface. If only one output is used the unused output lead should be insulated and stored carefully to prevent accidental contact with other parts of the system.

Both are active low outputs, when a power failure is detected the the open collector output (violet) will pull the line it is connected to low, generating an interrupt, and the totem-pole output (gray) will switch to a "TTL" low (0) level.

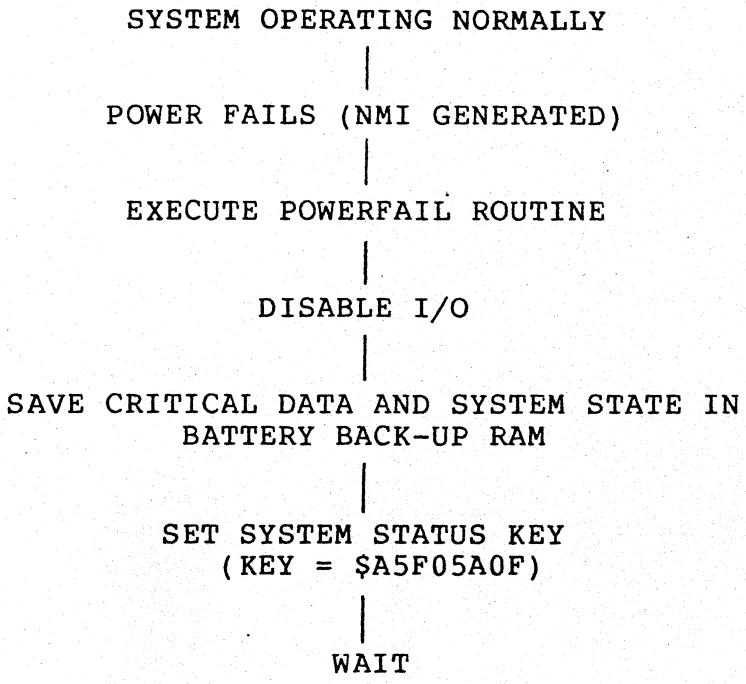
The choice of output connections depends entirely on the application and the user-written powerfail software. It is beyond the scope of this manual to list all of the possible configurations; however, the following section gives some general suggestions for using the GIMIX MISSING CYCLE DETECTOR.

APPLICATION SUGGESTIONS

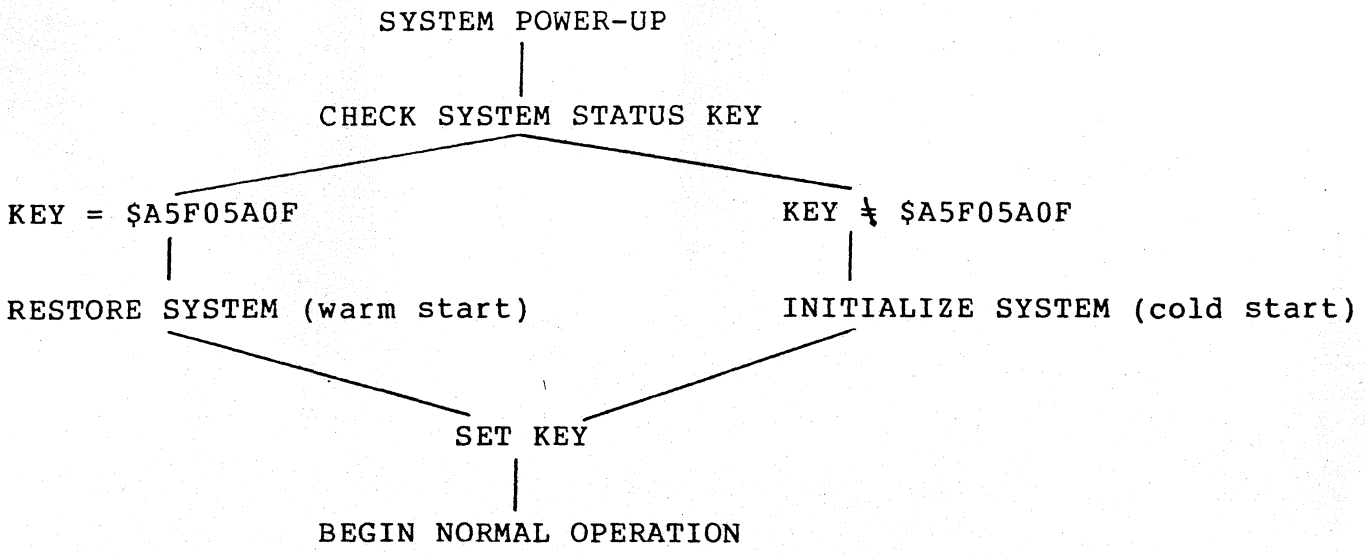
In many applications it is desirable to provide some type of tolerance to power failure. Critical data and the system status must be preserved so that when power is restored the system can be returned, as nearly as possible, to its original state. The GIMIX 64K CMOS RAM BOARD W/BATTERY BACK-UP and the battery back-up RAM option on the GIMIX 6809 PLUS CPU BOARD provide a means for data retention when system power is lost. Both of these boards also have circuitry that prevents unintentional alteration of data when the power supply output falls below safe levels. When AC power is lost, a certain amount of time elapses before the power supply output voltages fall below safe levels. This time can be used to prepare the system for power failure. The amount of time available depends mainly on the power supply capacity and system loading (number and type of boards installed), and can best be determined for a particular system by using a program (see the sample program) to measure the actual time between loss of AC power (MISSING CYCLE DETECTOR generates an interrupt) and system shut down (bus voltage falls below safe levels).

The AC input to the board is rectified and used to drive the opto-isolator, U-2. The output of the opto-isolator keeps the timing circuit, (U-3, C-3, etc.) reset, as long as the AC input is present. If the AC input falls below approximately 40 Volts the opto turns off and C-3 begins to charge. If the AC input remains off (below 40 V) for longer than 7 +/- 1 milliseconds the timing circuit times out and the outputs (IRQ/NMI and POWER FAIL) go low indicating a power failure. The 40 Volt turn-off threshold was chosen to match the characteristics of the ferro-resonant power transformer in the GIMIX mainframe. In systems without ferro-resonant supplies, the 40 Volt threshold may be too low to permit proper operation of the MISSING CYCLE DETECTOR.

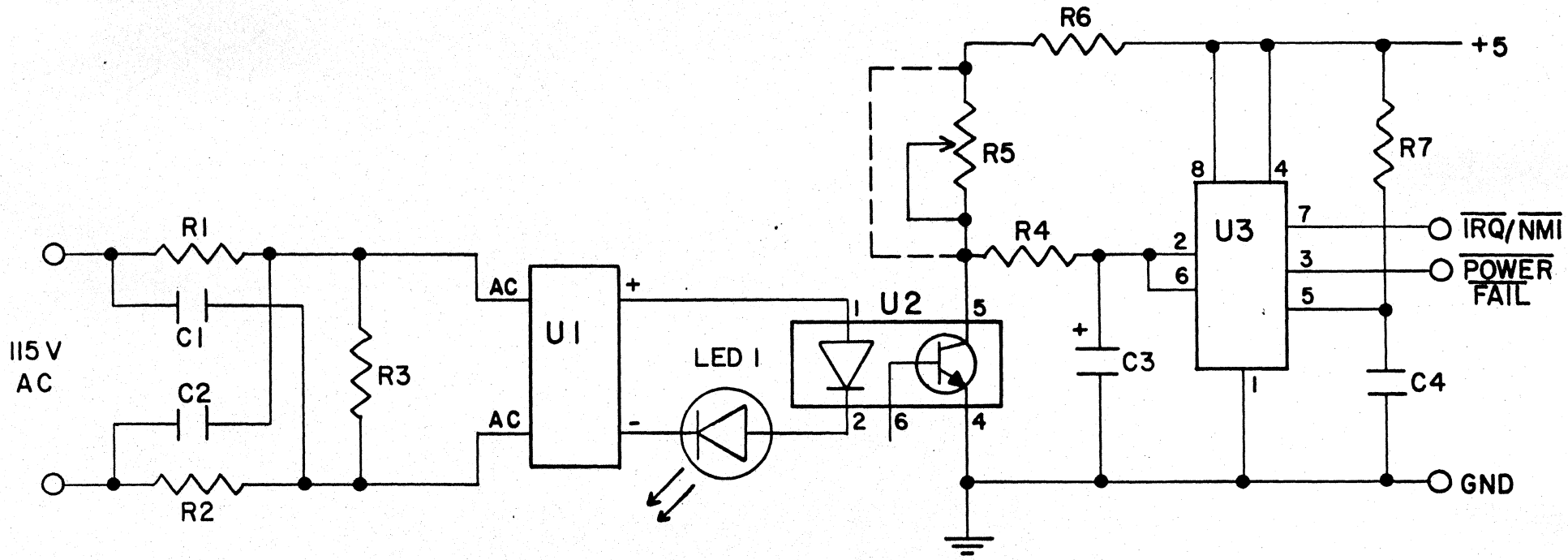
Assuming that the MISSING CYCLE DETECTOR is setup to generate an NMI (non-maskable interrupt) the following sequence could be used to handle power failure:

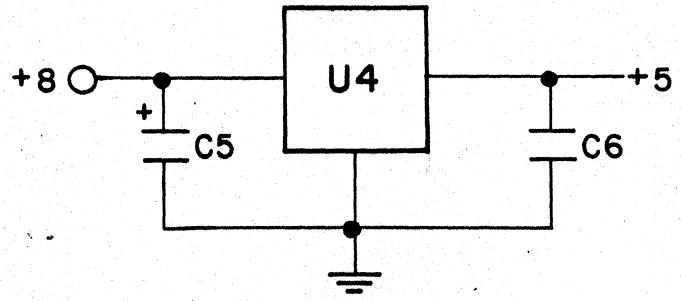


The system status key is an optional feature that would allow the software to determine the status of the system prior to the power failure. It could also be used to determine the proper restoration (reset) sequence to execute on power up as shown below. The key could be a sequence of four bytes, such as $A5F05A0F, stored in battery back-up RAM. There is virtually no chance of a sequence of this type occuring randomly in memory from a complete cold start.



Under certain conditions it is possible, if the power fails and then returns to normal before the bus voltages have fallen below safe levels and shut the memory and CPU down, for a second interrupt to occur while the system is in the "wait" portion of the powerfail sequence. Since the NMI cannot be masked, this would cause the powerfail sequence to be executed a second time. This may be undesirable in certain situations and may be prevented by reseting the NMI vector to point to another routine or simply an RTI instruction as part of the powerfail sequence. A momentary power failure of this type would also cause the system to "wait" until manually reset. This could be prevented by connecting the second output of the MISSING CYCLE DETECTOR to an input port and polling this port during the "wait" portion of the powerfail sequence to determine if power has been restored during the execution of the powerfail sequence.





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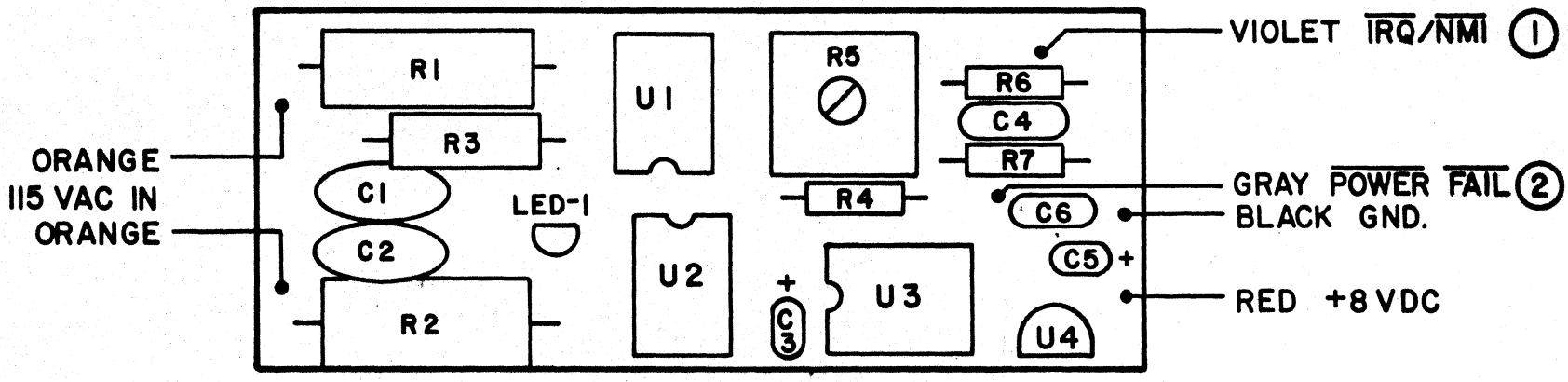
MISSING CYCLE DETECTOR

L24-0054



NOTES:

(1) OPEN COLLECTOR OUTPUT

(2) TOTEM-POLE TTL OUTPUT

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5-20-81	COMPONENT LAYOUT	
MISSING CYCLE DETECTOR		
		F24-0054

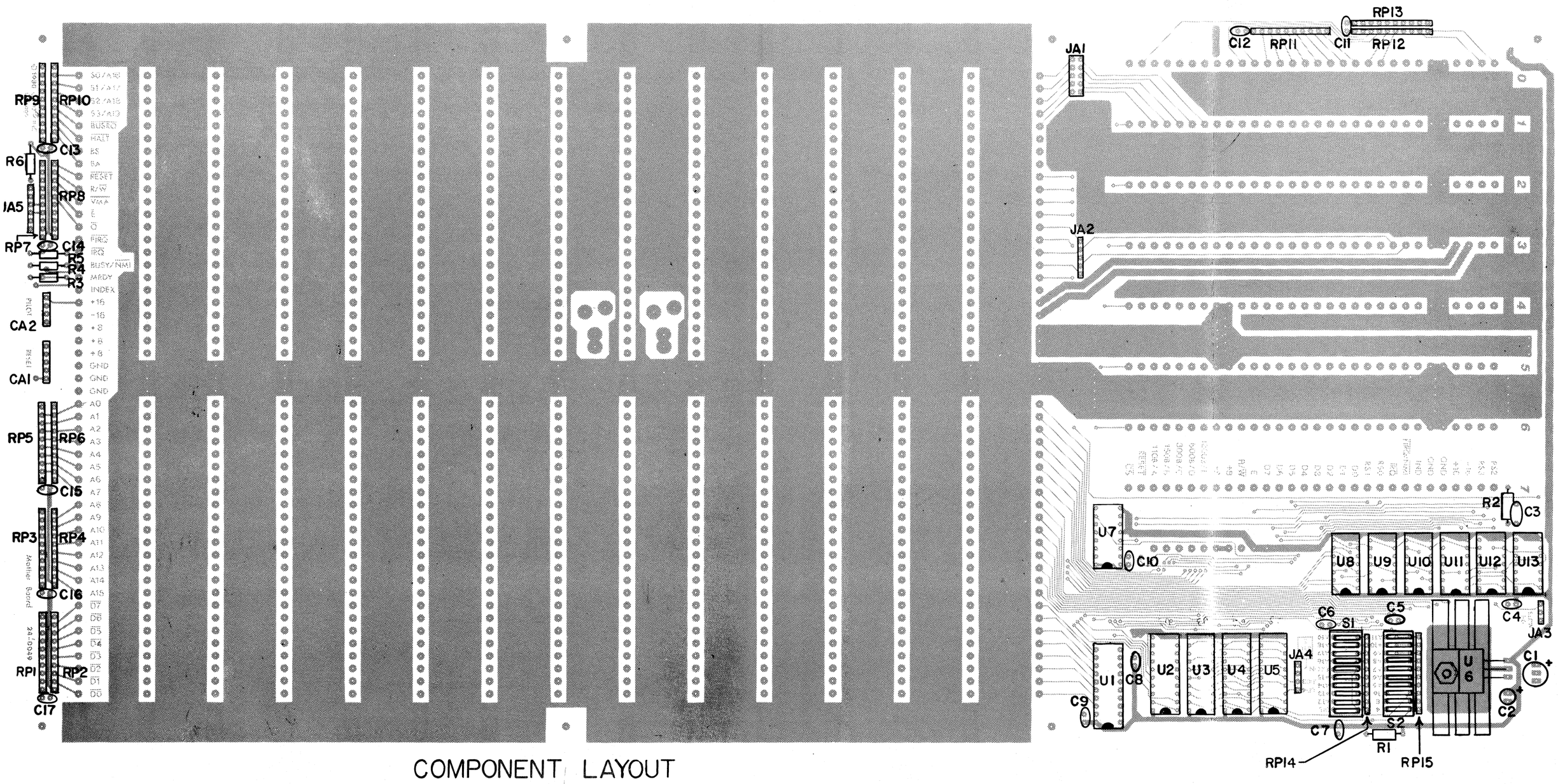
```
                        *  CYCLETST
                        *
                        *  THIS PROGRAM IS USED TO DETERMINE THE AMOUNT OF TIME
                        *  (IN MACHINE CYCLES) AVAILABLE BETWEEN DETECTION OF
                        *  A POWER FAILURE (NMI GENERATED) AND SYSTEM SHUTDOWN
                        *  (UNSAFE VOLTAGE THRESHOLD CIRCUITS ON GIMIX 6809
                        *  CPU and/or 64K RAM ACTIVATE).
                        *
                        *  THE GIMIX MISSING CYCLE DETECTOR MUST BE CONNECTED
                        *  TO THE NMI LINE AND ANY OTHER DEVICES THAT GENERATE
                        *  AN NMI MUST BE DISABLED. THE CPU MUST BE JUMPERED
                        *  TO ENABLE THE NMI.
                        *
                        *  THIS PROGRAM SHOULD BE LOADED INTO BATTERY BACK-UP
                        *  RAM (OR PROM).
                        *
                        *  TO START THIS PROGRAM JUMP TO LOCATION 'START1'
                        *  AND THEN TURN THE POWER OFF.  TURN THE POWER ON
                        *  AND JUMP TO LOCATION 'START2' TO PRINT THE NUMBER
                        *  OF CYCLES EXECUTED.
                        *
                        *  THIS PROGRAM IS POSITION INDEPENDANT AND ROMMABLE.
                        *  TO ROM THIS PROGRAM MOVE THE DATA AREA TO SOMEWHERE
                        *  IN THE BATTERY BACKED UP RAM AND RE-ASSEMBLE IT.
                        *
                        *
                        *  GMXBUG-09 EQUATES
                        *
                F80C    PDATA   EQU     $F80C       OUTPUT STRING
                F81A    PBYTE   EQU     $F81A       PRINT BYTE IN HEX
                E40A    NMIVEC  EQU     $E40A       GMXBUG-09 NMI VECTOR
                F80E    PCRLF   EQU     $F80E       PRINT CR/LF
                F802    NXTCMD  EQU     $F802       MONITOR WARM START
                        *
                        *  TWO BYTES FOR COUNTER
                        *
0000                            ORG     $0
0000                    COUNT   RMB     2
                        *
                        *  START OF COUNT ROUTINE
                        *
0100                            ORG     $100
0100 CC   0000          START1  LDD     #0          INITIALIZE THE COUNTER
0103 FD   0000                  STD     COUNT
0106 30   8D 0005               LEAX    NMI,PCR     POINT TO NMI HANDLER
010A BF   E40A                  STX     NMIVEC      STORE IN VECTOR ADDRESS
010D 20   FE            LOOP1   BRA     LOOP1       LOOP TILL NMI
                        *
                        *  ACTUAL NMI HANDLER AND COUNTER
                        *  THE TOTAL LENGTH OF THIS LOOP IS
                        *  100 MACHINE CYCLES.
                        *
```

```
010F BE   0000      NMI     LDX    COUNT     GET COUNT
0112 30   01                LEAX   1,X       INCREMENT IT
0114 BF   0000              STX    COUNT     STORE IT BACK
0117 C6   2E                LDB    #46       NUMBER OF TIMES THROUGH LOOP
0119 5A             LOOP2   DECB              DECREMENT COUNTER
011A 26   FD                BNE    LOOP2     LOOP TILL ZERO
011C 48                     ASLA              MAKE IT EVEN
011D 48                     ASLA              MAKE IT EVEN
011E 20   EF                BRA    NMI       LOOP AGAIN
                    *
                    *  THIS IS THE ROUTINE THAT PRINTS THE NUMBER
                    *  OF MACHINE CYCLES ACTUALLY EXECUTED
                    *
0120 AD   9F F80E   START2  JSR    [PCRLF]   PRINT CR/LF
0124 B6   0000             LDA    COUNT     GET MS BYTE
0127 AD   9F F81A          JSR    [PBYTE]   PRINT IT
012B B6   0001             LDA    COUNT+1   GET LS BYTE
012E AD   9F F81A          JSR    [PBYTE]   PRINT IT
0132 30   8D 0008          LEAX   MSG,PCR   POINT TO MESSAGE
0136 AD   9F F80C          JSR    [PDATA]   PRINT IT
013A 6E   9F F802          JMP    [NXTCMD]  RETURN TO MONITOR
                    *
                    *  MESSAGE
                    *
013E 30 30 20 43   MSG     FCC    /00 CYCLES EXECUTED AFTER THE NMI/
015E 04                    FCB    4
                           END    START1
```

0 ERROR(S) DETECTED

SYMBOL TABLE:

```
COUNT   0000   LOOP1   010D   LOOP2   0119   MSG     013E   NMI     010F
NMIVEC  E40A   NXTCMD  F802   PBYTE   F81A   PCRLF   F80E   PDATA   F80C
START1  0100   START2  0120
```



COMPONENT LAYOUT