SERVICE MANUAL

FRIDEN MODEL 1155
ADVANCED PROGRAMMABLE CALCULATOR

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SINGER
BUSINESS MACHINES
2350 WASHINGTON AVE.
SAN LEANDRO, CALIF. 94577

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SECTION 1

GENERAL DESCRIPTION

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1-1.0 GENERAL

The Friden* programmable printing calculator model 1155 is a small, light weight, desk top calculator having a program capacity of 511 instruction steps, two working registers, and twenty data storage registers (each independent of program storage and working registers). Register capacity is 13-digits with a 2-digit exponent, plus decimal point and sign. Its dynamic range is: 10^{-99} to 10^{99}. A plug-in magnetic card reader/recorder, reads and/or writes two 511 step programs. Provision is also made for plugging in an X-Y plotter.

The printed tape output is accomplished by a small compact single print wheel, helical printer under control of the 1155 logic. A description of the printer is covered in the following paragraphs.

For a description of the operating keys and machine functions, refer to the 1155 "Operator's Primer", publication #55-537. Also, refer to the 1155 Reference Manual, publication #55-538.

1-1.1 PHYSICAL CHARACTERISTICS

Size: 15-1/2" wide, 21-1/2" long, 8-1/4" high.
8-1/2" wide, 9-1/2" long, 4-1/4" high (card reader)

Weight: 42 pounds
5 pounds (card reader)

1-2.0 FUNCTIONAL DESCRIPTION OF PRINTER

The single print wheel helical printer used as the output mechanism for the 1155 programmable calculator operates under control of the 1155 logic to provide a printed tape output. The following is a functional description of the printer unit including mechanical operation and electrical actions.

1-2.1 POWER

The printer motor is turned on via 1155 logic when a print cycle is required, and the motor is turned off soon after the print cycle has ended, unless a new print cycle is called for immediately following the preceding print cycle. The printer motor supplies the driving power to the mechanical elements of the printer. Heat from the motor is dissipated by means of an air jet from a fan blade mounted on the motor shaft. A plastic shield covers the fan and provides an air passage to the motor.

1-2.2 PRINTING

Print speed is approximately 47 characters per second, utilizing a 30 character print wheel. Print action is from right to left, with symbols being printed first and then the digits, starting with the least significant digit (LSD).

A single line print can contain up to 15 digits, a decimal point, two symbols, and up to four spaces between high order digits to represent thousands. Character spacing is 10 to the inch and line spacing is 6 to the inch.

*A trademark of The Singer Company

1-2.2 PRINTING (Cont.)

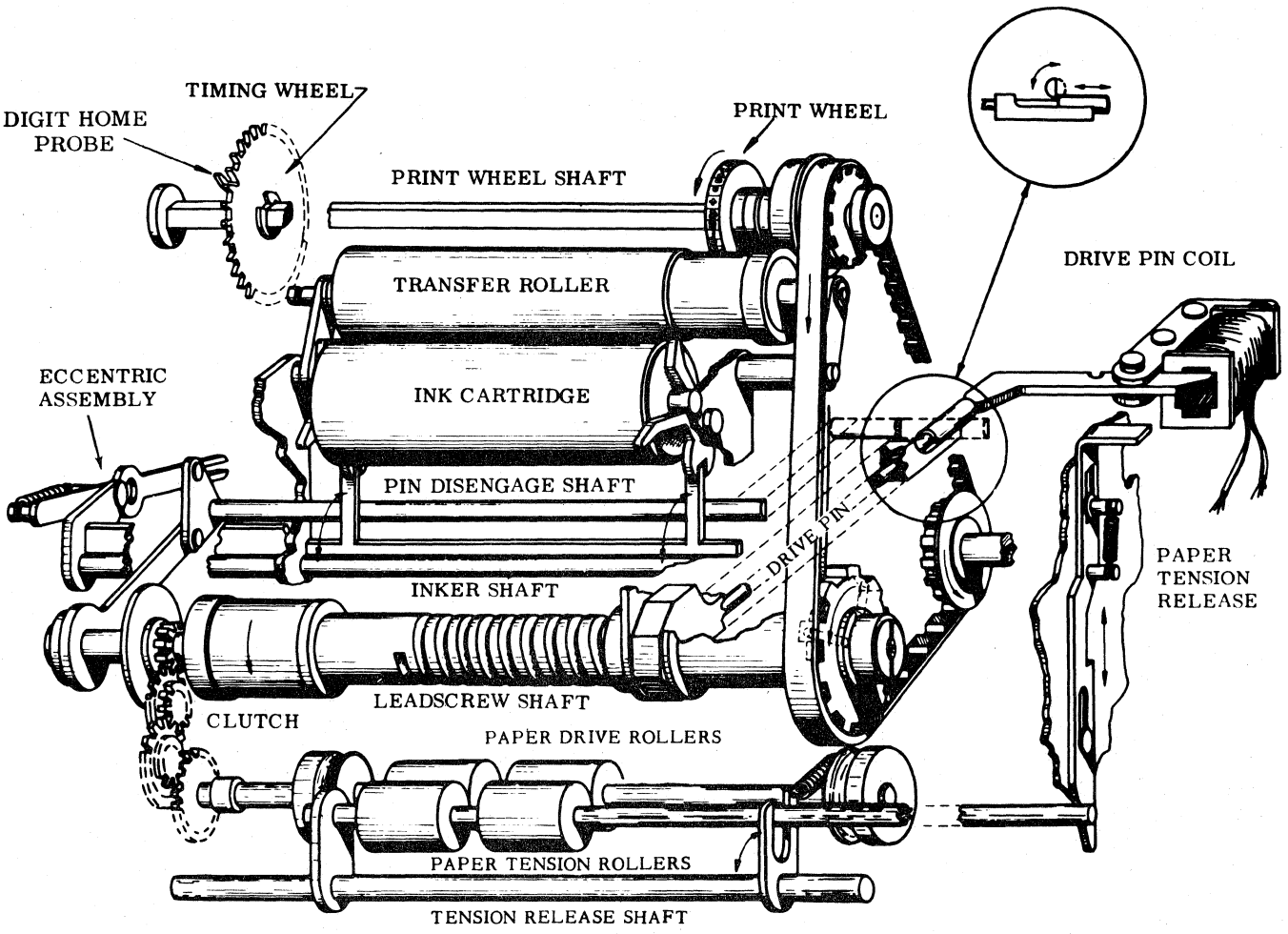


FIGURE 1-1

1-2.2 PRINTING (Cont.)

ZERO SUPPRESSION. All zeros before the most significant digit of the number are suppressed. This is accomplished by ending printing with the leftmost digit (MSD) of the number. This means that the print lines will be of varying length depending on the digit length of the number. However, this increases the functional printing speed since shorter numbers make for a shorter total print cycle time.

PAPER FEED. Paper feed is automatic between each line print cycle. Inserting a new roll of paper is a simple operation. All that an operator need do is open the new roll, make a smooth straight starting edge, and place the roll in the paper cradle. Then, depress "Paper Advance" and the paper automatically threads into position for printing.

TEAR-OFF. A Tear-off knife is provided for easy tear-off of tape portions. Also, a Paper Release lever frees the paper so that it can be pulled up incident to tear-off.

INKING. The ink is supplied by a large capacity, porous ink roller which supplies ink only at the end of a print cycle. By limiting ink transfer to a short portion of the cycle, excessive ink build-up is eliminated and longer ink supply established. The ink roller is supplied as a unit which is easily installed without soiling the fingers.

CHARACTER PRINT. The helical printer features a continually moving carriage and a continually rotating print wheel during a print cycle. The helical print wheel carriage, and hammer carriage travel along the writing line by means of a pin engaged in a helix screw shaft. The print wheel travels along the square print wheel shaft under the influence of a yoke which is attached to the print wheel carriage. Exact alignment between the two carriages is achieved by use of a "U" shaped coupling bail. The print wheel shaft and the helix shaft are driven by a cog belt, coupled to the motor pulley.

Printing is accomplished "on the fly" by actuation of an electronically timed hammer which strikes the back of the paper, causing the paper to be pressed against the inked print wheel at the time the desired character is in in position. Even though the print wheel is rotating as well as moving from left to right, the hammer impact time is so short that the character is printed clearly and legibly. The constant movement of the print wheel when engaged with the helix screw shaft is compensated by the helix arrangement of the characters on the print wheel.

Strobe signals from the timing wheel on the end of the print wheel shaft are used to identify the starting "home" point, and the position of each character on the print wheel.

The major components of the printer are shown in Figure 1-1.

1-2.3 PRINTER OUTPUTS

The printer supplies four outputs to the 1155 logic which are used to establish timing relations for print cycle control. These signals are: Carriage Home, Lead Screw Home, Digit Home, and Character pulses. The term "Home" when associated with a signal or mechanical action implies a beginning or starting point.

CARRIAGE HOME. In order to start a line-print cycle, the print hammer and print wheel carriages, which are coupled together, must be at the right margin at a position called "HOME". To identify this position in the logic, a signal is produced called Carriage Home. The signal is generated by means of a permanent magnet attached to the print hammer carriage. When the carriage is at the right margin in position to start a print cycle, this magnet closes a reed switch mounted on a PC board beneath the carriage, and produces the signal Carriage Home.

LEAD SCREW HOME. For optimum (best) start of the Hammer Carriage, the drive pin must engage the beginning of the Helix (Lead Screw) and always at the same point. To positively identify this point, a permanent magnet is mounted on the drive wheel of the helix shaft. This magnet is positioned to correspond to the drive-pin engagement point on the Helix. As this magnet rotates past a reed switch mounted on a PC board beneath the drive wheel, it closes the reed switch and produces the signal Lead Screw Home. This signal signifies to the logic that the Helix is in the correct position to receive the drive-pin. Since the Helix shaft is constantly rotating during a print cycle, a succession of Lead Screw Home signals is constantly being produced, each signifying one revolution of the Helix shaft. However, only one Lead Screw Home signal is used for each print cycle.

DIGIT HOME. On the timing wheel, at the left end of the print wheel shaft, is a probe which extends out from the left side of the timing wheel. As this probe passes a fixed electromagnet, a pulse is generated which is designated "Home" or Digit Home. This pulse is used in the logic along with the character pulses to identify the specif digit or symbol as it arrives in position to be printed.

CHARACTER PULSES. On the print wheel are a total of 30 characters (10 digits, decimal point, 3 symbols, and 16 alpha characters). On the circumference of the timing wheel are 30 points, each of which represents one of the characters. As these points pass an electromagnet, a series of pulses is produced, each one of which represents a character on the print wheel. For each revolution of the print wheel and timing wheel, there are 30 character pulses produced. These character pulses are used in the logic along with the Digit Home pulse to exactly identify the characters on the print wheel as they arrive in position to be printed.

1-2.4 PRINTER INPUTS

Control of the initiation of a line-print cycle, printing of the characters, and ending of the line-print cycle is by means of inputs to the printer from the logic. There are four inputs: Motor Start, Carriage Start, Hammer Drive, and Line Feed.

MOTOR START. The motor in the printer unit runs only when a line-print cycle is called for. Logic circuits provide this Motor Start signal at the time a print cycle is to occur. Soon after the end of the line-print cycle, the motor stops unless another print cycle is called for within about 1.5 seconds.

CARRIAGE START. The print hammer carriage moves to the left when the drive pin, which is part of the carriage, becomes engaged with the Helix screw. The drive pin is engaged via a signal from the logic which energizes an electromagnet. The armature linkage of the energized electromagnet drives the pin forward into the Helix screw. The drive pin engage signal can only result when Carriage Home, and Lead Screw Home signals are both valid in the logic. These signals together specify that the carriage is in home position and that the proper point on the Helix screw is in line with the drive pin.

HAMMER DRIVE. During the line print cycle, the logic calls for print action for specific symbols and digits. The actual printing occurs as a result of Hammer Drive signal from the logic that energizes an electromagnet. The armature of the electromagnet drives the hammer forward to strike the back of the paper at the time the desired character on the print wheel is in front of the paper.

LINE FEED. The line feed signal when received from the logic signifies the end of print action. When this signal is received, it energizes an electromagnet that releases a dog on the spring (capstan) clutch. When this dog is released, torque-spring action picks up the rotation of the Helix screw shaft and transfers it to an eccentric assembly. Rotation of this eccentric assembly, in turn, actuates Drive-pin disengagement, Paper feed for one line space, and ink transfer.

SECTION 2

LOGIC DESCRIPTION

SECTION CONTENTS

"T" TIME GENERATION

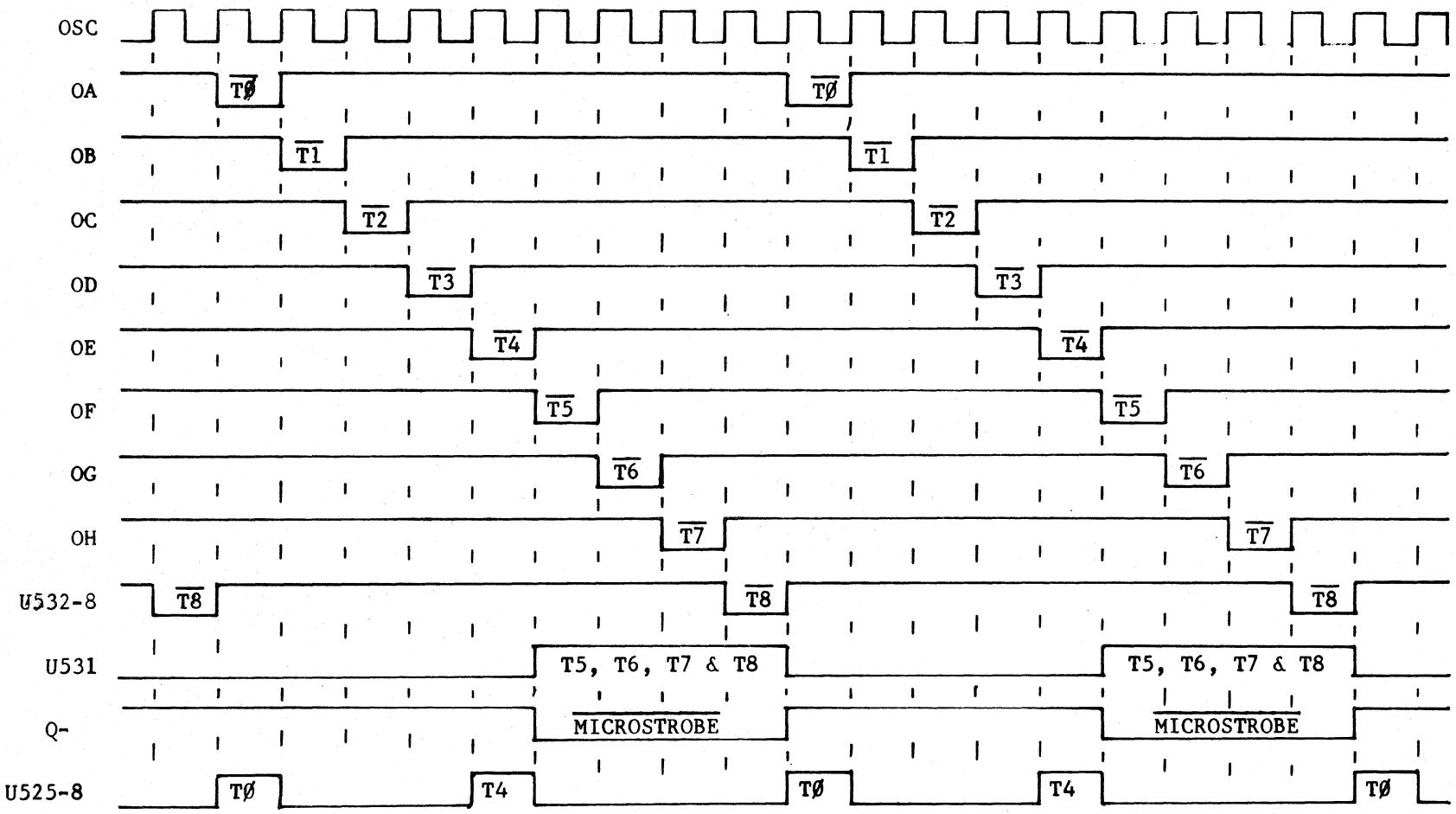


FIGURE 2-1

2-1.0 GENERAL

Functionally, the Friden 1155 Programmable Calculator operates like most electronic calculators, performing the four basic arithmetic operations of multiply, divide, add, and subtract, by use of storage and working registers, shift registers, timing clock circuitry, etc. Additionally, however, the 1155 contains 12 special arithmetic keys designed for use in higher mathematics. It also contains programming keys for storing a maximum of 512 program steps into its memory. A magnetic card reader/recorder is also supplied for the purpose of rapid entry of programs into the program storage area of the 1155, or for reading an existing program out of the 1155 memeory.

2-2.0 TIMING

Clock pulses called "T" times are used as the primary timing signals throughout the logic of the 1155 Calculator. These "T" times designated: $\overline{T\emptyset}$, $\overline{T1}$, $\overline{T2}$, $\overline{T3}$, $\overline{T4}$, $\overline{T5}$, $\overline{T6}$ and $\overline{T7}$ are the output signals from U528 (Board #5), Clock pulses designated T8 and $\overline{T8}$ are also generated via the output of flip flop U532.

Each "T" time is 400ns long. One complete timing cycle (9 "T" times) is 3.6usec. The signal $\overline{T8}$ occurs each 3.6 usec. The $\overline{T8}$ signal is used as the input to a binary counter on Board #1 designated U128, whose output is designated T400. The signal T400 goes to Board #4 (U426) and is used to develop the signal K1000(T400 and K1000 are the same time). The signal K1000 out of U426, pin 6 is applied to U122 (Z Counter) as its clock input. The generation of the "T" times is shown in the chart, Figure 2-1. Another timing chart, Figure 2-2 , shows the development of the T$\emptyset\emptyset$ and related Z times.

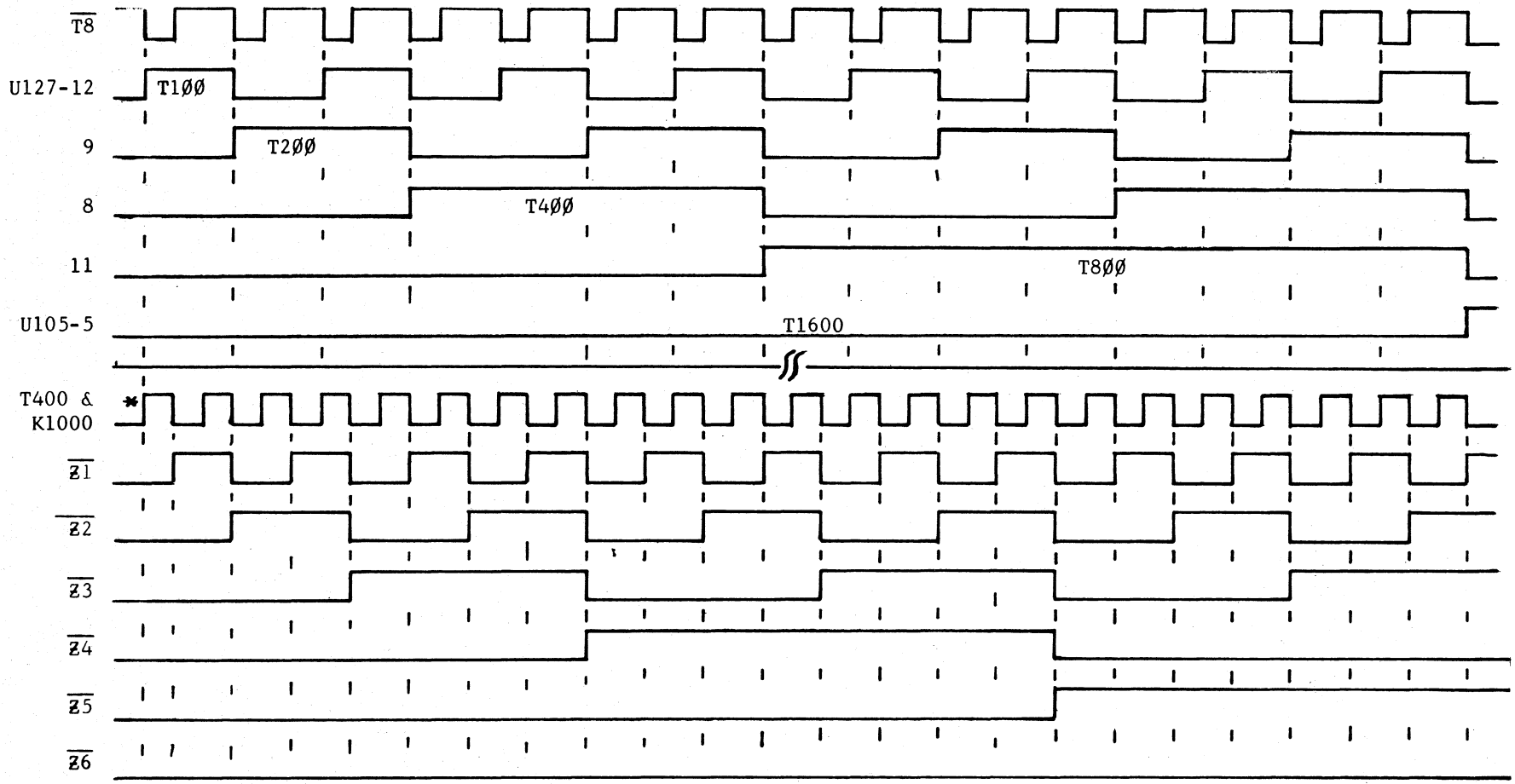
2-2.1 SHIFT REGISTER CLOCK PULSE GENERATOR

Two special chips (U109 and U110) with their associated discrete components provide the clock pulses for the shift registers. A data bit moves one position for each clock pulse to the shift register and there are two clock pulses for each "T" time cycle which means that the bits move through the shift register at the same rate as the Marker Counter counts, or twice for each "T" time cycle.

Inputs to the timing gates are the timing signals: $\overline{T1}$, $\overline{T6}$, $\overline{T8}$, and $\overline{T3}$. Also there is a cross coupled flip flop U117-11 and U117-8 tied to the Nand gate input of U109. When $\overline{T1}$ goes low, $\overline{T3}$ will be high and the output of gate U110 will go low, causing the junction of the 2.2K and the 470 ohm resistors to go to ground. The junction between the 2.2K and the 10K resistors will go low and when it does, the transistor Q2 will be saturated. Q2 being saturated will turn on the NPN transistor whose emitter goes to pin 9 and whose collector goes to pin 10. The collector of the upper NPN transistor will go to -12 volts and the lower NPN transistor will be turned off. The emitter of the lower NPN will go to -12 volts. The -12 volts is coupled as a negative going pulse and becomes $\Phi 2$ (phi 2) into pin 7 of each of the shift registers U101, U102, and U103. This signal ($\Phi 2$) occurs at $\overline{T1}$ time. The output signal $\Phi 1$ (phi 1) from U109 is developed in a similar manner as described for $\Phi 2$. Thus, the two output clock signals $\Phi 1$ and $\Phi 2$ going from +5volts to -12 volts will clock the shift registers.

The interrelationship of the shift register clock pulses and the marker counter is as follows: The Marker Counter is clocked at the end or trailing edge of T$\emptyset$ and T4 time and each time it is clocked, it remains at that count until the next T$\emptyset$ or T4 time. Then, during T1 through T3 and T5 through T6, the clock pulses ($\Phi 1$ and $\Phi 2$) are generated for the shift registers. Thus, the clock timing between the Marker Counter and the Shift Registers is closely related. That is, when we look at a time period in the Shift Register, we are also looking at a time period in the Marker Counter.

T1ØØ & Z COUNTER TIMING CHARTS



* K1ØØØ is the same signal as T4ØØ inverted twice. The last inversion is through a blocking gate. K1ØØØ may be blocked at this gate but T4ØØ runs as long as the oscillator is in operation.

FIGURE 2-2

2-3.0 SHIFT REGISTER OPERATION

The data that is being shifted through the shift registers consists of 6-bits of information. These data bits appear at the inputs of the shift registers and are clocked through the shift registers by the shift register clock pulses Ø1 and Ø2 during T1 or T6 time. The output from the shift registers appears at the inputs to six double inverters. The outputs from the first inverters appears at the inputs to the Z Counter. The outputs from the second inverters appear at the inputs to the delayed Data Registers U112 and U114, and also at the inputs to the Stored Program Input Multiplexers U106 , U107, and U113. At T4 time, the data on the inputs to the Delayed Data Registers will be loaded into the Delayed Data Registers where it may or may not get used, depending on certain conditions of logic. That is, the conditions governing whether the data will recirculate through the shift registers, or if data will be taken from the Delayed Data Register, or from the Z Counter, or from the Card Reader is dependent on the condition of the Data Selector signals H204 and H203 into pins 2 and 14 of the Stored Program Input Multiplexers, U106, U107, and U113. For example, the normal situation is with H203 low and $\overline{H204}$ high, in which case, data will merely circulate out of the multiplexers, through the shift registers, and back to the multiplexers, etc. On the other hand, if the data in the Delayed Data Register is to be used, or the data from the Z counter, or from the Card Reader, then it is necessary to modify the condition of H203 and $\overline{H204}$. The Truth Table shown in Figure 2-3 lists the various options associated with H203 and $\overline{H204}$.

TRUTH TABLE

SHIFT REGISTER INPUT DATA

H203	$\overline{H204}$	
A	B	DATA SELECTED
L	H	CIRC. DATA
L	L	Z COUNTER INPUTS
H	H	DELAYED DATA
H	L	CARD READER DATA

} TO SHIFT REGISTERS

FIGURE 2-3

2-3.1 REGISTER ASSIGNMENTS

There are a total of 32 sixteen digit registers in the 1155 calculator. Of the 32 registers, twenty are designated as storage registers for holding data for future use. These twenty registers are individually addressable by use of a two digit number ØØ through 19. Data stored in these registers can only be retrieved when addressed either via the program being run, or from the keyboard directly.

The remaining twelve registers are designated as working registers and are not addressable. These registers are divided into two groups designated upper registers and lower registers. Data is held in these registers until needed for the arithmetic computations in progress and as the data is developed, it is moved in and out of these registers under control the Macro Rom programs.

Movement of data from the storage registers to the working registers and vice versa is via register Ø

The addressing of the register to be utilized is done by the Macro Roms. The addressing of the digit within the selected register is a function of the Micro Roms.

A BCD digit 0-9 is stored in each digit position of each register. Four RAMS, each consisting of a 16 x 16 matrix are required to store one digit. Thus, one bit of a digit is stored in each RAM. The four RAMS are accessed at the same time to retrieve one digit, or to write one digit.

Octal notation is used within the RAMS for identifying the registers, thus, the octal numbers Ø through 13 are assigned to the twelve working registers and the octal numbers 14 through 37 are assigned to the twenty storage registers.

2-4.0 MARKER COUNTER OPERATION (REFERENCE LOGIC SCHEMATIC #1 TP 285-1)

There are a total of 512 program steps or spaces available in program storage, but only 511 of these spaces are available for actual program storage. The purpose of the Marker Counter Generator is to develop a marker that will identify the start and stop position of the program steps as the program develops. This includes the normal incrementing of the program as the instructions enter the program storage, as well as the necessary editing operations of delete and insert. The operation of the Marker Counter is as follows:

The Marker Counter consists of two 74L93 IC chips designated U116 and U123 on board #1. The two counters are connected in series and have a common reset. Each counter operates on a modulus 16 base, and since they are in series, the total count will be 512 which is the number of program steps.

The clock for the Marker Counter is a signal called Adv Marker Counter which originates from the set output of the Marker Counter Clock Input flip flop (U208-13). The clock input to the Marker Counter Clock Input flip flop is through an inverter 220-8 and a gate 223-8. The output of gate 223-8 will toggle the J-K flip flop each TØ or T4 time unless the gate is blocked by its other input. Since the J-K flip flop requires two clock inputs for each output transition, the signal Adv Marker Counter will clock the Marker Counter one time for each two clock pulses. The signal Adv H200 will make a transition each time the Marker Counter reaches a count of 256.

The starting or stopping of the Marker Counter must follow certain conditions or qualifications determined by the requirements of the machine logic. The control gate for starting or stopping the Marker Counter is gate 223-8. Pin 8 input to this gate is normally high and the TØ or T4 input to pin 10 allows the gate to clock the Marker Counter Clock Input flip flop 208-13. This flip flop (208-13) can be preset but it cannot be cleared. A junction from pin 2 of 208-13 goes to an inverter 218-6 whose output is a signal called Reset Marker Ctr. A low into pin 2 of 208-13 will cause the output of inverter 218-6 to go high and reset the Marker Counter to zero. Therefore, anytime the Marker Counter is cleared to zero, the Marker Counter Clock Input flip flop 208-13 must first be preset. Once it is preset, then the next time it is clocked, the flip flop is reset and the negative transition out of the set output (pin 13) clocks the Marker Counter. In effect, then, each time the Marker Counter clears to zero, it is immediately clocked again.

Control of the preset logic for the Marker Counter Clock Input flip flop 208-13 is by means of four NAND gates (223-6, 214-6, 214-12, and 214-8). These preset gates will be qualified by various logic conditions and will be explained later as the various operations occur.

In order for the Marker Counter to mark the point at which the data in a certain program is being used, the Marker Counter must be stopped at that precise point and then held there for one extra clock time. During this extra clock time, the data continues to move past the marker one complete step. The Marker Counter is then started again and each time it counts through 512 steps and reaches zero, the marker arrives at the point the next data position occupies. In effect, the Marker Counter is blocked during the interval in which data is being manipulated. The net result is that when the counter is unblocked and starts counting again, the marker has moved back one step in reference to the data that was manipulated. The marker is now referenced to the next instruction (data) position available for use in the program.

2-4.0 MARKER COUNTER OPERATION (Cont.)

Three flip flops designated H200 (U233-12), H201 (U233-9) and H202 (U204-5) control the blocking and unblocking of the Marker Counter. Each time that an instruction is to be used as required by the program, or keyboard, the H202 flip flop will be preset before the Marker Counter is counted to zero. This preset occurs prior to any shifting or manipulating of data and sets up the logic for blocking the Marker Counter.

The signal Adv H200 is the clock input to the H200 flip flop and is active on the trailing edge of TØ or T4. The output of the Marker Counter (U123) is the signal Adv H200 and it will go low when the Marker Counter steps to zero. At that time, the clock input to H200 flip flop will go low causing it to set. The set output from H200 will go high permissing the set of the H201 flip flop. The clock input to H201 is TØ or T4, therefore, if TØ is clocked and H200 sets on the trailing edge of TØ, the H201 flip flop will set on the trailing edge of T4. When the H201 set output goes high, it causes the $\overline{\text{H200}}$ flip flop to clear via gate 232-8. (The other input to gate 232-8 is the signal K40 which deals with program search and is high at this time.) The condition then, is: H200 low and H201 high during the period between TØ and T4 or T4 and TØ. Then, as the data that is to be manipulated causes the H202 flip flop to be preset, the Marker Counter counts to zero. At this time, the H200 flip flop has been reset, the H201 flip flop is set, and the H202 flip flop is set. Therefore, with the signals H201 and H202 both high into gate 224-11, the output of the gate will be low into gate 223-8, blocking the gate by keeping its output high and thus effectively blocking the Marker Counter clock input.

With the Marker Counter at zero and the Marker Counter Clock Input flip flop blocked, the Marker Counter cannot start counting again until the block is removed. In order for the Marker Counter to resume counting in the proper sequence with the unblocking of the gate 223-8 and the timing signals TØ or T4, the block is delayed one more clock time while the flip flop 233-9 (H201) is clocked to its reset state. When the H201 flip flop resets, it toggles the H202 flip flop (U204-5), causing it to reset. With both H201 and H202 flip flops reset, the gate 223-8 is unblocked. Then, on the next TØ or T4 time, the Marker Counter Clock Input flip flop (U208-13) will be clocked causing the signal Advance Marker Counter to clock the Marker Counter and the Marker Counter will resume counting.

2-5.0 KEYBOARD MATRIX DECODING (REFERENCE CARD #1 TP-285-1)

As shown in the accompanying list of keyboard codes, each key on the 1155 keyboard is assigned a particular output code designated "Z" code, which enables the machine to perform the instructions associated with the key that was depressed.

Depression of a key closes a reed switch. The reed switches are connected as shown in Figure 2-4 to form a matrix. The swinger side of the reed switches are connected to form eight parallel outputs designated a through h. The stationary side of the reed switches are connected to form eight parallel outputs designated i through p.

The "Z" counter (U22) is clocked on the negative going edge of each "T" clock and counts from "0" through "7". As the count goes from "7" to "0", the "0" count going negative clocks the "Z" counter (U5). Therefore, for each eight count in the Z counter (U22), the Z counter (U5) counts once. As the U22 "Z" counter initially counts from 7 to 0, both Z counters are at a count of 0 and the program buss line "i" is enabled. Thus, the reed switch output lines a and i are simultaneously enabled. As each line i through p is enabled, the a through h lines are strobed. Counting continues in this manner until a circuit is completed from ground on the U24 demultiplexer through one of the output lines i through p, to one of the output lines a through h on the multiplexer U26. At this point the NOR gate U18 is enabled and the signal "K" goes low. Output of the "K" signal sets the K' flip flop. The K' flip flop setting, causes the signal K1000 to stop the Z counter and also enables the set of the D flip flop. The count in the Z counter is then decoded via the Macro Rom input latches (U14 and U22 on card 4) at the same time the D flip flop sets. The Macro Rom address counter receives the decoded Z counter output via the Macro Rom input latches. The Macro Rom program is then stepped out of the Halt loop and the Macro Rom program steps the Instruction Counter to the instruction address corresponding to the key that was depressed.

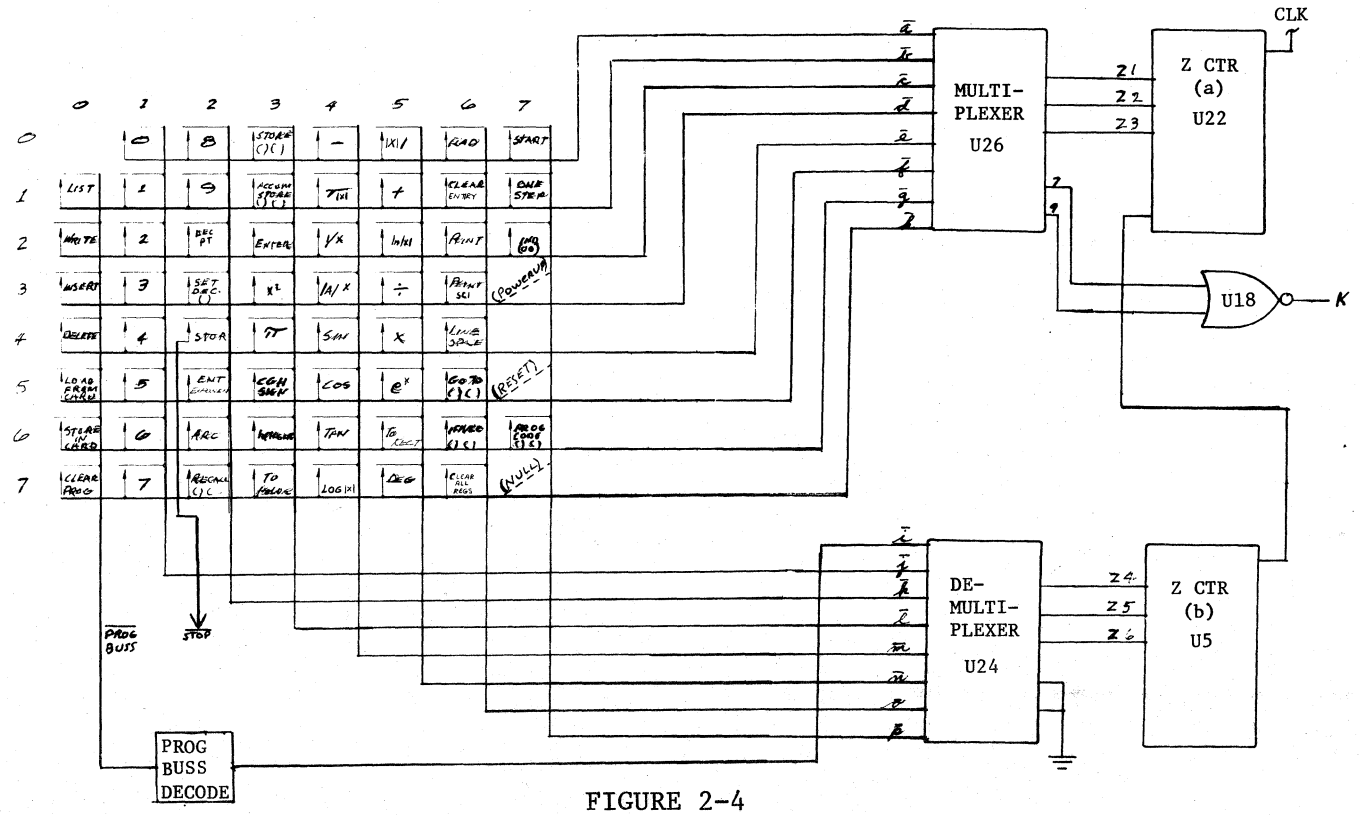


FIGURE 2-4

2-5.0 KEYBOARD MATRIX DECODING (Cont.)

KEYTOP	KEYBOARD CODE			Z CODE
LIST	$\overline{b}$	$(\overline{i})$	$\overline{PROG\ BUSS}$	1 - - - - - -
WRITE	$\overline{c}$	$(\overline{i})$	$\overline{PROG\ BUSS}$	- 2 - - - - -
INSERT	$\overline{d}$	$(\overline{i})$	$\overline{PROG\ BUSS}$	1 2 - - - - -
DELETE	$\overline{e}$	$(\overline{i})$	$\overline{PROG\ BUSS}$	- - 3 - - -
LOAD FROM CARD	$\overline{f}$	$(\overline{i})$	$\overline{PROG\ BUSS}$	1 - 3 - - -
STORE IN CARD	$\overline{g}$	$(\overline{i})$	$\overline{PROG\ BUSS}$	- 2 3 - - -
CLEAR PROG	$\overline{h}$	$(\overline{i})$	$\overline{PROG\ BUSS}$	1 2 3 - - -
0	$\overline{a}$	$\overline{j}$		- - - 4 - -
1	$\overline{b}$	$\overline{j}$		1 - - 4 - -
2	$\overline{c}$	$\overline{j}$		- 2 - 4 - -
3	$\overline{d}$	$\overline{j}$		1 2 - 4 - -
4	$\overline{e}$	$\overline{j}$		- - 3 4 - -
5	$\overline{f}$	$\overline{j}$		1 - 3 4 - -
6	$\overline{g}$	$\overline{j}$		- 2 3 4 - -
7	$\overline{h}$	$\overline{j}$		1 2 3 4 - -
8	$\overline{a}$	$\overline{k}$		- - - - 5 -
9	$\overline{b}$	$\overline{k}$		1 - - - 5 -
.	$\overline{c}$	$\overline{k}$		- 2 - - 5 -
SET DEC ( )	$\overline{d}$	$\overline{k}$		1 2 - - 5 -
STOP	$\overline{e}$	$(\overline{k})$	$\overline{STOP}$	- - 3 -(5)-
ENTER EXP	$\overline{f}$	$\overline{k}$		1 - 3 - 5 -
ARC	$\overline{g}$	$\overline{k}$		- 2 3 - 5 -
RECALL ( ) ( )	$\overline{h}$	$\overline{k}$		1 2 3 - 5 -
STORE ( ) ( )	$\overline{a}$	$\overline{\ell}$		- - - 4 5 -
ACCUM STORE ( ) ( )	$\overline{b}$	$\overline{\ell}$		1 - - 4 5 -
ENTER	$\overline{c}$	$\overline{\ell}$		- 2 - 4 5 -
x^2	$\overline{d}$	$\overline{\ell}$		1 2 - 4 5 -
π	$\overline{e}$	$\overline{\ell}$		- - 3 4 5 -
CHANGE SIGN	$\overline{f}$	$\overline{\ell}$		1 - 3 4 5 -
INTGR	$\overline{g}$	$\overline{\ell}$		- 2 3 4 5 -
TO POLAR	$\overline{h}$	$\overline{\ell}$		1 2 3 4 5 -

2-5.0 KEYBOARD MATRIX DECODING (Cont.)

KEYTOP	KEYBOARD CODE		Z CODE
−	$\overline{a}$	$\overline{m}$	- - - - - 6
$\sqrt{\lvert x \rvert}$	$\overline{b}$	$\overline{m}$	1 - - - - 6
$1/x$	$\overline{c}$	$\overline{m}$	- 2 - - - 6
$\lvert A \rvert^x$	$\overline{d}$	$\overline{m}$	1 2 - - - 6
SIN	$\overline{e}$	$\overline{m}$	- - 3 - - 6
COS	$\overline{f}$	$\overline{m}$	1 - 3 - - 6
TAN	$\overline{g}$	$\overline{m}$	- 2 3 - - 6
$\log \lvert x \rvert$	$\overline{h}$	$\overline{m}$	1 2 3 - - 6
$\lvert x \rvert !$	$\overline{a}$	$\overline{n}$	- - - 4 - 6
+	$\overline{b}$	$\overline{n}$	1 - - 4 - 6
$\ln \lvert x \rvert$	$\overline{c}$	$\overline{n}$	- 2 - 4 - 6
÷	$\overline{d}$	$\overline{n}$	1 2 - 4 - 6
X	$\overline{e}$	$\overline{n}$	- - 3 4 - 6
e^x	$\overline{f}$	$\overline{n}$	1 - 3 4 - 6
TO RECT	$\overline{g}$	$\overline{n}$	- 2 3 4 - 6
DEG	$\overline{h}$	$\overline{n}$	1 2 3 4 - 6
RAD	$\overline{a}$	$\overline{o}$	- - - - 5 6
CLEAR ENTRY (PLOT)	$\overline{b}$	$\overline{o}$	1 - - - 5 6
PRINT	$\overline{c}$	$\overline{o}$	- 2 - - 5 6
PRINT SCI	$\overline{d}$	$\overline{o}$	1 2 - - 5 6
LINE SPACE	$\overline{e}$	$\overline{o}$	- - 3 - 5 6
GO TO ( ) ( )	$\overline{f}$	$\overline{o}$	1 - 3 - 5 6
IF NEG ( ) ( )	$\overline{g}$	$\overline{o}$	- 2 3 - 5 6
CLEAR ALL REGS	$\overline{h}$	$\overline{o}$	1 2 3 - 5 6
START	$\overline{a}$	$\overline{p}$	- - - 4 5 6
ONE STEP	$\overline{b}$	$\overline{p}$	1 - - 4 5 6
IND ( ) ( )	$\overline{c}$	$\overline{p}$	- 2 - 4 5 6
RESET	($\overline{f}$)	($\overline{p}$)	(1 - 3 4 5 6)
PROG CODE ( ) ( )	$\overline{g}$	$\overline{p}$	- 2 3 4 5 6
POWER UP	($\overline{d}$)	($\overline{p}$)	1 2 - 4 5 6

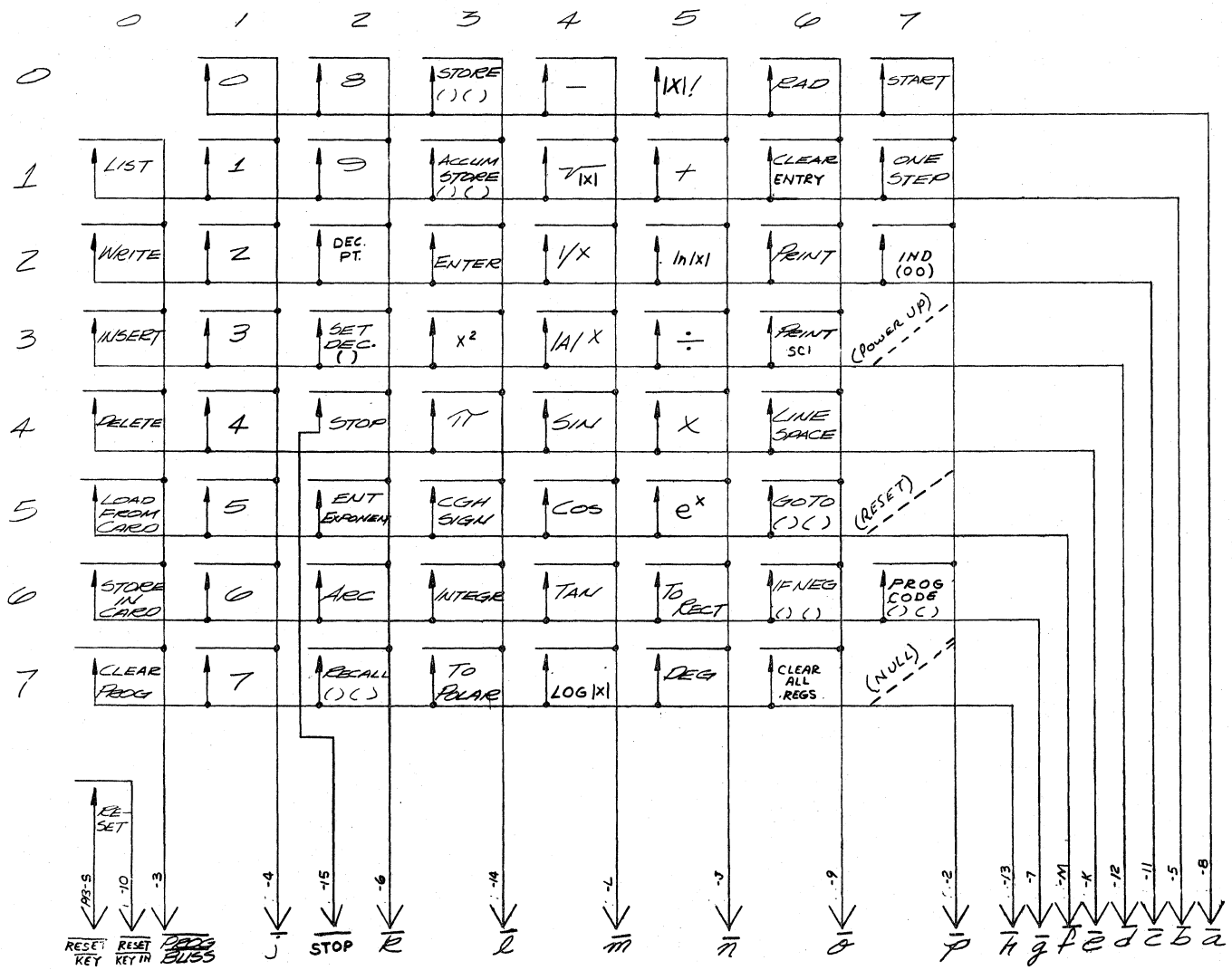

0 1 2 3 4 5 6 7
0
1
2
3
4
5
6
7
0
8
STORE ( ) ( )
—
|X|
READ
START
LIST
1
9
ACCUM STORE ( ) ( )
√|X|
+
CLEAR ENTRY
ONE STEP
WRITE
2
DEC. PT.
ENTER
1/X
ln|X|
PRINT
IND (00)
INSERT
3
SET DEC. ( )
X²
|A| X
÷
PRINT SCI
(POWER UP)
DELETE
4
STOP
π
SIN
X
LINE SPACE
LOAD FROM CARD
5
ENT EXPONENT
CGH SIGN
COS
e^x
GOTO ( ) ( )
(RESET)
STORE IN CARD
6
ARC
INTEGR
TAN
TO RECT
IF NEG ( ) ( )
PROG CODE ( ) ( )
CLEAR PROG
7
RECALL ( ) ( )
TO POLAR
LOG|X|
DEG
CLEAR ALL REGS
(NULL)
RESET
193-5
-10
-3
-4
-15
-6
-14
-1
-5
-9
-2
-13
-7
-11
-4
-12
-11
-5
-8
RESET KEY
RESET KEY IN
PROG BUSS
J
STOP
K
L
M
N
O
P
H
G
F
E
D
C
B
A

FIGURE 2-5

2-6.0 PROGRAM ENTRY FROM KEYBOARD

The Friden 1155 Programmable Calculator has seven function modes that are associated with program entry in addition to the manual or keyboard mode. The seven function modes are: Write, List, Insert, Delete, Store in Card, Load from Card, and Clear or Reset. For the Program Entry from Keyboard, the "WRITE" mode is used and is initiated by depressing the Write key.

WRITE is concerned with the direct entry of a program from the keyboard, Other modes enable the modification of the program once it is loaded into the machine. These modifications may include the insertion of new instruction, the deletion of instructions not required for the program, or the deletion of erroneous instructions and the insertion of correct instructions in its place.

There are 511 locations for program instructions in the program storage area of the machine. These instruction locations may or may not be completely occupied, at the option of the operator. Several programs may be entered or only one, however, when multiple programs are entered, each one must be defined by a program designator entered at the beginning of the program. This designator enables the operator to address the desired program directly. (See Operator's Primer, Form #55-537.)

All program instructions are entered serially one after the other. There are no gaps where no data exists between instructions or programs. Nulls or No Data indicators fill the area of program storage not occupied by instructions. Actually there are 512 positions of storage in the machine, but the 512th position is never used. One Null will always be present. The first Null sensed indicates that the last instruction has been sensed and the required logic action taken. The 512th position is retained to ensure that reset, initializing, etc., will be accomplished.

All stored data in the machine is volatile and will be lost if a power loss occurs, or anytime the machine is turned off. Therefore, to avoid the laborious re-entry of programs from the keyboard, the program may be stored on a magnetic card for future use. The storage of the program in this manner utilizes another one of the seven modes, namely Store In Card mode, that can be exercised as a one key function at the option of the operator.

A program is entered from the keyboard in two steps. The first is the depression of the Write key, and then the depression of keys representing the desired instructions. The depression of the Write key initializes all of the logic circuitry for enabling the entry of instructions into the program area of the machine. For purposes of this discussion, it will be assumed that the program area is initially clear.

When the Write key is depressed, a path for current through the keyboard matrix (Figure 2-5) will be completed to line $\overline{c}$ of U126 and line $\overline{i}$ of U124. The Z counter will count to 20_8. The multiplexer U126 will have a low out of pins 7 and 9 with a count of 20_8 in the Z counter. The signal "K" will go high at this time and permiss the setting of the flip flop designated K', U425-9.

The "T" counter (U528) and the 100's counter (U128) will continue to count. When the signal T400 goes high, the K' flip flop sets. This action starts the delay timer (U402), and blocks the further counting of the Z counter for as long as the Write key is depressed. The clock signal K1000 being blocked at gate U426-6 prevents the Z

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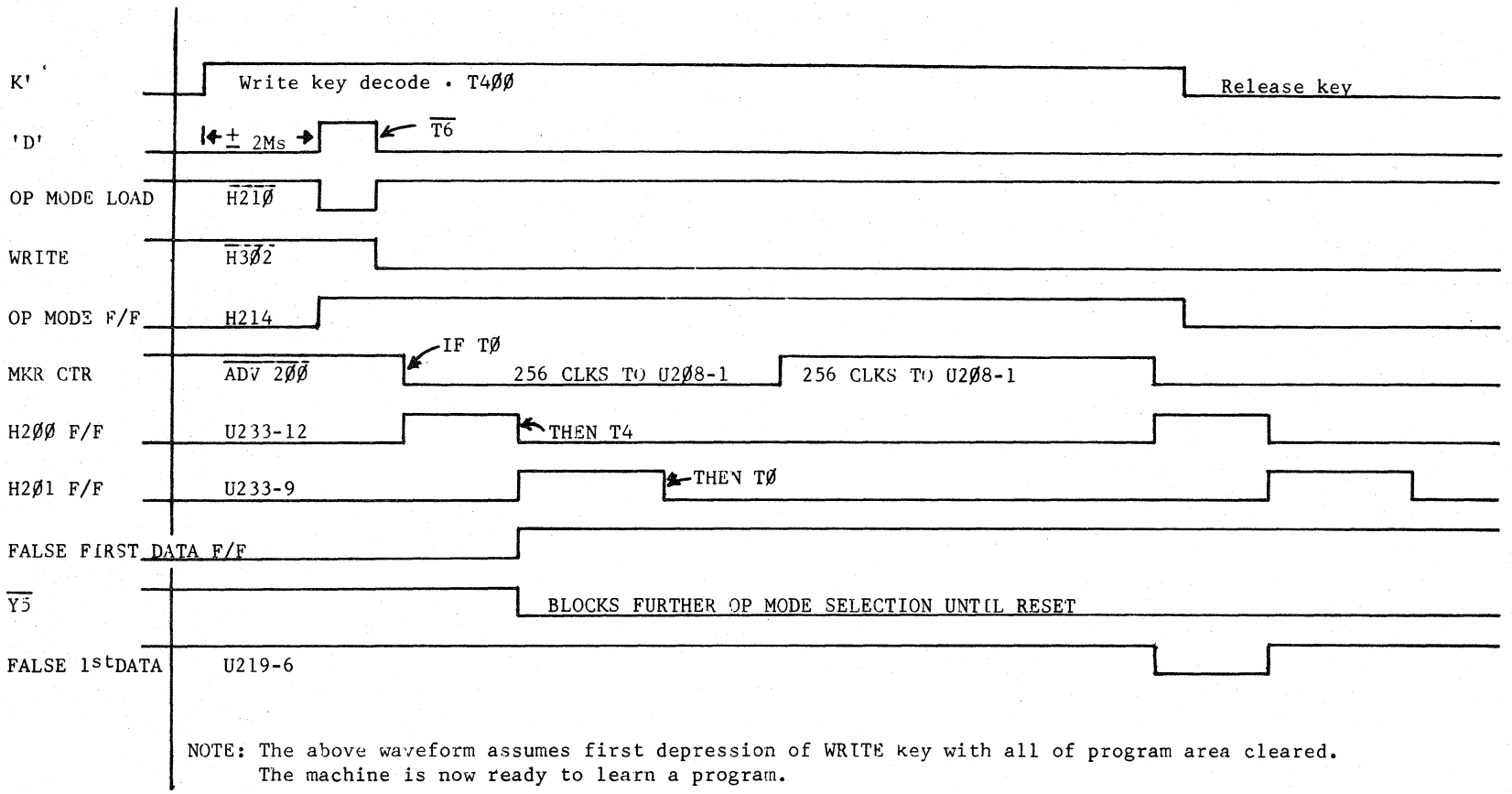
WRITE OPERATING MODE



NOTE: The above waveform assumes first depression of WRITE key with all of program area cleared. The machine is now ready to learn a program.

FIGURE 2-5

2-6.0 PROGRAM ENTRY FROM KEYBOARD (Cont.)

counter from stepping to the next keyboard code. The Z counter transitions on the negative edge of the clock signal. The positive leading edge of the signal T400 sets the K' flip flop and prevents the clock K1000 from transitioning high to low to step the Z counter.

The "D" flip flop (U425-5) sets at the end of the keyboard delay if the K' flip flop is still in a set condition. The output of gate U426-8 goes low when the "D" flip flop sets. This low signal designated H210, performs three functions: (1) It loads the Write decode into the Program Mode Latch (U227). (2) It blocks the Program Mode Decoder (U222) until the "D" flip flop resets, and (3) it initiates the clearing of the "D" flip flop. H210 low makes all outputs of the Program Mode Decoder to go high, setting the Program Mode flip flop (U212-9).

The signal H210 is double inverted via gate 207-6 and inverter U209-12 and the output becomes H213. The signal H213 clears the Read New Instruction flip flop (U212-5) and sets the Clr "D" Latch (U125-3 and U117-3). The output of the Clr D Latch , designated H217, is negatively "anded" with the signal T6 and the "D" flip flop is cleared. The Clr D Latch is reset at T8 time.

The signal H210 goes high, the Z counter outputs are latched into the Program Mode Latch, the block is removed from the Program Mode Decoder, and the Write Mode, H302 becomes active.

The Program Mode flip flop (U212-9) will be set only for the length of time the key selecting the operating mode is depressed. It will then reset and cannot be set again until the Program Mode Latch has been cleared by the Reset key. The Program Mode flip flop performs several necessary functions during the time it is set.

The Marker Counter has been running free up until this point. The shift registers have also been stepping twice for each "T" time cycle. In this discussion, it is assumed that the shift registers have no data, therefore, the outputs will all be high indicating all Nulls. With no data entered, there will be no "First Null" since there is nothing to reference it to.

The False First Data flip flop (U226-9) is used to enable the entry of the first data into the shift registers. The clock gate for the False First Data flip flop is U225-8. Pin 9 of this gate will be high when either Write, Insert, or Card mode have been selected. Pin 11 will be high when one of the aforementioned modes have been selected and the Program Mode flip flop (U212-9) is set. Pin 10 will go high when the Marker Counter counts to zero. This output of the Marker Counter sets the H200 flip flop (U233-12). The next TØ + T4 will set the H201 flip flop (U233-9). The signal H201 is the last required high into the clock gate U225-8 for the False First Data flip flop. When the signal H201 goes high into the gate, the output goes low. Then the next TØ + T4 will reset the H201 flip flop and set the False First Data flip flop. The Marker Counter continues to count. The Y5 Latch is set via the output from gate U219-3 going low. As long as the Y5 Latch is set, no other operating mode can be selected.

On the next data pass (512 steps), when the H200 flip flop (U233-12) sets, an attempt will be made via gate U219-6 to indicate first data, however, the gate is blocked by inverter U209-10 as long as the signal H214 is high out of the Program Mode flip flop.

WRITE MODE

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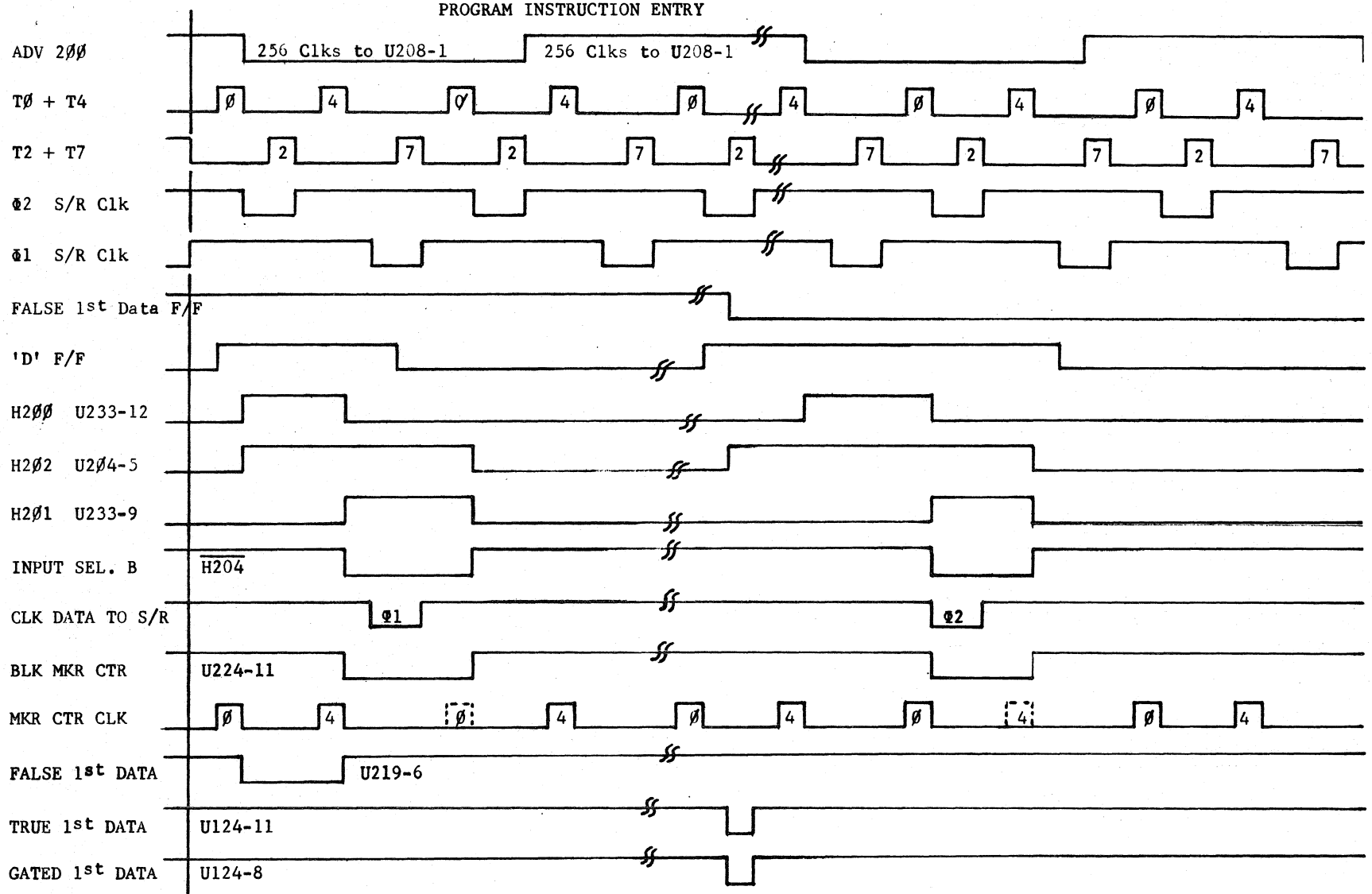
PROGRAM INSTRUCTION ENTRY



TIMING CHART IS FOR 1st and SUBSEQUENT INSTRUCTIONS ENTERED IN WRITE MODE. THE PATTERN WILL REPEAT UNTIL ENTIRE PROGRAM ENTERED. NOTE MUTATION OF MARKER COUNTER CLOCK, WHICH EFFECTIVELY SHIFTS ALL PREVIOUSLY ENTERED DATA ONE POSITION RIGHT. NEW DATA ENTERED TRAILING OLD BY ONE CLOCK POSITION.

10/2/72

FIGURE 2-7

2-6.0 PROGRAM ENTRY FROM KEYBOARD (Cont.)

The Delete or Null flip flop (U206-9) is held cleared, first by the Program Mode flip flop, and then by the False First Data flip flop, as long as it is set.

The release of the Write key allows the K' flip flop to reset which in turn, resets the Program Mode flip flop. The Program Mode flip flop resetting unblocks the lst data input to the H202 flip flop (U204-5) preset input. The machine is now prepared to "Learn" the instructions required to complete a program

The second step, or the "Learning" of the instructions in a program is accomplished in the following manner. (Reference Timing Chart, Figure 2-7.)

Each time the Marker Counter sets the H200 flip flop (U233-12), the False First Data flip flop presents a high input to the H202 flip flop (U204-5) preset input gate U217-12, making the input ineffective until another key is depressed and the "D" flip flop sets.

A key representing the first instruction of the program to be entered is depressed and the "D" flip flop is set. The development of false first data when the signal H200 goes high, now finds the signal "D" high into gate U217-12 and the output of this gate presets the H202 flip flop (U204-5). The next TØ + T4 will set the H201 flip flop which immediately clears the H200 flip flop. The status of the three flip flops (H200 reset, and H201 and H202 set) will remain constant for four "T" times (T1-T4 or T5-TØ).

When the H200 flip flop resets and the H201 flip flop sets, the output of gate U205-1, designated $\overline{H204}$, goes low as a gating signal for the shift register multiplexers. The other multiplexer gating signal is designated $\overline{H203}$, and is low throughout a program entry. Both gating signals to the multiplexers (U206, 107, and 113) going low decodes the outputs of the Z counter, and presents them to the shift register inputs. The Z counter data will then be placed in the shift registers at either T1 or T6 time, depending on whether H201 flip flop set at the end of TØ or the end of T4.

To sync the Marker Counter to the data flow through the shift register, the Marker Counter is blocked during the clock time that shifts the data into the shift register. The Marker Counter will then be in step with the next data entry. The operation is accomplished as follows: The H201 flip flop (U233-9) will reset at the end of the first TØ or T4 time after the H200 flip flop (U233-12) resets. When the H201 flip flop sets, the clock to the Marker Counter is blocked and the TØ or T4 that resets the H201 and H202 flip flops does not get through to clock the Marker Counter. The clock to the shift registers, however, causes the data to shift into the registers. The H201 and H202 flip flops resetting makes the multiplexer gating signal $\overline{H204}$ go high. With the configuration of gating signals $\overline{H204}$ high, and $\overline{H203}$ low, the data will continue to recirculate through the shift registers.

FIRST DATA. A complete data pass (512 steps) is required to enter one instruction. The first instruction will recirculate and when it reaches the output of the shift registers, the signal First Data (lst Data) will be developed. The signal lst Data clears the False First Data flip flop (U226-9) at T2 or T7 time and gate U124-8 develops the true First Data signal. This signal, First Data, will be developed each data pass until a key is depressed and the "D" flip flop is set. Once again, the H202 flip flop will be preset when First Data goes high at T2 or T7 time.

PROGRAM ENTRY FROM KEYBOARD

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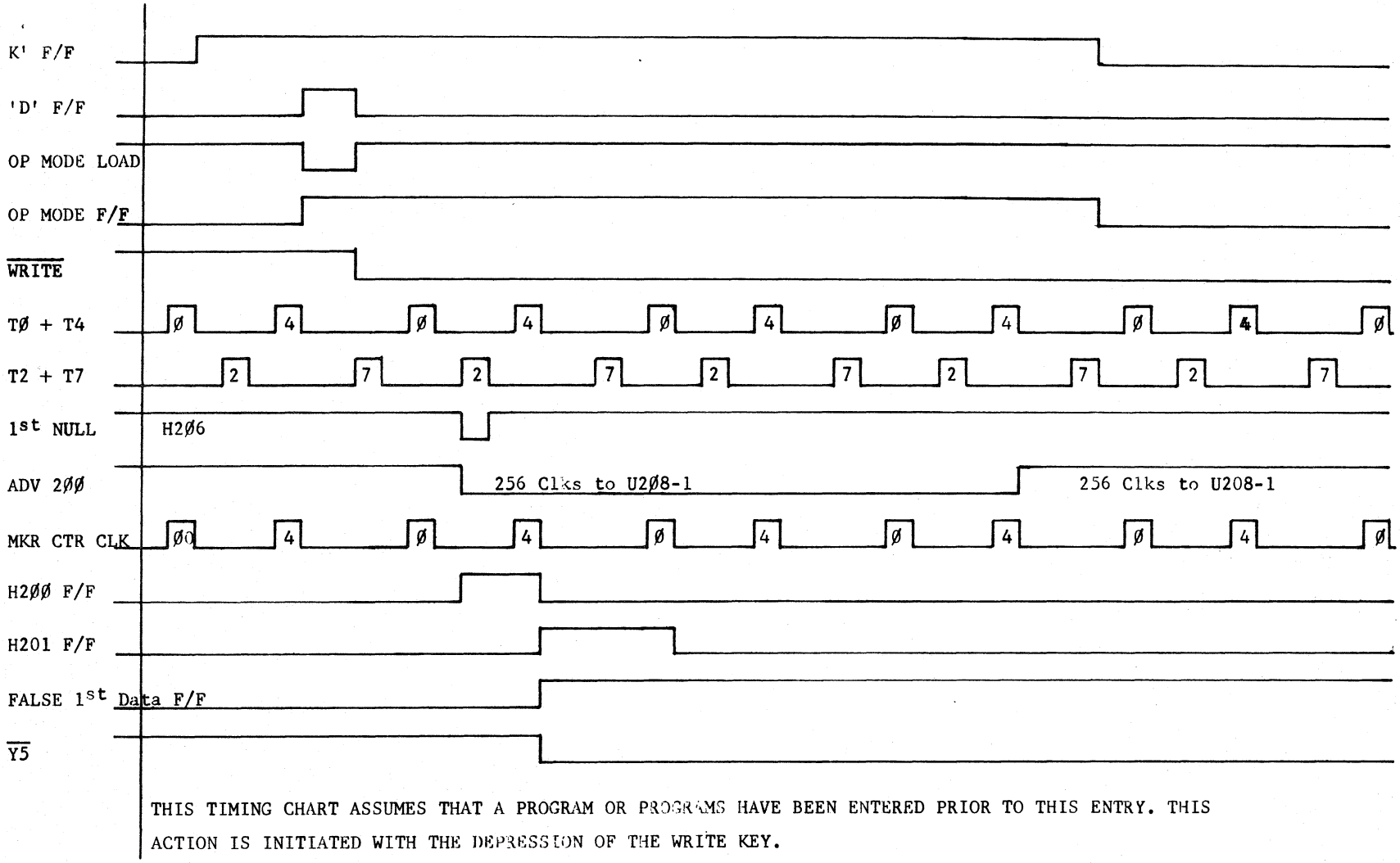


THIS TIMING CHART ASSUMES THAT A PROGRAM OR PROGRAMS HAVE BEEN ENTERED PRIOR TO THIS ENTRY. THIS ACTION IS INITIATED WITH THE DEPRESSION OF THE WRITE KEY.

FIGURE 2-8

2-6.0 PROGRAM ENTRY FROM KEYBOARD (Cont.)

The Marker Counter will count to zero, set the H200 flip flop, the H201 will set at the end of the next TØ or T4 time, clearing the H200 flip flop; the new keyboard instruction will be loaded into the shift registers at T1 or T6 time, and the marker counter will be retarded by one count. This procedure will continue until all instructions are entered. The Write mode and Program Entry can only be terminated by depressing the Reset key. The Reset key clears the Program Mode Latch and Program Mode Decoder, and the machine returns to the Idle Mode.

2-6.1 ENTRY OF MULTIPLE PROGRAMS

Identifying numbers should be assigned to each program when more than one program is entered in the machine. These numbers may be any two digit number between ØØ and 99, and in any order. Sequential numbering is not necessary. The numbers are for identification only and will be recognized when sampled. The procedure for entering and identifying multiple programs has been covered in the Operator's Primer form number 55-537.

As mentioned earlier, all keyboard program entries are initiated by depressing the Write key. Since several functions may have taken place since the last program entry, additional program entries become a bit more complex.

The Write key sets up the logic to receive a new program as described earlier. The first key depressed after the Write key in a multiple program entry is the Program Code key. Depressing this key places a program identifier code in the very first program location following the last instruction of the previously entered program. This code designated under the octal notation 76_8 identifies the beginning of a new program when the machine is in a program search. The two digits entered immediately following the Program Code key identifies the program that is to follow. The balance of the program is entered serially following the two digit program identifier.

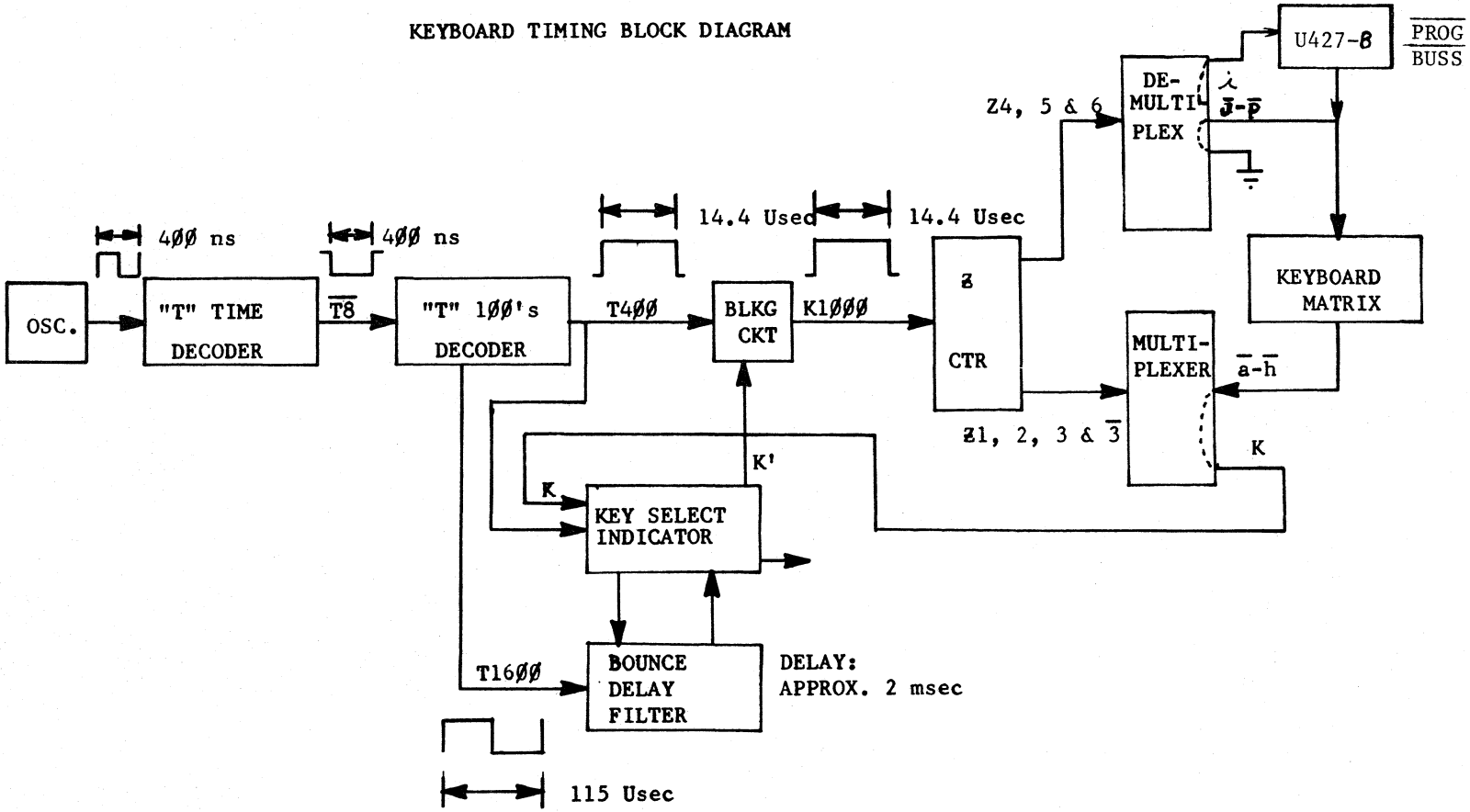
MARKER SYNC TO NEW PROGRAM (Refer to Timing Diagram, Figure 2-8.)

The Marker Counter must by synced to the first Null location immediately following the last program entered. This is necessary for the proper placing of the program identifier, and is accomplished as described in the following paragraphs.

Depression of the Reset key returns the machine to the Manual mode of operation. Next, the Write key is depressed and many of the same functions initiated by the Write key in the initial program entry are the same as described in the preceding paragraphs that is: K' flip flop sets, keyboard delay, "D" flip flop sets, Program Mode flip flop sets, Program Mode Latch loads the Write keyboard code into the Program Mode Decoder, the "D" flip flop is reset, and Write is decoded. The False 1st Data flip flop is set, but is only effective when the program storage area is cleared. The Y5 latch is also set to prevent selection of any other operating mode until the Reset key is depressed.

The outputs of the shift registers are sampled by a special gating network. A Null, or no data, is detected in this network when the first position following the last instruction of the last program entered is clocked to the output of the shift registers. The Null, octal notation 77_8 is moved to the shift register outputs at T1 or T6 time. The first Null is gated out at T2 or T7 times.

KEYBOARD TIMING BLOCK DIAGRAM



NOTE: THE BASIC OSCILLATOR FREQUENCY MAY VARY FROM MACHINE TO MACHINE. ALL TIMES SHOWN ARE APPROXIMATE.

FIGURE 2-9

2-6.1 ENTRY OF MULTIPLE PROGRAMS (Cont.)

The first Null is decoded as $\overline{H206}$ in gate U117-6. It is then inverted and combined in gate U214-12 with the Program Mode flip flop and Write. The output of this gate clears the Marker counter. The Marker Counter output signal, Adv 200, going low sets the H200 flip flop (U233-12). Then the H201 flip flop is set the very next TØ or T4 time after the Marker Counter is cleared. The Marker Counter begins its new count cycle with the same TØ or T4 that set the H201 flip flop.

The False 1st Data flip flop U226-9 will be reset on the very next data pass when the first output is clocked out of the shift registers following the last Null that was shifted out. 1st Data will also be generated each data pass, but will be ineffective until a key is depressed and the D flip flop is set. This key should be the Program Code key to identify the new program being entered.

The program will now be entered in exactly the same manner as was previously described for the first program entry. Again, the program entry will be terminated by the Reset key.

Each succeeding program will be entered the same way, i.e., depress Write key to initiate the logic for a program entry and to sync the timing to the first Null. Then enter the Program Code and two identifying digits, followed by the program in its entirety; and finally terminate the entry by depressing the Reset key.

LOAD INITIAL PROGRAM FROM CARD READER

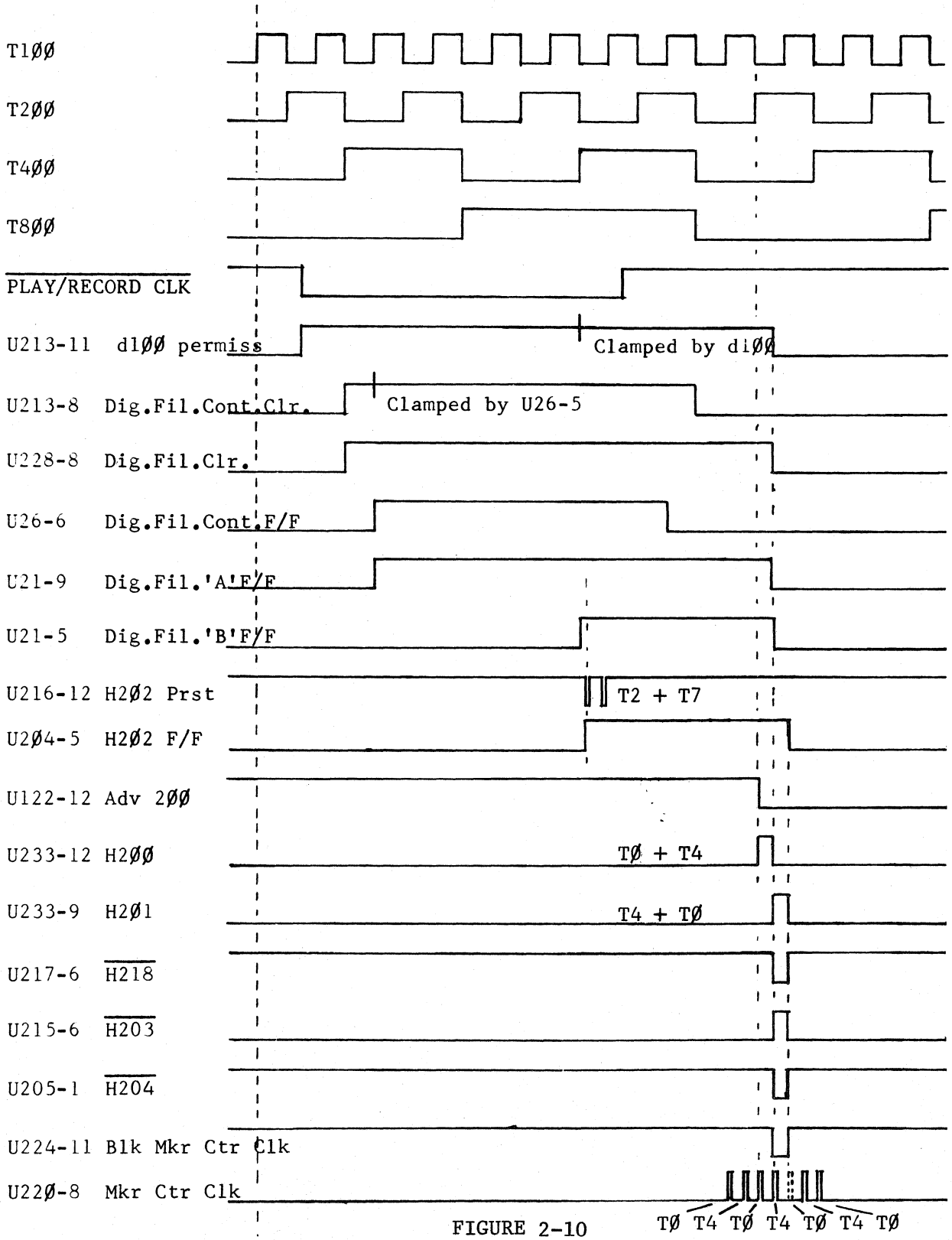


FIGURE 2-10

2-7.0 PROGRAM LOAD/STORE FROM CARD READER

The Friden 1155 Calculator is designed for connecting a Magnetic Card Reader/Player (Model 511 Magnetic Card Reader) to a plug at the rear of the machine. A stored program in the 1155 can then be read into the Card Reader for storage on a magnetic card, or a program stored on the magnetic card can be read into 1155 for storage in the 1155 memory. Each of these function modes is initiated by depressing the Store In Card key or the Load from Card key located on the 1155 keyboard. The logic description for each mode of operation will be discussed in the following paragraphs.

2-7.1 LOAD FROM CARD MODE

The 1155 calculator can also be programmed from the 511 Magnetic Card Reader/Player either as a complete program load of 511 instruction steps or partially, depending on the requirements of the operation.

Depressing the Reset key retores the machine to the manual, or idle mode of operation. The Load From Card key is then depressed to setup the logic necessary to receive a program from a magnetic card inserted into the Card Reader/Player. Depression of the Load From Card key generates a signal which becomes a permiss (when combined with a signal generated by inserting a card in the reader) to start the card reader motor, and drive the card through the reader heads.

NOTE: The Card Reader motors will vary slightly in speed, from one card reader to another. Transmission from the card reader into the 1155 program area is asynchronous, being strobed or clocked each time a new instruction is to be transmitted from the card reader. This clock pulse synchronizes the logic of the 1155 with that of the card reader.

THEORY OF LOAD FROM CARD

In Load from Card, the signal $\overline{\text{H305}}$ goes into gate 213-6 (which is the same gate as used for Load from Keyboard). The output of gate 213-6 goes to gate 214-2 and if the signal First Null ($\overline{\text{H206}}$) is developed into gate 214-12, it will clear the Marker Counter at the point of the First Null. (As previously explained under "Program Entry From Keyboard" a First Null cannot be developed if the Program Storage is clear since there will be 512 Nulls to choose from.) Up to this point, the logic is the same as described for the Write Mode, however, at the end of the Write Mode, it was necessary to depress the Reset key in order to return to Manual Mode. In the event the Load From Card key is depressed and a Load does not take place, then it will be necessary to depress the Reset key to restore the machine to Manual Mode.

The signal $\overline{\text{ADV 200}}$ goes low at TØ or T4 when the Marker Counter steps to zero and sets the H200 flip flop. H200 will be stepped at either TØ or T4 time. H201 will set at TØ or T4 following the setting of H200.

The False First Data flip flop (U226-9) sets when H201 sets. The False First Data flip flop being set will have no effect in loading first data as it did in programming from the keyboard. It will clamp the Delete/Null flip flop reset until True First Data is shifted out of the Shift Register. This will ensure that the Card Reader input will not be blocked.

2-7.1 LOAD FROM CARD MODE (Cont.)

When the Load From Card is released and the K' flip flop resets, the signal $\overline{\text{PLAY}}$ is made low. This signal goes to the card reader as a permiss and a signal to the card reader as an indication that the machine is ready to be programmed from the card reader. The 1155 will not accept data from any other source until the Reset key is depressed.

It is assumed initially that there are no instructions stored in the program area.

A signal designated $\overline{\text{PLAY/RECORD CLOCK}}$ is recorded on the card preceding each recorded instruction. As the card proceeds through the card reader, this signal is read prior to reading the instruction and is returned to the 1155 as a strobe or clock pulse. The $\overline{\text{PLAY/RECORD CLOCK}}$ signal will be low for approximately 1 ms. The data associated with a particular strobe input will be presented to the input gates for approximately 1.5 ms.

The signal $\overline{\text{CARD BUSY}}$ goes low when a card is inserted. The first time after the card is inserted that the H201 flop flop resets, the Load from Card flip flop (U226-6) will set. The reset side of U226-6 blocks the clock input of flip flop U203-12 and prevents its setting. The set output of U203-12 (H229) remaining low unblocks the set input of the Clr "D" latch and H213 may now go low because of the action of the Clr "D" inputs.

The flip flop U203-12 remaining reset also insures that the Reset key must be depressed to get out of the Card Mode.

The signal $\overline{\text{PLAY/RECORD CLOCK}}$ goes low when a card is being transported through the reader and an instruction is coming into position to read. $\overline{\text{PLAY/RECORD CLOCK}}$ going low into gate U213-11 permisses the setting of flip flop d100 (U201-5). $\overline{\text{PLAY RECORD CLOCK}}$ also goes to the reset permiss of flip flop U206-6, allowing the U206-6 flip flop to set on the next T100 clock. At T400 time, $\overline{\text{T400}}$ will go low into gate U213-8 and the output will go high, removing the clear input to U206-6 (Digital Filter A) flip flop via gates U230-13 and U228-8.

Clock pulse T100 sets the flip flop U206-6. The reset output of the control flip flop U206-6 clamps the clear signal high out of gate U213-8 when T400 goes high once again. The set output of flip flop U206-6 clocks the Digital Filter flip flop "A" (U201-9). The set output of the "A" flip flop (U201-9) removes the clear from the Digital Filter flip flop "B" (U201-5), and the next T400 pulse sets the "B" flip flop making the signal d100 high. The signal d100 high clamps the Digital Filter clear input high via gate U230-13; and presets the H202 flip flop (U204-5) via gate U216-12 at T2 or T7 time. The signal d100 clamps the set permiss of the d100 flip flop (U201-5) high, via gate U213-11.

The signal $\overline{\text{PLAY/RECORD CLOCK}}$ will go high and permiss the reset of the Digital Filter Control flip flop U206-6. The reset will occur on the next T100 time. The permiss will remain high until the next instruction is to be read from the card.

2-7.1 LOAD FROM CARD MODE (Cont.)

The Marker Counter will count to zero and set the H200 flip flop (U233-12). The H201 flip flop (U233-9) will set on the next TØ or T4 after H200 sets. H201 setting clears the H200 flip flop via gate U232-8.

The Data Control signal ($\overline{H218}$) out of gate U217-6 will go low when the H201 flip flop sets. $\overline{H218}$ clears the Digital Filter via gates U205-4 and U232-11. $\overline{H218}$ makes H203 high via gates U205-4 and U215-6; and $\overline{H204}$ low via gates U205-4 and 205-1. The signal $\overline{H218}$ low, also resets the Digit Filter Control Latch (U119-3 and U124-6). This clamps the Digit Filter cleared until the next Null output of gate U111-6.

The combination of H203 high and H204 low, selects the inputs from the Card Reader to the shift register input multiplexers. The data from the Card Reader is selected and presented to the shift register inputs. At T1 or T6 time, the data is loaded into the shift registers.

When H201 flip flop sets, one count is deleted from the Marker Counter clock input via gate U224-11, resulting in the next instruction being placed in the next instruction position. H201 will reset at the next TØ or T4. Then $\overline{H218}$ goes high, H203 goes low, and $\overline{H204}$ goes high, causing the data in the shift registers to recirculate. H201 resetting also reset H202.

The machine idles, waiting for the next PLAY/RECORD CLOCK to go low and initiate another cycle. These cycles will repeat until all the instructions on the card have been read, or until a total of 511 instructions have been read from a number of cards. No more instructions can be entered after the 511th.

PROGRAM ENTRY FROM CARD READER AFTER INITIAL PROGRAM ENTRY

For this explanation, it is assumed that one or more programs have been entered and additional programs are to be entered from the card reader. As in the entry from the keyboard, timing must be synchronized with the first location in program storage, immediately following the last instruction that was previously entered.

Depression of the LOAD FROM CARD key will stop the Z Counter at 50_8. The "D" flip flop will set and when it resets, the signal $\overline{H210}$ going high sets a count of five in the Program Mode Decoder (U222) and the signal Load From Card ($\overline{H305}$) goes low. The Program Mode flip flop (U212-9) sets when the signal $\overline{H210}$ goes high. When First Null (H206) comes out of the shift register, at either T2 or T7 time, the signal Reset Marker Counter will go low at the output of gate U214-12; presetting the Marker Counter Clock flip flop (U208-13), and clearing the Marker Counters U116-12 and U123-12). The output of U123-12 (Adv 200) sets the H200 flip flop (U233-12). The Marker Counter is now synchronized with the data already entered, and is setup to place the next bit of entered data in the First Null position.

The key is released and the machine goes into an idle condition with $\overline{H305}$ low. The signal $\overline{PLAY}$ goes low and the Y5 latch sets. The 1155 is now ready to read a card. The balance of the loading from the card is done exactly as in the initial loading of a program from the card reader.

2-7.2 STORE IN CARD MODE

The program entered and circulating in the 1155 can be stored on a magnetic card by means of the Model 511 Magnetic Card Reader/Player connected to the 1155. Storing of data on the magnetic card is initiated by depressing the Store In Card key. Depressing the Store In Card key sets up the logic required for this operation, and places the first instruction in position to be read when the card is inserted into the card reader. As the data is recorded on the magnetic card, it is retained within the 1155 storage.

Since the Card Reader is slower than the 1155 logic, data from the 1155 is buffered on the RECORD lines that input to the card reader and the 1155 logic is then held up until the data is recorded on the magnetic card and the card reader notifies the 1155 that it is ready to accept new data.

THEORY OF STORE IN CARD

With the Store In Card key depressed, the signal K will go high when the Z counter has a count of 608. The K' flip flop is set when T400 goes high, starting the delay timer. The "D" flip flop will set approximately 1 ms after the K' flip flop sets, and "D" setting causes the signal H210 to go low. The signal H210 going low, loads the the Z counter bits 1, 2, and 3 into the Program Mode Latch (U227) and makes the 8-bit input to the Program Mode Decoder (U222) a high, and this high 8-bit input results in making all of the used outputs of U222 high. The signal H300 going high sets the Program Mode flip flop (U212-9) and the output signal H214 goes high. H214 will remain high until the first T400 after the key is released.

The signal $\overline{\text{H210}}$ going low immediately sets the Clr "D" Latch and the "D" flip flop is reset when T6 goes low. The latch will reset at T8 time. The "D" flip flop resetting causes the signal H210 to go high, latching the Z counter inputs into the Program Mode Latch, and removing the high from the 8-bit input to the Program Mode Decoder (U222). The signal H306 then goes low and the logic for the Store In Card Mode is underway.

The signal Card Mode goes high at gate U219-11 when $\overline{\text{H306}}$ goes low and Card Mode going high into gate U219-3 sets the Y5 latch and unblocks the clock input to the False 1st Data flip flop . It also unblocks the flip flop U226-6 which is used to prevent a Clear operation while the Card Reader is operating. The signal Card Mode unblocks the junction of U231-8 and U210-6, allowing the clearing and counting of the Digital Filter for each instruction loaded into the Card Reader.

The $\overline{\text{Store In Card}}$ signal ($\overline{\text{H306}}$) going low causes the signal $\overline{\text{H310}}$ to go high at the output of gate U215-8. H310 going high enables the setting of the "D" flip flop and the loading of the next instruction into the Z counter. Store In Card clamps the signal H210 high in the output of gate U120-6. The signal H240 is used to unblock the Digital Filter clear gate U228-8.

The signal ADV 200 goes low when the Marker Counter (U116 and 123) is counted to zero. ADV 200 going low sets the H200 flip flop (U233-12) at the trailing edge of either TØ or T4 time. The H201 flip flop will set on the next TØ or T4 time after H200 flip flop sets, and will immediately clear the H200 flip flop. On the next TØ or T4 time, the H201 flip flop will reset and as it resets, it clocks the False 1st Data flip flop. The False 1st Data Flip flop set output clamps the Delete or Null flip flop reset until 1st Data clears the Marker Counter to zero, and syncs on the

2-7.2 STORE IN CARD MODE (Cont.)

first data out of the counter. Once the Marker Counter is synced to the data, the Delete or Null flip flop cannot set and block the Store In Card operation.

The signal $\overline{\text{1st Data}}$ clears the Marker Counter to zero via gate U214-8 and clears the False 1st Data flip flop.

(NOTE: Once the Marker Counter is synced to the data, every data pass will result in the setting of the H200 and H201 flip flops, the clearing of the False First Data flip flop, and the setting of the False First Data flip flop. Since a data pass is slightly under 1ms, the False First Data flip flop can be observed setting and resetting at that rate until the Store In Card key is released. The Marker Counter will be reset each time first data comes out of the shift register, but it will not be apparent because the Marker Counter will already be at zero due to having been synced to data, prior to this time.)

When the Store In Card key is released, the K' flip flop and the Program Mode flip flop will reset. The K' flip flop resetting unblocks the H202 preset gate (U216-8) and the first T2 or T7 after K' resets, the H202 flip flop will be preset. The K' flip flop resetting also clamps the Start + One-Step flip flop reset and makes the signal $\overline{\text{Record}}$ a low signal at gate U231-11.

The first instruction will be transferred to the Z Counter after the Store In Card key is released, and it will be held in the Z Counter until a card is inserted in the card reader. The card reader will record the data and indicate that it has been recorded. The 1155 will then transfer the next instruction to the Z Counter and the action will repeat.

The load in Z Counter, transfer to the Card Reader, record cycle will be followed until the first null is loaded into the Z counter. From that point on, no other loads will be accomplished. The null will remain in the Z counter and all nulls will be recorded by the card reader.

The logic action necessary to accomplish the loading and transferring of instructions to the card reader is as follows:

The K' flip flop will reset the first T400 time after the key is released and gate U209-8 will unblock the H202 flip flop preset gate (U216-8). Since T400 is a multiple of the T8's , the K' flip flop will reset at T8 time. The H202 flip flop will be preset the next T2 time due to the action of gate U225-12. Nothing more happens until the Marker Counter counts to zero. (Note: It is assumed for this discussion that the Marker Counter will count to zero at TØ time.) Advance 200 will set the H200 flip flop. H201 flip flop will set at the end of T4 time, immediately clearing the H200 flip flop. The output of gate U217-8 will go low, presetting the "D" flip flop and loading the instruction in the output of the shift registers into the Z counter. This instruction will be the first instruction in the program or programs to be loaded on the card.

Presetting the D flip flop blocks any further transfer of data by blocking the presetting of the H202 flip flop at gate U225-12. Nothing more can be done until the card reader has recorded the first instruction on the card. Then, at TØ time, immediately following the presetting of the D flip flop and the loading of the instruction in the Z counter, gate U224-11 blocks one count of the Marker Counter clock. The Marker Counter is now synchronized with the second instruction to be transferred.

2-7.2 STORE IN CARD MODE (Cont.)

The machine may be in an idle condition for one or many data passes, waiting for a card to be inserted in the reader/recorder. Finally, however, a card will be inserted.

The signal $\overline{\text{Reader Busy}}$ goes low when the card is inserted, permissing the set of flip flop U226-6. The first time that the H201 flip flop resets, U226-6 will set. U226-6 setting insures that the only way the Store In Card operation can be terminated before the Store in Card operation is complete is by depressing the Reset key.

The signal $\overline{\text{Play/Record Clock}}$ is generated in the Card Reader/Recorder just prior to a read or write by the card reader/recorder. This signal permisses the set of the Digital Filter Control flip flop (U206-6) and permisses the set of the Digital Filter "B" flip flop (d100) U210-5. At T400 time, the clear is removed from U206-6 flip flop and at T500 time, the flip flop is set. U206-6 setting , sets the U201-9 flip flop removing the clear from the U201-5 flip flop. The next T400 time sets U201-5 and the signal d100 goes high. The output of U207-8 ($\overline{\text{H213}}$), goes low and sets the Clr "D" latch. The "D" flip flop is cleared at T6 time and the latch is reset at T8 time.

The "D" flip flop is cleared at T6 time and the H202 flip flop will be preset at T7 time. The Marker Counter will count to zero, H200 will set, H201 will set, clearing H200, and the D flip flop will be preset,initiating the loading of the next instruction.

The Marker Counter will miss one clock and be in step with the next instruction to be transferred. The $\overline{\text{Play/Record Clock}}$ will go low, indicating that the instruction is being recorded and the D flip flop will be cleared once more. This cycle of operation will continue until all of the instructions for every program have been transferred and recorded.

The first null will be loaded and transferred in exactly the same manner as the legitimate instruction. However, the second null will be loaded into the Z counter and the "D" flip flop will be blocked from clearing for the balance of the card.

The signal $\overline{\text{H57}}$ will be low and H571 will be high when the second null is ready for transfer to the Z counter. H201 will go high to transfer the null to the Z counter and at either TØ or T2, depending on the clocking of the Marker Counter, H250 will go high. H250 going low at the end of TØ or T4 time will cause U201-9 flip flop to set, blocking the Clr "D" gate, U207-8.

The signal $\overline{\text{Reader Busy}}$ will go high when the card moves out of the card reader, and will permiss the reset of U226-6. H201 resetting after its next set, will reset U226-6. The reset output of U226-6 will clock U203-12 setting it. The reset of U203-12 permisses the set of the Reset flip flop (U203-8). The next TØ or T4 will set U203-8. The set outputs of U203-12 and U203-8 will cause the Clr "D" latch to set via gate U202-11. This action provides the Clr "D" latch that was blocked during the recording of nulls.

The reset output of the Reset flip flop (U203-8) resets the Y5, Y6, and Y7 latches. It also clears the Program Mode Latch and makes all outputs of the Program Mode Decoder high. The reset input to the Reset flip flop ($\overline{\text{H216}}$) is high and the Reset flip flop will reset the next TØ or T4 after the one which set it.

The 1155 logic then returns to the Manual Mode ($\overline{\text{H300}}$)low and U203-12 and U226-6 are clamped reset. The machine is now ready for the next keyboard selection.

2-7.2 STORE IN CARD MODE (Cont.)

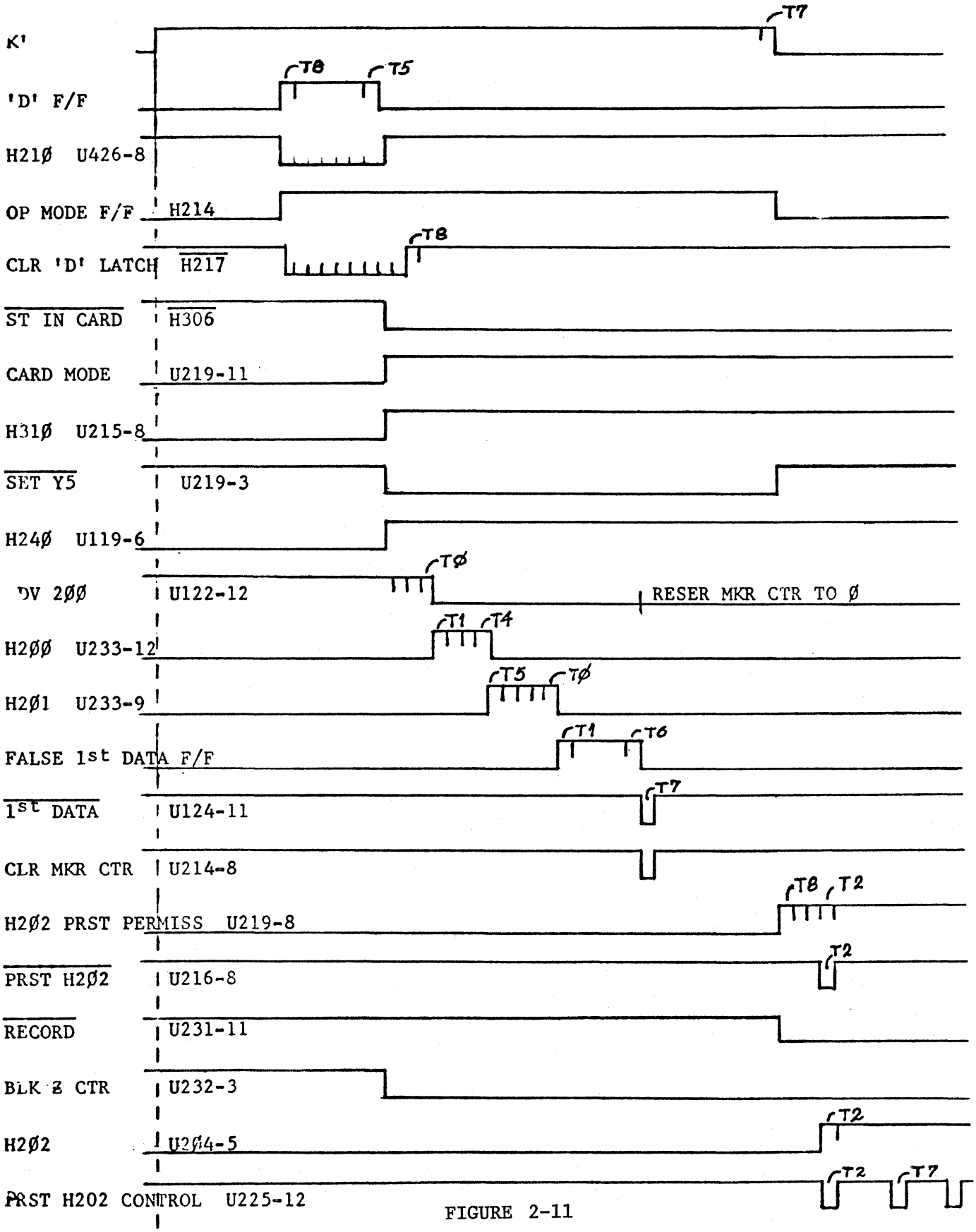
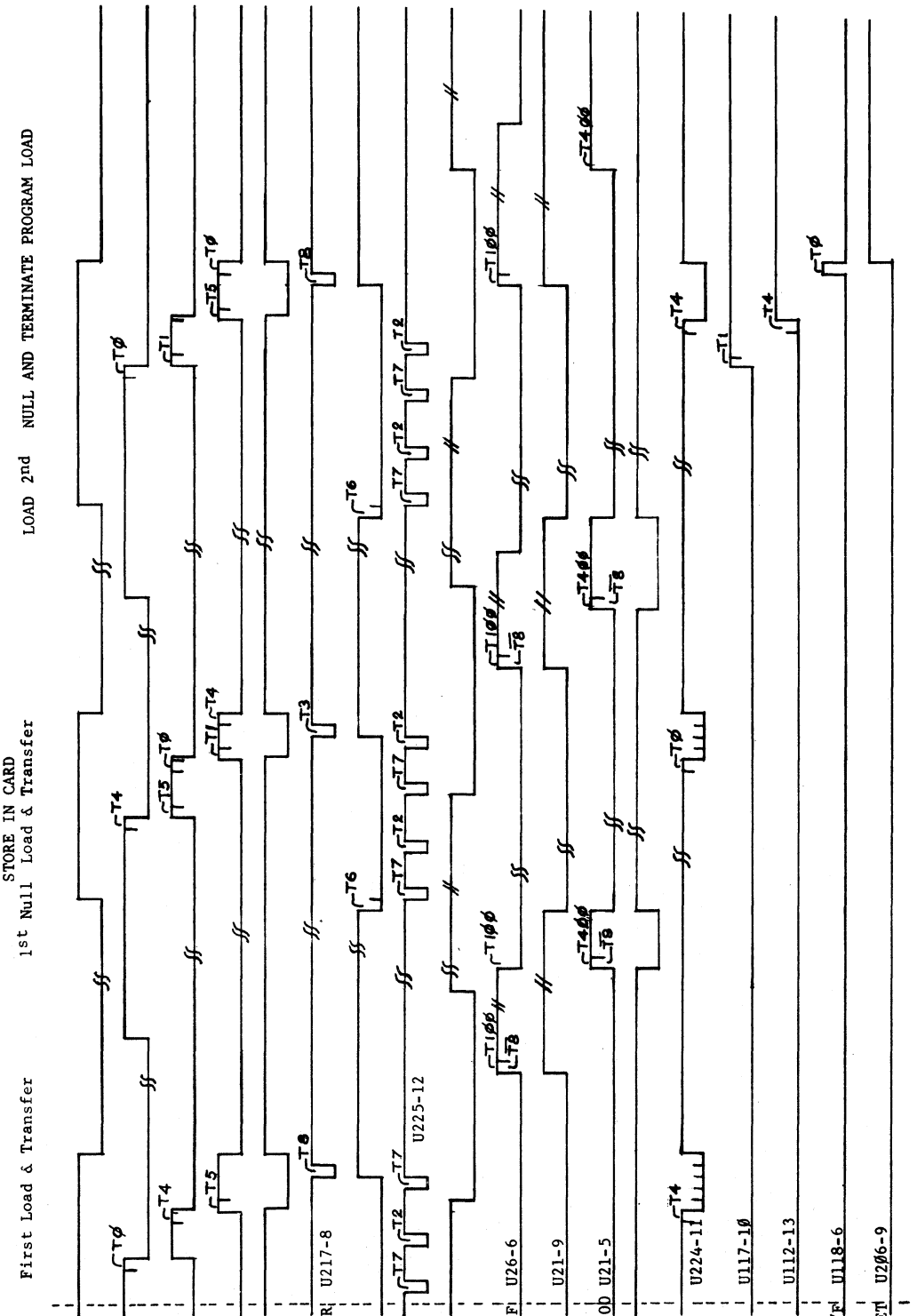


FIGURE 2-11

2-7.2 STORE IN CARD MODE (Cont.)



** For correct timing relationship of the Digital Filter, refer to timing diagram, "LOAD FROM CARD READER #1".

FIGURE 2-12

2-8.0 "Y" LATCH CONTROL

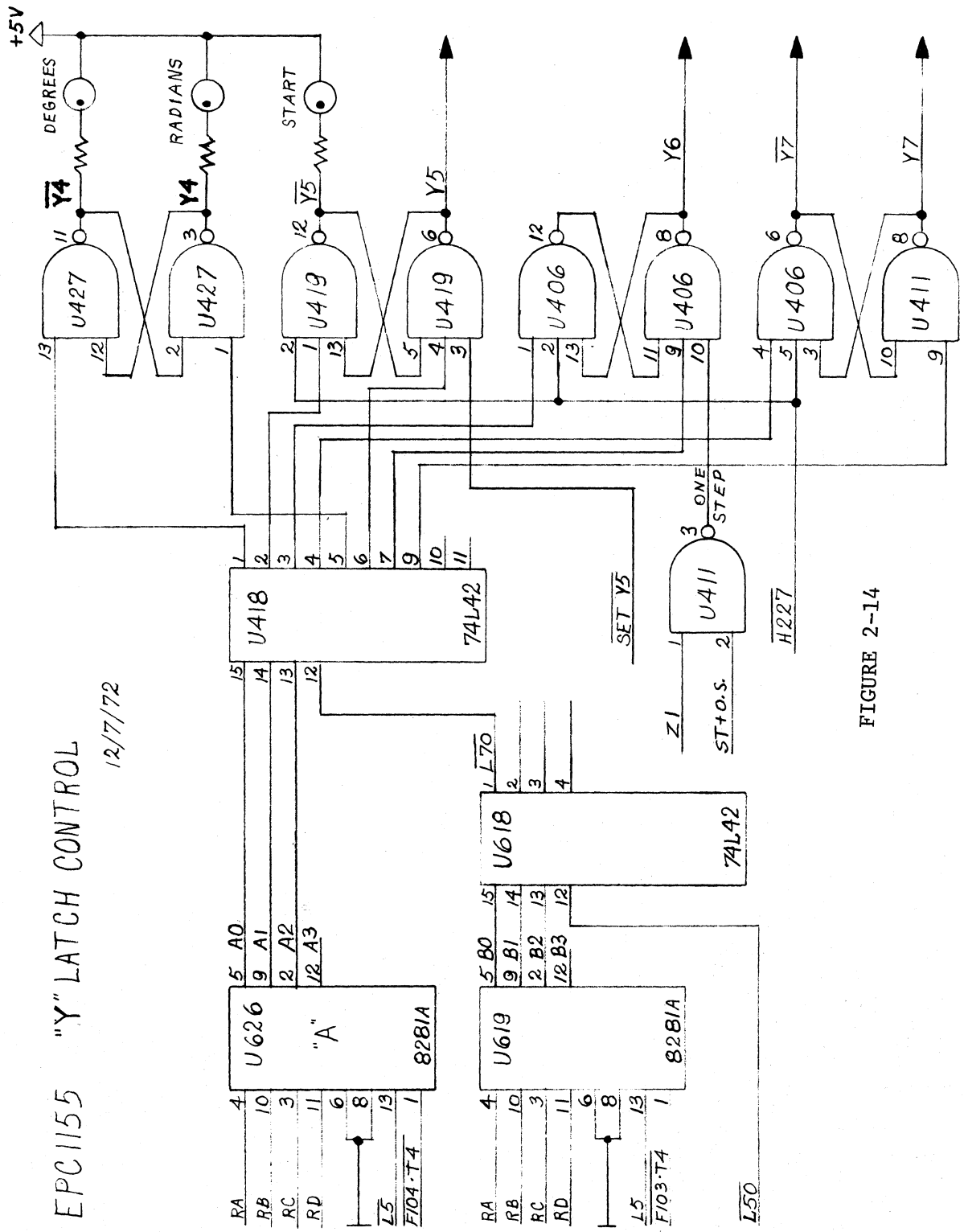


FIGURE 2-14

2-8.0 "Y" LATCH CONTROL

The "Y" latches with the exception of the Y4 latch, are used to provide control logic to enable an operation. The Y5 latch is set by the Start or One Step key, the Card Mode key, the Write key, or the Insert key. It may also be set or reset by the program being run. The Y5 latch, when set, permits the completion of the operations listed.

The Y6 latch, when set, allows either the One Step, or Plot operation to be completed.

The Y7 latch, when set, permits the search for a new program code.

The Y4 latch, when set, lights the Degrees light. When Reset, it lights the Radian light.

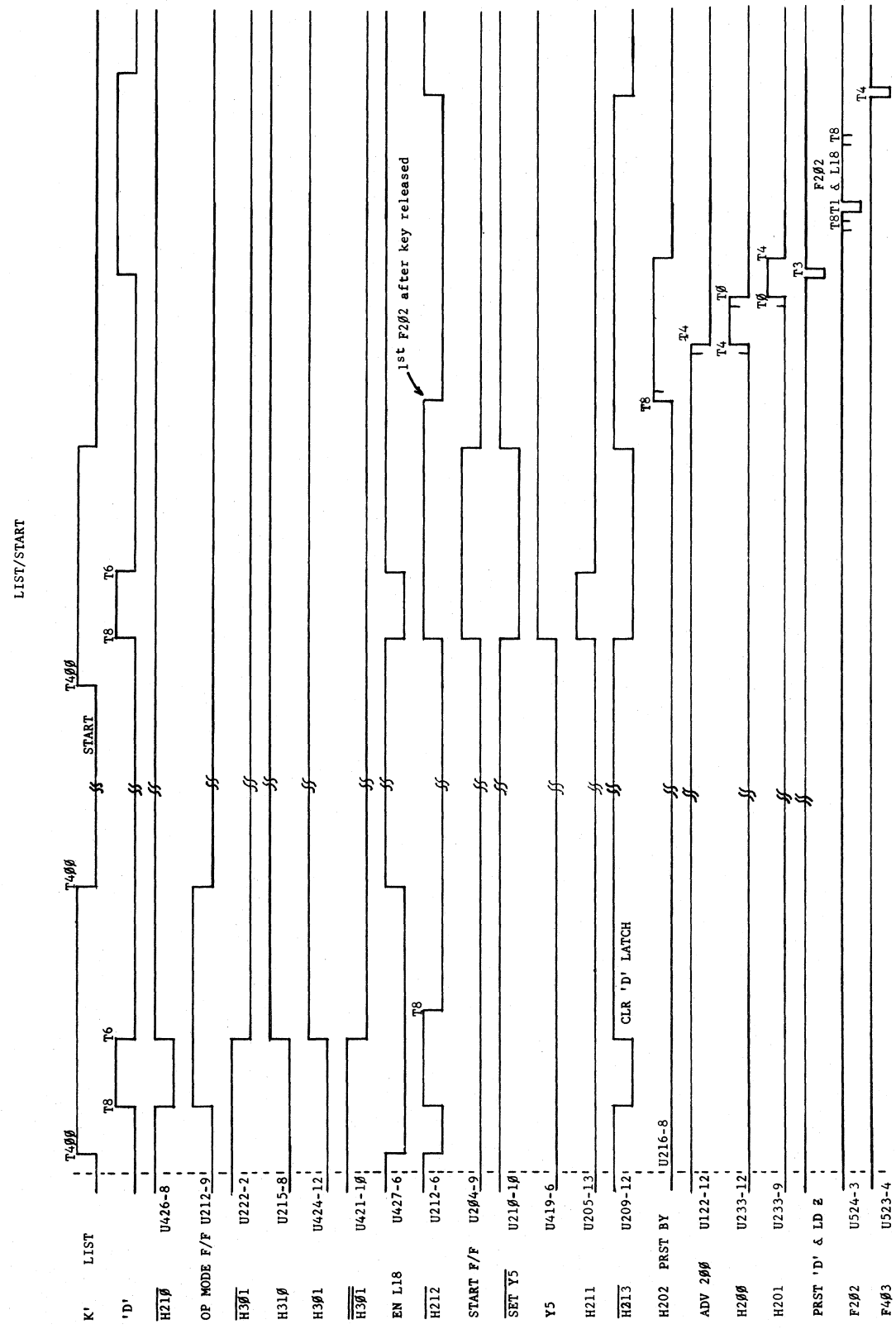
The latches are controlled by the program in the following manner.

The signal $\overline{\text{F103.T4}}$ transfers data from the RAMS to the RAM output register "B" (U619). The signal L50 will allow the "B" register output to be decoded. A zero loaded into the "B" register will result in $\overline{\text{L70}}$ going low for T1 time. $\overline{\text{L70}}$ low will allow the "A" register output to be decoded and the selected latch will be set or reset. The Chart, Figure 2-13, shows the various states of the latches in respect to the outputs of Register "A" and "B".

REGISTER "A"	REGISTER "B"	LATCH	SET	RESET
0	0	Y4		X
1	0	Y5		X
2	0	Y6		X
3	0	Y7		X
4	0	Y4	X	
5	0	Y5	X	
6	0	Y6	X	
7	0	Y7	X	

FIGURE 2-13

2-9.0 LIST OPERATING MODE (Cont.)



LIST #1

1Ø/19/72

FIGURE 2-15

2-9.0 LIST OPERATING MODE

The List key is used to control several functions. For example:

When used with the + key, a number called the Check Sum is developed and printed to verify that the program entered is correct within parameters.

When used with the Start key, a listing of the entire stored program is printed out for information and verification.

When used with the One Step key, each instruction is printed, beginning with the first instruction of the first program, unless otherwise addressed. The machine then stops and waits. This stop is to allow for program modification, such as insertion of one or more new instructions in the program, or the deletion of the last instruction printed.

LIST/START OPERATION (Reference List #1, Figure 2-15)

The first operation to be described will be that of the List key when used in conjunction with the Start key.

The List key is decoded when the Z counter has a count of 10_8, and the signal "K" goes high. The K flip flop will set at the first T400 time after the signal K goes high and initiate the keyboard delay timer action.

The "D" flip flop sets when the timer counts to zero (approx. 1ms.). The "D" flip flop setting, causes the signal $\overline{H210}$ to go low which indirectly sets the Program Mode flip flop (U212-9). The signal $\overline{H210}$ sets the Clr "D" latch, and at T6 time, the "D" flip flop is reset. The "D" flip flop resetting makes the signal $\overline{H210}$ high, and the Program Mode Decoder (U222-2) makes the signal List (H310) low. The $\overline{\text{List}}$ signal will remain low until the Reset key is depressed, at which time, the signal $\overline{H310}$ will go high causing $\overline{H301}$ to go high and H301 to go low. These signals become constants and will not change as long as the signal List (H301) is low.

The signal EN L18 is blocked during the depression of all of the Program Mode keys, and the Start and One Step keys. The signal EN L18 (U427-6) is made low when the "K" flip flop sets, and it remains low until the K flip flop resets. The reason for blocking EN L18 during this time is to prevent the Micro Roms from stepping out of the idle loop into a key entry routine while the contants for the operation to be performed are being established. During this time, the control signal for the preset of the H202 flip flop (signal $\overline{H212}$, U212-5) goes low, but is ineffective. The "K" flip flop being set, blocks the preset of H202 (U204-5) until the "K" flip flop resets, thus preventing the transfer of any data from program storage.

The List key is released and the machine returns to an idle List Mode, waiting for the depression of one of the keys that will initiate the desired action. All of the constants, logic levels, etc., required in a List program mode are now set.

Depression of the Start key initiates a retrieval and printout of all of the stored program. The operation is described as follows:

The Start key is decoded as 07_8. The "K" flip flop sets and after the delay circuit counts down, the "D" flip flop sets. The signal H211 (U205-13) goes high when the "D" flip flop sets. The signal H211 high, sets the Start flip flop (U204-9) which sets

2-9.0 LIST OPERATING MODE

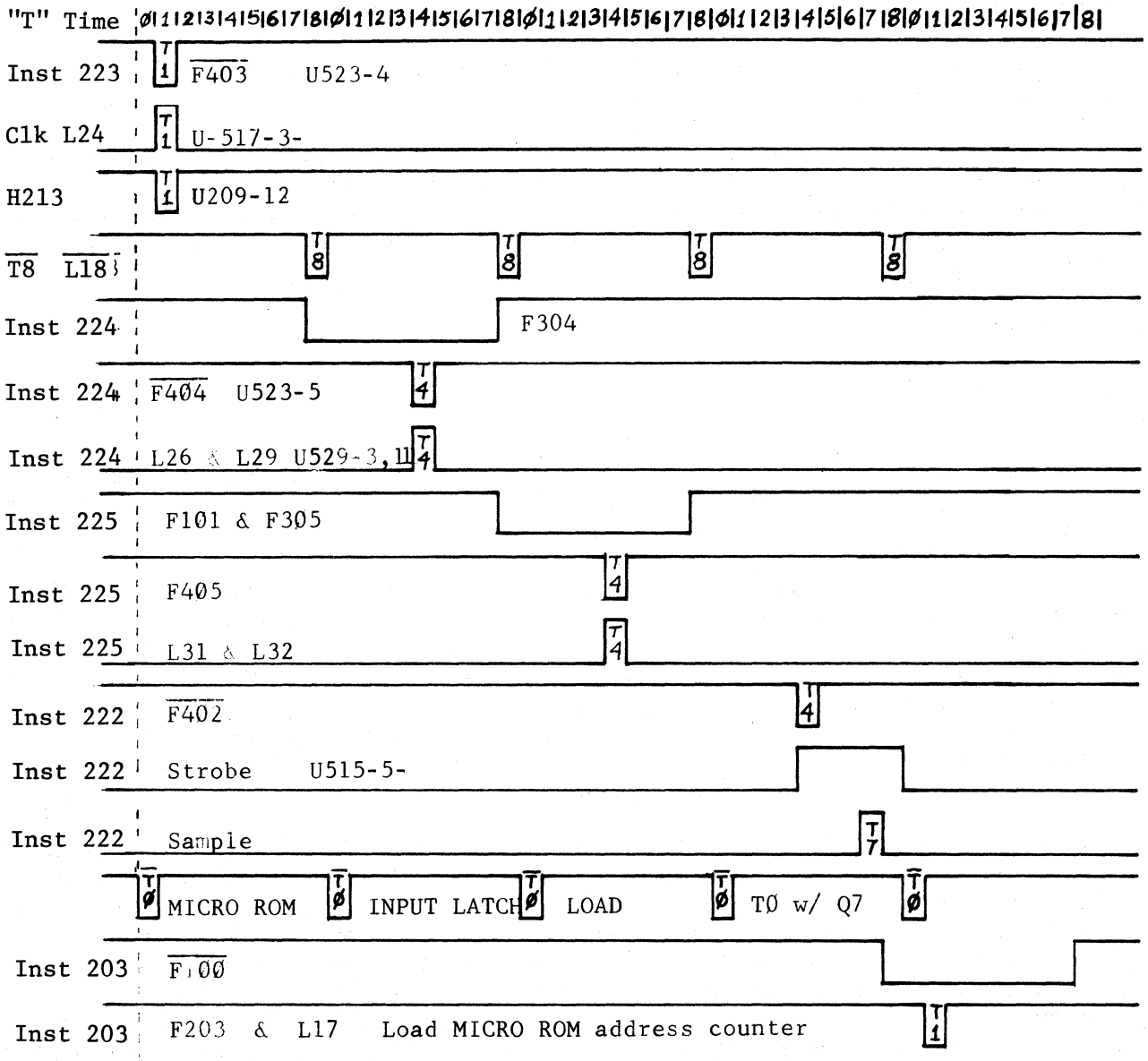


FIGURE 2-16

2-9.0 LIST OPERATING MODE (Cont.)

the Clr "D" latch. The H202 flip flop (Read New Instruction flip flop) U212-5 is cleared and clamped in that condition until the "K" flip flop resets via the same signal ($\overline{H213}$) that set the Clr "D" latch.

The Y5 latch sets when the signal H211 goes high, and will remain set until cleared. The function of the Start key (in this instance) is to set the Y5 latch and block the initiation of the automatic transferring of program data from storage to printer until the logic for this purpose is synchronized. The block is removed when the Start key is released.

The signal EN L18 was once again blocked during the time the "D" flip flop was set. This action prevented the Micro Roms from stepping out of the idle loop into the program.

The Start flip flop is cleared by the "K" flip flop resetting. This action unblocks the H202 preset control flip flop (U212-5) and the Clr D latch. The first $\overline{H202}$ decoded from the Micro Rom output in the idle loop after the "K" flip flop resets will preset the H202 preset control flip flop (U212-5). The primary function of H202 is to obtain the next instruction for listing.

The Advance (Adv 200) signal goes low and sets the H200 flip flop, and the H201 flip flop sets, clearing the H200 flip flop. The "D" flip flop will be preset, and the first instruction will be loaded into the Z counter.

The signal $\overline{F202}$ will go low at T1 time as the Micro Rom steps around the idle loop. The signal $\overline{L18}$ will then go low the first time $\overline{F202}$ goes low after the "D" flip flop is preset. The signal L18 going low increments the ROM address counter and allows the ROM to be stepped out of the idle loop and into the keyboard input routine. At T4 time of the next "T" time cycle, the signal $\overline{F403}$ (U523-4) will go low and the output of the Z counter will be loaded into the Macro Rom input register.

With the signal $\overline{F403}$ low into gate U207-6, the Clr "D" latch will set and clear the $\overline{H202}$ preset control flip flop (U212-5). The next character will now be blocked until the one already transferred has been printed. The Micro Rom will not return to the idle routine to accept the next instruction until the current instruction has been printed.

MACRO ROM INPUT REGISTERS (Reference List #2, Figure 2-16.)

The Macro Rom input registers for keyboard data are U422 and U414. The selection of the Rom to be addressed is by U416 in the List mode of operation. The Micro Rom output 223 will cause the signal $\overline{F301}$ to remain high. $\overline{F301}$ high selects pins 1, 4, 6, and 7 of the three gates listed above. These inputs are latched to the outputs when $\overline{F403}$ goes high. $\overline{F403}$ going high makes the clock signal L24 transition low and the data is latched.

The Micro Rom output steps to 224. $\overline{F304}$ goes low and inputs 2, 3, 5, and 12 of U410 and 415 are permissed. $\overline{F404}$ goes low at T4 time and the clock signals for the two listed components goes high. The data is set when $\overline{F404}$ goes high at the end of T4.

The Micro Rom steps to 225. $\overline{F305}$ will go low and inputs 2, 3, 5, and 12 of U405 U408, and U409 will be permissed. $\overline{F405}$ will go low at T4 time and the clocks L31 and

2-9.0 LIST OPERATING MODE (Cont.)

L32 will go high. They will transition low at the end of T4 time and the data will be set.

The Micro Rom steps to 222 and the address will be latched in the Macro Rom Address counter and the Macro Rom Enable Selectro latch. $\overline{F402}$ will go low at T4 time of the 222 timing cycle, and the address and selection of the Macro Rom will be latched.

The signal $\overline{F402}$ going low also sets the Macro Rom Strobe flip flop. *V_{GG} goes low and will remain low until the Strobe flip flop is reset. V_{GG} low allows the inputs to the Macro Rom to be decoded in the Rom and coupled to the inputs of the Rom instruction latch.

SAMPLE (U511-4) is made high at T7 time and the clock inputs to the Macro Rom Instruction Latch goes low. The clocks transition high at the end of T7 and the Rom output is latched. The instruction will change at T4 time of the next instruction cycle. The Strobe flip flop will be cleared at TØ time and V_{GG} going high blocks the Macro Roms. Sample will go low, blocking the Instruction Latch clock. Instruction will remain latched until the next $\overline{F402}$.

The Micro Rom steps to 203. $\overline{F100}$ goes low and at T1 time, $\overline{F203}$ goes low. $\overline{F203}$ makes $\overline{L17}$ low at gate U525-11. $\overline{L17}$ clears the Micro Rom Address Counter Bit 1 flip flop, and loads the new address from the input latch. $\overline{F203}$ also clears the Carry flip flop (U530-5), loads PØ, P1, and P2 outputs from the Macro Rom Instruction Latch into U630, and clears the Ram output registers A, and B (U619 and U626).

* ROM enabling voltage

2-10.0 EDIT FUNCTION

2-10.1 DELETE MODE

Delete is one-half of the Edit function. Insert is the other half and will be covered under its own heading.

The purpose of the Delete function is to remove instructions from a program so that it may be corrected. Erroneous or redundant instructions are removed with the use of Delete.

Depression of the Delete key follows a one step listing of the stored program. The program is listed one step at a time until the unwanted instruction is printed. Reset is then depressed, returning the machine to the Keyboard Mode.

The Marker Counter is retarded each time the one-step List Mode operation is performed, syncing the Marker counter to the instruction to be deleted.

Depression of the Delete key will result in the recognition of the delete operating mode. The logic action will ultimately result in the signal Delete (H304), going low. The following logic levels will be established and remain so until the signal Delete becomes high by either completing the delete function or depression of the Reset key.

U221-3 functions as a Marker Counter Clear gate for both Delete and Insert functions. It is also used to clear the Marker Counter on the first Null after the unwanted instruction has been deleted. U221-3 becomes a high and remains so until H304 becomes a high.

The Marker Counter cannot be cleared until after the Delete or Null flip flop (U206-9) sets. The signal H214 going high clears the flip flop and Delete into gate U221-6 blocks the clock to prevent unwanted clearing of the Marker Counter.

The H304 signal Delete (U220-6) going high, unblocks gate U223-11 and U229-8. This will allow U208-8 to be preset and then reset. It also allows the automatic reset function to take place.

The Start key is depressed and the following actions take place:

The "K" and "D" flip flops will set, the signal En L18 will be blocked and the Start One-Step flip flop (U204-9) will be set.

The Start flip flop will set the clear "D" latch and reset the "D" flip flop. The Start flip flop will also prevent the reset of the Mode Clear flip flop (U203-8) until after the Start key is released.

The output of gate U225-12 will go low at T7 time after the "D" flip flop is cleared at T6 time. It will go low every T2 and T7 time thereafter, until Y5 latch is reset. U211-1 will go high when 1st Data is decoded. U223-11 will go low and U208-8 will be preset. H203 and H204 go high and will remain high until U208-8 is reset.

H203 and $\overline{\text{H204}}$ high cause U107, U113, and U106 to accept data from the delayed Data Registers for input to the shift registers.

The Marker Counter sets the H200 flip flop, U233-12 at the end of the next TØ or T4 time. The output of gate U229-8 goes low and the output of gate 221-8 goes high, per-

2-10.0 EDIT FUNCTION

2-10.1 DELETE MODE (Cont.)

missing the reset of U208-8. The Mode Clear flip flop (U203-8) is also permissed to set.

The instruction to be deleted counts out of the shift registers at T1 or T6 time, following the permiss to reset U208-8. On the following trailing edge of TØ or T4 time, the instruction will count into the Delayed Data Register. Then, U208 will reset, causing U215-6 (Data Select A) to go low. All other data will now go to the shift registers directly instead of through the Delayed Data Registers (U114 and 112).

The unwanted instruction has been left sitting in the Delay Register and will be lost. The Mode Clear flip flop will also set on the same TØ or T4 that loads the instruction into the delay circuits. The Mode Clear flip flop (U203-8) will clear the Y5 latch, the Program Mode Selector Latch, and Program Decoder. The machine will be returned to the Keyboard Mode.

Another instruction can now be deleted, if desired, because the Marker is sitting on the next instruction in line. Otherwise, the operator may start another operation if she chooses.

2-10.0 EDIT FUNCTION

2-10.2 INSERT MODE

The Insert Mode is used to add instructions to an existing program as part of the Edit function. In using the Insert Mode, entire routines or sub-routines may be added at locations within the program selected by the operator. When used in the edit function, Insert is used to either replace erroneous instructions removed by Delete, or to enter instructions omitted in the original loading of the stored program. In reality, Insert Mode enables a "Write" operation at a selected location in a program that is already stored. Therefore, many of the logic functions are identical to those of the Write Mode.

Depression of the Insert key takes the machine out of the manual mode and sets up logic levels that will remain as constants until cleared by the depression of the Reset key.

To reach the position in the program in which the new instruction is to be inserted the machine is placed in a "List" operating mode, and then one-stepped until the instruction immediately preceding the insertion location is printed and then Reset. The Marker Counter is now zeroed at the insertion point. Depressing the Insert key will then set up the logic constants and the new instruction can be keyed in as desired. The new instruction is written into the area indicated by the Marker Counter and the Marker Counter will be retarded one step. Repeated instruction entries can be made to build a new routine, sub-routine, or replace instruction(s) removed by Delete.

INSERT LOGIC

Depression of the Insert key will result in the key being decoded in the multiplexer and de-multiplexer (U124 and U126). The signal "K" out of gate U118 will go high permissing the set of the "K" flip flop. The "K" flip flop being set will block the Z counter and initiate the bounce delay flip flops (U407-11 and 407-15). The bounce delay timing out will set the "D" flip flop. The signal H210 out of gate U426-8) will go low when the "D" flip flop sets, loading the code for Insert (3) into the Program Mode Latch (U227) and disabling the Program Mode Decoder (U222). The signal H210 going low will also set the Clr "D" latch (U125-3 and U117-3).

The Program Mode flip flop (U212-9) sets when the Program Mode Latch (U222) is disabled. It will remain set as long as the "K" flip flop is set. The "D" flip flop will be cleared at T6 time and the signal H210 will go high. H210 high enables the Program Mode Decoder (U222) and latches the Insert Code into the Program Mode Latch (U227). The signal H303 now becomes a constant low.

The signal H214 out of the Program Mode flip flop U212-9 is used to clear the Delete or Null flip flop (U206-9). The signal EN L18 is also blocked and will remain so until the machine is returned to the manual mode.

Release of the Insert key will allow the Program Mode flip flop (U212-9) to reset. The signal H214 will go low. 1st Data will clear the False 1st Data flip flop (U226-9) and it will remain cleared.

2-10.0 EDIT FUNCTION

2-10.2 INSERT MODE (Cont.)

With the signal $\overline{H303}$ low into gate U223-3, the output signal H228 becomes a constant high. H228 is inverted low by gate U218-2 and $\overline{H228}$ will be a constant low. Gate 219-3 sets the Y5 latch and gate 225-8 sets the False 1st Data flip flop U226-9.

A key representing an instruction is depressed. The key is decoded and the "D" flip flop will be set. 1st Data decoded after the set of the "D" flip flop will preset the H202 flip flop (U204-5) due to the action of gate U217-12.

The Marker Counter will count to zero in the position designated for insertion. H201 flip flop (U233-9) will set and H200 flip flop (U233-12) will be cleared at the end of TØ or T4 time.

The signal $\overline{H218}$ out of gate U217-6 will go low and U211-13 will go high. $\overline{H204}$ will go low and data will be entered into the shift registers from the Z Counter. $\overline{H218}$ going low permissed the set of the Delete/Insert flip flop U203-8 via gate U230-1.

The TØ or T4 that resets H201 flip flop (U233-9) and the H202 flip flop (U204-5) will set the Delete/Insert flip flop (U208-8). The signal H204 will then return to its normal high condition and H203 will be high for the balance of the data pass.

The signals $\overline{H203}$ and $\overline{H204}$ (U215-6 and U205-1) being high causes all of the instructions in storage, after the insert is completed, to be routed back to the shift registers via the Delayed Data Registers (U112 and U114).

Since the Marker Counter was retarded one count when the H201 flip flop set via gate 224-11, it is now pointing to the position immediately following the last inserted data.

The first null out of the shift registers permisses the reset of the Delete/Insert flip flop (U208-8). The next TØ or T4 will reset the flip flop and H203 will be made low at gate U215-6. Data will now be routed from the output of the shift registers to the input of the shift registers directly. The insertion of one instruction is complete. All other insertions of instructions are accomplished in the same manner. Depression of the Reset key causes the machine to return to the manual mode.

2-10.0 EDIT FUNCTION

2-10.2 INSERT (Cont.)

INSERT

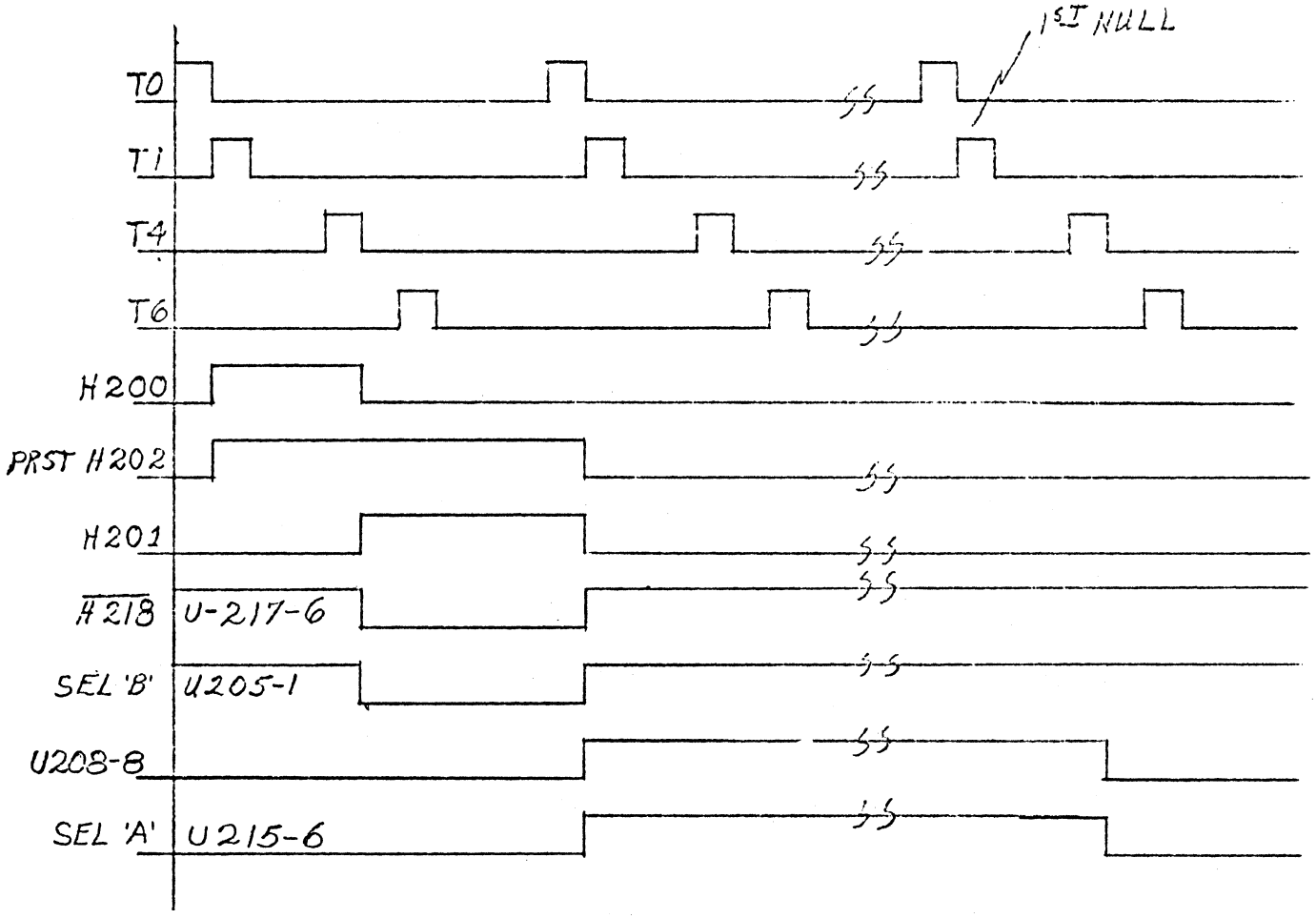
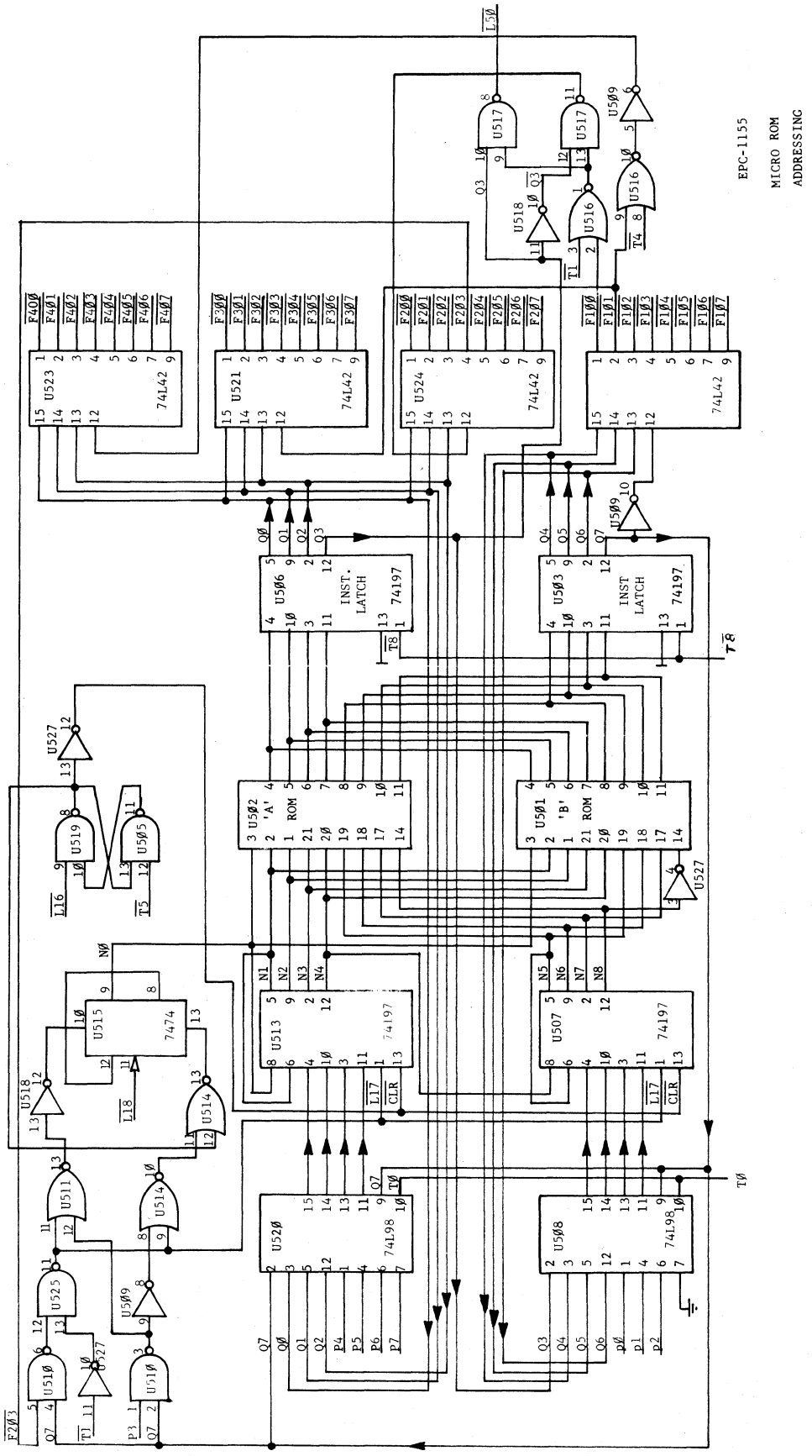


FIGURE 2-17


EPC-1155
MICRO ROM
ADDRESSING
INST. LATCH
74197
74L42
74L98
7474
ROM
'A'
'B'

2-11.0 OPERATIONAL TIMING FOR THE MICRO ROMS

The "T" Counter is the key on which the Micro Roms and their attendant circuitry function.

The output of the Micro Roms is latched in the Instruction Latches at the beginning of T8 time. The bit "0" flip flop is clocked, incrementing the Rom Address Counter and changing the address bit "0" at the end of T8.

The Rom latch output will be stored in the two Address Selection Registers, U508 and U520, unless a branch is required. This loading will be at the end of TØ time.

The output of the Macro Roms will be loaded into the Address Selection Registers at the end of TØ time if a branch is required.

The determination of the address to be stored at the end of TØ time is made by the Micro Rom instruction bit 7. It will select the Branch instruction from the Macro Rom Instruction Latches if the seventh bit is high, or it will select the Micro Rom Latch output if the seventh bit is low.

The instruction will be stored until the end of the next TØ time. It will be changed to the next selected instruction at that time.

The Micro Rom bit Ø address flip flop provides an input to the Ø address input of the selected Rom and clocks the Rom address counter.

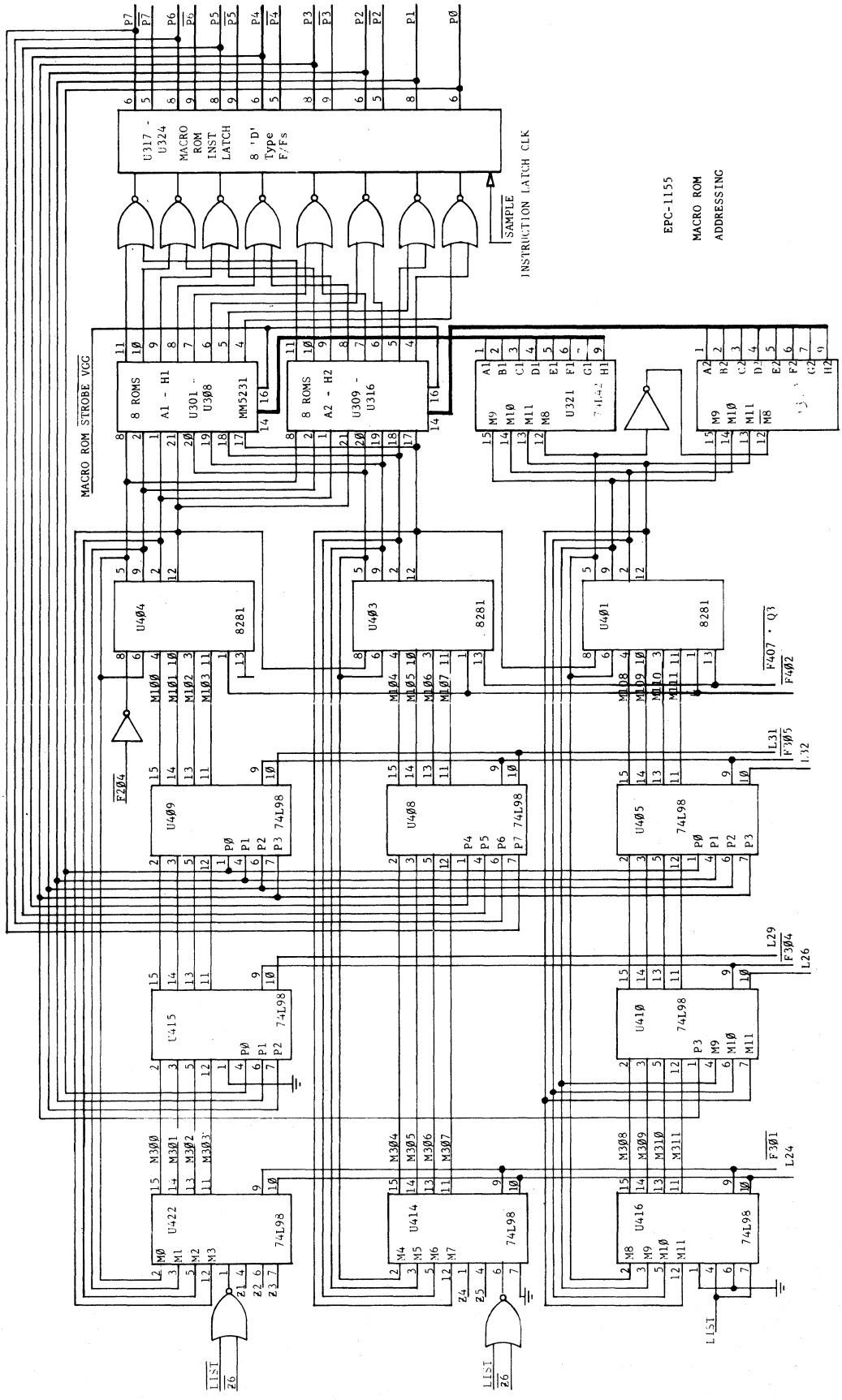
Normally, the Bit Ø address flip flop is clocked at the end of T8. However, it may be cleared or preset at T1 time, or it may be clocked one additional time in this timing cycle at the end of T1. This additional clocking will cause two addresses to appear at the inputs to the Micro Rom in one "T" timing cycle. The one present at the beginning of T8 will be the one set into the Rom instruction latch. Thus, one instruction has been skipped.

One other condition would cause a skip to occur at T4 time. A test is made to determine the status of the printer. The Bit Ø flip flop is made to skip an instruction if the printer is busy. The signal: Printer Busy (F) and Test Printer Busy (F400) are combined in U514-1 for the test.

The skips at T1 time are generated by successful tests as is the one at T4 time.

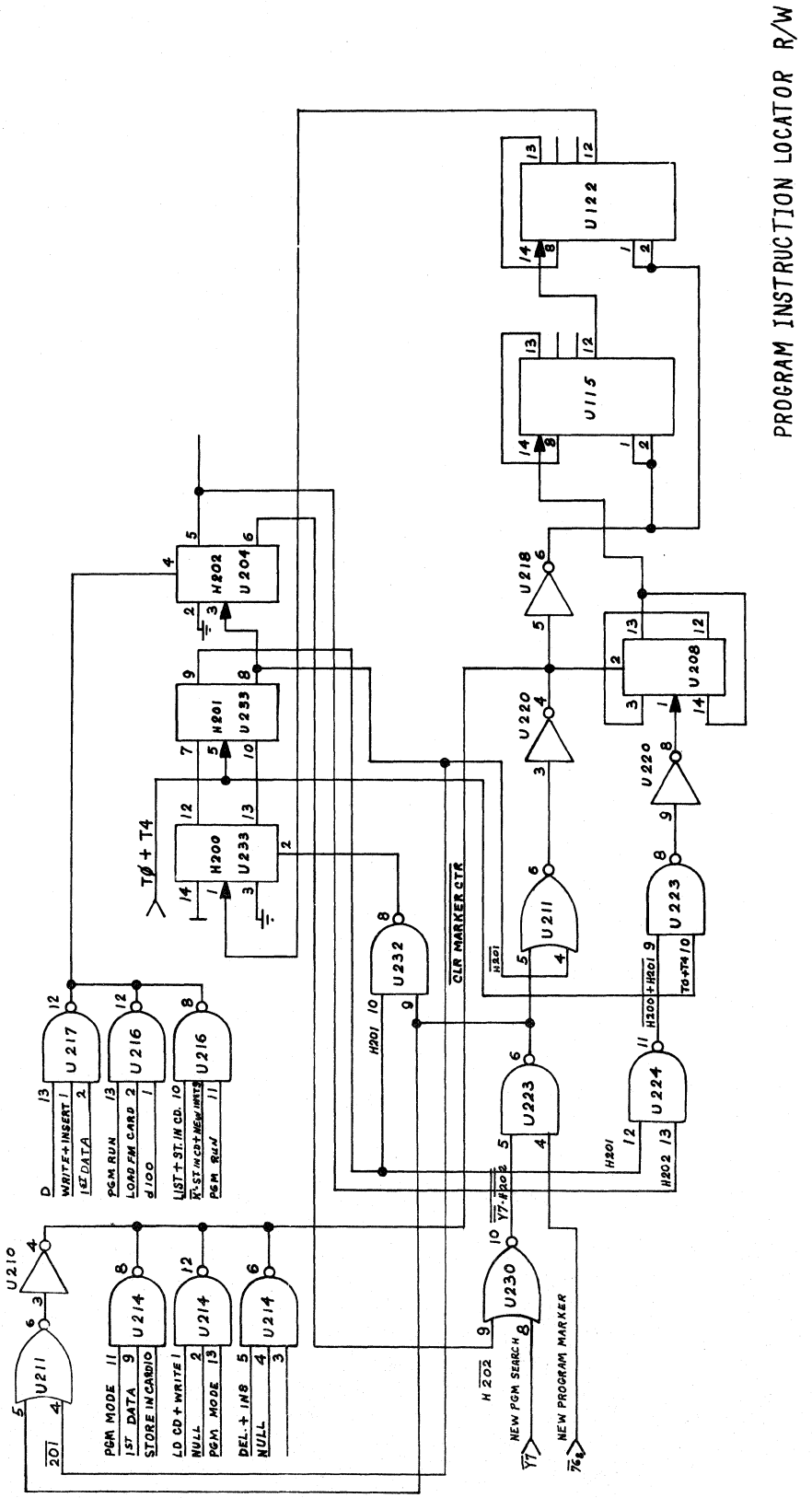
A test to check the status of the Carry flip flop is made when arithmetic is being done. The signal Carry Set (C)is combined with the signal Test Carry Set (F201) in gate U516-4. The Bit Ø flip flop will be clocked at the end of T1 time if the Carry Flip flop is set and a skip will be done.

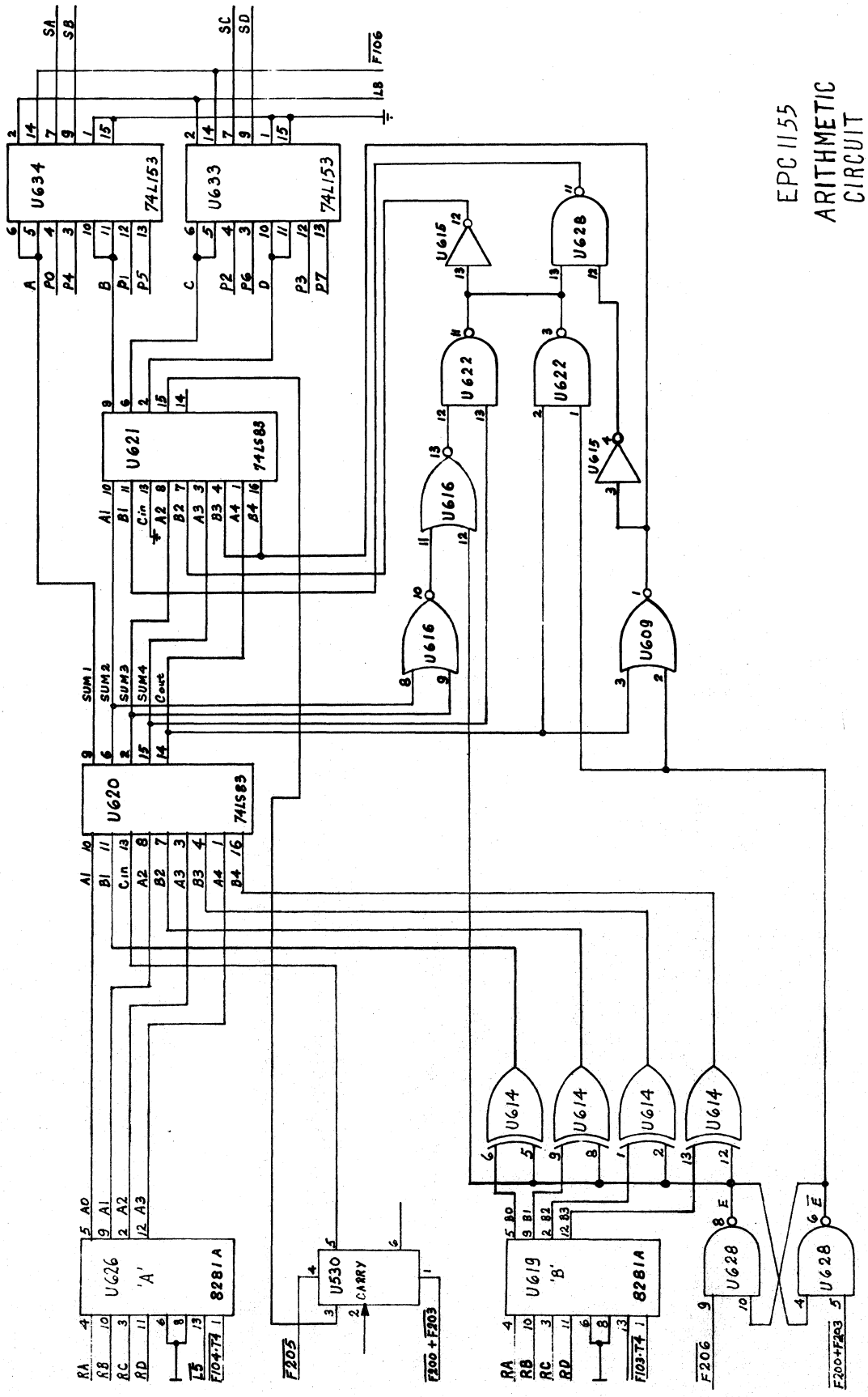
The final test to bring about a skip determines whether or not a keyboard entry, either program instruction or data, is being made. The skip will not take place unless En L18 is low. En L18 will be made low when the machine is in Manual or Run From Program mode if the Start, One Step, or a program key is not depressed. It will also go low when in the List Program Mode and no other program key, the Start key, or the One Step key is depressed.


EPC-1155
MACRO ROM
ADDRESSING
U317 - U324
MACRO ROM INST LATCH
8 'D' Type F/Fs
SAMPLE
INSTRUCTION LATCH CLK
MACRO ROM STROBE VGG
8 ROMS
A1 - H1
U301 - U308
MM5231
8 ROMS
A2 - H2
U309 - U316
U321
U4Ø4
U4Ø3
U4Ø1
8281
U4Ø9
U4Ø8
U4Ø5
U415
U41Ø
U422
U414
U416
74L98
F2Ø4
F4Ø7 · Q3
F4Ø2
L31
F3Ø5
L32
L29
F3Ø4
L26
F3Ø1
L24
LIST
26

PROGRAM INSTRUCTION LOCATOR R/W

EPC-1155




EPC 1155
ARITHMETIC
CIRCUIT
U634
U633
U621
U620
U622
U614
U615
U616
U628
U609
U626
'A'
U619
'B'
U530
CARRY
8281A
74LS83
74L153
F106
F205
F206
F200+F203

2-12.0 PRINT LOGIC

A two digit print control code is used to determine the action to be taken by the printer. The Most Significant Digit is transferred to the Ram "B" (U619) output register and determines whether or not a character will be printed or another action will take place. If a print function is to be initiated, a "1" will be transferred to Ram "B" and the motor will start. A "2" will cause the carriage return/line feed function to be activated. A "3" will be loaded into Ram "B",if the Clear Entry key has been depressed, and the "Spin" latch will be set causing the Motor Spin to be initiated. If the number in Ram "B" is a 4, 5, 6, or 7, the motor has already started, the carriage has started to move, and a character will be printed.

If a "0" is loaded into Ram "B", the signal L70 will go low and the Y4, Y5, Y6, or Y7 latches will be either set or reset.

The Least Significant Digit of the print control code will be transferred from Register 3 to Ram Output Register "A" (U626). The outputs of both "A" and "B" will be transferred to the Print Counter Register if the number in "B" is a 4, 5, 6, or 7.

The "Y" control decoder (U418) will cause the setting or resetting of one of the "Y" latches if the number in Ram "B" is "0". The number in the "A" register determines which of the "Y" latches will be set or reset. The Chart, Page 2-53, shows the Print Control Output Codes.

All print action begins with the signal Motor Start (U629-6) going high, as a result of any one of the 3 inputs to U629-6 going low. Depressing the Paper Feed Switch causes the signal Paper Feed to go low. However, since the signal Paper Feed is the result of manually depressing a switch, no print action will occur. The other two inputs are the signals, Spin; and SO.

A normal print function is initiated by a "1" being transferred from Register Ø to the Ram Output Register "B". The "1" will be latched in the register and decoded in the "B" Output Register Decoder (U618) when the signal L50 goes low. L50 will go low when Q3 of the Micro Rom instruction is high, and F100 is a low signal. The instruction is 210_8.

The signal $\overline{\text{K3009}}$ will go low for one "T" time. The output of U622-8 will go high into the clock input of the Zone Counter (U611). The Zone Counter was cleared on the last depression of the Reset key.

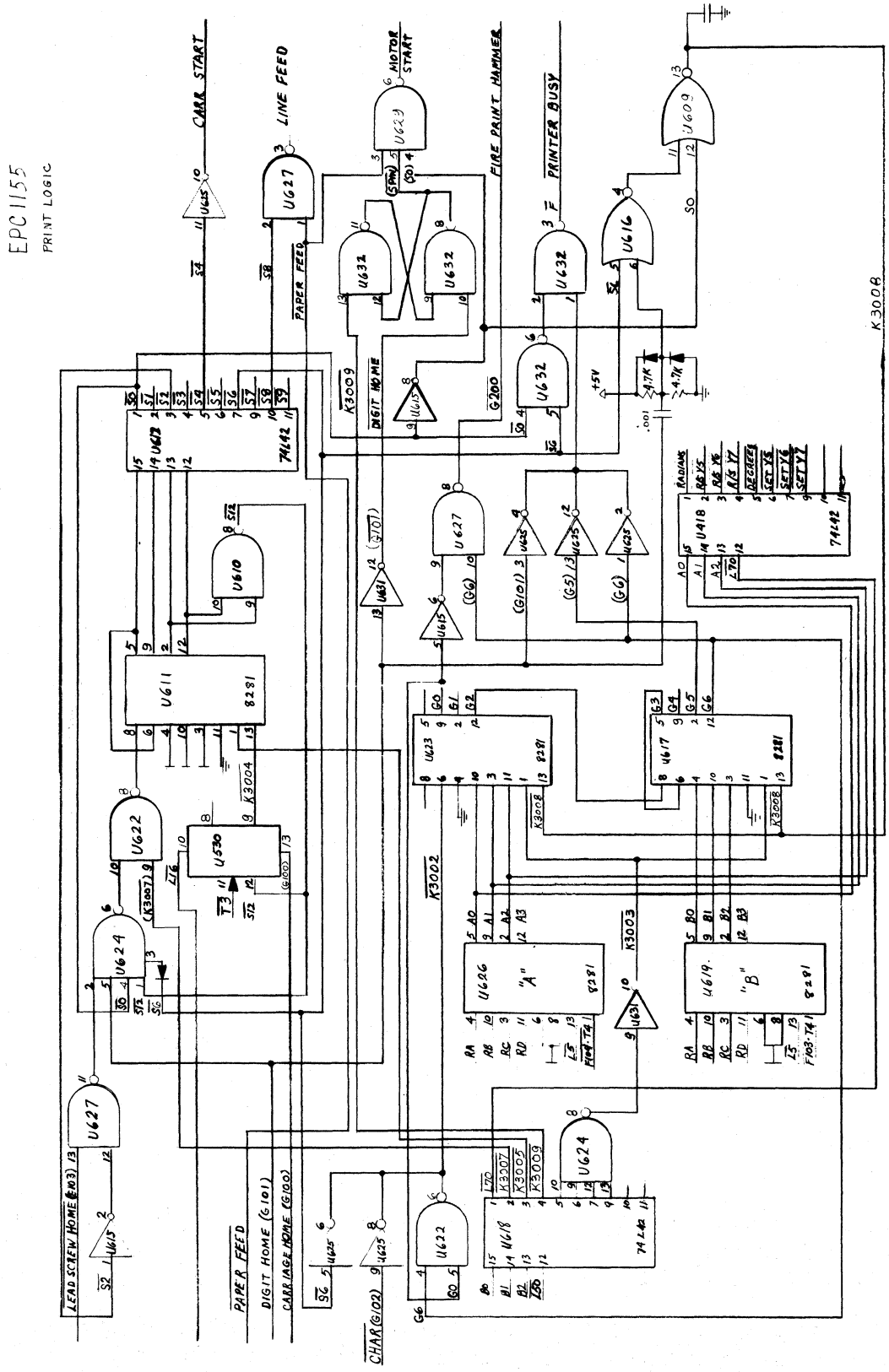
The signal $\overline{\text{K3007}}$ will go high at the end of T1 time and the output of U611 will step to "1". The signal $\overline{\text{SØ}}$ will go high and SØ will go low. The motor will start and continue to run until the Zone Counter is at zero once more.

The signal $\overline{\text{Printer Busy}}$ blocks a skip in the stepping of the Micro Rom until the Zone Counter steps to six.

All inputs to gate U624-6 are high with the exception of the digit home input. The digit home input will go high when the probe is rotated past the pickup coil. The Zone Counter U611 will step to "2" when the signal Digit Home goes low once more.

When the signal $\overline{\text{S2}}$ goes low into inverter U615-2, and the output of gate U627-11 goes low when the signal Lead Screw Home goes high, the Zone Counter steps to "3". The output of gate U627-11 will be high once again.

2-12.0 PRINT LOGIC (Cont.)



2-12.0 PRINT LOGIC (Cont.)

The Zone Counter steps to "4" at the end of the next Digit Home and the signal Carriage Start goes high. The pin is set in the helix and the print wheel begins to move across the paper. The next Digit Home pulse steps the Zone Counter to "5", and the signal S4 goes high. At the end of the next Digit Home, the Zone Counter steps to "6". The signal S6 going low clamps the output of gate U624-6 high and all the characters to be printed will print during the time S6 is low. The signal K3002 is also unblocked when S6 is low

CHARACTER PRINT

Characters are printed in the following manner. The code for a digit, symbol, or letter is transferred to the Ram Output Registers A and B. The most significant digit will be transferred from Register Ø, and the least significant digit will be transferred from Register "3". Register Ø will go to R.A.M. "B" register and register "3" will go to R.A.M. "A" register.

The output of the RAM output register "B" (U619) will cause the Load signal $\overline{\text{K3003}}$ to go low and the most significant digit is loaded into U617 (one-half of the Character Counter) while the least significant digit is loaded into the other half of the Character Counter (U623).

The Character Counter increments once each time a probe on the character wheel passes the Character pickup coil. The Print Hammer will be fired when the Character Counter has a count of 100_8. The Character Counter will always step once more than the output code preset into the Character Counter, i.e., a "1" is represented by the output code 76_8. Two counts are required to step the counter to 100_8 and fire the print hammer. The character must be printed before the end of the next Digit Home. When Digit Home goes low, a negative going pulse is developed on pin 6 of U616-4. The signal S6 is low on pin 5 of U616-4 and U616-4 goes high causing K3008 to go low for the duration of the developed pulse. With the signal K3008 low, the Character Counter is cleared. The Character Counter will then remain at 100_8 for one character time on the timing wheel. During this time, the signal Fire Print Hammer will be low. The Character Counter will step to 101_8 on the next character pulse, and the signal Fire Print Hammer will go high. The signal G6 and GØ will go high and block the Character Counter clock until the Character Counter is cleared by K3008.

The next character to be printed will be loaded into the RAM output registers and then loaded into the character counter. The counter will count from the code loaded until the count reaches 100_8 and the Print Hammer will be fired again. The print cycle will continue until all characters have been printed. Instruction $21Ø_8$ will load a "2" into the RAM Output Register "B". The "2" will decode as K3005 and will preset the Zone Counter to "7".

With the Zone Counter preset to "7", the signal $\overline{\text{Printer Busy}}$ will go high and block the skipping of the Micro ROM Address Counter until a new print cycle is initiated. The signal S6 high also blocks the Character Counter Clock and permisses U624-6 to function as one of the Zone Counter Clocks.

The next Digit Home pulse will step the Zone Counter to "8", causing the signal Line Feed to go high, the paper to be advanced, the pin to be retracted, and the

2-12.0 PRINT LOGIC (Cont.)

carriage to return home. The Digit Home pulses will continue to step the Zone Counter until a count of "12" is reached. At that time, the Zone Counter Clear flip flop will be permissed to set and it will set on the next T3 time, clearing the Zone Counter.

The signal $\overline{S\emptyset}$ now goes low, and the signal Motor Start goes low stopping the motor. The Printer Busy gate U632-3 is also unblocked by SØ going low. The signal K3008 going low clamps the Character Counter clear.

The print cycle is now complete and waiting for the initiation of the next print instruction.

2-12.0 PRINT LOGIC (Cont.)

1155 PRINT CONTROL

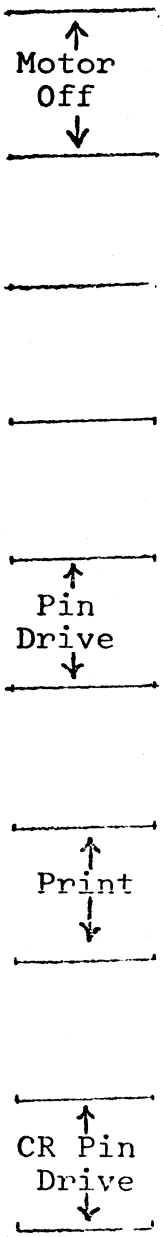
OUTPUT CODES

BA 03		BA 03	
77	0	57	L
76	1	56	I
75	2	55	C
74	3	54	X
73	4	53	E
72	5	52	P
71	6	51	O
70	7	50	T
67	8	47	D
66	9	46	Q
65	.	45	N
64	+	44	R
63	-	43	S
62	÷	42	A
61	G	41	SPACE
60	F	40	SPACE
27		17	
26		16	
25		15	
24		14	
23	CARRIAGE RETURN	13	PRINT START
22		12	
21		11	
20		10	
37		07	SET Y7
36		06	SET Y6
35		05	SET Y5
34		04	SET Y4
33	SPIN	03	RESET Y7
32		02	RESET Y6
31		01	RESET Y5
30		00	RESET Y4

The MSD comes to B from R0. The LSD comes to A from R3.

2-12.0 PRINT LOGIC (Cont.)

PRINT CYCLE -



0

COUNT TO 1 ONE "PRINT START"

1

COUNT TO 2 ON HOME

2

COUNT TO 3 ON SHAFT REED

3

COUNT TO 4 ON HOME

4

COUNT TO 5 ON HOME

5

COUNT TO 6 ON HOME

6

COUNT TO 7 ON CARRIAGE RETURN

7

COUNT TO 8 ON HOME

8

RETURN TO ZONE 0 ON CARRIAGE RETURN REED CLOSURE.

2-13.0 MAGNETIC CARD READER

2-13.1 GENERAL

The Model 511 Magnetic Card reader is a peripheral for the Model 1155 Calculator providing permanent program storage on 2" x 8" cards with magnetic backing. Each card can hold two programs of up to 511 steps.

The card reader has no operator controls of its own, but is operated by the STORE IN CARD or LOAD FROM CARD keys on the calculator. Start of recording or playback is affected by inserting a card into the front panel slot until a switch turns on the drive motor and the card is automatically run through the reader.

All logic signals and power to the card reader run through a single cable of 21 wires, which is plugged into the rear of the calculator.

2-13.2 SPECIFICATIONS

SIZE:	8.1" wide, 9.5" long, 4.3" high.
WEIGHT:	$\sim$ 4.5#
CABLE:	30" long, 25 conductor (21 used + 4 spare), PVC jacketed.
COVERS:	Cast Aluminum and Molded Noryl SE-1 (or KHP Cycoloy) thermoplastic.
COLOR:	String, with ebony front mask, grill and bottom.
FEET:	(4) gray polyurethane thermoplastic.
POWER:	From two secondaries of (Model 1155) 115 VAC $\pm$ 10%, 60 HZ transformer. At 115 VAC input: a) 11.7 VAC, 60 HZ, 0.35A, 2.7W b) 18.6 VAC, 60 HZ, 0.17A, 1.6W (IDLE) 0.40A, 5.1W (RUNNING)
POWER SUPPLIES:	a) +5 VDC, 5% regulation, 200 ma b) -12.5 VDC, 7% regulation, 200 ma fused 3/4A, slo blo.
LOGIC:	+5 V_{cc} DTL & TTL
MAGNETIC HEAD:	4 - track record - play head.

2-13.0 MAGNETIC CARD READER (Cont.)

2-13.2 SPECIFICATIONS (Cont.)

RECORD SCHEME:	6 parallel bits separated into 2 groups of 3 bits and recorded on 3 data tracks; fourth track used to record a CLOCK signal.
RECORDING SYSTEM:	NRZ (non-return-to-zero).
RECORD CURRENT:	4 milliamp.
PLAY VOLTAGE:	15 millivolts pk-to-pk.
OPERATION:	Operated by STORE ON CARD or LOAD FROM CARD keys on 1155 calculator, and by insertion of magnetic card into card chute.
CONTROLS:	None.
CARD CHUTE:	2.000 in. wide, entry in front and exit top rear.
MAGNETIC CARD:	1.997 in. wide, 8.00 in. long, 0.0085 in. thick polyester (mylar) magnetic coated card.
STORAGE CAPACITY:	3066 bits (511 program steps x 6 bits per program step); plus 1022 clock bits.
BIT DENSITY:	162.5 bits/in. ± 12 bits/in. (DATA).
MOTOR SPEED:	3000 RPM ± 60 RPM.
DRIVE WHEEL SPEED:	378 RPM ± 15 RPM.
CARD VELOCITY:	8.0 in/sec. ± 0.7 in/sec.
OSCILLATOR FREQUENCY:	42. KHZ ± 3. KHZ.
RECORD FREQUENCY:	1312.5 HZ ± 100 HZ.
STEPS:	1022 (511 program steps x 2).
RECORD TIME:	0.78 sec. ± 0.06 sec.
RECORD LENGTH:	6.28 in. ± 0.8 in.
EDGE-HEAD DISTANCE:	0.608 in. ± 0.003 in. from edge of magnetic card to nearest edge of Track 1 recording.
AMPLIFIER OFFSET:	0 Volt ± 0.15V
AMPLIFIER OUTPUT:	-0.7V minimum, ground to average negative peak.
SNR:	12 : 1

2-13.0 MAGNETIC CARD READER (Cont.)

2-13.3 OPERATION

CALCULATOR CODE:

The Model 1155 Calculator transmits to and receives from the Model 511 Card Reader a six-bit code (called Z-code). See "Model 1155 Keyboard Codes" chart on Page 2-85. Each six-bit code corresponds to one calculator machine instruction.

RECORDING CODE:

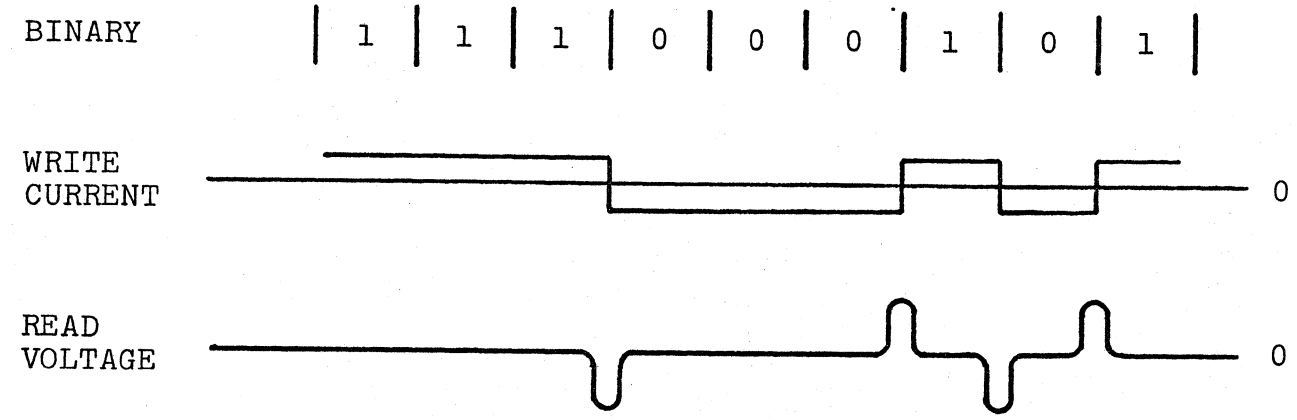
The non-return-to-zero (NRZ) coding scheme is used in the Model 511 Magnetic Card Reader (also called modified dipole). This is a level type of recording.

This coding method uses a positive current flow for the duration of writing 1's and a negative current flow for the duration of writing 0's. When a 1 is recorded, the entire cell is magnetized to plus saturation. When a series of 1's is recorded, the entire length of the tract is magnetized to plus saturation. The first 1 initiates the DC level change and subsequent 1's maintain a constant write current.

A long series of like digits records a long single magnet on the card. Polarity reversal occurs only when a 1 follows a 0 or a 0 follows a 1. The card surface is continually saturated at one polarity or the other.

The readback voltage only appears where there is a change of flux: $E = N \frac{d\phi}{dt}$, or only when a 1 follows a 0 or a 0 follows a 1.

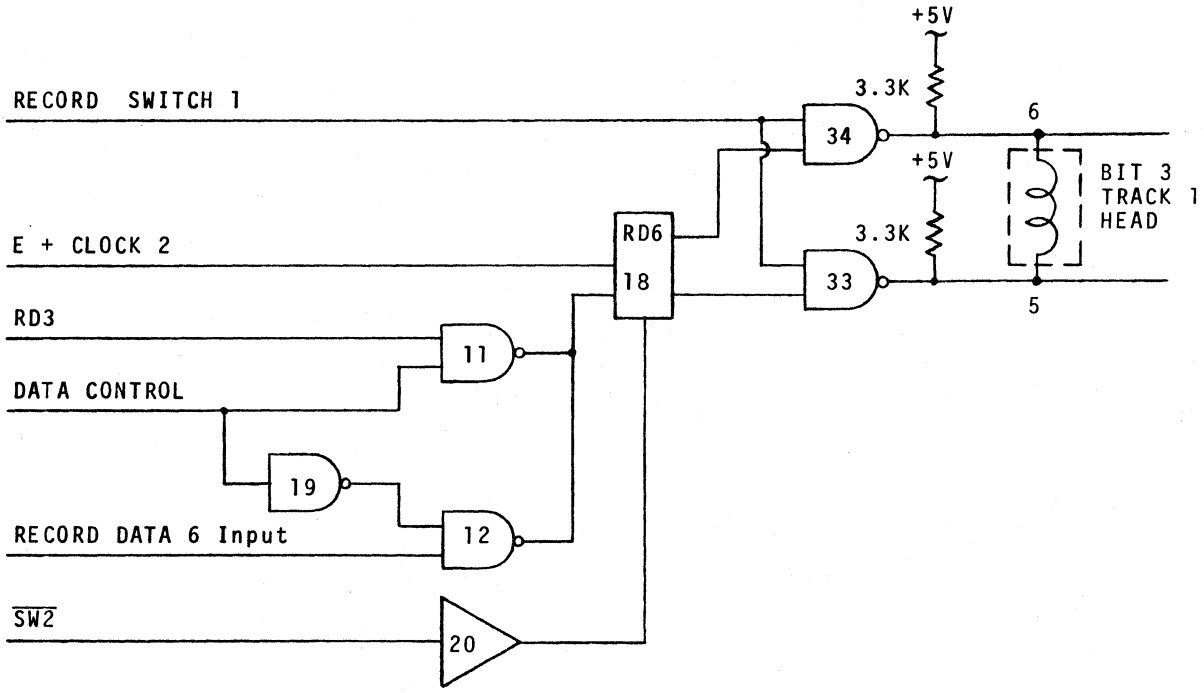
Since there is not necessarily any change of flux at each bit time, in NRZ coding, clock pulses are separately generated.



Non-return-to-zero (NRZ) coding

2-13.0 MAGNETIC CARD READER (Cont.)

BLOCK DIAGRAM
RECORD DATA 6



2-13.0 MAGNETIC CARD READER (Cont.)

2-13.3 OPERATION (Cont.)

RECORDING:

The RECORD DATA 1 to RECORD DATA 6 inputs carry the six parallel data bits from the calculator that are to be stored. Since the card reader has only three heads available for recording data (and one for recording a clock), three bits are recorded in parallel immediately and three bits are held temporarily and then recorded in parallel in the next bit location on the magnetic card.

Data is transferred and recorded at the E clock frequency of 1.25 kHz (see timing diagram). RECORD DATA 4 to RECORD DATA 6 are recorded immediately, then RECORD DATA 1 to RECORD DATA 3 bits are shifted to RECORD DATA 4 to RECORD DATA 6 and recorded.

RECORD DATA 6 will be described; RECORD DATA 4 and RECORD DATA 5 are identical. RECORD DATA 1 to RECORD DATA 3 are similar.

BIT 6, BEFORE RECORDING:

Consider that RECORD DATA 6 input signal is negative before recording. The RECORD DATA 6 (Gate 12) DATA CONTROL input is held negative and the output, or D input to RD6 flip-flop (Number 18) is positive. RD CLEAR is held negative by SWITCH 2 through Gate 20. The RD6 output is negative and $\overline{\text{RD6}}$ output is positive.

RECORD is negative and so the TRACK 1, BIT 3 Pin 5 and TRACK 1, BIT 3 Pin 6 nodes (from Gates 34 and 33) are both held positive. Current cannot flow between Pin 5 and Pin 6 of Bit 3 head since both are positive (and recording can not take place).

If RECORD DATA 6 input signal is positive before recording, the resultant (recording can not take place) is unchanged.
(See Block Diagram, Page 2-58.)

BIT 6, LEADING EDGE:

When recording is to take place, the normally positive $\overline{\text{RECORD}}$ input is forced negative by the STORE ON CARD key on the Model 1155 calculator (see timing diagram).

Some time later a magnetic card is inserted into the card reader, activating SWITCH 1. At this time, the RECORD signal goes positive permitting the outputs of the RD6 flip-flop,

2-13.0 MAGNETIC CARD READER (Cont.)

2-13.3 OPERATION (Cont.)

(which were still held by a negative RD CLEAR) to be seen at the BIT 3 head. The RD6 signal is negative and $\overline{RD6}$ is positive. BIT 3 Pin 6 at the output of Gate 34 is positive and BIT 3 Pin 5 at the output of Gate 33 is negative.

Current defined as negative to positive (from Bit 3 Head, Pin 5 to Pin 6) will record a (call it minus saturation) zero. This minus saturation is continuously recorded on the leading edge of the magnetic card before data recording, in order to initialize the leading edge. Current from 5 to 6 records a zero; from 6 to 5 records a 1.

BIT 6, DELAY:

Approximately 135 milliseconds after the motor starts and $\overline{RECORD}$ goes negative, the magnetic card activates SWITCH 2.

At this time, the RD CLEAR signal goes positive, preparing the RD6 flip-flop for RECORD DATA 6 input to be clocked. The clock is not yet turned on, so data is not yet transferred. The 10 millisecond delay is started at this time.

BIT 6, RECORDING:

At the end of the 10 millisecond delay the $\overline{DELAY}$ signal goes positive, releasing the overriding negative preset on the A and B flip-flops of the timing chain and the timing chain starts to run.

Initially DATA CONTROL will be low, unblocking Gate 12, allowing the D permiss of RD6 flip-flop to be controlled by RECORD DATA 6 input. The RD6 flip-flop will change state on the clock input as controlled by the RECORD DATA 6 input.

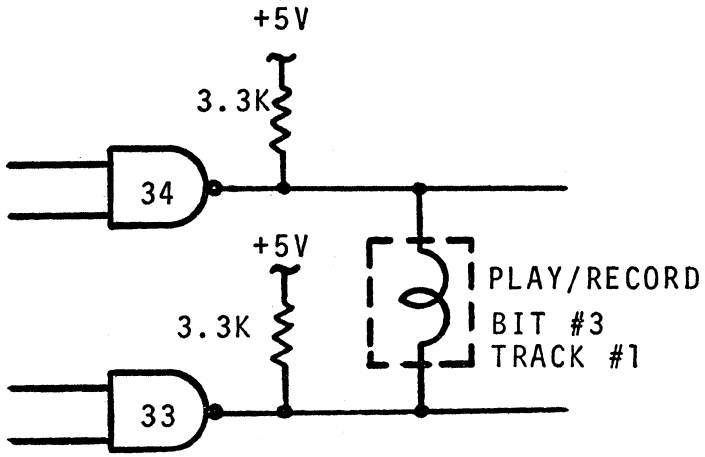
If RECORD DATA 6 input is positive, the BIT 3 Head will record a one.

At F time, DATA CONTROL will go high, blocking RECORD DATA 6 input at Gate 12, unblocking Gate 11 allowing RD6 to be controlled by RD3.

2-13.0 MAGNETIC CARD READER (Cont.)

2-13.3 OPERATION (Cont.)

RECORD DRIVERS:



The 3.3K resistors are used on the outputs of the DTL gate head drivers as current source resistors.

When the output of Gate 33 is positive and the output of Gate 34 is negative, the 3.3K resistor on the output of Gate 33 provides approximately 4 ma. head drive.

PLAYING:

The PLAY DATA 1 to PLAY DATA 6 outputs carry the six parallel data bits that are to be transferred to the Model 1155 calculator. Since the card reader has only three heads available for recording data (and one for recording a clock), three bits are played in parallel and held while the next three bits are played; then all six bits are transferred to the calculator.

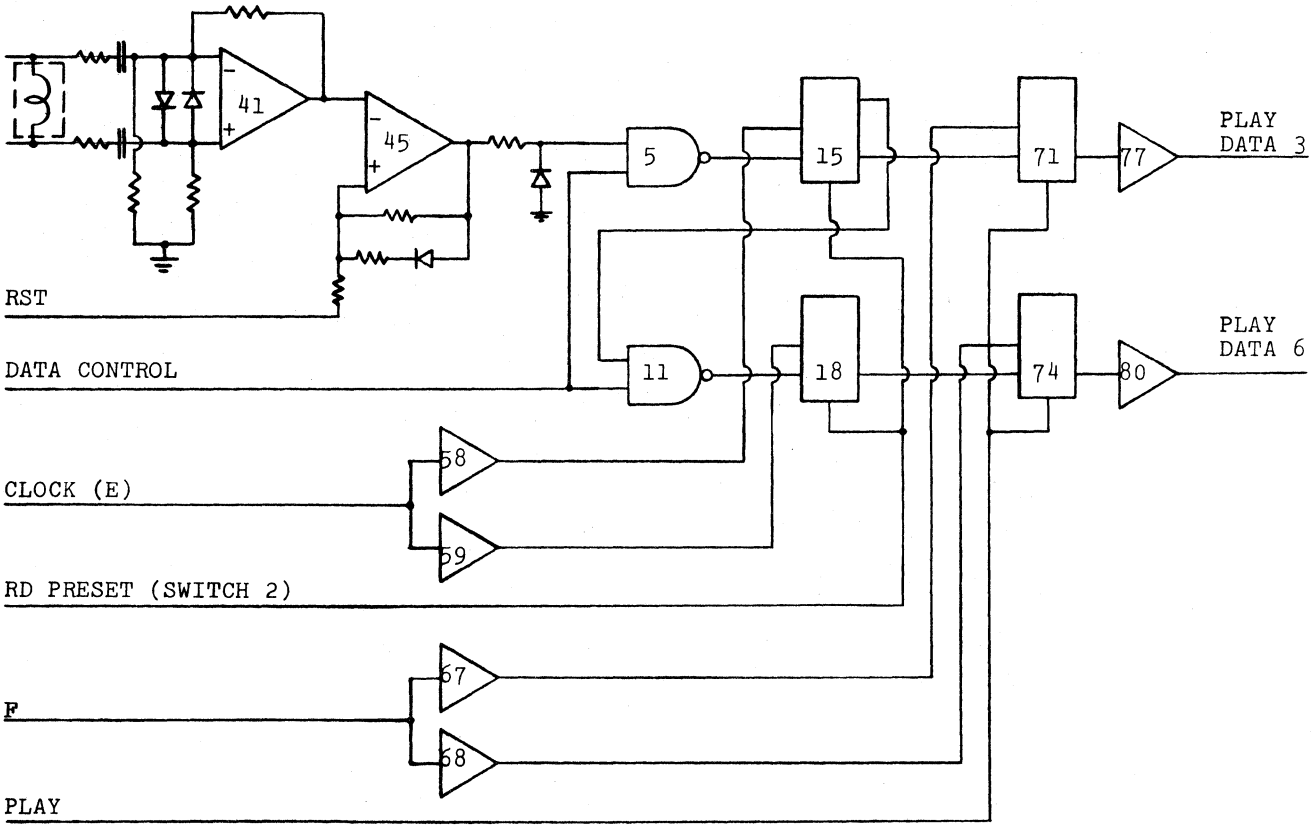
Data is transferred at the F clock frequency of 0.625 kHz from clock data recorded at the E clock frequency of 1.25 kHz (see timing diagram). Bits 4 to 6 are played and shifted to outputs PD4 to PD6, then Bits 1 to 3 are played and shifted to PD1 to PD3.

PLAY DATA 6 will be described: PLAY DATA 4 and PLAY DATA 5 are identical. PLAY DATA 1 to PLAY DATA 3 are similar. (See Play Data 6 Block Diagram, Page 2-62.)

2-13.0 MAGNETIC CARD READER (Cont.)

2-13.3 OPERATION (Cont.)

BLOCK DIAGRAM
PLAY DATA 6



BIT 6, BEFORE PLAYING:

The $\overline{\text{RECORD}}$ signal is held positive before and during playing, forcing RECORD from Gate 27 to be negative. RECORD staying negative:

(a) disables the CLOCK signal by forcing the output of Gate 49 to stay positive;

(b) forces the output of Gate 61 positive, preventing E and F from being anded;

(c) forces the output of Gate 64 positive, permitting only PLAY control of the motor;

(d) forces the outputs of Gates 29 through 36 positive, preventing recording;

(e) forces DATA CONTROL output from Gate 50 positive, blocking RECORD DATA 1 to RECORD DATA 6 inputs through Gates 2, 4, 6, 8, 9 and 12;

(f) permits transfers through Gates 1, 3, 5, 7, 10 and 11.

2-13.0 MAGNETIC CARD READER (Cont.)

2-13.3 OPERATION (Cont.)

The $\overline{\text{PLAY}}$ signal is held positive before playing, forcing PLAY from Gate 28 to be negative. PLAY staying negative:

(a) disables the CLOCK signal from Track 3 by forcing the output of Gate 48 positive;

(b) holds the motor off by forcing the output of Gate 65 positive;

(c) presets PD1 to PD6 and thus PLAY DATA 1 to PLAY DATA 6 negative.

Before playing, the SWITCH 1 signal is negative:

(a) holding the motor off by forcing the outputs of Gates 64 and 65 positive;

(b) forcing the $\overline{\text{READER BUSY}}$ signal positive through Gate 66.

(c) holding the F output of the F flip-flop negative.

Before playing, the SWITCH 2 signal is negative preventing the B, C and D flip-flops from running.

Before playing, the $\overline{\text{SWITCH 2}}$ signal is positive:

(a) holding $\overline{\text{PLAY RECORD CLOCK}}$ negative through Gate 63.

(b) holding RD CLEAR negative and clearing RD1 to RD6;

(c) holding $\overline{\text{DELAY}}$ positive.

BIT 6, START OF PLAY:

When playing is to take place, the normally positive $\overline{\text{PLAY}}$ input is forced negative by the LOAD FROM CARD key on the Model 1155 calculator. This allows the PLAY signal to go positive:

(a) permitting the played CLOCK signal from Track 3 through Gate 48;

(b) permitting the SWITCH 1 signal to control the motor;

(c) removing the clear from PD1 to PD6 flip-flops.

2-13.0 MAGNETIC CARD READER (Cont.)

2-13.3 OPERATION (Cont.)

Some time later a magnetic card is inserted into the card reader, activating SWITCH 1. The SWITCH 1 signal going positive:

(a) sends a negative $\overline{\text{READER BUSY}}$ signal to the calculator through Gate 66 to prepare the calculator to receive data;

(b) starts the motor through Gate 65;

(c) removes the clear from the F flip-flop.

The $\overline{\text{SWITCH 1}}$ signal has no effect at this time.

Since a zero is recorded on the leading edge of the magnetic card in the record mode, no changes in flux saturation are played at this time.

After approximately 135 milliseconds of card travel, the magnetic card activates SWITCH 2. The SWITCH 2 signal going positive has no effect. The $\overline{\text{SWITCH 2}}$ signal going negative:

(a) sets the RESET SCHMITT TRIGGERS positive, setting the four Schmitt triggers to negative saturation;

(b) starts the DELAY circuit, which has no effect;

(c) puts a negative input on Gate 63 which permits PLAY RECORD CLOCK through action of Gate 62;

(d) removes the overriding negative preset to the RD1 to RD6 flip-flops by making RD CLEAR positive through Gate 20.

BIT 6 PLAY:

One DELAY time, approximately 10 milliseconds, after SWITCH 2 is activated, the first recorded Bit 6 signal will be played.

Assuming that this signal is a ONE bit, a change in recorded flux direction from negative saturation to positive saturation will produce a negative voltage pulse across the inputs of the READ AMPLIFIER. This will be amplified and appear at the input to the Schmitt trigger. This negative pulse, with the Schmitt trigger preset to negative saturation, will switch the output of the Schmitt trigger to positive saturation.

This level change will appear at the D input of RD3 as a change from positive to negative after inversion in Gate 5.

2-13.0 MAGNETIC CARD READER (Cont.)

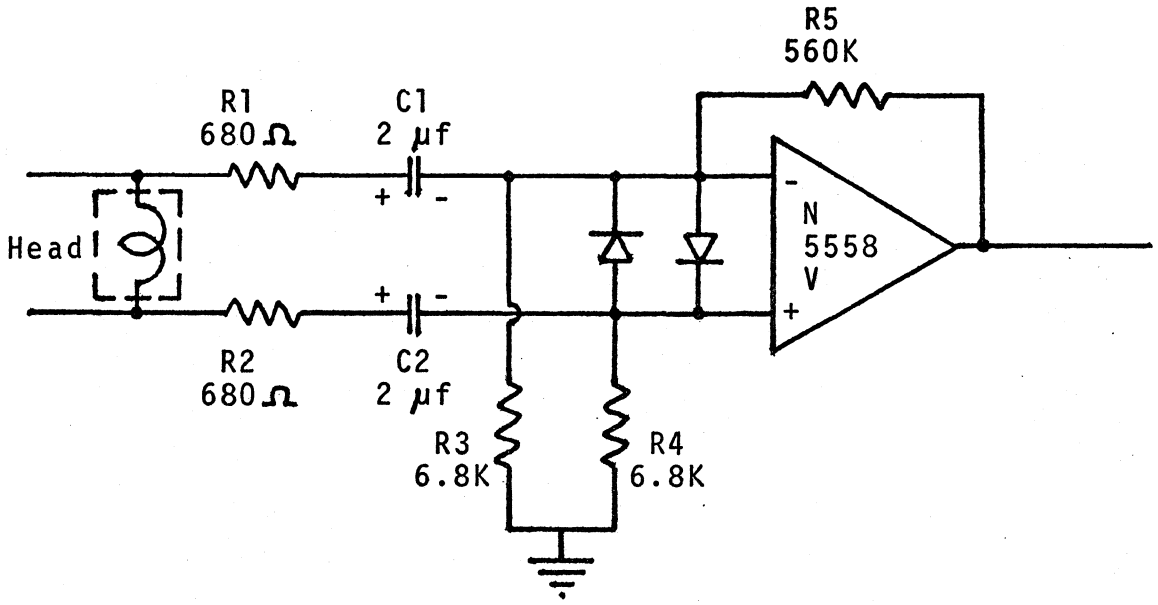
2-13.3 OPERATION (Cont.)

At the next CLOCK (E-time) positive-going edge RD3 will be clocked and the RD3 signal will change (from preset negative) to positive.

$\overline{RD3}$ going negative will be seen at the D input of PD3 and will be seen at the output of PD3 at the next E negative going edge (F-time).

RD3 going positive will be seen at the D input of RD6 as going negative after inversion through Gate 11 and be clocked into RD6 at the next CLOCK (E-time) positive-going edge, changing the RD6 signal to positive.

$\overline{RD6}$ going negative will be seen at the D input of PD6 and will be seen at the output of PD6 at the next F-time.



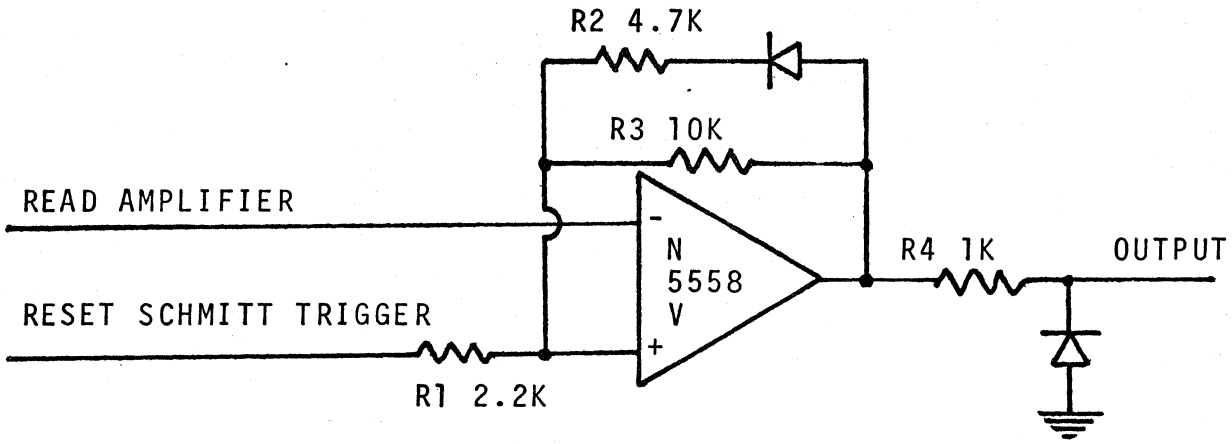
READ AMPLIFIERS:

N5558V operational amplifiers are used to amplify the low level voltage output from the heads. The two 680 ohm series impedances are high relative to X_L of the head and X_C of C1 and C2 in order to make them the predominant impedances of the input circuit. The two 2μf capacitors provide AC coupling. Two 6.8K ohm resistors are DC returns to ground for the amplifier; common mode impedances from head to amplifier. The 560K ohm negative feedback resistor and the two 680 ohm resistors provide the gain of approximately 800.

2-13.0 MAGNETIC CARD READER (Cont.)

2-13.3 OPERATION (Cont.)

SCHMITT TRIGGERS:



N 5558V operational amplifiers are used as Schmitt triggers to change the READ AMPLIFIER outputs from pulses to levels in order to restore the played signal back to the 1155 calculator coding scheme.

R1 biases the input from RESET SCHMITT TRIGGER. R2 and R3 provide positive feedback to clamp the op amp positive or negative. R4 provides output current control and the output clamp diode prevents a negative input to the DTL gate fed by the output.

The - input to the op amp is near ground. Operation of SWITCH 2 by the magnetic card sets RESET SCHMITT TRIGGER positive. The positive RESET sets the SCHMITT TRIGGER output to negative saturation.

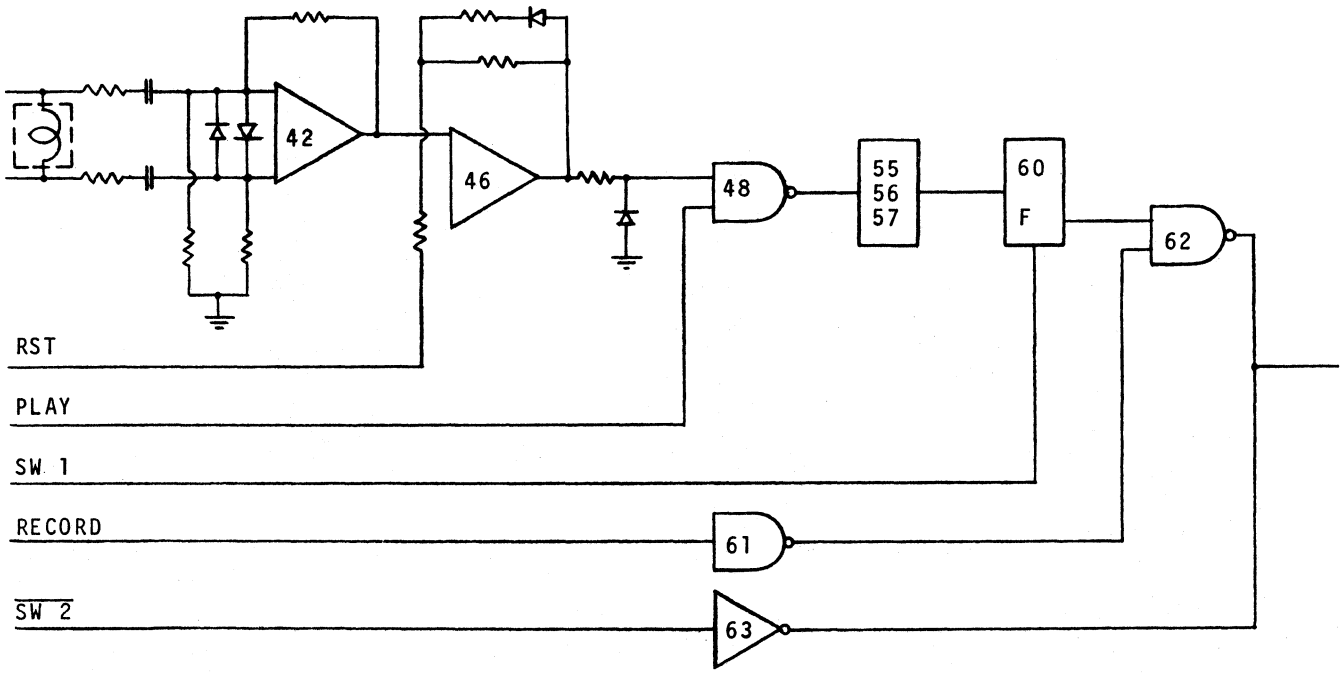
In this state a positive pulse on the - input to the op amp will have no effect on the output, but a negative pulse will switch the output to positive saturation.

With the output at positive saturation, a positive pulse in the - input will switch the output back to negative saturation while a negative pulse will have no effect.

2-13.0 MAGNETIC CARD READER (Cont.)

2-13.3 OPERATION (Cont.)

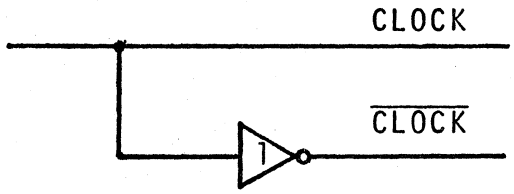
BLOCK DIAGRAM
PLAY CLOCK



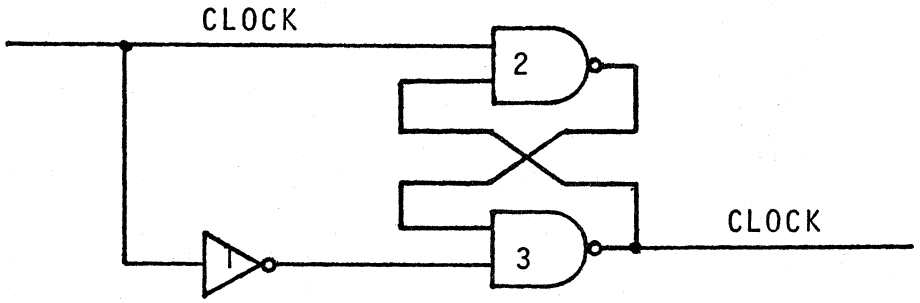
2-13.0 MAGNETIC CARD READER (Cont.)

2-13.3 OPERATION (Cont.)

This CLOCK signal is inverted:

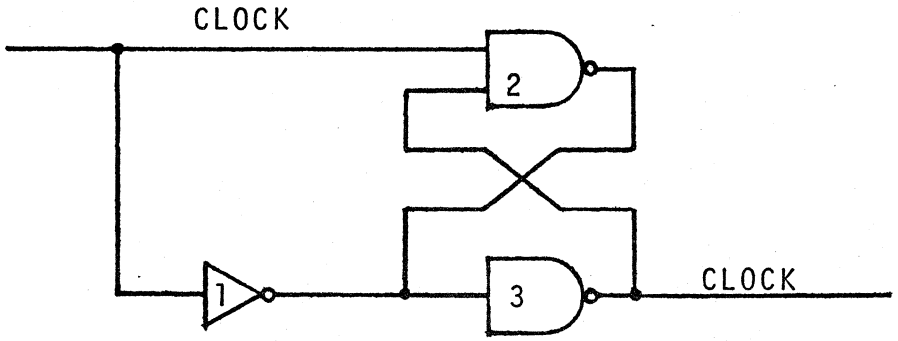


CLOCK and $\overline{\text{CLOCK}}$ are now fed to cross-coupled gates:

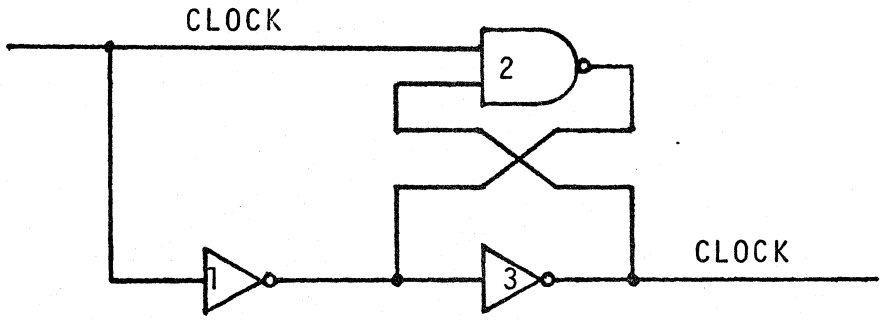


Note that Gate 1 output and Gate 2 output are negative when CLOCK is positive and Gate 1 output and Gate 2 output are both forced positive when CLOCK is negative.

Therefore, Gate 1 and Gate 2 outputs can be wire-ored:



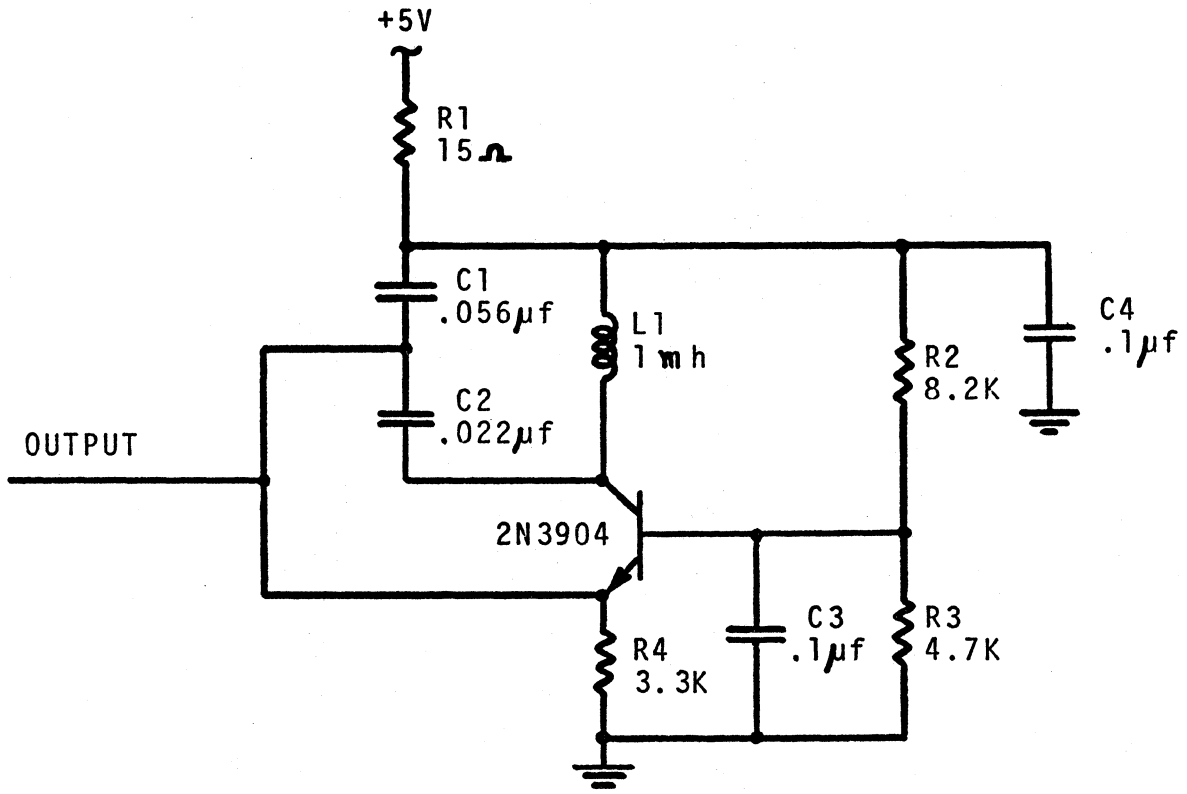
Gate 3 can now be replaced by an inverter:



2-13.0 MAGNETIC CARD READER (Cont.)

2-13.3 OPERATION (Cont.)

OSCILLATOR:



The oscillator is a Colpitts oscillator whose frequency is determined by C1, C2 and L1 where:

$$f = \frac{1}{2\pi\sqrt{LC}} \qquad \text{where} \quad C = \frac{(C1)x(C2)}{C1 + C2}$$

$C \cong .016\ \mu fd$

$L = 1$ mh

$f \cong 40$ kHz

2-13.0 MAGNETIC CARD READER (Cont.)

2-13.3 OPERATION (Cont.)

CLOCK PLAY:

Approximately one DELAY time (about 10 milliseconds) after SWITCH 2 is operated, the first recorded signal will be played.

The first recorded transition of the E clock will give a positive pulse to the Clock Schmitt trigger which will have no effect on the preset to negative saturation. The second recorded transition of the E clock will give a negative pulse to the Clock Schmitt trigger which will switch the output to positive saturation.

The PLAY signal, being positive, will permit the CLOCK signal to be inverted by Gate 48. The shaper will pass the inverted CLOCK signal to the F flip-flop. The E signal, inverted by Gate 61 and permitted by SWITCH 2 operation through Gate 63 becomes the PLAY portion of the PLAY RECORD CLOCK output to the calculator.

The clock signal is at the recorded E flip-flop rate of 1.25 kHz.

SHAPER:

The CLOCK signal shaper consists of Gates 55, 56 and 57. It is used in both the RECORD and PLAY modes, but is only required in the PLAY modes to shape the CLOCK signal from the CLOCK amplifier, Number 46. The CLOCK signal shaper output polarity follows the input polarity after a double inversion.

Inputs to the CLOCK signal shaper are:

(A) the playback CLOCK pulses in the PLAY mode from Gate 48 or;
(B) the E signal from the timing chain in the RECORD mode from Gate 49.

The shaped output from this circuit:

(A) clocks the F flip-flop of the timing chain, Number 60;
(B) drives Gate 61 at E frequency in RECORD mode;
(C) clocks RECORD DATA 1, 2 and 3 at E frequency through Inverter 67, and
(D) clocks RECORD DATA 4, 5 and 6 at E frequency through Inverter 68.

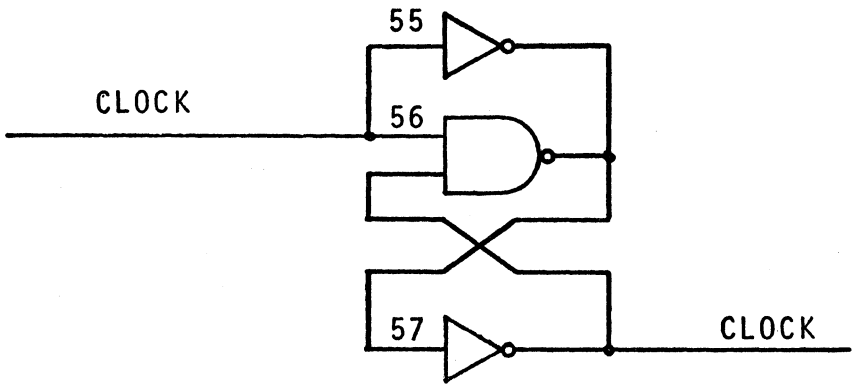
This circuit is essentially a cross-coupled two gate flip-flop, similar to the SWITCH 1 flip-flop. To explain its operation, first note that only one CLOCK signal is available in the PLAY mode:

CLOCK

2-13.0 MAGNETIC CARD READER (Cont.)

2-13.3 OPERATION (Cont.)

The circuit is now redrawn as shown on the schematic:



This shaper circuit is placed in the CLOCK circuit after the PLAY mode Gate 48 and RECORD mode Gate 49 (instead of directly in the output of the CLOCK amplifier, Number 46), in order to take advantage of the TTL inverter Number 57 (7404) to drive the clock input of the F flip-flop.

OSCILLATOR:

OSCILLATOR is the output from the oscillator and pulse shaper. The oscillator is free running whenever the power to the card reader is turned on. The oscillator operates at 40kHz nominally.

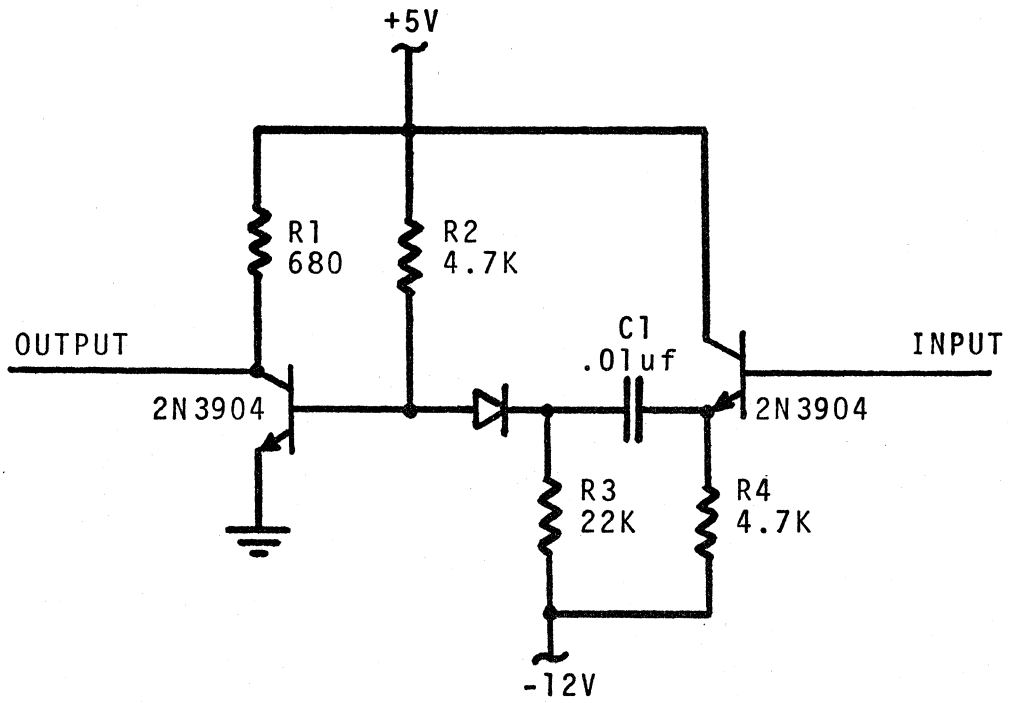
$\overline{\text{OSCILLATOR}}$ is formed by inverting OSCILLATOR in Gate 21 which isolates the oscillator from the timing chain.

2-13.0 MAGNETIC CARD READER (Cont.)

2-13.3 OPERATION (Cont.)

R1 and C4 form a by-pass network to prevent oscillator noise from entering the +5V supply. R2 and R3 are a voltage divider to bias the transistor for self-starting and self-adjusting. C3 is a by-pass for lower impedance on the base of the 2N3904 at the oscillator frequency. R4 is the current source for the oscillator circuit.

OSCILLATOR SHAPER:



OSCILLATOR SHAPER:

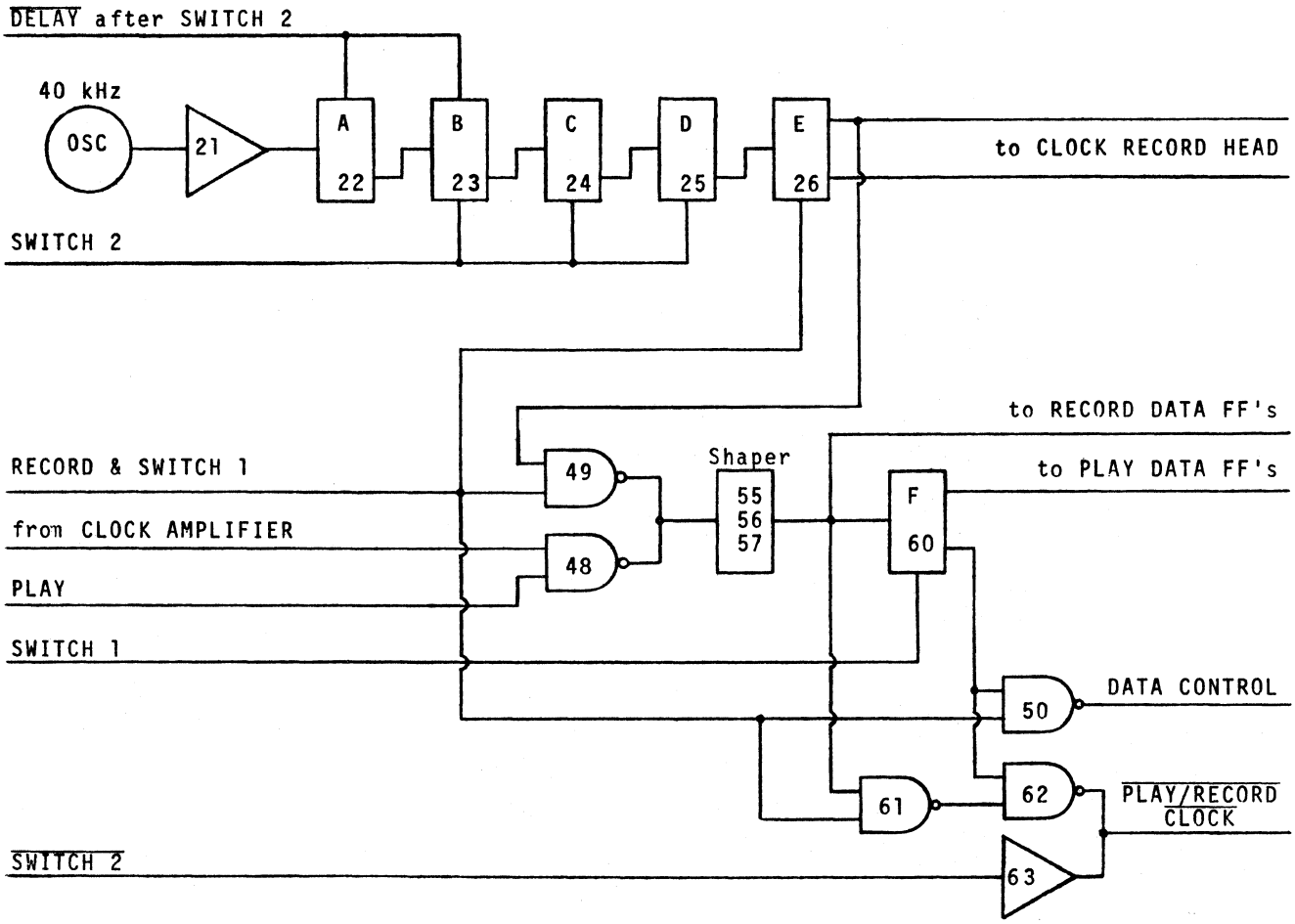
The shaper input has an emitter follower stage for impedance matching and a low load on the oscillator input.

C1 provides AC coupling to the output stage. R2 and R3 are chosen to set the slicing level for a 50% duty cycle. The diode is to prevent the base-emitter junction of the output transistor from loading the balancing action of R2 and R3. R1, the output stage load resistor, is small for fast turn-off.

2-13.0 MAGNETIC CARD READER (Cont.)

2-13.3 OPERATION (Cont.)

BLOCK DIAGRAM
CARD READER TIMING



2-13.0 MAGNETIC CARD READER (Cont.)

2-13.3 OPERATION (Cont.)

TIMING CHAIN:

The timing chain A flip-flop Number 22 is clocked at the 40 kHz rate of the oscillator through Inverter 21, which squares the oscillator output and provides noise suppression. A follows the oscillator except during the $\overline{\text{DELAY}}$ negative pulse which holds the over-riding preset input negative forcing Q positive.

The 20 kHz $\overline{A}$ output drives the B flip-flop Number 23.

The timing chain B flip-flop Number 23 is clocked at the 20 kHz rate of the output of the A flip-flop.

B follows A:

(A) whenever SWITCH 2 is activated by a magnetic card (changing the output of the SWITCH 2 flip-flop to positive) which removes the over-riding negative clear input forcing Q negative;

(B) except when the $\overline{\text{DELAY}}$ negative pulse holds the over-riding preset input negative forcing Q positive.

The 10 kHz $\overline{B}$ output drives the C flip-flop Number 24.

The timing chain C flip-flop Number 24 is clocked at the 10 kHz rate of the output of the B flip-flop.

C can follow B whenever SWITCH 2 is activated by a magnetic card (changing the output of the SWITCH 2 flip-flop to positive) which removes the over-riding negative clear input forcing Q negative.

The 5 kHz $\overline{C}$ output drives the D flip-flop Number 25.

The timing chain D flip-flop Number 25 is clocked at the 5 kHz rate of the output of the C flip-flop.

D can follow C whenever SWITCH 2 is activated by a magnetic card (changing the output of the SWITCH 2 flip-flop to positive) which removes the over-riding negative clear forcing Q negative.

The 2.5 kHz $\overline{D}$ output drives the E flip-flop Number 26.

The timing chain E flip-flop Number 26 is clocked at the 2.5 kHz rate of the output of the D flip-flop.

E can follow D only in the RECORD mode which removes the over-riding negative clear forcing Q negative.

2-13.0 MAGNETIC CARD READER (Cont.)

2-13.3 OPERATION (Cont.)

The 1.25 kHz E output drives:

(A) the input Gate 35 to the clock magnetic head and;

(B) the RECORD mode input to the CLOCK signal shaper at Gate 48.

The 1.25 kHz $\overline{E}$ output drives the input Gate 36 to the clock magnetic head.

The timing chain F flip-flop Number 59 is clocked at the 1.25 kHz rate of the output of the E flip-flop in the RECORD mode (through the CLOCK signal shaper). The F flip-flop is clocked by the recorded CLOCK at approximately 1.25 kHz in the PLAY mode (through the CLOCK signal shaper).

The F flip-flop is allowed to run only when SWITCH 1 is activated by a magnetic card (turning the SWITCH 1 flip-flop positive) which removes the over-riding negative clear input.

The 0.625 kHz F output:

(A) Clocks the PLAY DATA 1, 2 and 3 flip-flops through Inverter 64;

(B) clocks the PLAY DATA 4, 5 and 6 flip-flops through Inverter 65.

The 0.625 kHz $\overline{F}$ output:

(A) is anded with the output of the CLOCK signal shaper in Gate 61 to form (along with SWITCH 2 from SWITCH 2) $\overline{\text{PLAY RECORD CLOCK}}$.

(B) is anded with RECORD in Gate 49 to form the input data control.

The $\overline{\text{PLAY RECORD CLOCK}}$ output signal to the calculator provides timing to the calculator in both the RECORD and PLAY modes.

This signal is made by wire-oring SWITCH 2 from Gate 62 which follows SWITCH 2 with the clock signal from Gate 61 in order to provide timing to the calculator only when SWITCH 2 is activated by a magnetic card.

RECORD is made by inverting the $\overline{\text{RECORD}}$ input in Gate 27 and wire-oring it with the output of Gate 38. The RECORD signal goes positive when $\overline{\text{RECORD}}$ goes negative upon depression of the STORE ON CARD key on the 1155 calculator and a card has been inserted into the card reader far enough to operate SWITCH 1.

2-13.0 MAGNETIC CARD READER (Cont.)

2-13.3 OPERATION (Cont.)

It stays positive until the card has passed by SWITCH 1 completely, which turns RECORD negative and through the 1155 calculator turns $\overline{\text{RECORD}}$ positive, which holds RECORD negative.

RECORD, going positive:

(A) allows flip-flop E, Number 26, of the timing chain to operate (when flip-flop D is driving it) by removing the over-riding negative clear to flip-flop E;

(B) permits the eight input Gates 29 to 36 to the four-track recording head to invert the eight outputs from flip-flops DATA 4, DATA 5, DATA 6 and E;

(C) permits E from the timing chain to be inverted by Gate 48 to make the $\overline{\text{RECORD CLOCK}}$ signal (portion of $\overline{\text{PLAY RECORD CLOCK}}$);

(D) permits $\overline{\text{CLOCK DATA}}$ from the CLOCK DATA flip-flop Number 59 to be inverted by Gate 49 to clock the six RECORD DATA inputs.

PLAY is made by inverting the $\overline{\text{PLAY}}$ input in Gate 28. The PLAY signal goes positive when $\overline{\text{PLAY}}$ goes negative upon depression of the READ FROM CARD key on the 1155 calculator.

PLAY going positive:

(A) allows the data being read to be transferred through the six PLAY DATA flip-flops, Numbers 69 to 74, by removing the over-riding negative preset to these flip-flops;

(B) permits the CLOCK signal to be inverted by Gate 47 to make the $\overline{\text{PLAY CLOCK}}$ signal (portion of $\overline{\text{PLAY RECORD CLOCK}}$);

(C) permits the MOTOR CONTROL signal to turn on the motor when a magnetic card is inserted.

The SWITCH 1 flip-flop, made from cross-coupled Gates 50 and 51, is activated by SWITCH 1.

SWITCH 1 normally negative, going positive when activated by SWITCH 1:

(A) is inverted by Gate 65 to make the $\overline{\text{READER BUSY}}$ signal;

2-13.0 MAGNETIC CARD READER (Cont.)

2-13.3 OPERATION (Cont.)

(B) is anded with PLAY in Gate 64 to turn the motor on during magnetic card playback.

(C) is anded with RECORD in Gate 63 to turn the motor on during recording.

(D) allows the F timing chain flip-flop, Number 59, to operate by removing the over-riding negative clear.

$\overline{\text{SWITCH 1}}$ is inverted by Gate 38 to form (along with $\overline{\text{RECORD}}$) RECORD.

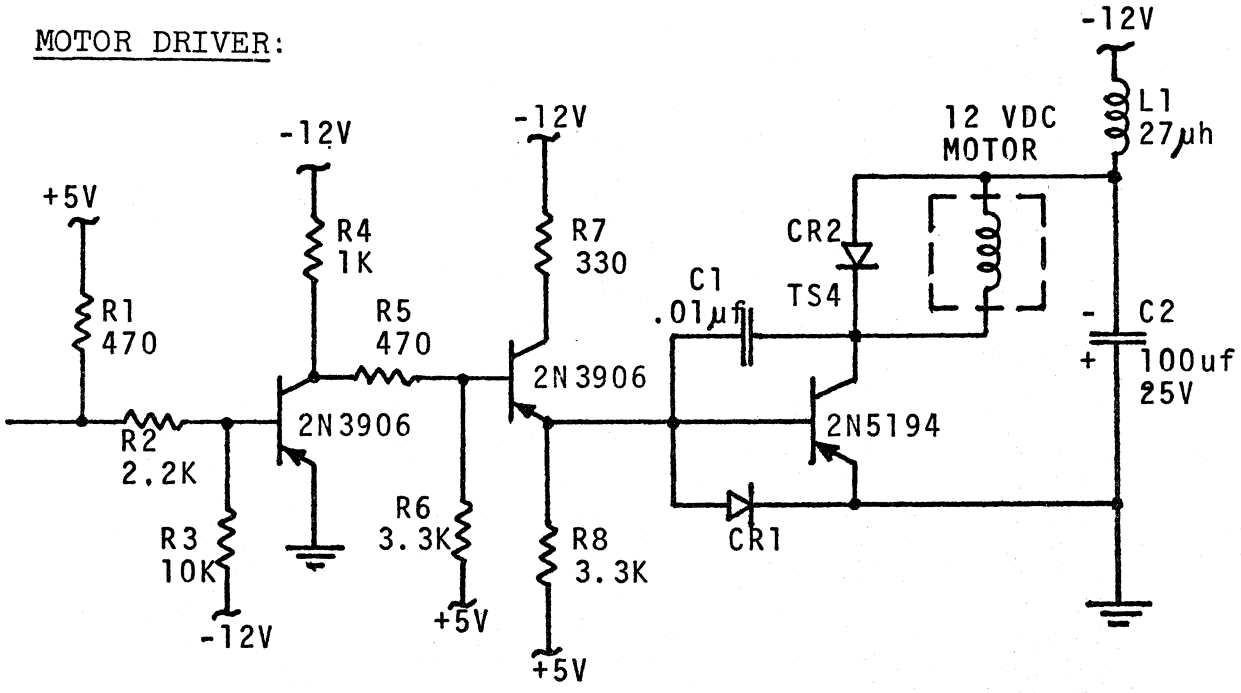
MOTOR, the output signal of Gate 66 is normally negative and goes positive to turn on the motor through a transistor driver circuit.

MOTOR is made by a wire-or of:

(A) SWITCH 1 and PLAY, Gate 64, or

(B) SWITCH 1 and RECORD, Gate 63.

MOTOR DRIVER:

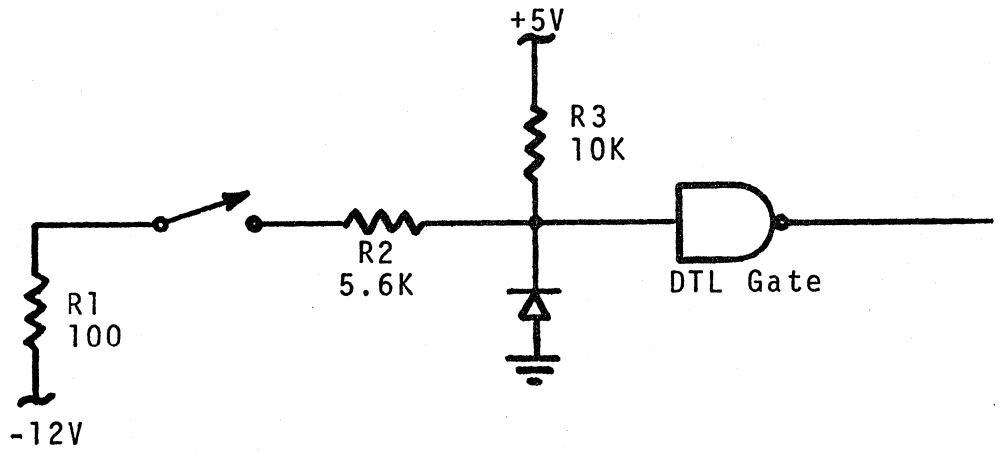


The motor driver circuit shifts the level and amplifies the input signal to drive the 12 VDC motor.

2-13.0 MAGNETIC CARD READER (Cont.)

2-13.3 OPERATION (Cont.)

R1 is a pull-up resistor. R2 is the current limiting and drive resistor for the base of the first 2N3906. R3 is the current source. R4 is the pull-up resistor. R5 limits current and R6 is the source. R7 biases the second 2N3906 to insure it can reach off condition. R8 is the load and 2N5194 output switch turn-on resistor. The .01 μf Miller capacitor and the TS4 diode are for noise suppression. CR1 prevents back biasing the 2N5194. L1 and C2 decouple motor noise from the -12V supply.

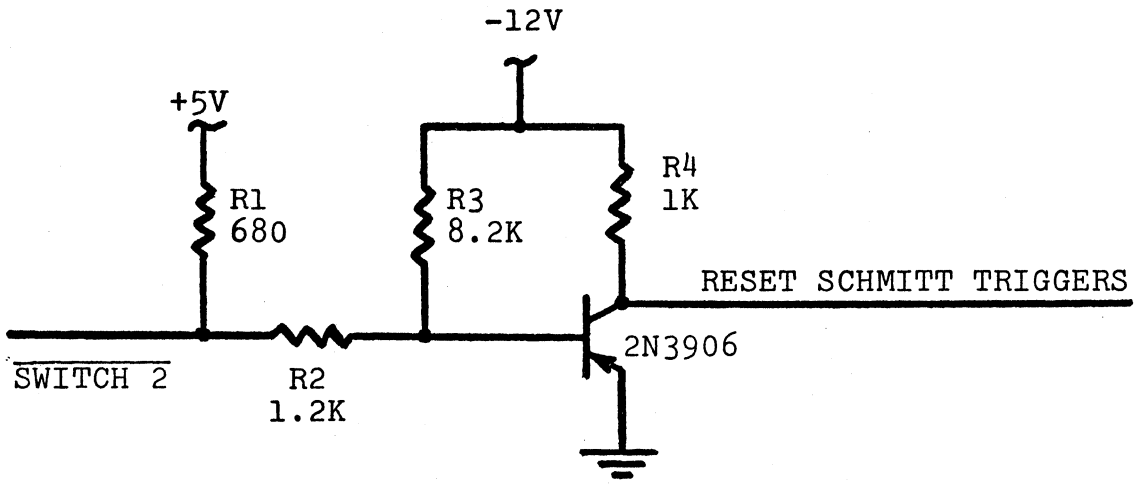


The switches are wired to a -12V clamp through a 100 ohm line capacity noise suppression resistor. The 5.6K ohm resistor provides current source control. The 10K ohm resistor is a pull-up resistor to back-bias the internal input diodes in the DTL gate. The diode prevents excessive negative voltage on the input of the DTL gate.

2-13.0 MAGNETIC CARD READER (Cont.)

2-13.3 OPERATION (Cont.)

SCHMITT RESET AMP:



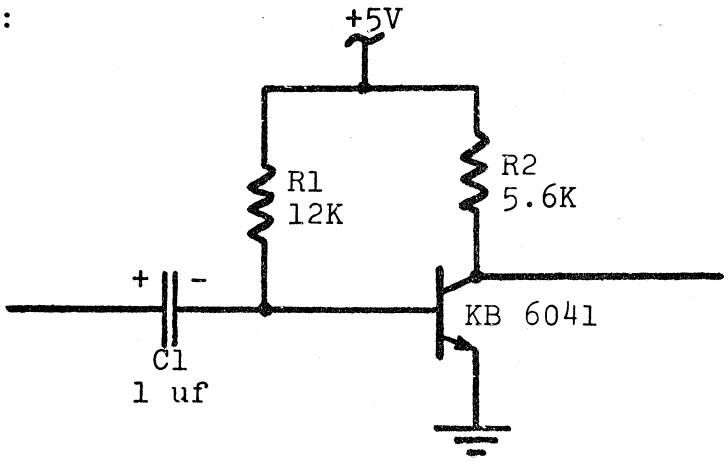
R1 is the load resistor for the DTL driver and current source to overcome the on bias. R2 and R3 provide level shift and isolation. R4 is the transistor load resistor.

When SWITCH 2 is operated by the magnetic card, $\overline{\text{SWITCH 2}}$ goes negative and RESET SCHMITT TRIGGER goes positive. When the card has passed by SWITCH 2, RESET SCHMITT TRIGGER returns to negative.

2-13.0 MAGNETIC CARD READER (Cont.)

2-13.3 OPERATION (Cont.)

ONE-SHOT:



The input is normally positive, holding the transistor on and the output negative. A negative input turns the transistor off and the output goes positive until the RC network recharges, at which time the transistor turns on and the output goes negative.

The one-shot time constant is approximately 0.7 RC: (.7) x (12K) x (1×10^{-6}) = 8.4 milliseconds.

Slicing is close to the half-way point between -5V and +5V near ground.

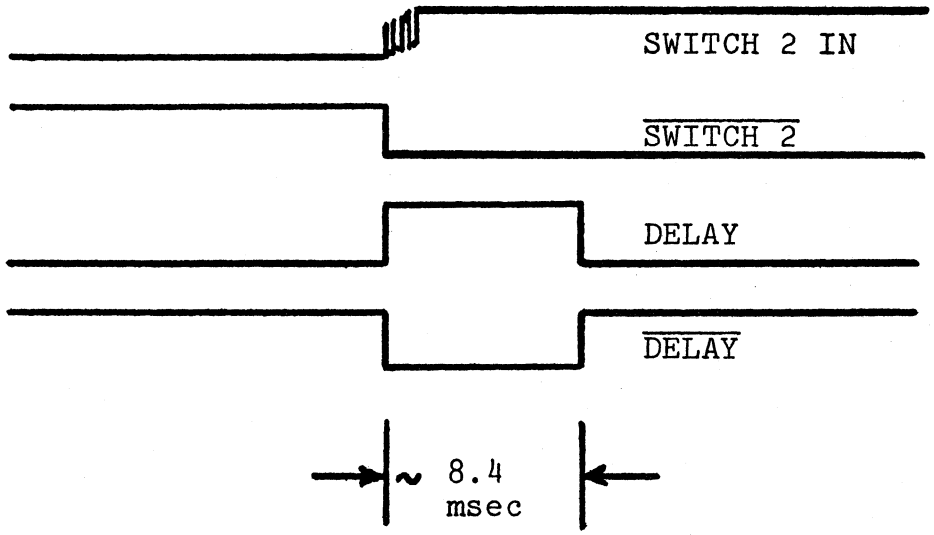
A 10 millisecond delay before recording is incorporated in order to ensure that the first recorded bits on the magnetic card are well within the confines of the card so that they will not be missed during playback.

When SWITCH 2 is activated, $\overline{\text{SWITCH 2}}$ goes negative. This forces the output of the delay transistor one-shot, normally negative, to go positive for an RC time of (12 K ohm times 1 μfd) approximately 10 milliseconds. This DELAY pulse is inverted in Gate 37 to $\overline{\text{DELAY}}$ which stops the timing chain by an over-riding clear on the A and B flip-flops, Numbers 22 and 23.

2-13.0 MAGNETIC CARD READER (Cont.)

2-13.3 OPERATION (Cont.)

DELAY TIMING:



The SWITCH 2 flip-flop, made from cross-coupled Gates 52 and 53, is activated by SWITCH 2.

SWITCH 2,normally negative, going positive when activated by SWITCH 2 allows flip-flops B, C and D, Numbers 22, 23 and 24, of the timing chain, to operate (when flip-flop A is driving them) by removing the over-riding negative clear.

$\overline{\text{SWITCH 2}}$, normally positive, going negative when activated by SWITCH 2:

(A) presets the four playback amplifiers on through a transistor driver circuit;

(B) activates the 10 millisecond delay circuit on the initial negative-going edge;

2-13.0 MAGNETIC CARD READER (Cont.)

2-13.3 OPERATION (Cont.)

(C) allows, after inversion in Gate 20, the six RECORD DATA flip-flops, Numbers 13 to 18 to control data inputs by removing the over-riding negative clears;

(D) permits the $\overline{\text{PLAY RECORD CLK}}$ output after inversion in Gate 62.

SWITCH 1 is activated by the leading edge of the magnetic card when it is inserted into the card reader and deactivated by the trailing edge of the card after it has passed through the card reader.

SWITCH 1 IN and $\overline{\text{SWITCH 1 IN}}$ control, after a switch bounce noise suppression circuit, the SWITCH 1 flip-flop, made of cross-coupled Gates 51 and 52.

SWITCH 2 is activated by the leading edge of the magnetic card when it is running through the card reader and deactivated by the trailing edge of the card after it has passed through the card reader.

SWITCH 2 IN and $\overline{\text{SWITCH 2 IN}}$ control, after a switch bounce noise suppression circuit, the SWITCH 2 flip-flop, made of cross-coupled Gates 53 and 54.

$\overline{\text{PLAY}}$, an input signal to the card reader operated by the LOAD FROM CARD key on the 1155 calculator, is normally positive and goes negative when a recorded card is to be read. This signal must stay negative until playback is completed.

$\overline{\text{PLAY}}$ is set negative by the $\overline{\text{READER BUSY}}$ output going negative and reset positive by $\overline{\text{READER BUSY}}$ going positive.

Note that $\overline{\text{PLAY}}$ can also be reset positive by depression of the RESET key on the 1155 calculator. This action will terminate playback and stop the motor. If the motor is stopped with the card within the reader, the card may be manually extracted from the card reader (be careful not to scratch it!) or by redepression of the LOAD FROM CARD key, the motor will restart and eject the card. Transferred data under these condition is not to be trusted.

$\overline{\text{RECORD}}$, an input signal to the card reader operated by the STORE ON CARD key on the 1155 calculator, is normally positive and goes negative when a recording is to be made. This signal must stay negative until recording is completed.

$\overline{\text{RECORD}}$ is set negative by the $\overline{\text{READER BUSY}}$ output going negative and reset positive by $\overline{\text{READER BUSY}}$ going positive.

2-13.0 MAGNETIC CARD READER (Cont.)

2-13.3 OPERATION (Cont.)

Note that $\overline{\text{RECORD}}$ can also be reset positive by depression of the RESET key on the 1155 calculator. This action will terminate recording and stop the motor. If the motor is stopped with the card within the card reader, the card may be manually extracted from the card reader (be careful not to scratch it!) or by redepression of the STORE ON CARD key, the motor will restart and eject the card. Transferred data under these conditions is not to be trusted.

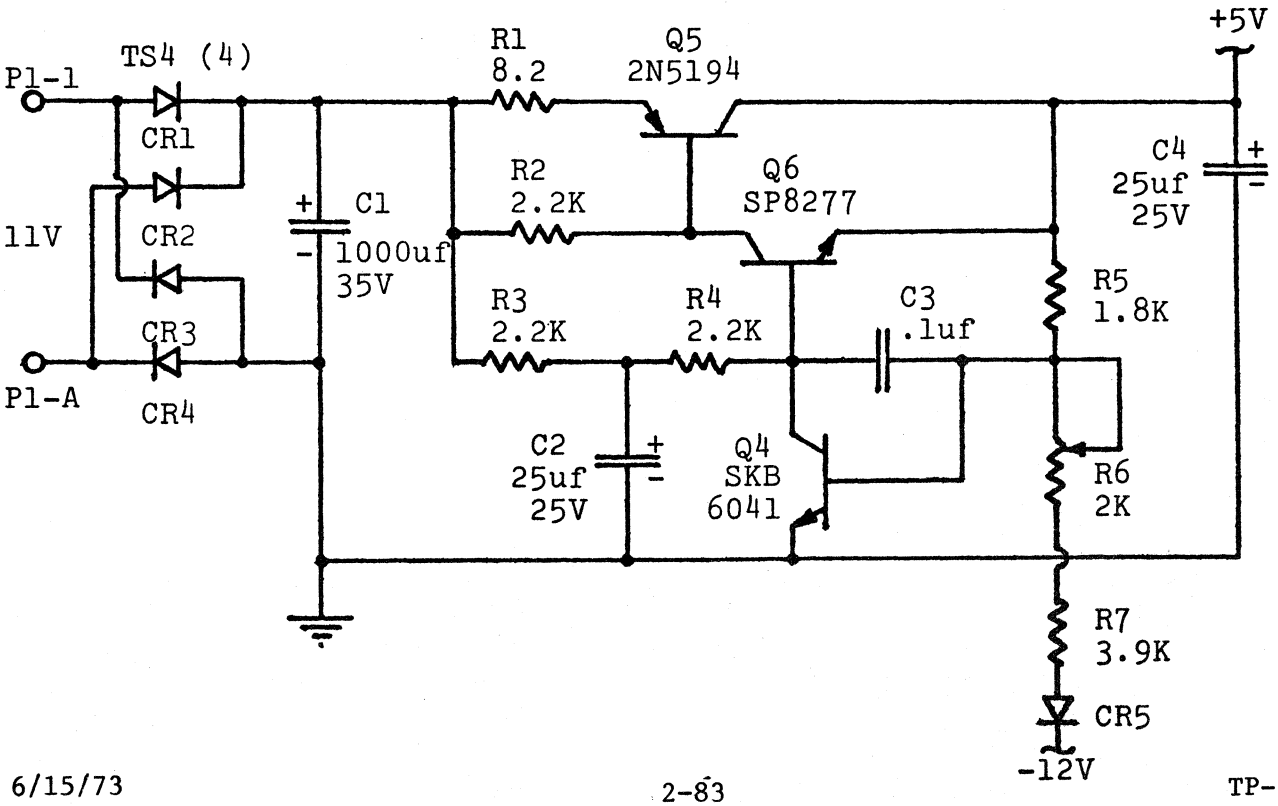
POWER SUPPLIES:

Two separate windings from the secondary of the Model 1155 power transformer provide power to the card reader power supply. The windings are 11 VAC to power the +5 VDC supply and 18VAC to power the -12 VDC supply.

The +5 VDC and -12 VDC supplies are similiar series regulated supplies with a common ground.

POWER SUPPLY +5V:

A full wave bridge and capacitive input filter feed a series power regulator (2N5194) with a series 8.2 ohm current limiting resistor. Q6 (SP8277) is the



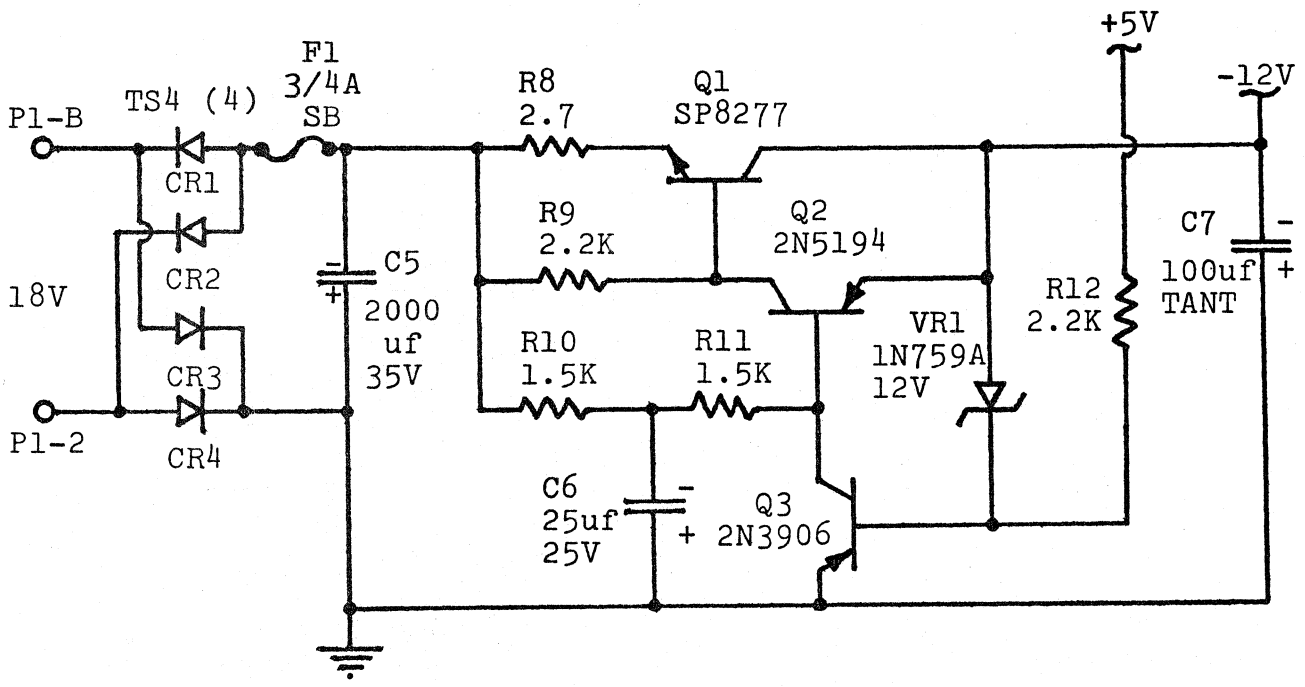
2-13.0 MAGNETIC CARD READER (Cont.)

2-13.3 OPERATION (Cont.)

driver for the power regulating transistor and R2 is the turn-off resistor. R3 and R4 are the load for Q4 and current source for Q6. C2 provides decoupling for prevention of 120 Hz modulation of the amplifier. The -12V is the reference voltage from which a reference current flows through R6 and R7. R5 is a negative feedback resistor from the +5V through which a compare current flows. Q4 is the sensing transistor that compares the junction of the feedback current and the reference current. The 2K ohm potentiometer R6 adjusts the reference current and R7 limits the adjustment. The diode to -12V provides temperature compensation. C3 is a Miller capacitor to slow down the response of Q3 to prevent oscillation.

POWER SUPPLY -12V:

A full wave bridge and capacitive input filter feed a series power regulator (SP8277) with a series 2.7 ohm current limiting resistor. Q2 (2N5194) is the driver for the power regulating transistor and R9 is the turn-off resistor. R10 and R11 are the load for Q3 and current source for Q2. C6 provides decoupling for prevention of 120 Hz modulation of the amplifier. Q3 is the sensing transistor and a 1N759A, 12V zener diode is the voltage reference element. R12 provides threshold current for the zener diode. C7 is a noise by-pass capacitor and energy storage in order to maintain a low impedance beyond the frequency response of the regulator. F1 provides short circuit or stalled motor current protection.



2-13.0 MAGNETIC CARD READER (Cont.)

2-13.3 OPERATION (Cont.)

MODEL 1155 KEYBOARD CODES

KEYTOP	KEYBOARD CODE	Z CODE
LIST	$\overline{b}$ $(\overline{x})$ $\overline{PROG\ BUSS}$	1 - - - - - -
WRITE	$\overline{c}$ $(\overline{x})$ $\overline{PROG\ BUSS}$	- 2 - - - - -
INSERT	$\overline{d}$ $(\overline{x})$ $\overline{PROG\ BUSS}$	1 2 - - - - -
DELETE	$\overline{e}$ $(\overline{x})$ $\overline{PROG\ BUSS}$	- - 3 - - - -
LOAD FROM CARD	$\overline{f}$ $(\overline{x})$ $\overline{PROG\ BUSS}$	1 - 3 - - - -
STORE IN CARD	$\overline{g}$ $(\overline{x})$ $\overline{PROG\ BUSS}$	- 2 3 - - - -
CLEAR PROG	$\overline{h}$ $(\overline{x})$ $\overline{PROG\ BUSS}$	1 2 3 - - - -
0	$\overline{a}$ $\overline{j}$	- - - 4 - - -
1	$\overline{b}$ $\overline{j}$	1 - - 4 - - -
2	$\overline{c}$ $\overline{j}$	- 2 - 4 - - -
3	$\overline{d}$ $\overline{j}$	1 2 - 4 - - -
4	$\overline{e}$ $\overline{j}$	- - 3 4 - - -
5	$\overline{f}$ $\overline{j}$	1 - 3 4 - - -
6	$\overline{g}$ $\overline{j}$	- 2 3 4 - - -
7	$\overline{h}$ $\overline{j}$	1 2 3 4 - - -
8	$\overline{a}$ $\overline{k}$	- - - - 5 - -
9	$\overline{b}$ $\overline{k}$	1 - - - 5 - -
.	$\overline{c}$ $\overline{k}$	- 2 - - 5 - -
SET DEC ( )	$\overline{d}$ $\overline{k}$	1 2 - - 5 - -
STOP	$\overline{e}$ $(\overline{k})$ $\overline{STOP}$	- - 3 -(5)-
ENTER EXP	$\overline{f}$ $\overline{k}$	1 - 3 - 5 - -
ARC	$\overline{g}$ $\overline{k}$	- 2 3 - 5 - -
RECALL ( ) ( )	$\overline{h}$ $\overline{k}$	1 2 3 - 5 - -
STORE ( ) ( )	$\overline{a}$ $\overline{\ell}$	- - - 4 5 - -
ACCUM STORE ( ) ( )	$\overline{b}$ $\overline{\ell}$	1 - - 4 5 - -
ENTER	$\overline{c}$ $\overline{\ell}$	- 2 - 4 5 - -
x^2	$\overline{d}$ $\overline{\ell}$	1 2 - 4 5 - -
π	$\overline{e}$ $\overline{\ell}$	- - 3 4 5 - -
CHANGE SIGN	$\overline{f}$ $\overline{\ell}$	1 - 3 4 5 - -

2-13.0 MAGNETIC CARD READER (Cont.)

2-13.3 OPERATION (Cont.)

KEYTOP	KEYBOARD CODE		Z CODE
INTGR	$\overline{g}$	$\overline{\ell}$	- 2 3 4 5 -
TO POLAR	$\overline{h}$	$\overline{\ell}$	1 2 3 4 5 -
−	$\overline{a}$	$\overline{m}$	- - - - - 6
$\sqrt{\lvert x \rvert}$	$\overline{b}$	$\overline{m}$	1 - - - - 6
1/x	$\overline{c}$	$\overline{m}$	- 2 - - - 6
$\lvert A \rvert^x$	$\overline{d}$	$\overline{m}$	1 2 - - - 6
SIN	$\overline{e}$	$\overline{m}$	- - 3 - - 6
COS	$\overline{f}$	$\overline{m}$	1 - 3 - - 6
TAN	$\overline{g}$	$\overline{m}$	- 2 3 - - 6
$\log \lvert x \rvert$	$\overline{h}$	$\overline{m}$	1 2 3 - - 6
$\lvert x \rvert !$	$\overline{a}$	$\overline{n}$	- - - 4 - 6
+	$\overline{b}$	$\overline{n}$	1 - - 4 - 6
$\ln \lvert x \rvert$	$\overline{c}$	$\overline{n}$	- 2 - 4 - 6
÷	$\overline{d}$	$\overline{n}$	1 2 - 4 - 6
X	$\overline{e}$	$\overline{n}$	- - 3 4 - 6
e^x	$\overline{f}$	$\overline{n}$	1 - 3 4 - 6
TO RECT	$\overline{g}$	$\overline{n}$	- 2 3 4 - 6
DEG	$\overline{h}$	$\overline{n}$	1 2 3 4 - 6
RAD	$\overline{a}$	$\overline{o}$	- - - - 5 6
CLEAR ENTRY (PLOT)	$\overline{b}$	$\overline{o}$	1 - - - 5 6
PRINT	$\overline{c}$	$\overline{o}$	- 2 - - 5 6
PRINT SCI	$\overline{d}$	$\overline{o}$	1 2 - - 5 6
LINE SPACE	$\overline{e}$	$\overline{o}$	- - 3 - 5 6
GO TO ( ) ( )	$\overline{f}$	$\overline{o}$	1 - 3 - 5 6
IF NEG ( ) ( )	$\overline{g}$	$\overline{o}$	- 2 3 - 5 6
CLEAR ALL REGS	$\overline{h}$	$\overline{o}$	1 2 3 - 5 6
START	$\overline{a}$	$\overline{p}$	- - - 4 5 6
ONE STEP	$\overline{b}$	$\overline{p}$	1 - - 4 5 6
IND ( ) ( )	$\overline{c}$	$\overline{p}$	- 2 - 4 5 6
RESET	($\overline{f}$)	($\overline{p}$)	(1 - 3 4 5 6)
PROG CODE ( ) ( )	$\overline{g}$	$\overline{p}$	- 2 3 4 5 6

8 7 6 5 4 3 2 1

BIT 3
BIT 2
BIT 1

PI-14 RECORD DATA 1
PI-12 RECORD DATA 2
PI-J RECORD DATA 3
PI-B RECORD DATA 4
PI-7 RECORD DATA 5
PI-H RECORD DATA 6

RD1 74L74
RD2 74L74
RD3 74L74
RD4 74L74
RD5 74L74
RD6 74L74

R82 1.2K A
R81 1.2K B

PLAY DATA 1
PLAY DATA 2
PLAY DATA 3
PLAY DATA 4
PLAY DATA 5
PLAY DATA 6

PLAY

PI-1
PI-A
PI-2
PI-B
11V
18V
TS4 (4)
3/4 A SB F1

CR29 CR28 CR31 CR30 CR26 CR25 CR24 CR23

C23 1000uF 35V
C22 2000uF 35V

Q5 8.2Ω 2W 5% 2N5194 * (2.5W)
R70 2.2K
R71 2.2K
R72 2.2K
SP8277 Q6
C19 .1uf
C15 25uF 25V
Q4 KB6041
C17 25uf 25V
C14 .047uf
1.8K R73
R52 2K ±20% 1/4W
R65 3.9K
CR21 -12V (100mA) (LESS MOTOR)

Q1 SP8277 * (4W)
R77 2.7Ω 2W 5%
R68 2.2K
R69 1.5K
R67 1.5K
2N5194 Q2
VR1 INTERSIL 400mW 12V
R66 2.2K
C16 25uF 25V
2N 3906 Q3
C18. 100uf 20V TANT.

+5V (225mA)

(1.4 A)

L2 27μH

100uf 25V C21

MOTOR M1 M2

Q7 2N5194
Q14 2N3906
Q8 2N 3906
CR22 662
CR27 TS4
C24 .01uf
R84 10K
R85 330Ω
R86 2.2K
R87 470Ω
R88 3.3K
R89 470Ω
R83 3.3K

PD1 8 74L74
PD2 3 74L74
PD3 16 74L74
PD4 16 74L74
PD5 17 74L74
PD6 17 74L74

PI-N PLAY DATA 1
PI-P PLAY DATA 2
PI-M PLAY DATA 3
PI-11 PLAY DATA 4
PI-10 PLAY DATA 5
PI-L PLAY DATA 6

PLAY RECORD CLK PI-K
READER BUSY PI-9

P2-7 P2-9 P2-10 P2-12 P2-13 P2-15 P2-16 P2-18

R12 680Ω C5 2μf
R13 680Ω C6 2μf
R14 680Ω C8 2μf
R15 680Ω C7 2μf
R16 680Ω C1 2μf
R17 680Ω C2 2μf
R18 680Ω C3 2μf
R19 680Ω C4 2μf

R26 100K R34 2.7K 10K R33 R32 1K CR13 CR12
R28 6.8K R27 6.8K
R35 330Ω R30 100K R36 1K CR14
R31 6.8K R29 6.8K R37 2.7K CR15 R39 330Ω 10K R38
R20 100K R45 2.7K 10K R46 R44 1K CR16 CR17
R22 6.8K R21 6.8K
R23 100K R48 1K CR18 CLK
R25 6.8K R24 6.8K R51 2.7K CR19 R49 330Ω R50 10K

R59 3.3K R58 3.3K R60 3.3K R57 3.3K R64 3.3K R63 3.3K R61 3.3K R62 3.3K

E
E + CLOCK 2
DATA CONTROL
E + CLOCK 1

DELAY
PLAY
SWITCH 2
SWITCH
SWITCH 2

R1 680Ω R56 4.7K
KB 6041 Q11 CR20 C10 .01uF R55 22K R54 4.7K
KB 6041 Q12
KB 6041 Q13
L1 1mh
C13 .056uF ±5% C11 .022uF ±5%
R75 8.2K R76 4.7K R53 3.3K C12 .1uF
C9 .1uF
R74 15Ω
R80 12K C20 1uF R79 5.6K KB 6041 Q10

MUCH GND
PI-5, 6, E, F

PI-13 RECORD 3
PI-15 PLAY 11
RECORD
PLAY

P2-1 OFF CARD SW1 SW2
P2-2 P2-3 P2-4 P2-6 100Ω -12V
R3 5.6K R2 10K CR1
R4 5.6K R5 10K CR2
R6 5.6K R7 10K CR32
R9 5.6K R10 10K CR3

R43 680Ω R42 1.2K R40 82K R41 1K 2N 3906 Q9
SWITCH 1

REF. TIMING DIAGRAM

1) UNLESS SPECIFIED— ALL RESISTORS 1/4 WATT, ± 5%. ALL DIODES IN662.
2) * ON HEAT SINK.

TP-285-8
CIRCUIT SCHEMATIC
MAGNETIC CARD READER

43-4 REV 6/69

SECTION 3

MAINTENANCE

SECTION CONTENTS

3-1.0 GENERAL

This section contains information concerning: Lubrication, adjustments, safety precautions, and other pertinent information on proper maintenance of the 1155 Electronic Calculator. A chart showing various Troubleshooting procedures is also included.

3-1.1 SAFETY PRECAUTIONS

When servicing the 1155 Electronic Calculator, observe the standard safety precautions as follows:

(1) Turn off the power when removing or installing PC boards.

(2) When using test probes or other test equipment use care to prevent accidental short circuiting of adjacent circuit traces or components.

(3) Use the proper tool(s) for installing and extracting IC chips. (See Tool List.)

3-1.2 LUBRICATION

Shown in the Chart below are the types of lubricants and points that require lubrication. Preventive maintenance for general cleaning and lubrication of the printer must be performed at least once per year. More frequently for machines subject to heavy usage.

LUBRICANT	WHERE USED
SAE 40 Motor Oil (Shell X-100 or equivalent) (Purchase Locally)	1. All bearing (except ball bearings) 2. Levers and links 3. Rotating shafts 4. Carriage Guide Shafts 5. Eccentric Cam 6. Drive pin (two drops) *7. Dashpot Felt Washer *8. Print Shaft Felt Washer * CAUTION: Saturate and squeeze to eliminate excessive oil so that oil doesn't splash off due to rotation of the Print Wheel.
Shell non-stain Grease (T-18407)	1. Screw shaft threads 2. Print wheel yoke groove 3. Gear train for paper feed roll 4. Clutch spring

3-1.2 LUBRICATION (Cont.)

LUBRICANT	WHERE USED
Poly Oil (Type 3030-280) (T-18587)	1. Lubrication cups at each end of the coil armature pivots (six places) 2. The right end of the screw shaft. 3. The clutch bearing hub.

3-1.3 INSPECTION PROCEDURE

The following is a list of essential actions for assurance of optimum printer performance.

CHECK:

1. All printer adjustments as listed.
2. Drive pin for wear and smooth action.
3. Eccentric action: Clutch, Line Feed, Inking, Pin disengage.
4. Character print, clear impression, even printing, ink transfer.
5. Ink cartridge for possible replacement.
6. Belt tension, wear.

3-2.0 PRINTER ADJUSTMENTS

Adjustments for best printer operation are as follows. Also, a list of necessary tools and their tool numbers is included for reference.

TOOL LIST:

1/16 and #050 Allen Wrenches (T-18430 and 18339)
6" Screwdrivers, Common and Narrow Blade
Long Nose, or Needle Nose Pliers
3/8 x 1/2 Open End Wrench (T-18115)
1/4" Open End Wrench
5/16 Open End Wrench
Tru-Arc Pliers (T-18623)

3-2.1 DRIVE BELT

Adjust the motor position for approximately 1/8" deflection of the drive belt as measured at a point midway between the motor pulley and the print shaft pulley.

3-2.0 PRINTER ADJUSTMENTS (Cont.)

3-2.2 PRINT WHEEL TO TIMING WHEEL RELATIONSHIP

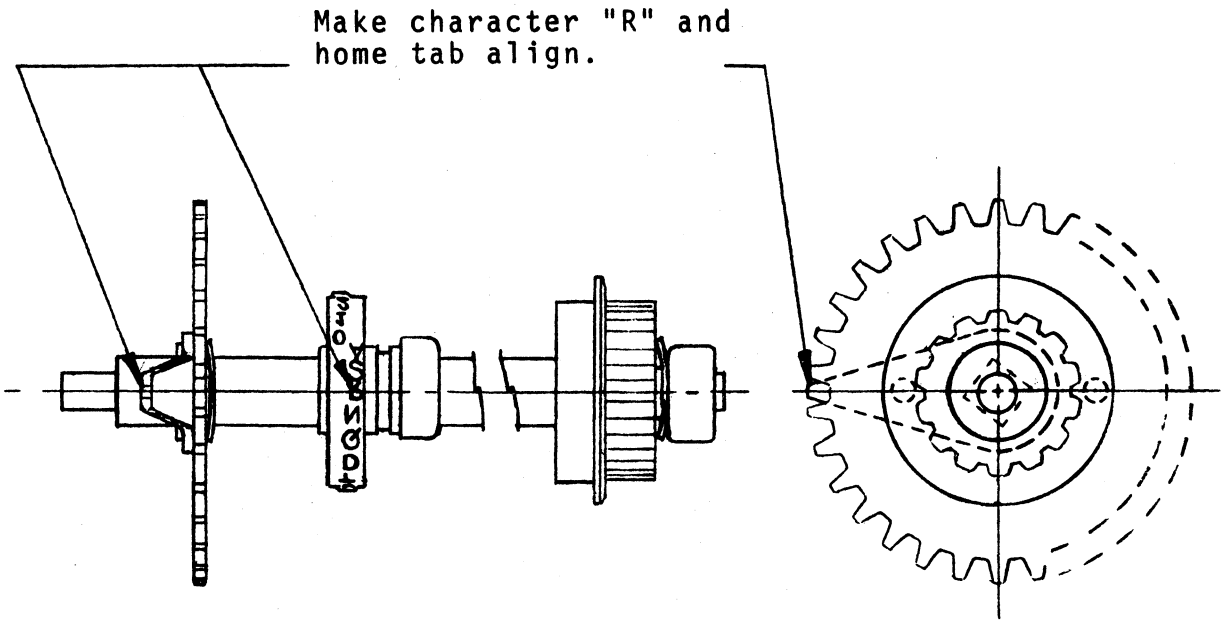


FIGURE 3-1

Install the print wheel so that the character "R" of the print wheel is in line with the home tab on the timing wheel.

3-2.0 PRINTER ADJUSTMENTS (Cont.)

3-2.3 CARRIAGE TIE BAIL

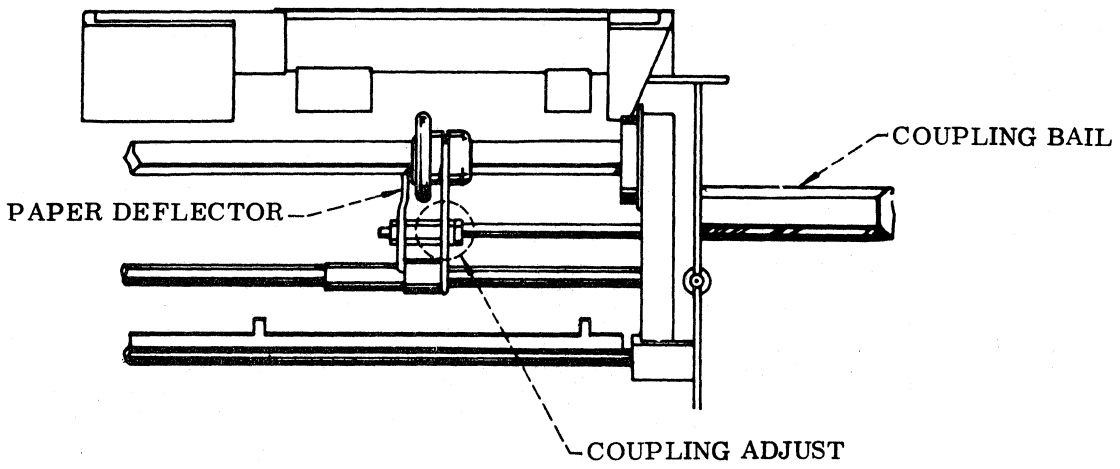


FIGURE 3-2

The print hammer carriage and the print wheel carriage are coupled together by a U-shaped tie-rod or coupling bail. For best hammer to print wheel action, the hammer must strike the print wheel directly on the character to be printed. Centering is adjusted by use of the coupling nuts on the print wheel carriage.

NOTE: For best centering of hammer to character, use the characters: 0, 9, E, or -.

To assure a free, smooth running carriage, the coupling bail shaft should be aligned so that its threaded end is centered in the hole where it is attached to the coupling yoke. Failure to align the bail will cause a bind in the carriage due to the twist applied to the coupling yoke when the hexagon adjusting nut is turned at time of adjusting the centering of the hammer.

After alignment of the coupling bail shaft, proceed to adjust the centering of the hammer as follows:

1. Remove the printer front plate.
2. Loosen the coupling nuts at the print carriage.
3. Manually push the hammer against the character on the print wheel and align them squarely.
4. Adjust the coupling nuts until the print wheel is centered on hammer.
5. Tighten the locknuts.
6. Check to see that the paper deflector holds the paper inward so that it does not touch the print wheel. Adjust, and tighten nut.
7. Replace the print front plate.
8. Check to see that the hammer face is parallel with the character face. Slight twisting of the hammer is permissible.

3-2.0 PRINTER ADJUSTMENTS (Cont.)

3-2.4 CARRIAGE HOME

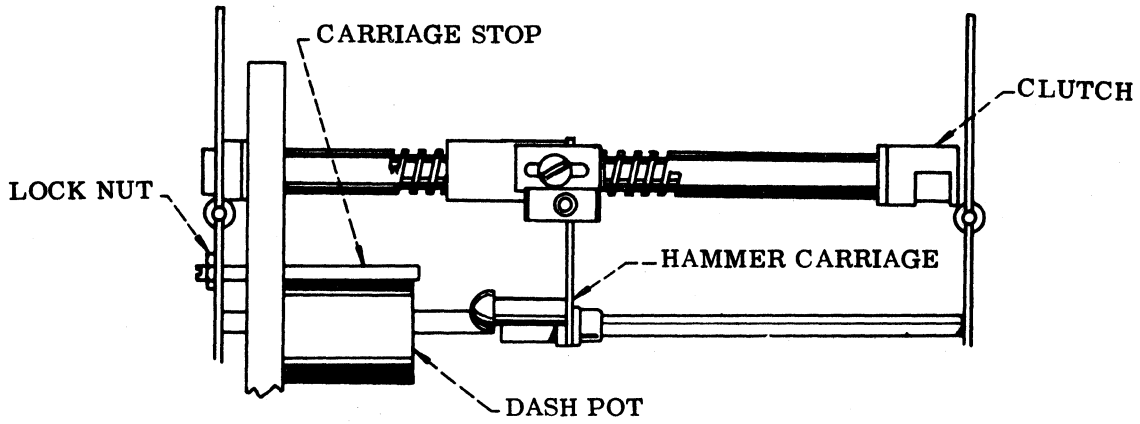


FIGURE 3-3

When the Pin is "fired" to engage the Lead Screw, it is very important that the carriage be at its precise "home" position, and that the thread be properly aligned in its lateral direction; otherwise, rapid wear of the Pin will result. Adjust as follows:

1. Carriage End Stop

   a. Check end play in screw shaft to see that it is correct (.005").
   b. Engage the pin into the screw shaft and gently rotate the screw shaft backwards until the pin stops against the end of the helix thread.
   c. Turn the carriage stop screw inward until it just touches the carriage bracket.
   d. Now back off the stop screw 1/8 to 1/4 turn and tighten the lock nut.

2. Carriage Home Reed Switch

   a. Connect an Ohmmeter to the carriage reed switch.
   b. Disengage the pin from the lead screw.
   c. Adjust the magnet on the bottom of the carriage assembly (through the access hole in the base) until the reed switch closes within the last .029" of carriage travel.

3-2.0 PRINTER ADJUSTMENTS (Cont.)

3-2.5 DRIVE PIN

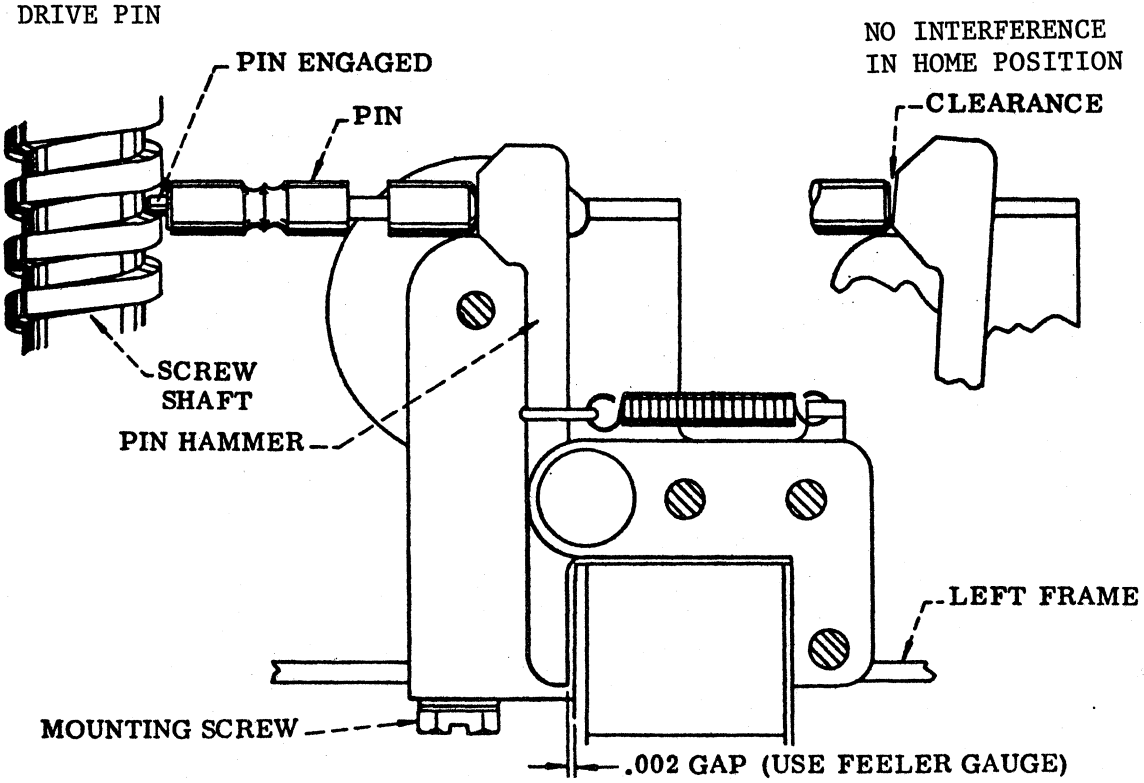


FIGURE 3-4

The drive pin armature must move forward enough to fully engage the pin into the screw shaft thread, and be fully clear of the drive pin when it is disengaged. NOTE: A drive pin not being fully engaged will cause accelerated wear on the pin and also the helix shaft, as well as early disengagement (pop-out) of the drive pin. The adjustment is as follows:

1. Engage the drive pin into the screw thread.
2. Loosen the bracket mounting screws.
3. With a .002" feeler gauge between the coil and the hammer, depress the hammer against the pin until the pin is fully engaged into the screw thread.
4. Holding the hammer depressed against the pin, move the bracket assembly to obtain the .002" clearance between the coil and the hammer. (Full accessability of the drive pin and armature can be achieved by removing the paper cradle.)
5. Tighten the bracket mounting screws.
6. With the pin and hammer fully restored to home position, check for minimum clearance between the disengaged drive pin and pin hammer on armature. NOTE: Interference between pin hammer and drive pin could prevent full pin disengagement which would result in unwanted carriage travel after a line feed operation.
7. With the armature fully restored, check to see that the back of the pin hammer and hammer stop are parallel.

3-2.0 PRINTER ADJUSTMENTS (Cont.)

3-2.6 MAGNETIC PICKUP GAP (Output Voltage)

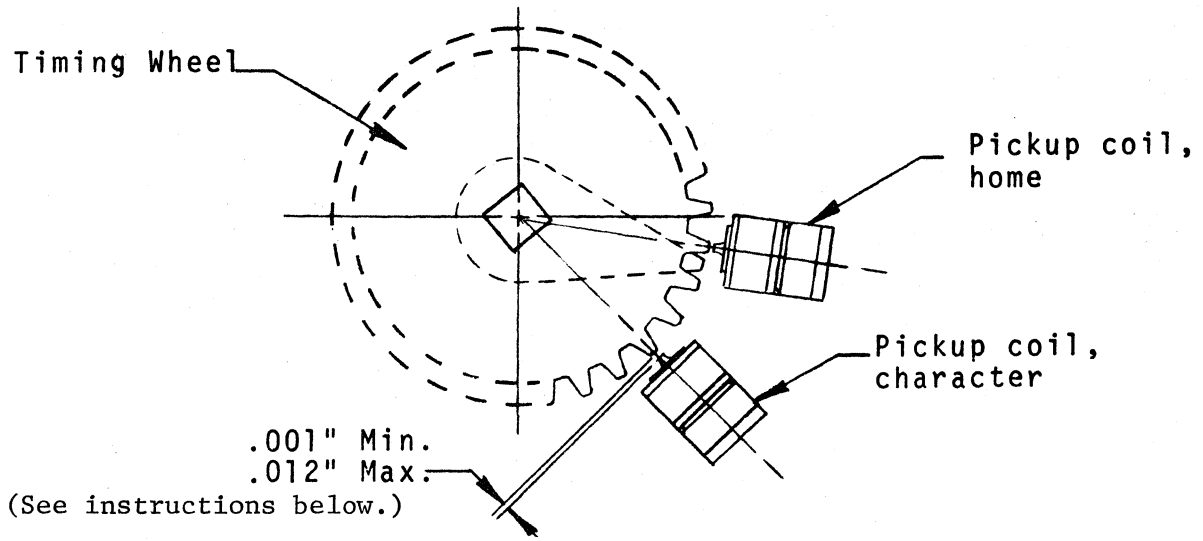


FIGURE 3-5

(1) Initially the gap between the magnet poles and the timing wheel teeth and home tab should be set for .001" minimum and .012" maximum, by positioning the magnet brackets and/or slight forming of the coil bracket as required. The actual clearance will be determined by setting the gap for the specified output voltage specified in Step 2 (below).

(2) The output voltage of the home and character pickup coils should be adjusted to meet the following specifications:

Home Pickup Coil: 2 to 10 volts.

Character Pickup: 2 to 10 volts.

(3) To check, connect a scope to the coil output terminal under test (DC card terminals 1 and 3). With the printer running, observe the output voltage waveform. The output waveform should appear as shown in Figure 3-6 .

(4) Stop the printer and readjust the gaps as required to achieve the proper output. Before starting the printer, manually check for safe clearance between the teeth and the magnet poles.

NOTE: Make sure that the voltage output of the home pickup coil is <u>less than</u> or <u>equal to</u> the outputs of the character pickup coil.

The following signal shapes should be observed on the oscilloscope for the pickup outputs.

3-2.0 PRINTER ADJUSTMENTS (Cont.)

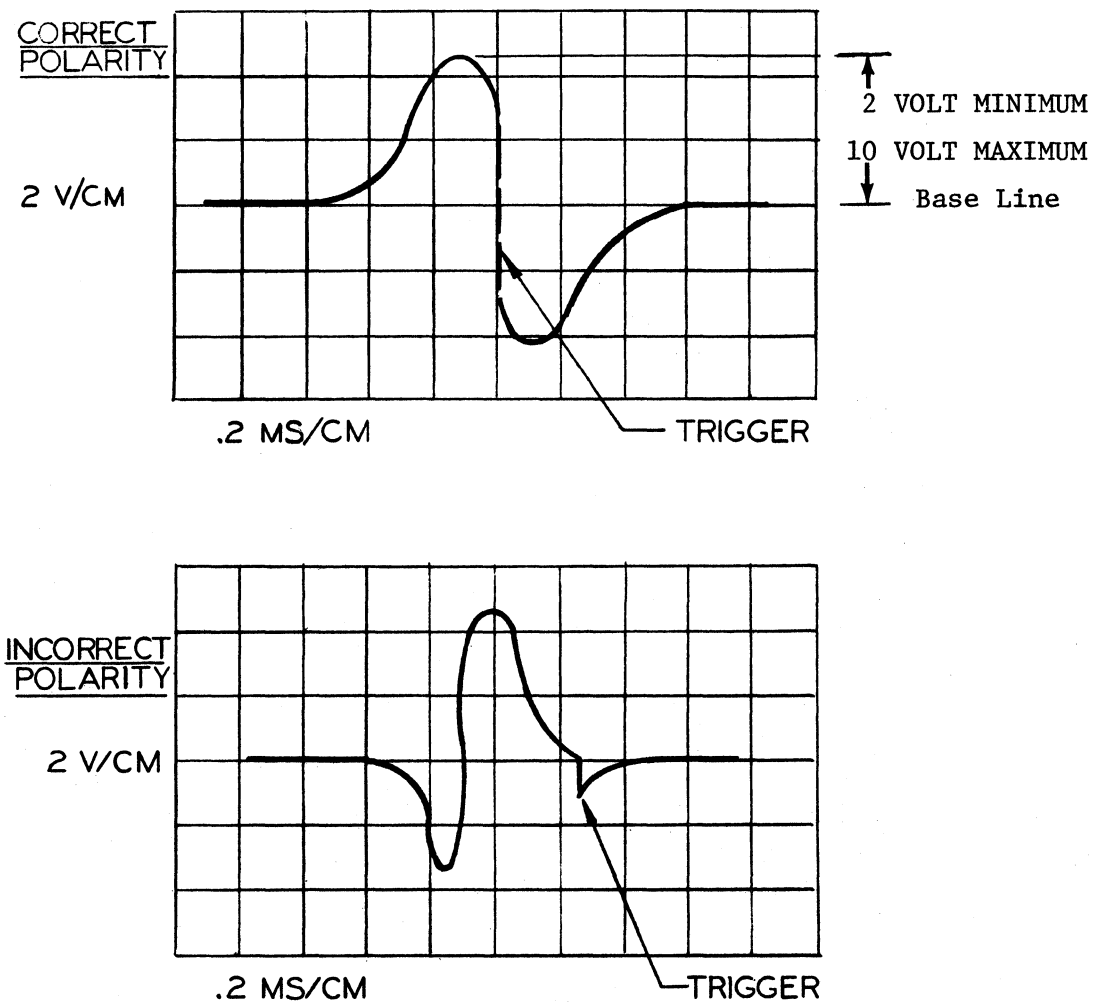


FIGURE 3-6

3-2.0 PRINTER ADJUSTMENTS (Cont.)

3-2.7 SCREW SHAFT TO PRINT SHAFT TIMING

(1) Loosen the two setscrews securing the screw shaft pulley. Then, with the allen wrench in screw A, hold the allen wrench against the U-shaped stud as shown in Figure 3-7.

(2) Disengage the timing belt.

(3) Depress the pin hammer and rotate the screw shaft by means of the slot in its left end until the pin engages the screw shaft thread. Then, gently rotate the screw shaft in the reverse direction until the pin stops against the end of the thread.

(4) Mark the position of the screw shaft by means of a pencil mark adjacent to the slot in the screw shaft.

(5) Rotate the screw shaft 180° $^{+10^\circ}_{0^\circ}$ in its normal direction.

(6) With the screw shaft pulley still positioned as shown in Figure 3-7, insert a .005" feeler gauge between the pulley and the flange bearing, then tighten the two setscrews.

(7) Rotate the screw shaft until the center of the magnet on the pulley is in line with the center of the reed switch when viewed through the opening in the right side frame. (See Figure 3-8.)

(8) Disengage the timing belt and without changing the position of the screw shaft pulley, rotate the print wheel shaft until the home tab on the timing wheel is in line with its pickup coil as shown in Figure 3-8.

(9) Re-engage the timing belt making sure that the relationship of the screw shaft and print wheel shaft changes as little as possible.

3-2.8 PAPER ADVANCE SWITCH

The micro switch which is depressed by the Paper Advance button on the top cover should be adjusted by loosening the screw on the front plate of the printer and sliding the switch bracket up or down as required. DO NOT BEND the micro switch to adjust.

3-2.9 CLUTCH PAWL

Check to see that the clutch pawl has clearance from the clutch sleeve when the line feed coil is energized. When the coil is deenergized, the pawl rides the sleeve until it falls into the pawl slot, causing the clutch to disengage.

3-2.7 SCREW SHAFT TO PRINT SHAFT TIMING (Cont.)

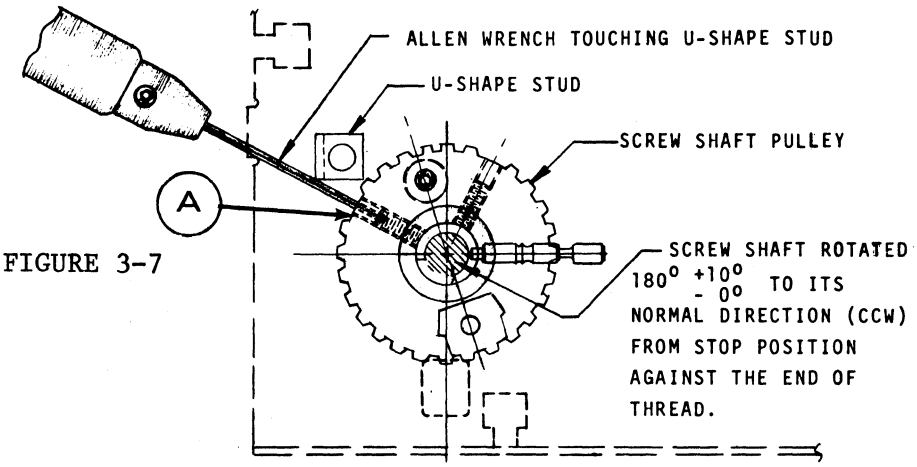


FIGURE 3-7

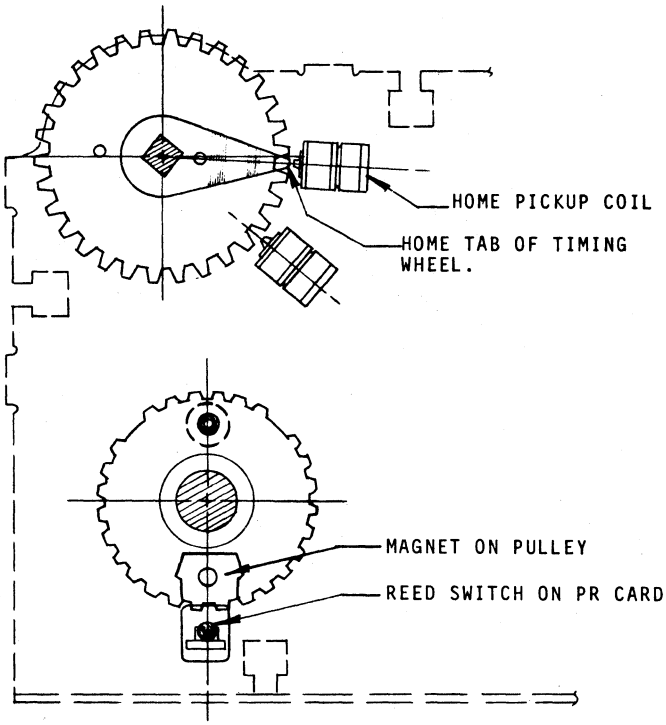


FIGURE 3-8

3-2.0 PRINTER ADJUSTMENTS (Cont.)

3-2.10 PRINT QUALITY

The adjustments affecting print quality are: Transfer Roller, Hammer Drive, Timing Eccentric, and Eccentric Guide Shaft. These four adjustments interact somewhat with each other and it is necessary, therefore, to alternate back and forth among the four adjustments to achieve best print quality. A description of each of the four adjustments is as follows:

1. TRANSFER ROLLER (Inking)

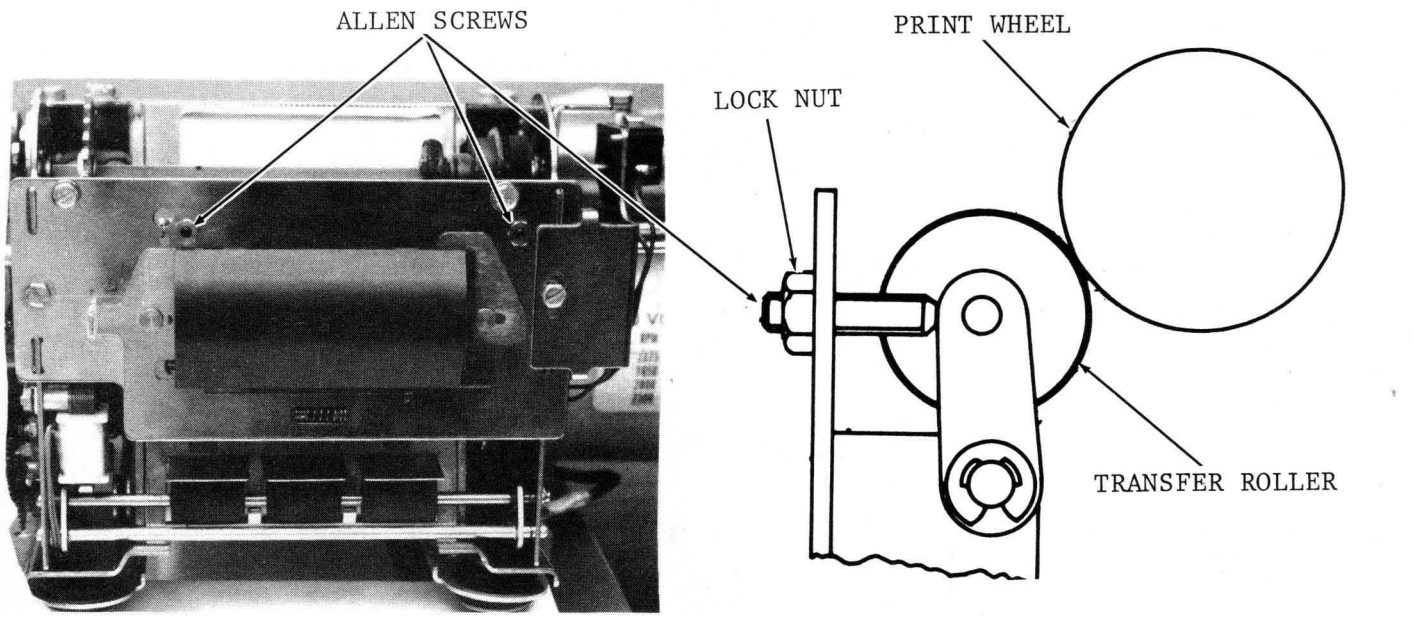


FIGURE 3-9

(1) Loosen the lock nuts and back off the setscrews so that the transfer roller doesn't touch the print wheel or print wheel pulley.

(2) With the print wheel shaft rotating under power, turn the right hand setscrew inward until the transfer roller begins to rotate. Continue turning the screw slowly until no clearance is observed between the transfer roller and drive pulley. Then tighten the lock nut.

(3) Next, turn the left hand setscrew inward while printing a full line of characters (series of 8's) until the darkness of the line is uniform across the paper. Tighten the lock nut. The rough adjustment is now complete.

(4) For fine adjustment, turn the printer off and manually move the print hammer carriage to the left across the full length of the transfer roller to make certain that the print wheel touches the roller at all points.

(5) Make minor adjustments of first one setscrew and then the other until satisfied that the print wheel characters touch lightly and evenly across the full length of the transfer roller surface.

(6) Manually pull the print carriage over both the full and short range and allow to return under carriage return spring tension. Note that no drag of the print wheel on the transfer roller occurs and that the carriage returns to home position.

3-2.10 PRINT QUALITY (Cont.)

(7) Check to see that the locknuts are tight on the Allen screws after adjustment.

NOTE: Machine speed will be affected if the carriage is dragging as a result of the allen screws being in too far. This can be checked by printing a full line of characters for exactly one minute, before and after adjustment. Then compare the number of lines printed before the adjustment and after the adjustment. If fewer lines are printed after adjustment, the carriage is dragging.

2. HAMMER DRIVE (Print Pulse Width)

Attach scope probe to the rear power transistor on the printer driver card. The pulse width must be: 750 $^{+50}_{-100}$ micro seconds. Adjust by turning pot on driver card.

NOTE: Ideally, this control is adjusted by use of an oscilloscope, in the field however, a practical and quick method of adjusting this control is accomplished by turning the control while observing repeated digit 8 printing until best print quality has been obtained without embossing the paper. The adjustment may effect the top or bottom of the character being printed, therefore, the adjustment should be accompanied by adjusting the Timing Eccentric.

3. TIMING ECCENTRIC (Magnetic Pickup Gap)

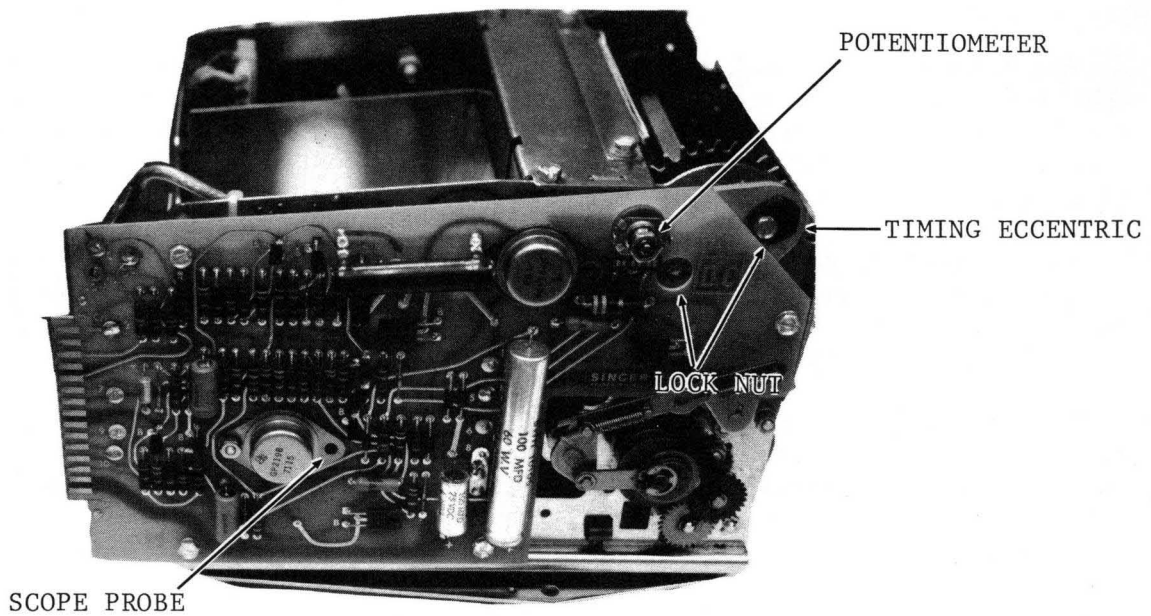


FIGURE 3-10

The magnetic pickup gap adjustment (Adj. 3-2.6) can be varied by the eccentric nut (Figure 3-10) which moves the pickup coil mounting plate. Loosen lock nuts and rotate the eccentric nut to obtain full print with uniform impact. NOTE: Avoid prolonged printing at out-of-time state, or it could cause physical damage to the hammer and print wheel.

3-2.10 PRINT QUALITY (Cont.)

4. ECCENTRIC GUIDE SHAFT (Hammer-Print Wheel Distance)

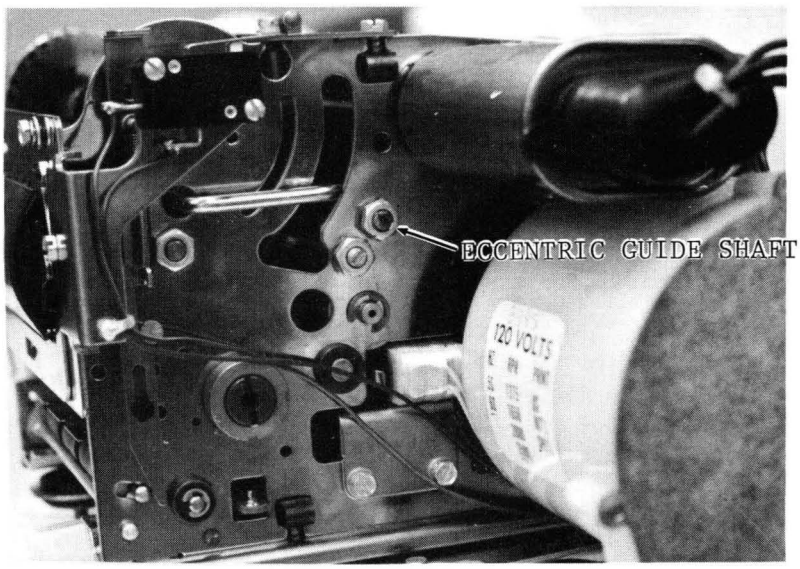


FIGURE 3-11

The Hammer Print Wheel distance can be varied to obtain best print quality by the use of the Eccentric Guide Shaft (Figure 3-11). While observing the printout (series of 8's) and with the eccentric lock nut loose, slowly turn the eccentric guide shaft once around 360 degrees (clockwise); then continue back to the position that gives the best print quality. Secure the lock nut.

The printed characters must appear dark and free of obvious ink starvation and must be distinct and uniformly detailed without flat or missing tops or bottom of characters. Also, the characters must not vary in intensity from one end of the line of print to the other.

If all characters do not print with close to the same degree of quality, it is most likely due to run-out caused by bad print wheel or print shaft, or improperly adjusted hammer assembly and these parts should therefore be replaced.

3-2.11 PAPER DEFLECTOR

If smearing print is observed during the print quality adjustments, it may be necessary to adjust the paper deflector. This is accomplished by gently tapping the paper deflector toward the paper until smearing stops. After adjusting, check to see that the locking screw is tight.

3-3.0 POWER SUPPLY ADJUSTMENT

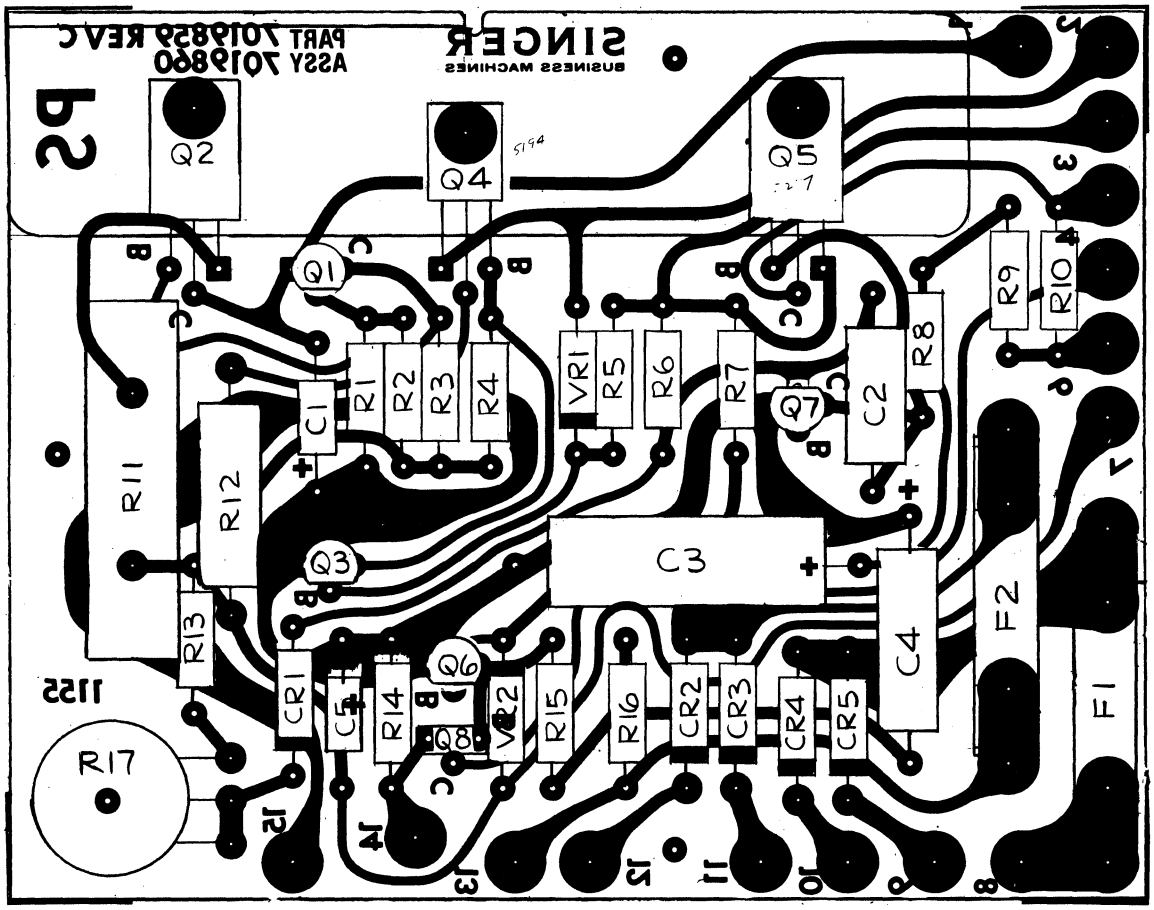


FIGURE 3-12

Adjust potentiometer R17 on the power supply card for an output of +5 volts ±5%. Connet VOM on pin 3.

Check each of the following outputs:

PIN 1 ——————→ -5 volts
PIN 2 ——————→ -9 volts
PIN 3 ——————→ +5 volts
PIN 7 ——————→ -12 volts
PIN 15 ——————→ Ground

3-4.0 MAGNETIC CARD READER

The Model 511 Magnetic Card Reader is factory adjusted using various gages to set the Head position, the card drive shaft angle, etc., therefore, it is not intended that these critical adjustments be made in the field. Other adjustments and checks are as follows:

3-4.1 SWITCH ADJUSTMENTS

The two microswitches must be adjusted so that a magnetic card will operate them reliably. If adjustment is indicated, proceed as follows:

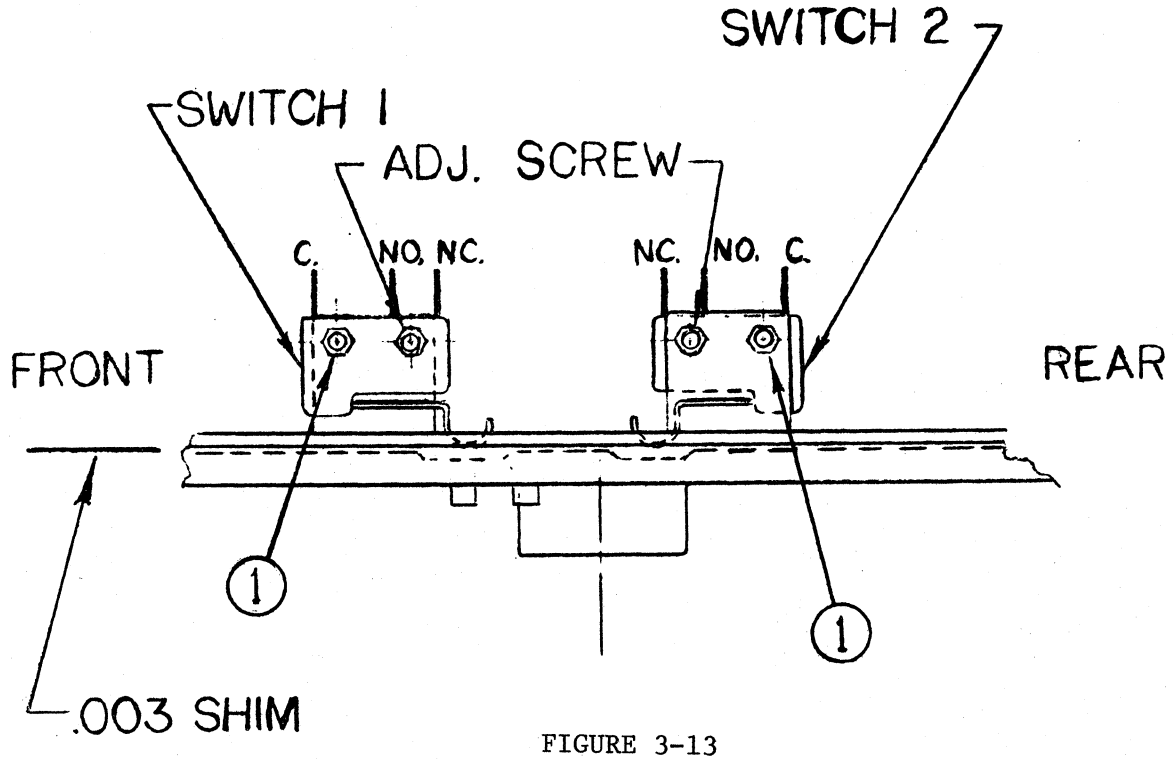


FIGURE 3-13

(1) As shown in Figure 3-13, the screws designated "1" are to be tight, and the two adjustment screws are to be loose.

(2) Attach an ohmmeter to the "C" and "NC" pins of Switch #1.

(3) Set Switch #1 so it will be actuated by an 0.003" thick by 1.5" wide shim stock inserted in the card chute from the FRONT of the card reader. Tighten the adjment screw.

(4) Attach an ohmmeter to the "C" and "NC" pins of Switch #2.

(5) Set Switch #2 so it will be actuated by the same shim stock inserted in the card chute from the REAR of the card reader. Tighten the adjustment screw.

(6) Recheck the operation of both switches by the shim stock and by a magnetic card.

3-4.0 MAGNETIC CARD READER ADJUSTMENTS (Cont.)

3-4.2 +5 VOLT SUPPLY

The 2K ohm potentiometer on the printed circuit board is used to set the +5 volt output. Use a voltmeter connected to the +5 volt output and adjust the potentiometer for an output of +5 volts, $\pm$ 0.1 volt.

3-4.3 MAGNETIC CARDS

Care must be taken to insure that magnetic cards are kept clean. Cards must be stored in their envelopes at all times when not in use. Cards may be cleaned with isopropyl alcohol, and wiped dry with a lint-free cloth or paper, or blown dry with dry, oil-free air.

Maximum life of a magnetic card is 100 passes.

3-4.4 TEST PROGRAM

A recommended test program for the card reader is: 511 program steps of "Enter Exponent". This program has a check sum of: ++732 on the Model 1155 Calculator.

3-4.5 SIGNAL LEVEL CHECK

DC Offset level, Crosstalk voltage, and Play Output Signal voltage should be monitered on each track of the magnetic head as follows:

(1) Equipment required

1. 1155 Programmable Calculator
2. 511 Magnetic Card Reader
3. Pre-programmed card #3.
4. Pre-programmed card #4.
5. Tektronix Model 547 Oscilloscope with 1A1 Plug-in and X1 probe (or equivalent).

(2) Tests

1. Set oscilloscope to 1V/cm, 0.5 msec/cm. Set INPUT SELECTOR to GROUND, and center track on the center line.
2. Attach oscilloscope to U12, pin 7 with ground on card reader chassis.
3. Set Input Selector to DC.
4. Turn on power to calculator and card reader.
5. Read DC offset level = 0V $\pm$ 0.15V maximum as shown in Figure 3-14.
6. Load from Card pre-programmed Card #4 and observe sum of DC offset level and crosstalk voltage = 0V $\pm$ 0.3V maximum as shown in Figure 3-14.
7. Load from Card pre-programmed Card #3 and observe output signal voltage = +0.7V minimum and -0.7V minimum as shown in Figure 3-14.
8. Repeat steps 4 through 7 with the scope attached to U12, pin 1.
9. Repeat steps 4 through 7 with the scope attached to U25, pin 1.
10. Repeat steps 4, 5, and 7 with the scope attached to U25, pin 7.

(3) Oscillator Frequency: The frequency of the oscillator is measured at U5, pin 9. The measured frequency must be: 40kHz $\pm$ 7% (37.2kHz to 42.8kHz).

3-5.0 PC CARD COMPONENT LAYOUT & SCHEMATICS

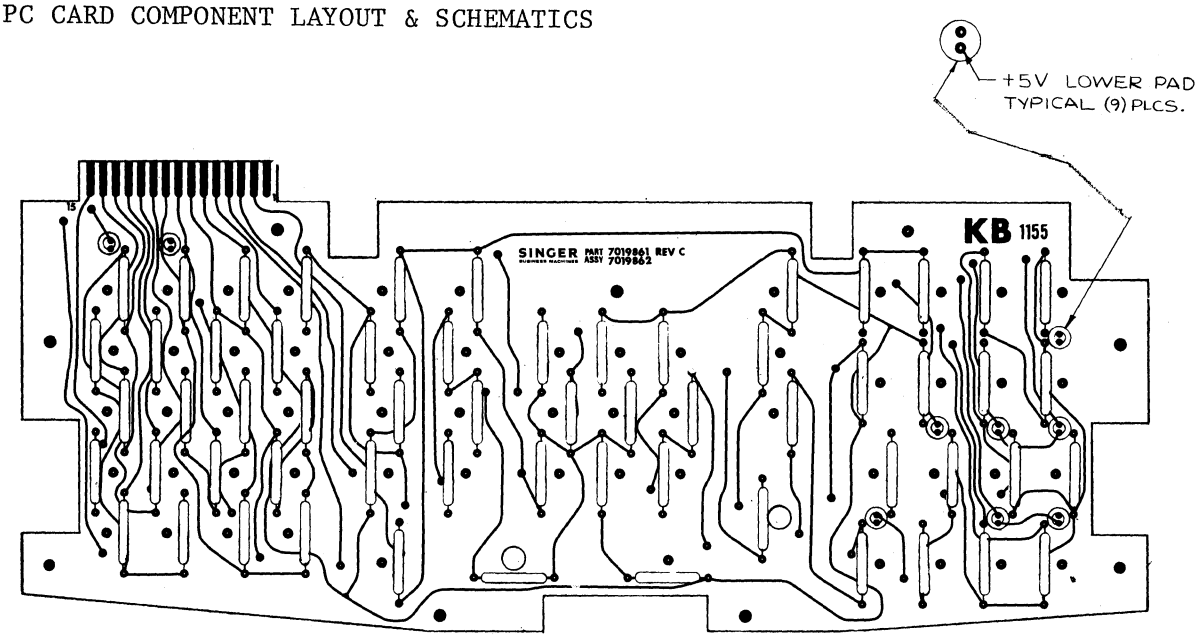


FIGURE 3-15

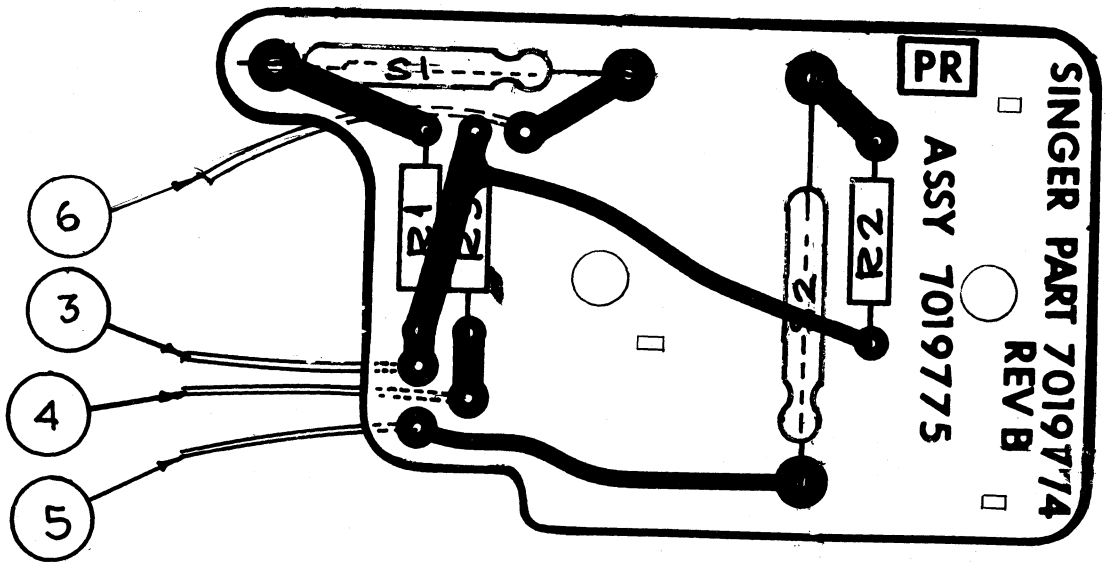


FIGURE 3-16

3-4.5 SIGNAL LEVEL CHECK (Cont.)

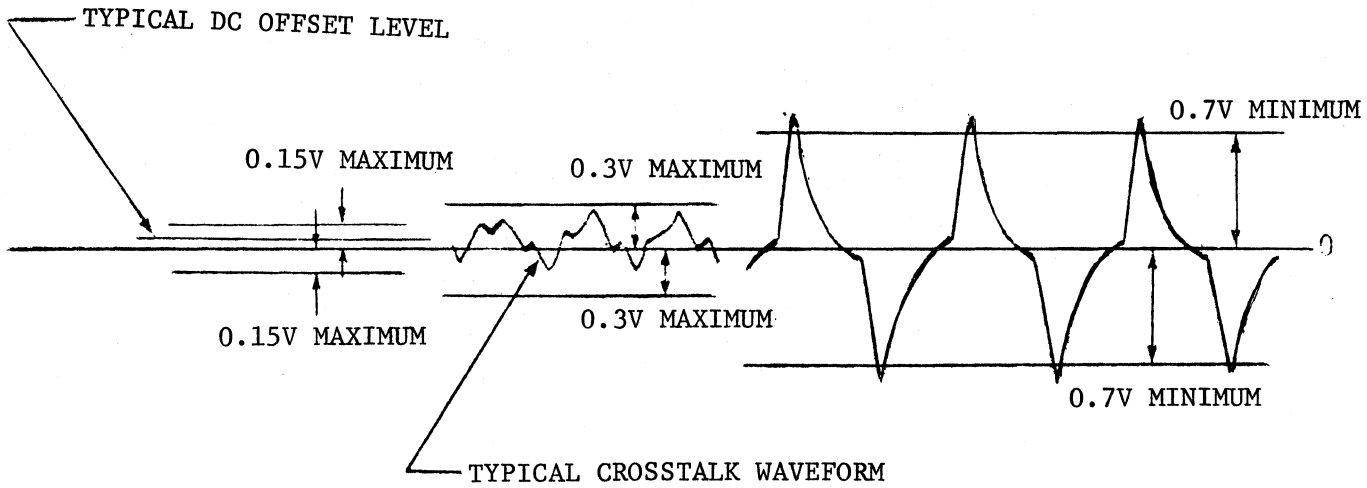


FIGURE 3-14

3-4.6 CARD READER CLEANING

The card chute should be cleaned periodically, using air pressure at approximately 15 psi.

3-5.0 PC CARD COMPONENT LAYOUT & SCHEMATICS (Cont.)

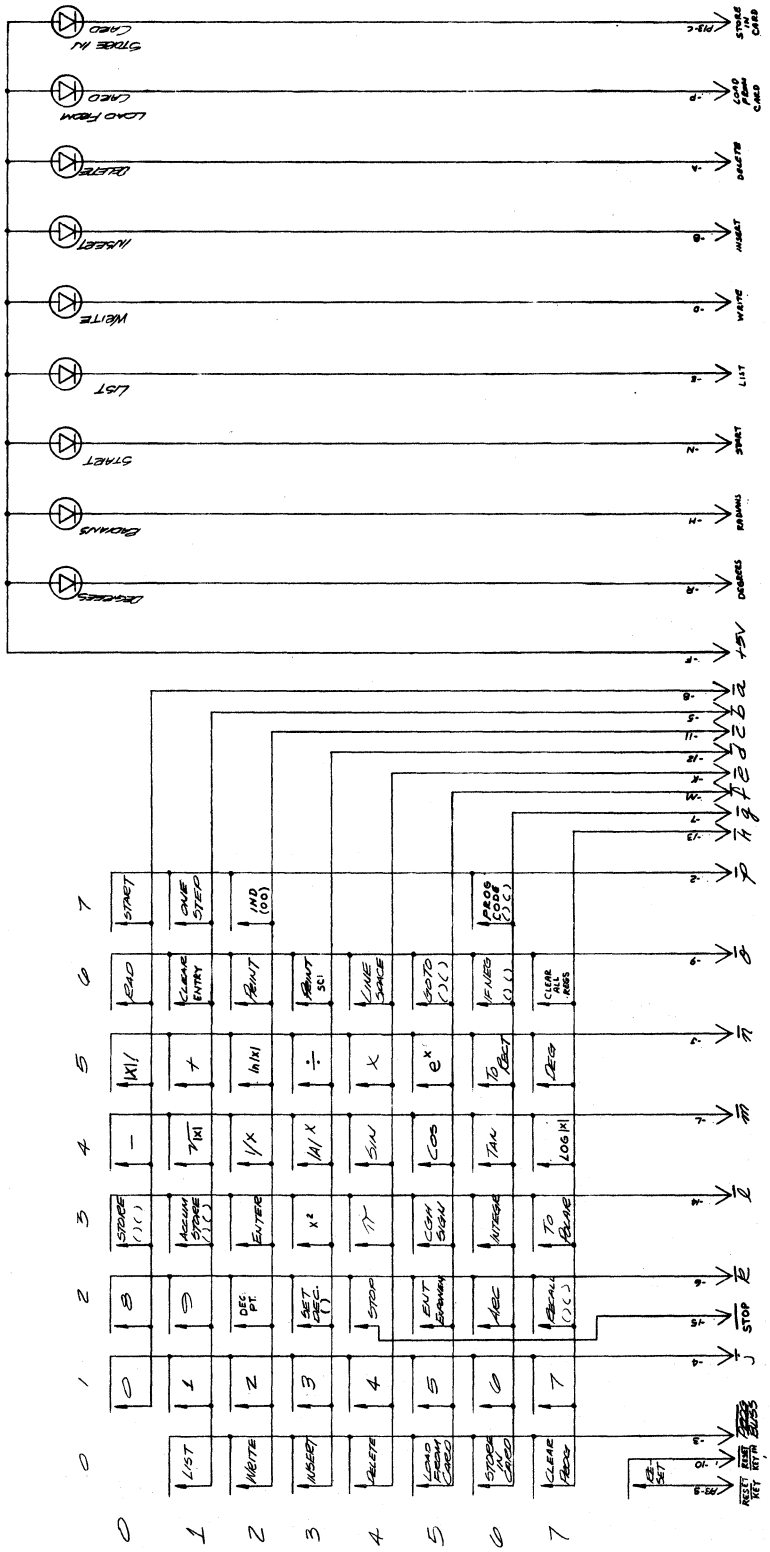


FIGURE 3-17

3-5.0 PC CARD COMPONENT LAYOUT & SCHEMATICS

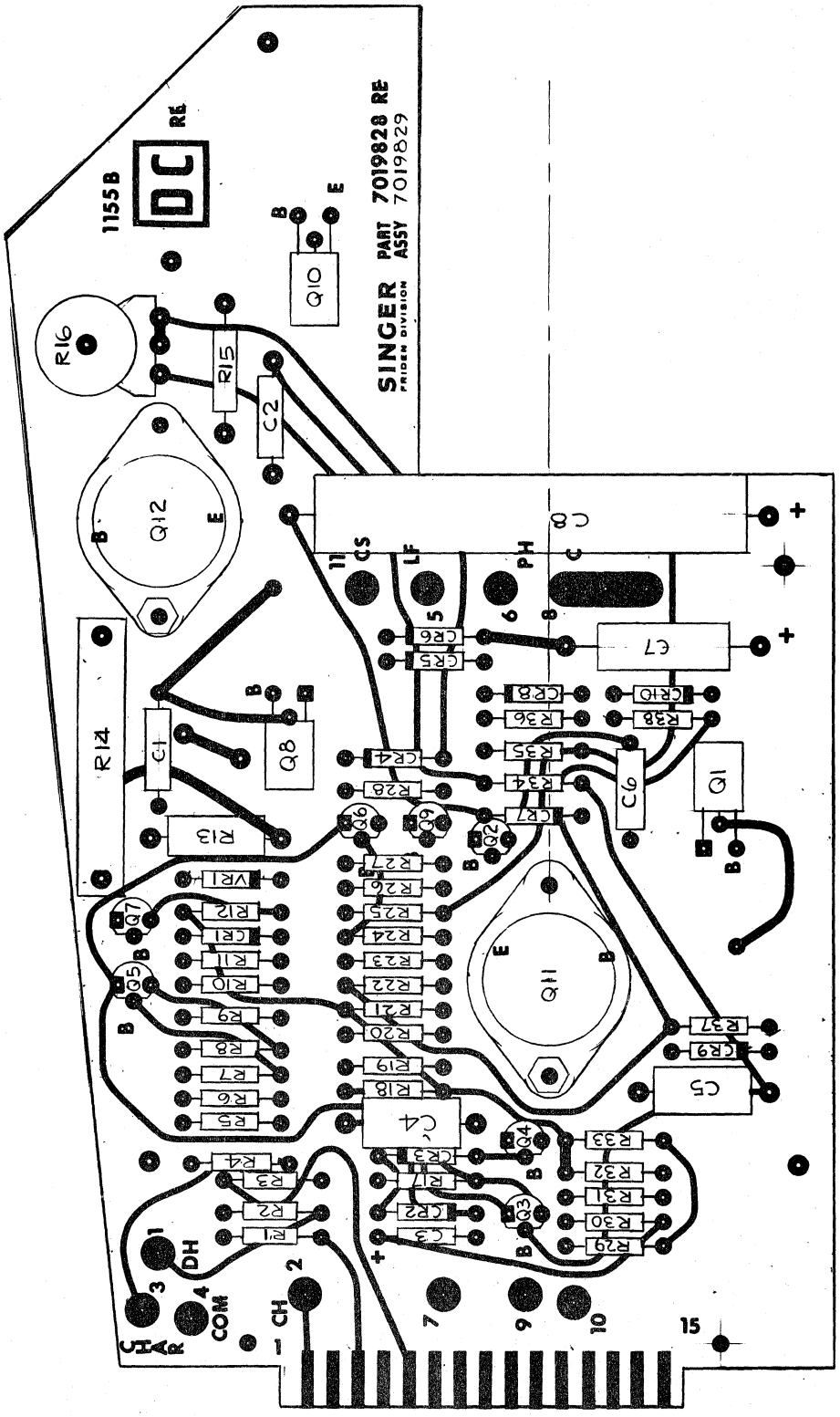


FIGURE 3-18

3-5.0 PC CARD COMPONENT LAYOUT & SCHEMATICS (Cont.)

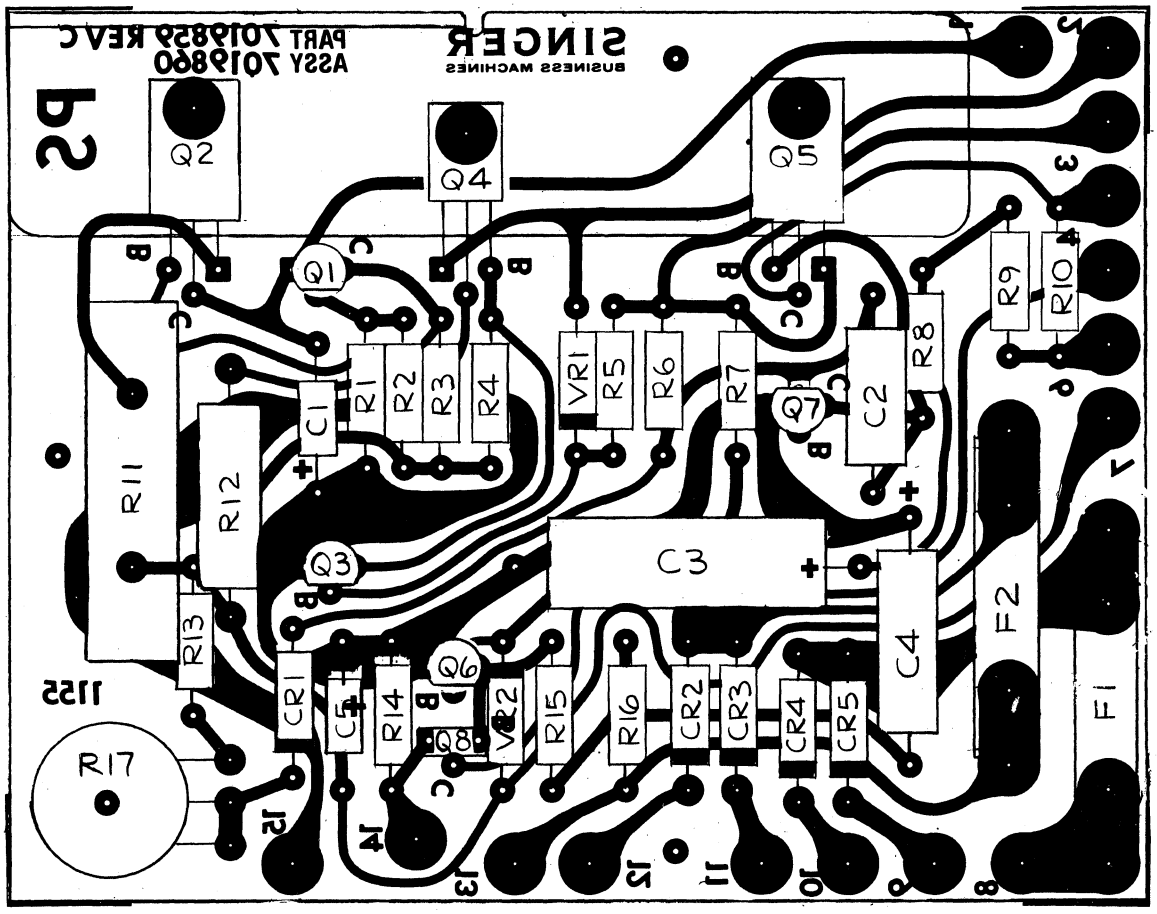


FIGURE 3-19

3-5.0 PC CARD COMPONENT LAYOUT & SCHEMATICS (Cont.)

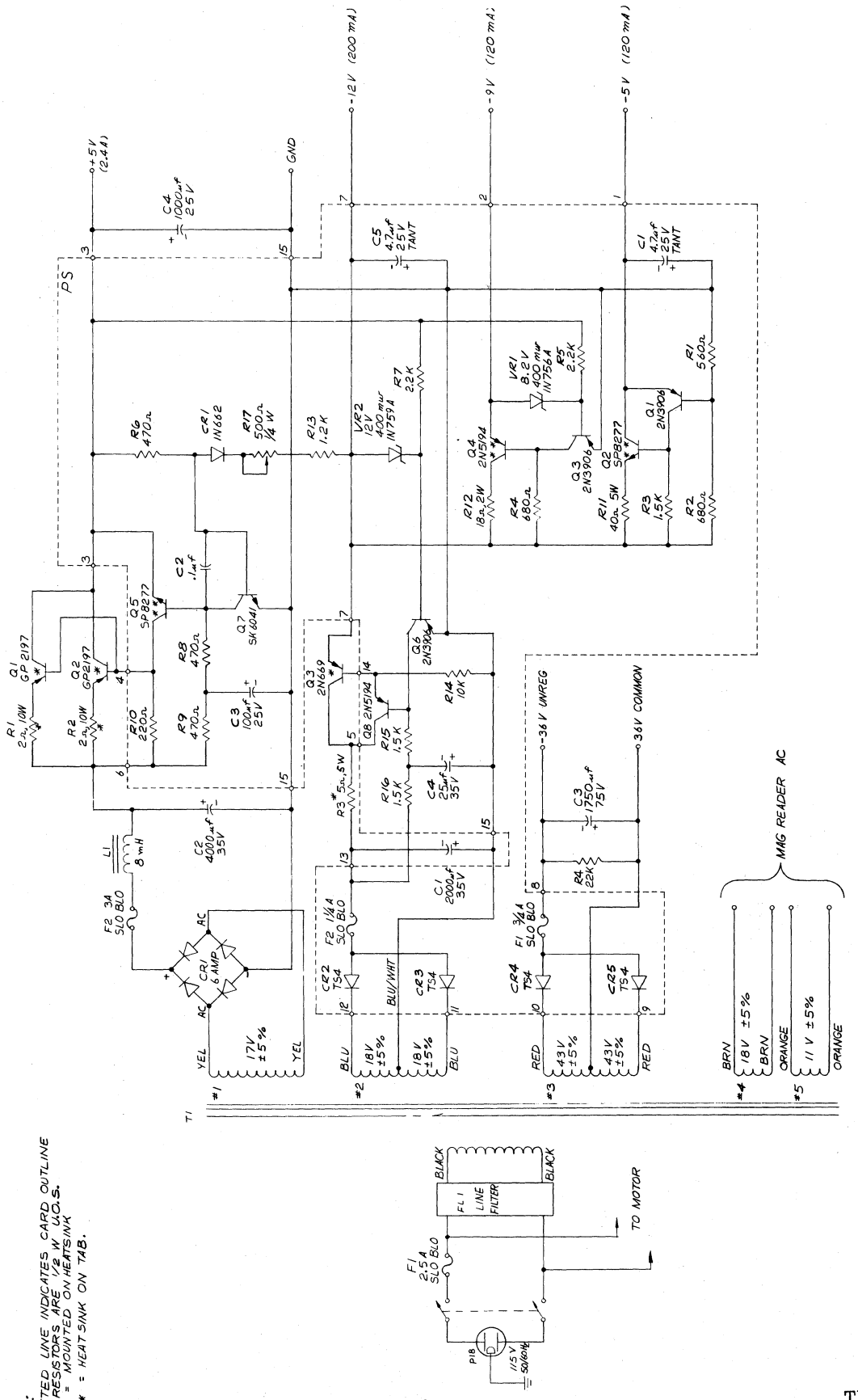


FIGURE 3-20

3-5.0 PC CARD COMPONENT LAYOUT & SCHEMATICS (Cont.)

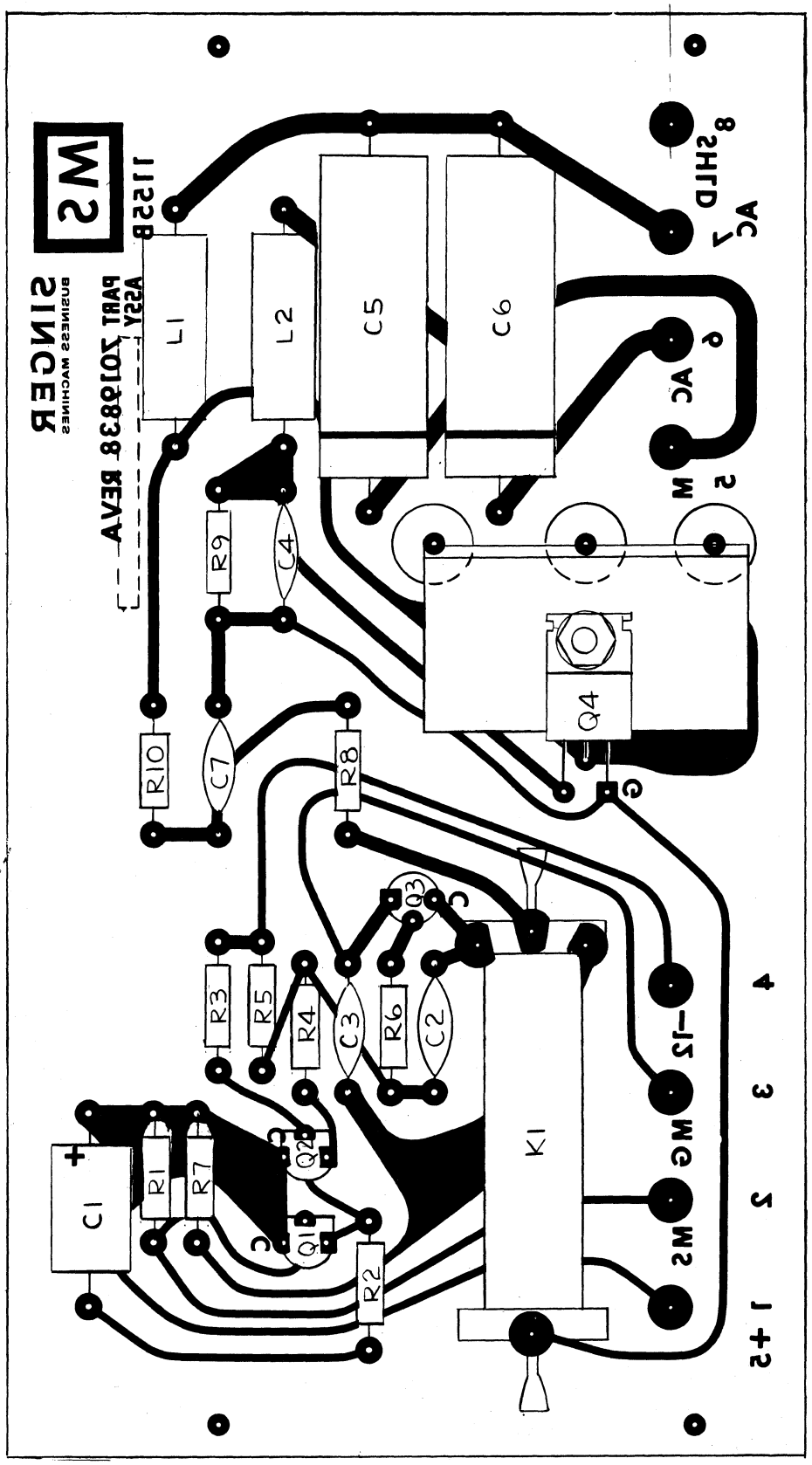


FIGURE 3-22

3-5.0 PC CARD COMPONENT LAYOUT & SCHEMATICS (Cont.)

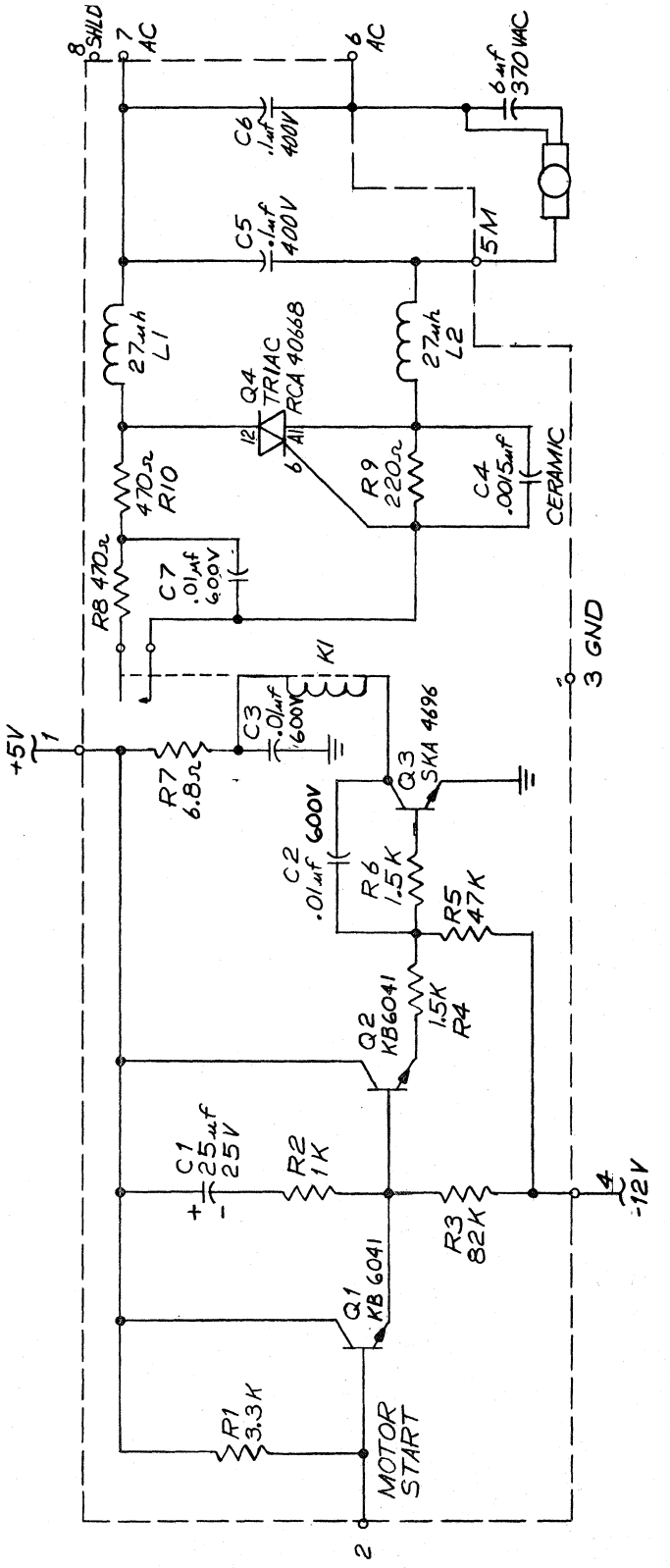


FIGURE 3-21

NOTE:
ALL RESISTORS ±5%, 1/2 W

3-5.0 PC CARD COMPONENT LAYOUT & SCHEMATICS (Cont.)

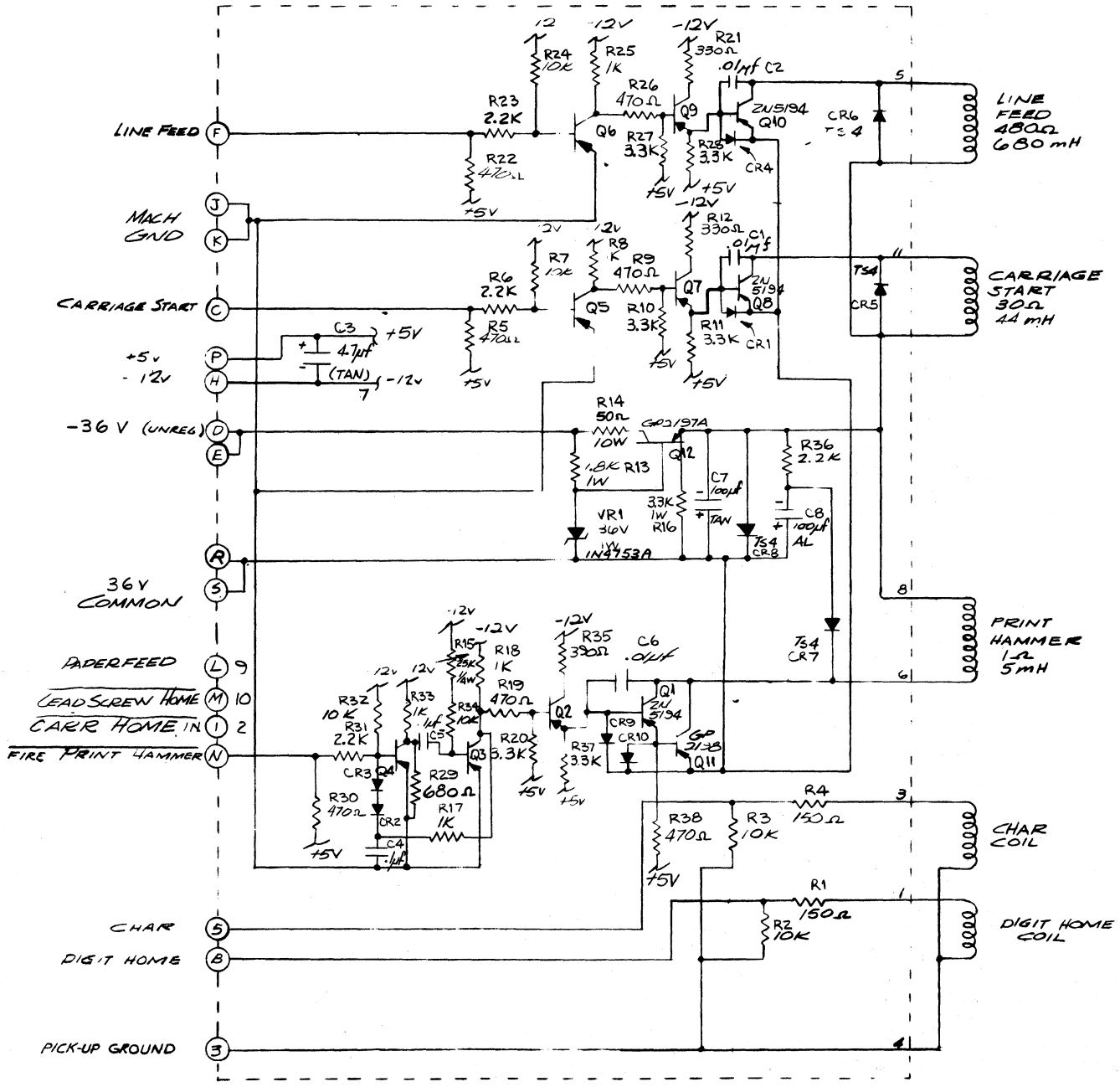


FIGURE 3-23

3-5.0 PC CARD COMPONENT LAYOUT & SCHEMATICS (Cont.)

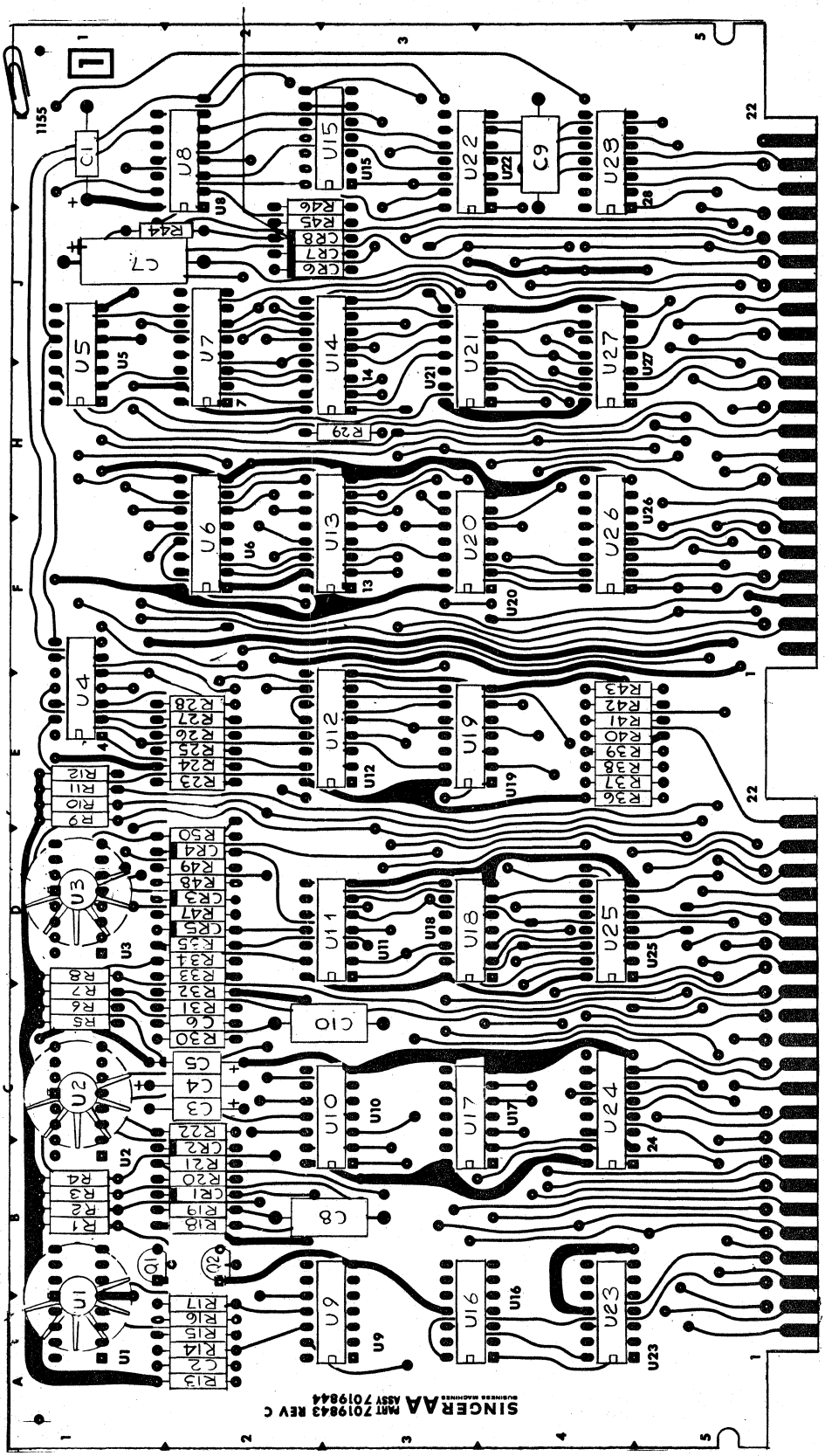


FIGURE 3-24

3-5.0 PC CARD COMPONENT LAYOUT & SCHEMATICS (Cont.)

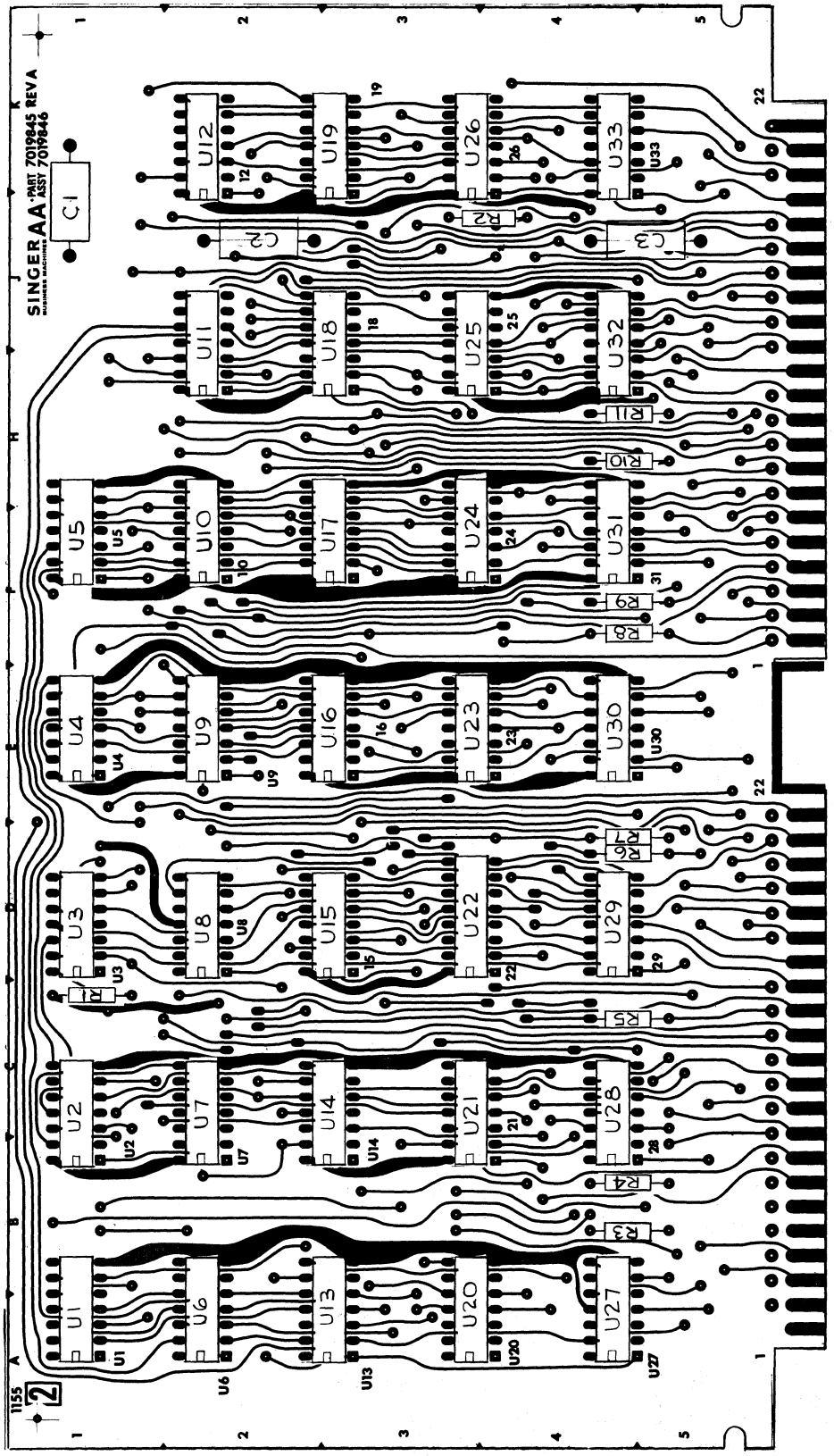


FIGURE 3-25

3-5.0 PC CARD COMPONENT LAYOUT AND SCHEMATICS (Cont.)

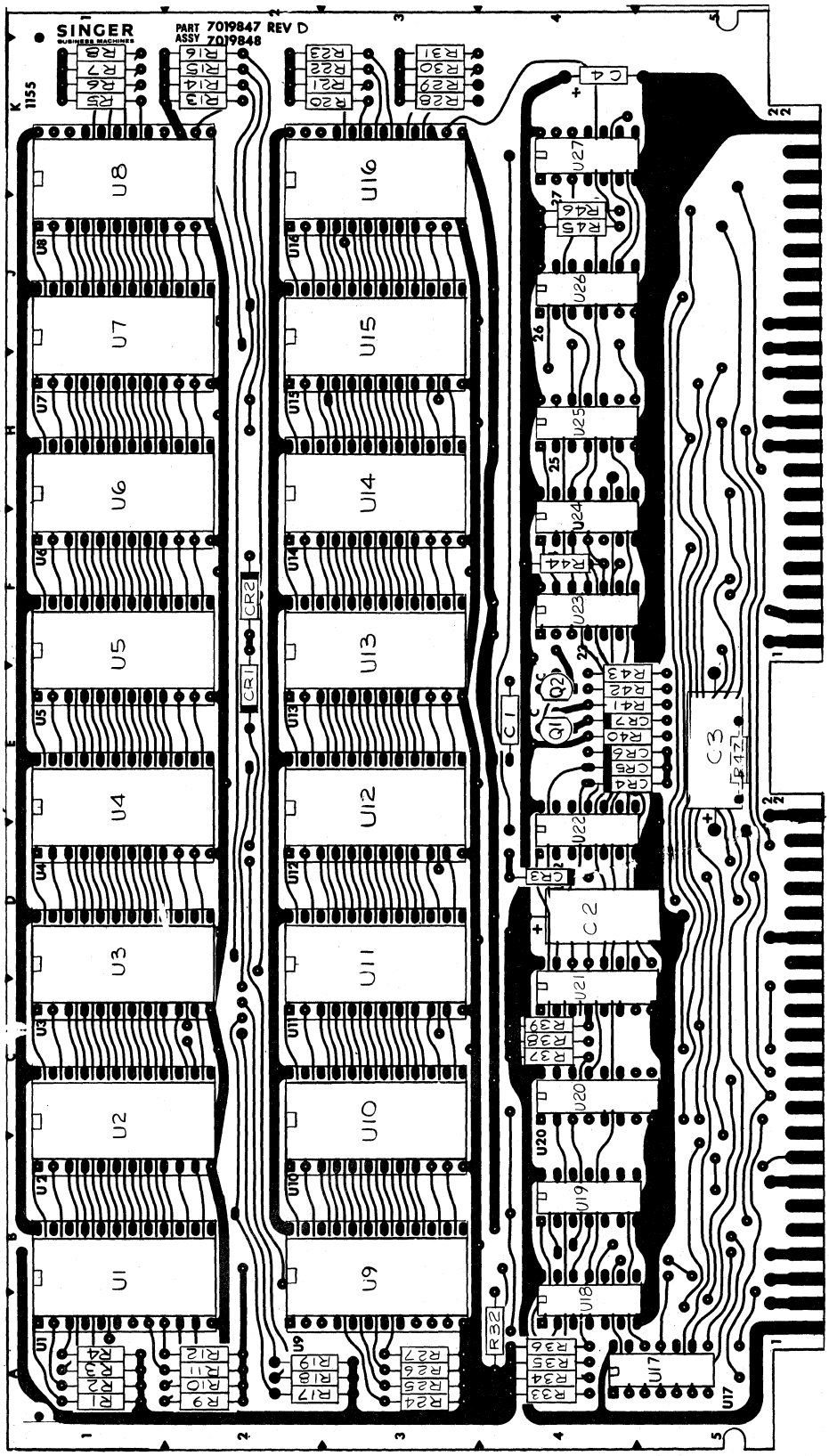


FIGURE 3-26

3-5.0 PC CARD COMPONENT LAYOUT & SCHEMATICS (Cont.)

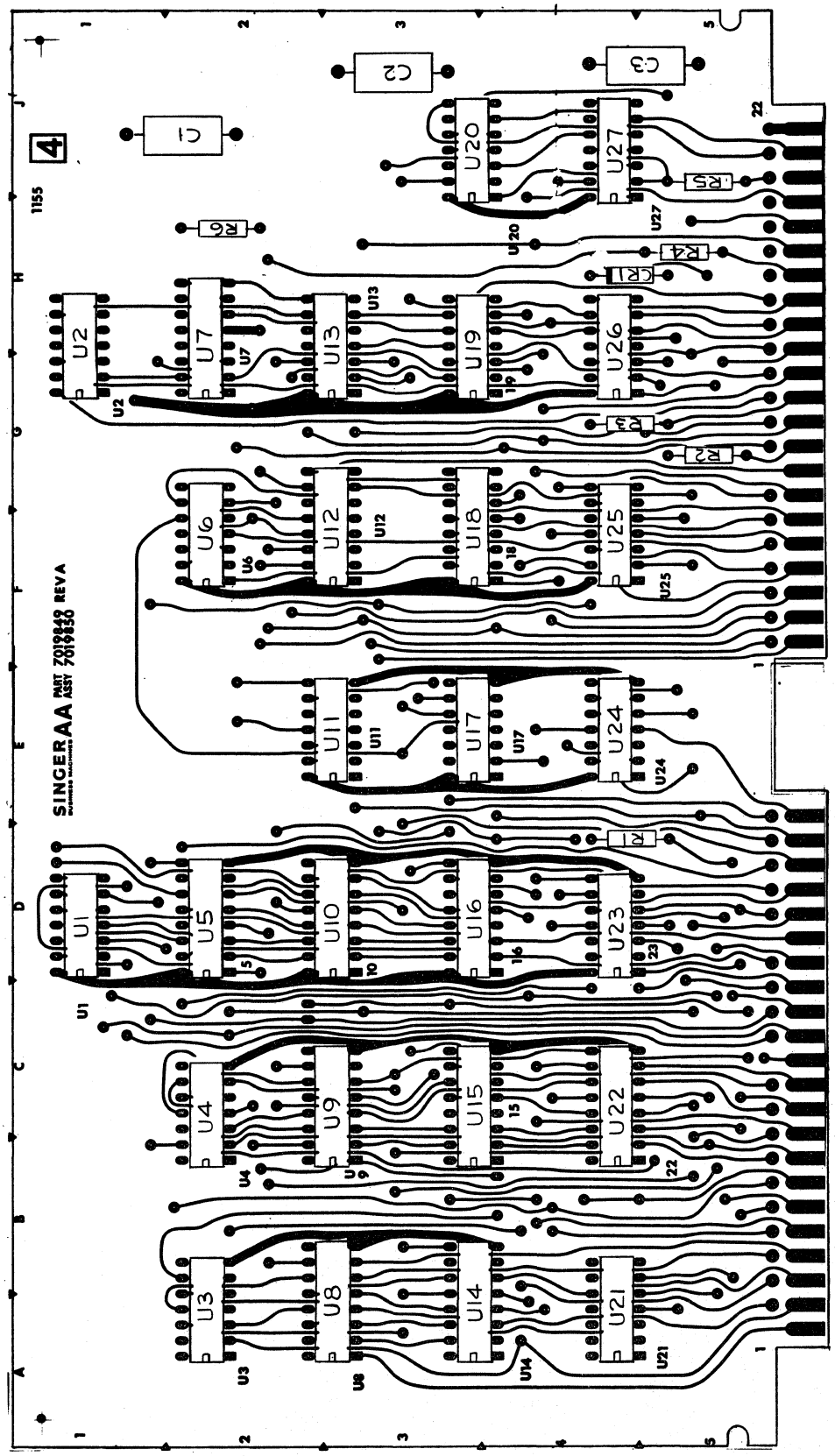


FIGURE 3-27

3-5.0 PC CARD COMPONENT LAYOUT & SCHEMATICS (Cont.)

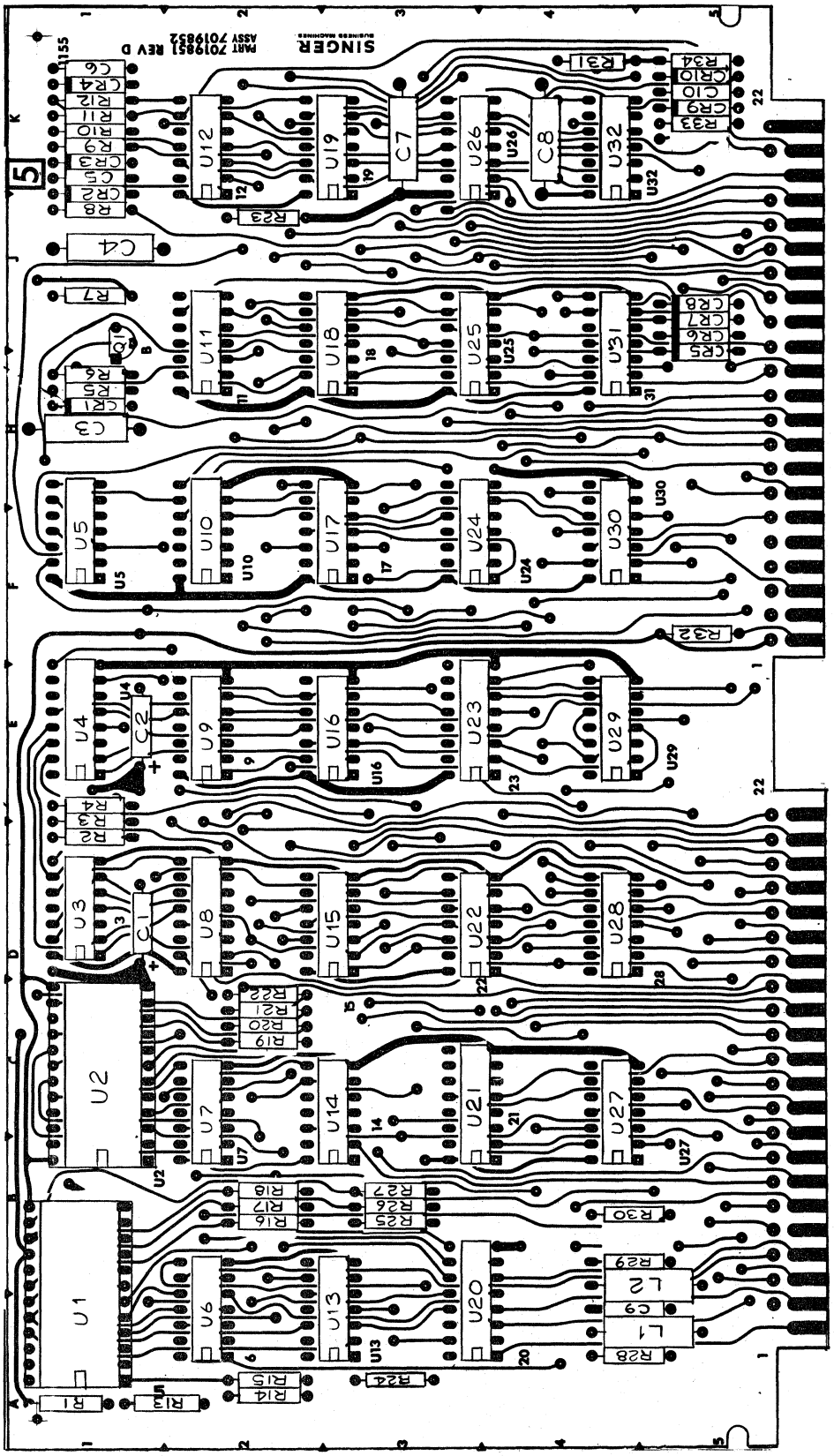


FIGURE 3-28

3-5.0 PC CARD COMPONENT LAYOUT & SCHEMATICS (Cont.)

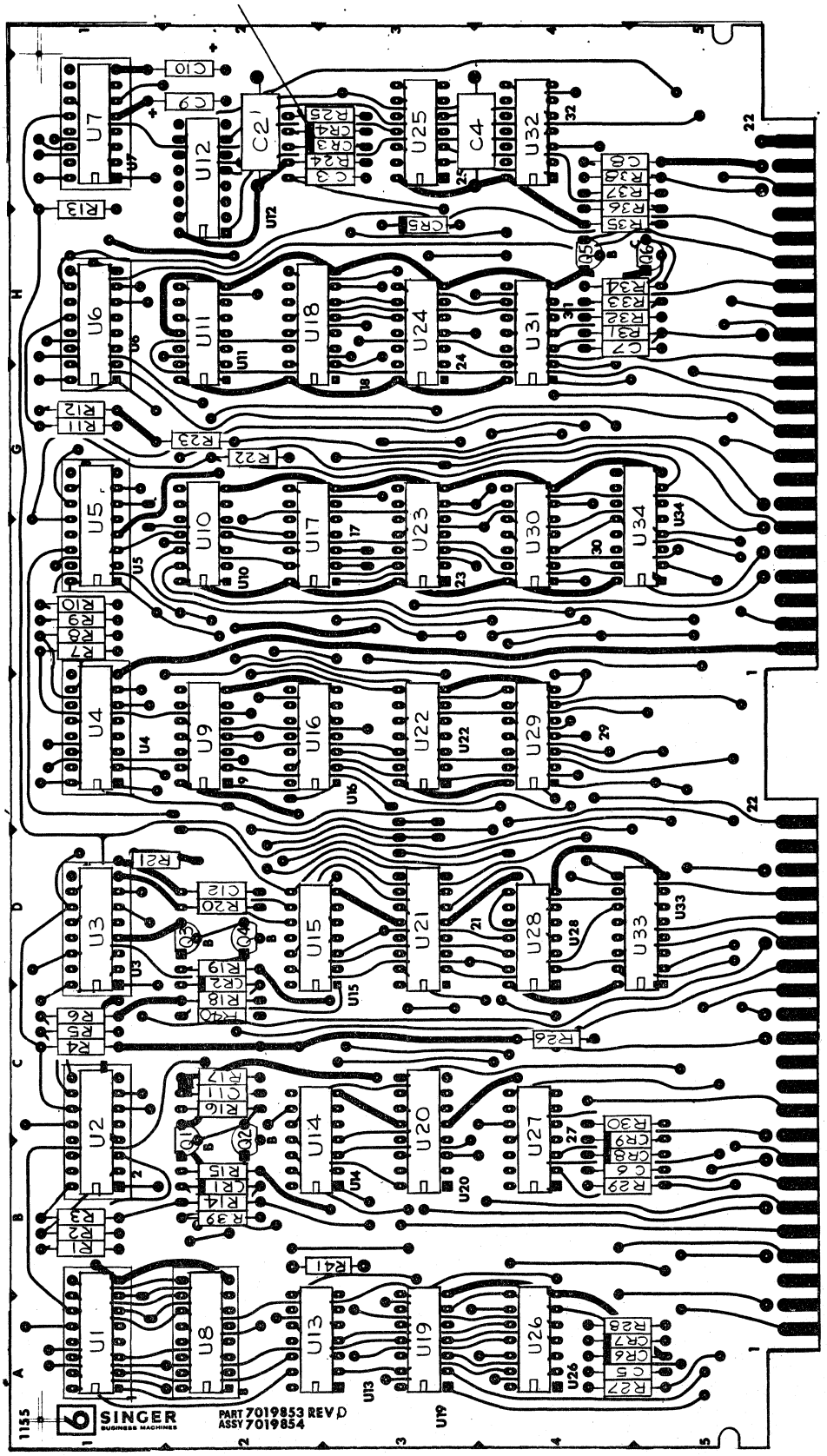


FIGURE 3-29

3-6.0 MOTHER BOARD WIRING LIST

SIGNAL NAME	CARD 1	CARD 2	CARD 3	CARD 4	CARD 5	CARD 6
$\overline{a}$ (P13-8)	XP1-1					
$\overline{b}$ (P13-5)	XP1-B					
$\overline{c}$ (P13-11)	XP1-2					
$\overline{d}$ (P13-12)	XP1-10				XP9-10	
$\overline{e}$ (P13-K)	XP1-22			XP7-22		
$\overline{f}$ (P13-M)	XP1-11				XP9-M	
$\overline{g}$ (P13-7)	XP2-5					
$\overline{h}$ (P13-13)	XP2-M					
$\overline{i}$	XP2-12			XP8-11		
$\overline{j}$ (P13-4)	XP1-3					
$\overline{k}$ (P13-6)	XP1-4					
$\overline{l}$ (P13-14)	XP1-8					
$\overline{m}$ (P13-L)	XP1-12					
$\overline{n}$ (P13-J)	XP1-15					
$\overline{o}$ (P13-9)	XP1-21					
$\overline{p}$ (P13-2)	XP1-X	XP3-20			XP9-X	
p0				XP8-H	XP10-7	
p1				XP7-Y	XP9-21	
p2				XP8-8	XP10-J	
AØ				XP8-4		XP12-D
A1				XP8-E		XP12-E
A2				XP8-F		XP12-F
ADV H200	XP1-C	XP3-3				
ADV MARKER CTR	XP1-D	XP3-4				
C					XP9-E	XP11-5
$\overline{\text{CARR HOME IN}}$ (P14-1)					XP9-8	
CARR START (P14-C)						XP11-P
CHAR COIL (P14-5)						P12-R
$\overline{\text{CLR LINE}}$	XP1-J	XP3-8				
D		XP4-13		XP8-P		
$\overline{D}$		XP4-10		XP8-L	XP10-10	
DEGREES LED (P13-R)				XP8-X		
DELETE LED (P13-A)		XP3-R				
DIGIT COIL (P14-B)						P12-X
EN L18				XP8-21	XP10-21	

3-6.0 MOTHER BOARD WIRING LIST (Cont.)

SIGNAL NAME	CARD 1	CARD 2	CARD 3	CARD 4	CARD 5	CARD 6
EN SET C					XP9-F	XP11-6
$\overline{F}$					XP9-H	XP11-7
FIRST DATA	XP1-P	XP3-13				
$\overline{\text{FIRST DATA}}$	XP1-R	XP3-14				
$\overline{F100}$					XP9-J	XP11-8
$\overline{F101}$					XP9-L	XP11-10
$\overline{F103.T4}$					XP9-S	XP11-15
$\overline{F104.T4}$					XP9-T	XP11-16
$\overline{F106}$					XP9-U	XP11-17
$\overline{F200+F203}$					XP9-W	XP11-19
$\overline{F202}$		XP3-T			XP9-15	
$\overline{F203}$					XP9-Z	XP11-22
$\overline{F204}$				XP7-T	XP9-16	
$\overline{F206}$					XP10-K	XP12-9
$\overline{F301}$				XP7-N	XP9-12	
$\overline{F304}$				XP7-12	XP9-N	
$\overline{F305}$				XP7-R	XP9-14	
$\overline{F402}$				XP7-13	XP9-P	
$\overline{F403}$		XP3-P			XP9-R	
$\overline{F407}$					XP10-L	XP12-10
$\overline{F407.Q3}$				XP7-P	XP9-13	XP11-P
$\overline{\text{FIRE PRINT HAMMER}}$ (P14-N)						XP11-J
HI M.B. IN					XP9-C	
HI JUMPER OUT					XP9-3	
$\overline{H20}$	XP1-5	XP3-15				
H55	XP1-T	XP3-16				
H57	XP1-U	XP3-17				
$\overline{H57}$	XP1-V	XP3-18				
H203	XP1-W	XP3-19				
$\overline{H204}$	XP1-N	XP3-12				
$\overline{H206}$	XP1-H	XP3-7				
$\overline{H210}$		XP4-S		XP8-15		
H211		XP3-22		XP7-Z		
$\overline{H213}$	XP1-K	XP3-9				
$\overline{H214}$		XP4-W		XP8-19		

3-6.0 MOTHER BOARD WIRING LIST (Cont.)

SIGNAL NAME	CARD 1	CARD 2	CARD 3	CARD 4	CARD 5	CARD 6
$\overline{H215}$	XP2-B	XP4-2				
$\overline{H216}$		XP4-A		XP8-1		
$\overline{H217}$	XP1-F			XP7-6		
$\overline{H218}$	XP2-D	XP4-4				
$\overline{H224}$		XP4-P		XP8-13		
$\overline{H227}$		XP4-9		XP8-K		
$\overline{H234}$	XP2-E	XP4-5		XP8-5		
$\overline{H236}$	XP2-F	XP4-6				
$\overline{H238}$	XP2-J	XP4-8				
H240	XP2-R	XP4-14				
H250	XP2-Y	XP4-21				
$\overline{H300}$		XP4-T		XP8-17		
$\overline{H301}$		XP3-S		XP7-S		
$\overline{H306}$	XP2-U	XP4-17				
$\overline{ILLEGAL}$		XP4-15		XP8-S		
INSERTED (P13-B)		XP3-K				
K	XP2-4			XP8-D		
K'		XP4-V		XP8-18		
$\overline{K'}$		XP4-R		XP8-14		
K1000	XP2-14			XP8-R		
$\overline{K3004}$					XP10-M	XP12-11
$\overline{L4}$					XP10-N	XP12-12
L5					XP10-P	XP12-13
L8					XP10-R	XP12-14
$\overline{L16}$	XP2-N	XP4-12		XP8-N	XP10-12	
L24				XP7-9	XP9-K	
L26				XP7-W	XP9-19	
L29				XP7-M	XP9-11	
L31			XP5-K	XP7-K	XP9-9	
L32				XP7-X	XP9-20	
L33					XP10-S	XP12-15
$\overline{L50}$					XP10-T	XP12-16
$\overline{L70}$				XP8-6		XP12-H
LINE FEED (P14-F)						XP11-K

3-6.0 MOTHER BOARD WIRING LIST (Cont.)

SIGNAL NAME	CARD 1	CARD 2	CARD 3	CARD 4	CARD 5	CARD 6
LIST LED (P13-E)		XP3-U				
LOAD FROM CARD LED(P13-P)		XP3-V				
$\overline{\text{LS HOME IN}}$ (P14-M)						XP11-L
M0			XP5-8	XP7-J		
M1			XP5-L	XP7-10		
M2			XP5-J	XP7-8		
M3			XP5-7	XP7-H		
M4			XP5-C	XP7-3		
M5			XP5-3	XP7-C		
M6			XP5-B	XP7-2		
M7			XP5-R	XP7-14		
M8			XP5-u	XP7-U		
$\overline{\text{M8}}$			XP5-S	XP7-15		
M9			XP5-17	XP7-17		
M10			XP5-T	XP7-16		
M11			XP5-W	XP7-19		
MOTOR START (MS-2)						XP11-P
$\overline{\text{NEW POINT}}$ (PM-6)					XP9-7	
$\overline{\text{OUT 1}}$ (P17-1)			XP6-9			
$\overline{\text{OUT 2}}$ (P17-2)			XP6-10			
$\overline{\text{OUT 4}}$ (P17-3)			XP6-12			
$\overline{\text{OUT 8}}$ (P17-4)			XP6-13			
PØ			XP6-B	XP8-2		XP12-B
P1			XP6-2	XP8-B		XP12-2
P2			XP5-X	XP7-20		XP11-X
$\overline{\text{P2}}$			XP6-A	XP8-A		
P3			XP5-V	XP7-18	XP9-V	XP11-18
P4			XP5-A	XP7-1	XP9-1	XP11-1
P5			XP5-2	XP7-B	XP9-2	XP11-B
P6			XP5-4	XP7-0	XP9-4	XP11-D
P7			XP5-D	XP7-4	XP9-D	XP11-4
$\overline{\text{P3.P4.P5.P6.P7}}$			XP6-L	XP8-10		
$\overline{\text{PAPER FEED IN}}$ (P14-L)						XP11-5
$\overline{\text{PLAY}}$ (P15-13)		XP3-Y				

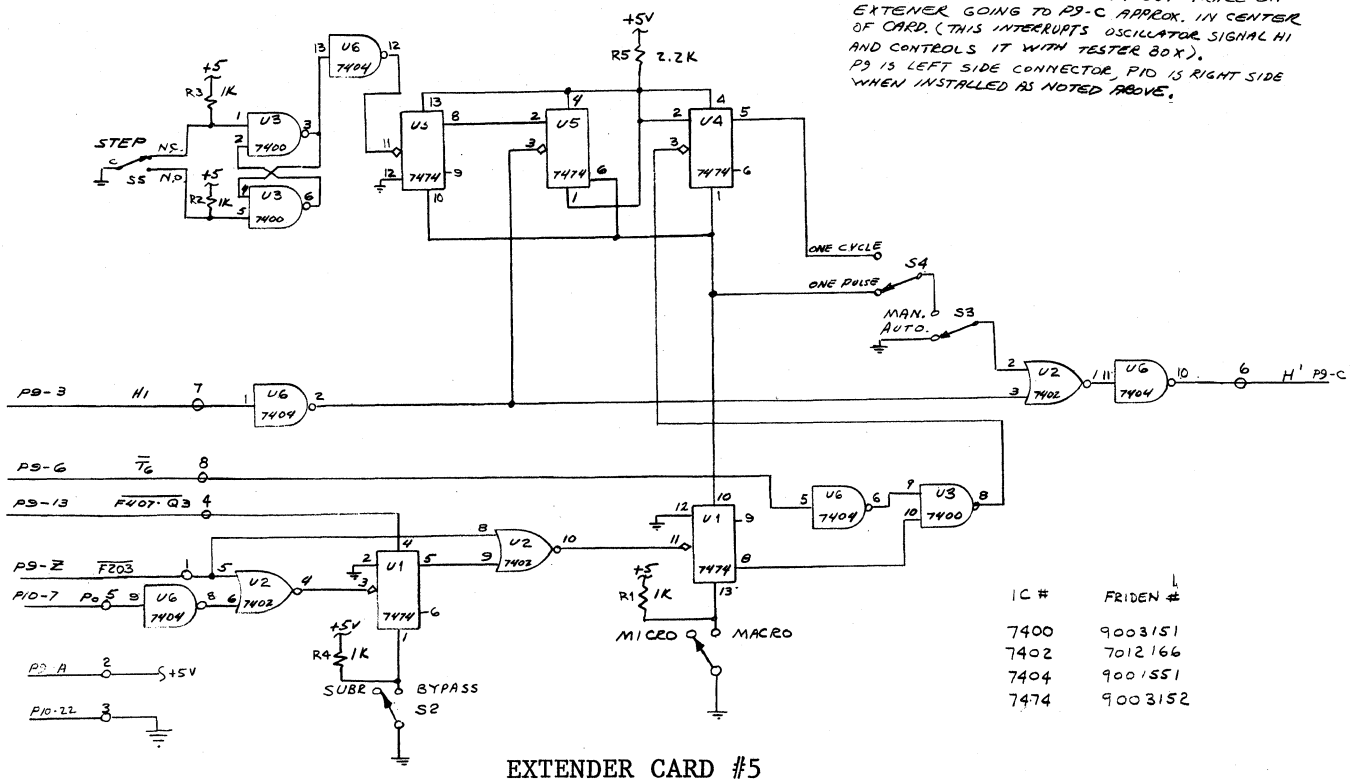
3-6.0 MOTHER BOARD WIRING LIST (Cont.)

SIGNAL NAME	CARD 1	CARD 2	CARD 3	CARD 4	CARD 5	CARD 6
$\overline{\text{PLAY RECORD CLOCK}}$ (P15-21)		XP4-F				
PLAY DATA 1 (P15-23)	XP1-16					
PLAY DATA 2 (P15-25)	XP1-17					
PLAY DATA 3 (P15-22)	XP1-18					
PLAY DATA 4 (P15-9)	XP1-19					
PLAY DATA 5 (P15-8)	XP1-20					
PLAY DATA 6 (P15-24)	XP2-2					
$\overline{\text{POWER UP}}$	XP2-V	XP4-18			XP10-18	
$\overline{\text{PROG BUSS}}$ (P13-3)				XP8-Y		
QØ					XP9-17	XP11-u
Q1					XP10-V	XP12-18
Q2					XP10-u	XP12-17
Q3					XP10-W	XP12-W
$\overline{\text{Q7}}$					XP10-X	XP12-20
RADIANS LED (P13-H)				XP8-16		
$\overline{\text{READER BUSY}}$ (P16-7)		XP4-D				
$\overline{\text{RECORD}}$ (P16-11)		XP4-E				
RECORD DATA 1 (P16-12)	XP2-6					
RECORD DATA 2 (P16-10)	XP2-7					
RECORD DATA 3 (P16-20)	XP2-10					
RECORD DATA 4 (P16-6)	XP2-13					
RECORD DATA 5 (P16-5)	XP2-15					
REOCRD DATA 6 (P16-19)	XP2-16					
$\overline{\text{RESET}}$		XP4-H			XP10-H	
$\overline{\text{RST 227}}$		XP3-W			XP9-18	
$\overline{\text{RESET MARKER CTR}}$	XP2-W	XP4-19				
$\overline{\text{SAMPLE}}$			XP6-K		XP10-9	
$\overline{\text{SEND}}$ (P17-5)			XP6-14			
$\overline{\text{RESET KEY IN}}$ (P13-10)					XP10-1	
$\overline{\text{SET Y5}}$		XP4-N		XP8-12		
START LED (P13-N)				XP8-9		
$\overline{\text{STOP}}$ (P13-15)				XP7-V		
STORE IN CARD LED (P13-C)		XP4-11				
$\overline{\text{RESET KEY}}$ (P13-S)					XP10-15	

3-6.0 MOTHER BOARD WIRING LIST (Cont.)

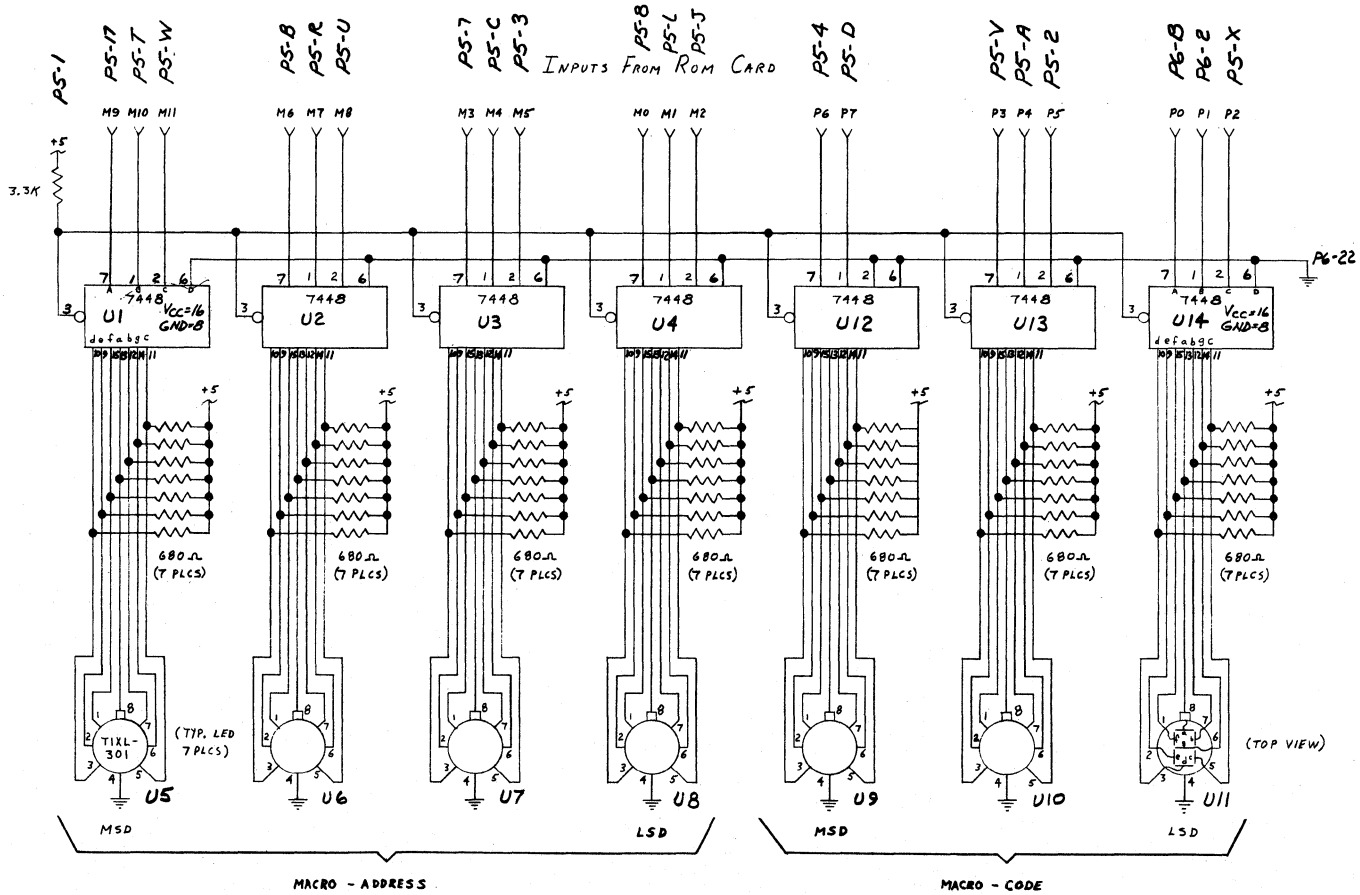
SIGNAL NAME	CARD 1	CARD 2	CARD 3	CARD 4	CARD 5	CARD 6
STROBE			XP5-22		XP9-Y	
$\overline{S12}$					XP10-F	XP12-6
TØ + T4	XP2-X	XP4-20			XP10-19	
$\overline{T1}$	XP2-21				XP10-Y	
T2 + T7	XP2-T	XP4-16			XP10-16	
$\overline{T2}$		XP4-5			XP10-3	
$\overline{T3}$	XP2-20	XP4-X			XP10-20	
$\overline{T6}$	XP1-6			XP7-F	XP9-6	
$\overline{T8}$	XP2-17	XP4-u			XP10-17	
T100	XP2-9	XP4-K				
T400	XP2-C	XP4-3		XP8-3		
$\overline{T400}$	XP2-8	XP4-J				
T1600	XP2-11			XP8-M		
WRITE LED (P13-D)		XP4-1				
Y5		XP4-7		XP8-7		
$\overline{Y7}$		XP4-6		XP8-C		
Z1	XP1-Y	XP3-21		XP7-21		
Z2	XP1-L	XP3-10		XP7-L		
Z3	XP1-M	XP3-11		XP7-11		
Z4	XP1-5			XP7-E		
Z5	XP1-E			XP7-5		
$\overline{Z6}$	XP1-7			XP7-7		
+5V (P13-F)	XP1-A	XP3-A	XP5-A1	XP7-A	XP9-A	XP11-A
-5V	XP2-3					
-9V						XP12-1
-12V	XP2-A		XP6-1		XP10-A	
GND	XP2-Z	XP4-Z	XP6-Z	XP8-Z	XP10-Z	XP12-Z
GND	XP2-22	XP4-22	XP6-22	XP8-22	XP10-22	XP12-22
PU GND (P14-3)						XP12-Y

NOTE:
P9 & P10 NUMBERS REFER TO EXTENDER CARD USED WITH CARD 5 FOR THIS TESTER. INSTALL EXTENDER WITH CONNECTORS IN FRONT. CUT TRACE ON EXTENER GOING TO P9-C APPROX. IN CENTER OF CARD. (THIS INTERRUPTS OSCILLATOR SIGNAL HI AND CONTROLS IT WITH TESTER BOX).
P9 IS LEFT SIDE CONNECTOR, P10 IS RIGHT SIDE WHEN INSTALLED AS NOTED ABOVE.



IC #	FRIDEN #
7400	9003151
7402	7012166
7404	9001551
7474	9003152

EXTENDER CARD #5



ROM READOUT EXTENDER CARD #3

3-7.0 1155 ONE STEP SERVICE TOOL

The 1155 One Step Service Tool provides a means for manually stepping the machine through several modes of clock steps (One T time, 9 T times, or One Macro Instruction) depending on the position of the selector switches on the One Step Control Box.

The tool consists of a One Step Control Box connected to an extender card (Tool Number T19153) for the #5 Board, and an extender card containing LED's (Tool Number T-19154) for the #3 Board. In operation, the One Step Control Box extender card is installed in the #5 position and the #5 Board installed in the extender card. The LED extender board is installed in the #3 position so the LED's are on the right hand side. The #3 Board is then installed in the extender with its component side facing forward (normal orientation).

CAUTION

When this tool is in use and the One Step Box is in the Manual Mode, the power supplies are heavily loaded due to the +5V current used for the LED's, and also due to the fact that the ROM's are not being strobed, thereby increasing the -12V current. Discretion should be used for the amount of time spent in this mode of operation.

3-7.1 OPERATING INSTRUCTIONS

Manual/Auto switch right, machine runs normally.

Manual/Auto switch left, machine runs in one of the following modes:

1. Cycle/Pulse switch right, clock advances one "T" time with each step switch depression.
2. Cycle/Pulse switch left, clock advances 9 "T" times with each step switch depression. (From T6 to T6.)

   NOTE: Cycle/Pulse switch has to be left if Micro/Macro, or Subroutine Bypass switches are left.
3. Micro/Macro switch left, clock advances one macro instruction with each step switch depression.
4. Subroutine Bypass switch right and Micro/Macro switch left, clock advances one Macro instruction with each step switch depression as above, and will advance through the next macro instruction if the instruction is a subroutine. (It will bypass the subroutine.)

3-8.0 MAGNETIC CARD READER TROUBLESHOOTING GUIDE

MALFUNCTION	DETECTION	CAUSE	REMEDY
Motor will not start in RECORD.	Mag. Card will not travel.	1) No power.	1) Plug in calculator to 120 VAC. 2) Turn calculator "ON". 3) Plug Card Reader into calculator.
		2) No signal.	1) Redepress and release RESET and STORE ON CARD keys on calculator. 2) Reinsert Mag. Card far enough to operate SWITCH 1.
		3) No power.	1) Replace fuse F1 in -12V supply. 2) Repair -12V supply. 3) Repair +5V supply.
		4) No signal.	1) Adjust or replace SWITCH 1. 2) Repair motor driver circuit. 3) Replace gates 50, 51, 63, 66 as required. 4) Replace gates 27, 38, 64 as req'd.
		5) Drive systems.	1) Replace drive belt. 2) Tighten drive wheel set screws.
		6) Motor	1) Replace motor.
		7) Calculator	1) Repair calculator.
Motor will not start in PLAY.	Mag. Card will not travel.	1) No power.	1) Plug in calculator to 120 VAC. 2) Turn calculator "ON". 3) Plug Card Reader into calculator.
		2) No signal.	1) Redepress and release RESET and LOAD FROM CARD keys on calculator.

3-8.0 MAGNETIC CARD READER TROUBLESHOOTING GUIDE (Cont.)

MALFUNCTION	DETECTION	CAUSE	REMEDY
			2) Reinsert Mag. Card far enough to operate SWITCH 1.
		3) No power.	1) Replace fuse F1 in -12V supply. 2) Repair -12V supply. 3) Repair +5V supply.
		4) No signal.	1) Adjust or replace SWITCH 1. 2) Repair motor driver circuit. 3) Replace gates 50, 51, 64, 66 as required. 4) Replace gates 28, 63 as req'd.
		5) Drive systems.	1) Replace drive belt. 2) Tighten drive wheel set screws.
		6) Motor	1) Replace motor.
		7) Calculator	1) Repair calculator.
Will not RECORD	Mag. Card will travel, but nothing recorded.	1) Drive System	1) Readjust SWITCH 2.
Will not PLAY	Mag. Card will travel, but nothing played.	1) Drive System	1) Readjust SWITCH 2.

3-8.0 MAGNETIC CARD READER TROUBLESHOOTING GUIDE (Cont.)

MALFUNCTION	DETECTION	CAUSE	REMEDY
RECORD improperly	Mag. Card travels jerkily.	1) Drive System	1) Check for dirty card. 2) Check for loose belt. 3) Tighten driver roller spring. 4) Tighten lower drive spring. 5) Check edges and width of Mag. Card.
PLAY improperly	Mag. Card travels jerkily.	1) Drive System	1) Check for dirty card. 2) Check for loose belt. 3) Tighten drive roller spring. 4) Tighten lower drive spring. 5) Check edges and width of Mag. Card.

SECTION 4

REFERENCE

SECTION CONTENTS

4-1.0 MICRO PROGRAMS

1. All numbers are in octal.
2. The first column is a 3-digit octal number corresponding to N8, N7, N6/N5, N4, N3/N2, N1, N0, the location 000 to 777 in the two micro-roms.
3. The second column corresponds to Q7, Q6/Q5, Q4, Q3/Q2, Q1, Q0, the micro-rom output code 000 to 377.
4. The third column is the name of the micro instruction corresponding to the micro rom output code.
5. For some micro instructions, two quantities appear in parenthesis (e.g. (Y)(17)). The first parenthesis refers to the RAM register being addressed. The second parenthesis refers to the digit within the register.

HALT 000

0	56	GO TO 270
270	202	SKIP ON D=1
271	056	GO TO 270
272	223	GATE 3
273	224	GATE 4
274	225	GATE 5
275	222	GATE 2
276	203	DECODE

RETURN 001

040	224	GATE 4
041	225	GATE 5
042	222	GATE 2
043	044	GO TO 220
220	204	DELTA PGM CTR
221	203	DECODE

NO-OP 002

100	044	GO TO 220
220	204	DELTA PGM CTR
221	203	DECODE

OUTPUT 003

140	220	SKIP ON F=1
141	030	GO TO 140
142	260	LOAD B FM (0)(0)
143	300	LOAD A FM (3)(0)
144	210	OUTPUT ONE BYTE
145	044	GO TO 220
220	204	DELTA PGM CTR
221	203	DECODE

4-1.0 MICRO PROGRAMS (Cont.)

SKIP 004-007

SKIP tests the state of Y4, Y5, Y6 or Y7. If the Y being tested is true then a Really Skip is done starting at 300. Otherwise a NO-OP is done starting at 100.

REALLY SKIP

300	204	DELTA PGM CTR
301	204	DELTA PGM CTR
302	044	GO TO 220
220	204	DELTA PGM CTR
221	203	DECODE

NO-OP

100	044	GO TO 220
220	204	DELTA PGM CTR
221	203	DECODE

GO SUB 010-017

001	026	GO TO 130
130	221	GATE 1
131	225	GATE 5
132	222	GATE 2
133	237	~~0->M4 THROUGH M11~~ CLR MACRO ROM ADDR CTR M4-M11
134	203	DECODE

RT SH 020-027

002	045	GO TO 224
224	301	LOAD A FM (Y)(1)
225	320	STORE SUM IN (Y)(0)
226	302	LOAD A FM (Y)(2)
227	303	STORE SUM IN (Y)(1)
.	.	
261	336	STORE SUM IN (Y)(16)
262	200	SET C=0, CLR A & B
263	337	STORE SUM IN (Y)(17)
264	044	GO TO 220
220	204	DELTA PROG CTR INCREMENT MACRO ROM ADD CTR
221	203	DECODE

4-1.0 MICRO PROGRAMS (Cont.)

LF SH 030-037

003	114	GO TO 460
460	316	LOAD A FM (Y)(16)
461	337	STORE SUM IN (Y)(17)
462	315	LOAD A FM (Y)(15)
463	336	STORE SUM IN (Y)(16)
515	321	STORE SUM IN (Y)(1)
516	200	SET C=0, CLR A & B
517	320	STORE SUM IN (Y)(0)
520	044	GO TO 220
220	204	DELTA PGM CTR
221	203	DECODE

+ Δ 040-047

004	033	GO TO 154
154	205	SET C=1, CLR A & B
155	034	GO TO 160
160	300	LOAD A FM (Y)(0)
161	320	STORE SUM IN (Y)(0)
216	317	LOAD A FM (Y)(17)
217	337	STORE SUM IN (Y)(17)
220	204	DELTA PGM CTR
221	203	DECODE

- Δ 050-057

005	032	GO TO 150
150	206	SET B COMP, CLR A & B
151	034	GO TO 160
160	300	LOAD A FM (Y)(0)
161	320	STORE SUM IN (Y)(0)
216	317	LOAD A FM (Y)(17)
217	337	STORE SUM IN (Y)(17)
220	204	DELTA PGM CTR
221	203	DECODE

4-1.0 MICRO PROGRAMS (Cont.)

ADD 060-067

```
006     126     GO TO 530
530     260     LOAD B FM (0)(0)
531     300     LOAD A FM (Y)(0)
532     320     STORE SUM IN (Y)(0)


605     277     LOAD B FM (0)(17)
606     317     LOAD A FM (Y)(17)
607     337     STORE SUM IN (Y)(17)
610     044     GO TO 220
220     204     DELTA PGM CTR
221     203     DECODE
```

SUB 070-077

```
007     125     GO TO 524
524     205     SET C=1, CLR A & B
525     206     SET B COMP, CLR A & B
526     126     GO TO 530
530     260     LOAD B FM (0)(0)
531     300     LOAD A FM (Y)(0)
532     320     STORE SUM IN (Y)(0)


605     277     LOAD B FM (0)(17)
606     317     LOAD A FM (Y)(17)
607     337     STORE SUM IN (Y)(17)
610     044     GO TO 220
220     204     DELTA PGM CTR
221     203     DECODE
```

4-1.0 MICRO PROGRAMS (Cont.)

LOAD 100-137

010	143	GO TO 614
011	143	GO TO 614
012	143	GO TO 614
013	143	GO TO 614
614	227	SET 5-BIT-ADDRESS FLAG clk 4630
615	300	LOAD A FM (Y)(0)
616	240	STORE SUM IN (0)(0)
617	301	LOAD A FM (Y)(1)
620	241	STORE SUM IN (0)(1)
653	317	LOAD A FM (Y)(17)
654	257	STORE SUM IN (0)(17)
655	044	GO TO 220
220	204	DELTA PGM CTR
221	203	DECODE

STORE 140-177

014	154	GO TO 660
015	154	GO TO 660
016	154	GO TO 660
017	154	GO TO 660
660	227	SET 5-BIT-ADDRESS FLAG
661	260	LOAD B FM (0)(0)
662	320	STORE SUM IN(Y)(0)
663	261	LOAD B FM (0)(1)
664	321	STORE SUM IN (Y)(1)
717	277	LOAD B FM (0)(17)
720	337	STORE SUM IN (Y)(17)
721	044	GO TO 220
220	204	DELTA PGM CTR
221	203	DECODE

4-1.0 MICRO PROGRAMS (Cont.)

BRANCH ALL ≠ 0 200-217

```
020     072     GO TO 350
021     072     GO TO 350
350     206     SET B COMP, CLR A & B
351     300     LOAD A FM (Y)(0)
352     207     UPDATE CARRY
353     301     LOAD A FM (Y)(1)
354     207     UPDATE CARRY


407     317     LOAD A FM (Y)(17)
410     207     UPDATE CARRY
411     071     GO TO 344
```

BRANCH ALL=0 220-237

```
022     103     GO TO 414
023     103     GO TO 414
414     206     SET B COMP, CLR A & B
415     300     LOAD A FM (Y)(0)
416     207     UPDATE CARRY
417     301     LOAD A FM (Y)(1)
420     207     UPDATE CARRY


453     317     LOAD A FM (Y)(17)
454     207     UPDATE CARRY
455     070     GO TO 340
```

BRANCH MSD≠0 240-257

```
024     011     GO TO 044
025     011     GO TO 044
044     206     SET B COMP, CLR A & B
045     317     LOAD A FM (Y)(17)
046     207     UPDATE CARRY
047     071     GO TO 344
```

4-1.0 MICRO PROGRAMS (Cont.)

BRANCH	MSD=0	260-277

026	063	GO TO 314
027	063	GO TO 314
314	206	SET B COMP, CLR A & B
315	317	LOAD A FM (Y)(17)
316	207	UPDATE CARRY
317	070	GO TO 340

BRANCH	LSD≠0	300-317

030	065	GO TO 324
031	065	GO TO 324
324	206	SET B COMP, CLR A & B
325	300	LOAD A FM (Y)(0)
326	207	UPDATE CARRY
327	071	GO TO 344

BRANCH	LSD=0	320-337

032	064	GO TO 320
033	064	GO TO 320
320	206	SET B COMP, CLR A & B
321	300	LOAD A FM (Y)(0)
322	207	UPDATE CARRY
323	070	GO TO 340

4-1.0 MICRO PROGRAMS (Cont.)

BRANCH IF ALL, MSD, OR LSD = 0

```
340    201    SKIP ON C=1
341    066    GO TO 330 (REALLY BRANCH)
342    067    GO TO 334 (CONTINUE)
```

BRANCH IF ALL, MSD, OR LSD ≠ 0

```
344    201    SKIP ON C=1
345    067    GO TO 334  (CONTINUE)
346    066    GO TO 330  (REALLY BRANCH)
```

REALLY BRANCH

```
330    226    GATE 6
331    204    DELTA PGM CTR
332    225    GATE 5
333    062    GO TO 310
310    226    GATE 6
311    222    GATE 2
312    203    DECODE
```

CONTINUE

```
334    204    DELTA PGM CTR
335    204    DELTA PGM CTR
336    203    DECODE
```

4-1.0 MICRO PROGRAMS (Cont.)

GO TO 340-357

```
034     061     GO TO 304
035     061     GO TO 304
304     224     GATE 4
305     204     DELTA PGM CTR
306     200     SET C=0, CLR A & B
307     200     SET C=0, CLR A & B
310     226     GATE 6
311     222     GATE 2
312     203     DECODE
```

LOAD 2 DIGITS 360-367

```
036     021     GO TO 104
104     204     DELTA PGM CTR
105     340     STORE ROM LSD IN (Y)(0)
106     361     STORE ROM MSD IN (Y)(1)
107     200     SET C=0, CLR A & B
110     322     STORE SUM IN (Y)(2)
111     323     STORE SUM IN (Y)(3)
 .       .
 .       .
125     337     STORE SUM IN (Y)(17)
126     044     GO TO 220
220     204     DELTA PGM CTR
221     203     DECODE
```

LOAD 16 DIGITS 370-377

```
037     012     GO TO 050
050     204     DELTA PGM CTR
051     356     STORE ROM LSD IN (Y)(16)
052     377     STORE ROM MSD IN (Y)(17)
053     204     DELTA PGM CTR
054     354     STORE ROM LSD IN (Y)(14)
055     375     STORE ROM MSD IN (Y)(15)
 .       .
 .       .
075     204     DELTA PGM CTR
076     340     STORE ROM LSD IN (Y)(0)
077     361     STORE ROM MSD IN (Y)(1)
100     044     GO TO 220
220     204     DELTA PGM CTR
221     203     DECODE
```

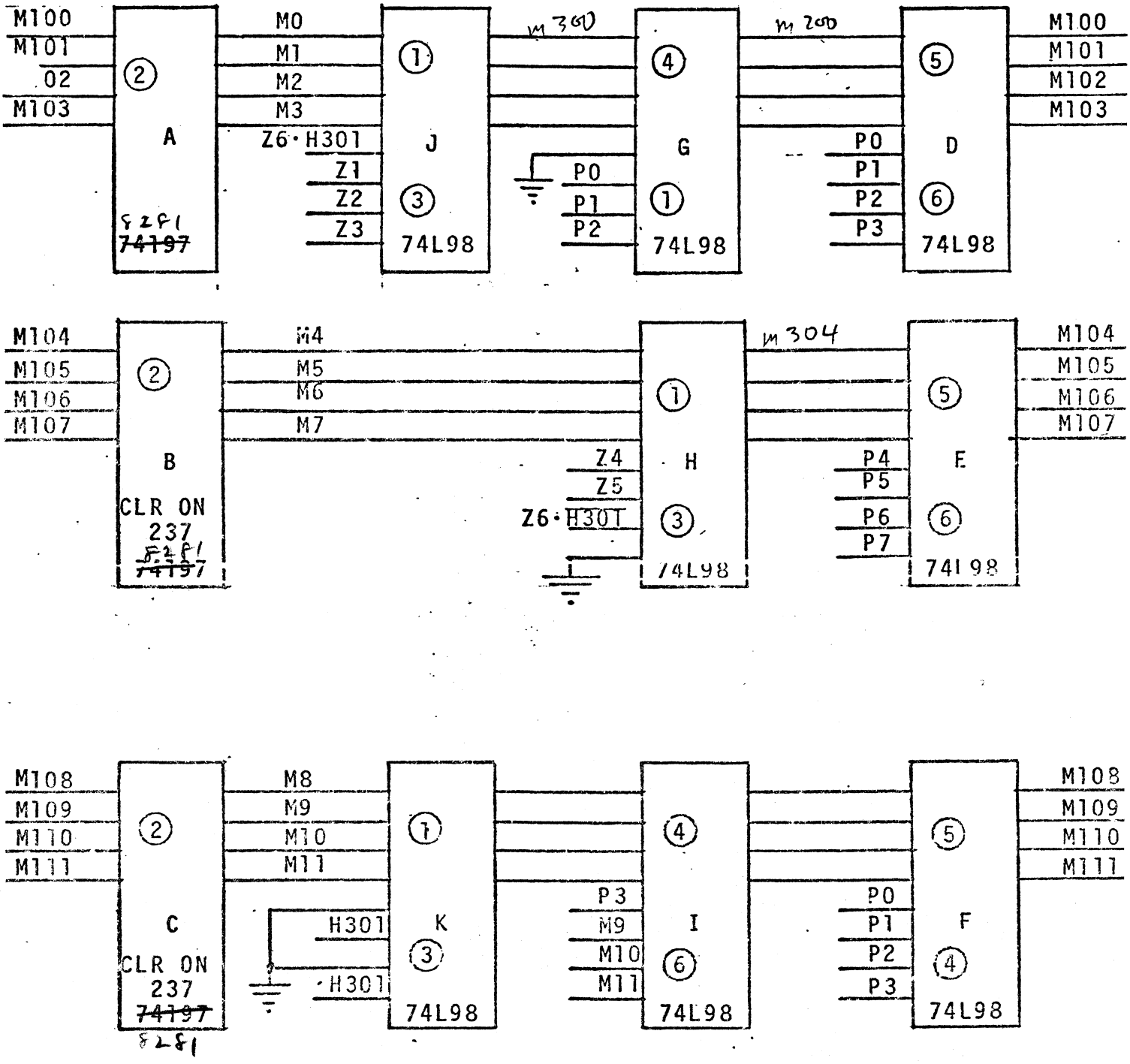
4-1.0 MICRO PROGRAMS (Cont.)

4-1.1 FUNCTION DESCRIPTIONS

F100 - ENABLES F20n FUNCTION GROUP
F101 - ENABLES F30n & F40n FUNCTION GROUPS
F102 - ENABLES CARRY LATCH IN ADDITION & ADDRESSES & WRITES IN RAM
F103 - LOADS CHARACTER REGISTER 'B' & ADDRESSES RAM
F104 - LOADS CHARACTER REGISTER 'A'
F105 - ENABLES CARRY LATCH & WRITES IN RAM
F106 - WRITES IN RAM & SELECTS RAM DATA
F107 - SELECTS RAM DATA & WRITES IN RAM
F200 - TERMINATES ARITHMETIC (CLEARS CARRY, ETC.)
F201 - ADJUSTS Q-ROM ADDRESS SEQUENCE FOR CARRY
F202 - ADJUSTS Q-ROM ADDRESS SEQUENCE FOR D (KB ENTRY)
F203 - TERMINATES ARITHMETIC & LOADS U-ADDRESS REGISTER & N-CNTR.
F204 - CLOCKS ADDRESS REGISTER FOR P-ROM
F205 - PRESETS CARRY & CLEARS CHAR. REGISTER
F206 - PRESETS E-LATCH & CLEARS CHAR. REGISTER
F207 - ENABLES CARRY LATCH
F300 - (UNUSED)
F301 - USED TO SELECT KB ENTRY AS P-ROM ADDRESS OR PREVIOUS ADDRESS
F302 - (UNUSED)
F303 - (UNUSED)
F304 - USED TO SELECT PRVIOUS ADDRESS AS P-ROM ADR. OR INSTRUCTED ADDRESS
F305 - USED TO SELECT PREVIOUS ADDRESS AS P-ROM ADR. OR INSTRUCTED ADDRESS
F306 - (UNUSED)
F307 - (UNUSED)
F400 - ADJUSTS Q-ROM ADDRESS FOR PRINT CYCLE OPERATION
F401 - USED IN CLOCKING ADDRESS REGISTERS FOR P-ROM
F402 - LOADS ADDRESS REGISTER/CNTR. FOR P-ROM
F403 - USED IN CLOCKING ADDRESS REGISTERS FOR P-ROM & RESETS ENTRY LATCHES
F404 - USED IN CLOCKING ADDRESS REGISTERS FOR P-ROM & RESETS ENTRY LATCHES
F405 - CLEARS M-CNTR. (ADR. REG. FOR P-ROM) & USED IN CLOCKING ADR.'S
F406 - USED IN CLOCKING ADR. REGISTERS FOR P-ROM
F407 - USED AS CLOCK FOR U-ADDRESS REGISTER FOR RAM

4-1.0 MICRO PROGRAMS (Cont.)

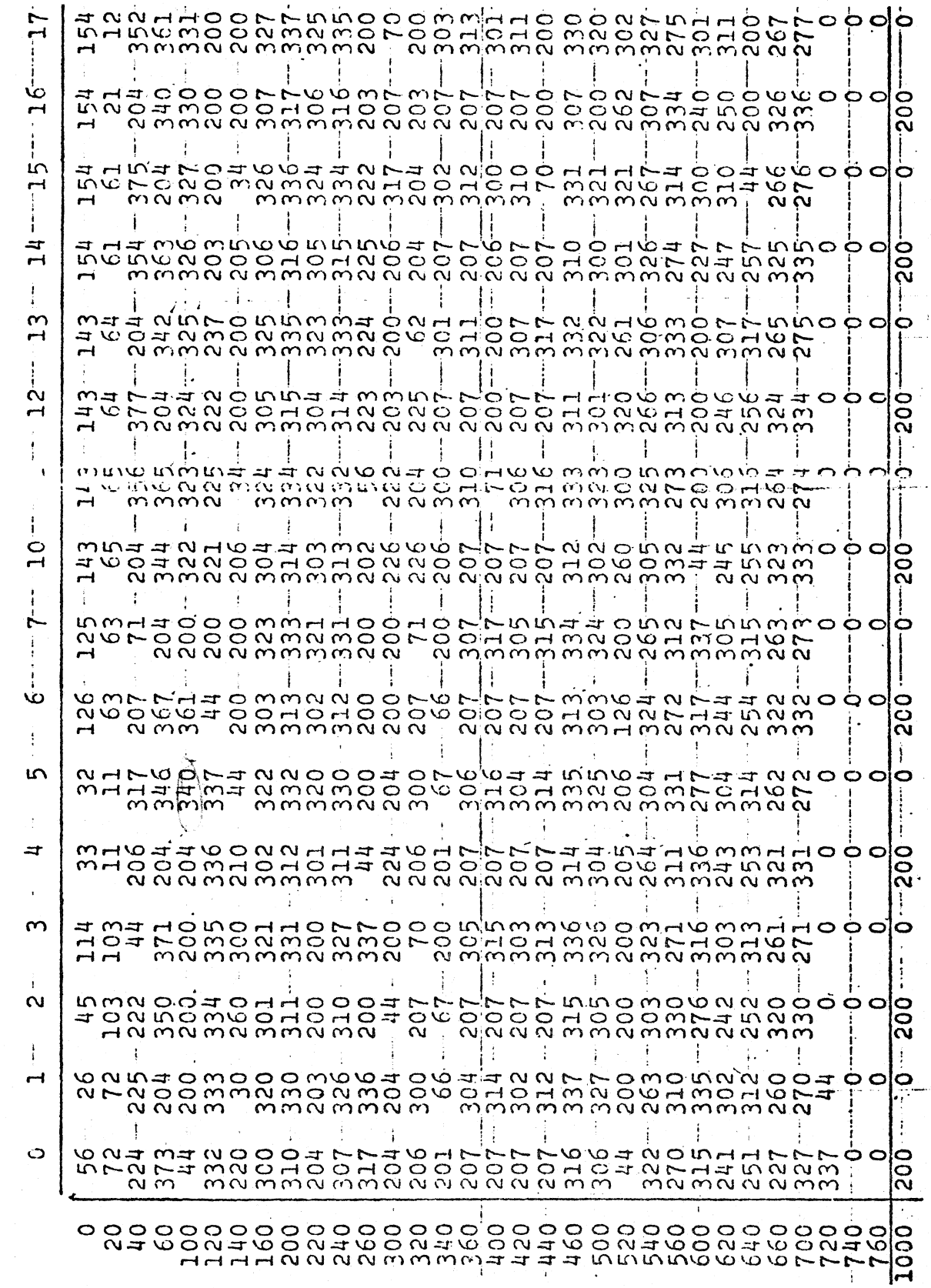
4-1.2 MAIN PROGRAM COUNTER CONTROLS



① ③ = $\overline{F301}$·L24
② = $\overline{F402}$
④ ⑥ = $\overline{F304}$·L26
④ ① = $\overline{F304}$·L29
⑤ ⑥ = F305·L31
⑤ ④ = $\overline{F305}$·L32

4-1.0 MICRO PROGRAMS (Cont.)

4-1.3 MICRO ROMS A & B



4-1.0 MICRO PROGRAMS (Cont.)

4-1.4 MICRO ROM LISTING WITH DESCRIPTION

ADDRESS	INSTRUCTION		MACRO-ROM INSTRUCTION
x 0	56 GOTO 270	HALT(Get next keyboard code)	000
x 1	26 GOTO 130	GOSUB	010-017
x 2	45 GOTO 224	SHIFT RIGHT	020-027
x 3	114 GOTO 460	SHIFT LEFT	030-037
x 4	33 GOTO 154	+	040-047
x 5	32 GOTO 150	-	050-057
x 6	126 GOTO 530	ADD	050-067
x 7	125 GOTO 524	SUB	070-077
x 10	143 GOTO 614	LOAD	110-107
x 11	143 GOTO 614	"	110-117
x 12	143 GOTO 614	"	120-127
x 13	143 GOTO 614	"	130-137
x 14	154 GOTO 660	STORE	140-147
x 15	154 GOTO 660	"	150-157
x 16	154 GOTO 660	"	160-167
x 17	154 GOTO 660	"	170-177
x 20	72 GOTO 350	BRANCH ON ENTIRE ≠ 0	200-207
x 21	72 GOTO 350	" " ≠ 0	210-217
x 22	103 GOTO 414	" " = 0	220-227
x 23	103 GOTO 414	" " = 0	230-237
x 24	11 GOTO 44	" MSD ≠ 0	240-247
x 25	11 GOTO 44	" " ≠ 0	250-257
x 26	63 GOTO 314	" " = 0	260-267
x 27	63 GOTO 314	" " = 0	270-277
x 30	65 GOTO 324	" LSD ≠ 0	300-307
x 31	65 GOTO 324	" " ≠ 0	310-317
x 32	64 GOTO 320	" " = 0	320-327
x 33	64 GOTO 320	" " = 0	330-337
x 34	61 GOTO 304	BRANCH	340-347
x 35	61 GOTO 304	BRANCH	350-357
x 36	21 GOTO 104	LOAD 2 DIGITS	360-367
x 37	12 GOTO 50	LOAD 16 DIGITS	370-377

4-1.4 MICRO ROM LISTING WITH DESC. (Cont.)

	ADDRESS	INSTRUCTION			MACRO-ROM INSTRUCTION
x	40	224	COUNTER GATE 4	RETURN	001
	41	225	COUNTER GATE 5		
	42	222	COUNTER GATE 2		
	43	44	GOTO 220		
	-44	206	SET B-COMP TO ON, CLEAR A & B		
	45	317	LOAD A FROM Y17		
	46	207	UPDATE CARRY		
	47	71	GOTO 344	C=1 FOR MSD≠0 (REALLY BRANCH)	
	-50	204	DELTA PROG COUNTER		
	51	356	STORE ROM LSD IN Y16		
	52	377	STORE ROM MSD IN Y17		
	53	204	DELTA PROG COUNTER		
	54	354	STORE ROM LSD IN Y14		
	55	375	STORE ROM MSD IN Y15		
	56	204	DELTA PROG COUNTER		
	57	352	STORE ROM LSD IN Y12		
	60	373	STORE ROM MSD IN Y13		
	61	204	DELTA PROG COUNTER		
	62	350	STORE ROM LSD IN Y10		
	63	371	STORE ROM MSD IN Y11		
	64	204	DELTA PROG COUNTER		
	65	346	STORE ROM LSD IN Y 6		
	66	367	STORE ROM MSD IN Y 7		
	67	204	DELTA PROG COUNTER		
	70	344	STORE ROM LSD IN Y 4		
	71	365	STORE ROM MSD IN Y 5		
	72	204	DELTA PROG COUNTER		
	73	342	STORE ROM LSD IN Y 2		
	74	363	STORE ROM MSD IN Y 3		
	75	204	DELTA PROG COUNTER		
	76	340	STORE ROM LSD IN Y 0		
	77	361	STORE ROM MSD IN Y 1		

4-1.4 MICRO ROM LISTING WITH DESCRIPTION (Cont)

ADDRESS	INSTRUCTION		MACRO-ROM INSTRUCTION
x 100	44	GOTO 220 NO OP	002
101	200	SET C=0, CLEAR A & B	
102	200	SET C=0, CLEAR A & B	
103	200	SET C=0, CLEAR A & B	
-104	204	DELTA PROG COUNTER	
105	340	STORE ROM LSD IN Y 0	
106	361	STORE ROM MSD IN Y 1	
107	200	SET C=0, CLEAR A & B	
110	322	STORE SUM IN Y 2	
111	323	STORE SUM IN Y 3	
112	324	STORE SUM IN Y 4	
113	325	STORE SUM IN Y 5	
114	326	STORE SUM IN Y 6	
115	327	STORE SUM IN Y 7	
116	330	STORE SUM IN Y10	
117	331	STORE SUM IN Y11	
120	332	STORE SUM IN Y12	
121	333	STORE SUM IN Y13	
122	334	STORE SUM IN Y14	
123	335	STORE SUM IN Y15	
124	336	STORE SUM IN Y16	
125	337	STORE SUM IN Y17	
126	44	GOTO 220	
127	200	SET C=0, CLEAR A & B	
-130	221	COUNTER GATE 1	
131	225	COUNTER GATE 5	
132	222	COUNTER GATE 2	
133	237	CLEAR M4 - M11 TO ZERO	
134	203	DECODE NEW INSTRUCTION	
135	200	SET C=0, CLEAR A & B	
136	200	SET C=0, CLEAR A & B	
137	200	SET C=0, CLEAR A & B	

4-1.4 MICRO ROM LISTING WITH DESC. (Cont.)

ADDRESS	INSTRUCTION		MACRO-ROM INSTRUCTION
x 140	220	SKIP NEXT INSTR: ON F=1 OUTPUT	003
141	30	GOTO 140	
142	260	LOAD B FROM 0 0	
143	300	LOAD A FROM Y 0	
144	210	OUTPUT ONE BYTE	
145	44	GOTO 220	
146	200	SET C=0, CLEAR A & B	
147	200	SET C=0, CLEAR A & B	
150	206	B-COMP TO ON, CLEAR A & B	
151	34	GOTO 160	
152	200	SET C=0, CLEAR A & B	
153	200	SET C=0, CLEAR A & B	
154	205	SET C=1, CLEAR A & B	
155	34	GOTO 160	
156	200	SET C=0, CLEAR A & B	
157	200	SET C=0, CLEAR A & B	
160	300	LOAD A FROM Y 0	
161	320	STORE SUM IN Y 0	
162	301	LOAD A FROM Y 1	
163	321	STORE SUM IN Y 1	
164	302	LOAD A FROM Y 2	
165	322	STORE SUM IN Y 2	
166	303	LOAD A FROM Y 3	
167	323	STORE SUM IN Y 3	
170	304	LOAD A FROM Y 4	
171	324	STORE SUM IN Y 4	
172	305	LOAD A FROM Y 5	
173	325	STORE SUM IN Y 5	
174	306	LOAD A FROM Y 6	
175	326	STORE SUM IN Y 6	
176	307	LOAD A FROM Y 7	
177	327	STORE SUM IN Y 7	

4-1.4 MICRO ROM LISTING WITH DESC. (Cont.)

ADDRESS	INSTRUCTION		MACRO-ROM INSTRUCTION
200	310	LOAD A FROM Y10	
201	330	STORE SUM IN Y10	
202	311	LOAD A FROM Y11	
203	331	STORE SUM IN Y11	
204	312	LOAD A FROM Y12	
205	332	STORE SUM IN Y12	
206	313	LOAD A FROM Y13	
207	333	STORE SUM IN Y13	
210	314	LOAD A FROM Y14	
211	334	STORE SUM IN Y14	
212	315	LOAD A FROM Y15	
213	335	STORE SUM IN Y15	
214	316	LOAD A FROM Y16	
215	336	STORE SUM IN Y16	
216	317	LOAD A FROM Y17	
217	337	STORE SUM IN Y17	
220	204	DELTA PROG COUNTER	
221	203	DECODE NEW INSTRUCTION	
222	200	SET C=0, CLEAR A & B	
223	200	SET C=0, CLEAR A & B	
224	301	LOAD A FROM Y 1	
225	320	STORE SUM IN Y 0	
226	302	LOAD A FROM Y 2	
227	321	STORE SUM IN Y 1	
230	303	LOAD A FROM Y 3	
231	322	STORE SUM IN Y 2	
232	304	LOAD A FROM Y 4	
233	323	STORE SUM IN Y 3	
234	305	LOAD A FROM Y 5	
235	324	STORE SUM IN Y 4	
236	306	LOAD A FROM Y 6	
237	325	STORE SUM IN Y 5	
240	307	LOAD A FROM Y 7	
241	326	STORE SUM IN Y 6	

4-1.4 MICRO ROM LISTING WITH DESC. (Cont.)

ODRESS	INSTRUCTION		MACRO-ROM INSTRUCTION
242	310	LOAD A FROM Y10	
243	327	STORE SUM IN Y 7	
244	311	LOAD A FROM Y11	
245	330	STORE SUM IN Y10	
246	312	LOAD A FROM Y12	
247	331	STORE SUM IN Y11	
250	313	LOAD A FROM Y13	
251	332	STORE SUM IN Y12	
252	314	LOAD A FROM Y14	
253	333	STORE SUM IN Y13	
254	315	LOAD A FROM Y15	
255	334	STORE SUM IN Y14	
256	316	LOAD A FROM Y16	
257	335	STORE SUM IN Y15	
260	317	LOAD A FROM Y17	
261	336	STORE SUM IN Y16	
262	200	SET C=0, CLEAR A & B	
263	337	STORE SUM IN Y17	
264	44	GOTO 220	
265	200	SET C=0, CLEAR A & B	
266	200	SET C=0, CLEAR A & B	
267	200	SET C=0, CLEAR A & B	
270	202	SKIP NEXT INSTR. ON D=1	
271	56	GOTO 270	
272	223	COUNTER GATE 3	
273	224	COUNTER GATE 4	
274	225	COUNTER GATE 5	
275	222	COUNTER GATE 2	
276	203	DECODE NEW INSTRUCTION	
277	200	SET C=0, CLEAR A & B	
300	204	DELTA PROG COUNTER REALLY SKIP 2	{004, 005, 006, 007} IF CORRESPONDING Y
301	44	GOTO 220	
303	200	SET C=0, CLEAR A & B	

4-1.4 MICRO ROM LISTING WITH DESC. (Cont.)

ADDRESS	INSTRUCTION		MACRO-ROM INSTRUCTION
303	200	SET C=0, CLEAR A & B	
-304	224	COUNTER GATE 4	
305	204	DELTA PROG COUNTER	
306	200	SET C=0, CLEAR A & B	
307	200	SET C=0, CLEAR A & B	
-310	226	COUNTER GATE 6	
311	222	COUNTER GATE 2	
312	203	DECODE NEW INSTRUCTION	
313	200	SET C=0, CLEAR A & B	
-314	206	SET B-COMP TO ON, CLEAR A & B	
315	317	LOAD A FROM Y17	
316	207	UPDATE CARRY	
317	70	GOTO 340 c=1 FOR MSD≠0 (DON'T BRANCH)	
-320	206	SET B-COMP TO ON, CLEAR A & B	
321	300	LOAD A FROM Y 0	
322	207	UPDATE CARRY	
323	70	GOTO 340 C=1 FOR LSD≠0 (DON'T BRANCH)	
-324	206	SET B-COMP TO ON, CLEAR A & B	
325	300	LOAD A FROM Y 0	
326	207	UPDATE CARRY	
327	71	GOTO 344 C=1 FOR LSD≠0 (REALLY BRANCH)	
-330	226	COUNTER GATE 6 BRANCH	
331	204	DELTA PROG COUNTER	
332	225	COUNTER GATE 5	
333	62	GOTO 310	
-334	204	DELTA PROG COUNTER (DON'T BRANCH)	
335	204	DELTA PROG COUNTER	
336	203	DECODE NEW INSTRUCTION	
337	200	SET C=0, CLEAR A & B	
-340	201	SKIP NEXT INSTRUCTION ON C=1 (DON'T BRANCH IF C=1)	
341	66	GOTO 330 (BRANCH)	

4-1.4 MICRO ROM LISTING WITH DESC. (Cont.)

DDRESS	INSTRUCTION		MACRO-ROM INSTRUCTION
342	67	GOTO 334 (DON'T BRANCH)	
343	200	SET C=0, CLEAR A & B	
-344	201	SKIP NEXT INSTR. ON C=1 (REALLY BRANCH IF C=1)	
345	67	GOTO 334 (DON'T BRANCH)	
346	66	GOTO 330 (BRANCH)	
347	200	SET C=0, CLEAR A & B	
-350	206	SET B-COMP TO ON, CLEAR A & B	
351	300	LOAD A FROM Y 0	
352	207	UPDATE CARRY	
353	301	LOAD A FROM Y 1	
354	207	UPDATE CARRY	
355	302	LOAD A FROM Y 2	
356	207	UPDATE CARRY	
357	303	LOAD A FROM Y 3	
360	207	UPDATE CARRY	
361	304	LOAD A FROM Y 4	
362	207	UPDATE CARRY	
363	305	LOAD A FROM Y 5	
364	207	UPDATE CARRY	
365	306	LOAD A FROM Y 6	
366	207	UPDATE CARRY	
367	307	LOAD A FROM Y 7	
370	207	UPDATE CARRY	
371	310	LOAD A FROM Y10	
372	207	UPDATE CARRY	
373	311	LOAD A FROM Y11	
374	207	UPDATE CARRY	
375	312	LOAD A FROM Y12	
376	207	UPDATE CARRY	
377	313	LOAD A FROM Y13	
400	207	UPDATE CARRY	
401	314	LOAD A FROM Y14	

4-1.4 MICRO ROM LISTING WITH DESC. (Cont.)

ADDRESS	INSTRUCTION	MACRO-ROM INSTRUCTION
402	207 UPDATE CARRY	
403	315 LOAD A FROM Y15	
404	207 UPDATE CARRY	
405	316 LOAD A FROM Y16	
406	207 UPDATE CARRY	
407	317 LOAD A FROM Y17	
410	207 UPDATE CARRY	
411	71 GOTO 344 C=1 FOR ENTIRE≠0 (REALLY BRANCH)	
412	200 SET C=0, CLEAR A & B	
413	200 SET C=0, CLEAR A & B	
414	206 SET B-COMP TO ON, CLEAR A & B	
415	300 LOAD A FROM Y 0	
416	207 UPDATE CARRY	
417	301 LOAD A FROM Y 1	
420	207 UPDATE CARRY	
421	302 LOAD A FROM Y 2	
422	207 UPDATE CARRY	
423	303 LOAD A FROM Y 3	
424	207 UPDATE CARRY	
425	304 LOAD A FROM Y 4	
426	207 UPDATE CARRY	
427	305 LOAD A FROM Y 5	
430	207 UPDATE CARRY	
431	306 LOAD A FROM Y 6	
432	207 UPDATE CARRY	
433	307 LOAD A FROM Y 7	
434	207 UPDATE CARRY	
435	310 LOAD A FROM Y10	
436	207 UPDATE CARRY	
437	311 LOAD A FROM Y11	
440	207 UPDATE CARRY	
441	312 LOAD A FROM Y12	
442	207 UPDATE CARRY	

4-1.4 MICRO ROM LISTING WITH DESC. (Cont.)

ADDRESS	INSTRUCTION	MACRO-ROM INSTRUCTION
443	313	LOAD A FROM Y13
444	207	UPDATE CARRY
445	314	LOAD A FROM Y14
446	207	UPDATE CARRY
447	315	LOAD A FROM Y15
450	207	UPDATE CARRY
451	316	LOAD A FROM Y16
452	207	UPDATE CARRY
453	317	LOAD A FROM Y17
454	207	UPDATE CARRY
455	70	GOTO 340 C=1 FOR ENTIRE ≠0 (DON'T BRANCH)
456	200	SET C=0, CLEAR A & B
457	200	SET C=0, CLEAR A & B
460	316	LOAD A FROM Y16
461	337	STORE SUM IN Y17
462	315	LOAD A FROM Y15
463	336	STORE SUM IN Y16
464	314	LOAD A FROM Y14
465	335	STORE SUM IN Y15
466	313	LOAD A FROM Y13
467	334	STORE SUM IN Y14
470	312	LOAD A FROM Y12
471	333	STORE SUM IN Y13
472	311	LOAD A FROM Y11
473	332	STORE SUM IN Y12
474	310	LOAD A FROM Y10
475	331	STORE SUM IN Y11
476	307	LOAD A FROM Y 7
477	330	STORE SUM IN Y10
500	306	LOAD A FROM Y 6
501	327	STORE SUM IN Y 7
502	305	LOAD A FROM Y 5
503	326	STORE SUM IN Y 6

4-1.4 MICRO ROM LISTING WITH DESC. (Cont.)

ADDRESS	INSTRUCTION		MACRO-ROM INSTRUCTION
504	304	LOAD A FROM Y 4	
505	325	STORE SUM IN Y 5	
506	303	LOAD A FROM Y 3	
507	324	STORE SUM IN Y 4	
510	302	LOAD A FROM Y 2	
511	323	STORE SUM IN Y 3	
512	301	LOAD A FROM Y 1	
513	322	STORE SUM IN Y 2	
514	300	LOAD A FROM Y 0	
515	321	STORE SUM IN Y 1	
516	200	SET C=0, CLEAR A & B	
517	320	STORE SUM IN Y 0	
520	44	GOTO 220	
521	200	SET C=0, CLEAR A & B	
522	200	SET C=0, CLEAR A & B	
523	200	SET C=0, CLEAR A & B	
524	205	SET C=1, CLEAR A & B	
525	206	SET B-COMP TO ON, CLEAR A & B	
526	126	GOTO 530	
527	200	SET C=0, CLEAR A & B	
530	260	LOAD B FROM 0 0	
531	300	LOAD A FROM Y 0	
532	261	LOAD B FROM 0 1	
534	301	LOAD A FROM Y 1	
535	321	STORE SUM IN Y 1	
536	262	LOAD B FROM 0 2	
537	302	LOAD A FROM Y 2	
540	322	STORE SUM IN Y 2	
541	263	LOAD B FROM 0 3	
542	303	LOAD A FROM Y 3	
543	323	STORE SUM IN Y 3	
544	264	LOAD B FROM 0 4	
545	304	LOAD A FROM Y 4	
546	324	STORE SUM IN Y 4	

4-1.4 MICRO ROM LISTING WITH DESC. (Cont.)

ADDRESS	INSTRUCTION		MACRO-ROM INSTRUCTION
547	265	LOAD B FROM 0 5	
550	305	LOAD A FROM Y 5	
551	325	STORE SUM IN Y 5	
552	266	LOAD B FROM 0 6	
553	306	LOAD A FROM Y 6	
554	326	STORE SUM IN Y 6	
555	267	LOAD B FROM 0 7	
556	307	LOAD A FROM Y 7	
557	327	STORE SUM IN Y 7	
560	270	LOAD B FROM 010	
561	310	LOAD A FROM Y10	
562	330	STORE SUM IN Y10	
563	271	LOAD B FROM 011	
564	311	LOAD A FROM Y11	
565	331	STORE SUM IN Y11	
566	272	LOAD B FROM 012	
567	312	LOAD A FROM Y12	
570	332	STORE SUM IN Y12	
571	273	LOAD B FROM 013	
572	313	LOAD A FROM Y13	
573	333	STORE SUM IN Y13	
574	274	LOAD B FROM 014	
575	314	LOAD A FROM Y14	
576	334	STORE SUM IN Y14	
577	275	LOAD B FROM 015	
600	315	LOAD A FROM Y15	
601	335	STORE SUM IN Y15	
602	276	LOAD B FROM 016	
603	316	LOAD A FROM Y16	
604	336	STORE SUM IN Y16	
605	277	LOAD B FROM 017	
606	317	LOAD A FROM Y17	
607	337	STORE SUM IN Y17	
610	44	GOTO 220	

4-1.4 MICRO ROM LISTING WITH DESC. (Cont.)

ADDRESS	INSTRUCTION		MACRO-ROM INSTRUCTION
611	200	SET C=0, CLEAR A & B	
612	200	SET C=0, CLEAR A & B	
613	200	SET C=0, CLEAR A & B	
-614	227	SET 5-BIT FLAG TO ON	
615	300	LOAD A FROM Y 0	
616	240	STORE SUM IN 0 0	
617	301	LOAD A FROM Y 1	
620	241	STORE SUM IN 0 1	
621	302	LOAD A FROM Y 2	
622	242	STORE SUM IN 0 2	
623	303	LOAD A FROM Y 3	
624	243	STORE SUM IN 0 3	
625	304	LOAD A FROM Y 4	
626	244	STORE SUM IN 0 4	
627	305	LOAD A FROM Y 5	
630	245	STORE SUM IN 0 5	
631	306	LOAD A FROM Y 6	
632	246	STORE SUM IN 0 6	
633	307	LOAD A FROM Y 7	
634	247	STORE SUM IN 0 7	
635	310	LOAD A FROM Y10	
636	250	STORE SUM IN 010	
637	311	LOAD A FROM Y11	
640	251	STORE SUM IN 011	
641	312	LOAD A FROM Y12	
642	252	STORE SUM IN 012	
643	313	LOAD A FROM Y13	
644	253	STORE SUM IN 013	
645	314	LOAD A FROM Y14	
646	254	STORE SUM IN 014	
647	315	LOAD A FROM Y15	
650	255	STORE SUM IN 015	
651	316	LOAD A FROM Y16	
652	256	STORE SUM IN 016	

4-1.4 MICRO ROM LISTING WITH DESC. (Cont.)

ADDRESS	INSTRUCTION		MACRO-ROM INSTRUCTION
653	317	LOAD A FROM Y17	
654	257	STORE SUM IN 017	
655	44	GOTO 220	
656	200	SET C=0, CLEAR A & B	
657	200	SET C=0, CLEAR A & B	
660	227	SET 5-BIT FLAG TO ON	
661	260	LOAD B FROM 0 0	
662	320	STORE SUM IN Y 0	
663	261	LOAD B FROM 0 1	
664	321	STORE SUM IN Y1	
665	262	LOAD B FROM 0 2	
666	322	STORE SUM IN Y 2	
667	263	LOAD B FROM 0 3	
670	323	STORE SUM IN Y 3	
671	264	LOAD B FROM 0 4	
672	324	STORE SUM IN Y 4	
673	265	LOAD B FROM 0 5	
674	325	STORE SUM IN Y 5	
675	266	LOAD B FROM 0 6	
676	326	STORE SUM IN Y 6	
677	267	LOAD B FROM 0 7	
700	327	STORE SUM IN Y 7	
701	270	LOAD B FROM 010	
702	330	STORE SUM IN Y10	
703	271	LOAD B FROM 011	
704	331	STORE SUM IN Y11	
705	272	LOAD B FROM 012	
706	332	STORE SUM IN Y12	
707	273	LOAD B FROM 013	
710	333	STORE SUM IN Y13	
711	274	LOAD B FROM 014	
712	334	STORE SUM IN Y14	
713	275	LOAD B FROM 015	

4-1.4 MICRO ROM LISTING WITH DESC. (Cont.)

ADDRESS	INSTRUCTION		MACRO-ROM INSTRUCTION
714	335	STORE SUM IN Y15	
715	276	LOAD B FROM 016	
716	336	STORE SUM IN Y16	
717	277	LOAD B FROM 017	
720	337	STORE SUM IN Y17	
721	44	GOTO 220	
722	0	GOTO 0	

INSTRUCTION NAME	OCTAL FIRST WORD	BINARY FIRST WORD 76	543	210	SECOND WORD 76	543	210
HALT	000	00	000	000			
RETURN	001	00	000	001			
NO-OP	002	00	000	010			
OUTPUT	003	00	000	011			
SKIP-4 (DEG/RAD)	004	00	000	100			
SKIP-5 (RUN + LIST)	005	00	000	101			
SKIP-6 (1 STEP + PLOTTER)	006	00	000	110			
SKIP-7 (PROG. CODE SEARCH)	007	00	000	111			
GO-SUB	010 - 017	00	001	SSS			
RT-SH	020 - 027	00	010	AAA			
LF-SH	030 - 037	00	011	AAA			
+△	040 - 047	00	100	AAA			
-△	050 - 057	00	110	AAA			
ADD	060 - 067	00	110	AAA			
SUB	070 - 077	00	111	AAA			
LOAD	100 - 137	01	0AA	AAA			
STORE	140 - 177	01	1AA	AAA			
BRANCH ALL ≠ 0	200 - 217	10	00L	AAA	LL	LLL	LLL
BRANCH ALL = 0	220 - 237	10	01L	AAA	LL	LLL	LLL
BRANCH MSD ≠ 0	240 - 257	10	10L	AAA	LL	LLL	LLL
BRANCH MSD = 0	260 - 277	10	11L	AAA	LL	LLL	LLL
BRANCH LSD ≠ 0	300 - 317	11	00L	AAA	LL	LLL	LLL
BRANCH LSD = 0	320 - 337	11	01L	AAA	LL	LLL	LLL
GO-TO	340 - 357	11	10L	LLL	LL	LLL	LLL
INPUT-2-DIGITS	360 - 367	11	110	AAA	DD	DDD	DDD
INPUT-16-DIGITS	370 - 377	11	111	AAA	..NEXT 8 WORDS..		

S = SUB-ROUTINE NUMBER
A = RAM REGISTER ADDRESS
L = MACRO INSTRUCTION LOCATION
D = DATA

4-2.1 MACRO ROM ENTRY POINTS

	0	1	2	3	4	5	6	7	8	9
0	****	4000	6403	6453	6465	6566	****	6473	6500	6762
10	6505	6510	6541	6545	6603	6623	6774	6766	4303	6735
20	6440	352	733	740	747	750	306	331	342	535
30	560	1342	1770	1334	474	1107	1120	1137	1154	1164
40	1174	1324	1356	1370	1400	1407	1415	1434	1443	1502
50	3774	1776	1534	1541	1552	1564	1572	3770	1613	1625
60	1635	1663	1733	675	703	710	522	613	615	624
70	632	640	565	611	3663	2357	2002	2006	2014	2022
80	2045	2053	2061	2066	2074	2103	2116	2125	2132	2302
90	2311	2315	2332	2341	2774	2776	2420	2436	2447	2451
100	2456	225	2462	2465	2472	2503	2665	2714	2730	643
110	647	657	661	667	672	3456	3000	3014	3017	3024
120	3034	3044	3070	3100	3101	3104	3111	3764	3120	3143
130	3316	3334	3337	3342	3347	3355	3363	3367	3405	3415
140	3425	3431	3433	3444	3453	3766	3772	3503	3523	3541
150	3550	3561	3600	3602	3606	3627	3633	3651	3655	3672
160	3700	3674	3711	1000	1004	1006	1020	1042	1046	1766
180	4756	441	4754	4366	4336	4464	4356	361	230	237
190	4742	242	245	250	256	264	300	322	1772	1774
200	212	211	210	207	206	205	204	203	202	201
210	6760	502	452	432	215	221	2000	476	3776	4647
220	4776	4700	3576	2355	4412	4762	4510	4563	4530	4557
230	4546	4535	4770	1716	1560	752	4766	4600	4772	4630
240	4774	3706	3631	776	4750	4760	4744	3647	6776	4746
250	372	403	374	4121	4127	4752	4133	4141	4165	4154
260	4275	4167	4177	4304	4417	4434	4421	4210	4206	4227
270	4244	4263	4050	4062	2732	3721	1052	4001	1671	4706
280	1725	5562	6003	5526	5574	5617	5566	5536	5650	5611
290	5772	5321	5672	5135	5642	5324	5257	5322	6030	6133
300	6236	5323	5571	4543	1476	6000	5774	5721	5725	5733
310	5703	5366	5326	5704	5423	5776	5747	5557	6770	5751
320	5754	7016	7146	7123	7152	6772	5405	5631	6341	7075
330	7042	7033	7052	7070	4474	4764	6764	421	0	5000
340	6503	423	1056	1061	1346	1510	1512	2363	2365	3113
350	3462	3472	3501	3514	3611	4034	4042	4061	4067	4360
360	4364	4426	4477	4514	4566	4603	4623	4634	4660	5425
370	5525	5713	7213	6376	6417	6441	6606	6625	6725	4725
380	4710	320	7171	7261	7012	7161	7256	7301	7423	7446
390	7014	6600	7323	7327	7337	7376	7211	7450	7511	7520
400	5166	5202	5224	5216	5207	5232	5305	407	7002	7736
410	7740	7742	7744	7746	7750	7752	7754	7756	7760	7762
420	7764	7766	7770	7772	7774	7776	7430	7363	7410	7401

PROCESSING------16 UNITS

4-2.1 MACRO ROM ENTRY POINTS (Cont.)

7736,7777

409 7736 GOTO 387	Plot Entry Point (7301)
410 7740 GOTO 397	0
411 7742 GOTO 397	1
412 7744 GOTO 397	2
413 7746 GOTO 397	3
414 7750 GOTO 397	4
415 7752 GOTO 397	5
416 7754 GOTO 397	6
417 7756 GOTO 397	7
418 7760 GOTO 397	8
419 7762 GOTO 397	9
420 7764 GOTO 388	10 (Interrogate)
421 7766 GOTO 389	11 (Special Function)
422 7770 GOTO 389	12 (Quadrant III)
423 7772 GOTO 389	13 (Quadrant IV)
424 7774 GOTO 389	14 (Quadrant II)
425 7776 GOTO 389	15 (Quadrant I)

?

4-2.2 MACRO ROM ROUTINE ENTRY POINTS

	338	2	KEYBOARD
215	214	17	SINE/COS/TAN
225	101	26	MISC. KEY-FUNCTIONS
432	213	27	A↑X
452	212	16	1/X
476	217	28	LOG 10
502	211	13	SQUARE ROOT
535	29	7	PRINT SUBROUTINE
565	72	15	UNPACK SUBROUTINE
613	67	14	MULTIPLY SUBROUTINE
643	109	19	DIVIDE SUBROUTINE
675	63	12	SQUARE ROOT SUBROUTINE
733	22	4	KEY SUBROUTINE
752	235	32	PRINT START SUBROUTINE
776	243		
1000	163	24	PACK SUBROUTINE
1056	342	25	PACKOUT
1061	343	9	EXPONENTIAL
1346	344	10	RECTANGULAR TO POLAR
1502	49	11	ADD/SUBTRACT
1766	169		
2000	216	17	SINE/COS/TAN
2363	347	18	LOG E
2774	94		
3000	116	21	ARC SINE/COS/TAN
3462	350	22	MULTIPLY/DIVIDE
3611	354	23	FACTORIAL
3764	127		
4000	1	3	PRINT CONTROL
4477	362	30	PROGRAM STORE
4647	219	29	POLAR TO RECTANGULAR
4710	380	26	MISC. KEY FUNCTIONS
4744	246		
5000	339	1	LIST PRINT
5772	290		
6000	305	1	LIST PRINT
6376	373	2	KEYBOARD
6762	9		
7016	321	33	INDIRECT ADDRESS
7161	385	3	PRINT CONTROL
7301	387	5	DIGITAL OUTPUT
7736	409		

PROCESSING 5 UNITS

4-2.3 MACRO ROM LISTING WITH DESCRIPTION

	0	1	2	3	4	5	6	7
0	341	135	341	165	342	0	341	213
10	341	243	341	275	341	333	341	352
20	340	212	340	211	340	210	340	207
30	340	206	340	205	340	204	340	203
40	340	202	340	201	355	360	340	225
50	351	374	340	230	340	237	351	342
60	340	242	340	245	340	250	340	256
70	340	264	340	300	340	322	351	354
100	343	374	341	102	341	52	341	32
110	340	215	340	221	344	0	341	76
120	347	376	343	376	345	374	347	366
130	347	372	343	370	351	356	340	372
140	341	3	357	336	351	350	351	360
150	351	344	351	372	351	366	340	361
160	0	0	0	0	356	16	340	352
170	0	0	341	23	351	370	0	0
200	2	44	44	44	44	44	44	44
210	44	44	141	355	364	367	21	344
220	2	367	2	344	2	366	3	0
230	366	20	36	46	365	0	0	364
240	1	0	366	2	0	366	42	0
250	142	237	21	47	355	376	142	147
260	364	0	347	374	150	370	61	101
270	131	46	123	131	1	0	351	346
300	11	363	0	301	306	43	21	207
310	320	146	360	1	152	106	343	366
320	355	362	11	142	363	0	321	331
330	43	21	364	21	34	360	3	64
340	101	74	41	54	22	264	342	102
350	343	366	360	2	151	20	363	4
360	3	360	1	147	143	20	150	142
370	355	374	363	4	141	360	0	3
400	101	355	366	363	0	340	374	237
410	21	110	142	360	3	3	20	150
420	102	355	366	360	2	3	20	150
430	355	366	142	110	210	41	150	351
440	346	141	102	150	360	1	153	101
450	345	374	372	20	0	0	0	0
460	0	1	0	364	1	147	210	74
470	366	10	350	0	347	374	363	20
500	345	376	11	142	21	22	101	144
510	61	101	64	64	360	5	334	122
520	74	32	30	24	64	102	15	142
530	104	141	102	343	366	106	141	20
540	146	30	71	101	142	363	7	364
550	6	360	10	71	271	160	61	44
560	101	73	104	3	1	141	20	20
570	20	30	30	146	30	71	31	41
600	360	40	30	30	71	271	211	61

4-2.3 MACRO ROM LISTING WITH DESC. (Cont.)

610	51	106	1	362	20	32	272	215
620	62	101	361	0	332	232	61	52
630	341	224	232	240	21	22	341	224
640	71	101	1	362	20	341	257	71
650	271	267	252	272	61	31	32	271
660	247	71	271	267	42	341	261	42
670	341	247	32	102	1	142	22	360
700	20	143	33	33	50	210	303	141
710	72	103	61	101	72	272	310	62
720	103	71	101	62	23	32	213	310
730	30	30	1	333	340	360	0	1
740	215	350	337	347	142	341	350	101
750	55	1	360	1	143	3	360	4
760	3	3	1	2	2	2	2	2
770	2	2	2	2	2	2	341	7
1000	200	6	141	1	51	30	260	4
1010	20	362	120	62	262	20	22	41
1020	22	22	32	32	32	241	46	41
1030	360	40	30	71	261	52	61	323
1040	42	61	102	61	101	1	360	0
1050	141	1	366	7	350	0	12	351
1060	346	11	143	101	144	145	24	103
1070	141	370	2	60	45	205	11	51
1100	224	5	14	242	107	32	54	360
1110	20	30	146	40	40	74	264	334
1120	22	44	244	120	102	30	30	30
1130	20	147	20	20	72	360	23	50
1140	22	200	137	102	66	325	164	76
1150	76	56	360	20	30	260	154	77
1160	107	367	0	77	36	107	67	267
1170	174	46	37	27	107	141	13	20
1200	145	20	141	370	10	107	203	151
1210	131	203	221	200	61	105	13	370
1220	5	165	207	65	207	223	26	20
1230	61	101	144	143	105	141	370	0
1240	3	201	145	110	201	221	141	13
1250	370	1	41	211	44	27	100	207
1260	1	61	105	13	370	3	61	111
1270	224	204	165	66	66	61	107	13
1300	74	103	61	104	14	22	326	324
1310	102	141	370	3	26	42	167	146
1320	1	150	70	14	363	0	106	20
1330	141	102	343	366	325	342	360	0
1340	351	346	366	1	350	0	367	20
1350	11	20	143	321	356	47	21	101
1360	145	110	11	20	37	321	370	47
1370	146	21	101	144	105	71	251	7
1400	23	51	271	0	33	343	15	41
1410	26	251	7	105	144	106	141	103
1420	71	66	236	76	37	271	34	47
1430	101	361	0	71	106	14	145	141

4-2.3 MACRO ROM LISTING WITH DESC. (Cont.)

1440	13	360	20	30	270	43	61	21
1450	101	61	61	61	61	101	15	141
1460	106	13	30	142	104	141	102	12
1470	152	150	105	146	347	364	366	20
1500	350	0	104	74	66	101	46	0
1510	364	20	141	360	20	30	76	56
1520	236	102	101	11	147	234	134	51
1530	331	134	41	41	363	0	331	141
1540	43	101	20	145	110	11	331	152
1550	43	43	146	113	310	160	104	150
1560	101	20	144	75	27	275	172	45
1570	343	164	55	44	26	275	172	103
1600	50	250	213	50	50	270	213	107
1610	367	0	77	107	66	276	225	106
1620	366	0	76	53	53	253	333	53
1630	53	273	333	363	0	104	141	113
1640	144	106	12	334	263	141	110	142
1650	112	150	113	20	145	363	0	367
1660	0	355	374	5	343	271	6	355
1670	366	153	110	144	112	141	360	0
1700	150	40	152	3	143	360	4	3
1710	143	360	6	234	316	53	3	101
1720	51	231	325	351	352	360	2	3
1730	113	355	366	363	1	343	235	2
1740	2	2	2	2	2	2	2	2
1750	2	2	2	2	2	2	2	2
1760	2	2	2	2	2	2	342	56
1770	342	61	342	346	343	110	343	112
2000	367	60	324	6	346	0	27	11
2010	307	14	21	31	145	363	0	321
2020	22	43	21	101	144	105	141	370
2030	6	50	61	205	60	161	171	131
2040	4	344	53	360	66	30	260	45
2050	20	54	54	14	360	20	30	40
2060	74	22	44	244	61	32	32	54
2070	264	66	360	45	30	260	74	307
2100	103	47	62	22	102	62	57	262
2110	116	32	22	307	116	43	102	62
2120	262	132	327	125	43	102	30	20
2130	72	72	102	146	20	141	61	101
2140	13	144	145	370	6	43	127	204
2150	7	162	166	160	141	370	6	226
2160	171	31	127	30	46	121	64	104
2170	14	370	3	166	5	223	205	170
2200	44	1	141	370	0	142	161	71
2210	30	47	61	210	72	105	62	102
2220	14	370	64	40	131	130	3	210
2230	21	207	141	370	4	24	123	23
2240	170	222	210	226	62	105	20	62
2250	62	102	14	370	67	220	223	41
2260	2	170	40	164	72	102	141	106

4-2.3 MACRO ROM LISTING WITH DESC. (Cont.)

2270	13	30	327	332	57	327	311	67
2300	362	20	32	262	302	106	72	344
2310	132	101	146	226	357	36	42	266
2320	315	26	52	52	107	141	102	147
2330	106	14	144	53	53	263	341	43
2340	43	361	231	113	145	107	61	104
2350	12	325	355	347	370	351	346	366
2360	2	350	0	363	0	230	332	11
2370	21	145	146	372	3	26	42	167
2400	146	1	150	70	360	20	30	71
2410	271	20	43	41	101	361	0	71
2420	101	30	147	313	36	102	75	255
2430	62	360	5	67	345	72	105	72
2440	252	47	360	5	67	345	56	362
2450	20	32	272	51	105	72	102	145
2460	345	72	65	360	20	30	270	65
2470	20	75	106	66	105	141	76	333
2500	103	66	66	106	20	14	22	102
2510	146	20	141	13	145	362	0	371
2520	0	0	0	126	2	45	25	140
2530	374	0	22	27	171	163	20	204
2540	220	62	102	74	104	14	371	0
2550	0	10	126	123	123	165	11	374
2560	0	31	62	23	40	202	3	100
2570	105	62	102	74	104	14	371	0
2600	5	166	105	144	231	162	170	374
2610	0	125	62	21	62	5	123	60
2620	105	62	102	74	104	14	371	0
2630	11	210	146	20	63	41	225	374
2640	2	47	64	104	30	204	100	131
2650	105	62	102	74	104	14	141	106
2660	13	20	146	360	22	50	37	210
2670	265	106	67	103	20	310	314	371
2700	2	60	45	205	11	51	224	5
2710	107	13	30	147	113	145	361	20
2720	31	41	107	12	315	330	351	346
2730	347	372	366	3	350	0	2	2
2740	2	2	2	2	2	2	2	2
2750	2	2	2	2	2	2	2	2
2760	2	2	2	2	2	2	2	2
2770	2	2	2	2	344	363	344	365
3000	11	146	36	107	20	30	77	360
3010	20	321	14	67	21	30	71	30
3020	260	17	261	34	26	41	241	24
3030	337	364	346	44	327	70	211	56
3040	76	216	56	66	141	142	106	71
3050	62	102	20	13	30	145	65	15
3060	265	100	142	106	141	102	346	104
3070	20	51	261	70	26	141	346	101
3100	141	106	363	40	14	146	327	111
3110	57	103	67	37	106	142	360	101
3120	30	260	120	20	72	242	143	30

4-2.3 MACRO ROM LISTING WITH DESC. (Cont.)

3130	30	66	141	61	106	71	21	20
3140	14	47	146	106	141	13	20	142
3150	145	144	370	0	1	120	130	123
3160	104	123	20	141	370	1	63	207
3170	141	30	2	11	44	62	102	14
3200	74	370	2	161	202	230	171	27
3210	11	210	64	370	0	71	50	65
3220	61	146	131	22	141	104	14	75
3230	370	5	100	142	107	50	25	22
3240	104	65	370	3	21	70	130	163
3250	130	63	4	141	105	14	370	2
3260	1	61	26	22	125	102	201	62
3270	102	141	106	13	370	7	205	71
3300	201	143	71	164	110	146	142	327
3310	316	71	101	361	0	71	27	107
3320	20	20	220	367	101	327	334	27
3330	327	337	346	342	27	327	342	62
3340	346	347	72	262	347	362	0	106
3350	66	106	327	355	62	27	363	0
3360	327	363	43	102	141	347	33	106
3370	66	360	40	77	257	5	77	106
3400	71	101	361	0	71	360	20	363
3410	0	67	257	15	43	337	31	313
3420	25	101	361	0	71	363	0	106
3430	61	101	142	4	347	44	106	21
3440	20	14	20	72	361	231	4	347
3450	53	41	41	102	343	366	366	4
3460	350	0	364	1	210	103	366	5
3470	350	0	364	0	147	110	142	347
3500	374	364	0	147	110	142	360	0
3510	5	360	1	150	107	363	0	11
3520	331	123	43	147	21	360	231	71
3530	101	145	102	11	331	141	333	206
3540	53	146	105	21	214	150	61	61
3550	71	101	145	106	141	107	234	202
3560	14	105	141	113	145	102	12	335
3570	200	55	335	176	351	376	343	370
3600	351	346	13	142	347	161	43	347
3610	141	11	143	21	360	20	30	144
3620	71	251	306	231	227	33	51	211
3630	321	362	22	23	52	44	272	233
3640	360	5	63	23	213	247	43	103
3650	141	271	255	21	44	101	30	270
3660	263	21	44	53	233	311	103	142
3670	101	71	332	300	52	61	347	272
3700	232	251	30	22	347	274	23	347
3710	231	101	142	104	141	102	41	343
3720	366	366	6	350	0	2	2	2
3730	2	2	2	2	2	2	2	2
3740	2	2	2	2	2	2	2	2
3750	2	2	2	2	2	2	2	2
3760	2	2	2	2	346	113	347	62

4-2.3 MACRO ROM LISTING WITH DESC. (Cont.)

3770	347	72	347	101	347	114	347	211
4000	17	10	206	1	360	4	143	3
4010	40	363	1	3	50	143	3	3
4020	40	53	3	53	103	3	20	150
4030	53	3	355	366	153	360	1	152
4040	350	304	5	350	50	6	355	366
4050	153	112	50	220	62	17	112	351
4060	352	153	360	1	152	17	113	145
4070	11	101	147	21	111	143	20	30
4100	73	103	144	61	360	20	30	71
4110	360	25	71	101	142	53	203	121
4120	42	360	6	74	264	127	42	105
4130	272	34	36	41	261	141	26	206
4140	133	111	145	20	30	75	360	5
4150	66	26	235	17	55	10	205	154
4160	360	6	363	5	3	365	2	226
4170	275	245	177	55	10	350	167	360
4200	4	363	0	3	350	165	47	26
4210	26	26	26	106	145	360	20	30
4220	77	267	227	107	77	77	41	107
4230	146	101	147	10	10	360	6	363
4240	4	327	244	53	27	3	360	5
4250	363	3	3	50	363	0	3	105
4260	146	365	20	55	10	265	263	360
4270	6	363	5	3	10	327	304	360
4300	6	363	3	3	360	2	143	3
4310	112	240	62	220	62	50	220	336
4320	147	20	20	145	146	30	30	77
4330	57	360	1	152	356	12	111	141
4340	20	142	30	71	101	151	52	113
4350	252	64	322	356	343	372	351	247
4360	365	40	350	366	365	20	153	111
4370	65	105	151	112	145	360	1	152
4400	105	55	225	336	5	351	12	6
4410	350	336	141	17	101	351	352	206
4420	165	360	7	143	350	303	153	360
4430	1	152	17	113	230	21	11	101
4440	31	20	144	147	360	120	30	66
4450	266	210	44	24	24	54	54	244
4460	206	76	350	210	110	50	210	74
4470	150	360	2	3	113	355	366	316
4500	110	104	145	74	35	46	101	0
4510	104	65	74	26	113	50	330	163
4520	50	330	130	50	330	157	351	163
4530	105	147	5	351	146	360	0	144
4540	146	363	7	3	101	0	360	0
4550	363	5	3	43	3	351	135	107
4560	75	215	135	101	355	366	5	351
4570	230	147	11	360	1	331	200	40
4600	153	107	0	5	351	230	141	360
4610	3	7	360	4	153	360	0	363
4620	3	351	143	147	360	2	351	200

4-2.3 MACRO ROM LISTING WITH DESC. (Cont.)

4630	366	11	350	0	141	360	0	363
4640	1	3	43	3	23	101	0	152
4650	364	0	360	3	153	112	340	215
4660	55	335	300	141	112	142	101	152
4670	360	2	153	364	0	102	340	221
4700	150	112	141	110	152	101	351	346
4710	141	360	22	76	236	325	146	147
4720	110	142	101	150	0	102	351	346
4730	2	2	2	2	2	2	2	2
4740	2	2	351	310	350	34	350	42
4750	350	61	350	67	350	360	350	364
4760	351	26	351	77	351	114	351	166
4770	351	203	351	223	351	234	351	260
5000	44	44	44	44	44	44	44	44
5010	44	44	44	44	44	44	44	44
5020	44	44	44	44	44	44	44	44
5030	44	44	44	44	44	44	44	44
5040	44	44	44	44	44	44	44	44
5050	44	44	44	44	44	44	44	44
5060	44	44	44	44	44	44	44	44
5070	44	44	44	44	44	44	44	5
5100	352	166	110	50	220	224	50	220
5110	216	50	220	207	234	162	367	125
5120	104	64	64	64	64	104	20	77
5130	324	135	360	62	77	107	142	144
5140	257	321	20	220	321	360	110	74
5150	244	257	54	54	224	323	20	74
5160	214	321	367	110	352	322	360	104
5170	74	204	202	360	3	150	20	363
5200	5	3	360	0	144	143	0	204
5210	202	360	2	150	352	202	224	202
5220	360	1	150	146	224	232	104	66
5230	352	202	101	363	1	3	17	10
5240	10	10	360	6	363	4	3	3
5250	360	2	3	20	150	355	366	360
5260	25	72	242	323	222	305	52	52
5270	52	242	322	360	47	72	222	322
5300	52	222	322	352	323	361	25	110
5310	71	201	322	366	0	367	121	354
5320	3	45	45	45	103	65	235	272
5330	55	235	347	55	235	23	55	235
5340	242	360	4	75	255	5	235	325
5350	75	255	321	235	333	55	235	303
5360	360	2	3	3	17	56	10	206
5370	366	360	4	363	5	3	360	2
5400	3	3	3	352	326	105	67	360
5410	110	77	217	321	110	147	366	231
5420	36	354	3	354	0	370	21	21
5430	21	21	21	27	167	226	152	373
5440	146	46	147	130	66	121	170	202
5450	371	205	142	203	163	162	163	30

4-2.3 MACRO ROM LISTING WITH DESC. (Cont.)

5460	67	374	66	47	47	61	145	164
5470	144	167	372	165	27	106	147	206
5500	167	46	46	375	127	167	201	164
5510	146	170	147	162	370	26	46	46
5520	47	107	227	67	41	47	50	330
5530	174	217	136	313	166	143	20	210
5540	126	105	153	102	145	104	142	101
5550	144	103	141	112	237	157	143	113
5560	353	126	113	300	324	0	53	50
5570	3	33	353	136	57	257	250	217
5600	136	147	102	150	17	216	217	3
5610	3	110	142	107	77	353	171	56
5620	106	20	20	210	231	10	10	353
5630	211	360	4	363	5	3	23	3
5640	353	211	107	146	17	3	3	10
5650	360	2	3	50	153	50	141	150
5660	6	355	370	363	1	3	43	3
5670	355	370	363	1	360	0	3	43
5700	3	363	22	46	360	0	144	145
5710	40	153	0	363	4	107	150	353
5720	304	366	21	350	0	107	146	363
5730	10	353	304	107	36	66	110	147
5740	141	360	110	71	231	351	46	354
5750	3	17	362	20	3	52	272	354
5760	10	10	353	250	2	2	2	2
5770	2	2	353	125	353	313	353	25
6000	6	353	374	360	20	77	77	247
6010	30	77	247	133	40	77	247	236
6020	360	7	77	267	341	67	353	376
6030	67	370	21	166	142	145	150	27
6040	126	167	152	373	47	126	141	144
6050	167	167	145	162	371	163	146	165
6060	26	127	47	66	147	374	121	146
6070	165	167	144	171	171	26	372	106
6100	147	161	165	147	162	142	165	375
6110	166	164	26	127	47	67	101	145
6120	370	165	162	142	151	165	167	30
6130	161	353	372	67	370	21	21	21
6140	167	163	145	26	127	152	373	206
6150	161	144	142	162	163	142	166	371
6160	26	147	127	167	207	101	145	150
6170	374	142	146	162	30	121	162	163
6200	142	372	164	163	171	144	146	27
6210	206	167	375	47	130	67	126	141
6220	163	164	164	370	142	145	170	203
6230	147	27	107	201	353	372	67	370
6240	21	21	26	146	106	227	206	106
6250	152	373	166	121	151	165	203	146
6260	165	165	371	145	27	47	66	46
6270	147	127	167	374	41	165	142	162

4-2.3 MACRO ROM LISTING WITH DESC. (Cont.)

6300	163	142	166	27	372	141	204	27
6310	226	166	47	121	206	375	30	46
6320	107	167	46	147	221	171	370	163
6330	203	230	231	27	46	106	161	353
6340	372	370	147	70	66	47	167	66
6350	227	121	375	227	206	147	127	167
6360	41	27	106	372	21	165	166	167
6370	203	27	206	166	353	372	113	330
6400	3	351	362	106	330	53	50	330
6410	110	50	330	145	104	151	101	141
6420	111	142	20	30	72	102	151	20
6430	6	355	40	363	1	3	43	3
6440	153	143	144	145	146	147	142	40
6450	152	101	0	217	65	367	21	37
6460	360	4	67	101	150	104	255	73
6470	57	35	65	106	20	310	100	47
6500	107	141	105	12	152	364	0	0
6510	106	143	20	20	30	30	73	101
6520	11	142	103	146	105	74	30	64
6530	104	65	21	61	23	333	141	71
6540	71	102	33	355	362	30	20	20
6550	50	50	50	270	203	104	74	145
6560	35	360	100	66	101	0	217	200
6570	367	21	37	47	47	47	47	150
6600	366	20	0	147	104	65	105	30
6610	40	153	33	57	107	50	50	310
6620	223	367	21	356	14	114	16	154
6630	115	16	155	116	16	156	117	16
6640	157	120	16	160	121	16	161	122
6650	16	162	123	16	163	124	16	164
6660	125	16	165	126	16	166	127	16
6670	167	130	16	170	131	16	171	132
6700	16	172	133	16	173	134	16	174
6710	135	16	175	136	16	176	137	16
6720	177	107	20	310	335	360	1	152
6730	102	237	366	351	346	110	152	101
6740	150	364	0	366	0	102	343	376
6750	2	2	2	2	2	2	2	2
6760	355	166	355	103	354	376	355	17
6770	355	41	355	206	355	225	355	325
7000	146	17	10	206	2	360	2	3
7010	355	366	356	213	356	161	144	113
7020	320	75	114	11	321	42	66	21
7030	266	33	41	21	21	201	146	101
7040	356	70	360	21	30	21	71	51
7050	51	51	41	26	241	52	360	5
7060	66	26	106	20	20	200	146	106
7070	145	104	141	351	364	104	153	106
7100	56	56	306	146	20	40	147	114
7110	11	301	146	21	360	21	30	40
7120	40	40	71	26	41	241	123	113
7130	141	360	5	66	26	106	145	220

4-2.3 MACRO ROM LISTING WITH DESC. (Cont.)

7140	146	20	50	50	240	152	366	22
7150	350	0	366	62	107	30	66	355
7160	372	101	153	5	356	171	6	356
7170	261	112	50	220	211	35	35	47
7200	47	105	67	107	152	17	101	351
7210	352	105	146	107	50	220	261	17
7220	10	10	360	5	363	3	3	50
7230	43	3	40	363	1	3	23	3
7240	50	363	3	3	327	256	40	143
7250	3	3	50	363	2	3	360	2
7260	3	113	141	142	363	0	105	30
7270	40	153	355	374	2	2	2	2
7300	2	5	341	376	153	360	0	145
7310	147	6	360	1	152	20	363	6
7320	3	23	113	11	301	327	43	21
7330	360	3	71	360	21	30	71	41
7340	26	241	337	360	5	66	26	106
7350	141	20	20	20	220	363	361	20
7360	31	31	51	217	10	20	20	20
7370	146	220	376	20	230	23	333	1
7400	43	43	101	40	147	110	356	323
7410	57	107	30	30	30	61	101	146
7420	36	103	145	6	357	30	357	364
7430	55	255	366	55	255	370	55	255
7440	372	55	255	374	357	376	365	7
7450	55	255	111	106	26	330	340	50
7460	330	342	50	330	344	50	330	346
7470	50	330	350	50	330	352	50	330
7500	354	50	330	356	50	330	360	357
7510	362	112	230	120	20	363	5	3
7520	113	355	366	2	2	2	2	2
7530	2	2	2	2	2	2	2	2
7540	2	2	2	2	2	2	2	2
7550	2	2	2	2	2	2	2	2
7560	2	2	2	2	2	2	2	2
7570	2	2	2	2	2	2	2	2
7600	2	2	2	2	2	2	2	2
7610	2	2	2	2	2	2	2	2
7620	2	2	2	2	2	2	2	2
7630	2	2	2	2	2	2	2	2
7640	2	2	2	2	2	2	2	2
7650	2	2	2	2	2	2	2	2
7660	2	2	2	2	2	2	2	2
7670	2	2	2	2	2	2	2	2
7700	2	2	2	2	2	2	2	2
7710	2	2	2	2	2	2	2	2
7720	2	2	2	2	2	2	2	2
7730	2	2	2	2	2	2	356	301
7740	357	50	357	50	357	50	357	50
7750	357	50	357	50	357	50	357	50
7760	357	50	357	50	357	23	357	46
7770	357	46	357	46	357	46	357	46

4-2.4 MACRO ROM LISTING (000-777$_8$)

338	GOTO 29/0535	PRINT	0	341 SUB-ROUTINES
2	GOTO 72/0565	UNPACK	1	
4	GOTO 163/1000	PACK	2	
6	GOTO 67/0613	MULTIPLY	3	
10	GOTO 109/0643	DIVIDE	4	
12	GOTO 63/0675	SQ. RT.	5	
14	GOTO 22/0733	KEY	6	
16	GOTO 235/0752	PRINT STO	7	
20	GOTO 200/0212	0.		
22	GOTO 201/0211	1		
24	GOTO 202/0210	2		
26	GOTO 203/0207	3		
30	GOTO 204/0206	4		340 206
32	GOTO 205/0205	5		
34	GOTO 206/0204	6		
36	GOTO 207/0203	7		
40	GOTO 208/0202	8		
42	GOTO 209/0201	9.		
44	GOTO 210/6750	0		
46	GOTO 101/0225	SET DEC ( )		
50	GOTO 240/4774	STOP		
MISC KEY 1 52	GOTO 188/0230	ENT EXP		
MISC KEY 1 54	GOTO 189/0237	ARC		
MISC KEY 2 56	GOTO 190/4742	RECALL ( ) ( )		
MISC KEY 1 60	GOTO 191/0272	STORE ( ) ( )		
MISC KEY 1 62	GOTO 192/0245	ACCUM STORE ( ) ( )		

4-2.4 MACRO ROM LISTING - $000\text{-}777_8$ (Cont.)

MISC KEY 1	64 GOTO 193/0250	ENTER
MISC KEY 1	66 GOTO 194/0256	$\cdot X^2$
1	70 GOTO 195/0264	π
MISC KEY 1	72 GOTO 196/0300	CHG SIGN
MISC KEY 1	74 GOTO 197/0372	INTGER
	76 GOTO 182/4754	TO POLAR
	100 GOTO 199/1774	. —
	102 GOTO 211/0502	$\sqrt{\lvert X \rvert}$
	104 GOTO 212/0452	$1/X$
	106 GOTO 213/0432	$\lvert A \rvert^X$
	110 GOTO 214/0215	SIN
	112 GOTO 215/0221	COS
	114 GOTO 216/2060	TAN
	116 GOTO 217/0476	LOG|X|
	120 GOTO 218/3776	$\lvert X \rvert !$
	122 GOTO 51/1776	+ 343
	124 GOTO 94/2774	LN|X|
	126 GOTO 145/3766	$\frac{\%}{\%}$
	130 GOTO 146/3772	$X\%$
	132 GOTO 32/1770	e^X
	134 GOTO 180/4756	TO RECT
MISC KEY 1	136 GOTO 250/0372	DEG
MISC KEY 1	140 GOTO 251/0403	RAD
	142 GOTO 409/7736	CLEAR ENTRY
	144 GOTO 244/4750	PRINT
	146 GOTO 245/4760	PRINT SCI

4-2.4 MACRO ROM LISTING - $000\text{-}777_8$ (Cont.)

```
LINE FEED
  1 . 150 GOTO 246 / 4744      LINE SPACE
      152 GOTO 238 / 4772      GO TO ( ) ( )
      154 GOTO 236 / 4766      IF NEG ( ) ( )
      156 GOTO 187 / 0361      CLR ALL REGS
      160 HALT                 START
      161 HALT
      162 HALT                 ONE STEP
      163 HALT
      164 GOTO 321 / 7016      INDIRECT
MISC KEY
  1   166 GOTO  21 / 0352340   (POWER UP)
      170 HALT
      171 HALT
      172 GOTO 341 / 0423      (RESET)
      174 GOTO 232 / 4770      PROG CODE ( ) ( )
      176 HALT                 (NULL)
      177 HALT
      200
  209 201 +DEL 4 (044)
  208 202 +DEL 4
  207 203 +DEL 4
  206 204 +DEL 4
  205 205 +DEL 4
  204 206 +DEL 4               N → R4
  203 207 +DEL 4
  202 210 +DEL 4
  201 211 +DEL 4
  200 212 STORE 1              Save R0 → R1
      213 GOTO 336 / 6704

  214 215 11 TO 7
      217 GOTO  76

  215 221 02 TO 7
      223 GOTO  76
```

4-2.4 MACRO ROM LISTING - 000-777$_8$ (Cont.)

```
101  225 03 TO 6
     227 HALT

188  0230 10 TO 6
     232 LEFT 6
     233 +DEL 6
     234 00 TO 5
     236 HALT

189  237 01 TO 4
     241 HALT

191  242 02 TO 6
     244 HALT

192  245 22 TO 6
     247 HALT

193  250 STORE 2
     251 BRANCH TO 337 IF #7 ENTIRE=0
     253 +DEL 7
     254 GOTO 248
194  256 STORE 2
     257 STORE 7
     260 00 TO 4
     262 GOTO  50

195  264 STORE 10
     265 31415926535890100 TO 0
     276 GOTO 249

196  300 GOSUB UNPACK
     301 00 TO 3
     303 BRANCH TO  26 IF #1 LSD≠0
     305 +DEL 3
 26  306 RIGHT 1
     307 BRANCH TO 381 IF #7 ENTIRE≠0
     311 STORE 6
     312 01 TO 0
     314 STORE 12
     315 LOAD 6
     316 GOTO 169

381  320 GOTO   9

197  322 GOSUB UNPACK
     323 STORE 2
     324 00 TO 3
     326 BRANCH TO  27 IF #1 LSD=0
     330 +DEL 3
```

4-2.4 MACRO ROM LISTING - 000-777$_8$ (Cont.)

```
 27  331 RIGHT 1
     332 11 TO 4
     334 LEFT 4
     335 03 TO 0
     337 ADD 4
     340 LOAD 1
     341 SUB 4
 28  342 +DEL 1
     343 -DEL 4
     344 RIGHT 2
     345 BRANCH TO  28 IF #4 MSD=0
     347 LOAD 2
     350 GOTO 169

 21  352 02 TO 0 AD                          POWER UP
     354 STORE 11      DEC PT 2
     355 RIGHT 0     } SET YY
     356 04 TO 3       DEGREES LIGHT
     360 OUTPUT      }
187  361 01 TO 0
     363 STORE 7
     364 STORE 3
     365 RIGHT 0
     366 STORE 10
     367 STORE 2
     370 GOTO  16.    6774
250  372 04 TO 3
252  374 STORE 1
     375 00 TO 0
     377 OUTPUT
     400 LOAD 1
     401 GOTO 17

251  403 00 TO 3
     405 GOTO 252

407  407 BRANCH TO 337 IF #7 ENTIRE=0
     411 LOAD 10
     412 STORE 2
     413 03 TO 0
     415 OUTPUT
     416 RIGHT 0
     417 STORE 10
     420 LOAD 2
337  421 GOTO  17

341  423 02 TO 0
     425 OUTPUT
     426 RIGHT 0
     427 STORE 10
     430 GOTO  17
```

4-2.4 MACRO ROM LISTING - $000\text{-}777_8$ (Cont.)

```
213  432 STORE 2
     433 LOAD 10
     434 BRANCH TO 181 IF #0 ENTIRE≠0
     436 STORE 10
     437 GOTO 249

181  441 STORE 1
     442 LOAD 2
     443 STORE 10
     444 01 TO 0
     446 STORE 13
     447 LOAD 1
     450 GOTO  94

212  452 1000000000000100 TO 2
     463 01 TO 4
     465 STORE 7
     466 BRANCH TO  34 IF #0 ENTIRE≠0
     470 08 TO 6
     472 GOTO   1

 34  474 GOTO  50

217  476 10 TO 3
     500 GOTO  95
211  502 GOSUB UNPACK
     503 STORE 2
     504 RIGHT 1
     505 RIGHT 2
     506 LOAD 1
     507 STORE 4
     510 ADD 1
     511 LOAD 1
     512 ADD 4
     513 ADD 4
     514 05 TO 0
     516 BRANCH TO  66 IF #4 LSD=0
     520 SUB 4
     521 LEFT 2
 66  522 LEFT 0
     523 RIGHT 4
     524 ADD 4
     525 LOAD 2
     526 GOSUB SQUARE ROOT
     527 STORE 2
     530 LOAD 4
     531 STORE 1
     532 LOAD 2
     533 GOTO 169
 29  535 LOAD 6
     536 STORE 1
```

IAIX STARTS HERE

not needed

PRINT

4-2.4 MACRO ROM LISTING - $000\text{-}777_8$ (Cont.)

```
      537 RIGHT 0
      540 STORE 6
      541 LEFT 0
      542 SUB 1
      543 LOAD 1
      544 STORE 2
      545 07 TO 3
      547 06 TO 4
      551 08 TO 0
      553 SUB 1
      554 BRANCH TO  30 IF #1 MSD=0
      556 ADD 1
      557 +DEL 4
30    560 LOAD 1
      561 SUB 3
      562 LOAD 4
      563 OUTPUT
      564 RETURN

72    565 STORE 1  UNPACK S/R          141
      566 RIGHT 0                      020
      567 RIGHT 0                      020
      570 RIGHT 0                      020
      571 LEFT 0                       030
      572 LEFT 0
      573 STORE 6                      146
      574 LEFT 0
      575 SUB 1
      576 LEFT 1
      577 +DEL 1
      600 20 TO 0
      602 LEFT 0
      603 LEFT 0
      604 SUB 1
      605 BRANCH TO  73 IF #1 MSD=0
      607 ADD 1
      610 -DEL 1
>73   611 LOAD 6
      612 RETURN

67    613 10 TO 2
68    615 LEFT 2
      616 BRANCH TO  68 IF #2 MSD=0
      620 ADD 2
      621 LOAD 1
      622 00 TO 1
69    624 BRANCH TO  70 IF #2 LSD=0
      626 ADD 1
      627 -DEL 2
      630 GOTO  69
```

4-2.4 MACRO ROM LISTING - $000\text{-}777_8$ (Cont.)

```
 70  632 BRANCH TO  71 IF #2 ENTIRE=0
     634 RIGHT 1
     635 RIGHT 2
     636 GOTO  69

 71  640 SUB 1
     641 LOAD 1
     642 RETURN

109  643 10 TO 2
     645 GOTO 111

110  647 SUB 1
     650 BRANCH TO 113 IF #1 MSD=0
     652 BRANCH TO 114 IF #2 MSD≠0
     654 ADD 1
     655 LEFT 1
     656 LEFT 2
111  657 BRANCH TO 110 IF #1 MSD=0
112  661 SUB 1
     662 BRANCH TO 113 IF #1 MSD=0
     664 +DEL 2
     665 GOTO 112

113  667 +DEL 2
     670 GOTO 110

114  672 LEFT 2
     673 LOAD 2
     674 RETURN

 63  675 STORE 2
     676 RIGHT 2
     677 10 TO 0
     701 STORE 3
     702 LEFT 3
 64  703 LEFT 3
     704 -DEL 0
     705 BRANCH TO  64 IF #0 ENTIRE≠0
     707 STORE 1
 65  710 SUB 2
     711 LOAD 3
     712 ADD 1
     713 LOAD 1
     714 SUB 2
     715 BRANCH TO 65 IF #2 MSD=0
     717 ADD 2
     720 LOAD 3
     721 SUB 1
     722 LOAD 1
     723 ADD 2
```

4-2.4 MACRO ROM LISTING - $000\text{-}777_8$ (Cont.)

```
     724 RIGHT 3
     725 LEFT 2
     726 BRANCH TO 65 IF #3 ENTIRE≠0
     730 LEFT 0
     731 LEFT 0
     732 RETURN
--------------------------------------------------
 22  733 BRANCH TO  23 IF #3 LSD=0
     735 00 TO 0
     737 RETURN
--------------------------------------------------
 23  740 BRANCH TO  25 IF #5 ENTIRE≠0
     742 BRANCH TO 24 IF #7 LSD=0
     744 STORE 2
     745 GOTO 25

 24  747 LOAD 1
 25  750 =DEL 5
     751 RETURN

235  752 01 TO 0
     754 STORE 3
     755 OUTPUT
     756 04 TO 0
     760 OUTPUT
     761 OUTPUT
     762 RETURN

     763
     764
     765
     766
     767
     770
     771
     772
     773
     774
     775
243  776 GOTO 407
--------------------------------------------------
?
```

4-2.4 MACRO ROM LISTING - $1000\text{-}1777_8$ (Cont.)

```
163 1000 BRANCH TO 165 IF #0 ENTIRE≠0
    1002 STORE 1
    1003 RETURN

164 1004 -DEL 1
    1005 LEFT 0
165 1006 BRANCH TO 164 IF #0 MSD=0
    1010 RIGHT 0
    1011 50 TO 2
    1013 ADD 2
    1014 BRANCH TO 166 IF #2 MSD=0
    1016 RIGHT 2
    1017 +DEL 1
166 1020 RIGHT 2
    1021 RIGHT 2
    1022 LEFT 2
    1023 LEFT 2
    1024 LEFT 2
    1025 BRANCH TO 168 IF #1 MSD≠0
    1027 +DEL 1
    1030 20 TO 0
    1032 LEFT 0
    1033 SUB 1
    1034 BRANCH TO 276 IF #1 MSD=0
    1036 ADD 1
    1037 BRANCH TO 167 IF #3 LSD=0
    1041 ADD 1
167 1042 LOAD 2
    1043 ADD 1
    1044 LOAD 1
    1045 RETURN

168 1046 00 TO 0
    1050 STORE 1
    1051 RETURN

276 1052 07 TO 6
    1054 GOTO  1

342 1056 GOSUB PACK
    1057 GOTO 249

343 1061 GOSUB UNPACK
    1062 STORE 3
    1063 LOAD 1
    1064 STORE 4
    1065 STORE 5
    1066 RIGHT 4
    1067 LOAD 3
    1070 STORE 1
    1071 0230258509299405 TO 0   k
    1102 GOSUB DIVIDE
```

4-2.4 MACRO ROM LISTING - $1000\text{-}1777_8$ (Cont.)

```
      1103 BRANCH TO  35 IF #2 MSD≠0
      1105 LEFT 2
      1106 -DEL 4
 35   1107 10 TO 0
      1111 LEFT 0
      1112 STORE 6
      1113 +DEL 0
      1114 +DEL 0
      1115 SUB 4
      1116 BRANCH TO  33 IF #4 MSD=0
 36   1120 RIGHT 2
      1121 +DEL 4
      1122 BRANCH TO  36 IF #4 MSD≠0
      1124 LOAD 2
      1125 LEFT 0
      1126 LEFT 0
      1127 LEFT 0
      1130 RIGHT 0
      1131 STORE 7
      1132 RIGHT 0
      1133 RIGHT 0
      1134 SUB 2
      1135 13 TO 0
 37   1137 -DEL 0
      1140 RIGHT 2
      1141 BRANCH TO  37 IF #0 ENTIRE≠0
      1143 LOAD 2
      1144 ADD 6
      1145 BRANCH TO  39 IF #5 LSD=0
      1147 SUB 6
      1150 SUB 6
      1151 -DEL 6
      1152 10 TO 0
 38   1154 LEFT 0
      1155 BRANCH TO  38 IF #0 MSD=0
      1157 SUB 7
      1160 LOAD 7
      1161 00 TO 7
      1163 SUB 7
 39   1164 LEFT 6
      1165 LOAD 7
      1166 ADD 7
      1167 BRANCH TO  40 IF #7 MSD=0
      1171 +DEL 6
      1172 LEFT 7
      1173 RIGHT 7
 40   1174 LOAD 7
      1175 STORE 1
      1176 GOSUB MULTIPLY
      1177 RIGHT 0
      1200 STORE 5
```

4-2.4 MACRO ROM LISTING - $1000\text{-}1777_8$ (Cont.)

```
    1201 RIGHT 0
    1202 STORE 1
    1203 0847836959839180 TO 0
    1214 ADD 1
    1215 LOAD 5
    1216 GOSUB MULTIPLY
    1217 0575873587931610 TO 0
    1230 ADD 1
    1231 LOAD 1
    1232 STORE 4
    1233 STORE 3
    1234 LOAD 5
    1235 STORE 1
    1236 0003816548819161 TO 0
    1247 GOSUB MULTIPLY
    1250 0121892417408701 TO 0
    1261 ADD 1
    1262 LOAD 5
    1263 GOSUB MULTIPLY
    1264 0331499484753236 TO 0
    1275 ADD 1
    1376 LOAD 7
    1277 GOSUB MULTIPLY
    1300 SUB 4
    1301 LOAD 3
    1302 ADD 1
    1303 LOAD 4
    1304 GOSUB DIVIDE
    1305 RIGHT 2
    1306 BRANCH TO  41 IF #6 LSD=0
    1310 LOAD 2
    1311 STORE 1
    1312 0316227766016838 TO 0
    1323 GOSUB DIVIDE
41  1324 00 TO 3
    1326 LOAD 6
    1327 RIGHT 0
    1330 STORE 1
    1331 LOAD 2
    1332 GOTO 169

33  1334 BRANCH TO  31 IF #5 LSD=0
    1336 00 TO 0
    1340 GOTO 249

31  1342 01 TO 6
    1344 GOTO  1

344 1346 10 TO 7
    1350 GOSUB UNPACK
    1351 RIGHT 0
    1352 STORE 3
```

4-2.4 MACRO ROM LISTING - 1000-17778 (Cont.)

```
     1353 BRANCH TO  42 IF #1 LSD=0
     1355 +DEL 7
  42 1356 RIGHT 1
     1357 LOAD 1
     1360 STORE 5
     1361 LOAD 10
     1362 GOSUB UNPACK
     1363 RIGHT 0
     1364 LEFT 7
     1365 BRANCH TO  43 IF #1 LSD=0
     1367 +DEL 7
  43 1370 STORE 6
     1371 RIGHT 1
     1372 LOAD 1
     1373 STORE 4
     1374 LOAD 5
     1375 SUB 1
     1376 BRANCH TO  45 IF #1 MSD≠0
  44 1400 RIGHT 3
     1401 -DEL 1
     1402 BRANCH TO  44 IF #1 MSD=0
     1404 LEFT 3
     1405 GOTO  46
  45 1407 +DEL 1
     1410 RIGHT 6
     1411 BRANCH TO  45 IF #1 MSD≠0
     1413 LOAD 5
     1414 STORE 4
  46 1415 LOAD 6
     1416 STORE 1
     1417 LOAD 3
     1420 SUB 1
     1421 ADD 6
     1422 BRANCH TO 304 IF #6 ENTIRE=0
     1424 LEFT 7
     1425 BRANCH TO  47 IF #1 MSD=0
     1427 +DEL 7
     1430 LOAD 1
     1431 00 TO 1
     1433 SUB 1
  47 1434 LOAD 6
     1435 GOSUB DIVIDE
     1436 STORE 5
     1437 STORE 1
     1440 GOSUB MULTIPLY
     1441 10 TO 0
  48 1443 LEFT 0
     1444 BRANCH TO  48 IF #0 MSD=0
     1446 ADD 1
     1447 RIGHT 1
     1450 LOAD 1
```

4-2.4 MACRO ROM LISTING - $1000\text{-}1777_8$ (Cont.)

```
      1451 ADD 1
      1452 ADD 1
      1453 ADD 1
      1454 ADD 1
      1455 LOAD 1
      1456 GOSUB SQUARE ROOT
      1457 STORE 1
      1460 LOAD 6
      1461 GOSUB MULTIPLY
      1462 LEFT 0
      1463 STORE 2
      1464 LOAD 4
      1465 STORE 1
      1466 LOAD 2
      1467 GOSUB PACK
      1470 STORE 12
      1471 STORE 10
      1472 LOAD 5
      1473 STORE 6
      1474 GOTO 127
304   1476 10 TO 6
      1500 GOTO  I          R4=>R0

 49   1502 LOAD 4      > Clr R4
      1503 SUB 4
      1504 ADD 6        R6=R6+R4
      1505 LOAD 1       R1->R0
      1506 +DEL 6       R6 = R6+1
      1507 HALT

345   1510 10 TO 4      10->R4
346   1512 STORE 1      R0->R1
      1513 10 TO 0      10->R0
      1515 LEFT 0       R0=100
      1516 SUB 6     >  R6=R6-100
      1517 -DEL 6
      1520 BRANCH TO 49 IF #6 ENTIRE=0
      1522 LOAD 1
      1523 GOSUB UNPACK GO TO 0002
      1524 STORE 7
      1525 BRANCH TO 52 IF #4 ENTIRE=0
      1527 -DEL 1
      1530 BRANCH TO 52 IF #1 LSD=0
      1532 +DEL 1
      1533 +DEL 1
 52   1534 00 TO 3
      1536 BRANCH TO 53 IF #1 LSD=0
      1540 +DEL 3
 53   1541 LOAD 1       R3=3 or 4
      1542 RIGHT 0
      1543 STORE 5
```

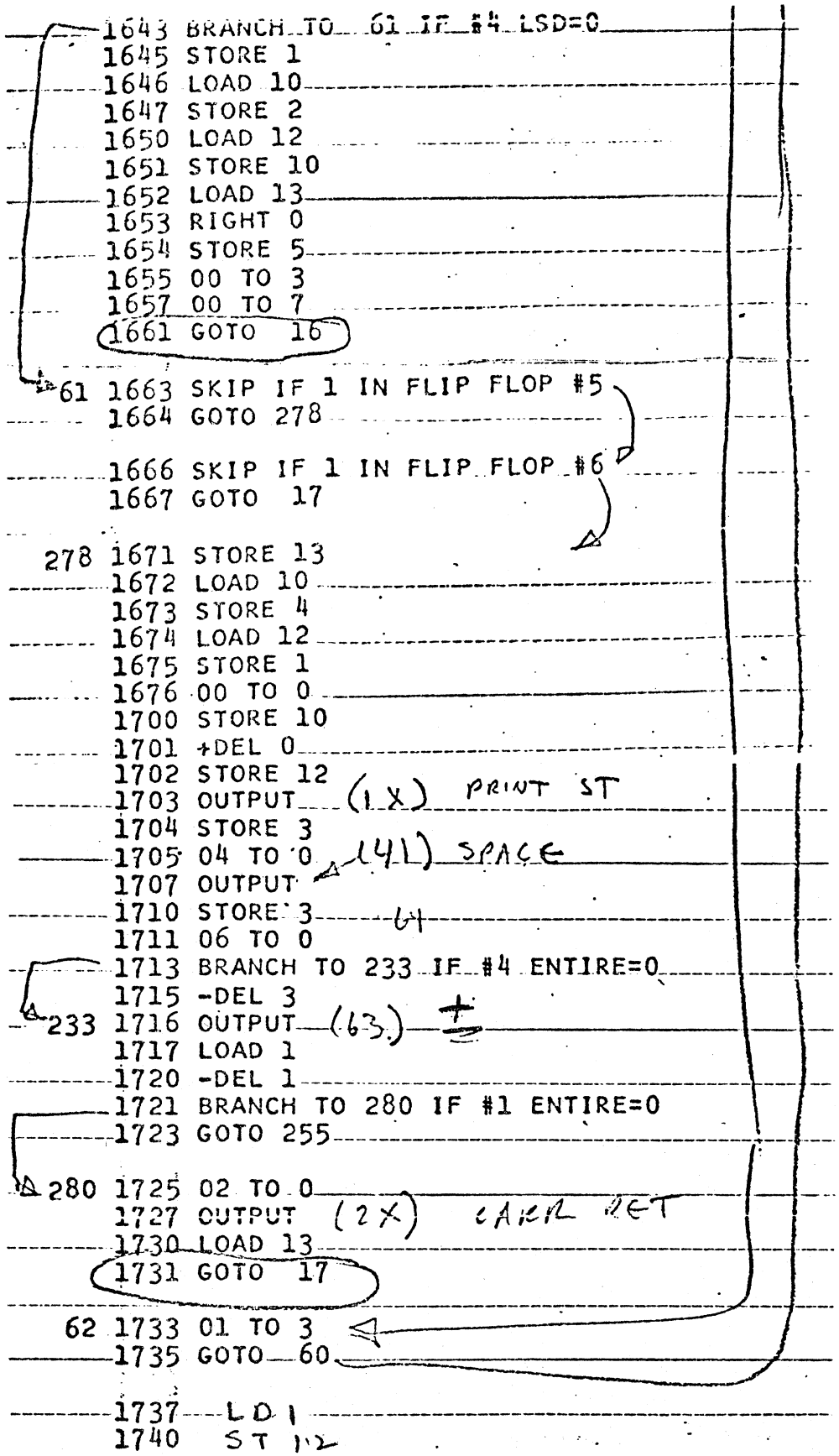
141
362
030
076
056
236
101
011

4-2.4 MACRO ROM LISTING - $1000\text{-}1777_8$ (Cont.)

```
      1544 LOAD 10
      1545 GOSUB UNPACK
      1546 BRANCH TO  54 IF #1 LSD=0
      1550 +DEL 3
      1551 +DEL 3
54    1552 STORE 6
      1553 LOAD 13
      1554 BRANCH TO 234 IF #0 LSD≠0
      1556 LOAD 4
      1557 STORE 10
234   1560 LOAD 1
      1561 RIGHT 0
      1562 STORE 4
      1563 SUB 5
55    1564 RIGHT 7
      1565 BRANCH TO  56 IF #5 MSD=0
      1567 +DEL 5
      1570 GOTO  55

56    1572 -DEL 5
      1573 +DEL 4
      1574 RIGHT 6
      1575 BRANCH TO  56 IF #5 MSD=0
      1577 LOAD 3
      1600 -DEL 0
      1601 BRANCH TO  58 IF #0 MSD≠0
      1603 -DEL 0
      1604 -DEL 0
      1605 BRANCH TO  58 IF #0 MSD=0
      1607 LOAD 7
      1610 00 TO 7
      1612 SUB 7
58    1613 LOAD 7
      1614 ADD 6
      1615 BRANCH TO  59 IF #6 MSD=0
      1617 LOAD 6
      1620 00 TO 6
      1622 SUB 6
      1623 -DEL 3
      1624 -DEL 3
59    1625 BRANCH TO  62 IF #3 MSD≠0
      1627 -DEL 3
      1630 -DEL 3
      1631 BRANCH TO  62 IF #3 MSD=0
      1633 00 TO 3
60    1635 LOAD 4
      1636 STORE 1
      1637 LOAD 13
      1640 STORE 4
      1641 LOAD 6
      1642 GOSUB PACK
```

4-2.4 MACRO ROM LISTING - $1000\text{-}1777_8$ (Cont.)



4-2.4 MACRO ROM LISTING - $1000\text{-}1777_8$ (Cont.)

```
        1741   LD 4
        1742   RT 1
        1743   ADD I
        1744   GO TO
        1745   6534
        1746   LD 3
        1747   ST 4
        1750   LD 12
        1751   ST 3
        1752   LD 2
        1753   PACK
        1754   ST 12
        1755   LD 4
        1756   ST 3
        1757   RT 1
        1760   GO
        1761   LD 1
        1762   HALT
        1763
        1764
        1765
  169   1766   GOTO 342
   32   1770   GOTO 343
  198   1772   GOTO 344
  199   1774   GOTO 345
   51   1776   GOTO 346 / 1512   343
? 2000,2777
```

4-2.4 MACRO ROM LISTING - $2000\text{-}2777_8$

```
 216 2000 30 TO 7
 -76 2002 BRANCH TO --77-- IF #4 LSD=0
     2004 GOTO 116
-------------------------------------------------------
  77 2006 RIGHT 7
 ---- 2007 GOSUB UNPACK
     2010 BRANCH TO  78 IF #7 LSD≠0
 -------2012 RIGHT 1
     2013 LEFT 1
 ---78 2014 STORE 5
     2015 00 TO 3
 ---- 2017 BRANCH TO --79 IF #1 LSD=0
     2021 +DEL 3
 ---79 2022 RIGHT 1
     2023 LOAD 1
 -------2024 STORE 4
     2025 LOAD 5
 -------2026 STORE 1
     2027 06283185307179 59 TO 0          K1
 -------2040 SKIP IF 1 IN FLIP-FLOP #4
     2041 GOTO  81
-------------------------------------------------------
     2043 36 TO 0
 --80 2045 LEFT 0
     2046 BRANCH TO  80 IF #0 MSD=0
 -------2050 RIGHT 0
     2051 -DEL 4
 -------2052 -DEL 4
   81 2053 GOSUB DIVIDE
     2054 10 TO 0
     2056 LEFT 0
 -------2057 +DEL 0
     2060 SUB 4
 ---82 2061 RIGHT 2
     2062 +DEL 4
 ---- 2063 BRANCH TO - 82 IF #4 MSD≠0
     2065 LEFT 2
 ---83 2066 LEFT 2
     2067 -DEL 4
 -------2070 BRANCH TO-- 83 IF #4 MSD=0
     2072 25 TO 0
 --84 2074 LEFT 0
     2075 BRANCH TO  84 IF #0 MSD=0
 -------2077 BRANCH TO-- 85 IF #7 LSD≠0
     2101 +DEL 7
 ------- 2102 ADD 2
   85 2103 RIGHT 2
 ------ 2104 LOAD 2
     2105 ADD 2
 -------2106 -DEL 7
     2107 BRANCH TO  86 IF #2 MSD=0
 -------2111 LEFT 2
```

4-2.4 MACRO ROM LISTING - $2000\text{-}2777_8$ (Cont.)

```
      2112 RIGHT 2
      2113 BRANCH TO 86 IF #7 LSD≠0
      2115 +DEL 3
86    2116 LOAD 2
      2117 ADD 2
      2120 BRANCH TO  88 IF #2 MSD=0
      2122 BRANCH TO  87 IF #7 LSD=0
      2124 +DEL 3
87    2125 LOAD 2
      2126 LEFT.0
      2127 RIGHT 0
      2130 SUB 2
      2131 SUB 2
88    2132 LOAD 2
      2133 STORE 6
      2134 RIGHT 0
      2135 STORE 1
      2136 ADD 1
      2137 LOAD 1
      2140 GOSUB MULTIPLY
      2141 STORE 4
      2142 STORE 5
      2143 0623578407727670 TO 0   K2
      2154 STORE 1
      2155 0696791957182651 TO 0   K3
      2166 ADD 4
      2167 LOAD 4
      2170 GOSUB DIVIDE
      2171 0376059385782401 TO 0   K4
      2202 STORE 1
      2203 0062713918273188 TO 0   K5
      2214 SUB 2
      2215 LOAD 5
      2216 ADD 2
      2217 LOAD 2
      2220 GOSUB DIVIDE
      2221 3420595803881187 TO 0   K6
      2232 STORE 1
      2233 0414531378928896 TO 0   K7
      2244 ADD 2
      2245 LOAD 5
      2246 RIGHT 0
      2247 ADD 2
      2250 ADD 2
      2251 LOAD 2
      2252 GOSUB DIVIDE
      2253 3790932102782074 TO 0   K8
      2264 SUB 2
      2265 LOAD 2
      2266 STORE 1
      2267 LOAD 6
      2270 GOSUB MULTIPLY
```

4-2.4 MICRO ROM LISTING - $2000\text{-}2777_8$ (Cont.)

```
     2271 LEFT 0
     2272 BRANCH TO  92 IF #7 LSD=0
     2274 -DEL 7
     2275 BRANCH TO 90 IF #7 LSD=0
     2277 ADD 7
     2300 10 TO 2
 89  2302 LEFT 2
     2303 BRANCH TO 89 IF #2 MSD=0
     2305 LOAD 6
     2306 SUB 2
     2307 GOTO 88
 90  2311 LOAD 1
     2312 STORE 6
     2313 BRANCH TO  75 IF #6 ENTIRE=0
 91  2315 LEFT 6
     2316 +DEL 2
     2317 BRANCH TO  91 IF #6 MSD=0
     2321 RIGHT 6
     2322 -DEL 2
     2323 -DEL 2
     2324 LOAD 7
     2325 STORE 1
     2326 LOAD 2
     2327 STORE 7
     2330 LOAD 6
     2331 GOSUB DIVIDE
 92  2332 STORE 4
     2333 -DEL 3
     2334 -DEL 3
     2335 BRANCH TO  93 IF #3 MSD=0
     2337 +DEL 3
     2340 +DEL 3
 93  2341 99 TO 1
     2343 LOAD 13
     2344 STORE 5
     2345 LOAD 7
     2346 ADD 1
     2347 LOAD 4
     2350 GOSUB PACK
     2351 BRANCH TO 223 IF #5 LSD=0
     2353 GOTO 57

223  2355 GOTO 249

 75  2357 02 TO 6
     2361 GOTO  1

347  2363 00 TO 3
348  2365 BRANCH TO 274 IF #0 ENTIRE=0
     2367 GOSUB UNPACK
     2370 RIGHT 1
     2371 STORE 5
```

4-2.4 MACRO ROM LISTING - $2000\text{-}2777_8$ (Cont.)

```
      2372 STORE 6
      2373 0316227766016838 TO 2
      2404 10 TO 0
      2406 LEFT 0
      2407 SUB 1
      2410 BRANCH TO  96 IF #1 MSD=0
      2412 +DEL 3
      2413 +DEL 1
      2414 LOAD 1
      2415 00 TO 1
      2417 SUB 1
   96 2420 LOAD 1
      2421 LEFT 0
      2422 STORE 7
      2423 BRANCH TO  97 IF #3 LSD≠0
      2425 LOAD 2
      2426 SUB 5
      2427 BRANCH TO 102 IF #5 MSD≠0
      2431 05 TO 0
      2433 ADD 7
      2434 GOTO 104
   97 2436 LOAD 5
      2437 SUB 2
      2440 BRANCH TO  98 IF #2 MSD≠0
      2442 05 TO 0
      2444 ADD 7
      2445 GOTO 100

   98 2447 10 TO 2
   99 2451 LEFT 2
      2452 BRANCH TO  99 IF #2 MSD=0
      2454 LOAD 5
      2455 SUB 2
  100 2456 LOAD 2
      2457 STORE 5
      2460 GOTO 104

  102 2462 ADD 5
      2463 10 TO 0
  103 2465 LEFT 0
      2466 BRANCH TO 103 IF #0 MSD=0
      2470 RIGHT 0
      2471 SUB 5
  104 2472 LOAD 6
      2473 ADD 6
      2474 LOAD 5
      2475 STORE 1
      2476 SUB 6
      2477 BRANCH TO 105 IF #3 LSD=0
      2501 ADD 6
      2502 ADD 6
```

4-2.4 MACRO ROM LISTING - $2000-2777_8$ (Cont.)

```
105 2503 LOAD 6
    2504 RIGHT 0
    2505 GOSUB DIVIDE
    2506 RIGHT 2
    2507 LOAD 2
    2510 STORE 6
    2511 RIGHT 0
    2512 STORE 1
    2513 GOSUB MULTIPLY
    2514 STORE 5
    2515 00 TO 2
    2517 0000005602251560 TO 1 K2
    2530 0012177973108490 TO 4 K3
    2541 ADD 2
    2542 LOAD 2
    2543 SUB 4
    2544 LOAD 4
    2545 GOSUB DIVIDE
    2546 0000085653537509 TO 1 K4
    2557 0019321320820340 TO 4 K5
    2570 LOAD 5
    2571 ADD 2
    2572 LOAD 2
    2573 SUB 4
    2574 LOAD 4
    2575 GOSUB DIVIDE
    2576 0005764564997278 TO 1 K6
    2607 0055321132055330 TO 4 K7
    2620 LOAD 5
    2621 ADD 2
    2622 LOAD 2
    2623 SUB 4
    2624 LOAD 4
    2625 GOSUB DIVIDE
    2626 0009886610332195 TO 1 K8
    2637 0227344418844059 TO 4 K9
    2650 LOAD 5
    2651 ADD 2
    2652 LOAD 2
    2653 SUB 4
    2654 LOAD 4
    2655 GOSUB DIVIDE
    2656 STORE 1
    2657 LOAD 6
    2660 GOSUB MULTIPLY
    2661 RIGHT 0
    2662 STORE 6
    2663 12 TO 0
106 2665 -DEL 0
    2666 LEFT 7
    2667 BRANCH TO 106 IF #0 ENTIRE≠0
    2671 LOAD 6
```

4-2.4 MACRO ROM LISTING 2000-2777$_8$ (Cont.)

```
      2672 ADD 7
      2673 LOAD 3
      2674 RIGHT 0
      2675 BRANCH TO 107 IF #0 LSD≠0
      2677 0230258509299405 TO 1
      2710 LOAD 7
      2711 GOSUB MULTIPLY
      2712 LEFT 0
      2713 STORE 7
  107 2714 LOAD 13
      2715 STORE 5
      2716 10 TO 1
      2720 LEFT 1
      2721 +DEL 1
      2722 LOAD 7
      2723 GOSUB PACK
      2724 BRANCH TO 108 IF #5 LSD≠0
      2726 GOTO 249

  108 2730 GOTO 146
  274 2732 03 TO 6
      2734 GOTO  1

      2736   2736        LOAD 1          101
      2737      7        STORE 12        152
      2740   2740        LOAD 4          104
      2741      1        RIGHT 1         021
      2742      2        ADD 1           061
      2743      3        RIGHT 3         023
      2744      4        BRANCH IF
      2745               3L=0            333
      2746      5        2750            350
      2747      6        SUB 1           071
      2750      7        SUB 1           071
      2751   2750        LOAD 2          102
      2752      1        LEFT 3          033
      2753      2        LOAD 3          103
      2754      3        STORE 4         144
      2755      4        LOAD 12         112
      2756      5        STORE 3         143
      2757      6        LOAD 2          102
      2760      7        GOSUB PACK      012
      2761
      2762
      2763
      2764          2773
      2765     94 2774 GOTO 347
      2766
      2767     95 2776 GOTO 348
      2770
      2771      ?
      2772  3000,3777
```

4-2.4 MACRO ROM LISTING - $3000\text{-}3777_8$

```
116 3000 GOSUB UNPACK
    3001 STORE 6
    3002 LEFT 6
    3003 LOAD 7
    3004 RIGHT 0
    3005 LEFT 0
    3006 SUB 7
    3007 10 TO 0
    3011 BRANCH TO 117 IF #1 LSD=0
    3013 ADD 7
117 3014 RIGHT 1
    3015 LEFT 0
    3016 SUB 1
118 3017 LEFT 0
    3020 BRANCH TO 118 IF #0 MSD=0
    3022 BRANCH TO 120 IF #1 MSD=0
119 3024 RIGHT 6
    3025 +DEL 1
    3026 BRANCH TO 119 IF #1 MSD≠0
    3030 BRANCH TO 127 IF #7 LSD=0
    3032 GOTO 121
-------------------------------------------------
120 3034 BRANCH TO 122 IF #7 LSD=0
    3036 BRANCH TO 115 IF #1 ENTIRE≠0
    3040 SUB 6
    3041 BRANCH TO 115 IF #6 ENTIRE≠0
    3043 ADD 6
121 3044 STORE 1
    3045 STORE 2
    3046 LOAD 6
    3047 SUB 1
    3050 ADD 2
    3051 LOAD 2
    3052 RIGHT 0
    3053 GOSUB MULTIPLY
    3054 LEFT 0
    3055 STORE 5
    3056 ADD 5
    3057 GOSUB SQUARE ROOT
    3060 BRANCH TO 123 IF #5 MSD=0
    3062 STORE 2
    3063 LOAD 6
    3064 STORE 1
    3065 LOAD 2
    3066 GOTO 125
-------------------------------------------------
122 3070 RIGHT 0
    3071 -DEL 1
    3072 BRANCH TO 122 IF #1 MSD=0
    3074 RIGHT 6
    3075 STORE 1
    3076 GOTO 124
```

4-2.4 MACRO ROM LISTING - $3000-3777_8$ (Cont.)

```
123 3100 STORE 1
124 3101 LOAD 6
    3102 20 TO 3
125 3104 GOSUB DIVIDE
    3105 STORE 6
    3106 BRANCH TO 126 IF #7 LSD=0
    3110 -DEL 7
126 3111 LOAD 3
    3112 ADD 7
349 3113 LEFT 7
    3114 LOAD 6
    3115 STORE 2
    3116 41 TO 0
128 3120 LEFT 0
    3121 BRANCH TO 128 IF #0 MSD=0
    3123 RIGHT 0
    3124 SUB 2
    3125 BRANCH TO 129 IF #2 MSD≠0
    3127 LEFT 0
    3130 LEFT 0
    3131 ADD 6
    3132 STORE 1
    3133 ADD 1
    3134 LOAD 6
    3135 SUB 1
    3136 RIGHT 1
    3137 RIGHT 0
    3140 GOSUB DIVIDE
    3141 +DEL 7
    3142 STORE 6
129 3143 LOAD 6
    3144 STORE 1
    3145 GOSUB MULTIPLY
    3146 RIGHT 0
    3147 STORE 2
    3150 STORE 5
    3151 STORE 4
    3152 0001505853445310 TO 0   K1
    3163 STORE 1
    3164 0133876118020924 TO 0   K2
    3175 ADD 2
    3176 LOAD 2
    3177 GOSUB DIVIDE
    3200 SUB 4
    3201 0271829879170988 TO 0   K3
    3212 ADD 4
    3213 0039283531665912 TO 0   K4
    3224 STORE 1
    3225 LOAD 4
    3226 GOSUB DIVIDE
    3227 SUB 5
    3230 0540624728151244 TO 0   K5
```

4-2.4 MACRO ROM LISTING - $3000-3777_8$ (Cont.)

```
      3241 ADD 5
      3242 0311385873583304 TO 0    K6
      3253 STORE 1
      3254 LOAD 5
      3255 GOSUB DIVIDE
      3256 0201311612554281 TO 0    K7
      3267 ADD 2
      3270 LOAD 2
      3271 STORE 1
      3272 LOAD 6
      3273 GOSUB MULTIPLY
      3274 0785398163397448 TO 0    K8
      3305 STORE 6
      3306 STORE 2
      3307 BRANCH TO 130 IF #7 LSD=0
      3311 SUB 1
      3312 LOAD 1
      3313 00 TO 1
      3315 SUB 1
130   3316 RIGHT 7
      3317 LOAD 7
      3320 RIGHT 0
      3321 RIGHT 0
      3322 BRANCH TO 137 IF #0 ENTIRE=0
      3324 LOAD 1
      3325 BRANCH TO 131 IF #7 LSD=0
      3327 RIGHT 7
      3330 BRANCH TO 132 IF #7 LSD=0
      3332 GOTO 133

131   3334 RIGHT 7
      3335 BRANCH TO 133 IF #7 LSD=0
132   3337 ADD 2
      3340 GOTO 134

133   3342 SUB 2
      3343 BRANCH TO 134 IF #2 MSD=0
      3345 00 TO 2
134   3347 LOAD 6
      3350 ADD 6
      3351 LOAD 6
      3352 BRANCH TO 135 IF #7 LSD=0
      3354 ADD 2
135   3355 RIGHT 7
      3356 00 TO 3
      3360 BRANCH TO 136 IF #7 LSD=0
      3362 +DEL 3
136   3363 LOAD 2
      3364 STORE 1
      3365 GOTO 142
```

4-2.4 MACRO ROM LISTING - $3000-3777_8$ (Cont.)

```
137 3367 LOAD 6
    3370 ADD 6
    3371 20 TO 0
    3373 SUB 7
    3374 BRANCH TO 138 IF #7 MSD≠0
    3376 SUB 7
    3377 LOAD 6
    3400 SUB 1
    3401 LOAD 1
    3402 00 TO 1
    3404 SUB 1
138 3405 10 TO 0
    3407 00 TO 3
    3411 ADD 7
    3412 BRANCH TO 139 IF #7 MSD≠0
    3414 +DEL 3
139 3415 BRANCH TO 141 IF #7 LSD=0
    3417 BRANCH TO 140 IF #3 LSD≠0
    3421 LOAD 1
    3422 00 TO 1
    3424 SUB 1
140 3425 00 TO 3
    3427 LOAD 6
    3430 ADD 1
141 3431 LOAD 1
    3432 STORE 2
142 3433 SKIP IF 1 IN FLIP FLOP #4
    3434 GOTO 143

    3436 LOAD 6
    3437 RIGHT 1
    3440 RIGHT 0
    3441 GOSUB DIVIDE
    3442 RIGHT 0
    3443 SUB 2
143 3444 99 TO 1
    3446 SKIP IF 1 IN FLIP FLOP #4
    3447 GOTO 144

    3451 +DEL 1
    3452 +DEL 1
144 3453 LOAD 2
    3454 GOTO 169

115 3456 04 TO 6
    3460 GOTO 1

350 3462 01 TO 4
    3464 BRANCH TO 147 IF #0 ENTIRE≠0
    3466 05 TO 6
    3470 GOTO 1
```

4-2.4 MACRO ROM LISTING - $3000\text{-}3777_8$ (Cont.)

```
 351 3472 00 TO 4
     3474 STORE 7
     3475 LOAD 10
     3476 STORE 2
     3477 GOTO  50

 352 3501 00 TO 4
 147 3503 STORE 7
     3504 LOAD 10
     3505 STORE 2
     3506 00 TO 0
     3510 SKIP IF 1 IN FLIP FLOP #5
     3511 01 TO 0
     3513 STORE 10
 353 3514 LOAD 7
     3515 00 TO 3
     3517 GOSUB UNPACK
     3520 BRANCH TO 148 IF #1 LSD=0
     3522 +DEL 3
 148 3523 STORE 7
     3524 RIGHT 1
     3525 99 TO 0
     3527 SUB 1
     3530 LOAD 1
     3531 STORE 5
     3532 LOAD 2
     3533 GOSUB UNPACK
     3534 BRANCH TO 149 IF #1 LSD=0
     3536 BRANCH TO 154 IF #3 LSD=0
     3540 -DEL 3
 149 3541 STORE 6
     3542 LOAD 5
     3543 RIGHT 1
     3544 BRANCH TO 150 IF #4 ENTIRE≠0
     3546 ADD 1
     3547 ADD 1
 150 3550 SUB 1
     3551 LOAD 1
     3552 STORE 5
     3553 LOAD 6
     3554 STORE 1
     3555 LOAD 7
     3556 BRANCH TO 153 IF #4 ENTIRE=0
     3560 GOSUB DIVIDE
 151 3561 LOAD 5
     3562 STORE 1
     3563 LOAD 13
     3564 STORE 5
     3565 LOAD 2
     3566 GOSUB PACK
     3567 BRANCH TO 152 IF #5 LSD=0
```

4-2.4 MACRO ROM LISTING - 3000-3777$_8$ (Cont.)

```
     3571 -DEL 5
     3572 BRANCH TO 222 IF #5 LSD=0
     3574 GOTO 220

222  3576 GOTO  32

152  3600 GOTO 249

153  3602 GOSUB MULTIPLY
     3603 STORE 2
     3604 GOTO 151

154  3606 +DEL 3
     3607 GOTO 149

354  3611 GOSUB UNPACK
     3612 STORE 3
     3613 RIGHT 1
     3614 10 TO 0
     3616 LEFT 0
     3617 STORE 4
     3620 SUB 1
     3621 BRANCH TO 241 IF #1 MSD≠0
     3623 BRANCH TO 155 IF #1 ENTIRE=0
     3625 LEFT 3
     3626 -DEL 1
155  3627 BRANCH TO 275 IF #1 ENTIRE≠0
242  3631 12 TO 2
156  3633 RIGHT 3
     3634 -DEL 2
     3635 +DEL 4
     3636 BRANCH TO 156 IF #2 MSD=0
     3640 05 TO 0
     3642 ADD 3
     3643 RIGHT 3
     3644 BRANCH TO 247 IF #3 ENTIRE≠0
     3646 +DEL 3
247  3647 LOAD 3
     3650 STORE 1
157  3651 BRANCH TO 158 IF #1 MSD=0
     3653 RIGHT 1
     3654 +DEL 4
158  3655 LOAD 1
     3656 LEFT 0
     3657 BRANCH TO 74 IF #0 MSD=0
     3661 RIGHT 1
     3662 +DEL 4
 74  3663 -DEL 3
     3664 BRANCH TO 162 IF #3 ENTIRE=0
     3666 LOAD 3
     3667 STORE 2
     3670 LOAD 1
     3671 SUB 1
```

4-2.4 MACRO ROM LISTING - 3000-3777$_8$ (Cont.)

```
159 3672 BRANCH TO 160 IF #2 LSD=0
161 3674 -DEL 2
    3675 ADD 1
    3676 GOTO 159

160 3700 BRANCH TO 157 IF #2 ENTIRE=0
    3702 LEFT 0
    3703 RIGHT 2
    3704 GOTO 161

241 3706 RIGHT 3
    3707 GOTO 242

162 3711 LOAD 1
    3712 STORE 2
    3713 LOAD 4
    3714 STORE 1
    3715 LOAD 2
    3716 +DEL 1
    3717 GOTO 169

275 3721 06 TO 6
    3723 GOTO  1

    3725                          3747
    3726                          3750
    3727                          3751
    3730                          3752
    3731                          3753
    3732                          3754
    3733                          3755
    3734                          3756
    3735                          3757
    3736                          3760
    3737                          3761
    3740                          3762
    3741                          3763
    3742                      127 3764 GOTO 349
    3743
    3744                      145 3766 GOTO 350
    3745
    3746                       57 3770 GOTO 351

                              146 3772 GOTO 352

                               50 3774 GOTO 353

                              218 3776 GOTO 354
```

?

4-2.4 MACRO ROM LISTING - $4000-4777_8$

```
   1 4000 GOSUB PRINT START
277  4001 GOSUB PRINT
     4002 BRANCH TO 277 IF #6 ENTIRE≠0
     4004 04 TO 0
     4006 STORE 3
     4007 OUTPUT (44)  R
     4010 +DEL 0
     4011 01 TO 3
     4013 OUTPUT (51)  O
     4014 -DEL 0
     4015 STORE 3
     4016 OUTPUT (44)  R
     4017 OUTPUT (44)  R
     4020 +DEL 0
     4021 -DEL 3
     4022 OUTPUT (53)  E
     4023 -DEL 3
     4024 LOAD 3
     4025 OUTPUT (22)  C.R.
     4026 RIGHT 0      0→R0
     4027 STORE 10     0→R11
     4030 -DEL 3       1→R3
     4031 OUTPUT (01)  RESET  Y5
     4032 GOTO 17

 355 4034 STORE 13
     4035 01 TO 0
     4037 STORE 12
     4040 GOTO 263

 356 4042 SKIP IF 1 IN FLIP FLOP #5
     4043 GOTO 272      4050

     4045 SKIP IF 1 IN FLIP FLOP #6
     4046 GOTO 17

 272 4050 STORE 13
     4051 LOAD 12
     4052 -DEL 0
     4053 BRANCH TO 273 IF #0 ENTIRE=0
     4055 GOSUB PRINT START
     4056 LOAD 12
     4057 GOTO 255 / 4752   GOTO 378  4067

 357 4061 STORE 13
 273 4062 01 TO 0
     4064 STORE 12
     4065 GOSUB PRINT START
     4066 LOAD 13
358  4067 STORE 5
     4070 GOSUB UNPACK
```

4-2.4 MACRO ROM LISTING - $4000-4777_8$ (Cont.)

```
     4071 LOAD 1
     4072 STORE 7
     4073 RIGHT 1
     4074 LOAD 11
     4075 STORE 3
     4076 RIGHT 0
     4077 LEFT 0
     4100 SUB 3
     4101 LOAD 3
     4102 STORE 4
     4103 ADD 1
     4104 10 TO 0
     4106 LEFT 0
     4107 SUB 1
     4110 15 TO 0
     4112 SUB 1
     4113 LOAD 1
     4114 STORE 2
     4115 -DEL 3
     4116 BRANCH TO 253 IF #3 ENTIRE≠0
     4120 +DEL 2
253  4121 06 TO 0
     4123 SUB 4
     4124 BRANCH TO 254 IF #4 MSD=0
     4126 +DEL 2
254  4127 LOAD 5
     4130 BRANCH TO 265 IF #2 MSD=0
     4132 LEFT 6
256  4133 +DEL 1
     4134 BRANCH TO 257 IF #1 MSD=0
     4136 RIGHT 6
     4137 BRANCH TO 256 IF #6 ENTIRE≠0
257  4141 LOAD 11
     4142 STORE 5
     4143 RIGHT 0
     4144 LEFT 0
     4145 SUB 5
     4146 05 TO 0
     4150 ADD 6
     4151 RIGHT 6
     4152 BRANCH TO 264 IF #5 ENTIRE=0
259  4154 -DEL 5
     4155 GOSUB PRINT
     4156 BRANCH TO 259 IF #5 ENTIRE≠0
     4160 06 TO 0
     4162 05 TO 3
     4164 OUTPUT
258  4165 02 TO 5
261  4167 BRANCH TO 260 IF #6 ENTIRE=0
     4171 BRANCH TO 262 IF #5 MSD≠0
     4173 -DEL 5
     4174 GOSUB PRINT
     4175 GOTO 261
```

4-2.4 **MACRO** ROM LISTING - $4000-4777_8$ (Cont.)

```
262 4177 04 TO 0
    4201 00 TO 3
    4203 OUTPUT
    4204 GOTO 258

268 4206 +DEL 7
    4207 RIGHT 6
267 4210 RIGHT 6
    4211 RIGHT 6
    4212 RIGHT 6
    4213 LOAD 6
    4214 STORE 5
    4215 10 TO 0
    4217 LEFT 0
    4220 SUB 7
    4221 BRANCH TO 269 IF #7 MSD=0
    4223 LOAD 7
    4224 SUB 7
    4225 SUB 7
    4226 +DEL 1
269 4227 LOAD 7
    4230 STORE 6
    4231 LOAD 1
    4232 STORE 7
    4233 GOSUB PRINT
    4234 GOSUB PRINT
    4235 06 TO 0
    4237 04 TO 3
    4241 BRANCH TO 270 IF #7 LSD=0
    4243 -DEL 3
270 4244 RIGHT 7
    4245 OUTPUT
    4246 05 TO 0
    4250 03 TO 3
    4252 OUTPUT
    4253 -DEL 0
    4254 00 TO 3
    4256 OUTPUT
    4257 LOAD 5
    4260 STORE 6
    4261 10 TO 5
271 4263 -DEL 5
    4264 GOSUB PRINT
    4265 BRANCH TO 271 IF #5 MSD=0
    4267 06 TO 0
    4271 05 TO 3
    4273 OUTPUT
    4274 GOSUB PRINT
260 4275 BRANCH TO 263 IF #7 LSD=0
    4277 06 TO 0
    4301 03 TO 3
```

4-2.4 MACRO ROM LISTING - $4000-4777_8$ (Cont.)

```
 18 4303 OUTPUT
263 4304 02 TO 0
    4306 STORE 3
    4307 OUTPUT
    4310 LOAD 12
    4311 BRANCH TO 273 IF #0 MSD≠0
    4313 BRANCH TO 273 IF #0 ENTIRE=0
    4315 -DEL 0
    4316 BRANCH TO 184 IF #0 ENTIRE=0
    4320 STORE 7
    4321 RIGHT 0
    4322 RIGHT 0
    4323 STORE 5
    4324 STORE 6
    4325 LEFT 0
    4326 LEFT 0
    4327 SUB 7
    4330 -DEL 7
    4331 01 TO 0
    4333 STORE 12
    4334 GOTO 384
184 4336 LOAD 11
    4337 STORE 1
    4340 RIGHT 0
    4341 STORE 2
    4342 LEFT 0
    4343 SUB 1
    4344 LOAD 1
    4345 STORE 11
    4346 -DEL 2
    4347 LOAD 13
    4350 BRANCH TO 185 IF #2 MSD≠0
    4352 BRANCH TO 186 IF #2 LSD=0
    4354 GOTO 198

186 4356 GOTO 219

359 4360 20 TO 5
    4362 GOTO 183

360 4364 10 TO 5
183 4366 STORE 13
    4367 LOAD 11
    4370 ADD 5
    4371 LOAD 5
    4372 STORE 11
    4373 LOAD 12
    4374 STORE 5
    4375 01 TO 0
    4377 STORE 12
    4400 LOAD 5
```

4-2.4 MACRO ROM LISTING - $4000-4777_8$ (Cont.)

```
     4401 -DEL 5
     4402 BRANCH TO 184 IF #5 ENTIRE=0
     4404 SKIP IF 1 IN FLIP FLOP #5
     4405 GOTO 224

     4407 SKIP IF 1 IN FLIP FLOP #6
     4410 GOTO 184

224  4412 STORE 1
     4413 GOSUB PRINT START
     4414 LOAD 1
     4415 GOTO 255

264  4417 BRANCH TO 258 IF #6 ENTIRE≠0
266  4421 07 TO 0
     4423 STORE 3
     4424 GOTO  18
361  4426 STORE 13
     4427 01 TO 0
     4431 STORE 12
     4432 GOSUB PRINT START
     4433 LOAD 13
265  4434 BRANCH TO 266 IF #0 ENTIRE=0
     4436 GOSUB UNPACK
     4437 LOAD 1
     4440 LEFT 1
     4441 RIGHT 0
     4442 STORE 4
     4443 STORE 7
     4444 50 TO 0
     4446 LEFT 0
     4447 ADD 6
     4450 BRANCH TO 267 IF #6 MSD=0
     4452 +DEL 4
     4453 RIGHT 4
     4454 RIGHT 4
     4455 -DEL 4
     4456 -DEL 4
     4457 BRANCH TO 268 IF #4 MSD≠0
     4461 SUB 6
     4462 GOTO 267
     4571 STORE 7
     4572 GOSUB UNPACK
     4573 01 TO 0
     4575 BRANCH TO 237 IF #1 LSD=0
     4577 +DEL 0
237  4600 STORE 13
     4601 LOAD 7
     4602 HALT
```

4-2.4 MACRO ROM LISTING - $4000\text{-}4777_8$ (Cont.)

```
365 4603 SKIP IF 1 IN FLIP FLOP #5
    4604 GOTO 239

    4606 STORE 1
    4607 03 TO 0
    4611 SKIP IF 1 IN FLIP FLOP #7
    4612 04 TO 0
    4614 STORE 13
    4615 00 TO 0
    4617 03 TO 3
    4621 GOTO 303

366 4623 STORE 7
    4624 02 TO 0
    4626 GOTO 237 / 4600

239 4630 09 TO 6
    4632 GOTO  1

367 4634 STORE 1
    4635 00 TO 0
    4637 01 TO 3
    4641 OUTPUT
    4642 +DEL 3
    4643 OUTPUT
    4644 RIGHT 3
    4645 LOAD 1
    4646 HALT

219 4647 STORE 12
    4650 00 TO 4
    4652 03 TO 0
    4654 STORE 13
    4655 LOAD 12
    4656 GOTO 214

368 4660 -DEL 5
    4661 BRANCH TO 221 IF #5 LSD=0
    4663 STORE 1
    4664 LOAD 12
    4665 STORE 2
    4666 LOAD 1
    4667 STORE 12
    4670 02 TO 0
    4672 STORE 13
    4673 00 TO 4
    4675 LOAD 2
    4676 GOTO 215
```

4-2.4 MACRO ROM LISTING 4000-4777$_8$ (Cont.)

```
221 4700 STORE 10
    4701 LOAD 12
    4702 STORE 1
    4703 LOAD 10
    4704 STORE 12
    4705 LOAD 1
279 4706 GOTO 249
    4711 12 TO 0 / 4725
    4713 SUB 6
    4714 BRANCH TO 379 IF #6 ENTIRE=0
    4716 STORE 6
    4717 STORE 7
    4720 LOAD 10
    4721 STORE 2
    4722 LOAD 1
    4723 STORE 10
    4724 HALT
-------------------------------------
379 4725 LOAD 2
    4726 GOTO 249 / 4746
    4730
    4731
    4732
    4733
    4734
    4735
    4736
    4737
    4740
    4741
190 4742 GOTO 380 / 4710
246 4744 GOTO 355 / 4034
249 4746 GOTO 356 / 4042
244 4750 GOTO 357 / 4061
255 4752 GOTO 358 / 4067
182 4754 GOTO 359 / 4360
180 4756 GOTO 360 / 4364
245 4760 GOTO 361 / 4426
225 4762 GOTO 362 / 4477
335 4764 GOTO 363 / 4514
236 4766 GOTO 364 / 4566
232 4770 GOTO 365 / 4603
238 4772 GOTO 366 / 4623
240 4774 GOTO 367 / 4634
220 4776 GOTO 368 / 4660
    ?
```

4-2.4 MACRO ROM LISTING - $5000-5777_8$

```
5001 +DEL 4
5002 +DEL 4
5003 +DEL 4
5004 +DEL 4
5005 +DEL 4
5006 +DEL 4
5007 +DEL 4
5010 +DEL 4
5011 +DEL 4
5012 +DEL 4
5013 +DEL 4
5014 +DEL 4
5015 +DEL 4
5016 +DEL 4
5017 +DEL 4
5020 +DEL 4
5021 +DEL 4
5022 +DEL 4
5023 +DEL 4
5024 +DEL 4
5025 +DEL 4
5026 +DEL 4
5027 +DEL 4
5030 +DEL 4
5031 +DEL 4
5032 +DEL 4
5033 +DEL 4
5034 +DEL 4
5035 +DEL 4
5036 +DEL 4
5037 +DEL 4
5040 +DEL 4
5041 +DEL 4
5042 +DEL 4
5043 +DEL 4
5044 +DEL 4
5045 +DEL 4
5046 +DEL 4
5047 +DEL 4
5050 +DEL 4
5051 +DEL 4
5052 +DEL 4
5053 +DEL 4
5054 +DEL 4
5055 +DEL 4
5056 +DEL 4
5057 +DEL 4
5060 +DEL 4
5061 +DEL 4
5062 +DEL 4
5063 +DEL 4
5064 +DEL 4
```

4-2.4 MACRO ROM LISTING - 5000-5777$_8$ (Cont.)

```
     5065 +DEL 4
     5066 +DEL 4
     5067 +DEL 4
     5070 +DEL 4
     5071 +DEL 4
     5072 +DEL 4
     5073 +DEL 4
     5074 +DEL 4
     5075 +DEL 4
     5076 +DEL 4
     5077 SKIP IF 1 IN FLIP FLOP #5
     5100 GOTO 400
     5102 LOAD 10
     5103 -DEL 0
     5104 BRANCH TO 402 IF #0 ENTIRE=0
     5106 -DEL 0
     5107 BRANCH TO 403 IF #0 ENTIRE=0
     5111 -DEL 0
     5112 BRANCH TO 404 IF #0 ENTIRE=0
     5114 BRANCH TO 281 IF #4 ENTIRE=0
     5116 55 TO 7
     5120 LOAD 4
     5121 ADD 4
     5122 ADD 4
     5123 ADD 4
     5124 ADD 4
     5125 LOAD 4
     5126 RIGHT 0
     5127 SUB 7
     5130 BRANCH TO 293 IF #4 LSD=0
     5132 32 TO 0
     5134 SUB 7
293  5135 LOAD 7
     5136 STORE 2
     5137 STORE 4
     5140 BRANCH TO 307 IF #7 MSD≠0
     5142 RIGHT 0
     5143 BRANCH TO 291 IF #0 ENTIRE=0
     5145 48 TO 0
     5147 SUB 4
     5150 BRANCH TO 296 IF #4 MSD≠0
     5152 -DEL 4
     5153 -DEL 4
     5154 BRANCH TO 301 IF #4 ENTIRE=0
     5156 RIGHT 0
     5157 SUB 4
     5160 BRANCH TO 307 IF #4 ENTIRE≠0
     5162 48 TO 7
     5164 GOTO 297
```

4-2.4 MACRO ROM LISTING - $5000\text{-}5777_8$ (Cont.)

```
400 5166 44 TO 0
    5170 SUB 4
    5171 BRANCH TO 401 IF #4 ENTIRE≠0
    5173 03 TO 0
    5175 STORE 10
    5176 RIGHT 0
    5177 05 TO 3
    5201 OUTPUT
401 5202 00 TO 0
    5204 STORE 4
    5205 STORE 3
    5206 HALT

404 5207 BRANCH TO 401 IF #4 ENTIRE≠0
    5211 02 TO 0
    5213 STORE 10
    5214 GOTO 401

403 5216 BRANCH TO 401 IF #4 ENTIRE=0
    5220 01 TO 0
    5222 STORE 10
    5223 STORE 6
402 5224 BRANCH TO 405 IF #4 ENTIRE=0
    5226 LOAD 4
    5227 ADD 6
    5230 GOTO 401
405 5232 LOAD 4
    5233 01 TO 3
    5235 OUTPUT
    5236 GOSUB PRINT START
    5237 GOSUB PRINT
    5240 GOSUB PRINT
    5241 GOSUB PRINT
    5242 06 TO 0
    5244 04 TO 3
    5246 OUTPUT
    5247 OUTPUT
    5250 02 TO 0
    5252 OUTPUT
    5253 RIGHT 0
    5254 STORE 10
    5255 GOTO 17

296 5257 15 TO 0
    5261 SUB 2
    5262 BRANCH TO 301 IF #2 MSD≠0
    5264 BRANCH TO 406 IF #2 ENTIRE=0
    5266 -DEL 2
    5267 -DEL 2
    5270 -DEL 2
    5271 BRANCH TO 297 IF #2 MSD≠0
```

4-2.4 MACRO ROM LISTING - $5000\text{-}5777_8$ (Cont.)

```
      5273 27 TO 0
      5275 SUB 2
      5276 BRANCH TO 297 IF #2 ENTIRE=0
      5300 -DEL 2
      5301 BRANCH TO 297 IF #2 ENTIRE=0
      5303 GOTO 301

 406  5305 15 TO 1
      5307 LOAD 10
      5310 SUB 1
      5311 BRANCH TO 297 IF #1 ENTIRE≠0
      5313 00 TO 6
      5315 51 TO 7
      5317 GOTO 282

 291  5321 +DEL 5
 297  5322 +DEL 5
 301  5323 +DEL 5
 295  5324 LOAD 3
      5325 ADD 5
 312  5326 BRANCH TO 292 IF #5 ENTIRE=0
      5330 -DEL 5
      5331 BRANCH TO 316 IF #5 ENTIRE=0
      5333 -DEL 5
      5334 BRANCH TO 314 IF #5 ENTIRE=0
      5336 -DEL 5
      5337 BRANCH TO 294 IF #5 ENTIRE=0
      5341 04 TO 0
      5343 SUB 5
      5344 BRANCH TO 326 IF #5 MSD≠0
      5346 BRANCH TO 308 IF #5 ENTIRE=0
      5350 SUB 5
      5351 BRANCH TO 307 IF #5 MSD≠0
      5353 BRANCH TO 309 IF #5 ENTIRE=0
      5355 -DEL 5
      5356 BRANCH TO 310 IF #5 ENTIRE=0
      5360 02 TO 0
      5362 OUTPUT
      5363 OUTPUT
      5364 GOSUB PRINT START
      5365 -DEL 6
 311  5366 GOSUB PRINT
      5367 BRANCH TO 311 IF #6 ENTIRE≠0
      5371 04 TO 0
      5373 05 TO 3
      5375 OUTPUT
      5376 02 TO 0
      5400 OUTPUT
      5401 OUTPUT
      5402 OUTPUT
      5403 GOTO 312
```

4-2.4 MACRO ROM LISTING - $5000\text{-}5777_8$ (Cont.)

```
 326 5405 LOAD 5
     5406 ADD 7
     5407 48 TO 0
     5411 SUB 7
     5412 BRANCH TO 307 IF #7 ENTIRE≠0
     5414 LOAD 10
     5415 STORE 7
     5416 99 TO 6
     5420 LEFT 6
     5421 GOTO 282

 314 5423 GOTO 305

 369 5425 1111111111177796 TO 0
     5436 STORE 12
     5437 6626675836517882 TO 3
     5450 8562837372731637 TO 1
     5461 3627273165746477 TO 4
     5472 7517466786772626 TO 2
     5503 5777817466786772 TO 5
     5514 1626262747973721 TO 0
 370 5525 +DEL 7
 283 5526 -DEL 0
     5527 BRANCH TO 284 IF #0 LSD=0
     5531 BRANCH TO 287 IF #7 ENTIRE≠0
     5533 BRANCH TO 286 IF #3 LSD≠0
     5535 STORE 3
 287 5536 RIGHT 0
     5537 BRANCH TO 283 IF #0 ENTIRE≠0
     5541 LOAD 5
     5542 STORE 13
     5543 LOAD 2
     5544 STORE 5
     5545 LOAD 4
     5546 STORE 2
     5547 LOAD 1
     5550 STORE 4
     5551 LOAD 3
     5552 STORE 1
     5553 LOAD 12
     5554 BRANCH TO 317 IF #7 ENTIRE=0
     5556 STORE 3
 317 5557 LOAD 13
     5560 GOTO 283

 281 5562 LOAD 13
     5563 BRANCH TO 295 IF #0 LSD≠0
     5565 HALT
```

4-2.4 MACRO ROM LISTING - 5000-5777$_8$ (Cont.)

```
286 5566 -DEL 3
    5567 -DEL 0
    5570 OUTPUT
302 5571 LEFT 3
    5572 GOTO.287

284 5574 -DEL.7
    5575 BRANCH TO 288 IF #7 MSD≠0
    5577 BRANCH TO 287 IF #7 ENTIRE≠0
    5601 STORE 7
    5602 LOAD 2
    5603 STORE 10
    5604 GOSUB PRINT START
    5605 BRANCH TO 285 IF #6 ENTIRE≠0
    5607 OUTPUT
    5610 OUTPUT
289 5611 LOAD 10
    5612 STORE 2
    5613 LOAD 7
    5614 SUB 7
    5615 GOTO 302

285 5617 -DEL 6
    5620 LOAD 6
    5621 RIGHT 0
    5622 RIGHT 0
    5623 BRANCH TO 327 IF #0 ENTIRE≠0
    5625 GOSUB PRINT
    5626 GOSUB PRINT
    5627 GOTO 289

327 5631 04 TO 0
    5633 05 TO 3
    5635 OUTPUT
    5636 RIGHT 3
    5637 OUTPUT
    5640 GOTO 289

294 5642 LOAD 7
    5643 STORE 6
    5644 GOSUB PRINT START
    5645 OUTPUT
    5646 OUTPUT
    5647 GOSUB PRINT
288 5650 02 TO 0
    5652 OUTPUT
    5653 -DEL 0
    5654 STORE 13
    5655 -DEL 0
    5656 STORE 1
    5657 STORE 10
```

4-2.4 MACRO ROM LISTING - $5000-5777_8$ (Cont.)

```
      5660 SKIP IF 1 IN FLIP FLOP #6
      5661 GOTO 318

      5663 01 TO 3
      5665 OUTPUT
      5666 +DEL 3
      5667 OUTPUT
      5670 GOTO 318

  292 5672 01 TO 3
      5674 00 TO 0
      5676 OUTPUT
      5677 +DEL 3
      5700 OUTPUT
      5701 12 TO 3
  310 5703 +DEL 6
  313 5704 00 TO 0
      5706 STORE 4
      5707 STORE 5
      5710 +DEL 0
      5711 STORE 13
      5712 HALT

  371 5713 04 TO 3
      5715 LOAD 7
      5716 STORE 10
      5717 GOTO 313

  307 5721 11 TO 6
      5723 GOTO   1

  308 5725 LOAD 7
      5726 STORE 6
      5727 08 TO 3
      5731 GOTO 313

  309 5733 LOAD 7
      5734 LEFT 6
      5735 ADD 6
      5736 LOAD 10
      5737 STORE 7
      5740 STORE 1
      5741 48 TO 0
      5743 SUB 1
      5744 BRANCH TO 319 IF #1 ENTIRE=0
      5746 +DEL 6
  316 5747 GOTO 282

  319 5751 GOSUB PRINT START
      5752 10 TO 2
  320 5754 OUTPUT
      5755 -DEL 2
```

4-2.4 MACRO ROM LISTING - 5000-5777$_8$ (Cont.)

```
          5756 BRANCH TO 320 IF #2 MSD=0
          5760 GOSUB PRINT
          5761 GOSUB PRINT
          5762 GOTO 288
          5764
          5765
          5766
          5767
          5770
          5771
   290    5772 GOTO 370
   306    5774 GOTO 371
   315    5776 GOTO 369
   ?
```

4-2.4 MACRO ROM LISTING - $6000-6777_8$

```
305 6000 SKIP IF 1 IN FLIP FLOP #6
    6001 GOTO 306

282 6003 10 TO 0
    6005 SUB 7
    6006 SUB 7
    6007 BRANCH TO 298 IF #7 MSD≠0
    6011 SUB 7
    6012 BRANCH TO 299 IF #7 MSD≠0
    6014 +DEL 0
    6015 SUB 7
    6016 BRANCH TO 300 IF #7 MSD≠0
    6020 07 TO 0
    6022 SUB 7
    6023 BRANCH TO 328 IF #7 MSD=0
    6025 ADD 7
    6026 GOTO 315

298 6030 ADD 7
    6031 1176626568175677 TO 0
    6042 STORE 12
    6043 2756616477776572 TO 3
    6054 7366751657273667 TO 1
    6065 5166757764797916 TO 4
    6076 4667717567726275 TO 2
    6107 7674165727374165 TO 5
    6120 7572626975771871 TO 0
    6131 GOTO 290

299 6133 ADD 7
    6134 1111117773651657 TO 0
    6145 STORE 12
    6146 8671646272736276 TO 3
    6157 1667577787416568 TO 1
    6170 6266721851727362 TO 4
    6201 7473796466178677 TO 2
    6212 2758375661737474 TO 5
    6223 6265788367174781 TO 0
    6234 GOTO 290

300 6236 ADD 7
    6237 1111166646978646 TO 0
    6250 STORE 12
    6251 7651697583667575 TO 3
    6262 6517273626675777 TO 1
    6273 2175627273627617 TO 4
    6304 6184179676275186 TO 2
    6315 1826477726679179 TO 5
    6326 7383989917264671 TO 0
    6337 GOTO 290
```

4-2.4 MACRO ROM LISTING - $6000-6777_8$ (Cont.)

```
328 6341 6738362777369751 TO 0
    6352 9786675777211746 TO 5
    6363 1175767783178676 TO 2
    6374 GOTO 290
373 6376 LOAD 13                                   R13→R0
    6377 BRANCH TO   2 IF #0 LSD=0
    6401 GOTO 225 /4762
    6403 LOAD 6                                    R6→R0
    6404 BRANCH TO   3 IF #0 LSD=0
    6406 -DEL 0
    6407 BRANCH TO  11 IF #0 LSD=0
    6411 -DEL 0
    6412 BRANCH TO  13 IF #0 LSD=0
    6414 LOAD 4
    6415 STORE 11
    6416 LOAD 1
374 6417 STORE 1
    6420 LOAD 11
    6421 STORE 2
    6422 RIGHT 0
    6423 LEFT 0
    6424 SUB 2
    6425 LOAD 2
    6426 STORE 11
    6427 RIGHT 0
    6430 SKIP IF 1 IN FLIP FLOP #6
    6431 GOTO  20

    6433 01 TO 3
    6435 OUTPUT
    6436 +DEL 3
    6437 OUTPUT
 20 6440 STORE 13
375 6441 STORE 3
    6442 STORE 4
    6443 STORE 5
    6444 STORE 6
    6445 STORE 7
    6446 STORE 2
    6447 +DEL 0
    6450 STORE 12
    6451 LOAD 1
    6452 HALT

  3 6453 BRANCH TO   4 IF #7 ENTIRE≠0
    6455 11 TO 7
    6457 LEFT 7
    6460 04 TO 0
    6462 ADD 7
    6463 LOAD 1
    6464 STORE 10
```

4-2.4 MACRO ROM LISTING - 6000-6777$_8$ (Cont.)

```
    4 6465 LOAD 4
      6466 BRANCH TO  7 IF #5 MSD≠0
      6470 -DEL 7
      6471 LEFT 5
      6472 ADD 5
    7 6473 LOAD 6
      6474 RIGHT 0
      6475 BRANCH TO  8 IF #0 LSD≠0
      6477 +DEL 7
    8 6500 LOAD 7
      6501 STORE 1
      6502 LOAD 5
  340 6503 GOSUB PACK
      6504 STORE 12
   10 6505 00 TO 4
      6507 HALT
   11 6510 LOAD 6
      6511 STORE 3
      6512 RIGHT 0
      6513 RIGHT 0
      6514 LEFT 0
      6515 LEFT 0
      6516 SUB 3
      6517 LOAD 1
      6520 GOSUB UNPACK
      6521 STORE 2
      6522 LOAD 3
      6523 STORE 6
      6524 LOAD 5          GO TO 1737
      6525 SUB 4
      6526 LEFT 0
      6527 ADD 4
      6530 LOAD 4
      6531 ADD 5
      6532 ~~RIGHT 1~~     GO TO 345
      6533 ~~ADD 1~~       2736  336
      6534 RIGHT 3
      6535 BRANCH TO  12 IF #3 LSD=0
      6537 SUB 1
      6540 SUB 1
   12 6541 LOAD 2
      6542 LEFT 3
      6543 GOTO  9         (1746)

   13 6545 LEFT 0
      6546 RIGHT 0
      6547 RIGHT 0
      6550 -DEL 0
      6551 -DEL 0
      6552 -DEL 0
      6553 BRANCH TO  14 IF #0 MSD=0
```

4-2.4 MACRO ROM LISTING - $6000\text{-}6777_8$ (Cont.)

```
      6555 LOAD 4
      6556 SUB 4
      6557 STORE 5
      6560 LEFT 5
      6561 40 TO 0
      6563 ADD 6
      6564 LOAD 1
      6565 HALT

    5 6566 BRANCH TO 391 IF #7 ENTIRE≠0
      6570 11 TO 7
      6572 LEFT 7
      6573 +DEL 7
      6574 +DEL 7
      6575 +DEL 7
      6576 +DEL 7
      6577 STORE 10
  391 6600 10 TO 6
      6602 HALT
   14 6603 STORE 7
      6604 LOAD 4
      6605 ADD 5
  376 6606 LOAD 5
      6607 LEFT 0
      6610 +DEL 0
      6611 STORE 13
      6612 LEFT 3
      6613 -DEL 7
      6614 LOAD 7
      6615 -DEL 0
      6616 -DEL 0
      6617 BRANCH TO  15 IF #0 LSD≠0
      6621 11 TO 7
   15 6623 GOTO 390

  377 6625 LOAD 14
      6626 GOSUB KEYBOARD
      6627 STORE 14
      6630 LOAD 15
      6631 GOSUB KEYBOARD
      6632 STORE 15
      6633 LOAD 16
      6634 GOSUB KEYBOARD
      6635 STORE 16
      6636 LOAD 17
      6637 GOSUB KEYBOARD
      6640 STORE 17
      6641 LOAD 20
      6642 GOSUB KEYBOARD
      6643 STORE 20
      6644 LOAD 21
```

4-2.4 MACRO ROM LISTING - $6000\text{-}6777_8$ (Cont.)

```
      6645 GOSUB KEYBOARD
      6646 STORE 21
      6647 LOAD 22
      6650 GOSUB KEYBOARD
      6651 STORE 22
      6652 LOAD 23
      6653 GOSUB KEYBOARD
      6654 STORE 23
      6655 LOAD 24
      6656 GOSUB KEYBOARD
      6657 STORE 24
      6660 LOAD 25
      6661 GOSUB KEYBOARD
      6662 STORE 25
      6663 LOAD 26
      6664 GOSUB KEYBOARD
      6665 STORE 26
      6666 LOAD 27
      6667 GOSUB KEYBOARD
      6670 STORE 27
      6671 LOAD 30
      6672 GOSUB KEYBOARD
      6673 STORE 30
      6674 LOAD 31
      6675 GOSUB KEYBOARD
      6676 STORE 31
      6677 LOAD 32
      6700 GOSUB KEYBOARD
      6701 STORE 32
      6702 LOAD 33
      6703 GOSUB KEYBOARD
      6704 STORE 33
      6705 LOAD 34
      6706 GOSUB KEYBOARD
      6707 STORE 34
      6710 LOAD 35
      6711 GOSUB KEYBOARD
      6712 STORE 35
      6713 LOAD 36
      6714 GOSUB KEYBOARD
      6715 STORE 36
      6716 LOAD 37
      6717 GOSUB KEYBOARD
      6720 STORE 37
      6721 LOAD 7
      6722 RIGHT 0
      6723 BRANCH TO 19 IF #0 LSD≠0
 378  6725 01 TO 0
      6727 STORE 12
      6730 LOAD 2
      6731 BRANCH TO 17 IF #7 ENTIRE=0
      6733 GOTO 249
```

6/15/73

4-2.4 MACRO ROM LISTING - $6000-6777_8$ (Cont.)

```
19 6735 LOAD 10
   6736 STORE 12
   6737 LOAD 1
   6740 STORE 10
   6741 00 TO 4
   6743 00 TO 6
   6745 LOAD 2
   6746 GOTO 51 /1776
   6750 LD 1
   6751 ST 12
   6752 RT 1
   6753 A=0 1
   6754 GO TO
   6755 6534
9  6756
   6757
210 6760 GOTO 5/6566
 9 6762 GOTO 340/6503
336 6764 GOTO 373/ 6376
 17 6766 GOTO 374/6417
318 6770 GOTO 375/6441
325 6772 GOTO 376 /6606
 16 6774 GOTO 377 /1625
248 6776 GOTO 378 /6725
?
```

4-2.4 MACRO ROM LISTING - $7000\text{-}7777_8$

```
      7000 STORE 6
      7001 GOSUB PRINT START
408   7002 GOSUB PRINT
      7003 BRANCH TO 408 IF #6 ENTIRE≠0
      7005 02 TO 0
      7007 OUTPUT
      7010 GOTO 17

384   7012 GOTO 372

390   7014 GOTO 385

321   7016 STORE 4
      7017 LOAD 13
      7020 BRANCH TO 329 IF #0 LSD=0
      7022 LOAD 14
      7023 GOSUB UNPACK
      7024 BRANCH TO 330 IF #1 LSD=0
      7026 ADD 6
      7027 RIGHT 1
      7030 BRANCH TO 331 IF #6 MSD=0
      7032 +DEL 1
331   7033 RIGHT 1
      7034 RIGHT 1
      7035 BRANCH TO 322 IF #1 ENTIRE≠0
      7037 LOAD 1
      7040 GOTO 333

330   7042 11 TO 0
      7044 LEFT 0
      7045 RIGHT 1
      7046 SUB 1
      7047 -DEL 1
      7050 -DEL 1
      7051 -DEL 1
332   7052 +DEL 1
      7053 RIGHT 6
      7054 BRANCH TO 332 IF #1 MSD≠0
      7056 05 TO 0
      7060 ADD 6
      7061 RIGHT 6
      7062 LOAD 6
      7063 RIGHT 0
      7064 RIGHT 0
      7065 BRANCH TO 322 IF #0 ENTIRE≠0
      7067 LOAD 6
333   7070 STORE 5
      7071 LOAD 4
      7072 STORE 1
      7073 GOTO 335
```

4-2.4 MACRO ROM LISTING - $7000-7777_8$ (Cont.)

```
329 7075 LOAD 4
    7076 STORE 13
    7077 LOAD 6
    7100 -DEL 6
    7101 -DEL 6
    7102 BRANCH TO 322 IF #6 LSD≠0
    7104 RIGHT 0
    7105 +DEL 0
    7106 STORE 7
    7107 LOAD 14
    7110 GOSUB UNPACK
    7111 BRANCH TO 322 IF #1 LSD≠0
    7113 RIGHT 1
    7114 11 TO 0
    7116 LEFT 0
    7117 +DEL 0
    7120 +DEL 0
    7121 +DEL 0
    7122 SUB 1
323 7123 RIGHT 6
    7124 +DEL 1
    7125 BRANCH TO 323 IF #1 MSD≠0
    7127 LOAD 13
    7130 STORE 1
    7131 05 TO 0
    7133 ADD 6
    7134 RIGHT 6
    7135 LOAD 6
    7136 STORE 5
    7137 BRANCH TO 322 IF #0 ENTIRE=0
    7141 RIGHT 0
    7142 -DEL 0
    7143 -DEL 0
    7144 BRANCH TO 324 IF #0 MSD≠0
322 7146 12 TO 6
    7150 GOTO 1

324 7152 32 TO 6
    7154 LOAD 7
    7155 LEFT 0
    7156 ADD 6
    7157 GOTO 325

385 7161 LOAD 1
    7162 STORE 13
    7163 SKIP IF 1 IN FLIP FLOP #5
    7164 GOTO 382

    7166 SKIP IF 1 IN FLIP FLOP #6
    7167 GOTO 383
```

4-2.4 MACRO ROM LISTING - $7000-7777_8$ (Cont.)

```
382 7171 LOAD 12
    7172 -DEL 0
    7173 BRANCH TO 396 IF #0 ENTIRE=0
    7175 LEFT 5
    7176 LEFT 5
    7177 +DEL 7
    7200 +DEL 7
    7201 LOAD 5
    7202 ADD 7
    7203 LOAD 7
    7204 STORE 12
    7205 GOSUB PRINT START
    7206 LOAD 1
    7207 GOTO 372
396 7211 LOAD 5
    7212 STORE 6
372 7213 LOAD 7
    7214 -DEL 0
    7215 BRANCH TO 383 IF #0 ENTIRE=0
    7217 GOSUB PRINT START
    7220 GOSUB PRINT
    7221 GOSUB PRINT
    7222 05 TO 0
    7224 03 TO 3
    7226 OUTPUT
    7227 -DEL 0
    7230 +DEL 3
    7231 OUTPUT
    7232 +DEL 0
    7233 01 TO 3
    7235 OUTPUT
    7236 RIGHT 3
    7237 OUTPUT
    7240 -DEL 0
    7241 03 TO 3
    7243 OUTPUT
    7244 BRANCH TO 386 IF #7 LSD=0
    7246 +DEL 0
    7247 STORE 3
    7250 OUTPUT
    7251 OUTPUT
    7252 -DEL 0
    7253 02 TO 3
    7255 OUTPUT
386 7256 02 TO 0
    7260 OUTPUT
383 7261 LOAD 13
    7262 STORE 1
    7263 STORE 2
    7264 00 TO 3
    7266 LOAD 5
```

4-2.4 MACRO ROM LISTING - 7000-7777$_8$ (Cont.)

```
      7267 LEFT 0
      7270 +DEL 0
      7271 STORE 13
      7272 GOTO  16

      7274
      7275
      7276
      7277
      7300
  387 7301 SKIP IF 1 IN FLIP FLOP #5
      7302 GOTO 243

      7304 STORE 13
      7305 00 TO 0
      7307 STORE 5
      7310 STORE 7
      7311 SKIP IF 1 IN FLIP FLOP #6
      7312 01 TO 0
      7314 STORE 12
      7315 RIGHT 0
      7316 06 TO 3
      7320 OUTPUT
      7321 RIGHT 3
      7322 LOAD 13
  392 7323 GOSUB UNPACK
      7324 BRANCH TO 393 IF #1 LSD≠0
      7326 +DEL 3
  393 7327 RIGHT 1
      7330 03 TO 0
      7332 SUB 1
      7333 11 TO 0
      7335 LEFT 0
      7336 SUB 1
  394 7337 +DEL 1
      7340 RIGHT 6
      7341 BRANCH TO 394 IF #1 MSD≠0
      7343 05 TO 0
      7345 ADD 6
      7346 RIGHT 6
      7347 LOAD 6
      7350 STORE 1
      7351 RIGHT 0
      7352 RIGHT 0
      7353 RIGHT 0
      7354 BRANCH TO 427 IF #0 ENTIRE=0
      7356 10 TO 1
      7360 LEFT 1
      7361 LEFT 1
      7362 -DEL 1
```

4-2.4 MACRO ROM LISTING - $7000-7777_8$ (Cont.)

```
      7363 BRANCH TO 428 IF #7 ENTIRE≠0
427   7365 RIGHT 0
      7366 RIGHT 0
      7367 RIGHT 0
      7370 STORE 6
      7371 BRANCH TO 395 IF #0 ENTIRE=0
      7373 RIGHT 0
      7374 BRANCH TO 388 IF #0 ENTIRE=0
      7376 BRANCH TO 429 IF #3 LSD=0
395   7400 +DEL 3
      7401 +DEL 3
429   7402 LOAD 1
      7403 +DEL 0
      7404 STORE 7
      7405 LOAD 10
      7406 GOTO 392

      7410 -DEL 7
428   7411 LOAD 7
      7412 LEFT 0
      7413 LEFT 0
      7414 LEFT 0
      7415 ADD 1
      7416 LOAD 1
      7417 STORE 6
      7420 LEFT 6
      7421 LOAD 3
      7422 STORE 5
      7423 SKIP IF 1 IN FLIP-FLOP #6
388   7424 GOTO 426

      7426 GOTO 420
      7430 -DEL 5
426   7431 BRANCH TO 421 IF #5 MSD≠0
      7433 -DEL 5
      7434 BRANCH TO 422 IF #5 MSD≠0
      7436 -DEL 5
      7437 BRANCH TO 423 IF #5 MSD≠0
      7441 -DEL 5
      7442 BRANCH TO 424 IF #5 MSD≠0
      7444 GOTO 425

389   7446 07 TO 5
397   7450 -DEL 5
      7451 BRANCH TO 398 IF #5 MSD≠0
      7453 LOAD 6
      7454 RIGHT 6
      7455 BRANCH TO 410 IF #0 LSD=0
      7457 -DEL 0
      7460 BRANCH TO 411 IF #0 LSD=0
      7462 -DEL 0
      7463 BRANCH TO 412 IF #0 LS
      7465 -DEL 0
```

4-2.4 MACRO ROM LISTING - $7000-7777_8$ (Cont.)

```
      7466 BRANCH TO 413 IF #0 LSD=0
      7470 -DEL 0
      7471 BRANCH TO 414 IF #0 LSD=0
      7473 -DEL 0
      7474 BRANCH TO 415 IF #0 LSD=0
      7476 -DEL 0
      7477 BRANCH TO 416 IF #0 LSD=0
      7501 -DEL 0
      7502 BRANCH TO 417 IF #0 LSD=0
      7504 -DEL 0
      7505 BRANCH TO 418 IF #0 LSD=0
      7507 GOTO 419
-------------------------------------------------
398   7511 LOAD 12
      7512 BRANCH TO 399 IF #0 ENTIRE=0
      7514 RIGHT 0.
      7515 05 TO 3
      7517 OUTPUT
-------------------------------------------------
399   7520 LOAD 13
      7521 GOTO  17
-------------------------------------------------

?
```

4-3.0 DEFINITIONS

1. ALGORITHM - A rule of procedure for solving a mathematical problem usually involving repetitions.

2. BINARY NUMBER SYSTEM - A number system using only the symbols "0" and "1" and having two as its base, i.e., the place values are --- 64, 32, 16, 8, 4, 2, 1, 1/2, 1/4, ---

3. BIT - A single character of a language employing exactly two distinct kinds of characters.

4. BRANCHING - Diverging from the usual sequential execution of program instructions to an instruction(s) either preceding or succeeding the one being currently executed.

   CONDITIONAL - Branching to another part of a program when a certain condition has been meet.

   UNCONDITIONAL - Branching on every and all conditions to another instruction in a program.

5. CALCULATOR - A machine for performing mathematical operations.

6. COMPUTER - An automatic electronic machine for performing calculations.

7. DECIMAL NUMBER SYSTEM - A number system using the symbols "0", "1", "2", "3", "4", "5", "6", "7", "8", "9", and having ten as its base; i.e., this place values are --- 10000, 1000, 100, 10, 1, .1, .01 ---.

8. FLOW CHART - A diagram or outline showing progress in the solution of a problem.

4-3.0 DEFINITIONS (Cont.)

9. I/O - Abbreviation for input - output to/from a computing machine.

10. LOOPING - Repeating the execution of the same series of instructions ad infinitum.

11. MACHINE LANGUAGE - A language occurring within a machine, ordinarily not perceptible or intelligible to people without special equipment or training.

12. MODE OF OPERATION - The operational state in which a calculating machine finds itself at a given point in time.

13. NON-VOLATILE MEMORY - Memory which is not destroyed by a power-down condition (under most circumstances).

14. PROGRAMMABLE CALCULATOR - A calculator in which a sequence of coded instructions may be stored and executed at will.

15. PROGRAM CODE, LABEL OR ADDRESS - A marker which points to a particular position (instruction) in a series of instructions making up a program.

16. PROGRAM DEBUGGING - The process by which a person determines if a program is executing correctly under all circumstances.

17. PROGRAM EDITING - The process by which a person deletes and/or inserts program steps or instructions to correct a program.

18. PROGRAM INSTRUCTION - One or more program steps which instructs the machine to perform an operation.

4-3.0 DEFINITIONS (Cont.)

19. PROGRAMMING LANGUAGE - A series of codes which a machine will recognize and translate into machine language.

20. PROGRAM LISTING - A listing of the program code which has been given to the calculator to translate into machine language.

21. PROGRAM STEP - The smallest coded element of the program memory.

22. RAM - (RANDOM ACCESS MEMORY) - Storage in which the next position from which information is to be obtained is in no way dependent on the previous one.

23. REGISTER - An electronic device which is capable of storing a number.

24. REGISTER STACK - Two or more registers which are thought of as a stack ; i.e., information is passed from Reg. to Reg. automatically as new information is introduced into the lowest member.

25. ROM -(READ ONLY MEMORY) - That storage from which information can only be obtained, not stored,after the initial storage.

26. SCIENTIFIC NOTATION - A system by which all numbers can be written as X.XXX ------ times a power of 10.
Ex: $172.36 = 1.7236 \cdot 10^2$

27. SIGNIFICANT DIGITS - Digits of a number that end with the last figure to the right being non-zero or a zero of an integral value.

28. STORAGE REGISTER - A register that is used only for storing a number not for performing any type of arithmetic.

4-3.0 DEFINITIONS (Cont.)

29. SUBROUTINE - A subordinate routine usually repeated several times at different points in a program. Control is transferred from a master routine to the subroutine and then back again.

30. VOLATILE MEMORY - Storage medium in which information cannot be retained without continuous power dissipation.

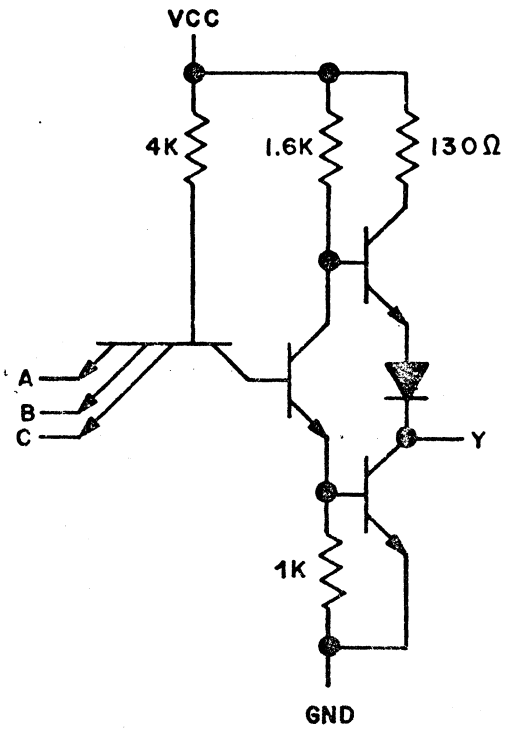
31. WORKING REGISTER - A register which can be used for performing mathematical functions. (+, -, COS, SIN, etc.).

4-4.0 INTEGRATED CIRCUITS

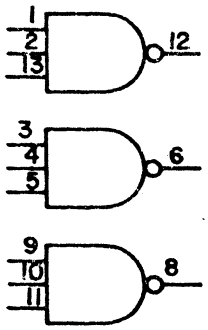
TYPE SN7410N
VENDOR TEXAS INST.
Friden PN 9003091

TRIPLE 3-INPUT POSITIVE NAND GATES

SCHEMATIC DIAGRAM



LOGIC DIAGRAM

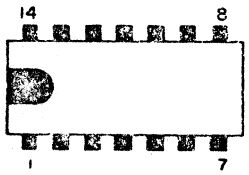


VCC-14 GND-7

CIRCUIT DESCRIPTION

The SN7410N integrated circuit is a Triple 3-Input Positive NAND gate.

PIN NUMBERING AND LOCATION



ABSOLUTE MAXIMUM RATINGS

VCC	=	7 volts
Vin	=	5.5 volts (max)
t storage	=	-65° to 150° C
t operate	=	0° to 70° C

ELECTRICAL CHARACTERISTIC

Vin (1)	=	2 volts (min)
Vin (0)	=	.8 volts (max)
Vout (1)	=	2.4 volts (min)
Vout (0)	=	.4 volts (max)
t pd (1)	=	22 nsec (max)
t pd (0)	=	15 nsec (max)

4-4.0 INTEGRATED CIRCUITS (Cont.)

CIRCUIT TYPES

TTL
MSI

SN7442, 4-LINE-TO-10-LINE DECODERS (1-OF-10)

- BCD-to-Decimal
- ~~Excess-3-to-Decimal~~
- ~~Excess-3-Gray-to-Decimal~~

Also for applications as

- 4-Line-to-16-Line Decoders
- 3-Line to 8-Line Decoders

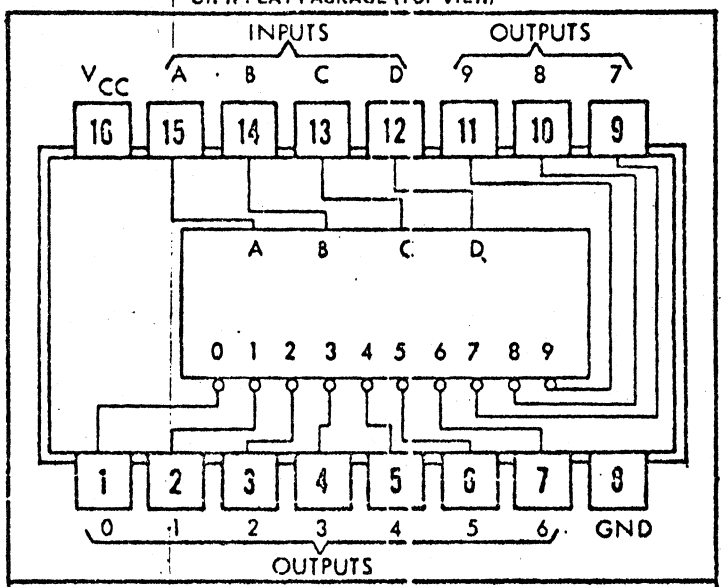
- featuring diode-clamped inputs

description

These monolithic decimal decoders consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic ensures that all outputs remain off for all invalid input conditions.

The SN5442/SN7442 BCD-to-decimal, ~~SN5443/SN7443 excess-3-to-decimal~~, and ~~SN5444/SN7444 excess-3-gray-to-decimal~~ decoders feature familiar transistor-transistor-logic (TTL) circuits with inputs and outputs which are compatible for use with other TTL and DTL circuits. D-c noise margins are typically one volt and power dissipation is typically 140 milliwatts. Full fan-out of 10 is available at all outputs.

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†

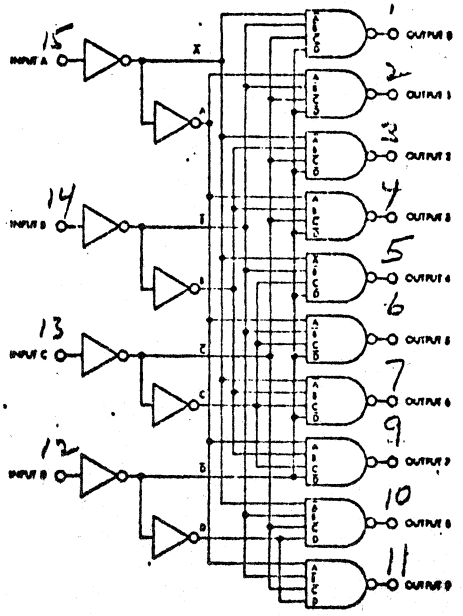


positive logic: see truth tables

†Pin assignments for these circuits are the same for all packages.

SN5442/SN7442

BCD INPUT				ALL TYPES DECIMAL OUTPUT									
D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	1	1	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1
0	1	1	1	1	1	1	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0
1	0	1	0	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1



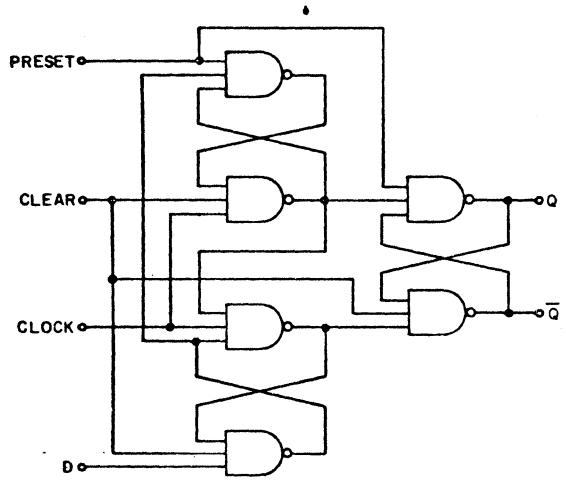
'SN7442 BCD-TO-DECIMAL

4-4.0 INTEGRATED CIRCUITS (Cont.)

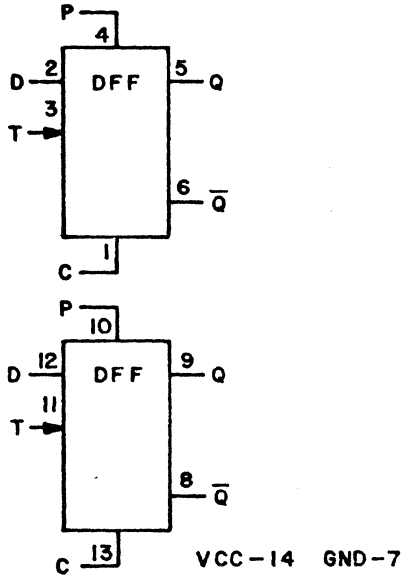
DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOP (TTL)

TYPE SN7474N
VENDOR-Texas Inst.
Friden PN 811784
9003152

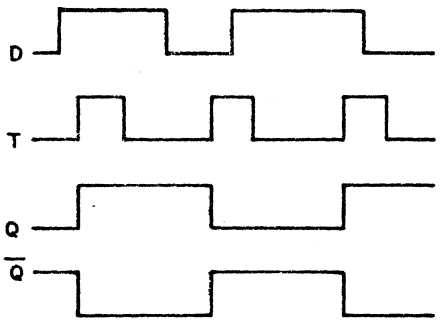
FUNCTIONAL BLOCK DIAGRAM
(each flip-flop)



LOGIC DIAGRAM



TIMING WAVEFORM



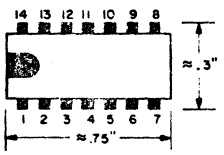
CIRCUIT DESCRIPTION

The SN7474N integrated circuit is a dual, D-type edge-triggered flip-flop with direct-coupled preset and clear inputs. The logic level at the D input is transferred to the Q output on the positive edge of the clock pulse. After the clock threshold voltage has been passed the D input is locked out. Preset and clear must be high for the clock and D inputs to operate. Low to clear resets and low to preset sets the flip-flop. If both preset and clear are low, both Q and Q̄ are high.

ABSOLUTE MAXIMUM RATINGS

V_{CC}	= 7 volts
$t_{storage}$	= -65° to 150° C
$t_{operate}$	= 0° to 70° C

PIN NUMBERING AND LOCATION (top view)



ELECTRICAL CHARACTERISTICS

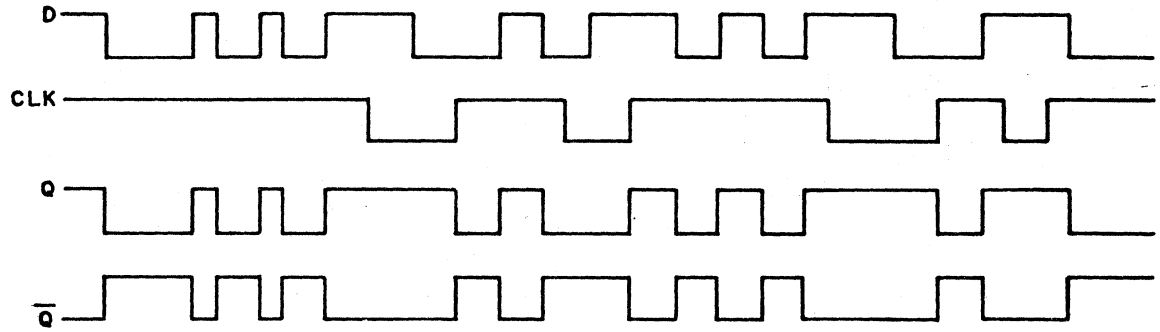
Vin (1-0)	= 2 volts (min)
Vin (0-1)	= .8 volts (max)
Vout (0)	= .4 volts (max)
Vout (1)	= 2.4 volts (min)
$f_{clock\ (max)}$	= 15 MHz (min)

4-4.0 INTEGRATED CIRUCITS (Cont.)

QUADRUPLE BISTABLE LATCH (Cont.)

TYPE SN7475N
VENDOR-Texas Inst.
Friden PN 7011203

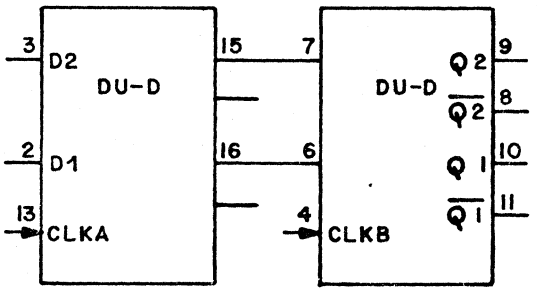
TIMING WAVEFORMS FOR SINGLE LATCH



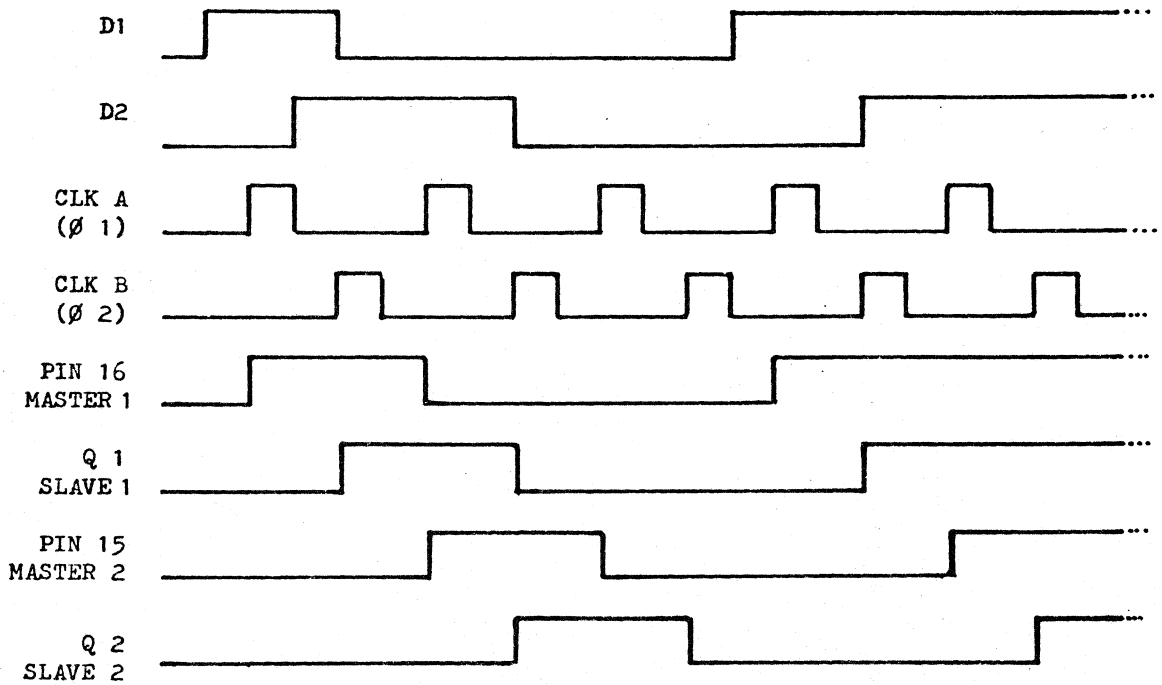
TYPICAL APPLICATION

The SN7475N can be used as a dual D-type master-slave flip-flop by connecting the Q output of one latch to the input of the second latch, such that the input latch (master) operates on Clock 1 and the output latch (slave) operates on Clock 2. Clock 2 occurs later in time than Clock 1. The accompanying waveforms illustrate this mode of operation.

INTERCONNECTION



TIMING WAVEFORMS FOR MASTER SLAVE FLIP-FLOP

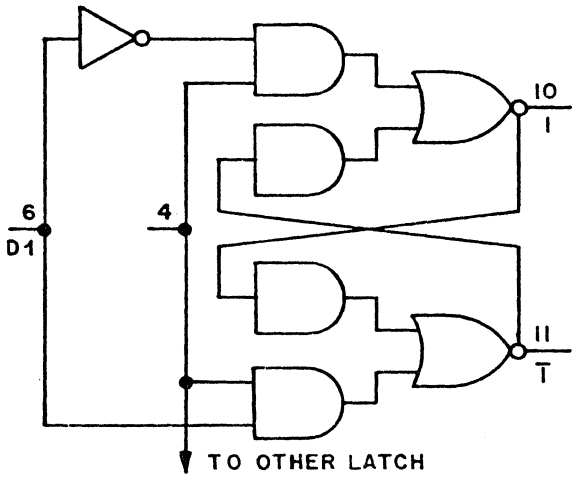


4-4.0 INTEGRATED CIRCUITS (Cont.)

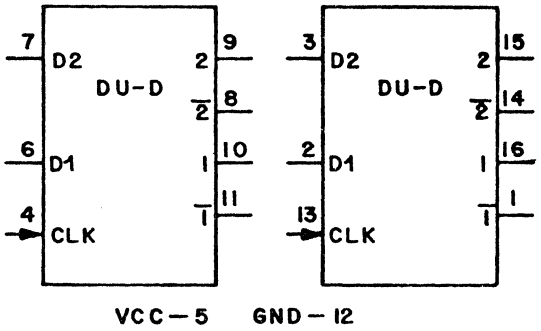
QUADRUPLE BISTABLE LATCH

TYPE SN7475N
VENDOR-Texas Inst.
Friden PN 7011203

FUNCTIONAL BLOCK DIAGRAM



LOGIC DIAGRAM



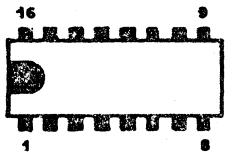
CIRCUIT DESCRIPTION

The SN7475N is a quadruple bistable latch with complementary Q and $\overline{Q}$ outputs. Data at D is transferred to Q when the clock is high. When the clock input is low the outputs are not changed by changes on the input data lines.

ABSOLUTE MAXIMUM RATINGS

V_{CC}	= + 7 volts
V_{input}	= 5.5 volts
$t_{storage}$	= -65° C to 150° C

PIN NUMBERING AND LOCATION



ELECTRICAL CHARACTERISTICS

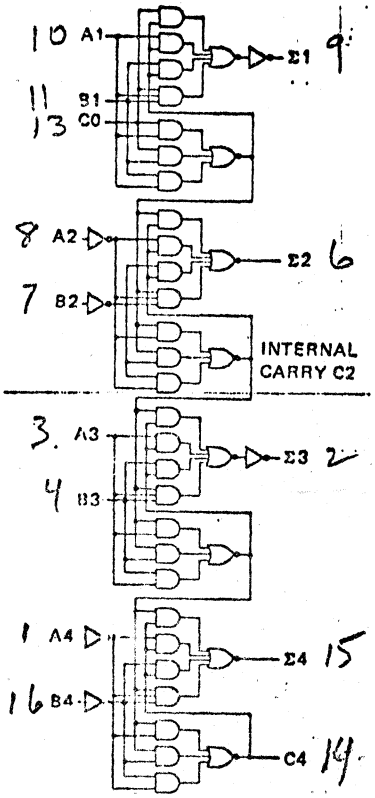
V_{in} (1)	= 2 volts (min)
V_{in} (0)	= .8 volts (max)
V_{out} (1)	= 2.4 volts (min)
V_{out} (0)	= .4 volts (max)

4-4.0 INTEGRATED CIRUCITS (Cont.)

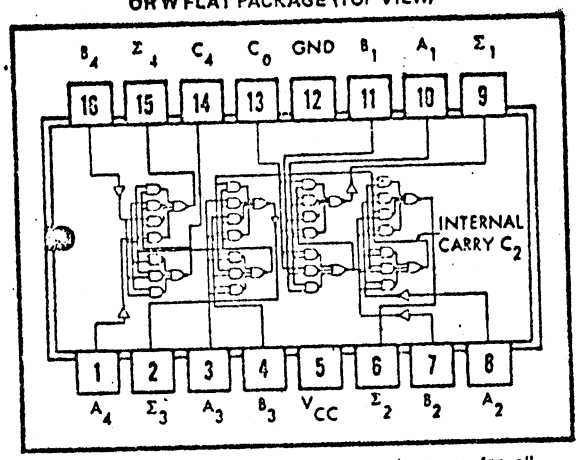
CIRCUIT TYPES SN7483 SN74LS83
4-BIT BINARY FULL ADDERS

description

This full adder performs the addition of two 4-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C_4) is obtained from the fourth bit. Designed for medium-to-high-speed, multiple-bit, parallel-add/serial-carry applications, the circuit utilizes high-speed, high-fan-out transistor-transistor logic (TTL) but is compatible with both DTL and TTL families. The implementation of a single-inversion, high-speed, Darlington-connected serial-carry circuit within each bit minimizes the necessity for extensive "look-ahead" and carry-cascading circuits. The power dissipation level has been maintained considerably below that attainable with equivalent standard integrated circuits connected to perform four-bit full-adder functions.



J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



†Pin assignments for these circuits are the same for all packages.

TRUTH TABLE

INPUT				OUTPUT					
				WHEN C0 = L			WHEN C0 = H		
				WHEN C2 = L			WHEN C2 = H		
A1 / A3	B1 / B3	A2 / A4	B2 / B4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

NOTE 1: Input conditions at A1, A2, B2, and C0 are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4, are then used to determine outputs Σ3, Σ4, and C4.

4-4.0 INTEGRATED CIRCUITS (Cont.)

TTL
MSI

CIRCUIT TYPES SN5493, SN749
4-BIT BINARY COUNTER

MSI TTL HIGH-SPEED RIPPLE-THROUGH COUNTERS

for applications in

- Digital Computer Systems
- Data-Handling Systems
- Control Systems

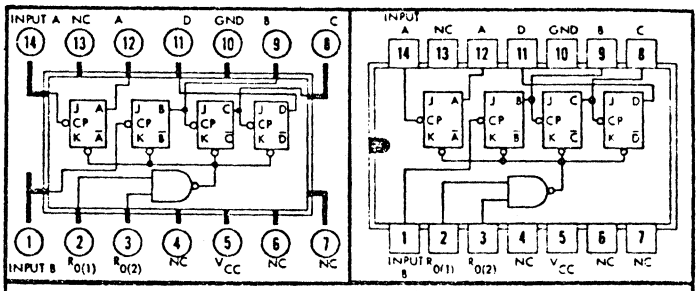
logic

TRUTH TABLE (See Notes 1, 2, and 3)

COUNT	OUTPUT D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

W
FLAT PACKAGE (TOP VIEW)

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: see truth table

NC—No Internal Connection

NOTES: 1. Output A connected to input B
2. To reset all outputs to logical 0 both $R_{0(1)}$ and $R_{0(2)}$ inputs must be at logical 1.
3. Either (or both) reset inputs $R_{0(1)}$ and $R_{0(2)}$ must be at a logical 0 to count.

description

These high-speed, monolithic 4-bit binary counters consist of four master-slave flip-flops which are internally interconnected to provide a divide-by-two counter and a divide-by-eight counter. A gated direct reset line is provided which inhibits the count inputs and simultaneously returns the four flip-flop outputs to a logical 0. As the output from flip-flop A is not internally connected to the succeeding flip-flops the counter may be operated in two independent modes:

1. When used as a 4-bit ripple-through counter, output A must be externally connected to input B. The input count pulses are applied to input A. Simultaneous divisions of 2, 4, 8, and 16 are performed at the A, B, C, and D outputs as shown in the truth table above.

2. When used as a 3-bit ripple-through counter, the input count pulses are applied to input B. Simultaneous frequency divisions of 2, 4, and 8 are available at the B, C, and D outputs. Independent use of flip-flop A is available if the reset function coincides with reset of the 3-bit ripple-through counter.

These circuits are completely compatible with Series 54/74 TTL and DTL logic families. Average power dissipation is 40 mW per flip-flop (160 mW total).

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 4)		7 V
Input Voltage, V_{in} (See Notes 4 and 5)		5.5 V
Operating Free-Air Temperature Range:	SN5493 Circuits	−55°C to 125°C
	SN7493 Circuits	0°C to 70°C
Storage Temperature Range		−65°C to 150°C

NOTES: 4. These voltage values are with respect to network ground terminal.
5. Input signals must be zero or positive with respect to network ground terminal.

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4-4.0 INTEGRATED CIRCUITS (Cont.)

LOW-POWER TTL MSI

CIRCUIT TYPES SN54L93, SN74L93 4-BIT BINARY COUNTERS

A SERIES 54L/74L TTL LOW-POWER RIPPLE-THROUGH COUNTER FOR APPLICATIONS IN

● Digital Computer Systems ● Data-Handling Systems ● Control Systems

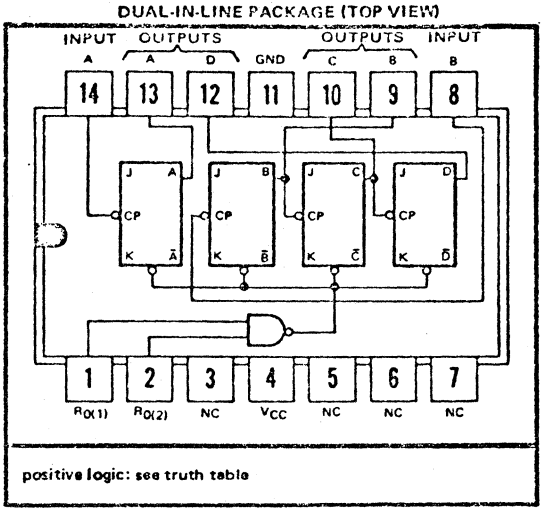
logic

TRUTH TABLE (See Notes 1 and 2)

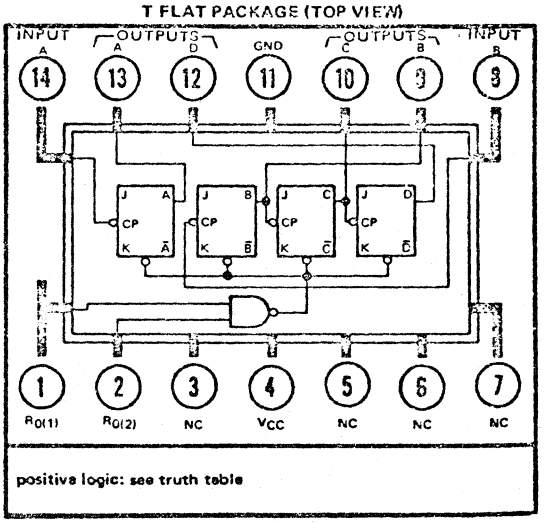
COUNT	OUTPUT			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

NOTES: 1. Output A connected to input B.
2. To reset all outputs to logical 0 both $R_{0(1)}$ and $R_{0(2)}$. Inputs must be at a logical 1.
3. Either (or both) reset inputs $R_{0(1)}$ and $R_{0(2)}$ must be at a logical 0 to count.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



T FLAT PACKAGE (TOP VIEW)



NC—No Internal Connection

description

The SN54L93/SN74L93 are low-power TTL monolithic 4-bit binary counters consisting of four master-slave flip-flops which are internally interconnected to provide a divide-by-two counter and a divide-by-eight counter. A gated direct reset line is provided which inhibits the count inputs and simultaneously returns the four flip-flop outputs to a logical 0. As the output from flip-flop A is not internally connected to the succeeding flip-flops the counter may be operated in two independent modes:

1. When used as a 4-bit ripple-through counter, output A must be externally connected to input B. The input count pulses are applied to input A. Simultaneous divisions of 2, 4, 8, and 16 are performed at the A, B, C, and D outputs as shown in the truth table above.
2. When used as a 3-bit ripple-through counter, the input count pulses are applied to input B. Simultaneous frequency divisions of 2, 4, and 8 are available at the B, C, and D outputs. Independent use of flip-flop A is available if the reset function coincides with reset of the 3-bit ripple-through counter.

The SN54L93/SN74L93 is completely compatible with TTL and DTL logic families. Average power dissipation is typically 16 mW.

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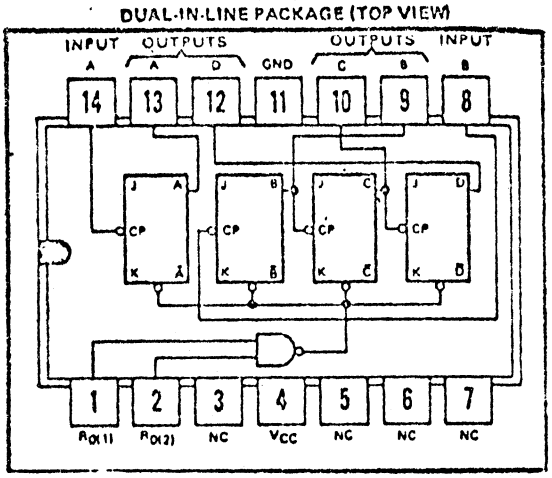
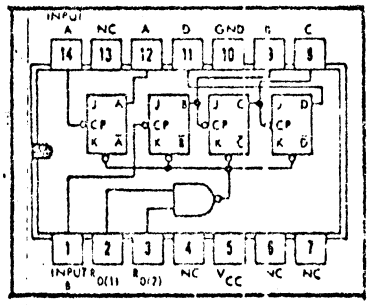
4-4.0 INTEGRATED CIRCUITS (Cont.)

SN74L93 SN7493

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



RESET = $R_{0(1)} \cdot R_{0(2)}$

CLOCK = ↓

TRUTH TABLE (See Notes 1 and 2)

COUNT	OUTPUT			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

NOTES: 1. Output A connected to input B.
2. To reset all outputs to logical 0 both $R_{0(1)}$ and $R_{0(2)}$, inputs must be at a logical 1.
3. Either (or both) reset inputs $R_{0(1)}$ and $R_{0(2)}$ must be at a logical 0 to count.

description

These high-speed, monolithic 4-bit binary counters consist of four master-slave flip-flops which are internally interconnected to provide a divide-by-two counter and a divide-by-eight counter. A gated direct reset line is provided which inhibits the count inputs and simultaneously returns the four flip-flop outputs to a logical 0. As the output from flip-flop A is not internally connected to the succeeding flip-flops the counter may be operated in two independent modes:

1. When used as a 4-bit ripple-through counter, output A must be externally connected to input B. The input count pulses are applied to input A. Simultaneous divisions of 2, 4, 8, and 16 are performed at the A, B, C, and D outputs as shown in the truth table above.
2. When used as a 3-bit ripple-through counter, the input count pulses are applied to input B. Simultaneous frequency divisions of 2, 4, and 8 are available at the B, C, and D outputs. Independent use of flip-flop A is available if the reset function coincides with reset of the 3-bit ripple-through counter.

LOW-POWER TTL MSI

4-4.0 INTEGRATED CIRUCITS (Cont.)

CIRCUIT TYPES SN54L98, SN74L98
4-BIT DATA SELECTORS/STORAGE REGISTERS

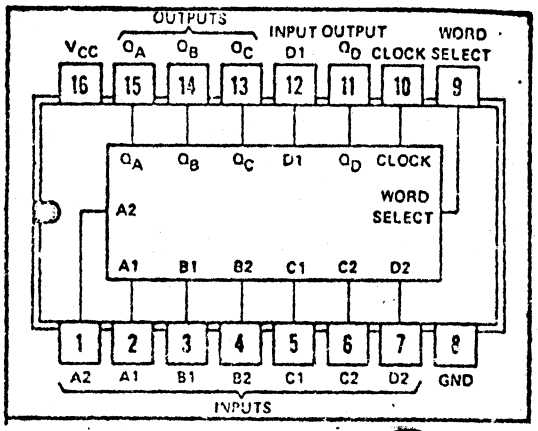
description

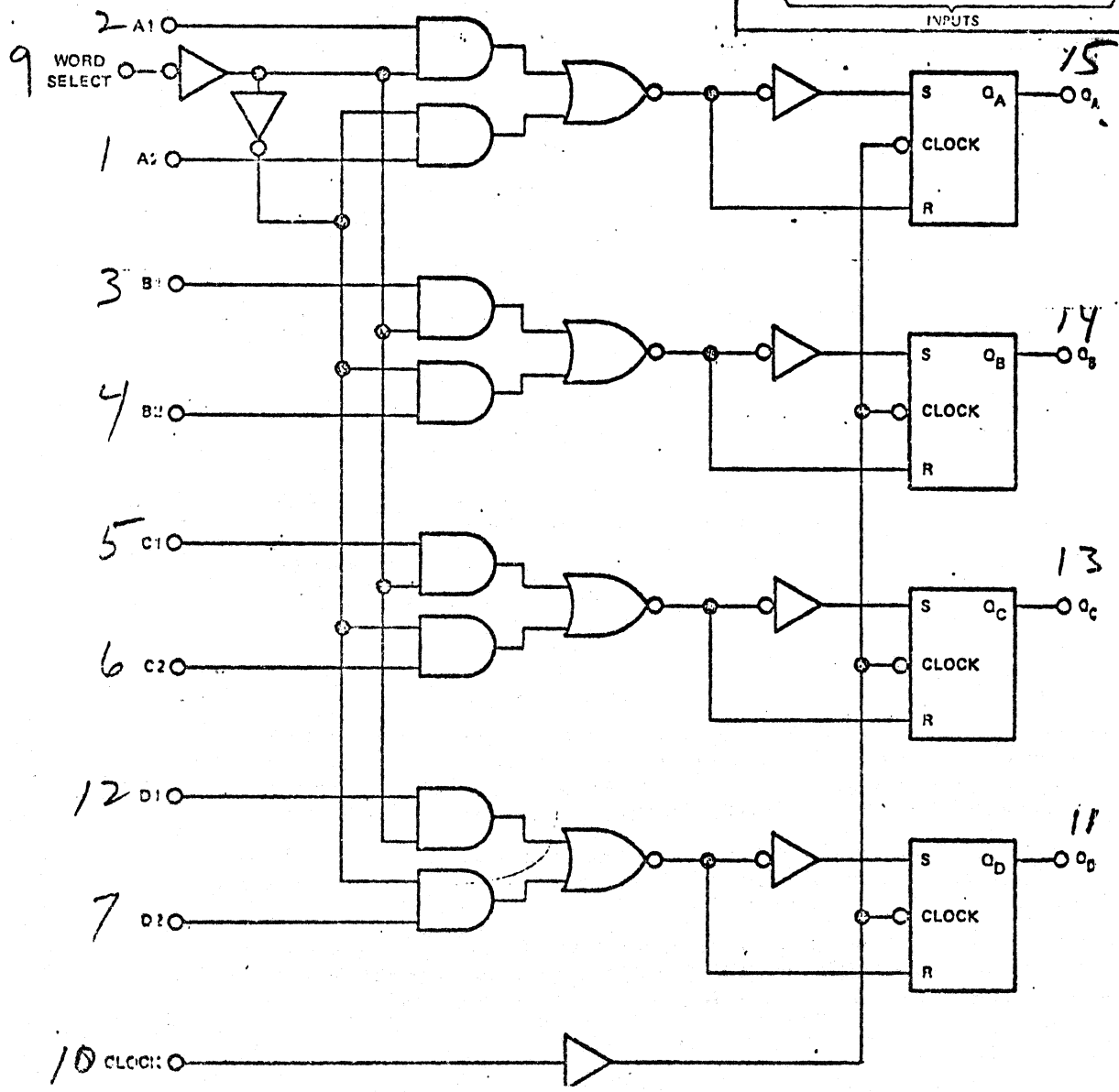
These monolithic data selectors/storage registers are composed of four S-R master-slave flip-flops, four AND-OR-INVERT gates, one buffer, and six inverter/drivers.

When the word select input is low, word 1 (A1, B1, C1, D1) is applied to the flip-flops. A high input to word select will cause the selection of word 2 (A2, B2, C2, D2). The selected word is shifted to the output terminals on the negative-going edge of the clock pulse.

Typical power dissipation is 25 mW. The SN54L98 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74L98 is characterized for operation from 0°C to 70°C.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)





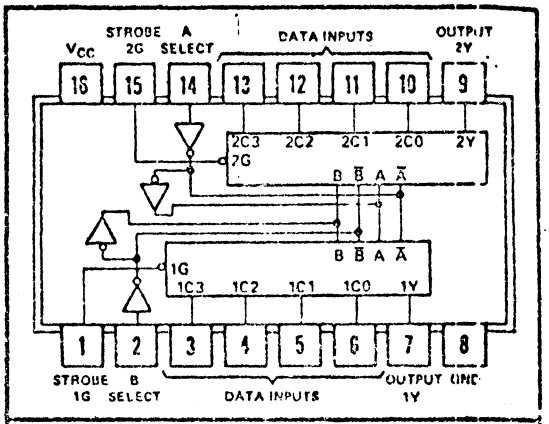
4-4.0 INTEGRATED CIRCUITS (Cont.) SN74153

LOW-POWER TTL MSI CIRCUIT TYPES SN74L153

DUAL 4-LINE-TO-1-LINE DATA SELECTORS/MULTIPLEXERS

- Permits Multiplexing from N lines to 1 line
- Performs Parallel-to-Serial Conversion
- Strobe (Enable) Line Provided for Cascading (N lines to n lines)
- Typical Average Propagation Delay Times:
  - Data Input to Output . . . 27 ns
  - Strobe Input to Output . . . 34 ns
  - Select Input to Output . . . 44 ns
- High-Fan-Out, Low-Impedance, Totem-Pole Outputs
- Fully Compatible with most TTL and DTL Circuits
- Low Power Dissipation . . . 90 mW Typical

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: see truth tables

description

Each of these monolithic, data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR gates. Separate strobe inputs are provided for each of the two four-line sections.

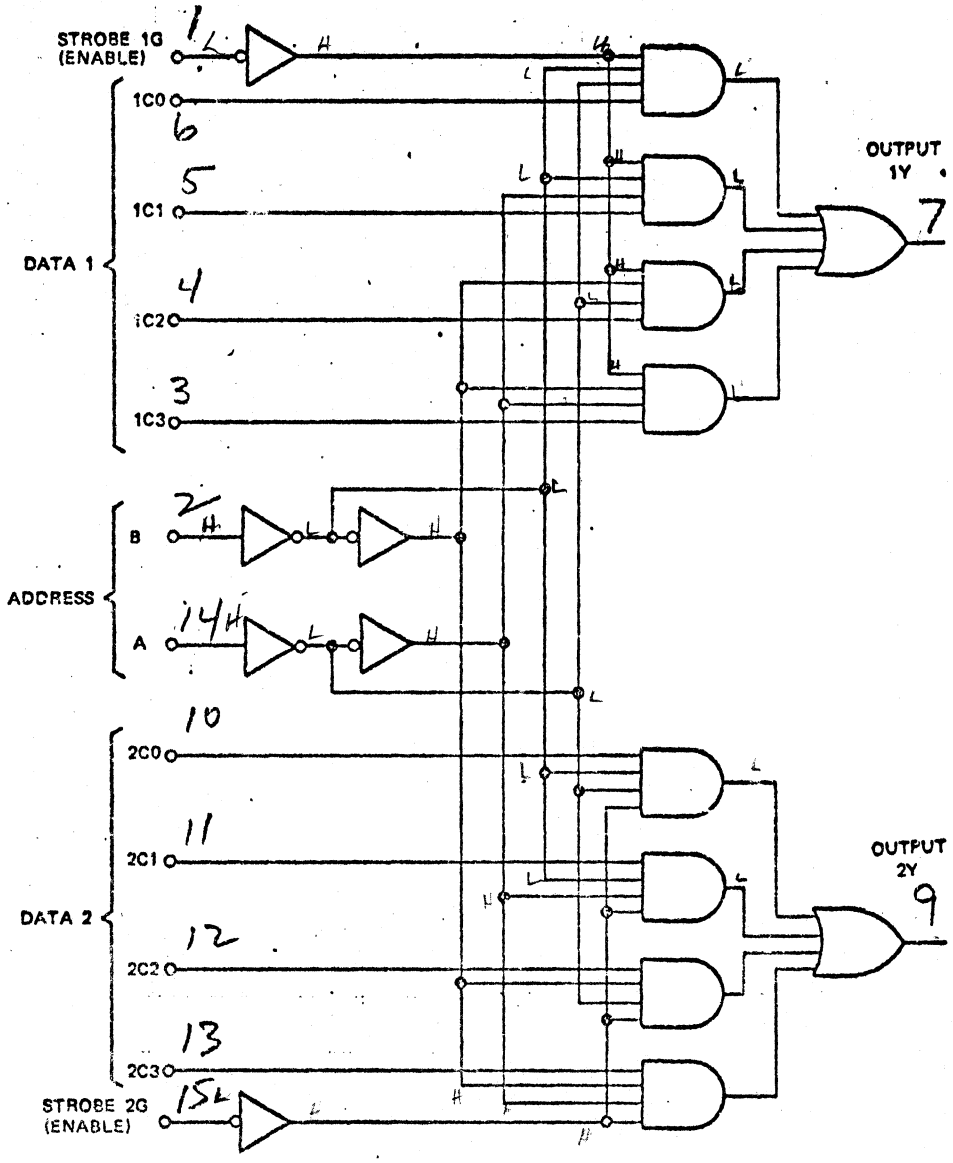
These data selectors/multiplexers are fully compatible for use with most TTL and DTL circuits. Each diode-clamped input represents only one-half of one normalized Series 54/74 load, or approximately five Series 54L/74L gate loads at a low logic level, or two Series 54L/74L gate loads at a high logic level. A fan-out to 5 normalized Series 54/74 loads in the low-level state and 10 in the high-level state is available from each output. Typical power dissipation is 90 milliwatts.

TRUTH TABLE

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.
H = high level, L = low level, X = irrelevant

4-4.0 INTEGRATED CIRCUITS (Cont.) SN74153 SN74L153



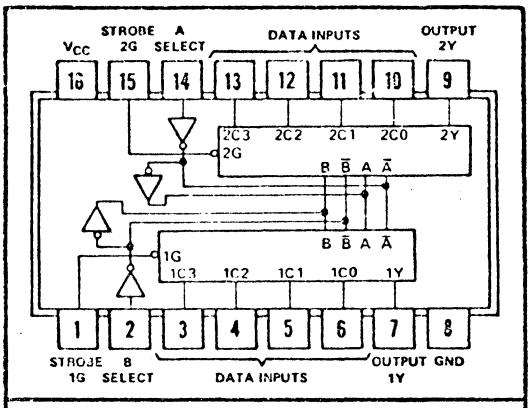
4-4.0 INTEGRATED CIRCUITS (Cont.)

LOW-POWER TTL MSI

CIRCUIT TYPES SN54L153, SN74L153
DUAL 4-LINE-TO-1-LINE DATA SELECTORS/MULTIPLEXERS

- Permits Multiplexing from N lines to 1 line
- Performs Parallel-to-Serial Conversion
- Strobe (Enable) Line Provided for Cascading (N lines to n lines)
- Typical Average Propagation Delay Times:
  - Data Input to Output . . . 27 ns
  - Strobe Input to Output . . . 34 ns
  - Select Input to Output . . . 44 ns
- High-Fan-Out, Low-Impedance, Totem-Pole Outputs
- Fully Compatible with most TTL and DTL Circuits
- Low Power Dissipation . . . 90 mW Typical

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: see truth tables

description

Each of these monolithic, data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR gates. Separate strobe inputs are provided for each of the two four-line sections.

These data selectors/multiplexers are fully compatible for use with most TTL and DTL circuits. Each diode-clamped input represents only one-half of one normalized Series 54/74 load, or approximately five Series 54L/74L gate loads at a low logic level, or two Series 54L/74L gate loads at a high logic level. A fan-out to 5 normalized Series 54/74 loads in the low-level state and 10 in the high-level state is available from each output. Typical power dissipation is 90 milliwatts.

TRUTH TABLE

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.
H = high level, L = low level, X = irrelevant

Resistor values in the OR function have been reduced to minimize the capactive effects of paralleling the phase-splitter transistors and to reduce the propagation delay times. The SN54L153 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74L153 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (see Note 1)	5.5 V
Operating free-air temperature range: SN54L153 Circuits	−55°C to 125°C
SN74L153 Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

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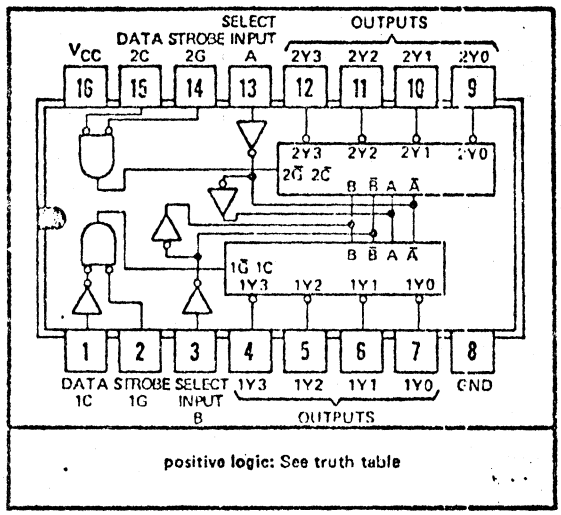
4-4.0 INTEGRATED CIRCUITS (Cont.)

TTL
MSI

CIRCUIT TYPES SN54155, SN54156, SN74155, SN74156
DUAL 2-LINE-TO-4-LINE DECODERS/DEMULTIPLEXERS

- Applications:
  - Dual 2-to-4-Line Decoder
  - Dual 1-to-4-Line Demultiplexer
  - 3-to-8-Line Decoder
  - 1-to-8-Line Demultiplexer
- Individual Strobes Simplify Cascading for Decoding or Demultiplexing Larger Words
- Input Clamping Diodes Simplify System Design
- Choice of Outputs:
  - Totem Pole (SN54155, SN74155)
  - Open-Collector (SN54156, SN74156)
- Typical Average Propagation Delay Times:
  - 16 ns through 2 levels of logic
  - 21 ns through 3 levels of logic
- Typical Power Dissipation . . . 125 mW

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



†Pin assignments for these circuits are the same for all packages.

description

These monolithic transistor-transistor-logic (TTL) circuits feature dual 1-line-to-4-line demultiplexers with individual strobes and common binary-address inputs in a single 16-pin package. When both sections are enabled by the strobes, the common binary-address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired. Data applied to input 1C is inverted at its outputs and data applied at 2C is not inverted through its outputs. The inverter following the 1C data input permits use as a 3-to-8-line decoder or 1-to-8-line demultiplexer without external gating. See typical applications data and the truth tables for more details.

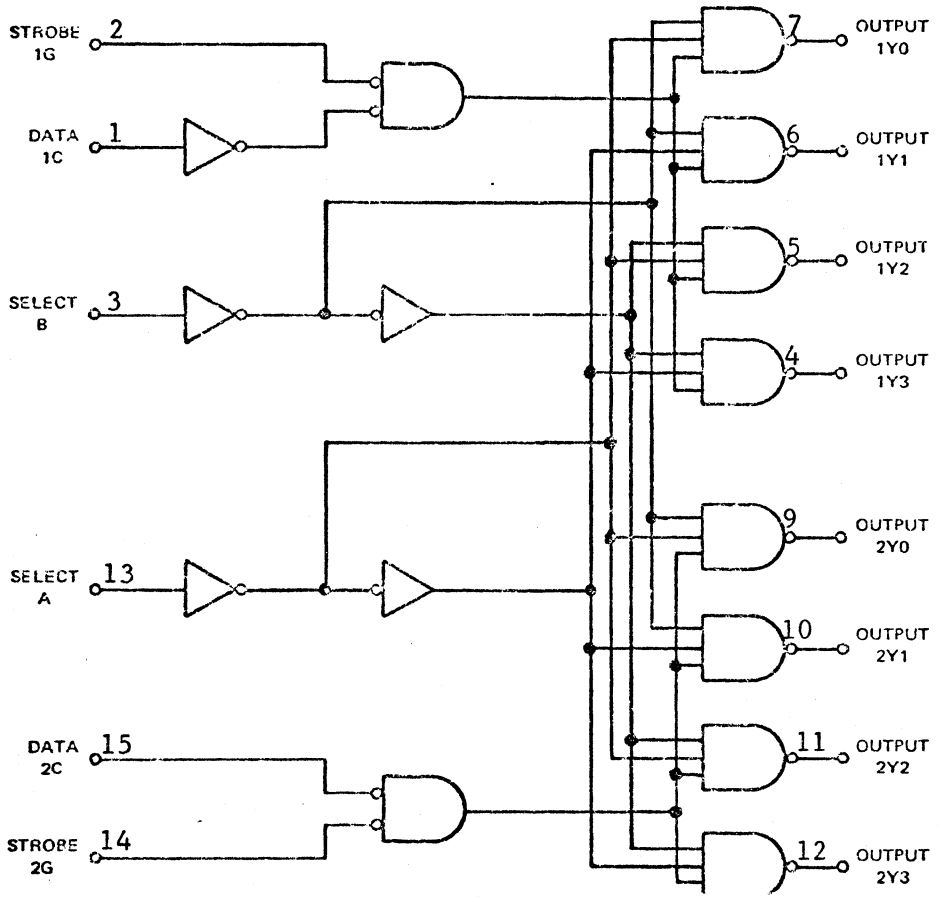
The SN54155/SN74155 circuits, with totem-pole outputs, are rated to fan-out to 10 normalized Series 54/74 loads in the low-level output state, and to 20 loads in the high-level output state. The SN54156/SN74156 circuits, with open-collector outputs, are rated to sink 16 milliamperes at a low-level output voltage of less than 0.4 volt. Input-clamping diodes are provided on all of these circuits to minimize transmission-line effects and simplify system design. Typical power dissipation is 125 milliwatts. Typical average propagation delay times are 16 nanoseconds through 2 levels of logic and 21 nanoseconds through 3 levels of logic for the SN54155/SN74155.

The SN54155 and SN54156 are characterized for operation over the full military temperature range of −55°C to 125°C; the SN74155 and SN74156 are characterized for operation from 0°C to 70°C.

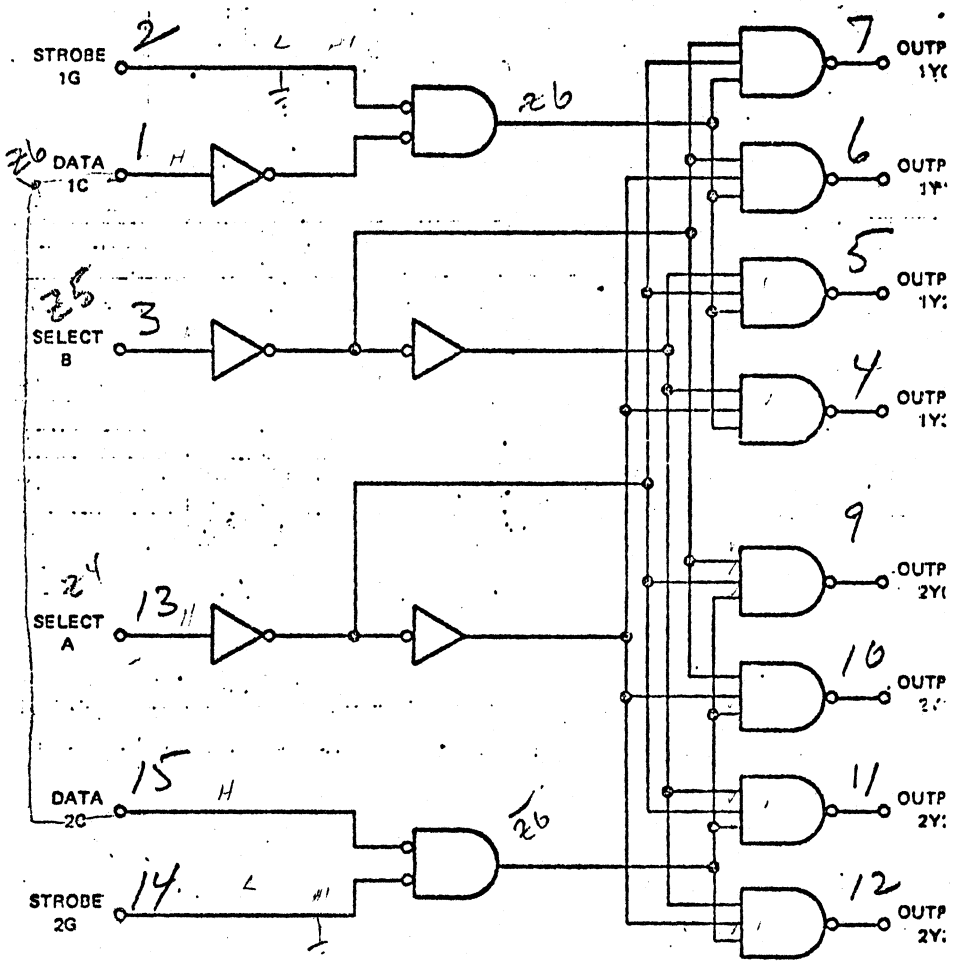
4-4.0 INTEGRATED CIRCUITS (Cont.)

CIRCUIT TYPES SN54155, SN54156, SN74155, SN74156 DUAL 2-LINE-TO-4-LINE DECODERS/DEMULTIPLEXERS

functional block diagram



4-4.0 INTEGRATED CIRCUITS (Cont.) SN54155, SN54156, SN74155, SN74156



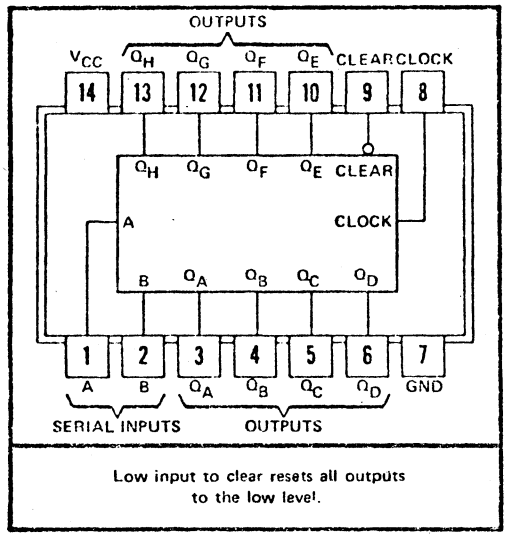
4-4.0 INTEGRATED CIRCUITS (Cont.)

TTL
MSI

CIRCUIT TYPES SN54164, SN74164
8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

- Gated (Enable/Disable) Serial Inputs
- Fully Buffered Clock and Serial Inputs
- Asynchronous Clear
- Typical Maximum Input Clock Frequency . . . 36 MHz

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



†Pin assignments for these circuits are the same for all packages.

TRUTH TABLE
SERIAL INPUTS A AND B

INPUTS AT t_n		OUTPUT AT t_{n+1}
A	B	Q_A
H	H	H
L	H	L
H	L	L
L	L	L

description

These 8-bit shift registers feature gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data as a low at either (or both) input(s) inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high, but only information meeting the setup requirements will be entered. Clocking occurs on the low-to-high-level transition of the clock input.

All inputs are diode-clamped to minimize transmission-line effects, and are buffered to represent only one Series 54/74 load which simplifies system design. Power dissipation is typically 21 milliwatts per bit. Maximum input clock frequency is typically 36 megahertz.

The SN54164 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74164 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (see Note 1)	5.5 V
Operating free-air temperature range: SN54164 Circuits	−55°C to 125°C
SN74164 Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

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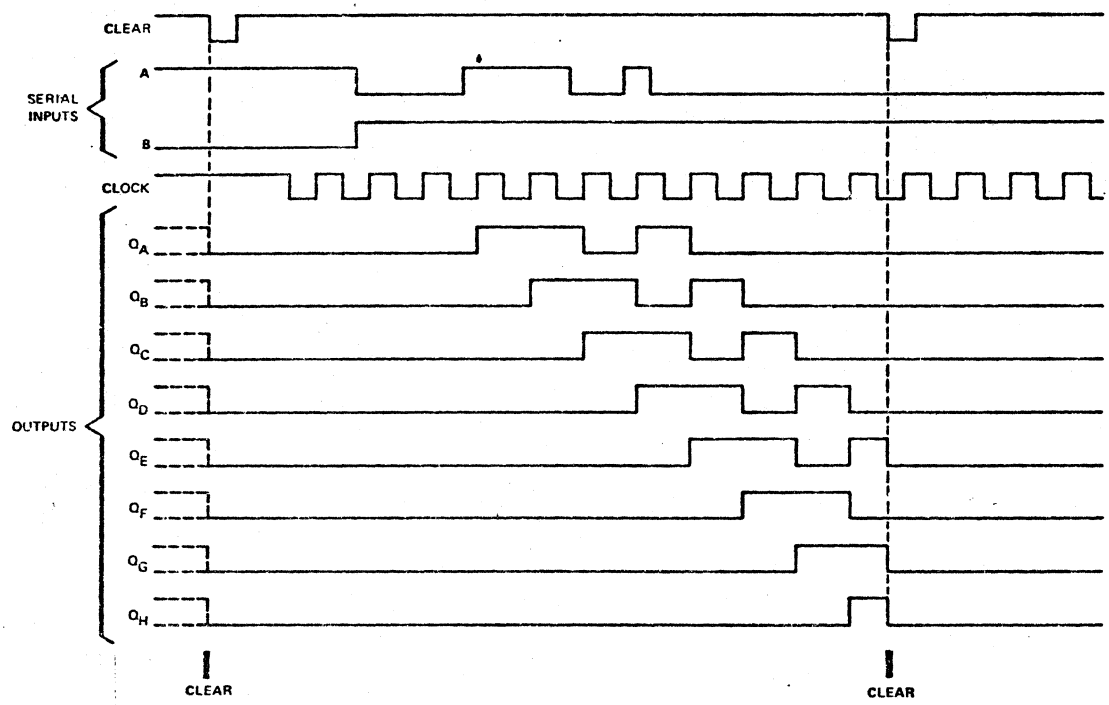
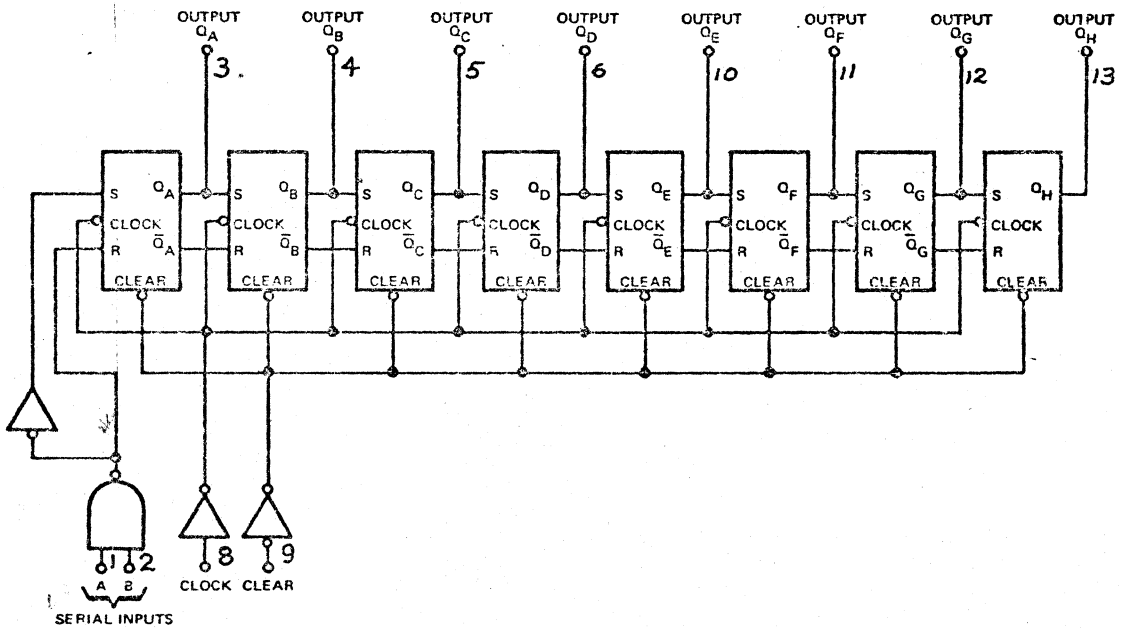
4-4.0 INTEGRATED CIRCUITS (Cont.)

CIRCUIT TYPES SN54164, SN74164
8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

typical clear, inhibit, shift, clear, and inhibit sequences

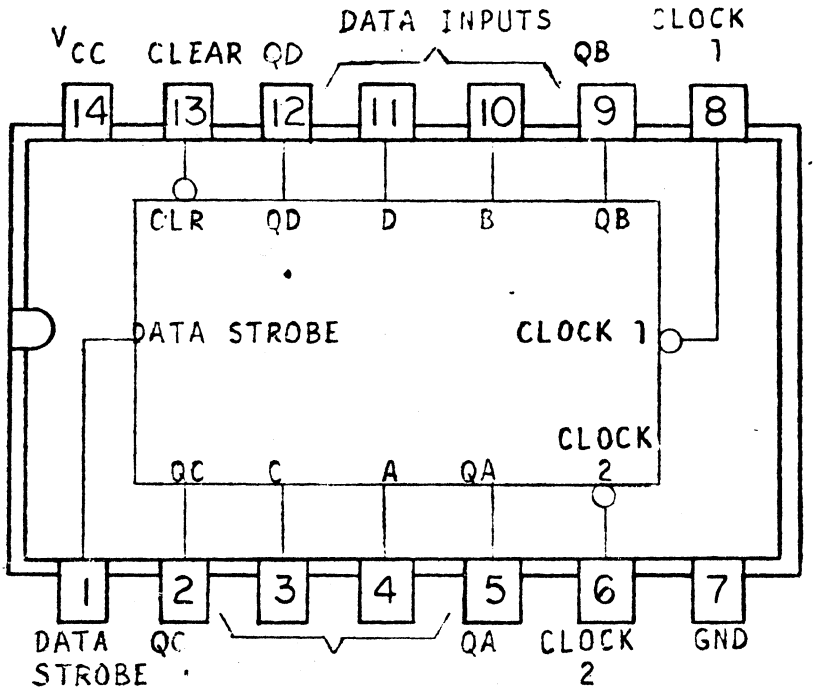


functional block diagram



4-4.0 INTEGRATED CIRCUITS (Cont.)

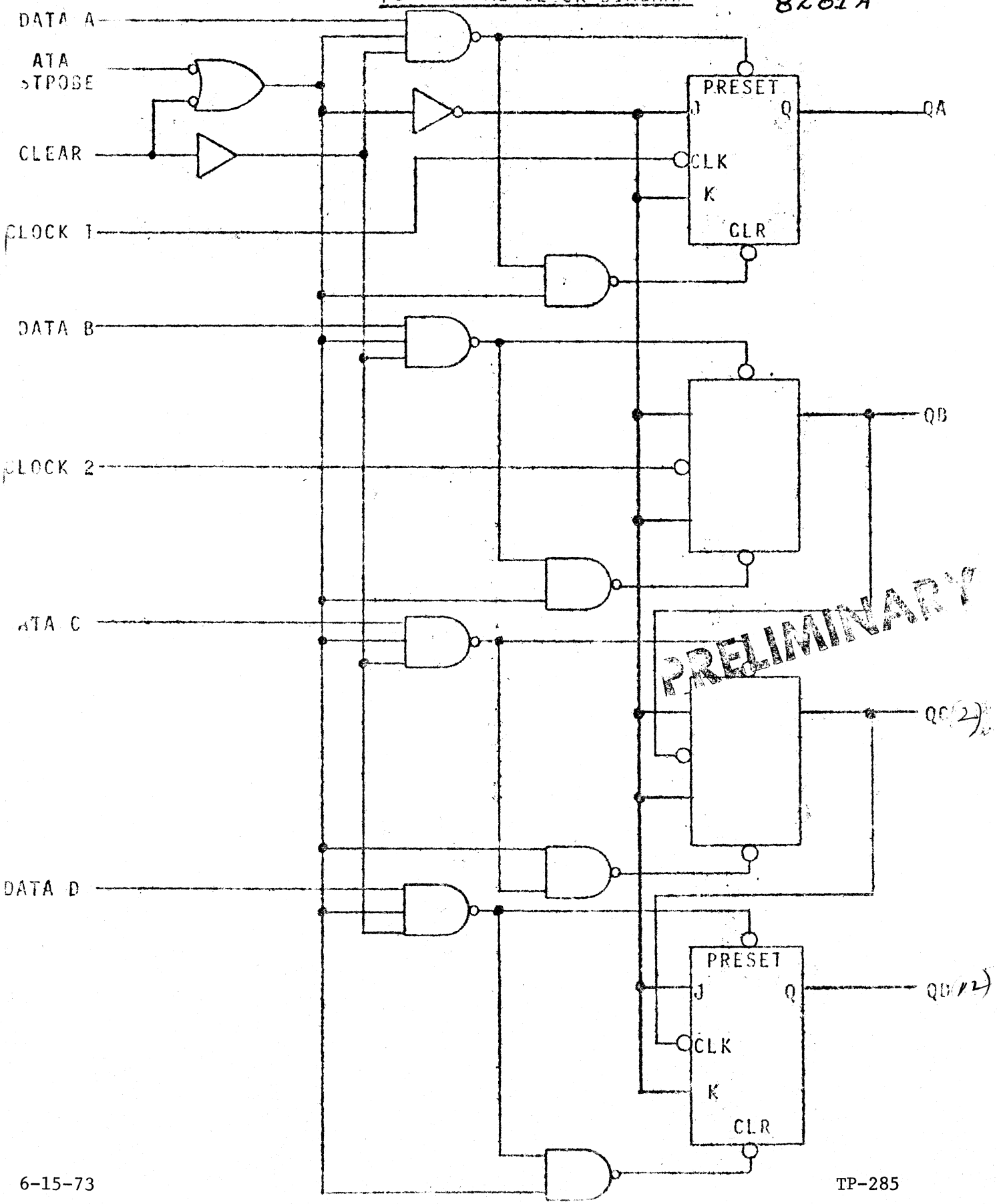
8281A



4-4.0 INTEGRATED CIRCUITS (Cont.)

FUNCTIONAL BLOCK DIAGRAM

8281A



MOS LSI Memory

1101A, 1101A1

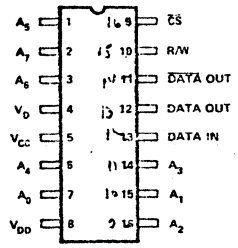
1101A,

4-4.0 INTEGRATED CIRCUITS (Cont.)

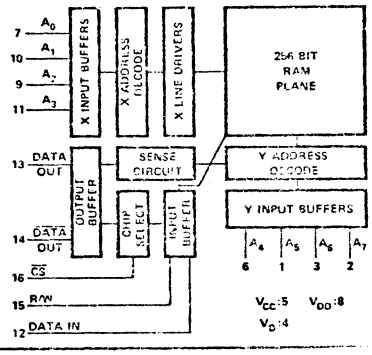
256 BIT FULLY DECODED RANDOM ACCESS MEMORY

- Access Time -- Typically Below 650 nsec - 1101A1, 850 nsec - 1101A
- Low Power Standby Mode
- Low Power Dissipation -- Typically less than 1.5 mW/bit during access
- Directly DTL and TTL Compatible
- OR-Tie Capability
- Simple Memory Expansion -- Chip Select Input Lead
- Fully Decoded --On Chip Address Decode and Sense
- Inputs Protected -- All Inputs Have Protection Against Static Charge
- Ceramic and Plastic Package -- 16 Pin Dual In-Line Configuration

PIN CONFIGURATION



BLOCK DIAGRAM



The 1101A is an improved version of the 1101 which requires only two power supplies (+5V and −9V) for operation. The 1101A is a direct pin for pin replacement for the 1101.

The Intel 1101A is a 256 word by 1 bit random access memory element using normally off P-channel MOS devices integrated on a monolithic array. It uses fully dc stable (static) circuitry and therefore requires no clocks to operate.

The 1101A is designed primarily for small buffer storage applications where high performance, low cost, and ease of interfacing with other standard logic circuits are important design objectives. The unit will directly interface with standard bipolar integrated logic circuits (TTL, DTL, etc.) The data output buffers are capable of driving TTL loads directly. A separate chip select ($\overline{CS}$) lead allows easy selection of an individual package when outputs are OR-tied.

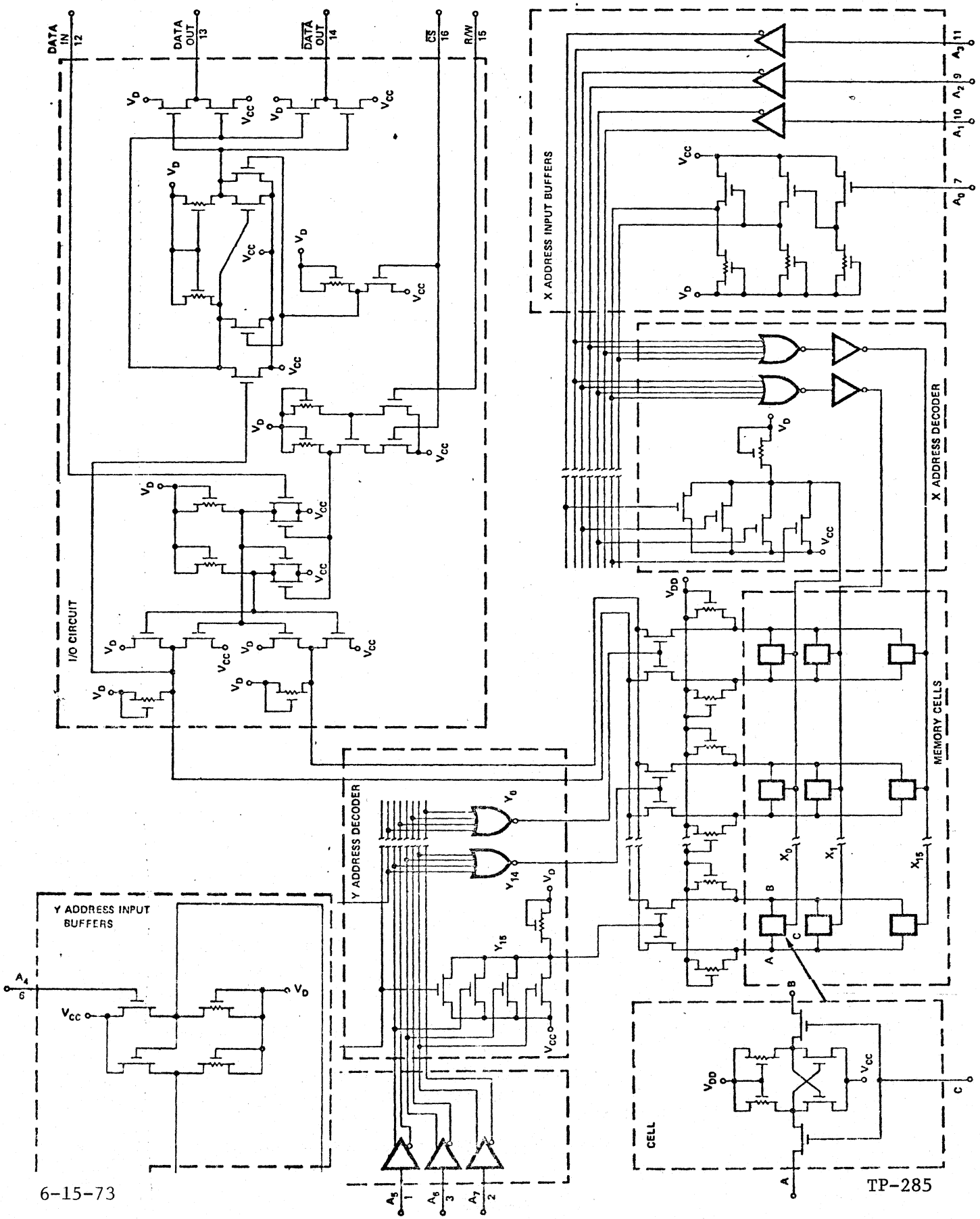
For applications requiring a faster access time we recommend the 1101A1 which is a selection from the 1101A and has a guaranteed maximum access time of 1.0 μsec.

The Intel 1101A is fabricated with silicon gate technology. This low threshold technology allows the design and production of higher performance MOS circuits and provides a higher functional density on a monolithic chip than conventional MOS technologies.

Intel's silicon gate technology also provides excellent protection against contamination. This permits the use of low cost silicone packaging.

Circuit Schematic

4-4.0 INTEGRATED CIRCUITS (Cont.)

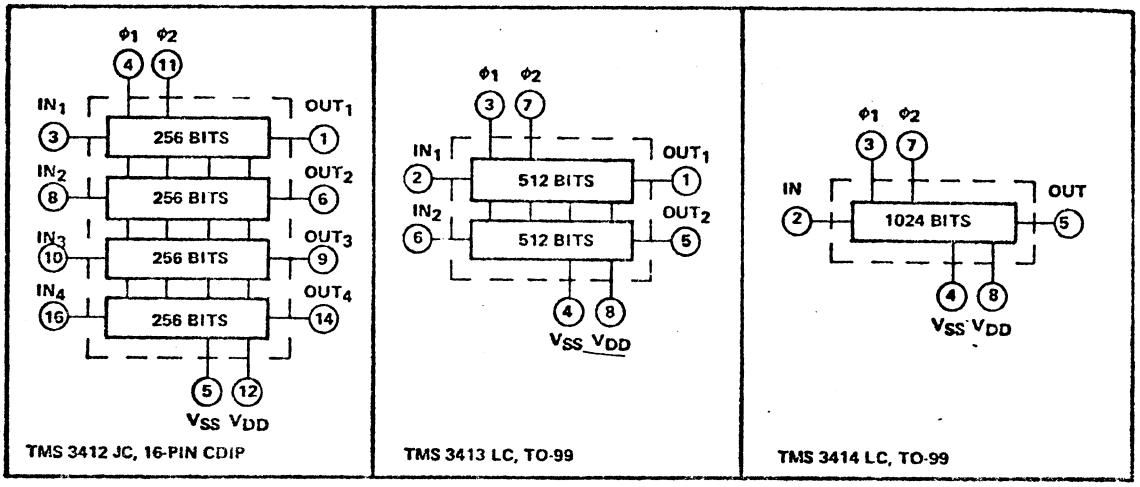


6-15-73

4-4.0 INTEGRATED CIRCUITS (Cont.)

TMS 3412 JC, NC; TMS 3413 LC, NC; TMS 3414 LC, NC
1024-BIT DYNAMIC SHIFT REGISTER

functional block diagram



recommended operating conditions

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNITS
Operating Voltage					
Substrate supply V_{SS}	V_{DD} = −5 V ± 5%	+4.75	5	5.25	V
Drain supply V_{DD}	V_{SS} = +5 V ± 5%	−4.75	−5	−5.25	V
Logic Levels					
Input High level V_{IH}		V_{SS}−1.7		V_{SS}+0.3	V
Input Low level V_{IL}		V_{SS}−4.2		V_{SS}−10	V
Clock Voltage Levels					
Clock High level $V_{\phi H}$		V_{SS}−1.0		V_{SS}+0.3	V
Clock Low level $V_{\phi L}$		V_{SS}−15.0		V_{SS}−17.0	V
Pulse Timing					
Clock pulse transition $t_{r\phi}$, $t_{f\phi}$				1000	ns
Clock pulse width 1 $PW_{\phi 1}$		100			ns
Clock pulse width 2 $PW_{\phi 2}$		100			ns
Pulse spacing					
Clock delay $t_{D\phi 12}$	$PW_{\phi 1}$ = $PW_{\phi 2}$ = 100 ns	40			ns
Clock delay $t_{D\phi 21}$	$PW_{\phi 1}$ = $PW_{\phi 2}$ = 100 ns	40			ns
Data setup t_{DS}		40			ns
Data hold t_{DH}		40			ns
Pulse Repetition Rate PRR					
Data				6	MHz
Clock				3	MHz

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4-4.0 INTEGRATED CIRCUITS (Cont.)

TMS 3412 JC, NC; TMS 3413 LC, NC; TMS 3414 LC, NC
1024-BIT DYNAMIC SHIFT REGISTER

static electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNITS
I_{IL}	Input Current	V_{IN} = −5 V,	V_{SS} = +5 V			500	nA
$I_{\phi L}$	Clock Current	V_{ϕ} = −10 V,	V_{SS} = +5 V			1000	nA
Output Voltage Levels							
V_{OL}	Output Low level	R_L = 3 kΩ, V_{SS} = +5 V	I_L = 1.6 mA,			0.5	V
V_{OH}	Output High level	Driving TTL, V_{SS} = 4.75 V	R_L = 3 kΩ,	2.5			V
Power Supply Current Drain							
I_{DD}	Drain supply	V_{SS} = +5 V, V_{ϕ} = −12 V	V_{DD} = −5 V,		35	50	mA
P_D	Power Dissipation	5-MHz Data Rate,	35% Duty Cycle			600	mW

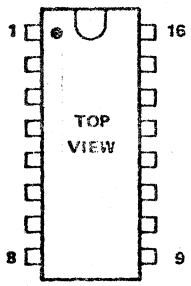
dynamic electrical characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Logic Delay						
t_{DLH1}	Output Low level	1 TTL load (See Note 2)			80	ns
t_{DHL1}	Output High level	1 TTL load (See Note 2)			80	ns
Output Logic Delay						
t_{DLH2}	Output Low level	MOS load (See Note 3)			80	ns
t_{DHL2}	Output High level	MOS load (See Note 3)			80	ns
Capacitance						
C_{IN}	Input	(See Note 4)	2.5		5	pF
C_{ϕ}	Clock		60	70	80	pF

NOTES: 2. V_{SS} = +5 V ± 5%, V_{DD} = −5 V ± 5%, $V_{\phi L}$ = −10 V
3. V_{SS} = 0 V, V_{DD} = −10 V ± 10%, $V_{\phi L}$ = −15 V
4. 16-pin CDIP — C_{IN} min, 7 pF; C_{IN} max, 8 pF

mechanical data and pin configuration

The TMS 3412 is available in both a 16-pin hermetically sealed ceramic dual-in-line package (JC) and a 16-pin plastic package (NC). The packages are designed for insertion in mounting-hole rows on 0.300-inch centers. (See MOS/LSI packaging section.)



PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	OUT_1	9	OUT_3
2	NC	10	IN_3
3	IN_1	11	ϕ_2
4	ϕ_1	12	V_{DD}
5	V_{CC} (V_{SS})	13	NC
6	OUT_2	14	OUT_4
7	NC	15	NC
8	IN_2	16	IN_4

— continued

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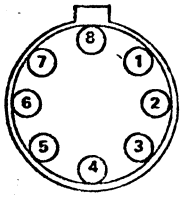
4-4.0 INTEGRATED CIRCUITS (Cont.)

TMS 3412 JC, NC; TMS 3413 LC, NC; TMS 3414 LC, NC
1024-BIT DYNAMIC SHIFT REGISTER

mechanical data and pin configuration (continued)

The TMS 3413 and TMS 3414 are available both in 8-lead TO-99 packages (LC) and in 16-pin dual-in-line plastic packages (NC) designed for insertion in mounting-hole rows on 0.300-inch centers. (See MOS/LSI packaging section.)

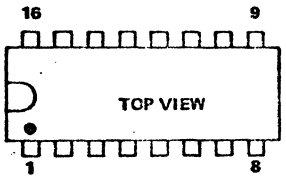
1155



BOTTOM VIEW

TMS 3413 LC	
LEAD NO.	FUNCTION
1	Output 1
2	Input 1
3	ϕ_1
4	V_{CC} (V_{SS})
5	Output 2
6	Input 2
7	ϕ_2
8	V_{DD}

TMS 3414 LC	
LEAD NO.	FUNCTION
1	NC
2	Input
3	ϕ_1
4	V_{CC} (V_{SS})
5	Output
6	NC
7	ϕ_2
8	V_{DD}



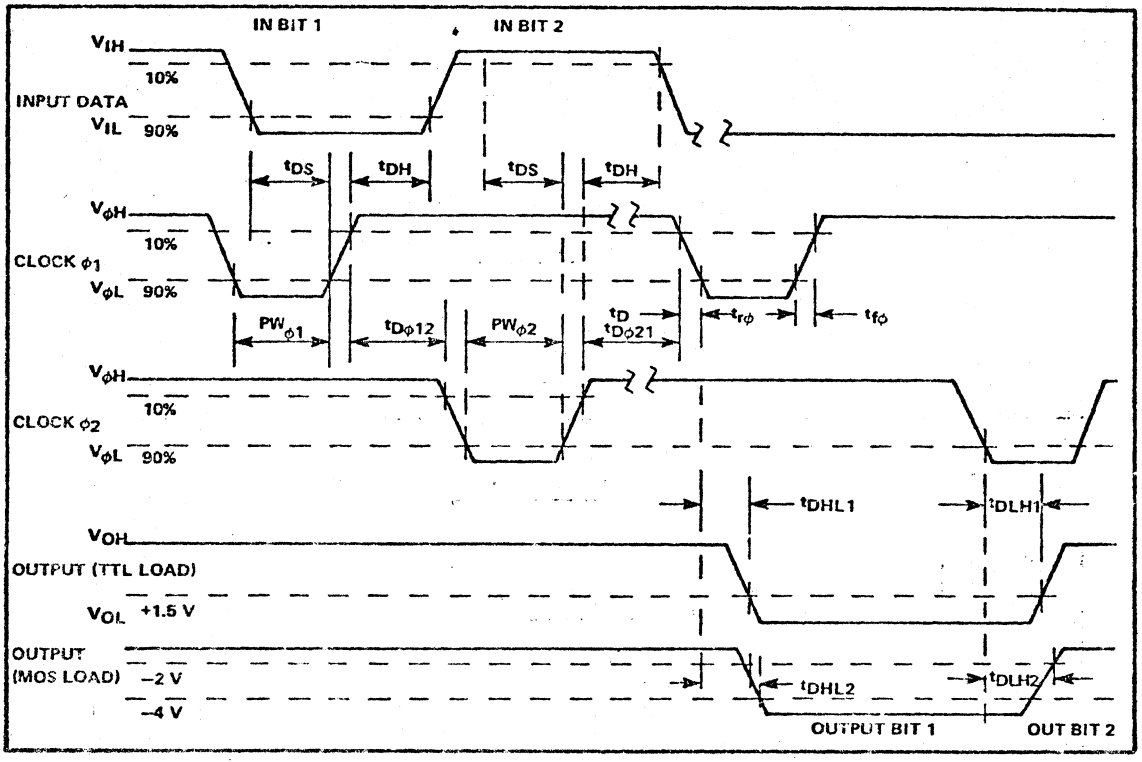
TMS 3413 NC	
PIN NO.	FUNCTION
1	NC
2	NC
3	Input 1
4	ϕ_1
5	V_{SS}
6	Output 2
7	NC
8	NC
9	NC
10	Input 2
11	ϕ_2
12	V_{DD}
13	NC
14	Output 1
15	NC
16	NC

TMS 3414 NC	
PIN NO.	FUNCTION
1	NC
2	NC
3	Input
4	ϕ_1
5	V_{SS}
6	Output
7	NC
8	NC
9	NC
10	NC
11	ϕ_2
12	V_{DD}
13	NC
14	NC
15	NC
16	NC

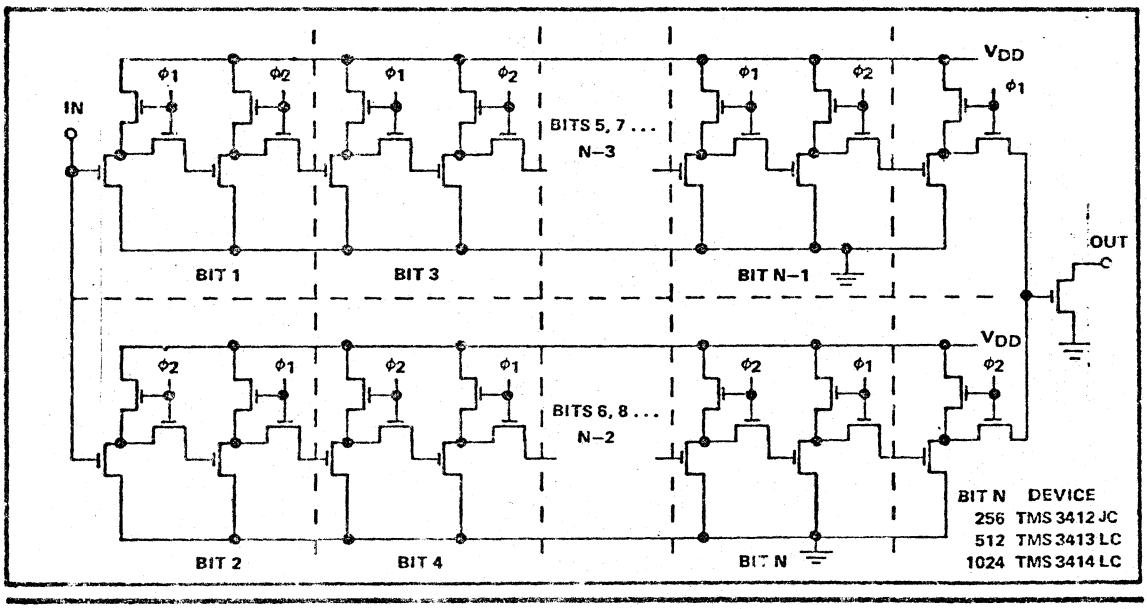
4-4.0 INTEGRATED CIRCUITS (Cont.)

TMS 3412 JC, NC; TMS 3413 LC, NC; TMS 3414 LC, NC
1024-BIT DYNAMIC SHIFT REGISTER

timing diagram and voltage waveforms



circuit diagram



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4-4.0 INTEGRATED CIRCUITS (Cont.)

MM4231/MM5231 2048-bit read only memory

general description

The MM4231/MM5231 is a 2048-bit static read only memory. It is a P-channel enhancement mode monolithic MOS integrated circuit utilizing low threshold voltage technology. The device is a non-volatile memory organized as a 256-8 bit words or 512-4 bit words. Programming of the memory contents is accomplished by changing one mask during the device fabrication.

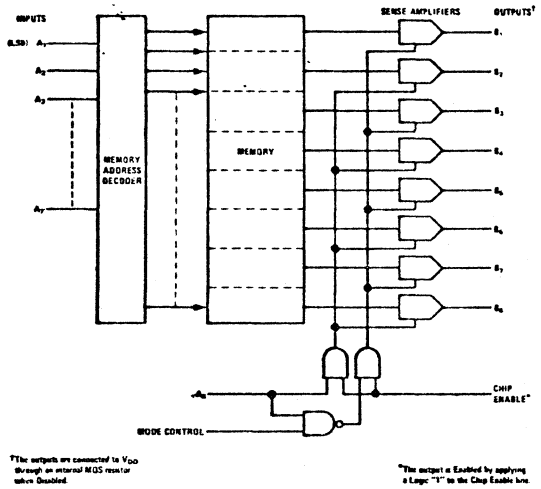
features

- Bipolar compatibility — +5V, −12V operation
- High speed operation — 640 ns typ.
- Static operation — No clocks required
- Common data busing — Output wire AND capability
- Chip enable output control

applications

- Code conversion
- Random logic synthesis
- Table look-up
- Character generator
- Micro-programming

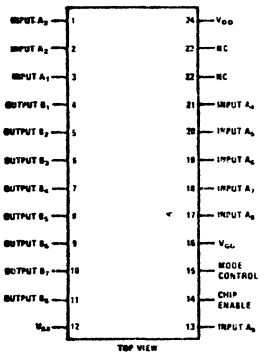
block and connection diagrams



*The outputs are connected to V_{DD} through an internal MOS resistor when Disabled.

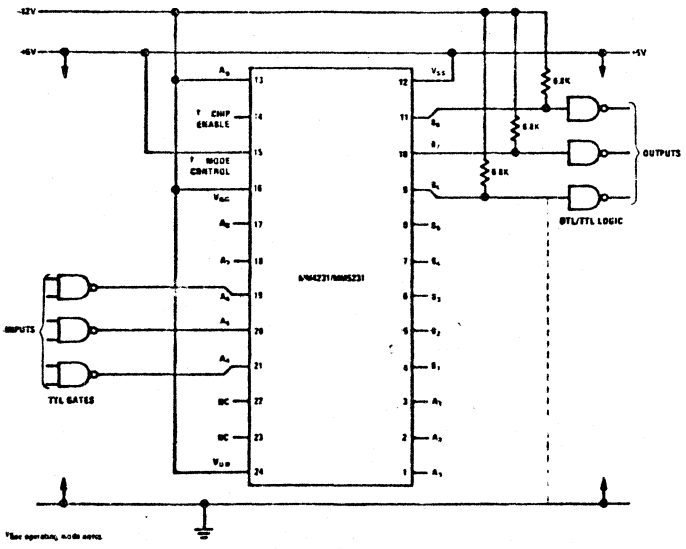
*The output is Enabled by applying a Logic "1" to the Chip Enable line.

Dual-In-Line Package



typical application

256 x 8 Bit ROM Showing TTL Interface



*See operating mode notes.

Operating Modes

256x8 ROM connection (shown)
Mode Control – Logic "0"
A_9 – Logic "1"

512x4 ROM connection
Mode Control – Logic "1"
A_9 – Logic "0" Enables the odd (B_1, B_3 ... B_9) outputs
– Logic "1" Enables the even (B_2, B_4 ... B_8) outputs.

The outputs are "Enabled" when a logic "1" is applied to the Chip Enable line.

Logic levels are negative true MOS logic

Mode Control should be "hard wired" to V_{DD} (Logical "1") or V_{SS} (Logical "0").

4-4.0 INTEGRATED CIRCUITS (Cont.)

MM4231/MM5231

absolute maximum ratings

V_{GG} Supply Voltage		V_{SS} – 20V
V_{DD} Supply Voltage		V_{SS} – 20V
Input Voltage		$(V_{SS} - 20)V < V_{IN} < (V_{SS} + 0.3)V$
Storage Temperature		–65°C to +150°C
Operating Temperature	MM4231	–55°C to +125°C
	MM5231	–25°C to +70°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Levels					
MOS to TTL					
Logical "1"	6.8 kΩ ±5% to V_{DD} Plus One			+0.4	V
Logical "0"	Standard Series 54/74 Gate	2.4			V
Output Current Capability					
Logical "0"	V_{OUT} = 2.4V	2.5			mA
Input Voltage Levels					
Logical "1"				V_{SS} – 4.2	V
Logical "0"		V_{SS} – 2.0			V
Power Supply Current	T_A = 25°C				
I_{DD}	V_{SS} = +5V		15	30	mA
I_{GG} (Note 1)	$V_{GG} = V_{DD}$ = –12V			1	µA
Input Leakage	V_{IN} = –12V			1	µA
Input Capacitance	f = 1.0 MHz, V_{IN} = 0V		5		pF
V_{GG} Capacitance	f = 1.0 MHz, V_{IN} = 0V		15		pF
Address Time (Note 2)	See Timing Diagram				
T_{ACCESS}	T_A = 25°C V_{SS} = +5.0V $V_{GG} = V_{DD}$ = –12.0V		640	950	ns
Output AND Connections (Note 3)	6.8 kΩ ±5% to V_{DD} Plus One Standard Series 54/74 Gate			8	

Note 1: These specifications apply for V_{SS} = +5V ±5%, $V_{GG} = V_{DD}$ = –12V, ±5%, and T_A = –55°C to +125°C (MM4231), T_A = –25°C to +70°C (MM5231) unless otherwise specified.

Note 2: The V_{GG} supply may be clocked to reduce device power without affecting access time.

Note 3: Address time is measured from the change of data on any input or Chip Enable line to the output of a TTL gate. (See Timing Diagram.) See curves for guaranteed limit over temperature.

Note 4: The address time in the TTL load configuration follows the equation:
T_{ACCESS} = The specified limit + (N – 1) (50) ns.
Where N = Number of AND connections.

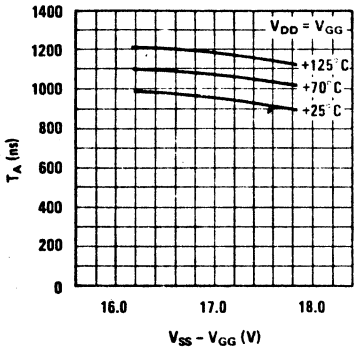
Note 5: Capacitances are measured on a lot sample basis only.

MM4231/MM5231

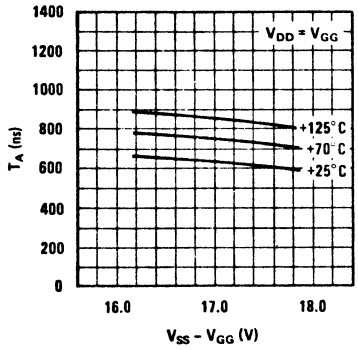
4-4.0 INTEGRATED CIRCUITS (Cont.)

performance characteristics

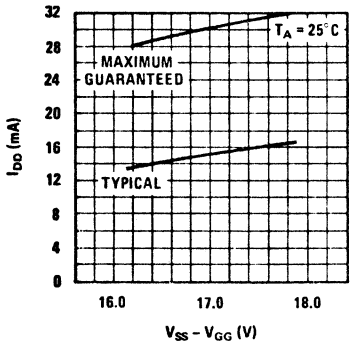
Guaranteed Access Time (T_A) vs Power Supply Voltage



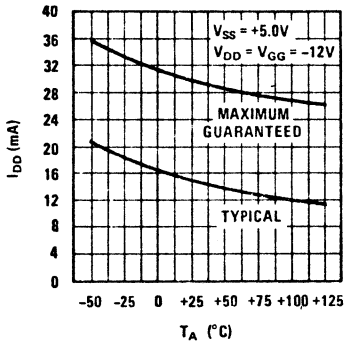
Typical Access Time (T_A) vs Power Supply Voltage



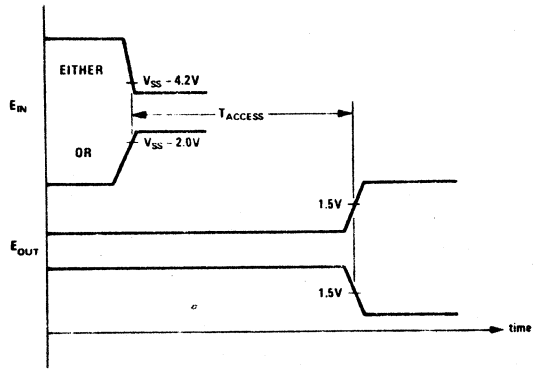
Power Supply Current vs Power Supply Voltage

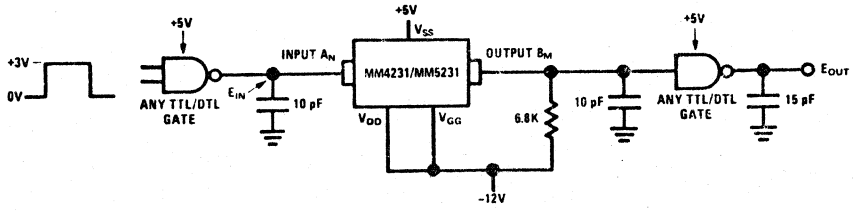


Power Supply Current vs Ambient Temperature



timing diagram/address time





4-4.0 INTEGRATED CIRCUITS (Cont.)

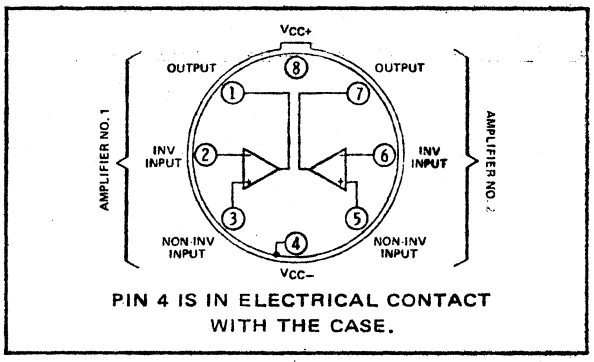
LINEAR INTEGRATED CIRCUITS

CIRCUIT TYPES SN52558, SN72558 DUAL HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

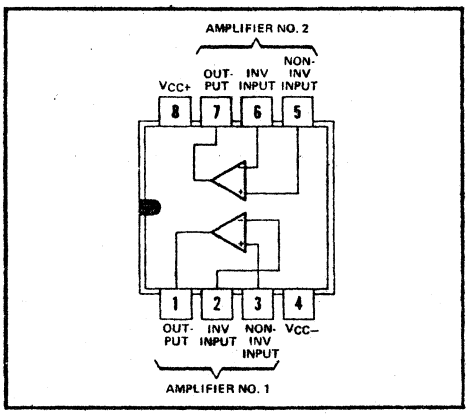
CIRCUIT TYPES SN52558, SN72558
BULLETIN NO. DL-S 7111467, FEBRUARY 1971

- Short-Circuit Protection
- Large Common-Mode and Differential Voltage Ranges
- No Frequency Compensation Required
- Low Power Consumption
- No Latch-up
- Designed to be Interchangeable with Motorola MC1558/MC1458 and Signetics S5558/N5558

L PLUG-IN PACKAGE
(TOP VIEW)



P DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

The SN52558 and SN72558 are dual high-performance operational amplifiers with each half electrically similar to SN52741/SN72741 except that offset null capability is not provided.

The high common-mode input voltage range and the absence of latch-up make these amplifiers ideal for voltage-follower applications. The devices are short-circuit protected and the internal frequency compensation ensures stability without external components.

The SN52558 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN72558 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

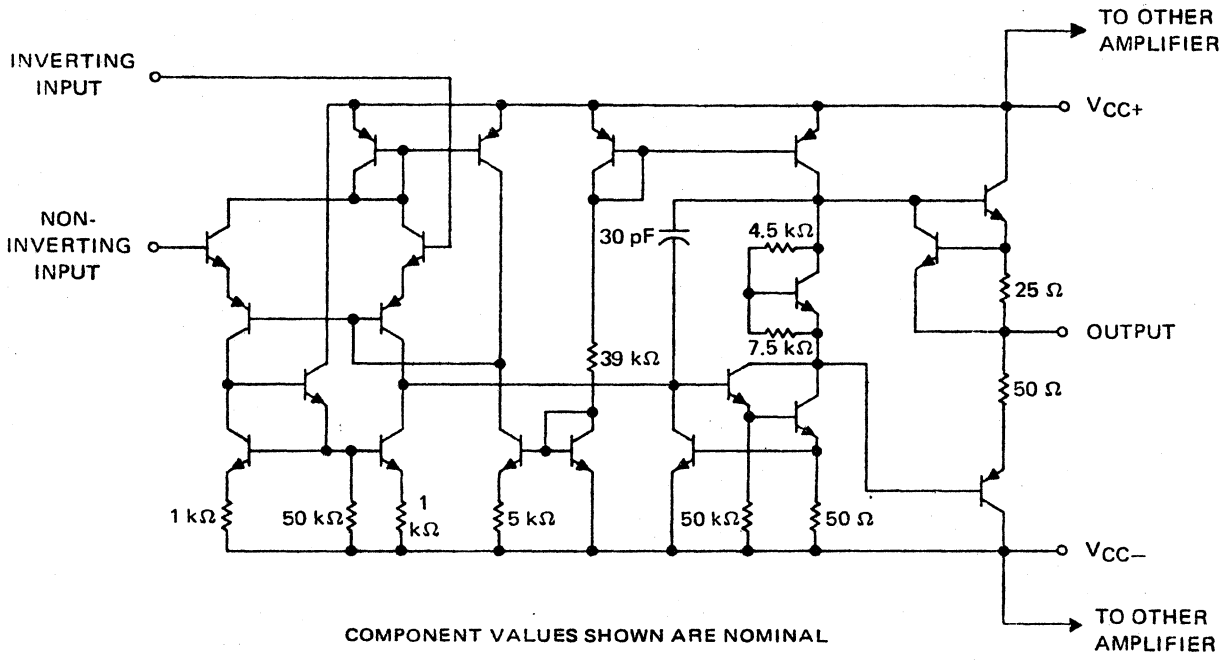
		SN52558	SN72558	UNIT
Supply voltage V_{CC+} (see Note 1)		22	18	V
Supply voltage V_{CC-} (see Note 1)		−22	−18	V
Differential input voltage (see Note 2)		±30	±30	V
Input voltage (either input, see Notes 1 and 3)		±15	±15	V
Duration of output short-circuit (see Note 4)		unlimited	unlimited	
Continuous total dissipation at (or below) 70°C free-air temperature range (see Note 5)	Each amplifier	500	500	mW
	Total package	680	680	
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	L Package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	P Package	260	260	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or either power supply. For the SN52558 only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 75°C free-air temperature.
For operation of SN52558 above 70°C free-air temperature, refer to Dissipation Derating Curve, Figure 1.

4-4.0 INTEGRATED CIRCUITS (Cont.)

CIRCUIT TYPES SN52558, SN72558
DUAL HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

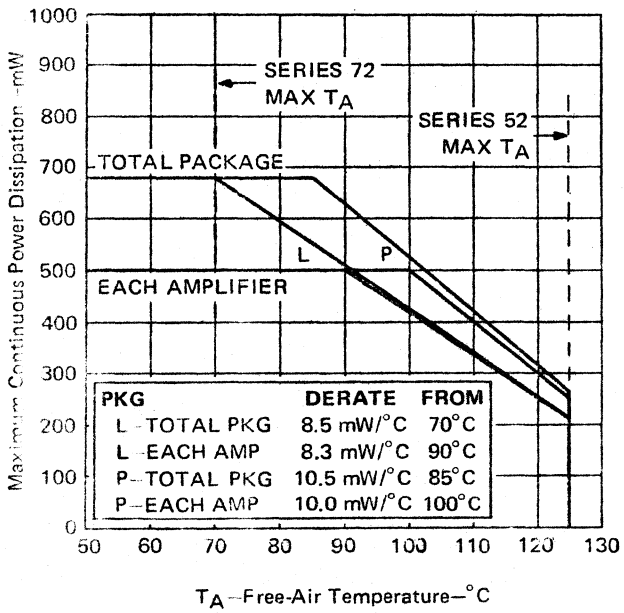
schematic (each amplifier)



COMPONENT VALUES SHOWN ARE NOMINAL

THERMAL INFORMATION

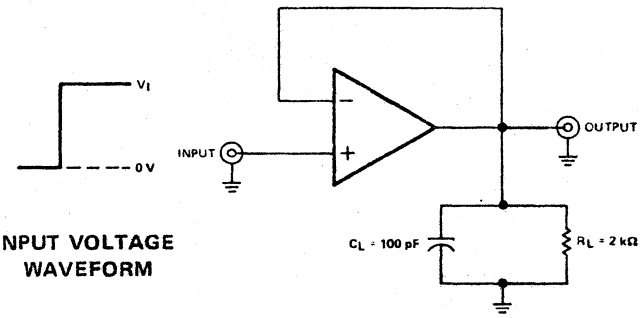
DISSIPATION DERATING CURVE



PKG	DERATE	FROM
L – TOTAL PKG	8.5 mW/°C	70°C
L – EACH AMP	8.3 mW/°C	90°C
P – TOTAL PKG	10.5 mW/°C	85°C
P – EACH AMP	10.0 mW/°C	100°C

FIGURE 1

PARAMETER MEASUREMENT INFORMATION



INPUT VOLTAGE WAVEFORM

TEST CIRCUIT

FIGURE 2–RISE TIME, OVERSHOOT, AND SLEW RATE