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FOX 1

Hardware Overview User's Guide

The information contained in this document is general in nature and not intended for specific application purposes. The Foxboro Company reserves the right to make changes in specifications shown herein and to make product changes at any time without notice or obligation.

HISTORY

Date	Version	Copies	Remarks
12-71	A	800	Original Edition
11-75	B	50	Reprint; new cover, title page, preface

PREFACE

This publication is a comprehensive description of the FOX 1 hardware system and the hardware system components. It can be used as an introductory textbook for hardware system analysts, engineers, and machine-language programmers learning the basic equipment structure and operation. It can also be used as a "quick look-up" reference manual for basic machine functions. Details of hardware logic and maintenance, or software that drives and utilizes the features of the hardware units are not in this book. Details of FOX 1 hardware configuration and operation at the machine-language level are presented here.

This manual presents system overview information describing the FOX 1 hardware components, the system hardware configurations, and the participation of each hardware component in system functions. In general, sections on system hardware components are described in terms of a functional description, physical description, standard and optional features, interface considerations, and specifications.

DOCUMENTATION STRUCTURE

Readers should be aware of the relationship between this document and other books in the FOX 1 anthology, a complete listing of which may be obtained by writing to Systems Technical Marketing Communications, Documentation Control, Dept. 121C, The Foxboro Company.

Pages are assigned a two-part number in which the section number precedes and is separated from the page sequence number by a hyphen. All headings and paragraphs are assigned a two-part number in which the section number precedes and is separated from a sequence number by a decimal point. The span of these numbers is indicated at the top of each page, allowing subjects to be referenced (such as in the index) not only by page, but also by location on a page.

Document information contained herein is preliminary in nature, being printed in advance of exhaustive formal technical and corporate review; it is subject to change without notice.

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INTRODUCTION

Foxboro's FOX 1 Digital Control Computer System (Figure 1-1-1) is a computer-based data acquisition and control system designed specifically for process control applications. The FOX 1 hardware and software modules are designed for console-centered plant-level control of medium to large-scale applications. The FOX 1 is capable of being applied to full depth process control installations including multi-unit control, supervisory control, setpoint control (SPC), and direct digital control (DDC). The FOX 1 system monitors, alarms, logs, and controls the process; executes plant performance calculations; and performs various scientific/economic analyses.

Standard and optional hardware is fully supported by standard software designed for full and direct implementation by process engineers using Fortran IV and a macro processor language called MAX.

Subsequent headings in this section describe the hardware, functions performed, and configurations of the FOX 1 system. The hardware is described by analyzing the system into major subsystems, and discussing the optional and basic standard modular components in each subsystem. The most important part of this section deals with functions performed by the total hardware/software system; or the manner in which the system operates, the capabilities and limitations, and the ways in which it is applied to process control.

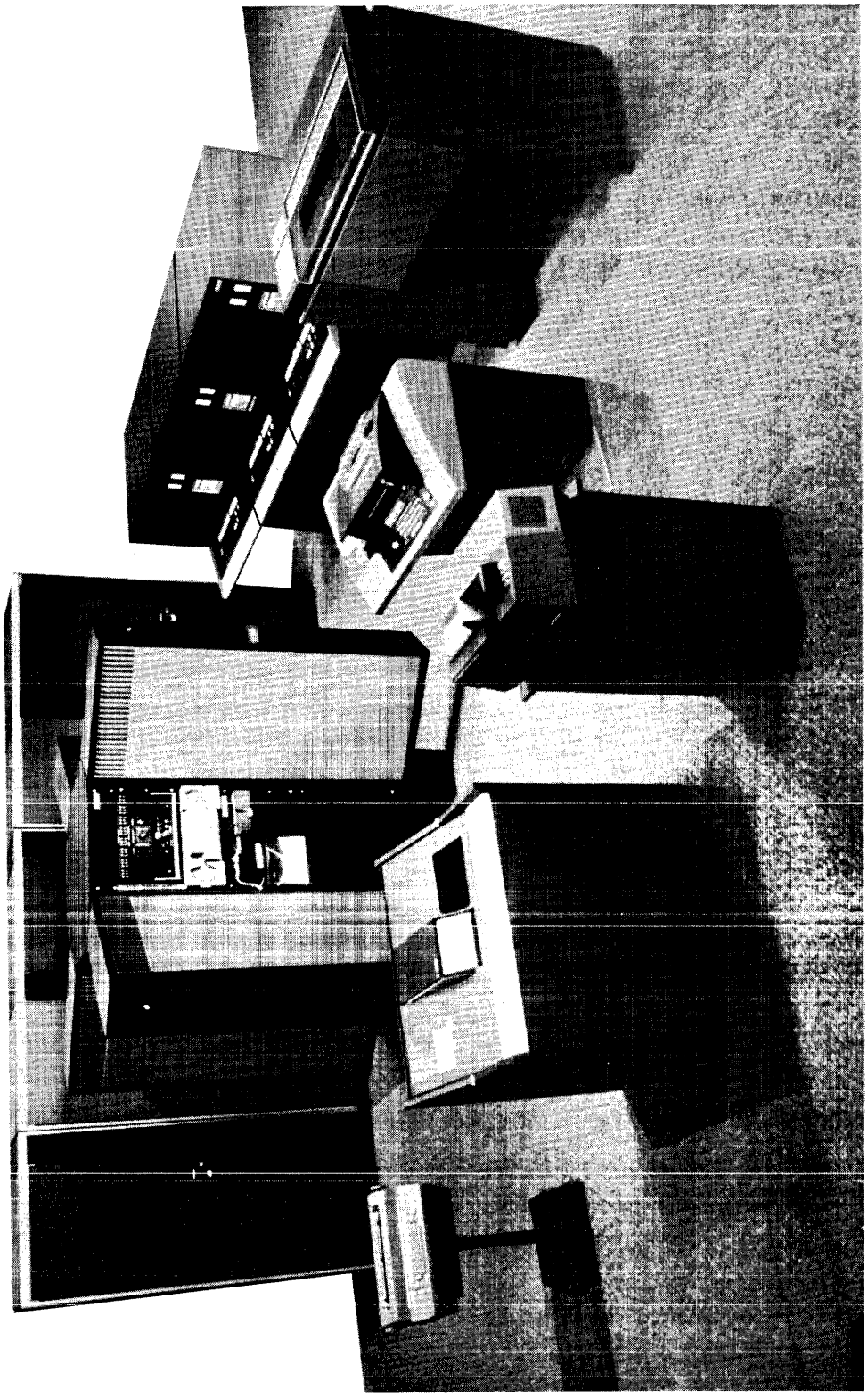


Figure 1-1-1. A Typical FOX 1 System

SYSTEM HARDWARE

The FOX 1 system hardware (Figure 1-1-2) is separated into three major subdivisions: computer elements; process-oriented elements; and computer-peripheral elements. Each of these elementary groups is composed of standard subsystems, functional units, and input/output devices, implemented to the extent or capacity required to fulfill specific system application needs. Therefore, the following discussion of system hardware distinguishes between the "basic standard" equipment required in each FOX 1 system, and "optional" equipment features that might be added to the basic standard to produce a system for use at a specific installation. Optional System components include system hardware not supplied as part of the basic system, but which the basic hardware system can accommodate, and which may be considered for inclusion in the digital process control system.

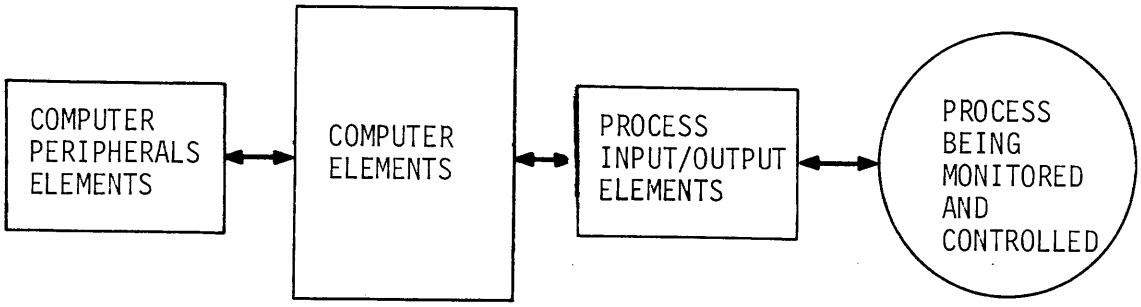


Figure 1-1-2. FOX 1 System Overview

Computer System Components

Computer system components include the following:

- Central Processor/Input Output Unit
- Power Distribution Unit (Optional, but strongly recommended)

Central Processor/Input Output Unit (CP/IO) - The CP/IO unit is the master programmer and control element in the system. It performs all program executions, handles all data storage and transfer operations, and controls all information transfers with other major elements of the system. The primary components of the unit are a central processor, an input/output section, and a core/drum memory.

The central processor is the heart of the FOX 1 process control system to which is associated control software. It is a 24-bit digital computer which handles real time process monitoring and control. Components of the CP/IO unit include:

- Interface Buses
- Maintenance Panel
- Core Memory
- 16 Addressable Registers
- Real Time Clocks
- Drum Memory

The central processor and core memory communicate with external devices through two types of data channels -- programmed IO (PIO) and channel IO (CIO). The processor receives device status information and issues control commands to all IO devices by means of the programmed IO bus. Data may also be transmitted through the PIO bus, which operates in a single-word mode. Character-oriented devices such as the Teletype and paper tape reader/punch use the PIO bus for data transmission.

The channel IO (CIO) facility, on the other hand, operates in a block-transfer mode, transmitting variable-length blocks as data rather than single words. CIO has direct access to memory; it operates independently of the process on a cycle-stealing basis. Thus, data transfers can take place concurrently (in effect) with program execution.

All direct memory access is scheduled by the input/output master, which accommodates up to eight different peripheral and process IO devices. An integral part of the central processor, the IO master controls direct memory access operations on the basis of hardwired priorities established when the system is configured for a particular application.

Power Distribution Unit (PDU) - The power distribution unit is an optional, although strongly recommended, element that provides highly stable 400 Hertz main power and 50/60 Hertz auxiliary power to other units in the FOX 1 hardware system. It consists of a motor-generator set and associated power control panels. Plant power drives the motor and is split into separate, protected circuits providing auxiliary power to various system components. The generator produces 400 Hertz main power that is free of the noise and transients in the plant power. For instance, rotor inertia maintains the main power output during momentary interruptions in the exciter power.

Process-Oriented Components

Process-oriented components include the following:

- Console
- Analog Input Unit
- Digital Input/Output Unit
- Termination Unit (Optional)

Console - The FOX 1 system provides complete, interactive facilities for the operator, programmer, or process engineer to communicate with the system and with the process through the console. Supervisory and control functions as well as program preparation and testing can be accomplished at the console. The primary components of the unit consist of an alpha-numeric keyboard and a graphic (CRT) display.

Analog Input Unit (AIU) - The AIU provides the interface between the CP/IO unit and all inputs from the analog process instrumentation. It selects a specified input signal, converts the analog amplitude to a digital value, and transmits this value to the CP/IO unit.

Digital Input/Output Unit (DIOU) - The DIOU provides interface between the CP/IO unit and all digital process instrumentation; including valve controllers and trend recorders. Field generated digital signals are received by circuits designed to request a program interrupt upon signal detection, to receive status information from contacts, or to serve as pulse counters. Computer generated data are supplied to the field as DIOU outputs in the form of analog signals, solid state digital signals, relay contact operation bits, or valve control pulses.

Termination Units (TU) - Termination units provide an optional alternative to direct termination of field signals at the analog input unit and digital input/output unit. By providing an interposing termination facility between the field signal wiring and both the AIU and the DIOU, termination units can simplify the interface between the process and the FOX 1 system and can reduce the time required to install the FOX 1 system hardware units. Termination units are cabinets of prewired termination panels, containing convenient terminal boards for field wiring and cable connectors to run the field signals to the AIU and DIOU through standard cables.

Computer-Peripheral System Components

Computer-peripheral system components include the following:

- Teletype
- Paper Tape Reader (Optional)
- Paper Tape Punch (Optional)
- Card Reader (Optional)
- Card Punch (Optional)
- Line Printer (Optional)
- Logging Typewriter (Optional)
- Disk Drive (Optional)
- Communications Module (Optional)

Teletypewriter - The teletypewriter is an input/output device designed for bidirectional communications between a programmer and the computer. The device is considered an integral component of the CP/IO unit for use in program development and as a backup device for inoperative peripherals such as typers, paper tape IO, etc. System error messages are printed on this device.

Paper Tape Reader and Punch - These optional, computer-peripheral system components provide input/output information to/from the CP/IO unit. The paper tape reader provides a means of transferring data from punched paper tape to the computer core memory. The paper tape punch provides an output medium for copying information from the computer memory onto punched paper tape.

Card Reader and Punch - Like the paper tape reader and punch, the card reader and punch are optional, computer-peripheral system components

providing similar input/output information services and interface between the CP/IO unit.

Line Printer - The line printer is an optional, computer-peripheral output system component. This device interfaces with the CP/IO unit to provide large and/or frequent on-line program and message printouts. The line printer may also be used for general background data processing operations.

Logging Typewriter - The logging typewriters are optional computer-peripheral output system components used for permanetly recording process logs, plant reports, status and alarm messages, and shift summaries. This device interfaces with the CP/IO unit and may be used as a backup device or alternate for an inoperative line printer or other peripherals, when specified by the system software.

Disk Memory - The disk memory is an optional computer-peripheral system component providing (auxiliary) on-line bulk storage for use by the operating system software. This device is capable of reading and writing process data from the computer core memory in the CP/IO unit. A moving-head disk memory is available as two types of drive: one which provides 831,488 words of storage on a single disk in a removable cartridge; and another which provides the same removable storage, plus an additional 831,448 words on a nonremovable disk. Both disks on the two-disk drive share a common spindle and head mechanism. The disk memory synchronizer, in wing A4 of the CP/IO unit, controls up to four disk drives: each drive may be of either of the two available types. The subsystem is thus configurable to provide from 831,488 to 6,654,904 24-bit words of on-line storage.

Communications Module - The communications module is another optional element in the FOX 1 system hardware providing a communications link of ASCII-coded information between the computer and long-distance and/or local equipment. This module, in wing A4 of the CP/IO unit, provides an interface between external devices and the channel IO and/or programmed IO facilities of the computer. Various organizations of the module are available to service devices in the following classes:

a. Other computers in a multi-computer system such as one containing a supervisory FOX 1 computer linked to several minicomputers; each dedicated to a particular process function.

b. Synchronous or asynchronous communications modems to supply data over land lines to remote stations.

c. Teletype-compatible devices such as plotters, terminals, etc.

SYSTEM FUNCTIONS

The system has a capacity for performing the full range of functions related to process surveillance and control. It can perform control operations such as tuning control loops, changing setpoints, and driving final operators; it performs supervisory operations such as scanning process variable signals, performing process calculations, and producing alarms and logs; it can execute hierarchical tasks such as management reporting, inventory control, and economic evaluation of the plant. System functions outlined here include man/machine interface, process control, process monitoring, logging, alarming, and system security.

Man/Machine Interface

The FOX 1 system provides complete, interactive facilities for the operator or process control engineer to communicate with the system and with the process. These facilities include console keyboards, trend recorders, a teletypewriter, a line printer, logging typewriters, and the visual displays provided by the console.

The consoles provide the key link the the man/machine interface concept. They permit the operator to: interrogate the process for specified parameters, modify specified parameters of control programs, notify the operator of certain alarm conditions, and to initiate specified noncontrol functions such as plant inventories, production planning, sales forecasting, etc.

Multiple consoles can be time-shared between the process loops of a particular plant section, and used simultaneously by operators in different locations. Any loop may be called for display of measurement, setpoint, etc., or to change setpoints, alarm limits, or tuning constants through use of any plant section console(s).

Process Controlling

Process control functions of the FOX 1 system are performed by core resident and drum resident programs. Programs which perform the DDC, SPC, and control panel functions, such as driving the rack-mounted controller stations, are stored on drum and sequenced into core memory by supervisory routines.

During DDC and SPC operations, analog, pulse counting, and contact inputs in the FOX 1 system are scanned, processed, and stored at periodic intervals. These measurements are inserted into control or alarm

algorithms and the results provide signals to position final control elements or to generate alarm messages.

Process Monitoring

To provide the FOX 1 control software with the ability to access live process data and status information in a suitable form, the system utilizes two major process interface units, the AIU and the DIOU (see Figure 1-1-3). The following is a brief description of how these units perform the various process monitoring functions, and how they interface with the central processor.

Analog Input Unit (AIU) - The AIU provides the interface between the CP/IO unit and all inputs from the analog process instrumentation. Its primary functions are to select a specified input signal, convert its analog value to an equivalent digital value, and transmit this value to the CP/IO unit for subsequent processing by the system's scan and control software. Conversion speed is less than 25 us with overall accuracy of ±0.10 percent full scale (except ±0.15 percent full scale ±10mv range). Points are scanned in either a random or sequential mode and can be read through either the programmed or channel IO bus facilities.

Signals from typical field transmitters and other devices used for digital conversion and transmission to the CP/IO unit include:

- Thermocouples
- Resistance Temperature Detectors (RTD's)
- 10 to 50 ma Current Transmitters

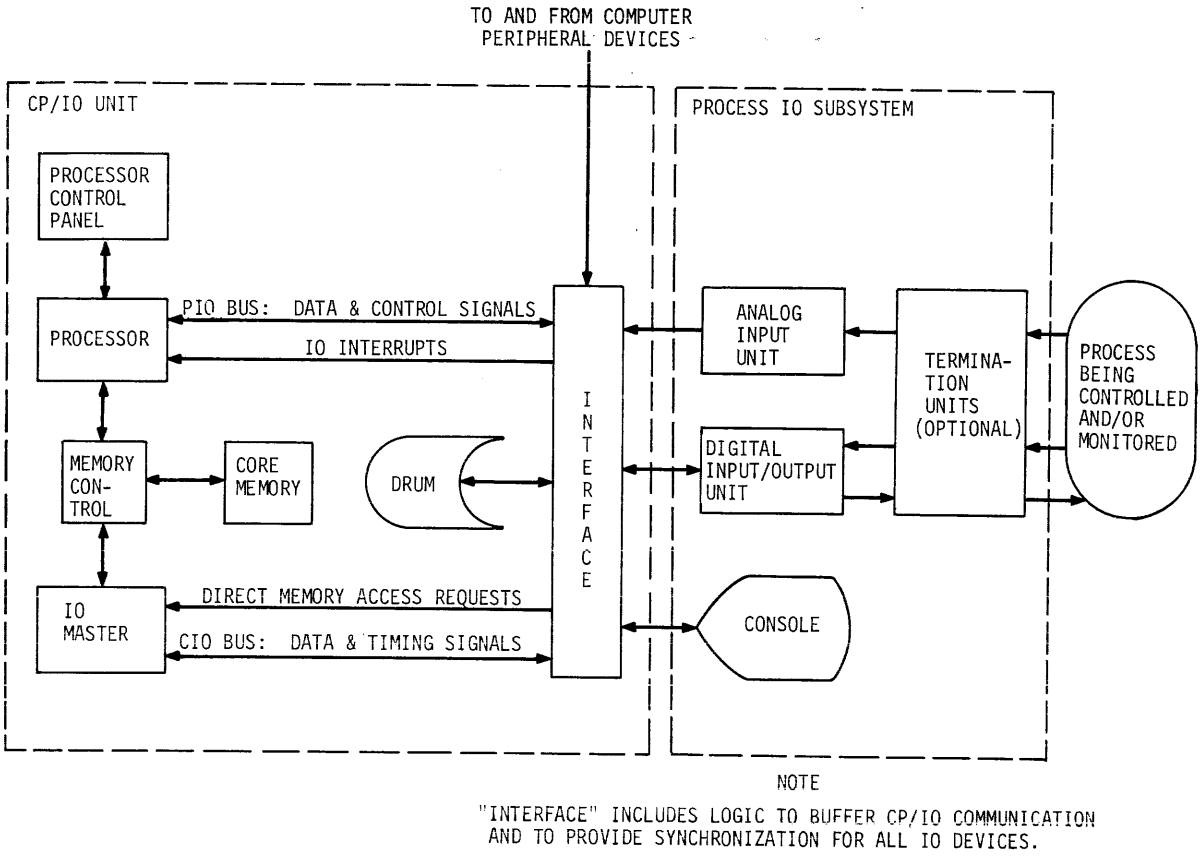


Figure 1-1-3. FOX 1 System Process Interface

- 4 to 20 ma Current Transmitters
- 1 to 5 ma Current Transmitters
- Slide Wires
- Other Miscellaneous Voltage Inputs (within the ranges of 0 to ±10 volts).

Digital Input/Output Unit (DIOU) - The DIOU provides the interface between the CP/IO unit and all digital process instrumentation; and operates the valve controllers and trend recorders. It accepts digital input signals from the process, either status information or field-generated interrupts, and transmits them to the CP/IO unit. The DIOU also senses switches and pushbuttons, transmits drive signals to indicators and trend recorders, and operates DDC and SPC valve controllers.

A summary of the different types of process inputs and outputs transmitted between the DIOU and CP/IO unit include:

- Contact Inputs
- Process Interrupt Inputs (384 maximum)
- Pulse Counter Inputs (100 and 15,000 pps)
- Solid-State Digital Outputs (Steady State and Momentary)
- Relay Outputs (Latching and Nonlatching)
- Analog Outputs (10 to 50 ma, 4 to 20 ma, and 2 to 10 volts)
- Valve Control Outputs

Logging

System logging provides periodic and demand logs in varied formats specified in the software supplied by The Foxboro Company or by user developed programs for specific process control applications. The principal logging device is the Selectric® typewriter. The line printer may be used as an alternate device for logging purposes when specified in the software.

Alarming

The system is designed to detect abnormal conditions in the plant and in the system, and to generate a corresponding alarm signal both visual and

audible to the operator. When an alarm condition is detected, lamps on the CP/IO unit, the console, and/or the controller stations are illuminated. An alarm horn is also sounded at the console, and a message is printed on a logging typewriter or other device.

Visual Indicators - The following backlighted alarm keys and lamps at the console provide visual indication of an alarm condition:

Field Monitor Alarm Lamps - Wired directly to the console, these lamps monitor critical fail-on-open or fail-on-closed field contacts.

CP/IO Monitor Alarm Lamps - Monitored by the central processor under program control, these lamps are both set and reset using a data bit, an address, and a programmed command.

Console Keys - PROCESS ON and PROCESS OFF pushbuttons are illuminated green or red, to indicate the status of the process control system. These keys, along with the CP/IO unit, control the system flunk relay. A yellow light indicates that the CP/IO unit is on scan and capable of control.

Over-Temperature Alarm - Although not considered an alarm device, these thermal switches on the CP/IO, AIU, DIOU, and console energize indicator lights whenever the internal cabinet (bays) or wing temperature exceeds 130 degrees. This corresponds to ambient temperatures of 110 to 120 degrees F.

Audible Indicators - In the console, an alarm horn acts as an audible indicator, and sounds whenever any of the following conditions occur:

- CP Monitor Alarm
- Field Monitor Alarm
- System High Temperature (Over-Temperature Alarm)
- Central Processor Stallout
- Security Calculation Check Error

Alarm Messages - Alarm messages typed on the logging typewriter record function alterations. Such alterations include typeouts for nonalarm functions, including setpoint changes, high and low absolute limit changes, deviation changes, and control status changes.

Specific logging functions may be divided among the Selectric typewriters, when more than one is used in the system, as specified in the software. An alternate Selectric typewriter or any suitable output device (such as the line printer or the teletypewriter) may be designated as a backup device at system generation. Normally, the Teletype is used to print hardware malfunction messages pertaining to the system peripherals.

System Security

System security in the FOX 1 system is accomplished in a variety of ways by the logic circuits in the CP/IO unit. The system security logic is connected to the PIO bus. Also connected to the PIO bus are the synchronizers for the analog input and the digital input/output units, the VCOM (valve control output module) and the logging typewriters. The PIO communication link in the console is connected to logic in the console controller. System security involves both hardware and software.

Hardware Security Features - Hardware security features of the FOX 1 system include:

- Stall Alarm
- Line Power Failure Timer
- Security Check
- Protective Registers
- Processor Control Panel
- Privileged I/O Resources
- Priority Interrupt System
- Analog Input Subsystem Checks
- Valve Control Output Subsystem Checks

Software Security Features - Software security features of the FOX 1 system include:

- Parity Checking
- Program Fences
- Program Traps
- On-Line Exercisers
- Off-Line Diagnostics

System Security Keys - The system security keys in the console enable the user to take appropriate action following a system malfunction. The system is designed so a running program can go to any of three security states during a malfunction (such as red, green, or yellow) by executing PIO instructions and using fixed alarm addresses reserved for this purpose.

Digital Input/Output Unit - This unit initializes all input and output functions to a known state during system turnon and turnoff. The DIOU also reverts to a backup mode of operation during conditions such as system flunk.

SYSTEM CONFIGURATION

Modularity, physical characteristics, and system configuration must be considered if the user plans to modify the FOX 1 to meet specific applications. A detailed description of these factors follows.

Modularity

Modularity permits application of FOX 1 systems to a wide range of industrial processes by varying configurations in the hardware and software on a system and/or unit level. Modularity includes the implementation of both the basic standard equipment and the addition of optional equipment features. This is accomplished in one of three ways:

a. To implement a feature at the printed wiring board (card) level, the card is plugged directly into the nest with which the feature is associated. In all cases the nest will be prewired to accommodate the features.

b. To accommodate variations in I/O count, multiplexer nests (as well as all other nests in the system) are added and connected into the system by standard cables with pluggable connectors at both ends. Only power and ground connections are exceptions to this rule, and these are easily connected to the nest.

c. To expand the system may require the addition of free-standing units. Additional units are implemented into the system with standard system cables. Connector accommodations for these units are provided as part of the basic system.

Configuring a System

Figure 1-1-4 illustrates a FOX 1 hardware configuration (maximum implementation). The basic components required for a minimum system are:

a. A central processor/input output unit (CP/IOU) which includes a central processor (computer), a 16-K word core memory and memory control, a 128-K word drum memory for bulk storage, a programmed input output (PIO) bus for data and control signals, a channel input output (CIO) bus for direct memory access data and timing signals, an IO master (IOM) that controls the CIO bus, and an interface that provides synchronization and control of all equipment using the CIO and PIO buses.

b. A console for keyboard calling and visual display of process data.

c. An analog input unit (AIU) to receive analog process signals, convert them to digital form, and supply the digitized data to the CP/IO unit.

d. A digital input output unit (DIOU) to receive digital process signals for transmittal to the CP/IO unit and to supply analog or digital signals to the field instrumentation under control of the CP/IO unit.

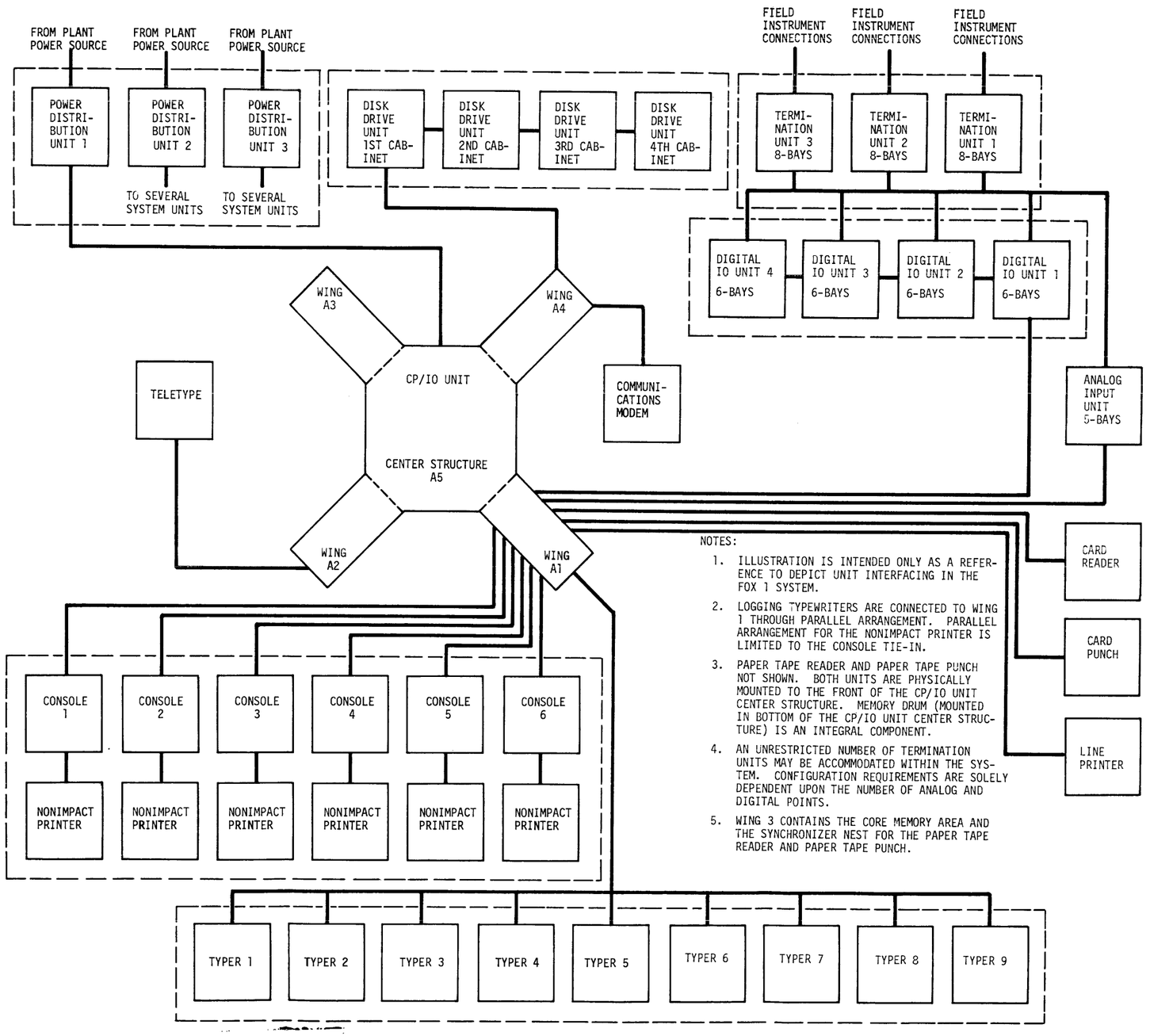


Figure 1-1-4. FOX 1 System - Maximum Configuration

e. Optional peripheral devices, such as paper tape reader, paper tape punch, card reader, card punch, line printer, disk drives, teletypewriter, logging typewriters (IBM Selectric), communications module, etc.

Hardware Physical Characteristics

Details of the system physical characteristics are given in the reference discussions of each unit in this manual and also in the FOX 1 System Installation Guide. These charactistics are summarized as follows:

The system is designed for installation in an environment where the temperature does not exceed 50 to 120 degrees F (10 to 50 degrees C) and where the relative humidity is held between 50 and 95 percent. (NOTE: This does not include vendor-manufactured peripheral equipment. To ensure maximum operating efficiency, the system unit specifications should be consulted.)

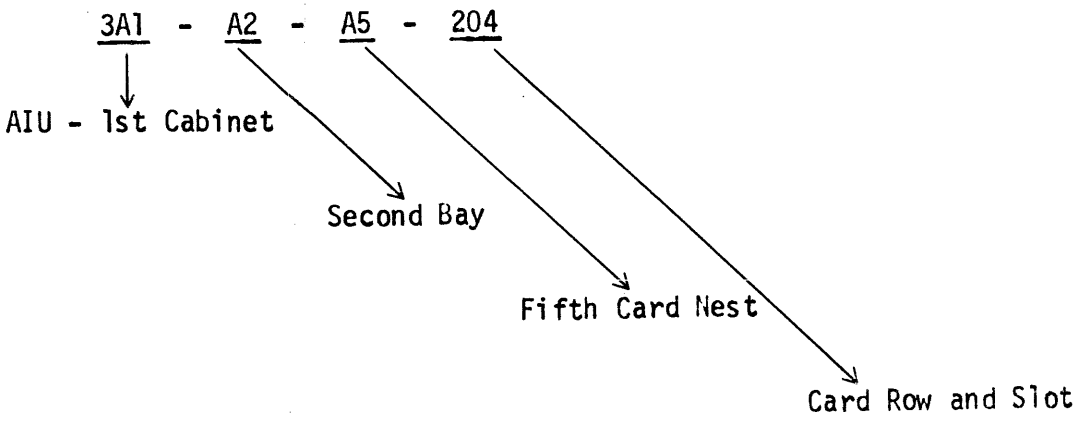
Primary power to operate the system is usually supplied from a single source at the site. This source can be 208-220, 380, or 440 volts at 60 Hertz; or can be 220, 240, 380, or 415 volts at 50 Hertz. Power consumption is quoted on a per-job basis, but is usually less than 15KVA. (Refer to the reference section on the PDU for details.)

Space required for the system depends on many variable factors. Most system units are free-standing; offering both flexibility and modularity, to accommodate site requirements.

Reference Designations - Alphanumeric reference designations are assigned to each major unit, including cabinets, bays, assemblies, subassemblies (such as motors, blower fans, power supplies, printed wiring card nests,

and cables), to the final piece part. Reference designations facilitate the physical identification of each item. That is, each item in the system gears a unique reference designation. Where an item is used more than once, such as cables, the item bears a unique part number and reference designation. The reference designations are stenciled on the equipment (where applicable). They also appear in a number of system drawings and schematics referred to in this manual.

For example, a printed wiring card assigned to the fifth nest housed in the second bay of the analog input unit, would be designated thusly:



A detailed breakdown showing reference designations, is given in the applicable hardware manuals describing the particular unit.

Reference designations for each major unit are:

Central Processor Input/Output	Unit 01
Power Distribution	Unit 02
Digital Input/Output Multiplexer	Unit 03
Analog Input Multiplexer	Unit 04
Console	Unit 05
Typewriter	Unit 06
Teletypewriter	Unit 07

Line Printer	Unit 08
Card Reader	Unit 09
Card Punch	Unit 10
Disk Drive	Unit 11
Nonimpact Printer	Unit 12
Termination	Unit 13

The fact that cables may be identical in every physical detail, including length, necessitates assigning different reference desginations and part numbers. All cables have reference designations marked on both ends, to facilitate system connections. Cables are reference-designated by the letter "W" prefixed to a number.

For example:

W17 signifies a signal cable used in the CP/IO unit.

SECTION 2
CENTRAL PROCESSOR/IO UNIT

SCOPE

This section reviews topics first presented in the FOX 1 System Introduction Manual, extends the discussion of hardware concepts, and describes the functional components of the Central Processor/IO Unit (Figure 1-2-1). The FOX 1 Hardware Reference Manual provides specific information at the machine language programming level. The FOX 1 Theory of Operation Manual provides detailed discussion of the hardware logic.

FUNCTIONAL ELEMENTS

Basic to any computer system are the following functional elements:

a. Memory and associated control logic.
b. Arithmetic unit.
c. IO devices and associated control logic.
d. Overall processor control logic.

The interconnection of these units in a system using low speed input/output devices is illustrated in Figure 1-2-2.

PROCESSOR AND MEMORY CONTROL

In most medium and large scale computers, memory functions as a semi-autonomous unit. Logic external to the memory unit requests a read or write operation, and furnishes address information. Memory unit internal

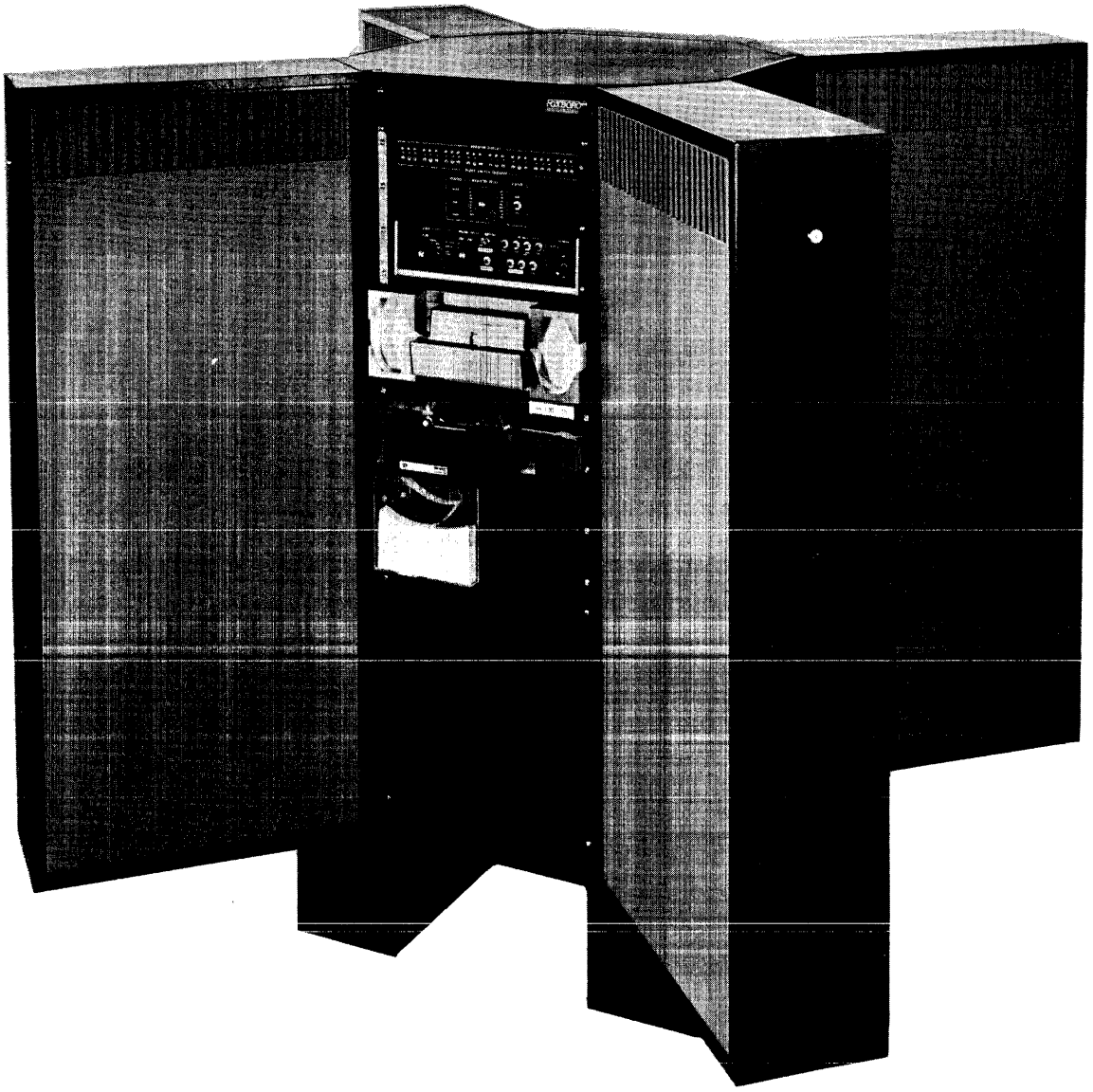


Figure 1-2-1. CP/IO Unit

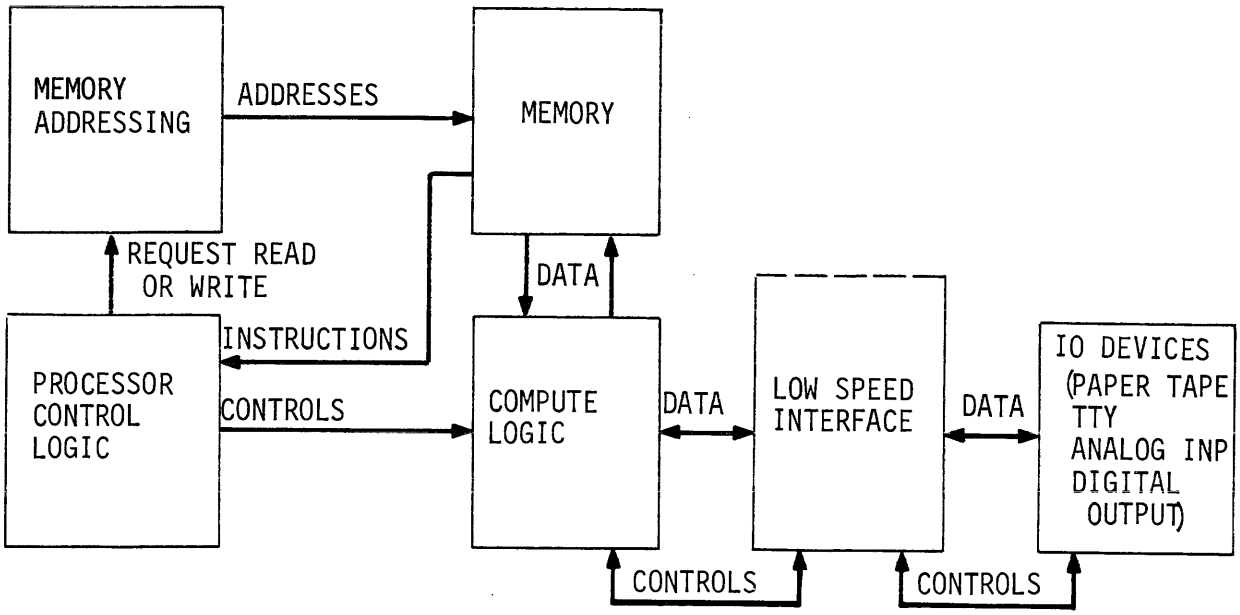


Figure 1-2-2. Typical Basic Computer

logic governs the actual read or write cycle. Processor control fetches and decodes stored instructions, which reference data in memory. The data word is obtained and manipulated in the arithmetic unit at the direction of the processor control logic.

PROGRAMMED IO

The hardware registers of the arithmetic unit provide the path between memory and IO. Since the flow of data through these registers is determined by the program, this interface is called programmed IO. The several devices using programmed IO have "party line" access to data in the processor. That is, only one device can communicate at a time.

DIRECT MEMORY ACCESS

Internal processing speeds of a computer far exceed IO speed. To achieve more efficient use of processor capability, a second IO interface for high speed IO devices can be added, as shown in Figure 1-2-3. IO data is transferred by "stealing" memory cycles from the processor.

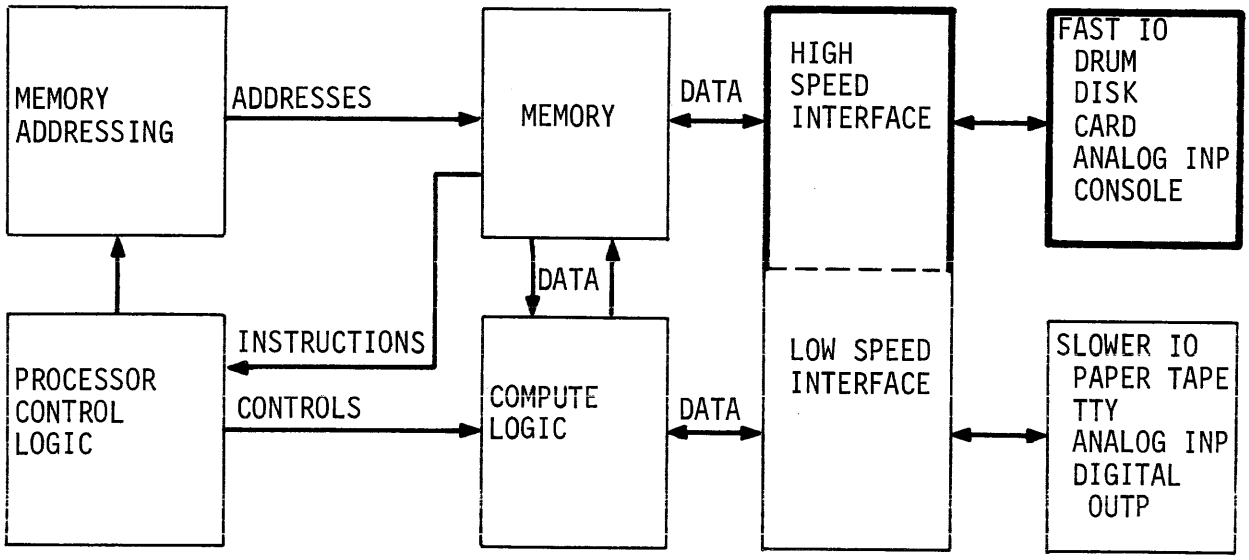


Figure 1-2-3. Basic Computer With Direct Memory Access

CHANNEL IO CONTROL

Bypassing the arithmetic registers relieves the processor from the task of monitoring high speed IO, but introduces the need for additional control logic. The added blocks in Figure 1-2-4 indicate the more elaborate memory interface, the logic for sharing memory cycles, and the IO channel control logic. By providing separate paths, or channels, the channel control logic permits several devices to operate simultaneously, each at its own maximum transfer rate, without affecting one another.

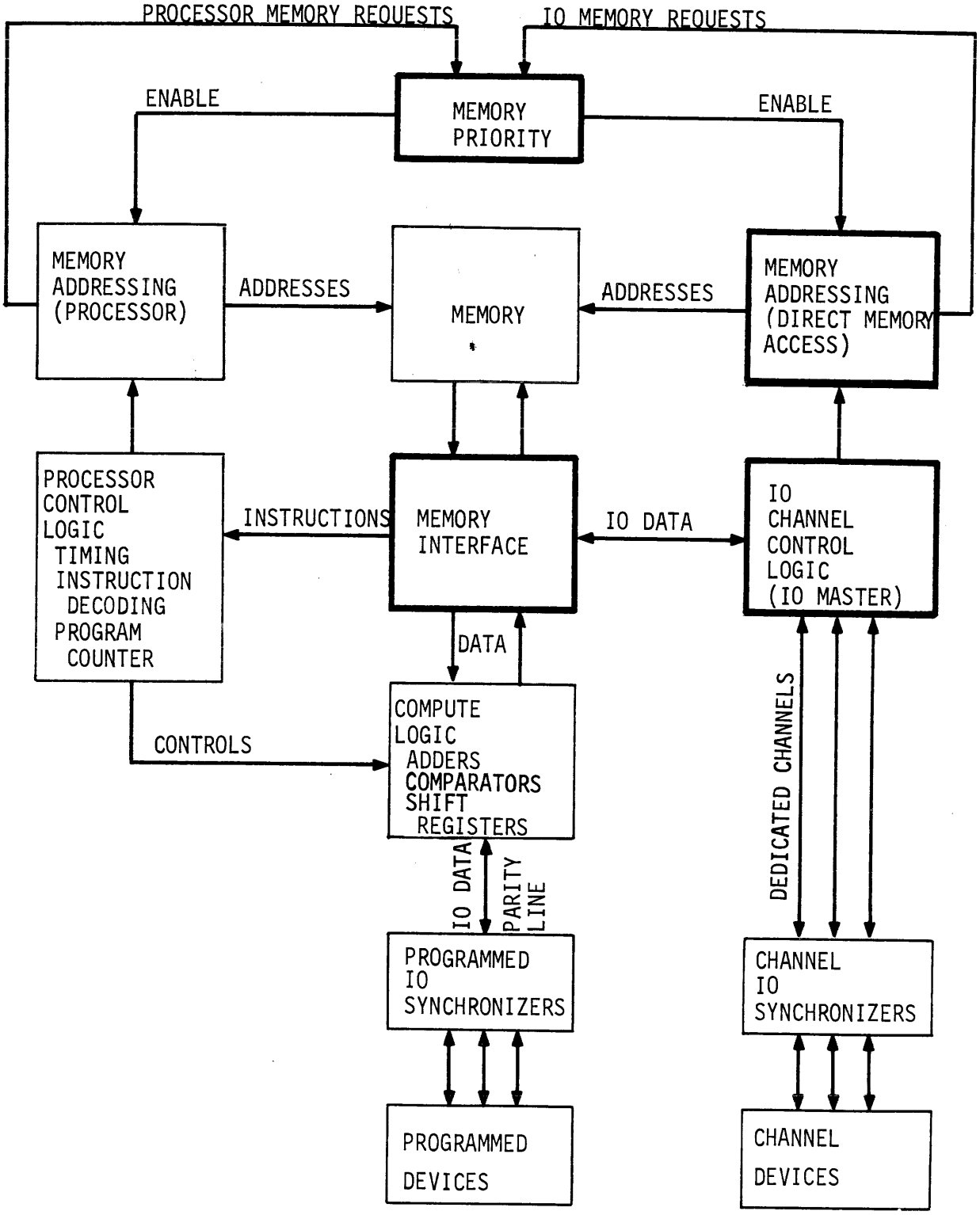


Figure 1-2-4. Computer With Multiple Channel IO

REAL TIME CLOCK

To make the computer useful in process control applications, the program sequence must be regulated in real time. A real time clock in the system, as shown in Figure 1-2-5, operates as an IO device to provide time signals at programmable intervals. The clock signal interrupts a sequence of noncritical (background) instructions for such time-critical (foreground) functions as scanning process instrument inputs.

INTERRUPT SOURCES

A number of other factors dictate exceptions to sequential program execution, as follows:

a. IO requests -- All IO operations require some degree of processor attention. Low speed devices require several instructions to transfer each word through the arithmetic registers. Channel operations must be checked at the end of each block of data.

b. Software requests -- Individual programs in a multiprogramming environment must request blocks of processor time.

c. Hardware requests -- Handling machine or program errors must take precedence over most other functions.

PRIORITY INTERRUPT SYSTEM

A basic computer system might employ a single interrupt level; more elaborate computers provide a number of interrupt levels, giving a predetermined priority to IO, hardware, and software requests for

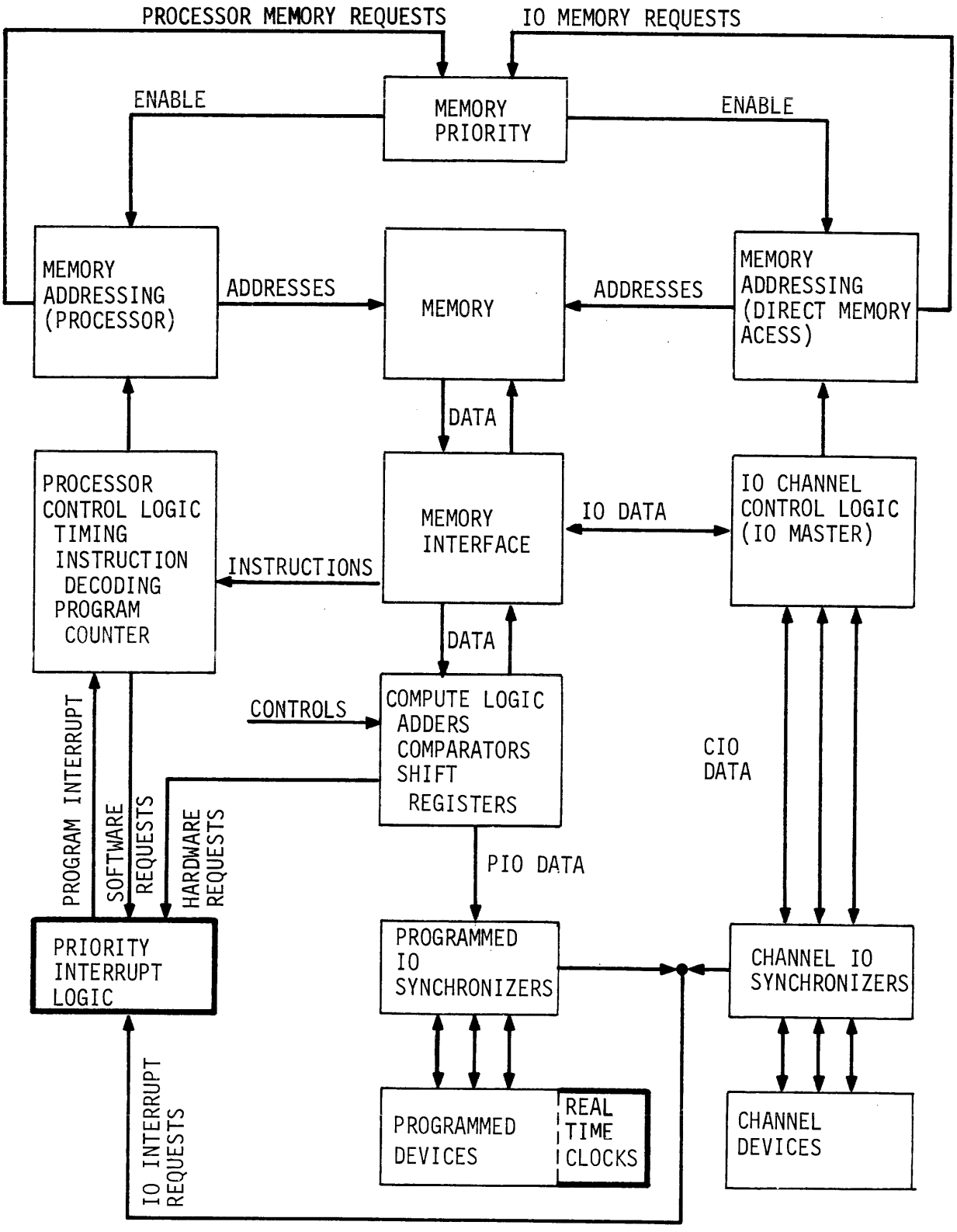


Figure 1-2-5. Computer With Multiprogram Capability

computer time. The interrupt logic block in Figure 1-2-5 weighs the urgency of requests against the importance of the current program, and transmits a program interrupt signal to the processor control logic, if warranted.

SYSTEM SECURITY

The organization of the FOX 1 CP/IO Unit, basically that developed in the last figure, can be reduced to the simplified form shown in Figure 1-2-6.

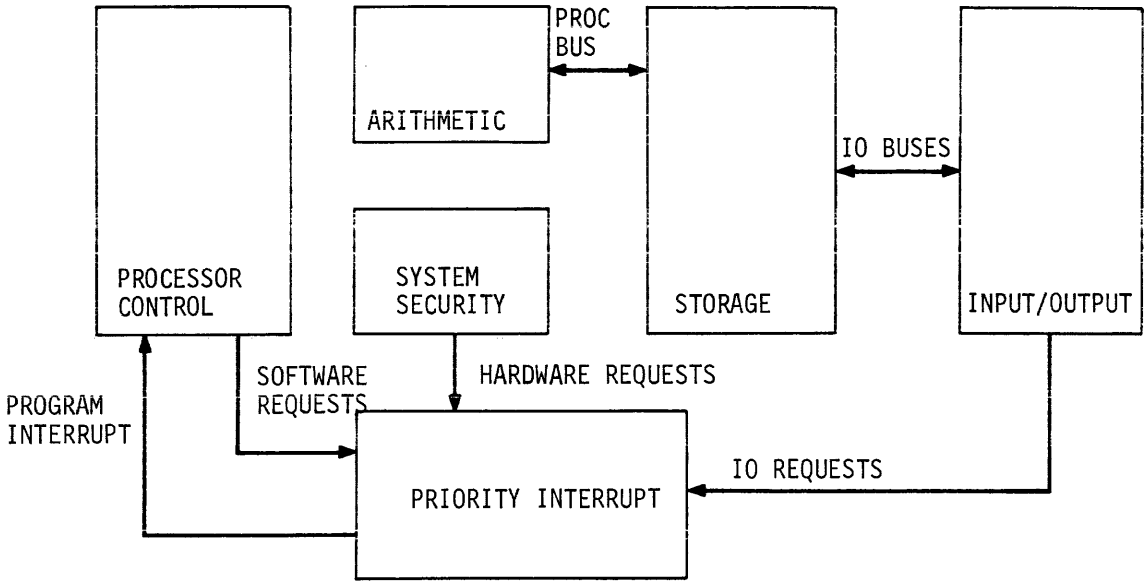


Figure 1-2-6. FOX 1 CP/IO Unit, Simplified Block

Since hardware and software is checked extensively to ensure dependable performance, a block has been added which includes all protective measures under the heading of "system security".

STORAGE

The FOX 1 stores instructions and data in 24-bit words. This word size accommodates the 58 basic operation codes, provides 8 addressing modes and full 32K addressing capability, and is more than adequate to represent the number range of process control data. Word-parallel buses transfer instructions and data from storage to processing registers and IO devices.

A crucial requirement for a computer to be used in plant control is fast access and processing of critical data, and moderately fast access to large quantities of noncritical data. The FOX 1 provides balanced speed and capacity at the following levels:

a. Sixteen addressable hardware registers accessible within a 320 nanosecond basic processing interval.

b. Core main storage of 16K, 24K, or 32K with a 960 nanosecond full cycle time.

c. Magnetic drum bulk storage of 256K or 512K with an average initial access time of 8.3 milliseconds (at 60 Hz power input) and a continuous transfer rate of one word every 15.2 microseconds (up to 1024 words).

Data for controlling the program currently being executed, and information for immediate input to the arithmetic unit is contained in hardware registers. The program and its data and subroutines are retained in core memory. The operating system and several other programs are also present in core, the exact number depending upon the core capacity and the size of the programs. But, obviously, even the maximum of 32K core storage cannot hold all FOX 1 system programs. The drum,

with 8 to 32 times the capacity of core forms a reservoir of programs and data for transfer to core as the need for them arises.

HARDWARE REGISTER STORAGE

The hardware registers provide the fastest access time in the FOX 1 storage heirarchy. Data is readily moved between registers, compared, altered in the arithmetic unit, or manipulated within the arithmetic registers within the 320 nanosecond basic processing interval. This speed and flexibility is attained through the use of double rank logic circuits. Dual flip-flops, such as shown in Figure 1-2-7, isolate the register output from its input switching logic.

Sixteen of the processor's hardware registers are addressable. The addressable registers perform three functions: address modification, program control, and arithmetic. The address registers have a 15-bit capacity, control registers range from 5-bits to 24-bits, and the arithmetic registers hold 24-bits. The arithmetic registers can be used in pairs to extend their effective capacity to 48 bits for double word operations. Addressable and nonaddressable registers and their functions are listed in Table 1-2-1 and 1-2-2, respectively.

CORE STORAGE

Core is the main storage medium of the FOX 1 computer. The basic storage configuration consists of one module having 16K capacity. A second module can be added to provide an additional 8K or 16K. Each memory module consists of a 2 1/2 D core array with three-wire control -- X and Y address lines plus sense windings. Duplicate timing and selection logic make the two modules completely independent of each other. A fifteen bit addressing system can select any location in the 32K maximum

Table 1-2-1. Addressable Registers*

NAME	MNE-MONIC	SIZE (BITS)	ADDRESS	SAVED ON INTER-RUPT	PROTECTION	USED FOR ADDR MOD	FUNCTION
Address Stop - Lower	ASL	19	77760	No	TCP		Upper address limit of protected area, single word resolution. Also, four selectable classes of protection. Selected operations not allowed inside protected area.
Address Stop - Upper	ASU	15	77761	No	TCP		Lower address limit of protected area.
Index Executive	XE	15	77762	No	RMP	X	Base reference for operating system data.
Word Switch	WSR	24	77763	No	Read Only		Read only hardware toggle switches for manual entry and program control.
Software Interrupt Status	SIS	24	77764	No	RMP, SIP		Stores software interrupt requests.
Central Processor Status	CPS	16	77765	No	RMP		Stores hardware interrupt requests.
Memory Fence	FNC	24	77766	Yes	RMP		Divided into high and low limits, 8 word resolution. Instruction fetch or write operation should be inside fence limits.
Privilege and Level	PL	24	77767	Yes	RMP, SPL		IO and register usage privileges, address stop enable, instruction fetch address check, program priority.
Program Counter	PC	15	77770	Yes	None	X	Base reference for instructions in relocatable programs.
Index Common	XC	15	77771	Yes	None	X	Base reference for data common area.
Index Top-of-Stack	XT	15	77772	Yes	None	X	Base reference for subroutine linkage.
Index B	XB	15	77773	Yes	None	X	Pre-indirect or general index; post index if used alone.
Index A	XA	15	77774	Yes	None	X	Post-indirect or general index.
Accumulator (Arithmetic Register)	A	24	77775	Yes	None		Input (together with B register) to arithmetic adder; arithmetic result.
Arithmetic Extender	E	24	77776	Yes	None		Double precision arithmetic or double word storage; extends arithmetic result.
Central Processor Indicator	CPI	5	77777	Yes	None		Stores status resulting from floating point and byte operations; does not cause interrupt.

*All addressable registers connect to the central processor bus (CPB).

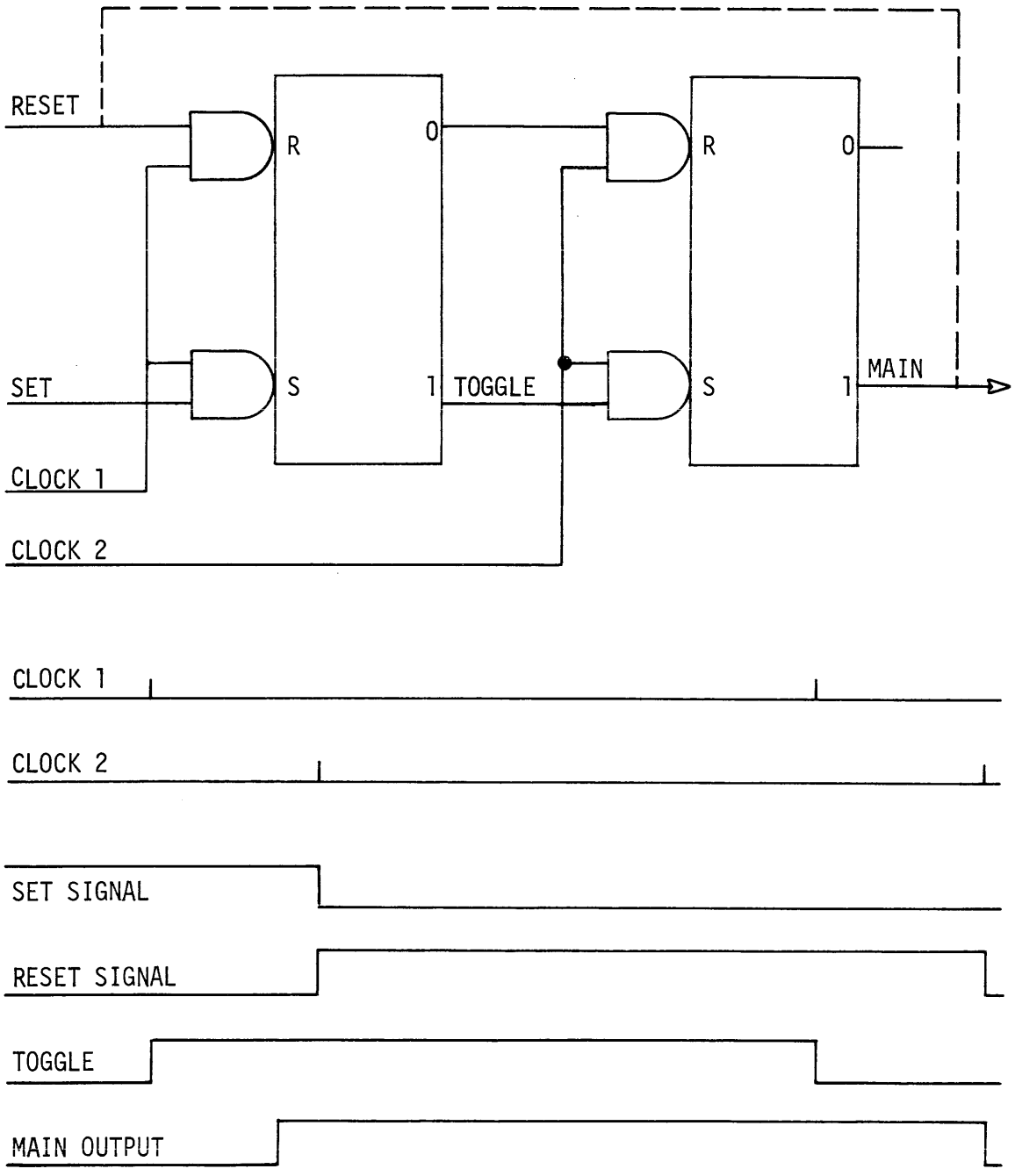


Figure 1-2-7. Dual Rank Flip-Flop

Table 1-2-2. Nonaddressable Registers

REGISTER	USE	SYSTEM BUS	CENTRAL PROCES-SOR BUS	INTER-RUPT BUS
Instruction	Operation code, addressing mode, indirect and indexing bits, absolute address or displacement.	X	X	
Shift Counter	Secondary operation code (2 word instructions) or shift count.	X	X	
B	Operands.	X	X	
T	Double precision or double word operands.			
Effective Address	Address arithmetic result register, provides processor memory address to core.		X	
Interrupt Matrix	Receives interrupt requests from all sources.			X

configuration. One address bit selects the first or second module (lower or upper 16K), and fourteen bits address the desired word within the modules.

The single port core memory is shared on a priority basis between the processor and the channel IO. A memory cycle can be initiated by either. Separate requests for a memory cycle are handled as received, but the channel IO is given priority when simultaneous requests are made.

The start of each memory cycle is synchronized with the processor clock, but the 960 nanosecond full cycle timing is controlled by an internal delay line. Because ferrite core readout destroys the stored data, a read operation must also rewrite the original word of data. This is

known as read and restore. Conversely, a write operation must clear the location (by reading) before entering new data. This operation is a clear and write. Internally, every memory cycle consists of a 500 nanosecond read portion and a 460 nanosecond write portion, but to the external user -- the processor or the channel IO -- the entire 960 nanosecond cycle is either a read or a write operation.

A parity bit is added to the 24 data bits -- as needed to maintain an even number of one bits in the word -- whenever a word is written into memory. Parity is checked at the memory interface whenever a word is read, but the parity bit is not transmitted to the processor registers or the IO master.

Forty-eight words of core are dedicated as shown in Figure 1-2-8 to four types of data storage:

a. Interrupt vectors.
b. Channel IO control addresses.
c. Floating point temporary storage.
d. Hardware trap vectors.

Hardware register addresses are fixed as 77760_8 through 77777_8 for all processors. In a maximum memory configuration, hardware register addresses supercede the last 16 core addresses.

DRUM STORAGE

The magnetic drum is available with a basic capacity of 256 tracks, or an optional 512 tracks, with each track storing 1024 words. Each track is divided into 1100 sectors, with information stored serial-by-bit in the tracks at a density of 30 bits per sector. A guard bit marks the beginning of each sector, and four data synchronizing bits precede the 24

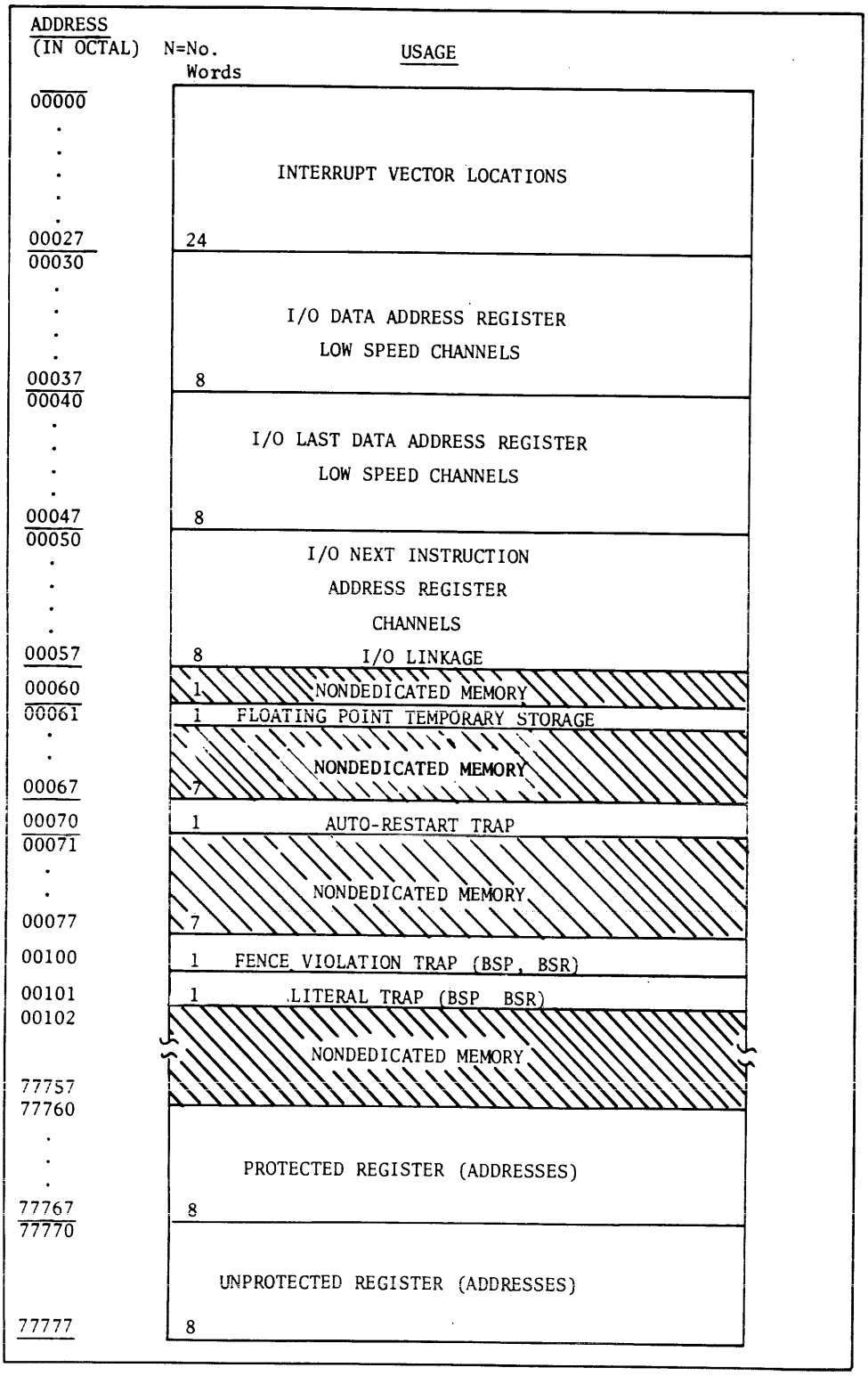


Figure 1-2-8. Dedicated Memory Allocation

data bits. A parity bit is written -- either a logical one or zero, as needed to maintain an even number of one bits in the word -- after the last data bit. Parity is checked at the drum interface whenever a word is read, but the parity bit is not transmitted to the central processor.

Drum speed is nominally 3600 rpm at 60 Hz input to the drive motor, or 3000 rpm with a 50 Hz input. Design allows up to four percent reduction in speed without detriment to operation. The interval for one revolution (at nominal speed) equals 16.7 milliseconds at 60 Hz or 20.0 milliseconds at 50 Hz. Average initial access time, therefore, approximates 8.3 milliseconds or 10.0 milliseconds, and continuous data are available at 15.2 microseconds per word or 18.1 microseconds per word. The interval between tracks is approximately 1.2 milliseconds at 60 Hz or 1.4 milliseconds at 50 Hz. To fill the maximum 32K memory from the drum takes from 531 to 555 milliseconds at 60 Hz (high and low limits of drum speed, respectively).

Two types of addressing are required to access a given word, static and dynamic. Since the drum is constructed with a head for each track, static selection picks the head corresponding to the desired track. Dynamic selection requires locating the proper sector on the revolving surface. Pulses read from permanently recorded timing tracks drive a counter and associated logic which indicates the physical position of the drum. Dynamic addressing is accomplished by obtaining coincidence between the sector counter and the desired sector address.

Data transfer may be any size from a single word to a full track, but each read or write command must end by word 1023 -- there is no automatic switching from track to track. However, each track includes 76 unused sectors of 30 bits each. These 2280 bits maintain synchronization between timing and data tracks for the interval between the last address of one track and the first address of the next. The program has approximately one millisecond to select another track or to change from

read to write. Delay beyond one millisecond means losing the first sector and requires waiting approximately 17 milliseconds for a complete drum revolution.

Drum track zero is dedicated to the storage of the hardware bootstrap and loader programs. A LOAD BOOTS switch on the processor control panel initiates a hardware controlled read from track zero. The bootstrap program contains instructions needed to read in other programs for system startup. Accidental erasure of this permanent information is prevented by a pair of interlock pushbuttons (WRITE BOOTS) which must be pressed to permit a program to write on track zero.

PROCESSOR CONTROL

Overall control of processor data flow is accomplished through a matrix of sequence states and operational states: timed sequence counter outputs are interpreted according to the pattern of a selected operational state.

MAJOR STATES

The processor progresses through three operational states for each instruction that is performed:

a. Instruction Access.
b. Address Modification (operand access).
c. Instruction Execution.

Each of the first two major states has one sequence counter associated with it. The instruction execution operational state has eight sequence counters, each associated with a group of functionally related

instructions. The coding of the word in the instruction register selects the appropriate execution sequence counter for use in the execution state.

Instruction Access State

Just prior to the beginning of the instruction access state, the contents of the program counter are transferred to the effective address register to read a memory word into the instruction register. After the instruction operand has been read, the value in the program counter is incremented by one (in the address modification state) to point to the memory location of the next instruction in sequence.

The instruction word, shown in Figure 1-2-9 (a), is composed of three elements: an operation code, a mode identifier, and an address field. A six bit operation code provides 64 possible operations, of which the 58 assigned are listed in Table 1-2-3. The three-bit mode identifier determines the significance of the address field contents.

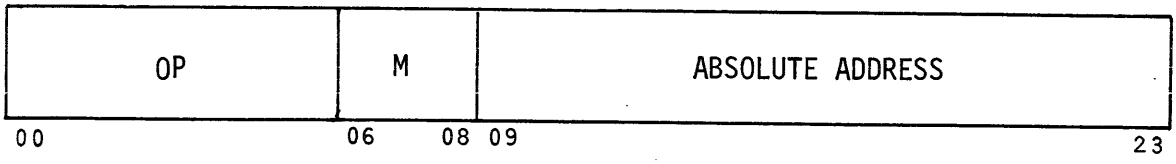
The format of the second word of two-word instructions (BIT, CWM, MOV) is similar to that of the first, except that a secondary control field occupies the place of the operation code. A complete operational state sequence -- access, modify, and execute -- is required for each instruction word. The first execute state merely stores significant fields from the first operand. The second instruction access is modified to read the secondary operation control field into the shift counter, while retaining the original operation code in the instruction register.

The instruction word address field has three principal interpretations:

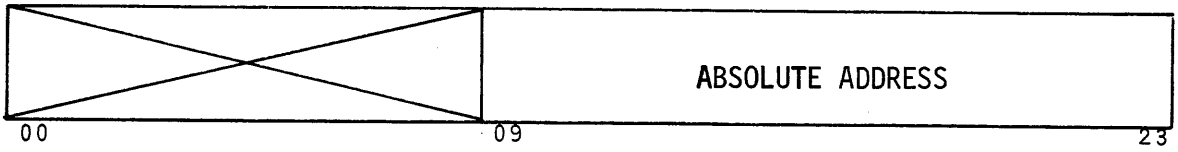
a. A literal address or operand.

A.

ABSOLUTE
INSTRUCTION

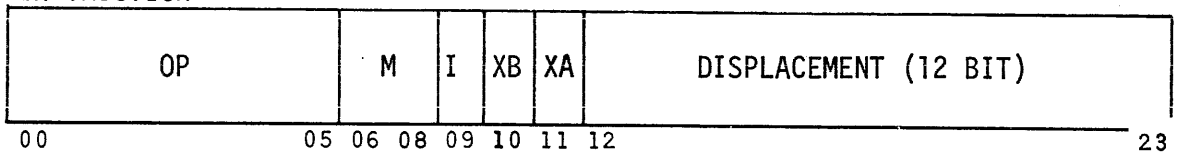


ABSOLUTE
VECTOR

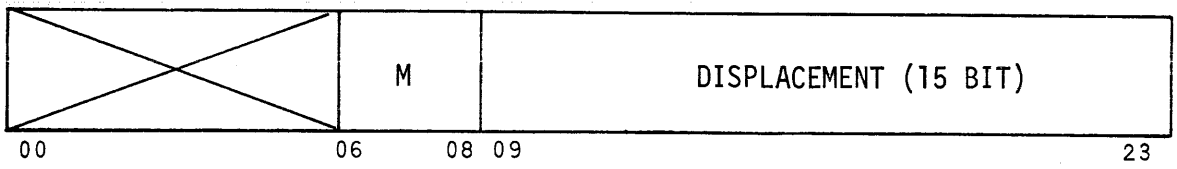


B.

RELATIVE
INSTRUCTION



RELATIVE
VECTOR



KEY

OP = OPERATION CODE
M = ADDRESSING MODE
I = INDIRECT BIT
XB = INDEX B REG
XA = INDEX A REG

Figure 1-2-9. Address Formats

Table 1-2-3. FOX 1 Instruction Summary

FUNCTIONAL SUMMARY	INSTRUCTION NAMES	MNEMONICS
ARITHMETIC OPERATIONS		
1. Fixed point binary arithmetic -- add or subtract, using single or double word data; multiply, which yields a double word product; and divide, which yields a single word quotient.	ADD; ADD LONG SUBTRACT ; SUBTRACT LONG MULTIPLY DIVIDE	ADD; ADL SUB; SBL MPY DIV
2. Boolean functions -- AND, OR, exclusive OR.	LOGICAL AND INCLUSIVE OR; EXCLUSIVE OR	AND IOR; XOR
DATA MANIPULATION AND TESTING		
1. Shift operations -- Arithmetic shifts, which retain the original sign; logical shifts and rotation, which treat words as 24 bits unsigned; and normalize instructions. All have single or double word capability.	SHIFT NORMALIZE SHORT: NORMALIZE LONG ROTATE LEFT E REGISTER	SHF NMS; NML RLE
2. Byte Manipulation -- Using two independently variable length fields (bytes), this group of instructions can perform any of eight functions as follows: Load or Load Complement Add or Subtract AND, OR, Exclusive OR, or Exclusive OR NOT Accumulator right justified operation can be specified. Additional micro-coding permits testing for byte zero, byte overflow, and byte parity with or without changing the contents of the accumulator, and permits binary operation of the byte status indicators (as in generating and checking parity).	BYTE MANIPULATION	BYT
3. Bit Manipulation -- A set of instructions that select an individual bit for test, and may also set, reset, or complement it. The instruction may be coded to initiate a skip on either the set or reset condition of the bit.	BIT MANIPULATION	BIT
4. Memory Count Decrement -- An instruction that decrements a 24-bit count in memory by one each time the instruction is executed, and initiates a program skip when the count reaches zero.	DECREMENT MEMORY	DEM

Table 1-2-3. FOX 1 Instruction Summary (contd)

FUNCTIONAL SUMMARY	INSTRUCTION NAMES	MNEMONICS
TESTING ARITHMETIC AND LOGIC CONDITION		
1. Memory comparison -- Compares A or E, or A and E double word against memory operand for sign analysis or value comparison, and skips or branches if the tested condition is true. Includes a three-way test for high, low, or equal condition in a single instruction. The program branches, skips, or continues in sequence based on the results of the comparison.	COMPARE WITH MEMORY	CWM
2. Arithmetic result test -- Instructions to branch on negative or zero results.	BRANCH IF REGISTER A IS NEGATIVE BRANCH IF REGISTER A IS ZERO	BRN BRZ
DATA MOVEMENT		
1. Load instructions -- A single word of data or its complement can be loaded into either the A or E register, or a double word can be loaded into the combined A,E.	LOAD A REGISTER; LOAD E REGISTER LOAD LOGICAL COMPLEMENT; LOAD LONG	LDA; LDE LLC; LDL
2. Store -- A single word of data can be stored into memory from either the A or E register, or a double word from the combined A, E. The contents of the A register can be exchanged with the contents of a memory location. The contents of the A register can be stored under control of a mask word contained in the E register.	STORE A REGISTER; STORE E REGISTER STORE LONG EXCHANGE A REGISTER WITH MEMORY MASKED STORE	STA; STE STL EAM MST
3. Multiple Move -- A variable length record of up to 64 words from one location can be duplicated, starting in a designated memory location.	MOVE MULTIPLE	MOV
4. Program initiated IO -- Read or write either data or status information on a word at a time basis with character oriented IO devices, or initiate a multiple word transfer on high speed devices controlled by the IO master. Each instruction includes the option to initiate a program skip if the command is accepted. Includes an instruction to determine which device on an interrupt level has requested an interrupt. The read status instructions include an option to clear status after reading.	PROGRAMMED INPUT/OUTPUT	PIO

Table 1-2-3. FOX 1 Instruction Summary (contd)

FUNCTIONAL SUMMARY	INSTRUCTION NAMES	MNEMONICS
ADDRESS MANIPULATION		
1. Generate absolute address -- An instruction to generate a fifteen bit address from a base and an absolute displacement. Generates absolute addresses required for channel IO, interrupt, and auto-restart vectors, and for fence and literal trap vectors.	GENERATE EFFECTIVE ADDRESS	GEA
2. Indexing -- Either of two index registers can be addressed to perform the following functions:		
Load or Store	LOAD XA; LOAD XB	LXA; LXB
	STORE XA; STORE XB	SXA; SXB
Add or Subtract	ADD TO XA; ADD TO XB	AXA; AXB
Compare and skip if index > operand, no action if not.	COMPARE XA AND SKIP	CXA
	COMPARE XB AND SKIP	CXB
Test and increment index if index < operand, clear and skip if not.	TEST AND INCREMENT XA	TIA
	TEST AND INCREMENT XB	TIB
Branch and decrement index if index ≠ zero, no action if equal to zero.	BRANCH AND DECREMENT XA	BDA
	BRANCH AND DECREMENT XB	BDB
PROGRAM SEQUENCE CONTROL		
An absolute or unconditional branch. Special branches that store a return vector for use in subroutine call, and two branches that pick up the vector for return from interrupt or subroutine. An instruction to change program priority and operating privileges. An instruction to exit to hardware interrupt level zero, or if already at that level, to stop program execution.	BRANCH UNCONDITIONAL	BRU
	BRANCH AND SAVE PLACE	BSP
	BRANCH AND SAVE REGION	BSR
	RETURN FROM INTERRUPT	RFI
	SET PRIORITY LEVEL	SPL
	HALT	HLT
FLOATING POINT ARITHMETIC		
Optional floating point hardware add, subtract, multiply, or divide, using either a single or a double word memory operand, and an instruction to store the result as a truncated normalized value in a single (word) location in memory.	FLOATING ADD SHORT	FAS
	FLOATING SUBTRACT SHORT	FSS
	FLOATING MULTIPLY SHORT	FMS
	FLOATING DIVIDE SHORT	FDS
	FLOATING ADD LONG	FAL
	FLOATING SUBTRACT LONG	FSL
	FLOATING MULTIPLY LONG	FML
	FLOATING DIVIDE LONG	FDL
	STORE NORMALIZED AND ROUNDED	SNR

b. An absolute address.

(1) Absolute direct
(2) Absolute indirect

c. A relative address.

(1) Relative direct
(2) Relative indirect

Address Modification State

In addition to the operation code obtained in the instruction access state, in most cases an operand is obtained by another memory read operation (memory operand access). A memory read requires inserting a value in the effective address register. This effective address is derived in one of the addressing sequences charted in Table 1-2-4 and companion Figures 1-2-9 and 1-2-10. The table and figure titled Address Modification are correlated by reference letters.

Memory Operand Access - Except in two instances, instructions require a memory operand access. In the first exception, store instructions, the operand is already in the register implied by the operation code (A register for Store A, E register for Store E). Branch instructions are the second exception. The address modification state is completed for branch or store instructions when a final address is placed in the effective address register. Instructions written in the literal mode include the operand as part of the instruction word.

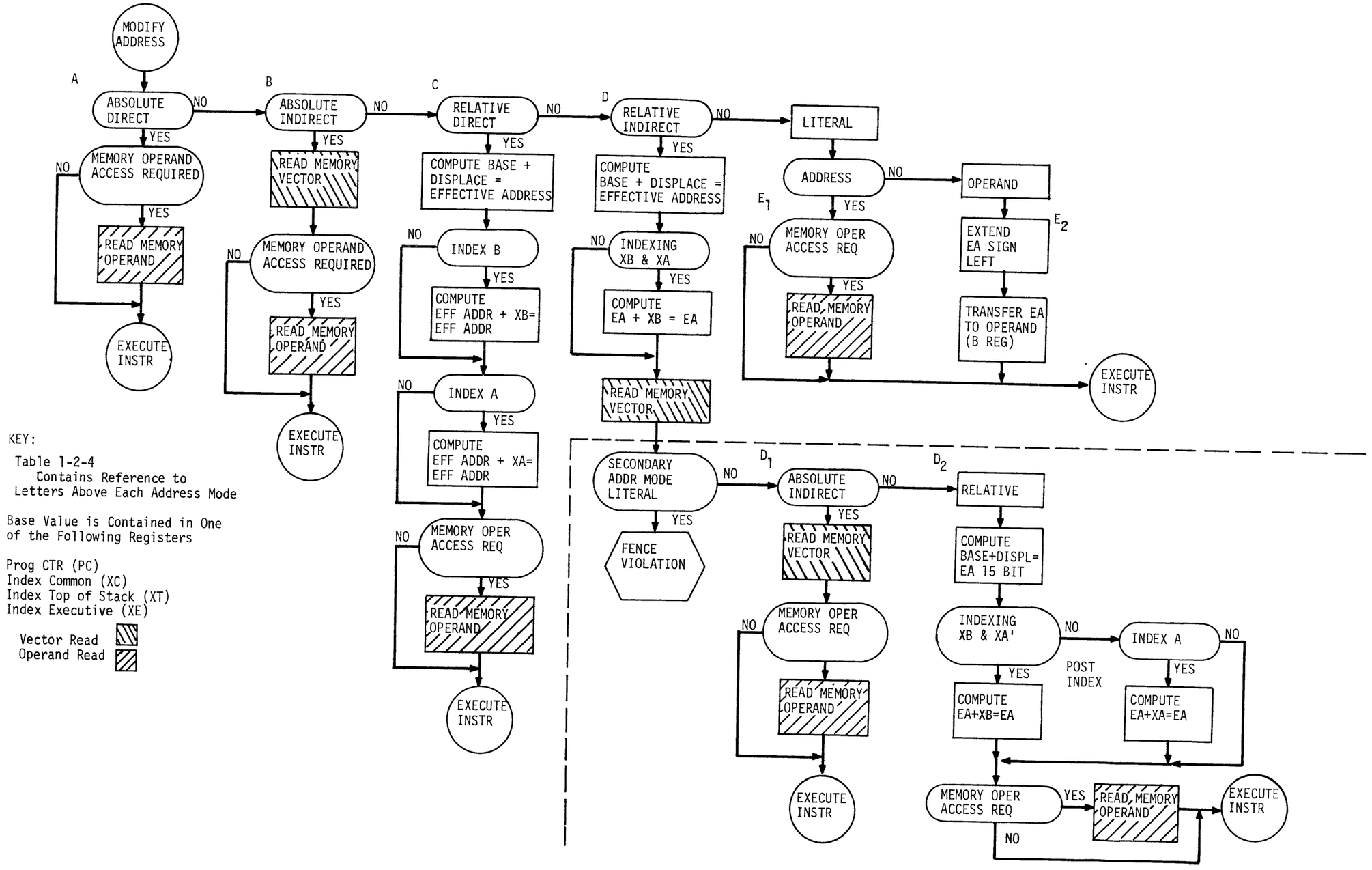
Table 1-2-4. Address Modification

DIAG REF	ADDRESS TYPE	SEQUENCE
A	Absolute Direct	Absolute address field used to read operand from memory[1].
B	Absolute Indirect	1. Absolute address field used to read absolute indirect vector from memory. 2. Address field from absolute indirect vector used to read operand from memory[1].
C	Relative Direct	1. Compute effective address a. Displacement field value added to contents of base register designated in mode field. b. If either index bit is set, value in corresponding register is added to previous total. 2. Effective address is used to read operand from memory[1].
D	Relative Indirect	1. Compute effective address a. Displacement field value added to contents of base register designated in mode field. b. If both index bits are set, add index B value to previous total as pre-indirect index. 2. Effective address is used to read relative indirect vector from memory.
D_1	Secondary Absolute Indirect	Same as B
D_2	Secondary Relative Direct	1. Compute effective address a. Displacement field value added to contents of base register designated in secondary mode field.

Table 1-2-4. Address Modification (contd)

DIAG REF	ADDRESS TYPE	SEQUENCE
		b. Post indirect indexing as determined from original instruction index bits: (1) Index A only, add value in index A (2) Index A and index B, add value in index B 2. Effective address is used to read operand from memory[1].
E_1	Literal Address	Absolute address field is used to read operand from memory[1].
E_2	Literal Operand	Absolute address field is transferred to operand (B) register, and bit 9, sign bit, is propogated leftward through position 0.

[1]Memory read operation omitted for address-only instructions such as Branch or Store.



KEY:

Table 1-2-4
Contains Reference to
Letters Above Each Address Mode

Base Value is Contained in One of the Following Registers

Prog CTR (PC)
Index Common (XC)
Index Top of Stack (XT)
Index Executive (XE)

Vector Read
Operand Read

Figure 1-2-10. Address Modification

Instruction Execution State

The instruction execution state begins with an operand already in the B register, or an effective address already computed. The duration of the execution state depends upon the nature of the instruction, and for some operations, the actual values being processed. The basic machine timing logic produces a series of four 40-nanosecond pulses separated from each other by an interval of 80-nanoseconds. The complete series, called a pulse train, marks the basic processing interval of 320 nanoseconds. Register information may be routed to the arithmetic adder or address adder, the result obtained, and then entered into the first rank of the accumulator or effective address register within this period.

All instructions require at least one execution state. Execution time ranges from a single pulse train for a single precision add or subtract, or a load instruction, to many trains for iterative operations such as multiply (28 pulse trains) and divide (52 to 79 pulse trains). The execution of each instruction is controlled by a hardware counter. There are eight execution counters, each controlling a group of functionally similar instructions.

CENTRAL PROCESSOR CONTROL PANEL

The central processor control panel provides direct control of the CP/IO Unit for system startup and for maintenance. Some of the uses of the panel controls, shown in Figure 1-2-11, are listed in Table 1-2-5.

MAJOR STATE CONTROL

The central processor control panel START button initiates the first instruction access state upon system startup, as shown in Figure 1-2-12.

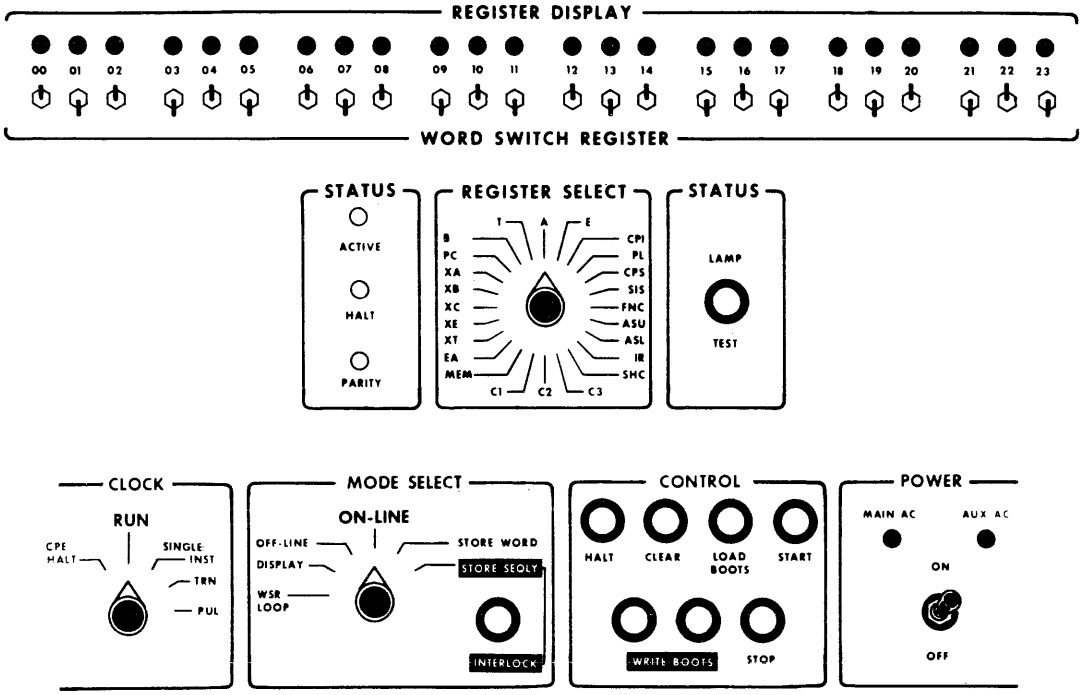


Figure 1-2-11. Central Processor Control Panel

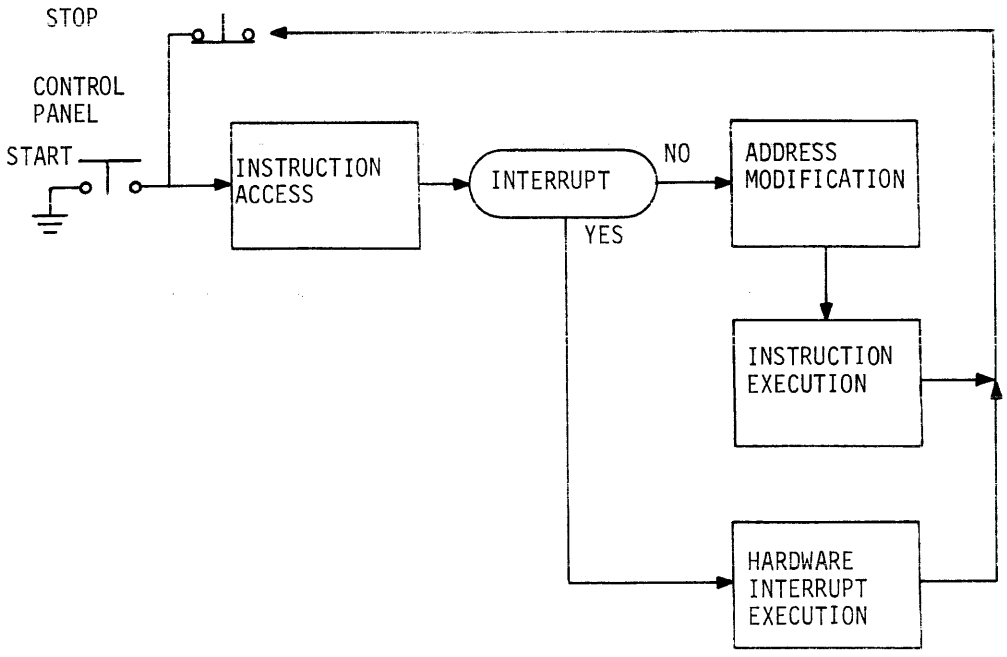


Figure 1-2-12. Processor State Control

Table 1-2-5. Control Panel Usage

PURPOSE	CAPABILITY
Start up	1. Control primary power to the CP/IO Unit and its integrated IO devices (drum, paper tape reader and punch, and the Teletype). 2. Clear all major registers in the processor and all IO device synchronizers simultaneously. 3. Load drum track zero bootstrap program. 4. Initiate (or halt) program execution.
Maintenance	1. Select and control off-line diagnostic and utility programs. 2. Control instruction execution -- a. Provide single step control for diagnostic purposes. b. Stop on core parity error. c. Block process interrupts. 3. Execute a single instruction set in the hardware switches of the word switch register. 4. Display or alter the contents of any addressable register or core location.

Thereafter, the sequence is automatic, proceeding from instruction access, through address modification, to instruction execution; then repeating the process with the next stored instruction. The normal sequence can be broken, however, by a priority interrupt. At the end of the instruction fetch state, interrupt requests pending are examined. If there is a request having higher priority than the current program, the execution state is entered and a hard-wired interrupt "instruction" is executed in place of the fetched instruction.

ARITHMETIC AND LOGIC OPERATIONS

FIXED POINT DATA FORMAT

All fixed point arithmetic uses binary notation, shown in Figure 1-2-13, with 23 bits representing magnitude for single precision, or 47 bits for double precision. In either case, the leftmost bit is reserved for the sign. Negative numbers are in binary two's complement form, eliminating sign analysis and recomplementing in most algebraic computations. For logical operations, such as analyzing status information, data may be treated as 24 bits or 48 bits of unsigned data.

Single Precision Arithmetic

Fixed point arithmetic is performed upon A register and B register inputs in a 24-bit parallel adder. Results are accumulated in the A register. Multiply is performed by a shift right and add (to multiplicand or partial product) algorithm for each of the 23 magnitude bits of the multiplier. Divide is performed by a shift left and subtract (complement add) algorithm for each of the 23 magnitude bits of the divisor.

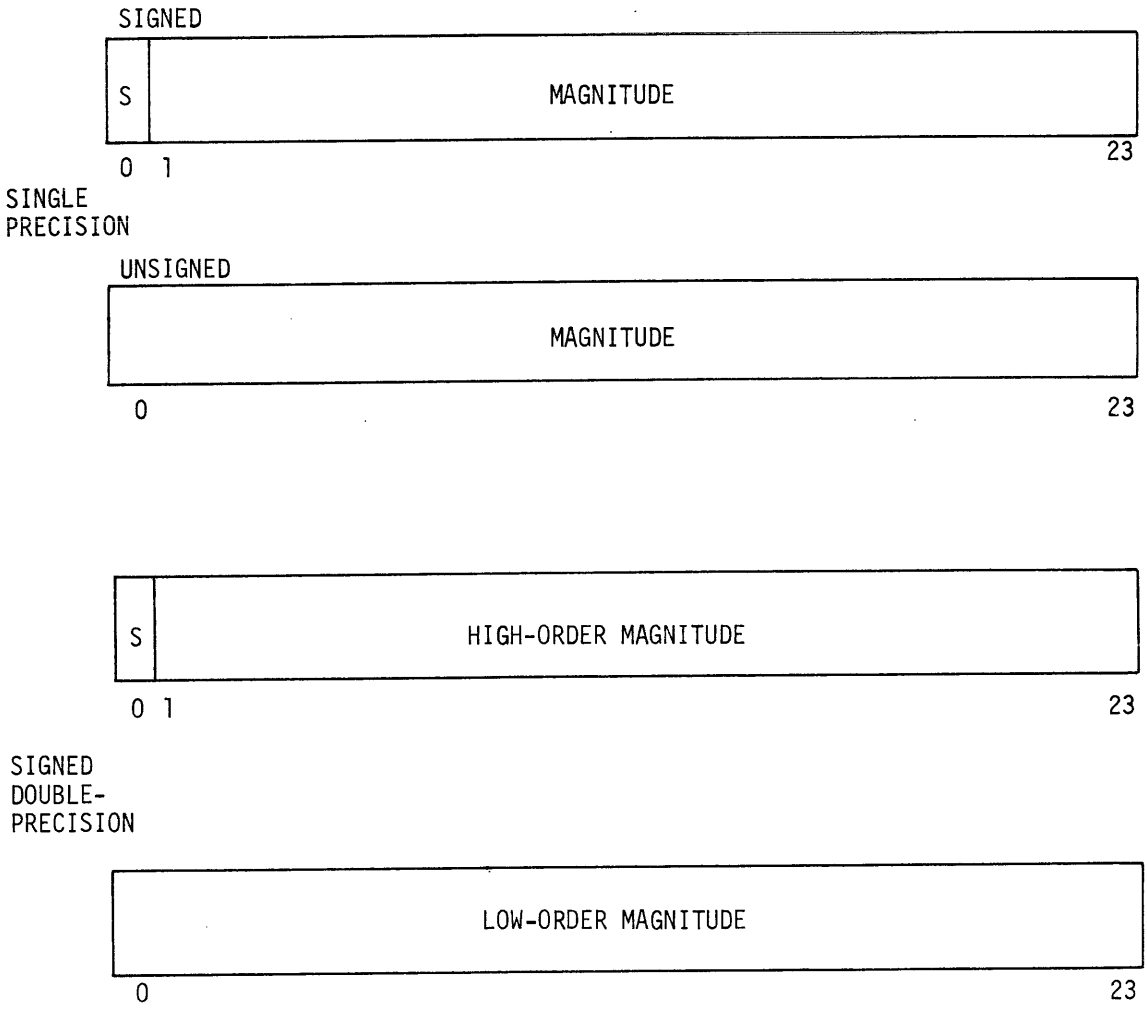


Figure 1-2-13. Fixed-point Binary Number Format

Double Precision Arithmetic

Double precision operations are carried out one word at a time. Since only the A and B register contents can be routed to the arithmetic adder, the contents of the A and B registers are operated upon, then the result is exchanged with the contents of the E and T registers for processing the second word.

FLOATING POINT DATA FORMAT

Floating point data can be represented, as shown in Figure 1-2-14, in single or double word format. Where number range permits, the use of the single word format conserves core. However, all single word operands are expanded to double word format when used for floating point computation.

Floating Point Hardware Option

Optional floating point hardware operates on double word operands using a 12-bit auxiliary adder for the characteristic and processing the 24 least significant bits of the mantissa in the main adder, and the 12 most significant bits of the mantissa in the auxiliary adder. A dedicated core location stores the characteristic while the mantissa is being processed in multiply or divide.

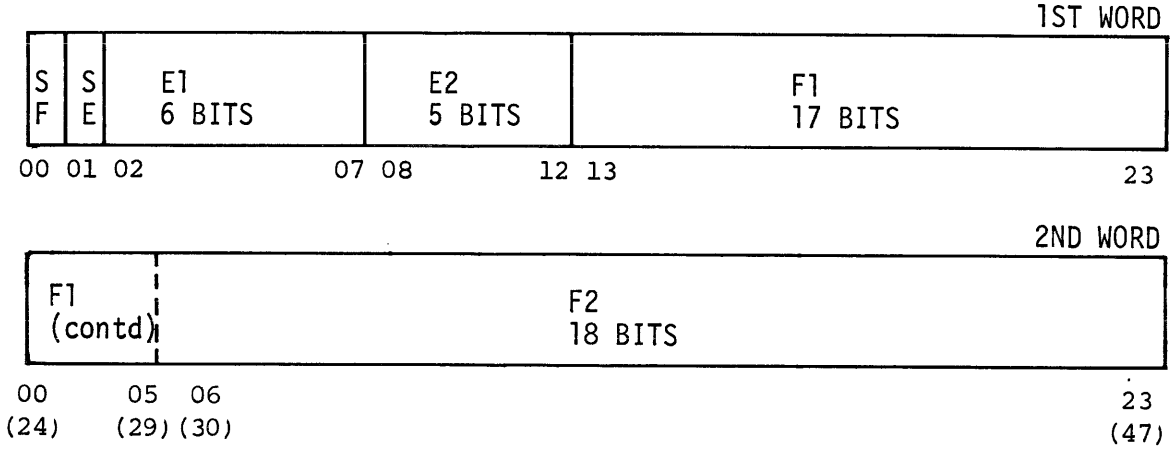
SHIFT AND ROTATE FUNCTIONS

For arithmetic or logical shift instructions, the contents of the A and E registers can be shifted right or left separately, or as a double word in

Floating Point Single-Precision Numbers is:

$$+(1-2^{-17})(2^{+31}) \geq N \geq -(1-2^{-17})(2^{+31})$$

A. Single Word Representation of Floating Point Data



Range of floating-point double-precision number is:

$$+(1-2^{-35})(2^{+2047}) \geq N \geq -(1-2^{-35})(2^{+2047})$$

B. Double Word Representation of Floating Point Data

Key:

SF = Sign of Fraction (Mantissa)
SE = Sign of Exponent (Characteristic)
E1 = Most significant 6 bits of Exponent
E2 = Least significant 5 bits of Exponent
F1 = Most significant 17 bits of Fraction
F2 = Least significant 18 bits of Fraction

Figure 1-2-14. Floating-Point Numbers

linked registers. The shift counter, in conjunction with the execution counters, controls the number of places shifted.

ADDRESS ARITHMETIC

The instruction register, the program counter, and the three other base registers, the two index registers, the B register (memory operand) and the effective address register can be routed (in various pair combinations) to the address adder. Address arithmetic is algebraic -- index and displacement values can raise or lower the base address, producing a 15-bit sum or difference.

INPUT/OUTPUT COMMUNICATION

PROGRAMMED IO

All IO operations are initiated over the programmed IO bus, which runs from the B register in the central processor to all IO device synchronizers. Table 1-2-6 lists the signals included in the PIO bus.

Slow speed, character-oriented devices use the programmed IO bus for all their functions. Each PIO instruction can transfer only one 24-bit word of data. Figure 1-2-15 illustrates the bit assignment within the data word for individual IO devices.

Command Sequence

PIO operation is initiated from a command word placed in the B register during the address modification state of the programmed IO operation.

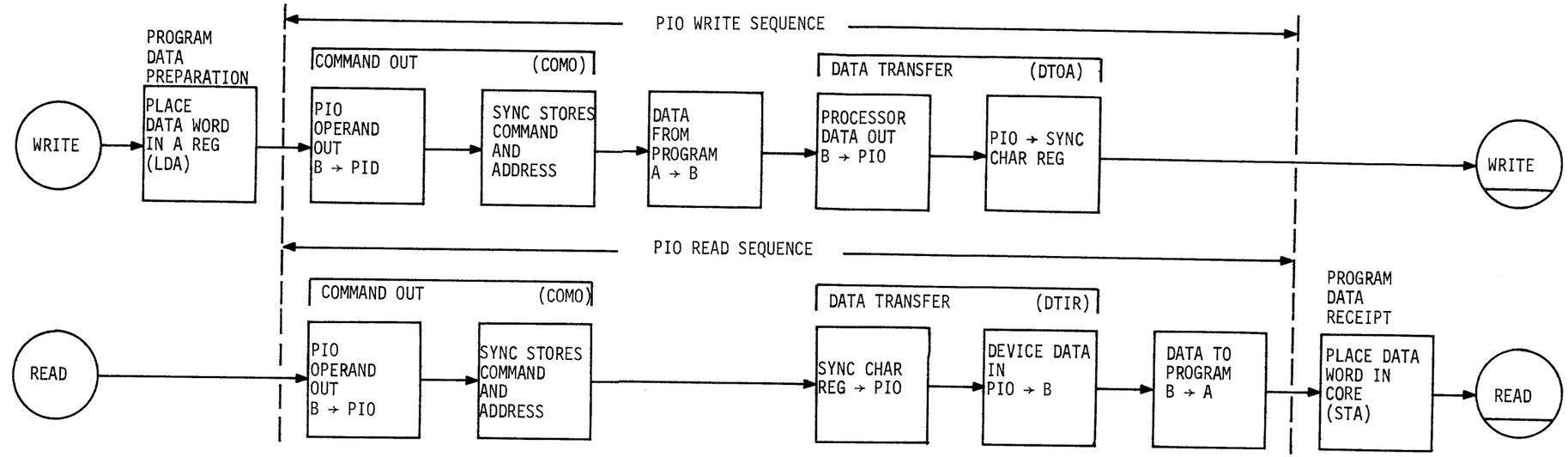
Table 1-2-6. Programmed IO Bus Signals (53 lines)

NAME	DEFINITION	FLOW*	LINES
INTn- 00-23	Interrupt request. Each device is connected to only one line. As many as 24 devices may be assigned to a single line or level.	S → P	24
PDBn- 00-23	Programmed data bus. During the command cycle, contains bits 00-23 of the PIO operand. During the execution of a status command, transfers status bits to the accumulator for a read status, or from the accumulator to the status flip-flops for a write status (A23=Ø).	P → S S → P P → S	24
COMO-	Command output. Signals the device synchronizer that a command is settled on the PDB.	P → S	1
DTOA-	Data output available. Generated from PIO operand and transmitted when the accumulator contents are settled on the PDB.	P → S	1
DTIR	Data input request. Signal to the addressed device to place its data on the PDB.	P → S	1
ACK-	Acknowledge. Generated by the addressed device: in response to COMO when the command has been stored and decoded; in response to DTOA when the data have been stored; in response to DTIR when the requested data have been placed on the PDB.	S → P	1
REJ-	Reject. Sent by the device synchronizer, along with ACK, when the command cannot currently be executed. The processor checks REJ during COMO cycles when ACK is received, but ignores REJ during DTIR and DTOA.	S → P	1
	SUPPLEMENTARY IO SIGNALS (5 Lines)		
BOOT-	Load bootstrap. Derived from the LOAD BOOTS switch on the CP control panel to command the drum synchronizer to load low core from track Ø.	P → S	1

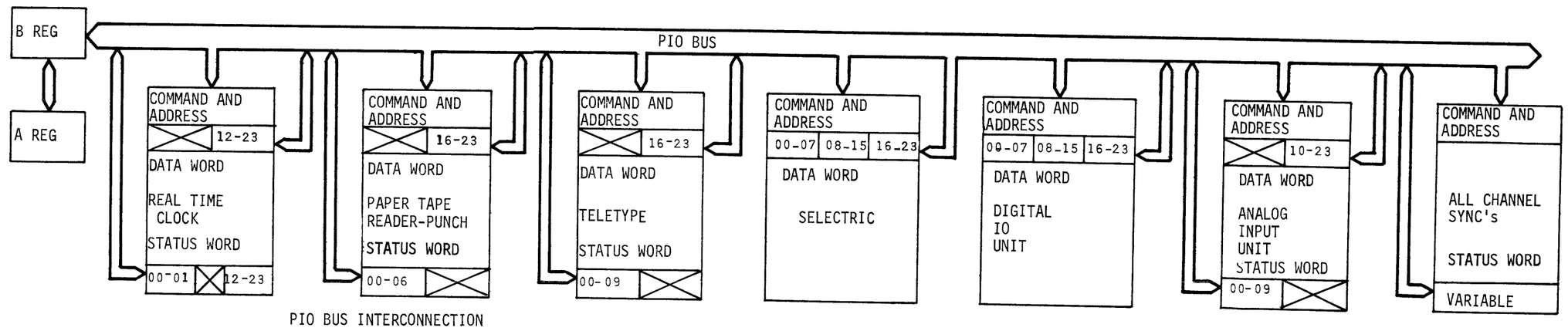
Table 1-2-6. Programmed IO Bus Signals (53 lines) (contd)

NAME	DEFINITION	FLOW*	LINES
WRBT-	Write bootstrap. Derived from the WRITE BOOTS switches on the CP control panel to permit bypassing the track Ø write protection.	P → S	1
CPC-	Central processor clock. Used by the synchronizers for PTR, PTP, TTY, and RTC as a logic clock source.	P → S	1
MCL-	Master clear. Sets each control flip-flop in the CP/IO to its proper initial state. Derived from the CLEAR switch on the CP control panel or from the power failure detection circuitry.	P → S	1
OFF-	Off-Line. Derived from the MODE SELECT switch on the CP control panel, this signal inhibits interrupts from all sources within the system interface nest and the console interface nest.	P → S	1

*P = Central processor
S = Device synchronizer



PIO DATA FLOW DIAGRAM



PIO BUS INTERCONNECTION

Figure 1-2-15. Programmed IO Operation

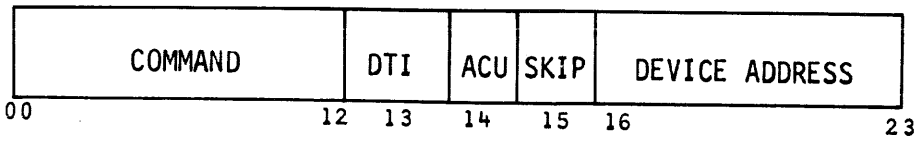
This command word, shown in Figure 1-2-16, is transmitted over the PIO bus to all IO devices. When one of the IO device synchronizers recognizes (decodes) its address on the PIO bus, it generates an acknowledge signal for return over one of the PIO bus lines. PIO bus communication is on an asynchronous basis, using a command-response exchange to correlate processor and device synchronizer signals.

Data Transfer Sequence

All instructions that involve an exchange of data require two exchange sequences -- comand-response, and data transfer-response. The central processor follows up the command (when acknowledged) with a request to transfer data. The selected device synchronizer either places data on the PIO lines, or takes data from the lines, as directed in the request, then sends a response signal to the central processor.

PIO DEVICE SYNCHRONIZERS

Since one set of bidirectional lines, the programmed data bus (PDB), carries both command and data within the CP/IO Unit, the device synchronizer must retain the command until the data has been handled. PIO synchronizers consist of control logic which decodes the device address and command, and stores both for reference during the data cycle. Busy, interrupt request, and error conditions are stored in a status register for subsequent transfer to the processor in response to a read status command. The synchronizer must provide a character or word register (where three characters per word are transferred, as in Selectric typer operation) for buffering the device, and encoding or decoding logic to translate between device code and ASCII for code sensitive devices. Timing logic is needed to synchronize device operations with PIO bus signals, and control logic for electro-mechanical elements in the device.



The following information defines the field represented by the operand given:

Bits:

0-12 Command that the selected device is to execute. The following commands are executed by most devices:

COMMAND	MNEMONICS
Read Interrupt Level Status	RILS
Write Data	WDA
Read Data	RDA
Read Status	RST
Read Status and Clear	RSTC
Write Status	WST

13 Data In - This bit specified whether the accumulator is to send or receive data, if a data transmission is specified by bit 14. (Bit 13 = ZERO, Accumulator sends data, Bit 13 = ONE, Accumulator receives data.) If Bit 14 = ZERO, then bit 13 is ignored.

14 Accumulator Usage Bit - This bit specifies whether a data transmission to or from the device via the accumulator is to occur after the command is transmitted. (Bit 14 = ZERO: Terminate after sending command, Bit 14 = ONE: Accumulator will send or receive data dependent on Bit 13.)

Figure 1-2-16. PIO Instruction Format

PIO Addresses

Two levels of addresses are used with most PIO devices.

a. Device address -- Part of the PIO instruction operand addresses one device synchronizer.

b. RILS address -- The RILS command selects all device synchronizers on a given interrupt level. Any device assigned to the selected interrupt level responds with its assigned interrupt bit set if it has an interrupt pending.

PIO Commands

The single IO instruction in the FOX 1 repertoire provides a subset of programmed IO commands, summarized in Figure 1-2-16. Execution time for various PIO operations is shown in Table 1-2-7.

A PIO read or write command transfers a single word (24 bits) between the central processor accumulator and the selected device. When there are less than 24 meaningful bits of data to be transferred, the insignificant bits are read as zeros, or, in write operations, ignored. Status bits are transferred in similar fashion. Busy, interrupt and various error bits indicate conditions in the device. A write status command, which sets status bits equal to corresponding accumulator bits, can be used to simulate situations for diagnostic or test purposes. A write status command with accumulator bit 23 set provides a master clear signal to the device logic to reset error conditions. The RILS command is used to determine which of several devices assigned the same interrupt level has a request pending.

2.89 to 2.90

Table 1-2-7. PIO Timing*

OPERATION	TIMING (MICROSECONDS)
RILS	9.60
Aborted Command	
IO usage violation	2.24
IO timeout violation (Unimplemented device)	16.64
Rejected Command	3.52 to 26.88
Accepted Command	
No data transfer	3.52 to 26.88
Data transfer	4.80 to 51.84

*Execution time for PIO is dependent upon the specific device addressed. Times listed are based on literal addressing. For some devices, absolute addressing is necessary (adding 320 nanoseconds).

CHANNEL IO

The channel IO subsystem provides for data exchange between device synchronizers and core, independent from the processor. The components of the channel IO subsystem and their interconnection are shown in Figure 1-2-17. Signals included in the channel IO bus to the synchronizers are listed in Table 1-2-8. Users of the channel IO are typical high speed, word-oriented devices which transfer data in bursts. The complete list includes the drum, disk, analog input, card reader/card punch, line printer, and the CRT consoles. The IO master functions as a dedicated slave-computer (or hard-wired controller) to interface requests from

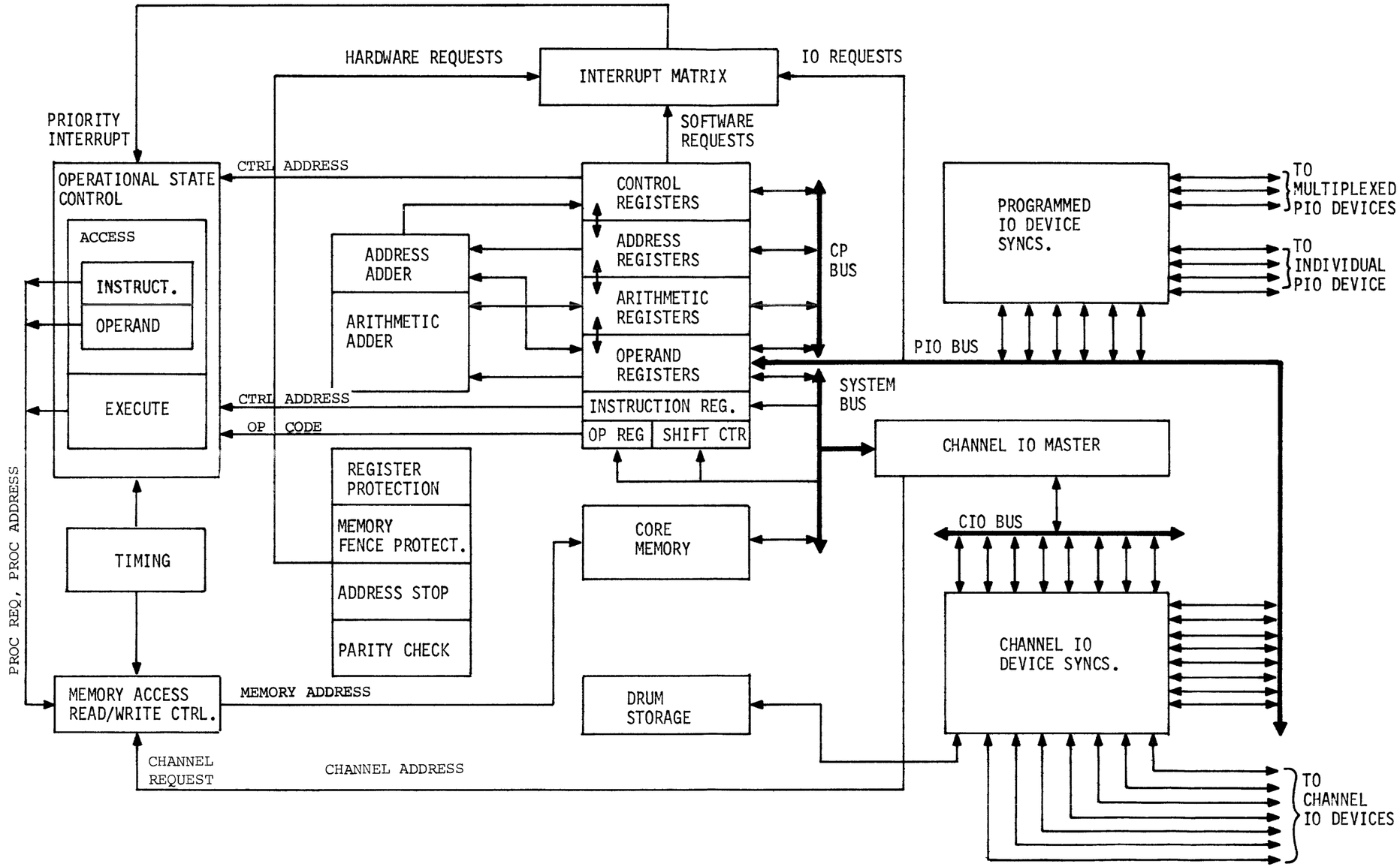


Figure 1-2-17. FOX 1 CP/IO Unit Data Flow

Table 1-2-8. Channel IO Bus (59 Lines)

NAME	DEFINITION	FLOW*	LINES
LWL-	Last word level. Channel detected the end of a block transfer. LWL is transmitted along with the last data word and sampled by the device synchronizer at the trailing edge of ENB.	C → S	1
PER-	Parity error. During a core cycle stolen for SIR, IDR, or ODR, channel detected a real parity error or an attempted access to nonexistent memory. PER is sampled by the device synchronizer at the trailing edge of ENB.	C → S	1
CDBn-00-23	Channel data bus. In response to SIR; carries the first word of the COTW; in response to IDR or ODR, transmits data between the CIO word register and the device synchronizers.	C → S S → C C → S	24
SIRn-Ø-7	Sequence instruction request. Sets up the CIO for a subsequent input or output data transmission.	S → C	8
ODRn-Ø-7	Output data request. Signals the channel to transmit a word to the device synchronizer. The channel responds with an enable (ENB) signal, resetting ODR until the synchronizer is ready for the next word of a multiword output data transfer.	S → C	8
IDRn-Ø-7	Input data request. Signals the channel to receive a data word on the CDB into its word register.	S → C	8
ENBn-Ø-7	Enable. Allocates CDB usage to the device synchronizer sending SIR, ODR, or IDR. Generates STBO for an SIR or ODR, and provides a request for data in response to IDR. ENB permits the synchronizer to reset its request.	C → S	8

Table 1-2-8. Channel IO Bus (59 Lines) (contd)

NAME	DEFINITION	FLOW*	LINES
STBO-	Strobe output. Following an ODR or IDR, signals the device synchronizer that the data on the CDB is now valid; not used for IDR.	C → S	1

*P = Channel
S = Device synchronizer

device synchronizers on eight IO channels for use of the channel data bus, the system bus, and the single port entry of core storage (shared with the processor).

IO Master

The IO master is analogous to a reduced logic, hard-wired version of the central processor. In both, overall control of data flow is accomplished through a matrix of sequence states and major states: timed sequence counter outputs are interpreted according to the pattern of a selected major state. The IO master differs from the central processor in having seven major states in place of the central processor's three, and in using the same sequence state counter in all operations. The seven major states are as follows:

a. Scanning the channel IO bus for activity requests.

b. High speed channel activity.

    (1) Input data request.
    (2) Output data request.
    (3) Sequence instruction request.

c. Low speed channel activity.

    (1) Input data request.
    (2) Output data request.
    (3) Sequence instruction request.

The sequence counter runs continuously, except in the interval between a memory cycle request and the memory cycle complete signal. Rather than following an established order, as in the central processor, the IO

master enters its operational states in response to external requests originating in IO device synchronizers. Requests are honored as received; simultaneous requests are taken in a priority based on channel address, with the lower numbered channel receiving the higher priority.

Channel Order Triple Word

The IO master obtains instructions from memory for the channel IO synchronizers. The channel IO equivalent of the central processor instruction word is the channel order triple word (COTW), shown in Figure 1-2-18. Three consecutive words in memory indicate the type of operation to be performed, the number of words to be transferred by the order, and the address of the first word to be transferred, respectively. The first part of the triple word, the command word, is sent to the device synchronizer. The next two words are used by the IO master to keep track of the transmission and to notify the synchronizer when the last word has been transferred.

Next Instruction Address Register

The channel order triple word is prepared by a central processor program before it issues the instruction to start channel IO. Eight dedicated core registers, one for each channel, store vectors provided by central processor programs pointing to a second vector ("double-indirect" addressing) containing the address of the channel order triple word (COTW) for each channel. The central processor issues a start channel IO instruction over the PIO bus to one of the CIO device synchronizers. The PIO instruction commands the synchronizer to make a sequence instruction request (SIR) to the channel IO master. The IO master responds to the SIR by obtaining the COTW from core memory.

WORD 1

OUT	CHR	EOI	NOP	DEVICE CONTROL
00	01	02	03	04 05 06 07 08 09 10 11 12 13 14 15 16 17 18 19 20 21 22 23

WORD 2

IGNORED	WORD COUNT
00 01 02 03 04 05 06 07 08 09 10 11	12 13 14 15 16 17 18 19 20 21 22 23

WORD 3

IGNORED	FIRST WORD ADDRESS
00 01 02 03 04 05 06 07 08	09 10 11 12 13 14 15 16 17 18 19 20 21 22 23

WORD 4 (Optional)

IGNORED	CHAINING LINK ADDRESS
00 01 02 03 04 05 06 07 08	09 10 11 12 13 14 15 16 17 18 19 20 21 22 23

NOTES:

Word 1 is the Channel Order. The remaining three words provide sequencing information.

OUT - Designates the direction of transfer: out = ONE means output from CIO to device

CHR - Designates Chaining Request

EOI - Designates End-Order-Interrupt

NOP - Designates no data to be transferred

Device Control Field - Defined in device description.

Word Count - Designates maximum number of words to be handled in the data transfer

Core Start Address - Designates starting memory address from which data are to be read or written

Figure 1-2-18. Channel Order Triple-Word Format

2.98 to 2.103

Channel Order Chaining

When the channel order requests chaining, the device synchronizer makes another sequence instruction request upon completing the current order, without intervention from the central processor.

HIGH/LOW SPEED CHANNELS

The maximum channel IO configuration consists of two high speed channels and six low speed channels. High speed channels use hardware registers in the IO master to keep track of the memory location for the next word of data, and the number of words remaining to be processed in the current channel order. Low speed channels use dedicated core locations as registers, and store current data address and last data address in them as each word is processed. Table 1-2-9 indicates the relative speeds of the two types of channels.

Table 1-2-9. Channel IO Timing

OPERATION	HIGH SPEED CHANNEL	LOW SPEED CHANNEL
Input Data	2.24 to 2.56 µs/word	4.16 to 4.8 µs/word
Output Data	2.56 to 2.88 µs/word	4.48 to 5.12 µs/word
Sequence Instruction	6.08 to 6.72 µs	8.32 to 8.96 µs

CHANNEL IO DEVICE SYNCHRONIZERS

In addition to having the same logic required in PIO synchronizers, CIO device synchronizers must control exchanges over the CIO bus. The CIO

synchronizer must decode its device address from the PIO bus, and the CIO command word (obtained by a sequence instruction request), and store both for reference during the CIO data transfer. Busy, interrupt request, and error conditions are stored in a status register for subsequent transfer of status information.

The synchronizer must provide a data register to hold CIO data for transfer to channel data bus or to the device, and encoding or decoding logic to translate between device code and ASCII for code sensitive devices. Timing logic is needed to synchronize device operations with CIO bus signals, and control logic is required for electro-mechanical elements in some devices.

The IO master furnishes control information in a CIO command word to be stored in the device synchronizer. For example, an out flip-flop "remembers" that a write operation was ordered. When the last word level signal is received from the IO master, the state of the end order interrupt flip-flop, set from the command word, determines whether device interrupt is requested. A stored chaining request, together with last word level, initiates another sequence instruction request, without resort to the central processor. If any of the error flip-flops -- such as core parity error, or timing error -- are set during channel operation, the synchronizer ignores chaining request and forces an end order interrupt.

MEMORY INTERFACE

The processor and the IO master connect with core memory through the system bus and associated control lines, and connect with the memory access enable and memory read/write control logic, as shown previously in Figure 1-2-17. The system bus and its control lines comprise the following:

a. System Bus, 24 data lines.

b. Memory Address.

(1) Channel Memory Address, 15 lines.

(2) Memory Address from effective address register in central processor, 15 lines.

c. Requests.

(1) Memory Cycle Requests, 2 lines, from IOM, CP.
(2) Memory Write Requests, 2 lines, from IOM, CP.

d. Responses.

(1) Memory Access Enable, 2 lines, to IOM, CP.
(2) Memory Read Complete, 2 lines, to IOM, CP.
(3) Memory Parity Error, 2 lines, to IOM, CP.

Core memory is a resource shared between the central processor and the IO master. Two blocks of control logic govern the interface, as follows:

a. Memory Access Control.

(1) Allocates memory cycles.
(2) Selects the source of memory address.

b. Read/Write Control.

(1) Determines the direction of system bus data flow.
(2) Synchronizes transfers to and from the system bus.

The two users, the processor and the IO master, make independent requests for memory service. Rather than cycling continuously, memory becomes active on a demand basis. Requests for service received while memory is inactive (not engaged in a cycle) are honored immediately. Requests received while memory is active remain pending until the cycle in progress is finished. When requests are received simultaneously, or both users have requests pending, priority is given to the IO master. A read request is presumed, unless the write control line is active. Each user activates its group of 15 address lines along with its request for service. Either request, when accepted, gates its associated address lines into memory's address selection logic.

After requesting a memory read operation, the internal sequence counter of either user, processor or IO master, waits while memory's internal logic gates data onto the system bus. A read data complete signal from memory read/write control logic gates system bus data into the IO master or processor register and permits the user's sequence counter to advance again.

In a memory write operation, either access enable line -- processor or IO master -- gates its associated data onto the system bus. The processor or IO master sequence counter waits for memory's internal logic to accept the system bus data. After the first half of the memory cycle, read/write control signals the user to proceed. Memory completes the write portion of its cycle without reference to the system bus or external address lines.

SYSTEM SECURITY

A comprehensive system of hardware and software checking ensures detection of failures, preservation of system data and operating environment, and a smooth, automatic transition to analog (or manual)

backup control of the process in emergency situations. Built-in system security logic and standard process control software provide the following types of protection:

a. System Data Protection.

   (1) Core Memory.
   (2) Hardware Registers.
   (3) Drum.

b. Process IO System Security.

c. Instruction Execution Control.

   (1) Illegal Instruction.
   (2) Fixed Point Overflow.
   (3) Floating Point Overflow/Underflow.

d. Program Protection.

   (1) Memory Fence.
   (2) Address Stop.

e. IO Safeguard.

   (1) IO Timeout.
   (2) IO Usage Violation.

f. Main Power Monitoring.

SYSTEM DATA PROTECTION

Core Memory Parity Checking

During every memory cycle, the central processor generates a parity bit, a logical one or zero, as required to bring the number of one-bits in the word to an even sum. The parity bit is entered into core whenever the data are written. On a read operation, the parity bit generated is compared with that read from core. An unequal comparison indicates a core parity error.

Nonexistent Memory Referencing

On systems with less than maximum core capacity, hardware detects any attempt to access an unimplemented core location.

Memory Crowbar Protection

A memory protection circuit known as the "memory crowbar" withholds voltage from the memory drivers during power-on sequencing, and quickly removes it during power-off sequencing (including power failure) to prevent loss of information.

Register Protection

Three categories of protection are provided for seven of the addressable registers. Control registers and the base register associated with executive software are protected from unintentional alteration. Only programs assigned the register manipulation privilege can change the

contents of these registers. The control register governing software requests for interrupt is separately protected against alteration by programs lacking the interrupt privilege. Two registers associated with the address stop option require a program to have the trace control privilege to change their contents. An executive mode bit accords a program the privileges of all three categories. Should a program lacking the appropriate privilege attempt to change a protected register, the attempt is blocked, and a hardware interrupt is requested.

Drum Memory Parity Checking

A parity bit is written along with each 24-bit data word on the drum. On a drum read operation, each word is checked for correct parity (in the drum synchronizer).

PROCESS IO SYSTEM SECURITY

Computer hardware performance is checked by on-line diagnostic programs that are run at one second intervals. Software delays or program loops are detected by stall alarm timing logic that signals an error unless reset every 1.2 seconds (approximate). A system flunk line from the FOX 1 keeps process controllers in the direct digital control mode. Computer hardware or software failures interrupt the system flunk line, placing the controllers in the backup mode.

INSTRUCTION CHECKING

Instructions accessed for execution are checked for:

a. Any of the six unassigned operation codes.

b. Any of the floating point operation codes when the floating point hardware is not implemented.

Instruction executions are checked for:

a. Fixed point overflow (such as can be caused by addition, subtraction, arithmetic left shift, normalize, or illegal division).

b. Floating point overflow (such as exceeding the capacity of the characteristic field or illegal floating point division).

Detection of any of these conditions initiates a hardware interrupt request.

PROGRAM PROTECTION

Memory Fence

A standard feature called the memory fence protects the contents of core memory from alteration due to program error. A 24-bit (addressable) fence register is split into 12-bit high and low limit fields with a resolution of either words. Separate comparators check memory address (effective address register output) against the two fence limits. The results of the fence comparison are checked for each instruction fetched and for each attempt to write into a memory location. Fence checking does not increase processing time. A fence violation results in a hardware interrupt request. A program operating in the executive mode is not affected by fence limits.

Address Stop

A useful aid in program debugging is the optional address stop feature. A protected memory area is defined by 15-bit fields in separate upper and lower limit (addressable) registers, providing single word resolution. Individually selectable operations may be prohibited within the protected area, as follows: instruction read, indirect read, operand read, or data store or modify. A single comparator checks the memory address contained in the effective address register against the lower and upper limits in turn, extending the duration of the memory cycle. The address stop feature may be activated or deactivated under program control. If one of the prohibited operations is attempted inside the limits of the address stop area while the function is enabled, the operation is aborted, and a hardware interrupt is requested. Because of its affect on throughput, the address stop feature is normally used only in background debugging of programs.

IO OPERATION CHECKING

IO Time-out

All programmed IO exchange sequences -- both command and data transfers -- are timed for a maximum of approximately 12 microseconds for completion. When, for any reason, the central processor does not receive a response within that interval, the IO operation is aborted and an interrupt is requested. An IO timer violation results when a command is issued to a nonexistent (unimplemented) address.

IO Usage Restriction

All IO devices are assigned one of three priority levels: system IO, critical IO or noncritical IO. To be entitled to use a device, a program

must be given a corresponding IO privilege by the operating system software. Without the proper privilege, a program attempting to execute an IO instruction violates the IO usage restriction. The operation is aborted, and a hardware interrupt is requested.

POWER MONITORING

System power failure is detected by monitoring the output of four critical dc power supplies in the CP/IO Unit: +5 volts CP, +5 volts IO, and memory +12 volts and -6 volts supplies. Imminent failure is detected, and the main power failure bit in the CP STATUS register set, while at least 600 microseconds of good operation remains (power supplies maintain usable output for at least two milliseconds after loss of input).

Power Fail/Auto Restart

The purpose of the power fail/auto restart logic is threefold:

a. Detect imminent loss of ac power in time to save the execution status of the processor for subsequent restart.

b. Prevent execution of instructions and memory cycles while ac power is inadequate for reliable operation.

c. Restart the processor without operator intervention when ac power has been restored.

Power Fail Detection Noise Immunity

Although the power failure detection hardware is sensitive to noise signals, the affect of noise upon the system is limited to setting the

main power failure bit in the central processor status register. (The processor is stopped by a program instruction, not a hardware signal.) Software effectively filters out noise by sampling the main power failure bit again after a suitable interval to determine whether the failure is more than momentary.

Memory Crowbar

For an actual failure, the program stores status information needed for restart, and executes a halt instruction, placing the processor in the halt state. Halt status enables hardware to crowbar the master clear line at the active level, and to crowbar the memory driver 24-volt supply to the inactive level.

NOTE

CROWBAR -- A protective circuit triggered by a slight change in sampled voltage to throw a short circuit (crowbar) across the output terminals of the monitored source.

The power failure condition remains latched until 50 milliseconds elapse without a power failure sensed signal. Then, the crowbar releases the 24 volt memory supply, and after another 50 milliseconds settling time, releases the master clear signal line. The power failure crowbar forces 00070_8 into the program counter and sets the executive mode bit in the central processor status register.

Power Fail Timer

A pneumatic power fail timer relay (agastat) monitors the duration of a power loss. If the duration of the loss exceeds a preset (by adjustment

of the agastat) value, software will restart the system with the process control devices in backup mode.

SYSTEM CONTROL

Topics to this point have covered control of computer components. The ultimate purpose is to make these components function efficiently as the FOX 1 Process Control System. Integrated hardware-software design allocates system resources for optimum use of storage, computation, and IO facilities in real-time process control operations, and background data processing functions.

Unless directed to do otherwise, the central processor executes instructions in the same sequence as they are stored in core memory. For optimum performance, the sequence must be modified to cope with varying operating conditions. The normal sequence may be changed by five types of operations:

a. Program skip.
b. Program branch.
c. Subroutine call.
d. Trap call.
e. Priority Interrupt.

PROGRAM SKIP

The smallest change in program sequence is provided by the skip operation, which causes the program counter to "jump over" one word in the sequence of stored instructions. (For correct operation, a skip must not be followed by a two-word instruction.) A skip breaks the program sequence when a program tested condition exists -- a predefined

relationship between a memory word or literal operand and the contents of a designated register, the state of a designated bit, or the acceptance of a programmed IO instruction.

PROGRAM BRANCH

A program branch may be an unconditional jump to a new group of instructions, or the jump may be dependent upon a specific arithmetic or logical relationship. The new location must be within the confines of the memory fence for the program being executed (except for a program operating in the executive mode, which is not limited by a fence). The branch, then, can transfer control to another part of the program being executed.

SUBROUTINE CALL AND PUSHDOWN STACK

Two subroutine call instructions can be used to transfer control to a subroutine temporarily, while retaining the next sequential instruction address for return to the calling program. Combined software and hardware functions link the calling program and the subroutine. Software assigns an expandable area of memory called the pushdown stack to each program brought into core. A hardware top of stack index register effectively expands the stack area as each subroutine is called, and contracts it as execution of each subroutine is completed. A return from subroutine instruction picks up the vector at the top of stack location, decrements the top of stack index register, and returns control to the calling program instruction at the location designated by the stack vector.

Reentrant/Nonreentrant Subroutines

There are two types of subroutines -- reentrant, and nonreentrant. The subroutine call for a nonreentrant subroutine need only store a return vector. The results of any computations done by the subroutine are stored within it. Reentrant subroutines -- those which can be interrupted at any point to permit use by another program -- must store any changeable data outside the subroutine to prevent change or loss as a result of interruption. A reentrant subroutine call instruction, in addition to storing a return vector in the stack, reserves a work area to preserve data for exchange with the calling program. Alternatively, the reserved area may contain the address of a work area outside of the stack.

Nested Subroutines

A subroutine may in turn call another subroutine -- each execution of a subroutine call instruction stores a return vector in the location above the previous top of the push-down stack, and increments the top of stack register to point to the new top. These are called nested subroutines. The return vectors are picked up in reverse sequence as the path is retraced from the subroutines to the calling program.

TRAP CALL

A trap is a special form of hardware-activated change in the instruction sequence, in which control is transferred to a known location.

Auto-Restart Trap

Manual Start/Auto-restart Trap -- The restart is the simplest trap of the three used in the FOX 1. In the manual startup procedure, the operator presses HALT, CLEAR, and START switches on the processor control panel. Following a power failure, approximately one second after power is restored, an automatic sequence is initiated which duplicates the manual procedure. Either the control panel CLEAR switch or the auto-restart logic forces a value of 00070_8 into the program counter.

Subroutine Call Trap

To transfer control to a subroutine outside the fence of the calling program (as in summoning a subroutine common to several programs), a trap call is used. The appropriate subroutine call instruction is used to store a return vector only (for nonreentrant subroutines) or a return vector and data or data address. The program does not branch to the address of the subroutine call. If the address is a literal, the program is forced to memory location 00101_8. If the address violates the memory fence, the program is forced to memory location 00100_8. In either case, the effective address of the call instruction is stored in the location above the top of the push-down stack. The trap handler program for literal traps or fence violation traps examines the address above the top of stack to determine the desired subroutine.

PRIORITY INTERRUPT

A priority interrupt system is essential to real-time processing and foreground/background swapping. The interrupt operation must preserve data in process, and acquire control information, such as a new priority

level and operating privileges, for executing the interrupting program. Since it reduces the time available for processing, context switching time, or overhead, must be minimal. Hardware and software interaction is required to accomplish these goals.

Context Switching

Two storage areas are reserved for processing interrupts -- a hardware dedicated core word for each interrupt level, and a software assigned block of 16 words for each level for preserving program context. The first 24 words of core are dedicated to interrupt vector storage, with the address of each word corresponding with an interrupt level. Stored in each vector location is the address of a 16-word block designated by operating system software. The first ten words of each block are reserved to receive the contents of ten significant registers stored at the beginning of an interrupt. The last six words store values to be inserted in base, index, and control registers to establish the operating environment of the interrupt handler program.

When an interrupt is taken, the vector for the interrupting level is read from dedicated core to obtain the address of the proper interrupt memory block. Operating privileges, relocation values, accumulated results and status information for the interrupted program are preserved by storing the contents of the last ten sequentially addressed hardware registers, starting at the memory location indicated by the interrupt vector. Values establishing the relocation parameters and operating privileges of the interrupting program are then loaded into the fence register, the privilege and level register, three base registers, and an index register. These are the first six registers of the ten previously stored.

Return From Interrupt

After the purpose of the interrupt has been accomplished, control is returned to the interrupted program through the use of a special return from interrupt instruction. Using the interrupt vector as an absolute indirect address, the return from interrupt instruction loads the fence register with the first context word saved in memory. The instruction loads the next nine memory words into the remaining nine hardware registers in ascending address sequence. Since the program counter is one of the registers restored, the program previously interrupted resumes with the next instruction in its sequence.

Interrupt Status

The Priority interrupt controls the sharing of system resources in a multiprogramming environment. Each individual program is initially assigned a priority level, its interrupt status, by operating system software, and a range within which the interrupt status can be varied during program execution. A program can only be interrupted by a request from a higher priority source. The basic system provides 12 levels of priority, which can be expanded to 24 levels as an option. Interrupt requests are divided into three categories:

a. Hardware Requests.
b. Software Requests.
c. IO Requests.

Interrupt Sources

Hardware Interrupt Requests - System protection logic generates hardware interrupt requests. Core parity and main power failure detection

interrupts are assigned to level zero, the highest interrupt priority. Program errors, memory fence violations, register protection violation, IO timeout, or IO usage violations interrupt at level one. Address stop interrupt, if implemented, is assigned one level above the lowest priority -- level 11 or 23.

Software Interrupt Requests - Programs having the software interrupt privilege can make a request on any of the 12 or 24 available levels (subject to operating system restrictions). The halt instruction generates a level zero interrupt.

IO Interrupt Requests - IO operations proceed at a much slower rate than instruction execution. The direct memory access capability of channel IO permits the processor and channel device to proceed asynchronously. Once a channel operation is initiated, the central processor can return to the execution of instructions in either the same program that requested an IO operation, or another program. When the channel IO operation has been completed, the device synchronizer sends an interrupt request to the central processor to obtain another instruction. IO interrupt requests stored in 12 or 24 interrupt flip-flops remain active until cleared by an instruction from the processor.

Interrupt Matrix and Mark Register

Five flip-flops called the mark register are positively set at the beginning of each instruction access state to the highest priority request level then pending. The setting of these five flip-flops is compared against the interrupt status stored in the last five bits (19 to 23) of the privilege and level register. If the interrupt request

contained in the mark register is higher in level than the interrupt status of the program, control is turned over to the execution hardware for program interrupt.

REAL TIME CLOCK

The real time clock is a necessary adjunct to the FOX 1 system for scheduling foreground programs at standard intervals, and for sharing processor time among multiple background programs. Clock 0, supplied with the basic processor, operates at line frequency, for such uses as timing the process IO scan interval and triggering periodic log outputs. The optional clocks are crystal oscillator driven at 100 kHz for clocks 1 and 3, and at 5 kHz for clock 2. These clocks are useful for timing events between or within the one-second-scan intervals.

All clocks drive 12-bit down-counters. A desired interval is timed by inserting in the counter a binary value scaled for the selected clock frequency. The desired interval is divided by the cycle time of the clock, and the result entered (in binary form) into the counter, as in the following example:

$$\text{(Desired interval = 500 ms)} \div \text{(clock 1 cycle time = 200 } \mu\text{s)} = \text{(count = } 2500_{10}\text{)} = \text{(clock entry = } 4704_{8}\text{)}$$

A write command transfers a count value to a selected clock and starts it counting. An interrupt request is generated when the clock count reaches zero.

The program can stop the clock at any time to read the count value. After reading the count, the program can restart the clock from the same point or start it with a new count value.

POWER CONTROL AND DISTRIBUTION

The CP/IO Unit requires two single phase ac inputs -- main and auxiliary power. The preferred source of power, the FOX 1 Power Distribution Unit (PDU), provides transient-free main power of 120 VAC at 400 Hz, and auxiliary power of 120 VAC at 50 Hz or 60 Hz. Where the PDU is not used, a highly reliable, transient-free source of 120 VAC at 50 Hz or 60 Hz must be used for main power, and a separate source of conventional quality 120 VAC at 50 Hz or 60 Hz for auxiliary requirements.

Each ac input is connected through a primary circuit breaker to separate contacts of the primary contactor, K1. A 27.5 VDC supply connected directly to the load side of the main ac breaker energizes the primary contactor through the POWER switch on the processor control panel. The load side of the contactor feeds auxiliary power to the Teletype, drum, paper tape reader, paper tape punch, and blowers in the center section and each wing of the CP/IO Unit. Separate breakers protect each IO unit. Pedestal convenience outlets receive auxiliary power through a circuit breaker connected directly to the load side of the primary breaker. A low voltage transformer converts auxiliary power to a 3.15 VAC signal driving real-time clock 0.

Main power from the load side of the contactor is distributed through branch circuit breakers to dc supplies as shown in Table 1-2-10.

Table 1-2-10. DC Power Supplies

+5 V @ 100 A	Central Processor Logic
+5 V @ 100 A	IO Logic
-6 V @ 1.7 A +12 V @ 4.0 A	Core Memory Sense Amplifiers
-12 V @ 1.6 A +18 V @ 7.9 A	Drum Memory Linear Electronics
24 V @ 11 A	Core Memory Drivers
+48 V @ 16 A	Selectric Typer Magnets
+25.7 V Unregulated	AC Contactor Coil

Two large, vertical bus bars distribute the +5 VDC for the processor and IO synchronizer nests, respectively. Cable assemblies distribute the remaining dc voltages.

With all circuit breakers ON, the POWER switch on the processor control panel controls both the CP/IO Unit and the drum, Teletype, and paper tape devices. Power is automatically reapplied to this much of the system when the input is restored following a primary power loss.

FUNCTIONAL SUMMARY

The functional overview of the CP/IO Unit has been based on the simplified block diagram, Figure 1-2-19, first presented at the end of the introduction. Each block on the diagram has been the subject of a chapter of functional description. A few significant points regarding each block are offered in the following summary.

STORAGE

Register, core, and drum facilities are correlated to provide rapid, efficient storage and retrieval of information. As programs are swapped between core and drum, corresponding context data are swapped between registers and core. Both core and drum function as intermediate IO units supporting the processor. In addition, core interfaces directly with the IO master.

PROCESSOR CONTROL

Operational state counters govern the progression from instruction to operand to result. The eight addressing modes available in the address

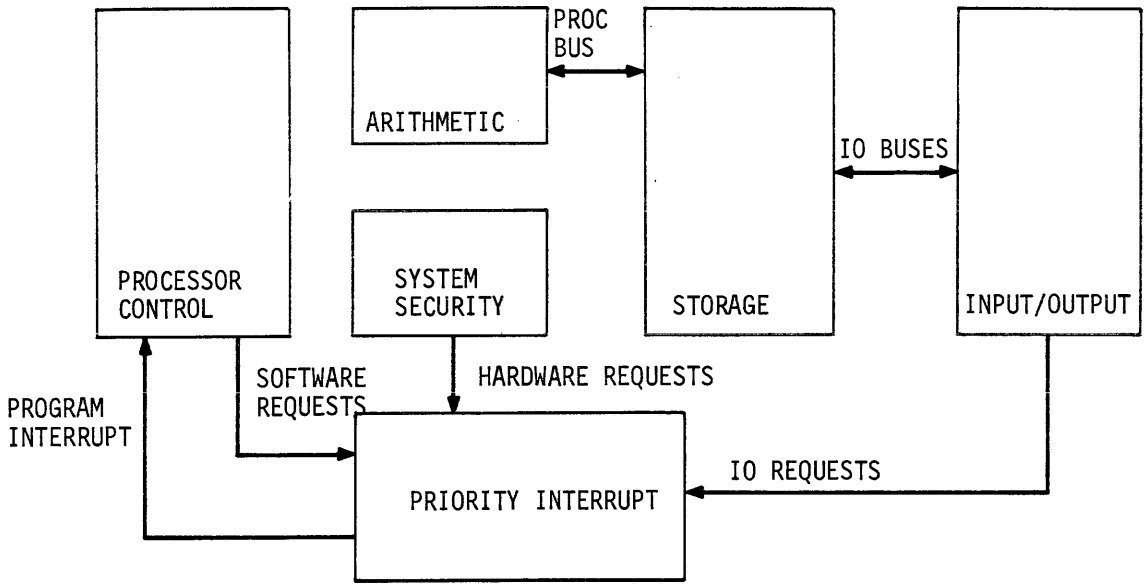


Figure 1-2-19. FOX 1 CP/IO Unit, Simplified Block

modification state provide flexible assignment of programs and data in core. The word-parallel processing of operands in the execution state provides maximum throughput.

ARITHMETIC AND LOGIC OPERATIONS

The instruction set is planned to provide the most efficient use of the arithmetic and storage facilities for a wide range of data. Choice of single or double precision fixed point arithmetic matches storage area and compute time requirements to the number range of individual problems. In a similar way, floating point short notation reduces core space requirements. The compare instruction, compatible with both fixed and floating point formats, includes a three-way branch to reduce the number

of instruction steps in arithmetic or logical testing. Bit and byte instructions provide flexible operations within the boundaries of the 24-bit word.

INPUT/OUTPUT

The programmed IO bus provides a low speed path through the arithmetic registers to all device synchronizers. Low speed device synchronizers decode read or write data or status commands on the PIO bus. High speed device synchronizers decode status commands and the single "start channel IO" command. A PIO read or write command exchanges a single word between a low speed device and the processor. A PIO start channel IO command initiates the independent transfer of a block of data between a high speed device and memory.

The IO master controls operation over the two high speed and six low speed channels available in a maximum system. Each is dedicated to a specific type of device (single devices such as the drum or line printer, or multiple units of the same type, as CRT consoles or disk units).

An asynchronous interrupt bus relays interrupt requests to the processor immediately. The PIO connection to channel synchronizers permits the processor to check the status of one channel device while other CIO operations continue.

Either the IO master or the processor can initiate a memory cycle. Channel IO takes priority over the processor when both have a request pending. The data access interval is 640 nanoseconds, permitting processing to overlap one third of the 960 nanosecond full memory cycle.

SYSTEM SECURITY

Two hardware devices provide program security. The memory fence keeps a program inside assignable address limits. The address stop feature (optional, for background testing only) keeps a program outside assignable address limits.

Other system security hardware includes parity checking whenever data is read from drum or core, program or arithmetic error detection (by on-line diagnostics), IO interface timing check, main power failure detection, and special process IO security checks. In most cases, automatic recovery procedures keep the system on-line even when several simultaneous errors occur.

SYSTEM CONTROL

Program branch, program skip, trap call, or priority interrupt can modify the stored sequence of instructions according to such factors as the result of arithmetic or logical comparisons, IO device status, the need for subroutine service, or real-time process control or time-sharing demands.

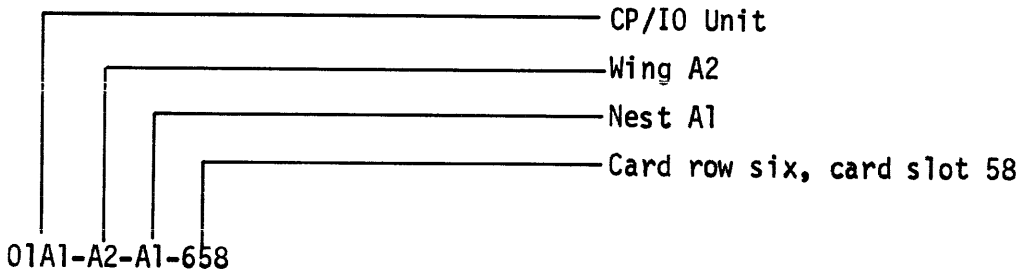
The priority interrupt system provides for foreground/background swapping and a multiprogramming environment. The 12 or 24 levels of priority can each accommodate 24 interrupt sources, with a discrete interrupt bit assigned to each source. An interrupt handler program interrogates the interrupt bit status to determine the specific source and the appropriate response.

PHYSICAL DESCRIPTION

The elements of the central processor are housed in a drip-proof enclosure consisting of four "wings" attached to a center structure. The wings contain nests of printed circuit cards, and the center structure houses the Drum, Paper Tape Reader/Punch, Control Panel, power supplies, and Power Distribution Panel.

REFERENCE DESIGNATION

The Central Processor/IO Unit reference designation is 01. Since there is only one such unit in the system, the cabinet designation is A1. The wings are designated A1 through A4, numbered clockwise around the center structure, beginning to the right of the control panel. The center frame is designated 05. Nests within each wing are numbered from top to bottom. Locations on the front portion of the center frame are numbered top to bottom, A1 through A5. Locations in the rear portion of the center frame are numbered top to bottom, A6 through A12. Nests contain from two to ten rows. Card slots in wings 1 and 4 number 01 through 34, wing 2 number 01 through 60, wing 3 number 01 through 28. A typical full reference designation is written:



MAJOR COMPONENTS

The major components, as shown in Figures 1-2-20 and 1-2-21, consist of the following:

Wing 1

System Interface Nest
Peripheral Interface Nest
Console Interface Nest

Wing 2

Processor
IO Master
Drum Synchronizer
Teletype Synchronizer
Real Time Clock Module

Wing 3

Basic 16K Memory Module
Optional 16K Memory Module
Paper Tape Reader/Punch Synchronizer

Wing 4

Disk Memory Synchronizer

The cabinet occupies a 6-foot cube and is designed for shipping without disassembly. However, the wings are bolted to the center structure and may be removed if required.

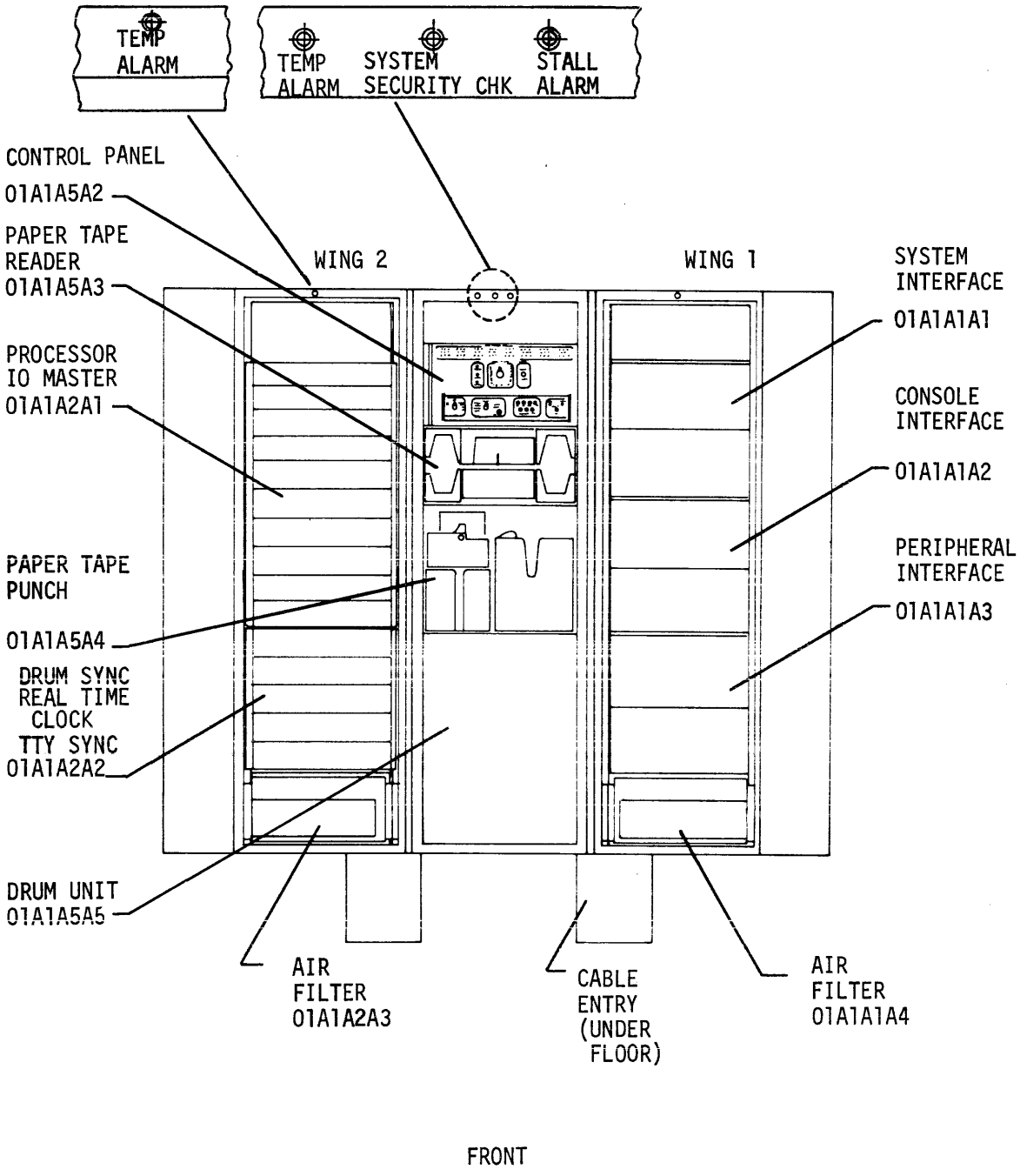


Figure 1-2-20. CP/IO Unit, Front View

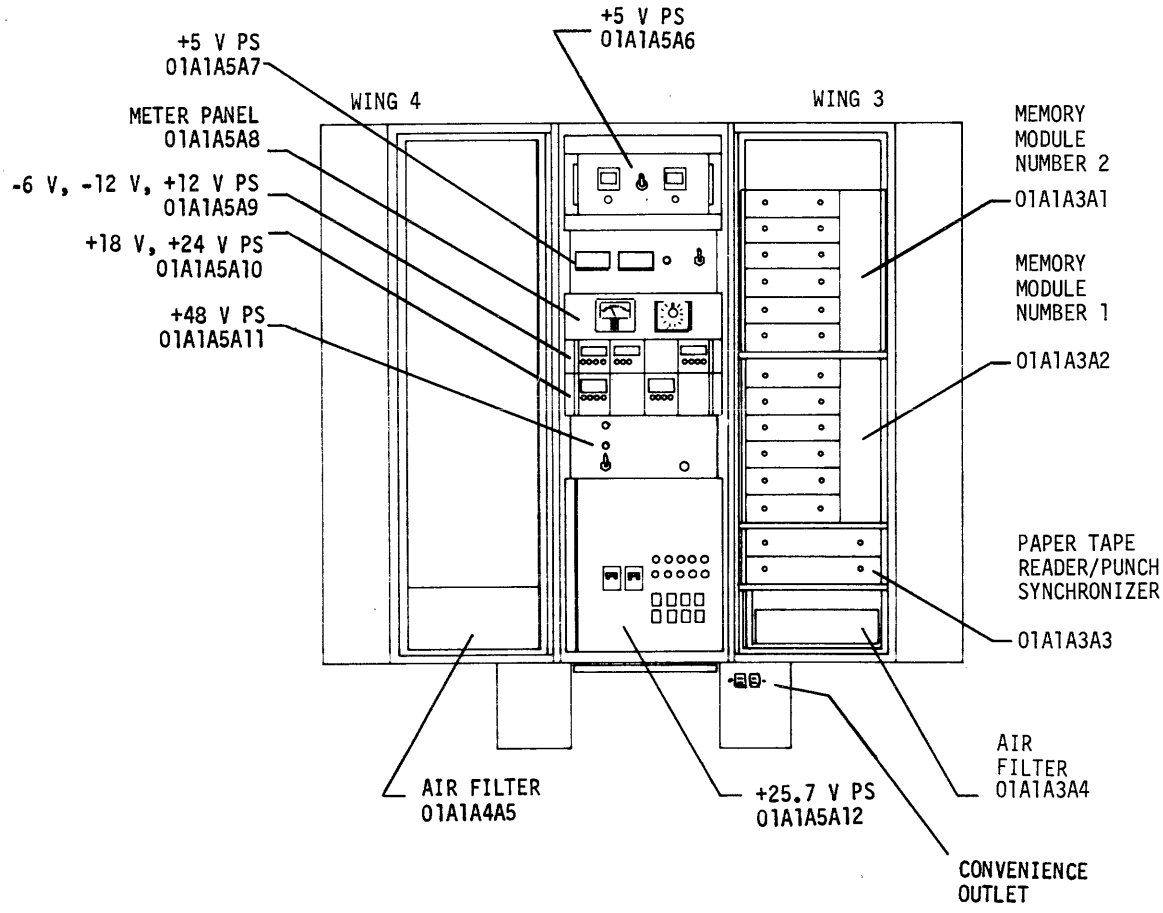


Figure 1-2-21. CP/IO Unit, Rear View

Wing nests are electrically coupled into the rest of the system by standard plug-in cables, and ground and logic-power buses.

The pedestal between wings 2 and 3 forms the air inlet section of the air plenum. The pedestal between wings 1 and 4 forms a passage for cable entrance and exit. This design incorporates five independent cooling systems: one system for cooling the center chamber and one for each of the four wings.

An air plenum is located in the left hand trapezoidal cross section of the center section. Ambient air is drawn in through replaceable air filters located in the bottom of the plenum. One wall of the plenum serves as the left hand interior of the center section. This wall contains a number of holes that allow ambient air to be forced into the center section. Fans beneath the power supplies keep the air circulating within the center section. The heated air is evacuated through a louvered panel on the right hand side of the center section. Additional ducting directs air from the plenum to the front drum shroud.

Each wing is cooled by a fan and ducting assembly located at the bottom of the wing. Ambient air is drawn in through replaceable air filters located on the underside of the wing. The nests have cover plates, which cause the captured air to rise through the nests of logic circuits before it is exhausted through louvers in the top of the wing. Each wing and the center section has a thermal switch located on the interior underside of the top cover. These thermal switches operate associated alarm lights shown in Figure 1-2-19 visible at the top of each wing and center structure. The thermal switches are set to operate at a temperature of 130 ± 3 degrees F, which corresponds to ambient temperatures of 110 to 120 degrees F.

CORE MODULE PHYSICAL DESCRIPTION

Basic core memory for the system is provided by a single module in which 24 bits of each word are spread over 24 matrices of 16,384 ferrite cores each. The bit matrices are packaged four to a frame. The complete module consists of seven frames, the last frame containing only two matrices, one for the parity bit, and one spare.

Memory may be expanded to the next larger size by installing a second module having 8,192 ferrite cores in each matrix. Added to the basic 16,384, this provides 24,576 positions. Maximum core capacity is obtained by adding a second module having 16,384 cores in each matrix (identical to the first module) for a total of 32,768 positions. Either of these changes may be made in the field after the initial system installation.

Memory is housed in wing A3 of the X-frame. The first 16K (K=1024 words) is located in 01A1A3A2. The 8K or 16K second module, if present, is located directly above the first in 01A1A3A1.

MAGNETIC DRUM UNIT PHYSICAL DESCRIPTION

The drum unit consists of a sealed disk memory assembly, bearings, drive motor, base plate assembly, and an electronics assembly containing head selection diodes and read amplifiers. The base plate is slide-mounted in a 19-inch rack in the CP/IO Unit center frame. The unit is shock-mounted within a hermetically sealed cover filled with helium. An integral, replaceable gas supply cylinder replenishes helium lost through seepage. The contents of one cylinder should be sufficient for at least three months of operation. Pressure inside the sealed chamber is maintained at

approximately 0.75 pounds per square inch pressure (0.5 to 1.5 psig) by a 2-stage regulator. The helium environment excludes dust, moisture, and contaminants.

The drive motor is an integral induction motor operating from single phase 115 VAC at a stabilized operating speed of 3528 ± 72 r/min with 60 Hz input, or 2940 ± 60 r/min at 50 Hz input. A fixed head magnetic pickup senses drum speed. The output from the pickup head is fed to a speed detection circuit in the drum electronics assembly.

Read/write heads are of the hydrodynamic, gas-lubricated bearing type. In the retracted position, heads are approximately 0.004 inches from the recording surface. When the disk is up to speed, a pressure pump is activated to develop pneumatic pressure (air, not helium) to move the heads into recording position. Table 1-2-11 indicates speed for head pull-in and drop-out. Heads "fly" at a nominal spacing of 100 microinches from the disk surface, never touching it. Heads are assembled in groups of four; each block of four heads constitutes a flying unit. Four blocks of 16 heads each are mounted in a head plate assembly, providng 64 heads for each recording surface.

Table 1-2-11. Drum Characteristics

PARAMETER	R/MIN @ 60 Hz	R/MIN @ 50 Hz
Stable Operating Speed	3456 to 3600	2880 to 3000
Head Pull-In	3170 to 3300	2620 to 2780
Head Drop-Out	20 to 200 r/min below pull-in speed.	
Switching Time:		
Read to Write --	1 bit cell time	
Write to Read --	30 microseconds	
Track Change --	30 microseconds	

The disk memory assembly consists of two or four disks driven by a directly coupled ac motor. The 256K drum option uses two disks, with four head plates for the four disk surfaces; the 512K drum option uses four disks, and eight head plates. The 12-inch aluminum disks are nickel cobalt plated. Each disk mounts on a common eight-inch hub, which in turn is fastened directly to the drive motor shaft.

A single flying head assembly reads two identical pairs of timing tracks permanently recorded on the periphery of one disk during manufacture. Circuit design prevents electrical component failure from erasing the timing tracks. One set of timing signals is selected for use, the other is held in reserve. A hermetically sealed toggle switch below the base plate transfers control from the normal clock set to the alternate. Data written using one clock can be read using the other.

An over-temperature thermal switch is located in the drum end plate. Another thermal switch is located in the motor winding. If the shroud temperature exceeds 150 degrees F or the motor exceeds 300 degrees F, ac power is removed. A motor rest button on the drum front panel must be pressed to restart the motor following an over-temperature shutdown.

Four indicators on the drum front panel monitor the following:

a. Power on -- ac available.

b. Speed low -- drum not up to speed.

c. Head actuator pressure low -- pneumatic pump is operating.

d. Temperature high -- excessive temperature in shroud or motor winding.

Power supplies in the CP/IO Unit furnish the drum with +15 VDC, +5 VDC, and -12 VDC. The drum drive motor receives 115 VAC single phase from the CP/IO Unit auxiliary power distribution bus. Conversion from 50 Hz to 60 Hz is accomplished by replacing the drum speed detection card.

CONFIGURATION

STANDARD CONFIGURATION

The smallest CP/IO Unit configuration and peripherals that will support FOX 1 software is the following:

a. 16K Core

b. 256K Drum

c. Teletype (ASR 35 or KSR 35)

d. Paper Tape Reader/Punch or Card Reader/Punch

e. System Interface Nest with appropriate process IO synchronizer card sets

Primary Power

The CP/IO Unit and peripherals can be configured to operate from either 50 Hz or 60 Hz input power.

Basic Components

The basic CP/IO Unit consists of the following:

a. Processor.
b. IO Master.
c. High Speed Channel 0 (for Drum).
d. Low Speed Channel 2 (for Analog Input System).
e. Low Speed Channel 7 (for Consoles).
f. Drum Synchronizer.
g. Teletype Synchronizer.
h. Clock 0 (Line Frequency).
i. 16K Memory Module.
j. Automatic Power Restart.
k. Twelve Levels of Priority Interrupt.
l. System Interface Nest (with basic card set).

OPTIONAL FEATURES

The following optional features can be added to the basic configuration:

a. Additional 16K Memory Module.

b. Address Stop Module.

c. Priority Interrupt Expander -- 12 additional levels of priority interrupt.

d. Hardware Floating Point.

e. Optional Clocks -- one, two, or three additional clocks can be implemented in the Real Time Clock Module.

f. 512K Drum.

g. High Speed Channel 1.

h. Low Speed Channels 3 through 6.

SPECIFICATIONS

Input Power Requirements

Primary ac of two different grades is required -- main power, a high quality, transient-free input for dc supplies; and auxiliary power of conventional quality for fans and convenience outlets. The dc power supplies are designed to operate from a nominal 120 VAC single phase source in the frequency range of 47 to 430 Hz. The FOX 1 Power Distribution Unit is strongly recommended as the source for these supplies. Any alternative source must be highly reliable, and noise and transient free.

a. Main Power (single phase)

1.	Voltage	105 to 133 volts rms
2.	Current	50 amperes, maximum
3.	Frequency	48 to 433 Hertz
4.	Harmonic content	4 percent maximum, with no single harmonic greater than 2 percent
5.	Transient content	No voltage transients outside the limits specified above are allowed.

b. Auxiliary Power (single phase)

1.	Voltage	117 volts rms ±10 percent

2.	Current	45 amperes, maximum
3.	Frequency	50 or 60 Hertz ±2 Hertz

Environmental Specifications

Temperature - The ambient temperature range with the equipment operating is 40 to 120 degrees F (4.4 to 49 degrees C). Ambient temperature range for storage is -30 to 150 degrees F (-34.4 to 66 degrees C). The maximum rate of operating temperature change is 1 degree F/minute up to the maximum operating temperature.

Relative Humidity - 20 to 95 percent (up to 85 degrees F, wet bulb). 0 to 95 percent nonoperating.

Ambient Air Contamination -- Up to 10 ppm hydrogen sulfide or sulfur dioxide.

Altitude - The equipment will operate at altitudes ranging from -1000 feet up to 6,000 feet. For transport or storage, the altitude range extends to 50,000 feet.

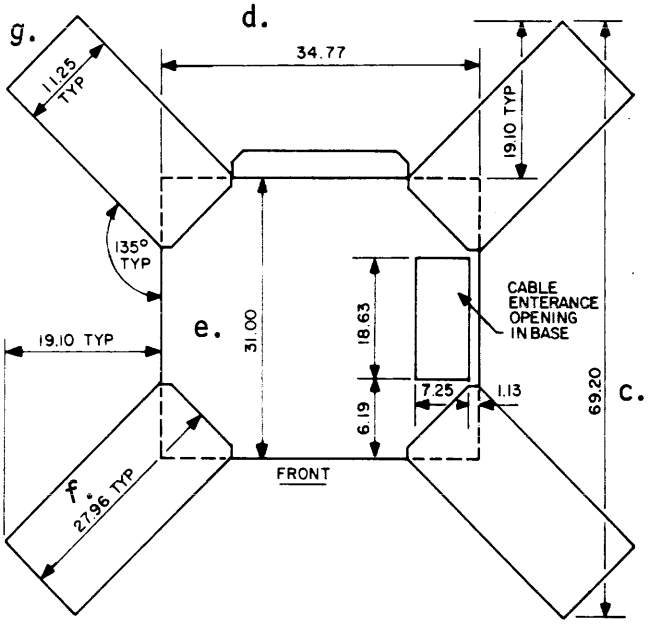
Vibration- Per MIL-STD-810B, dated 15 June 1967, Method 514, Figure 514-6, Curve AB, as follows:

5 to 27 Hz	±1.0 g (peak), Sinusoidal Input
27 to 52 Hz	0.036 inches (Double amplitude displacement), Sinusoidal Input
52 to 300 Hz	±5.0 g (peak), Sinusoidal Input

Dimensions - Physical measurements of the CP/IO Unit are diagrammed in Figure 1-2-22 with reference letters corresponding with the following list:

a.	Height	72 inches
b.	Width, overall	73 inches
c.	Depth, overall	69.2 inches
d.	Center section width	34.77 inches
e.	Center section depth	31 inches
f.	Wing length	27.96 inches
g.	Wing depth	11.25 inches

Maximum weight is approximately 2500 pounds.



NOTES:

1. ACCESS REQUIRED TO ENTIRE PERIPHERY.
2. DOORS & COVERS ARE LIFT-OFF TYPE. NO SWING SPACE NECESSARY.
3. CABLE ENTRY FROM BENEATH RAISED FLOOR.
4. FLOOR MOUNTING NOT REQUIRED.
5. ESTIMATED MAXIMUM WEIGHT: 2500 lbs.
6. ALL DIMENSIONS ARE IN INCHES.

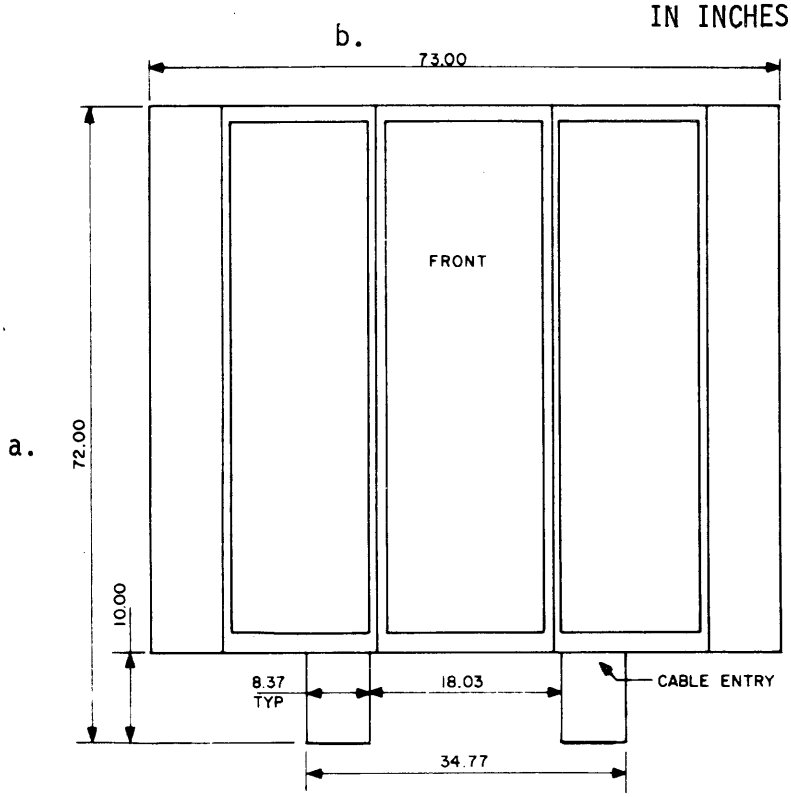


Figure 1-2-22. CP/IO Unit Dimensions

SECTION 3
POWER DISTRIBUTION UNIT

The Power Distribution Unit (PDU) contains a motor generator set, and control and distribution circuits which serve as a buffer between the primary power source and the FOX 1 system power supplies. The PDU is strongly recommended as an option to the FOX 1 to enhance system reliability in two ways. First, by isolating sensitive logic circuits from power line transients and RF interference on the ac source that would otherwise pass through ordinary power supply filters. Second, by providing a minimum of 50 milliseconds of float-through for power loss -- the generator's inertia or "fly-wheel effect" sustains power to the system for at least 50 milliseconds after a loss of power. A power loss from a momentary overload should be restored in 2.5 to 3 cycles, so that the power provided to the system will be continuous despite the interruption in the primary source. For prolonged loss, ample time is provided for an orderly shutdown of the system.

As its name suggests, the Power Distribution Unit is the source of primary power for most of the FOX 1 system. The power provided is of two grades -- a stringently defined, transient-free main power for the logic power supplies of the central processor, drum, process IO, and CRT consoles; and a normal commercial grade auxiliary power for the drum drive motor, for blowers and convenience outlets in all units receiving main power, and for all primary power requirements in the Teletype, paper tape reader, and paper tape punch. Main power, 120 VAC at 400 Hz, is produced by a motor generator in the PDU which is driven by the plant or commerical power. Auxiliary power is the plant or commercial source of 120 VAC at 50 or 60 Hz routed through the PDU for centralized control and overload protection. The PDU inputs and outputs are shown in Figure 1-3-1.

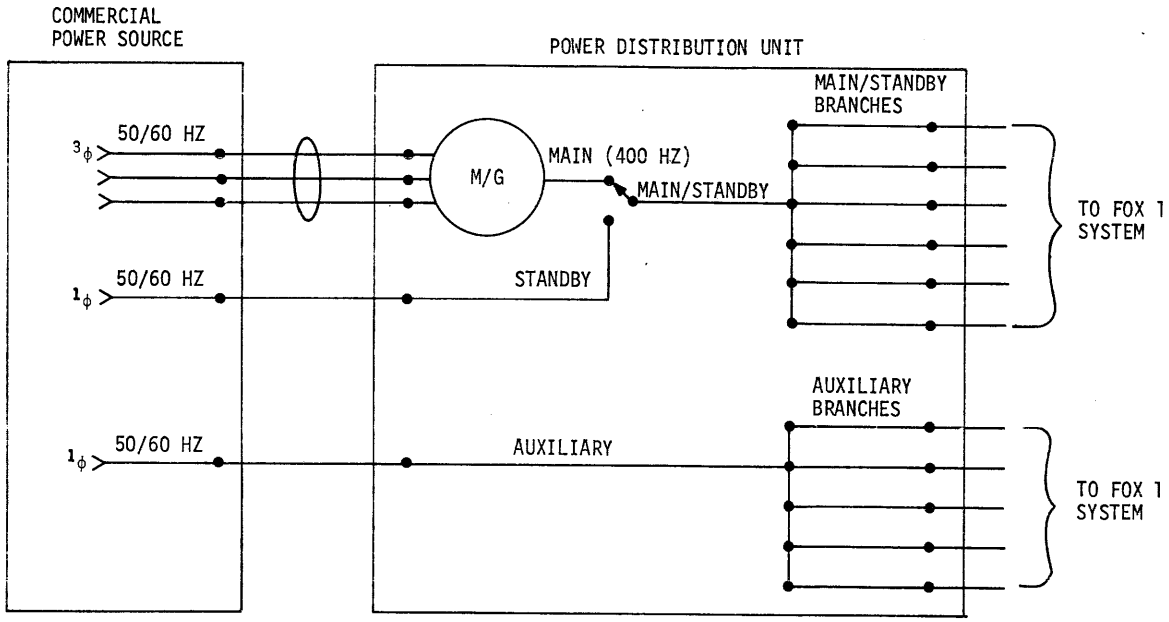


Figure 1-3-1. Power Distribution Unit Inputs and Outputs

The PDU also includes a manual switching arrangement to connect the system to an alternate (or back-up) source of main power for the infrequent periods when maintenance is required on the motor generator. This standby power, which must be free of transients, is 120 VAC at either 50 or 60 Hz. All system power supplies are designed to operate satisfactorily over an input frequency range of 48 to 433 Hz, allowing the direct substitution of 50 or 60 Hz for the normal 400 Hz source.

FUNCTIONAL DESCRIPTION

The Power Distribution Unit is a stand-alone unit housed in a single-bay cabinet lined with sound-absorbing material. Major components diagrammed in Figure 1-3-2, include the following:

a. Motor generator.
b. Motor generator control panel.

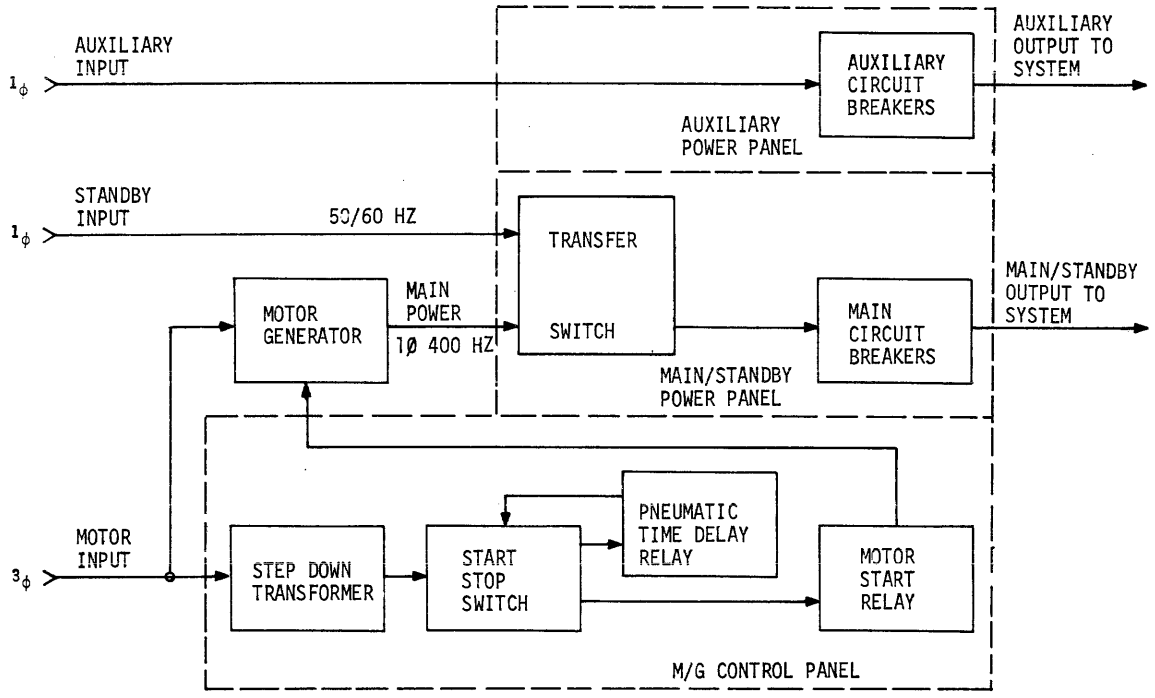


Figure 1-3-2. PDU Functional Diagram

c. Main and standby power control panel.

d. Auxiliary power control panel.

Motor Generator

The heavy duty, industrial motor generator set is a high-reliability, almost maintenance-free integral unit. The motor generator set, or converter, comprises a three-phase induction motor mounted above a generator on a common, vertical shaft. The two sets of ball bearings in the drive motor are sealed for lifetime lubrication. Bearing life is estimated at more than 10,000 operating hours under normal conditions. Bearings need be replaced only as they become noisy. The permanent magnet rotor should not ordinarily require remagnetization, and, of course, there are no brushes to replace. The generator can withstand a momentary short circuit of the output, and a continuous 20 percent

overload. The main/standby circuit breaker protects the generator from prolonged heavy overload.

Motor Generator Control Panel

The motor generator control panel shown in Figure 1-3-3 has a START/STOP pushbutton with a MOTOR RUN indicator, and a separate AC INPUT indicator for each of the three input phases. The operating elements of this control panel include the following:

a. START/STOP switch.
b. Motor starter.
c. Time delay relay.
d. Control transformer.

The START/STOP switch, an integrated assembly of two switches and an indicator, is the only means of starting or stopping the generator on demand -- there is no provision for remote control. The motor starter, an electro-magnetically operated switch controlled by the manual START/STOP switch, applies three-phase power to the generator drive motor, and, in addition, protects it from overload damage. An over-current relay in each input leg is an integral part of the motor starter. The over-current device consists of a heater coil and a eutectic (fusible) alloy sensing element in series with the line. Reset is manual, by pressing a reset button on the starter assembly. The motor starter and its heater coil are chosen (during assembly) according to the motor generator capacity and line frequency.

Not to be confused with a remote start control, the pneumatic time delay relay merely maintains the electrical connection to the motor starter during an input power loss shorter than the float-through period (50 milliseconds) provided by the generator. As long as the time delay

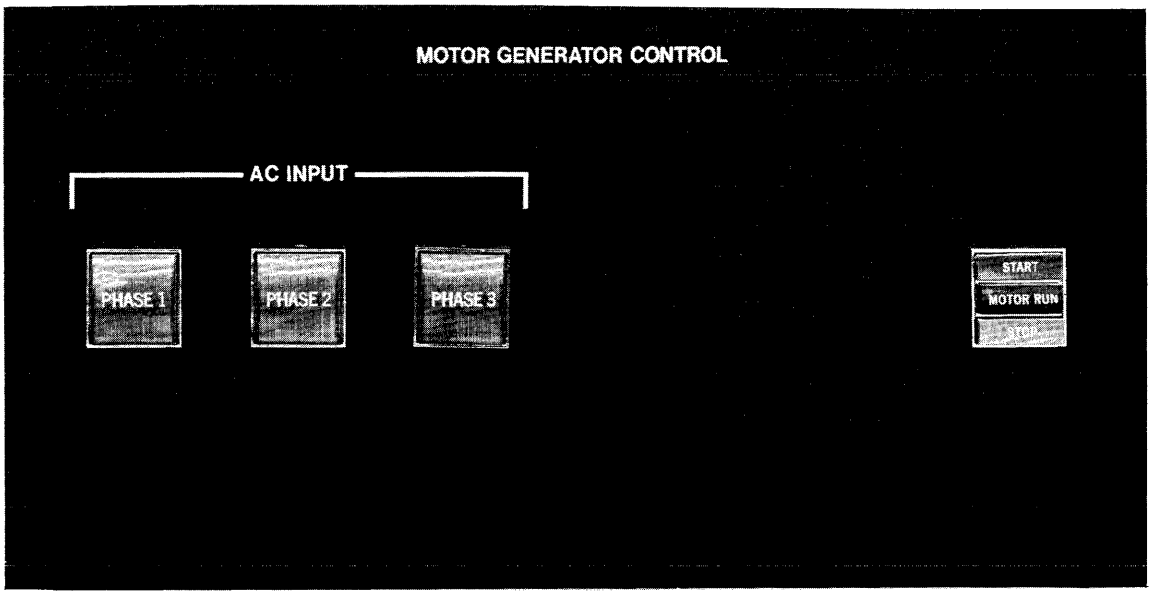


Figure 1-3-3. Motor Generator Control Panel

points remain closed, the motor starter will re-energize when power is restored. To resume operation after a longer interruption, the operator must press the PDU START button.

The control transformer provides the 120 VAC at 60 Hz or 110 VAC at 50 Hz required by the motor starter and time delay relay.

Main and Standby Power Control Panel

The main and standby power control panel shown in Figure 1-3-4, enables the operator to select either power source through a 75-ampere, rotary, 3-pole, double-throw, break-before-make MAIN/STBY power transfer switch. Either the MAIN (green) or the STANDBY (red) POWER lamp indicates power available once the source is selected. The MAIN/STBY POWER circuit breaker, rated at 50 amperes for the 5 KVA motor generator or 70 amperes for the 7.5 KVA unit, connects the load to the selected power source. The breaker is a front connected, series-trip, hydraulic-magnetic breaker for 120 VAC at 50/60/400 Hz. Six branch circuit breakers distribute the

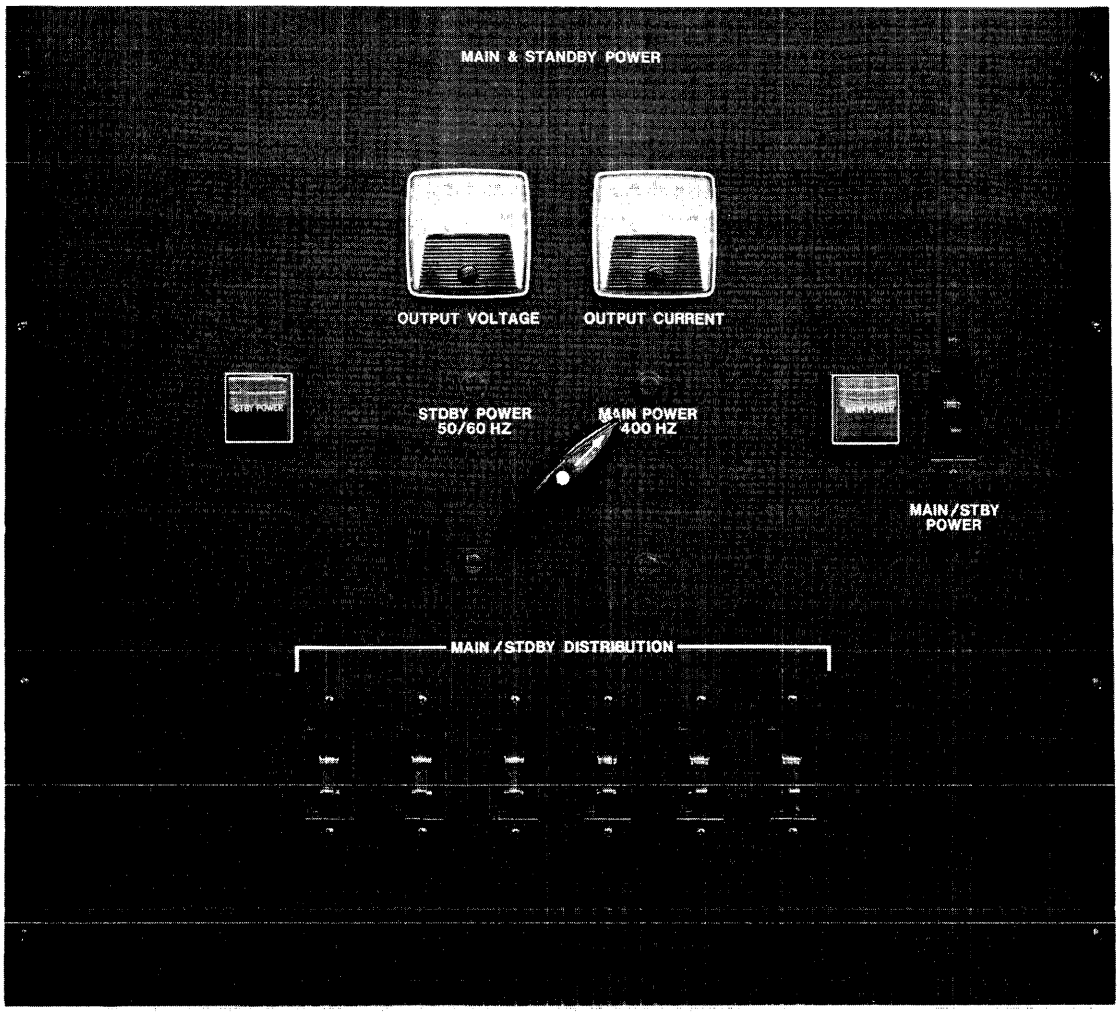


Figure 1-3-4. Main and Standby Power Control Panel

main or standby power to the system. One rated at 50 amperes supplies the CP/IO Unit, and five branches at 30 amperes each supply the Analog Input Unit, two Digital IO cabinets, and consoles.

Two panel meters are located above the power transfer switch. A 150 VAC (full-scale deflection) meter measures generator output or standby source voltage. A 100 ampere (full-scale reading) ammeter indicates the total current drawn from the motor generator or standby source.

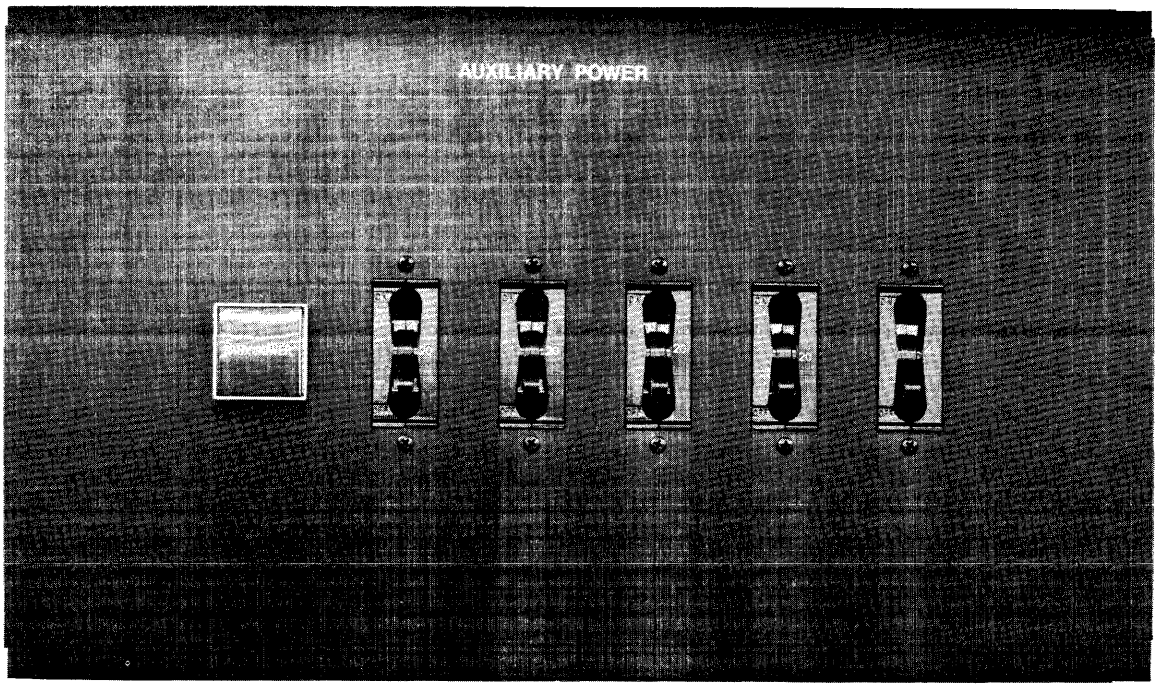


Figure 1-3-5. Auxiliary Power Control Panel

Auxiliary Power Control Panel

The auxiliary power control panel shown in Figure 1-3-5 contains an AUX POWER indicator and five circuit breakers for distributing plant or commercial power to the system. The CP/IO Unit circuit breaker is rated at 45 amperes, the other four at 20 amperes each.

PHYSICAL DESCRIPTION

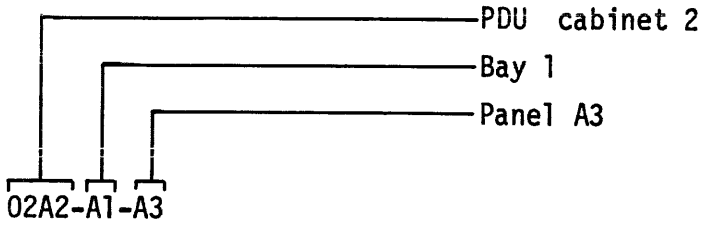
The Power Distribution Unit shown in Figure 1-3-6, is housed in a drip-proof cabinet consisting of a standard NEMA rack frame with a Foxboro-designed six-inch-wide wireway attached. The cabinet is 78.59 inches high, 24.88 inches deep, and 34.31 inches wide. The rack is 28.31 inches wide and designed to accept standard 24-inch front panel assemblies. A 24-inch hinged door provides access to the front, and another to the rear.

All components are on panel mounted units that slide out to the front for servicing, except the motor-generator, which slides out on a U-channel to the front or rear. Cable entry is through the bottom of the cabinet to a terminal box mounted on the right (viewed from the front) side-frame. The right side cover may be removed for access to the terminals. Three convenience outlets and a switch-controlled (ON/OFF) light are provided inside. Cabinet locks protect the equipment and prevent accidental contact with the high voltage inside.

Centrifugal fans incorporated in the motor-generator assembly, together with vent louvres in the rear door of the cabinet, limit heat build-up to not more than 20 degrees fahrenheit above ambient temperature. Sound-absorbing material lining the cabinet reduces noise to an acceptable level for computer room installation.

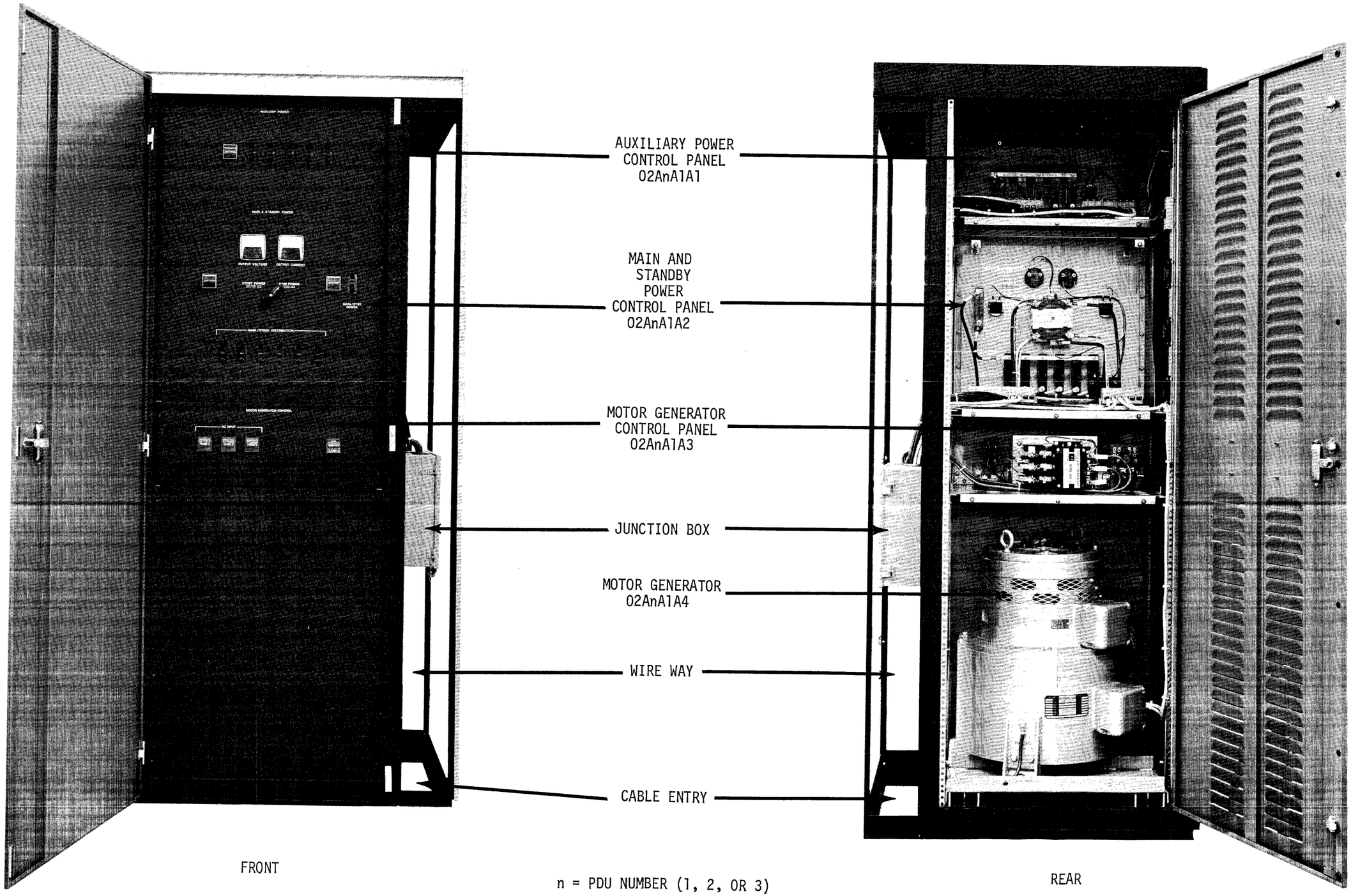
Reference Designation

The Power Distribution Unit reference designation is 02. For a system using multiple PDU's, the cabinets are designated A1, A2, or A3. Since the PDU is a single bay unit, the bay designation is always A1. The PDU panels are equivalent to nests in other equipment, and are designated A1 through A4. A typical full reference designation would be written:



PDU STANDARD FEATURES

All configurations of the PDU have the same internal wiring (except generator drive motor and control transformer connections) and the same generator output frequency and voltage -- 120 VAC at 400 Hz. Each unit



n = PDU NUMBER (1, 2, OR 3)

Figure 1-3-6. PDU Front and Rear Views

provides six branches of main/standby power and five branches of auxiliary power. The standard enclosure is a drip-proof cabinet with sound-absorbing lining. Cable entry is provided through the bottom of the cabinet.

PDU OPTIONAL AND CUSTOM FEATURES

One basic design is adapted to provide two different output capacitites and to meet 50 or 60 Hz input requirements. A computer system (called the hardware configurator) for processing customer orders guides Foxboro manufacturing in the selection and assembly of components. Four motor generator assemblies are available: 5 KVA for 50 Hz input, 5 KVA for 60 Hz, 7.5 KVA for 50 Hz input, and 7.5 KVA for 60 Hz. Generator drive motors used in the assemblies are 7.5 horsepower for the 5 KVA capacity, or 15 horsepower for the 7.5 KVA. The motor starter, over-current relay heater coil (part of the motor starter), time delay relay, and control transformer are selected according to motor generator capacity, input line frequency, and input voltage, as shown in Table 1-3-1.

The PDU can operate on either 220 or 380 VAC at 50 Hz or 208, 220, or 440 VAC at 60 Hz. The unit is set up for the desired voltage (during assembly) by selecting voltage taps and inserting jumpers on the input terminals of the generator drive motor and the control transformer. Main and auxiliary branch circuits are labelled on a custom basis to indicate which powers the CP/IO Unit, AIU, DIOU (by cabinet), individual consoles, and peripheral devices.

INTERFACE CONSIDERATIONS

System Configuration

Calculation of system power dissipation and selection of components to match input frequency, voltage, and current is accomplished automatically

Table 1-3-1. PDU Component Selection

COMPONENTS	PART NUMBERS					
	50 HZ INPUT			60 HZ INPUT		
	5 KVA	7.5 KVA	5/7.5 KVA	5 KVA	7.5 KVA	5/7.5 KVA
Motor Generator	D3000BM	D3000BN		D3000BP	D3000BQ	
Main Circuit Breaker	D3000HG	D3000HH		D3000HG	D3000HH	
Motor Starter	D3000HT	D3000HW		D3000HT	D3000HW	
	(NEMA 1)	(NEMA 2)		(NEMA 1)	(NEMA 2)	
Heater Coil	D3004UH	D3000HV	D3004UJ	D3004UG	D3000HY	D3004UJ
		D3000HY				
Time Delay Relay			D3004UM			D3004UN
Transformer						
208 VAC						D3004UL
220 VAC			D3000HX			D3000HX
380 VAC			D3004UK			
440 VAC						D3000HX

as part of the FOX 1 system configuration procedure. Guided by information from configuration questionnaires, a computer program determines system power requirements, based on standard and optional equipment ordered, and selects the proper PDU capacity. Where more than one PDU is required, the load is distributed equally between or among the units so that each is loaded to the same proportion of its maximum rating as the others.

In determining whether more than one PDU is required, the need for separate branch circuits is considered, along with the system load. Each free-standing unit -- CP/IO Unit, AIU, each console, and each DIOU cabinet -- requires one main (400 Hz) power branch from the PDU. No more than six main/standby power branches can be connected to one PDU. The CP/IO Unit, AIU, and each DIOU cabinet all require separate auxiliary

power branches in addition to the main power branch. A maximum number of five auxiliary power branches is available from each PDU.

The Teletype, drum paper tape reader, and paper tape punch are connected to auxiliary power through outlets in the central processor center frame. Most of the free-standing peripherals -- typewriters, line printer, card reader, and card punch -- have their own line cords with three-pronged plugs which can be plugged into wall outlets. Spare auxiliary branches in the PDU can be used to service these devices. Note that the CRT consoles must have main or standby power from the PDU or equivalent high grade source, but console auxiliary power can be obtained from a source other than the PDU. Console main and auxiliary power can be daisy-chained, provided that the line drop to the farthest unit is less than three volts. The nonimpact printer obtains power from its associated console. Figure 1-3-7 illustrates a typical power distribution system configuration.

Utility Power Connections

One three-phase and two single-phase ac input services are required. The three-phase line drives the motor-generator set. The first single phase line supplies the auxiliary power; the second, standby power. The source for standby power must meet very stringent requirements to qualify as a substitute for the motor generator output. (Refer to PDU Specifications for exact information.) All three ac input power services are brought through the bottom of the PDU cabinet and up through the wireway to a terminal box on the right side.

Unit Location

Sufficient space should be allotted to provide maintenance access to the front and rear of the equipment.

POWER DISTRIBUTION UNIT SPECIFICATIONS

Electrical Specifications

Table 1-3-2 for 60 Hz and Table 1-3-3 for 50 Hz list electrical specifications. Main or standby power is distributed by six branch circuit breakers, including one rated at 50 amperes, and five rated at 30 amperes. Auxiliary power is distributed by five branch circuit breakers, including one rated at 45 amperes, and four rated at 20 amperes. Normal generator loading is 50 to 100 percent of rated capacity; the generator will withstand continuous 20 percent overload, and momentary direct short. Generator output will be maintained for 50 to 200 milliseconds after loss of input, depending upon the system load being carried.

Physical Specifications

Generator Drive Motor - 7.5 horsepower for 5 KVA unit, 15 horsepower for 7.5 KVA unit. The motor is a continuous duty, low slip induction type, with a speed of 1760 RPM at 60 Hz input, or 1450 RPM at 50 Hz input. Temperature rise of 99 degrees F (37.2 degrees C).

Generator - 5 KVA or 7.5 KVA capacity. Temperature rise of 72 degrees F (22.2 degrees C).

Motor Generator Weight - 262 lbs for the 5 KVA unit, 400 lbs for the 7.5 KVA unit.

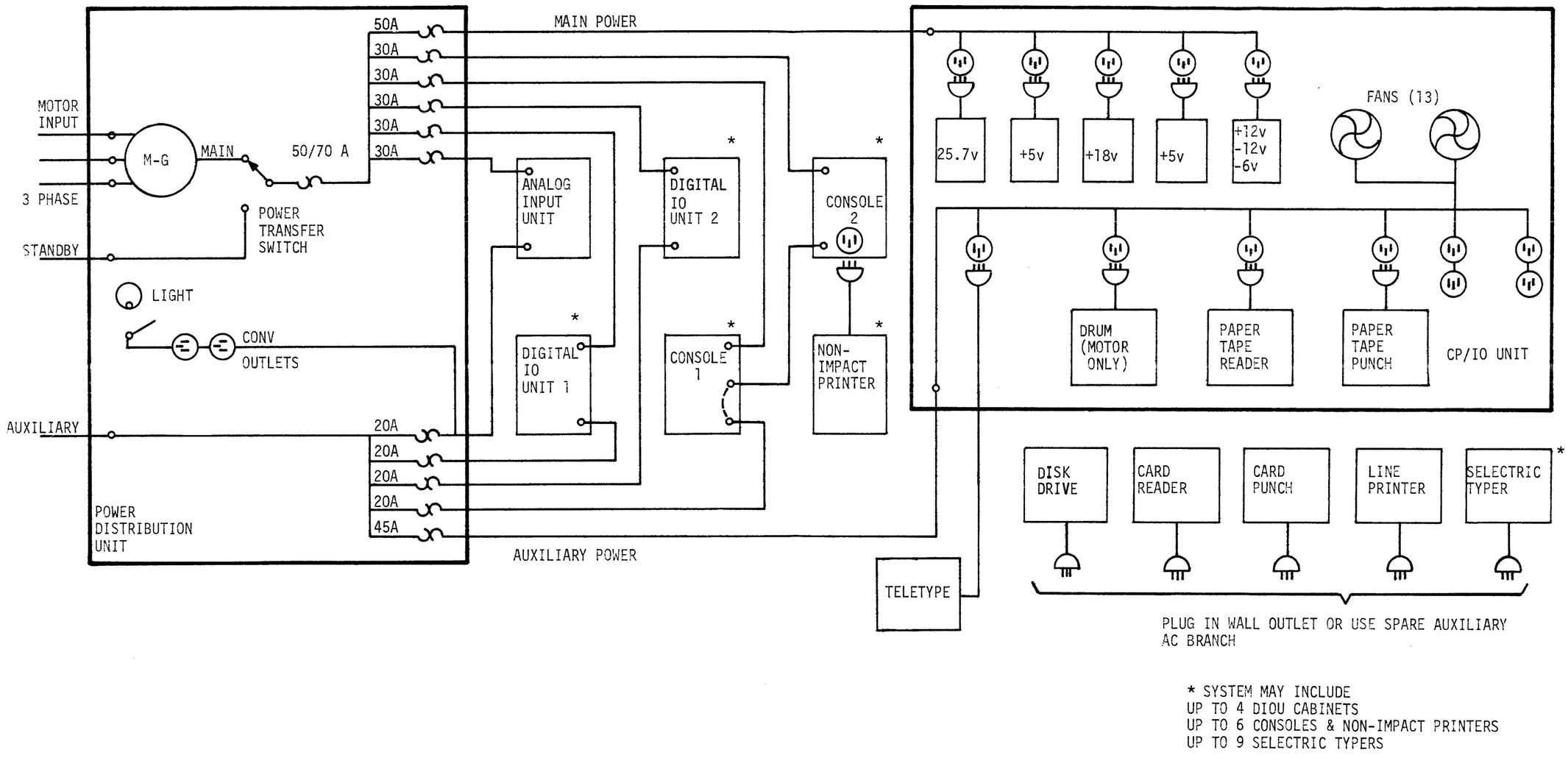


Figure 1-3-7. Typical System AC Power Distribution

Table 1-3-2. PDU Electrical Specifications -- 60 Hz Input

SERVICE	PHASE	FREQUENCY (HZ)			VOLTAGE			CURRENT (A)	
		NOM	MIN	MAX	NOM	MIN	MAX	5 KVA	7.5 KVA
MOTOR INPUT	3	60	58	62	208	187.2	228.8	20	39
					220	198	242	20	39
					440	396	484	10	19.5
STANDBY INPUT (Transient-Free) Harmonic Distortion: 4%, Max	1	60	58	62	120	108	132	50	70
AUXILIARY INPUT	1	60	57	63	120	108	132	70	70
GENERATOR OUTPUT[1] (Min Volt, Full Load; Max Volt, No Load) Harmonic Distortion: 4%, Max	1	400	396	430	120	108	136	50	70

[1]Based on a 0.9 power factor

Table 1-3-3. PDU Electrical Specifications -- 50 Hz Input

SERVICE	PHASE	FREQUENCY (HZ)			VOLTAGE			CURRENT (A)	
		NOM	MIN	MAX	NOM	MIN	MAX	5 KVA	7.5 KVA
MOTOR INPUT	3	50	48	52	220	198	242	20.8	41
					380	342	418	12	24
STANDBY INPUT (Transient-Free) Harmonic Distortion: 4%, Max	1	50	48	52	120	108	132	50	70
AUXILIARY INPUT	1	50	47	53	120	108	132	70	70
GENERATOR OUTPUT[1] (Min Volt, Full Load; Max Volt, No Load) Harmonic Distortion: 4%, Max	1	400	372	411	120	108	136	50	70

[1]Based on a 0.9 power factor

Cabinet Dimensions -

a. Height 78.59 inches
b. Width 34.31 inches
c. Depth 26.13 inches

Cabinet Weight, Fully Equipped - approximately 500 lbs for the 5 KVA unit, 750 lbs for the 7.5 KVA unit.

Environmental Specifications

Temperature - The ambient temperature range with the equipment operating is 40 to 120 degrees F (4.4 to 49 degrees C). Ambient termperature range for storage is -30 to +150 degrees F (-34.4 to 66 degrees C). The maximum rate of operating temperature change is 19.8 degrees F/hr (11 degrees C/hr) up to the maximum operating temperature. The only cooling requirement is free air flow.

Relative Humidity - 10 to 95 percent (up to 86 degrees F, wet bulb).

Ambient Air Contamination - up to 10 ppm hydrogen sulfide or sulfur dioxide.

Altitude- The equipment will operate at altitudes ranging from -1000 feet up to 6,000 feet. For transport or storage, the altitude range extends to 50,000 feet.

Noise Level - 83 dB measured at 3 feet on the B scale in accordance with ASA Z24-7-1950.

Vibration - Per MIL-STD-810B, data 15 June 1967, Method 514, Figure 514-6, Curve AB, as follows:

5 to 27 Hz	±1.0 g (peak), Sinusoidal Input
27 to 52 Hz	0.036 inches (Double amplitude displacement), Sinusoidal Input
52 to 300 Hz	±5.0 g (peak), Sinusoidal Input

SECTION 4
TELETYPE

The Teletype (reference designation 07) provides low-speed bidirectional communication between the programmer and the computer. Primarily used for program development, it also provides backup for an inoperative typer or paper tape reader or punch. It can also be used for regular output duty in noncritical areas such as special logs.

The Teletype is available in two models. The Keyboard Send/Receive (KSR) model contains a keyboard for entering information and a page printer for typing out information. The Automatic Send/Receive (ASR) model also contains a paper tape reader and a paper tape punch. All operate asynchronously at 10 characters per second. Data transmission is in ASCII code, serially at 110 Baud/second.

Either LOCAL or ON LINE operation can be selected by the operator. Local operation disconnects the unit from the computer to prevent any interaction. The programmer can then use the keyboard to type out and/or punch a program, or use the tape reader to copy and/or type out the contents of a punched tape, as selected by the MODE switch.

On-line operations are more extensive, and involve interaction with the computer. Using the keyboard, the programmer can type characters to be interpreted as commands or data by the computer, according to the program being run. Thus the programmer may interrogate memory, compile or assemble new programs, work with data files, or do any other permissible on-line operations. All keyboard input is simultaneously printed by the page printer for verification, when in the K or KT mode. The computer can also control the page printer/punch for recording special types of information (logs, alarm messages, printouts, etc), as well as using them

to replace a failed typer or paper tape punch. When used as such, the unit automatically turns on with the first character, and turns off after the last character to increase motor life.

The Teletype is used in conjunction with a Teletype Synchronizer of the System Interface Nest in Wing 1 of the CP/IO Unit; and a one-line output buffer on the Drum, the Input and Output Device Driver and Teletype Handler routines in the Input/Output Control Software (IOCS), and the operator communications routines of the Console Software System. The standard FOX 1 System supports one teletype unit, which uses the Programmed Input/Output (PIO) bus, as shown in Figure 1-4-1.

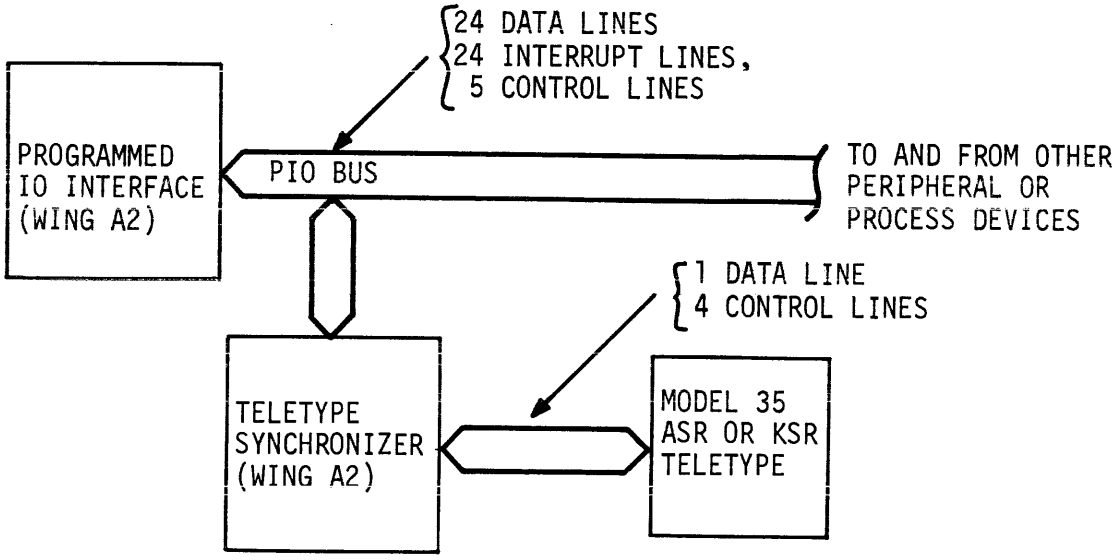


Figure 1-4-1. Teletype Signal Interconnections

TELETYPE SPECIFICATIONS - ASR MODEL

Operating

Operating Rate	10 characters per second
Line Length	7.2 inches
Line Spacing	6 per inch
Character Spacing	10 per inch
Printing Characters	Numerical: 0 to 9
	Alphabetical: A to Z
	Symbolical: /@#$=%<+>↑←\
	Punctuation: .,:;!?'-"()[]
Character Transmission	11-Unit Serial
	(Start, 8 Data, 2 Stop)
Character Punching	8 Data + Feed/row
Controls	MODE (K,KT,T,TTS,TTR)
	ON LINE/OFF/LOC.
	LOC C R (Local Carriage Return)
	LOC L F (Local Line Feed)
	LOC B SP (Local Back Space)
	REPT (Repeat)
	TIMEOUT BYPASS
	MANUAL INTERRUPT
	tape reader FREE/STOP/RUN
Indicators	End-Of-Line
	Print Location
	Chad Box Full

Physical

Height	40 inches
Width	41.5 inches
Depth	24.5 inches
Weight	320 pounds

TELETYPE SPECIFICATIONS - ASR MODEL (contd)

Power

Signal Power	50 mA at +10VDC(space) 500 mA at -15VDC (mark)
Voltage	115VAC±10% single phase
Current	5 Amperes
Frequency	50±0.5 or 60±0.5 Hertz
Dissipation	207 Watts

Environmental

Temperature	32 to 130 degrees F
Humidity	30 to 90% noncondensing

TELETYPE SPECIFICATIONS - KSR MODEL

Operating

Operating Rate	10 characters per second
Line Length	7.2 inches
Line Spacing	6 per inch
Character Spacing	10 per inch
Printing Characters	Numerical: 0 to 9 Alphabetical: A to Z Symbolical: /@#$=%<+>↑←\ Punctuation: .,:;!?'-"()[]
Character Transmission	11-Unit Serial (Start, 8 Data, 2 Stop)

TELETYPE SPECIFICATIONS - KSR MODEL (contd)

Controls	ON LINE/OFF/LOC.
	LOC C R (Local Carriage Return)
	LOC L F (Local Line Feed)
	LOC B SP (Local Back Space)
	REPT (Repeat)
	TIMEOUT BYPASS
	MANUAL INTERRUPT
Indicators	End-Of-Line
	Print Location

Physical

Height	38.5 inches
Width	20 inches
Depth	24 inches
Weight	150 pounds

Power

Signal Power	50 mA at +10VDC (space)
	500 mA at -15VDC (mark)
Voltage	115VAC±10% single phase
Current	3 Amperes
Frequency	50±0.5 or 60±0.5 Hertz

Environmental

Temperature	32 to 130 degrees F
Humidity	30 to 90% noncondensing

SECTION 5
PAPER TAPE READER AND PUNCH

The paper tape reader and punch are used for transfer of information to and from the computer memory. The information may be programs and/or data; in binary, ASCII, or other code. (System software determines the interpretation and use of the information received from the reader.) Asynchronous operation from the computer is accomplished using the Paper Tape Reader/Punch Synchronizer in Wing 3 of the CP/IO Unit. The Reader and Punch use the Programmed Input/Output (PIO) Bus as shown in Figure 1-5-1.

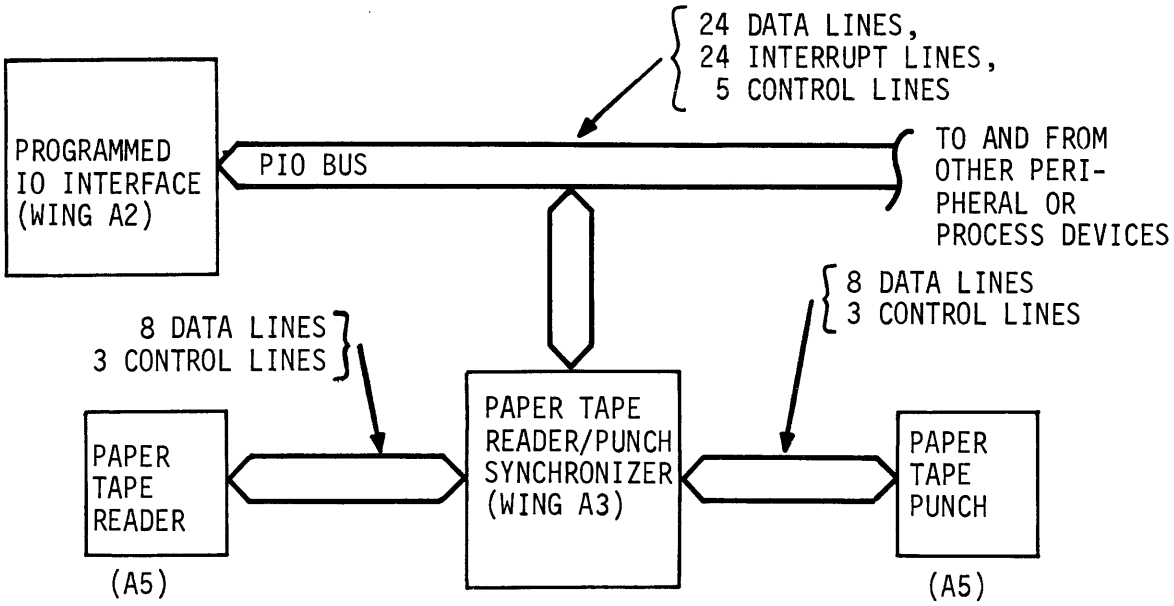


Figure 1-5-1. Paper Tape Reader and Punch Signal Interconnections

PAPER TAPE READER

The paper tape reader (reference designation 01 A5 A3) is a rack-mounted unit on the main trunk of the computer, directly below the Control Panel. It consists of a tape transport and photoelectric reader mechanism, interface and control circuits, and either a tape spooler or pair of fanfold tape holders. It reads either 5-, 7- or 8-channel paper or Mylar tape at up to 300 frames per second (asynchronous operation). The tape reels (when supplied) hold 300 feet of 4.5-mil tape (32,000 frames) or 540 feet of 2.5-mil tape (64,000 frames). The spooler (if used) rewinds tape at 40 inches per second.

The paper tape reader is software controlled by the Input Device Driver and Paper Tape Reader Handler routines in the Input/Output Control Software (IOCS).

PAPER TAPE READER SPECIFICATIONS

Operating

Tape Material	Paper or Aluminized Mylar
Tape Size	1 inch wide, 2.5 to 5.0 mils thick
Hole Sensing	Photoelectric
Start Time	15 milliseconds
Slewing Rates - Reader:	30 inches/second reading,
- Spooler (Reel Models Only):	40 inches/second (rewinding)
Stop Distance	0.045 inch
Reading Rate	300 frames/second slew
	150 frames/second incremental mode
Reel Size	4.875 inches

PAPER TAPE READER SPECIFICATIONS (contd)

Reel Capacity	300 ft of 4.5-mil tape, 540 ft of 2.5-mil tape
Controls	OFF/LOAD/RUN 5/7/8 channel OFF/ON/REWIND reel model

Physical

Height	7 inches
Width	19 inches
Depth	8.5 inches behind panel, 2.75 inches projection

Power

Voltage	117 VAC ±10% single phase
Frequency	48 to 62 Hertz
Current	1.125 Amp fanfold model 2.75 Amps reel model
Dissipation	135 Watts fanfold model 450 Watts reel model

Environmental

Temperature	Operating: 32 to 131 degrees F Storage: -65 to 150 degrees F
Humidity	Operating: 10 to 90 percent Storage: 0 to 100% noncondensing
Altitude	Operating: -1000 to +10,000 feet Storage: -1000 to +50,000 feet

PAPER TAPE PUNCH

The paper tape punch (reference designation 01 A5 A4) is a rack-mounted unit on the main frame of the computer, below the paper tape reader. It consists of a punch mechanism, interface and control circuits, and either a tape spooler or a fan-fold tape holder. It punches 8-level tape at 60 frames per second. The punch can handle paper tape from 2.5 to 5 mils thick. It operates asynchronously from the computer by way of an output buffer.

The paper tape punch is software controlled by the Output Device Driver and Paper Tape Punch Handler routines in the Input/Output Control Software.

PAPER TAPE PUNCH SPECIFICATIONS

Operating

Tape Size	1 inch wide, 2.5 to 5 mils thick
Tape Material	Paper
Holes Punched	Per EIA RS-227
Punching Rate	60 frames/second
Frame Spacing	10 per inch

Physical

Height	10.5 inches
Width	19 inches
Depth	14.5 inches, behind panel, 2.75 inches projection

PAPER TAPE PUNCH SPECIFICATIONS (contd)

Power

Voltage	117 VAC ±10%, single phase
Frequency	50 ±2 or 60 ±2 Hertz
Current	2 Amperes fan-fold model
	2.5 Amperes reel model
Dissipation	230 Watts fan-fold model
	280 Watts reel model

Environmental

Temperature	Operating: 32 to 120 degrees F
	Storage: -65 to 150 degrees F
Humidity	Operating: 10 to 90 percent
	Storage: 0 to 100 percent noncondensing
Altitude	Operating: -1000 to +10,000 feet
	Storage: -1000 to +50,000 feet

SECTION 6
CARD READER AND PUNCH

The card reader and punch transfer information to and from the computer memory, operating asynchronously by way of the card reader/punch synchronizer in the I/O Wing. The information contained in the cards may be programs and/or data, in binary or Hollerith codes: interpretation, use and selection is determined by the program using the card reader or punch. These units use the Programmed Input/Output (PIO) and Channel Input/Output (CIO) buses, as shown in Figure 1-6-1.

CARD READER

The card reader (reference designation 09) is a desk-top unit, permitting convenient location and ease of operation. Its hoppers hold 600 cards, which can be read at up to 300 cards per minute. It reads standard paper cards punched in 80 columns of 12 rows. The reader operates automatically on-line, performing self checks to ensure proper operation. Off-line operation is also possible for testing and maintenance purposes. The reader is controlled from the card reader synchronizer hardware in the computer. Software control is from the Input Device Driver and Card Reader Handler routines in the Input/Output Control Software (IOCS).

CARD READER SPECIFICATIONS

Operating

Card Stock	7.375 x 3.25 inch, 80-pound paper

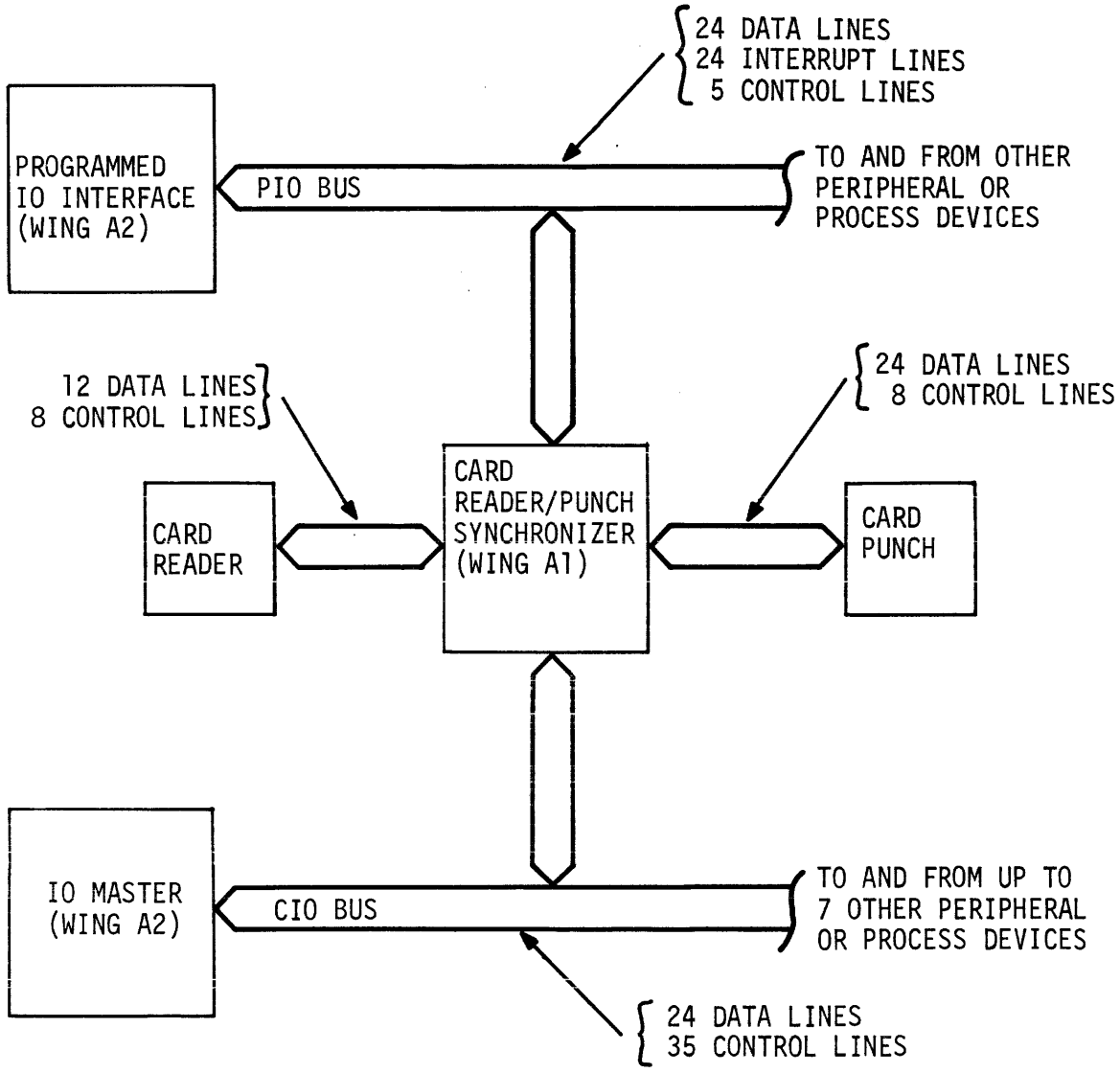


Figure 1-6-1. Card Reader and Punch Signal Interconnections

CARD READER SPECIFICATIONS (contd)

Card Punching	12 row, 80 column rectangular
Hole Sensing	Photoelectric
Hopper Capacities	600 cards
Reading Rate	300 cards/minute 5 cards/second
Error Detection	Sensor Malfunction Card Feed Failure Card Discharge Failure
Indicating Control Switches	STOP START OFF ON
Maintenance Switches	READ OFF-LINE FAST READ OFF-LINE SLOW MARGIN CHECK HIGH MARGIN CHECK LOW
Indicators	HOPPER READY FEED READ

Physical

Height	15 inches
Width	23 inches
Depth	17.5 inches
Weight	70 pounds

Power

Voltage	115 or 220VAC±10%, single phase
Frequency	50 ±2 or 60 ±3 Hertz
Current	Starting: 10 Amperes Running: 6 Amperes
Power	750 VA

CARD READER SPECIFICATIONS (contd)

Environmental

Temperature	Operating: 50 to 100 degrees F
	Storage: 0 to 135 degrees F
Humidity	Operating: 10 to 90 percent
	Storage: 5 to 95% noncondensing
Altitude	Operating: -250 to +10,000 feet
	Storage: -1000 to +50,000 feet

CARD PUNCH

The card punch (reference designation 10) is a free-standing unit on casters, permitting convenient location and ease of operation. Its hoppers hold 1000 cards, which are punched at up to 90 cards per minute. Punching is done one column at a time, in 12 rows, for all 80 columns. Before a column is punched, the received data are echoed back to the card reader/punch synchronizer, where they are checked to verify reception of each specified bit. The card punch operates automatically on-line, performing self checks to ensure proper operation. (Off-line operation is also possible for testing and maintenance purposes.) After operation it turns off automatically to prolong motor life.

The card punch interfaces with the computer through the card reader/punch synchronizer, and is software controlled by the Output Device Driver and Card Punch Handler routines in the Input/Output Control Software.

CARD PUNCH SPECIFICATIONS

Operating

Card Stock	3.25 x 7.375 inch, 80-pound paper
Hopper Capacities	1000 cards
Hole Punching	12 row, 80 column, rectangular
Punching Rate	90 cards/minute 1.5 cards/second
Error Detection	Full/Missing Chip Box Card Feed Failure Card Discharge Failure Input Hopper Empty Output Stacker Full
Panel Indicators	POWER, TEST MODE, CHIP BOX, NON-PICK, HOLD, HOPPER FULL, HOPPER EMPTY
Panel Control Switches	ON/OFF, HOLD, MASTER CLEAR
Maintenance Switches	AUTO SHUTOFF ON/OFF AUTOPUNCH ON/OFF TEST PATTERN ON/OFF

Physical

Height	42 inches
Width	37.5 inches
Depth	33 inches
Weight	500 pounds

CARD PUNCH SPECIFICATIONS (contd)

Power

Voltage	115 or 220 VAC ±10% single phase
Frequency	50 ±2 or 60 ±2 Hertz
Current	Starting: 20 Amperes
	Running: 14 Amperes
Power	2.4 KVA

Environmental

Temperature	Operating: 50 to 100 degrees F
	Storage: 0 to 135 degrees F
Humidity	Storage: 5 to 95% noncondensing
	Operating: 10 to 90%
Altitude	Operating: -250 to +10,000 feet
	Storage: -1000 to +50,000 feet

SECTION 7
LINE PRINTER

The line printer is a high-speed output device for recording large amounts of data from the computer. It is especially valuable for large and/or frequent logging operations and for extensive on-line program development, as well as for background data processing operations. It prints alphanumeric characters and symbols on continuous fanfold paper, 24 characters at a time. A full line of 132 characters is printed in 205 milliseconds, with 20 milliseconds more to advance the paper for the next line, yielding an effective rate of 245 full lines per minute. Shorter lines are printed faster, with 1110 lines of 24 characters per minute the fastest rate.

Print hammer life is greater than half-a-billion operations; sealed bearings and oil-impregnated brushes eliminate the need for lubrication. Integrated control circuitry provides off-line self testing capabilities. Paper loading and ribbon changing is accomplished from the front of the unit through a swinging drum gate.

The line printer uses both the PIO and CIO buses, as illustrated in Figure 1-7-1. The PIO bus is used to initiate the transfer operation, and the CIO bus is used for the actual transfer of data. Interfacing between the line printer and the computer is provided by the line printer synchronizer in the I/O wing of the computer. Software control is provided by the Output Driver and Line Printer Handler routines in the Input/Output Control Software (IOCS).

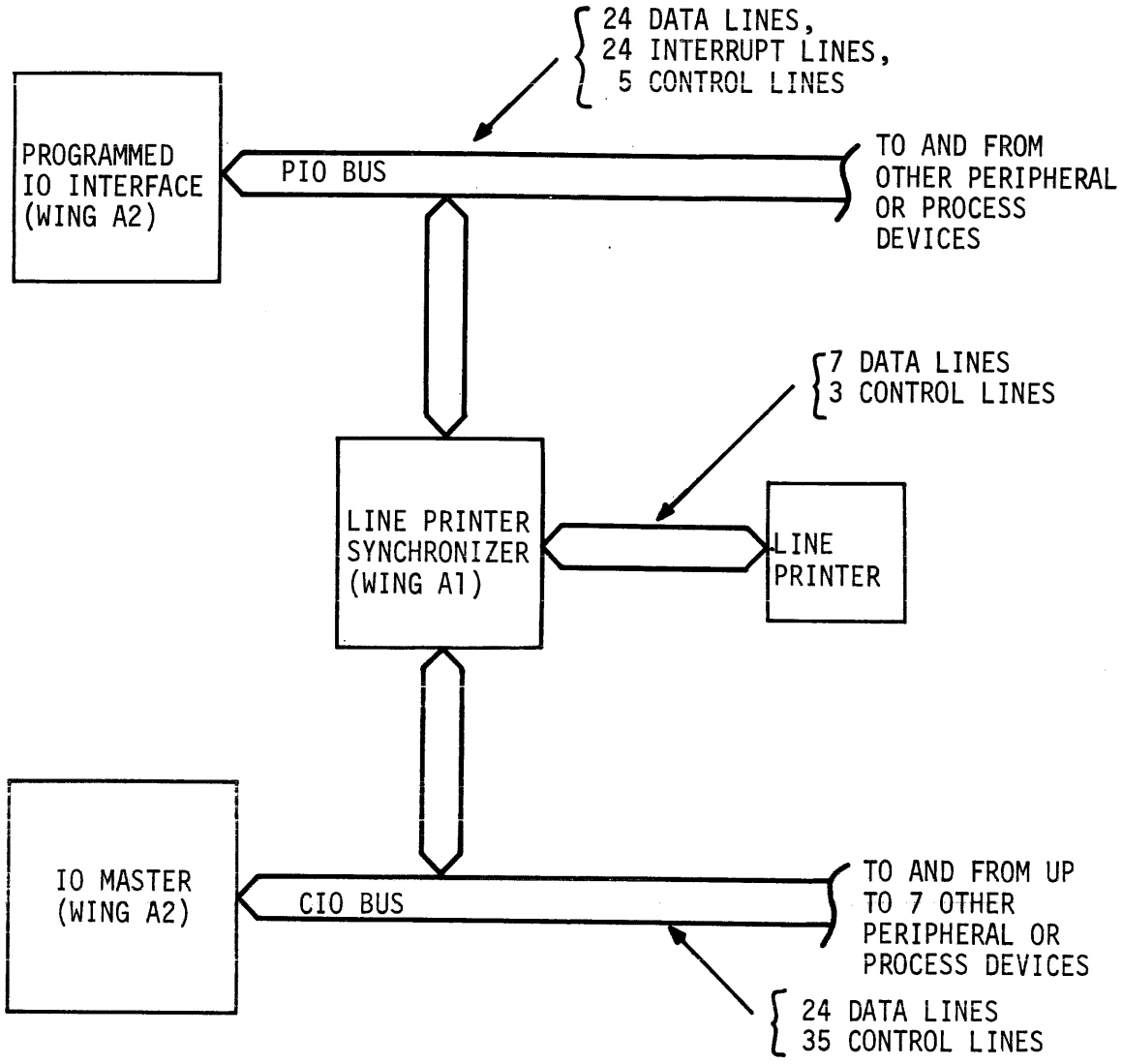


Figure 1-7-1. Line Printer Signal Interconnections

All information is stored and transmitted in ASCII code, three 8-bit characters per word. Sixty-three visible (printable) characters are used in common, along with the appropriate invisible (nonprinting) function characters. All code conversion is done automatically by the device synchronizer, with unrecognized codes treated as no-operations. The line printer can back up and be backed up by logging typewriters, the card punch, and the paper tape punch.

LINE PRINTER SPECIFICATIONS

Operating

Paper Slew Speed	13 inches per second
Line Advance Time	20 milliseconds
Drum Rotation	1760 revolutions per minute
	34.1 milliseconds per revolution
Panel Indicators	POWER
	READY
Panel Control Switches	FORM FEED
	LINE FEED
	ON-LINE/OFF-LINE
Maintenance Switches	POWER ON/OFF
	MASTER CLEAR
	INHIBIT PRINT
Adjustments	Multiple Copy
	Paper Width
	Vertical Position (±1 line)
	Horizontal Tension
	Vertical Tension
Maintenance Indicators	DRUM GATE
	PAPER FAULT
	PRINT INHIBIT

LINE PRINTER SPECIFICATIONS (contd)

Printing Rate:	
24 characters/line	1110 lines/minute
48 characters/line	650 lines/minute
72 characters/line	460 lines/minute
96 characters/line	356 lines/minute
120 characters/line	290 lines/minute
132 characters/line	245 lines/minute

Printing

Character Font	Gothic
Printing Characters	Numerical: 0 to 9 Alphabetical: A to Z Symbolical: /@#&*$=%<+>\^ Punctuation: .,:;!?'-"()[]
Nonprinting Characters	Space, Line Feed, Form Feed, Carriage Return
Character Spacing	10 per inch
Line Spacing	6 per inch
Line Length	13.2 inches

Paper

Type	Edge-punched perforated fanfold, single copy (min. 15-lb bond) to 6-part multi-copy (max. 12-lb bond) with integral one-use carbon sheets.
Size	11 inches between folds, 4 to 14.875 inches wide.

LINE PRINTER SPECIFICATIONS (contd)

Physical

Height	48 inches
Width	50 inches
Depth	26 inches
Weight	600 pounds

Power

Voltage	117 VAC±10%, single phase
Frequency	50 ±2 or 60 ±2 Hertz
Current	Starting: 10 Amperes
	Running: 6 Amperes
Dissipation	500 Watts

Environmental

Temperature	Operating: 50 to 110 degrees F
	Storage: 0 to 125 degrees F
Humidity	Operating: 5 to 80 percent
	Storage: 5 to 95% noncondensing
Altitude	Operating: -1000 to +10,000 feet
	Storage: -1000 to +50,000 feet

SECTION 8
TYPERS

The typers (reference designation 06) are used for permanently recording operating information such as process logs, plant reports, status and alarm messages, and shift summaries. They are Selectric typewriters that use a moving typehead/stationary platen mechanism to type alphanumeric data in two colors at speeds greater than 15 charcters per second. The typers have either a 50 or 60 Hertz motor, a 10 or 12 pitch escapement, and 9.375 or 13.625 inch pin-feed platen. Information transmitted to the typers is in ASCII code, three eight-bit characters per word. Sixty-three visible (printable) characters are used in common, along with the invisible nonprinting function characters. The typers can back up and be backed up by the line printer, the card punch, and the paper tape punch.

Interfacing between the typers and the computer is provided by the typer synchronizer in the I/O wing (Figure 1-8-1). The typer synchronizer contains nine two-card controllers, which are implemented only when the associated typer is connected to the system. A separate cable connects each typer to the synchronizer.

The typers are software controlled by the Output Driver and Typewriter Handler routines in the Input/Output Control Software (IOCS). Up to nine typers may be controlled simultaneously in overlapping fashion.

TYPER SPECIFICATIONS

Operating

Type Face	Manifold 12

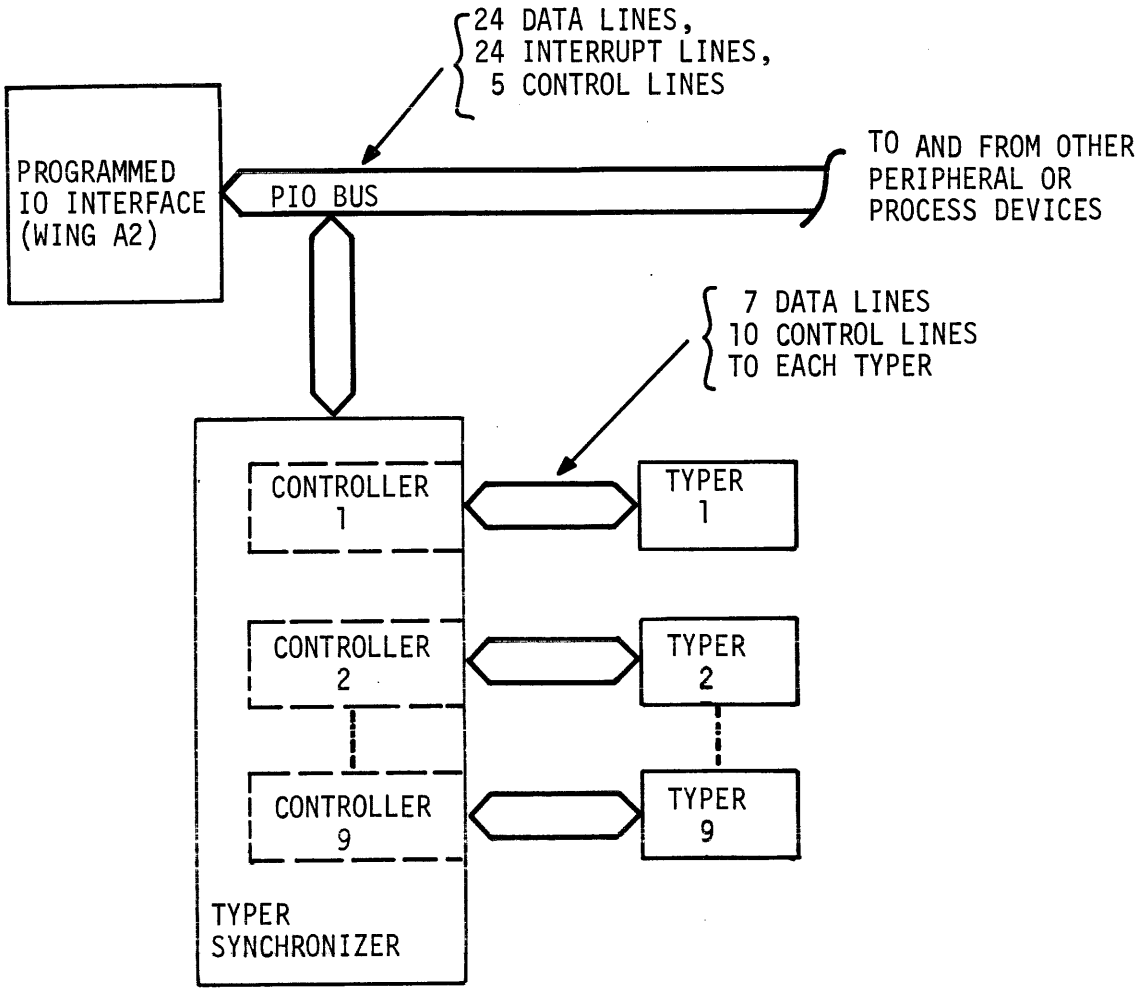


Figure 1-8-1. Typer Signal Interconnections

TYPER SPECIFICATIONS (contd)

Typing Characters	Numerical: 0 to 9 Alphabetical: A to Z Symbolical: /@#&*$=%<+>| Punctuation: .,:;!?'-"()[]
Function Characters	Tab, Space, Red Shift, Black Shift, Carriage Return/Line Feed
Speed	15.5 characters/second
Pitch	10 or 12 characters/inch
Line Spacing	6 per inch
Line Length	8 or 12.25 inches
Platen	Pin Feed, 9.375 or 13.625 inches
Ribbon	Red & black

Physical

Height	9.5 inches
Width	17.5 or 22 inches
Depth	16 inches
Weight	53 or 61 pounds

Power

Voltage	115 VAC ±10%, single phase
Frequency	50 ±2 or 60 ±2 Hertz
Current	0.7 Amperes
Dissipation	120 Watts

SECTION 9
DISK MEMORY SUBSYSTEM

The Disk Memory Subsystem is an optional element for storing and transferring large amounts of information. It consists of one to four disk drive units, a variable quantity of removable disk cartridges, a disk memory synchronizer in Wing 4 of the CP/IO Unit, and an integrated set of programs and routines in the FOX 1 software. Each disk drive unit handles one two-sided fourteen-inch diameter magnetic oxide-coated aluminum disk in a removable disk cartridge, and a second, nonremovable disk on the same spindle. Storage capacity is 831, 488 data words per disk, with a maximum of 6,651,904 words available on-line, in a fully-implemented subsystem. The disk drive units are mounted in cabinets, each cabinet containing up to two units.

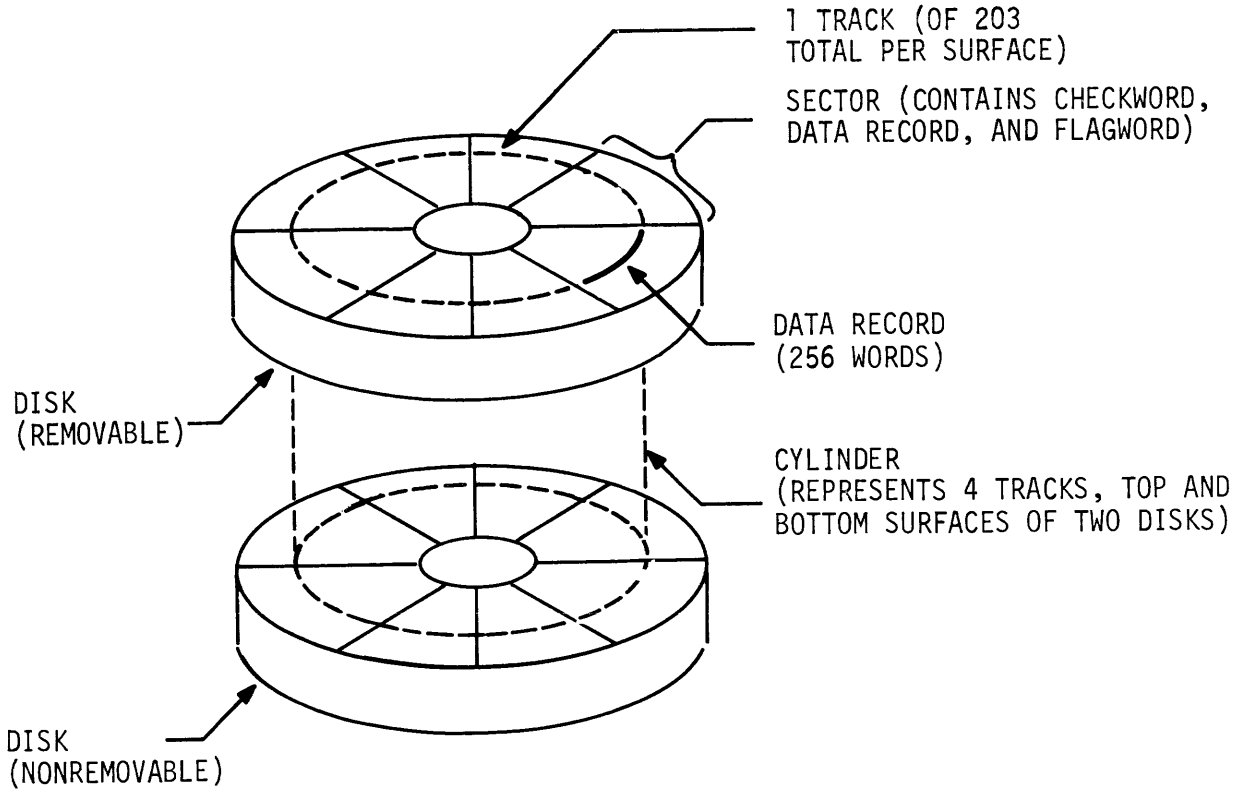


Figure 1-9-1. Disk Data Organization

Both top and bottom surfaces of each disk are recorded. Each surface contains 203 circular tracks, each holding 2048 data words (Figure 1-9-1). The circular tracks are divided into eight sectors, each containing a 256-word data record, a 24-bit flag word for data record identification, and a 24-bit check word for error determination.

The disk drives include four read/write heads (one for each recording surface), mounted in an assembly. The heads move in unison, and are positioned over corresponding tracks on the disk surfaces. The 203 recording positions of the heads thus represent 203 cylinders, each containing four tracks.

The disk drives are connected in daisy-chain fashion as shown in Figure 1-9-2. Both the PIO and CIO buses are used, the PIO bus for initiating the operation and the CIO bus for the actual transfer of data.

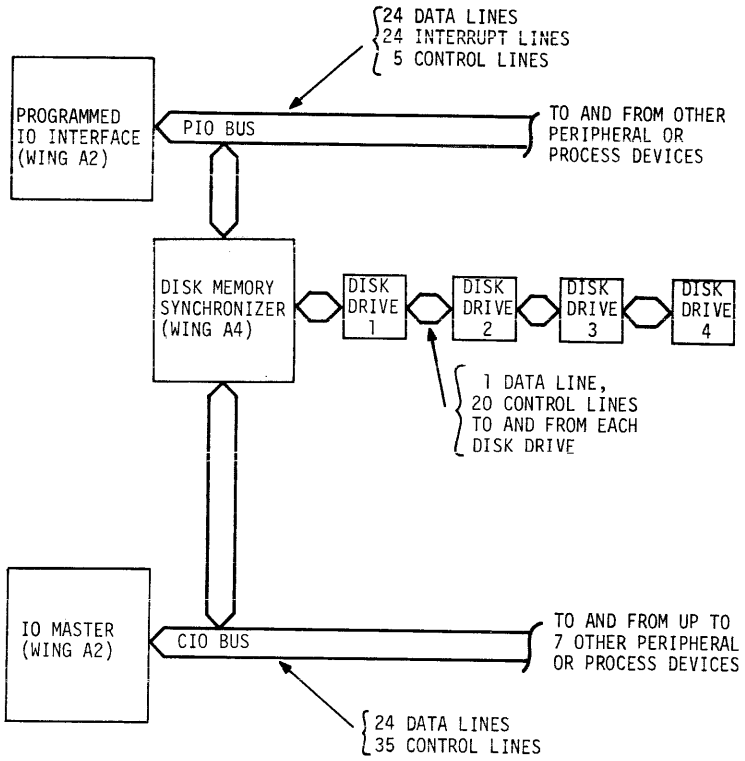


Figure 1-9-2. Disk Memory Signal Interconnections (Fully Complemented Subsystem

OPERATION

Operation occurs in two computer-initiated phases: a record acquisition (seeking) phase and a data transfer (reading or writing) phase. During the record acquisition phase, first the heads are positioned over the specified cylinder. Head positioning time ranges from 15 milliseconds for adjacent cylinders to 110 milliseconds for full-stroke travel, with an average of 60 milliseconds. An optical detent positions the head over the selected cylinder to within 0.2 mils. Note that during the time the head positioning is taking place on one drive, seeks and data transfers on other drives may be executed and/or initiated.

The drive then locates the sector preceding the specified sector. Sector location takes up to 25 milliseconds, with an average of 12.5 milliseconds. Maximum seeking time is thus 135 milliseconds, with an average of 75 milliseconds. When the preceding sector is located, the synchronizer notifies the computer, which then has up to 3.1 milliseconds (sector time) to initiate the data transfer phase before losing a revolution.

During the second phase of the operation, the data transfer phase, data are transferred in 24-bit words, over a high-speed direct memory access channel. Transfers may be initiated for blocks of 1 to 256 words; however, the synchronizer reads or writes only full 256 word records from (or onto) the disk. Therefore, a read or write operation of any size will always require the same time as a read or write of a full sector. When less than a full 256 word record is to be written on the disk, the record is filled out with zeros by the synchronizer to make it exactly 256 words long. When less than a 256 word record is read from the disk, only the firstword, lastword, and those in between are transmitted by the synchronizer to the central processor.

Actual data transfer, initiated by a CIO command, may be executed only after a seeking phase has been completed. The CIO command causes the synchronizer to become "busy" until all data have been transferred. Upon receipt of the CIO command, the synchronizer compares its most recent record acquisition information (consisting of disk, head, cylinder, and sector data) against that recorded in the flag word associated with the requested record. This comparison takes place before any data transfer is allowed to occur; any detected error causes termination of the sequence and discontinues any chaining operation.

PRESERVATION OF DATA INTEGRITY

Integrity of the data stored and transferred is preserved by many features in both the hardware and software. In the hardware category, the disk memory synchronizer (1) responds to any core memory parity error; (2) computes a checkword for every record written or read (and compares it with the stored checkword); (3) checks all transfer commands for prohibited actions, correct record address, and size; and (4) determines whether core memory failed to store or supply information fast enough to maintain synchronization. The synchronizer uses the checkword associated with a particular record to check the parity of that record. The checkword is generated, written, and read by the synchronizer hardware; it is not software accessible.

The software is implemented such that a checkword error (computed value disagrees with recorded value) is initially classified as a recoverable error, and the record is read again. After several unsuccessful attempts it is reclassified as a nonrecoverable error, and the operator is notified. Recoverable errors are those transient errors caused by loose dirt particles on the disk surface, and which are brushed off by the head. Nonrecoverable errors are nontransient errors, usually caused by particles that are inbedded in the surface or cause scraping off of the

oxide coating. Flexibility of checkword design allows it to be affected by both transient and nontransient discrepancies.

Stored data can be verified using either of two verification modes: Read Verify or Write Verify. These are initiated by CIO commands and are implemented by the disk drive synchronizer. In the Read Verify mode the synchronizer reads a record, computes a checkword, and compares it to the checkword read from the disk. In the Write Verify mode the synchronizer compares data from the disk against data from the computer core memory, one word at a time; the synchronizer then computes a checkword and compares it to the checkword read from the disk, as in the Read Verify mode.

RELIABILITY AND SECURITY

The disk drive units are designed for reliable, trouble-free operation. Design life exceeds five years or 24,000 operating hours, with an MBTF of 4500 hours. They operate 1200 hours between routine maintenance checks and require no field adjustments for normal operation. Particle contamination is minimized by operation in a positive-pressure atmosphere filtered to remove more than 99.97 percent of all particles greater than 0.3 microns in size. Operation is prevented if the cover is not closed and locked, and the ambient air has not been purged for at least 1.5 minutes. The heads are automatically unloaded (lifted from their flying positions and retracted beyond the disk edge) if the cover is unlocked, the speed drops, power is lost, or the position transducer lamp fails. An off-line exerciser, consisting of a special printed circuit card, provides a quick check of any disk unit without using the computer. Electrical design and construction meet all requirements of Underwriters Laboratories standard 478 for Data Processing Units.

DISK DRIVE UNIT POWER

A separate power supply in each cabinet provides dc power for one or two disk drive units. The power supply incorporates circuits to detect loss of ac power, sense any undervoltage condition, and provide protection against overcurrent conditions.

SUMMARY OF FEATURES

- 6,651,904 words on-line capacity
- 15 to 110 millisecond head positioning time
- 75 millisecond average latent time
- 2400 rpm, 25 milliseconds/resolution
- Optical detent on head positioning
- *Automatic checkword generation and comparison: Longitudinal byte parity, bit checksum, oxide continuity checking
- *Simultaneous seek and transfer operations
- *Transfer command chaining
- *Automatic error checking (terminates transfer): command, timing, power continuity
- Automatic malfunction detection (prevents operation): cartridge loading, cover lock, spindle speed, multiple head selection, power loss, bulb burnout

- Automatic head unloading on malfunction
- Power down sequencing
- Write protection switch
- *Data verification, no transferring or rewriting
- Filtered positive-pressure atmosphere
- Off-line exerciser

*Synchronizer features (not characteristic of disk drive).

DISK MEMORY SPECIFICATIONS

Operating

Disk Drive Units	1 to 4
Removable Disk/Unit	1
Permanent Disk/Unit	1 (optional)
Disk Capacity	831,488 words
Cylinders/Surface	203 tracks per surface
Sectors/Cylinder	8
Words/Sector	256
Transfer Time/Sector	3.125 msec
Access Time	up to 25 msec
Acquisition Time	up to 110 msec
Total Latency Time	Less than 75 msec average

Physical

Cabinet

Height	56 inches
Width	23 inches
Depth	33 inches
Weight	500 pounds
Disk Drive Units/Cabinet	1 or 2
Power Supplies	1

Disk Drive Unit

Height	18 inches
Width	19 inches
Depth	29 inches
Weight	110 pounds
Dissipation	700 Watts/unit maximum, including power supply
Rotation	2400 rpm
Disks	1 removable cartridge, 1 nonremovable disk (optional)
Indicators	READY/SAFE
Switches	START/STOP

Disk Cartridge

Diameter	15 inches
Thickness	1.43 inches
Weight	~4.5 pounds
Capacity	831,488 words
Bit Density	2200/inch
Cylinder Density	100/inch

Power

Disk Drive

Volts	115/230 ±10% VAC, single phase
Frequency	50/60 ±2 Hertz
Current	6 Amperes

Environmental

Temperature	Operating: 65 to 95 degrees F
	Storage: 20 to 165 degrees F
Thermal Shock	20 degrees F/hr maximum
Humidity	Operating: 0 to 80 percent noncondensing
	Storage: 5 to 95 percent noncondensing
Altitude*	Operating: -250 to 10,000 feet
	Storage: -1000 to 50,000 feet
Shock*	Operating: 10 g at 11 milliseconds
	Shipping: 5 g, 1 to 300 Hertz
Vibration*	1-10 Hertz: 0.15 g
(sinusoidal)	10-100 Hertz: 0.25 g

*Untested design objectives

SECTION 10
COMMUNICATIONS MODULE

The communications module provides a means of communication between the FOX 1 computer and distant data terminals or other computer systems. At the time of this printing the ultimate configuration of the communications module had not been established, so detailed information is not yet presented. This section will be revised to describe the communications module as information becomes available.

SECTION 11
CONSOLE

The console (Reference Designation 5) is the primary means of interactive communication between the computer control system and its users. It provides for complete finger-tip control of the plant and its processes, as well as of the control system, at one central location.

Figure 1-11-1 shows the console controls and indicators. Most of the console functions are based on the use of a cathode ray tube (CRT) for dynamically displaying a large amount of information in a centralized viewing area.

A semiconductor refresh memory stores the information being displayed; a keyboard provides a means of requesting and modifying information displayed, and indicating or initiating specific control actions. The keyboard gives the user control over the display, the computer, and the process, consistent with the restraints within the system.

CONSOLE CONFIGURATIONS

The basic console unit contains the CRT assembly, refresh memory, one of two types of keyboards, and all control circuitry and power supplies mounted in a stand-alone console. Available options are:

a. A vector generator for graphic display capabilities.

b. Up to two Foxboro Series 64 Trend Recorders, and/or up to twelve alarm lamp assemblies. (8 alarm lamps per assembly)

c. A separately enclosed nonimpact printer.

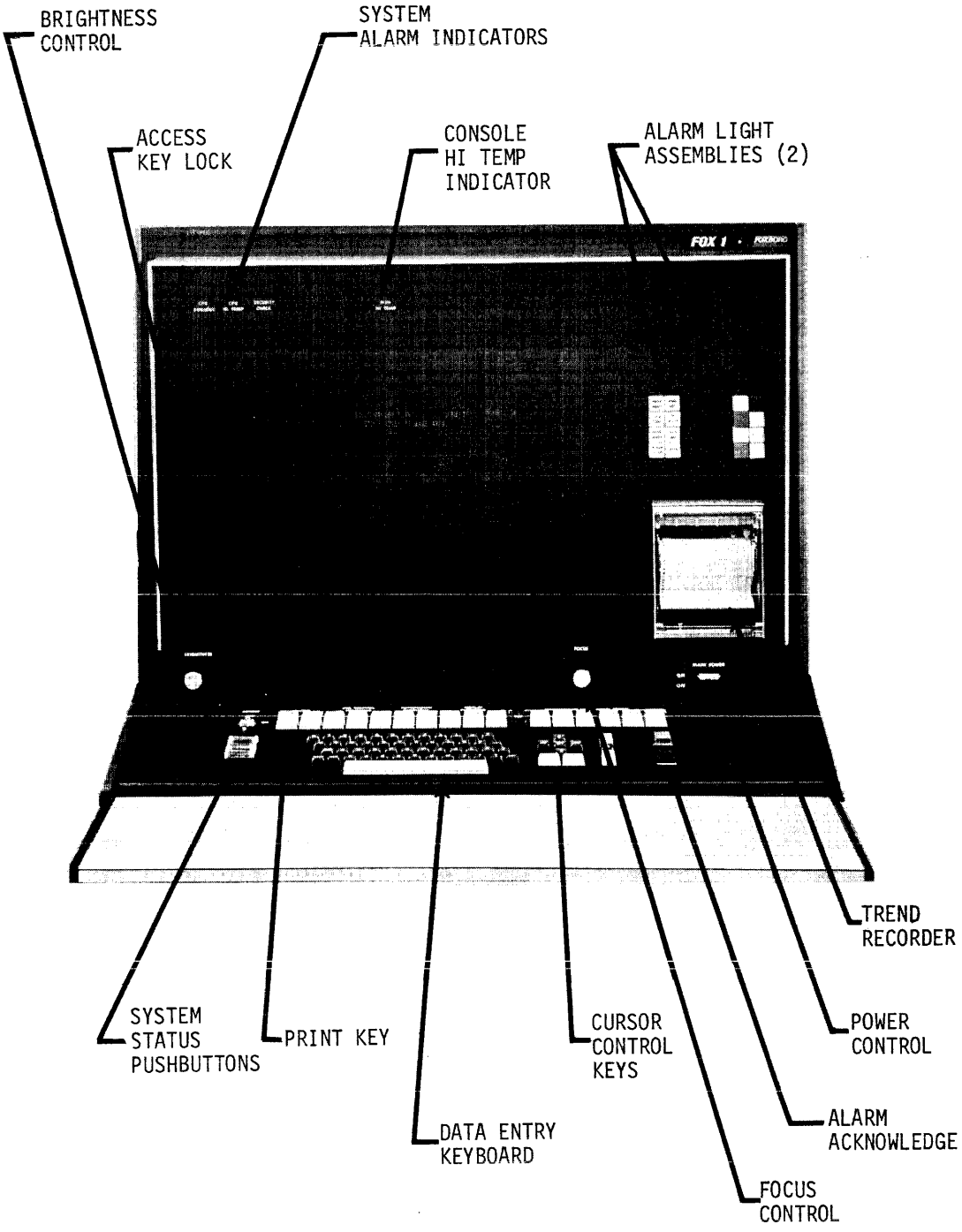


Figure 1-11-1. Console Controls and Displays

Up to six independent console units (with their options) may be employed in a FOX 1 Control System. Separate items used in conjunction with the consoles are: the optional nonimpact printer; a console synchronizer (in the computer IO wing); and a comprehensive package of programs, routines, tables, and files within the FOX 1 software. The console uses the PIO and CIO buses, as shown in Figure 1-11-2.

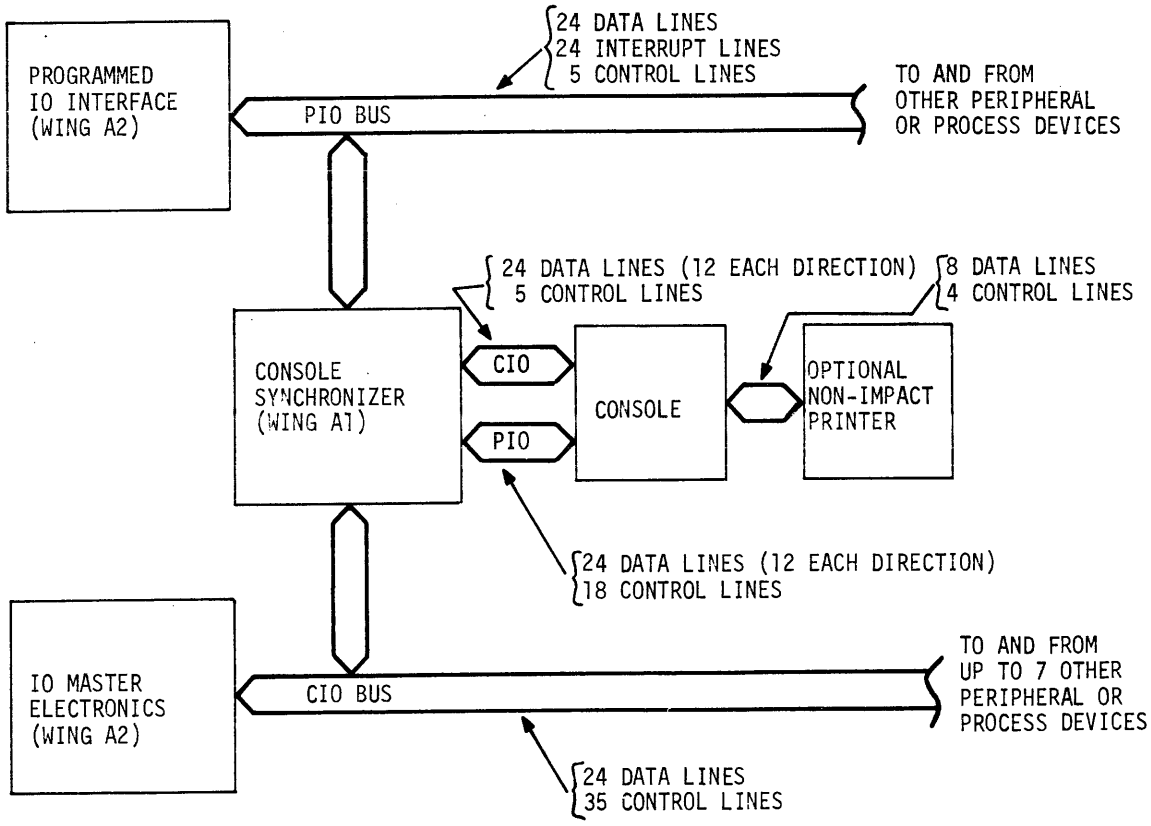


Figure 1-11-2. Console Signal Interconnections (Single-Console Configuration)

CRT ASSEMBLY

The CRT Assembly is a modular unit containing a 21-inch cathode ray tube, associated beam control circuits, and high-voltage power supplies. It resembles the chassis of a television receiver with solid-state controls, and slides in and out of the console for fast and easy access.

Electrostatic focus is used to provide a sharp 30- to 40-mil spot, and electromagnetic deflection is used to position the spot on the screen. The display area measures 12 by 15 inches and has 800,000 addressable locations in an 800 by 1000 matrix. It is subdivided into 2000 character spaces arranged in 25 rows and 80 columns. Characters are written in these spaces in a left-to-right, top-to-bottom pattern. Each space displays the alphanumeric character contained in its associated location in the refresh memory -- characters are traced out in an 8 by 16 dot matrix measuring approximately 1/8 by 1/4 inches. Characters are formed by a character generator, using a read-only memory.

Display capacity is further increased by a settling detector, which determines the minimum time required for spot repeatability within ±0.015 inches. The settling detector is also used with a phosphor protector circuit to automatically dim the intensity if a spot location does not change, preventing the screen from being burned in the event of a malfunction. Linearity within ±0.15 inches is achieved with two linearity compensation circuits that reduce the pincushion distortion.

REFRESH MEMORY

All information displayed on the screen is stored in a semiconductor refresh memory of 2048 12-bit words. During a refresh cycle the first 2000 words are read sequentially, and sent to a character generator (or an optional vector generator). The memory location of each character word corresponds to a particular location on the console screen; that is, the first 80 characters go into the 80 character spaces on the first line, and so forth.

Each character word contains one 8-bit ASCII character and 4 bits of control data, or a 10-bit vector component and 2 bits of control data. Two successive words are required to define a vector; the first for the

vector mode and the X coordinate, the second for the line type and the Y coordinate. The refresh memory can also be read by the computer CIO master and by the nonimpact printer.

Information can be written into the refresh memory from both the computer and the keyboard. The computer transfers individual words or blocks of up to 2000 words (a display format file) over its channel IO direct memory access channel. Thus, it both updates the current display with live data or gives a totally new display. The keyboard can enter an individual character at the cursor location if the character already there is not protected. Any character space can be protected to prevent its being changed.

CHARACTER AND VECTOR GENERATORS

The character generator produces the beam movement and unblanking signals which actually write the characters onto the CRT screen. Character words are decoded by a read-only memory (ROM) in the character generator. It provides the series of deflection and intensification signals required. Each character starts at the lower left corner of its 8 by 16 matrix, and is drawn by moving the beam one position at a time in the required direction.

When a vector is to be drawn, the deflection and intensification information is supplied by the (optional) vector generator. A vector is either absolute or relative, and can be displayed as an invisible line (blanked movement to a new starting location), a dotted line (three consecutive dots alternately on and off), a dashed line (eight consecutive dots alternately on and off), or a solid line (all dots intensified). In absolute vectors, the ten-bit coordinates are positive displacement values referenced from the lower left corner of the display area -- the vector is drawn to this absolute location from wherever the

last vector ended. Relative vectors use signed values to specify the end of the line relative to the location where the last vector ended. Both types use the end point of the last vector as the starting point. Each vector is drawn at an 80 nanosecond/dot rate. Total maximum connected vector length that can be drawn exceeds 3000 inches.

KEYBOARDS

Each console contains one of two different types of keyboards: a general purpose keyboard (Figure 1-11-3) or a process operator's keyboard (Figure 1-11-4). Direct control of the process is performed by the process operator using the process operator's keyboard. It provides the easiest and fastest method of obtaining and modifying actual control data such as setpoints; and for substituting values. Alphabetical and numerical key matrices permit easy specification of loop and block identification and values. Special jogging keys increase or decrease the value of a specified setpoint, input, or output when pressed.

The general purpose keyboard permits all functions except jogging to be performed. It is primarily designed for supervisory control, on-line program development, and data base manipulation. It has a complete 50-key alphanumerical keyboard which provides all 64 ASCII characters, and a set of special job control function keys. The latter permit pushbutton control of the various steps and actions (jobs) required in on-line program development and testing.

All the necessary logic for a keyboard is located on a printed circuit board, which is mounted directly beneath the keyboard. This logic interfaces with either type of keyboard.

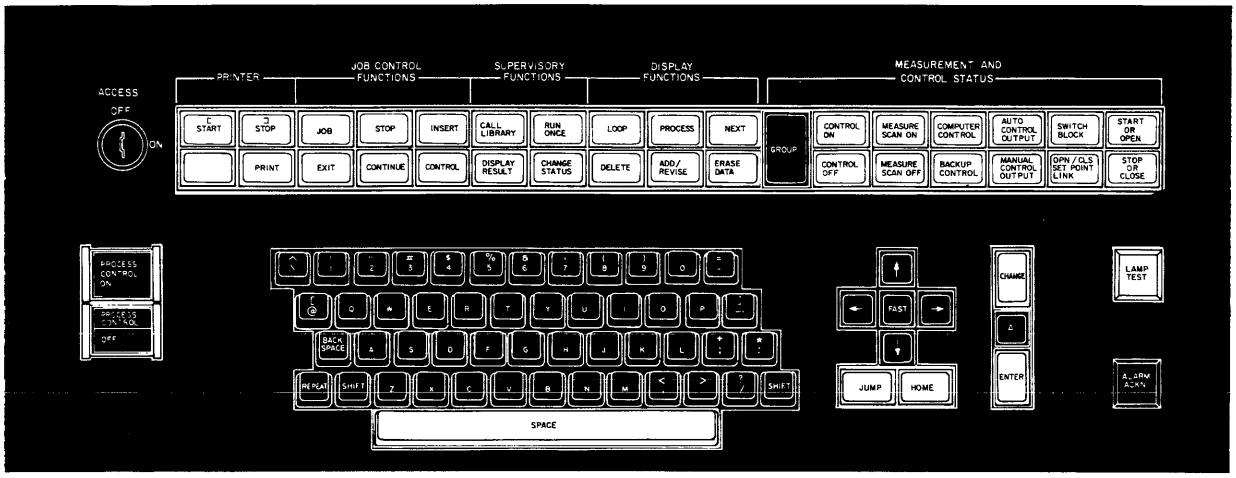


Figure 1-11-3. General Purpose Keyboard

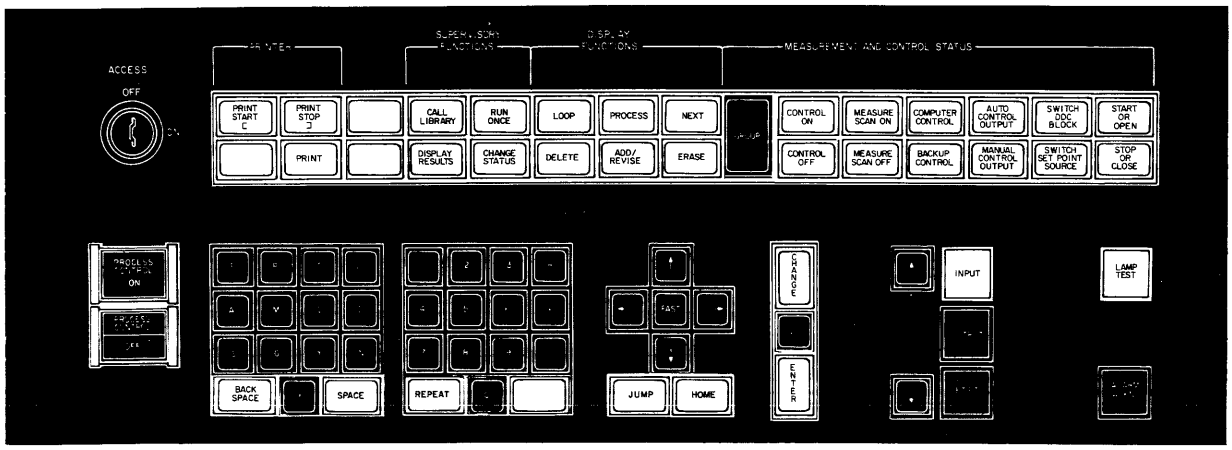


Figure 1-11-4. Process Operator's Keyboard

NONIMPACT PRINTER

The nonimpact printer (Reference Designation 12) provides printed copies of the alphanumeric information displayed on the console screen, or any other alphanumeric data output from the computer, such as operating logs and status reports. It is capable of printing 120 characters per second on 80-character lines. Characters are printed sequentially from 8-level ASCII code on standard 8.5-inch roll paper. The 62 printing characters include all numerals, uppercase letters, punctuation, and common symbols. Nonprinting characters include two spaces and other control characters.

Printing is accomplished by electrostatically deflecting a jet of minute ink drops. Characters are formed by placing the drops in an eight-by-ten matrix as defined by an internal character generator. The ink is continuously heated and circulated past 40 fixed nozzles by a diaphragm pump -- the only moving part in the printing mechanism. Ink usage is very low -- about 125 million characters (1.4 million full lines) between each 1/2-pint filling, enough to fill about fifty 400-foot rolls of paper.

The paper transport uses four separate motors; one to feed paper into the mechanism and maintain a tensionless loop, one to space accurately the paper at six lines to the inch, one to maintain tension in the printing and viewing area, and one to roll up to the printed paper. These provide smooth paper control at slewing rates up to 60 lines per second.

Operation is completely automatic. The printer turns itself on upon receipt of a character from the computer or the display, then asynchronously decodes and prints the character or performs the function specified. It turns itself off automatically about 20 seconds after the last character was accepted. Internal safety circuits check for proper operating temperature and deflection voltages, and adequate paper supply. If any item is not normal the printer rejects incoming data, turns its READY lamp off, and signals the CPU by means of an error flag.

TREND RECORDERS

One or two Foxboro Series 64H Recorders can be mounted in each console unit. Each two-speed recorder has up to three separate pens. A printed circuit digital to analog converter card for each recorder is included in the console unit to provide the analog signals for the pens. Each card has three circuits which accept ten-bit data words and provide 10 to 50 milliampere output currents.

ALARM LAMP ASSEMBLIES

These optional illuminated pushbuttons (shown in Figure 1-11-1) play a vital role in man/machine communications. They indicate both acknowledged and unacknowledged alarm conditions and call for a specific CRT display. Up to twelve alarm lamp assemblies can be mounted in a single console, each assembly being made up of eight pushbuttons. Two types of assemblies are available -- process alarm lamp assemblies and computer alarm lamp assemblies. The process alarm lamp assemblies monitor field contacts directly; the computer alarm lamp assemblies monitor out-of-tolerance field measurements or computed values, and are operated by the computer.

Each pushbutton of either type of assembly is associated with a specific process or unit variable. Pressing the pushbutton causes a pertinent display and its live data to be shown instantly on the screen. Each console unit can mount one process alarm lamp assembly and up to eleven computer alarm lamp assemblies. If a trend recorder is mounted in a console unit, only six assemblies can be accommodated.

INTER-CABINET INTERFACING

Figure 1-11-5 shows the cable connections between the console unit cabinet and the CP/IO unit cabinet, and between the console unit cabinet and the nonimpact printer cabinet. Twisted-pair wire cables and differential drivers and receivers are used for these communications, for reliable operation in a high electrical-noise environment.

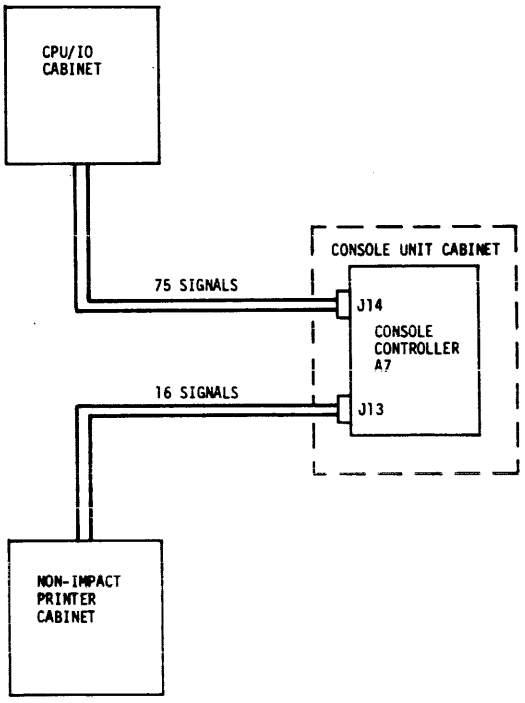


Figure 1-11-5. Cable Interconnections

FIELD INTERFACE

Communications between the Console Unit and the "field" consist of signals to control the process alarm lamps, and miscellaneous system security signals which operate the alarm horn, mounted in the console unit. Both types of signals connect directly to the console unit. The

number of signals used is dependent upon application, but cannot exceed 16 process alarm lamp signals and 10 system security signals.

SUMMARY OF CONSOLE FEATURES

- Large Display Capacity -- 2000 ASCII characters
- High Resolution Characters -- 1/4 inch high, 8 x 16 overlapping matrix
- Graphic Capability -- 1000 straight-line vectors
- Electromagnetic Deflection -- best positioning
- Electrostatic Focus -- sharpest spot
- Phosphor Protection -- longer CRT life
- Settling Time Detector -- increased display capacity
- Linearity Compensation -- minimum distortion
- Pushbutton Display Callup -- preprogrammed formats
- Live Process Display -- updated values
- Blink Capability -- quick identification
- Hard Copy Option -- 120 characters per second
- Line Synchronization -- minimizes flicker

- Analog Trend Recording
- Keyboard Entry
- Drip-proof Cabinet
- Overtemperature Alarm
- High Voltage Protection
- Ease of Maintenance: slide-out console controller, plug-in printed circuit cards, removable CRT Assembly, prewired options

CONSOLE SPECIFICATIONS

Operating

Display Area	12 by 15 inches
Dot Matrix	800 by 1000 locations
Dot Spacing	0.015 inch
Dot Size	0.03 to 0.04 inch
Brightness	30 foot-Lamberts
Contrast	10:1 in 25 foot-candles ambient
Linearity	±1.0% (±0.15 inch) of full scale
Repeatability	±0.1% (±0.15 inch) of full scale
Drift-Long Term	±1.0% (±0.15 inch) of full scale
Organization	25 rows, 80 characters per row
Character Size	0.12 by 0.24 inch @ dot centers
	8 by 16 dot matrix
Character Set (ASCII Code)	Numbers 0 to 9
	Letters: A to Z
	Symbols: /@#&*$=%<+>^_
	Punctuation: .,:;!?'-"()[]

Line Types	Solid
	Invisible
	Dotted (3 dots alternated)
	Dashed (8 dots alternated)
Connected Line Length	3000 inches
Incrementing Rate	80 nsec/dot
Retrace Time	20 µsec edge-to-edge
Refresh Rate	50 or 60 per second
	(line frequency synchronized)
Capacity	2048 words
	(2000 usable)
Word Size	12 bits
Inputs	Computer and Keyboard
Outputs	Display, Computer, Printer
Controls	Main Power On/Off
	Focus
	Brightness
	Access On/Off
	Miscellaneous Keyboard Functions
Indicators	CPU Stallout
	CPU Hi Temp.
	Security Check
	Console Hi Temp.

Physical

Overall Height	53.125 inches
Shelf Height	29.5 inches
Overall Depth	48.5 inches
Shelf Depth	18.5 inches
Unit Width	33.5 inches
Cable Length	300 ft
Display Tube	21-inch diagonal

Screen Size	15 x 12 inches
Phosphor	P31

Logic Power

(400 Hz Power Distribution Unit recommended)

Voltage	105-133 VAC, single phase
Frequency	47 to 440 Hertz
Current	3 Amperes

CRT and Convenience Power

Voltage	105-133 VAC, single phase
Frequency	47 to 63 Hertz
CRT Current (25 Ampere source)	7 Amperes
Convenience Outlet Current	Fused for 20 Amperes

Environmental

Ambient Light Level	30 foot-candles
Temperature	Operating: +40 to +120 degrees F
	Storage: -30 to +130 degrees F
Thermal Shock	1 degree F/minute
Humidity*	Operating: 20 to 95%, 85 F max wet bulb
	Storage: 0 to 95% noncondensing
Altitude*	Operating: -1000 to +10,000 ft
	Storage: -1000 to +50,000 ft
Trace Contaminants*	H_2S and SO_2

*Untested Design Objectives

NONIMPACT PRINTER SPECIFICATIONS

Printing

Character Font	approx. Gothic
Printing Characters	Numerical: 0 to 9 Alphabetical: A to Z Symbolical: /@#&*$=%<+>↑← Punctuation: .,:;!?'-"()[]
Character Spacing	10 per inch
Line Spacing	6 per inch
Line Length	8 inches
Printing Method	Jetted Ink
Printing Matrix	8 by 10
Printing Rate	120 characters/sec
Paper Slewing Rate	15, 30, 60 lines/sec

Physical

Height	56 inches
Width	18 inches
Depth	26 inches
Weight	380 pounds

Power

Voltage	115 ±10% VAC, single phase
Frequency	60 ±0.5 Hertz
Current	6 Amperes
Dissipation	600 Watts

Operating

Panel Indicators	BREAK
	TRANS START
	PRINTER ON
	READY
	PAPER ADVANCE
	PAPER ALARM
Panel Switches	PRINTER ON
	PAPER ADVANCE
	READY
Maintenance Indicators and Switches	ON/OFF
	PAPER JAM/RESET

Environmental

Temperature	Operating: 40 to 110 degrees F
	Storage: 32 to 110 degrees F
Humidity	10 to 95% noncondensing
Altitude	up to 6,500 feet
Tilt	5 degrees

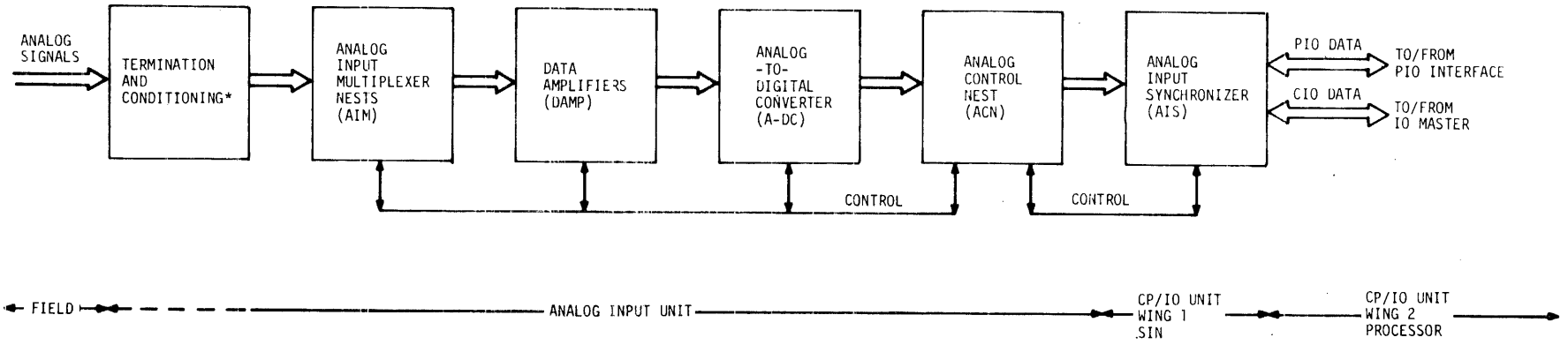
SECTION 12
ANALOG INPUT SUBSYSTEM

The Analog Input Subsystem provides the interface between the Central Processor and all inputs from analog process instrumentation. Primarily, this subsystem selects a specified input signal (point), converts the analog amplitude to a digital representation, and transfers this digital value to the computer. Components of the Analog Input Subsystem are shown in block-diagram form in Figure 1-12-1.

This subsystem is highly modular and can receive up to 2048 inputs from the process. It provides a converted digital value to a resolution of 13 bits plus sign (0.012% of full scale) with an overall accuracy of ±0.1 percent of full scale (±0.15% for 10 mv range). Most signals use complete solid-state switching in the multiplexer, giving a selection-and-conversion rate of up to 5000 points per second (pps). Signals that require a high common-mode rejection (to ±155 volts) use guarded-relay multiplexer switching which operates at 100 pps scanning random points, or up to 1000 pps on sequential scanning.

FUNCTIONAL DESCRIPTION

The Analog Input Subsystem consists of an Analog Input Synchronizer (AIS) and an Analog Input Unit (AIU). In addition, Termination Units (TU) can be part of this subsystem when analog input signals are terminated in a location distant from the AIU. The AIS is part of the System Interface Nest in wing 1 of the CP/IO Unit, and serves as an interface and control unit between the processor (computer) and the AIU. The AIU is the primary element in the subsystem and is shown in Figure 1-12-2. It



*EITHER PART OF ANALOG INPUT UNIT OR SEPARATE TERMINATION UNIT

Figure 1-12-1. Analog Input Subsystem Functional/Physical Block Diagram

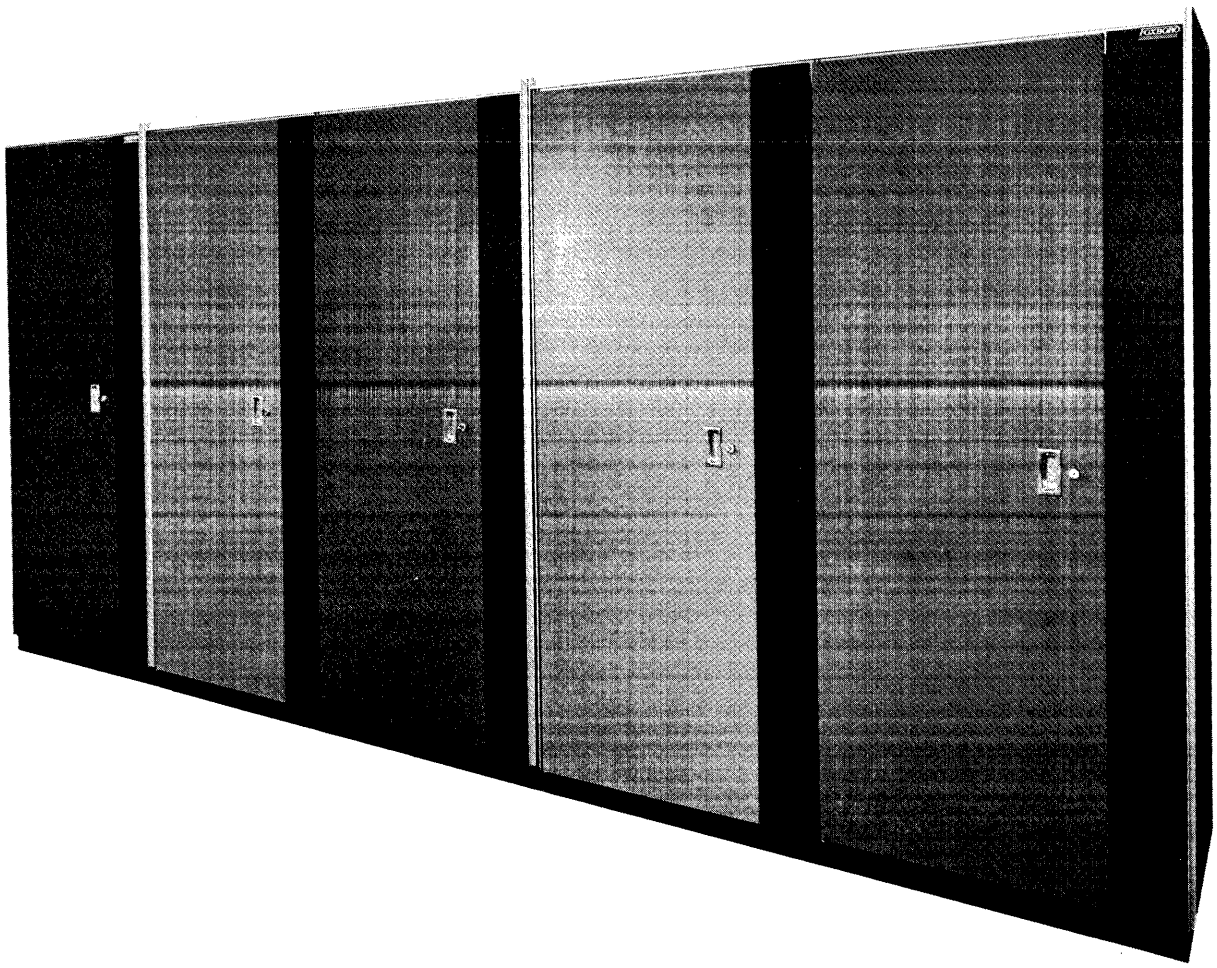


Figure 1-12-2. Typical Analog Input Unit

consists of a control bay plus from one to four other bays that can be either multiplexer bays or UTR (uniform temperature reference) termination panel bays.

A control bay (A3) contains an Analog Control Nest that provides timing and control signals used throughout the AIU, an Analog-to-Digital Converter (ADC) that converts the amplitude of the selected analog input signal to a 14-bit digital representation, an optional Test Panel that can be used to completely exercise the AIU under manual control, and the necessary power supply and distribution elements for the entire AIU. Implementation of the control bay is fixed and does not change except for the addition or deletion of the optional Test Panel and the addition or deletion of a second multi-output power supply for the multiplexer bays (depending upon the number of Analog Input Multiplexer nests in the other bays).

Multiplexer bays contain one or two Analog Input Multiplexer (AIM) nests and one or two Data Amplifiers (DAMP). An AIM nest is an assembly of two rows of multiplexer printed-wiring circuit cards that switch one selected analog input signal to the input of a DAMP. The DAMP provides the amplification appropriate to the signal range to raise the selected signal to the 0-to-10 volt input range of the Analog-to-Digital Converter (ADC).

Termination of analog input signals (connection of field process instrument signals to the multiplexers) is accomplished in one or more of the following ways:

a. Remote: Connections are made to terminal boards on Termination Panels of remote Termination Units (cabinets) and cabled to the AIU multiplexer.

b. Local: One or two bays of the AIU can be assigned as UTR termination panel bays; in which case thermocouple inputs are connected to UTR Termination Panels in these bays, and cabled to adjacent multiplexer bays.

c. Direct: Connections can be made directly to multiplexer bays. In this technique individual field wires are crimped into a connector block which is connected directly to the multiplexer circuit cards or indirectly through a printed-wiring board "paddle" when signal conditioning is required. These "paddles" have an extra set of output signals to provide a 2:1 fan-out capability for connecting trend recorders or similar devices across the inputs, and have a connection for supplying any required power from separate instrumentation power supplies.

UTR termination panel bays can mount four UTR Termination Panels on the front and four UTR Termination Panels on the back. Each UTR panel can terminate up to 32 thermocouple inputs, yielding a maximum of 256 thermocouple inputs per UTR termination panel bay. Temperature on a UTR panel is uniform throughout and this temperature is monitored by a Dynatherm RTD (resistance temperature detector) bulb in the panel. This RTD bulb is connected to a standard RTD multiplexer card for reading by the Analog Input Subsystem (for junction compensation).

The AIU incorporates many good design features which enhance its high operating speed, accuracy, resolution, reliability, and modularity. For example, the accurate, reliable, low-noise analog-to-digital converter is a customized unit that produces a 14-bit 2's complement output within 25 microseconds of point selection. Photon-coupled output and a separate power supply provide total isolation between process inputs and the computer.

The Data Amplifiers are customized, low-noise differential amplifiers. Each amplifier provides a fixed-gain, fixed-bandwidth input to the Analog-to-Digital Converter. An amplifier is set to one of seven different gains and one of five different bandwidths for various input signal ranges. (These settings represent some trade-off between speed and accuracy.)

Configurations of Data Amplifiers and Analog Input Multiplexer nests within a given multiplexer bay are limited to those shown in Figure 1-12-3.

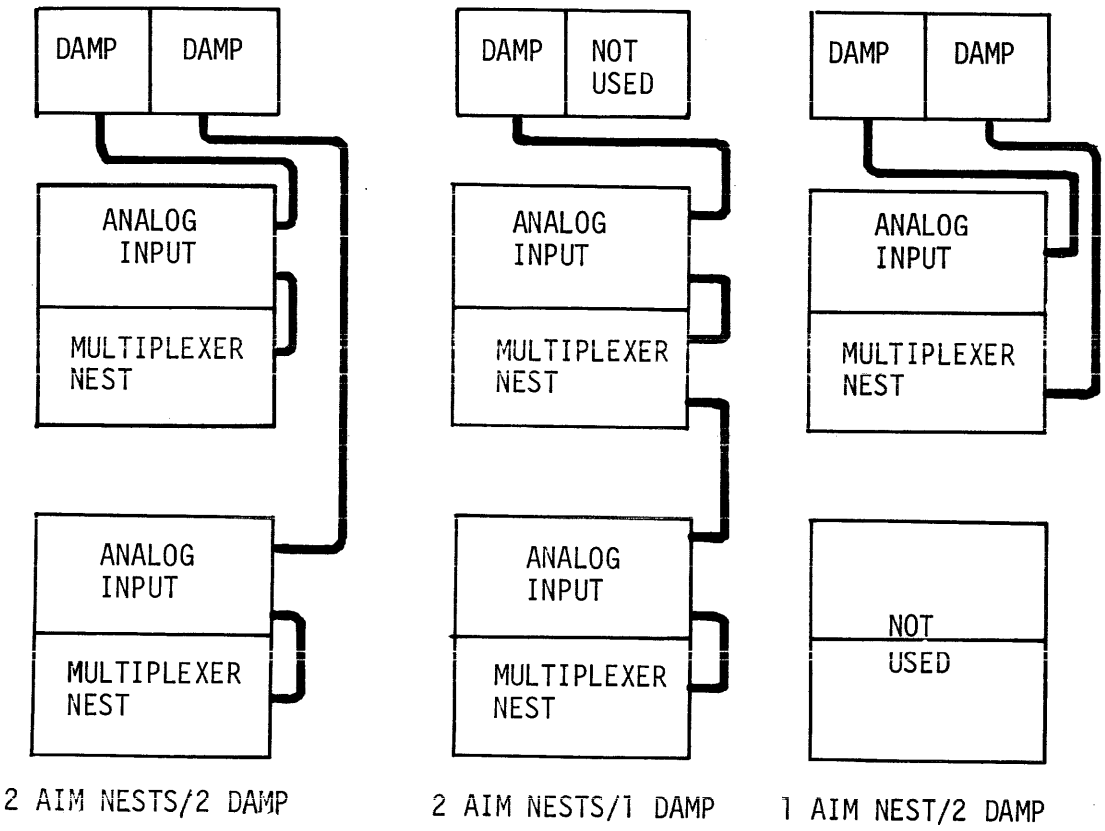


Figure 1-12-3. Multiplexer Bay Configurations

All Analog Input Multiplexer nests are prewired to receive two rows of multiplexer cards. Each of the two rows of an AIM nest accommodates up to 16 multiplexer cards. There are 16 types of interchangeable multiplexer cards available to handle all types of process signals. Each card receives eight voltage or current input signals, or four resistive (RTD) inputs. Any card serving current loops can be removed without opening the loop and losing control

A reference voltage card is used in the highest address position associated with each Data Amplifier. This card provides known precision voltage inputs signals to allow programmed checking and compensation for drift, etc. in the Analog Input Subsystem. Readings taken from this card are used to produce compensation curves (or tables) for all field inputs read through the same logic elements. This operation is completely automatic (performed by programming).

Overall subsystem accuracy of ±0.10 percent of full scale is obtained by the basic accuracy, repeatability, and linearity of the amplifiers and converter; the low offset of the multiplexer switches; the complete electrical isolation with separate signal, analog, and logic grounds; complete driven-guard shielding of the amplifier and multiplexer cards; and self-calibration which compensates for the inevitable amplifier drift and offset (however small).

The Analog Input Subsystem operates in two addressing modes: random and sequential. In random addressing, each input point to be monitored is individually specified by the computer and points can be read in any sequence. In sequential addressing, the first point address and the number of points to be monitored are specified by the computer, then each point is converted and data sent to the computer in sequence for each address in the specified block of point addresses. (Amplifier gain and point addressing are specified to the AIS by a command from the computer as described in detail in the reference chapter on the Analog Input

Subsystem, i.e., Volume 4 Chapter 2 of this manual.) If prespecified, the AIS can request a program interrupt to inform the computer when the last data word of a sequence has been transferred. In sequential addressing, relay multiplexer switching time can be shared among many points, thereby increasing the average points per second rate by a factor of 5 to 10 times the random addressing rate.

Communications between the Analog Input Subsystem and the computer use both the programmed IO (PIO) bus and the channel IO (CIO) bus. The PIO bus transfers status and command data between the computer and the AIS, initiates a random addressing operation, or initiates a sequential addressing operation. Random addressing operations can be executed completely through the PIO bus, or through the CIO bus initiated by the PIO bus. Sequential addressing operations can be executed only through the CIO bus after initiation through the PIO bus.

Both random and sequential operation can be initiated manually from the optional Test Panel. In this manner commands from the computer are inhibited during operations initiated from the Test Panel. This means of operating the AIU allows complete testing and troubleshooting off line.

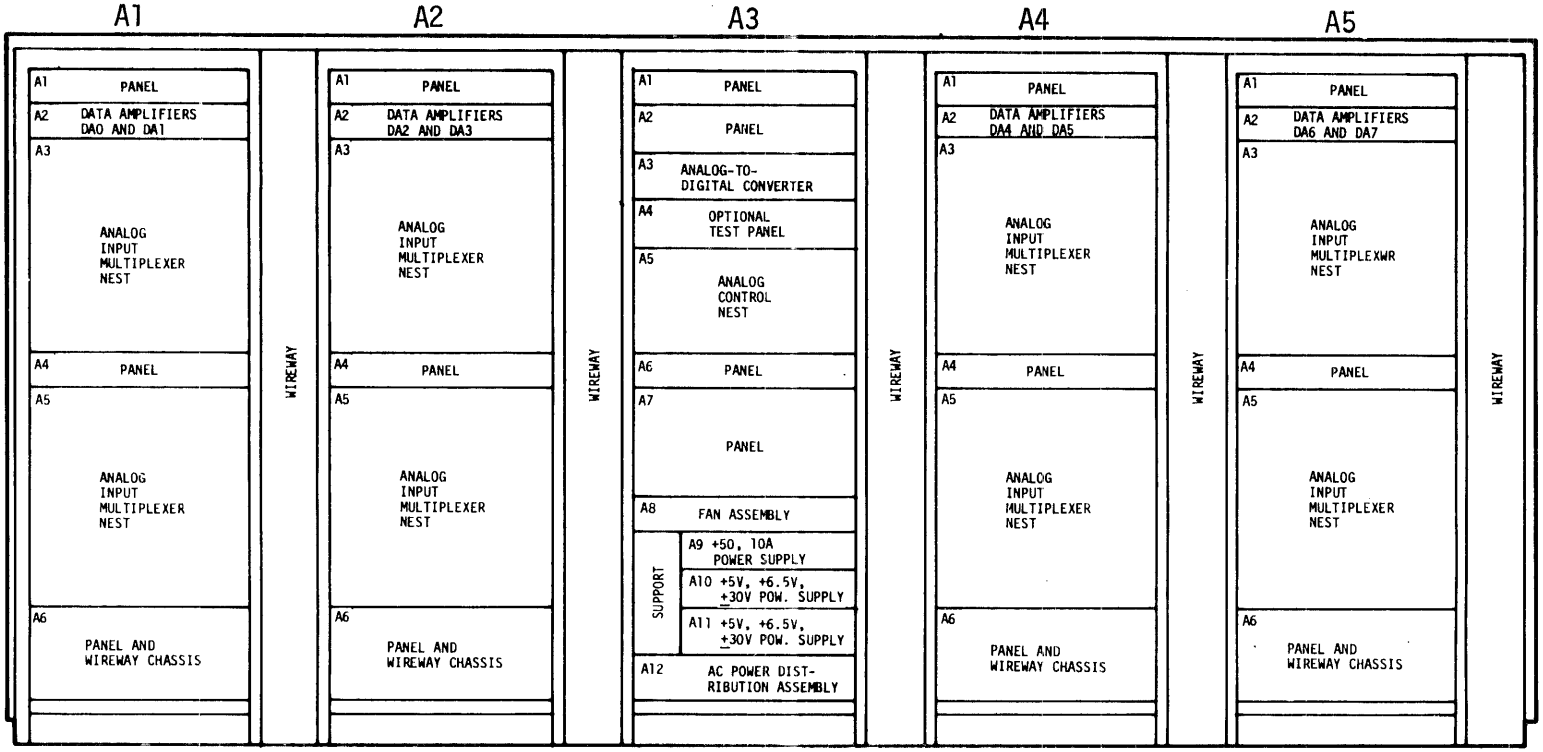
PHYSICAL DESCRIPTION

The physical location of components for a maximum-capacity Analog Input Subsystem is shown in Figure 1-12-4. Smaller configurations can be determined from this illustration by removing multiplexer bays, and/or replacing them with UTR bays.

Analog Input Synchronizer

The AIS consists of seven printed circuit cards in row 1 of the System Interface Nest located in Wing 1 of the CP/IO Unit.

Reference Designator 03A1 for AIU, Cabinet 1



AUI SIZE	BAYS USED					MAX. POINTS
2 BAYS		A2	A3			512
3 BAYS	A1	A2	A3			1024
4 BAYS	A1	A2	A3	A4		1536
5 BAYS	A1	A2	A3	A4	A5	2048

Figure 1-12-4. Analog Input Unit Physical Configuration

Analog Input Unit

The AIU cabinet assembly consists of from two to five standard racks (hereafter referred to as bays). Bays of the AIU are of three types: one control bay per AIU and one to four multiplexer bays and/or UTR termination panel bays.

Cabinets - The AIU cabinet assembly is constructed of from one to five standard bays bolted together. Each bay is 78 inches high, 25.5 inches deep, and 27 inches wide. Internal bay space is divided into a 21-inch wide column for nests and a 6-inch wide column for wireways. Up to 70 vertical inches of nests, up to 25 inches deep, can be installed in a bay. Cable entry and exit ports for each bay are located above and below the wireways. (The preferred cable input-output ports are in the bottom of the bay.) All cabinets are of drip-proof design, yielding a watertight enclosure when the top cable entry ports are not used. Each bay is provided with key-locked doors and a temperature detection circuit that issues an alarm when the internal temperature exceeds 115 ± 5 degrees F. (A thermal switch at the top of each cabinet operates at 130 ± 3 F, which corresponds to an ambient internal temperature of 110 to 120 F.)

Control Bay - The control bay (03A1A3) contains the analog-to-digital converter, the test panel (when provided), the analog control nest, an assembly of six fans, the dc power supplies for the entire AIU, and the ac power distribution unit for the AIU as shown in Figure 1-12-4. All electrical connections between the AIU and the AIS are made by one cable connected to the AIU in the control bay.

Multiplexer Bay - Multiplexer bays contain one or two data amplifiers and one or two analog input multiplexer nests, depending on the configuration required for the number and type of analog input signals to be monitored. All analog input signals from process instrumentation are received by the analog input multiplexer nests.

UTR Bay - Zero, one, or two UTR panel bays can replace multiplexer bays where less than the maximum number of analog inputs are received. One of these bays can hold four UTR Termination Panels inside the front doors, and four UTR Termination Panels inside the back doors.

Reference Designations

The Analog Input Unit is assigned reference designation 03. Only one AIU is permitted per system so the AIU is always designated 03A1. Bays are numbered A1 through A5 from left to right for the maximum-size configuration. A 2-bay AIU has bays A2 and A3 -- all other configurations have bays numbered consecutively from A1 up to A3, A4, or A5. Assemblies within a bay are numbered from top to bottom as A1 through A4, A6, or A12 depending upon the number of assemblies and the type of bay. (Refer to Figure 1-12-4.) Printed-wiring circuit cards within a nest are specified by a three-digit number -- the first digit indicates the card row (numbered from top to bottom) and the last two digits indicate the card position within the row (numbered from left to right as seen from the card-receptacle side of the nest). For example: 03A1-A2-A5-234 is the reference designation for the last card in the bottom row (234) of the lower AIM nest (A5) of bay 2 (A2) of the Analog Input Subsystem (03A1).

Configuration Rules

Analog Input Units are configured according to the following rules:

1. Only one AIU per CP/IO Unit.

2. The maximum AIU cabinet size is five bays (one control bay plus up to four other bays, no more than two of which can be UTR panel bays).

3. Multiplexer bays can only be configured in the three forms shown in Figure 1-12-3. Multiplexer bays can never contain termination panels of any type.

4. Analog Input Multiplexer nests can be configured most economically by placing cards having the same signal amplification requirements in the same nest. However, it is possible to commit each row in a nest to a different data amplifier (within the limit of two amplifiers per bay). Solid-state multiplexer cards permit the fastest sampling speeds. However, relay multiplexer and solid-state multiplexer cards can be intermixed in the same row. (The programming is not affected by this intermixing because the hardware automatically takes care of all timing differences; however, it should be noted that sequential scanning should be used in intermixed nests to optimize scanning speed.) A precision reference supply card must be provided for each data amplifier implemented. This card must be placed in the lowest addressable position available after the last field input multiplexer card is implemented. It supplies precision voltage inputs of 0 volts, 9mv, 45mv, 180mv, and 900mv to normal input points. By reading these known supply voltages as normal analog input signals, the program can calculate

system error factors and produce (effectively) correction curves for all inputs passing through each multiplexer/data amplifier path.

STANDARD AND OPTIONAL FEATURES

Accuracy, design characteristics, etc. described previously are all standard features of the AIU. Standard multiplexer cards, prewired nests, and preestablished bay configurations make manufacture of each AIU highly adaptable to specific installation requirements. The number, type, and range of inputs to be received determine which predesigned configuration is used and the extent of implementation of each Analog Input Multiplexer nest. Major options available are:

a. Open Channel Detection (OCD) facilities are standard on relay multiplexer inputs of ±100 mv or less. Optional OCD facilities are available for solid-state multiplexer inputs of ±100 mv or less (on a per card basis).

b. A test panel is available as an optional addition to the control bay. This panel allows the AIU to be completely disconnected from the CP/IO Unit and provides facilities for manual exercise of all AIU logic circuits for testing and maintenance.

c. Input analog signals can be received directly by the AIU at "paddles" providing the input connection to the AIM nests, thermocouple inputs can be received locally on UTR Termination Panels in bays of the AIU for cabling to the AIM nests, or can be received remotely at Termination Units and cabled into the AIM nests. UTR Termination Panels, voltage-input termination panels, and current-input termination panels

can be provided in Termination Units for remote (stand-alone) installations.

INTERFACE CONSIDERATIONS

Cabling for the Analog Input Subsystem is of four types:

a. Interface between the computer and the AIS is provided as an integral part of the manufacture of the CP/IO Unit.

b. Interface between the AIS and the AIU is provided by one cable of 50 twisted pairs of wires between the System Interface Nest in the CP/IO Unit, wing 1, and connector J16 of the Analog Control Nest in by A3 of the AIU. Maximum cable length is 300 feet.

c. Primary power for the AIU is supplied to the ac Power Distribution Assembly in bay A3 by two cables, usually from the Power Distribution Unit. One of these cables carries auxiliary power for the fans and the other cable carries main power for the power supplies, Analog-to-Digital Converter, and Data Amplifiers.

d. Analog Input, or customer input, termination is available in two forms. One involves terminating on terminal strips in a UTR Termination Panel bay or in a separate Termination Unit. In using this method, cables are connected from the back of the multiplexer cards in the Analog Input Multiplexer Nest to the termination panels in either the UTR Termination Panel bay or Termination Unit. The second method provides higher-density termination directly within the Analog Input Unit.

The high-density termination method provides the ability to terminate customer inputs (using up to number 16 AWG wire) directly to the multiplexer plug-in cards. In this approach, it is possible to eliminate the need for bulky panels and cabinets for certain signal types. A printed-wiring board (PWB) assembly (paddle) can provide any necessary signal/circuit conditioning. At one end of the PWB is a female 32-pin connector that mates with the multiplexer card. The other end contains a 34-pin connector which is separable from the PWB and provides the interface with customer input wires.

The backplane connector mounting plate is mounted directly to the multiplexer backplane. The multiplexer card is then inserted from the other side of the nest such that the 32-pin connector portion of the multiplexer card plugs directly into the connector on the backplane connector mounting plate. The input connector block is wired directly to this backplane by means of the PWB. The customer inputs are inserted into the input connector block by pins which are crimped to the customer input wires. The female crimp contacts accept up to number 16 AWG wire. The printed wiring on the paddle provides the circuit path to connect this input connector to the backplane connector. The paddle is also used for mounting various types of signal conditioning when necessary. An effort has been made to place the signal conditioning on the multiplexer cards wherever possible, thereby eliminating the need for the paddle in some cases. The signal conditioning located directly on multiplexer cards is used for such things as open channel detection for solid-state multiplexing circuits, current-to-voltage converters for transmitter inputs, input voltage attenuators, input filters, etc. Note that for current loops, although the current-to-voltage converters are on the multiplexer cards, provisions have been made to assure that removal of the multiplexer card does not open the current loop. This is accomplished by zener diodes on the paddle.

Customer wires or Termination Unit cables are routed vertically through the cabinet wireway and horizontally into the Analog Input Multiplexer Nest. The Analog Input Multiplexer Nest has two horizontal wireways integrated into the back panel design. The wireway, which is of Polyvinylchloride material, affords a convenient method for dressing the cables and wires into the individual cards.

SPECIFICATIONS

Environmental Specifications

The Analog Input Subsystem operates satisfactorily in the following environmental conditions.

Temperature:	40 F to 120 F with a maximum time rate of ambient temperature change of 1 degree F per minute
Relative Humidity:	20% to 95% over the operating temperature range, to a maximum wetbulb temperature of 86 F.
Vibration:	As per MIL-STD-810B, dated 15 June 1967, Method 514, Figure 514-6, Curve AB. Specifically:
	-5 to 27 Hz: ±1.0g (peak), sinusoidal input
	-27 to 52 Hz: 0.036 inches double amplitude displacement, sinusoidal input

	-52 to 300 Hz: ±5.0g (peak), sinusoidal input
Altitude:	-1000 to 10,000 feet
Contaminants:	0 to 10 PPM of H_2S or SO_2

The Analog Input Subsystem is designed to operate in accordance with its performance requirements when returned to its operational environment after unpowered exposure to the following conditions, either singly or in any combination.

Temperature:	-30 F to 150 F
Relative Humidity:	0 to 95%
Altitude:	-1000 to 50,000 feet
Contaminants:	0 to 10 PPM of H_2S or SO_2

Primary Power Specifications

Two supplies of primary power are required by the AIU: a main source and an auxiliary source.

Main primary power, preferably supplied by the FOX 1 Power Distribution Unit, specifications are as follows.

Voltage:	108 to 132 v rms single phase
Current:	20 amperes

Frequency:	48 to 430 Hz (400 Hz PDU source recommended)
Harmonic Content:	4% max. with no single harmonic greater than 2%
Transients:	No voltage transients outside the limits specified above are allowed.

Auxiliary primary power specifications are as follows:

Voltage:	120 v rms ±10% single phase
Current:	20 amp (1 amp is required for AMU, balance is available through convenience outlets)
Frequency:	47 to 63 Hz

Functional Specifications

Capacity:	1 to 8 AIM nests of up to 256 inputs each for a maximum of 2048 inputs

Speed:

Realay multiplexer - random mode:	100 points/sec (minimum)
Relay multiplexer - sequential mode:	1000 points/sec (maximum)

Solid state multiplexer - random mode:	5000 points/sec (maximum)*
Solid state multiplexer - sequential mode:	5000 points/sec (maximum)*
Accuracy:	±0.10% of full scale (0.15% on 10 mv scale)
Resolution:	14-bit sign-and-magnitude representation using 2's complement notation
Temperature Coefficient:	±0.01% per degree C
Normal Mode Rejection:	57 to 64 dB at 60 Hz
Common Mode Rejection:	86 to 120 dB at 0 to 60 Hz
Scales	±10 mv (DAMP Gain = 1000) ±20 mv (DAMP Gain = 500) ±50 mv (DAMP Gain = 200) ±100 mv (DAMP Gain = 100) ±200 mv (DAMP Gain = 50) +0.5 v to -0.2 v (DAMP Gain = 20) +1.0 v to -0.2 v (DAMP Gain = 10)
Input Protection:	Up to 155 vac or vdc All solid state multiplexer inputs are fused at 0.03125 ampere

*Speed depends upon bandwidth setting of Data Amplifier.

Interface Specifications

Analog input signals interface onto the FOX 1 system at the multiplexer cards of the AIM nests. The interface characteristics of the various types of standard multiplexer cards are as follows.

Solid State Multiplexer - Current Input -

Maximum Line Length:	1000 feet
Number of Inputs/Card:	8
Current Ranges Available: (for amplifier gain of 10)	10 to 50 ma (D3001RB) 4 to 20 ma (D3001RD) 1 to 5 ma (D3001RC)
Maximum Scanning Speed:	5000 points/sec.
Maximum Common Mode Voltage:	±10 v
Common Mode Rejection: (with up to 1K source unbalance)	86 dB (dc to 60 Hz)
Normal Mode Rejection:	-50 dB at 60 Hz -47 dB at 50 Hz
Maximum Normal Mode Voltage: (within specification)	-0.2 to 1 v dc
Maximum Normal Mode Voltage: (non-catastrophic)	± 20 v

Max. Settling Time of Input Filter:	2.3 sec to within 0.2% of final value
	0.9 sec to within 10% of final value

Solid State Multiplexer - Voltage Input (D3001DK) -

Max. Line Length:	1000 feet
Full Scale Input Voltage Range: (function of amplifier gain)	±100 mv, ±20 mv, ±50 mv ±100 mv, ±200 mv -200 mv to +500 mv, and -200 mv to +1 v dc
Number of Inputs/Card:	8
Maximum Scanning Speed:	5000 points/sec
Maximum Common Mode Voltage:	±10 v
Common Mode Rejection: (with up to 1K source unbalance)	86 dB (dc to 60 Hz)
Maximum Source Resistance: (including line resistance)	1K (including up to 1K unbalance)
Normal Mode Rejection:	-50 dB at 60 Hz -47 dB at 50 Hz
Maximum Normal Mode Voltage: (within specifications)	-0.2 to +1 v dc

Maximum Normal Mode Voltage: (non-catastrophic)	±20 v
Max. Settling Time of Input Filter:	2.3 sec to within 0.2% of final value with zero source resistance
	5.4 sec to within 0.2% of final value with 1K source resistance
	0.9 sec to within 10% of final value with zero source resistance
	2.0 sec to within 10% of final value with 1K source resistance

Guarded Relay Multiplexer - Current Input -

Maximum Line Length:	1000 feet
Number of Inputs/Card:	8
Current Ranges Available: (for amplifier gain of 10)	10 to 50 ma (D3001RE) 4 to 20 ma (D3001RG) 1 to 5 ma (D3001RF)
Maximum Scanning Speed:	
Sequential Mode:	1000 points/sec
Random Mode:	100 points/sec

Common Mode Rejection: (with up to 1K source unbalance)	120 dB (dc to 60 Hz)
Maximum Common Mode Voltage:	±155 vdc or peak ac
Normal Mode Rejection:	-57 dB at 60 Hz -54 dB at 50 Hz
Maximum Normal Mode Voltage: (within specifications)	-0.2 to +1 vdc
Maximum Normal Mode Voltage: (non-catastrophic)	±20 v
Max. Settling Time of Input Filter:	2.2 sec (to 0.2% of final value) 0.9 sec (to 10% of final value)

Guarded Relay Multiplexer - Voltage Input (D3001DS) -

Maximum Line Length:	1000 feet
Full Scale Input Voltage Range: (function of amplifier gain)	±10 mv, ±20 mv, ±50 mv ±100 mv, ±200 mv -200 mv to +500 mv, and -200 mv to +1 v dc
Number of Inputs/Card:	8

Maximum Scanning Speed:	
Sequential Mode:	1000 points/sec
Random Mode:	100 points/sec
Common Mode Rejection: (with up to 1K source unbalance)	120 dB (dc to 60 Hz)
Maximum Commom Mode Voltage:	±155 vdc or peak ac
Maximum Source Resistance: (including line resistance)	1K (including up to 1K unbalance)
Normal Mode Rejection:	-57 dB at 60 Hz -54 dB at 50 Hz
Maximum Normal Mode Voltage: (within specifications)	-0.2 to +1 vdc
Maximum Normal Mode Voltage: (non-catastrophic)	±20 v
Max. Settling Time of Input Filter:	2.2 sec to within 0.2% of final value with zero source resistance
	6.6 sec to within 0.2% of final value with 1K source resistance
	0.9 sec to within 10% of final value with zero source resistance

	2.5 sec to within 10% of final value with 1K source resistance

Solid State Low Level Multiplexer (D3001DL) -

Maximum Line Length:	1000 feet
Number of Inputs/Card:	8
Full Scale Input Voltage Range: (function of amplifier gain)	±10 mv, ±20 mv, ±50 mv ±100 mv
Maximum Scanning Speed:	5000 point/sec (either mode)
Maximum Common Mode Voltage:	±10 v
Common Mode Rejection: (with up to 1K source unbalance)	120 dB (dc to 60 Hz)
Maximum Source Resistance: (including line resistance)	1K (with up to 1K unbalance)
Maximum Normal Mode Voltage: (within specifications)	±100 mv dc
Maximum Normal Mode Voltage: (non-catastrophic)	±20 v
Normal Mode Rejection:	-67 dB at 60 Hz -64 dB at 50 Hz

Max. Settling Time of Input Filter:	4.2 sec to within 0.2% of final value with zero source resistance
	8.6 sec to within 0.2% of final value with 1K source resistance
	1.7 sec to within 10% of final value with zero source resistance
	3.3 sec to within 10% of final value with 1K source resistance

Solid State Low Level Multiplexer with Open Channel Detector (D3001RA) -

Maximum Line Length:	1000 feet
Number of Inputs/Card:	8
Full Scale Input Voltage Range: (function of amplifier gain)	±10 mv, ±20 mv, ±50 mv, ±100 mv
Maximum Scanning Speed:	5000 point/sec (either mode)
Common Mode Rejection: (with up to 100 ohm source unbalance)	110 dB (dc to 60 Hz)

Maximum Common Mode Voltage:	±10 v
Maximum Normal Mode Voltage: (within specifications)	±100 mv dc
Maximum Normal Mode Voltage: (non-catastrophic)	±20 v
Maximum Source Resistance: (including line resistance)	200 ohms (with up to 200 ohms unbalance)
Normal Mode Rejection:	-67 dB at 60 Hz -64 dB at 50 Hz
Max. Settling Time of Input Filter:	4.2 sec to within 0.2% of final value with zero source resistance
	5.1 sec to within 0.2% of final value with 200 ohms source resistance
	1.7 sec to within 10% of final value with zero source resistance
	2.0 sec to within 10% of final value with 200 ohms source resistance

Max. Time Required to Detect Open T/C: 50 seconds

*Additional Error (offset) in Reading due to Open Thermocouple Detector:	100 μv offset

*This error can be decreased on an individual basis by measuring the specific offset value in the field and compensating in the operating system program.

Dynatherm RTD Multiplexer (D3001RH) -

Maximum Line Length:	1000 feet
Maximum Line Resistance: (including wire temperature coeff.)	4 ohms
Multiplexer Switching Element:	Solid state
Number of Inputs/Card:	4
Speed:	5000 points/sec
Maximum Common Mode Voltage: (RTDs are referenced to ground at card)	Not applicable
Maximum Line Unbalance:	2.5% of line resistance
Temperature Measurement Range:	-100 to +600 F
RTD Curve:	NR 226
Multiplexer Input Voltage Range:	-50 mv to +50 mv
Maximum Bulb Current:	0.9 ma

Dynatherm RTD Multiplexer with Span Adjustment (D3001RL) - Same specifications as Dynatherm RTD Multiplexer without span adjustment (D3001RH) but with ±0.5% span adjustment.

Copper RTD Multiplexer (D3001RJ) -

Maximum Line Length:	1000 feet
Maximum Line Resistance: (including wire temperature coeff.)	4 ohms
Number of Inputs/Card:	4
Speed:	5000 points/sec
Maximum Common Mode Voltage: (RTDs are referenced to ground at card)	Not applicable
Maximum Line Unbalance:	2.5% of line resistance
Temperature Measurement Range:	0 to 300 F
RTD Curve:	CR 228
Multiplexer Input Voltage Range:	-50 mv to +50 mv
Multiplexer Switching Element:	Solid state
Maximum Bulb Current:	31.2 ma

Copper RTD Multiplexer with Span Adjustment (D3001RM) - Same specifications as Copper RTD Multiplexer without span adjustment (D3001RJ) but with ±0.5% span adjustment.

Platinum RTD Multiplexer (D3001RK) -

Maximum Line Length:	1000 feet
Maximum Line Resistance:	4 ohms
Number of Inputs/Card:	4
Speed:	5000 points/sec
Maximum Common Mode Voltage: (RTDs are referenced to ground at card)	Not applicable
Maximum Line Unbalance:	2.5% of line resistance
Temperature Measurement Range:	-200 C to 600 C
RTD Curve:	PT 100
Multiplexer Input Voltage Range:	-50 mv to +50 mv
Multiplexer Switching Element:	Solid state
Maximum Bulb Current:	2.6 ma

Platinum RTD Multiple with Span Adjustment (D3001RN) - Same specifications as Platinum RTD Multiplexer without span adjustment (D3001RK) but with ±0.5% span adjustment.

	8.75 inches vertical panel space.)
Flexibility:	Accepts all thermocouple type wire.

SECTION 13
DIGITAL IO UNIT

The Digital IO Unit furnishes a two-way communication path between the FOX 1 computer and the process. It carries information from digital measurement devices and status recognition elements (contacts) in the plant process instrumentation to the central processor. It routes the digital result of control algorithm computations from the processor to a digital process device, or converts the digital output to an analog signal appropriate for trend recorders or valve controllers.

The Digital IO Unit supplies up to 32 pulse counter inputs, up to 512 valve control outputs, up to 32 trend recorder outputs, and a combined total up to 6,144 contact inputs and dc outputs. Standard FOX 1 control software is capable of handling the maximum digital hardware configuration.

FUNCTIONAL DESCRIPTION

Components of the Digital IO subsystem, shown in Figure 1-13-1, include a programmed IO (PIO) interface and device synchronizing logic nest in the CP/IO Unit, and up to ten multiplexer nests in the first digital IO cabinet. The digital input/output devices and the valve control outputs require separate synchronizers, but share system interface nest logic that decodes PIO bus signals. In the Digital IO Unit cabinet, separate sections of the digital control nest steer signals to digital IO, pulse counter input, or analog output multiplexer nests; or to valve control output multiplexer nests. The subsystem can include up to four cabinets, as in Figure 1-13-2, with the multiplexers in each cabinet driven by a separate digital control nest.

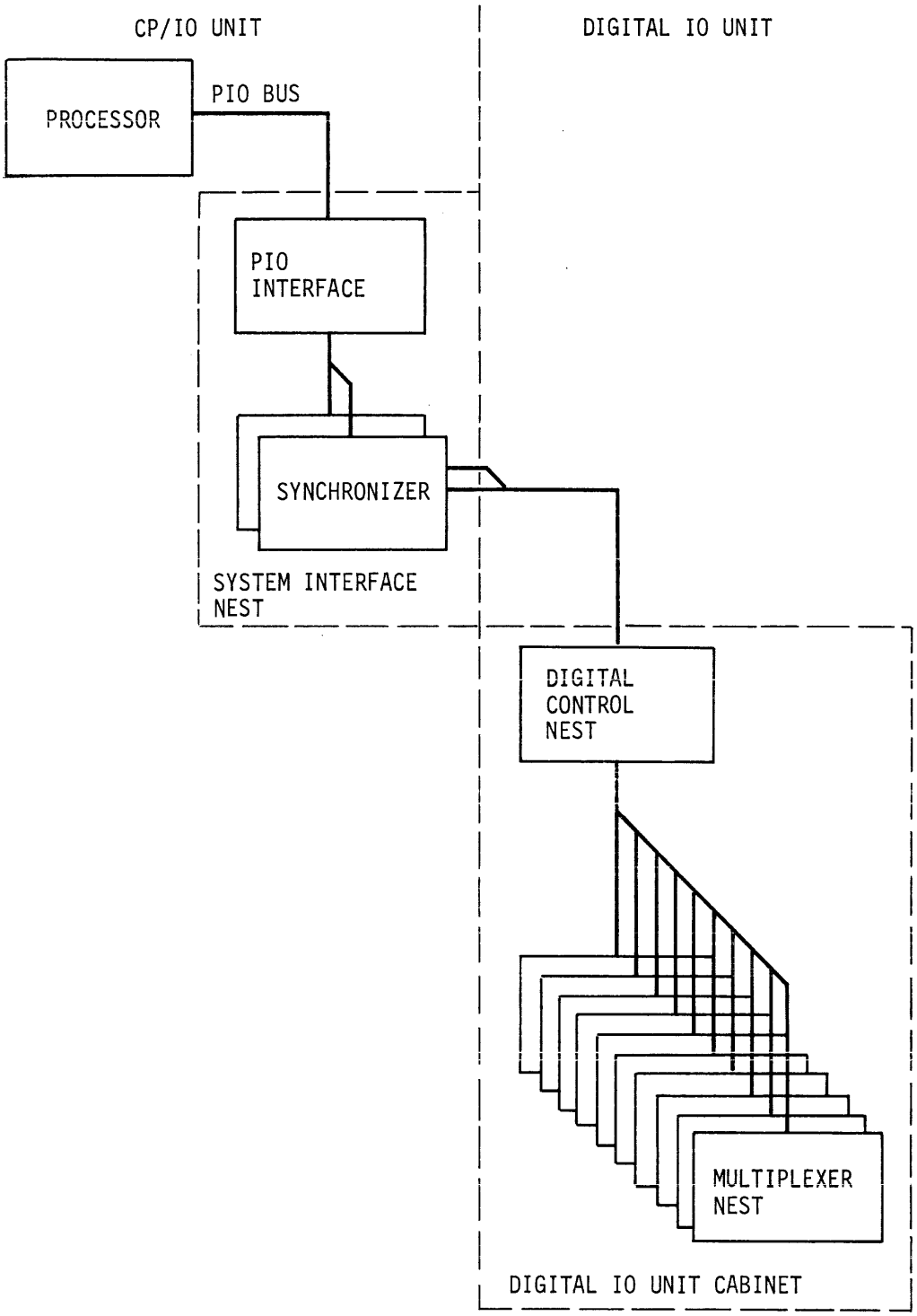


Figure 1-13-1. Digital IO Subsystem Components

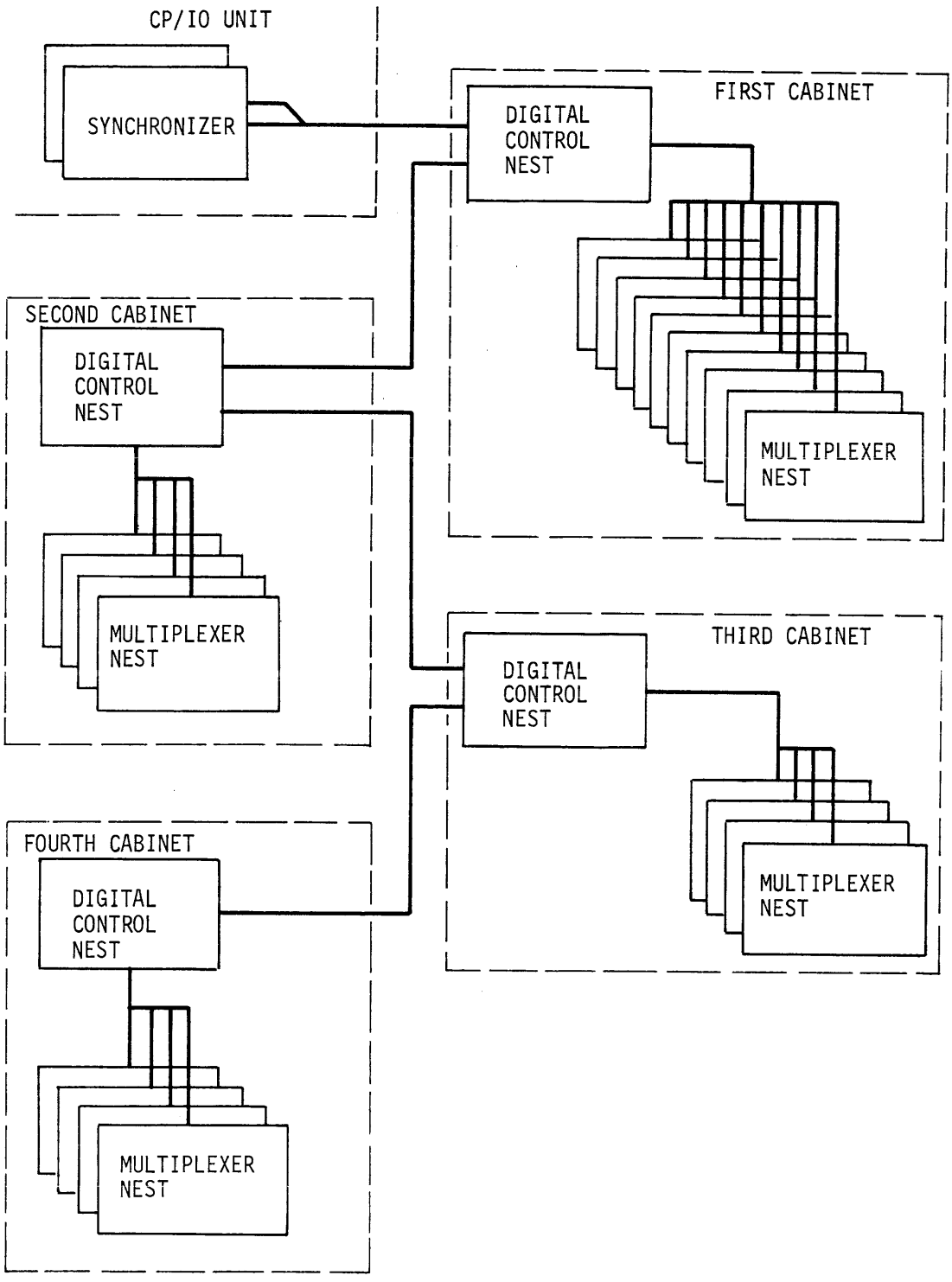


Figure 1-13-2. Digital IO Subsystem

Digital IO Multiplexer Nests

The digital IO multiplexer nests are organized into groups of one, two, or three printed circuit cards that transfer data between the central processor and the process in bytes of 8-, 16-, or 24-bits. The entire three-row nest can be assigned in a single function, input or output, as shown in section A of Figure 1-13-3, or the nest can be split into one function for the top row, and another for the lower two rows, as in section B of the same figure. The split nest is less efficient for scanning, since fewer bits are transferred at one time. However, it is useful for the last nest in the subsystem, when not enough signals remain to justify separate additional nests for inputs and outputs. Partially implemented nests, split and whole, are shown in section C of Figure 1-13-3.

Each implemented row of the digital IO multiplexer nest contains one or two control cards (depending upon the type of multiplexed signal) and one to sixteen multiplexer cards, as in section D of Figure 1-13-3. Each digital multiplexer card provides eight inputs or eight outputs. The hierarchy of card, group, nest, and cabinet accommodates up to 6,144 digital input/output signals.

The variety of multiplexer cards usable in the digital IO nest provides the system with the following types of inputs and outputs:

a. Contact input
b. Process interrupt input
c. DC output

    (1) Steady-state
    (2) Momentary
    (3) Relay driver

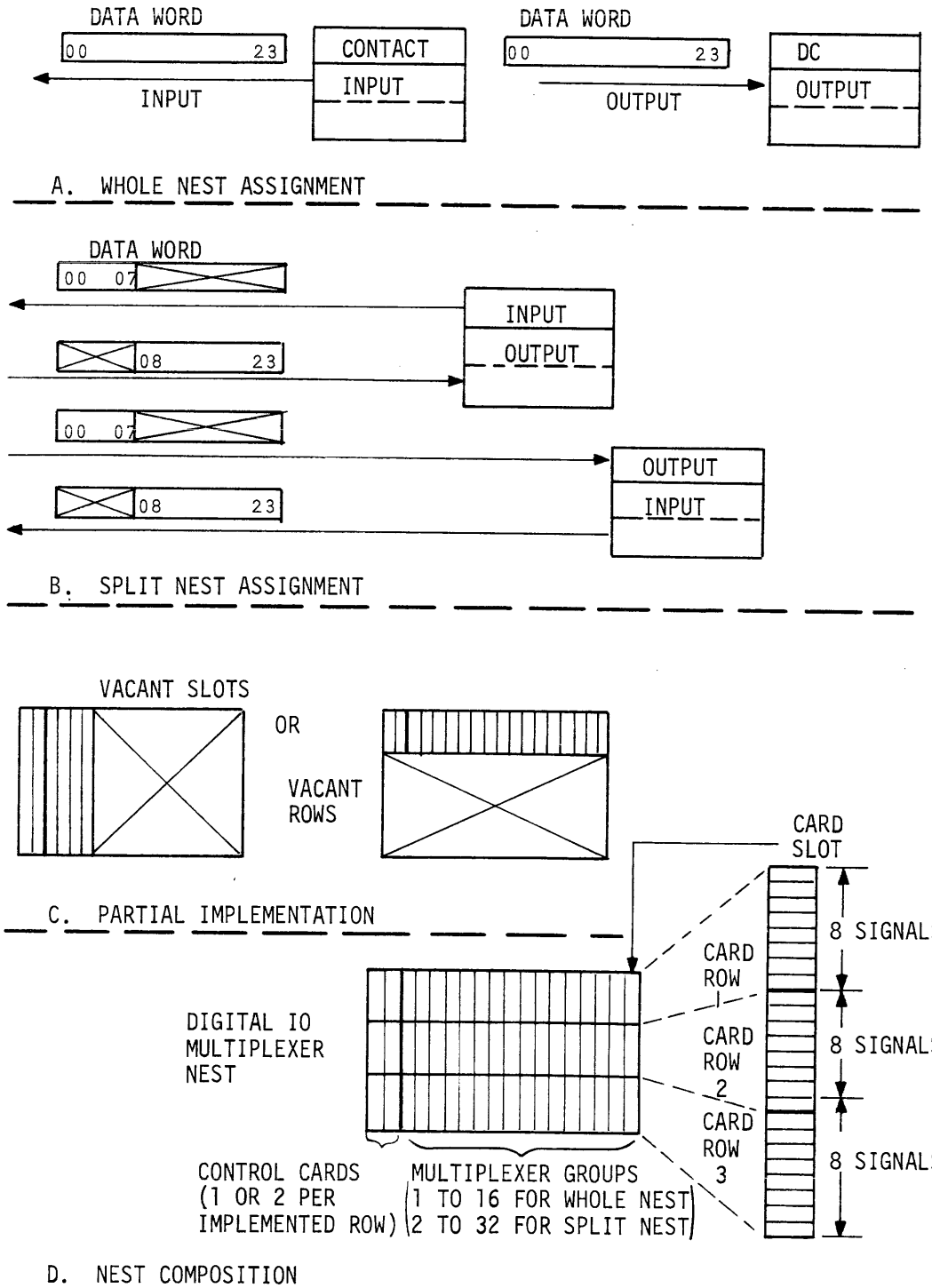


Figure 1-13-3. Nest Implementation - Digital IO Multiplexer

Contact Inputs - The simplest type of digital input is contact closure sensing. Voltage supplied by FOX 1 equipment is returned to the digital input through a contact in the process instrumentation. This arrangement requires a pair of cable wires (supply and return) for each contact input. The method of connecting contact inputs is illustrated in Figure 1-13-4. A closed circuit current of eight milli mperes aids in keeping the contacts clean.

Contact inputs can be read into core at regular intervals determined by the control software (using the real time clock) or at the request of a user program. The requesting program may determine the current state of a single contact, or compare 24 contacts, read as a single word of data, with a 24-bit word from a table in memory representing the desired status for those contacts.

Typical contact inputs, limit switches or relays, provide the following kinds of information to the FOX 1 system:

a. Controller station status -- indicates whether the controller is in DDC or backup mode.

b. On-off valve position -- indicates when the valve is fully open or fully closed.

c. Pump and motor on-off status -- ammeter or tachometer triggered.

d. Capacitance probe condition -- wet or dry, indicates presence of liquid at extreme points in a vessel.

e. Measurement readout -- digital devices transmit readings (using several contacts) from the following sources:

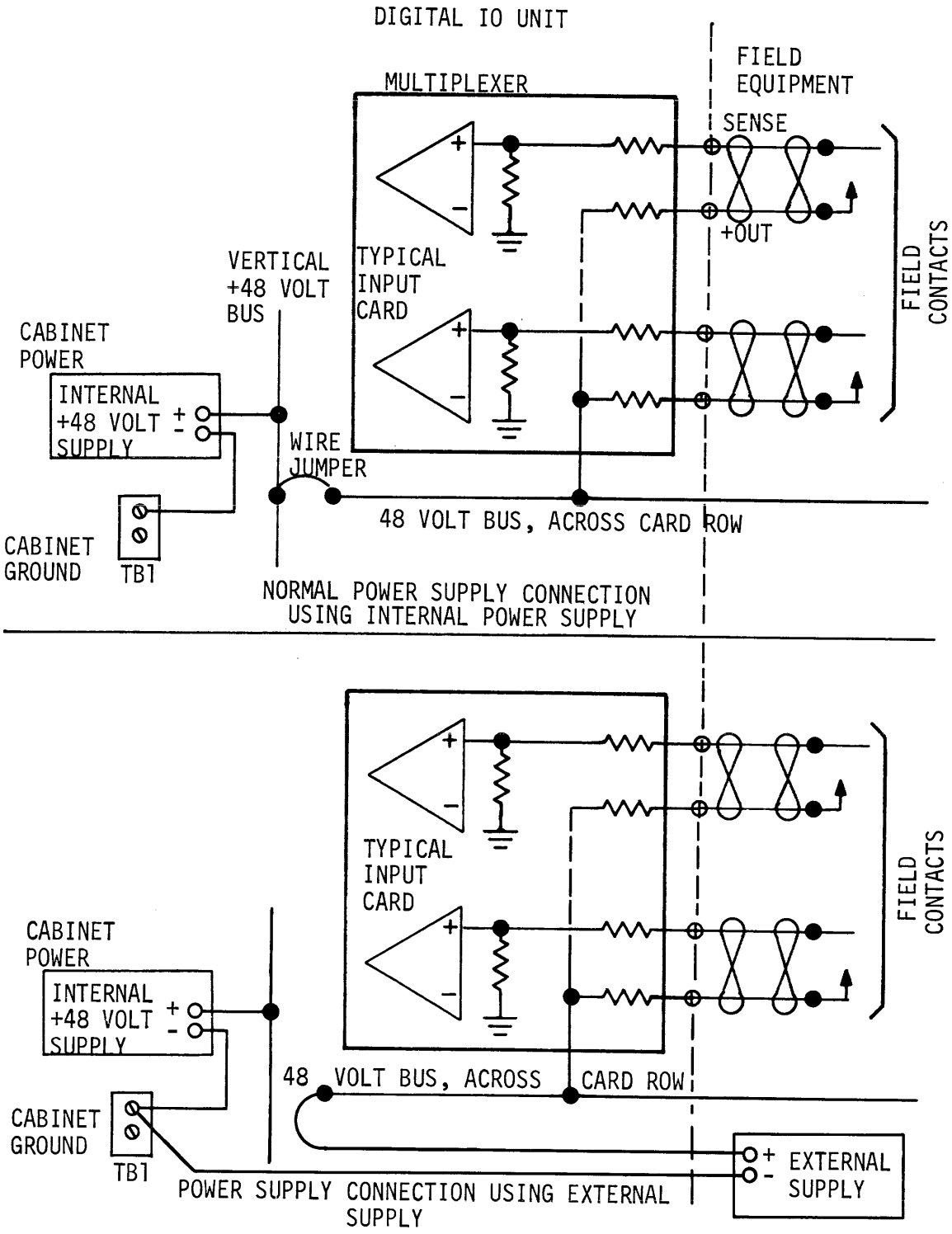


Figure 1-13-4. Contact Input, Power Supply Connections

(1) Level gauges
(2) Strain gauges and weight cells
(3) Instantaneous tachometer readings

Process Interrupt Input - The process interrupt input is identical with a contact input, except for the addition of an OR circuit to provide a signal -- the program interrupt request -- when any one of the 8, 16, or 24 contacts in the group closes. Unlike the passive contact input, which must be scanned periodically by the control software, the process interrupt demands service.

The process interrupt handles inputs that are beyond the limits of the basic one second contact scan interval, providing fast response for critical devices, and minimizing processor time required for inputs that change infrequently. For devices requiring fast response, the process interrupt can provide service within approximately two milliseconds. For an input that changes infrequently, for example, only once in several hours, the process interrupt demands computer time only when a change occurs.

The FOX 1 system interface accepts up to 384 process interrupt inputs. This total is divided among 16 groups, each of which may have 8, 16, or 24 inputs. Since the sixteen possible groups are assigned within eight interrupt levels, most of these levels serve two or more process interrupt groups. The four steps in servicing a process interrupt are diagrammed in Figure 1-13-5. A bit identifying the interrupt group is stored in one of the multiplexer control cards until the level has been interrogated by a command from the central processor. The bit (or bits) returned in response to the command indicates which group requested interrupt. A command directed to that group transfers 24 bits indicating which contact (or contacts) within the group initiated the request.

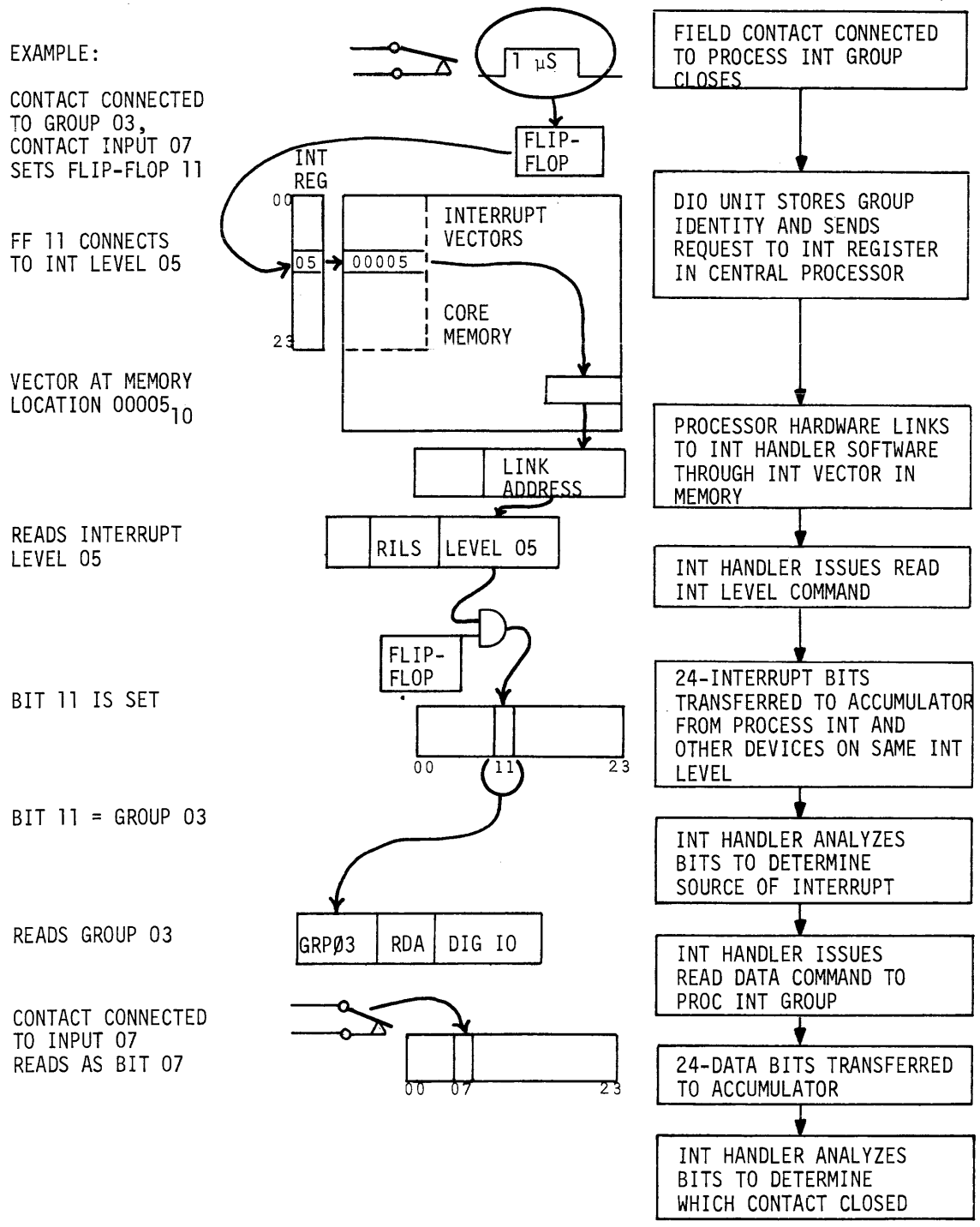


Figure 1-13-5. Process Interrupt Sequence

Process interrupt inputs are used to:

a. Indicate that an instrument requiring fast response is ready to be read.

b. Indicate an alarm condition when a pressure switch contact closes at pressure threshold.

DC Outputs - The solid state dc output printed circuit card consists of an 8-bit storage register and eight single-ended output driver circuits. DC outputs may be subdivided into the following:

a. Steady state -- Each solid state card in an output group stores 8-bits from the central processor and provides continuous outputs corresponding to the logical state of the individual bits. Whenever a change in one or more of the bits in an output group (one, two, or three cards) is desired, the central processor transfers a 24-bit data word to the group. Each card in the group stores in its 8-bit register its portion of the information, which is reflected immediately in the eight driver outputs. The output then remains at the new binary value until the central processor transmits another change instruction.

b. Relay Driver -- The relay driver card output is really an intermediate output. Each relay driver card is connected by a separate cable to a relay card containing eight relays which provide the output to the process. The relay driver cards have eight pairs of complementary outputs; each output of a driver pair connects to one of the two coils in a latching relay. When nonlatching relays are used, one output in each pair goes unused.

c. Momentary -- A 16.5 millisecond gate enables the momentary output driver circuits. Each time the central processor transmits data to it, the momentary output card stores the eight bits, then transmits a 16.5 millisecond pulse on each output line associated with a logical one state in the bit storage register.

Relay Output Nests

Relay driver cards in a dc output nest connect to relay cards in a relay output nest. Two types of relay outputs are available: nonlatching, and latching. Latching relays employ two coils, and retain their setting when power is removed. Nonlatching relays use one coil, and revert to their deenergized position upon loss of power. Both types use mercury-wetted contacts that may be wired as either normally open or normally closed points. Eight relays, each having one set of contacts, are mounted on an 8 x 8 inch pluggable card. Each relay output card is driven by a digital output relay driver card. Up to 3,072 relay outputs may be housed in the Digital IO Unit cabinets; additional relay outputs may be housed in optional relay Termination Unit cabinets.

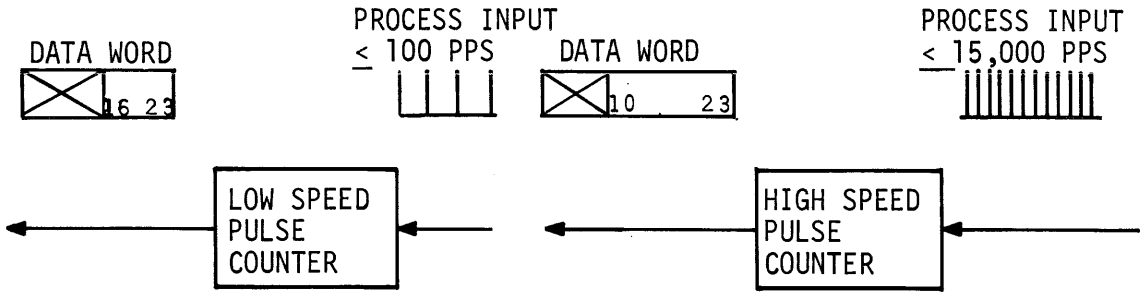
Relay outputs are required in the following situations:

a. The voltage or current requirements exceed the limits of 60 VDC and 0.5 amperes provided by solid state outputs.

b. AC must be controlled.

c. The circuit must remain closed, or the status of the output must be retained in the event of a power failure. A magnetic latching relay fulfills either requirement.

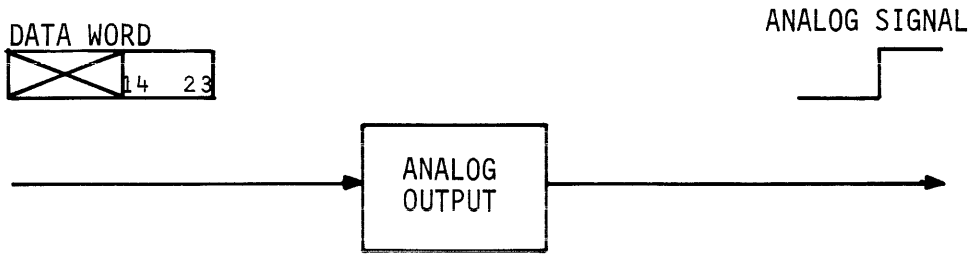
Pulse Counter Input



Pulse inputs are generated at a rate proportional to the movement rate of the measuring device, such as turbine meter, tachometer, or watt-hour meter. The pulse repetition rate may vary from less than 10 Hz up to 15 kHz for different devices and services. Pulses are counted and the sum accumulated in a register which is read by the computer at regular one-second intervals under program control. For each pulse input there is one counter and associated register. Up to 32 pulse counter inputs can be implemented in the FOX 1 process IO system.

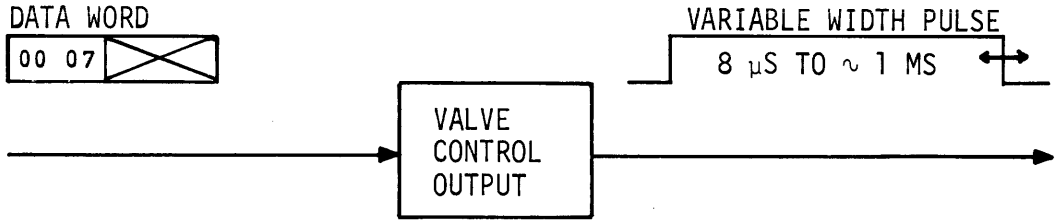
Two standard pulse counters are available. One fills an eight-bit register and is suitable for rates up to 100 pps. The other has a 14-bit register for up to 15,000 pps. Both the pulse rate and the total are important, since the counter accumulates pulses over a period of approximately one second. The value in the counter at each sampling interval is converted to engineering units by software.

Analog Output



A single analog output element, occupying one-half of a printed circuit card, converts 10-bits of binary data received from the central processor to one output current or voltage signal in one of three ranges: 10 to 50 milliamperes, 4 to 20 milliamperes, or 2 to 10 volts. The FOX 1 can handle up to 32 analog outputs. Each analog output element consists of a 10-bit storage register and a digital-to-analog converter. Whenever a change in one of the outputs is desired, the central processor transfers a 10-bit binary value representing the new output value to the selected analog element, which stores the information in its 10-bit register. The stored information is converted to a continuous output signal proportional to the binary value of the input. The output then remains at the same level until the central processor transmits another change instruction.

Valve Control Output



The valve control output converts eight bits of digital information into a constant-amplitude, variable-width pulse intended for Foxboro 62 and 67 series controllers. The valve control branch produces only one output signal change at a time, a constant amplitude pulse with a duration equal to a binary value multiplied by eight microseconds. Pulse widths range from 8 microseconds to 1.024 milliseconds. The central processor transfers binary data to the valve control logic in the digital control nest; then it is released to continue with other instructions while the valve control logic generates a pulse. Two separate outputs provide

control of direction, increase or decrease. Valve movement produced is in direct proportion to the width of the pulse applied to the valve controller. Between outputs from the computer, the controller maintains the valve in the last position attained.

The control program determines the amount of valve movement required, and selects the corresponding pulse width. The choices available permit valve changes from 0.1 percent to 12.7 percent (of full-scale) increase, or up to 12.8 percent decrease, in increments of 0.1 percent. Greater changes must be accomplished in steps such that the entire change is made as quickly as possible.

PIO Bus Communications

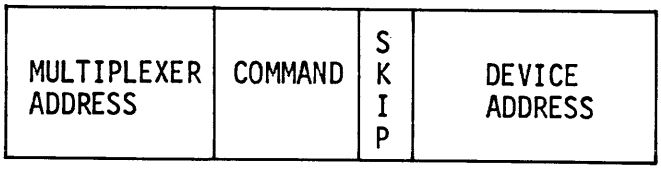
The Digital IO Unit and the central processor communicate through the programmed IO bus (PIO). The processor initiates PIO bus activity by executing a PIO instruction. The PIO instruction accesses a 24-bit memory operand in the format shown in Table 1-13-1 and 1-13-2, which explain address and command fields, respectively.

Data are transferred over the PIO bus to and from the B register in the central processor. Incoming (to the processor) data are transferred under PIO hardware control from the B register to the A register (accumulator) where the information is available to the requesting program. Outgoing data are loaded into the A register prior to the PIO command and transferred from the A register to the B register under PIO hardware control. The sequence of events for all digital IO operations is summarized in Figure 1-13-6.

Command Sequence - PIO bus communication is on an asychronous basis, using a command-response exchange to correlate processor and device

Table 1-13-1. Digital IO Subsystem Addressing

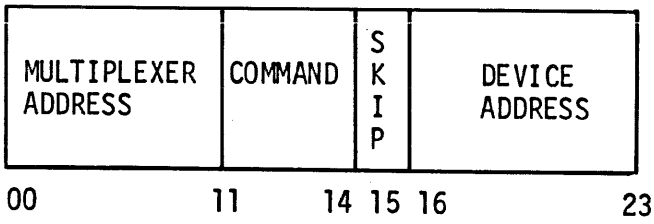
PIO OPERAND



ADDRESS FIELD	ADDRESSED LOGIC	FUNCTION
DEVICE ADDRESS (16–23)	Digital IO Critical	1. Read and reset process interrupt or pulse counter inputs. 2. Write digital or analog outputs.
	Digital IO Noncritical	Read only.
	Valve Control	All operations.
DITIAL IO MULTIPLEXER ADDRESS (00–09)	Digital IO	1. Select one of 512 digital IO groups. 2. Select one of 32 pulse counter inputs. 3. Select one of 32 analog outputs.
VALVE CTRL MULTIPLEXER ADDRESS (00–08) PARITY (10)	Valve Control	Select one of 512 valve control outputs.
INTERRUPT LEVEL (16–23)	All on addressed level	Device synchronizer responds with its assigned interrupt bit.

Table 1-13-2. Digital IO Subsystem Commands

PIO COMMAND



COMMAND	FUNCTION
Read Data	1. Transfers a single word (24-bits) over the PIO bus from the device synchronizer to the central processor accumulator. 2. A read data command using the critical device address acts as a read and reset for process interrupt or pulse counter inputs.
Write Data	Transfers a single word (24-bits) over the PIO bus from the central processor accumulator to the device synchronizer.
Read Status	Transfers a single word (up to 24-bits) representing conditions in the device or its synchronizer to the central processor accumulator, using the PIO bus.
Read Status and Clear	Transfers the status word to the accumulator, then clears the status register in the device synchronizer.
Write Status	1. If bit 23 in the accumulator is reset, the status register bits are set equal to corresponding bits in the accumulator. 2. If bit 23 in the accumulator is set, a master clear signal is generated to reset the device synchronizer control and status logic.
Read Interrupt Level Status	All device synchronizers assigned to the addressed interrupt level respond with their respective interrupt bits.

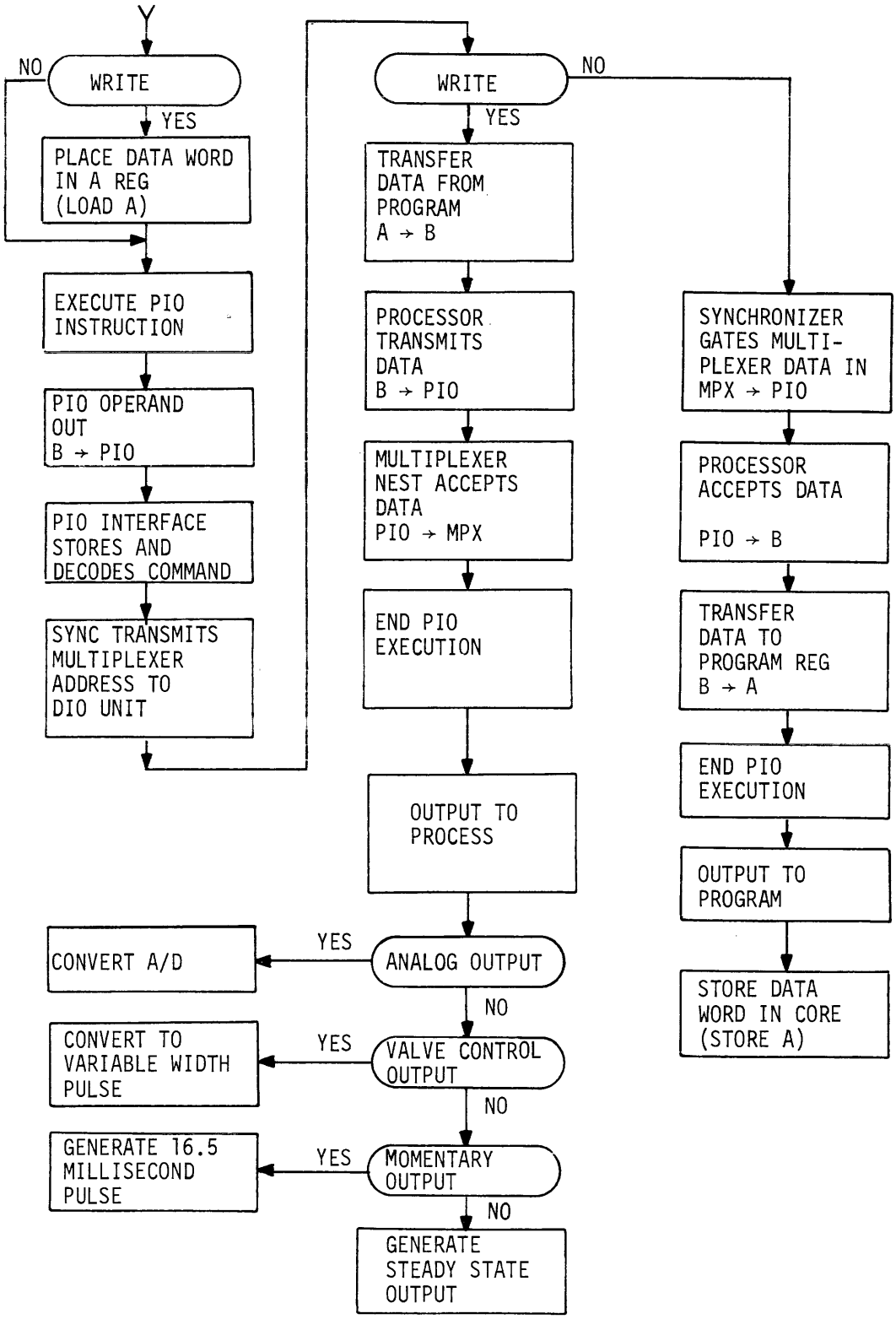


Figure 1-13-6. Digital IO Sequence

signals. The central processor transmits a command (the operand of the PIO instruction) addressing the digital or the valve control synchronizer, then waits for a response from the selected synchronizer to indicate that it has received the command.

Data Transfer Sequence - All instructions that transfer data require two exchange sequences -- command-response, and data transfer-response. The central processor follows up the command (when acknowledged) with a request to transfer data. The Digital IO Unit either places data on the PIO lines, or takes data from the lines, as directed in the request, then sends a response signal to the central processor. A complete PIO data transfer sequence takes approximately six microseconds.

Intercabinet Interface

All control and data signals are passed from the central processor to the first cabinet, from cabinet to cabinet, and distributed within the cabinet through digital control nest driver and receiver circuits, as shown in Figure 1-13-7. Signals between units are carried over twisted pairs connecting differential drivers and receivers. Two cables, each containing 48 twisted pairs, carry lines coming into the cabinet, and two similar cables carry the lines leaving the cabinet. Data from the central processor uses 24 pairs, data to the central processor, another 24 pairs; control and response signals make use of most of the remaining lines.

Intracabinet Interface

Within the cabinet, signals are carried over flat, controlled impedance cables. Using one conductor per signal, 40-conductor cables distribute signals from the control nest to multiplexer nests. Cables carrying data bits within the cabinet are bidirectional.

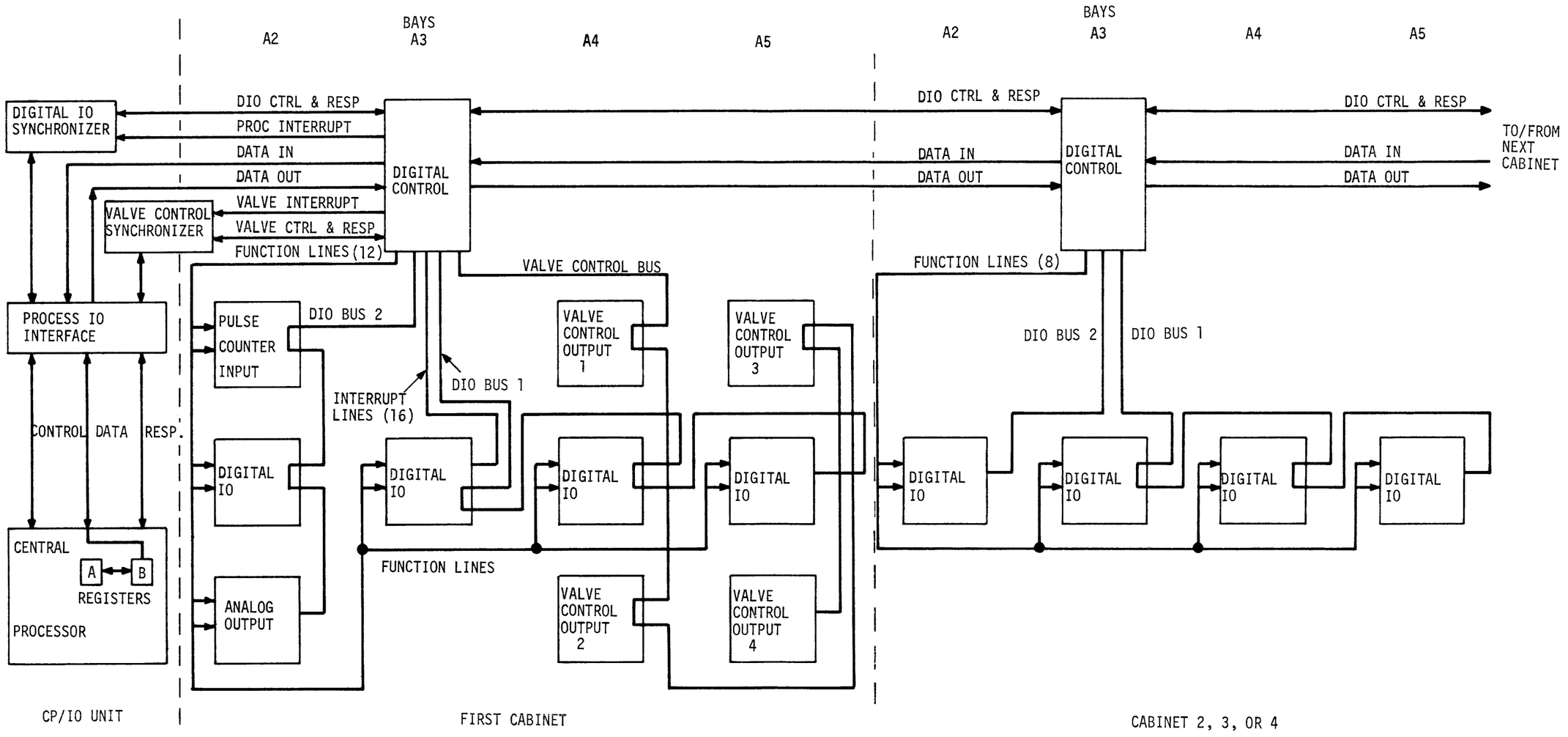


Figure 1-13-7. Digital IO Unit Cabinet and Nest Interconnection Diagram

Implementation

The FOX 1 Digital IO Unit offers a wide variety of input and output signal types and capacities, which are summarized in Table 1-13-3. Functional packaging permits the customer to select a configuration that closely matches his control requirements. The system may be expanded at any time by either of two methods -- adding multiplexer cards in nests that are not initially filled to capacity, or adding prewired nests, to which cards may be added as required.

Wiring from the process instrumentation may be connected directly to the multiplexer card receptacles in the Digital IO Unit, or terminated remotely in an optional Termination Unit.

Table 1-13-3. Summary of Digital Inputs and Outputs

INPUT TYPE	MAXIMUM NUMBER PER SYSTEM	OUTPUT TYPE	MAXIMUM NUMBER PER SYSTEM
Contact	*	DC Output	*
Process Interrupt	384	Solid State	
Pulse Counter	32	Relay	
		Momentary	*
		Valve Control	512
		Analog	32

*The combined total for contact and interrupt inputs, and steady state and momentary outputs is 6,144.

System Security Measures

A comprehensive system of hardware and software checking ensures detection of failures, and a smooth, automatic transition to analog (or manual) backup control in emergency situations. Built-in system security

logic and standard process control software detect the following types of problems:

a. Computer hardware failure
b. Computer software failure
c. Main power failure
d. IO interface failure
e. Software IO error
f. Address parity error (valve control)
g. Address/data transmission error (valve control diagnostic read)
h. Hardware integrity (driver/receiver card and cable interlock)

System Flunk - Process controllers are kept in the direct digital control (DDC) mode by a normally-energized flunk relay that is part of the process instrumentation. A system flunk line from the FOX 1 completes the electrical path to hold the flunk relay energized. Computer hardware or software failures interrupt the system flunk line to deenergize the flunk relay, placing the controllers in backup mode.

Hardware Interrupt - The other failures listed generate program interrupt requests, permitting software to determine what action should be taken. The interrupt handling software can issue a command to interrupt the system flunk line, returning the controllers to backup mode.

System Failure Detection

Computer Hardware Failure - Computer hardware performance is checked by on-line diagnostic programs that are run at one second intervals. A "fail-safe" approach requires sending a security check OK signal to the

system security logic when the proper results are obtained. Failure to get this SCOK indication automatically transfers process control to the backup mode by interrupting the system flunk line.

Computer Software Failure - Software delays or program loops are detected by stall alarm (SA) timing logic that must be reset every 1.2 seconds by issuing a write data instruction to the system security logic. As with the hardware security check, failure to reset the stall alarm interrupts the system flunk line, transferring process control to backup operation.

Main Power Failure - System power failure is detected by monitoring the output of critical dc power supplies in the CP/IO Unit. Imminent failure is detected while at least one millisecond of good operation remains (power supplies maintain usable output for at least two milliseconds after loss of input). A power failure interrupt (highest priority) enables the operating system to preserve status information and provide for an orderly shutdown. A pneumatic power fail timer relay (agastat) monitors the duration of the outage. If the duration of the outage exceeds a preset (by adjustment of the agastat) value, the system will restart with the process control in backup mode.

IO Interface Failure - All IO exchange sequences -- both command and data transfers -- are timed for a maximum of approximately 12 microseconds. When, for any reason, the central processor does not receive a response within that interval, the IO operation is aborted and an interrupt requested. An IO timer violation results when a command is issued to a nonexistent (unimplemented) address, or power is off in the selected DIO Unit cabinet.

Software IO Error - Process control IO manipulation is limited to programs assigned the proper privilege. A special DIO "critical device address" must be used to change outputs or to reset inputs. An attempt by an unauthorized program to use process IO produces an IO usage violation, which results in a program interrupt.

Address Parity Error - Special effort is made to ensure that the proper valve control multiplexer is selected before a command is executed. The multiplexer address from the central processor includes a software-generated parity bit. Hardware parity checking circuits in the addressed valve control multiplexer nest develop a parity bit from the address as it is received in the nest. The hardware developed parity bit is returned to the process interface logic in the CP/IO Unit where it is checked against the original parity bit before the command is executed. If an address parity error is detected, the command is rejected. Since the data are transferred over the same lines as the address, correct address parity is a good indication that the transmission of data over these lines will be satisfactory also.

Address/Data Transmission Error - An even more thorough check of valve control multiplexer addressing and data transmission can be accomplished by executing a series of diagnostic read instructions. The first and last multiplexer address in each implemented nest generates a predetermined data word in response to a read data command. The first eight bits of the 24-bit computer word are used to send data to the valve control multiplexer. Each of the eight diagnostic words consists of a different one of these bits set to a logical one, and the other seven bits to a logical zero. By reading from all eight addresses (on a maximum configuration) in turn, all valve data bit lines are checked in both the one and zero logic states.

Hardware Integrity - An interlock line runs through all cables and driver/receiver cards connecting the CP/IO Unit and the DIO Unit. Removing any card or disconnecting any cable that is part of this interface disables all DIO and valve control paths in both directions. In this way, erroneous signals are prevented from reaching the process controllers.

Digital IO Unit Test Panel

A Digital IO Unit Test Panel, available as a standard option, permits off-line operation. A key-lock switch turned to OFF-LINE isolates the DIO Unit from the central processor. Switching the panel LOGIC ON and pressing the panel START button prepares it for use. This panel simulates the following operations:

a. Reading digital IO inputs
b. Writing digital IO outputs
c. Reading Digital IO Unit interrupt status
d. Writing valve control outputs
e. Reading valve control diagnostic inputs

PHYSICAL DESCRIPTION

The entire digital IO subsystem comprises a digital and a valve control synchronizer and common interface circuitry in central processor wing A1, and from one to four free-standing units, or cabinets. There are five basic levels of physical modularity used in the Digital IO Unit:

a. Cabinet
b. Bay
c. Multiplexer nest

d. Function
e. Multiplexer card

Cabinet

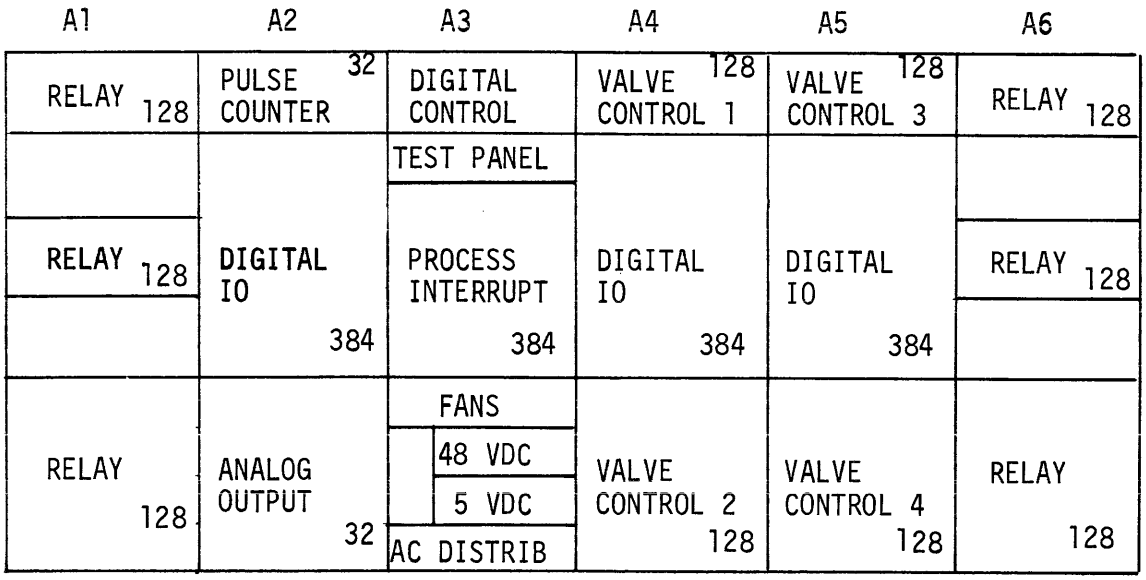
Depending upon the number of options implemented, the Digital IO Unit occupies from one to four equipment cabinets. The size and number of cabinets is chosen as best to house a particular process control configuration in the smallest space practicable. The cabinets are drip-proof units with full-length, hinged doors for access to the front and rear of each section or bay. Locks prevent unauthorized access.

Bay

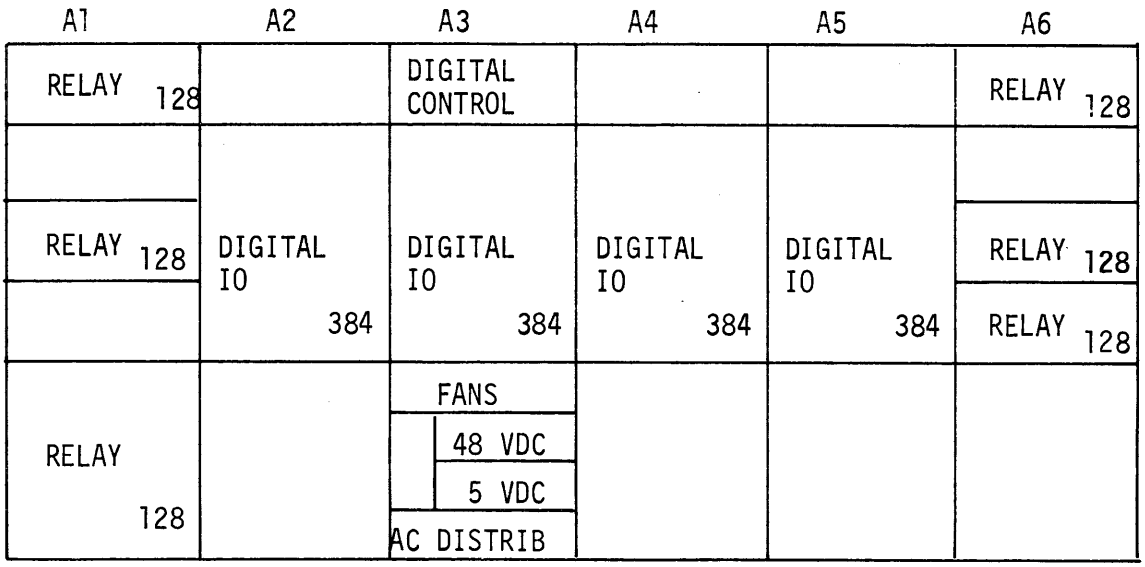
From two to six 24-inch equipment racks, or bays, each with a 6-inch wireway are joined to make up a cabinet. Control and multiplexer nests mount directly in the 24-inch racks. Relay nests and dc power supplies require an adapter for 19-inch panel mounts. There are three types of bays -- control, IO, and relay bay.

Control Bay - Cabinets are built up, as shown in Figure 1-13-8, in modular fashion around the control bay, which is present in any size cabinet. The control bay always includes the following basic elements:

a. An ac distribution panel
b. Two dc power supplies
c. A cooling fan assembly
d. A digital control nest
e. A 3-row digital IO multiplexer nest



MAXIMUM FIRST CABINET



MAXIMUM CABINET 2, 3, OR 4

Figure 1-13-8. DIO Unit Cabinet Space Assignment

AC Distribution Panel - The ac distribution panel requires two separate inputs. Auxiliary power, 50/60 Hz, is needed for the fans and convenience outlets. Main power, normally 400 Hz from the PDU (or equivalent high grade source of 50 or 60 Hz), is distributed to the 5 vdc and 48 vdc cabinet power supplies, and to nest power supplies in the analog output (one) and valve control output (up to four) nests from eight twist-lock connectors (one is a spare) at the rear of the panel. The auxiliary and main ac inputs are each protected by circuit breakers. If a PDU is not part of the system, the source for the main input should meet the same requirements listed for "standby power" in Section 3, PDU Specifications. The dc power supplies require a 19-inch-wide relay rack mount.

DC Supplies and Distribution - The 5-VDC supply provides all power for the logic circuits except the special voltages needed for analog outputs and valve control outputs. The input is protected by a circuit breaker, and the output has crowbar over-voltage protection, and automatic current limiting. Two panel meters monitor output voltage and current.

The 48-VDC supply provides the internal power used by the contact sensing digital input circuits. The input to the supply is protected by a circuit breaker, and the output by a 25 ampere fuse. Two panel meters monitor output voltage and current.

Cabinet dc (+5 and +48V) is distributed, as shown in Figure 1-13-9, over horizontal and vertical buses made of four flat, laminated conductors, each separated by a thin insulator. Filtering of the 5-volt line is improved by sandwiching its conductor between the 48-volt and 5-volt returns for added capacitance. Individual supplies (-13V, ±15V) contained in the analog output nest and each valve control output nest are also shown in the figure.

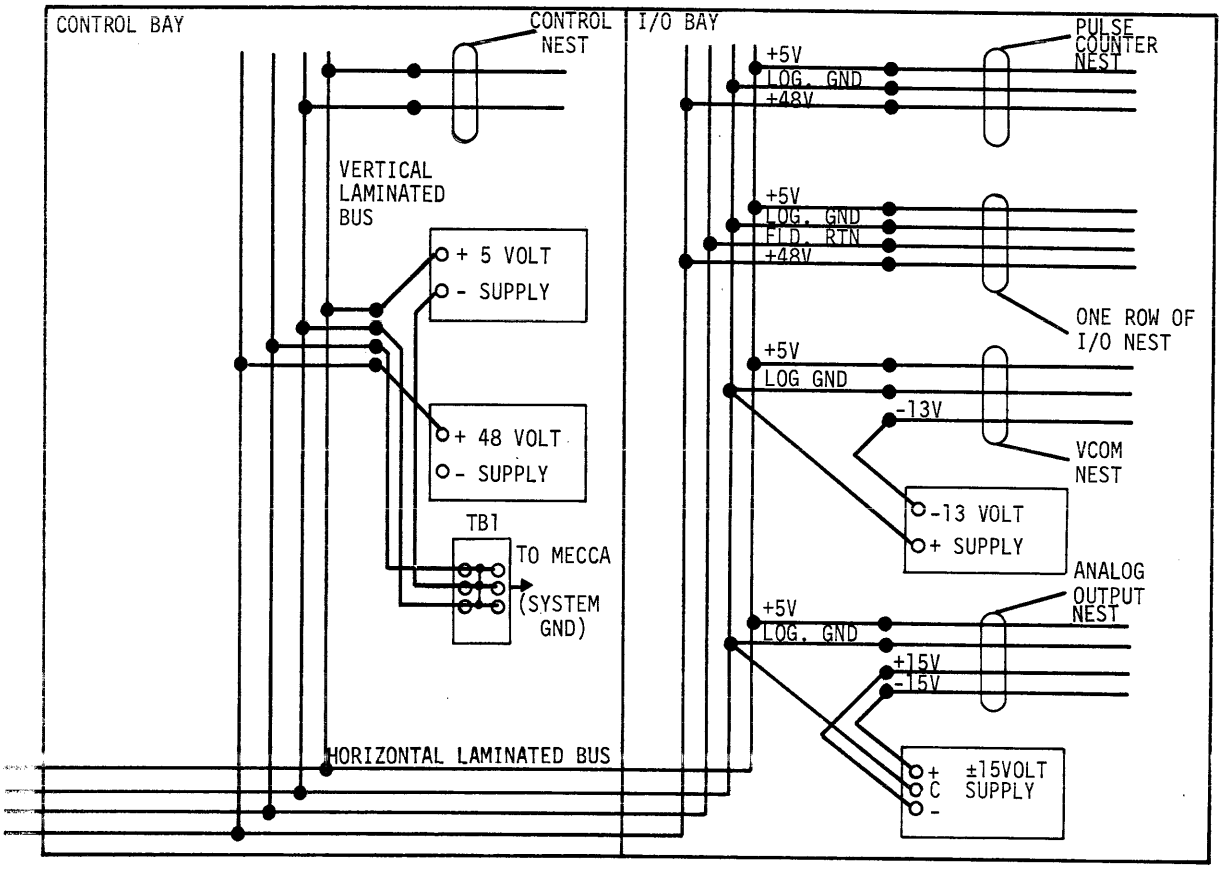


Figure 1-13-9. Cabinet DC Power Distribution

Cabinet Cooling - Six small muffin fans blow air downward over the power supplies. These fans circulate the air within the cabinet, increasing the velocity and turbulence of the air flowing past the power supplies to increase heat transfer and to prevent the formation of hot spots.

A thermal switch on the fan assembly operates a cabinet over-temperature alarm light located at the top right front of the control bay in each cabinet. The alarm is repeated by similar indicators at the CP/IO Unit

and each console. This thermal switch is set to operate at a temperature of 130 ± 3 degrees Fahrenheit, which corresponds with ambient temperatures of 110 to 120 degrees Fahrenheit.

Digital Control Nest - Each Digital IO Unit cabinet has one digital control nest. The nest, shown in Figure 1-13-10, consists of a single row of 34 card slots (one-half inch spacing), four 104-pin cable connectors and six 40-pin connectors, four terminal blocks, a CABINET MASTER CLEAR switch, and an ON LINE/OFF LINE switch. Each card slot contains an 80-pin NAFI connector. The printed circuit cards, measuring 6 x 8 inches, use medium scale integration circuit modules.

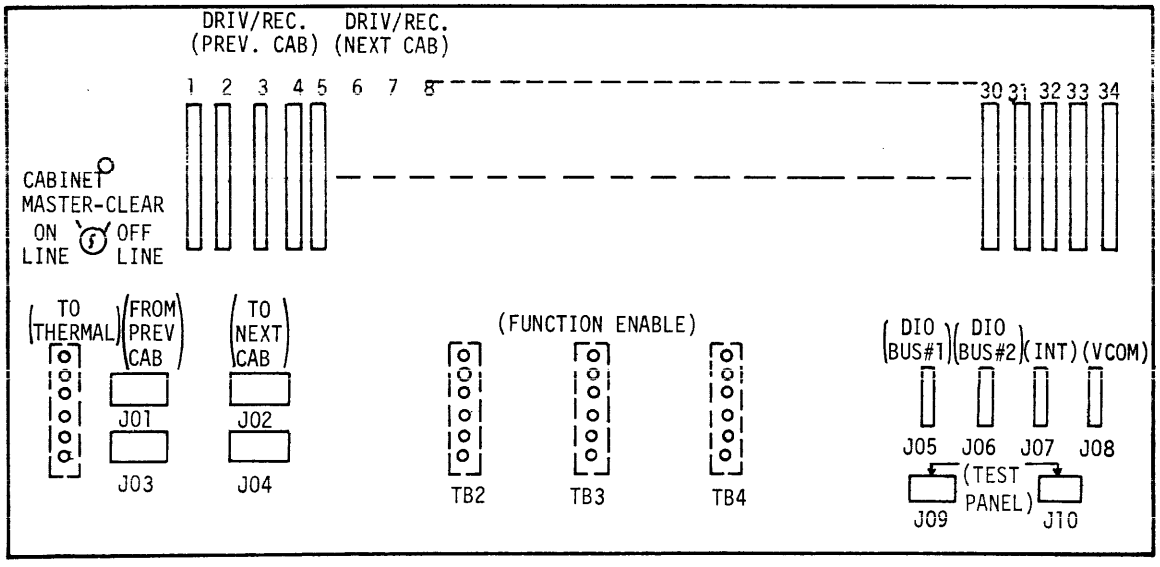


Figure 1-13-10. Digital Control Nest, Front (Card Side) View

Two 104-pin cable connectors in the digital control nest handle the 24 (twisted pair) incoming data bits plus control signals, and 24 outgoing data bits, interrupt request levels, and response lines. In the first cabinet, these cables connect to the central processor; in cabinets two, three, or four, they connect to the preceding cabinet. The first cabinet, and all but the last cabinet require two more 104-pin connectors to daisy-chain PIO signals and controls. The remaining connectors are 40-pin for intracabinet exchange of data, control signals, interrupts (first cabinet only), and for the optional test panel (first cabinet only). Four terminal blocks distribute one or two address lines (function lines) to each nest.

CABINET MASTER CLEAR, when pressed, resets all stored information within that cabinet. Placing the ON LINE/OFF LINE switch in the OFF LINE position prevents signals from passing through that cabinet in either direction.

Test Panel - The Digital IO Unit Test Panel, an option for the first cabinet only, is located beneath the digital control nest, and connected to it by two cables. Switches and lights shown in Figure 1-13-11 connect to two printed circuit cards in the digital control nest.

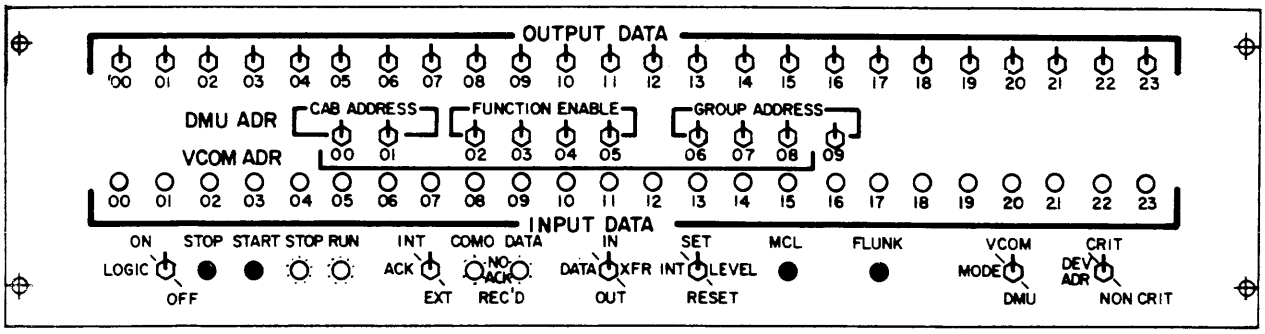


Figure 1-13-11. Digital IO Unit

IO Bay - Although each control bay contains one DIO nest, most multiplexer signals are handled in IO bays. An IO bay in the first DIO Unit cabinet can contain one DIO multiplexer nest and two single-row nests, either valve control, pulse counter input, or D/A output. Each IO bay in cabinets other than the first contains a DIO nest only.

Relay Bay - Each DIO Unit Cabinet can include a relay bay as the outermost bay to the right and to the left of the control bay. Each relay bay holds three relay nests, each consisting of one row of sixteen relay cards. The relay bays do not provide any internal logic or power. Each relay card is connected by a separate cable to a digital output relay driver card in an IO bay. Field connections to the relay points are made through 16 terminal boards, one per relay card, each having 24 screw connectors for N/O or N/C wiring to the eight relay contact sets on the card.

Multiplexer Nest

There are two sizes of multiplexer nests used in the Digital IO Unit -- three-row and single row. Refer to Figures 1-13-12 and 1-13-13. Each multiplexer row has 18 slots to accommodate up to 16 multiplexer cards, along with one or two control cards. An IO plate provides two control card slots for each multiplexer row, and three connectors for the nest data bus and control signals.

All cards in the multiplexer nests measure 8 x 8 inches; the control cards mounted in the two slots of the IO plate have 72 connector pins. Multiplexer cards, mounted in the remaining 16 slots in the row, have 56 pins, separated into two groups -- the upper 32 for field connections from the process instrumentation, the lower 24 dedicated to control logic. Control cards are composed entirely of medium scale integration (MSI) circuit modules, multiplexer cards contain both integrated circuits

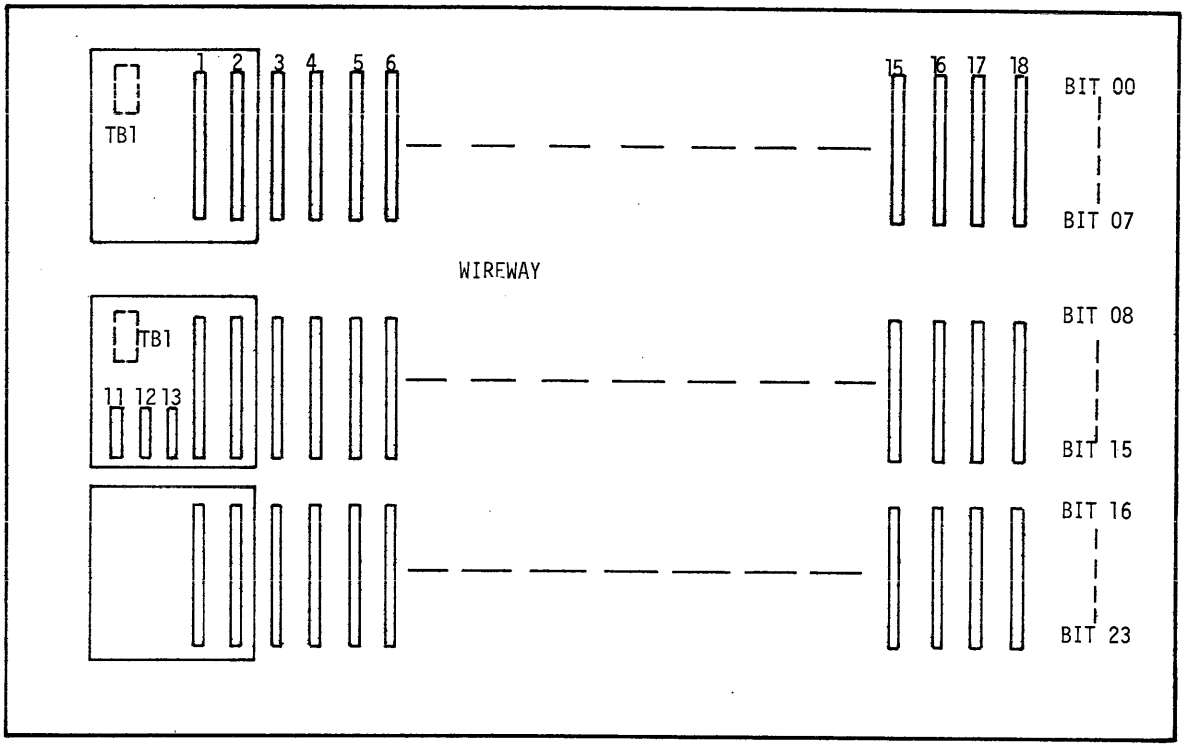


Figure 1-13-12. Digital I/O Multiplexer Nest, Front (Card Side) View

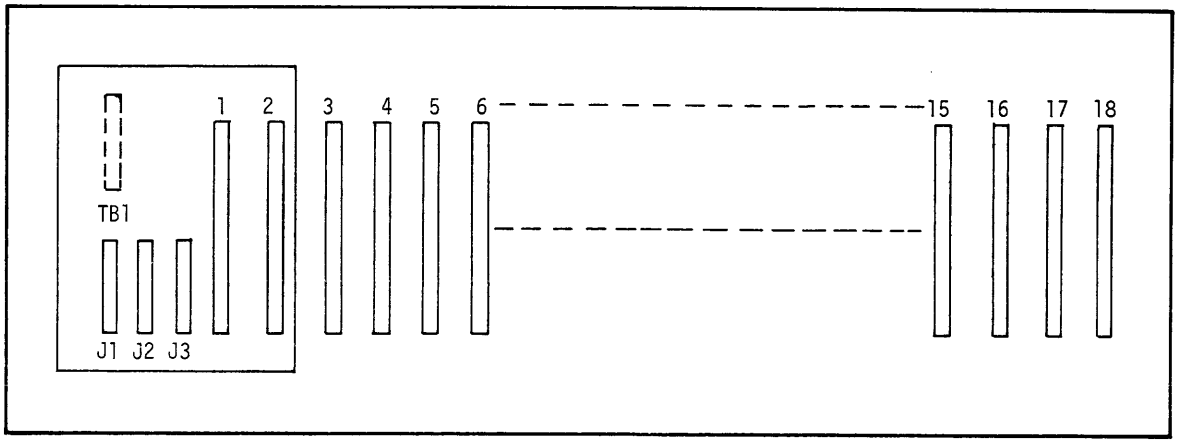


Figure 1-13-13. Pulse Counter/Analog Output/VCOM Nest, Front (Card Side) View

and discrete components. The analog output nest includes its own 15-VDC supply, and each valve control output nest has a -13.2-VDC supply.

Function

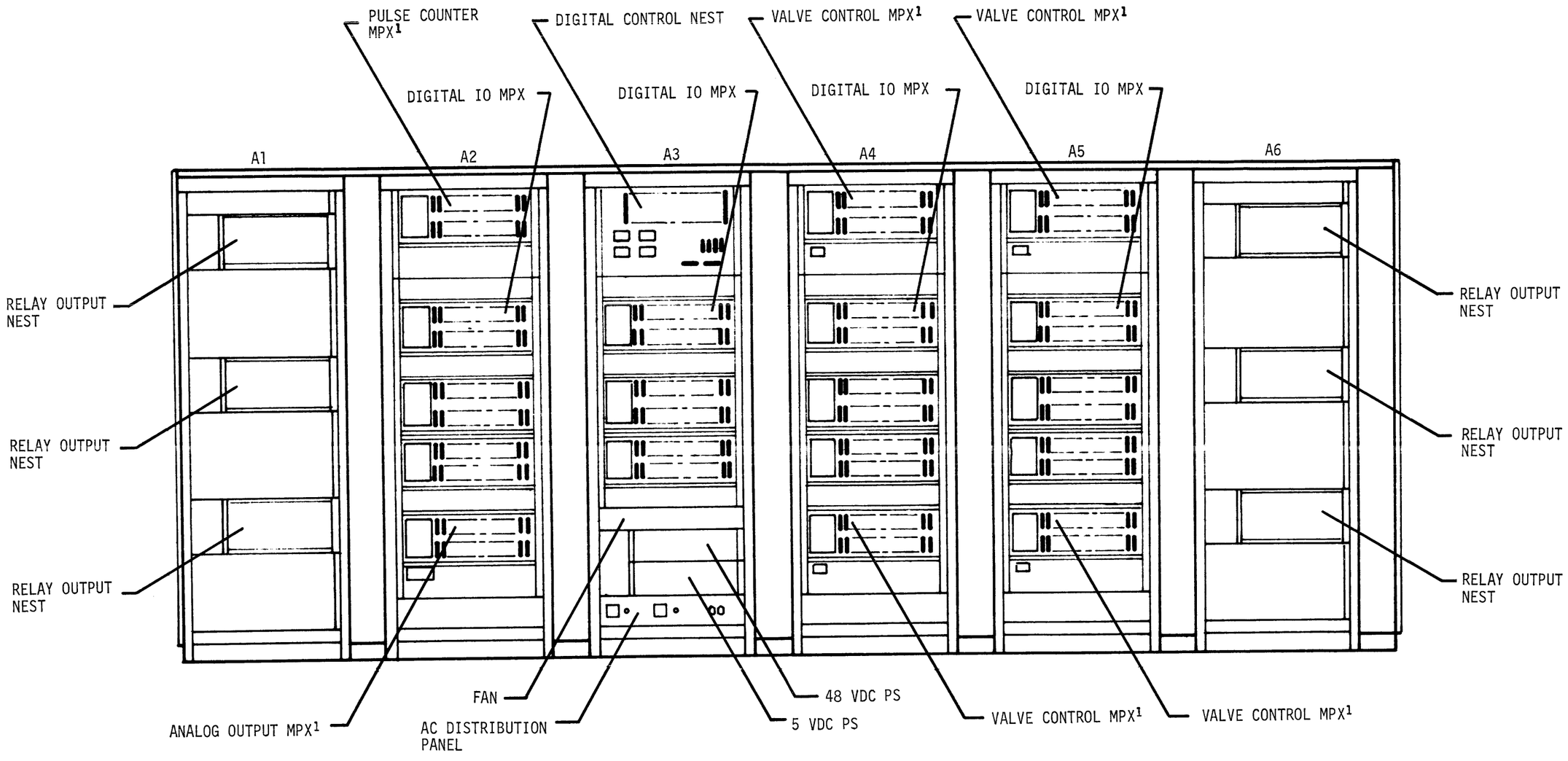
Two types of multiplexer nests are subdivided into functions -- three-row nests (DIO), which may be split into input and output rows, and single row nests in which a single card contains two separate multiplexer channels. An entire digital IO nest may be dedicated as either an input or output function, or the top row may be assigned one use, and the lower two rows, the other. A pulse counter multiplexer card contains a separate input channel in each half of the card. The upper half of every card in the row is assigned one function address; the lower half of every card, another. The analog output multiplexer is similarly packaged with two outputs per card. Again, two function lines are needed to select between upper and lower card halves. The digital control nest can provide for up to 12 function assignments in one cabinet.

Multiplexer Card

The Digital IO Unit multiplexer cards are packaged so that each card handles multiples of a particular type of input or output. Small increments in system capacity are accomplished by plugging in additional cards. Depending upon the type of multiplexer, a card contains from two to eight separate inputs or outputs that interface with the central processor's programmed data bus.

Reference Designation

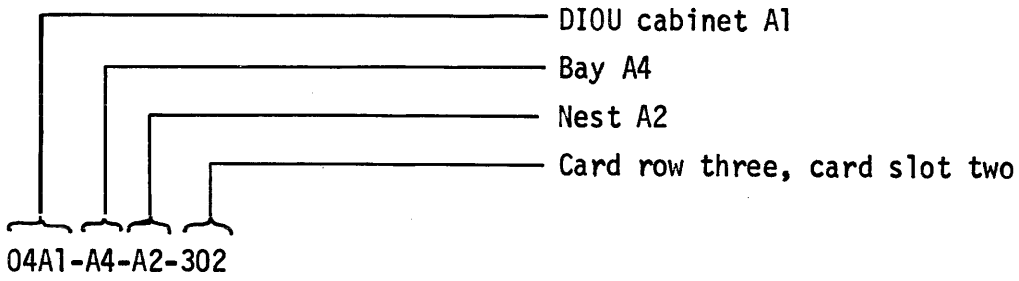
The Digital IO Unit reference designation is 04. DIOU cabinets, shown in Figure 1-13-14, are designated A1 through A4, bays within each cabinet



[1]First cabinet only.

Figure 1-13-14. Digital IO Unit

are designated A1 through A6. Nests within each bay are designated A1 through A3 for relay and IO bays, and A1 through A6 for the control bay. Digital control nest cards are designated 101-134. Multiplexer nest cards are designated 101-118, 201-218 and 301-318 (for three-row nests only). A typical full reference designation is written:



CONFIGURATION

Modularity is the keystone of the digital IO subsystem. The flexibility of the building-block approach allows system hardware to be matched closely to the number and variety of inputs and outputs initially required, without restricting future growth. A system of reserved space provides for orderly expansion by plugging additional printed circuit cards or adding prewired card nests. Similarly, new types of inputs or outputs can easily be added as required for changes in the process instrumentation. In short, the customer buys only what he needs, as he needs it.

To keep the variety of cabinet hardware and cable requirements within reason, some constraints must be placed on the physical arrangement of subsystem components. These restrictions concern assigning cabinet space, and implementing certain options.

Control Bay

Bay A3 in each cabinet is designated the control bay. Its top row is reserved for a digital control nest. AC is brought into a distribution panel at the bottom of the control bay, and the 5-VDC and 48-VDC power supplies for the cabinet are located in the two rows directly above the ac entry. The remainder of the control bay is taken up by a three-row digital IO nest. If the system is to include process interrupt inputs, these must be located in this DIO nest below the digital control nest in the first cabinet.

The smallest cabinet contains only the control bay. Larger cabinets may have two or three IO bays and possibly one or two relay bays in addition to the control bay.

First Cabinet Options

One of the restrictions in assigning cabinet space is that all options other than digital IO must be implemented in the first DIO Unit cabinet. These are the process interrupts, the pulse counters, the analog outputs, and the valve control outputs. Cabinets 2, 3, and 4 are used as required to implement the desired portion of the maximum 6,144 digital points. Relay bays are the end or outside bays in any size cabinet. As shown in Figure 1-13-15, the number and type of signals required determines the specific hardware configuration.

Digital Control Nest Options

The actual number of cards used in the digital control nest depends upon the number of bays within the cabinet, whether signals are daisy-chained to another cabinet, and (first cabinet only) whether process interrupts

CABINETS USED	REQUIRED					TOTAL BAYS	BAY DESIGNATIONS USED					
	DIGITAL IN/OUT SIGNALS	OTHER SIGNAL TYPES* RLY	PC	A/D	VC							
FIRST CABINET	384	---	--	--	---	1			A3			
	384	384	--	--	---	2	A1	--	A3			
	768	---	32	32	---	2		A2	A3			
	768	---	**	**	**	2			A3	A4		
	768	384	32	32	---	3	A1	A2	A3			
	768	384	**	**	**	3			A3	A4	--	A6
	1152	---	32	32	256	3		A2	A3	A4		
	1152	---	--	--	512	3			A3	A4	A5	
	1152	384	32	32	256	4	A1	A2	A3	A4		
	1152	384	--	--	512	4			A3	A4	A5	A6
	1536	---	32	32	512	4		A2	A3	A4	A5	
	1536	384	32	32	512	5	A1	A2	A3	A4	A5	
	1536	384	32	32	512	5		A2	A3	A4	A5	A6
	1536	768	32	32	512	6	A1	A2	A3	A4	A5	A6
SECOND CABINET	1920	***				1	***		A3			
	2304					2		A2	A3			
	2688					3		A2	A3	A4		***
	3072					4		A2	A3	A4	A5	
THIRD CABINET	3456	***				1	***		A3			
	3840					2		A2	A3			***
	4224					3		A2	A3	A4		
	4608					4		A2	A3	A4	A5	
FOURTH CABINET	4992	***				1	***		A3			
	5376					2		A2	A3			***
	5760					3		A2	A3	A4		
	6144					4		A2	A3	A4	A5	

CABINET SPACE ASSIGNMENT

FIRST CABINET

A1	A2	A3	A4	A5	A6
RELAY	PULSE COUNTER	DIGITAL CONTROL	VALVE CONTROL 1	VALVE CONTROL 3	RELAY
	DIGITAL IO	PROCESS INTERRUPT	DIGITAL IO	DIGITAL IO	
RELAY					RELAY
RELAY	ANALOG OUTPUT	FANS 48 VDC 5 VDC AC DISTRIB	VALVE CONTROL 2	VALVE CONTROL 4	RELAY

CABINET 2, 3, OR 4

A1	A2	A3	A4	A5	A6
RELAY		DIGITAL CONTROL			RELAY
	DIGITAL IO	DIGITAL IO	DIGITAL IO	DIGITAL IO	
RELAY					RELAY
RELAY		FANS 48 VDC 5 VDC AC DISTRIB			RELAY

*RLY = Relay outputs; PC = Pulse counter inputs; A/D = Analog outputs; VC = Valve control outputs.

**If not more than 128 valve outputs are required, 32 pulse counter inputs or 32 analog outputs can be provided in Bay A4.

***Relay bays designated A1, A6, or both can be added.

Figure 1-13-15. Digital IO Unit Cabinet Configuration

or valve control outputs are implemented. Refer to Figure 1-13-7. One card group (always present) exchanges signals with the central processor (first cabinet) or previous cabinet in a daisy chain; another group (as required) interfaces with the cabinet following in the chain. Similarly, for intracabinet communication, one group of cards (always present) services bays to the right of the control bay, and another (as required) services bays to the left. Refer to Table 1-13-4 for specific card types.

Test Panel

An optional test panel is available for the first Digital IO Unit cabinet. The panel is present (below the digital control nest) only in the cabinets implementing this option.

DIO Multiplexer Nest Options

From one to four DIO multiplexer nests may be implemented in each of up to four cabinets. From one to sixteen multiplexer cards may be inserted per row, with one, two, or three rows implemented in the nest. Nests may be split into input and output signal functions, with the top row dedicated to one function, and the lower two rows, another. Within the same vertical slot, each card row, top, center, and bottom, corresponds with an 8-bit block of the computer word -- bits 0 through 7, 8 through 15, and 16 through 23, respectively. Zeros will be read in place of the block associated with a row that is not implemented, or is assigned an output function. Similarly, bits of output data that correspond with a row that is not implemented, or is assigned an input function will have no effect.

Table 1-13-4. Card Complement, Digital Control Nest

CARD ASSY. NO.	CARD NAME	NUMBER REQUIRED
D3001BG	Differential Line Driver	2 each/cabinet plus 2 more if going to a subsequent cabinet
D3001BJ	Differential Line Receiver	
D3006RD	*DMU, Control, Nest Decoder, (wired), First Cabinet	1 in First cabinet only
D3006RE	*DMU, Control, Nest Decoder, (wired), Second Cabinet	1 in Second cabinet only
D3006RF	*DMU, Control, Nest Decoder, (wired), Third Cabinet	1 in Third cabinet only
D3006RG	*DMU, Control Nest Decoder, (wired), Fourth Cabinet	1 in Fourth cabinet only
D3001MY	DMU, Control, Output Data Oring	2/cabinet
D3001DD	DMU, Control, Input Data Oring	1/cabinet
D3001DJ	DMU, Control, Bus Splitter	2/Digital Control Bay and any bays to right of Digital Control Bay, plus 2 more for any bays to left of Digital Control Bay
D3001TJ	***DMU, Cabinet Tester, Control A	1/cabinet
D3001TK	***DMU, Cabinet Tester, Control B	1/cabinet
D3006RC	**DMU, Control, Interrupt Jumper	1 each/cabinet in first cabinet only
D3001DF	DMU, Control, Interrupt Storage	
D3001BU	DMU, VCOM, Address Control	1 each/cabinet only if cabinet contains VCOM Nest
D3001BV	DMU, VCOM, Time Pulse Gen.	

*A jumper zone on the DMU Nest Decoder card is wired differently for each of the four cabinets.

**This card provides the Standard (Default) Interrupt Level and bit position assignments for the Digital IO Unit.

***Required only if Test Panel is implemented.

The card type inserted in slot one of the row determines whether the row is an input or an output function. (Inputs and outputs can not be mixed in the same row.) Process interrupt multiplexer cards may be intermixed with contact input cards in an input row. The presence of one or more process interrupt inputs in a row requires an input buffer (storage) card in slot two, in addition to the control card in slot one. There is a choice of standard or high voltage versions for contact inputs and process interrupt inputs. The choice of output multiplexers includes steady-state, momentary, and relay driver (refer to Table 1-13-5).

Pulse Counter Input Multiplexer Nest Options

The single-row pulse counter multiplexer nest (only one per system) requires an input buffer card in slot two, in addition to the control card in slot one. Two counter speeds are available -- 100 pps with an 8-bit storage capacity, and 15,000 pps with 14-bit storage. Both are available in standard and high voltage versions, all may be intermixed in the row.

Analog Output Multiplexer Nest Options

The analog output is a single-row multiplexer nest (one per system) implemented with a control card in slot one, and from one to sixteen multiplexer cards. The standard multiplexer card converts a 10-bit binary sum to a current level from 10 to 50 milliamperes. Two optional cards make the conversion to a current level of 4-20 mA or a voltage level from 2- to 10-VDC output.

Table 1-13-5. Cards Required to Implement Multiplexer Nests

NEST TYPE	FUNCTION: TYPE	CONTROL CARD(S) (ONE OR TWO PER ROW, AS SHOWN)		PER-POINT CARDS (UP TO 16 PER ROW)
		SLOT 1	SLOT 2	SLOTS 3 to 18
Pulse Counter	High Speed Counter			
	Standard	D3001CP	D3001CN	D3001RU
	High Voltage Opt	D3001CP	D3001CN	D3001CQ
	Low Speed Counter			
	Standard	D3001CP	D3001CN	D3001RV
	High Voltage Opt	D3001CP	D3001CN	D3001CR
Digital IO	Contact Input:			
	Standard	D3001CH		D3001RS
	High Voltage Opt	D3001CH		D3001CG
	Process Interrupt:			
	Standard	D3001CH	D3001CN	D3001RT
	High Voltage Opt	D3001CH	D3001CN	D3001CM
	DC Output:			
	Momentary	D3001CL		D3001CK
	Steady-State	D3001CL		D3001CJ
	Relay Driver*	D3001CL		D3001CY
	*Latching Relay D3001DC			
	*Nonlatching Relay D3001DB			
Analog Output	Current Output			
	4 to 20 mA	D3001CX		D3001MZ
	10 to 50 mA	D3001CX		D3001CZ
	Voltage Output			
	2 to 10 V	D3001CX		D3001RZ
Valve Control	Valve Control Output	D3001BW		D3001BX

Notes: 1. Relay drivers located in the digital IO multiplexer nest are connected by individual cables to relays in relay nest.

2. Termination card D3001DH is inserted in J02 of the nest that terminates each digital IO bus (one or two per cabinet).

Valve Control Output Multiplexer Nest Options

Up to four valve control multiplexer nests can be implemented in the system. A control card in slot two selects one of the multiplexer cards in the single card row, and one of eight output driver pairs within the card. Up to 16 multiplexer cards may be inserted in each nest. There is only one type of valve control multiplexer card.

Cable Options

Although the standard cable entry to the DIO Unit is through the bottom of the cabinet, provision is made for an optional top entry. Signal cables are available in lengths ranging from 30 to 300 feet.

Cabinet 5-VDC Supply

The 5-VDC power supply used in each cabinet is available in two capacities -- 50 ampere, and 100 ampere. The choice is dictated by the number of signals implemented in the cabinet.

INTERFACE CONSIDERATIONS

Grounding

Considerable care has been paid to the grounding design. The neutral conductors of the ac prime power sources are <u>not</u> connected to the cabinet or signal ground. Provision is made, however, for connection of neutral to cabinet ground, should any installation require it.

Ground loops are avoided by keeping the cabinet and signal grounds electrically isolated except for one common tie-point. This point, in turn, is connected to the system ground point (MECCA) in the CP/IO Unit.

All synchronizer and control logic nests are electrically isolated from their frame (cabinet) supports through the use of insulating mounting brackets. Having the nests operate at signal ground, rather than cabinet ground, provides a greater degree of noise immunity.

Field Connections

Field wiring connections can be made directly at the nest backplane. A gold-plated male contact is crimped on wire as large as 16 AWG. These contacts are inserted in labelled 32-pin connector plates associated with each multiplexer card. As many as eight signals, having up to four connections, can be accommodated.

Alternatively, connections can be made to screw terminals on panels in an optional remote Termination Unit. Each prefabricated cable to the termination panels connects two, four, or sixteen multiplexer cards to field wiring, depending upon signal type.

The line drop at usable wire size limits line length for field inputs to 1000 feet, maximum. Although some integration is available at each input, long lines must be isolated from high power lines or other sources of excessive noise.

SPECIFICATIONS

Input Power Requirements

Primary ac of two different grades is required -- main power, a high quality, transient-free input for dc supplies; and auxiliary power, much

less critical, for fans and convenience outlets. The dc power supplies are designed to operate from a nominal 120-VAC supply in the frequency range of 47 to 430 Hz. The FOX 1 Power Distribution Unit is strongly recommended as the source for these supplies. Any alternative source must be highly reliable, and noise and transient free. Any transients will cause erroneous operation of the logic circuitry. Refer to Table 1-13-6 for a summary of input power specifications.

Table 1-13-6. Digital IO Unit Input Power Specifications

SOURCE	PHASE	FREQUENCY (HZ)			VOLTAGE			CURRENT (A)
		NOM	MIN	MAX	NOM	MIN	MAX	
POWER DISTRIBUTION UNIT 4 percent maximum harmonic content, with no single harmonics greater than 2 percent	1	400	372	430	120	108	133	25
ALTERNATIVE MAIN POWER	1	50	48	52	120	108	132	25
4 percent maximum harmonic content, with no single harmonics greater than 2 percent, and TRANSIENT-FREE	1	60	58	62	120	108	132	25
AUXILIARY POWER	1	50	47	53	120	108	132	20
	1	60	57	63	120	108	132	20

Physical Specifications

Bay Dimensions

a. Height 78.59 inches
b. Width 34.31 inches (includes 6-inch wireway)
c. Depth 26.13 inches

Weight Per Bay

a. Control Bay approximately 250 pounds
b. IO Bay approximately 200 pounds
c. Relay Bay approximately 200 pounds

Environmental Specifications

Temperature - The ambient temperature range with the equipment operating is 40 to 120 degrees F (4.4 to 49 degrees C). Ambient temperature range for storage is -30 to +150 degrees F (-34.4 to 66 degrees C). The maximum rate of operating temperature change is 1 degree F/minute.

Relative Humidity - The humidity range with the equipment operating is 20 percent to 95 percent (up to 86 F, wet bulb). The range for storage is 0-95 percent.

Ambient Air Contamination - Up to 10 ppm hydrogen sulfide or sulfur dioxide.

Altitude - The equipment will operate at altitudes ranging from -1000 feet up to 10,000 feet. For transport or storage, the altitude range extends to 50,000 feet.

Multiplexer Specifications

Input multiplexer specifications are summarized in Table 1-13-7. Output multiplexer specifications are summarized in Table 1-13-8.

Table 1-13-7. Input Multiplexer Card Specifications

CARD NAME OPTION	PART NO.	SIG/ CARD	INPUT VOLTAGE RANGE AT 48 VDC INTERNAL SUPPLY	CURRENT AT 48 V	OTHER SPECIFICATIONS
Contact Sensing	D3001RS	8	27-60 VDC	8 mA	
High Volt	D3001CG	8	100 VDC 130 V rms		
Process Interrupt	D3001RT	8	27-60 VDC	8 mA	
High Volt	D3001CM	8	100 VDC 130 V rms		
Pulse Counter (Low Speed)	D3001RV	2	27-60 VDC	8 mA	100 pps maximum input repetition rate. Read or Read and Reset capability.
High Volt	D3001CR	2	100 VDC 130 V rms		
Pulse Counter (High Speed)	D3001RU	2	9-20 VDC		15,000 pps maximum input repetition rate. Minimum pulse width 1 us.
High Volt	D3001CQ	2	100 VDC 130 V rms		

Note: Maximum line length for all inputs is 1000 feet. Contact, process interrupt, and low speed counter inputs all provide a 2 millisecond integration period.

Table 1-13-8. Output Multiplexer Card Specifications

CARD NAME OPTION	PART NO.	SIG/ CARD	MAX VOLT	MAX CURRENT	OTHER SPECIFICATIONS
Steady State	D3001CJ	8	60 VDC	0.5 A	0.4 V maximum offset, +1.1 mV/mA of load current ("ON"). Max leakage current 1.2 mA ("OFF"). 0-55 V lamp load, ≤ 5 A inrush current; 55-60 V lamp load, ≤ 3 A inrush. Positive output. Will withstand short circuit for at least 5 seconds.*
Momentary	D3001CK	8	60 VDC	0.5 A	16.5 ms pulse duration minimum standard.
Relay Driver	D3001CY	8			
Relay, Latch	D3001DC	8	300 VDC	100 VA	0.4 A at 115 rms max load accommodated by suppression values provided.
Relay, Non-L	D3001DB	8	230 V rms (to 400 Hz)	2 A (peak)	
Analog Output Current	D3001CZ	2		51.15 mA	50 µA/bit, 10-bit binary resolution. 0.35% of full scale accuracy, 0.1% linearity. Max load resistance 200 ohms. 0 to full scale in 50 µs (purely resistive load).
	D3001MZ	2		20.46 mA	Same as above except 20 µA/bit, 500 ohm max load.
Voltage	D3001RZ	2	10.23 VDC		Same as above except 10 mV/bit, output resistance 0.1 ohms. Overall accuracy 0.5% of full scale (no load).
Valve Control	D3001BX	8	-6.5 VDC		500 feet maximum line length, 22 AWG twisted pair cable. Nominal load resistance 100 ohms (for -6.5 volt output). Short circuit proof. Pulse width range 8.0 µs to 1.024 ms.

*Customer must furnish inductive load suppression to guarantee output terminal level at no time exceeds +60 V.

SECTION 14
TERMINATION UNITS

FIELD INSTRUMENTATION TERMINATION

Field instrument signals are received by, or originate in, either the Analog Input Unit (AIU) or the Digital Input/Output Unit (DIOU) of the FOX 1 system. These alarm, status, and process variable input signals to the FOX 1 system and manipulated variable and other control output signals from the FOX 1 system can interface with field instruments in several ways. Actual connections of field signals with the FOX 1 system can occur in three ways:

a. Direct local connection to the AIU and DIOU multiplexer circuit cards by crimped connector, or paddle where signal conditioning is required.

b. Indirect local connection to relay nests in relay bays of the DIOU or to Uniform Temperature Reference (UTR) Termination Panels in UTR bays of the AIU.

c. Remote connection to termination panels in Termination Units for cabling to the AIU and DIOU.

Local connection is less expensive but more complicated than remote connection. Remote connection provides a central place to terminate field wiring, presents a clear-cut interface between the field wiring and the computer system, and provides a central location for monitoring field signals by maintenance personnel. In addition, remote connection in Termination Units facilitates junction and tie-point connections, reduces the time required for system installation, and allows process interface

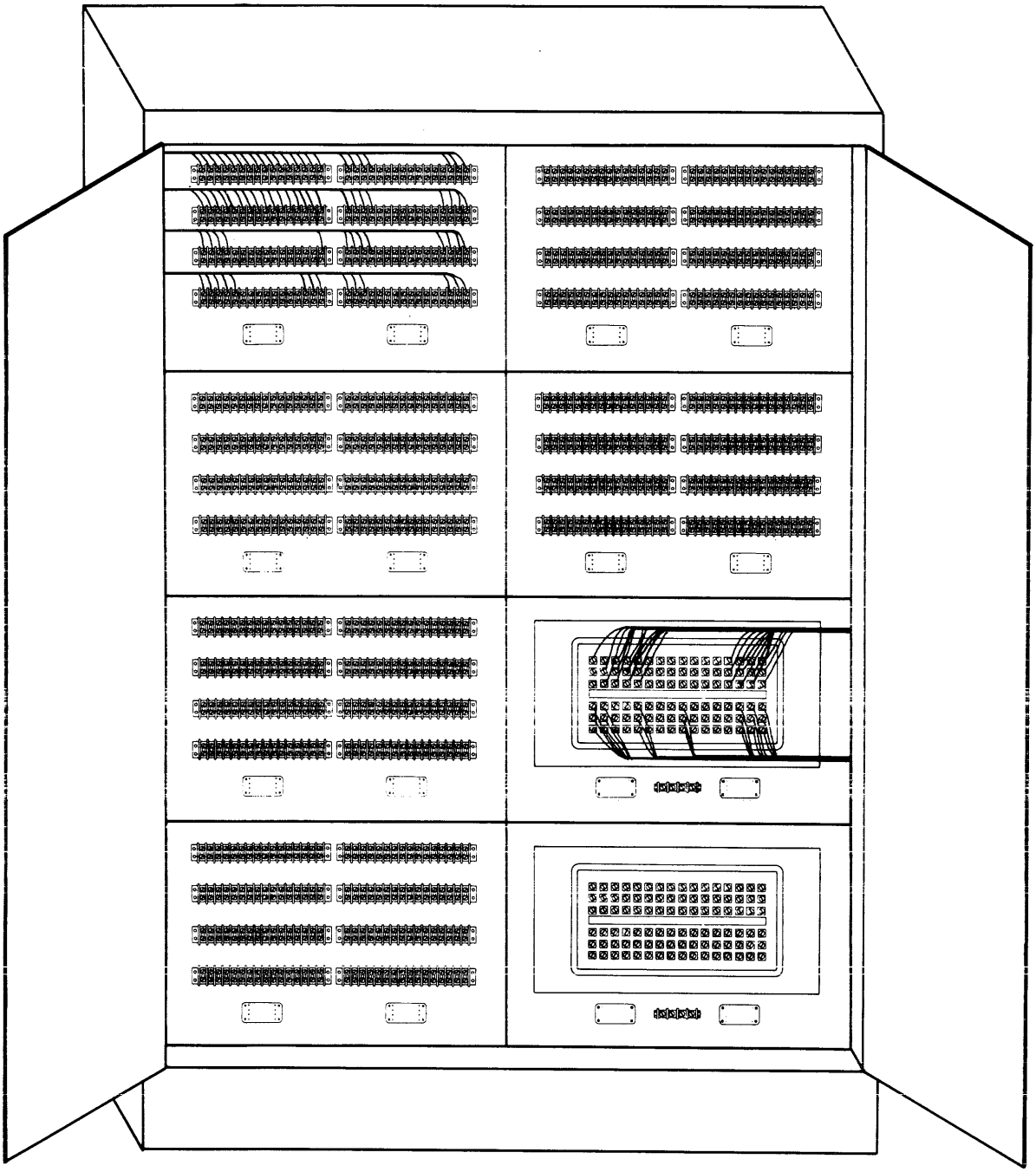


Figure 1-14-1. Typical Termination Unit (2 Bay, Front Access Only)

wiring to be completed (and ready) prior to installation of the FOX 1 functional units. Some systems will use a combination of these termination methods.

Additional information on local connection facilities and techniques is in documents related to the AIU and DIOU. The remainder of this chapter deals with remote connection using Termination Units.

TERMINATION UNITS

Termination Units (TU) provide an interposing facility between the field instrument wiring and the FOX 1 system AIU and DIOU. The TU is an optional alternative to terminating field wiring locally at analog or digital multiplexers. A typical TU is shown in Figure 1-14-1.

Termination Units consist of a sheet metal cabinet containing termination panels specifically designed to simplify connection of field wiring. Cabinets are available in four configurations of size and number of access doors. Termination Panels of six standard types are available to receive specific types of field signals on terminal boards. The panels are prewired from the terminal boards to cable connectors. Standard cables coupled to these connectors run horizontally across the panel to wireways, vertically through the wireways, and out of the top or bottom of the cabinet to cable raceways run to the AIU or DIOU. There are no active elements in TUs requiring power. A chassis ground connection from the Power Distribution Unit is the only nonsignal electrical connection received by most TUs. (External power supply connections are received by Analog Externally-Powered Transmitter Termination Panels.)

CABINETS

Cabinets for Termination Units are fabricated from 11 gauge cold rolled steel utilizing welded construction. Additional strength and stiffness are obtained by 7 gauge steel strapping and angle iron. All doors are constructed of 16 gauge steel and are assembled as pairs into a single door frame. The right-hand door of each pair is provided with a key lock to prevent access by unauthorized personnel. A lip on the left-hand door extends behind the right-hand door so that the left-hand door must be closed first, and cannot be opened when the right-hand door is closed. The entire cabinet is of a drip-proof design.

All TU cabinets are open at the bottom to allow cable entry/exit through the floor. From two to six openings (depending upon cabinet size) are provided in the top of each cabinet as cable ports. These ports are all 12 inches wide and 7 inches deep, and are covered by a metal plate held in place by pan-head screws when not used. Bottom cable entry/exit is recommended over top cable entry/exit, particularly where a water-tight enclosure is required.

Unistrut, welded to the top and bottom of the enclosure, provides a mounting for vertical struts to which the termination panels are attached. Vertical wireways, with access to cabinet cable ports, are provided for field (customer) wiring to all termination panels.

Cabinets are provided with or without thermal insulation at the customer's option. (Cabinets in which thermocouples are terminated must be insulated when Direct Analog Voltage Input Termination Panels receive the connections, and can be insulated when Uniform Temperature Reference Termination Panels receive the connections.) Insulated cabinets are internally lined with sufficient insulating material to maintain a temperature uniformity within the cabinet of ±2 degrees F. The internal cabinet temperature is read into the Analog Input System as a voltage

from a platinum RTD within the cabinet. This input must be connected in the same manner as a (standard) RTD field input either to the AIU cabinet or to a termination panel in the cabinet. This temperature is then used in the system program for junction compensation of all thermocouples terminated within that particular cabinet.

Insulating material used in TU cabinets is rigid fiberglass board made of fine glass fibers bonded with an inert thermosetting resin, pressed into a rigid self-supporting board, and faced with a vapor barrier of aluminum foil. One-inch thick insulating material is attached to all interior surfaces of the cabinet with adhesive. In like manner, 0.75-inch thick insulating material is attached to the entire inside surface of all doors.

Four basic cabinet configurations are available; each can be provided with or without insulation. Each configuration consists of two, four, or eight bays, where a "bay" is defined as the portion of a cabinet accessible through one door and capable of mounting one column of four termination panels. Specifications for each cabinet configuration are given in Table 1-14-1 and Table 1-14-2.

TERMINATION PANELS

Termination panels provide screw-type connection points for all field wiring terminated in Termination Units. There are six standard types of termination panel:

a. Direct Analog Voltage Input Termination Panel (D3005PY)

b. Analog Self-Powered Transmitter Termination Panel (D3005PZ)

c. Analog Externally-Powered Transmitter Termination Panel (D3004XA)

Table 1-14-1. Termination Unit Cabinet Data

TERMINATION PANEL	TERMINAL BLOCKS	REFERENCE DESIGNATION	TERMINAL SCREWS	SCREW TYPE	WIRE SIZE	SYSTEM CABLE CONNECTORS
Direct Analog Voltage Input	8 (4 rows of 2 blocks)	TB1 through TB8	32 per block	6-32	12 through 22 AWG	J1, J2
Analog Self-Powered Transmitter	8 (4 rows of 2 blocks)	TB1 through TB8	32 per block	6-32	12 through 22 AWG	J1, J2
Analog Externally-Powered Transmitter	8 (4 rows of 2 blocks)*	TB1 through TB8	32 per block	6-32	12 through 22 AWG	J1, J2
Digital IO	8 (4 rows of 2 blocks)	TB1 through TB8	32 per block	6-32	12 through 22 AWG	J1, J2
Uniform Temperature Reference	1 (6 rows of 16 terminals	0S, 0+, 0-1S, etc. through 32S, 32+, and 32-	96 total field screws	10-32 slotted pan-head with 0.00005 gold over 0.00002 nickel	14 through 22 AWG	J1, J2, TB1**
Relay Output	16	TB1 through TB16	24 per block	6-32	14 through 22 AWG	01 through 16***

* An additional 8-screw terminal block is provided (total of 9) to allow connection to four external power supplies for the connected transmitters.

** An additional 4-screw terminal block (TB1) is provided for connection to the RTD bulb. Wiring to TB1 is determined on a sales order basis to allow combining of this wiring from several UTR Termination Panels to form a single cable to the AIU.

*** Connectors are designated only by associated relay card position.

Table 1-14-2. Termination Unit Cabinet Capacities

CABINET PART NUMBERS	BAYS	ACCESS	TERMINATION PANEL CAPACITY	SIGNAL CAPACITY
D3004VA and D3005NE	2	Front Only	8	Up to 256 analog inputs, or up to 512 digital inputs or outputs
D3004MC and D3005NG	4	Front and Back	16	Up to 512 analog inputs, or up to 1024 digital inputs or outputs
D3004VB and D3005NF	4	Front Only	16	Up to 512 analog inputs, or up to 1024 digital inputs or outputs
D3004VC and D3005NH	8	Front and Back	32	Up to 1024 analog inputs, or up to 2048 digital inputs or outputs

d. Digital IO Termination Panel (D3004NE)

e. Uniform Temperature Reference Termination Panel (D3006HP)

f. Relay Output Termination Panel (D3004GV)

Various types of field input/output signals connected to the FOX 1 system are listed in Table 1-14-3 with the appropriate termination panel and termination panel capacity. Termination panel connection data are summarized in Table 1-14-4 and physical data are presented in Table 1-14-5.

The first four termination panels in the previous list are basic assemblies consisting of an aluminum panel 19 inches wide and 17.469 inches high, eight 32-pin terminal boards, and two 75-pin cable connectors. Individual field signal connections are made to the terminal boards and standard cables couple the termination panels to the Analog Input Unit or Digital IO Unit.

The last two termination panels in the previous list are unique assemblies designed for a specific type of input and output signals. The Uniform Temperature Reference Termination Panel provides a highly accurate means of terminating thermocouple inputs, without the need for reference junction ovens or ice water baths. This panel is the same size as the four basic panels, but is made of cold rolled steel and contains special insulated terminals with insulated covers.

The Relay Output Termination Panel contains a nest of relay circuit cards (operated by a Real Output Multiplexer nest in the Digital IO Unit) and a terminal board for field connection to the relay contacts. This panel is 19 inches wide, 26.1875 inches high, and 18 inches deep. Therefore, it can only be mounted in a cabinet having both front and back access. If only front access TU cabinets are available for a specific system, the

Table 1-14-3. Termination Panel Applications

TYPE OF INPUT OR OUTPUT SIGNAL	TERMINATION PANEL NAME	TERMINATION PANEL PART NUMBER	SIGNALS PER PANEL (MAX.)	SYSTEM CABLE CONNECTIONS
Direct Analog Voltage Inputs	Direct Analog Voltage Input	D3005PY	32 (3 wires)	To AIU
Resistance Temperature Detector Inputs	Direct Analog Voltage Input	D3005PY	16 (6 wires)	
Thermocouple Inputs	Direct Analog Voltage Input* Uniform Temperature Reference	D3005PY D3006HP	32 (3 wires) 32 (3 wires)	
Motion Balance Transmitter Inputs	Direct Analog Voltage Input Analog Self-Powered Transmitter	D3005PY D3005PZ	32 (4 wires) 32 (4 wires)	
Force Balance Transmitter Inputs	Analog Externally-Powered Transmitter	D3004XA	32 (4 wires)	
Contact Inputs	Digital IO	D3004NE	64 (2 wires)	To DIOU
Process Interrupt Inputs	Digital IO	D3004NE	64 (2 wires)	
Pulse Counter Inputs**	Digital IO	D3004NE	64 (2 wires)	
Digital Outputs (Solid State)	Digital IO	D3004NE	64 (2 wires)	From DIOU
Analog Outputs**	Digital IO	D3004NE	64 (2 wires)	
Valve Control Outputs	Digital IO	D3004NE	32 (16 increase and 16 decrease)	
Relay Outputs	Relay Output	D3004GV	128 (2 wires)	

* Must be in an insulated TU cabinet.

** One Digital Input Output Unit can handle a maximum of 32 pulse counter inputs and 32 analog outputs. One Digital IO Termination Panel can handle a maximum of 64 2-wire signals, which can be 32 pulse counter inputs and 32 analog outputs.

Table 1-14-4. Termination Panel Connection Data

FOXBORO PART	BAYS	ACCESS	PAIRS OF ACCESS DOORS	CABINET SIZE (INCHES)			DOOR CLEARANCE (INCHES)	TOP CABLE PORTS	INSULATION	APPROXIMATE WEIGHT (IN POUNDS)
				HEIGHT	WIDTH	DEPTH				
D3004VA	2	Front Only	1	76.875	45	20	19.125	2	NO	400
D3005NE	2	Front Only	1	76.875	45	20	19.125	2	YES	420
D3004MC	4	Front and Back	2	76.875	45	30	38.25	4	NO	500
D3005NG	4	Front and Back	2	76.875	45	30	38.25	4	YES	540
D3004VB	4	Front Only	2	76.875	86	20	19.125	3	NO	700
D3005NF	4	Front Only	2	76.875	86	20	19.125	3	YES	760
D3004VC	8	Front and Back	4	76.875	86	30	38.25	6	NO	800
D3005NH	8	Front and Back	4	76.875	86	30	38.25	6	YES	880

Table 1-14-5. Termination Panel Physical Data

TERMINATION PANEL	ASSEMBLY OUTLINE DIMENSIONS (IN INCHES)			MOUNTING PLATE DIMENSIONS (IN INCHES)			MOUNTING PLATE MATERIAL
	WIDTH	HEIGHT	DEPTH(MIN.)	WIDTH	HEIGHT	DEPTH	
Direct Analog Voltage Input	19.0	17.469	1.0	19.0	17.469	0.125	Aluminum
Analog Self-Powered Transmitter	19.0	17.469	1.0	19.0	17.469	0.125	Aluminum
Analog Externally-Powered Transmitter	19.0	17.469	1.0	19.0	17.469	0.125	Aluminum
Digital IO	19.0	17.469	1.0	19.0	17.469	0.125	Aluminum
Uniform Temperature Reference	19.0	17.469	4.625	13.750	5.812	0.125	Steel (CRS)
Relay Output	19.0	26.1875	18.0	15.950	4.156	0.125	Aluminum

Relay Output Termination Panel(s) must be mounted in a multiplexer bay added to the DIOU cabinet.

Black mylar marker strips painted with white mnemonics are available as options. These pressure-sensitive strips attach to the termination panels adjacent to the terminal boards to facilitate field wiring and to aid in locating signals for field maintenance. Nine standard marker strips are available for use with various type termination panels.

Detailed information on each termination panel is presented in the following descriptions.

Direct Analog Voltage Input Termination Panel

This panel (D3005PY) can receive analog signals from field instruments and cables them to the Analog Input Unit. The signals received by any one panel can correspond to any one entry in the following list:

a. 32 direct input analog voltage signals within the range of 0 to 1 volt

b. 32 direct input analog voltage signals within the range of 0 to 10 volts

c. 16 RTD inputs

d. 32 thermocouple inputs, provided the termination panel is in an insulated Termination Unit cabinet

Items a and b can be mixed in any combination for a maximum total of 32 inputs.

Physically, the panel consists of an aluminum plate on which are mounted four rows of two 16-point termination boards to receive the field wiring connections. The eight terminal boards contain number 6-32 screws and are capable of receiving field wiring from 22 AWG to 12 AWG wire. Two 75-pin cable connectors below the terminal boards provide coupling of the panel to the AIU by standard cables. Backplane wiring by shielded twisted-pair wire couples the top two rows of terminal boards to one cable connector (J1 on the left) and couples the bottom two rows of terminal boards to the other cable connector (J2 on the right).

Analog Self-Powered Transmitter Termination Panel

This panel (D3005PZ) can terminate up to 32 inputs from instrument transmitters, such as Foxboro motion balance type transmitters having current outputs of 10 to 50 ma, 4 to 20 ma, and 1 to 5 ma. Current loop resistors must be mounted on the panel so the voltage drop across them can be read as an analog input signal by the Analog Input Subsystem. Terminals are also prewired so that external recorders can be connected to any inputs, by locating a resistor either on the panel or externally. If no recorder connection is used, a jumper bar is inserted on the panel.

This panel consists of an aluminum plate on which are mounted four rows of two 16-point terminal boards to receive the field wiring and signal conditioning resistors. The eight terminal boards contain number 6-32 screws and are capable of receiving wiring from 22 AWG to 12 AWG. Two 75-pin cable connectors below the terminal boards provide coupling from the panel to the AIU by standard cables. Backplane wiring by shielded twisted-pair wires connects the top two rows of terminal boards to one cable connector (J1 on the left) and couples the bottom two rows of terminal boards to the other cable connector (J2 on the right). This panel is very similar to the Direct Analog Voltage Input Termination Panel described previously, except that this panel is wired to

accommodate signal conditioning required for implementing motion balance types of transmitters and their associated recorders.

Analog Externally-Powered Transmitter Termination Panel

This panel (D3004XA) can terminate up to 32 inputs from instruments such as Foxboro force balance transmitters requiring an external power supply.

The Analog Externally-Powered Transmitter Termination Panel has the same prewired capabilities as the Analog Self-Powered Transmitter Termination Panel plus the additional capability of providing connections to external power supplies. Connection to the external supply is made at a terminal strip, on this panel, which can accommodate up to four power supply inputs. These terminals are prewired to each row of the field terminal strips; i.e., each remotely located power supply can drive up to eight force balance transmitters. (If a requirement exists for redundant power supplies, this connection must be made externally.) Individual fuses provide over-current protection for the transmitters. Finally, a potentiometer for inserting loop (balancing) resistance has been provided.

This panel consists of an aluminum plate on which are mounted four rows of two 16-point terminal boards to receive the field wiring and signal conditioning resistors. The eight terminal boards contain number 6-32 screws and are capable of receiving wiring from 22 AWG to 12 AWG. Space for customer wiring is limited on the front of this panel due to the area required by the fuses and potentiometers. The full capacity of the panel can be used with AWG 22 customer wiring -- termination capacity is reduced as customer wire size increases -- approximately half capacity is available using AWG 12 customer wiring. Two 75-pin cable connectors below the terminal boards provide coupling from the panel to the AIU by standard cables. Backplane wiring by shielded twisted-pair wires

connects the top two rows of terminal boards to one cable connector (J1 on the left) and couples the bottom two rows of terminal boards to the other cable connector (J2 on the right). This panel is somewhat similar to the Direct Analog Voltage Input Termination Panel described previously, except that this panel is wired to accommodate signal conditioning required for implementing motion balance types of transmitters and their associated recorders. Terminals are prewired so that external recorders can be connected to any input, by locating a resistor either on the panel or externally. If no recorder connection is used, a jumper bar is inserted on the panel. The backplane wiring of this panel has provision for accommodating various transmitter current output ranges: 10 to 50 ma, 4 to 20 ma, and 1 to 5 ma. Resistors may be mounted on the terminal strip to convert various input current ranges to 1 volt full scale input signals which can be read into the FOX 1 Analog Input Subsystem.

Each of the eight terminal boards can provide connection for four inputs. Each group of input terminals is provided with an individual balancing potentiometer and fuse in series with the connection to an external power supply. The potentiometers are 500 ohms, 10 percent, 5 watts connected to terminals 1, 5, 9, and 13. The fuses are 0.062 ampere, quick-acting, glass tube type. The eight fuses in one row of terminal boards are connected in common to one power supply terminal. Eight individual terminals are provided on the panel as four pairs for connection to the positive and negative output of four external power supplies. Each pair of terminals is prewired to one row of field connection terminal boards (eight input signals), i.e., one supply can power the transmitters connected to TB1 and TB2, a second power supply can power the transmitters connected to TB3 and TB4, etc. If desired, the power supply terminals can be wired together to permit connecting all TB's to one power supply.

Digital IO Termination Panel

This panel (D3004NE) can terminate up to 64 inputs or outputs of the Digital Input Output Unit. Termination can be provided by this panel for the following:

a. 64 process interrupt inputs, in groups of 8

b. 64 contact inputs, in groups of 8

c. 64 digital outputs (solid state), in groups of 32

d. 32 pulse counter inputs, in one group, plus 32 other 2-wire signals

e. 32 analog outputs, in one group, plus 32 other 2-wire signals

f. 32 valve control outputs (16 increase and 16 decrease), in groups of 16

System cabling considerations require that once assigned, the Digital IO Termination Panel must be used only for that one type of digital input or output in groups of 32. The only exception is that priority interrupt inputs, contact inputs, and solid state digital outputs can be mixed in groups of eight on one panel (i.e., if 16 inputs are required on a particular panel for priority interrupts, 48 inputs may be implemented as contact inputs). All other types of digital inputs or outputs (valve control outputs, pulse counter inputs, and analog outputs may only be mixed on the same panel in groups of 32.

This panel consists of an aluminum plate on which are mounted four rows of two 16-point terminal boards to receive the field wiring. The eight terminal boards contain number 6-32 screws and are capable of receiving

wiring from 22 AWG to 12 AWG. Two 75-pin cable connectors below the terminal boards provide coupling from the panel to the DIOU by standard cables. Backplane wiring by shielded twisted-pair wires connects the left four terminal boards to one cable connector (J1 on the left) and couples the right four terminal boards to the other cable connector (J2 on the right). This panel is similar in appearance to the Direct Analog Voltage Input Termination Panel described previously except that this panel is wired differently, and the backplane wiring is different (this panel uses twisted-pair wiring and the Direct Analog Voltage Input Termination Panel used shielded twisted-pair wiring).

No signal conditioning of any type is provided on this panel. The backplane wiring of this panel is twisted-pair wires; backplane connections are made directly from the back of the terminal strips to the output connectors J1 and J2. The mating plugs are wired to cables which connect to the desired multiplexer nests in the DIOU.

Field wiring to the Digital IO Termination Panel is the same for all types of digital inputs and outputs (i.e., TB1 terminals 1 and 2, terminals 3 and 4,... to TB8 terminals 15 and 16 are used in pairs to terminate field wiring). The backplane wiring of the Digital IO Termination Panel is identical for all applications; therefore, the different applications require only different cable configurations and different multiplexer connector arrangements to interface to the various types of multiplexer cards.

Uniform Temperature Reference Termination Panel

This panel (D3006HP) provides termination facilities for up to 32 thermocouples with a high degree of accuracy. The panel is designed so that the termination surface temperature is uniform within ±0.2 degree F. A platinum RTD at the center of the termination surface monitors this

temperature and is connected as an input to the Analog Input Subsystem. The RTD error of ±0.2 degree F and the possible error in the Analog Input Subsystem of ±0.2 degree F produces an overall accuracy of temperature readings used for junction compensation of ±0.4 degree F.

The UTR Termination Panel consists of three major components:

a. A cold rolled steel mounting plate 17.469 inches high, 19 inches wide, and 0.125 inch thick that provides a mounting for the UTR plate assembly, the terminal board, and two 75-pin cable connectors.

b. A UTR plate assembly 5.812 inches high and 13.75 inches wide that provides the termination surface for thermocouple input wiring and the RTD for junction compensation.

c. Two cover assemblies (one for each side of the UTR plate assembly) 8.468 inches high, 17.5 inches wide, and 1.5 inches deep filled with insulating material to inhibit thermal changes at the UTR plate assembly.

The UTR plate assembly is the primary element of a UTR Termination Panel. It contains 96 separate nickel plated copper terminals arranged as six horizontal rows of 16 terminals. The top three rows of terminals provide the shield, plus, and minus connections for 16 thermocouples and the bottom three rows of terminals provide the minus, plus, and shield connections for 16 more thermocouples (from top to bottom, respectively). These terminals are cast in a special electrically-insulating, thermally-conducting epoxy resin to maintain electrical isolation and common temperature of each terminal. Thermal insulation is also provided in mounting the UTR plate assembly on the mounting plate.

Both ends of the terminals are tapped; the front end to receive the thermocouple connection screws, and the back end to receive the wiring-harness connection screws. All connection screws are 10-32 pan-head brass screws, plated with 0.00005 gold over 0.00002 nickel. These screws will accept field wiring from 22 AWG to 14 AWG. Fixed wiring-harness connections cable the terminals to the two 75-pin cable connectors (J1 on the left and J2 on the right) on the mounting plate. Standard system cables coupled to these connectors run the thermocouple signals to the Analog Input Unit.

A platinum resistance temperature detector (RTD), or thermal resistor, with an overall accuracy of ±0.02 ohms, at the center of the terminal matrix is cabled to a terminal board (TB1) at the front of the mounting panel. Wiring from this terminal board can be combined with similar wiring from other UTR Termination Panels in one cabinet for cabling to the AIU. The resistance of this RTD (100 ohms ±0.02 ohms at 32 degrees F) is monitored by a Type D3001RK RTD Multiplexer Input circuit card in the AIU to produce software-generated junction temperature compensation.

Two identical cover assemblies each attach to the mounting plate by four knurled nuts. One cover insulates the front of the UTR plate assembly; the other insulates the back.

Relay Output Termination Panel

This panel (D3004GV) provides normally open or normally closed relay contact termination for up to 128 field outputs. Output signals from Type D3001CY Relay Driver circuit cards in the Digital IO Unit are cabled to a wireway at the top of the Relay Output Termination Panel, and distributed to a row of 16 32-pin connectors. Each of these connectors provides the input to a type D3001DC Latching Relay Output or D3001DB Nonlatching Relay Output circuit card. Contact ouput connections from

each of these cards are available on a corresponding terminal board. Terminal boards are arranged in a row across the panel and numbered from TB16 through TB1 from left to right. Pins on the terminal boards are numbered from 1 through 24 from top to bottom. Terminals are available for field wiring in groups of three terminals per relay contact set -- eight contact sets per terminal board. Relay contacts are in Form C configuration. Field wiring follows the terminal boards vertically to a wireway at the bottom of the panel, then passes horizontally across the bottom of the panel to the cabinet wireway, then runs vertically to the cable port at the top or bottom of the cabinet.

A Relay Output Termination Panel consists of the following major components:

a. A relay nest of up to 16 circuit cards, which can be any mixture of Latching Relay (D3001DC) or Nonlatching Relay (D3001DB) types. Each card contains eight relays with Form C contacts. Cards are numbered 01 through 16 from left to right as viewed from the front of the TU cabinet. An electrical connector plate contains two horizontal rows of 16 connectors. Signals from one Relay Driver (D3001CY) circuit card in the Digital IO Unit are received at a 32-pin connector at the top of this plate, and passed directly to the relay circuit card. Output connections from the relay circuit card are received by a 24-pin connector at the bottom of this plate and passed by wire-wrapped leads to the terminal board panel.

b. A terminal board panel provides mounting for 16 24-point terminal boards. The terminal boards are in one horizontal row across the panel and numbered TB16 through TB1 from left to right as viewed from the back of the TU cabinet. Each terminal board is mounted vertically so the terminals are numbered from 1 through 24 from top to bottom. Terminals are

also labeled NC (normally closed), C (common), and NO (normally open) from top to bottom for each of the eight relay contact sets represented. Field wiring to these terminal boards can be from 22 AWG to 12 AWG and is attached by number 6-32 pan-head screws.

c. Two plastic (PVC) wireways. The wireway at the top of the assembly conducts input cables from the cabinet wireway to the 32-pin connectors of the relay nest. The wireway at the bottom of this assembly conducts output cables from the terminal boards to the cabinet wireway.

The relay nest extends 9 inches from the mounting unistrut towards the front of the cabinet. The wireways extend 9 inches from the mounting unistrut towards the back of the cabinet. Therefore, the entire Relay Output Termination Panel is 18 inches deep, and requires use of a 30-inch deep TU cabinet (front and back access).

The entire Relay Output Termination Panel assembly is 19 inches wide and 26.1875 inches high. Therefore, three of these assemblies can be mounted in a 2-bay column (front and back bays) of any Termination Unit. (Three Relay Output Termination Panels can also be mounted in a multiplexer bay of a DIOU.) These panels can not share any 2-bay column with any other type of termination panel. For example, a 4-bay front and back access termination unit could contain up to six Relay Output Termination Panels in two 2-bay columns. No other type termination panel can be used in a cabinet housing Relay Output Termination Panels.

CONFIGURATIONS

General rules for configurating a Termination Unit are:

1. The maximum number of termination cabinets per system is ten.

2. Digital IO Termination Panels may not be located in any bay containing any other type of termination panel.

3. Relay Output Termination Panels may not be located in a cabinet containing any other type of termination panel.

4. Thermocouple inputs must be terminated at an insulated cabinet and/or a UTR Termination Panel, i.e., at a Direct Analog Voltage Input Termination Panel in an insulated cabinet, or at a UTR Termination Panel in any cabinet.

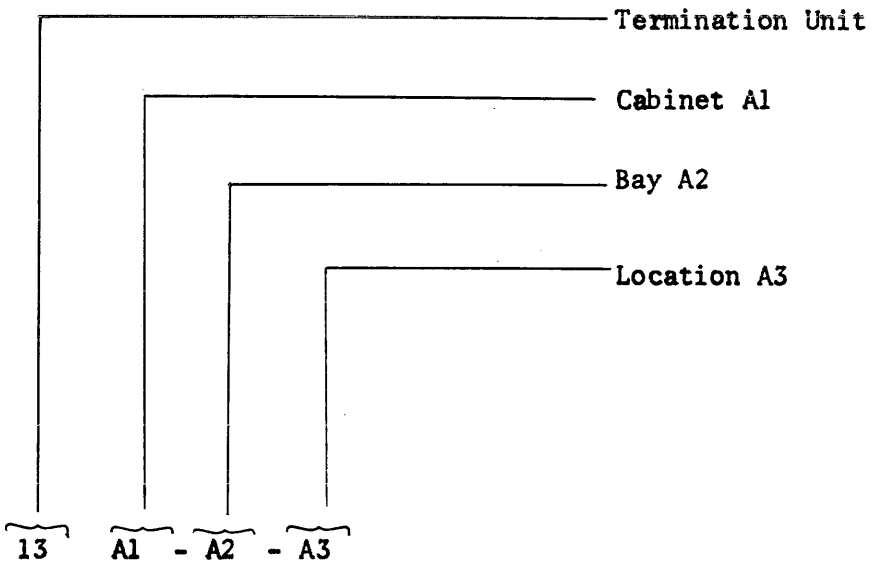
5. All termination panels except Relay Output Termination Panels or Digital IO Termination Panels, may be used in any available space in insulated TU cabinets in accordance with rules 2 and 3.

6. Blank panels are used in any locations not occupied by termination panels.

7. Relay Output Termination Panels may be used only in cabinets having both front and back access (cabinets D3004MC and D3004VC).

8. Terminal board marker strips, which vary according to signal type, are selected on a sales order basis.

Reference designation 13 is assigned to Termination Units and cabinets are numbered based on customer installation plans. Bays are numbered A1 through A8 from left to right as viewed from the front, then continued from left to right as viewed from the back. Panel locations are numbered A1 through A4 from top to bottom. A Relay Output Termination Panel, which extends through two back-to-back bays is assigned a location designation based on the front bay alone. For example:



ENVIRONMENT

Termination Unit cabinets are of drip-proof design, i.e., overhead condensation does not enter the cabinet when the bottom cable ports are used. When the top cable ports are used the cabinet affords some water repellent qualities, but can not be considered weatherproof.

The Termination Units operate satisfactorily in the following environmental conditions.

Temperature:	40F to 120F with a maximum time rate of ambient temperature change of 1 degree F per minute.
Relative Humidity:	20% to 95% over the operating temperature range, to a maximum wet-bulb temperature of 86F.

Vibration:	As per MIL Standard 810B, dated 15 June 1967, Method 514, Figure 514-6, Curve AB:
	5 to 27 Hz: ±1g (peak), sinusoidal input
	27 to 52 Hz: 0.036 inches (double amplitude displacement, sinusoidal input)
	52 to 300 Hz: ±5g (peak), sinusoidal input
Altitude:	-1000 to 10,000 feet
Contaminants:	0 to 10 ppm of H_2S or SO_2

The Termination Units will operate according to their performance specifications when returned to service following shipping or storage under the following environmental conditions, either singly or in any combination.

Temperature:	-30F to 150F
Relative Humidity:	0 to 95%
Altitude:	-1000 to 50,000 feet
Contaminants:	0 to 10 ppm of H_2S or SO_2

INDEX

READER'S COMMENT FORM

DOCUMENT TITLE FOX 1 Hardware Overview
NUMBER 73001BA-01-B

1. Are the scope, purpose, and content of this document as stated in the Preface what you expected them to be? ☐ Yes ☐ No

2. Do you feel this document fulfills the purpose and remains within the scope defined in the Preface? ☐ Yes ☐ No

3. Which of the following reference aids did you find most useful?

   ☐ Table of Contents ☐ Tabular Data ☐ Illustrations

4. How do you use this book? As a textbook (read from cover to cover) ☐
   As a reference book (selected portions) ☐ Both? ☐

5. Please rate this book as follows:

Textbook	Reference Book	Grade
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6. Please rate this book on presentation of material:

   ☐ Clear and concise ☐ Unclear and concise

   ☐ Clear but verbose ☐ Unclear and verbose

7. Please rate this book on extent of coverage

   ☐ Overabundant ☐ Sufficient ☐ Needed information missing

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