REVISIONS					
ZONE	SYM.	DESCRIPTION	BY	DATE	APPROVAL
	50	REL TO PILOT PROD # 3491	RP	9.27.77	
	51	RMV'D SHORT PCO # 3661	RP	12.12.77	
	52	ADDED SIGNAL *IPECLR TO SCHEM PER PCO # 3684	VC	2.13.78	
	A	REV CHG PER PCO 5382	NS	1.19.81	

J2

PIN	SIGNAL
1	GND
2	B3*Ø
3	B3*1
4	B3*2
5	B3*3
6	B3*4
7	B3*5
8	B3*6
9	B3*7
10	B3*8
11	B3*9
12	B3*1Ø
13	B3*11
14	B3*12
15	B3*13
16	B3*14
17	B3*15
18	B3*16
19	B3*17
20	B3*18
21	B3*19
22	B3*2Ø
23	B3*21
24	B3*22
25	B3*23
26	GND
27	RLP 25*
28	RLP 24*
29	RLP 23*
30	RLP 22*
31	RLP 21*
32	RLP 2Ø*
33	GND
34	GND
35	MM-R*
36	MM-B*
37	MM-M*
38	MM-W*
39	GND
40	READ KEYS*
41	GND
42	B3 H TO Z*
43	GND
44	CNTRL P TO IV/70*
45	GND
46	B3P TO IV/70*
47	GND
48	INT ON Z*
49	GND
50	GND

J1

PIN	SIGNAL
1	GND
2	C0
3	C1
4	C2
5	GND
6	LOAD
7	GND
8	SYS RST
9	GND
10	TB
11	GND
12	RSP
13	GND
14	MEM FAIL*
15	GND
16	AUTO
17	GND
18	REPEAT
19	GND
20	STEP
21	GND
22	A CYCLE
23	GND
24	DAV
25	GND
26	B3 P TO IV/90*
27	GND
28	CNTRL P TO IV/90
29	GND
30	LSI/Q*
31	GND
32	IV/90 TO IV/70*
33	GND
34	IOP 22*
35	IOP 21*
36	IOP 2Ø*
37	GND
38	
39	
40	
41	GND
42	ØZ
43	GND
44	
45	
46	
47	GND
48	
49	GND
50	GND

IV/70 MEMORY INTERFACE

J4

SIGNAL	PIN B	PIN A	SIGNAL
Vcc (+5V)	1	1	Vcc (+5V)
Vcc (+5V)	2	2	Vcc (+5V)
	3	3	
GND	4	4	GND
GND	5	5	GND
B3*Ø	6	6	BI-Ø
B3*1	7	7	BI-1
B3*2	8	8	BI-2
B3*3	9	9	BI-3
B3*4	10	10	BI-4
B3*5	11	11	BI-5
B3*6	12	12	BI-6
B3*7	13	13	BI-7
B3*8	14	14	BI-8
B3*9	15	15	BI-9
B3*1Ø	16	16	BI-1Ø
B3*11	17	17	BI-11
B3*12	18	18	BI-12
B3*13	19	19	BI-13
B3*14	20	20	BI-14
B3*15	21	21	BI-15
B3*16	22	22	BI-16
B3*17	23	23	BI-17
B3*18	24	24	BI-18
B3*19	25	25	BI-19
B3*2Ø	26	26	BI-2Ø
B3*21	27	27	BI-21
B3*22	28	28	BI-22
B3*23	29	29	BI-23
RLP 25*	30	30	P BUS-Ø
RLP 24*	31	31	P BUS-1
RLP 23*	32	32	P BUS-2
RLP 22*	33	33	P BUS-3
RLP 21*	34	34	MAV
RLP 2Ø*	35	35	MEM FAIL
INT ON Z*	36	36	MDATA TO BI
IOP 22*	37	37	
IOP 21*	38	38	SPR 1
IOP 2Ø*	39	39	
READ KEYS*	40	40	TEST CONDN

IV/70 MEMORY INTERFACE

J3

SIGNAL	PIN B	PIN A	SIGNAL
MM-R*	1	1	TEST SEL Ø
MM-B*	2	2	TEST SEL 1
MM-M*	3	3	TEST SEL 2
MM-W*	4	4	TEST SEL 3
LSI/Q*	5	5	TEST SEL 4
	6	6	TEST SEL 5
IV/90 TO IV/70*	7	7	PULSE SEL Ø
B3 H TO Z*	8	8	PULSE SEL 1
B3 P TO IV/70*	9	9	PULSE SEL 2
CNTRL P TO IV/70*	10	10	PULSE SEL 3
C0	11	11	PULSE SEL 4
C1	12	12	PULSE SEL 5
C2	13	13	PULSE SEL 6
AUTO	14	14	STEADY SEL Ø
REPEAT	15	15	STEADY SEL 1
LOAD	16	16	STEADY SEL 2
STEP	17	17	STEADY SEL 3
SYS RST	18	18	
ACYCLE	19	19	P PAGE-Ø
TB	20	20	P PAGE-1
DAV	21	21	P PAGE-2
RSP	22	22	P PAGE-3
B3 P TO IV/90*	23	23	P PAGE-4
MEM FAIL*	24	24	12V LO
CNTRL P TO IV/90	25	25	FORCE BREAK
ØZ	26	26	SLOW MEM OK
GND	27	27	SYS RST
	28	28	FLAG 1
	29	29	LSI OK
	30	30	MOD 2
	31	31	12V HI
	32	32	CLOCK
	33	33	5V LO
	34	34	OTHER CK
	35	35	5V HI
	36	36	GND
GND	37	37	GND
*MAL-EST	38	38	P MAP
Vcc (+5V)	39	39	Vcc (+5V)
Vcc (+5V)	40	40	Vcc (+5V)

CPU BOARD 1

J5

SIGNAL	PIN	PIN	SIGNAL
GND	1	A	GND
Vcc (+5V)	2	B	Vcc (+5V)
VDD (+12V)	3	C	VDD (+12V)
VBB (-5V)	4	D	VEE (-12V)
BI-Ø	5	E	BI-1
BI-2	6	F	BI-3
BI-4	7	H	BI-5
BI-6	8	J	BI-7
BI-8	9	K	BI-9
BI-1Ø	10	L	BI-11
BI-12	11	M	BI-13
BI-14	12	N	BI-15
GND	13	P	GND
BI-16	14	R	BI-17
BI-18	15	S	BI-19
BI-2Ø	16	T	BI-21
BI-22	17	U	BI-23
	18	V	
SYS RST	19	W	TEST CONDN
P BUS-Ø	20	X	P BUS-1
P BUS-2	21	Y	P BUS-3
TEST SELØ	22	Z	TEST SEL 1
TEST SEL 2	23	A	TEST SEL 3
TEST SEL 4	24	B	TEST SEL 5
GND	25	C	GND
PULSE SEL Ø	26	D	PULSE SEL 1
PULSE SEL 2	27	E	PULSE SEL 3
PULSE SEL 4	28	F	PULSE SEL 5
PULSE SEL 6	29	H	LSI OK
STEADY SELØ	30	J	STEADY SEL 1
STEADY SEL 2	31	R	STEADY SEL 3
DECIMAL L	32	L	DECIMAL M
DECIMAL R	33	M	FLAG 2
STORED OVFL	34	N	STORED ZERO
STORED MINUS	35	P	STORED CARRY
ADR Ø	36	R	ADR 1
ADR 2	37	S	ADR 3
GND	38	T	GND
ADR 6	39	U	ADR 7
ADR 8	40	V	ADR 9
ADR 1Ø	41	W	ADR 11
ADR 4	42	X	ADR 5
	43	Y	
CLOCK	44	Z	OTHER CK
GND	45	AA	GND
GND	46	BB	GND
GND	47	CC	GND
VDD (+12V)	48	DD	VDD (+12V)
Vcc (+5V)	49	EE	Vcc (+5V)
GND	50	FF	GND

TB1

1	+5V SENSE
2	GND
3	-5V
4	+12V
5	-12V

TB2

1	GND
2	+5V

NOTES: UNLESS OTHERWISE SPECIFIED
1. J10 IS NOT USED

ITEM NO	QTY	PART NUMBER	REF. DES.	DESCRIPTION

MATERIAL:
FINISH:
TREATMENT:
UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS INCHES TOLERANCES
DECIMAL XX ± XXX ± FRACTIONAL ± ANGULAR ±

SCALE:
DRAWN R. CALEJO 6-17-76
CHD J LYBERG 11-30-76
ENGR
MFG
RELEASED 4/11/81

FOUR-PHASE SYSTEMS, INC. ® CUPERTINO, CALIFORNIA

IV/90 BACKPLANE

D 900620072-07 A

SHEET 1 OF 3

REV

REVISIONS					
ZONE	SYM.	DESCRIPTION	BY	DATE	APPROVAL

CPU BOARD 2

J6

SIGNAL	PIN	PIN	SIGNAL
GND	1	A	GND
VCC (+5V)	2	B	VCC (+5V)
VDD (+12V)	3	C	VDD (+12V)
VBB (-5V)	4	D	VEE (-12V)
BI-Ø	5	E	BI-1
BI-2	6	F	BI-3
BI-4	7	H	BI-5
BI-6	8	J	BI-7
BI-8	9	K	BI-9
BI-10	10	L	BI-11
BI-12	11	M	BI-13
BI-14	12	N	BI-15
GND	13	P	GND
BI-16	14	R	BI-17
BI-18	15	S	BI-19
BI-20	16	T	BI-21
BI-22	17	U	BI-23
———	18	V	———
SYS RST	19	W	TEST CONDN
P BUS-Ø	20	X	P BUS-1
P BUS-2	21	Y	P BUS-3
TEST SEL Ø	22	Z	TEST SEL 1
TEST SEL 2	23	Ā	TEST SEL 3
TEST SEL 4	24	B̄	TEST SEL 5
GND	25	C̄	GND
PULSE SEL Ø	26	D̄	PULSE SEL 1
PULSE SEL 2	27	Ē	PULSE SEL 3
PULSE SEL 4	28	F̄	PULSE SEL 5
PULSE SEL 6	29	H̄	FLAG 1
STEADY SEL Ø	30	J̄	STEADY SEL 1
STEADY SEL 2	31	K̄	STEADY SEL 3
DECIMAL L	32	L̄	DECIMAL M
DECIMAL R	33	M̄	FLAG 2
STORED OVFL	34	N̄	STORED ZERO
STORED MINUS	35	P̄	STORED CARRY
ADR Ø	36	R̄	ADR 1
ADR 2	37	S̄	ADR 3
GND	38	T̄	GND
ADR 6	39	Ū	ADR 7
ADR 8	40	V̄	ADR 9
ADR 10	41	W̄	ADR 11
ADR 4	42	X̄	ADR 5
———	43	Ȳ	SPAR 1
CLOCK	44	Z̄	OTHER CK
GND	45	AA	GND
GND	46	BB	GND
GND	47	CC	GND
VDD (+12)	48	DD	VDD (+12)
VCC (+5)	49	EE	VCC (+5)
GND	50	FF	GND

MEMORY MAP BOARD

J7

SIGNAL	PIN	PIN	SIGNAL
GND	1	A	GND
VCC (+5V)	2	B	VCC (+5V)
VDD (+12V)	3	C	VDD (+12V)
VBB (-5V)	4	D	VEE (-12V)
BI-Ø	5	E	BI-1
BI-2	6	F	BI-3
BI-4	7	H	BI-5
BI-6	8	J	BI-7
BI-8	9	K	BI-9
BI-10	10	L	BI-11
BI-12	11	M	BI-13
BI-14	12	N	BI-15
GND	13	P	GND
BI-16	14	R	BI-17
BI-18	15	S	BI-19
BI-20	16	T	BI-21
BI-22	17	U	BI-23
*IPECLR	18	V	———
SYS RST	19	W	TEST CONDN
P BUS-Ø	20	X	P BUS-1
P BUS-2	21	Y	P BUS-3
TEST SEL Ø	22	Z	TEST SEL 1
TEST SEL 2	23	Ā	TEST SEL 3
TEST SEL 4	24	B̄	TEST SEL 5
GND	25	C̄	GND
PULSE SEL Ø	26	D̄	PULSE SEL 1
PULSE SEL 2	27	Ē	PULSE SEL 3
PULSE SEL 4	28	F̄	PULSE SEL 5
PULSE SEL 6	29	H̄	*MALF RST
STEADY SEL Ø	30	J̄	STEADY SEL 1
STEADY SEL 2	31	K̄	STEADY SEL 3
BANK-Ø	32	L̄	BANK-1
BANK-2	33	M̄	PPAGE-Ø
PPAGE-1	34	N̄	PPAGE-2
PPAGE-3	35	P̄	PPAGE-4
MAV	36	R̄	MEM FAIL
MDATA TO BI	37	S̄	FORCE BREAK
GND	38	T̄	GND
MOD 2	39	Ū	SLOW MEM OK
MPR	40	V̄	CONST TO BI
MRAM-R	41	W̄	———
S1	42	X̄	———
———	43	Ȳ	———
CLOCK	44	Z̄	OTHER CK
GND	45	AA	GND
GND	46	BB	GND
GND	47	CC	GND
VDD (+12)	48	DD	VDD (+12)
VCC (+5)	49	EE	VCC (+5)
GND	50	FF	GND

MEMORY BOARD 1

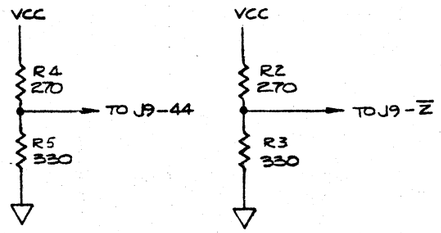
J8

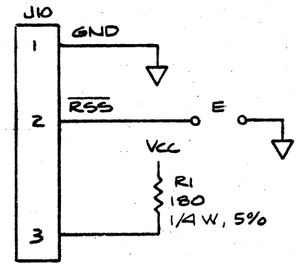
SIGNAL	PIN	PIN	SIGNAL
GND	1	A	GND
VCC (+5V)	2	B	VCC (+5V)
VDD (+12V)	3	C	VDD (+12V)
VBB (-5V)	4	D	VEE (-12V)
BI-Ø	5	E	BI-1
BI-2	6	F	BI-3
BI-4	7	H	BI-5
BI-6	8	J	BI-7
BI-8	9	K	BI-9
BI-10	10	L	BI-11
BI-12	11	M	BI-13
BI-14	12	N	BI-15
GND	13	P	GND
BI-16	14	R	BI-17
BI-18	15	S	BI-19
BI-20	16	T	BI-21
BI-22	17	U	BI-23
*IPECLR	18	V	BI-23
SYS RST	19	W	———
P BUS-Ø	20	X	P BUS-1
P BUS-2	21	Y	P BUS-3
SP1	22	Z	SP7
SP2	23	Ā	SP8
SP3	24	B̄	SP9
GND	25	C̄	GND
PULSE SEL Ø	26	D̄	PULSE SEL 1
PULSE SEL 2	27	Ē	PULSE SEL 3
PULSE SEL 4	28	F̄	PULSE SEL 5
PULSE SEL 6	29	H̄	*MALF RST
SP4	30	J̄	SP10
SP5	31	K̄	SP11
BANK-Ø	32	L̄	BANK-1
BANK-2	33	M̄	PPAGE-Ø
PPAGE-1	34	N̄	PPAGE-2
PPAGE-3	35	P̄	PPAGE-4
MAV	36	R̄	MEM FAIL
MDATA TO BI	37	S̄	SP12
GND	38	T̄	GND
SP6	39	Ū	SP13
MPR	40	V̄	CONST TO BI
MRAM-R	41	W̄	S2
S1	42	X̄	EMAP
OPEN	43	Ȳ	SPAR 1
CLOCK	44	Z̄	OTHER CK
GND	45	AA	GND
GND	46	BB	GND
GND	47	CC	GND
VDD (+12)	48	DD	VDD (+12)
VCC (+5)	49	EE	VCC (+5)
GND	50	FF	GND

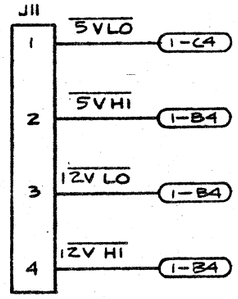
MEMORY BOARD 2

J9

SIGNAL	PIN	PIN	SIGNAL
GND	1	A	GND
VCC (+5V)	2	B	VCC (+5V)
VDD (+12V)	3	C	VDD (+12V)
VBB (-5V)	4	D	VEE (-12V)
BI-Ø	5	E	BI-1
BI-2	6	F	BI-3
BI-4	7	H	BI-5
BI-6	8	J	BI-7
BI-8	9	K	BI-9
BI-10	10	L	BI-11
BI-12	11	M	BI-13
BI-14	12	N	BI-15
GND	13	P	GND
BI-16	14	R	BI-17
BI-18	15	S	BI-19
BI-20	16	T	BI-21
BI-22	17	U	BI-23
*IPECLR	18	V	BI-22
SYS RST	19	W	———
P BUS-Ø	20	X	P BUS-1
P BUS-2	21	Y	P BUS-3
SP1	22	Z	SP7
SP2	23	Ā	SP8
SP3	24	B̄	SP9
GND	25	C̄	GND
PULSE SEL Ø	26	D̄	PULSE SEL 1
PULSE SEL 2	27	Ē	PULSE SEL 3
PULSE SEL 4	28	F̄	PULSE SEL 5
PULSE SEL 6	29	H̄	*MALF RST
SP4	30	J̄	SP10
SP5	31	K̄	SP11
BANK-Ø	32	L̄	BANK-1
BANK-2	33	M̄	PPAGE-Ø
PPAGE-1	34	N̄	PPAGE-2
PPAGE-3	35	P̄	PPAGE-4
MAV	36	R̄	MEM FAIL
MDATA TO BI	37	S̄	SP12
GND	38	T̄	GND
SP6	39	Ū	SP13
MPR	40	V̄	CONST TO BI
MRAM-R	41	W̄	S2
S1	42	X̄	EMAP
GND	43	Ȳ	SPAR 1
CLOCK	44	Z̄	OTHER CK
GND	45	AA	GND
GND	46	BB	GND
GND	47	CC	GND
VDD (+12)	48	DD	VDD (+12)
VCC (-5)	49	EE	VCC (+5)
GND	50	FF	GND







ITEM NO	QTY	PART NUMBER	REF. DES.	DESCRIPTION

MATERIAL: ———
WEIGHT:
FINISH: ———
TREATMENT:
UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS INCHES TOLERANCES
DECIMAL .XX ± .XXX ± FRACTIONAL ± ANGULAR ±

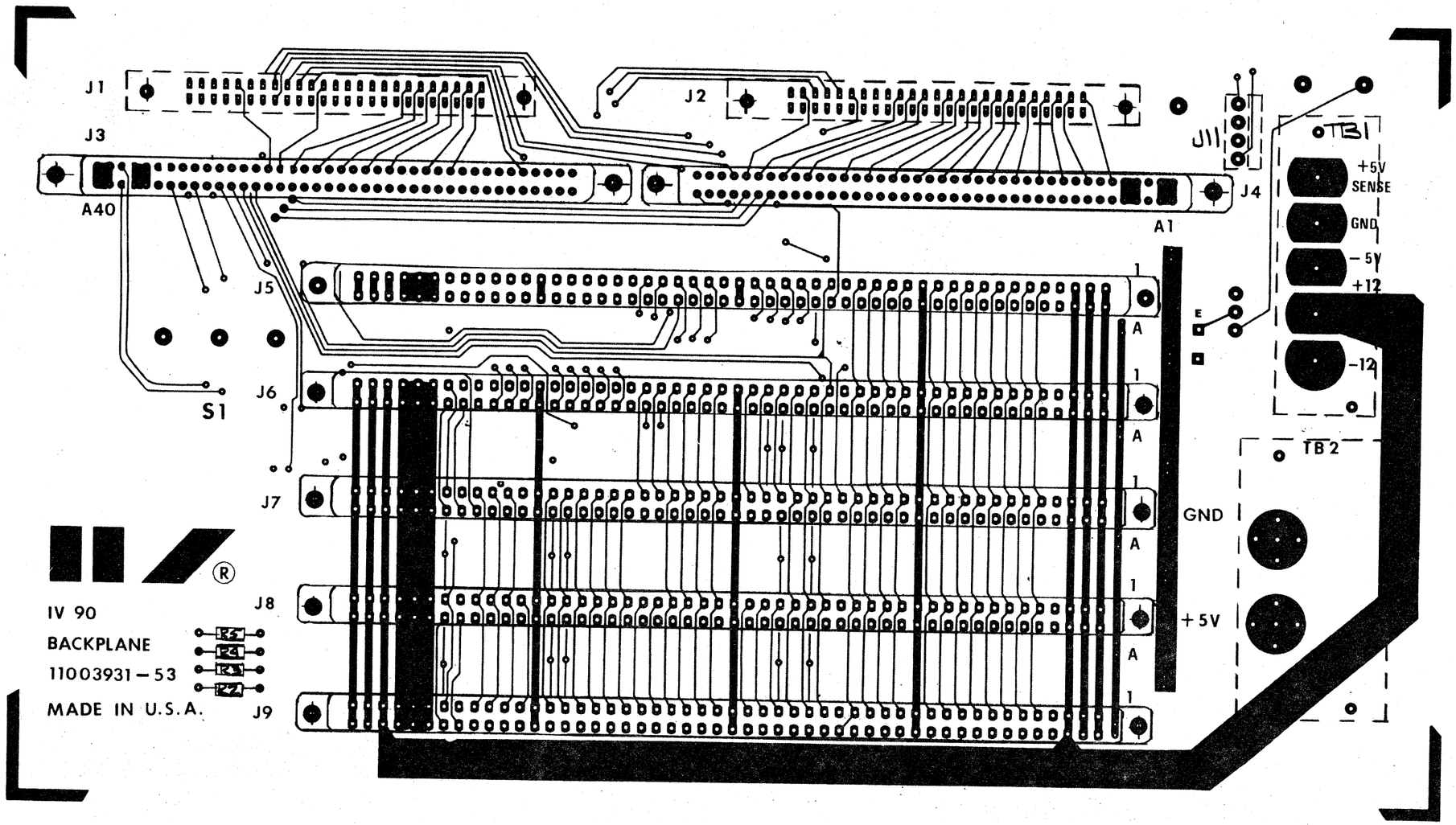
SCALE: ———
DRAWN R. CLAVEJO DATE 6-17-76
CKD J. LYBERG DATE 11-30-76
ENGR DATE
MFG DATE
RELEASED DATE 12/1/76

FOUR-PHASE SYSTEMS, INC.® CUPERTINO, CALIFORNIA

IV/90 BACKPLANE

D 90062072-07 A

SHEET 2 OF 3 REV



DRAWN VIKKI DATE 1.3.78	FOUR-PHASE SYSTEMS, INC. CUPERTINO, CALIFORNIA	
CHECKED Hans Sasso 1-4-78		
ENGINEER	IV/90 BACKPLANE	
MFG A.J. DiFrancesco 1-4-78	90062072-07	A
RELEASED Christoffersen 1/4/78	SHEET 3 OF 3	REV