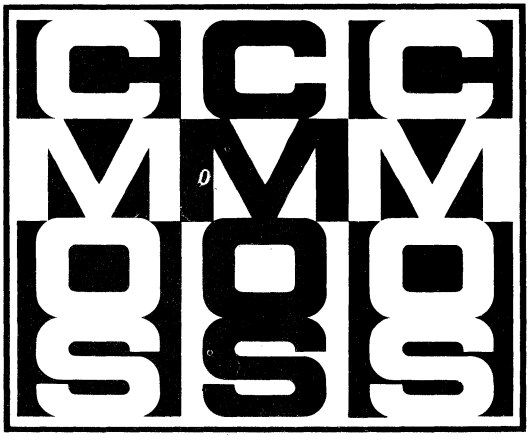
FAIRCHILD SEMICONDUCTOR

34000
ISOPLANAR
CMOS DATA BOOK

1975

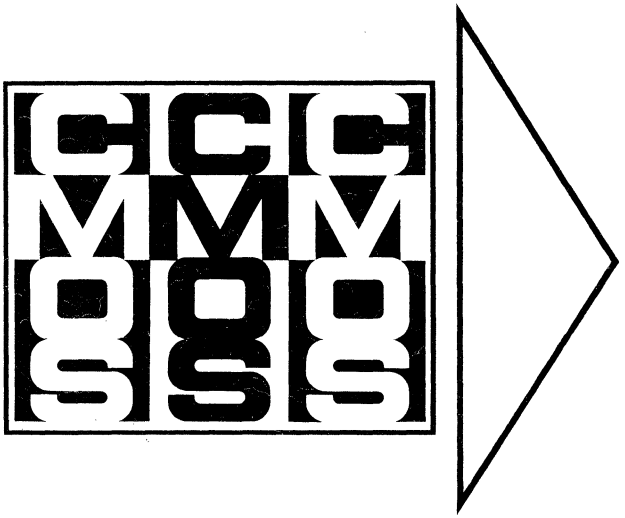
34000 ISOPLANAR CMOS DATA BOOK



FAIRCHILD
SEMICONDUCTOR

464 Ellis Street, Mountain View, California 94042

TABLE OF CONTENTS



34000
SERIES CMOS

GENERAL DESCRIPTION – Fairchild CMOS logic combines the popular 4000 series functions with the advanced Isoplanar C process. The result is a logic family with a superior combination of noise immunity and standardized drive characteristics. At static conditions, these devices dissipate very low power, typically 10 nW per gate. The low power combined with the wide (3 to 15 V) recommended operating supply voltage requirement greatly minimizes power supply costs. The CMOS family is designed with standardized output drive characteristics which, combined with relative insensitivity to output capacitance loading, simplify system design.

- **LOW POWER – TYPICALLY 10 nW PER GATE STATIC**
- **WIDE OPERATING SUPPLY VOLTAGE RANGE –**
  3 TO 15 V RECOMMENDED
  18 V ABSOLUTE MAXIMUM
- **HIGH NOISE IMMUNITY**
- **BUFFERED OUTPUTS STANDARDIZE OUTPUT DRIVE AND REDUCE VARIATION OF PROPAGATION DELAY WITH OUTPUT CAPACITANCE**
- **WIDE OPERATING TEMPERATURE RANGE**
  COMMERCIAL –40°C TO +85°C
  MILITARY –55°C TO +125°C
- **HIGH DC FAN OUT – GREATER THAN 50**

ISOPLANAR C

The Fairchild CMOS logic family uses Isoplanar C for high performance. This technology combines local oxidation isolation techniques with silicon gate technology to achieve an approximate 35% savings in area as shown in Figure 1-1a. Operating speeds are increased due to the self-alignment of the silicon gate and reduced sidewall capacitance.

Conventional CMOS circuits are fabricated on an n-type substrate as shown in Figure 1-1b. The p-type substrate required for complementary n-channel MOS is obtained by diffusing a lightly doped p-region into the n-type substrate. Conventional CMOS fabrication requires more chip area and has slower circuit speeds than Isoplanar C CMOS. This is a result of the n+ or p+ channel stop which surrounds the p- or n-channels respectively in CMOS, Silicon gate CMOS (Figure 1-1c) has a negligible reduction in area, though transient performance is improved.

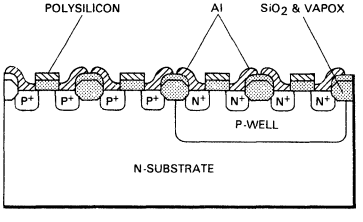


Fig. 1-1a. ISOPLANAR C CMOS STRUCTURE REDUCES AREA 35%

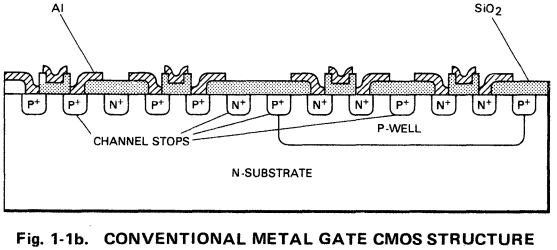


Fig. 1-1b. CONVENTIONAL METAL GATE CMOS STRUCTURE

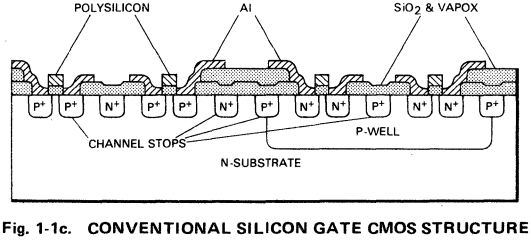


Fig. 1-1c. CONVENTIONAL SILICON GATE CMOS STRUCTURE REDUCES AREA 8%

FULLY BUFFERED CONFIGURATION DESCRIPTION

Fairchild CMOS logic is designed with the system user in mind. Output buffering is used on all devices to achieve high performance, standardized output drive, highest noise immunity and decreased ac sensitivity to output loading. Figure 1-2 illustrates a conventional unbuffered 2-Input NOR Gate. Either n-channel transistor connected to V_{SS} (ground) conducts when either input is HIGH, causing the output to go LOW through the ON resistance of the device. If both inputs are HIGH, both n-channel devices are on; effectively halving the ON resistance, thereby making the output impedance (and hence fall time) a function of input variables. Similarly the p-channel devices are switched on by LOW signals; i.e. when both inputs are LOW, conduction from V_{DD} to the output will occur.

Since the p-channel devices are in series, their ON resistance must be decreased (larger chip area) to hold output HIGH impedance within specification. As the number of gate inputs increases, even larger p-channel devices are required, and the output impedance to V_{SS} becomes even more pattern sensitive.

A conventional unbuffered CMOS 2-Input NAND Gate interchanges the parallel and serial transistor gating to achieve the NAND function (Figure 1-3). The changes in output resistance then move to the p-channel transistors connected to V_{DD}, while the n-channel devices must be increased in size due to their serial connection.

Fairchild CMOS uses small geometry logic transistors to generate the required function which drive standard low impedance output buffers (Figures 1-4 and 5). This technique reduces chip size, since only two large output transistors are required and rise and fall times are independent of input pattern. Buffered outputs also increase system speeds and make propagation delay less sensitive to output capacitance. Figure 1-6 illustrates typical propagation delay vs. output capacitance for conventional and buffered CMOS Gates.

Another advantage of the Fairchild approach is improved noise immunity. Because of the increased voltage gain, nearly ideal transfer characteristics are realized as shown in Figure 1-7. The high gain (greater than 10,000) also provides significant pulse shaping; the waveforms of Figures 1-8 and 9 compare the output waveforms of conventional and buffered CMOS gates. For input transition times of 100 ns or less, the outputs of both gate types are similar. When the input transitions are stretched to one microsecond, the conventional gate exhibits increased transition times while the buffered gate has unchanged output transition times. This feature eliminates progressive deterioration of pulse characteristics in a system. The combination of Isoplanar C and buffered outputs results in new standards of CMOS logic performance.

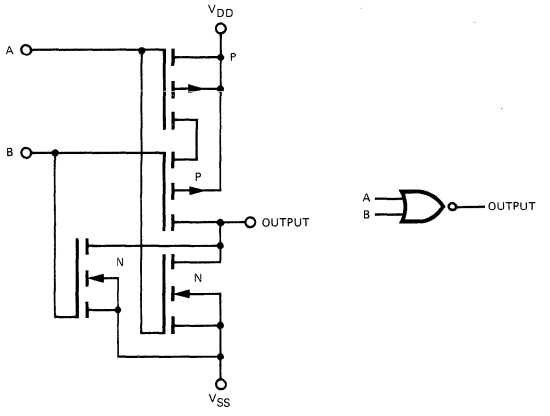


Fig. 1-2. CONVENTIONAL NON-BUFFERED 2-INPUT NOR GATE

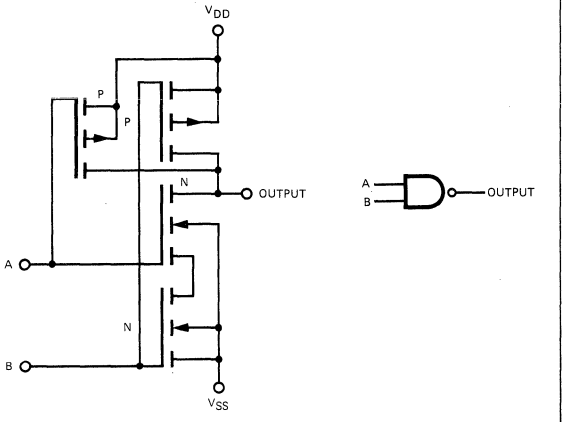


Fig. 1-3. CONVENTIONAL NON-BUFFERED 2-INPUT NAND GATE

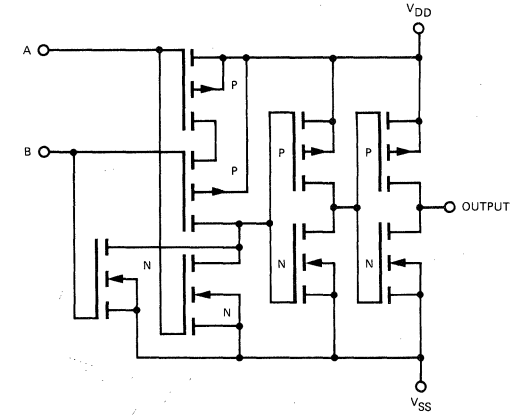


Fig. 1-4. FAIRCHILD 34001 FULLY BUFFERED NOR GATE

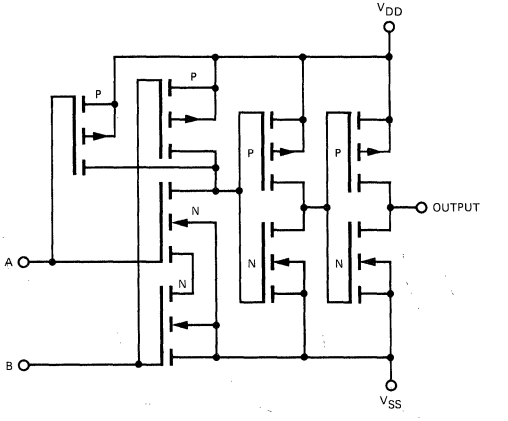


Fig. 1-5. FAIRCHILD 34011 FULLY BUFFERED NAND GATE

Fig. 1-6
COMPARISON OF PROPAGATION DELAY VS LOAD CAPACITANCE FOR CONVENTIONAL AND FULLY BUFFERED NAND GATES

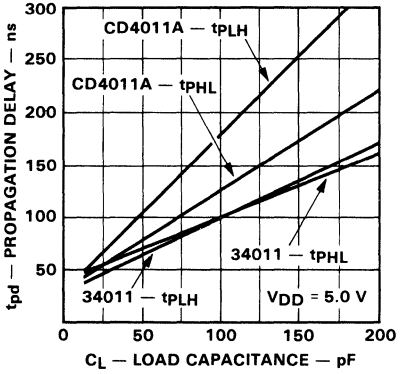


Fig. 1-7
TYPICAL VOLTAGE TRANSFER CHARACTERISTICS FOR CONVENTIONAL AND FULLY BUFFERED DEVICES

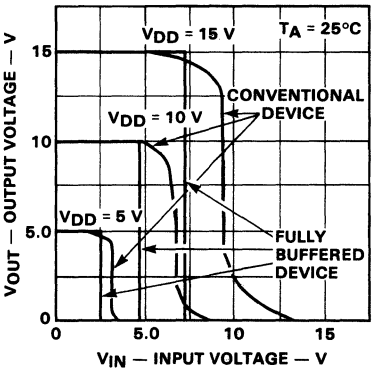


Fig. 1-8
POSITIVE-GOING INPUT RAMPS OF 0.1 μs AND 1.0 μs APPLIED TO CONVENTIONAL AND FULLY BUFFERED GATES

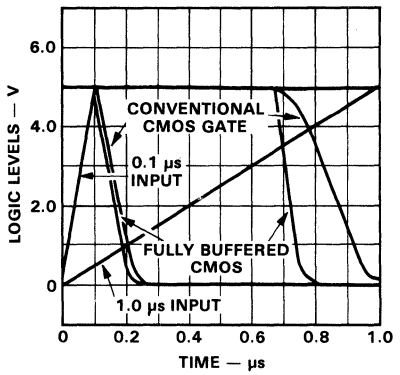
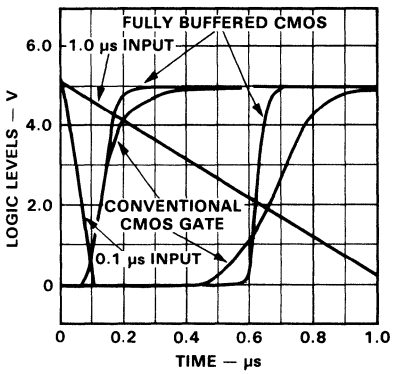
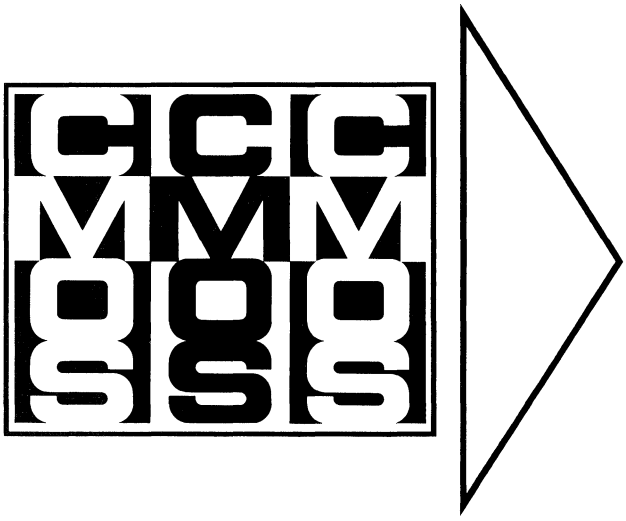


Fig. 1-9
NEGATIVE-GOING INPUT RAMPS OF 0.1 μs AND 1.0 μs APPLIED TO CONVENTIONAL AND FULLY BUFFERED GATES





DESIGN CONSIDERATIONS WITH 34000 SERIES CMOS

INTRODUCTION

Complementary MOS digital logic building blocks of SSI and MSI complexity have been hailed as the ideal logic family. They are rapidly gaining popularity as more and more manufacturers introduce increasing numbers of parts at reasonable prices.

Originally designed for aerospace applications, CMOS now finds its way into portable instruments, industrial and medical electronics, automotive applications and computer peripherals, besides dominating the electronic watch market.

In late 1973, Fairchild introduced the 34000 CMOS family, using Isoplanar technology to achieve superior electrical performance. Most of these devices are functional equivalents and pin-for-pin replacements of the well-known 4000 series; some are equivalent to TTL circuits and some are proprietary logic designs.

A few CMOS devices, such as bidirectional analog switches, exploit the unique features of CMOS technology; some take advantage of the smaller device size and higher potential packing density to achieve true LSI complexity; but most of the available CMOS elements today are of SSI and MSI complexity and perform logic functions that have been available in DTL or TTL for many years. Therefore, it is both helpful and practical to compare the performance of CMOS with that of the more familiar DTL/TTL *(Figure 2-1)*. The TTL to CMOS Comparison Guide in Section 3 lists numerous CMOS circuits that are pinout identical to their TTL counterparts, others that are functionally identical only, still others that are similar and, in most cases, offer added features.

CMOS speed is comparable to 74L-TTL and DTL, and about three to six times slower than TTL or Low Power Schottky (LS-TTL). Voltage noise immunity and fan out are almost ideal, supply voltage is noncritical, and the quiescent power consumption is close to zero-several orders of magnitude lower than for any competing technology.

POWER CONSUMPTION

Under static conditions, the p-channel (top) and the n-channel (bottom) transistors are not conducting simultaneously, thus only leakage current flows from the positive (V_{DD}) to the negative (V_{SS}) supply connection. This leakage current is typically 0.5 nA per gate, resulting in very attractive low power consumption of 2.5 nW per gate (at 5 V).

Whenever a CMOS circuit is exercised, when data or clock inputs change, additional power is consumed to charge and discharge capacitances (on-chip parasitic capacitances as well as load capacitances). Moreover, there is a short time during the transition when both the top and the bottom transistors are partially conducting. This dynamic power consumption is

	STANDARD TTL	74L	DTL	9LS LOW POWER SCHOTTKY	74LS LOW POWER SCHOTTKY	34000 CMOS 5 V SUPPLY	34000 CMOS 10 V SUPPLY
PROPAGATION DELAY	10 ns	33 ns	30 ns	5 ns	10 ns	35 ns	25 ns
FLIP-FLOP TOGGLE FREQUENCY	35 MHz	3 MHz	5 MHz	80 MHz	40 MHz	5 MHz	10 MHz
QUIESCENT POWER	10 mW	1 mW	8.5 mW	2 mW	2 mW	10 nW	10 nW
NOISE IMMUNITY	1 V	1 V	1 V	0.8 V	0.8 V	2 V	4 V
FAN OUT	10	10	8	20	20	50*	50*

*OR AS DETERMINED BY ALLOWABLE PROPAGATION DELAY

Fig. 2-1 CMOS COMPARED TO OTHER LOGIC FAMILIES

obviously proportional to the frequency at which the circuit is exercised, to the load capacitance and to the square of the supply voltage. As shown in *Figure 2-2,* the power consumption of a CMOS gate exceeds that of a Low Power Schottky gate somewhere between 500 kHz and 2 MHz of actual output frequency.

At 100 transitions per second, the dynamic power consumption is far greater than the static dissipation; at one million transitions per second, it exceeds the power consumption of LS-TTL. Comparing the power consumption of more complex devices (MSI) in various technologies may show a different result. In any complex design, only a small fraction of the gates actually switch at the full clock frequency, most gates operate at a much lower average rate and consume, therefore, much less power.

A realistic comparison of power consumption between different technologies involves a thorough analysis of the average switching speed of each gate in the circuit. The small static supply current, I_{DD} is specified on individual data sheets for 5, 10 and 15 V. The dynamic power dissipation for 5, 10 and 15 V, 15 and 50 pF may be found in graph form for frequencies of 100 Hz to 10 MHz. The total power may be calculated, $P_T = (I_{DD} \times V_{DD})$ + dynamic power dissipation.

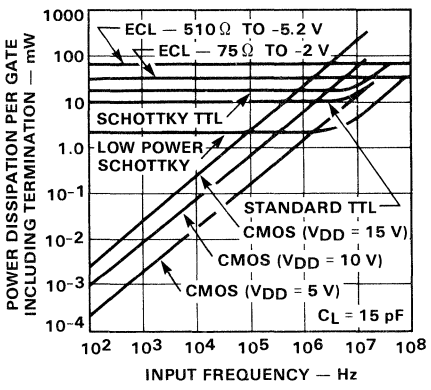
SUPPLY VOLTAGE RANGE

CMOS is guaranteed to function over the unprecedented range of 3 to 18 V supply voltage. Characteristics are guaranteed for 5, 10 and 15 V operation and can be extrapolated for any voltage in between. Operation below 4.5 V is not very meaningful because of the increase in delay (loss of speed), the increase in output impedance and the loss of noise immunity. Operation above 15 V is not recommended because of high dynamic power consumption and risk of noise spikes on the power supply exceeding the breakdown voltage (typ>20 V), causing SCR-latch-up and destroying the device unless the current is externally limited.

The lower limit of power supply voltage, including ripple, is determined by the required noise immunity, propagation delay or interface to TTL. The upper limit of supply voltage, including ripple and transients, is determined by power dissipation or direct interface to TTL. The 34049, 34050 and 34104 provide level translation between TTL and CMOS when CMOS supply voltages over 5 V are used. While devices are usable to 18 V, operation above 12 V is discouraged for reasons of power dissipation.

Low static power consumption combined with wide supply voltage range make CMOS the ideal logic family for battery operated equipment.

Fig. 2-2
TYPICAL POWER DISSIPATION VERSUS INPUT FREQUENCY FOR SEVERAL POPULAR LOGIC FAMILIES



PROPAGATION DELAY

Compared to TTL and LS-TTL, all CMOS devices are slow and very sensitive to capacitive loading. See *Figure 2-3.* The Fairchild 34000 family uses both advanced processing (Isoplanar) and improved circuit design (buffered gates) to achieve propagation delays and output rise times that are superior to any other junction-isolated CMOS design. (Silicon-on-sapphire, SOS, can achieve similar performance but at a substantial cost penalty).

Isoplanar processing achieves lower parasitic capacitances which reduce the on-chip delay and increase the maximum toggle frequency of flip-flops, registers and counters. Buffering all outputs, even on gates, results in lower output impedance and thus reduces the effect of capacitive loading.

Propagation delay is affected by three parameters: capacitive loading, supply voltage, and temperature.

Capacitive Loading Effect

Historically, semiconductor manufacturers have always specified the propagation delay at an output load of 15 pF, not because anybody considers this a representative systems environment, but rather because it was the lowest practical test-jig capacitance. It also generated the most impressive specifications. TTL with an output impedance less than 100 Ω is little affected by an increase in capacitive loading; a 100 pF load increases the delay by only about 4 ns. CMOS, however, with an output impedance of 1 kΩ (worst case at 5 V) is 10 times more sensitive to capacitive loading. *Figure 2-4* shows the positive- and negative-going delays as a function of load capacitance. It should be noted that the older, unbuffered gates have an even higher output impedance, a larger dependence on output loading, and do not show the same symmetry.

Fig. 2-3
NORMALIZED PROPAGATION DELAY VERSUS LOAD CAPACITANCE FOR TTL AND CMOS

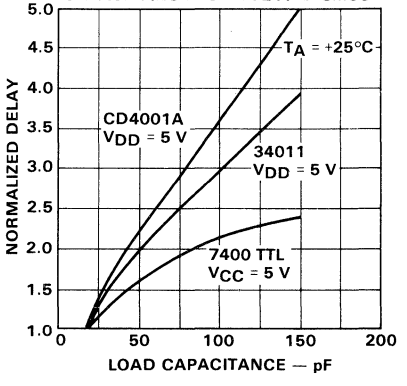


Fig. 2-4a
POSITIVE-GOING PROPAGATION DELAY VERSUS LOAD CAPACITANCE

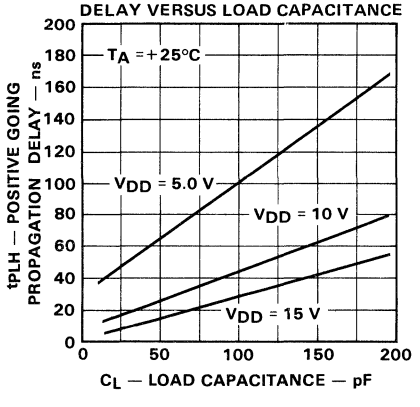
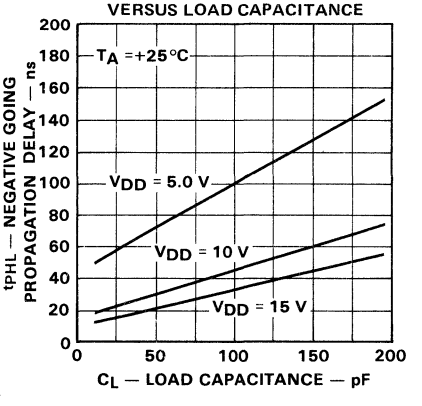


Fig. 2-4b
NEGATIVE-GOING PROPAGATION DELAY VERSUS LOAD CAPACITANCE



Supply Voltage Effect

Figure 2-5 shows propagation delay as a function of supply voltage and again indicates the symmetry of the positive- and negative-going delays. Increasing the supply voltage from 5 to 10 V more than doubles the speed of CMOS gates. Increasing the supply voltage to 15 V almost doubles the speed again, but, as mentioned before, results in a significant increase in dynamic power dissipation.

The best choice for slow applications is 5 V. For reasonably fast systems, choose 10 or 12 V. Any application requiring 15 V to achieve short delays and fast operation should be investigated for excessive power dissipation and should be weighed against an LS-TTL approach.

Fig. 2-5a
POSITIVE-GOING PROPAGATION DELAY VERSUS POWER SUPPLY VOLTAGE

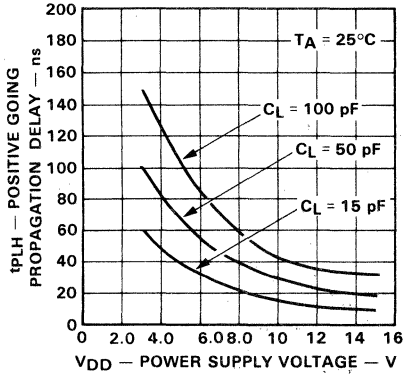
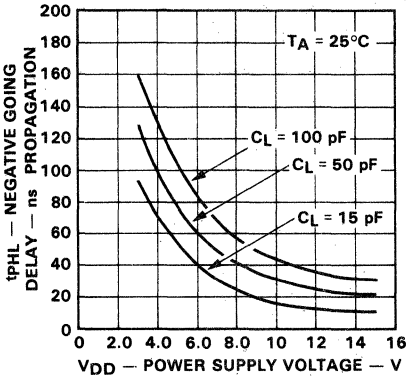


Fig. 2-5b
NEGATIVE-GOING PROPAGATION DELAY VERSUS POWER SUPPLY VOLTAGE



Temperature Effect

Figure 2-6 shows propagation delay as a function of ambient temperature. The temperature dependence of CMOS is much simpler than with TTL, where three factors contribute—increase of beta with temperature, increase of resistor value with temperature, and decrease of junction forward voltage drop with increasing temperature. In CMOS, essentially only the carrier mobility changes, thus increasing the impedance and hence the delay with temperature. For 34000 devices, this temperature dependence is less than 0.3% per °C, practically linear over the full temperature range. Note that the commercial temperature range is –40 to +85°C rather than the usual 0 to +75°C.

Fig. 2-6a
PROPAGATION DELAY VERSUS AMBIENT TEMPERATURE WITH V_{DD} = 5 V

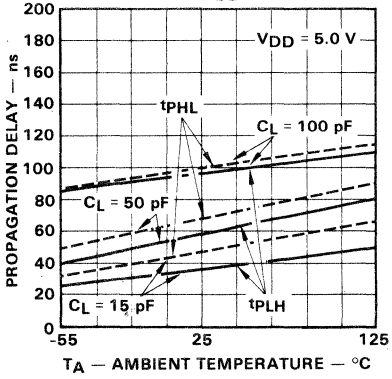
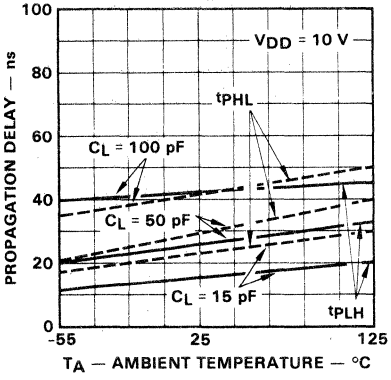


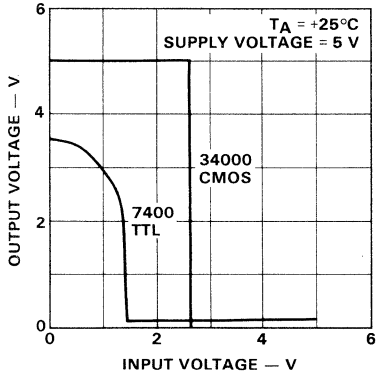
Fig. 2-6b
PROPAGATION DELAY VERSUS AMBIENT TEMPERATURE WITH V_{DD} = 10 V



CMOS delays increase with temperature. They are very sensitive to capacitive loading but can be reduced by increasing the supply voltage to 10 or even 15 V.

To determine propagation delays, the effects of capacitive loading, supply voltage, manufacturing tolerances and ambient temperature must be considered. Start with the values of t_{PLH} (propagation delay, a LOW-to-HIGH output transition) and t_{PHL} (propagation delay, a HIGH-to-LOW output transition) given in the individual data sheets. Delay values for V_{DD} at 5, 10 and 15 V and output capacity of 15 and 50 pF are provided. Manufacturing tolerances account for the differences between MIN, TYP and MAX. Starting with the nearest applicable delay value, correct for effects of capacitive loading, ambient temperature and supply voltage using the general family characteristics of Section 3.

Fig. 2-7
TYPICAL TRANSFER CHARACTERISTICS FOR TTL AND CMOS



NOISE IMMUNITY

One of the most advertised and also misunderstood CMOS features is noise immunity. The input threshold of a CMOS gate is approximately 50% of the supply voltage and the voltage transfer curve is almost ideal. As a result, CMOS can claim very good voltage noise immunity, typically 40% of the supply voltage, *i.e.,* 2 V in a 5 V system, 4 V in a 10 V system. Compare this with the TTL transfer curve in *Figure 2-7* and its resultant 1 V noise immunity in a lightly loaded system and only 0.4 V worst case.

Since CMOS output impedance, output voltage and input threshold are symmetrical with respect to the supply voltage, the LOW and HIGH level noise immunities are practically equal. Therefore, a CMOS system can tolerate ground or V_{DD} drops and noise on these supply lines of more than 1 V, even in a 5 V system. Moreover, the inherent CMOS delays act as a noise filter; 10 ns spikes tend to disappear in a chain of CMOS gates, but are amplified in a chain of TTL gates. Because of these features, CMOS is very popular with designers of industrial control equipment that must operate in an electrically and electromagnetically "polluted" environment.

Unfortunately these impressive noise margin specifications disregard one important fact: the output impedance of CMOS is 10 to 100 times higher than that of TTL. CMOS interconnections are therfore less "stiff" and much more susceptible to capacitively coupled noise. In terms of such current injected crosstalk from high noise voltages through small coupling capacitances, CMOS has about six times *less* noise margin than TTL. It takes more than 20 mA to pull a TTL output into the threshold region, but it takes only 3 mA to pull a CMOS output into the threshold of a 5 V system.

The nearly ideal transfer characteristic and the slow response of CMOS circuits make them insensitive to low voltage, magnetically coupled noise. The high output impedance, however, results in a poor rejection of capacitively coupled noise.

INTERFACE TO TTL

When CMOS is operated with a 5 V power supply, interface to TTL is straightforward. The input impedance of CMOS is very high, so that any form of TTL will drive CMOS without loss of fan out in the LOW state. Unfortunately, most TTL has insufficient HIGH state voltage (typically 3.5 V) to drive CMOS reliably. A pull up resistor (1 kΩ to 10 kΩ) from the output of the TTL device to the 5 V power supply will effectively pull the HIGH state level to 4.5 V or above. Alternately, DTL Hex inverters may be used between the TTL and CMOS. 9LS Low Power Schottky and 93L00 Low Power TTL/MSI utilize the unique output configuration shown in *Figure 2-8* to pull its output to V_{CC}–V_{BC} or approximately 4.3 V when lightly loaded.

All 34000 logic elements will drive a single 9LS Low Power Schottky input fan in directly. A 9LS Hex inverter such as the 9LS04 makes an excellent low cost TTL buffer with a fan out of 20 into 9LS or 5 into standard TTL. Alternately, the 34049 and 34050 Hex buffers may be used to drive a fan out of 8 into 9LS or 2 into standard TTL.

When operating CMOS at voltages higher than 5 V direct interface to TTL cannot be used. The 34104 Quad Level Translator converts TTL levels to high voltage CMOS up to 15 V. The 34049 and 34050 Hex Buffers will accept high voltage CMOS levels up to 15 V and drive 2 standard TTL loads.

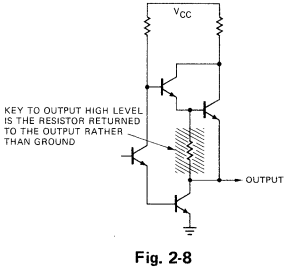


Fig. 2-8
THE 93L00 AND 9LS00 TTL FAMILIES WILL DRIVE CMOS DIRECTLY WITHOUT RESISTORS AS LONG AS THERE ARE ONLY CMOS DEVICES BEING DRIVEN FROM THE OUTPUT.

INPUT/OUTPUT CAPACITY

CMOS devices exhibit input capacities in the 1.5 to 5 pF range and output capacity in the 3 to 7 pF range.

OUTPUT IMPEDANCE

All 34000 logic devices employ standardized output buffers. Section 3 details output characteristics. It should be noted that these impedances do not change with input pattern as do conventional CMOS gates. Buffers, analog switches and analog multiplexers employ special output configurations which are detailed in individual data sheets.

INPUT PROTECTION

The gate input to any MOS transistor appears like a small (<1 pF) very low leakage ($<10^{-12}$ A) capacitor. Without special precautions, these inputs could be electrostatically charged to a high voltage, causing a destructive breakdown of the dielectric and permanently damaging the device. Therefore, all CMOS inputs are protected by a combination of series resistor and shunt diodes. Various manufacturers have used different approaches; some use a single diode, others use two diodes, and some use a resistor with a parasitic substrate diode.

Each member of the 34000 family utilizes a series resistor, nominally 200 Ω, and two diodes, one to V_{DD}, and the other to V_{SS} *(Figure 2-9)*. The resistor is a poly-silicon "true resistor" without a parasitic substrate diode. This ensures that the input impedance is always at least 200 Ω under all biasing conditions, even when V_{DD} is short circuited to V_{SS} (selective power-down). A parasitic substrate diode would represent a poorly defined shunt to V_{SS} in this particular case.

The diodes exhibit typical forward voltage drops of 0.9 V at 1 mA and reverse breakdowns of 20 V for D1 and 26 V for D2. For certain special applications such as oscillators, the diodes actually conduct during normal operation. However, currents must be limited to 10 mA.

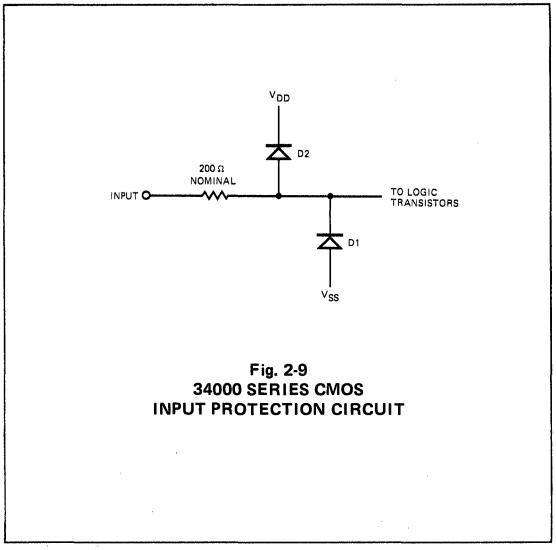


Fig. 2-9
34000 SERIES CMOS
INPUT PROTECTION CIRCUIT

HANDLING PRECAUTIONS

All MOS devices are subject to damage by large electrostatic charges. All 34000 devices employ the input protection described in *Figure 2.9*, however, electrostatic damage can still occur. The following handling precautions should be observed.

1. All 34000 devices are shipped in conducting foam or tubes. They should be removed for inspection or assembly using proper precautions.
2. Ionized air blowers are recommended when automatic incoming inspection is performed.
3. 34000 devices, after removal from their shipping material, should be placed leads down on a grounded surface. Conventional cookie tins work well. Under no circumstances should they be placed in polystyrene foam or plastic trays used for shipment and handling of conventional ICs.
4. Individuals and tools should be grounded before coming in contact with 34000 devices.
5. Do not insert or remove devices in sockets with power applied. Ensure power supply transients, such as occur during power turn-on or off; do not exceed maximum ratings.
6. In the system, all unused inputs must be connected to either a logic HIGH or logic LOW level such as V_{SS}, V_{DD} or the output of a logic element.
7. After assembly on PC boards, ensure that static discharge cannot occur during storage or maintenance. Boards may be stored with their connectors surrounded with conductive foam. Board input/output pins may be protected with large value resistors (10 MΩ) to ground.
8. In extremely hostile environments, an additional series input resistor (10 to 100 kΩ) provides even better protection at a slight speed penalty.

A WORD TO THE TTL DESIGNER

Designing with CMOS is generally an easy transition and allows the designer to discard many of the old design inhibitions for new found freedoms. A few of these are:

Fan out—It is practically unlimited from a dc point of view and is restricted only by delay and rise time considerations.

Power Supply Regulation—Anything between 3 V and 15 V goes, as long as all communicating circuits are fed from the same voltage.

Ground and V_{CC} Line Drops—The currents are normally so small that there is no need for heavy supply line bussing.

V_{CC} Decoupling—It can be reduced to a few capacitors per board.

Heat Problems—They do not exist, unless an attempt is made to run CMOS very fast and from more than 10 V.

It should also be noted that there are a few warnings called for when designing with CMOS and that many of the hard-earned good engineering basics cannot be forgotten. A few of the new design challenges include:

Unused Inputs—They must be connected to V_{SS} or V_{DD} (V_{CC} or ground) lest they generate a logical "maybe". The bad TTL habit of leaving unused inputs open is definitely out.

Oscillations—Slowly rising or falling input signals can lead to oscillations and multiple triggering. A poorly regulated and decoupled power supply magnifies this problem since the CMOS input threshold varies with the supply voltage.

Timing Details—Even slow systems require a careful analysis of worst case timing delays, derated for maximum temperature, minimum supply voltage and maximum capacitive loading. Many CMOS flip-flops, registers and latches have a real hold time requirement, *i.e.*, inputs must remain stable even after the active clock edge; some require a minimum clock rise time. This hasn't been a problem with TTL. CMOS systems, even slow ones, are prone to unsuspected clock skew problems, especially since a heavily loaded clock generator can have a poor rise time.

Compatibility—The TTL designer knows that devices sold by different manufacturers under the same generic part number are electrically almost identical. The same electrical compatibility is not yet achieved in CMOS. Many semiconductor houses manufacture 4000-type devices with wide variations in output drive capability and speed. Sometimes even the functions are different and incompatible; two cases in point are the 1-of-10 decoder (CD4028A and MC14028) and the magnitude comparator (MC14585 and MM74C85).

Data Sheet Format—The original CD4000 series data sheets may appear confusing to the TTL user because a range of input voltage requirements is not specified. Rather, this information is contained in a "noise immunity" specification and is not immediately obvious.

Both TTL and CMOS tolerate deviations from the ideal LOW and HIGH input voltages. TTL is therefore specified as follows:

	MIN	MAX	
V_{IH}	2.0		V
V_{IL}		0.8	V

Any voltage below 0.8 V is considered LOW; any voltage above +2.0 V is considered HIGH. The actual threshold is somewhere in between these values, depending on manufacturing tolerances, supply voltage, and temperature.

Fairchild's 34000 CMOS is specified in a similar way. For $V_{DD} = 5$ V;

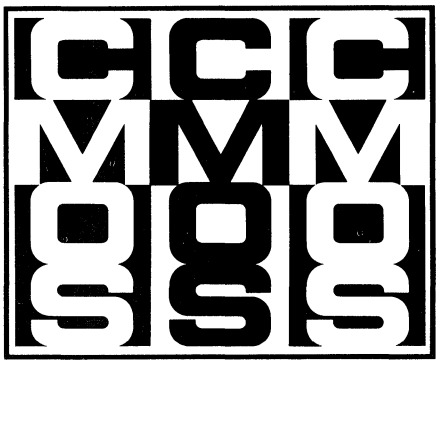
	MIN	MAX	
V_{IH}	3.5		V
V_{IL}		1.5	V

The CD4000 data sheets, on the other hand, do not call out V_{IH} and V_{IL} but specify a "noise immunity" which is somewhat arbitrarily defined relative to the appropriate supply voltage.

$$V_{NL} = V_{IL}$$
$$V_{NH} = V_{DD} - V_{IH}$$

For $V_{DD} = 5$ V, therefore
$V_{NL} = 1.5$ V min is equivalent to $V_{IL} = 1.5$ V max
$V_{NH} = 1.4$ V min is equivalent to $V_{IH} = 3.6$ V min, etc.

Systems Oriented MSI—Available CMOS circuits, especially the original 4000 series, are not as well suited for synchronous systems as are the 9300/7400 TTL families. Control polarities are inconsistent; many circuits cannot be cascaded or extended synchronously without additional gates, etc. This will improve as more good synchronous building blocks, like the 340160 are introduced.



NUMERICAL INDEX OF DEVICES

NUMERICAL INDEX OF DEVICES

SELECTOR GUIDE BY FUNCTION

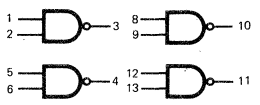
SELECTOR GUIDE BY FUNCTION

TTL TO CMOS FUNCTION SELECTOR GUIDE

TTL	FUNCTION	CMOS	FUNCTIONAL DIFFERENCES BETWEEN CMOS AND TTL	PAGE NO.
			NAND GATES	
7400 9002	Quad 2-Input NAND Gate	34011	Different Pinout, Functionally Identical	3-25
7410 9003	Triple 3-Input NAND Gate	34023	Different Pinout, Functionally Identical	3-48
7420 9004	Dual 4-Input NAND Gate	34012	Different Pinout, Functionally Identical	3-25
7430 9007	8-Input NAND Gate	34068	Different Pinout, Functionally Identical	3-85
			AND GATES	
7408	Quad 2-Input AND Gate	34081	Different Pinout, Functionally Identical	3-92
			NOR GATES	
7402	Quad 2-Input NOR Gate	34001	Different Pinout, Functionally Identical	3-23
7427	Triple 3-Input NOR Gate	34025	Different Pinout, Functionally Identical	3-52
7425	Dual 4-Input NOR Gate	34002	Different Pinout. The 7425 has a Strobe input on each gate; the 34002 does not.	3-23
	8-Input NOR Gate	34078	No TTL Equivalent	3-91
			OR GATES	
7432	Quad 2-Input OR Gate	34071	Different Pinout, Functionally Identical	3-89
			INVERTERS AND BUFFERS	
7404 9016	Hex Inverter	34069	Same Pinout, Functionally Identical	3-86
7416 7404 9016	Hex Buffer, Inverting	34049	Different Pinout. The 34049 has an active pull-up and pull-down output. The 7416 has an open collector output. The 7404 and 9016 have an active pull-up and pull-down output.	3-73
7417	Hex Buffer, Non-Inverting	34050	Different Pinout. The 34050 has an active pull-up and pull-down output. The 7417 has an open collector output.	3-73
74367 8097	Hex Buffer, Non-Inverting, 3-State Outputs	340097	Same Pinout, Functionally Identical	3-136
74368 8098	Hex Buffer, Inverting, 3-State Outputs	340098	Same Pinout, Functionally Identical	3-136
			COMPLEX GATES	
74L86	Quad Exclusive-OR Gate	34030/ 34070	Same Pinout, Functionally Identical	3-63,3-88
74LS266	Quad Exclusive-NOR Gate	34077	Same Pinout, Functionally Identical	3-90
7450 9005	Dual 2-Wide, 2-Input AND-OR-INVERT Gate	34085	Different Pinout. The 34085 has an extra input which can be used as either an expander input or an inhibit input by connecting it to any standard CMOS output. Only one-half of a 7450 and 9005 can be expanded by connecting it to a special expander circuit. The 7450 and 9005 do not have an inhibit capability.	3-93

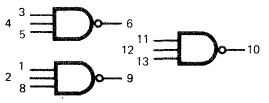
TTL TO CMOS FUNCTION SELECTOR GUIDE

34011



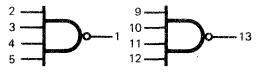
V_{DD} = Pin 14
V_{SS} = Pin 7

34023



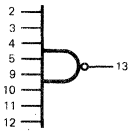
V_{DD} = Pin 14
V_{SS} = Pin 7

34012



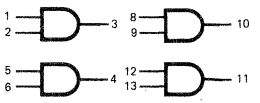
V_{DD} = Pin 14
V_{SS} = Pin 7
NC = Pins 6, 8

34068



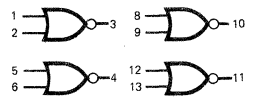
V_{DD} = Pin 14
V_{SS} = Pin 7
NC = Pins 1, 6, 8

34081



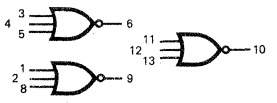
V_{DD} = Pin 14
V_{SS} = Pin 7

34001



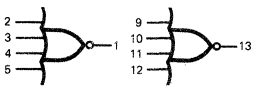
V_{DD} = Pin 14
V_{SS} = Pin 7

34025



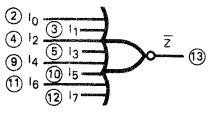
V_{DD} = Pin 14
V_{SS} = Pin 7

34002



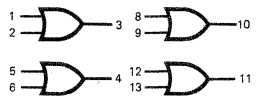
V_{DD} = Pin 14
V_{SS} = Pin 7
NC = Pins 6, 8

34078



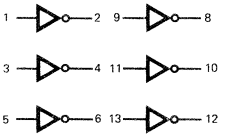
V_{DD} = Pin 14
V_{SS} = Pin 7
NC = Pins 1, 6, 8

34071



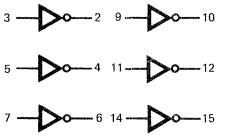
V_{DD} = Pin 14
V_{SS} = Pin 7

34069



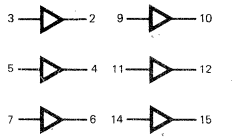
V_{DD} = Pin 14
V_{SS} = Pin 7

34049



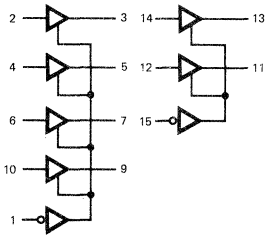
V_{DD} = Pin 1
V_{SS} = Pin 8
NC = Pins 13, 16

34050



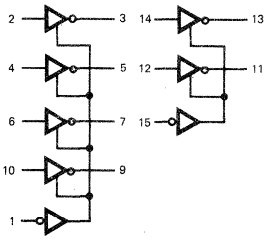
V_{DD} = Pin 1
V_{SS} = Pin 8
NC = Pins 13, 16

340097



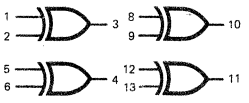
V_{DD} = Pin 16
V_{SS} = Pin 8

340098



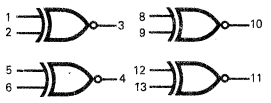
V_{DD} = Pin 16
V_{SS} = Pin 8

34030 AND 34070



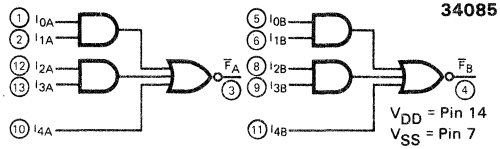
V_{DD} = Pin 14
V_{SS} = Pin 7

34077



V_{DD} = Pin 14
V_{SS} = Pin 7

34085



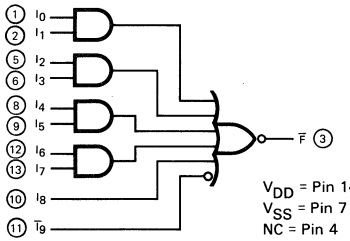
V_{DD} = Pin 14
V_{SS} = Pin 7

TTL TO CMOS FUNCTION SELECTOR GUIDE

TTL	FUNCTION	CMOS	FUNCTIONAL DIFFERENCES BETWEEN CMOS AND TTL	PAGE NO.
			COMPLEX GATES (Cont'd)	
7453	4-Wide, 2-Input AND-OR-INVERT Gate	34086	Different Pinout. The 34086 has two additional inputs which can be used as either expander inputs or inhibit inputs by connecting them to any standard CMOS output. The 7453 can be expanded only by connecting it to a special expander circuit. The 7453 does not have an inhibit capability.	3-95
			FLIP-FLOPS	
7474	Dual D Flip-Flop	34013	Different Pinout. The 7474 has active LOW S_D and C_D inputs; the 34013 has active HIGH S_D and C_D inputs.	3-27
74109 9024	Dual JK Flip-Flop, Edge-Triggered	34027	Different Pinout. The 7474 has active LOW S_D and C_D inputs; the 34013 has the 34027 has active HIGH S_D, C_D and K inputs.	3-53
74175	Quad D Flip-Flop	340175	Same Pinout, Functionally Identical	3-148
74174	Hex D Flip-Flop	340174	Same Pinout, Functionally Identical	3-145
			COUNTERS	
93S10 9310 74160	Synchronous, BCD Up Counter, Asynchronous Master Reset	340160	Same Pinout. The 340160 and 93S10 are fully edge-triggered. The 74160 and 9310 are "opposite state catching" on the Count Enable and Parallel Enable inputs. The Terminal Count is fully decoded on the 340160, 9310 and 93S10 ($TC = CET \bullet Q_0 \bullet \overline{Q_1} \bullet \overline{Q_2} \bullet Q_3$) but is not fully decoded on the 74160 ($TC = CET \bullet Q_0 \bullet Q_3$). For the count sequence above 9, the 340160 is the same as the 74160, different than the 9310 and 93S10.	3-139
93S16 9316 74161	Synchronous, Binary Up Counter, Asynchronous Master Reset	340161	Same Pinout. The 340161 is fully edge-triggered; the 74161 and 9316 are "opposite state catching" on the Count Enable and Parallel Enable inputs. The 340161 is functionally identical to the 93S16.	3-139
74162	Synchronous, BCD Up Counter, Synchronous Reset	340162	Same Pinout. The 340162 is fully edge-triggered and the Terminal Count is fully decoded ($TC = CET \bullet Q_0 \bullet \overline{Q_1} \bullet \overline{Q_2} \bullet Q_3$); the 74162 is "opposite state catching" on the Count Enable, Parallel Enable and Synchronous Reset inputs and the Terminal Count is not fully decoded ($TC = CET \bullet Q_0 \bullet Q_3$).	3-139
74163	Synchronous Binary Up Counter, Synchronous Reset	340163	Same Pinout. The 340163 is fully edge-triggered; the 74163 is "opposite state catching" on the Count Enable, Parallel Enable and Synchronous Reset inputs.	3-139
74490	Dual BCD Up Counter	34518	Different Pinout. The 34518 has two clock inputs per counter and is fully synchronous internally. The 74490 has a single clock input per counter, has a "set to nine" input and is a ripple counter internally.	3-107
74393	Dual Binary Up Counter	34520	Different Pinout. The 34520 has two clock inputs per counter and is fully synchronous internally. The 74393 has a single clock input per counter and is internally organized as a ripple counter.	3-107
	Synchronous, Binary/ Decade, Up/Down Counter	34029	No TTL Equivalent	3-58
74192	BCD, Up/Down Counter	340192	Same Pinout. The $\overline{TC_u}$ is fully decoded on the 340192 ($TC_u = Q_0 \bullet \overline{Q_1} \bullet \overline{Q_2} \bullet Q_3 \bullet \overline{CP_u}$); on the 74192 $\overline{TC_u}$ is not fully decoded ($TC_u = Q_0 \bullet Q_3 \bullet \overline{CP_u}$).	3-150
74193	Binary, Up/Down Counter	340193	Same Pinout, Functionally Identical	3-150
74142	Divide-by-10 Counter with Decoded Outputs	34017	Different Pinout. The 74142 is a BCD Counter/Latch/Decoder. The decoded outputs are active LOW and can have decoding spikes. The 34017 is a 5-stage Johnson decade counter with active HIGH, glitchless decoded outputs.	3-38
74393	7-Stage Binary Counter	34024	Different Pinout. The 74393, a dual 4-bit counter, can be connected as a 7-stage counter.	3-49

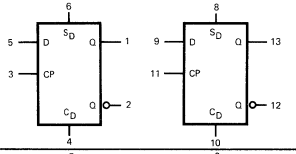
TTL TO CMOS FUNCTION SELECTOR GUIDE

34086



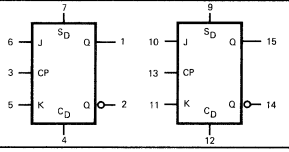
V_{DD} = Pin 14
V_{SS} = Pin 7
NC = Pin 4

34013



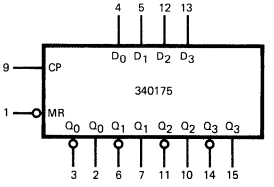
V_{DD} = Pin 14
V_{SS} = Pin 7

34027



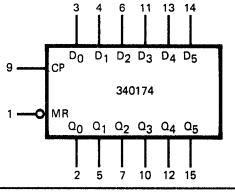
V_{DD} = Pin 16
V_{SS} = Pin 8

340175



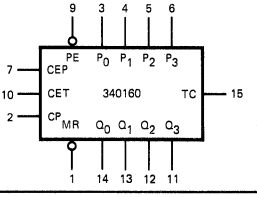
V_{DD} = Pin 16
V_{SS} = Pin 8

340174



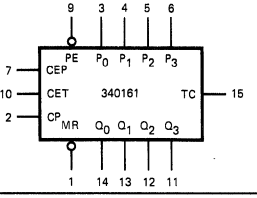
V_{DD} = Pin 16
V_{SS} = Pin 8

340160



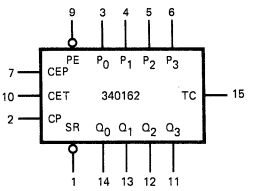
V_{DD} = Pin 16
V_{SS} = Pin 8

340161



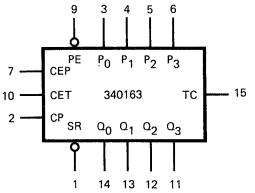
V_{DD} = Pin 16
V_{SS} = Pin 8

340162



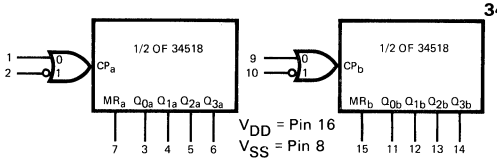
V_{DD} = Pin 16
V_{SS} = Pin 8

340163



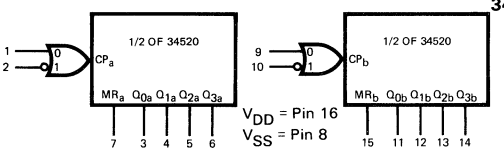
V_{DD} = Pin 16
V_{SS} = Pin 8

34518



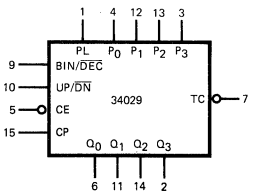
V_{DD} = Pin 16
V_{SS} = Pin 8

34520



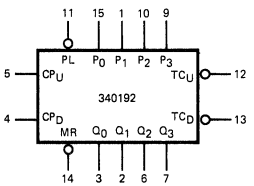
V_{DD} = Pin 16
V_{SS} = Pin 8

34029



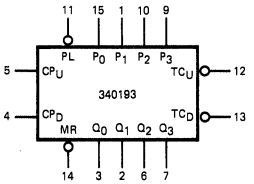
V_{DD} = Pin 16
V_{SS} = Pin 8

340192



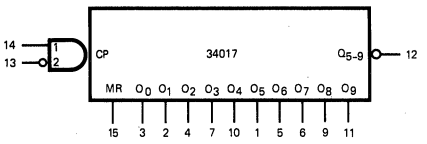
V_{DD} = Pin 16
V_{SS} = Pin 8

340193



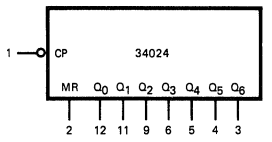
V_{DD} = Pin 16
V_{SS} = Pin 8

34017



V_{DD} = Pin 16
V_{SS} = Pin 8

34024



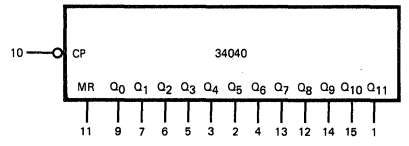
V_{DD} = Pin 14
V_{SS} = Pin 7
NC = Pins 8, 10, 13

TTL TO CMOS FUNCTION SELECTOR GUIDE

TTL	FUNCTION	CMOS	FUNCTIONAL DIFFERENCES BETWEEN CMOS AND TTL	PAGE NO.
			COUNTERS (Cont'd)	
	12-Stage Binary Counter	34040	No TTL Equivalent	3-67
	14-Stage Binary Counter	34020	No TTL Equivalent	3-43
			REGISTERS	
74195 9300	4-Bit Shift Register,	340195	Same Pinout, Functionally Identical	3-159
74LS194	4-Bit Shift Register; Shift Left, Shift Right, Parallel Load and Hold Modes	340194	Same Pinout, Functionally Identical	3-154
74195 9300	4-Bit Shift Register, SI/PI/SO/PO, Output Polarity Control	34035	Different Pinout. The 34035 has an output polarity control and active HIGH Parallel Enable and Master Reset inputs. The 74195 and 9300 do not have output polarity control but they give both the true and complement of Q_3. They have active LOW Parallel Enable and Master Reset inputs.	3-64
	Dual 4-Bit Shift Register, SI/SO/PO	34015	No TTL Equivalent	3-32
74166	8-Bit Shift Register, SI/PI/SO	34014	Different Pinout. The 74166 has two Clock inputs and a Master Reset input. It does not have the Q_5 and Q_6 outputs available. The Parallel Enable input is active LOW. The 34014 has a single Clock input and does not have a Master Reset input. It has the Q_5 and Q_6 outputs available. The Parallel Enable input is active HIGH.	3-30
74165	8-Bit Shift Register, SI/PI/SO	34021	Different Pinout. The 74165 has two Clock inputs and a $\overline{Q_7}$ output. It does not have the Q_5 and Q_6 outputs available. The Parallel Load input is active LOW. The 34021 has a single Clock input and does not have a $\overline{Q_7}$ output. It has the Q_5 and Q_6 outputs available. The Parallel Load input is active HIGH.	3-46
			DECODERS	
74LS139 9321	Dual 1-of-4 Decoder, Active LOW Outputs	34556	Same Pinout, Functionally Identical	3-112
74LS139 9321	Dual 1-of-4 Decoder, Active HIGH Outputs	34555	Same Pinout. The outputs of the 34555 are the complement of the outputs of the 74LS139 and 9321.	3-112
7442A 9301	1-of-10 Decoder, Active HIGH Outputs	34028	Different Pinout. For input codes 0–9, the outputs of the 34028 are the complements of the outputs of the 7442A and 9301. For input codes 10–15, all outputs of the 7442A and the 9301 are HIGH. On the 34028, input codes 10, 12 and 14 generate a HIGH on O_8, a LOW on all other outputs, while input codes 11, 13 and 15 generate a HIGH on O_9, a LOW on all other outputs.	3-56
			MULTIPLEXERS	
74157 9322	Quad AND-OR Select Gate (Quad 2-Input Multiplexer)	34019	Different Pinout. The 34019 has two Select inputs which allow the choice of four possible outputs: O, A, B, A+B. The 74157 and 9322 have a single Select input which allows the selection of either A or B inputs, and an active LOW Enable input.	3-41
74153	Dual 4-Input Multiplexer	34539	Same Pinout, Functionally Identical	3-110
74251	8-Input Multiplexer 3-State Outputs	34512	Different Pinout. The 34512 has an Enable input which forces all outputs LOW, but it does not have a $\overline{Z}$ output. The 74251 does not have an Enable input, but has both Z and $\overline{Z}$ outputs.	3-103
(74151 9312)			The 74151 and 9312 do not have 3-state outputs; they provide the $\overline{Z}$ output in lieu of the Output Enable input. The 34512 can perform the same function as the 74151 and 9312.	

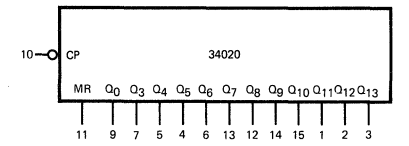
TTL TO CMOS FUNCTION SELECTOR GUIDE

34040



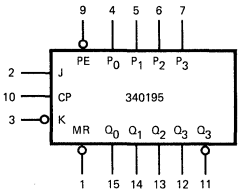
V_{DD} = Pin 16
V_{SS} = Pin 8

34020



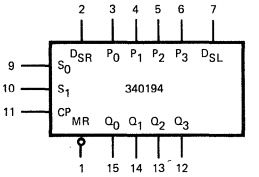
V_{DD} = Pin 16
V_{SS} = Pin 8

340195



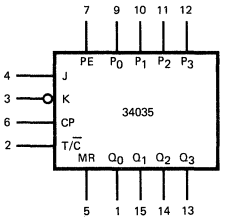
V_{DD} = Pin 16
V_{SS} = Pin 8

340194



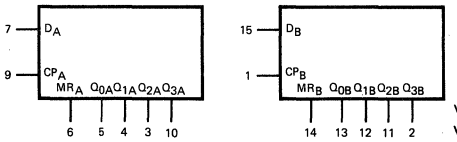
V_{DD} = Pin 16
V_{SS} = Pin 8

34035



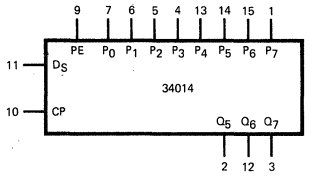
V_{DD} = Pin 16
V_{SS} = Pin 8

34015



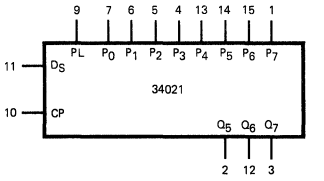
V_{DD} = Pin 16
V_{SS} = Pin 8

34014



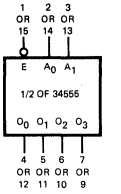
V_{DD} = Pin 16
V_{SS} = Pin 8

34021



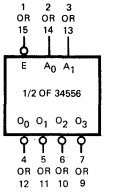
V_{DD} = Pin 16
V_{SS} = Pin 8

34555



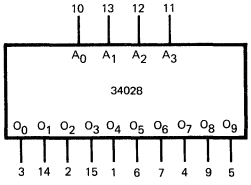
V_{DD} = Pin 16
V_{SS} = Pin 8

34556



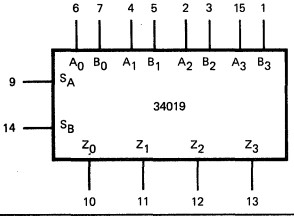
V_{DD} = Pin 16
V_{SS} = Pin 8

34028



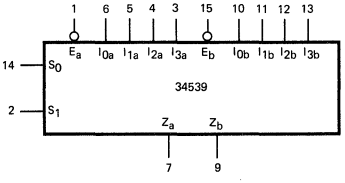
V_{DD} = Pin 16
V_{SS} = Pin 8

34019



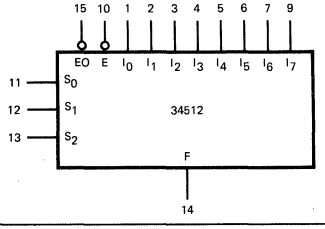
V_{DD} = Pin 16
V_{SS} = Pin 8

34539



V_{DD} = Pin 16
V_{SS} = Pin 8

34512



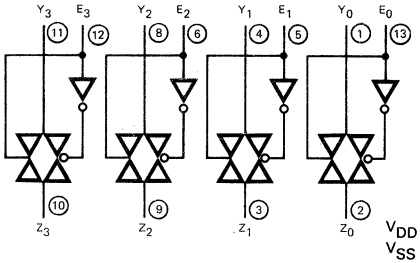
V_{DD} = Pin 16
V_{SS} = Pin 8

TTL TO CMOS FUNCTION SELECTOR GUIDE

TTL	FUNCTION	CMOS	FUNCTIONAL DIFFERENCES BETWEEN CMOS AND TTL	PAGE NO.
			MULTIPLEXERS	
74157 9322	Quad AND-OR Select Gate (Quad 2-Input Multiplexer)	34019	Different Pinout. The 34019 has two Select inputs which allow the choice of four possible outputs: 0, A, B, A+B. The 74157 and 9322 have a single Select input which allows the selection of either A or B inputs, and an active LOW Enable input.	3-41
74153	Dual 4-Input Multiplexer	34539	Same Pinout, Functionally Identical	3-110
74251	8-Input Multiplexer 3-State Outputs	34512	Different Pinout. The 34512 has an Enable input which forces all outputs LOW, but it does not have a Z output. The 74251 does not have an Enable input, but has both Z and Z outputs.	3-103
(74151 9312)			The 74151 and 9312 do not have 3-state outputs; they provide the Z output in lieu of the Output Enable input. The 34512 can perform the same function as the 74151 and 9312.	
			ANALOG SWITCHES AND MULTIPLEXERS/DEMULTIPLEXERS	
	Quad Bilateral Switch	34016/ 34066	No TTL Equivalent. The 34016 and 34066 are "analog" switches.	3-35,3-82
(74151 9312)	8-Channel Analog Multiplexer/Demultiplexer	34051	No TTL Equivalent. The 34051 can be used as a digital circuit to perform the same function as the 74151 and 9312. The 34051 in an "analog" multiplexer/demultiplexer.	3-76
(9309)	Dual 4-Channel Analog Multiplexer/Demultiplexer	34052	No TTL Equivalent. The 34052 can be used as a digital circuit to perform the same function as the 9309. The 34052 is an "analog" multiplexer/demultiplexer.	3-79
			LATCHES	
7475	4-Bit Latch	34042	Different Pinout. The 7475 has separate Enable inputs for bits, 0 1 and 2,3. The 34042 has a Common Enable input for all four bits; but with the Exclusive-NOR Enable inputs, it is possible to have either an active HIGH or an active LOW Enable input.	3-70
9334 74259	8-Bit Addressable Latch	34099	Same Pinout. The 9334 and 74259 have active LOW Clear inputs, the 34099 has an active HIGH Clear input.	3-97
	Dual 4-Bit Addressable Latch	34723	No TTL Equivalent	3-127
			TRANSLATORS	
75367	Quad TTL-to-CMOS Converter, 3-State Outputs	34104	Different Pinout. The 34104 has true and complement outputs and a common active HIGH Output Enable input. The 75367 has only the inverted outputs available and has individual active LOW Output Enable inputs.	3-100
			ARITHMETIC OPERATORS, ADDERS, COMPARATORS	
74L85	4-Bit Magnitude Comparator	340085	Same Pinout, Functionally Identical	3-133
			LSI — SPECIAL FUNCTION	
	Programmable Bit Rate Generator	34702	No TTL Equivalent	3-114
			RAMs	
74S189 7489	16 x 4-Bit RAM with 3-State Outputs	34725	Same Pinout, Functionally Identical. The 34725 is also similar to the 7489. The 7489 has open collector outputs which are HIGH impedance when Chip Select and Write Enable are HIGH. Outputs are the complement of data inputs when Write Enable is LOW irrespective of Chip Select. Outputs are the complement of the selected word when Write Enable is HIGH and Chip Select is LOW.	3-130
74200	256 x 1-Bit RAM with 3-State Outputs	34720	Different Pinout. The 74200 has three Chip Select inputs but does not have a Q output. Write Enable is active LOW. The 34720 has only one Chip Select input but has both Q and $\overline{Q}$ outputs. Write Enable is active HIGH. The 37420 is transparent in the Write mode.	3-124

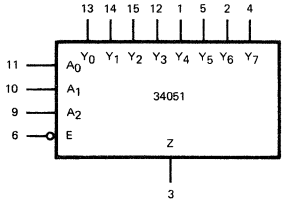
TTL TO CMOS FUNCTION SELECTOR GUIDE

34016 AND 34066



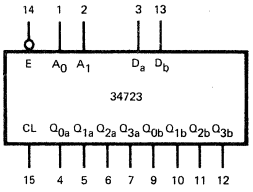
V_{DD} = Pin 14
V_{SS} = Pin 8

34051



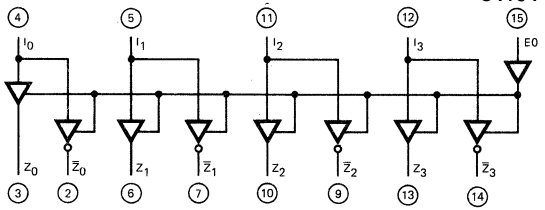
V_{DD} = Pin 16
V_{SS} = Pin 8
V_{EE} = Pin 7

34723



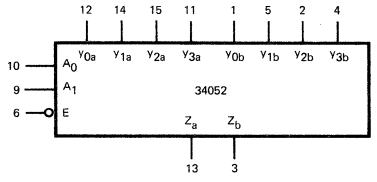
V_{DD} = Pin 16
V_{SS} = Pin 8

34104



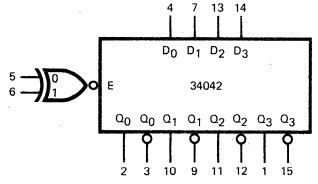
V_{DDO} = Pin 1 V_{DDI} = Pin 16 V_{SS} = Pin 8

34052



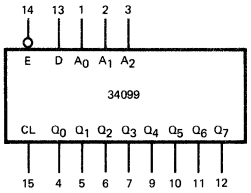
V_{DD} = Pin 16
V_{SS} = Pin 8
V_{EE} = Pin 7

34042



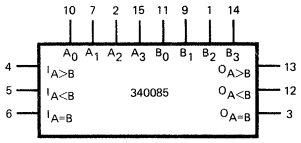
V_{DD} = Pin 16
V_{SS} = Pin 8

34099



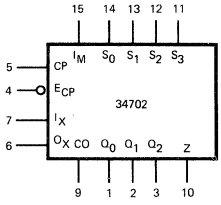
V_{DD} = Pin 16
V_{SS} = Pin 8

340085



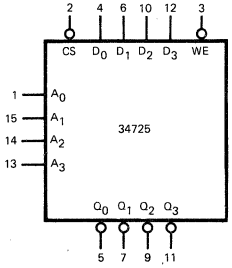
V_{DD} = Pin 16
V_{SS} = Pin 8

34702



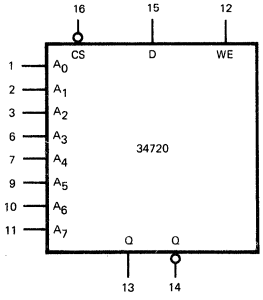
V_{DD} = Pin 16
V_{SS} = Pin 8

34725



V_{DD} = Pin 16
V_{SS} = Pin 8

34720



V_{DD} = Pin 5
V_{SS} = Pin 8
NC = Pin 4

CROSS REFERENCE GUIDE

Fairchild	RCA Series A	RCA* Series B	Motorola	National	Solid State Scientific	Solitron	Harris	Texas Instruments
340098				MM80C98				
340160			MC14160	MM74C160			HD74C160	TP4360
340161			MC14161	MM74C161			HD74C161	TP4361
340162			MC14162	MM74C162			HD74C162	TP4362
340163			MC14163	MM74C163			HD74C163	TP4363
340174			MC14174	MM74C174			HD74C174	
340175			MC14175	MM74C175				
340192		CD40192B		MM74C192			HD74C192	
340193		CD40193B		MM74C193			HD74C193	
340194		CD40194B	MC14194					
340195				MM74C195			HD74C195	

PACKAGE CODE CROSS REFERENCE

Package	Fairchild	RCA	Motorola	National	Solid State Scientific	Solitron	Harris	Texas Instruments
Plastic DIP	P	E	P	N	E	E	1	N
Ceramic DIP	D	D or F	L	D	D	D	1	J
Ceramic Flatpak	F	K	–	F	F	–	9	–

TEMPERATURE CODE CROSS REFERENCE

Temperature Range	Fairchild	RCA	Motorola	National	Solid State Scientific	Solitron	Harris	Texas Instruments
Military (–55°C to +125°C)	M	D, K, F Packages Only	A	54CXX 70CXX 46XX	D, F Packages Only	D Package Only	2	TF
Commercial (–40°C to +85°C)	C	E Package Only	C	56XX	E Package Only	E Package Only	4	TP
Commercial (0°C to +70°C)	–	–	–	74CXX 80CXX	–	–	5	TL

*These devices are members of the new RCA Series B CMOS. Specifications include: Maximum operating voltage range of 3 to 18 volts; recommended operating voltage range of 4 to 15 volts; symmetrical rise and fall times of 50 ns; output source and sink capability of 1.8 mA typical at V_{DD} = 10 volts and T_A = 25°C; and worst case noise immunity of 1.4 volts. All Fairchild 34000 Series CMOS devices are direct pin-for-pin replacements for RCA's Series A and Series B CMOS.

**This device is a functional equivalent only.

***This device is pin-for-pin compatible if leads 4 and 8 are tied together.

CROSS REFERENCE GUIDE

Fairchild	RCA Series A	RCA* Series B	Motorola	National	Solid State Scientific	Solitron	Harris	Texas Instruments
34001	CD4001A		MC14001A	MM4601A	SCL4001A	CM4001A	HD4001A	TP4001A
34002	CD4002A		MC14002A	MM4602A	SCL4002A	CM4002A	HD4002A	TP4002A
34011	CD4011A		MC14011A	MM4611A	SCL4011A	CM4011A	HD4011A	TP4011A
34012	CD4012A		MC14012A	MM4612A	SCL4012A	CM4012A	HD4012A	TP4012A
34013	CD4013A		MC14013A	MM4613A	SCL4013A	CM4013A	HD4013A	TP4013A
34014	CD4014A		MC14014A	MM4614A	SCL4014A	CM4014A		TP4014A
34015	CD4015A		MC14015A	MM4615A	SCL4015A			TP4015A
34016	CD4016A		MC14016A	MM4616A	SCL4016A	CM4016A		TP4016A
34017	CD4017A		MC14017A	MM4617A	SCL4017A	CM4017A		TP4017A
34019	CD4019A			MM4619A	SCL4019A	CM4019A	HD4019A	TP4019A
34020	CD4020A		MC14020A	MM4620A	SCL4020A	CM4020A		TP4020A
34021	CD4021A		MC14021A	MM4621A	SCL4021A	CM4021A		TP4021A
34023	CD4023A		MC14023A	MM4623A	SCL4023A	CM4023A	HD4023A	TP4023A
34024	CD4024A		MC14024A	MM4624A	SCL4024A	CM4024A		TP4024A
34025	CD4025A		MC14025A	MM4625A	SCL4025A	CM4025A	HD4025A	TP4025A
34027	CD4027A		MC14027A	MM4627A	SCL4027A		HD4027A	TP4027A
34028	CD4028A		MC14028A	MM4628A	SCL4028A			TP4028A
34029	CD4029A			MM4629A	SCL4029A			TP4029A
34030	CD4030A			MM4630A	SCL4030A		HD4030A	TP4030A
34035	CD4035A		MC14035A	MM4635A	SCL4035A			TP4035A
34040	CD4040A		MC14040A	MM4640A	SCL4040A			TP4040A
34042	CD4042A		MC14042A	MM4642A	SCL4042A			TP4042A
34049	CD4049A		MC14049A	MM4649A	SCL4049A			TP4049A
34050	CD4050A		MC14050A	MM4650A	SCL4050A			TP4050A
34051	CD4051A			MM4651A				TP4051A
34052	CD4052A			MM4652A				TP4052A
34066	CD4066A			MM4666A				
34068		CD4068B						
34069		CD4069B	MM74C04					
34070		CD4070B						
34071		CD4071B						
34077		CD4077B					HD4811	
34078		CD4078B						
34081		CD4081B						
34085		CD4085B						
34086		CD4086B						
34099		CD4099B						
34104						CM4104		
34512			MC14512					TP4512A
34518		CD4518B	MC14518		SCL4518			TP4518A
34520		CD4520B	MC14520		SCL4520			TP4520A
34539			MC14539					TP4539A
34555		CD4555B	MC14555					
34556		CD4556B	MC14556					
34702								
34720	***CD4061A							
34723								
34725								
340085			**MC14585	MM74C85				
340097				MM80C97				

34000
SERIES CMOS FAMILY CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (Non-operating) above which useful life may be impaired. All voltages are referenced to V_{SS}.

Supply Voltage V_{DD}	−0.5 to 18 V
Voltage on any Input	−0.5 to V_{DD} +0.5 V
Current into any Input	±10 mA
Maximum Power Dissipation	400 mW
Storage Temperature	−65°C to 150°C
Lead Temperature (Soldering, 10 s)	300°C

RECOMMENDED OPERATING CONDITIONS

Fairchild CMOS will operate over a recommended V_{DD} power supply range of 3 to 15 V, as referenced to V_{SS} (usually ground). Parametric limits are guaranteed for V_{DD} equal to 5, 10 and 15 V. Where low power dissipation is required, the lowest power supply voltage, consistent with required speed, should be used. For larger noise immunity, higher power supply voltages should be specified. Because of its wide operating range, power supply regulation and filtering are less critical than with other types of logic. The lower limit of supply regulation is 3 V, or as determined by required system speed and/or noise immunity or interface to other logic. The recommended upper limit is 15 V or as determined by power dissipation constraints or interface to other logic.

Unused inputs must be connected to V_{DD}, V_{SS} or another input.

Care should be used in handling CMOS devices; large static charges may damage the device.

Operating temperature ranges are −40°C to +85°C for Commercial and −55°C to +125°C for Military.

PARAMETER	34000XC			34000XM			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
Supply Voltage, V_{DD}	3		15	3		15	V
Operating Free Air Temperature Range	−40	+25	+85	−55	+25	+125	°C

X = Package Type; F for Flatpak, D for Ceramic DIP, P for Plastic DIP. See Section 6 for Ordering Information.

DC CHARACTERISTICS FOR THE 34000 SERIES CMOS FAMILY — Parametric Limits listed below are guaranteed for the entire Fairchild CMOS Family unless otherwise specified on the individual data sheets.

DC CHARACTERISTICS: V_{DD} = 5 V, V_{SS} = 0 V

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEMP	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage		3.5			V	All	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				1.5	V	All	Guaranteed Input LOW Voltage	
V_{OH}	Output HIGH Voltage		4.99			V	MIN, 25°C	I_{OH} = 0 mA, Inputs at 0 or 5 V per	
			4.95				MAX	the Logic Function or Truth Table	
			4.0			V	All	I_{OH} = 0 mA, Inputs at 1.5 or 3.5 V	
V_{OL}	Output LOW Voltage				0.01	V	MIN, 25°C	I_{OL} = 0 mA, Inputs at 0 or 5 V per	
					0.05		MAX	the Logic Function or Truth Table	
					0.5	V	All	I_{OL} = 0 mA, Inputs at 1.5 or 3.5 V	
I_{IN}	Input Current	XC			0.1	μA	25°C	Lead under test at 0 or 5 V	
		XM			0.01			All other Inputs simultaneously at 0 or 5 V	
I_{OH}	Output HIGH Current		−1.5			mA	MIN, 25°C	V_{OUT} = 2.5 V	Inputs at 0 or 5 V per the Logic Function or Truth Table
			−1.0				MAX		
			−0.7			mA	MIN, 25°C	V_{OUT} = 4.5 V	
			−0.4				MAX		
I_{OL}	Output LOW Current		1.0			mA	MIN	V_{OUT} = 0.4 V	
			0.8				25°C		
			0.4				MAX		

34000 SERIES CMOS FAMILY CHARACTERISTICS

DC CHARACTERISTICS: V_{DD} = 10 V, V_{SS} = 0 V

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEMP	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		7.0			V	All	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage				3.0	V	All	Guaranteed Input LOW Voltage
V_{OH}	Output HIGH Voltage		9.99 9.95			V	MIN, 25°C MAX	I_{OH} = 0 mA, Inputs at 0 or 10 V per the Logic Function or Truth Table
			9.0			V	All	I_{OH} = 0 mA, Inputs at 3 or 7 V
V_{OL}	Output LOW Voltage				0.01 0.05	V	MIN, 25°C MAX	I_{OL} = 0 or 10 V per the Logic Function or Truth Table
					1.0	V	All	I_{OL} = 0 mA, Inputs at 3 or 7 V
I_{IN}	Input Current	XC			0.1	μA	25°C	Lead under test at 0 or 10 V All other Inputs Simultaneously at 0 or 10 V
		XM			0.01			
I_{OH}	Output HIGH Current		−1.4 −0.8			mA	MIN, 25°C MAX	V_{OUT} = 9.5 V — Inputs at 0 or 10 V per the Logic Function or Truth Table
I_{OL}	Output LOW Current		2.6 2.0 1.2			mA	MIN 25°C MAX	V_{OUT} = 0.5 V — Inputs at 0 or 10 V per the Logic Function or Truth Table

DC CHARACTERISTICS: V_{DD} = 15 V, V_{SS} = 0 V

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEMP	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		10.5			V	All	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage				4.5	V	All	Guaranteed Input LOW Voltage
V_{OH}	Output HIGH Voltage		14.99 14.95			V	MIN, 25°C MAX	I_{OH} = 0 mA, Inputs at 0 or 15 V per the Logic Function or Truth Table
			13.0			V	All	I_{OH} = 0 mA, Inputs at 4.5 or 10.5 V
V_{OL}	Output LOW Voltage				0.01 0.05	V	MIN, 25°C MAX	I_{OL} = 0 mA, Inputs at 0 or 15 V per the Logic Function or Truth Table
					2.0	V	All	I_{OL} = 0 mA, Inputs at 4.5 or 10.5 V
I_{IN}	Input Current	XC			1.0	μA	25°C	Lead under test at 0 or 15 V All other Inputs Simultaneously at 0 or 15 V
		XM			1.0			
I_{OH}	Output HIGH Current		−2.2 −1.4			mA	MIN, 25°C MAX	V_{OUT} = 14.5 V — Inputs at 0 or 15 V per the Logic Function or Truth Table
I_{OL}	Output LOW Current		3.6 2.0			mA	MIN, 25°C MAX	V_{OUT} = 0.5 V — Inputs at 0 or 15 V per the Logic Function or Truth Table

TYPICAL 34000 SERIES CHARACTERISTICS

Fig. 3-1
POSITIVE-GOING PROPAGATION DELAY VERSUS SUPPLY VOLTAGE

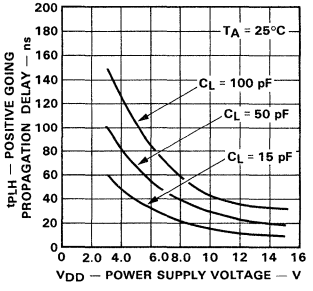


Fig. 3-2
NEGATIVE-GOING PROPAGATION DELAY VERSUS SUPPLY VOLTAGE

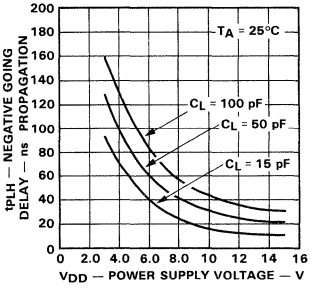


Fig. 3-3
POSITIVE-GOING PROPAGATION DELAY VERSUS LOAD CAPACITANCE

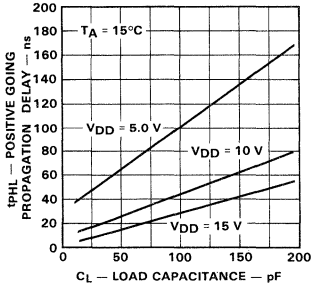


Fig. 3-4
NEGATIVE-GOING PROPAGATION DELAY VERSUS LOAD CAPACITANCE

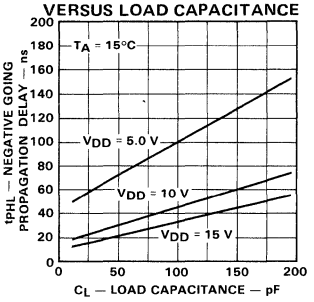


Fig. 3-5
VOLTAGE TRANSFER CHARACTERISTICS OVER −55°C TO +125°C RANGE

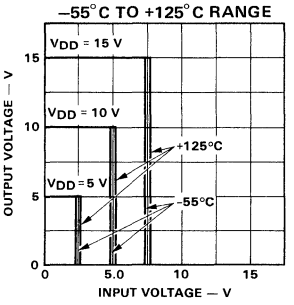


Fig. 3-6
GATE POWER DISSIPATION VERSUS FREQUENCY

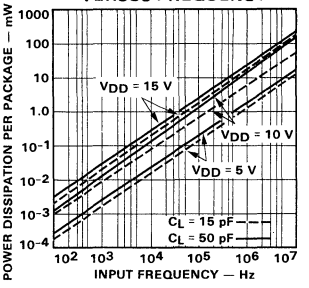


Fig. 3-7
PROPAGATION DELAY VERSUS AMBIENT TEMPERATURE @ V_{DD} = 5.0 V

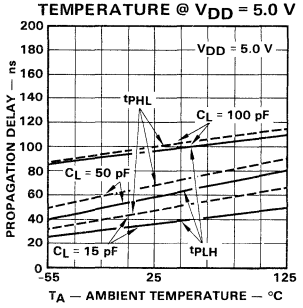


Fig. 3-8
PROPAGATION DELAY VERSUS AMBIENT TEMPERATURE @ V_{DD} = 10 V

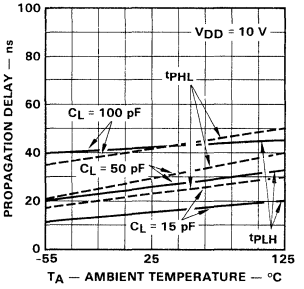


Fig. 3-9
PROPAGATION DELAY VERSUS AMBIENT TEMPERATURE @ V_{DD} = 15 V

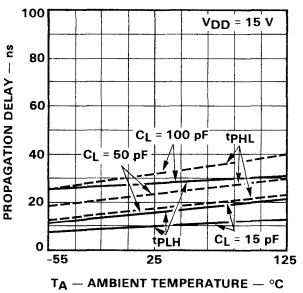


Fig. 3-11
n-CHANNEL DRAIN CHARACTERISTICS

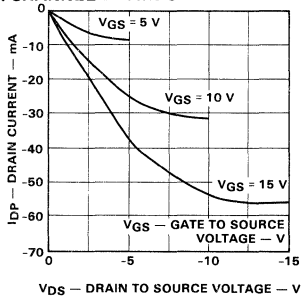
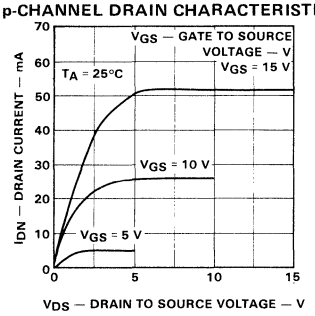


Fig. 3-12
p-CHANNEL DRAIN CHARACTERISTICS



OUTPUT TRANSITION TIME VERSUS LOAD CAPACITANCE

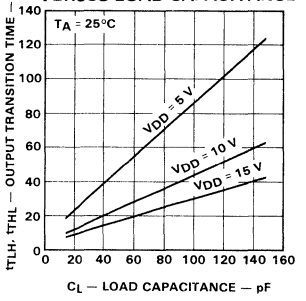
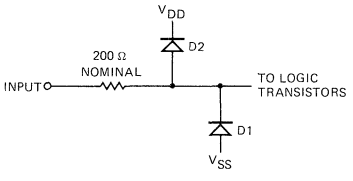


Fig. 3-13
INPUT PROTECTION CIRCUIT



INPUT CIRCUITRY

All inputs are protected by the network of Figure 3-13; a series input resistor plus diodes D1 and D2 clamp input voltages between V_{SS} and V_{DD}. Forward conduction of these diodes is typically 0.9 V at 1 mA. When V_{SS} or V_{DD} is not connected, avalanche breakdown of the diodes limit input voltage; D1 typically breaks down at 20 V, D2 at 26 V. In normal logic operation the diodes never conduct, but for certain special applications such as oscillators, circuit operation may actually depend on diode conduction. Operation in this mode is permissible so long as input currents do not exceed 10 mA.

Input capacitance is typically 5 pF across temperature for any input.

DEFINITION OF SYMBOLS AND TERMS USED IN DATA SHEETS

CURRENTS — Positive current is defined as conventional current flow into a device. Negative current is defined as conventional current flow out of a device.

I_{IN} — (Input Current) — The current flowing into a device at specified input voltage and V_{DD}.

I_{OH} — (Output HIGH Current) — The drive current flowing out of the device at specified HIGH output voltage and V_{DD}.

I_{OL} — (Output LOW Current) — The drive current flowing into the device at specified LOW output voltage and V_{DD}.

I_{DD} — (Quiescent Power Supply Current) — The current flowing into the V_{DD} lead at specified input and V_{DD} conditions.

I_{OZH} — (Output OFF Current HIGH) — The leakage current flowing into the output of a 3-state device in the "OFF" state at a specified HIGH output voltage and V_{DD}.

I_{OZL} — (Output OFF Current LOW) — The leakage current flowing out of a 3-state device in the "OFF" state at a specified HIGH output voltage and V_{DD}.

I_{IL} — (Input Current LOW) — The current flowing into a device at a specified LOW level input voltage and a specified V_{DD}.

I_{IH} — (Input Current HIGH) — The current flowing into a device at a specified HIGH level input voltage and a specified V_{DD}.

I_{DDL} — (Quiescent Power Supply Current LOW) — The current flowing into the V_{DD} lead with a specified LOW level input voltage on all inputs and specified V_{DD} conditions.

I_{DDH} — (Quiescent Power Supply Current HIGH) — The current flowing into the V_{DD} lead with a specified HIGH level input voltage on all inputs and specified V_{DD} conditions.

I_Z — (OFF State Leakage Current) — The leakage current flowing into the output of a 3-state device in the "OFF" state at a specified output voltage and V_{DD}.

VOLTAGES — All voltages are referenced to V_{SS} which is the most negative potential applied to the device.

V_{DD} — (Drain Voltage) — The most positive potential on the device.

V_{IH} — (Input HIGH Voltage) — The range of input voltages that represents a logic HIGH level in the system.

V_{IL} — (Input LOW Voltage) — The range of input voltages that represents a logic LOW level in the system.

V_{IH} (min) — (Minimum Input HIGH Voltage) — The minimum allowed input HIGH level in a logic system.

V_{IL} (max) — (Maximum Input LOW Voltage) — The maximum allowed input LOW level in a system.

V_{OH} — (Output HIGH Voltage) — The range of voltages at an output terminal with specified output loading and supply voltage. Device inputs are conditioned to establish a HIGH level at the output.

V_{OL} — (Output LOW Voltage) — The range of voltages at an output terminal with specified output loading and supply voltage. Device inputs are conditioned to establish a LOW level at the output.

V_{SS} — (Source Voltage) — For a device with a single negative power supply, the most negative power supply, used as the reference level for other voltages. Typically ground.

V_{EE} — (Source Voltage) — One of two (V_{SS} and V_{EE}) negative power supplies. For a device with dual negative power supplies, the most negative power supply used as a reference level for other voltages.

ANALOG TERMS

R_{ON} — (ON Resistance) — The effective "ON" state resistance of an analog transmission gate, at specified input voltage, output load and V_{DD}.

R_{ON} — ("Δ" ON Resistance) — The difference in effective "ON" resistance between any two transmission gates of an analog device at specified input voltage, output load and V_{DD}.

AC SWITCHING PARAMETERS

f_{MAX} — (Toggle Frequency/Operating Frequency) — The maximum rate at which clock pulses may be applied to a sequential circuit with the output of the circuit changing between 30% of V_{DD} and 70% of V_{DD}. Above this frequency the device may cease to function. See Figure 3-15.

t_{PLH} — (Propagation Delay Time) — The time between the specified reference points, normally 50% points on the input and output voltage waveforms, with the output changing from the defined LOW level to the defined HIGH level. See Figure 3-14.

t_{PHL} — (Propagation Delay Time) — The time between the specified reference points, normally 50% points on the input and output voltage waveforms, with the output changing from the defined HIGH level to the defined LOW level. See Figure 3-14.

t_{TLH} — (Transition Time, LOW to HIGH) — The time between two specified reference points on a waveform, normally 10% and 90% points, which is changing from LOW to HIGH. See Figure 3-14.

t_{THL} — (Transition Time, HIGH to LOW) — The time between two specified reference points on a waveform, normally 90% to 10% points, which is changing from HIGH to LOW. See Figure 3-14.

t_w — (Pulse Width) — The time between 50% amplitude points on the leading and trailing edges of pulse.

t_h — (Hold Time) — The interval immediately following the active transition of the timing pulse (usually the clock pulse) or following the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its continued recognition. A negative hold time indicates that the correct logic level may be released prior to the active transition of the timing pulse and still be recognized.

t_s — (Set-up Time) — The interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its recognition. A negative set-up time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.

t_{PHZ} — (3-State Output Disable Time, HIGH to Z) — The time between the specified reference points, normally the 50% point on the Output Enable input voltage waveform and a point representing a 0.1 V_{DD} drop on the Output voltage waveform of a 3-state device, with the output changing from the defined HIGH level to a high impedance OFF state.

t_{PLZ} — (3-State Output Disable Time, LOW to Z) — The time between the specified reference points, normally the 50% point on the Output Enable input voltage waveform and a point representing a 0.1 V_{DD} rise on the Output voltage waveform of a 3-state device, with the output changing from the defined LOW level to a high impedance OFF state.

t_{PZH} — (3-State Output Enable Time, Z to HIGH) — The time between the specified reference points, normally the 50% point on the Output Enable input voltage waveform and a point representing 0.5 V_{DD} on the Output voltage waveform of a 3-state device, with the output changing from a high impedance OFF state to the defined HIGH level.

t_{PZL} — (3-State Output Enable Time, Z to LOW) — The time between the specified reference points, normally the 50% point on the Output Enable input voltage waveform and a point representing 0.5 V_{DD} on the Output voltage waveform of a 3-state device, with the output changing from a high impedance OFF state to the defined LOW level.

t_{rec} — (Recovery Time) — The time between the end of an overriding asynchronous input, typically a Clear or Reset input, and the earliest allowable beginning of a synchronous control input, typically a Clock input, normally measured at 50% points on both input voltage waveforms.

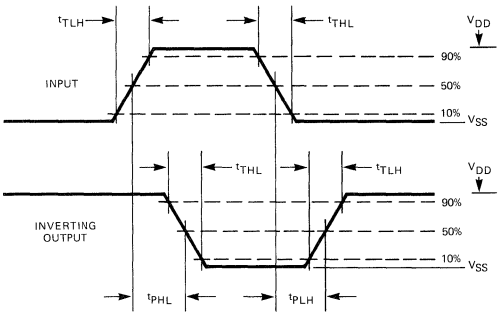


Fig. 3-14. Propagation Delay, Transition Time

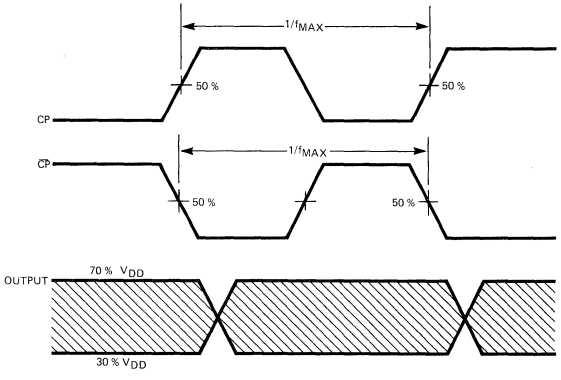
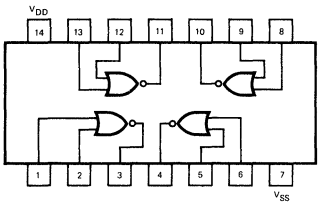


Fig. 3-15. Maximum Operating Frequency

34001 QUAD 2-INPUT NOR GATE • 34002 DUAL 4-INPUT NOR GATE

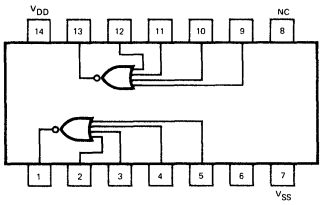
DESCRIPTION — These CMOS logic elements provide the positive input NOR function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

34001
LOGIC AND CONNECTION DIAGRAM
DIP(TOP VIEW)



NOTE:
The Flatpak versions have the same pinouts (Connection Diagram) as the Dual In-Line Package.

34002
LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V

SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEMP	TEST CONDITIONS
I_{DD}	Quiescent Power Supply Current	XC			0.5			5.0		1.0		MIN, 25°C	All inputs common and at 0 V or V_{DD}
					15.0			30.0		6.0	μA	MAX	
		XM			0.05			0.1		0.02		MIN, 25°C	
					3.0			6.0		1.2	μA	MAX	

NOTE: Additional DC Characteristics are listed in this section under 34000 Series CMOS Family Characteristics.

AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C, 34001 only

SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEST CONDITIONS
t_{PLH}	Propagation Delay		40	75		20	40		15		ns	
t_{PHL}			40	75		20	40		15		ns	C_L = 15 pF
t_{TLH}	Output Transition		25	75		10	40		8	25	ns	Input Transition Times ⩽ 20 ns
t_{THL}	Time		25	75		10	40		8	25	ns	
t_{PLH}	Propagation Delay		60	110		25	60		20		ns	
t_{PHL}			60	110		25	60		20		ns	C_L = 50 pF
t_{TLH}	Output Transition		60	135		30	70		20	45	ns	Input Transition Times ⩽ 20 ns
t_{THL}	Time		60	135		30	70		20	45	ns	

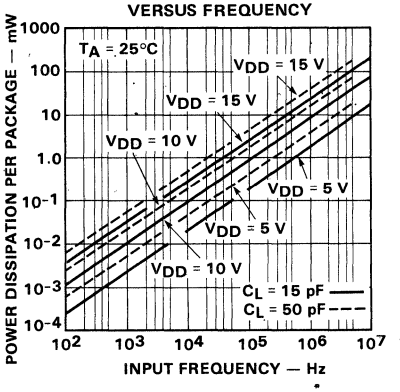
AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C, 34002 only

SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEST CONDITIONS
t_{PLH}	Propagation Delay		50	75		20	40		15		ns	
t_{PHL}			50	75		23	40		17		ns	C_L = 15 pF
t_{TLH}	Output Transition		30	75		15	40		11	25	ns	Input Transition Times ⩽ 20 ns
t_{THL}	Time		25	75		10	40		7	25	ns	
t_{PLH}	Propagation Delay		65	110		30	60		20		ns	
t_{PHL}			70	110		30	60		23		ns	C_L = 50 pF
t_{TLH}	Output Transition		75	135		40	70		30	45	ns	Input Transition Times ⩽ 20 ns
t_{THL}	Time		60	135		23	70		15	45	ns	

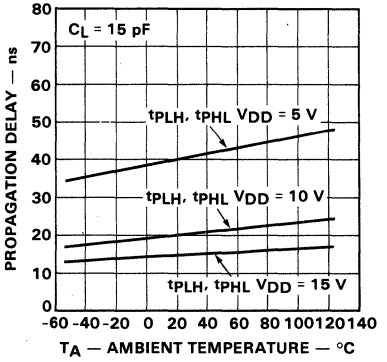
NOTE:
Propagation delays and output transition times are graphically described in this section under 34000 Series CMOS Family Characteristics.

TYPICAL ELECTRICAL CHARACTERISTICS

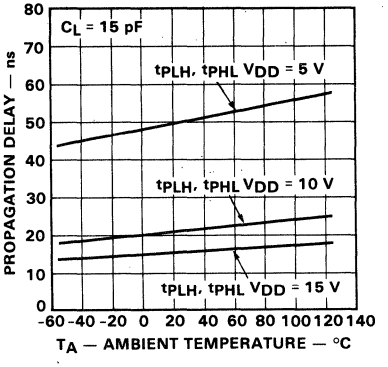
34001 AND 34002
POWER DISSIPATION
VERSUS FREQUENCY



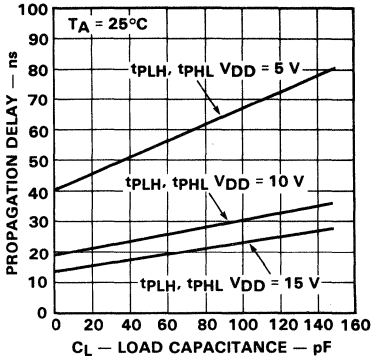
34001
PROPAGATION DELAY
VERSUS TEMPERATURE



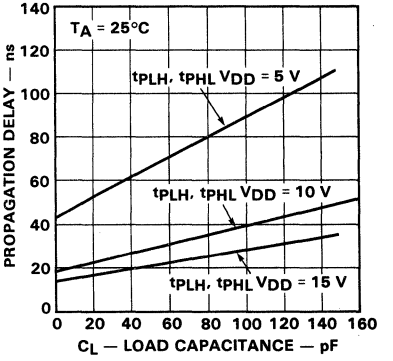
34002
PROPAGATION DELAY
VERSUS TEMPERATURE



34001
PROPAGATION DELAY
VERSUS LOAD CAPACITANCE



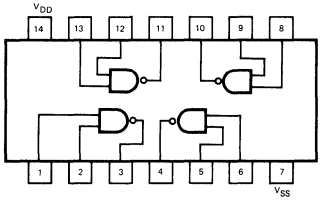
34002
PROPAGATION DELAY
VERSUS LOAD CAPACITANCE



34011 QUAD 2-INPUT NAND GATE • 34012 DUAL 4-INPUT NAND GATE

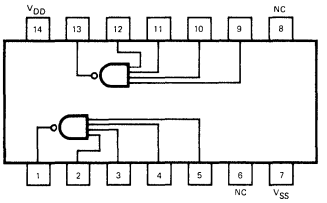
DESCRIPTION — These CMOS logic elements provide the positive input NAND function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

34011
LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak versions have the same pinouts (Connection Diagram) as the Dual In-Line Package.

34012
LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



3

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V

SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEMP	TEST CONDITIONS
I_{DD}	Quiescent Power Supply Current	XC			0.5			5.0		1.0			
					15.0			30.0		6.0	μA	MIN, 25°C MAX	All inputs common and at 0 V or V_{DD}
		XM			0.05			0.1		0.02			
					3.0			6.0		1.2	μA	MIN, 25°C MAX	

NOTE: Additional DC Characteristics are listed in this section under 34000 Series CMOS Family Characteristics.

AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C, 34011 only

SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEST CONDITIONS
t_{PLH}	Propagation Delay		40	75		20	40		15		ns	
t_{PHL}			40	75		20	40		15		ns	C_L = 15 pF
t_{TLH}	Output Transition		25	75		10	40		8	25	ns	Input Transition Times ⩽ 20 ns
t_{THL}	Time		25	75		10	40		8	25	ns	
t_{PLH}	Propagation Delay		60	110		25	60		20		ns	
t_{PHL}			60	110		25	60		20		ns	C_L = 50 pF
t_{TLH}	Output Transition		60	135		30	70		20	45	ns	Input Transition Times ⩽ 20 ns
t_{THL}	Time		60	135		30	70		20	45	ns	

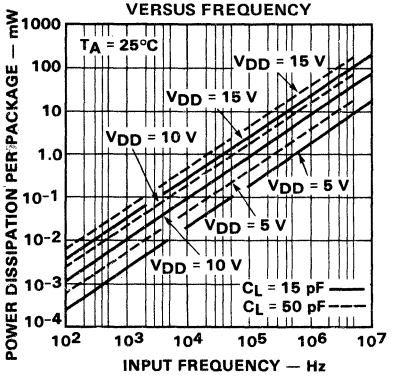
AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C, 34012 only

SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEST CONDITIONS
t_{PLH}	Propagation Delay		54	75		24	40		18		ns	
t_{PHL}			61	75		23	40		15		ns	C_L = 15 pF
t_{TLH}	Output Transition		22	75		16	40		11	25	ns	Input Transition Times ⩽ 20 ns
t_{THL}	Time		31	75		12	40		8	25	ns	
t_{PLH}	Propagation Delay		73	110		33	60		24		ns	
t_{PHL}			85	110		31	60		20		ns	C_L = 50 pF
t_{TLH}	Output Transition		76	135		37	70		27	45	ns	Input Transition Times ⩽ 20 ns
t_{THL}	Time		67	135		25	70		17	45	ns	

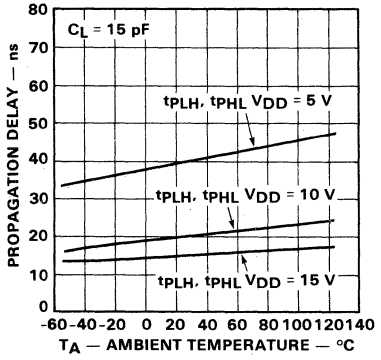
NOTE: Propagation delays and output transition times are graphically described in this section under 34000 Series CMOS Family Characteristics.

TYPICAL ELECTRICAL CHARACTERISTICS

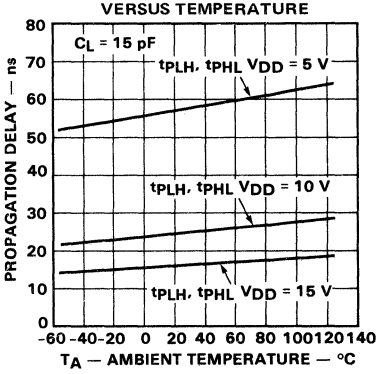
34011 AND 34012
POWER DISSIPATION
VERSUS FREQUENCY



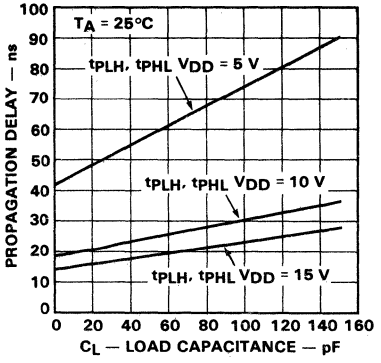
34011
PROPAGATION DELAY
VERSUS TEMPERATURE



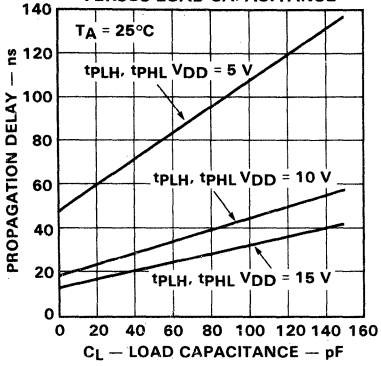
34012
PROPAGATION DELAY
VERSUS TEMPERATURE



34011
PROPAGATION DELAY
VERSUS LOAD CAPACITANCE



34012
PROPAGATION DELAY
VERSUS LOAD CAPACITANCE



34013
DUAL D FLIP-FLOP

DESCRIPTION — The 34013 is a CMOS Dual D Flip-Flop which is edge-triggered and features independent Set Direct, Clear Direct, and Clock inputs. Data is accepted when the Clock is LOW and transferred to the output on the positive-going edge of the Clock. The active HIGH asynchronous Clear Direct (C_D) and Set Direct (S_D) are independent and override the D or Clock inputs. The outputs are buffered for best system performance.

PIN NAMES

D	Data Input
CP	Clock Input (L→H Edge-Triggered)
S_D	Asynchronous Set Direct Input (Active HIGH)
C_D	Asynchronous Clear Direct Input (Active HIGH)
Q	True Output
$\overline{Q}$	Complement Output

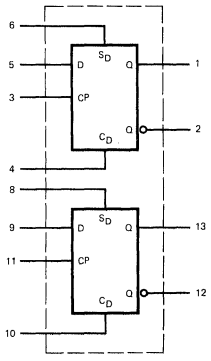
34013
TRUTH TABLE

INPUTS				OUTPUTS	
S_D	C_D	CP	D	Q_{n+1}	$\overline{Q}_{n+1}$
H	L	X	X	H	L
L	H	X	X	L	H
H	H	X	X	H	H
L	L	⌐¬	L	L	H
L	L	⌐¬	H	H	L

L = LOW Level
H = HIGH Level
⌐¬ = Positive-Going Transition
X = Don't Care
Q_{n+1} = State After Clock Positive Transition

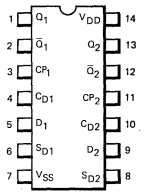
LOGIC SYMBOL

34013



V_{DD} = Pin 14
V_{SS} = Pin 7

CONNECTION DIAGRAM
DIP (TOP VIEW)
34013



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V

SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEMP	TEST CONDITIONS
I_{DD}	Quiescent Power Supply Current	XC			10			20		4		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					140			280		56			MAX	
		XM			1			2		0.4		μA	MIN, 25°C	
					60			120		24			MAX	

NOTE: Additional DC Characteristics are listed in this section under 34000 Series CMOS Family Characteristics.

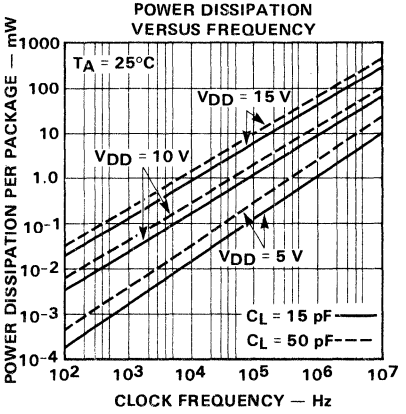
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C

SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEST CONDITIONS
t_{PLH}	Propagation Delay,		80	150		35	66		25		ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
t_{PHL}	CP to Q, $\overline{Q}$		80	150		35	66		25		ns	
t_{PLH}	Propagation Delay,		95	171		40	72		30		ns	
t_{PHL}	S_D or C_D to $\overline{Q}$		60	110		30	55		20		ns	
t_{PLH}	Propagation Delay,		100	170		45	80		30		ns	
t_{PHL}	S_D or C_D to $\overline{Q}$		100	170		45	80		30		ns	
t_{TLH}	Output Transition		34	75		20	40		10	25	ns	
t_{THL}	Time		34	75		20	40		10	25	ns	
t_{PLH}	Propagation Delay,		95	170		38	72		29		ns	C_L = 50 pF Input Transition Times ⩽ 20 ns
t_{PHL}	CP to Q, $\overline{Q}$		95	170		38	72		29		ns	
t_{PLH}	Propagation Delay,		130	220		45	90		32		ns	
t_{PHL}	S_D or C_D to $\overline{Q}$		75	135		35	65		20		ns	
t_{PLH}	Propagation Delay,		115	190		50	90		35		ns	
t_{PHL}	S_D or C_D to $\overline{Q}$		115	190		50	90		35		ns	
t_{TLH}	Output Transition		60	135		30	70		20	45	ns	
t_{THL}	Time		60	135		30	70		20	45	ns	
t_s	Set-Up Time, Data to CP	80	30		40	15			8		ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
t_h	Hold Time, Data to CP	0	-25		0	-12			-6		ns	
t_wCP(L)	Minimum Clock Pulse Width	100	55		55	30			18		ns	
t_w S_D(H)	Minimum S_D Pulse Width	60	30		30	15			10		ns	
t_w C_D(H)	Minimum C_D Pulse Width	60	30		30	15			10		ns	
t_{rec} S_D	Recovery Time for S_D	-20	-9		-10	-4			-2		ns	
t_{rec} C_D	Recovery Time for C_D	0	11		0	6			6		ns	
f_{MAX}	Maximum CP Frequency (Note 2)	5	8		8	16					MHz	

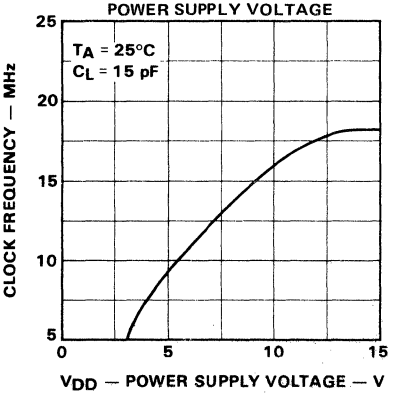
NOTES:
1. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Set-up Times (t_s), Hold Times (t_h), Recovery Times (t_{rec}), and Minimum Pulse Widths (t_w) do not vary with load capacitance.
2. For f_{MAX} input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
3. Propagation Delays and Output Transition Times are graphically described in this section under 34000 Series CMOS Family Characteristics.
4. It is recommended that input rise and fall times to the Clock Input be less than 15 μs.

TYPICAL ELECTRICAL CHARACTERISTICS

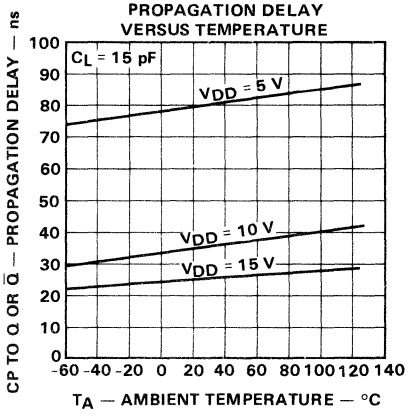
POWER DISSIPATION VERSUS FREQUENCY



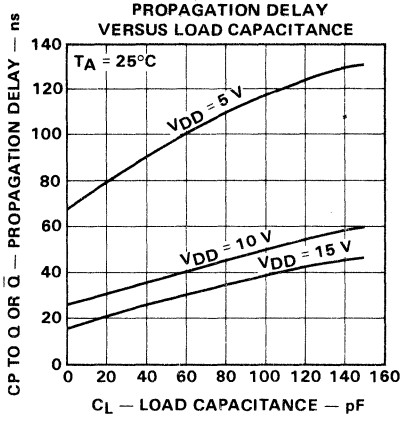
CLOCK FREQUENCY VERSUS POWER SUPPLY VOLTAGE



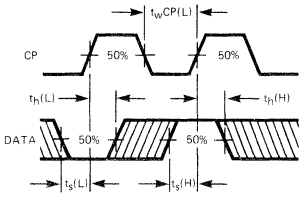
PROPAGATION DELAY VERSUS TEMPERATURE



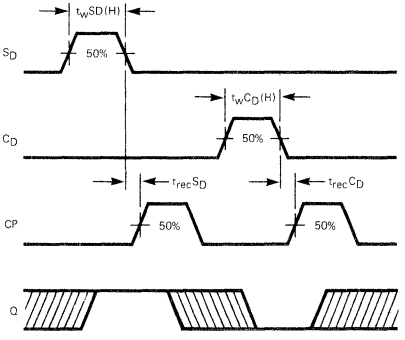
PROPAGATION DELAY VERSUS LOAD CAPACITANCE



WAVEFORMS



SET-UP TIMES, HOLD TIMES, AND MINIMUM CLOCK PULSE WIDTH



RECOVERY TIME FOR S_D, RECOVERY TIME FOR C_D, MINIMUM S_D PULSE WIDTH, AND MINIMUM C_D PULSE WIDTH

NOTE: Set-up Times and Hold Times are shown as positive values but may be specified as negative values.

34014
8-BIT SHIFT REGISTER

DESCRIPTION – The 34014 is a fully synchronous edge-triggered 8-Bit Shift Register with eight synchronous Parallel Inputs (P_0–P_7), a synchronous Serial Data Input (D_S), a synchronous Parallel Enable Input (PE), a LOW-to-HIGH edge-triggered Clock Input (CP) and Buffered Parallel Outputs from the last three stages (Q_5–Q_7).

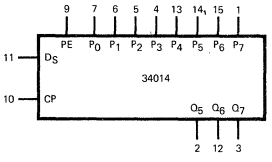
Operation is synchronous and the device is edge-triggered on the LOW-to-HIGH transition of the Clock Input (CP). When the Parallel Enable Input (PE) is HIGH, data is loaded into the register from the Parallel Inputs (P_0–P_7) on the LOW-to-HIGH transition of the Clock Input (CP). When the Parallel Enable Input (PE) is LOW, data is shifted into the first register position from the Serial Data Input (D_S) and all the data in the register is shifted one position to the right on the LOW-to-HIGH transition of the Clock Input (CP).

- **TYPICAL SHIFT FREQUENCY OF 14.7 MHz AT V_{DD} = 10 V**
- **PARALLEL OR SERIAL TO SERIAL DATA TRANSFER**
- **AVAILABLE OUTPUTS FROM THE LAST THREE STAGES**
- **FULLY SYNCHRONOUS**

PIN NAMES

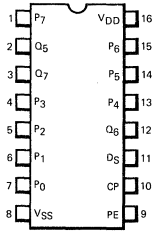
PE	Parallel Enable Input
P_0–P_7	Parallel Data Inputs
D_S	Serial Data Input
CP	Clock Input (L→H Edge-Triggered)
Q_5, Q_6, Q_7	Buffered Parallel Outputs from the Last Three Stages

LOGIC SYMBOL



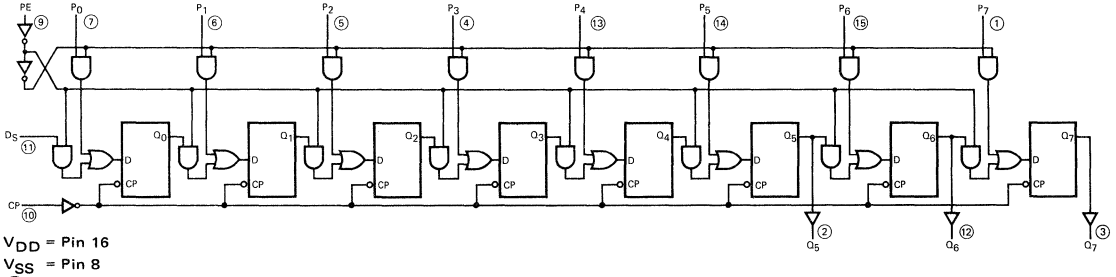
V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
◯ = Pin Number

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V

SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEMP	TEST CONDITIONS
I_{DD}	Quiescent Power Supply Current	XC			50			100		20		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					600			1200		240			MAX	
		XM			5			10		2		μA	MIN, 25°C	
					300			600		120			MAX	

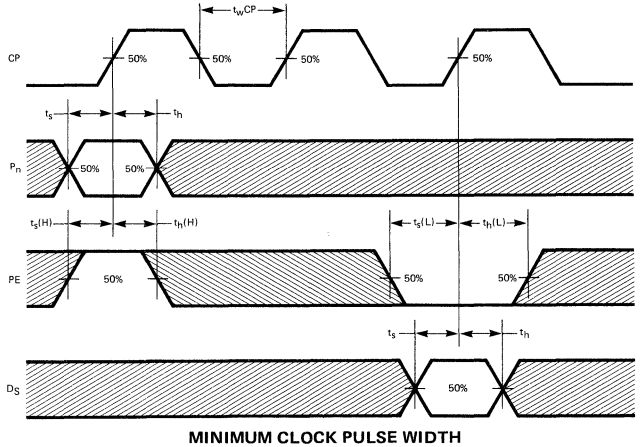
NOTE: Additional DC Characteristics are listed in this section under 34000 Series CMOS Family Characteristics.

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C

SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEST CONDITIONS
t_{PHL}	Propagation Delay, CP to any Q		109			47			33		ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
t_{PHL}			139			57			38		ns	
t_{TLH}	Output Transition Time		33			19			13		ns	
t_{THL}			37			19			15		ns	
t_{PLH}	Propagation Delay, CP to any Q		129			57			41		ns	C_L = 50 pF Input Transition Times ⩽ 20 ns
t_{PHL}			165			68			47		ns	
t_{TLH}	Output Transition Time		70			37			21		ns	
t_{THL}			77			34			21		ns	
t_wCP	CP Minimum Pulse Width		93			33			22		ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
t_s	Set-Up Time PE to CP		118			44			29		ns	
t_h	Hold Time PE to CP		117			43			27		ns	
t_s	Set-Up Time D_S to CP		80			28			17		ns	
t_h	Hold Time D_S to CP		77			27			16		ns	
t_s	Set-Up Time P_n to CP		108			37			23		ns	
t_h	Hold Time P_n to CP		107			36			22		ns	
f_{MAX}	Max. Input Clock Frequency (Note 3)		5.8			14.7					MHz	

NOTES:
1. Propagation Delays and Output Transition Times are graphically described in this section under 34000 Series CMOS Family Characteristics.
2. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Set-up Times (t_s). Hold Times (t_h), and Minimum Pulse Widths (t_w) do not vary with load capacitance.
3. For f_{MAX} input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
4. It is recommended that input rise and fall times to the Clock Input be less than 15 μs.

SWITCHING WAVEFORMS



MINIMUM CLOCK PULSE WIDTH AND SET-UP AND HOLD TIMES, PE TO CP, D_S TO CP, AND P_n TO CP

NOTE: Set-up and Hold Times are shown as positive values but may be specified as negative values.

34015
DUAL 4-BIT STATIC SHIFT REGISTER

DESCRIPTION — The 34015 is a Dual Edge-Triggered 4-Bit Static Shift Register (Serial-to-Parallel Converter). Each Shift Register has a Serial Data Input (D), a Clock Input (CP), four fully buffered parallel Outputs (Q_0-Q_3) and an overriding asynchronous Master Reset Input (MR).

Information present on the serial Data Input (D) is shifted into the first register position, and all the data in the register is shifted one position to the right on the LOW-to-HIGH transition of the Clock Input (CP).

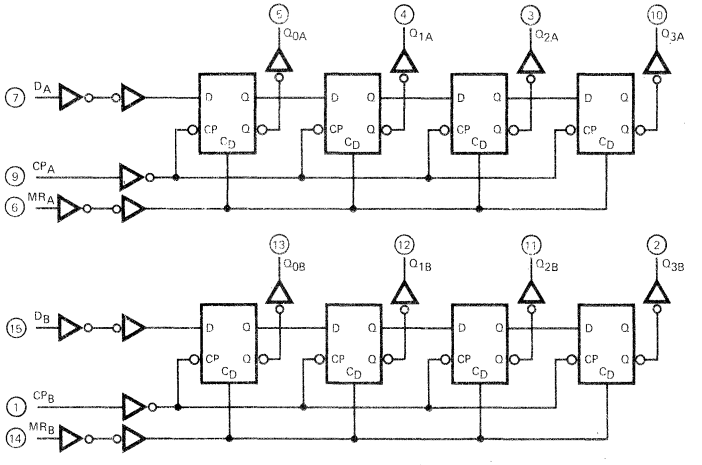
A HIGH on the Master Reset Input (MR) clears the register and forces the Outputs (Q_0-Q_3) LOW, independent of the Clock and Data Inputs (CP and D).

- **TYPICAL SHIFT FREQUENCY OF 14 MHz AT V_{DD} = 10 V**
- **ASYNCHRONOUS MASTER RESET**
- **SERIAL-TO-PARALLEL DATA TRANSFER**
- **FULLY BUFFERED OUTPUTS FROM EACH STAGE**

PIN NAMES

D_A, D_B	Serial Data Input
MR_A, MR_B	Master Reset Input (Active HIGH)
CP_A, CP_B	Clock Input (L→H Edge-Triggered)
Q_{0A}, Q_{1A}, Q_{2A}, Q_{3A}	Parallel Outputs
Q_{0B}, Q_{1B}, Q_{2B}, Q_{3B}	Parallel Outputs

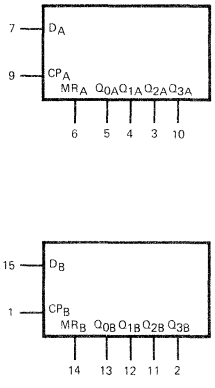
LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
◯ = Pin Number

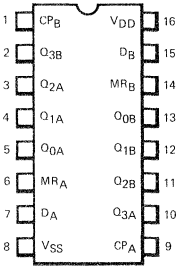
LOGIC SYMBOL

34015



V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			10			20		4		µA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					100			200		40			MAX	
		XM			1			2		0.4		µA	MIN, 25°C	
					30			60		12			MAX	

NOTE: Additional DC Characteristics are listed in this section under 34000 Series CMOS Family Characteristics.

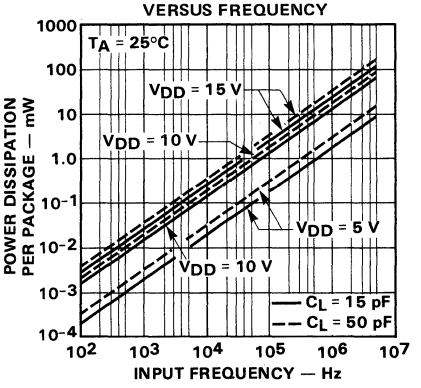
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, CP to Q		140	250		75	135		45		ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
t_{PHL}			140	250		75	135		45		ns	
t_{PHL}	Propagation Delay, MR to Q		150	300		85	150		60		ns	
t_{TLH}	Output Transition Time		50	100		25	60		20	40	ns	
t_{THL}			50	100		25	60		20	40	ns	
t_{PLH}	Propagation Delay, CP to Q		165	300		85	150		50		ns	C_L = 50 pF Input Transition Times ⩽ 20 ns
t_{PHL}			165	300		85	150		50		ns	
t_{PHL}	Propagation Delay, MR to Q		180	325		90	160		60		ns	
t_{TLH}	Output Transition Time		85	150		45	85		30	50	ns	
t_{THL}			85	150		45	85		30	50	ns	
t_s	Set-Up Time, D to CP	150	70		50	30			25		ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
t_h	Hold Time, D to CP	0	-5		0	-20			-10		ns	
$t_wCP(L)$	Minimum Clock Pulse Width	120	60		70	35			25		ns	
$t_wMR(H)$	Minimum MR Pulse Width	75	40		45	25			20		ns	
t_{rec}	MR Recovery Time	300	160		120	60			45		ns	
f_{MAX}	Maximum CP Frequency (Note 3)	4	8		7	14					MHz	

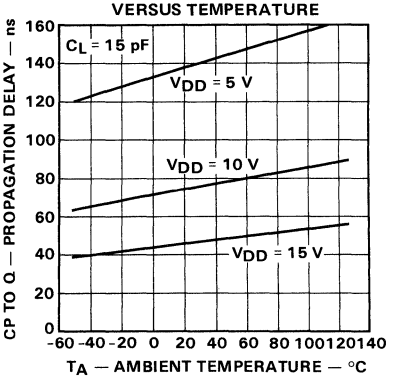
NOTES:
1. Propagation Delays and Output Transition Times are graphically described in this section under 34000 Series CMOS Family Characteristics.
2. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Set-up Times (t_s), Hold Times (t_h), Recovery Times (t_{rec}), and Minimum Pulse Widths (t_w) do not vary with load capacitance.
3. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
4. It is recommended that input rise and fall times to the Clock Input be less than 15 µs.

TYPICAL ELECTRICAL CHARACTERISTICS

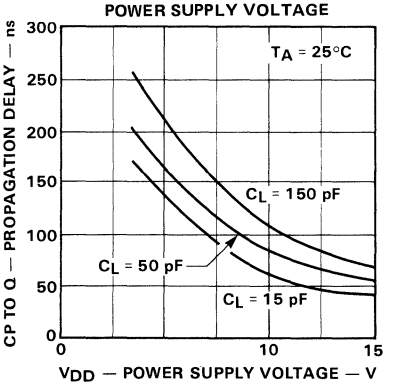
POWER DISSIPATION VERSUS FREQUENCY



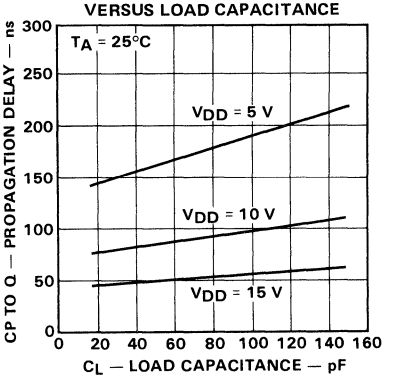
PROPAGATION DELAY VERSUS TEMPERATURE



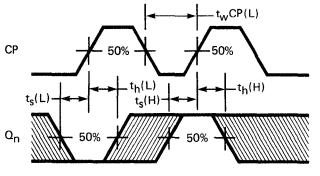
PROPAGATION DELAY VERSUS POWER SUPPLY VOLTAGE



PROPAGATION DELAY VERSUS LOAD CAPACITANCE

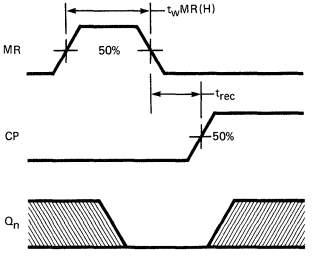


SWITCHING WAVEFORMS



SET-UP TIMES, HOLD TIMES AND MINIMUM CLOCK PULSE WIDTH

NOTE:
t_s and t_h are shown as positive values but may be specified as negative values.



RECOVERY TIME FOR MR AND MINIMUM MR PULSE WIDTH

34016
QUAD BILATERAL SWITCHES

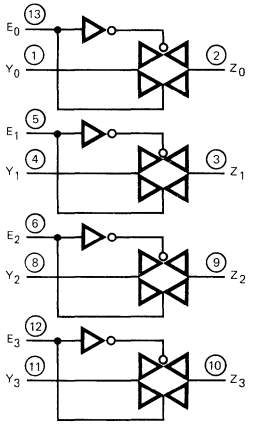
DESCRIPTION – The 34016 has four independent bilateral analog switches (transmission gates). Each switch has two Input/Output Terminals (Y_n, Z_n) and an active HIGH Enable Input (E_n). A HIGH on the Enable Input establishes a low impedance bidirectional path between Y_n and Z_n (ON condition). A LOW on the Enable Input disables the switch and establishes a high impedance between Y_n and Z_n (OFF condition).

- **DIGITAL OR ANALOG SIGNAL SWITCHING**
- **INDIVIDUAL ENABLE INPUTS (ACTIVE HIGH)**

PIN NAMES

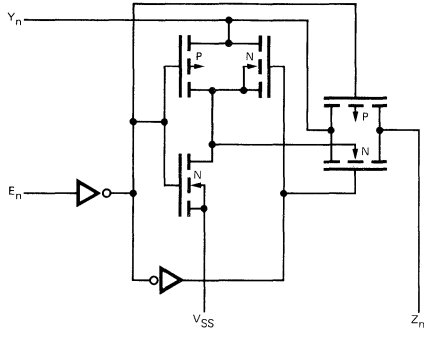
E_0 - E_3	Enable Inputs
Y_0 - Y_3	Input/Output Terminals
Z_0 - Z_3	Input/Output Terminals

LOGIC SYMBOL

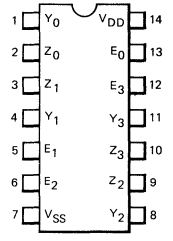


V_{DD} = Pin 14
V_{SS} = Pin 7
○ = Pin Numbers

LOGIC DIAGRAM (1/4 OF A 34016)



CONNECTION DIAGRAM
DIP (TOP VIEW)



Note: The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V

SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEMP	TEST CONDITIONS	
R_{ON}	ON Resistance	XC						610 660 840			370 400 520	Ω	MIN 25°C MAX	$V_{is} = V_{DD}$	R_L = 10 kΩ $E_n = V_{DD}$
								610 660 840			370 400 520	Ω	MIN 25°C MAX	$V_{is} = V_{SS}$ +0.25 V	
					1900 2000 2380							Ω	MIN 25°C MAX	V_{is} = 2.5 V	
								1750 1800 2360				Ω	MIN 25°C MAX	V_{is} = 5.6 V	
											775 800 1020	Ω	MIN 25°C MAX	V_{IN} = 9.3 V	
		XM						600 660 960			360 400 600	Ω	MIN 25°C MAX	$V_{is} = V_{DD}$	R_L = 10 kΩ $E_n = V_{DD}$
								600 660 960			360 400 600	Ω	MIN 25°C MAX	$V_{is} = V_{SS}$ +0.25 V	
					1870 2000 2600							Ω	MIN 25°C MAX	V_{is} = 2.5 V	
								1700 1800 2000				Ω	MIN 25°C MAX	V_{is} = 5.6 V	
											750 800 1200	Ω	MIN 25°C MAX	V_{is} = 9.3 V	
ΔR_{ON}	"Δ" ON Resistance Between Any Two Switches						15			10		Ω	25°C	$V_{is} = V_{DD}$ or V_{SS}, $E_n = V_{DD}$ R_L = 10 kΩ	
I_Z	OFF State Leakage Current, Any Y to Z							125			200	nA	25°C	$V_{is} = V_{DD}$ or V_{SS}, $E_n = V_{SS}$	
I_{DD}	Quiescent Power Supply Current	XC			0.25 7			0.5 8		0.1 1.6		μA	MIN, 25°C MAX	All inputs common and at V_{DD} or V_{SS}	
		XM			0.25 25			0.5 30		0.1 6		μA	MIN, 25°C MAX		

NOTES:

1. Additional DC Characteristics for the Enable Inputs are listed in this section under 34000 Series CMOS Family Characteristics.
2. V_{is} is the input voltage to Input/Output Terminal (Y_n/Z_n).

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, Y_n to Z_n or Z_n to Y_n		4 3			1.5 1.5			1 1		ns ns	R_L = 10 kΩ , E_n = V_{DD} C_L = 15 pF Input Transition Times ⩽ 20 ns V_{is} = V_{DD} (square wave)
t_{PZL} t_{PZH}	Output Enable Time		26 26			14 14			10 10		ns ns	E_n = V_{DD} (square wave) R_L = 10 kΩ , C_L = 15 pF Input Transition Times ⩽ 20 ns V_{is} = V_{DD}
t_{PLZ} t_{PHZ}	Output Disable Time		160 160			170 170			182 182		ns ns	
t_{PLH} t_{PHL}	Propagation Delay, Y_n to Z_n or Z_n to Y_n		8 8			3 4			2 2.5		ns ns	R_L = 10 kΩ , E_n = V_{DD} C_L = 50 pF Input Transition Times ⩽ 20 ns V_{is} = V_{DD} (square wave)
t_{PZL} t_{PZH}	Output Enable Time		32 32			16 16			13 13		ns ns	R_L = 10 kΩ , C_L = 50 pF Input Transition Times ⩽ 20 ns E_n = V_{DD} (square wave) V_{is} = V_{DD}
t_{PLZ} t_{PHZ}	Output Disable Time		380 380			380 380			400 400		ns ns	
	Distortion, Sine Wave Response		0.31			0.31			0.31		%	R_L = 10 kΩ , C_L = 15 pF Input Frequency = 1 kHz E_n = V_{DD} V_{is} = $V_{DD}/2$ (sine wave)
	Crosstalk Between Any Two Switches					0.9					MHz	R_L = 1 kΩ , E_A = V_{DD}, E_B = V_{SS} V_{is} = $V_{DD}/2$ sine wave at – 50 dB, 20 Log_{10} [V_{os} (B)/V_{is} (A)] = –50 dB
	Crosstalk, Enable Input to Output					50					mV	$R_{L(OUT)}$ = 10 kΩ, $R_{L(IN)}$ = 1 kΩ Input Transition Times ⩽ 20 ns E_n = V_{DD} (square wave)
	OFF State Feedthrough					1.25					MHz	R_L = 1 kΩ , E_n = V_{SS}, V_{is} = $V_{DD}/2$ sine wave 20 Log_{10} (V_{os}/V_{is}) = –50 dB
	ON State Frequency Response					90					MHz	R_L = 1 kΩ , V_{is} = $V_{DD}/2$ sine wave E_n = V_{DD}, 20 Log_{10} (V_{os}/V_{is}) = –3 dB
f_{MAX}	Enable Input Frequency (Note 2)					10					MHz	R_L = 1 kΩ , C_L = 15 pF Input Transition Times ⩽ 20 ns E_n = V_{DD} (square wave) V_{is} = V_{DD}

NOTES:
1. Propagation Delays and Output Transition Times are graphically described in this section under 34000 Series CMOS Family Characteristics.
2. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
3. V_{is}/V_{os} is the voltage signal at an Input/Output Terminal (Y_n/Z_n).

34017
5-STAGE JOHNSON COUNTER

DESCRIPTION — The 34017 is a 5-Stage Johnson Decade Counter with ten glitch free decoded active HIGH Outputs (O_0-O_9), an active LOW Output from the most significant flip-flop ($\overline{Q_{5-9}}$), active HIGH and active LOW Clock Inputs (CP_0, $\overline{CP_1}$) and an overriding asynchronous Master Reset Input (MR).

The counter is advanced by either a LOW-to-HIGH transition at CP_0 while $\overline{CP_1}$ is LOW or a HIGH-to-LOW transition at $\overline{CP_1}$ while CP_0 is HIGH (see Functional Truth Table). When cascading 34017 counters, the $\overline{Q_{5-9}}$ output, which is LOW while the counter is in states 5, 6, 7, 8 and 9, can be used to drive the CP_0 input of the next 34017.

A HIGH on the Master Reset Input (MR) resets the counter to zero (O_0 = $\overline{Q_{5-9}}$ = HIGH, O_1-O_9 = LOW) independent of the Clock Inputs (CP_0, $\overline{CP_1}$).

- **TYPICAL COUNT FREQUENCY OF 13.8 MHz AT V_{DD} = 10 V**
- **ACTIVE HIGH DECODED OUTPUTS**
- **TRIGGERS ON EITHER A HIGH-TO-LOW OR LOW-TO-HIGH TRANSITION**
- **CASCADABLE**

PIN NAMES

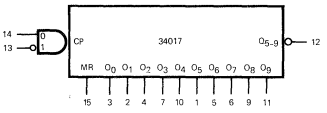
CP_0	Clock Input (L→H Triggered)
$\overline{CP_1}$	Clock Input (H→L Triggered)
MR	Master Reset Input
O_0-O_9	Decoded Outputs
$\overline{Q_{5-9}}$	Carry Output (Active LOW)

FUNCTIONAL TRUTH TABLE

MR	CP_0	$\overline{CP_1}$	OPERATION
H	X	X	$O_0 = \overline{Q_{5-9}} = H$; O_1-O_9 = L
L	H	H→L	Counter Advances
L	L→H	L	Counter Advances
L	L	X	No Change
L	X	H	No Change
L	H	L→H	No Change
L	H→L	L	No Change

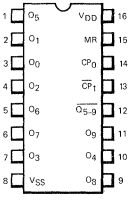
H = HIGH Level
L = LOW Level
L→H = LOW-to-HIGH Transition
H→L = HIGH-to-LOW Transition
X = Don't Care

LOGIC SYMBOL



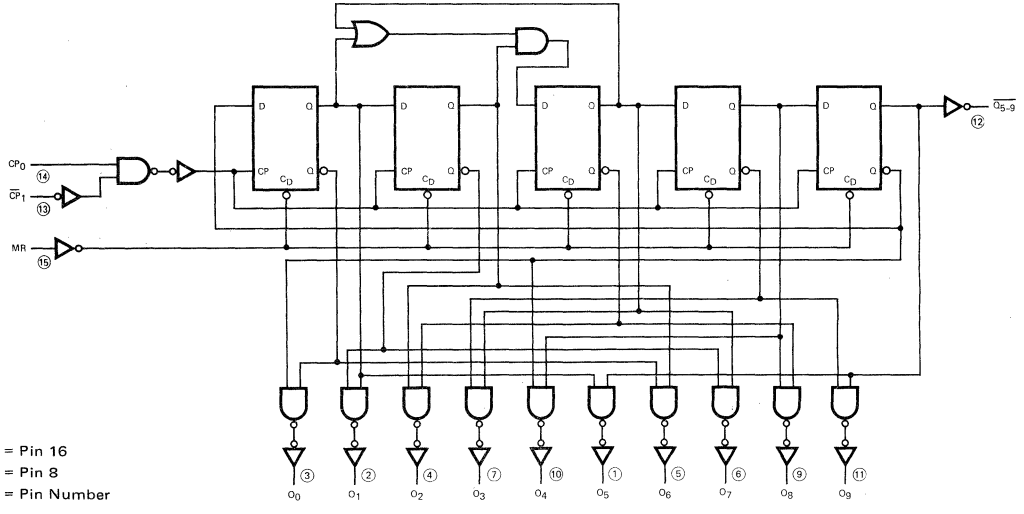
V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Number

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			50			100		20		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					700			1400		280			MAX	
		XM			5			10		2		μA	MIN, 25°C	
					300			600		120			MAX	

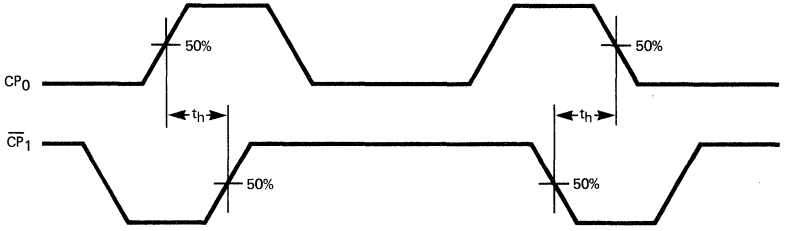
NOTE: Additional DC Characteristics are listed in this section under 34000 Series CMOS Family Characteristics.

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, CP_0 or $\overline{CP}_1$ to O_n		262			104			76		ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
t_{PHL}			197			86			61		ns	
t_{PLH}	Propagation Delay, CP_0 or $\overline{CP}_1$ to $\overline{Q}_{5-9}$		189			80			57		ns	
t_{PHL}			240			96			67		ns	
t_{PHL}	Propagation Delay, MR to O_n		151			62			45		ns	
t_{PLH}	Propagation Delay, MR to $\overline{Q}_{5-9}$		102			42			34		ns	
t_{TLH}	Output Transition Time		32			16			13		ns	
t_{THL}			27			13			10		ns	
t_{PLH}	Propagation Delay, CP_0 or $\overline{CP}_1$ to O_n		278			114			82		ns	C_L = 50 pF Input Transition Times ⩽ 20 ns
t_{PHL}			226			94			67		ns	
t_{PLH}	Propagation Delay, CP_0 or $\overline{CP}_1$ to $\overline{Q}_{5-9}$		205			87			63		ns	
t_{PHL}			261			105			73		ns	
t_{PHL}	Propagation Delay, MR to O_n		170			80			52		ns	
t_{PLH}	Propagation Delay, MR to $\overline{Q}_{5-9}$		125			65			40		ns	
t_{TLH}	Output Transition Time		59			31			23		ns	
t_{THL}			63			26			19		ns	
t_wCP	Min. CP_0 or $\overline{CP}_1$ Pulse Width		85			37			28		ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
t_wMR	Minimum MR Pulse Width		52			22			18		ns	
t_{rec}	MR Recovery Time		16			6			3		ns	
t_h	Hold Time, CP_0 to $\overline{CP}_1$		90			39			26		ns	
t_h	Hold Time, $\overline{CP}_1$ to CP_0		89			39			22		ns	
f_{MAX}	Input Count Frequency (Note 3)		5.8			13.8					MHz	

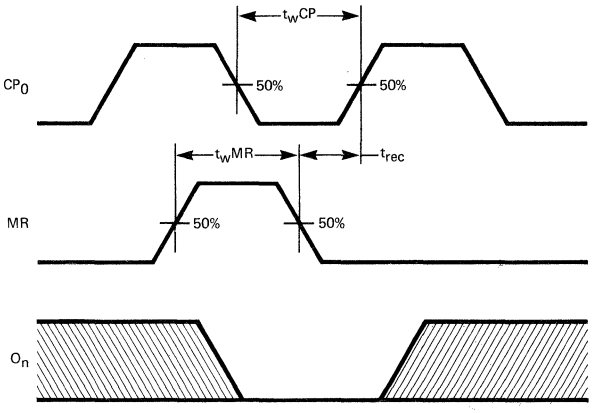
NOTES:
1. Propagation Delays and Output Transition Times are graphically described in this section under 34000 Series CMOS Family Characteristics.
2. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Hold Times (t_h) Recovery Times (t_{rec}), and Minimum Pulse Widths (t_w), do not vary with load capacitance.
3. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
4. It is recommended that input rise and fall times to either Clock Input (CP_0 or $\overline{CP}_1$) be less than 15 μs.

SWITCHING WAVEFORMS



HOLD TIMES, CP_0 TO $\overline{CP}_1$ AND $\overline{CP}_1$ TO CP_0

Hold Times are shown as positive values, but may be specified as negative values.



MINIMUM PULSE WIDTHS FOR CP AND MR AND RECOVERY TIME FOR MR

CONDITIONS: $\overline{CP}_1$ = LOW while CP_0 is triggered on a LOW-to-HIGH transition. t_wCP and t_{rec} also apply when CP_0 = HIGH and $\overline{CP}_1$ is triggered on a HIGH-to-LOW transition.

34019
QUAD 2-INPUT MULTIPLEXER

DESCRIPTION – The 34019 provides four multiplexing circuits with common selection inputs; each circuit contains two inputs and one output. It may be used to select four bits of information from one of two sources. The A inputs are selected when S_A is HIGH, the B inputs when S_B is HIGH. When S_A and S_B are HIGH, output (Z_n) is the logical OR of the A_n and B_n inputs ($Z_n = A_n + B_n$). When S_A and S_B are LOW, output (Z_n) is LOW independent of the multiplexer inputs (A_n and B_n). The 34019 cannot be used to multiplex analog signals. The outputs utilize standard buffers for best performance.

PIN NAMES

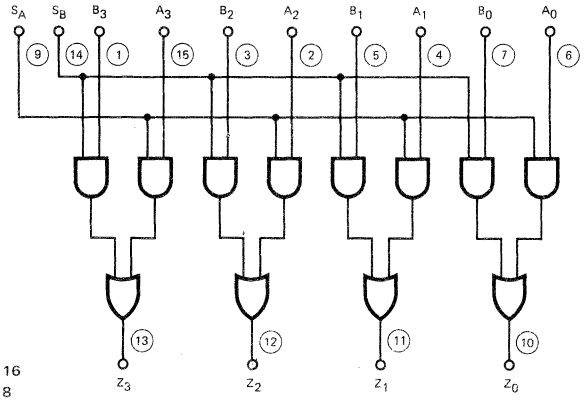
S_A, S_B	Select Inputs (Active HIGH)
$A_0 - A_3$, $B_0 - B_3$	Multiplexer Inputs
$Z_0 - Z_3$	Multiplexer Outputs

TRUTH TABLE

SELECT		INPUTS		OUTPUT
S_A	S_B	A_n	B_n	Z_n
L	L	X	X	L
H	L	L	X	L
H	L	H	X	H
L	H	X	L	L
L	H	X	H	H
H	H	H	X	H
H	H	X	H	H
H	H	L	L	L

H = HIGH Level
L = LOW Level
X = Don't Care

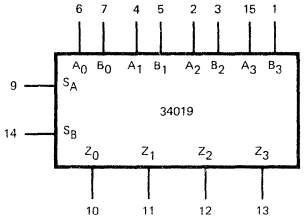
LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
◯ = Pin Number

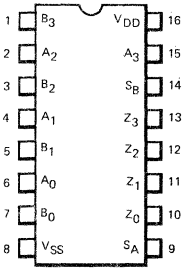
$Z_n = S_A A_n + S_B B_n$

LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			30			60		12		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					600			1200		24			MAX	
		XM			5			10		2		μA	MIN, 25°C	
					100			200		40			MAX	

NOTE: Additional DC Characteristics are listed in this section under 34000 Series CMOS Family Characteristics.

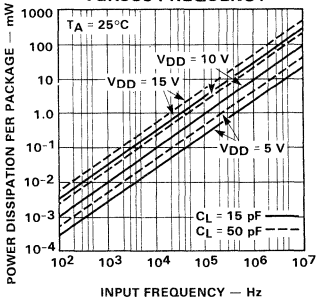
AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay,		50	100		20	45		16		ns	
t_{PHL}	S_A,S_B, A_n or B_n to Z_n		50	110		25	55		20		ns	C_L = 15 pF
t_{TLH}	Output Transition		40	75		20	40		15	25	ns	Input Transition Times ⩽ 20 ns
t_{THL}	Time		45	75		22	40		15	25	ns	
t_{PLH}	Propagation Delay,		75	150		35	70		24		ns	
t_{PHL}	S_A,S_B, A_n or B_n to Z_n		85	160		37	75		29		ns	C_L = 50 pF
t_{TLH}	Output Transition		80	135		42	70		32	45	ns	Input Transition Times ⩽ 20 ns
t_{THL}	Time		90	135		40	70		30	45	ns	

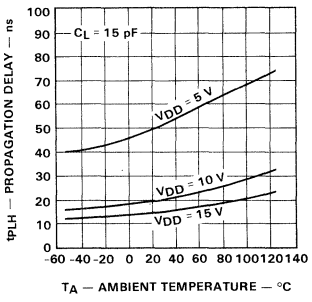
NOTE:
1. Propagation Delays and Output Transition Times are graphically described in this section under 34000 Series CMOS Family Characteristics.

TYPICAL ELECTRICAL CHARACTERISTICS

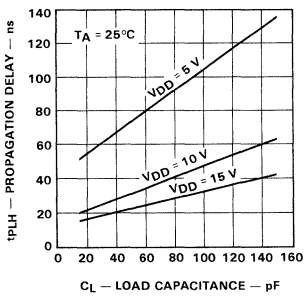
POWER DISSIPATION VERSUS FREQUENCY



PROPAGATION DELAY VERSUS TEMPERATURE



PROPAGATION DELAY VERSUS LOAD CAPACITANCE



34020
14-STAGE BINARY COUNTER

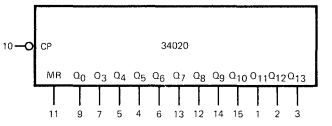
DESCRIPTION — The 34020 is a 14-Stage Binary Ripple Counter with a Clock Input ($\overline{CP}$), an overriding asynchronous Master Reset Input (MR) and twelve fully buffered Outputs (Q_0, Q_3-Q_{13}). The counter advances on the HIGH-to-LOW transition of the Clock Input ($\overline{CP}$). A HIGH on the Master Reset Input (MR) clears all counter stages and forces all Outputs (Q_0, Q_3-Q_{13}) LOW, independent of the Clock Input ($\overline{CP}$).

- **25 MHz TYPICAL COUNT FREQUENCY AT V_{DD} = 10 V**
- **COMMON ASYNCHRONOUS MASTER RESET**
- **FULLY BUFFERED OUTPUTS FROM THE FIRST STAGE AND THE LAST ELEVEN STAGES**

PIN NAMES

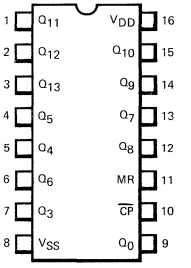
$\overline{CP}$	Clock Input (H→L Triggered)
MR	Master Reset Input (Active HIGH)
Q_0, Q_3-Q_{13}	Parallel Outputs

LOGIC SYMBOL



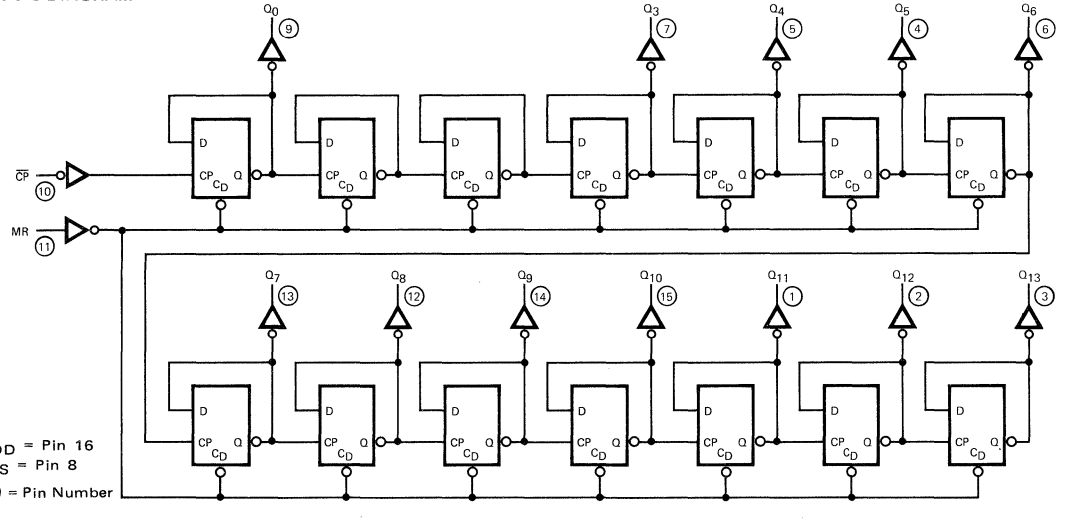
V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
◯ = Pin Number

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			50			100		20		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					700			1400		280			MAX	
		XM			15			25		5		μA	MIN, 25°C	
					900			1500		300			MAX	

NOTE: Additional DC Characteristics are listed in this section under 34000 Series CMOS Family Characteristics.

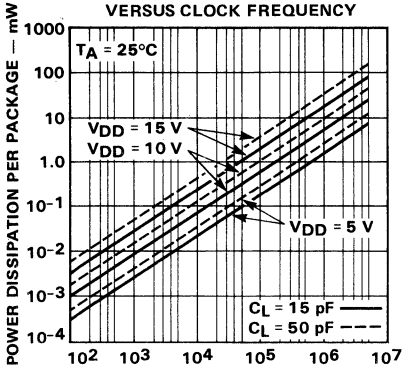
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, $\overline{CP}$ to Q_0		110	220		45	90		30		ns	C_L = 15 pF Input Transition Times ≤ 20 ns
t_{PHL}			85	170		37	75		25		ns	
t_{PHL}	Propagation Delay, MR to Q_n		150	300		65	130		43		ns	
t_{TLH}	Output Transition Time		30	75		13	40		10	25	ns	
t_{THL}			30	75		13	40		10	25	ns	
t_{PLH}	Propagation Delay, $\overline{CP}$ to Q_0		130	260		55	110		37		ns	C_L = 50 pF Input Transition Times ≤ 20 ns
t_{PHL}			110	220		45	90		33		ns	
t_{PHL}	Propagation Delay, MR to Q_n		180	360		75	150		50		ns	
t_{TLH}	Output Transition Time		65	135		35	70		25	45	ns	
t_{THL}			65	135		35	70		25	45	ns	
$t_W\overline{CP}(H)$	Minimum Clock Pulse Width	100	50		40	20			16		ns	C_L = 15 pF Input Transition Times ≤ 20 ns
$t_W MR(H)$	Minimum MR Pulse Width	140	70		55	27			20		ns	
t_{rec}	Recovery Time for MR	85	43		35	17			12		ns	
f_{MAX}	Input Clock Frequency (Note 2)	5	10		12	25					MHz	

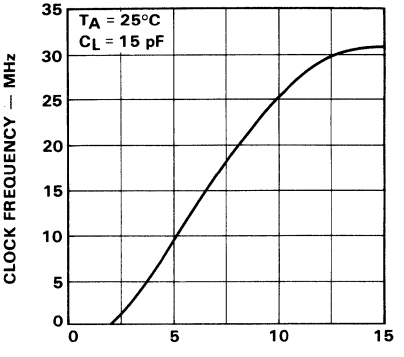
NOTES:
1. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Recovery Times (t_{rec}) and Minimum Pulse Widths (t_W) do not vary with load capacitance.
2. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
3. It is recommended that input rise and fall times to the Clock Input be less than 15 μs.

TYPICAL ELECTRICAL CHARACTERISTICS

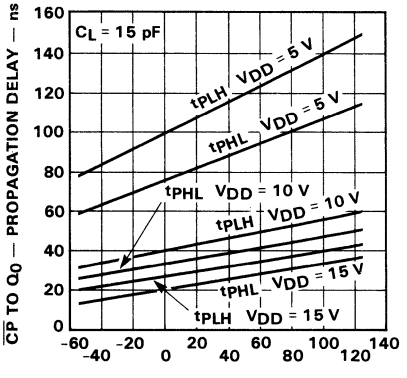
POWER DISSIPATION
VERSUS CLOCK FREQUENCY



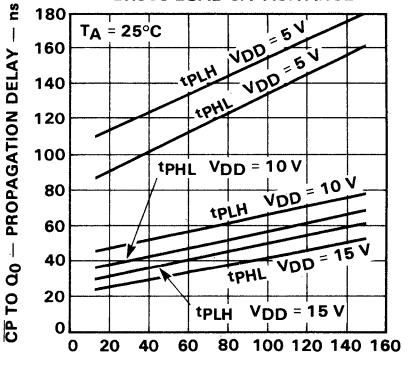
CLOCK FREQUENCY
VERSUS
POWER SUPPLY VOLTAGE



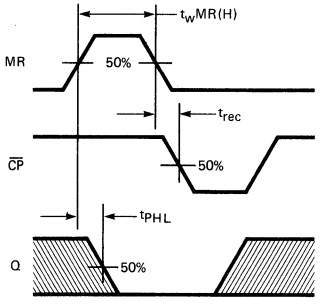
PROPAGATION DELAY
VERSUS TEMPERATURE



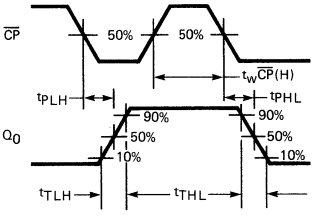
PROPAGATION DELAY
VERSUS LOAD CAPACITANCE



SWITCHING WAVEFORMS



PROPAGATION DELAY MASTER
RESET TO OUTPUT, MINIMUM MASTER RESET
PULSE WIDTH AND RECOVERY TIME FOR MASTER RESET



PROPAGATION DELAY CLOCK TO
OUTPUT Q_0, OUTPUT TRANSITION
TIMES AND MINIMUM CLOCK PULSE WIDTH

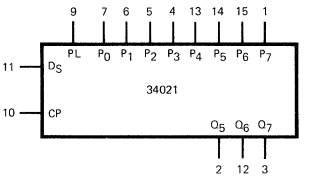
34021
8-BIT SHIFT REGISTER

DESCRIPTION — The 34021 is an edge-triggered 8-Bit Shift Register (Parallel-to-Serial Converter) with a synchronous Serial Data Input (D_S), a Clock Input (CP), an asynchronous active HIGH Parallel Load Input (PL), eight asynchronous Parallel Data Inputs (P_0–P_7) and Buffered Parallel Outputs from the last three stages (Q_5–Q_7).

Information on the Parallel Data Inputs (P_0–P_7) is asynchronously loaded into the register while the Parallel Load Input (PL) is HIGH, independent of the Clock (CP) and Serial Data (D_S) inputs. Data present in the register is stored on the HIGH-to-LOW transition of the Parallel Load Input.(PL).

When the Parallel Load Input is LOW, data on the Serial Data Input (D_S) is shifted into the first register position and all the data in the register is shifted one position to the right on the LOW-to-HIGH transition of the Clock Input (CP).

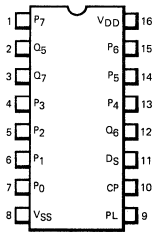
LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

- **TYPICAL SHIFT FREQUENCY OF 18.1 MHz AT V_{DD} = 10 V**
- **PARALLEL-TO-SERIAL DATA TRANSFER**
- **BUFFERED OUTPUTS AVAILABLE LAST THREE STAGES**
- **CLOCK INPUT IS L → H EDGE-TRIGGERED**

CONNECTION DIAGRAM
DIP (TOP VIEW)

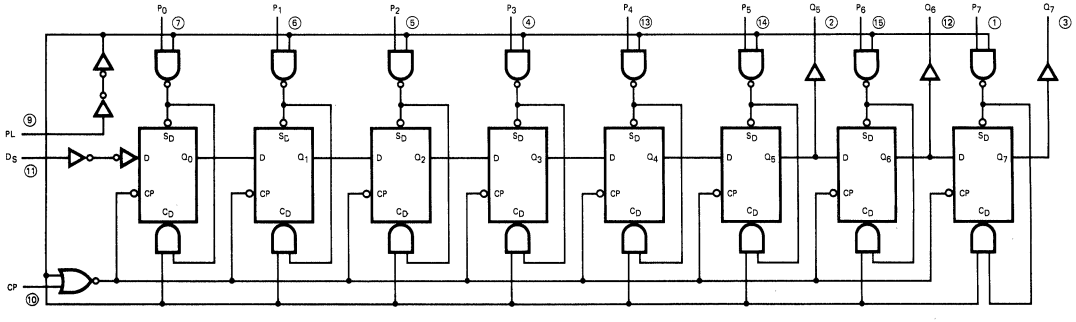


NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

PL	Parallel Load Input
P_0–P_7	Parallel Data Inputs
D_S	Serial Data Input
CP	Clock Input (L→H Edge-Triggered)
Q_5–Q_7	Buffered Parallel Outputs from the Last Three Stages

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Number

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			50			100		20		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					600			1200		240			MAX	
		XM			5			10		2		μA	MIN, 25°C	
					300			600		120			MAX	

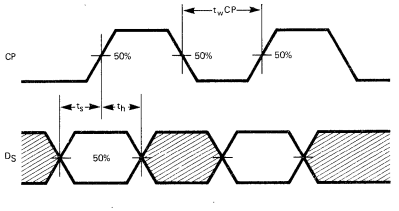
NOTE: Additional DC Characteristics are listed in this section under 34000 Series CMOS Family Characteristics.

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C

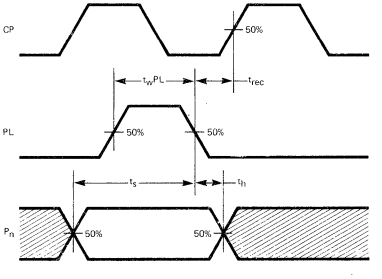
SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, CP to Q_n		119			51			34		ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
t_{PHL}			161			64			43		ns	
t_{PLH}	Propagation Delay, PL to Q_n		172			70			48		ns	
t_{PHL}			150			96			66		ns	
t_{TLH}	Output Transition Time		28			15			10		ns	
t_{THL}			32			14			9		ns	
t_{PLH}	Propagation Delay, CP to Q_n		134			59			40		ns	C_L = 50 pF Input Transition Times ⩽ 20 ns
t_{PHL}			184			74			49		ns	
t_{PLH}	Propagation Delay, PL to Q_n		188			78			54		ns	
t_{PHL}			274			105			72		ns	
t_{TLH}	Output Transition Time		58			31			22		ns	
t_{THL}			69			27			22		ns	
t_wCP	CP Minimum Pulse Width		61			21			14		ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
t_wPL	PL Minimum Pulse Width		67			24			16		ns	
t_{rec}	PL Recovery Time		71			28			21		ns	
t_s	Set-Up Time D_S to CP		51			16			12		ns	
t_h	Hold Time D_S to CP		49			15			11		ns	
t_s	Set-Up Time P_n to PL		78			28			18		ns	
t_h	Hold Time, P_n to PL		72			26			16		ns	
f_{MAX}	Shift Frequency (Note 3)		7.8			18.1					MHz	

NOTES:
1. Propagation Delays and Output Transition Times are graphically described in this section under 34000 Series CMOS Family Characteristics.
2. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Set-up Times (t_s), Hold Times (t_h), Recovery Times (t_{rec}), and Minimum Pulse Widths (t_w), do not vary with load capacitance.
3. For f_{MAX} input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
4. It is recommended that input rise and fall times to the Clock Input be less than 15 μs.

SWITCHING WAVEFORMS



MINIMUM CLOCK PULSE WIDTH AND SET-UP AND HOLD TIMES, D_S TO CP



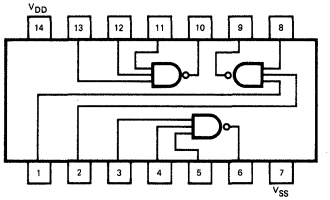
MINIMUM PL PULSE WIDTH, RECOVERY TIME FOR PL, AND SET-UP AND HOLD TIMES, P_n TO PL

NOTE: Set-up and Hold Times are shown as positive values but may be specified as negative values.

TRIPLE 3-INPUT NAND GATE

DESCRIPTION — This CMOS logic element provides a 3-input positive NAND function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V

SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V MIN	TYP	MAX	LIMITS V_{DD} = 10 V MIN	TYP	MAX	LIMITS V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEMP	TEST CONDITIONS
I_{DD}	Quiescent Power Supply Current	XC			0.5			5.0		1.0		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					15.0			30.0		6.0			MAX	
		XM			0.05			0.1		0.02		μA	MIN, 25°C	
					3.0			6.0		1.2			MAX	

NOTE: Additional DC Characteristics are listed in this section under 34000 Series CMOS Family Characteristics.

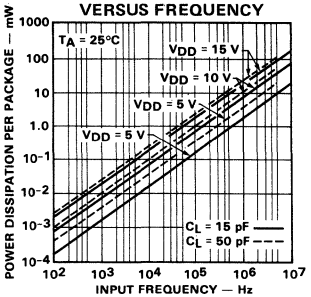
AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C

SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V MIN	TYP	MAX	LIMITS V_{DD} = 10 V MIN	TYP	MAX	LIMITS V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEST CONDITIONS
t_{PLH}	Propagation Delay		35	75		20	40		15		ns	
t_{PHL}			35	75		20	40		9		ns	C_L = 15 pF
t_{TLH}	Output Transition		19	75		9	40		6	25	ns	Input Transition Times ⩽ 20 ns
t_{THL}	Time		19	75		7	40		5	25	ns	
t_{PLH}	Propagation Delay		45	110		25	60		19		ns	
t_{PHL}			51	110		25	60		12		ns	C_L = 50 pF
t_{TLH}	Output Transition		45	135		18	70		17	45	ns	Input Transition Times ⩽ 20 ns
t_{THL}	Time		45	135		18	70		12	45	ns	

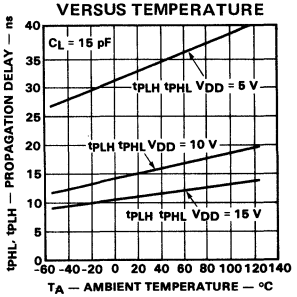
NOTE: Propagation delays and output transition times are graphically described in this section under 34000 Series CMOS Family Characteristics.

TYPICAL ELECTRICAL CHARACTERISTICS

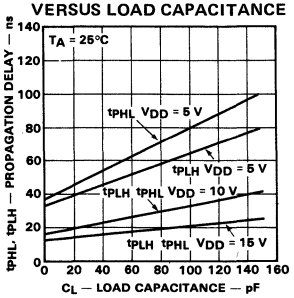
POWER DISSIPATION VERSUS FREQUENCY



PROPAGATION DELAY VERSUS TEMPERATURE



PROPAGATION DELAY VERSUS LOAD CAPACITANCE

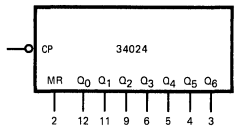


34024
7-STAGE BINARY COUNTER

DESCRIPTION – The 34024 is a 7-Stage Binary Ripple Counter with a Clock Input ($\overline{CP}$), an overriding asynchronous Master Reset Input (MR) and seven fully Buffered Parallel Outputs (Q_0-Q_6). The counter advances on the HIGH-to-LOW transition of the Clock Input ($\overline{CP}$). A HIGH on the Master Reset Input (MR) clears all counter stages and forces all Outputs (Q_0-Q_6) LOW, independent of the Clock Input ($\overline{CP}$).

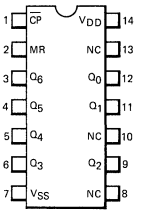
- **TYPICAL COUNT FREQUENCY OF 30 MHz AT V_{DD} = 10 V**
- **CLOCK TRIGGERED ON THE HIGH-TO-LOW TRANSITION**
- **ASYNCHRONOUS ACTIVE HIGH MASTER RESET**
- **OUTPUTS AVAILABLE FROM ALL SEVEN STAGES**

LOGIC SYMBOL



V_{DD} = Pin 14
V_{SS} = Pin 7
NC = Pins 8, 10 and 13

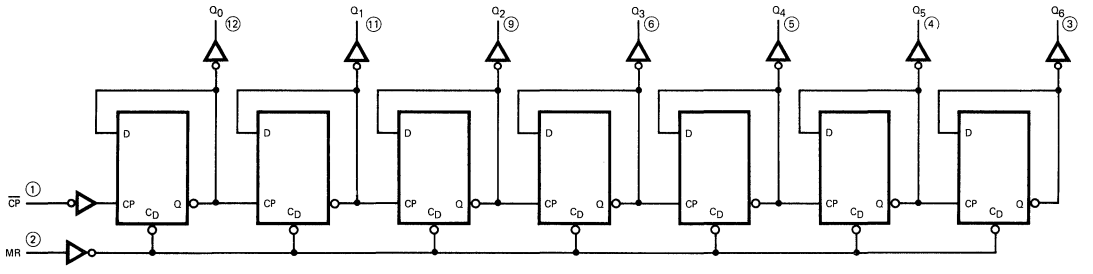
CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

$\overline{CP}$	Clock Input (H→L Triggered)
MR	Master Reset Input
Q_0-Q_6	Buffered Parallel Outputs



V_{DD} = Pin 14
V_{SS} = Pin 7
○ = Pin Number
NC = Pins 8, 10 and 13

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			50			100		20		µA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					700			1400		280			MAX	
		XM			5			10		2		µA	MIN, 25°C	
					300			600		120			MAX	

NOTE: Additional DC Characteristics are listed in this section under 34000 Series CMOS Family Characteristics.

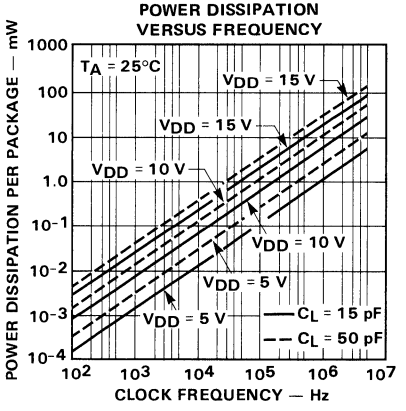
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, $\overline{CP}$ to Q_0		82	165		37	75		23		ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
t_{PHL}			75	150		35	70		20		ns	
t_{PHL}	Propagation Delay, MR to Q_n		105	210		42	85		30		ns	
t_{TLH}	Output Transition Time		25	75		13	40		10	25	ns	
t_{THL}			25	75		13	40		10	25	ns	
t_{PLH}	Propagation Delay, $\overline{CP}$ to Q_0		100	200		45	90		30		ns	C_L = 50 pF Input Transition Times ⩽ 20 ns
t_{PHL}			97	195		40	80		25		ns	
t_{PHL}	Propagation Delay, MR to Q_n		130	260		50	100		35		ns	
t_{TLH}	Output Transition Time		60	130		30	70		25	45	ns	
t_{THL}			60	130		30	70		25	45	ns	
$t_w\overline{CP}$	$\overline{CP}$ Minimum Pulse Width	90	45		35	17			13		ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
t_wMR	MR Minimum Pulse Width	80	40		30	15			12		ns	
t_{rec}	MR Recovery Time	60	30		25	12			9		ns	
f_{MAX}	Input Count Frequency (Note 3)	6	12		15	30					MHz	

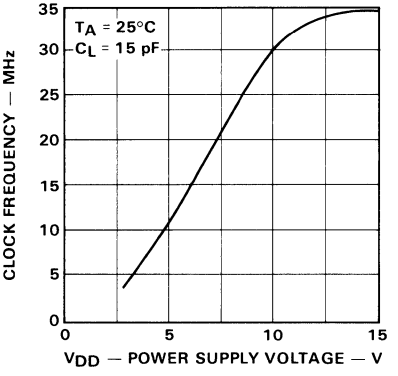
NOTES:
1. Propagation Delays and Output Transition Times are graphically described in this section under 34000 Series CMOS Family Characteristics.
2. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Recovery Times (t_{rec}) and Minimum Pulse Widths (t_w) do not vary with load capacitance.
3. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
4. It is recommended that input rise and fall times to the Clock Input be less than 15 µs.

TYPICAL ELECTRICAL CHARACTERISTICS

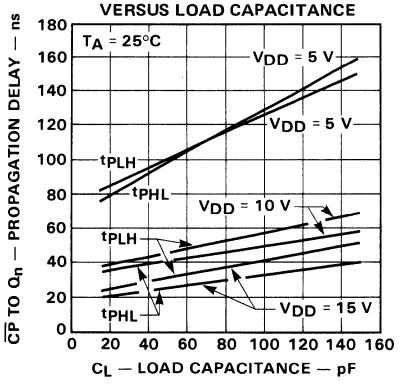
POWER DISSIPATION VERSUS FREQUENCY



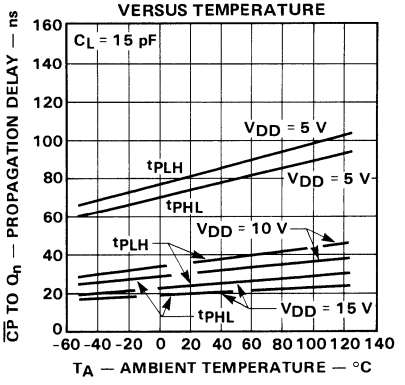
CLOCK FREQUENCY VERSUS POWER SUPPLY VOLTAGE



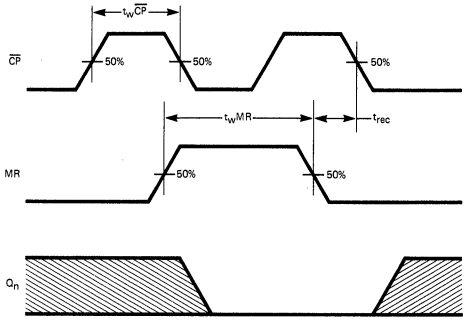
PROPAGATION DELAY VERSUS LOAD CAPACITANCE



PROPAGATION DELAY VERSUS TEMPERATURE



SWITCHING WAVEFORMS

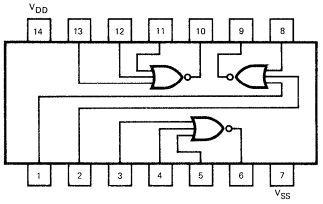


MINIMUM PULSE WIDTH FOR $\overline{CP}$ AND MR AND MR RECOVERY TIME

TRIPLE 3-INPUT NOR GATE

DESCRIPTION — This CMOS logic element provides a 3-input positive NOR function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			0.5			5.0		1.0		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					15.0			30.0		6.0			MAX	
		XM			0.05			0.1		0.02		μA	MIN, 25°C	
					3.0			6.0		1.2			MAX	

NOTE: Additional DC Characteristics are listed in this section under 34000 Series CMOS Family Characteristics.

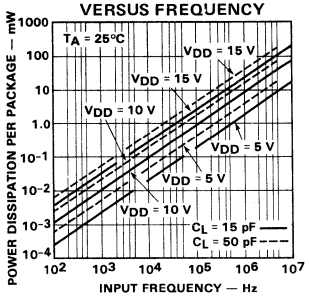
AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay		30	75		13	40		12		ns	
t_{PHL}			35	75		20	40		16		ns	C_L = 15 pF
t_{TLH}	Output Transition		15	75		8	40		6	25	ns	Input Transition Times ⩽ 20 ns
t_{THL}	Time		16	75		6	40		4	25	ns	
t_{PLH}	Propagation Delay		45	110		20	60		15		ns	
t_{PHL}			47	110		25	60		21		ns	C_L = 50 pF
t_{TLH}	Output Transition		38	135		20	70		15	45	ns	Input Transition Times ⩽ 20 ns
t_{THL}	Time		38	135		15	70		11	45	ns	

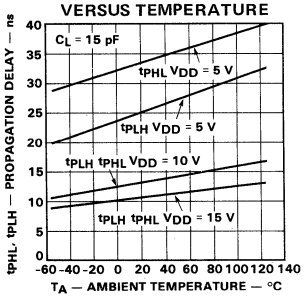
NOTE: Propagation delays and output transition times are graphically described in this section under 34000 Series CMOS Family Characteristics.

TYPICAL ELECTRICAL CHARACTERISTICS

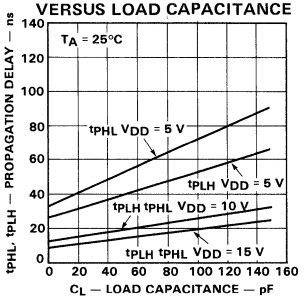
POWER DISSIPATION VERSUS FREQUENCY



PROPAGATION DELAY VERSUS TEMPERATURE



PROPAGATION DELAY VERSUS LOAD CAPACITANCE



34027
DUAL JK FLIP-FLOP

DESCRIPTION – The 34027 is a Dual JK Flip-Flop which is edge-triggered and features independent Direct Set, Direct Clear, and Clock inputs. Data is accepted when the Clock is LOW and transferred to the output on the positive-going edge of the Clock. The active HIGH asynchronous Clear Direct (C_D) and Set Direct (S_D) are independent and override the J, K, or Clock inputs. The outputs are buffered for best system performance.

PIN NAMES

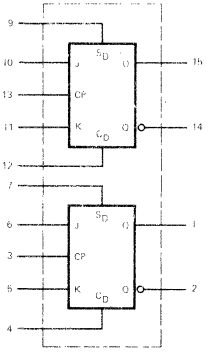
J, K	Synchronous Inputs
CP	Clock Input (L → H Edge-Triggered)
S_D	Asynchronous Direct Set Input (Active HIGH)
C_D	Asynchronous Direct Clear Input (Active HIGH)
Q	True Output
$\overline{Q}$	Complement Output

TRUTH TABLE

INPUTS					OUTPUTS	
S_D	C_D	CP	J	K	Q_{n+1}	$\overline{Q}_{n+1}$
H	L	X	X	X	H	L
L	H	X	X	X	L	H
H	H	X	X	X	H	H
L	L	⌐	L	L	NO CHANGE	
L	L	⌐	H	L	H	L
L	L	⌐	L	H	L	H
L	L	⌐	H	H	$\overline{Q}_n$	Q_n

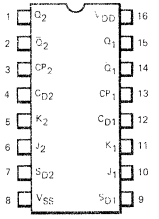
L = LOW Level
H = HIGH Level
⌐ = Positive -Going Transition
X = Don't Care
Q_{n+1} = State After Clock Positive Transition

LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAMS
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			10			20		4		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					140			280		56			MAX	
		XM			1			2		0.4		μA	MIN, 25°C	
					60			120		24			MAX	

NOTE: Additional DC Characteristics are listed in this section under 34000 Series CMOS Family Characteristics.

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C

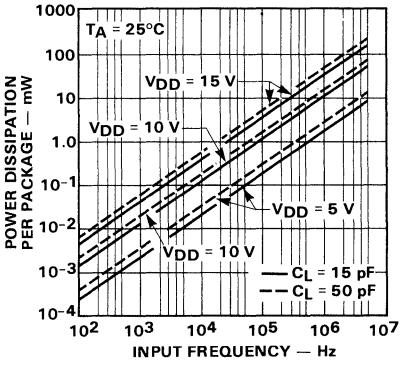
SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, CP to Q, $\overline{Q}$		75	150		35	75		25		ns	C_L = 15 pF
t_{PHL}			75	150		35	75		25		ns	
t_{PLH}	Propagation Delay, S_D to Q		160	300		80	150		60		ns	Input Transition Times ⩽ 20 ns
t_{PHL}	Propagation Delay, C_D to Q		160	300		80	150		60		ns	
t_{TLH}	Output Transition Time		50	100		30	60		20	40	ns	
t_{THL}			50	100		30	60		20	40	ns	
t_{PLH}	Propagation Delay, CP to Q, $\overline{Q}$		100	200		45	85		30		ns	C_L = 50 pF
t_{PHL}			100	200		45	85		30		ns	
t_{PLH}	Propagation Delay, S_D to Q		180	350		90	175		75		ns	Input Transition Times ⩽ 20 ns
t_{PHL}	Propagation Delay, C_D to Q		180	350		90	175		75		ns	
t_{TLH}	Output Transition Time		85	150		45	85		30	50	ns	
t_{THL}			85	150		45	85		30	50	ns	
t_s	Set-Up Time, J, K to CP	100	45		40	20			15		ns	
t_h	Hold Time, J, K to CP	0	-25		0	-10			-5		ns	
t_wCP(L)	Minimum Clock Pulse Width	150	75		70	35			25		ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
t_w S_D(H)	Minimum S_D Pulse Width	150	75		60	30			25		ns	
t_w C_D(H)	Minimum C_D Pulse Width	150	75		60	30			25		ns	
t_{rec} S_D	Recovery Time for S_D	0	-5		0	-4			-3		ns	
t_{rec} C_D	Recovery Time for C_D	0	-5		0	-4			-3		ns	
f_{MAX}	Maximum CP Frequency (Note 2)	4	8		8	16					MHz	

NOTES:

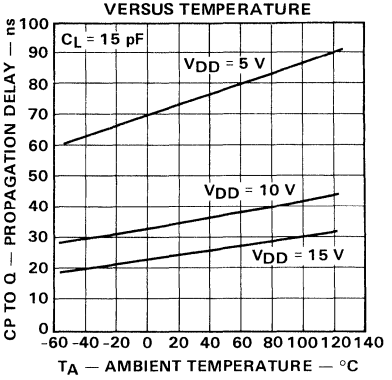
1. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Set-up Times (t_s), Hold Times (t_h), Recovery Times (t_{rec}), and Minimum Pulse Widths (t_w) do not vary with load capacitance.
2. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
3. Propagation Delays and Output Transition Times are graphically described in this section under 34000 Series CMOS Family Characteristics.
4. It is recommended that input rise and fall times to the Clock Input be less than 15 μs.

TYPICAL ELECTRICAL CHARACTERISTICS

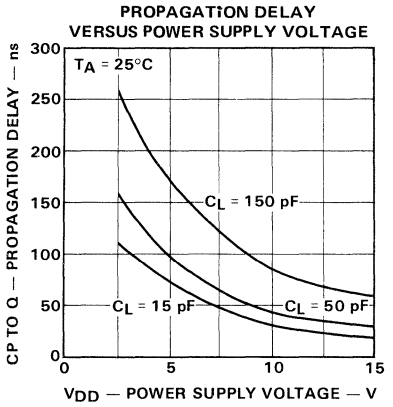
POWER DISSIPATION VERSUS FREQUENCY



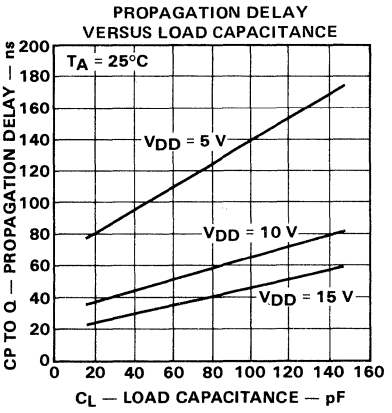
PROPAGATION DELAY VERSUS TEMPERATURE



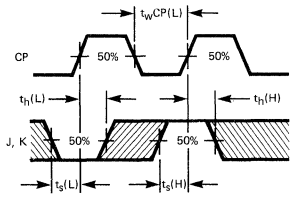
PROPAGATION DELAY VERSUS POWER SUPPLY VOLTAGE



PROPAGATION DELAY VERSUS LOAD CAPACITANCE

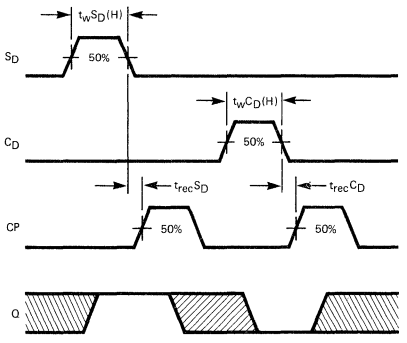


SWITCHING WAVEFORMS



NOTE:
t_s & t_h are shown as positive values but may be specified as negative values.

SET-UP TIMES, HOLD TIMES, AND MINIMUM CLOCK PULSE WIDTH



RECOVERY TIME FOR S_D, RECOVERY TIME FOR C_D, MINIMUM S_D PULSE WIDTH, AND MINIMUM C_D PULSE WIDTH

34028
1-OF-10 DECODER

DESCRIPTION – The 34028 is a CMOS 4-bit BCD to 1-of-10 active HIGH decoder. A 1-2-4-8 BCD code applied to inputs A_0 through A_3 causes the selected output to be HIGH, the other nine will be LOW. If desired, the 34028 may be used as a 1-of-8 decoder with enable; 3-bit octal inputs are applied to inputs A_0, A_1, and A_2 selecting an output 0 through 7. Input A_3 then becomes an active LOW enable, forcing the selected output LOW when A_3 is HIGH. The 34028 may also be used as an 8-input demultiplexer with an active LOW data input. The outputs are fully buffered for best performance.

- **BCD TO 1-OF-10 DECODER**
- **1-OF-8 DECODER WITH ACTIVE LOW ENABLE**
- **8-INPUT DEMULTIPLEXER WITH ACTIVE LOW DATA INPUT**

PIN NAMES

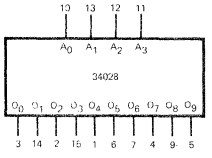
$A_0 - A_3$	Address Inputs, 1-2-4-8 BCD
$O_0 - O_9$	Outputs (Active HIGH)

TRUTH TABLE

INPUTS				OUTPUTS									
A_3	A_2	A_1	A_0	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7	O_8	O_9
L	L	L	L	H	L	L	L	L	L	L	L	L	L
L	L	L	H	L	H	L	L	L	L	L	L	L	L
L	L	H	L	L	L	H	L	L	L	L	L	L	L
L	L	H	H	L	L	L	H	L	L	L	L	L	L
L	H	L	L	L	L	L	L	H	L	L	L	L	L
L	H	L	H	L	L	L	L	L	H	L	L	L	L
L	H	H	L	L	L	L	L	L	L	H	L	L	L
L	H	H	H	L	L	L	L	L	L	L	H	L	L
H	L	L	L	L	L	L	L	L	L	L	L	H	L
H	L	L	H	L	L	L	L	L	L	L	L	L	H
H	L	H	L	L	L	L	L	L	L	L	L	H	L
H	L	H	H	L	L	L	L	L	L	L	L	L	H
H	H	L	L	L	L	L	L	L	L	L	L	H	L
H	H	L	H	L	L	L	L	L	L	L	L	L	H
H	H	H	L	L	L	L	L	L	L	L	L	H	L
H	H	H	H	L	L	L	L	L	L	L	L	L	H

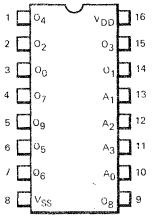
H = HIGH Level
L = LOW Level

LOGIC SYMBOL



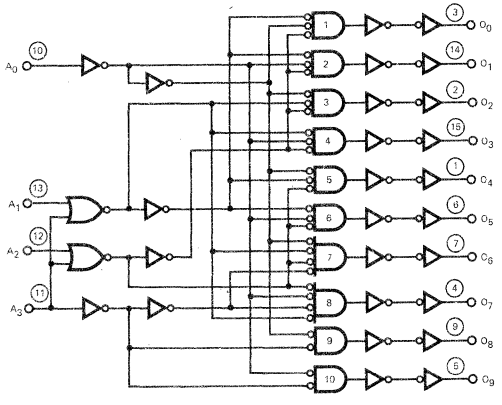
V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Number

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			30			60		12		µA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					600			1200		240			MAX	
		XM			5			10		2		µA	MIN, 25°C	
					100			200		40			MAX	

NOTE: Additional DC Characteristics are listed in this section under 34000 Series CMOS Family Characteristics.

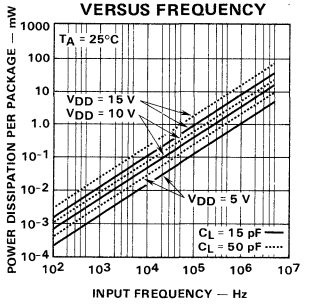
AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay,		145	290		60	130		37		ns	
t_{PHL}	A_n to O_n		125	290		45	130		30		ns	C_L = 15 pF
t_{TLH}	Output Transition		40	100		20	60		15	40	ns	Input Transition Times ⩽ 20 ns
t_{THL}	Time		40	100		20	60		15	40	ns	
t_{PLH}	Propagation Delay,		167	325		66	145		45		ns	
t_{PHL}	A_n to O_n		157	325		57	145		40		ns	C_L = 50 pF
t_{TLH}	Output Transition		85	200		40	100		31	70	ns	Input Transition Times ⩽ 20 ns
t_{THL}	Time		110	200		37	100		25	70	ns	

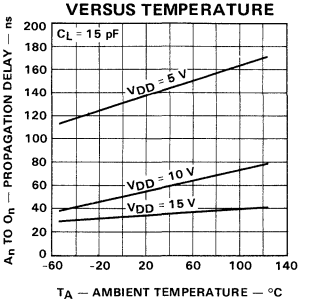
NOTE:
1. Propagation Delays and Output Transition Times are graphically described in this section under 34000 Series CMOS Family Characteristics.

TYPICAL ELECTRICAL CHARACTERISTICS

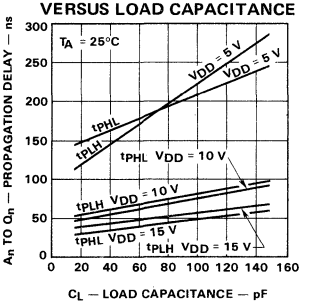
POWER DISSIPATION VERSUS FREQUENCY



PROPAGATION DELAY VERSUS TEMPERATURE



PROPAGATION DELAY VERSUS LOAD CAPACITANCE



34029
SYNCHRONOUS UP/DOWN COUNTER

DESCRIPTION — The 34029 is a Synchronous Edge-Triggered Up/Down 4-Bit Binary/BCD Decade Counter with a Clock Input (CP), an active LOW Count Enable Input ($\overline{CE}$), an Up/Down Control Input (UP/$\overline{DN}$), a Binary/Decade Control Input (BIN/$\overline{DEC}$), an overriding asynchronous active HIGH Parallel Load Input (PL), four Parallel Data Inputs (P_0-P_3), four Parallel Buffered Outputs (Q_0-Q_3) and an active LOW Terminal Count Output ($\overline{TC}$).

Information on the Parallel Inputs (P_0-P_3) is loaded into the counter while the Parallel Load Input (PL) is HIGH, independent of all other input conditions. With the Parallel Load Input (PL) LOW, operation is synchronous and is edge-triggered on the LOW-to-HIGH transition of the Clock Input (CP). Operation is determined by the three synchronous Mode Control Inputs; UP/$\overline{DN}$, BIN/$\overline{DEC}$ and $\overline{CE}$ (see the Mode Selection Table). These inputs must be stable only during the set-up time prior to the LOW-to-HIGH transition of the Clock Input (CP) and the hold time after this clock transition. The Terminal Count Output ($\overline{TC}$) is LOW when the counter is at its terminal count, as determined by the counting mode, and the Count Enable Input ($\overline{CE}$) is LOW (see Logic Equation for $\overline{TC}$).

- **BINARY OR DECADE UP/DOWN COUNTER**
- **ASYNCHRONOUS PARALLEL LOAD**
- **ACTIVE LOW COUNT ENABLE**
- **CLOCK EDGE-TRIGGERED ON THE LOW-TO-HIGH TRANSITION**
- **ACTIVE LOW TERMINAL COUNT FOR CASCADING**
- **TYPICAL COUNT FREQUENCY OF 12 MHz AT V_{DD} = 10 V**

PIN NAMES

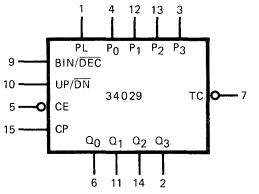
PL	Parallel Load Input
P_0-P_3	Parallel Data Inputs
BIN/$\overline{DEC}$	Binary/Decade Control Input
UP/$\overline{DN}$	Up/Down Control Input
$\overline{CE}$	Count Enable Input (Active LOW)
CP	Clock Input (L→H Edge-Triggered)
Q_0-Q_3	Buffered Parallel Outputs
$\overline{TC}$	Terminal Count Output (Active LOW)

MODE SELECTION TABLE

PL	BIN/$\overline{DEC}$	UP/$\overline{DN}$	$\overline{CE}$	CP	MODE
H	X	X	X	X	Parallel Load ($P_n \rightarrow Q_n$)
L	X	X	H	X	No Change
L	L	L	L	⎍	Count Down, Decade
L	L	H	L	⎍	Count Up, Decade
L	H	L	L	⎍	Count Down, Binary
L	H	H	L	⎍	Count Up, Binary

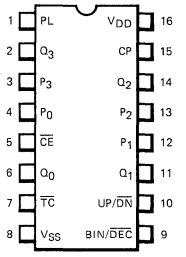
H = HIGH Level
L = LOW Level
X = Don't Care
⎍ = Positive-Going Transition

LOGIC SYMBOL



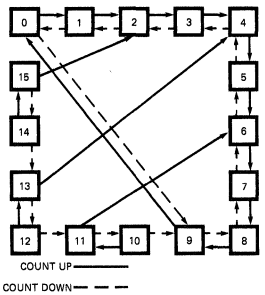
V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)

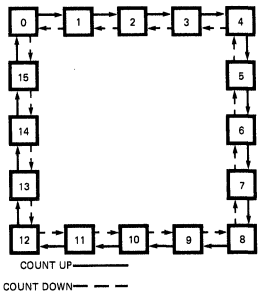


NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

34029 STATE DIAGRAM, BIN/$\overline{DEC}$ = LOW



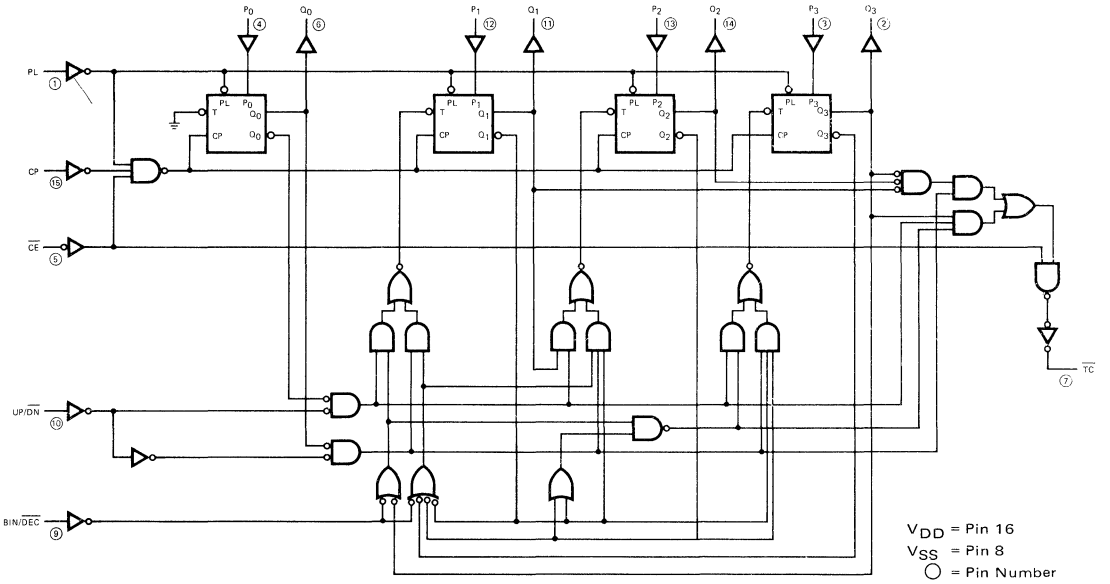
34029 STATE DIAGRAM, BIN/$\overline{DEC}$ = HIGH

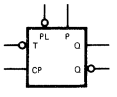


LOGIC EQUATION FOR TERMINAL COUNT

$$\overline{TC} = CE \bullet [((UP/\overline{DN}) \bullet Q_0 \bullet Q_3 \bullet ((Q_1 \bullet Q_2) + \overline{(BIN/\overline{DEC})})) + \overline{((UP/\overline{DN}) \bullet \overline{Q_0} \bullet \overline{Q_1} \bullet \overline{Q_2} \bullet \overline{Q_3}}$$

LOGIC DIAGRAM





$\overline{PL}$ (Parallel Load Input) — Asynchronously Loads P into Q, Overriding all Other Inputs
P (Parallel Input) — Data on this Pin is Asynchronously Loaded into Q, when PL is LOW Overriding all Other Inputs
$\overline{T}$ (Toggle Input) — Forces the Q Output to Synchronously Toggle when a LOW is Placed on this Input.
CP (Clock Pulse Input)
Q, $\overline{Q}$ (True and Complimentary Outputs)

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			50			100		20		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					700			1400		280			MAX	
		XM			5			10		2		μA	MIN, 25°C	
					300			600		120			MAX	

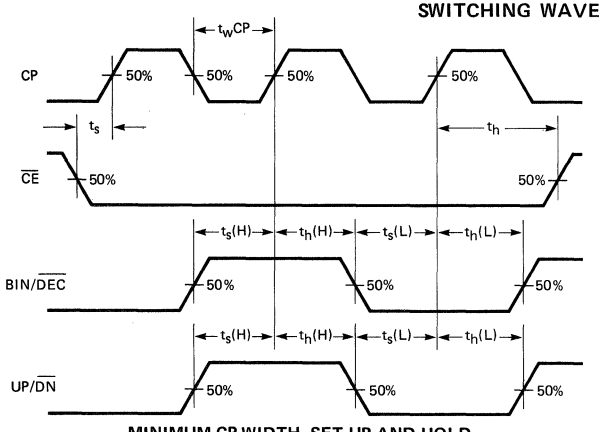
NOTE: Additional DC Characteristics are listed in this section under 34000 Series CMOS Family Characteristics.

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C

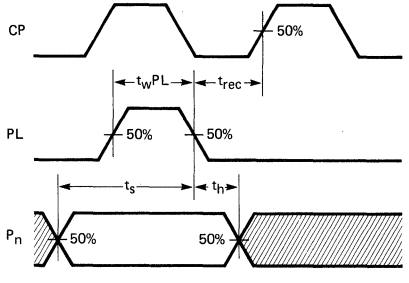
SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, CP to Q_n		135 135			54 50			35 33		ns ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
t_{PLH} t_{PHL}	Propagation Delay, CP to $\overline{TC}$		150 228			62 90			42 60		ns ns	
t_{PLH} t_{PHL}	Propagation Delay, PL to Q_n		152 194			59 80			38 56		ns ns	
t_{TLH} t_{THL}	Output Transition Time		25 25			13 13			10 10		ns ns	
t_{PLH} t_{PHL}	Propagation Delay, CP to Q_n		150 150			62 59			41 39		ns ns	C_L = 50 pF Input Transition Times ⩽ 20 ns
t_{PLH} t_{PHL}	Propagation Delay, CP to $\overline{TC}$		167 252			71 100			48 66		ns ns	
t_{PLH} t_{PHL}	Propagation Delay, PL to Q_n		170 220			70 90			45 62		ns ns	
t_{TLH} t_{THL}	Output Transition Time		60 65			31 25			23 18		ns ns	
t_wCP	CP Minimum Pulse Width		50			21			14		ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
t_wPL	PL Minimum Pulse Width		60			21			16		ns	
t_{rec}	PL Recovery Time		62			24			17		ns	
t_s t_h	Set-Up Time, BIN/$\overline{DEC}$ to CP Hold Time, BIN/$\overline{DEC}$ to CP		106 104			41 40			29 28		ns ns	
t_s t_h	Set-Up Time, UP/$\overline{DN}$ to CP Hold Time, UP/$\overline{DN}$ to CP		145 101			55 38			38 25		ns ns	
t_s t_h	Set-Up Time, $\overline{CE}$ to CP Hold Time, $\overline{CE}$ to CP		118 101			49 38			33 25		ns	
t_s t_h	Set-Up Time, P_n to PL Hold Time, P_n to PL		29 26			11 7			8 4		ns ns	
f_{MAX}	Input Clock Frequency		5			12			-		MHz	

NOTES:
1. Propagation Delays and Output Transition Times are graphically described in this section under 34000 Series CMOS Family Characteristics.
2. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Set-up Times (t_s), Hold Times (t_h), Recovery Times (t_{rec}), and Minimum Pulse Widths (t_w) do not vary with load capacitance.
3. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
4. It is recommended that input rise and fall times to the Clock Input be less than 15 μs.

SWITCHING WAVEFORMS



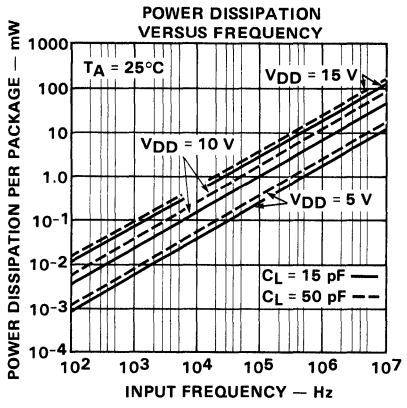
MINIMUM CP WIDTH, SET-UP AND HOLD TIMES, $\overline{CE}$ TO CP, BIN/$\overline{DEC}$ TO CP AND UP/$\overline{DN}$ TO CP

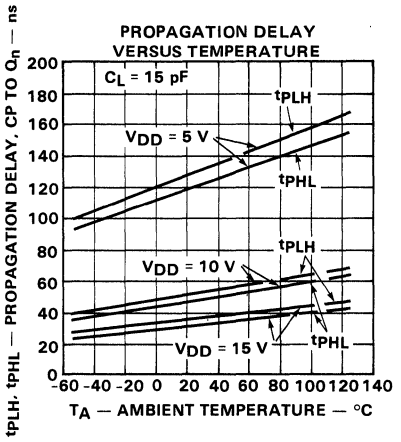


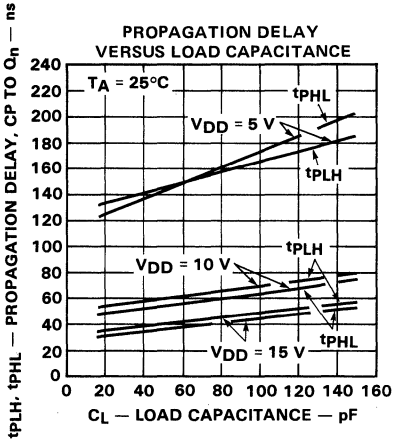
MINIMUM PL PULSE WIDTH, RECOVERY TIME FOR PL, AND SET-UP AND HOLD TIMES, P_n TO PL

NOTE: Set-up and Hold Times are shown as positive values but may be specified as negative values.

TYPICAL ELECTRICAL CHARACTERISTICS







APPLICATIONS

Interconnection techniques for multistage counting are shown in Figures 1 through 4. When using the schemes shown in Figures 1, 3 and 4, the BIN/$\overline{\text{DEC}}$ and UP/$\overline{\text{DN}}$ Inputs may be changed only when the Clock Input to the first stage is HIGH. However, when using the scheme shown in Figure 2, UP/$\overline{\text{DN}}$, BIN/$\overline{\text{DEC}}$ and $\overline{\text{CE}}$ may be changed independent of the state of the Clock Input. The methods illustrated in Figures 1 and 3 will operate with long transition times at the Clock Input to the first counter; whereas, the other schemes require a fast transition at the Clock Input.

Figure 1 is a ripple clock expansion scheme in which the maximum counting frequency is limited only by the frequency capability of the first counter. The disadvantage of this technique is that the Outputs of the most significant stage do not change until the clock has rippled through all the preceding stages.

A fully synchronous expansion method is shown in Figure 2. Since the Clock Input is applied simultaneously to all stages, the Outputs of all stages change simultaneously. The maximum counting frequency is limited by the time required for the Count Enable to ripple through all the stages before the next Clock Input is applied.

The semi-synchronous technique illustrated in Figure 3 allows a higher counting frequency than the method shown in Figure 2 by allowing $\overline{\text{TC}}$ to take either 10 or 16 clock periods to ripple from the second stage to the most significant stage (10 clock periods when BIN/$\overline{\text{DEC}}$ = L, 16 clock periods when BIN/$\overline{\text{DEC}}$ = H). The Outputs of all stages, except the first, change simultaneously. The Outputs of the first stage change before the other stages.

The speed advantage of this scheme is lost if the count direction or count modulus is rapidly changed.

The method shown in Figure 4 is the same as in Figure 3 except an external gate is added to reduce the delay between the Clock Input to the first stage and the Clock Input to the following stages.

APPLICATIONS (Cont'd)

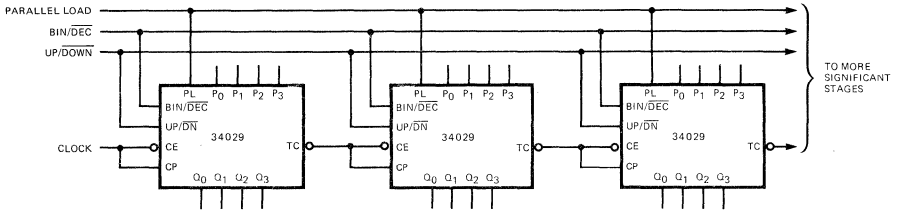


Fig. 1 RIPPLE CLOCK EXPANSION

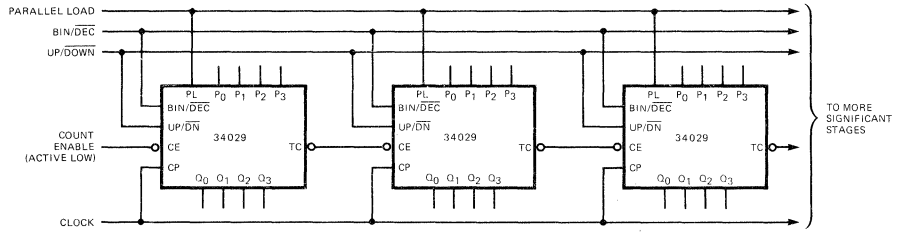


Fig. 2 PARALLEL CLOCK EXPANSION (FULLY SYNCHRONOUS)

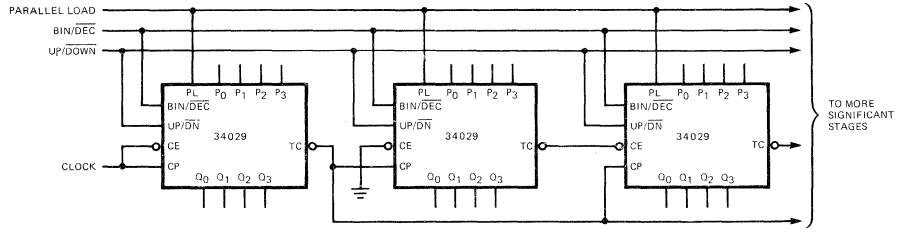


Fig. 3 SEMI-SYNCHRONOUS EXPANSION

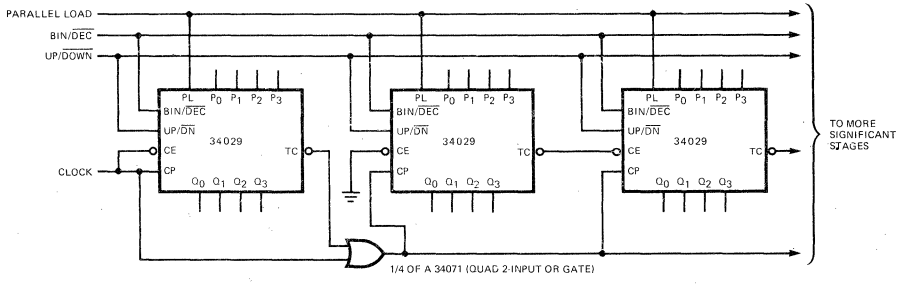
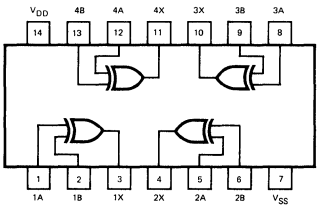


Fig. 4 HIGH SPEED SEMI-SYNCHRONOUS EXPANSION

QUAD EXCLUSIVE-OR GATE

DESCRIPTION — The 34030 CMOS logic element provides the Exclusive-OR function. The outputs are fully buffered for best performance.

34030 QUAD EXCLUSIVE-OR GATE



$X = \overline{A}B + A\overline{B}$

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V

SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEMP	TEST CONDITIONS
I_{DD}	Quiescent Power Supply Current	XC			5.0			10.0		2			
					70.0			140.0		28	μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
												MAX	
		XM			0.5			1.0		0.2		MIN, 25°C	
					30.0			60.0		12	μA	MAX	

NOTE: Additional DC Characteristics are listed in this section under 34000 Series CMOS Family Characteristics.

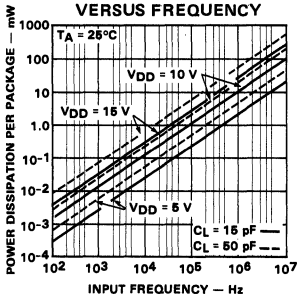
AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C

SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEST CONDITIONS
t_{PLH}	Propagation Delay,		65	130		33	65		23		ns	
t_{PHL}	A or B to X		65	130		33	65		23		ns	C_L = 15 pF
t_{TLH}	Output Transition		23	45		10	25		8	20	ns	Input Transition Times ⩽ 20 ns
t_{THL}	Time		23	45		10	25		8	20	ns	
t_{PLH}	Propagation Delay,		85	170		45	90		27		ns	
t_{PHL}	A or B to X		85	170		45	90		27		ns	C_L = 50 pF
t_{TLH}	Output Transition		50	100		23	50		17	35	ns	Input Transition Times ⩽ 20 ns
t_{THL}	Time		50	100		23	50		17	35	ns	

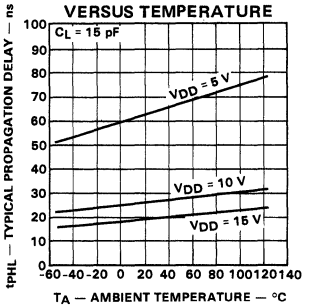
NOTE: Propagation delays and output transition times are graphically described in this section under 34000 Series CMOS Family Characteristics.

TYPICAL ELECTRICAL CHARACTERISTICS

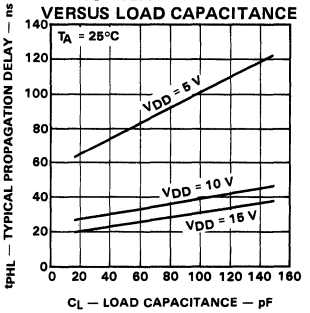
POWER DISSIPATION VERSUS FREQUENCY



PROPAGATION DELAY VERSUS TEMPERATURE



PROPAGATION DELAY VERSUS LOAD CAPACITANCE



34035
4-BIT UNIVERSAL SHIFT REGISTER

DESCRIPTION – The 34035 is a fully synchronous edge-triggered 4-Bit Shift Register with a Clock Input (CP), four synchronous Parallel Data Inputs (P_0–P_3), two synchronous Serial Data Inputs (J, $\overline{K}$), a synchronous Parallel Enable Input (PE), Buffered Parallel Outputs from all 4-bit positions (Q_0–Q_3), a True/Complement Input ($T/\overline{C}$) and an overriding asynchronous Master Reset Input (MR).

Operation is synchronous (except for Master Reset) and is edge-triggered on the LOW-to-HIGH transition of the Clock Input (CP). When the Parallel Enable Input (PE) is HIGH, data is loaded into the register from Parallel Inputs (P_0–P_3) on the LOW-to-HIGH transition of the Clock Input (CP). When the Parallel Enable Input (PE) is LOW, data is shifted into the first register position from the Serial Data Inputs (J, $\overline{K}$) and all the data in the register is shifted one position to the right on the LOW-to-HIGH transition of the Clock Input (CP). D-type entry is obtained by tying the two Serial Data Inputs (J, $\overline{K}$) together.

The Outputs (Q_0–Q_3) are either inverting or non-inverting, depending on the True/Complement Input ($T/\overline{C}$). With the $T/\overline{C}$ Input HIGH, the Outputs (Q_0–Q_3) are non-inverting (Active HIGH). With the $T/\overline{C}$ Input LOW, the Outputs (Q_0–Q_3) are inverting (Active LOW).

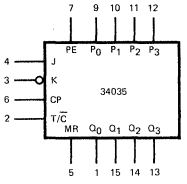
A HIGH on the Master Reset Input (MR) resets all four bit positions (Q_0–Q_3 = LOW if $T/\overline{C}$ = HIGH, Q_0–Q_3 = HIGH if $T/\overline{C}$ = LOW) independent of all other input conditions.

- **TYPICAL SHIFT FREQUENCY OF 12 MHz AT V_{DD} = 10 V**
- **J, $\overline{K}$ INPUTS TO THE FIRST STAGE**
- **$T/\overline{C}$ INPUT FOR TRUE OR COMPLEMENTARY OUTPUTS**
- **SYNCHRONOUS PARALLEL ENABLE**
- **CLOCK EDGE-TRIGGERED ON LOW-TO-HIGH TRANSITION**
- **ASYNCHRONOUS MASTER RESET**

PIN NAMES

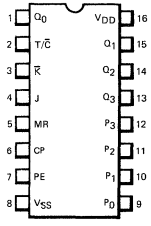
PE	Parallel Enable Input
P_0–P_3	Parallel Data Inputs
J	First Stage J Input (Active HIGH)
$\overline{K}$	First Stage K Input (Active LOW)
CP	Clock Input (L→H Edge-Triggered)
$T/\overline{C}$	True/Complement Input
MR	Master Reset Input
Q_0–Q_3	Buffered Parallel Outputs

LOGIC SYMBOL



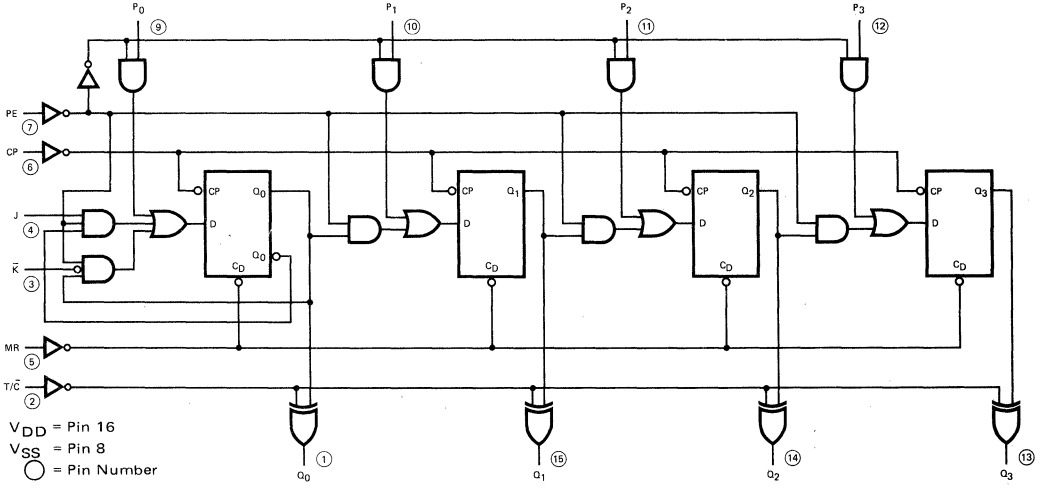
V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
◯ = Pin Number

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			50			100		20		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					500			1000		200			MAX	
		XM			5			10		2		μA	MIN, 25°C	
					40			80		16			MAX	

NOTE: Additional DC Characteristics are listed in this section under 34000 Series CMOS Family Characteristics.

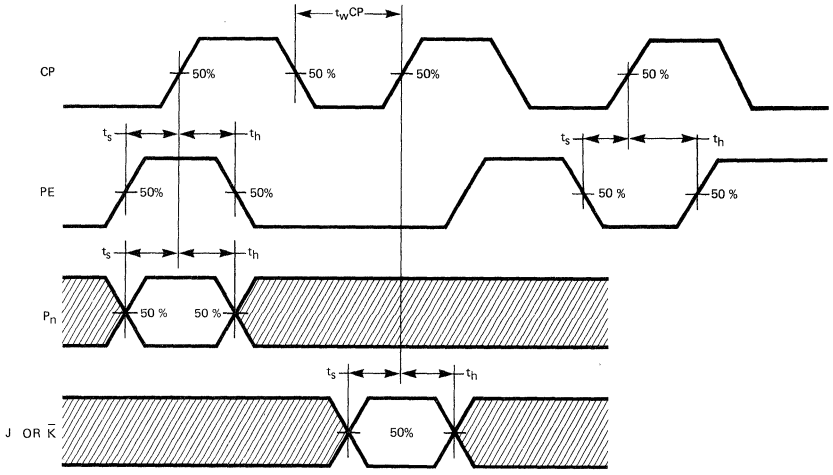
3

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C

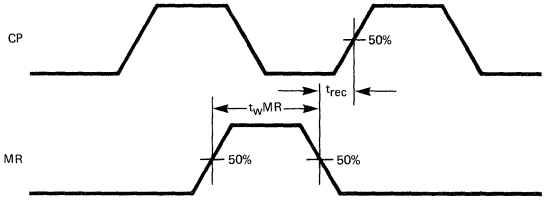
SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, CP to Q_n		180			80			50		ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
t_{PHL}			180			80			50		ns	
t_{PLH}	Propagation Delay, MR to Q_n		225			100			60		ns	
t_{PHL}			225			100			60		ns	
t_{PLH}	Propagation Delay, T/C to Q_n		100			45			35		ns	
t_{PHL}			100			45			35		ns	
t_{TLH}	Output Transition Time		50			25			20		ns	
t_{THL}			50			25			20		ns	
t_{PLH}	Propagation Delay, CP to Q_n		200			90			60		ns	C_L = 50 pF Input Transition Times ⩽ 20 ns
t_{PHL}			200			90			60		ns	
t_{PLH}	Propagation Delay, MR to Q_n		250			120			75		ns	
t_{PHL}			250			120			75		ns	
t_{PLH}	Propagation Delay, T/C to Q_n		125			55			40		ns	
t_{PHL}			125			55			40		ns	
t_{TLH}	Output Transition Time		85			45			30		ns	
t_{THL}			85			45			30		ns	
t_wCP	CP Minimum Pulse Width		75			30			20		ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
t_wMR	MR Minimum Pulse Width		60			25			20		ns	
t_{rec}	MR Recovery Time		160			60			45		ns	
t_s	Set-Up Time, P_n to CP		100			40			25		ns	
t_h	Hold Time, P_n to CP		−10			−5			−5		ns	
t_s	Set-Up Time, PE to CP		100			40			25		ns	
t_h	Hold Time, PE to CP		−10			−5			−5		ns	
t_s	Set-Up Time, J, K to CP		100			40			25		ns	
t_h	Hold Time, J, K to CP		−10			−5			−5		ns	
f_{MAX}	Max. Input Clock Frequency (Note 3)		5			12					MHz	

NOTES:
1. Propagation Delays and Output Transition Times are graphically described in this section under 34000 Series CMOS Family Characteristics.
2. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Set-up Times (t_s), Hold Times (t_h), Recovery Times (t_{rec}), and Minimum Pulse Widths (t_w) do not vary with load capacitance.
3. For f_{MAX} input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
4. It is recommended that input rise and fall times to the Clock Input be less than 15 μs.

SWITCHING WAVEFORMS



MINIMUM CP PULSE WIDTH AND SET-UP AND HOLD TIMES, PE TO CP, P_n TO CP, AND J OR $\overline{K}$ TO CP



MR RECOVERY TIME AND MINIMUM MR PULSE WIDTH

Note: Set-up and Hold Times are shown as positive values but may be specified as negative values.

34040
12-STAGE BINARY COUNTER

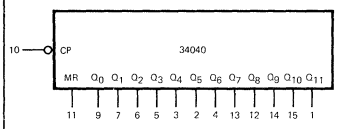
DESCRIPTION — The 34040 is a 12-Stage Binary Ripple Counter with a Clock Input ($\overline{CP}$), an overriding asynchronous Master Reset Input (MR) and twelve fully buffered Outputs (Q_0-Q_{11}). The counter advances on the HIGH-to-LOW transition of the Clock Input ($\overline{CP}$). A HIGH on the Master Reset Input (MR) clears all counter stages and forces all Outputs (Q_0-Q_{11}) LOW, independent of the Clock Input ($\overline{CP}$).

- **25 MHz TYPICAL COUNT FREQUENCY AT V_{DD} = 10 V**
- **CLOCK IS H→L TRIGGERED**
- **COMMON ASYNCHRONOUS MASTER RESET**
- **FULLY BUFFERED OUTPUTS FROM ALL 12 STAGES**

PIN NAMES

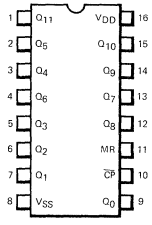
$\overline{CP}$	Clock Input (H→L Triggered)
MR	Master Reset Input (Active HIGH)
Q_0-Q_{11}	Parallel Outputs

LOGIC SYMBOL



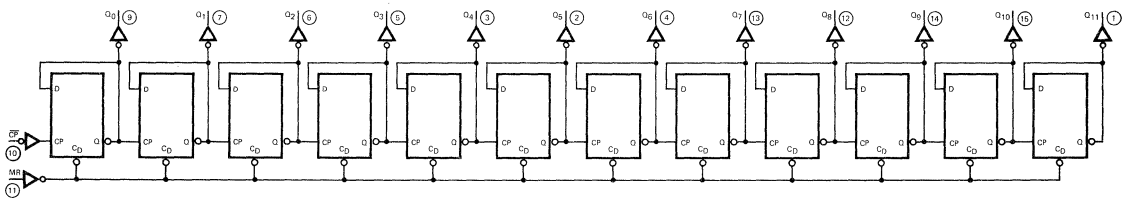
V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Numbers

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			50			100		20		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					700			1400		280			MAX	
		XM			15			25		5		μA	MIN, 25°C	
					900			1500		300			MAX	

NOTE: Additional DC Characteristics are listed in this section under 34000 Series CMOS Family Characteristics.

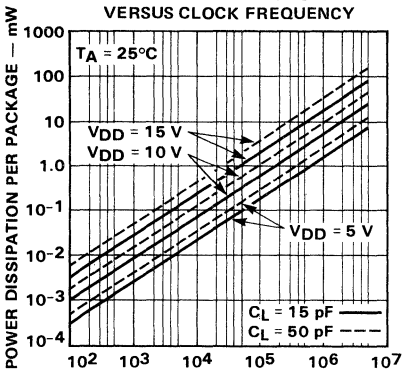
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, $\overline{CP}$ to Q_0		110	220		45	90		30		ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
t_{PHL}			85	170		37	75		25		ns	
t_{PHL}	Propagation Delay, MR to Q_n		150	300		65	130		43		ns	
t_{TLH}	Output Transition Time		30	75		13	40		10	25	ns	
t_{THL}			30	75		13	40		10	25	ns	
t_{PLH}	Propagation Delay, $\overline{CP}$ to Q_0		130	260		55	110		37		ns	C_L = 50 pF Input Transition Times ⩽ 20 ns
t_{PHL}			110	220		45	90		33		ns	
t_{PHL}	Propagation Delay, MR to Q_n		180	360		75	150		50		ns	
t_{TLH}	Output Transition Time		65	135		35	70		25	45	ns	
t_{THL}			65	135		35	70		25	45	ns	
$t_w\overline{CP}(H)$	Minimum Clock Pulse Width	100	50		40	20			16		ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
$t_w MR(H)$	Minimum MR Pulse Width	140	70		55	27			20		ns	
t_{rec}	Recovery Time for MR	85	43		35	17			12		ns	
f_{MAX}	Input Clock Frequency (Note 2)	5	10		12	25					MHz	

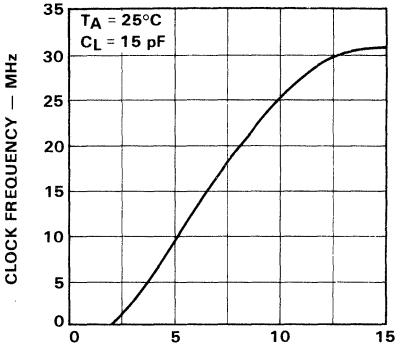
NOTES:
1. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Recovery Times (t_{rec}), and Minimum Pulse Widths (t_w) do not vary with load capacitance.
2. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
3. It is recommended that input rise and fall times to the Clock Input be less than 15 μs.

TYPICAL ELECTRICAL CHARACTERISTICS

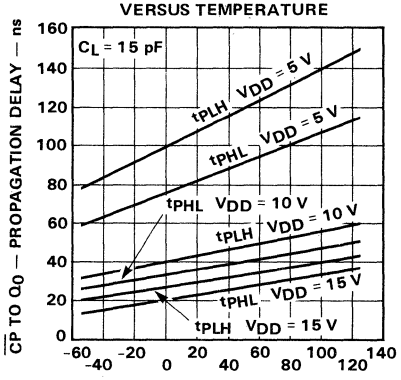
POWER DISSIPATION VERSUS CLOCK FREQUENCY



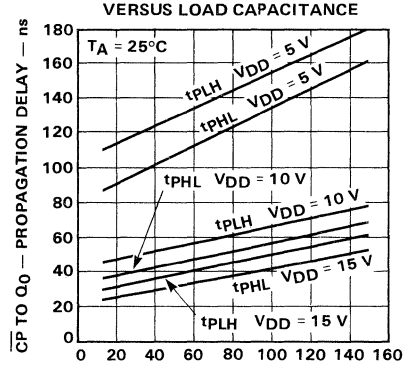
CLOCK FREQUENCY VERSUS POWER SUPPLY VOLTAGE



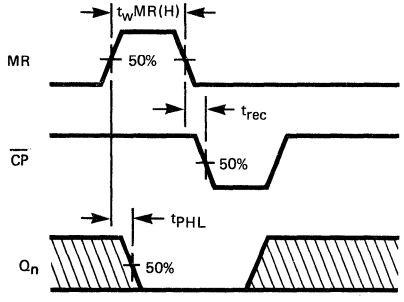
PROPAGATION DELAY VERSUS TEMPERATURE



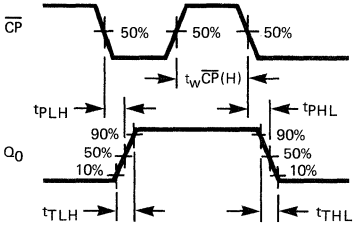
PROPAGATION DELAY VERSUS LOAD CAPACITANCE



SWITCHING WAVEFORMS



PROPAGATION DELAY MASTER RESET TO OUTPUT, MINIMUM MASTER RESET PULSE WIDTH AND RECOVERY TIME FOR MASTER RESET



PROPAGATION DELAY CLOCK TO OUTPUT Q_0, OUTPUT TRANSITION TIMES AND MINIMUM CLOCK PULSE WIDTH

34042
QUAD D LATCH

DESCRIPTION – The 34042 is a 4-Bit Latch with four Data Inputs (D_0-D_3), four buffered Latch Outputs (Q_0-Q_3), four buffered Complementary Latch Outputs ($\overline{Q}_0$-$\overline{Q}_3$) and two Common Enable Inputs (E_0 and E_1). Information on the Data Inputs (D_0-D_3) is transferred to the Outputs (Q_0-Q_3) while both Enable Inputs (E_0, E_1) are in the same state, either HIGH or LOW. The Outputs (Q_0-Q_3) follow the Data Inputs (D_0-D_3) as long as both Enable Inputs (E_0, E_1) remain in the same state. When the two Enable Inputs (E_0, E_1) are different, the Data Inputs (D_0-D_3) do not affect the Outputs (Q_0-Q_3) and the information in the latch is stored. The $\overline{Q}_0$-$\overline{Q}_3$ Outputs are always the complement of the Q_0-Q_3 Outputs. The Exclusive-OR input structure allows the choice of either polarity for the Enable Input. With one Enable Input HIGH, the other Enable Input is active HIGH; with one Enable Input LOW, the other Enable Input is active LOW.

The last moment prior to the trailing end of the enable condition that the Latch Outputs can still be affected by the inputs is specified as a set-up time. A negative set-up time, as typically exhibited by this device, means that the latches respond to input changes after the end of the enable condition. Following established industry practice, a hold time is specified, defining the time after the end of the enable condition, that the inputs must be held stable, so that they do not affect the state of the latches. It follows from this definition, that the hold time is identical with the negative set-up time. Set-up and hold times have a tolerance, due to manufacturing process variations, temperature and supply voltage changes. For predictable operation the data input levels must be held stable over the full spread of this timing window starting with the earliest set-up time (largest positive or smallest negative value) to the latest hold time.

- **ACTIVE HIGH OR ACTIVE LOW ENABLE**
- **TRUE AND COMPLEMENTARY OUTPUTS (Q & $\overline{Q}$)**

PIN NAMES

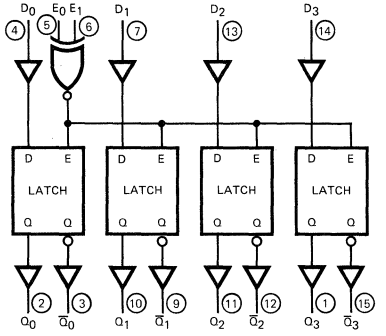
D_0-D_3	Data Inputs
E_0, E_1	Enable Inputs
Q_0-Q_3	Parallel Latch Outputs
$\overline{Q}_0$-$\overline{Q}_3$	Complementary Parallel Latch Outputs

TRUTH TABLE

E_0	E_1	LATCH CONDITION
L	L	Enabled
L	H	Not Enabled
H	L	Not Enabled
H	H	Enabled

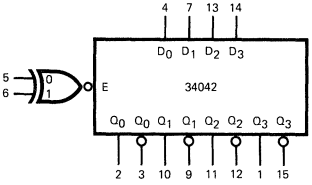
L = LOW Level
H = HIGH Level

LOGIC DIAGRAM



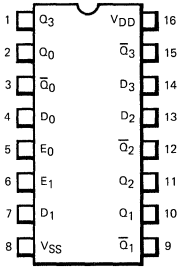
V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Numbers

LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			10			20		4		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					140			280		56			MAX	
		XM			1			2		0.4		μA	MIN, 25°C	
					60			120		24			MAX	

NOTE: Additional DC Characteristics are listed in this section under 34000 Series CMOS Family Characteristics.

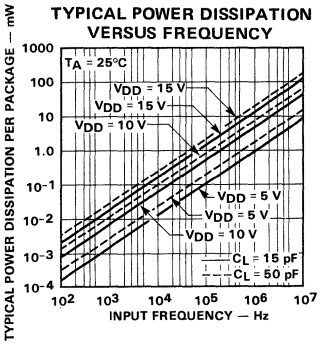
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay,		85	170		36	72		27		ns	
t_{PHL}	Data to Output		80	160		35	70		26		ns	C_L = 15 pF
t_{PLH}	Propagation Delay,		135	270		55	110		41		ns	Input Transition
t_{PHL}	Enable to Output		115	230		45	90		35		ns	Times ⩽ 20 ns
t_{TLH}	Output Transition		29	75		15	40		11	25	ns	
t_{THL}	Time		27	75		15	40		10	25	ns	
t_{PLH}	Propagation Delay,		101	200		45	90		33		ns	
t_{PHL}	Data to Output		99	200		44	88		33		ns	C_L = 50 pF
t_{PLH}	Propagation Delay,		156	310		66	132		47		ns	Input Transition
t_{PHL}	Enable to Output		137	275		58	116		41		ns	Times ⩽ 20 ns
t_{TLH}	Output Transition		65	135		31	70		25	45	ns	
t_{THL}	Time		60	135		26	70		20	45	ns	
t_s	Set-Up Time, D_n to E_0 or E_1	10	−12		10	−6			−4		ns	C_L = 15 pF
t_h	Hold Time, D_n to E_0 or E_1	50	25		25	13			7		ns	Input Transition
$t_w E_n$	Minimum Enable Pulse Width	80	40		32	16			12		ns	Times ⩽ 20 ns

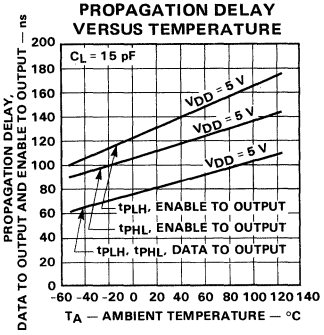
NOTE:
1. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Set-up Times (t_s), Hold Times (t_h), and Minimum Pulse Widths (t_w) do not vary with load capacitance.

TYPICAL ELECTRICAL CHARACTERISTICS

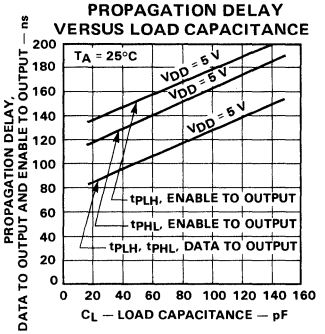
TYPICAL POWER DISSIPATION VERSUS FREQUENCY



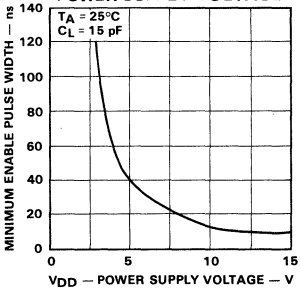
PROPAGATION DELAY VERSUS TEMPERATURE



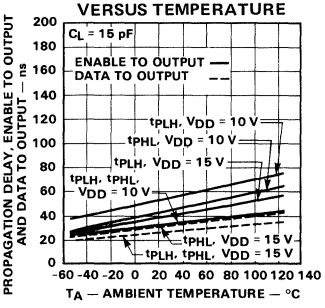
PROPAGATION DELAY VERSUS LOAD CAPACITANCE



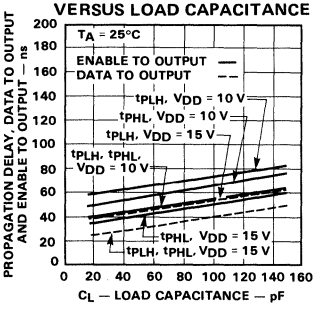
MINIMUM ENABLE PULSE WIDTH VERSUS POWER SUPPLY VOLTAGE



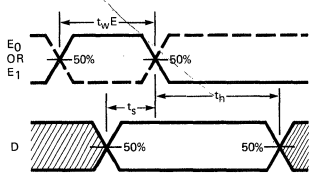
PROPAGATION DELAY VERSUS TEMPERATURE



PROPAGATION DELAY VERSUS LOAD CAPACITANCE

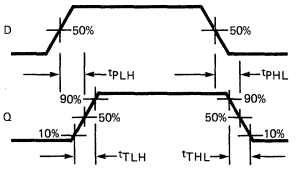


SWITCHING WAVEFORMS

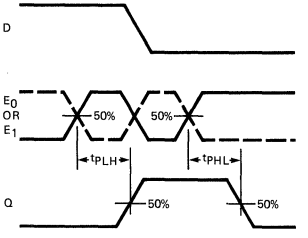


SET-UP AND HOLD TIMES, MINIMUM ENABLE PULSE WIDTH

NOTE:
Either E_0 or E_1 is held HIGH or LOW while the other Enable Input is pulsed as per the Truth Table. t_s and t_h are shown as positive values but may be specified as negative values.



PROPAGATION DELAY DATA TO OUTPUT AND TRANSITION TIMES, WITH LATCH ENABLED



PROPAGATION DELAY ENABLE TO OUTPUT

NOTE:
Either E_0 or E_1 is held HIGH or LOW while the other Enable Input is pulsed as per the Truth Table.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, 34049XC and 34050XC (Cont'd)

SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEMP	TEST CONDITIONS
I_{OH}	Output HIGH Current	-1.5									mA	MIN	V_{OUT} = 2.5 V for V_{DD} = 5 V
		-1.25	-2.5								mA	25°C	Inputs at 0 or V_{DD}
		-1.0									mA	MAX	per Function
													V_{OUT} = 4.5 V for V_{DD} = 5 V
		-0.6			-1.5				-5.2		mA	MIN	V_{OUT} = 9.5 V for V_{DD} = 10 V
		-0.5	-1.0		-1.25	-2.5			-4.7		mA	25°C	V_{OUT} = 14.5 V for V_{DD} = 15 V
		-0.4			-1.0				-4.0		mA	MAX	Inputs at 0 or V_{DD}
													per Function
I_{OL}	Output LOW Current	3.6			9.6				24.5		mA	MIN	V_{OUT} = 0.4 V for V_{DD} = 5 V
		3.0	6.0		8.0	16.0			22.0		mA	25°C	V_{OUT} = 0.5 V for V_{DD} = 10 V
		2.5			6.6				19.0		mA	MAX	V_{OUT} = 0.5 V for V_{DD} = 15 V
													Inputs at 0 or V_{DD}
													per Function
		3.1									mA	MIN	V_{OUT} = 0.4 V for V_{DD} = 4.5 V
		2.6	5.2								mA	25°C	Inputs at 0 V or V_{DD}
		2.1									mA	MAX	per Function
I_{DD}	Quiescent Power Supply Current			3.0			5.0		1.0		µA	MIN,25°C	All inputs common
				42.0			70.0		14.0			MAX	and at 0 V or V_{DD}

AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C, 34049 only

SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEST CONDITIONS
t_{PLH}	Propagation Delay		45	90		20	55		15		ns	
t_{PHL}			40	75		20	40		15		ns	C_L = 15 pF
t_{TLH}	Output Transition Time		30	60		17	35		12	25	ns	Input Transition Times ⩽ 20 ns
t_{THL}			20	40		7	20		5	10	ns	
t_{PLH}	Propagation Delay		65	130		30	65		29		ns	
t_{PHL}			50	105		25	50		17		ns	C_L = 50 pF
t_{TLH}	Output Transition Time		73	145		40	80		30	60	ns	Input Transition Times ⩽ 20 ns
t_{THL}			33	65		13	25		9	20	ns	

AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C, 34050 only

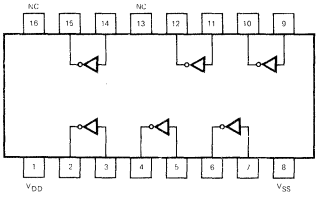
SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEST CONDITIONS
t_{PLH}	Propagation Delay		45	90		20	55		15		ns	
t_{PHL}			30	60		17	35		15		ns	C_L = 15 pF
t_{TLH}	Output Transition Time		30	60		17	35		12	25	ns	Input Transition Times ⩽ 20 ns
t_{THL}			20	40		7	20		5	10	ns	
t_{PLH}	Propagation Delay		65	130		30	65		24		ns	
t_{PHL}			43	95		23	45		17		ns	C_L = 50 pF
t_{TLH}	Output Transition Time		73	145		90	80		30	60	ns	Input Transition Times ⩽ 20 ns
t_{THL}			33	65		13	25		9	20	ns	

NOTE:
1. Propagation Delays and Output Transition Times are graphically described in this section under 34000 Series CMOS Family Characteristics.

34049 HEX INVERTING BUFFER • 34050 HEX NON-INVERTING BUFFER

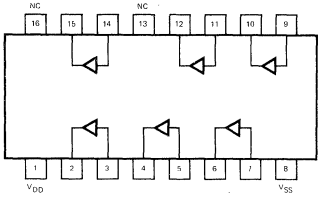
DESCRIPTION – These CMOS buffers provide high current output capability suitable for driving TTL or high capacitance loads. Since input voltages in excess of the buffers' supply voltage are permitted, these buffers may also be used to convert logic levels of up to 15 V to standard TTL levels. The 34049 provides six inverting buffers, the 34050 six non-inverting buffers. Their guaranteed fan out into common bipolar logic elements is shown in Table 1.

34049
LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)

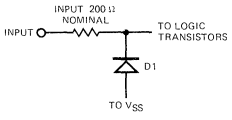


NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

34050
LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



INPUT PROTECTION



NOTE: Typical Breakdown Voltage of Diode D1 is 20 V.

TABLE 1
Guaranteed fan out of 34049, 34050 into common logic families

DRIVEN ELEMENT	GUARANTEED FAN OUT
Standard TTL, DTL	2
9LS, 93L, 74LS	9
74L	16

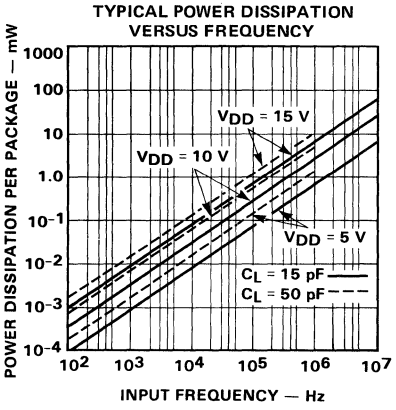
Conditions: $V_{DD} = V_{CC} = 5.0 \pm 0.25$ V
$V_{OL} \leq 0.5$ V, $T_A = 0$ to 75 °C

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, 34049XM and 34050XM

SYMBOL	PARAMETER	LIMITS									UNITS	TEMP	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{OH}	Output HIGH Current	-1.85									mA	MIN	V_{OUT} = 2.5 V for V_{DD} = 5 V
		-1.25	-2.5								mA	25°C	Inputs at 0 or V_{DD}
		-0.9									mA	MAX	per Function
		-0.62			-1.85				-5.2		mA	MIN	V_{OUT} = 4.5 V for V_{DD} = 5 V V_{OUT} = 9.5 V for V_{DD} = 10 V
		-0.5	-1.0		-1.25	-2.5			-4.7		mA	25°C	V_{OUT} = 14.5 V for V_{DD} = 15 V
		-0.35			-0.9				-3.5		mA	MAX	Inputs at 0 or V_{DD} per Function
I_{OL}	Output LOW Current	3.75			10.0				24.5		mA	MIN	V_{OUT} = 0.4 V for V_{DD} = 5 V V_{OUT} = 0.5 V for V_{DD} = 10 V
		3.0	6.0		8.0	16.0			22.0		mA	25°C	V_{OUT} = 0.5 V for V_{DD} = 15 V
		2.1			5.6				16.8		mA	MAX	Inputs at 0 or V_{DD} per Function
		3.3									mA	MIN	V_{OUT} = 0.4 V for V_{DD} = 4.5 V
		2.6	5.2								mA	25°C	Inputs at 0 V or V_{DD}
		1.8									mA	MAX	per Function
I_{DD}	Quiescent Power Supply Current			0.3			0.5		0.1		μA	MIN,25°C	All inputs common and at 0 V or V_{DD}
				20.0			30.0		6.0			MAX	

NOTE: Additional DC Characteristics are listed in this section under 34000 Series CMOS Family Characteristics.

TYPICAL ELECTRICAL CHARACTERISTICS



34051
8-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

DESCRIPTION – The 34051 is an 8-Channel Analog Multiplexer/Demultiplexer with three Address Inputs (A_0-A_2), an active LOW Enable Input ($\overline{E}$), eight Independent Inputs/Outputs (Y_0-Y_7) and a Common Input/Output (Z).

The 34051 contains eight bidirectional analog switches, each with one side connected to an Independent Input/Output (Y_0-Y_7) and the other side connected to a Common Input/Output (Z). With the Enable Input ($\overline{E}$) LOW, one of the eight switches is selected (low impedance, ON state) by the three Address Inputs (A_0-A_2). With the Enable Input ($\overline{E}$) HIGH, all switches are in the high impedance OFF state, independent of the Address Inputs.

V_{DD} and V_{SS} are the two supply voltage connections for the digital control inputs (A_0-A_2, $\overline{E}$). Their voltage limits are the same as for all other digital CMOS. The analog inputs/outputs (Y_0-Y_7, Z) can swing between V_{DD} as a positive limit and V_{EE} as a negative limit. V_{DD}-V_{EE} may not exceed 15 V. For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to V_{SS} (typically ground).

- **ANALOG OR DIGITAL MULTIPLEXER/DEMULTIPLEXER**
- **COMMON ENABLE INPUT (ACTIVE LOW)**

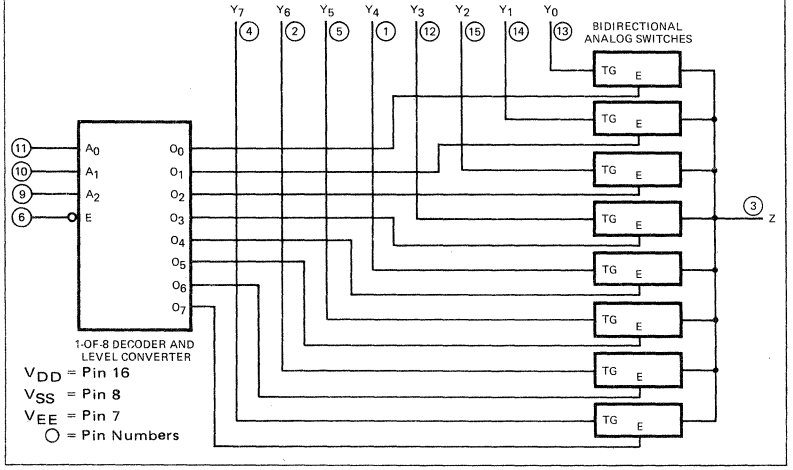
PIN NAMES	FUNCTION
Y_0-Y_7	Independent Inputs/Outputs
A_0-A_2	Address Inputs
$\overline{E}$	Enable Input (Active LOW)
Z	Common Input/Output

TRUTH TABLE

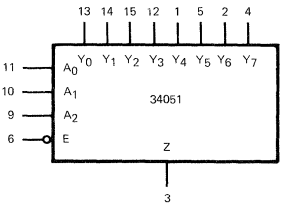
INPUTS				CHANNELS							
E	A_2	A_1	A_0	Y_0–Z	Y_1–Z	Y_2–Z	Y_3–Z	Y_4–Z	Y_5–Z	Y_6–Z	Y_7–Z
L	L	L	L	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF
L	L	L	H	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF
L	L	H	L	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF
L	L	H	H	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF
L	H	L	L	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF
L	H	L	H	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF
L	H	H	L	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF
L	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON
H	X	X	X	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

L = LOW Level
H = HIGH Level
X = Don't Care

34051 FUNCTIONAL LOGIC DIAGRAM

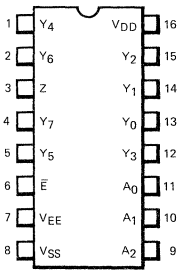


LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8
V_{EE} = Pin 7

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{EE} = 0 V

SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEMP	TEST CONDITIONS
R_{ON}	ON Resistance	XC		95			55			35		Ω	MIN 25°C MAX	V_{is} = V_{DD} Note 2
				100			65			40				
				125			100			65				
				95			55			35		Ω	MIN 25°C MAX	V_{is} = V_{EE} Note 2
				100			65			40				
				125			100			65				
				1600			110			55		Ω	MIN 25°C MAX	Note 3
				1000			125			60				
				850			200			95				
		XM		90			50			30		Ω	MIN 25°C MAX	V_{is} = V_{DD} Note 2
				100			65			40				
				150			110			70				
				90			50			30		Ω	MIN 25°C MAX	V_{is} = V_{EE} Note 2
				100			65			40				
				150			110			70				
				1750			100			50		Ω	MIN 25°C MAX	Note 3
				1000			125			60				
				700			220			100				
ΔR_{ON}	"Δ" ON Resistance Between Any Two Channels						10			5		Ω	25°C	Note 2
I_Z	OFF State Leakage Current, All Channels OFF	XC						800				Ω	25°C	$\overline{E}$ = V_{DD}, V_{SS} = $V_{DD}/2$ V_{is} = V_{DD} or V_{EE}
		XM						80				nA		
	Any Channel OFF	XC						100						$\overline{E}$ = V_{SS} = $V_{DD}/2$ V_{is} = V_{DD} or V_{EE}
		XM						10						
I_{DD}	Quiescent Power Supply Dissipation	XC			20			40		8		μA	MIN,25°C	V_{SS} = V_{EE} All inputs common and and at V_{DD} or V_{EE}
					700			1400		280			MAX	
		XM			2			4		0.8		μA	MIN,25°C	
					70			140		28			MAX	

NOTES:
1. Additional DC Characteristics for the Address and Enable Inputs are listed in this section under 34000 Series CMOS Family Characteristics.
2. $\overline{E}$ = V_{SS}, R_L = 10 kΩ, any channel selected and V_{SS} = V_{EE} or $V_{DD/2}$.
3. V_{is} = 8.6 V for V_{DD} = 15 V
   V_{is} = 5.1 V for V_{DD} = 10 V
   V_{is} = 1.9 V for V_{DD} = 5 V
4. V_{is} is the voltage signal at an Input/Output Terminal (Y_n/Z_n).

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{EE} = 0 V, T_A = 25°C

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay,		20			7			4		ns	C_L = 15 pF, $\overline{E}$ = V_{SS} = V_{EE},
t_{PHL}	Input to Output		8			4			3		ns	A_n or V_{is} = V_{DD} or V_{EE}
t_{PLH}	Propagation Delay,		160			90			75		ns	Note 3
t_{PHL}	Address to Output		200			120			90		ns	
t_{PZL}	Output Enable Time		180			90			70		ns	C_L = 15 pF
t_{PZH}			200			100			80		ns	$\overline{E}$ or A_n = V_{SS} = V_{EE}
t_{PLZ}	Output Disable Time		1000			900			860		ns	V_{is} = V_{DD} or V_{EE}
t_{PHZ}			1000			900			850			Note 3
t_{PLH}	Propagation Delay,		25			10			6		ns	C_L = 50 pF
t_{PHL}	Input to Output		10			6			4		ns	$\overline{E}$ = V_{SS} = V_{EE},
t_{PLH}	Propagation Delay,		170			95			80		ns	A_n or V_{is} = V_{DD} or V_{EE}
t_{PHL}	Address to Output		210			125			95		ns	Note 3
t_{PZL}	Output Enable Time		185			95			75		ns	C_L = 50 pF
t_{PZH}			205			105			85		ns	$\overline{E}$ or A_n = V_{SS} = V_{EE}
t_{PLZ}	Output Disable Time		1250			1130			1080		ns	V_{is} = V_{DD} or V_{EE}
t_{PHZ}			1240			1120			1070		ns	Note 3
	Distortion, Sine Wave Response		0.2			0.2			0.2		%	C_L = 15 pF R_L = 10 kΩ , V_{SS} = $V_{DD}/2$ $\overline{E}$ = V_{EE}, V_{is} = $V_{DD}/2$ (sine wave) f_{is} = 1 kHz
	Crosstalk Between Any Two Channels					1					MHz	R_L = 1 kΩ , $\overline{E}$ = V_{EE} V_{is} = $V_{DD}/2$ (sine wave) at -40 dB V_{SS} = $V_{DD}/2$, 20 Log_{10} (V_{os}/V_{is}) = -40 dB
	OFF State Feedthrough					1					MHz	R_L = 1 kΩ , V_{SS} = $V_{DD}/2$ $\overline{E}$ = V_{DD} V_{is} = $V_{DD}/2$ (p-p), 20 Log_{10} (V_{os}/V_{is}) = -40 dB
f_{MAX}	ON State Frequency Response		13			40			70		MHz	R_L = 1 kΩ V_{is} = $V_{DD}/2$ (sine wave) V_{SS} = $V_{DD}/2$ 20 Log_{10} (V_{os}/V_{is}) = -3 dB

NOTES:
1. Propagation Delays and Output Transition Times are graphically described in this section under 34000 Series CMOS Family Characteristics.
2. V_{is}/V_{os} is the voltage signal at an Input/Output terminal (Y_n/Z_n).
3. V_{IN} = V_{DD} (Square Wave), Input transition times ≤ 20 ns, R_L = 10 kΩ.

34052
DUAL 4-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

DESCRIPTION – The 34052 is a Dual 4-Channel Analog Multiplexer/Demultiplexer with common channel select logic. Each Multiplexer/Demultiplexer has four Independent Inputs/Outputs (Y_0–Y_3) and a Common Input/Output (Z). The common channel select logic includes two Address Inputs (A_0, A_1) and an active LOW Enable Input ($\overline{E}$).

Both multiplexer/demultiplexers contain four bidirectional analog switches, each with one side connected to an Independent Input/Output (Y_0–Y_3) and the other side connected to a Common Input/Output (Z). With the Enable Input LOW, one of the four switches is selected (low impedance, ON state) by the two Address Inputs. With the Enable Input HIGH, all switches are in the high impedance OFF state, independent of the Address Inputs.

V_{DD} and V_{SS} are the two supply voltage connections for the digital control inputs (A_0, A_1, $\overline{E}$). Their voltage limits are the same as for all other digital CMOS. The analog inputs/outputs (Y_0–Y_3, Z) can swing between V_{DD} as a positive limit and V_{EE} as a negative limit. V_{DD}–V_{EE} may not exceed 15 V. For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to V_{SS} (typically ground).

- **DIGITAL OR ANALOG MULTIPLEXER/DEMULTIPLEXER**
- **COMMON ENABLE INPUT (ACTIVE LOW)**

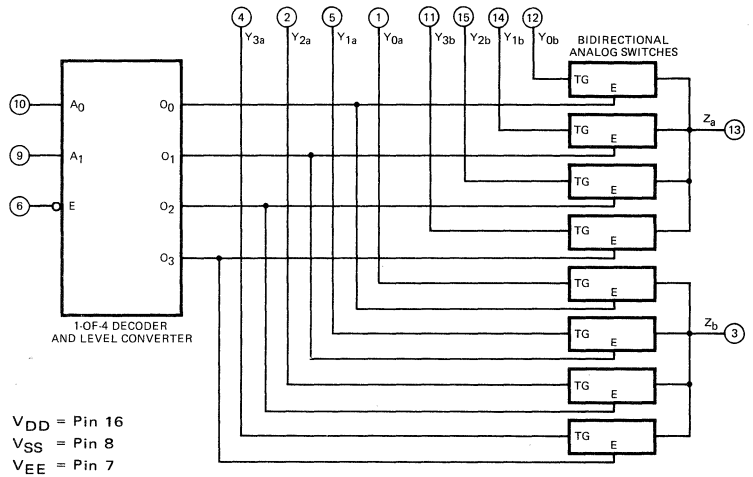
PIN NAMES	FUNCTION
Y_{0a}–Y_{3a}	Independent Inputs/Outputs
Y_{0b}–Y_{3b}	Independent Inputs/Outputs
A_0, A_1	Address Inputs
$\overline{E}$	Enable Input (Active LOW)
Z_a, Z_b	Common Input/Output

TRUTH TABLE

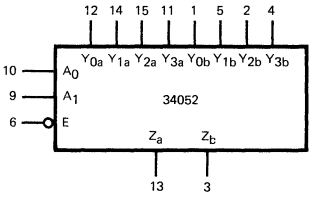
INPUTS			CHANNELS			
$\overline{E}$	A_1	A_0	Y_0–Z	Y_1–Z	Y_2–Z	Y_3–Z
L	L	L	ON	OFF	OFF	OFF
L	L	H	OFF	ON	OFF	OFF
L	H	L	OFF	OFF	ON	OFF
L	H	H	OFF	OFF	OFF	ON
H	X	X	OFF	OFF	OFF	OFF

L = LOW Level, H = HIGH Level, X = Don't care.

34052 FUNCTIONAL LOGIC DIAGRAM

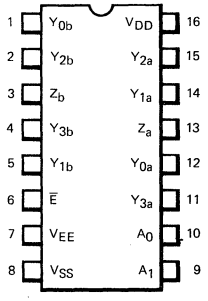


LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8
V_{EE} = Pin 7

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{EE} = 0 V

SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEMP	TEST CONDITIONS
R_{ON}	ON Resistance	XC		95			55			35		Ω	MIN	$V_{is} = V_{DD}$
				100			65			40			25°C	Note 2
				125			100			65			MAX	
				95			55			35		Ω	MIN	$V_{is} = V_{EE}$
				100			65			40			25°C	Note 2
				125			100			65			MAX	
				1600			110			55		Ω	MIN	
				1000			125			60			25°C	Note 3
				850			200			95			MAX	
		XM		90			50			30		Ω	MIN	$V_{is} = V_{DD}$
				100			65			40			25°C	Note 2
				150			110			70			MAX	
				90			50			30		Ω	MIN	$V_{is} = V_{EE}$
				100			65			40			25°C	Note 2
				150			110			70			MAX	
				1750			100			50		Ω	MIN	
				1000			125			60			25°C	Note 3
				700			220			100			MAX	
ΔR_{ON}	" " ON Resistance Between Any Two Channels						10			5		Ω	25°C	Note 2
I_Z	OFF State Leakage Current, All Channels OFF	XC						800				nA	25°C	$\bar{E} = V_{DD}$, $V_{SS} = V_{DD}/2$ $V_{is} = V_{DD}$ or V_{EE}
		XM						80						
	Any Channel OFF	XC						100						$\bar{E} = V_{SS} = V_{DD}/2$ $V_{is} = V_{DD}$ or V_{EE}
		XM						10						
I_{DD}	Quiescent Power Supply Dissipation	XC			20			40		8		μA	MIN,25°C	$V_{SS} = V_{EE}$ All Inputs Common and at 0 V or V_{DD}
					700			1400		280			MAX	
		XM			2			4		0.8		μA	MIN,25°C	
					70			140		28			MAX	

NOTES:
1. Additional DC Characteristics for the Address and Enable Inputs are listed in this section under 34000 Series CMOS Family Characteristics.
2. $\bar{E} = V_{SS}$, R_L = 10 kΩ, any channel selected and $V_{SS} = V_{EE}$ or $V_{DD}/2$.
3. V_{is} = 8.6V for V_{DD} = 15V
   V_{is} = 5.1V for V_{DD} = 10V
   V_{is} = 1.9V for V_{DD} = 5V
4. V_{is} is the voltage signal at an Input/Output Terminal (Y_n/Z_n).

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{EE} = 0 V, T_A = 25°C

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, Input to Output		20 8			7 4			4 3		ns ns	C_L = 15 pF, $\overline{E}$ = V_{SS} = V_{EE}, A_n or V_{is} = V_{DD} or V_{EE} Note 3
t_{PLH} t_{PHL}	Propagation Delay, Address to Output		160 200			90 120			75 90		ns ns	
t_{PZL} t_{PZH}	Output Enable Time		180 200			90 100			70 80		ns ns	C_L = 15 pF $\overline{E}$ or A_n = V_{SS} = V_{EE}
t_{PLZ} t_{PHZ}	Output Disable Time		1000 1000			900 900			860 850		ns	V_{is} = V_{DD} or V_{EE} Note 3
t_{PLH} t_{PHL}	Propagation Delay, Input to Output		25 10			10 6			6 4		ns ns	C_L = 50 pF $\overline{E}$ = V_{SS} = V_{EE},
t_{PLH} t_{PHL}	Propagation Delay, Address to Output		170 210			95 125			80 95		ns ns	A_n or V_{is} = V_{DD} or V_{EE} Note 3
t_{PZL} t_{PZH}	Output Enable Time		185 205			95 105			75 85		ns ns	C_L = 50 pF $\overline{E}$ or A_n = V_{SS} = V_{EE}
t_{PLZ} t_{PHZ}	Output Disable Time		1250 1240			1130 1120			1080 1070		ns ns	V_{is} = V_{DD} or V_{EE} Note 3
	Distortion, Sine Wave Response		0.2			0.2			0.2		%	C_L = 15 pF R_L = 10 kΩ , V_{SS} = $V_{DD}/2$ $\overline{E}$ = V_{EE}, V_{is} = $V_{DD}/2$ (sine wave) f_{is} = 1 kHz
	Crosstalk Between Any Two Channels					1					MHz	R_L = 1 kΩ , $\overline{E}$ = V_{EE} V_{is} = $V_{DD}/2$ (sine wave) at −40 dB V_{SS} = $V_{DD}/2$, 20 Log_{10} (V_{os}/V_{is}) = −40 dB
	OFF State Feedthrough					1					MHz	R_L = 1 kΩ , V_{SS} = $V_{DD}/2$ $\overline{E}$ = V_{DD} V_{is} = $V_{DD}/2$ (sine wave) 20 Log_{10} (V_{os}/V_{is}) = −40 dB
f_{MAX}	ON State Frequency Response		13			40			70		MHz	R_L = 1 kΩ , $\overline{E}$ = V_{SS} V_{is} = $V_{DD}/2$ (sine wave) V_{SS} = $V_{DD}/2$ 20 Log_{10} (V_{os}/V_{is}) = −3 dB

NOTES:
1. Propagation Delays and Output Transition Times are graphically described in this section under 34000 Series CMOS Family Characteristics.
2. V_{is}/V_{os} is the voltage signal at an Input/Output Terminal (Y_n/Z_n).
3. V_{IN} = V_{DD} (Square Wave), Input Transition Times ⩽20 ns and R_L = 10 kΩ.

34066
QUAD BILATERAL SWITCHES

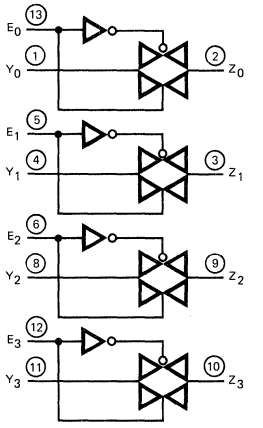
DESCRIPTION – The 34066 has four independent bilateral analog switches (transmission gates). Each switch has two Input/Output Terminals (Y_n, Z_n) and an active HIGH Enable Input (E_n). A HIGH on the Enable Input establishes a low impedance bidirectional path between Y_n and Z_n (ON condition). A LOW on the Enable Input disables the switch; high impedance between Y_n and Z_n (OFF condition).

- **DIGITAL OR ANALOG SIGNAL SWITCHING**
- **INDIVIDUAL ENABLE INPUTS (ACTIVE HIGH)**

PIN NAMES

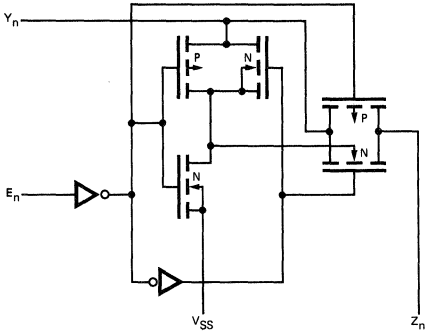
E_0 - E_3	Enable Inputs
Y_0 - Y_3	Input/Output Terminals
Z_0 - Z_3	Input/Output Terminals

LOGIC SYMBOL

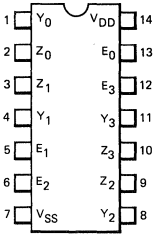


V_{DD} = Pin 14
V_{SS} = Pin 7
◯ = Pin Numbers

LOGIC DIAGRAM (1/4 OF A 34066)



CONNECTION DIAGRAM
DIP (TOP VIEW)



Note: The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
R_{ON}	ON Resistance	XC		190	900		100	450		80	250		MIN	R_L = 10 kΩ
				270	1000		120	500		80	280	Ω	25°C	E_n = V_{DD},
				330	1090		170	520		130	300		MAX	V_{is} = V_{DD} to V_{SS}
		XM		160	850		85	400		60	220		MIN	R_L = 10 kΩ
				270	1000		120	500		80	280	Ω	25°C	E_n = V_{DD},
				360	1150		190	550		145	320		MAX	V_{is} = V_{DD} to V_{SS}
ΔR_{ON}	"Δ" ON Resistance Between Any Two Switches						10			5		Ω	25°C	V_{is} = V_{DD} to V_{SS}, E_n = V_{DD} R_L = 10 kΩ
I_Z	OFF State Leakage Current, Any Y to Z							100			100	nA	MIN, 25°C	V_{is} = V_{DD} or V_{SS},
								200			200		MAX	E_n = V_{SS}
I_{DD}	Quiescent Power Supply Current	XC			0.25			0.5		0.1		μA	MIN, 25°C	All inputs common and at V_{DD} or V_{SS}
					25			30		6			MAX	
		XM			0.25			0.5		0.1		μA	MIN, 25°C	
					25			30		6			MAX	

NOTES: 1. Additional DC Characteristics for the Enable Inputs are listed in this section under 34000 Series CMOS Family Characteristics.
2. V_{is} is the input voltage to Input/Output Terminal (Y_n/Z_n).

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C

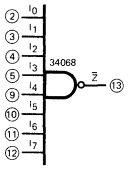
SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, Y_n to Z_n or Z_n to Y_n		4 3			1.5 1.5			1 1		ns	C_L = 15 pF, R_L = 10 kΩ Input Transition Times ⩽ 20 ns $E_n = V_{DD}$ $V_{is} = V_{DD}$ (square wave)
t_{PZL} t_{PZH}	Output Enable Time		24 24			14 14			10 10		ns ns	C_L = 15 pF, R_L = 300 Ω $E_n = V_{DD}$ (square wave)
t_{PLZ} t_{PHZ}	Output Disable Time		160 160			170 170			182 182		ns ns	Input Transition Times ⩽ 20 ns $V_{is} = V_{DD}$
t_{PLH} t_{PHL}	Propagation Delay, Y_n to Z_n or Z_n to Y_n		8 8			3 4			2 2.5		ns ns	C_L = 50 pF, R_L = 10 kΩ Input Transition Times ⩽ 20 ns $E_n = V_{DD}$ $V_{is} = V_{DD}$ (square wave)
t_{PZL} t_{PZH}	Output Enable Time		32 32			16 16			13 13		ns ns	C_L = 50 pF, R_L = 300 Ω $E_n = V_{DD}$ (square wave)
t_{PLZ} t_{PHZ}	Output Disable Time		380 380			380 380			400 400		ns ns	Input Transition Times ⩽ 20 ns $V_{is} = V_{DD}$
	Distortion, Sine Wave Response		0.31			0.31			0.31		%	C_L = 15 pF, R_L = 10 kΩ Input Frequency = 1 kHz $E_n = V_{DD}$ $V_{is} = V_{DD}/2$ (sine wave)
	Crosstalk Between Any Two Switches					0.9					MHz	R_L = 1 kΩ $E_A = V_{DD}$, $E_B = V_{SS}$ $V_{is} = V_{DD}/2$ (sine wave) at -50 dB, 20 Log_{10} $[V_{os}$ (B)/V_{is} (A)] = -50 dB
	Crosstalk, Enable Input to Output					50					mV	Input Transition Times ⩽ 20 ns $R_{L(OUT)}$ = 10 kΩ , $R_{L(IN)}$ = 1 kΩ $E_n = V_{DD}$ (square wave)
	OFF State Feedthrough					1.25					MHz	R_L = 1 kΩ $E_n = V_{SS}$, $V_{is} = V_{DD}/2$(sine wave) 20 Log_{10} (V_{os}/V_{is}) = -50 dB
	ON State Frequency Response					90					MHz	R_L = 1 kΩ $V_{is} = V_{DD}/2$ (sine wave) $E_n = V_{DD}$, 20 Log_{10} (V_{os}/V_{is}) = -3 dB
f_{MAX}	Enable Input Frequency (Note 2)					10					MHz	C_L = 15 pF, R_L = 1 kΩ Input Transition Times ⩽ 20 ns $E_n = V_{DD}$ (square wave) $V_{is} = V_{DD}$

NOTES:
1. Propagation Delays and Output Transition Times are graphically described in this section under 34000 Series CMOS Family Characteristics.
2. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
3. V_{is}/V_{os} is the voltage signal at an Input/Output Terminal (Y_n/Z_n).

8-INPUT NAND GATE

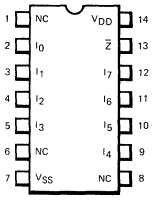
DESCRIPTION — This CMOS logic element provides the positive 8-Input NAND function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

34068 LOGIC SYMBOL



V_{DD} = Pin 14
V_{SS} = Pin 7
NC = Pins 1, 6, 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



PIN NAMES

I_0-I_7	NAND Gate Inputs
$\overline{Z}$	Output (Active LOW)

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V

SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEMP	TEST CONDITIONS
I_{DD}	Quiescent Power Supply Current	XC			0.5			5.0		1.0		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					15.0			30.0		6.0			MAX	
		XM			0.05			0.1		0.02		μA	MIN, 25°C	
					3.0			6.0		1.2			MAX	

NOTE: Additional DC Characteristics are listed in this section under 34000 Series CMOS Family Characteristics.

AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C

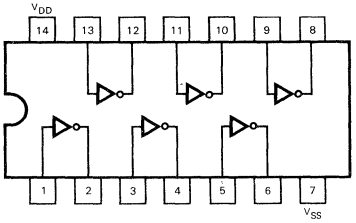
SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEST CONDITIONS
t_{PLH}	Propagation Delay		65			30			22		ns	
t_{PHL}			70			32			22		ns	C_L = 15 pF
t_{TLH}	Output Transition		25			13			10		ns	Input Transition Times ⩽ 20 ns
t_{THL}	Time		25			10			8		ns	
t_{PLH}	Propagation Delay		82			40			29		ns	
t_{PHL}			88			40			28		ns	C_L = 50 pF
t_{TLH}	Output Transition		64			32			24		ns	Input Transition Times ⩽ 20 ns
t_{THL}	Time		55			23			16		ns	

NOTE:
Propagation delays and output transition times are graphically described in this section under 34000 Series CMOS Family Characteristics.

HEX INVERTER

DESCRIPTION — The 34069 is a general purpose Hex Inverter which has standard Fairchild input and output characteristics. A single-stage design has been used since the output impedance of a single-input gate is not pattern sensitive.

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			3.0			5.0		1.0		µA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					42.0			70.0		14.0			MAX	
		XM			0.3			0.5		0.1		µA	MIN, 25°C	
					20.0			30.0		6.0			MAX	

NOTE: Additional DC Characteristics are listed in this section under 34000 Series CMOS Family Characteristics.

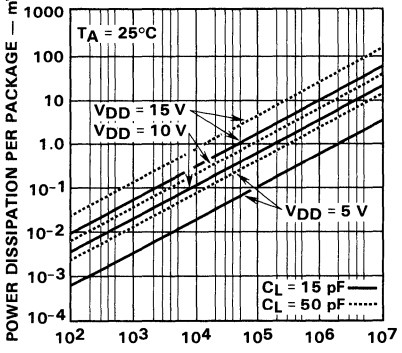
AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay		20	36		10	20		7		ns	C_L = 15 pF
t_{PHL}			20	36		10	20		7		ns	
t_{TLH}	Output Transition Time		20	45		12	25		11	20	ns	Input Transition Times ≤ 20 ns
t_{THL}			20	45		12	25		11	20	ns	
t_{PLH}	Propagation Delay		32	64		16	32		13		ns	C_L = 50 pF
t_{PHL}			32	64		16	32		13		ns	
t_{TLH}	Output Transition Time		45	135		23	70		18	45	ns	Input Transition Times ≤ 20 ns
t_{THL}			45	135		23	70		18	45	ns	

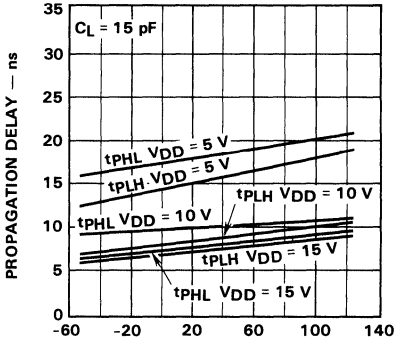
NOTE:
1. Propagation Delays and Output Transition Times are graphically described in this section under 34000 Series CMOS Family Characteristics.

TYPICAL ELECTRICAL CHARACTERISTICS

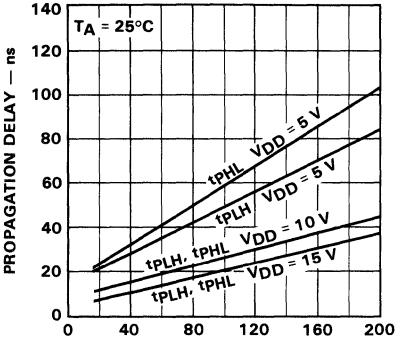
POWER DISSIPATION VERSUS FREQUENCY



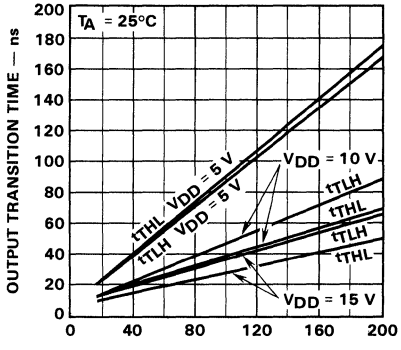
PROPAGATION DELAY VERSUS TEMPERATURE



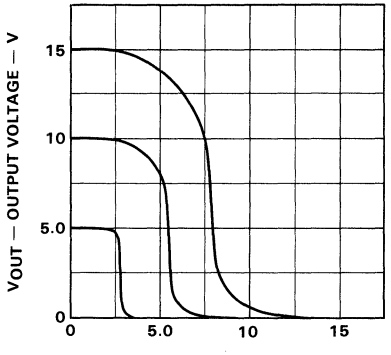
PROPAGATION DELAY VERSUS LOAD CAPACITANCE



OUTPUT TRANSITION TIME VERSUS LOAD CAPACITANCE



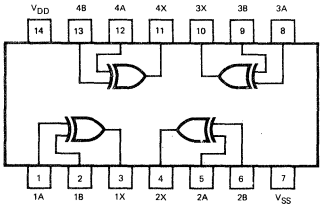
TYPICAL VOLTAGE TRANSFER CHARACTERISTICS FOR THE UNBUFFERED 34069 HEX INVERTER



QUAD EXCLUSIVE-OR GATE

DESCRIPTION — The 34070 CMOS logic element provides the Exclusive-OR function. The outputs are fully buffered for best performance.

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



$X = \overline{A}B + A\overline{B}$

NOTE:
The Flatpak version has the same pinout (Connection Diagram) as the Dual In-Line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V

SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEMP	TEST CONDITIONS
I_{DD}	Quiescent Power Supply Current	XC			5.0			10.0		2.0		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					70.0			140.0		18.0			MAX	
		XM			0.5			1.0		0.2		μA	MIN, 25°C	
					30.0			60.0		12.0			MAX	

NOTE: Additional DC Characteristics are listed in this section under 34000 Series CMOS Family Characteristics.

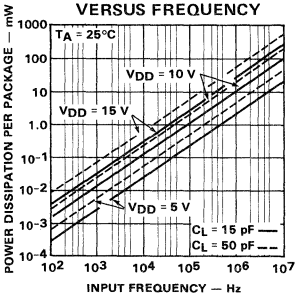
AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C

SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEST CONDITIONS
t_{PLH}	Propagation Delay,		65	130		33	65		23		ns	
t_{PHL}	A or B to X		65	130		33	65		23		ns	C_L = 15 pF
t_{TLH}	Output Transition		23	45		10	25		8	20	ns	Input Transition Times ⩽ 20 ns
t_{THL}	Time		23	45		10	25		8	20	ns	
t_{PLH}	Propagation Delay,		85	170		45	90		27		ns	
t_{PHL}	A or B to X		85	170		45	90		27		ns	C_L = 50 pF
t_{TLH}	Output Transition		50	100		23	50		17	35	ns	Input Transition Times ⩽ 20 ns
t_{THL}	Time		50	100		23	50		17	35	ns	

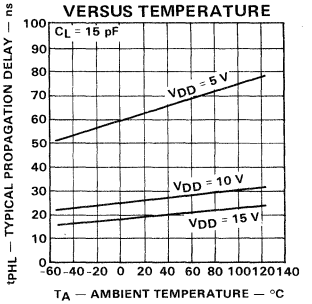
NOTE: Propagation delays and output transition times are graphically described in this section under 34000 Series CMOS Family Characteristics.

TYPICAL ELECTRICAL CHARACTERISTICS

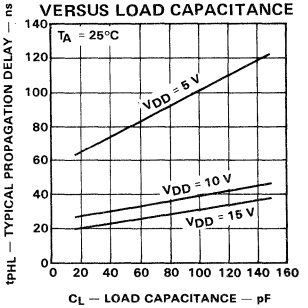
POWER DISSIPATION VERSUS FREQUENCY



PROPAGATION DELAY VERSUS TEMPERATURE



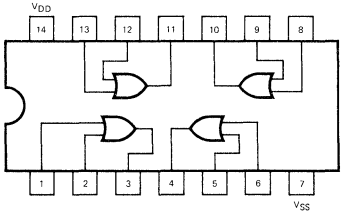
PROPAGATION DELAY VERSUS LOAD CAPACITANCE



QUAD 2-INPUT OR GATE

DESCRIPTION — The 34071 is a positive logic Quad 2-Input OR Gate. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V

SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEMP	TEST CONDITIONS
I_{DD}	Quiescent Power Supply Current	XC			0.5			5.0		1.0		MIN, 25°C	All inputs common and at 0 V or V_{DD}
					15.0			30.0		6.0	µA	MAX	
		XM			0.05			0.1		0.02		MIN, 25°C	
					3.0			6.0		1.2	µA	MAX	

NOTE: Additional DC Characteristics are listed in this section under 34000 Series CMOS Family Characteristics.

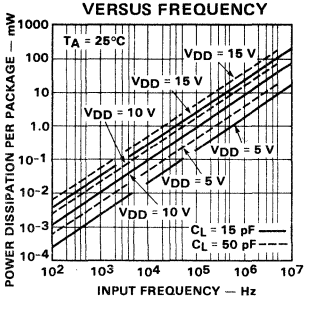
AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C

SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEST CONDITIONS
t_{PLH}	Propagation Delay		30	60		15	30		11		ns	
t_{PHL}			35	60		14	30		11		ns	C_L = 15 pF
t_{TLH}	Output Transition		19	75		10	40		8	25	ns	Input Transition Times ⩽ 20 ns
t_{THL}	Time		24	75		10	40		7	25	ns	
t_{PLH}	Propagation Delay		43	85		22	40		17		ns	
t_{PHL}			52	100		23	40		15		ns	C_L = 50 pF
t_{TLH}	Output Transition		45	135		24	70		18	45	ns	Input Transition Times ⩽ 20 ns
t_{THL}	Time		54	135		21	70		15	45	ns	

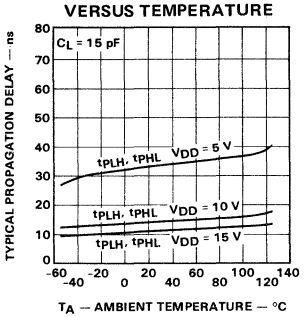
NOTE:
1. Propagation Delays and Output Transition Times are graphically described in this section under 34000 Series CMOS Family Characteristics.

TYPICAL ELECTRICAL CHARACTERISTICS

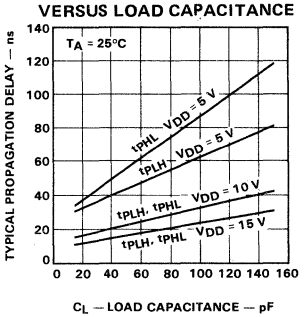
POWER DISSIPATION VERSUS FREQUENCY



PROPAGATION DELAY VERSUS TEMPERATURE



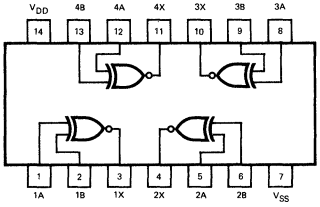
PROPAGATION DELAY VERSUS LOAD CAPACITANCE



QUAD EXCLUSIVE-NOR GATE

DESCRIPTION — The 34077 CMOS logic element provides the Exclusive-NOR function. The outputs are fully buffered for best performance. The 34077 may be used interchangeably for the 4811.

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



$X = AB + \overline{A}\overline{B}$

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V

SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEMP	TEST CONDITIONS
I_{DD}	Quiescent Power Supply Current	XC			5.0			10.0		2.0		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					70.0			140.0		28.0			MAX	
		XM			0.5			1.0		0.2		μA	MIN, 25°C	
					30.0			60.0		12.0			MAX	

NOTE: Additional DC Characteristics are listed in this section under 34000 Series CMOS Family Characteristics.

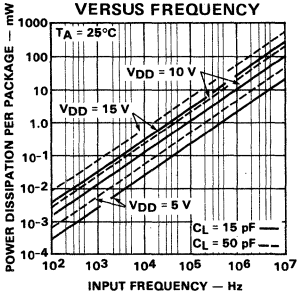
AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C

SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEST CONDITIONS
t_{PLH}	Propagation Delay,		45	90		20	40		15		ns	
t_{PHL}	A or B to X		55	110		20	40		17		ns	C_L = 15 pF
t_{TLH}	Output Transition		23	45		10	25		7	20	ns	Input Transition Times ⩽ 20 ns
t_{THL}	Time		23	45		10	25		7	20	ns	
t_{PLH}	Propagation Delay,		55	110		27	55		17		ns	
t_{PHL}	A or B to X		65	130		27	55		20		ns	C_L = 50 pF
t_{TLH}	Output Transition		53	100		20	50		15	35	ns	Input Transition Times ⩽ 20 ns
t_{THL}	Time		53	100		20	50		15	35	ns	

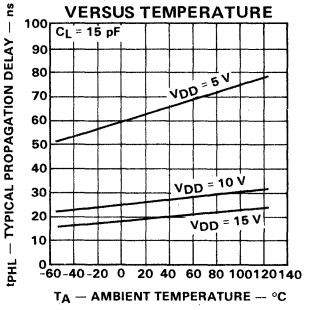
NOTE: Propagation delays and output transition times are graphically described in this section under 34000 Series CMOS Family Characteristics.

TYPICAL ELECTRICAL CHARACTERISTICS

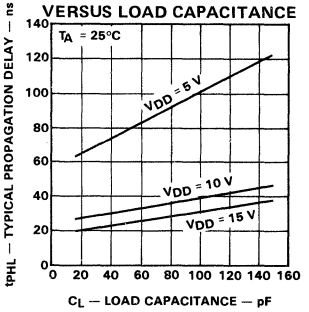
POWER DISSIPATION VERSUS FREQUENCY



PROPAGATION DELAY VERSUS TEMPERATURE



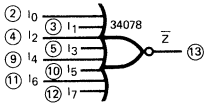
PROPAGATION DELAY VERSUS LOAD CAPACITANCE



8-INPUT NOR GATE

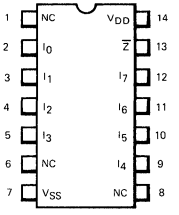
DESCRIPTION – This CMOS logic element provides the positive 8-Input NOR function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

34078 LOGIC SYMBOL



V_{DD} = Pin 14
V_{SS} = Pin 7
NC = Pins 1, 6, 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



PIN NAMES

I_0–I_7	NOR Gate Inputs
$\overline{Z}$	Output (Active LOW)

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V

SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V			LIMITS V_{DD} = 10 V			LIMITS V_{DD} = 15 V			UNITS	TEMP	TEST CONDITIONS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			0.5			5.0		1.0		µA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					15.0			30.0		6.0			MAX	
		XM			0.05			0.1		0.02		µA	MIN, 25°C	
					3.0			6.0		1.2			MAX	

NOTE: Additional DC Characteristics are listed in this section under 34000 Series CMOS Family Characteristics.

AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C

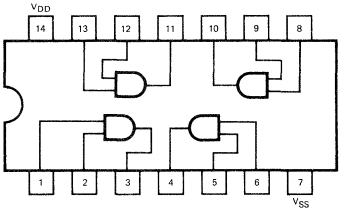
SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V			LIMITS V_{DD} = 10 V			LIMITS V_{DD} = 15 V			UNITS	TEST CONDITIONS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay		87			36			27		ns	
t_{PHL}			102			40			29		ns	C_L = 15 pF
t_{TLH}	Output Transition Time		35			20			16		ns	Input Transition Times ⩽ 20 ns
t_{THL}			37			17			15		ns	
t_{PLH}	Propagation Delay		108			46			34		ns	
t_{PHL}			129			50			35		ns	C_L = 50 pF
t_{TLH}	Output Transition Time		76			39			30		ns	Input Transition Times ⩽ 20 ns
t_{THL}			80			32			24		ns	

NOTE:
Propagation delays and output transition times are graphically described in this section under 34000 Series CMOS Family Characteristics.

QUAD 2-INPUT AND GATE

DESCRIPTION — The 34081 is a positive logic Quad 2-Input AND Gate. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V

SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V MIN	TYP	MAX	LIMITS V_{DD} = 10 V MIN	TYP	MAX	LIMITS V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEMP	TEST CONDITIONS
I_{DD}	Quiescent Power Supply Current	XC			0.5			5.0		1.0		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					15.0			30.0		6.0			MAX	
		XM			0.05			0.1		0.02		μA	MIN, 25°C	
					3.0			6.0		1.2			MAX	

NOTE: Additional DC Characteristics are listed in this section under 34000 Series CMOS Family Characteristics.

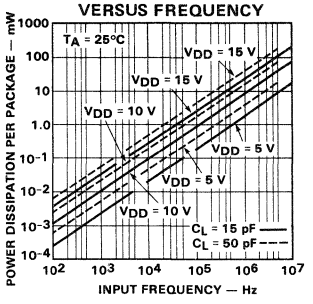
AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C

SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V MIN	TYP	MAX	LIMITS V_{DD} = 10 V MIN	TYP	MAX	LIMITS V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEST CONDITIONS
t_{PLH}	Propagation Delay		35	60		16	33		11		ns	
t_{PHL}			35	60		18	33		13		ns	C_L = 15 pF
t_{TLH}	Output Transition		27	75		13	40		10	25	ns	Input Transition Times ⩽ 20 ns
t_{THL}	Time		25	75		10	40		7	25	ns	
t_{PLH}	Propagation Delay		55	95		23	50		17		ns	
t_{PHL}			60	95		25	50		19		ns	C_L = 50 pF
t_{TLH}	Output Transition		70	135		30	70		23	45	ns	Input Transition Times ⩽ 20 ns
t_{THL}	Time		57	135		23	70		16	45	ns	

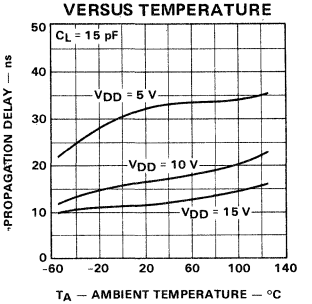
NOTE:
1. Propagation Delays and Output Transition Times are graphically described in this section under 34000 Series CMOS Family Characteristics.

TYPICAL ELECTRICAL CHARACTERISTICS

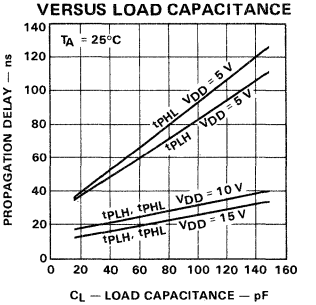
POWER DISSIPATION VERSUS FREQUENCY



PROPAGATION DELAY VERSUS TEMPERATURE



PROPAGATION DELAY VERSUS LOAD CAPACITANCE



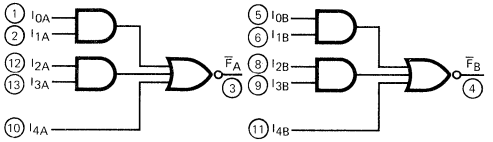
DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATE

DESCRIPTION — The 34085 is a Dual 2-Wide 2-Input AND-OR-Invert (AOI) Gate, each with an additional input (I_{4A} or I_{4B}) which can be used as either an Expander Input or an Inhibit Input by connecting it to any standard CMOS output. A HIGH on this Input (I_4) forces the Output ($\overline{F}$) LOW independent of the other four inputs (I_0-I_3). The Outputs ($\overline{F_A}$ and $\overline{F_B}$) are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

PIN NAMES

I_{0A}-I_{4A}, I_{0B}-I_{4B}	Gate Inputs
$\overline{F}_A$, $\overline{F}_B$	Outputs (Active LOW)

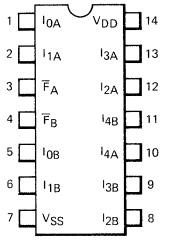
LOGIC DIAGRAM



$\overline{F} = \overline{I_0 \bullet I_1 + I_2 \bullet I_3 + I_4}$

V_{DD} = Pin 14
V_{SS} = Pin 7

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V

SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEMP	TEST CONDITIONS
I_{DD}	Quiescent Power Supply Current	XC			0.5			5.0		1.0		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					15.0			30.0		6.0			MAX	
		XM			0.05			0.1		0.02		μA	MIN, 25°C	
					3.0			6.0		1.2			MAX	

NOTE: Additional DC Characteristics are listed in this section under 34000 Series CMOS Family Characteristics.

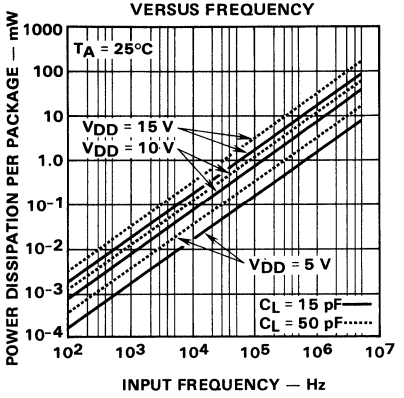
AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C

SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEST CONDITIONS
t_{PLH}	Propagation Delay,		40	80		18	40		12		ns	
t_{PHL}	Any I to $\overline{F}$		54	100		28	50		15		ns	C_L = 15 pF
t_{TLH}	Output Transition		20	45		12	25		10	20	ns	Input Transition Times ⩽20 ns
t_{THL}	Time		20	45		12	25		10	20	ns	
t_{PLH}	Propagation Delay,		56	115		25	55		17		ns	
t_{PHL}	Any I to $\overline{F}$		74	135		30	65		20		ns	C_L = 50 pF
t_{TLH}	Output Transition		45	100		22	50		15	35	ns	Input Transition Times ⩽20 ns
t_{THL}	Time		45	100		22	50		15	35	ns	

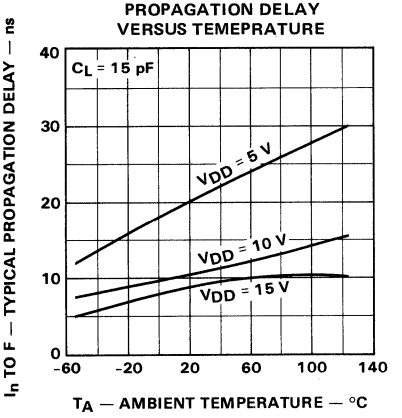
NOTE:
1. Propagation Delays and Output Transition Times are graphically described in this section under 34000 Series CMOS Family Characteristics.

TYPICAL ELECTRICAL CHARACTERISTICS

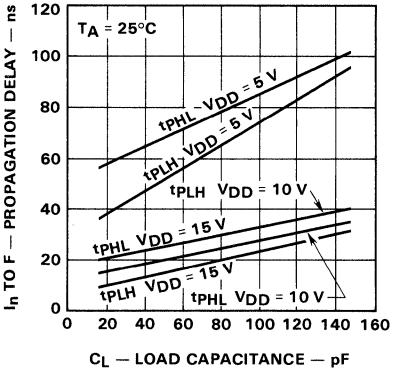
POWER DISSIPATION
VERSUS FREQUENCY



PROPAGATION DELAY
VERSUS TEMEPRATURE



PROPAGATION DELAY
VERSUS LOAD CAPACITANCE



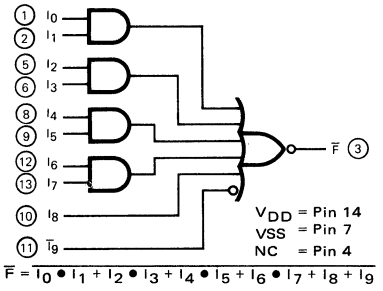
4-WIDE 2-INPUT AND-OR-INVERT GATE

DESCRIPTION – The 34086 is a 4-Wide 2-Input AND-OR-Invert (AOI) Gate with two additional inputs (I_8 and $\overline{I_9}$) which can be used as either expander inputs or inhibit inputs by connecting them to any standard CMOS output. A HIGH on I_8 or a LOW on $\overline{I_9}$ forces the Output ($\overline{F}$) LOW independent of the other eight inputs (I_0–I_7). The Output ($\overline{F}$) is fully buffered for highest noise immunity and pattern insensitivity of output impedance.

PIN NAMES

I_0–I_8	Gate Inputs
$\overline{I_9}$	Gate Input (Active LOW)
$\overline{F}$	Output (Active LOW)

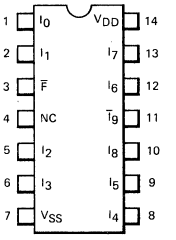
LOGIC DIAGRAM



$\overline{F} = \overline{I_0 \bullet I_1 + I_2 \bullet I_3 + I_4 \bullet I_5 + I_6 \bullet I_7 + I_8 + I_9}$

NOTE:
A HIGH on I_8 or a LOW on $\overline{I_9}$ forces the output ($\overline{F}$) LOW.

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V

SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEMP	TEST CONDITIONS
I_{DD}	Quiescent Power Supply Current	XC			0.5			5.0		1.0		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					15.0			30.0		6.0			MAX	
		XM			0.05			0.1		0.02		μA	MIN, 25°C	
					3.0			6.0		1.2			MAX	

NOTE: Additional DC Characteristics are listed in this section under 34000 Series CMOS Family Characteristics.

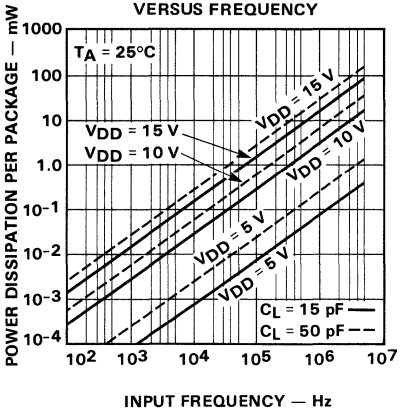
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C

SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEST CONDITIONS
t_{PLH}	Propagation Delay, I_0 through I_8 to $\overline{F}$		80	150		35	70		20		ns	
t_{PHL}			80	150		35	70		20		ns	
t_{PLH}	Propagation Delay, $\overline{I_9}$ to $\overline{F}$		40	60		20	30		10		ns	C_L = 15 pF
t_{PHL}			40	60		20	30		10		ns	Input Transition Times ⩽20 ns
t_{TLH}	Output Transition Time		25	45		12	25		8	20	ns	
t_{THL}			25	45		12	25		8	20	ns	
t_{PLH}	Propagation Delay, I_0 through I_8 to $\overline{F}$		100	180		40	80		25		ns	
t_{PHL}			100	180		40	80		25		ns	
t_{PLH}	Propagation Delay, $\overline{I_9}$ to $\overline{F}$		65	100		35	50		20		ns	C_L = 50 pF
t_{PHL}			65	100		35	50		20		ns	Input Transition Times ⩽ 20 ns
t_{TLH}	Output Transition Time		55	100		25	50		18	35	ns	
t_{THL}			55	100		25	50		18	35	ns	

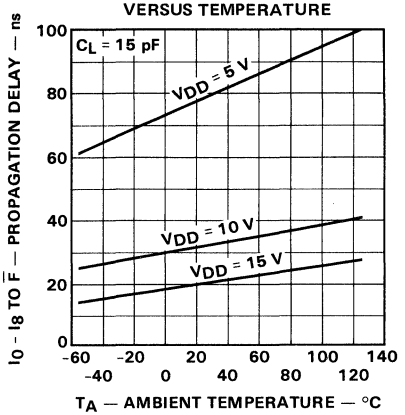
NOTE:
1. Propagation Delays and Output Transition Times are graphically described in this section under 34000 Series CMOS Family Characteristics.

TYPICAL ELECTRICAL CHARACTERISTICS

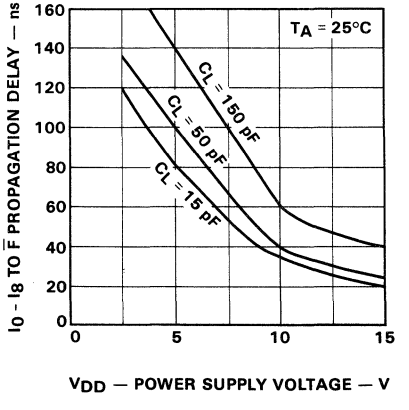
POWER DISSIPATION
VERSUS FREQUENCY



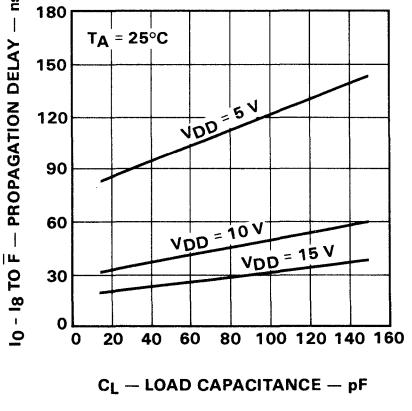
PROPAGATION DELAY
VERSUS TEMPERATURE



PROPAGATION DELAY
VERSUS
POWER SUPPLY VOLTAGE



PROPAGATION DELAY
VERSUS LOAD CAPACITANCE



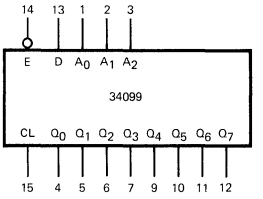
34099
8-BIT ADDRESSABLE LATCH

DESCRIPTION – The 34099 is an 8-Bit Addressable Latch with three Address Inputs (A_0-A_2), a Data Input (D), an active LOW Enable Input ($\overline{E}$), an active HIGH Clear Input (CL) and eight Parallel Latch Outputs (Q_0-Q_7).

When the Enable ($\overline{E}$) and the Clear (CL) Inputs are HIGH, all Outputs (Q_0-Q_7) are LOW. Eight-channel demultiplexing or active HIGH 1-of-8 decoding with output enable operation occurs when the Clear Input (CL) is HIGH and the Enable Input ($\overline{E}$) is LOW.

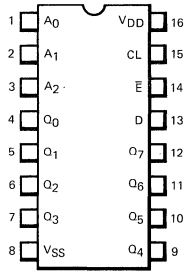
When the Clear (CL) and Enable ($\overline{E}$) Inputs are LOW, the selected Output (Q_0-Q_7)(determined by the address Inputs A_0-A_2) follows the Data Input (D). When the Enable Input ($\overline{E}$) goes HIGH, the contents of the latch are stored. When operating in the addressable latch mode ($\overline{E}$ = CL = LOW), changing more than one bit of the address (A_0-A_2) could impose a transient wrong address. Therefore, this should only be done while in the memory mode ($\overline{E}$ = HIGH, CL = LOW).

LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



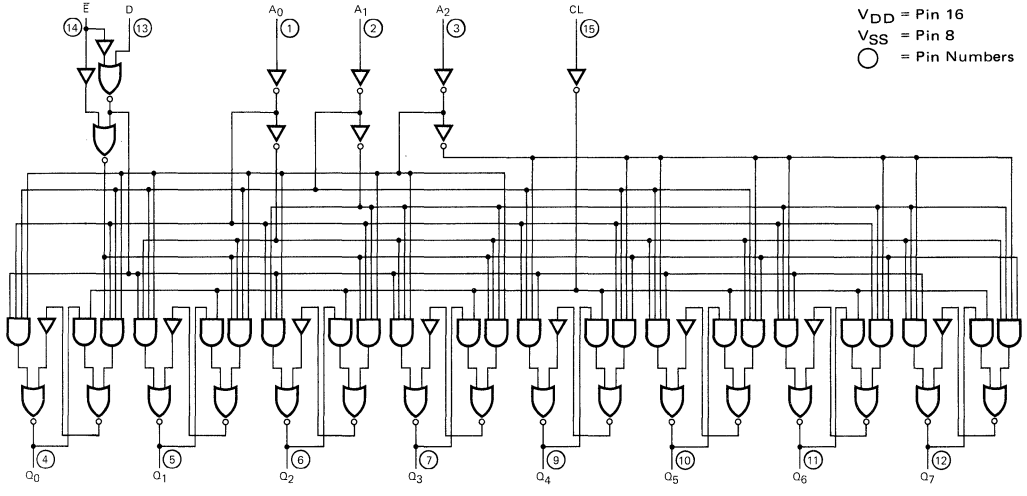
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

- **SERIAL-TO-PARALLEL CAPABILITY**
- **EIGHT BITS OF STORAGE WITH THE OUTPUT OF EACH BIT AVAILABLE**
- **RANDOM (ADDRESSABLE) DATA ENTRY**
- **ACTIVE HIGH DEMULTIPLEXING OR DECODING CAPABILITY**
- **EASILY EXPANDABLE**
- **COMMON ACTIVE HIGH CLEAR**

PIN NAMES

A_0-A_2	Address Inputs
D	Data Input
$\overline{E}$	Enable Input (Active LOW)
CL	Clear Input (Active HIGH)
Q_0-Q_7	Parallel Latch Outputs

LOGIC DIAGRAM



MODE SELECTION

$\overline{E}$	CL	MODE
L	L	Addressable Latch
H	L	Memory
L	H	Active HIGH 8-Channel Demultiplexer
H	H	Clear

L = LOW Level
H = HIGH Level
Q_{N-1} = State Before the Positive Transition of the Enable Input

TRUTH TABLE

						PRESENT OUTPUT STATES								
CL	$\overline{E}$	D	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	MODE
H	H	X	X	X	X	L	L	L	L	L	L	L	L	CLEAR
H	L	L	L	L	L	L	L	L	L	L	L	L	L	DEMULTIPLEX
H	L	H	L	L	L	H	L	L	L	L	L	L	L	
H	L	L	H	L	L	L	L	L	L	L	L	L	L	
H	L	H	H	L	L	L	H	L	L	L	L	L	L	
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	
H	L	H	H	H	H	L	L	L	L	L	L	L	H	
L	H	X	X	X	X	Q_{N-1} →								MEMORY
L	L	L	L	L	L	L	Q_{N-1}	Q_{N-1}	Q_{N-1} →					ADDRESSABLE
L	L	H	L	L	L	H	Q_{N-1}	Q_{N-1} →						LATCH
L	L	L	H	L	L	Q_{N-1}	L	Q_{N-1} →						
L	L	H	H	L	L	Q_{N-1}	H	Q_{N-1} →						
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮						
L	L	L	H	H	H	Q_{N-1} →						Q_{N-1}	L	
L	L	H	H	H	H	Q_{N-1} →						Q_{N-1}	H	

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			10			20		4		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					100			200		40			MAX	
		XM			1			2		0.4		μA	MIN, 25°C	
					15			30		6			MAX	

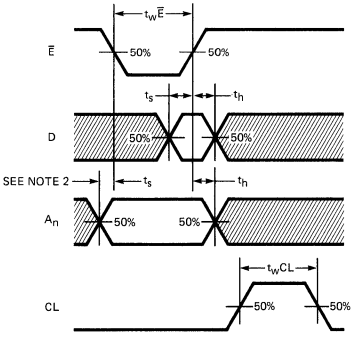
NOTE: Additional DC Characteristics are listed in this section under 34000 Series CMOS Family Characteristics.

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, $\bar{E}$ to Q_n		90 90			40 40			30 30		ns ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
t_{PLH} t_{PHL}	Propagation Delay, D to Q_n		75 75			35 35			25 25		ns ns	
t_{PLH} t_{PHL}	Propagation Delay, Address to Q_n		100 100			45 45			35 35		ns ns	
t_{PHL}	Propagation Delay, CL to Q_n		75			35			25		ns	
t_{TLH} t_{THL}	Output Transition Time		40 40			20 20			15 15		ns ns	
t_{PLH} t_{PHL}	Propagation Delay, $\bar{E}$ to Q_n		110 110			50 50			35 35		ns ns	C_L = 50 pF Input Transition Times ⩽ 20 ns
t_{PLH} t_{PHL}	Propagation Delay, D to Q_n		95 95			45 45			30 30		ns ns	
t_{PLH} t_{PHL}	Propagation Delay, Address to Q_n		120 120			55 55			40 40		ns ns	
t_{PHL}	Propagation Delay, CL to Q_n		95			45			30		ns	
t_{TLH} t_{THL}	Output Transition Time		75 75			40 40			25 25		ns ns	
t_s t_h	Set-Up Time, D to $\bar{E}$ Hold Time, D to $\bar{E}$		30 40			10 20			5 20		ns ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
t_s t_h	Set-Up Time, Address to $\bar{E}$ Hold Time, Address to $\bar{E}$		30 40			10 20			5 20		ns ns	
$t_w\bar{E}$	Minimum $\bar{E}$ Pulse Width		50			20			15		ns	
t_wCL	Minimum CL Pulse Width		50			20			15		ns	

NOTES:
1. Propagation Delays and Output Transition Times are graphically described in this section under 34000 Series CMOS Family Characteristics.
2. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Set-up Times (t_s), Hold Times (t_h), and Minimum Pulse Widths (t_w) do not vary with load capacitance.

SWITCHING WAVEFORMS



MINIMUM PULSE WIDTH FOR $\bar{E}$ AND CL AND SET-UP AND HOLD TIMES, D TO $\bar{E}$ AND A_n TO $\bar{E}$

NOTES:
1. Set-up and Hold Times are shown as positive values but may be specified as negative values.
2. The Address to Enable Set-up Time is the time before the HIGH-to-LOW Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.

34104
QUAD LOW VOLTAGE TO HIGH VOLTAGE TRANSLATER WITH 3-STATE OUTPUTS

DESCRIPTION – The 34104 Quad Low Voltage to High Voltage Translator with 3-State Outputs provides the capability of interfacing low voltage circuits to high voltage circuits, such as low voltage CMOS and TTL to high voltage CMOS. It has four Data Inputs (I_0-I_3), an active HIGH Output Enable input (EO), four Data Outputs (Z_0-Z_3) and their Complements ($\overline{Z}_0$-$\overline{Z}_3$). With the Output Enable input HIGH, the Outputs (Z_0-Z_3, $\overline{Z}_0$-$\overline{Z}_3$) are in the low impedance "ON" state, either HIGH or LOW as determined by the Data Inputs; with the Output Enable input LOW, the Outputs are in the high impedance "OFF" state.

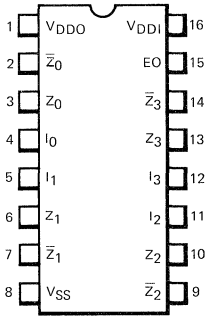
The device uses a common negative supply (V_{SS}) and separate positive supplies for inputs (V_{DDI}) and outputs (V_{DDO}). V_{DDI} must always be less than or equal to V_{DDO}, even during power turn-on and turn-off. For the allowable operating range of V_{DDI} and V_{DDO} see Figure 1. Each input protection circuit is terminated between V_{DDO} and V_{SS}. This allows the input signals to be driven from any potential between V_{DDO} and V_{SS}, without regard to current limiting. When driving from potentials greater than V_{DDO} or less than V_{SS}, the current at each input must be limited to 10 mA.

When used in a bus organized system, all 34104 devices on the same bus line should be connected to the same V_{DDO} and V_{SS} supplies. Otherwise, parasitic diodes from the output to V_{DDO} and V_{SS} can become forward biased, even while the device is in the OFF state, causing catastrophic failure if the current is not limited to 10 mA.

- **3-STATE FULLY BUFFERED OUTPUTS**
- **OUTPUT ENABLE INPUT (ACTIVE HIGH)**
- **DUAL POWER SUPPLY**

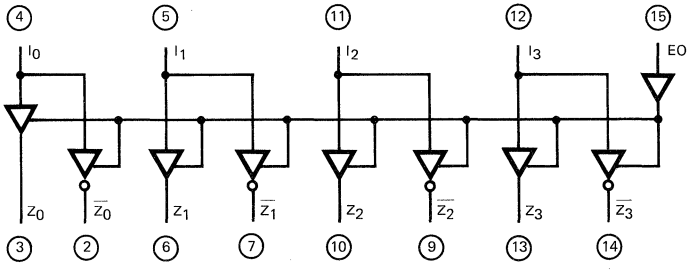
PIN NAMES	FUNCTION
I_0–I_3	Data Inputs
EO	Output Enable Input
Z_0–Z_3	Data Outputs
$\overline{Z}_0$–$\overline{Z}_3$	Complimentary Data Outputs

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC SYMBOL



V_{DDO} = Pin 1
V_{DDI} = Pin 16
V_{SS} = Pin 8
○ = Pin Number

DC CHARACTERISTICS: $V_{DDO} = V_{DDI}$ as shown, $V_{SS} = 0$ V

SYMBOL	PARAMETER		LIMITS $V_{DDO/I} = 5$ V MIN	TYP	MAX	LIMITS $V_{DDO/I} = 10$ V MIN	TYP	MAX	LIMITS $V_{DDO/I} = 15$ V MIN	TYP	MAX	UNITS	TEMP	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		3.5		*	7.0		*	10.5		*	V	All	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage		**		1.5	**		3.0	**		4.5	V	All	Guaranteed Input LOW Voltage
V_{OH}	Output HIGH Voltage		4.99			9.99			14.99			V	MIN, 25°C	$I_{OH} = 0$ mA
			4.95			9.95			14.95				MAX	Note 1
			4.0			9.0			13.0				All	$I_{OH} = 0$ mA Note 2
V_{OL}	Output LOW Voltage				0.01			0.01			0.01	V	MIN, 25°C	$I_{OL} = 0$ mA
					0.05			0.05			0.05		MAX	Note 1
					0.5			1.0			2.0		All	$I_{OL} = 0$ mA Note 2
I_I	Input Current	XC			0.1			0.1			1.0	µA	25°C	Lead Under Test at 0 V or V_{DDO}. All Other Inputs Simultaneously at 0 V or V_{DDO}
		XM			0.01			0.01			1.0			
I_{OH}	Output HIGH Current		-1.5									mA	MIN, 25°C	$V_{OUT} = 2.5$ V for
			-1.0										MAX	$V_{DDO} = 5$ V Note 1
			-0.7			-1.4			-2.2				MIN, 25°C	$V_{OUT} = V_{DDO} - 0.5$ V
			-0.4			-0.8			-1.4				MAX	Note 1
I_{OL}	Output LOW Current		1.0			2.6			3.6			mA	MIN	$V_{OUT} = 0.4$ V for
			0.8			2.0			3.6				25°C	$V_{DDO} = 5$ V
			0.4			1.2			2.0				MAX	$V_{OUT} = 0.5$ V for $V_{DDO} = 10$ V $V_{OUT} = 0.5$ V for $V_{DDO} = 15$ V Note 1
I_{OZH} Note 3	Output OFF Current HIGH,XM				0.05			0.1		0.02		µA	MIN, 25°C	Output Returned
					3.0			6.0		1.2			MAX	to V_{DDO}, EO = V_{SS}
I_{OZL} Note 3	Output OFF Current LOW,XM				-0.05			-0.1		-0.02		µA	MIN, 25°C	Output Returned
					-3.0			-6.0		-1.2			MAX	to V_{SS}, EO = V_{SS}
I_{DD}	Quiescent Power Supply Current	XC			50			100		20		µA	MIN, 25°C	All Inputs Common and at 0 V or V_{DDI}
					700			1400		280			MAX	
		XM			5			300		60		µA	MIN, 25°C	
					10			600		120			MAX	

*V_{IH} must be less than or equal to V_{DDO}. If V_{IH} is greater than V_{DDO}, current at each input must be limited to 10 mA.
**V_{IL} must be greater than or equal to V_{SS}. If V_{IL} is less than V_{SS}, current at each input must be limited to 10 mA.

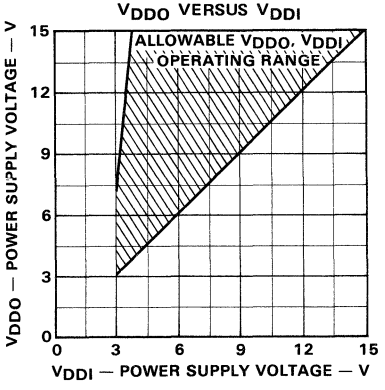
Notes:
1. Inputs at 0 V or V_{DDO} per function.
2. Inputs at 0.3 V_{DDO} or 0.7 V_{DD} per function.
3. For I_{OZH} and I_{OZL} commercial product limits, multiply the above military product limits by 10.

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DDI} = 5 V, V_{DDO} as shown, V_{SS} = 0 V, T_A = 25°C

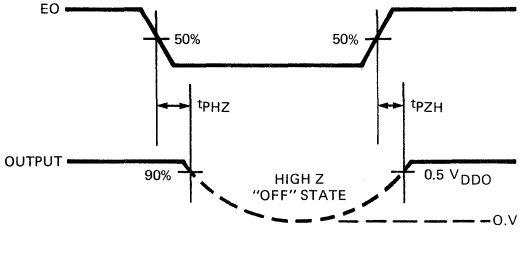
SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DDO} = 5 V			V_{DDO} = 10 V			V_{DDO} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay,		135			75			65		ns	C_L = 15 pF
t_{PHL}	I_n to Z_n or $\overline{Z_n}$		135			75			65		ns	Input Transition Times ≤ 20 ns
t_{PZH}	Output Enable		190			95			75		ns	R_L = 1 kΩ to V_{SS}
t_{PZL}	Time		185			90			75		ns	R_L = 1 kΩ to V_{DDO}
t_{PHZ}	Output Disable		100			75			70		ns	R_L = 1 kΩ to V_{SS}
t_{PLZ}	Time		100			70			60		ns	R_L = 1 kΩ to V_{DDO}
t_{TLH}	Output Transition		30			18			16		ns	
t_{THL}	Time		30			18			16		ns	
t_{PLH}	Propagation Delay,		160			85			75		ns	C_L = 50 pF
t_{PHL}	I_n to Z_n or $\overline{Z_n}$		160			85			75		ns	Input Transition Times ≤ 20 ns
t_{PZH}	Output Enable		200			100			80		ns	R_L = 1 kΩ to V_{SS}
t_{PZL}	Time		200			100			80		ns	R_L = 1 kΩ to V_{DDO}
t_{PHZ}	Output Disable		115			80			75		ns	R_L = 1 kΩ to V_{SS}
t_{PLZ}	Time		110			80			70		ns	R_L = 1 kΩ to V_{DDO}
t_{TLH}	Output Transition		60			30			25		ns	
t_{THL}	Time		60			30			25		ns	

NOTE:
1. Propagation Delays and Output Transition Times are graphically described in this section under 34000 Series CMOS Family Characteristics.

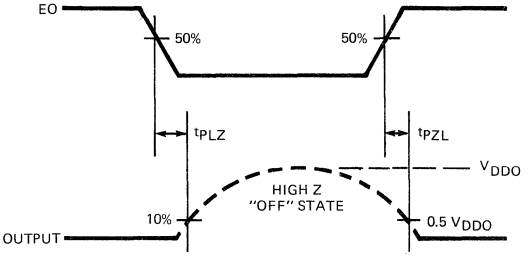
Fig. 1 TYPICAL ELECTRICAL CHARACTERISTICS



SWITCHING WAVEFORMS



OUTPUT ENABLE TIME (t_{PZH}) AND OUTPUT DISABLE TIME (t_{PHZ})

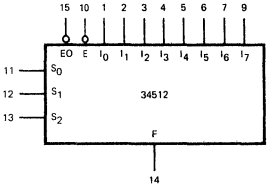


OUTPUT ENABLE TIME (t_{PZL}) AND OUTPUT DISABLE TIME (t_{PLZ})

34512
8-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

DESCRIPTION — The 34512 is an 8-Input Multiplexer with Active LOW logic and output enables ($\overline{E}$, $\overline{EO}$). One of eight binary inputs is selected by Select Inputs S_0, S_1 and S_2 and is routed to the output F. A HIGH on the Output Enable ($\overline{EO}$) causes the F output to assume a high impedance or "OFF" state, regardless of other input conditions. This allows the output to interface directly with bus oriented systems (3-state). When the active LOW Enable ($\overline{E}$) is HIGH, it forces the output LOW provided the Output Enable ($\overline{EO}$) is LOW. By proper manipulation of the inputs, the 34512 can provide any logic functions of four variables. The 34512 cannot be used to multiplex analog signals.

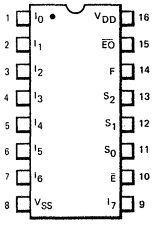
LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

- SELECTS ONE-OF-EIGHT DATA SOURCES
- PERFORMS PARALLEL-TO-SERIAL CONVERSION
- 3-STATE OUTPUTS WITH ACTIVE LOW OUTPUT ENABLE
- ACTIVE LOW LOGIC ENABLE

CONNECTION DIAGRAM
DIP (TOP VIEW)

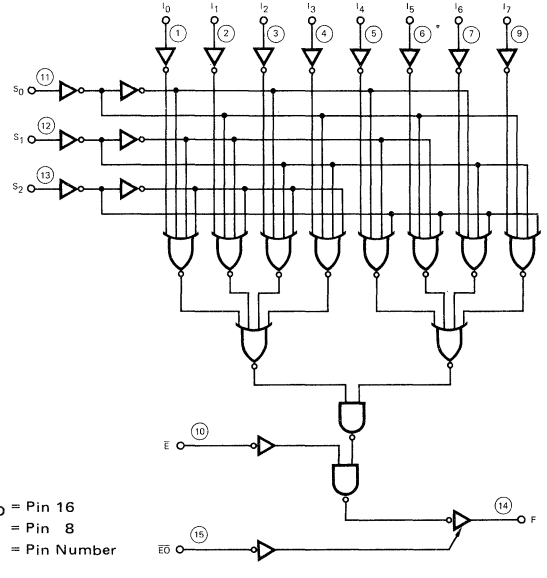


NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

S_0, S_1, S_2	Select Inputs
$\overline{EO}$	Output Enable (Active LOW)
$\overline{E}$	Enable (Active LOW)
I_0 to I_7	Multiplexer Inputs
F	Multiplexer Output

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Number

TRUTH TABLE

INPUTS													OUTPUT
$\overline{EO}$	$\overline{E}$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	F
L	H	X	X	X	X	X	X	X	X	X	X	X	L
L	L	L	L	L	L	X	X	X	X	X	X	X	L
L	L	L	L	L	H	X	X	X	X	X	X	X	H
L	L	L	L	H	X	L	X	X	X	X	X	X	L
L	L	L	L	H	X	H	X	X	X	X	X	X	H
L	L	L	H	L	X	X	L	X	X	X	X	X	L
L	L	L	H	L	X	X	H	X	X	X	X	X	H
L	L	L	H	H	X	X	X	L	X	X	X	X	L
L	L	L	H	H	X	X	X	H	X	X	X	X	H
L	L	H	L	L	X	X	X	X	L	X	X	X	L
L	L	H	L	L	X	X	X	X	H	X	X	X	H
L	L	H	L	H	X	X	X	X	X	L	X	X	L
L	L	H	L	H	X	X	X	X	X	H	X	X	H
L	L	H	H	L	X	X	X	X	X	X	L	X	L
L	L	H	H	L	X	X	X	X	X	X	H	X	H
L	L	H	H	H	X	X	X	X	X	X	X	L	L
L	L	H	H	H	X	X	X	X	X	X	X	H	H
H	X	X	X	X	X	X	X	X	X	X	X	X	Z

L = LOW Level
H = HIGH Level
X = Don't Care
Z = High Impedance State

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V

SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEMP	TEST CONDITIONS
I_{OZH} (Note 2)	Output OFF Current HIGH,XM				0.05 3.0			0.1 6.0		0.02 1.2		μA	MIN, 25°C MAX	Output returned to V_{DD}, $\overline{EO}$ = V_{DD}
I_{OZL} (Note 2)	Output OFF Current LOW,XM				-0.05 -3.0			-0.1 -6.0		-0.02 -1.2		μA	MIN, 25°C MAX	Output returned to V_{SS}, $\overline{EO}$ = V_{DD}
I_{DD}	Quiescent Power Supply Current	XC			30 600			60 1200		12 240		μA	MIN, 25°C MAX	All inputs common and at 0 V or V_{DD}
		XM			5 100			10 200		2 40		μA	MIN, 25°C MAX	

NOTES:
1. Additional DC Characteristics are listed in this section under 34000 Series CMOS Family characteristics.
2. For I_{OZH} and I_{OZL} commercial product limits, multiply the above military product limits by 10.

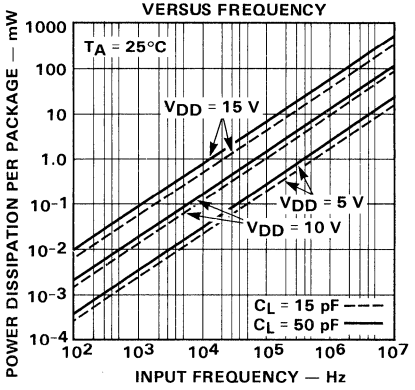
AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C

SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEST CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay, Data to Output		130 130	260 260		65 65	130 130		45 45		ns ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
t_{PLH} t_{PHL}	Propagation Delay, Select to Output		150 150	300 300		75 75	150 150		55 55		ns ns	
t_{PLH} t_{PHL}	Propagation Delay, E to Output		70 70	140 140		35 35	70 70		25 25		ns ns	
t_{PZH} t_{PZL}	Output Enable Time		26 28	70 70		11 11	35 35		10 10		ns ns	(R_L = 1 kΩ to V_{SS}) (R_L = 1 kΩ to V_{DD})
t_{PHZ} t_{PLZ}	Output Disable Time		34 39	90 90		20 20	45 45		15 15		ns ns	(R_L = 1 kΩ to V_{SS}) (R_L = 1 kΩ to V_{DD})
t_{TLH} t_{THL}	Output Transition Time		45 45	100 100		20 20	60 60		15 15	40 40	ns ns	
t_{PLH} t_{PHL}	Propagation Delay, Data to Output		150 150	300 300		75 75	150 150		52 52		ns ns	C_L = 50 pF Input Transition Times ⩽ 20 ns
t_{PLH} t_{PHL}	Propagation Delay, Select to Output		175 175	350 350		85 85	170 170		60 65		ns ns	
t_{PLH} t_{PHL}	Propagation Delay, E to Output		90 90	175 175		45 45	90 90		30 32		ns ns	
t_{PZH} t_{PZL}	Output Enable Time		33 30	85 85		20 22	45 45		18 20		ns ns	(R_L = 1 kΩ to V_{SS}) (R_L = 1 kΩ to V_{DD})
t_{PHZ} t_{PLZ}	Output Disable Time		39 40	100 100		20 20	50 50		15 15		ns ns	(R_L = 1 kΩ to V_{SS}) (R_L = 1 kΩ to V_{DD})
t_{TLH} t_{THL}	Output Transition Time		90 100	200 200		40 40	100 100		33 30	65 65	ns ns	

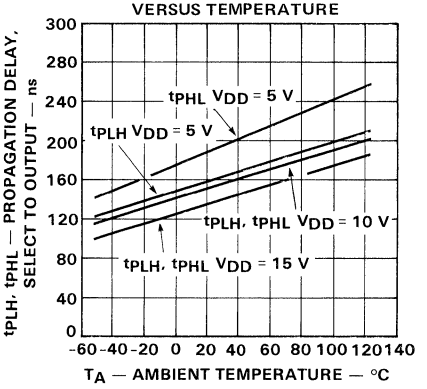
NOTE:
1. Propagation Delays and Output Transition Times are graphically described in this section under 34000 Series CMOS Family Characteristics.

TYPICAL ELECTRICAL CHARACTERISTICS

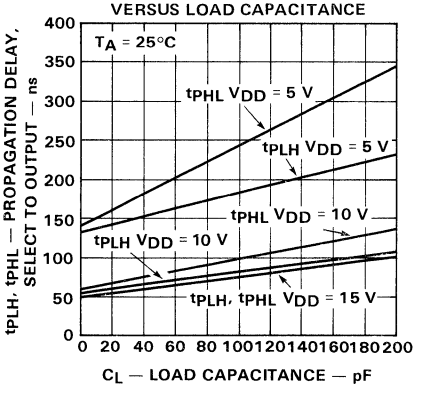
TYPICAL POWER DISSIPATION VERSUS FREQUENCY



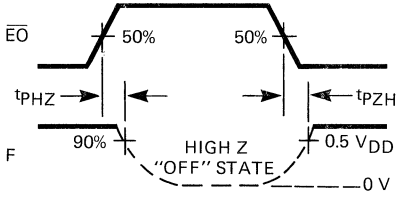
PROPAGATION DELAY VERSUS TEMPERATURE



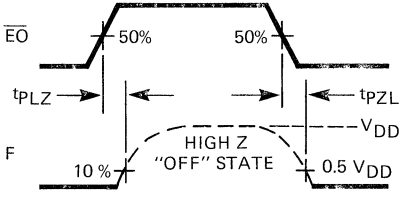
PROPAGATION DELAY VERSUS LOAD CAPACITANCE



SWITCHING WAVEFORMS



OUTPUT ENABLE TIME (t_{PZH}) AND OUTPUT DISABLE TIME (t_{PHZ})



OUTPUT ENABLE TIME (t_{PZL}) AND OUTPUT DISABLE TIME (t_{PLZ})

3

APPLICATIONS

MULTIPLEXER AS A FUNCTION GENERATOR – In most digital systems there are areas, usually in the control section, where a number of inputs generate an output in a highly irregular way. In other words, an unusual function must be generated which is apparently not available as an MSI building block. In such cases, many designers tend to return to classical methods of logic design with NAND and NOR gates using Boolean Algebra, Karnaugh maps and Veitch diagrams for logic minimization. Surprisingly enough, multiplexers can simplify these designs.

The 34512 8-Input multiplexer can generate any one of the 65,536 different functions of four variables. An example will illustrate the technique. Assume four binary inputs are A, B, C and D and F is the desired function (See Fig. 1). If C is connected to S_0, B to S_1 and A to S_2, any combination of A, B and C will select an input (assuming the output is enabled). For each combination of A, B and C, the required output, as a function of the fourth variable D, is either H or L the same as D or the opposite of D. Therefore, the truth table may be examined and each input of the 34512 is connected to V_{DD}, V_{SS}, D or $\overline{D}$ as required and in such fashion the function is generated.

In the example shown, (Fig. 1) the first two outputs are the opposite of D, so I_0 is connected to D. The second two are HIGH, so I_1 is connected to V_{DD}, etc.

32-INPUT MULTIPLEXER – The 3-State Output Enable can be used to expand the 34512. A 32-Input Multiplexer utilizing four 34512s and a 34011 is shown in Fig. 2.

INPUT VARIABLES				REQUIRED FUNCTION
A	B	C	D	F
L	L	L	L	H
L	L	L	H	L
L	L	H	L	H
L	L	H	H	H
L	H	L	L	L
L	H	L	H	H
L	H	H	L	L
L	H	H	H	L
H	L	L	L	L
·	·	·	·	·
·	·	·	·	·
		·	·	·

H = HIGH Level
L = LOW Level

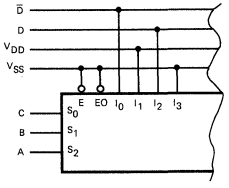


Fig. 1

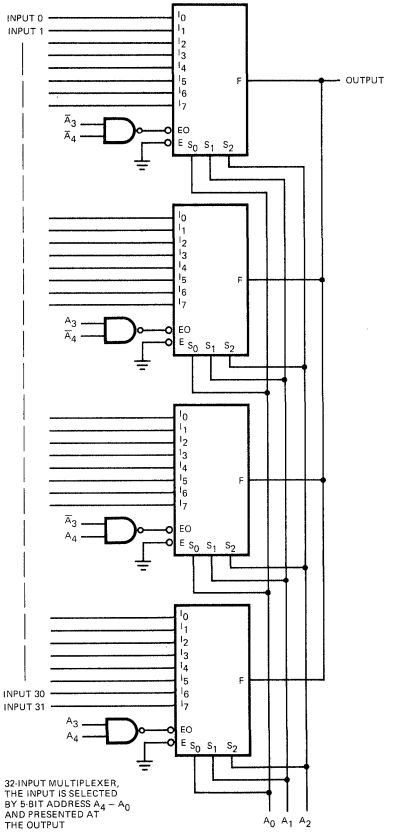


Fig. 2

34518 • 34520

DUAL 4-BIT DECADE/BINARY COUNTERS

DESCRIPTION — The 34518 is a Dual 4-Bit Internally Synchronous BCD Counter and the 34520 is a Dual 4-Bit Internally Synchronous Binary Counter. Both have the same operation except for the count sequence. Each counter has both an active HIGH Clock Input (CP_0) and an active LOW Clock Input ($\overline{CP}_1$), buffered Outputs from all four bit positions (Q_0–Q_3) and an active HIGH overriding asynchronous Master Reset Input (MR).

The counter advances on either the LOW-to-HIGH transition of the CP_0 Input if $\overline{CP}_1$ is HIGH or the HIGH-to-LOW transition of the $\overline{CP}_1$ Input if CP_0 is LOW (see the Truth Table). Either Clock Input (CP_0, $\overline{CP}_1$) may be used as the Clock Input to the counter and the other Clock Input may be used as a Clock Inhibit Input.

A HIGH on the Master Reset Input (MR) resets the counter (Q_0–Q_3 = LOW) independent of the Clock Inputs (CP_0, $\overline{CP}_1$).

- **TYPICAL COUNT FREQUENCY OF 10 MHz AT V_{DD} = 10 V**
- **TRIGGERED ON EITHER A LOW-TO-HIGH OR A HIGH-TO-LOW TRANSITION**
- **ASYNCHRONOUS ACTIVE HIGH MASTER RESET**
- **BUFFERED OUTPUTS FROM ALL FOUR BIT POSITIONS**
- **FULLY SYNCHRONOUS COUNTING**

PIN NAMES

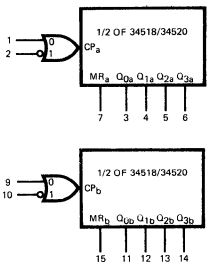
CP_{0a}, CP_{0b}	Clock Input (L → H Triggered)
$\overline{CP}_{1a}$, $\overline{CP}_{1b}$	Clock Input (H → L Triggered)
MR_a, MR_b	Master Reset Inputs
Q_{0a}–Q_{3a}	Outputs
Q_{0b}–Q_{3b}	Outputs

TRUTH TABLE

CP_0	$\overline{CP}_1$	MR	MODE
⎍	H	L	Counter Advances
L	⎎	L	Counter Advances
⎎	X	L	No Change
X	⎍	L	No Change
⎍	L	L	No Change
H	⎎	L	No Change
X	X	H	Reset (Asynchronous)

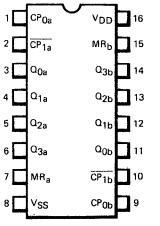
X = Don't Care
L = LOW Level
H = HIGH Level
⎍ = Positive-Going Transition
⎎ = Negative-Going Transition

LOGIC SYMBOLS



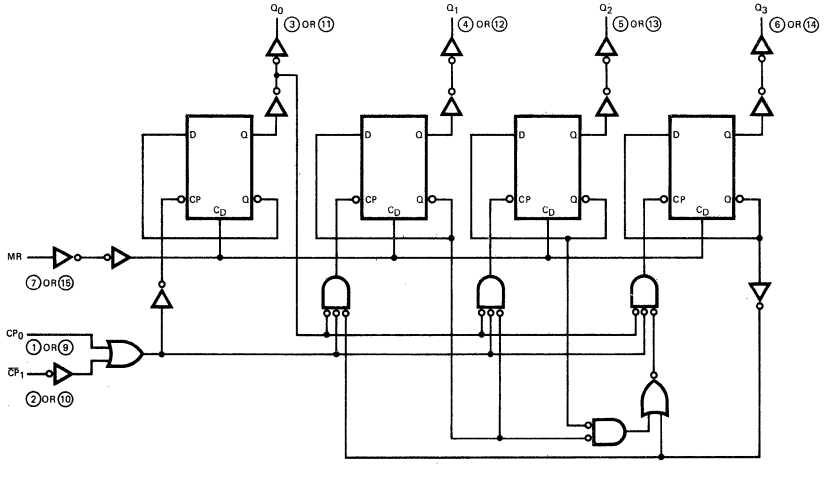
V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



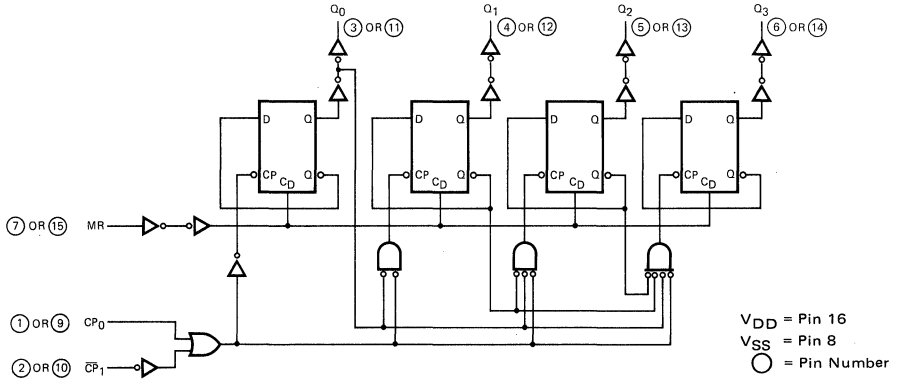
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

1/2 OF A 34518 LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
◯ = Pin Number

1/2 OF A 34520 LOGIC DIAGRAM



DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V

SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEMP	TEST CONDITIONS
I_{DD}	Quiescent Power Supply Current	XC			50			100		20		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					700			1400		280			MAX	
		XM			15			25		5		μA	MIN, 25°C	
					900			1500		300			MAX	

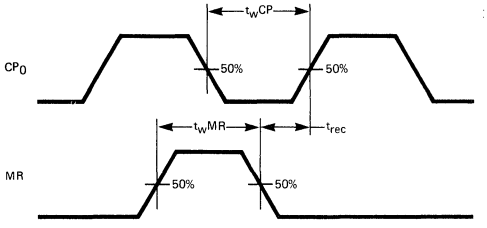
NOTE: Additional DC Characteristics are listed in this section under 34000 Series CMOS Family Characteristics.

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C

SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEST CONDITIONS
t_{PLH}	Propagation Delay, CP_0 or $\overline{CP_1}$ to Q_n		200			85			55		ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
t_{PHL}			200			85			55		ns	
t_{PHL}	Propagation Delay, MR to Q_n		200			80			55		ns	
t_{TLH}	Output Transition Time		35			18			12		ns	
t_{THL}			35			18			12		ns	
t_{PLH}	Propagation Delay, CP_0 or $\overline{CP_1}$ to Q_n		220			95			60		ns	C_L = 50 pF Input Transition Times ⩽ 20 ns
t_{PHL}			220			95			60		ns	
t_{PHL}	Propagation Delay, MR to Q_n		220			90			60		ns	
t_{TLH}	Output Transition Time		65			35			25		ns	
t_{THL}			65			35			25		ns	
t_wMR	MR Minimum Pulse Width		70			30			20		ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
t_wCP	CP_0 or $\overline{CP_1}$ Minimum Pulse Width		120			50			35		ns	
t_{rec}	MR Recovery Time		15			5			0		ns	
t_s	Set-Up Time, CP_0 to $\overline{CP_1}$		130			57			40		ns	
t_s	Set-Up Time, $\overline{CP_1}$ to CP_0		130			57			40		ns	
f_{MAX}	Input Count Frequency (Note 3)		4			10					MHz	

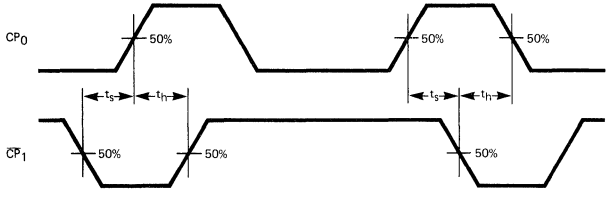
NOTES:
1. Propagation Delays and Output Transition Times are graphically described in this section under 34000 Series CMOS Family Characteristics.
2. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Set-up Times (t_s), Hold Times (t_h), Recovery Times (t_{rec}), and Minimum Pulse Widths (t_w) do not vary with load capacitance.
3. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
4. It is recommended that input rise and fall times to either Clock Input (CP_0 or $\overline{CP_1}$) be less than 15 μs.

SWITCHING WAVEFORMS



Conditions: $\overline{CP_1}$ = HIGH and the device triggers on a LOW-to-HIGH transition at CP_0. The timing also applies when CP_0 = LOW and the device triggers on a HIGH-to-LOW transition at $\overline{CP_1}$.

MINIMUM PULSE WIDTHS FOR CP_0, $\overline{CP_1}$ AND MR AND MR RECOVERY TIME



NOTE:
Set-up and Hold Times are shown as positive values but may be specified as negative values.

SET-UP AND HOLD TIMES, CP_0 TO $\overline{CP_1}$ AND $\overline{CP_1}$ TO CP_0

34539
DUAL 4-INPUT MULTIPLEXER

DESCRIPTION — The 34539 is a Dual 4-Input Digital Multiplexer with common select logic. Each multiplexer has four Multiplexer Inputs (I_0-I_3), an active LOW Enable Input ($\overline{E}$) and a Multiplexer Output (Z). When HIGH, the Enable Input ($\overline{E}$) forces the Multiplexer Output (Z) of the respective multiplexer LOW, independent of the Select (S_0, S_1) and Multiplexer (I_0-I_3) Inputs. With the Enable Input ($\overline{E}$) LOW, the common Select Inputs (S_0, S_1) determine which Multiplexer Input (I_0-I_3) on each of the multiplexers is routed to the respective Multiplexer Output (Z).

- **COMMON SELECT LOGIC**
- **ACTIVE LOW ENABLES**

PIN NAMES

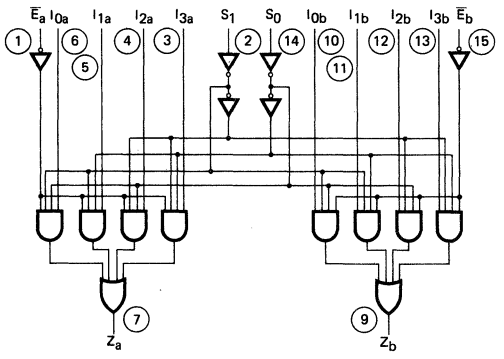
I_{0a}, I_{1a}, I_{2a}, I_{3a}	Multiplexer Inputs
I_{0b}, I_{1b}, I_{2b}, I_{3b}	
S_0, S_1	Select Inputs
$\overline{E}_a$, $\overline{E}_b$	Enable Inputs (Active LOW)
Z_a, Z_b	Multiplexer Outputs

TRUTH TABLE

INPUTS			OUTPUT
S_0	S_1	$\overline{E}$	Z
X	X	H	L
L	L	L	I_0
H	L	L	I_1
L	H	L	I_2
H	H	L	I_3

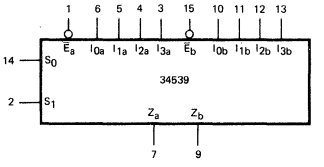
H = HIGH Level
L = LOW Level
X = Don't Care

LOGIC DIAGRAM



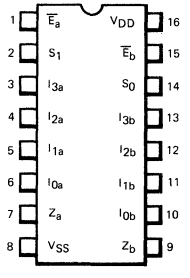
V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Number

LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			30			60		12		µA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					600			1200		240			MAX	
		XM			5			10		2		µA	MIN, 25°C	
					100			200		40			MAX	

NOTE: Additional DC Characteristics are listed in this section under 34000 Series CMOS Family Characteristics.

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, I_X to Z		145			61			43		ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
t_{PHL}			120			50			33		ns	
t_{PLH}	Propagation Delay, Select to Z		190			78			55		ns	
t_{PHL}			192			78			55		ns	
t_{PLH}	Propagation Delay, $\overline{E}$ to Z		100			42			29		ns	
t_{PHL}			96			42			32		ns	
t_{TLH}	Output Transition Time		38			19			12		ns	
t_{THL}			31			15			12		ns	
t_{PLH}	Propagation Delay, I_X to Z		166			71			51		ns	C_L = 50 pF Input Transition Times ⩽ 20 ns
t_{PHL}			140			58			40		ns	
t_{PLH}	Propagation Delay, Select to Z		210			88			62		ns	
t_{PHL}			210			88			62		ns	
t_{PLH}	Propagation Delay, $\overline{E}$ to Z		120			53			37		ns	
t_{PHL}			118			51			38		ns	
t_{TLH}	Output Transition Time		76			39			29		ns	
t_{THL}			66			30			22		ns	

NOTE:
Propagation Delays and Output Transition Times are graphically described in this section under 34000 Series CMOS Family Characteristics.

34555 • 34556

DUAL 1-OF-4 DECODERS/DEMULTIPLEXERS

DESCRIPTION — The 34555 and 34556 are Dual 1-of-4 Decoders/Demultiplexers. Each decoder/demultiplexer has two Address Inputs (A_0, A_1), an active LOW Enable Input ($\overline{E}$) and four mutually exclusive Outputs which are active HIGH for the 34555 (O_0-O_3) and active LOW for the 34556 ($\overline{O}_0$-$\overline{O}_3$).

When the 34555 is used as a decoder, the Enable Input ($\overline{E}$) when HIGH, forces all Outputs (O_0-O_3) LOW. When used as a demultiplexer, the appropriate Output is selected by the data on the Address Inputs (A_0, A_1) and follows as the inverse of the Enable Input ($\overline{E}$). All unselected Outputs are LOW.

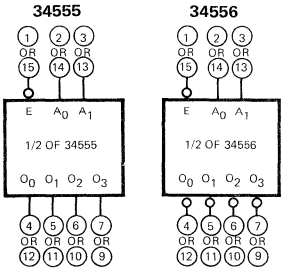
When the 34556 is used as a decoder, the Enable Input ($\overline{E}$) when HIGH forces all Outputs ($\overline{O}_0$-$\overline{O}_3$) HIGH. When used as a demultiplexer, the appropriate Output is selected by the data on the Address Inputs (A_0, A_1) and follows the state of the Enable Input ($\overline{E}$). All unselected Outputs are HIGH.

- **ACTIVE HIGH OUTPUTS FOR THE 34555 AND ACTIVE LOW OUTPUTS FOR THE 34556**
- **OVERRIDING ACTIVE LOW ENABLE**

PIN NAMES

$\overline{E}$	Enable Input (Active LOW)
A_0, A_1	Address Inputs
O_0-O_3	Outputs (Active HIGH — 34555 Only)
$\overline{O}_0$-$\overline{O}_3$	Outputs (Active LOW — 34556 Only)

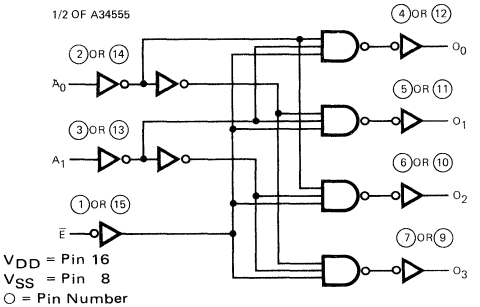
LOGIC SYMBOLS



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Number

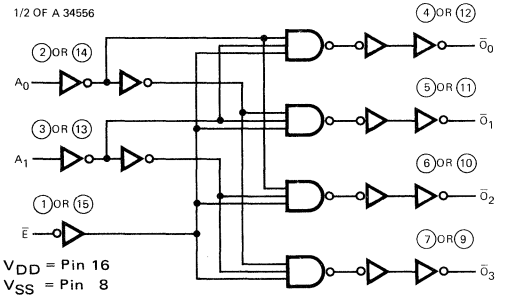
LOGIC DIAGRAMS

1/2 OF A 34555



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Number

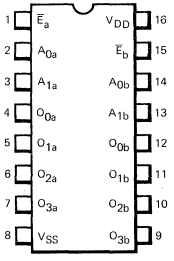
1/2 OF A 34556



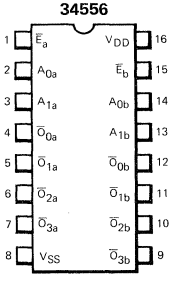
V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Number

CONNECTION DIAGRAMS
DIP (TOP VIEW)

34555



34556



Note: The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

34555 TRUTH TABLE

$\overline{E}$	A_0	A_1	O_1	O_2	O_3	O_4
L	L	L	H	L	L	L
L	H	L	L	H	L	L
L	L	H	L	L	H	L
L	H	H	L	L	L	H
H	X	X	L	L	L	L

H = HIGH Level
L = LOW Level
X = Don't Care

34556 TRUTH TABLE

$\overline{E}$	A_0	A_1	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L
H	X	X	H	H	H	H

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V

SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEMP	TEST CONDITIONS
I_{DD}	Quiescent Power Supply Current	XC			20			40		8		µA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					200			400		80			MAX	
		XM			2			4		0.8		µA	MIN, 25°C	
					100			200		40			MAX	

Note: Additional DC Characteristics are listed in this section under 34000 Series CMOS Family Characteristics.

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C, 34555 only

SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEST CONDITIONS
t_{PLH}	Propagation Delay, Address to Output		130			54			33		ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
t_{PHL}			105			45			40		ns	
t_{PLH}	Propagation Delay, $\overline{E}$ to Output		130			51			32		ns	
t_{PHL}			105			45			32		ns	
t_{TLH}	Output Transition Time		35			15			12		ns	
t_{THL}			33			13			10		ns	
t_{PLH}	Propagation Delay, Address to Output		148			60			40		ns	C_L = 50 pF Input Transition Times ⩽ 20 ns
t_{PHL}			127			54			45		ns	
t_{PLH}	Propagation Delay, $\overline{E}$ to Output		148			60			40		ns	
t_{PHL}			127			53			40		ns	
t_{TLH}	Output Transition Time		65			20			25		ns	
t_{THL}			66			25			20		ns	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C, 34556 only

SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEST CONDITIONS
t_{PLH}	Propagation Delay, Address to Output		120			48			33		ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
t_{PHL}			160			58			40		ns	
t_{PLH}	Propagation Delay, $\overline{E}$ to Output		114			45			32			
t_{PHL}			125			50			32		ns	
t_{TLH}	Output Transition Time		37			18			12		ns	
t_{THL}			35			15			10		ns	
t_{PLH}	Propagation Delay, Address to Output		140			57			40		ns	C_L = 50 pF Input Transition Times ⩽ 20 ns
t_{PHL}			185			68			45		ns	
t_{PLH}	Propagation Delay, $\overline{E}$ to Output		134			55			40		ns	
t_{PHL}			145			58			40		ns	
t_{TLH}	Output Transition Time		75			37			25		ns	
t_{THL}			77			29			20		ns	

NOTE:
1. Propagation Delays and Output Transition Times are graphically described in this section under 34000 Series CMOS Family Characteristics.

34702
PROGRAMMABLE BIT RATE GENERATOR
FAIRCHILD CMOS LSI

DESCRIPTION – The 34702 Bit Rate Generator provides the necessary clock signals for digital data transmission systems, such as Universal Asynchronous Receiver and Transmitter circuits (UARTs). It generates any of the 13 commonly used bit rates using an on-chip crystal oscillator, but it's design also provides for easy and economical multichannel operation, where any of the possible frequencies must be made available on any output channel.

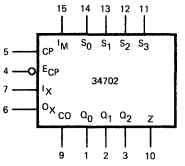
One 34702 can control up to eight output channels. When more than one bit rate generator is required, they can still be operated from one crystal.

- **PROVIDES ALL 13 COMMONLY USED BIT RATES**
- **ONE 34702 CONTROLS UP TO EIGHT TRANSMISSION CHANNELS**
- **USES 2.4576 MHz INPUT FOR STANDARD FREQUENCY OUTPUTS (16 TIMES BIT RATE)**
- **CONFORMS TO EIA RS-404**
- **ON-CHIP INPUT PULL UP CIRCUITS**
- **TTL COMPATIBLE–OUTPUTS WILL DRIVE 1.6 mA**
- **INITIALIZATION CIRCUIT FACILITATES DIAGNOSTIC FAULT ISOLATION**
- **LOW POWER DISSIPATION–1.35 mA POWER DISSIPATION AT 5 V AND 2.4576 MHz**
- **16-PIN DUAL IN-LINE PACKAGE**

PIN NAMES

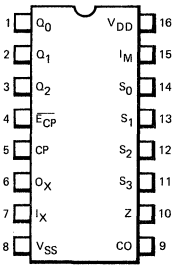
CP	External Clock Input
$\overline{E_{CP}}$	External Clock Enable Input (Active LOW)
I_X	Crystal Input
I_M	Multiplexed Input
S_0-S_3	Rate Select Inputs
C_O	Clock Output
O_X	Crystal Drive Output
Q_0-Q_2	Scan Counter Outputs
Z	Bit Rate Output

LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

BLOCK DIAGRAM

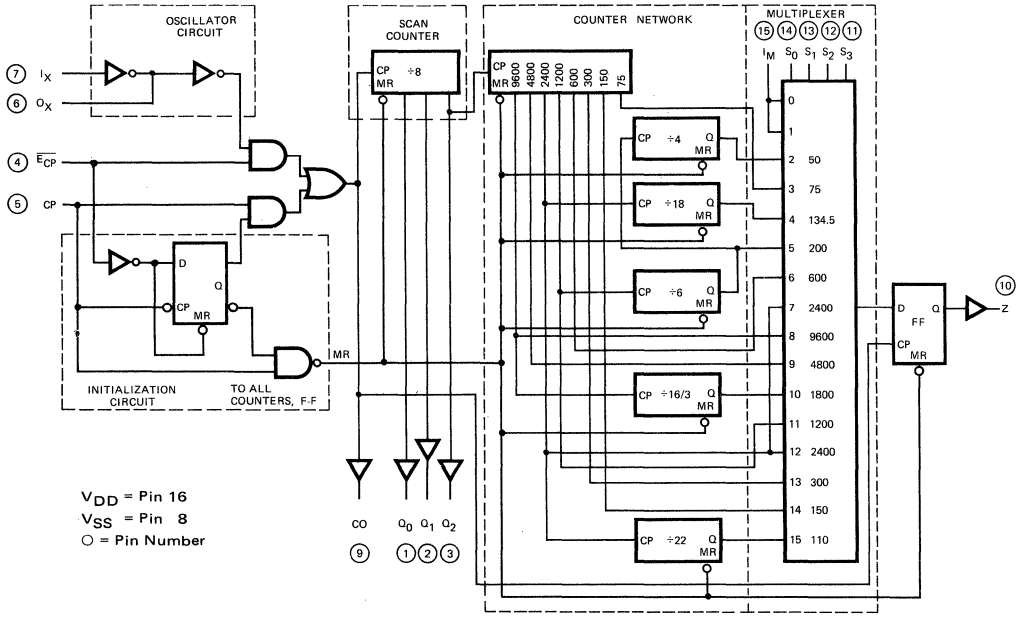


TABLE 1
CLOCK MODES AND INITIALIZATION

I_X	$\overline{E_{CP}}$	CP	OPERATION
⎍⎍⎍	H	L	Clocked from I_X
X	L	⎍⎍⎍	Clocked from CP
X	H	H	Continuous Reset
X	L	⎍⎺⎍	Reset During First CP = HIGH Time

H = HIGH Level
L = LOW Level
X = Don't Care
⎍⎺⎍ = 1st HIGH Level Clock Pulse After $\overline{E_{CP}}$ Goes LOW
⎍⎍⎍ = Clock Pulses

TABLE 2
TRUTH TABLE FOR RATE SELECT INPUTS

S_3	S_2	S_1	S_0	Output Rate (Z) Note 1
L	L	L	L	Multiplexed Input (I_M)
L	L	L	H	Multiplexed Input (I_M)
L	L	H	L	50 Baud
L	L	H	H	75 Baud
L	H	L	L	134.5 Baud
L	H	L	H	200 Baud
L	H	H	L	600 Baud
L	H	H	H	2400 Baud
H	L	L	L	9600 Baud
H	L	L	H	4800 Baud
H	L	H	L	1800 Baud
H	L	H	H	1200 Baud
H	H	L	L	2400 Baud
H	H	L	H	300 Baud
H	H	H	L	150 Baud
H	H	H	H	110 Baud

Note 1.
Actual output frequency is 16 times the indicated Output Rate, assuming a clock frequency of 2.4576 MHz.

FUNCTIONAL DESCRIPTION – Digital data transmission systems employ a wide range of standardized bit rates, ranging from 50 baud interfacing with electromechanical devices, to 9600 baud for high speed modems. Modern electronic systems commonly use Universal Asynchronous Receiver and Transmitter circuits (UARTs) to convert parallel data inputs into a serial bit stream (transmitter) and to reconvert the serial bit stream into parallel outputs (receiver). In order to resynchronize the incoming serial data, the receiver requires a clock rate that is a multiple of the incoming bit rate. Popular MOS-LSI UART circuits use a clock that is 16 times the transmitted bit rate. The 34702 can generate 13 standardized clock rates from one common high frequency input.

The 34702 contains the following five functional subsystems which are discussed in detail below:

1. An Oscillator Circuit with associated gating.
2. A Prescaler used as scan counter for multichannel operation (described in the applications section).
3. A network of Counter Chains to generate the required standardized frequencies.
4. An Output Multiplexer (frequency selector) with resynchronizing output flip-flop.
5. An Initializing (reset) Circuit.

OSCILLATOR

For conventional operation generating 16 output clock pulses per bit period, the input clock frequency must be 2.4576 MHz (i.e. 9600 baud x 16 x 16, since the scan counter and the first flip-flop of the counter chain act as an internal ÷ 16 prescaler). A lower input frequency will obviously result in a proportionally lower output frequency.

The 34702 can be driven from two alternate clock sources: (1) When the $\overline{E_{CP}}$ (active LOW External Clock Enable) input is LOW, the CP input is the clock source. (2) When the $\overline{E_{CP}}$ input is HIGH, a crystal connected between I_X and O_X, or a signal applied to the I_X input is the clock source.

PRESCALER (SCAN COUNTER)

The clock frequency is made available on the CO (Clock Output) pin and is applied to the ÷ 8 prescaler with buffered Outputs Q_0, Q_1, and Q_2. This prescaler is of no particular advantage in single frequency applications, but it is essential for the simple and economical multichannel scheme described in the Applications section of this data sheet.

COUNTER NETWORK

The prescaler Output Q_2 is a square wave of 1/8 the input frequency and is used to drive the frequency counter network generating the 13 standardized frequencies. Note that the frequencies are labeled in the Block Diagram and described here in terms of the transmission bit rate. In a conventional system using a 2.4576 MHz clock input, the actual output frequencies are 16 times higher.

The output from the first frequency divider flip-flop is thus labeled 9600, since it is used to transmit or receive 9600 baud (bits per second). The actual frequency at this node is 16 x 9.6 kHz = 153.6 kHz. Seven more cascaded binaries generate the appropriate frequencies for bit rates 4800, 2400, 1200, 600, 300, 150, and 75.

The other five bit rates are generated by individual counters:

bit rate 1200 is divided by 6 to generate bit rate 200,
bit rate 200 is divided by 4 to generate bit rate 50,
bit rate 2400 is divided by 18 to generate bit rate 134.5 with a frequency error of −0.87%,
bit rate 2400 is also divided by 22 to generate bit rate 110 with a frequency error of −0.83%, and
bit rate 9600 is divided by 16/3 to generate bit rate 1800.

The 16/3 division is accomplished by alternating the divide ratio between 5 (twice) and 6 (once). The result is an exact average output frequency with some frequency modulation. Taking advantage of the ÷ 16 feature of the UART, the resulting distortion is less than 0.78%, irrespective of the number of elements in a character, and therefore well within the timing accuracy specified for high speed communications equipment. All signals except 1800, have a 50% duty cycle.

OUTPUT MULTIPLEXER

The outputs of the counter network are fed to a 16-input multiplexer, which is controlled by the Rate Select Inputs (S_0-S_3). The multiplexer output is then resynchronized with the incoming clock in order to cancel all cumulative delays and to present an output signal at the buffered Output (Z) that is synchronous with the prescaler Outputs (Q_0-Q_2). Table 2 lists the correspondence between select code and output bit rate. Two of the 16 codes do not select an internally generated frequency, but select an input into which the user can feed either a different, non-standardized frequency, or a static level (HIGH or LOW) to generate "zero baud".

The bit rates most commonly used in modern data terminals (110, 150, 300, 1200, 2400 baud) require that not more than one input be grounded, easily achieved with a single pole, 5-position switch. 2400 baud is selected by two different codes, so that the whole spectrum of modern digital communication rates has a common HIGH on the S_3 input.

INITIALIZATION (RESET)

The initialization circuit generates a common master reset signal for all flip-flops in the 34702. This signal is derived from a digital differentiator that senses the first HIGH level on the CP input after the $\overline{E_{CP}}$ input goes LOW. When $\overline{E_{CP}}$ is HIGH, selecting the Crystal Input, CP must be LOW. A HIGH level on CP would apply a continuous reset.

All inputs to the 34702, except I_X have on-chip pull up circuits which improve TTL compatibility and eliminate the need to tie a permanently HIGH input to V_{DD}.

DC CHARACTERISTICS: V_{DD} = 5 V, V_{SS} = 0 V

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEMP	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		3.5			V	All	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage				1.5	V	All	Guaranteed Input LOW Voltage
V_{OH}	Output HIGH Voltage		4.99 4.95 4.0			V	MIN, 25°C MAX All	I_{OH} = 0 mA, Inputs at 0 or 5 V per the Logic Function or Truth Table I_{OH} = 0 mA, Inputs at 1.5 or 3.5 V
V_{OL}	Output LOW Voltage				0.01 0.05 0.5	V	MIN, 25°C MAX All	I_{OL} = 0 mA, Inputs at 0 or 5 V per the Logic Function or Truth Table I_{OL} = 0 mA, Inputs at 1.5 or 3.5 V
I_{IL}*	Input LOW Current for Input I_X	XC XM			−0.1 −0.01	µA	25°C	Lead Under Test at 0 V All Other Inputs Simultaneously at 5 V
	Input LOW Current for all Other Inputs	XC XM		−30 −30				
I_{IH}	Input HIGH Current for Input I_X	XC XM			0.1 0.01	µA	25°C	Lead Under Test at 5 V All Other Inputs Simultaneously at 0 V
	Input HIGH Current for all Other Inputs	XC XM			0.1 0.01			
I_{OH}	Output HIGH Current		-1.5 -1.0	-3.0 -2.0		mA	MIN, 25°C MAX	V_{OUT} = 2.5 V Inputs at 0 or 5 V per the Logic Function or Truth Table
			-0.7 -0.4	-1.4 -0.8		mA	MIN, 25°C MAX	V_{OUT} = 4.5 V
I_{OL}	Output LOW Current		3.5 3.5 1.6	5.5 5.5 3.2		mA	MIN 25°C MAX	V_{OUT} = 0.4 V
I_{DDL}*	Quiescent Power Supply Current, LOW	XC		200 400		µA	MIN, 25°C MAX	All Inputs at 0 V
		XM		200 400		µA	MIN, 25°C MAX	
I_{DDH}	Quiescent Power Supply Current, HIGH	XC		10 60		µA	MIN, 25°C MAX	All Inputs at 5 V
		XM		5 30		µA	MIN, 25°C MAX	

*Input Current and Quiescent Power Supply Current are relatively higher for this device because of active pull up circuits on all inputs except I_X. This is done for TTL compatibility.

DC CHARACTERISTICS: V_{DD} = 15 V, V_{SS} = 0 V

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEMP	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		10.5			V	All	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage				4.5	V	All	Guaranteed Input LOW Voltage
V_{OH}	Output HIGH Voltage		14.99 14.95 13.0			V	MIN, 25°C MAX All	I_{OH} = 0 mA, Inputs at 0 or 15 V per the Logic Function or Truth Table I_{OH} = 0 mA, Inputs at 4.5 or 10.5 V
V_{OL}	Output LOW Voltage				0.01 0.05 2.0	V	MIN, 25°C MAX All	I_{OL} = 0 mA, Inputs at 0 or 15 V per the Logic Function or Truth Table I_{OL} = 0 mA, Inputs at 4.5 or 10.5 V
I_{IL}*	Input LOW Current for Input I_X	XC XM			−0.2 −0.02	µA	25°C	Lead Under Test at 0 V All Other Inputs Simultaneously at 15 V
	Input LOW Current for all Other Inputs	XC XM		−100 −100				
I_{IH}	Input HIGH Current for Input I_X	XC XM			0.2 0.02	µA	25°C	Lead Under Test at 15 V All Other Inputs Simultaneously at 0 V
	Input HIGH Current for all Other Inputs	XC XM			0.2 0.02			
I_{OH}	Output HIGH Current		−2.2 −1.4	−4.4 −2.8		mA	MIN, 25°C MAX	V_{OUT} = 14.5 V Inputs at 0 or 15 V per the Logic Function or Truth Table V_{OUT} = 0.5 V
I_{OL}	Output LOW Current			18.0 18.0 10.0		mA	MIN 25°C MAX	
I_{DDL}*	Quiescent Power Supply Current, LOW	XC		500 1000		µA	MIN, 25°C MAX	All Inputs at 0 V
		XM		500 1000		µA	MIN, 25°C MAX	
I_{DDH}	Quiescent Power Supply Current, HIGH	XC		40 240		µA	MIN, 25°C MAX	All Inputs at 15 V
		XM		40 120		µA	MIN, 25°C MAX	

*Input Current and Quiescent Power Supply Current are relatively higher for this device because of active pull up circuits on all inputs except I_X. This is done for TTL compatibility.

DC CHARACTERISTICS: V_{DD} = 10 V, V_{SS} = 0 V

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEMP	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		7.0			V	All	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage				3.0	V	All	Guaranteed Input LOW Voltage
V_{OH}	Output HIGH Voltage		9.99 9.95 9.0			V	MIN, 25°C MAX All	I_{OH} = 0 mA, Inputs at 0 or 10 V per the Logic Function or Truth Table I_{OH} = 0 mA, Inputs at 3 or 7 V
V_{OL}	Output LOW Voltage				0.01 0.05 1.0	V	MIN, 25°C MAX All	I_{OL} = 0 mA, Inputs at 0 or 10 V per the Logic Function or Truth Table I_{OL} = 0 mA, Inputs at 3 or 7 V
I_{IL}*	Input LOW Current for Input I_X	XC XM			−0.1 −0.01	µA	25°C	Lead Under Test at 0 V All Other Inputs Simultaneously at 10 V
	Input LOW Current for all Other Inputs	XC XM		−60 −60				
I_{IH}	Input HIGH Current for Input I_X	XC XM			0.1 0.01	µA	25°C	Lead Under Test at 10 V All Other Inputs Simultaneously at 0 V
	Input HIGH Current for all Other Inputs	XC XM			0.1 0.01			
I_{OH}	Output HIGH Current		−1.4 −0.8	−2.8 −1.6		mA	MIN, 25°C MAX	V_{OUT} = 9.5 V Inputs at 0 or 10 V per V_{OUT} = 0.5 V the Logic Function or Truth Table
I_{OL}	Output LOW Current		10.0	14.0 14.0 7.0		mA	MIN 25°C MAX	
I_{DDL}*	Quiescent Power Supply Current, LOW	XC		400 800		µA	MIN, 25°C MAX	All Inputs at 0 V
		XM		400 800		µA	MIN, 25°C MAX	
I_{DDH}	Quiescent Power Supply Current, HIGH	XC		20 120		µA	MIN, 25°C MAX	All Inputs at 10 V
		XM		10 60		µA	MIN, 25°C MAX	

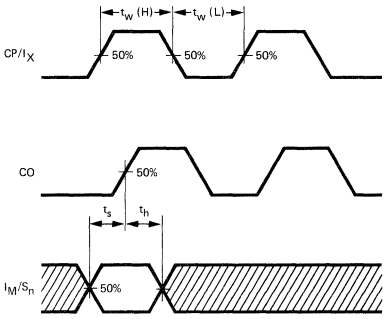
*Input Current and Quiescent Power Supply Current are relativély higher for this device because of active pull up circuits on all inputs except I_X. This is done for TTL compatibility.

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, I_X to CO		105 105			55 55			35 35		ns ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
t_{PLH} t_{PHL}	Propagation Delay, CP to CO		80 80			40 40			30 30		ns ns	
t_{PLH} t_{PHL}	Propagation Delay, CO to Q_n		40 40			20 20			15 15		ns ns	
t_{PLH} t_{PHL}	Propagation Delay, CO TO Z		50 50			25 25			20 20		ns	
t_{TLH} t_{THL}	Output Transition Time		50 35			25 20			15 10		ns ns	
t_{PLH} t_{PHL}	Propagation Delay, I_X to CO		150 150			75 75			55 55		ns ns	C_L = 50 pF Input Transition Times ⩽ 20 ns
t_{PLH} t_{PHL}	Propagation Delay, CP to CO		100 100			50 50			35 35		ns ns	
t_{PLH} t_{PHL}	Propagation Delay, CO to Q_n		60 60			30 30			25 25		ns ns	
t_{PLH} t_{PHL}	Propagation Delay, CO TO Z		70 70			35 35			25 25		ns ns	
t_{TLH} t_{THL}	Output Transition Time		70 40			35 25			25 15		ns ns	
t_s t_h	Set-Up Time, Select to CO Hold Time, Select to CO		150 -10			100 -7			75 -5		ns ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
t_s t_h	Set-Up Time, I_M to CO Hold Time, I_M to CO		150 -10			70 -7			50 -5		ns ns	
$t_wCP(L)$ $t_wCP(H)$	Minimum Clock Pulse Width, LOW and HIGH		150 150			75 75			50 50		ns ns	
$t_wI_X(L)$ $t_wI_X(H)$	Minimum I_X Pulse Width, LOW and HIGH		150 150			75 75			50 50		ns ns	

NOTES:
1. Propagation Delays and Output Transition Times are graphically described in this section under 34000 Series CMOS Family Characteristics.
2. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Set-up Times (t_s), Hold Times (t_h), and Minimum Pulse Widths (t_w) do not vary with load capacitance.
3. The first HIGH Level Clock Pulse after E_{CP} goes LOW must be at least 350 ns long to guarantee reset of all Counters.
4. It is recommended that input rise and fall times to the Clock Inputs (CP, I_X) be less than 15 μs.

SWITCHING WAVEFORMS



MINIMUM CP AND I_X PULSE WIDTHS AND SET-UP AND HOLD TIMES, SELECT INPUT (S_n) TO CLOCK OUTPUT (CO) AND I_M INPUT TO CLOCK OUTPUT (CO)

Note: Set-up and Hold Times are shown as positive values but may be specified as negative values.

APPLICATION

SINGLE CHANNEL BIT RATE GENERATOR

Figure 1 shows the simplest application of the 34702. This circuit generates one of five possible bit rates as determined by the setting of a single pole, 5-position switch. The Bit Rate Output (Z) drives one standard TTL load or four low power Schottky loads over the full temperature range. The possible output frequencies correspond to 110, 150, 300, 1200, and 2400 Baud. For many low cost terminals these five bit rates are adequate.

SIMULTANEOUS GENERATION OF SEVERAL BIT RATES

Fixed Programmed Multichannel Operation

Figure 2 shows a simple scheme that generates eight bit rates on eight output lines, using one 34702 and one 93L34 8-Bit Addressable Latch. This and the following applications take advantage of the built-in scan counter (prescaler) outputs. As shown in the block diagram, these outputs (Q_0 to Q_2) go through a complete sequence of eight states for every half-period of the highest output frequency (9600 Baud). Feeding these Scan Counter Outputs back to the Select Inputs of the multiplexer causes the 34702 to interrogate sequentially the state of eight different frequency signals. The 93L34 8-Bit Addressable Latch, addressed by the same Scan Counter Outputs, reconverts the multiplexed single Output (Z) of the 34702 into eight parallel output frequency signals. In the simple scheme of Figure 2, input S_3 is left open (HIGH) and the following bit rates are generated:

Q_0: 110 Baud, Q_1: 9600 Baud, Q_2: 4800 Baud, Q_3: 1800 Baud,
Q_4: 1200 Baud, Q_5: 2400 Baud, Q_6: 300 Baud, Q_7: 150 Baud.

Other bit rate combinations can be generated by changing the Scan Counter to Selector interconnection or by inserting logic gates into this path.

Fully Programmable Multichannel Operation

Figure 3 shows a fully programmable 8-channel bit rate generator system that, under computer control, generates arbitrarily assigned bit rates on all eight outputs simultaneously. The basic operation is similar to the previously described fixed programmed system, but two 9LS170 4 x 4 Register File MSI packages are connected as programmable look-up tables between the Scan Counter Outputs (Q_0 to Q_2) and the multiplexer Select Inputs (S_0 to S_3). The content of this 8-word by 4-bit memory determines which frequency appears at what output.

19200 Baud Operation

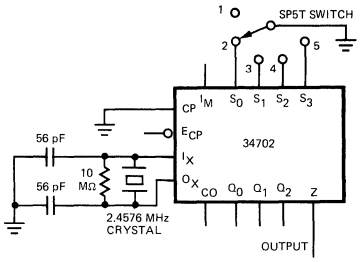
Though a 19200 Baud signal is not internally routed to the multiplexer, the 34702 can be used to generate this bit rate by connecting the Q_2 output to the I_M input and applying select code 0 or 1. An additional 2-input NAND gate can be used to retain the "Zero Baud" feature on select code 0. Any multichannel operation that involves 19200 Baud must be limited to four outputs as shown in Figure 4. Only the two least significant Scan Counter Outputs are used, so that the scan is completed within one half period of the 19200 output frequency.

CLOCK EXPANSION

One 34702 can control up to eight output channels. For more than eight channels, additional Bit Rate Generators are required. These Bit Rate Generators can all be run from the same crystal or clock input. Figure 5 shows one possible expansion scheme. One 34702 is provided with a crystal. All other devices derive their clock from this master. Figure 6 shows a different scheme where the master clock output feeds into the I_X input of all slaves and all $\overline{E_{CP}}$ inputs are normally held HIGH. This scheme retains the reset feature and the selection between two different clock sources of the basic 34702 circuit.

During normal operation, the common $\overline{E_{CP}}$ line is HIGH and the common clock line (CP) is LOW. For diagnostic purposes the common $\overline{E_{CP}}$ is forced LOW. This deselects the crystal frequency and initiates the diagnostic mode. When CP goes HIGH for the first time, all 34702s are reset through their individual on-chip initialization circuitry. Subsequent LOW-to-HIGH clock transitions on the common CP line advance the scan counter, causing all 34702s to operate synchronously.

TYPICAL APPLICATIONS (Cont'd)



SWITCH POSITION	BIT RATE
1	110 Baud
2	150 Baud
3	300 Baud
4	1200 Baud
5	2400 Baud

Fig. 1 SWITCH SELECTABLE BIT RATE GENERATOR CONFIGURATION PROVIDING FIVE BIT RATES

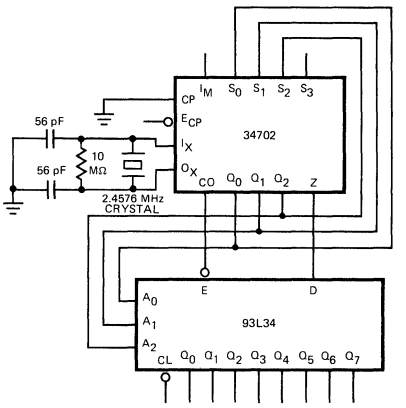


Fig. 2 BIT RATE GENERATOR CONFIGURATION WITH EIGHT SIMULTANEOUS FREQUENCIES

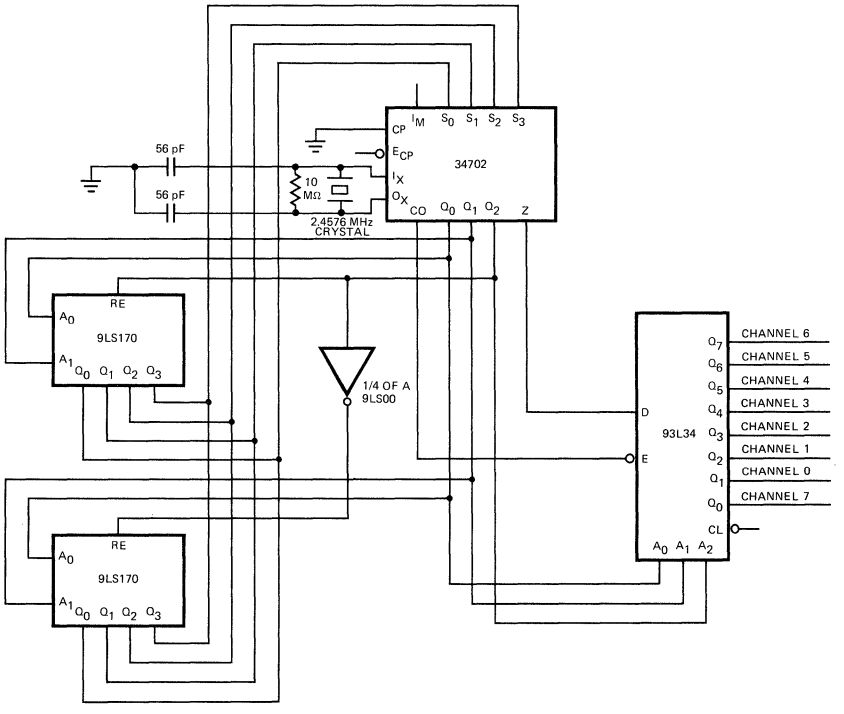


Fig. 3 A FULLY PROGRAMMABLE 8-CHANNEL BIT RATE GENERATOR SYSTEM

TYPICAL APPLICATIONS

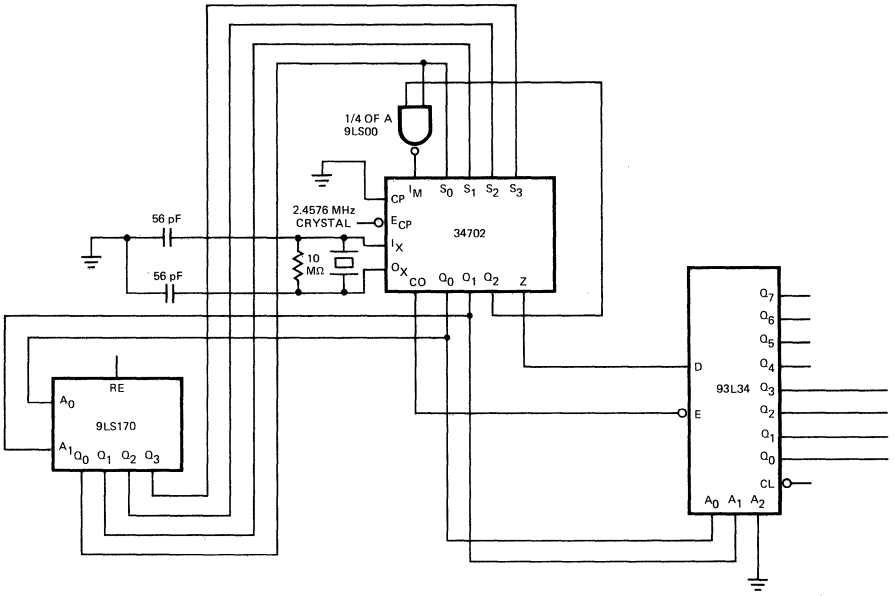


Fig. 4 FULLY PROGRAMMABLE 4-CHANNEL BIT RATE GENERATOR SYSTEM WITH THE 19.2 k BAUD FEATURE.

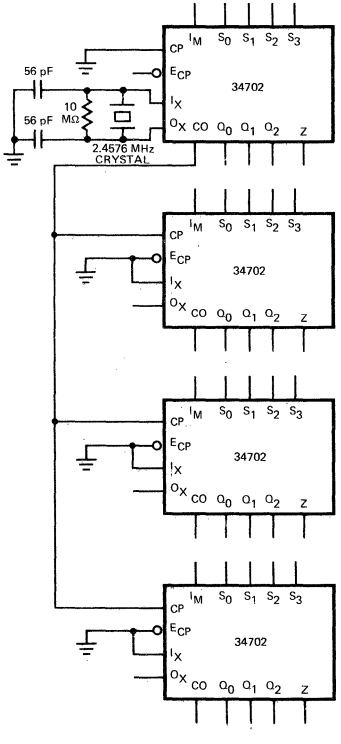


Fig. 5 CASCADE CLOCK EXPANSION SCHEME

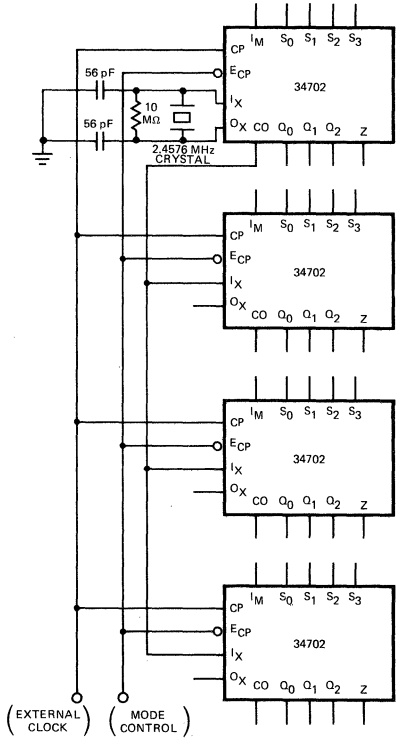


Fig. 6 TANDEM CLOCK EXPANSION SCHEME

CRYSTAL SPECIFICATION RECOMMENDATIONS – Table 3 is a convenient listing of recommended crystal specifications. Crystal manufacturers are also listed below.

TABLE 3 CRYSTAL SPECIFICATIONS

PARAMETERS	COMMERCIAL CRYSTAL SPEC
Frequency	2.4576 MHz "AT" Cut
Series Resistance (Max)	250 Ω
Unwanted Modes	–6.0 dB (Min)
Type of Operation	Parallel
Load Capacitance	32 pF ±0.5

CRYSTAL MANUFACTURERS

CTS Knights, Inc.
Sandwich, Ill. 60548
(815) 786-8411

X - Tron Electronics
1869 National Ave.
Hayward, Calif.
(415) 783-2145

Erie Frequency Control
499 Lincoln St.
Carlisle, Pa. 17013
(717) 249-2232

International Crystal Mfg. Company
10 No. Lee
Oklahoma City, Okla. 73102
(405) 236-3741

34720

256-BIT RANDOM ACCESS MEMORY WITH 3-STATE OUTPUTS

FAIRCHILD CMOS • LSI

DESCRIPTION — The 34720 is a 256-Bit Random Access Memory with 3-State Outputs. It has a Data Input (D), eight Address Inputs (A_0-A_7), an active HIGH Write Enable Input (WE), an active LOW Chip Select Input ($\overline{CS}$), an active HIGH 3-State Output (Q) and an active LOW 3-State Output ($\overline{Q}$). Information on the Data Input (D) is written into the memory location selected by the Address Inputs (A_0-A_7) when the Chip Select Input ($\overline{CS}$) is LOW and the Write Enable Input (WE) is HIGH. Under these conditions, the device is transparent, i.e. the data input is reflected at the True and Complementary Outputs (Q, $\overline{Q}$). Information is read from the memory location selected by the Address Inputs (A_0-A_7) while the Chip Select ($\overline{CS}$) and the Write Enable (WE) Inputs are LOW. The Q Output is the information written into the memory, $\overline{Q}$ is its complement. When the Chip Select Input ($\overline{CS}$) is HIGH, both Outputs (Q, $\overline{Q}$) are held in the high impedance OFF state. This allows other 3-State outputs to be wired together in a bus arrangement. The 34720 offers fully static operation.

- 3-STATE OUTPUTS
- ORGANIZATION – 256 WORDS X 1-BIT
- ON-CHIP DECODING
- TRUE AND COMPLEMENT OUTPUTS AVAILABLE
- FULLY STATIC
- LOW POWER DISSIPATION
- HIGH SPEED

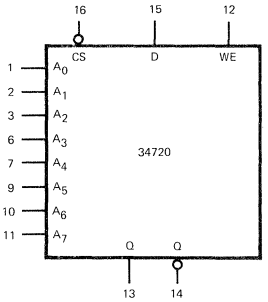
PIN NAMES

$\overline{CS}$	Chip Select Input (Active LOW)
WE	Write Enable Input
D	Data Input
A_0-A_7	Address Inputs
Q	3-State Output (Active HIGH)
$\overline{Q}$	3-State Output (Active LOW)

MODE SELECTION

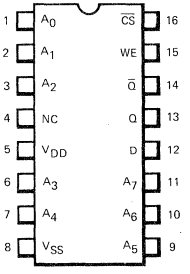
$\overline{CS}$	WE	Q	$\overline{Q}$	MODE
L	H	Data Written Into Memory	Complement of Data Written Into Memory	Write
L	L	Data Written Into Memory	Complement of Data Written Into Memory	Read
H	X	High Impedance	High Impedance	Inhibit

LOGIC SYMBOL



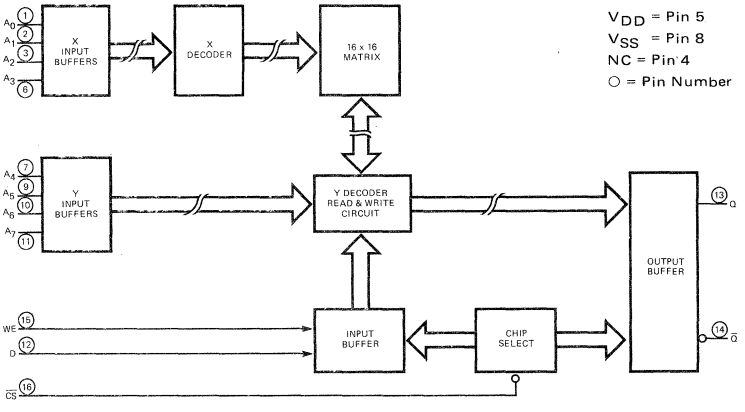
V_{DD} = Pin 5
V_{SS} = Pin 8
NC = Pin 4

CONNECTION DIAGRAM
DIP (TOP VIEW)



Note: The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

BLOCK DIAGRAM



DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V

SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEMP	TEST CONDITIONS
I_{OZH}	Output OFF Current, HIGH			0.05 3.0			0.1 6.0			0.2 12		µA	MIN, 25°C MAX	Output Returned to V_{DD}, $\overline{CS}$ = V_{DD}
I_{OZL}	Output OFF Current, LOW			-0.05 -3.0			-0.1 -6.0			-0.2 -12		µA	MIN, 25°C MAX	Output Returned to V_{SS}, $\overline{CS}$ = V_{DD}
I_{DD}	Quiescent Power Supply Current	XC		0.5 30			2 60			4 120		µA	MIN, 25°C MAX	All inputs common and at 0 V or V_{DD}
		XM		0.5 30			2 60			4 120		µA	MIN, 25°C MAX	

Note: Additional DC Characteristics are listed in this section under 34000 Series CMOS Family Characteristics.

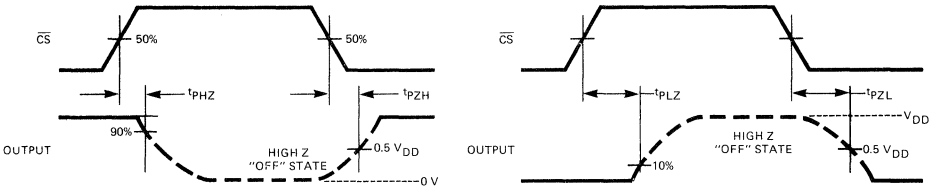
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C

SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEST CONDITIONS
	READ MODE											C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Address to Output		200 200			100 100			75 75		ns ns	Input Transition Times ⩽ 20 ns
t_{PZH} t_{PZL}	Enable Time, $\overline{CS}$ to Output		125 125			60 60			40 40		ns ns	R_L = 1 kΩ to V_{SS} R_L = 1 kΩ to V_{DD}
t_{PHZ} t_{PLZ}	Disable Time, $\overline{CS}$ to Output		125 125			60 60			40 40		ns ns	R_L = 1 kΩ to V_{SS} R_L = 1 kΩ to V_{DD}
t_{TLH} t_{THL}	Output Transition Time		40 40			20 20			15 15		ns ns	
	WRITE MODE											
t_{PLH} t_{PHL}	Propagation Delay, WE to Output		125 125			60 60			40 40		ns ns	
	READ MODE											C_L = 50 pF
t_{PLH} t_{PHL}	Propagation Delay, Address to Output		250 250			125 125			100 100		ns ns	Input Transition Times ⩽ 20 ns
t_{PZH} t_{PZL}	Enable Time, $\overline{CS}$ to Output		150 150			70 70			50 50		ns ns	R_L = 1 kΩ to V_{SS} R_L = 1 kΩ to V_{DD}
t_{PHZ} t_{PLZ}	Disable Time, $\overline{CS}$ to Output		150 150			70 70			50 50		ns ns	R_L = 1 kΩ to V_{SS} R_L = 1 kΩ to V_{DD}
t_{TLH} t_{THL}	Output Transition Time		75 75			35 35			25 25		ns ns	
	WRITE MODE											
t_{PLH} t_{PHL}	Propagation Delay, WE to Output		150 150			70 70			50 50		ns ns	
	WRITE MODE											
t_wWE	Minimum WE Pulse Width		100			80			60		ns	
t_s t_h	Set-Up Time, D to WE Hold Time, D to WE		50 40			20 20			15 15		ns ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
t_s t_h	Set-Up Time, Address to WE Hold Time, Address to WE		50 40			20 20			15 15		ns ns	
t_s t_h	Set-Up Time, $\overline{CS}$ to WE Hold Time, $\overline{CS}$ to WE		50 40			20 20			15 15		ns ns	

NOTES:
1. Propagation delays and output transition times are graphically described in this section under 34000 Series CMOS Family Characteristics.
2. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with output load capacitance (C_L). Set-up Times (t_s), Hold Times (t_h), Minimum Pulse Widths (t_w) do not vary with load capacitance.

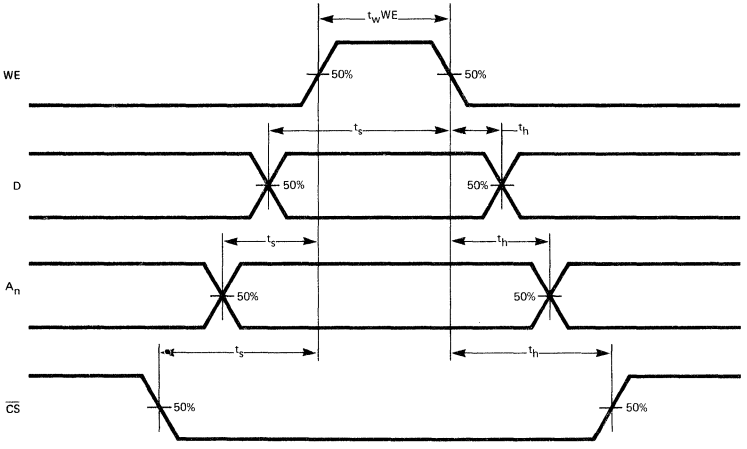
SWITCHING WAVEFORMS

READ MODE



$\overline{CS}$ TO OUTPUT ENABLE AND DISABLE TIMES

WRITE MODE



MINIMUM PULSE WIDTH FOR WE AND SET-UP AND HOLD TIMES, D TO WE, A_n TO WE, AND $\overline{CS}$ TO WE

Note: Set-up and Hold Times are shown as positive values but may be specified as negative values.

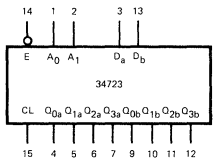
34723
DUAL 4-BIT ADDRESSABLE LATCH

DESCRIPTION – The 34723 is a Dual 4-Bit Addressable Latch with common control inputs; these include two Address Inputs (A_0, A_1), an active LOW Enable Input ($\overline{E}$) and an active HIGH Clear Input (CL). Each latch has a Data Input (D) and four Outputs (Q_0-Q_3).

When the Enable ($\overline{E}$) and Clear (CL) Inputs are HIGH, all Outputs (Q_0-Q_3) are LOW. Dual 4-channel demultiplexing occurs when the Clear Input (CL) is HIGH and the Enable Input ($\overline{E}$) is LOW.

When the Clear (CL) and Enable ($\overline{E}$) inputs are LOW, the selected Output (Q_0-Q_3), determined by the Address Inputs (A_0, A_1), follows the Data Input (D). When the Enable Input ($\overline{E}$) goes HIGH, the contents of the latch are stored. When operating in the addressable latch mode ($\overline{E}$ = CL = LOW), changing more than one bit of the address (A_0, A_1) could impose a transient wrong address. Therefore, this should only be done while in the memory mode ($\overline{E}$ = HIGH, CL = LOW).

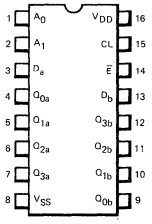
LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

- **SERIAL-TO-PARALLEL CAPABILITY**
- **OUTPUT FROM EACH STORAGE BIT IS AVAILABLE**
- **RANDOM (ADDRESSABLE) DATA ENTRY**
- **ACTIVE HIGH DECODING OR DEMULTIPLEXING CAPABILITY**
- **EASILY EXPANDABLE**
- **ACTIVE HIGH COMMON CLEAR**

CONNECTION DIAGRAM
DIP (TOP VIEW)

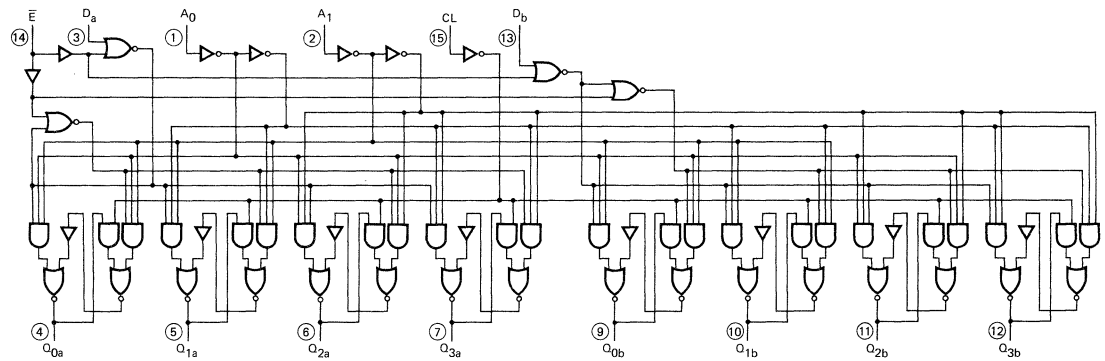


Note: The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

A_0, A_1	Address Inputs
D_a, D_b	Data Inputs
$\overline{E}$	Enable Input (Active LOW)
CL	Clear Input (Active HIGH)
Q_{0a}-Q_{3a}, Q_{0b}-Q_{3b}	Parallel Latch Outputs

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
◯ = Pin Numbers

MODE SELECTION

$\overline{E}$	CL	MODE
L	L	Addressable Latch
H	L	Memory
L	H	Dual 4-Channel Demultiplexer
H	H	Clear

H = HIGH Level
L = LOW Level

TRUTH TABLE

CL	$\overline{E}$	D	A_0	A_1	Q_0	Q_1	Q_2	Q_3	MODE
H	H	X	X	X	L	L	L	L	Clear
H	L	L	L	L	L	L	L	L	Demultiplex
H	L	H	L	L	H	L	L	L	
H	L	L	H	L	L	L	L	L	
H	L	H	H	L	L	H	L	L	
H	L	L	L	H	L	L	L	L	
H	L	H	L	H	L	L	H	L	
H	L	L	H	H	L	L	L	L	
H	L	H	H	H	L	L	L	H	
L	H	X	X	X	Q_{N-1}	Q_{N-1}	Q_{N-1}	Q_{N-1}	Memory
L	L	L	L	L	L	Q_{N-1}	Q_{N-1}	Q_{N-1}	Addressable
L	L	H	L	L	H	Q_{N-1}	Q_{N-1}	Q_{N-1}	Latch
L	L	L	H	L	Q_{N-1}	L	Q_{N-1}	Q_{N-1}	
L	L	H	H	L	Q_{N-1}	H	Q_{N-1}	Q_{N-1}	
L	L	L	L	H	Q_{N-1}	Q_{N-1}	L	Q_{N-1}	
L	L	H	L	H	Q_{N-1}	Q_{N-1}	H	Q_{N-1}	
L	L	L	H	H	Q_{N-1}	Q_{N-1}	Q_{N-1}	L	
L	L	H	H	H	Q_{N-1}	Q_{N-1}	Q_{N-1}	H	

L = LOW Level
H = HIGH Level
X = Don't Care
Q_{N-1} = State before the positive transition of the Enable Input

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			10			20		4		µA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					100			200		40			MAX	
		XM			1			2		0.4		µA	MIN, 25°C	
					15			30		6			MAX	

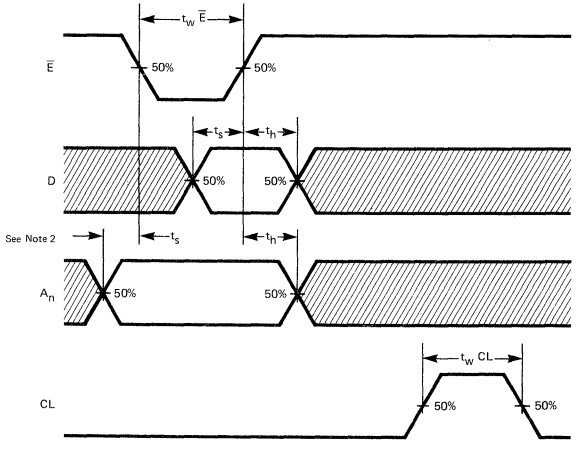
Note: Additional DC Characteristics are listed in this section under 34000 Series CMOS Family Characteristics.

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, $\overline{E}$ to Q_n		90 90			40 40			30 30		ns ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
t_{PLH} t_{PHL}	Propagation Delay, D to Q_n		75 75			35 35			25 25		ns ns	
t_{PLH} t_{PHL}	Propagation Delay, Address to Q_n		100 100			45 45			35 35		ns ns	
t_{PHL}	Propagation Delay, CL to Q_n		75			35			25		ns	
t_{TLH} t_{THL}	Output Transition Time		40 40			20 20			15 15		ns ns	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{E}$ to Q_n		110 100			50 50			35 35		ns ns	C_L = 50 pF Input Transition Times ⩽ 20 ns
t_{PLH} t_{PHL}	Propagation Delay, D to Q_n		95 95			45 45			30 30		ns ns	
t_{PLH} t_{PHL}	Propagation Delay, Address to Q_n		120 120			55 55			40 40		ns ns	
t_{PHL}	Propagation Delay, CL to Q_n		95			45			30		ns	
t_{TLH} t_{THL}	Output Transition Time		75 75			40 40			25 25		ns ns	
t_s t_h	Set-Up Time, D to $\overline{E}$ Hold Time, D to $\overline{E}$		30 40			10 20			5 20		ns ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
t_s t_h	Set-Up Time, Address to $\overline{E}$ Hold Time, Address to $\overline{E}$		30 40			10 20			5 20		ns ns	
$t_w\overline{E}$	Minimum $\overline{E}$ Pulse Width		50			20			15		ns	
t_wCL	Minimum CL Pulse Width		50			20			15		ns	

NOTES:
1. Propagation delays and output transition times are graphically described in this section under 34000 Series CMOS Family Characteristics.
2. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with output load capacitance (C_L). Set-up Times (t_s), Hold Times (t_h), and Minimum Pulse Widths (t_w) do not vary with load capacitance.

SWITCHING WAVEFORMS



MINIMUM PULSE WIDTH FOR $\overline{E}$ AND CL AND SET-UP AND HOLD TIMES, D TO $\overline{E}$ AND A_n TO $\overline{E}$

NOTES:
1. Set-up and Hold Times are shown as positive values but may be specified as negative values.
2. The Address to Enable Set-up Time is the time before the HIGH-to-LOW Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.

34725

64-BIT (16×4) RANDOM ACCESS MEMORY WITH 3-STATE OUTPUTS

DESCRIPTION – The 34725 is a 64-Bit Random Access Memory with 3-State Outputs organized as 16 words by four bits with four Data Inputs (D_0-D_3), four Address Inputs (A_0-A_3), an active LOW Write Enable Input ($\overline{WE}$), an active LOW Chip Select Input ($\overline{CS}$) and four active LOW 3-State Outputs ($\overline{Q}_0$-$\overline{Q}_3$).

Information on the four Data Inputs (D_0-D_3) is written into the memory location selected by the Address Inputs (A_0-A_3) when both the Chip Select Input ($\overline{CS}$) and the Write Enable Input ($\overline{WE}$) are LOW. Under these conditions, the Outputs ($\overline{Q}_0$-$\overline{Q}_3$) are held in a high impedance OFF state. Information is read from the memory location selected by the Address Inputs (A_0-A_3) while the Chip Select Input ($\overline{CS}$) is LOW and the Write Enable Input ($\overline{WE}$) is HIGH. The Outputs ($\overline{Q}_0$-$\overline{Q}_3$) are the complement of the information written into the memory. When the Chip Select Input ($\overline{CS}$) is HIGH, all Outputs ($\overline{Q}_0$-$\overline{Q}_3$) are held in the high impedance OFF state. This allows other 3-State outputs to be wired together in a bus arrangement. The 34725 offers fully static operation.

- **3-STATE OUTPUTS**
- **ORGANIZATION – 16 WORDS X 4 BITS**
- **ON-CHIP DECODING**
- **INVERTED DATA OUTPUT**
- **FULLY STATIC OPERATION**

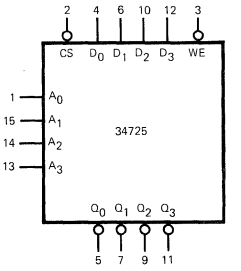
PIN NAMES

$\overline{CS}$	Chip Select Input (Active LOW)
$\overline{WE}$	Write Enable Input (Active LOW)
D_0-D_3	Data Inputs
A_0-A_3	Address Inputs
$\overline{Q}_0$-$\overline{Q}_3$	3-State Outputs (Active LOW)

MODE SELECTION

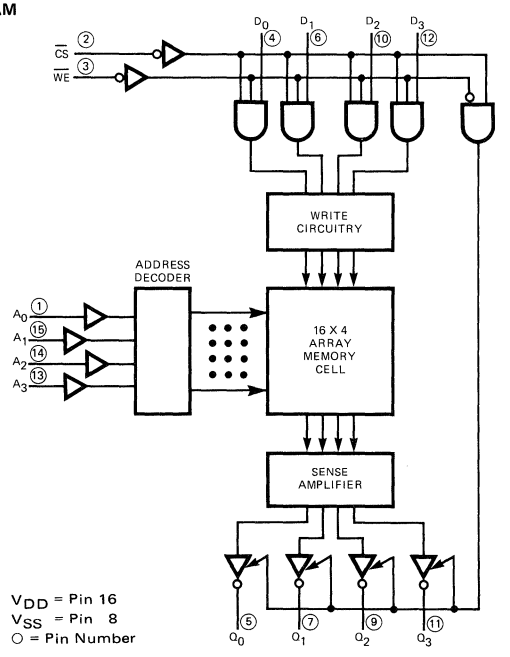
$\overline{CS}$	$\overline{WE}$	OUTPUTS	MODE
L	L	High Impedance	Write
L	H	Outputs are Complement of Data Written into Location	Read
H	X	High Impedance	Inhibit

LOGIC SYMBOL



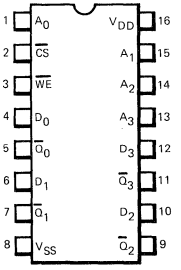
V_{DD} = Pin 16
V_{SS} = Pin 8

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Number

CONNECTION DIAGRAM
DIP (TOP VIEW)



Note: The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V

SYMBOL	PARAMETER	LIMITS									UNITS	TEMP	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{OZH}	Output OFF Current HIGH		0.05 3.0			0.1 6.0			0.2 12.0		µA	MIN, 25°C MAX	Output Returned to V_{DD}, $\overline{CS}$ = V_{DD}
I_{OZL}	Output OFF Current LOW		-0.05 -3.0			-0.1 -6.0			-0.2 -12.0		µA	MIN, 25°C MAX	Output Returned to V_{SS}, $\overline{CS}$ = V_{DD}
I_{DD}	Quiescent Power Supply Current XC		2.5 15			5 30			10 60		µA	MIN, 25°C MAX	All inputs common and at 0 V or V_{DD}
	Quiescent Power Supply Current XM		2.5 15			5 30			10 60		µA	MIN, 25°C MAX	

Note: Additional DC Characteristics are listed in this section under 34000 Series CMOS Family Characteristics.

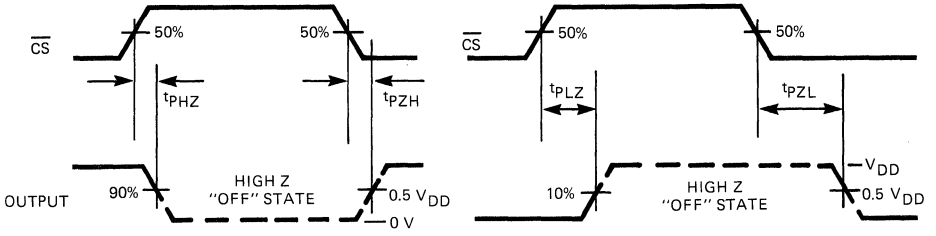
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
	READ MODE											C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Address to Output		180 180			70 70			50 50		ns ns	Input Transition Times ⩽ 20 ns
t_{PZH} t_{PZL}	Enable Time, $\overline{CS}$ to Output		135 135			60 60			45 45		ns ns	R_L = 1 kΩ to V_{SS} R_L = 1 kΩ to V_{DD}
t_{PHZ} t_{PLZ}	Disable Time, $\overline{CS}$ to Output		135 135			60 60			45 45		ns ns	R_L = 1 kΩ to V_{SS} R_L = 1 kΩ to V_{DD}
t_{TLH} t_{THL}	Output Transition Time		40 40			20 20			15 15		ns ns	
	WRITE MODE											
t_{PZH} t_{PZL}	Enable Time $\overline{WE}$ to Output		135 135			60 60			45 45		ns ns	R_L = 1 kΩ to V_{SS} R_L = 1 kΩ to V_{DD}
t_{PHZ} t_{PLZ}	Disable Time, $\overline{WE}$ to Output		135 135			60 60			45 45		ns ns	R_L = 1 kΩ to V_{SS} R_L = 1 kΩ to V_{DD}
	READ MODE											C_L = 50 pF
t_{PLH} t_{PHL}	Propagation Delay, Address to Output		200 200			95 95			70 70		ns ns	Input Transition Times ⩽ 20 ns
t_{PZH} t_{PZL}	Enable Time, $\overline{CS}$ to Output		150 150			70 70			50 50		ns ns	R_L = 1 kΩ V_{SS} R_L = 1 kΩ V_{DD}
t_{PHZ} t_{PLZ}	Disable Time, $\overline{CS}$ to Output		150 150			70 70			50 50		ns ns	R_L = 1 kΩ to V_{SS} R_L = 1 kΩ to V_{DD}
t_{TLH} t_{THL}	Output Transition Time		75 75			35 35			25 25		ns ns	
	WRITE MODE											
t_{PZH} t_{PZL}	Enable Time, $\overline{WE}$ to Output		150 150			70 70			50 50		ns ns	R_L = 1 kΩ to V_{SS} R_L = 1 kΩ to V_{DD}
t_{PHZ} t_{PLZ}	Disable Time, $\overline{WE}$ to Output		150 150			70 70			50 50		ns ns	R_L = 1 kΩ to V_{SS} R_L = 1 kΩ to V_{DD}
	WRITE MODE											
$t_w\overline{WE}$	Minimum $\overline{WE}$ Pulse Width		180			100			80		ns	
t_s t_h	Set-Up Time, D_n to $\overline{WE}$ Hold Time, D_n to $\overline{WE}$		150 40			120 20			115 15		ns ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
t_s t_h	Set-Up Time, Address to $\overline{WE}$ Hold Time, Address to $\overline{WE}$		150 40			120 20			115 15		ns ns	
t_s t_h	Set-Up Time, $\overline{CS}$ to $\overline{WE}$ Hold Time, $\overline{CS}$ to $\overline{WE}$		150 40			120 20			115 15		ns ns	

NOTES:
1. Propagation Delays and Output Transition Times are graphically described in this section under 34000 Series CMOS Family Characteristics.
2. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Set-up Times (t_s), Hold Times (t_h), and Minimum Pulse Widths (t_w) do not vary with load capacitance.

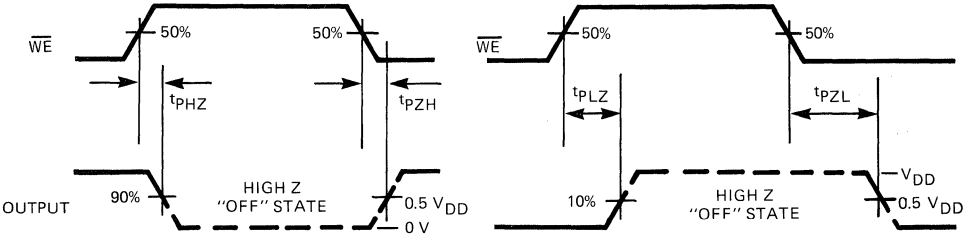
SWITCHING WAVEFORMS

READ MODE

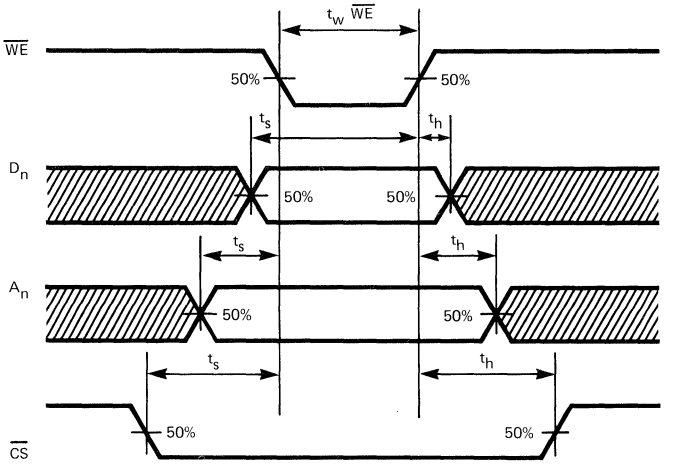


$\overline{CS}$ TO OUTPUT ENABLE AND DISABLE TIMES

WRITE MODE



$\overline{WE}$ TO OUTPUT ENABLE AND DISABLE TIMES



MINIMUM $\overline{WE}$ PULSE WIDTH AND SET-UP AND HOLD TIMES, D_n TO $\overline{WE}$, A_n TO $\overline{WE}$, AND $\overline{CS}$ TO $\overline{WE}$

Note: Set-up and Hold Times are shown as positive values but may be specified as negative values.

340085

4-BIT MAGNITUDE COMPARATOR

DESCRIPTION – The 340085 is a 4-Bit Magnitude Comparator which compares two 4-bit words (A, B), each word having four Parallel Inputs (A_0-A_3,B_0-B_3); A_3,B_3 being the most significant inputs. Operation is not restricted to binary codes, the device will work with any monotonic code. Three Outputs are provided: "A greater than B" ($O_{A>B}$), "A less than B" ($O_{A<B}$), "A equal to B" ($O_{A=B}$). Three Expander Inputs, $I_{A>B}$, $I_{A<B}$, $I_{A=B}$, allow cascading without external gates. For proper compare operation the Expander Inputs to the least significant position must be connected as follows: $I_{A<B} = I_{A>B} = L$, $I_{A=B} = H$. For serial (ripple) expansion, the $O_{A>B}$, $O_{A<B}$ and $O_{A=B}$ Outputs are connected respectively to the $I_{A>B}$, $I_{A<B}$, and $I_{A=B}$ inputs of the next most significant comparator, as shown in Figure 1. Refer to Applications section of data sheet for high speed method of comparing large words.

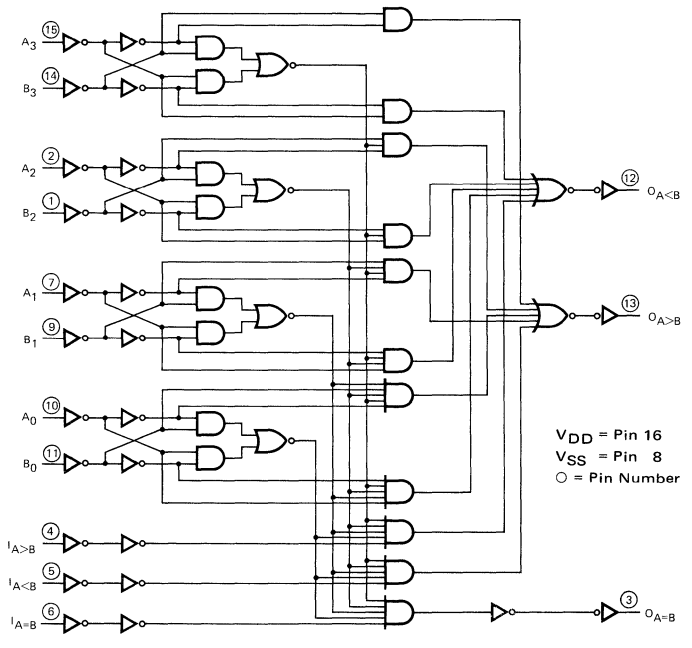
The Truth Table on the following page describes the operation of the 340085 under all possible logic conditions. The upper 11 lines describe the normal operation under all conditions that will occur in a single device or in a series expansion scheme. The lower five lines describe the operation under abnormal conditions on the cascading inputs. These conditions occur when the parallel expansion technique is used.

- **EASILY EXPANDABLE**
- **BINARY OR BCD COMPARISON**
- **$O_{A>B}$, $O_{A<B}$, AND $O_{A=B}$ OUTPUTS AVAILABLE**

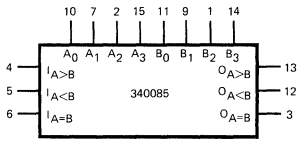
PIN NAMES

A_0-A_3	Word A Parallel Inputs
B_0-B_3	Word B Parallel Inputs
$I_{A>B}$, $I_{A<B}$, $I_{A=B}$	Expander Inputs
$O_{A>B}$	A Greater than B Output
$O_{A<B}$	A Less than B Output
$O_{A=B}$	A Equal to B Output

LOGIC DIAGRAM

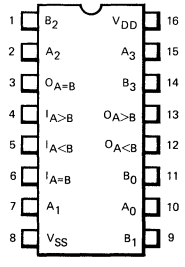


LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



Note: The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

TRUTH TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A_3,B_3	A_2,B_2	A_1,B_1	A_0,B_0	$I_{A>B}$	$I_{A<B}$	$I_{A=B}$	$O_{A>B}$	$O_{A<B}$	$O_{A=B}$
$A_3>B_3$	X	X	X	X	X	X	H	L	L
$A_3<B_3$	X	X	X	X	X	X	L	H	L
$A_3=B_3$	$A_2>B_2$	X	X	X	X	X	H	L	L
$A_3=B_3$	$A_2<B_2$	X	X	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1>B_1$	X	X	X	X	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1<B_1$	X	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0>B_0$	X	X	X	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0<B_0$	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	L	L	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	H	L	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	L	H	L	L	H
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	H	H	L	H	H
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	L	H	H	L	H
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	H	H	H	H	H
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	H	L	H	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	L	L	L	L	L

H = HIGH Level
L = LOW Level
X = Don't Care

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V

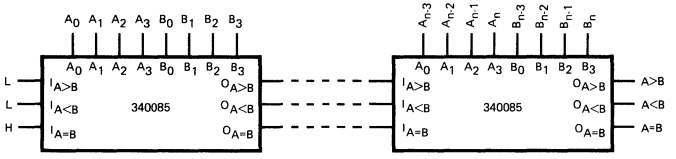
SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			50			100		20		µA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					700			1400		280			MAX	
		XM			5			10		2		µA	MIN, 25°C	
					300			600		120			MAX	

Note: Additional DC Characteristics are listed in this section under 34000 Series CMOS Family Characteristics.

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay,		160			65			45		ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
t_{PHL}	A_n or B_n to any Output		160			65			45		ns	
t_{PLH}	Propagation Delay,		115			45			30		ns	
t_{PHL}	Any I to any Output		115			45			30		ns	
t_{TLH}	Output Transition		30			17			13		ns	
t_{THL}	Time		30			17			13		ns	
t_{PLH}	Propagation Delay,		180			70			50		ns	C_L = 50 pF Input Transition Times ⩽ 20 ns
t_{PHL}	A_n or B_n to any Output		180			70			50		ns	
t_{PLH}	Propagation Delay,		135			55			40		ns	
t_{PHL}	Any I to any Output		135			55			40		ns	
t_{TLH}	Output Transition		60			30			20		ns	
t_{THL}	Time		60			30			20		ns	

NOTE:
1. Propagation delays and output transition times are graphically described in this section under 34000 Series CMOS Family Characteristics.



L = LOW Level
H = HIGH Level

Fig. 1. COMPARING TWO n-BIT WORDS

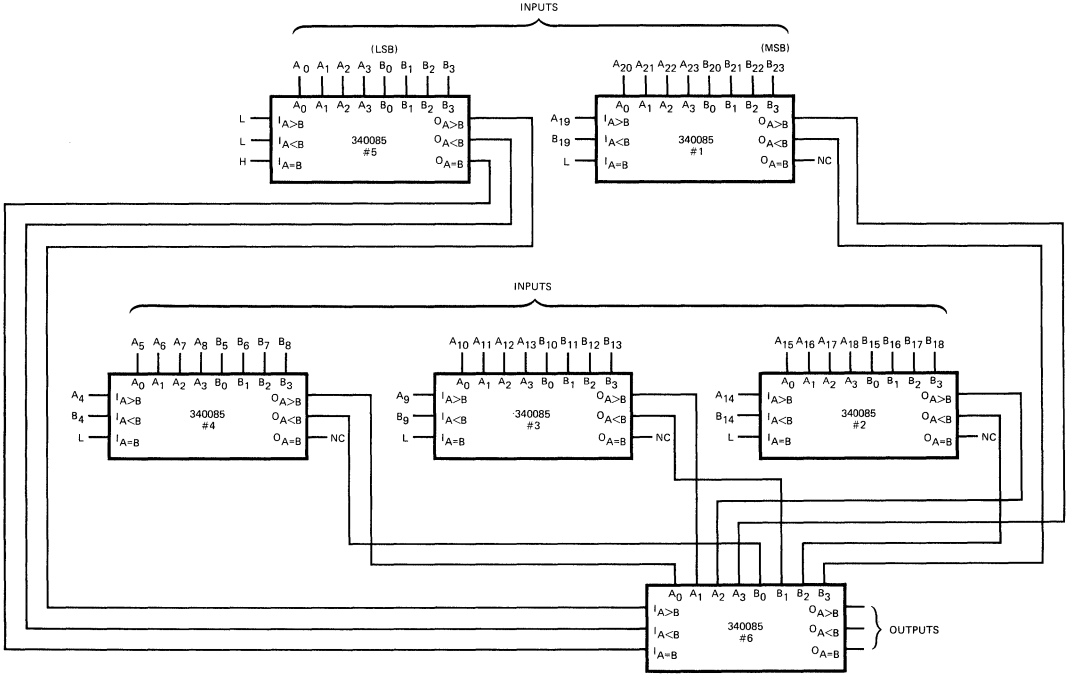
APPLICATIONS

Figure 2 shows a high speed method of comparing two 24-bit words with only two levels of device delay. With the technique shown in Figure 1, six levels of device delay result when comparing two 24-bit words. The parallel technique can be expanded to any number of bits, see Table I.

TABLE I

WORD LENGTH	NUMBER OF PKGS.
1-4 Bits	1
5-24 Bits	2 - 6
25-120 Bits	8 - 31

NOTE:
The 340085 can be used as a 5-bit comparator only when the outputs are used to drive the A_0-A_3 and B_0-B_3 inputs of another 340085 as shown in Figure 2 in positions #1, 2, 3, and 4.



MSB = Most Significant Bit
LSB = Least Significant Bit

L = LOW Level
H = HIGH Level
NC = No Connection

Fig. 2. COMPARISON OF TWO 24-BIT WORDS

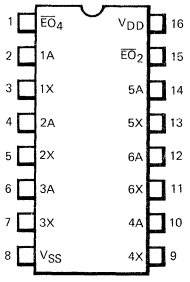
340097 • 340098

3-STATE HEX NON-INVERTING AND INVERTING BUFFERS

DESCRIPTION – These two CMOS buffers provide high current output capability suitable for driving high capacitance loads. The 340097 is a Non-Inverting CMOS Buffer with 3-state outputs and the 340098 is an Inverting CMOS Buffer with 3-state outputs. The 3-state outputs of each device are controlled by two Enable Inputs ($\overline{EO}_4$, $\overline{EO}_2$). A HIGH on Enable Input $\overline{EO}_4$ causes the Outputs of four of the six buffer elements to assume a high impedance or OFF state, regardless of other input conditions and a HIGH on Enable Input $\overline{EO}_2$ causes the Outputs of the remaining two buffer elements to assume a high impedance or OFF state, regardless of other input conditions.

- **3-STATE OUTPUTS**
- **TTL COMPATIBLE – FAN OUT OF ONE TTL LOAD**
- **ACTIVE LOW ENABLE INPUTS**

CONNECTION DIAGRAM
DIP (TOP VIEW)

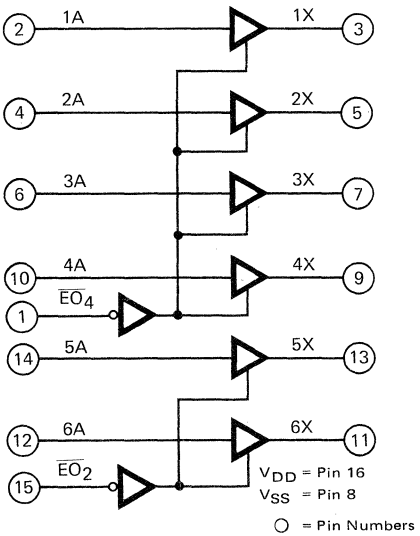


NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

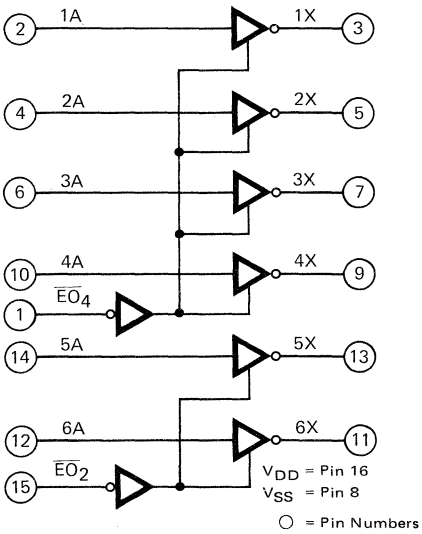
PIN NAMES

1A-6A	Buffer Inputs
$\overline{EO}_4$, $\overline{EO}_2$	Enable Inputs (Active LOW)
1X-6X	Buffer Outputs (Active HIGH for the 340097 and Active LOW for the 340098)

340097 LOGIC DIAGRAM



340098 LOGIC DIAGRAM



DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V

SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEMP	TEST CONDITIONS
$I_{SC(H)}$	Output Short Circuit Current		-4.35			-20						mA	All	V_{IN} = V_{DD} or V_{SS} per Function, V_{OUT} = V_{SS}
$I_{SC(L)}$	Output Short Circuit Current		4.35			20						mA	All	V_{IN} = V_{DD} or V_{SS} per Function, V_{OUT} = V_{DD}
I_{OH}	Output HIGH Current		-1.6 Note 2									mA	All	V_{OUT} = 2.4 V, Inputs at 0 V or V_{DD} per Function
I_{OL}	Output LOW Current		1.6 Note 2									mA	All	V_{OUT} = 0.4 V, Inputs at 0 V or V_{DD} per Function
I_{OZH}	Output OFF Current HIGH	XC			0.5 7			0.5 7			0.5 7	µA	MIN, 25°C MAX	Output Returned to V_{DD}, $\overline{EO}_n$ = V_{DD}
		XM			0.05 3			0.05 3			0.05 3	µA	MIN, 25°C MAX	
I_{OZL}	Output OFF Current LOW	XC			-0.5 -7			-0.5 -7			-0.5 -7	µA	MIN, 25°C MAX	Output Returned to V_{SS}, $\overline{EO}_n$ = V_{DD}
		XM			-0.05 -3			-0.05 -3			-0.05 -3	µA	MIN, 25°C MAX	
I_{DD}	Quiescent Power Supply Current	XC			3 42			5 70		1 14		µA	MIN, 25°C MAX	All inputs common and at 0 V or V_{DD}
		XM			0.3 20			0.5 30		0.1 6		µA	MIN, 25°C MAX	

NOTES:
1. Additional DC Characteristics are listed in this section under 34000 Series CMOS Family Characteristics.
2. For I_{OH} and I_{OL} tests, V_{DD} = 4.5 V for military grade product and V_{DD} = 4.75 V for commercial grade product.

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C, 340097 only

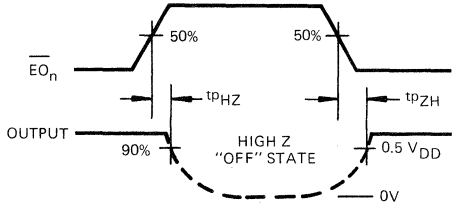
SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEST CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay, Data to Output		45 45			22 22			18 18		ns ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
t_{PZH} t_{PZL}	Output Enable Time		60 85			30 35			25 28		ns ns	R_L = 1 kΩ to V_{SS} R_L = 1 kΩ to V_{DD}
t_{PHZ} t_{PLZ}	Output Disable Time		35 55			28 33			25 27		ns ns	R_L = 1 kΩ to V_{SS} R_L = 1 kΩ to V_{DD}
t_{TLH} t_{THL}	Output Transition Time		25 25			15 15			10 10		ns ns	
t_{PLH} t_{PHL}	Propagation Delay, Data to Output		65 65			28 28			20 20		ns ns	C_L = 50 pF Input Transition Times ⩽ 20 ns
t_{PZH} t_{PZL}	Output Enable Time		70 95			35 40			29 30		ns ns	R_L = 1 kΩ to V_{SS} R_L = 1 kΩ to V_{DD}
t_{PHZ} t_{PLZ}	Output Disable Time		40 60			31 35			29 30		ns ns	R_L = 1 kΩ to V_{SS} R_L = 1 kΩ to V_{DD}
t_{TLH} t_{THL}	Output Transition Time		40 40			20 20			15 15		ns ns	

NOTE:
1. Propagation Delays and Output Transition Times are graphically described in this section under 34000 Series CMOS Family Characteristics.

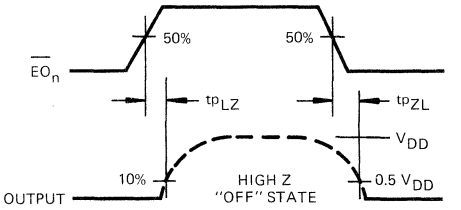
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C, 340098 only

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay,		45			30			25		ns	C_L = 15 pF
t_{PHL}	Data to Output		45			30			25		ns	Input Transition Times ⩽ 20 ns
t_{PZH}	Output Enable		60			30			25		ns	R_L = 1 kΩ to V_{SS}
t_{PZL}	Time		85			35			28		ns	R_L = 1 kΩ to V_{DD}
t_{PHZ}	Output Disable		35			28			25		ns	R_L = 1 kΩ to V_{SS}
t_{PLZ}	Time		55			33			27		ns	R_L = 1 kΩ to V_{DD}
t_{TLH}	Output Transition		25			15			10		ns	
t_{THL}	Time		25			15			10		ns	
t_{PLH}	Propagation Delay,		75			35			30		ns	C_L = 50 pF
t_{PHL}	Data to Output		75			35			30		ns	Input Transition Times ⩽ 20 ns
t_{PZH}	Output Enable		70			35			29		ns	R_L = 1 kΩ to V_{SS}
t_{PZL}	Time		95			40			30		ns	R_L = 1 kΩ to V_{DD}
t_{PHZ}	Output Disable		40			31			29		ns	R_L = 1 kΩ to V_{SS}
t_{PLZ}	Time		60			35			30		ns	R_L = 1 kΩ to V_{DD}
t_{TLH}	Output Transition		40			20			15		ns	
t_{THL}	Time		40			20			15		ns	

SWITCHING WAVEFORMS



OUTPUT ENABLE TIME
(t_{PZH}) AND OUTPUT DISABLE TIME (t_{PHZ})



OUTPUT ENABLE TIME
(t_{PZL}) AND OUTPUT DISABLE TIME (t_{PLZ})

340160 • 340161 • 340162 • 340163

4-BIT SYNCHRONOUS COUNTERS

DESCRIPTION — The 340160 and the 340162 are fully synchronous edge-triggered 4-Bit Decade Counters. The 340161 and the 340163 are fully synchronous edge-triggered 4-Bit Binary Counters. Each device has a Clock Input (CP); four synchronous Parallel Data Inputs (P_0-P_3); three synchronous Mode Control Inputs, Parallel Enable ($\overline{PE}$), Count Enable Parallel (CEP) and Count Enable trickle (CET); Buffered Outputs from all four bit positions (Q_0-Q_3); and a Terminal Count Output (TC). The 340162 and 340163 have an additional synchronous Mode Control Input, Synchronous Reset ($\overline{SR}$). Alternately, the 340160 and 340161 have an overriding asynchronous Master Reset ($\overline{MR}$).

Operation is fully synchronous (except for Master Reset on the 340160 and 340161) and occurs on the LOW-to-HIGH transition of the Clock Input (CP). When the Parallel Enable Input ($\overline{PE}$) is LOW, the next LOW-to-HIGH transition of the Clock Input (CP) loads data into the counter from Parallel Inputs (P_0-P_3). When the Parallel Enable Input ($\overline{PE}$) is HIGH, the next LOW-to-HIGH transition of the Clock Input (CP) advances the counter to its next state only if both Count Enable Inputs (CEP and CET) are HIGH; otherwise, no change occurs in the state of the counter. The Terminal Count Output (TC) is HIGH when the state of the counter is nine ($Q_0 = Q_3$ = HIGH, $Q_1 = Q_2$ = LOW) for the 340160 and 340162/fifteen ($Q_0 = Q_1 = Q_2 = Q_3$ = HIGH) for the 340161 and 340163 and the Count Enable Trickle Input (CET) is HIGH. For the 340162 and 340163, a LOW on the Synchronous Reset Input ($\overline{SR}$) sets all Outputs (Q_0-Q_3 and TC) LOW on the next LOW-to-HIGH transition of the Clock Input (CP), independent of the state of all other synchronous Mode Control Inputs (CEP, CET, $\overline{PE}$). For the 340160 and 340161, a LOW on the overriding asynchronous Master Reset ($\overline{MR}$) sets all outputs (Q_0-Q_3 and TC) LOW, independent of the state of all other inputs.

These devices perform multistage synchronous counting without additional components by using a carry look-ahead counting technique.

The 340160, 340161, 340162, and 340163 are edge-triggered; therefore, the synchronous Mode Control Input (CEP, CET, $\overline{PE}$ for the 340160/340161 and CEP, CET, $\overline{PE}$, $\overline{SR}$ for the 340162/340163) must be stable only during the set-up time before the LOW-to-HIGH transition of the Clock Input (CP).

- **12 MHz TYPICAL COUNT FREQUENCY AT V_{DD} = 10 V**
- **DECODED TERMINAL COUNT**
- **FULLY SYNCHRONOUS COUNTING AND PARALLEL ENTRY**
- **SYNCHRONOUS (340162/340163) OR ASYNCHRONOUS (340160/340161) RESET**
- **BUILT-IN CARRY CIRCUITRY**
- **FULLY EDGE-TRIGGERED**

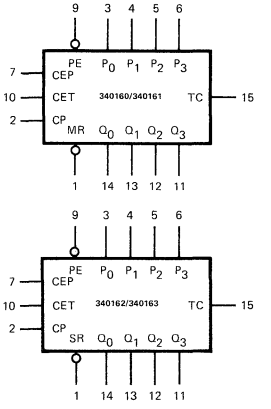
PIN NAMES

$\overline{PE}$	Parallel Enable Input (Active LOW)
P_0-P_3	Parallel Inputs
CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock Input (L→H Edge-Triggered)
$\overline{MR}$	Master Reset Input (Active LOW) for the 340160/340161 Only
$\overline{SR}$	Synchronous Reset Input (Active LOW) for the 340162/340163 Only
Q_0-Q_3	Parallel Outputs
TC	Terminal Count Output

SELECTOR GUIDE

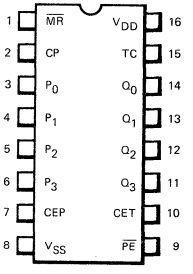
RESET	MODULUS	
	DECADE	BINARY
Asynchronous	340160	340161
Synchronous	340162	340163

LOGIC SYMBOL

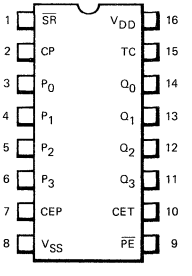


V_{DD} = Pin 16
V_{SS} = Pin 8

340160/340161 CONNECTION DIAGRAM DIP (TOP VIEW)



340162/340163 CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

SYNCHRONOUS MODE SELECTION
340160/340161

$\overline{PE}$	CEP	CET	MODE
L	X	X	Preset
H	L	X	No Change
H	X	L	No Change
H	H	H	Count

$\overline{MR}$ = HIGH

SYNCHRONOUS MODE SELECTION
340162/340163

$\overline{SR}$	$\overline{PE}$	CEP	CET	MODE
H	L	X	X	Preset
H	H	L	X	No Change
H	H	X	L	No Change
H	H	H	H	Count
L	X	X	X	Reset

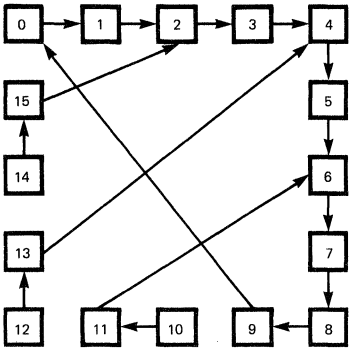
TERMINAL COUNT GENERATION

CET	340160/340162 $(Q_0 \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot Q_3)$	340161/340163 $(Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3)$	TC
L	L	L	L
L	H	H	L
H	L	L	L
H	H	H	H

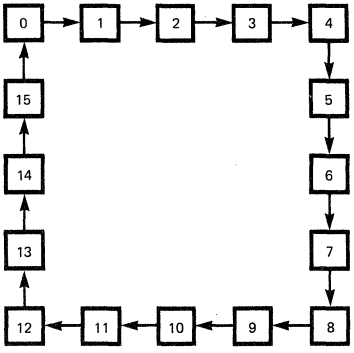
$TC = CET \cdot Q_0 \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot Q_3$ (340160/340162)
$TC = CET \cdot Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3$ (340161/340163)

H = HIGH Level
L = LOW Level
X = Don't Care

STATE DIAGRAM
340160 · 340162



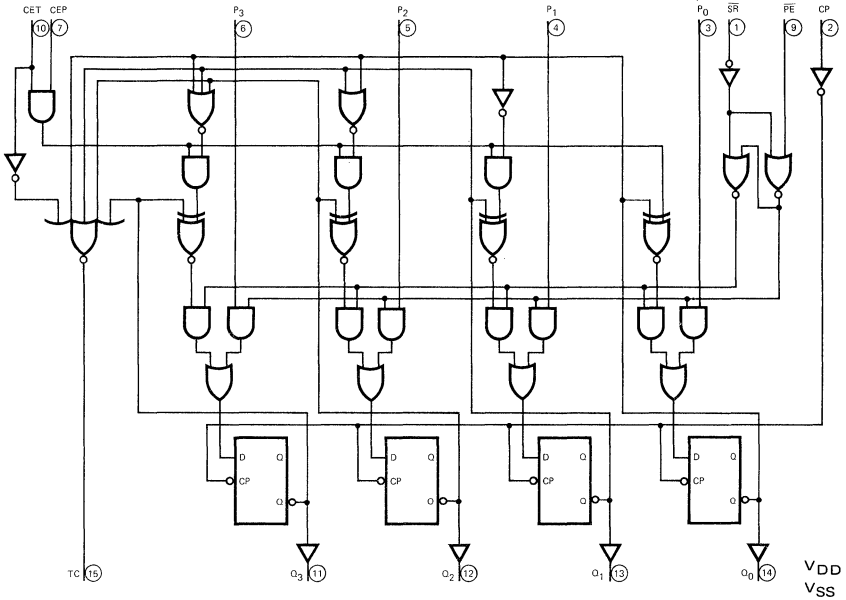
STATE DIAGRAM
340161 · 340163



NOTE:
The 340160 or 340162 can be preset to any state, but will not count beyond 9. If preset to state 10, 11, 12, 13, 14 or 15, they will return to their normal sequence within two clock pulses.

340161/340163 LOGIC DIAGRAM

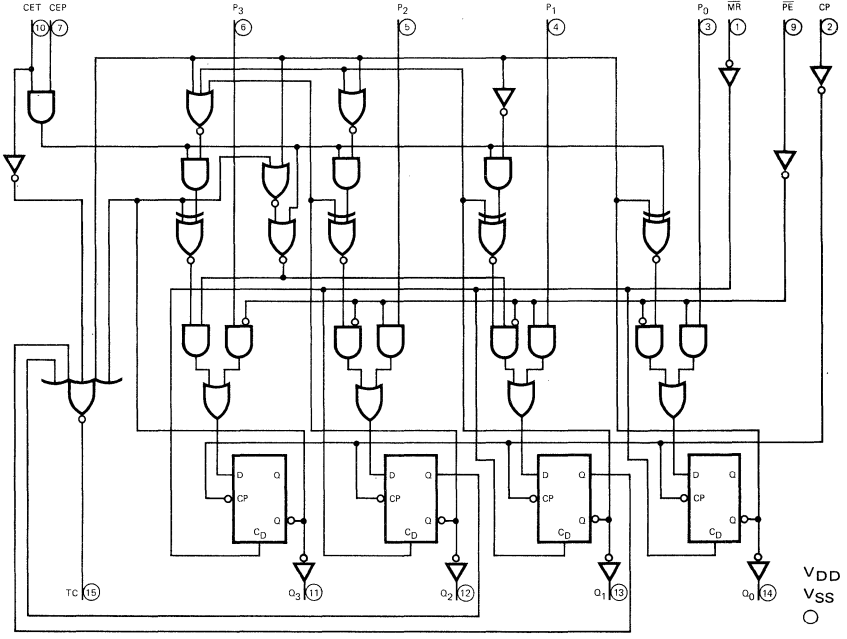
The 340161 and 340163 binary synchronous counters are similar. However, the 340161 has an asynchronous master reset circuit as shown on the 340160/340162 Logic Diagram.



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Numbers

340160/340162 LOGIC DIAGRAM

The 340160 and 340162 BCD synchronous counters are similar. However, the 340162 has a synchronous reset circuit as shown on the 340161/340163 Logic Diagram.



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Numbers

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V

SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEMP	TEST CONDITIONS
I_{DD}	Quiescent Power Supply Current	XC			100			200		40		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					700			1400		280			MAX	
		XM			20			40		8		μA	MIN, 25°C	
					300			600		120			MAX	

NOTE: Additional DC Characteristics are listed in this section under 34000 Series CMOS Family Characteristics.

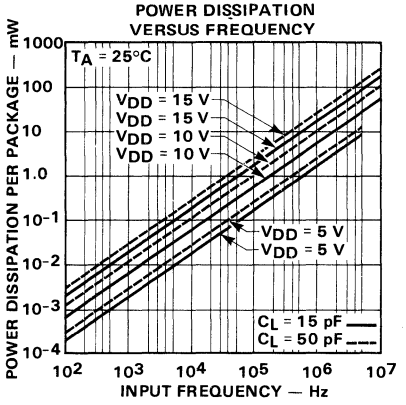
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C

SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEST CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay, CP to Q		95 95	185 185		50 50	90 90		33 35		ns ns	
t_{PLH} t_{PHL}	Propagation Delay, CP to TC		130 130	250 250		60 60	115 115		37 37		ns ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
t_{PLH} t_{PHL}	Propagation Delay, CET to TC		70 75	130 130		32 45	65 80		20 30		ns ns	
t_{PHL}	Propagation Delay, $\overline{MR}$ to Q		128	250		55	110		37		ns	(340160/340161)
t_{PHL}	Propagation Delay, $\overline{MR}$ to TC		153	300		65	130		45		ns	(340160/340161)
t_{TLH} t_{THL}	Output Transition Time		35 40	75 75		20 20	40 40		15 15	25 25	ns ns	
t_{PLH} t_{PHL}	Propagation Delay, CP to Q		120 120	220 220		55 55	105 105		40 38		ns ns	
t_{PLH} t_{PHL}	Propagation Delay, CP to TC		155 155	285 285		70 70	130 130		45 40		ns ns	C_L = 50 pF Input Transition Times ⩽ 20 ns
t_{PLH} t_{PHL}	Propagation Delay, CET to TC		95 95	165 165		40 55	80 95		27 36		ns ns	
t_{PHL}	Propagation Delay, $\overline{MR}$ to Q		150	285		65	125		44		ns	(340160/340161)
t_{PHL}	Propagation Delay, $\overline{MR}$ to TC		175	335		75	145		52		ns	(340160/340161)
t_{TLH} t_{THL}	Output Transition Time		60 70	135 135		35 30	70 70		25 23	45 45	ns ns	
t_{rec}	$\overline{MR}$ Recovery Time	3	1		20	1			1		ns	(340160/340161)
$t_W\overline{MR}(L)$	$\overline{MR}$ Minimum Pulse Width	110	60		55	27			17		ns	(340160/340161)
t_WCP	CP Minimum Pulse Width	90	50		40	20			15		ns	
t_s t_h	Set-Up Time, Data to CP Hold Time, Data to CP	70 0	35 -30		35 0	18 -15			13 -10		ns ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
t_s t_h	Set-Up Time, $\overline{PE}$ to CP Hold Time, $\overline{PE}$ to CP	110 -10	60 -57		60 -5	30 -28			20 -18		ns ns	
t_s t_h	Set-Up Time, CEP, CET to CP Hold Time, CEP, CET to CP	200 -20	115 -110		95 -10	50 -48			35 -32		ns ns	
t_s t_h	Set-Up Time, $\overline{SR}$ to CP Hold Time, $\overline{SR}$ to CP	40 0	15 -5		18 0	15 -2			4 0		ns ns	(340162/340163) (340162/340163)
f_{MAX}	Input Count Frequency (Note 3)	3	6		7	12					MHz	

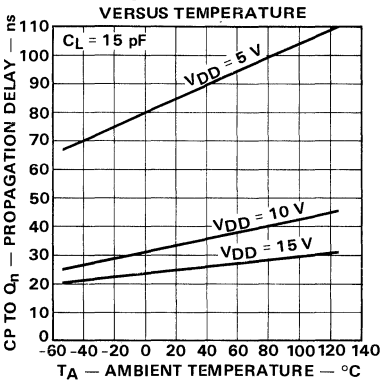
NOTES:
1. Propagation Delays and Output Transition Times are graphically described in this section under 34000 Series CMOS Family Characteristics.
2. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Set-up Times (t_s), Hold Times (t_h), Recovery Times (t_{rec}), and Minimum Pulse Widths (t_w), do not vary with load capacitance.
3. For f_{MAX} input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
4. It is recommended that input rise and fall times to the Clock Input be less than 15 μs.

TYPICAL ELECTRICAL CHARACTERISTICS

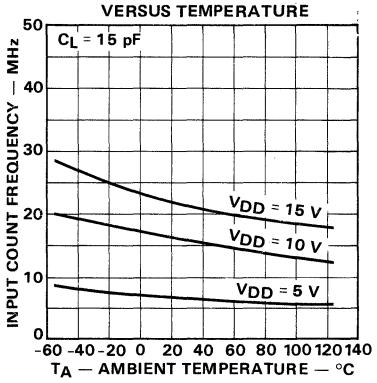
POWER DISSIPATION VERSUS FREQUENCY



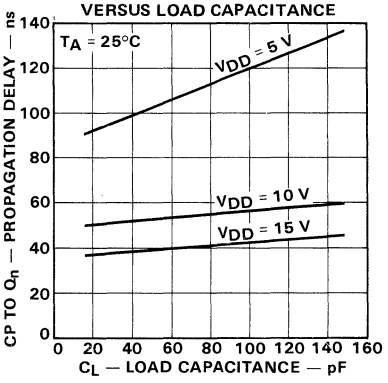
PROPAGATION DELAY VERSUS TEMPERATURE



INPUT COUNT FREQUENCY VERSUS TEMPERATURE

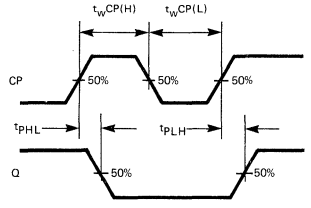


PROPAGATION DELAY VERSUS LOAD CAPACITANCE



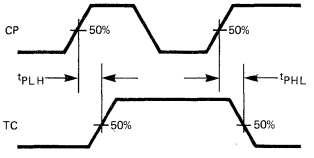
SWITCHING DIAGRAMS

CLOCK (CP) TO OUTPUT (Q) PROPAGATION DELAYS AND MINIMUM CLOCK PULSE WIDTH



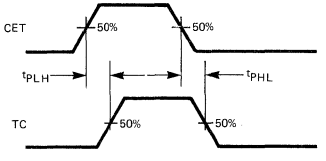
CONDITIONS: $\overline{PE}$ = $\overline{MR}$ = CEP = CET = H for 340160/340161 and $\overline{PE}$ = $\overline{SR}$ = CEP = CET = H for 340162/340163.

CLOCK (CP) TO TERMINAL COUNT (TC) PROPAGATION DELAYS



CONDITIONS: See the Terminal Count Generation Table. $\overline{PE}$ = CEP = CET = $\overline{MR}$ = H for 340160/340161 and $\overline{PE}$ = CEP = CET = $\overline{SR}$ = H for 340162/340163.

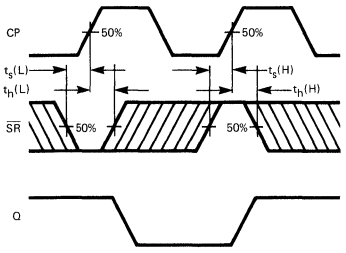
COUNT ENABLE TRICKLE INPUT (CET) TO TERMINAL COUNT OUTPUT (TC) PROPAGATION DELAYS



CONDITIONS: See the Terminal Count Generation Table. CP = $\overline{PE}$ = CEP = $\overline{MR}$ = H for 340160/340161 and CP = $\overline{PE}$ = CEP = $\overline{SR}$ = H for 340162/340163.

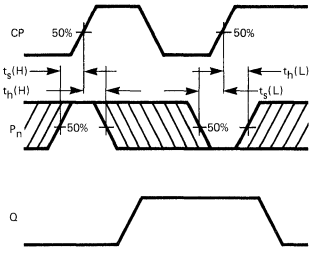
SWITCHING DIAGRAMS (Cont'd)

340162/340163
SET-UP TIMES (t_s) AND HOLD TIMES (t_h) FOR SYNCHRONOUS RESET ($\overline{SR}$)



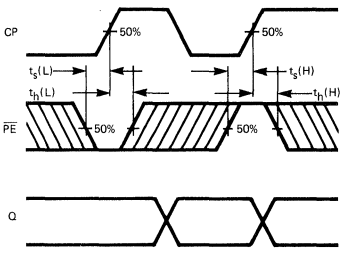
CONDITIONS: $\overline{PE}$ = L, P_0-P_3 = H.

SET-UP TIMES (t_s) AND HOLD TIMES (t_h) FOR PARALLEL DATA INPUTS (P_0-P_3).



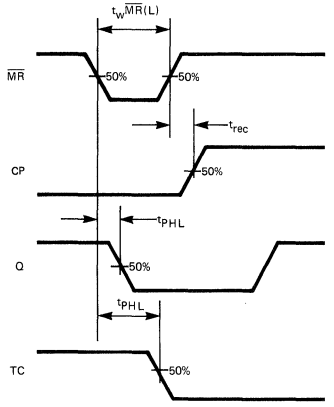
CONDITIONS: $\overline{PE}$ = L, $\overline{MR}$ = H for 340160/340161 and $\overline{PE}$ = L, $\overline{SR}$ = H for 340162/340163.

SET-UP TIMES (t_s) AND HOLD TIMES (t_h) FOR PARALLEL ENABLE INPUT $\overline{PE}$



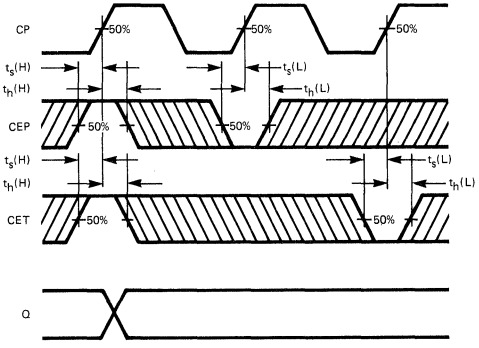
CONDITIONS: $\overline{MR}$ = H for 340160/340161 and $\overline{SR}$ = H for 340162/340163.

340160/340161
MASTER RESET ($\overline{MR}$) TO OUTPUT (Q) DELAY, MASTER RESET PULSE WIDTH, MASTER RESET RECOVERY TIME, AND MASTER RESET TO TERMINAL COUNT (TC) DELAY



CONDITIONS: $\overline{PE}$ = L and P_0 = P_1 = P_2 = P_3 = H.

SET-UP TIMES (t_s) AND HOLD TIMES (t_h) FOR COUNT ENABLE INPUTS (CEP AND CET)



CONDITIONS: $\overline{PE}$ = $\overline{MR}$ = H for 340160/340161 and $\overline{PE}$ = $\overline{SR}$ = H for 340162/340163.

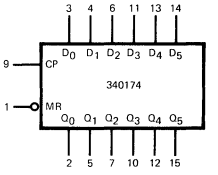
NOTE:
1. Set-up Times (t_s) and Hold Times (t_h) are shown as positive values, but may be specified as negative values.

340174
HEX D FLIP-FLOP

DESCRIPTION — The 340174 is a Hex Edge-Triggered D Flip-Flop with six Data Inputs (D_0-D_5), a Clock Input (CP) an overriding asynchronous Master Reset ($\overline{MR}$), and six Buffered Outputs (Q_0-Q_5).

Information on the Data Inputs (D_0-D_5) is transferred to the Buffered Outputs (Q_0-Q_5) on the LOW-to-HIGH transition of the Clock Input (CP) if the Master Reset Input ($\overline{MR}$) is HIGH. When LOW, the Master Reset Input ($\overline{MR}$) resets all flip-flops (Q_0-Q_5 = LOW) independent of the Clock (CP) and Data Inputs (D_0-D_5).

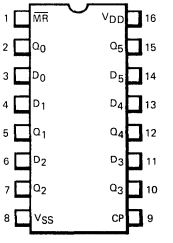
LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

- **TYPICAL CLOCK FREQUENCY OF 16 MHz AT V_{DD} = 10 V**
- **COMMON CLOCK TRIGGERED ON LOW-TO-HIGH TRANSITION**
- **COMMON ACTIVE LOW MASTER RESET**
- **FULLY EDGE-TRIGGERED CLOCK INPUT**

CONNECTION DIAGRAM
DIP (TOP VIEW)

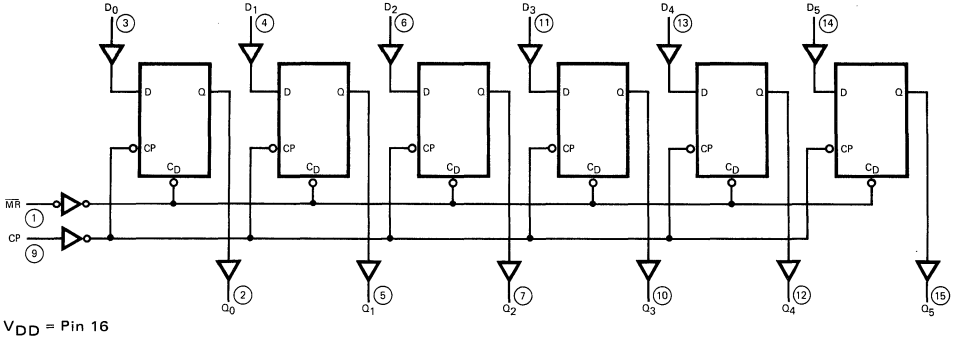


NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

D_0-D_5	Data Inputs
CP	Clock Input (L→H Edge-Triggered)
$\overline{MR}$	Master Reset Input (Active LOW)
Q_0-Q_5	Buffered Outputs from the Flip-Flops

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
◯ = Pin Number

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			20			40		8		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					200			400		80			MAX	
		XM			2			4		0.8		μA	MIN, 25°C	
					100			200		40			MAX	

NOTE: Additional DC Characteristics are listed in this section under 34000 Series CMOS Family Characteristics.

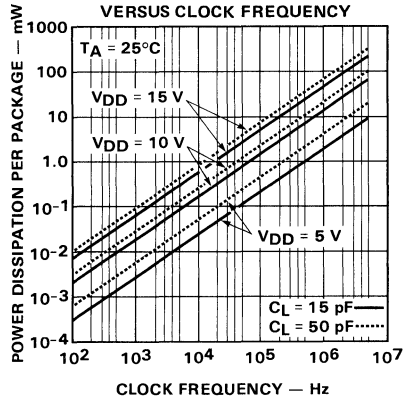
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, CP to Q_n		60	100		25	45		18		ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
t_{PHL}			60	100		25	45		18		ns	
t_{PHL}	Propagation Delay, $\overline{MR}$ to Q_n		65	105		30	50		20		ns	
t_{TLH}	Output Transition Time		35	75		20	40		10	25	ns	
t_{THL}			35	75		20	40		10	25	ns	
t_{PLH}	Propagation Delay, CP to Q_n		70	115		35	60		25		ns	C_L = 50 pF Input Transition Times ⩽ 20 ns
t_{PHL}			70	115		35	60		25		ns	
t_{PHL}	Propagation Delay, $\overline{MR}$ to Q_n		80	125		40	65		25		ns	
t_{TLH}	Output Transition Time		65	135		35	70		15	45	ns	
t_{THL}			65	135		35	70		15	45	ns	
t_wCP(L)	Minimum Clock Pulse Width	45	25		20	10			8		ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
$t_w\overline{MR}$(L)	Minimum $\overline{MR}$ Pulse Width	55	35		35	20			15		ns	
t_{rec}	$\overline{MR}$ Recovery Time	25	6		13	5			2		ns	
t_s	Set-Up Time, D_n to CP	5	1		5	1			0		ns	
t_h	Hold Time, D_n to CP	20	10		10	2			1		ns	
f_{MAX}	Maximum Clock Frequency (Note 3)	5	9		8	16					MHz	

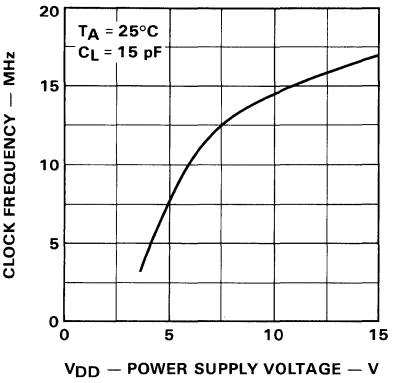
NOTES:
1. Propagation Delays and Output Transition Times are graphically described in this section under 34000 Series CMOS Family Characteristics.
2. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Set-up Times (t_s), Hold Times (t_h), Recovery Times (t_{rec}), and Minimum Pulse Widths (t_w) do not vary with load capacitance.
3. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
4. It is recommended that input rise and fall times to the Clock Input be less than 15 μs.

TYPICAL ELECTRICAL CHARACTERISTICS

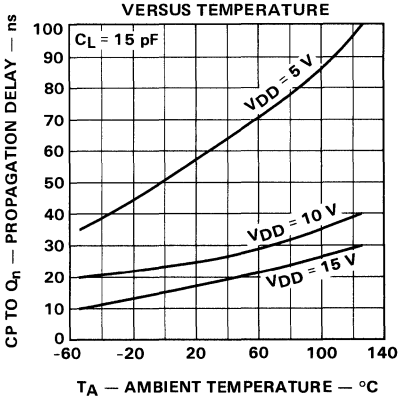
TYPICAL POWER DISSIPATION VERSUS CLOCK FREQUENCY



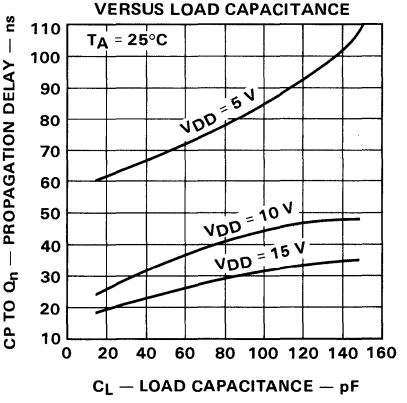
CLOCK FREQUENCY VERSUS POWER SUPPLY VOLTAGE



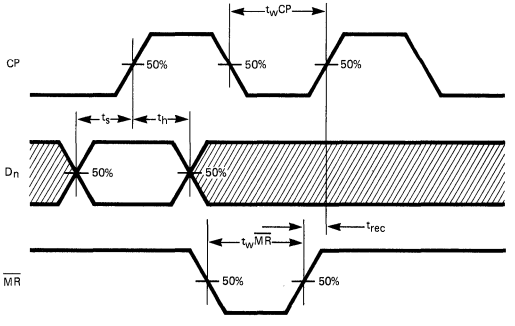
PROPAGATION DELAY VERSUS TEMPERATURE



PROPAGATION DELAY VERSUS LOAD CAPACITANCE



SWITCHING WAVEFORM



MINIMUM PULSE WIDTHS FOR CP AND $\overline{MR}$, $\overline{MR}$
RECOVERY TIME, AND SET-UP AND HOLD TIMES, D_n TO CP

NOTE: Set-up and Hold Times are shown as positive values but may be specified as negative values

340175
QUAD D FLIP-FLOP

DESCRIPTION — The 340175 is a Quad Edge-Triggered D Flip-Flop with four Data Inputs (D_0-D_3), a Clock Input (CP) an overriding asynchronous Master Reset ($\overline{MR}$), four Buffered Outputs (Q_0-Q_3) and four Complementary Buffered Outputs ($\overline{Q}_0$-$\overline{Q}_3$).

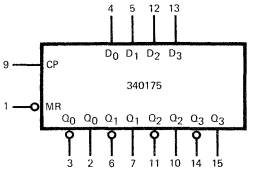
Information on the Data Inputs (D_0-D_3) is transferred to Outputs (Q_0-Q_3) on the LOW-to-HIGH Transition of the Clock Input (CP) if the Master Reset Input ($\overline{MR}$) is HIGH. When LOW, the Master Reset Input ($\overline{MR}$) resets all flip-flops (Q_0-Q_3 = LOW, $\overline{Q}_0$-$\overline{Q}_3$ = HIGH), independent of the Clock (CP) and Data (D_0-D_3) Inputs.

- **TYPICAL CLOCK FREQUENCY OF 16 MHz AT V_{DD} = 10 V**
- **COMMON CLOCK TRIGGERED ON LOW-TO-HIGH TRANSITION**
- **COMMON ACTIVE LOW MASTER RESET**
- **TRUE AND COMPLEMENTARY OUTPUTS AVAILABLE**
- **FULLY EDGE-TRIGGERED CLOCK INPUT**

PIN NAMES

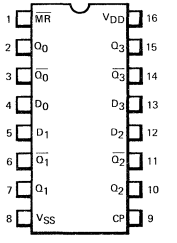
D_0-D_3	Data Inputs
CP	Clock Input (L→H Edge-Triggered)
$\overline{MR}$	Master Reset Input (Active LOW)
Q_0-Q_3	Buffered Outputs from the Flip-Flops
$\overline{Q}_0$-$\overline{Q}_3$	Complimentary Buffered Outputs from the Flip-Flops

LOGIC SYMBOL



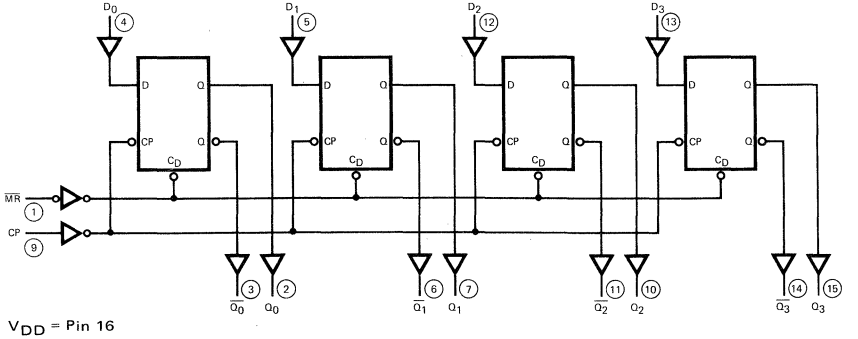
V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



Note: The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
◯ = Pin Number

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V

SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEMP	TEST CONDITIONS
I_{DD}	Quiescent Power Supply Current	XC		2			4			8		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
				20			40			80			MAX	
		XM		0.2			0.4			0.8		μA	MIN, 25°C	
				10			20			40			MAX	

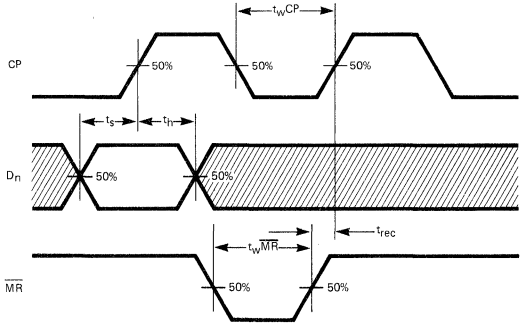
NOTE: Additional DC Characteristics are listed in this section under 34000 Series CMOS Family Characteristics.

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C

SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEST CONDITIONS
t_{PLH}	Propagation Delay, CP to Q_n or $\overline{Q_n}$		60			25			18		ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
t_{PHL}			60			25			18		ns	
t_{PLH}	Propagation Delay, $\overline{MR}$ to Q_n or $\overline{Q_n}$		65			30			20		ns	
t_{PHL}			65			30			20		ns	
t_{TLH}	Output Transition Time		35			20			10		ns	
t_{THL}			35			20			10		ns	
t_{PLH}	Propagation Delay, CP to Q_n or $\overline{Q_n}$		70			35			25		ns	C_L = 50 pF Input Transition Times ⩽ 20 ns
t_{PHL}			70			35			25		ns	
t_{PLH}	Propagation Delay, $\overline{MR}$ to Q_n or $\overline{Q_n}$		80			40			25		ns	
t_{PHL}			80			40			25		ns	
t_{TLH}	Output Transition Time		65			35			15		ns	
t_{THL}			65			35			15		ns	
t_wCP(L)	Minimum Clock Pulse Width		25			10			8		ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
$t_w\overline{MR}$(L)	Minimum $\overline{MR}$ Pulse Width		35			20			15		ns	
t_{rec}	$\overline{MR}$ Recovery Time		6			5			2		ns	
t_s	Set-Up Time, D_n to CP		1			1			0		ns	
t_h	Hold Time, D_n to CP		10			2			1		ns	
f_{MAX}	Maximum Clock Frequency (Note 3)		9			16					MHz	

NOTES:
1. Propagation Delays and Output Transition Times are graphically described in this section under 34000 Series CMOS Family Characteristics.
2. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Set-up Times (t_s), Hold Times (t_h), Recovery Times (t_{rec}), and Minimum Pulse Widths (t_w), do not vary with load capacitance.
3. For f_{MAX} input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
4. It is recommended that input rise and fall times to the Clock Input be less than 15 μs.

SWITCHING WAVEFORMS



MINIMUM PULSE WIDTHS FOR CP AND $\overline{MR}$, $\overline{MR}$ RECOVERY TIME, AND SET-UP AND HOLD TIMES, D_n TO CP

Note: Set-up and Hold Times are shown as positive values but may be specified as negative values.

340192 • 340193
4-BIT UP/DOWN DECADE AND BINARY COUNTER

DESCRIPTION — The 340192 is a 4-Bit Synchronous Up/Down BCD Decade Counter and the 340193 is a 4-Bit Synchronous Up/Down Binary Counter. Both operate the same except for the count sequence. Both counters have a Count Up Clock Input (CP_U), a Count Down Clock Input (CP_D), an asynchronous Parallel Load Input ($\overline{PL}$), four Parallel Data Inputs (P_0–P_3), an overriding asynchronous Master Reset (MR), four Counter Outputs (Q_0–Q_3), a Terminal Count Up (Carry) Output ($\overline{TC_U}$) and a Terminal Count Down (Borrow) Output ($\overline{TC_D}$).

When the Master Reset Input (MR) is LOW and the Parallel Load Input ($\overline{PL}$) is HIGH, the Counter Outputs change state on the LOW-to-HIGH transition of either Clock Input. However, for correct counting, both Clock Inputs cannot be LOW simultaneously. With the Master Reset Input (MR) LOW, information on the Parallel Data Inputs (P_0–P_3) is loaded into the counter when the Parallel Load Input ($\overline{PL}$) is LOW and stored in the counter when the Parallel Load Input ($\overline{PL}$) goes HIGH, independent of Clock Inputs (CP_U, CP_D). When HIGH, the Master Reset (MR) resets the counter independent of all other input conditions. See equations below for Terminal Count Outputs ($\overline{TC_U}$, $\overline{TC_D}$).

- **TYPICAL COUNT FREQUENCY OF 8 MHz AT V_{DD} = 10 V**
- **SYNCHRONOUS OPERATION**
- **INTERNAL CASCADING CIRCUITRY PROVIDED**
- **ACTIVE LOW PARALLEL LOAD**
- **ACTIVE HIGH ASYNCHRONOUS MASTER RESET**

PIN NAMES

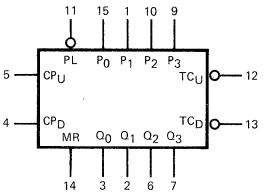
$\overline{PL}$	Parallel Load Input (Active LOW)
P_0–P_3	Parallel Data Inputs
CP_U	Count Up Clock Pulse Input (L→H Edge-Triggered)
CP_D	Count Down Clock Pulse Input (L→H Edge-Triggered)
MR	Master Reset Input (Asynchronous)
Q_0–Q_3	Buffered Counter Outputs
$\overline{TC_U}$	Buffered Terminal Count Up (Carry) Output (Active LOW)
$\overline{TC_D}$	Buffered Terminal Count Down (Borrow) Output (Active LOW)

MODE SELECTION
(Both Counters)

MR	$\overline{PL}$	CP_U	CP_D	MODE
H	X	X	X	Reset (Asyn.)
L	L	X	X	Preset (Asyn.)
L	H	H	H	No Change
L	H	⎍	H	Count Up
L	H	H	⎍	Count Down

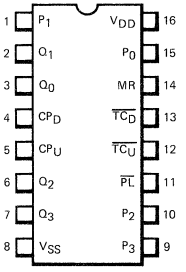
L = LOW Level
H = HIGH Level
X = Don't Care
⎍ = Positive-Going Clock Pulse Edge

LOGIC SYMBOL



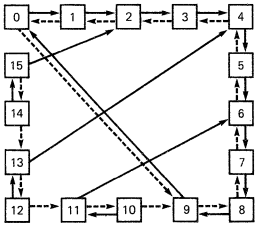
V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



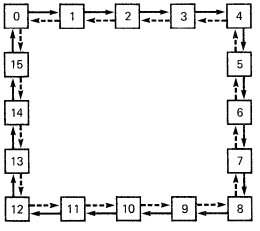
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

340192 STATE DIAGRAM



Count Up ————
Count Down ----------

340193 STATE DIAGRAM



340192 LOGIC EQUATIONS FOR TERMINAL COUNT

$TC_U = Q_0 \bullet Q_3 \bullet \overline{CP_U}$

$TC_D = \overline{Q_0} \bullet \overline{Q_1} \bullet \overline{Q_2} \bullet \overline{Q_3} \bullet \overline{CP_D}$

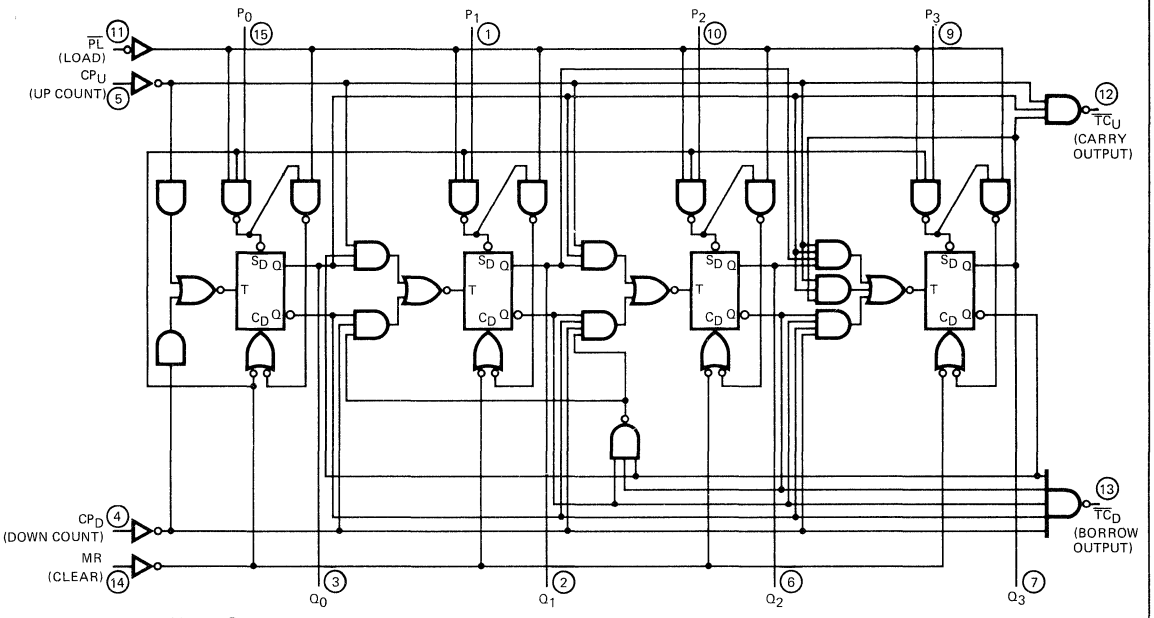
340193 LOGIC EQUATIONS FOR TERMINAL COUNT

$TC_U = Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3 \bullet \overline{CP_U}$

$TC_D = \overline{Q_0} \bullet \overline{Q_1} \bullet \overline{Q_2} \bullet \overline{Q_3} \bullet \overline{CP_D}$

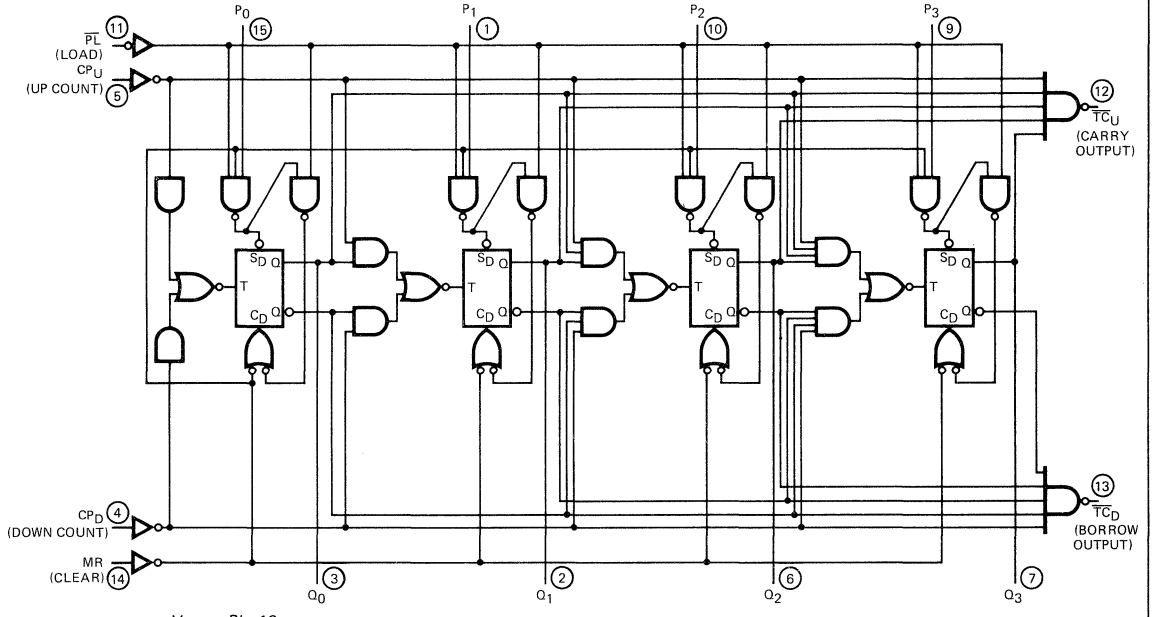
LOGIC DIAGRAMS

340192



V_{DD} = Pin 16
V_{SS} = Pin 8
◯ = Pin Number

340193



V_{DD} = Pin 16
V_{SS} = Pin 8
◯ = Pin Number

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V

SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEMP	TEST CONDITIONS
I_{DD}	Quiescent Power Supply Current	XC			50			100		20		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					700			1400		280			MAX	
		XM			15			25		5		μA	MIN, 25°C	
					900			1500		3000			MAX	

NOTE: Additional DC Characteristics are listed in this section under 34000 Series CMOS Family Characteristics.

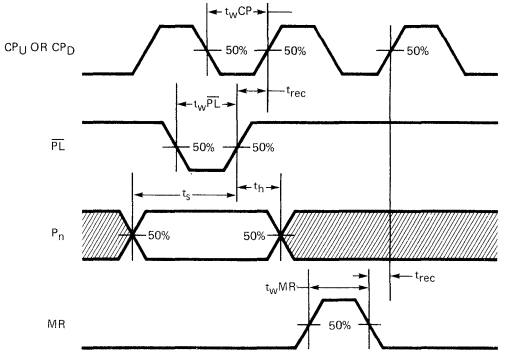
AC CHARACTERISTICS AND SWITCHING REQUIREMENTS:

SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEST CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay, CP_U to Q_n		225 225			95 95			65 65		ns ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
t_{PLH} t_{PHL}	Propagation Delay, CP_D to Q_n		225 225			95 95			65 65		ns ns	
t_{PLH} t_{PHL}	Propagation Delay, CP_U to $\overline{TC_U}$		110 110			50 50			35 35		ns ns	
t_{PLH} t_{PHL}	Propagation Delay, CP_D to $\overline{TC_D}$		125 125			50 50			35 35		ns ns	
t_{PHL}	Propagation Delay, MR to Q_n		250			110			75		ns	
t_{PLH}	Propagation Delay, MR to $\overline{TC_U}$ or $\overline{TC_D}$		350			150			100		ns	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{PL}$ to Q_n		250 250			100 100			65 65		ns ns	
t_{TLH} t_{THL}	Output Transition Time		35 35			20 20			15 15		ns ns	
t_{PLH} t_{PHL}	Propagation Delay, CP_U to Q_n		245 245			105 105			70 70		ns ns	C_L = 50 pF Input Transition Times ⩽ 20 ns
t_{PLH} t_{PHL}	Propagation Delay, CP_D to Q_n		245 245			105 105			70 70		ns ns	
t_{PLH} t_{PHL}	Propagation Delay, CP_U to $\overline{TC_U}$		130 130			60 60			40 40		ns ns	
t_{PLH} t_{PHL}	Propagation Delay, CP_D to $\overline{TC_D}$		145 145			60 60			40 40		ns ns	
t_{PHL}	Propagation Delay, MR to Q_n		270			120			80		ns	
t_{PLH}	Propagation Delay, MR to $\overline{TC_U}$ or $\overline{TC_D}$		370			170			105		ns	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{PL}$ to Q_n		270 270			110 110			70 70		ns ns	
t_{TLH} t_{THL}	Output Transition Time		55 55			30 30			20 20		ns ns	
t_wCP	Min. CP_U or CP_D Pulse Width		85			30			20		ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
t_wMR	Minimum MR Pulse Width		60			30			20		ns	
$t_w\overline{PL}$	Minimum $\overline{PL}$ Pulse Width		75			25			20		ns	
t_{rec}	MR Recovery Time		75			30			20		ns	
t_{rec}	$\overline{PL}$ Recovery Time		75			30			20		ns	
t_s t_h	Set-Up Time, P_n to $\overline{PL}$ Hold Time, P_n to $\overline{PL}$		85 -83			30 -28			20 -19		ns ns	
f_{MAX}	Input Count Frequency (Note 3)		4			8					MHz	

See note on following page.

NOTES:
1. Propagation Delays and Output Transition Times are graphically described in this section under 34000 Series CMOS Family Characteristics.
2. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Set-up Times (t_s), Hold Times (t_h), Recovery Times (t_{rec}), and Minimum Pulse Widths (t_w), do not vary with load capacitance.
3. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
4. It is recommended that input rise and fall times to the Clock Inputs (CP_U or CP_D) be less than 15 μs.

SWITCHING WAVEFORMS



RECOVERY TIMES FOR $\overline{PL}$ AND MR, MINIMUM PULSE WIDTHS FOR CP_U, CP_D, $\overline{PL}$ AND MR AND SET-UP AND HOLD TIMES P_n TO $\overline{PL}$

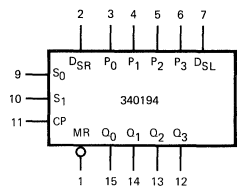
NOTE: Set-up and Hold Times are shown as positive values but may be specified as negative values.

340194
4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

DESCRIPTION — The 340194 is a 4-Bit Bidirectional Shift Register with two Mode Control Inputs (S_0, S_1), a Clock Input (CP), a Serial Data Shift Left Input (D_{SL}), a Serial Data Shift Right Input (D_{SR}), four Parallel Data Inputs (P_0-P_3), an overriding asynchronous Master Reset Input ($\overline{MR}$) and four Buffered Parallel Outputs (Q_0-Q_3).

When LOW, the Master Reset Input ($\overline{MR}$) resets all stages and forces all Outputs (Q_0-Q_3) LOW, overriding all other input conditions. When the Master Reset Input ($\overline{MR}$) is HIGH, the operating mode is controlled by the two Mode Control Inputs (S_0, S_1) as shown in the Truth Table. Serial and parallel operation is edge-triggered on the LOW-to-HIGH transition of the Clock Input (CP). The inputs at which the data is to be entered and the Mode Control Inputs (S_0, S_1) must be stable for a set-up time before the LOW-to-HIGH transition of the Clock Input CP).

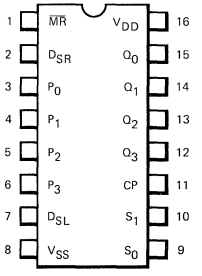
LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

- **TYPICAL SHIFT FREQUENCY OF 14 MHz AT V_{DD} = 10 V**
- **ASYNCHRONOUS MASTER RESET**
- **HOLD (DO NOTHING) MODE**
- **FULLY SYNCHRONOUS SERIAL OR PARALLEL DATA TRANSFERS**
- **POSITIVE EDGE-TRIGGERED CLOCK**

CONNECTION DIAGRAM
DIP (TOP VIEW)

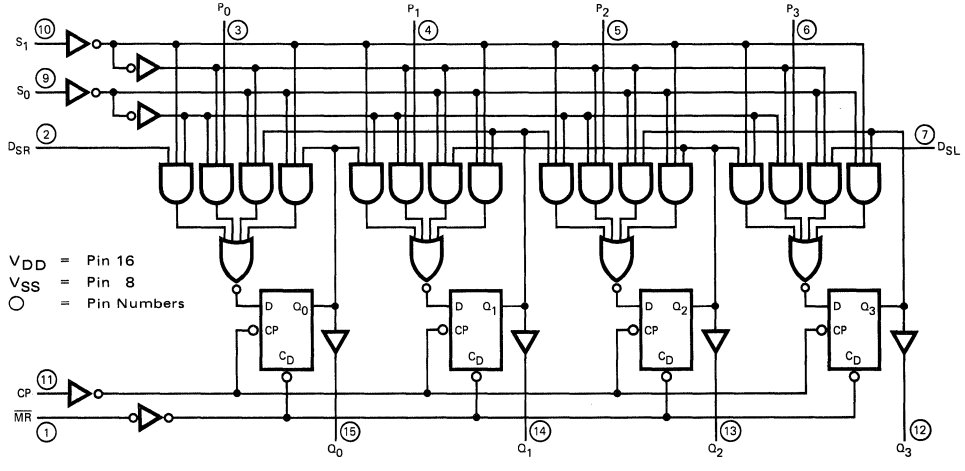


NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

S_0, S_1	Mode Control Inputs
P_0-P_3	Parallel Data Inputs
D_{SR}	Serial (Shift Right) Data Input
D_{SL}	Serial (Shift Left) Data Input
CP	Clock Input (L→H Edge-Triggered)
$\overline{MR}$	Master Reset Input (Active LOW)
Q_0-Q_3	Parallel Outputs

LOGIC DIAGRAM



TRUTH TABLE

OPERATING MODE	INPUTS ($\overline{MR}$ = H)					OUTPUTS AT t_{n+1}			
	S_1	S_0	D_{SR}	D_{SL}	P_0,P_1,P_2,P_3	Q_0	Q_1	Q_2	Q_3
Hold	L	L	X	X	X	Q_0	Q_1	Q_2	Q_3
Shift Left	H	L	X	L	X	Q_1	Q_2	Q_3	L
	H	L	X	H	X	Q_1	Q_2	Q_3	H
Shift Right	L	H	L	X	X	L	Q_0	Q_1	Q_2
	L	H	H	X	X	H	Q_0	Q_1	Q_2
Parallel Load	H	H	X	X	L	L	L	L	L
	H	H	X	X	H	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
(t_{n+1}) = Indicates state after next LOW-to-HIGH clock transition.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			50			100		20		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					500			1000		200			MAX	
		XM			5			10		2		μA	MIN, 25°C	
					40			80		16			MAX	

NOTE: Additional DC Characteristics are listed in this section under 34000 Series CMOS Family Characteristics.

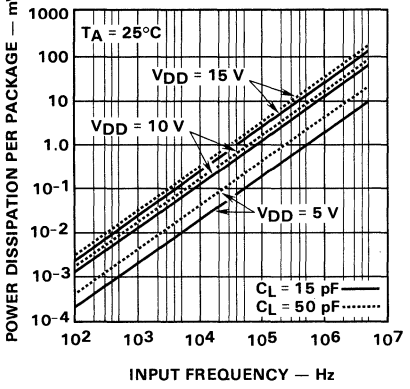
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay,		80	150		35	65		25		ns	
t_{PHL}	CP to Q		80	150		35	65		25		ns	C_L = 15 pF
t_{PHL}	Propagation Delay, $\overline{MR}$ to Q		80	150		35	65		25		ns	Input Transition
t_{THL}	Output Transition		40	75		20	40		15	25	ns	Times ⩽ 20 ns
t_{TLH}	Time		40	75		20	40		15	25	ns	
t_{PLH}	Propagation Delay,		100	180		45	80		35		ns	
t_{PHL}	CP to Q		100	180		45	80		35		ns	C_L = 50 pF
t_{PHL}	Propagation Delay, $\overline{MR}$ to Q		100	180		45	80		35		ns	Input Transition
t_{THL}	Output Transition		75	135		40	70		25	45	ns	Times ⩽ 20 ns
t_{TLH}	Time		75	135		40	70		25	45	ns	
t_s	Set-Up Time, $P_0 - P_3$, D_{SL}, D_{SR} to CP	80	40		40	20			15		ns	
t_h	Hold Time, $P_0 - P_3$, D_{SL}, D_{SR} to CP	0	-10		0	-5			-5		ns	
t_s	Set-Up Time, S to CP	100	60		50	30			20		ns	
t_h	Hold Time, S to CP	0	-10		0	-5			-5		ns	C_L = 15 pF
t_WCP(L)	Minimum Clock Pulse Width	100	60		60	35			25		ns	Input Transition
$t_W\overline{MR}$(L)	Minimum $\overline{MR}$ Pulse Width	75	40		45	25			15		ns	Times ⩽ 20 ns
t_{rec}	Recovery Time for $\overline{MR}$	180	100		90	50			35		ns	
f_{MAX}	Maximum CP Frequency (Note 3)	4.5	9		9	14					MHz	

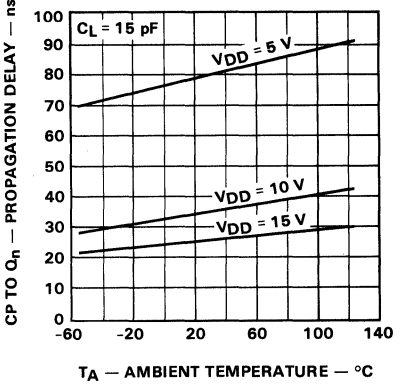
NOTES:
1. Propagation Delays and Output Transition Times are graphically described in this section under 34000 Series CMOS Family Characteristics.
2. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Set-up Times (t_s), Hold Times (t_h), Recovery Times (t_{rec}), and Minimum Pulse Widths (t_W) do not vary with load capacitance.
3. For f_{MAX} input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
4. It is recommended that input rise and fall times to the Clock Input be less than 15 μs.

TYPICAL ELECTRICAL CHARACTERISTICS

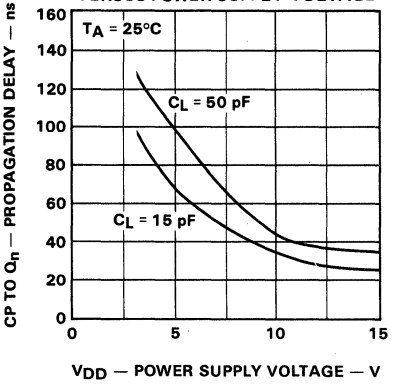
POWER DISSIPATION VERSUS FREQUENCY



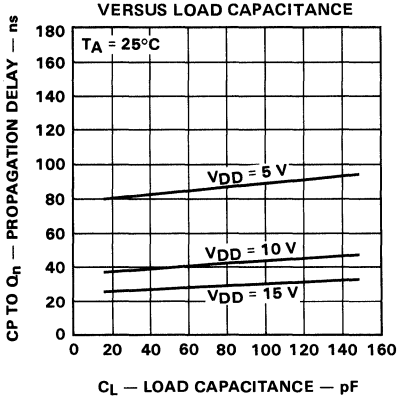
PROPAGATION DELAY VERSUS TEMPERATURE



PROPAGATION DELAY VERSUS POWER SUPPLY VOLTAGE

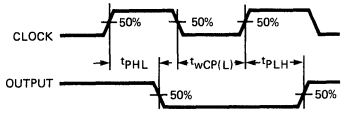


PROPAGATION DELAY VERSUS LOAD CAPACITANCE



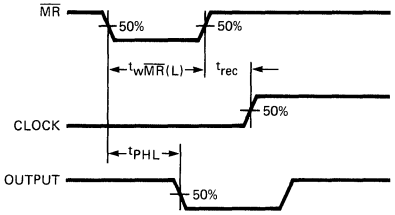
SWITCHING TIME WAVEFORMS

The shaded areas indicate when the input is permitted to change for predictable output performance.



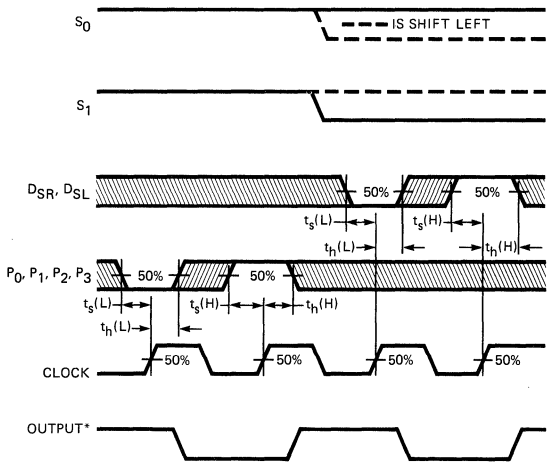
CLOCK TO OUTPUT DELAYS
CLOCK PULSE WIDTH

OTHER CONDITIONS: S_1 = L, $\overline{MR}$ = H, S_0 = H



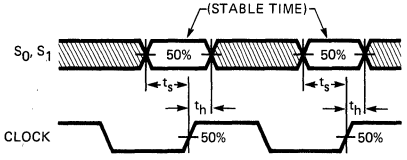
MASTER RESET PULSE WIDTH,
MASTER RESET TO OUTPUT DELAY AND
MASTER RESET TO CLOCK RECOVERY TIME

OTHER CONDITIONS: S_0, S_1 = H
$P_0 = P_1 = P_2 = P_3$ = H



SET-UP (t_s) AND HOLD (t_h) TIME FOR SERIAL DATA (D_{SR}, D_{SL}) AND PARALLEL DATA (P_0, P_1, P_2, P_3)

OTHER CONDITIONS: $\overline{MR}$ = H
*D_{SR} Set-up Time Affects Q_0 Only
D_{SL} Set-up Time Affects Q_3 Only



SET-UP (t_s) AND HOLD (t_h) TIME FOR S INPUT

OTHER CONDITIONS: $\overline{MR}$ = H

340195
4-BIT UNIVERSAL SHIFT REGISTER

DESCRIPTION — The 340195 is a fully synchronous edge-triggered 4-Bit Shift Register with a Clock Input (CP), four synchronous Parallel Data Inputs (P_0-P_3), two synchronous Serial Data Inputs (J, $\overline{K}$), a synchronous Mode Control Input ($\overline{PE}$), Buffered Outputs from all four bit positions (Q_0-Q_3), a Buffered Inverted Output from the last bit position ($\overline{Q}_3$) and an overriding asynchronous Master Reset Input ($\overline{MR}$).

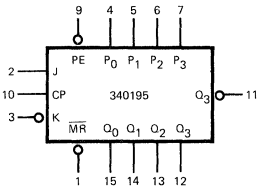
Operation is synchronous (except for Master Reset) and is edge-triggered on the LOW-to-HIGH transition of the Clock Input (CP). When the Mode Control Input ($\overline{PE}$) is LOW, a LOW-to-HIGH clock transition loads data into the register from Parallel Data Inputs (P_0-P_3). When the Mode Control Input ($\overline{PE}$) is HIGH, a LOW-to-HIGH clock transition shifts data into the first register position from the Serial Data Inputs (J, $\overline{K}$), and shifts all the data in the register one position to the right. D-type entry is obtained by tying the two Serial Data Inputs (J, $\overline{K}$) together. A LOW on the Master Reset Input ($\overline{MR}$) resets all four bit positions (Q_0-Q_3 = LOW, $\overline{Q}_3$ = HIGH) independent of all other input conditions.

- **TYPICAL SHIFT FREQUENCY OF 12 MHz AT V_{DD} = 10 V**
- **ASYNCHRONOUS MASTER RESET**
- **J, $\overline{K}$ INPUTS TO THE FIRST STAGE**
- **FULLY SYNCHRONOUS SERIAL OR PARALLEL DATA TRANSFERS**
- **COMPLEMENTARY OUTPUT FROM THE LAST STAGE**
- **POSITIVE EDGE-TRIGGERED CLOCK**

PIN NAMES

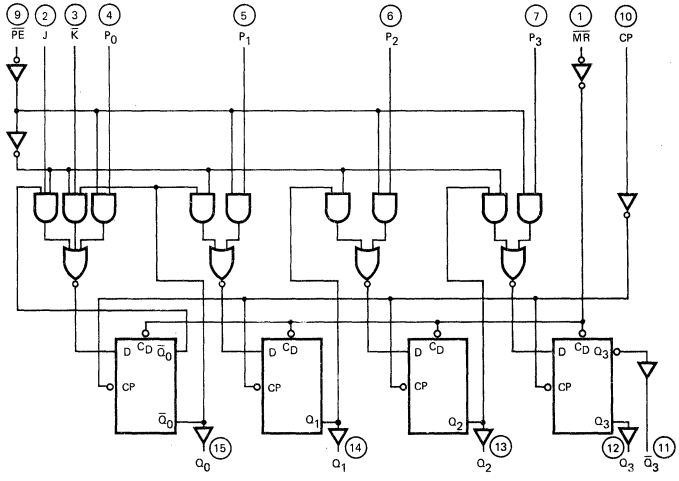
$\overline{PE}$	Parallel Enable Input (Active LOW)
P_0-P_3	Parallel Data Inputs
J	First Stage J Input (Active HIGH)
$\overline{K}$	First Stage K Input (Active LOW)
CP	Clock Input (L → H Edge-Triggered)
$\overline{MR}$	Master Reset Input (Active LOW)
Q_0-Q_3	Parallel Outputs
$\overline{Q}_3$	Complementary Last Stage Output

LOGIC SYMBOL



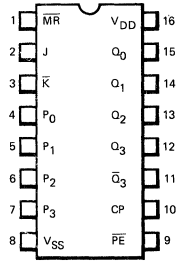
V_{DD} = Pin 16
V_{SS} = Pin 8

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Numbers

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

TRUTH TABLE

OPERATING MODE	INPUTS ($\overline{MR}$ = H)							OUTPUTS AT t_{n+1}				
	$\overline{PE}$	J	$\overline{K}$	P_0	P_1	P_2	P_3	Q_0	Q_1	Q_2	Q_3	$\overline{Q}_3$
Shift Mode	H	L	L	X	X	X	X	L	Q_0	Q_1	Q_2	$\overline{Q}_2$
	H	L	H	X	X	X	X	Q_0	Q_0	Q_1	Q_2	$\overline{Q}_2$
	H	H	L	X	X	X	X	$\overline{Q}_0$	Q_0	Q_1	Q_2	$\overline{Q}_2$
	H	H	H	X	X	X	X	H	Q_0	Q_1	Q_2	$\overline{Q}_2$
Parallel Entry Mode	L	X	X	L	L	L	L	L	L	L	L	H
	L	X	X	H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
(t_{n+1}) = Indicates state after next LOW to HIGH clock transition.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			50			100		20		μA	MIN, 25°C	Inputs at 0 V or V_{DD} per the Logic Function or Truth Table
					500			1000		200			MAX	
		XM			5			10		2		μA	MIN, 25°C	
					40			80		16			MAX	

NOTE: Additional DC Characteristics are listed in this section under 34000 Series CMOS Family Characteristics.

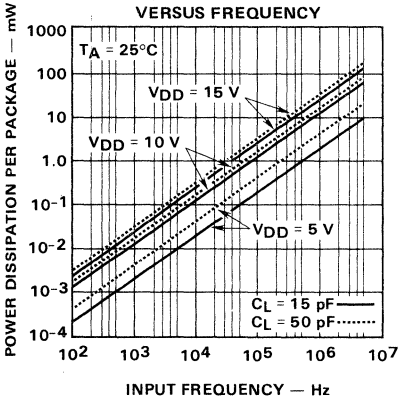
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, CP to Q_n		80	150		35	65				ns	C_L = 15 pF
t_{PHL}			80	150		35	65				ns	
t_{PHL}	Propagation Delay, MR to Q_3		80	150		35	65				ns	Input Transition
t_{PHL}	Propagation Delay, MR to Q_n		80	150		35	65				ns	Times ⩽ 20 ns
t_{THL}	Output Transition Time		40	70		20	35			25	ns	
t_{TLH}			40	70		20	35			25	ns	
t_{PLH}	Propagation Delay, CP to Q_n or Q_3		100	180		45	80				ns	C_L = 50 pF
t_{PHL}			100	180		45	80				ns	
t_{PHL}	Propagation Delay, MR to Q_3		100	180		45	80				ns	Input Transition
t_{PHL}	Propagation Delay, MR to Q_n		100	180		45	80				ns	Times ⩽ 20 ns
t_{THL}	Output Transition Time		75	135		40	70			45	ns	
t_{TLH}			75	135		40	70			45	ns	
t_s	Set-Up Time, J, K, P_0 – P_3 to CP	80	40		40	20		25			ns	
t_h	Hold Time, J, K, P_0 – P_3 to CP	0	-10		0	-5		0			ns	
t_s	Set-Up Time, PE to CP	100	60		50	30		35	20		ns	
t_h	Hold Time, PE to CP		0			0			0		ns	C_L = 15 pF
t_wCP(L)	Minimum Clock Pulse Width	100	60		60	35		40	25		ns	Input Transition
t_wMR(L)	Minimum MR Pulse Width	75	40		45	25		25	15		ns	Times ⩽ 20 ns
t_{rec}	Recovery Time for MR	180	100		90	50		60	35		ns	
f_{MAX}	Maximum CP Frequency (Note 3)	4.5	9		9	14					MHz	

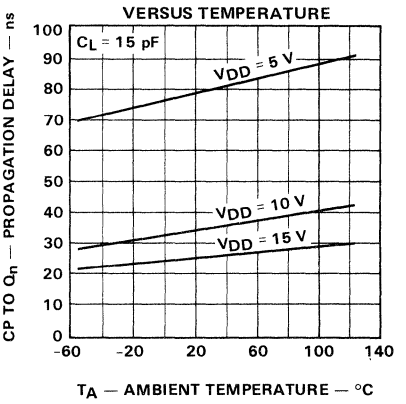
NOTES:
1. Propagation Delays and Output Transition Times are graphically described in this section under 34000 Series CMOS Family Characteristics.
2. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Set-up Times (t_s), Hold Times (t_h), Recovery Times (t_{rec}), and Minimum Pulse Widths (t_w), do not vary with load capacitance.
3. For f_{MAX} input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
4. It is recommended that input rise and fall times be less than 15 μs.

TYPICAL ELECTRICAL CHARACTERISTICS

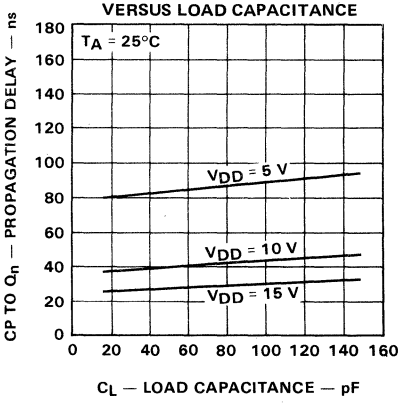
POWER DISSIPATION VERSUS FREQUENCY



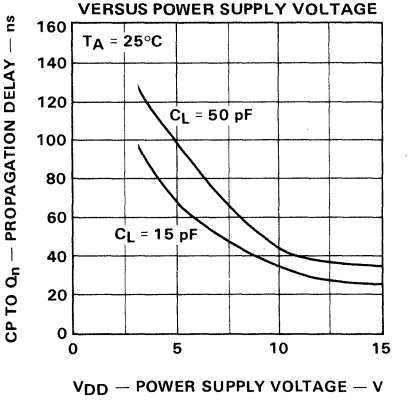
PROPAGATION DELAY VERSUS TEMPERATURE



PROPAGATION DELAY VERSUS LOAD CAPACITANCE



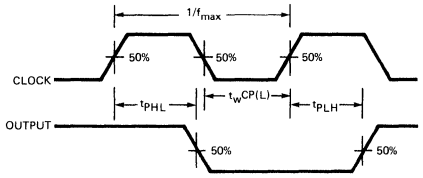
PROPAGATION DEALY VERSUS POWER SUPPLY VOLTAGE



SWITCHING TIME WAVEFORMS

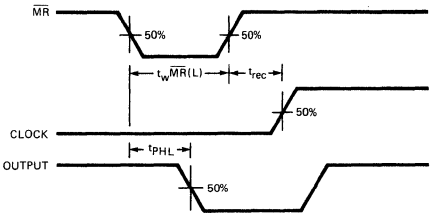
The shaded areas indicate when the input is permitted to change for predictable output performance.

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



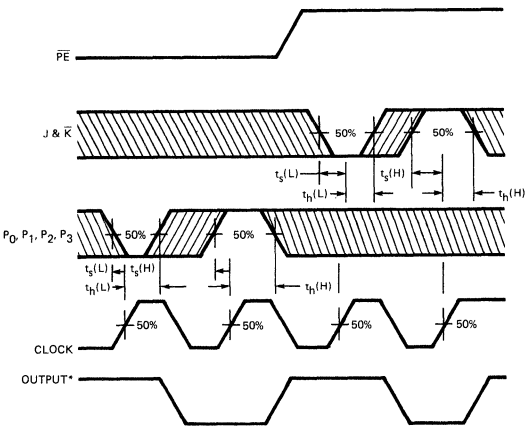
OTHER CONDITIONS: $J = \overline{PE} = \overline{MR} = H$
$\overline{K} = L$

MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY AND MASTER RESET TO CLOCK RECOVERY TIME



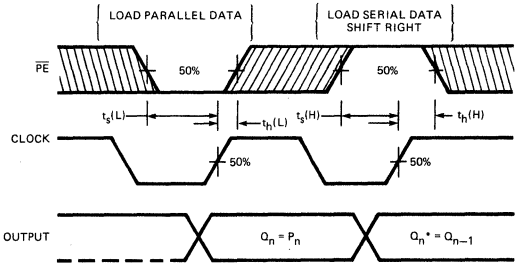
OTHER CONDITIONS: $\overline{PE} = L$
$P_0 = P_1 = P_2 = P_3 = H$

SET-UP (t_s) AND HOLD (t_h) TIME FOR SERIAL DATA (J & $\overline{K}$) AND PARALLEL DATA (P_0, P_1, P_2, P_3)



OTHER CONDITIONS: $\overline{MR} = H$
*J & $\overline{K}$ Set-up Time Affects Q_0 Only

SET-UP (t_s) AND HOLD (t_h) TIME FOR $\overline{PE}$ INPUT



OTHER CONDITIONS: $\overline{MR} = H$
*Q_0 State will be Determined by J & $\overline{K}$ Inputs

NUMERICAL INDEX OF PLANNED PRODUCTS

34006

18-STAGE STATIC SHIFT REGISTER

DESCRIPTION – The 34006 is an 18-Stage Shift Register arranged as two 4-stage and two 5-stage shift registers with a common Clock Input ($\overline{CP}$). The two 4-stage shift registers, each have a Data Input (D_a, D_b) and a Data Output (Q_{3a}, Q_{3b}); the two 5-stage shift registers each have a Data Input (D_c, D_d) and Data Outputs from the fourth and fifth stages (Q_{3c}, Q_{4c}, Q_{3d}, Q_{4d}).

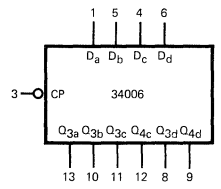
The registers can be operated in parallel or interconnected to form a single shift register of up to 18 bits. Data is shifted into the first register position of each register from the Data Inputs (D_a-D_d) and all the data in each register is shifted one position to the right on the HIGH-to-LOW transition of the Clock Input ($\overline{CP}$).

- **CLOCK EDGE-TRIGGERED ON A HIGH-TO-LOW TRANSITION**
- **CASCADABLE**
- **SERIAL-TO-SERIAL DATA TRANSFER**

PIN NAMES

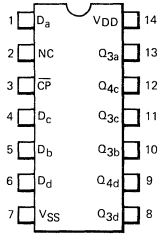
D_a-D_d	Data Inputs
$\overline{CP}$	Clock Input (H→L Edge-Triggered)
Q_{3a}-Q_{3d}, Q_{4c}, Q_{4d}	Data Outputs

LOGIC SYMBOL



V_{DD} = Pin 14
V_{SS} = Pin 7
NC = Pin 2

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE: The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

34007

DUAL COMPLEMENTARY PAIR PLUS INVERTER

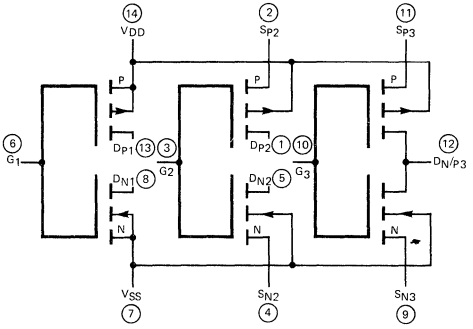
DESCRIPTION – The 34007 is a Dual Complementary Pair and an Inverter with access to each device. It has three n-channel and three p-channel enhancement mode MOS transistors. For proper operation $V_{SS} \leq V_I \leq V_{DD}$.

- **INPUT DIODE PROTECTION ON ALL INPUTS**
- **DRAINS AND SOURCES TO N- AND P-CHANNEL TRANSISTORS AVAILABLE**

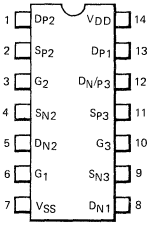
PIN NAMES

S_{P2}, S_{P3}	Source Connection to Second and Third p-channel Transistors
D_{P1}, D_{P2}	Drain Connection from the First and Second p-channel Transistors
D_{N1}, D_{N2}	Drain Connection from the First and Second n-channel Transistors
S_{N2}, S_{N3}	Source Connection to the Second and Third n-channel Transistors
$D_{N/P3}$	Common Connection to the Third p-channel and n-channel Transitor Drains
G_1-G_3	Gate Connection to n- and p-channel Transistors 1, 2 and 3

LOGIC SYMBOL



CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE: The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

4

34008

4-BIT BINARY FULL ADDER

DESCRIPTION – The 34008 is a 4-Bit Binary Full Adder with two 4-bit Data Inputs (A_0-A_3, B_0-B_3); a Carry Input (C_0), four Sum Outputs (S_0-S_3) and a Carry Output (C_4).

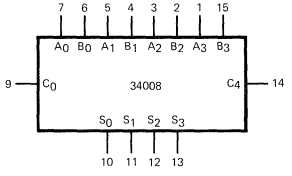
The 34008 uses full lookahead across 4-bits to generate the Carry Output (C_4). This minimizes the necessity for extensive "lookahead" and carry-cascading circuits.

- **CARRY LOOKAHEAD BUFFERED OUTPUT**
- **EASILY CASCADED**

PIN NAMES

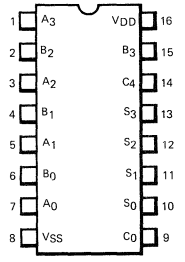
A_0-A_3, B_0-B_3	Data Inputs
C_0	Carry Input
S_0-S_3	Sum Outputs
C_4	Carry Output

LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP(TOP VIEW)



NOTE: The Flatpak version has the same pinouts(Connection Diagram) as the Dual In-Line Package.

34018

PRESETTABLE DIVIDE-BY-N COUNTER

DESCRIPTION – The 34018 is a 5-Stage Johnson Counter with a Clock Input (CP), a Data Input (D), an asynchronous Parallel Load Input (PL), five Parallel Inputs (P_0–P_4), five active LOW buffered Outputs ($\overline{Q}_0$–$\overline{Q}_4$) and an overriding asynchronous Master Reset Input (MR).

Information on the Parallel Inputs (P_0–P_4) is asynchronously loaded into the counter while the Parallel Load Input (PL) is HIGH, independent of the Clock (CP) and Data (D) Inputs. Data present in the counter is stored on the HIGH-to-LOW transition of the Parallel Load Input (PL). When the Parallel Load Input is LOW, the counter advances on the LOW-to-HIGH transition of the Clock Input (CP). By connecting the Outputs ($\overline{Q}_0$–$\overline{Q}_4$) to the Data Input (D), the counter operates as a divide-by-n counter ($2 \leqslant n \leqslant 10$); see below.

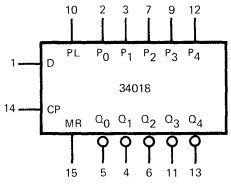
A HIGH on the Master Reset Input (MR) resets the counter ($\overline{Q}_0$–$\overline{Q}_4$ = HIGH) independent of all other inputs.

- **ASYNCHRONOUS MASTER RESET INPUT (ACTIVE HIGH)**
- **ACTIVE LOW FULLY BUFFERED DECODED OUTPUTS**
- **DIVIDE-BY-N WITH $2 \leqslant N \leqslant 10$**
- **CLOCK INPUT L→H EDGE-TRIGGERED**
- **ASYNCHRONOUS PARALLEL LOAD INPUT (ACTIVE HIGH)**

PIN NAMES

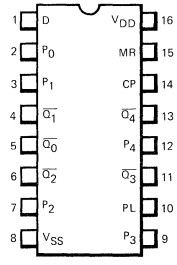
PL	Parallel Load Input
P_0–P_4	Parallel Inputs
D	Data Input
CP	Clock Input (L→H Edge-Triggered)
MR	Master Reset Input
$\overline{Q}_0$–$\overline{Q}_4$	Buffered Outputs (Active LOW)

LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE: The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

DIVIDE-BY-N MODE SELECTION

DIVIDE BY	D INPUT
2	$\overline{Q}_0$
3	$\overline{Q}_0 \cdot \overline{Q}_1$
4	$\overline{Q}_1$
5	$\overline{Q}_1 \cdot \overline{Q}_2$
6	$\overline{Q}_2$
7	$\overline{Q}_2 \cdot \overline{Q}_3$
8	$\overline{Q}_3$
9	$\overline{Q}_3 \cdot \overline{Q}_4$
10	$\overline{Q}_4$

34022
4-STAGE DIVIDE-BY-8 JOHNSON COUNTER

DESCRIPTION – The 34022 is a 4-Stage Divide-by-8 Johnson Counter with eight glitch free active HIGH Decoded Outputs (O_0–O_7), an active LOW Output from the most significant flip-flop ($\overline{Q_{4-7}}$), an active HIGH and an active LOW Clock Input (CP_0, $\overline{CP_1}$) and an overriding asynchronous Master Reset Input (MR).

The counter is advanced by either a LOW-to-HIGH transition at CP_0 while $\overline{CP_1}$ is LOW or a HIGH-to-LOW transition at $\overline{CP_1}$ while CP_0 is HIGH (see Functional Truth Table). When cascading the counters, the $\overline{Q_{4-7}}$ Output (which is LOW while the counter is in states 4, 5, 6 and 7) can be used to drive the CP_0 Input of the next 34022. A HIGH on the Master Reset Input (MR) resets the counter to Zero (O_0 = $\overline{Q_{4-7}}$ = HIGH, O_1– O_7 = LOW) independent of the Clock Inputs (CP_0, $\overline{CP_1}$).

- **CLOCK EDGE-TRIGGERED ON EITHER A LOW-TO-HIGH TRANSITION OR A HIGH-TO-LOW TRANSITION**
- **BUFFERED CARRY OUTPUT ($\overline{Q_{4-7}}$) AVAILABLE FOR CASCADING**
- **BUFFERED FULLY DECODED OUTPUTS**

PIN NAMES

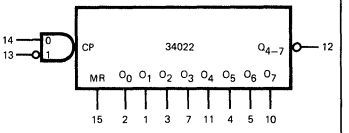
CP_0	Clock Input (L→H Edge-Triggered)
$\overline{CP_1}$	Clock Input (H→L Edge-Triggered)
MR	Master Reset Input
O_0–O_7	Decoded Outputs
$\overline{Q_{4-7}}$	Carry Output (Active LOW)

FUNCTIONAL TRUTH TABLE

MR	CP_0	$\overline{CP_1}$	OPERATION
H	X	X	O_0 = $\overline{Q_{4-7}}$ = H; O_1–O_7 = L
L	H	H→L	Counter Advances
L	L→H	L	Counter Advances
L	L	X	No Change
L	X	H	No Change
L	H	L→H	No Change
L	H→L	L	No Change

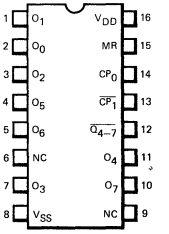
H = HIGH Level
L = LOW Level
L→H = LOW-to-HIGH Transition
H→L = HIGH-to-LOW Transition
X = Don't Care

LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8
NC = Pin 6, 9

CONNECTION DIAGRAM
DIP(TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

34031

64-STAGE STATIC SHIFT REGISTER

DESCRIPTION – The 34031 is an edge-triggered 64-Stage Static Shift Register with two Serial Data Inputs (D_0, D_1) a Data Select Input (S), a Clock Input (CP), a buffered Clock Output (CO) and buffered Outputs from the 64th bit position (Q_{63}, $\overline{Q}_{63}$).

Data from the selected Data Inputs (D_0 or D_1), as determined by the state of the Select Input (S), is shifted into the first shift register position and all the data in the register is shifted one position to the right on the LOW-to-HIGH transition of the Clock Input (CP). D_0 is selected by a LOW on the Select Input (S) and D_1 is selected by a HIGH on the Select Input (S).

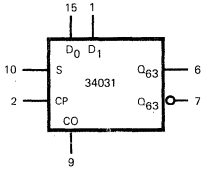
Registers can be cascaded either by connecting all the Clock Inputs (CP) together or by driving the Clock Input (CP) of the right-most register with the system clock and connecting the Clock Output (CO) to the Clock Input (CP) of the preceding register. When the second technique is used in the recirculating mode, a flip-flop must be used to store the Output (Q_{63}) of the right-most register until the left-most register is clocked.

- **CLOCK INPUT IS L→H EDGE-TRIGGERED**
- **DATA SELECT INPUT (S) ALLOWS DATA INPUT AT EITHER D_0 OR D_1 INPUTS**
- **EASILY CASCADED**
- **TRUE AND COMPLEMENTARY BUFFERED OUTPUTS AVAILABLE FROM 64TH STAGE**

PIN NAMES

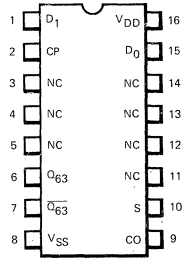
D_0, D_1	Data Inputs
S	Data Select Input
CP	Clock Input (L→H Edge-Triggered)
CO	Buffered Clock Output
Q_{63}	Buffered Output from the 64th Stage
$\overline{Q}_{63}$	Complementary Buffered Output from the 64th Stage

LOGIC SYMBOL



V_{DD} = Pin 16 V_{SS} = Pin 8
NC = Pins 3,4,5,11,12,13,14

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE: The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

34041

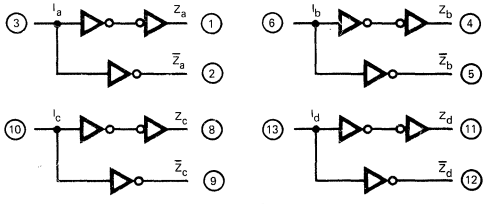
QUAD TRUE/COMPLEMENT BUFFER

DESCRIPTION – The 34041 is a Quad True/Complement Buffer which provides both an inverted active LOW Output ($\overline{Z}$) and a non-inverted active HIGH Output (Z) for each Input (I).

PIN NAMES

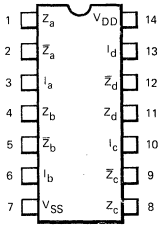
I_a, I_b, I_c, I_d	Buffer Input
Z_a, Z_b, Z_c, Z_d	Buffered True Output
$\overline{Z}_a$, $\overline{Z}_b$, $\overline{Z}_c$, $\overline{Z}_d$	Buffered Complementary Output

LOGIC DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE: The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

34043

QUAD R/S LATCH WITH 3-STATE OUTPUTS

DESCRIPTION — The 34043 is a Quad R/S Latch with 3-State Outputs with a common Output Enable Input (EO). Each latch has an active HIGH Set Input (S_n), an active HIGH Reset Input (R_n) and an active HIGH 3-State Output (Q_n).

When the Output Enable Input (EO) is HIGH, the state of the Latch Outputs (Q_n) can be determined from the Truth Table (see below). When the Output Enable Input (EO) is LOW, the Latch Outputs are in the high impedance OFF state. The Output Enable Input (EO) does not affect the state of the latch.

- **3-STATE BUFFERED OUTPUTS (ACTIVE HIGH)**
- **COMMON OUTPUT ENABLE**
- **SET INPUTS TO EACH LATCH (ACTIVE HIGH)**
- **RESET INPUTS TO EACH LATCH (ACTIVE HIGH)**

PIN NAMES

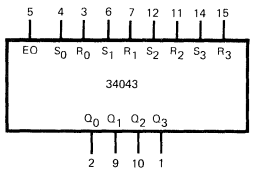
EO	Common Output Enable Input
S_0–S_3	Set Inputs
R_0–R_3	Reset Inputs
Q_0–Q_3	3-State Buffered Latch Outputs

TRUTH TABLE

INPUTS			OUTPUT (Q_n)
EO	S_n	R_n	
L	X	X	High Impedance
H	H	L	H
H	L	H	L
H	H	H	H
H	L	L	No Change

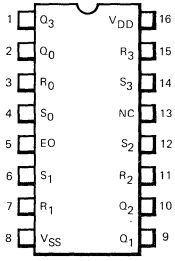
H = HIGH Level, L = LOW Level, X = Don't Care

LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8
NC = Pin 13

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE: The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

34044

QUAD R/S LATCH WITH 3-STATE OUTPUTS

DESCRIPTION — The 34044 is a Quad R/S Latch with 3-State Outputs with a common Output Enable Input (EO). Each latch has an active LOW Set Input ($\overline{S_n}$), an active LOW Reset Input ($\overline{R_n}$) and an active HIGH 3-State Output (Q_n).

When the Output Enable Input (EO) is HIGH, the state of the Latch Outputs (Q_n) can be determined from the Truth Table (see below). When the Output Enable Input (EO) is LOW, the Latch Outputs are in the high impedance OFF state. The Output Enable Input (EO) does not affect the state of the latch.

- **3-STATE BUFFERED OUTPUTS (ACTIVE HIGH)**
- **COMMON OUTPUT ENABLE**
- **SET INPUTS TO EACH LATCH (ACTIVE LOW)**
- **RESET INPUTS TO EACH LATCH (ACTIVE LOW)**

PIN NAMES

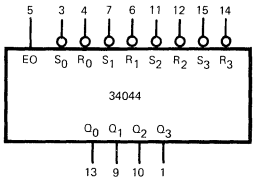
EO	Output Enable Input
$\overline{S_0}$–$\overline{S_3}$	Set Inputs (Active LOW)
$\overline{R_0}$–$\overline{R_3}$	Reset Inputs (Active LOW)
Q_0–Q_3	3-State Buffered Latch Outputs

TRUTH TABLE

INPUTS			OUTPUT (Q_n)
EO	$\overline{S}_n$	$\overline{R}_n$	
L	X	X	High Impedance
H	L	H	H
H	H	L	L
H	L	L	L
H	H	H	No Change

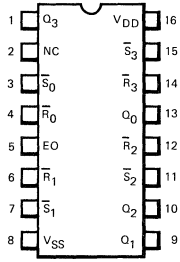
H = HIGH Level, L = LOW Level, X = Don't Care

LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8
NC = Pin 2

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE: The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

4

34046
MICROPOWER PHASE-LOCKED LOOP

DESCRIPTION – The 34046 is a Micropower Phase-Locked Loop consisting of a low power linear Voltage-Controlled Oscillator, a Source Follower Circuit, two different Phase Comparators, and a Zener diode. The Voltage-Controlled Oscillator has two External Capacitor connections (C_{exta}, C_{extb}), two External Resistor connections (R_{exta}, R_{extb}), a Voltage-Controlled Oscillator Input (I_{VCO}) and a Voltage-Controlled Oscillator Output (O_{VCO}). The Source Follower Circuit provides a Demodulated Output (O_D) from the Voltage-Controlled Oscillator. An active LOW Enable Input ($\overline{E}$) common to both the Voltage-Controlled Oscillator and the Source Follower Circuit is also provided. Phase Comparator I and Phase Comparator II have common Signal (I_S) and Comparator (I_C) Inputs and separate outputs; Phase Comparator I Output (O_{PCI}), Phase Comparator II Output (O_{PCII}), and Phase Pulse Output (O_{PII}). An input to the Zener diode (I_Z) is also provided.

The Voltage-Controlled Oscillator requires one external capacitor (C_1) and one external resistor (R_1) to determine operational frequency range. A second external resistor (R_2) may be used to allow frequency offset. External resistor R_3 and external capacitor C_2 combined serve as a low pass filter to the Voltage-Controlled Oscillator Input (I_{VCO}). Output O_D is provided to avoid loading the low pass filter. External resistor R_4 is required if this output is utilized. O_D must be left open when not utilized. The output from the Voltage-Controlled Oscillator (O_{VCO}) may be connected directly or indirectly through CMOS frequency dividers (i.e., the 34018, 34020, 34022, 34024, 34029, 34040, 34518, 34520, 340160, 340161, 340162, 340163, 340192, or 340193) to the Comparator Input (I_C). With the Enable Input ($\overline{E}$) HIGH both the Voltage-Controlled Oscillator and the Source Follower Circuit are OFF to minimize power consumption. With $\overline{E}$ LOW, both are enabled.

For direct-coupling between O_{VCO} and I_C, the voltage swing at the Voltage-Controlled Oscillator Output (O_{VCO}) must be within standard CMOS logic levels ($V_{OH} \geq 0.7 \times V_{DD}$ and $V_{OL} \leq 0.3 \times V_{DD}$); otherwise the signal from O_{VCO} must be capacitively coupled to the Signal Input (I_S).

Phase Comparator I is an Exclusive OR circuit ($I_D \oplus I_S$). I_C and I_S must have 50% duty cycles to maximize lock range. When the Output of Phase Comparator I (O_{PCI}) is connected back to the Voltage-Controlled Oscillator through the low pass filter network, an averaged voltage to I_{VCO} forces oscillation at a center frequency.

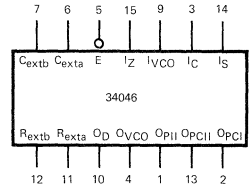
Phase Comparator II is an edge-triggered digital memory network with four flip-flop stages, associated control circuitry and a 3-state output. Phase Comparator II triggers on LOW-to-HIGH transitions at the Signal (I_S) and Comparator (I_C) Inputs and is independent of duty cycle at these inputs. The Output of Phase Comparator II (O_{PCII}) provides voltage levels and duty cycles corresponding to frequency and phase differentials between I_C and I_S. When O_{PCII} is connected to the Voltage-Controlled Oscillator Input (I_{VCO}) through the low pass filter network, a corresponding voltage across capacitor C_2 is adjusted until the Signal (I_S) and Comparator (I_C) Inputs are equal in both frequency and phase. At this point Phase Comparator II maintains a constant voltage across Capacitor C_2. When this stability has been established, the Phase Pulse Output (O_{PII}) is HIGH indicating a locked condition. Power dissipation in the low pass filter is reduced when Phase Comparator II is used.

A 5.2 V, on chip zener diode is provided for regulating the power supply voltage, if necessary.

- **CHOICE OF 2-PHASE COMPARATORS**
- **ENABLE INPUT (ACTIVE LOW) FOR LOW POWER DISSIPATION IN STANDBY MODE**
- **ON-CHIP ZENER DIODE FOR SUPPLY REGULATION**

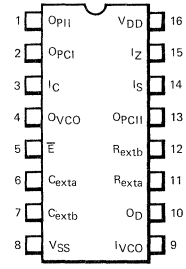
PIN NAMES	FUNCTION
I_Z	Zener Diode Input
I_S	Signal Input
I_C	Comparator Input
I_{VCO}	Voltage-Controlled Oscillator Input
$\overline{E}$	Enable Input (Active LOW)
C_{exta}, C_{extb}	External Capacitor Connections
R_{exta}, R_{extb}	External Resistor Connections
O_{PCI}	Phase Comparator I Output
O_{PCII}	Phase Comparator II Output
O_{PII}	Phase Pulse Output
O_D	Demodulator Output
O_{VCO}	Voltage-Controlled Oscillator Output

LOGIC SYMBOL



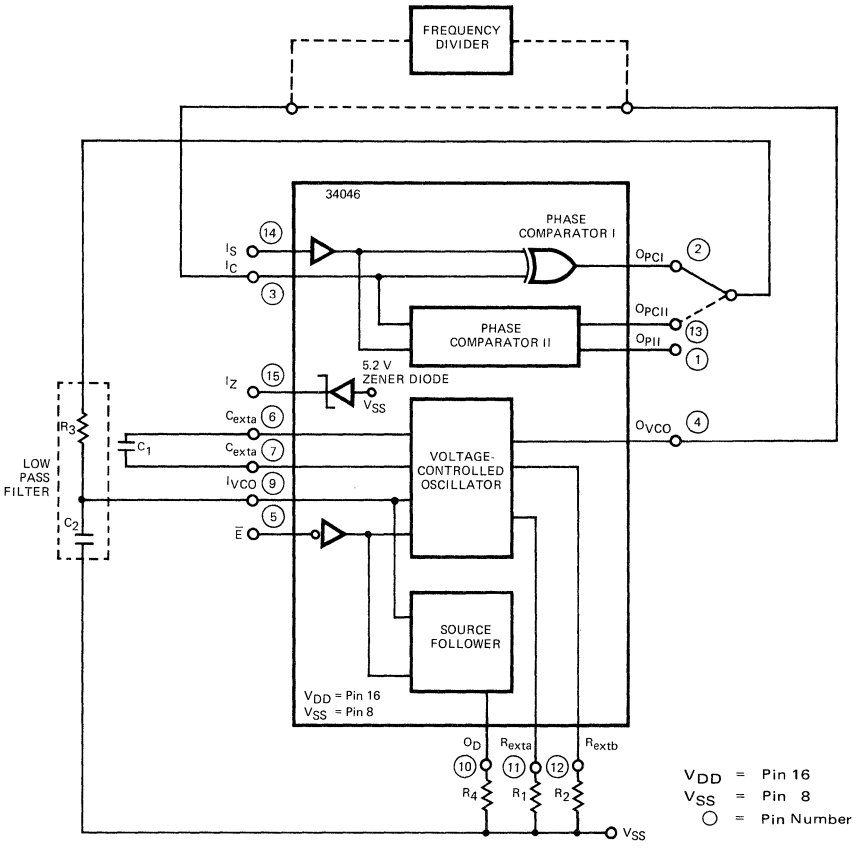
V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

BLOCK DIAGRAM



34047

MONOSTABLE/ASTABLE MULTIVIBRATOR

DESCRIPTION — The 34047 is a Monostable/Astable Multivibrator capable of operating in either the monostable or astable mode. Operation in either mode requires an external capacitor (C_x) between pins 1 and 3 (C_{ext},R_{ext}/C_{ext}) and an external resistor (R_x) between pins 2 and 3 (R_{ext},R_{ext}/C_{ext}). These external timing components (R_x,C_x) determine the output pulse width in the monostable mode and the output frequency in the astable mode. The 34047 also has active HIGH and active LOW astable mode Enable Inputs (E_{A0},$\overline{E}_{A1}$), active HIGH and active LOW Trigger Inputs (T_0,$\overline{T}_1$) for operation in the monostable mode, a Retrigger Input (I_{RT}), an Oscillator Output (O), active HIGH and active LOW flip-flop Outputs (Q,$\overline{Q}$) and an overriding asynchronous Master Reset Input (MR).

ASTABLE OPERATION. Astable operation is obtained by either a HIGH on the E_{A0} input or a LOW on the $\overline{E}_{A1}$ input. The frequency of the 50% duty cycle output at the Q and $\overline{Q}$ outputs is determined by the external timing components (R_x,C_x). A frequency twice that of the Q and $\overline{Q}$ outputs is available at the Oscillator Output (O). However, a 50% duty cycle is not guaranteed. The 34047 can be used as a gated oscillator by controlling the E_{A0} and $\overline{E}_{A1}$ inputs.

MONOSTABLE OPERATION. Monostable operation is obtained by connecting the E_{A0} input LOW and the $\overline{E}_{A1}$ input HIGH. The device can be triggered by either a LOW-to-HIGH transition at the T_0 input while the $\overline{T}_1$ input is LOW or a HIGH-to-LOW transition at the $\overline{T}_1$ input while the T_0 is HIGH. The output pulse width at Q and $\overline{Q}$ is determined by the external timing components (R_x,C_x). The device can be retriggered by applying a simultaneous LOW-to-HIGH transition to both the Retrigger Input (I_{RT}) and the T_0 input while the $\overline{T}_1$ input is LOW.

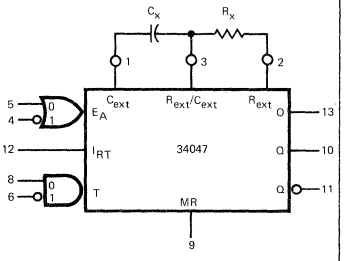
A HIGH on the Master Reset Input (MR) resets the output flip-flop (Q = LOW,$\overline{Q}$ =HIGH) independent of all other input conditions.

- **MONOSTABLE OR ASTABLE OPERATION**
- **TRUE AND COMPLEMENTARY BUFFERED OUTPUTS**
- **ENABLED WITH EITHER A LOW OR A HIGH LEVEL IN THE ASTABLE MODE**
- **TRIGGERED ON EITHER A LOW-TO-HIGH OR A HIGH-TO-LOW TRANSITION IN THE MONOSTABLE MODE**
- **ASYNCHRONOUS MASTER RESET**

PIN NAMES

C_{ext}	External Capacitor Connection
R_{ext}	External Resistor Connection
R_{ext}/C_{ext}	Common External Capacitor and Resistor Connection
I_{RT}	Retrigger Input
T_0	Trigger Input (L → H Triggered)
$\overline{T}_1$	Trigger Input (H → L Triggered)
E_{A0}	Enable Input (Active HIGH)
$\overline{E}_{A1}$	Enable Input (Active LOW)
MR	Master Reset
O	Oscillator Output
Q,$\overline{Q}$	True and Complementary Buffered Outputs

LOGIC SYMBOL



V_{DD} = Pin 14
V_{SS} = Pin 7

CONNECTION DIAGRAM
DIP (TOP VIEW)

NOTE: The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

34053
TRIPLE 2-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

DESCRIPTION — The 34053 is a Triple 2-Channel Analog Multiplexer/Demultiplexer with a common Enable Input ($\overline{E}$). Each Multiplexer/Demultiplexer has two Independent Inputs/Outputs (Y_0,Y_1), a Common Input/Output (Z), and a Select Input (S). Each multiplexer/demultiplexer contains two bidirectional analog switches, each with one side connected to an Independent Input/Output (Y_0,Y_1) and the other side connected to a Common Input/Output (Z). With the Enable Input ($\overline{E}$) LOW, one of the two switches is selected (low impedance, ON state) by the Select Input (S). With the Enable Input ($\overline{E}$) HIGH, all switches are in the high impedance OFF state, independent of the Select Inputs (S_a-S_c).

V_{DD} and V_{SS} are the two supply voltage connections for the Digital Control Inputs (S_a-S_c,$\overline{E}$). Their voltage limits are the same as for all other digital CMOS. The analog Inputs/Outputs (Y_0,Y_1,Z) can swing between V_{DD} as a positive limit and V_{EE} as a negative limit. V_{DD}-V_{EE} may not exceed 15 V. For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to V_{SS} (typically ground).

- **ANALOG OR DIGITAL MULTIPLEXER/DEMULTIPLEXER**
- **COMMON ENABLE INPUT (ACTIVE LOW)**

PIN NAMES

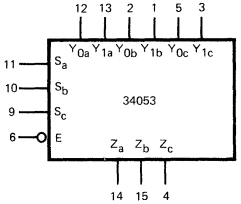
Y_{0a}-Y_{0c}, Y_{1a}-Y_{1c}	Independent Input/Outputs
S_a-S_c	Select Inputs
$\overline{E}$	Enable Input (Active LOW)
Z_a-Z_c	Common Input/Outputs

TRUTH TABLE

INPUTS		CHANNELS	
$\overline{E}$	S	Y_0-Z	Y_1-Z
L	L	ON	OFF
L	H	OFF	ON
H	X	OFF	OFF

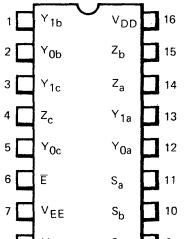
H = HIGH Level
L = LOW Level
X = Don't Care

LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8
V_{EE} = Pin 7

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE: The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

34067

16-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

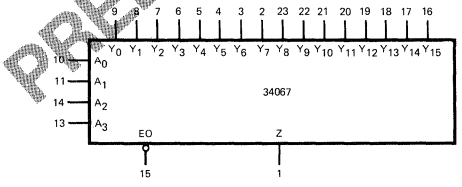
DESCRIPTION – The 34067 is a 16-Channel Analog Multiplexer/Demultiplexer with four Address Inputs (A_0-A_3), 16 Independent Inputs/Outputs (Y_0-Y_{15}), an active LOW Output Enable input ($\overline{EO}$), and a Common Input/Output (Z). The 34067 contains 16 bidirectional analog switches, each with one side connected to an Independent Input/Output (Y_0-Y_{15}) and the other side connected to a Common Input/Output (Z). One of the 16 switches is selected (low impedance, ON state) by the four Address Inputs (A_0-A_3) when the Output Enable input ($\overline{EO}$) is LOW. All unselected switches are in the high impedance OFF state. With the Output Enable input ($\overline{EO}$) HIGH, all 16 switches are in the high impedance OFF state. The Analog Input/Outputs (Y_0-Y_{15},Z) can swing between V_{DD} and V_{SS}. V_{DD}-V_{SS} may not exceed 15 V.

- **ANALOG OR DIGITAL MULTIPLEXER/DEMULTIPLEXER**
- **24-PIN PACKAGE**
- **SINGLE POWER SUPPLY**

PIN NAMES

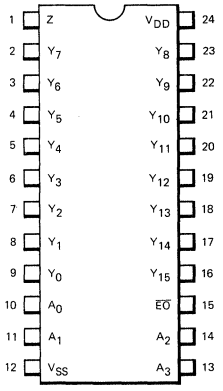
Y_0–Y_{15}	Independent Inputs/Outputs
A_0–A_3	Address Inputs
Z	Common Input/Output
$\overline{EO}$	Output Enable Input (Active LOW)

LOGIC SYMBOL



V_{DD} = Pin 24
V_{SS} = Pin 12

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE: The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

TRUTH TABLE

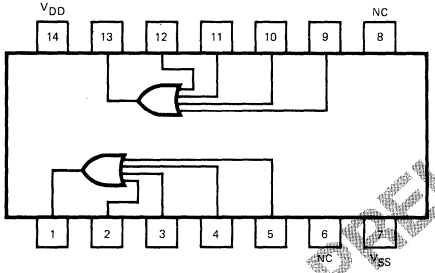
INPUTS				CHANNEL															
A_3	A_2	A_1	A_0	Y_0-Z	Y_1-Z	Y_2-Z	Y_3-Z	Y_4-Z	Y_5-Z	Y_6-Z	Y_7-Z	Y_8-Z	Y_9-Z	Y_{10}-Z	Y_{11}-Z	Y_{12}-Z	Y_{13}-Z	Y_{14}-Z	Y_{15}-Z
L	L	L	L	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
L	L	L	H	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
L	L	H	L	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
L	L	H	H	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
L	H	L	L	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
L	H	L	H	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
L	H	H	L	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
L	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
H	L	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF
H	L	L	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF
H	L	H	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF
H	L	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF
H	H	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF
H	H	L	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF
H	H	H	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF
H	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON

L = LOW Level H = HIGH Level $\overline{EO}$ = LOW Level

34072

DUAL 4-INPUT OR GATE

DESCRIPTION – This CMOS logic element provides the positive Dual 4-Input OR function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

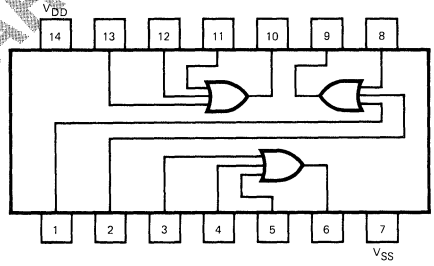


NOTE: The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

34075

TRIPLE 3-INPUT OR GATE

DESCRIPTION – This CMOS logic element provides the positive Triple 3-Input OR function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

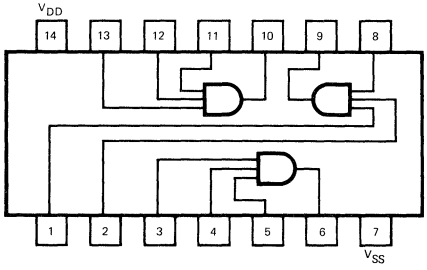


NOTE: The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

34073

TRIPLE 3-INPUT AND GATE

DESCRIPTION – This CMOS logic element provides the positive Triple 3-Input AND function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

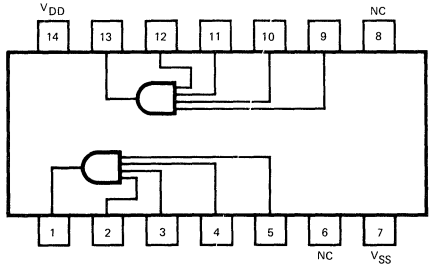


NOTE: The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

34082

DUAL 4-INPUT AND GATE

DESCRIPTION – This CMOS logic element provides the positive Dual 4-Input AND function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.



NOTE: The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

34510
UP/DOWN DECADE COUNTER

DESCRIPTION — The 34510 is an Edge-Triggered Synchronous Up/Down BCD Counter with a Clock Input ($\overline{CP}$), an active HIGH Up/Down Count Control Input (Up/$\overline{Dn}$), an active LOW Count Enable Input ($\overline{CE}$), an asynchronous active HIGH Parallel Load Input (PL), four Parallel Inputs (P_0-P_3), four Parallel Outputs (Q_0-Q_3), an active LOW Terminal Count Output ($\overline{TC}$) and an overriding asynchronous Master Reset Input (MR).

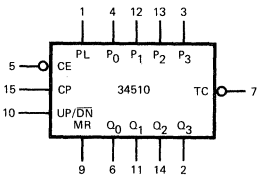
Information on the Parallel Inputs (P_0-P_3) is loaded into the counter while the Parallel Load Input (PL) is HIGH, independent of all other input conditions except the Master Reset Input (MR) which must be LOW. With the Parallel Load Input (PL) LOW, the counter changes on the LOW-to-HIGH transition of the Clock Input (CP) if the Count Enable Input ($\overline{CE}$) is LOW. The Up/Down Count Control Input (Up/$\overline{Dn}$) determines the direction of the count, HIGH for counting up, LOW for counting down. When counting up, the Terminal Count Output ($\overline{TC}$) is LOW when the Parallel Outputs (Q_0-Q_3) are HIGH and the Count Enable ($\overline{CE}$) is LOW. When counting down, the Terminal Count Output ($\overline{TC}$) is LOW when all the Parallel Outputs (Q_0-Q_3) and the Count Enable Input ($\overline{CE}$) are LOW. A HIGH on the Master Reset Input resets the counter (Q_0-Q_3 = LOW) independent of all other input conditions.

- **UP/DOWN COUNT CONTROL**
- **SINGLE CLOCK INPUT (L→H EDGE-TRIGGERED)**
- **ASYNCHRONOUS PARALLEL LOAD INPUT**
- **ASYNCHRONOUS MASTER RESET**
- **EASILY CASCADABLE**

PIN NAMES

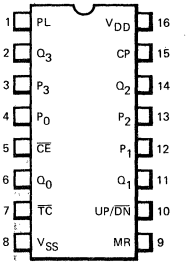
PL	Parallel Load Input (Active HIGH)
P_0-P_3	Parallel Inputs
$\overline{CE}$	Count Enable Input (Active LOW)
CP	Clock Pulse Input (L→H Edge-Triggered)
Up/$\overline{Dn}$	Up/Down Count Control Input
$\overline{TC}$	Terminal Count Output (Active LOW)
Q_0-Q_3	Parallel Outputs
MR	Master Reset Input

LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

34511
BCD-TO-7 SEGMENT LATCH/DECODER/DRIVER

DESCRIPTION — The 34511 is a BCD-to-7-Segment Latch/Decoder/Driver with four Address Inputs (A_0-A_3), an active LOW Latch Enable Input ($\overline{EL}$), an active LOW Ripple Blanking Input ($\overline{I_B}$), an active LOW Lamp Test Input ($\overline{I_{LT}}$) and seven active HIGH NPN bipolar segment outputs (a-g).

When the Latch Enable Input ($\overline{EL}$) is LOW, the state of the Segment Outputs (a-g) is determined by the data on the Address Inputs (A_0-A_3). When the Latch Enable Input ($\overline{EL}$) goes HIGH, the last data present at the Address Inputs (A_0-A_3) is stored in the latches and the Segment Outputs (a-g) remain stable.

When the Lamp Test Input ($\overline{I_{LT}}$) is LOW, all the Segment Outputs (a-g) are HIGH independent of all other input conditions. With the Lamp Test Input ($\overline{I_{LT}}$) HIGH, a LOW on the Ripple Blanking Input ($\overline{I_B}$) forces all Outputs (a-g) LOW. The Lamp Test Input ($\overline{I_{LT}}$) and the Ripple Blanking Input ($\overline{I_B}$) do not affect the latch circuit.

- **HIGH CURRENT SOURCING OUTPUTS (UP TO 25 mA)**
- **BLANKING INPUT (ACTIVE LOW)**
- **LAMP TEST INPUT (ACTIVE LOW)**
- **LAMP INTENSITY MODULATION CAPABILITY**
- **MULTIPLEXING CAPABILITY**

PIN NAMES

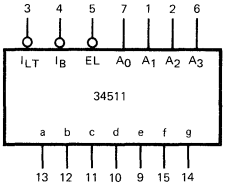
A_0-A_3	Address (Data) Inputs
$\overline{EL}$	Latch Enable Input (Active LOW)
$\overline{I_B}$	Ripple Blanking Input (Active LOW)
$\overline{I_{LT}}$	Lamp Test Input (Active LOW)
a-g	Segment Outputs

TRUTH TABLE

INPUTS							OUTPUTS							
$\overline{EL}$	$\overline{I_B}$	$\overline{I_{LT}}$	A_3	A_2	A_1	A_0	a	b	c	d	e	f	g	DISPLAY
X	X	L	X	X	X	X	H	H	H	H	H	H	H	8
X	L	H	X	X	X	X	L	L	L	L	L	L	L	BLANK
L	H	H	L	L	L	L	H	H	H	H	H	H	L	0
L	H	H	L	L	L	H	L	H	H	L	L	L	L	1
L	H	H	L	L	H	L	H	H	L	H	H	L	H	2
L	H	H	L	L	H	H	H	H	H	H	L	L	H	3
L	H	H	L	H	L	L	L	H	H	L	L	H	H	4
L	H	H	L	H	L	H	H	L	H	H	L	H	H	5
L	H	H	L	H	H	L	L	L	H	H	H	H	H	6
L	H	H	L	H	H	H	H	H	H	L	L	L	L	7
L	H	H	H	L	L	L	H	H	H	H	H	H	H	8
L	H	H	H	L	L	H	H	H	H	L	L	H	H	9
L	H	H	H	L	H	L	L	L	L	L	L	L	L	BLANK
L	H	H	H	L	H	H	L	L	L	L	L	L	L	BLANK
L	H	H	H	H	L	L	L	L	L	L	L	L	L	BLANK
L	H	H	H	H	L	H	L	L	L	L	L	L	L	BLANK
L	H	H	H	H	H	L	L	L	L	L	L	L	L	BLANK
L	H	H	H	H	H	H	L	L	L	L	L	L	L	BLANK
H	H	H	X	X	X	X				*				*

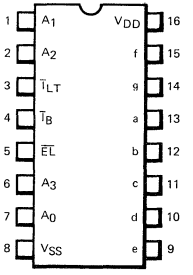
H = HIGH Level
L = LOW Level
X = Don't Care
* = Depends upon the BCD code applied during the LOW-to-HIGH transition of $\overline{EL}$.

LOGIC SYMBOL



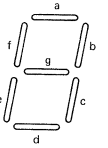
V_{DD} = Pin 16
V_{SS} = Pin 8

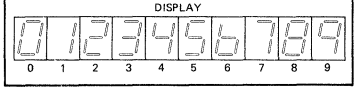
CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

NUMERICAL DESIGNATIONS





34514
1-OF-16 DECODER/DEMULTIPLEXER WITH INPUT LATCH

DESCRIPTION – The 34514 is a 1-of-16 Decoder/Demultiplexer with four binary weighted Address Inputs (A_0-A_3), a Latch Enable Input (EL), an active LOW Enable Input ($\overline{E}$) and sixteen mutually exclusive active HIGH Outputs (O_0-O_{15}).

When the Latch Enable Input (EL) is HIGH, the selected Output (O_0-O_{15}) is determined by the data on the Address Inputs (A_0-A_3). When the Latch Enable Input (EL) goes LOW, the last data present at the Address inputs (A_0-A_3) is stored in the latches and the Outputs (O_0-O_{15}) remain stable. When the Enable Input ($\overline{E}$) is LOW, the selected Output (O_0-O_{15}), determined by the contents of the latch, is HIGH. When the Enable Input ($\overline{E}$) is HIGH, all Outputs (O_0-O_{15}) are LOW. The Enable Input ($\overline{E}$) does not affect the state of the latch.

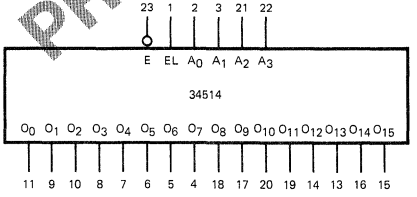
With the Latch Enable Input (EL) HIGH, 16-channel demultiplexing results when data is applied to the Enable Input ($\overline{E}$) and the desired output is selected by A_0-A_3. The selected output (O_0-O_{15}) will follow as the inverse of the data. All unselected outputs (O_0-O_{15}) are LOW.

- **LATCH ENABLE INPUT (ACTIVE HIGH)**
- **ENABLE INPUT (ACTIVE LOW)**
- **SELECTED BUFFERED OUTPUTS (ACTIVE HIGH) COMPLEMENT OF THE INPUT**

PIN NAMES

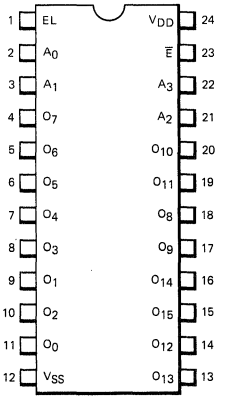
A_0-A_3	Address Inputs
$\overline{E}$	Enable Input (Active LOW)
EL	Latch Enable Input
O_0-O_{15}	Outputs

LOGIC SYMBOL



V_{DD} = Pin 24
V_{SS} = Pin 12

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

TRUTH TABLE

INPUTS					OUTPUTS														
$\overline{E}$	A_0	A_1	A_2	A_3	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7	O_8	O_9	O_{10}	O_{11}	O_{12}	O_{13}	O_{14}	O_{15}
H	X	X	X	X	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	H	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	H	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L
L	H	H	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	H	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L
L	H	L	H	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L
L	L	H	H	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L
L	H	H	H	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L
L	L	L	L	H	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L
L	H	L	L	H	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L
L	L	H	L	H	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L
L	H	H	L	H	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L
L	L	L	H	H	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L
L	H	L	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L
L	L	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L
L	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H

H = HIGH Level
L = LOW Level
EL = HIGH

34515

1-OF-16 DECODER/DEMULTIPLEXER WITH INPUT LATCH

DESCRIPTION — The 34515 is a 1-of-16 Decoder/Demultiplexer with four binary weighted Address Inputs (A_0-A_3), a Latch Enable Input (EL), an active LOW Enable Input ($\overline{E}$) and sixteen mutually exclusive active LOW Outputs ($\overline{O_0}$-$\overline{O_{15}}$).

When the Latch Enable Input (EL) is HIGH, the selected Output ($\overline{O_0}$-$\overline{O_{15}}$) is determined by the data on the Address Inputs (A_0-A_3). When the Latch Enable Input (EL) goes LOW, the last data present at the Address Inputs (A_0-A_3) is stored in the latches and the Outputs ($\overline{O_0}$-$\overline{O_{15}}$) remain stable. When the Enable Input ($\overline{E}$) is LOW, the selected Output ($\overline{O_0}$-$\overline{O_{15}}$), determined by the contents of the latch, is LOW. When the Enable Input ($\overline{E}$) is HIGH, all Outputs ($\overline{O_0}$-$\overline{O_{15}}$) are HIGH. The Enable Input ($\overline{E}$) does not affect the state of the latch.

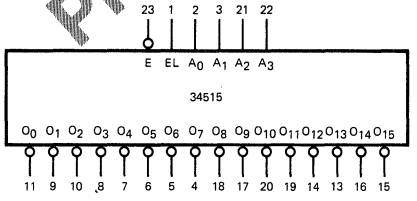
With the Latch Enable Input (EL) HIGH, 16-channel demultiplexing results when data is applied to the Enable Input ($\overline{E}$) and the desired output is selected by A_0-A_3. The selected Output ($\overline{O_0}$-$\overline{O_{15}}$) will follow the data at the Enable Input ($\overline{E}$). All unselected outputs ($\overline{O_0}$-$\overline{O_{15}}$) are HIGH.

- **LATCH ENABLE INPUT (ACTIVE HIGH)**
- **ENABLE INPUT (ACTIVE LOW)**
- **BUFFERED OUTPUTS (ACTIVE LOW)**

PIN NAMES

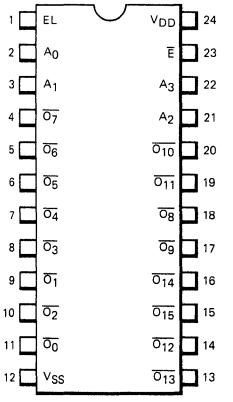
A_0-A_3	Address Inputs
$\overline{E}$	Enable Input (Active LOW)
EL	Latch Enable Input
$\overline{O_0}$-$\overline{O_{15}}$	Outputs (Active LOW)

LOGIC SYMBOL



V_{DD} = Pin 24
V_{SS} = Pin 12

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

TRUTH TABLE

INPUTS					OUTPUTS														
$\overline{E}$	A_0	A_1	A_2	A_3	$\overline{O_0}$	$\overline{O_1}$	$\overline{O_2}$	$\overline{O_3}$	$\overline{O_4}$	$\overline{O_5}$	$\overline{O_6}$	$\overline{O_7}$	$\overline{O_8}$	$\overline{O_9}$	$\overline{O_{10}}$	$\overline{O_{11}}$	$\overline{O_{12}}$	$\overline{O_{13}}$	$\overline{O_{14}}$	$\overline{O_{15}}$
H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	H	H	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	H	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	H	H	H	L	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Level
L = LOW Level
EL = HIGH

34516

UP/DOWN COUNTER

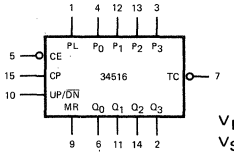
DESCRIPTION — The 34516 is an edge-triggered synchronous Up/Down 4-Bit Binary Counter with a Clock Input (CP), an active HIGH Count Up/Down Control Input (Up/$\overline{Dn}$), an active LOW Count Enable Input ($\overline{CE}$), an asynchronous active HIGH Parallel Load Input (PL), four Parallel Inputs (P_0–P_3), four Parallel Outputs (Q_0–Q_3), an active LOW Terminal Count Output ($\overline{TC}$) and an overriding asynchronous Master Reset Input (MR).

Information on the Parallel Inputs (P_0-P_3) is loaded into the counter while the Parallel Load Input (PL) is HIGH, independent of all other input conditions except the Master Reset Input (MR) which must be LOW. When the Parallel Load Input (PL) and the Count Enable Input ($\overline{CE}$) are LOW, the counter changes on the LOW-to-HIGH transition of the Clock Input (CP). The Count Up/Down Control Input (Up/Dn) determines the direction of the count, HIGH for counting up, LOW for counting down. When counting up, the Terminal Count Output ($\overline{TC}$) is LOW when $Q_0 = Q_1 = Q_2 = Q_3$ = HIGH and $\overline{CE}$ = LOW. When counting down the Terminal Count Output ($\overline{TC}$) is LOW when $Q_0 = Q_1 = Q_2 = Q_3$ = LOW and the $\overline{CE}$ = LOW. A HIGH on the Master Reset Input (MR) resets the counter ($Q_0 = Q_1 = Q_2 = Q_3$ = LOW) independent of all other input conditions.

- **UP/DOWN COUNT CONTROL**
- **SINGLE CLOCK INPUT (L→H EDGE-TRIGGERED)**
- **ASYNCHRONOUS PARALLEL LOAD INPUT**
- **ASYNCHRONOUS MASTER RESET**

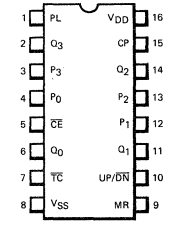
PIN NAMES	FUNCTION
PL	Parallel Load Input (Active HIGH)
P_0–P_3	Parallel Inputs
$\overline{CE}$	Count Enable Input (Active LOW)
CP	Clock Pulse Input (L→H Edge-Triggered)
Up/$\overline{Dn}$	Up/Down Count Control Input
$\overline{TC}$	Terminal Count Output (Active LOW)
Q_0–Q_3	Parallel Outputs
MR	Master Reset Input

LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

34519

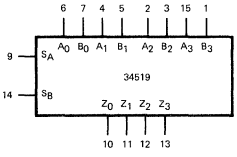
QUAD 2-INPUT MULTIPLEXER

DESCRIPTION — The 34519 provides four multiplexing circuits with common selection inputs; each circuit contains two inputs and one output. It may be used to select four bits of information from one of two sources. The A inputs are selected when S_A is HIGH, the B inputs when S_B is HIGH. When S_A and S_B are HIGH, the output (Z_a) is the logical Exclusive-NOR of the A_n and B_n inputs ($Z_n = A_n \odot B_n$). When S_A and S_B are LOW, the output (Z_n) is LOW, independent of the multiplexer inputs (A_n and B_n). The 34519 cannot be used to multiplex analog signals. The outputs utilize standard buffers for best performance.

- **COMMON SELECT INPUTS**
- **FULLY BUFFERED OUTPUTS**

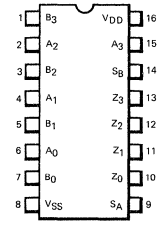
PIN NAMES	FUNCTION
S_A, S_B	Select Inputs (Active HIGH)
A_0–A_3, B_0–B_3	Multiplexer Inputs
Z_0–Z_3	Multiplexer Outputs

LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE: The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

TRUTH TABLE

SELECT		INPUTS		OUTPUT
S_A	S_B	A_n	B_n	Z_n
L	L	X	X	L
H	L	L	X	L
H	L	H	X	H
L	H	X	L	L
L	H	X	H	H
H	H	L	L	H
H	H	L	H	L
H	H	H	L	L
H	H	H	H	H

H = HIGH Level
L = LOW Level
X = Don't Care

34522

PROGRAMMABLE 4-BIT BINARY DOWN COUNTER

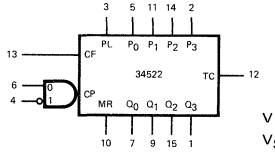
DESCRIPTION — The 34522 is a synchronous Programmable 4-Bit BCD Down Counter with an active HIGH and an active LOW Clock Input (CP_0, $\overline{CP}_1$), an asynchronous Parallel Load Input (PL), four Parallel Inputs (P_0–P_3), a Carry Forward Input (CF), four buffered Parallel Outputs (Q_0–Q_3), a Terminal Count Output (TC) and an overriding asynchronous Master Reset Input (MR).

Information on the Parallel Inputs (P_0-P_3) is loaded into the counter while the Parallel Load Input (PL) is HIGH, independent of all other input conditions except Master Reset Input (MR) which must be LOW. When the Parallel Load Input (PL) and the active LOW Clock Input ($\overline{CP}_1$) are LOW, the counter advances on a LOW-to-HIGH transition of the active HIGH Clock Input (CP_0). When the Parallel Load Input (PL) is LOW and the active HIGH Clock Input (CP_0) is HIGH, the counter advances on a HIGH-to-LOW transition of the $\overline{CP}_1$ Input. The Terminal Count Output (TC) is HIGH when the counter is in the zero state (Q_0 = Q_1 = Q_2 = Q_3 = LOW) and the Carry Forward Input (CF) is HIGH. A HIGH on the Master Reset Input (MR) resets the counter (Q_0-Q_3 = LOW) independent of other input conditions.

- **FULLY SYNCHRONOUS PROGRAMMABLE BCD DOWN COUNTER**
- **CLOCK INPUT EITHER HIGH-TO-LOW OR LOW-TO-HIGH EDGE-TRIGGERED**
- **ASYNCHRONOUS MASTER RESET**
- **CASCADABLE**
- **ASYNCHRONOUS PARALLEL LOAD**

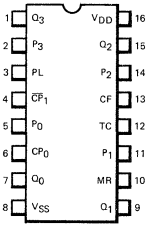
PIN NAMES	FUNCTION
PL	Parallel Load Input
P_0–P_3	Parallel Inputs
CF	Carry Forward Input
CP_0	Clock Input (L→H Edge-Triggered)
$\overline{CP}_1$	Clock Input (H→L Edge-Triggered)
MR	Asynchronous Master Reset Input
TC	TC Terminal Count Output
Q_0–Q_3	Buffered Outputs

LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

34526

PROGRAMMABLE 4-BIT BCD DOWN COUNTER

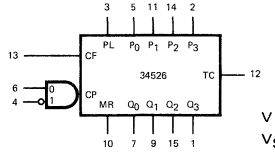
DESCRIPTION — The 34526 is a synchronous Programmable 4-Bit Binary Down Counter with an active HIGH and an active LOW Clock Input (CP_0, $\overline{CP}_1$), an asynchronous Parallel Load Input (PL), four Parallel Inputs (P_0–P_3), a Carry Forward Input (CF), four buffered Parallel Outputs (Q_0–Q_3), a Terminal Count Output (TC) and an overriding asynchronous Master Reset Input (MR).

Information on the Parallel Inputs (P_0-P_3) is loaded into the counter while the Parallel Load Input (PL) is HIGH, independent of all other input conditions except Master Reset Input (MR) which must be LOW. When the Parallel Load Input (PL) and the active LOW Clock Input ($\overline{CP}_1$) are LOW, the counter advances on a LOW-to-HIGH transition of the active HIGH Clock Input (CP_0). When the Parallel Load Input (PL) is LOW and the active HIGH Clock Input (CP_0) is HIGH, the counter advances on a HIGH-to-LOW transition of the $\overline{CP}_1$ Input. The Terminal Count Output (TC) is HIGH when the counter is in the zero state (Q_0 = Q_1 = Q_2 = Q_3 = LOW) and the Carry Forward Input (CF) is HIGH. A HIGH on the Master Reset Input (MR) resets the counter (Q_0-Q_3 = LOW) independent of other input conditions.

- **FULLY SYNCHRONOUS PROGRAMMABLE BCD DOWN COUNTER**
- **CLOCK INPUT EITHER HIGH-TO-LOW OR LOW-TO-HIGH EDGE-TRIGGERED**
- **ASYNCHRONOUS MASTER RESET**
- **CASCADABLE**
- **ASYNCHRONOUS PARALLEL LOAD**

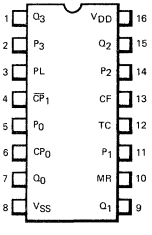
PIN NAMES	FUNCTION
PL	Parallel Load Input
P_0–P_3	Parallel Inputs
CF	Carry Forward Input
CP_0	Clock Input (L→H Edge-Triggered)
$\overline{CP}_1$	Clock Input (H→L Edge-Triggered)
MR	Asynchronous Master Reset Input
TC	Terminal Count Output
Q_0–Q_3	Buffered Outputs

LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

4

34528
DUAL RETRIGGERABLE RESETTABLE MONOSTABLE MULTIVIBRATOR

DESCRIPTION – The 34528 is a Dual Retriggerable Resettable Monostable Multivibrator. Each Multivibrator has an active LOW Input ($\overline{I_0}$), an active HIGH Input (I_1), an active LOW Clear Direct Input ($\overline{C_D}$), an Output (Q), its Complement ($\overline{Q}$) and two pins for connecting the external timing components (C_{ext}, C_{ext}/R_{ext}). An external timing capacitor must be connected between C_{ext} and C_{ext}/R_{ext} and an external resistor must be connected between C_{ext}/R_{ext} and V_{DD}.

A HIGH-to-LOW transition on the $\overline{I_0}$ Input when the I_1 Input is LOW or a LOW-to-HIGH transition on the I_1 Input when the $\overline{I_0}$ Input is HIGH produces a positive pulse (L→H→L) on the Q Output and a negative pulse (H→L→H) on the $\overline{Q}$ Output if the Clear Direct Input ($\overline{C_D}$) is HIGH. A LOW on the Clear Direct Input ($\overline{C_D}$) forces the Q Output LOW, $\overline{Q}$ Output HIGH and inhibits any further pulses until the Clear Direct Input ($\overline{C_D}$) is HIGH.

- **RESETTABLE**
- **TRIGGER ON EITHER A HIGH-TO-LOW TRANSITION ON $\overline{I_0}$ OR A LOW-TO-HIGH TRANSITION ON I_1**
- **COMPLEMENTARY OUTPUTS AVAILABLE**

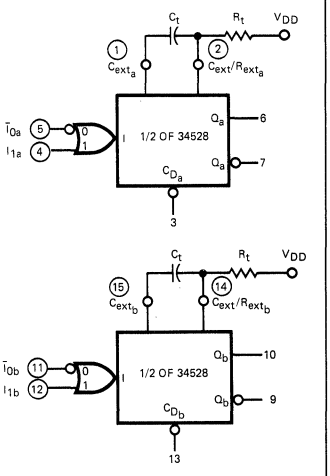
PIN NAMES	FUNCTION
$\overline{I_{0a}}$, $\overline{I_{0b}}$	Input (H→L Triggered)
I_{1a}, I_{1b}	Input (L→H Triggered)
$\overline{CD}_a$, $\overline{CD}_b$	Clear Direct Input (Active LOW)
Q_a, Q_b	Output
$\overline{Q}_a$, $\overline{Q}_b$	Complimentary Output (Active LOW)
C_{exta}, C_{extb}	External Capacitor Connections
C_{ext}/R_{exta}, C_{ext}/R_{extb}	External Capacitor/Resistor Connections

TRUTH TABLE

$\overline{I_0}$	I_1	$\overline{C_D}$	OPERATION
H→L	L	H	Trigger
H	L→H	H	Trigger
X	X	L	Reset

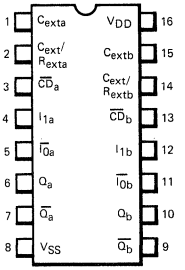
H = HIGH Level
L = LOW Level
H→L = HIGH-to-LOW Transition
L→H = LOW-to-HIGH Transition
X = Don't Care

34528 LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

34531

13-INPUT PARITY CHECKER GENERATOR

DESCRIPTION – The 34531 is a 13-Input Parity Checker/Generator with 13 Parity Inputs (I_0–I_{12}) and a Parity Output (Z). When the number of Parity Inputs that are HIGH is even, the Output (Z) is LOW. When the number of Parity Inputs that are HIGH is odd, the Output (Z) is HIGH. For words of 12 bits or less, the Output (Z) can be used to generate either odd or even parity by appropriate termination of the unused Parity Input (s). For words of 14 or more bits, the devices can be cascaded by connecting the output (Z) of one device to any Parity Input (I_0–I_{12}) of another device. When cascading devices, it is recommended that the Output (Z) of one device be connected to the I_{12} input of the other device since there is less delay to the Output (Z) from the I_{12} input than from any other Input (I_0-I_{11}).

- **VARIABLE WORD LENGTH**
- **FULLY BUFFERED OUTPUT (ACTIVE HIGH)**
- **PARITY INPUTS (ACTIVE HIGH)**

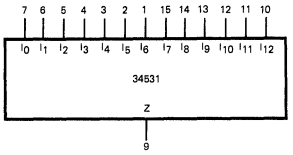
PIN NAMES	FUNCTION
I_0–I_{12}	Parity Inputs
Z	Buffered Output

TRUTH TABLE

INPUTS		OUTPUT
I_0 I_1 I_2 I_3 I_4 I_5 I_6 I_7 I_8 I_9 I_{10} I_{11} I_{12}		Z
All Thirteen	Inputs LOW	L
Any One	Input HIGH	H
Any Two	Inputs HIGH	L
Any Three	Inputs HIGH	H
Any Four	Inputs HIGH	L
Any Five	Inputs HIGH	H
Any Six	Inputs HIGH	L
Any Seven	Inputs HIGH	H
Any Eight	Inputs HIGH	L
Any Nine	Inputs HIGH	H
Any Ten	Inputs HIGH	L
Any Eleven	Inputs HIGH	H
Any Twelve	Inputs HIGH	L
All Thirteen	Inputs HIGH	H

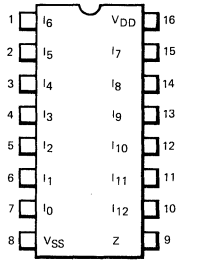
L = LOW Level
H = HIGH Level

LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

34532

8-INPUT PRIORITY ENCODER

DESCRIPTION – The 34532 is an 8-Input Priority Encoder with eight active HIGH Priority Inputs (I_0-I_7), three active HIGH Address Outputs (A_0-A_2), an active HIGH Enable Input (E_{In}), an active HIGH Enable Output (E_{Out}) and an active HIGH Group Select Output (GS).

Data is accepted on the eight Priority Inputs (I_0-I_7). The binary code corresponding to the highest Priority Input (I_0-I_7) which is HIGH is generated on the Address Outputs (A_0-A_2) if the Enable Input (E_{In}) is HIGH. Priority Input I_7 is assigned the highest priority. The Group Select output (GS) is HIGH when one or more Priority Inputs (I_0-I_7) and the Enable Input (E_{In}) are HIGH. The Enable Output (E_{Out}) is HIGH when all the Priority Inputs (I_0-I_7) are LOW and the Enable Input (E_{In}) is HIGH. The Enable Input (E_{In}) when LOW, forces all Outputs (A_0-A_2, GS, E_{Out}) LOW.

- **ACTIVE HIGH PRIORITY INPUTS**
- **CASCADABLE**

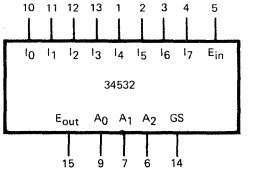
PIN NAMES	FUNCTION
I_0-I_7	Priority Inputs
E_{In}	Enable Input
E_{Out}	Enable Output
GS	Group Select Output
A_0-A_2	Address Outputs

TRUTH TABLE

INPUTS									OUTPUTS				
E_{In}	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	GS	A_2	A_1	A_0	E_{Out}
L	X	X	X	X	X	X	X	X	L	L	L	L	L
H	L	L	L	L	L	L	L	L	L	L	L	L	H
H	H	X	X	X	X	X	X	X	H	H	H	H	L
H	L	H	X	X	X	X	X	X	H	H	H	L	L
H	L	L	H	X	X	X	X	X	H	H	L	H	L
H	L	L	L	H	X	X	X	X	H	H	L	L	L
H	L	L	L	L	H	X	X	X	H	L	H	H	L
H	L	L	L	L	L	H	X	X	H	L	H	L	L
H	L	L	L	L	L	L	H	X	H	L	L	H	L
H	L	L	L	L	L	L	L	H	H	L	L	L	L

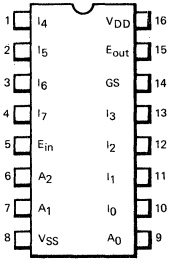
X = Don't Care
L = LOW Level
H = HIGH Level

LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

34582
CARRY LOOKAHEAD GENERATOR

DESCRIPTION – The 34582 is a Carry Lookahead Generator which provides high speed lookahead over word lengths of more than four bits. The device has a Carry Input (C_n), four active LOW Carry Generate Inputs ($\overline{G}_0$-$\overline{G}_3$), four active LOW Carry Propagate Inputs ($\overline{P}_0$-$\overline{P}_3$), three Carry Outputs (C_{n+x},C_{n+y},C_{n+z}), an active LOW Carry Propagate Output ($\overline{P}$) and an active LOW Carry Generate Output ($\overline{G}$). The logic equations for all outputs are shown below.

- **EXPANDABLE TO ANY NUMBER OF BITS**
- **HIGH SPEED LOOKAHEAD OVER WORD LENGTHS OF MORE THAN FOUR BITS**

PIN NAMES

C_n	Carry Input
$\overline{G}_0$-$\overline{G}_3$	Carry Generate Inputs (Active LOW)
$\overline{P}_0$-$\overline{P}_3$	Carry Propagate Inputs (Active LOW)
C_{n+x},C_{n+y},C_{n+z}	Carry Outputs
$\overline{G}$	Carry Generate Output (Active LOW)
$\overline{P}$	Carry Propagate Output (Active LOW)

LOGIC EQUATIONS

$$C_{n+x} = G_0 + P_0 \cdot C_n$$

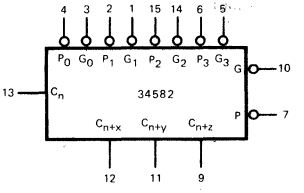
$$C_{n+y} = G_1 + P_1 \cdot G_0 + P_1 \cdot P_0 \cdot C_n$$

$$C_{n+z} = G_2 + P_2 \cdot G_1 + P_2 \cdot P_1 \cdot G_0 + P_2 \cdot P_1 \cdot P_0 \cdot C_n$$

$$\overline{G} = \overline{G_3 + P_3 \cdot G_2 + P_3 \cdot P_2 \cdot G_1 + P_3 \cdot P_2 \cdot P_1 \cdot G_0}$$

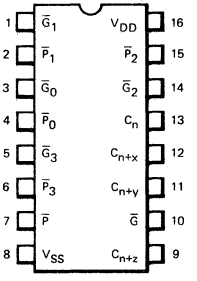
$$\overline{P} = \overline{P_3 \cdot P_2 \cdot P_1 \cdot P_0}$$

LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

340283
4-BIT BINARY FULL ADDER

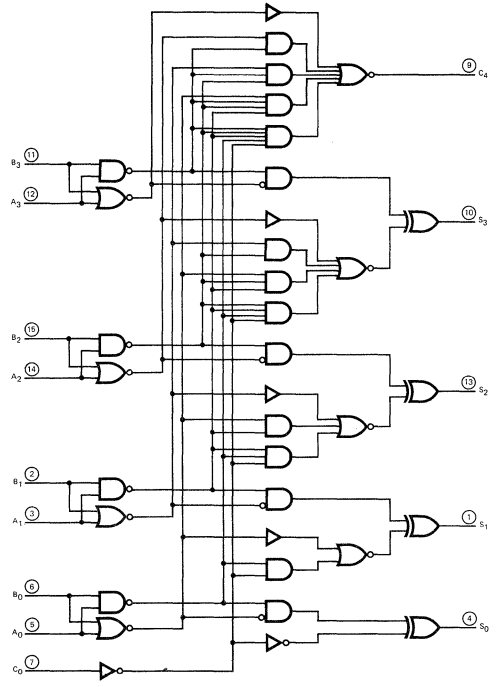
DESCRIPTION — The 340283 is a 4-Bit Binary Full Adder with two 4-bit Data Inputs (A_0–A_3, B_0–B_3), a Carry Input (C_0), four Sum Outputs (S_0–S_3) and a Carry Output (C_4).

The 340283 uses full lookahead across 4-bits to generate the Carry Output (C_4). This minimizes the necessity for extensive "lookahead" and carry-cascading circuits.

- **FULL CARRY LOOKAHEAD ACROSS FOUR BITS**
- **EASILY CASCADED**

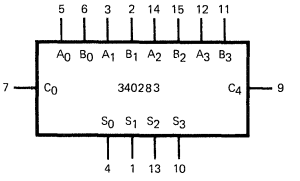
PIN NAMES	FUNCTION
A_0, B_0, A_1, B_1	Data Inputs
A_2, B_2, A_3, B_3	Data Inputs
C_0	Carry Input
S_0–S_3	Sum Outputs
C_4	Carry Output

LOGIC DIAGRAM



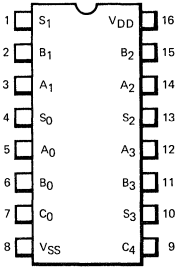
V_{DD} = Pin 16
V_{SS} = Pin 8

LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

34703

16 × 4 PARALLEL/SERIAL FIFO

FAIRCHILD CMOS MACROLOGIC*

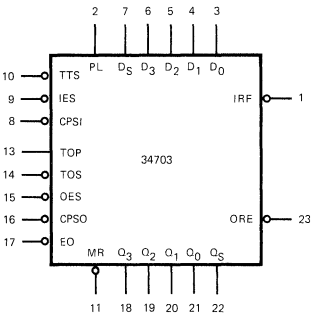
DESCRIPTION — The 34703 is an expandable high speed First-In First Out (FIFO) buffer memory with totally asynchronous and independent data inputs and outputs, in either serial or 4-bit parallel form. It can be extended to any number of words and to any number of parallel bits without additional circuitry and without compromising any features. It has 3-state output buffers which provide added versatility and make the 34703 compatible with the other circuits of the bus-oriented CMOS Macrologic family.

- **SERIAL OR PARALLEL INPUT**
- **SERIAL OR PARALLEL OUTPUT**
- **EXPANDABLE WITHOUT EXTERNAL LOGIC**
- **3-STATE FULLY BUFFERED OUTPUTS**
- **24-PIN PACKAGE**

PIN NAMES

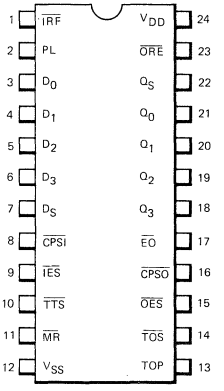
D_0-D_3	Parallel Data Inputs
D_S	Serial Data Input
PL	Parallel Load Input
$\overline{CPSI}$	Serial Input Clock Input (HIGH-to-LOW Triggered)
$\overline{CPSO}$	Serial Output Clock Input (HIGH-to-LOW Triggered)
$\overline{IES}$	Serial Input Enable (Active LOW)
$\overline{TTS}$	Transfer to Stack Input (Active LOW)
$\overline{TOS}$	Transfer Out Serial Input (Active LOW)
TOP	Transfer Out Parallel Input
$\overline{OES}$	Serial Output Enable Input (Active LOW)
$\overline{OE}$	Output Enable Input (Active LOW)
$\overline{MR}$	Master Reset Input (Active LOW)
$\overline{IRF}$	Input Register Full Output (Active LOW)
$\overline{ORE}$	Output Register Empty Output (Active LOW)
Q_0-Q_3	Parallel Data Outputs
Q_S	Serial Data Output

LOGIC SYMBOL



V_{DD} = Pin 24
V_{SS} = Pin 12

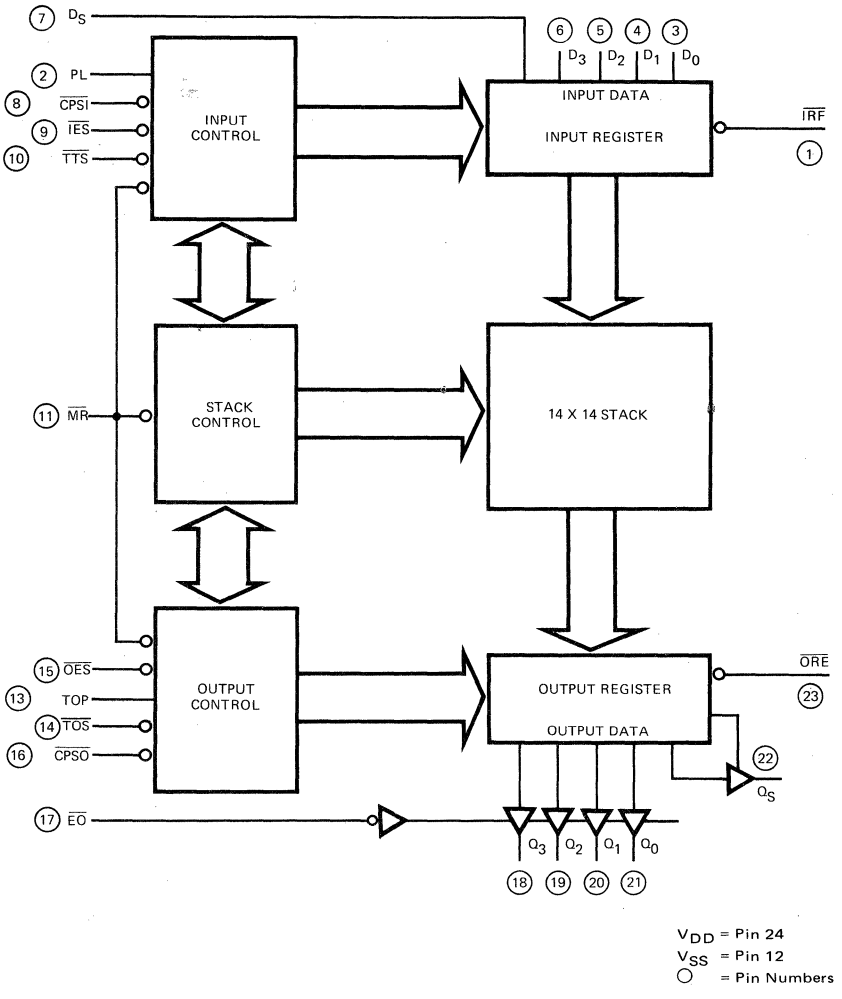
CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

*A Trademark of Fairchild Camera and Instrument Corporation.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION – As shown in the block diagram, the 34703 consists of three parts: 1) an input register with parallel and serial data inputs as well as control inputs and outputs for input handshaking and expansion. 2) a 4-bit wide, 14-word deep fall-through stack with self-contained control logic. 3) an output register with parallel and serial data outputs as well as control inputs and outputs for output handshaking and expansion. Since these three sections operate asynchronously and almost independently, they will be described separately below:

INPUT REGISTER (DATA ENTRY):
The input register can receive data in either bit-serial or in 4-bit parallel form, store it until it is sent to the fall-through stack, and generate and accept the necessary status and control signals.

Figure 1 is a conceptual logic diagram of the input section. As described later, this 5-bit register is initialized by setting the F3 flip-flop and resetting the other flip-flops. The $\overline{Q}$ output of the last flip-flop (FC) is brought out as the "Input Register Full" output ($\overline{IRF}$). After initialization this output is HIGH.

PARALLEL ENTRY:
A HIGH level on the PL input loads the D_0-D_3 data inputs into the F_0-F_3 flip-flops and sets the FC flip-flop, which forces $\overline{IRF}$ LOW, indicating "input register full". The D inputs must be stable while PL is HIGH. During parallel entry the $\overline{IES}$ input should be LOW; the $\overline{CPSI}$ input may be either HIGH or LOW.

*A Trademark of Fairchild Camera and Instrument Corporation.

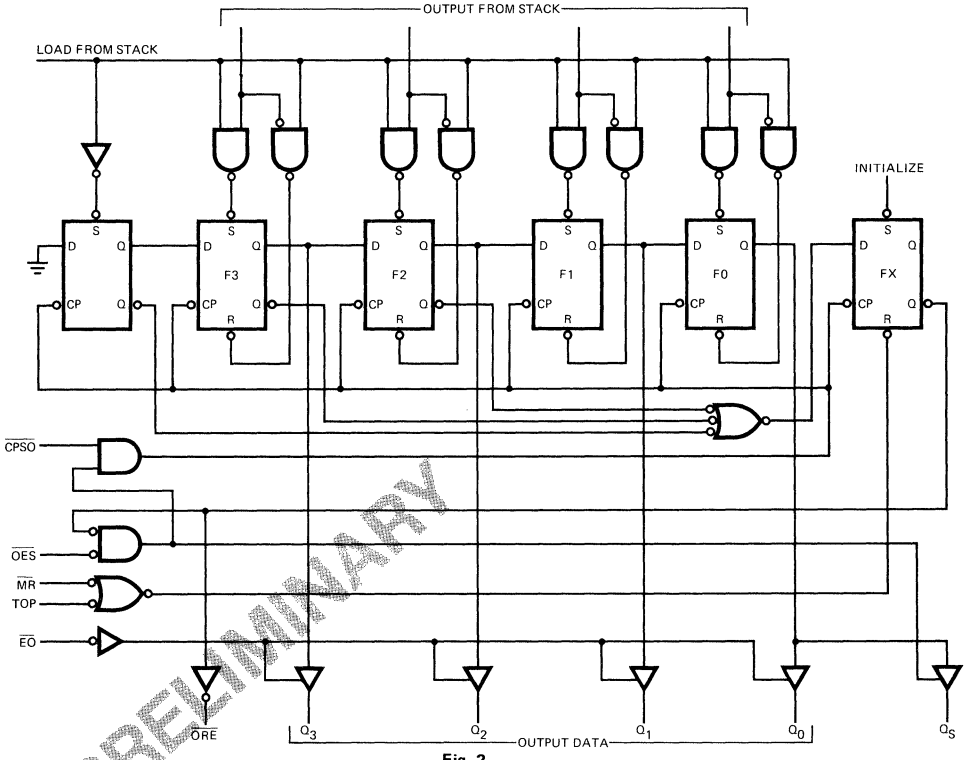


Fig. 2
CONCEPTUAL OUTPUT SECTION

SERIAL ENTRY:
Data on the DS input is serially entered into the F_3, F_2, F_1, F_0, FC shift register on each HIGH-to-LOW transition of the $\overline{CPSI}$ clock input, provided $\overline{IES}$ and PL are LOW.

After the fourth clock transition the four serial data bits are aligned in the four data flip-flops and the FC flip-flop is set, forcing $\overline{IRF}$ LOW (input register full) and internally inhibiting further $\overline{CPSI}$ clock pulses.

Figure 3 illustrates the final positions in a 34703 resulting from a 64-bit serial bit train. B_0 is the first bit, B_{63} the last bit.

TRANSFER TO THE FALL-THROUGH STACK:
The outputs of the flip-flops F_0-F_3 feed the stack. A LOW level on the $\overline{TTS}$ input attempts to initiate a "fall-through" action. If the top location of the stack is empty, data is loaded into the stack and the input register is re-initialized. Note that this initialization is postponed until PL is LOW again. Thus automatic FIFO action is achieved by connecting the $\overline{IRF}$ output to the $\overline{TTS}$ input.

Data falls through the stack automatically, pausing only when it is necessary for an empty next location. In the 34703, like in most modern FIFO designs, the $\overline{MR}$ input initializes the stack control section only and does not clear the data.

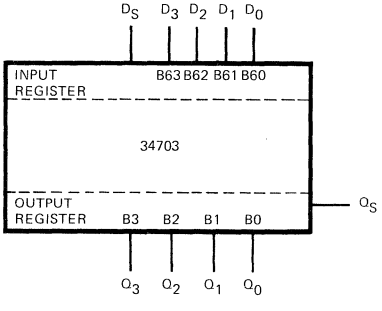


Fig. 3
FINAL POSITIONS IN A 34703 RESULTING FROM A 64-BIT SERIAL TRAIN

OUTPUT REGISTER (DATA EXTRACTION):
The output register receives a 4-bit data word from the bottom stack location, stores it and puts it on a 3-state 4-bit parallel data bus or on a 3-state serial data bus. The output section generates and receives the necessary status and control signals. Figure 2 is a conceptual logic diagram of the output section.

PARALLEL DATA EXTRACTION:
When the FIFO is empty (after a LOW pulse is applied to $\overline{MR}$), the Output Register Empty ($\overline{ORE}$) output is LOW. After data has been entered into the FIFO and has fallen through to the bottom stack location, it is transferred into the output register, provided the "Transfer Out Parallel" (TOP) input is HIGH, and the $\overline{OES}$ input is LOW. As a result of the data transfer $\overline{ORE}$ goes HIGH, indicating valid data on the data outputs (provided the 3-state buffer is enabled).

TOP can now be used to clock out the next word. When TOP goes LOW, $\overline{ORE}$ will go LOW indicating that the output data has been extracted, but the data itself remains on the output bus until the next LOW-to-HIGH transition of TOP transfers the next word (if available) into the output register as explained above. During parallel data extraction $\overline{TOS}$, $\overline{CPSO}$ and $\overline{OES}$ should be LOW.

SERIAL DATA EXTRACTION:
When the FIFO is empty (after a LOW pulse is applied to $\overline{MR}$), the Output Register Empty ($\overline{ORE}$) output is LOW. After data has been entered into the FIFO and has fallen through to the bottom stack location, it is transferred into the output shift register provided the "Transfer Out Serial" ($\overline{TOS}$) input is LOW. TOP must be HIGH, and $\overline{OES}$ and $\overline{CPSO}$ must be LOW.

As a result of the data transfer $\overline{ORE}$ goes HIGH indicating valid data in the shift register. The 3-state serial data output Q_S is automatically enabled and puts the first data bit on the output bus. Data is serially shifted out on the HIGH-to-LOW transition of $\overline{CPSO}$. The fourth transition empties the shift register, forces $\overline{ORE}$ LOW and disables the serial output Q_S. For serial operation the $\overline{ORE}$ output is tied to the $\overline{TOS}$ input, requesting a new word from the stack as soon as the previous one has been shifted out.

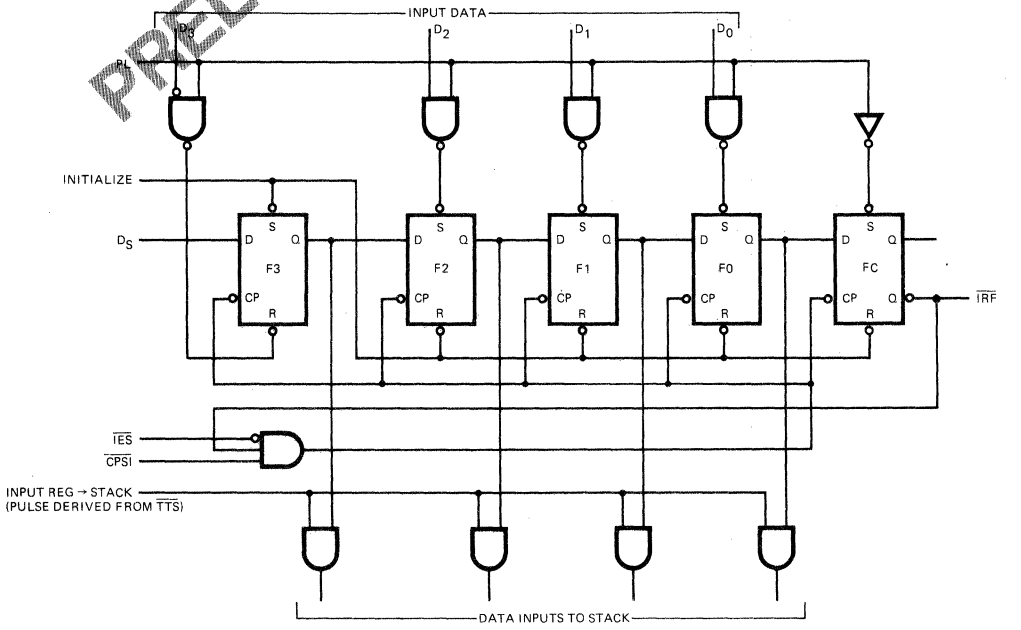


Fig. 1
CONCEPTUAL INPUT SECTION

EXPANSION

VERTICAL EXPANSION — The 34703 can be vertically expanded to store more words without any external parts. The interconnections necessary to form a 46-word by 4-bit FIFO are shown in Figure 4. Using the same technique, any FIFO of 15n + 1 words by four bits can be constructed. Note that expansion does not sacrifice any of the FIFO's flexibility for Serial/Parallel input and output.

HORIZONTAL EXPANSION — The 34703 can also be horizontally expanded to store long words (in multiples of four bits) without any external logic. The inter-connections necessary to form a 16-word by 12-bit FIFO are shown in Figure 5. Using the same technique, any FIFO of 16 words by 4 x n bits can be constructed. When expanding in the horizontal direction, it is necessary to connect the $\overline{IRF}$ and $\overline{ORE}$ outputs of the right most device (most significant device) to the $\overline{TTS}$ and $\overline{TOS}$ inputs respectively of all devices to the left (less significant devices).

As in the vertical expansion scheme, horizontal expansion does not require sacrificing any of the FIFO's flexibility for Serial/Parallel input and output.

HORIZONTAL AND VERTICAL EXPANSION — The 34703 can be expanded in both the horizontal and vertical direction without any external parts and without sacrificing any of the FIFO's flexibility for Serial/Parallel input and output. The interconnections necessary to form a 31-word by 16-bit FIFO are shown in Figure 6.

Figures 7 and 8 show the timing diagrams for serial data entry and extraction for the 31-word by 16-bit FIFO shown in Figure 6. The final position of data after serial insertion of 496 bits into the FIFO array of Figure 6 is shown in Figure 9.

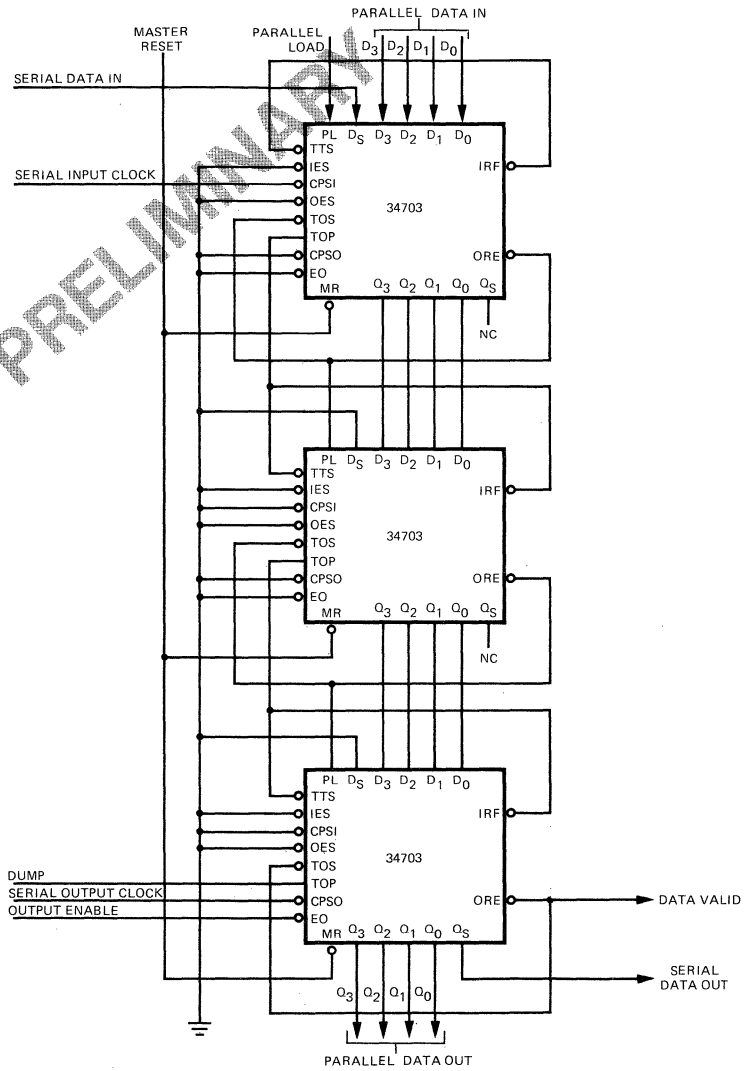


Fig. 4
A VERTICAL EXPANSION SCHEME FOR THE 34703

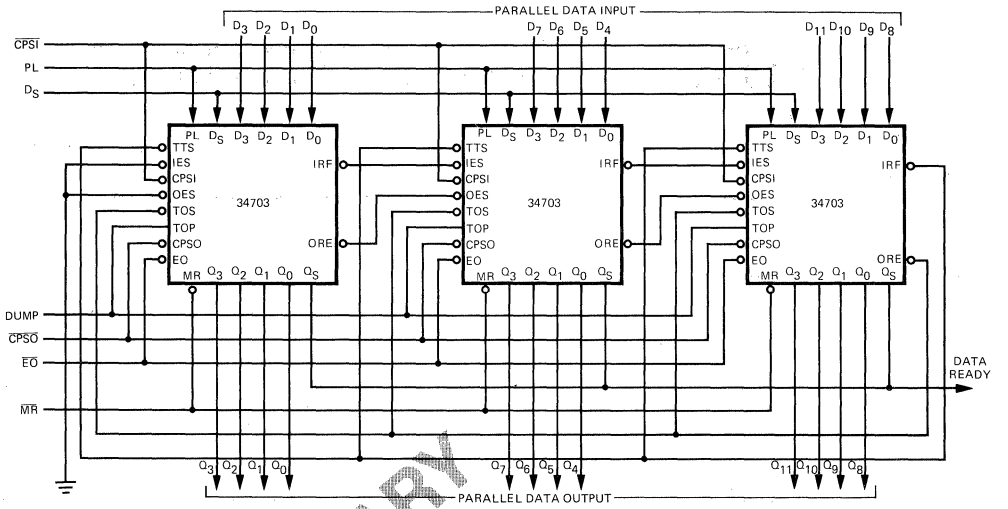


Fig. 5
A HORIZONTAL EXPANSION SCHEME FOR THE 34703

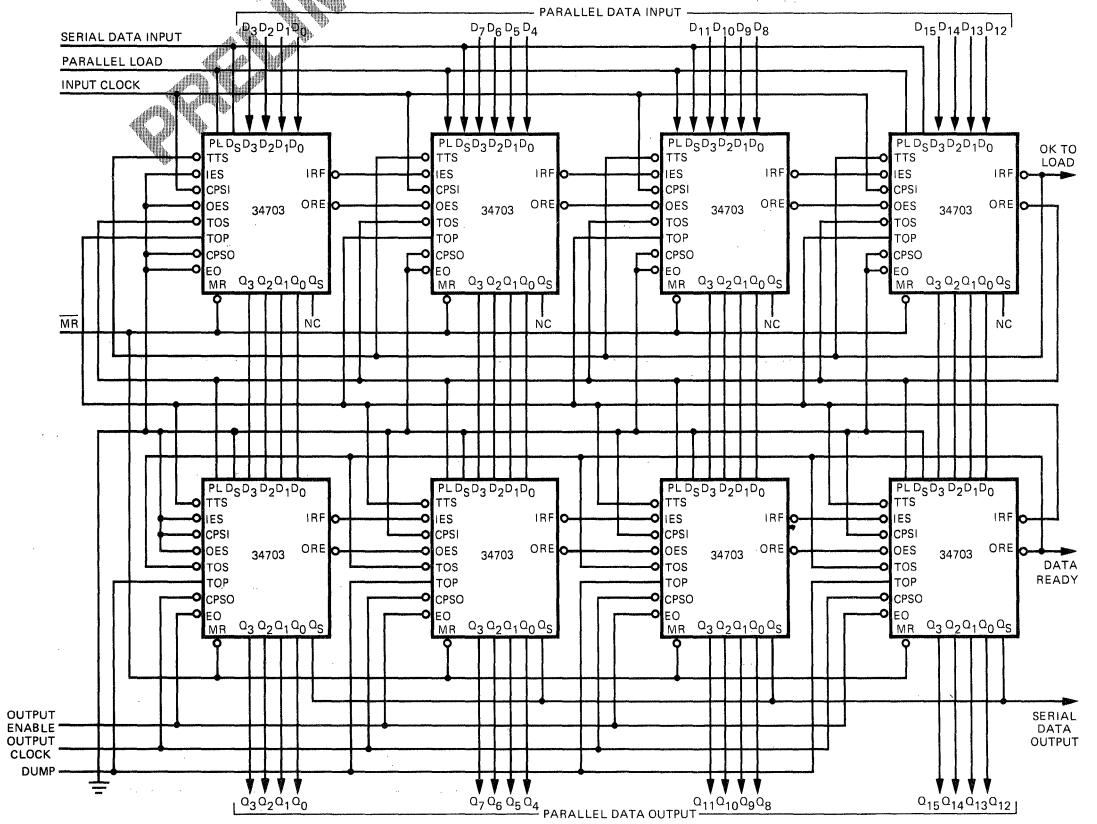


Fig. 6
A 31 X 16 FIFO ARRAY

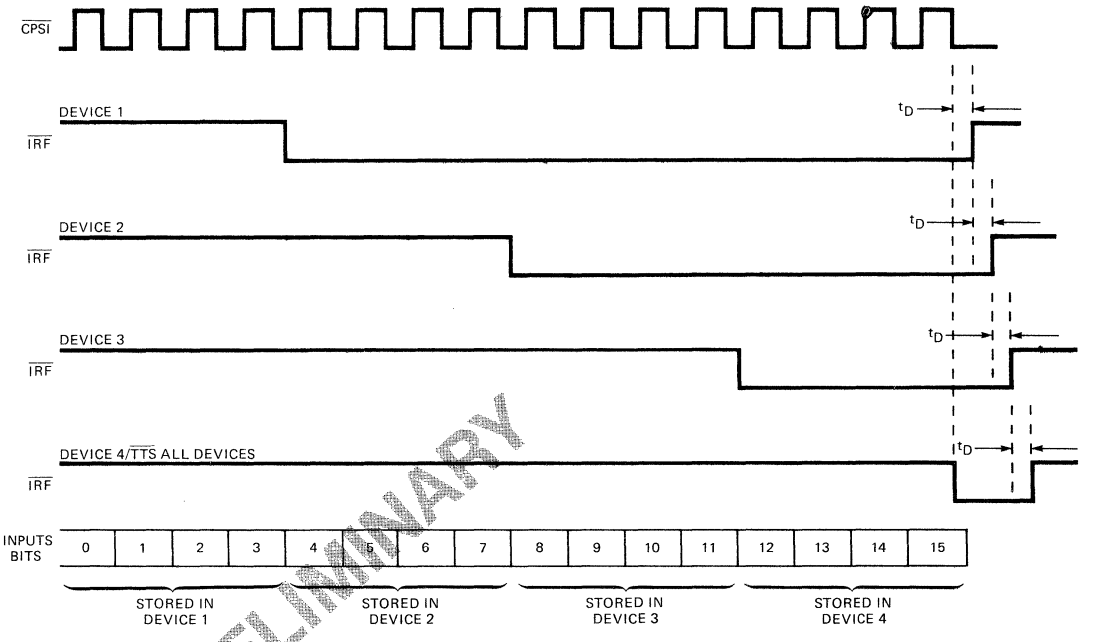


Fig. 7
SERIAL DATA ENTRY FOR ARRAY OF FIG. 6

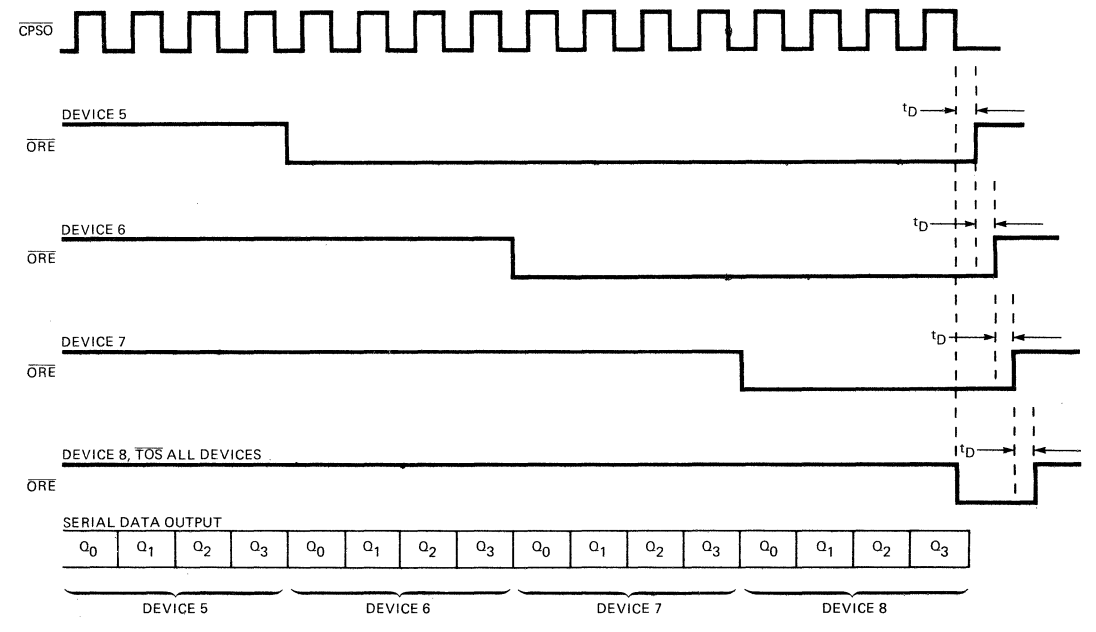


Fig. 8
SERIAL DATA EXTRACTION FOR ARRAY OF FIG. 6

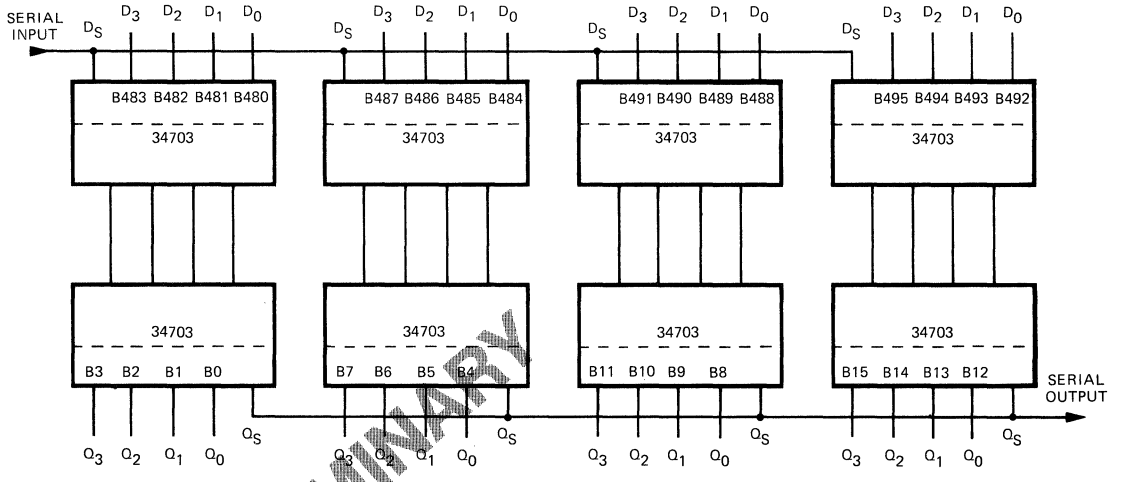


Fig. 9
FINAL POSITION OF A 496-BIT SERIAL INPUT

34704

DATA PATH SWITCH

FAIRCHILD CMOS MACROLOGIC*

DESCRIPTION — The 34704 Data Path Switch (DPS) is a combinatorial array for closing data path loops around arithmetic/logic networks such as the 34705 (Arithmetic Logic Register Stack). A total of 32 instructions (see Table 1) facilitate logic shifting, byte swapping, masking, sign extension, introduction of common constants and other operations.

The 5-bit Instruction word (I_0-I_4) selects one of the 32 instructions operating on two sets of 4-bit Data Inputs ($\overline{D}_0$-$\overline{D}_3$, $\overline{K}_0$-$\overline{K}_3$). Shift Left Input ($\overline{LI}$) and Output ($\overline{LO}$) and Shift Right Input ($\overline{RI}$) and Output ($\overline{RO}$) are available for expansion in 4-bit increments. An active LOW Output Enable Input ($\overline{EO}$) provides for 3-state control of the Data Outputs ($\overline{O}_0$-$\overline{O}_3$) for bus oriented applications.

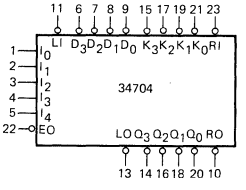
The 34704 is packaged in the new slim 24-pin Dual In-Line package.

- **EXPANDABLE IN MULTIPLES OF FOUR BITS**
- **TWO 4-BIT DATA INPUT BUSES**
- **4-BIT DATA OUTPUT BUS WITH 3-STATE OUTPUT BUFFERS**
- **USEFUL FOR BYTE MASKING AND SWAPPING**
- **PROVIDES ARITHMETIC OR LOGIC SHIFT**
- **PROVIDES FOR SIGN EXTENSION**
- **GENERATES COMMONLY USED CONSTANTS**
- **NEW SLIM 24-PIN DIP**

PIN NAMES

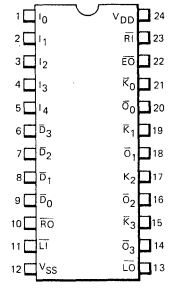
$\overline{D}_0$-$\overline{D}_3$, $\overline{K}_0$-$\overline{K}_3$	Data Inputs (Active LOW)
I_0-I_4	Instruction Word Input
$\overline{LI}$	Shift Left Input (Active LOW)
$\overline{LO}$	Shift Left Output (Active LOW)
$\overline{RI}$	Shift Right Input (Active LOW)
$\overline{RO}$	Shift Right Output (Active LOW)
$\overline{EO}$	Output Enable Input (Active LOW)
$\overline{O}_0$-$\overline{O}_3$	Data Output (Active LOW)

LOGIC SYMBOL



V_{DD} = Pin 24
V_{SS} = Pin 12

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

TABLE 1
INSTRUCTION SET FOR THE 34704

INPUTS I_4	I_3	I_2	I_1	I_0	OUTPUTS $\overline{O}_3$	$\overline{O}_2$	$\overline{O}_1$	$\overline{O}_0$	FUNCTION
L	L	L	L	L	L	L	L	L	Byte Mask
L	L	L	L	H	H	H	H	H	Byte Mask
L	L	L	H	L	L	L	L	H	Minus "2" in 2s Comp(1)
L	L	L	H	H	L	L	L	L	Minus "1" in 2s Comp(1)
L	L	H	L	L	$\overline{D}_3$	$\overline{D}_2$	$\overline{D}_1$	$\overline{D}_0$	Byte Mask D-Bus
L	L	H	L	H	H	H	H	H	Byte Mask D-Bus
L	L	H	H	L	$\overline{D}_3$	$\overline{D}_2$	$\overline{D}_1$	$\overline{D}_0$	Byte Mask D-Bus
L	L	H	H	H	L	L	L	L	Byte Mask D-Bus
L	H	L	L	L	L	H	H	H	Negative Byte Sign Mask
L	H	L	L	H	H	H	H	H	Positive Byte Sign Mask
L	H	L	H	L	$\overline{K}_3$	$\overline{K}_2$	$\overline{K}_1$	$\overline{K}_0$	Byte Mask K-Bus
L	H	L	H	H	L	L	L	L	Byte Mask K-Bus
L	H	H	L	L	$\overline{D}_3$	$\overline{D}_2$	$\overline{D}_1$	$\overline{D}_0$	Load Byte
L	H	H	L	H	$\overline{K}_3$	$\overline{K}_2$	$\overline{K}_1$	$\overline{K}_0$	Load Byte
L	H	H	H	L	H	H	H	L	Plus "1"
L	H	H	H	H	H	H	H	H	Zero

INPUTS I_4	I_3	I_2	I_1	I_0	OUTPUTS $\overline{LO}$	$\overline{O}_3$	$\overline{O}_2$	$\overline{O}_1$	$\overline{O}_0$	$\overline{RO}$	FUNCTION
H	L	L	L	L	$\overline{RI}$	$\overline{RI}$	$\overline{RI}$	$\overline{RI}$	$\overline{RI}$		K-Bus Sign Extend
H	L	L	L	H	$\overline{K}_3$	$\overline{K}_3$	$\overline{K}_2$	$\overline{K}_1$	$\overline{K}_0$		K-Bus Sign Extend
H	L	L	H	L	$\overline{RI}$	$\overline{RI}$	$\overline{RI}$	$\overline{RI}$	$\overline{RI}$		D-Bus Sign Extend
H	L	L	H	H	$\overline{D}_3$	$\overline{D}_3$	$\overline{D}_2$	$\overline{D}_1$	$\overline{D}_0$		D-Bus Sign Extend
H	L	H	L	L	$\overline{D}_3$	$\overline{D}_2$	$\overline{D}_1$	$\overline{D}_0$	$\overline{RI}$		D-Bus Shift Left
H	L	H	L	H	$\overline{K}_3$	$\overline{K}_2$	$\overline{K}_1$	$\overline{K}_0$	$\overline{RI}$		K-Bus Shift Left
H	L	H	H	L	$\overline{LI}$	$\overline{D}_3$	$\overline{D}_2$	$\overline{D}_1$	$\overline{D}_0$		D-Bus Shift Right
H	L	H	H	H	$\overline{D}_3$	$\overline{D}_3$	$\overline{D}_2$	$\overline{D}_1$	$\overline{D}_0$		D-Bus Shift Right Arith(2)
H	H	L	L	L	$\overline{LI}$	$\overline{K}_3$	$\overline{K}_2$	$\overline{K}_1$	$\overline{K}_0$		K-Bus Shift Right
H	H	L	L	H	$\overline{K}_3$	$\overline{K}_3$	$\overline{K}_2$	$\overline{K}_1$	$\overline{K}_0$		K-Bus Shift Right Arith(2)
H	H	L	H	L	$\overline{K}_3$	$\overline{K}_2$	$\overline{K}_1$	$\overline{K}_0$			Byte Mask K-Bus
H	H	L	H	H	H	H	H	H			Byte Mask K-Bus
H	H	H	L	L	D_3	D_2	D_1	D_0			Complement D-Bus
H	H	H	L	H	K_3	K_2	K_1	K_0			Complement K-Bus
H	H	H	H	L							Undefined
H	H	H	H	H							Undefined

H = HIGH Level
L = LOW Level

(1) Comp = Complement
(2) Arith = Arithmetic

*A Trademark of Fairchild Camera and Instrument Corporation.

34705

ARITHMETIC LOGIC REGISTER STACK

FAIRCHILD CMOS MACROLOGIC*

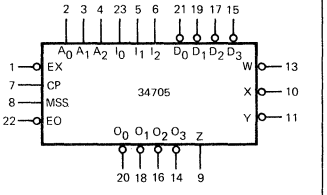
DESCRIPTION – The Arithmetic Logic Register Stack (ALRS) is designed to implement general registers in programmable digital systems. The device contains a 4-bit arithmetic logic unit (ALU), an 8-word by 4-bit RAM and associated control logic. The ALU implements eight arithmetic and logic functions where one 4-bit operand is supplied from an external source (input data bus) and the second 4-bit operand is supplied internally from one of the eight RAM words selected by the Address Inputs (A_0–A_2). The result of the operation performed on the operands is loaded into the same RAM location and simultaneously loaded into the output register, making it available at the 3-state output data bus.

The 34705 operates on four bits of data but features are provided for expansion to longer word lengths. Carry Propagate and Carry Generate outputs are provided for an external carry lookahead where maximum operating speed is required. In applications where high speed arithmetic is not needed, ripple expansion may also be implemented. The 34705 provides three status signals – Zero, Negative and Overflow – to qualify the result of an operation.

The 34705 is a member of Fairchild's 34000 CMOS Macrologic family and is available in the new slim 24-pin Dual In-Line package.

- **EIGHT GENERAL REGISTERS/ACCUMULATORS IN A SINGLE PACKAGE**
- **2 MHz MICROINSTUCTION RATE**
- **VERY LOW POWER – IDEAL FOR BATTERY OPERATION**
- **EXPANDABLE IN MULTIPLES OF FOUR BITS**
- **PROVIDES FOR RIPPLE OR CARRY LOOKAHEAD**
- **IMPLEMENTS 64 MICROINSTRUCTIONS**
- **PROVIDES THREE STATUS SIGNALS – ZERO, NEGATIVE AND OVERFLOW**
- **3-STATE OUTPUTS**
- **NEW SLIM 24-PIN DIP**

LOGIC SYMBOL



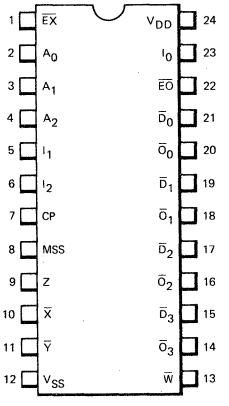
V_{DD} = Pin 24
V_{SS} = Pin 8

PIN NAMES

$\overline{D}_0$-$\overline{D}_3$	Data Inputs (Active LOW)
A_0-A_2	Address Instruction Inputs
I_0-I_2	ALU Instruction Inputs
MSS	Most Significant Slice Input
CP	Clock Input
$\overline{EO}$	Output Enable Input (Active LOW)
$\overline{EX}$	Execute Input (Active LOW)
$\overline{O}_0$-$\overline{O}_3$	Data Outputs (Active LOW)
$\overline{W}$	Ripple Carry Output (Active LOW, Note a)
$\overline{X}$	Carry Propagate Output (Active LOW, Note b)
$\overline{Y}$	Carry Generate Output (Active LOW, Note c)
Z	Zero Status Output (Active HIGH, Open Drain)

NOTES:
a. $\overline{W}$ output also carries instruction information.
b. $\overline{X}$ output provides negative status on most significant slice.
c. $\overline{Y}$ output provides overflow status on most significant slice.

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

TABLE 1
INSTRUCTION FIELD ASSIGNMENT

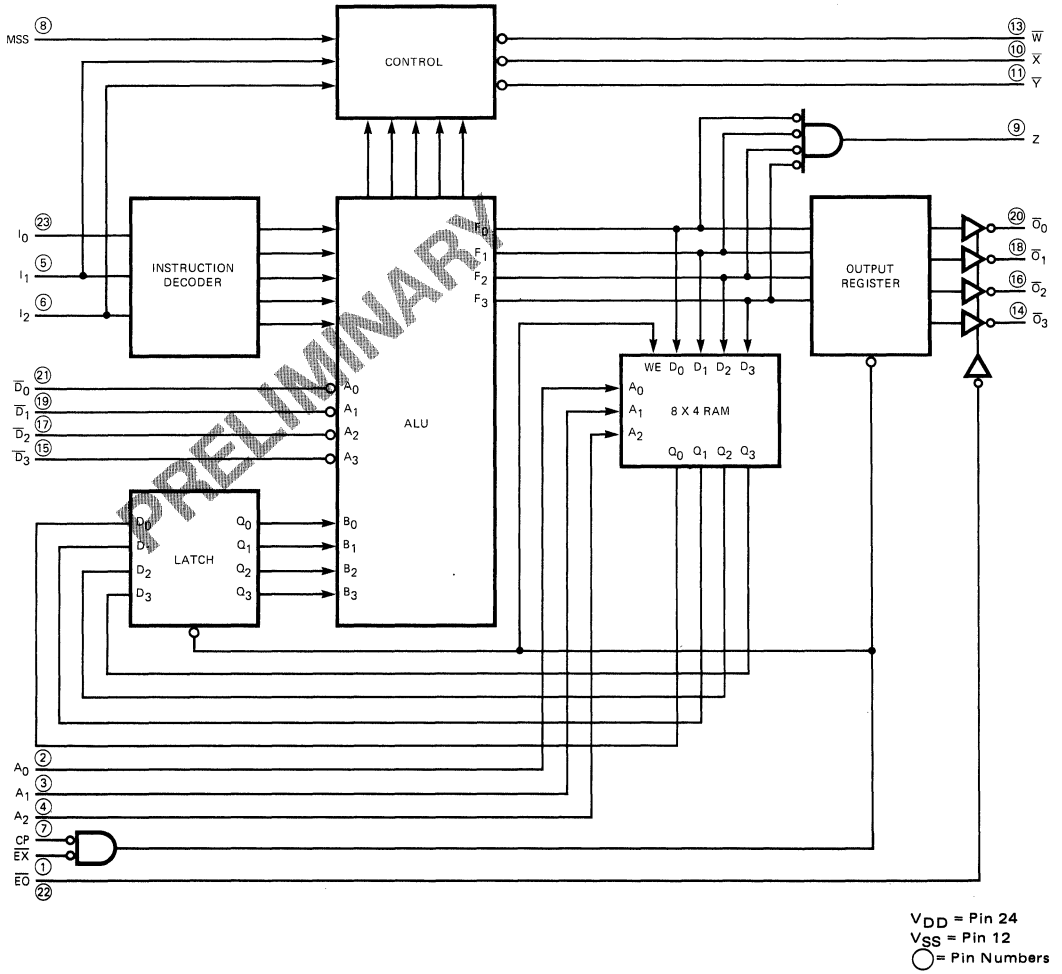
I_2	I_1	I_0	INTERNAL OPERATION
L	L	L	Rx plus D-Bus plus 1 → Rx
L	L	H	Rx plus D-Bus → Rx
L	H	H	Rx · D-Bus → Rx (Logic AND)
L	H	H	D-Bus → Rx
H	L	L	Rx → Rx
H	L	H	Rx + D-Bus → Rx (Logic OR)
H	H	L	Rx ⊕ D-Bus → Rx
H	H	H	$\overline{\text{D-Bus}}$ → Rx

H = Logic HIGH Level L = Logic LOW Level

NOTES:
1. Rx is the RAM location addressed by A_0–A_2.
2. The result of any operation is always loaded into the Output Register.

*A Trademark of Fairchild Camera and Instrument Corporation.

34705 BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION – As shown in the Block Diagram, the 34705 Arithmetic Logic Register Stack (ALRS) consists of a 4-bit ALU, an 8-word by 4-bit RAM with output latches, an instruction decode network, control logic, and a 4-bit output register.

The ALU receives the active LOW input data ($\overline{D}_0$–$\overline{D}_3$) as one operand while the RAM provides the second operand through latches. The ALU output is stored in both the RAM and output register. The active LOW output data bus (O_0–O_3) is obtained from the output register through 3-state buffers. An active LOW Output Enable ($\overline{EO}$) input controls these buffers; a HIGH level on $\overline{EO}$ disables them (high impedance state).

The instruction bus for the 34705 consists of two fields, A and I; A_0, A_1, A_2 specify the desired location on the RAM and I_0, I_1, I_2 specify the desired function to be performed. Table 1 lists Instruction Field Code assignments. Thus, the 34705 provides eight registers (R_0–R_7) and eight different operations may be performed on any of these registers. The I_0, I_1, I_2 inputs are decoded by the instruction decode network to generate necessary control signals for the ALU. The ALU also generates and transmits to the control logic the following signals: carry out, carry propagate, carry generate, negative status and overflow status. The control logic manipulates the status signals as a function of I_0, I_1, I_2 and a control input MSS. A HIGH level on the MSS (Most Significant Slice Input) declares the most significant slice in a 34705 array. All devices, except the most significant 34705, should have a LOW level (ground) on the MSS input. The control logic generates three device outputs, $\overline{W}$, $\overline{X}$ and $\overline{Y}$ for arrayed operation of 34705 arrays. An all zero result from the ALU is decoded and presented at the open drain Zero Status (Z) Output.

The I_0 input serves a dual purpose: for arithmetic instructions, it is used as the carry input and for non-arithmetic instructions it serves as an instruction input. This is possible because only two arithmetic instructions require carry. The dual purpose use of I_0 plays an important role in 34705 expansion schemes.

OPERATION – The 34705 operates on a single clock. CP and $\overline{EX}$ are inputs to a 2-input active LOW AND gate. A microcycle starts as the clock goes HIGH. For normal operation the Execute ($\overline{EX}$) is LOW. Data is read from the RAM through enabled latches and applied as one operand to the ALU. Data inputs ($\overline{D}_0$–$\overline{D}_3$) are applied to the ALU as the other operand and the operation as determined by instruction lines I_0, I_1, I_2 is executed. When CP is LOW, the latches are disabled and the result of the operation is written back into the RAM provided that $\overline{EX}$ is LOW. Then A lines must obviously be held stable during this time. On the LOW-to-HIGH CP transition, the result of the operation is loaded into the output register and a new microcycle can start. If $\overline{EX}$ is held HIGH, the operation selected by the I and A inputs is performed, but the result is not written back into the RAM and is not clocked into the output register.

34705 ARRAYS

The 34705 is organized to operate on a 4-bit wide data bus but can easily be expanded for longer words. Expansion requires that carries from lesser significant slices be propagated towards the most significant slice. The 34705 provides full lookahead capability for high speed arithmetic. Appropriate Carry Generate ($\overline{Y}$) and Carry Propagate ($\overline{X}$) outputs are provided so that only one external carry lookahead generator is needed for every four 34705s. When speed is not a prime consideration, it is possible to implement ripple carry expansion.

In arrayed operation, it is common to bus $\overline{EX}$, CP and $\overline{EO}$ inputs of all devices. The Z output is open drain and is normally OR-tied with the other devices and to an external load resistor so that a HIGH level indicates a zero result from an operation in the array.

Figure 2 shows a ripple carry 16-bit wide array using four 34705s. The MSS input is tied to V_{DD} on the most significant slice (ALRS 4). The MSS input of the other devices are tied to ground (V_{SS}). The instruction bus of this array consists of A-Field and I-Field. A-Field is obtained by connecting corresponding A inputs of all 4 devices. The I_0 input of device 1 (i.e., least significant slice) in conjunction with the bussed I_1, I_2 inputs forms the I-Field for the array. The I_0 inputs of devices 2, 3 and 4 are connected to the $\overline{W}$ outputs of devices 1, 2 and 3 respectively. The ALU network generates the carry propagate output. The control logic operates on this signal as a function of I_1 and I_2 to generate the $\overline{W}$ output. If both I_1 and I_2 are LOW (i.e., an arithmetic instruction), the $\overline{W}$ output is the carry output of that slice. In case of non-arithmetic instructions, it will assume the state of the I_0 input. Thus, in Figure 1, if an arithmetic instruction is specified, carry will propagate through the $\overline{W}$ output to I_0 input of the next higher significant slice. On the other hand, non-arithmetic instructions will effectively connect all I_0 inputs together to form the I-Field for the array. The $\overline{W}$ output of device 4 is the carry output from the array. The control logic also generates $\overline{X}$ and $\overline{Y}$ outputs which participate in expansion when full carry lookahead is required. These outputs are normally ignored in ripple expansion except for the most significant slice. If a device is the most significant slice, $\overline{X}$ and $\overline{Y}$ correspond to negative and overflow status signals. Thus $\overline{X}$ output of Device 4 will be LOW, if the result of an operation has its most significant bit as "1" (i.e., negative result). Similarly a LOW level on $\overline{Y}$ output of device 4 indicates that arithmetic overflow has occurred. If the two operands have the same sign and the result has opposite sign, then it is assumed that an overflow has occurred. It should be noted that $\overline{W}$, $\overline{X}$ and $\overline{Y}$ are not controlled by $\overline{EX}$ or CP. Figure 2 shows a 16-bit array with full carry lookahead expansion. Implementation of the lookahead scheme requires the use of an external 34582 in addition to the four 34705s in the array. Since device 1 is the least significant and device 4 is the most significant slice, the MSS inputs of the first three devices are connected to ground while device 4 has a HIGH level at this input. The A-Field for the array instruction bus is obtained by connecting corresponding A inputs of all four devices. Bussed I_1 and I_2 inputs together with the I_0 input of device 1 form the I-Field for the array. The I_0 inputs for devices 2, 3 and 4 are obtained from the 34582 carry outputs (Cn+x, Cn+y and Cn+z respectively). Also the P and G inputs of 34582 are connected to $\overline{X}$ and $\overline{Y}$ outputs of the 34705s as shown. The control logic in the 34705 (see Block Diagram) generates $\overline{X}$ and $\overline{Y}$ outputs as a function of I_1, I_2 and MSS inputs as well as the carry generate and carry propagate outputs of the ALU. If the MSS input of a slice is LOW and an arithmetic instruction is specified, its $\overline{X}$ output will reflect carry propagate and $\overline{Y}$ will reflect carry generate outputs from that slice. For an arithmetic instruction the I_0 input will be treated as carry-in into a slice irrespective of MSS. Thus, whenever I_1 and I_2 are LOW, the array behaves as an adder with full carry lookahead. The $\overline{W}$ outputs still reflect carry output, which is ignored for devices 1, 2 and 3. The $\overline{W}$ carry input to the array so the I_0 input of device 1 must be connected to the appropriate 34582 input as shown.

When a non-arithmetic instruction is specified to the array, the control logic of the 34705 forces a LOW level on $\overline{X}$ and a HIGH level on $\overline{Y}$ outputs on all except the most significant slice. An examination of the 34582 logic reveals that whenever P is LOW and G is HIGH, the associated carry output is the same as the carry input. Thus, in Figure 2, devices 2 3 and 4 will assume the logic level as that presented to the I_0 input of device 1 during non-arithmetic instructions effectively bussing I_0 through all four devices. As in the case of ripple expansion, $\overline{X}$ and $\overline{Y}$ outputs of device 4 represent negative and overflow from the array.

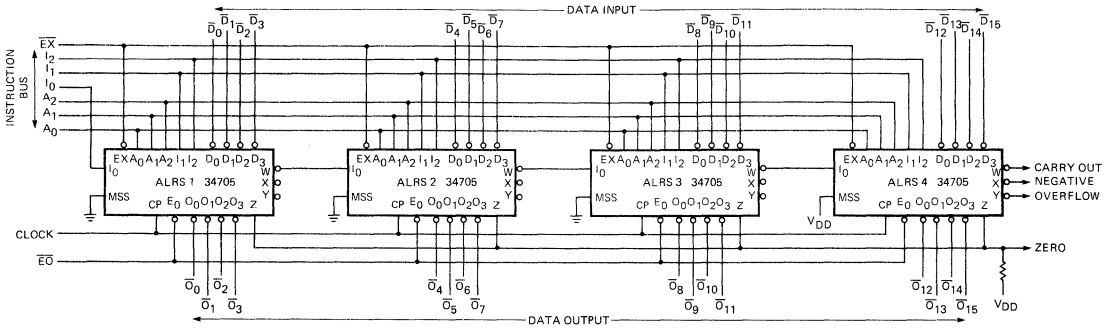


FIG. 1

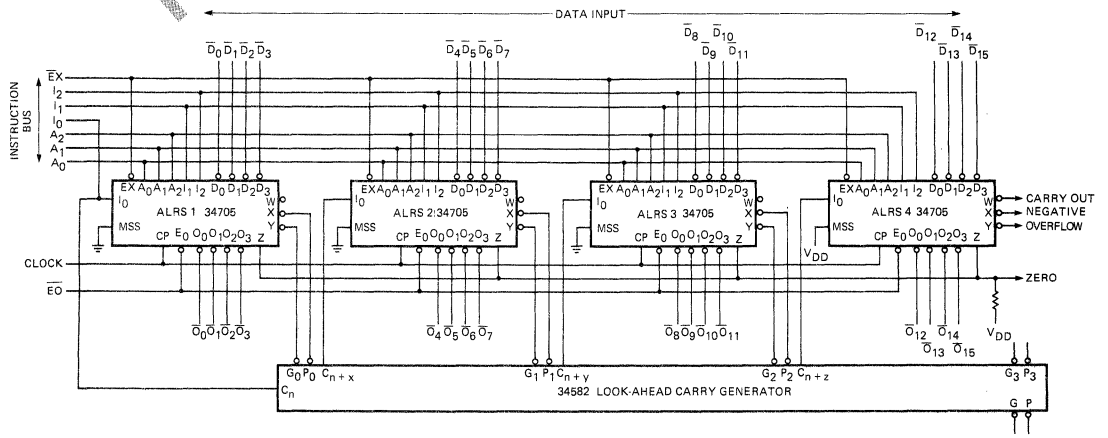


FIG. 2

34706

PROGRAM STACK

FAIRCHILD CMOS MACROLOGIC*

DESCRIPTION — The 34706 is a 16-word by 4-bit "Push-Down Pop-Up" Program Stack. It is designed to implement Program Counter (PC) and return address storage for nested subroutines in programmable digital systems. The 34706 executes four instructions: Return, Branch, Call and Fetch as specified by a 2-bit instruction. When the device is initialized, the program counter (PC) is in the top location of the stack. As a new PC value is "pushed" into the stack (Call Operation), all previous PC values effectively move down one level. The top location of the stack is the current PC. Up to 16 PC values can be stored, which gives the 34706 a 15 level nesting capability. "Popping" the stack (Return Operation) brings the most recent PC to the top of the stack and makes it available at the two output buses. The remaining two instructions affect only the top location of the stack. In the Branch Operation a new PC value is loaded into the top location of the stack from the $\overline{D}_0 - \overline{D}_3$ inputs. In the Fetch Operation, the contents of the top stack location (current PC value) are put on the $X_0 - X_3$ bus and the current PC value is incremented.

The 34706 may be expanded to any word length without additional logic. Three-state output drivers are provided on the 4-bit Address ($X_0 - X_3$) and Data Outputs, ($\overline{O}_0 - \overline{O}_3$); the X-bus outputs are enabled internally and only during the Fetch Instruction whereas the O-bus outputs are controlled by an Output Enable ($\overline{EO}_0$). Two status outputs, Stack Full ($\overline{SF}$) and Stack Empty ($\overline{SE}$) are provided. The 34706 is a member of Fairchild's 34000 CMOS Macrologic family, and is available in the new slim 24-pin package.

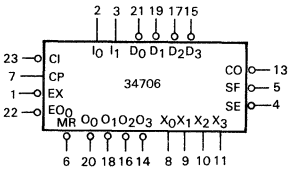
- **16-WORD BY 4-BIT LIFO**
- **15-LEVEL NESTING CAPABILITY**
- **VERY LOW POWER — IDEAL FOR BATTERY OPERATION**
- **RELATIVE ADDRESSING CAPABILITY**
- **2 MHz MICROINSTRUCTION RATE**
- **PROGRAM COUNTER LOADABLE FROM DATA BUS**
- **OPTIONAL AUTOMATIC INCREMENT OF PROGRAM COUNTER**
- **STACK LIMIT STATUS INDICATORS**
- **NEW SLIM 24-PIN DIP**

PIN NAMES

$\overline{D}_0$-$\overline{D}_3$	Data Inputs (Active LOW)
I_0, I_1	Instruction Inputs
$\overline{EX}$	Execute Input (Active LOW)
CP	Clock Input
$\overline{MR}$	Master Reset Input (Active LOW)
$\overline{CI}$	Carry Input (Active LOW)
$\overline{EO}_0$	Output Enable Input (Active LOW)
$\overline{O}_0$-$\overline{O}_3$	Output Data Outputs (Active LOW)
$\overline{X}_0$-$\overline{X}_3$	Address Outputs
$\overline{CO}$	Carry Output (Active LOW)
$\overline{SF}$	Stack Full Output (Active LOW)
$\overline{SE}$	Stack Empty Output (Active LOW)

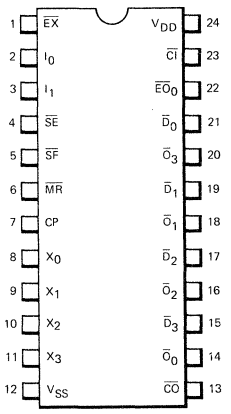
*A Trademark of Fairchild Camera and Instrument Corporation

LOGIC SYMBOL



V_{DD} = Pin 24
V_{SS} = Pin 12

CONNECTION DIAGRAM
DIP (TOP VIEW)



FUNCTIONAL DESCRIPTION — As shown in the Block Diagram, the 34706 consists of an input multiplexer, a 16 x 4 RAM with output latches addressed by the Stack Pointer (SP), an incrementor, control logic, and output buffers. The 34706 is organized around three 4-bit buses; the Input Data (D) Bus ($\overline{D}_0$, $\overline{D}_1$, $\overline{D}_2$, $\overline{D}_3$), Output Data (O) Bus ($\overline{O}_0$, $\overline{O}_1$, $\overline{O}_2$, $\overline{O}_3$) and the Address (X) Bus (X_0, X_1, X_2, X_3). The 34706 implements four instructions as determined by inputs I_0 and I_1. (See Table I). The O-bus is derived from the RAM output latches and enabled by the active LOW Output Enable ($\overline{EO}_0$) input. The X-bus is also derived from the output latches; it is enabled internally during the Fetch Instruction. Execution of instructions is controlled by the Execute ($\overline{EX}$) and Clock (CP) inputs.

FETCH OPERATION — The Fetch Operation places the content of the current Program Counter (PC) on the X-bus. If the Carry In ($\overline{CI}$) is LOW, the current PC is incremented in preparation for the next Fetch. If $\overline{CI}$ is HIGH, the value of the current program is unchanged, (Iterative Fetch).

The instruction code is set up on the I lines when CP is HIGH. The active level LOW Execute ($\overline{EX}$) is normally set up at this time as well. The control logic interprets I_0 and I_1 and selects the incrementor output as the data source to the RAM via the input multiplexer. The current PC value is loaded into the latches and is available on the O-bus if $\overline{EO}_0$ is LOW. When CP is LOW (assuming $\overline{EX}$ is also LOW) the output latches are disabled from following the RAM output and the X-bus Output buffers are enabled, applying the current PC to the X-bus. The output of the incrementor is written into the RAM during the period when CP and $\overline{EX}$ are LOW. If $\overline{CI}$ is LOW, the value stored in the current PC, plus one, is written into the RAM. If $\overline{CI}$ is HIGH, the current PC is not incremented. Carry Out ($\overline{CO}$) is LOW when the contents of the current PC is at its maximum, i.e., all ones. When CP or $\overline{EX}$ goes HIGH, writing into the RAM is inhibited and the Address buffers ($X_0 - X_3$) are disabled.

BRANCH OPERATION — During a Branch Operation, the Data Inputs ($D_0 - D_3$) are loaded into the current program counter.

The instruction code and the $\overline{EX}$ input are set up when CP is HIGH. The stack pointer remains unchanged. When CP goes LOW (assuming $\overline{EX}$ is LOW), the D-bus inputs are written into the current PC. The X-bus drivers are not enabled during a Branch Operation.

CALL OPERATION — During a Call Operation the content of the data bus is loaded into the top location of the stack and all previous PC values are effectively moved down one level.

The instruction code and the $\overline{EX}$ input are set up when CP is HIGH. When $\overline{EX}$ is LOW, a "one" is added to the stack pointer value thus incrementing the RAM address. When CP is LOW (assuming $\overline{EX}$ is LOW), the D-bus inputs are written into this new RAM location. On the LOW-to-HIGH CP transition, the incremented stack pointer value is loaded into the stack pointer register. When the RAM address is "1111" the Stack Full output ($\overline{SF}$) is LOW, indicating that no further Call Operations should be initiated. If an additional Call Operation is performed $\overline{SP}$ is incremented to "0000", the contents of that location will be written over, $\overline{SF}$ will go HIGH and the Stack Empty ($\overline{SE}$) will go LOW.

The X-bus drivers are not enabled during a Call Operation.

RETURN OPERATION — During the Return Operation the previous PC is "popped" to become the current PC.

The instruction is set up when CP is HIGH. When $\overline{EX}$ is LOW, a "one" is subtracted from the stack pointer value, thus decrementing the RAM address, presenting the "popped" PC value through the enabled latches to the three-state O-bus drivers. When CP is LOW, the latches are disabled, thereby holding the new current value of the PC. On the LOW-to-HIGH CP transition the decremented stack pointer value is loaded into the stack pointer register.

The X-bus drivers are not enabled during a return operation.

When the RAM address is "0000", the Stack Empty output ($\overline{SE}$) is LOW, indicating that no further return operations should be initiated. If an additional Return Operation is performed, $\overline{SP}$ is decremented to "1111", the $\overline{SE}$ will go HIGH and the Stack Full output ($\overline{SF}$) will go LOW. Operation of the active LOW Master Reset ($\overline{MR}$) causes the $\overline{SP}$ to be reset and the contents of that RAM location (0000) to be cleared. The Stack Empty ($\overline{SE}$) output goes LOW. This operation overrides all other inputs.

MULTIPLE 34706 OPERATION — The 34706 may be expanded to any word length in multiples of four without external logic. The connection for expanded operation is shown in Figure 1. Carry In ($\overline{CI}$) and Carry Out ($\overline{CO}$) are connected to provide automatic increment of the current program counter during the Fetch Operation. The $\overline{CI}$ input of the least significant 34706 is tied LOW to ground; the $\overline{CO}$ input of the least significant 34706 is connected to the $\overline{CI}$ input of the next significant 34706.

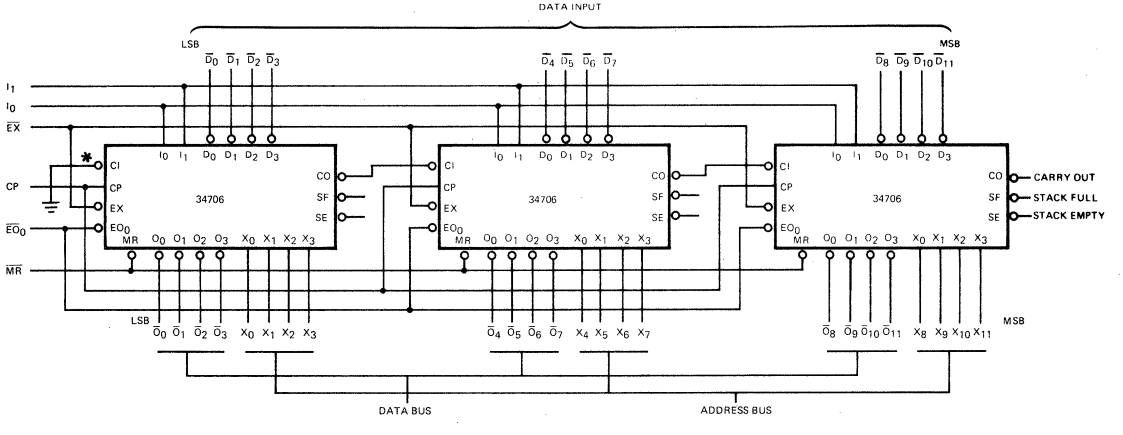


FIGURE 1. 34706 EXPANSION A 16 BY 12 PROGRAM STACK

*Tie to V_{DD} to disable automatic increment.

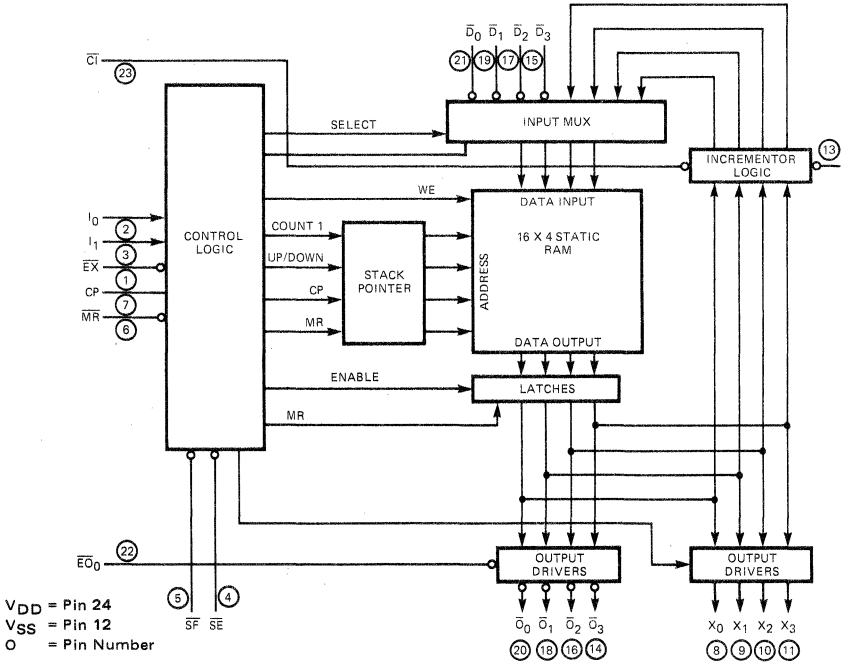
4

TABLE I
INSTRUCTION SET FOR THE 34706

I_1	I_0	INSTRUCTION	INTERNAL OPERATION	X-BUS	O-BUS (WITH $\overline{EO}_0$ LOW)
L	L	Return (Pop)	Decrement Stack Pointer	Disabled	New ("popped") Program Counter value when $\overline{EX}$ goes LOW
L	H	Branch (Load PC)	Load D-Bus into current Program Counter location	Disabled	Current Program Counter until CP goes HIGH again, then updated with newly entered PC value
H	L	Call (Push)	Increment Stack Pointer & Load D-Bus into new Program Counter Location	Disabled	Current Program Counter until CP goes HIGH again, then updated with newly entered PC value
H	H	Fetch (Increment PC)	Increment Current Program Counter if $\overline{CI}$ is LOW	Current Program Counter while both CP & $\overline{EX}$ are LOW, disabled while CP or $\overline{EX}$ is HIGH	Current Program Counter until CP goes HIGH again, then updated with incremented PC value

H = HIGH Level
L = LOW Level

34706 BLOCK DIAGRAM



34707
DATA ACCESS REGISTER
FAIRCHILD CMOS MACROLOGIC*

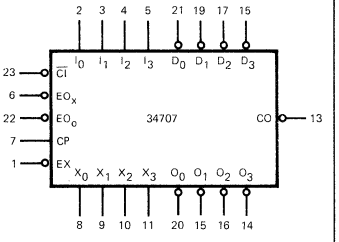
DESCRIPTION — The 34707 Data Access Register (DAR) performs memory address arithmetic for RAM resident stack applications. It contains three 4-bit registers intended for program counter (R_0), stack pointer (R_1) and operand address (R_2). The 34707 implements 16 instructions (see Table 1) which allow either pre or post decrement/increment and register-to-register transfer in a single clock cycle. It is expandable in 4-bit increments and can operate at a 2 MHz microinstruction rate on a 16-bit word. The 3-state outputs are provided for bus oriented applications. The 34707 is packaged in the new slim 24-pin Dual In-Line package.

- **16 INSTRUCTIONS FOR ADDRESS MANIPULATION**
- **EXPANDABLE IN 4-BIT INCREMENTS**
- **OPTIONAL PRE OR POST INCREMENT/DECREMENT**
- **3-STATE OUTPUTS**
- **2 MHz MICROINSTRUCTION RATE ON A 16-BIT WORD**
- **NEW SLIM 24-PIN DIP**

PIN NAMES

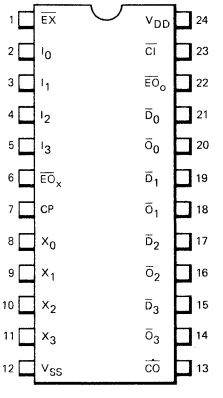
I_0-I_3	Instruction Word Inputs
$\overline{D_0}$-$\overline{D_3}$	Data Inputs (Active LOW)
CP	Clock Input (L → H Edge-Triggered)
$\overline{CI}$	Carry Input (Active LOW)
$\overline{CO}$	Carry Output (Active LOW)
$\overline{EX}$	Execute Input (Active LOW)
$\overline{EO_x}$	Address Output Enable Input (Active LOW)
$\overline{EO_o}$	Data Output Enable Input (Active LOW)
X_0-X_3	Address Outputs
$\overline{O_0}$-$\overline{O_3}$	Data Outputs (Active LOW)

LOGIC SYMBOL



V_{DD} = Pin 24
V_{SS} = Pin 12

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

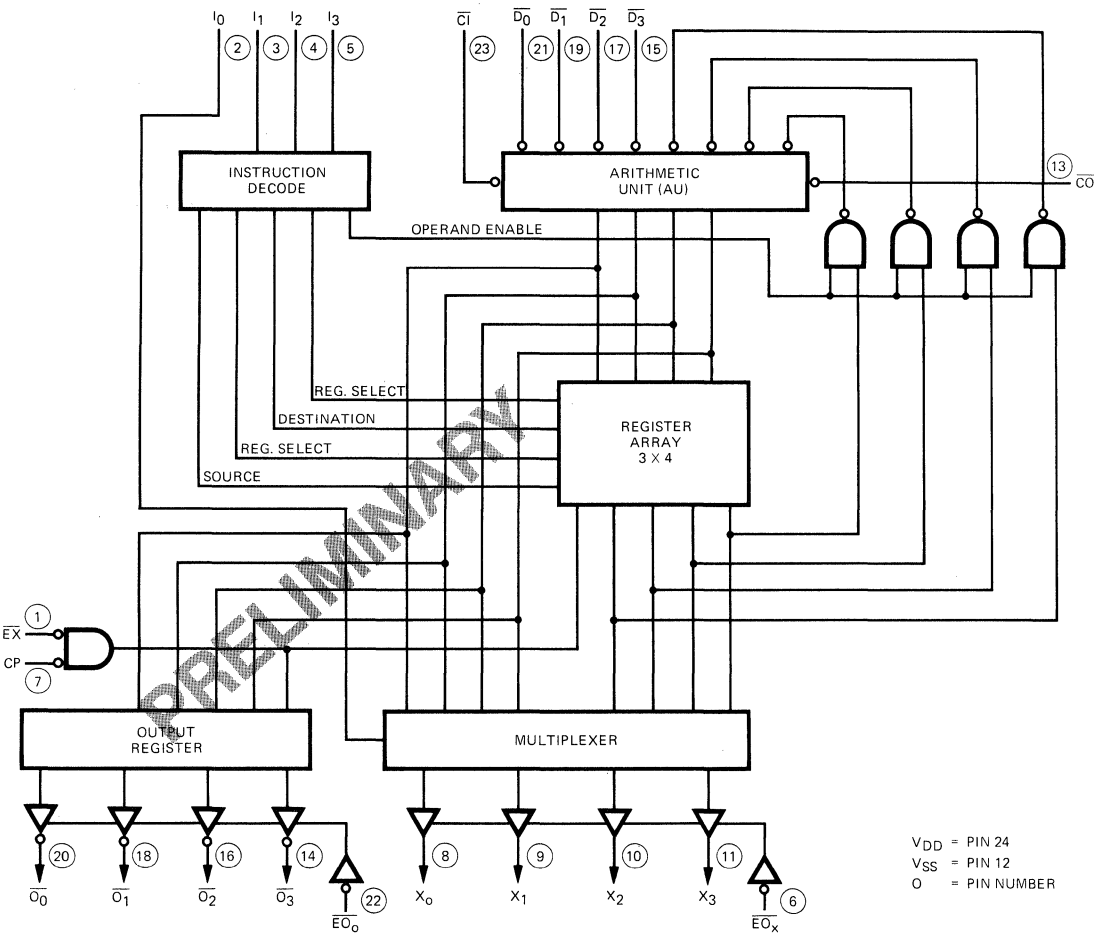
TABLE 1
INSTRUCTION SET FOR THE 34707

INSTRUCTION				COMBINATORIAL FUNCTION	SEQUENTIAL FUNCTION OCCURRING
I_3	I_2	I_1	I_0	AVAILABLE ON THE X-BUS	ON THE NEXT RISING CP EDGE
L	L	L	L	R_0	R_0 plus D plus CI → R_0 and 0-register
L	L	L	H	R_0 plus D plus CI	
L	L	H	L	R_0	R_0 plus D plus CI → R_1 and 0-register
L	L	H	H	R_0 plus D plus CI	
L	H	L	L	R_0	R_0 plus D plus CI → R_2 and 0-register
L	H	L	H	R_0 plus D plus CI	
L	H	H	L	R_1	R_1 plus D plus CI → R_1 and 0-register
L	H	H	H	R_1 plus D plus CI	
H	L	L	L	R_2	D plus CI → R_2 and 0-register
H	L	L	H	D plus CI	
H	L	H	L	R_0	D plus CI → R_0 and 0-register
H	L	H	H	D plus CI	
H	H	L	L	R_2	R_2 plus D plus CI → R_2 and 0-register
H	H	L	H	R_2 plus D plus CI	
H	H	H	L	R_1	D plus CI → R_1 and 0-register
H	H	H	H	D plus CI	

L = LOW Level H = HIGH Level

*A Trademark of Fairchild Camera and Instrument Corporation.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION – The 34707 contains a 4-bit slice of three registers (R_0, R_1, R_2), a 4-bit adder, a 3-state address output buffer (X_0-X_3), and a separate output register with 3-state buffers ($\overline{O_0}$-$\overline{O_3}$), that can put the register contents on the data bus (refer to the Block Diagram). The DAR can perform 16 instructions, selected by I_0-I_3, as listed in Table 1.

OPERATION – The 34707 operates on a single clock. CP and $\overline{EX}$ are inputs to a two input, active LOW AND gate. For normal operation $\overline{EX}$ is LOW. A microcyle starts as the clock goes HIGH. Data inputs $\overline{D_0}$-$\overline{D_3}$ are applied to the Adder as one of the operands. Three (I_1, I_2, I_3) of the four instruction lines select which of the three registers, if any, is to be used as the other operand. The next LOW-to-HIGH CP transition writes the result from the Adder into one register (R_0, R_1, R_2) and into the output register provided $\overline{EX}$ is LOW. If the I_0 instruction input is HIGH, the multiplexer routes the result from the Adder to the 3-state buffer controlling the address bus (X_0-X_3) independent of $\overline{EX}$ and CP. If I_0 is LOW, the multiplexer routes the output of the selected register directly into the 3-state buffer controlling the address bus (X_0-X_3), independent of $\overline{EX}$ and CP.

34707 ARRAYS – The 34707 is organized as a 4-bit register slice. The active LOW $\overline{CI}$ and $\overline{CO}$ lines allow ripple-carry expansion over longer word lengths.

APPLICATIONS – In a typical application, the register utilization in the DAR may be as follows: R_0 is the program counter (PC), R_1 is the stack pointer (SP) for memory resident stacks and R_2 contains the operand address. For an instruction fetch, PC can be gated on the X-bus while it is being incremented (i.e., D-bus = 1). If the instruction fetched calls for an effective address for execution, which is displaced from the PC, the displacement can be added to the PC and loaded into R_2 during the next microcycle.

34710

16 × 4 BIT CLOCKED RAM WITH 3-STATE OUTPUT REGISTER

FAIRCHILD CMOS MACROLOGIC*

DESCRIPTION — The 34710 is a register-oriented 64-Bit Read/Write Memory organized as 16 words by four bits. An edge-triggered 4-bit output register allows new data to be written while the previous data is held. The 3-state data outputs provide flexibility and make the 34710 compatible with the other bus oriented circuits in the CMOS Macrologic family.

The 34710 consists of a 16 x 4-bit RAM selected by the four Address Inputs (A_0-A_3) and an edge-triggered 4-bit output register with 3-state output buffers.

WRITE OPERATION — When the three control inputs; Write Enable ($\overline{WE}$), Chip Select ($\overline{CS}$), and Clock (CP), are LOW the information on the Data Inputs ($\overline{D}_0$-$\overline{D}_3$) is written into the memory location selected by the Address Inputs (A_0-A_3). If the input data changes while $\overline{WE}$, $\overline{CS}$, and CP are LOW, the contents of the selected memory location follows these changes, provided set-up time criteria are met.

READ OPERATION — Whenever $\overline{CS}$ is LOW and CP goes from LOW-to-HIGH, the contents of the memory location selected by the Address Inputs (A_0-A_3) is edge-triggered into the Output Register.

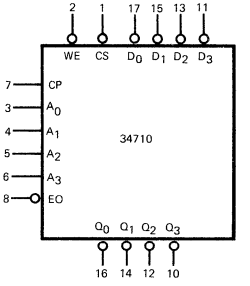
A 3-State Output Enable ($\overline{EO}$) controls the output buffers. When $\overline{EO}$ is HIGH the four Outputs ($\overline{Q}_0$-$\overline{Q}_3$) are in a high impedance or OFF state; when $\overline{EO}$ is LOW, the Outputs are determined by the state of the output register.

- **EDGE-TRIGGERED OUTPUT REGISTER**
- **3-STATE OUTPUTS**
- **OPTIMIZED FOR REGISTER STACK OPERATION**
- **18-PIN PACKAGE**

PIN NAMES

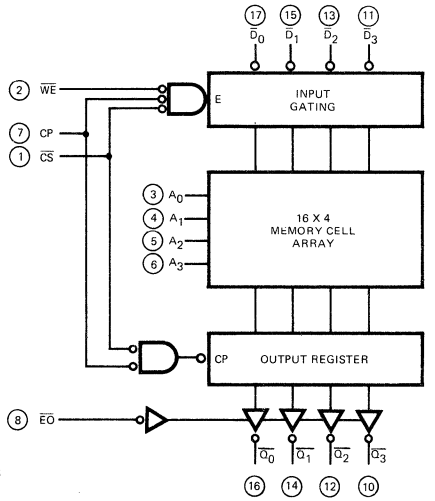
A_0-A_3	Address Inputs
$\overline{D}_0$-$\overline{D}_3$	Data Inputs (Active LOW)
$\overline{CS}$	Chip Select (Active LOW) Input
$\overline{EO}$	Output Enable (Active LOW) Input
$\overline{WE}$	Write Enable (Active LOW) Input
CP	Clock Input (L → H Edge-Triggered)
$\overline{Q}_0$-$\overline{Q}_3$	Buffered Outputs (Active LOW)

LOGIC SYMBOL



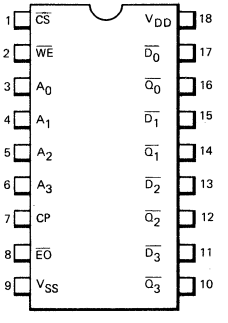
V_{DD} = Pin 18
V_{SS} = Pin 9

BLOCK DIAGRAM



V_{DD} = Pin 18
V_{SS} = Pin 9
○ = Pin Numbers

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

*A Trademark of Fairchild Camera and Instrument Corporation.

34731

QUAD 64-BIT STATIC SHIFT REGISTER

FAIRCHILD CMOS LSI

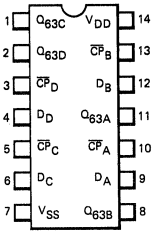
DESCRIPTION — The 34731 is a Quad 64-Bit Shift Register each with separate Serial Data Inputs (D_A-D_D), Clock Inputs ($\overline{CP}_A$-$\overline{CP}_D$) and Data Outputs (Q_{63A}-Q_{63D}) from the 64th register position.

Information present on the Serial Data Inputs is shifted into the first register position and all the data in the register is shifted one position to the right on a HIGH-to-LOW transition of the Clock Inputs ($\overline{CP}_A$-$\overline{CP}_D$).

Low impedance outputs are provided for direct interface to TTL.

- **FREQUENCIES UP TO 4 MHz AT V_{DD} = 10 V**
- **SERIAL-TO-SERIAL DATA TRANSFER**
- **SEPARATE CLOCK INPUTS, DATA INPUTS AND FULLY BUFFERED OUTPUTS FOR EACH REGISTER**
- **DIRECT INTERFACE TO TTL**
- **14-PIN PACKAGE**

CONNECTION DIAGRAM
DIP (TOP VIEW)

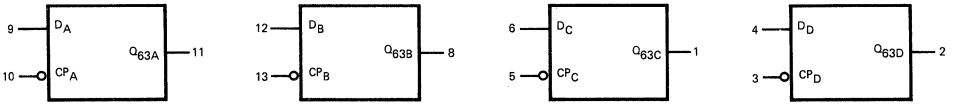


NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

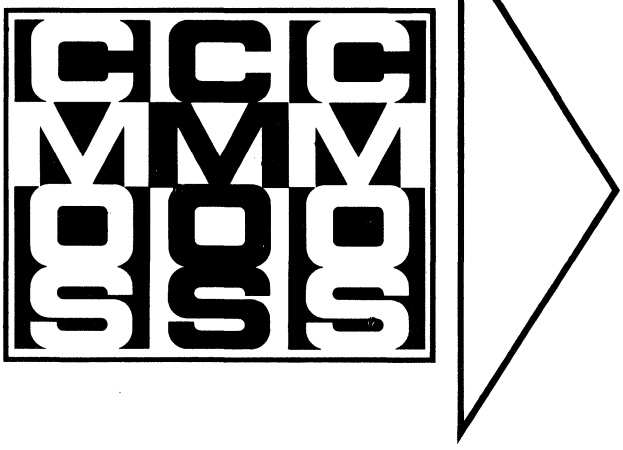
PIN NAMES

D_A-D_D	Serial Data Inputs
$\overline{CP}_A$-$\overline{CP}_D$	Clock Input (H→L Edge-Triggered)
Q_{63A}-Q_{63D}	Buffered Outputs from the 64th Register Position

LOGIC SYMBOL



V_{DD} = Pin 14
V_{SS} = Pin 7



BIPOLAR INTERFACE CIRCUITS FOR CMOS

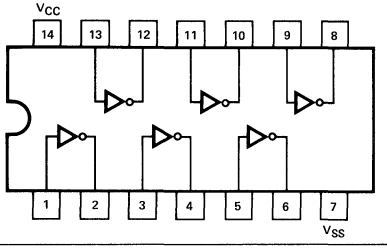
CMOS TO TTL DRIVER

9LS04 Hex Inverter
(Reference: Fairchild Low Power TTL Data Book)

When multi-TTL drive capability is required, the CMOS 34049 and 34050 Hex Buffers can be used to drive two standard TTL loads with typical delays of 45 ns (V_{DD} = 5 V). However, the 9LS04 drives five standard TTL loads with typical delays of 5 ns. The 9LS04 must be operated from a 5 V TTL supply, but it can accept input voltage to 11 V, allowing its use with CMOS operated up to 10 V.

- **34000 COMPATIBLE INPUTS**
- **DRIVES FIVE TTL LOADS**
- **5 ns DELAY**
- **ACCEPTS 11 V INPUTS**
- **2 mW PER INVERTER**

9LS04 LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



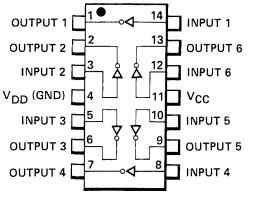
MOS TO LED DIGIT DRIVER

9664 MOS to LED Digit Driver
(Reference: Fairchild 9664 Data Sheet)

This driver is ideal for driving high current devices such as LEDs, relays and lamps. High input impedance allows direct drive from 34000 CMOS devices; however, there is some degradation in logic level at the CMOS output. The 9664 is specified to 10 V operation, the 9664A to 20 V.

- **150 mA SINK CAPABILITY**
- **CMOS COMPATIBLE INPUTS**
- **VERY LOW STANDBY POWER**
- **SIX HIGH GAIN DARLINGTON CIRCUITS**
- **10 AND 20 V OPERATION**

9664/9664A LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



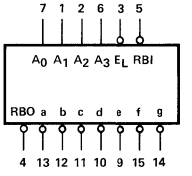
CMOS TO 7-SEGMENT LED DISPLAY

9374 7-Segment Decoder/Driver/Latch
(Reference: Fairchild 9374 Data Sheet)

This bipolar device contains latches for storage, a 7-segment decoder and 15 mA constant current drivers. The 9374 must operate at 5 V; its inputs are also limited to 5 V.

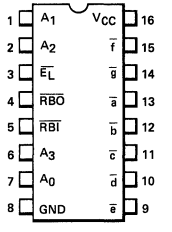
- **HIGH SPEED INPUT LATCHES FOR DATA STORAGE**
- **15 mA CONSTANT CURRENT SINK CAPABILITY TO DIRECTLY DRIVE COMMON ANODE LED DISPLAYS**
- **INCREASES INCANDESCENT DISPLAY LIFE**
- **DATA INPUT LOADING ESSENTIALLY ZERO WHEN LATCH DISABLED**
- **AUTOMATIC RIPPLE BLANKING FOR SUPPRESSION OF LEADING EDGE ZEROS AND/OR TRAILING EDGE ZEROS**

9374
LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

9374
CONNECTION DIAGRAM



5

BIPOLAR INTERFACE CIRCUITS FOR CMOS (Cont'd)

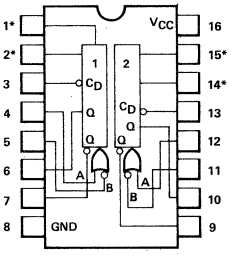
ONE-SHOT MULTIVIBRATOR

96L02 Low Power Dual
Retriggerable Resettable Monostable Multivibrator
(Reference: Fairchild Low Power TTL Book)

The 96L02 is pin and function compatible with the 34528 Dual Monostable and exhibits improved stability and speed. It is usable in 5 V CMOS systems.

- **TYPICAL POWER DISSIPATION OF 25 mW/ONE SHOT**
- **50 ns TYPICAL PROPAGATION DELAY**
- **RETRIGGERABLE 0 TO 100% DUTY CYCLE**
- **34000 COMPATIBLE INPUTS**
- **OPTIONAL RETRIGGER LOCK-OUT CAPABILITY**
- **PULSE WIDTH COMPENSATED FOR V_{CC} AND TEMPERATURE VARIATIONS**
- **RESETTABLE**

96L02 LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



*Leads for external timing

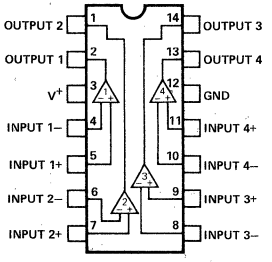
VOLTAGE COMPARATOR

μA775-Quad Comparator
(Reference: Fairchild μA775 Data Sheet)

In a CMOS system it may be necessary to detect differences between two voltage levels and convert to logic levels. The μA775 Quad Comparator is capable of operating over the CMOS power supply range. These comparators have a unique characteristic in that the input common mode voltage range includes ground, even though operated from a single power supply voltage. Applications include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators and wide range V_{CO}.

- **SINGLE SUPPLY OPERATION—+2.0 V TO +36 V**
- **COMPARES VOLTAGES NEAR GROUND POTENTIAL**
- **LOW CURRENT DRAIN—700 μA TYPICAL**
- **COMPATIBLE WITH ALL FORMS OF CMOS**
- **LOW INPUT BIAS CURRENT—25 nA TYPICAL**
- **LOW INPUT OFFSET CURRENT—25 nA**
- **LOW OFFSET VOLTAGE—5 mV MAX**

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



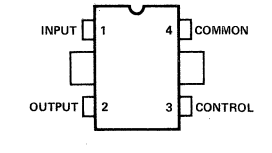
POWER SUPPLY REGULATOR

μA78MG 4-Terminal Regulator
(Reference: Fairchild μA78 MG • μA79 MG Data Sheet)

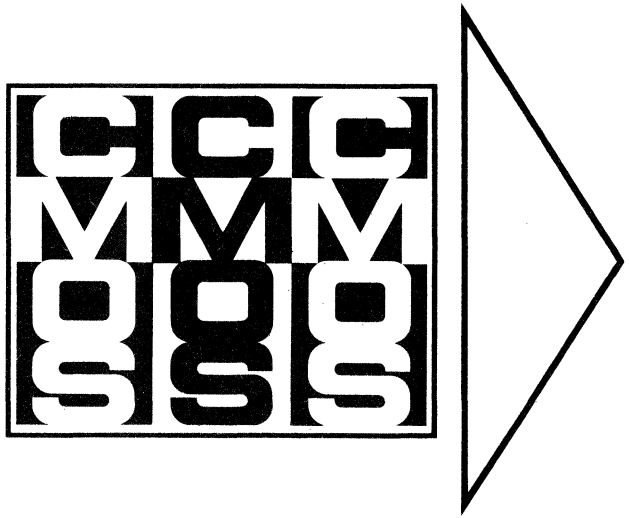
This single compact regulator with its 500 mA capability is sufficient for all but the very largest CMOS systems. The adjustable output voltage feature allows fine tuning of system speed product.

- **OUTPUT CURRENT IN EXCESS OF 0.5 A**
- **POSITIVE OUTPUT VOLTAGE 5 TO 30 V**
- **INTERNAL THERMAL OVERLOAD PROTECTION**
- **INTERNAL SHORT CIRCUIT CURRENT PROTECTION**
- **OUTPUT SAFE AREA PROTECTION**
- **POWER MINI DUAL IN-LINE PACKAGE**

μA78 MGCONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE: Heat sink tabs connected to common

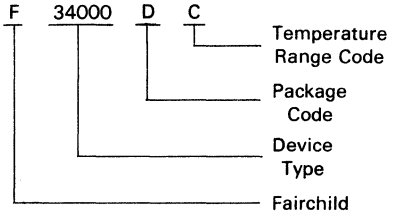


ORDER AND PACKAGE INFORMATION

Fairchild CMOS circuits may be ordered using a simplified purchasing code where the package style and temperature range are defined as follows:

PACKAGE STYLE

D = Dual In-Line — Ceramic (hermetic)
P = Dual In-Line — Plastic
F = Flatpak



In order to accommodate varying die sizes and numbers of leads (14, 16, 24, etc.), a number of different package forms are required. The Package Information list on the following pages indicates the specific package codes currently used for each device type. The detailed package outline corresponding to each package code is shown at the end of this section.

Temperature Range

Two Basic temperature grades are in common use: C = Commercial-Industrial, 40°C to +85°C; M = Military, -55°C to +125 'C. Exact values and conditions are indicated on the data sheets.

Examples

(a) 34014FM
This number code indicates a 34014 Register in a Flatpak with military temperature rating.

(b) 34720DC
This number code indicates a 34720 256 x 1 RAM in a ceramic Dual In-Line package with commercial temperature rating.

Device Identification/Marking

All Fairchild standard catalog CMOS circuits will be marked as follows:

F Device Type XX
Date Code

DEVICE	MILITARY (M) -55°C to +125°C		COMMERCIAL (C)/INDUSTRIAL -40°C to +85°C		
	CERAMIC DIP (D)	FLATPAK (F)	CERAMIC DIP (D)	PLASTIC DIP (P)	FLATPAK (F)
34001	6A	3I	6A	9A	3I
34002	6A	3I	6A	9A	3I
34011	6A	3I	6A	9A	3I
34012	6A	3I	6A	9A	3I
34013	6A	3I	6A	9A	3I
34014	6B	4L	6B	9B	4L
34015	6B	4L	6B	9B	4L
34016	6A	3I	6A	9A	3I
34017	6B	4L	6B	9B	4L
34019	6B	4L	6B	9B	4L
34020	6B	4L	6B	9B	4L
34021	6B	4L	6B	9B	4L
34023	6A	3I	6A	9A	3I

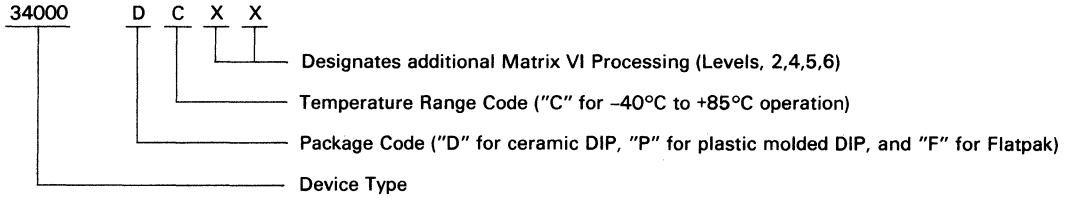
ORDER AND PACKAGE INFORMATION

DEVICE	MILITARY (M) -55°C to +125°C		COMMERCIAL (C)/INDUSTRIAL -40°C to +85°C		
	CERAMIC DIP (D)	FLATPAK (F)	CERAMIC DIP (D)	PLASTIC DIP (P)	FLATPAK (F)
34024	6A	3I	6A	9A	3I
34025	6A	3I	6A	9A	3I
34027	6B	4L	6B	9B	4L
34028	6B	4L	6B	9B	4L
34029	6B	4L	6B	9B	4L
34030	6A	3I	6A	9A	3I
34035	6B	4L	6B	9B	4L
34040	6B	4L	6B	9B	4L
34042	6B	4L	6B	9B	4L
34049	6B	4L	6B	9B	4L
34050	6B	4L	6B	9B	4L
34051	6B	4L	6B	9B	4L
34052	6B	4L	6B	9B	4L
34066	6A	3I	6A	9A	3I
34068	6A	3I	6A	9A	3I
34069	6A	3I	6A	9A	3I
34070	6A	3I	6A	9A	3I
34071	6A	3I	6A	9A	3I
34077	6A	3I	6A	9A	3I
34078	6A	3I	6A	9A	3I
34081	6A	3I	6A	9A	3I
34085	6A	3I	6A	9A	3I
34086	6A	3I	6A	9A	3I
34099	6B	4L	6B	9B	4L
34104	6B	4L	6B	9B	4L
34512	6B	4L	6B	9B	4L
34518	6B	4L	6B	9B	4L
34520	6B	4L	6B	9B	4L
34539	6B	4L	6B	9B	4L
34555	6B	4L	6B	9B	4L
34556	6B	4L	6B	9B	4L
34702	6B	4L	6B	9B	4L
34720	6B	4L	6B	9B	4L
34723	6B	4L	6B	9B	4L
34725	6B	4L	6B	9B	4L
340085	6B	4L	6B	9B	4L
340097	6B	4L	6B	9B	4L
340098	6B	4L	6B	9B	4L
340160	6B	4L	6B	9B	4L
340161	6B	4L	6B	9B	4L
340162	6B	4L	6B	9B	4L
340163	6B	4L	6B	9B	4L
340174	6B	4L	6B	9B	4L
340175	6B	4L	6B	9B	4L
340192	6B	4L	6B	9B	4L
340193	6B	4L	6B	9B	4L
340194	6B	4L	6B	9B	4L
340195	6B	4L	6B	9B	4L

MATRIX VI PROGRAM ORDERING INFORMATION

Matrix VI is a full spectrum/cost effective reliability and quality program for commercial/industrial ICs only. It features six levels of screening/package flows, each tailored to a user's field application/environment and his incoming quality/equipment reliability requirements.

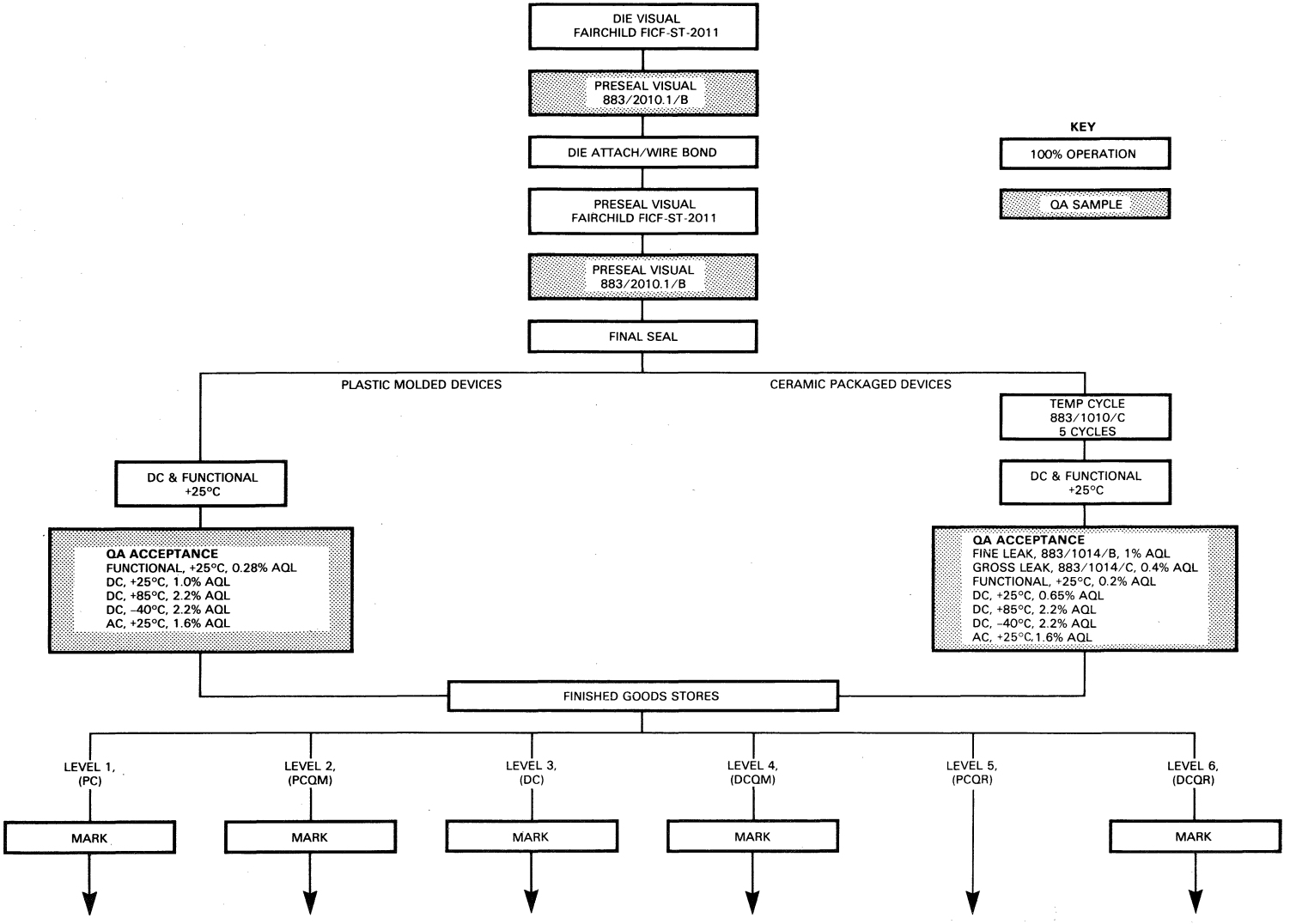
A Matrix VI part number consists of the device type followed by the package code letter, the temperature range code letter, and the Matrix VI code letter (as applicable, see flow chart).

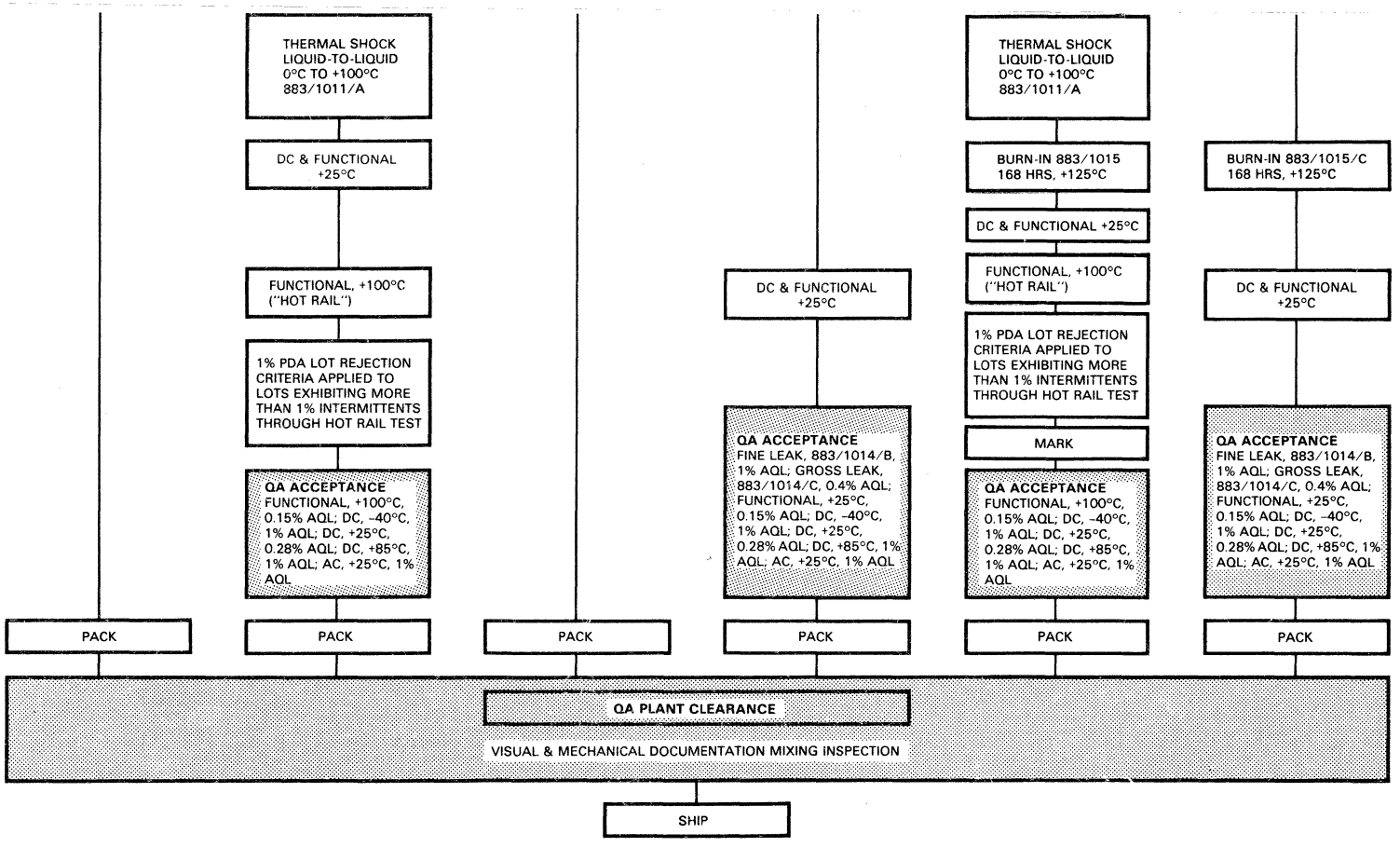


EXAMPLES

(a)	34001PC	Device type 34001, packaged in plastic Dual In-Line (P), in commercial temperature range (C) and processed to Matrix VI Level 1.
(b)	34001PCQM	Device type 34001, packaged in plastic Dual In-Line (P), in commercial temperature range (C(with supplemental Matrix VI Level 2 testing including 100% thermal shock, "hot rail" test and 0.15% AQL functional testing.
(c)	34001DC	Device type 34001, packaged in ceramic Dual In-Line (D), in commercial temperature range and processed to Matrix VI Level 3.
(d)	34001DCQM	Device type 34001, packaged in ceramic Dual In-Line, in commercial temperature range (C) with supplemental Matrix VI Level 4 screening including second 100% DC/functional testing and 0.15% AQL functional testing.
(e)	34001PCQR	Device type 34001, packaged in Dual In-Line, in commercial temperature range (C) with supplemental Matrix VI Level 5 screening including 100% thermal shock, "hot rail" test, 168 hours 125°C burn-in and 0.15% AQL functional testing.
(f)	34001DCQR	Device type 34001, packated in ceramic Dual In-Line, in commercial temperature range with supplemental Matrix VI Level 6 screening including burn-in, three 100% DC/functional tests and 0.15% AQL functional testing.

6 MATRIX VI PROCESS FLOW OPTIONS & COST EFFECTIVENESS



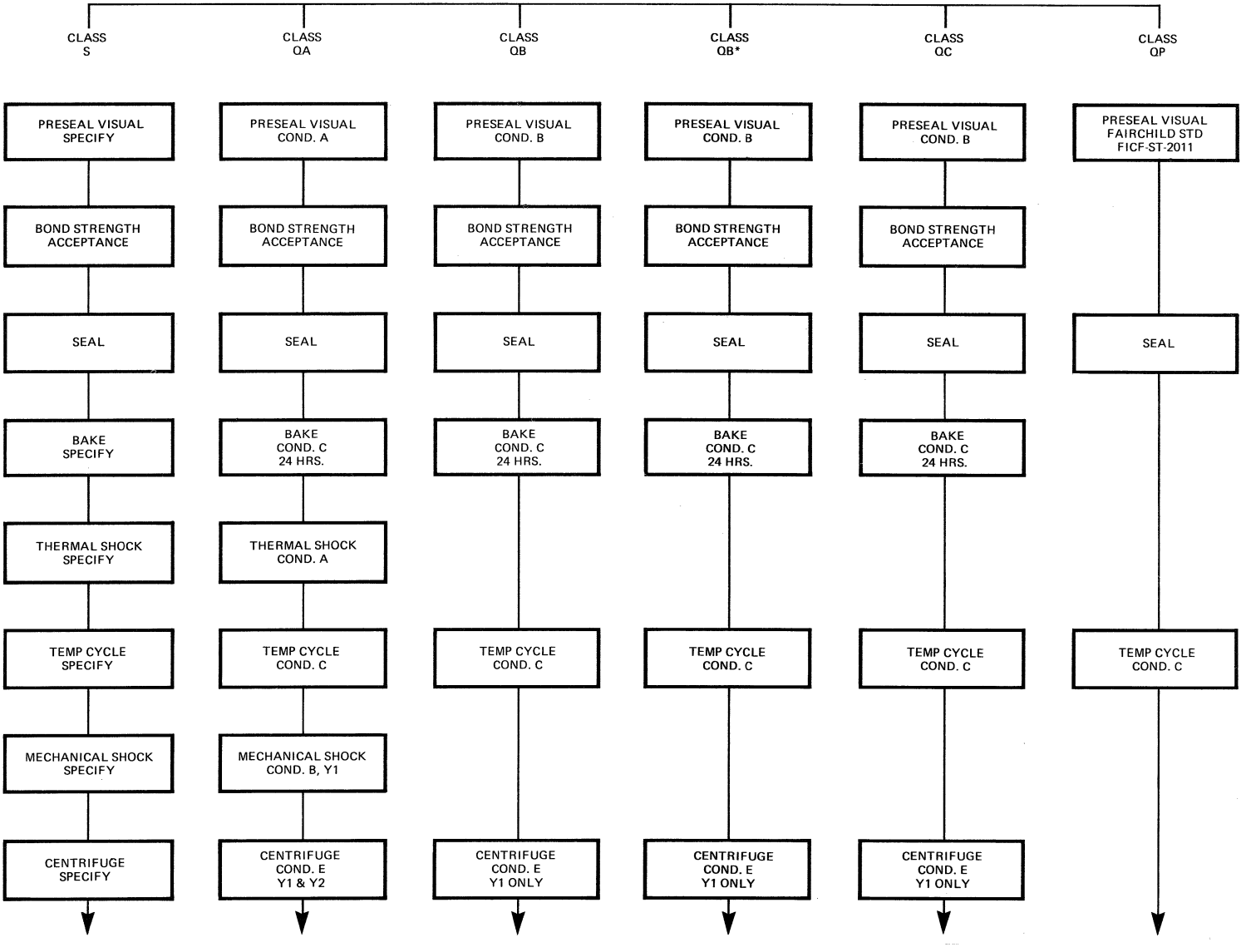


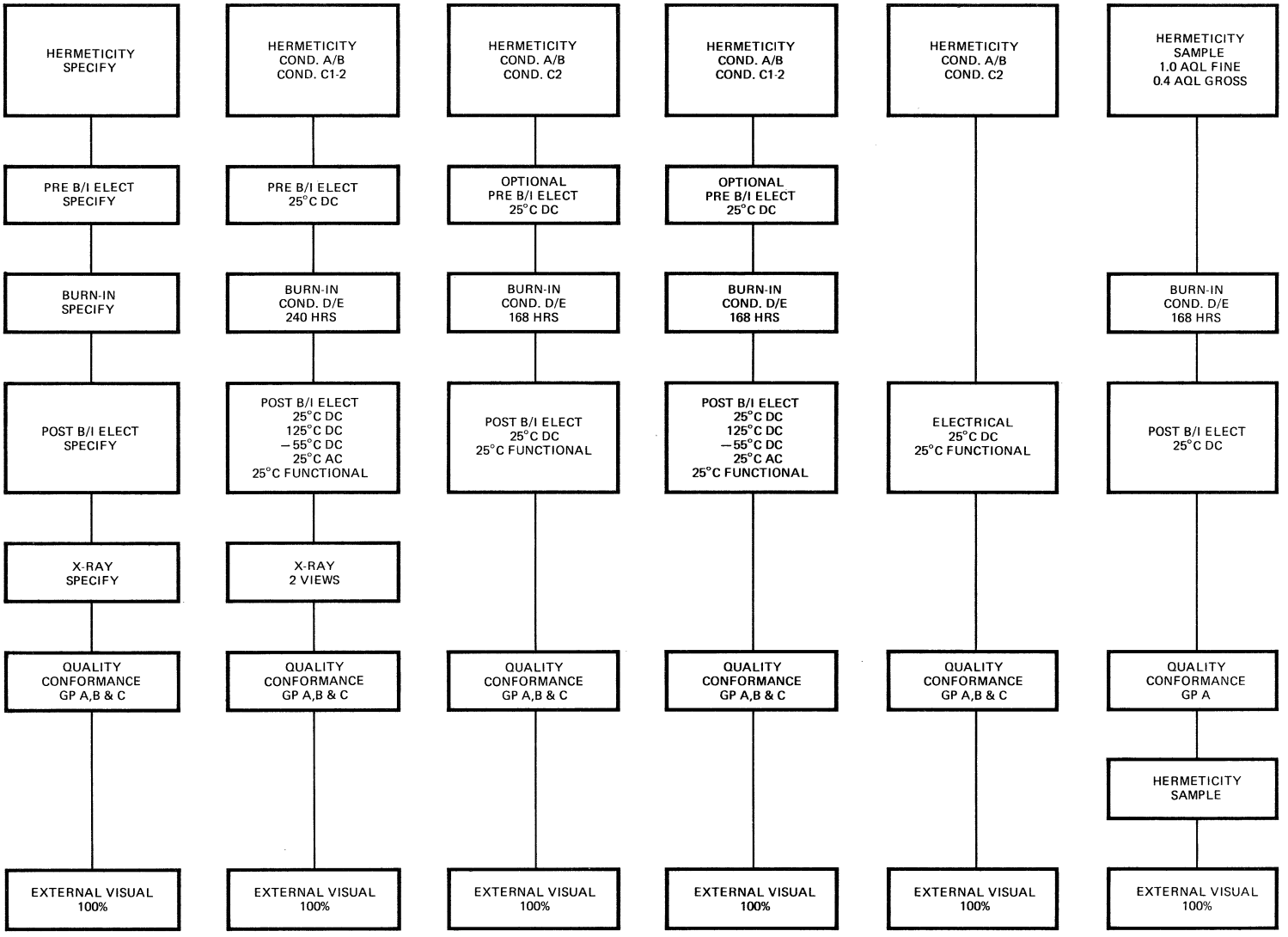
COST EFFECTIVENESS ANALYSIS

RELIABILITY FACTOR = 1X QUALITY GUARANTEE ON FUNCTIONALITY = 0.28% AQL COST SEQUENCE 1	RELIABILITY FACTOR ≅ 1.4X QUALITY GUARANTEE ON FUNCTIONALITY = 0.15% AQL COST SEQUENCE 2	RELIABILITY FACTOR ≅ 2X QUALITY GUARANTEE ON FUNCTIONALITY = 0.2% AQL COST SEQUENCE 3	RELIABILITY FACTOR ≅ 2.3X QUALITY GUARANTEE ON FUNCTIONALITY = 0.15% AQL COST SEQUENCE 4	RELIABILITY FACTOR ≅ 7.5X - 9X (1) QUALITY GUARANTEE ON FUNCTIONALITY = 0.15% AQL COST SEQUENCE 5	RELIABILITY FACTOR ≅ 14X QUALITY GUARANTEE ON FUNCTIONALITY = 0.15% AQL COST SEQUENCE 6

NOTE:
1. Burn-in has the same relative effectiveness for plastic molded devices as for ceramic/hermetic packaged devices. Assuming a controlled (air conditioned and constant power) field application/environment, the reliability factor would be approximately 9X. But should the field application be in a less controlled and power on/off application, the reliability factor would be approximately 7.5X.

UNIQUE 38510





*Upon customer request only. Class B processing in this case includes adding post burn-in testing; dc testing at +125°C and −55°C and ac testing. at 25°C.

PROCESS SCREENING REQUIREMENTS

MIL-STD-883 TEST METHODS	DESCRIPTION
Preseal Visual MTD. 2010.1:	Cond. A Maximum Visual Criteria Cond. B Optimum Visual Criteria FICF-ST-02011 Fairchild Standard
Bond Strength:	Bond strength is monitored on a sample basis three times per shift per mach.
Seal:	Devices are hermetically sealed for compliance to MIL-STD-883 requirements
High Temperature Storage:	Cond. B Tstg = 125°C Specify Time Cond. C Tstg = 150°C Cond. D Tstg = 200°C
Thermal Shock MTD 1011:	Cond. A 0°/100°C 15 cycles Cond. B −55°/125°C
Temperature Cycle MTD 1010:	Cond. B −55°/125°C Cond. C −65°/150°C 10 cycles Cond. D −65°/200°C
Mechanical Shock MTD 2002:	Cond. A 500 Gs 5 Shocks in X_1, X_2 Cond. B 1500 Gs Y_1, Y_2, Z_1 & Z_2
Constant Acceleration MTD 2001:	Cond. D 20000 Gs 2 minute in each Cond. E 30000 Gs X_1 X_2 Y_1 Y_2 Cond. F 50000 Gs Z_1 Z_2
Hermetic Seal MTD 1014:	Cond. A Fine-Helium $5x10^{-8}$ cc/sec Cond. B Fine-Radiflo $5x10^{-8}$ cc/sec Cond. C1 Gross-FC43/Hot 10^{-3} cc/sec Cond. C2 Gross-FC78/Vacuum 10^{-5} cc/sec
Pre Burn-in Electrical (5004.1):	25°C DC electrical testing to remove rejects prior to submission to burn-in screen
Burn-in Screen MTD 1015:	Cond. A, Cond. B, Cond. C Cond. D and Cond. E
Post Burn-in Electrical (5004.1):	Post Burn-in electrical screening to cull out devices which failed as a result of burn-in. Test Parameters may include: 25°C DC, 125°C DC, −55°C DC, 25°C AC and 25°C Functional tests.
Radiography MTD 2012:	6X, 8X magnification and criteria specify number of views
Quality Conformance Inspection MTD 5005:1:	Group A: Electrical Characteristics Group B: Package oriented Tests Group C: Environmental and Life Tests
External Visual MTD 2009:	3X, 20X magnification: Verify dimensions, configuration, lead structure, marking and workmanship

UNIQUE 38510 PROGRAM ORDERING INFORMATION

The Fairchild Unique 38510 Program is written in accordance with MIL-M-38510 and MIL-STD-883

To meet the need of improved reliability in the military market, CMOS Integrated Circuits are available with special processing. Devices ordered to this program are subjected to the 100% screening as outlined in the Process. Devices will be marked in accordance with MIL-M-38510 unless otherwise specified under number Option 6.

UNIQUE 38510 devices are not normally stocked by distributors.

Customer procurement documents should specify the following:

(a) Fairchild Product Code indicating the basic device type and package combination.
(b) The Unique 38510 Device Class. (A, B, C, S, P)
(c) Number and/or Letter Options required.
(d) Special Marking requirements.

The order code number consists of (a) and (b) as shown above. The order code detailed format is shown below.

34000	D	M	QX
DEVICE TYPE	PACKAGE TYPE D = CERAMIC DIP P = PLASTIC DIP F = CERAMIC FLAT	TEMPERATURE RANGE C = −40°C TO +85°C(59X) M = −55°C TO +125°C(51X)	DESIGNATES UNIQUE 38510 PROCESSING IF REQUIRED. SEE DESCRIPTION OF SCREENING REQUIREMENTS

Order code examples are:

34029FMQB	34001DMQC
Class QB Unique 38510	Class QC Unique 38510

Number Options: These options apply to operations performed on each unit delivered:

OPTION 1 Lead form to dimensions in detail specifications, followed by hermetic seal tests.
OPTION 2 Hot solder dip finish.
OPTION 3 Read and record critical parameters before and after burn-in.
OPTION 4 Initial qualification, Group B & C quality conformance not required.
OPTION 5 Radiographic inspection shall be performed on all devices.
OPTION 6 Special marking required.
OPTION 7 Non-conforming variation — refer to procurement documents for details (must be negotiated with factory).

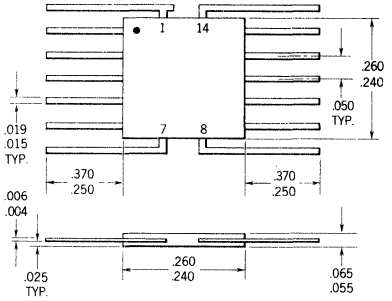
Letter Options: These options apply once per Purchase Order or line item and are considered Test Charges:

OPTION A Group B testing shall be performed on customer's parts.
OPTION B Group C testing shall be performed on customer's parts.
OPTION C Generic data to be supplied from the latest completed lot.
OPTION D Unique 38510 program plan, pertinent to the device family being purchased, shall be supplied.

CERAMIC FLATPAKS — USED ON ALL FM DEVICES

3I

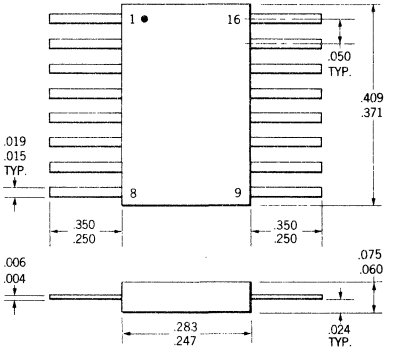
In Accordance with JEDEC TO-86 Outline 14-Lead Cerpak



NOTES: All dimensions in inches
Leads are gold-plated kovar
Package weight is 0.26 gram
Hermetically sealed alumina package
Lead 1 orientation may be either tab or dot

4L

16-Lead Cerpak

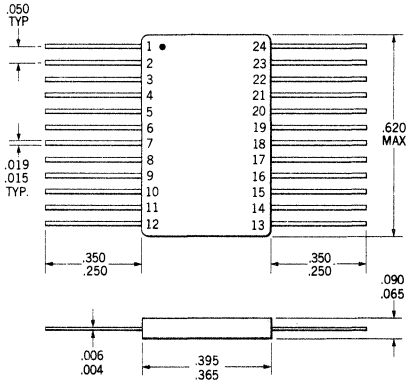


NOTES: All dimensions in inches
Leads are gold-plated kovar
Package weight is 0.4 gram
Hermetically sealed beryllia package

6

4M

24-Lead BeO Cerpak



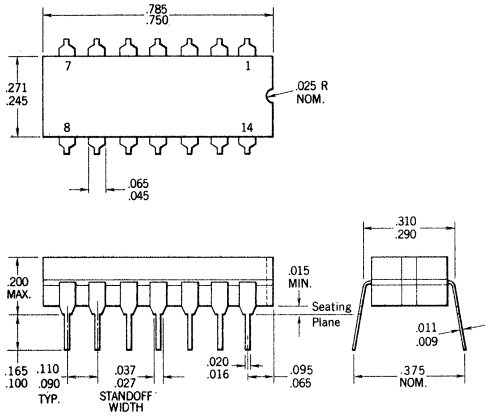
NOTES: All dimensions in inches
Leads are gold-plated kovar
Package weight is 0.8 gram
Hermetically sealed beryllia package

PACKAGE OUTLINES

CERAMIC PACKAGES — USED ON ALL DC AND DM DEVICES

6A

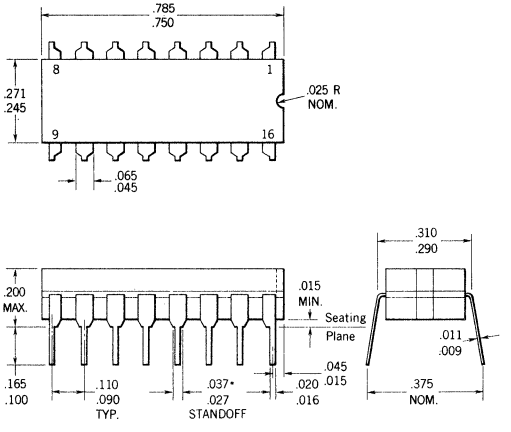
14-Lead Ceramic Dual In-Line



NOTES: All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.0 grams

6B

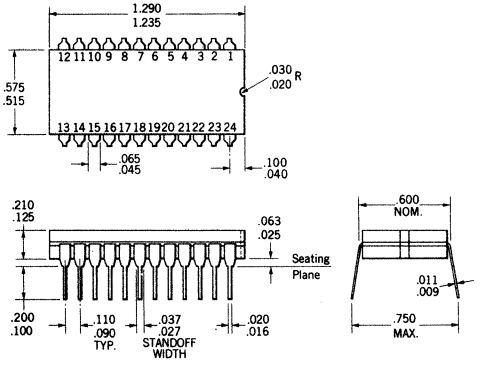
16-Lead Ceramic Dual In-Line



NOTES: All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.0 grams
*The .037/.027 dimension does not apply to the corner leads

6N

24-Lead Ceramic MSI Dual In-Line

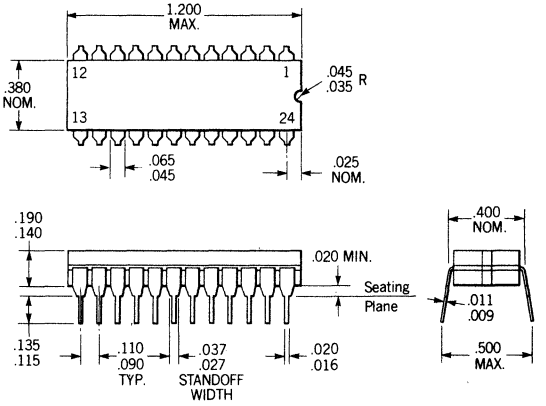


NOTES: All dimensions in inches
Leads are intended for insertion in hole rows on .700" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Leads are tin-plated kovar
Package weight is 6.5 grams
Package material is alumina

CERAMIC PACKAGES — USED ON ALL DC AND DM DEVICES

6Q

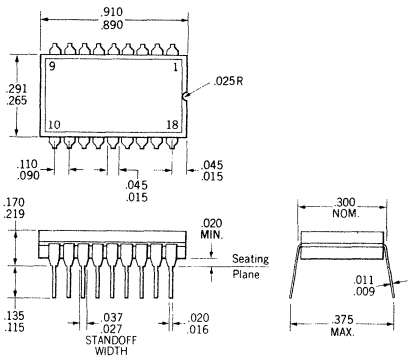
24-Lead Ceramic Dual In-Line



NOTES: All dimensions in inches
Leads are intended for insertion in hole rows on .500" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar

7D

18-Lead Ceramic Dual In-Line



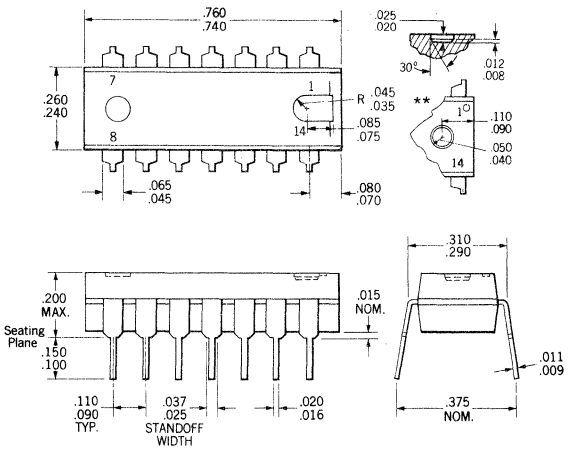
NOTES: All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar

PACKAGE OUTLINES

PLASTIC PACKAGES — USED ON ALL PC DEVICES

9A

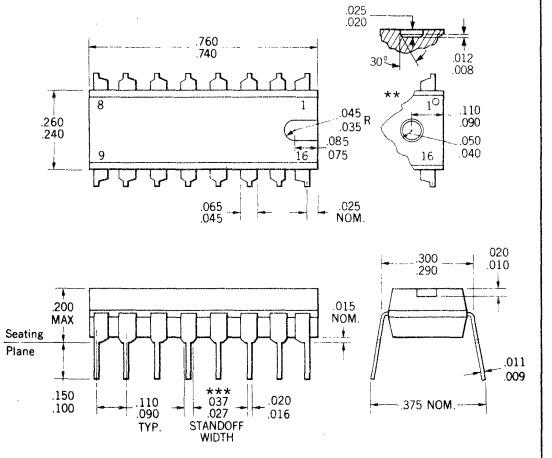
14-Lead Plastic Dual In-Line



NOTES: All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers.
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 0.9 gram
Package material is silicone

9B

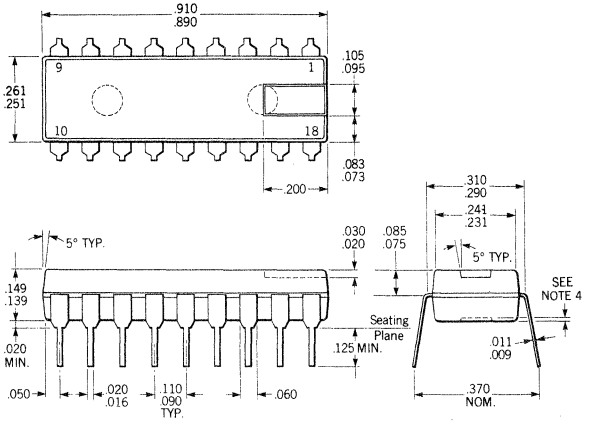
16-Lead Plastic Dual In-Line



NOTES: All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers.
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 0.9 gram
*The .037/.027 dimension does not apply to the corner leads

9M

18-Lead Plastic Dual In-Line

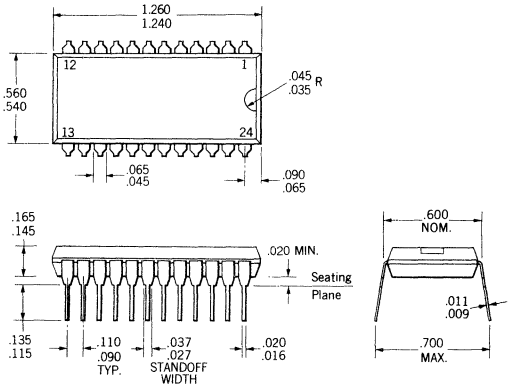


NOTES: All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers.
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar

PLASTIC PACKAGES — USED ON ALL PC DEVICES

9N

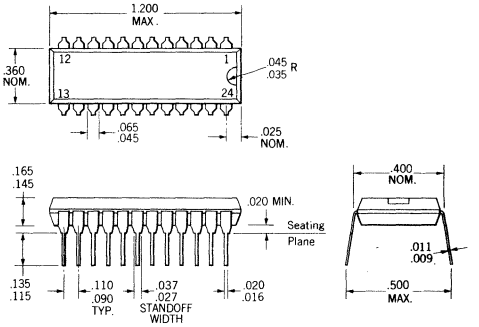
24-Lead Plastic MSI Dual In-Line



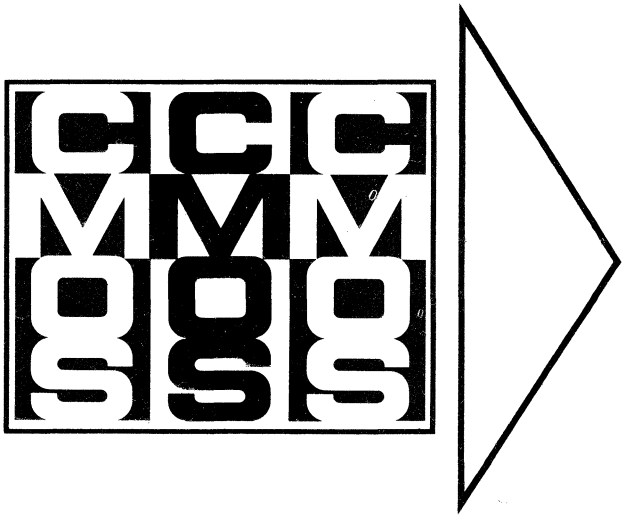
NOTES: All dimensions in inches
Leads are intended for insertion in hole rows on .700" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar

9U

24-Lead Plastic Dual In-Line



NOTES: All dimensions in inches
Leads are intended for insertion in hole rows on .500" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar



FAIRCHILD FRANCHISED DISTRIBUTORS

ALABAMA
HALLMARK ELECTRONICS
4739 Commercial Drive
Huntsville, Alabama 35805
Tel: 205-837-8700 TWX: 810-726-2187

HAMILTON/AVNET ELECTRONICS
805 Oster Drive, N.W.
Huntsville, Alabama 35805
Tel: 205-533-1170
Telex: None — use HAMAVLECB DAL 73-0511
(Regional Hq. in Dallas, Texas)

ARIZONA
HAMILTON/AVNET ELECTRONICS
2615 S. 21st Street
Phoenix, Arizona 85034
Tel: 602-275-7851 TWX: 910-951-1535

LIBERTY ELECTRONICS/ARIZONA
3130 N. 27th Avenue
Phoenix, Arizona 85016
Tel: 602-257-1272 TWX: 910-951-4282

CALIFORNIA
AVNET ELECTRONICS
10916 W. Washington Blvd.
Culver City, California 90230
Tel: 213-558-2345 TWX: 910-340-6364

ELMAR ELECTRONICS
2288 Charleston Rd.
Mountain View, California 94042
Tel: 415-961-3611 TWX: 910-379-6437

HAMILTON ELECTRO SALES
10912 W. Washington Blvd.
Culver City, California 90230
Tel: 213-558-2121 TWX: 910-340-6364

HAMILTON/AVNET ELECTRONICS
575 E. Middlefield Road
Mountain View, California 94040
Tel: 415-961-8600 TWX: 910-379-6486

HAMILTON/AVNET ELECTRONICS
8917 Complex Drive
San Diego, California 92123
Tel: 714-279-2421
Telex: HAMAVELEC SDG 69-5415

G.S. MARSHALL COMPANY
9674 Telstar Avenue
El Monte, California 91731
Tel: 213-686-0141 TWX: 910-587-1565

G.S. MARSHALL COMPANY
17975 Skypark Blvd.
Irvine, California 92707
Tel: 714-556-6400

G.S. MARSHALL COMPANY
8057 Raytheon Rd., Suite 1
San Diego, California 92111
Tel: 714-278-6350 TWX: 910-335-1191

G.S. MARSHALL COMPANY
788 Palomar Avenue
Sunnyvale, California 94086
Tel: 408-732-1100 TWX: 910-339-9263

LIBERTY ELECTRONICS
124 Maryland Street
El Segundo, California 90245
Tel: 213-322-8100 TWX: 910-348-7111

LIBERTY ELECTRONICS/SAN DIEGO
8248 Mercury Court
San Diego, California 92111
Tel: 714-565-9171 TWX: 910-335-1590

COLORADO
ELMAR ELECTRONICS
6777 E. 50th Avenue
Commerce City, Colorado 80022
Tel: 303-287-9611 TWX: 910-936-0770

G.S. MARSHALL COMPANY
5633 Kendall Court
Arvada, Colorado 80002
Tel: 303-423-9670 TWX: 910-938-2902

HAMILTON/AVNET ELECTRONICS
5921 N. Broadway
Denver, Colorado 80216
Tel: 303-534-1212 TWX: 910-931-0510

CONNECTICUT
HAMILTON/AVNET ELECTRONICS
643 Danbury Road
Georgetown, Connecticut 06829
Tel: 203-762-0361
TWX: None — use 710-897-1405
(Regional Hq. in Mt. Laurel, N.J.)

SCHWEBER ELECTRONICS
Finance Drive
Commerce Industrial Park
Danbury, Connecticut 06810
Tel: 203-792-3500

FLORIDA
HALLMARK ELECTRONICS
1302 W. McNab Road
Ft. Lauderdale, Florida 33309
Tel: 305-971-9280 TWX: 510-956-3092

HALLMARK ELECTRONICS
7233 Lake Ellenor Drive
Orlando, Florida 32809
Tel: 305-855-4020 TWX: 810-850-0183

HAMILTON/AVNET ELECTRONICS
4020 North 29th Avenue
Hollywood, Florida 33021
Tel: 305-925-5401 TWX: 510-954-9808

SCHWEBER ELECTRONICS
2830 North 28th Terrace
Hollywood, Florida 33020
Tel: 305-927-0511 TWX: 510-954-0304

GEORGIA
HAMILTON/AVNET ELECTRONICS
6700 Interstate 85 Access Road, Suite 1E
Norcross, Ga. 30071
Tel: 404-448-0800
Telex: None — use HAMAVLECB DAL 73-0511
(Regional Hq. in Dallas, Texas)

SCHWEBER ELECTRONICS
4126 Pleasantdale Rd., Suite 14
Atlanta, Ga. 30340
Tel: 404-449-9170

ILLINOIS
ALLIED ELECTRONICS
1355 Sleepy Hollow Road
Elgin, Illinois 60120
Tel: 312-697-8200
Telex: 72-2465 or 72-2466

KIERULFF ELECTRONICS
9340 Williams Street
Rosemont, Illinois 60018
Tel: 312-678-8560 TWX: 910-227-3166

HAMILTON/AVNET ELECTRONICS
3901 N. 25th Avenue
Schiller Park, Illinois 60176
Tel: 312-678-6310 TWX: 910-227-0060

SCHWEBER ELECTRONICS, INC.
1380 Jarvis Ave.
Elk Grove Village, Ill. 60007
Tel: 312-593-2740 TWX: 910-222-3453

SEMICONDUCTOR SPECIALISTS, INC.
(mailing address)
O'Hare International Airport
P.O. Box 66125
Chicago, Illinois 60666

(shipping address)
195 Spangler Avenue
Elmhurst Industrial Park
Elmhurst, Illinois 60126
Tel: 312-279-1000 TWX: 910-254-0169

INDIANA
PIONEER INDIANA ELECTRONICS, INC.
6408 Castleplace Drive
Indianapolis, Indiana 46250
Tel: 317-849-7300 TWX: 810-260-1794

SEMICONDUCTOR SPECIALISTS, INC.
(mailing address)
Weir Cook Airport
P.O. Box 41630
Indianapolis, Indiana 46241

(shipping address)
1885 Banner Ave.
Indianapolis, Indiana 46241
Tel: 317-243-8271 TWX: 810-341-3126

IOWA
SCHWEBER ELECTRONICS
Suite 302, Executive Plaza
4403 First Avenue S.E.
Cedar Rapids, Iowa 52402
Tel: 319-393-9125

KANSAS
HAMILTON/AVNET ELECTRONICS
37 Lenexa Industrial Center
9900 Pflumm Road
Lenexa, Kansas 66215
Tel: 913-888-8900
Telex: None — use HAMAVLECB DAL 73-0511
(Regional Hq. in Dallas, Texas)

LOUISIANA
STERLING ELECTRONICS CORP.
5029 Veterans Memorial Highway
Metairie, Louisiana 70002
Tel: 504-887-7610
Telex: STERLE LEC MRIE 58-328

MARYLAND
HAMILTON/AVNET ELECTRONICS
(mailing address)
Friendship International Airport
P.O. Box 8647
Baltimore, Maryland 21240

(shipping address)
7255 Standard Drive
Hanover, Maryland 21076
Tel: 301-796-5000 TWX: 710-862-1861
Telex: HAMAVLECA HNVE 87-968

SCHWEBER ELECTRONICS
5640 Fisher Lane
Rockville, Maryland 20852
Tel: 301-881-2970 TWX: 710-828-0536

PIONEER WASHINGTON ELECTRONICS, INC.
9100 Gaither Road
Gaithersburg, Maryland 20760
Tel: 301-948-0710 TWX: 710-828-9784

MASSACHUSETTS
HAMILTON/AVNET ELECTRONICS
185 Cambridge Street
Burlington, Massachusetts 01803
Tel: 617-273-2120 TWX: 710-332-1201

KIERULFF ELECTRONICS
13 Fortune Drive
Billerica, Massachusetts 01865
Tel: 617-667-8331 (Local)
617-935-5134 (from Boston Area)
TWX: 710-390-1449

SCHWEBER ELECTRONICS
213 Third Avenue
Waltham, Massachusetts 02154
Tel: 617-890-8484

FAIRCHILD FRANCHISED DISTRIBUTORS (cont.)

MICHIGAN
HAMILTON/AVNET ELECTRONICS
12870 Farmington Rd.
Livonia, Michigan 48150
Tel: 313-522-4700 TWX: 810-242-8775

PIONEER/DETROIT
13485 Stamford
Livonia, Michigan 48150
Tel: 313-525-1800

SCHWEBER ELECTRONICS
86 Executive Drive
Troy, Michigan 48084
Tel: 313-583-9242

SHERIDAN SALES CO.
24543 Indoplex Drive (P.O. Box 529)
Farmington, Mich. 48024
Tel: 313-477-3800

MINNESOTA
HAMILTON/AVNET ELECTRONICS
7683 Washington Ave. South
Edina, Minnesota 55435
Tel: 612-941-3801
TWX: None — use 910-227-0060
(Regional Hq. in Chicago, Ill.)

SCHWEBER ELECTRONICS
7015 Washington Ave. South
Edina, Minnesota 55435
Tel: 612-941-5280

SEMICONDUCTOR SPECIALISTS, INC.
8030 Cedar Avenue South
Minneapolis, Minnesota 55420
Tel: 612-854-8841 TWX: 910-576-2812

MISSOURI
HAMILTON/AVNET ELECTRONICS
364 Brookes Lane
Hazelwood, Missouri 63042
Tel: 314-731-1144
Telex: HAMAVLECA HAZW 44-2348

SEMICONDUCTOR SPECIALISTS, INC.
3805 N. Oak Trafficway
Kansas City, Mo. 64116
Tel: 816-452-3900 TWX: 910-771-2114

SEMICONDUCTOR SPECIALISTS, INC.
Lakeview Square
1020 Anglum Road
Hazelwood, Missouri 63042
Tel: 314-731-2400 TWX: 910-762-0645

NEW JERSEY
HAMILTON/AVNET ELECTRONICS
113 Gaither Drive
East Gate Industrial Park
Mt. Laurel, N.J. 08057
Tel: 609-234-2133 TWX: 710-897-1405

HAMILTON/AVNET ELECTRONICS
218 Little Falls Road
Cedar Grove, New Jersey 07009
Tel: 201-239-0800 TWX: 710-994-5787

KIERULFF ELECTRONICS
#5 Industrial Drive
Rutherford, New Jersey 07070
Tel: 201-935-2120 TWX: 710-989-0225

STERLING ELECTRONICS
774 Pfeiffer Blvd.
Perth Amboy, N.J. 08861
Tel: 201-442-8000 Telex: 138-679

SCHWEBER ELECTRONICS
43 Belmont Drive
Somerset, N.J. 08873
Tel: 201-469-6008 TWX: 710-480-4733

NEW MEXICO
CENTURY ELECTRONICS
121 Elizabeth, N.E.
Albuquerque, New Mexico 87123
Tel: 505-292-2700 TWX: 910-989-0625

HAMILTON/AVENT ELECTRONICS
2450 Baylor Dr. S.E.
Albuquerque, New Mexico 87119
Tel: 505-765-1500
TWX: None — use 910-379-6486
(Regional Hq. in Mt. View, Ca.)

NEW YORK
HAMILTON/AVNET ELECTRONICS
167 Clay Road
Rochester, New York 14623
Tel: 716-442-7820
TWX: None — use 710-332-1201
(Regional Hq. in Burlington, Mass.)

HAMILTON/AVNET ELECTRONICS
6500 Joy Road
E. Syracuse, New York 13057
Tel: 315-437-2642 TWX: 710-541-0959

HAMILTON/AVNET ELECTRONICS
70 State Street
Westbury, L.I., New York 11590
Tel: 516-333-5800 TWX: 510-222-8237

SCHWEBER ELECTRONICS
Jericho Turnpike
Westbury, L.I., New York 11590
Tel: 516-334-7474 TWX: 510-222-3660

SCHWEBER ELECTRONICS, INC.
2 Town Line Circle
Rochester, New York 14623
Tel: 716-461-4000

SEMICONDUCTOR CONCEPTS
195 Engineers Rd.
Hauppauge, New York 11787
Tel: 516-273-1234 TWX: 510-227-6232

SUMMIT DISTRIBUTORS, INC.
916 Main Street
Buffalo, New York 14202
Tel: 716-884-3450 TWX: 710-522-1692

NORTH CAROLINA
HALLMARK ELECTRONICS
3000 Industrial Drive
Raleigh, North Carolina 27609
Tel: 919-832-4465 TWX: 510-928-1831

PIONEER/CAROLINA ELECTRONICS
2906 Baltic Avenue
Greensboro, North Carolina 27406
Tel: 919-273-4441

OHIO
ARROW ELECTRONICS, INC.
3100 Plainfield Road
Kettering, Ohio 45429
Tel: 513-253-9176 TWX: 810-459-1611

HAMILTON/AVNET ELECTRONICS
761 Beta Drive, Suite "E"
Cleveland, Ohio 44143
Tel: 216-461-1400
TWX: None — use 910-227-0060
(Regional Hq. in Chicago, Ill.)

HAMILTON/AVNET ELECTRONICS
118 Westpark Road
Dayton, Ohio 45459
Tel: 513-433-0610 TWX: 810-450-2531

PIONEER/CLEVELAND
4800 East 131st Street
Cleveland, Ohio 44105
Tel: 216-587-3600

SCHWEBER ELECTRONICS
23880 Commerce Park Road
Beachwood, Ohio 44122
Tel: 216-464-2970 TWX: 810-427-9441

SHERIDAN SALES COMPANY
23224 Commerce Park Road
Beachwood Ohio 44122
Tel: 216-831-0130 TWX: 810-427-2957

SHERIDAN SALES CO.
(mailing address)
P.O. Box 37826
Cincinnati, Ohio 45222
(shipping address)
10 Knollcrest Drive
Reading, Ohio 45237
Tel: 513-761-5432 TWX: 810-461-2670

OKLAHOMA
HALLMARK ELECTRONICS
4846 South 83rd East Avenue
Tulsa, Oklahoma 74145
Tel: 918-835-8458 TWX: 910-845-2290

PENNSYLVANIA
PIONEER/DELWARE VALLEY, INC.
203 Witmer Rd.
Horsham, Pennsylvania 19044
Tel: 215-674-5710 (from Pennsylvania phones)
Tel: 609-541-1120 (from New Jersey phones)

HALLMARK ELECTRONICS, INC.
458 Pike Road
Huntington Valley, Pennsylvania 19006
Tel: 215-355-7300 TWX: 510-667-1727

PIONEER ELECTRONICS, INC.
560 Alpha Drive
Pittsburgh, Pennsylvania 15238
Tel: 412-782-2300 TWX: 710-795-3122

SHERIDAN SALES COMPANY
1717 Penn Ave.
Suite 5009
Pittsburgh, Pennsylvania 15221
Tel: 412-244-1640

TEXAS
HAMILTON/AVNET ELECTRONICS
4445 Sigma Road
Dallas, Texas 75240
Tel: 214-661-8661
Telex: HAMAVLECB DAL 73-0511

HAMILTON/AVNET ELECTRONICS
1216 West Clay
Houston, Texas 77019
Tel: 713-526-4661
Telex: HAMAVLECB HOU 76-2589

NORVELL ELECTRONICS, INC.
10210 Monroe Drive
(P.O. Box 20279)
Dallas, Texas 75220
Tel: 214-350-6771 TWX: 910-861-4512

NORVELL ELECTRONICS, INC.
6440 Hillcroft Avenue
Houston, Texas 77036
Tel: 713-774-2568 TWX: 910-881-2560

SCHWEBER ELECTRONICS, INC.
2628 Longhorn Blvd.
Austin, Texas 78758
Tel: 512-837-2890 TWX: 910-874-1359

SCHWEBER ELECTRONICS, INC.
14177 Proton Road
Dallas, Texas 75240
Tel: 214-661-5010 TWX: 910-860-5493

FAIRCHILD FRANCHISED DISTRIBUTORS (cont.)

SCHWEBER ELECTRONICS, INC.
7420 Harwin Drive
Houston, Texas 77036
Tel: 713-784-3600 TWX: 910-881-1109

STERLING ELECTRONICS
4201 Southwest Freeway
Houston, Texas 77027
Tel: 713-627-9800 TWX: 910-881-5042
Telex: STELECO HOUA 77-5299

UTAH
HAMILTON/AVNET ELECTRONICS
647 W. Billinis Rd.
Salt Lake City, Utah 84119
Tel: 801-262-8451
TWX: None — use 910-379-6486
(Regional Hq. in Mt. View, Ca.)

WASHINGTON
HAMILTON/AVNET ELECTRONICS
13407 Northrup Way
Bellevue, Washington 98005
Tel: 206-746-8750 TWX: 910-443-2449

LIBERTY ELECTRONICS
5305 2nd Ave. South
Seattle, Washington 98108
Tel: 206-763-8200 TWX: 910-444-1379

WISCONSIN
HAMILTON/AVNET ELECTRONICS
6055 N. Santa Monica Blvd.
Whitefish Bay, Wisconsin 53717
Tel: 414-964-3482

MARSH ELECTRONICS, INC.
6047 Beloit Road
Milwaukee, Wisconsin 53219
Tel: 414-545-6500 TWX: 910-262-3321

SEMICONDUCTOR SPECIALISTS, INC.
10855 W. Potter Road
Wauwatosa, Wisconsin 53226
Tel: 414-257-1330 TWX: 910-262-3022

CANADA
CAM GARD SUPPLY LTD.
640 42nd Avenue S.E.
Calgary, Alberta, T2G 1Y6, Canada
Tel: 403-287-0520 Telex: 03-822811

CAM GARD SUPPLY LTD.
10505 111th Street
Edmonton, Alberta, T5H 3E8, Canada
Tel: 403-426-1805 Telex: 03-72960

CAM GARD SUPPLY LTD.
4910 52nd Street
Red Deer, Alberta, T4N 2C8, Canada
Tel: 403-346-2088

CAM GARD SUPPLY LTD.
825 Notre Dame Drive
Kamloops, British Columbia, V2C 5N8, Canada
Tel: 604-372-3338

CAM GARD SUPPLY LTD.
1777 Ellice Avenue
Winnepeg, Manitoba, R3H 0W5, Canada
Tel: 204-786-8401 Telex: 07-57622

CAM GARD SUPPLY LTD.
Rookwood Avenue
Fredericton, New Brunswick, E3B 4Y9, Canada
Tel: 506-455-8891

CAM GARD SUPPLY LTD.
15 Mount Royal Blvd.
Moncton, New Brunswick, E1C 8N6, Canada
Tel: 506-855-2200

CAM GARD SUPPLY LTD.
Courtenay Center
Saint John, New Brunswick, E2L 2X6, Canada
Tel: 506-657-4666 Telex: 01-447489

CAM GARD SUPPLY LTD.
3065 Robie Street
Halifax, Nova Scotia, B3K 4P6, Canada
Tel: 902-454-8581 Telex: 01-921528

CAM GARD SUPPLY LTD.
1303 Scarth Street
Regina, Saskatchewan, S4R 27, Canada
Tel: 306-525-1317 Telex: 07-12667

CAM GARD SUPPLY LTD.
1501 Ontario Avenue
Saskatoon, Saskatchewan, S7K 17, Canada
Tel: 306-652-6424 Telex: 07-42825

ELECTRO SONIC INDUSTRIAL SALES
(TORONTO) LTD.
1100 Gordon Baker Rd.
Willowdale, Ontario, M2H 3B3, Canada
Tel: 416-494-1666
Telex: ESSCO TOR 06-22030

HAMILTON/AVNET INTERNATIONAL
(CANADA) LTD.
6291 Dorman Rd., Unit #16
Mississauga, Ontario, L4V 1H2, Canada
Tel: 416-677-7432 TWX: 610-492-8867

HAMILTON/AVNET INTERNATIONAL
(CANADA) LTD.
1735 Courtwood Crescent
Ottawa, Ontario, K1Z 5L9, Canada
Tel: 613-226-1700

HAMILTON/AVNET INTERNATIONAL
(CANADA) LTD.
2670 Paulus Street
St. Laurent, Quebec, H4S 1G2, Canada
Tel: 514-331-6443 TWX: 610-421-3731

R.A.E. INDUSTRIAL ELECTRONICS, LTD.
1629 Main Street
Vancouver, British Columbia, V6A 2W5, Canada
Tel: 604-687-2621 TWX: 610-929-3065
Telex: RAE-VCR 04-54550

SCHWEBER ELECTRONICS
2724 Rena Road
Mississauga, Ontario, L4T 3J9, Canada
Tel: 416-678-9050

FAIRCHILD SALES REPRESENTATIVES

CALIFORNIA
CELTEC COMPANY
7380 Clairemont Mesa Blvd., Suite 109
San Diego, California 92111
Tel: 714-279-7961 TWX: 910-335-1512

CELTEC COMPANY
2041 Business Center Drive, Suite 211
Irvine, California 92664
Tel: 714-752-6111

COLORADO
SIMPSON ASSOCIATES, INC.
2552 Ridge Road
Littleton, Colorado 80120
Tel: 303-794-8381 TWX: 910-935-0719

CONNECTICUT
LORAC SALES, INC.
2777 Summer Street
Stamford, Connecticut 06905
Tel: 203-348-7701 TWX: 710-474-1763

FLORIDA
WMM ASSOCIATES, INC.
101 Wymore Road, Suite 300
Altamonte Springs, Florida 32701
Tel: 305-862-4700

WMM ASSOCIATES, INC.
1822 Drew Street
Clearwater, Florida 33519
Tel: 813-447-2533 TWX: 810-866-4108

WMM ASSOCIATES, INC.
1628 E. Atlantic Blvd.
Pompano Beach, Florida 33060
Tel: 305-943-3091

GEORGIA
CARTWRIGHT & BEAN, INC.
P.O. Box 52846
90 W. Wieuca Square, Suite 155
Atlanta, Georgia 30342
Tel: 404-255-5262

INDIANA
LESLIE M. DEVOE COMPANY
7172 North Keystone Ave., Suite C
Indianapolis, Indiana 46240
Tel: 317-257-1227 TWX: 810-341-3284

KANSAS
B.C. ELECTRONICS
1015 West Santa Fe
Olathe, Kansas 66061
Tel: 913-782-6696 TWX: 910-749-6414

B.C. ELECTRONICS
1229 South Paige
Wichita, Kansas 67207
Tel: 316-686-3394

MASSACHUSETTS
SPECTRUM ASSOCIATES, INC.
888 Worcester Street
Wellesley, Massachusetts 02181
Tel: 617-237-2796 TWX: 710-348-0424

MICHIGAN
RATHSBURG ASSOCIATES
16621 E. Warren Ave.
Detroit, Michigan 48224
Tel: 313-882-1717 Telex: 23-5229

MISSISSIPPI
CARTWRIGHT & BEAN, INC.
P.O. Box 3730
5250 Galaxy Drive, Suite J
Jackson, Mississippi 39207
Tel: 601-981-1368

MISSOURI
B.C. ELECTRONICS
348 Brookes Drive
Hazelwood, Missouri 63042
Tel: 314-731-1255 TWX: 910-762-0651

NEW JERSEY
LORAC SALES, INC.
580 Valley Road
Wayne, New Jersey 07470
Tel: 201-696-7070 TWX: 710-988-5846

NORTH CAROLINA
CARTWRIGHT & BEAN, INC.
625 Harwyn Drive
Charlotte, North Carolina 28215
Tel: 704-333-6457

CARTWRIGHT & BEAN, INC.
P.O. Box 11209
2415-G Crabtree Blvd.
Raleigh, North Carolina 27604
Tel: 919-832-7128

NEW YORK
LORAC SALES, INC.
275 Broadhollow Road
Melville, New York 11746
Tel: 516-293-2970 TWX: 510-224-6480

OHIO
COMPONENTS, INC.
7461 N. Linden Lane
Cleveland, Ohio
Tel: 216-842-2737

TENNESSEE
CARTWRIGHT & BEAN, INC.
P.O. Box 4760
560 S. Cooper Street
Memphis, Tennessee 38104
Tel: 901-276-4442

CARTWRIGHT & BEAN, INC.
8501 Kingston Pike
Knoxville, Tennessee 37919
Tel: 615-693-7450

TEXAS
TECHNICAL MARKETING
4445 Alpha Road
Dallas, Texas 75240
Tel: 214-387-3601

UTAH
SIMPSON ASSOCIATES, INC.
2480 So. Main Street, Suite 105
Salt Lake City, Utah 84115
Tel: 801-486-3731 TWX: 910-925-5253

WASHINGTON
QUADRA
1621 - 114th Avenue S.E.
Suite 212
Bellevue, Washington 98004
Tel: 206-264-4948 TWX: 910-951-1544

CANADA
AVOTRONICS LIMITED
200 Consumers Road, Suite 200
Willowdale, Ontario, M2J 1P8, Canada
Tel: 416-493-9711

AVOTRONICS LIMITED
6600 Trans Canada Highway, Suite 750
Pointe Claire, Quebec, H9R 4S2, Canada
Tel: 514-697-2135 TWX: 610-422-3908
Telex: 05-821-762

FAIRCHILD SALES OFFICES

***HUNTSVILLE, ALABAMA**
3322 So. Memorial Parkway 35801
Suite 92
Tel: 205-883-7020 TWX: 810-726-2214

PHOENIX, ARIZONA
4414 N. 19th Avenue 85015
Suite G
Tel: 602-264-4948 TWX: 910-951-1544

***LOS ANGELES, CALIFORNIA**
6922 Hollywood Blvd. 90028
Suite 818
Tel: 213-466-8393 TWX: 910-321-3009

SAN DIEGO, CALIFORNIA
8333 Clairemont Mesa Blvd. 92111
Suite 109
Tel: 714-279-6021

***SANTA ANA, CALIFORNIA**
2101 East Fourth St. 92705
Bldg. B, Suite 185
Tel: 714-558-1881 TWX: 910-595-1109

***SANTA CLARA, CALIFORNIA**
3080 Olcott Street 95050
Suite 210A
Tel: 408-244-1400 TWX: 910-338-0241

***DENVER, COLORADO**
7475 W. 5th Ave., Suite 100
Lakewood, Colo. 80226
Tel: 303-234-9292

***STAMFORD, CONNECTICUT**
2nd Floor
2777 Summers Street 06905
Tel: 203-348-7701 TWX: 710-474-1763

ORLANDO, FLORIDA
Crane's Roost Office Park
303 Whooping Loop
Altamonte Springs, Fla. 32701
Tel: 305-834-7000 TWX: 810-850-0152

TAMPA, FLORIDA
12945 Seminole Blvd.
Florida Twin Towers Bldg. 2, Room 6
Largo, Fla. 33540
Tel: 813-585-3892

***CHICAGO, ILLINOIS**
9950 W. Lawrence Avenue
Room 311
Schiller Park, Ill. 60176
Tel: 312-671-4660 TWX: 910-227-0051

FORT WAYNE, INDIANA
2118 Inwood Drive 46805
Suite 111
Tel: 219-483-6453 TWX: 810-332-1507

***INDIANAPOLIS, INDIANA**
7202 N. Shadeland 46250
Tel 317-849-5412 TWX: 810-260-1793

BLADENSBURG, MARYLAND
5801 Annapolis Road 20710
Suite 500
Tel: 301-779-0954 TWX: 710-826-9654

***BOSTON, MASSACHUSETTS**
888 Worcester Street
Wellesley Hills, Mass. 02181
Tel: 617-237-3400 TWX: 710-348-0424

DETROIT, MICHIGAN
Westland Office Plaza
33300 Warren Avenue Suite 101
Westland, Mich. 48185
Tel: 313-425-3250 TWX: 810-242-2973

MINNEAPOLIS, MINNESOTA
7600 Parklawn Avenue
Room 251
Edina, Minn. 55435
Tel: 612-835-3322 TWX:910-576-2944

WAYNE, NEW JERSEY
580 Valley Road 07490
Suite 1
Tel: 201-696-7070

ALBUQUERQUE, NEW MEXICO
2403 San Mateo N.E. 87110
Plaza #2
Tel: 505-265-5601 TWX: 910-989-1186

BINGHAMTON, NEW YORK
3215 E. Main St. Suite 7
Endwell, NY 13760
Tel: 607-754-1094

***MELVILLE, NEW YORK**
275 Broadhollow Road 11746
Tel: 516-293-2900 TWX: 510-224-6480

POUGHKEEPSIE, NEW YORK
15 College View Ave. 12603
Tel: 914-452-4200 TWX: 510-248-0030

***ROCHESTER, NEW YORK**
600 Kreag Rd.
Pittsford, NY 14534
Tel: 716-385-1130

SYRACUSE, NEW YORK
333 E. Onondaga Street 13202
Tel: 315-471-3391 TWX: 710-541-0499

CLEVELAND, OHIO
6151 Wilson Mills Rd.
Suite 101
Highland Heights, Ohio 44143
Tel: 216-461-8288 TWX: 810-427-9271

DAYTON, OHIO
4812 Frederick Road 45414
Suite 101
Tel: 513-278-8278 TWX: 810-459-1803

TULSA, OKLAHOMA
5321 S. Sheridan Road 74145
Suite 15
Tel: 918-663-7131

***PHILADEPHIA, PENNSYLVANIA**
Fort Washington Industrial Park
500 Office Center
Fort Washington, Pa. 19034
Tel: 215-886-6623 TWX: 510-665-1654

***DALLAS, TEXAS**
13771 N. Central Expressway 75231
Suite 809
Tel: 214-234-3391 TWX: 910-867-4757

***HOUSTON, TEXAS**
6430 Hillcroft 77036
Suite 102
Tel: 713-771-3547 TWX: 910-881-6278

MILWAUKEE, WISCONSIN
4642 76th Street
Suite 101
Greenfield, Wisconsin 53220
Tel: 414-282-5260

*Field Applications Engineer available.

*Field Applications Engineer available.

INTERNATIONAL FIELD SALES OFFICES

AUSTRALIA
Fairchild Australia Pty. Ltd.
420 Mount Dandenong Road
Croydon, Victoria, 3136
Australia
Tel: 723-4131 TWX: 30846

AUSTRIA
Fairchild Electronics
Schwedenplatz 2
1010 Vienna
Tel: 0043 222635821
Telex: 0047 75096

BRAZIL
Fairchild Electronica Ltd.
Caixa Postal 30407
Rua de Consola Cao, 3542
Sao Paulo, S.P. Brazil
Tel: 81-6168 Telex: 021-261
Cable: FAIRLEC

CANADA
Toronto Regional Office
FSC
1590 Matheson Blvd. Unit 26
Mississauga, Ontario L4W 1J1, Canada
Tel: 416-625-7070 TWX: 610-492-4311

Fairchild Semiconductor
1385 Mazurette Suite 3
Montreal, Quebec, H4N 1G8, Canada
Tel: 514-382-2552 TWX: 610-421-3178

FRANCE
Fairchild Semiconducteurs, S.A.
121 Avenue d'Italien
750310, Paris, France
Tel: 00331 5805566
Telex: 0042 20614

GERMANY
Fairchild Halbleiter GmbH
European Headquarters
6202 Wiesbaden-Biebrich
Postfach 4559
Hagenauer Strasse 38
Tel: 06121 2051 Telex: 841-4186588

Fairchild Halbleiter GmbH
8 Munchen 80
Truderinger Str. 13
Tel: 089 4701091-3 Telex: 05 24831

Fairchild Halbleiter GmbH
8500 Nurnberg
Waldluststr. 1
Tel: 0911 407005 Telex: 06-23665

Fairchild Halbleiter GmbH
725 Leonberg-Eltingen
Poststr. 37
Tel: 07152-41026 Telex: 07-22644

HONG KONG
Fairchild Semiconductor (HK) Ltd.
135 Hoi Bun Road
Kwun Tong
Kowloon, Hong Kong
Tel: K-890271 Telex: HKG-531

ITALY
Fairchild Semiconduttori, S.p.A.
Viale Cortina d'Ampezzo, 152
00135 Rome, Italy
Tel: 00396 3274006

Fairchild Semiconduttori S.p.A.
Via Rosselini, 12
20124 Milano, Italy
Tel: 00392 6887451-5

JAPAN
TDK-Fairchild
Sanyo Kokusaku Pulp Bldg. 2nd Fl.
7-8 Shibuya 1-Chome
Shibuya-ku
Tokyo 150, Japan
Tel: 03-400-8351 Telex: 2424173

MEXICO
Fairchild Mexicana S.A.
Blvd. Adolfo Lopez Mateos No. 163
Mexico 19, D.F.
Tel: 905-563-5411 Telex: 017-71-038

SCOTLAND
Fairchild Semiconductor Ltd.
Shiel House
Craigshill
Livingston
West Lothian, Scotland
Tel: 00445 8932891
Telex: 0051 72629

SWEDEN
Fairchild Semiconductor AB
Svartensgatan 6,
S-11620 Stockholm
Tel: 00468-449255 Telex: 0054-17759

TAIWAN
Fairchild Semiconductor (Taiwan) Ltd.
Hsietsu Building, Room 502
47 Chung Shan North Road
Sec. 3, Taipei, Taiwan
Tel: 573205 thru 573207

THE NETHERLANDS
Fairchild Semiconductor
Paradijslaan 39
Eindhoven, Holland
Tel: 003140-446909 Telex: 0044-51024

UNITED KINGDOM
Fairchild Semiconductor Ltd.
Kingmaker House
Station Road
New Barnet/Hertfordshire
Tel: 00441 4407311 Telex: 0051 262835

FAIRCHILD
SEMICONDUCTOR

Printed in U.S.A./2006-12-0008-114/50M