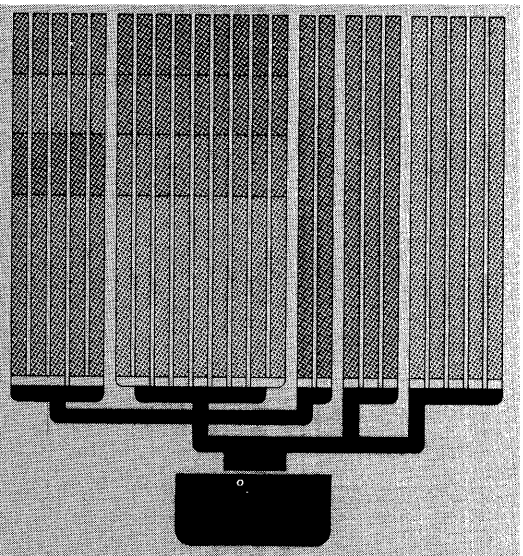


SSI
9000, 9H(54/74H), 9L, 9N(54/74) and 9S(54/74S) Series Data Sheets

This section comprises data sheets on the five basic Fairchild TTL/SSI series.

9000
9H00/54H, 74H00
9L00
9N00/54, 7400
9S00/54S, 74S00

Devices are presented in alpha-numerical sequence, with the exception of the 9000. elements. All 9000 series functions are grouped together at the beginning of this section.

TTL/SSI INTRODUCTION

INTRODUCTION – The Fairchild TTL/SSI line offers the designer a broad selection of gates and flip-flops for use with Fairchild MSI, Interface and Memory products in implementing TTL system designs. These TTL/SSI functions are available for use in military and industrial temperature range applications. These products are available in the popular Dual In-Line package as well as flat packages. All Fairchild TTL products are logic and supply voltage compatible so that circuit families may be mixed within a system for optimum speed, power and economy.

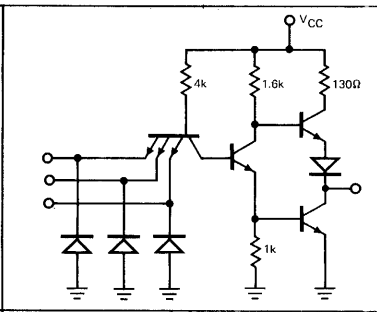
9N/54, 74 SERIES TTL/SSI

FEATURES

- 10 ns Typical Gate Delay
- 10 mW Typical Gate Power Dissipation
- Input Clamp Diodes Minimize Termination Effects
- Military and Industrial Temperature Range
- Available in DIP and Flat Packages

DESCRIPTION

The 9N/54, 74 Series is a broad family of SSI devices which are pin and function identical with the popular 7400 series. These gates and binaries are available in industrial and military temperature ranges in both DIP and Flat packages. The line included NAND gates, NOR gates, Exclusive-OR gates, AND gates, open collector gates as well as single and dual flip-flops.



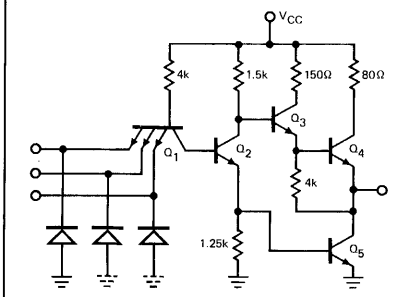
9000 SERIES TTL/SSI

FEATURES

- 8 ns Typical Gate Delay
- 10 mW Typical Gate Power Dissipation
- Input Clamp Diodes Reduce Termination Effects
- Darlington Output Stage Increases Circuit Speed
- Military and Industrial Temperature Range
- Available in DIP and Flat Packages

DESCRIPTION

The 9000 Series of gates and flip-flops offers a family of high speed functions with speed and power specifications in between the 9N/54, 74 Series and the 9H/54H, 74H Series. The Darlington output stage provides faster switching times and increased capacitive drive capability over the 9N/54, 74 Series.



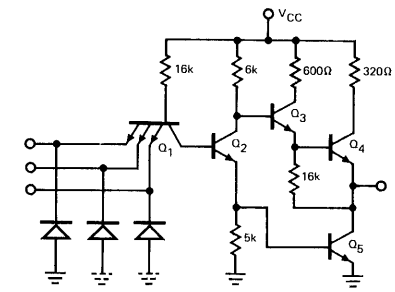
9L SERIES LPTTL/SSI

FEATURES

- 20 ns Typical Gate Delay
- 2 mW Typical Gate Power Dissipation
- Input Clamp Diodes Minimize Termination Effects
- Darlington Output Stage Increases Circuit Speed
- Military and Industrial Temperature Range
- Available in DIP and Flat Packages

DESCRIPTION

The 9L Series of low power TTL gates and flip-flops offers a speed/power trade-off well suited to both industrial and military applications. The power is one fourth that of a standard TTL gate and typical system speeds of up to 10 MHz are possible. The 9L Series TTL/SSI functions are used with the 93L low power TTL/MSI devices to implement low power, moderate speed systems.



9H/54H, 74H SERIES HSTTL/SSI

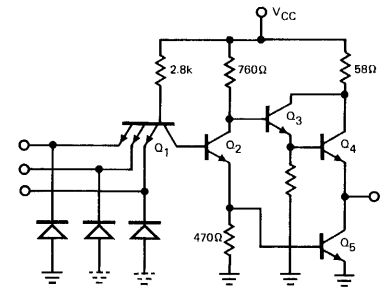
FEATURES

- 6 ns Typical Gate Delay
- 22 mW Typical Gate Power Dissipation
- Input Clamp Diodes to Minimize Termination Effects
- Darlington Output State to Increase Circuit Speed
- Military and Industrial Temperature Range
- Available in DIP and Flat Packages
- 11 Functions Available

DESCRIPTION

The 9H/54H, 74H Series is a line of high speed gates and flip-flops which are pin and function identical with the popular 74H00 Series.

These devices are used with the 9300 and 93H Series of TTL/MSI devices to substantially reduce critical path delay times and enhance overall system speeds.



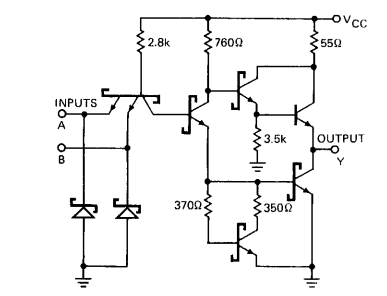
9S/54S, 74S SERIES TTL/SSI

FEATURES

- 3 ns Typical Gate Delay
- 125 MHz Typical Input Clock Frequency for J-K Flip-Flops
- 22 mW Gate Power Dissipation
- Input Clamp Diodes to Minimize Termination Effects
- Low Output Impedance to Drive High Capacitive Loads

DESCRIPTION

The 9S00 Series is a line of super high speed devices featuring Schottky-barrier diode clamping on all normally saturated devices. The result is an overall improvement in propagation delays and greatly reduced sensitivity of delay times to temperature variation. These gate and flip-flop functions can be used with Fairchild's 93S00 Series of MSI Schottky-clamped logic elements to achieve the highest possible system speeds and still maintain typical 1.0 V noise immunity.



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	0.5 V to +V_{CC}
Output Current (dc) (Output LOW)	
9N/54,74 and 9L Series	+30 mA
9000, 9H and 9S Series	+50 mA
See Detail Data Sheets for Buffer Drive Capability.	

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

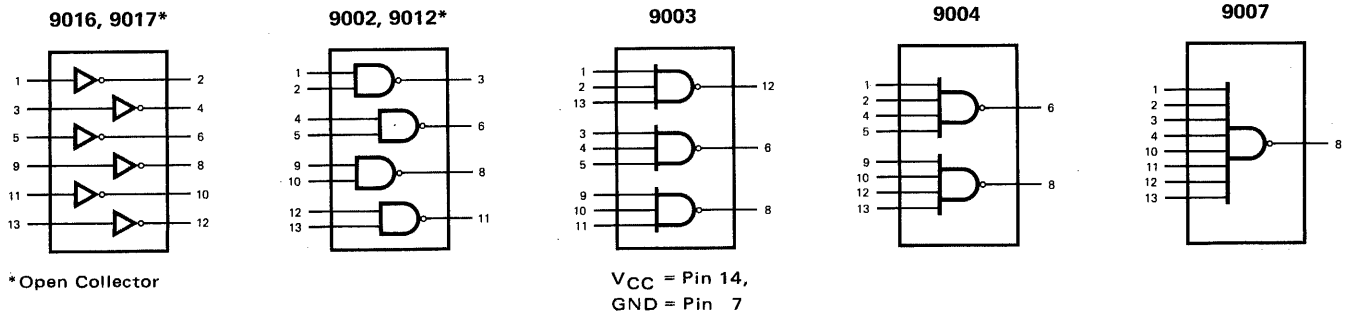
INPUT AND OUTPUT LOAD FACTORS FOR THE 9000 SERIES GATES & FLIP-FLOPS

The test conditions and resulting limits for the input and output levels of the 9000 Series gates and flip-flops differs from the other 9N, 9H, 9L, and 9S series of devices. These 9000 Series levels and conditions are equivalent to the other families for all practical purposes. For instance, an input HIGH level current guaranteed to be 60 μA when measured at 4.5 V, will be less than 40 μA for most operating conditions. Therefore, the load factors for the 9000 Series has been normalized to simplify system design considerations.

NAND GATES – 9002, 9003, 9004, 9007 AND 9012*
HEX INVERTER – 9016 AND 9017*

The 9002, 9003, 9004, 9007 and 9012 are active LOW level output AND gates commonly known as NAND gates. The 9016 and 9017 are hex inverters with input and output characteristics identical to NAND gate. The variety of gate combinations provides the system designer the utmost in logic flexibility and reduces package count.

LOGIC SYMBOL AND PIN CONFIGURATIONS



*Open Collector

V_{CC} = Pin 14,
GND = Pin 7

Fig. 1

BASIC GATE CIRCUIT

Nominal Resistor Values

$R_1 = R_5 = 4.0\ k\Omega$
$R_2 = 1.5\ k\Omega$
$R_3 = 150\ \Omega$
$R_4 = 80\ \Omega$
$R_6 = 1.25\ k\Omega$

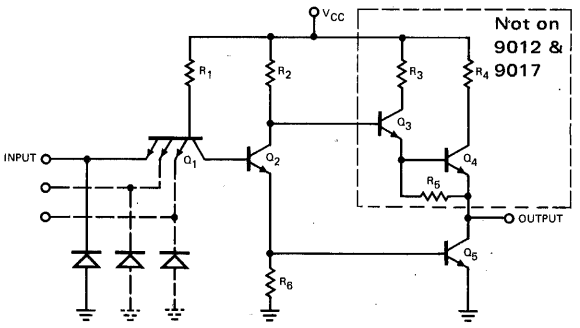


Fig. 2

LOADING FACTORS

PIN NAMES	LOADING
All Inputs	1 U.L.
All Outputs	10 U.L.*

(1 U.L. = 40 μA HIGH/1.6 mA LOW)

*The 9012 & 9017 need external resistors to provide HIGH level drive.

Fig. 3

ELECTRICAL CHARACTERISTICS 9002XC, 9003XC, 9004XC, 9007XC, 9012XC, 9016XC AND 9017XC ($T_A = 0°C$ to $75°C$, $V_{CC} = 5.0\ V \pm 5\%$)

SYMBOL	PARAMETER		LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS 25°C MIN.	LIMITS 25°C TYP.	LIMITS 25°C MAX.	LIMITS 75°C MIN.	LIMITS 75°C MAX.	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage		1.9		1.8			1.6		Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs	
V_{IL}	Input LOW Voltage			0.85			0.85		0.85	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs	
V_{OH}	Output HIGH Voltage (except 9012, 9017)		2.4		2.4	2.9		2.4		Volts	$V_{CC} = 4.75\ V$, $I_{OH} = -1.2\ mA$, Inputs at V_{IL}	
V_{OL}	Output LOW Voltage			0.45		0.21	0.45		0.45	Volts	$V_{CC} = 5.25\ V$, $I_{OL} = 16.0\ mA$, $V_{IN} = 5.25\ V$	
											$V_{CC} = 4.75\ V$, $I_{OL} = 14.1\ mA$, Inputs at V_{IH}	
I_{IH}	Input HIGH Current					10	60		60	μA	$V_{CC} = 5.25\ V$, $V_{IN} = 4.5\ V$ GND on Other Inputs	
I_{IL}	Input LOW Current			−1.6		−1.0	−1.6		−1.6	mA	$V_{CC} = 5.25\ V$	$V_{IN} = 0.45\ V$
				−1.41		−0.91	−1.41		−1.41		$V_{CC} = 4.75\ V$	5.25 V on Other Inputs
I_{CEX}	Output Reverse Current 9012, 9017 only					2.0	250		250	μA	$V_{CC} = 4.75\ V$, $V_{IN} = V_{IL}$, $V_{OUT} = 5.5\ V$	
I_{CC}	V_{CC} Current, Gate On (each gate)			6.1		3.6	6.1		6.1	mA	Inputs HIGH	$V_{CC} = 5.0\ V$
	V_{CC} Current, Gate Off (each gate)			1.7		1.07	1.7		1.7		Inputs at GND	
t_{PLH}	Turn OFF Delay Input to Output					3.0	13			ns		$V_{CC} = 5.0\ V$, $C_L = 15\ pF$ See Fig. 12
		9012, 9017 only				3.0	45				$R_L = 4.0\ k\Omega$	
t_{PHL}	Turn ON Delay Input to Output					3.0	15			ns		
		9012, 9017 only				3.0	15				$R_L = 400\ \Omega$	

ELECTRICAL CHARACTERISTICS 9002XM, 9003XM, 9004XM, 9007XM, 9012XM, 9016XM, AND 9017XM ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$)

SYMBOL	PARAMETER		LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS 25°C MIN.	LIMITS 25°C TYP.	LIMITS 25°C MAX.	LIMITS 125°C MIN.	LIMITS 125°C MAX.	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage		2.0		1.7			1.4		Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs	
V_{IL}	Input LOW Voltage			0.8			0.9		0.8	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs	
V_{OH}	Output HIGH Voltage (except 9012, 9017)		2.4		2.4	2.7		2.4		Volts	$V_{CC} = 4.5\ V$, $I_{OH} = -1.32\ mA$, Inputs at V_{IL}	
V_{OL}	Output LOW Voltage			0.4		0.21	0.4		0.4	Volts	$V_{CC} = 5.5\ V$, $I_{OL} = 17.6\ mA$, $V_{IN} = 5.5\ V$	
											$V_{CC} = 4.5\ V$, $I_{OL} = 13.6\ mA$, Inputs at V_{IH}	
I_{IH}	Input HIGH Current					10	60		60	μA	$V_{CC} = 5.5\ V$, $V_{IN} = 4.5\ V$ GND on Other Inputs	
I_{IL}	Input LOW Current			−1.6		−1.1	−1.6		−1.6	mA	$V_{CC} = 5.5\ V$	$V_{IN} = 0.4\ V$
				−1.24		−0.87	−1.24		−1.24		$V_{CC} = 4.5\ V$	5.5 V on Other Inputs
I_{CEX}	Output Reverse Current 9012, 9017 only					2.0	250		250	μA	$V_{CC} = 4.5\ V$, $V_{IN} = V_{IL}$, $V_{OUT} = 5.5\ V$	
I_{CC}	V_{CC} Current, Gate On (each gate)			5.5		3.5	5.5		5.5	mA	Inputs HIGH	$V_{CC} = 5.0\ V$
	V_{CC} Current, Gate Off (each gate)			1.6		1.07	1.6		1.6		Inputs at GND	
t_{PLH}	Turn OFF Delay Input to Output					3.0	10			ns		$V_{CC} = 5.0\ V$, $C_L = 15\ pF$ See Fig. 12
		9012, 9017 only				3.0	45				$R_L = 4.0\ k\Omega$	
t_{PHL}	Turn ON Delay Input to Output					3.0	12			ns		
		9012, 9017 only				3.0	15				$R_L = 400\ \Omega$	

9002, 9003, 9004, 9007, 9012, 9016 AND 9017
TYPICAL INPUT AND OUTPUT CHARACTERISTICS

OUTPUT VOLTAGE VERSUS INPUT VOLTAGE

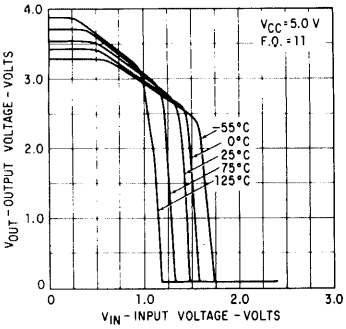


Fig. 4

INPUT CURRENT VERSUS INPUT VOLTAGE

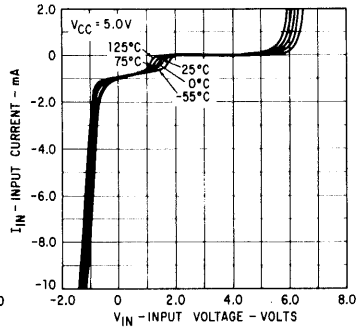


Fig. 5

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)

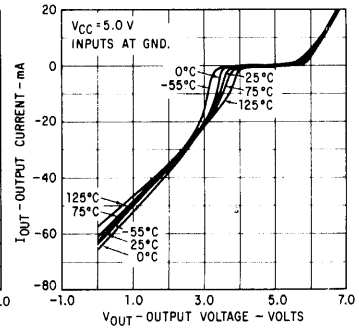


Fig. 6

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)

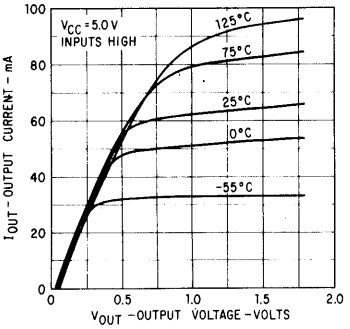


Fig. 7

POWER DISSIPATION, LOGIC LEVELS AND NOISE IMMUNITY

POWER DISSIPATION VERSUS SUPPLY VOLTAGE

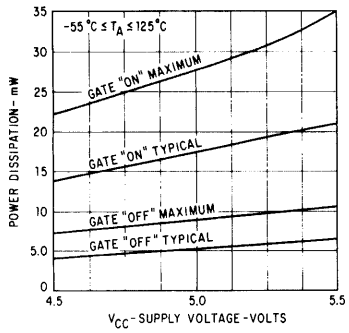


Fig. 8

WORST CASE LOGIC LEVELS VERSUS AMBIENT TEMPERATURE

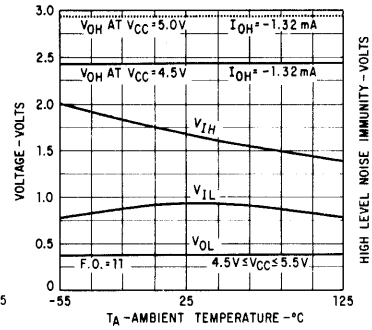


Fig. 9

WORST CASE HIGH LEVEL NOISE IMMUNITY VERSUS AMBIENT TEMPERATURE

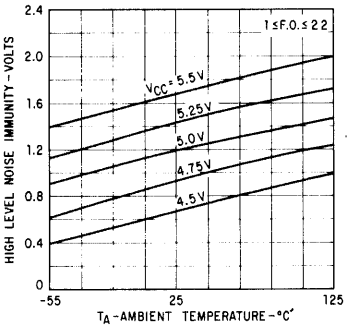


Fig. 10

WORST CASE LOW LEVEL NOISE IMMUNITY VERSUS AMBIENT TEMPERATURE

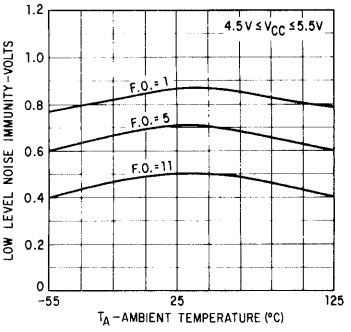
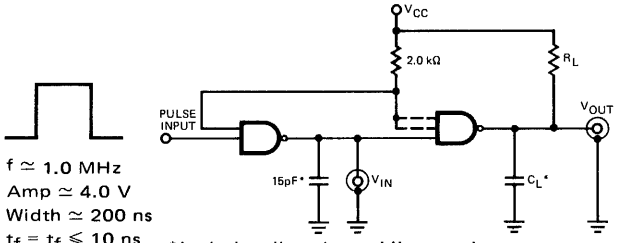


Fig. 11

SWITCHING CHARACTERISTICS

TEST CIRCUIT



WAVEFORM

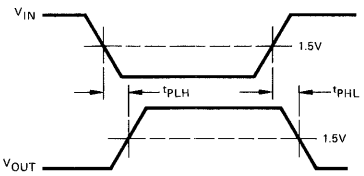


Fig. 12

WORST CASE TURN OFF DELAY VERSUS AMBIENT TEMPERATURE

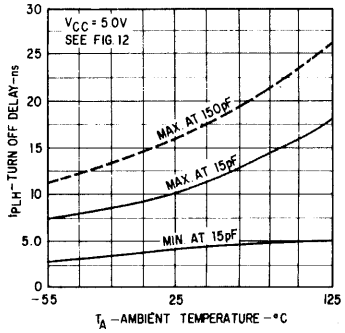


Fig. 13

WORST CASE TURN ON DELAY VERSUS AMBIENT TEMPERATURE

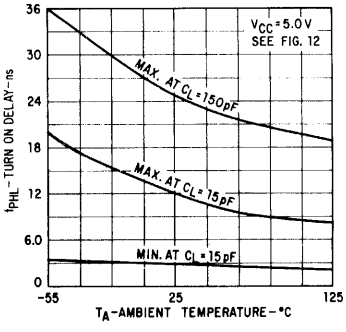


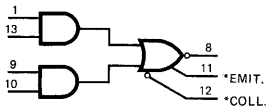
Fig. 14

EXTENDABLE AND-OR-INVERT GATES – 9005, 9008
EXTENDER – 9006

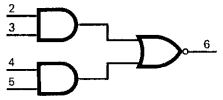
The TTL 9005 and 9008 are AND-OR-INVERT gates which may be OR extended with the use of the 9006. For noise immunity and operating level curves, refer to the gate section.

LOGIC DIAGRAMS

9005
EXTENDABLE GATE

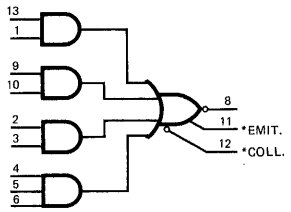


NON-EXTENDABLE GATE



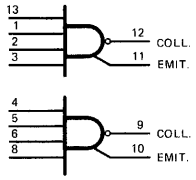
V_{CC} = Pin 14
GND = Pin 7
*Four Extenders (9006) may be tied to these terminals

9008



V_{CC} = Pin 14
GND = Pin 7
*Four Extenders (9006) may be tied to these terminals

9006

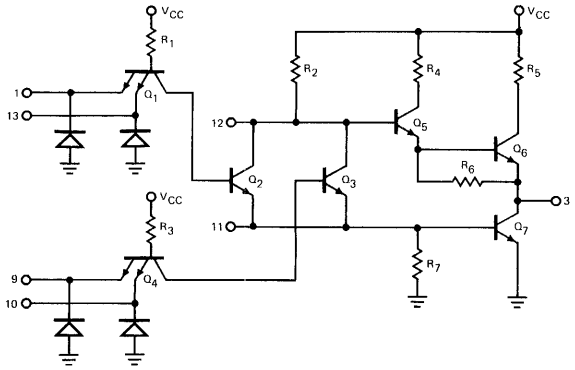


V_{CC} = Pin 14
GND = Pin 7

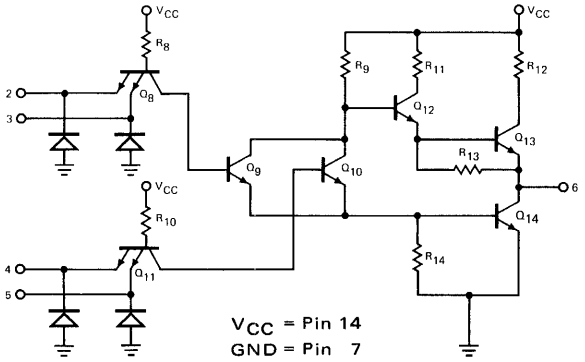
Fig. 1

CIRCUIT DIAGRAMS

9005
EXTENDABLE GATE



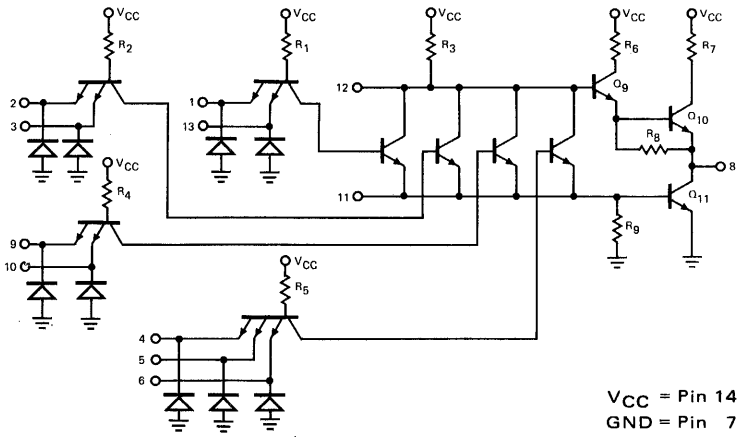
NON-EXTENDABLE GATE



V_{CC} = Pin 14
GND = Pin 7

Typical Resistor Values
$R_1 = R_3 = 2.6\ k\Omega$
$R_2 = 800\ \Omega$
$R_4 = R_{11} = 150\ \Omega$
$R_5 = R_{12} = 80\ \Omega$
$R_6 = R_8 = R_{10} = R_{13} = 4.0\ k\Omega$
$R_7 = 665\ \Omega$
$R_9 = 1.5\ k\Omega$
$R_{14} = 1.25\ k\Omega$

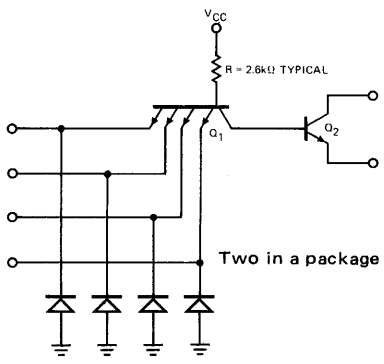
9008



V_{CC} = Pin 14
GND = Pin 7

Typical Resistor Values
$R_1 = R_2 = R_4 = R_5 = 2.6\ k\Omega$
$R_3 = 800\ \Omega$
$R_6 = 150\ \Omega$
$R_7 = 80\ \Omega$
$R_8 = 4.0\ k\Omega$
$R_9 = 665\ \Omega$

9006



V_{CC} = Pin 14
GND = Pin 7

Fig. 2

LOADING FACTORS

9005		9008		9006	
PIN NAMES	**LOADING**	**PIN NAMES**	**LOADING**	**PIN NAMES**	**LOADING**
Non-extendable Gate Inputs	1.0 U.L.	All Inputs	1.5 U.L.	All Inputs	1.5 U.L.
Extendable Gate Inputs	1.5 U.L.	Outputs	10 U.L.	Outputs	*
All Outputs	10 U.L.				

*Outputs on 9006 have open emitter and collector.

(1 U.L. = 40 μA HIGH/1.6 mA LOW)

Fig. 3

ELECTRICAL CHARACTERISTICS 9005XC, 9006XC AND 9008XC (T_A = 0°C to 75°C, V_{CC} = 5.0 V ±5%)

SYMBOL	PARAMETER	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS 25°C MIN.	LIMITS 25°C TYP.	LIMITS 25°C MAX.	LIMITS 75°C MIN.	LIMITS 75°C MAX.	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage	1.9		1.8			1.6		Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage		0.85			0.85		0.85	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs
V_{OH}	Output HIGH Voltage	2.4		2.4	2.9		2.4		Volts	V_{CC} = 4.75 V, I_{OH} = −1.2 mA V_{IL} = Value indicated on This Table
V_{OL}	Output LOW Voltage		0.45		0.2	0.45		0.45	Volts	V_{CC} = 5.25 V, I_{OL} = 16.0 mA, V_{IN} = 5.25 V V_{CC} = 4.75 V, I_{OL} = 14.1 mA, Inputs at V_{IL}
I_{IH}	Input HIGH Current 9005 Non-Extendable Gate				5.0	60		60	μA	V_{IN} = 4.5 V V_{CC} = 4.75 V GND on All Other Inputs
	Input HIGH Current Extendable Gates and Extender				7.5	90		90		
I_{IL}	Input LOW Current 9005 Non-Extendable Gate		−1.6		−1.04	−1.6		−1.6	mA	V_{CC} = 5.25 V; V_{IN} = 0.45 V, 5.25 V on Other Inputs
			−1.41		−0.79	−1.41		−1.41		V_{CC} = 4.75 V
	Input LOW Current Extendable Gates and Extender		−2.4		−1.56	−2.4		−2.4	mA	V_{CC} = 5.25 V
			−2.12		−1.19	−2.12		−2.12		V_{CC} = 4.75 V
I_{CC}	V_{CC} Current, Gate "ON" 9005 Non-Extendable Gate		7.7		4.5	7.7		7.7	mA	V_{CC} = 5.0 V All Inputs Open
	9005 Extendable Gate		13.6		7.6	13.6		13.6		
	9008		17.7		9.3	17.7		17.7		
	V_{CC} Current, Gate "OFF" 9005 Non-Extendable Gate		3.4		2.2	3.4		3.4	mA	V_{CC} = 5.0 V All Inputs Except Extender Inputs GND
	9005 Extendable Gate		5.1		3.3	5.1		5.1		
	9008		10.2		6.6	10.2		10.2		
ΔI_{CC}	Extra Current Drain when one 9006 Extender is attached to a 9005 Gate "ON"		2.05		1.08	2.05		2.05	mA	V_{CC} = 5.0 V All Inputs HIGH
	Extra Current Drain when one 9006 Extender is attached to a 9005 Gate 'OFF"		2.54		1.65	2.54		2.54	mA	V_{CC} = 5.0 V All Inputs GND

NOTE:
Output characteristics above apply to a 9005 (both gates) or a 9008.
Input characteristics above apply to a 9005 (both gates) or a 9008 using either the internal gates or an external 9006 extender.

ELECTRICAL CHARACTERISTICS 9005XM, 9006XM AND 9008XM (T_A = −55°C to 125°C, V_{CC} = 5.0 V ±10%)

SYMBOL	PARAMETER	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS 25°C MIN.	LIMITS 25°C TYP.	LIMITS 25°C MAX.	LIMITS 125°C MIN.	LIMITS 125°C MAX.	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage	2.0		1.7			1.4		Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs	
V_{IL}	Input LOW Voltage		0.8			0.9		0.8	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs	
V_{OH}	Output HIGH Voltage	2.4		2.4	2.7		2.4		Volts	V_{CC} = 4.5 V, I_{OH} = −1.32 mA V_{IL} = Value Indicated on This Table	
V_{OL}	Output LOW Voltage		0.4		0.2	0.4		0.4	Volts	V_{CC} = 5.5 V, I_{OL} = 17.6 mA, V_{IN} = 5.5 V	
										V_{CC} = 4.5 V, I_{OL} = 13.6 mA, Inputs at V_{IH}	
I_{IH}	Input HIGH Current 9005 Non-extendable Gate				5.0	60		60	μA	V_{CC} = 5.5 V V_{IN} = 4.5 V	GND on All Other Inputs
	Input HIGH Current Extendable Gate and Extender				7.5	90		90			
I_{IL}	Input LOW Current 9005 Non-extendable Gate		−1.6		−1.1	−1.6		−1.6	mA	V_{CC} = 5.5 V	V_{IN} = 0.4 V, 5.5 V on Other Inputs
			−1.24		−0.87	−1.24		−1.24		V_{CC} = 4.5 V	
	Input LOW Current Extendable Gate and Extender		−2.4		−1.5	−2.4		−2.4	mA	V_{CC} = 5.5 V	
			−1.86		−1.31	−1.86		−1.86		V_{CC} = 4.5 V	
I_{CC}	V_{CC} Current, Gate "ON" 9005 Non-extendable Gate		6.5		4.5	6.5		6.5	mA	V_{CC} = 5.0 V	All Inputs Open
	9005 Extendable Gate		11.3		7.6	11.3		11.3			
	9008		12.5		9.3	12.5		12.5			
	V_{CC} Current, Gate "OFF" 9005 Non-extendable Gate		3.1		2.1	3.1		3.1	mA	V_{CC} = 5.0 V	All Inputs Except Extender Inputs GND
	9005 Extendable Gate		4.7		3.3	4.7		4.7			
	9008		9.4		6.6	9.4		9.4			
ΔI_{CC}	Extra Current Drain from one 9006 Extender Gate "ON"		1.61		1.08	1.61		1.61	mA	V_{CC} = 5.0 V, All Inputs HIGH 9006 Attached to a 9005	
	Extra Current Drain from one 9006 Extender Gate 'OFF"		2.35		1.65	2.35		2.35	mA	V_{CC} = 5.0 V, All Inputs GND 9006 Attached to a 9005	

NOTE:
Output characteristics apply to a 9005 (both gates) or a 9008.
Input characteristics apply to a 9005 (both gates) or a 9008 using either the internal gates or an external 9006 extender.

9005, 9006, 9008
TYPICAL INPUT-OUTPUT CHARACTERISTICS
(EXTENDABLE GATES)

OUTPUT VOLTAGE VERSUS INPUT VOLTAGE

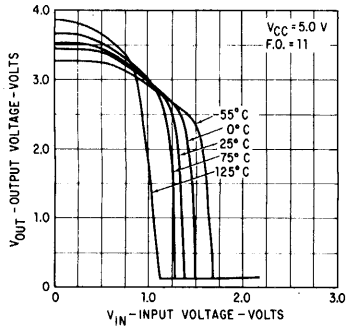


Fig. 4

INPUT CURRENT VERSUS INPUT VOLTAGE

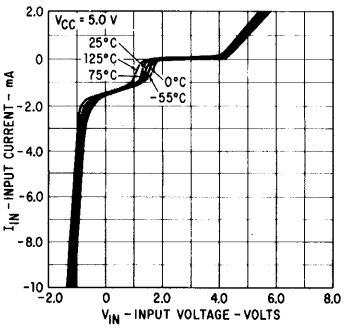


Fig. 5

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)

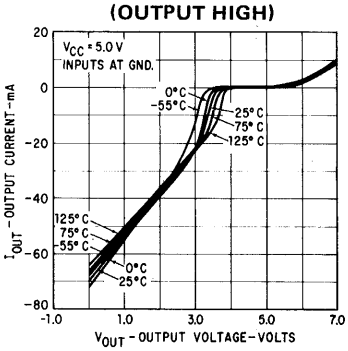


Fig. 6

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)

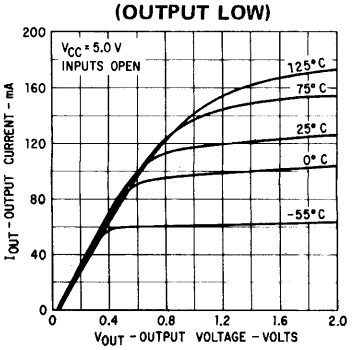


Fig. 7

SWITCHING CHARACTERISTICS

TEST CIRCUITS

9005 NON-EXTENDABLE GATE

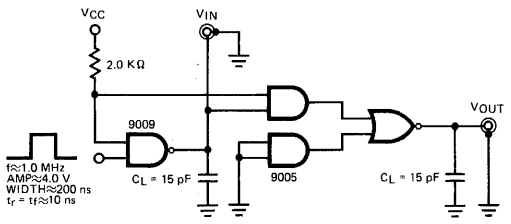
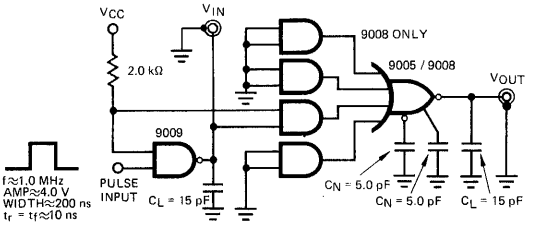


Fig. 8

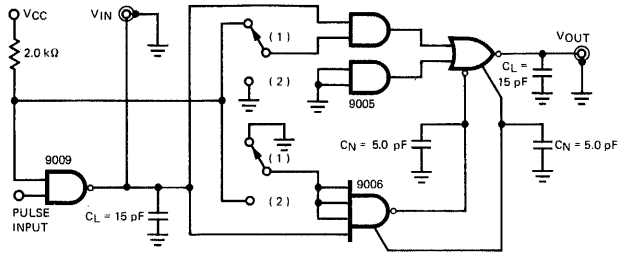
9005 OR 9008 EXTENDABLE GATE



Note: Capacitance includes probe and jig capacitance

Fig. 9

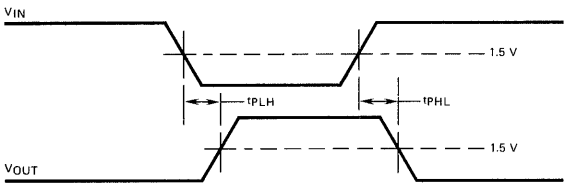
9006 EXTENDER



Note: Capacitance includes probe and jig capacitance

Fig. 10

SWITCHING WAVEFORM



NOTES:
With switch in position (1) measure delay of 9005. With switch in position (2) measure delay (9005) + Δdelay (9006). Capacitances include probe and jig capacitances.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	LIMITS MIN.	LIMITS MAX.	UNITS	TEST CONDITIONS
t_{PLH}	3.0	12	ns	V_{CC} = 5.0 V, C_L = 15 pF
t_{PHL}	3.0	14		9005 Non-extendable Gate Only, See Figure 8
t_{PLH}	3.0	15	ns	V_{CC} = 5.0 V, C_L = 15 pF, C_N = 5.0 pF
t_{PHL}	3.0	12		9005 Extendable Gate and 9008, See Figure 9
Δt_{PLH}	−2.0	4.0	ns	9006 Only
Δt_{PHL}	−2.0	4.0		The 9006 is tested by measuring its propagation time through the 9005. The delay readings shall not exceed the 9005 readings by the specified amount. See Figure 10.

Symbols are defined in the test circuit.

WORST CASE TURN OFF DELAY OF EXTENDABLE GATE VERSUS AMBIENT TEMPERATURE

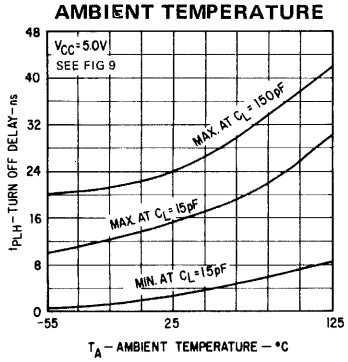


Fig. 11

WORST CASE TURN ON DELAY OF EXTENDABLE GATE VERSUS AMBIENT TEMPERATURE

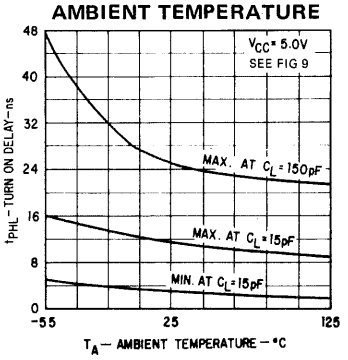


Fig. 12

WORST CASE TURN OFF DELAY OF NON-EXTENDABLE GATE VERSUS AMBIENT TEMPERATURE

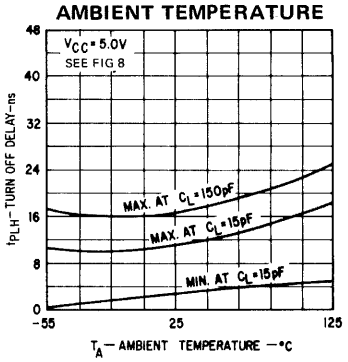


Fig. 13

WORST CASE TURN ON DELAY OF NON-EXTENDABLE GATE VERSUS AMBIENT TEMPERATURE

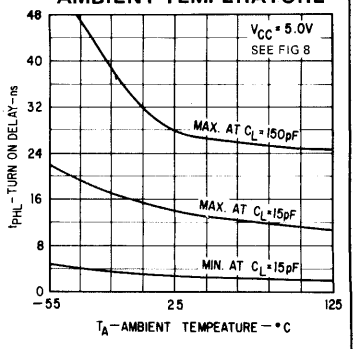
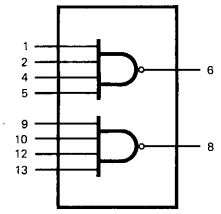


Fig. 14

NAND BUFFER – 9009

The 9009 is a power gate capable of sinking and sourcing large currents for high fan out applications. Logically it is the same as the 9004.

LOGIC DIAGRAM AND PIN CONFIGURATION



V_{CC} = Pin 14
GND = Pin 7

Fig. 1

CIRCUIT DIAGRAM (One Gate)

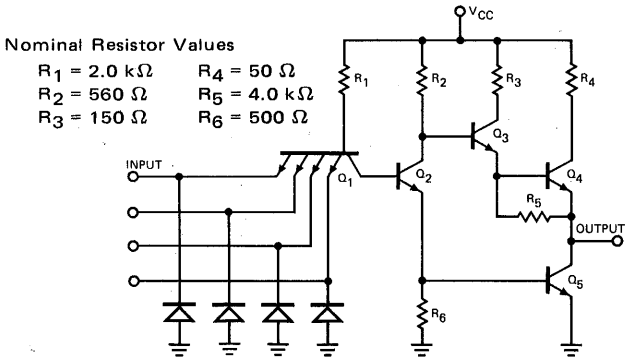


Fig. 2

LOADING FACTORS

PIN NAMES	LOADING
All Inputs	2.0 U.L.
All Outputs	30 U.L. LOW
	90 U.L. HIGH

(1 U.L. = 40 μA HIGH/1.6 mA LOW)

Fig. 3

ELECTRICAL CHARACTERISTICS 9009XC (T_A = 0°C to 75°C, V_{CC} = 5.0 V ±5%)

SYMBOL	PARAMETER	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS 25°C MIN.	LIMITS 25°C TYP.	LIMITS 25°C MAX.	LIMITS 75°C MIN.	LIMITS 75°C MAX.	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage	1.9		1.8			1.6		Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage		0.85			0.85		0.85	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs
V_{OH}	Output HIGH Voltage	2.4		2.4	2.9		2.4		Volts	V_{CC} = 4.75 V, I_{OH} = −3.6 mA, Inputs at V_{IL}
V_{OL}	Output LOW Voltage		0.45		0.21	0.45		0.45	Volts	V_{CC} = 5.25 V, I_{OL} = 48.0 mA, V_{IN} = 5.25 V
										V_{CC} = 4.75 V, I_{OL} = 42.3 mA, Inputs at V_{IH}
I_{IH}	Input HIGH Current				20	120		120	μA	V_{CC} = 5.25 V, V_{IN} = 4.5 V GND on Other Inputs
I_{IL}	Input LOW Current		−3.2		−2.0	−3.2		−3.2	mA	V_{CC} = 5.25 V; V_{IN} = 0.45 V
			−2.82		−1.82	−2.82		−2.82		V_{CC} = 4.75 V; 5.25 V on Other Inputs
I_{CC}	V_{CC} Current, Gate On (each gate)		14.6		8.6	14.6		14.6	mA	Inputs HIGH; V_{CC} = 5.0 V
	V_{CC} Current, Gate Off (each gate)		3.4		2.15	3.4		3.4		Inputs at GND; V_{CC} = 5.0 V
t_{PLH}	Turn Off Delay				3.0	17			ns	V_{CC} = 5.0 V, See Figure 12 C_L = 15 pF
t_{PHL}	Turn On Delay				2.0	13			ns	

ELECTRICAL CHARACTERISTICS 9009XM (T_A = −55°C to 125°C, V_{CC} = 5.0 V ±10%)

SYMBOL	PARAMETER	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS 25°C MIN.	LIMITS 25°C TYP.	LIMITS 25°C MAX.	LIMITS 125°C MIN.	LIMITS 125°C MAX.	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage	2.0		1.7			1.4		Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage		0.8			0.9		0.8	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs
V_{OH}	Output HIGH Voltage	2.4		2.4	2.7		2.4		Volts	V_{CC} = 4.5 V, I_{OH} = −3.96 mA, Inputs at V_{IL}
V_{OL}	Output LOW Voltage		0.4		0.21	0.4		0.4	Volts	V_{CC} = 5.5 V, I_{OL} = 52.8 mA, V_{IN} = 5.5 V
										V_{CC} = 4.5 V, I_{OL} = 40.8 mA, Inputs at V_{IH}
I_{IH}	Input HIGH Current				20	120		120	μA	V_{CC} = 5.5 V, V_{IN} = 4.5V GND on Other Inputs
I_{IL}	Input LOW Current		−3.2		−2.2	−3.2		−3.2	mA	V_{CC} = 5.5 V; V_{IN} = 0.4 V
			−2.48		−1.74	−2.48		−2.48		V_{CC} = 4.5 V; 5.5 V on Other Inputs
I_{CC}	V_{CC} Current, Gate On (each gate)		12.9		8.6	12.9		12.9	mA	Inputs HIGH; V_{CC} = 5.0 V
	V_{CC} Current, Gate Off (each gate)		3.2		2.15	3.2		3.2		Inputs at GND; V_{CC} = 5.0 V
t_{PLH}	Turn Off Delay				4.0	15			ns	V_{CC} = 5.0 V, See Figure 12
t_{PHL}	Turn On Delay				3.0	10			ns	C_L = 15 pF

9009
TYPICAL INPUT AND OUTPUT CHARACTERISTICS

OUTPUT VOLTAGE VERSUS INPUT VOLTAGE

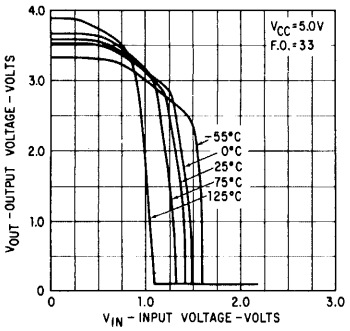


Fig. 4

INPUT CURRENT VERSUS INPUT VOLTAGE

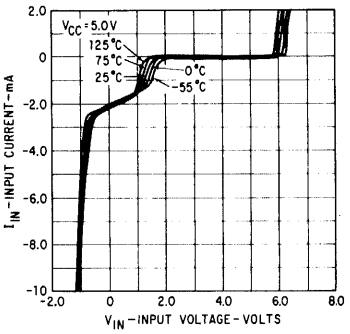


Fig. 5

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE

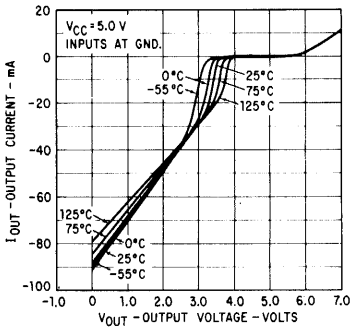


Fig. 6

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)

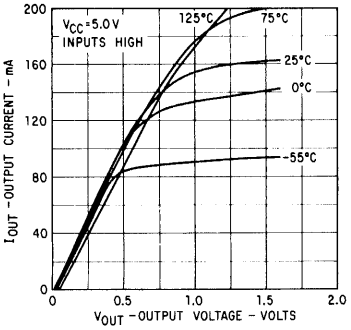


Fig. 7

POWER DISSIPATION, LOGIC LEVELS AND NOISE IMMUNITY

POWER DISSIPATION VERSUS SUPPLY VOLTAGE

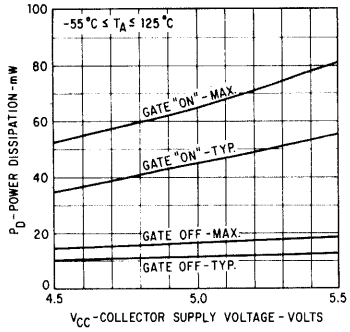


Fig. 8

WORST CASE LOGIC LEVELS VERSUS AMBIENT TEMPERATURE

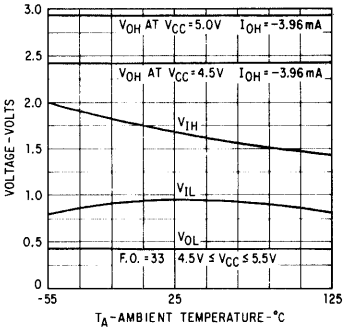


Fig. 9

WORST CASE HIGH LEVEL NOISE IMMUNITY VERSUS AMBIENT TEMPERATURE

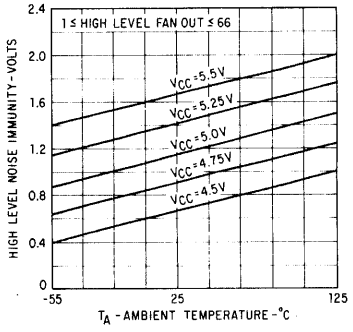


Fig. 10

WORST CASE LOW LEVEL NOISE IMMUNITY VERSUS AMBIENT TEMPERATURE

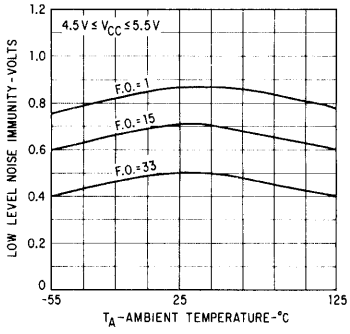
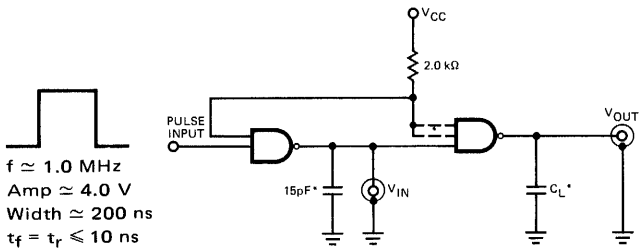


Fig. 11

SWITCHING CHARACTERISTICS

TEST CIRCUIT



WAVEFORM

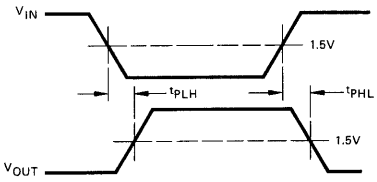


Fig. 12

WORST CASE TURN OFF DELAY VERSUS AMBIENT TEMPERATURE

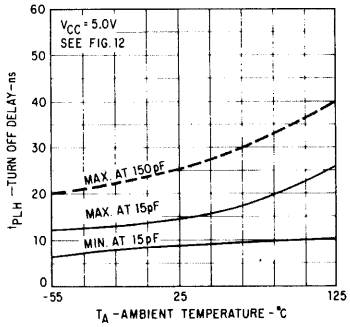


Fig. 13

WORST CASE TURN ON DELAY VERSUS AMBIENT TEMPERATURE

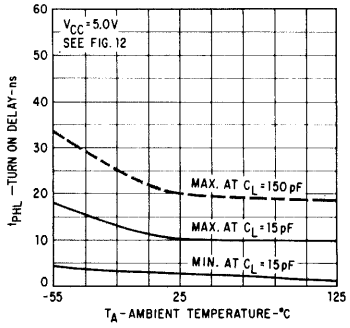
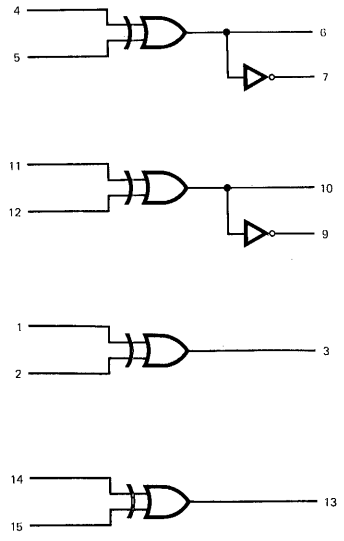


Fig. 14

QUAD EXCLUSIVE OR GATE – 9014

The 9014 consists of four exclusive OR gates, useful in a large number of code conversion, parity generation/checking, and comparison applications. Two of the gates have an additional complemented output for greater system flexibility. The 9014 has high speed, high fanout capabilities and is compatible with all members of the Fairchild TTL family.

LOGIC DIAGRAM



V_{CC} = PIN 16
GND = PIN 8

Fig. 1

CIRCUIT DIAGRAM

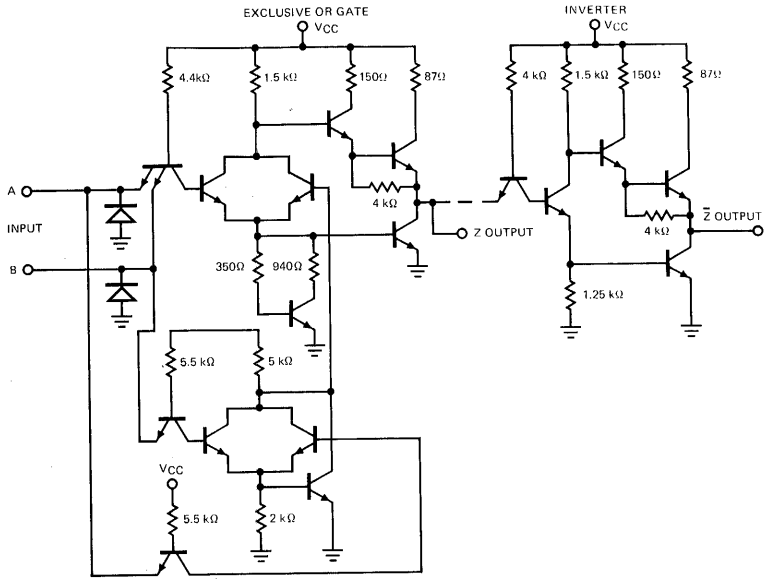


Fig. 2

LOADING FACTORS

PIN NAMES	LOADING (Note a)
All Inputs	1.5 U.L.
Outputs	
3, 7, 9, 13 (Note b)	10 U.L.
6, 10 (Note c)	9 U.L.

NOTES:
a. 1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW
b. 10 U.L. is the output LOW drive factor and 20 U.L. is the output HIGH drive factor.
c. 9 U.L. is the output LOW drive factor and 19 U.L. is the output HIGH drive factor.

Fig. 3

FUNCTIONAL DESCRIPTION – The exclusive OR gate produces an output when the inputs are complementary. Two gates have an additional inverted output which provides directly a compare capability. The Boolean experessions for the gates are: $Z = A\overline{B} + \overline{A}B$; $\overline{Z} = AB + \overline{A}\overline{B}$.

TRUTH TABLE

A	B	Z	$\overline{Z}$
L	L	L	H
L	H	H	L
H	L	H	L
H	H	L	H

H = HIGH Voltage Level
L = LOW Voltage Level

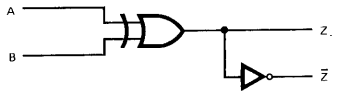
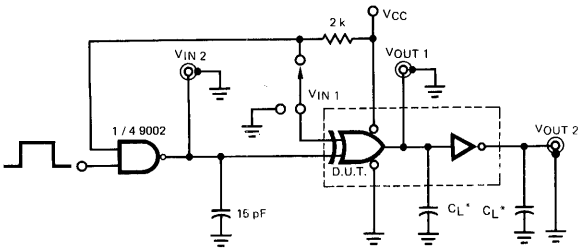


Fig. 4

SWITCHING TEST CIRCUIT



f ≃ 1 MHz
Amp. ≃ 4.0 V
Pulse Width = 200 ± 20 ns
$t_r = t_f \leqslant 10$ ns

Fig. 5

*C_L includes probe and jig capacity

WAVEFORMS

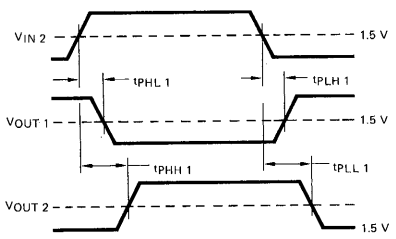


Fig. 6

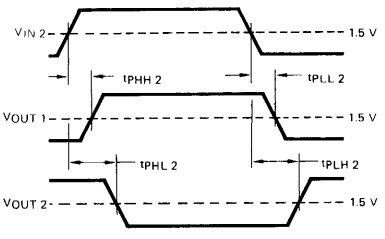


Fig. 7

ELECTRICAL CHARACTERISTICS 9014XC (T_A = 0°C to +75°C, V_{CC} = 5.0 V ±5%)

SYMBOL	PARAMETER	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage	1.9		1.8			1.6		Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage		0.85			0.85		0.85	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs
V_{OH}	Output HIGH Voltage	2.4		2.4	3.1		2.4		Volts	V_{CC} = 4.75 V, I_{OH} = −1.20 mA I_{OH} = −1.14 mA (Pins 6 & 10) Inputs at V_{IL} & V_{IH} per Truth Table
V_{OL}	Output LOW Voltage		0.45		0.29	0.45		0.45	Volts	V_{CC} = 5.25 V, I_{OL} = 16.0 mA I_{OL} = 14.4 mA (Pins 6 & 10) Inputs = 5.25 V or 0 V per Truth Table
			0.45			0.45		0.45	Volts	V_{CC} = 4.75 V, I_{OL} = 14.1 mA I_{OL} = 12.7 mA (Pins 6 & 10) Inputs = 5.25 V or 0 V per Truth Table
I_{IH}	Input HIGH Current				15	90		90	μA	V_{CC} = 5.25 V, V_{IN} = 4.5 V Other Inputs = GND
I_{IL}	Input LOW Current		−2.4		−1.54	−2.4		−2.4	mA	V_{CC} = 5.25 V; V_{IN} = 0.45 V
			−2.1			−2.1		−2.1	mA	V_{CC} = 4.75 V; Other Inputs = 5.25 V
I_{CC}	V_{CC} Current, Gate On (each gate)		4.5		3.15	4.5		4.5	mA	V_{CC} = 5.0 V, One Input = 5.5 V, One Input = GND
	V_{CC} Current, Gate Off (each gate)		8.7		6.06	8.7		8.7	mA	V_{CC} = 5.0 V, Inputs = GND
			7.6		5.38	7.6		7.6	mA	V_{CC} = 5.0 V, Inputs = 5.5 V
	V_{CC} Current Per Inverter — On		6.1		3.6	6.1		6.1	mA	V_{CC} = 5.0 V, Input Node HIGH
	V_{CC} Current Per Inverter — Off		1.7		1.07	1.7		1.7	mA	V_{CC} = 5.0 V, Input Node LOW
t_{PLH} 1	Switching Tests				3.0	8.0	13		ns	V_{CC} = 5.0 V, V_{IN1} = 5.0 V C_L = 15 pF See Figures 5 & 6 on previous page
t_{PHL} 1					3.0	11	15		ns	
t_{PHH} 1					6.0	16	28		ns	
t_{PLL} 1					6.0	16	28		ns	
t_{PHH} 2	Switching Tests				7.0	11	17		ns	V_{CC} = 5.0 V, V_{IN1} = 0 V C_L = 15 pF See Figures 5 & 7 on previous page
t_{PLL} 2					7.0	15	19		ns	
t_{PLH} 2					10	21	32		ns	
t_{PHL} 2					10	20	32		ns	

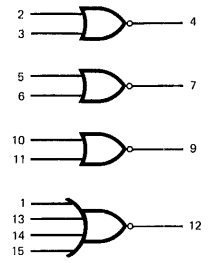
ELECTRICAL CHARACTERISTICS 9014XM (T_A = −55°C to +125°C, V_{CC} = 5.0 V ±10%)

SYMBOL	PARAMETER	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS 125°C MIN.	LIMITS 125°C MAX.	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage	2.0		1.7			1.4		Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage		0.8			0.9		0.8	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs
V_{OH}	Output HIGH Voltage	2.4		2.4	2.9		2.4		Volts	V_{CC} = 4.5 V, I_{OH} = −1.32 mA I_{OH} = −1.20 mA (Pins 6 & 10) Inputs at V_{IL} & V_{IH} per Truth Table
V_{OL}	Output LOW Voltage		0.4		0.27	0.4		0.4	Volts	V_{CC} = 5.5 V, I_{OL} = 17.6 mA I_{OL} = 16 mA (Pins 6 & 10) Inputs = 5.5 V or 0 V per Truth Table
			0.4			0.4		0.4	Volts	V_{CC} = 4.5 V, I_{OL} = 13.6 mA I_{OL} = 12.4 mA (Pins 6 & 10) Inputs = 5.5 V or 0 V per Truth Table
I_{IH}	Input HIGH Current				10	90		90	μA	V_{CC} = 5.5 V, V_{IN} = 4.5 V Other Inputs = GND
I_{IL}	Input LOW Current		−2.4		−1.65	−2.4		−2.4	mA	V_{CC} = 5.5 V; V_{IN} = 0.4 V
			−1.86			−1.86		−1.86	mA	V_{CC} = 4.5 V; Other Inputs = 5.5 V
I_{CC}	V_{CC} Current, Gate On (each gate)		4.2		3.15	4.2		4.2	mA	V_{CC} = 5.0 V, One Input = 5.5 V, One Input = GND
	V_{CC} Current, Gate Off (each gate)		8.1		6.06	8.1		8.1	mA	V_{CC} = 5.0 V, Inputs = GND
			7.2		5.38	7.2		7.2	mA	V_{CC} = 5.0 V, Inputs = 5.5 V
	V_{CC} Current Per Inverter — On		5.5		3.5	5.5		5.5	mA	V_{CC} = 5.0 V, Input Node HIGH
	V_{CC} Current Per Inverter — Off		1.6		1.07	1.6		1.6	mA	V_{CC} = 5.0 V, Input Node LOW
t_{PLH} 1	Switching Tests				3.0	7.0	10		ns	V_{CC} = 5.0 V, V_{IN1} = 5.0 V C_L = 15 pF See Figures 5 & 6 on previous page
t_{PHL} 1					3.0	8.0	12		ns	
t_{PHH} 1					6.0	14	22		ns	
t_{PLL} 1					6.0	14	22		ns	
t_{PHH} 2	Switching Tests				7.0	10	14		ns	V_{CC} = 5.0 V, V_{IN1} = 0 V C_L = 15 pF See Figures 5 & 7 on previous page
t_{PLL} 2					7.0	12	16		ns	
t_{PLH} 2					10	18	26		ns	
t_{PHL} 2					10	17	26		ns	

QUAD NOR GATE – 9015

The TTL 9015 consists of three 2-input and one 4-input NOR gates. The NOR gate produces a LOW output if any of the inputs are HIGH.

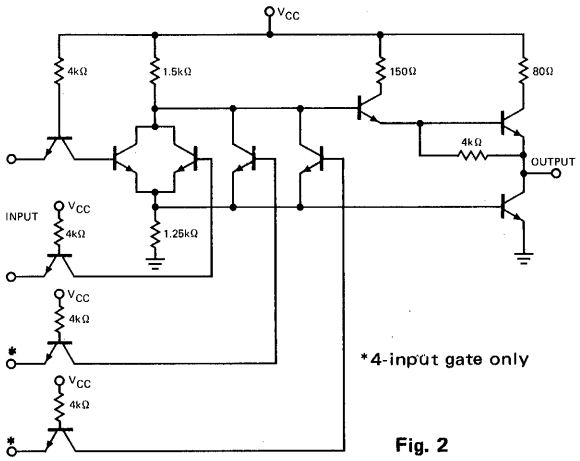
LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

Fig. 1

CIRCUIT DIAGRAM



*4-input gate only

Fig. 2

LOADING FACTORS

PIN NAMES	LOADING
All Inputs	1 U.L.
All Outputs	10 U.L.

(1 U.L. = 40 μA HIGH/1.6 mA LOW)

Fig. 3

SWITCHING WAVEFORMS

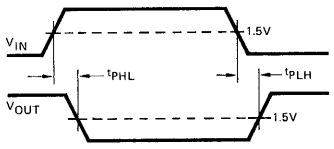


Fig. 4

ELECTRICAL CHARACTERISTICS 9015XC (0°C to +75°C, V_{CC} = 5.0 V ±5%)

SYMBOL	PARAMETER	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage	1.9		1.8			1.6		Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage		0.85			0.85		0.85	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs
V_{OH}	Output HIGH Voltage	2.4		2.4	2.9		2.4		Volts	V_{CC} = 4.75 V, I_{OH} = −1.2 mA, Inputs = V_{IL}
V_{OL}	Output LOW Voltage		0.45		0.21	0.45		0.45	Volts	V_{CC} = 5.25 V, I_{OL} = 16.0 mA, Inputs = 5.25 V
			0.45		0.21	0.45		0.45	Volts	V_{CC} = 4.75 V, I_{OL} = 14.1 mA, Inputs = V_{IH}
I_{IH}	Input HIGH Current				10	60		60	μA	V_{CC} = 5.25 V, GND on Other Inputs
I_{IL}	Input LOW Current		−1.6		−1.0	−1.6		−1.6	mA	V_{CC} = 5.25 V, V_{IN} = 0.45 V
			−1.41		−0.91	−1.41		−1.41	mA	V_{CC} = 4.75 V, 5.25 V on Other Inputs
I_{CC}	V_{CC} Current, Gate On (each gate)		6.55		4.25	6.55		6.55	mA	Inputs HIGH; V_{CC} = 5.0 V
			8.75		5.7	8.75		8.75	mA	Inputs HIGH (4-Input Gate Only); V_{CC} = 5.0 V
	V_{CC} Current, Gate Off (each gate)		3.38		2.2	3.38		3.38	mA	Inputs LOW; V_{CC} = 5.0 V
			6.77		4.4	6.77		6.77	mA	Inputs LOW (4-Input Gate Only); V_{CC} = 5.0 V
t_{PLH}	Turn Off Delay				3.0	7.0	13		ns	V_{CC} = 5.0 V, C_L = 15 pF
t_{PHL}	Turn On Delay				3.0	9.0	15		ns	(See Figure 4)

ELECTRICAL CHARACTERISTICS 9015XM (−55°C to +125°C, V_{CC} = 5.0 V ±10%)

SYMBOL	PARAMETER	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage	2.0		1.7			1.4		Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage		0.8			0.9		0.8	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs
V_{OH}	Output HIGH Voltage	2.4		2.4	2.7		2.4		Volts	V_{CC} = 4.5 V, I_{OH} = −1.32 mA, Inputs = V_{IL}
V_{OL}	Output LOW Voltage		0.4		0.21	0.4		0.4	Volts	V_{CC} = 5.5 V, Inputs = 5.5 V, I_{OL} = 17.6 mA
			0.4		0.21	0.4		0.4	Volts	V_{CC} = 4.5 V, V_{IN} = V_{IH}, I_{OL} = 13.6 mA
I_{IH}	Input HIGH Current				10	60		60	μA	V_{CC} = 5.5 V, V_{IN} = 4.5 V GND on Other Inputs
I_{IL}	Input LOW Current		−1.6		−1.1	−1.6		−1.6	mA	V_{CC} = 5.5 V, V_{IN} = 0.4 V
			−1.24		−0.87	−1.24		−1.24	mA	V_{CC} = 4.5 V, 5.5 V on Other Inputs
I_{CC}	V_{CC} Current, Gate On (each gate)		6.07		4.25	6.07		6.07	mA	Inputs HIGH; V_{CC} = 5.0 V
			8.14		5.7	8.14		8.14	mA	Inputs HIGH (4-Input Gate Only); V_{CC} = 5.0 V
	V_{CC} Current, Gate Off (each gate)		3.2		2.2	3.2		3.2	mA	Inputs LOW; V_{CC} = 5.0 V
			6.4		4.4	6.4		6.4	mA	Inputs LOW (4-Input Gate Only); V_{CC} = 5.0 V
t_{PLH}	Turn Off Delay				3.0	6.0	10		ns	V_{CC} = 5.0 V, C_L = 15 pF
t_{PHL}	Turn On Delay				3.0	8.0	12		ns	(See Figure 4)

5

JK FLIP-FLOPS – 9000, 9001
DUAL JK FLIP-FLOPS – 9020, 9022

DESCRIPTION – The TTL 9000 series has four flip-flops to satisfy the storage requirements of a logic system. All are master/slave JK designs and have the same high speed and high noise immunity as the rest of the 9000 series. As with the gates, all inputs have diode clamps to reduce ringing caused by long lines and impedance mismatches.

The JK type flip-flop was chosen for all flip-flop elements in this family because of its inherent logic power. The input function required to produce a given sequence of states for a JK flip-flop will, in general, contain more "don't care" conditions than the corresponding function for an RS flip-flop. These additional "don't care" conditions will, in most cases, reduce the amount of gating elements required to implement the input function.

The master/slave design offers the advantage of a dc threshold on the clock input initiating the transition of the outputs, so that careful control of clock pulse rise and fall times is not required.

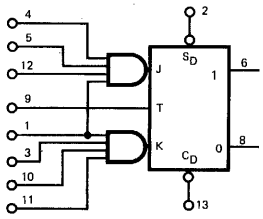
Data is accepted by the master while the clock is in the LOW state. Refer to the truth table for definition of HIGH and LOW data. Transfer from the master to the slave occurs on the LOW to HIGH transition of the clock. When the clock is HIGH, the J and K inputs are inhibited.

A joint (JK) input is provided for all flip-flops in this family. This common input removes the necessity of gating the clock signal with an external gate in many applications. This not only reduces package count, but also reduces the possibility of clock skew problems, since with internal gating provided, all flip-flops may be driven from a common clock line. Several TTL drivers may be used in parallel to drive this common clock line if the load exceeds the F.O. capability of the 9009 buffer.

The asynchronous inputs provide ability to control the state of the flip-flop independent of static conditions of the clock and synchronous inputs. Both asynchronous set and clear are provided on all flip-flops except the 9020, which because of a logic trade-off has only clear inputs. The set or clear pin being LOW absolutely guarantees that one output will be HIGH, but if opposing data is present at the synchronous inputs and the flip-flop is clocked, the LOW output may momentarily spike HIGH synchronous with a positive transition of the clock. If the LOW output of the flip-flop is connected to other flip-flop inputs clocked from the same line, the spike will be masked by the clock. If the clock is suspended during the time when the asynchronous inputs are activated, no spike will occur. When the spikes can cause problems, a simple solution is to common the joint JK inputs with the synchronous set or reset signal.

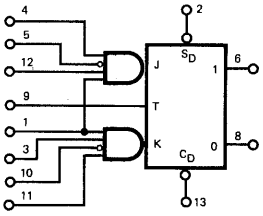
LOGIC DIAGRAMS

9000



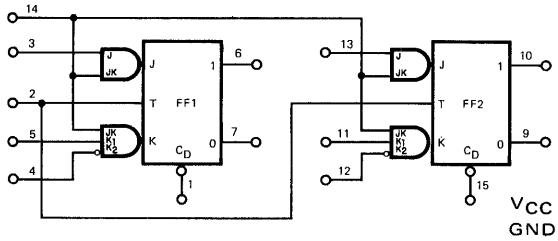
V_{CC} = 14
GND = 7

9001



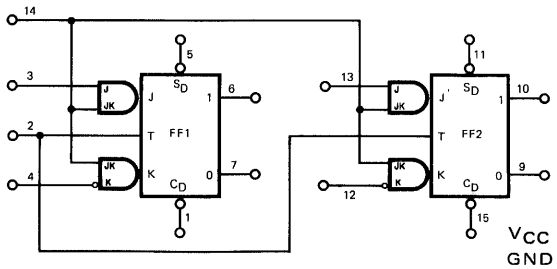
V_{CC} = 14
GND = 7

9020



V_{CC} = 16
GND = 8

9022

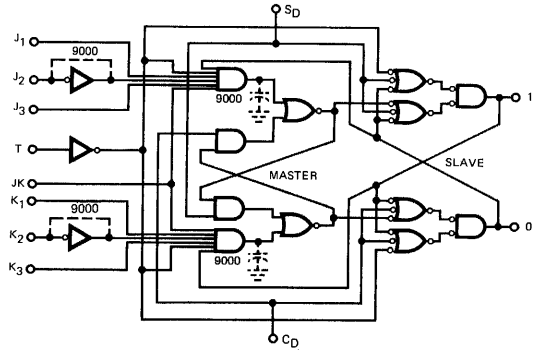


V_{CC} = 16
GND = 8

Fig. 1

FUNCTIONAL LOGIC DIAGRAMS

9000/9001



9020/9022

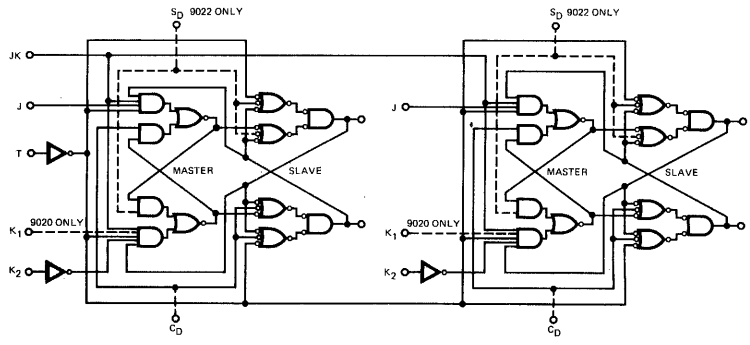


Fig. 2

TRUTH TABLES

SYNCHRONOUS OPERATION

BEFORE CLOCK				AFTER CLOCK	
OUTPUTS		INPUTS		OUTPUTS	
ONE	ZERO	J	K	ONE	ZERO
L	H	L*	X	L	H
L	H	H*	X	H	L
H	L	X	L*	H	L
H	L	X	H*	L	H

ASYNCHRONOUS OPERATION

INPUTS		OUTPUTS	
S_D	C_D	ONE	ZERO
L	L	H	H
L	H	H	L
H	L	L	H
H	H	SYNCHRONOUS INPUTS CONTROL	

SYNCHRONOUS OPERATION – The truth table defines the next state of the flip-flop after a LOW to HIGH transition of the clock pulse. The next state is a function of the present state and the J and K inputs as shown in the table.

The J and K inputs in the table refer to the basic flip-flop J and K inputs as indicated on the logic diagrams. These internal inputs are for every flip-flop the result of a logic operation on the external J and K inputs. This operation is represented symbolically by AND gates in the logic diagram for each flip-flop. Logic diagrams are in accordance with MIL Standard 806B.

The L* symbol in the J and K input column is defined as meaning that **input does not go HIGH at any time while the clock is LOW.**

The H* symbol in the J or K input column is defined as meaning that the **input is HIGH at some time while the clock is LOW.**

The X symbol indicates that the condition of that input has no effect on the next state of the flip-flop.

The H and L symbols refer to steady state HIGH and LOW voltage levels, respectively.

UNUSED INPUTS – The 9001, 9020 and 9022 all have active level LOW synchronous inputs. When not in use they must be grounded. All other unused inputs, including asynchronous, should be tied HIGH for maximum operating speed.

5

ELECTRICAL CHARACTERISTICS 9000XC, 9001XC, 9020XC AND 9022XC (T_A = 0°C to 75°C, V_{CC} = 5.0 V ±5%)

SYMBOL	PARAMETER	LIMITS 0°C MIN.	0°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	75°C MIN.	75°C MAX.	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage	1.9		1.8			1.6		Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs	
V_{IL}	Input LOW Voltage		0.85			0.85		0.85	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs	
V_{OH}	Output HIGH Voltage	2.4		2.4	3.0		2.4		Volts	V_{CC} = 4.75 V, I_{OH} = −1.2 mA	
V_{OL}	Output LOW Voltage		0.45		0.21	0.45		0.45	Volts	V_{CC} = 4.75 V, I_{OL} = 14.1 mA	
										V_{CC} = 5.25 V, I_{OL} = 16 mA	
I_{IH}	Input HIGH Current All J, K Inputs T Inputs 9000, 9001				5.0	60		60	μA	V_{CC} = 5.25 V, V_{IN} = 4.5 V GND on Other Inputs	
	JK Inputs 9000, 9001 T Inputs 9020, 9022				10	120		120			
	JK Inputs 9020, 9022				20	240		240			
	S_D, C_D (all Flip-Flops)				14	160		160			
I_{IL}	Input LOW Current All J, K Inputs T Inputs 9000, 9001		−1.60		−1.0	−1.60		−1.60	mA	V_{CC} = 5.25 V	V_{IN} = 0.45 V 5.25 V on Other Inputs
	JK Inputs 9000, 9001 T Inputs 9020, 9022		−3.20		−2.0	−3.20		−3.20			
	JK Inputs 9020, 9022		−6.40		−4.0	−6.40		−6.40			
	S_D, C_D (all Flip-Flops)		−4.32		−2.7	−4.32		−4.32			
	Input LOW Current All J, K Inputs T Inputs 9000, 9001		−1.41		−0.94	−1.41		−1.41	mA	V_{CC} = 4.75 V	
	JK Inputs 9000, 9001 T Inputs 9020, 9022		−2.82		−1.88	−2.82		−2.82			
	JK Inputs 9020, 9022		−5.64		−3.76	−5.64		−5.64			
	S_D C_D (all Flip-Flops)		−3.78		−2.54	−3.78		−3.78			
I_{CC}	V_{CC} Current 9000		28			28		28	mA	S_D at GND	V_{CC} = 5.0 V
	9001		33			33		33		S_D at GND	
	9020, 9022 each Flip-Flop		30			30		30		C_{D1}, C_{D2} at GND	

LOADING FACTORS

9000

PIN NAMES	LOADING (Note a)
JK	2 U.L.
$J_1, J_2, J_3, K_1, K_2, K_3, T$	1 U.L.
S_D, C_D	3 U.L.
Outputs (Note b)	10 U.L.

9001

PIN NAMES	LOADING (Note a)
JK	2 U.L.
$J_1, J_2, J_3, K_1, K_2, K_3, T$	1 U.L.
S_D, C_D	3 U.L.
Outputs (Note b)	10 U.L.

9020

PIN NAMES	LOADING (Note a)
JK	4 U.L.
J, K_1, K_2	1 U.L.
T	2 U.L.
C_D	3 U.L.
Outputs (Note b)	10 U.L.

9022

PIN NAMES	LOADING (Note a)
JK	4 U.L.
J, K	1 U.L.
T	2 U.L.
C_D	3 U.L.
Outputs (Note b)	10 U.L.

NOTES:

a. 1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW; the HIGH load factor of 40 μA measured at 2.4 V is considered equivalent to 60 μA measured at 4.5 V for purposes of system loading calculations.

b. 10 U.L. is the LOW drive factor and 30 U.L. is the HIGH drive factor.

Fig. 3

ELECTRICAL CHARACTERISTICS 9000XM, 9001XM, 9020XM AND 9022XM ($T_A = -55°C$ to $125°C$, $V_{CC} = 5.0$ V ±10%)

SYMBOL	PARAMETER	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS 25°C MIN.	LIMITS 25°C TYP.	LIMITS 25°C MAX.	LIMITS 125°C MIN.	LIMITS 125°C MAX.	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage	2.0		1.7			1.4		Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs	
V_{IL}	Input LOW Voltage		0.8			0.9		0.8	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs	
V_{OH}	Output HIGH Voltage	2.4		2.4	2.7		2.4		Volts	$V_{CC} = 4.5$ V, $I_{OH} = -1.2$ mA	
V_{OL}	Output LOW Voltage		0.4		0.21	0.4		0.4	Volts	$V_{CC} = 4.5$ V, $I_{OL} = 12.4$ mA	
										$V_{CC} = 5.5$ V, $I_{OL} = 16.0$ mA	
I_{IH}	Input HIGH Current All J, K Inputs T Inputs 9000, 9001				5.0	60		60	μA	$V_{CC} = 5.5$ V, $V_{IN} = 4.5$ V GND on Other Inputs	
	JK Inputs 9000, 9001 T Inputs 9020, 9022				10	120		120			
	JK Inputs 9020, 9022				20	240		240			
	S_D, C_D (all Flip-Flops)				14	160		160			
I_{IL}	Input LOW Current All J, K Inputs T Inputs 9000, 9001		−1.60		−1.1	−1.60		−1.60	mA	$V_{CC} = 5.5$ V	$V_{IN} = 0.4$ V 5.5 V GND on Other Inputs
	JK Inputs 9000, 9001 T Inputs 9020, 9022		−3.20		−2.2	−3.20		−3.20			
	JK Inputs 9020, 9022		−6.40		−4.4	−6.40		−6.40			
	S_D, C_D (all Flip-Flops)		−4.32		−2.97	−4.32		−4.32			
	Input LOW Current All J, K Inputs T Inputs 9000, 9001		−1.24		−0.87	−1.24		−1.24	mA	$V_{CC} = 4.5$ V	
	JK Inputs 9000, 9001 T Inputs 9020, 9022		−2.48		−1.74	−2.48		−2.48			
	JK Inputs 9020, 9022		−4.96		−3.48	−4.96		−4.96			
	S_D, C_D (all Flip-Flops)		−3.35		−2.35	−3.75		−3.35			
I_{CC}	V_{CC} Current 9000		24		13	24		24		S_D at GND	$V_{CC} = 5.0$ V
	9001		28		14	28		28	mA	S_D at GND	
	9020, 9022 each Flip-Flop		27		14	27		27		C_{D1}, C_{D2}, at GND	

TYPICAL INPUT AND OUTPUT CHARACTERISTICS 9000, 9001, 9020 AND 9022

OUTPUT VOLTAGE VERSUS INPUT VOLTAGE ASYNCHRONOUS INPUTS

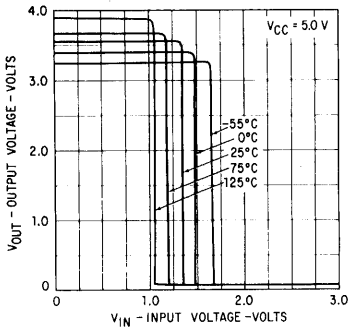


Fig. 4

CLOCK OUTPUT VOLTAGE VERSUS INPUT VOLTAGE

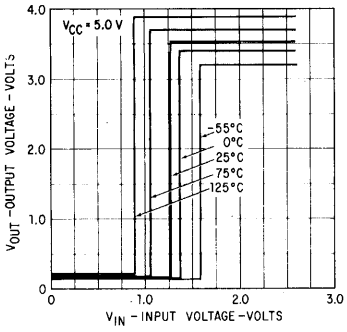


Fig. 5

INPUT CURRENT VERSUS INPUT VOLTAGE 9004

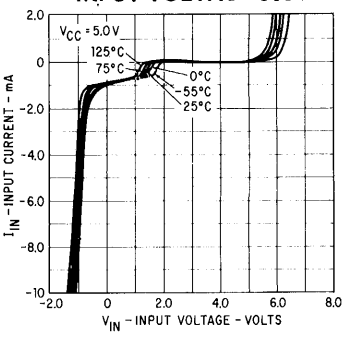


Fig. 6

INPUT CURRENT VERSUS INPUT VOLTAGE 9009

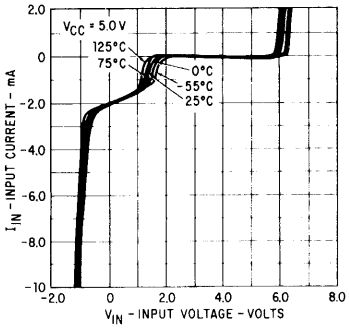


Fig. 7

INPUT CURRENT VERSUS INPUT VOLTAGE JK INPUT 9000, 9001

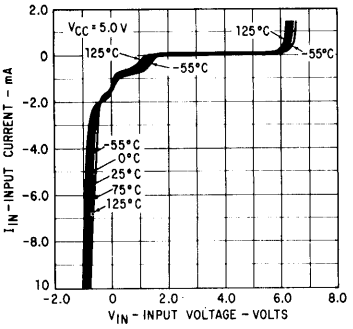


Fig. 8

INPUT CURRENT VERSUS INPUT VOLTAGE JK INPUT 9020, 9022

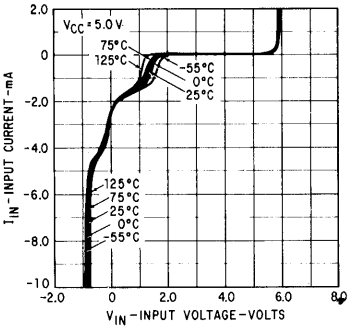


Fig. 9

INPUT CURRENT VERSUS INPUT VOLTAGE ASYNCHRONOUS INPUTS – ALL FLIP-FLOPS

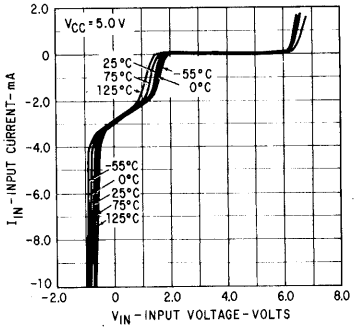


Fig. 10

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)

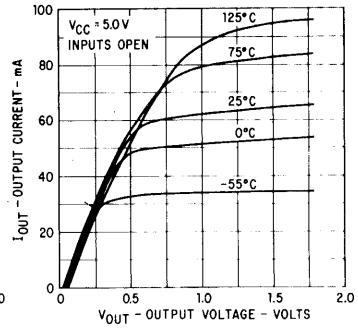


Fig. 11

SWITCHING CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V, C_L = C_1 = 15 pF of all flip-flops unless otherwise noted)

SYMBOL	PARAMETER			LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	FIGURES
t_{PLH}	Clock to Output				12	20	ns	17, 18, 19
	S_D or C_D to Output				12	20	ns	17, 18, 19
t_{PHL}	Clock to Output				20	30	ns	17, 18, 19
	S_D or C_D to Output				25	35	ns	17, 18, 19
$t_{set\text{-}up}$	J, K or JK	9000XM		30	22		ns	17, 19
		9000XC		35	22			
		9001XM, 9020XM, 9022XM		10	8		ns	17, 18, 19
		9001XC, 9020XC, 9022XC		15	8			
	$\overline{J}$ or $\overline{K}$ Data Entry			17	12			
$t_{release}$	J, K or JK	9000 only			18	10	ns	17, 19
		9001, 9020, 9022			7	1.0	ns	17, 18, 19
	$\overline{J}$ or $\overline{K}$ Data Entry				11	4.0		
Pulse Widths	Clock	9000 only	Positive		20		ns	17, 19
			Negative		25		ns	17, 19
		9001, 9020, 9022	Positive		8.0		ns	17, 18, 19
			Negative		10		ns	17, 18, 19
	S_D or C_D		Negative		25		ns	17, 18, 19
Toggle Frequency			9000 only		20		MHz	17, 19
			9001, 9020, 9022		50		MHz	17, 18, 19

MAX. AND MIN. PROPAGATION DELAYS VERSUS AMBIENT TEMPERATURE T TO OUTPUT

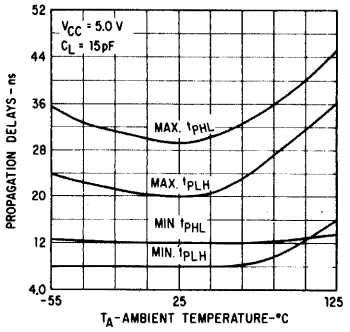


Fig. 12

MAX. AND MIN. PROPAGATION DELAYS VERSUS AMBIENT TEMPERATURE ASYNCHRONOUS INPUTS TO OUTPUTS

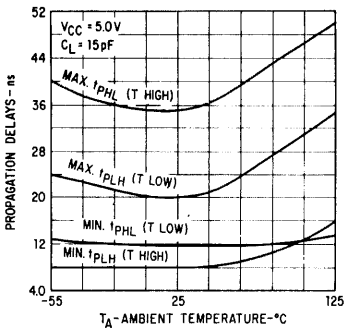


Fig. 13

INCREASE IN ASYNCHRONOUS OR CLOCK INPUT DUE TO OUTPUT CAPACITANCE

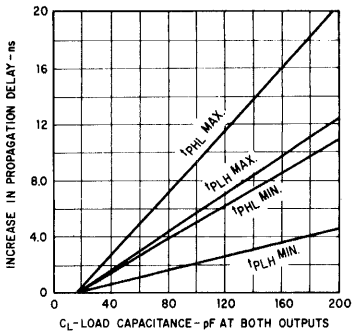


Fig. 14

9001 – 9020 – 9022 SET-UP/RELEASE TIME AND NEGATIVE CLOCK PULSE WIDTH VERSUS AMBIENT TEMPERATURE

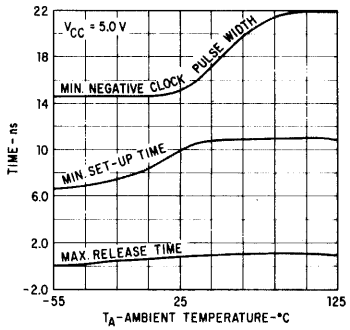


Fig. 15

9000 NEGATIVE CLOCK PULSE WIDTH SET-UP/RELEASE TIME VERSUS AMBIENT TEMPERATURE

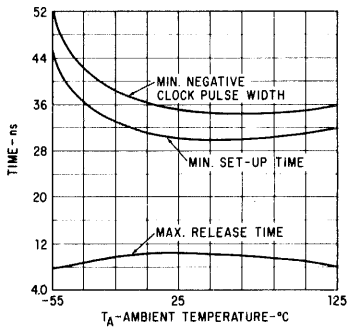
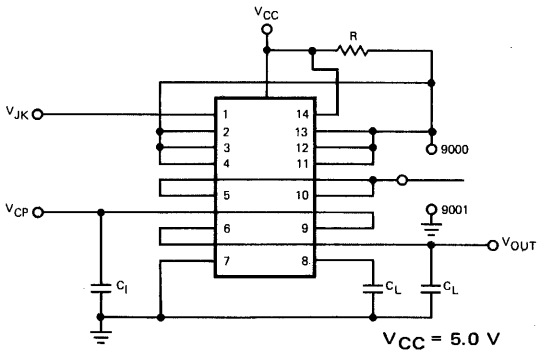


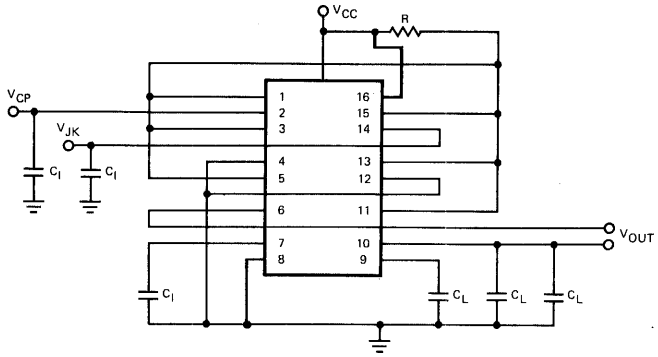
Fig. 16

SWITCHING TEST CIRCUITS

9000/9001



9020/9022



V_{CC} = 5.0 V
R = 2.0 kΩ
C_l = C_L = 15 pF including probe and jig capacitance

Fig. 17 Fig. 18

WAVEFORMS

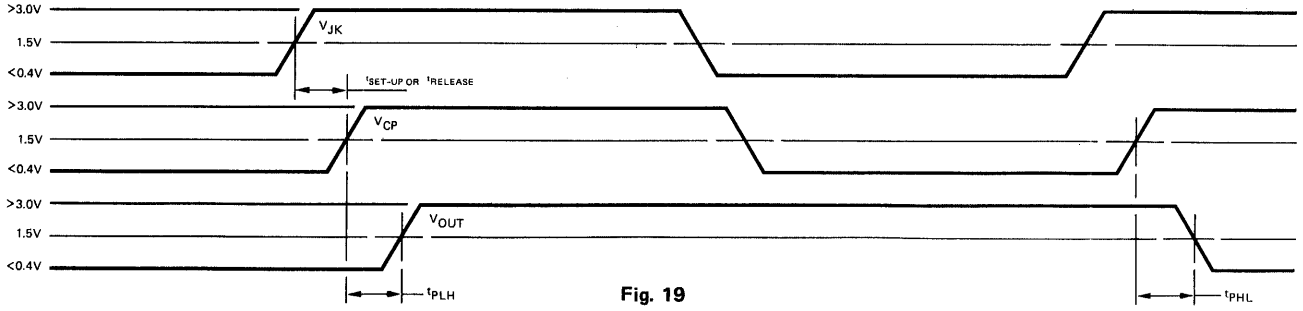


Fig. 19

SWITCHING TEST NOTES

t_{PLH} and t_{PHL}

1. V_{JK} should be kept at the HIGH logic level when performing t_{PLH}/t_{PHL} tests.
2. Drive the clock pulse input with a suitable pulse source. t_{PLH} and t_{PHL} delays are as defined in the waveforms.

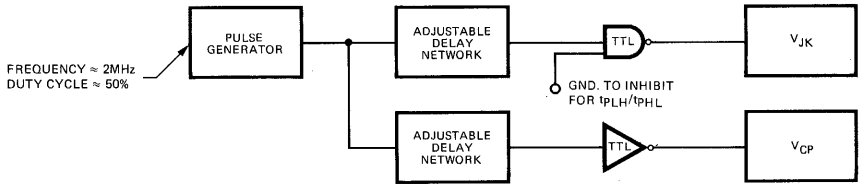
$t_{set\text{-}up}$

1. $t_{set\text{-}up}$ is defined as the minimum time required for a HIGH to be present at a synchronous logic input at any time during the LOW state of the clock in order for the flip-flop to respond to the data.
2. The test for $t_{set\text{-}up}$ is performed by adjusting the timing relationship between the V_{CP} and V_{JK} inputs to the $t_{set\text{-}up}$ minimum value. A device that passes the test will have the output waveform shown. The output of a device that does not pass the $t_{set\text{-}up}$ test will remain at a static logic level (no switching will occur).

$t_{release}$

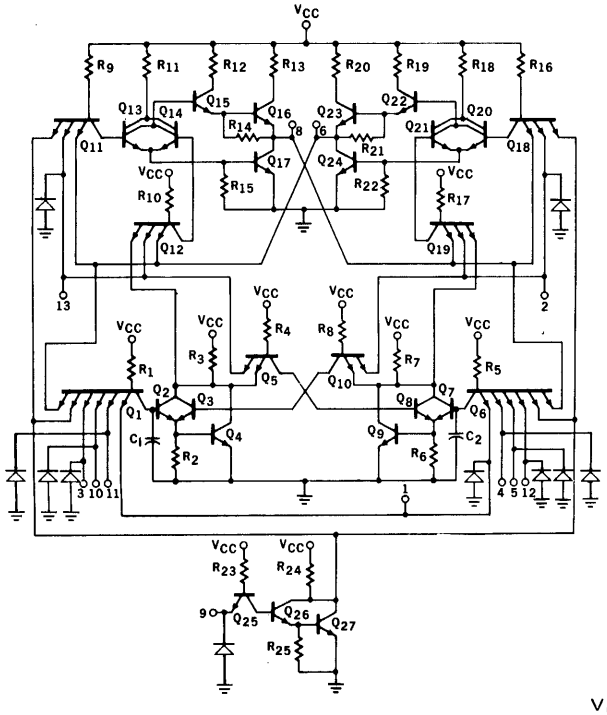
1. $t_{release}$ is defined as the maximum time allowed for a HIGH to be present at a synchronous logic input at any time during the LOW state of the clock and not be recognized.
2. The test for $t_{release}$ is performed by adjusting the timing relationship between V_{CP} and V_{JK} to the $t_{release}$ maximum value. The outputs of devices that pass will remain at static logic levels. In order to check both J and K sides of the flip-flop it is necessary to perform the test with the flip-flop in each of its two possible states, i.e., set and clear. This can be accomplished by making use of the appropriate direct inputs to establish the state before a test. The outputs of devices that do not pass the $t_{release}$ test will exhibit pulses instead of static levels.

RECOMMENDED INPUT PULSE SOURCES

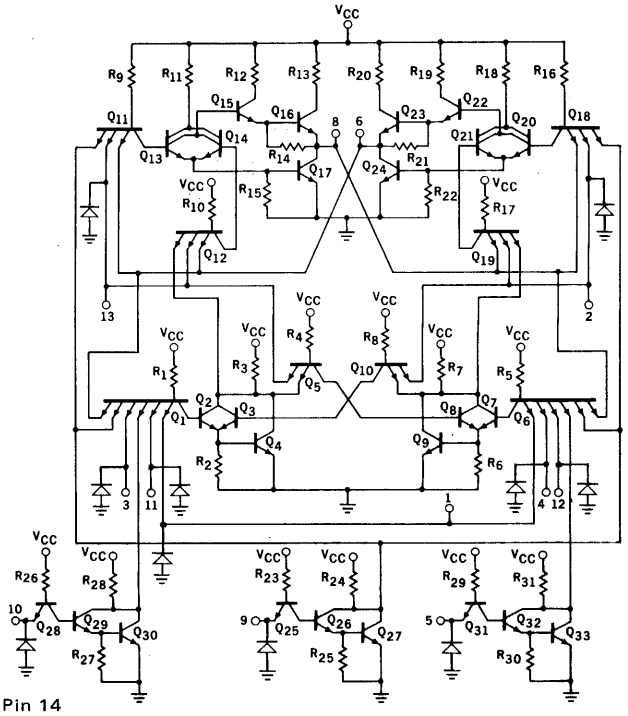


DTL9932 gates with adjustable capacitors connected from extender inputs to ground make suitable delay elements.

9000 SCHEMATIC DIAGRAM

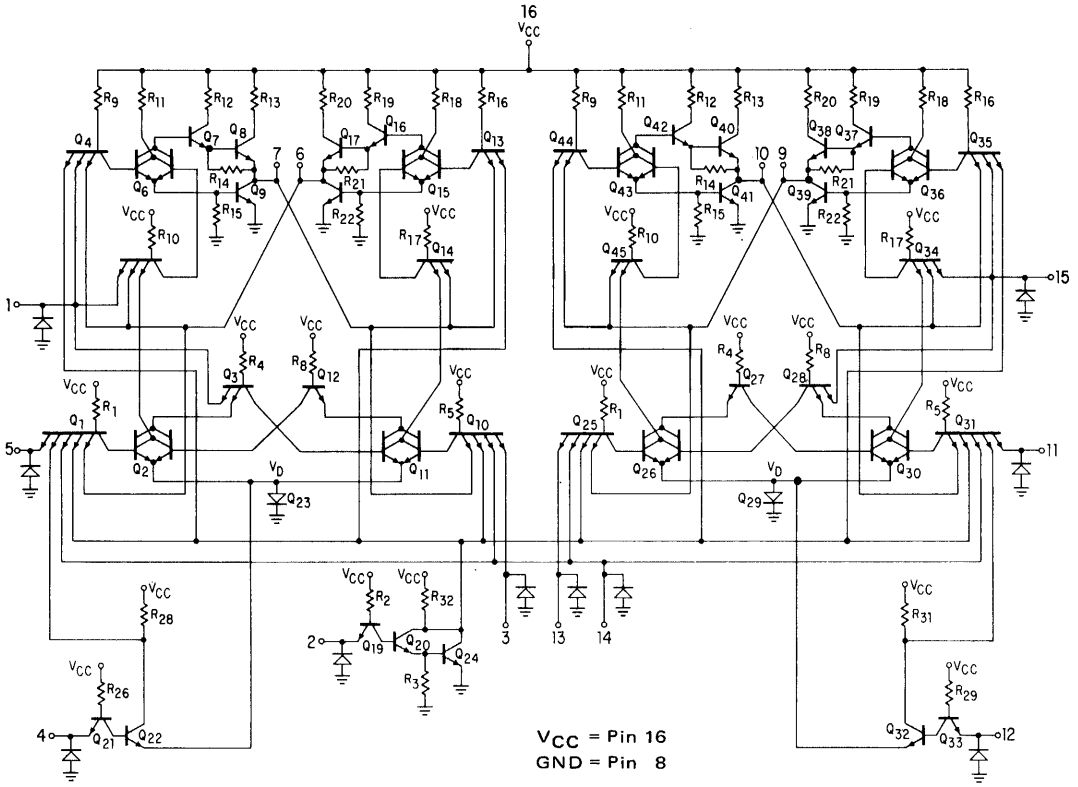


9001 SCHEMATIC DIAGRAM



V_{CC} = Pin 14
GND = Pin 7

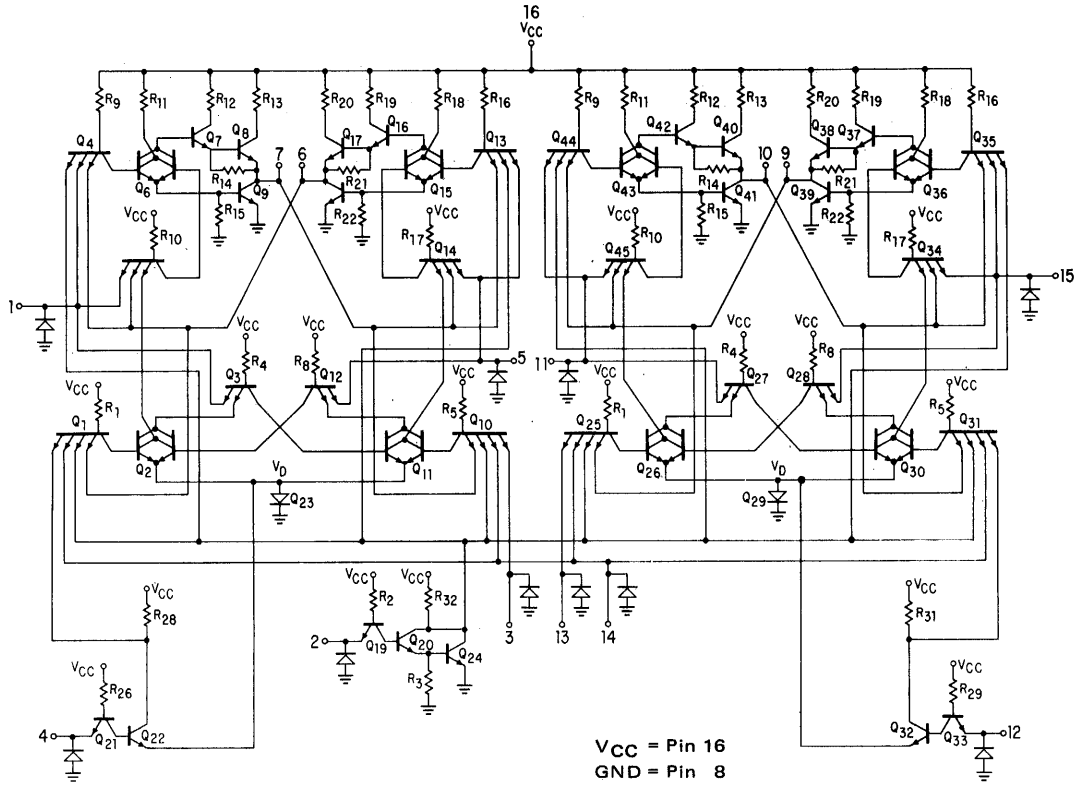
9020 SCHEMATIC DIAGRAM



NOMINAL COMPONENT VALUES (ALL FLIP-FLOPS)

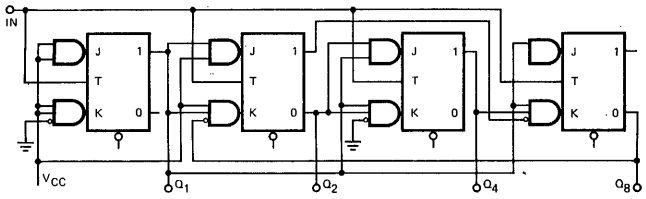
R_1, R_4, R_5, R_8, R_{10}, R_{14}, R_{17}, R_{21}, R_{22}, R_{23}, R_{24}, R_{26}, R_{29} = 4.0 kΩ
R_2, R_3, R_6, R_7 = 2.0 kΩ
R_9, R_{16}, R_{28}, R_{31} = 6.0 kΩ
R_{11}, R_{18} = 1.5 kΩ
R_{12}, R_{19} = 150 Ω
R_{13}, R_{20} = 80 Ω
R_{15}, R_{22}, R_{25}, R_{27}, R_{30} = 1.25 kΩ
R_{32} = 1.0 kΩ
C_1, C_2 = 10 pF

9022 SCHEMATIC DIAGRAM



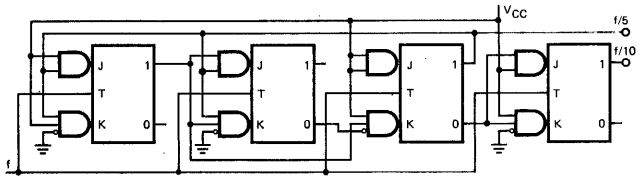
APPLICATIONS

SYNCHRONOUS BDC COUNTER



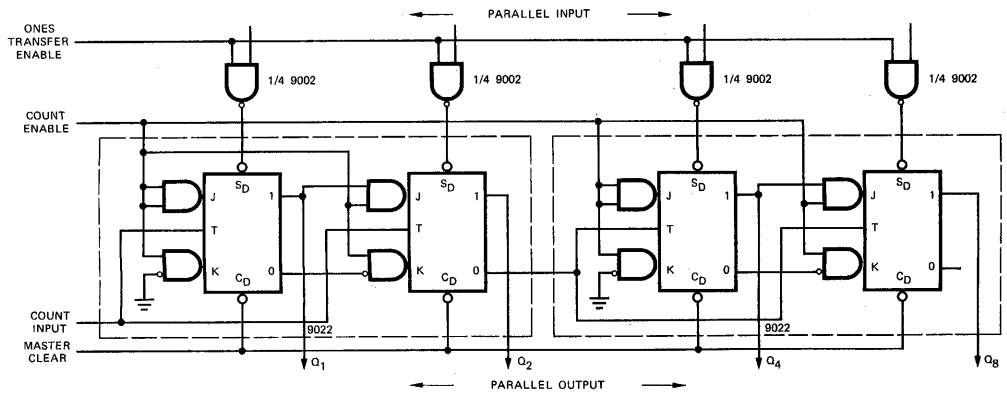
Two TTL 9020 Dual Flip-Flops require no additional gating to produce a fully synchronous 8421 code BCD Counter.

DIVIDE BY TEN COUNTER



Two TTL 9020 Dual Flip-Flops require no additional gating elements to produce divide by ten circuit with a square wave divide by ten output and a divide by five output.

BINARY COUNTER WITH ASYNCHRONOUS PARALLEL LOAD AND CLEAR



Binary counter using synchronous 2-bit stages with trickle down between stages illustrates method of utilizing dual JK flip-flops having common clocks in counter applications.

DUAL J$\overline{K}$ (OR D) FLIP-FLOP – 9024

The 9024 consists of two high speed, completely independent transition clocked J$\overline{K}$ flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The J$\overline{K}$ design allows operation as a D flip-flop by simply connecting the J and $\overline{K}$ pins together.

LOGIC DIAGRAM

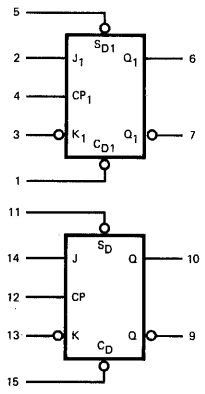


Fig.1

FUNCTIONAL LOGIC DIAGRAM

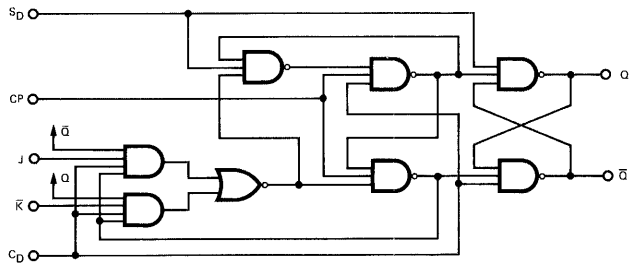


Fig. 2

LOADING FACTORS

PIN NAMES	LOADING (Note a)
J, $\overline{K}$	1 U.L.
Clock, S_D	2 U.L.
C_D	3 U.L.
Outputs (Note b)	10 U.L.

Fig. 3

NOTES:

a. 1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW; the HIGH load factor of 40 μA measured at 2.4 V is considered equivalent to 60 μA measured at 4.5 V for purposes of system loading calculations.

b. 10 U.L. is the LOW drive factor and 30 U.L. is the HIGH drive factor.

TRUTH TABLES

SYNCHRONOUS ENTRY J-$\overline{K}$ MODE OPERATION

INPUTS AT t_n		OUTPUTS AT t_{n+1}	
J	$\overline{K}$	Q	$\overline{Q}$
L	H	No Change	
L	L	L	H
H	H	H	L
H	L	Toggles	

SYNCHRONOUS ENTRY D MODE OPERATION

INPUTS AT t_n	OUTPUTS AT t_{n+1}	
D	Q	$\overline{Q}$
L	L	H
H	H	L

ASYNCHRONOUS ENTRY INDEPENDENT OF CLOCK & SYNCHRONOUS INPUTS

INPUTS		OUTPUTS	
S_D 5(11)	C_D 1(15)	Q 6(10)	$\overline{Q}$ 7(9)
L	L	H	H
L	H	H	L
H	L	L	H
H	H	No Change	

L = LOW Logic Level
H = HIGH Logic Level

ELECTRICAL CHARACTERISTICS 9024XC (T_A = 0°C to 75°C, V_{CC} = 5 V ±5%) (Note 3)

SYMBOL	PARAMETER	LIMITS 0°C MIN.	0°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	75°C MIN.	75°C MAX.	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage	1.9		1.8			1.6		Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs	
V_{IL}	Input LOW Voltage		0.85			0.85		0.85	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs	
V_{OH}	Output HIGH Voltage	2.4		2.4	3.0		2.4		Volts	V_{CC} = 4.75 V, I_{OH} = −1.2 mA	
V_{OL}	Output LOW Voltage		0.45		0.21	0.45		0.45	Volts	V_{CC} = 4.75 V, I_{OL} = 14.1 mA	
										V_{CC} = 5.25 V, I_{OL} = 16 mA	
I_{IH}	Input HIGH Current J, $\overline{K}$				5.0	60		60	μA	V_{CC} = 5.25 V, V_{IN} = 4.5 V GND on Other Inputs	
	Clock Input, S_D				10	120		120			
	$\overline{C}_D$				20	240		240			
I_{IL}	Input LOW Current J, $\overline{K}$		−1.6		−1.0	−1.6		−1.6	mA	V_{CC} = 5.25 V	V_{IN} = 0.45 V 4.5 V on Other Inputs
	Clock Input, S_D		−3.2		−2.0	−3.2		−3.2			
	$\overline{C}_D$ (Note 4)		−4.8		−3.0	−4.8		−4.8			
	J, $\overline{K}$		−1.41		−0.94	−1.41		−1.41	mA	V_{CC} = 4.75 V	
	Clock Input, S_D		−2.82		−1.88	−2.82		−2.82			
	$\overline{C}_D$ (Note 4)		−4.23		−2.82	−4.23		−4.23			
I_{SC}	Output HIGH Short Circuit Current	−30	−100	−30	−65	−100	−30	−100	mA	V_{CC} = 5.25 V, V_{OUT} = 0.0 V	
I_{CC}	Current Drain				9.0	14			mA	Per Flip-Flop in Worst Logic State	

ELECTRICAL CHARACTERISTICS 9024XM (T_A = −55°C to 125°C, V_{CC} = 5 V ±10%) (Note 3)

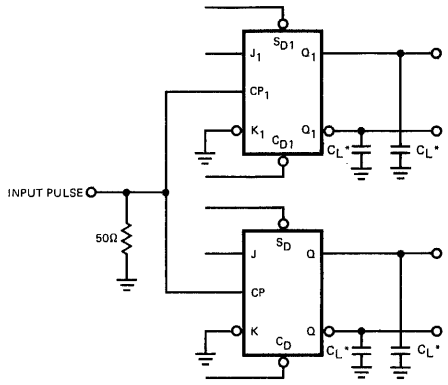
SYMBOL	PARAMETER	LIMITS −55°C MIN.	−55°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	125°C MIN.	125°C MAX.	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage	2.0		1.7			1.4		Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs	
V_{IL}	Input LOW Voltage		0.8			0.9		0.8	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs	
V_{OH}	Output HIGH Voltage	2.4		2.4	2.7		2.4		Volts	V_{CC} = 4.5 V, I_{OH} = −1.2 mA	
V_{OL}	Output LOW Voltage		0.4		0.2	0.4		0.4	Volts	V_{CC} = 4.5 V, I_{OL} = 12.4 mA	
			0.4		0.25	0.4		0.4	Volts	V_{CC} = 5.5 V, I_{OL} = 16 mA	
I_{IH}	Input HIGH Current J, $\overline{K}$				5.0	60		60	μA	V_{CC} = 5.5 V, V_{IN} = 4.5 V GND on Other Inputs	
	Clock Input, S_D				10	120		120			
	$\overline{C}_D$				20	240		240			
I_{IL}	Input LOW Current J, $\overline{K}$		−1.6		−1.1	−1.6		−1.6	mA	V_{CC} = 5.5 V	V_{IN} = 0.4 V 4.5 V on Other Inputs
	Clock Input, S_D		−3.2		−2.2	−3.2		−3.2			
	$\overline{C}_D$ (Note 4)		−4.8		−3.3	−4.8		−4.8			
	J, $\overline{K}$		−1.24		−0.91	−1.24		−1.24	mA	V_{CC} = 4.5 V	
	Clock Input, S_D		−2.48		−1.82	−2.48		−2.48			
	$\overline{C}_D$ (Note 4)		−3.72		−2.73	−3.72		−3.72			
I_{SC}	Output HIGH Short Circuit Current	−30	−100	−30	−65	−100	−30	−100	mA	V_{CC} = 5.5 V, V_{OUT} = 0.0 V	
I_{CC}	Current Drain				9.0	14			mA	Per Flip-Flop in Worst Logic State	

NOTES:
1. The maximum V_{CC} value of 8.0 V is not the primary factor in determining the maximum V_{CC} which may be applied to a number of interconnected devices. The voltage at a HIGH output is approximately 1 V_{BE} below the V_{CC} voltage, so the primary limit on the V_{CC} is that the voltage at any input may not go above 5.5 V unless the current is limited, so this effectively limits the system V_{CC} to approximately 7.0 V.
2. Because of the input clamp diodes, excess current can be drawn out of the inputs if the dc input voltage is more negative than −0.5 V. The diode is designed to clamp off large negative ac swings associated with fast fall times and long lines. This maximum rating is intended only to limit the steady state input voltage and current.
3. Postive current is into device and negative current is out of device.
4. Denotes maximum current under normal operation. These currents may increase up to 4 I_{IL} if J, $\overline{K}$ = HIGH and S_D = LOW.

SWITCHING CHARACTERISTICS (T_A = 25°C)

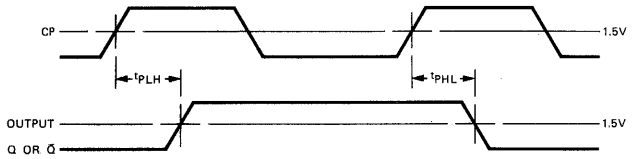
SYMBOL	PARAMETER	LIMITS MIN.	LIMITS 25°C TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS
t_{PLH}	Clock to Q or $\overline{Q}$		12	20	ns	
t_{PHL}	Clock to Q or $\overline{Q}$		22	33	ns	
$t_{release}$			2.0		ns	V_{CC} = 5.0 V
$t_{set\text{-}up}$		20	15	1.0	ns	C_L = 15 pF
t_{PLH}	S_D to Q, C_D to $\overline{Q}$		8.0	12	ns	Each Flip-Flop
t_{PHL}	S_D to $\overline{Q}$, C_D to Q		20	25	ns	
	Toggle Frequency	25	30		MHz	

SWITCHING TEST CIRCUIT

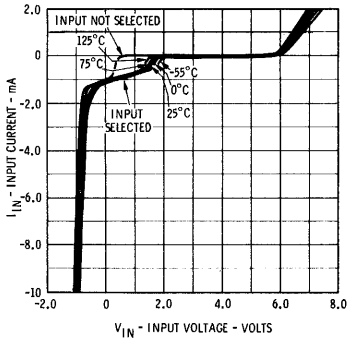


*C_L includes probe and jig capacitance

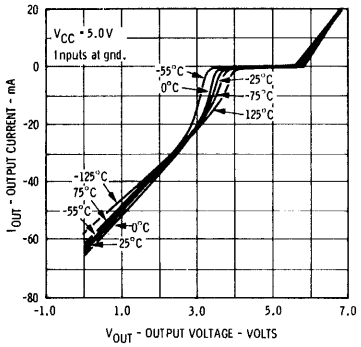
WAVEFORMS



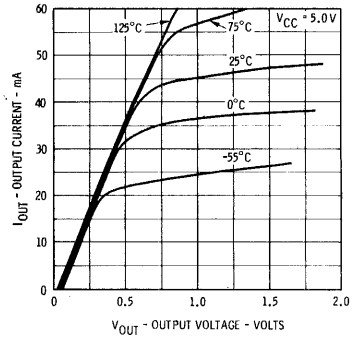
INPUT CURRENT VERSUS INPUT VOLTAGE



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)



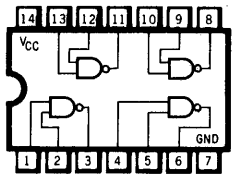
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)



QUAD 2-INPUT NAND GATE

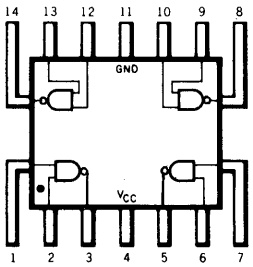
LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)

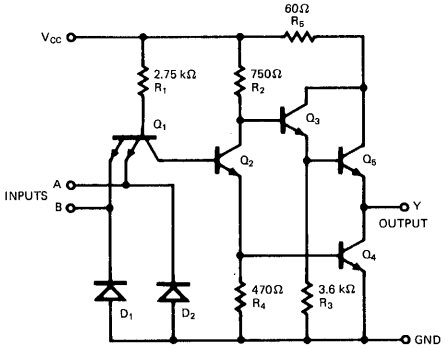


Positive logic: $Y = \overline{AB}$

FLATPAK (TOP VIEW)



SCHEMATIC DIAGRAM
(EACH GATE)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9H00XM/54H00XM			9H00XC/74H00XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	70	°C
Input Loading for Each Input			1.25			1.25	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage		1
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage		2
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = −0.5 mA, V_{IN} = 0.8 V		2
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 20 mA, V_{IN} = 2.0 V		1
I_{IH}	Input HIGH Current			50	μA	V_{CC} = MAX., V_{IN} = 2.4 V	Each Input	4
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current			−2.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V, Each Input		3
I_{OS}	Output Short Circuit Current (Note 3)	−40		−100	mA	V_{CC} = MAX.		5
I_{CCH}	Supply Current HIGH		10	16.8	mA	V_{CC} = MAX., V_{IN} = 0 V		6
I_{CCL}	Supply Current LOW		26	40	mA	V_{CC} = MAX., V_{IN} = 4.5 V		6

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		5.9	10	ns	V_{CC} = 5.0 V C_L = 25 pF R_L = 280Ω	T
t_{PHL}	Turn On Delay Input to Output		6.2	10	ns		

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

LPTTL/SSI 9L00

LOW POWER QUAD 2-INPUT NAND GATE

DESCRIPTION — The low power TTL/SSI 9L00 consists of four NAND gates. Each gate has two inputs and performs positive logic. The 9L00 is designed for low power and medium speed operation.

- **TYPICAL PROPAGATION DELAY OF 20 ns**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **ALL CERAMIC "HERMETIC" 14-LEAD DUAL IN-LINE AND FLAT PACKAGES**
- **TTL COMPATIBLE**

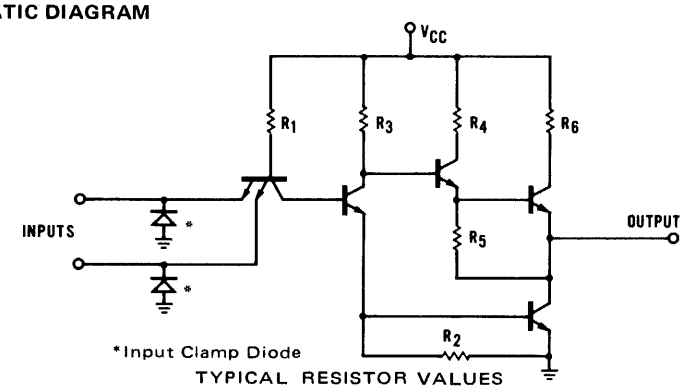
PIN NAMES

INPUTS (Pins 1, 2, 4, 5, 9, 10, 12, 13)
OUTPUTS (Pins 3, 6, 8, 11)

LOADING	
HIGH	LOW
0.5 U.L.	0.25 U.L.
10 U.L.	2.5 U.L.

1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.

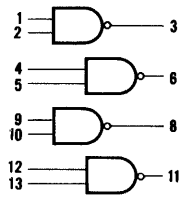
SCHEMATIC DIAGRAM



TYPICAL RESISTOR VALUES

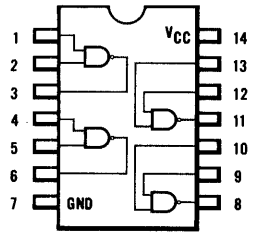
R_1 = 16 kΩ R_3 = 6 kΩ R_5 = 16 kΩ
R_2 = 5 kΩ R_4 = 600 Ω R_6 = 320 Ω

LOGIC SYMBOL

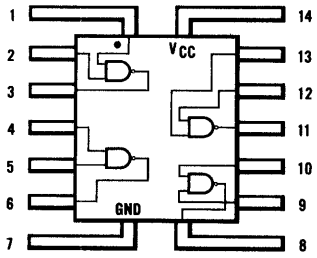


V_{CC} = PIN 14
GND = PIN 7

CONNECTION DIAGRAM
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
9L00XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9L00XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X=package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted) (See Notes 1, 2)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP. Note 3	LIMITS MAX.	UNITS	CONDITIONS	
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = −0.4 mA, V_{IN} = V_{IL}	
V_{OL}	Output LOW Voltage		0.1	0.3	Volts	V_{CC} = MIN., I_{OL} = 4.0 mA, V_{IN} = V_{IH}	
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed input LOW threshold voltage for all inputs	
V_{IL}	Input LOW Voltage			0.7	Volts	Guaranteed input HIGH threshold voltage for all inputs	
I_{IL}	Input LOW Current		−0.25	−0.4	mA	V_{CC} = MAX., V_{IN} = 0.3 V, Other Input = 4.5V	
I_{IH}	Input HIGH Current		2.0	20	μA	V_{CC} = MAX., V_{IN} = 2.4 V	Other Input = 0.0V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{SC} (Note 4)	Output Short Circuit Current	−10	−22	−40	mA	V_{CC} = MAX., V_{OUT} = 0.0 V, Inputs Grounded	
I_{CC}	Power Supply Current		0.9	1.56	mA	V_{CC} = MAX., Inputs HIGH	
	per Gate		0.28	0.41	mA	V_{CC} = MAX., Inputs LOW	

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, 25°C, and max. loading.
4. Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	CONDITIONS
t_{PLH}	Turn Off Delay Input to Output		15		ns	V_{CC} = 5.0V See Fig. 1
t_{PHL}	Turn On Delay Input to Output		25		ns	C_L = 15 pF

SWITCHING TIME WAVEFORMS

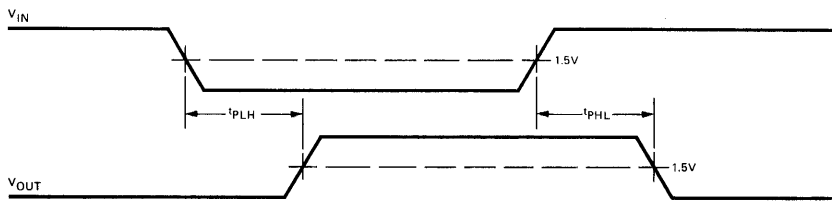
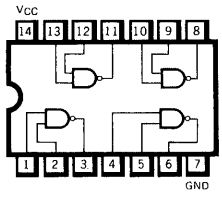


Fig. 1

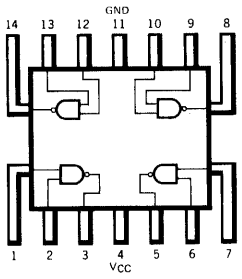
QUAD 2-INPUT NAND GATE

LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)

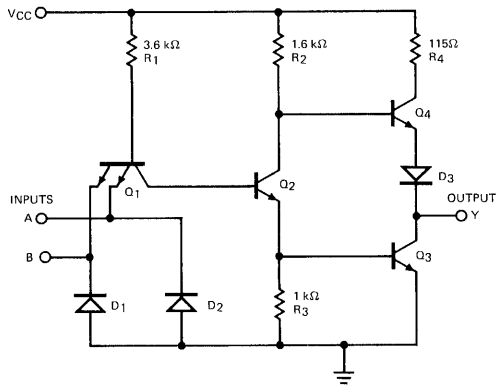


FLATPAK (TOP VIEW)



Positive logic: $Y = \overline{AB}$

SCHEMATIC DIAGRAM (EACH GATE)



Component values shown are typical

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9N00XM/5400XM			9N00XC/7400XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	70	°C
Normalized Fan-Out from Each Output, N			10			10	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage		1
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage		2
V_{OH}	Output HIGH Voltage	2.4	3.3		Volts	V_{CC} = MIN., I_{OH} = 0.4 mA, V_{IN} = 0.8 V		2
V_{OL}	Output LOW Voltage		0.22	0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA, V_{IN} = 2.0 V		1
I_{IH}	Input HIGH Current			40	μA	V_{CC} = MAX., V_{IN} = 2.4 V	Each Input	4
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current			−1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V,	Each Input	3
I_{OS}	Output Short Circuit Current (Note 3)	−20		−55	mA	9N00/5400	V_{CC} = MAX.	5
		−18		−55	mA	9N00/7400		
I_{CCH}	Supply Current HIGH		4.0	8.0	mA	V_{CC} = MAX., V_{IN} = 0V		6
I_{CCL}	Supply Current LOW		12	22	mA	V_{CC} = MAX., V_{IN} = 5.0 V		6

SWITCHING CHARACTERISTICS (T_A = 25°C)

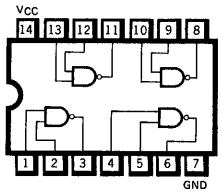
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		11	22	ns	V_{CC} = 5.0 V C_L = 15 pF R_L = 400Ω	A
t_{PHL}	Turn On Delay Input to Output		7.0	15	ns		

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Note more than one output should be shorted at a time.

QUAD 2-INPUT NAND GATE

LOGIC AND CONNECTION DIAGRAM

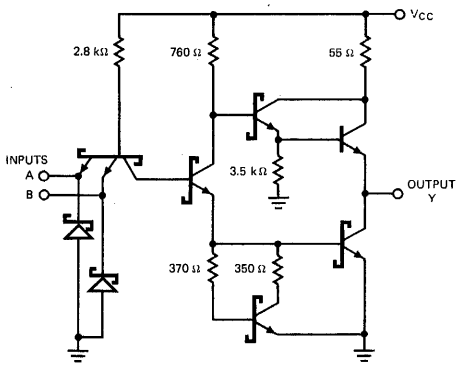
DIP (TOP VIEW)



Positive logic: $Y = \overline{AB}$

SCHEMATIC DIAGRAM

(EACH GATE)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9S00XM/54S00XM			9S00XC/74S00XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	75	°C
Input Loading for Each Input			1.25			1.25	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER		LIMITS MIN.	LIMITS TYP. (Note 2)	LIMITS MAX.	UNITS	TEST CONDITIONS (Note 1)	
V_{IH}	Input HIGH Voltage		2.0			Volts	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	Volts	Guaranteed Input LOW Voltage	
V_{CD}	Input Clamp Diode Voltage			-0.65	-1.2	Volts	V_{CC} = MIN., I_{IN} = -18mA	
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		Volts	V_{CC} = MIN., I_{OH} = -1.0mA, V_{IN} = 0.8V	
		XC	2.7	3.4				
V_{OL}	Output LOW Voltage			0.35	0.5	Volts	V_{CC} = MIN., I_{OL} = 20mA, V_{IN} = 2.0V	
I_{IH}	Input HIGH Current			1.0	50	μA	V_{CC} = MAX., V_{IN} = 2.7V	Each Input
					1.0	mA	V_{CC} = MAX., V_{IN} = 5.5V	
I_{IL}	Input LOW Current			-1.4	-2.0	mA	V_{CC} = MAX., V_{IN} = 0.5 V	Each Input
I_{OS}	Output Short Circuit Current (Note 3)		-40	-65	-100	mA	V_{CC} = MAX., V_{OUT} = 0V	
I_{CCH}	Supply Current HIGH			10.8	16.0	mA	V_{CC} = MAX., V_{IN} = 0V	
I_{CCL}	Supply Current LOW			25.2	36.0	mA	V_{CC} = MAX., Inputs Open	

SWITCHING CHARACTERISTICS (T_A = 25°C)

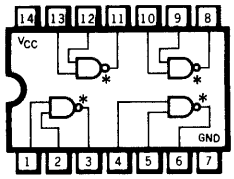
SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS	TEST FIGURES
t_{PLH}	Turn Off Delay Input to Output	2.0	3.0	4.5	ns	V_{CC} = 5.0V	DD
t_{PHL}	Turn On Delay Input to Output	2.0	3.0	5.0	ns	C_L = 15pF	

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0V, 25°C.
(3) Not more than one output should be shorted at a time.

QUAD 2-INPUT NAND GATE (WITH OPEN-COLLECTOR OUTPUT)

LOGIC AND CONNECTION DIAGRAM

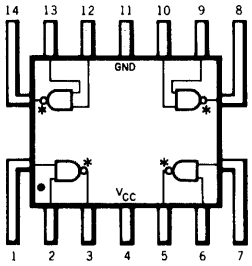
DIP (TOP VIEW)



*Open collector

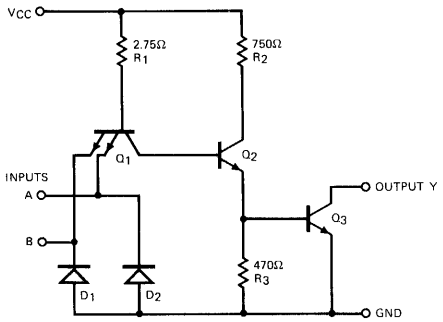
Positive logic: $Y = \overline{AB}$

FLATPAK (Top View)



*Open collector

SCHEMATIC DIAGRAM (EACH GATE)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9H01XM/54H01XM			9H01XC/74H01XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	70	°C
Input Loading for Each Input			1.25			1.25	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP. (Note 2)	LIMITS MAX.	UNITS	TEST CONDITIONS (Note 1)	TEST FIGURE
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage	1
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage	7
I_{OH}	Output HIGH Current			0.25	mA	V_{CC} = MIN., V_{OH} = 5.5 V, V_{IN} = 0.8 V	7
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 20 mA, V_{IN} = 2.0 V	1
I_{IH}	Input HIGH Current			50	μA	V_{CC} = MAX., V_{IN} = 2.4 V, Each Input	4
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V, Each Input	
I_{IL}	Input LOW Current			−2.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V, Each Input	3
I_{CCH}	Supply Current HIGH		6.8	10	mA	V_{CC} = MAX., V_{IN} = 0 V	6
I_{CCL}	Supply Current LOW		26	40	mA	V_{CC} = MAX., V_{IN} = 4.5 V	6

SWITCHING CHARACTERISTICS (T_A = 25°C)

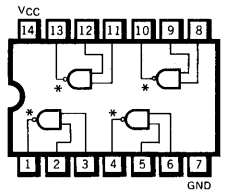
SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS	TEST FIGURE
t_{PLH}	Turn Off Delay Input to Output		10	15	ns	V_{CC} = 5.0 V, C_L = 25 pF, R_L = 280Ω	T
t_{PHL}	Turn On Delay Input to Output		7.5	12	ns		

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.

QUAD 2-INPUT NAND GATE
(WITH OPEN-COLLECTOR OUTPUT)

LOGIC AND CONNECTION DIAGRAM

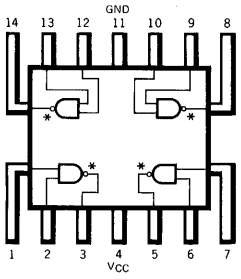
DIP (TOP VIEW)



*OPEN COLLECTOR

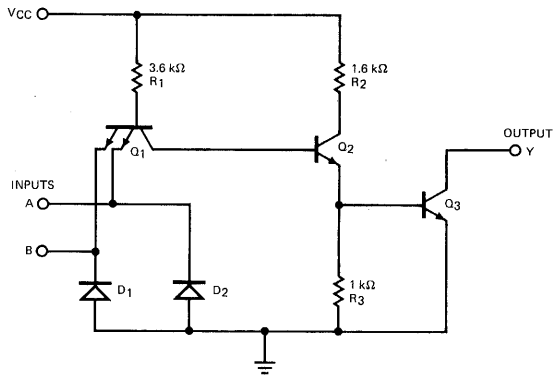
Positive logic: $Y = \overline{AB}$

FLATPAK (TOP VIEW)



*OPEN COLLECTOR

SCHEMATIC DIAGRAM
(EACH GATE)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9N01XM/5401XM			9N01XC/7401XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	70	°C
Normalized Fan-Out from Each Output, N			10			10	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage		1
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage		7
I_{OH}	Output HIGH Current			0.25	mA	V_{CC} = MIN., V_{OH} = 5.5 V, V_{IL} = 0.8 V		7
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA, V_{IN} = 2.0 V (On Level)		1
I_{IH}	Input HIGH Current			40	μA	V_{CC} = MAX., V_{IN} = 2.4 V	Each Input	4
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current			–1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V,	Each Input	3
I_{CCH}	Supply Current HIGH		4.0	8.0	mA	V_{CC} = MAX., V_{IN} = 0 V		6
I_{CCL}	Supply Current LOW		12	22	mA	V_{CC} = MAX., V_{IN} = 5.0 V		6

SWITCHING CHARACTERISTICS (T_A = 25°C)

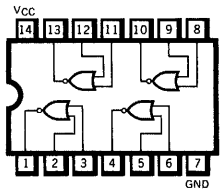
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS		TEST FIGURE
		MIN.	TYP.	MAX.				
t_{PLH}	Turn Off Delay Input to Output		35	45	ns	R_L = 4.0 kΩ	V_{CC} = 5.0 V, C_L = 15 pF	A
t_{PHL}	Turn On Delay Input to Output		8.0	15	ns	R_L = 400Ω		

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.

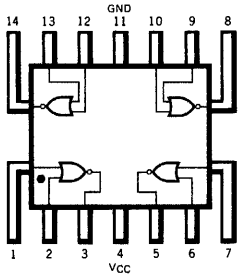
QUAD 2-INPUT NOR GATE

LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)

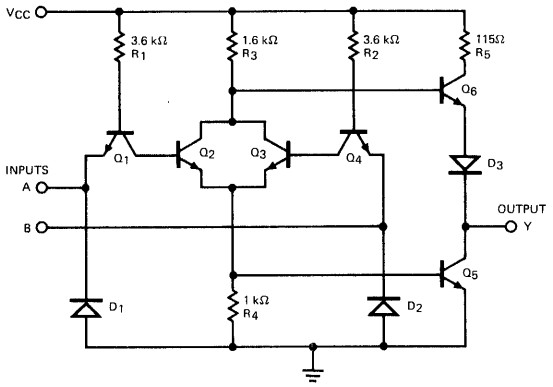


FLATPAK (TOP VIEW)



Positive logic: $Y = \overline{A+B}$

SCHEMATIC DIAGRAM (EACH GATE)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9N02XM/5402XM			9N02XC/7402XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	70	°C
Normalized Fan-Out from Each Output, N			10			10	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage		8
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage		9
V_{OH}	Output HIGH Voltage	2.4	3.3		Volts	V_{CC} = MIN., I_{OH} = −0.4 mA, V_{IN} = 0.8 V		9
V_{OL}	Output LOW Voltage		0.22	0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA, V_{IN} = 2.0 V		10
I_{IH}	Input HIGH Current			40	µA	V_{CC} = MAX., V_{IN} = 2.4 V	Each Input	12
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current			−1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V, Each Input		11
I_{OS}	Output Short Circuit Current (Note 3)	−20		−55	mA	9N02/5402	V_{CC} = MAX.	13
		18		−55	mA	9N02/7402		
I_{CCH}	Supply Current HIGH		8.0	16	mA	V_{CC} = MAX., V_{IN} = 0 V		14
I_{CCL}	Supply Current LOW		14	27	mA	V_{CC} = MAX., V_{IN} = 5.0 V		14

SWITCHING CHARACTERISTICS (T_A = 25°C)

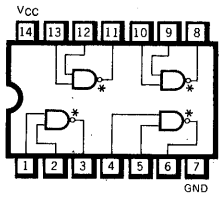
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		12	22	ns	V_{CC} = 5.0 V C_L = 15 pF R_L = 400Ω	A
t_{PHL}	Turn On Delay Input to Output		8.0	15	ns		

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.

QUAD 2-INPUT NAND GATE
(WITH OPEN-COLLECTOR OUTPUT)

LOGIC AND CONNECTION DIAGRAM

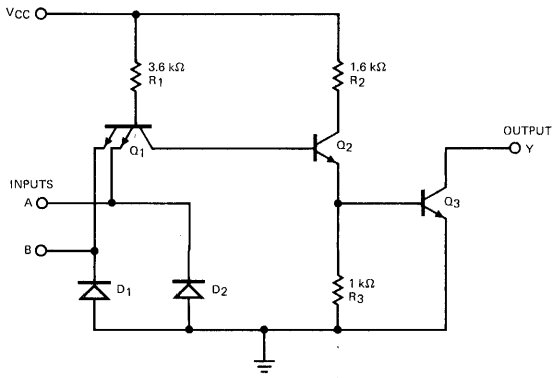
DIP (TOP VIEW)



*OPEN COLLECTOR

Positive logic: $Y = \overline{AB}$

SCHEMATIC DIAGRAM
(EACH GATE)



Component values shown are typical.

5

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9N03XM/5403XM			9N03XC/7403XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	70	°C
Normalized Fan-Out from Each Output, N			10			10	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP. (Note 2)	LIMITS MAX.	UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage		1
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage		7
I_{OH}	Output HIGH Current			0.25	mA	V_{CC} = MIN., V_{OH} = 5.5 V, V_{IN} = 0.8 V		7
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA, V_{IN} = 2.0 V (On Level)		1
I_{IH}	Input HIGH Current			40	μA	V_{CC} = MAX., V_{IN} = 2.4 V	Each Input	4
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current			–1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V,	Each Input	3
I_{CCH}	Supply Current HIGH		4.0	8.0	mA	V_{CC} = MAX., V_{IN} = 0V		6
I_{CCL}	Supply Current LOW		12	22	mA	V_{CC} = MAX., V_{IN} = 5.0 V		6

SWITCHING CHARACTERISTICS (T_A = 25°C)

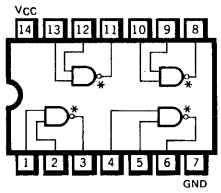
SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS		TEST FIGURE
t_{PLH}	Turn Off Delay Input to Output		35	45	ns	R_L = 4.0 kΩ	V_{CC} = 5.0 V	A
t_{PHL}	Turn On Delay Input to Output		8.0	15	ns	R_L = 400Ω	C_L = 15 pF	

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.

QUAD 2-INPUT NAND GATE
(WITH OPEN-COLLECTOR OUTPUT)

LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)

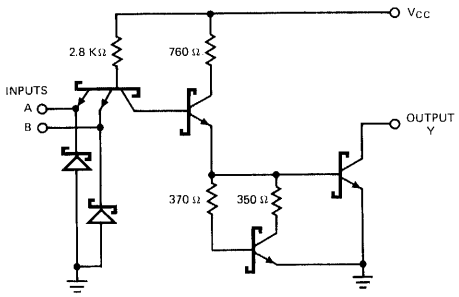


* OPEN COLLECTOR

Positive logic: $Y = \overline{AB}$

SCHEMATIC DIAGRAM

(EACH GATE)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	† 9S03XM/54S03XM			9S03XC/74S03XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	75	°C
Input Loading for Each Input			1.25			1.25	U.L.

X= package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage	
V_{CD}	Input Clamp Diode Voltage		–0.65	–1.2	Volts	V_{CC} = MIN., I_{IN} = -18mA	
I_{OH}	Output HIGH Current		0.1	250	μA	V_{CC} = MIN., V_{OH} = 5.5V, V_{IN} = 0.8V	
V_{OL}	Output LOW Voltage		0.35	0.5	Volts	V_{CC} = MIN., I_{OL} = 20mA, V_{IN} = 2.0V	
I_{IH}	Input HIGH Current		1.0	50	μA	V_{CC} = MAX., V_{IN} = 2.7V	Each Input
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5V	
I_{IL}	Input LOW Current		–1.4	–2.0	mA	V_{CC} = MAX., V_{IN} = 0.5 V	Each Input
I_{CCH}	Supply Current HIGH		6.0	13.2	mA	V_{CC} = MAX., V_{IN} = 0V	
I_{CCL}	Supply Current LOW		25.2	36.0	mA	V_{CC} = MAX., Inputs Open	

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURES
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output	2.0	5.0	7.5	ns	V_{CC} = 5.0V	EE
t_{PHL}	Turn On Delay Input to Output	2.0	4.5	7.0	ns	C_L = 15pF	

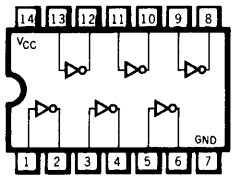
NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0V, 25°C.

† To be announced 1972

HEX INVERTER

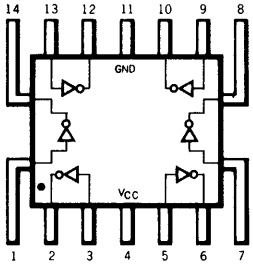
LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)

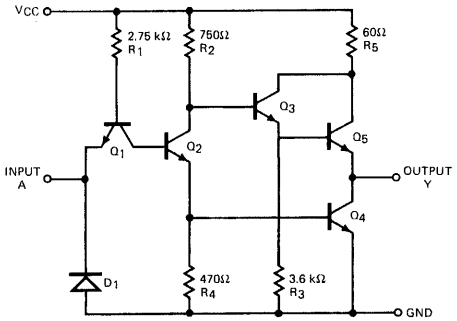


Positive logic: $Y = \overline{A}$

FLATPAK (TOP VIEW)



SCHEMATIC DIAGRAM (EACH INVERTER)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9H04XM/54H04XM			9H04XC/74H04XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	70	°C
Input Loading for Each Input			1.25			1.25	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage	15
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage	16
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = −0.5 mA, V_{IN} = 0.8 V	16
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 20 mA, V_{IN} = 2.0V	15
I_{IH}	Input HIGH Current			50	μA	V_{CC} = MAX., V_{IN} = 2.4 V	18
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IL}	Input LOW Current			−2.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V,	18
I_{OS}	Output Short Circuit Current (Note 3)	−40		−100	mA	V_{CC} = MAX.	19
I_{CCH}	Supply Current HIGH		16	26	mA	V_{CC} = MAX., V_{IN} = 0 V	20
I_{CCL}	Supply Current LOW		40	58	mA	V_{CC} = MAX., V_{IN} = 4.5 V	20

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		6.5	10	ns	V_{CC} = 5.0V C_L = 25 pF R_L = 280Ω	T
t_{PHL}	Turn On Delay Input to Output		9.0	13	ns		

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

LPTTL/SSI 9L04
LOW POWER HEX INVERTER

DESCRIPTION — The low power TTL/SSI 9L04 consists of six TTL gates, each performing a single inversion function. Designed for low power, medium speed operation, the 9L04 is very useful where a number of complement signals are desired simultaneously.

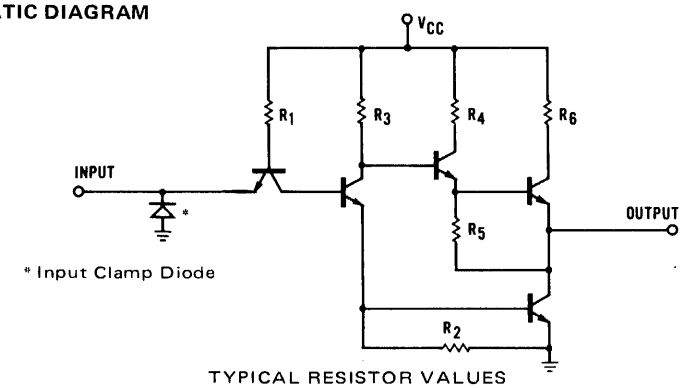
- **TYPICAL PROPAGATION DELAY OF 20 ns**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **ALL CERAMIC "HERMETIC" 14-LEAD DUAL IN-LINE AND FLAT PACKAGES**
- **TTL COMPATIBLE**

PIN NAMES

	LOADING	
	HIGH	LOW
INPUTS (Pins 1, 3, 5, 9, 11, 13)	0.5 U.L.	0.25 U.L.
OUTPUTS (Pins 2, 4, 6, 8, 10, 12)	10 U.L.	2.5 U.L.

1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.

SCHEMATIC DIAGRAM

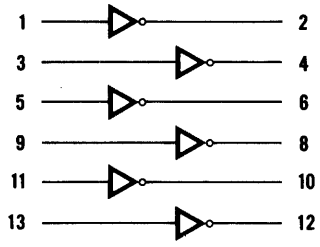


* Input Clamp Diode

TYPICAL RESISTOR VALUES

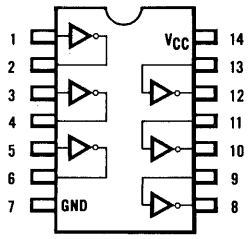
R_1 = 16 kΩ R_3 = 6 kΩ R_5 = 16 kΩ
R_2 = 5 kΩ R_4 = 600 Ω R_6 = 320 Ω

LOGIC SYMBOL

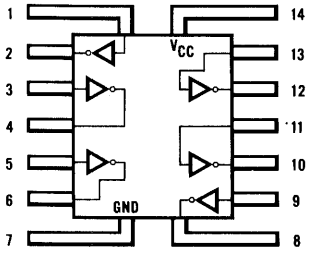


V_{CC} = Pin 14
GND = Pin 7

CONNECTION DIAGRAMS
DIP (Top View)



FLATPAK (Top View)



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
9L04XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9L04XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (UNLESS OTHERWISE NOTED) (See Notes 1 & 2)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP. Note 3	MAX.		
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = −0.4 mA, V_{IN} = V_{IL}
V_{OL}	Output LOW Voltage		0.1	0.3	Volts	V_{CC} = MIN., I_{OL} = 4.0 mA, V_{IN} = V_{IH}
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed input logical HIGH voltage for all inputs
V_{IL}	Input LOW Voltage			0.7	Volts	Guaranteed input logical LOW voltage for all inputs
I_{IL}	Input LOW Current		−0.25	−0.4	mA	V_{CC} = MAX., V_{IN} = 0.3 V
I_{IH}	Input HIGH Current		2.0	20	μA	V_{CC} = MAX., V_{IN} = 2.4 V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{SC} (Note 4)	Output Short Circuit Current	−10	−22	−40	mA	V_{CC} = MAX., V_{OUT} = 0.00 V, Inputs grounded
I_{CC}	Power Supply Current		0.9	1.56	mA	V_{CC} = MAX., Input HIGH
	per Gate		0.28	0.45	mA	V_{CC} = MAX., Input LOW

NOTES: 1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, 25°C, and max. loading.
4. Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP.	MAX.		
t_{PLH}	Turn Off Delay Input to Output		15		ns	V_{CC} = 5.0V See Fig. 1
t_{PHL}	Turn On Delay Input to Output		25		ns	C_L = 15 pF

SWITCHING TIME WAVEFORM

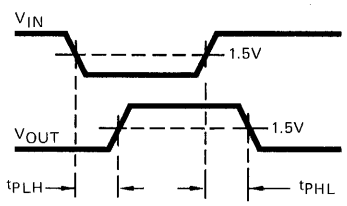
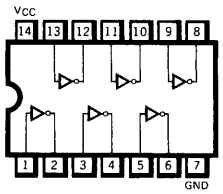


Fig. 1

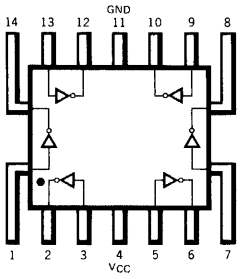
HEX INVERTER

LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)

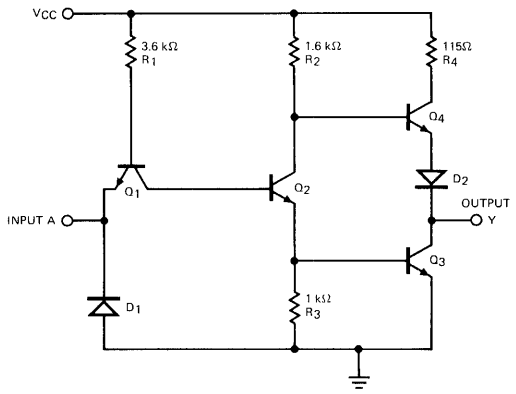


FLATPAK (TOP VIEW)



Positive logic: $Y = \overline{A}$

SCHEMATIC DIAGRAM (EACH INVERTER)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9N04XM/5404XM			9N04XC/7404XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	70	°C
Normalized Fan-Out from Each Output, N			10			10	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage		15
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage		16
V_{OH}	Output HIGH Voltage	2.4	3.3		Volts	V_{CC} = MIN., I_{OH} = −0.4 mA, V_{IN} = 0.8 V		16
V_{OL}	Output LOW Voltage		0.22	0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA, V_{IN} = 2.0 V		15
I_{IH}	Input HIGH Current			40	μA	V_{CC} = MAX., V_{IN} = 2.4 V		18
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current			−1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V		18
I_{OS}	Output Short Circuit Current (Note 3)	−20		−55	mA	9N04/5404	V_{CC} = MAX.	19
		−18		−55	mA	9N04/7404		
I_{CCH}	Supply Current HIGH		6.0	12	mA	V_{CC} = MAX., V_{IN} = 0 V		20
I_{CCL}	Supply Current LOW		18	33	mA	V_{CC} = MAX., V_{IN} = 5.0 V		20

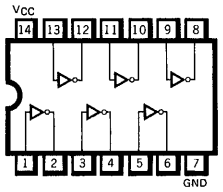
SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		12	22	ns	V_{CC} = 5.0 V C_L = 15 pF R_L = 400Ω	A
t_{PHL}	Turn On Delay Input to Output		8.0	15	ns		

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.

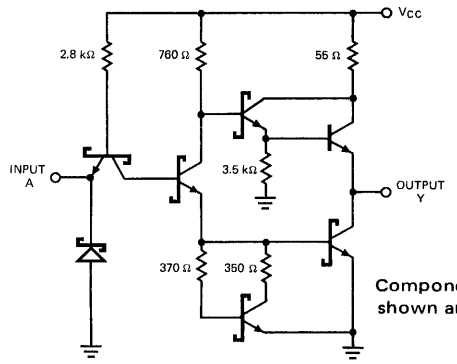
HEX INVERTER

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



Positive logic: $Y = \overline{A}$

SCHEMATIC DIAGRAM
(EACH INVERTER)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9S04XM/54S04XM 9S04AXM			9S04XC/74S04XC 9S04AXC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	75	°C
Input Loading for Each Input			1.25			1.25	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER		LIMITS MIN.	LIMITS TYP. (Note 2)	LIMITS MAX.	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			Volts	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage				0.8	Volts	Guaranteed Input LOW Voltage
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.2	Volts	V_{CC} = MIN., I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		Volts	V_{CC} = MIN., I_{OH} = −1.0 mA, V_{IN} = 0.8 V
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage			0.35	0.5	Volts	V_{CC} = MIN., I_{OL} = 20 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	50	μA	V_{CC} = MAX., V_{IN} = 2.7 V
					1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{IL}	Input LOW Current			−1.4	−2.0	mA	V_{CC} = MAX., V_{IN} = 0.5 V
I_{OS}	Output Short Circuit Current (Note 3)		−40	−65	−100	mA	V_{CC} = MAX., V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			16.2	24.0	mA	V_{CC} = MAX., V_{IN} = 0 V
I_{CCL}	Supply Current LOW			37.8	54.0	mA	V_{CC} = MAX., Inputs Open

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS	TEST FIGURES
t_{PLH}	Turn Off Delay Input to Output	9S04	2.0	3.0	4.5	ns	V_{CC} = 5.0 V	DD
		9S04A	1.0	2.5	3.5			
t_{PHL}	Turn On Delay Input to Output	9S04	2.0	3.0	5.0	ns	C_L = 15 pF	
		9S04A	1.0	2.5	4.0			

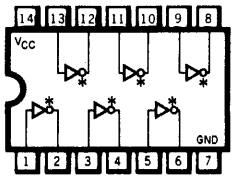
NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.

5

HEX INVERTER (WITH OPEN-COLLECTOR OUTPUT)

LOGIC AND CONNECTION DIAGRAM

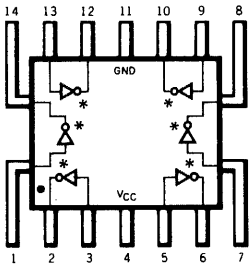
DIP (TOP VIEW)



*OPEN COLLECTOR

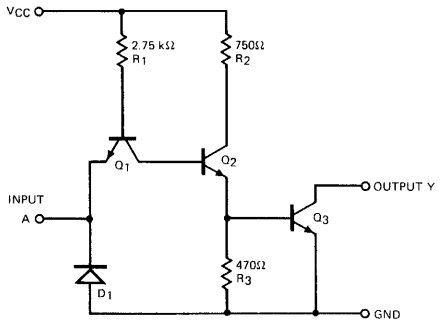
Positive logic: $Y = \overline{A}$

FLATPAK (TOP VIEW)



*OPEN COLLECTOR

SCHEMATIC DIAGRAM (EACH INVERTER)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9H05XM/54H05XM			9H05XC/74H05XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	70	°C
Input Loading for Each Input			1.25			1.25	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage	15
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage	17
I_{OH}	Output HIGH Current			0.25	mA	V_{CC} = MIN., V_{OH} = 5.5 V, V_{IN} = 0.8 V	17
V_{OL}	Output LOW Voltage (On Level)			0.4	Volts	V_{CC} = MIN., I_{OL} = 20 mA, V_{IN} = 2.0 V	15
I_{IH}	Input HIGH Current			50	μA	V_{CC} = MAX., V_{IN} = 2.4 V	18
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IL}	Input LOW Current			−2.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V	18
I_{CCH}	Supply Current HIGH		16	26	mA	V_{CC} = MAX., V_{IN} = 0 V	20
I_{CCL}	Supply Current LOW		40	58	mA	V_{CC} = MAX., V_{IN} = 4.5 V	20

SWITCHING CHARACTERISTICS (T_A = 25°C)

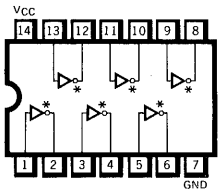
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		13	18	ns	V_{CC} = 5.0 V C_L = 25 pF R_L = 280Ω	T
t_{PHL}	Turn On Delay Input to Output		10	15	ns		

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.

HEX INVERTER
(WITH OPEN-COLLECTOR OUTPUT)

LOGIC AND CONNECTION DIAGRAM

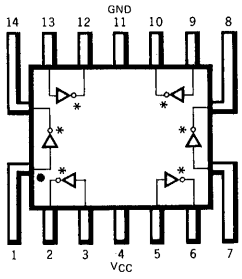
DIP (TOP VIEW)



*OPEN COLLECTOR

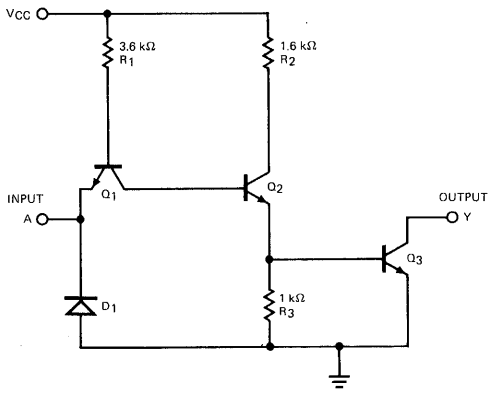
Positive logic: $Y = \overline{A}$

FLATPAK (TOP VIEW)



*OPEN COLLECTOR

SCHEMATIC DIAGRAM
(EACH INVERTER)



Component values shown are typical.

5

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9N05XM/5405XM			9N05XC/7405XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	70	°C
Normalized Fan-Out from Each Output, N			10			10	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage		15
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage		17
I_{OH}	Output HIGH Current			0.25	mA	V_{CC} = MIN., V_{OH} = 5.5 V, V_{IN} = 0.8 V		17
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA, V_{IN} = 2.0 V (On Level)		15
I_{IH}	Input HIGH Current			40	μA	V_{CC} = MAX., V_{IN} = 2.4 V		18
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current			−1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V		18
I_{CCH}	Supply Current HIGH		6	12	mA	V_{IN} = 0 V	V_{CC} = 5.0 V, T_A = 25°C	20
I_{CCL}	Supply Current LOW		18	33	mA	V_{IN} = 5 V		20

SWITCHING CHARACTERISTICS (T_A = 25°)

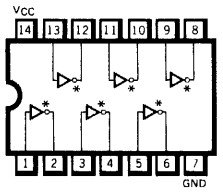
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS		TEST FIGURE
		MIN.	TYP.	MAX.				
t_{PLH}	Turn Off Delay Input to Output		40	55	ns	R_L = 4kΩ	V_{CC} = 5.0 V	A
t_{PHL}	Turn On Delay Input to Output		8.0	15	ns	R_L = 400Ω	C_L = 15 pF	

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.

HEX INVERTER
(WITH OPEN-COLLECTOR OUTPUT)

LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)

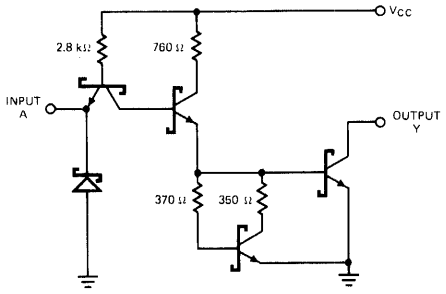


* OPEN COLLECTOR

Positive logic: $Y = \overline{A}$

SCHEMATIC DIAGRAM

(EACH INVERTER)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	† 9S05XM/54S05XM † 9S05AXM			9S05XC/74S05XC 9S05AXC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	75	°C
Input Loading for Each Input			1.25			1.25	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP. (Note 2)	LIMITS MAX.	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage
V_{CD}	Input Clamp Diode Voltage		−0.65	−1.2	Volts	V_{CC} = MIN., I_{IN} = -18mA
I_{OH}	Output HIGH Current		0.1	250	μA	V_{CC} = MIN., V_{OH} = 5.5V, V_{IN} = 0.8V
V_{OL}	Output LOW Voltage		0.35	0.5	Volts	V_{CC} = MIN., I_{OL} = 20mA, V_{IN} = 2.0V
I_{IH}	Input HIGH Current		1.0	50	μA	V_{CC} = MAX., V_{IN} = 2.7V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5V
I_{IL}	Input LOW Current		−1.4	−2.0	mA	V_{CC} = MAX., V_{IN} = 0.5 V
I_{CCH}	Supply Current HIGH		9.0	19.8	mA	V_{CC} = MAX., V_{IN} = 0V
I_{CCL}	Supply Current LOW		37.8	54.0	mA	V_{CC} = MAX., Inputs Open

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS	TEST FIGURES
t_{PLH}	Turn Off Delay Input to Output	9S05	2.0	5.0	7.5	ns	V_{CC} = 5.0V	EE
		9S05A	2.0	4.0	5.5			
t_{PHL}	Turn On Delay Input to Output	9S05	2.0	4.5	7.0	ns	C_L = 15pF	
		9S05A	1.5	3.4	5.0			

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0V, 25°C.

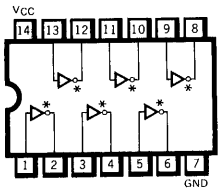
† To be announced 1972.

HEX INVERTER BUFFER/DRIVER
(WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUT)

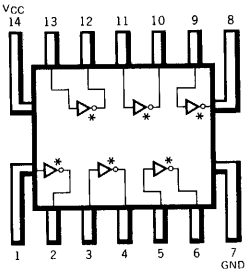
DESCRIPTION – These TTL/SSI hex inverter buffer/driver feature high voltage open collector output for interfacing with high level circuits (such as MOS), or for driving high current loads (such as lamps or relays) and are also characterized for use as inverter buffers for driving TTL inputs. For increased fan out, several inverters in a single package may be paralleled. The 9N06/5406, 7406 have minimum breakdown voltages of 30V and the 9N16/5416, 7416 have minimum breakdown voltages of 15V. The maximum sink current is 30 mA for the 9N06/5406 and 9N16/5416 and 40 mA for the 9N06/7406 and 9N16/7416.

LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)



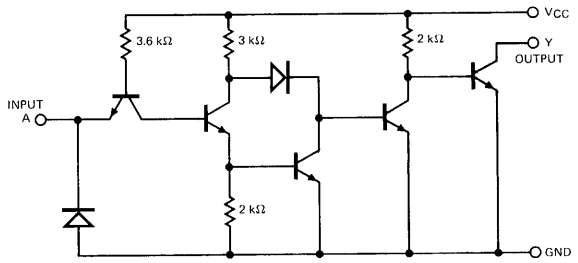
FLATPAK (TOP VIEW)



*OPEN COLLECTOR

Positive logic = $Y = \overline{A}$

SCHEMATIC DIAGRAM
(EACH INVERTER)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		9N06XM/5406XM 9N16XM/5416XM			9N06XC/7406XC 9N16XC/7416XC			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	Volts
Operating Free-Air Temperature Range		–55	25	125	0	25	70	°C
Output HIGH Voltage, V_{OH}	9N06/5406, 7406			30			30	Volts
	9N16/5416, 7416			15			15	
Output LOW Current, I_{OL}				30			40	mA

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP. (Note 2)	LIMITS MAX.	UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage		65
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage		66
I_{OH}	Output HIGH Current			0.25	mA	V_{CC} = MIN., V_{OH} = MAX., V_{IN} = 0.8 V		66
V_{OL}	Output LOW Voltage			0.7	Volts	I_{OL} = MAX.	V_{CC} = MIN., V_{IN} = 2.0 V	65
				0.4	Volts	I_{OL} = 16 mA		
I_{IH}	Input HIGH Current			40	μA	V_{CC} = MAX., V_{IN} = 2.4 V	Each Input	67
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current			–1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V,	Each Input	68
I_{CCH}	Supply Current HIGH		30	42	mA	V_{CC} = MAX., V_{IN} = 0V		69
I_{CCL}	Supply Current LOW		27	38	mA	V_{CC} = MAX., V_{IN} = 5.0 V		69

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS	TEST FIGURE
t_{PLH}	Turn Off Delay Input to Output		10	15 *	ns	V_{CC} = 5.0 V, C_L = 15 pF, R_L = 110Ω	J
t_{PHL}	Turn On Delay Input to Output		15	23	ns		

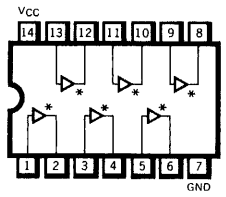
NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
* Max. 17 ns at 125°C

HEX BUFFER/DRIVER
(WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUT)

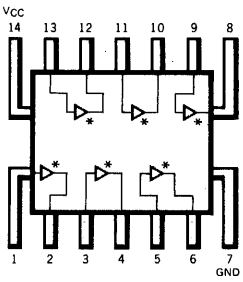
DESCRIPTION – These TTL/SSI hex buffer/driver feature high voltage open collector output for interfacing with high level circuits (such as MOS), or for driving high current loads (such as lamps or relays) and are also characterized for use as buffers for driving TTL inputs. For increased fan out, several buffers in a single package may be paralleled. The 9N07/5407, 7404 have minimum breakdown voltages of 30V and the 9N17/5417, 7417 have minimum breakdown voltages of 15V. The maximum sink current is 30 mA for the 9N07/5407 and 40 mA for the 9N07/7407 and 9N17/7417.

LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)



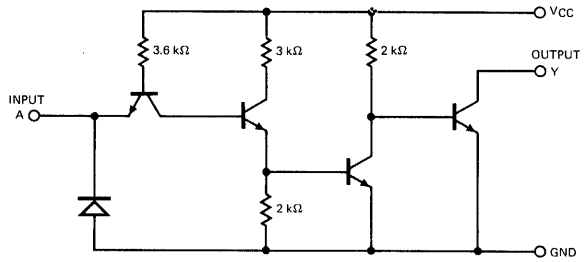
FLATPAK (TOP VIEW)



*OPEN COLLECTOR

Positive logic: Y = A

SCHEMATIC DIAGRAM
(EACH BUFFER/DRIVER)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		9N07XM/5407XM 9N17XM/5417XM			9N07XC/7407XC 9N17XC/7417XC			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	Volts
Operating Free-Air Temperature Range		-55	25	125	0	25	70	°C
Output HIGH Level Voltage, V_{OH}	9N07/5407, 7407			30			30	Volts
	9N17/5417, 7417			15			15	
Output LOW Level Current, I_{OL}				30			40	mA

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP. (Note 2)	LIMITS MAX.	UNITS	TEST CONDITIONS (Note 1)			TEST FIGURE
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage			70
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage			71
I_{OH}	Output HIGH Current			0.25	mA	V_{CC} = MIN., V_{OH} = MAX., V_{IN} = 2.0 V			70
V_{OL}	Output LOW Voltage			0.7	Volts	I_{OL} = MAX.	V_{CC} = MIN.		71
				0.4	Volts	I_{OL} = 16 mA	V_{IN} = 0.8 V		
I_{IH}	Input HIGH Current			40	μA	V_{CC} = MAX., V_{IN} = 2.4 V		Each Input	72
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		Each Input	
I_{IL}	Input LOW Current			-1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V,		Each Input	73
I_{CCH}	Supply Current HIGH		29	41	mA	V_{CC} = MAX., V_{IN} = 5 V			74
I_{CCL}	Supply Current LOW		21	30	mA	V_{CC} = MAX., V_{IN} = 0V			74

SWITCHING CHARACTERISTICS (T_A = 25°C)

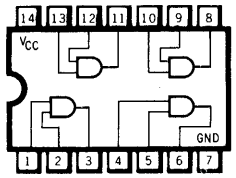
SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS	TEST FIGURE
t_{PLH}	Turn Off Delay Input to Output		6.0	10	ns	V_{CC} = 5.0 V, C_L = 15 pF, R_L = 110Ω	K
t_{PHL}	Turn On Delay Input to Output		20	30	ns		

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.

QUAD 2-INPUT AND GATE

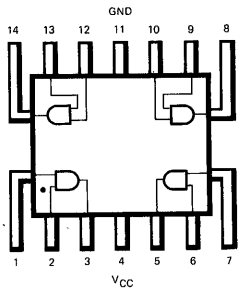
LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)

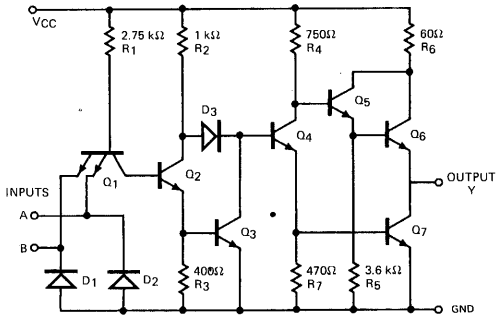


Positive logic: Y = AB

FLATPAK (TOP VIEW)



SCHEMATIC DIAGRAM (EACH GATE)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9H08XM/5408XM			9H08XC/74H08XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	70	°C
Input Loading for Each Input			1.25			1.25	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage	75
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage	77
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = −0.5 mA, V_{IN} = 2.0V	75
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 20 mA, V_{IN} = 0.8 V	77
I_{IH}	Input HIGH Current			50	μA	V_{CC} = MAX., V_{IN} = 2.4 V, Each Input	78
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V, Each Input	
I_{IL}	Input LOW Current			−2.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V, Each Input	79
I_{OS}	Output Short Circuit Current (Note 3)	−40		−100	mA	V_{CC} = MAX. V_{IN} = 4.5 V	80
I_{CCH}	Supply Current HIGH		24	40	mA	V_{CC} = MAX., V_{IN} = 4.5 V	81
I_{CCL}	Supply Current LOW		40	64	mA	V_{CC} = MAX., V_{IN} = 0 V	81

SWITCHING CHARACTERISTICS (T_A = 25°C)

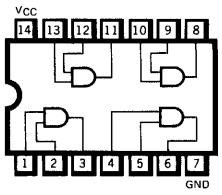
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		7.6	12	ns	V_{CC} = 5.0V, C_L = 25 pF, R_L = 280Ω	T
t_{PHL}	Turn On Delay Input to Output		8.8	12	ns		

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

QUAD 2-INPUT AND GATE

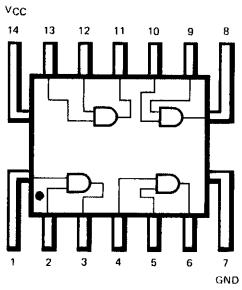
LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)

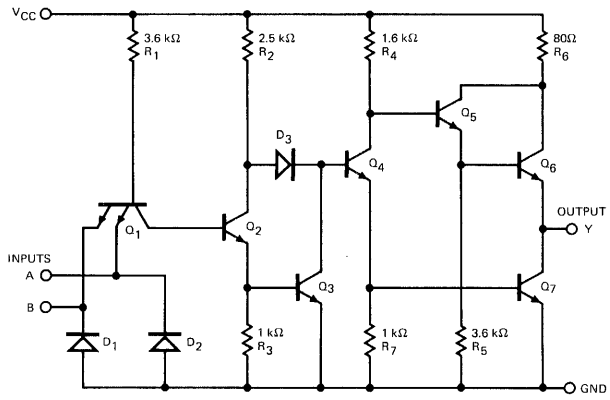


Positive logic: Y = AB

FLATPAK (TOP VIEW)



SCHEMATIC DIAGRAM (EACH GATE)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9N08XM/5408XM			9N08XC/7408XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	70	°C
Normalized Fan Out from Each Output, N			10			10	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage		75
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage		77
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = −0.8 mA, V_{IH} = 2.0 V		75
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA, V_{IL} = 0.8 V		77
I_{IH}	Input HIGH Current			40	μA	V_{CC} = MAX., V_{IN} = 2.4 V	Each Input	78
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current			−1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V,	Each Input	79
I_{OS}	Output Short Circuit Current (Note 3)	−40		−100	mA	V_{CC} = MAX.		80
I_{CCH}	Supply Current HIGH			20	mA	V_{CC} = MAX., V_{IN} = 5 V		81
I_{CCL}	Supply Current LOW			32	mA	V_{CC} = MAX., V_{IN} = 0 V		81

SWITCHING CHARACTERISTICS (T_A = 25°C)

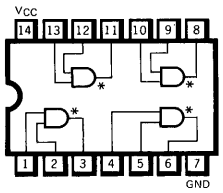
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		17.5	40	ns	V_{CC} = 5.0 V C_L = 15 pF R_L = 400Ω	L
t_{PHL}	Turn On Delay Input to Output		12	25	ns		

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C
(3) Not more than one output should be shorted at a time.

QUAD 2-INPUT AND GATE (WITH OPEN-COLLECTOR OUTPUT)

LOGIC AND CONNECTION DIAGRAM

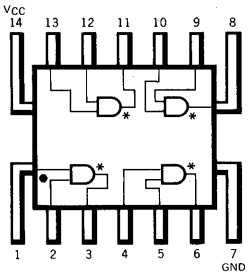
DIP (TOP VIEW)



*OPEN COLLECTOR

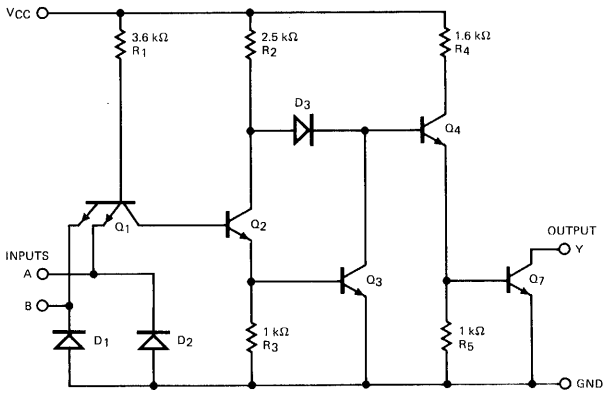
Positive logic: Y = AB

FLATPAK (TOP VIEW)



*OPEN COLLECTOR

SCHEMATIC DIAGRAM (EACH GATE)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9N09XM/5409XM			9N09XC/7409XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	70	°C
Normalized Fan-Out from Each Output, N			10			10	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage		76
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage		77
I_{OH}	Output HIGH Current			0.25	mA	V_{CC} = MIN., V_{IH} = 2.0 V, V_{OH} = 5.5 V		76
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA, V_{IL} = 0.8 V		77
I_{IH}	Input HIGH Current			40	μA	V_{CC} = MAX., V_{IN} = 2.4 V	Each Input	78
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current			−1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V;	Each Input	79
I_{CCH}	Supply Current HIGH		11	21	mA	V_{CC} = MAX., V_{IN} = 5.0 V		81
I_{CCL}	Supply Current LOW		20	33	mA	V_{CC} = MAX., V_{IN} = 0 V		81

SWITCHING CHARACTERISTICS (T_A = 25°C)

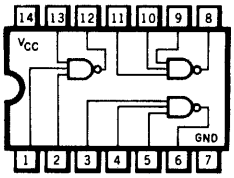
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		21	32	ns	V_{CC} = 5.0 V C_L = 15 pF R_L = 400Ω	L
t_{PHL}	Turn On Delay Input to Output		16	24	ns		

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.

TRIPLE 3-INPUT NAND GATE

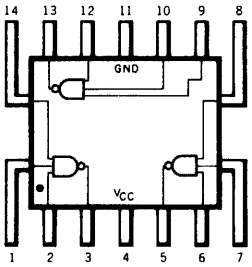
LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)

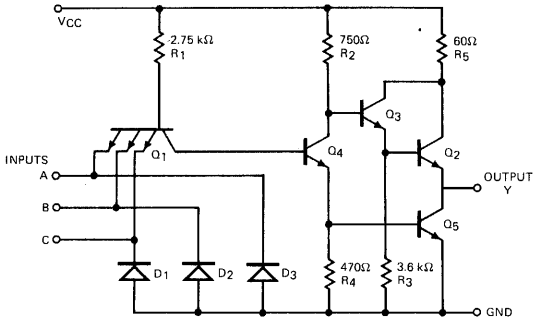


Positive logic: $Y = \overline{ABC}$

FLATPAK (TOP VIEW)



SCHEMATIC DIAGRAM (EACH GATE)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9H10XM/54H10XM			9H10XC/74H10XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	70	°C
Input Loading for Each Input			1.25			1.25	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage	1
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage	2
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = −0.5 mA, V_{IN} = 0.8 V	2
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 20 mA, V_{IN} = 2.0V	1
I_{IH}	Input HIGH Current			50	μA	V_{CC} = MAX., V_{IN} = 2.4 V, Each Input	4
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V, Each Input	
I_{IL}	Input LOW Current			−2.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V, Each Input	3
I_{OS}	Output Short Circuit Current (Note 3)	−40		−100	mA	V_{CC} = MAX.	5
I_{CCH}	Supply Current HIGH		7.5	12.6	mA	V_{CC} = MAX., V_{IN} = 0 V	6
I_{CCL}	Supply Current LOW		19.5	30	mA	V_{CC} = MAX., V_{IN} = 4.5 V	6

SWITCHING CHARACTERISTICS (T_A = 25°C)

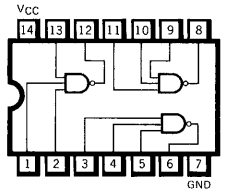
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		5.9	10	ns	V_{CC} = 5.0V, C_L = 25 pF, R_L = 280Ω	T
t_{PHL}	Turn On Delay Input to Output		6.3	10	ns		

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

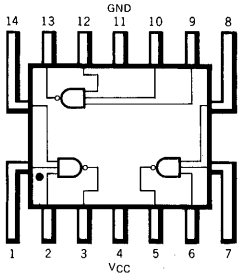
TRIPLE 3-INPUT NAND GATE

LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)

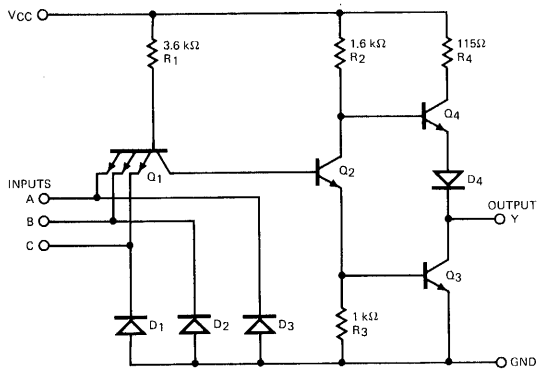


FLATPAK (TOP VIEW)



Positive logic: $Y = \overline{ABC}$

SCHEMATIC DIAGRAM (EACH GATE)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9N10XM/5410XM			9N10XC/7410XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	70	°C
Normalized Fan-Out from Each Output, N			10			10	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage		1
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage		2
V_{OH}	Output HIGH Voltage	2.4	3.3		Volts	V_{CC} = MIN., I_{OH} = –0.4 mA, V_{IN} = 0.8 V		2
V_{OL}	Output LOW Voltage		0.22	0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA, V_{IN} = 2.0 V		1
I_{IH}	Input HIGH Current			40	µA	V_{CC} = MAX., V_{IN} = 2.4 V	Each Input	4
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current			–1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V, Each Input		3
I_{OS}	Output Short Circuit Current (Note 3)	–20		–55	mA	9N10/5410	V_{CC} = MAX.	5
		–18		–55	mA	9N10/7410		
I_{CCH}	Supply Current HIGH		3.0	6.0	mA	V_{CC} = MAX., V_{IN} = 0 V		6
I_{CCL}	Supply Current LOW		9.0	16.5	mA	V_{CC} = MAX., V_{IN} = 5.0 V		6

SWITCHING CHARACTERISTICS (T_A = 25°C)

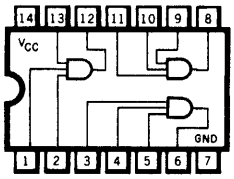
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		11	22	ns	V_{CC} = 5.0 V C_L = 15 pF R_L = 400Ω	A
t_{PHL}	Turn On Delay Input to Output		7.0	15	ns		

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.

TRIPLE 3-INPUT AND GATE

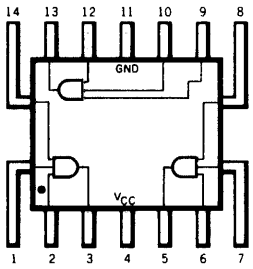
LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)

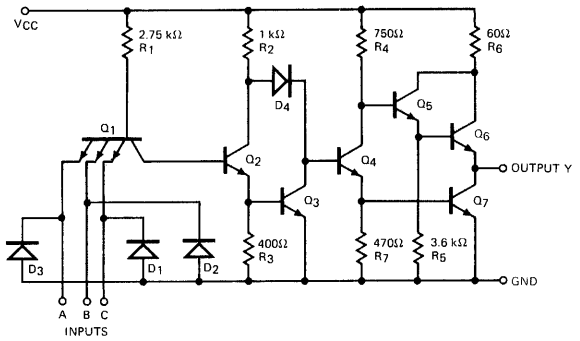


Positive logic: Y = ABC

FLATPAK (TOP VIEW)



SCHEMATIC DIAGRAM
(EACH GATE)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9H11XM/54H11XM			9H11XC/74H11XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	70	°C
Input Loading for Each Input			1.25			1.25	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage	75
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage	77
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = −0.5 mA, V_{IN} = 2.0V	75
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 20 mA, V_{IN} = 0.8 V	77
I_{IH}	Input HIGH Current			50	μA	V_{CC} = MAX., V_{IN} = 2.4 V, Each Input	78
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V, Each Input	
I_{IL}	Input LOW Current			−2.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V, Each Input	79
I_{OS}	Output Short Circuit Current (Note 3)	−40		−100	mA	V_{CC} = MAX., V_{IN} = 4.5 V	80
I_{CCH}	Supply Current HIGH		18	30	mA	V_{CC} = MAX., V_{IN} = 4.5V	81
I_{CCL}	Supply Current LOW		30	48	mA	V_{CC} = MAX., V_{IN} = 0 V	81

SWITCHING CHARACTERISTICS (T_A = 25°C)

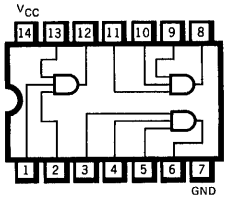
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		7.6	12	ns	V_{CC} = 5.0V, C_L = 25 pF, R_L = 280Ω	T
t_{PHL}	Turn On Delay Input to Output		8.8	12	ns		

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

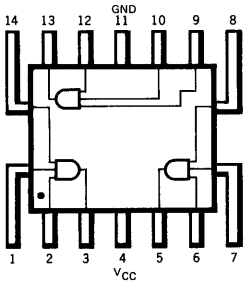
TRIPLE 3-INPUT AND GATE

LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)

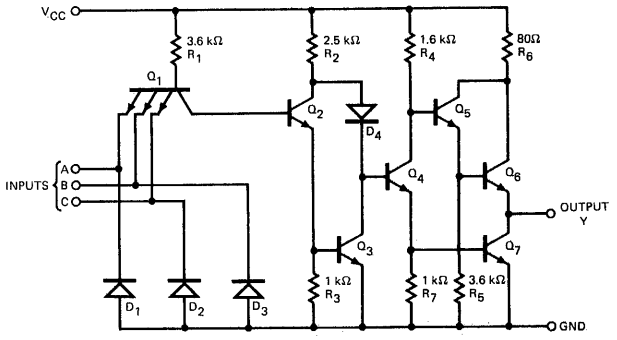


FLATPAK (TOP VIEW)



Positive logic: Y = ABC

SCHEMATIC DIAGRAM (EACH GATE)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9N11XM/5411XM			9N11XC/7411XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	70	°C
Normalized Fan Out from Each Output, N			10			10	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)
		MIN.	TYP. (Note 2)	MAX.		
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = −0.4 mA, V_{IN} = 2 V
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA, V_{IN} = 0.8 V
I_{IH}	Input HIGH Current			40	μA	V_{CC} = MAX., V_{IN} = 2.4 V — Each Input
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V — Each Input
I_{IL}	Input LOW Current			−1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V, Each Input
I_{OS}	Output Short Circuit Current (Note 3)	−40		−100	mA	V_{CC} = MAX., V_{IN} = 4.5 V
I_{CCH}	Supply Current HIGH		10	15	mA	V_{CC} = MAX., V_{IN} = 0 V
I_{CCL}	Supply Current LOW		6.0	24	mA	V_{CC} = MAX., V_{IN} = 5.0 V

SWITCHING CHARACTERISTICS (T_A = 25°C)

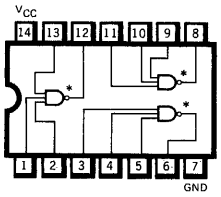
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN.	TYP.	MAX.		
t_{PLH}	Turn Off Delay Input to Output		18	40	ns	V_{CC} = 5.0 V, C_L = 15 pF, R_L = 400Ω
t_{PHL}	Turn On Delay Input to Output		14	25	ns	

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.

TRIPLE 3-INPUT NAND GATE (WITH OPEN-COLLECTOR OUTPUT)

LOGIC AND CONNECTION DIAGRAM

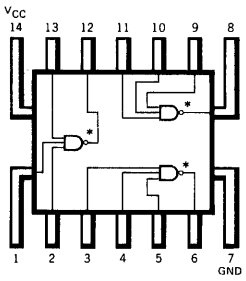
DIP (TOP VIEW)



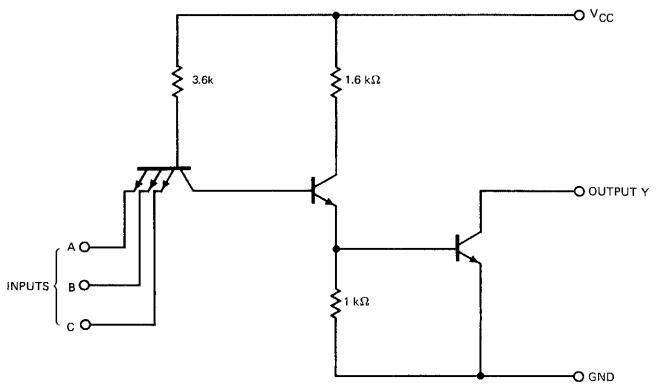
* Open collector

Positive logic: $Y = \overline{ABC}$

FLATPAK (TOP VIEW)



SCHEMATIC DIAGRAM
(EACH GATE)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9N12XM/5412XM			9N12XC/7412XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	70	°C
Normalized Fan Out from Each Output, N			10			10	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage		1
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage		7
I_{OH}	Output HIGH Current			0.25	mA	V_{CC} = MIN., V_{OH} = 5.5 V, V_{IL} = 0.8 V		7
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA, V_{IN} = 2.0 V (On Level)		1
I_{IH}	Input HIGH Current			40	μA	V_{CC} = MAX., V_{IN} = 2.4 V	Each Input	4
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current			–1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V, Each Input		3
I_{CCH}	Supply Current HIGH		~~3.0~~	6.0	mA	V_{CC} = MAX., V_{IN} = 0 V		6
I_{CCL}	Supply Current LOW		9.0	16.5	mA	V_{CC} = MAX., V_{IN} = 5.0 V		6

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS		TEST FIGURE
		MIN.	TYP.	MAX.				
t_{PLH}	Turn Off Delay Input to Output		35	45	ns	R_L = 4 kΩ	V_{CC} = 5.0 V	A
t_{PHL}	Turn On Delay Input to Output		8.0	15	ns	R_L = 400Ω	C_L = 15 pF	

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.

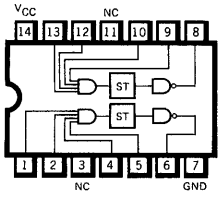
DUAL NAND SCHMITT TRIGGER

DESCRIPTION — The 9N13/5413, 7413 are dual Schmitt triggers functions, compatible with standard TTL output logic levels. Each function is essentially a 4-input NAND gate with different input threshold levels for positive and negative going signals. Typically the hysteresis, the difference between the two threshold levels, is 800 mV.

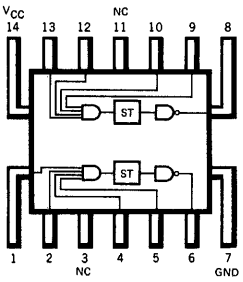
On-chip temperature compensation ensures excellent stability of the hysteresis over a wide temperature range. Typically the hysteresis changes by 3% over the range of –55°C to +125°C, the upper threshold changes by 1% over the same range. The 9N13/5413, 7413 can be triggered from slow input ramps and straight dc levels.

LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)



FLATPAK (TOP VIEW)



Positive logic: $Y = \overline{ABCD}$
NC — No internal connection

RECOMMENDED OPERATING CONDITIONS

PARAMETER		9N13XM/5413XM			9N13XC/7413XC			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}		4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free Air Temperature Range		–55	25	125	0	25	70	°C
Normalized Fan Out from Each Output, N	HIGH Logic			20			20	U.L.
	LOW Logic			10			10	U.L.
Maximum Input Rise and Fall Time		No Restriction			No Restriction			

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.			
V_{T+}	Positive-Going Threshold Voltage	1.5	1.7	2.0	Volts	V_{CC} = 5.0 V	82
V_{T-}	Negative-Going Threshold Voltage	0.6	0.9	1.1	Volts	V_{CC} = 5.0 V	83
$V_{T+}-V_{T-}$	Hysteresis	0.4	0.8		Volts	V_{CC} = 5.0 V	82 & 83
V_{CD}	Input Clamp Diode Voltage			–1.5	Volts	V_{CC} = MIN., I_I = –12 mA	85
V_{OH}	Output HIGH Voltage	2.4	3.3		Volts	V_{CC} = MIN., V_{IN} = 0.6 V, I_{OH} = –0.8 mA	83
V_{OL}	Output LOW Voltage		0.22	0.4	Volts	V_{CC} = MIN., V_{IN} = 2.0 V, I_{OL} = 16 mA	82
I_{T+}	Input Current at Positive-Going Threshold		–0.65		mA	V_{CC} = 5.0 V, V_{IN} = V_{T+}	82
I_{T-}	Input Current at Negative-Going Threshold		–0.85		mA	V_{CC} = 5.0 V, V_{IN} = V_{T-}	83
I_I	Input Current at Maximum Input Voltage			1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	84
I_{IH}	Input HIGH Current			40	μA	V_{CC} = MAX., V_{IN} = 2.4 V	84
I_{IL}	Input LOW Current		–1.0	–1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V	85
I_{OS}	Output Short Circuit Current (Note 3)	–18		–55	mA	V_{CC} = MAX.	86
I_{CCH}	Supply Current HIGH		14	23	mA	V_{CC} = MAX., V_{IN} = 0V	87
I_{CCL}	Supply Current LOW		20	32	mA	V_{CC} = MAX., V_{IN} = 4.5 V	87

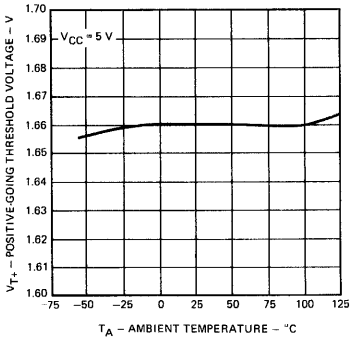
NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS ($T_A = 25°C$)

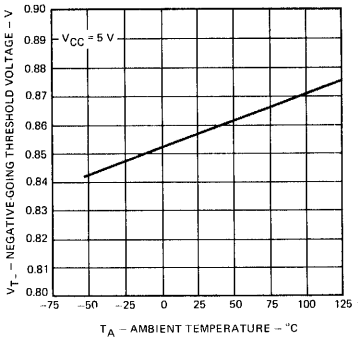
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		18	27	ns	$V_{CC} = 5.0$ V $C_L = 15$ pF $R_L = 400\Omega$	M
t_{PHL}	Turn On Delay Input to Output		15	22	ns		

TYPICAL CHARACTERISTICS

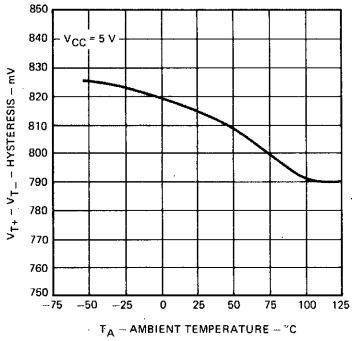
POSITIVE-GOING THRESHOLD VOLTAGE VERSUS AMBIENT TEMPERATURE



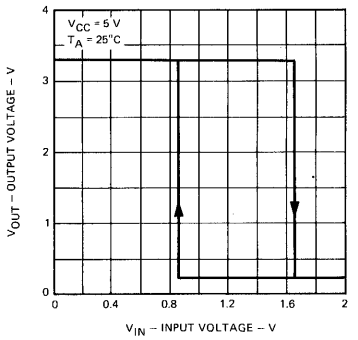
NEGATIVE-GOING THRESHOLD VOLTAGE VERSUS AMBIENT TEMPERATURE



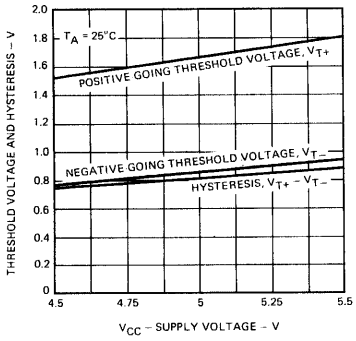
HYSTERESIS VERSUS AMBIENT TEMPERATURE



OUTPUT VOLTAGE VERSUS INPUT VOLTAGE



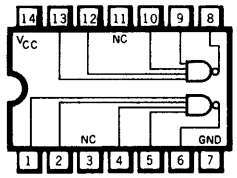
THRESHOLD VOLTAGES AND HYSTERESIS VERSUS SUPPLY VOLTAGE



DUAL 4-INPUT NAND GATE

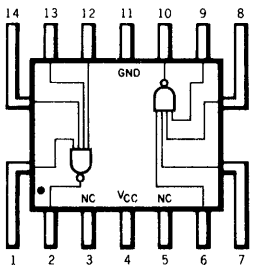
LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)



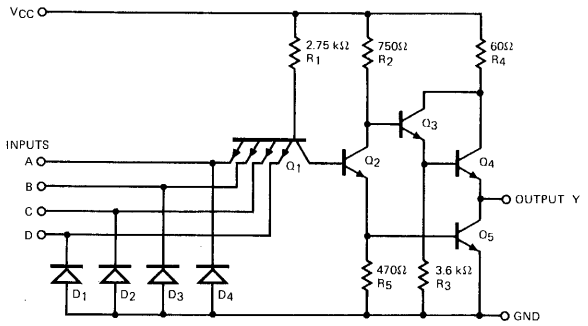
Positive logic: $Y = \overline{ABCD}$

FLATPAK (TOP VIEW)



NC — No internal connection.

SCHEMATIC DIAGRAM (EACH GATE)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9H20XM/54H20XM			9H20XC/74H20XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	70	°C
Input Loading for Each Input			1.25			1.25	U.L.

X = package type; F for Flatapk, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage	1
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage	2
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = −0.5 mA, V_{IN} = 0.8 V	2
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 20 mA, V_{IN} = 2.0V	1
I_{IH}	Input HIGH Current			50	μA	V_{CC} = MAX., V_{IN} = 2.4 V, Each Input	4
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V, Each Input	
I_{IL}	Input LOW Current			−2.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V, Each Input	3
I_{OS}	Output Short Circuit Current (Note 3)	−40		−100	mA	V_{CC} = MAX.	5
I_{CCH}	Supply Current HIGH		5.0	8.4	mA	V_{CC} = MAX., V_{IN} = 0 V	6
I_{CCL}	Supply Current LOW		13	20	mA	V_{CC} = MAX., V_{IN} = 4.5 V	6

SWITCHING CHARACTERISTICS (T_A = 25°C)

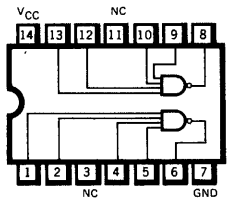
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		6.0	10	ns	V_{CC} = 5.0V, C_L = 25 pF, R_L = 280Ω	T
t_{PHL}	Turn On Delay Input to Output		7.0	10	ns		

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

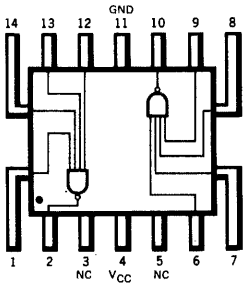
DUAL 4-INPUT NAND GATE

LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)



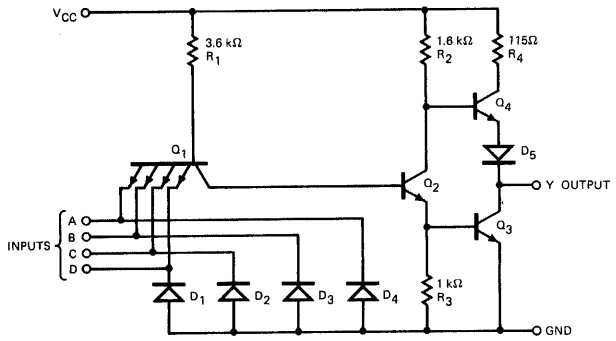
FLATPAK (TOP VIEW)



Positive logic: $Y = \overline{ABCD}$

NC — No internal connection.

SCHEMATIC DIAGRAM (EACH GATE)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9N20XM/5420XM			9N20XC/7420XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	70	°C
Normalized Fan Out From Each Output, N			10			10	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage		1
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage		2
V_{OH}	Output HIGH Voltage	2.4	3.3		Volts	V_{CC} = MIN., I_{OH} = −0.4 mA, V_{IN} = 0.8 V		2
V_{OL}	Output LOW Voltage		0.22	0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA, V_{IN} = 2.0 V		1
I_{IH}	Input HIGH Current			40	μA	V_{CC} = MAX., V_{IN} = 2.4 V	Each Input	4
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current			−1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V, Each Input		3
I_{OS}	Output Short Circuit Current (Note 3)	−20		−55	mA	9N20/5420	V_{CC} = MAX.	5
		−18		−55	mA	9N20/7420		
I_{CCH}	Supply Current HIGH		2.0	4.0	mA	V_{CC} = MAX., V_{IN} = 0 V		6
I_{CCL}	Supply Current LOW		6.0	11	mA	V_{CC} = MAX., V_{IN} = 5.0 V		6

SWITCHING CHARACTERISTICS (T_A = 25°C)

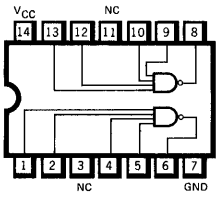
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		12	22	ns	V_{CC} = 5.0 V C_L = 15 pF R_L = 400Ω	A
t_{PHL}	Turn On Delay Input to Output		8.0	15	ns		

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.

DUAL 4-INPUT NAND GATE

LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)

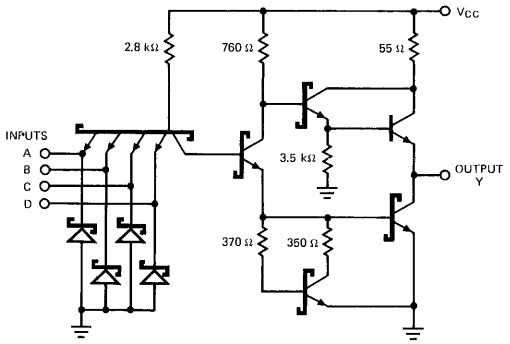


Positive logic: $Y = \overline{ABCD}$

NC—No internal connection.

SHCEMATIC DIAGRAM

(EACH GATE)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9S20XM/54S20XM			9S20XC/74S20XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	-55	25	125	0	25	75	°C
Input Loading for Each Input			1.25			1.25	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER		LIMITS MIN.	LIMITS TYP. (Note 2)	LIMITS MAX.	UNITS	TEST CONDITIONS (Note 1)	
V_{IH}	Input HIGH Voltage		2.0			Volts	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	Volts	Guaranteed Input LOW Voltage	
V_{CD}	Input Clamp Diode Voltage			-0.65	-1.2	Volts	V_{CC} = MIN., I_{IN} = -18mA	
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		Volts	V_{CC} = MIN., I_{OH} = -1.0mA, V_{IN} = 0.8V	
		XC	2.7	3.4				
V_{OL}	Output LOW Voltage			0.35	0.5	Volts	V_{CC} = MIN., I_{OL} = 20mA, V_{IN} = 2.0V	
I_{IH}	Input HIGH Current			1.0	50	μA	V_{CC} = MAX., V_{IN} = 2.7V	Each Input
					1.0	mA	V_{CC} = MAX., V_{IN} = 5.5V	
I_{IL}	Input LOW Current			-1.4	-2.0	mA	V_{CC} = MAX., V_{IN} = 0.5V	Each Input
I_{OS}	Output Short Circuit Current (Note 3)		-40	-65	-100	mA	V_{CC} = MAX., V_{OUT} = 0V	
I_{CCH}	Supply Current HIGH			5.4	8.0	mA	V_{CC} = MAX., V_{IN} = 0V	
I_{CCL}	Supply Current LOW			12.6	18.0	mA	V_{CC} = MAX., Inputs Open	

SWITCHING CHARACTERISTICS (T_A = 25°C)

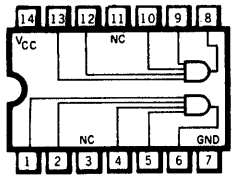
SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS	TEST FIGURES
t_{PLH}	Turn Off Delay Input to Output	2.0	3.0	4.5	ns	V_{CC} = 5.0V	DD
t_{PHL}	Turn On Delay Input to Output	2.0	3.0	5.0	ns	C_L = 15pF	

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0V, 25°C.
(3) Not more than one output should be shorted at a time.

DUAL 4-INPUT AND GATE

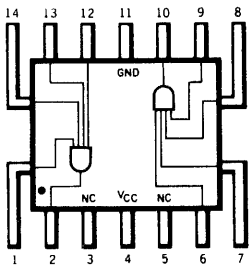
LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)

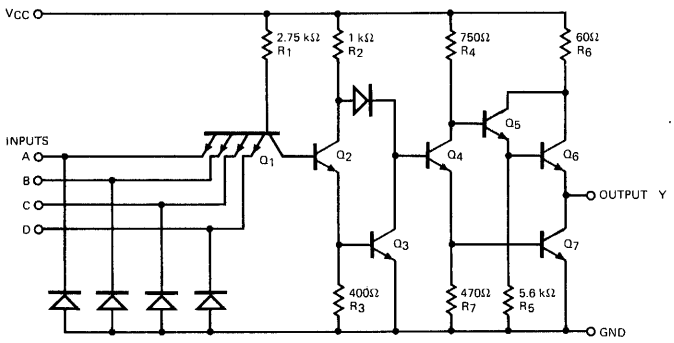


Positive logic: Y = ABCD

FLATPAK (TOP VIEW)



SCHEMATIC DIAGRAM (EACH GATE)



Component values shown are typical.
NC — No internal connection.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9H21XM/54H21XM			9H21XC/74H21XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	70	°C
Input Loading for Each Input			1.25			1.25	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage	75
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage	77
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = −0.5 mA, V_{IN} = 2.0V	75
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 20 mA, V_{IN} = 0.8 V	77
I_{IH}	Input High Current			50	μA	V_{CC} = MAX., V_{IN} = 2.4 V, Each Input	78
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V, Each Input	
I_{IL}	Input LOW Current			−2.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V, Each Input	79
I_{OS}	Output Short Circuit Current (Note 3)	−40		−100	mA	V_{CC} = MAX., V_{IN} = 4.5 V	80
I_{CCH}	Supply Current HIGH		12	20	mA	V_{CC} = MAX., V_{IN} = 4.5 V	81
I_{CCL}	Supply Current LOW		20	32	mA	V_{CC} = MAX., V_{IN} = 0 V	81

SWITCHING CHARACTERISTICS (T_A = 25°C)

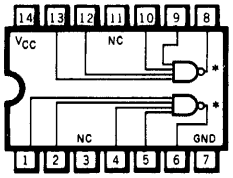
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		7.6	12	ns	V_{CC} = 5.0V, C_L = 25 pF, R_L = 280Ω	T
t_{PHL}	Turn On Delay Input to Output		8.8	12	ns		

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

DUAL 4-INPUT NAND GATE (WITH OPEN-COLLECTOR OUTPUT)

LOGIC AND CONNECTION DIAGRAM

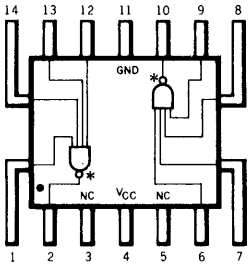
DIP (TOP VIEW)



*OPEN COLLECTOR

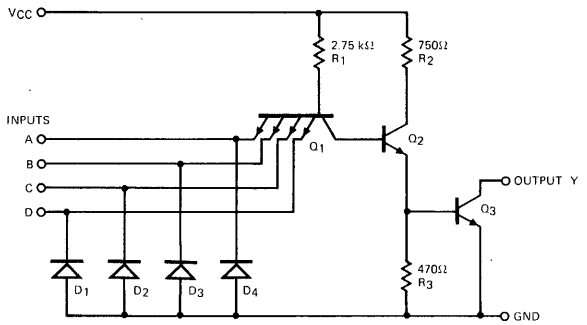
Positive logic: $Y = \overline{ABCD}$

FLATPAK (TOP VIEW)



*OPEN COLLECTOR

SCHEMATIC DIAGRAM (EACH GATE)



Component values shown are typical.
NC — No internal connection.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9H22XM/54H22XM			9H22XC/74H22XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	70	°C
Input Loading for Each Input			1.25			1.25	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP. (Note 2)	LIMITS MAX.	UNITS	TEST CONDITIONS (Note 1)	TEST FIGURE
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage	1
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage	7
I_{OH}	Output HIGH Current			0.25	mA	V_{CC} = MIN., V_{OH} = 5.5 V, V_{IN} = 0.8 V	7
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 20 mA, V_{IN} = 2.0 V	1
I_{IH}	Input HIGH Current			50	μA	V_{CC} = MAX., V_{IN} = 2.4 V, Each Input	4
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V, Each Input	
I_{IL}	Input LOW Current			−2.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V, Each Input	3
I_{CCH}	Supply Current HIGH		3.4	5.0	mA	V_{CC} = MAX., V_{IN} = 0 V	6
I_{CCL}	Supply Current LOW		26	40	mA	V_{CC} = MAX., V_{IN} = 4.5 V	6

SWITCHING CHARACTERISTICS (T_A = 25°C)

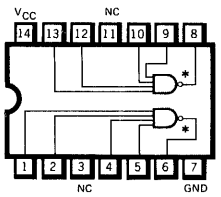
SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS	TEST FIGURE
t_{PLH}	Turn Off Delay Input to Output		10	15	ns	V_{CC} = 5.0 V, C_L = 25 pF, R_L = 280Ω	T
t_{PHL}	Turn On Delay Input to Output		7.5	12	ns		

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.

DUAL 4-INPUT NAND GATE
(WITH OPEN-COLLECTOR OUTPUT)

LOGIC AND CONNECTION DIAGRAM

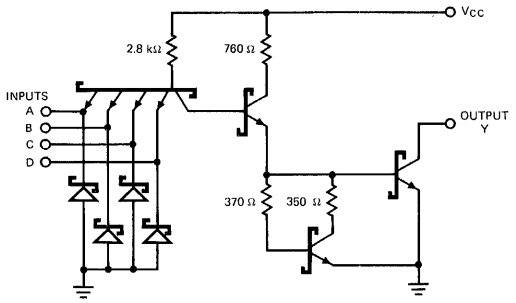
DIP (TOP VIEW)



*OPEN COLLECTOR
NC—No internal connection.
Positive logic: $Y = \overline{ABCD}$

SCHEMATIC DIAGRAM

(EACH GATE)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	† 9S22XM/54S22XM			9S22XC/74S22XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	75	°C
Input Loading for Each Input			1.25			1.25	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage	
V_{CD}	Input Clamp Diode Voltage		-0.65	-1.2	Volts	V_{CC} = MIN., I_{IN} = -18mA	
I_{OH}	Output HIGH Current		0.1	250	μA	V_{CC} = MIN., V_{OH} = 5.5V, V_{IN} = 0.8V	
V_{OL}	Output LOW Voltage		0.35	0.5	Volts	V_{CC} = MIN., I_{OL} = 20mA, V_{IN} = 2.0V	
I_{IH}	Input HIGH Current		1.0	50	μA	V_{CC} = MAX., V_{IN} = 2.7V	Each Input
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5V	
I_{IL}	Input LOW Current		-1.4	-2.0	mA	V_{CC} = MAX., V_{IN} = 0.5V	Each Input
I_{CCH}	Supply Current HIGH		3.0	6.6	mA	V_{CC} = MAX., V_{IN} = 0V	
I_{CCL}	Supply Current LOW		12.6	18.0	mA	V_{CC} = MAX., Inputs Open	

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURES
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output	2.0	5.0	7.5	ns	V_{CC} = 5.0V	EE
t_{PHL}	Turn On Delay Input to Output	2.0	4.5	7.0	ns	C_L = 15pF	

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0V, 25°C.

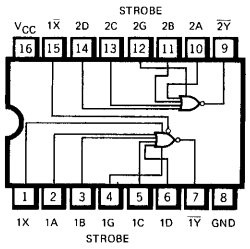
† To be announced 1972

DUAL 4-INPUT NOR GATE WITH STROBE

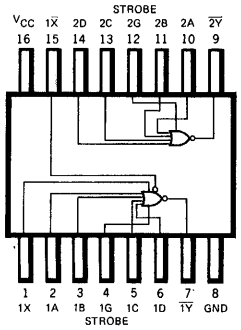
LOGIC AND CONNECTION DIAGRAM

9N23/5423, 7423

DIP (TOP VIEW)



FLATPAK (TOP VIEW)



Positive logic:

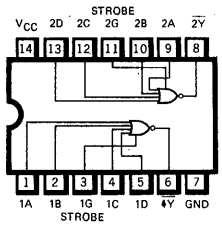
$1Y = \overline{1G(1A+1B+1C+1D)+X}$

$2Y = \overline{2G(2A+2B+2C+2D)}$

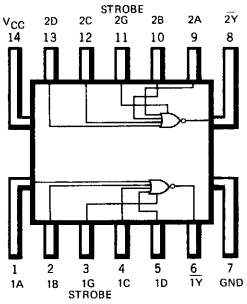
X = Output of 9N60/5460, 7460

9N25/5425, 7425

DIP (TOP VIEW)



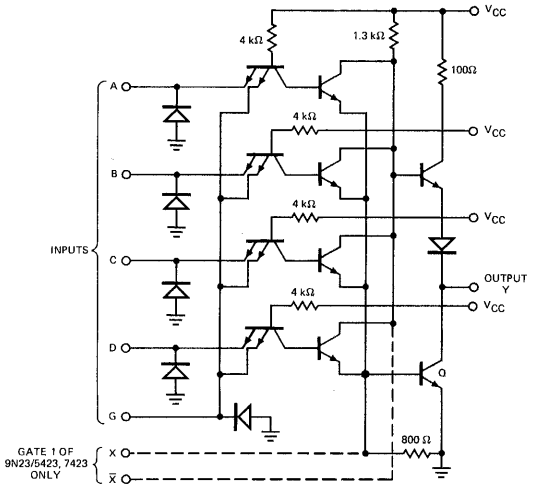
FLATPAK (TOP VIEW)



Positive logic:

$Y = \overline{G(A+B+C+D)}$

SCHEMATIC DIAGRAM
(EACH GATE)



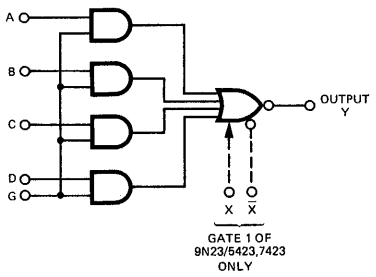
TRUTH TABLE

INPUTS					OUTPUT
A	B	C	D	G	Y
H	X	X	X	H	L
X	H	X	X	H	L
X	X	H	X	H	L
X	X	X	H	H	L
L	L	L	L	X	H
X	X	X	X	L	H

Expander inputs are open.
H = HIGH level, L = LOW level, X = irrelevant

NOTES:
(a) Component values shown are typical.
(b) Both expander inputs are used simultaneously for expanding.
(c) If expander is not used leave X and $\overline{X}$ open.
(d) A total of four expander gates can be connected to the expander inputs.

LOGIC DIAGRAM
(EACH GATE)



RECOMMENDED OPERATING CONDITIONS

PARAMETER		9N23XM/5423XM 9N25XM/5425XM			9N23XC/7423XC 9N25XC/7425XC			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}		4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range		–55	25	125	0	25	70	°C
Normalized Fan Out from Each Output, N	HIGH Level			20			20	U.L.
	LOW Level			10			10	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP. (Note 2)	LIMITS MAX.	UNITS	TEST CONDITIONS (Note 1)	
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage	
V_{CD}	Input Clamp Diode Voltage			–1.5	Volts	V_{CC} = MIN., I_I = –12 mA	
V_{OH}	Output HIGH Voltage	2.4	3.3		Volts	V_{CC} = MIN., I_{OH} = –0.8 mA, V_{IL} = 0.8 V	
V_{OL}	Output LOW Voltage		0.22	0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA, V_{IH} = 2.0 V	
I_I	Input Current at Maximum Input Voltage			1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IH}	Input HIGH Current			40	µA	Data Inputs	V_{CC} = MAX.
				160	µA	Strobe Inputs	V_{IN} = 2.4 V
I_{IL}	Input LOW Current			–1.6	mA	Data Inputs	V_{CC} = MAX.
				–6.4	mA	Strobe Inputs	V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)	–20		–55	mA	V_{CC} = MAX.	
I_{CCH}	Supply Current HIGH		8.0	16	mA	V_{CC} = MAX., All Input at 0 V	
I_{CCL}	Supply Current LOW		10	19	mA	V_{CC} = MAX., All Input at 5.0 V	

ELECTRICAL CHARACTERISTICS (9N23/5423 Circuits Only) Using Expander Inputs, V_{CC} = 4.5 V, T_A = –55°C

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS	TEST FIGURE
I_X	Expander Current			2.9	mA	V_1 = 0.4 V, I_{OL} = 16 mA	28
$V_{BE(Q)}$	Base-Emitter Voltage of Output Transistor Q			1.0	Volt	I_{OL} = 16 mA, I_1 = 0.41 mA, R_1 = 0	29
V_{OH}	Output HIGH Voltage	2.4	3.3		Volts	I_{OH} = –400 µA, I_1 = 0.15 mA, I_2 = –0.15 mA	30
V_{OL}	Output LOW Voltage		0.22	0.4	Volts	I_{OL} = 16 mA, I_1 = 0.3 mA, R_1 = 138Ω	29

ELECTRICAL CHARACTERISTICS (9N23/7423 Circuits Only) Using Expander Inputs, V_{CC} = 4.75 V, T_A = 0°C

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS	TEST FIGURE
I_X	Expander Current			3.1	mA	V_1 = 0.4 V, I_{OL} = 16 mA	28
$V_{BE(Q)}$	Base-Emitter Voltage of Output Transistor Q			1.0	Volt	I_{OL} = 16 mA, I_1 = 0.62 mA, R_1 = 0	29
V_{OH}	Output HIGH Voltage	2.4	3.3		Volts	I_{OH} = –400 µA, I_1 = 0.27 mA, I_2 = –0.27 mA	30
V_{OL}	Output LOW Voltage		0.22	0.4	Volts	I_{OL} = 16 mA, I_1 = 0.43 mA, R_1 = 130Ω	29

SWITCHING CHARACTERISTICS (T_A = 25°C) (Note 4)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS
t_{PLH}	Turn Off Delay Input to Output		13	22	ns	V_{CC} = 5.0 V, C_L = 15 pF, R_L = 400Ω
t_{PHL}	Turn On Delay Input to Output		8.0	15	ns	

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type. Expander inputs X and $\overline{X}$ are open.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.
(4) Switching characteristics of the 9N23/5423, 7423 are tested with the expander pins open.

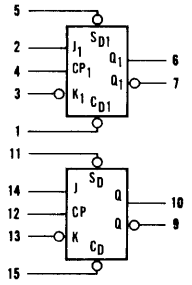
LPTTL/SSI 9L24

LOW POWER DUAL $J\overline{K}$ (OR D) FLIP-FLOP

DESCRIPTION – The Low Power TTL/SSI 9L24 consists of two completely independent transition clocked $J\overline{K}$ flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The $J\overline{K}$ design allows operation as a D flip-flop by simply connecting the J and $\overline{K}$ pins together.

- DUAL RANK TYPE CIRCUIT
- SEPARATE CLOCKS
- SEPARATE ASYNCHRONOUS SET AND CLEAR INPUTS
- 10 MHz TYPICAL TOGGLE FREQUENCY
- TYPICAL POWER DISSIPATION OF 30mW
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- ALL CERAMIC "HERMETIC" 16-LEAD DUAL IN-LINE AND FLAT PACKAGES
- TTL COMPATIBLE

LOGIC SYMBOL

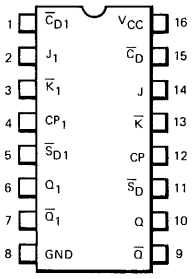


V_{CC} = PIN 16
GND = PIN 8

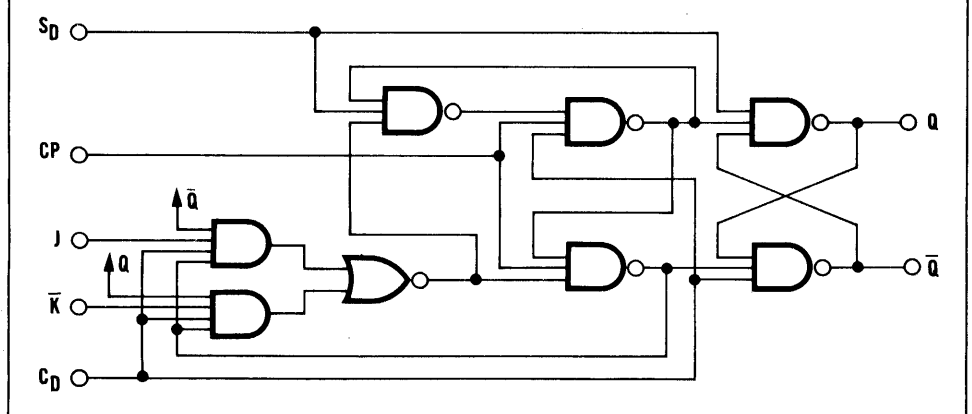
PIN NAMES		LOADING HIGH	LOADING LOW
$J, J_1, \overline{K}, \overline{K}_1$	Flip-Flop Inputs	0.5 U.L.	0.25 U.L.
$\overline{S}_D, \overline{S}_{D1}$	Set Inputs	1.0 U.L.	0.5 U.L.
$\overline{C}_D, \overline{C}_{D1}$	Clear Inputs	2.0 U.L.	0.75 U.L.
CP, CP_1	Clock Inputs	1.0 U.L.	0.5 U.L.
$Q, \overline{Q}, Q_1, \overline{Q}_1$	Flip-Flop Outputs	10 U.L.	2.5 U.L.

1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.

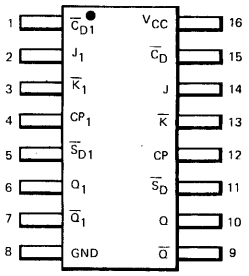
CONNECTION DIAGRAMS
DIP (TOP VIEW)



LOGIC DIAGRAM



FLATPAK (TOP VIEW)



5

TRUTH TABLES

SYNCHRONOUS ENTRY J-$\overline{K}$ MODE OPERATION

INPUTS AT t_n		OUTPUTS AT t_{n+1}	
J	$\overline{K}$	Q	$\overline{Q}$
L	H	No Change	
L	L	L	H
H	H	H	L
H	L	Toggles	

t_n = before clock
t_{n+1} = after clock

SYNCHRONOUS ENTRY D MODE OPERATION

INPUTS AT t_n	OUTPUTS AT t_{n+1}	
D	Q	$\overline{Q}$
L	L	H
H	H	L

J & $\overline{K}$ inputs connected together

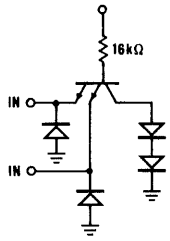
ASYNCHRONOUS ENTRY INDEPENDENT OF CLOCK & SYNCHRONOUS INPUTS

INPUTS		OUTPUTS	
$\overline{S}_D$ 5(11)	$\overline{C}_D$ 1(15)	Q 6(10)	$\overline{Q}$ 7(9)
L	L	H	H
L	H	H	L
H	L	L	H
H	H	No Change	

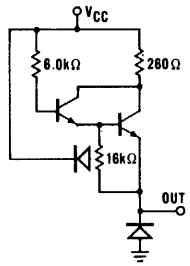
L = LOW Logic Level, H = HIGH Logic Level

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

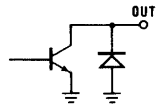
EQUIVALENT INPUT CIRCUIT



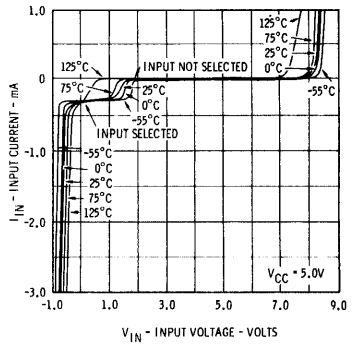
OUTPUT HIGH EQUIVALENT CIRCUIT



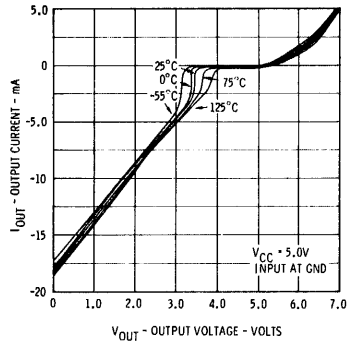
OUTPUT LOW EQUIVALENT CIRCUIT



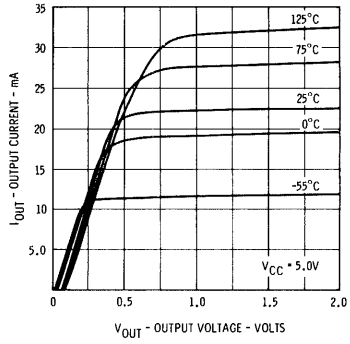
INPUT CURRENT VERSUS INPUT VOLTAGE



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
9L24XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9L24XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP. (Note 4)	LIMITS MAX.	UNITS	CONDITIONS
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = –0.4 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.1	0.3	Volts	V_{CC} = MIN., I_{OL} = 4.0 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage for all Inputs.
V_{IL}	Input LOW Voltage			0.7	Volts	Guaranteed Input LOW Threshold Voltage for all Inputs.
I_{IL}	Input LOW Current J, $\overline{K}$ CP, $\overline{S}_D$ $\overline{C}_D$ (Note 3)		 –0.25 –0.50 –0.75	 –0.4 –0.8 –1.2	mA	V_{CC} = MAX., V_{IN} = 0.3 V.
I_{IH}	Input HIGH Current J, $\overline{K}$ CP, $\overline{S}_D$ $\overline{C}_D$		 2 4 8	 20 40 80	μA	V_{CC} = MAX., V_{IN} = 2.4 V.
	Input HIGH Current			1.0	mA	V_{CC} = MAX., V_{IN} = 5.5V.
I_{SC} (Note 5)	Output Short Circuit Current	–10	–22	–40	mA	V_{CC} = MAX., V_{OUT} = 0.0 V.
I_{CC}	Power Supply Current		6.0	8.8	mA	V_{CC} = MAX.

NOTES:

(1) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.

(2) The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

(3) Denotes maximum current under normal operation. These currents may increase up to 4 I_{IL} if J, $\overline{K}$ = Logic HIGH and $\overline{S}_D$ = Logic LOW.

(4) Typical limits are at V_{CC} = 5.0 V, 25°C, and max. loading.

(5) Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V, C_L = 15 pF)

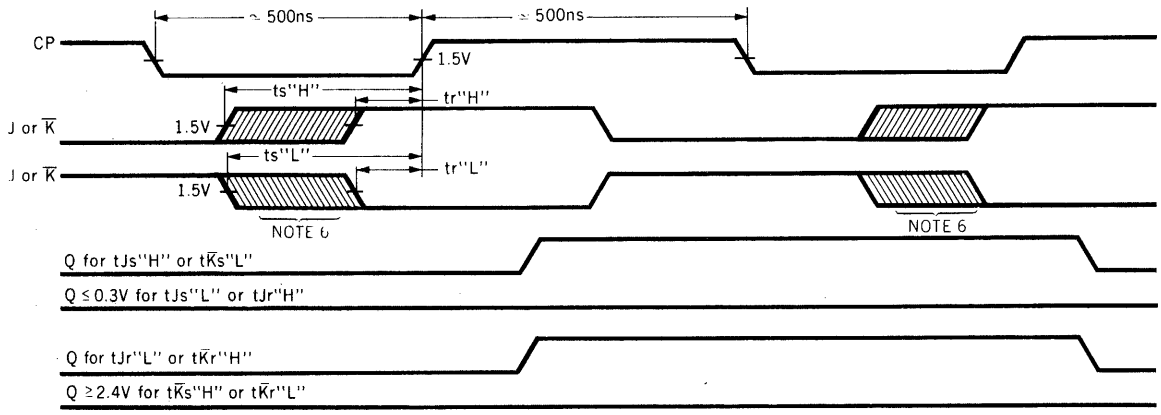
PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	CONDITIONS
t_{PLH} (CP to Q) t_{PLH} (CP to $\overline{Q}$)		40 40		ns	J ≥ 2.4 V, $\overline{K}$ ≤ 0.3 V Fig. 2
t_{PHL} (CP to Q) t_{PHL} (CP to $\overline{Q}$)		60 60		ns	J ≥ 2.4 V, $\overline{K}$ ≤ 0.3 V Fig. 2
t_{PLH} (S_D to Q) t_{PLH} (C_D to $\overline{Q}$)		14 14		ns	J ≥ 2.4 V, $\overline{K}$ ≤ 0.3 V Fig 3
t_{PHL} (S_D to $\overline{Q}$) t_{PHL} (C_D to Q)		50 40		ns	J ≥ 2.4 V, $\overline{K}$ ≤ 0.3 V Fig. 3
t_s "H" (J to CP) t_r "H" (J to CP)		20 20		ns	$\overline{K}$ ≤ 0.3 V Fig. 1
t_s "H" ($\overline{K}$ to CP) t_r "H" ($\overline{K}$ to CP)		1.0 1.0		ns	J ≥ 2.4 V Fig. 1
t_s "L" (J to CP) t_r "L" (J to CP)		–2.0 –2.0		ns	$\overline{K}$ ≤ 0.3 V Fig. 1
t_s "L" ($\overline{K}$ to CP) t_r "L" ($\overline{K}$ to CP)		9.0 9.0		ns	J ≥ 2.4 V Fig. 1
t_{pw} "H" (Clock Pulse Width) t_{pw} "L" (S_D Pulse Width) t_{pw} "L" (C_D Pulse Width)		40 50 40		ns	J ≥ 2.4 V, $\overline{K}$ ≤ 0.3 V
Toggle Frequency		10		MHz	J ≥ 2.4 V, $\overline{K}$ ≤ 0.3 V

5

SET UP TIME – t_s is defined as the time required for the new logic level to be present at the J or $\overline{K}$ inputs prior to the clock transition from LOW to HIGH in order for the flip-flop to respond to the new $J\overline{K}$ mode.

RELEASE TIME – t_r is defined as the time allowed for a new logic level to be present at the J or $\overline{K}$ inputs prior to the clock transition from LOW to HIGH in order for the flip-flop not to respond to the new $J\overline{K}$ mode. A negative Release Time means the new logic level must not occur until after the clock transition.

SET UP AND RELEASE WAVEFORMS



Note (6) FORBIDDEN ZONE, if data changes during the shaded time, the state of the outputs cannot be predetermined.

FIG.1

SWITCHING WAVEFORMS

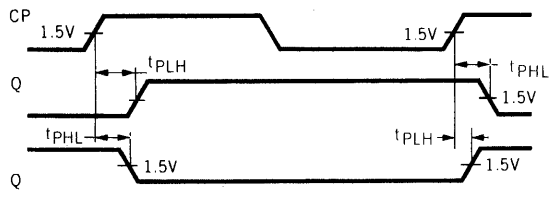


FIG.2

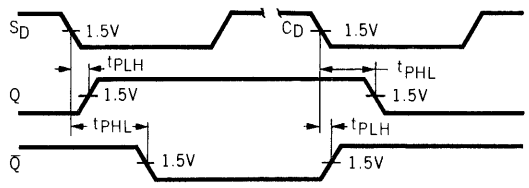


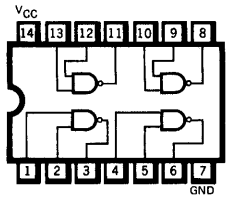
FIG.3

QUAD 2-INPUT HIGH VOLTAGE INTERFACE NAND GATE

DESCRIPTION — These open-collector NAND gates feature high output voltage ratings for interfacing with low threshold voltage MOS logic circuits or other 12V systems. Although the output is rated to withstand 15V, the V_{CC} terminal is connected to the standard 5V source. The output transistor will sink 16 mA while maintaining a low-level output voltage of 0.4V maximum thus providing a high fan out driver with the nominal power dissipation standard Series 9N/54, 74 gates.

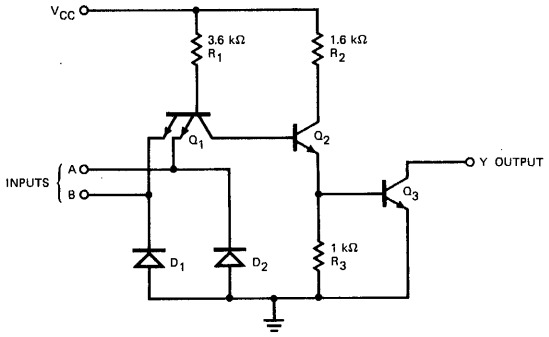
LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)



Positive logic: $Y = \overline{AB}$

SCHEMATIC DIAGRAM
(EACH GATE)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9N26XM/5426XM			9N26XC/7426XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Output Voltage, V_{OH}			15			15	Volts
LOW Level Output Current, I_{OL}			16			16	mA
Operating Free-Air Temperature Range	−55	25	125	0	25	70	°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage		88
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage		89
V_{OH}	Output HIGH Voltage	15			Volts	V_{CC} = MIN., V_{IL} = 0.8 V, I_{OH} = 1.0 mA		89
I_{OH}	Output HIGH Current			50	μA	V_{CC} = MIN., V_{IL} = 0.8 V, V_{OH} = 12 V		89
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA, V_{IH} = 2.0 V		88
I_{IH}	Input HIGH Current			40	μA	V_{CC} = MAX., V_{IN} = 2.4 V	Each Input	90
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current			−1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V, Each Input		91
I_{CCH}	Supply Current HIGH		4.0	8.0	mA	V_{CC} = MAX., V_{IN} = 0 V		92
I_{CCL}	Supply Current LOW		12	22	mA	V_{CC} = MAX., V_{IN} = 5.0 V		92

SWITCHING CHARACTERISTICS (T_A = 25°C)

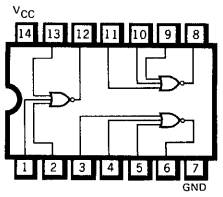
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		16	24	ns	V_{CC} = 5.0 V C_L = 15 pF R_L = 1.0 kΩ	N
t_{PHL}	Turn On Delay Input to Output		11	17	ns		

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.

TRIPLE 3-INPUT NOR GATE

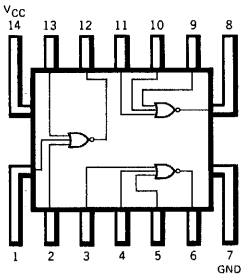
LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)

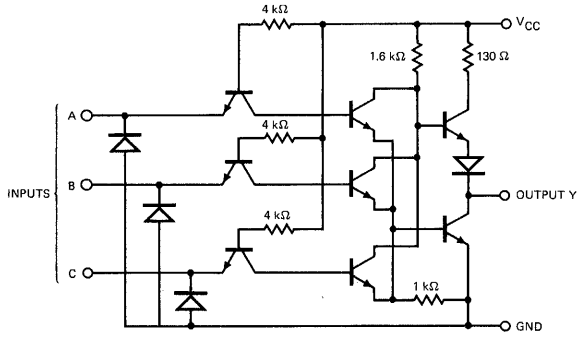


Positive logic: $Y = \overline{A+B+C}$

FLATPAK (TOP VIEW)



SCHEMATIC DIAGRAM
(EACH GATE)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		9N27XM/5427XM			9N27XC/7427XC			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}		4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free Air Temperature Range		−55	25	125	0	25	70	°C
Normalized Fan Out from Each Output, N	HIGH Level			20			20	U.L.
	LOW Level			10			10	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage	
V_{CD}	Input Clamp Diode Voltage			−1.5	Volts	V_{CC} = MIN., I_I = −12 mA	
V_{OH}	Output HIGH Voltage	2.4	3.3			V_{CC} = MIN., I_{OH} = −0.8 mA, V_{IL} = 0.8 V	
V_{OL}	Output LOW Voltage		0.22	0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA, V_{IH} = 2.0 V	
I_I	Input Current at Max. Input Vol.			1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IH}	Input HIGH Current			40	μA	V_{CC} = MAX., V_{IN} = 2.4 V	
I_{IL}	Input LOW Current			−1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current (Note 3)	−20		−55	mA	9N27/5427	V_{CC} = MAX.
		−18		−55	mA	9N27/7427	
I_{CCH}	Supply Current HIGH		10	16	mA	V_{CC} = MAX., (Note 4)	
I_{CCL}	Supply Current LOW		16	26	mA	V_{CC} = MAX., (Note 5)	

SWITCHING CHARACTERISTICS (T_A = 25°C)

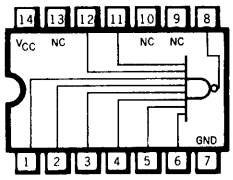
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN.	TYP.	MAX.		
t_{PLH}	Turn Off Delay Input to Output		10	15	ns	V_{CC} = 5.0 V, C_L = 15 pF, R_L = 400Ω
t_{PHL}	Turn On Delay Input to Output		7.0	11	ns	

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.
(4) Measured with all inputs grounded, and outputs open.
(5) Measured with one input of each gate at 4.5 V, the remaining inputs grounded, and outputs open.

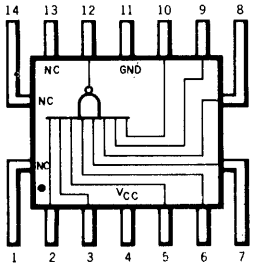
8-INPUT NAND GATE

LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)

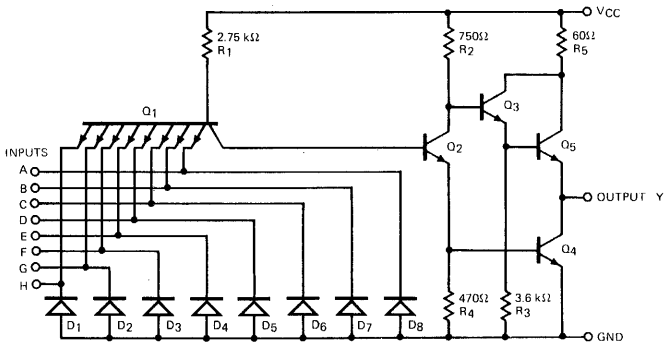


FLATPAK (TOP VIEW)



Positive logic: $Y = \overline{ABCDEFGH}$

SCHEMATIC DIAGRAM (EACH GATE)



Component values shown are typical.
NC — No internal connection.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9H30XM/54H30XM			9H30XC/74H30XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	70	°C
Input Loading for Each Input			1.25			1.25	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage	1
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage	2
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = −0.5 mA, V_{IN} = 0.8 V	2
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 20 mA, V_{IN} = 2.0V	1
I_{IH}	Input HIGH Current			50	μA	V_{CC} = MAX., V_{IN} = 2.4 V, Each Input	4
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V, Each Input	
I_{IL}	Input LOW Current			−2.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V, Each Input	3
I_{OS}	Output Short Circuit Current (Note 3)	−40		−100	mA	V_{CC} = MAX.	5
I_{CCH}	Supply Current HIGH		2.5	4.2	mA	V_{CC} = MAX., V_{IN} = 0 V	6
I_{CCL}	Supply Current LOW		6.5	10	mA	V_{CC} = MAX., V_{IN} = 4.5 V	6

SWITCHING CHARACTERISTICS (T_A = 25°C)

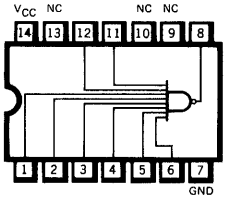
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		6.8	10	ns	V_{CC} = 5.0V, C_L = 25 pF, R_L = 280Ω	T
t_{PHL}	Turn On Delay Input to Output		8.9	12	ns		

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

8-INPUT NAND GATE

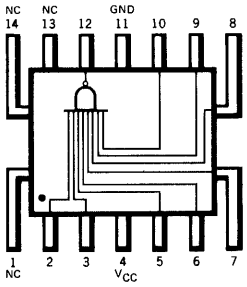
LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)

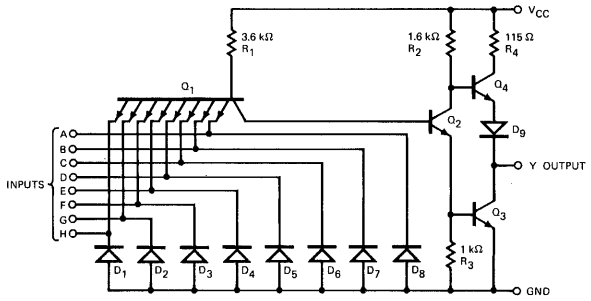


Positive logic: $Y = \overline{ABCDEFGH}$

FLATPAK (TOP VIEW)



SCHEMATIC DIAGRAM



NC — No internal connection.

Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9N30XM/5430XM			9N30XC/7430XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	70	°C
Normalized Fan Out from Each Output, N			10			10	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage		1
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage		2
V_{OH}	Output HIGH Voltage	2.4	3.3		Volts	V_{CC} = MIN., I_{OH} = –0.4 mA, V_{IN} = 0.8 V		2
V_{OL}	Output LOW Voltage		0.22	0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA, V_{IN} = 2.0 V		1
I_{IH}	Input HIGH Current			40	µA	V_{CC} = MAX., V_{IN} = 2.4 V	Each Input	4
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current			–1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V, Each Input		3
I_{OS}	Output Short Circuit Current (Note 3)	–20		–55	mA	9N30/5430	V_{CC} = MAX.	5
		–18		–55	mA	9N30/7430		
I_{CCH}	Supply Current HIGH		1.0	2.0	mA	V_{CC} = MAX., V_{IN} = 0 V		6
I_{CCL}	Supply Current LOW		3.0	6.0	mA	V_{CC} = MAX., V_{IN} = 5.0 V		6

SWITCHING CHARACTERISTICS (T_A = 25°C)

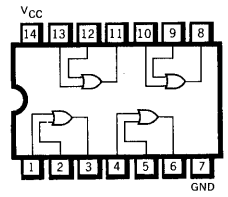
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		13	22	ns	V_{CC} = 5.0 V C_L = 15 pF R_L = 400Ω	A
t_{PHL}	Turn On Delay Input to Output		8.0	15	ns		

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.

QUAD 2-INPUT OR GATE

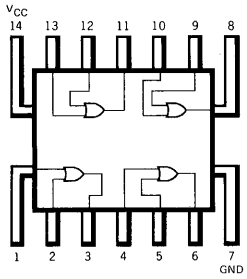
LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)

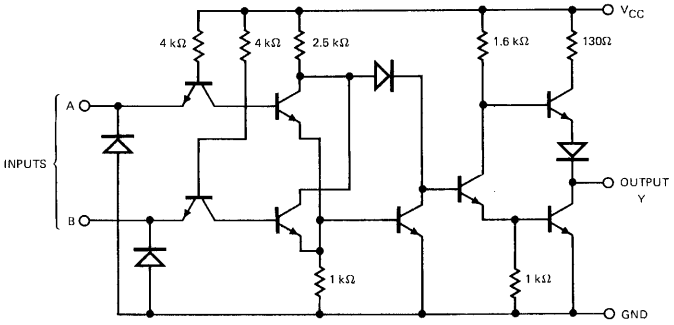


Positive logic: Y = A+B

FLATPAK (TOP VIEW)



SCHEMATIC DIAGRAM
(EACH GATE)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		9N32XM/5432XM			9N32XC/7432XC			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}		4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range		–55	25	125	0	25	70	°C
Normalized Fan Out from Each Output, N	HIGH Level			20			20	U.L.
	LOW Level			10			10	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage	
V_{CD}	Input Clamp Diode Voltage			–1.5	Volts	V_{CC} = MAX., I_I = –12 mA	
V_{OH}	Output HIGH Voltage	2.4	3.3		Volts	V_{CC} = MIN., I_{OH} = –0.8 mA, V_{IH} = 2.0 V	
V_{OL}	Output LOW Voltage		0.22	0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA, V_{IL} = 0.8 V	
I_I	Input Current at Maximum Input Voltage			1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IH}	Input HIGH Current			40	μA	V_{CC} = MAX., V_{IN} = 2.4 V	
I_{IL}	Input LOW Current			–16	mA	V_{CC} = MAX., V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current (Note 3)	–20		–55	mA	9N32/5432	V_{CC} = MAX.
		–18		–55	mA	9N32/7432	
I_{CCH}	Supply Current HIGH		15	22	mA	V_{CC} = MAX., (Note 4)	
I_{CCL}	Supply Current LOW		23	38	mA	V_{CC} = MAX., (Note 5)	

SWITCHING CHARACTERISTICS (T_A = 25°C)

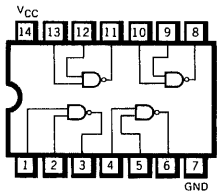
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN.	TYP.	MAX.		
t_{PLH}	Turn Off Delay Input to Output		10	15	ns	V_{CC} = 5.0 V C_L = 15 pF R_L = 400Ω
t_{PHL}	Turn On Delay Input to Output		14	22	ns	

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.
(4) Measured with one input of each gate at 4.5 V, the remaining inputs grounded and outputs open.
(5) Measured with both inputs of all gates grounded, and outputs open.

QUAD 2-INPUT NAND BUFFER

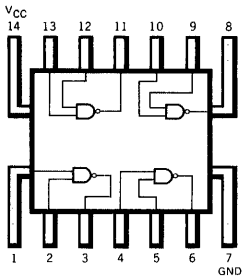
LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)



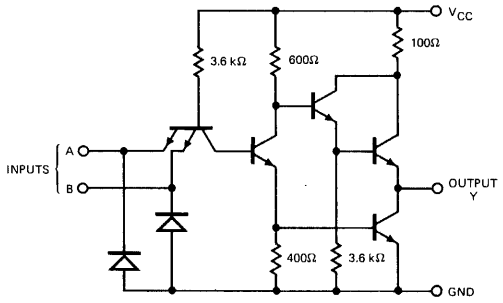
Positive logic: $Y = \overline{AB}$

FLATPAK (TOP VIEW)

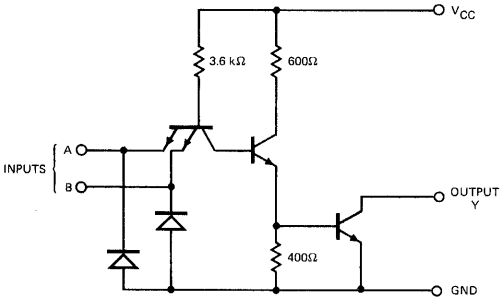


SCHEMATIC DIAGRAM
(EACH BUFFER)

9N37/5437, 7437
(TOTEM-POLE OUTPUT)



9N38/5438, 7438
(OPEN-COLLECTOR OUTPUT)



RECOMMENDED OPERATING CONDITIONS

PARAMETER	9N37XM/5437XM 9N38XM/5438XM			9N37XC/7437XC 9N38XC/7438XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	70	°C
Normalized Fan Out from Each Output, N			30			30	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

9N37/5437, 7437

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)
		MIN.	TYP. (Note 2)	MAX.		
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage
V_{CD}	Input Clamp Diode Voltage			−1.5	Volts	V_{CC} = MIN., I_I = −12 mA
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = −1.2 mA, V_{IL} = 0.8 V
V_{OL}	Output LOW Voltage		0.22	0.4	Volts	V_{CC} = MIN., I_{OL} = 48 mA, V_{IH} = 2.0 V
I_I	Input Current at Maximum Input Voltage			1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{IH}	Input HIGH Current			40	μA	V_{CC} = MAX., V_{IN} = 2.4 V
I_{IL}	Input LOW Current			−1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)	−20		−70	mA	V_{CC} = MAX., V_{IN} = 0 V
I_{CCH}	Supply Current HIGH		9.0	15.5	mA	V_{CC} = MAX., All Inputs at 0 V
I_{CCL}	Supply Current LOW		34	54	mA	V_{CC} = MAX., All Inputs at 5.0 V

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN.	TYP.	MAX.		
t_{PLH}	Turn Off Delay Input to Output		13	22	ns	V_{CC} = 5.0 V C_L = 45 pF R_L = 133Ω
t_{PHL}	Turn On Delay Input to Output		8.0	15	ns	

9N38/5438, 7438

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)
		MIN.	TYP. (Note 2)	MAX.		
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage
V_{CD}	Input Clamp Diode Voltage			−1.5	Volts	V_{CC} = MIN., I_I = −12 mA
I_{OH}	Output HIGH Current			250	μA	V_{CC} = MIN., V_{OH} = 5.5 V, V_{IL} = 0.8 V
V_{OL}	Output LOW Voltage		0.22	0.4	Volts	V_{CC} = MIN., I_{OL} = 48 mA, V_{IH} = 2.0 V
I_I	Input Current at Maximum Input Voltage			1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{IH}	Input HIGH Current			40	μA	V_{CC} = MAX., V_{IN} = 2.4 V
I_{IL}	Input LOW Current			−1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V
I_{CCH}	Supply Current HIGH		5.0	8.5	mA	V_{CC} = MAX., All Inputs at 0 V
I_{CCL}	Supply Current LOW		34	54	mA	V_{CC} = MAX., All Inputs at 5.0 V

SWITCHING CHARACTERISTICS (T_A = 25°C)

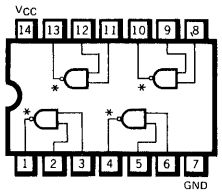
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN.	TYP.	MAX.		
t_{PLH}	Turn Off Delay Input to Output		14	22	ns	V_{CC} = 5.0 V C_L = 45 pF R_L = 133Ω
t_{PHL}	Turn On Delay Input to Output		11	18	ns	

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

QUAD 2-INPUT NAND BUFFER (WITH OPEN COLLECTOR OUTPUT)

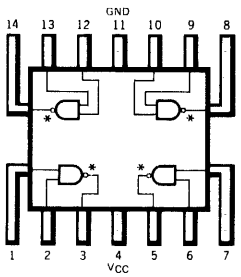
LOGIC AND CONNECTION DIAGRAMS

DIP (TOP VIEW)



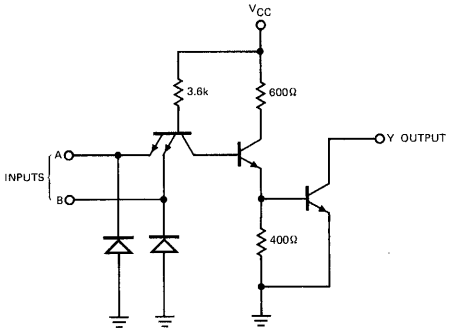
Positive logic: $Y = \overline{AB}$

FLATPAK (TOP VIEW)



*Open Collector

SCHEMATIC DIAGRAM
(EACH GATE)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9N39XM/5439XM			9N39XC/7439XC			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating free-air temperature range	-55	25	125	0	25	70	°C
Normalized fan out from each output, N			30			30	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP (Note 2)	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)	TEST FIGURE
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage	1
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage	7
V_{CD}	Input Clamp Diode Voltage			-1.5	Volts	V_{CC} = MIN., I_I = -12 mA, Other Input OPEN	85
I_{OH}	Output HIGH Current			250	μA	V_{OH} = 5.5 V, V_{IL} = 0.8 V; V_{CC} = MIN., Other input = V_{CC}	7
V_{OL}	Output LOW Voltage		0.22	0.4	Volts	I_{OL} = 48 mA; V_{CC} = MIN.	1
				0.5	Volts	I_{OL} = 60 mA; V_{IN} = 2.0 V	
	9N39/7439			0.6	Volts	I_{OL} = 80 mA; Other input = 2.0V	
I_{IH}	Input HIGH Current			40	μA	V_{CC} = MAX., V_{IN} = 2.4 V, Other Input = 0 V	4
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V, Other Input = 0 V	
I_{IL}	Input LOW Current			-1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V, Other Input = 4.5 V	3
I_{CCH}	Supply Current HIGH		5.0	8.5	mA	V_{CC} = MAX., All Inputs = 0 V	6
I_{CCL}	Supply Current LOW		34	54	mA	V_{CC} = MAX., All Inputs = 5.0 V	6

SWITCHING CHARACTERISTICS (T_A = 25°C)

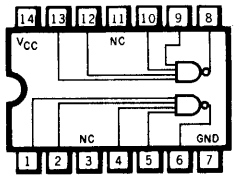
SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	TEST FIGURE
t_{PLH}	Turn Off Delay Input to Output		14	22	ns	V_{CC} = 5.0 V, C_L = 45 pF, R_L = 133Ω	A
t_{PHL}	Turn On Delay Input to Output		12	18	ns		

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.

DUAL 4-INPUT NAND BUFFER

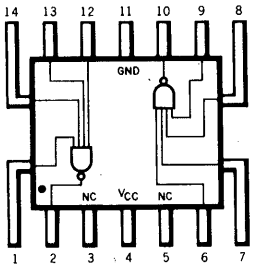
LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)

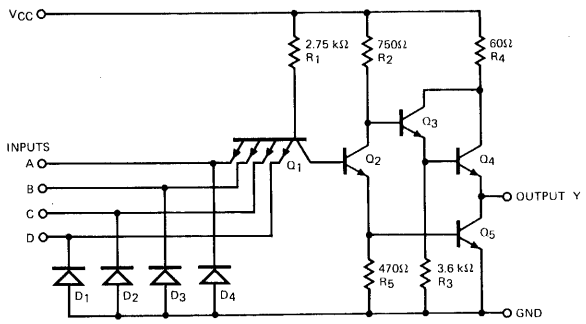


Positive logic: $Y = \overline{ABCD}$

FLATPAK (TOP VIEW)



SCHEMATIC DIAGRAM
(EACH GATE)



Component values shown are typical.
NC — No internal connection

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9H40XM/54H40XM			9H40XC/74H40XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	70	°C
Fan Out from Each Output			37.5			37.5	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage	1
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage	2
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = −1.5 mA, V_{IN} = 0.8 V	2
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 60 mA, V_{IN} = 2.0V	1
I_{IH}	Input HIGH Current			100	μA	V_{CC} = MAX., V_{IN} = 2.4 V, Each Input	4
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V, Each Input	
I_{IL}	Input LOW Current			−4.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V, Each Input	3
I_{OS}	Output Short Circuit Current (Note 3)	−40		−125	mA	V_{CC} = MAX.	5
I_{CCH}	Supply Current HIGH		10.4	16	mA	V_{CC} = MAX., V_{IN} = 0 V	6
I_{CCL}	Supply Current LOW		25	40	mA	V_{CC} = MAX., V_{IN} = 4.5 V	6

SWITCHING CHARACTERISTICS (T_A = 25°C)

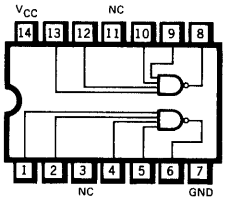
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		6.5	12	ns	V_{CC} = 5.0V, C_L = 25 pF, R_L = 93Ω	T
t_{PHL}	Turn On Delay Input to Output		8.5	12	ns		

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25° C.
(3) Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

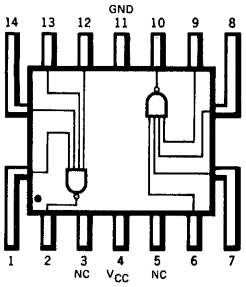
DUAL 4-INPUT NAND BUFFER

LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)



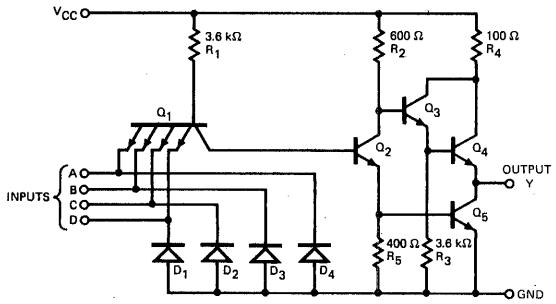
FLATPAK (TOP VIEW)



Positive logic: $Y = \overline{ABCD}$

NC — No internal connection.

SCHEMATIC DIAGRAM
(EACH GATE)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9N40XM/5450XM			9N40XC/7440XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	70	°C
Normalized Fan Out from Each Output, N			30			30	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage		1
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage		2
V_{OH}	Output HIGH Voltage	2.4	3.3		Volts	V_{CC} = MIN., I_{OH} = −1.2 mA, V_{IN} = 0.8 V		2
V_{OL}	Output LOW Voltage		0.28	0.4	Volts	V_{CC} = MIN., I_{OL} = 48 mA, V_{IN} = 2.0 V		1
I_{IH}	Input HIGH Current			40	μA	V_{CC} = MAX., V_{IN} = 2.4 V	Each Input	4
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current			−1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V, Each Input		3
I_{OS}	Output Short Circuit Current (Note 3)	−20		−70	mA	9N40/5440	V_{CC} = MAX.	5
		−18		−70	mA	9N40/7440		
I_{CCH}	Supply Current HIGH		4.0	8.0	mA	V_{CC} = MAX., V_{IN} = 0 V		6
I_{CCL}	Supply Current LOW		17	27	mA	V_{CC} = MAX., V_{IN} = 5.0 V		6

SWITCHING CHARACTERISTICS (T_A = 25°C)

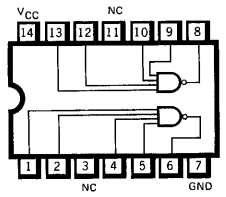
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		13	22	ns	V_{CC} = 5.0 V C_L = 15 pF R_L = 133 Ω	A
t_{PHL}	Turn On Delay Input to Output		8.0	15	ns		

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.

DUAL 4-INPUT NAND BUFFER

LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)

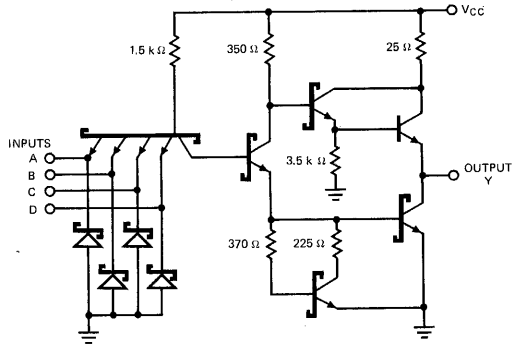


NC—No internal connection.

Positive logic: $Y = \overline{ABCD}$

SCHEMATIC DIAGRAM

(EACH GATE)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9S40XM/54S40XM			9S40XC/74S40XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	75	°C
Fan Out From Each Output			37.5*			37.5*	U.L.

*37.5 (U.L.) is the LOW drive factor and 75 (U.L.) is the HIGH drive factor.
X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER		LIMITS MIN.	LIMITS TYP. (Note 2)	LIMITS MAX.	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			Volts	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage				0.8	Volts	Guaranteed Input LOW Voltage
V_{CD}	Input Clamp Diode Voltage			–0.65	–1.2	Volts	V_{CC} = MIN., I_{IN} = -18mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		Volts	V_{CC} = MIN., I_{OH} = -3.0mA, V_{IN} = 0.8V
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage			0.4	0.5	Volts	V_{CC} = MIN., I_{OL} = 60mA, V_{IN} = 2.0V
I_{IH}	Input HIGH Current			1.0	100	μA	V_{CC} = MAX., V_{IN} = 2.7V — Each Input
					1.0	mA	V_{CC} = MAX., V_{IN} = 5.5V
I_{IL}	Input LOW Current			–2.5	–4.0	mA	V_{CC} = MAX., V_{IN} = 0.5V — Each Input
I_{OS}	Output Short Circuit Current (Note 3)		–50	–150	–225	mA	V_{CC} = MAX., V_{OUT} = 0V
I_{CCH}	Supply Current HIGH			8.2	18.0	mA	V_{CC} = MAX., V_{IN} = 0V
I_{CCL}	Supply Current LOW			27.2	44.0	mA	V_{CC} = MAX., Inputs Open

SWITCHING CHARACTERISTICS (T_A = 25°C)

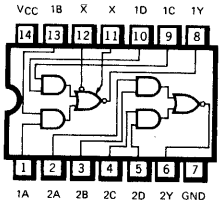
SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS	TEST FIGURES
t_{PLH}	Turn Off Delay Input to Output	2.0	4.0	6.5	ns	V_{CC} = 5.0V, C_L = 50pF	DD
t_{PHL}	Turn On Delay Input to Output	2.0	4.0	6.5	ns		

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0V, 25°C.
(3) Not more than one output should be shorted at a time.

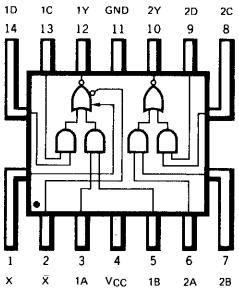
DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATE

LOGIC AND CONNECTION DIAGRAM

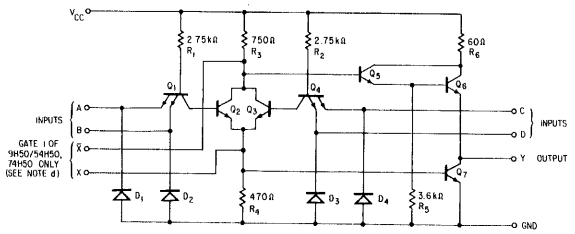
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



SCHEMATIC DIAGRAM
(EACH GATE)



Positive logic: $Y = \overline{(AB) + (CD) + (X)}$
(X = Output of 9H60/54H60, 74H60 or 9H62/54H62, 74H62)

NOTES:
(a) Component values shown are typical.
(b) Both expander inputs are used simultaneously for expanding.
(c) If expander is not used leave X and $\overline{X}$ pins open.
(d) Expander inputs X and $\overline{X}$ are functional on the 9H50/54H50, 74H50 circuits only. Make no external connection to X and $\overline{X}$ pins of the 9H51/54H51, 74H51.
(e) A total of four 9H60/54H60, 74H60 expander gates or one 9H62/54H62, 74H62 expander gate may be connected to the expander inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9H50XM/54H50XM 9H51XM/54H51XM			9H50XC/74H50XC 9H51XC/74H51XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	70	°C
Input Loading for Each Input			1.25			1.25	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP. (Note 2)	LIMITS MAX.	UNITS	TEST CONDITIONS (Note 1)	TEST FIGURE
V_{IH}	Input HIGH Voltage (Note 4)	2.0			Volts	Guaranteed Input HIGH Voltage	21
V_{IL}	Input LOW Voltage (Note 5)			0.8	Volts	Guaranteed Input LOW Voltage	22
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = −0.5 mA, V_{IN} = 0.8 V	22
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 20 mA, V_{IN} = 2.0 V	21
I_{IH}	Input HIGH Current			50	μA	V_{CC} = MAX., V_{IN} = 2.4 V; Each Input	24
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IL}	Input LOW Current			−2.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V, Each Input	23
I_{OS}	Output Short Circuit Current (Note 3)	−40		−100	mA	V_{CC} = MAX.	25
I_{CCH}	Supply Current HIGH		8.2	12.8	mA	V_{CC} = MAX., V_{IN} = 0 V	27
I_{CCL}	Supply Current LOW		15.2	24	mA	V_{CC} = MAX., V_{IN} = 4.5 V	26

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type. Expander pins are open.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.
(4) Required at both input terminals of either AND section to ensure LOW level at output.
(5) Required at one input terminal of each AND section to ensure HIGH level at output.

ELECTRICAL CHARACTERISTICS (9H50/54H50 Circuits Only) Using Expander Inputs, V_{CC} = 4.5 V, T_A = –55°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
$I_{IN\overline{X}}$	Expander-Node Input Current			–5.85	mA	$V_{\overline{X}}$ = 1.4 V	104
$V_{BE(Q)}$	Base-Emitter Voltage of Output Transistor Q			1.0	Volts	I_{OL} = 20 mA, I_1 = 700 μA, R_1 = 0Ω	29
V_{OH}	Output HIGH Voltage	2.4			Volts	I_{OH} = –500 μA, I_1 = 320 μA, I_2 = –320 μA	30
V_{OL}	Output LOW Voltage			0.4	Volts	I_{OL} = 20 mA, I_1 = 470 μA, R_1 = 68Ω	29

ELECTRICAL CHARACTERISTICS (9H50/74H50 Circuits Only) Using Expander Inputs, V_{CC} = 4.75 V, T_A = 0°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
$I_{IN\overline{X}}$	Expander-Node Input Current			–6.3	mA	$V_{\overline{X}}$ = 1.4 V	104
$V_{BE(Q)}$	Base-Emitter Voltage of Output Transistor Q			1.0	Volts	I_{OL} = 20 mA, I_1 = 1.1 mA, R_1 = 0Ω	29
V_{OH}	Output HIGH Voltage	2.4			Volts	I_{OH} = –500 μA, I_1 = 570 μA, I_2 = –570 μA	30
V_{OL}	Output LOW Voltage			0.4	Volts	I_{OL} = 20 mA, I_1 = 600 μA, R_1 = 63Ω	29

SWITCHING CHARACTERISTICS, Expander Pins are Open (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		6.8	11	ns	V_{CC} = 5.0 V C_L = 25 pF R_L = 280Ω	T
t_{PHL}	Turn On Delay Input to Output		6.2	11	ns		

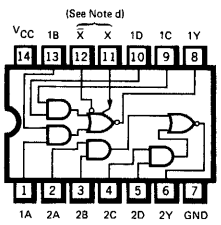
SWITCHING CHARACTERISTICS (9H50/54H50, 74H50 Circuits Only) (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		11		ns	V_{CC} = 5.0 V C_L = 25 pF R_L = 280Ω *C_X = 15 pF	U *MM & NN
t_{PHL}	Turn On Delay Input to Output		7.4		ns		

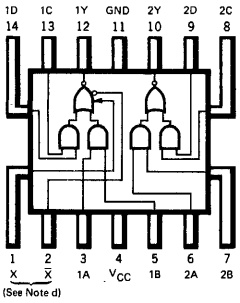
EXPANDABLE DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATE

LOGIC AND CONNECTION DIAGRAM

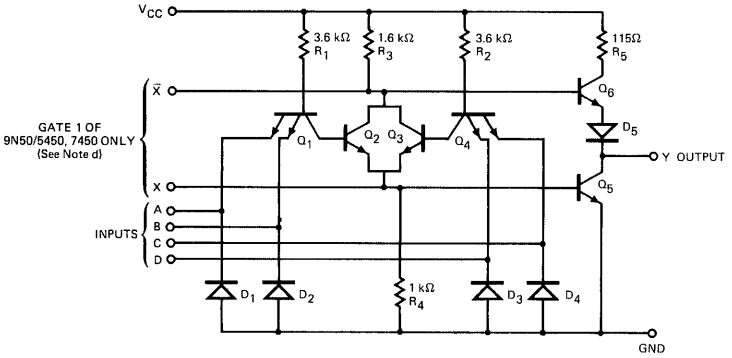
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



SCHEMATIC DIAGRAM
(EACH GATE)



Positive logic: $Y = \overline{(AB) + (CD) + (X)}$
(X = Output of 9N60/5460, 7460)

NOTES:
(a) Component values shown are typical.
(b) Both expander inputs are used simultaneously for expanding.
(c) If expander is not used leave X and $\overline{X}$ pins open.
(d) Make no external connection to X and $\overline{X}$ pins of the 9N51/5451, 7451.
(e) A total of four expander gates can be connected to the expander inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9N50XM/5450XM 9N51XM/5451XM			9N50XC/7450XC 9N51XC/7451XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	70	°C
Normalized Fan Out from Each Output, N			10			10	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP. (Note 2)	LIMITS MAX.	UNITS	TEST CONDITIONS (Note 1)	TEST FIGURE
V_{IH}	Input HIGH Voltage (Note 4)	2.0			Volts	Guaranteed Input HIGH Voltage	21
V_{IL}	Input LOW Voltage (Note 5)			0.8	Volts	Guaranteed Input LOW Voltage	22
V_{OH}	Output HIGH Voltage	2.4	3.3		Volts	V_{CC} = MIN., I_{OH} = –0.4 mA, V_{IN} = 0.8 V	22
V_{OL}	Output LOW Voltage		0.22	0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA, V_{IN} = 2.0 V	21
I_{IH}	Input HIGH Current			40	μA	V_{CC} = MAX., V_{IN} = 2.4 V; Each Input	24
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V; Each Input	24
I_{IL}	Input LOW Current			–1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V, Each Input	23
I_{OS}	Output Short Circuit Current (Note 3)	–20		–55	mA	9N50/5450; 9N51/5451; V_{CC} = MAX.	25
		–18		–55	mA	9N50/7450; 9N51/7451; V_{CC} = MAX.	25
I_{CCH}	Supply Current HIGH		4.0	8.0	mA	V_{CC} = MAX., V_{IN} = 0 V	26
I_{CCL}	Supply Current LOW		7.4	14	mA	V_{CC} = MAX., V_{IN} = 5.0 V	27

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type. Expander inputs X and $\overline{X}$ are open.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.
(4) Required at both input terminals of either AND section to ensure LOW level at output.
(5) Required at one input terminal of each AND section to ensure HIGH level at output.

ELECTRICAL CHARACTERISTICS (9N50/5450 CIRCUITS), Using Expander Inputs, V_{CC} = 4.5 V, T_A = –55°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
I_X	Expander Current			2.9	mA	V_1 = 0.4 V, I_{OL} = 16 mA	28
$V_{BE(Q)}$	Base-Emitter Voltage of Output Transistor Q			1.0	Volts	I_{OL} = 16 mA, I_1 = 0.41 mA, R_1 = 0Ω	29
V_{OH}	Output HIGH Voltage	2.4	3.3		Volts	I_{OH} = –400 μA, I_1 = 0.15 mA, I_2 = –0.15 mA	30
V_{OL}	Output LOW Voltage		0.22	0.4	Volts	I_{OL} = 16 mA, I_1 = 0.3 mA, R_1 = 138Ω	29

ELECTRICAL CHARACTERISTICS (9N50/7450 CIRCUITS), Using Expander Inputs, V_{CC} = 4.75 V, T_A = 0°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
I_X	Expander Current			3.1	mA	V_1 = 0.4 V, I_{OL} = 16 mA	28
$V_{BE(Q)}$	Base-Emitter Voltage of Output Transistor Q			1.0	Volts	I_{OL} = 16 mA, I_1 = 0.62 mA, R_1 = 0Ω	29
V_{OH}	Output HIGH Voltage	2.4	3.3		Volts	I_{OH} = –400 μA, I_1 = 270 μA, I_2 = –270 μA	30
V_{OL}	Output LOW Voltage		0.22	0.4	Volts	I_{OL} = 16 mA, I_1 = 0.43 mA, R_1 = 130Ω	29

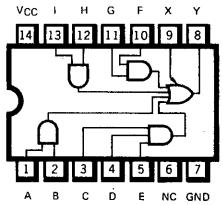
SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		13	22	ns	V_{CC} = 5.0 V C_L = 15 pF R_L = 400Ω	A
t_{PHL}	Turn On Delay Input to Output		8.0	15	ns		

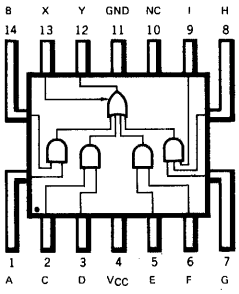
EXPANDABLE 2-2-2-3-INPUT AND-OR GATE

LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)



FLATPAK (TOP VIEW)



Positive logic:

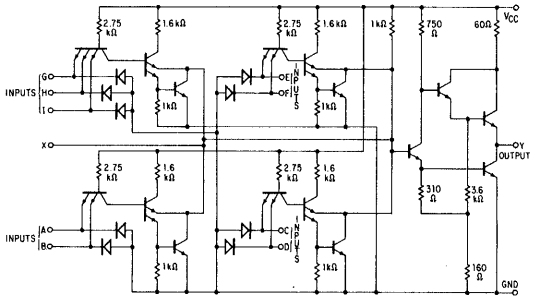
$Y = (AB) + (CDE) + (FG) + (HI) + (X)$

Positive logic:

$Y = (AB) + (CD) + (EF) + (GHI) + (X)$

(X = Output of 9H61/54H61, 74H61)

SCHEMATIC DIAGRAM



NOTES:
(a) Component values shown are typical.
(b) A total of six expander gates may be connected to the expander input X.
(c) NC — No internal connection.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9H52XM/54H52XM			9H52XC/74H52XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	70	°C
Input Loading for Each Input			1.25			1.25	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage (Note 4)	2.0			Volts	Guaranteed Input HIGH Voltage		105
V_{IL}	Input LOW Voltage (Note 5)			0.8	Volts	Guaranteed Input LOW Voltage		106
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = −0.5 mA, V_{IN} = 2.0 V		105
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 20 mA, V_{IN} = 0.8 V		106
I_{IH}	Input HIGH Current			50	μA	V_{CC} = MAX., V_{IN} = 2.4 V	Each Input	108
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current			−2.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V, Each Input		107
I_{OS}	Output Short Circuit Current (Note 3)	−40		−100	mA	V_{CC} = MAX., V_{IN} = 4.5 V		109
I_{CCH}	Supply Current HIGH		20	31	mA	V_{CC} = MAX., V_{IN} = 4.5 V		110
I_{CCL}	Supply Current LOW		15.2	24	mA	V_{CC} = MAX., V_{IN} = 0V		110

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type. Expander pin is open.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Duration of short-circuit test should not exceed 1 second.
(4) Required at all input terminals of one AND section to ensure HIGH level at output.
(5) Required at one input terminal of each AND section to ensure LOW level at output.

ELECTRICAL CHARACTERISTICS (9H52/54H52 Circuits Only) Using Expander Inputs, V_{CC} = 4.5 V

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
I_{INX}	Expander-Node Input Current	−2.7		−4.5	mA	V_X = 1.0 V, I_{OH} = −500 μA, T_A = −55°C	111
V_{OH}	Output HIGH Voltage	2.4			Volts		
V_{OL}	Output LOW Voltage			0.4	Volts	I_{INX} = −300 μA, I_{OL} = 20 mA, T_A = 125°C	112

ELECTRICAL CHARACTERISTICS (9H52/74H52 Circuits Only) Using Expander Inputs, V_{CC} = 4.75 V

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
I_{INX}	Expander-Node Input Current	−2.9		−5.35	mA	V_X = 1.0 V, I_{OH} = −500 μA, T_A = 0°C	111
V_{OH}	Output HIGH Voltage	2.4			Volts		
V_{OL}	Output LOW Voltage			0.4	Volts	I_{INX} = −300 μA, I_{OL} = 20 mA, T_A = 70°C	112

SWITCHING CHARACTERISTICS, Expander Pin is Open (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		10.6	15	ns	V_{CC} = 5.0 V C_L = 25 pF R_L = 280Ω	T
t_{PHL}	Turn On Delay Input to Output		9.2	15	ns		

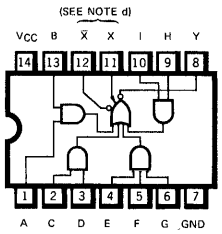
SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		14.8		ns	V_{CC} = 5.0 V C_L = 25 pF R_L = 280Ω *C_X = 15 pF	V *MM & NN
t_{PHL}	Turn On Delay Input to Output		9.8		ns		

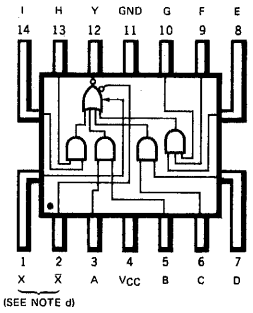
EXPANDABLE 2-2-2-3 INPUT AND-OR-INVERT GATE

LOGIC AND CONNECTION DIAGRAM

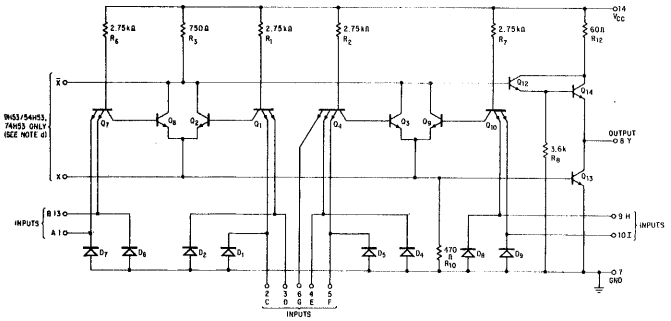
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



SCHEMATIC DIAGRAM



Positive logic: $Y = \overline{(AB) + (CD) + (EFG) + (HI)\,E\,(X)}$
(X = Output of 9H60/54H60, 74H60 or 9H62/54H62, 74H62)

NOTES:
(a) Component values shown are typical.
(b) Both expander inputs are used simultaneously for expanding.
(c) If expander is not used leave X and $\overline{X}$ pins open.
(d) Expander inputs X and $\overline{X}$ are functional on the 9H53/54H53, 74H53 circuits only. Make no external connection to X and $\overline{X}$ pins of the 9H54/54H54, 74H54.
(e) A total of four 9H60/54H60, 74H60 expander gates or one 9H62/54H62, 74H62 expander gate may be connected to the expander inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9H53XM/54H53XM 9H54XM/54H54XM			9H53XC/74H53XC 9H54XC/74H54XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	70	°C
Input Loading for Each Input			1.25			1.25	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP. (Note 2)	LIMITS MAX.	UNITS	TEST CONDITIONS (Note 1)	TEST FIGURE
V_{IH}	Input HIGH Voltage (Note 4)	2.0			Volts	Guaranteed Input HIGH Voltage	21
V_{IL}	Input LOW Voltage (Note 5)			0.8	Volts	Guaranteed Input LOW Voltage	22
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = −0.5 mA, V_{IN} = 0.8 V	22
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 20 mA, V_{IN} = 2.0 V	21
I_{IH}	Input HIGH Current			50	µA	V_{CC} = MAX., V_{IN} = 2.4 V, Each Input	24
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V, Each Input	24
I_{IL}	Input LOW Current			−2.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V, Each Input	23
I_{OS}	Output Short Circuit Current (Note 3)	−40		−100	mA	V_{CC} = MAX.	25
I_{CCH}	Supply Current HIGH		7.1	11	mA	V_{CC} = MAX., V_{IN} = 0 V	27
I_{CCL}	Supply Current LOW		9.4	14	mA	V_{CC} = MAX., V_{IN} = 4.5 V	26

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type. Expander pins are open.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Duration of short-circuit test should not exceed 1 second.
(4) Required at all input terminals of one AND section to ensure LOW level at output.
(5) Required at one input terminal of each AND section to ensure HIGH level at output.

ELECTRICAL CHARACTERISTICS (9H53/54H53 Circuits Only) Using Expander Inputs, V_{CC} = 4.5 V, T_A = −55°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX			
$I_{IN\overline{X}}$	Expander-Node Input Current			−5.85	mA	$V_{\overline{X}}$ = 1.4 V	104
$V_{BE(Q)}$	Base-Emitter Voltage of Output Transistor Q			1.0	Volts	I_{OL} = 20 mA, I_1 = 700 μA, R_1 = 0Ω	29
V_{OH}	Output HIGH Voltage	2.4			Volts	I_{OH} = −500 μA, I_1 = 320 μA, I_2 = −320 μA	30
V_{OL}	Output LOW Voltage			0.4	Volts	I_{OL} = 20 mA, I_1 = 470 μA, R_1 = 68Ω	29

ELECTRICAL CHARACTERISTICS (9H53/74H53 Circuits Only) Using Expander Inputs, V_{CC} = 4.75 V, T_A = 0°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
$I_{IN\overline{X}}$	Expander-Node Input Current			−6.3	mA	$V_{\overline{X}}$ = 1.4 V	104
$V_{BE(Q)}$	Base-Emitter Voltage of Output Transistor Q			1.0	Volts	I_{OL} = 20 mA, I_1 = 1.1 mA, R_1 = 0Ω	29
V_{OH}	Output HIGH Voltage	2.4			Volts	I_{OH} = −500 μA, I_1 = 570 μA, I_2 = −570 μA	30
V_{OL}	Output LOW Voltage			0.4	Volts	I_{OL} = 20 mA, I_1 = 600 μA, R_1 = 63Ω	29

SWITCHING CHARACTERISTICS, Expander Pins are Open (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		7.0	11	ns	V_{CC} = 5.0V C_L = 25 pF R_L = 280Ω	T
t_{PHL}	Turn On Delay Input to Output		6.2	11	ns		

SWITCHING CHARACTERISTICS (9H53/54H53, 74H53 Circuits Only) (T_A = 25°C)

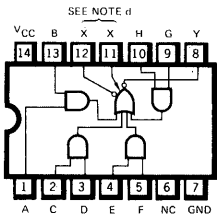
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		11.4			V_{CC} = 5.0 V C_L = 25 pF R_L = 280Ω *C_X = 15 pF	U *MM & NN
t_{PHL}	Turn On Delay Input to Output		7.4				

5

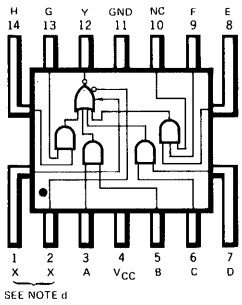
EXPANDABLE 4-WIDE 2-INPUT AND-OR-INVERT GATE

LOGIC AND CONNECTION DIAGRAM

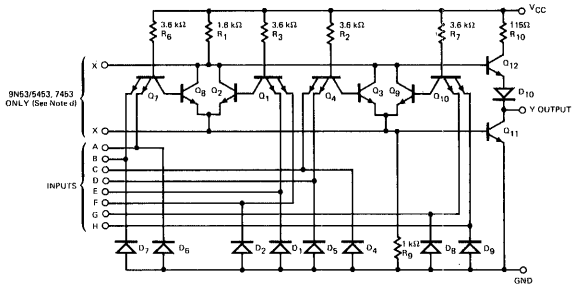
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



SCHEMATIC DIAGRAM



Positive logic: $Y = \overline{(AB) + (CD) + (EF) + (GH) + (X)}$
(X = Output of 9N60/5460, 7460)

NOTES:
(a) Component values shown are typical.
(b) Both expander inputs are used simultaneously for expanding.
(c) If expander is not used leave X and $\overline{X}$ pins open.
(d) Make no external connection to X and $\overline{X}$ pins of the 9N54/5454, 7454.
(e) A total of four expander gates can be connected to the expander inputs.
(f) NC — No internal connection.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9N53XM/5453XM 9N54XM/5454XM			9N53XC/7453XC 9N54XC/7454XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	70	°C
Normalized Fan-Out from Each Output, N			10			10	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP. (Note 2)	LIMITS MAX.	UNITS	TEST CONDITIONS (Note 1)	TEST FIGURE
V_{IH}	Input HIGH Voltage (Note 4)	2.0			Volts	Guaranteed Input HIGH Voltage	21
V_{IL}	Input LOW Voltage (Note 5)			0.8	Volts	Guaranteed Input LOW Voltage	22
V_{OH}	Output HIGH Voltage	2.4	3.3		Volts	V_{CC} = MIN., I_{OH} = −0.4 mA, V_{IN} = 0.8 V	22
V_{OL}	Output LOW Voltage		0.22	0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA, V_{IN} = 2.0 V	21
I_{IH}	Input HIGH Current			40	μA	V_{CC} = MAX., V_{IN} = 2.4 V	Each Input 24
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IL}	Input LOW Current			−1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V, Each Input	23
I_{OS}	Output Short Circuit Current (Note 3)	−20		−55	mA	9N53/5453; 9N54/5454	V_{CC} = MAX. 25
		−18		−55	mA	9N53/7453; 9N54/7454	
I_{CCH}	Supply Current HIGH		4.0	8.0	mA	V_{CC} = MAX., V_{IN} = 0 V	26
I_{CCL}	Supply Current LOW		5.1	9.5	mA	V_{CC} = MAX., V_{IN} = 5.0 V	27

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type. Expander inputs X and $\overline{X}$ are open.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.
(4) Required at both input terminals of one AND section to ensure LOW level at output.
(5) Required at one input terminal of each AND section to ensure HIGH level at output.

ELECTRICAL CHARACTERISTICS 9N53/5453 CIRCUITS, Using Expander Inputs, V_{CC} = 4.5 V, T_A = 55°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
I_X	Expander Current			2.9	mA	V_1 = 0.4 V, I_{OL} = 16 mA	28
$V_{BE(Q)}$	Base-Emitter Voltage of Output Transistor Q			1.0	Volts	I_{OL} = 16 mA, I_1 = 0.41 mA, R_1 = 0Ω	29
V_{OH}	Output HIGH Voltage	2.4	3.3		Volts	I_{OH} = –400 μA, I_1 = 0.15 mA, I_2 = –0.15 mA	30
V_{OL}	Output LOW Voltage		0.22	0.4	Volts	I_{OL} = 16 mA, I_1 = 0.3 mA, R_1 = 138Ω	29

ELECTRICAL CHARACTERISTICS 9N53/7453 CIRCUITS, Using Expander Inputs, V_{CC} = 4.75 V, T_A = 0°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
I_X	Expander Current			3.1	mA	V_1 = 0.4 V, I_{OL} = 16 mA	28
$V_{BE(Q)}$	Base-Emitter Voltage of Output Transistor Q			1.0	Volts	I_{OL} = 16 mA, I_1 = 0.62 mA, R_1 = 0Ω	29
V_{OH}	Output HIGH Voltage	2.4	3.3		Volts	I_{OH} = –400 μA, I_1 = 270 μA, I_2 = –270 μA	30
V_{OL}	Output LOW Voltage		0.22	0.4	Volts	I_{OL} = 16 mA, I_1 = 0.43 mA, R_1 = 130Ω	29

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		13	22	ns	V_{CC} = 5.0 V C_L = 15 pF R_L = 400Ω	A
t_{PHL}	Turn On Delay Input to Output		8.0	15	ns		

LPTTL/SSI 9L54

LOW POWER AND-OR-INVERT GATE

DESCRIPTION — The Low Power TTL/SSI 9L54 is a four wide, 2-2-2-3-input AND-OR-INVERT Gate. It is designed for low power and medium speed operation.

- **TYPICAL POWER DISSIPATION OF 10 mW**
- **TYPICAL DELAY OF 25 ns**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **HIGH CAPACITIVE DRIVE CAPABILITY**
- **TTL COMPATIBLE**
- **ALL CERAMIC "HERMETIC" PACKAGES**

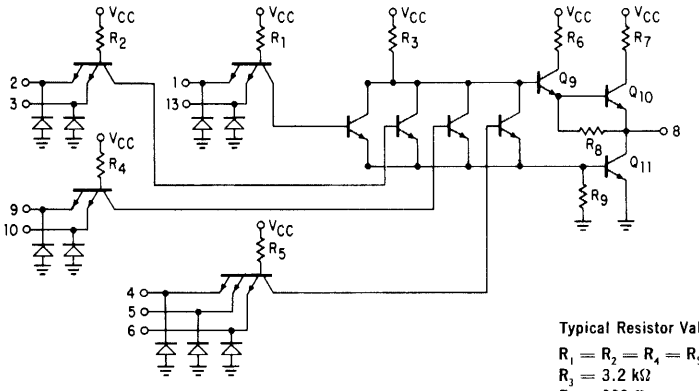
PIN NAMES

INPUTS (Pins 1, 2, 3, 4, 5, 6, 9, 10, 13)
OUTPUT (Pin 8)

LOADING	
HIGH	LOW
0.75 U.L.	0.38 U.L.
10 U.L.	2.5 U.L.

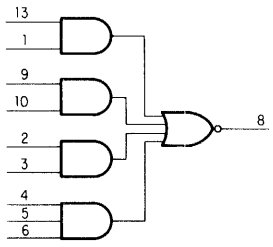
1 Unit Load (U.L.) = 40μA HIGH/1.6 mA LOW.

SCHEMATIC DIAGRAM



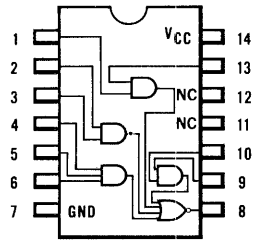
Typical Resistor Values
$R_1 = R_2 = R_4 = R_5 = 10.4\ k\Omega$
$R_3 = 3.2\ k\Omega$
$R_6 = 600\ \Omega$
$R_7 = 320\ \Omega$
$R_8 = 16\ k\Omega$
$R_9 = 2.66\ \Omega$

LOGIC SYMBOL

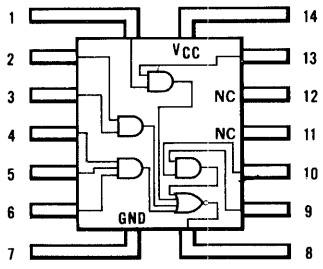


V_{CC} = Pin 14
Gnd = Pin 7

CONNECTION DIAGRAMS
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



NC = No Internal Connection

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
9L54XM	4.5V	5.0V	5.5V	−55°C to 125°C
9L54XC	4.75V	5.0V	5.25V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted) (See Notes 1 & 2)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP. (Note 3)	MAX.		
V_{OH}	Output HIGH Voltage	2.4	3.3		Volts	V_{CC} = MIN., I_{OH} = -0.4 mA, V_{IN} = V_{IL}
V_{OL}	Output LOW Voltage		0.1	0.3	Volts	V_{CC} = MIN., I_{OL} = 4.0 mA, V_{IN} = V_{IH}
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed input logical HIGH voltage for all inputs
V_{IL}	Input LOW Voltage			0.7	Volts	Guaranteed input logical LOW voltage for all inputs
I_{IL}	Input LOW Current		−0.38	−0.6	mA	V_{CC} = MAX., V_{IN} = 0.3 V
I_{IH}	Input HIGH Current		3.0	30	μA	V_{CC} = MAX., V_{IN} = 2.4 V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{SC} (Note 4)	Output Short Circuit Current	−10	−22	−40	mA	V_{CC} = MAX., V_{OUT} = 0.0 V Inputs grounded.
I_{CC}	Power Supply Current		2.6	3.7	mA	V_{CC} = MAX., Inputs HIGH
			1.6	2.7	mA	V_{CC} = MAX., Inputs LOW
t_{PLH}	Turn Off Delay		28		ns	V_{CC} = 5.0 V, See Fig. 1
t_{PHL}	Turn On Delay		22		ns	C_L = 15 pF

NOTES:

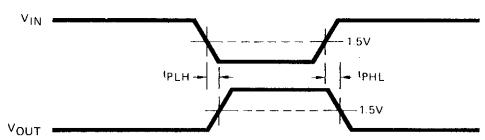
(1) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.

(2) The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

(3) Typical limits are at V_{CC}= 5.0V, 25°C, and max. loading.

(4) Not more than one output should be shorted at a time.

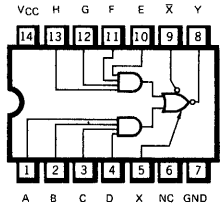
Fig. 1 SWITCHING TIME WAVEFORM



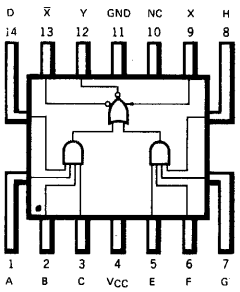
EXPANDABLE 4-INPUT AND-OR-INVERT GATE

LOGIC AND CONNECTION DIAGRAM

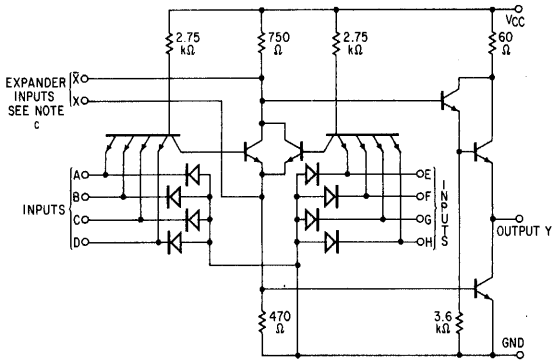
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



SCHEMATIC DIAGRAM



Positive logic: $Y = \overline{(ABCD) + (EFGH) + (X)}$
X = Output of 9H60/54H60, 74H60 or 9H62/54H62, 74H62.

NOTES:
(a) Component values shown are typical.
(b) Both expander inputs are used simultaneously for expanding.
(c) If expander is not used leave X and $\overline{X}$ pins open.
(d) A total of four 9H60/54H60, 74H60 expander gates or one 9H62/54H62, 74H62 expander gate may be connected to the expander inputs.
(e) NC — No internal connection.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9H55XM/54H55XM			9H55XC/74H55XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	70	°C
Input Loading for Each Input			1.25			1.25	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage (Note 4)	2.0			Volts	Guaranteed Input HIGH Voltage		21
V_{IL}	Input LOW Voltage (Note 5)			0.8	Volts	Guaranteed Input LOW Voltage		22
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = –0.5 mA, V_{IN} = 0.8 V		22
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 20 mA, V_{IN} = 2.0 V		21
I_{IH}	Input HIGH Current			50	μA	V_{CC} = MAX., V_{IN} = 2.4 V	Each Input	24
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current			–2.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V, Each Input		23
I_{OS}	Output Short Circuit Current (Note 3)	–40		–100	mA	V_{CC} = MAX.		25
I_{CCH}	Supply Current HIGH		4.5	6.4	mA	V_{CC} = MAX., V_{IN} = 0 V		27
I_{CCL}	Supply Current LOW		7.5	12	mA	V_{CC} = MAX., V_{IN} = 4.5 V		26

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type. Expander pins are open.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Duration of short-circuit test should not exceed 1 second.
(4) Required at all input terminals of either AND section to ensure LOW level at output.
(5) Required at one input terminal of each AND section to ensure HIGH level at output.

ELECTRICAL CHARACTERISTICS (9H55/54H55 Circuits Only) Using Expander Inputs, V_{CC} = 4.5 V, T_A = −55°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
$I_{IN\overline{X}}$	Expander-Node Input Current			−5.85	mA	$V_{\overline{X}}$ = 1.4 V	104
$V_{BE(Q)}$	Base-Emitter Voltage of Output Transistor Q			1.0	Volts	I_{OL} = 20 mA, I_1 = 700 μA, R_1 = 0Ω	29
V_{OH}	Output HIGH Voltage	2.4			Volts	I_{OH} = −500 μA, I_1 = 320 μA, I_2 = −320 μA	30
V_{OL}	Output LOW Voltage			0.4	Volts	I_{OL} = 20 mA, I_1 = 470 μA, R_1 = 68Ω	29

ELECTRICAL CHARACTERISTICS (9H55/74H55 Circuits Only) Using Expander Inputs, V_{CC} = 4.75 V, T_A = 0°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
$I_{IN\overline{X}}$	Expander-Node Input Current			−6.3	mA	$V_{\overline{X}}$ = 1.4 V	104
$V_{BE(Q)}$	Base-Emitter Voltage of Output Transistor Q			1.0	Volts	I_{OL} = 20 mA, I_1 = 1.1 mA, R_1 = 0Ω	29
V_{OH}	Output HIGH Voltage	2.4			Volts	I_{OH} = −500 μA, I_1 = 570 μA, I_2 = −570 μA	30
V_{OL}	Output LOW Voltage			0.4	Volts	I_{OL} = 20 mA, I_1 = 600 μA, R_1 = 63Ω	29

SWITCHING CHARACTERISTICS, Expander Pins are Open (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		7.0	11	ns	V_{CC} = 5.0 V C_L = 25 pF R_L = 280Ω	T
t_{PHL}	Turn On Delay Input to Output		6.5	11	ns		

SWITCHING CHARACTERISTICS (T_A = 25°C)

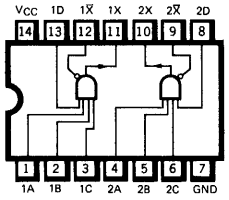
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		11.4		ns	V_{CC} = 5.0 V C_L = 25 pF R_L = 280Ω *C_X = 15 pF	U *MM & NN
t_{PHL}	Turn On Delay Input to Output		7.7		ns		

5

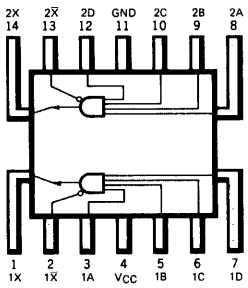
DUAL 4-INPUT EXPANDER

LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)

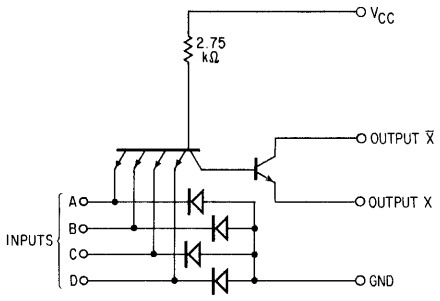


FLATPAK (TOP VIEW)



Positive logic: X = ABCD when connected to X and $\overline{X}$ pins of 9H50/54H50, 74H50; 9H53/54H53, 74H53 or 9H55/54H55, 74H55 circuit.

SCHEMATIC DIAGRAM (EACH EXPANDER)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9H60XM/54H60XM			9H60XC/74H60XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	70	°C
Maximum number of expanders that may be fanned in to one expandable AND OR Invert Gate			4			4	

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP. (Note 2)	LIMITS MAX.	UNITS	TEST CONDITIONS (Note 1)	TEST FIGURE
V_{IH}	Input HIGH Voltage	2.0			Volts	(Note 3)	31
V_{IL}	Input LOW Voltage			0.8	Volts	(Note 4)	32
V_{ON}	On-State Output Voltage			0.4	Volts	V_{CC} = MIN., V_{IN} = 2.0 V, V_1 = 1.0 V; T_A = –55°C, I_{ON} = 5.85 mA; T_A = 0°C I_{ON} = 6.3 mA	31
				0.4	Volts	V_{CC} = MAX., V_{IN} = 2.0 V, V_1 = 0.6 V; T_A = 125°C, I_{ON} = 7.85 mA; T_A = 70°C, I_{ON} = 7.4 mA	
I_{OFF}	Off-State Output Current			320	μA	T_A = –55°C; V_{CC} = MIN., V_{IN} = 0.8 V; V_1 = 4.5 V, R = 575Ω	32
				570	μA	T_A = 0°C	
I_{ON}	On-State Output Current	–470			μA	T_A = –55°C; V_{CC} = MIN., V_{IN} = 2.0 V; V_1 = 1.0 V	33
		–600			μA	T_A = 0°C	
I_{IH}	Input HIGH Current			50	μA	V_{CC} = MAX., V_{IN} = 2.4 V; Each Input	34
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IL}	Input LOW Current			–2.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V, Each Input	32
$I_{CC(ON)}$	On-State Supply Current		1.9	3.5	mA	V_{CC} = MAX., V_{IN} = 4.5 V, V_1 = 0.85 V	35
$I_{CC(OFF)}$	Off-State Supply Current		3.0	4.5	mA	V_{CC} = MAX., V_{IN} = 0 V, V_1 = 0.85 V	35

OUTPUT CAPACITANCE, V_{CC} AND GND TERMINALS OPEN (T_A = 25°C)

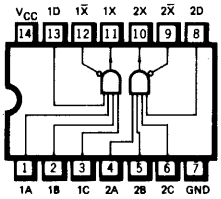
SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS	TEST FIGURE
$C_{\overline{X}}$	Effective Capacitance of Output Transistor Q_1		1.3		pF	f = 1 MHz	BB

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Required at all input terminals to ensure output is in the on state.
(4) Required at any input terminal to ensure output is in the off state.

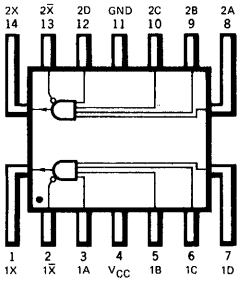
DUAL 4-INPUT EXPANDER

LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)

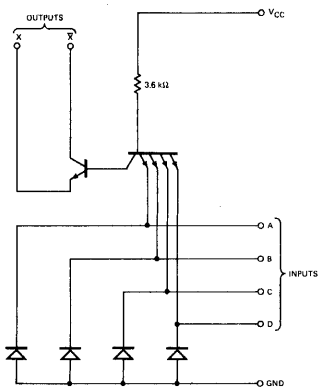


FLATPAK (TOP VIEW)



Positive logic: X = ABCD when connected to X and $\overline{X}$ pins of 9N50/5450, 7450; 9N53/5453, 7453 circuit.

SCHEMATIC DIAGRAM (EACH EXPANDER)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9N60XM/5460XM			9N60XC/7460XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	70	°C
Maximum number of expanders that may be fanned-in to one expandable AND OR Invert Gate			4			4	

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP. (Note 2)	LIMITS MAX.	UNITS	TEST CONDITIONS (Note 1)	TEST FIGURE
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage	31
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage	32
V_{ON}	On-State Output Voltage			0.4	Volts	V_{CC} = MIN., V_{IN} = 2.0 V; V_1 = 1.0 V, R = 1.1 kΩ; T_A = –55°C; T_A = 0°C	31
I_{OFF}	Off-State Output Current			150	μA	T_A = –55°C; V_{CC} = MIN., V_{IN} = 0.8 V	32
				270	μA	T_A = 0°C; V_1 = 4.5 V, R = 1.2 kΩ	
I_{ON}	On-State Output Current	–0.3			mA	T_A = –55°C, V_{CC} = MIN., V_{IN} = 2.0 V, V_1 = 1.0 V	33
		–0.43			mA	V_{CC} = 4.75 V, V_{IN} = 2.0 V, V_1 = 1.0 V	
I_{IH}	Input HIGH Current			40	μA	V_{CC} = MAX., V_{IN} = 2.4 V; Each Input	34
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IL}	Input LOW Current			–1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V, Each Input	32
$I_{CC\ (on)}$	On-State Supply Current		1.2	2.5	mA	V_{CC} = MAX., V_{IN} = 5.0 V, V_1 = 0.85 V	35
$I_{CC\ (off)}$	Off-State Supply Current		2.0	4.0	mA	V_{CC} = MAX., V_{IN} = 0 V, V_1 = 0.85 V	35

SWITCHING CHARACTERISTICS (T_A = 25°C)

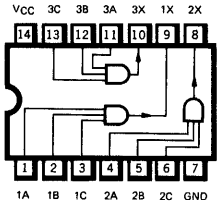
SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS	TEST FIGURE
t_{PLH}	*Turn Off Delay Input to Output		15	30	ns	V_{CC} = 5.0 V; C_L = 15 pF; R_L = 400Ω	B
t_{PHL}	*Turn On Delay Input to Output		10	20	ns		

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
*Through 9N50/5450, 7450; 9N53/5453, 7453.

TRIPLE 3-INPUT EXPANDER

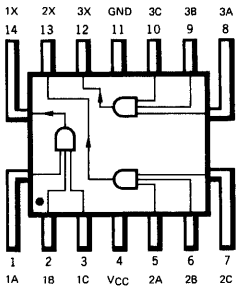
LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)

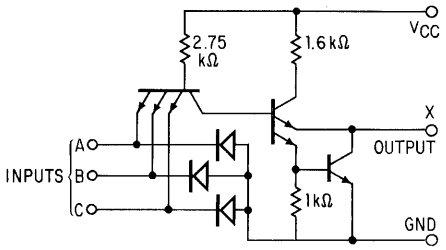


Positive logic: X = ABC

FLATPAK (TOP VIEW)



SCHEMATIC DIAGRAM
(EACH EXPANDER)



Component values shown are typical.

When connected to the X input of the 9H52/54H52, 74H52 circuit.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9H61XM/54H61XM			9H61XC/74H61XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	70	°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	(Note 3)	114
V_{IL}	Input LOW Voltage			0.8	Volts	(Note 4)	113
V_{ON}	On-State Output Voltage			1.0	Volts	V_{CC} = MIN., V_{IH} = 2 V T_A = –55°C, I_{ON} = 4.5 mA T_A = 0°C, I_{ON} = 5.35 mA	114
I_{OFF}	Off-State Output Current			50	μA	V_{CC} = MIN., V_{IL} = 0.8 V V_{OFF} = 2.2 V, T_A = MAX.	113
I_{IH}	Input HIGH Current			50	μA	V_{CC} = MAX., V_{IN} = 2.4 V	78
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	78
I_{IL}	Input LOW Current			–2.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V, Each Input	79
$I_{CC(ON)}$	On-State Supply Current		11	16	mA	V_{CC} = MAX., V_{IN} = 4.5 V	81
$I_{CC(OFF)}$	Off-State Supply Current		5.0	7.0	mA	V_{CC} = MAX., V_{IN} = 0 V	81

OUTPUT CAPACITANCE, V_{CC} AND GND TERMINALS OPEN (T_A = 25°C)

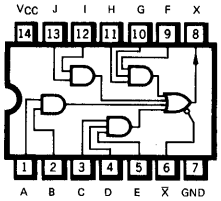
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
C_X	Effective Capacitance of Output Transistor Q_1		1.3		pF	f = 1 MHz	CC

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Required at all input terminals to ensure output is in the on state.
(4) Required at any input terminal to ensure output is in the off state.

3-2-2-3-INPUT AND-OR EXPANDER

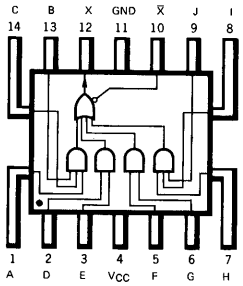
LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)



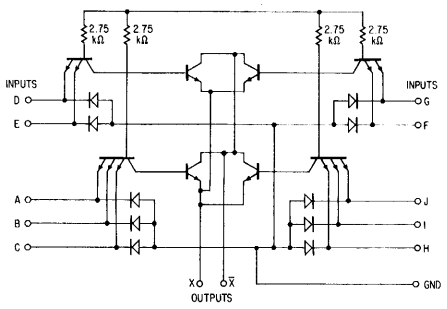
Positive logic:
$X = (AB) + (CDE) + (FGH) + (IJ)$

FLATPAK (TOP VIEW)



Positive logic:
$X = (ABC) + (DE) + (FG) + (HIJ)$

SCHEMATIC DIAGRAM



Component values shown are typical.

When connected to X and $\overline{X}$ pins of 9H50/54H50, 74H50; 9H53/54H53, 74H53 or 9H55/54H55, 74H55 circuit.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9H62XM/54H62XM			9H62XC/74H62XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	70	°C
Maximum number of expanders that may be fanned in to one expandable AND OR Invert Gate			1			1	

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP. (Note 2)	LIMITS MAX.	UNITS	TEST CONDITIONS (Note 1)	TEST FIGURE
V_{IH}	Input HIGH Voltage	2.0			Volts	(Note 3)	115
V_{IL}	Input LOW Voltage			0.8	Volts	(Note 4)	116
V_{ON}	On-State Output Voltage			0.4	Volts	V_{CC} = MIN., V_{IN} = 2.0 V, V_1 = 1.0 V; T_A = −55°C, I_{ON} = 5.85 mA; T_A = 0°C, I_{ON} = 6.3 mA	115
				0.4	Volts	V_{CC} = MAX., V_{IN} = 2.0 V, V_1 = 0.6 V; T_A = 125°C, I_{ON} = 7.85 mA; T_A = 70°C, I_{ON} = 7.4 mA	
I_{OFF}	Off-State Output Current			320	µA	T_A = −55°C; V_{CC} = MIN., V_{IN} = 0.8 V	116
				570	µA	T_A = 0°C; V_1 = 4.5 V, R = 575Ω	
I_{ON}	On-State Output Current	−470			µA	T_A = −55°C; V_{CC} = MIN., V_{IN} = 2.0 V	117
		−600			µA	T_A = 0°C; V_1 = 1.0 V	
I_{IH}	Input HIGH Current			50	µA	V_{CC} = MAX., V_{IN} = 2.4 V; Each Input	119
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IL}	Input LOW Current			−2.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V, Each Input	118
$I_{CC(ON)}$	On-State Supply Current		3.8	7.0	mA	V_{CC} = MAX., V_{IN} = 4.5 V, V_1 = 0.85 V	120
$I_{CC(OFF)}$	Off-State Supply Current		6.0	9.0	mA	V_{CC} = MAX., V_{IN} = 0 V, V_1 = 0.85 V	120

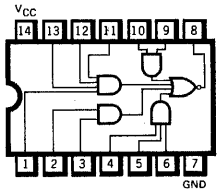
OUTPUT CAPACITANCE, V_{CC} AND GND TERMINALS OPEN (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS	TEST FIGURE
$C_{\overline{X}}$	Effective Capacitance of Output Transistor Q_1		1.3		pF	f = 1 MHz	BB

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Required at all input terminals of one AND section to ensure output is in the on state.
(4) Required at one input terminal of each AND section to ensure output is in the off state.

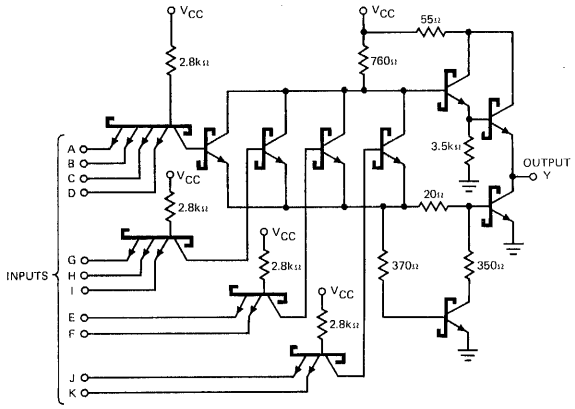
4-2-3-2-INPUT AND-OR-INVERT GATE

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



Positive logic: $\overline{ABCD + EF + GHE + JK}$

SCHEMATIC DIAGRAM



All inputs have Schottky clamp diodes.
Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9S64XM/54S64XM			9S64XC/74S64XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	75	°C
Input Loading for Each Input			1.25			1.25	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER		LIMITS MIN.	LIMITS TYP. (Note 2)	LIMITS MAX.	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			Volts	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage				0.8	Volts	Guaranteed Input LOW Voltage
V_{CD}	Input Clamp Diode Voltage			–0.65	–1.2	Volts	V_{CC} = MIN., I_{IN} = –18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		Volts	V_{CC} = MIN., I_{OH} = –1.0 mA, V_{IN} = 0.8 V
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage			0.35	0.5	Volts	V_{CC} = MIN., I_{OL} = 20 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	50	μA	V_{CC} = MAX., V_{IN} = 2.7 V
					1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{IL}	Input LOW Current			–1.4	–2.0	mA	V_{CC} = MAX., V_{IN} = 0.5 V
I_{OS}	Output Short Circuit Current (Note 3)		–40	–65	–100	mA	V_{CC} = MAX., V_{OUT} = 0V
I_{CCH}	Supply Current HIGH			7.0	12.5	mA	V_{CC} = MAX., V_{IN} = 0 V
I_{CCL}	Supply Current LOW			8.5	16	mA	V_{CC} = MAX., (Note 4)

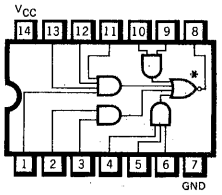
SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS	TEST FIGURES
t_{PLH}	Turn Off Delay Input to Output	2.0	3.5	5.5	ns	V_{CC} = 5.0 V, C_L = 15 pF	FF
t_{PHL}	Turn On Delay Input to Output	2.0	3.5	5.5	ns		

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.
(4) I_{CCL} is measured with all inputs of one gate open, and remaining inputs grounded.

4-2-3-2-INPUT AND-OR-INVERT GATE (WITH OPEN COLLECTOR)

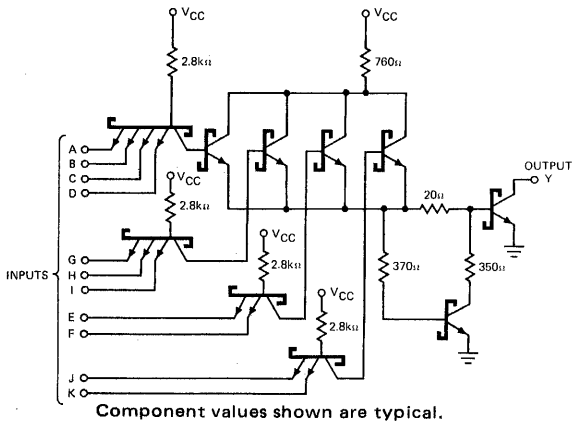
LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



*OPEN COLLECTOR

Positive logic: $\overline{ABCD + EF + GHI + JK}$

SCHEMATIC DIAGRAM



Component values shown are typical.
All inputs have clamp diodes (not shown).

RECOMMENDED OPERATING CONDITIONS

PARAMETER	† 9S65XM/54S65XM			9S65XC/74S65XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	75	°C
Input Loading for Each Input			1.25			1.25	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)
		MIN.	TYP. (Note 2)	MAX.		
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage
V_{CD}	Input Clamp Diode Voltage			–1.2	Volts	V_{CC} = MIN., I_{IN} = –18 mA
I_{OH}	Output HIGH Current		0.1	250	μA	V_{CC} = MIN., V_{OH} = 5.5 V, V_{IN} = 0.8 V
V_{OL}	Output LOW Voltage		0.35	0.5	Volts	V_{CC} = MIN., I_{OL} = 20 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current		1.0	50	μA	V_{CC} = MAX., V_{IN} = 2.7 V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{IL}	Input LOW Current		–1.4	–2.0	mA	V_{CC} = MAX., V_{IN} = 0.5 V
I_{CCH}	Supply Current HIGH		6.0	11.0	mA	V_{CC} = MAX., V_{IN} = 0 V
I_{CCL}	Supply Current LOW		8.5	16	mA	V_{CC} = MAX., (Note 3)

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURES
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output	2.0	5.0	7.5	ns	V_{CC} = 5.0 V, C_L = 15 pF	FF
t_{PHL}	Turn On Delay Input to Output	2.0	5.5	8.5	ns		

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) I_{CCL} is measured with all inputs of one gate open, and remaining inputs grounded.

† To be announced 1972

EDGE TRIGGERED JK FLIP-FLOP

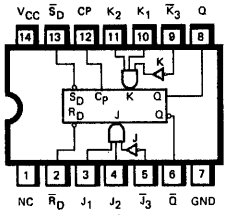
DESCRIPTION – The 9N70/5470, 7470 is a gated input edge triggered JK flip-flop offering direct clear and preset inputs, and complementary Q and $\overline{Q}$ outputs. Information at the J and K inputs is transferred to the outputs on the positive edge of the clock pulse.

Direct-coupled clock triggering occurs at a specific voltage level of the clock pulse, when the clock input threshold voltage has been passed, the gated inputs are locked out.

These flip-flops are designed for medium to high speed applications and offer a significant saving in system power dissipation and package count where input gating is required.

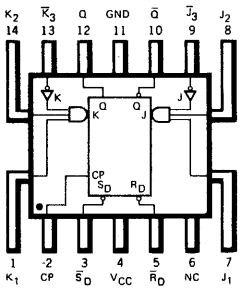
LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)

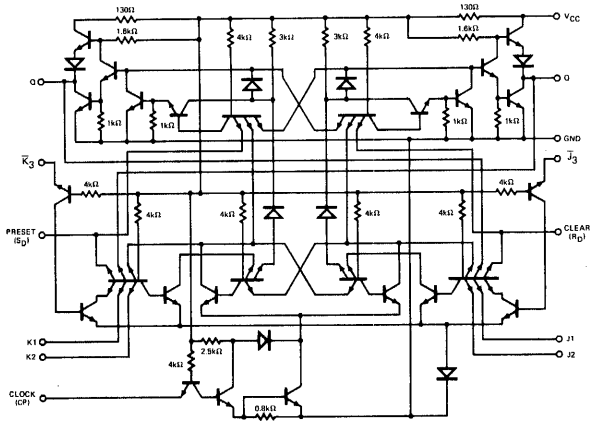


NC – No internal connection.

FLATPAK (TOP VIEW)



SCHEMATIC DIAGRAM



Component values shown are typical.

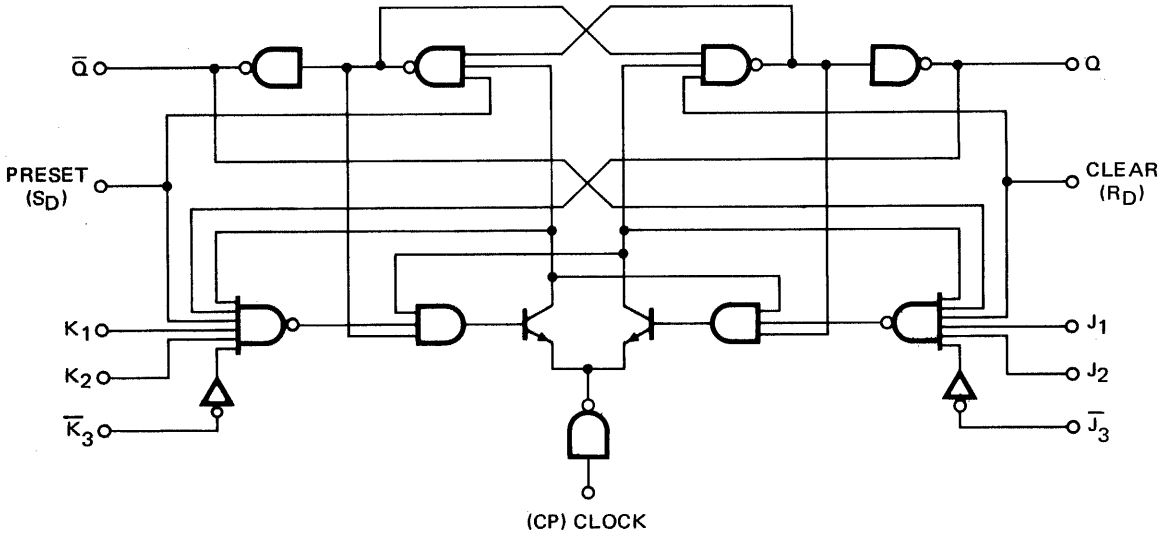
Positive logic:
LOW input to preset sets Q to HIGH level
LOW input to clear sets Q to LOW level
Preset or clear function can occur only when clock input is LOW

TRUTH TABLE

t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

NOTES:
$J = J1 \cdot J2 \cdot \overline{J3}$
$K = K1 \cdot K2 \cdot \overline{K3}$
t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.
If inputs $\overline{J3}$ or $\overline{K3}$ are not used they must be grounded.

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

PARAMETER	9N70XM/5470XM			9N70XC/7470XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	70	°C
Normalized Fan Out from Each Output, N			10			10	U.L.
Clock Pulse Transition Time to HIGH Level, $t_{1(clock)}$ (See Fig. D)	5.0		150	5.0		150	ns
Width of Clock Pulse, $t_{p(clock)}$ (See Fig. D)	20			20			ns
Width of Preset Pulse, $t_{p(preset)}$ (See Fig. C)	25			25			ns
Width of Clear Pulse, $t_{p(clear)}$ (See Fig. C)	25			25			ns

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH	36 & 37
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW	36 & 37
V_{OH}	Output HIGH Voltae	2.4	3.5		Volts	V_{CC} = MIN., I_{OH} = –0.4 mA	36
V_{OL}	Output LOW Voltage		0.22	0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA	37
I_{IH}	Input HIGH Current at J_1, J_2, $\overline{J}_3$, K_1, K_2, $\overline{K}_3$ or Clock			40	µA	V_{CC} = MAX., V_{IN} = 2.4 V	39
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
	Input HIGH Current at Clear or Preset			80	µA	V_{CC} = MAX., V_{IN} = 2.4 V	39
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IL}	Input LOW Current at J_1, J_2, $\overline{J}_3$, K_1, K_2, $\overline{K}_3$ or Clock			–1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V	38
	Input LOW Current at Clear or Preset			–3.2	mA	V_{CC} = MAX., V_{IN} = 0.4 V	38
I_{OS}	Output Short Circuit Current (Note 3)	–20		–57	mA	9N70/5470 V_{CC} = MAX.	40
		–18		–57	mA	9N70/7470 V_{IN} = 0 V	
I_{CC}	Supply Current		13	26	mA	V_{CC} = MAX., V_{IN} = 5.0 V	39

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
f_{max}	Maximum Clock Frequency	20	35		MHz	V_{CC} = 5.0 V, C_L = 15 pF, R_L = 400Ω	D
t_{setup}	Maximum Input Setup Time		10	20	ns		D
t_{hold}	Maximum Input Hold Time		0	5.0	ns		D
t_{PLH}	Turn Off Delay Clear or Preset to Output			50	ns		C
t_{PHL}	Turn On Delay Clear or Preset to Output			50	ns		C
t_{PLH}	Turn Off Delay Clock to Output	10	27	50	ns		D
t_{PHL}	Turn On Delay Clock to Output	10	18	50	ns		D

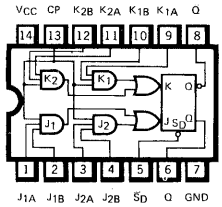
NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.

JK MASTER/SLAVE FLIP-FLOP WITH AND-OR INPUTS

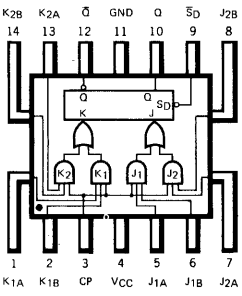
DESCRIPTION – The HSTTL/SSI 9H71/54H71, 74H71 is a High Speed JK Master/Slave flip-flop with AND-OR gate inputs. The AND-OR gate inputs for entry into the master section are controlled by the clock pulse. The clock pulse also regulates the circuitry which connects the master and slave sections. The sequence of operation is as follows: 1) Isolate slave from master. 2) Enter information from AND-OR gate inputs to master. 3) Disable AND-OR gate inputs. 4) Transfer information from master to slave. Logic state of J and K inputs must not be allowed to change when the clock pulse is in a HIGH state.

LOGIC AND CONNECTION DIAGRAM

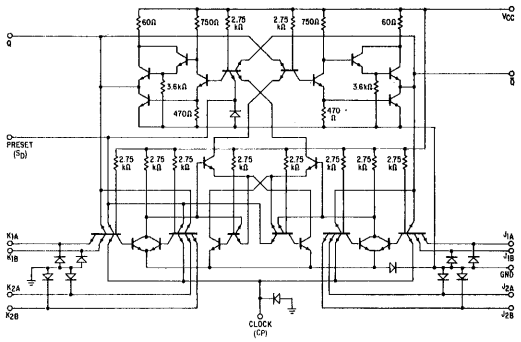
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



SCHEMATIC DIAGRAM



Component values shown are typical.

Positive logic:

LOW input to preset sets Q to HIGH level

Preset is independent of clock

TRUTH TABLE

t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

NOTES:

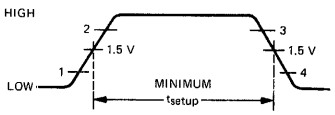
J = (J1A·J1B)+(J2A·J2B)

K = (K1A·K1B)+(K2A·K2B)

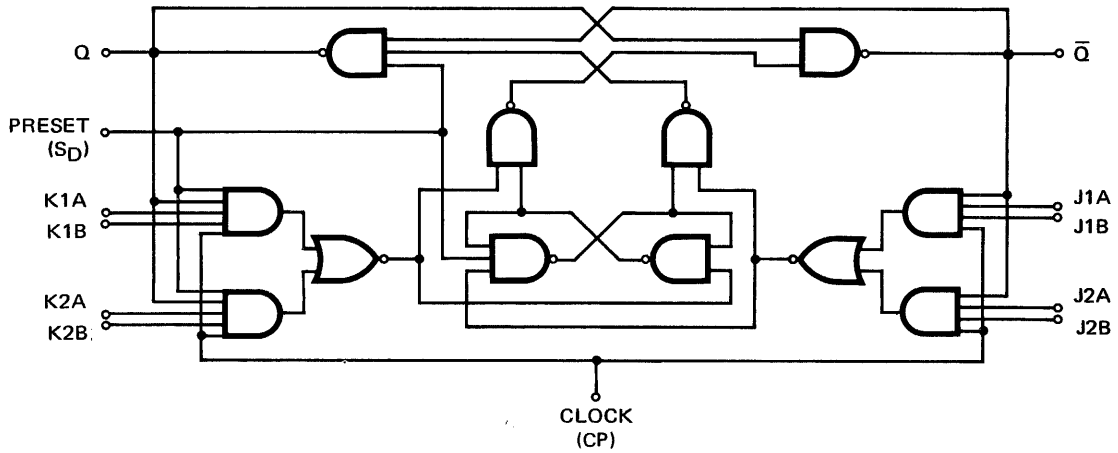
t_n = Bit time before clock pulse

t_{n+1} = Bit time after clock pulse

CLOCK WAVEFORM



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

PARAMETER	9H71XM/54H71XM			9H71XC/74H71XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	70	°C
Fan Out from Each Output			12.5			12.5	U.L.
Width of Clock Pulse, $t_{p(clock)}$ (See Fig. W)	12			12			ns
Width of Preset Pulse, $t_{p(preset)}$ (See Fig. X)	16			16			ns
Input Setup Time, t_{setup} (See Clock Waveform)	$\geq t_{p(clock)}$			$\geq t_{p(clock)}$			
Input Hold Time, t_{hold}	0			0			

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH	121 & 122
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW	121 & 122
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = –0.5 mA	121
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 20 mA	122
I_{IH}	Input HIGH Current at J1A, J1B, J2A, J2B, K1A, K1B, K2A, or K2B			50	µA	V_{CC} = MAX., V_{IN} = 2.4 V	124
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
	Input HIGH Current at Preset			150	µA	V_{CC} = MAX., V_{IN} = 2.4 V	124
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
	Input HIGH Current at Clock			100	µA	V_{CC} = MAX., V_{IN} = 2.4 V	124
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IL}	Input LOW Current at J1A, J1B, J2A, J2B, K1A, K1B, K2A, or K2B			–2.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V	123
	Input LOW Current at Preset			–6.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V	123
	Input LOW Current at Clock			–4.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V	123
I_{OS}	Output Short Circuit Current (Note 3)	–40		–100	mA	V_{CC} = MAX., V_{IN} = 0 V	127
I_{CC}	Supply Current		19	30	mA	V_{CC} = MAX.	124

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
f_{CLOCK}	Maximum Clock Frequency	25	30		MHz	V_{CC} = 5.0 V C_L = 25 pF R_L = 280Ω	W
t_{PLH}	Turn Off Delay Preset to Output		6.0	13	ns		X
t_{PHL}	Turn On Delay Preset to Output		12	24	ns		X
t_{PLH}	Turn Off Delay Clock to Output	6.0	14	21	ns		W
t_{PHL}	Turn On Delay Clock to Output	10	22	27	ns		W

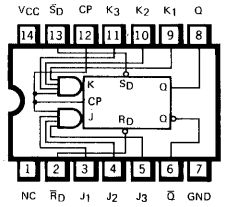
NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

JK MASTER/SLAVE FLIP-FLOP WITH AND INPUTS

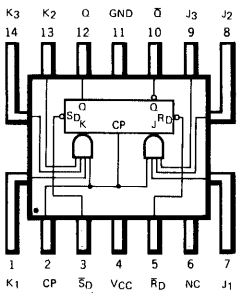
DESCRIPTION – The HSTTL/SSI 9H72/54H72, 74H72 is a High Speed JK Master/Slave flip-flop with AND gate inputs. The AND gate inputs for entry into the master section are controlled by the clock pulse. The clock pulse also regulates the circuitry which connects the master and slave sections. The sequence of operation is as follows: 1) Isolate slave from master. 2) Enter information from AND gate inputs to master. 3) Disable AND gate inputs. 4) Transfer information from master to slave. Logic state of J and K inputs must not be allowed to change when the clock pulse is in a HIGH state.

LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)



FLATPAK (TOP VIEW)



NC – No internal connection.

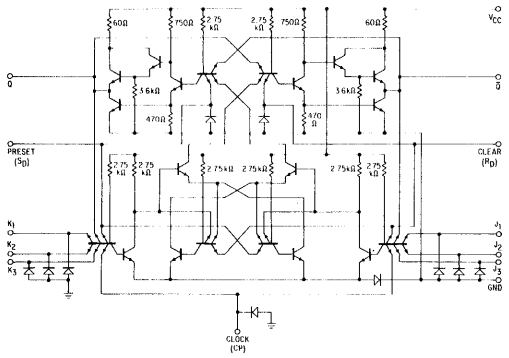
Positive logic:

LOW input to preset sets Q to HIGH level

LOW input to clear sets Q to LOW level

Preset and clear are independent of clock

SCHEMATIC DIAGRAM



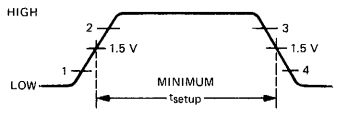
Component values shown are typical.

TRUTH TABLE

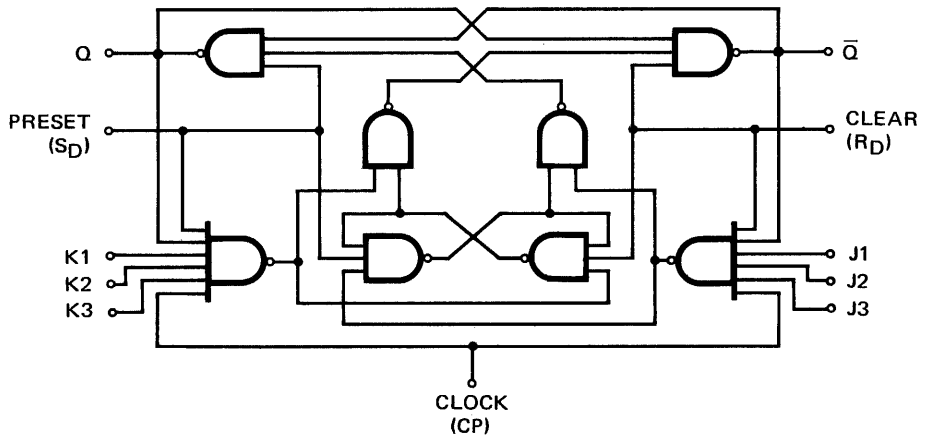
t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

NOTES:
J = J1·J2·J3
K = K1·K2·K3
t_n = Bit time before clock pulse
t_{n+1} = Bit time after clock pulse

CLOCK WAVEFORM



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

PARAMETER	9H72XM/54H72XM			9H72XC/74H72XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	70	°C
Fan Out from Each Output			12.5			12.5	U.L.
Width of Clock Pulse, $t_{p(clock)}$ (See Fig. W)	12			12			ns
Width of Preset Pulse, $t_{p(preset)}$ (See Fig. X)	16			16			ns
Width of Clear Pulse, $t_{p(clear)}$ (See Fig. X)	16			16			ns
Input Setup Time, t_{setup} (See Clock Waveform)	$\geq t_{p(clock)}$			$\geq t_{p(clock)}$			
Input Hold Time, t_{hold}	0			0			

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH	41 & 42
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW	41 & 42
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = −0.5 mA	41
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 20 mA	42
I_{IH}	Input HIGH Current at J2, J3, K1, K2, or K3			50	µA	V_{CC} = MAX., V_{IN} = 2.4 V	44
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
	Input HIGH Current at J1,			50	µA	V_{CC} = MAX., V_{IN} = 2.4 V	44
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
	Input HIGH Current at Clock Preset or Clear			100	µA	V_{CC} = MAX., V_{IN} = 2.4 V	44
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IL}	Input LOW Current at J1, J2, J3, K1, K2, K3, or Clock			−2.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V	43
	Input LOW Current at Preset or Clear			−4.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V	43
I_{OS}	Output Short Circuit Current (Note 3)	−40		−100	mA	V_{CC} = MAX., V_{IN} = 0 V	45
I_{CC}	Supply Current		16	25	mA	V_{CC} = MAX.	44

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
f_{CLOCK}	Maximum Clock Frequency	25	30		MHz	V_{CC} = 5.0 V C_L = 25 pF R_L = 280Ω	W
t_{PLH}	Turn Off Delay Clear or Preset to Output		6.0	13	ns		X
t_{PHL}	Turn On Delay Clear or Preset to Output		12	24	ns		X
t_{PLH}	Turn Off Delay Clock to Output	6.0	14	21	ns		W
t_{PHL}	Turn On Delay Clock to Output	10	22	27	ns		W

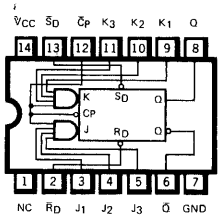
NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Note more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

JK MASTER/SLAVE FLIP-FLOP WITH AND INPUTS

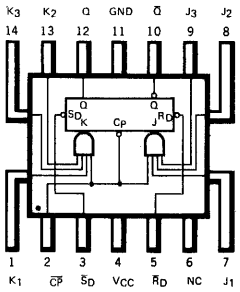
DESCRIPTION – The TTL/SSI 9N72/5472, 7472 is a JK Master/Slave flip-flop with AND gate inputs. The AND gate inputs for entry into the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows: 1) Isolate slave from master. 2) Enter information from AND gate inputs to master. 3) Disable AND gate inputs. 4) Transfer information from master to slave.

LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)



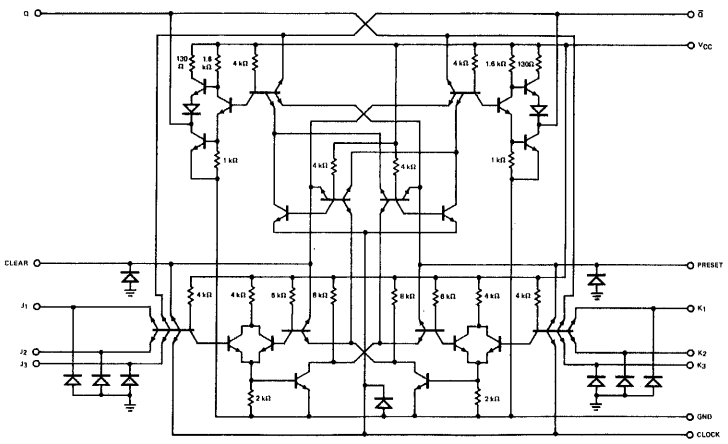
FLATPAK (TOP VIEW)



NC – No internal connection.

Positive logic:
LOW input to preset sets Q to HIGH level
LOW input to clear sets Q to LOW level
Preset and clear are independent of clock

SCHEMATIC DIAGRAM



Component values shown are typical.

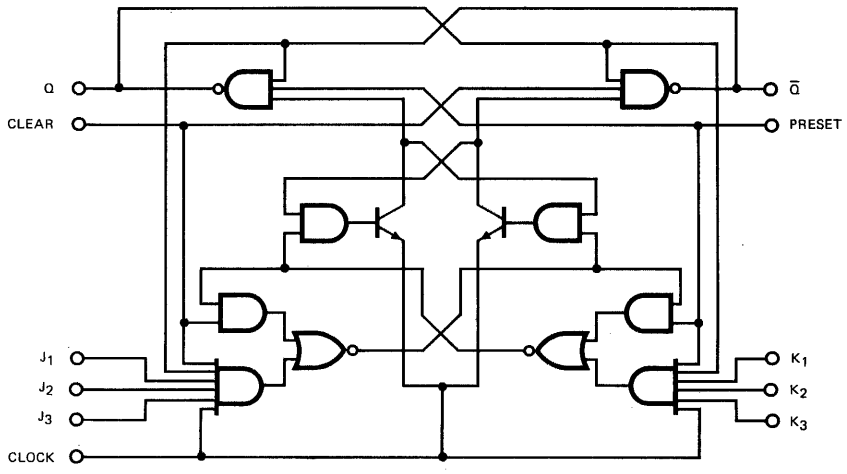
TRUTH TABLE

t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\bar{Q}_n$

NOTES:
J = J1 · J2 · J3
K = K1 · K2 · K3
t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.

CLOCK WAVEFORM

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

PARAMETER	9N72XM/5472XM			9N72XC/7472XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	70	°C
Normalized Fan Out from Each Output, N			10			10	U.L.
Width of Clock Pulse, $t_{p(clock)}$ (See Fig. E)	20			20			ns
Width of Preset Pulse, $t_{p(preset)}$ (See Fig. F)	25			25			ns
Width of Clear Pulse, $t_{p(clear)}$ (See Fig. F)	25			25			ns
Input Setup Time, t_{setup} (See Fig. E)	$\geqslant t_{p(clock)}$			$\geqslant t_{p(clock)}$			
Input Hold Time, t_{hold}	0			0			

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH	41 & 42
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW	41 & 42
V_{OH}	Output HIGH Voltage	2.4	3.5		Volts	V_{CC} = MIN., I_{OH} = −0.4 mA	41
V_{OL}	Output LOW Voltage		0.22	0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA	42
I_{IH}	Input HIGH Current at J_1, J_2, J_3, K_1, K_2 or K_3			40	µA	V_{CC} = MAX., V_{IN} = 2.4 V	44
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
	Input HIGH Current at Clear Preset or Clock			80	µA	V_{CC} = MAX., V_{IN} = 2.4 V	44
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IL}	Input LOW Current at J_1, J_2, J_3, K_1, K_2 or K_3			−1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V	43
	Input LOW Current at Clear, Preset or Clock			−3.2	mA	V_{CC} = MAX., V_{IN} = 0.4 V	43
I_{OS}	Output Short Circuit Current (Note 3)	−20		−57	mA	9N72/5472 | V_{CC} = MAX.	45
		−18		−57	mA	9N72/7472 | V_{IN} = 0 V	
I_{CC}	Supply Current		10	20	mA	V_{CC} = MAX., V_{IN} = 5.0 V	44

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
f_{max}	Maximum Clock Frequency	15	20		MHz	V_{CC} = 5.0 V C_L = 15 pF R_L = 400Ω	E
t_{PLH}	Turn Off Delay Clear or Preset to Output		16	25	ns		F
t_{PHL}	Turn On Delay Clear or Preset to Output		25	40	ns		F
t_{PLH}	Turn Off Delay Clock to Output	10	16	25	ns		E
t_{PHL}	Turn On Delay Clock to Output	10	25	40	ns		E

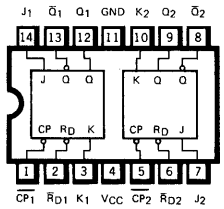
NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.

DUAL JK MASTER/SLAVE FLIP-FLOP WITH SEPARATE CLEARS AND CLOCKS

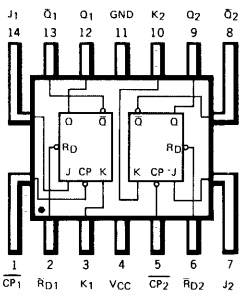
DESCRIPTION – The HSTTL/SSI 9H73/54H73, 74H73 is a High Speed Dual JK Master/Slave flip-flop with separate clears and separate clocks. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the circuitry which connects the master and slave sections. The sequence of operation is as follows: 1) Isolate slave from master. 2) Enter information from J and K inputs to master. 3) Disable J and K inputs. 4) Transfer information from master to slave. Logic state of J and K inputs must not be allowed to change when the clock pulse is in a HIGH state.

LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)



FLATPAK (TOP VIEW)

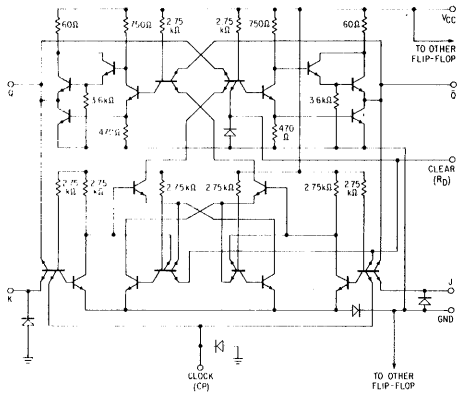


Positive logic:

LOW input to clear sets Q to LOW level

Clear is independent of clock

SCHEMATIC DIAGRAM
(EACH FLIP-FLOP)



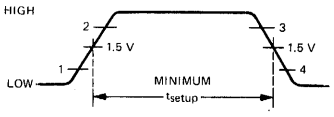
Component values shown are typical.
Resistor values are in ohms.

TRUTH TABLE

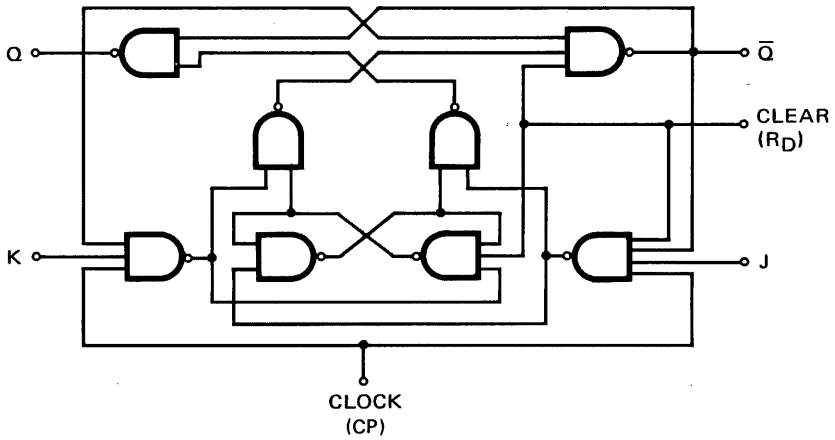
t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

NOTES:
t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.

CLOCK WAVEFORMS



LOGIC DIAGRAM
(EACH FLIP-FLOP)



RECOMMENDED OPERATING CONDITIONS

PARAMETER	9H73XM/54H73XM			9H73XC/74H73XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	70	°C
Fan Out from Each Output			12.5			12.5	U.L.
Width of Clock Pulse, $t_{p(clock)}$ (See Fig. W)	12			12			ns
Width of Clear Pulse, $t_{p(clear)}$ (See Fig. X)	16			16			ns
Input Setup Time, t_{setup} (See Clock Waveform)	$\geq t_{p(clock)}$			$\geq t_{p(clock)}$			
Input Hold Time, t_{hold}	0			0			

X = package type; F for Flaptak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH	46 & 47
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW	46 & 47
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = −0.5 mA	46
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 20 mA	47
I_{IH}	Input HIGH Current at J or K			50	µA	V_{CC} = MAX., V_{IN} = 2.4 V	126
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
	Input HIGH Current at Clock			5.0	µA	V_{CC} = MAX., V_{IN} = 2.4 V	126
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
	Input HIGH Current at Clear			100	µA	V_{CC} = MAX., V_{IN} = 2.4 V	126
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IL}	Input LOW Current at J, K or Clock			−2.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V	125
	Input LOW Current at Clear			−4.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V	125
I_{OS}	Output Short Circuit Current (Note 3)	−40		−100	mA	V_{CC} = MAX., V_{IN} = 0V	50
I_{CC}	Supply Current		32	50	mA	V_{CC} = MAX.	126

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
f_{CLOCK}	Maximum Clock Frequency	25	30		MHz	V_{CC} = 5.0 V C_L = 25 pF R_L = 280Ω	W
t_{PLH}	Turn Off Delay Clear to Output		6.0	13	ns		X
t_{PHL}	Turn On Delay Clear to Output		12	24	ns		X
t_{PLH}	Turn Off Delay Clock to Output	6.0	14	21	ns		W
t_{PHL}	Turn On Delay Clock to Output	10	22	27	ns		W

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

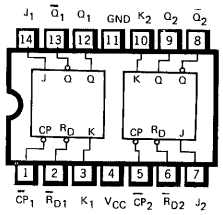
DUAL JK MASTER/SLAVE FLIP-FLOP WITH SEPARATE CLEARS AND CLOCKS

DESCRIPTION – The TTL/SSI 9N73/5473, 7473 and 9N107/54107, 74107 are Dual JK Master/Slave flip-flops with a separate clear and a separate clock for each flip-flop. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows: 1) Isolate slave from master. 2) Enter information from J and K inputs to master. 3) Disable J and K inputs. 4) Transfer information from master to slave.

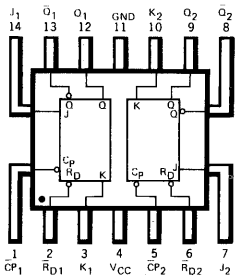
LOGIC AND CONNECTION DIAGRAM

9N73/5473, 7473

DIP (TOP VIEW)

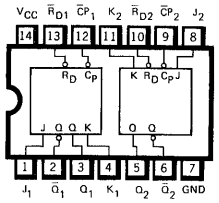


FLATPAK (TOP VIEW)



9N107/54107, 74107

DIP (TOP VIEW)



Positive logic:
LOW input to clear sets Q to LOW level
Clear is independent of clock

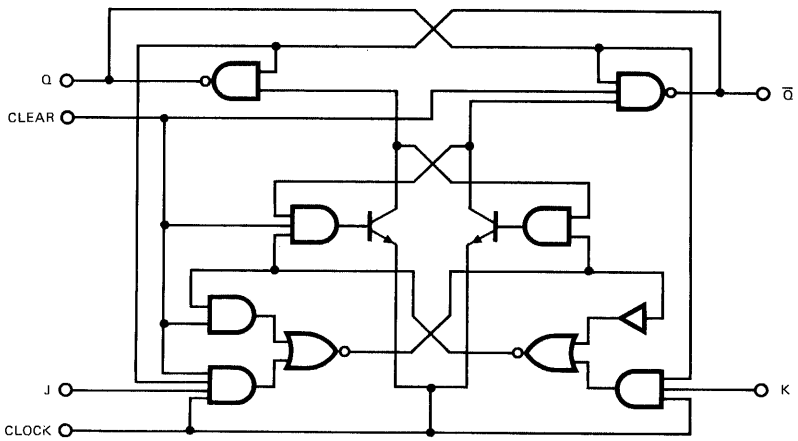
TRUTH TABLE

t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\bar{Q}_n$

CLOCK WAVEFORM

NOTES:
t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.

LOGIC DIAGRAM
(EACH FLIP-FLOP)



RECOMMENDED OPERATING CONDITIONS

PARAMETER	9N73XM/5473XM 9N107XM/54107XM			9N73XC/7473XC 9N107XC/74107XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	70	°C
Normalized Fan Out from Each Output, N			10			10	U.L.
Width of Clock Pulse, $t_{p(clock)}$ (See Fig. E)	20			20			ns
Width of Clear Pulse, $t_{p(clear)}$ (See Fig. F)	25			25			ns
Input Setup Time, t_{setup} (See Fig. E)	$\geqslant t_{p(clock)}$			$\geqslant t_{p(clock)}$			
Input Hold Time, t_{hold}	0			0			

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP. (Note 2)	LIMITS MAX.	UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH		46 & 47
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW		46 & 47
V_{OH}	Output HIGH Voltage	2.4	3.5		Volts	V_{CC} = MIN., I_{OH} = −0.4 mA		46
V_{OL}	Output LOW Voltage		0.22	0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA		47
I_{IH}	Input HIGH Current at J or K			40	μA	V_{CC} = MAX., V_{IN} = 2.4 V		49
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
	Input HIGH Current at Clock or Clear			80	μA	V_{CC} = MAX., V_{IN} = 2.4 V		49
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current at J or K			−1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V		48
	Input LOW Current at Clear or Clock			−3.2	mA	V_{CC} = MAX., V_{IN} = 0.4 V		48
I_{OS}	Output Short Circuit Current (Note 3)	−20		−57	mA	9N73/5473; 9N107/54107	V_{CC} = MAX.	50
		−18		−57	mA	9N73/7473; 9N107/74107	V_{IN} = 0 V	
I_{CC}	Supply Current		20	40	mA	V_{CC} = MAX.		49

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS	TEST FIGURE
f_{max}	Maximum Clock Frequency	15	20		MHz	V_{CC} = 5.0 V, C_L = 15 pF, R_L = 400Ω	E
t_{PLH}	Turn Off Delay Clear to Output		16	25	ns		F
t_{PHL}	Turn On Delay Clear to Output		25	40	ns		F
t_{PLH}	Turn Off Delay Clock to Output	10	16	25	ns		E
t_{PHL}	Turn On Delay Clock to Output	10	25	40	ns		E

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.

DUAL D TYPE EDGE TRIGGERED FLIP-FLOP

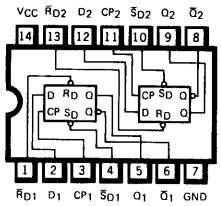
DESCRIPTION — The HSTTL/SSI 9H74/54H74, 74H74 is a High Speed Dual, Edge Triggered flip-flop utilizing TTL circuitry to perform D type flip-flop logic. Each flip-flop has individual clear and preset inputs, and also complementary Q and Q outputs.

Information at input D is transferred to the Q output on the positive going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. When the clock input is at either the HIGH or LOW level, the D input signal has no effect.

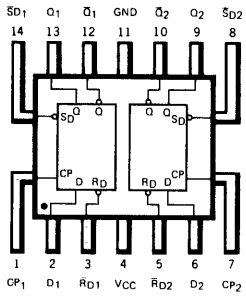
These circuits are fully compatible for use with the Fairchild TTL family. Input clamping diodes are provided to minimize transmission line effects and thereby simplify systems design. Maximum clock frequency is 35 MHz, with a typical power dissipation of 75 mW per flip-flop.

LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)

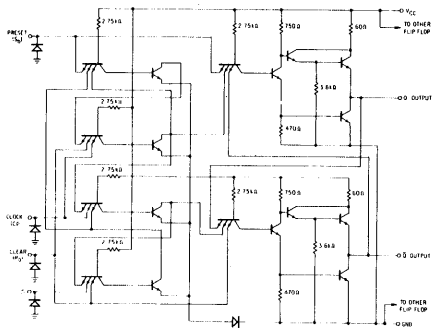


FLATPAK (TOP VIEW)



Asynchronous Inputs:
LOW input to preset sets Q to HIGH level
LOW input to clear sets Q to LOW level
Preset and clear are independent of clock

SCHEMATIC DIAGRAM (EACH FLIP-FLOP)



Component values shown are typical.

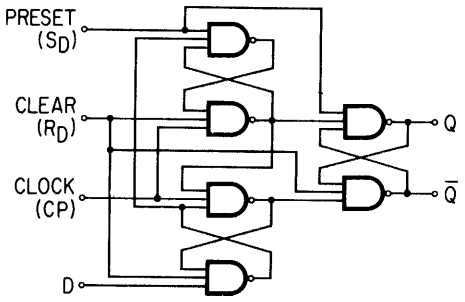
TRUTH TABLE (Each Flip-Flop)

t_n	t_{n+1}	
INPUT D	OUTPUT Q	OUTPUT $\bar{Q}$
L	L	H
H	H	L

H = HIGH Level, L = LOW Level

NOTES: t_n = bit time before clock pulse.
t_{n+1} = bit time after clock pulse.

LOGIC DIAGRAM (EACH FLIP-FLOP)



RECOMMENDED OPERATING CONDITIONS

PARAMETER		9H74XM/54H74XM			9H74XC/74H74XC			UNIT
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Operating Free-Air Temperature Range		−55	25	125	0	25	70	°C
Fan Out from Each Output	LOW Level			12.5			12.5	U.L.
	HIGH Level			25			25	
Clock Frequency, f_{clock}		0		35	0		35	MHz
Width of Clock Pulse, $t_{pw(clock)}$ (See Figure Z or AA)		15			15			ns
Width of Preset pulse, $t_{pw(preset)}$ (See Figure Y)		25			25			ns
Width of Clear Pulse, $t_{pw(clear)}$ (See Figure Y)		25			25			ns
Input Setup Time, t_{setup} (See Note a)	HIGH Level Data (See Figure Z)	10			10			ns
	LOW Level Data (See Figure AA)	15			15			ns
Input Hold Time, t_{hold} (See Note b and Figures Z and AA)		0			0			ns

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

NOTES:
(a) Setup time is the interval immediately preceding the positive going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.
(b) Hold time is the interval immediately following the positive going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to ensure its continued recognition.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH		52 & 53
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW		52 & 53
V_{OH}	Output HIGH Voltage	2.4	3.5		Volts	V_{CC} = MIN., I_{OH} = −1.0 mA		52
V_{OL}	Output LOW Voltage		0.22	0.4	Volts	V_{CC} = MIN., I_{OL} = 20 mA		53
I_{IH}	Input HIGH Current into D			50	μA	V_{CC} = MAX., V_{IN} = 2.4 V		55
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
	Input HIGH Current into Preset or Clock			100	μA	V_{CC} = MAX., V_{IN} = 2.4 V		55
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
	Input HIGH Current into Clear into Clear			150	μA	V_{CC} = MAX., V_{IN} = 2.4 V		55
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current into Preset or D			−2.0	mA	V_{CC} = MAX. V_{IN} = 5.5 V		54
	Input LOW Current into Clear or Clock			−4.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V		54
I_{OS}	Output Short Circuit Current (Note 3)	−40		−100	mA	V_{CC} = MAX., V_{IN} = 0 V		56
I_{CC}	Supply Current		30	42	mA	9H74/54H74	V_{CC} = MAX.	55
			30	50	mA	9H74/74H74		

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
f_{CLOCK}	Maximum Clock Frequency	35	43		MHz	V_{CC} = 5.0 V C_L = 25 pF R_L = 280Ω	Z & AA
t_{PLH}	Turn Off Delay Clear or Preset Inputs to Output			20	ns		Y
t_{PHL}	Turn On Delay Clear or Preset Inputs to Output			30	ns		Y
t_{PLH}	Turn Off Delay Clock Input to Output	4.0	8.5	15	ns		Z & AA
t_{PHL}	Turn On Delay Clock Input to Output	7.0	13	20	ns		Z & AA

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

DUAL D TYPE EDGE TRIGGERED FLIP-FLOP

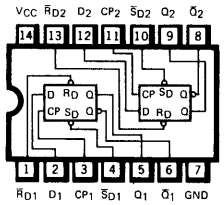
DESCRIPTION – The 9N74/5474, 7474 are edge triggered dual D type flip-flops with direct clear and preset inputs and both Q and $\overline{Q}$ outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. They are designed for use in medium to high speed applications.

Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. After the clock input threshold voltage has been passed, the data input (D) is locked out and information present will not be transferred to the output.

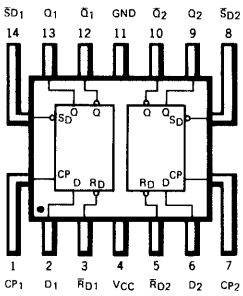
The 9N74/5474, 7474 have the same clocking characteristics as the 9N70/5470, 7470 gated (edge triggered) flip-flop circuits. They can result in a significant saving in system power dissipation and package count in applications where input gating is not required.

LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)

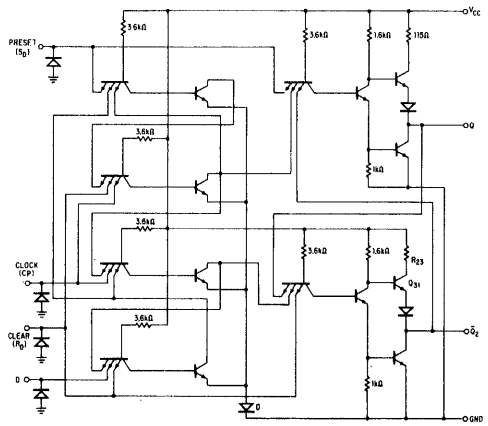


FLATPAK (TOP VIEW)



Positive logic:
LOW input to preset sets Q to HIGH level
LOW input to clear sets Q to LOW level
Preset and clear are independent of clock

SCHEMATIC DIAGRAM
(EACH FLIP-FLOP)



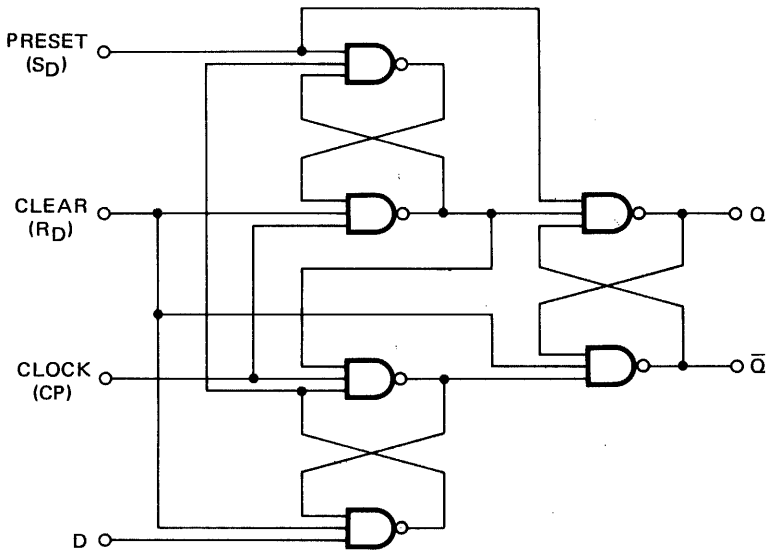
Component values shown are typical.

TRUTH TABLE (Each Flip-Flop)

t_n	t_{n+1}	
INPUT D	OUTPUT Q	OUTPUT $\overline{Q}$
L	L	H
H	H	L

NOTES:
t_n = bit time before clock pulse.
t_{n+1} = bit time after clock pulse.

LOGIC DIAGRAM (EACH FLIP-FLOP)



RECOMMENDED OPERATING CONDITIONS

PARAMETER	9N74XM/5474XM			9N74XC/7474XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	70	°C
Normalized Fan Out from Each Output, N			10			10	U.L.
Width of Clock Pulse, $t_{p(clock)}$ (See Fig. G)	30			30			ns
Width of Preset Pulse, $t_{p(preset)}$ (See Fig. C)	30			30			ns
Width of Clear Pulse, $t_{p(clear)}$ (See Fig. C)	30			30			ns

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH	52 & 53
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW	52 & 53
V_{OH}	Output HIGH Voltage	2.4	3.5		Volts	V_{CC} = MIN., I_{OH} = –0.4 mA	52
V_{OL}	Output LOW Voltage		0.22	0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA	53
I_{IH}	Input HIGH Current at D			40	μA	V_{CC} = MAX., V_{IN} = 2.4 V	55
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
	Input HIGH Current at Preset or Clock			80	μA	V_{CC} = MAX., V_{IN} = 2.4 V	55
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
	Input HIGH Current at Clear			120	μA	V_{CC} = MAX., V_{IN} = 2.4 V	55
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IL}	Input LOW Current at Preset or D			–1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V	54
	Input LOW Current at Clear or Clock			–3.2	mA	V_{CC} = MAX., V_{IN} = 0.4 V	54
I_{OS}	Output Short Circuit Current (Note 3)	–20		–57	mA	9N74/5474 V_{CC} = MAX.	56
		–18		–57	mA	9N74/7474 V_{IN} = 0 V	
I_{CC}	Supply Current		17	30	mA	V_{CC} = MAX.	55

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
f_{max}	Maximum Clock Frequency	15	25		MHz	V_{CC} = 5.0 V C_L = 15 pF R_L = 400Ω	G
t_{setup}	Maximum Input Setup Time		15	20	ns		G
t_{hold}	Maximum Input Hold Time		2.0	5.0	ns		G
t_{PLH}	Turn Off Delay Clear or Preset to Output			25	ns		C
t_{PHL}	Turn On Delay Clear or Preset to Output			40	ns		C
t_{PLH}	Turn Off Delay Clock to Output	10	14	25	ns		G
t_{PHL}	Turn On Delay Clock to Output	10	20	40	ns		G

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.

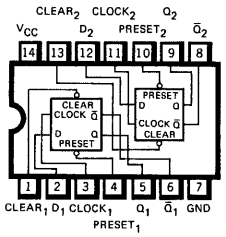
DUAL D-TYPE EDGE TRIGGERED FLIP-FLOP

DESCRIPTION – The 9S74/54S74, 74S74 dual edge-triggered flip-flops utilize Schottky TTL circuitry to produce very high speed D-type flip-flops. Each flip-flop has individual clear and preset inputs, and also complementary Q and $\overline{Q}$ outputs.

Information at input D is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the HIGH or LOW level the D-input signal has no effect.

These circuits are fully compatible for use with most TTL or DTL circuits. Maximum clock frequency is 100 MHz with a typical power dissipation of 66 mW per flip-flop.

LOGIC AND CONNECTION DIAGRAM DIP (TOP VIEW)



Positive logic: LOW input to preset sets Q to HIGH level
LOW input to clear resets Q to LOW level
Preset and clear are independent of clock

SYNCHRONOUS TRUTH TABLE (EACH FLIP-FLOP)

t_n	t_{n+1}	
INPUT	OUTPUT	
D	Q	$\overline{Q}$
L	L	H
H	H	L

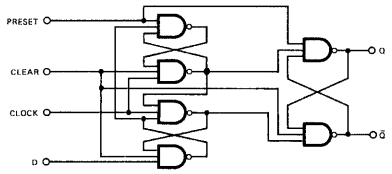
H = HIGH level
L = LOW level
D = Data

NOTES:
A. t_n = bit time before clock pulse
B. t_{n+1} = bit time after clock pulse

ASYNCHRONOUS TRUTH TABLE (EACH FLIP-FLOP)

INPUT		OUTPUT	
Preset	Clear	Q	$\overline{Q}$
L	L	H	H
L	H	H	L
H	L	L	H
H	H	No Change	

LOGIC DIAGRAM (EACH FLIP-FLOP)



RECOMMENDED OPERATING CONDITIONS

PARAMETER	† 9S74XM/54S74XM			9S74XC/74S74XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	75	°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

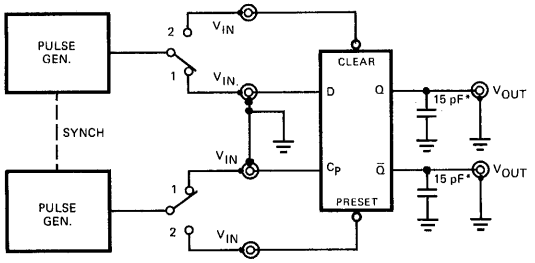
SYMBOL	PARAMETER		LIMITS MIN.	LIMITS TYP. (Note 2)	LIMITS MAX.	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			Volts	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage				0.8	Volts	Guaranteed Input LOW Voltage
V_{CD}	Input Clamp Diode Voltage			–0.65	–1.2	Volts	V_{CC} = MIN., I_{IN} = –18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		Volts	V_{CC} = MIN., I_{OH} = –1.0 mA
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage			0.35	0.5	Volts	V_{CC} = MIN., I_{OL} = 20 mA
I_{IH}	Input HIGH Current at	D		1.0	50	μA	V_{CC} = MAX., V_{IN} = 2.7 V
		Preset or Clock		2.0	100		
		Clear		3.0	150		
I_{IL}	Input LOW Current at	D		–1.4	–2.0	mA	V_{CC} = MAX., V_{IN} = 0.5 V
		Preset or Clock		–2.8	–4.0		
		Clear		–4.2	–6.0		
I_{OS}	Output Short Circuit Current (Note 3)		–40	–65	–100	mA	V_{CC} = MAX., V_{OUT} = 0V
I_{CC}	Supply Current			30	50	mA	V_{CC} = MAX. (Note 4)

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.
(4) I_{CC} is measured with clock and data inputs grounded and either preset or clear inputs grounded.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN.	TYP.	MAX.		
f_{max}	Maximum Clock Frequency		100		MHz	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH}	Turn Off Delay Clear or Preset to Output		4.0		ns	
t_{PHL}	Turn On Delay Clear or Preset to Output		7.0		ns	
t_{PLH}	Turn Off Delay Clock to Output		7.0		ns	
t_{PHL}	Turn On Delay Clock to Output		7.0		ns	

SWITCHING CHARACTERISTICS



*Includes all probe and jig capacitance.

PULSE GENERATOR SETTINGS

CLOCK

f ≈ 1 MHz
$t_f = t_r$ = 2.5 ns
Amp = 0 to 3 V
Duty cycle= 50%

D

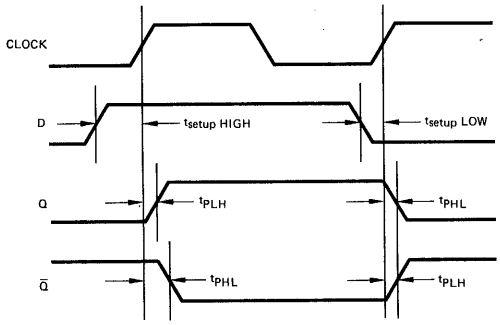
f ≈ 500 kHz
$t_f = t_r$ = 2.5 ns
Amp = 0 to 3 V
t_{setup} (HIGH) = 5 ns
t_{setup} (LOW) = 4 ns
Duty cycle = Adjust pulse width to attain t_{setup} (HIGH) and t_{setup} (LOW) relative to clock as shown in waveforms.

DIRECT SET, CLEAR

f ≈ 1 MHz
$t_f = t_r$ = 2.5 ns
Amp = 0 to 3 V
Duty cycle =Adjust pulse width and synch to attain waveforms shown.

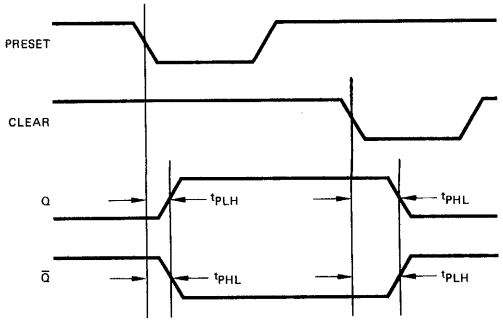
SWITCHING WAVEFORMS

CLOCK TO OUTPUT DELAY†



SWITCH IN POSITION 1

DIRECT SET, AND CLEAR TO OUTPUT DELAY



SWITCH IN POSITION 2

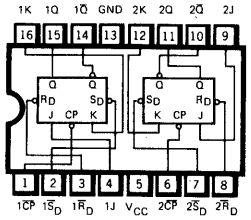
†Direct set and clear inputs connected to V_{CC} thru 2 kΩ resistor during test.

DUAL JK MASTER/SLAVE FLIP-FLOP WITH SEPARATE PRESETS, CLEARS AND CLOCKS

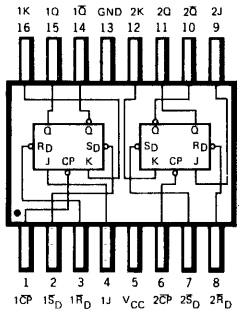
DESCRIPTION – The HSTTL/SSI 9H76/54H76, 74H76 is a High Speed Dual JK Master/Slave flip-flop with separate presets, separate clears and separate clocks. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the circuitry which connects the master and slave sections. The sequence of operation is as follows: 1) Isolate slave from master. 2) Enter information from J and K inputs to master. 3) Disable J and K inputs. 4) Transfer information from master to slave. Logic state of J and K inputs must not be allowed to change when the clock pulse is a HIGH state.

LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)



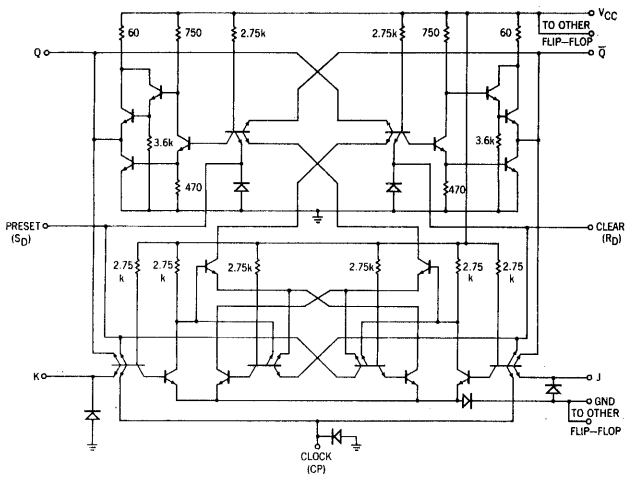
FLATPAK (TOP VIEW)



Positive logic:

LOW input to preset sets Q to HIGH level
LOW input to clear sets Q to LOW level
Clear and preset are independent of clock

SCHEMATIC DIAGRAM
(EACH FLIP-FLOP)



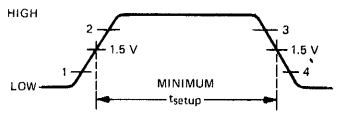
Component values shown are typical.

TRUTH TABLE

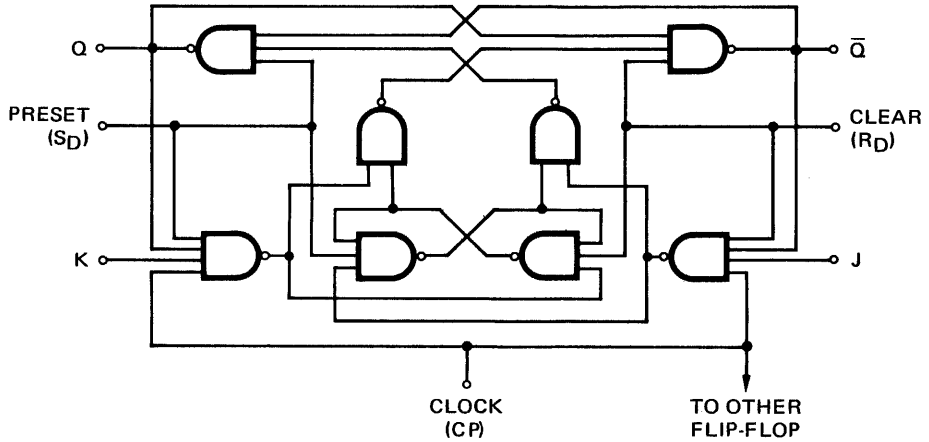
t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

NOTES:
t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.

CLOCK WAVEFORM



LOGIC DIAGRAM
(EACH FLIP-FLOP)



RECOMMENDED OPERATING CONDITIONS

PARAMETER	9H76XM/54H76XM			9H76XC/74H76XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	70	°C
Fan Out from Each Output			12.5			12.5	U.L.
Width of Clock Pulse, $t_{p(clock)}$ (See Fig. W)	12			12			ns
Width of Preset Pulse, $t_{p(preset)}$ (See Fig. X)	16			16			ns
Width of Clear Pulse, $t_{p(clear)}$ (See Fig. X)	16			16			ns
Input Setup Time, t_{setup} (See Clock Waveform)	$\geq t_{p(clock)}$			$\geq t_{p(clock)}$			
Input Hold Time, t_{hold}	0			0			

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH	46 & 47
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW	46 & 47
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = −0.5 mA	46
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 20 mA	47
I_{IH}	Input HIGH Current at J, K or Clock			50	μA	V_{CC} = MAX., V_{IN} = 2.4 V	126
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
	Input HIGH Current at Clear or Preset			100	μA	V_{CC} = MAX., V_{IN} = 2.4 V	126
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IL}	Input LOW Current at J, K or Clock			−2.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V	125
	Input LOW Current at Clear or Preset			−4.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V	125
I_{OS}	Output Short Circuit Current (Note 3)	−40		−100	mA	V_{CC} = MAX., V_{IN} = 0	50
I_{CC}	Supply Current		32	50	mA	V_{CC} = MAX., V_{IN} = 4.5 V	126

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
f_{CLOCK}	Maximum Clock Frequency	25	30		MHz	V_{CC} = 5.0 V C_L = 25 pF R_L = 280Ω	W
t_{PLH}	Turn Off Delay Clear or Preset to Output		6.0	13	ns		X
t_{PHL}	Turn On Delay Clear or Preset to Output		12	24	ns		X
t_{PLH}	Turn Off Delay Clock to Output	6.0	14	21	ns		W
t_{PHL}	Turn on Delay Clock to Output	10	22	27	ns		W

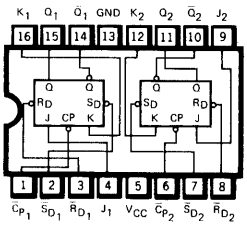
NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

DUAL JK MASTER/SLAVE FLIP-FLOP WITH SEPARATE PRESETS, CLEARS AND CLOCKS

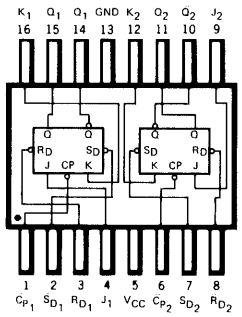
DESCRIPTION – The TTL/SSI 9N76/5476, 7476 is a Dual JK Master/Slave flip-flop with separate presets, separate clears and separate clocks. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows: 1) Isolate slave from master. 2) Enter information from J and K inputs to master. 3) Disable J and K inputs. 4) Transfer information from master to slave.

LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)

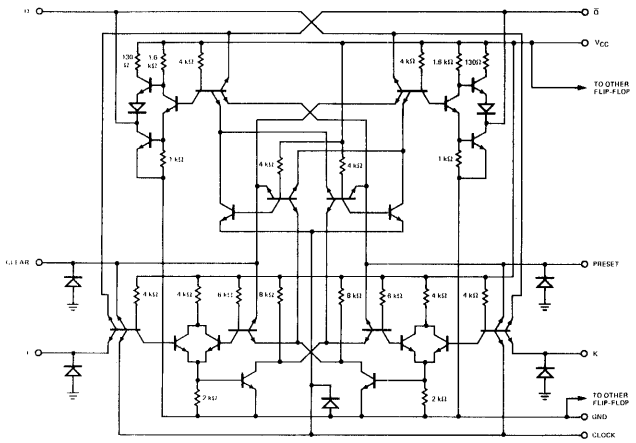


FLATPAK (TOP VIEW)



Positive logic:
LOW input to preset sets Q to HIGH level
LOW input to clear sets Q to LOW level
Clear and preset are independent of clock

SCHEMATIC DIAGRAM
(EACH FLIP-FLOP)



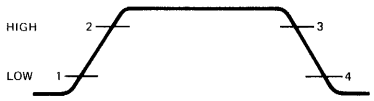
Component values shown are typical.

TRUTH TABLE

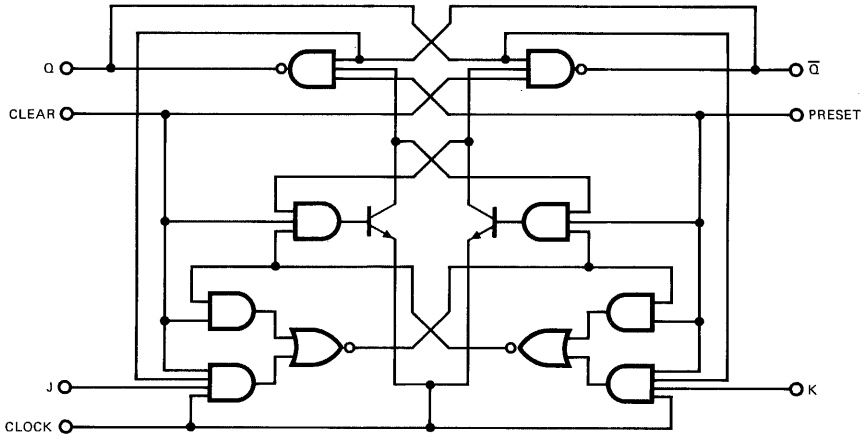
t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\bar{Q}_n$

NOTES:
t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.

CLOCK WAVEFORM



LOGIC DIAGRAM
(EACH FLIP-FLOP)



RECOMMENDED OPERATING CONDITIONS

PARAMETER	9N76XM/5476XM			9N76XC/7476XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	70	°C
Normalized Fan Out from Each Output, N			10			10	U.L.
Width of Clock Pulse, $t_{p(clock)}$ (See Fig. E)	20			20			ns
Width of Preset Pulse, $t_{p(preset)}$ (See Fig. F)	25			25			ns
Width of Clear Pulse, $t_{p(clear)}$ (See Fig. F)	25			25			ns
Input Setup Time, t_{setup} (See Fig. E)	$\geq t_{p(clock)}$			$\geq t_{p(clock)}$			
Input Hold Time, t_{hold}	0			0			

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH	46 & 47
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW	46 & 47
V_{OH}	Output HIGH Voltage	2.4	3.5		Volts	V_{CC} = MIN., I_{OH} = −0.4 mA	46
V_{OL}	Output LOW Voltage		0.22	0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA	47
I_{IH}	Input HIGH Current at J or K			40	μA	V_{CC} = MAX., V_{IN} = 2.4 V	49
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
	Input HIGH Current at Clear, Preset or Clock			80	μA	V_{CC} = MAX., V_{IN} = 2.4 V	49
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IL}	Input LOW Current at J or K			−1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V	48
	Input LOW Current at Clear, Preset, or Clock			−3.2	mA	V_{CC} = MAX., V_{IN} = 0.4 V	48
I_{OS}	Output Short Circuit Current (Note 3)	−20		−57	mA	9N76/5476 | V_{CC} = MAX.	51
		−18		−57	mA	9N76/7476 | V_{IN} = 0 V	
I_{CC}	Supply Current		20	40	mA	V_{CC} = MAX.	49

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
f_{max}	Maximum Clock Frequency	15	20		MHz	V_{CC} = 5.0 V C_L = 15 pF R_L = 400Ω	E
t_{PLH}	Turn Off Delay Clear or Preset to Output		16	25	ns		F
t_{PHL}	Turn On Delay Clear or Preset to Output		25	40	ns		F
t_{PLH}	Turn Off Delay Clock to Output	10	16	25	ns		E
t_{PHL}	Turn On Delay Clock to Output	10	25	40	ns		E

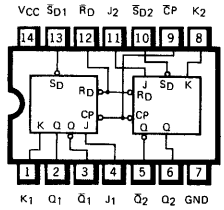
NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Note more than one output should be shorted at a time.

DUAL JK MASTER/SLAVE FLIP-FLOP WITH SEPARATE PRESETS, AND A COMMON CLEAR AND CLOCK

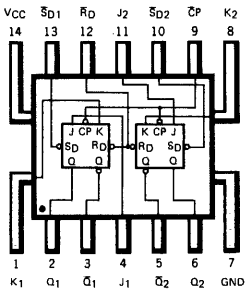
DESCRIPTION – The HSTTL/SSI 9H78/54H78, 74H78 is a High Speed Dual JK Master/Slave flip-flop with separate presets, a common clear and a common clock. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the circuitry which connects the master and slave sections. The sequence of operation is as follows: 1) Isolate slave from master. 2) Enter information from J and K inputs to master. 3) Disable J and K inputs. 4) Transfer information from master to slave. Logic state of J and K inputs must not be allowed to change when the clock pulse is in a HIGH state.

LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)



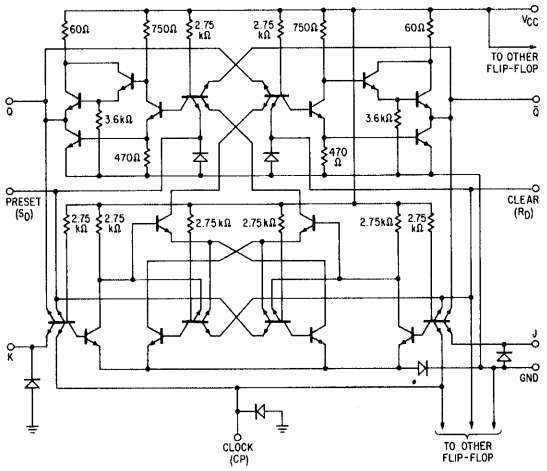
FLATPAK (TOP VIEW)



Positive logic:

LOW input to preset sets Q to HIGH level
LOW input to clear sets Q to LOW level
Preset and clear are independent of clock

SCHEMATIC DIAGRAM
(EACH FLIP FLOP)



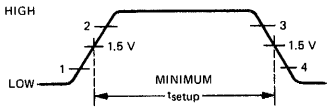
Component values shown are typical.

TRUTH TABLE

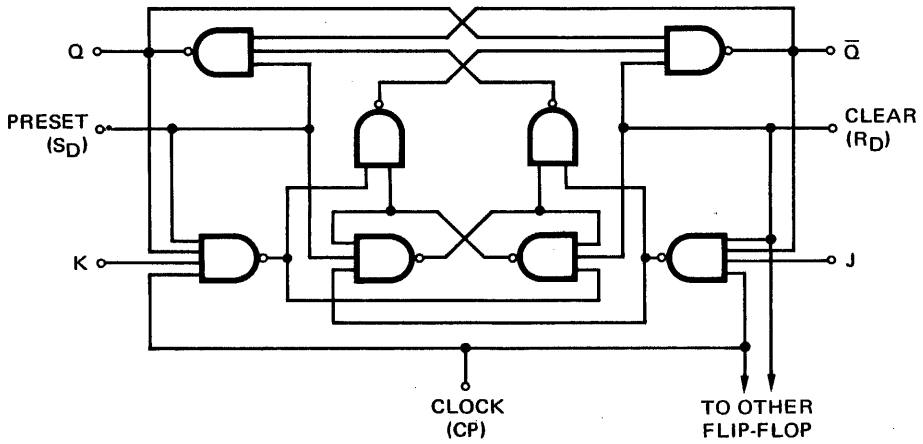
t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\bar{Q}_n$

NOTES:
t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.

CLOCK WAVEFORM



LOGIC DIAGRAM
(EACH FLIP-FLOP)



RECOMMENDED OPERATING CONDITIONS

PARAMETER	9H78XM/54H78XM			9H78XC/74H78XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	70	°C
Fan Out from Each Output			12.5			12.5	U.L.
Width of Clock Pulse, $t_{p(clock)}$ (See Fig. W)	12			12			ns
Width of Preset Pulse, $t_{p(preset)}$ (See Fig. X)	16			16			ns
Width of Clear Pulse, $t_{p(clear)}$ (See Fig. X)	16			16			ns
Input Setup Time, t_{setup} (See Clock Waveform)	$\geq t_{p(clock)}$			$\geq t_{p(clock)}$			
Input Hold Time, t_{hold}	0			0			

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage	46 & 47
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage	46 & 47
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = −0.5 mA	46
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 20 mA	47
I_{IH}	Input HIGH Current at J or K			50	µA	V_{CC} = MAX., V_{IN} = 2.4 V	126
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
	Input HIGH Current at Preset or Clock			100	µA	V_{CC} = MAX., V_{IN} = 2.4 V	126
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
	Input HIGH Current at Clear			200	µA	V_{CC} = MAX., V_{IN} = 2.4 V	126
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IL}	Input LOW Current at J or K			−2.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V	125
	Input LOW Current at Preset or Clock			−4.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V	125
	Input LOW Current at Clear			−8.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V	125
I_{OS}	Output Short Circuit Current (Note 3)	−40		−100	mA	V_{CC} = MAX., V_{IN} = 0V	51
I_{CC}	Supply Current		32	50	mA	V_{CC} = MAX.	126

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
f_{CLOCK}	Maximum Clock Frequency	25	30		MHz	V_{CC} = 5.0 V, C_L = 25 pF, R_L = 280Ω	W
t_{PLH}	Turn Off Delay Clear to Output		6	13	ns		X
t_{PHL}	Turn On Delay Clear to Output		12	24	ns		X
t_{PLH}	Turn On Delay Clock to Output	6.0	14	21	ns		W
t_{PHL}	Turn On Delay Clock to Output	10	22	27	ns		W

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

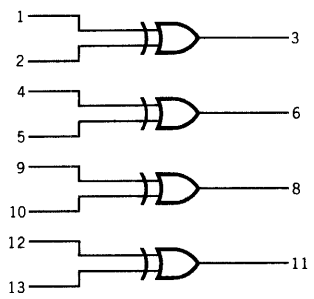
LPTTL/SSI 9L86

LOW POWER QUAD EXCLUSIVE OR GATE

DESCRIPTION — The Low Power TTL/SSI 9L86 consists of four Exclusive OR Gates. Designed for low power, medium speed operation, the 9L86 is useful in large number of code conversion, parity generation/checking and comparison applications. The exclusive OR gate produces an output when the inputs are complementary. The Boolean expression for the device is: $Z = A\bar{B} + \bar{A}B$.

- TYPICAL PROPAGATION DELAY OF 25 ns
- TYPICAL POWER DISSIPATION OF 25 mW
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- ALL CERAMIC "HERMETIC" 14-LEAD DUAL IN-LINE AND FLAT PACKAGES
- TTL COMPATIBLE

LOGIC SYMBOL



V_{CC} = PIN 14
GND = PIN 7

PIN NAMES

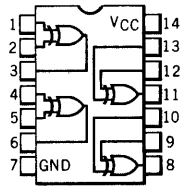
INPUTS (Pins 1, 2, 4, 5, 9, 10, 12, 13)
OUTPUTS (Pins 3, 6, 8, 11)

LOADING

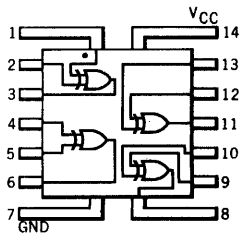
HIGH	LOW
0.75 U.L.	0.38 U.L.
10 U.L.	2.5 U.L.

1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.

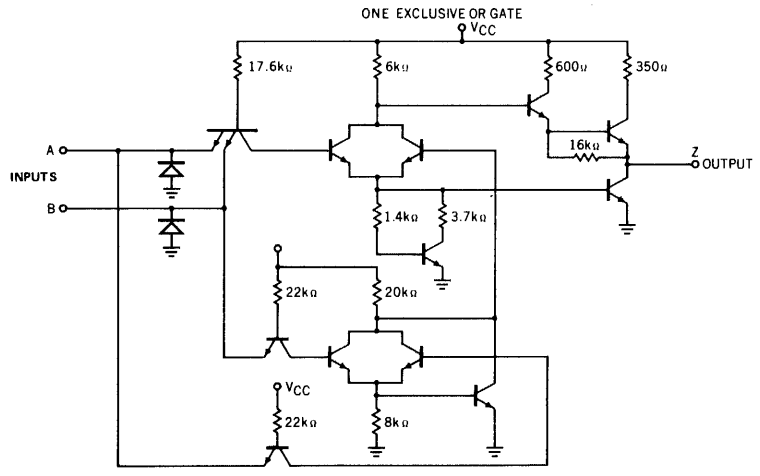
CONNECTION DIAGRAMS
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
9L86XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9L86XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted) (See Notes 1, 2 & 3)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP. Note 3	LIMITS MAX.	UNITS	CONDITIONS
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = −0.4 mA, V_{IN} = V_{IL} or V_{IH} per Truth Table
V_{OL}	Output LOW Voltage		0.1	0.3	Volts	V_{CC} = MIN., I_{OL} = 4.0 mA, V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed input HIGH voltage for all inputs
V_{IL}	Input LOW Voltage			0.7	Volts	Guaranteed input LOW voltage for all inputs
I_{IL}	Input LOW Current		−0.48	−0.6	mA	V_{CC} = MAX., V_{IN} = 0.3 V, other input = 4.5 V
I_{IH}	Input HIGH Current		6.0	30	µA	V_{CC} = MAX., V_{IN} = 2.4 V; other input = 0.0 V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V; other input = 0.0 V
I_{SC}*	Output Short Circuit Current	−10	−22	−40	mA	V_{CC} = MAX., V_{OUT} = 0.0 V, "A" inputs = 0.0 V, "B" inputs = 4.5 V
I_{CC}	Power Supply Current		6.8	9.5	mA	V_{CC} = MAX., All inputs = 0.0 V
			3.4	5.0	mA	V_{CC} = MAX., "A" inputs = 4.5 V, "B" inputs = 0.0 V
			6.3	9.0	mA	V_{CC} = MAX., All inputs = 4.5 V

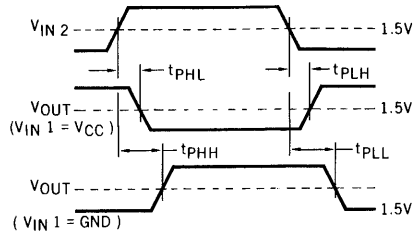
NOTES:
1. Conditions for testing, not shown in the Table, are chose to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, 25°C, and max. loading.

* Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	9L86XM MIN.	9L86XM TYP.	9L86XM MAX.	9L86XC MIN.	9L86XC TYP.	9L86XC MAX.	UNITS	CONDITIONS	
t_{PLH}	Switching Times	8	15	20	8	15	25	ns	V_{IN1} = 5.0 V	V_{CC} = 5.0 V, C_L = 15 pF
t_{PHL}		10	25	35	10	25	40	ns		
t_{PHH}	Switching Times	12	25	40	12	25	40	ns	V_{IN1} = 0.0 V	
t_{PLL}		20	35	45	20	35	50	ns		

SWITCHING TIME WAVEFORMS



TRUTH TABLE

A	B	Z
L	L	L
L	H	H
H	L	H
H	H	L

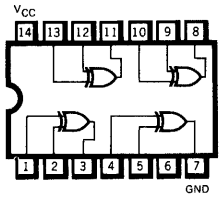
QUAD 2-INPUT EXCLUSIVE OR GATE

DESCRIPTION — The TTL/SSI 9N86/5486, 7486 is a Quad 2-input Exclusive OR gate designed to perform the function: $Y = A\overline{B} + \overline{A}B$. When the input states are complementary, the output goes to the HIGH level.

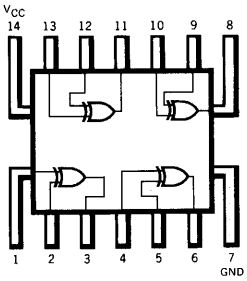
Input clamping diodes are provided to minimize transmission line effects. On chip input buffers are also provided to lower the fan in requirement to only 1 U.L. (unit load). The 9N86/5486, 7486 is fully compatible with all members of the Fairchild TTL family.

LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)



FLATPAK (TOP VIEW)

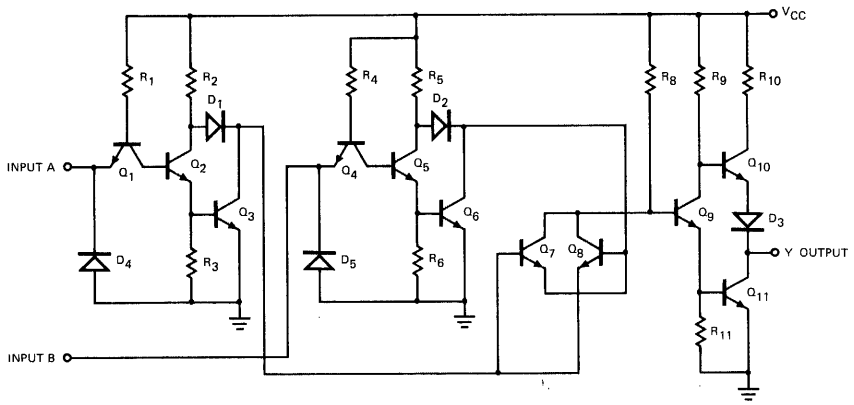


TRUTH TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

Positive logic: $Y = A \oplus B$

SCHEMATIC DIAGRAM



1/4 of Circuit shown.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		9N86XM/5486XM			9N86XC/7486XC			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}		4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range		–55	25	125	0	25	70	°C
Normalized Fan Out	LOW Level			10			10	U.L.
from Each Output N	HIGH Level			20			20	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage		98
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage		98
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = –800 μA, V_{IH} = 2.0 V, V_{IL} = 0.8 V		98
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA, V_{IH} = 2.0 V, V_{IL} = 0.8 V		99
I_{IH}	Input HIGH Current			40	μA	V_{CC} = MAX., V_{IN} = 2.4 V	(Each Input)	100
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current			–1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V	(Each Input)	101
I_{OS}	Output Short Circuit Current (Note 3)	–20		–55	mA	9N86/5486	V_{CC} = MAX., V_{IH} = 4.5 V, V_{IL} = 0 V	102
		–18		–55	mA	9N86/7486		
I_{CC}	Supply Current		30	43	mA	9N86/5486	V_{CC} = MAX., V_{IN} = 4.5 V	103
			30	50	mA	9N86/7486		

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS		TEST FIGURE
		MIN.	TYP.	MAX.				
t_{PLH}	Turn Off Delay Input to Output		15	23	ns	Other Input Low	V_{CC} = 5.0 V, C_L = 15 pF, R_L = 400Ω	S
			18	30		Other Input High		
t_{PHL}	Turn On Delay Input to Output		11	17		Other Input Low		
			13	22		Other Input High		

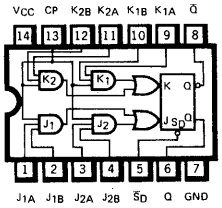
NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.

JK EDGE TRIGGERED FLIP-FLOP WITH AND-OR INPUTS

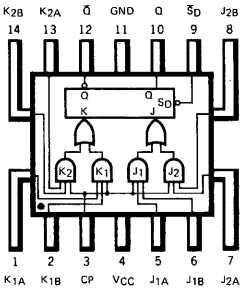
DESCRIPTION — The HSTTL/SSI 9H101/54H101, 74H101 is a High Speed JK Negative Edge Triggered flip-flop. The AND-OR gate inputs are inhibited while the clock input is LOW; when the clock goes HIGH, the inputs are enabled and data will be accepted. Logic state of J and K inputs may be allowed to change when the clock pulse is in a HIGH state and bistable will perform according to the truth table as long as minimum set up times are observed. Input data is transferred to the outputs on the negative edge of the clock pulse.

LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)



FLATPAK (TOP VIEW)

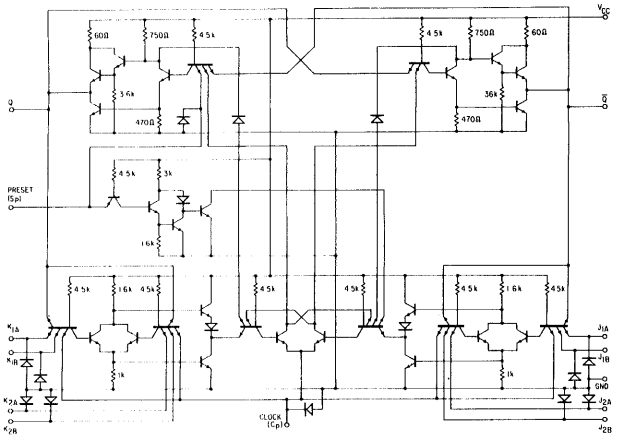


Positive logic:

LOW input to preset sets Q to HIGH level

Preset is independent of clock

SCHEMATIC DIAGRAM



TRUTH TABLE

t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	Q_n

NOTES:

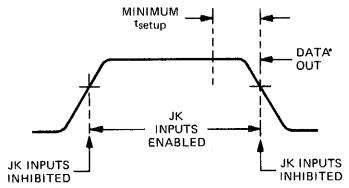
J = (J1A·J1B) + (J2A·J2B)

K = (k1A·K1B) + (K2A·K2B)

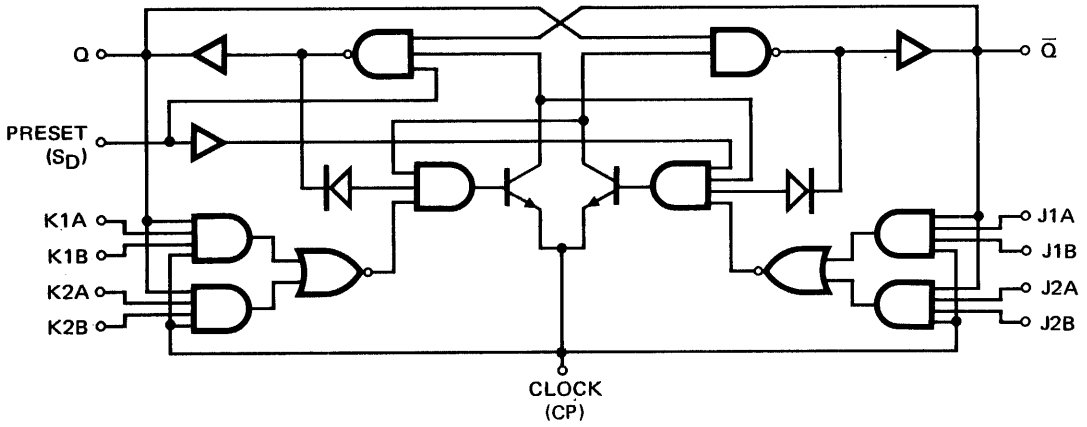
t_n = Bit time before clock

t_{n+1} = Bit time after clock pulse

CLOCK WAVEFORM



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

PARAMETER		9H101XM/54H101XM			9H101XC/74H101XC			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}		4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range		−55	25	125	0	25	70	°C
Fan Out from Each Output				12.5			12.5	U.L.
Width of Clock Pulse, $t_{p(clock)}$ (See Fig. W)		10			10			ns
Width of Preset Pulse, $t_{p(preset)}$ (See Fig. X)		16			16			ns
Input Setup Time, t_{setup} (See Clock Waveform)	LOW Level	13			13			ns
	HIGH Level	10			10			
Input Hold Time, t_{hold}		0			0			
Clock Pulse Transition Time, t_0 (See Fig. W)				150			150	ns

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH	121&122
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW	121&122
V_{OH}	Output HIGH Voltage	2.4	3.2		Volts	V_{CC} = MIN., I_{OH} = −0.5 mA	121
V_{OL}	Output LOW Voltage		0.25	0.4	Volts	V_{CC} = MIN., I_{OL} = 20 mA	122
I_{IH}	Input HIGH Current at J or K			50	μA	V_{CC} = MAX., V_{IN} = 2.4 V	124
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
	Input HIGH Current at Preset			100	μA	V_{CC} = MAX., V_{IN} = 2.4 V	124
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
	Input HIGH Current at Clock	0		−1.0	mA	V_{CC} = MAX., V_{IN} = 2.4V	124
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IL}	Input LOW Current at J1A, J1B, J2A, J2B, K1A, K1B, K2A, K2B, or Preset		−1.0	−2.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V	123
	Input LOW Current at Clock		−3.0	−4.8	mA	V_{CC} = MAX., V_{IN} = 0.4 V	123
I_{OS}	Output Short Circuit Current (Note 3)	−40		−100	mA	V_{CC} = MAX., V_{IN} = 0 V	127
I_{CC}	Supply Current		20	38	mA	V_{CC} = MAX.	124

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
f_{CLOCK}	Maximum Clock Frequency	40	50		MHz	V_{CC} = 5.0 V C_L = 25 pF R_L = 280Ω	W
t_{PLH}	Turn Off Delay Preset to Output		8.0	12	ns		X
t_{PHL}	Turn On Delay Preset to Output (Clock LOW)		23	35	ns		X
t_{PHL}	Turn On Delay Preset to Output (Clock HIGH)		15	20	ns		X
t_{PLH}	Turn Off Delay Clock to Output	5.0	10	15	ns		W
t_{PHL}	Turn On Delay Clock to Output	8.0	16	20	ns		W

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

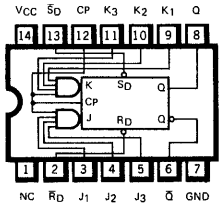
5

JK EDGE TRIGGERED FLIP-FLOP WITH AND INPUTS

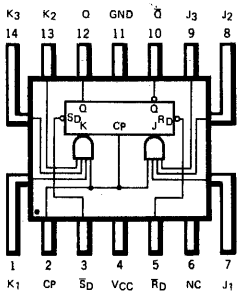
DESCRIPTION — The HSTTL/SSI 9H102/54102, 74H102 is a High Speed JK Negative Edge Triggered flip-flop. They feature gated JK inputs and an asynchronous clear input. The AND gate inputs are inhibited while the clock input is LOW; when the clock goes HIGH, the inputs are enabled and data will be accepted. Logic state of J and K inputs may be allowed to change when the clock pulse is in a HIGH state and bistable will perform according to the truth table as long as minimum set-up times are observed. Input data is transferred to the outputs on the negative edge of the clock pulse.

LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)

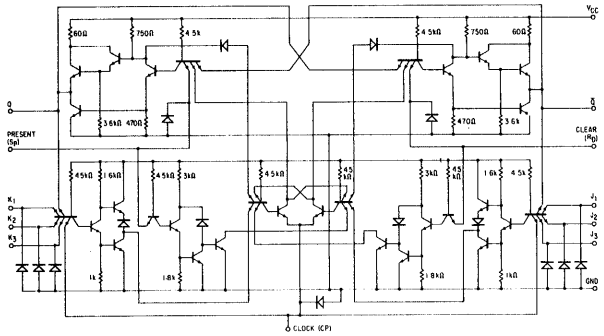


FLATPAK (TOP VIEW)



NC — No internal connection.

SCHEMATIC DIAGRAM



Positive logic:

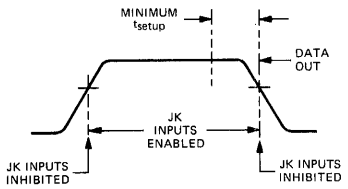
LOW input to preset sets Q to HIGH level
LOW input to clear sets Q to LOW level
Preset and clear are independent of clock

TRUTH TABLE

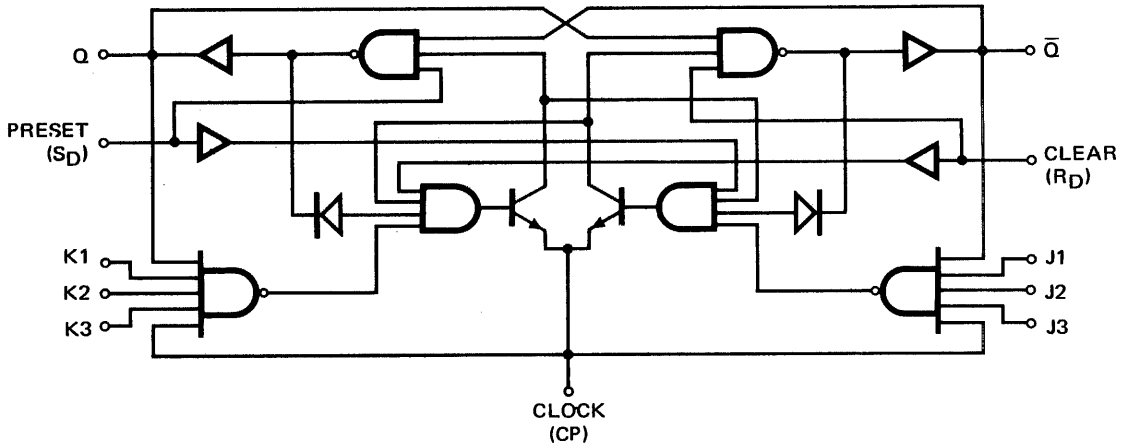
t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

NOTES:
J = J1·J2·J3
K = K1·K2·K3
t_n = Bit time before clock pulse
t_{n+1} = Bit time after clock pulse

CLOCK WAVEFORM



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

PARAMETER		9H102XM/54H102XM			9H102XC/74H102XC			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}		4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range		−55	25	125	0	25	70	°C
Fan Out from Each Output				12.5			12.5	U.L.
Width of Clock Pulse, $t_{p(clock)}$ (See Fig. W)		10			10			ns
Width of Preset Pulse, $t_{p(preset)}$ (See Fig. X)		15			15			ns
Width of Clear Pulse, $t_{p(clear)}$ (See Fig. X)		15			15			ns
Input Setup Time, t_{setup} (See Clock Waveform)	LOW Level	13			13			ns
	HIGH Level	10			10			
Input Hold Time, t_{hold}		0			0			
Clock Pulse Transition Time, t_0 (See Fig. W)				150			150	ns

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	TEST FIGURE
		MIN.	TYP. (Note 1)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH	41 & 42
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW	41 & 42
V_{OH}	Output HIGH Voltage	2.4	3.2		Volts	V_{CC} = MIN., I_{OH} = −0.5 mA	41
V_{OL}	Output LOW Voltage		0.25	0.4	Volts	V_{CC} = MIN., I_{OL} = 20 mA	42
I_{IH}	Input HIGH Current at J1, J2, J3 K1, K2, or K3			50	μA	V_{CC} = MAX., V_{IN} = 2.4 V	44
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
	Input HIGH Current at Clock	0		−1.0	mA	V_{CC} = MAX., V_{IN} = 2.4 V	44
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
	Input HIGH Current at Preset or Clear			100	μA	V_{CC} = MAX., V_{IN} = 2.4 V	44
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IL}	Input LOW Current at J1, J2, J3 K1, K2, K3, Preset, or Clear		−1.0	−2.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V	43
	Input LOW Current at Clock		−3.0	−4.8	mA	V_{CC} = MAX., V_{IN} = 0.4 V	43
I_{OS}	Output Short Circuit Current (Note 3)	−40		−100	mA	V_{CC} = MAX., V_{IN} = 0 V	45
I_{CC}	Supply Current		20	38	mA	V_{CC} = MAX.	44

SWITCHING CHARACTERISTICS (T_A = 25°)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
f_{CLOCK}	Maximum Clock Frequency	40	50		MHz	V_{CC} = 5.0 V C_L = 25 pF R_L = 280Ω	W
t_{PLH}	Turn Off Delay Preset to Output		8.0	12	ns		X
t_{PHL}	Turn On Delay Clear or Preset to Output (Clock LOW)		23	35	ns		X
t_{PHL}	Turn On Delay Clear or Preset to Output (Clock HIGH)		15	20	ns		X
t_{PLH}	Turn Off Delay Clock to Output	5.0	10	15	ns		W
t_{PHL}	Turn On Delay Clock to Output	8.0	16	20	ns		W

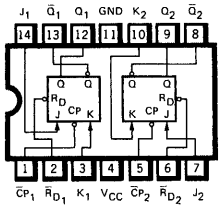
NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

DUAL JK EDGE TRIGGERED FLIP-FLOP WITH SEPARATE CLEARS AND CLOCKS

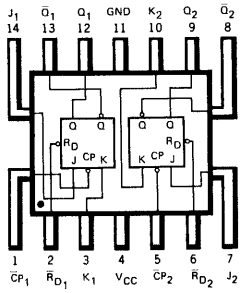
DESCRIPTION — The HSTTL/SSI 9H103/54H103, 74H103 is a High Speed JK Negative Edge Triggered flip-flop. They feature individual J, K, clock, and asynchronous clear inputs to each flip-flop. When the clock goes HIGH, the inputs are enabled and data will be accepted. Logic state of J and K inputs may be allowed to change when the clock pulse is in a HIGH state and bistable will perform according to the truth table as long as minimum set-up times are observed. Input data is transferred to the outputs on the negative edge of the clock pulse.

LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)

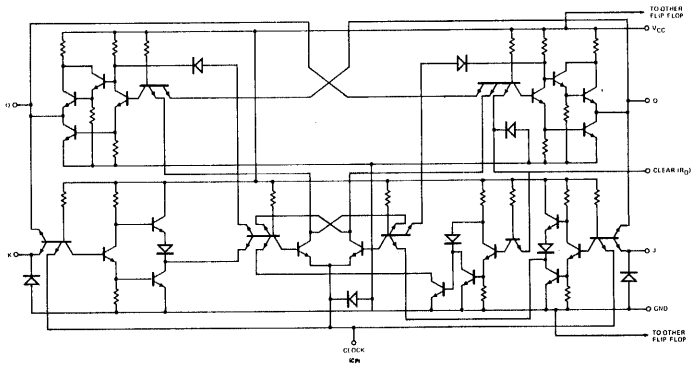


FLATPAK (TOP VIEW)



Positive logic: LOW input to clear sets Q to LOW level
Clear is independent of clock

SCHEMATIC DIAGRAM
(EACH FLIP-FLOP)

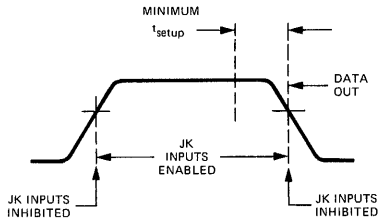


TRUTH TABLE

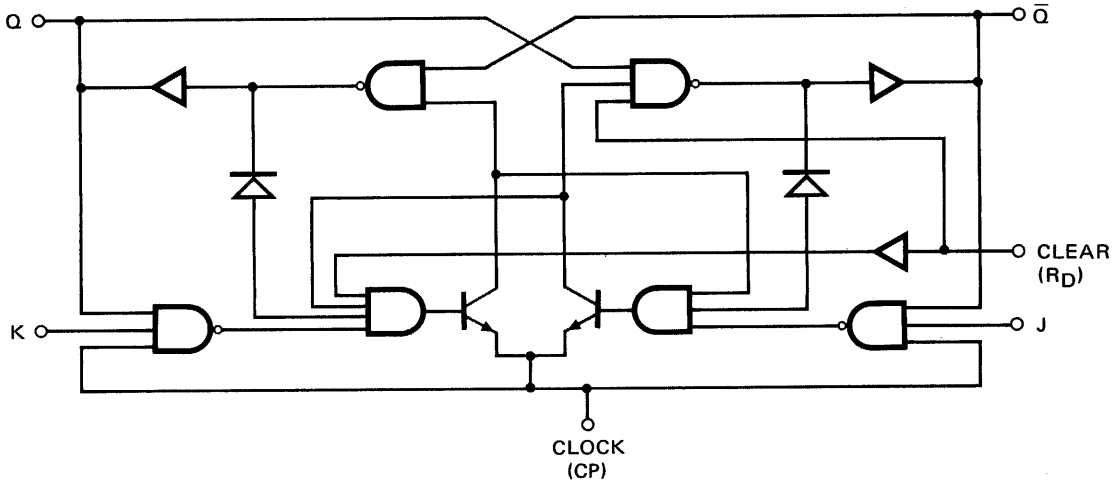
t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

NOTES:
t_n = Bit time before clock pulse
t_{n+1} = Bit time after clock pulse

CLOCK WAVEFORM



LOGIC DIAGRAM
(EACH FLIP-FLOP)



RECOMMENDED OPERATING CONDITIONS

PARAMETER		9H103XM/54H103XM			9H103XC/74H103XC			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}		4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range		−55	25	125	0	25	70	°C
Fan Out from Each Output				12.5			12.5	U.L.
Width of Clock Pulse, $t_{p(clock)}$ (See Fig. W)		10			10			ns
Width of Clear Pulse, $t_{p(clear)}$ (See Fig. X)		16			16			ns
Input Setup Time, t_{setup} (See Clock Waveform)	LOW Level	13			13			ns
	HIGH Level	10			10			
Input Hold Time, t_{hold}		0			0			
Clock Pulse Transition Time, t_0 (See Fig. W)				150			150	ns

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH	46 & 47
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW	46 & 47
V_{OH}	Output HIGH Voltage	2.4	3.2		Volts	V_{CC} = MIN., I_{OH} = −0.5 mA	46
V_{OL}	Output LOW Voltage		0.25	0.4	Volts	V_{CC} = MIN., I_{OL} = 20 mA	47
I_{IH}	Input HIGH Current at J or K			50	μA	V_{CC} = MAX., V_{IN} = 2.4 V	126
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
	Input HIGH Current at Clock	0		−1.0	mA	V_{CC} = MAX., V_{IN} = 2.4 V	126
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
	Input HIGH Current at Clear			100	μA	V_{CC} = MAX., V_{IN} = 2.4 V	126
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IL}	Input LOW Current at J, K, or Clear		−1.0	−2.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V	125
	Input LOW Current at Clock		−3.0	−4.8	mA	V_{CC} = MAX., V_{IN} = 0.4 V	125
I_{OS}	Output Short Circuit Current (Note 3)	−40		−100	mA	V_{CC} = MAX., V_{IN} = 0 V	50
I_{CC}	Supply Current		40	76	mA	V_{CC} = MAX.	126

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
f_{CLOCK}	Maximum Clock Frequency	40	50		MHz	V_{CC} = 5.0 V C_L = 25 pF R_L = 280Ω	W
t_{PLH}	Turn Off Delay Clear to Output		8.0	12	ns		X
t_{PHL}	Turn On Delay Clear to Output (Clock LOW)		23	35	ns		X
t_{PHL}	Turn On Delay Clear to Output (Clock HIGH)		15	20	ns		X
t_{PLH}	Turn Off Delay Clock to Output	5.0	10	15	ns		W
t_{PHL}	Turn On Delay Clock to Output	8.0	16	20	ns		W

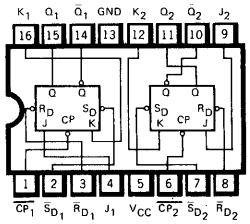
NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time and duration of short circuit test should not exceed 1 second.

DUAL JK EDGE TRIGGERED FLIP-FLOP WITH SEPARATE PRESETS, CLEARS AND CLOCKS

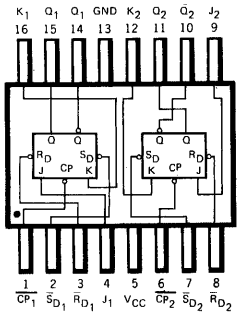
DESCRIPTION – The HSTTL/SSI 9H106/54H106, 74H106 is a High Speed JK Negative Edge Triggered flip-flop. They feature individual J, K, clock, and asynchronous preset and clear inputs to each flip-flop. When the clock goes HIGH, the inputs are enabled and data will be accepted. Logic state of J and K inputs may be allowed to change when the clock pulse is in a HIGH state and bistable will perform according to the truth table as long as minimum set up times are observed. Input data is transferred to the outputs on the negative edge of the clock pulse.

LOGIC AND CONNECTION DIAGRAM

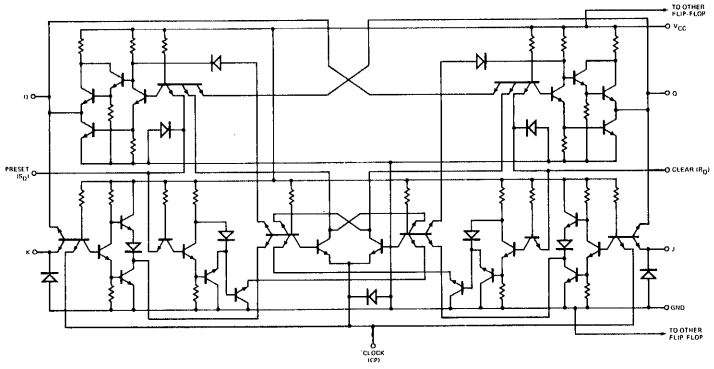
DIP (TOP VIEW)



FLATPAK (Top View)



SCHEMATIC DIAGRAM
(EACH FLIP-FLOP)



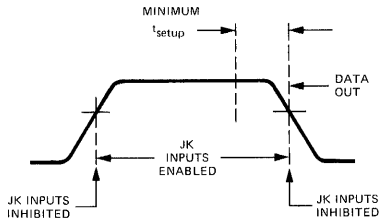
Positive logic: LOW input to preset sets Q to HIGH level
LOW input to clear sets Q to LOW level
Preset and clear are independent of clock

TRUTH TABLE

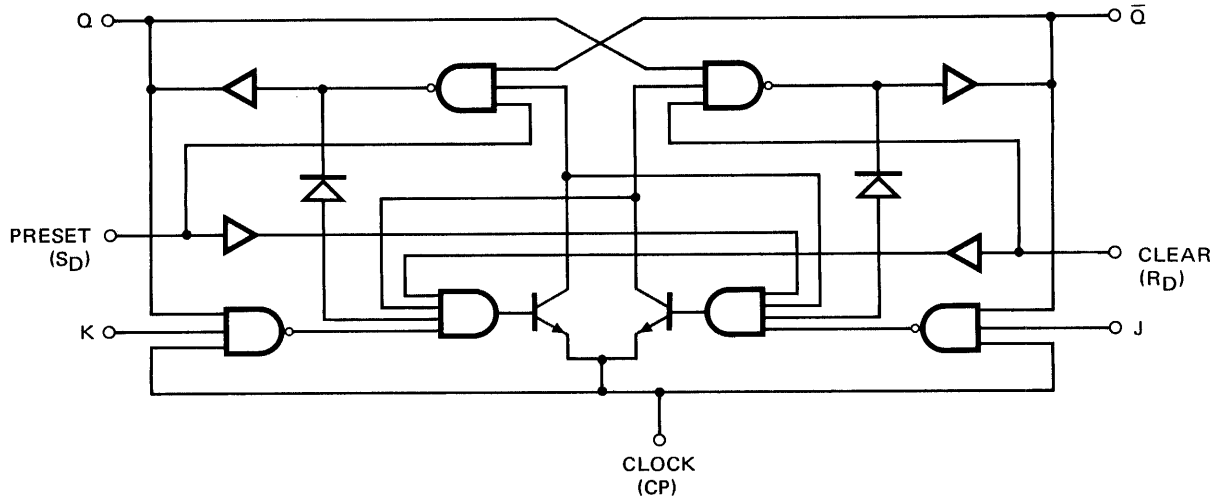
t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\bar{Q}_n$

NOTES:
t_n = Bit time before clock pulse
t_{n+1} = Bit time after clock pulse

CLOCK WAVEFORM



LOGIC DIAGRAM
(EACH FLIP-FLOP)



RECOMMENDED OPERATING CONDITIONS

PARAMETER		9H106XM/54H106XM			9H106XC/74H106XC			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}		4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range		−55	25	125	0	25	70	°C
Fan Out from Each Output				12.5			12.5	U.L.
Width of Clock Pulse, $t_{p(clock)}$ (See Fig. W)		10			10			ns
Width of Preset Pulse, $t_{p(preset)}$ (See Fig. X)		16			16			ns
Width of Clear Pulse, $t_{p(clear)}$ (See Fig. X)		16			16			ns
Input Setup Time, t_{setup} (See Clock Waveform)	LOW Level	13			13			ns
	HIGH Level	10			10			
Input Hold Time, t_{hold}		0			0			
Clock Pulse Transition Time, t_0 (See Fig. W)				150			150	ns

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH	46 & 47
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW	46 & 47
V_{OH}	Output HIGH Voltage	2.4	3.2		Volts	V_{CC} = MIN., I_{OH} = −0.5 mA	46
V_{OL}	Output LOW Voltage		0.25	0.4	Volts	V_{CC} = MIN., I_{OL} = 20 mA	47
I_{IH}	Input HIGH Current at J or K			50	µA	V_{CC} = MAX., V_{IN} = 2.4 V	126
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
	Input HIGH Current at Clock	0		−1.0	mA	V_{CC} = MAX., V_{IN} = 2.4 V	126
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
	Input HIGH Current at Preset or Clear			100	µA	V_{CC} = MAX., V_{IN} = 2.4 V	126
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IL}	Input LOW Current at J, K, Preset, or Clear		−1.0	−2.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V	125
	Input LOW Current at Clock		−3.0	−4.8	mA	V_{CC} = MAX., V_{IN} = 0.4 V	125
I_{OS}	Output Short Circuit Current (Note 3)	−40		−100	mA	V_{CC} = MAX., V_{IN} = 0 V	51
I_{CC}	Supply Current		40	76	mA	V_{CC} = MAX.	126

SWITCHING CHARACTERISTICS (T_A = 25°)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
f_{CLOCK}	Maximum Clock Frequency	40	50		MHz	V_{CC} = 5.0 V C_L = 25 pF R_L = 280Ω	W
t_{PLH}	Turn Off Delay Preset or Clear to Output		8.0	12	ns		X
t_{PHL}	Turn On Delay Clear or Preset to Output (Clock LOW)		23	35	ns		X
t_{PHL}	Turn On Delay Clear or Preset to Output (Clock HIGH)		15	20	ns		X
t_{PLH}	Turn Off Delay Clock to Output	5.0	10	15	ns		W
t_{PHL}	Turn On Delay Clock to Output	8.0	16	20	ns		W

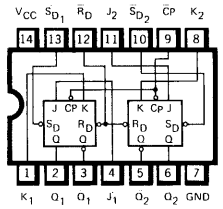
NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time and duration of short circuit test should not exceed 1 second.

DUAL JK EDGE TRIGGERED FLIP-FLOP WITH SEPARATE PRESETS AND A COMMON CLEAR AND CLOCK

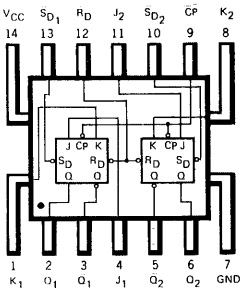
DESCRIPTION — The HSTTL/SSI 9H108/54H108, 74H108 is a High Speed JK Negative Edge Triggered flip-flop. They feature individual J,K, and asynchronous preset inputs to each flip-flop as well as common clock and asynchronous clear inputs. When the clock goes HIGH, the inputs are enabled and data will be accepted. Logic state of J and K inputs may be allowed to change when the clock pulse is in a HIGH state and bistable will perform according to the truth table as long as minimum set-up times are observed. Input data is transferred to the outputs on the negative edge of the clock pulse.

LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)

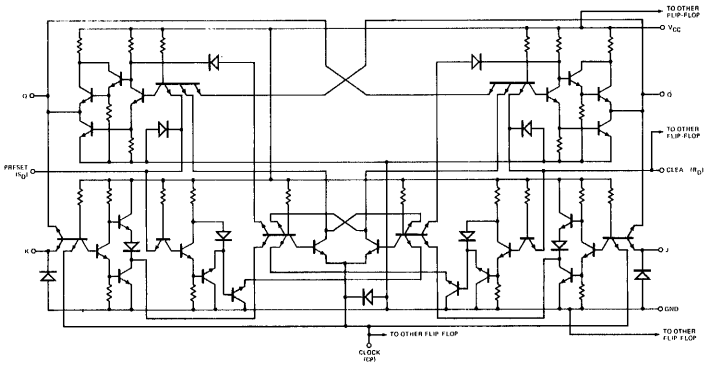


FLATPAK (TOP VIEW)



Positive logic: LOW input to preset sets Q to HIGH level
LOW input to clear sets Q to LOW level
Preset and clear are independent of clock

SCHEMATIC DIAGRAM
(EACH FLIP–FLOP)

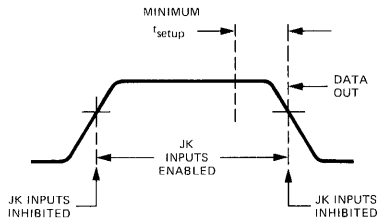


TRUTH TABLE

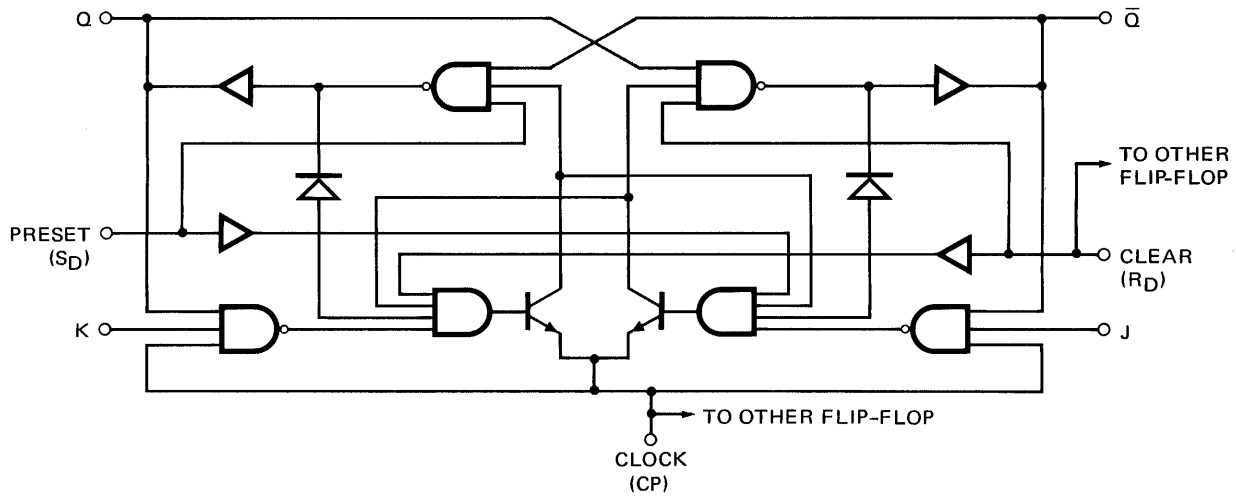
t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

NOTES:
t_n = Bit time before clock pulse
t_{n+1} = Bit time after clock pulse

CLOCK WAVEFORM



LOGIC DIAGRAM
(EACH FLIP–FLOP)



RECOMMENDED OPERATING CONDITIONS

PARAMETER		9H108XM/54H108XM			9H108XC/74H108XC			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}		4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range		–55	25	125	0	25	70	°C
Fan Out from Each Output				12.5			12.5	U.L.
Width of Clock Pulse, $t_{p(clock)}$ (See Fig. W)		10			10			ns
Width of Preset Pulse, $t_{p(preset)}$ (See Fig. X)		15			15			ns
Width of Clear Pulse, $t_{p(clear)}$ (See Fig. X)		16			16			ns
Input Setup Time, t_{setup} (See Clock Waveform)	LOW Level	13			13			ns
	HIGH Level	10			10			
Input Hold Time, t_{hold}		0			0			
Clock Pulse Transition Time, t_0 (See Fig. W)				150			150	ns

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH	46 & 47
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW	46 & 47
V_{OH}	Output HIGH Voltage	2.4	3.2		Volts	V_{CC} = MIN., I_{OH} = –0.5 mA	46
V_{OL}	Output LOW Voltage		0.25	0.4	Volts	V_{CC} = MIN., I_{OL} = 20 mA	47
I_{IH}	Input HIGH Current at J or K			50	µA	V_{CC} = MAX., V_{IN} = 2.4 V	126
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
	Input HIGH Current at Clock	0		–1.0	mA	V_{CC} = MAX., V_{IN} = 2.4 V	126
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
	Input HIGH Current at Preset			100	µA	V_{CC} = MAX., V_{IN} = 2.4 V	126
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
	Input HIGH Current at Clear			200	µA	V_{CC} = MAX., V_{IN} = 2.4 V	126
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IL}	Input LOW Current at J, K, or Preset		–1.0	–2.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V	125
	Input LOW Current at Clock		–6.0	–9.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V	125
	Input LOW Current at Clear		–2.0	–4.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V	125
I_{OS}	Output Short Circuit Current (Note 3)	–40		–100	mA	V_{CC} = MAX., V_{IN} = 0 V	51
I_{CC}	Supply Current		40	76	mA	V_{CC} = MAX.	126

SWITCHING CHARACTERISTICS (T_A = 25°C)

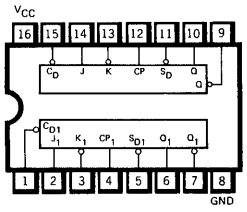
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
f_{CLOCK}	Maximum Clock Frequency	40	50		MHz	V_{CC} = 5.0 V C_L = 25 pF R_L = 280Ω	W
t_{PLH}	Turn Off Delay Preset or Clear to Output		8.0	12	ns		X
t_{PHL}	Turn On Delay Clear or Preset to Output (Clock LOW)		23	35	ns		X
t_{PHL}	Turn On Delay Clear or Preset to Output (Clock HIGH)		15	20	ns		X
t_{PLH}	Turn Off Delay Clock to Output	5.0	10	15	ns		W
t_{PHL}	Turn On Delay Clock to Output	8.0	16	20	ns		W

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time and duration of short circuit test should not exceed 1 second.

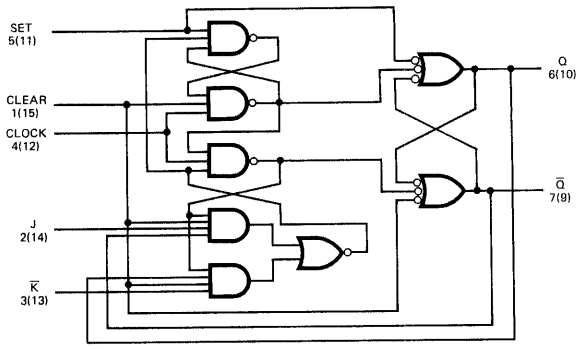
DUAL J$\overline{K}$ FLIP-FLOP

DESCRIPTION — The 9S109 consists of two high speed, completely independent transition clocked J$\overline{K}$ flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The J$\overline{K}$ design allows operation as a D flip-flop by simply connecting the J and $\overline{K}$ pins together. The 9S109 is a pin for pin replacement of the 9024.

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



LOGIC DIAGRAM



TRUTH TABLES

SYNCHRONOUS ENTRY D MODE OPERATION

INPUTS AT t_n	OUTPUTS AT t_{n+1}	
D	Q	$\overline{Q}$
L	L	H
H	H	L

SYNCHRONOUS ENTRY J-$\overline{K}$ MODE OPERATION

INPUTS AT t_n		OUTPUTS AT t_{n+1}	
J	$\overline{K}$	Q	$\overline{Q}$
L	H	No Change	
L	L	L	H
H	H	H	L
H	L	Toggles	

ASYNCHRONOUS ENTRY INDEPENDENT OF CLOCK & SYNCHRONOUS INPUTS

INPUTS		OUTPUTS	
$\overline{S}_D$	$\overline{C}_D$	Q	$\overline{Q}$
L	L	H	H
L	H	H	L
H	L	L	H
H	H	No Change	

L = LOW Logic Level
H = HIGH Logic Level

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9S109XM			9S109XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	/5	°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER		LIMITS MIN.	LIMITS TYP. (Note 2)	LIMITS MAX.	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			Volts	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage				0.8	Volts	Guaranteed Input LOW Voltage
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.2	Volts	V_{CC} = MIN., I_I = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		Volts	V_{CC} = MIN., I_{OH} = −1.0 mA
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage			0.35	0.5	Volts	V_{CC} = MIN., I_{OL} = 20 mA
I_{IH}	Input HIGH Current at	J$\overline{K}$		1.0	50	µA	V_{CC} = MAX., V_{IN} = 2.7 V
		$\overline{S}_D$		2.0	100		
		$\overline{C}_D$		4.0	200		
I_{IL}	Input LOW Current at	J$\overline{K}$		−1.4	−2.0	mA	V_{CC} = MAX., V_{IN} = 0.5 V
		$\overline{S}_D$		−2.8	−4.0		
		$\overline{C}_D$		−5.6	−8.0		
I_{OS}	Output Short Circuit Current (Note 3)		−40	−65	−100	mA	V_{CC} = MAX., V_{OUT} = 0V
I_{CC}	Supply Current			32	52	mA	V_{CC} = MAX., (Note 4)

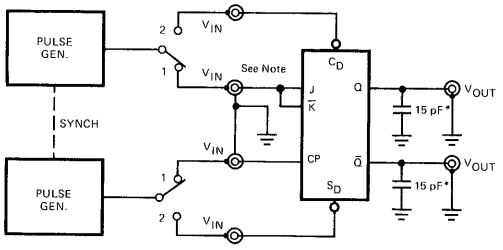
Notes on following page

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN.	TYP.	MAX.		
f_{max}	Maximum Clock Frequency		100		MHz	V_{CC} = 5.0 V, C_L = 15 pF
t_{PLH}	Turn Off Delay Clear or Preset to Output		4.0		ns	
t_{PHL}	Turn On Delay Clear or Preset to Output		7.0		ns	
t_{PLH}	Turn Off Delay Clock to Output		7.0		ns	
t_{PHL}	Turn On Delay Clock to Output		7.0		ns	

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.
(4) I_{CC} is measured Clock, Set and $\overline{K}$ inputs grounded.

SWITCHING CHARACTERISTICS



*Includes all probe and jig capacitance.

NOTE: For testing 9S109, connect J,$\overline{K}$ pins together to form a D input.

PULSE GENERATOR SETTINGS

CLOCK

f ≈ 1 MHz
$t_f = t_r$ = 2.5 ns
Amp = 0 to 3 V
Duty cycle = 50%

J$\overline{K}$

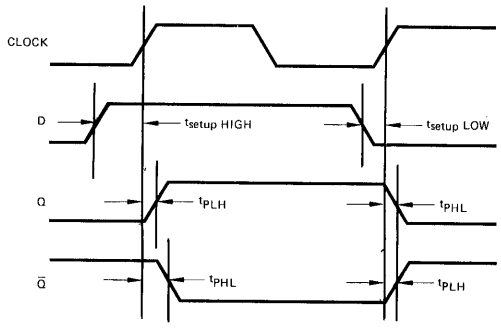
f ≈ 500 kHz
$t_f = t_r$ = 2.5 ns
Amp = 0 to 3 V
t_{setup} (HIGH)
t_{setup} (LOW)
Duty cycle = Adjust pulse width to attain t_{setup} (HIGH) and t_{setup} (LOW) relative to clock as shown in waveforms.

DIRECT SET, CLEAR

f ≈ 1 MHz
$t_f = t_r$ = 2.5 ns
Amp = 0 to 3 V
Duty cycle = Adjust pulse width and synch to attain waveforms shown.

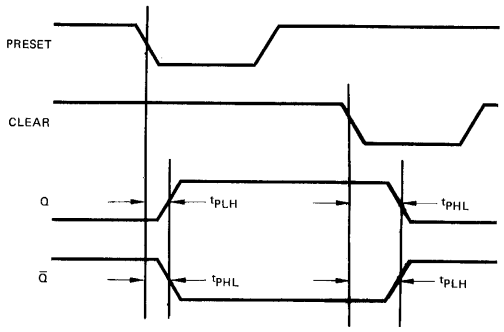
SWITCHING WAVEFORMS

CLOCK TO OUTPUT DELAY†



SWITCH IN POSITION 1

DIRECT SET, AND CLEAR TO OUTPUT DELAY



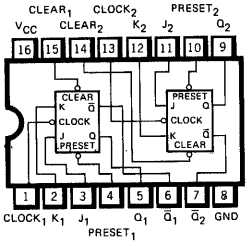
SWITCH IN POSITION 2

†Direct set and clear inputs connected to V_{CC} thru 2 kΩ resistor during test.

DUAL JK EDGE-TRIGGERED FLIP-FLOP

DESCRIPTION — The 9S112/54S112, 74S112 dual JK flip-flops feature individual J, K, clock, and asynchronous preset and clear inputs to each flip-flop. When the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will perform according to the truth table as long as minimum setup and hold time are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



Positive logic: LOW input to preset sets Q to HIGH level.
LOW input to clear resets Q to LOW level.
Clear and preset are independent of clock.

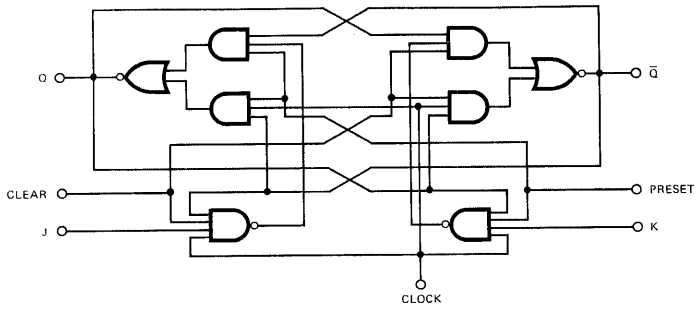
TRUTH TABLES

t_n		t_n+1
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\bar{Q}_n$

Preset	Clear	Q	$\bar{Q}$
L	L	H	H
L	H	H	L
H	L	L	H
H	H	No Change	

NOTES:
A. t_n = Bit time before clock pulse.
B. t_n+1 = Bit time after clock pulse.

LOGIC DIAGRAM
(Each Flip-Flop)



RECOMMENDED OPERATING CONDITIONS

PARAMETER	9S112XM/54S112XM			9S112XC/74S112XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	75	°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER		LIMITS MIN.	LIMITS TYP. (Note 2)	LIMITS MAX.	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			Volts	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage				0.8	Volts	Guaranteed Input LOW Voltage
V_{CD}	Input Clamp Diode Voltage			−0 65	−1.2	Volts	V_{CC} = MIN., I_I = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		Volts	V_{CC} = MIN., I_{OH} = −1.0 mA
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage			0.35	0.5	Volts	V_{CC} = MIN., I_{OL} = 20 mA
I_{IH}	Input HIGH Current at	J,K		1.0	50	µA	V_{CC} = MAX., V_{IN} = 2.7 V
		Clock Preset Clear		2.0	100		
I_{IL}	Input LOW Current at	J,K		−0.96	−1.6	mA	V_{CC} = MAX., V_{IN} = 0.5 V
		Clock		−2.8	−4.0		
		Preset Clear		−4.9	−7.0		
I_{OS}	Output Short Circuit Current (Note 3)		−40	−65	−100	mA	V_{CC} = MAX., V_{OUT} = 0V
I_{CC}	Supply Current			30	50	mA	V_{CC} = MAX. (Note 4)

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS
f_{max}	Maximum Clock Frequency	80	125		MHz	V_{CC} = 5.0 V, C_L = 15 pF
t_{PLH}	Turn Off Delay Clear or Preset to Output			7.0	ns	
t_{PHL}	Turn On Delay Clear or Preset to Output			7.0	ns	
t_{PLH}	Turn Off Delay Clock to Output			7.0	ns	
t_{PHL}	Turn On Delay Clock to Output			7.0	ns	

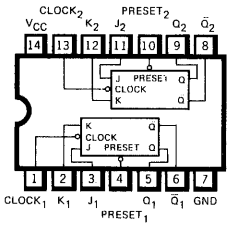
NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.
(4) I_{CC} is measured with outputs open, clock grounded and J,K, preset and clear at 4.5 V.

5

DUAL JK EDGE-TRIGGERED FLIP-FLOP

DESCRIPTION — The 9S113/54S113, 74S113 offer individual J, K, preset, and clock inputs. These monolithic dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will perform according to the truth table as long as minimum setup times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



Positive logic: LOW input to preset sets Q to HIGH level
Preset is independent of clock

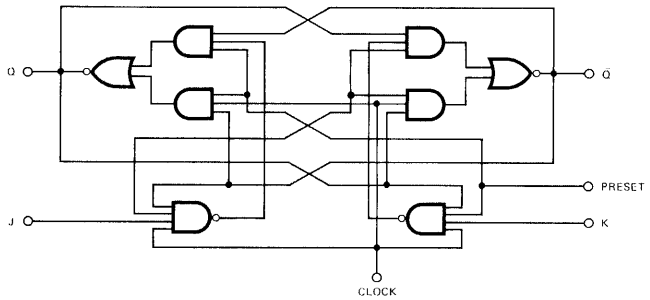
TRUTH TABLES

t_n		t_n+1
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\bar{Q}_n$

Preset	Q	$\bar{Q}$
L	H	L
H	No Change	

NOTES:
A. t_n = Bit time before clock pulse.
B. t_n+1 = Bit time after clock pulse.

LOGIC DIAGRAM
(Each Flip-Flop)



RECOMMENDED OPERATING CONDITIONS

PARAMETER	9S113XM/54S113XM			9S113XC/74S113XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	75	°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER		LIMITS MIN.	LIMITS TYP. (Note 2)	LIMITS MAX.	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			Volts	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage				0.8	Volts	Guaranteed Input LOW Voltage
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.2	Volts	V_{CC} = MIN., I_I = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		Volts	V_{CC} = MIN., I_{OH} = −1.0 mA
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage			0.35	0.5	Volts	V_{CC} = MIN., I_{OL} = 20 mA
I_{IH}	Input HIGH Current at	J,K		1.0	50	μA	V_{CC} = MAX., V_{IN} = 2.7 V
		Clock		2.0	100		
		Preset		2.0	100		
I_{IL}	Input LOW Current at	J,K		−0.96	−1.6	mA	V_{CC} = MAX., V_{IN} = 0.5 V
		Clock		−2.8	−4.0		
		Preset		−4.9	−7.0		
I_{OS}	Output Short Circuit Current (Note 3)		−40	−65	−100	mA	V_{CC} = MAX., V_{OUT} = 0V
I_{CC}	Supply Current			30	50	mA	V_{CC} = MAX. (Note 4)

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS
f_{max}	Maximum Clock Frequency	80	125		MHz	V_{CC} = 5.0 V, C_L = 15 pF
t_{PLH}	Turn Off Delay Clear or Preset to Output			7.0	ns	
t_{PHL}	Turn On Delay Clear or Preset to Output			7.0	ns	
t_{PLH}	Turn Off Delay Clock to Output			7.0	ns	
t_{PHL}	Turn On Delay Clock to Output			7.0	ns	

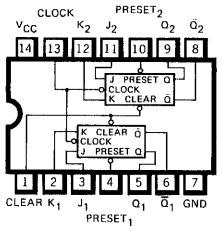
NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.
(4) I_{CC} is measured with outputs open, clock grounded and J,K, preset and clear at 4.5 V.

5

DUAL JK EDGE-TRIGGERED FLIP-FLOP

DESCRIPTION — The 9S114/54S114, 74S114 offer common clock and common clear inputs and individual J, K, and preset inputs. These monolithic dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will perform according to the truth table as long as minimum setup times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



Positive logic: LOW input to preset sets Q to HIGH level.
LOW input to clear resets Q to LOW level.
Preset and clear are independent of clock.

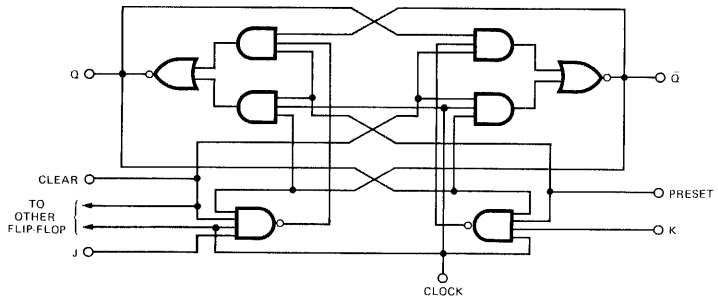
TRUTH TABLES

t_n		t_n+1
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\bar{Q}_n$

Preset	Clear	Q	$\bar{Q}$
L	L	H	H
L	H	H	L
H	L	L	H
H	H	No Change	

NOTES:
A. t_n = Bit time before clock pulse.
B. t_n+1 = Bit time after clock pulse.

LOGIC DIAGRAM
(Each Flip-Flop)



RECOMMENDED OPERATING CONDITIONS

PARAMETER	9S114XM/54S114XM			9S114XC/74S114XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	75	°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER		LIMITS MIN.	LIMITS TYP. (Note 2)	LIMITS MAX.	UNITS	TEST CONDITIONS (Note 2)
V_{IH}	Input HIGH Voltage		2.0			Volts	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage				0.8	Volts	Guaranteed Input LOW Voltage
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.2	Volts	V_{CC} = MIN., I_I = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		Volts	V_{CC} = MIN., I_{OH} = −1.0 mA
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage			0.35	0.5	Volts	V_{CC} = MIN., I_{OL} = 20 mA
I_{IH}	Input HIGH Current at	JK		1.0	50	μA	V_{CC} = MAX., V_{IN} = 2.7 V
		Clock		4.0	200		
		Preset		2.0	100		
		Clear		4.0	200		
I_{IL}	Input LOW Current at	JK		−0.96	−1.6	mA	V_{CC} = MAX., V_{IN} = 0.5 V
		Clock		−5.6	−8.0		
		Preset		−4.9	−7.0		
		Clear		−9.8	−14		
I_{OS}	Output Short Circuit Current (Note 3)		−40	−65	−100	mA	V_{CC} = MAX., V_{OUT} = 0V
I_{CC}	Supply Current			30	50	mA	V_{CC} = MAX. (Note 4)

SWITCHING CHARACTERISTICS (T_A = 25° C)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS
f_{max}	Maximum Clock Frequency	80	125		MHz	V_{CC} = 5.0 V, C_L = 15 pF
t_{PLH}	Turn Off Delay Clear or Preset to Output			7.0	ns	
t_{PHL}	Turn On Delay Clear or Preset to Output			7.0	ns	
t_{PLH}	Turn Off Delay Clock to Output			7.0	ns	
t_{PHL}	Turn On Delay Clock to Output			7.0	ns	

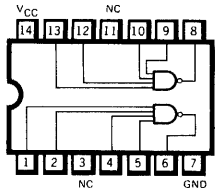
Notes:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.
(4) I_{CC} is measured with outputs open, clock grounded and J, K, preset and clear at 4.5 V.

5

DUAL 4-INPUT NAND LINE DRIVER

LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)

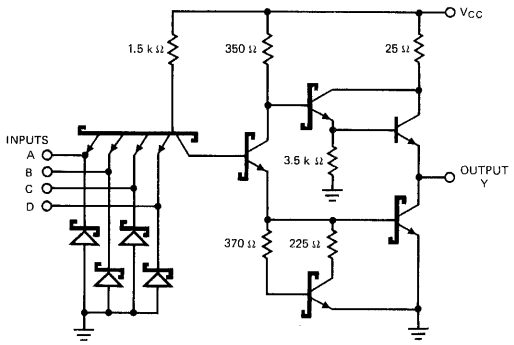


Positive logic: $Y = \overline{ABCD}$

NC—No internal connection.

SCHEMATIC DIAGRAM

(EACH GATE)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9S140XM/54S140XM			9S140XC/74S140XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	75	°C
Fan Out From Each Output			37.5*			37.5*	U.L.

*37.5 (U.L.) is the LOW drive factor and 75 (U.L.) is the HIGH drive factor.
X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER		LIMITS MIN.	LIMITS TYP. (Note 2)	LIMITS MAX.	UNITS	TEST CONDITIONS (Note 1)	
V_{IH}	Input HIGH Voltage		2.0			Volts	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	Volts	Guaranteed Input LOW Voltage	
V_{CD}	Input Clamp Diode Voltage			–0.65	–1.2	Volts	V_{CC} = MIN., I_{IN} = -18mA	
V_{OH}	Output HIGH Voltage	XM	2.0	2.8		Volts	V_{CC} = MIN., V_{IN} = 0.5V, R_0 = 50Ω to Gnd	
		XC	2.0	2.8				
V_{OL}	Output LOW Voltage			0.4	0.5	Volts	V_{CC} = MIN., I_{OL} = 60mA, V_{IN} = 2.0V	
I_{IH}	Input HIGH Current			1.0	100	μA	V_{CC} = MAX., V_{IN} = 2.7V	Each Input
					1.0	mA	V_{CC} = MAX., V_{IN} = 5.5V	
I_{IL}	Input LOW Current			–2.5	–4.0	mA	V_{CC} = MAX., V_{IN} = 0.5V	Each Input
I_{OS}	Output Short Circuit Current (Note 3)		–50	–150	–225	mA	V_{CC} = MAX., V_{OUT} = 0V	
I_{CCH}	Supply Current HIGH			8.2	18.0	mA	V_{CC} = MAX., V_{IN} = 0V	
I_{CCL}	Supply Current LOW			27.2	44.0	mA	V_{CC} = MAX., Inputs Open	

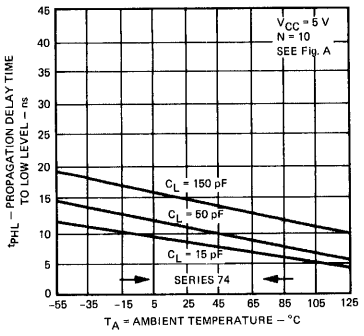
SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS	TEST FIGURES
t_{PLH}	Turn Off Delay Input to Output	2.0	4.0	6.5	ns	V_{CC} = 5.0V, C_L = 50pF	DD
t_{PHL}	Turn On Delay Input to Output	2.0	4.0	6.5	ns		

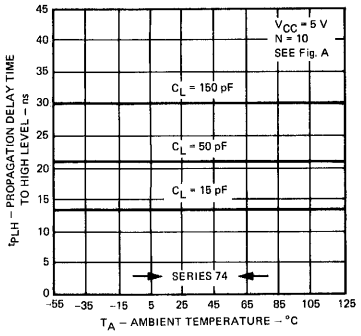
NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0V, 25°C.
(3) Not more than one output should be shorted at a time.

9N/54,74
TYPICAL CHARACTERISTICS*

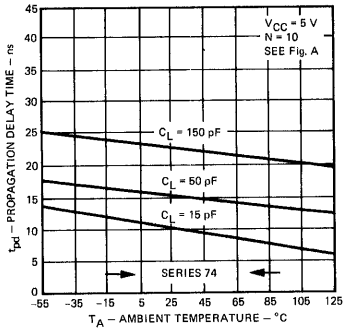
PROPAGATION DELAY TIME TO LOW LEVEL VERSUS AMBIENT TEMPERATURE



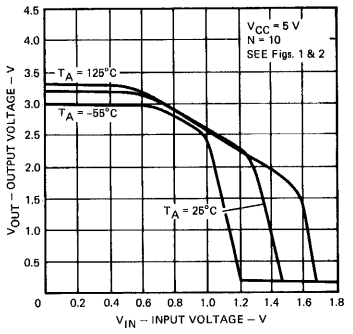
PROPAGATION DELAY TIME TO HIGH LEVEL VERSUS AMBIENT TEMPERATURE



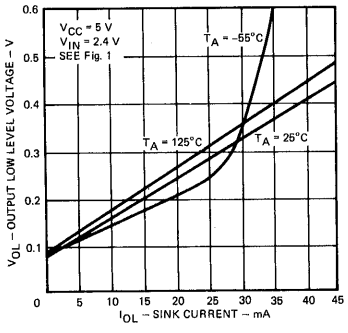
PROPAGATION DELAY TIME VERSUS AMBIENT TEMPERATURE



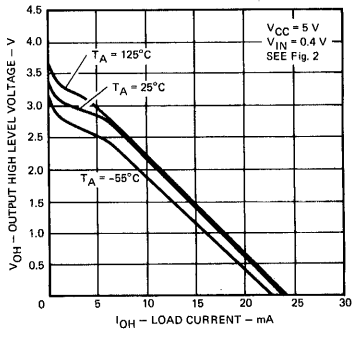
OUTPUT VOLTAGE VERSUS INPUT VOLTAGE



LOW LEVEL OUTPUT VOLTAGE VERSUS SINK CURRENT



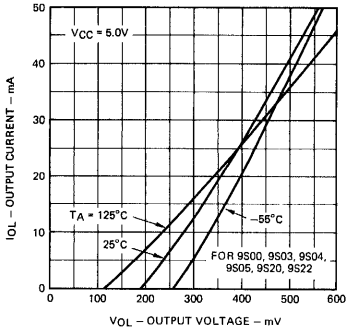
HIGH LEVEL OUTPUT VOLTAGE VERSUS LOAD CURRENT



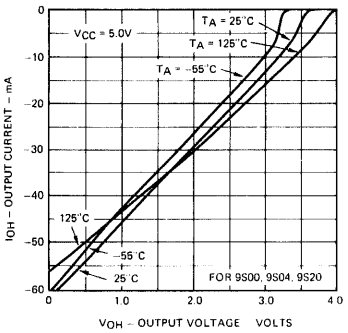
*Unless otherwise noted, data as shown is applicable for: 9N00/5400, 7400; 9N02/5402, 7402; 9N04/5404, 7404; 9N10/5410, 7410; 9N20/5420, 7420; 9N30/5430, 7430; 9N50/5450, 7450; 9N51/5451, 7451; 9N53/5453, 7453; 9N54/5454, 7454.

9S/54S,74S
TYPICAL INPUT AND OUTPUT CHARACTERISTICS

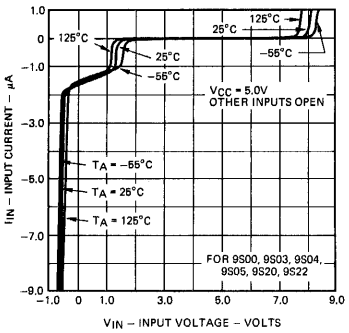
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)



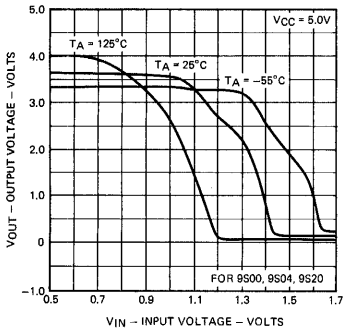
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)



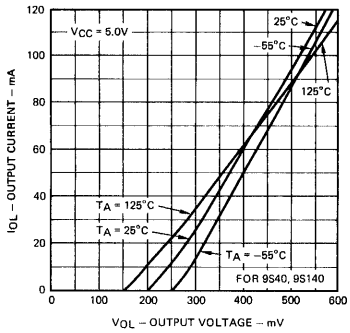
INPUT CURRENT VERSUS INPUT VOLTAGE



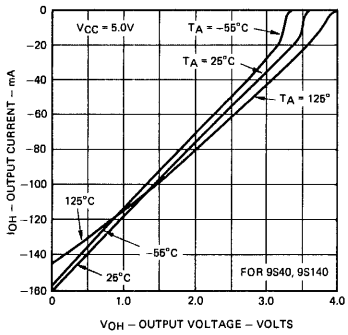
OUTPUT VOLTAGE VERSUS INPUT VOLTAGE



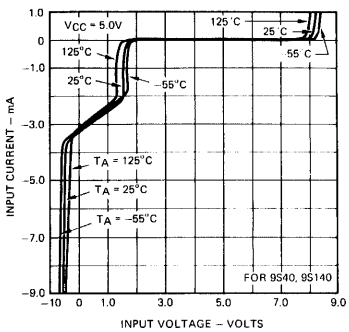
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)



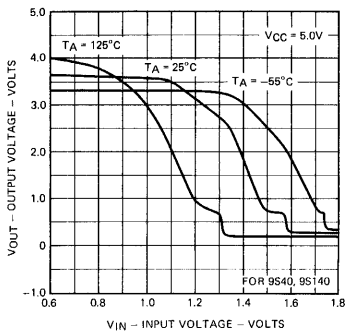
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)



INPUT CURRENT VERSUS INPUT VOLTAGE

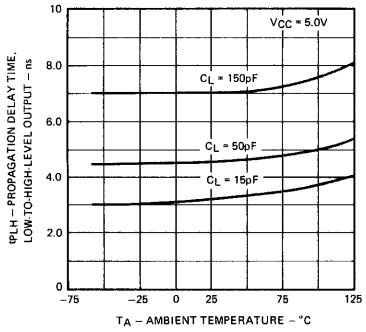


OUTPUT VOLTAGE VERSUS INPUT VOLTAGE

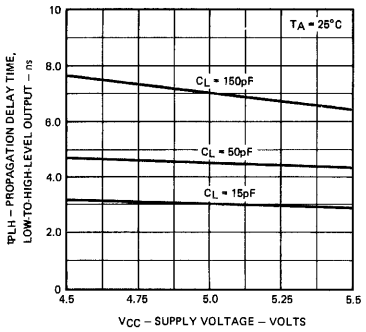


TYPICAL PROPAGATION DELAY TIME CHARACTERISTICS
FOR 9S GATES, BUFFER, AND INVERTER

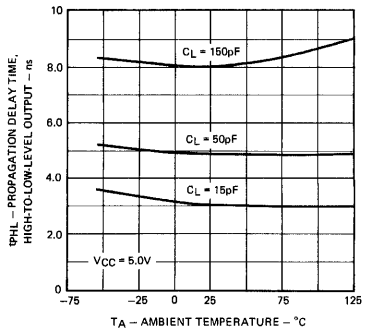
PROPAGATION DELAY TIME, LOW-TO-HIGH-LEVEL OUPUT VERSUS FREE-AIR TEMPERATURE



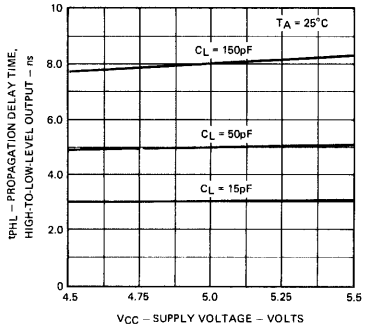
PROPAGATION DELAY TIME, LOW-TO-HIGH-LEVEL OUTPUT VERSUS SUPPLY VOLTAGE



PROPAGATION DELAY TIME, HIGH-TO-LOW-LEVEL OUTPUT VERSUS FREE-AIR TEMPERATURE



PROPAGATION DELAY TIME, HIGH-TO-LOW LEVEL OUTPUT VERSUS SUPPLY VOLTAGE



POWER DISSIPATION PER GATE VERSUS FREQUENCY