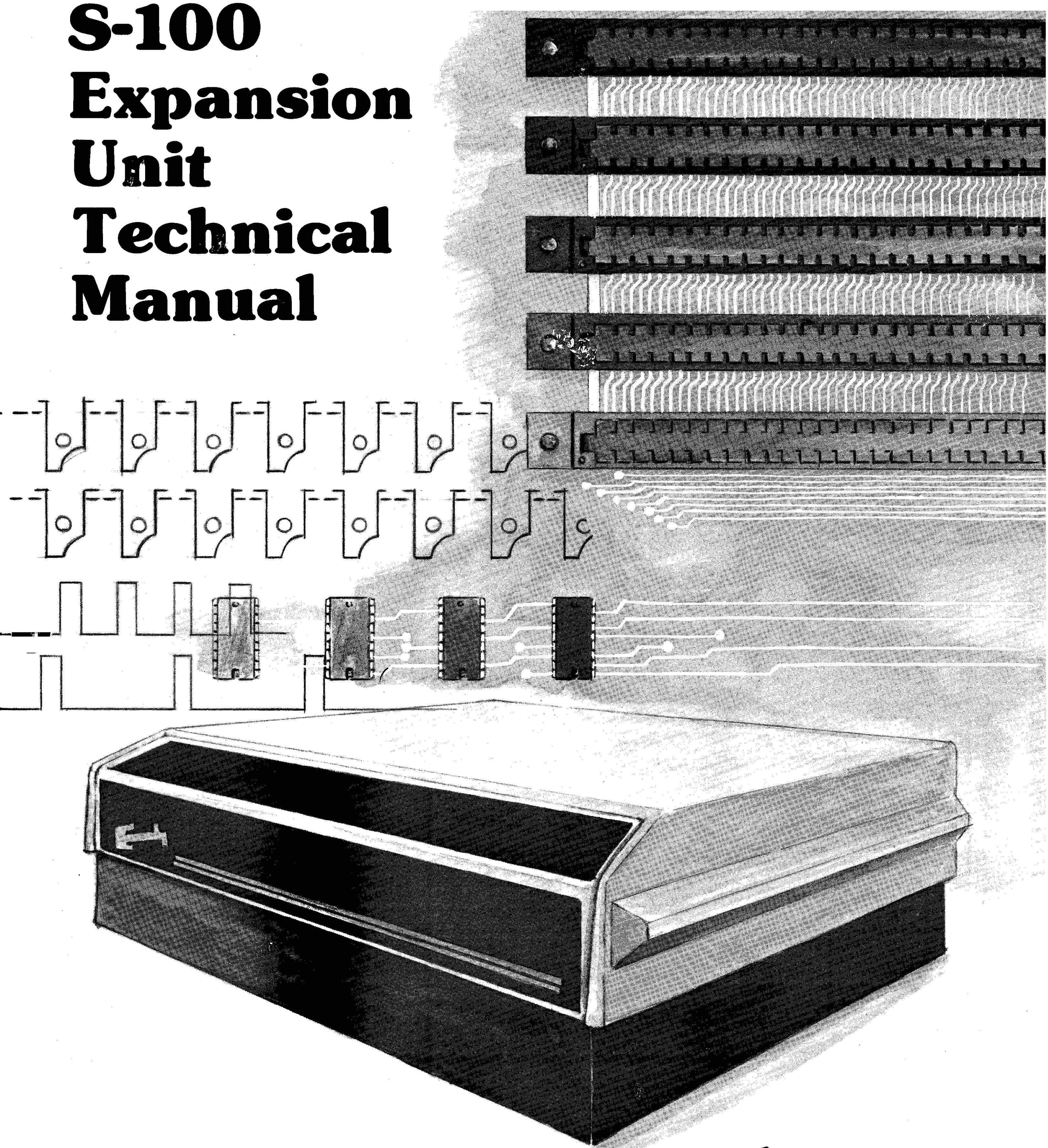
S-100 Expansion Unit Technical Manual



By the Sorcerer of Exidy inc.

390 Java Drive
Sunnyvale, California 94086

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FOREWORD

The S-100 bus is a collection of 100 information lines which carry address, data, status, control and power signals between a microcomputer (such as the Sorcerer) and other computers or special devices (such as memory expansion cards, music synthesizers, input/output devices, etc.). The Exidy S-100 Expansion Unit lets your Sorcerer use this bus to communicate with as many as six different devices.

An industry standard for the S-100 bus has recently been proposed; previously, each manufacturer used his own version, although these versions are all generally compatible. Table 2 lists the pinouts for both the Exidy S-100 bus and the standard S-100 bus proposed by a committee of the Institute of Electrical and Electronics Engineers (IEEE). The timing diagrams starting on page 8 give the complete signal timing for the bus, for users who wish to design their own S-100 devices.

Use the performance tests on page 14B to determine whether your S-100 Expansion Unit is working properly. However, the diagnostic tests starting on page 14A are intended for experienced service technicians. We strongly recommend that owners not attempt to service their own units.

NOTE

All service should be done by an authorized Exidy dealer; unauthorized service will void our warranty.

We refer to an IC device by its location on the board. Thus, 1A is the device in column 1, row A of the board.

We refer to a pin of an IC device (and sometimes the signal at that pin) by a hyphenated number following the location. Thus, 1A-5 is pin 5 of device 1A.

If an IC chip contains more than one device, we refer to each by one of its pins. Thus, 1A-5 also designates one of the devices on chip 1A — the one containing pin 5. Context will make clear whether a designation such as 1A-5 refers to a pin or to a device.

MECHANICAL LAYOUT

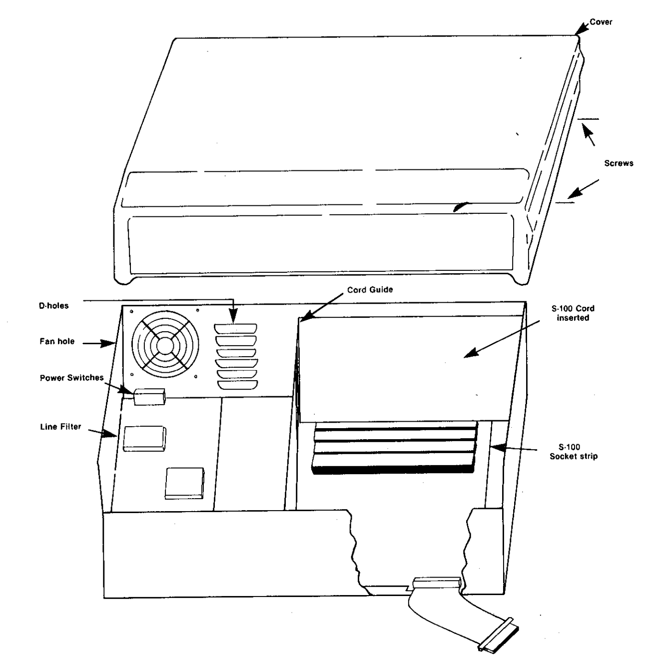
To open the S-100 Expansion Unit, unscrew the four screws that secure the cover (two on each side) and lift the cover off. To insert an S-100 card into an empty slot, fit the side edges of the card into the plastic guides, with the card's edge connector down, and its components facing toward the front of the S-100 unit. Then lower the card and push its edge connector firmly into the female edge connector on the mother board. ***Do not force.*** To remove an S-100 card, simply lift it out of the slot.

In time the contacts may loosen in a female connector. This causes no trouble when a card is in the connector, but when there is no card in place, the contacts on opposite sides of the connector may touch, shorting two bus lines together. If this happens, insert a strip of cardboard into the connector to keep the pins apart.

The 4.5" round hole in the back of the chassis is for a fan. If you decide you need one, use a standard 4.7" 110V 60Hz fan, ROTRON Whisper (WR2H1) or equivalent. The fan should move 65 to 75 cubic feet per minute — anything more powerful will also be noisier. Tie the fan into the AC power line between the power switch and the line filter.

Next to the fan hole there are six D-shaped holes for mounting standard 25-pin D-sockets. Such sockets can be tied to the input or output of S-100 cards, or can be tied directly into the S-100 bus.

Figure 1. Interior of Expansion Chassis



110V—220V CONVERSION

The S-100 Expansion Unit's power supply transformer has two primary windings. For 110V use, these windings are connected in parallel; for 220V use, the primary windings must be connected in series (see Figure 2).

Figure 2. 110V—220V Transformer Conversion

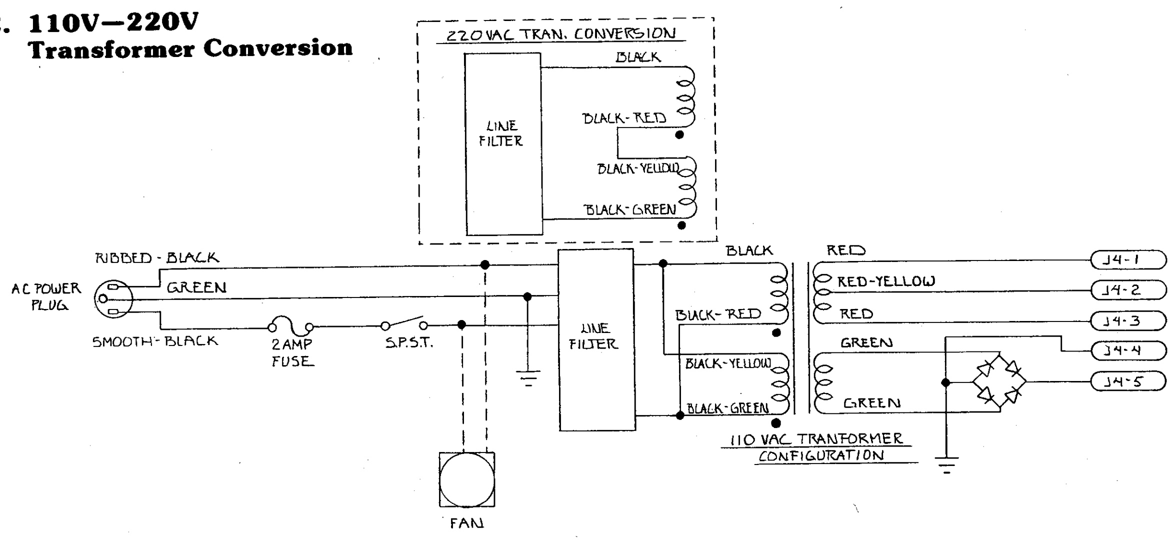


TABLE 1
Sorcerer 50-Pin Edge Connector
Pinout Table

S100 Pin Male Connect
in pencil

Pin #	Signal	Pin #	Signal	Pin #	Signal	Pin #	Signal
1	$\overline{\text{PRESET}}$ (out of Sorcerer)	11	ROM PRE	25	Address bit 15	39	Data bit 2
2	$\overline{\text{INT}}$	12	$\overline{\text{Reset Acknowledge}}$	26	Address bit 11	40	Data bit 1
3	$\overline{\text{WAIT}}$	13	ϕ2 (Clock out)	27	Address bit 13	41	Data bit 4
4	Data Bus Enable (into Sorcerer)	14	UP8K	28	Address bit 14	42	Data bit 3
5	$\overline{\text{BUSRQ}}$	15	$\overline{\text{MREQ}}$	29	Address bit 0	43	Data bit 6
6	$\overline{\text{NMI}}$	16	$\overline{\text{M1}}$	30	Address bit 12	44	Data bit 5
7	$\overline{\text{BUSACK}}$	17	$\overline{\text{RD}}$	31	Address bit 2	45	RESET (into Sorcerer)
8	Data Bus Direction (into Sorcerer)	18	$\overline{\text{IORQ}}$	32	Address bit 1	46	Data bit 7
		19	$\overline{\text{RFSH}}$	33	Address bit 4	47	Unused
		20	$\overline{\text{WR}}$	34	Address bit 3	48	I/O
9	$\overline{\text{RAM DR}}$ or $\overline{\text{ROM ENABLE}}$	21	Address bit 8	35	Address bit 6	49	Ground
10	ϕ1	22	$\overline{\text{HALT}}$	36	Address bit 5	50	Ground
		23	Address bit 10	37	Data bit 0		
		24	Address bit 9	38	Address bit 7		

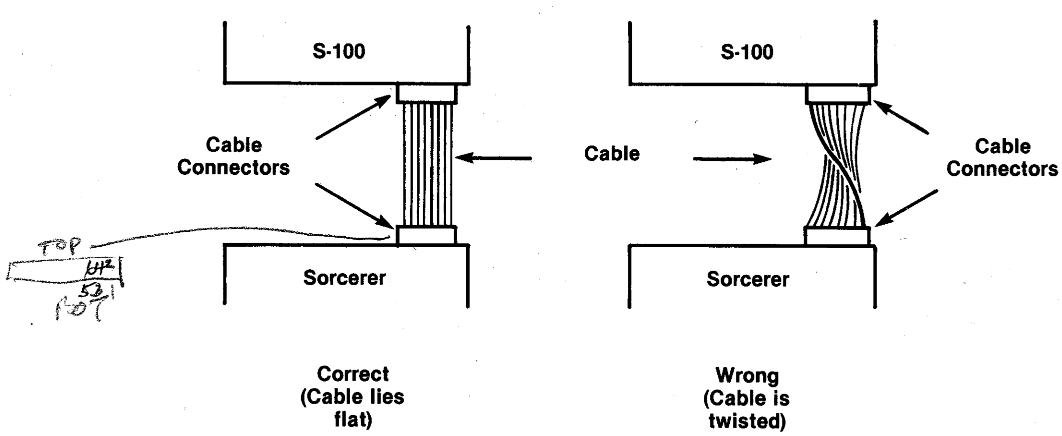
ATTACHING THE RIBBON CABLE

The ribbon cable has a large female edge connector at one end, and a smaller female pin connector at the other. The smaller connector attaches to the S-100 mother board. There is a slot at the bottom front of the S-100 unit, next to the 50-pin male connector on the mother board. Push the smaller cable connector up through the wide part of the slot, from the bottom of the S-100 unit. Then slide the cable into the narrow part of the slot and plug the cable connector onto the mother board; ***do not force.*** Plug the large cable connector onto the Sorcerer's 50-pin edge connector.

CAUTION

When you connect the S-100 Expansion Unit to the Sorcerer, the connecting cable must lie ***flat.*** If it is twisted, the Sorcerer's 50-pin edge connector will be ***cross-connected*** to the S-100 unit's 50-pin connector.

Figure 3. Sorcerer — S-100 Unit Connecting Cable



The following table gives the pinouts of the Exidy S-100 bus, together with the proposed IEEE standard for S-100. The 100-pin connectors are not numbered in the usual way (odd numbers on one side and even on the other). Instead, the numbers run 1 to 50 on one side of the connector and 51 to 100 on the other, with 51 opposite 1 and 100 opposite 50; the pins are on .125 centers. Over-barred signals (such as $\overline{SWO}$) are negative-active; all others (except the −16V utility) are positive-active. For explanation of the signal types, see p. 11B.

TABLE 2

		Exidy S-100 Bus		Proposed IEEE Standard	
Pin #	**Type**	**Name**	**Function**	**Name**	**Function**
1	B	+8V	Unregulated input to +5V regulators. Minimum available under full load.	+8V	Instantaneous minimum greater than +7V, instantaneous max less than +35V, average max less than +11V.
2	B	+16V	Unregulated input to +12V regulators. Minimum available under full load.	+16V	Instantaneous min greater than +14V, instantaneous max less than +35V, average max less than +20V.
3	S	XRDY	Ready input to current bus master. The bus is ready when both XRDY and PRDY are true.	XRDY	Same
4 to 11	S	Unused		VI0 to VI7	Vectored interrupt lines
12	S	$\overline{NMI}$	Non-maskable interrupt		Unspecified
13 to 17		Unused			Unspecified
18	M	Unused		$\overline{STAT\ DSB}$	Control signal to disable status signals
19	M	Unused		$\overline{C/C\ DSB}$	Control signal to disable command/control signals
20		Unused		UNPROT	Unspecified
21		Unused		SS	Unspecified
22	M	Unused		$\overline{ADD\ DSB}$	Control signal to disable address signals
23	M	Unused		$\overline{DO\ DSB}$	Control signal to disable data-out signals
24	B	$\phi 2$	The master timing signal for the bus	$\phi 2$	Same
25		$\phi 1$	TTL clock		Unspecified
26	M	PHLDA	Used together with $\overline{PHOLD}$ to coordinate DMA	PHLDA	Same
27	M	PWAIT	Wait acknowledge	PWAIT	The acknowledge signal to either of the bus ready signals XRDY, PRDY, or to a HALT instruction.
28	M	PINTE	Interrupt enable	PINTE	Unspecified
29	M	A5	Address bits	A5	Same
30	M	A4		A4	
31	M	A3		A3	
32	M	A15		A15	
33	M	A12		A12	
34	M	A9		A9	
35	M	DO1	Data-out bits	DO1	Same
36	M	DO0		DO0	
37	M	A10	Address bit	A10	Same
38	M	DO4	Data-out bits	DO4	Same
39	M	DO5		DO5	
40	M	DO6		DO6	

TABLE 2 (continued)

		Exidy S-100 Bus		Proposed IEEE Standard	
Pin #	**Type**	**Name**	**Function**	**Name**	**Function**
41	S	DI2		DI2	
42	S	DI3	Data-in bits	DI3	Same
43	S	DI7		DI7	
44	M	SM1		SM1	
45	M	SOUT		SOUT	
46	M	SINP	Status signals; indicate current status of bus	SINP	Same
47	M	SMEMR		SMEMR	
48	M	SHLTA		SHLTA	
49	B	CLOCK	2MHz local clock	$\overline{\text{CLOCK}}$	Unspecified
50	B	GND	Signal and power ground	GND	Same
51	B	+8V	Same as pin 1	+8V	Same
52	B	−16V	Unregulated input to −12V regulators. Max available under full load.	−16V	Instantaneous max less than −14V, instantaneous min greater than −35V, average min greater than −20V.
53		Unused		$\overline{\text{SSWI}}$	Unspecified
54	M	$\overline{\text{RESET}}$	Reset from Sorcerer	$\overline{\text{EXT CLR}}$	Unspecified
55 to 65		Unused			Unspecified
66	M	$\overline{\text{RFSH}}$	Refresh signal from CPU		Unspecified
67		Unused		$\overline{\text{PHANTOM}}$	Unspecified
68	B	MWRITE	Memory write enable	MWRITE	The logical negation of $\overline{\text{PWR}}$ and $\overline{\text{SOUT}}$; must follow $\overline{\text{PWR}}$ by no more than 30ns.
69				$\overline{\text{PS}}$	
70		Unused		PROT	Unspecified
71				RUN	
72	M	PRDY	See pin #3	PRDY	See pin #3
73	S	$\overline{\text{PINT}}$	Interrupt request	$\overline{\text{PINT}}$	Same
74	M	$\overline{\text{PHOLD}}$	See pin #26	$\overline{\text{PHOLD}}$	See pin #26
75	B	$\overline{\text{PRESET}}$	Clear CPU	$\overline{\text{PRESET}}$	Reset signal for bus masters; must stay low for at least three bus cycles
76	M	PSYNC	Indicates the beginning of each machine cycle	PSYNC	Indicates the beginning of each bus cycle
77	M	$\overline{\text{PWR}}$	Write enable	$\overline{\text{PWR}}$	Signifies valid data on DO bus
78	M	PDBIN	Data bus in	PDBIN	Requests data from current slave, on the DI bus
79	M	A0		A0	
80	M	A1		A1	
81	M	A2		A2	
82	M	A6		A6	
83	M	A7	Address bits	A7	Same
84	M	A8		A8	
85	M	A13		A13	
86	M	A14		A14	
87	M	A11		A11	

TABLE 2 (continued)

		Exidy S-100 Bus		Proposed IEEE Standard	
Pin #	**Type**	**Name**	**Function**	**Name**	**Function**
88	M	DO2		DO2	
89	M	DO3	Data-out bits	DO3	Same
90	M	DO7		DO7	
91	S	DI4		DI4	
92	S	DI5		DI5	
93	S	DI6	Data-in bits	DI6	Same
94	S	DI1		DI1	
95	S	DI0		DI0	
96	M	SINTA	Interrupt acknowledge	SINTA	Identifies the instruction fetch following an accepted $\overline{\text{PINT}}$ interrupt
97	M	$\overline{\text{SWO}}$	Indicates data transfer bus cycle	$\overline{\text{SWO}}$	Same
98		Unused		SSTACK	Unspecified
99	B	$\overline{\text{POC}}$	Power-on clear	$\overline{\text{POC}}$	Same; must stay low for at least three bus states
100	B	GND	Same as pin #50	GND	Same as pin #50

NOTE

The proposed IEEE standard requires XRDY, $\overline{\text{STAT DSB}}$, $\overline{\text{C/C DSB}}$, $\overline{\text{ADD DSB}}$, $\overline{\text{DO DSB}}$, PRDY, $\overline{\text{PINT}}$, $\overline{\text{PHOLD}}$, and $\overline{\text{PRESET}}$, (pins #3, 18, 19, 22, 23, 72, 73, 74, and 75) to be generated by open collector bus drivers capable of sinking at least 20 mA at no more than .5V.

Figure 4. Timing Diagram, Clock Signals

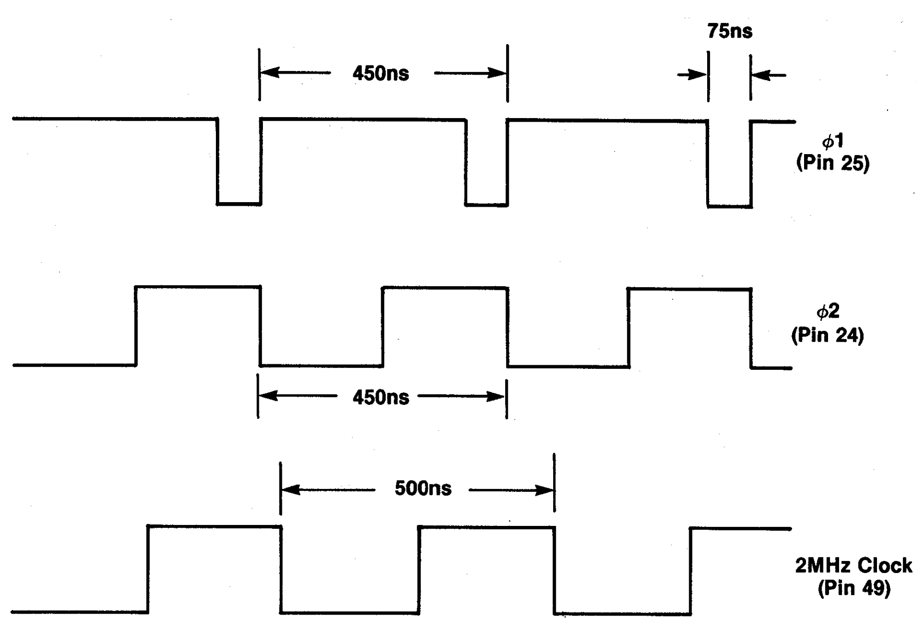


Figure 5. Memory or I/O Read

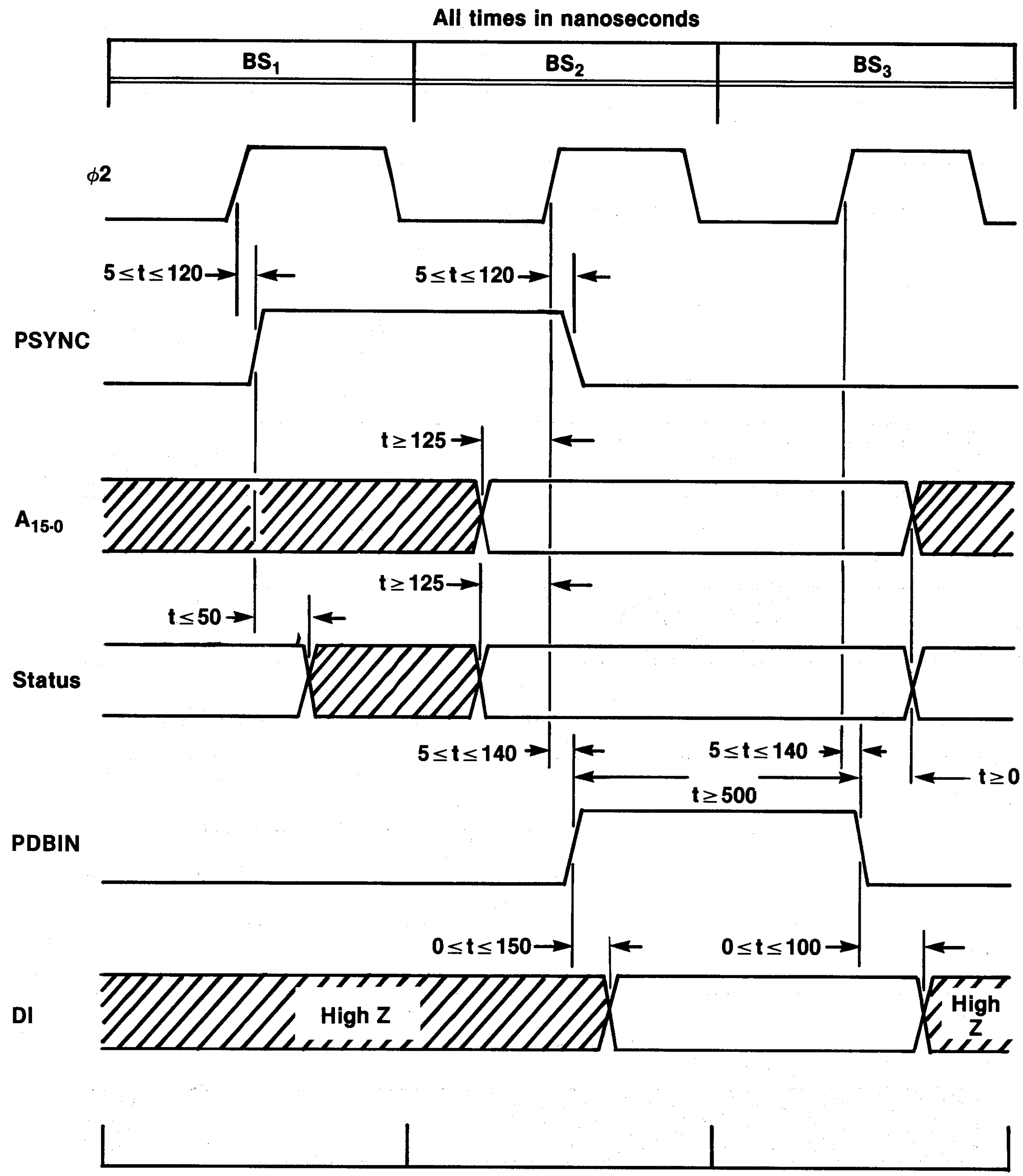


Figure 6. Memory or I/O Write

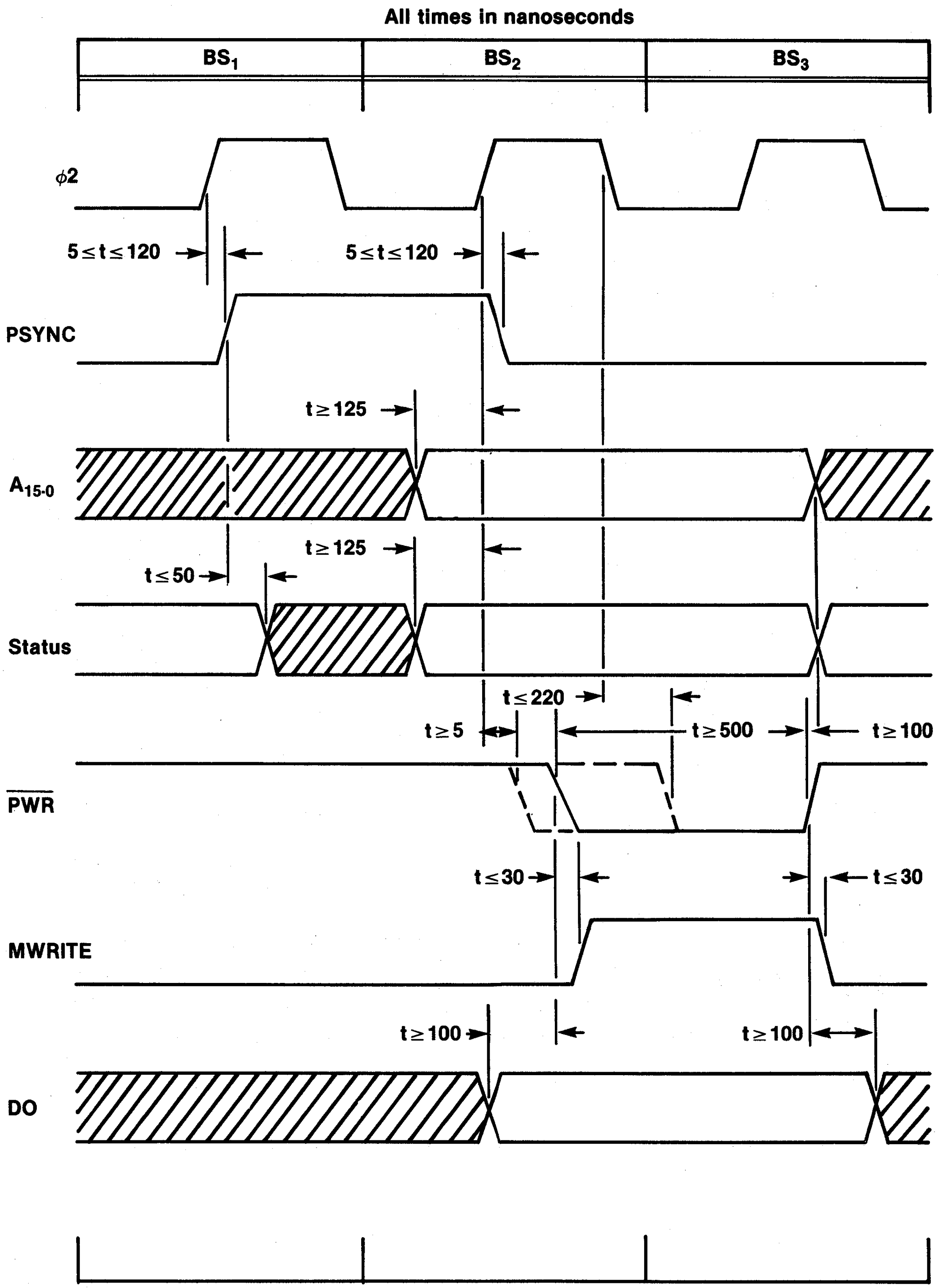
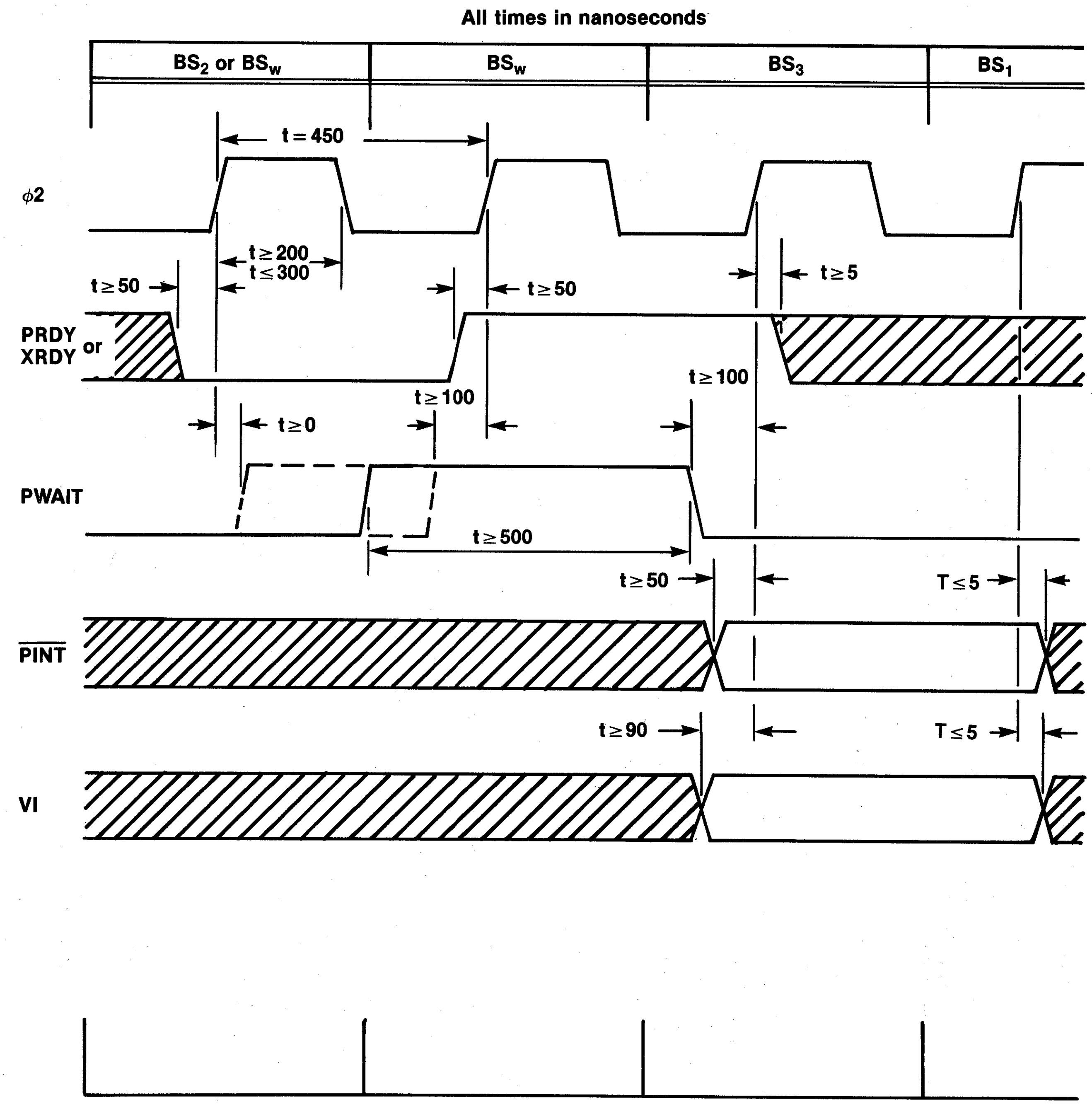


Figure 7. Interrupt and Wait Timing



PROPOSED IEEE STANDARD FOR THE S-100 BUS

Signal Types

There are three types of signal on the S-100 bus:

- Bus master signals, designated M. Each bus master must generate ***all*** of these signals while controlling the bus.
- Bus slave signals, designated S. A bus slave generates only those slave signals it needs to communicate with bus masters.
- Bus signals, designated B. This is the default type; any signal not of type M or S.

Device Types

By definition, a bus master is a device which generates at least all of the M signals, and a bus slave is a device which generates some slave signals. A device can be both a master and a slave.

Signal Subsets

- There are eight status signals (prefix S): SMEMR, SINP, SM1, SOUT, SHLTA, SSTACK (unspecified), $\overline{SWO}$, and SINTA.
- There are six command and control signals (prefix P): PHLDA, PSYNC, PDBIN, PINTE (unspecified), $\overline{PWR}$, and PWAIT
- There are sixteen address signals A15 through A0, with A15 the most significant bit, and A0 the least.
- There are eight data-out signals DO7 through DO0, with DO7 the most significant bit and DO0 the least. These are the data transmitted by the current bus master.
- There are eight data-in signals, DI7 through DI0, with DI7 the most significant bit and DI0 the least. These are the data received by the current bus master.

Signal Characteristics

Bus drivers must sink at least 24mA at no more than .5V and (except for open collector drivers) must source at least 2mA at no less than 2.4V.

Bus receivers must sink no more than 80μa at 2.4V and source no more than .8mA at .5V. They must interpret any signal less than .8V as logic 0, and any signal greater than 2V as logic 1. They must be diode clamped to prevent negative excursions, and must load the input no more than 25pF.

Bus States

A bus cycle is a sequence of three or more of the following states. The basic cycle is BS1, BS2, BS3; any number of BSw states may be inserted between BS2 and BS3, and one, two, or three BSi states may follow BS3.

- BS1 — The first state of any bus cycle. The address lines are unstable; PSYNC goes high during the second half.
- BS2 — The second state of any bus cycle. Address, data, status, and ready signals stabilize.
- BSw — may occur between BS2 and BS3 to synchronize bus masters and slaves.
- BS3 — the data transfer state.
- BSi — the bus-idle state.

PIN	SORCERER			S100	
1	6H-15	R	2	1A-5	
2	6H-17	R	1	1A-3	
3	6H-2	R	4	1A-18	
4	6H-13	R	3	1A-7	
5	6H-6	R	6	1A-14	
6	6H-4	R	5	1A-16	
7	5H-18		8	1B-2	
8	6H-8	R	7	1A-12	
9	5H-14		10	1B-6	
10	5H-16		9	1B-4	
11	5H-7		12	1B-13	
12	5H-12		11	1B-8	
13	5H-3		14	1B-17	
14	5H-5		13	1B-15	
15	5F-12		16	2B-3	3B-17
16	5F-19		15	2B-18	3B-2
17	5F-14		18	2B-5	3B-15
18	5F-13		17	2B-16	3B-4
19	5F-16		20	2B-7	3B-13
20	5F-15		19	2B-14	3B-6
21	4H-18		22	2A-2	
22	5F-17		21	2B-12	3B-8
23	4H-16		24	2A-4	
24	4H-17		23	2A-3	
25	4H-19		26	2A-1	

	SORCERER		S100		
26	4H-15	25	2A-5		
27	4H-13	28	2A-7		
28	4H-12	27	2A-8		
29	3H-18	30	3A-2		
30	4H-14	29	2A-6		
31	3H-16	32	3A-4		
32	3H-17	31	3A-3		
33	3H-14	34	3A-6		
34	3H-15	33	3A-5		
35	3H-12	36	3A-8		
36	3H-13	35	3A-7		
37	2H-18	38	4A-2	5A-2	
38	3H-19	37	3A-1		
39	2H-16	40	4A 4	5A-4	
40	2H-17	39	4A-3	5A-3	
41	2H-14	42	4A-6	5A-6	
42	2H-15	41	4A-5	5A-5	
43	2H-12	44	4A-8	5A-8	
44	2H-13	43	4A-7	5A-7	
45	? *	46	N/C		
46	2H-19	45	4A-1	5A-1	
47	N/C	48	7A-1		+5V
48	5H-9	47	1B-11		
49	GROUND	50	- GROUND		
50	GROUND	49	- GROUND		

Note 9E-5 - Master Reset
5H-8 Reset
6H-5 Reset Exp

DIRECT MEMORY ACCESS (DMA)

Bus Exchange

DMA is the process a bus master (the DMA device) uses to take control of the bus from the CPU, and read or write in memory. The cycle begins when the DMA device signals PHOLD. This signal must be given only when PHLDA is false. The CPU interprets PHOLD as a bus request (BUSRQ).

The proposed IEEE standard assumes that the DMA device will disable the CPU's bus drivers with the signals ADD DSB, DO DSB, STAT DSB, and C/C DSB. The Sorcerer does not handle DMA in this manner. Instead, the CPU disables its own drivers (but ***not*** the buffers to the 50-pin edge connector) when it responds to the bus request. The CPU acknowledges the bus request with a BUSAK signal, and the S-100 unit responds to the BUSAK by giving the bus to the DMA device.

To keep the bus signals stable, the CPU and the DMA device must ***both*** drive the bus at two periods during the DMA cycle: when the DMA device takes control of the bus, and when it returns control to the CPU. During these two periods, the CPU and DMA device must both drive the command and control signals for at least 200ns and the command and control signals must have these values:

- PSYNC = 0
- PWAIT = 0
- PHLDA = 1
- PDBIN = 0
- PWR = 1

Proposed DMA Sequence

The following DMA sequence is part of the proposed IEEE standard for the S-100 bus. To start the sequence, the DMA device must send the PHOLD signal; PHLDA will then go true during BS3 of the last CPU cycle (the S-100 unit interprets the CPU's BUSAK signal as PHLDA). The exchange starts at the falling edge of $\phi 2$ while PHLDA is true, and the entire cycle is controlled by the edges of $\phi 2$.

$\phi 2$ edge 1: CPU address and data bus drivers disabled; DMA command and control drivers on. CPU and DMA command and control signals as described above.

$\phi 2$ edge 2: CPU status and command and control drivers off; DMA address, data-out, and status drivers on. PSYNC = 1.

$\phi 2$ edge 3: No change.

$\phi 2$ edge 4: PSYNC = 0; PDBIN = 1 if memory read or PWR = 0 if memory write.

$\phi 2$ edge 5: No change.

$\phi 2$ edge 6: PDBIN = 0 and PWR = 1.

$\phi 2$ edge 7: CPU command and control drivers on; DMA address and data-out drivers off.

$\phi 2$ edge 8: DMA device sends PHOLD = 1. CPU address, data, and status drivers on; DMA status and command and control drivers off.

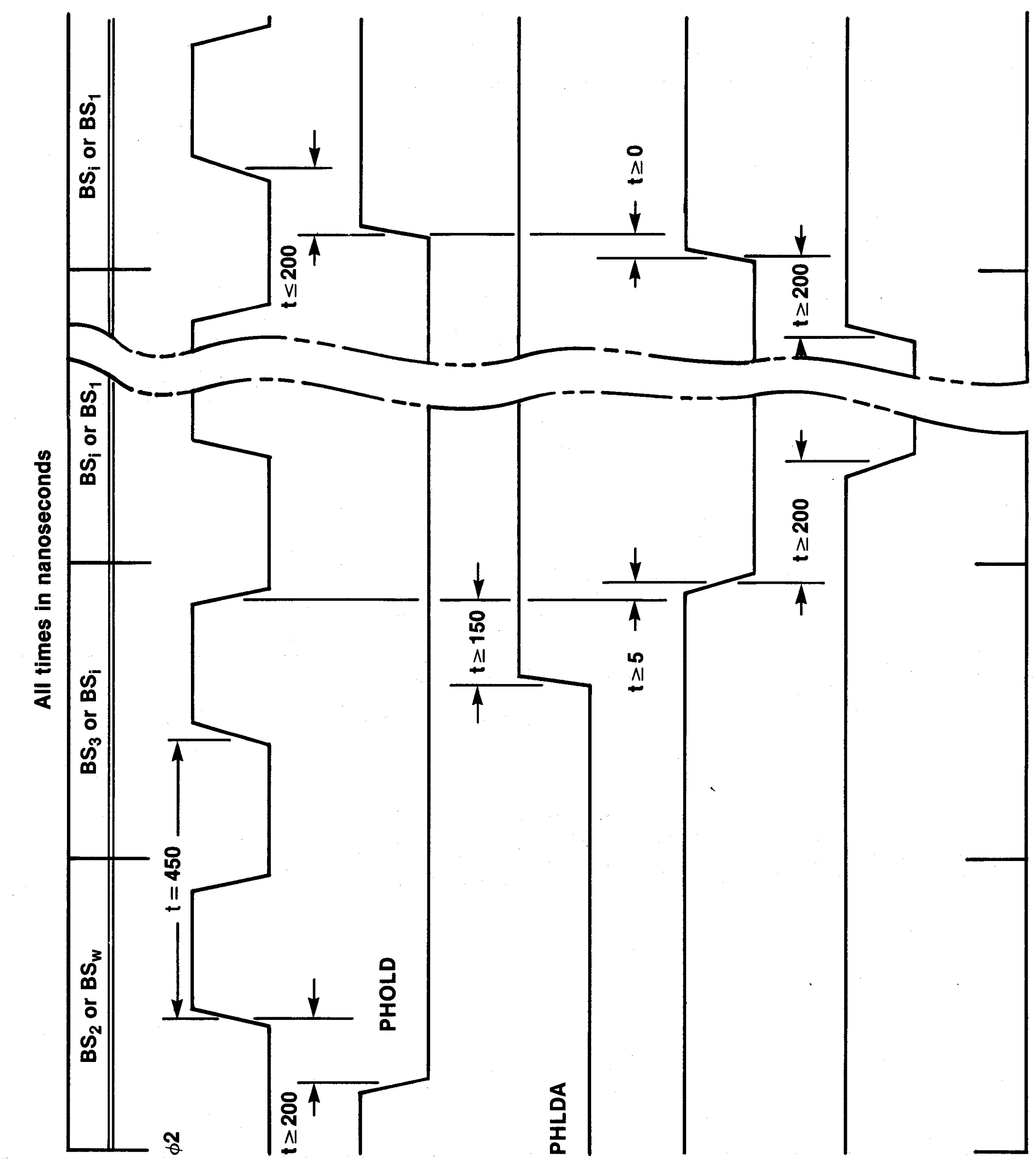


Figure 8. Bus Exchange Timing

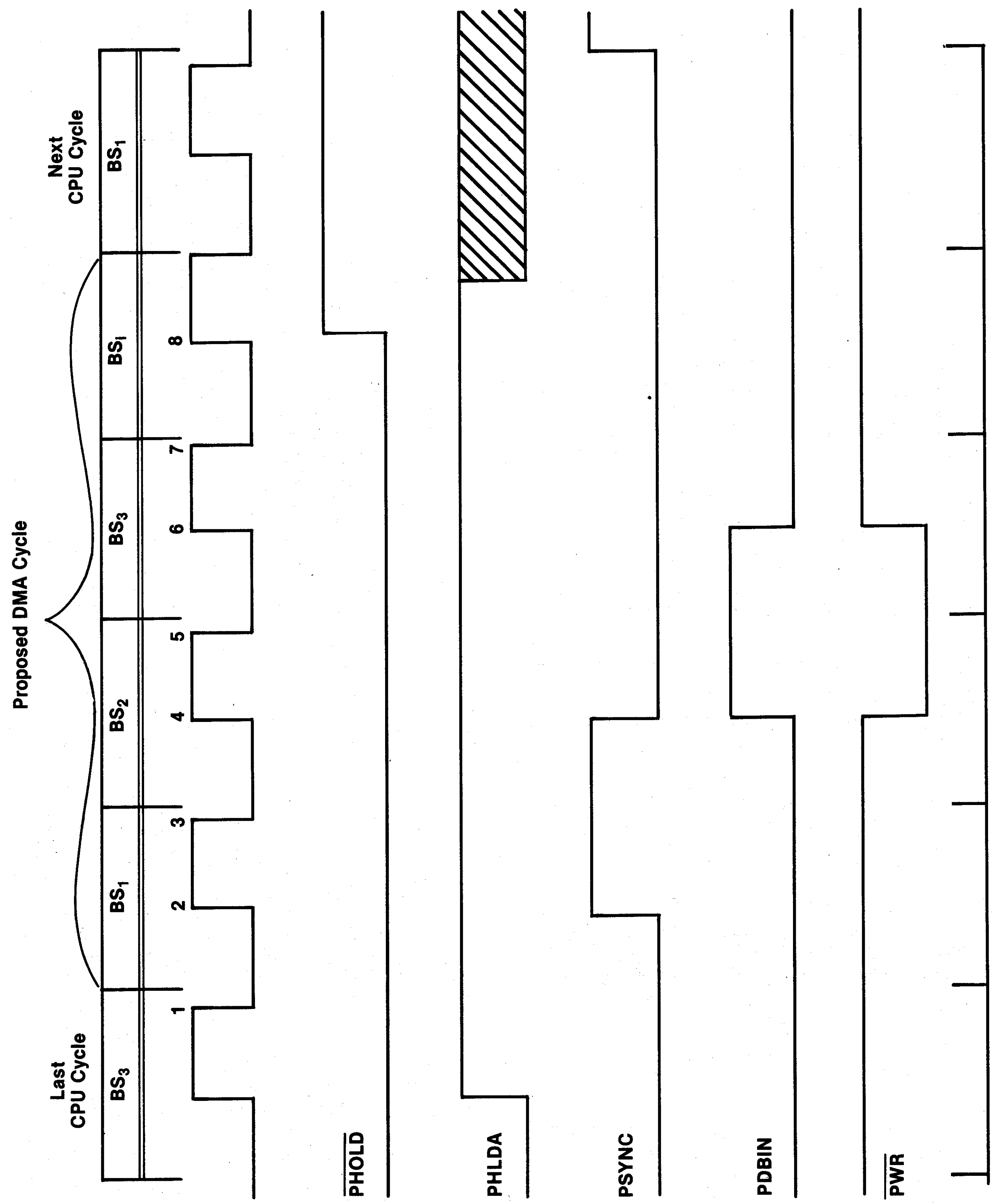


Figure 9. Proposed DMA Cycle

Theory of Operation

When the S-100 bus was created, bi-directional ICs were uncommon. Therefore, the address bus is assumed to function in one direction only, and there are two data buses — one for data out of the CPU, and another for data into the CPU.

The circuitry on the S-100 Expansion Unit mother board translates between the Sorcerer's bi-directional data signals and the uni-directional signals required by S-100 devices. It will also drive the address bus in reverse during a direct memory access (DMA).

The bus controller enables and controls the direction of the data and control signal buffers. This is analogous to the function of the Screen Controller on the Sorcerer logic board. The 6331 PROM at 5B (Program # S-100) controls the data-in and data-out buffers (4A and 5A) and the Sorcerer's bi-directional data buffer (the control signals pass through the S-100 CPU control buffer 1A, and the Sorcerer's CPU control buffer). The address buffer (2A and 3A) is always enabled; it takes its direction signal directly from the Sorcerer's bus request acknowledge ($\overline{\text{BBUSAK}}$, buffered through 1B).

Table 3 gives the input signals to 5B. A memory address is assumed to be in the S-100 unit, if it is not on the Sorcerer (i.e., ***not*** in the ROM PAC, internal RAM, or the upper 8K of memory). Similarly, any I/O port other than FCH, FDH, FEH, or FFH is assumed to be in the S-100 unit. Any I/O device other than a cassette recorder, Centronics printer, or RS232 is assumed to be in the S-100 unit. During an I/O request, the I/O port number appears on the lower half of the address bus; it is ***not*** duplicated on the upper half of the bus.

Table 3
Input to 6331 PROM
Conditions for High and Low Input Signals

Pin #	Low	High
14	When CPU is servicing a bus request	Otherwise
13	During a read or interrupt	No read or interrupt
12	Address in S-100	Address in Sorcerer
11	During refresh	Otherwise
10	I/O port in Sorcerer	I/O port in S-100

Besides controlling the buses, the S-100 unit also provides three clocks. A local 2MHz oscillator generates a clock signal for S-100 devices which cannot use the Sorcerer's 2.106MHz clock. The other clock signals are $\phi 1$ and $\phi 2$, generated by the Sorcerer.

There are thirty-two possible combinations of signals to 5B's five inputs. We consider each of these combinations to be a five-bit binary number; pin 5B-14 is the most significant bit, and pins 13, 12, 11, and 10 are the other bits, in decreasing significance. For example, 10011 signifies pins 14, 11, and 10 high, and pins 13 and 12 low. The S-100 program in 5B divides these thirty-two possible inputs into five cases:

Case 1 — DMA read (inputs 00010, 00110, and 00111; output 101011)

- The Sorcerer data buffer is enabled high.
- 4A is enabled high.
- 5A is disabled.
- Data flows into the controlling device through the data-in bus.

Case 2 — DMA write (inputs 01010, 01110, and 01111; output 001100)

- The data buffer is enabled low.
- 4A is disabled.
- 5A is enabled low.
- Data flows from the controlling device through the data-out bus.

Case 3 — Normal read (input 10011; output 000011)

- The Sorcerer data buffer is enabled low.
- 4A is enabled low.
- 5A is disabled.
- Data flows into the CPU on the data-in bus.

Case 4 — Normal write (input 11011; output 101110)

- The Sorcerer data buffer is enabled high.
- 4A is disabled.
- 5A is enabled high.
- Data flows out of the CPU on the data-out bus.

Case 5 — Default (all other inputs; output 111111)

- The Sorcerer data buffer, 4A, and 5A are all disabled.

Note that during DMA the $\overline{\text{BBUSAK}}$ signal to 5B-14 also enables 2B and reverses the direction of the address bus (2A and 3A).

PERFORMANCE TESTS

If your unit passes these tests, you have a good assurance that it functions correctly; if it fails one or more tests, the test results will indicate which part of the unit is malfunctioning.

You will need a known good Sorcerer and the following S-100 plug-in cards, also known good:

- A RAM card, DIP switch addressable
- An I/O device and interfacing card
- A DMA device and interfacing card (optional).

1. RAM Test: This tests the address bus, both data buses, parts of the status and command buses, and the bus controller.
   a. Address the RAM card to an S-100 area (that is, between the bottom of the ROM PAC area and the top of internal RAM). Run the Power-On Monitor bit test (TE) on these addresses.
   b. Re-address the RAM card to all parts of the S-100 area and repeat the bit test.
   c. Address the RAM card so that part of it lies inside the ROM PAC area and part of it lies outside. Repeat the bit test with the ROM PAC inserted, and again with it removed.
   d. All addresses should pass the bit test, except addresses in the ROM PAC area; those addresses should pass the test when the ROM PAC is removed. If any address fails this test, proceed to the diagnostic tests, giving special attention to the read/write tests.

> **NOTE**
>
> If only some of the S-100 addresses fail the test, the data buses are probably not malfunctioning. The problem probably lies in the address bus or the bus controller.

2. I/O Test: This tests the bus controller, and portions of the status and command buses which are not tested by the RAM test.
   a. Address the I/O device to any I/O port other than FCH, FDH, FEH, or FFH.
   b. Enter and run a short program which reads or writes data (whichever is appropriate) to your device. You can do this in BASIC, using the INP function or the OUT command; you can also do it in Z80 machine language.
   c. The data sent or received by the I/O device should be the same as that received or sent by the Sorcerer. If your unit fails this test, proceed to the diagnostic tests, giving special attention to the bus controller test and the status and command bus test. If the unit has already passed the RAM test, you may skip the diagnostic read/write test.

3. DMA Test (optional): This tests the bus controller, and portions of the status and command buses which are not tested by the RAM test or the I/O test.
   a. If you have a DMA device, interface it to the Sorcerer through the S-100 unit. Follow the manufacturer's instructions for addressing, I/O port assignment, etc.
   b. Initiate a DMA read or write (whichever is appropriate), and check whether data is being read or written correctly.
   c. If your unit fails this test, go to the diagnostic tests, giving special attention to the bus controller test and the status and command bus tests. If your unit has already passed the RAM test, you may skip the read/write test.

DIAGNOSTIC TESTS

These tests will locate malfunctions in the S-100 unit. You will need the following equipment:

- A dual-trace externally triggered scope (Tektronix 465 or equivalent).
- A known good Sorcerer.
- A known good RAM card, DIP switch addressable.
- Six double-ended clip-on test leads.

1. Power Supply and Clock test
   a. Pull all S-100 cards out of the unit. Then test for these voltages on the 100-pin bus:

Pin #	Voltage
1	+11±1VDC
2	+18±1VDC
51	Same as pin 1
52	−18±1VDC

   b. Put the local clock (pin #49) on the scope and check for 2MHz frequency (500ns cycle time).
   c. Put the $\phi 1$ and $\phi 2$ clocks (pins #25 and 24) on the scope, triggering on the edge of $\phi 2$. Compare to the timing diagram (Figure 4); verify 2.106MHz frequency for $\phi 2$ (450ns cycle time).

2. Address and Data Bus Read/Write Test, Part I:
   a. Check the mother board visually for shorts or open lines in the buses.
   b. Remove the ROM PAC from the Sorcerer, and remove all S-100 cards from the S-100 Expansion Unit, except the RAM card. Address the RAM card to 8000H.
   c. Load program 1 (address and data line send and receive) into the Sorcerer at address 0000, and run it with the Monitor GO command. This program tests selected addresses from 8000H to C000H; if your RAM card is smaller than 16K, you must re-address it and rerun the program to cover the entire area tested. See Table 4

Example: If you have a 4K RAM card (1000H addresses), you must run the program four times, with the RAM card assigned to these blocks of addresses:

8000H to 8FFFH
9000H to 9FFFH
A000H to AFFFH
C000H to C000H

   1) Check for bad data in the block of addresses actually covered by the RAM card (for example, 8000H to 8FFFH for a 4K card). Ignore any bad data at other addresses.
   2) Check all address failures, even those outside the area covered by the RAM card.

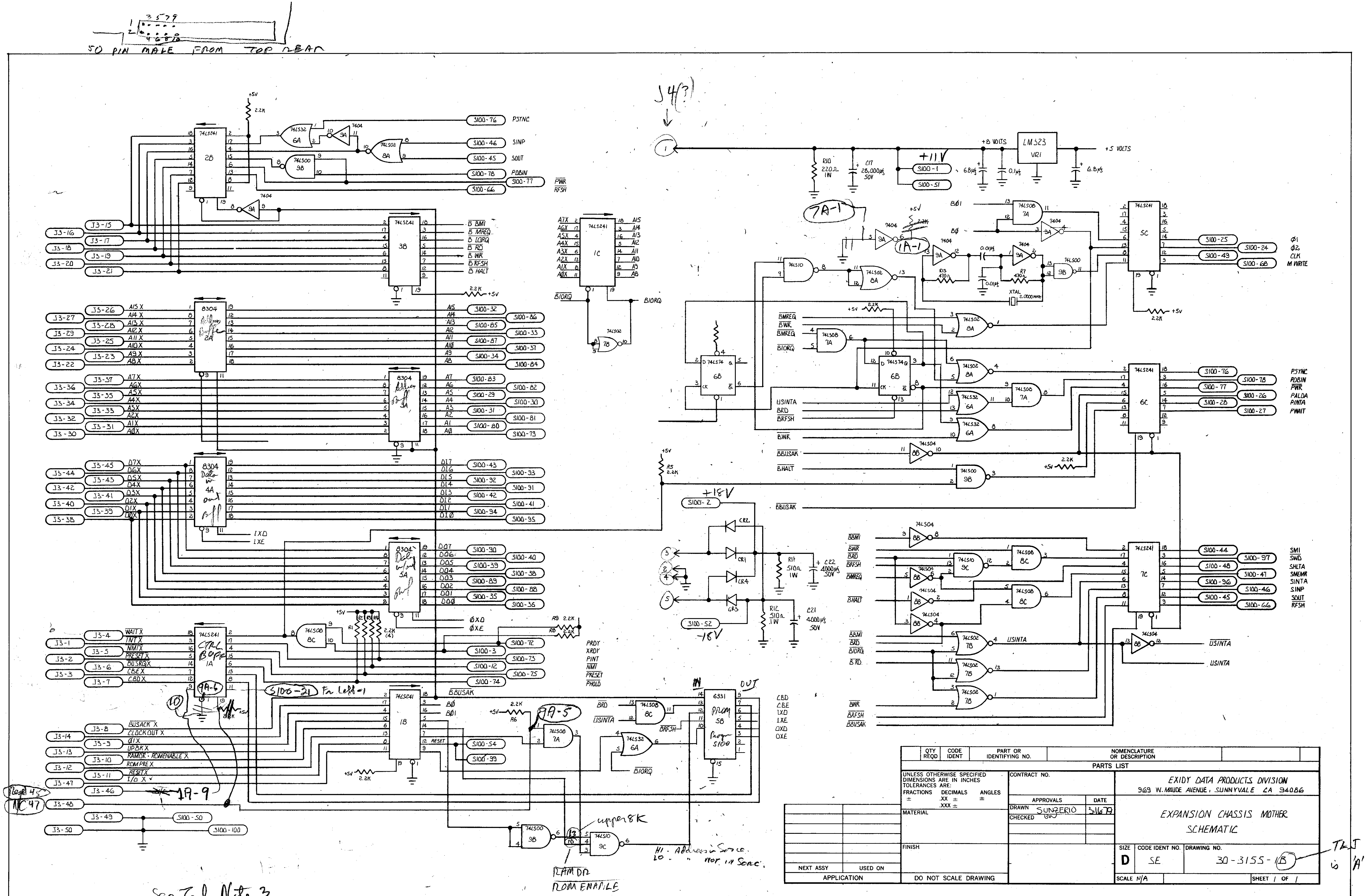
   d. This program tests all the data lines, and all address lines A0 to A14.
   1) If the Sorcerer is an 8K or 16K model, you can also check A15. Address the RAM card to 4000H and run program 1. Check only for bad addresses.
   2) If you have a 32K Sorcerer, you must check A15 manually. Pull 2A-1 high and low with a clip lead, and check whether the signal passes to 2A-19. Also check the line for shorts and open circuits.

   e. Use ESC or RUN/STOP to momentarily pause the program; use CTRL C to stop it. You can restart it with the Monitor command GO 0000.

3. Address and Data Bus Read/Write Test, Part II: (Do this part of the test only if your unit fails Part I)
   a. Remove all S-100 cards from the unit. Load program 2 (address and data-out bus exerciser) into the Sorcerer at address 0000, and run it with the Monitor command GO 0000.
   b. Set the scope sweep to 2ms/division. Put probe #1 on pin 2A-19 and trigger on that signal. Use probe #2 to check all address lines (pins 12 through 19 on 2A and 3A).
   c. On each address line you should see a group of eight pulses (one pulse for each data line) lasting about 94μs total.(See Figure 10.) Each address line is pulsed about 120μs earlier than the next higher address line.
   d. The pulses on the lower order address lines A0 to A6 (chip 3A) are superimposed on the refresh signal. You will probably not be able to read lines A0 to A5; check these lines with a logic pulser.
   e. Reset the scope sweep to 10μs/division but keep probe #1 and the triggering as before. Test each data-out line with probe #2 (all pins on 5A). You should see a 1.5μs pulse on each line; each line is pulsed about 13μs earlier than the next higher line (see Figure 11).
   f. If the address and data-out lines pass the test, reset the Sorcerer and load program 3 (data-in bus exerciser) at address 0000. Insert the RAM card, and address it to 8000H; then run program 3 with the Monitor command GO 0000.
   g. Trigger the scope on 2A-12; put probe #1 on 2A-19 and use probe #2 to test the data-in lines (pins 1 through 8 and 12 through 19 on 4A). You should see a 1.5μs pulse on each data-in line; each line is pulsed about 11.5μs before the next higher line (see Figure 12).

4. Bus Controller Test
   a. Using clip leads to pull the input signals high and low, test the gates leading into 5B (gates 6A-6, 7A-3, 8C-11, 9B-6, and 9C-6).
   b. Simulate a normal read by using clip leads to put 10011 on the input of 5B. Check whether the output is 000011; also check whether 4A and 5A are enabled and disabled as described in Theory of Operation, Case 3.
   c. Use the clip leads to simulate a normal write, a DMA read, and a DMA write. Check that the outputs of 5B are as described in Theory of Operation, Cases 4, 1, and 2. In each case, check that 4A and 5A are enabled and disabled correctly. When 5B-14 is pulled low (Cases 1 and 2, DMA read and write) check that 2B is enabled high, and 2A and 3A are driven low.
   d. Using the clip leads, check that all other inputs to 5B produce the output 111111.

5. Status and Control Bus Test
   a. Check that 1A, 1B, and 3B are enabled high.
   b. Using clip leads or a logic pulser, verify that 1A, 1B, and 3B will pass data from each input pin to the corresponding output pin.
   c. Using a clip lead, pull the $\overline{BBUSAK}$ signal low; check whether 6C and 7C are enabled high. Then pull $\overline{BBUSAK}$ high, and check whether 6C and 7C are disabled.



15A

15B

See comments on Numbering of J3 in MSA 4(6):135, Sept 82

Schematic 30-3155A 8/3/78 Rev. 10/31/78 is in Tech II Manual

TABLE 4

Addresses Tested by Program 1

Hexadecimal	Binary															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
8001	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
8002	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
8004	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
8008	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
8010	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
8020	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
8040	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
8080	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
8100	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
8200	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
8400	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
8800	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
9000	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
A000	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
C000	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

TABLE 5

Test Data Sent to Each Test Address

Hexadecimal	Binary							
	7	6	5	4	3	2	1	0
01	0	0	0	0	0	0	0	1
02	0	0	0	0	0	0	1	0
04	0	0	0	0	0	1	0	0
08	0	0	0	0	1	0	0	0
10	0	0	0	1	0	0	0	0
20	0	0	1	0	0	0	0	0
40	0	1	0	0	0	0	0	0
80	1	0	0	0	0	0	0	0

PROGRAM 1

Address and Data Line Send and Receive

```
Address  Obj Code   Label      Mnemonic          Comment
                    ;MONITOR SUBROUTINE EQUATES
         E1E8       ADDOUT:    EQU   E1E8H
         E205       CRLF:      EQU   E205H
         E21C       HEXSPC:    EQU   E21CH
         E015       QUIKCK:    EQU   E015H
         E01B       VIDEO:     EQU   E01BH
         E003       WARM:      EQU   E003H
                    ;MAIN PROGRAM
                               ORG   0
0000     21 01 80   START:     LD    HL,8001H
0003     18 0B                 JR    Z3
                    ; SET UP HL TO POINT TO NEXT ADDRESS
```

Continued on Page 16A

PROGRAM 1 (continued)

Address and Data Line Send and Receive

```
Address  Obj Code   Label      Mnemonic          Comment
0005     A7         Z2:        AND   A           ;CLEAR CARRY
0006     ED 6A                 ADC   HL,HL       ;SHIFT HL LEFT
0008     7C                    LD    A,H         ;SET MOST SIGNIFICANT BIT
0009     FE 80                 CP    80H
000B     28 F3                 JR    Z,START
000D     F6 80                 OR    80H         ;SET MOST
000F     67                    LD    H,A         ;        SIGNIFICANT BIT
0010     3E 01      Z3:        LD    A,01H
0012     18 04                 JR    Z4
                    ;SEND AND RECEIVE, AND CHECK IF OTHER
                    ;ADDRESSES DISTURBED
0014     CB 27      Z1:        SLA   A
0016     28 ED                 JR    Z,Z2
0018     4F         Z4:        LD    C,A
0019     CD 15 E0   Z6:        CALL  QUIKCK      ;CHECK
001C     FE 1B                 CP    1BH         ;     FOR
001E     28 F9                 JR    Z,Z6        ;        PAUSE
0020     FE 03                 CP    03H         ;            OR ABORT
0022     CA 03 E0              JP    Z,WARM
0025     11 00 20              LD    DE,2000H
0028     CD 4E 00              CALL  SDCAD
002B     11 00 40              LD    DE,4000H
002E     CD 4E 00              CALL  SDCAD
0031     11 00 80              LD    DE,8000H
0034     CD 4E 00              CALL  SDCAD
0037     79                    LD    A,C
0038     46                    LD    B,(HL)
0039     B8                    CP    B
003A     28 D8                 JR    Z,Z1
                    ;PRINT ADDRESS, DATA SENT, AND BAD DATA RECEIVED
003C     4F                    LD    C,A
003D     CD 64 00              CALL  PRHL        ;PRINT ADDRESS
0040     79                    LD    A,C
0041     CD 1C E2              CALL  HEXSPC      ;PRINT DATA SENT
0044     78                    LD    A,B
0045     CD 1C E2              CALL  HEXSPC      ;PRINT DATA RECEIVED
0048     CD 05 E2              CALL CRLF
004B     79                    LD    A,C
004C     18 C6                 JR    Z1
                    ;SUBROUTINES
                    ;SEND TEST DATA AND CHECK FOR ADDRESSES DISTURBED
004E     AF         SDCAD:     XOR   A           ;CLEAR ADDRESS POINTED
004F     12                    LD    (DE),A      ;          TO BY DE REG.
0050     71                    LD    (HL),C      ;SEND TEST DATA
0051     1A                    LD    A,(DE)
0052     B9                    CP    C           ;RETURN IF DIFFERENT
0053     C0                    RET   NZ          ;       FROM DATA SENT
0054     CD 6A 00              CALL  SPACE
0057     CD 64 00              CALL  PRHL        ;PRINT HL (ADDRESS REQUESTED)
005A     CD 6A 00              CALL  SPACE
005D     CD E8 E1              CALL  ADDOUT      ;PRINT DE (ADDRESS DISTURBED)
0060     CD 05 E2              CALL  CRLF
0063     C9                    RET
                    ;PRINT HL
0064     EB         PRHL:      EX    DE,HL
0065     CD E8 E1              CALL  ADDOUT
0068     EB                    EX    DE,HL
0069     C9                    RET
                    ;PRINT SPACE
006A     3E 20      SPACE:     LD    A,20H
006C     CD 1B E0              CALL  VIDEO
006F     C9                    RET
                               END
```

HOW TO INTERPRET THE ERROR MESSAGES

1. The address/data line send and receive program only gives an error message when data sent to one address goes to a different address, or when the data received from an address differs from the data sent to that address.

2. If the data buses pass incorrect data, the program will print the address of each malfunction, followed by the data sent, followed by the data received, all in hexadecimal.

Example:

8001 10 00

This means that 10H was sent to address 8001H, but 00 was received.

This will detect malfunctions in the data buses, but will not determine whether the malfunction is in the data-out or the data-in bus.

3. To find which lines are malfunctioning, convert the data sent and data received to binary, and compare them.

Example:

data sent: 10H which is 0001 0000 binary

data received: 00 which is 0000 0000

The malfunction is in data bit 4 (recall that bit 0 is the least significant bit, and bit 7 is the most significant).

4. Bad or nonexistent RAM addresses will usually show as FFH received. This does not indicate a malfunction unless the address involved actually has RAM assigned to it.

5. If the address bus malfunctions, the program will print the address intended, followed by the address actually reached.

Example:

8020 8000

This means that data was sent to address 8020H, but actually went to 8000H.

These error messages are indented one space, to make it easier to tell an address error from a data error.

6. To find which address lines are malfunctioning, convert the addresses to binary and compare them.

Example:

address intended: 8020H which is 1000 0000 0010 0000 binary

address reached: 8000H which is 1000 0000 0000 0000 binary

The malfunction is in address bit A5.

ILLUSTRATIVE EXAMPLES

These examples show the results Program 1 will give for some typical address and data bus malfunctions. We assume a 4K RAM card.

Example 1:

Malfunction — A14 shorted to ground

RAM card addressing — 8000H to 8FFFH

Program results:

```
 .   .   .
 .   .   .
 .   .   .
A000 80  FF
 C000 8000
 C000 8000
 C000 8000
 C000 8000
 C000 8000
 C000 8000
 C000 8000
 C000 8000
9000 01  FF
 .   .   .
 .   .   .
 .   .   .
```

Example 2A:

Malfunction — A15 held high (you must use an 8K or 16K Sorcerer)

RAM card addressing — 4000H to 4FFFH

Program results: No error indication (Program 1 doesn't send any data to addresses lower than 8000H).

Example 2B:

Malfunction — Same as 2A.

RAM card addressing — C000H to CFFFH

Program results:

```
 .   .
 .   .
 .   .
 C000 4000
 .   .
 .   .
 .   .
```

When the program tries to read address 4000H, it actually gets C000H (since A15 is held high). The data went to C000H as intended. The result is that the program thinks the data intended for C000H went to 4000H.

Example 3A:

Malfunction — A15 held low

RAM card addressing — 4000H to 4FFFH

Program results:

```
 C000 4000
```

Example 3B:

Malfunction: Same as 3A

RAM card addressing — C000H to CFFFH

Program results:

```
 .   .   .
 .   .   .
 .   .   .
C000 01  FF
C000 02  FF
 .   .   .
 .   .   .
 .   .   .
C000 80  FF
 .   .   .
 .   .   .
 .   .   .
```

Example 4:

Malfunction — A14 shorted to DO7

RAM card addressing — 8000H to 8FFFH

Program results:

```
A000 80  FF   { May be 7F instead of FF, if A14
 C000 8000      is capable of pulling DO7 low
C000 01  FF
 C000 8000
C000 02  FF
 C000 8000
C000 04  FF
 C000 8000
C000 08  FF
 C000 8000
C000 10  FF
 C000 8000
C000 20  FF
 C000 8000
C000 40  FF   { No addressing error, since
C000 80  FF     DO7 is high here
8001 80  00
8002 80  00
8004 80  00
8008 80  00
8010 80  00
8020 80  00
8040 80  00
8080 80  00
8100 80  00
8200 80  00
8400 80  00
8800 80  00
9000 01  FF
```

Example 5:

Malfunction — D0X or DI0 shorted to ground

RAM card addressing — 8000H to 8FFFH

Program results:

```
8001 01  00
8002 01  00
 .   .   .
 .   .   .
 .   .   .
8800 01  00
9000 01  FE
9000 02  FE
 .   .   .
 .   .   .
 .   .   .
C000 80  FE
```

Example 6:

Malfunction — D7X shorted to D0X or DO7 shorted to DO0 or DI7 shorted to DI0

RAM card addressing — 8000H to 8FFFH

Program results:

```
8001 01  00
8001 80  00
8002 01  00
 .   .   .
 .   .   .
 .   .   .
8800 01  00
8800 80  00
9000 01  FF
 .   .   .
 .   .   .
 .   .   .
```

Example 7:

Malfunction — DO0 shorted to ground

RAM card addressing — 8000H to 8FFFH

Program results:

```
8001 01  00
8002 01  00
 .   .   .
 .   .   .
 .   .   .
8800 01  00
9000 01  FF
 .   .   .
 .   .   .
 .   .   .
```

PROGRAM 2
Address and Data-Out Bus Exerciser

Address	Obj Code	Label	Mnemonic	Comment
0000	21 20 00	START:	LD HL,0020H	;START WITH ADDRESS LINE A5
0003	3E 01	Z1:	LD A,01H	;START WITH DATA-OUT LINE DO0
0005	77	Z2:	LD (HL),A	;SEND DATA TO ADDRESS
0006	CB 27		SLA A	;SHIFT 1-BIT TO NEXT HIGHER DATA LINE
0008	20 FB		JR NZ,Z2	;REPEAT UNTIL DATA=0
000A	A7		AND A	;CLEAR CARRY
000B	ED 6A		ADC HL,HL	;SHIFT 1-BIT TO NEXT HIGHER ADDRESS LINE
000D	20 F4		JR NZ,Z1	;REPEAT UNTIL ADDRESS=0
000F	18 EF		JR START	

PROGRAM 3
Data-In Bus Exerciser

Address	Obj Code	Label	Mnemonic	Comment
0000	26 80	DIN:	LD H,80H	;INITIALIZE ADDRESS
0002	2E 01		LD L,01H	;INITIALIZE DATA
0004	75	Z1:	LD (HL),L	;SEND DATA TO ADDRESS
0005	CB 25		SLA L	;INCREMENT DATA AND ADDRESS
0007	C2 04 00		JP NZ,Z1	;REPEAT FOR EACH DATA LINE
000A	2E 01	Z2:	LD L,01H	;RE-INITIALIZE
000C	7E	Z3:	LD A,(HL)	;READ DATA
000D	CB 25		SLA L	;MOVE TO NEXT DATA LINE
000F	C2 0C 00		JP NZ,Z3	;REPEAT FOR EACH DATA-IN LINE
0012	32 00 C0		LD (C000H),A	;SYNC POINT FOR SCOPE
0015	C3 0A 00		JP Z2	;REPEAT DATA-IN READ

Figure 10. Address Line Waveforms (Program 2)

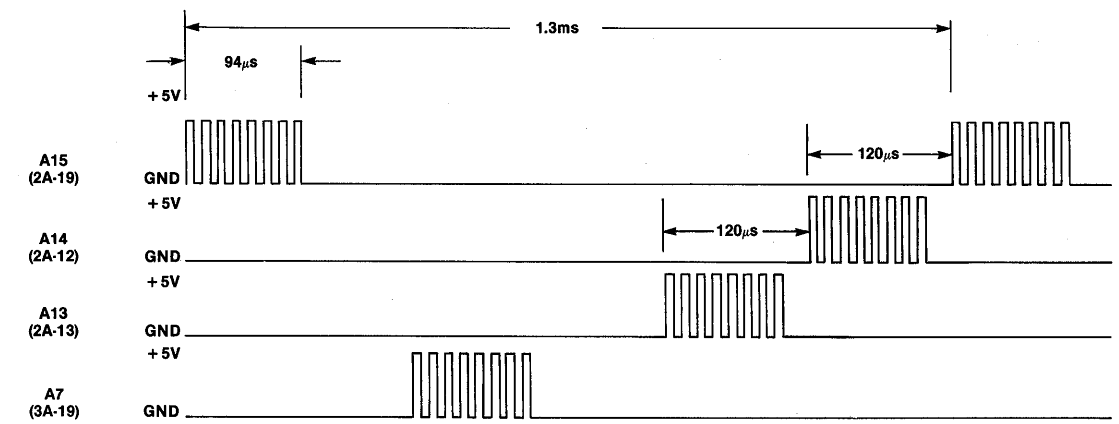


Figure 11. Data-Out Line Waveforms (Program 2)

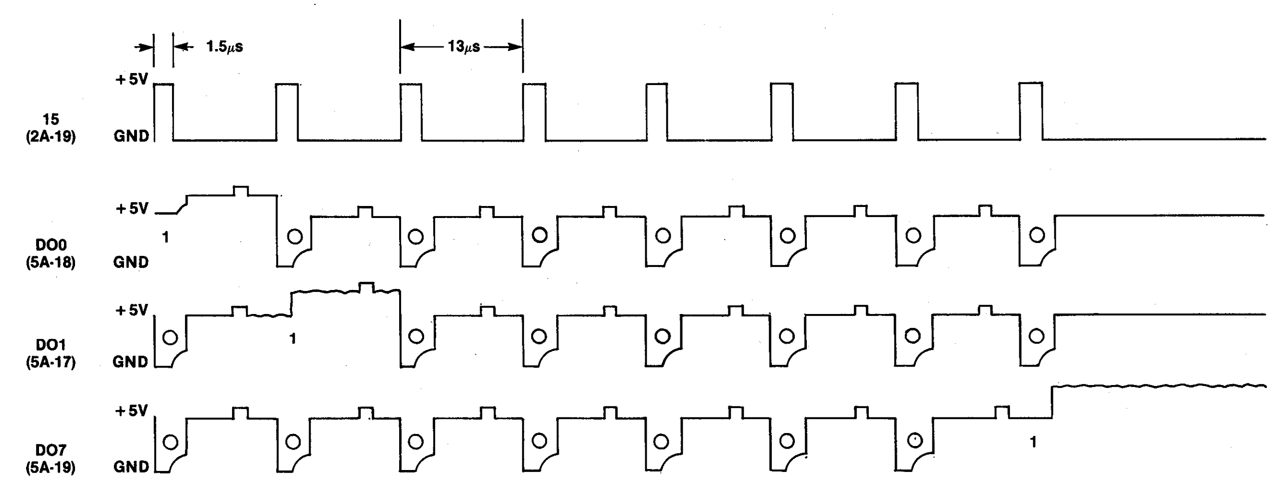
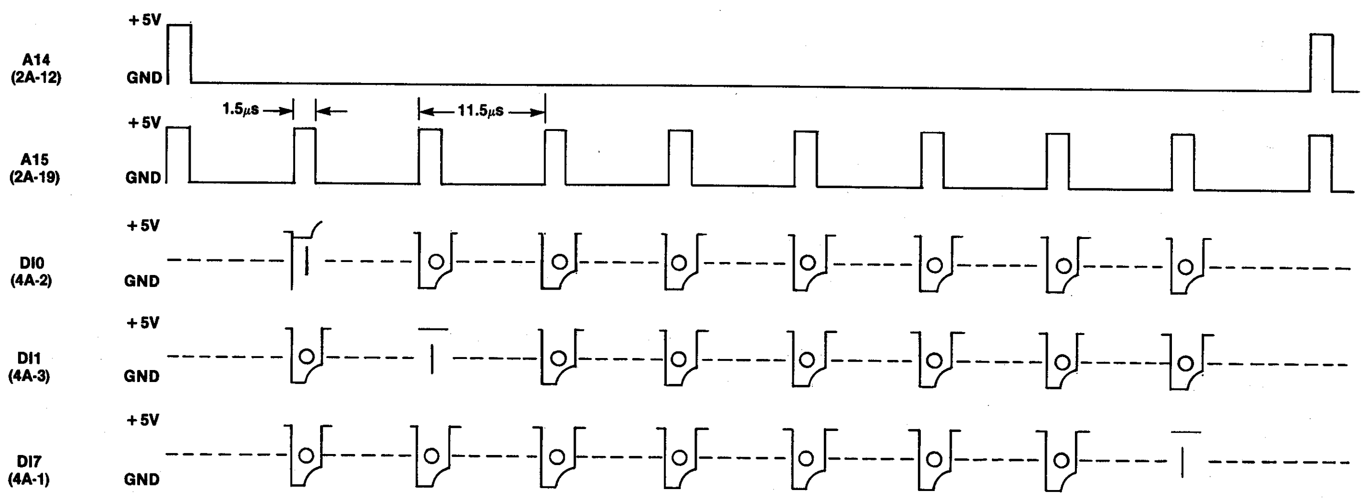


Figure 12. Data-In Line Waveforms (Program 3)



PARTS LIST

	Mother Board				Mother Board		
Part	**Qty/ Board**	**Locations**	**Exidy Part #**	**Part**	**Qty/ Board**	**Locations**	**Exidy Part #**
Complete Assembly	1		SE77-3155	.1µF ceramic cap.	14		SE23-4035
Bare PCB	1		SE77-3150	6.8µF 10V Dip tant. cap.	2		SE21-4016
Pre-programmed 6331 PROM (S-100)	1	5B	SE48-5005	4000µF 50V axial elect. cap.	2		SE20-4000
74LS00	1	9B	SE48-2300	28,000µF 15 WVDC radial cap.	2		SE25-1008
74LS02	2	7B, 8A	SE48-2301	220 ohm 1W resistor	1		SE57-5004
7404	1	9A	SE48-2302	470 ohm ¼W resistor	2		SE59-5135
74LS04	1	8B	SE48-2302	510 ohm 1W resitor	2		SE57-5005
74LS08	2	7A, 8C	SE48-2312	2.2K ¼W resistor	8		SE59-5110
74LS10	1	9C	SE48-2306	100-pin edge connector	6		SE61-8015
74LS32	1	6A	SE48-2315	Male 50-pin wirewrap header AMP #2-87227-5	1		SE61-8005
74LS74	1	6B	SE48-2305	5-pin male Molex header 09-65-1051 09-65-1059	1		SE61-8073
74S241 (74LS241)	7	1A, 1B, 2B, 3B, 5C, 6C, 7C	SE48-2328	Heatsink, Thermaloy 6013	1		SE68-8000
8304	4	2A, 3A, 4A, 5A	SE48-2327				
LM323K	1	8D	SE48-2336				
60S1 diode	4	8J	SE46-3016				
2.0MHz crystal	1	9A	SE45-3040				
.01µF 16V±10% mylar cap.	2		SE25-1013				

	Chassis	
Part	**Qty/ Unit**	**Exidy Part #**
Plastic Cover	1	SE91-4004
Steel chassis assembly (box)	1	SE68-1003
Overlay set	1	SE89-2008
Transformer	1	SE63-4027
MDA 970-1 Bridge Rectifier	1	SE47-3004
or	or	or
60S1	4	SE46-3016
2KI line filter	1	SE90-3000
Power switch	1	SE72-3052
Power cord	1	SE71-2328
2 amp SB fuse	1	SE60-6004
2 amp fuse holder	1	SE60-6005
12" Ribbon cable assembly with connectors	1	SE71-2022
5-pin female Molex connector 09-50-3051	1	SE61-8074
#8 ring lug P18-8R-C Panduit (or equiv.)	2	SE74-5153
.250 fast-on (insulated push-on connector)	11	SE61-8049
18 ga insulated butt splice	1	SE74-5154
Fan finger guard	1	SE74-5149
Rubber feet	4	SE82-1009

	Chassis	
Part	**Qty/ Unit**	**Exidy Part #**
Card guide, 2½" SAE 1250F (or equiv.)	12	SE75-4002
Strain relief gromet	1	
½" standoffs 6-32 thread aluminum	15	
6-23 x ¾" phil pan head machine screws	5	
6-32 kep nuts	25	
#6 flat washer	6	
6-32 x ¼" phil pan head machine screws	32	
6-32 x ½" phil pan head machine screws	10	
6-32 x 1¼" phil pan head machine screws	6	
8-32 x ¾" phil pan head machine screws	5	
6-32 x ¼" black iron oxide button head phil machine screws	4	
6-32 x ¾" black iron oxide button head phil machine screws	4	

LIMITED WARRANTY

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