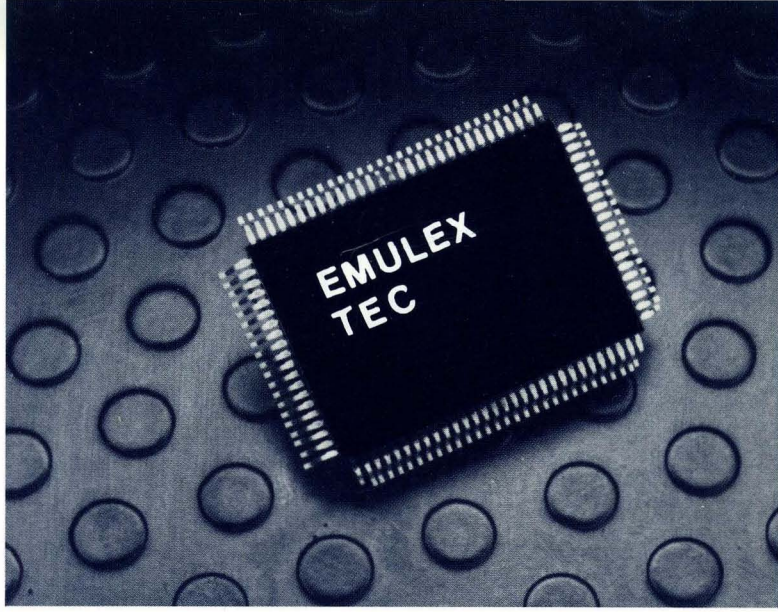
EMULEX MICRO DEVICES
TRIPLE EMBEDDED CONTROLLER
TEC 200*

EMBEDDED SCSI DISK CONTROLLERS



- **Provides Disk Formatter, Buffer Controller, and SCSI Bus Interface**
- **Supports SCSI-2, Fast SCSI, and SCSI-2 Information Structures**
- **Sustained SCSI Data Transfer Rate 10MB/sec in Fast SCSI Mode**
- **Connects directly to 8031/8051 and 80188/80186 Microprocessors**
- **Tristate Mode Allows Connection of Multiple TEC 200 Chips to Support Multiple SCSI Ports**
- **DMA Throughput in Excess of 10MB/sec**
- **Supports 40 MHz NRZ Data Rate**
- **64-Bit ECC**
- **Data Flow Control**
- **Direct Connection to Differential Transceivers**
- **Asynchronous Event Notification**
- **Pipelined Command Sequence**

PRODUCT DESCRIPTION

The Emulex Triple Embedded Controller (TEC 200/TEC 220) is a member of the Emulex family of single-chip controllers. A surface-mount, VLSI chip, it provides most of the functional circuitry needed to build an embedded SCSI disk controller in a space saving, high performance, single chip for small form factor drives. The TEC 200 is capable of handing both high disk data rates (40 Mbits/sec) and Fast SCSI rates (10 Mbytes/sec). The TEC 200 supports single-ended SCSI mode and the TEC 220 supports both single-ended and differential SCSI modes.

The TEC 200, a second generation triple embedded controller, provides a fast disk formatter, a bursting DRAM buffer controller, and a proven SCSI bus interface solution (Emulex ESP), all in a single chip. (See Figure 1, TEC 200 System Block Diagram.) The chip features SCSI-2 format support, asynchronous event notification, 64 bit ECC, data flow control, and the ability to connect multiple chips to one buffer.

SYSTEM ORGANIZATION

SCSI Bus Interface

The internal Emulex SCSI Protocol (ESP) solution consists of a number of sequencers and programmable registers which provide direct single-ended SCSI bus control. The sequencers are a collection of high and low level state machines that perform the various functions required by the SCSI bus and the DMA channel. The high level state machines manage the bus connect, disconnect, target, and initiator modes. The low level state machines perform the interface operations and actual bus cycle timing.

Because the common SCSI sequences are implemented in hardware inside the cell, firmware processing and host intervention are significantly reduced. Further overhead reduction is achieved by means of a double ranked transfer counter register. A watchdog timer enhances overall system reliability.

*TEC 200 will refer to TEC 220 as well, except as noted.

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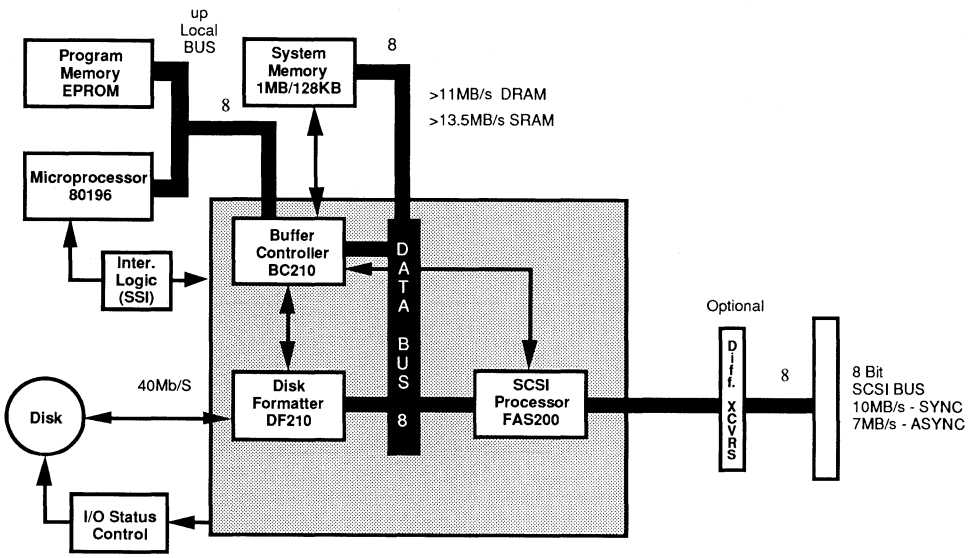

TEC200 - 100PQFP

TEC220 - 120PQFP

Figure 1.
TEC 200 System Block Diagram

Other features of the SCSI bus interface include:

- Support of ANSI X.3T9.2 SCSI Standard
- Support of SCSI-2 enhancements

  Asynchronous event notification
  Automatic message checks
  - Queue tag 3-byte commands
  - ID message check

  Extended message byte handling
  Buss free delay
- On-chip 48mA single-ended SCSI transceivers
- Support of differential SCSI mode with a direct interface to external differential transceivers (TEC 220)
- Support of the following SCSI data transfer rates:

  Asynchronous to 7MB/sec
  Synchronous
  - 5MB/sec (normal SCSI)
  - 10MB/sec (Fast SCSI)
- Bus target and initiator modes
- Pipelined command structure
- Parity check/generate or pass-through to the buffer
- 16-byte deep FIFO between DMA and SCSI channels

Buffer Control

The buffer controller subsection of the TEC 200 provides complete DMA control and direct data movement into and out of local dynamic RAM buffer memory (DRAM or SRAM). It also provides a connection between the two controller buses, the microprocessor bus, and the buffer data bus.

The buffer controller also provides microprocessing address decoding, priority arbitration for the buffer resource, limit/reload control of address pointers, pass-through odd parity support (DRAM mode only), and automatic DRAM refresh control. The DMA control logic is optimized to achieve the maximum level of performance from DRAM based designs.

Other features of the buffer controller include:

- DMA throughput exceeding 10MB/sec using high speed page mode or static column DRAMs
- Programmable burst memory cycle timing for DRAM speed selection
- Addressing of 64K, 256K, 1Mbit and 4Mbit buffer memory
- Two dedicated DMA ports plus auto refresh capability
- Data flow mechanism to automatically monitor data buffer condition and reduce firmware interrupt processing

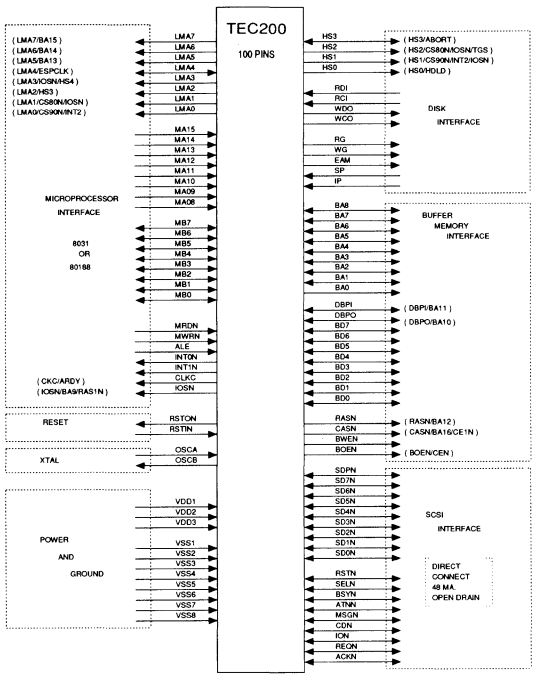

Figure 2.
TEC 200 Functional Signal Grouping

Disk Formatter Architecture

The disk formatter subsection of the TEC 200 provides a complete serial NRZ interface to the disk with four lines for read and write of data and clock. Four or five head select lines provide the necessary timing for fast 1:1 sector interleave. These lines can also be configured for various I/O operations. The disk formatter architecture consists for fast state machine and programmable registers which can be configured to support a wide variety of formats, providing the essential flexibility and savings in parts costs required in embedded designs.

Headers are protected by a 16-bit CRC and data fields by a 64-bit ECC. An ECC error-correction shift register supports the automatic generation of CRC/ECC and detection of errors. The shift register also provides a hardware assist in data-field correction processing. A FIFO buffers the flow of data between a serial I/O shift register (SERDES) and the disk formatter DMA port.

The disk formatter subsection of the TEC 200 chip also provides or supports:

- 40MHz data rate
- Highly programmable gap registers
- Hard or soft sector schemes
- Multi-sector/single sector operations
- Zero latency read
- Auto re-command

Microprocessor Interface

The microprocessor interface provides or supports the following features:

- Compatibility with 8031/8051 and 80188/80186 type microprocessors
- A watchdog timer to monitor system operation
- Additional decoded/chip selects for simplified system design
- Low order address latched for direct EPROM connection
- Tristate mode so multiple TEC 200 chips can be connected to one buffer

Microcode Firmware

To reduce SCSI overhead, the following features are included in the microcode firmware:

- Write data prefetch
- Target disconnect/reconnect capability
- Fast SCSI support
- Track and cylinder skew
- Defect management
- Data flow buffer management

PACKAGING

The TEC 200 is available in 100-pin PQFP packaging, part number 2400082. The TEC 220 is available in 120-pin PQFP packaging, part number 2400083.

Functional signal groupings are shown in Figures 2 and 3; pin diagrams in Figures 4 and 5.

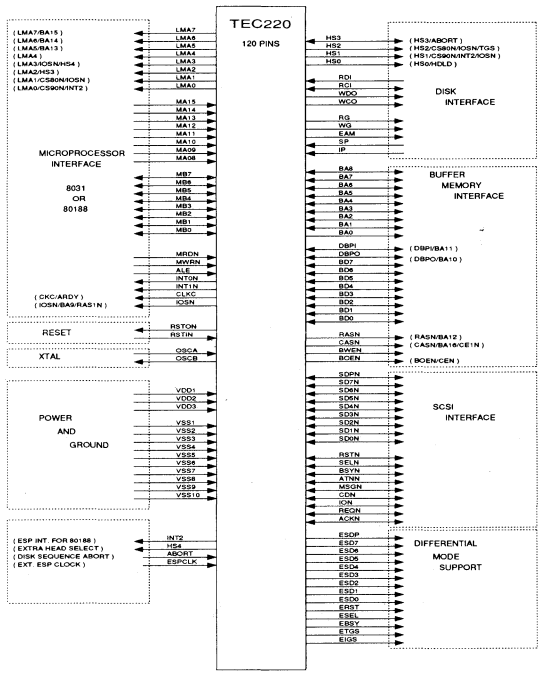

Figure 3.
TEC 220 Functional Signal Grouping

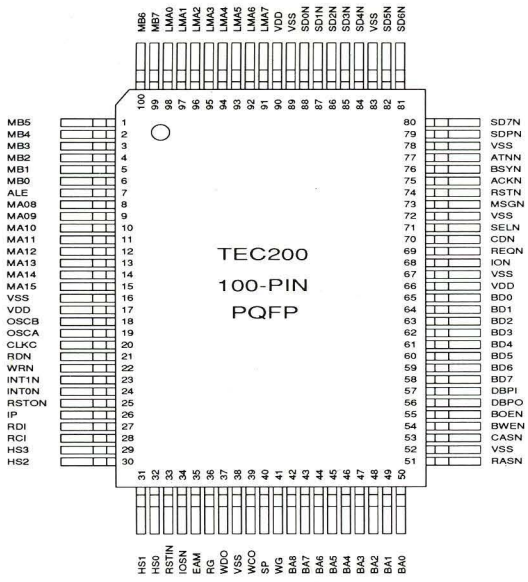

Figure 4.
TEC 200 100-Pin PQFP Pin Diagram

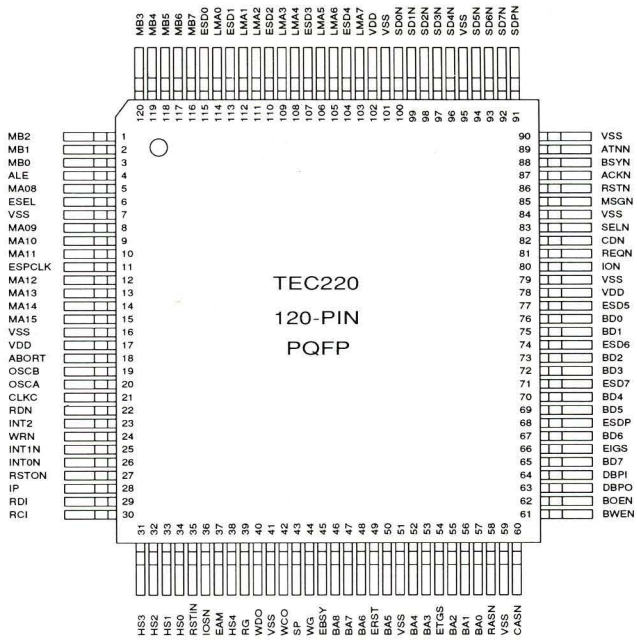

Figure 5.
TEC 220 120-Pin PQFP Pin Diagram

TEC 200 FEATURES AND BENEFITS

Feature	Benefit
40 MHz disk data rate	By supporting ZBR (zone bit recording) and high rotational speeds, the chip can be used with high bit density drives.
Low SCSI bus overhead	With more efficient bus utilization, the SCSI bus can be shared with more peripherals. Information is delivered faster to the host.
High data througput	Both SCSI and the disk itself can be run at maximum data transfer rates.
Direct addressing of 1 MB DRAM or 128K SRAM	User is given the option of a speed/cost tradeoff in memory; RAM can be selected for either speed or cost.
Support of Fast SCSI data rates	Data can be transferred in half the time (twice as fast) as with normal SCSI.
Data flow	Offers automatic monitoring of buffer memory when handling small sector sizes at high speeds. Drives with fast data rates and/or small sector sizes are supported without interrupting the CPU.
64-bit ECC	Longer error bursts can be detected and corrected.

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