MT02 (TITLEIST)
TAPE CONTROLLER
TECHNICAL MANUAL

3545 Harbor Boulevard
Costa Mesa, California 92626
(714) 662-5600 TWX 910-595-2521

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WARNING

This equipment generates, uses and can radiate radio frequency energy, and if not installed and used in accordance with the technical manual, may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of Federal Communications Commission (FCC) Rules, which are designed to provide reasonable protection against such interference when operating in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

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TABLE OF CONTENTS

TABLE OF CONTENTS

TABLE OF CONTENTS

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

SECTION 1
MT02 Controller Specifications

1.1 Introduction

The Titleist Tape Controller Model MT02, called the MT02 Controller, was designed by Emulex Corporation to interface Small Computer System Interface (SCSI) host adapters and controllers to a 0.25-inch streaming cartridge tape drive (hereafter called tape drive). (The SCSI bus can interface with up to eight host adapters and/or related microcontroller devices.) The MT02 Controller supports the QIC-11 and QIC-24 standard tape data format and the QIC-36 interface between the MT02 Controller and the tape drive. This manual is designed to help you install the MT02 Controller and to provide information about buffering, signal translation capabilities, and applications. The contents of the eight sections and two appendices are described briefly below.

Section 1 **General Description**: This section contains an overview of the MT02 Controller.

Section 2 **MT02 Controller Specification**: This section contains specifications for the major components of the MT02 Controller.

Section 3 **Installation**: This section contains the information necessary to install the MT02 Controller, including switch settings.

Section 4 **Troubleshooting**: This section describes diagnostic procedures that can be used to pinpoint problem areas on the MT02 Controller.

Section 5 **Functional Description**: This section describes the architecture and tape operations of the MT02 Controller.

Section 6 **Interfaces**: This section describes the SCSI bus and QIC-36 interfaces; it includes information about SCSI bus signals and timing.

Section 7 **SCSI Bus Protocol**: This section describes phases, phase sequencing, and bus conditions necessary for the SCSI bus protocol.

Section 8 **SCSI Command Set**: This section describes SCSI commands and their corresponding Command Descriptor Blocks which are supported by the MT02 Controller.

Appendix A **General Error Conditions**: This section describes general media-related and drive-related error conditions that can occur during MT02 Controller tape operations.

Appendix B **MT02 Firmware Revisions**: This section lists the firmware release history for the MT02 Controller.

For reference convenience, Section 1 is divided into four subsections, as listed in the following table:

Subsection	Title
1.1	Introduction
1.2	Physical Description
1.3	Functional Overview
1.4	Compatibility

1.1.1 Related Documents

This manual is designed to be used by system programmers who are writing operating system drivers and support utilities. This manual assumes familiarity with the SCSI bus standard, the QIC-11 and QIC-24 data interchange specifications, and the QIC-36 tape drive interface specification.

The Small Computer System Interface (SCSI) command set for the MT02 Controller is based on the ANSI X3T9.2/82-2 Revision 14 B (06 Nov 84) SCSI Specification. Copies of the ANSI SCSI Specification can be obtained from the following publisher:

American National Standard Task Group X3T9.2/82-2
Computer and Business Equipment Manufacturers Association
311 First Street, NW, Suite 500
Washington, DC 20001

Because the SCSI standard is currently changing, this ANSI specification is subject to change without notice. It is the intent of Emulex to maintain SCSI compatibility as the standard evolves.

The QIC-36 interface between the MT02 Controller and the tape drive is described in the ANSI X3T9.6/84-9 Revision B (02 February 84) Specification for the 1/4-inch Cartridge Tape Drive Basic Interface.

The 0.25-inch tape format and recording standard is described in the proposed standard for Data Interchange on the Streaming 1/4-inch Magnetic Tape Cartridge Using Group Code Recording (GCR) at 10,000 flux reversals per inch (FRPI). This standard is the QIC-24 document, revision D, April 1983 or the QIC-11 document, revision B, September 1982.

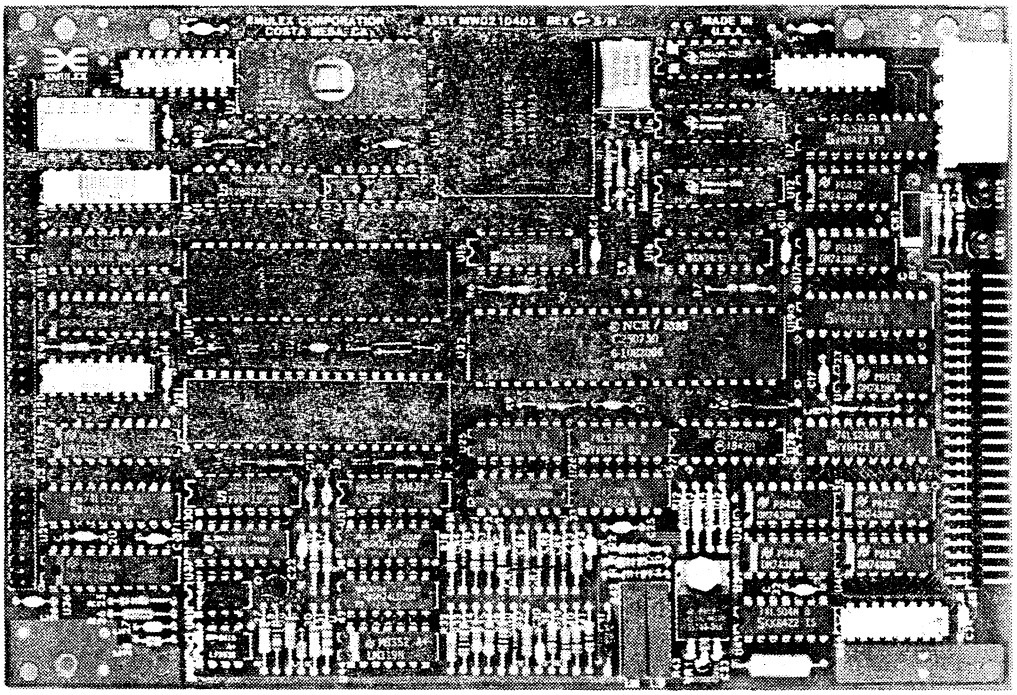
1.1.2 Technical Manual Conventions

To avoid possible confusion with other uses of the same words, throughout this manual we use the following conventions:

- All SCSI commands (such as **READ, MODE SELECT,** and **INQUIRY)** are printed in uppercase boldface.
- All SCSI status and error messages (such as CHECK CONDITION and DRIVE NOT READY) are printed in uppercase.
- All SCSI bus phases and conditions (such as Arbitration Phase) and SCSI Command Descriptor Block names (such as Extended Sense Byte) are printed in initial caps.
- All SCSI command and message codes are given in their hexadecimal values.

1.2 Physical Description

The MT02 Controller, shown in Figure 1-1, is assembled on a single board, approximately 14.6 cm by 20.3 cm (5.75 inches by 8 inches) and can be installed up to 3 meters (10 feet) away from the tape drive. It contains two Emulex custom Very Large Scale Integration (VLSI) chips: a Buffer Controller and a Tape Formatter. It also contains an 8031 microprocessor chip, a 32-kilobyte Erasable Programmable Read Only Memory (EPROM), and a 16-kilobyte Random Access Memory (RAM) which provides 14 kilobytes of data buffering.



MT0201-0626

Figure 1-1. MT02 (Titleist) Tape Controller

In combination with an independent host adapter, the SCSI bus allows a wide variety of computers to interface with the MT02 Controller. Compatible computers include DEC systems that use the Q-bus and Unibus, IBM Personal Computers systems such as the IBM PC/XT, and Multibus-based computers. Up to eight bus devices, in any combination of host systems and intelligent controllers, can be supported by the SCSI bus. The MT02 Controller/tape drive unit provides a low-cost, compact reliable backup for hard disk media in a microcomputer environment.

The architecture of the MT02 Controller and the SCSI bus features it supports make the MT02 Controller an ideal building block for use by OEMs and system integrators. The MT02 Controller supports a powerful set of SCSI commands. By using those commands, an efficient multiple-Initiator configuration can be constructed with the support of the disconnect function. (The disconnect function allows the MT02 Controller, when it is performing a time-consuming task, to release the SCSI bus temporarily and reconnect at a later time when the task is complete.) The MT02 Controller may be considered a SCSI extended-bus device because it uses all standard and extended SCSI commands.

Emulex currently offers two additional SCSI bus microcontrollers that can be used with SCSI bus subsystems: the Medalist and the Champion. The Medalist disk controller interfaces the SCSI bus to up to two standard ST506 interface 5.25-inch Winchester-type disk drives. The Champion disk controller interfaces up to two Enhanced Small Disk Interface (ESDI) 5.25-inch disk drives to the SCSI bus.

In addition to basic stand-alone controller products, Emulex also offers complete SCSI bus disk and tape packaged subsystems for microcomputer applications.

A sample configuration of a SCSI system is shown in Figure 1-2.

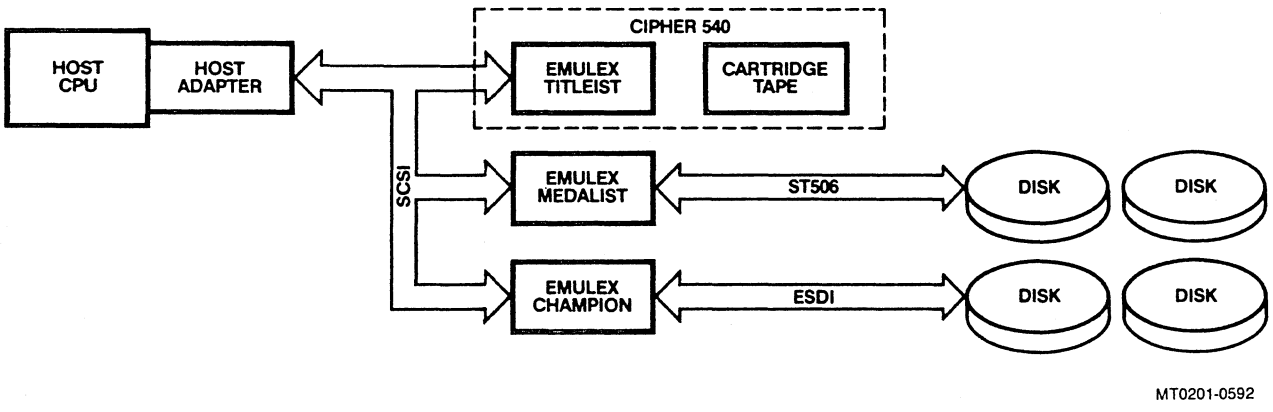


Figure 1-2. Sample SCSI Bus System Configuration

1.2.1 Features

MT02 Controller features are summarized below. More details on these features are given in subsequent sections.

- SCSI Implementation based on ANSI X3T9.2/82-2 Rev 14 B (06 Nov 84) Specification
- Support of QIC-11 and QIC-24 0.25-inch cartridge streaming tape formats
- Support of QIC-36 0.25-inch Cartridge Tape Drive Basic Interface
- Powerful SCSI command set including:

  -Standard Commands
  -Sequential Access Device Commands
  -**COPY** Command
  -Linked Command Support

- Support of disconnect/reconnect function
- Hard Reset
- Buffered operation to optimize tape streaming
- Extensive self-test and diagnostic facilities
- Compatibility with Emulex's ST506/ESDI disk controllers

There is one Dual In-Line Package (DIP) switch pack on the MT02 Controller. Switch SW1 is a ten-pole general control switch configuring SCSI bus device Identifications (IDs), tape drive parameters, and parity checking on the SCSI bus. For configuration details, see Section 3 (Installation).

1.3 Compatibility

Compatibility of the MT02 Controller with the SCSI host adapter systems and related microcontrollers and the tape drive is described in the following subsections.

1.3.1 SCSI Bus Hardware Compatibility

A disk drive or tape drive that is connected to the SCSI bus, and that follows the protocol outlined in the ANSI X3T9.2/82-2 SCSI Specification, is compatible with the MT02 Controller and 0.25-inch tape drive unit. A 50-pin male connector, reference designated J5, on the MT02 Controller plugs directly into the SCSI bus cable.

The MT02 Controller supports the single-ended SCSI bus option. The overall length of the cable that connects the SCSI host adapters and controllers in a daisy-chained manner can extend to 6 meters (20 feet). All SCSI bus signals in the cable are terminated at each end by terminating resistors of 220 ohms to +5 VDC, and 330 ohms to ground. Terminators are optionally installed on the MT02 Controller, and depend on the physical profile of the SCSI bus (see subsection 3.3.5 for details). The MT02 Controller complies with the FCC limits for a Class B computing device (see subsection 3.5).

1.3.2 SCSI Bus Protocol and Command Compatibility

The MT02 Controller contains an on-board SCSI protocol controller that controls SCSI protocol and the SCSI bus. The MT02 Controller supports the SCSI arbitration and reselection capabilities, and data bus parity. The MT02 Controller supports all standard SCSI commands described in the ANSI X3T9.2/82-2 SCSI specification. For more information on SCSI bus commands supported by the MT02 Controller, see Section 8.

1.3.3 SCSI Command Set

The hexadecimal codes for the SCSI commands supported by the MT02 Controller are shown in Table 1-1. Detailed command descriptions are given in Section 8.

Table 1-1. MT02 Controller SCSI Command Set

Group 0 Command	Hex Code	Group 0 Command	Hex Code
COPY	18	**ERASE**	19
INQUIRY	12	**LOAD/UNLOAD**	1B
MODE SELECT	15	**MODE SENSE**	1A
PREVENT/ALLOW MEDIUM REMOVAL	1E	**READ**	08
READ BLOCK LIMITS	05	**RECOVER BUFFERED DATA**	14
RELEASE UNIT	17	**REQUEST SENSE**	03
RESERVE UNIT	16	**REWIND**	01
SEND DIAGNOSTIC	1D	**SPACE**	11
TEST DRIVE READY	00	**VERIFY**	13
WRITE	0A	**WRITE FILE MARK**	10
READ REVISION LEVEL	C1		

1.3.4 Deviations From SCSI Standard

Because the MT02 Controller supports 0.25-inch tape drives that stream in a serpentine format, reverse tape movement is not supported (except in error recovery). Block sizes are fixed at 512 bytes, therefore, commands employing the Fixed Block bit have that bit set. (The Fixed Block bit is Byte 01, Bit 00 in the Command Descriptor Block; see Figure 8-1.)

The MT02 Controller has a cache memory that can be used to buffer data to optimize streaming performance (for more information on buffered operations, see subsection 5.3.2). When writing file marks, a vendor-unique option has been added to avoid flushing the cache. If this option is not used, the tape stops streaming after each file mark. With this option, and depending upon cache content, the data source may be fast enough to maintain the streaming mode.

The MT02 Controller does not support the SCSI command queuing function.

The MT02 Controller does not check Reserved bits, fields, and bytes to ensure they are zero.

Table 1-2 lists deviations from the SCSI Standard for each SCSI command supported by the MT02 Controller.

Table 1-2. MT02 Controller Deviations from the SCSI Standard

Command	Hex Code	Deviation
COPY	18	(1) Does not support third party copy operations. One of the peripheral devices involved in the copy operation must be connected to the MT02. However, the MT02 does support the third-party reservation operation needed for the copy operation. The MT02 supports block sizes of 256 and 512 bytes for external devices involved in the copy operation. (2) Does not support the priority field in the **COPY** parameter list.
ERASE	19	(1) The MT02 erases the entire tape, not just a portion of it, and it does so not just from the current position to the end-of-tape. (2) The Long bit (Byte 01, Bit 00) must be 1, otherwise the MT02 rejects the command.
INQUIRY	12	(1) The RMB flag in the **INQUIRY** Data Format is always 1 for removable media. (2) The device type is always 0 for sequential access devices.

(continued on next page)

Table 1-2. MT02 Controller Deviations from the SCSI Standard (continued)

Command	Hex Code	Deviation
INQUIRY (Continued)	12	(3) The device type qualifier is not used (it is always 0). (4) If the **INQUIRY** command is sent to a nonexistent LUN, the MT02 does not return any data during the Data In Phase. In this situation, it does not return a peripheral device type of 7F (hex) as specified in the SCSI standard. Instead, the MT02 sets the vendor-unique Nonexistent LUN bit in the status byte (returned during the Status Phase).
LOAD/UNLOAD	1B	(1) The MT02 does not support the Immediate bit (it returns status only after it positions the tape). (2) The EOT bit is vendor-unique. (3) The MT02 does not support the Immediate bit (Byte 01, Bit 00).
MODE SELECT	15	(1) The Speed field must be zero (use the default speed). The MT02 does not support the option to vary the speed. (2) The MT02 supports 3 tape densities: default (0.25 QIC-24), QIC-11 on 4-track, and QIC-11 on a 9-track tape. (3) The MT02 supports only 1 block descriptor. The recording density cannot be varied and the MT02 ignores the Number of Blocks field. (4) The block size is not selectable; the MT02 supports only block sizes of 512 bytes. (5) The Disable Erase Ahead (DEA) bit is vendor-unique. (6) The Auto-load option (AUI) bit is vendor-unique. (7) The Soft Error Reporting (SEC bit) is vendor-unique. (8) Selecting the buffered mode may affect the **VERIFY** command as well as the **WRITE** command. To select the buffered mode for the **VERIFY** command, the buffered mode bit and a vendor-unique bit in the **VERIFY** command (IMED bit) must both be cleared.
MODE SENSE	1A	(1) The Disable Erase Ahead (DEA) bit is vendor-unique. (2) The Auto-load option (AUI bit) is vendor-unique. (3) The Soft Error Reporting (SEC bit) is vendor-unique. (4) The MT02 returns vendor-unique values for the media type.
PREVENT/ALLOW MEDIUM REMOVAL	1E	The user cannot use the command to prevent the physical removal of the tape. The MT02 uses the command to illuminate a warning light.

(continued on next page)

Table 1-2. MT02 Controller Deviations from the SCSI Standard (continued)

Command	Hex Code	Deviation
READ	08	(1) The MT02 supports only fixed-length records. (2) The MT02 distinguishes between the logical end-of-media and physical end-of-media. The SCSI standard does not do so. (3) When it encounters the physical end-of-media, the MT02 sets the Sense Key to NO SENSE rather than MEDIUM ERROR (as specified in the SCSI standard).
READ REVISION LEVEL	C1	This is a vendor-unique command used to return the MT02 firmware revision level.
READ REVERSE	0F	The MT02 does not support this command.
RECEIVE DIAGNOSTIC RESULTS	1C	The MT02 does not support this command.
RECOVER BUFFERED DATA	14	The MT02 supports only fixed-length blocks.
REQUEST SENSE	03	(1) In the Standard Sense Data Format, the MT02 error class/code assignments are vendor-unique. (2) In the Extended Sense Data Format, the MT02 always returns error class/ code assignments as additional sense bytes. (3) The MT02 supports a vendor-unique option to report the number of recoverable errors.
REWIND	01	The MT02 does not support the Immediate bit (Byte 01, Bit 00).
SPACE	11	The MT02 does not support negative counts (which require backward tape motion).
TRACK SELECT	0B	The MT02 does not support this command.

1.3.5 Tape Drive Compatibility

The MT02 Controller can be installed up to 3 meters (6 feet) away from any 0.25-inch streaming cartridge tape drive that supports a QIC-36 Tape Drive Basic Interface. The tape drive connects to the MT02 Controller via a 50-pin connector reference designated J3 on the MT02 Controller. The MT02 Controller can also be installed in the subchassis of the tape drive by using the alternate mounting holes in the MT02 Controller. The MT02 Controller was designed specifically for use with the QIC-36 1/4-inch Cartridge Tape Drive Basic Interface, and uses the QIC-24 tape data format. This format provides 9-track, sequential, serpentine recording.

2.1 Overview

This section contains the specifications for the components on the MT02 Controller. A general description of each component is included under **FUNCTIONAL** in the General and Electrical Specifications table. For a detailed description of the MT02 Controller's function as a whole, see Section 5, Functional Description. The general, electrical, physical, and environmental specifications for the MT02 Controller are described in separate subsections, as listed in the following table.

Subsection	Title
2.1	Overview
2.2	General and Electrical Specifications
2.3	Physical Specifications
2.4	Environmental Specifications

2.2 General and Electrical Specifications

Table 2-1 lists and describes the general and electrical specification for the MT02 Controller.

Table 2-1. General and Electrical Specifications

Parameter	Description
FUNCTIONAL	
Design	High-speed microprocessor based tape controller for QIC-36 Basic Interface 0.25-inch cartridge tape drive
SCSI Bus/Controller Interface	Standard SCSI bus interface (ANSI X3T9.2/82-2 specification), via a 50-pin male connector
Tape Drive Interface	QIC-36 Basic Interface 1/4-inch GCR 8000 bits-per-inch streaming tape drive, via a 50-pin connector

(continued on next page)

Table 2-1. General and Electrical Specifications (continued)

Parameter	Description
FUNCTIONAL	
Subsystem	Single non-intelligent tape drive Configuration and controller per subsystem
Tape Media	0.25-inch, 600-foot or 450-foot tape data cartridge
Tape Speed	90 inches-per-second (ips)
Tape Density	8000 bits-per-inch (bpi) (10,000 flux changes per inch)
Recording Mode	Serial GCR recording in QIC-11 or QIC-24 tape data format
Data Block Capacity	512 bytes per block, fixed
Data Burst Rate	1.25 megabytes/second
Track Configuration	4 or 9 data tracks, with sequential, serpentine track recording
Data Buffering	16 kbytes (approximately 2 kbytes for operating system and program, 14 kbytes for data buffering)
Max. Burst Rate	1.25 Megabytes/second on SCSI bus
Self-Test	Controller automatically executes power-up Self-Test Diagnostic routines
INDICATORS	
Fault/Activity Display	Light-emitting diodes (LEDs) indicate detected MT02 Controller fault and load activity; MT02 Controller provides signals that can be used to control off-board LEDs
Option/Configuration Switches	On-board switch module for MT02 Controller configuration

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Table 2-1. General and Electrical Specifications (continued)

Parameter	Description
INTERFACES	
Bus Interface	Standard SCSI bus single-ended option uses approved receivers and drivers
Transport Interface	Standard QIC-36 Basic Interface. Cable length up to 3 meters (10 feet).
RELIABILITY	
Mean-Time Between Failures (MTBF)	65,040 hours
ELECTRICAL	
Power	+5 VDC, ± 5%, 1.5 amperes (amps) nominal +12 VDC, ±5%, 40 milliamps nominal

2.3 Physical Specifications

Figure 2-1 shows the physical dimensions of the MT02 Controller. Table 2-2 lists and describes the physical specifications for the MT02 Controller.

Table 2-2. Physical Specifications

Parameter	Description
Packaging	Single printed circuit board assembly (PCBA), 5.25-inch footprint, 5.75-inch by 8-inch
Cabling	Single 50-conductor, flat-ribbon cable to tape transport, maximum length of 3 meters (10 feet); 50-conductor flat ribbon cable to SCSI connector, maximum length of 6 meters (20 feet)
Mounting	May be mounted up to 3 meters (10 feet) away from tape transport frame; Emulex recommends mounting the controller on the drive itself

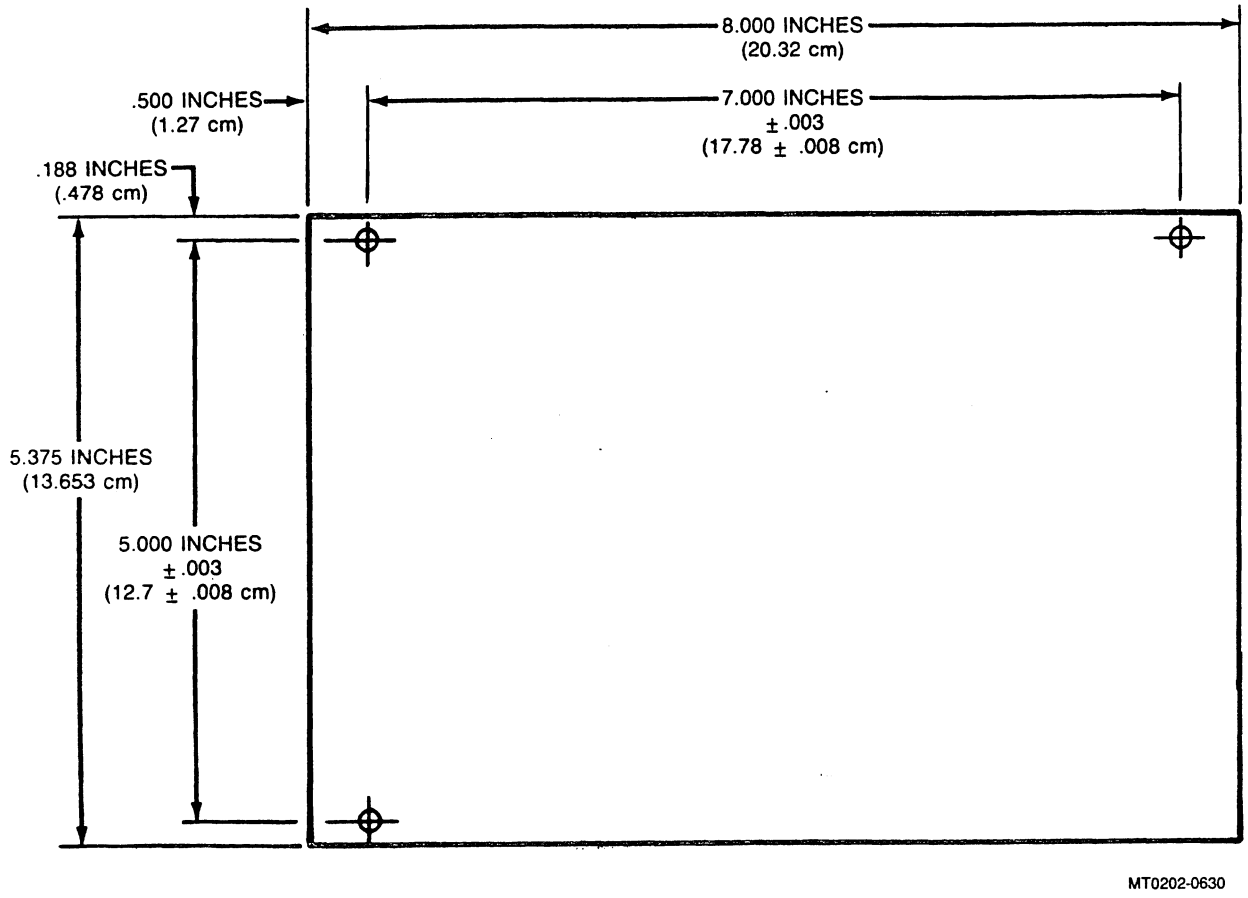


Figure 2-1. MT02 Controller Dimensions

2.4 Environmental Specifications

Table 2-3 lists and describes the environmental specifications for the MT02 Controller.

Table 2-3. Environmental Specifications

Parameter	Description
Temperature (Operating)	5°C - 50°C (41°F - 122°F)

BLANK

3.1 OVERVIEW

This section describes the step-by-step procedure for installing the MT02 Controller, including switch setting data and physical installation instructions. This installation procedure is divided into six subsections, as listed in the following table:

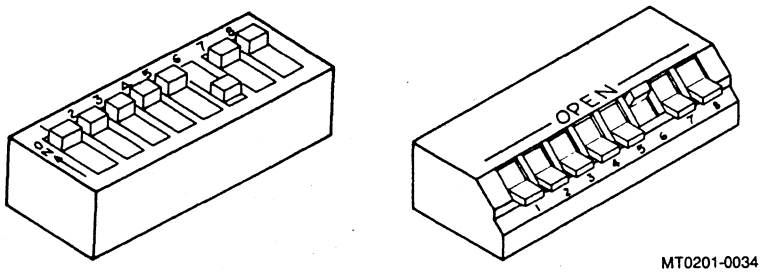
Subsection	Title
3.1	Overview
3.2	Inspection
3.3	MT02 Controller Setup
3.4	MT02 Controller Installation
3.5	FCC Compliance
3.6	Tape Cartridges

If you are unfamiliar with the MT02 Controller installation procedure, we recommend reading this Installation Section before beginning.

3.1.1 DIP Switch Types

Switch-setting tables in this manual use the numeral one (1) to indicate the ON (closed) position and the numeral zero (0) to indicate the OFF (open) position.

Figure 3-1 shows the two DIP switch types used in this product. Both switches are set to the code shown in the switch setting example.



----------SW1----------

1	2	3	4	5	6	7	8
1	1	1	1	1	0	1	1

Figure 3-1. Switch Setting Example

3.2 Inspection

Emulex products are shipped in special containers designed to provide full protection under normal transit conditions. Immediately upon receipt, the shipping container should be inspected for evidence of possible damage incurred in transit. Any obvious damage to the container, or indications of actual or probable equipment damage, should be reported to the carrier company in accordance with instructions on the form included in the container.

Unpack the MT02 Controller and verify that all components listed on the shipping invoice are present. Verify that the model or part number (P/N) designation, revision level, and serial numbers agree with those on the shipping invoice. These verifications are important to confirm warranty. If evidence of physical damage or identity mismatch is found, notify an Emulex representative immediately.

A visual inspection of the MT02 Controller is recommended after unpacking. Specific checks should be made for such items as bent or broken connector pins, damaged components, or any other visual evidence of physical damage. Carefully examine all socketed components to ensure that they are firmly and completely seated.

3.3 MT02 Controller Setup

The switches in DIP switch pack SW1 on the MT02 Controller allow configuration of various options available with the MT02 Controller. All switches on the MT02 Controller are set to a standard configuration before the MT02 Controller is shipped from the factory. DIP switch functions are listed and described in applicable tables in this section. Table 3-1 lists the function and factory configuration of all switches on the MT02 Controller. This subsection provides an overview of the switch settings, as well as a description of the function of each switch.

Figure 3-2 shows the locations of the configuration switches, connectors, and jumpers referenced in the following subsections. Jumpers A and B are used to select the memory size of the EPROM on the MT02 Controller. The jumpers are connected on the factory version of the MT02 Controller; they must remain connected.

Table 3-1. DIP Switch Settings, MT02 Controller

Switch	Factory Setting	Function	Section
SW1-1	ON (1)	SCSI Bus Address Bit 0	3.3.1
SW1-2	OFF (0)	SCSI Bus Address Bit 1	3.3.1
SW1-3	OFF (0)	SCSI Bus Address Bit 2	3.3.1
SW1-4	OFF (0)	Not Used	--
SW1-5	OFF (0)	Tape Drive Type	3.3.2
SW1-6	OFF (0)	Tape Drive Type	3.3.2
SW1-7	OFF (0)	Tape Drive Type	3.3.2
SW1-8	OFF (0)	SCSI Bus Parity Check	3.3.3
OFF (0) = Open ON (1) = Closed			

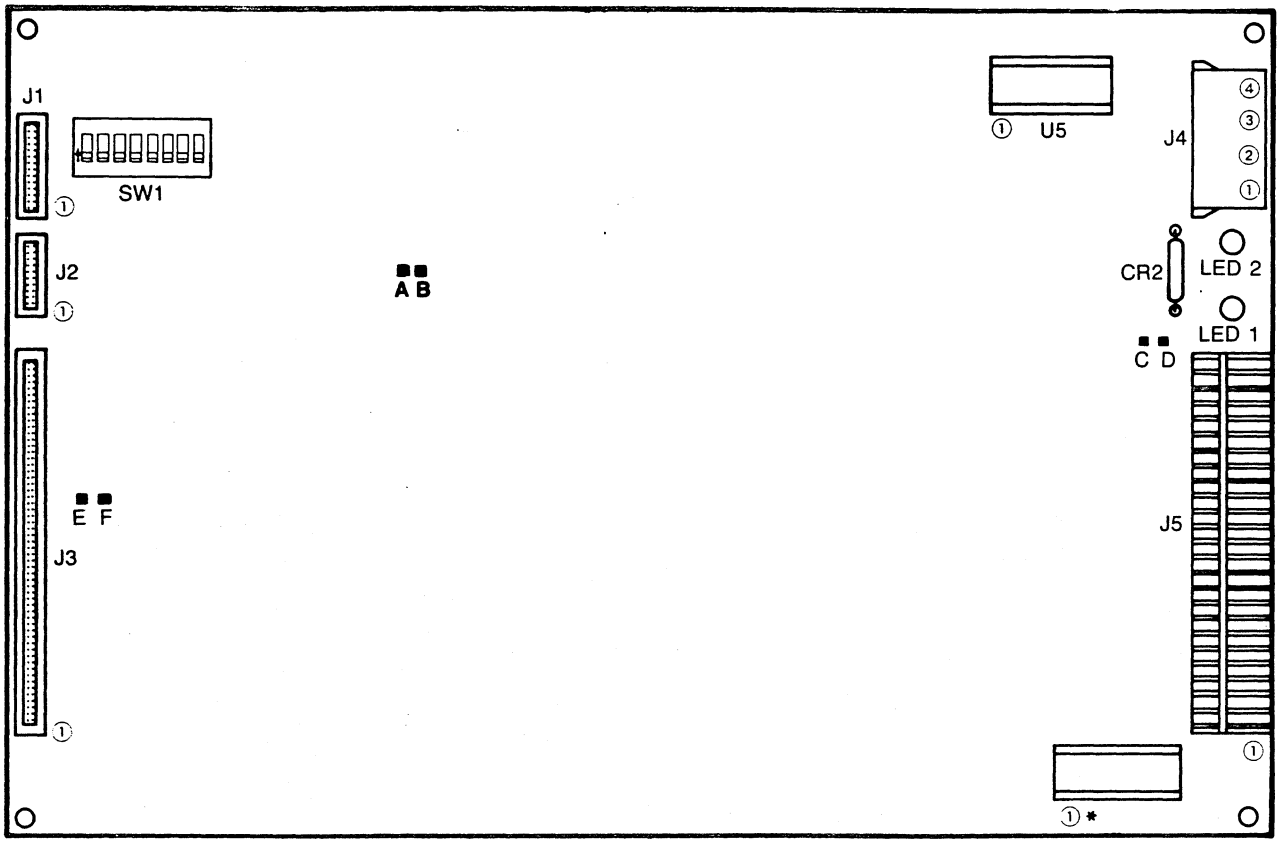


Figure 3-2. MT02 Controller Switch and Jumper Locations

3.3.1 SCSI Bus Device Address (SW1-1 through SW1-3)

Switches SW1-1, SW1-2, and SW1-3 are used to select any one of eight possible SCSI bus addresses. This address establishes the SCSI bus identity of the MT02 Controller in the system. An Initiator must specify this address to select the MT02 Controller as a Target device. Switch setting for the eight possible MT02 Controller Device Address identities are listed in Table 3-2. Make sure you do not assign the same SCSI Bus Device Address to two separate host adapters or controllers.

Table 3-2. SCSI Bus Device Address Selection Switches

Switch			SCSI Device Address
SW1-3	SW1-2	SW1-1	
0	0	0	00
0	0	1	01
0	1	0	02
0	1	1	03
1	0	0	04
1	0	1	05
1	1	0	06
1	1	1	07
0 = OFF (OPEN)		1 = ON (CLOSED)	

3.3.2 Tape Drive Type (SW1-5 through SW1-7)

Switches SW1-5 through SW1-7 are used to specify the type of tape drive connected to the MT02 Controller and the Tach rate supported for that specified tape drive. Supported tape drive types and their Tach rates are listed in Table 3-3.

3.3.3 SCSI Bus Parity Check (SW1-8)

The MT02 Controller always generates parity on the SCSI bus. However, the MT02 Controller must be configured to check parity on the SCSI bus. Switch SW1-8 indicates whether the MT02 Controller checks parity on the SCSI bus. Setting switch SW1-8 to ON causes the MT02 Controller to check parity on the SCSI bus. Setting switch SW1-8 to OFF causes the MT02 Controller to ignore parity on the SCSI bus.

The use of parity is a system option. Either all SCSI bus devices must generate and detect parity, or all SCSI bus devices must not generate and detect parity. Parity is not valid during the Arbitration Phase (see subsection 7.3.1). Normally, switch SW1-8 is set to OFF, as listed in the following table:

Switch	OFF	ON	Factory
SW1-8	Parity is not checked	Parity is checked	OFF

Table 3-3. MT02 Controller Tape Drive Types

SW1-7 MSB	Switch SW1-6	SW1-5 LSB	Tape Drive Type	Tach Rate
0	0	0	* Cipher (QIC-36)	122 mils
0	0	1	* Archive Scorpion	193 mils
0	1	0	** Wangtek (Series 5000 Basic)	145 mils
0	1	1	** Wangtek (Series 5000E)	145 mils
1	0	0	** Kennedy 6500	145 mils
1	1	0	Not Used	
1	1	1	Not Used	

0 = OFF (OPEN) 1 = ON (CLOSED)

* The MT02 Controller controls write current for this tape drive; see subsection 3.3.6.

** Although the tach rate is the same for these tape drives, the MT02 must use different methods to determine cartridge size for these 3 drives.

3.3.4 SCSI Bus External Termination Power Option

The SCSI Termination option allows the MT02 Controller to supply between +4 and +5 VDC power to the subsystem's external terminators via pin 26 of the SCSI bus. The SCSI Termination option is not required if the MT02 Controller is resident in an Emulex subsystem.

If the SCSI Termination option is required, install a #1N5817 diode at reference designator CR2 on the MT02 Controller printed circuit board assembly (PCBA). Also connect a wire-wrap jumper between jumper posts C and D on the MT02 Controller (see Figure 3-2) to supply between +4 and +5 VDC for the SCSI bus external termination.

Note that it is not necessary to install this option for the board terminators to work properly. (See section 3.3.5 below.)

CAUTION

If the diode leads are reversed so that the anode of the diode is in the wrong hole, the system does not function properly.

If diode CR2 is to be installed, insert the diode leads in holes provided at the upper right portion of PCBA (see Figure 3-2). The anode of the diode must be inserted in the hole next to reference designator CR2. After proper insertion of the diode, secure it in place by soldering its leads on the reverse (solder) side of the PCBA.

3.3.5 SCSI Bus Termination

The MT02 Controller can be configured to terminate the SCSI bus by inserting one 220/330-ohm resistor pack in each of the two sockets located at U5 and U45 (U46 on Assembly Number MT0210403) on the MT02 Controller (see Figure 3-2). The resistor packs are available in the Emulex SCSI terminators kit, P/N MD0113002. A SCSI system configuration should contain only two devices that terminate the SCSI bus. Usually these devices are a host adapter and one peripheral device controller (such as the MT02 Controller), or an external terminator pack.

3.3.6 Write Current Selection

Jumpers E and F (see Figure 3-2) are used to allow the MT02 Controller to provide a High/Low Write current for Cipher 540 and Archive tape drives. Connect jumper posts E and F with a wire-wrap jumper for these tape drives. On the MT02 Controller that has Assembly Number MT0210403, there is no need to make this connection.

3.4 MT02 Controller Installation

The instructions in this subsection describe the procedure for configuring the MT02 Controller and connecting various cables to it. The MT02 Controller contains several mounting holes for installing it either in the subchassis of the tape drive that supports the QIC-36 interface, or up to 3 meters (10 feet) away from the tape drive. The location of the MT02 Controller is dependent on tape drive and system requirements. To install the MT02 Controller, see Figures 3-3 and 3-4 and use the following procedure:

1. Configure the MT02 Controller. This action involves setting switches SW1-1 through SW1-8 before installing the MT02 Controller. All switches have been set at factory; however, you may need to reset certain switches to satisfy your specific needs.

2. Install the MT02 Controller in the subchassis of the tape drive or up to 3 meters away from the tape drive.

3. Connect the data cable from the tape drive to 50-pin connector J3 on the MT02 Controller (see Figure 3-3).

4. Connect the cable from the power supply to power connector J4 on the MT02 Controller (see Figure 3-3).

5. Connect the SCSI bus cable to SCSI bus connector J5 on the MT02 Controller (see Figure 3-4).

NOTE

Note that Figure 3-4 shows a SCSI flat-ribbon cable that is used to internally connect the MT02 Controller with a SCSI host adapter. If the MT02 Controller and SCSI host adapter reside in different cabinets, you must use a shielded SCSI cable to connect them to maintain FCC compliance (see subsection 3.5). For more information on shielded cable requirements, see subsection 6.2.1.2.

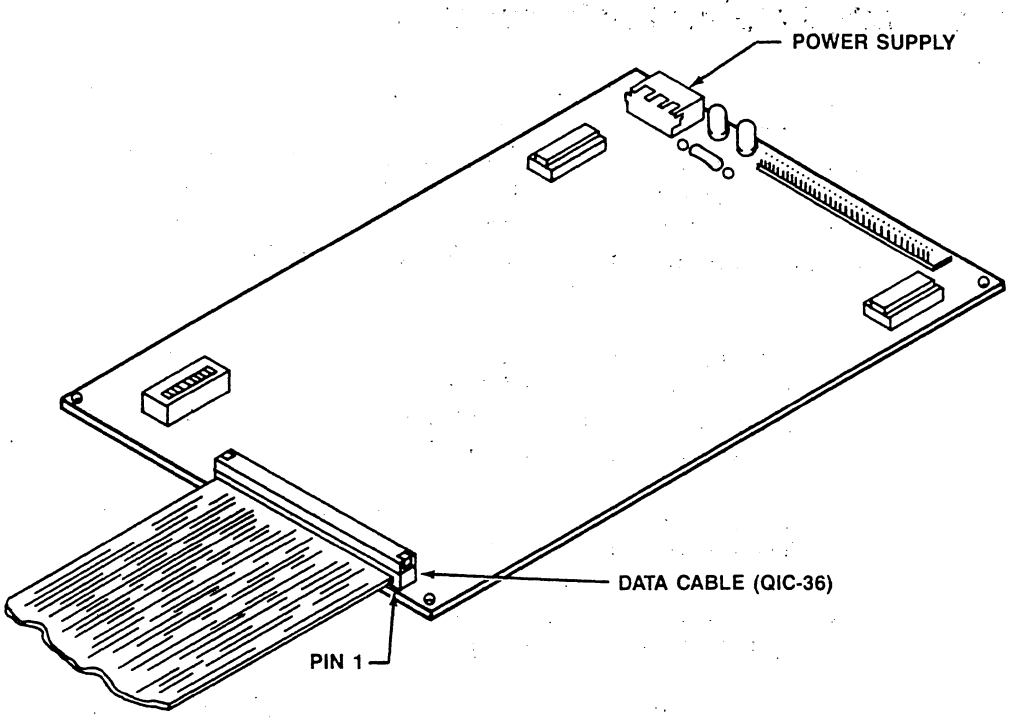


Figure 3-3. Connecting the Tape Drive Data Cable to the MT02 Controller

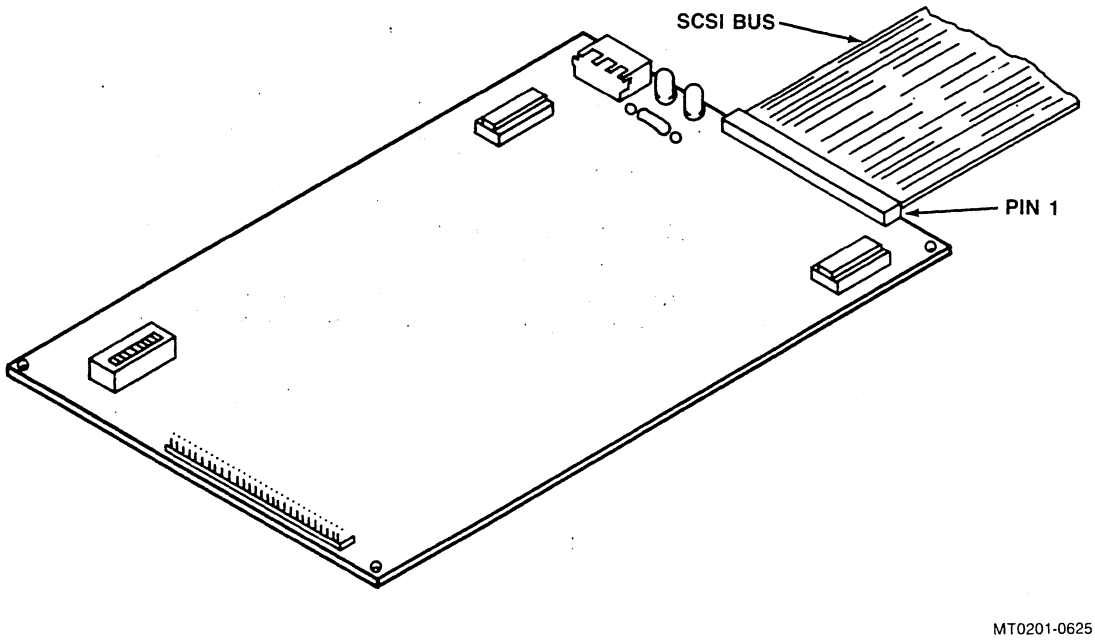


Figure 3-4. Connecting the SCSI Bus Cable to the MT02 Controller

3.5 FCC Compliance

The Federal Communications Commission (FCC) has established technical standards regarding radiation of electromagnetic interference (EMI) emitted by computing devices. The MT02 Controller has been type tested and found to comply with the EMI emission limits for a Class B computing device in accordance with the specifications in Subpart J of Part 15 of FCC Rules. However, there is no guarantee that interference will not occur in a particular installation.

The MT02 Controller was tested for FCC compliance in a compliant subsystem that was properly shielded (enclosed so that no electro-magnetic radiation escapes). The subsystem was connected to other SCSI port devices via a shielded SCSI cable. Emulex offers shielded cables, compatible with the MT02 Controller, that are available in various lengths. For information on SCSI bus cable and connector requirements, see subsection 6.2.1.

Since the MT02 Controller equipment generates and uses radio frequency energy, if it is not installed and used in strict accordance with Emulex's instructions, it may cause EMI with radio and television reception. It is the responsibility of the user to properly install the MT02 Controller in the tape drive subsystem chassis and to properly install the MT02 Controller and tape drive unit in a compliant subsystem. MT02 Controller installation instructions are described in subsection 3.4. Emulex is not responsible for any radio or TV interference caused by unauthorized modifications to the MT02 Controller.

If the MT02 Controller causes interference with radio or television reception, as determined by turning the equipment on and off, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient the receiving antenna.
- Relocate the compliant subsystem (that contains the MT02 Controller) with respect to the receiver.
- Move the compliant subsystem away from the receiver.
- Plug the compliant subsystem into a different outlet so that the subsystem and receiver are on different branch circuits.
- Verify that the mounting screws and grounding wires on the compliant subsystem are tightly secured.

If necessary, you should consult the dealer or an experienced radio/television technician for additional suggestions. You may find helpful a booklet prepared by the FCC:

Title:	How to Identify and Resolve Radio-TV Interference Problems
Publication Number:	Stock No. 004-000-00345-4
Publisher:	U.S. Government Printing Office Washington, DC 20402

3.6 Tape Cartridges

Emulex recommends two kinds of blank tape cartridges for use with the MT02 Controller. These cartridges have been tested and certified to exhibit low error rates. The following table lists the cartridges types by Emulex part number.

Emulex Part Number	Length (in feet)
1090025	450 feet
1090037	600 feet

NOTE

Three other types of blank tape cartridges can be used with the MT02 Controller: 150 feet, 300 feet, and 555 feet. However, currently Emulex does not test and certify these types of cartridges.

SECTION 4
TROUBLESHOOTING

4.1 Overview

This section describes the diagnostic features with which the MT02 Controller is equipped. MT02 Controller diagnostic modes include power-up (and reset) self-test and online host-initiated diagnostic facilities. The principal function of these tests is to determine MT02 Controller functional integrity and to distinguish failures of the MT02 Controller from those of the tape drive. This section is divided into four subsections, as listed in the following table:

Subsection	Title
4.1	Overview
4.2	Self-Test Procedures
4.3	Online Diagnostic Commands
4.4	MT02 Controller LEDs

4.1.1 Service

The components of your Emulex MT02 Controller have been designed to give years of trouble-free service, and they were thoroughly tested before leaving the factory.

If one of the diagnostic procedures described in this section indicates that a component is not working properly, the MT02 Controller must be returned to the factory, or to an Emulex authorized repair center, for service. Emulex products are not designed to be repaired in the field.

Before returning the component to Emulex, whether the product is or is not under warranty, you must contact Emulex's Technical Support for instructions and a Return Materials Authorization (RMA) number.

DO NOT RETURN AN MT02 CONTROLLER TO EMULEX WITHOUT AUTHORIZATION. An MT02 Controller returned for service without an authorization will be returned to the owner at the owner's expense.

In the continental United States, Alaska, and Hawaii contact:

Emulex Customer Support
3545 Harbor Boulevard
Costa Mesa, CA 92626
(714) 662-5600 TWX 910-595-2521

Outside the United States, contact the distributor from whom the MT02 Controller was initially purchased.

After you have contacted Emulex and received an RMA number, package the MT02 Controller (preferably by using the original packing material) and send it **POSTAGE PAID** to the address supplied by the Emulex representative. The sender should also insure the package.

4.2 Self-Test Procedures

MT02 Controller performs a self-test procedure when it operates in either of two modes: the Normal mode or the Burn-In mode. These two modes and their corresponding self-test procedures are described in the following subsections.

4.2.1 Normal Mode

The MT02 Controller operates in the Normal mode when it performs typical tape controller functions such as a Tape Format operation or a read operation. When the MT02 Controller is operating in the Normal mode and power-up or reset conditions occur, it performs a self-test procedure to determine whether its interface circuits, memory, and on-board microprocessor are operative. The self-test procedure consists of several individual tests that exercise separate components of the MT02 Controller. These tests are performed sequentially; the success of one test enables the next test to be executed. If an individual test fails, the MT02 Controller self-test procedure stops at the location of the failure.

Before the self-test procedure begins, a Power-up Reset Clear code is output to the two on-board LEDs to indicate that the MT02 Controller is ready to perform a self-test. If the MT02 Controller self-test procedure succeeds, a Self-Test Pass code is output to the on-board LEDs. The LED locations on the MT02 Controller are shown in Figure 4-1, and LED Test Code descriptions are listed in Table 4-1.

Table 4-1. LED Test Code Descriptions

LED 2	LED 1	Test Description
0	0	Power-up Reset Clear
1	1	Power-Up Self-Test Pass Code
0 = OFF (not lit)		1 = ON (lit)

If the MT02 Controller is operative, LED 1 (see subsection 4.4) blinks. If the MT02 Controller fails its self-test procedure, LED 1 does not blink.

After the self-test procedure is successfully completed, the MT02 Controller continues with the initialization routine. If the SCSI interface circuits and the 8031 microprocessor are functioning, the MT02 Controller enters the online mode and is available to the Initiator. Failures in the Tape Formatter and/or tape drive result in a CHECK CONDITION status code in response to the completed **TEST UNIT READY** command (see subsection 8.3.17) or in response to a completed data transfer command (such as **READ** or **WRITE**). Further analysis of these failures can be made by using the **SEND DIAGNOSTIC** command (see subsection 8.3.15).

NOTE

If the MT02 Controller self-test procedure is initiated online, the host-supplied device parameter definitions are lost. The host must resubmit the parameters to the MT02 Controller by using the **MODE SELECT** command (see subsection 8.3.5).

4.2.2 Burn-In Mode

During the Burn-In mode, the MT02 Controller self-test procedure is repeated continuously until a failure is detected. The MT02 Controller contains two connectors used to report self-test failures when the MT02 Controller is operating in the Burn-In mode. Eight bits are provided from four pin assignments on the Burn-In Connector, reference designator J1 on the MT02 Controller (see Figure 3-2), and four pin assignments on the User's Panel Connector, reference designator J2 on the MT02 Controller (see Figure 3-2). The Burn-In Connector pin assignments are shown below:

Bit	07	06	05	04	03	02	01	00
Connector	J1-9	J1-8	J1-7	J1-12	J2-4	J2-6	J2-7	J2-9

As each individual test is performed during the MT02 Controller Burn-In mode, a test code is output to the connectors to indicate which component on the MT02 Controller is currently being tested. If an individual test fails, the corresponding test code is output. The individual tests in the self-test procedure and their corresponding hexadecimal codes are listed in Table 4-2.

To establish the MT02 Controller Burn-In mode, ground pin J1-5. Once the Burn-In mode has been established, to cause the MT02 Controller to perform its self-test procedure continuously, ground pin J2-8 and reset the MT02 Controller.

Table 4-2. MT02 Controller Test Code Descriptions

Test Code* (hexadecimal)	Test Description
00	Power-up Start Code
01	Buffer Controller Reset Status Test
03	Tape Formatter Reset Status Test
04	SCSI Reset Latch Test
40	8031 Microprocessor Self-Test
41	ROM Checksum Test
42	Buffer Controller LSI Register Test
43	External RAM Data Test
44	External RAM Parity Test
45	Buffer Controller LSI Parity Detection Test
46	Buffer Controller LSI Parity Interrupt Test
82	Tape Formatter LSI Register Test
83	SCSI Controller LSI Self-Diagnostic Test
84	SCSI Controller LSI Interrupt Test
85	SCSI Controller LSI Register Test
* Asserted bits are low true.	

4.3 Online Diagnostic Commands

MT02 Controller diagnostics are specified and executed by the **SEND DIAGNOSTIC** command (see subsection 8.3.15). The host may detect the diagnostic has passed if the MT02 Controller responds to other commands following its Reset condition. If a failure occurs, the MT02 Controller halts and the failure is indicated by the test code output at the Burn-In Connector (see Table 4-2). The host adapter can issue a SCSI bus Reset Condition to cause a retry of the diagnostics.

NOTE

Execution of the Send Diagnostic command results in an MT02 Controller Reset function.

4.4 MT02 Controller LEDs

The locations of the two MT02 Controller on-board LEDs are shown in Figure 4-1.

LED 1 indicates the status of the MT02 Controller. LED 1 blinks on and off when the MT02 Controller is operating properly. LED 1 remains either illuminated or extinguished if the MT02 Controller malfunctions or has encountered a fatal hardware condition. If this last situation occurs, the MT02 Controller must be reset to recover from the fatal hardware condition.

LED 2 indicates when it is not safe to remove the tape cartridge. When LED 2 (also called the Unsafe to Remove Cartridge LED) is illuminated, a tape cartridge is currently inserted in the tape drive and one of the following conditions is also true:

- the MT02 Controller receives a **LOAD** command
- the tape is loaded using the MT02 auto-load option
- a **PREVENT MEDIUM REMOVAL** command is received.

The MT02 Controller turns off the LED 2 when one of these 3 conditions occur:

- it executes an **UNLOAD** command (unless there is an outstanding **PREVENT MEDIUM REMOVAL** request)
- an **ALLOW MEDIUM REMOVAL** command is received and there is no logically loaded tape
- it detects a Unit Attention condition on the SCSI bus (see subsection 7.6.3).

An Initiator can also issue an **PREVENT/ALLOW MEDIUM REMOVAL** command (see subsection 8.3.7) to control the actions of LED 2.

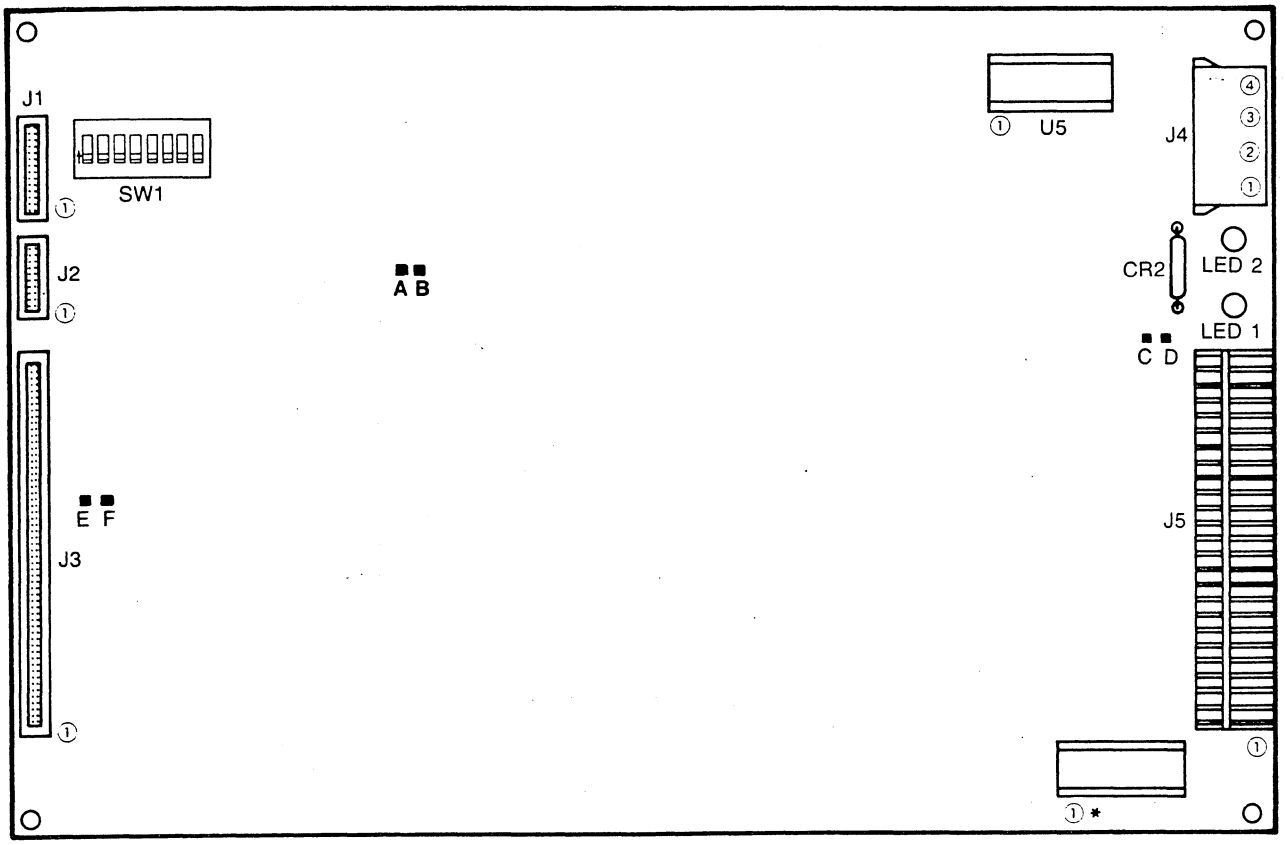


Figure 4-1. Locations of LEDs on the MT02 Controller

SECTION 5
FUNCTIONAL DESCRIPTION

5.1 Overview

This section describes MT02 Controller architecture and tape operation. For reference convenience, this section is divided into three subsections, as listed in the following table:

Subsection	Title
5.1	Overview
5.2	MT02 Controller Architecture
5.3	Tape Operations

5.2 MT02 Controller Architecture

Figure 5-1 is a block diagram that shows the major functional elements of the MT02 Controller. The MT02 Controller is organized around the 8031 microprocessor, and the tape formatter and buffer controller custom VLSI chips designed by Emulex.

Two buses are used in the MT02 Controller: the data bus and the microprocessor bus.

The data bus is connected directly to the tape formatter, buffer memory, and buffer controller. The buffer controller is connected directly to the buffer memory and the microprocessor bus. Therefore, the data bus and buffer controller provide a data path between the buffer memory, the 8031 microprocessor, and the registers in the tape formatter.

The microprocessor bus provides a path for transmission of control and status information. This information can be passed between the 8031 microprocessor, the EPROM, the buffer controller, and the Tape Control IC. The Tape Control IC controls the tape format (QIC-24 or QIC-11).

The MT02 Controller SCSI Interface is implemented using a single LSI chip on the MT02 Controller. In response to commands from the Initiator, the chip establishes and monitors SCSI bus phases appropriate to the command. It performs SCSI signal control and timing functions.

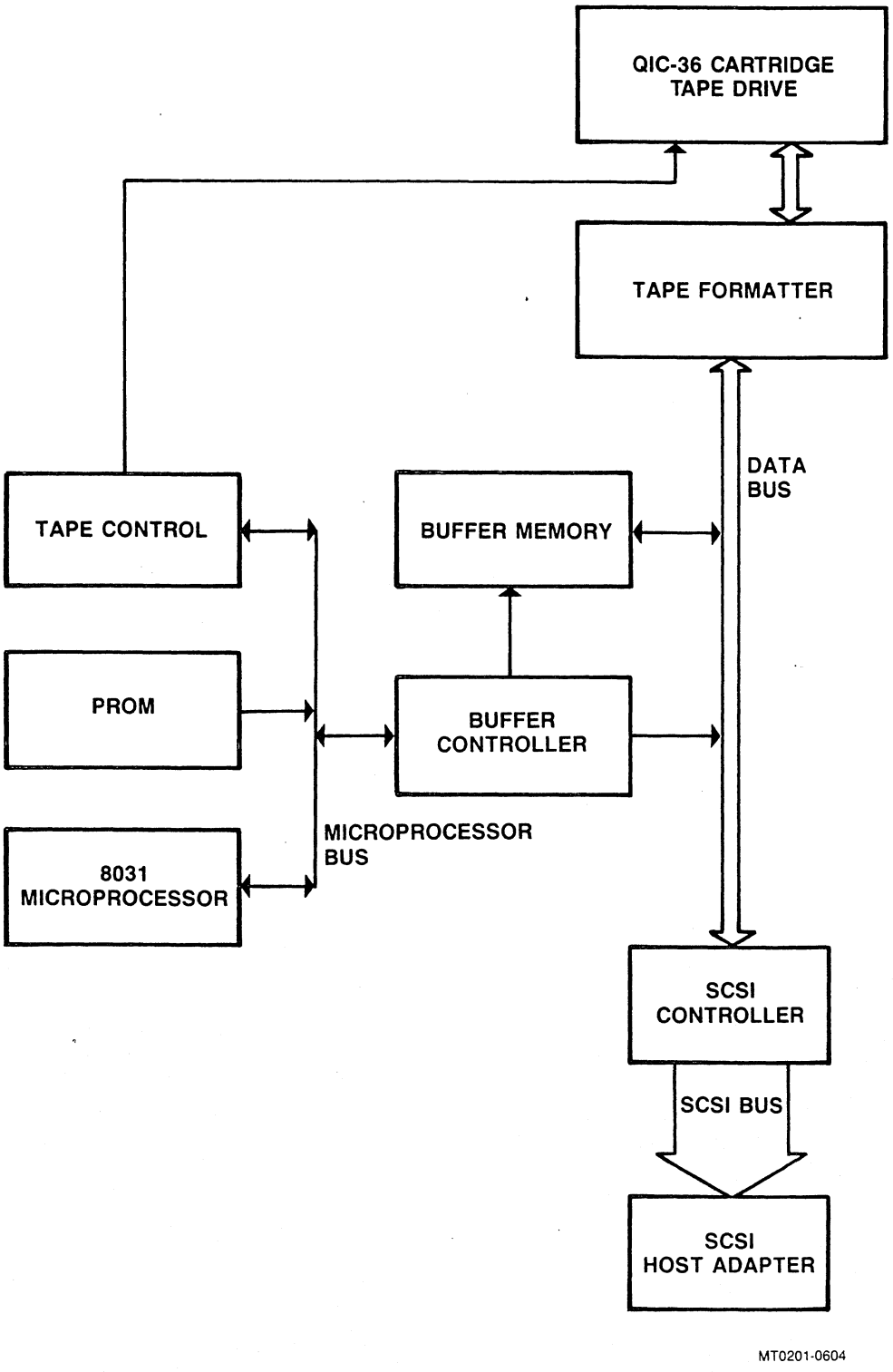


Figure 5-1. MT02 Controller Block Diagram

5.2.1 8031 Microprocessor

The 8031 microprocessor (with the tape formatter) controls all tape drive operations. These operations include drive control, head positioning, and reading drive status. The tape formatter controls formatting of the non-return to zero change on one (NRZI) GCR data that is written to, and read from, the tape drive. The 8031 microprocessor generates read and write commands that are executed by the tape formatter.

5.2.2 Tape Formatter

The tape formatter is a 40-pin VLSI integrated circuit (IC) fabricated with CMOS gate-array technology. This circuit, in conjunction with the 8031 microprocessor, handles the QIC-24 and QIC-11 format procedures on the tape during read and write operations.

5.2.3 Buffer Controller

The buffer controller is a 68-pin VLSI IC fabricated with CMOS gate-array technology. The circuit is basically a three-channel DMA controller. The buffer controller controls data movement in or out of a dynamic buffer memory and provides the connection between the microprocessor bus and the data bus.

The buffer controller circuit provides the address and control for multiple MT02 Controller activities that access a dynamic buffer memory. The buffer controller performs the following operations:

- handles addressing and control operations for the tape formatter
- handles dynamic memory timing and refresh
- performs parity checking and generation for the buffer memory
- connects the microprocessor bus to the data bus
- decodes the microprocessor address for the buffer memory and the internal input/output (I/O) space in the MT02 Controller
- determines priority of buffer memory access.

5.3 Tape Operations

The following subsections describe MT02 Controller functions during tape operations.

5.3.1 Tape Streaming

Tape streaming refers to the tape drive condition where tape motion does not stop between records and the inter-record gap is minimal. The use of streaming allows for the most efficient use of the tape media itself and generally increases total throughput.

To use the MT02 in a streaming mode, the host system must maintain an average data throughput rate of 100K bytes per second. Once the tape is up to speed, it takes approximately 5 milliseconds (ms) to read or write 1 block (512 bytes). Consequently, when writing to tape, the Initiator should present data at an average rate of 1 block every 5 ms. When reading from tape, the Initiator should accept data at an average rate of 1 block every 5 ms. To design host software which utilizes the MT02 and its associated tape drive most efficiently, the designer must understand the factors stated above as well as the actual SCSI bus transfer rate and overhead time in the host system interface.

5.3.2 Cache Buffer

In order to utilize the tape in streaming mode whenever possible, the MT02 Controller uses an internal RAM buffer (approximately 14K bytes) as a cache. Use of the cache decreases the impact of data underrun conditions during write operations, data overrun conditions during read operations, and data errors.

A block occupies one buffer in the cache. The cache on the MT02 Controller allows for read-ahead of up to 25 blocks and write buffering of up to 28 blocks. In write mode, the MT02 will buffer 4 blocks in the cache before it actually begins the tape motion; this is referred to as the write start threshold. In read mode, the MT02 attempts to maintain at least 7 blocks of read data in the cache at all times; this is referred to as the read start threshold.

NOTE

During read operations, the tape motor will not actually be started to read more tape records until the number of full buffers in the cache drops below the read start threshold.

During read operations, the MT02 uses the cache buffer in the following manner:

a. When the number of filled buffers in the cache drops below the read start threshold (which is 7 blocks in the cache), the MT02 starts the tape.

b. If possible, before stopping the tape, the MT02 will fill the cache (25 read buffers) with data read.

c. When the tape is stopped (cache full), the motor is reversed. Tape motion continues backward past the last block read for a distance of approximately 60 inches. When the number of filled buffers in the cache drops below the read start threshold, a read operation begins again by starting the tape motor in the forward direction. When the block following the last block read previously is found, the MT02 begins normal read operations to the cache.

d. If the cache becomes empty during the execution of a **READ** command (all of the data previously read into the cache has been passed to the Initiator), the MT02 disconnects from the SCSI bus. It reconnects when either the remaining requested blocks have been read or when 6 blocks have been read, whichever condition is smaller. Actual tape read operations will continue until the cache is full (25 buffers).

During write operations, the MT02 uses the cache buffer in the following manner:

a. When the number of blocks transferred from the Initiator to the cache reaches the write start threshold (which is 4 blocks in the cache), the tape is started. The MT02 will continue writing to tape as long as there is data in the cache.

b. If the cache is filled (the Initiator is passing data to the MT02 faster than it can be written to tape), the MT02 disconnects from the SCSI bus. It will reconnect when 6 blocks have been written, which enables 6 buffers in the cache to accept more data from the Initiator.

c. If the cache becomes empty (the MT02 is writing to tape faster than the Initiator is passing data to the MT02), the write operation stops. If the MT02 is currently writing on track 0, the erase operation continues for approximately 55 inches and the motor is reversed. If the MT02 is not writing on track 0, or if the disable erase ahead option (see subsection 5.3.8) is being used, the motor is reversed immediately. Tape motion then continues back past the last block written for approximately 60 inches and then stops. When the number of blocks transferred from the Initiator to the cache reaches the write start threshold, the write operation continues again by starting the motor in the forward direction. Blocks written previously are read until the last block written is encountered, at which time the write operation begins again.

d. If the host has disabled the buffered mode operation (specified in the **MODE SELECT** command), no data will be left in the cache at the end of execution of a **WRITE** command, regardless of whether the write start threshold has been reached.

NOTE

There is no overlapping use of the cache for read and write operations. Before a write operation can occur after a read operation, the host must first position the tape to the end-of-recorded-media. This action effectively flushes the cache. Before a read operation can occur after a write operation, the host must first rewind the tape. This action flushes the cache. (The cache is also flushed of write buffers during the execution of a **WRITE FILE MARK** command or an **UNLOAD** command.)

In addition to being used to maximize tape efficiency, the cache buffer is particularly important in a multiple-Initiator environment where the SCSI disconnect/reconnect function may be used as described above. This frees the SCSI bus for the use of other Initiators when the MT02 is either emptying the cache (write mode) or filling the cache (read mode).

5.3.3 End-of-Media Processing

The MT02 Controller keeps track of tape position and tape length. When the MT02 first writes to the tape, it erases all tracks by placing a "No Data" signal on the media. This "No Data" signal is detected during read operations and can cause an end-of-media indication. For instance, if only 1 block is written on the tape, an attempt to read more than 1 block causes the MT02 to send a CHECK CONDITION completion status message to the Initiator and to set the BLANK CHECK sense key in the Extended Sense Byte (see subsection 8.3.14.4).

During a write operation, for all tracks except the last track, the MT02 writes data between the Load Point (LP) hole and the Early Warning (EW) hole, as shown in Figure 5-2. On the last track, the MT02 writes data up to a point (called the Pseudo EOM point) approximately 300 blocks before the absolute EW hole.

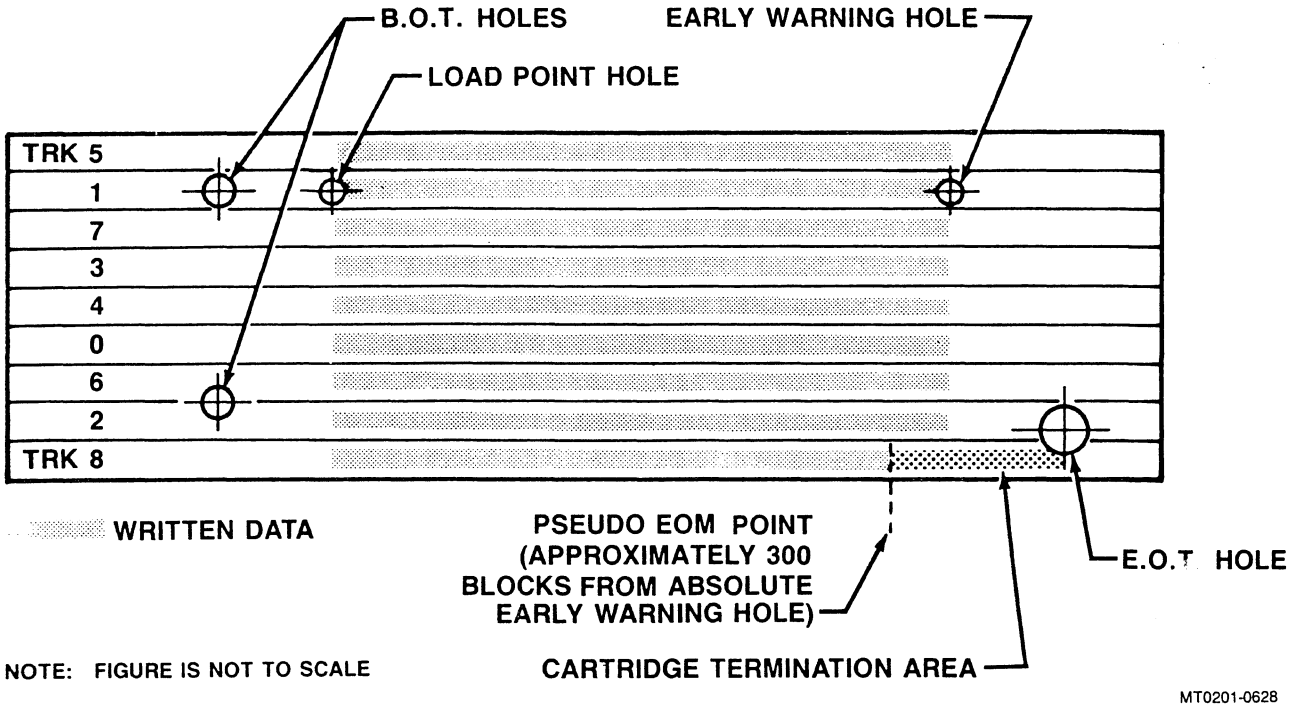


Figure 5-2. Write End-of-Media Point

When the MT02 encounters this point, it issues a CHECK CONDITION status code and returns an Early Warning EOM condition to the Initiator. It also returns a NO SENSE (00) send key, INSUFFICIENT CAPACITY (0A) Error Class/Code, and the number of blocks not transferred from the Initiator into the Sense Information Bytes in the Extended Sense format. Any buffered data will be flushed from the cache and written onto tape, unless an error prevented further writing onto the tape.

The pseudo EOM notification to the Initiator is issued only once; it is the responsibility of the Initiator to recognize that space available on the tape is limited.

When it receives the SCSI Write command, the MT02 uses the following calculation to determine the available block space:

(tp_cap) minus (tp_use) minus (300) = tp_spc

where

tp_cap = total tape block capacity of 450 or 600 foot tape. (This value is known for block 0, then recalculated after each track is completely filled.)

tp_use = total amount of blocks written to tape. (This value is all blocks, retried blocks and gaps.)

tp_spc = remainder of available tape block space to pseudo EOM.

Once tp_spc (the pseudo EOM point) is calculated, the MT02 determines if the SCSI Write command can transfer the total number of requested blocks. It then either processes the complete number of blocks requested or processes some of the requested blocks and terminates the command with a pseudo EOM CHECK CONDITION status. The tp_spc value is calculated on initial receipt of the SCSI Write commmand and is not calculated again until the next SCSI Write command. At this time, the Initiator may issue a **RECOVER BUFFERED DATA** command (see subsection 8.3.10) to retrieve the data remaining in the cache. Once a **RECOVER BUFFERED DATA** command has been issued, ALL data remaining in the cache must be recovered before another type of block transfer command is issued.

Although the MT02 has issued the pseudo EOM notification, the space remaining between it and the physical EOT hole is available to the Initiator for termination of the tape cartridge (for such things as volume labels, file marks, or other data).

If the Initiator writes data after the MT02 has issued an EOM notification, and continues to write data until the EOT is reached, the MT02 issues a CHECK CONDITION status to the Initiator. It also sets the VOLUME OVERFLOW (0D) Sense key, the INSUFFICIENT CAPACITY (0A) Error Class/Code, and the number of blocks not transferred from the Initiator plus the number of blocks remaining in the cache (if any) into the Sense Information Bytes in the Extended Sense format.

5.3.4 Physical Description of 450-foot Tape

Figure 5-3 shows the physical features of the tape, such as the relationship between tape hole locations and track positions.

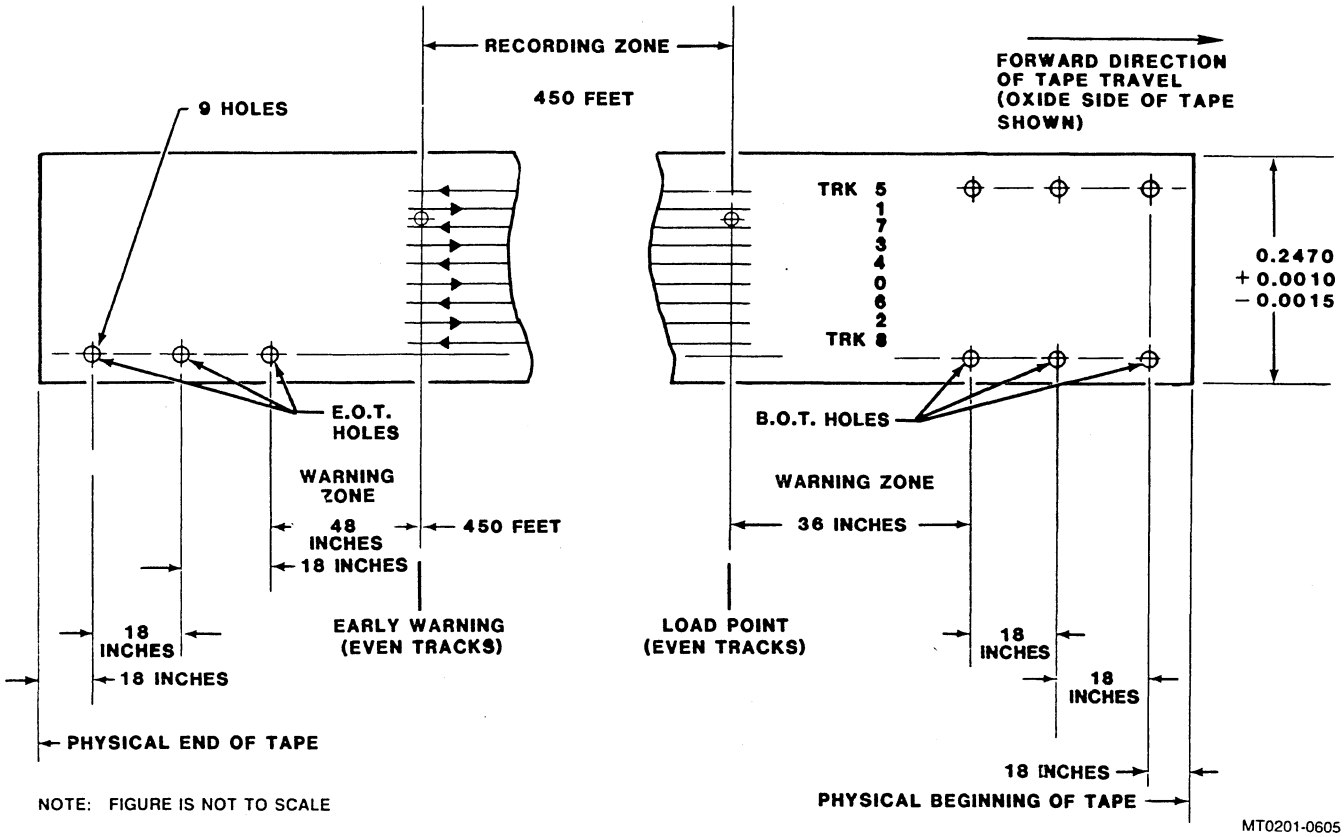


Figure 5-3. Physical Features of Cartridge Tape

5.3.5 Tape Format

The following subsections describe the QIC-24 and QIC-11 tape formats used by the MT02 Controller.

5.3.5.1 QIC-24 and QIC-11 Tape Formats

The MT02 Controller is compatible with the QIC-24 and QIC-11 standards which provide a format and recording standard for the streaming 0.25-inch wide magnetic tape cartridge. The method of recording is the NRZI, where a "one" is represented by a flux reversal (transition) in the bit cell and a "zero" is represented by the absence of a flux reversal in the bit cell. The MT02 Controller uses Group Code Recording so that encoded data has not more than two consecutive "zeros." The maximum nominal recording density (flux reversals in every bit cell) is 10,000 flux reversals per inch (FRPI). A cyclical redundancy check (CRC) consists of a two-byte code derived from information contained in the data block and block address bytes. It is recorded after these bytes for read-after-write check and read-only check.

The type of tape format (QIC-11 or QIC-24) used by the MT02 Controller is specified by the **MODE SELECT** command (see subsection 8.3.5).

5.3.5.2 Data Format

The tape data format for the QIC-24 and QIC-11 standards is described in this subsection. They are the same, except where noted. Figure 5-4 shows the data format for the QIC-24 standard.

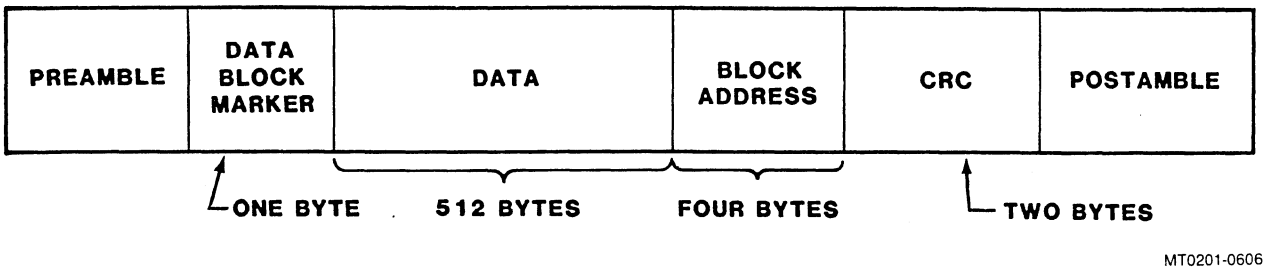


Figure 5-4. MT02 Controller QIC-24 Tape Format

Preamble

The preamble is used to synchronize the phase locked loop (PLL) in the read electronics to the data frequency. It normally contains a minimum of 120, and a maximum of 300, flux reversals.

Data Block Marker

The data block marker is a 1-byte code that identifies the start of data.

Data

The data block contains 512 bytes of either data or file marks encoded into GCR bytes.

Block Address

In the QIC-24 tape format, the block address consists of 4 bytes that uniquely identify a block recorded on tape. This field contains the track address, a control nibble, and the block address. (This address is not available to the Initiator.) In the QIC-11 tape format, the block address consists of 1 byte.

CRC

The cyclical redundancy check (CRC) consists of 2 bytes calculated from the 512 bytes of data and the 4-byte block address.

Postamble

The postamble is used as a guard band and normally consists of a minimum of five, and a maximum of 20, flux reversals.

5.3.6 Streaming Tape Operation

The relatively small physical space between write and read heads causes the tape drive to begin writing block N+1 before block N has been completely verified by a read-after-write check, as shown in Figure 5-5.

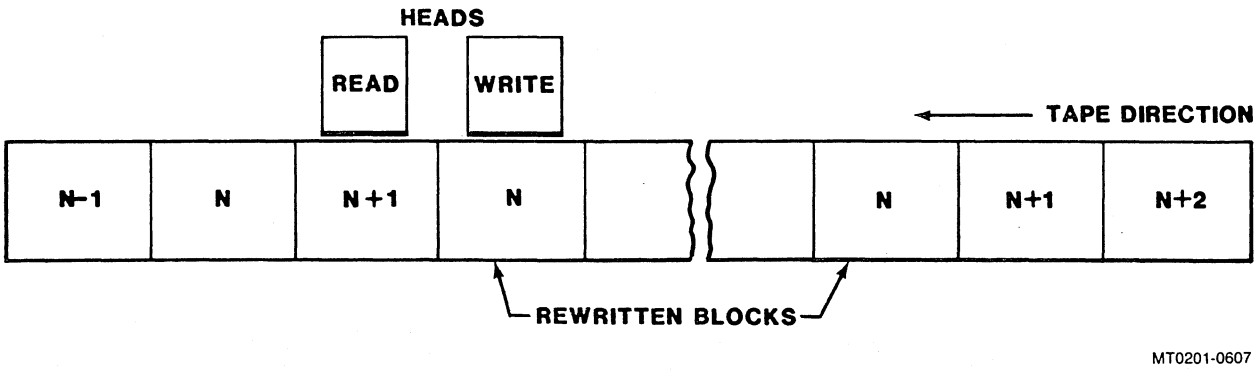


Figure 5-5. MT02 Write Operations

If block N is in error, the MT02 Controller rewrites block N after block N+1 is initially written. The MT02 Controller attempts to rewrite block N up to 16 times before the write operation is aborted. To preserve the sequential order of blocks, the MT02 Controller rewrites block N+1 after block N has been verified.

Streaming operation terminates when any one of the following conditions exists:

- Data underrun (no data received from the host adapter)
- End-of-File (may be optionally omitted, see the **WRITE FILE MARK** command in subsection 8.3.20)
- End-of-Media

The MT02 Controller causes the tape drive to perform a read-after-write check on the last data block and to rewrite the last data block, if necessary. Once the tape drive has written the last data block twice, it writes an elongated postamble with a minimum of 3500, and a maximum of 7000, flux reversals. The tape drive reverses tape motion past the last block written for approximately 60 inches. It then stops and waits for more data to write. When the MT02 is ready to resume streaming operations, it begins forward tape motion and searches for the last-written data block and its elongated postamble. At this time, it delays for a short time and then records an elongated preamble of 3500 to 7000 flux reversals. Normal recording can then resume, as shown in Figure 5-6.

If a write data underrun condition occurs, the MT02 positions the tape in the repositioned state, where it is ready for forward motion.

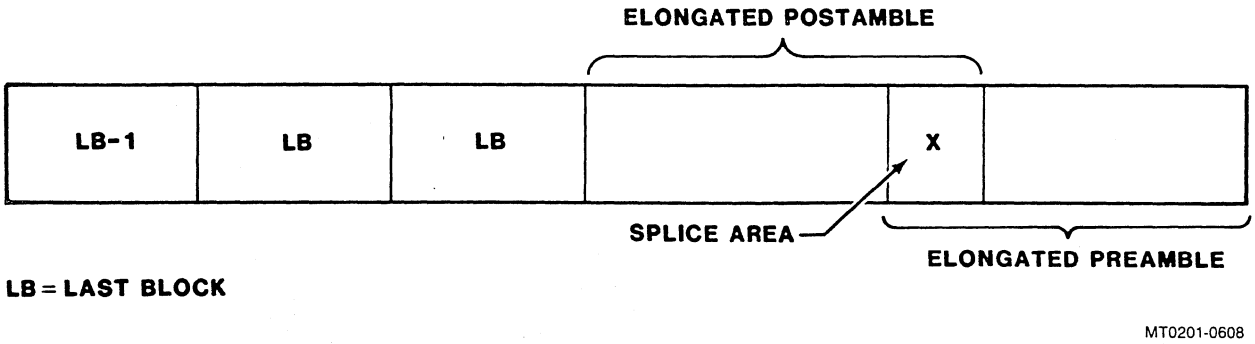


Figure 5-6. End-of-Data Write Operations

5.3.7 Hole Sensing Conditions

Figure 5-7 shows a side view of the tape cartridge. If the tape is positioned in the cartridge such that any tape holes (such as end-of-tape or Early Warning) are directly between the mirror and the sensor, the tape will not move. If this situation occurs, move the tape in the reverse direction by placing your thumb on the wheel and rotating the wheel. This action moves the tape holes so that the sensor lamp is not reflected in the mirror.

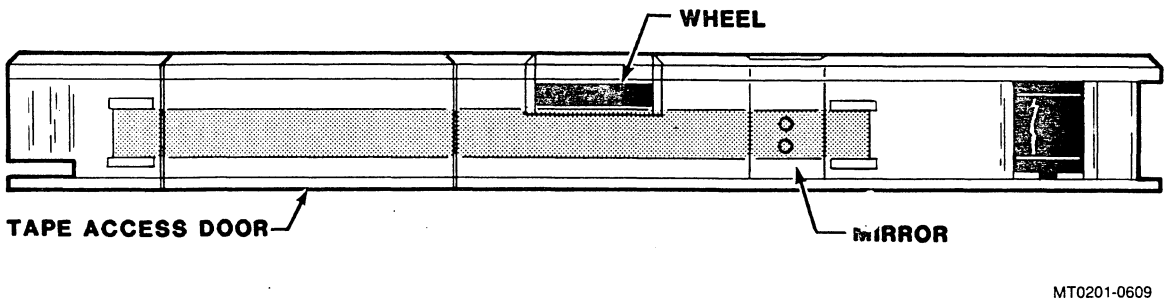


Figure 5-7. Side View of Tape Cartridge

5.3.8 Erasing the Tape

To ensure reliable recording operations, when writing on track 0, the MT02 Controller erases ahead of the area on which it is writing. Since the QIC-36 interface tape drive erase mechanism erases all tracks at once, the entire tape has been erased when track 0 has been written. Therefore, data overwrite operations (i.e., writing over an area previously written) are not supported by the MT02.

The QIC-24 tape data standard calls for 45 inches of blank tape to follow the last data recorded (the logical end-of-recorded-media). Since writing to track 0 effectively erases the whole tape, this requirement presents no special problems when the MT02 writes to tracks 1 through 8. However, during a write operation to track 0, when the operation completes, 45 inches of blank tape must be erased. A subsequent write operation to track 0 requires that the MT02 reposition the tape back those 45 inches with an associated delay in time. Therefore, the MT02 supports a disable erase ahead option that allows the Initiator to request that the MT02 erase ahead only when the last block written is a file mark or when a **REWIND** or **UNLOAD** command is received following a

write operation. Using the disable erase ahead option (which may be specified with the **MODE SELECT** command, see subsection 8.3.5) requires a controlled environment in which the user will never remove a tape cartridge without having first issued a **REWIND** or an **UNLOAD** command.

NOTE

The MT02 Controller actually erases 55 inches of tape after a write underrun on track 0.

The MT02 Controller supports an auto-load option. This option is specified with the **MODE SELECT** command. When this option is enabled and when either a cartridge tape is inserted in the tape drive or a cartridge is present during power-up or reset, the MT02 performs an auto-load procedure (the MT02 logically loads the tape as if it had received a **LOAD** command; the host does not need to issue a **LOAD** command). When this option is disabled, whenever a tape is inserted in the tape drive, the host must first issue a **LOAD** command before it attempts to access the tape. The MT02 defaults to using the auto-load option. The option may be disabled with the **MODE SELECT** command.

6.1 Overview

This section describes the interfaces used by the MT02 Controller. It includes information about how the MT02 Controller implements the SCSI bus interface electrical and mechanical requirements, and how it implements the QIC-36 interface electrical requirements. This section is divided into five subsections, as listed in the following table:

Subsection	Title
6.1	Overview
6.2	SCSI Bus Interface
6.3	User's Panel Connection
6.4	DC Power Connection
6.5	Tape Drive Interface

6.2 SCSI Bus Interface

Information about MT02 Controller implementation of SCSI bus electrical and mechanical requirements is provided in this subsection.

6.2.1 SCSI Bus Interface Physical Description

SCSI bus devices are daisy-chained with a common cable; both ends of the cable are terminated. All signals are common among all SCSI bus devices. The MT02 Controller supports the ANSI SCSI specification single-ended option for drivers and receivers. The maximum cable length allowed is 6 meters (20 feet). The length of the cable located within the FCC compliant subsystem cabinet (that contains the MT02 Controller) is included when calculating the total length of the SCSI bus. The SCSI cable that connects the compliant subsystem cabinet (that contains the MT02 Controller) to the host system must be shielded and properly grounded.

To support daisy-chain connections, SCSI devices that use shielded connectors should provide two shielded device connectors on the compliant subsystem cabinet. These two connectors may be wired one-to-one, with a stub going to the SCSI device's drivers and receivers (provided the maximum stub length specified in subsection 6.2.1.1 is not violated). Alternately, two cables may be run from two shielded connectors to the drivers and receivers so that the maximum stub length is not exceeded.

6.2.1.1 Internal Cable Requirements

If the MT02 Controller and the SCSI host adapter reside in the same compliant cabinet, you must use a 50-conductor flat-ribbon cable or a 25-twisted-pair flat cable to connect the MT02 Controller and SCSI host adapter. The maximum cumulative cable length is 6 meters. Each SCSI bus connection must have a 10-centimeter (4-inch) maximum stub length. For information on SCSI bus termination, see subsection 3.3.5.

6.2.1.2 Shielded Cable Requirements

If the MT02 Controller and SCSI host adapter do not reside in the same compliant subsystem, then a shielded SCSI cable must be used to connect the MT02 Controller and the host adapter. The connector for the SCSI bus shielded cable is a 50-pin connector that contains two rows of 25 female contacts on 100 mil centers. The connector shielding system must provide a direct current (DC) resistance of less than 10 milliohms from the cable shield at its termination point to the compliant subsystem cabinet. For information on FCC compliance, see subsection 3.5.

6.2.2 SCSI Interface Electrical Description

The MT02 Controller interfaces to SCSI host adapters and other controllers via the SCSI bus. A 50-pin male IDC connector reference designated J5 on the MT02 Controller plugs directly into the SCSI bus. Component locations for the MT02 Controller are shown in Figure 6-1. All signals use open collector drivers.

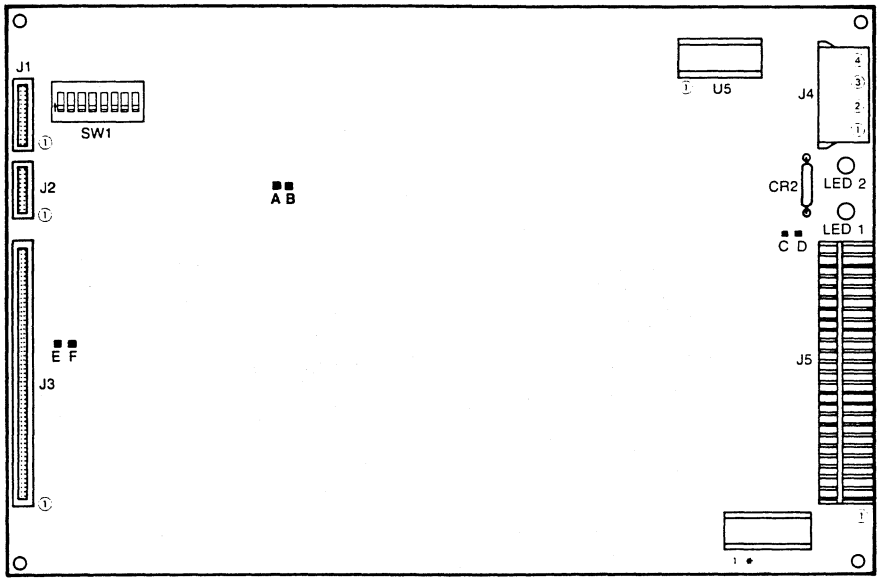


Figure 6-1. Component Locations, MT02 Controller

6.2.2.1 Output Signal Characteristics

When measured at the SCSI device's connection, each signal driven by a SCSI device has the following output characteristics:

- Signal assertion = 0.0 VDC to 0.4 VDC
- Minimum driver output capability = 48 milliamps (sinking) at 0.5 VDC
- Signal negation = 2.5 VDC to 5.25 VDC

All assigned signals are terminated with 220 ohms to +5 VDC (nominal) and 330 ohms to ground at each end of the SCSI cable as shown in Figure 6-2.

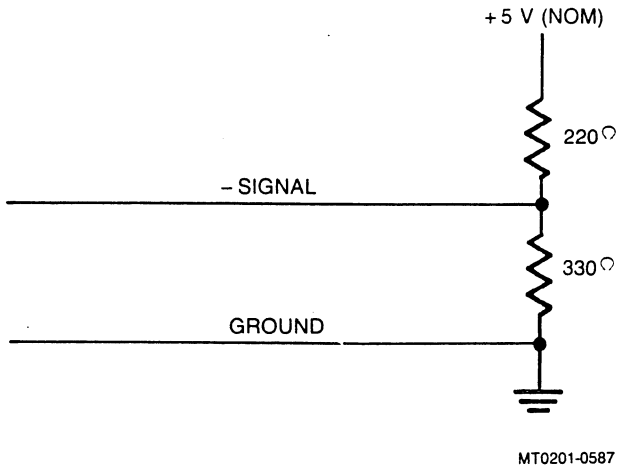


Figure 6-2. SCSI Bus Signals Termination

6.2.2.2 Input Signal Characteristics

When measured at the SCSI device's connection, each signal received by a SCSI device has the following input characteristics:

- Signal true = 0.0 VDC to 0.8 VDC
- Maximum total input load = -0.4 milliamps at 0.4 VDC
- Signal false = 2.0 VDC to 5.25 VDC
- Minimum input hysteresis = 0.2 VDC

6.2.2.3 Terminator Power (Optional)

The MT02 Controller supports the single-ended SCSI option that provides pin 26 with termination power that has the following characteristics:

V_{cc} = 4.0 VDC to 5.25 VDC (through diode)
800 milliamps maximum source drive capability

For information on implementing the SCSI Termination option, see subsection 3.3.4.

6.2.3 SCSI Bus Signals and Timing

SCSI bus activities involve one or more of the following SCSI phases of operation:

- Arbitration Phase
- Selection Phase
- Reselection Phase
- Command Phase
- Data Phase
- Status Phase
- Message Phase

These phases are described in subsection 7.3. When the SCSI bus is not involved in one of the above phases, it is in the Bus Free Phase. SCSI phase sequencing is accomplished by asserting or de-asserting the SCSI bus signals; the signals are described in subsection 6.2.3.1.

6.2.3.1 SCSI Bus Signals

There are 18 signals on the SCSI bus. Nine signals are control signals that coordinate transfer of data between SCSI bus host adapters and controllers; the other nine signals are for an eight-bit data bus with parity. The signals are listed and described in Table 6-1.

In Table 6-1, the eight data bit signals are represented by DB0 through DB7, DB7 is the most significant bit and has the highest priority during the Arbitration Phase. Bit number, significance, and priority decrease downward to DB0. The parity, represented by the DBP signal, is always odd. All host adapters and controllers on the SCSI bus generate parity. The MT02 Controller can be configured to enable its Parity Detection function (see subsection 3.3.3). During the Arbitration Phase, parity is not guaranteed to be valid.

Pin/signal assignments for the SCSI bus interface are listed in Table 6-2; they support only the SCSI single-ended option.

Table 6-1. SCSI Bus Signals

Mnemonic Name	Signal	Description
DB0	Data Bus	Data Bus Bit 0
DB1	Data Bus	Data Bus Bit 1
DB2	Data Bus	Data Bus Bit 2
DB3	Data Bus	Data Bus Bit 3
DB4	Data Bus	Data Bus Bit 4
DB5	Data Bus	Data Bus Bit 5
DB6	Data Bus	Data Bus Bit 6
DB7	Data Bus	Data Bus Bit 7
DBP	Data Bus	Data Bus Parity
ACK	Acknowledge	Indicates acknowledgment for a REQ/ACK data transfer handshake operation.
REQ	Request	Indicates a request for a REQ/ACK data transfer handshake operation.
ATN	Attention	Indicates ATTENTION condition (i.e., the Initiator has a message to send to the Target). The ATTENTION condition is described in subsection 7.6.2.
RST	Reset	Indicates RESET condition (i.e., clears the SCSI bus of all activity). The RESET condition is described in subsection 7.6.1.
SEL	Select	Used to select and/or reselect a SCSI bus device.
BSY	Busy	Indicates the SCSI bus is being used.
C/D	Control/Data	Indicates command, status, information transfer, or data in and/or data out transfer.
I/O	Input/Output	Indicates direction of data movement on the data bus with respect to an Initiator.
MSG	Message	Indicates the SCSI bus is in the Message Phase.

Table 6-2. Pin/Signal Assignments at SCSI Bus Interface

Pin	Signal Name	Input/Output
2	-D0	Input/Output
4	-D1	Input/Output
6	-D2	Input/Output
8	-D3	Input/Output
10	-D4	Input/Output
12	-D5	Input/Output
14	-D6	Input/Output
16	-D7	Input/Output
18	-DP (Data parity)	Input/Output
20	GND	--
22	GND	--
24	GND	--
26	Optional V_{cc}	--
28	GND	--
30	GND	--
32	-ATN	Input/Output
34	GND	--
36	-BSY	Input/Output
38	-ACK	Input/Output
40	-RST	Input/Output
42	-MSG	Input/Output
44	-SEL	Input/Output
46	-C/D	Input/Output
48	-REQ	Input/Output
50	-Input/Output	Input/Output
All odd pins are signal returns and are connected to signal GND at the tape drive.		

6.2.3.2 SCSI Bus Timing

Except where noted, the delay time measurements for each SCSI device (host adapter or controller) is calculated from signal conditions existing at the SCSI bus connection for that device. Normally these measurements do not consider delays in the SCSI bus cable. The SCSI timings are listed and described in Table 6-3.

The timing diagram shown in Figure 6-3, shows the typical relationship between SCSI bus signals and SCSI bus phase sequencing.

Table 6-3. SCSI Bus Timings

Timing	Duration	Description
Arbitration Delay	2.2 usec	The minimum time a SCSI bus host adapter or controller needs from the time the -BSY signal is asserted for arbitration until the MT02 Controller can examine the Data Bus to determine if arbitration has been won. There is no maximum time.
Bus Clear Delay*	800 nsec	The maximum time a SCSI bus host adapter or controller requires to stop driving all SCSI bus signals after: (1) a Bus Free Phase is detected, (2) the -SEL signal is received from another SCSI bus host adapter or controller during the Arbitration Phase.
Bus Free Delay	800 nsec	The minimum time a SCSI bus host adapter or controller waits after it has detected the Bus Free Phase until it asserts the -BSY signal when going to the Arbitration Phase.
* In the Bus Clear Delay, for condition (1) the maximum time allowed for a SCSI device to clear the SCSI bus is 1200 nsec from the time the -BSY and -SEL signals both first become false. If a SCSI device requires more than a Bus Settle Delay to detect the Bus Free Phase, it clears the SCSI bus within the time duration of a Bus Clear Delay minus the excess time.		

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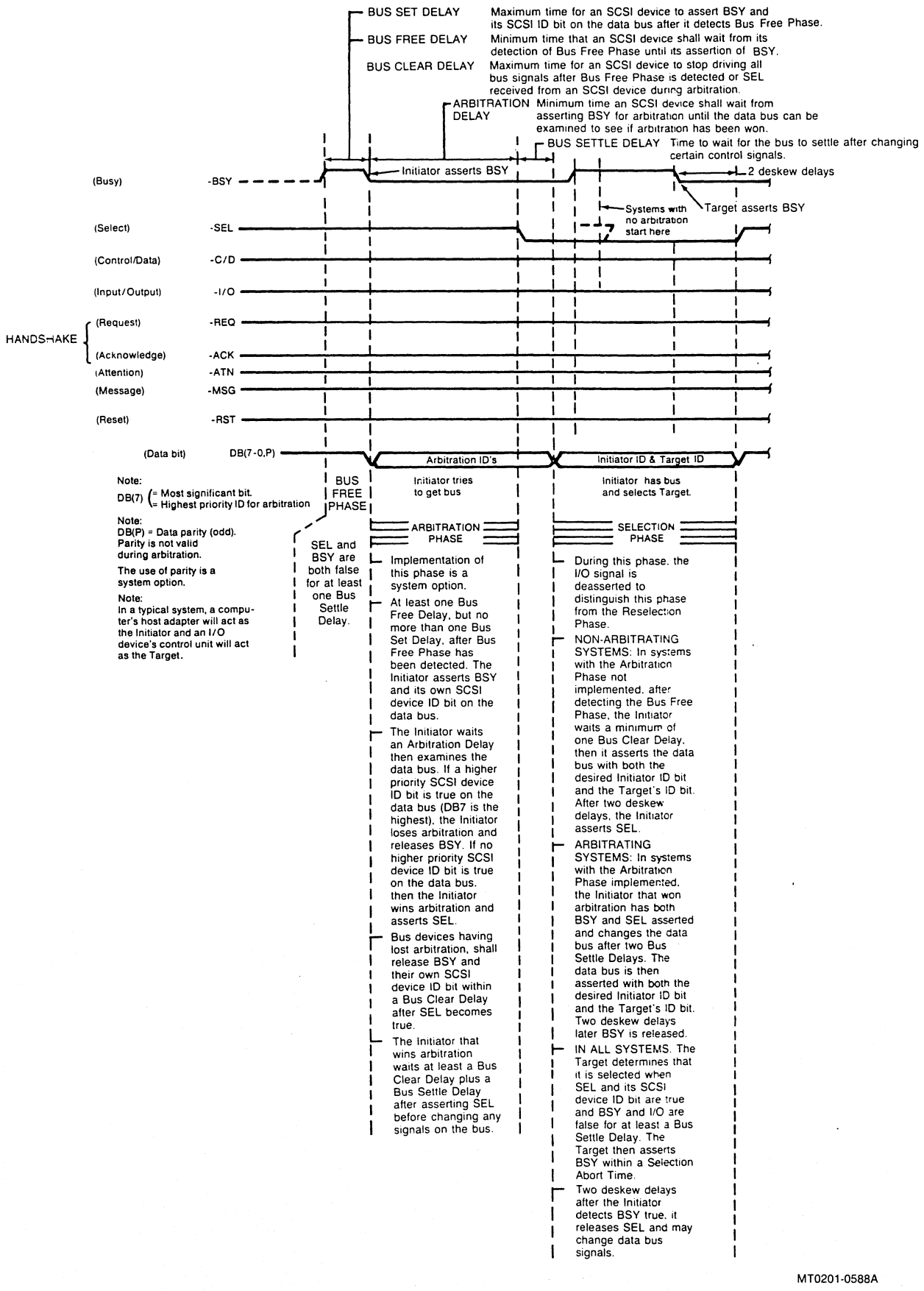

Figure 6-3. SCSI Bus Timing Diagram (Sheet 1 of 3)

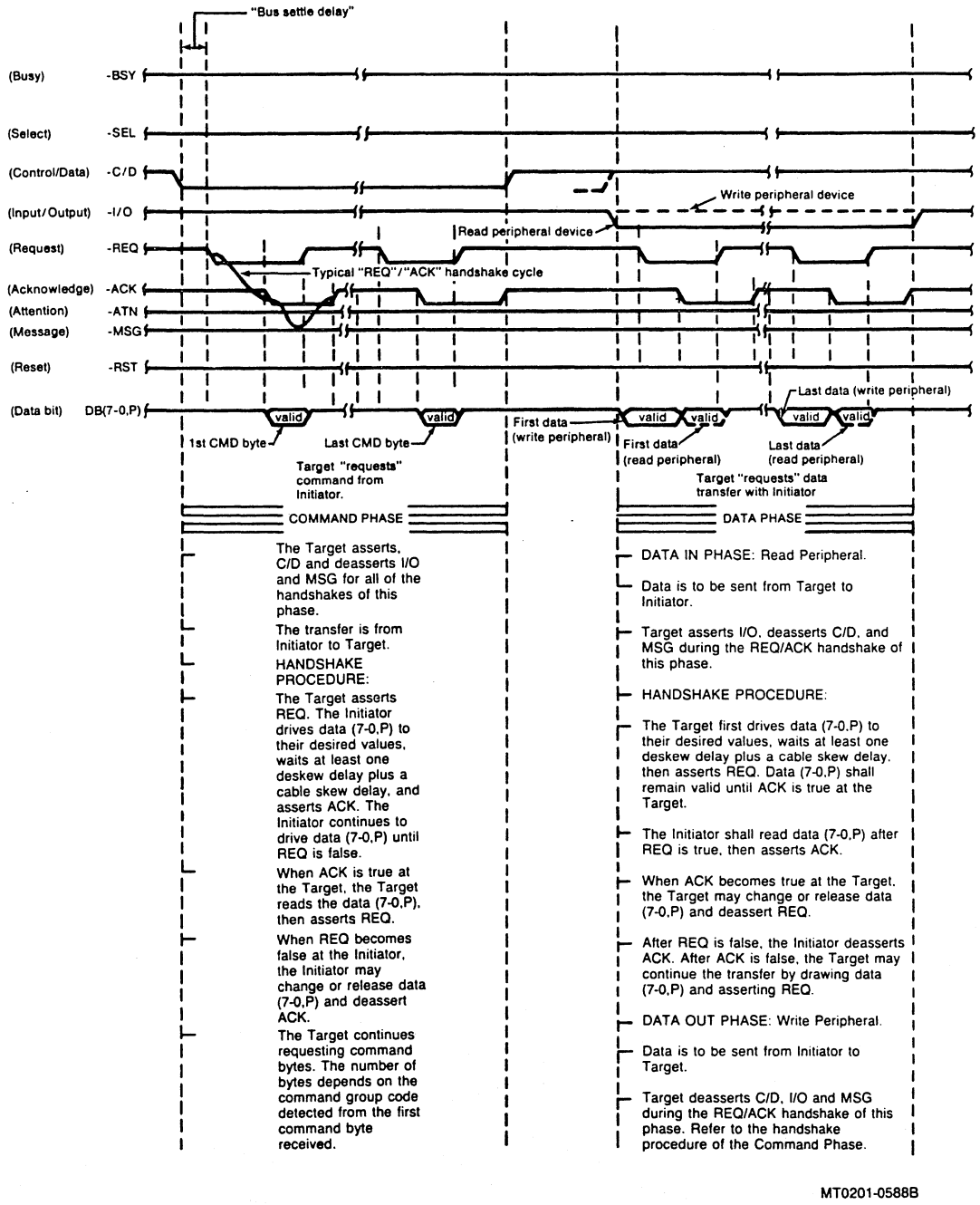

Figure 6-3. SCSI Bus Timing Diagram (Sheet 2 of 3)

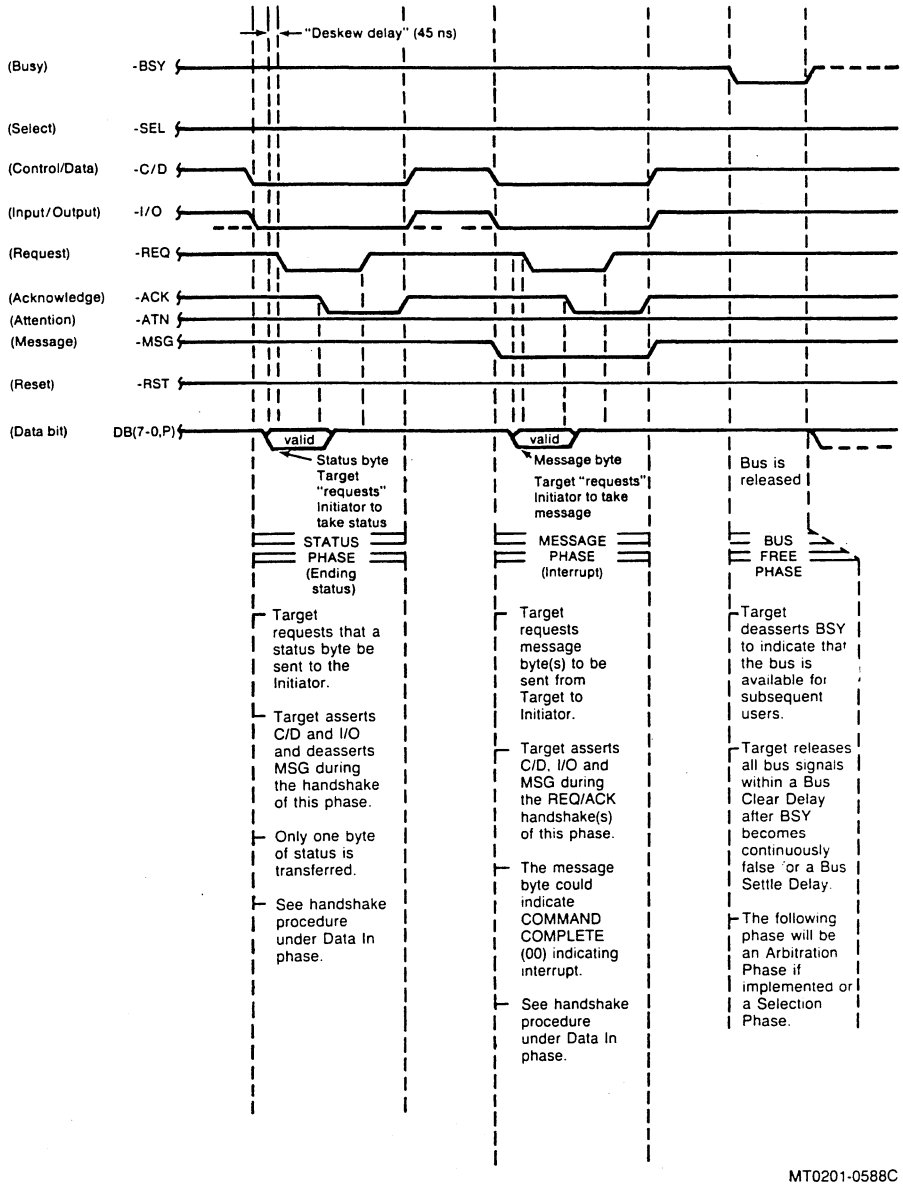

Figure 6-3. SCSI Bus Timing Diagram (Sheet 3 of 3)

6.3 User's Panel Connection

Connector J2 (see Figure 6-1), on the MT02 Controller is called the user's panel connector. It is used to connect the MT02 Controller to external LEDs. On Emulex subsystems, these external LEDs are located on the user's panel resident on the subsystem bezel. The user's panel connector is a 10-pin 3M Part Number 3446-1302. The connector pin descriptions are listed in Table 6-4.

Table 6-4. Connector J2 Pin Description

Pin	Connection	True	Function
1	Ground	--	--
2	--	--	--
3	SW1-3	High	Not Used
4	LED 4	Low	Not Used
5	SW1-2	High	Write Protect
6	LED 3	Low	Ready (LED)
7	LED 2	Low	Not Used
8	SW1-1	High	Not Used
9	LED 1	Low	Write Protect On (LED)
10	+5 VDC	--	

The MT02 Controller illuminates the Ready LED (connected to pin 6) when the tape drive is powered-up and the MT02 Controller is ready to accept commands. The MT02 Controller turns off the Ready LED when the MT02 Controller executes SCSI commands.

The MT02 Controller illuminates the Write Protect On LED (connected to pin 9) when a write operation to tape is inhibited because either of the following conditions are true:

- the user's panel Write Protect switch is set
- the Safe switch on the tape cartridge is set to Unsafe

The MT02 Controller periodically checks the status of the switches on the user's panel to detect changes in the write protect status of the tape. It updates the status of the Write Protect On LED as required. When a tape is loaded, the MT02 Controller reads the status of the Safe switch on the tape cartridge and updates the status of the Write Protect LED as required. When a tape is unloaded, or when the Write Protect switch is reset, the MT02 Controller resets the Write Protect On LED.

6.3.1 Power Fail Detect Signal

On the MT02 Controller that has Assembly Number MT0210403, pin 2 on connector J2 is an optional power fail detect signal. This signal allows the MT02 to detect failing DC power. When the signal is asserted (active low), a latch is set. When the MT02 microprocessor senses the latch, it inhibits disk drive activity. The signal must be asserted at least 2 milliseconds before the +5 VDC power falls below +4.75 VDC.

To use this power fail detect option, the power supply used in the subsystem in which the MT02 resides must contain a power fail signal. Connect pin 2 to the power fail signal in the power supply.

6.4 DC Power Connection

The MT02 Controller power connector, reference designated J4 (see Figure 6-1), is an AMP P/N 641737-1. Table 6-5 lists the power connections for this connector. The pin locations for this connector are shown in Figure 6-4.

Table 6-5. Power Supply Connections at Connector J4

Pin	Description
1	+12 VDC, ± 5%, 40 milliamps nominal
2	Ground
3	Ground
4	+5 VDC, ± 5%, 1.5 amps nominal

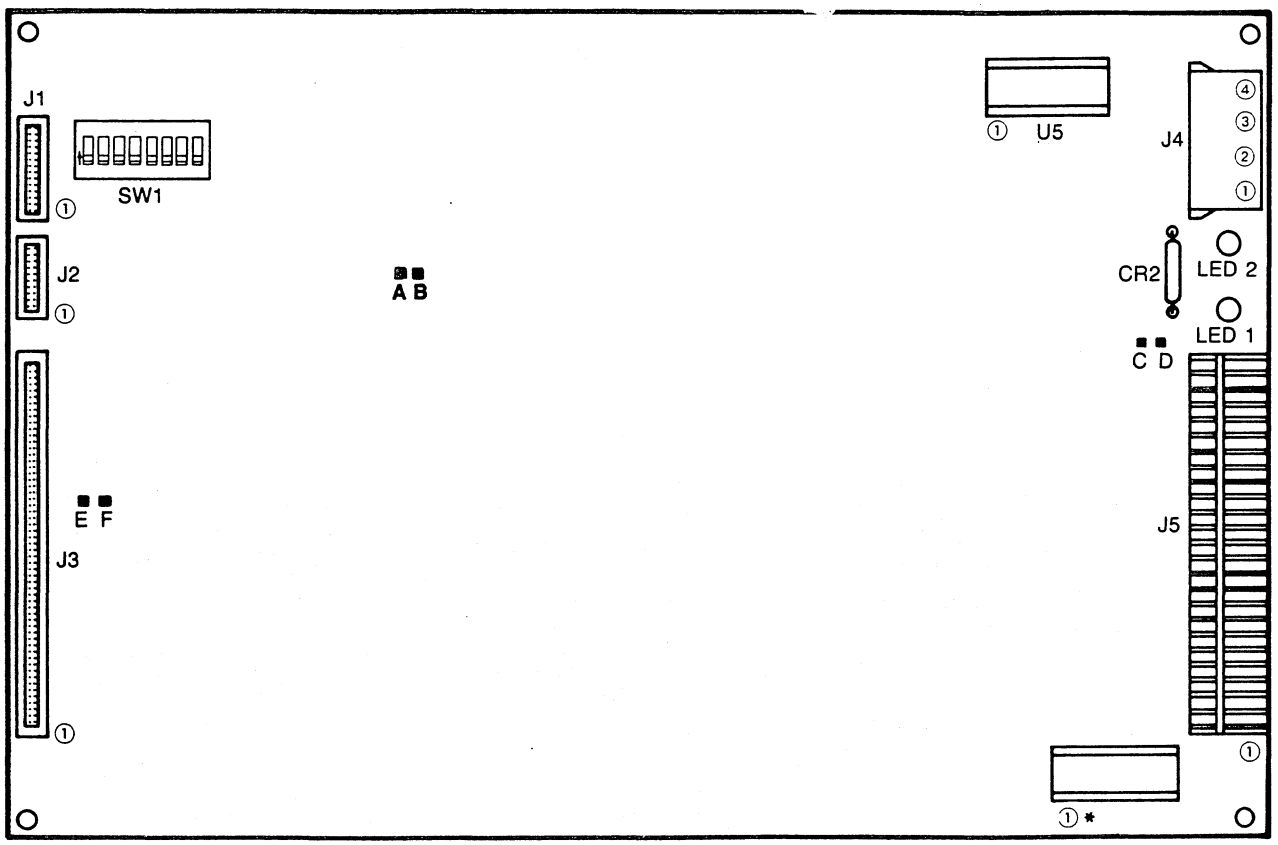

Figure 6-4. Pin Locations for Connector J4

6.5 Tape Drive Interface

The MT02 Controller interfaces with the 0.25-inch streaming cartridge tape drive via a 50-pin connector reference designated J3 on the MT02 Controller. The pin/signal assignments for this interface between the MT02 Controller and the tape drive are listed and described in Table 6-6.

Table 6-6. Pin/Signal Assignments at Tape Drive Interface

Pin	Signal Name	In/Out	True	Description
2	-GO	In	Low	Go Control for Capstan Servo
4	-REV	In	Low	Direction Control for Capstan Servo
6	-TR3	In	Low	Track Select Bit 3
8	-TR2	In	Low	Track Select Bit 2
10	-TR1	In	Low	Track Select Bit 1
12	-TR0	In	Low	Track Select Bit 0
14	-RST	In	Low	Reset Drive
16	NUS	-	-	Not Used
18	NUS	-	-	Not Used
20	NUS	-	-	Not Used
22	-DS0	In	Low	Drive 0 Select Control
24	-HC	In	Low	Select operation with alternate type of tape
26	-RDP	Out	Low	Read Data Pulse Output - one pulse per flux transition
28	-UTH	Out	Low	Upper Tape Position Code

(continued on next page)

Table 6-6. Pin/Signal Assignments at Tape Drive Interface (continued)

Pin	Signal Name	In/Out	True	Description
32	-SLD	Out	Low	Response from drive when selected
34	-CIN	Out	Low	Cartridge in Place
36	-USF	Out	Low	Unsafe: Cartridge Safe Plug in UNSAFE Position
38	-TCH	Out	Low	Capstan Tachometer Pulses
40	-WDA	In	Low	Inverse Write Data Signal
42	WDA	In	High	Inverse Write Data Signal
44	-THD	In	Low	Threshold - invokes a percentage qualifying amplitude for the read signal off the tape
46	-HSD	In	Low	High Speed - selects tape speed of 90 inches-per-second
48	-WEN	In	Low	Write Enable Control
50	-EEN	In	Low	Erase Enable Control
All odd pins are signal returns and are connected to signal GND at the tape drive.				

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SECTION 7
SCSI PROTOCOL DESCRIPTION

7.1 Overview

This section describes the SCSI bus protocol. It includes information on SCSI bus phases and phase sequencing and procedures for passing control and status information between SCSI bus host adapters and controllers by using SCSI memory address pointers. This section is divided into six subsections, as listed in the following table:

Subsection	Title
7.1	Overview
7.2	SCSI Bus Description
7.3	SCSI Bus Phases
7.4	SCSI Bus Phase Sequencing
7.5	SCSI Memory Address Pointers
7.6	SCSI Bus Conditions

7.2 SCSI Bus Interface

The Small Computer System Interface (SCSI) is a standard interface established to support mass storage, printer output, and network communication for microcomputers and minicomputers. The interface is an eight-port, daisy-chained bus. The SCSI command standard for the MT02 is based on the ANSI X3T9.2/82-2 Revision 14B (06 Nov 84) SCSI Interface Specification.

The SCSI bus can support up to eight SCSI host adapters and/or controllers. Each controller can be connected to a maximum of eight devices (called Logical Unit Numbers, or LUNs). The MT02 hardware supports any combination of host adapters, intelligent controllers, or intelligent peripherals connected to the SCSI bus. The MT02 supports one LUN: a 0.25-inch streaming cartridge tape drive that supports the QIC-36 Basic Tape Drive Interface. Three basic SCSI configurations are supported with the MT02 Controller and SCSI bus:

- Single initiator, single target
- Single initiator, multi target
- Multi initiator, multi target

Communication on the SCSI bus occurs between a host adapter and a controller. (The MT02 also supports communication between two controllers, as in a copy operation.) When a host adapter and a controller communicate, one acts as the Initiator and the other acts as the Target. The Initiator (usually the host adapter) originates an operation, and the Target (usually a peripheral controller, such as the MT02) performs the operation. Sample system configurations supported by MT02 hardware are shown in Figure 7-1.

Some SCSI bus functions are assigned to the Initiator and some functions are assigned to the Target. The Initiator can arbitrate for control of the SCSI bus and select a specific Target. The Target can request the transfer of command, data, status, or other information via the SCSI bus. In some circumstances, the Target can arbitrate for control of the SCSI bus to reselect an Initiator and continue an operation. Sometimes, the Target becomes an Initiator and arbitrates for control of the SCSI bus (for example, when it performs a copy operation).

SCSI bus data transfer operations are asynchronous and follow a defined request/acknowledge (REQ/ACK) handshake protocol. (This protocol is defined in the ANSI SCSI specification.) One eight-bit byte of information can be transferred with each handshake.

The SCSI bus consists of 18 signal lines. Nine signal lines are for an eight-bit data bus with parity; the other nine signal lines are for control and status signals that coordinate data transfer operations between the host adapter and SCSI controllers. SCSI bus signals are described in detail in subsection 6.2.3.1.

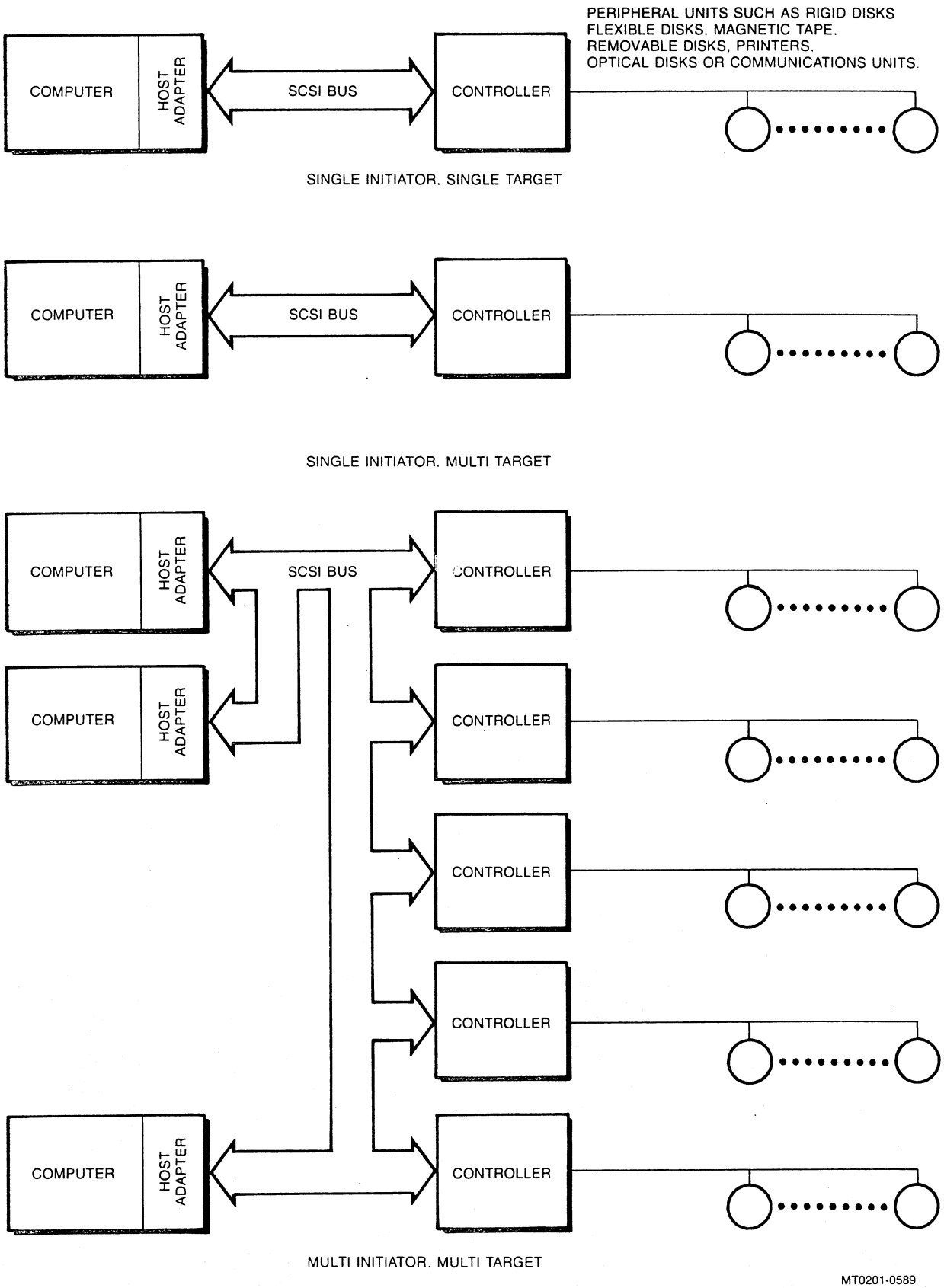

Figure 7-1. Sample SCSI Bus Configurations

7.3 SCSI Bus Phases

The activities on the SCSI bus can be divided into the following phases of operation:

- Arbitration
- Selection
- Reselection
- Information Transfer
  - Command
  - Data
  - Status
  - Message

These phases are supported as specified by the ANSI SCSI specification (listed in subsection 1.1.1). The phases are individually discussed in subsequent subsections. The last four phases (Command, Data, Status, and Message) are grouped together as Information Transfer Phases.

When the SCSI bus is not involved in one of the SCSI bus phases, it is in a Bus Free Phase. The Bus Free Phase indicates that no host adapter or controller is actively using the SCSI bus and the SCSI bus is available for subsequent users.

The SCSI bus activities, implemented by the MT02, include the disconnect function and reselection function. Overlapped operations on multiple controllers and multiple logical units are supported.

In the following subsections, no attempt is made to detail the SCSI bus signal sequences; the signals are listed in subsection 6.2.3.1. If detailed signal sequence information is required, refer to the ANSI SCSI standard.

7.3.1 Arbitration Phase

The Arbitration Phase is an optional implementation on the SCSI bus. This phase is used when multiple controllers or processors vie for SCSI bus ownership. Since multiple hosts adapters and/or controllers may desire control of the SCSI bus concurrently, arbitration for the SCSI bus is a requirement for the MT02 Controller.

7.3.2 Selection and Reselection Phases

The SCSI bus Selection and Reselection phases provide methods for establishing a link between the Initiator and a desired Target.

Usually the MT02 is selected by an Initiator to perform some function (e.g., read or write data). The MT02 then has the option of disconnecting from the SCSI bus. When the MT02 needs to re-establish the link to its original Initiator, it reselects that Initiator.

For the copy function, however, the MT02 can behave as an Initiator and select another controller as a Target source or destination for the copy operation. While in the Initiator mode, the MT02 always issues an IDENTIFY message (see subsection 7.3.3.4) after selecting a Target.

The SCSI Selection and Reselection Phases can be terminated for any one of three conditions:

1. The preceding Selection or Reselection Phase is successfully completed by using the Selection/Reselection handshake protocol.

2. A Selection/Reselection timeout occurs. The timeout results if any Target or Initiator does not respond to the Selection/Reselection Phase within a timeout period of 2 seconds.

3. A Reset (-RST) signal occurs on the SCSI bus. When this signal is asserted, all SCSI bus sequences are immediately terminated and the SCSI bus signals are released by all Initiators and Targets.

The Initiator can use the Attention (-ATN) signal to notify the MT02 that a message from the Initiator is ready. To guarantee that the Target recognizes the Attention condition before the Command Phase is entered, the -ATN signal level must be true before the Selection or Reselection Phase is completed.

If an IDENTIFY message is used during the Selection Phase sequence, the specified LUN has precedence over the LUN field in the Command Descriptor Block. (Command Descriptor Blocks are described in detail in Section 8.)

NOTE

If the Initiator selects a nonexistent LUN, a vendor unique status of nonexistent device (NED bit) is returned in the Status Byte (see subsection 7.3.3.3.1). Selected LUNs that have not been initialized by the MT02 report a BUSY status code (e.g., at startup, or when they are not connected to the MT02).

7.3.3 Information Transfer Phases

The Command, Data, Status, and Message Phases are grouped together as Information Transfer Phases because they are all used to transfer data or control information via the SCSI data bus. The Information Transfer Phases are described in the following subsections.

7.3.3.1 Command Phase

The Command Phase allows the Target to request command information from the Initiator. An Initiator issues SCSI commands to a Target by transferring a command packet, called a Command Descriptor Block (CDB). The length of the SCSI command and the meaning of the information in the command packet depends on which command is being transferred. (See Section 8 for definitions of SCSI commands and all SCSI CDBs supported by the MT02.)

The last byte of every command packet (see Figure 8-1) is a control byte and can be differentiated into the following bit groups:

- The low-order two bits control the ability to link commands in a sequence and to notify the host adapter when a particular command (CDB) step is completed. These two bits are designated Flag and Link in the descriptions of MT02 command packets in Section 8.

- The remaining bits in the control byte are either reserved bits (they are zero) or they are command-dependent bits.

The remainder of the bytes of the command packet are primarily command-dependent.

The Command Phase is interrupted only for the following exception conditions:

- **Reset Condition.** This condition can occur when the SCSI Reset (-RST) signal is asserted or a power fail or power-off condition in the Target occurs. In this case, the Command Phase and the connection established during the Selection/Reselection Phase are terminated by the Target with the release of the -BSY signal.

- **Parity Error Condition.** The Target detects a parity error on the SCSI bus during the command transfer operation. At this time, the MT02 Controller releases the -BSY signal, terminates the connection, and the SCSI bus returns to the Bus Free phase.

7.3.3.2 Data Phase

The Data Phase of a connection controls the transfer of data between the Initiator and Target devices. The Data Phase includes both the Data In Phase and the Data Out Phase. The Data In Phase allows the Target to request sending of data to the Initiator from the Target. The Data Out Phase allows the Target to request sending of data to the Target from the Initiator. The direction of the data transfer operation depends on the command being processed. Some commands may have no data to be transferred and therefore have a null Data Phase. Only the asynchronous data transfer mode is supported by the MT02.

The Data Phase is interrupted only for the following exception conditions:

- **Reset Condition.** This condition can occur when the SCSI Reset (-RST) signal is asserted or when a power fail or power-off condition in the Target occurs. In this condition, the Data Phase and the connection established during the Selection/Reselection Phase are terminated by the Target with the release of the -BSY signal.

- **Data Out Parity Error Condition.** The Target detects a parity error on the SCSI bus during the data transfer operation from the Initiator to the Target.

- **Data In Parity Error Condition.** The Initiator detects a parity error on the SCSI bus during the data transfer operation from the Target to the Initiator. The Initiator can then assert the -ATN signal along with the Acknowledge (-ACK) signal. The Target detects this condition and enters the message out phase to receive a message. The Initiator sends an Initiator-detected error message in response.

7.3.3.3 Status Phase

The Status Phase is used by the Target to send completion information to the Initiator. The status is sent in a single byte, the format of which is defined in subsection 7.3.3.3.1.

The Target can initiate the Status Phase when any one of the following conditions occurs:

- **Busy Status.** The Selection Phase is completed and the Target is in a BUSY state and unable to process any commands for an extended period of time. The Target can initiate the Status Phase immediately after this condition occurs. The Status Byte transferred has the BUSY status code set.

- **Reservation Conflict Status.** The Command or Reselection Phase is completed and the specified LUN is reserved for another Initiator. The Status Byte transferred has the RESERVATION CONFLICT status code set.

- **Terminated Status.** At the termination of a command, the Status Byte transferred has the GOOD STATUS code set to indicate the success of the command.

NOTE

In multi-Initiator environments, the Initiator delays a minimum of 200 microseconds before attempting another selection of a Target if a BUSY status code for that Target is received.

7.3.3.4 Status Byte Format

The format of the Status Byte used by the Target to send completion information to the Initiator is defined below.

Byte	Bit	07	06	05	04	03	02	01	00
0		0	0	0	Status Code				NED

Status Code - Bits <04:01>

These bits are used to specify the status code. Table 7-1 lists and describes the status codes.

Nonexistent Device (NED) - Bit 00

When the NED bit is set to 1, the Initiator selected a LUN that is not configured in the system.

Table 7-1. Status Codes

Bits 04	03	02	01	Status	Description
X	0	0	0	GOOD STATUS	The MT02 successfully completed the command.
0	0	0	1	CHECK CONDITION	An error, exception, or abnormal condition occurred.
0	1	0	0	BUSY	The MT02 is busy.
1	0	X	0	INTERMEDIATE STATUS	Sent for every command in a series of linked commands (see subsection 7.3.3.1) unless a CHECK CONDITION or RESERVATION CONFLICT status code is detected.
1	1	0	0	RESERVATION CONFLICT	Sent to an Initiator that attempts to access a LUN connected to the MT02 when another Initiator has reserved the LUN.
1 = Set		0 = Cleared		X = Don't Care	

7.3.3.5 Message Phase

The Message Phase is used to transfer information about exception conditions between the Initiator and the Target. The Message Phase includes both the Message In and the Message Out Phases. The Message In Phase allows a Target to request that messages be sent from the Target to the Initiator. The Message Out Phase allows a Target to request that messages be sent from the Initiator to the Target. Messages from the MT02 are a single byte in length. The messages and their corresponding hexadecimal codes are listed and described in Table 7-2.

Table 7-2. MT02 Controller SCSI Messages

Code	Message	Description
00	COMMAND COMPLETE	Issued by the Target just before releasing the -BSY signal at the end of a command execution. This message generally is sent immediately after a Status Phase.
02	SAVE DATA POINTER	Issued by the Target to direct the Initiator to save a copy of the present active data pointer. This message is issued just before the MT02 Controller issues the DISCONNECT message and disconnects from the bus.
04	DISCONNECT	Issued by the Target just before releasing the -BSY signal to indicate to the Initiator that the present physical connection is temporarily broken. The current data, command, and status pointers are not saved.
05	INITIATOR DETECTED ERROR	Issued by an Initiator to inform the Target that an error has occurred during a read operation.
06	ABORT	Issued by the Initiator to the Target to clear the specified LUN and cause the SCSI bus to go to the Bus Free Phase.
07	MESSAGE REJECT	Issued by the Initiator or Target in response to a received message that was undefined.
08	NO OPERATION	A null message issued by the Initiator if the Target requests a message from the Initiator but the Initiator has no message to convey.
09	MESSAGE PARITY ERROR	Issued by the Initiator to inform the MT02 Controller that a parity error has occurred on a message receive operation from the Target to the Initiator. The MT02 Controller attempts to send the message one more time.

(continued on next page)

Table 7-2. MT02 Controller SCSI Messages (continued)

Code	Message	Description
0A	LINKED COMMAND COMPLETE	Issued by the Target to the Initiator to indicate the completion of a linked command (see subsection 7.3.3.1).
0B	LINKED COMMAND COMPLETE WITH FLAG	Issued by the Target to the Initiator to indicate the completion of a linked command that had the Flag bit set.
0C	BUS DEVICE RESET	Issued by the Initiator to the Target to reset all current I/O activities on the SCSI bus MT02 Controller. This message generates a hard Reset Condition (see subsection 7.6.1).
80-FF	IDENTIFY *	Issued by the Target or Initiator to establish a connection to a particular LUN. The following bits have particular meaning: Bit 07 - Always set to 1. Bit 06 - Set if the Initiator can support Disconnect and Reconnect sequences. Bits <02:00> - Specify LUN address (hexadecimal) in a Target.
If the disconnect function is supported, this message is issued to the MT02 Controller at the beginning of every command sequence.		

7.4 SCSI Bus Phase Sequencing

The status of the SCSI bus is a function of the control signals. (The control signals are described in subsection 6.2.3.) These signals place the SCSI bus in one of four phases: Arbitration, Selection/Reselection, Information Transfer, or Bus Free. The order in which SCSI bus phases are used follows the prescribed sequence shown in Figure 7-2.

All SCSI command sequences start with the Bus Free Phase. The normal progression is from the Bus Free Phase to the Arbitration Phase. During arbitration, host adapters or controllers contest for control of the SCSI bus. Priority is given to the contestant that has the highest SCSI bus address.

Once a host adapter or controller has control (i.e., is the bus master) of the SCSI bus, the SCSI bus enters the Selection/Reselection Phase. This phase allows the bus master to select a specific device for communication. An Initiator can select a Target to initiate an operation, or a Target can reselect an Initiator to continue an operation.

After a physical path between an Initiator and a Target is established, the SCSI bus enters one of the Information Transfer Phases. These phases include six types of information exchange:

- Command Phase
- Data Out Phase
- Data In Phase
- Status Phase
- Message In Phase
- Message Out Phase

These types of SCSI bus information exchange are described in more detail in subsection 7.3.

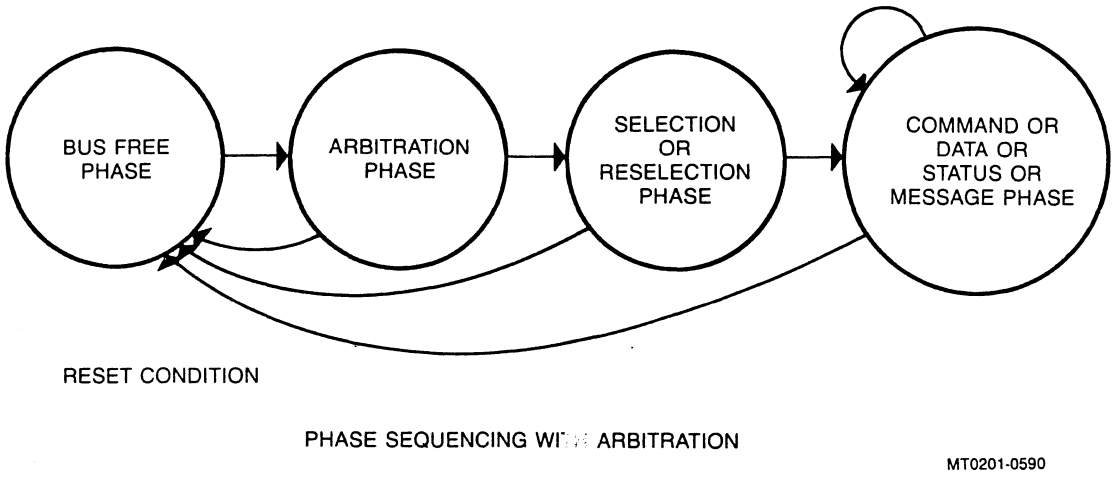

Figure 7-2. SCSI Bus Phase Sequences

7.5 SCSI Memory Address Pointers

There are three "conceptual" memory address pointers, located in host adapter memory, that point to the next byte of command, data, or status information to be accessed. The pointers are used to represent the state of the interface. After the pointers are initially loaded by the Initiator, their movement is under control of the Target. When the Target transfers a byte of information to or from one of the three pointers, the position of that pointer is incremented.

The SCSI command set is independent of the types of host adapters and peripheral device controllers (tape drives or disk drives) attached to the SCSI bus. The SCSI command set masks the internal structure of the device (cylinders, tracks, sectors, data blocks, etc.) from the SCSI bus. The SCSI command set supported by the MT02 Controller is defined in Section 8. The host memory contains three I/O blocks: command, data, and status. During SCSI bus I/O operations, the MT02 Controller initially reads a command block located in host memory to determine the I/O task to be performed. The MT02 Controller then reads from, or writes to, a host memory data block as an I/O task proceeds. At the end of an I/O operation, the MT02 Controller writes to a status block (in host memory).

There are two sets of three pointers within the host adapter. The first set, the Current Pointer Values, addresses the next command, status, or data byte to be transferred to the MT02 Controller. The second set, the Saved Pointer Values, always addresses the start of the command and status block, but increments for the data block.

During a disconnect operation, the MT02 Controller enters the Message Phase and issues a SAVE DATA POINTER message to the Initiator.

7.6 SCSI Bus Conditions

The SCSI bus has the following asynchronous conditions:

- Reset condition
- Attention condition
- Unit Attention condition

These conditions cause certain SCSI device actions and can alter the phase sequence. The two conditions are described in the following subsections.

7.6.1 Reset

The Reset condition is used to clear all bus masters immediately from the SCSI bus. This condition takes precedence over all other SCSI bus phases and conditions. During the reset condition, no SCSI bus signal except -RST is guaranteed to be valid.

The MT02 supports the SCSI hard reset option. It does not support the SCSI soft reset option. When it detects a reset condition, the MT02 performs the following actions:

- Clears all uncompleted commands
- Releases device reservations
- Returns device operating modes (such as the **MODE SELECT** command) to their default conditions

The hard reset condition has the same effect on the MT02 as power-on; therefore, all Initiator-defined parameters must be re-submitted to the MT02.

After a reset occurs, the MT02 Controller requires at least a 1 second delay before it will accept any commands. To ensure the MT02 Controller is ready to accept commands, the first command issued should be **TEST UNIT READY**.

The MT02 Controller with Assembly Number MT0210403 includes a watchdog timer feature. If a SCSI Hard Reset Condition occurs, a latch is set. If the MT02 microprocessor cannot service the reset latch within 40 milliseconds, the timer times out and the MT02 executes a power-on reset.

7.6.2 Attention

The attention condition allows an Initiator to inform a Target that the Initiator has a message ready. The Target can obtain this message in the Message Phase.

7.6.3 Unit Attention

The Target issues a unit attention condition to inform all Initiators the operating condition of the removable media may have changed.

When the MT02 detects the unit attention condition, the tape cartridge is logically unloaded from the tape drive and the Cartridge Unsafe to Remove (LED 2, located on the MT02, see subsection 4.4) is turned off.

After a SCSI bus reset condition occurs, the first command sent by each Initiator to the MT02 causes the MT02 to send a CHECK CONDITION status code and to set the Sense Key in the Extended Sense Byte (see subsection 8.3.12.2) to UNIT ATTENTION.

When the tape cartridge is inserted, a **LOAD** command causes the tape to be positioned to the beginning-of-tape. Except for the Initiator which issued the **LOAD** command, the first command sent by all other Initiators causes the MT02 to send a CHECK CONDITION status code and to set the Sense key in the Extended Sense Byte to UNIT ATTENTION.

Before the tape cartridge is to be removed, an Initiator may issue an **UNLOAD** command to cause the tape to be considered logically nonexistent. If a tape cartridge is removed before an **UNLOAD** command is issued, all drive-accessing commands cause the MT02 to send a CHECK CONDITION status code and to set the Sense Key in the Extended Sense Byte to NOT READY. At this time, the MT02 can be in one of four states. These four states are determined by the state of the AUI bit (see the **MODE SELECT** command, subsection 8.3.5.1) and whether a subsequent **LOAD** command will be issued. If a tape cartridge is then installed, the first command sent by all Initiators causes the MT02 to send a CHECK CONDITION status code and to set the Sense key in the Extended Sense Byte to the key that corresponds to the current MT02 state. Table 7-3 lists the four MT02 states and the corresponding Sense key issued by the MT02 at the time a cartridge is installed.

Table 7-3. MT02 Controller States That Occur When a Cartridge Is Removed, Then Installed and No **UNLOAD** Command Has Been Issued

MT02 Controller State		Corresponding Request Sense Key
Auto Load Inhibit (AUI) Bit	**LOAD** command is next command issued	
0	0	UNIT ATTENTION (06) on next command
0	1	UNIT ATTENTION (06) on **LOAD** command
1	0	NOT READY (02)
1	1	UNIT ATTENTION (06) on **LOAD** command
0 = Not Set	1 = Set	

8.1 Overview

This section describes the SCSI commands supported by the MT02 Controller. It is divided into four subsections, as listed in the following table:

Subsection	Title
8.1	Overview
8.2	SCSI Command Descriptor Block Structure
8.3	SCSI Group Code 0 Command Descriptions
8.4	SCSI Group Code 6 Command Descriptions

8.2 SCSI Command Descriptor Block Structure

An Initiator issues SCSI commands to a Target device by transferring a command packet, called a Command Descriptor Block (CDB). The command contained in the CDB determines the length of the CDB. The first byte of a CDB contains the command. This byte is called the Operation Code. It has two components: the Group Code and the Command Code.

Only SCSI Group Code 0 and Group Code 6 commands are acceptable to the MT02 Controller; thus, all CDBs supported by the MT02 Controller contain 6 bytes. The Command Code specifies the type of SCSI command. SCSI command types are defined as specific CDB bit patterns in the ANSI SCSI specification. CDBs supported by the MT02 Controller follow the guidelines listed in the ANSI SCSI specification.

The structure of each SCSI Group Code 0 command packet that can be accepted by the MT02 Controller is shown in the individual command packet descriptions in subsection 8.3. The structure of each SCSI Group Code 6 command packet that can be accepted by the MT02 Controller is shown in the individual command packet descriptions in subsection 8.4.

The following table lists, by subsection number, the SCSI command names and operation codes supported by the MT02 Controller.

Subsection	MT02 Controller SCSI Command	Code
8.3.1	**COPY**	18
8.3.2	**ERASE**	19
8.3.3	**INQUIRY**	12
8.3.4	**LOAD/UNLOAD**	1B
8.3.5	**MODE SELECT**	15
8.3.6	**MODE SENSE**	1A
8.3.7	**PREVENT/ALLOW MEDIUM REMOVAL**	1E
8.3.8	**READ**	08
8.3.9	**READ BLOCK LIMITS**	05
8.3.10	**RECOVER BUFFERED DATA**	14
8.3.11	**RELEASE UNIT**	17
8.3.12	**REQUEST SENSE**	03
8.3.13	**RESERVE UNIT**	16
8.3.14	**REWIND**	01
8.3.15	**SEND DIAGNOSTIC**	1D
8.3.16	**SPACE**	11
8.3.17	**TEST UNIT READY**	00
8.3.18	**VERIFY**	13
8.3.19	**WRITE**	0A
8.3.20	**WRITE FILE MARK**	10
8.4.1	**READ REVISION LEVEL**	C1

Certain commands are not permitted if the tape cartridge is not loaded. Loaded means a tape cartridge is physically installed in the tape drive and either the **LOAD** command has been issued by an Initiator or the MT02 auto-load option (see subsection 8.3.5.1) is being used. If the tape cartridge is unloaded, the MT02 Controller rejects all commands, except those listed in the following table:

Command Code	Command Name
12	**INQUIRY**
15	**MODE SELECT**
1A	**MODE SENSE**
05	**READ BLOCK LIMITS**
14	**RECOVER BUFFERED DATA**
03	**REQUEST SENSE**
1D	**SEND DIAGNOSTIC**
00	**TEST UNIT READY**
C1	**READ REVISION LEVEL**

8.3 SCSI Group Code 0 Command Descriptions

This subsection provides detailed descriptions of the SCSI Group Code 0 commands, including CDB formats, hexadecimal operation codes, byte and bit functions, and any effects produced by the commands. Each SCSI command is described in a separate subsection.

A sample Group Code 0 CDB is shown in Figure 8-1. The first byte of a command (Byte 00) contains two fields: the Group Code in the high order three bits (bits <07:05>), and the Operation Code in the low order five bits (bits <04:00>). The Group Code determines the length of the command packet in the CDB, and together the Group and Operation Codes determine the operation to be performed. Remember, for a command to be acceptable to the MT02 Controller, the bits in the Group Code must be 000.

Bits <07:05> of byte 01 in the CDB contain the LUN of the device being addressed. The MT02 Controller, acting as a SCSI Target, supports only 1 LUN (the QIC-36 interface tape drive). Therefore, the value for the LUN field in byte 01 in the CDB must be 000. The LUN must be specified for all commands. If a LUN value issued by the Initiator in an IDENTIFY message differs from the value specified in the CDB, the Initiator-specified value supersedes the value specified in the CDB. The definition of the low order bits in byte 01 is based on the current command.

The last byte (byte 05) in every CDB is a Control Byte which is differentiated into two groups of bits:

- The low-order two bits control the ability to link commands in a sequence and to notify the host adapter that a particular command (CDB) step has been completed. These two bits are designated Flag and Link in the command packet descriptions presented in this subsection for the MT02 Controller.

- The rest of the bits in the control byte are either reserved bits (they are 0) or are command-dependent bits.

  The remaining bytes in the CDB are primarily command-dependent.

Byte	Bit 07	06	05	04	03	02	01	00
00	Group Code			Command Code				
01	LUN			Command-Dependent				
02	Command-Dependent							
03	Command-Dependent							
04	Command-Dependent							
05	0	0	0	0	0	0	Flag	Link

Figure 8-1. Sample Group Code 0 Command Descriptor Block

8.3.1 Copy 18

The COPY CDB, shown below, causes large amounts of data to be moved from 1 peripheral device to another. The data transfer operation occurs offline and is performed without Initiator resources.

Byte	Bit 07	06	05	04	03	02	01	00
00	0	0	0	1	1	0	0	0
01	0	0	0	0	0	0	0	0
02	Length of Parameter List (MSB)							
03	Length of Parameter List							
04	Length of Parameter List (LSB)							
05	0	0	0	0	0	0	Flag	Link

An external device controller may be specified as either the source device or destination device, but at least one device must be internal to the MT02 Controller. If an external device is specified as a source or destination and the host adapter does not support the disconnect function, the **COPY** command terminates with an error because the MT02 Controller must disconnect from the host adapter before it can select the external device.

NOTE

The external device must support the **MODE SELECT** command so that the MT02 Controller can determine the block size of a direct-access device (disk drive).

The Initiator is responsible for properly positioning any sequential devices before beginning the **COPY** command. Any necessary error-recovery procedures for any external device are also the responsibility of the Initiator.

The MT02 Controller may disconnect from the Initiator on the SCSI bus during execution of this command without an error message being generated.

The MT02 Controller supports block sizes of 256 and 512 bytes for external devices.

Length of Parameter List - Bytes 02 through 04

The **COPY** command Parameter List specifies the length in bytes of the parameters that are sent during the Data Out Phase of the **COPY** command. The Parameter List is sent to the MT02 Controller as data, with Bytes 02 through 04 of the CDB specifying the length of the Parameter List. A zero value in the length indicates no copy of any data, but this condition is not treated as an error.

The **COPY** command Parameter List begins with a four-byte header that contains the Copy Function Code. One or more segment descriptors follow the header. The MT02 determines the format, length, and number of segment descriptors by the Copy Function Code (see Table 8-1). Up to 256 segment descriptors are permitted. The segment descriptors are identified by ascending numbers, beginning with 0.

Subsequent segments may change the source or destination LUN and device ID, if one of them is internal to the MT02 Controller.

The MT02 Controller supports sequential-to-random access, random-to-sequential access, and sequential-to-sequential access copy operations (see subsections 8.3.1.2 and 8.3.1.3).

Flag - Byte 05, Bit 01

The Flag bit is meaningful only when the Link bit (bit 00 in Byte 05) is set. Therefore, if both the Flag and Link bits are set, an interrupt is requested for this command in a group of linked commands.

Link - Byte 05, Bit 00

The use of the Link bit is optional. If the Link bit is set, an automatic link is made to the next command at the successful completion of the current command from the Initiator. Status is returned for each command executed.

NOTE

The MT02 disables recoverable errors on the internal sequential device before it begins the copy operation. The MT02 Controller only terminates the COPY command with a recoverable error if the destination device (disk or tape) had the recoverable error.

NOTE

For sequential-to-sequential access device copy operations, the host should issue the COPY command to the MT02 that acts as the destination device.

8.3.1.1 Parameter List Header

The Parameter List begins with a four-byte header that contains the **COPY** function code. One or more segment descriptors (see subsections 8.3.1.2 and 8.3.1.3) follow the Parameter List header.

Byte	Bit 07	06	05	04	03	02	01	00
00	0	0	0	CFC		0	0	0
01	0	0	0	0	0	0	0	0
02	0	0	0	0	0	0	0	0
03	0	0	0	0	0	0	0	0

Copy Function Code (CFC) - Byte 00, Bits <04:03>

These bits indicate the type of copy operation. Table 8-1 lists and describes the possible Copy Function Codes.

Table 8-1. **COPY** Command Function Codes

Bits 04	Bits 03	Description
0	0	Random-to-Sequential Access
0	1	Sequential-to-Random Access
1	0	Not Used
1	1	Sequential-to-Sequential Access

8.3.1.2 Random-to-Sequential Access and Sequential-to-Random Access Copy Operations

The **COPY** command segment descriptor for random-to-sequential access and sequential-to-random access copy operations is shown and described below. Up to 256 segment descriptors may be listed, provided they are within the Parameter List Length specified in Bytes 02 through 04 of the **COPY** CDB.

Byte	Bit 07	06	05	04	03	02	01	00
00	SCID			0	0	SLUN		
01	DCID			0	0	DLUN		
02	Sequential Device Block Size in Bytes (MSB)							
03	Sequential Device Block Size in Bytes (LSB)							
04	Number of Blocks (Random Device) (MSB)							
05	Number of Blocks							
06	Number of Blocks							
07	Number of Blocks (LSB)							
08	Logical Block Address (Random Device) (MSB)							
09	Logical Block Address							
10	Logical Block Address							
11	Logical Block Address (LSB)							

Source Controller ID (SCID) - Byte 00, Bits <07:05>

These bits specify the SCSI bus address of the controller for the source device.

Source Logical Unit Number (SLUN) - Byte 00, Bits <02:00>

These bits specify the LUN of the source device.

Destination Controller ID (DCID) - Byte 01, Bits <07:05>

These bits specify the SCSI bus address of the controller for the destination device.

Destination LUN (DLUN) - Byte 01, Bits <02:00>

These bits specify the LUN of the destination device.

Sequential Device Block Size - Bytes 02 and 03

These bytes specify the block size to be used for the sequential access device during the copy operation. If this block size cannot be supported, the MT02 Controller sends a CHECK CONDITION status code to the Initiator and sets the Sense Key in the Extended Sense Byte to the ILLEGAL REQUEST code. During a read or write operation to the sequential access device, if the MT02 Controller determines that the block size is invalid, it terminates the copy operation and sends a CHECK CONDITION status code to the Initiator and sets the Sense Key in the Extended Sense Byte to the COPY ABORTED code.

Number of Blocks (Random Device) - Bytes 04 through 07

These bytes specify the number of random access blocks to be transferred in the current segment. A zero value indicates that no blocks are to be transferred in this segment.

Logical Block Address (Random Device) - Bytes 08 through 11

These bytes specify the starting logical block address on the random access device for this Transfer operation. The value is in terms of the actual block size of the random access device. Odd block counts are allowable only if the sequential and random devices have identical block sizes (512-byte blocks only).

8.3.1.3 Sequential-to-Sequential Access Copy Operations

Up to 256 segment descriptors may be listed, provided they are within the Parameter List Length specified in Bytes 02 through 04 of the **COPY** CDB.

Source Controller ID (SCID) - Byte 00, Bits <07:05>

These bits specify the SCSI bus address of the MT02 Controller for the source device.

Byte	Bit 07	06	05	04	03	02	01	00
00	SCID			0	0	SLUN		
01	DCID			0	0	DLUN		
02	0	0	0	0	0	0	0	0
03	0	0	0	0	0	0	0	0
04	Source Block Size in bytes (MSB)							
05	Source Block Size in bytes (LSB)							
06	Destination Block Size in bytes (MSB)							
07	Destination Block Size in bytes (LSB)							
08	Source Number of Blocks (MSB)							
09	Source Number of Blocks							
10	Source Number of Blocks							
11	Source Number of Blocks (LSB)							

Source Logical Unit Number (SLUN) - Byte 00, Bits <02:00>

These bits specify the Logical Unit Number (LUN) of the source device.

Destination Controller ID (DCID) - Byte 01, Bits <07:05>

These bits specify the SCSI bus address of the MT02 Controller for the destination device.

Destination LUN (DLUN) - Byte 01, Bits <02:00>

These bits specify the Logical Unit Number (LUN) of the destination device.

Source Block Size - Bytes 04 and 05

These bytes specify the block size (i.e., number of blocks) to be used on the source device for this segment of the copy operation.

Destination Block Size - Bytes 06 and 07

These bytes specify the block size (i.e., number of bytes) to be used on the destination device for this segment of the copy operation.

Source Number of Blocks - Bytes 08 through 11

These bytes specify the number of blocks to be transferred from the source device during this segment. A zero value indicates no blocks are to be transferred.

8.3.1.4 Error and Other Conditions During a Copy Operation

The following paragraphs describe the two classes of unusual conditions that can occur during a copy operation and the ways the MT02 Controller responds to such conditions.

NOTE

Sense data for these unusual conditions must be returned in an Extended Sense Byte format, the Parameter Length field specified in the **REQUEST SENSE** CDB (see subsection 8.3.12) must be 12 hexadecimal.

8.3.1.4.1 Copy Operation Management Errors

The first class of unusual conditions consists of those detected by the MT02 Controller when it is managing the data transfer part of the copy operation. The unusual conditions include:

- Invalid parameters in the **COPY** command
- Invalid segment descriptors

If a copy operation management error occurs, the MT02 Controller performs the following operations:

- Terminates with CHECK CONDITION status code.
- Sets the Valid Address (VADD) bit in the Extended Sense Byte to 1. Sets the Sense Key to the Sense Key code that describes the unusual condition.
- Sets Extended Sense Byte 01 to the current Segment Descriptor number. The Segment Descriptors are identified by ascending numbers beginning with 0.
- Sets the Sense Information Bytes of the Extended Sense Bytes 03 through 06 to the difference (residue) between the value in the Number of Blocks field of the current segment descriptor for the source device and the actual number of source blocks written on the destination device media.

8.3.1.4.2 Copy Operation Data Transfer Errors

The second class of unusual conditions consists of errors detected by devices on the SCSI bus during the Data Transfer part of the copy operation. The MT02 Controller must recover the Sense data associated with the unusual condition.

After the MT02 Controller recovers the Sense data associated with the detected error, it performs the following operations:

- Terminates with CHECK CONDITION status code.
- Sets the VADD bit 07 in Extended Sense Byte 00 to 1.
- Sets the Segment Number in Extended Sense Byte 01 to the number of the current Segment Descriptor being processed at the time the unusual condition is detected. The Segment Descriptors are identified by ascending numbers beginning with 0.
- Sets the code in the Sense Key field in Extended Sense Byte 02 to the code for COPY ABORTED.
- Sets the Sense Information Bytes of the Extended Sense Bytes 03 through 06 to the difference (residue) between the value in the Number of Blocks field of the current segment descriptor for the source device and the actual number of source blocks successfully copied.
- Sets the First Additional Sense Length Byte (Byte 08) to the byte number (relative to Byte 00) of the beginning of the source device's Status Byte and Sense data. A zero value in the byte indicates no Status Byte and Sense data are being returned from the source device. If the source device is external to the MT02 Controller, the first byte of the area pointed to by the first Additional Sense Byte contains the completion status from the source device. Subsequent bytes contain the Standard (Non-Extended) Sense data (unchanged) recovered from the source device.

- Sets the Second Additional Sense Length Byte (Byte 09) to the byte number (relative to Byte 00) of the beginning of the destination device's Status Byte and Sense data. A zero value in this byte indicates no Status Byte and Sense data are being returned from the destination device. If the destination device is external to the MT02 Controller, the first byte of the area pointed to by the second Additional Sense Byte contains the completion status from the destination device. Subsequent bytes contain the Standard (Non-Extended) Sense data (unchanged) recovered from the destination device.

8.3.2 Erase 19

The **ERASE** CDB, shown below, causes the entire media cartridge to be erased.

Byte	Bit 07	06	05	04	03	02	01	00
00	0	0	0	1	1	0	0	1
01	0	0	0	0	0	0	0	1
02	0	0	0	0	0	0	0	0
03	0	0	0	0	0	0	0	0
04	0	0	0	0	0	0	0	0
05	0	0	0	0	0	0	Flag	Link

The SCSI standard specifies that only a portion of the tape be erased; however, the MT02 Controller erases the entire tape. Failure to set the Long bit (byte 01, bit 00) to logic 1 results in an error condition.

If the disconnect function is enabled, the MT02 Controller may disconnect from the Initiator while executing this command.

Flag - Byte 05, Bit 01

The Flag bit is meaningful only when the Link bit (bit 00 in Byte 05) is set. Therefore, if both the Flag and Link bits are set, an interrupt is requested for this command in a group of linked commands.

Link - Byte 05, Bit 00

The use of the Link bit is optional. If the Link bit is set, an automatic link is made to the next command at the successful completion of the current command from the Initiator. Status is returned for each command executed.

8.3.3 Inquiry 12

The **INQUIRY** CDB, shown below, causes a request to be made for the transfer of data from the Target to the Initiator. The data to be transferred describes unique parameters that are pertinent to the MT02 Controller. The number of bytes transferred depends on the number of bytes requested by the contents of Byte 04.

	Bit							
Byte	07	06	05	04	03	02	01	00
00	0	0	0	1	0	0	1	0
01	0	0	0	0	0	0	0	0
02	0	0	0	0	0	0	0	0
03	0	0	0	0	0	0	0	0
04	Number of Bytes in Transfer							
05	0	0	0	0	0	0	Flag	Link

The MT02 Controller will not disconnect from the Initiator while executing this command.

Number of Bytes in Transfer - Byte 04

This byte specifies the number of bytes which the Initiator has allocated for returned Target data. A value of 0 indicates that no data is transferred. This condition is not an error condition.

Flag - Byte 05, Bit 01

The Flag bit is meaningful only when the Link bit (bit 00 in Byte 05) is set. Therefore, if both the Flag and Link bits are set, an interrupt is requested for this command in a group of linked commands.

Link - Byte 05, Bit 00

The use of the Link bit is optional. If the Link bit is set, an automatic link is made to the next command at the successful completion of the current command from the Initiator. Status is returned for each command executed.

8.3.3.1 Inquiry Data Format

During the Data In Phase of the **INQUIRY** command, data is transferred in the following format:

Byte	Bit 07	06	05	04	03	02	01	00
00	0	0	0	0	0	0	0	DTYP
01	RMV	0	0	0	0	0	0	0
02	0	0	0	0	0	0	Version	
03	0	0	0	0	0	0	0	0
04	0	0	0	0	0	0	0	0

Device Type (DTYP) - Byte 00, Bit 00

Byte 00 indicates the Device Type code. The DTYP bit is set to 1 to indicate a sequential access device is being used with the MT02 Controller.

Device Type Qualifier - Byte 01

Bit 07 (RMV) of the Device Type Qualifier (Byte 01) is set to 1 to indicate that a removable media (i.e., tape cartridge) is being used with the MT02 Controller. Bits <06:00> of this byte are reserved and are 0.

Version - Byte 02

This byte is set to 1 (hex) to indicate compliance with the published ANSI SCSI standard.

Length of Additional Bytes - Byte 04

This byte is formatted to indicate there are no additional bytes to be transferred.

8.3.4 Load/Unload 1B

The **LOAD/UNLOAD** CDB, shown below, informs the MT02 Controller that a new tape cartridge is to be loaded and positioned to beginning-of-tape (BOT) if the **LOAD** command is issued, or that an existing tape cartridge is to be made ready for removal from the tape drive if the **UNLOAD** command is issued. The **LOAD/UNLOAD** command is also used to perform a re-tension pass on the tape. The **LOAD/UNLOAD** command is an optional command when the auto-load procedure is enabled (see the AUI bit definition in subsection 8.3.5.1); it does not need to be issued every time a tape cartridge is installed.

	Bit							
Byte	07	06	05	04	03	02	01	00
00	0	0	0	1	1	0	1	1
01	0	0	0	0	0	0	0	0
02	0	0	0	0	0	0	0	0
03	0	0	0	0	0	0	0	0
04	0	0	0	0	0	0	RET	Load
05	EOT	0	0	0	0	0	Flag	Link

If the disconnect function is enabled, the MT02 Controller may disconnect from the Initiator while executing this command.

If an auto-load operation is in progress, the MT02 Controller returns a BUSY status code on the **TEST UNIT READY** and **MODE SENSE** commands.

When a **LOAD** command is received, the MT02 Controller illuminates the Not Safe to Remove Cartridge LED (LED 2, see Figure 4-1). LED 2 remains lit until the tape cartridge is removed or until an **UNLOAD** command is executed, unless an outstanding **PREVENT MEDIUM REMOVAL** command (see subsection 8.3.7) exists.

Re-tension (RET) - Byte 04, Bit 01

When the RET bit is set to 1, the MT02 Controller performs a re-tension pass on the tape media before the **LOAD** or **UNLOAD** command is completed. When the bit is reset to 0, no re-tension pass is performed. Retensioning removes tension operation anomalies.

Load - Byte 04, Bit 00

When the Load bit is set to 1, the media on the addressed tape drive is loaded and positioned to BOT. When the Load bit is reset to 0, the media on the addressed tape unit is positioned for removal.

End-of-Tape (EOT) - Byte 05, Bit 07

When the EOT bit is set during an unload operation, the tape is positioned to end-of-tape (EOT) and logically unloaded. This action positions the tape so the MT02 Controller can perform a re-tension pass in the minimum amount of time when the tape is loaded. When the EOT bit is reset to 0, the tape is positioned to the beginning-of-tape (BOT) after an UNLOAD command is issued.

Flag - Byte 05, Bit 01

The Flag bit is meaningful only when the Link bit (bit 00 in Byte 05) is set. Therefore, if both the Flag and Link bits are set, an interrupt is requested for this command in a group of linked commands.

Link - Byte 05, Bit 00

The use of the Link bit is optional. If the Link bit is set, an automatic link is made to the next command at the successful completion of the current command from the Initiator. Status is returned for each command executed.

8.3.5 Mode Select 15

The **MODE SELECT** CDB, shown below, enables an Initiator to specify device parameters to the MT02 Controller.

Byte	Bit 07	06	05	04	03	02	01	00
00	0	0	0	1	0	1	0	1
01	0	0	0	0	0	0	0	0
02	0	0	0	0	0	0	0	0
03	0	0	0	0	0	0	0	0
04	0	0	0	0	Param List Length			
05	0	0	0	0	0	0	Flag	Link

The MT02 Controller will not disconnect from the Initiator while executing this command.

Parameter List Length - Byte 04, Bits <02:00>

These bytes specify the length in bytes of the parameters sent during the Data Out Phase of this command. Valid values for bits in the Parameter List Length field are 0, and four through thirteen. If the MT02 Controller receives a value of 0, it does not transfer any data, but it does not treat this condition as an error.

Flag - Byte 05, Bit 01

The Flag bit is meaningful only when the Link bit (bit 00 in Byte 05) is set. Therefore, if both the Flag and Link bits are set, an interrupt is requested for this command in a group of linked commands.

Link - Byte 05, Bit 00

The use of the Link bit is optional. If the Link bit is set, an automatic link is made to the next command at the successful completion of the current command from the Initiator. Status is returned for each command executed.

8.3.5.1 Mode Select Parameter List

The Mode Select Parameter List, shown below, is sent during the Data Phase of the **MODE SELECT** command:

Byte	Bit 07	06	05	04	03	02	01	00
00	0	0	0	0	0	0	0	0
01	0	0	0	0	0	0	0	0
02	0	0	0	BUFM	0	0	0	0
03	Descriptor Length							
04	Density Code							
05	Number of Blocks (MSB)							
06	Number of Blocks							
07	Number of Blocks (LSB)							
08	0	0	0	0	0	0	0	0
09	Block Size (MSB)							
10	Block Size							
11	Block Size (LSB)							
12	0	0	0	0	0	DEA	AUI	SEC

Byte 01

This byte is 0 to indicate the media type is the default value (the media type of the media currently loaded in the tape drive).

Buffered Mode - (BUFM) Byte 02, Bit 04

The Buffered Mode (BUFM) bit is used to indicate whether the MT02 Controller is or is not to report GOOD STATUS (defined in Table 7-1) as soon as the data block specified by the **WRITE** or **VERIFY** command has been transferred to the cache buffer in the MT02 Controller. The set condition of BUFM indicates GOOD STATUS is to be reported at that time. Four or more data blocks may be buffered before those data blocks

are written to the tape. If the BUFM bit is reset to 0, the MT02 Controller is not to report GOOD STATUS during execution of **WRITE** or **VERIFY** commands until the data blocks are actually written or verified to the tape.

When the MT02 Controller is operating in the buffered mode, it may terminate commands before data is actually written or verified to the tape. If this situation occurs, the MT02 Controller reports any errors encountered when the Initiator issues the next command. Usually, the MT02 Controller sends a CHECK CONDITION status code to the Initiator and sets the VADD bit in the Extended Sense Byte to 1. The Sense Information Bytes (in the Extended Sense Byte) contain the Residual Count, which may be greater than the requested count if the error occurred on a previous operation.

Descriptor Length - Byte 03

This byte specifies the length in bytes of the Parameter List. Valid values for this byte are 0 or 8.

Density Code - Byte 04

This byte defines the density of the medium on the MT02 Controller. This byte may be set to 0 or 5 (hex) to indicate the default density, which is a 0.25-inch tape with a QIC-24 data format and 9 tracks. The byte may also be set to 4 (hex) to indicate the tape cartridge is a 0.25-inch tape with a QIC-11 data format and 4 tracks, or to 84 (hex) to indicate the tape cartridge is a 0.25-inch tape with a QIC-11 data format and 9 tracks.

Number of Blocks (MSB) - Bytes 05 through 07

These bytes are ignored by the MT02 Controller.

Block Size - Bytes 09 through 11

These bytes are ignored by the MT02 Controller.

Disable Erase Ahead (DEA) - Byte 12, Bit 02

The DEA bit enables or disables the MT02 Controller erase ahead option. The default value for this bit is 0 (hex). When the DEA bit is reset to 0, after the MT02 Controller writes its last outstanding block, it will erase 55 inches of the tape if recording on track 0. This action allows the user to remove the tape cartridge at any time. When the DEA bit is set to 1 (hex), after the

8.3.6 Mode Sense 1A

The **MODE SENSE** CDB, shown below, causes an Initiator to determine the parameters of the MT02 Controller. **MODE SENSE** is a complementary command to the **MODE SELECT** command (see subsection 8.3.5), and is used for support of media that may contain different densities.

Byte	Bit 07	06	05	04	03	02	01	00
00	0	0	0	1	1	0	1	0
01	0	0	0	0	0	0	0	0
02	0	0	0	0	0	0	0	0
03	0	0	0	0	0	0	0	0
04	0	0	0	0	Length of Data List			
05	0	0	0	0	0	0	Flag	Link

If the MT02 receives a zero value in Byte 04, it does not transfer any data and does not treat this condition as an error.

If an auto-load operation is in progress, the MT02 Controller returns a BUSY status code and does not return any sense data.

The MT02 Controller will not disconnect from the Initiator while executing this command.

Length of Data List - Byte 04, Bits <03:01>

These bits specify the length in bytes of the parameters to be transferred during the Data Phase. If these bits equal 0, no data is to be transferred. A maximum of 13 (decimal) bytes will be returned.

Flag - Byte 05, Bit 01

The Flag bit is meaningful only when the Link bit (bit 00 in Byte 05) is set. Therefore, if both the Flag and Link bits are set, an interrupt is requested for this command in a group of linked commands.

Link - Byte 05, Bit 00

The use of the Link bit is optional. If the Link bit is set, an automatic link is made to the next command at the successful completion of the current command from the Initiator. Status is returned for each command executed.

8.3.7 Prevent/Allow Medium Removal 1E

The **PREVENT/ALLOW MEDIUM REMOVAL** command, shown below, requests the MT02 Controller to enable or to disable the function that allows the MT02 to remove the tape from the tape drive.

Byte	Bit 07	06	05	04	03	02	01	00
00	0	0	0	1	1	0	1	0
01	0	0	0	0	0	0	0	0
02	0	0	0	0	0	0	0	0
03	0	0	0	0	0	0	0	0
04	0	0	0	0	0	0	0	PREV
05	0	0	0	0	0		Flag	Link

The MT02 Controller will not disconnect from the Initiator while executing this command.

Prevent Removal (PREV) - Byte 04, Bit 00

Since 0.25-inch tape cartridge drives cannot be mechanically controlled to prevent the removal of the medium, when the PREV bit is set to 1, the MT02 Controller illuminates the Not Safe to Remove Cartridge LED (LED 2 on the MT02 Controller) and the LED on the tape access door. When the PREV bit is reset to 0, the MT02 Controller extinguishes LED 2, unless the cartridge is loaded.

The MT02 Controller also extinguishes LED 2 when there occurs either of the two following event sequences:

- Any Initiator issues a BUS DEVICE RESET message.
- A SCSI bus Hard Reset condition (see subsection 7.6.1) occurs.

If a **LOAD/UNLOAD** command is issued after a **PREVENT MEDIA REMOVAL** command is issued, the MT03 Controller does not change the state of LED 2.

Flag - Byte 09, Bit 01

The Flag bit is meaningful only when the Link bit (bit 00 in Byte 05) is set. Therefore, if both the Flag and Link bits are set, an interrupt is requested for this command in a group of linked commands.

MT02 Controller writes the last block, it performs the erase operation only when the last block is a file mark, or if the host issued a **REWIND** or **UNLOAD** command after the last **WRITE** command (see subsection 5.3.8).

NOTE

The erase ahead option enabled by the DEA bit provides faster write repositions, but the tape cartridge must not be removed until the host has issued a **REWIND** or **UNLOAD** command, otherwise data loss may occur.

Auto-Load Inhibit (AUI) - Byte 12, Bit 01

When the AUI bit is 0, and when the tape cartridge is inserted or when a cartridge is present during power-up or reset, the MT02 Controller performs an auto-load procedure. During an auto-load procedure, the tape cartridge is logically loaded and a **LOAD** command does not need to be issued. When the AUI bit is set to 1, the MT02 Controller inhibits the auto-load procedure and a **LOAD** command must be executed before the MT02 Controller can perform any additional commands.

Soft Error Count (SEC) - Byte 11, Bit 00

The SEC bit is used to specify if recoverable errors are to be reported by the MT02 Controller. When the SEC bit is 0, the MT02 Controller issues a CHECK CONDITION status code after it executes a command that caused a recoverable error to occur. Information about the Sense Key and Sense Code for the recoverable error can be obtained by issuing a **REQUEST SENSE** command. When the SEC bit is set to 1, the MT02 Controller does not issue a CHECK CONDITION status code; however, the accumulated number of soft errors can be retrieved by issuing a **REQUEST SENSE** command.

8.3.6 Mode Sense 1A

The **MODE SENSE** CDB, shown below, causes an Initiator to determine the parameters of the MT02 Controller. **MODE SENSE** is a complementary command to the **MODE SELECT** command (see subsection 8.3.5), and is used for support of media that may contain different densities.

Byte	Bit 07	06	05	04	03	02	01	00
00	0	0	0	1	1	0	1	0
01	0	0	0	0	0	0	0	0
02	0	0	0	0	0	0	0	0
03	0	0	0	0	0	0	0	0
04	0	0	0	0	Length of Data List			
05	0	0	0	0	0	0	Flag	Link

If the MT02 receives a zero value in Byte 04, it does not transfer any data and does not treat this condition as an error.

If an auto-load operation is in progress, the MT02 Controller returns a BUSY status code and does not return any sense data.

The MT02 Controller will not disconnect from the Initiator while executing this command.

Length of Data List - Byte 04, Bits <03:01>

These bits specify the length in bytes of the parameters to be transferred during the Data Phase. If these bits equal 0, no data is to be transferred. A maximum of 13 (decimal) bytes will be returned.

Flag - Byte 05, Bit 01

The Flag bit is meaningful only when the Link bit (bit 00 in Byte 05) is set. Therefore, if both the Flag and Link bits are set, an interrupt is requested for this command in a group of linked commands.

Link - Byte 05, Bit 00

The use of the Link bit is optional. If the Link bit is set, an automatic link is made to the next command at the successful completion of the current command from the Initiator. Status is returned for each command executed.

8.3.6.1 Mode Sense Data Format

Data is sent during the Data In Phase of the **MODE SENSE** command in the format shown below.

Byte	Bit 07	06	05	04	03	02	01	00
00	0	0	0	0	1	1	0	0
01	Media Type							
02	WRP	0	0	BUFM	0	0	SPD	
03	Descriptor Length							
04	Density Code							
05	Number of Blocks (MSB)							
06	Number of Blocks							
07	Number of Blocks (LSB)							
08	0	0	0	0	0	0	0	0
09	Block Size (MSB)							
10	Block Size							
11	Block Size (LSB)							
12	0	0	0	0	0	DEA	AUI	SEC

Byte 00

This byte indicates the length of the Mode Sense Data is 12 (decimal). The data length does not include this byte (Byte 00).

Media Type - Byte 01

The Media Type byte determines the type of media. When the Media Type byte is equal to 81 (hexadecimal), a low-corrosivity tape data cartridge is installed. When the Media Type byte is equal to 80 (hexadecimal), a high-corrosivity tape data cartridge is installed.

Write Protect (WRP) - Byte 02, Bit 07

When the Write Protect bit is set to 1, either the the tape drive is write protected or the loaded cartridge is write protected.

Buffered Mode - (BUFM) Byte 02, Bit 04

The Buffered Mode (BUFM) bit indicates when the MT02 Controller reports GOOD STATUS. The set condition of BUFM indicates GOOD STATUS will be reported. Four or more data blocks may be buffered before those data blocks are written to the tape. If the BUFM bit is reset to 0, the MT02 Controller will not report GOOD STATUS during execution of **WRITE** or **VERIFY** commands until the data blocks are actually written or verified to the tape.

Speed (SPD) - Byte 02, Bits <01:00>

These bits indicate the speed of the tape drive. These bits are equal to 10, indicating that the speed is 90 ips.

Descriptor Length - Byte 03

This byte specifies the length in bytes of the Parameter List. This byte has a value of 8. The vendor-unique byte (Byte 12) is not included in the Descriptor Length.

Density Code - Byte 04

This byte defines the density of the media on the MT02 Controller. This byte may be set to 0 or 5 (hex) to indicate the default density, which is a 0.25-inch tape with a QIC-24 data format and 9 tracks. The byte may also be set to 4 (hex) to indicate the tape cartridge is a 0.25-inch tape with a QIC-11 data format and 4 tracks, or to 84 (hex) to indicate the tape cartridge is a 0.25-inch tape with a QIC-11 data format and 9 tracks.

Number of Blocks (MSB) - Bytes 05 through 07

These bytes indicate the total number of data blocks on the tape. This value is an estimate. For media type equal to 80 hexadecimal, this estimate assumes a 450-foot tape. For media type equal to 81 hexadecimal, this estimate assumes a 600-foot tape.

Block Size - Bytes 09 through 11

These bytes are coded to indicate the block size is equal to 512 bytes.

Disable Erase Ahead (DEA) - Byte 12, Bit 02

The DEA bit indicates whether the MT02 Controller erase ahead option is enabled. If the DEA bit is reset to 0 (option not enabled), after the MT02 Controller writes the last block, it erases 55 inches of tape if recording on track 0. This action allows the user to remove the tape cartridge at any time. If the DEA bit is set to 1 (option enabled), after the MT02 Controller writes the last block, it performs the erase operation only when the last block is a file mark, or if the host issued a **REWIND** or **UNLOAD** command after the last **WRITE** command.

NOTE

The erase ahead option enabled by the DEA bit provides faster write repositions, but the tape cartridge must not be removed until the host has issued a **REWIND** or **UNLOAD** command, otherwise data loss may occur.

Auto-Load Inhibit (AUI) - Byte 12, Bit 01

The AUI bit indicates whether the auto-load option has been selected. If the AUI bit is 0, when the tape cartridge is inserted, the MT02 Controller performs an auto-load procedure. During an auto-load procedure, the tape cartridge is logically loaded and a **LOAD** command does not need to be issued. If the AUI bit is set to 1, the MT02 Controller inhibits the auto-load procedure and a **LOAD** command must be executed before the MT02 Controller can perform any additional commands.

Soft Error Count (SEC) - Byte 12, Bit 00

The SEC bit indicates if recoverable errors are being reported by the MT02 Controller. If the SEC bit is 0, the MT02 Controller issues a CHECK CONDITION status code after it executes a command that caused a recoverable error to occur. Information about the Sense Key and Sense Code for the recoverable error can be obtained by issuing a **REQUEST SENSE** command. If the SEC bit is set to 1, the MT02 Controller does not issue a CHECK CONDITION status code; however, the accumulated number of soft errors can be retrieved by issuing a **REQUEST SENSE** command.

8.3.7 Prevent/Allow Medium Removal 1E

The **PREVENT/ALLOW MEDIUM REMOVAL** command, shown below, requests the MT02 Controller to enable or to disable the function that allows the MT02 to remove the tape from the tape drive.

Byte	Bit 07	06	05	04	03	02	01	00
00	0	0	0	1	1	0	1	0
01	0	0	0	0	0	0	0	0
02	0	0	0	0	0	0	0	0
03	0	0	0	0	0	0	0	0
04	0	0	0	0	0	0	0	PREV
05	0	0	0	0	0	0	Flag	Link

The MT02 Controller will not disconnect from the Initiator while executing this command.

Prevent Removal (PREV) - Byte 04, Bit 00

Since 0.25-inch tape cartridge drives cannot be mechanically controlled to prevent the removal of the medium, when the PREV bit is set to 1, the MT02 Controller illuminates the Not Safe to Remove Cartridge LED (LED 2 on the MT02 Controller) and the LED on the tape access door. When the PREV bit is reset to 0, the MT02 Controller extinguishes LED 2, unless the cartridge is loaded.

The MT02 Controller also extinguishes LED 2 when there occurs either of the two following event sequences:

- Any Initiator issues a BUS DEVICE RESET message.
- A SCSI bus Hard Reset condition (see subsection 7.6.1) occurs.

If a **LOAD/UNLOAD** command is issued after a **PREVENT MEDIA REMOVAL** command is issued, the MT03 Controller does not change the state of LED 2.

Flag - Byte 09, Bit 01

The Flag bit is meaningful only when the Link bit (bit 00 in Byte 05) is set. Therefore, if both the Flag and Link bits are set, an interrupt is requested for this command in a group of linked commands.

Link - Byte 09, Bit 00

The use of the Link bit is optional. If the Link bit is set, an automatic link is made to the next command at the successful completion of the current command from the Initiator. Status is returned for each command executed.

8.3.8 Read 08

The **READ** CDB, shown below, causes data to be read from the Target device and transferred to the Initiator. The amount of data transferred is a multiple of the block length (i.e., 512 data bytes/block). The **READ** command specifies the number of data blocks to be read. The **READ** command terminates when there is present one of the following conditions:

- The number of data blocks to be read is transferred
- A File Mark is encountered
- The End-of-Media is encountered
- An unrecoverable read error occurs on a block.

Byte	Bit 07	06	05	04	03	02	01	00
00	0	0	0	0	1	0	0	0
01	0	0	0	0	0	0	0	1
02	Number Blocks to Transfer (MSB)							
03	Number Blocks to Transfer							
04	Number Blocks to Transfer (LSB)							
05	0	0	0	0	0	0	Flag	Link

If a file mark is encountered during a **READ** command, the MT02 Controller sends a CHECK CONDITION status code to the Initiator and sets the File Mark bit in the Extended Sense (Byte 02) to 1 and the Sense Key (in the Extended Sense Byte) to GOOD. The Valid Address bit in Extended Sense Byte is set to 1 and the Sense Information Bytes are set to the difference between the requested transfer length and the actual number of blocks successfully read. The non-extended Error Class and Code are set to FILE MARK DETECTED.

NOTE

If a recoverable error occurs on a file mark block, the MT02 returns a Sense key that only reflects that a file mark was detected.

If a logical EOM (which indicates a lack of data on a tape cartridge) is detected during a **READ** command, the MT02 Controller sends a CHECK CONDITION status code to the Initiator and sets a BLANK CHECK error code in the Extended Sense Byte. The Valid Address bit is set to 1 and the Sense Information Bytes are set to the difference between the requested transfer length and the actual number of blocks successfully read. The non-extended Error Class and Code are set to READ EOM.

If an unrecoverable error occurs during a read operation, the MT02 Controller terminates the **READ** command and sends a CHECK CONDITION status code. It sets the VADD bit in the Extended Sense Byte to 1. The Sense Information Bytes contain the Residual Count (total number of blocks not read). Table 8-2 lists media-related or drive-related errors which can occur during a read operation and their corresponding Sense Keys and Sense Code. (Sense Keys and Sense Codes are listed in their hexadecimal values.) General error conditions that occur during MT02 Controller tape operations are listed and described in Table A-1.

If the physical end-of-tape (EOT) occurs during a **READ** command, the MT02 Controller sends a CHECK CONDITION status code to the Initiator and sets the Sense Key in Extended Sense (Byte 02) to NO SENSE with the EOM bit set to 1. The Valid Address bit is set to 1 and the Sense Information Bytes are set to the difference between the requested transfer length and the actual number of blocks successfully read.

The MT02 Controller does not require a file mark to be the absolute last block on a tape cartridge for an EOM condition to be detected. It is recommended that the host write a file mark as the last block and check that a file mark is the last block read during the execution of a **READ** command. This action ensures the MT02 Controller did not miss the last block because an error condition occurred on the block.

If an additional **READ** command is issued after a read error occurs, the read operation begins on the block that follows the block where the error occurred.

The Soft Error Count (the number of recoverable errors) is cleared on the first **READ** command that is issued after a non-**READ** command has been executed.

The MT02 Controller ignores blocks that have a non-zero control nibble (see subsection 5.3.4.2).

If the Disconnect function is enabled, the MT02 Controller may disconnect from the Initiator while executing this command.

Table 8-2. **READ** Command Error Conditions

Sense Key	Sense Code	Read Error
BLANK CHECK (08)	READ EOM (34)	The MT02 detected a logical end-of-media condition.
ILLEGAL REQUEST (05)	READ EOM (34)	A **READ** command was issued after a **WRITE** command but no intervening rewind operation occurred.
ILLEGAL REQUEST (05)	INVALID COMMAND (20)	After a **VERIFY** command in the immediate mode was issued, a **READ** command was issued before the verify operation was completed.
NO SENSE (00)	FILE MARK (1C)	The MT02 detected a file mark. The FM bit in the Extended Sense Byte is set to 1.
NO SENSE (00)	READ EOM (34)	The MT02 detected a physical end-of-media.

Byte 01, Bit 00

The MT02 Controller sends an INVALID COMMAND error code if the Fixed Block Mode bit (byte 01, bit 00) in the **READ** command packet is not set to 1.

Number of Blocks to Transfer - Bytes 02 to 04

These bytes specify the number of bytes the Initiator has allocated for the returned data. When this byte is 0, no data is transferred and the current position is not changed. This condition is not considered an error.

Flag - Byte 05, Bit 01

The Flag bit is meaningful only when the Link bit (bit 00 in Byte 05) is set. Therefore, if both the Flag and Link bits are set, an interrupt is requested for this command in a group of linked commands.

Link - Byte 05, Bit 00

The use of the Link bit is optional. If the Link bit is set, an automatic link is made to the next command at the successful completion of the current command from the Initiator. Status is returned for each command executed.

8.3.9 Read Block Limits 05

The **READ BLOCK LIMITS** CDB, shown below, returns the block-length limits of the addressed device as data. Fixed blocks of 512 bytes are the only supported block formats.

	Bit							
Byte	07	06	05	04	03	02	01	00
00	0	0	0	0	0	1	0	1
01	0	0	0	0	0	0	0	0
02	0	0	0	0	0	0	0	0
03	0	0	0	0	0	0	0	0
04	0	0	0	0	0	0	0	0
05	0	0	0	0	0	0	Flag	Link

The MT02 Controller will not disconnect from the Initiator while executing this command.

8.3.9.1 Read Block Limits Data Format

During the Data In Phase of the **READ BLOCK LIMITS** command, data is sent in the following format:

Byte	Bit 07	06	05	04	03	02	01	00
00	0	0	0	0	0	0	0	0
01	Maximum Block Length (MSB)							
02	Maximum Block Length							
03	Maximum Block Length (LSB)							
04	Minimum Block Length (MSB)							
05	Minimum Block Length (LSB)							

The maximum and minimum block length is 512 bytes.

8.3.10 Recovered Buffer Data 14

The **RECOVER BUFFERED DATA** CDB, shown below, causes recovery of data that has been written to the data buffer in the MT02 Controller but which has not yet been written to tape. Usually, this command is used only to recover from error or exception conditions that prevent writing the buffered data to tape.

This command function is similar to the **READ** command function, except the data is transferred from the MT02 Controller data buffer instead of from tape. The order in which data blocks are transferred is the same as they would have been transferred to the tape.

This command should be used only in response to a VOLUME OVERFLOW Sense Key Error code in the Extended Sense Bytes.

Byte	Bit 07	06	05	04	03	02	01	00
00	0	0	0	1	0	1	0	0
01	0	0	0	0	0	0	0	1
02	Number Blocks (MSB)							
03	Number Blocks							
04	Number Blocks (LSB)							
05	0	0	0	0	0	0	Flag	Link

If an attempt is made to read more blocks than are contained in the buffer, the MT02 Controller sends a CHECK CONDITION status code. It also issues the BLANK CHECK Sense Key and sets the VADD bit in the Extended Sense Bytes to 1. The Sense Information Bytes contain the number of blocks that could not be transferred.

If the disconnect function is enabled, the MT02 Controller may disconnect from the Initiator while executing this command.

Fixed - Byte 01, Bit 00

This bit must be set to 1 to ensure the Valid Address bit is set to 1 and the Sense Information Bytes contain the number of blocks that could not be transferred.

Number of Blocks - Bytes 02 to 04

These bytes specify the number of blocks of data to be transferred from the data buffer in the MT02 Controller to the Initiator.

Flag - Byte 05, Bit 01

The Flag bit is meaningful only when the Link bit (bit 00 in Byte 05) is set. Therefore, if both the Flag and Link bits are set, an interrupt is requested for this command in a group of linked commands.

Link - Byte 05, Bit 00

The use of the Link bit is optional. If the Link bit is set, an automatic link is made to the next command at the successful completion of the current command from the Initiator. Status is returned for each command executed.

8.3.11 Release Unit 17

The **RELEASE UNIT** CDB, shown below, causes the LUN connected to the MT02 Controller previously reserved with the **RESERVE UNIT** command to be released if the requesting Initiator reserved it last. Once the **RELEASE UNIT** command is issued, other Initiators can access the MT02 Controller.

Byte	Bit 07	06	05	04	03	02	01	00
00	0	0	0	1	0	1	1	1
01	0	0	0	THPR	Third Party ID			0
02	0	0	0	0	0	0	0	0
03	0	0	0	0	0	0	0	0
04	0	0	0	0	0	0	0	0
05	0	0	0	0	0	0	Flag	Link

It is not an error to attempt to release to the requesting Initiator any LUN that is not currently reserved.

The MT02 Controller will not disconnect from the Initiator while executing this command.

Third Party Reservation Release Option (THPR) - Byte 01, Bit 04

If the Third Party Reservation Release (THPR) bit is 1, then the reservation is released only if it was made by using the THP option (see subsection 8.3.13) by the requesting Initiator for the same SCSI bus device as specified in the Third Party Device ID field (Byte 01, Bits <03:01>).

Third Party ID - Byte 01, Bits <03:01>

If the THPR bit (Byte 01, Bit 04) is set, these bits specify the SCSI bus device code (ID) that identifies the LUN for which the Initiator reserved the MT02 Controller.

Flag - Byte 05, Bit 01

The Flag bit is meaningful only when the Link bit (bit 00 in Byte 05) is set. Therefore, if both the Flag and Link bits are set, an interrupt is requested for this command in a group of linked commands.

Link - Byte 05, Bit 00

The use of the Link bit is optional. If the Link bit is set, an automatic link is made to the next command at the successful completion of the current command from the Initiator. Status is returned for each command executed.

8.3.12 Request Sense 03

The **REQUEST SENSE** CDB, shown below, is used to obtain more detailed information, called Sense Information, after a command has been completed. Typically, a **REQUEST SENSE** command is issued after a previous command has been completed and a CHECK CONDITION status byte message has occurred (see subsection 7.3.3.3.1). A **REQUEST SENSE** command may be issued at any time by a diagnostic, device driver, or program, regardless of whether an error has or has not occurred, because significant sense information is only cleared upon receipt of an I/O- or access-type command.

Byte	Bit 07	06	05	04	03	02	01	00
00	0	0	0	0	0	0	1	1
01	0	0	0	0	0	0	0	0
02	0	0	0	0	0	0	0	0
03	0	0	0	0	0	0	0	0
04	Number of Requested Sense Bytes							
05	0	0	0	0	0	0	Flag	Link

The MT02 Controller will not disconnect from the Initiator while executing this command.

Number of Requested Sense Bytes - Byte 04

This byte contains the number of bytes of data the Initiator has allocated for the Sense Information. The count supplied determines the format of the returned sense data. The sense data can be returned in one of two supported sense byte formats: the Standard (non-extended) Sense Byte format and the Extended Sense Byte format. These formats are described in subsections 8.3.12.1 and 8.12.3.2.

A requested sense byte count of four or fewer bytes results in a transfer of four bytes in the Standard Sense Byte format.

A requested sense byte count of more than four bytes results in a data transfer of up to the requested number of sense bytes (but never more than the maximum number of sense bytes defined) of the Extended Sense Byte format.

Flag - Byte 05, Bit 01

The Flag bit is meaningful only when the Link bit (bit 00 in Byte 05) is set. Therefore, if both the Flag and Link bits are set, an interrupt is requested for this command in a group of linked commands.

Link - Byte 05, Bit 00

The use of the Link bit is optional. If the Link bit is set, an automatic link is made to the next command at the successful completion of the current command from the Initiator. Status is returned for each command executed.

8.3.12.1 Standard Sense Byte Format

The Standard Sense Byte format, shown below, is used when the requested number of bytes (Byte 04 of the **REQUEST SENSE** CDB) is less than or equal to four bytes.

Byte	Bit 07	06	05	04	03	02	01	00
00	VADD	ERCL			ERCD			
01	0	0	0	Sense Information (MSB)				
02	Sense Information							
03	Sense Information (LSB)							

Valid Address (VADD) - Byte 00, Bit 07

The Valid Address (VADD) bit indicates that the Sense Information Bytes (Bytes 01 through 03) contain valid device-type specifications. When the VADD bit is set to 1, the Sense Information Bytes specify the difference (residue) of the requested length to be accessed and the actual length accessed in data blocks.

Error Class (ERCL) - Byte 00, Bits <06:04>

The Error Class bits indicate the source of the error that occurred. Error Class codes are listed in Table 8-3. Error Classes 0 through 3 (hexadecimal) are valid for Standard Sense information.

Table 8-3. Standard Sense Error Classes

Bits 05	05	04	Error Class
0	0	0	DRIVE ERRORS
0	0	1	TARGET ERRORS
0	1	0	SYSTEM-RELATED ERRORS
0	1	1	VENDOR-UNIQUE ERROR CONDITIONS

Error Code (ERCD) - Byte 00, Bits <03:00>

The Error Code bits indicate the type of error that occurred. The hexadecimal Sense Error codes used in the Standard (non-extended) Sense Bytes for tape drive, Target, system-related, and vendor-unique errors are listed and described in Table 8-4.

Sense Information - Bytes 01 through 03

These bytes specify the difference (residue) of the requested and the actual Sense Information length transferred in data blocks.

Table 8-4. Standard Sense Error Class/Code Bytes

TAPE DRIVE ERRORS		
Hex Code	Error	Description
00	NO SENSE	The MT02 Controller detected no error during execution of the previous command.
04	DRIVE NOT READY	The tape drive is not powered up and ready.
09	MEDIA NOT LOADED	The media cartridge is not installed in the tape drive, as indicated by a tape drive status signal.
0A	INSUFFICIENT CAPACITY	There is insufficient space on the media to allow additional data from the Initiator to be accepted.
0B	DRIVE TIMEOUT	A timeout occurred during a tape drive operation.
TARGET ERRORS		
Hex Code	Error	Description
11	UNCORRECTABLE DATA ERROR	A block could not be written or read after 16 retry attempts.
14	BLOCK NOT FOUND	The block sequence is improper, or a block is missing.
16	DMA TIMEOUT ERROR	System activity reached a point at which DMA service for the MT02 Controller was suspended beyond the allowable timing limits, requiring one or more retry attempts.
17	WRITE PROTECTED	The media cartridge is write protected. The outstanding **WRITE** command has been aborted.

(continued on next page)

Table 8-4. Standard Sense Error Class/Code Bytes (continued)

TARGET ERRORS (continued)		
Hex Code	Error	Description
18	CORRECTABLE DATA CHECK	During read operations, a block had to be read two or more times. During write operations, a block had to be written more than once.
19	BAD BLOCK FOUND	A block cannot be read correctly after 16 retry attempts.
1C	FILE MARK DETECTED (Vendor-Unique)	A file mark block was encountered during a read operation. The outstanding **READ** and **VERIFY** commands are terminated and the tape is repositioned just after the file mark block.
1D	COMPARE ERROR (**VERIFY** only)	One or more bytes did not compare when the **VERIFY** command was issued.
SYSTEM-RELATED ERRORS		
Hex Code	Error	Description
20	INVALID COMMAND	The issued command cannot be implemented, or is not applicable.

(continued on next page)

Table 8-4. Standard Sense Error Class/Code Bytes (continued)

VENDOR-UNIQUE ERRORS		
Hex Code	Error	Description
30	UNIT ATTENTION	A Unit Attention condition occurred (see subsection 7.6.3). The removable media may have been changed, or the addressed LUN has been reset (by the BUS DEVICE RESET message), since the last command was issued to the addressed LUN. This error is reported the first time any command is issued after the condition is detected and the requested command is then not performed. This condition is cleared when the next I/O is issued by the same host adapter. UNIT ATTENTION is reported to all SCSI devices that subsequently issue a command to the Target.
31	COMMAND TIMEOUT	The command execution was not completed by the MT02 before a predetermined, command-specific time limit had expired.
33	APPEND ERROR	A write operation to the tape device was attempted before the end-of-media was reached.
34	READ END-OF-MEDIA	A read operation to the tape device was attempted past the end-of-media position.

8.3.12.2 Extended Sense Byte Format

The Extended Sense Byte format, shown below, is used when the requested number of bytes (Byte 04 of the **REQUEST SENSE** CDB) is greater than four bytes.

Byte	Bit 07	06	05	04	03	02	01	00
00	VADD	1	1	1	0	0	0	0
01	Segment Number							
02	FM	EOM	0	0	Sense Key			
03	Sense Information Byte (MSB)							
04	Sense Information Byte							
05	Sense Information Byte							
07	Additional Sense Length							
08	ERCL				ERCD			
09	Number of Recoverable Errors (MSB)							
10	Number of Recoverable Errors (LSB)							

Except for the operations that are initiated by the **COPY** command, the Additional Sense Length Bytes (Bytes 08 through 10) indicate the Standard Error Class and Error Code, and the number of recoverable errors (soft errors) that have occurred since the last **READ**, **WRITE**, or **VERIFY** command was executed. The Additional Sense Length Bytes field (Byte 07) is set to 3 for all commands except the **COPY** command. (For information about how the Additional Sense Length Bytes are used with the **COPY** command, see subsection 8.3.1.3.)

Valid Address (VADD) - Byte 00, Bit 07

The VADD bit indicates the Sense Information Bytes (bytes 03 through 06) contain valid device-type specifications. When the VADD bit is set, the Sense Information Bytes specify the difference (residue) of the requested length to be accessed and the actual length accessed in data blocks.

Segment Number - Byte 01

The Segment Number contains the current segment number if the Extended Sense information is in response to a **COPY** command. Up to 256 segments are supported.

File Mark (FM) - Byte 02, Bit 07

If the FM bit is set, the current command read a file mark.

End-of-Media (EOM) - Byte 02, Bit 06

If the EOM bit is set, an end-of-tape condition occurred.

Sense Key - Byte 02, Bits <03:00>

The Sense Key bits indicate status information about any errors detected during the operation. The errors are listed and defined in Table 8-5.

Sense Information Bytes - Bytes 03 through 06

These bytes specify the residual, or the difference between the requested and the actual data transfer.

Additional Sense Length - Byte 07

The Additional Sense Length byte specifies the number of Additional Sense Bytes. The Additional Sense Bytes contain command-specific data that further defines the nature of the CHECK CONDITION status. The Additional Sense Length byte is set to either 1 or 3. When it is 1, there is 1 additional sense byte that contains the standard error class and code. When the Additional Sense Length byte is 3, there are 3 additional sense bytes. The first byte contains the standard error class and code, the second byte contains the most significant soft error count byte, and the third byte contains the least significant soft error count byte. Typically, this field will be three. Under certain conditions (e.g., power up), this field will be 1 (no soft errors reported).

Table 8-5. Sense Key Error Codes

Hex Code	Error	Description
00	NO SENSE	There is no Sense Key information to be reported for the designated LUN. This code occurs for a successful command or for a command that was checked because the FM or EOM bit in the Extended Sense (Byte 02) was set to 1.
01	RECOVERABLE ERROR	The last command was completed successfully but with some recovery action performed.
02	NOT READY	The addressed LUN cannot be accessed. Operator intervention may be required.
03	MEDIA ERROR	The command terminated with a non-recoverable error condition which was probably caused by a flaw in the media or by an error in the recorded data.
04	HARDWARE ERROR	A non-recoverable hardware error was detected.
05	ILLEGAL REQUEST	There was an illegal parameter in the command or in the addi- tional parameters supplied as data for some commands.
06	UNIT ATTENTION	A Unit Attention condition occurred (see subsection 7.6.3). The removable media may have been changed, or the LUN has been reset (by the BUS DEVICE RESET message), since the last command was issued to the addressed LUN. This error is reported the first time any command is issued after the condition is detected and the requested command is then not performed. This condition is cleared when the next I/O is issued by the same host adapter. UNIT ATTENTION is reported to all SCSI devices that subsequently issue a command to the Target.
07	DATA PROTECT	A write operation was attempted on a write protected device either because the cartridge is in the SAFE state or the user panel write protect switch is engaged.

(continued on next page)

Table 8-5. Sense Key Error Codes (continued)

Hex Code	Error	Description
08	BLANK CHECK	The MT02 Controller encountered the end-of-recorded media (lack of data). This condition is not the same as the physical EOM.
09	VENDOR UNIQUE	A Vendor-Unique error condition occurred. The corresponding Error Class and Error Code are specified in Byte 08 of the Extended Sense Byte (see subsection 8.3.12.2).
0A	COPY ABORTED	A **COPY** command was aborted because an error condition was detected on the source or destination device.
0B	ABORTED COMMAND	The Target aborted the command. The Initiator may recover by trying the command again.
0C	RESERVED	
0D	VOLUME OVERFLOW	A buffered device has reached the end-of-media and data, which has not been written to tape, remains in the buffer. A **RECOVER BUFFERED DATA** command can be issued to read the unwritten data from the buffer.
OE	MISCOMPARE	Used by the **VERIFY** command to indicate that the source data did not match the data read from the tape.
0F	RESERVED	

Error Class (ERCL) - Byte 08, Bits <07:04>

The Error Class bits indicate the source of the error that occurred (see Table 8-3). Error Classes 0 through 3 (hexadecimal) are valid for the Extended Sense Information.

Error Code (ERCD) - Byte 08, Bits <03:00>

The Error Code bits indicate the type of error that occurred. The hexadecimal Sense Error Codes used in the Extended Sense Byte for the tape drive, Target, system-related, and vendor-unique errors are listed and described in Table 8-4.

Number of Recoverable Errors - Bytes 09 through 10

A recoverable error, also called a soft error, occurs when the MT02 Controller attempts to perform a read, write, or verify operation and, during that operation, it must perform a Retry. The MT02 attempts up to sixteen Retries. The Number of Recoverable Errors field indicates the accumulated number of recoverable errors that occurred during a series of either read, write, or verify operations. The value in this field is reset to 0 when a transition occurs from one of these operations to another. For example, if during the execution of a series of **READ** commands, recoverable errors occurred, when the Initiator issues a **REQUEST SENSE** command on the last read operation, the value in the Number of Recoverable Errors field indicates the number of recoverable errors that have occurred since the first **READ** command in the series was executed. In this example, once a **WRITE** or **VERIFY** command is issued, the number of recoverable errors count is reset to 0.

General media-related and drive-related error conditions that occur during MT02 Controller tape operations are listed and described in Table A-1 in Appendix A. Error conditions that occur during read, write, and verify operations are described separately in the descriptions of the **READ**, **WRITE**, and **VERIFY** commands.

8.3.13 Reserve Unit 16

The **RESERVE UNIT** CDB, shown below, causes the LUN to be reserved for exclusive use by the Initiator until that Initiator sends an appropriate **RELEASE UNIT** command. Since the MT02 Controller interfaces to only one LUN, whenever the LUN is reserved, the MT02 Controller is also reserved. If, while the MT02 Controller is reserved by an Initiator, a command is received from any other Initiator, the MT02 Controller sends a RESERVATION CONFLICT message and disconnects from the requesting Initiator. There is an exception to this rule when an Initiator reserves the controller for a second Initiator. (See the Third Party Reservation Option paragraph below.) In this case, though the second Initiator may give commands, the RELEASE UNIT must come from the original Initiator.

Byte	Bit 07	06	05	04	03	02	01	00
00	0	0	0	1	0	1	1	0
01	0	0	0	THP	Third Party ID			0
02	0	0	0	0	0	0	0	0
03	0	0	0	0	0	0	0	0
04	0	0	0	0	0	0	0	0
05	0	0	0	0	0	0	Flag	Link

The MT02 Controller will not disconnect from the Initiator while executing this command.

Third Party Reservation Option (THP) - Byte 01, Bit 04

The optional Third Party Reservation (THP) bit (Byte 01, Bit 04) allows an Initiator to reserve an LUN for another SCSI device. If the THP bit is set, an Initiator is allowed to reserve the MT02 Controller for the SCSI bus device specified in the Third Party ID field (Byte 01, Bits <03:00>). This option is intended for use in multiple-host adapter systems in which the **COPY** command is used. The MT02 Controller retains the reservation until it is released by the same Initiator that reserved it. Any attempt by another Initiator to obtain the MT02 Controller is ignored. The MT02 Controller does not disconnect from the SCSI bus during execution of this command. Any Target that uses the THP option must also use the Third Party Reservation Release (THPR) option (see subsection 8.3.11).

Third Party ID - Byte 01, Bits <03:01>

If the THP bit (Byte 01, Bit 04) is set, these bits specify the SCSI bus device ID for which the Initiator has reserved the MT02 Controller.

Flag - Byte 05, Bit 01

The Flag bit is meaningful only when the Link bit (bit 00 in Byte 05) is set. Therefore, if both the Flag and Link bits are set, an interrupt is requested for this command in a group of linked commands.

Link - Byte 05, Bit 00

The use of the Link bit is optional. If the Link bit is set, an automatic link is made to the next command at the successful completion of the current command from the Initiator. Status is returned for each command executed.

8.3.14 Rewind 01

The **REWIND** CDB, shown below, causes the selected tape drive to perform a rewind to the physical beginning-of-tape (BOT) or load point.

Byte	Bit 07	06	05	04	03	02	01	00
00	0	0	0	0	0	0	0	1
01	0	0	0	0	0	0	0	0
02	0	0	0	0	0	0	0	0
03	0	0	0	0	0	0	0	0
04	0	0	0	0	0	0	0	0
05	0	0	0	0	0	0	Flag	Link

If the disconnect function is enabled, the MT02 Controller may disconnect from the Initiator while executing this command.

Flag - Byte 05, Bit 01

The Flag bit is meaningful only when the Link bit (bit 00 in Byte 05) is set. Therefore, if both the Flag and Link bits are set, an interrupt is requested for this command in a group of linked commands.

Link - Byte 05, Bit 00

The use of the Link bit is optional. If the Link bit is set, an automatic link is made to the next command at the successful completion of the current command from the Initiator. Status is returned for each command executed.

8.3.15 Send Diagnostic 1D

The **SEND DIAGNOSTIC** CDB, shown below, causes a diagnostic function code to be sent to the Target. The only diagnostic function supported is self-test.

Byte	Bit 07	06	05	04	03	02	01	00
00	0	0	0	1	1	1	0	1
01	0	0	0	0	0	ST	0	0
02	0	0	0	0	0	0	0	0
03	0	0	0	0	0	0	0	0
04	0	0	0	0	0	0	0	0
05	0	0	0	0	0	0	Flag	Link

Self-Test (ST) - Byte 01, Bit 02

If the ST bit is set to 1, the Target is directed to complete its default self-test diagnostic routine. This test initiates a controller reset.

Flag - Byte 05, Bit 01

The Flag bit is meaningful only when the Link bit (bit 00 in Byte 05) is set. Therefore, if both the Flag and Link bits are set, an interrupt is requested for this command in a group of linked commands.

Link - Byte 05, Bit 00

The use of the Link bit is optional. If the Link bit is set, an automatic link is made to the next command at the successful completion of the current command from the Initiator. Status is returned for each command executed.

8.3.16 Space 11

The **SPACE** CDB, shown below, provides a variety of tape positioning functions which are determined by the Code Field and Count Bytes in the **SPACE** command CDB. Only forward spacing is allowed.

Byte	Bit 07	06	05	04	03	02	01	00
00	0	0	0	1	0	0	0	1
01	0	0	0	0	0	0	Code Field	
02	Count (MSB)							
03	Count							
04	Count (LSB)							
05	0	0	0	0	0	0	Flag	Link

If the disconnect function is enabled, the MT02 Controller may disconnect from the Initiator while executing this command.

Code Field - Byte 01, Bits <01:00>

The code field bits determine the tape positioning function to be executed. The codes are listed and described in Table 8-6.

Table 8-6. **SPACE** Command Code Field Bits

Bits 01	00	Description
0	0	Data Blocks
0	1	File Mark Blocks
1	0	Sequential File Mark Blocks
1	1	Physical End-of-Data

If a file mark is encountered during execution of a **SPACE** command that is spacing over data blocks, tape movement is stopped, with the media position placed after the file mark block. The MT02 Controller sends a CHECK CONDITION status code to the Initiator and sets the FM and VADD bits in the Extended Sense Bytes to 1. The Sense Information Bytes of the Extended Sense Bytes contain the number of data blocks not spaced over; the MT02 Controller sets the Sense Key to NO SENSE and the Sense Code to FILE MARK. The tape is positioned after the file mark.

NOTE

If a recoverable error occurs on a file mark block, the MT02 returns a Sense Key that only reflects that a file mark was detected.

When spacing over file mark blocks, the Count field specifies the number of file mark blocks required before stopping. If an end-of-media condition is encountered while spacing, the MT02 Controller sends a CHECK CONDITION status code to the Initiator, sets the EOM and VADD bits in Extended Sense Byte to 1, and sets the BLANK CHECK sense key code. The Information Bytes of the Extended Sense contain the number of file mark blocks not spaced over.

When spacing over Sequential file mark blocks, the Count bytes specify the number of consecutive file mark blocks required before stopping. The tape is positioned after the last file mark block of the sequence. If a data block is encountered during a space operation, the count is reset to its initial value and the space operation begins again with the media positioned after the data block. If a logical end-of-media condition is encountered (which indicates a lack of data on a tape cartridge) during a space operation, the MT02 Controller sends a CHECK CONDITION status code to the Initiator and sets the VADD bit in the Extended Sense Byte to 1. The MT02 Controller sets a BLANK CHECK error code in the Extended Sense. The Sense Information Bytes of the Extended Sense Bytes then contain the original specified number of file mark blocks.

When spacing to the physical end-of-data, the MT02 Controller ignores the Count field. Forward tape motion occurs until a blank tape region is detected, whereupon the tape is repositioned to allow future **WRITE** command operations to append data to the tape.

Count - Bytes 02 through 04

Only positive values are allowed in the Count Bytes (Bytes 02 through 04). A negative number (2's complement) results in a CHECK CONDITION status code and an ILLEGAL REQUEST Sense Key message in the Extended Sense Bytes. A zero value causes no tape motion.

Flag - Byte 05, Bit 01

The Flag bit is meaningful only when the Link bit (bit 00 in Byte 05) is set. Therefore, if both the Flag and Link bits are set, an interrupt is requested for this command in a group of linked commands.

Link - Byte 05, Bit 00

The use of the Link bit is optional. If the Link bit is set, an automatic link is made to the next command at the successful completion of the current command from the Initiator. Status is returned for each command executed.

8.3.17 Test Unit Ready 00

The **TEST UNIT READY** CDB, shown below, causes a test to be performed to ensure that the tape drive is powered-on and ready, and a tape cartridge is installed. This condition is indicated by a GOOD status code being returned for the command. If the tape drive is not ready, a **REQUEST SENSE** command can be issued to obtain detailed information on the reason the tape drive is not ready (unavailable).

	Bit							
Byte	07	06	05	04	03	02	01	00
00	0	0	0	0	0	0	0	0
01	0	0	0	0	0	0	0	0
02	0	0	0	0	0	0	0	0
03	0	0	0	0	0	0	0	0
04	0	0	0	0	0	0	0	0
05	0	0	0	0	0	0	Flag	Link

The MT02 Controller will not disconnect from the Initiator while executing this command.

If an auto-load operation is in progress, the MT02 Controller returns a BUSY status code.

Flag - Byte 05, Bit 01

The Flag bit is meaningful only when the Link bit (bit 00 in Byte 05) is set. Therefore, if both the Flag and Link bits are set, an interrupt is requested for this command in a group of linked commands.

Link - Byte 05, Bit 00

The use of the Link bit is optional. If the Link bit is set, an automatic link is made to the next command at the successful completion of the current command from the Initiator. Status is returned for each command executed.

8.3.18 Verify 13

The **VERIFY** CDB, shown below, causes one or more data blocks to be verified for correct data via a byte-for-byte compare, or it causes data blocks to be checked for correct cycle redundancy check (CRC) without needing a data transfer request from the Initiator.

Byte	Bit 07	06	05	04	03	02	01	00
00	0	0	0	1	0	0	1	1
01	0	0	0	0	0	0	BC	1
02	Number of Blocks to Verify (MSB)							
03	Number of Blocks to Verify							
04	Number of Blocks to Verify (LSB)							
05	0	IMED	0	0	0	0	Flag	Link

The Fixed Block Mode bit (Byte 01, bit 00) must be set, or an INVALID COMMAND error code message is generated.

If a file mark block is encountered during the execution of a **VERIFY** command, the MT02 Controller terminates the operation, positions the media after the file mark block, and sends a CHECK CONDITION status code to the Initiator. The MT02 Controller sets the VADD and FM bits in the Extended Sense Byte to 1. The Sense Information Bytes (in the Extended Sense Byte) contain the number of blocks not transferred from the Initiator plus the number of blocks remaining in the buffer of the Target.

If a MISCOMPARE (the source data did not match the data read from tape) Standard Sense Error Code is encountered, the MT02 Controller terminates the **VERIFY** command and sends a CHECK CONDITION status code to the Initiator.

If an unrecoverable error occurs during a verify operation, the MT02 Controller terminates the **VERIFY** command and sends a CHECK CONDITION status code. It sets the VADD bit in the Extended Sense Byte to 1. The Sense Information Bytes contain the Residual Count (total number of blocks not verified. Table 8-7 lists media-related or drive-related errors that can occur during a verify operation and their corresponding Sense Keys and Sense Code. (Sense Keys and Sense Codes are listed in their hexadecimal values.) General error conditions that occur during MT02 Controller tape operations are listed and described in Table A-1.

Table 8-7. **VERIFY** Command Error Conditions

Sense Key	Sense Code	Verify Error
BLANK CHECK (08)	READ EOM (34)	The MT02 Controller detected a logical EOM condition.
NO ERROR (00)	FILE MARK (1C)	The MT02 detected a file mark.
MISCOMPARE (0E)	MISCOMPARE (1D)	A data miscompare condition occurred during the verify operation.
MEDIA ERROR (03)	UNCORRECTABLE ERROR (11)	A CRC error occurred during the verify operation.
ILLEGAL REQUEST (05)	INVALID (20) COMMAND	The last command issued was a **WRITE** command, or it was a **VERIFY** CRC command following a **VERIFY** data command in the immediate mode.

The MT02 terminates the **VERIFY** command when the Number of Blocks to Verify is satisfied, when it encounters a file mark, or when it encounters the physical or logical end-of-media. When the MT02 completes the **VERIFY** command, it positions the tape at the end of the last block from which the data was verified or at the end of the file mark (if one was encountered).

If the MT02 is operating in the buffered mode, and the IMED bit is set to 1, any of the above error conditions may actually occur after the **VERIFY** command terminates. If this situation occurs, the MT02 reports a CHECK CONDITION status code on the next **VERIFY** command issued by the Initiator. The MT02 also sets the VADD bit in the Extended Sense Byte and sets the Sense Key appropriately. The Information Bytes (in the Extended Sense Byte) contain the Residual Count (which may be greater than the requested count if an error occurred on a previous operation).

If an additional **VERIFY** command is issued after a verify error occurs, the verify operation begins on the block that follows the block where the error occurred.

The Soft Error Count (the number of recoverable errors) is cleared on the first **VERIFY** command that is issued after a non-**VERIFY** command has been executed.

To ensure all data has been verified, issue the last **VERIFY** command (or the last **VERIFY** command with 0 bytes) with the IMED bit reset to 0.

If the disconnect function is enabled, the MT02 Controller may disconnect from the Initiator while executing this command.

Byte Compare (BC) - Byte 01, Bit 01

If the Byte Compare (BC) bit is set, data is transferred from the Initiator to the MT02 Controller as is done in a **WRITE** command. This data is compared byte-for-byte with the next data block from the present media position. If a MISCOMPARE occurs, the MT02 Controller terminates the **VERIFY** command with a CHECK CONDITION status code and the sets the Sense Key Error Code to MISCOMPARE. It also sets the VADD bit in the Extended Sense Byte to 1. The Sense Information Bytes contain the difference between the number of blocks to verify and the actual number of blocks successfully verified. If the BC bit is reset to 0, the MT02 Controller only performs a CRC media check. In this situation, no data is transferred between the Initiator and the Target.

Number of Blocks to Verify - Bytes 02 through 04

These bytes specify the number of blocks to verify. A zero value indicates no data is to be verified and the current position on the tape remains unchanged. This situation is not an error condition.

Immediate (IMED) - Byte 05, Bit 06

If the MT02 Controller is operating in the buffered mode (see subsection 8.3.5.1), when this vendor-unique bit is set to 1, the MT02 Controller operates in the streaming mode by immediately returning command completion status information to the Initiator. When the IMED bit is reset to 0, the MT02 Controller returns status information after completing execution of the command.

Flag - Byte 05, Bit 01

The Flag bit is meaningful only when the Link bit (bit 00 in Byte 05) is set. Therefore, if both the Flag and Link bits are set, an interrupt is requested for this command in a group of linked commands.

Link - Byte 05, Bit 00

The use of the Link bit is optional. If the Link bit is set, an automatic link is made to the next command at the successful completion of the current command from the Initiator. Status is returned for each command executed.

8.3.19 Write OA

The **WRITE** CDB, shown below, causes data to be transferred from the Initiator to the Target device and then to be written on the tape, starting at the current media position. The amount of data written is a multiple of the block length. The **WRITE** command specifies the number of blocks to be written.

Byte	Bit 07	06	05	04	03	02	01	00
00	0	0	0	0	1	0	1	0
01	0	0	0	0	0	0	0	1
02	Number Blocks to Transfer (MSB)							
03	Number of Blocks to Transfer							
04	Number of Blocks to Transfer (LSB)							
05	0	0	0	0	0	0	Flag	Link

During a write operation, the MT02 Controller allows data to be written only until pseudo EOM is detected. When the MT02 encounters this point, the write start threshold is ignored and data blocks are written to tape immediately.

The MT02 terminates the WRITE command with a CHECK CONDITION completion status to the Iniator. It also sets the EOM bit, NO SENSE (00) Sense Key, and INSUFFICIENT CAPACITY (0A) Error Class/Code, and sends the number of blocks not transferred from the Initiator into the Sense Information Bytes in the Extended Sense format. Data will be flushed from the cache and written onto tape, unless an error prevented further writing onto the tape.

The MT02 will issue only one pseudo EOM warning and it is the responsibility of the host to recognize that space available on the tape is limited (approximately 300 block spaces available to physical End-of-Tape).

After the MT02 notifies the host that a pseudo EOM condition has occurred, the host may continue to write to the tape until it encounters the physical end-of-tape (EOT). The Initiator can write data and file marks (volume labels) to terminate the tape. Attempts to write past the physical EOT result in a CHECK CONDITION completion status to the Initiator. Further, the controller sets the EOM bit, NO SENSE (00) Sense Key, and INSUFFICIENT CAPACITY (0A) Error Class/Code, and sends the number of blocks not transferred from the Initiator into the Sense Information Bytes in the Extended Sense format.

If an unrecoverable error occurs during a write operation, the MT02 Controller terminates the **WRITE** command and sends a CHECK CONDITION status code. It sets the VADD bit in the Extended Sense Byte to 1. The Sense Information Bytes contain the Residual Count (total number of blocks not written, i.e., the number of blocks not transferred from the Initiator plus the number of blocks remaining in the buffer of the Target). Table 8-8 lists media-related or drive-related errors that can occur during a write operation and their corresponding Sense Keys and Sense Code. (Sense Keys and Sense Codes are listed in their hexadecimal values.) General error conditions that occur during MT02 Controller tape operations are listed and described in Table A-1.

Table 8-8. **WRITE** Command Error Conditions

Sense Key	Sense Code	Verify Error
VOLUME OVERFLOW (0D)	INSUFFICIENT CAPACITY (0A)	The MT02 Controller encountered a physical end-of-tape. The **REQUEST SENSE** EOM bit will be set to 0.
ILLEGAL REQUEST (05)	APPEND ERROR (33)	An attempt to append data occurred when the tape was not at the end-of-recorded media.
EOM NO SENSE (00)	INSUFFICIENT CAPACITY (0A)	The MT02 Controller performed a normal write pseudo EOM operation (logical EOM). The **REQUEST SENSE** EOM bit will be set to 1.

If an additional **WRITE** command is issued after a write error occurs, the write operation begins on the block that follows the block where the error occurred.

The Soft Error Count (the number of recoverable errors) is cleared on the first **WRITE** command that is issued after a non-**WRITE** command has been executed.

The tape is erased automatically when the MT02 Controller writes on track 0.

The MT02 Controller does not automatically write a file mark on a tape if no additional data from the host is expected. The host should write a file mark as the last block of the tape to avoid any read-back problems that could occur if the MT02 Controller encounters error conditions during a tape operation on the last block.

If the MT02 Controller is operating in buffered mode (see subsection 8.3.5.3), it may report completion status before data is actually written to the tape. If this situation occurs, the MT02 will report any errors encountered when the Initiator issues the next command. If the MT02 is reporting an error that occurred on a previous command, it will return a CHECK CONDITION status code and set the VADD bit in the Extended Sense Byte to 1. The Sense Information Bytes will contain the residual count, which may be greater than the requested transfer count.

If the disconnect function is enabled, the MT02 Controller may disconnect from the Initiator while executing this command.

To ensure that all data that may still exist in the cache is written to tape, the host may cause a number of file marks to be written (including 0). When the **WRITE FILE MARK** command is completed, either all cache data is on the tape and a status code of GOOD STATUS has been issued, or a CHECK CONDITION status code has been issued. For additional information, see subsection 8.3.20, **WRITE FILE MARK** command).

Fixed Block Mode - Byte 01, Bit 00

If the Fixed Block Mode bit in the **WRITE** command packet is not set to 1, the MT02 Controller issues an INVALID COMMAND Error Code (see Table 8-4).

Number of Blocks to Transfer - Bytes 02 through 04

These bytes specify the number of blocks to be transferred. When the Number of Blocks to Transfer is 0, no data is transferred and the current position of the tape is not changed. This condition is not considered an error.

Flag - Byte 05, Bit 01

The Flag bit is meaningful only when the Link bit (Bit 00 in Byte 05) is set. Therefore, if both the Flag and Link bits are set, an Interrupt is requested for this command in a group of linked commands.

Link - Byte 05, Bit 00

The use of the Link bit is optional. If the Link bit is set, an automatic link is made to the next command at the successful completion of the current command from the Initiator. Status is returned for each command executed.

8.3.20 Write File Mark 10

The **WRITE FILE MARK** command causes one or more complete blocks of file marks to be written to tape, beginning at the logical current media position. The number of file mark blocks to be written is specified by the contents of the number of file marks (Bytes 02 through 04 of the CDB).

Byte	Bit 07	06	05	04	03	02	01	00
00	0	0	0	0	0	0	0	0
01	0	0	0	0	0	0	0	0
02	Number of File Marks (MSB)							
03	Number of File Marks							
04	Number of File Marks (LSB)							
05	0	IMED	0	0	0	0	Flag	Link

If the disconnect function is enabled, the MT02 Controller may disconnect from the Initiator while executing this command.

Number of File Marks - Bytes 02 through 04

These bytes specify the Number of file marks to be written on the addressed LUN. A zero value in these bytes indicates that no file mark blocks are to be written. If these bytes are equal to 0 and the IMED bit is equal to 0, the MT02 Controller purges the cache of all data. If the purge operation was successful, the MT02 Controller issues a COMMAND COMPLETE status code. If the purge operation was not successful, the MT02 Controller issues a CHECK CONDITION status code and the number of blocks remaining in the cache (the residue) is indicated in the Sense Information bytes of the **REQUEST SENSE** command (see subsection 8.3.12).

Immediate (IMED) - Byte 05, Bit 06

The Immediate bit is valid if the MT02 Controller is in cache buffering mode set by the BUFM bit in the **MODE SELECT** CDB (see subsection 8.3.5.1). If this vendor-unique bit (IMED bit) is set to 1, the MT02 Controller terminates the **WRITE FILE MARK** command immediately. If BUFM bit is reset to 0, the command terminates only after all buffered data and the file marks have been written to tape. The IMED bit is also used for Write Synchronization operations. When the Number of File Marks field (bytes 02 through 04) equals 0, and the IMED bit is reset to 0, the MT02 Controller writes to tape the contents of the cache before it terminates the **WRITE FILE MARK** command.

Flag - Byte 05, Bit 01

The Flag bit is meaningful only when the Link bit (Bit 00 in Byte 05) is set. Therefore, if both the Flag and Link Bits are set, an interrupt is requested for this command in a group of linked commands.

Link - Byte 05, Bit 00

The use of the Link bit is optional. If the Link bit is set, an automatic link is made to the next command at the successful completion of the current command from the Initiator. Status is returned for each command executed.

8.4 SCSI Group Code 6 Command Descriptions

This subsection provides detailed descriptions of the SCSI Group Code 6 commands, which are vendor-unique commands. Each SCSI command is described in a separate subsection.

The bytes in the CDB for Group Code 6 are command-dependent and are defined in the subsections for each individual Group Code 6 command.

8.4.1 Read Revision Level C1

The **READ REVISION LEVEL** CDB, shown below, returns to the host the current revision level of the PROM residing on the MT02 Controller.

	Bit							
Byte	07	06	05	04	03	02	01	00
00	1	1	0	0	0	0	0	1
01	0	0	0	0	0	0	0	0
02	0	0	0	0	0	0	0	0
03	0	0	0	0	0	0	0	0
04	0	0	0	0	0	0	0	0
05	0	0	0	0	0	0	0	0

8.4.1.1 Read Revision Level Data Format

During the Data In Phase of the **READ REVISION LEVEL** command, data is transferred in the following format:

Byte	Bit 07	06	05	04	03	02	01	00
00	0	1	0	0	0	0	0	1
01	0	0	1	1	0	0	0	0
02	0	0	1	1	1	0	0	0
03	Major Revision							
04	Engineering Revision							
05	Checksum							

Product Designation - Bytes 00 through 02

These bytes together form the ASCII Emulex product designation, which indicates the model number for the controller. For the MT02 Controller, these bytes are A08 (hexadecimal).

Major Revision - Byte 02

This byte indicates the major version number of the product.

Engineering Revision - Byte 03

If the product is a preliminary version, this byte indicates the Engineering revision of the product.

Checksum - Byte 05

This byte can be used to verify the validity of the PROM residing on the MT02 Controller.

Byte	Bit 07	06	05	04	03	02	01	00
00	VADD	1	1	1	0	0	0	0
01	Segment Number							
02FM	EOM	0	0			Sense Key		
03	Additional Sense Information Byte (MSB)							
04								
05								
06	Additional Sense Information Byte (LSB)							
07	Additional Sense Length							
08	Source Device Address Pointer*							
09	Destination Device Address Pointer*							
0A	Completion Status							
0B	Standard Sense Bytes							
0C								
0D								
0E								
0F	Completion Status							
10	Standard Sense Bytes							
11								
12								
13								

*Contain Completion Status and Standard Sense Bytes

BLANK

APPENDIX A
GENERAL ERROR CONDITIONS

A.1 Introduction

General media-related and drive-related error conditions that occur during MT02 Controller disk operations are listed and described in Table A-1.

Table A-1. General Error Conditions

Sense Key	Sense Code	Error Condition
HARDWARE ERROR (04)	DEVICE NOT READY (04)	The tape drive motor stalled.
ABORTED COMMAND (0B)	MEDIA NOT LOADED (09)	The tape cartridge was removed during the execution of the command.
MEDIA ERROR (03)	UNRECOVERABLE ERROR (11)	The MT02 Controller performed the maximum number of retries (16) on the block.
NOT READY (02)	MEDIA NOT LOADED (09)	The tape cartridge was not loaded before a command was issued.
UNIT ATTENTION (06)	UNIT ATTENTION (30)	The tape cartridge was removed and then installed before the execution of a command began.
RECOVERABLE ERROR (01)	CORRECTABLE DATA CHECK (18)	A recoverable error occurred during the execution of a command.

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APPENDIX B
MT02 FIRMWARE REVISIONS

Table B-1 lists the firmware release history for the MT02 Controller. It includes the firmware revision number, its release date, the corresponding manual revision level, and the main features of each revision. This list does not contain the correction history of the MT02 Controller firmware.

Table B-1. MT02 Controller Firmware Revisions

Manual Rev	Revision Number	Release Date	Features
Prelim	A08A	11/16/84	No new features.
	A08BX1	12/18/84	(1) The reposition time on track 0 was reduced to 4.3 seconds. (2) The time to detect a read EOM condition was reduced.
	A08BX2	12/22/84	The **COPY** command streams with the Adaptec external drive.
	A08BX3	1/7/85	No new features.
	A08BX4	1/14/85	No new features.
	A08BX5	1/21/85	No new features.
	A08CX1	2/4/85	(1) The MT02 supports a selectable erase ahead on track 0. (2) Preliminary MT02 support for QIC-11 with 4 or 9 track.
	A08CX2	2/8/85	No new features.
	A08CX3 (Rev D)	2/11/85	No new features.
	A08EX01	3/1/85	No new features.
	A08EX02	3/6/85	No new features.
	A08EX03	3/7/85	No new features.

(continued on next page)

Table B-1. MT02 Controller Firmware Revisions (continued)

Manual Rev	Revision Number	Release Date	Features
Prelim	A08FX01	3/22/85	(1) The MT02 fully supports QIC-11 except for 4-track write mode. (2) An unload operation after the cartridge is already loaded no longer produces an error condition. (3) The EOT option on the **UNLOAD** command no longer requires that the RET bit be set. (4) The residue on the **SPACE** command with sequential file marks selected has been defined more precisely than the definition in the SCSI standard. (5) The IMED bit can be used to maintain streaming on a **VERIFY** command with the CRC check only option selected. (6) The MT02 includes a new EOM detection method to allow for bad erase characteristics on some tape drives using DC600A cartridges.
	A08FX02	3/26/85	No new features.
	A08FX03	4/1/85	If a new cartridge is inserted in the tape drive, the MT02 may return a UNIT ATTENTION sense code on a **LOAD** command.
	A08FX04	4/4/85	No new features.
	A08FX05	4/9/95	No new features.
	A08FX06	4/25/85	The MT02 supports a new vendor-unique SCSI command: **READ REVISION LEVEL**. This command returns the firmware revision level to the Initiator.

(continued on next page)

Table B-1. MT02 Controller Firmware Revisions (continued)

Manual Rev	Revision Number	Release Date	Features
Prelim	A08FX07	5/2/85	During any load operation, the **TEST DRIVE READY** and **MODE SENSE** commands may return a TARGET BUSY status code.
	A08FX08	5/8/85	No new features.
A	A08FX09 (Rev F)	5/24/85	No new features.
	A08GX06	12/3/85	Bug fixes.
B	A08GX07 (Rev G)	12/5/85	No new features.
C	(Rev H)	3/21/86	Kennedy 6500 support added.
D	(Rev J)	6/10/86	Bugs fixed.

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APPENDIX C
SERVICE

C.1 Overview

The installation of the MT02 controller, when used with the recommended devices, should run smoothly and problem-free. The diagnostic procedures described in this manual are intended to help you identify and resolve any problems you may encounter. However, because of the wide variety of host adapters, disk drives and other devices to which the controller could be connected, diagnostic procedures cannot be specific or all-inclusive. The following subsections explain how to obtain technical assistance or service for problems you cannot resolve.

C.2 Problem Identification

The self-test, described in Section Four, diagnoses problems within the controller itself. It does not diagnose problems with the host adapter, disk drive, or other devices to which the controller is connected.

If the controller does not pass the self-test when it is connected to the other devices in your system, remove the devices and try the self-test again. If the controller passes the self-test, the problem may be elsewhere in the system. See directions for obtaining help from Emulex's technical support personnel in the subsection on Technical Assistance.

If the controller does not pass the self-test when it is tested apart from the devices, it may be defective and should be returned to the factory for replacement. See directions for returning the unit in the subsection on Service.

C.3 Technical Assistance

If the MT02 Controller passed the self-test, but you believe it is not performing as expected, you can obtain assistance from Emulex's technical support personnel. The SCSI Product Performance Report (see last two pages of Appendix C) allows you to gather all the required information. Complete the form and mail it to Emulex at the address on the form. A technical support representative will contact you within five days of receipt of the form.

Note that this form is required in order for you to receive technical assistance regarding your MT02 Controller. Please do not attempt to contact Technical Support by any other means. (If you have not heard from Emulex after five days, you may call in to check the status of your report.)

It is suggested that you use a photocopy of this form, so that the form will be available should you need to use it again.

C.4 Service

The components of your Emulex MT02 Controller have been designed to give years of trouble-free service, and they were thoroughly tested before leaving the factory.

If one of the diagnostic procedures described in this manual indicates that a component is not working properly, the controller must be returned to the factory, or to an Emulex authorized repair center, for service. Emulex products are not designed to be repaired in the field.

Before returning the component to Emulex, whether the product is or is not under warranty, you must contact Emulex's Repair Center for instructions and a Return Materials Authorization (RMA) number.

DO NOT RETURN AN MT02 CONTROLLER TO EMULEX WITHOUT AUTHORIZATION. A controller returned for service without an authorization will be returned to the owner at the owner's expense.

In the continental United States, Alaska, and Hawaii contact:

Emulex Repair Center
3545 Harbor Boulevard
Costa Mesa, CA 92626
(714) 662-5600 TWX 910-595-2521

Outside the United States, contact the distributor from whom the MT02 Controller was initially purchased.

SCSI PRODUCT PERFORMANCE REPORT

Please provide all information requested.

CUSTOMER INFORMATION

Name _____ Phone No. _____ Ext. _____
Position/Title _____
Company Name _____
Address _____
City _____ State _____ Zip _____

PRODUCT INFORMATION

EMULEX Product in Use: MD _____ MT _____ IB _____ UC _____
Top Assembly Number _____
Serial Number _____ Date of Purchase _____
Purchased From _____ Sales Engineer _____

PERIPHERAL INFORMATION

DISK

Manufacturer _____
Model Number _____
Interface: ST506 _____ ESDI _____
Geometry: No. of Cylinders _____
Number of Heads _____ Sectors _____
Number of Bytes/Track _____
Number of Drives _____

TAPE

Drive Interface: QIC36 _____ QIC44 _____
Media Interface: QIC11 _____ QIC24 _____
QIC120 _____ QIC150 _____

Tape Type: 300 _____ 450 _____ 600 _____
Tape Manufacturer: 3M _____ DEI _____
DYSAN _____ CARTREX _____ SCOTCH _____

SYSTEM CONFIGURATION

Bus Type: IBM _____ DEC _____ VME _____
MULTIBUS _____ OTHER _____
Software: Diagnostics _____
Utilities _____

Amount of Memory _____
Host Adapter _____
Formatter _____
Operating System _____

GRAPHIC REPRESENTATION OF YOUR SYSTEM

PROBLEM DESCRIPTION

Give a complete description of the problem you are encountering. Provide details of the command packet and/or test loop/routine that you are using to troubleshoot the problem. Include a copy of the program(s) that demonstrates the problem on either hard copy or magnetic media (DOS or FILES 11 format).

Please mail the completed form to:

EMULEX CORPORATION
National Technical Support
3545 Harbor Boulevard
Costa Mesa, CA 92626

Attn: SCSI Support

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