

CHECK DRAFT

MICROMEMORY 7405  
ADD-ON MEMORY SYSTEM

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**ELECTRONIC MEMORIES & MAGNETICS CORPORATION**

12621 Chadron Avenue, Hawthorne, California 90250 / Telephone: (213) 644-9881

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FOREWORD

Section Title

This manual contains information required to install, operate, and maintain the MICROMEMORY 7405 Add-on Memory System, part number 929494, manufactured by Electronic Memories and Magnetics Corporation, Hawthorne, California.

This 7405 Memory System is self-contained, with memory power supply and interface electronics for complete compatibility with PDP-11 Computer Systems manufactured by Digital Equipment Corporation, Maynard, Massachusetts.

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SECTION I

GENERAL DESCRIPTION

1-1. GENERAL

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1-2. The MICROMEMORY 7405 Memory System consists of an Electronic Memories standard chassis containing one to four 32K x 16\* MICROMEMORY 3000QD Cards, a Power Supply and a special UNIBUS-adaptable Interface Card. Switches on the Interface Card can be set to designate the Memory System for operation within an address block recognizable by the Computer.

1-3. The Memory System is modularly organized in 32K sub-blocks with each Memory Card constituting one sub-block. Thus, the System can be populated in corresponding increments. Table 1-1 indicates System versions based on number of Memory Cards and System capacity. Figure 1-1 illustrates Card and Power Supply locations.

1-4. POWER SUPPLY

1-5. The Power Supply is capable of supplying all necessary dc operating voltages for a full-populated Memory Module. The Power Supply also provides 115 vac to the cooling fans located within the Memory Module. For detailed description of Power Supply see Technical Manual TM929219.

1-6. MEMORY CARDS

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1-7. Each Memory Card is a complete 32K x 16 (or 18) memory subsystem on a single printed wiring board, including semiconductor memory array and support electronics. Refer to Technical Manual TM929162 for description of the Memory Card.

1-8. INTERFACE CARD

1-9. The Interface Card is a buffer/controller unit installed between the PDP-11 UNIBUS and the Memory Cards that constitute the Memory System.

Footnote

\*May be 18-bit words when parity option is included.

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1-10. CAPACITY      First Line of Text or Table Title

1-11. The Interface Card can provide buffering and control for up to 124K 18-bit words (including two parity bits) or 248K 9-bit bytes, depending on operating mode.

1-12. MODES OF OPERATION

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1-13. The Interface Card can accommodate the Memory System for operation in the following modes:

- Read/Restore Word,
- Clear/Write Word,
- Exchange Word (Read/Modify/Write)
- Read/Restore Either Byte, Clear/Write Other Bytes

1-14. ACCESS TIME      Vertical Illustration

1-15. Access and cycle times are as follows:

- Access Time for Full Page
- Access Time with parity
- Cycle Time

1-16. SYSTEM OPTION

1-17. The Memory System can optionally include provisions for checking and storing two parity bits. When this option is included, each Memory Card must include two extra bit storage capacity. Card capacity must be 32K x 18.

1-18. SYSTEM SPECIFICATIONS

1-19. A summary of Memory System specifications is contained in Table 1-2. For details of Memory Card specifications, see Technical Manual TM928647.

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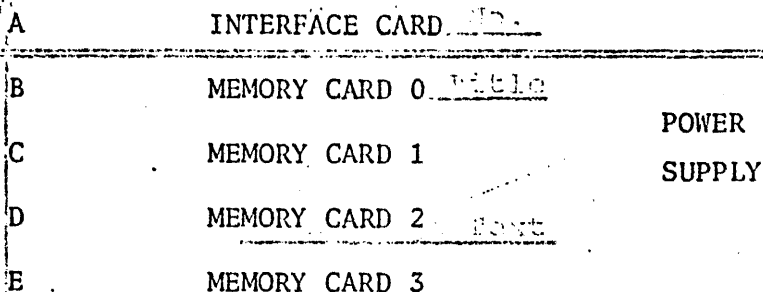


Figure 1-1. Memory Module Component Location

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Table 1-1. Memory System Version Chart

VERSION	CARD LOCATION *				
	A	B	C	D	E
Chassis with I/O and Power Supply	I				
128K x 18 bits	I	M	M	M	M
96K x 18 bits	I	M	M	M	
64K x 18 bits	I	M	M		
32K x 18 bits	I	M			

NOTE:

I = Interface Card P/N 929402-002

M = Memory Card P/N 928647-305

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Table 1-2. System Specifications

ITEM	Section Title	SPECIFICATION
Type of Memory		Random Access NMOS
Capacity per Memory Card:	<u>Drop Page Text</u>	
Without Parity		32,768 16-bit Words
With Parity		32,768 18-bit Words
Modes of Operation		Read/Restore
		Clear/Write
		Exchange Word (R/M/W)
	Width for P	Read/Restore Either Byte,
	Vertical Ill	Clear/Write Other Byte
Timing:	or	
Read Cycle	Height for Full Page	
Write Cycle	Landscape Illustration	
Exchange Cycle		
Access		
Access (with parity)		
Logic Levels:	or Full Page	
ZERO	Vertical Illustration	+2.5 to +5.0 volts
ONE	or	0.0 to +0.5 volts
AC Power Requirement	Page	
Voltage	Illustration	115 volts ±10%
Current (amps)		8 amps

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SECTION II

INSTALLATION AND OPERATION

- 2-1. INSTALLATION Drop Page Text
- 2-2. CHASSIS
- 2-3. Install Memory Module (Chassis) in EIA standard 19-inch rack-type cabinet as close as possible to the parent computer (PDP-11). Secure the chassis at the front panel, using four 5/8-inch 10-32 pan-head screws.
- 2-4. MEMORY CARD ASSEMBLIES Width for Full Page
- 2-5. As required install Memory Card Assemblies in card slots B thru E. Cards must be inserted with component-side down. If fewer than four Cards are included in Memory System, populate slots in alphabetic order (B thru E). Landscape Illustration
- 2-6. INTERFACE CARD
- 2-7. Preliminary Procedure
- 2-8. Prior to installing Interface Card in slot A, this Card must be adjusted for operation within the user-assigned memory range (Memory block). Also, if parity option is included, the assigned parity register address must be set. To accomplish this, set switches S1 and S2 as required per Tables 2-1 and 2-2.
- 2-9. Procedure Width for Full Page  
Landscape Illustration
- 2-10.
  - a. Turn off computer dc power.
  - b. Connect UNIBUS cable to any available UNIBUS slot in the computer mainframe or extension chassis.
  - c. Connect other end of UNIBUS cable to connectors J3 and J4 on the Interface Card. The A section of cable to J4; the B section to J3. (Interface Card connectors are keyed to prevent incorrect cable installation.)
  - d. If Memory Module is to be placed within a chain of peripheral devices, connect the adjacent peripheral device to Card connectors J5 and J6 using another UNIBUS cable; otherwise, go to step E.

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e. If Memory Module is the only device connected to the computer, or if it is the last device in a chain of devices, install a DEC M-930 UNIBUS terminator block in connectors J5 and J6.

f. See Figure 2-1 to verify connections.

g. Install Interface Card in Memory Module slot A, component side down.

h. Plug Memory Module AC line cord into suitable AC outlet. AC line power available must be 800 VA minimum.

2-11. MEMORY VERIFICATION

2-12. Verify Memory Module operation with diagnostic routing in Computer Reference Manual.

2-13. OPERATION width for Full Page

2-14. Except for Power Supply AC turn-on, the Memory Module is operated automatically by the parent computer. See System Power Supply Technical Manual TM929219 for details of Power Supply operation.

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Table 2-1. Starting Address Select Chart

STARTING ADDRESS	Section No.		S2 SWITCH POSITION *				
	OCTAL	BINARY	S2-5	S2-4	S2-3	S2-2	S2-1
000000	0	0	0	0	0	0	0
004000	4096	1	1	1	1	1	1
010000	8182	1	1	1	1	0	0
014000	12288	1	1	1	0	1	1
020000	16384	1	1	1	0	0	0
024000	20480	1	1	0	1	1	1
030000	24576	1	1	0	1	0	0
034000	28672	1	1	0	0	1	1
040000	32768	1	1	0	0	0	0
044000	36864	1	0	1	1	1	1
050000	40960	1	0	1	1	0	0
054000	45066	1	0	1	0	1	1
060000	49152	1	0	1	0	0	0
064000	53248	1	0	0	1	1	1
070000	57344	1	0	0	1	0	0
074000	61444	1	0	0	0	1	1
100000	65536	1	0	0	0	0	0
104000	69632	0	1	1	1	1	1
110000	73728	0	1	1	1	0	0
114000	77824	0	1	1	0	1	1
120000	81920	0	1	1	0	0	0
124000	86016	0	1	0	1	1	1
130000	90112	0	1	0	1	0	0
134000	94208	0	1	0	0	0	1

NOTE: 0 = Switch closed; 1 = Switch open

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Table 2-2. Parity Register Address Selection

PARITY REGISTER ADDRESS	S1 SWITCH POSITION *			
	S1-4	S1-3	S1-2	S1-1
772100	0	0	0	0
772102	0	0	0	1
772104	0	0	1	0
772106	0	0	1	1
772110	0	1	0	0
772112	0	1	0	1
772114	0	1	1	0
772116	0	1	1	1
772120	1	0	0	0
772122	1	0	0	1
772124	1	0	1	0
772126	1	0	1	1
772130	1	1	0	0
772132	1	1	0	1
772134	1	1	1	0
772136	1	1	1	1

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NOTE: \* 0 = Switch closed; 1 = Switch open

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SECTION III

THEORY OF OPERATION

3-1. GENERAL

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3-2. This section describes operating theory of the MICROMEMORY 7405 Memory System. Descriptions are keyed to appropriate figures in this section and the Interface schematic drawing in Section V. Detailed functional descriptions of the Memory Card and Power Supply are contained in Technical Manuals TM944709 and TM929219 respectively.

3-3. MEMORY SYSTEM

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3-4. The Memory System (Figure 3-1) consists of up to four 32K x 16 Memory Cards and an Interface Card that adapts the System to the PDP-11 UNIBUS. The System can optionally include provisions for parity processing.

3-5. ADDRESSING

3-6. It requires 16 bits to address 124K-words of memory. The PDP-11 generates 17 bits. Of these, Address Bit A00 is used as a control signal, Bits A01 thru A15 are used to access a selected Memory Card, and Bits A13 thru A17 are used to select the Memory Card for access. The Computer address scheme is based on the 17-bit word; however, in the Memory System, Address Bit A00 is excluded from the Memory internal addressing scheme; but, in conjunction with control signals C0 and C1 control the operating mode of the Memory System. Figure 3-2 illustrates Address Word configuration: external and internal.

EXTERNAL	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTERNAL	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	

32K CARD INTERNAL ADDRESS

CARD SELECT

CONTROL SIGNAL

Figure 3-2. Address Word Configuration

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3-7. MEMORY CARD SELECT Last Line of Text or Table Title

3-8. Memory Cards are selected by External Address Bits A13 thru A17 decoded by the Card Select circuit in the Interface Card. This circuit generates a specific Cycle Initiate signal (RP) which starts a memory cycle in the selected Card. The circuit can be set by switch S2 to start generating Cycle Initiate signals at a certain address, thus, setting the starting address of the Memory System. These starting addresses occur in 4K increments between 0 and 94208 (internal address). The upper limit of the address block is determined by the number of Memory Cards in the System. The maximum address from the Computer is 126,956 (24K). (See Table 2-1 for starting address versus switch setting. Note that the octal address is based on the Computer (17-bit) address.)

3-9. MODE CONTROL Width for Full Page

3-10. Operating mode is determined by the state of control signals A00, C0 and C1. These modes are designated Word Mode and Byte Mode, with a sub-mode of the Word Mode being Exchange Mode. Mode control to the Memory Cards is a function of Byte Control Level signals 1 and 2 (BCL1, BCL2). Table 3-1 indicates control versus mode.

Table 3-1. Mode Control

Height for MODE 1 Page Vertical Illustration or Width for Full Page Landscape Illustration	CONTROL			BYTE CONTROL	
	C1	C0	A00	BCL1	BCL2
WORD	0	0	0	1	0
READ	0	0	1	0	1
WRITE	0	1	x	0	0
EXCHANGE	1	x	x	1	1

NOTE: 1. 0 = low; 1 = high  
 2. Exchange = Read followed by Write in Word Mode

3-11. INTERFACE CARD DETAILS

3-12. The Interface Card is essentially a buffer/controller with data and address receivers/drivers, Card Select, Parity Control, Mode Control, and Timing and Control Circuitry. Last Line of Text

3-13. DATA/ADDRESS ROUTING Line of Text or Table Title

3-14. Data and Address are conveyed to/from Memory by receivers/drivers in the Interface Card. However, Address Bits A13 thru A17 (internal A12 thru A16) are processed by Memory Card Select and Starting Address Control (See Figure 3-3) to select a Cycle Initiate signal RP00 thru RP03.

3-15. Memory Card Select and Starting Address Control

3-16. Memory Card Select and Starting Address Logic consists of a binary adder U48, a 1/8 decoder U54, switch S2(1-4) and peripheral circuitry. Switch S2 is set to the complement of the desired starting address. When the starting address occurs, the complement added to it always equals 0000. The most significant bits E4, E3 are applied to the decoder, which generates RP00 to select Memory Card 0. Subsequent addresses above the starting address add to the switch-set input and because only the most significant output bits are used, RP changes in increments of 32K above the starting address. (See Table 2-1 for starting address versus switch settings.)

3-17. PARITY CONTROL (Optional)

3-18. Parity Control provides incoming data with a parity bit and checks outgoing data for correct parity. The circuit includes an address select circuit that can be set by switch S1(1-4) to activate parity when instructed by the Computer. The Computer instruction is conveyed by Address Bits A01 thru A12 (internal A00 thru A11) applied to Parity Control. Low order Bits 01 thru 04 (internal A00 thru A03) are compared to switch S1 settings to provide the parity select control for the Parity-Word Multiplexer (U24, U25) and Register (U35, U36). See Illustration

3-19. In event of a parity error in a Read word, the Parity Generator/Checker (U17, U18) generates a parity error flag, PB, which is sent to the Computer. In response the Computer executes a trap to location 114 or 116. (See PDP-11 Processor Handbook for details of Computer Operation.)

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SECTION IV.

MAINTENANCE

4-1. PREVENTIVE MAINTENANCE

4-2. Preventive maintenance consists of inspection, and cleaning as required. However, only cleaning of air filter should be done periodically. Inspection and cleaning of major components (circuit board assemblies) should be done only when the system MUST be shut down for corrective maintenance, and then, only on a circuit board that MUST be removed.

4-3. INSPECTION AND CLEANING

4-4. System Air Filter

4-5. Dependent on atmospheric dust conditions, and as periodically required, inspect, remove, and clean system air filter as follows:

- a. Remove System front panel.
- b. Hold panel with dirty side down, and tap gently to loosen accumulated dust particles.
- c. Remove dust with vacuum cleaner, or by immersing in clean water.

d. As applicable, shake out water, dry panel and filter, and reinstall.

4-6. Baseplate Connectors

4-7. Only when Memory Card MUST be removed, inspect and clean baseplate connectors as required:

- a. Saturate Memory Card contacts with contact cleaner.
- b. Insert Memory Card into and remove from baseplate connector.
- c. Wipe Memory Card connector clean with soft clean cloth.

CAUTION

Inserting anything into baseplate connector except PCB could damage contact surface or change contact pressure. Never insert anything but Memory Card into baseplate connector.

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4-8. CORRECTIVE MAINTENANCE Line of Text or Table Title

4-9. Corrective maintenance is herein limited to System troubleshooting, the goal of which is to isolate faults to a defective Memory Card, the Interface Card or the Power Supply. Defects related to data and address can be isolated to the data and address paths between Computer and Memory-Card memory matrix using a DEC PDP-11 diagnostic (such as DZQMB). However, to correlate Computer octal readouts with Memory Card address decoding, do the following:

- a. Construct two tables in the forms illustrated in Figure 4-1.
- b. For a given Computer octal readout, fill in the appropriate spaces in Table A.
- c. Insert binary equivalent of octal readout in Table A.
- d. Transfer binary equivalent to Table B according to Memory-Card interval bit positions.
- e. Refer to Memory Card Technical Manual TM929162, Section III for theory of address decoding.

f. Note that the decoding of Interval Address bits 15 and 16 represent RP Select: each RP selected selects a Memory Card. (See Theory, Section III.) (Figure 4-2 illustrates relationship among external Address (A), Address Input (AI) and Memory Address (MA).)

4-10. Computer designated data bits (BD) also do not correspond exactly to Memory System interval data bits. To correlate Computer to Memory data bits refer to Table 4-1. Page

4-11. MEMORY CARD SELECT

4-12. The Memory Card is selected (addressed) by UNIBUS Address Bits A17 and A16. Table 4-2 designates UNIBUS Address Bit configurations for selecting each Memory Card Slot. To use this chart, subtract the starting address of the Memory System from the UNIBUS address. The resulting binary states of Address Bits A17 and A16 correlate to the selected card slot.

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4-13. INTERFACE CARD TROUBLESHOOTING      Text or Table Title

4-14. Malfunctions common to all Memory Cards are most likely traceable to the Interface Card. All data and address bits are routed through this Card; thus, related buffers can be suspected in event of data and address failures. Similarly, the Parity circuit (when included) services all Memory Cards.

4-15. Card-selection problems can be isolated by interchanging Memory Cards. Continued malfunction of the apparently defective Memory Card indicates this Card is defective. If the substituted Card fails, the Interface Card is defective.

4-16. MEMORY CARD MODIFICATION

4-17. To accommodate the PDP-11 Computer System, the MICROMEMORY 3000QD Memory Cards are modified as follows:

Ref. TM929162:

Page 2-10. P1-70, Was AI15      Full Page

Landscape      AI14      Illustration

P1-64, Was AI14

Is RDAG

Section V, Schematic 929668

Sheet 1. P1-70; P1-64. Same as P2-10 above

Height for Full Page

Sheet 7. Zone A8, Was AI15 to 70

Vertical Illustration

Is RDAG to 64

or

Sheet 8. Zone C8, Was AI14 to 64

Width for Full Page

Is AI14 to 70

Landscape Illustration

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Table A. Octal to Binary Conversion

OCTAL READOUT	BINARY EQUIVALENT																
INT ADD BITS	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MEM CARD INT BITS			2	0	1	8	11	14	7	10	9	3	12	13	4	5	6

Table B. Binary Reorganization

MEM CARD INT BITS	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BINARY (From Table A)															

Figure 4-1. Computer Octal to Memory-Card Binary Conversion Chart

Table 4-1. Data Bit Correlation

BUS DATA BITS	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
DI/DO BITS	17	2	16	15	14	13	12	11	10	9	7	6	5	4	3	8	1	0
PARITY	P2	P1																

Table 4-2. Memory Card Select Chart

UNIBUS * ADDRESS BITS		SELECTED CARD SLOT
A17	A16	
0	0	B
0	1	C
1	0	D
1	1	E
A116	A115	
MEMORY INTERNAL ADDRESS BITS		

Note:

- 1.\* 1 = Low; 0 = High
- 2.\*\* 1 = High; 0 = Low

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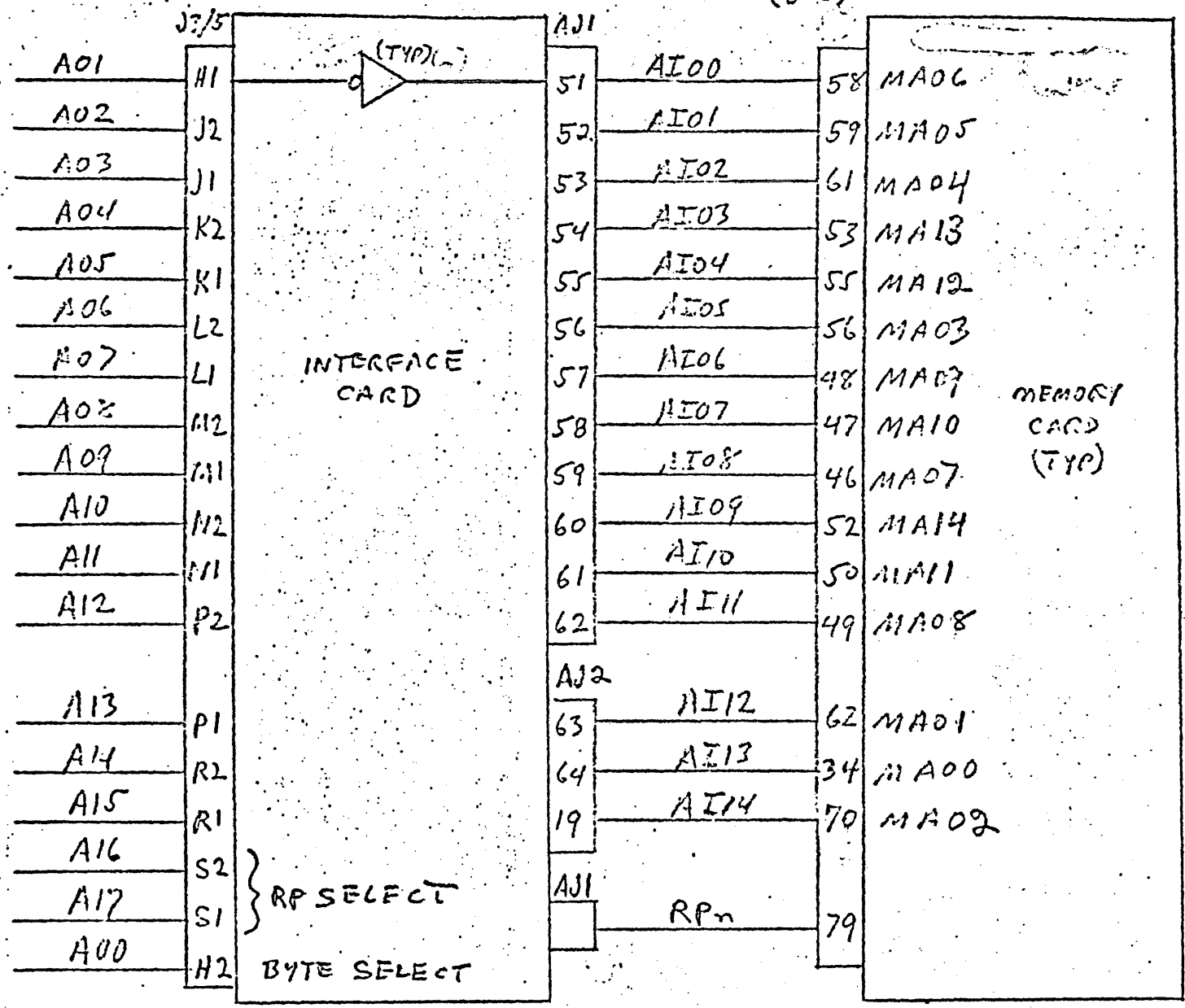


Figure 4-2. Address Routing and Designation.

4A

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SECTION V

Sec DRAWINGS

5-1. GENERAL

Drop Page Text

5-2. Drawings contained in this section are listed in Table 5-1.

Table 5-1. Drawings

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DRAWINGS

NUMBER

PAGE

Vertical Illustration

Interface Card Assembly      or      929402

Parts List      Height for PL929402-002

Schematic      Landscape Illustration      929405

NOTE: Power Supply Manual is TM929219

Memory Card Manual is TM929162

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or

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Landscape Illustration

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1.0 SCOPE

This document defines MICRO 7405 Memory Modules ( )K x 18 Bits with power supply. The system is a PDP11 compatible add on, designed with the parity option.

PART NUMBER	REV	TITLE	CARD TYPE	CARD LOCATION CHART				
				A	B	C	D	E
929490-001	A	Micro 7405 W/Chassis	929402-004	X	-	-	-	-
-002	A	Micro 7405 64K x 18 Bits W/Parity Board	927390-007 929402-004	X	X	X	X	X
-003	A	Micro 7405 48K x 18 Bits W/Parity Board	927390-007 929402-004	X	X	X	X	
-004	A	Micro 7405 32K x 18 Bits W/Parity Board	927390-007 929402-004	X	X	X		
-005	A	Micro 7405 16K x 18 Bits W/Parity Board	927390-007 929402-004	X	X			
-006	A	Micro 7405 64K x 18 Bits W/Parity Board	927390-007 929402-008	X	X	X	X	X
-007	A	Micro 7405 48K x 18 Bits W/Parity Board	927390-007 929402-008	X	X	X	X	
-008	A	Micro 7405 32K x 18 W/Parity Board	927390-007 929402-008	X	X	X		
929490-009	A	Micro 7405 16K x 18 W/Parity Board	927390-007 929402-008	X	X			

1.1

1.2

1.3 See sheet 3 of this document for parts list.

2.0 ASSEMBLY INSTRUCTIONS

2.1 Assemble per Memory Module Assembly instruction drawing 923670.

2.2 Install card assemblies per card location chart.

2.3 Mark and install nameplate per 923670.

2.4 Install label per 923670 unless otherwise specified by sales order.

3.0 TEST INSTRUCTIONS

3.1 The basic test criteria is specified in the Product Specification PS928321

	SIZE	CODE IDENT NO.	DWG NO.
	A	16224	929490
	SCALE	REV.	SHEET
		C	2

ITEM NO.	PART NUMBER	DESCRIPTION (SPEC/SOURCE)	001	002	003	004	005	006	007	008	009
2	923675-A02	Chassis	1	1	1	1	1	1	1	1	1
3	927390-007	Memory Assy (16K x 18)	-	4	3	2	1	4	3	2	1
3	929402-004	I/O Parity Board	1	1	1	1	1	-	-	-	-
4	912602-1	Nameplate	1	1	1	1	1	1	1	1	1
5	944160-001	Rear Panel Assembly	1	1	1	1	1	1	1	1	1
6	PS929219-002	Power Supply (115V)	1	1	1	1	1	1	1	1	1
7	928335-001	Front Panel Assembly	1	1	1	1	1	1	1	1	1
8	928083-002	Connector Bracket Assy	1	1	1	1	1	1	1	1	1
9	NC-832	Capnut (Blk) (Weckesser)	4	4	4	4	4	4	4	4	4
10	923645-001	Label	1	1	1	1	1	1	1	1	1
12	925601-001	Caution Decal	1	1	1	1	1	1	1	1	1
13	929402-008	I/O Parity Board with Auto Restart	-	-	-	-	-	1	1	1	1

*NOTE: 923755-A01 IS AN ACCEPTABLE ALTERNATE FOR 944160-001 UNTIL EXISTING INVENTORY IS USED UP.*

4.0 SHIPPING INSTRUCTIONS

- 4.1
- 4.2 Package and ship Memory Module per (TBD) using shipping container (TBD).

5.0 GENERAL INSTRUCTIONS

- 5.1 The Memory Card Extender Assembly 923718-A01 and Cable 929834-001 is not provided with the Memory Module and therefore must be ordered and shipped as a separate sales order item.
- 5.2 All items not provided with a Memory Module, such as, Product Specifications, Wire Lists, etc., must be ordered and shipped as a separate sales order item.

SIZE <b>A</b>	CODE IDENT NO. <b>16224</b>	DWG NO. 929490
SCALE NONE	REV. <b>E</b>	SHEET 3



# CHANGE REQUEST/CHANGE ORDER NO. 77121507

D. NO. 050

Sh. 1 of 1

ORIGINATOR: D. MARUCCIDATE: 11/8/77PROGRAM: 7405 PDP/11 PDD-0

## REASON FOR CHANGE/SUMMARY OF CHANGE

TO ADD MTP AND INCORPORATE  
220 V PS.

PART OR DOCUMENT	NEW REV.		CLASS OF CHG.	DISPOSITION			EFFECTIVITY
	DOC.	PART		USE	RWK	SCP	
929490 - 001							<u>12/29/77 All work returns <del>not</del> Affected</u>
- 002	F	B	#			<input checked="" type="checkbox"/>	
- 003							
- 004							
- 005							
- 007							
- 008							
- 009	V	B					
<u>REWORK PER MTP</u>							
<u>Z. UP REV</u>							

## Revise as follows:

① PARA 3.1 ADD MTP AS FOLLOWS----- PS928321 AND MTP 929490② RE-TYPE AND ADD VERSIONS 010 THRU 018  
INCORPORATING 220V PS PER  
SHEETS 2, 3, 4 OF THIS CROO.

ENGINEERING	MANUFACTURING ENGINEERING	PRODUCTION CONTROL	QUALITY	OTHER	CONFIGURATION CONTROL
<u>APL 11/8</u>	<u>12/20/77</u>	<u>W. Dechert</u> <u>12/20/77</u>	<u>1-5-78</u> <u>Denton</u>	<u>0.3. Bunker</u> <u>12/20/77</u>	<u>1578</u>

1.0 SCOPE

This document defines Micro 7405 Memory Modules ( )K x 18 bits with power supply. The system is a PDP11 compatible add-on, designed with the parity option.

1.1 See Sheet 4 of this document for Parts List.

PART NUMBER	REV	TITLE	CARD TYPE	CARD LOCATION CHART				
				A	B	C	D	E
929490-001		MICRO 7405 W/CHASSIS I/O ASSY. 115V PS	929402-004	x				
929490-002		MICRO 7405 64K x 18 115V PS	927390-007		x	x	x	x
929490-002			929402-004	x				
929490-003		MICRO 7405 48K x 18 115V PS	927390-007		x	x	x	
929490-003			929402-004	x				
929490-004		MICRO 7405 32K x 18 115V PS	927390-007		x	x		
929490-004			929402-004	x				
929490-005		MICRO 7405 16K x 18 115V PS	927390-007		x			
929490-005			929402-004	x				
929490-006		MICRO 7405 64K x 18 (AUTO RESTANT) 115V PS	927390-007		x	x	x	x
929490-006			929402-004	x				
929490-007		MICRO 7405 48K x 18 (AUTO RESTANT) 115V PS	927390-007		x	x	x	
929490-007			929402-004	x				
929490-008		MICRO 7405 32K x 18 (AUTO RESTANT) 115V PS	927390-007		x	x		
929490-008			929402-004	x				
929490-009		MICRO 7405 16K x 18 (AUTO RESTANT) 115V PS	927390-007		x			
929490-009			929402-004	x				
929490-010		MICRO 7405 W/CHASSIS I/O ASSY. 220V PS	927390-007					
929490-010			229402-004	x				
929490-011		MICRO 7405 64K x 18 220V PS	927390-007		x	x	x	x
929490-011			929402-004	x				
929490-012		MICRO 7405 48K x 18 220V PS	927390-007		x	x	x	
929490-012			929402-004	x				
929490-013		MICRO 7405 32K x 18 220V PS	927390-007		x	x		
929490-013			929402-004	x				
929490-014		MICRO 7405 16K x 18 220V PS	927390-007		x			
929490-014			929402-004	x				
929490-015		MICRO 7405 64K x 18 AUTO RESTANT 220V PS	927390-007		x	x	x	x
929490-015			929402-004	x				
929490-016		MICRO 7405 48K x 18 AUTO RESTANT 220V PS	927390-007		x	x	x	
929490-016			929402-004	x				
929490-017		MICRO 7405 32K x 18 AUTO RESTANT 220V PS	927390-007		x	x		
929490-017			929402-004	x				
929490-018		MICRO 7405 16K x 18 AUTO RESTANT 220V PS	927390-007		x			
929490-018			929402-004	x				

SIZE <b>A</b>	CODE IDENT NO. <b>16224</b>	DWG NO. <b>77121502</b> <del>5100</del>
SCALE	REV.	SHEET <b>2</b>



2.0 ASSEMBLY INSTRUCTIONS

2.1 Assemble per Memory Module Assembly instruction drawing 923670.

2.2 Install card assemblies per card location chart.

2.3 Mark and install nameplate per 923670.

2.4 Install label per 923670 unless otherwise specified by sales order.

3.0 TEST INSTRUCTIONS

3.1 The basic test criteria is specified in the Product Specification PS928321 and MTP 929490

4.0 SHIPPING INSTRUCTIONS

4.1 Package and ship Memory Module per (TBD) using shipping container (TBD).

5.0 GENERAL INSTRUCTIONS

5.1 The Memory Card Extender Assembly 923718-A01 and Cable 929834-001 is not provided with the Memory Module and therefore must be ordered and shipped as a separate sales order item.

5.2 All items not provided with a Memory Module, such as, Product Specifications, Wire Lists, etc., must be ordered and shipped as a separate sales order item.

SIZE	CODE IDENT NO.	DWG NO.
A	16224	77121502 <del>929490</del>
SCALE	REV.	SHEET
		3

QTY	PART NUMBER	DESCRIPTION (SPEC/SOURCE)	001	002	003	004	005	006	007	008	009	010	011	012	013	014	015	016	017	018
1	923675-A02	Chassis	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
2	927390-007	Memory Assy		4	3	2	1	4	3	2	1		4	3	2	1	4	3	2	1
3	929402-004	I/O Parity Board	1	1	1	1	1					1	1	1	1	1				
4	912602-1	Faceplate	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
5	944160-001	Rear Panel Assembly	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
6	PS929219-002	Power Supply (115V)	1	1	1	1	1	1	1	1	1									
7	PS929219-008	Power Supply (220V)										1	1	1	1	1	1	1	1	1
8	928335-001	Front Panel Assembly	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
9	928083-002	Connector Bracket Assy	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
10	934503-001	Capnut (Black)	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4
11	923645-001	Label	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
<del>11</del>	<del>923645-001</del>	<del>Label</del>																		
12	925601-001	Caution Decal	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
13	929402-008	I/O Parity Board (Auto Restant)						1	1	1	1						1	1	1	1
14	PS928321	Prod Spec																		R
15	MTP928480	Mfg Test Proc																		R

NOTE: 932755-A01 is an acceptable alternate for 944160-001 ~~until~~  
~~existing inventory is used up.~~

SCALE: A  
 SIZE: A  
 CODE IDENT NO.: 16224  
 REV.:  
 C/DG NO.: 37121502  
 SHEET: 4

FORM NO. 8084 10-72