

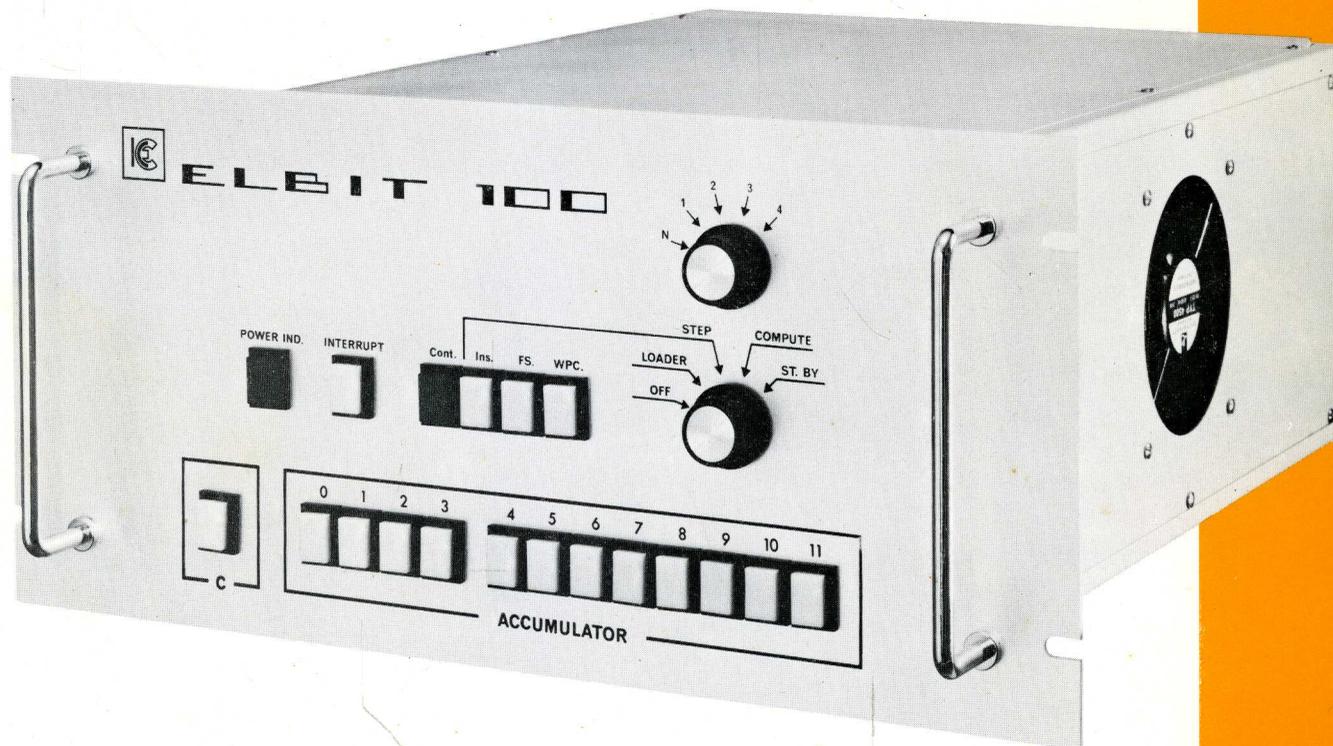
ELBIT 100

THE COMPUTER DESIGNED WITH THE SYSTEM IN MIND

Elbit Computers
9701 N. Kenton Ave.
Skokie, Ill. 60076

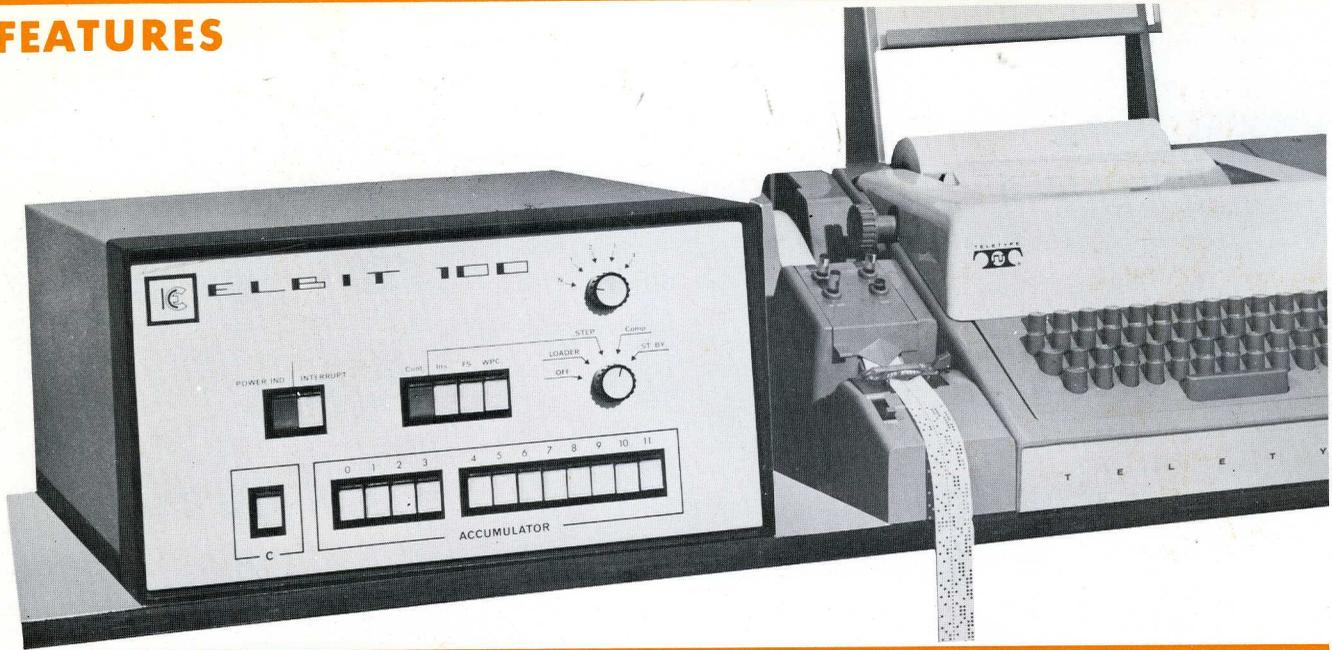
MAY 2 1969

TECHNICAL SPECIFICATIONS



ELBIT COMPUTERS LTD. • P.O.B. 5390 • HAIFA • ISRAEL

FEATURES



PROCESSOR

CORE MEMORY

12 bit, 2 usec cycle time. 1024, 2048 or 4096 words. Page oriented.

READ ONLY STORE

256 lines, 400 nsec cycle time. Factory micro-programmable.

ARITHMETIC

Parallel, two's complement binary. Add time 7.2 μ sec for full word length.

OPERATOR'S CONTROL PANEL

Designed for convenient and simple operation and debugging. It allows manual insertion of all available external instructions (single cycle operation). Displays computer registers.

DIMENSIONS

	HEIGHT	WIDTH	DEPTH	
DESK TOP	22	42	52.7	cm
	8 $\frac{3}{4}$	16 $\frac{1}{2}$	20 $\frac{3}{4}$	in
RACK MOUNT	22	48	50	cm
	8 $\frac{3}{4}$	19	19 $\frac{3}{4}$	in

POWER FAIL PROTECTION

Main frame includes automatic power fail protection and re-start.

CONSTRUCTION

DTL dual-in-line integrated circuits mounted on fiberglass printed circuit cards. Self contained instrument for desk or rack mounting.

POWER REQUIREMENTS

200 VA ;
115/230 volts ; 50/60 cps.

TEMPERATURE RANGE 0°—55°C.

WEIGHT : 25 kg. (52 lbs.).

INPUT/OUTPUT

- 256 Channels. Accessable via I/O bus.
- Hardware load.
- Peripherals need not be modified when interfaced.
- Standard cards available.

Interrupt

- A single level of priority interrupt available with standard unit. Real Time Adaptor available as an option to give 4 levels of priority interrupt.

Software

- Elbit Symbolic Language Assembler.
- Elbug - Conversational debugging program.
- Library of utility subroutines.
- Floating Point.
- Diagnostics.
- Arithmetic Library.
- Special Purpose routines.

ELBIT 100 - A SYSTEM COMPUTER

The ELBIT 100 is a low cost special purpose digital computer, designed to be readily integrated into the user's system, instrument or control loop. A 12 bit, single address, fixed word length computer with typical add time of 7.2 usec, the Elbit 100 is capable of operating with up to 256 channels of input output equipment via its I/O bus and uses DTL monolithic integrated circuits for high reliability and noise immunity. The Elbit 100 features a unique two-level memory system, with one memory being a standard read-write core store with 2 μ sec cycle time and the other being a fixed micro-programmable Read Only Store with 400 nanosecond cycle time. This micro-programmable feature of the R.O.S. allows the construction of an instruction list that exactly fits the application and thus the computer can be tailored to the application where quantities of computers are involved. This two-level memory concept is used in such large general purpose machines as the IBM 360, Spectra 70 and Honeywell 8200.

The Elbit 100 is offered with either 1024, 2048 or 4096 words of core memory. Due to the second level of memory and the extremely efficient programming language of the computer, many applications can be handled with as little as 1K of core memory effecting a great savings in cost.

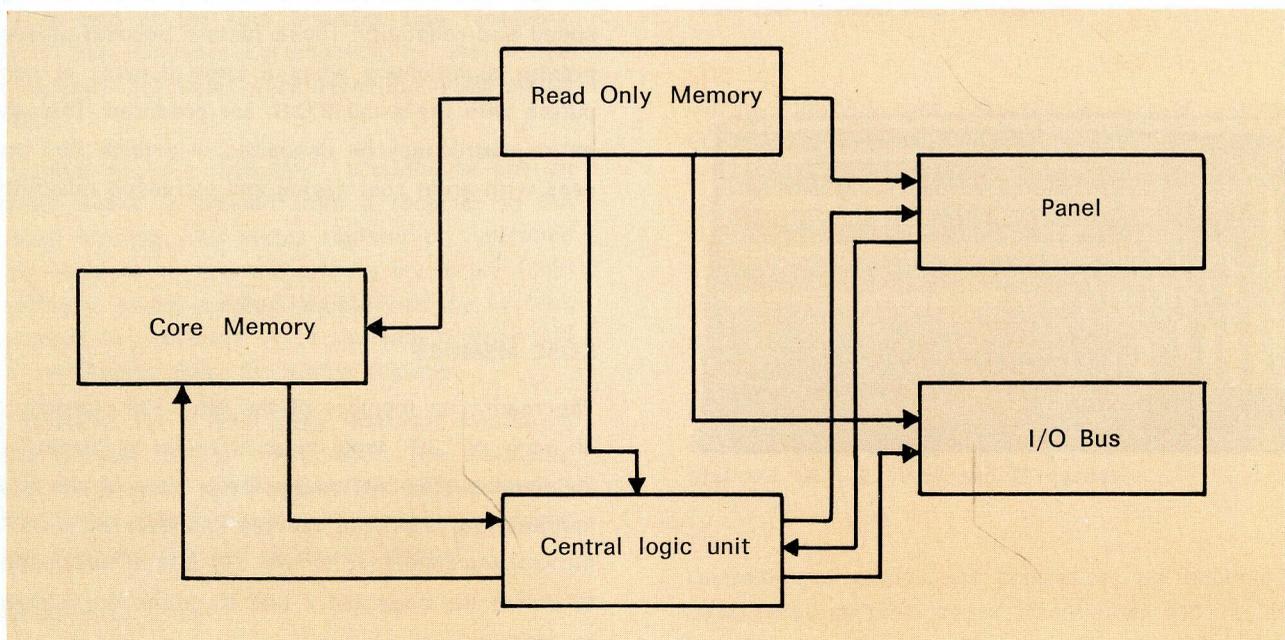
The base price of the computer always includes the core memory plus :

- | | |
|--------------------------------------|---|
| Central Processor | Power Fail protection and automatic restart |
| I/O Bus Connections for 256 channels | Chassis and control Panel |
| 256 words of Read Only Store | Interface to Standard Teletype |
| All power supplies | Priority Interrupt lines |

MACHINE ORGANIZATION

The main frame of the Elbit 100 consists of only eight (8) different cards for ease of maintenance and system integration. The general block diagram of the computer is given below.

It may be seen from this diagram that the Elbit 100 differs from the conventional small computer in that all blocks are controlled by the Read Only Store.



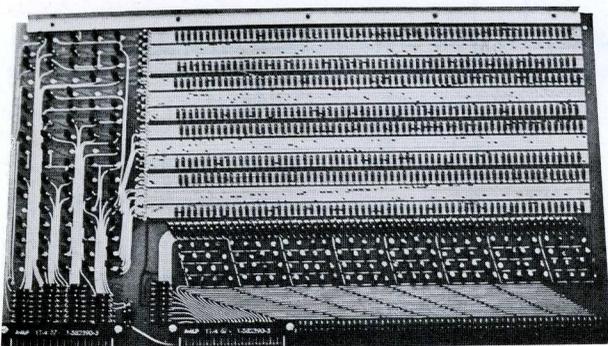
HARDWARE

READ ONLY STORE

The R.O.S. pictured below is a 256 line resistor — transistor matrix which exercises control over every register in the computer. A single line — also called a microstep — consists of a number of resistors connected (or not connected) to the base circuits of output transistors which control the basic operations of the machine. A series of R.O.S. microsteps, each of which takes 400 nsec to perform, combine to form microroutines which become the instructions of the computer. Although Elbit offers a number of standard Read Only Stores, the user may microprogram his own instruction list and thus tailor the specifications of the computer to exactly meet his requirement.

The Read Only Store Program is "written" in a simple symbolic form and then converted into hardware by means of a resistor matrix, address decoder, drive transistors and a clock that assures that each step takes place sequentially. The picture below shows the construction of the R.O.S. matrix with its address selection and output drive transistors.

The R.O.S. is divided into four parts called fields. Each field controls a different section of the computer.



field α : Controls the output selectors which connect the output register of the arithmetic unit with the various machine registers.

field β : Controls the input selectors connecting the machine registers with the arithmetic unit.

field K : Controls carry selectors connecting the various carry registers with the central logic unit. It also controls any conditional operations.

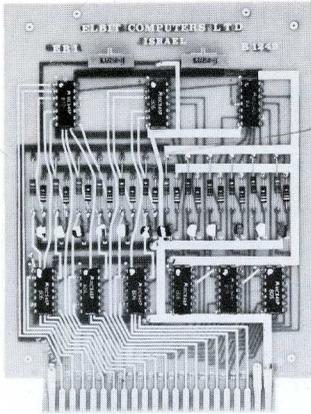
field P : Controls the following :

- Central logic unit (defining its operation)
- Core memory (read/write)
- I/O Selectors
- Jumps within the R.O.S. program.

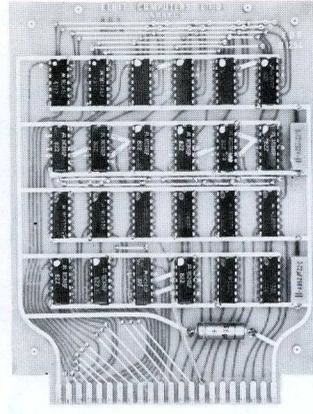
While some manufacturers of machines using read only memories have gone to the use of cores, transformers and other two-state devices, Elbit has chosen to use resistors for considerations of cost, speed and reliability. These factors become of even greater significance when a large number of computers with the same R.O.S. are produced. Then the entire matrix may be deposited in a thick film process with great cost saving and increased reliability.

CORE MEMORY

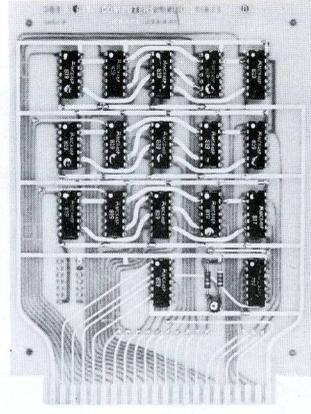
The read-write memory of the Elbit 100 consists of an array of "3D" type cores arranged in "pages" of 256 twelve (12) bit words: Cycle time of the R/W memory is 2 usec. The memory is addressed via a 12 bit register consisting of four (4) bits of information to define the page and 8 bits to define the address in page.



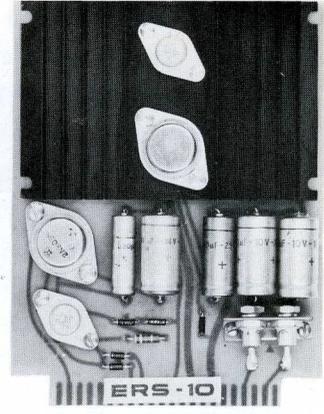
EBI



EDR



EDC



ERS-10

ROUTINE". This program sets all the devices to the state in which they existed at the time of the power fail, arms the interrupt F.F. and jumps to the fixed location or the previously stored address (depending on the nature of the program).

REAL TIME INTERRUPT

With the addition of the low-cost RTA option to the main frame, the ELBIT 100 has the ability to distinguish between four different levels of priority in real-time. Thus the main program is not interrupted unless priority actually exists.

The four states interrupt system divides external devices into four groups, according to the hardware configuration in which they are connected to the computer. Devices of each group are tied (wired "or") to one of the four interrupt line receivers. Each of the receivers corresponds to one of the four set-only flip-flops which form the 4 bit status register.

The status register "decides" whether or not an interrupt signal is passed from a receiver to the interrupt flip-flop. The status register is controlled by the program so that the priority levels are fixed by software, giving greater flexibility to the system. The power fail interrupt is of absolute priority and does not depend upon the status register.

The software for a four state interrupt system is similar to that of the single level. The additional task of the program is to control the status register. Details of all interrupt software routines are found in the Programming and Software Manual.

* See description of R.O.S.

** Device Service Routines for standard devices are given in the ELBIT 100 Programming Manual.

STANDARD INTERFACE CARDS

ELBIT offers a family of standard interface cards and mounting hardware to facilitate user designed interface systems.

EBI

Is an I/O bus receiver and transmitter card designed to communicate with the I/O bus from an external station. It contains 12 bidirectional driver transmitters for information transfer and one I/O channel pulse receiver.

EDR

This is the decoder card capable of receiving the information from V & U and decoding up to 16 channels (8 input and 8 output).

EDC

Device controller card. Controls the flow of information to and from the peripheral. Generates Interrupt; provides output buffering; accepts control signals and data; informs computer of device status.

EXU

For driving an I/O bus larger than 20 ft. or for more than ten external stations.

ERS-X

Regulated power supply card for powering external stations (X = 5, 10, 15 and 20 cards).

ES-X

Chassis plus guides and connectors for holding X cards. Also contains power transformer and I/O bus connectors (50 pin).

CENTRAL LOGIC UNIT

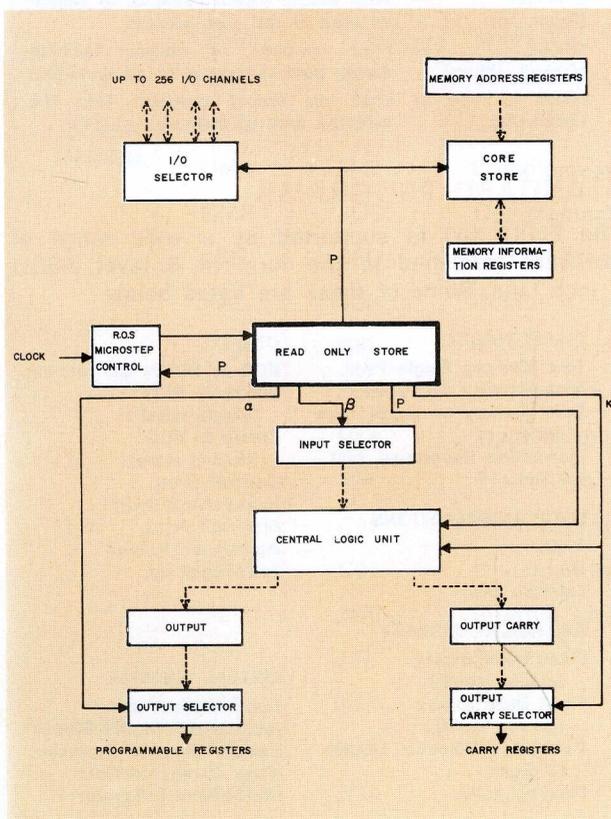
The Central Logic Unit performs all arithmetic and transfer operations under control of the Read Only Store and the timing system.

The heart of the C.L.U. is the four bit high speed parallel adder. All registers in the computer are four bits in length. In order to perform a twelve bit by twelve bit addition, three such operations must be performed with proper attention paid to resultant carries. One input to the adder is one of the 4 bit registers specified by the R.O.S. while the other input (the adder) is located in the Transfer (E) register. Since subtraction is performed by two's complement addition, the R.O.S. also determines whether the "true" or "one's complement" is fed into Adder. In the case of subtraction 1 is automatically added to the output. A transfer operation is performed by inhibiting the output of E from entering the adder and in effect adding zero to the value being shifted.

PROGRAMMABLE REGISTERS

ACCUMULATOR (ACC)

This is a twelve bit register made up of three 4 bit registers called 3Φ , 2Φ , and 1Φ . One of its functions is to "accumulate" the results of all arithmetic operations performed by the Central Logic Unit. Thus the results of all arithmetic operations are contained in the ACC. Its value is displayed on the front panel and may be altered by means of the illuminated pushbuttons. It also serves as the input/output register and as such is hooked to the I/O bus. Any 4 bit portion of the Accumulator may be cleared, shifted rotated, read into or out of.



MEMORY ADDRESS REGISTER (MAR)

This 12 bit register is made up of three 4 bit registers (W, V, U) with W holding the page number and (V, U) holding the address in page. Thus 16 pages of 256 words or a total of 4096 words may be directly addressed. The (VU) portion of this register also is used in the input/output operation to define the channel number of the device to be interfaced and so these eight lines are fed to the I/O bus.

MEMORY INFORMATION REGISTER (MIR)

This 12 bit register is made up of three 4 bit register (F, R, Y) and receives the information read out of the core storage. Under R.O.S. control, information may be shifted into or out of any or all 4 bit portions.

CARRY (C) 1 BIT

The ELBIT 100 has 7 one bit carry registers (designated $C_1 - C_7$) in which to store carries resulting from various operations. The programmer has access to C_3 only, and its value is displayed on the front panel. The remaining 6 flip-flops are for internal use by the R.O.S. microprogrammer.

MAIN PROGRAM COUNTER

The program counter, made up of two (2) four bit registers 2T, 1T, contains the address in page of the next instruction to be executed. Together with the W register it defines the next instruction address and is always incremented by one after the execution of an instruction. The Jump and Skip instructions alter the contents of the P.C.

There are many other registers in the computer, however, these are used only by the Read Only Store and are not accessible to the programmer.

SYSTEMS CONCEPT

In order to understand the operation of the ELBIT 100, it is necessary to understand the interrelationship between the Core Memory with its (the main) Program Counter and the Read Only Store and its program counter. When the programmer (or the assembler) writes an address, he is referring to the main program counter W, 2T, 1T. The computer, upon receipt of any instruction, automatically jumps to a R.O.S. microroutine called the "Supervisory Program" which is performed at the beginning of all operations. This microroutine does the following: transfers value of program counter to the Memory Address Register (WVU) to set up the reading of the current instruction from the core store; increments main program counter; reads out instruction to be performed and writes it back into correct memory location. The program jumps to address of the microroutine in the **ROS PROGRAM COUNTER** defined by the instruction and performs it. This is called an "Executive" microroutine and, upon completion, the ROS takes the present contents of the program counter (PC+1) and begins the process all over again. Thus the R.O.S. and its associated registers may be thought of as a computer within a computer.

PROGRAMMING

As this machine was designed to be used by engineers and scientists rather than programmers, the programming system has been designed to be as simple as possible. Programs are written in Elbit Symbolic Language (ESL) for which there is an assembler. Instructions are written in hexadecimal form and normally appear as shown below.



Since the 4 bits of order code allow selection of only 16 instructions this code may be extended into the operational section. In the instruction list it will be noted that many instructions are written without operand.

ELBIT ASSEMBLY PROGRAM (EAP)

The Elbit Assembly Program (EAP) accepts source programs written in the Elbit Symbolic Language and converts them into the machine code equivalent. This conversion is accomplished in two passes. The labels with assigned associated addresses are displayed during the first pass while the second provides the complete listing of the program with the error messages and the object tape. The large set of the operational pseudo-instructions together with the feature of the two level labeling allows the operator to assemble a set of standard software packages together with his own routines into a unified large program. The object tape may be fed into the computer without any additional software. The EAP recognises data of two radix systems and two types of alphanumeric codes. The EAP operates with a minimum configuration of 2K memory and on-line Teletype ASR33/620.

EAP OPERATIONAL INSTRUCTIONS

First	—	Switch program to the first pass
Second	—	Switch program to the second pass
Clear	—	Erase previous local labels
Reset	—	Erase previous local and common labels
Define	—	External label or channel definition
Origin	—	Initial address definition
Start	—	Start input device, begin processing Start disables TTY keyboard
End	—	Stop input device, terminate pressing End enables TTY keyboard

TINY

The One Pass Simplified Assembler assists in the preparation of small programs (up to one page), and offers significant time advantages at assembly time. The object tape is accompanied by the machine code listing with error symbols.

ETE

Elbit Tape Editor is used to edit and correct source program tapes by means of inserting, deleting and replacing proper lines. All operations may be prescribed in advance which saves operator time.

ELBUG

Elbug is an on-line debugging program that allows the operator to supervise loading and running of his object program. Eight powerful operations provide monitoring of the executed program, tracing the selected location, altering, printing and punching parts of the memory. Communication is via teletype and the self protection feature does not allow in experienced operators to destroy the Elbug program. Elbug occupies 2 memory pages and all the rest of memory space remains available for the program to be debugged.

ELBUG OPERATIONS

COMPUTE (From, To)	—	Execute selected point of the program.
REPORT (From, To)	—	Execute and monitor selected part of the program.
TRANSFER (From, To)	—	Direct transfer in the memory.
STORAGE (Object, To)	—	Store the word in the memory.
SEARCH (For)	—	Print all the addresses containing the requested constant.
DISPLAY (From, To)	—	Print and/or punch contents of selected area of the core storage.
TRACE (Object, When)	—	Print contents of chosen location during selected parts of computation.
LOAD (From, To)	—	Load an object program into the selected area of memory.

STANDARD PROGRAMS

The ELBIT 100 is supported by a wide range of software furnished in the form of 8 level, ASCII 1 inch tape. Some of these are listed below :

MAINTENANCE

Test Memory Single Page.
Test Memory All Pages
Test Memory — worst case pattern.
Instruction Repertoire Test.
I/O Test.

LOGICAL OPERATIONS

AND.
OR.
Exclusive OR.

ARITHMETIC LIBRARY

Fixed point Binary (single length).
Fixed point Binary (double word).
Decimal arithmetic Library (8 digit).
Floating point.

UTILITY

BCD to Binary Conversion.
Binary to BCD (single word).
Binary to BCD (double word).
Decimal Print.
Hexadecimal Print.
Bit-by-Bit Print.
Alphanumeric Print.
Table Look up.

SPECIAL PURPOSE

Data Concentrator.
Incremental Digital Plotter.
Sample Changer Controller.
Nixie display control.
Multichannel Integrator.

INSTRUCTION REPERTOIRE

R. O. S. U'

TYPE	MNEMONIC	CODE	DESCRIPTION
LOAD	LDA	Gxx	Load Accumulator from current page
	LDI	8xx	Load Accumulator from Indirect Address
	LDS	7xx	Load Accumulator with S portion of Instruction
STORE	STA	6xx	Store Accumulator in memory
	STI	0xx	Store Accumulator to Indirect Address
	STS	Fxx	Store S portion of the Accumulator
JUMP	JMA	38F	Jump According to Accumulator
	JMI	2xx	Jump According to Indirect Address
	JMS	Bxx	Jump According to S portion of Instruction
ARITH-METIC	ADA	5xx	Binary Addition to Accumulator
	SBA	Exx	Binary Subtraction from Accumulator
	ADM	Dxx	Add to Memory
SKIP	SNA	34n	Skip n Instructions (n = 1—15) on Negative Accumulator
	SPA	33n	Skip n Instructions on positive Accumulator
	SIC	37n	Skip n Instructions if carry exists
	SNZ	30n	Skip n Instructions if Accumulator not Zero
	SFN	31n	Skip n Instructions if F portion of Accumulator not Zero
OPERATIONAL	DTR	4xx	Direct Transfer
	IZS	9xx	Increment Memory, Skip if Zero
	MSK	1xx	Mask the Accumulator
	CLF	3B7	Clear F Portion of Accumulator
	CLC	3F7	Clear Carry
	CMA	3FD	Complement Accumulator
	CMS	3GD	Complement S Portion of Accumulator
	LSH	3FG	Left Shift of Accumulator and carry one bit
	RAL	3D0	Rotate Accumulator Left 4 bits
	RAR	396	Rotate Accumulator Right 4 bits
	CHP	3EE	Change Page
I/O	IOP	Cxx	Input/Output
	BIP	384	Block Input
	ARI	C02	Arm Interrupt
	DRI	C01	Disarm Interrupt
	INT	3EF	Internal Interrupt
HALT	STP	3BE	STOP
	HLT	3D3	HALT
	BRK	3D5	BREAK
	WAT	3B5	WAIT

NOTES :

1) F refers to first 4 bits, S to last 8 bits.

2) Elbit Hexadecimal does not use the letter "A" thus 10 = B and 15 = G.

INPUT OUTPUT

PRINCIPLES OF ELBIT 100 INTERFACE

One of the great advantages in using the ELBIT 100 as a system component of portion of a control loop is the ease with which it may be interfaced with the outside world. In designing this interface system great effort was expended in keeping it as simple as possible so that up to 128 channels each of input and output may be tied to the standard machine. In addition, since the system of interface used is a "bus" type, no logic changes are required when additional channels up to a total of 256 are added to the computer in the field.

Another important feature of the Elbit design philosophy for interfaces is to provide all interfaces independent of peripherals, and to make no modifications of standard I/O devices. This enables the user to purchase his interface, to say a card punch, from Elibt, and the actual card punch from the original equipment manufacturer. This saves the customer the usual mark up and handling charges and simplifies the servicing of the peripherals.

THE I/O INSTRUCTION

In order to perform a programmed I/O operation, the programmer must write his instruction in the following format :

F	V	U
4 bits	4 bits	4 bits

Where F is the order code of the I/O operation (see Instruction Lists) and VU are the hexadecimal equivalent of the channel number to be tied to the I/O bus.

THE I/O BUS

This is the feature of the ELBIT 100 which enables the computer to be interfaced with such ease to the outside world. A plug on the rear panel of the computer contains the 50 pin I/O bus which is made up of the following signals (2 lines per signal twisted pair).

Accumulator	— 12 lines of buffered bidirectional information.
Channel number	— 8 lines of buffered unidirectional information for feeding Channel number (VU) to device decoder.
Channel pulse	— Single buffered unidirectional line to enable the I/O operation.
Interrupt	— 4 unidirectional lines for four levels of priority interrupt.

For more detailed information on the ELBIT 100 Interface system see the Installation Interface Manual.

INTERRUPT

The basic ELBIT 100 has the ability to recognize a single level of interrupt with no additional hardware. Receipt of an interrupt signal triggers an interrupt flip-flop associated with the Read Only Store.

R.O.S. INTERRUPT MICROROUTINE

Upon termination of each instruction the R.O.S. interrupt flip flop is checked. If it has been set to "one" the microprogram jumps to the microroutine which performs the following :

- A. Disarms Interrupt.
- B. Resets Interrupt flip-flop.
- C. Stores value of Program Counter in the memory location 001.
- D. Sets Program Counter to the value 002.
- E. Jumps back to the R.O.S. supervisory routine.*

The steps D and E cause the computer to enter the program beginning in the memory locations 002. This routine is called Interrupt Supervisor Routine.

The software system consists of the Interrupt Supervisor and device service routines. The Interrupt Supervisor stores the conditions (value of Acc and Carry) of the program at the time of the interrupt and scans for the device that requested the interrupt. The device service routines are of two kinds : first order and second order.

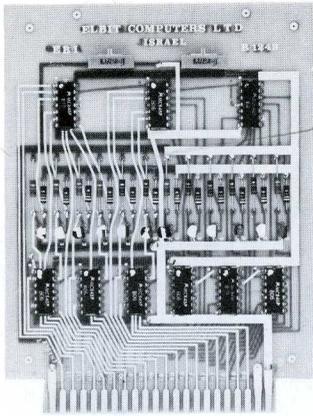
A first order device service routine (D.S.R.)** is always completely executed and cannot be overridden by any other device.

A second order device service routine may be itself interrupted by a call from any other device (even of equal order).

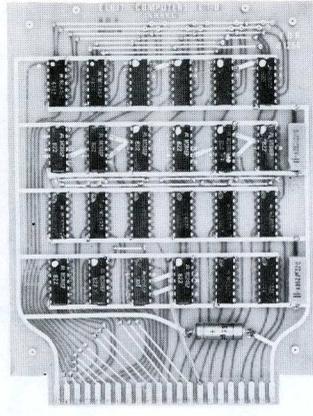
Although there is no external priority logic, the order in which the devices are scanned decides which device will be served first in the case where two call for an Interrupt simultaneously.

The power fail service is always accepted before any other Interrupt signal. Should a device service routine, of the first order, take more than one mSec to complete, it (the D.S.R.) has to check if the power fail has not been generated in the interim.

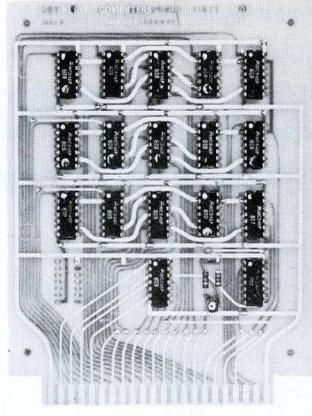
Every ELBIT 100 main frame contains power fail protection and restart. After power fail break, the program begins with the fixed routine called "INITIAL



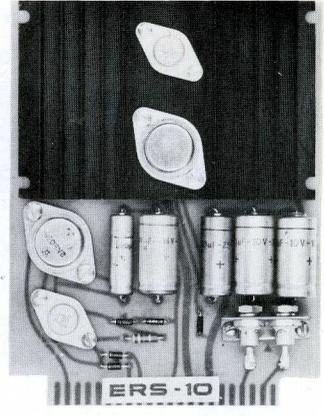
EBI



EDR



EDC



ERS-10

ROUTINE". This program sets all the devices to the state in which they existed at the time of the power fail, arms the interrupt F.F. and jumps to the fixed location or the previously stored address (depending on the nature of the program).

REAL TIME INTERRUPT

With the addition of the low-cost RTA option to the main frame, the ELBIT 100 has the ability to distinguish between four different levels of priority in real-time. Thus the main program is not interrupted unless priority actually exists.

The four states interrupt system divides external devices into four groups, according to the hardware configuration in which they are connected to the computer. Devices of each group are tied (wired "or") to one of the four interrupt line receivers. Each of the receivers corresponds to one of the four set-only flip-flops which form the 4 bit status register.

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The software for a four state interrupt system is similar to that of the single level. The additional task of the program is to control the status register. Details of all interrupt software routines are found in the Programming and Software Manual.

* See description of R.O.S.

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EDC

Device controller card. Controls the flow of information to and from the peripheral. Generates Interrupt; provides output buffering; accepts control signals and data; informs computer of device status.

EXU

For driving an I/O bus larger than 20 ft. or for more than ten external stations.

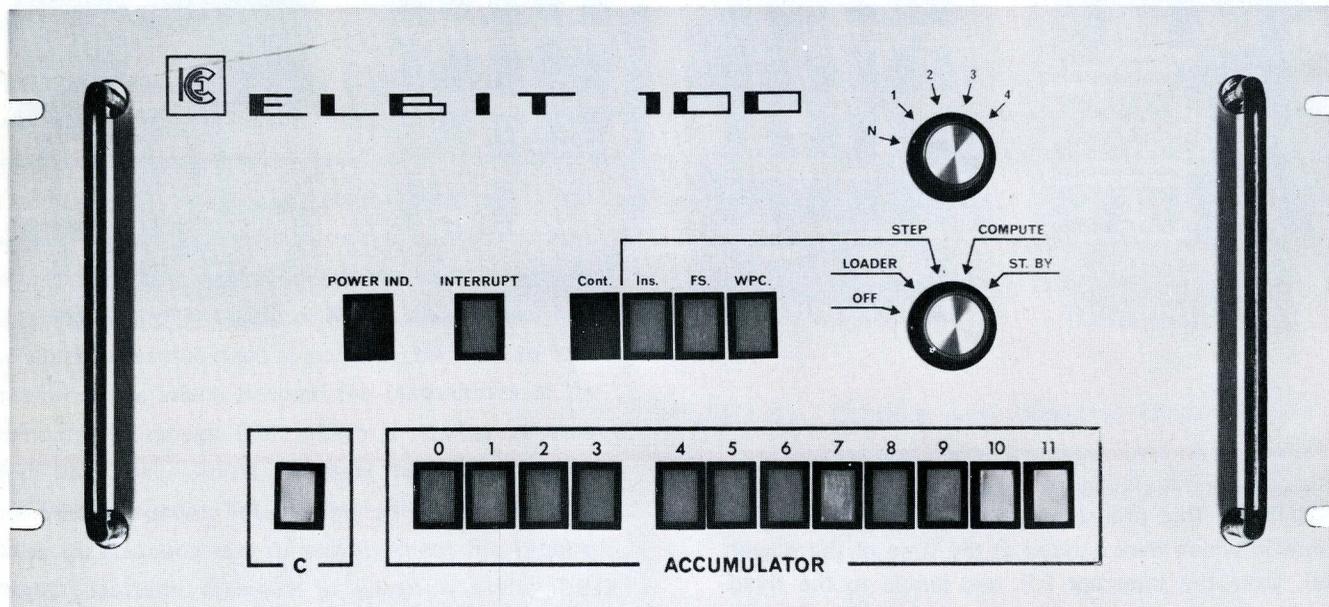
ERS-X

Regulated power supply card for powering external stations (X = 5, 10, 15 and 20 cards).

ES-X

Chassis plus guides and connectors for holding X cards. Also contains power transformer and I/O bus connectors (50 pin).

PANEL CONTROLS



The ELBIT 100 front panel is a model of functional simplicity. Thirteen illuminated pushbuttons indicate the contents of the Accumulator and Carry registers and these same pushbuttons allow the contents to be altered. In addition to the Power Indicator button (which is only an indicator), there are four functional illuminated pushbuttons :

CONTINUE BUTTON

When depressed, the program will continue from the present address of the Program Counter.

INTERRUPT BUTTON

When this button is depressed the program counter is reset to the value specified by initial address switch.

WPC BUTTON

This illuminated pushbutton provides access to the Program Counter to display or insert addresses.

FS BUTTON

Provides access to instruction register to display or insert instructions.

The remaining controls are two rotary switches :

MODE SWITCH (lower rotary)

This rotary selector switch may be in any of five possible modes :

- (a) Off — No power provided. Indicator lamp "Power Ind." not lit.
- (b) Loader — In this mode the computer is prepared to receive data from either punched paper tape or through manual entry.
- (c) Step — In this mode, the operator may perform "single shot" operations i.e. perform one step of the program and alter or display the contents of the main registers of the ELBIT 100.
- (d) Compute — Execution of a program.
- (e) Standby — The computer is in the memory protected state and all push-buttons are inhibited. Also referred to as Coffee Break Mode.

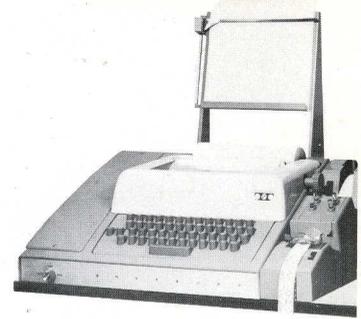
INITIAL ADDRESS SWITCH (upper rotary)

The user may specify up to four hard-wired addresses (1-4). When the rotary switch is in a position other than N (normal) data will enter into the specific fixed starting address.

STANDARD PERIPHERALS

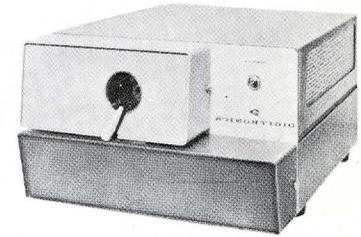
TELETYPE

The simplest and least expensive input-output device available for use with the ELBIT 100 is the Teletype model ASR 33. This device combines a typewriter, punched tape reader and tape punch which operate at 10 characters per second and provide an ASCII character set. Users purchasing the Teletype directly from the manufacturer are advised to specify the model 33/620 and to advise Elbit as to whether it is a 50 or 60 Hz device.



PHOTOELECTRIC TAPE READER

For rapid entry of punched tape programs and data into the ELBIT 100, a 300 character per second photoelectric tape reader is offered. A Digitronics model 2500 it can handle 5, 6, 7 or 8 level (plus sprocket) tapes interchangeably.



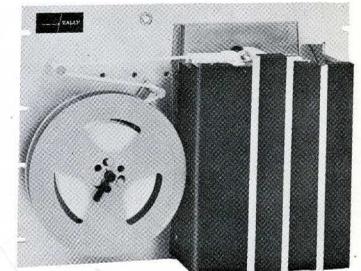
MECHANICAL TAPE READER

For those users who want faster entry of data than the Teletype at low cost, Elbit offers the Invac model R 360 mechanical reader capable of reading 60 characters per second.



HIGH SPEED TAPE PUNCH

Data may be output asynchronously from the ELBIT 100 at a 120 characters per second by use of a Tally P120 tape punch. The punch uses 8 level code and has built in parity checking.



INCREMENTAL MAGNETIC TAPE OUTPUT

Data output can be recorded on 1/2 inch magnetic tape in IBM 360 compatible format using the Kennedy model 1400/360 incremental recorder. Data is recorded with a density of 800 bpi on nine tracks at a maximum speed of 500 types per second.

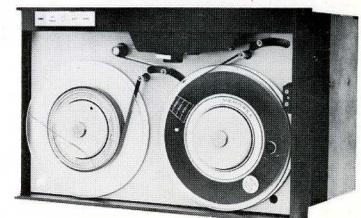
SYNCHRONOUS READ/WRITE TAPE RECORDERS

The ELBIT 100 may record on and read from 1/2 inch, 7 or 9 channel magnetic tape. The Peripheral Equipment model 5820 can record at 800 bpi.



MAGNETIC DRUM

For applications requiring bulk storage, Elbit offers a low cost magnetic drum with storage of more than 1 M bits. The Magnifile model 8403 offers an average access time of 8.5 ms with 64 data tracks.



ALSO AVAILABLE

Analog to Digital, Digital to Analog Converters available in 8-12 bit versions with and without multiplexing.

PERIPHERALS UNDER DEVELOPMENT

Disc Memory, Line Printer, Interface to IBM 360.

TYPICAL APPLICATIONS

DATA TERMINAL OR CONCENTRATOR

Connected to a time sharing system, the ELBIT 100 can edit, format, verify and concentrate data prior to transmission and perform corresponding operations on incoming data to reduce loads and costs on data lines and on the larger computer.

PROCESS CONTROL

Interfaced to various analog and digital devices, the ELBIT 100 may be programmed to monitor, calculate, display, record and exercise control over complex real-time processing systems.

DATA CONVERSION

Due to its low cost, the ELBIT 100 has been used in systems for converting paper tape to magnetic tape. Such a system may also be expanded to perform off-line plotting or printing.

PRODUCTION TESTERS

The ELBIT 100 has been used with test instruments such as I.C. testers which previously had to be programmed by hand. At the same approximate cost as a high speed tape reader the computer adds speed and flexibility to the system.

DATA VERIFICATION

The ELBIT 100 can operate with a larger computer as a satellite performing tedious operations on raw data and feeding only verified data to the main computer. As an example, in banking or accounting operations unverified data can be fed from a number of keyboards to an ELBIT 100 and checked for parity, legal codes, dates, etc. The verified and edited data is then output onto magnetic tape for feeding into a large computer.

MACHINE CONTROL

Numerical control of machine tools from instructions coded on punched tape greatly increases the speed, accuracy and repeatability of manufacturing operations. Preparation of the tapes however, is time consuming and subject to error. Use of a small digital computer solves these problems.
