DIGITAL SYSTEMS

FLOPPY DISK SYSTEM REFERENCE MATERIAL

List of Attachments

DIGITAL SYSTEMS is currently marketing only the FDC-1 floppy disk controller board and Shugart disk drives. We are providing documentation on the interface we have used to interface the FDC-1 to an Altair compatible machine. We have used the resulting system to run CP/M, a sophisticated disk operating system.

While the bus interface to the FDC-1 is a relatively simple cicuit, the total disk system is complex. Debugging a hand wired system may be beyond the capabilities of an inexperienced TTL designer.

DIGITAL SYSTEMS will produce a completely assembled and tested interface to the FDC-1 if there is sufficient demand. We estimate the cost of the board to be $30 with availability October 1. Let us know if you would be interested in this board as we believe this would be the best way for most users to bring up a disk system.

DIGITAL SYSTEMS
MODEL FDC-1
FLOPPY DISK CONTROLLER
INTERFACE MANUAL

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INTRODUCTION

This manual provides the information needed to utilize the DIGITAL SYSTEMS Model FDC-1 floppy disk controller within a data system. It is intended as a reference for technical personnel engaged is the specification, design, and implementation of a digital system with flexible disk drive storage devices. Both hardware and software requirements for integrating the FDC-1 with memories, processors, disk drives, and system wide controlling devices are described.

Details of the interior of the FDC-1 do not appear here; these are found in the FDC-1 Technical Description manual. Aspects of the controller detailed here include specification and timing for all exterior interface signals, physical layout, power requirements, and required command sequences generally supplied under program control from a host processor system to the disk controller.

A block diagram of the FDC appears in Figure 1.

The FDC-1 is a flexible disk drive controller for up to four selectable drives. The FDC-1 uses a high speed microprocessor based design providing reliable and flexible functions implemented in read-only memory logic. Features of the FDC-1 include drive write protect, automatic CRC generation and check, full IBM 3740 compatible soft sector formatting, automatic track seek verify, and head retraction after eight idle disk rotations to assure long diskette life. An automatic bootstrap load from Track 0, Sector 1 can be done at system initialization without system processor intervention.

The FDC-1 is fully TTL implemented and compatible. An adaptible, simple interface to mini and microprocessor systems is provided with 8 bit parallel input and output busses for control information. A DMA interface moves data directly in or out of memory once a transfer is initiated.

Packaging is on a single 10" x 12" PC board with system interface via standard edge connectors and flat cable to the flexible disk drives.

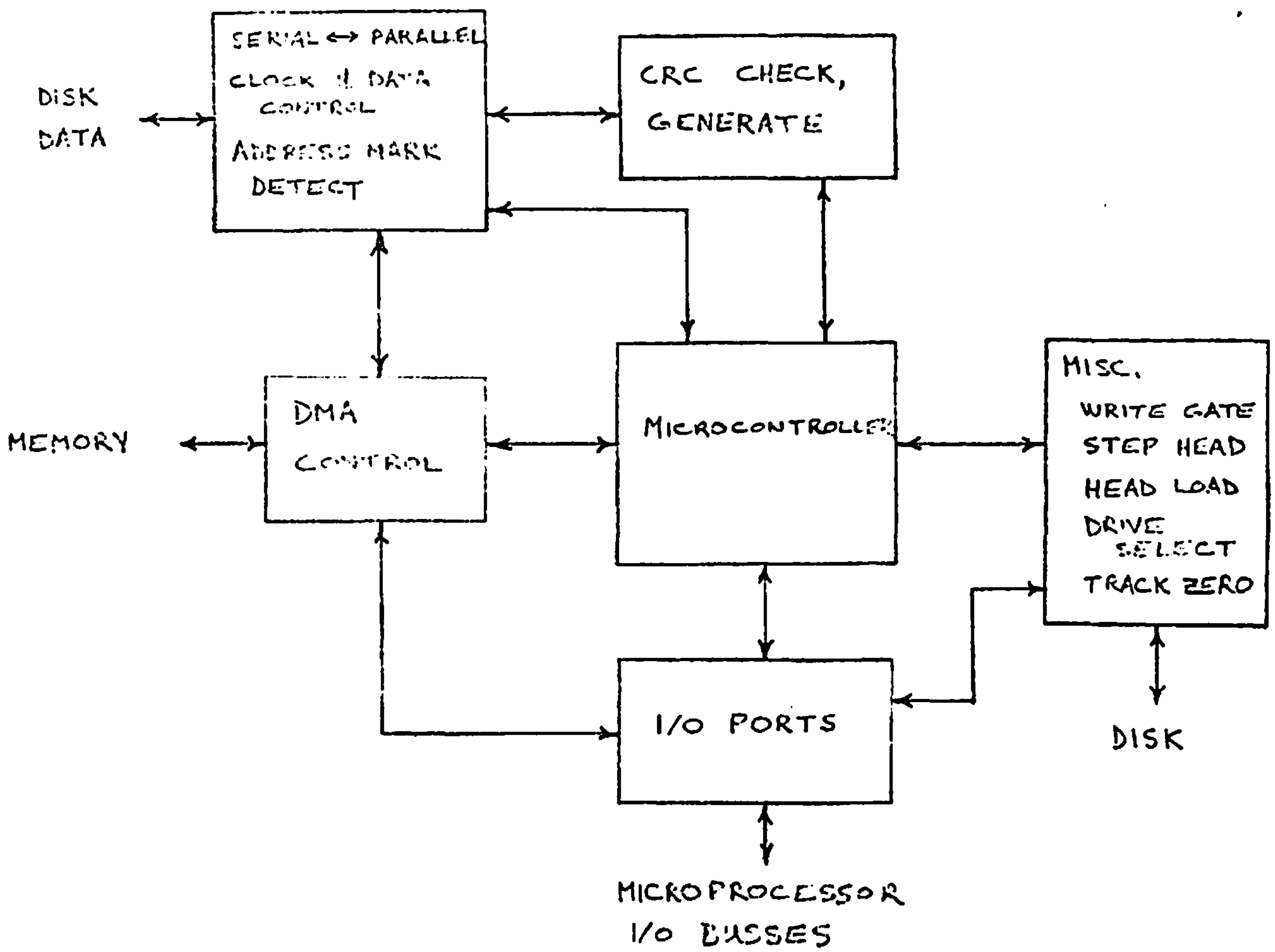

Figure 1. FDC-1 Block Diagram.

HARDWARE INTERFACE TO THE FDC-1

A diagram of the FDC external signals appears in Figure 2. The signals can be divided into three distinct interfaces; the device, direct memory interface (DMA), and disk interfaces. The device interface implements command and status information between host system control hardware (i.e. processor and processor support logic) and the FDC. The DMA interface exchanges data with up to 64 Kbytes of random access memory. The disk interface connects the FDC to a chain of flexible disk drives handling IBM format compatible diskette media. Initialization and power supply lines complete the FDC requirements.

A detailed description for each interface follows. Reference is made to the appendices containing backplane signal pinouts (J1 and J2), connector pinouts for the disk interface (J3), and the following table summarizing the mnemonic name, active state, and description for all interface signals.

SYSTEM BUSSES

Following is a summary of the busses and controls for the FDC, their names, active state, and description. All busses except MAD are 8 bits wide, bit 7 is the most significant bit, bit 0 the LSB. Index x varies from 0 to 7 unless otherwise noted.

Name	Active	Description
DINx	hi	device input bus data to host via backplane
-DOUTx	low	device output bus data from host via backplane
MDINx	hi	memory data in data to memory via backplane
MDOUTx	hi	memory data out data from memory via backplane
-DEVx	low	device address to devices
MADx	hi	x ranges from 0 to 15 16 bit memory address bus to memory via backplane
REQ	hi	single line raised by FDC to request a memory cycle
ACK	hi	single line raised by host memory system to grant a memory cycle
-WRITE	low	lowered after cycle is granted if FDC wishes to write to memory
-IN	low	input device strobe
OUT	high	output device strobe
-IRESET	low	system restart signal
-IOF	low	I/O finished by FDC
-BOOTSTRAP	low	forces FDC to execute bootstap and return -IOF
DZPROT	high	inhibit writing on disk 0

All bus levels are TTL standard, with low level signals below 0.4 VDC and high level signals above 2.5 VDC. All signals listed above except REQ and the last six signals in the table are implemented as high impedance (TRI-STATE) drivers which may be shared by other host system devices using appropriate strobing.

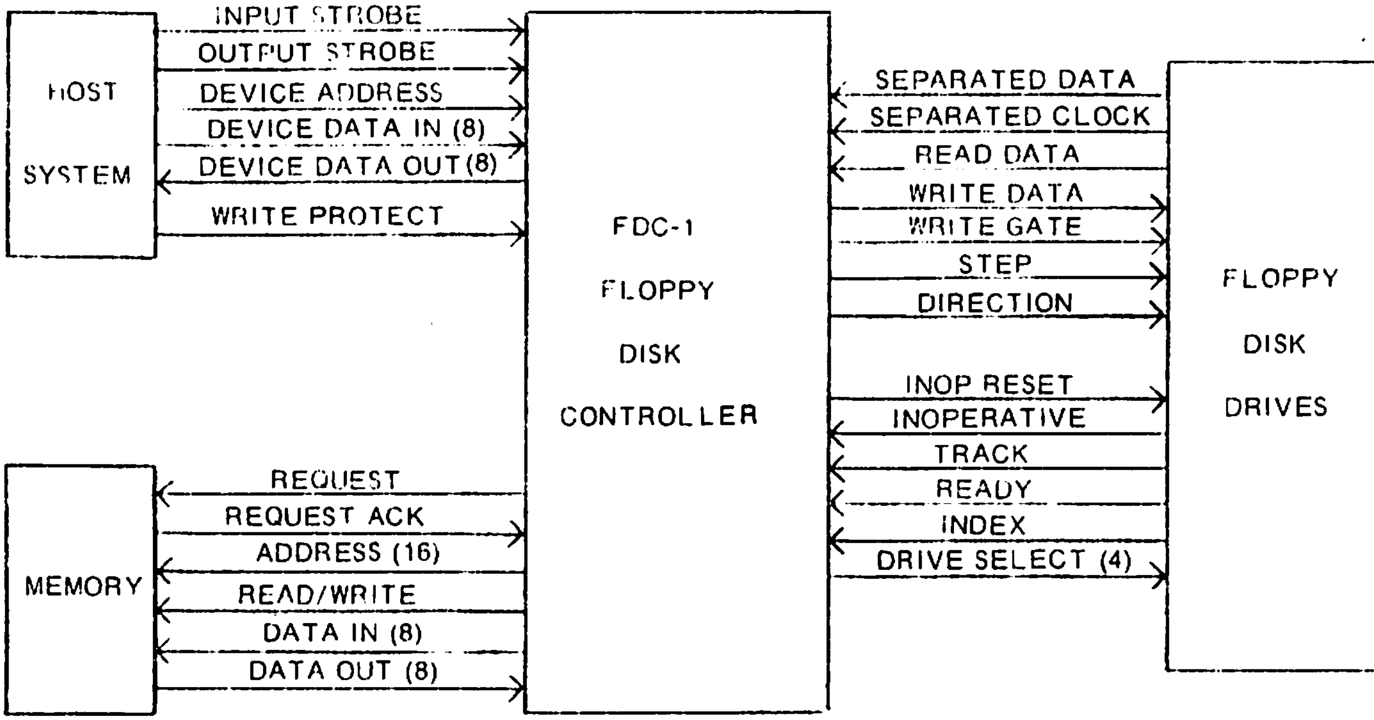

Figure 2. FDC-I External Signals.

DEVICE INTERFACE

Interaction between the host processor or controlling hardware and the FDC is implemented by the device interface. The controller is idle until an eight bit address appears on the device address bus (-DEVi) and one of two strobes (OUT or -IN) appears simultaneously with the device address. Strobes cause decoding logic to sense the state of the -DEVi bus and, if it is presenting one of the set of addresses given below with the appropriate strobe, a set of actions occurs. With a device address and an OUT strobe, data bits present on the device output bus (-DOUTi) will affect the FDC as indicated below. Device addresses decoded with -IN will cause the FDC to drive status bits onto the device input bus (DINi) for use by the host system. All signals must be stable at their active level for a minimum of 200 nanoseconds.

Note the locations of the device address bus (-DEVi), device input bus (DINi), device output bus (-DOUTi), and strobes OUT and -IN on the table in Appendix I.

Device 127D (177Q, 7F hex) is the status input device when strobed by -IN and the command output device when strobed by OUT. The status device delivers eight bits of disk system status to the device input bus bits 0 through 7. These bits will be stable 100 nanoseconds after the device address is available and remain stable for as long as the address and strobe are stable.

The status bits are:

Bit 0: file inoperative - an error signal from the disk indicating invalid writing sequencing

1: step ready - indicates 10 milliseconds elapsed since the last step command was executed and the disk is able to execute further commands

2: track zero - indicates that the read/write head on the selected disk is positioned at the outermost track

3: I/O finish - indicates that the FDC has completed processing (or aborted because of an error condition) the previous read or write command

4: track error - indicates the byte read from memory at the initial DMA address did not match the track byte of an ID field actually read from the disk. The current command is aborted.

5: ID CRC error - a CRC error was encountered in the ID field of the requested track/sector. Read commands will complete but Write commands are aborted.

6: Data CRC error - indicates a CRC error in the data fields during a Read command

7: Head Unloaded - indicates at least eight revolutions of the disk have occurred since the last Read or Write command, and the hardware has unloaded the head of the selected disk. If a software error results in a request for a sector number greater than 26D, this bit and a zero bit 3 (I/O never finishes) will indicate the error as the FDC will search forever for the requested illegal sector.

When device address 127D appears with the OUT strobe, the bits on the device output bus (-DOUTi) are interpreted by the FDC as command bits. The command register in the FDC is loaded using OUT as a strobe to the register.

The command bits are:

Bit 0: file inoperative reset - required response to the file inoperative status bit

1: step - commands the selected drive to move in the direction selected by bit 2.

2: direction - directs the disk drive to step towards Track 77 (innermost) when active (-DOUT2 low) and towards Track 00 when inactive (-DOUT2 high).

3: enable - enables loading of drive select bits 4 and 5

4: drive select - low order of two decoded select bits

5: drive select - high order of two decoded select bits. Bits 4 and 5 are latched and decoded to select one of four drives as the recipient of all commands directed to the FDC system. If bit 3 (enable) is inactive, bits 4 and 5 are ignored in a command word and the previously selected drive is used.

6: Read - initiate reading. The address of the memory buffer has been preloaded into the FDC memory address register (see below) and the host system has positioned the selected disk at the desired track. The Read command causes the first byte of the buffer to be fetched and compared to the track ID read from the drive. A mismatch causes a Track error. The second byte of the buffer is fetched and specifies a Sector number and the FDC reads sector ID fields until a match occurs. The third buffer byte is loaded by the FDC with the address mark for the data field read, then 128 bytes are transferred from the drive to memory.

7: Write - initiates a write operation. Track and sector are identified as for a Read and a Track error aborts the operation. After positioning, using track and sector bytes from the memory buffer, the third byte is written as the address mark for the data field and the next 128 bytes transferred from memory to the drive.

Note that all bits, except disk select bits, are reset on the FDC at the completion or abort of a Read or Write command. All bits are cleared when the controller is reset (-IRESET, below).

Device address 126D (176Q, 7E hex) is decoded and made available to the host system on J1-56 as signal -IN126 whenever it is issued with the -IN strobe. It is suggested that the host system use the signal as a software issued restart command by implementing the logic equivalent of Figure 3. A further explanation of Figure 3 appears in the section on initializing the FDC below.

DMA INTERFACE

The DMA interface communicates directly with any compatible random access memory once a Read or Write command is initiated by the host system. This interface uses the DMA address register loaded by OUT devices 126D and 125D as a starting address and always employs 131 sequential bytes of memory for a disk transfer. When the FDC is ready to access memory for any single byte transfer, signal REQ (J2-55) is raised. Nothing occurs until signal ACK (J2-56) appears true, raised by the host memory system when a memory cycle is granted to the FDC. ACK should be raised within (30 - memory cycle time) microseconds of the leading edge of REQ in order to service the FDC in time. ACK must remain true during the entire memory cycle.

When ACK appears high at the FDC, REQ is lowered and the DMA address register is gated to the memory address bus MADi, and signal -WRITE is lowered if a memory write (disk read) is requested. Address lines are stable within 100 nanoseconds of the leading edge of ACK. If -WRITE remains high, a memory read (disk write) is in progress. For memory read, the host memory must gate the contents of the memory byte addressed by MADi onto the memory data out bus MDOUTi (8 bits). When the data is stable, signal ACK must be lowered. The trailing edge of ACK is used by the FDC to latch the data byte. Busses are then released by the FDC within 50 nanoseconds of the trailing edge of ACK.

If a memory write is requested, the memory address is also gated to the MADi bus when ACK appears. In addition, -WRITE is lowered and data to be written in memory is placed on the memory data input bus MDINi (8 bits). Once the host memory has captured the data and address, ACK should be lowered and the busses will be released.

The FDC requests 131 sequential bytes of data for each transfer. The first three bytes are disk address information: track number, sector number, and data address mark. The remaining 128 bytes are data. The FDC automatically increments the DMA address appropriately, formats data, and generates or checks CRC characters.

In summary, the FDC directly accesses up to 64 Kbytes of random access memory using a simple asynchronous handshaking protocol. Memory address, READ/WRITE, input data, and output data are used after a request is made and acknowledged indicating that a memory cycle is granted to the FDC. Memory buffers of 131 bytes are required for each transfer.

DISK INTERFACE

The disk interface is a set of signals on a separate 50 pin connector (J3) providing control and data paths to one to four drives.

A description of each available signal appears below. All are active low TTL level signals. An asterisk (*) next to the signal name indicates signals from the drive to the controller. A plus (+) indicates an optional signal not vital to the FDC operation. Refer to Appendix 1 for pinout of connector J3.

Device address 126D when strobed by the OUT signal loads the contents of the -DOUTi data bus into the most significant byte of the DMA address register. Data on the -DOUTi bus should be stable when the OUT strobe is issued.

Device address 125D (175Q, 7D hex) when strobed by the OUT signal loads the contents of the -DOUTi data bus into the least significant byte of the DMA address register.

In summary, the device interface provides address bits to activate the FDC, uses strobes -IN and OUT to synchronize the actions of the controller with a host system, and has data paths for status and control information. These paths are used by the FDC as follows:

STROBE	ADDRESS	HOST DATA IN	HOST DATA OUT
OUT	127D	none	command word
OUT	126D	none	MSByte DMA address
OUT	125D	none	LSByte DMA address
-IN	127D	status	none
-IN	126D	none	none (J1-56: -IN126)

	Name	Description
*+	-FILEINOP	disk file inoperative - an error condition from the drive detecting illegal signal conditions during write
+	-FIR	file inoperative reset - response to the FILEINOP condition from the host system via the command byte
*	-INDEX	index pulse indicating rotating diskette is at the beginning of a track
*	-READY	ready level indicating drive is in an operable condition(door closed, diskette up to speed, etc.)
	-DS0	disk select 0 - disk select lines are wired one line per drive
	-DS1	disk select 1
	-DS2	disk select 2
	-DS3	disk select 3
	-DIR	direction - indicates direction head should move in response to a -STEP pulse. A low (active) on -DIR indicates stepping toward diskette center, a high towards diskette edge (Track 0).
	-STEP	step - 10 microsecond pulse to drive when a head step in the indicated direction is required
	-WRITEDATA	interleaved clock and data pulses to be written onto diskette
	-WG	write gate - signal windowing WRITEDATA to enable drive for writing
*	-TRKZRO	track zero - active when drive detects head positioned at track 00
*+	-READATA	interleaved data and clock pulses from drive
*	-SD	separated data pulses from drive
*	-SC	separated clock pulses from drive

The FDC requires that the drive electronics provide clock pulses on the -SC line and data pulses without clocks on the -SD line. -READATA is unused. The -STEP pulse may be longer than 10 microseconds.

INITIALIZATION

The sample circuitry in Figure 3 illustrates the initialization requirements for the FDC. System wide reset circuitry should place a TTL low signal (-IRESET) on J1-55 to the FDC and preset signal BOOTSTRAP. Active low -BOOTSTRAP must be available to the FDC on J1-57. When the FDC completes its bootstrap procedure of reading track zero, sector one into DMA addresses 00-7F hex, it will issue 50 nanosecond pulse -IOF . In fact, -IOF is issued at the completion of every disk input or output operation. -IOF is used to clear the BOOTSTRAP latch which in turn may be used to signal the host system to begin execution of the bootstrap program now in low memory. BOOTSTRAP may be invoked under program control by issuing an -IN strobe with device address 126D. Signal -IN126 will appear on J1-56 and set BOOTSTRAP on its trailing edge.

POWER SYSTEM

+5 volts DC should be wired to pins 1,2,3, and 4 of both connectors J1 and J2. 2.5 amps may be drawn by the FDC. Pins 83, 84, 85, and 86 of both connectors should be grounded. All odd numbered pins on connector J3 are grounded.

WRITE PROTECT

The FDC provides write protection for the disk drive selected by signal -DS0 or all drives(jumper selectable). In order to allow writing, the DZPROT signal on J1-9 must be grounded (TTL "0") by the host system.

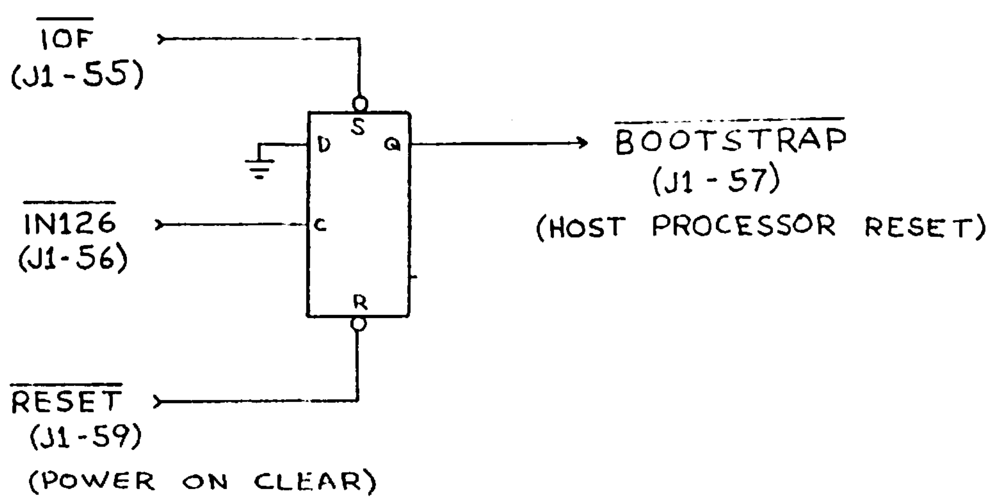

Figure 3. Initialization Circuitry.

SOFTWARE

The following system software control by the host CPU is required when using the FDC-1:

1. Software must step the head to the desired track (using STEP and DIRECTION bits of the command byte) before reading or writing.

2. The initial DMA address must be loaded (2 bytes) prior to issuing a READ or WRITE command.

3. The three bytes in memory starting at the DMA address must be set to the desired track, sector, and address mark (for write).

4. A simple retry scheme should be implemented to attempt recovery from disk errors. (For track error, seek track Ø and then desired track before retry).

Figures 4 to 7 contain flowcharts for the following routines:

HOME	-	seek track zero
STEP	-	step one track in or out
SEEK	-	seek any valid track
READ	-	read one sector
WRITE	-	write one sector

Assembly language code for the above routines is available for the 8080. Also available is a complete Disk Operating System for the 8080.

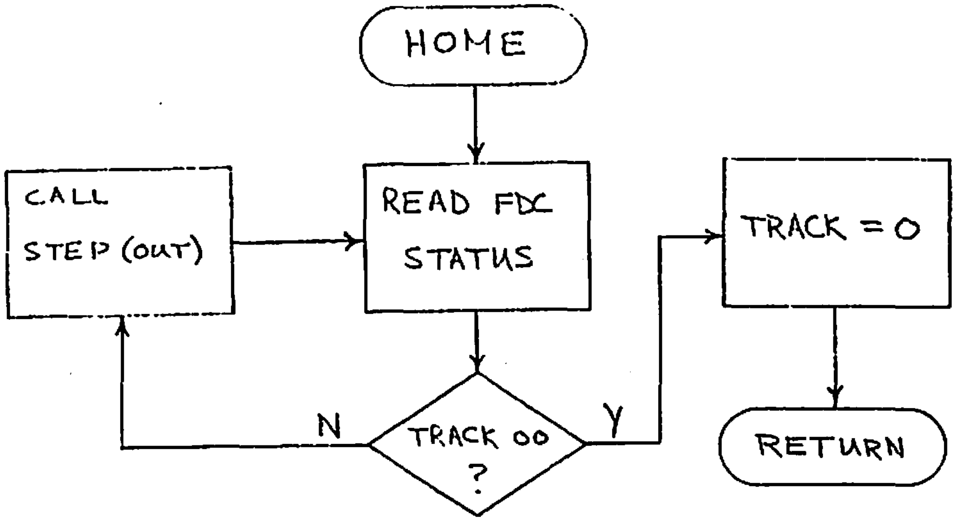

Figure 4. Subroutine HOME.

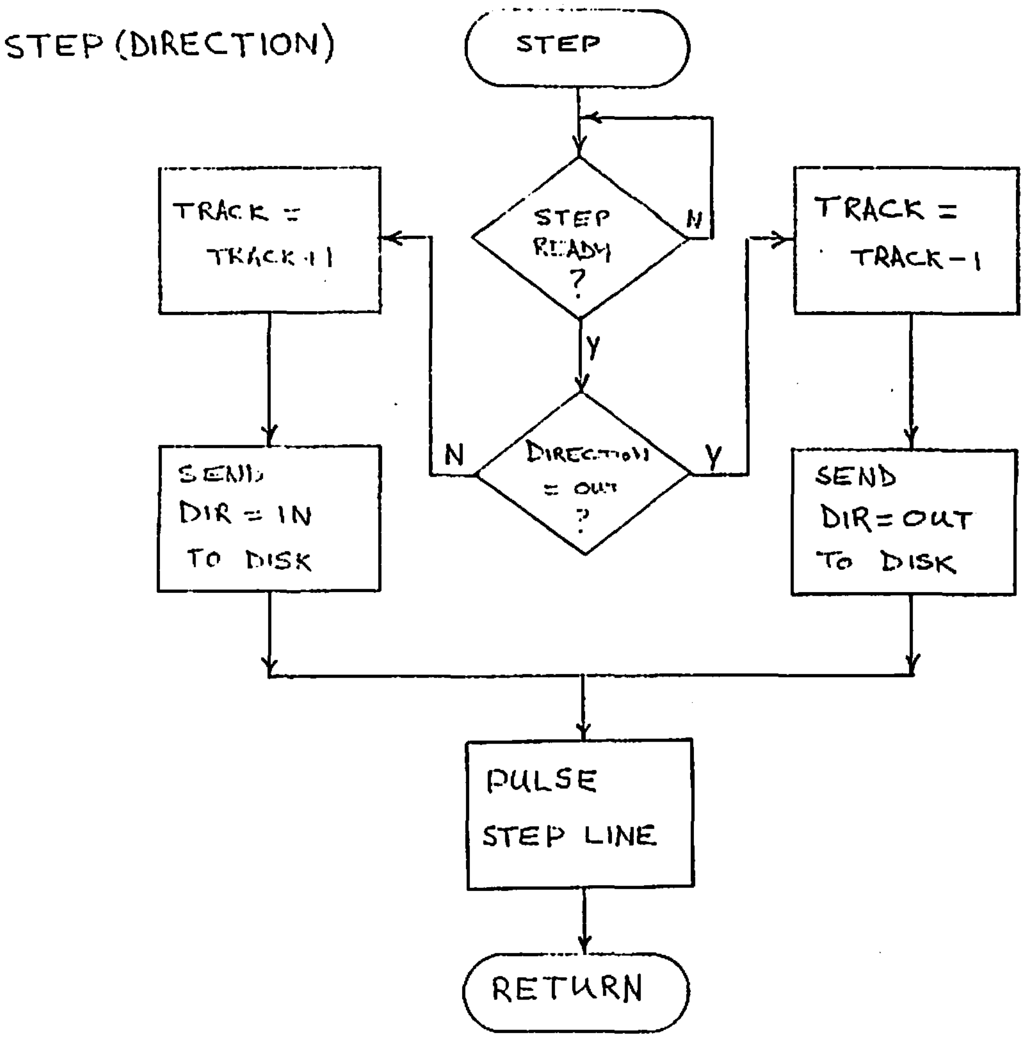

Figure 5. Subroutine STEP.

SEEK (N,ERR) MOVE HEAD TO TRACK N

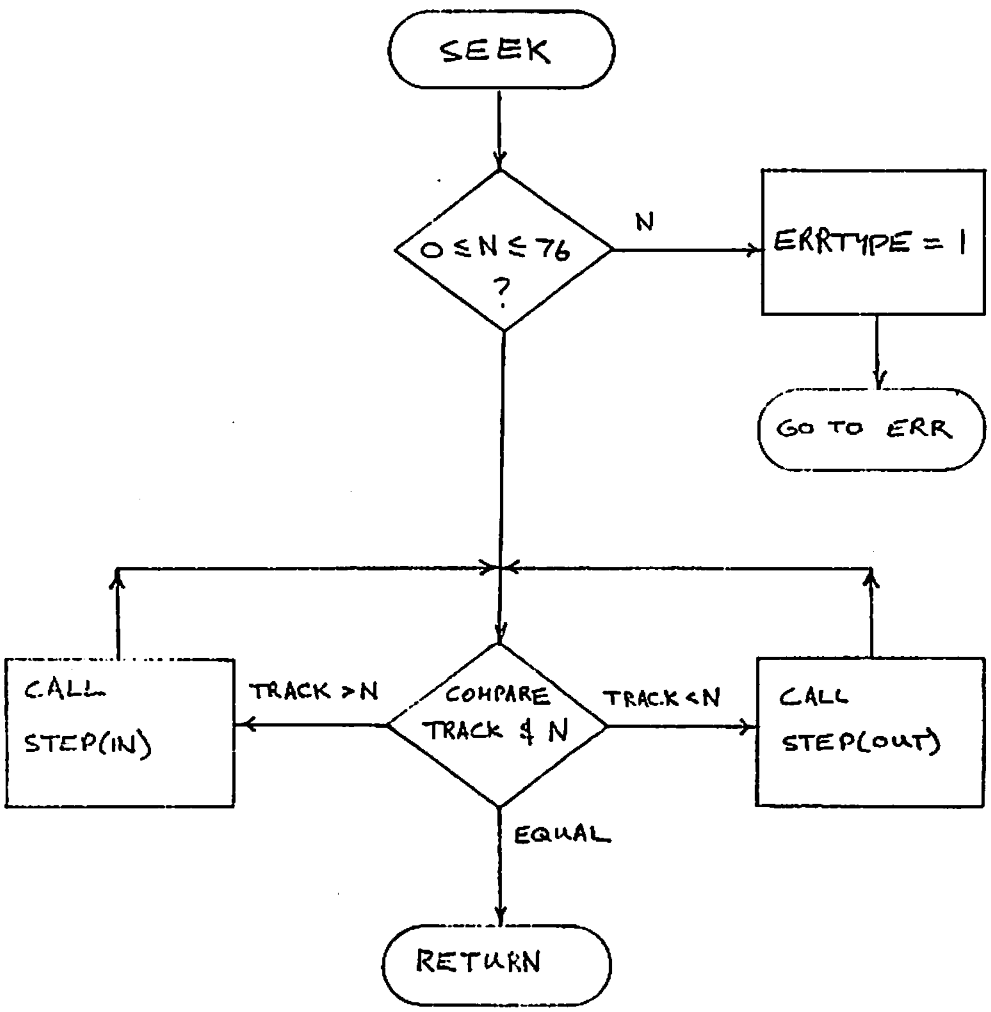

Figure 6. Subroutine SEEK.

READ or WRITE (TRK, SECT, BUF, ERR)

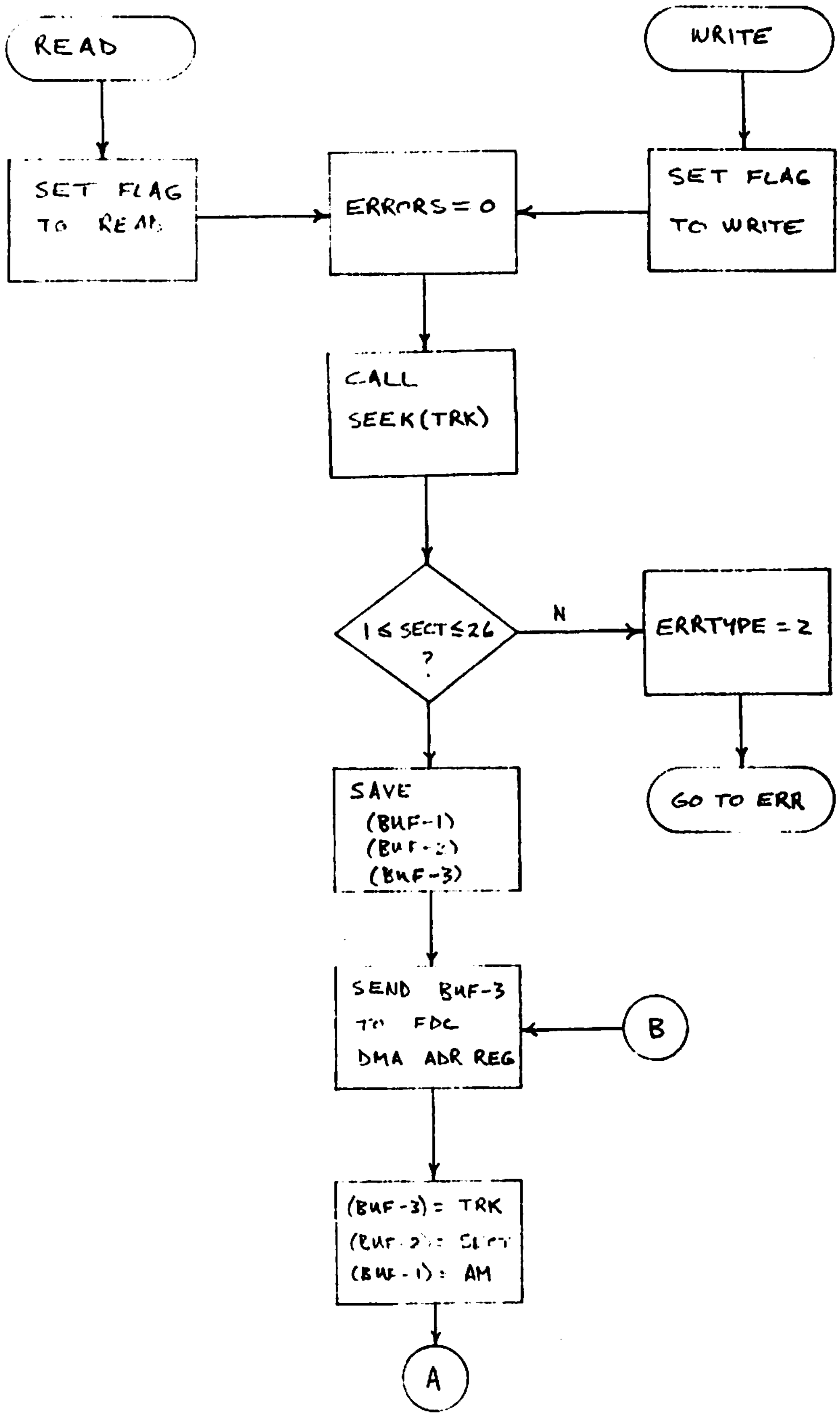

Figure 7. Subroutines READ and WRITE.

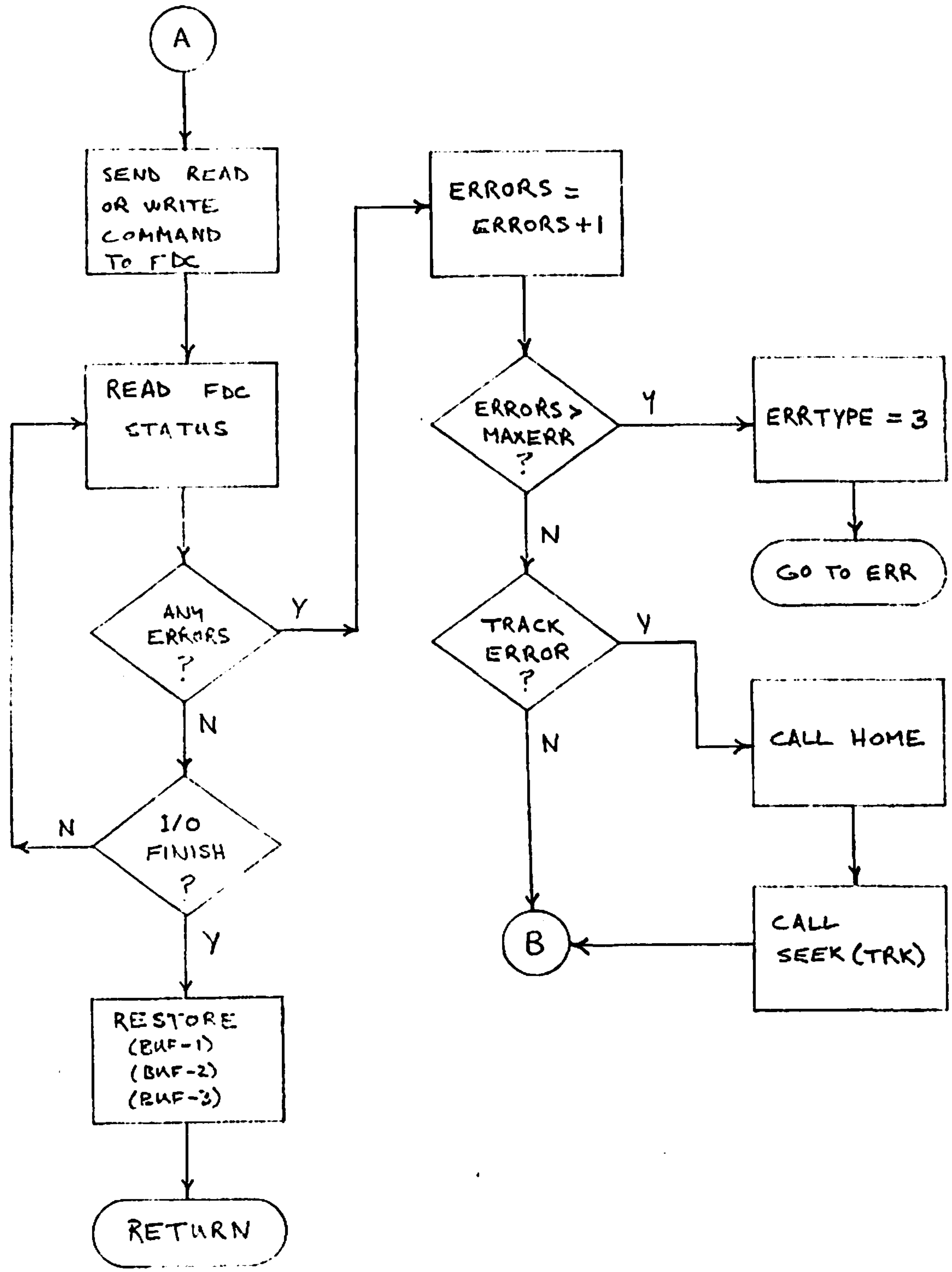

Figure 7a. Subroutines READ and WRITE (cont).

APPENDIX 1 EDGE CONNECTOR PINOUTS

J1 TOP EDGE CONNECTOR

1 +5 VDC	2 +5 VDC
3 +5 VDC	4 +5 VDC
5	6
7	8
9	10
11	12
13	14
15	16
17 GROUND	18 GROUND
19	20
21 -DEV0 (device address bus)	22 -DEV1
23 -DEV2	24 -DEV3
25 -DEV4	26 -DEV5
27 -DEV6	28 -DEV7
29 -DOUT0 (data out buss)	30 -DOUT1
31 -DOUT2	32 -DOUT3
33 -DOUT4	34 -DOUT5
35 -DOUT6	36 -DOUT7
37 DIN0 (data in buss)	38 DIN1
39 DIN2	40 DIN3
41 DIN4	42 DIN5
43 DIN6	44 DIN7
45 -IN (in strobe)	46 OUT (out strobe)
47	48
49	50
51	52
53	54
55 -IRESET (initial reset)	56 -IN126
57 -BOOTSTRAP	58
59 -IOF	60
61	62
63	64
65	66
67	68
69	70
71	72
73	74
75	76
77	78
79	80
81	82
83 GROUND	84 GROUND
85 GROUND	86 GROUND

J2 BOTTOM EDGE CONNECTOR

1 + 5 VDC	2 + 5 VDC
3 + 5 VDC	4 + 5 VDC
5	6
7	8
9	10
11	12
13	14
15	16
17	18
19	20
21 MDIN0 (memory data in)	22 MDIN1
23 MDIN2	24 MDIN3
25 MDIN4	26 MDIN5
27 MDIN6	28 MDIN7
29 MAD0 (memory address buss)	30 MAD1
31 MAD2	32 MAD3
33 MAD4	34 MAD5
35 MAD6	36 MAD7
37 MAD8	38 MAD9
39 MAD10	40 MAD11
41 MAD12	42 MAD13
43 MAD14	44 MAD15
45	46
47 MDOUT0 (memory data out)	48 MDOUT1
49 MDOUT2	50 MDOUT3
51 MDOUT4	52 MDOUT5
53 MDOUT6	54 MDOUT7
55 REQ	56 ACK
57	58
59	60
61	62
63 -WRITE (read)	64
65	66
67 GROUND	68 GROUND
69	70
71	72
73	74
75	76
77	78
79	80
81	82
83 GROUND	84 GROUND
85 GROUND	86 GROUND

J3 DISK DRIVE CONNECTOR

The controller uses a 50 connector cable for communication with the disk drives. This cable is designated J3 in the system. Pinout for the cable is:

PIN	SIGNAL NAME
2	
4	
6	
8	
10	
12	
14	
16	-FILEINOP (disk file inoperative)
18	-FIR (file inoperative reset)
20	-INDEX
22	-READY
24	
26	-DS0 (disk select 0)
28	-DS1
30	-DS2
32	-DS3
34	-DIR (direction select)
36	-STEP
38	-WRITEDATA
40	-WG (write gate)
42	-TRKZR0 (track 0)
44	
46	-READATA
48	-SD (separated data)
50	-SC (separated clock)

ALL ODD PINS: GROUND

SA800/801
Diskette Storage Drive

Original Equipment
Manufacturers Manual

SHUGART ASSOCIATES

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SA800

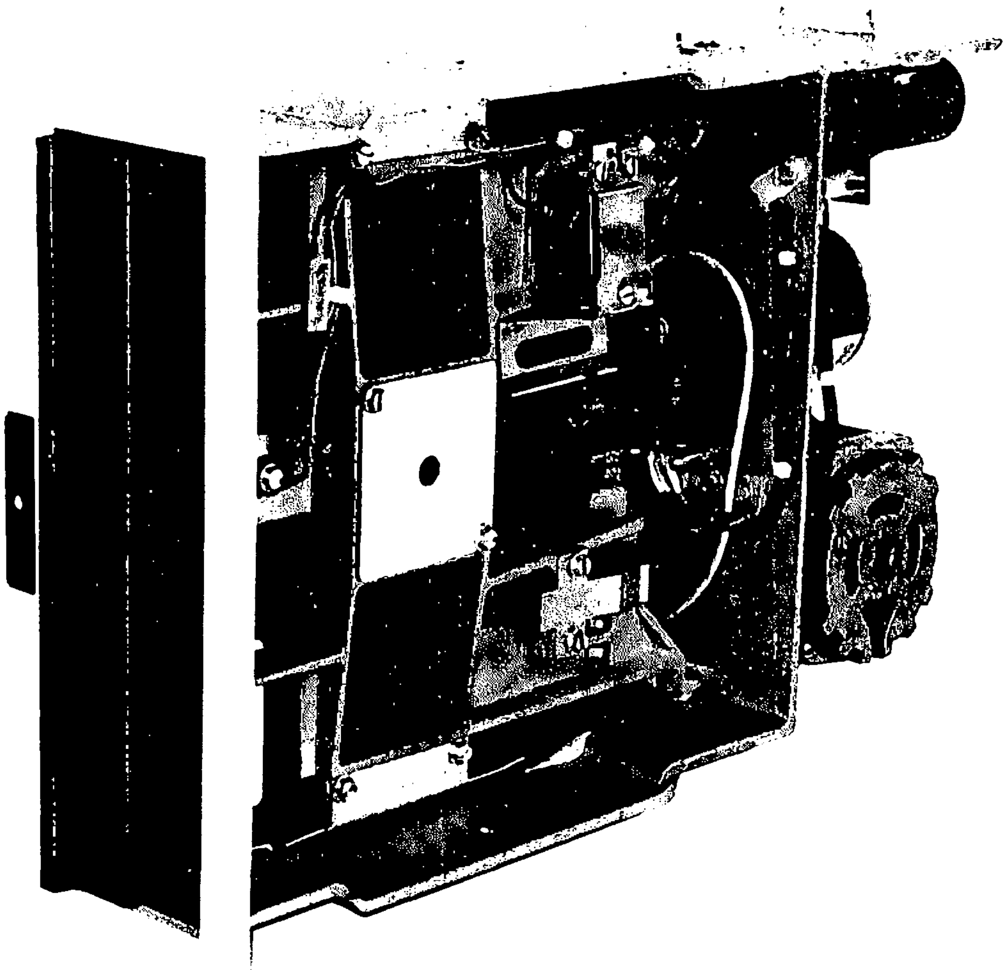


Figure 1. SA800/801 Diskette Storage Drive

1.0 INTRODUCTION

1.1 General Description

The SA800/801 are enhanced versions of the successful SA900/901 Diskette Storage Drive. The SA800/801 provides the customer with a mature and reliable product, manufactured to the same high standard of excellence as the 900/901, but with additional features.

The SA800 Diskette Storage Drive can read and write diskettes for interchange with other SA800's, the SA900, IBM 3741, 3742 or 3540 and with the new IBM System 32.

The SA801 provides the same features as the SA800 with additional flexibility for those requirements which preclude IBM compatibility.

The SA800/801 Diskette Storage Drives have as standard features: a patented diskette clamping/registration design which eliminates the possibility of damage to the diskette due to misregistration and guarantees over 30,000 interchanges with each diskette; single and double density capability on the same drive for the same price; a proprietary ceramic R/W head designed and manufactured by Shugart Associates to provide media life exceeding 3.5 million passes/track and head life exceeding 15,000 hours; an activity light which indicates drive in use; and ribbon cable or twisted pair connector for ease of packaging. All of these features and more are available with the SA800/801.

SA800/801 Diskette Storage Drives provide the system designer solutions to his applications requirements with greater performance and reliability than cassette or cartridge drives, and lower cost with increased function over card I/O and reel-to-reel tape drives.

Applications for the SA800/801 Diskette Storage Drive are key entry systems, point of sale recording systems, batch terminal data storage, microprogram load and error logging, minicomputer program and auxiliary data storage, word processing systems and data storage for small business systems.

The SA100 Diskette, IBM Diskette or equivalent, can be read and written interchangeably between any SA800 and IBM 3741/42, 3747 and 3540. The SA101 Diskette can be read or written interchangeably on any SA801.

1.2 Specification Summary

1.2.1 Performance Specifications

Capacity	Single Density	Double Density
Unformatted		
Per Disk	3.2 megabits	6.4 megabits
Per Track	41.7 kilobits	83.4 kilobits
IBM Format		
Per Disk	2.0 megabits	n/a
Per Track	26.6 kilobits	n/a
Transfer Rate	250 kilobits/sec	500 kilobits/sec
Latency (average)	83 ms	83 ms
Access Time		
Track to Track	10 ms	10 ms
Average	260 ms	260 ms
Settling Time	8 ms	8 ms
Head Load Time	35 ms	35 ms

1.2.2 Functional Specifications

	Single Density	Double Density
Rotational Speed	360 rpm	360 rpm
Recording Density		
(inside track)	3200 bpi	6400 bpi
Flux Density	6400 fci	6400 fci
Track Density	48 tpi	48 tpi
Tracks	77	77
Physical Sectors		
SA800	0	0
SA801	32/16/8	32/16/8
Index	1	1
Encoding Method	FM	M^2FM
Media Requirements		
SA800	SA100/IBM Diskette	SA100/IBM Diskette
SA801	SA101	SA101

1.2.3 Physical Specifications

Environmental Limits
- Ambient Temperature = 50°F to 100°F
- Relative Humidity = 20% to 80%
- Maximum Wet Bulb = 78°F

AC Power Requirements
- 50/60 Hz ± 0.5 Hz
- 100/115 VAC Installations = 90 to 127 V @ .4A typical
- 200/230 VAC Installations = 180 to 253 V @ .2A typical

DC Voltage Requirements
- +24 VDC ± 5% 1.3A typical
- + 5 VDC ± 5% 0.8A typical
- - 5 VDC ± 5% .05A typical (option -7 to -16 VDC)

Mechanical Dimensions
- Width = 4 5/8 in.
- Height = 9 1/2 in.
- Depth = 14 1/4 in.
- Weight = 13.0 lbs.

Heat Dissipation = 245 BTU/hr. typical

1.2.4 Reliability Specifications

MTBF:	5000 POH under heavy usage 8000 POH under typical usage.
PM:	Every 5000 POH under heavy usage. Every 15,000 POH under typical usage.
MTTR:	30 minutes.
Component Life:	15,000 POH.
Error Rates:	
Soft Read Errors:	1 per 10^9 bits read.
Hard Read Errors:	1 per 10^{12} bits read.
Seek Errors:	1 per 10^6 seeks.
Media Life:	
Passes per Track	3.5×10^6
Insertions:	30,000+

2.0 FUNCTIONAL CHARACTERISTICS

2.1 General Operation

The SA800/801 Diskette Storage Drive consists of read/write and control electronics, drive mechanism, read/write head, track positioning mechanism, and the removable diskette. These components perform the following functions:

> Interpret and generate control signals.
> Move read/write head to the selected track.
> Read and write data.

The relationship and interface signals for the internal functions of the SA800/801 are shown in Figure 2.

The Head Positioning Actuator positions the read/write head to the desired track on the diskette. The Head Load Actuator loads the diskette against the read/write head and data may then be recorded or read from the diskette.

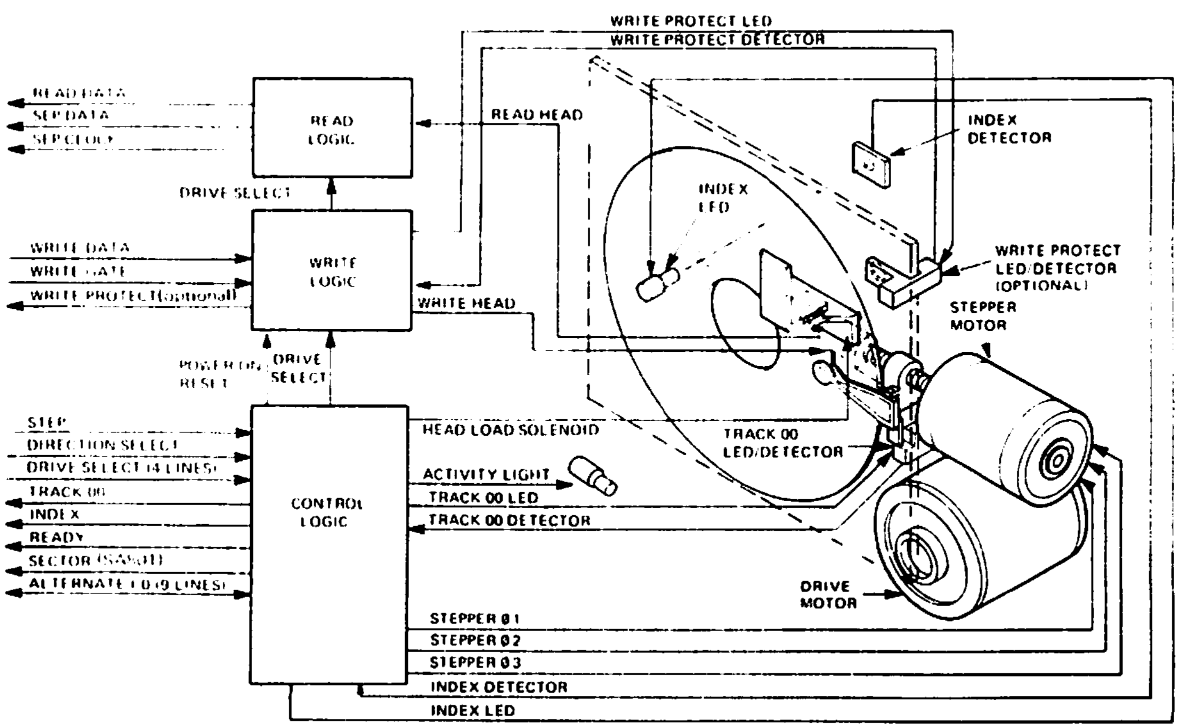


Figure 2. SA800/801 Functional Diagram

2.2 Read/Write and Control Electronics

The electronics are packaged on one PCB. The PCB contains:

1. Index Detector Circuits (Sector/Index for 801)
2. Head Position Actuator Driver
3. Head Load Actuator Driver
4. Read/Write Amplifier and Transition Detector
5. Data/Clock Separation Circuits
6. Write Protect
7. Drive Ready Detector Circuit
8. Drive Select Circuits

2.3 Drive Mechanism

The Diskette drive motor rotates the spindle at 360 rpm through a belt-drive system. 50 or 60 Hz power is accommodated by changing the drive pulley and belt. A registration hub, centered on the face of the spindle, positions the Diskette. A clamp that moves in conjunction with the cartridge guide fixes the Diskette to the registration hub.

2.4 Positioning Mechanism

An electrical stepping motor (Head Position Actuator) and lead screw positions the read/write head. The stepping motor rotates the lead screw clockwise or counterclockwise in 15° increments. A 15° rotation of the lead screw moves the read/write head one track position. The using system increments the stepping motor to the desired track.

2.5 Read/Write Head

The SA800/801 head is a single element ceramic read/write head with straddle erase elements to provide erased areas between data tracks. Thus normal interchange tolerances between media and drives will not degrade the signal to noise ratio and insures Diskette interchangeability.

The read/write head is mounted on a carriage which is located on the Head Position Actuator lead screw. The Diskette is held in a plane perpendicular to the read/write head by a platen located on the base casting. This precise registration assures perfect compliance with the read/write head. The Diskette is loaded against the head with a load pad actuated by the head load solenoid.

The read/write head is in direct contact with the Diskette. The head surface has been designed to obtain maximum signal transfer to and from the magnetic surface of the Diskette with minimum head/Diskette wear.

2.6 Recording Format

The format of the data recorded on the disk is totally a function of the host system, and can be designed around the users application to best take advantage of the total available bits that can be written on any one track.

For a detailed discussion of various recording formats, the systems designer should read one of the following:

1. IBM Compatibility Manual
   Publication number SA0006-5
2. Shugart Associates Double Density Design Guide
   Publication number SA0008-0
3. SA801/901 Track Formats
   Publication number SA0010-0

3.0 FUNCTIONAL OPERATIONS

3.1 Power Sequencing

Applying AC and DC power to the SA800/801 can be done in any sequence, however, once AC power has been applied, a 2 second delay must be introduced before any Read or Write operation is attempted. This delay is for stabilization of the Diskette rotational speed. Also, after application of DC power, a 90 millisecond delay must be introduced before a Read, Write, or Seek operation or before the control output signals are valid. After powering on, initial position of the R/W head with respect to data tracks is indeterminant. In order to assure proper positioning of the R/W head prior to any read/write operation after powering on, a Step Out operation should be performed until the Track 00 indicator becomes active.

3.2 Drive Selection

Drive selection occurs when a drive's Drive Select line is activated. Only the drive with this line active will respond to input lines or gate output lines. Under normal operation, the Drive Select line will load the R/W head, apply power to the stepper motor, enable the input lines and activate the output lines. Optional modes of operation are available to the user by cutting or connecting traces. Reference section 7 for these user installable features.

3.3 Track Accessing

Seeking the R/W head from one track to another is accomplished by:

a. Activating Drive Select line.

b. Selecting desired direction utilizing Direction Select line.

c. Write Gate being inactive.

d. Pulsing the Step line.

Multiple track accessing is accomplished by repeated pulsing of the Step line until the desired track has been reached. Each pulse on the Step line will cause the R/W head to move one track either in or out depending on the Direction Select line. Head movement is initiated on the trailing edge of the Step Pulse.

3.3.1 Step Out

With the Direction Select line at a plus logic level (2.5V to 5.25V) a pulse on the Step line will cause the R/W head to move one track away from the center of the disk. The pulse(s) applied to the Step line and the Direction Select line must have the timing characteristics shown in Figure 3.

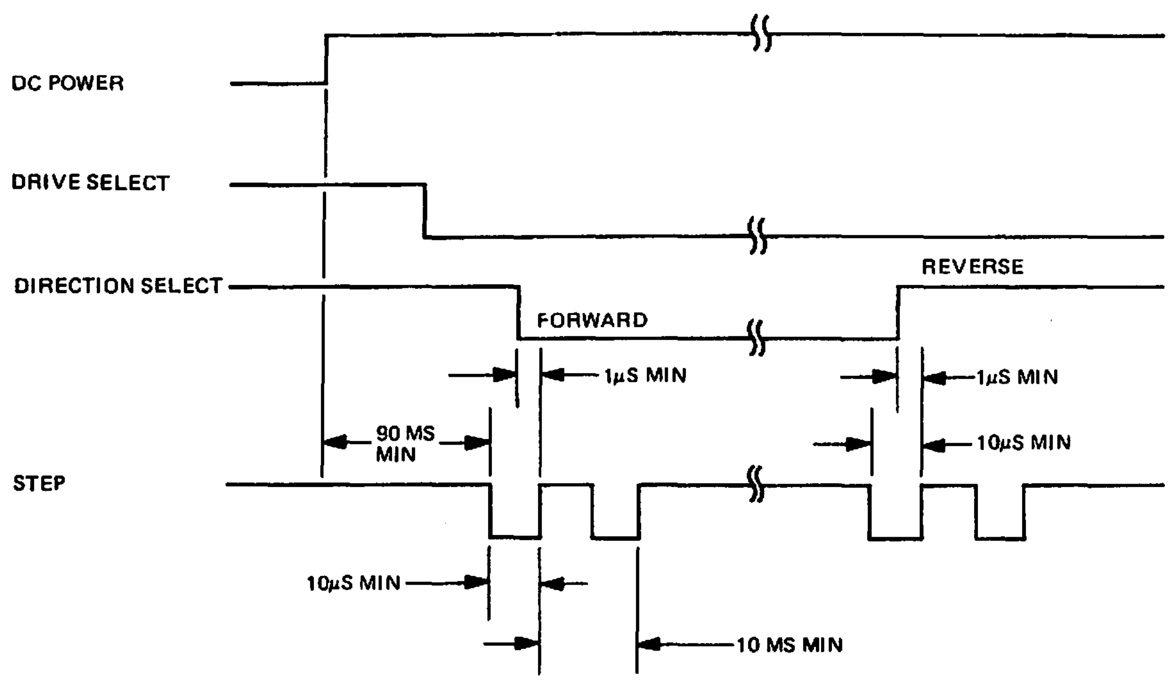
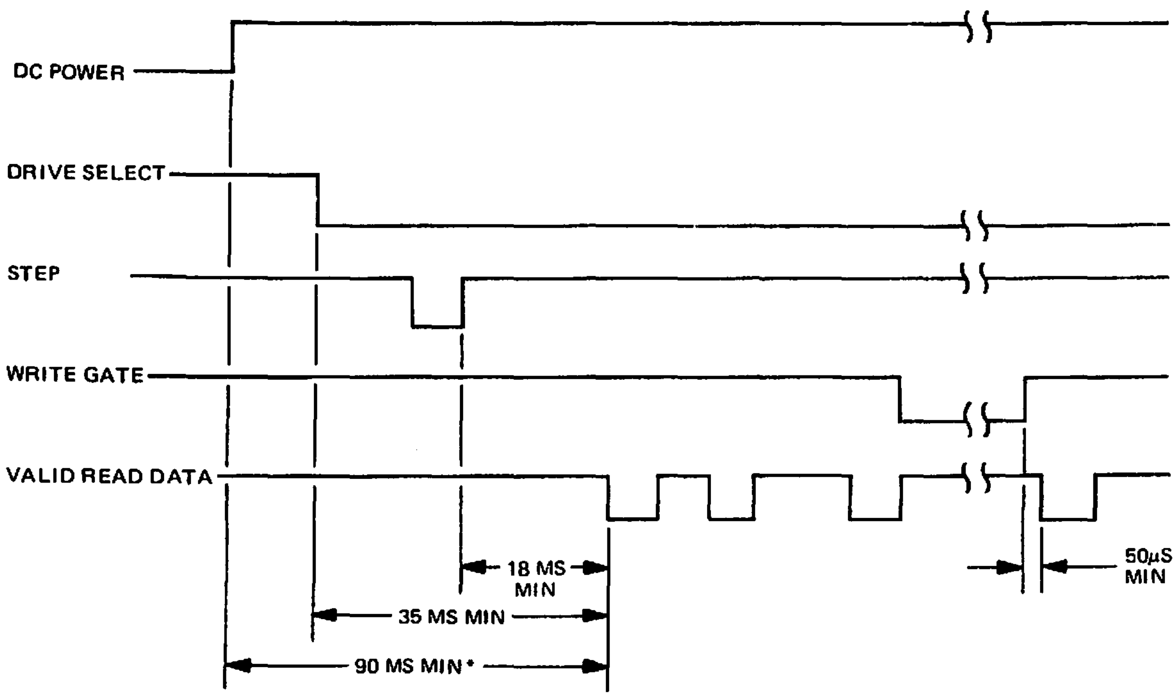


Figure 3. Track Access Timing



* 2 SECONDS IF AC AND DC POWER ARE APPLIED AT SAME TIME

Figure 4. Read Initiate Timing

3.3.2 Step In

With the Direction Select line at a minus logic level (0V to .4V), a pulse on the Step line will cause the R/W head to move one track closer to the center of the disk. The pulse(s) applied to the Step line must have the timing characteristics shown in Figure 3.

3.4 Read Operation

Reading data from the SA800/801 Diskette Storage drive is accomplished by:

a. Activating Drive Select line.

b. Write Gate being inactive.

The timing relationships required to initiate a read sequence are shown in Figure 4. These timing specifications are required in order to guarantee that the R/W head position has stabilized prior to reading.

The timing of the read signals, Read Data, Separated Data, and Separated Clock are shown in Figure 5.

3.5 Write Operation

Writing data to the SA800/801 is accomplished by:

a. Activating the Drive Select line.

b. Activating the Write Gate line.

c. Pulsing the Write Data line with the data to be written.

The timing relationships required to initiate a write data sequence are shown in Figure 6. These timing specifications are required in order to guarantee that the R/W head position has stabilized prior to writing.

The timing specifications for the Write Data pulses are shown in Figure 7.

3.6 Sequence of Events

The timing diagram shown in Figure 8 shows the necessary sequence of events with associated timing restrictions for proper operation.

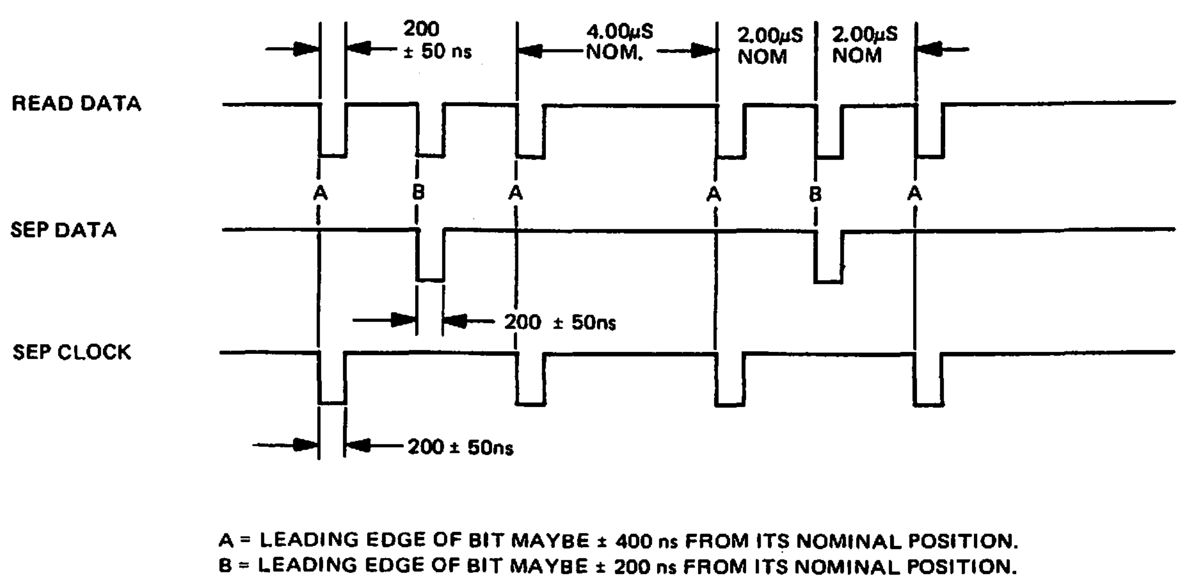


Figure 5. Read Signal Timing

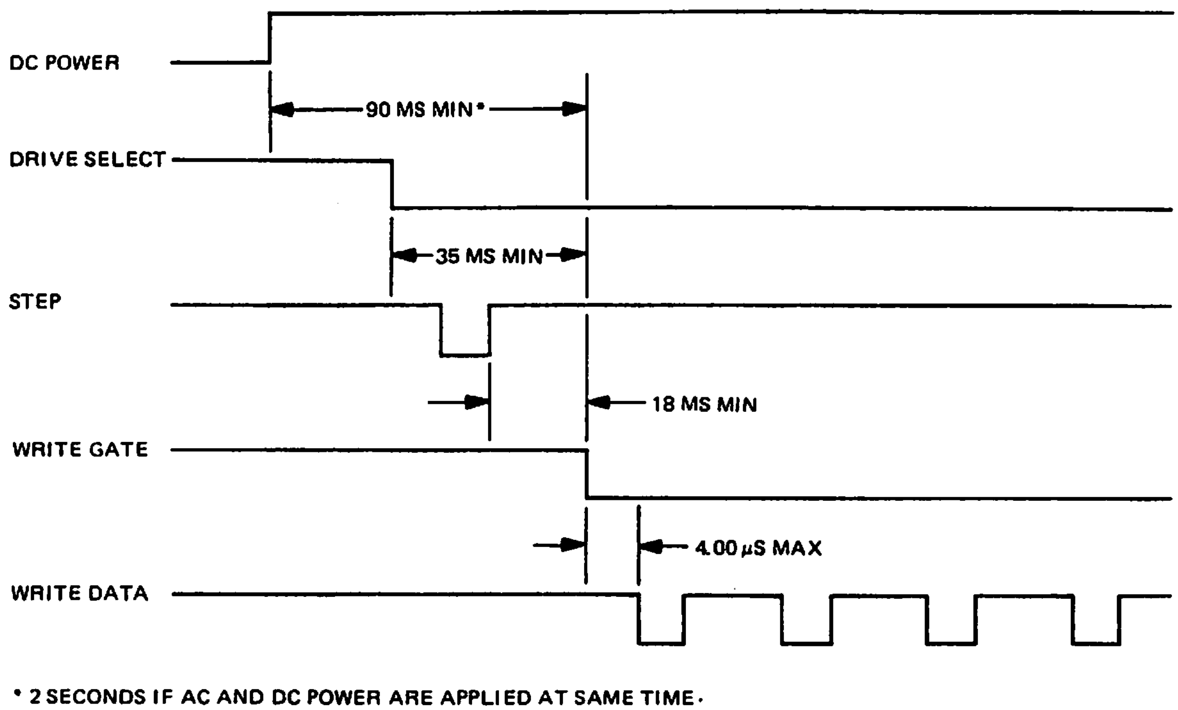


Figure 6. Write Initiate Timing

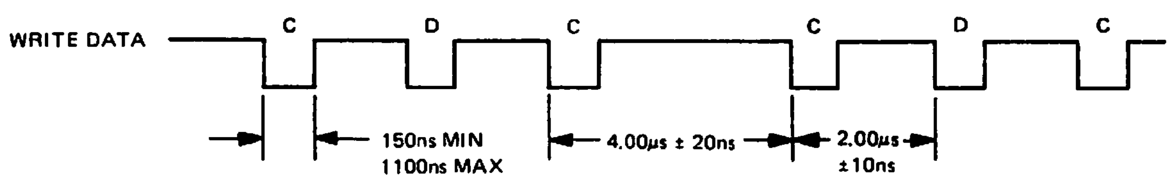
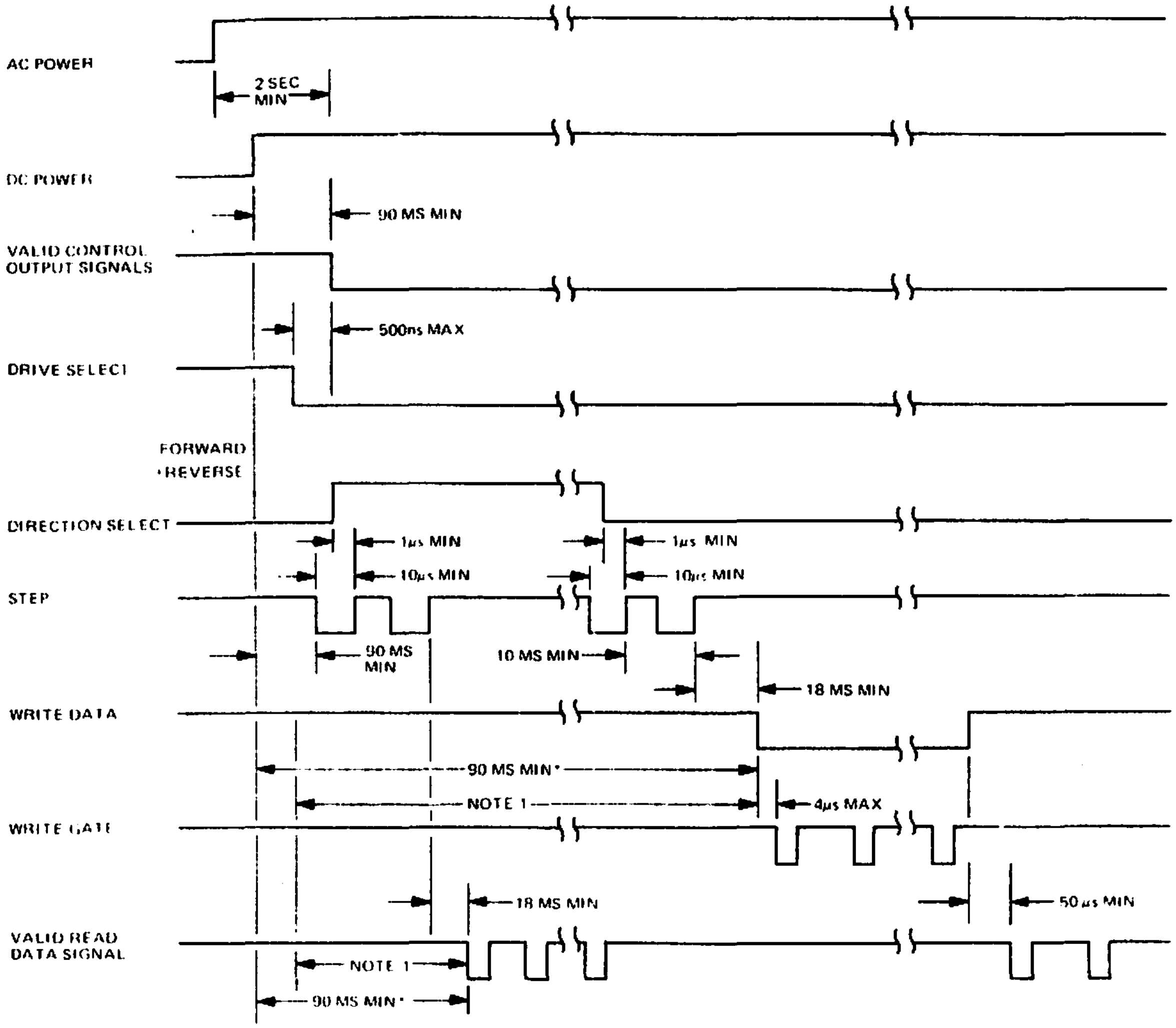


Figure 7. Write Data Timing



* 2 SECONDS IF AC AND DC POWER ARE APPLIED AT SAME TIME

NOTE 1 35ms minimum delay must be introduced after Drive Select to allow for proper head load settling. If stepper power is to be applied independent of Head Load, then an 8ms minimum delay must be introduced to allow for stepper settling. See section 7 on optional customer installable features.

Figure 8. General Control and Data Timing Requirements

4.0 ELECTRICAL INTERFACE

The interface of the SA800/801 Diskette drive can be divided into two categories:

1. Signal
2. Power

The following sections provide the electrical definition for each line.

Reference Figure 9 for all interface connections.

4.1 Signal Interface

The signal interface consists of two categories:

1. Control
2. Data transfer

All lines in the signal interface are digital in nature and either provide signals to the drive (input), or provide signals to the host (output), via interface connector P1/J1.

4.1.1 Input Lines

There are ten (10) signal input lines, eight (8) are standard and two (2) are user installable options (reference section 7).

The input signals are of two types, those intended to be multiplexed in a multiple drive system and those which will perform the multiplexing. The input signals to be multiplexed are:

1. Direction Select
2. Step
3. Write Data
4. Write Gate

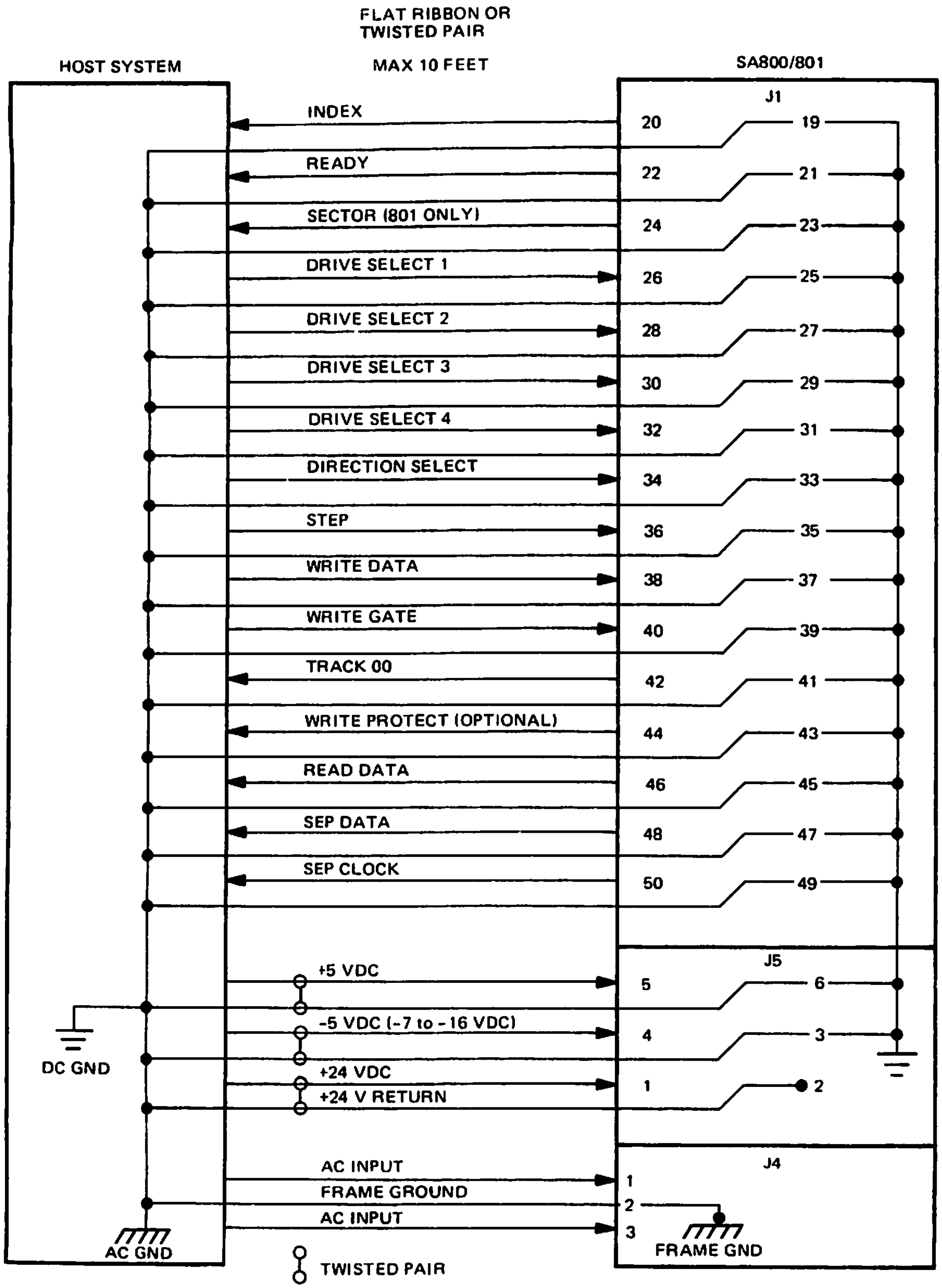
The input signals which are intended to do the multiplexing are:

1. Drive Select 1
2. Drive Select 2
3. Drive Select 3
4. Drive Select 4

The input lines have the following electrical specifications. Reference Figure 10 for the recommended circuit.

True = Logical zero = Vin ±0.0V to +0.4V
@ Iin = 40 ma (max)

False = Logical one = Vin +2.5V to +5.25V
@ Iin = 0 ma (open)
Input Impedence = 150 ohms



NOTE: Not shown are the nine Alternate I/O connections. The connections for these lines are on pins 2, 4, 6, 8, 10, 12, 14, 16, and 18. Signal return for these lines are on pins 1, 3, 5, 7, 9, 11, 13, 15, 17, and 19 respectively. Reference section 7 for uses of these lines.

Figure 9. Interface Connections

4.1.1.1 Input Line Termination

The SA800/801 has been provided with the capability of terminating the four input lines, which are meant to be multiplexed, by jumpering traces. The four lines and their respective jumpering traces are:

1. Direction Select . . . . Trace "T3"
2. Step. Trace "T4"
3. Write Data . . . . Trace "T5"
4. Write Gate . . . . Trace "T6"

In order for the drive to function properly, the last drive on the interface must have these four lines terminated. Termination of these four lines can be accomplished by either of two methods.

1. Install jumpers (on the last drive) across the posts provided on the PCB. The jumpers may be installed by soldering, wire wrapping, or by use of a shorting plug Shugart P/N 15648 or AMP P/N 530153-2. The shorting plugs are not supplied with each drive unless it is specified on the order.
2. External termination may be used provided the terminator is beyond the last drive. Each of the four lines should be terminated by using a 150 ohm, ¼ watt resistor, pulled up to +5 VDC.

4.1.1.2 Drive Select 1 - 4

Drive Select when activated to a logical zero level, activates the multiplexed I/O lines and loads the R/W head. In this mode of operation only the drive with this line active will respond to the input lines and gate the output lines.

Four separate input lines, Drive Select 1, Drive Select 2, Drive Select 3, and Drive Select 4, are provided so that up to four drives may be multiplexed together in a system and have separate Drive Select lines. Traces 'DS1', 'DS2', 'DS3', and 'DS4' have been provided to select which Drive Select line will activate the interface signals for a unique drive. As shipped from the factory, a shorting plug is installed on 'DS1'. To select another Drive Select line, this plug should be moved to the appropriate 'DS' pin. For additional methods of selecting drives, see section 7.1.

4.1.1.3 Direction Select

This interface line is a control signal which defines direction of motion the R/W head will take when the Step line is pulsed. An open circuit or logical one defines the direction as "out" and if a pulse is applied to the Step line the R/W head will move away from the center of the disk. Conversely, if this input is shorted to ground or a logical zero level, the direction of motion is defined as "in" and if a pulse is applied to the step line, the R/W head will move towards the center of the disk.

4.1.1.4 Step

This interface line is a control signal which causes the R/W head to move with the direction of motion as defined by the Direction Select line.

The access motion is initiated on each logical zero to logical one transition, or the trailing edge of the signal pulse. Any change in the Direction Select line must be made at least 1μs before the trailing edge of the Step pulse. Refer to Figure 3 for these timings.

4.1.1.5 Write Gate

The active state of this signal, or logical zero, enables Write Data to be written on the diskette. The inactive state, or logical one, enables the read data logic (Separated Data, Separated Clock, and Read Data) and stepper logic. Refer to Figure 6 for timings.

4.1.1.6 Write Data

This interface line provides the data to be written on the diskette. Each transition from a logical one level to a logical zero level, will cause the current through the R/W head to be reversed thereby writing a data bit. This line is enabled by Write Gate being active. Refer to Figure 7 for timings.

4.1.1.7 Head Load (Optional input trace 'C')

This customer installable option, when activated to a logical zero level and the diskette access door is closed, will load the R/W head load pad against the diskette. Refer to section 7 for uses and method of installation.

4.1.1.8 In Use (Optional input trace 'D')

This customer installable option, when activated to a logical zero level will turn on the Activity LED in the door push button. This signal is an "OR" function with Drive Select. Refer to section 7.8 for uses and method of installation.

4.1.2 Output Lines

There are seven (7) output lines from the SA800 and eight (8) from the SA801. There also is one (1) optional output line from the SA800/801.

The output signals are driven with an open collector output stage capable of sinking a maximum of 40 ma at a logical zero level or true state with a maximum voltage of 0.4V measured at the driver. When the line driver is in a logical one or false state the driver is off and the collector current is a maximum of 250 microamperes.

Refer to Figure 10 for the recommended circuit.

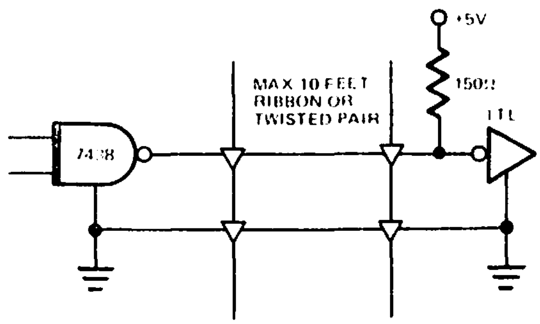


Figure 10. Interface Signal Driver/Receiver

4.1.2.1 Track 00

The active state of this signal, or a logical zero indicates when the drives R/W head is positioned at track zero (the outer most track) and the access circuitry is driving current through phase one of the stepper motor. This signal is at a logical one level, or false state, when the selected drives R/W head is not at track 00.

4.1.2.2 Index

This interface signal is provided by the drive once each revolution of the diskette (166.67ms) to indicate the beginning of the track. Normally this signal is a logical one and makes the transition to the logical zero level for a period of 1.7ms (0.4ms on SA801) once each revolution. The timing for this signal is shown in Figure 11.

To correctly detect Index at the control unit, Index should be false at Drive Select time, that is, the CU should see the transition from false to true after the drive has been selected.

For additional methods of detecting Index, refer to section 7.6.

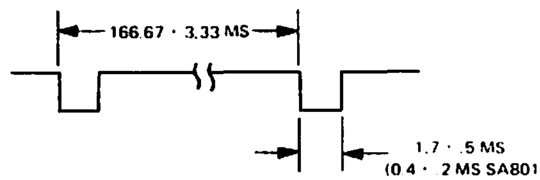


Figure 11. Index Timing

4.1.2.3 Sector (SA801 only)

This interface signal is provided by the drive 32 times each revolution. Normally, this signal is a logical one and makes the transition to a logical zero for a period of 0.4ms each time a sector hole on the Diskette is detected. Figure 12 shows the timing of this signal and its relationship to the Index pulse.

For additional methods of detecting Sector refer to section 7.7.

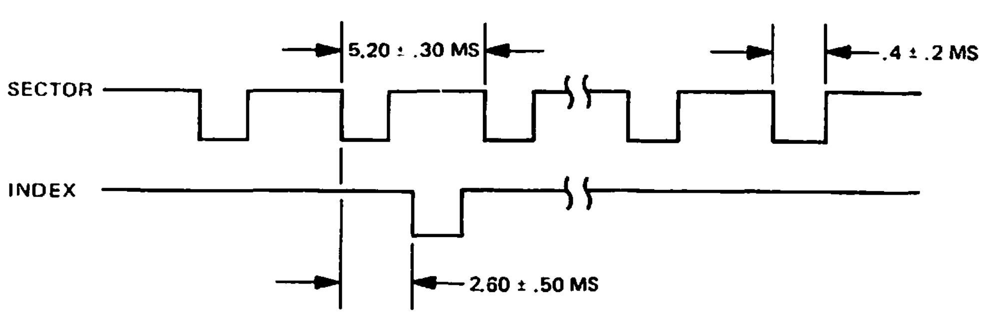


Figure 12. Sector Timing

4.1.2.4 Ready

This interface signal indicates that two (2) index holes have been sensed after properly inserting a diskette and closing the door, or that two index holes have been sensed following the application of +5V power to the drive.

For additional methods of using the Ready line, refer to section 7.5.

4.1.2.5 Read Data

This interface line provides the "raw data" (clock and data together) as detected by the drive electronics. Normally, this signal is a logical one level and becomes a logical zero level for the active state. Reference Figure 5 for the timing and bit shift tolerance within normal media variations.

4.1.2.6 Sep Data

This interface line furnishes the data bits as separated from the "raw data" by use of the internal data separator. Normally, this signal is a logical one level and becomes a logical zero level for the active state. Reference Figure 5 for the timing. This line is available on the SA800/801 Model 1 only.

4.1.2.7 Sep Clock

This interface line furnishes the clock bits as separated from the "raw data" by use of the internal data separator. Normally, this signal is a logical one level and becomes a logical zero level for the active state. Reference Figure 5 for the timing. This line is available on the SA800/801 Model 1 only.

4.1.2.8 Write Protect (Optional)

This interface signal is provided by the drive to give the user an indication when a Write Protected Diskette is installed. The signal is logical zero level when it is protected. Under normal operation, the drive will inhibit writing with a protected diskette installed in addition to notifying the interface.

For other methods of using Write Protect, refer to section 7.9.

4.1.3 Alternate I/O Pins

These interface pins have been provided for use with customer installable options. Refer to section 7 for methods of use.

4.2 Power Interface

The SA800/801 Diskette Storage Drive requires both AC and DC power for operation. The AC power is used for the spindle drive motor and the DC power is used for the electronics and the stepper motor.

4.2.1 AC Power

The AC power to the drive is via the connector P4/J4 located to the rear of the drive and below the AC motor capacitor. The P4/J4 pin designations are outlined below for standard as well as optional AC power.

P4 PIN	60 Hz		50 Hz	
	110 V (Standard)	208/230 V	110 V	220 V
1	90-127 VAC	180-253 VAC	90-127 VAC	180-253 VAC
2	Frame Gnd	Frame Gnd	Frame Gnd	Frame Gnd
3	90-127 V Rtn	180-253 V Rtn	90-127 V Rtn	180-253 V Rtn
MAX CURRENT	0.5 Amps	0.4 Amps	0.6 Amps	0.4 Amps
FREQ TOLERANCE	±0.5 Hz		±0.5 Hz	

4.2.2 DC Power

DC power to the drive is via connector P5/J5 located on non-component side of PCB near the P4 connector. The three DC voltages and their specifications along with their P5/J5 pin designators, are outlined below.

P5 PIN	DC VOLTAGE	TOLERANCE	CURRENT	MAX RIPPLE (p to p)
1	+24 VDC	±1.2 VDC	1.7 A Max** 1.3 A Typ	100 mv
2	+24 V Return*			
3	- 5 V Return			
4	- 5 VDC	±0.25 VDC	0.07 A Max 0.05 A Typ	50 mv
	Optional - 7 to -16 VDC (Cut Trace 'L')	NA	0.10 A Max 0.07 A Typ	NA
5	+ 5 VDC	±0.25 VDC	1.0 A Max 0.8 A Typ	50 mv
6	+ 5 V Return			

*The +24 VDC power requires a separate ground return line. Also, the +24V Return, other Ground Return lines, and Frame Ground must be connected together at the main power supply.

**If either customer installable option described in sections 7.2 and 7.4 are used, the current requirement for the +24 VDC is a multiple of the maximum +24V current times the number of drives on the line.

5.0 PHYSICAL INTERFACE

The electrical interface between the SA800/801 and the host system is via three connectors. The first connector, J1, provides the signal interface; the second connector, J5, provides the DC power; and the third connector, J4, provides the AC power and frame ground.

This section describes the physical connectors used on the drive and the recommended connectors to be used with them. Refer to Figure 16 for connector locations.

5.1 J1/P1 Connector

Connection to J1 is through a 50 pin PCB edge card connector. The dimensions for this connector are shown in Figure 13. The pins are numbered 1 through 50 with the even numbered pins on the component side of the PCB and the odd numbered pins on the non-component side. Pin 2 is located on the end of the PCB connector closest to the AC motor capacitor and is labeled 2. A key slot is provided between pins 4 and 6 for optional connector keying.

The recommended connectors tor P1 are tabulated below.

TYPE OF CABLE	MANUFACTURER	CONNECTOR P/N	CONTACT P/N
Twisted Pair, #26 (crimp or solder)	AMP	1-583717-1	583616-5 (crimp) 583854-3 (solder)
Twisted Pair #26 (solder term.)	VIKING	3VH25/1JN-5	NA
Flat Cable	3M "Scotchflex"	3415-0001	NA

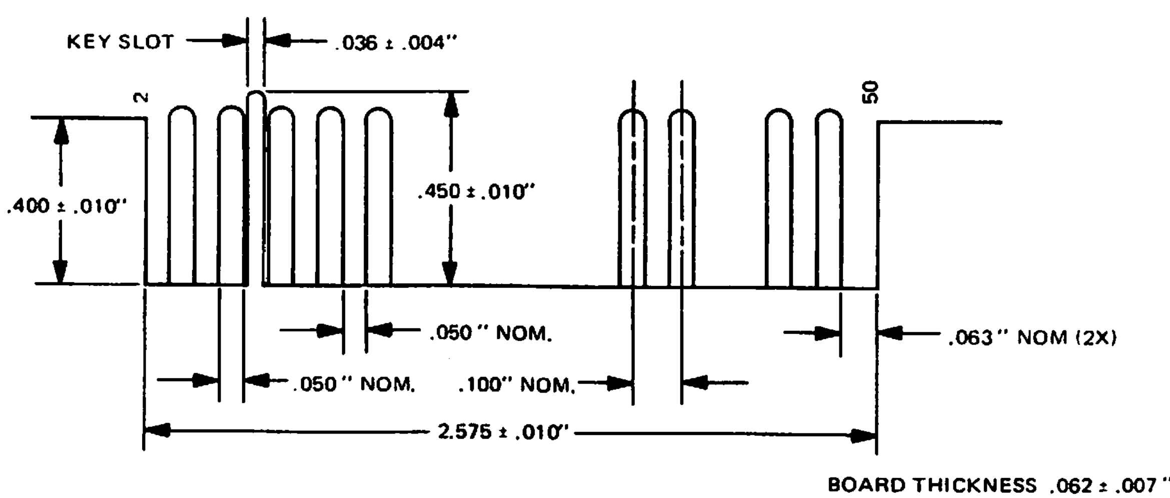


Figure 13. J1 Connector Dimensions

5.2 J5/P5 Connector

The DC power connector, J5, is mounted on the non-component side of the PCB and is located below the AC motor capacitor. J5 is a 6 pin AMP Mate-N-Lok connector P/N 1-380999-0. The recommended mating connector (P5) is AMP P/N 1-480270-0 utilizing AMP pins P/N 60619-1. J5 pins are labeled on the component side of the PCB with pin 5 located nearest J1/P1. Figure 14 illustrates J5 connector as seen on the drive PCB from non-component side.

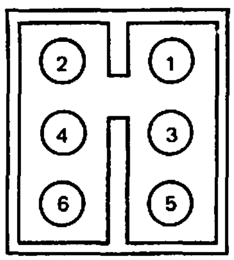


Figure 14. J5 Connector

5.3 J4/P4 Connector

The AC power connector, J4, is mounted on the AC motor capacitor bracket and is located just below the capacitor. J4 connector is a 3 pin connector AMP P/N 1-480305-0 with pins P/N 60620-1. The recommended mating connector (P4) is AMP P/N 1-480303-0 or 1-480304-0 both utilizing pins P/N 60619-1. Figure 15 illustrates J4 connector as seen from the rear of the drive.

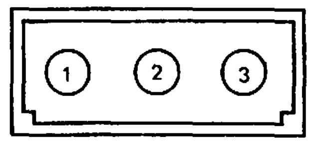


Figure 15. J4 Connector

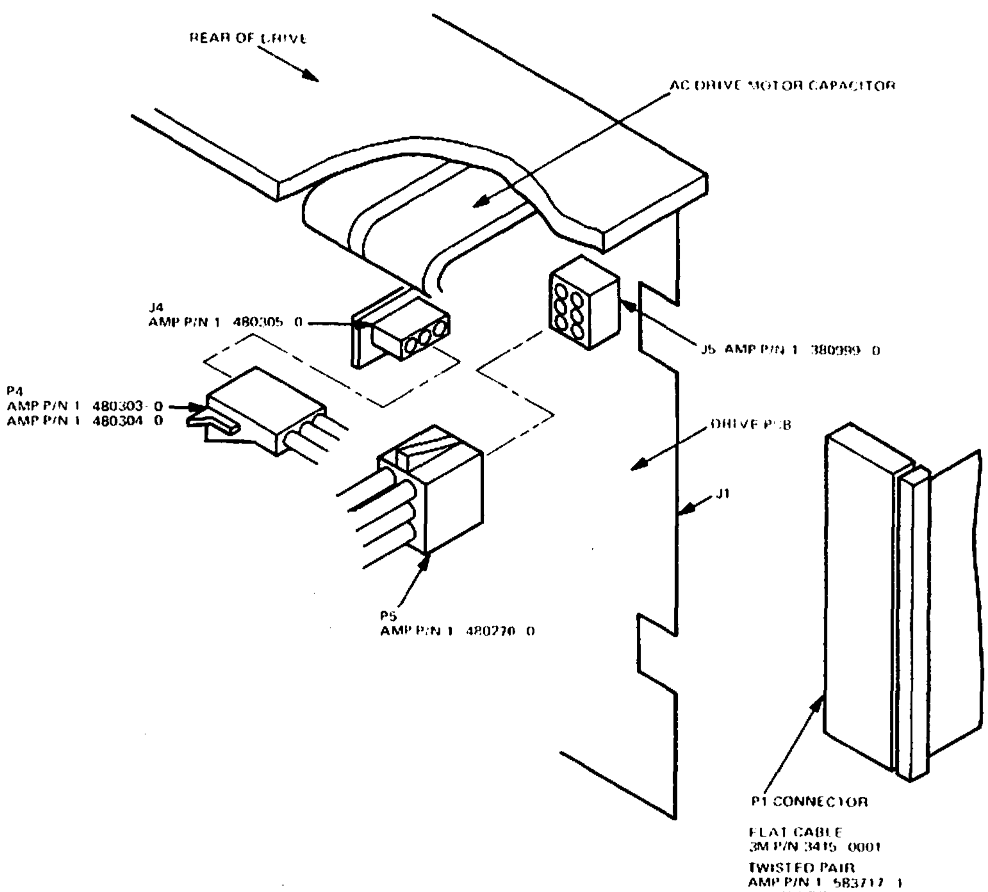


Figure 16. Interface Connectors – Physical Location Diagram

6.0 DRIVE PHYSICAL SPECIFICATIONS

This section describes the mechanical dimensions and mounting recommendations for the SA800/801.

6.1 Drive Dimensions

Reference Figure 18 for dimensions of the SA800/801.

6.2 Mounting Recommendations

The SA800/801 is capable of being mounted in one of the following positions:

1. Vertical   Door opening to the left or right.
2. Horizontal   Door opening up or down.
3. Upright   Door opening towards the front or rear.

6.2.1 Vertical Mounting

The drive, as shipped from the factory, is ready to be mounted in the vertical position, door opening left or right, without any adjustments.

6.2.2 Horizontal Mounting

If the drive is to be mounted horizontally with the door opening down (PCB up), the head load actuator return spring must be repositioned to allow for the proper head load time. Reference Figure 17 for the proper spring position on the actuator.

If the door is to open up (PCB down), it must be specified when ordering. This feature provides a heavier duty door opening spring. In addition, the head load actuator return spring must be repositioned to allow for proper head load time. Reference Figure 17 for the proper position for the spring on the actuator.

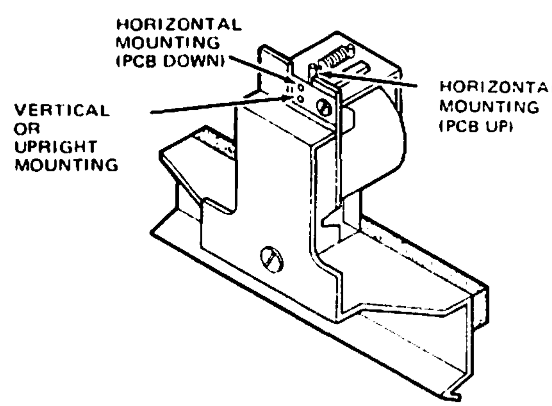
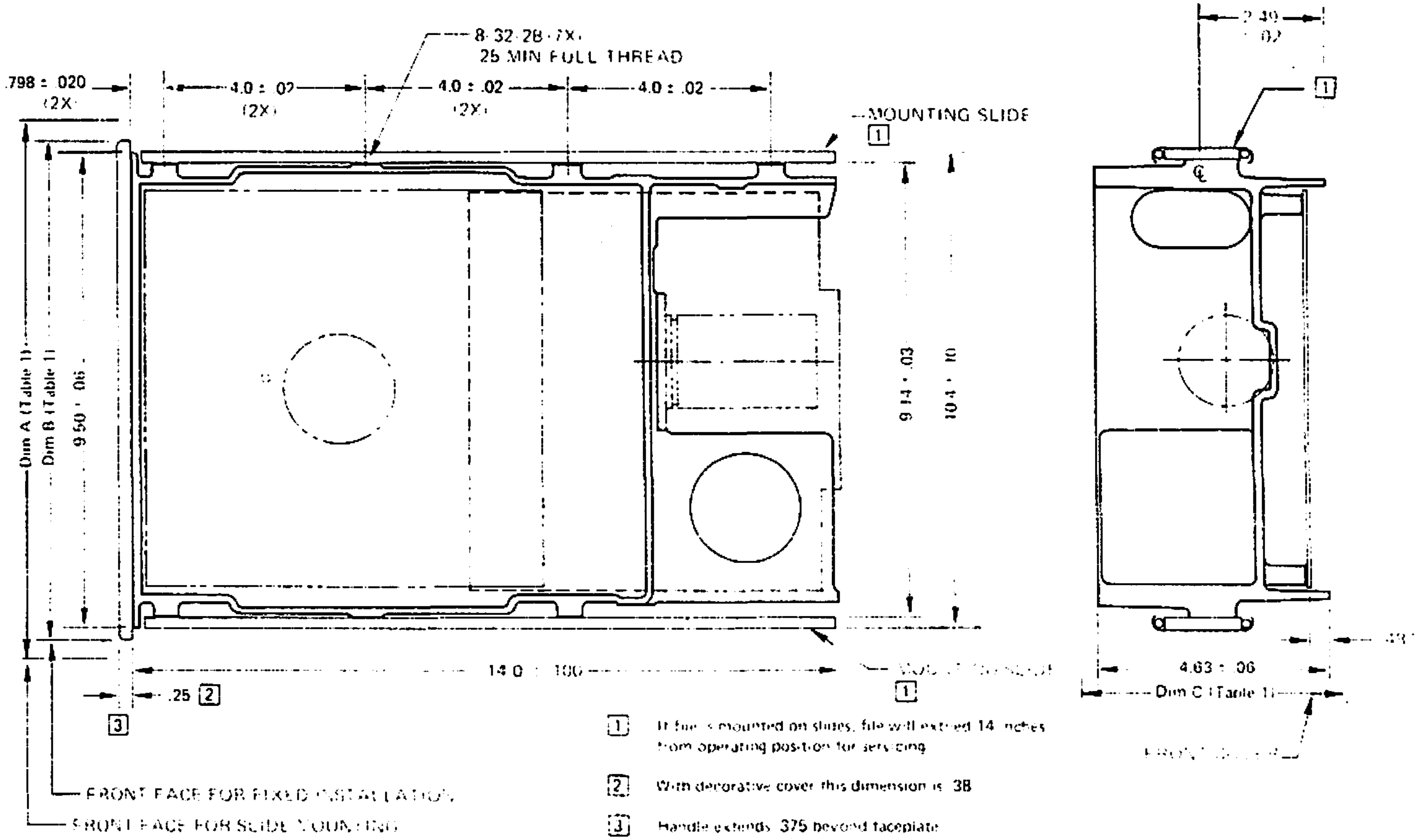


Figure 17. Head Load Actuator Mounting Prerequisites



1 If file is mounted on slides, file will extend 14 inches from operating position for servicing

2 With decorative cover this dimension is .38

3 Handle extends .375 beyond faceplate

4 All dimensions are in inches

TABLE 1

Decorative Cover Dimensions.			
Cover Size	Dim A	Dim B	Dim C
4-5/8 x 10	10.50	.240	4.62
5-1/4 x 10	10.00	.240	5.25
5-1/4 x 11	11.00	.740	5.25
Tolerance	±.03	±.030	±.03

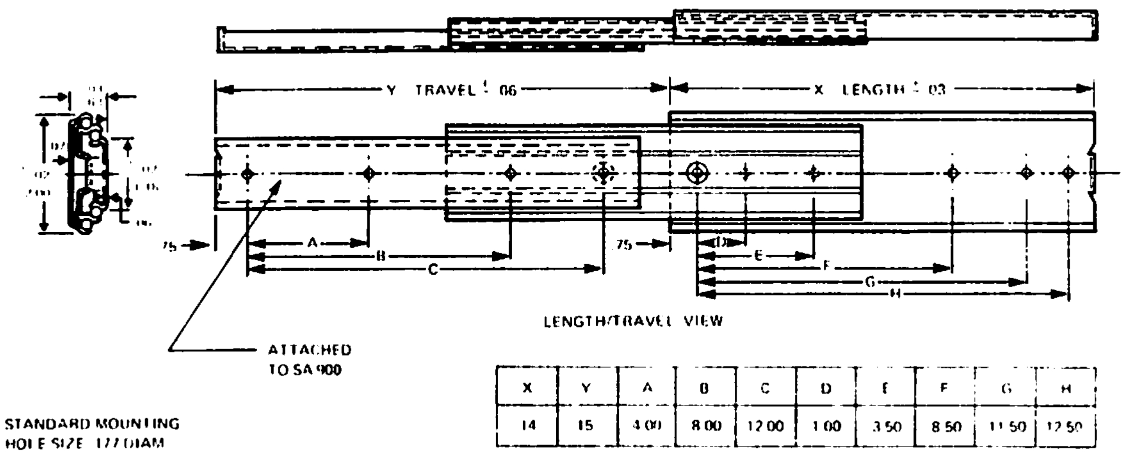
Figure 18. SA800/801 Diskette Storage Drive Dimensions

6.2.3 Upright Mounting

The drive, as shipped, is capable of being mounted in the upright position (IBM 3740 fashion) without any adjustments.

6.3 Chassis Slide

Available as an optional accessory is a chassis slide kit P/N 50239. This kit contains two slides, one locking and one non-locking, and seven screws. Dimensions of the slide are shown in Figure 19.



X	Y	A	B	C	D	E	F	G	H
14	15	4.00	8.00	12.00	1.00	3.50	8.50	11.50	12.50

Figure 19. Slide Mounting Dimensions

6.4 Decorative Face Plate

The SA800/801 may be ordered with one of the following decorative face plates:

SIZE	COLOR
4 5/8 x 10 1/2	Tan
4 5/8 x 10 1/2	White
5 1/4 x 10	Tan
5 1/4 x 10	White
5 1/4 x 11	Tan
5 1/4 x 11	White

If another color is required to match the system's color scheme, the face plate may be painted. The following information should be utilized to avoid potential problems in the painting process.

1. The front cover is made from GE's LEXAN. Dimensional stability of LEXAN exists from -60°F to +250°F. If the type paint used requires baking, the temperature should not exceed +250°F, including any hot spots which can contact the cover.

2. LEXAN is a polycarbonate. Any paint to be used should be investigated to insure that it does not contain chemicals that are solvents to polycarbonates.

7.0 CUSTOMER INSTALLABLE OPTIONS

The SA800/801 can be modified by the user to function differently than the standard method as outlined in sections 3 and 4. These modifications can be implemented by adding or deleting traces and by use of the Alternate I/O pins. This section will discuss a few examples of modifications and how to install them. The examples are:

1. Drive Select one to eight drives.
2. Select drive without loading head or enabling stepper.
3. Select drive and enable stepper without loading head.
4. Load head without selecting drive or enabling stepper.
5. Radial Ready.
6. Radial Index/Sector.
7. Eight, 16, or 32 Sector option.
8. In Use (Activity L.E.D.) optional input.
9. Write Protect options.

Tabulated below are the trace options with the condition of the trace as it is shipped from the factory. Figure 20 shows the location of these traces on the PCB.

CUSTOMER CUT/ADD TRACE OPTIONS

TRACE DESIGNATOR	DESCRIPTION	SHIPPED FROM FACTORY	
		OPEN	SHORT
T3,T4,T5,T6	Terminations for Multiplexed Inputs	X	
T2	Terminator for Drive Select		X
T1	Spare Terminator for Radial Head Load	X	
DS1,DS2,DS3, DS4	Drive Select Input Pins	X	DS1 is Plugged
RR	Radial Ready		X
RI	Radial Index and Sector		X
R,I,S	Ready, Index, Sector Alternate Output Pads		X
HL	Stepper Power From Head Load		X
DS	Stepper Power From Drive Select	X	
WP	Inhibit Write When Write Protected		X
NP	Allow Write When Write Protected	X	
8,16,32	8, 16, 32 Sectors (SA801 Only)	8 & 16	32
D	In Use Alternate Input	X	
2,4,6,8,10,12,14,16,18	Nine Alternate I/O Pins	X	
D1,D2,D4,DDS	Customer Installable Decode Drive Select Option	X	

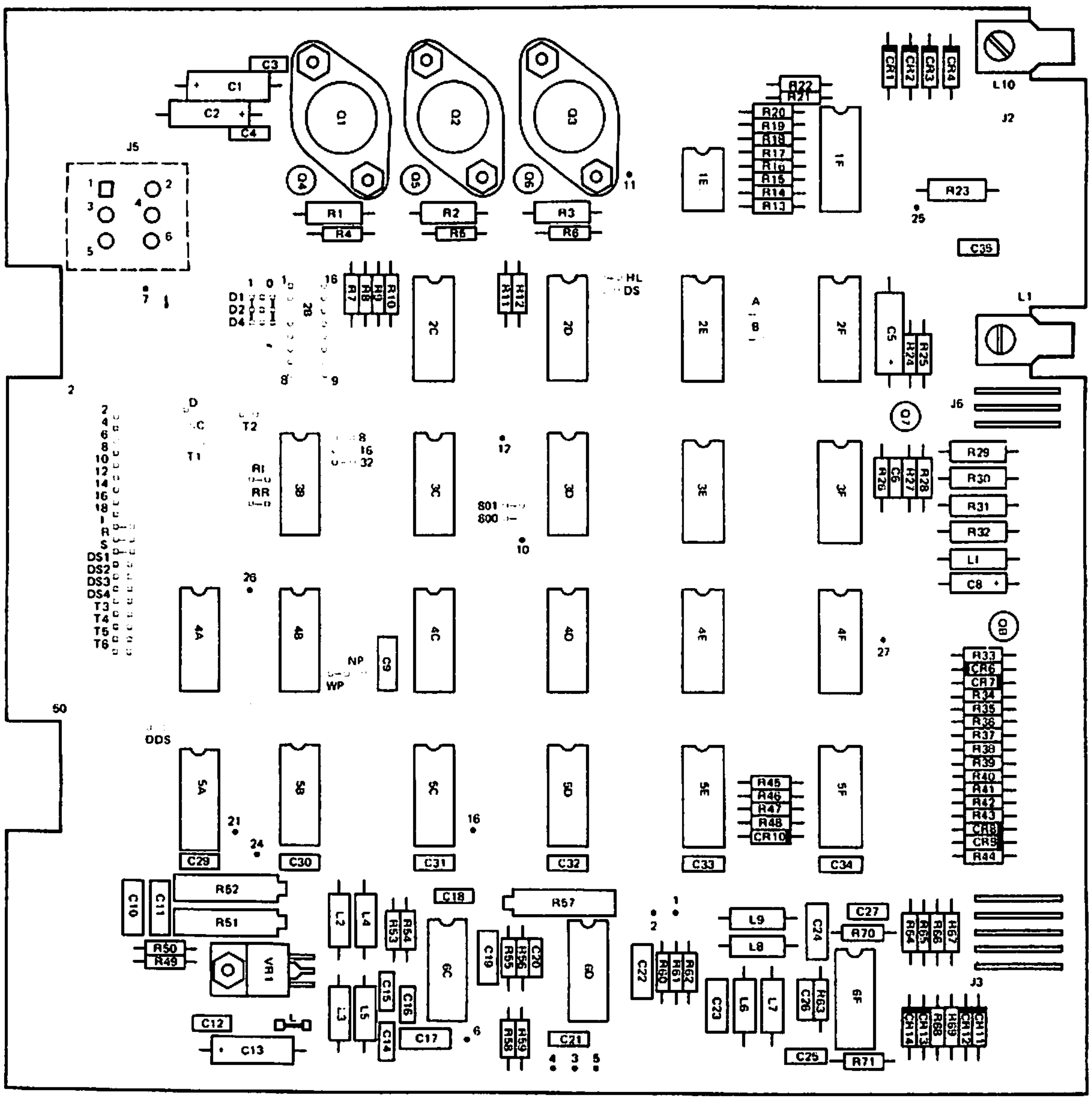


Figure 20. SA800/801 PCB Component Locations

7.1 Drive Select – One To Eight Drives

This customer installed option allows up to eight drives to be multiplexed together. This method of drive selection uses a binary address to select a drive.

To install this feature on a standard drive, the following traces should be added or deleted:

1. Add a 74L85, 4 bit comparator, into position 2B on PCB.
2. Connect trace 'DDS'.
3. Insure traces 'DS1' - 'DS4' are unplugged.
4. Jumper traces 'D1', 'D2', and 'D4' according to table below for the address of each drive.

ADDRESS	TRACE D1	TRACE D2	TRACE D4
0	0	0	0
1	1	0	0
2	0	1	0
3	1	1	0
4	0	0	1
5	1	0	1
6	0	1	1
7	1	1	1

The four Drive Select lines are to be used for addressing the drives. Pin 26 is used as Drive Select enable and pins 28 (binary 1), 30 (binary 2), and 32 (binary 4) are the address lines. The table below shows the logical state each line must be at to select each of the drives.

DRIVE	INTERFACE PIN 26	28	30	32
0	0	1	1	1
1	0	0	1	1
2	0	1	0	1
3	0	0	0	1
4	0	1	1	0
5	0	0	1	0
6	0	1	0	0
7	0	0	0	0

Figure 21 illustrates the circuitry.

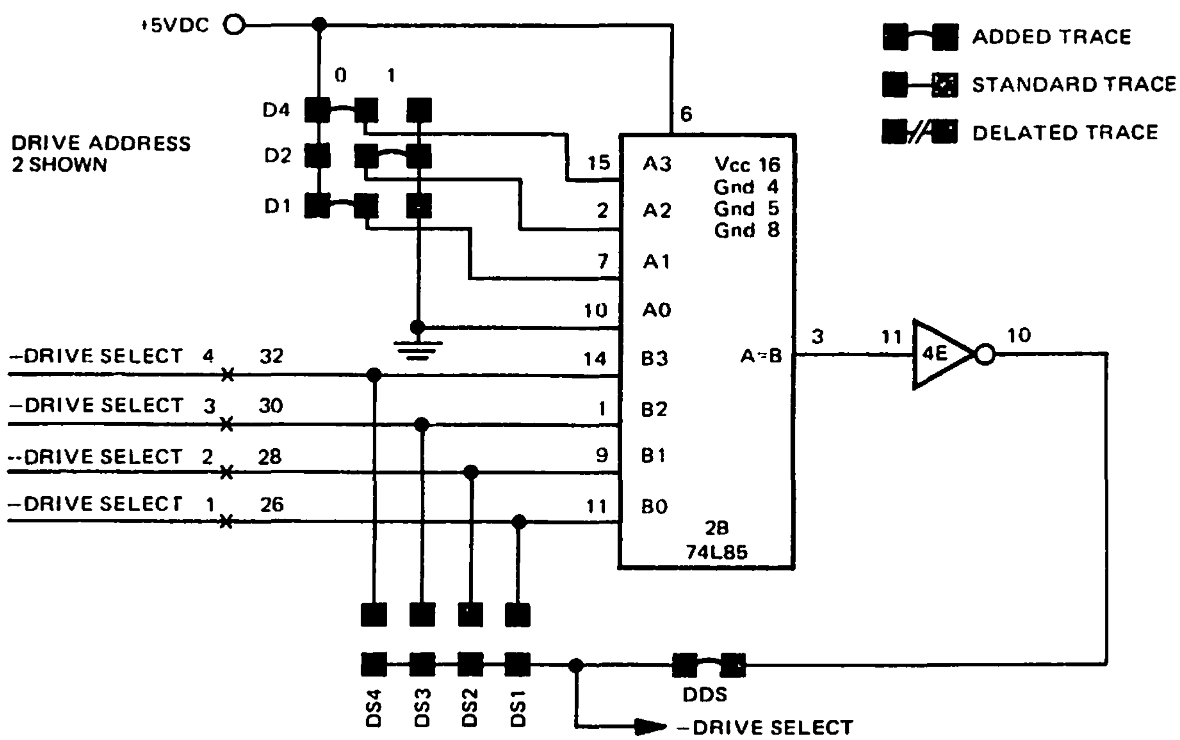


Figure 21. Drive Select Circuitry

7.2 Select Drive Without Loading Head Or Enabling Stepper Motor

This option would be advantageous to the user who requires a drive to be selected at all times. Normally, when a drive is selected, its head is loaded and the stepper motor is energized. The advantage of this option would be that the output control signals could be monitored (with the exception of Track Zero, which requires the stepper to be energized) while the head was unloaded thereby extending the head and media life. When the system requires the drive to perform a Read, Write, or Seek, the controller would activate the Head Load line (via one of the Alternate I/O lines) which in turn would load the head and energize the stepper motor. After the Head Load line is activated, a 35 ms delay must be introduced before Write Gate and Write Data may be applied or before Read Data is valid.

To install this option on a standard drive, the following traces should be added or deleted:

1. Connect trace 'T2'.
2. Cut trace 'B'.
3. Connect a wire from one of the Alternate I/O pins (2,4,6, etc.) to pad 'C' (-Head Load).

Figure 22 illustrates the circuitry.

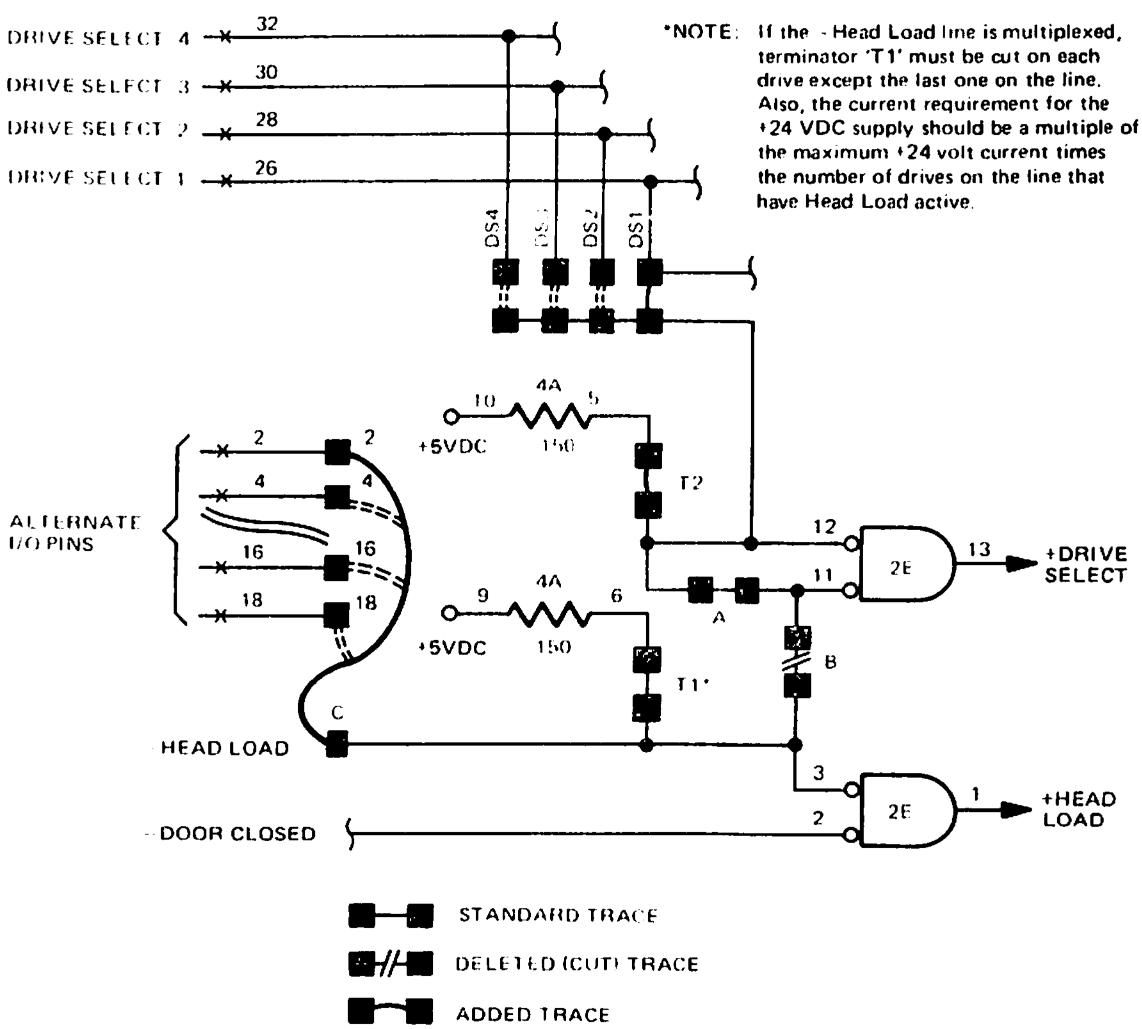


Figure 22. Select Drive Without Loading Head Circuit

7.3 Select Drive and Enable Stepper Without Loading Head

This option is useful to the user who wishes to select a drive and perform a seek operation without the head being loaded or with door open. An example use of this option is that at power on time, an automatic recalibrate (reverse seek to track zero) operation could be performed with the drive access door open. Normally for a seek to be performed, the door must be closed and the head loaded. Other advantages are those listed in section 7.2 in addition to being able to monitor Track Zero. When a Read or Write operation is to be performed, the head must be loaded (via one of the Alternate I/O lines). After the Head Load line is activated, a 35 ms delay must be introduced before Write Gate and Write Data may be applied or before Read Data is valid.

To install this option on a standard drive, the following traces should be added or deleted:

1. Connect trace 'T2'.
2. Cut trace 'B'.
3. Connect trace 'DS'.
4. Cut trace 'HL'.
5. Connect a wire from one of the Alternate I/O pins (2,4,6,etc.) to pad 'C' (-Head Load).

Figures 22 and 23 illustrate the circuitry.

7.4 Load Head Without Selecting Drive Or Enabling Stepper

This option is useful in disk to disk copy operations. It allows the user to keep the heads loaded on all drives thereby eliminating the 35 ms head load time. The head is kept loaded on each drive via an Alternate I/O pin. Each drive may have its own Head Load line (Radial or Simplexed) or they may share the same line (Multiplexed). When the drive is selected, an 8 ms delay must be introduced before a Read or Write operation can be performed. This is to allow the R/W head to settle after the stepper motor is energized. With this option installed, a drive can only be selected with both -Drive Select and -Head Load active.

To install this option on standard drive, the following traces should be added or deleted:

1. Connect trace 'T2'.
2. Cut trace 'A'.
3. Connect trace 'DS'.
4. Cut trace 'HL'.

*5. Connect a wire from one of the Alternate I/O pins (2,4,6,etc.) to pad 'C' (-Head Load).

*If the -Head Load line is multiplexed, terminator 'T1' must be cut on each drive except the last one on the line.

Figure 23 and 24 illustrate the circuitry.

NOTE: The 8 ms delay may be eliminated by keeping trace 'DS' open. This would keep the stepper motor energized at all times. If this is used, the current requirement of the +24 VDC supply must be a multiple of the maximum +24 Volt current times the number of drives on the line.

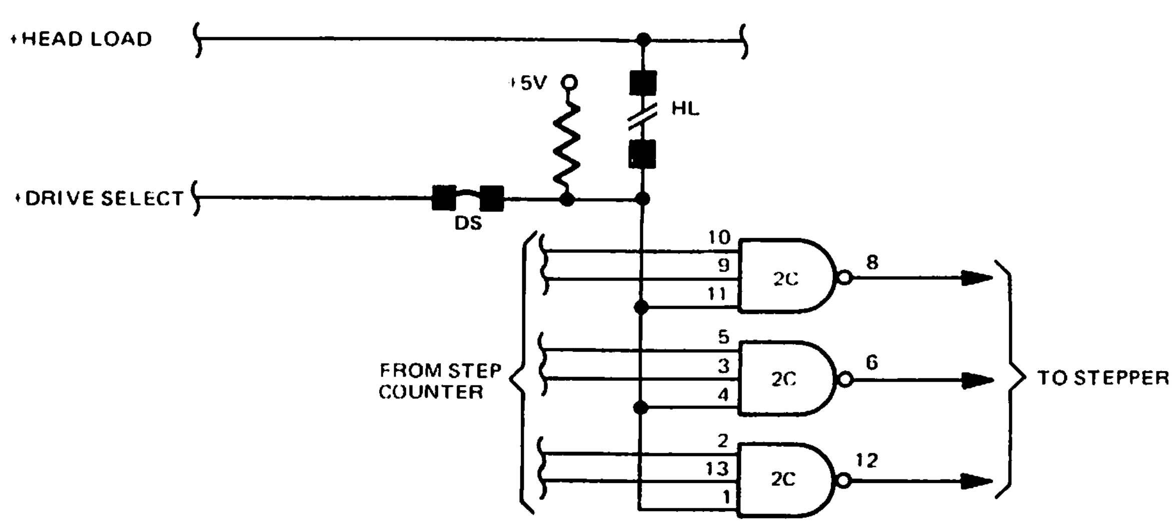
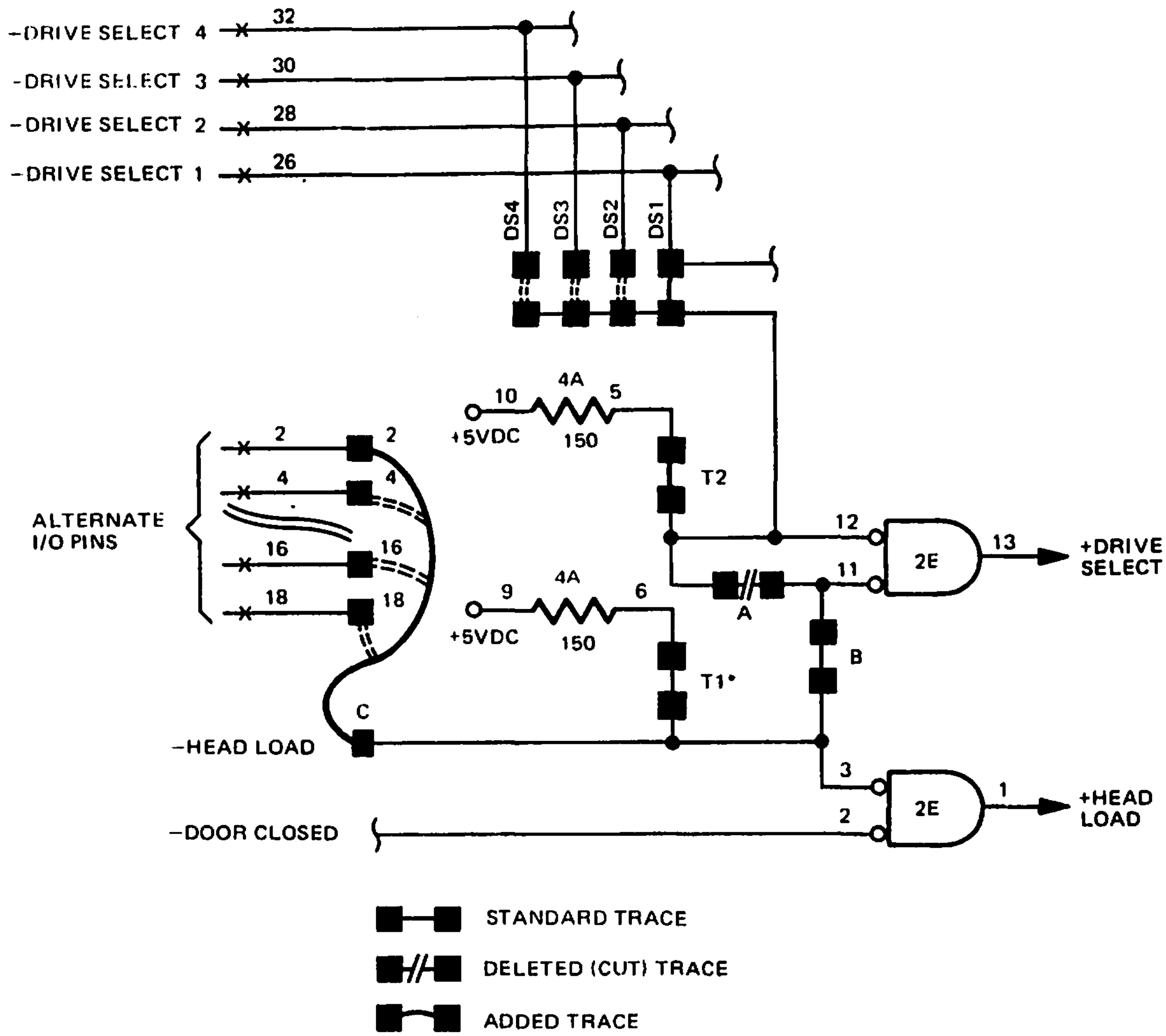


Figure 23. Stepper Motor Enable Circuit



* IF THE -HEAD LOAD LINE IS MULTIPLEXED, TERMINATOR 'T1' MUST BE CUT ON EACH DRIVE EXCEPT THE LAST ONE ON THE LINE.

Figure 24. Load Head Without Selecting Drive or Enabling Stepper Circuit

7.5 Radial Ready

This option enables the user to monitor the Ready line of each drive on the interface. This can be useful in detecting when an operator has removed or installed a Diskette in any drive. Normally, the Ready line from a drive is only available to the interface when it is selected.

To install this option on a standard drive, the following traces should be added or deleted:

1. Cut trace 'RR'.

*2. Cut trace 'R'.

*3. Add a wire from pad 'R' to one of the Alternate I/O pins.

*One of the drives on the interface may use pin 22 as its Ready line, therefore, steps 2 and 3 may be eliminated on this drive. All the other drives on the interface must have their own Ready line, therefore steps 2 and 3 must be incorporated.

Figure 25 illustrates the circuitry.

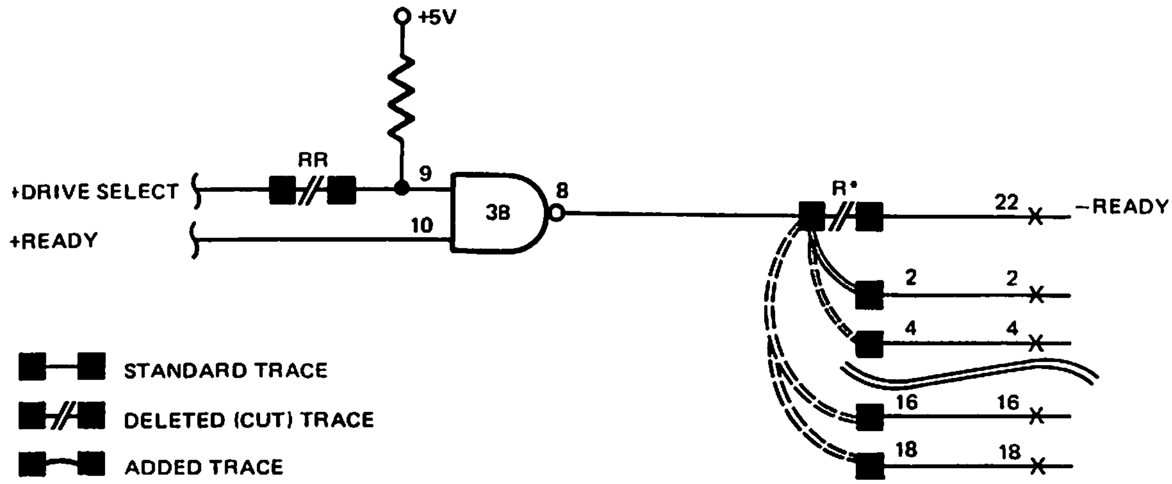


Figure 25. Radial Ready Circuit

7.6 Radial Index/Sector

This option enables the user to monitor the Index and Sector lines at all times so that the drive may be selected just prior to the sector that is to be processed. This option can be used to reduce average latency.

To install this option on a standard drive the following traces should be added or deleted:

1. Cut trace 'RI'.
*2. Cut trace 'I'.
*3. Cut trace 'S'.
*4. Add a wire from trace 'I' to one of the Alternate I/O pins.
*5. Add a wire from trace 'S' to one of the Alternate I/O pins.

*One of the drives on the interface may use pin 20 (-Index) and pin 24 (-Sector) as its Index and Sector lines, therefore, steps 2 - 5 may be eliminated for this drive. All other drives on the interface must have their own Index and Sector lines, therefore, steps 2 - 5 must be incorporated.

Figure 26 illustrates the circuitry.

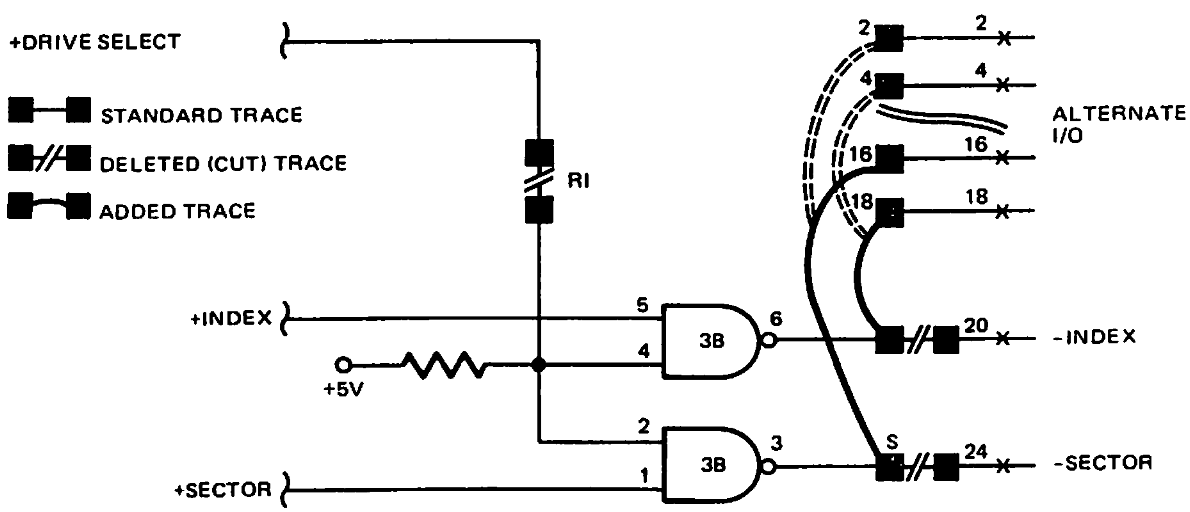


Figure 26. Radial Index/Sector Circuit

7.7 Eight, 16, Or 32 Sectors

The SA801, as shipped from the factory, is set up to provide 32 Sector pulses per revolution of the Diskette onto the interface. This option is provided for the user who wishes to have eight or 16 Sectors per revolution. The logic divides the Sector pulses by two or four. Reference Figure 27 for the timing relationships.

To install this option on a standard drive (SA801), the following traces should be added or deleted:

1. Cut trace '32'.
2. Connect trace '16' for 16 Sectors or connect trace '8' for eight Sectors.

Figure 28 illustrates the circuitry.

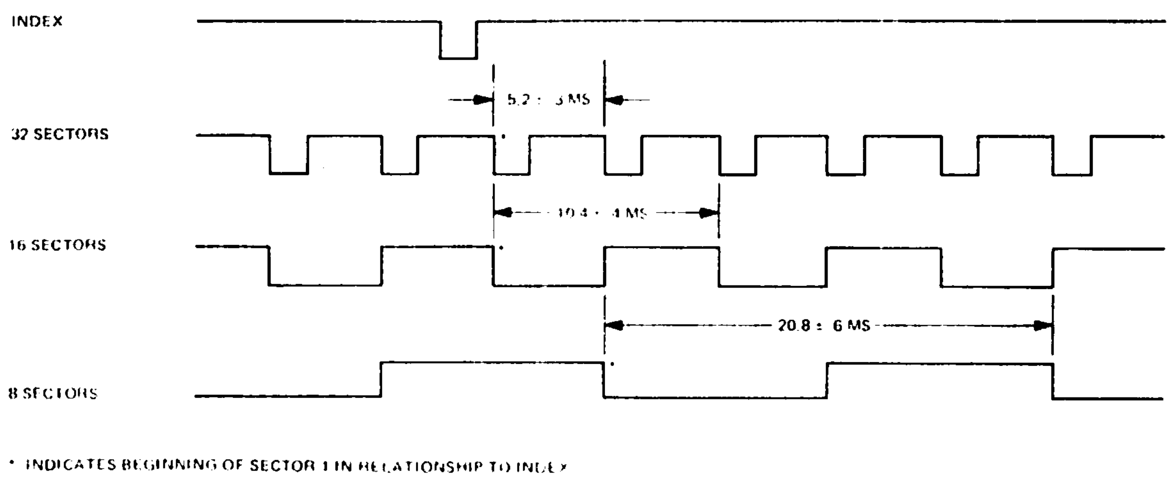


Figure 27. Sector Timing Relationships

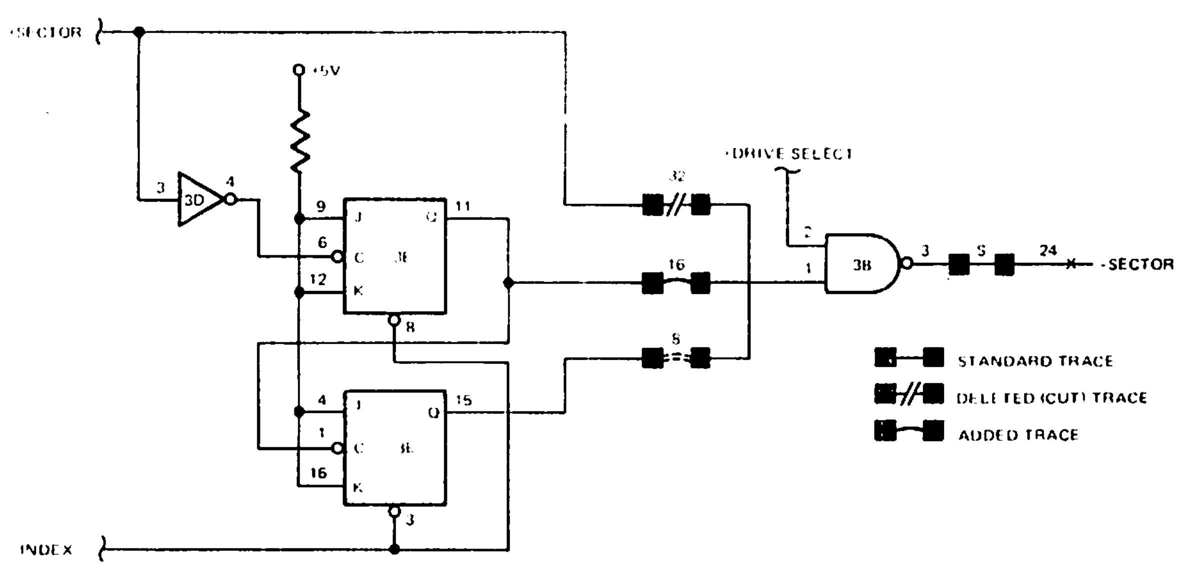


Figure 28. Sector Divide Circuit

7.8 In Use Optional Input (Activity Led)

This optional input, when activated to a logical zero level, will turn on the Activity LED mounted in the push bar on the front panel of the drive. It can be used as an indicator to the operator. Examples of some indications are:

1. Write protected Diskette is installed.
2. Drive in which the diskette is to be changed.
3. The operating system drive.
4. Drive with a special configuration.

To install this option on standard drive, add a wire from one of the Alternate I/O pins (2,4,etc.) to pad 'D'.

This signal is an "OR" function with Drive Select. Figure 29 illustrates the circuitry.

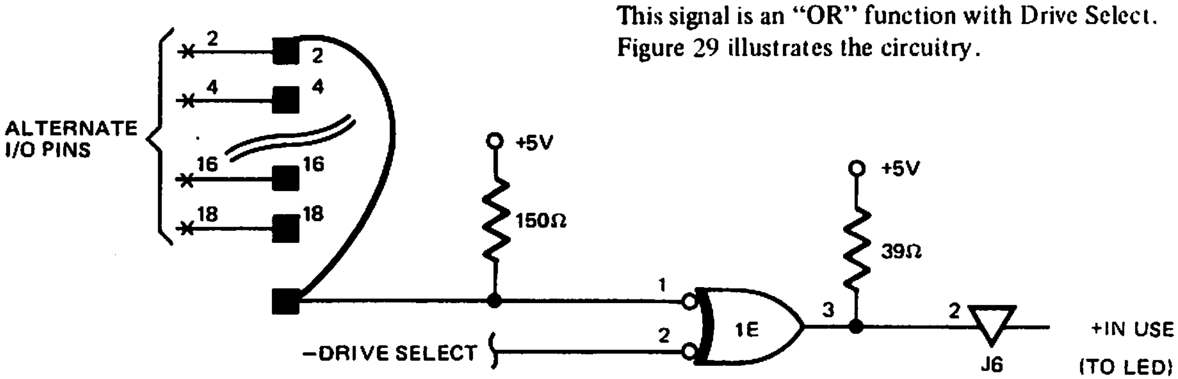


Figure 29. In Use/Activity LED Circuit

7.9 Write Protect Optional Use

As shipped from the factory, the optional Write Protect feature will internally inhibit writing when a Write Protected Diskette is installed. With this option installed, a Write Protected Diskette will not inhibit writing, but it will be reported to the interface. This option may be useful in identifying special use Diskettes.

To install this option on a drive with the Write Protect feature, the following traces should be added or deleted:

1. Cut trace 'WP'.
2. Connect trace 'NP'.

Figure 30 illustrates the circuitry.

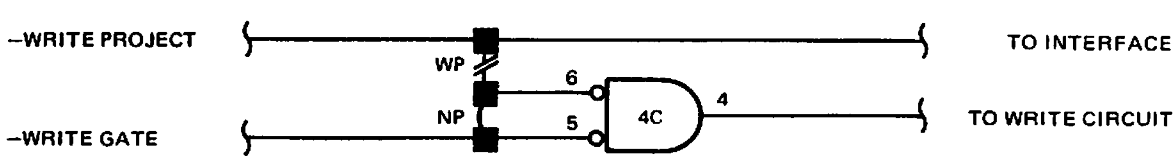


Figure 30. Write Protect Circuit

8.0 OPERATION PROCEDURES

The SA800/801 was designed for ease of operator use to facilitate a wide range of operator oriented applications. The following section is a guide for the handling and error recovery procedures on the diskette and diskette drive.

8.1 Diskette Loading and Handling

The diskette is a flexible disk enclosed in a plastic jacket. The interior of the jacket is lined with a wiping material to clean the disk of foreign material. Figure 31 shows the proper method of loading a diskette in the SA800/801 Diskette Storage Drive. To load the diskette, depress latch, insert the diskette with the label facing out. (See Figure 31.) Move the latch handle to the left to lock diskette on drive spindle. The diskette can be loaded or unloaded with all power on and drive spindle rotating.

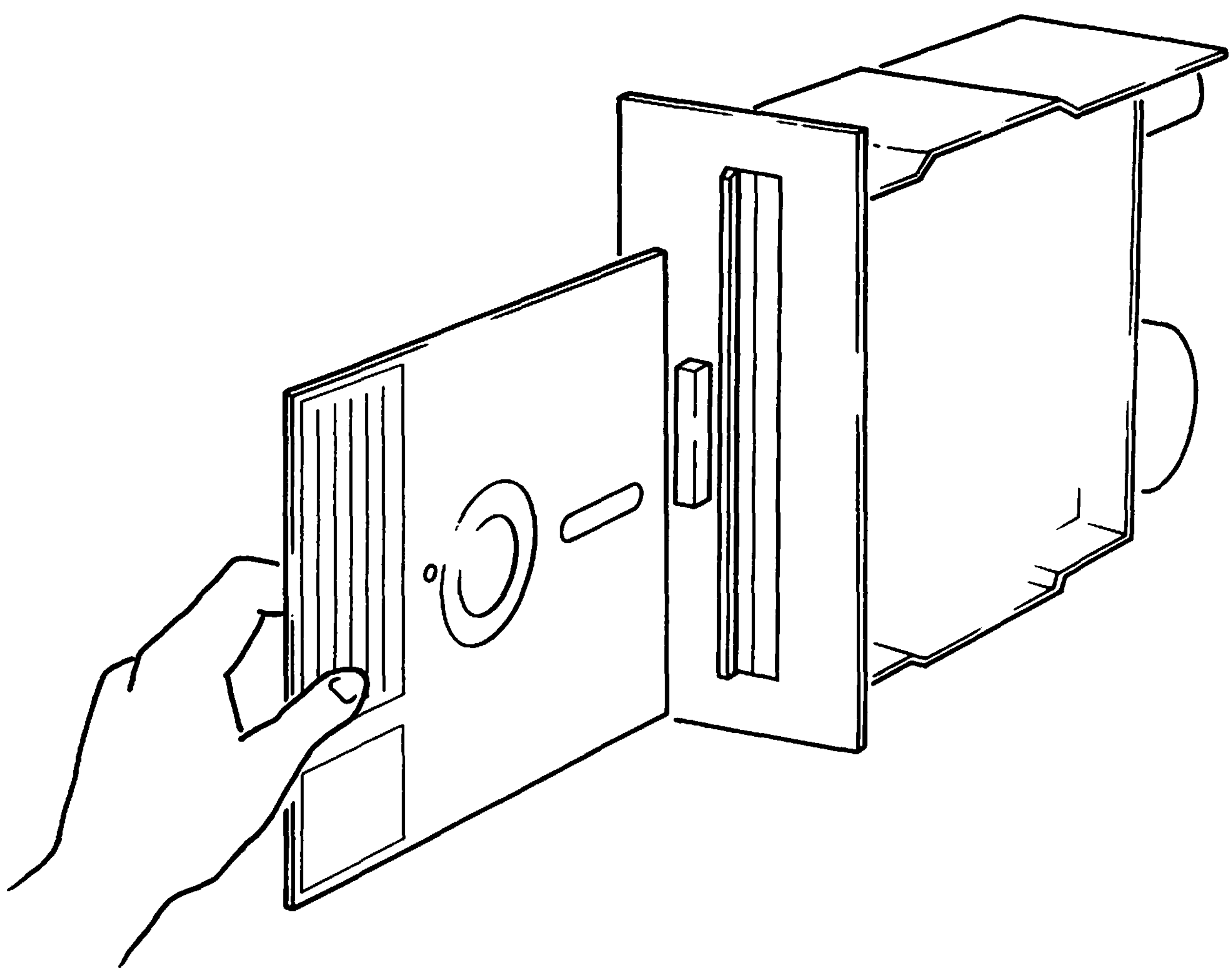


Figure 31. Loading SA800/801

When removed from the drive, the diskette is stored in an envelope. To protect the diskette, the same care and handling procedures specified for computer magnetic tape apply. These precautionary procedures are as follows:

1. Return the diskette to its storage envelope whenever it is removed from file.
2. Keep cartridges away from magnetic fields and from ferromagnetic materials which might become magnetized. Strong magnetic fields can distort recorded data on the disk.
3. Replace storage envelopes when they become worn, cracked or distorted. Envelopes are designed to protect the disk.
4. Do not write on the plastic jacket with a lead pencil or ball-point pen. Use a felt tip pen.
5. Heat and contamination from a carelessly dropped ash can damage the disk.
6. Do not expose diskette to heat or sunlight.
7. Do not touch or attempt to clean the disk surface. Abrasions may cause loss of stored data.

8.2 SA101 Write Protect

The SA101 has the capability of being write protected. The write protect feature is selected by the hole in the SA101. When the hole is open it is protected; when covered, writing is allowed. The hole is closed by placing a tab over the front of the hole, and the tab folded over covering the rear of the hole. The Diskette can then be write protected by removing the tab. See Figure 32.

8.3 SA100 Write Protect

The SA100 or IBM Diskettes are not manufactured with a write protect hole punched out as are the SA101 Diskettes. To Write-Protect one of these diskettes, a hole must be punched out as specified in Figure 33. The operation of the write protect is that which is outlined in paragraph 8.2.

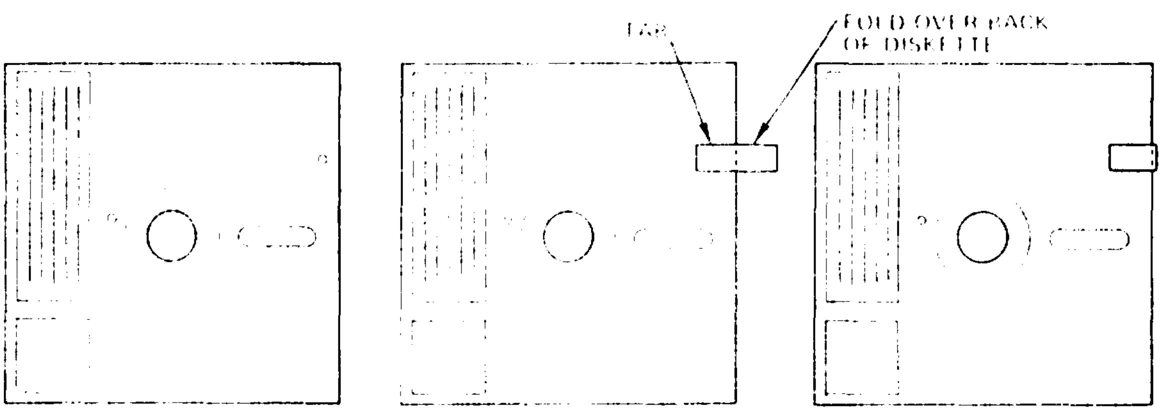


Figure 32. Diskette Write Protected

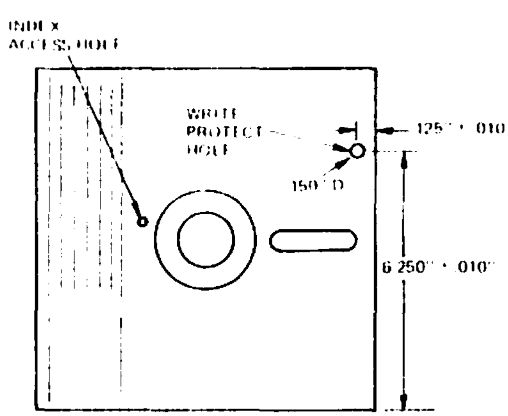


Figure 33. Write Protect Hole Specifications

9.0 ERROR DETECTION AND CORRECTION

9.1 Write Error

If an error occurs during a write operation, it will be detected on the next revolution by doing a read operation, commonly called a "write check." To correct the error, another write and write check operation must be done. If the write operation is not successful after ten (10) attempts have been made, a read operation should be attempted on another track to determine if the media or the drive is failing. If the error still persists, the disk should be considered defective and discarded.

9.2 Read Error

Most errors that occur will be "soft" errors; that is, by performing an error recovery procedure the data will be recovered.

Soft errors are usually caused by:

1. Airborne contaminants that pass between the read/write head and the disk. These contaminants will generally be removed by the cartridge self-cleaning wiper.
2. Random electrical noise which usually lasts for a few μ sec.
3. Small defects in the written data and/or track not detected during the write operation which may cause a soft error during a read.

The following procedures are recommended to recover from the above mentioned soft errors:

1. Reread the track ten (10) times or until such time as the data is recovered.
2. If data is not recovered after using step 1, access the head to the adjacent track in the same direction previously moved, then return to the desired track.
3. Repeat step 1.
4. If data is not recovered, the error is not recoverable.

THE ALTAIR-COMPATIBLE BUS INTERFACE CARD

THE INTERFACE BETWEEN THE ALTAIR COMMPATIBLE BUS AND THE FDC-1 ACCOMPLISHES 4 MAJOR FUNCTIONS.

1. IT IMPLEMENTS A PRIORITIZED DMA INTERFACE TO ALLOW THE FDC-1 TO OBTAIN CONTROL OF THE BUS.

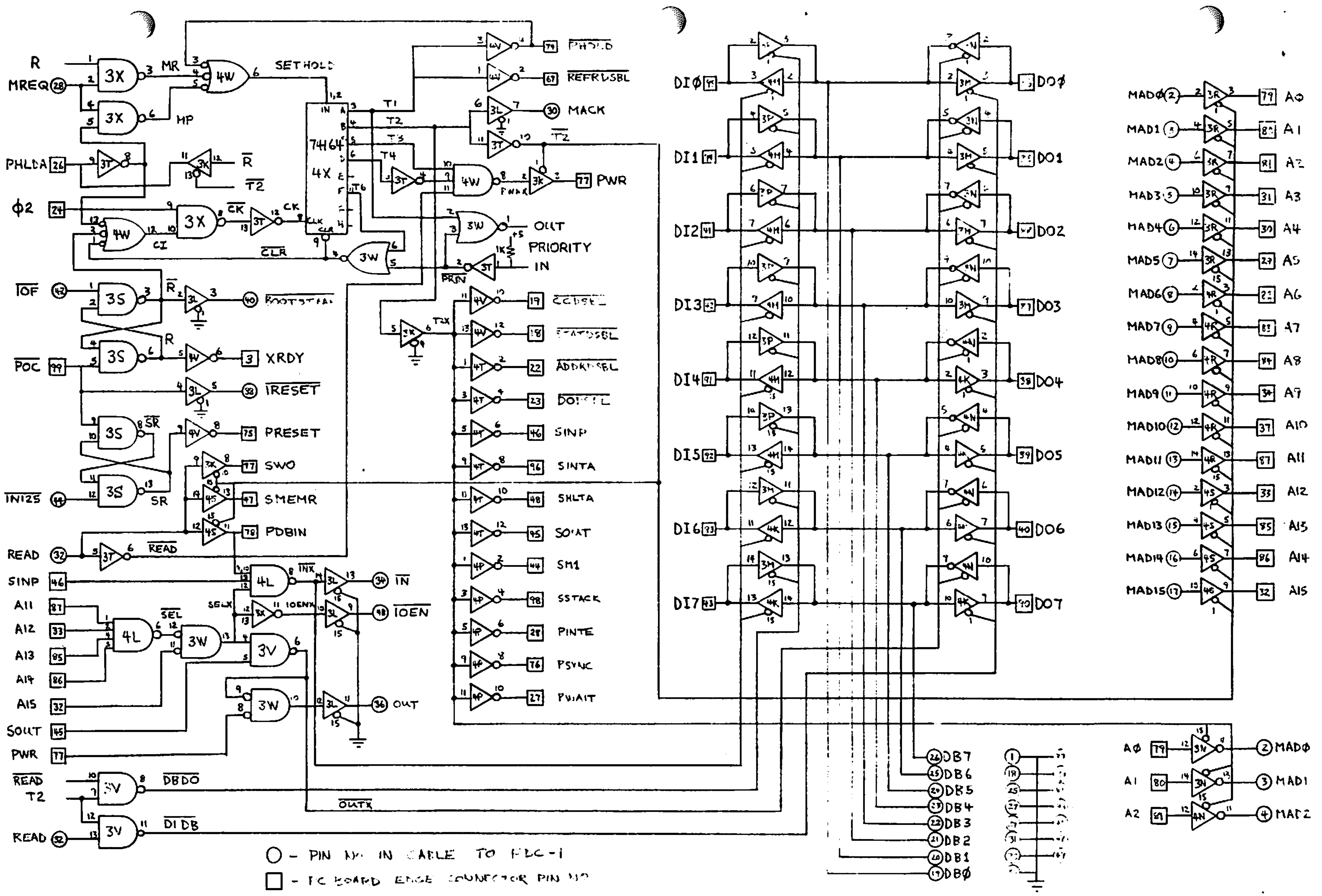
2. IT PHYSICALLY INTERFACES AND BUFFERS THE BUS WITH THE SIGNALS REQUIRED BY THE FDC-1.

3. IT PROVIDES THE CONTROL SIGNALS TO THE FDC-1 TO REQUEST A BOOTSTRAP LOAD AT POWER ON AND UNDER SOFTWARE CONTROL.

4. IT DECODES I/O PORTS USED BY THE FDC-1 FOR STATUS INPUT TO THE 8080 AND COMMAND OUTPUT.

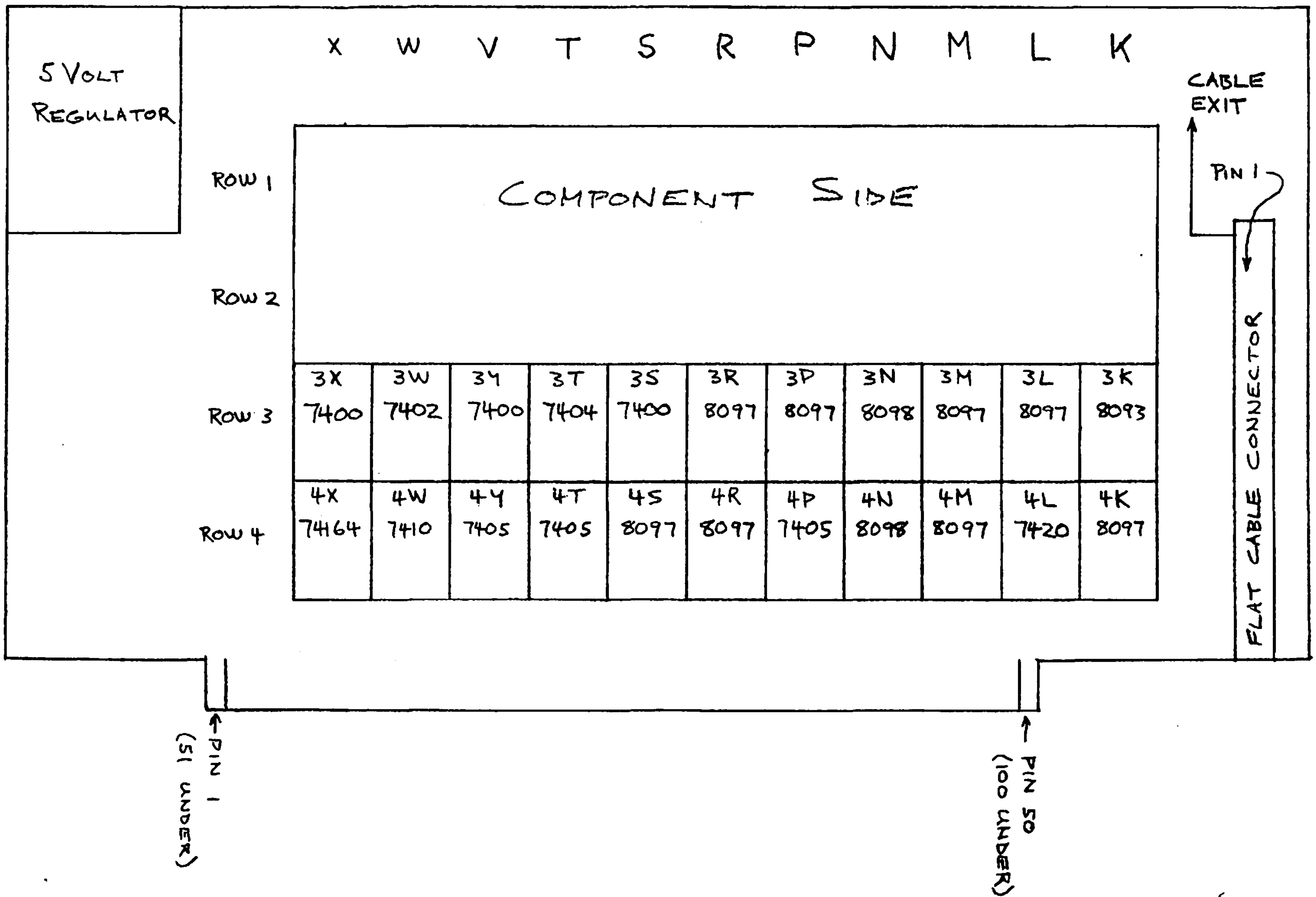
THE FOLLOWING MATERIAL CONTAINS A PARTS LIST, CIRCUIT DIAGRAM, WIRE LIST, AND COMPONENT LOCATION DIAGRAM. IT SHOULD BE REALIZED BY THE USER THAT THIS INFORMATION IS PRELIMINARY AND SUBJECT TO CHANGE. SIGNIFICANT CHANGES WILL BE COMMUNICATED TO ALL PURCHASERS OF THIS MANUAL.

B>



PRELIMINARY

DIGITAL SYSTEMS


5 VOLT
REGULATOR
X W V T S R P N M L K
CABLE
EXIT
PIN 1
ROW 1
COMPONENT SIDE
ROW 2
ROW 3
3X 7400
3W 7402
3Y 7400
3T 7404
3S 7400
3R 8097
3P 8097
3N 8098
3M 8097
3L 8097
3K 8093
ROW 4
4X 7464
4W 7410
4Y 7405
4T 7405
4S 8097
4R 8097
4P 7405
4N 8098
4M 8097
4L 7420
4K 8097
FLAT CABLE CONNECTOR
PIN 1
(51 UNDER)
PIN 50
(100 UNDER)

PARTS NEEDED TO BUILD THE BUS INTERFACE CARD

QUANTITY	DESCRIPTIION
1	VECTOR BOARD PART NUMBER 8800V OR EQUIVALENT
12	14 PIN SOCKETS
10	16 PIN SOCKETS
11	0.1 MF CERAMIC BYPASS CAPACITOR
1	10V 50MF ELECTROLYTIC CAPACITOR
1*	1K OHM RESISTOR

*(IMSAI USERS WILL NEED 2)

INTEGRATED CIRCUITS

QUANTITY	TYPE	LOCATIONS
3	7400	3X, 3V, 3S
1	7402	3W
1	7404	3T
3	7405	4V, 4T, 4P
1	7410	4W
1	7420	4L
1	74164	4X
1	8093	3K
8	8097	3R, 3P, 3M, 3L, 4S, 4R, 4M, 4K
2	8098	3N, 4N

POWER SUPPLIES

BUS INTERFACE CARD	PART NO. LM340T-5 OR EQUIVALENT ON-BOARD REQULATOR AND HEAT SINK.
FOR THE FDC-1	+5V AT 2.5 AMPS
FOR EACH SHUGART 800 DISK DRIVE	+5V AT 1.0 AMPS +24V AT 1.7 AMPS -5 TO -12V AT 0.1 AMPS (THE DRIVE WILL REGULATE TO -5)

CONSULT THE 800/801 OEM MANUAL FOR POWER CONNECTIONS TO THE DRIVES.
(CONNECTORS SUPPLIED WITH PURCHASE OF DRIVE)

CONSULT THE FDC-1 INTERFACE MANUAL FOR POWER CONNECTIONS.

WE WILL SUPPLY ALL CABLE AND CONNECTORS.

WIRE LIST

③ MEANS PIN THREE ON THE FLAT CABLE CONNECTOR

$\boxed{3}$ MEANS POSITION THREE ON THE BOARD EDGE CONNECTOR

SIGNAL	LOCATIONS				
DIØ	[95]	4MØ3	3PØ2		
DI1	[94]	4MØ5	3PØ4		
DI2	[41]	4MØ7	3PØ6		
DI3	[42]	4MØ9	3P1Ø		
DI4	[91]	4M11	3P12		
DI5	[92]	4M13	3P14		
DI6	[93]	4K11	3M12		
DI7	[43]	4K13	3M14		
DOØ	[36]	3MØ3	3NØ2		
DO1	[35]	3MØ5	3NØ4		
DO2	[88]	3MØ7	3NØ6		
DO3	[89]	3MØ9	3N1Ø		
DO4	[38]	4KØ3	4NØ2		
DO5	[39]	4KØ5	4NØ4		
DO6	[4Ø]	4KØ7	4NØ6		
DO7	[9Ø]	4KØ9	4N1Ø		
DBØ	[19]	4MØ2	3MØ2	3PØ3	3NØ3
DB1	[2Ø]	4MØ4	3MØ4	3PØ5	3NØ5
DB2	[21]	4MØ6	3MØ6	3PØ7	3NØ7
DB3	[22]	4M1Ø	3M1Ø	3PØ9	3NØ9
DB4	[23]	4M12	4KØ2	3P11	4NØ3
DB5	[24]	4M14	4KØ4	3P13	4NØ5
DB6	[25]	4K12	4KØ6	3M11	4NØ7
DB7	[26]	4K14	4K1Ø	3M13	4NØ9
MADØ	(2)	3RØ2	3N11		
MAD1	(3)	3RØ4	3N13		
MAD2	(4)	3RØ6	4N11		
MAD3	(5)	3R1Ø			
MAD4	(6)	3R12			
MAD5	(7)	3R14			
MAD6	(8)	4RØ2			
MAD7	(9)	4RØ4			
MAD8	(1Ø)	4RØ6			
MAD9	(11)	4R1Ø			
MAD1Ø	(12)	4R12			
MAD11	(13)	4R14			
MAD12	(14)	4SØ2			
MAD13	(15)	4SØ4			
MAD14	(16)	4SØ6			
MAD15	(17)	4S1Ø			
AØ	[79]	3RØ3	3N12		
A1	[8Ø]	3RØ5	3N14		
A2	[81]	3RØ7	4N12		
A3	[31]	3RØ9			
A4	[3Ø]	3R11			
A5	[29]	3R13			
A6	[82]	4RØ3			
A7	[83]	4RØ5			
A8	[84]	4RØ7			

A9	$\boxed{34}$	4R09					
A10	$\boxed{37}$	4R11					
A11	$\boxed{87}$	4R14	4L01				
A12	$\boxed{33}$	4S03	4L02				
A13	$\boxed{85}$	4S05	4L04				
A14	$\boxed{86}$	4S07	4L05				
A15	$\boxed{32}$	4S09	3W11				
R	3S06	3X01	3S02	4V05			
-R	3S03	3L02	4W02	3S04	3K12		
MREQ	28	3X02	3X04				
MR	3X03	4W04					
MP	3X06	4W05					
SETHOLD	4W06	4X01	4X02				
-PHOLD	$\boxed{74}$	4V04	4W03				
-REFRDSBL		67	4V02				
MACK	30	3L07					
PWR	$\boxed{77}$	3K03	3W08				
T1	4X03	4V01	4V03	3W02			
T2	4X04	3K05	3L06	3T11	3V09	3V12	
-T2	3T10	3K01	4S01	4R15	4R01	3R15	3R01
	4S15	3K10	3K13				
T3	4X05	4W10					
T4	4X06	3T03					
-T4	3T04	4W09					
T2X	3K06	4V11	4V13	4T01	4T03	4T05	4T09
	4T11	4T13	4P01	4P03	4P05	4P09	4P11
	3N15	4N15					
PWRX	4W08	3K02					
T6	4X11	3W06					
-PRIN	3T02	3W03	3W05				
PHLDA	$\boxed{26}$	3T09	3K11				
-PHLDA	3T08	3X05	4W13				
ϕ2	$\boxed{24}$	3X09					
-CK	3X08	3T13					
CK	3T12	4X08					
CI	4W12	3X10					
-CLR	3W04	4X09	4W01				
-IOF	42	3S01					
-POC	$\boxed{99}$	3S05	3L04	3S09			
-IN125	44	3S12					
SR	3S13	4V09	3S10				
-SR	3S08	3S11					
READ	32	3T05	4S12	4S14	3K09	3V13	
-READ	3T06	4W11	3V10				
SINP	$\boxed{46}$	4L13	4T06				
SOUT	$\boxed{45}$	3V05	4T12				
-DBD0	3V08	3M15	3P15	3P01			
-DIDB	3V11	4K01	3M01				
-SEL	4L06	3W12					
SELX	3W13	3V04	3X12	3X13	4L12		
IOENX	3X11	3L10					
-IOEN	48	3L09					
-INX	4L08	3L14	4K15	4M15	4M01		
-IN	34	3L13					
-OUTX	3V06	3W09	4N01	3N01			
OUTX	3W10	3L12					
OUT	36	3L11					

GND3L	3LØ8	3L15	3LØ1	
GND3K	3KØ7	3KØ4		
-BOOTSTRAP		4Ø	3LØ3	
XRDY	$\boxed{3}$	4VØ6		
-IRESET	38	3LØ5		
PRESET	$\boxed{75}$	4VØ8		
SWO	$\boxed{97}$	3KØ8		
SMEMR	$\boxed{47}$	4S13		
PDBIN	$\boxed{78}$	4S11	4LØ9	4L1Ø
-CCDSBL		$\boxed{19}$	4V1Ø	
-STATDSBL		$\boxed{18}$	4V12	
-ADDRDSBL		$\boxed{22}$	4TØ2	
-DODSBL		$\boxed{23}$	4TØ4	
SINTA	$\boxed{96}$	4TØ8		
SM1	$\boxed{44}$	4PØ2		
SSTACK	$\boxed{98}$	4PØ4		
PINTE	$\boxed{28}$	4PØ6		
PSYNC	$\boxed{76}$	4PØ8		
PWAIT	$\boxed{27}$	4P1Ø		
SHLTA	$\boxed{48}$	4T1Ø		

GROUNDX 4KØ8 1 18 25 27 31 35 39 41 43 45 47 49

1K RESISTOR	3TØ1	+5V
1K RESISTOR	4VØ4	+5V (IMSAI ONLY)

.1 µF BYPASS CAPCITOR FROM +5 TO GROUND-PLACE THEM AT LEAST EVERY TWO CHIPS

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THE FOLLOWING CONNECTIONS MUST BE MADE BETWEEN THE FDC-1 PC BOARD AND THE FLAT CABLE TO THE INTERFACE BOARD. THIS SHOULD BE ACCOMPLISHED BY WIRE WRAPING ON THE CABLE AND PC BOARD CONNECTORS SUPPLIED WITH FDC-1 PURCHASE. THE FDC-1 INTERFACE MANUAL SHOULD BE CONSULTED WHILE MAKING THESE CONNECTIONS.

SIGNAL NAME	FLAT CABLE CONNECTION	FDC-1 CONNECTIONS			
MADØ	2	J1-21	J2-29		
MAD1	3	J1-22	J2-3Ø		
MAD2	4	J1-23	J2-31		
MAD3	5		J2-32		
MAD4	6		J2-33		
MAD5	7		J2-34		
MAD6	8		J2-35		
MAD7	9		J2-36		
MAD8	1Ø		J2-37		
MAD9	11		J2-38		
MAD1Ø	12		J2-39		
MAD11	13		J2-4Ø		
MAD12	14		J2-41		
MAD13	15		J2-42		
MAD14	16		J2-43		
MAD15	17		J2-44		
DBØ	19	J1-29	J1-37	J2-21	J2-47
DB1	2Ø	J1-3Ø	J1-38	J2-22	J2-48
DB2	21	J1-31	J1-39	J2-23	J2-49
DB3	22	J1-32	J1-4Ø	J2-24	J2-5Ø
DB4	23	J1-33	J1-41	J2-25	J2-51
DB5	24	J1-34	J1-42	J2-26	J2-52
DB6	25	J1-35	J1-43	J2-27	J2-53
MREQ	28	J2-55			
MACK	3Ø	J2-56			
READ	32	J2-63			
-IN	34	J1-45			
OUT	36	J1-46			
-IRESET	38	J1-55			
-BOOTSTRAP	4Ø	J1-57			
-IOF	42	J1-59			
-IN125	44	J1-56			
-IOEN	48	J1-24	J1-25	J1-26	J1-27

TIE J1-28 TO +5V

GROUNDS:

MAKE THE FOLLOWING PINS COMMON

FLAT CABLE- 1, 18, 25, 27, 29, 31, 33, 35, 37, 39, 41, 43, 45, 47, 49

FDC-1 J1-83, J1-84, J1-85, J1-86
J2-83, J2-84, J2-85, J2-86

TIE J1-Ø9 TO GROUND (TTL HIGH WOULD WRITE PROTECT ALL DRIVES)