Diablo Systems Incorporated

Model 500 Programmable Tester Maintenance Manual

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PREFACE

This manual is intended to provide the information necessary to repair and maintain the Model 500 Programmable Tester. Detailed operating instructions are NOT included in this manual, because they are different for each of the different programs. Operating information can be found in the Program Manual pertaining to the particular program being used.

Comments on this manual and its use, as well as on the Model 500 Programmable Tester or any of the Tester programs, are welcome. Please address communications to the System Products department of Diablo Systems, Inc.

Diablo Systems, Inc. reserves the right to make improvements to products without incurring any obligation to incorporate such improvements in units previously sold.

MODEL 500 PROGRAMMABLE TESTER

Maintenance Manual

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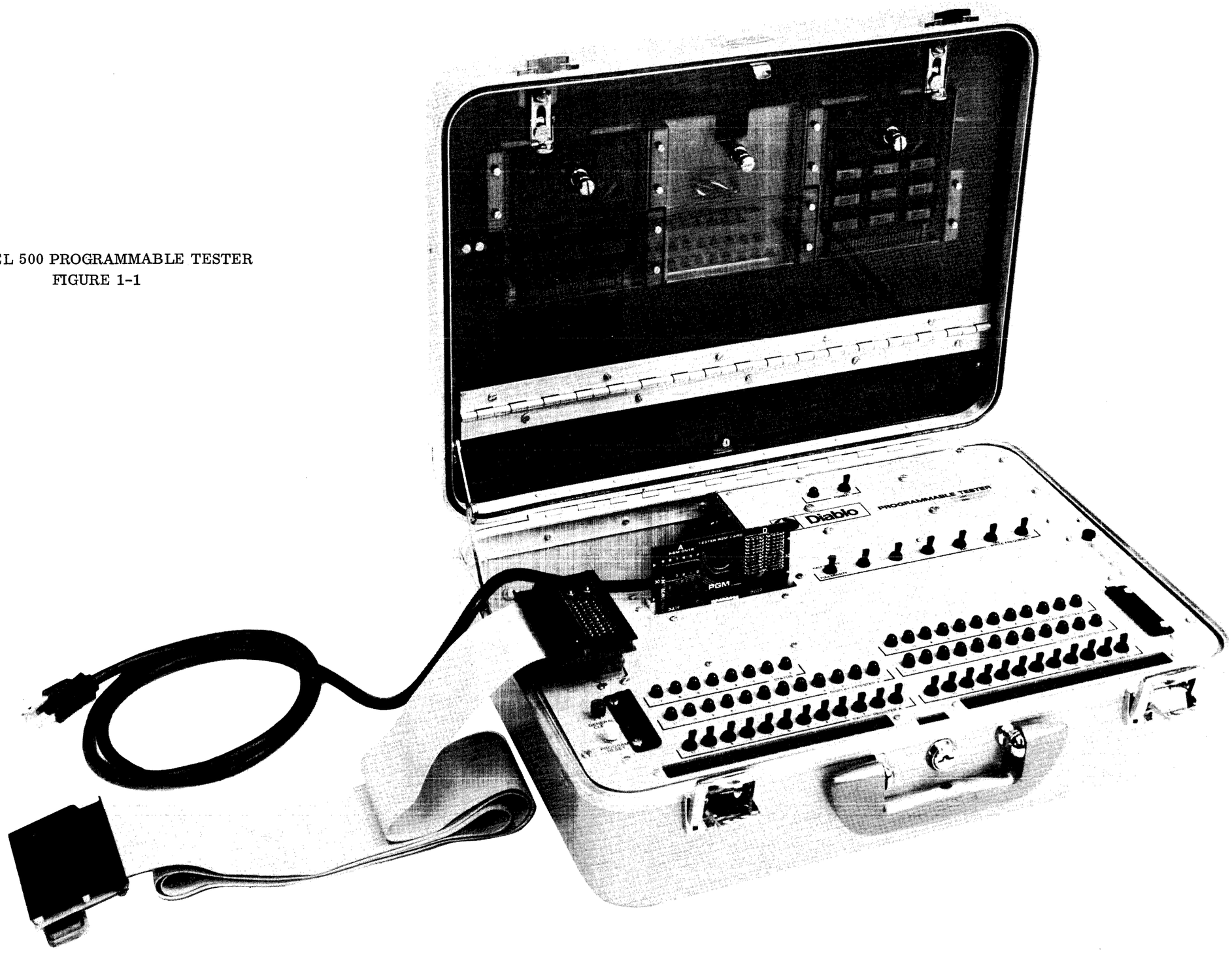
GENERAL INFORMATION

MODEL 500 PROGRAMMABLE TESTER
FIGURE 1-1



MODEL 500 PROGRAMMABLE TESTER

Maintenance Manual

Section 1

GENERAL INFORMATION

1.1 INTRODUCTION

The Diablo Systems Model 500 Programmable Tester, Figure 1-1, is a portable, solid-state electronics device used in troubleshooting and testing all Diablo Systems computer peripheral devices. The Model 500 Programmable Tester is basically a microcomputer which exercises the device under test as it executes its program steps. The program instructions are stored in Read Only Memory (ROM) integrated circuit chips on a small printed circuit board that plugs into the front panel of the tester. The device to be tested is cable-connected to the tester via a front-panel plug and an adapter cable. Only one device can be connected and tested at one time. If the tester is to be used with different types of devices (for example, both the Series 30 disk drive and the HyType printer), a different program card and different adapter cable are required for each type of device.

The tester is housed in a lockable, lightweight aluminum travel case, making it easily portable. The travel case also provides storage for adapter cables, the Programmable Tester Maintenance Manual, and up to three program cards.

1.2 RELATED DOCUMENTS

There is a separate manual covering each of the available programs. These documents contain program descriptions, operating procedures, and other information necessary for the proper testing of each device.

Occasionally, a device malfunction may be so involved that it requires a more detailed study of the tester's microprogram. For this reason, program manuals contain program listings and other information, sufficient to allow delving into the program in minute detail. This program information can also be of aid in troubleshooting the tester when problems arise.

1.3 SPECIFICATIONS

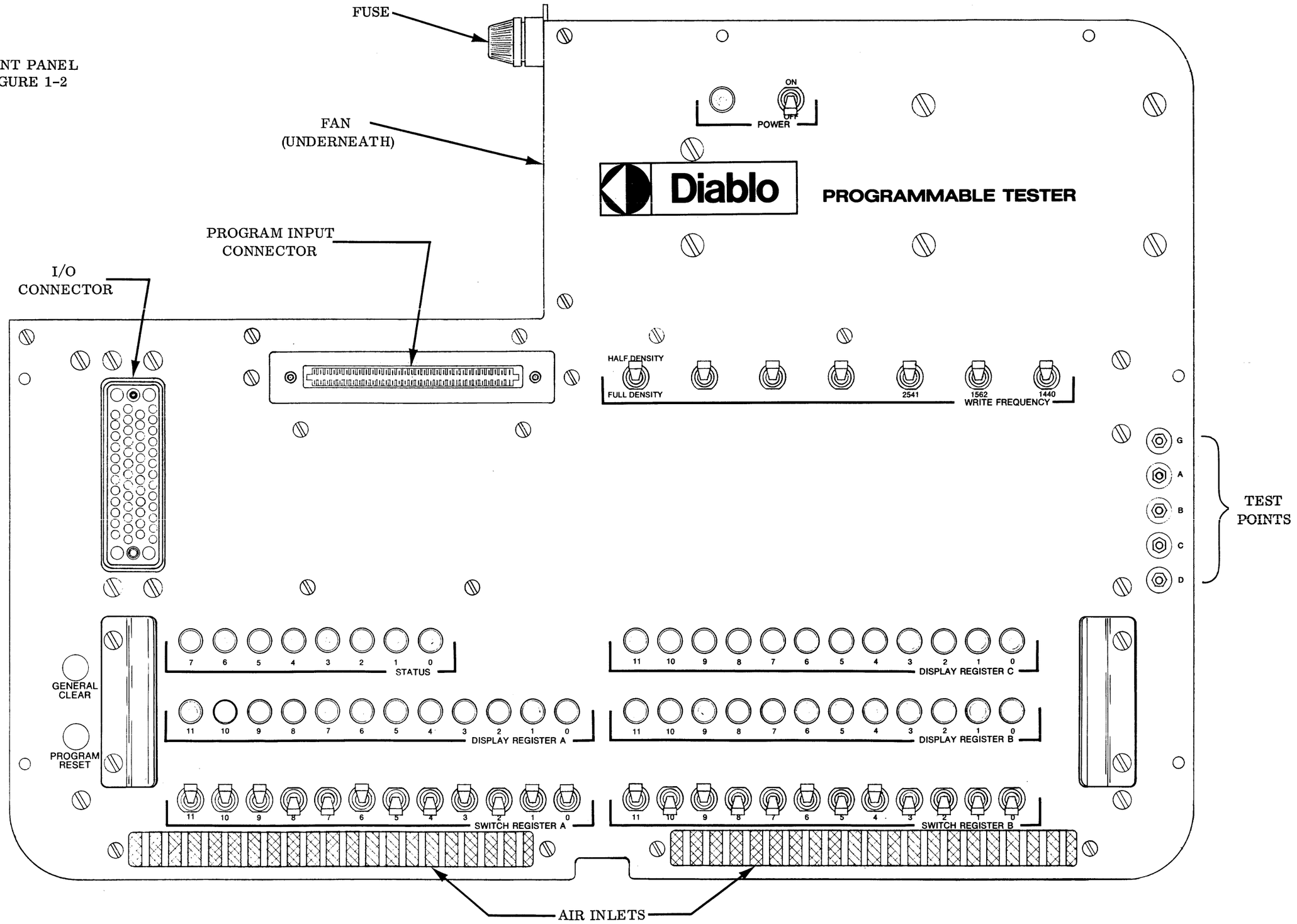
Clock rate, Microprocessor	5 MHz
Instruction execution time	400 nanoseconds
Disk write frequency	1440, 1562, or 2541 kilobits per second (kbps). Internal provision for three more frequencies, selected by installing crystals of the proper frequency. (Crystal frequency should be four times the desired bit rate.) Externally-generated frequencies may also be used.
Maximum practical program size	1024 12-bit instructions
Power requirements	60Hz ac, 115V $\pm$ 10%, 50 Watts

NOTE

The Programmable Tester does not provide power to the device being tested. An additional power supply is usually required to supply the necessary voltages to the device. Refer to the Product Description or Maintenance Manual for the device being tested for further information.

Size		
Height, closed	6 inches	15.2 cm
Height, open	17 1/2 inches	44.5 cm
Width	18 inches	45.7 cm
Depth, closed	14 inches	35.6 cm
Depth, open	16 3/4 inches	42.5 cm
Weight, including maintenance manual and three program cards (varies slightly because of different adapter cables)	25 lbs (approx.)	11.3kg (approx.)

FRONT PANEL
FIGURE 1-2



1.4 PHYSICAL DESCRIPTION

The front panel of the Programmable Tester is shown in Figure 1-2. All switches other than the Power Switch are two-position SPDT type. All indicators are Light-Emitting Diodes (LEDs).

POWER:
The POWER switch at the top center of the panel controls all power to the Tester. It is a DPST type, controlling both sides of the ac input line. Whenever power is on, the POWER LED will be illuminated and the cooling fan will operate.

WRITE FREQUENCY:
These switches control the frequency at which data is sent to a disk drive. The three switches on the right control the three standard frequencies of 1440, 1562, and 2541 kbps. The three unmarked switches may be used to control additional crystals that may be added internally. Externally generated frequencies can be applied to Test Point D: turning all Write Frequency switches off selects TPD as the frequency source. (See 3.7.4 for input signal requirements.) The left-hand switch allows selection of full or one-half of the otherwise-selected bit density.

PROGRAM INPUT CONNECTOR:
A 60-pin female socket for inserting a printed circuit card plug having ten contacts per inch.

I/O CONNECTOR:
50-pin Winchester socket used to connect the adapter cable to the Tester.

GENERAL CLEAR:
Pushbutton used to reset Program Counter, Status Registers, Display Registers, and other internal logic.

PROGRAM RESET:
Pushbutton used to clear Program Counter only.

STATUS:
Eight LEDs used to display status indications received from the device under test. The meaning of each is indicated on a front panel overlay sheet provided for each program and is further explained in the program operating instructions.

DISPLAY REGISTERS A, B, C:
Three sets of twelve LEDs which are turned on and off by the tester's program. The meaning of each is explained in the program operating instructions.

SWITCH REGISTERS A, B:
Two sets of twelve switches used to provide manual input to the tester. Instructions for using the switches are contained in the program operating instructions.

TEST POINTS:
The top point ("G") is logic GROUND. Test Points A and B can be energized by the program. Test Point C is READ SYNC DETECT, and Test Point D is the input for an externally-generated Write Clock. Instructions for using these points are contained in the program operating instructions.

FUSE:
A single 1-ampere 3AG fuse limiting ac input current to the tester.

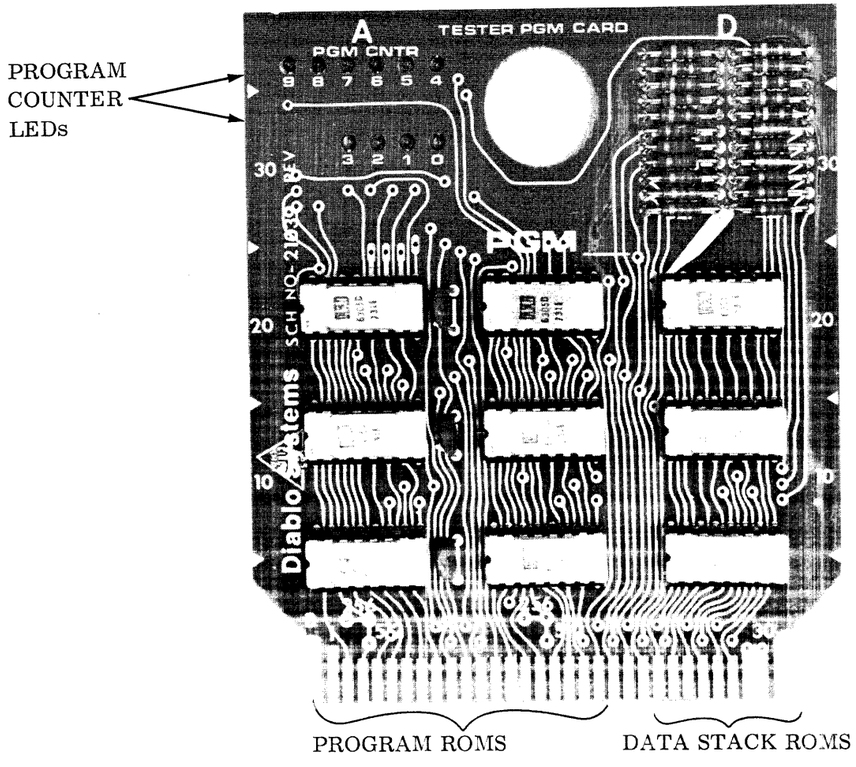
1.5 RELATED HARDWARE

There are several removable items which are part of the Programmable Tester, including program boards, I/O adapter cables, and the front panel overlay.

1.5.1 Program Boards (Figure 1-3)

These small printed circuit boards, approximately 4" x 4-1/2" (10.2 cm x 11.4 cm), contain the microcomputer program instructions and any necessary constant factors required by the program, all stored in ROM integrated circuit chips. Each board also contains ten LEDs which indicate the state of the Program Counter, or the binary address (in complement form) of the instruction being executed. Since this display register indicates the complement of the instruction address, the LEDs that are ON represent "0" bits; those that are OFF represent "1" bits in the instruction's binary address.

Up to 1024 twelve-bit instructions and 256 twelve-bit constants can be stored on any program board. There is a separate program board for each type of device to be tested.



PROGRAM BOARD
FIGURE 1-3

1.5.2 I/O Adapter Cables

For those using the Programmable Tester with only a single type of device, an adapter cable is provided to connect the device to the tester. A 50-pin Winchester connector is supplied on the tester end, and a connector suitable for the device to be tested is supplied on the other end.

For users testing more than one type of device, a modified 5-foot flat cable for the Diablo Systems Series 40 Disk Drive is supplied along with special short adapter cables. These special short cables adapt the disk drive end of the cable to the other devices capable of being tested. A different special short cable is needed for each type of device other than the Series 40 Disk Drive.

CAUTION

Do not use a Standard Series 40 I/O cable to connect the Tester to a Series 40 disk drive. The modified Series 40 cable has the connection to pin r broken: if a standard Series 40 cable is used, it will connect the disk drive's +5 Volts to the Tester's +5V supply, possibly resulting in improper operation.

A complete listing of all cables is located in Section 2 of this manual.

1.5.3 Front Panel Overlay

A plastic overlay is provided for each program. It is placed over and around the indicator LEDs on the front panel, and contains lettering that identifies the function of each of the indicators and switches used in the program. Since these functions can change from one program to the next, a separate overlay is required for each program.

1.6 BASIC OPERATING PROCEDURES

Detailed operating procedures will be found in the operating instructions provided by Diablo Systems for each of the available test programs. There are generally three aspects to performing a test--preliminary tasks, elementary testing, and, finally, executing the program.

1.6.1 Preliminary Tasks

This includes gathering all materials for the test (device power supply, cables, program board and program manual, disk cartridge or typing paper, etc.), reading the operating instructions to become familiar with the test procedures, connecting the various cables, and readying the device to be tested.

CAUTION

Apply no power to the device or to the tester until all cables and plugs are fully installed. No plugs should be installed or removed while power is applied.

1.6.2 Elementary Testing

The device must be capable of performing certain elementary functions before it can be fully tested. For example, if a disk does not rotate up to speed or if the heads do not load, no further testing can be accomplished. Similar fundamental actions can be observed on any device to be tested, and any such malfunctions must be corrected before testing can continue.

1.6.3 Executing the Program

Follow the steps listed in the program operating instructions. Different programs utilize different techniques for error display, option selection, and so forth, and these techniques require that specific operating sequences be followed in order to execute a valid test.

1.7 OPERATING HINTS

Following are hints of a general nature which will help to make operation of the tester easier and tend to reduce the possibility of malfunctions within the program or the tester itself.

(1) Follow the program operating instructions.

(2) Leave all tester switches OFF when not in use.

(3) Test general functions first, then make more specific tests.

(4) Do not cover air inlets or outlets. Be careful not to allow books or schematics to cover the openings and impede proper air circulation.

(5) Don't be fooled by a burned-out LED; although LEDs are much more reliable than ordinary light bulbs, occasionally one will burn out and give a false indication. The LEDs in the display registers can be tested simply by depressing the GENERAL CLEAR pushbutton, which lights all of them. The STATUS indicators are harder to test: GENERAL CLEAR turns these LEDs off, instead of on. However, if one of the STATUS indicators is suspect, it can be swapped with a known good LED. (See Section 4 for LED replacement hints.)

Section 2

INTERFACE

Section 2

INTERFACE

2.1 SIGNALS

All of the input and output signals passing through the front panel connector are listed in Table 2-1. The signal names are rather general in nature because they must be compatible with all possible devices capable of being tested. All interface signals are low-active.

2.1.1 Input Signals

All input signals enter the tester through identical line receivers. Details of these receivers will be found in paragraph 2.3.

(1) PARALLEL DATA IN 0-9: Ten lines bringing binary coded information into the the tester.

(2) STATUS IN 0-3, 6-7, 10-11: Eight lines providing device status indications to the tester. These lines are used to convey relatively constant status conditions, as opposed to momentary conditions (see FLAGs, next).

(3) FLAG 4-5, 8-9: Four lines providing momentary device status indications to the tester. Conditions on these lines are stored in the tester until cleared by the micro-program.

(4) SERIAL IN CLOCK: Provides serial clock input when reading from disk.

(5) SERIAL IN DATA: Provides serial data input when reading from disk.

2.1.2 Output Signals

All output signals are produced by identical line drivers. Details of these drivers will be found in paragraph 2.3.

(1) DATA OUT 0-8: Nine lines carrying parallel data from the output of the tester's Data Input Register to the device under test.

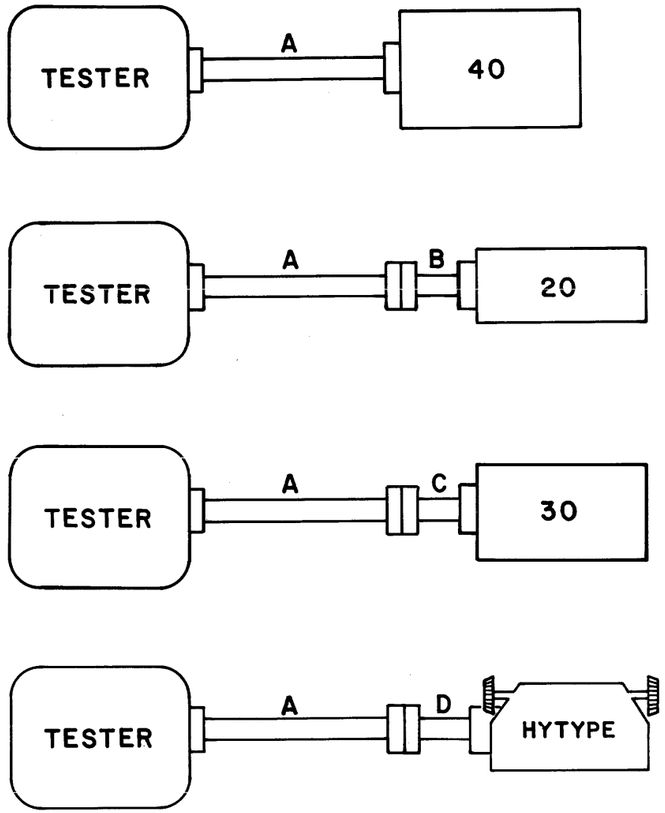
(2) OUT CONTROL 0-8: Nine lines providing control of device functions. Each line is individually controllable through execution of the Special Control Function instructions.

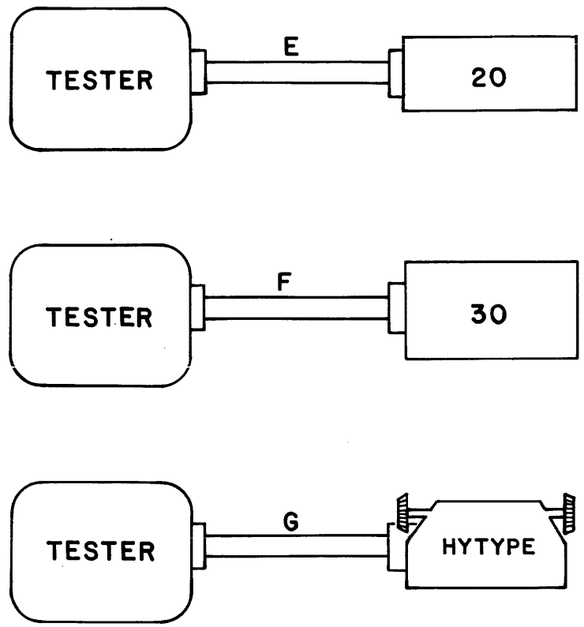
(3) WRITE SERIAL A, B: Two lines providing simultaneous control of disk write functions. Like the OUT CONTROL lines, these are controlled by SPC instructions, but are unique in that they also control internal tester circuits. Both lines are switched on and off simultaneously by the same SPC instructions. WRITE SERIAL A is normally used to control disk Write, while WRITE SERIAL B is normally used to control Erase. See note following (4).

TABLE 2-1

PROGRAMMABLE TESTER INTERFACE PLUG

SIGNAL	PIN	SIGNAL	
PARALLEL DATA IN 9	FF	DATA OUT 8	m
PARALLEL DATA IN 8	EE	DATA OUT 7	BB
PARALLEL DATA IN 7	DD	DATA OUT 6	b
PARALLEL DATA IN 6	CC	DATA OUT 5	T
PARALLEL DATA IN 5	d	DATA OUT 4	f
PARALLEL DATA IN 4	v	DATA OUT 3	X
PARALLEL DATA IN 3	n	DATA OUT 2	J
PARALLEL DATA IN 2	k	DATA OUT 1	s
PARALLEL DATA IN 1	j	DATA OUT 0	N
PARALLEL DATA IN 0	c	OUT CONTROL 8	L
STATUS IN 11	u	OUT CONTROL 7	R
STATUS IN 10	P	OUT CONTROL 6	V
FLAG 9	p	OUT CONTROL 5	Z
FLAG 8	y	OUT CONTROL 4	H
STATUS IN 7	U	OUT CONTROL 3	AA
STATUS IN 6	F	OUT CONTROL 2	w
FLAG 5	W	OUT CONTROL 1	t
FLAG 4	Y	OUT CONTROL 0	a
STATUS IN 3	M	WRITE SERIAL A	e
STATUS IN 2	D	WRITE SERIAL B	K
STATUS IN 1	z	READ	E
STATUS IN 0	h	SERIAL DATA OUT	B
SERIAL IN CLOCK	A	+5 Volts	r
SERIAL IN DATA	C	GND	S
GND	HH	GND	x





STANDARD CONFIGURATION:

MODIFIED SERIES 40 ADAPTER CABLE WITH ADAPTER PLUG FOR OTHER DEVICES.

CABLE	PART #
A=Tester to Series 40	21088
B=Adapter for Series 20	21109
C=Adapter for Series 30	21089
D=Adapter for HyType	21107

OPTIONAL CONFIGURATION:

INDIVIDUAL ADAPTER CABLE FOR EACH DEVICE WHEN TESTER IS USED WITH ONLY ONE DEVICE EXCLUSIVELY.

CABLE	PART #
E=Tester to Series 20	21108
F=Tester to Series 30	21090
G=Tester to HyType	21106

BLOCK DIAGRAM
EXTERNAL CABLE CONNECTIONS

FIGURE 2-1

(4) READ: Another line controlled by SPC instructions, but also controlling internal tester circuits:

NOTE

OUT CONTROL 0 through 8 may be used to control any external device functions other than disk Read and Write. READ and WRITE SERIAL A & B can be used only for their respective functions because they also activate internal tester circuits which affect data movement within the tester.

(5) SERIAL DATA OUT: A combination of serial data and clocks in the double-frequency format. Used only for writing to disk drives.

(6) +5 Volts: From the tester power supply, for possible future use in cable adapters, etc. This line should NOT be connected directly to any point in the device under test.

(7) GND: Tester logic ground. All three of these pins should be connected to logic ground in the device being tested to insure an adequate ground reference.

NOTE

Logic ground is isolated from chassis (frame) ground in the tester. It is expected that these two grounds will be connected in the normal wiring of the device being tested.

2.2 CABLES (Figure 2-1)

As usually configured, the Programmable Tester utilizes a modified Series 40 Disk Drive Adapter Cable, and special adapter plugs for interfacing this cable to other devices. If the tester is to be used with Series 40 Disk Drives exclusively, no adapter plugs are necessary, and the modified Series 40 Adapter Cable is all that is needed. If the tester is to be used exclusively with another type of device, special adapter cables are available for other devices, eliminating the need for any short adapter plugs. All adapter cables have cut away covers, providing access to all cable pins for scope probes, etc. Diablo part numbers for some of the various cables are shown in Figure 2-1 and in Section 5 of this manual, and in the Program Manual for each device.

CAUTION

Do not use a Standard Series 40 I/O cable to connect the Tester to a Series 40 disk drive. The modified Series 40 cable has the connection to pin r broken: if a standard Series 40 cable is used, it will connect the disk drive's +5 Volts to the Tester's +5V supply, possibly resulting in improper operation.

Cable wiring lists in each Program Manual show the relationships between the tester interface signals and the interface signals for the respective Diablo devices. For more detailed information concerning the device interface signals, consult the Maintenance Manual or the Product Description Manual for the particular device.

2.2.1 Connectors

The front panel connector is a Winchester MRAC 50SJ6 using socket contacts 1024S. Any mating connector of the MRAC50P-- series, using pin contacts 1024P, may be used with it. Adapter cables employ modified connectors, which provide access to the terminals for scoping, etc., while they are connected to the tester. The connectors on the device end of the adapter cables and plugs vary according to the device. The type of connector used in each case is referenced on the Diablo assembly drawing for the particular adapter.

2.2.2 Future Devices

Adapter cables and plugs will be made available for any new devices Diablo may manufacture in the future. These cables and plugs, and documentation covering them, will be available at the same time test programs for these new devices are made available.

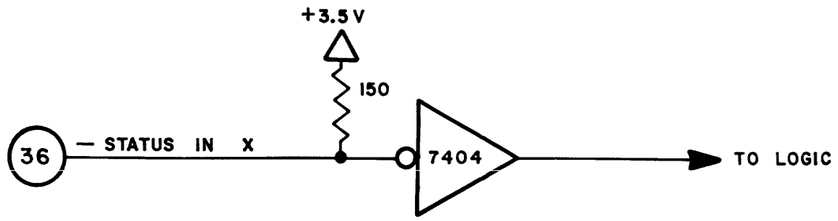
2.3 I/O CIRCUIT DESCRIPTION

There is very little logic involved in the line driver/receiver circuitry. The main design consideration is to maintain, as far as practical, the correct impedance-matching over the wide variety of adapter cables and plugs that may be used.

2.3.1 Input Receivers (Figure 2-2)

All input lines other than -SERIAL IN DATA and -SERIAL IN CLK are as shown in Figure 2-2. The 150Ω resistors are necessary to pull up and properly terminate the open-collector output lines of all Diablo devices. Any signal loss resulting from line and connection losses is compensated for by the 7404 hexinverter receivers, which restore waveforms to their original values, invert these input signals to their high-active form, and pass them on to the I/O logic.

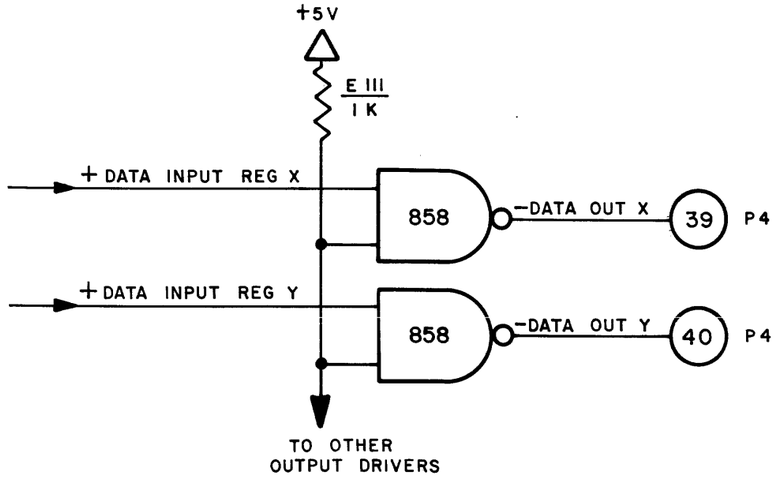
The -SERIAL IN DATA and -SERIAL IN CLK circuits are the same as that shown in Figure 2-2 except for the substitution of 82Ω resistors in place of the 150Ω resistors. This was done because these two signals have pulse widths substantially narrower than all other input signals.



TYPICAL INPUT RECEIVER
FIGURE 2-2

2.3.2 Output Drivers (Figure 2-3)

All output drivers are as shown in Figure 2-3. The 858 NAND gate is a DTL open-collector power driver, used primarily because of its power-sourcing capability. It should be noted that output circuits will not function properly if the output lines are not pulled up to some positive potential through a resistor. This is why it is necessary to use the terminator plug when operating the Programmable Tester with a disk drive. While troubleshooting the tester, if it is necessary to test the front panel connector outputs with the I/O adapter cable disconnected, each point must be returned to "+" through a resistor as it is tested. Refer to Section 4 for more details.



TYPICAL OUTPUT DRIVERS
FIGURE 2-3

Section 3

THEORY OF OPERATION

Section 3

THEORY OF OPERATION

3.1 FUNCTIONAL DESCRIPTION

Figure 3-1 is a basic block diagram of the Model 500 Programmable Tester microprocessor and its typical program instruction. Input to the microprocessor can come from a variety of sources -- either from the device under test, the front panel switches, the ROM constant factor Data Stack, one of the internal registers, or from the program itself. Output can go to a front panel indicator, to the device under test, or back to one of the internal registers.

3.1.1 Basic Concepts

Generally, each instruction in the program moves data from one location to another, and the data may or may not be altered in the process. Input source and output destination, as well as whatever modification of data is required as it passes through the Arithmetic Logical Unit (ALU), is specified by the program instruction.

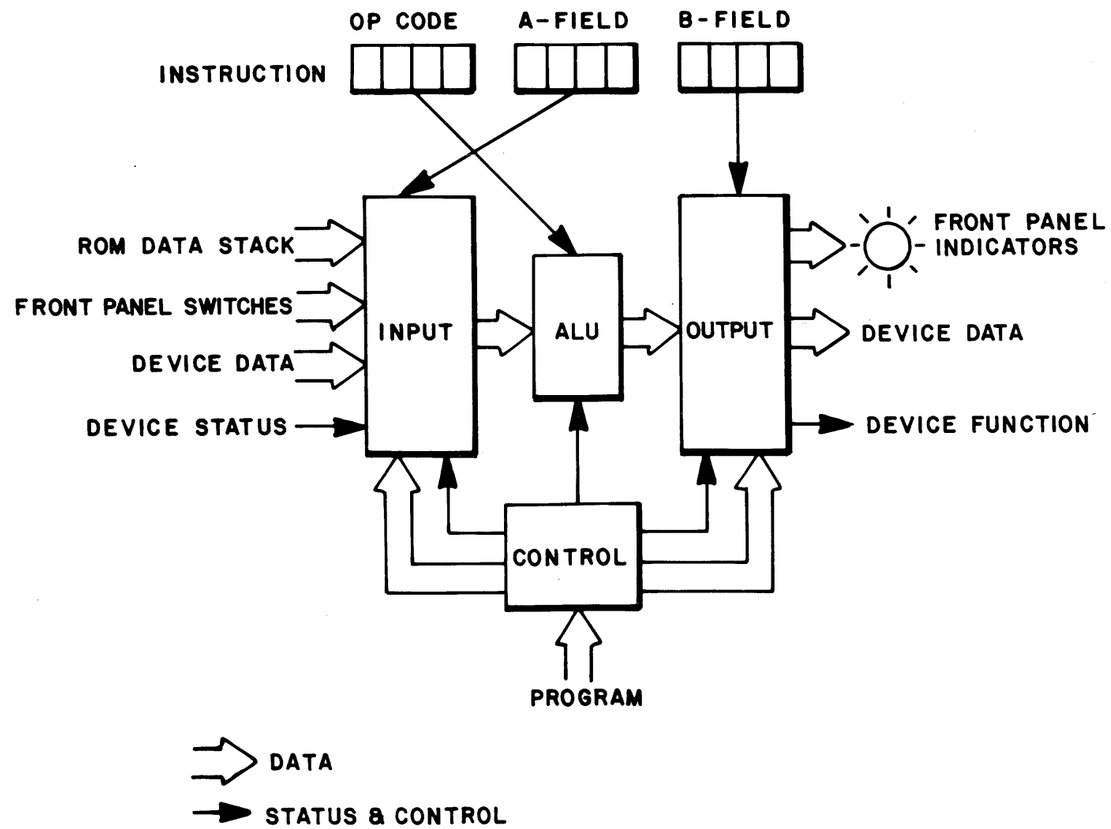
Each instruction is composed of twelve bits. The first four bits generally contain the op code, which tells what modification is to be made to the data. The next four bits comprise the A-field, which points to the data source. The last four bits make up the B-field, which identifies the final destination of the data. For example, an instruction could be written telling the microprocessor to take data from the constant factor Data Stack (A-field), complement it (op code), and display it in one of the front panel indicators (B-field).

As information is transferred from one location to another, it can pass through the ALU unchanged, it can be modified, or it can be combined with data from a second location. (When data is combined, the B-field defines both the second data source and the final destination of the result.) If the data is to remain unchanged, a Move instruction would be executed. The data modification and combination instructions that can be performed by the ALU are as follows:

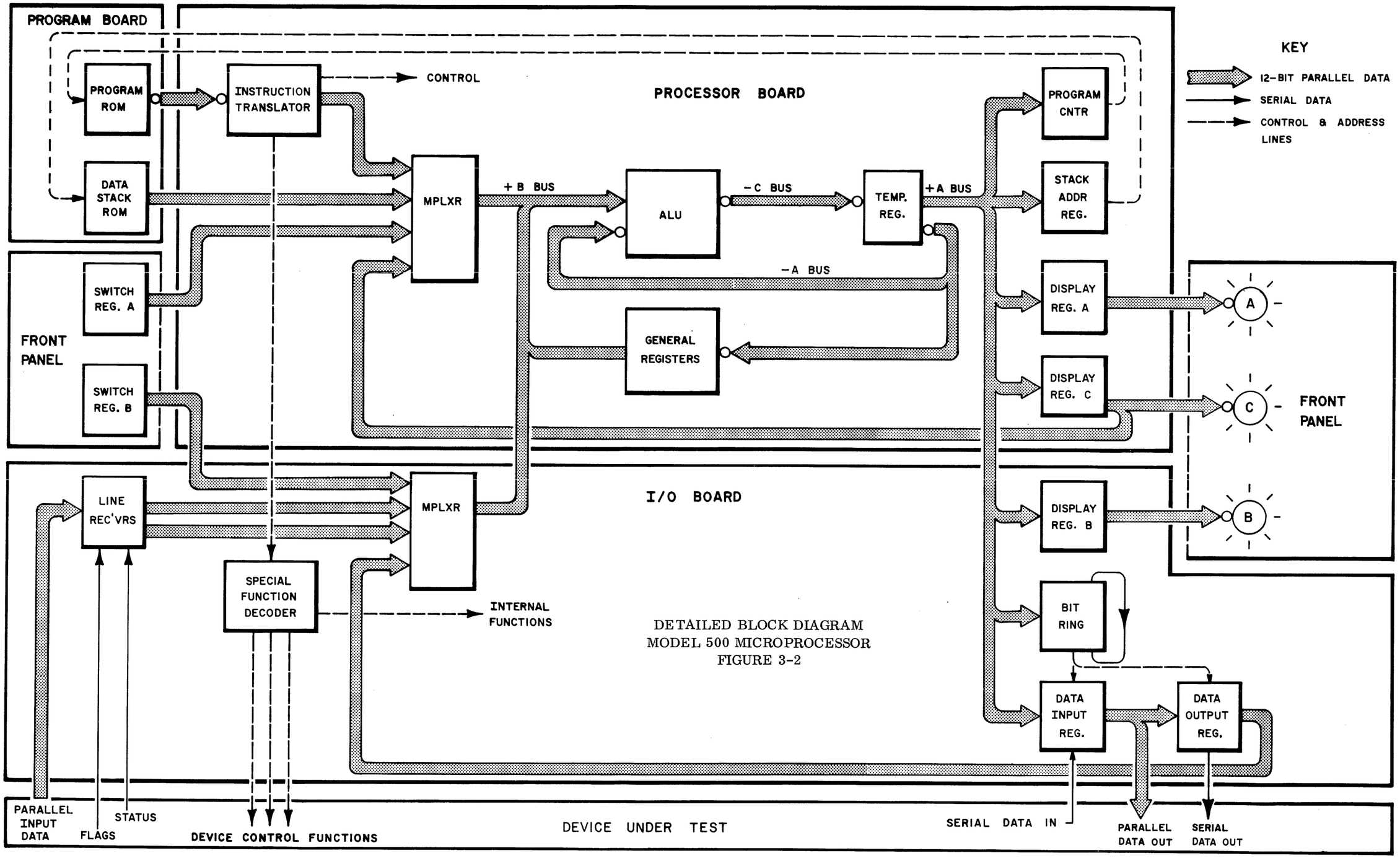
Complement
Increment
Decrement
Add
Subtract
And
Or
Exclusive-Or

These eight arithemetic and logical instructions and the Move and Compare instructions adhere strictly to the op code/A-field/B-field format.

There are three more instructions available, however, in which some of the various bits have different meanings. These three instructions (Branch, Special Control, and Load Zero) are explained in Paragraph 3.5 of this manual, along with a more detailed description of the other instructions.



BASIC BLOCK DIAGRAM
MODEL 500 MICROPROCESSOR
FIGURE 3-1



DETAILED BLOCK DIAGRAM
MODEL 500 MICROPROCESSOR
FIGURE 3-2

3.1.2 Logical Units

Figure 3-2 is a more detailed block diagram of the tester, with its important registers and other logical units identified. A brief description of each of these logical units follows:

3.1.2.1 Program ROM

The Program ROM physically consists of several ROM chips which contain the microprocessor program. A different Program card, containing a different program, is used to test each different type of device. The Program ROM contains a maximum of 1024 twelve-bit instructions. It is addressed by the Program Counter, and its output (the microprocessor program instruction) goes to the Instruction Translator.

3.1.2.2 Instruction Translator

The Instruction Translator consists of a ROM, a Multiplexer, and the ALU & GR Control Register. The primary function of the Instruction Translator is to convert the instruction bits into the proper ALU "op codes" and into the signals required to address the various registers and logical units.

3.1.2.3 Multiplexers

Two 4:1 multiplexers are used to select 12 bits of data from any of eight sources and put the data onto the B Bus, leading to the ALU. The Multiplexers are addressed by the Instruction Translator, and only one of the eight possible inputs is enabled at any one time.

3.1.2.4 B Bus

The B Bus is a 12-bit wide tri-state bus carrying data from the multiplexers and the General Registers to the ALU. Data on the B Bus is in its true form.

3.1.2.5 ALU

The Arithmetic/Logic Unit performs all of the mathematical and logical functions, as dictated by each instruction op code. Its two data inputs are the B Bus and the -A Bus. Its control comes from the ALU & GR Control Register, part of the Instruction Translator. Its output is the -C Bus, which carries data to the Temporary Register.

3.1.2.6 C Bus

The -C Bus is the main artery from the ALU to the Temporary Register. Data on the -C Bus is in complementary form. This bus is also 12 bits wide.

3.1.2.7 Temporary Register

The Temporary Register consists of 12 flip-flops and associated circuitry. It is used to store partially-processed data temporarily for feedback to the ALU, and to hold fully-processed data for output to the other registers and logical units. Input is from the -C Bus and output goes to two buses: True output goes to the +A Bus and complementary output goes to the -A Bus.

3.1.2.8 A Bus

These two buses are the complementary outputs of the Temporary Register. The +A Bus feeds many of the output logical units. The -A Bus feeds back to the ALU and supplies data to the General Registers. +A Bus data is in its true form; -A Bus data is complementary.

3.1.2.9 General Registers

There are 16 twelve-bit general-purpose registers which are used by the program to store data. Input is from the -A Bus, and addressing of the 16 registers is from the ALU & GR Control Register. The General Registers consist physically of three 16-word by 4-bit Random Access Memory (RAM) ICs. Since there is a natural inversion within these chips, data is put out on the +B Bus in its true form.

3.1.2.10 Data Stack ROM

This is the constant-factor storage area on the Program board containing data constants needed by each particular program. It can contain up to 256 twelve-bit constants. It is addressed by the Stack Address Register, and output goes to the Multiplexer for routing to the +B Bus.

3.1.2.11 Switch Registers A, B

These are the two rows of switches on the front panel. Output, twelve bits for each register, goes to the Multiplexer.

3.1.2.12 Line Receivers

Parallel Data, and Flag and Status information from the connected device is applied to the Multiplexer for routing onto the +B Bus. Flag Bits are stored, but there is no intermediate register for storage of data or status bits. Some of these bits also illuminate front panel status indicators.

3.1.2.13 Special Function Decoder

The fields of the Special Control instruction are decoded here to initiate or terminate particular functions in both the tester and the device under test. Tester functions such as "Wait for Bit Ring", and device functions such as Read, Write, Restore, Etc., are selected through this special Control Register.

3.1.2.14 Program Counter

The Program Counter is a 12-stage binary counter used to address the Program ROM. The two high-order outputs are not normally used. The Program Counter is normally incremented by one after executing each instruction, but it can have an entirely new value loaded into it in parallel through execution of a Branch instruction.

3.1.2.15 Stack Address Register

This is an 8-bit register used to access the constant factor Data Stack ROM. Whenever an instruction specifies the Data Stack ROM as the input source, the data is pulled from the ROM location specified by the Stack Address Register. Therefore, retrieving a constant is usually a 2-step operation: the first step is to load the desired address into the Stack Address Register, and the second step would be to Move (Add, Subtract, etc.) the constant to the desired location. Input to the Stack Address Register is from the +A Bus.

3.1.2.16 Display Registers A, B, C

Each of the display registers consists of twelve latches which are loaded from the +A Bus. Their outputs go to the corresponding LEDs on the front panel, for visual indication to the operator. The front panel LEDs light up when the corresponding latch is RESET, so the LEDs actually display the complement of the data stored in the display register. Display Register C also has its output routed back to the Multiplexer for input to the ALU.

3.1.2.17 Bit Ring

The Bit Ring is a twelve-bit shift register capable of being clocked by the device (disk) Read Clock or by one of the internal Write oscillators. It is normally utilized by first loading a single "one" into it and then shifting the "one" around by clocking it with either the Read Clock or the Write Clock. With the microprocessor having first executed the "wait for bit ring" Special Function, the processor clock stops until the Read Data is fully shifted in (to the Data Input Register) or until the Write Data is fully shifted out (of the Data Output Register). By this time the single "one" has been shifted around to the LSB position of the Bit Ring, allowing the processor clock to restart.

The Bit Ring can be permuted to an 8-bit ring to handle 8-bit data bytes. This is accomplished by prior execution of Special Control Function 23_{16}.

The Bit Ring cannot be loaded while either Read Control, Write Serial, or Bit Ring Auto Shift (Special Functions 03, 05, and 0B, respectively) are valid. The complementary Special Function (02, 04, or 0A) must be executed before the Bit Ring can be loaded.

The contents of the Bit Ring cannot be accurately predicted after turning off Write Serial, so in these cases the Bit Ring must be reloaded before it can be used again.

3.1.2.18 Data Input Register

This is a 12-bit register with both serial and parallel input, and parallel output. Serial input is from the device being tested. Parallel input is from the +A Bus. The parallel output data normally goes to the Data Output Register, but it is also available to the device being tested.

3.1.2.19 Data Output Register

This is a 12-bit register with parallel input and both serial and parallel output. Input is from the Data Input Register. Serial output is to the device being tested. Parallel output is to the Multiplexer for routing to the +B Bus. Parallel loading is disabled (serial shifting is enabled) only when performing a Disk Write.

3.2 TIMING

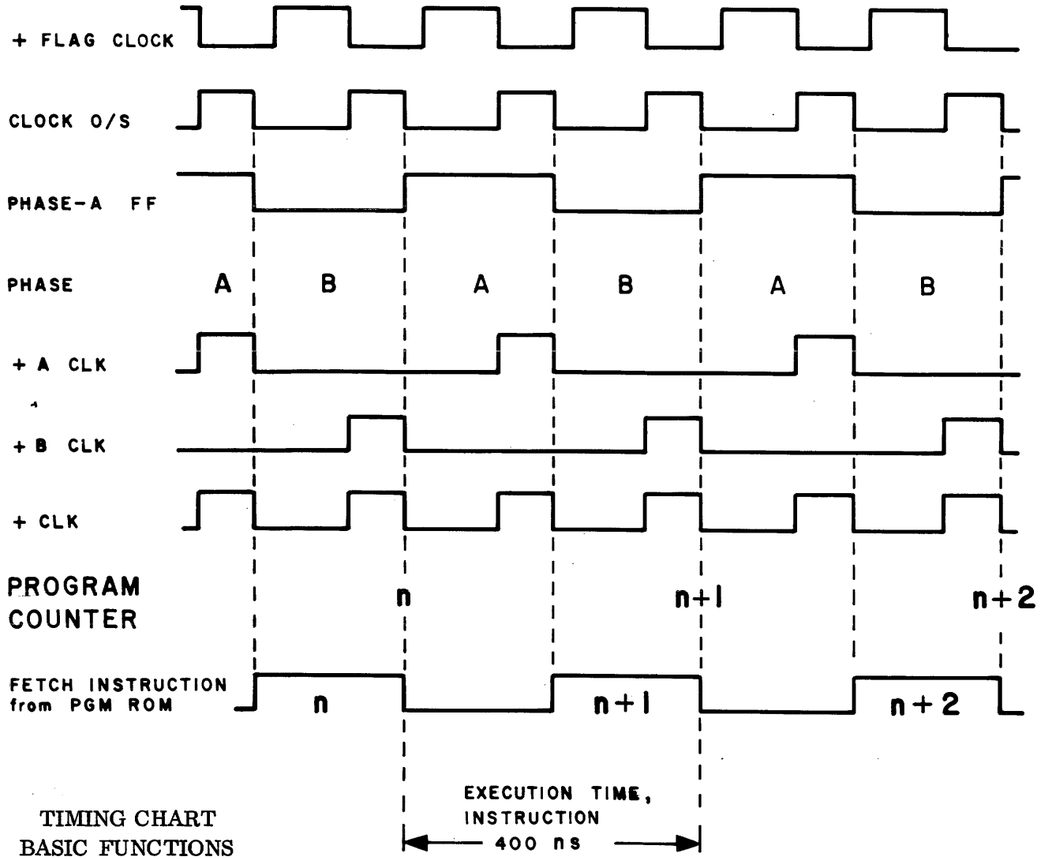
Figure 3-3 is a chart depicting the important timing signals and functions within the microprocessor. The oscillator runs at 5 MHz and drives +FLAG CLK at the same frequency. +FLAG CLK fires the CLOCK O/S every 200 ns, which times out after 70 ns and toggles the PHASE A flip-flop.

Instruction execution requires 400 ns. The execution of each instruction is broken up into two parts, called Phase A and Phase B. The phase is determined by the state of the Phase A flip-flop. The +A CLK signal occurs during the last 70 ns of Phase A and the +B CLK signal occurs during the last 70 ns of Phase B.

The Program Counter is incremented at the end of Phase A. Refer to the timing diagram (Figure 3-3) and note that this is at approximately the midpoint of instruction execution. This allows ample time for the Program ROM to be addressed at the next instruction location before its code bits are clocked into the Instruction Translator (ALU & GR Control Register). The instruction is actually fetched while the preceding instruction is still being executed.

3.3 BASIC INSTRUCTION CYCLE (Figure 3-4)

Fundamentally, the ALU receives data from the +B Bus and from the -A Bus, manipulates the data as dictated by the control code, and puts the result out on the -C Bus. Depending upon the control code, any of the arithmetic or logic operations can be performed on the data, or it can pass through unchanged.



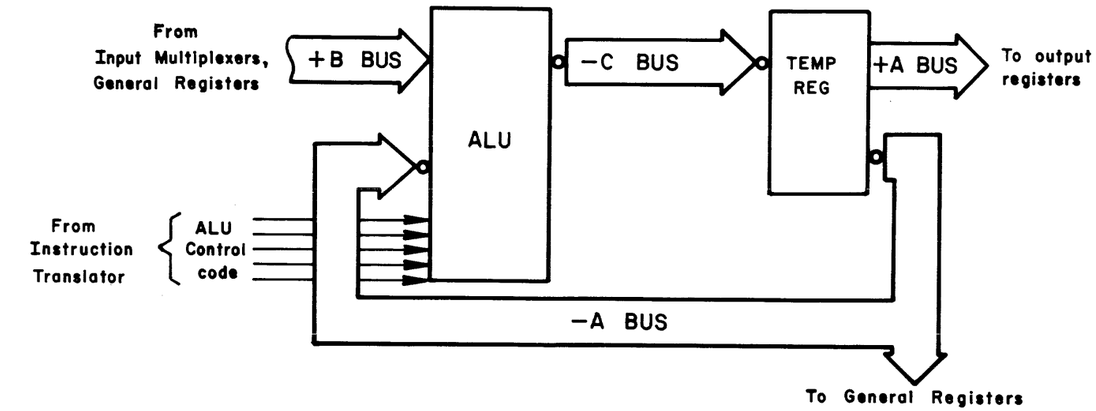
TIMING CHART
BASIC FUNCTIONS
FIGURE 3-3

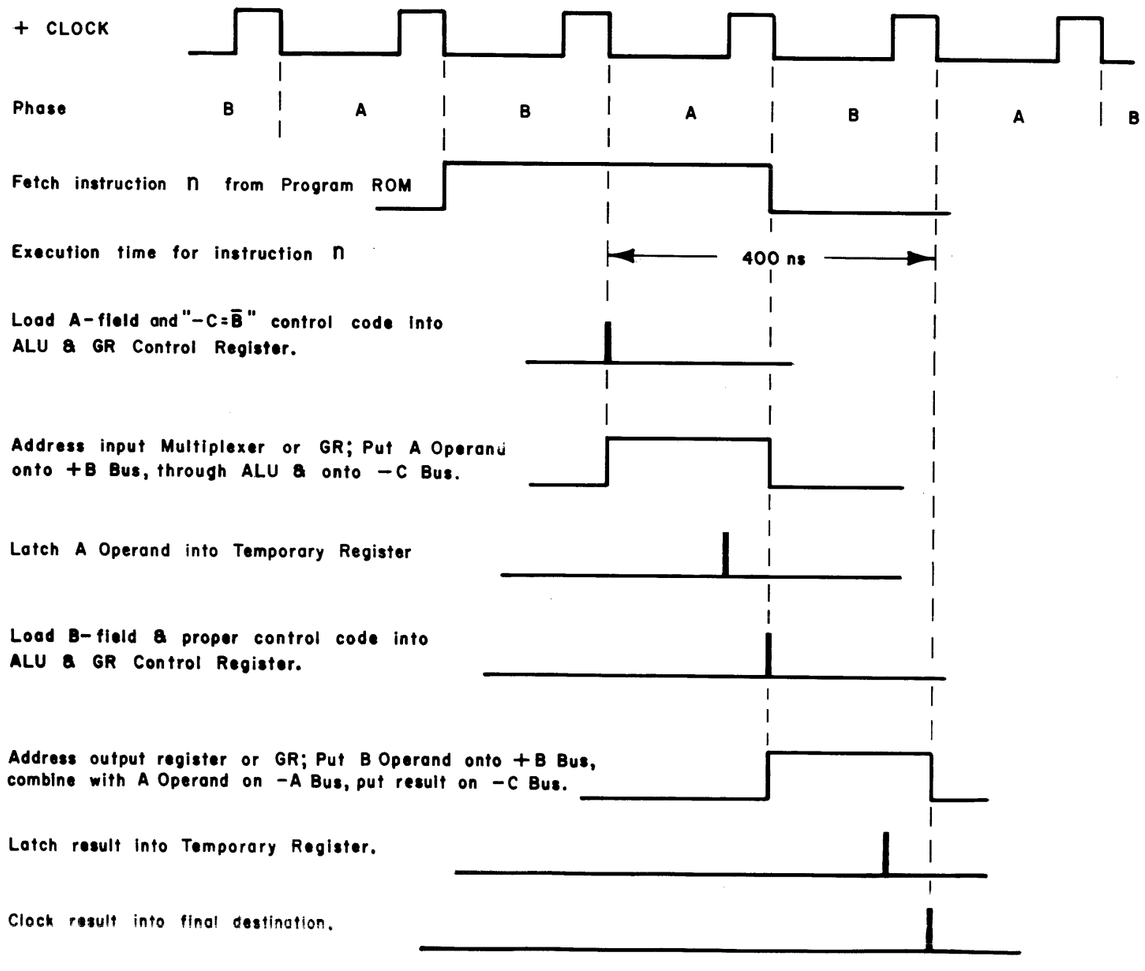
Since many instructions employ two operands, the A Operand is moved into the Temporary Register during Phase A. It is then combined with the B Operand during Phase B to produce the final result.

During Phase A, the A operand is placed onto the +B Bus and the ALU is given a control code that causes the ALU output (-C Bus) to become the complement of the +B Bus ($-C = \overline{B}$). The prior contents of the Temporary Register, resting on the -A Bus at the input to the ALU, are blocked by this $-C = \overline{B}$ control code. At A-Clock, this -C data is clocked into the Temporary Register.

Once the A Operand is in the Temporary Register, its complement is available on the -A Bus for input to the ALU. Now, during Phase B, the B Operand is applied to the +B Bus, the proper control code (dictated by the instruction) is applied to the ALU, and the result is available on the -C Bus. At the leading edge of B-Clock, this result is clocked into the Temporary Register, replacing the A Operand, and at the end of Phase B this result is clocked into the Output Register or General Register which is its final destination.

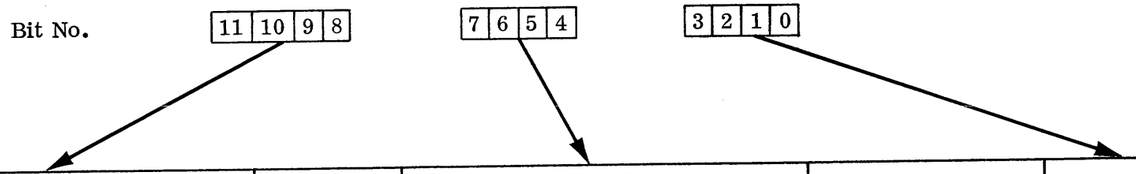
All instructions use the same ALU control code ($-C = \overline{B}$) during Phase A. (The -C Bus carries data in its complementary form simply because it requires less hardware to do it this way.) The ALU control code is then changed during Phase B to accomplish the data manipulation or combination required by the instruction.





TIMING CHART
BASIC INSTRUCTION CYCLE

FIGURE 3-4



MNEMONIC	OPERATION	HEX	A-FIELD (SOURCE)	BINARY	B-FIELD (DESTINATION)
CPR	COMPARE	0	GENERAL REGISTER 0*	0 0 0 0	GENERAL REGISTER 0*
ADD	ADD	1	GENERAL REGISTER 1	0 0 0 1	GENERAL REGISTER 1
SUB	SUBTRACT	2	GENERAL REGISTER 2	0 0 1 0	GENERAL REGISTER 2
AND	AND	3	GENERAL REGISTER 3	0 0 1 1	GENERAL REGISTER 3
OR	OR	4	GENERAL REGISTER 4	0 1 0 0	GENERAL REGISTER 4
DEC	DECREMENT	5	GENERAL REGISTER 5	0 1 0 1	GENERAL REGISTER 5
INC	INCREMENT	6	GENERAL REGISTER 6	0 1 1 0	GENERAL REGISTER 6
MOV	MOVE	7	GENERAL REGISTER 7	0 1 1 1	GENERAL REGISTER 7
CPL	COMPLEMENT	8	PROGRAM ROM	1 0 0 0	NOT USED
XOR	EXCLUSIVE-OR	9	DISPLAY REGISTER C	1 0 0 1	NOT USED
BR	BRANCH	A	SWITCH REGISTER A	1 0 1 0	DISPLAY REGISTER B
SPC	SPECIAL CONTROL	B	ROM STACK	1 0 1 1	DISPLAY REGISTER A
LDZ	LOAD GENERAL REGISTER 0**	C	SWITCH REGISTER B	1 1 0 0	DISPLAY REGISTER C
	LOAD GENERAL REGISTER 0	D	DATA OUTPUT REGISTER	1 1 0 1	STACK ADDRESS REGISTER
	LOAD GENERAL REGISTER 0	E	PARALLEL DATA IN	1 1 1 0	BIT RING
	LOAD GENERAL REGISTER 0	F	STATUS IN	1 1 1 1	DATA INPUT REGISTER

BRANCH QUALIFIERS (B-FIELD)

0 UNCONDITIONAL
1 ZERO
2 NOT ZERO
3 MINUS
4 NOT SECTOR MARK
5 NOT MISSING CLOCKS
6 (NOT USED)
7 (NOT USED)

*General Registers 8-15 are accessible through prior execution of SPECIAL CONTROL FUNCTIONS.

**LOAD (11XX----XX) puts the value 00XX----XX into General Register 0.

INSTRUCTION FORMAT

FIGURE 3-5

This sequence is followed by most instructions, but the Branch, Special Control, and Load Zero instructions are performed somewhat differently. These three instructions are covered in more detail in paragraph 3.5.

3.3.1 Condition Codes

There are two "Condition" flip-flops that can become set or reset at (or near) the end of instruction execution. The Zero flip-flop sets whenever the -C Bus contains numeric zero (all bits high) at the beginning of B-Clock time. The Minus flip-flop sets whenever bit 11 of the +A Bus is a 1 at the end of B-Clock time. The Zero and Minus flip-flops reset upon completion of any instruction resulting in non-zero or non-minus conditions, respectively. These two flip-flops thus store the conditions resulting from every instruction execution, so that the conditions can be tested by a subsequent Branch instruction to enable conditional branch functions. Note that the conditions are present only for the following instruction cycle: each new instruction is capable of setting up new conditions. Note also that the two conditions are mutually exclusive: if Zero is true, Minus cannot be true, and vice versa.

3.4 INSTRUCTION FORMAT

Most of the necessary information for all instructions is summarized in Figure 3-5. The only information not included is a list of the meaning of the A- and B-fields during the Special Control instruction: this is presented later in Table 3-1.

3.4.1 Operation Code

Bits 11, 10, 9 and 8 of the instruction are the Operation Code or Op Code. A value of 0000 through 1011 causes the corresponding operation on the chart to occur. A value of 11XX in bits 11 and 10 initiates a Load Zero instruction, regardless of the state of bits 9 and 8.

3.4.2 A-Field

For all instructions other than Special Control and Load Zero, the A-field points to the source of the data to be moved or modified. For example, a value of 1010 in bits 7, 6, 5 and 4 will take the twelve bits of data represented by the settings of the twelve Register-A toggle switches on the front panel, and use these twelve bits as the A Operand. Similarly, a value of 0111 in instruction bits 7, 6, 5, and 4 will take the twelve data bits presently stored in General Register 7 as the A Operand. General Registers 8-15 can be accessed by having an A-field of 0-7, respectively, after executing Special Control Function 13_{16} (see 3.5.13). The special use of the A-field in Load Zero and Special Control will be reviewed shortly (3.5.11 and 3.5.13).

3.4.3 B-Field

For instructions requiring two operands (Add, Subtract, Compare, And, Or, and Exclusive-Or) the B-field points to the source of the second operand. For example, if an Add instruction has a value of 0011 in bits 3, 2, 1 and 0, the A Operand will be added to the contents of General Register 3. For all instructions other than Compare, Branch, Special Control, and Load Zero, the B-field also points to the ultimate destination of the result. In the preceding example, the sum of the addition would appear in General Register 3. General Registers 8-15 can be accessed instead of General Registers 0-7, respectively, by first executing Special Control Function 15_{16} (see 3.5.13).

3.5 INSTRUCTION REPERTOIRE

In the following paragraphs, parentheses should be interpreted as meaning "the contents of", e.g., (A) means "the contents of A".

3.5.1 Move (MOV)

Op Code = 0111 = 7
A-field = address of data to be moved (Operand)
B-field = address of destination
(A)→B
The 12 bits of the Operand are duplicated into the B-address.
The contents of the A-address remain unchanged.

3.5.2 Complement (CPL)

Op Code = 1000 = 8
A-field = address of Operand
B-field = address of destination
$(\bar{A})$→B
The ones complement of the Operand is moved to the B-address. The contents of the A-address remain unchanged.

NOTE

In all instructions other than Move and Compare, the reference to "the contents of the A-address" or the "A Operand" being "unchanged" assumes that the A Operand and the B Operand are NOT contained in the same register. For example, during Complement, the contents of the A-address remain unchanged, UNLESS the A- and B-adress BOTH refer to the same register. In this case, of course, the contents of the specified register would become complemented.

3.5.3 Increment (INC)

Op Code = 0110 = 6
A-field = address of Operand
B-field = address of destination
(A) + 1→B
The 12 bits of the Operand are incremented by a binary 1 and the sum is moved to the B-address. The contents of the A-address remain unchanged.

3.5.4 Decrement (DEC)

Op Code = 0101 = 5
A-field = address of Operand
B-field = address of destination
(A) - 1→B
The 12 bits of the Operand are decremented by a binary 1 and the difference is moved to the B-address. The contents of the A-address remain unchanged.

3.5.5 Add (ADD)

Op Code = 0001 = 1
A-field = address of A Operand
B-field = address of B Operand and Sum
(A) + (B)→B
The 12 bits of the A Operand are added to the 12 bits of the B Operand. The sum replaces the B Operand. The A Operand is unchanged.

NOTE

The B Operand of the Add, Subtract, Compare, And, Or, and Exclusive-Or instructions is always a General Register, regardless of the state of Program Bit 3 in the B-field. When the B-field contains an address from 8 to 15, the contents of the corresponding General Register 0 to 7 are used as the B Operand, and NOT the contents of the register specified by the B-field. The B-field does, however, point directly to the destination of the answer (except in Compare). For example, if the B-field contains 1111, specifying the Data Input Register, the contents of General Register 7 are used as the B Operand instead. The result is placed in the Data Input Register, and the contents of General Register 7 are not changed.

General Registers 8-15 will be used instead of Registers 0-7 if the "B-FIELD" is set by prior execution of Special Control Function 15_{16}.

3.5.6 Subtract (SUB)

Op Code = 0010 = 2
A-field = address of A Operand (Minuend)
B-field = address of B Operand (Subtrahend) and Difference
(A)-(B)→B
The 12 bits of the B Operand are subtracted from the 12 bits of the A Operand, using twos-complement addition. The difference replaces the B Operand. The A Operand is unchanged. The B Operand is always a General Register, as noted in 3.5.5.

3.5.7 Compare (CPR)

Op Code = 0000 = 0
A-field = address of A Operand (Minuend)
B-field = address of B Operand (Subtrahend)
(A)-(B)→Condition flip-flops

The 12 bits of the B operand are subtracted from the 12 bits of the A Operand. The difference is not stored or saved anywhere--the purpose of this instruction is to set conditions which can be tested by a subsequent Branch instruction. Neither operand is changed. The B Operand is always a General Register, as noted in 3.5.5.

Resulting Conditions are stored in the Zero and Minus flip-flops as follows:

	ZERO	MINUS
Difference is positive*	Reset	Reset
Difference is Zero	Set	Reset
Difference is Negative*	Reset	Set

*Provided system limits are not exceeded, causing carry or borrow to affect sign bit (MSB).

3.5.8 And (AND)

Op Code = 0011 = 3
A-field = address of A Operand
B-field = address of B Operand and Product
(A) AND (B)→B

The 12 bits of the A Operand are logically ANDed with the 12 bits of the B Operand. The product replaces the B Operand. The A Operand is unchanged. The B Operand is always a General Register, as noted in 3.5.5.

3.5.9 Or (OR)

Op Code = 0100 = 4
A-field = address of A Operand
B-field = address of B Operand and Sum
(A) OR (B)—►B

The 12 bits of the A Operand are logically ORed with the 12 bits of the B Operand. The sum replaces the B Operand. The A Operand is unchanged. The B Operand is always a General Register, as noted in 3.5.5.

3.5.10 Exclusive Or (XOR)

Op Code = 1001 = 9
A-field = address of A Operand
B-field = address of B Operand and Difference
(A) XOR (B)—►B

The 12 bits of the A Operand are EXCLUSIVE-ORed with the 12 bits of the B Operand. The difference replaces the B Operand. The A Operand is unchanged. The B Operand is always a General Register, as noted in 3.5.5.

3.5.11 Load Zero (LDZ)

Op Code 11XX = C, D, E, or F
A-field = Data
B-field = Data
PGM Bits $\overline{11}\cdot\overline{10}\cdot 9\text{-}0$—►G.R. 0

Bits 11 and 10 of the instruction both being 1 denote a Load Zero instruction, in which the balance of the instruction bits are loaded into General Register 0. Bits 11 and 10 of General Register 0 are forced to 0. With bit 11 being 0, the Minus condition flip-flop resets upon execution of the Load Zero instruction.

NOTE

The Load Zero instruction always loads General Register 0, even if General Registers 8-15 had been enabled by a prior execution of Special Control Function 13_{16} or 15_{16}. Thus, if a branch is to be made to an address loaded from the Program ROM, the lower General Registers (0-7) must be enabled before the branch occurs. In the following program sequence, a branch would be made to the instruction address specified by General Register 8, NOT General Register 0.

HEX	MNEMONIC	FIELDS A	FIELDS B	DESCRIPTION
B13	EAFLD	1	3	Enable A-FIELD (Enable GRs 8-15 in A-field)
Cxx	LDZ	DATA		Load GR0
A00	BR	0	0	Branch Unconditional

In order to load the new address into General Register 0 and then branch to the new address, the sequence must be modified, such as:

HEX	MNEMONIC	FIELDS A	FIELDS B	DESCRIPTION
B13	EAFLD	1	3	Enable A-FIELD (Enable GRs 8-15 in A-field)
B12	DAFLD	1	2	Disable A-FIELD (Enable GRs 0-7 in A-field)
Cxx	LDZ	DATA		Load GR0
A00	BR	0	0	Branch unconditional

3.5.12 Branch (BR)

Op Code = 1010 = A
A-field = address of Operand
B-field = Branch qualifier
(A)→PC, if "B"

If the conditions specified by the qualifier (B-field) are present, the 12 bits of the Operand are loaded into the Program Counter, becoming the address of the next program instruction. The branch qualifiers and corresponding conditions are as follows:

BRANCH QUALIFIER	CONDITION
0	None (Unconditional Branch)
1	Zero
2	Not Zero
3	Minus
4	Not Flag 5 (Status In 5)
5	Not Address Mark Detected
6	(Not Used)
7	(Not Used)

3.5.13 Special Control Functions (SPC)

Op Code = 1011 = B
A-field = MSD of Special Function List
B-field = LSD of Special Function List
AB→Special Function Decoder

The A-field and B-field are decoded directly into addressable latches which perform the stated function. Once initiated, the function generally remains effective until cancelled by a complementary Special Control Function. The list of functions appears in Table 3-1. Functions pertaining to OUT CONTROL signals are explained more fully in the program manuals for each device.

TABLE 3-1

SPECIAL CONTROL FUNCTIONS

MNEMONIC	A-FIELD		B-FIELD		FUNCTION
DOC0	0 0 0 0	0	0	0 0 0 0	Disable Output Control 0
EOC0	0 0 0 0	0	1	0 0 0 1	Enable Output Control 0
DREAD	0 0 0 0	0	2	0 0 1 0	Disable Read Control
EREAD	0 0 0 0	0	3	0 0 1 1	Enable Read Control
DWTS	0 0 0 0	0	4	0 1 0 0	Disable Write Serial
EWTS	0 0 0 0	0	5	0 1 0 1	Enable Write Serial
DOC1	0 0 0 0	0	6	0 1 1 0	Disable Output Control 1
EOC1	0 0 0 0	0	7	0 1 1 1	Enable Output Control 1
DOC2	0 0 0 0	0	8	1 0 0 0	Disable Output Control 2
EOC2	0 0 0 0	0	9	1 0 0 1	Enable Output Control 2
DBRASH	0 0 0 0	0	A	1 0 1 0	Disable Bit Ring Auto Shift
EBRASH	0 0 0 0	0	B	1 0 1 1	Enable Bit Ring Auto Shift
DOC3	0 0 0 0	0	C	1 1 0 0	Disable Output Control 3
EOC3	0 0 0 0	0	D	1 1 0 1	Enable Output Control 3
DOC4	0 0 0 0	0	E	1 1 1 0	Disable Output Control 4
EOC4	0 0 0 0	0	F	1 1 1 1	Enable Output Control 4
	0 0 0 1	1	0	0 0 0 0	
	0 0 0 1	1	1	0 0 0 1	
DAFLD	0 0 0 1	1	2	0 0 1 0	Enable Gen. Regs. 0-7 (A-field)
EAFLD	0 0 0 1	1	3	0 0 1 1	Enable Gen. Regs. 8-15 (A-field)
DBFLD	0 0 0 1	1	4	0 1 0 0	Enable Gen. Regs. 0-7 (B-field)
EBFLD	0 0 0 1	1	5	0 1 0 1	Enable Gen. Regs. 8-15 (B-field)
DOC5	0 0 0 1	1	6	0 1 1 0	Disable Output Control 5
EOC5	0 0 0 1	1	7	0 1 1 1	Enable Output Control 5
DOC6	0 0 0 1	1	8	1 0 0 0	Disable Output Control 6
EOC6	0 0 0 1	1	9	1 0 0 1	Enable Output Control 6
DOC7	0 0 0 1	1	A	1 0 1 0	Disable Output Control 7
EOC7	0 0 0 1	1	B	1 0 1 1	Enable Output Control 7
DOC8	0 0 0 1	1	C	1 1 0 0	Disable Output Control 8
EOC8	0 0 0 1	1	D	1 1 0 1	Enable Output Control 8
	0 0 0 1	1	E	1 1 1 0	
	0 0 0 1	1	F	1 1 1 1	
	0 0 1 0	2	0	0 0 0 0	
	0 0 1 0	2	1	0 0 0 1	
DBYMD	0 0 1 0	2	2	0 0 1 0	Disable Byte Mode
EBYMD	0 0 1 0	2	3	0 0 1 1	Enable Byte Mode
DMSCLK	0 0 1 0	2	4	0 1 0 0	Disable Missing Clock Detection
EMSCLK	0 0 1 0	2	5	0 1 0 1	Enable Missing Clock Detection
DSKCKO	0 0 1 0	2	6	0 1 1 0	Disable Skip Clock Out
ESKCKO	0 0 1 0	2	7	0 1 1 1	Enable Skip Clock Out
	0 0 1 0	2	8	1 0 0 0	
	0 0 1 0	2	9	1 0 0 1	
	0 0 1 0	2	A	1 0 1 0	
	0 0 1 0	2	B	1 0 1 1	
TPAL	0 0 1 0	2	C	1 1 0 0	Test Point A Low
TPAH	0 0 1 0	2	D	1 1 0 1	Test Point A High
TPBL	0 0 1 0	2	E	1 1 1 0	Test Point B Low
TPBH	0 0 1 0	2	F	1 1 1 1	Test Point B High
WBTRNG	0 0 1 1	3	0	0 0 0 0	Wait for Bit Ring
CLRFGS	0 0 1 1	3	1	0 0 0 1	Clear Flag Storage
	0 0 1 1	3	2	0 0 1 0	
	0 0 1 1	3	3	0 0 1 1	

3.6 LOGIC INTRODUCTION

Immediately following is a brief discussion of the Programmable Tester's logic in general. Then the larger part of this section is devoted to analysis of the logic diagrams.

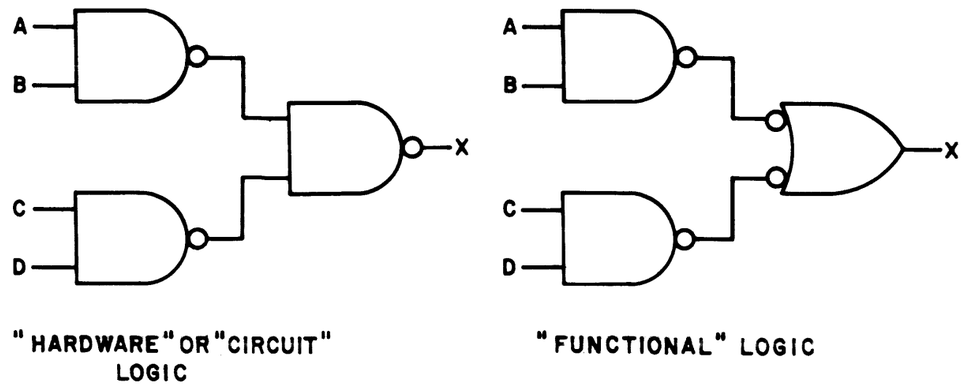
3.6.1 Positive Logic

Positive logic is used throughout the Programmable Tester. The following relationships are valid:

	TRUE	FALSE
Nominal	+5V	0V
Minimum	+2V	0V
Maximum	+5.5V	+.8V

3.6.2 Functional Logic

The Programmable Tester logic diagrams utilize "functional" logic, as opposed to "circuit" or "hardware" logic. This means that the symbol used to depict a gate is the symbol representative of that gate's function in the logic, and not necessarily the symbol appearing in the manufacturer's data sheets. Figure 3-6 illustrates two methods of drawing the same circuitry. The functional example clearly shows that the signal "X" is produced by either of two conditions, A·B or C·D. The functional depiction also identifies signal levels needed at any point in the circuit to produce the desired output: a low level on either of the lines having "bubbles" on its ends will make "X" active.



"HARDWARE" LOGIC VS. "FUNCTIONAL" LOGIC

FIGURE 3-6

3.6.3 Signal Names

Signal names in the tester are not limited to a maximum number of characters or digits, so they are generally self-explanatory. However, in the interface area, many names are general in nature because they must be compatible with a variety of devices. Refer to the interface section (Section 2) for further details.

All signal names are preceded with either a plus sign (+) or a minus sign (-). The plus represents an active high signal; the minus represents an active low signal. For example, if -GEN CLR is low (0 volts), the General Clear function is active. If -GEN CLR is high (+5 volts), the General Clear function is inactive. If +MINUS is low, the Minus flip-flop is reset; if +MINUS is high, the Minus flip-flop is set.

Signal names appearing in the text will be printed in all capital letters so that signals will not be confused with functions that are being performed. For example, +PHASE A is a signal name, whereas Phase A refers to the first phase of instruction execution in general.

3.7 CIRCUIT DESCRIPTION

The remainder of this section is keyed to the logic diagrams, which can be found in the last section of this manual. Each page of each logic diagram will be discussed following the order in which the diagrams appear. It is suggested that these diagrams be kept handy for reference while studying these circuit descriptions.

The five logic printed circuit boards in the Programmable Tester are as follows:

NAME	MNEMONIC	PART NO.
PROCESSOR BOARD	PROC	21037
I/O LOGIC BOARD	I/O	21035
PROGRAM BOARD	PRGM	*
WRITE OSCILLATOR BOARD	WOSC	21031
DISPLAY BOARD	DISP	21033

*Program Board part numbers vary according to the program they contain.

3.7.1 Processor Board

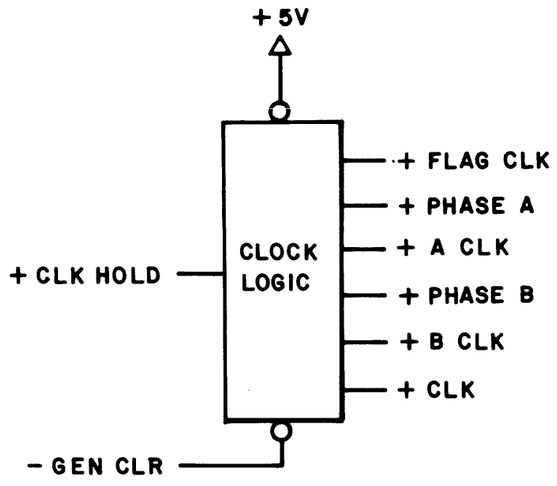
The major elements of the Processor board are Clock Logic, Stack Address Register and Program Counter, Instruction Translator, ALU and General Registers, Multiplexer, Display Registers A and C, and Miscellaneous Controls.

3.7.1.1 Clock Logic (Figure 3-7, PROC-SH1)

The 5MHz crystal oscillator runs whenever power is on, producing +FLAG CLK. In addition to triggering the Clock O/S, +FLAG CLK also leaves the processor board (via P3-6) to be used on the I/O board.

The Stop flip-flop is normally reset, allowing each +FLAG CLK to fire the Clock O/S. Each time the Clock O/S fires (for 70 ns) it does two things: first, it develops either +A CLK or +B CLK, depending upon the setting of the Phase A flip-flop. Second, at the end of the 70 ns period of the Clock O/S, the Phase A flip-flop toggles, enabling the other clock pulse to be developed at the next firing of the Clock O/S.

Both +A CLK and +B CLK develop +CLK and -CLK. +PHASE A and +PHASE B are complementary, alternating as the Phase A flip-flop toggles.

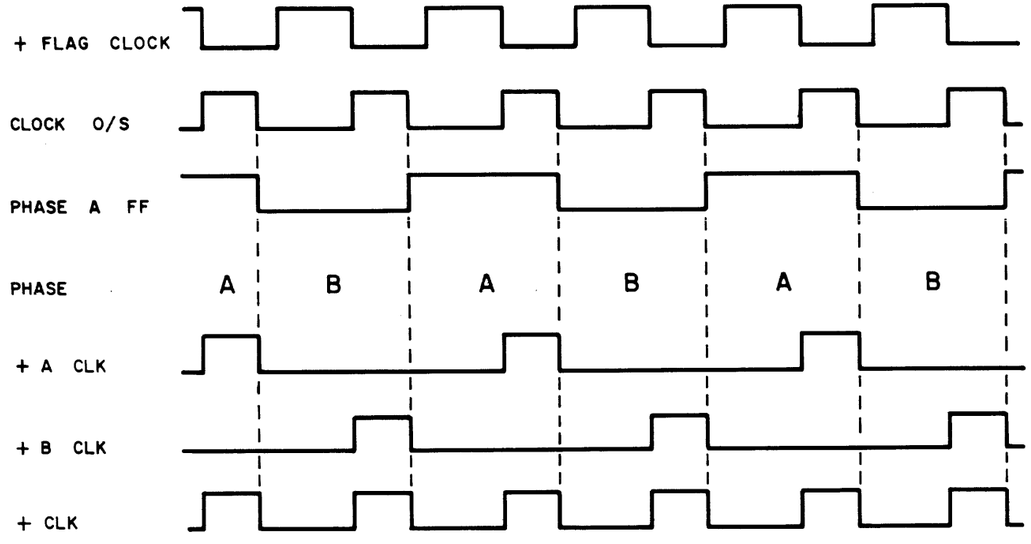


FUNCTIONAL BLOCK DIAGRAM
CLOCK LOGIC

FIGURE 3-7

All of these clocks run continuously until either the General Clear button is pushed or a Wait-for-Bit-Ring instruction is executed. In the case of General Clear, releasing the button allows normal operation to resume. In the latter case, Wait-for-Bit-Ring (Special Control Function 30_{16}) develops +CLK HOLD, allowing the Stop flip-flop to set. Then, when the Bit Ring cycle is completed, +CLK HOLD goes low, the Stop flip-flop resets, and normal operation resumes. General Clear can be used to override the Wait-for-Bit-Ring function if desired.

Part of Figure 3-3 is reproduced here as Figure 3-8 to illustrate Clock Logic timing relationships.



BASIC TIMING

FIGURE 3-8

3.7.1.2 Program Counter & Stack Address Register (Figure 3-9, PROC-SH2)

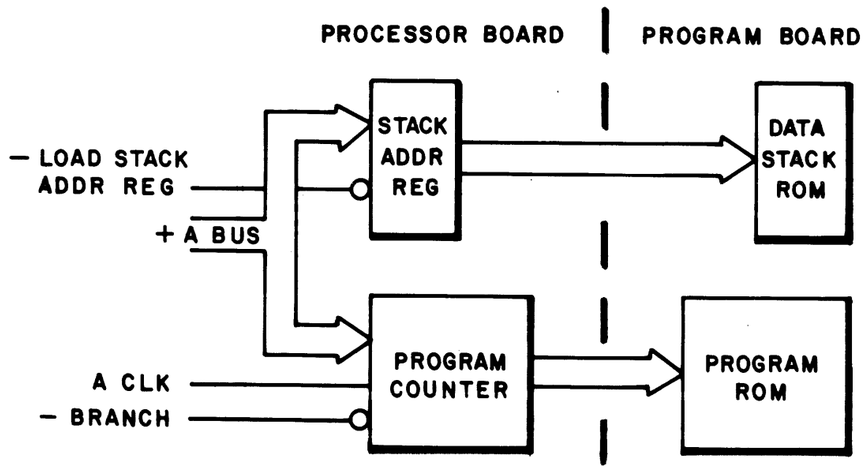
The Program Counter is a 12-bit binary counter that is normally incremented at the end of each A-Clock. Its outputs go to the Program Board to address the Program ROM. The two high-order outputs are not normally used, even though they are taken to the Program Board connector for possible future use.

The counter can be reset to zero by either the General Clear or the Program Reset pushbuttons. One of the two Enable inputs to each counter chip (EN-P) is connected to -BRANCH, which blocks counting when a branch is occurring. The other Enable input (EN-T) of the low-order counter chip is always enabled. The EN-T inputs to the two higher order chips are connected to the Carry output of the preceding chip, allowing each stage to increment only upon a carry from the preceding stage.

Execution of a successful Branch instruction parallel-loads the contents of the +A Bus into the Program Counter, and inhibits the counting operation. The 74161 chip was chosen for this counter because it features synchronous counting of all stages, thus eliminating "slivers" on the outputs.

The Stack Address Register is an 8-bit latch that is parallel-loaded from the +A Bus when the Stack Address Register is called out by the instruction B-Field. It can be cleared to zero by General Clear. Its outputs go to the Program Board to address the constant factor Data Stack ROM.

The Stack Address Register is physically composed of 74195 (9300) shift register chips which are hard-wired for parallel loading only.



FUNCTIONAL BLOCK DIAGRAM
PROGRAM COUNTER & STACK ADDRESS REGISTER

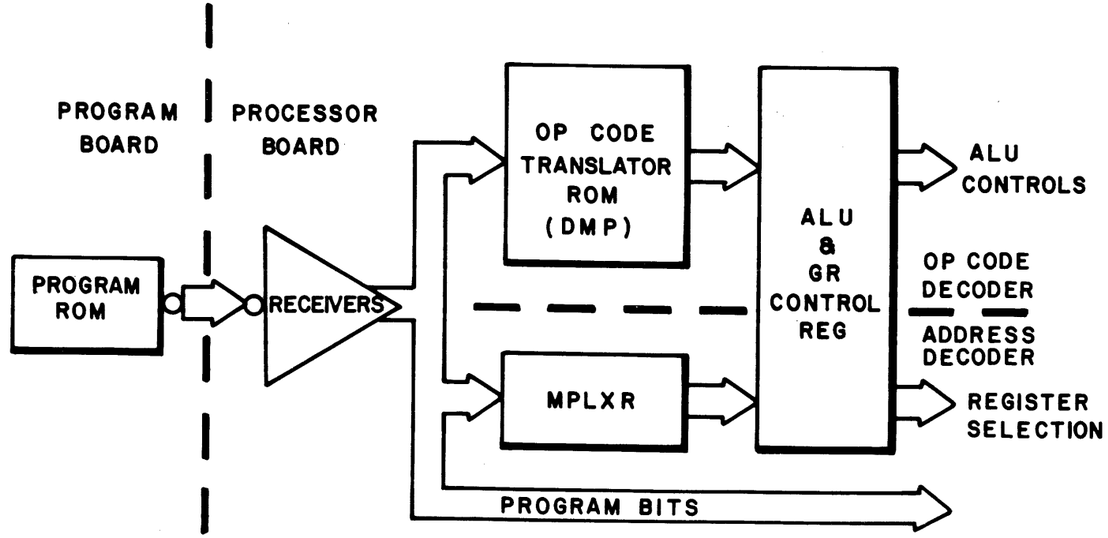
FIGURE 3-9

3.7.1.3 Instruction Translator (Figure 3-10, PROC-SH3)

There are two basic sections to the Instruction Translator; the Op Code Decoder and the Address Decoder. All translator outputs come from latches in the ALU & GR Control Register. These outputs supply the control codes to the ALU and provide addressing for A Operand and B Operand selection.

The Op Code Decoder is made up of a 32 x 8-bit ROM and associated ALU & GR Control Register latches. The ROM inputs are the four most significant bits of the instruction (from the Program ROM) and +PHASE A. Five of the eight decoder outputs (+ALU MODE, and +ALU SEL 0-3) combine to form the control code for the ALU. The other three outputs are developed in special cases: -BRANCH IF is developed only by Branch instructions, -GATED SPC INSTRUCTION is developed only by Special Control Function instructions, and +DONT SAVE RESULTS is developed at various times to block all transfer of data between internal registers.

The ROM is programmed so that during Phase B (the Phase B portion of the previous instruction) its output is always $B7 \cdot \overline{B6} \cdot B5 \cdot \overline{B4} \cdot B3$. The -CLK occurring at the end of Phase B sets this condition into the ALU & GR Control Register, which develops +ALU MODE·-ALU SEL 3·+ALU SEL 2·-ALU SEL 1·+ALU SEL 0 during the subsequent Phase A. This is the $-C = \overline{B}$ control code mentioned in paragraph 3.3, which results in the complement of the A Operand being transferred to the Temporary Register during the Phase A portion of every instruction.



FUNCTIONAL BLOCK DIAGRAM
INSTRUCTION TRANSLATOR

FIGURE 3-10

Also during Phase A the translator ROM decodes the Program ROM bits into the proper bit pattern to effect the desired operation of the ALU. The -CLK occurring at the end of Phase A loads this new configuration into the ALU & GR Control Register so that it is available to the ALU during the subsequent Phase B. Then the process repeats.

+CARRY is the inverse of +PROG BIT 8. It goes high when bit 8 is low, but is not necessarily used in all cases: it is used only in some arithmetic operations.

Table 3-2 summarizes the Op Code Decoder outputs for all instructions. Bear in mind that the ALU control codes appear first at the ROM outputs during a given phase and then are clocked into the ALU & GR Control Register as the phase changes. In other words, the ROM produces the control code during one phase, but this code is not used by the ALU until the following phase. This table can therefore be used as a ROM truth table if the Phase A and Phase B headings are reversed.

The Address Decoder uses a 4 x 2-bit Multiplexer that is enabled for all instructions other than Load Zero. (Load Zero always uses General Register 0, so all address lines are forced to the zero-state.) Its inputs are the four bits representing the A-field and B-field of the instruction. Selection is controlled by the +PHASE B signal so that the A-field bits are actually selected during Phase B, and vice-versa. This allows the Multiplexer output to be set into to the ALU & GR Control Register by the -CLK occurring at the end of each phase. Thus A-field data is in the ALU & GR Control Register during Phase A and B-field data is in it during Phase B.

The +ADDR 1, +ADDR 2, and +ADDR 4 outputs of the ALU & GR Control Register are used for addressing both the General Registers and other input and output registers and logical elements. +ADDR 1A and +ADDR 2A are duplicates of +ADDR 1 and +ADDR 2, and are used exclusively on the I/O Board. The +ADDR 8 output is used only for selecting General Registers 8-15, and is developed by the +A FIELD and +B FIELD signals, which are controlled by special Control Functions 12_{16} through 15_{16}.

There are three other addressing outputs of the ALU & GR Control Register:

-GEN REG ENA goes low during Phase A if Program Bit 7 is 0, unless a Load Zero instruction is being performed. This provides General Register input to the ALU whenever the A-field is 0 through 7, except during Load Zero. -GEN REG ENA also goes low, during Phase B of every instruction, providing input to or output from the General Registers. This is what forces the B Operand of many instructions to be a General Register, even if the B-field contains 8-15, as explained in paragraph 3.5.5.

+INPUT SEL goes high during Phase A if either Program Bit 7 is a 1 or if Load Zero is being performed: this gates the Multiplexer output, instead of the General Register's output, onto the B Bus. +INPUT SEL is always low during Phase B, because the Multiplexer output is never needed during Phase B.

+OUTPUT SEL goes high when Program Bit 3 is a 1 and Load Zero is NOT being performed. This enables selection of the various output registers, and blocks writing into the General Registers, all during Phase B.

TABLE 3-2
TRUTH TABLE
OP CODE DECODER ROM
VERSION DMP3

INSTRUCTION	PROGRAM BITS				ALU & GR CONTROL REGISTER OUTPUTS								USED DURING
					ALU CONTROL CODES					SPECIAL OUTPUTS			
	11	10	9	8	MODE	ALU SEL3	ALU SEL2	ALU SEL1	ALU SEL0	BRANCH IF	SPC INSTR	DON'T SAVE	
COMPARE	0	0	0	0	1	0	1	0	1	0	0	0	
ADD	0	0	0	1	1	0	1	0	1	0	0	0	
SUBTRACT	0	0	1	0	1	0	1	0	1	0	0	0	P
AND	0	0	1	1	1	0	1	0	1	0	0	0	H
OR	0	1	0	0	1	0	1	0	1	0	0	0	A
DECREMENT	0	1	0	1	1	0	1	0	1	0	0	0	S
INCREMENT	0	1	1	0	1	0	1	0	1	0	0	0	E
MOVE	0	1	1	1	1	0	1	0	1	0	0	0	
COMPLEMENT	1	0	0	0	1	0	1	0	1	0	0	0	A
EXCLUSIVE-OR	1	0	0	1	1	0	1	0	1	0	0	0	
BRANCH	1	0	1	0	1	0	1	0	1	1	0	0	
SPEC. FUNC.	1	0	1	1	1	0	1	0	1	0	1	1	
LOAD ZERO	1	1	x	x	1	0	1	0	1	0	0	0	
COMPARE	0	0	0	0	0	1	0	0	1	0	0	1	
ADD	0	0	0	1	0	0	1	1	0	0	0	0	
SUBTRACT	0	0	1	0	0	1	0	0	1	0	0	0	P
AND	0	0	1	1	1	1	1	0	1	0	0	0	H
OR	0	1	0	0	1	0	1	1	1	0	0	0	A
DECREMENT	0	1	0	1	0	0	0	0	0	0	0	0	S
INCREMENT	0	1	1	0	0	1	1	1	1	0	0	0	E
MOVE	0	1	1	1	1	1	1	1	1	0	0	0	
COMPLEMENT	1	0	0	0	1	0	0	0	0	0	0	0	B
EXCLUSIVE-OR	1	0	0	1	1	0	1	1	0	0	0	0	
BRANCH	1	0	1	0	1	1	1	1	1	0	0	1	
SPEC. FUNC.	1	0	1	1	1	1	1	1	1	0	1	1	
LOAD ZERO	1	1	x	x	1	1	1	1	1	0	0	0	
					7	6	5	4	3	2	1	0	
					ROM OUTPUT BITS								

3.7.1.4 Arithmetic-Logic Section (Figure 3-11, PROC-SH4)

The 16 General Registers are contained in three 16 x 4-bit Random Access Memory (RAM) chips. Each chip contains four bits of each General Register. The RAM at location B33 contains bits 11, 10, 9 and 8; the RAM at location B47 contains bits 7, 6, 5 and 4 and the RAM at locations B61 contains bits 3, 2, 1 and 0.

The RAMs are Tri-State devices: their +B Bus outputs represent a high impedance state which can neither sink nor source current when the -GEN REG ENA signal is high. When this select signal goes low, the outputs are driven to the level dictated by the data stored in the register selected by the ADDR lines. The ADDR lines and the -GEN REG ENA signal come from the Address Decoder portion of the Instruction Translator.

New data is written by first selecting the desired General Register through development of the ADDR lines, and then driving both -GEN REG ENA and -WRITE GEN REGS low. The data on the -A Bus will be written into the selected General Register. When this data is then read back out (-GEN REG ENA low and -WRITE GEN REGS high) its complement appears at the output. This data inversion within the RAM chips is compensated for by inputting the complementary data from the -A Bus, resulting in true data appearing on the +B Bus. Data can also be placed on the +B Bus by either of the multiplexers, one located on the Processor Board and the other on the I/O Board.

The ALU is comprised of three 4-bit ALU chips, each chip handling one-third of the 12-bit data word. Each chip has four data inputs from the -A Bus, and four data inputs from the +B Bus. The ALU commands, or functions, are controlled by five signals, +ALU MODE and +ALU SELECT 0, 1, 2 and 3 from the Op Code Decoder. The control signals are wired to all three chips in parallel. +CARRY is an input to the least significant bit chip. This chip's "carry" output is connected to the next chip's "carry" input, and so on, making possible 12-bit arithmetic operations.

The data outputs of the ALU make up the -C Bus, and +ALU ZERO is developed when all ALU outputs go "high", which is equal to numeric zero on the -C Bus. +ALU ZERO is used to control the Zero flip-flop for Branch conditions.

NOTE

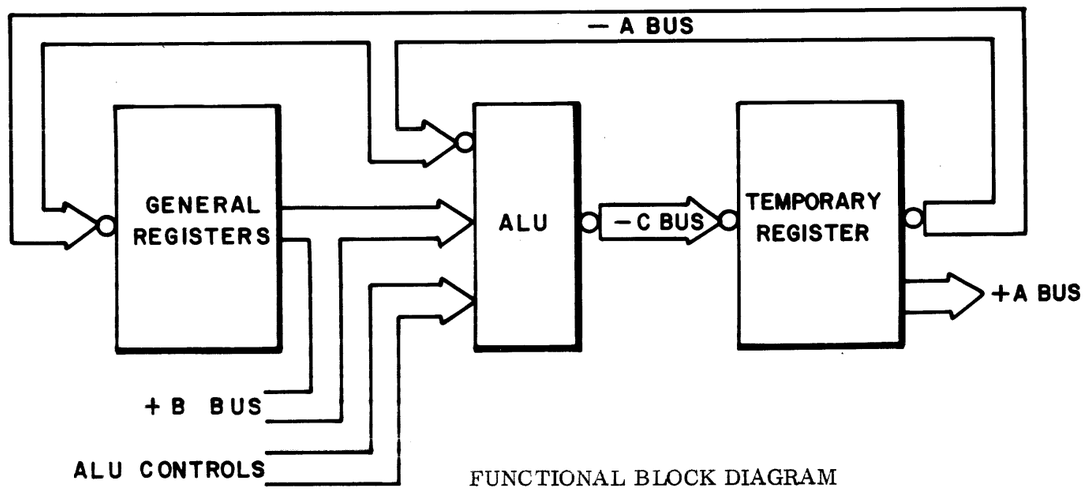
The ALU control codes are summarized in Table 3-3. Some of these control codes are different from those listed in the chip manufacturer's data sheets for corresponding functions because in this case there is a mixture of active-high and active-low data. Because of this, care should be exercised when attempting to compare these control codes with the manufacturer's specifications.

The Temporary Register is comprised of three Quad-D latches having synchronous clock and clear inputs. At every +CLK time, the code on the -C Bus is set into the Temporary Register. Since the -C Bus contains complementary data, the Q outputs of the Temporary Register make up the -A Bus, and the $\overline{Q}$ outputs make up the +A Bus. The -A Bus feeds only the ALU and General Registers. The +A Bus feeds all other output registers and decoders in the tester.

TABLE 3-3
COMPARISON OF ALU CONTROL CODES AND ALU FUNCTIONS

PHASE	OPERATION	ALU MODE	ALU SEL3	ALU SEL2	ALU SEL1	ALU SEL0	CRY IN	ALU FUNCTION (F =) HIGH-ACTIVE INPUTS	ALU FUNCTION (F =) LOW-ACTIVE A-INPUT**
A	ALL	1	0	1	0	1	x*	$\overline{B}$	$\overline{B}$
B	COMPARE	0	1	0	0	1	1	A plus B	$\overline{A}$ plus B = $\overline{A \text{ minus } B}$
	ADD	0	0	1	1	0	0	A minus B	$\overline{A}$ minus B = $\overline{A \text{ plus } B}$
	SUBTRACT	0	1	0	0	1	1	A plus B	$\overline{A}$ plus B = $\overline{A \text{ minus } B}$
	AND	1	1	1	0	1	x	A + B	$\overline{A} + \overline{B} = \overline{AB}$
	OR	1	0	1	1	1	x	$A\overline{B}$	$\overline{A} \cdot \overline{B} = \overline{A + B}$
	DECREMENT	0	0	0	0	0	0	A plus 1	$\overline{A}$ plus 1 = $\overline{A \text{ minus } 1}$
	INCREMENT	0	1	1	1	1	1	A minus 1	$\overline{A}$ minus 1 = $\overline{A \text{ plus } 1}$
	MOVE	1	1	1	1	1	x	$\overline{A}$	$\overline{A} = \overline{A}$
	COMPLEMENT	1	0	0	0	0	x	A	$\overline{A} = \overline{A}$
	EXCLUSIVE OR	1	0	1	1	0	x	$A \oplus B$	$\overline{A} + \overline{B} = \overline{A \oplus B}$
	BRANCH	1	1	1	1	1	1	A	$\overline{A} = \overline{A}$
	SPEC. FUNC.	1	1	1	1	1	1	A	$\overline{A} = \overline{A}$
	LOAD ZERO	1	1	1	1	1	1	A	$\overline{A} = \overline{A}$

*x = Irrelevant
**Low-active A-input causes high-active function to be reinterpreted so as to obtain the desired answer in complement form.



FUNCTIONAL BLOCK DIAGRAM
ALU & GENERAL REGISTERS
FIGURE 3-11

Table 3-4 summarizes the type of data contained on each bus during Phase A and Phase B. Since the Temporary Register is reloaded each +CLK time, the A Bus and -C Bus contents also change. Therefore, table 3-4 is valid only for that portion of each phase that occurs before +CLK. Note also that this table is not necessarily valid for Branch, Special Control, or Load instructions.

TABLE 3-4

BUS CONTENTS

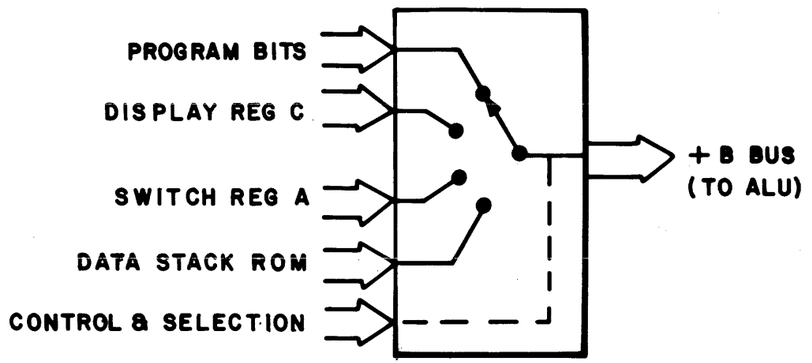
	(BEFORE "CLOCK" TIME)	
	PHASE A	PHASE B
-A Bus	-Result of previous instruction	-A Operand
+A Bus	+Result of previous instruction	+A Operand
+B Bus	+A Operand	+B Operand
-C Bus	-A Operand	-Result of Instruction

3.7.1.5 Multiplexer (Figure 3-12, PROC-SH5)

The Multiplexer acts as a 12-pole 4-position switch. It takes 12 bits of data from any of four sources, as dictated by the A-field of the instruction, and switches the data onto the +B Bus for input to the ALU. It is one of two identical multiplexers, the other one being located on the I/O Board.

The Multiplexer is physically made up of six dual 4-bit multiplexer chips. Each chip handles two bits of data. The chips must be tri-state devices because they connect to the tri-state B Bus. The chip outputs remain in the high impedance state until the Strobe A and Strobe B inputs go low. Then each output assumes the level of the corresponding input that has been enabled by the Select A and Select B inputs.

This multiplexer is enabled by a combination of +INPUT SEL, which says in effect that input will NOT be from a General Register, and -ADDR 4. The other multiplexer, on the I/O Board, is enabled by +INPUT SEL and +ADDR 4. Table 3-5 shows the relationship between different A-field combinations and the respective multiplexer input used.



FUNCTIONAL BLOCK DIAGRAM
MULTIPLEXER

FIGURE 3-12

TABLE 3-5

MULTIPLEXER INPUT SELECTION

A-FIELD	ADDRESS SIGNALS AD2	AD1	AD0	INPUT SELECTED
1 0 0 0	0	0	0	PROGRAM ROM
1 0 0 1	0	0	1	DISP REG C
1 0 1 0	0	1	0	SWITCH REG A
1 0 1 1	0	1	1	DATA STACK ROM
1 1 0 0	1	0	0	OTHER MULTIPLEXER (I/O Board)
1 1 0 1	1	0	1	
1 1 1 0	1	1	0	
1 1 1 1	1	1	1	

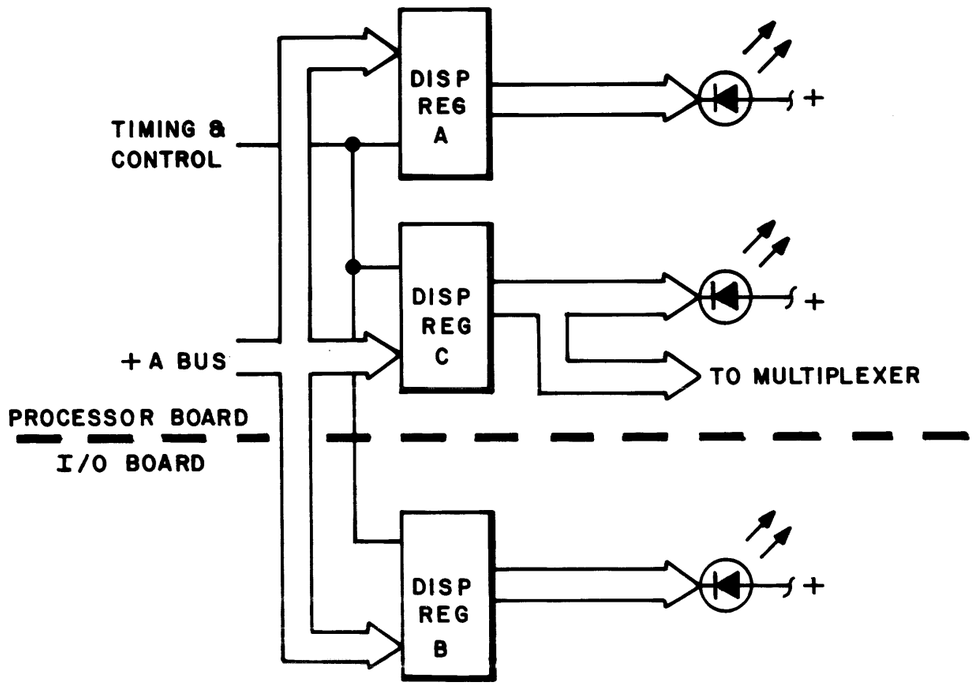
3.7.1.6 Display Registers (Figure 3-13, PROC-SH6)

Display Registers A and C are located on the Processor Board. Display Register B is on the I/O Board. All three registers are very similar in construction and operation. Each register is composed of two chips, each containing six D-type latches. Input is from the +A Bus, and output is to the display LEDs on the front panel. Display Register C also has its output routed to the multiplexer for input to the +B Bus.

Data from the +A Bus is set into the Display Register at the trailing edge of -B CLK after the appropriate LOAD DISP REG signal has been enabled. All registers are cleared by -GEN CLR.

Figure 3-13 illustrates the Display Register output circuit. Since the LEDs are connected to +5V, they turn on when the corresponding latch is reset. Thus they actually display the complement of what is stored in the Display Register.

The LED cartridge contains an internal current-limiting resistor.



FUNCTIONAL BLOCK DIAGRAM
DISPLAY REGISTERS

FIGURE 3-13

3.7.1.7 Miscellaneous Controls (Figure 3-14, PROC-SH7)

There are two major functions performed by these miscellaneous controls: Branching, and B Operand selection.

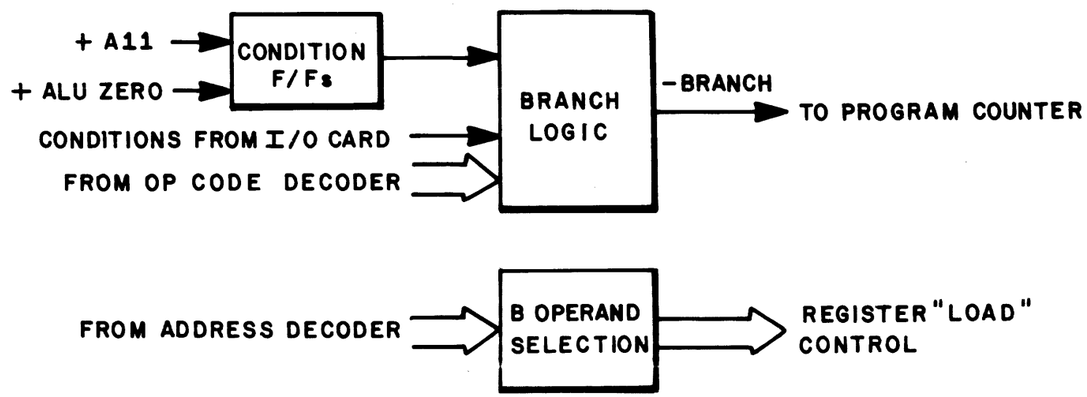
The Zero and Minus flip-flops record the conditions present upon completion of an instruction, for testing by a subsequent Branch instruction. Zero sets at +B CLK if the -C Bus contains all "highs" (ALU result = 0), and resets if at least one data bit of the result is 1. Minus sets at the end of -B CLK if the MSB of the result is a 1, and resets if it is a 0.

These conditions are applied to the Branch Logic multiplexer along with other Branch condition signals from the I/O Logic board. When a Branch instruction is performed, the -BRANCH IF signal enables the decoder, and PROGRAM BITS 2, 1, and 0 (representing the instruction B-field) select which of the inputs will be seen at the output. If the selected input is high, -BRANCH will go low and allow the branch to take place. If the selected input is low, -BRANCH remains high and no branching occurs.

The choice of whether the B Operand will be a general register or some other destination is determined by the state of +OUTPUT SEL, from the Instruction Translator.

If +OUTPUT SEL is low and if the instruction DOES save results, then -WRITE GENERAL REGS will go low at B-Clock time.

If +OUTPUT SEL is high, some other register will receive the result of the instruction. A binary-to-decimal (1-of 10) decoder is used to select the destination of the answer. The binary "8" input to this decoder is used as an "enable", effectively making it a 1-of-8 decoder. When the enable goes low, one of the eight decoder outputs will go low, determined by the states of +ADDR 4, 2, and 1. The decoder outputs are routed to the various registers to enable loading them at the end of Phase B.



FUNCTIONAL BLOCK DIAGRAM
MISCELLANEOUS CONTROLS
FIGURE 3-14

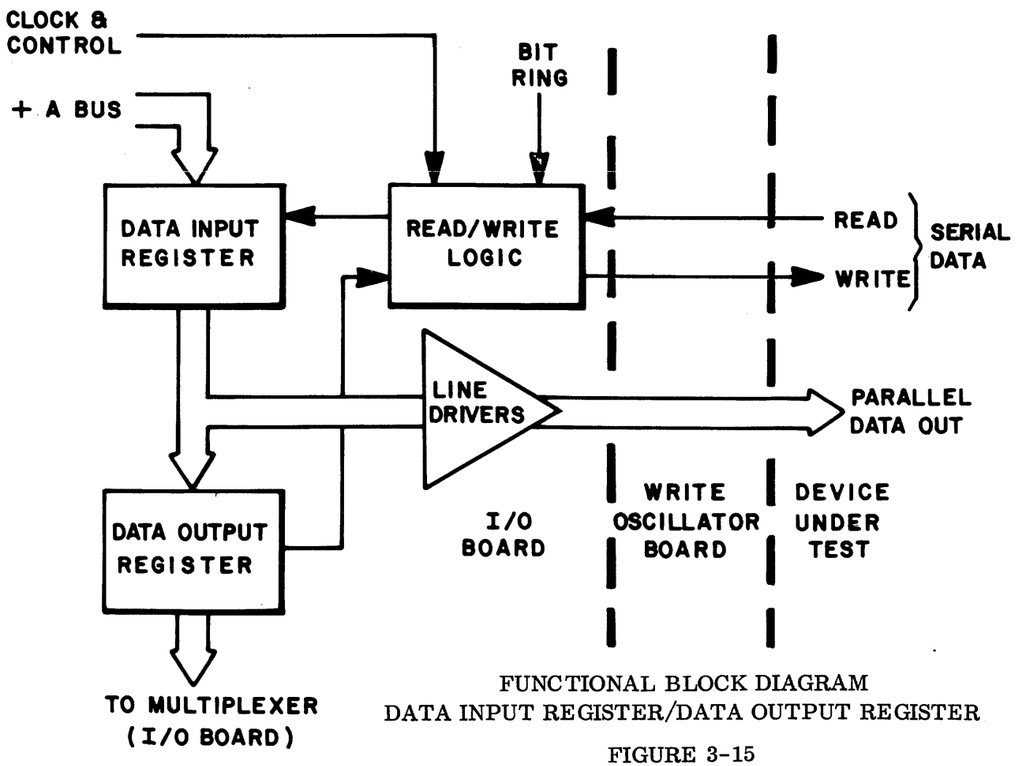
3.7.2 I/O Board

The major elements of the I/O Board are the Bit Ring, the Data Input Register and Data Output Register, the Read/Write Logic, the Line Receivers and Flag Storage, the Multiplexer, the Special Function Decoder, and Display Register B. An appropriate place to begin the discussion of the I/O Board is with the Data Input and Data Output Registers on Sheet 2 of the logic diagrams.

3.7.2.1 Data Input Register/Data Output Register (Figure 3-15, I/O-SH2)

These two registers control all microprocessor output data and most input data. Output data from the +A Bus is parallel loaded into the Data Input Register. From here it is available, in parallel form, to the output drivers, or it can be parallel loaded into the Data Output Register and then shifted out serially through the Read/Write Logic, to the device under test.

Serial input data from the Read/Write Logic is shifted into the Data Input Register and then transferred in parallel to the Data Output Register. From here it can be introduced to the +B Bus via the I/O Multiplexer. Parallel input data is received through the Parallel Data In lines, discussed in paragraph 3.7.2.4.



FUNCTIONAL BLOCK DIAGRAM
DATA INPUT REGISTER/DATA OUTPUT REGISTER

FIGURE 3-15

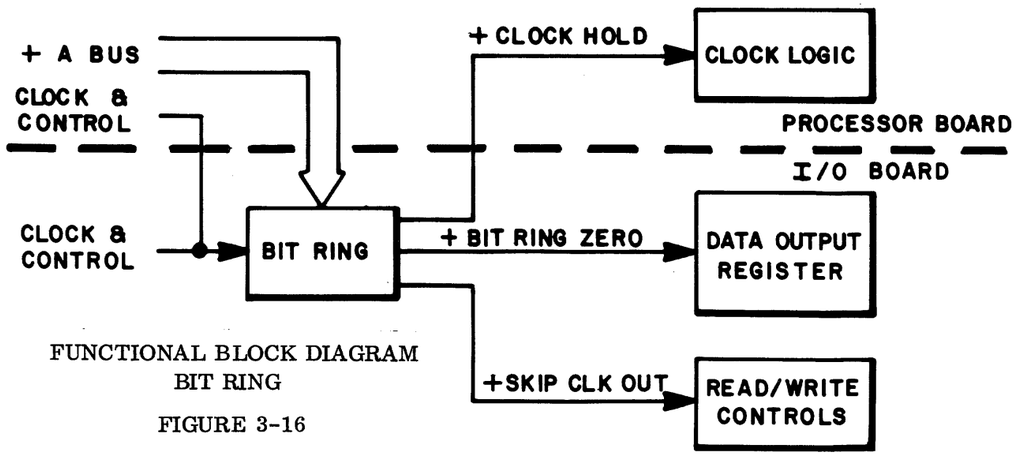
Each register is composed of three 4-bit shift register chips having parallel-load capability. The Data Input Register is in serial shift mode only when "Read" is turned on, at which time +SERIAL CLK IN O/S Controls shifting and data input is via +BIT DETECTED from the Read/Write Logic. In parallel mode, -LOAD DATA INPUT REG and -B CLK control loading.

With "Read" on, the Data Output Register can be loaded in parallel at the coincidence of +SERIAL CLK IN O/S and +BIT RING ZERO. During "Write", shifting of the Data Output Register is controlled by -WRITE CLK PHASE from the Read/Write Logic, and data output to the Read/Write Logic is via +DATA OUTPUT REG 11.

3.7.2.2 Bit Ring (Figures 3-16, 3-17, I/O-SH1)

The purpose of the Bit Ring is to synchronize incoming and outgoing serial data to the microprocessor instruction sequence. For example, during disk read, the incoming serial data cannot be examined until all bits of each word are fully shifted into the Data Input Register and transferred to the Data Output Register. Synchronization is accomplished by loading a single 1-bit into the Bit Ring and then clocking the Bit Ring at the same rate as the incoming data (using +SERIAL IN CLK). The single bit will pass through the Bit Ring 0 position once for each data word received. After processing each data word, the microprocessor executes a "Wait for Bit Ring" instruction (Special Function 30_{16}). This stops the processor clock, inhibiting instruction execution, until the single bit in the Bit Ring again passes through position 0, signalling that the next data word is available. (Since microprocessor speed is quite high in relation to disk read/write speed, several instructions can be executed while the next data word is being shifted into the Data Input Register.)

The Bit Ring cannot be loaded while either Read Control, Write Serial, or Bit Ring Auto Shift (Special Functions 03, 05, and 0B, respectively) are active. The complementary Special Function (02, 04, or 0A) must be executed before the Bit Ring can be loaded.



FUNCTIONAL BLOCK DIAGRAM
BIT RING

FIGURE 3-16

When writing, each new data word is automatically strobed from the Data Input Register to the Data Output Register as soon as the preceding word is fully shifted out. In this case, the Bit Ring is needed to delay the microprocessor so it cannot place the next word to be written into the Data Input Register before the preceding word has been transferred to the Data Output Register. During Writing, the Bit Ring is clocked by +WRITE SHIFT, at the same rate as the Data Output Register. After WRITE is turned off, the contents of the Bit Ring cannot be accurately predicted, and it must be reloaded before it can be used again.

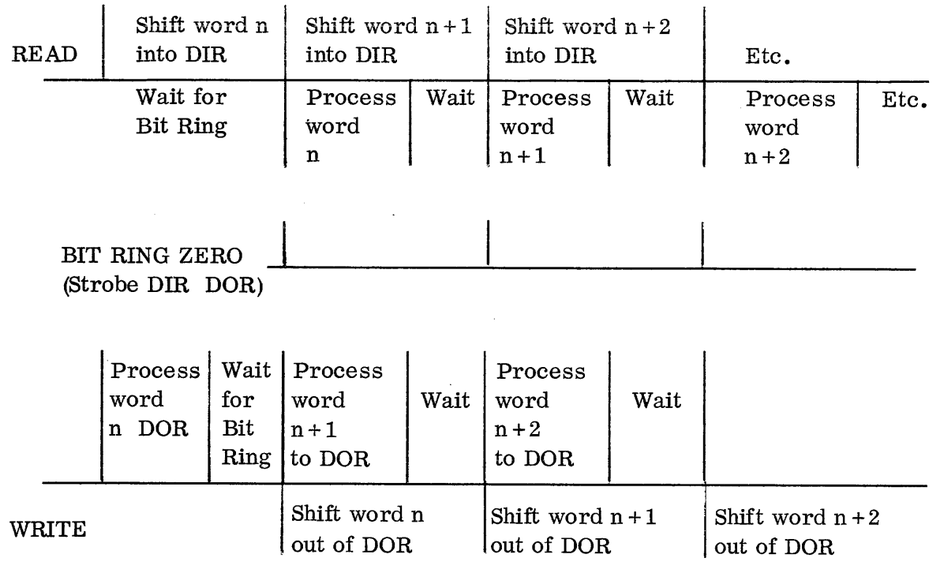
When the Read mode is entered, the Bit Ring does not begin shifting immediately. Instead, it waits for +READ SYNC DETECT to synchronize it to the incoming data.

The Bit Ring can be converted from a 12-bit ring to an 8-bit ring by executing Special Function 23_{16} which develops +BYTE MODE. Special Function 22_{16} switches it back to 12-bit operation.

The +CLK HOLD signal is developed after executing the Wait for Bit Ring instruction, and is reset by the single 1-bit passing through position 0. +CLK HOLD goes to the Clock Logic to stop the main microprocessor clock.

+BIT RING ZERO goes to the Data Output Register to enable the parallel loading of data into it from the Data Input Register.

+SKIP CLK OUT is developed for two successive bit cell periods and is used only when writing "address marks", during the formatting of disks in certain configurations. This signal goes to the Write Logic, but has no effect until after Special Function 27_{16} has been executed. Address marks are discussed further in the Read/Write Logic, following.

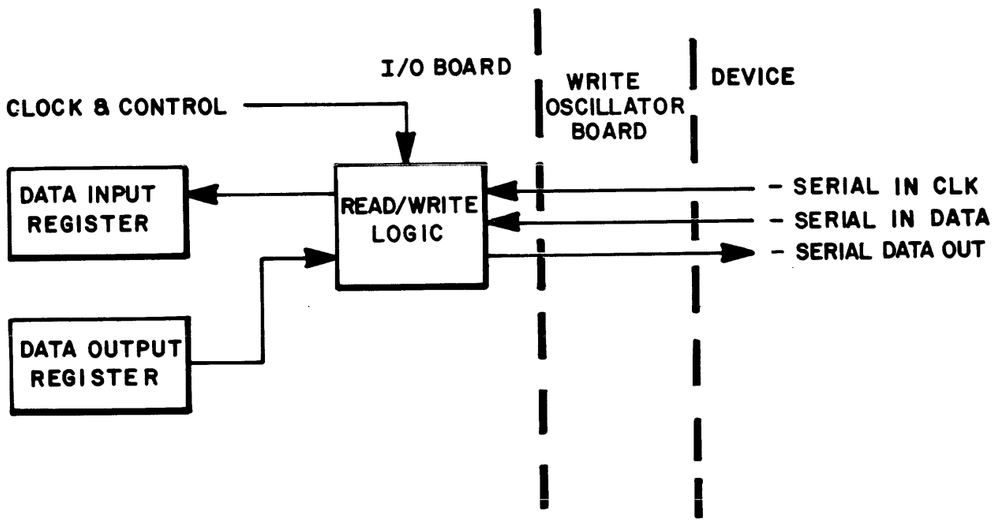


BIT RING FUNCTION

FIGURE 3-17

3.7.2.3 Read/Write Logic (Figure 3-18, I/O-SH3)

Write Logic: The major function of the Write Logic is to mix clocks and data pulses together to develop the double-frequency -SERIAL DATA OUT signal which is sent to a disk drive under test. Clock input is from the Disk Oscillator on the Write Oscillator Board. Data input is from the MSB of the Data Output Register. Whenever +WRITE is developed (Special Control Function 5) the Write Sync flip-flop sets in sync with the Disk Oscillator and writing begins. -WRITE CLOCK PHASE is developed to shift the data out of the Data Output Register, and -WRITE SHIFT is developed between -WRITE CLOCK PHASEs to shift the Bit Ring.



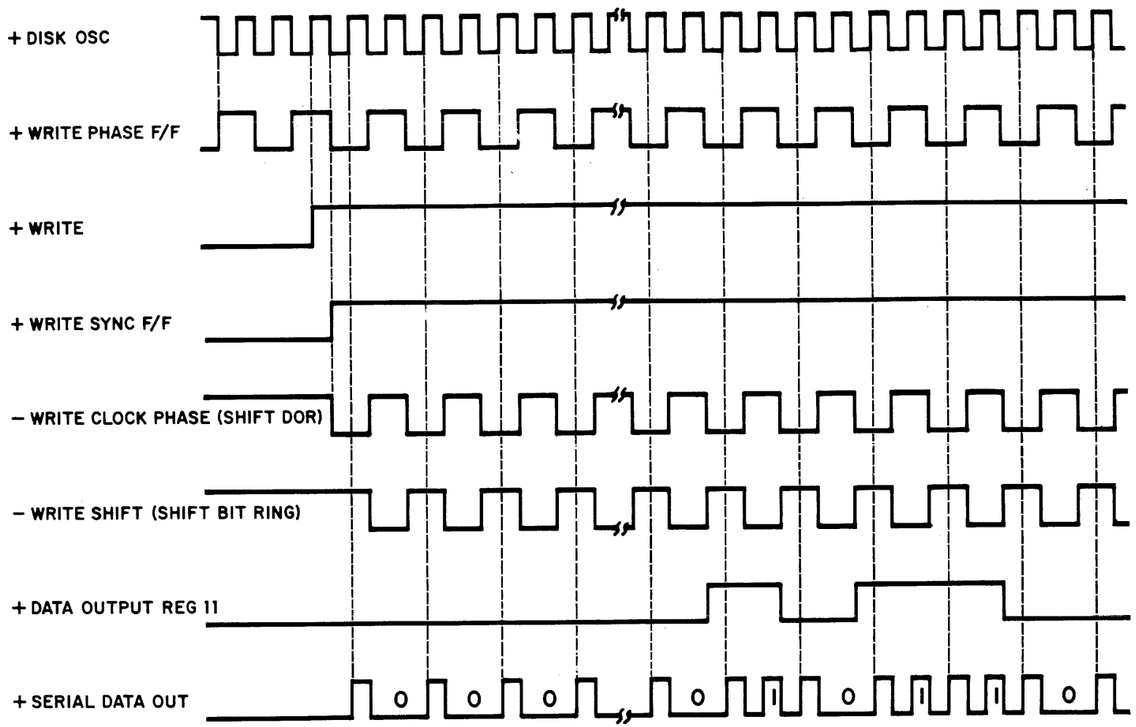
FUNCTIONAL BLOCK DIAGRAM
READ/WRITE LOGIC

FIGURE 3-18

Either -WRITE CLOCK PHASE or -WRITE SHIFT may be developed first as +WRITE is initiated, depending upon the state of the Write Phase flip-flop. No elaborate measures have been taken to initially synchronize the Data Output Registers and the Bit Ring to the Write Logic because all data records written begin with a repetitive pattern of all "0"s. Thereafter, synchronization is easily accomplished after several words of zeros have been written. Figure 3-19 illustrates typical timing relationships.

+ENA SKIP CLK OUT from the Special Function Decoder and +SKIP CLK OUT from the Bit Ring are used to prevent the writing of certain clock bits when writing address marks in System 3 format. This function is enabled by executing Special Control Function 27_{16}, and is gated by having the "1" in the proper location of the Bit Ring at the proper time.

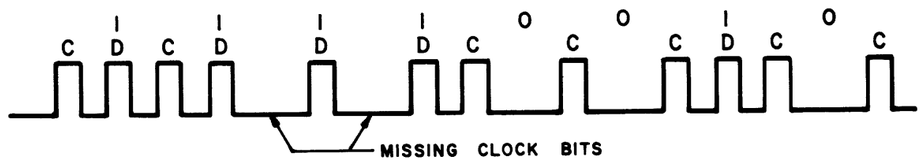
Figure 3-20 illustrates the address mark format. For a more detailed description of this format, refer to the Diablo Systems Series 40 Disk Drives Product Description manual, Chapter 3.



BASIC TIMING CHART
WRITE LOGIC

FIGURE 3-19

Hex F2

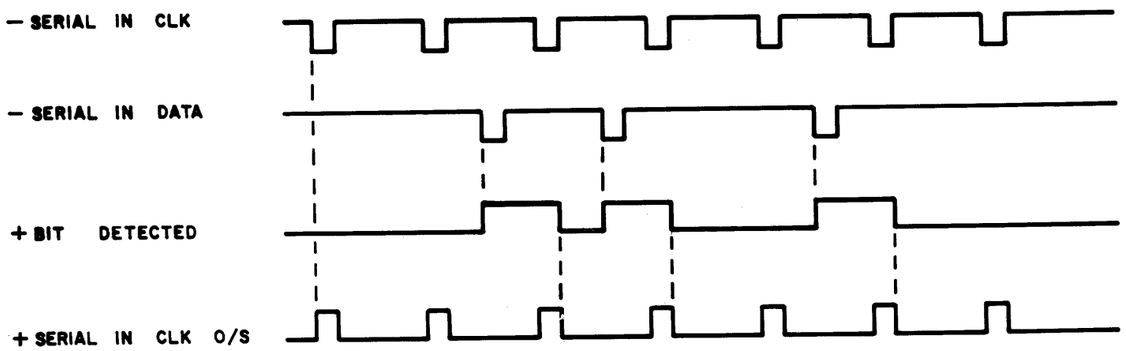


ADDRESS MARK FORMAT

FIGURE 3-20

Read Logic: The Read Logic performs three separate functions. The Serial in Clk O/S and Bit Detected flip-flop interface the incoming signal to the microprocessor; the Read Sync Detected flip-flop synchronizes the incoming data to the Bit Ring; and the Missing Clock O/S and flip-flops recognize incoming System 3 address marks.

The timing chart in Figure 3-21 illustrates the action of the Bit Detected flip-flop in stretching incoming data pulses to a length usable by the microprocessor. Incoming pulse widths shown in the figure are generally representative of Diablo Series 40 Disk Drives. The Serial In Clk O/S provides constant pulse widths (100 ns) regardless of the width of the incoming clock signal. This one-shot is really needed only when the VFI board is used with the VFO option on the series 40 disk drive--otherwise it is redundant.

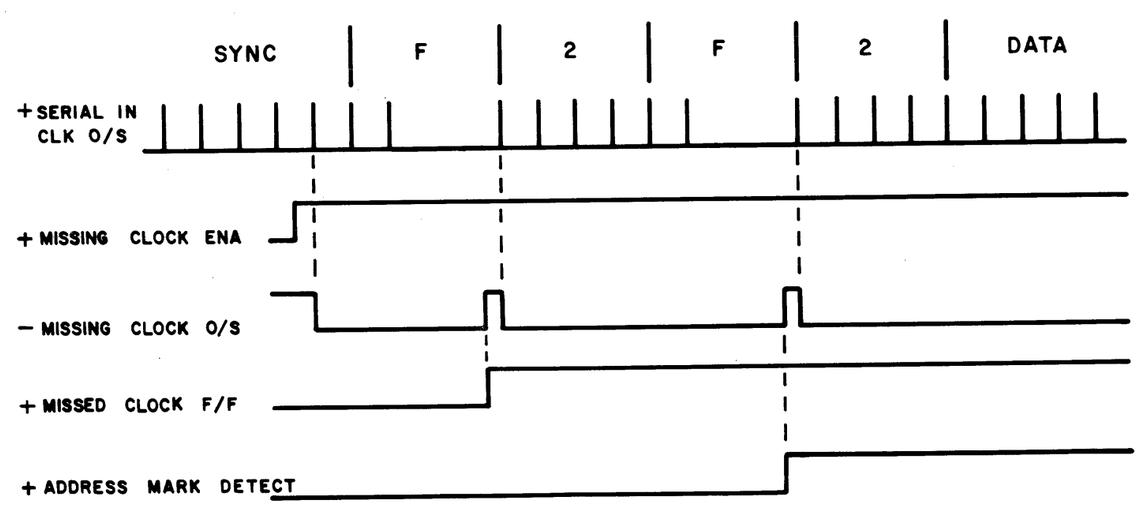


BASIC TIMING CHART
READ LOGIC

FIGURE 3-21

The initial reading of a data record usually involves sensing a series of "0"s (preamble) and a single "1" sync bit. The Read Sync Detected flip-flop sets when this "1" arrives in the "4" position of the Data Input Register, and the +READ SYNC DETECTED signal is then used to enable shifting the Bit Ring, thus synchronizing the Bit Ring to the incoming data.

The action of the Missing Clock O/S and flip-flops is illustrated in the timing chart in Figure 3-22. +MISSING CLK ENA (from the Special Function Decoder) has no effect as long as +SERIAL IN CLKs continue to appear, triggering the Serial In Clk O/S, which retriggers the Missing Clock O/S. However, when two successive clocks fail to appear, the Missing Clk O/S times out and sets the Missed Clk flip-flop. Clocks again reappear to trigger and retrigger the Missing Clk O/S, but when the second pair of clocks is missed, the O/S again times out and sets the Address Mark Detect flip-flop. +ADDRESS MARK DETECT then remains high until +MISSING CLK ENA is removed by the execution of Special Function 24_{16}.



TIMING CHART
MISSING CLOCK DETECTION

FIGURE 3-22

3.7.2.4 Line Receivers & Flag Storage (Figure 3-23, I/O-SH4)

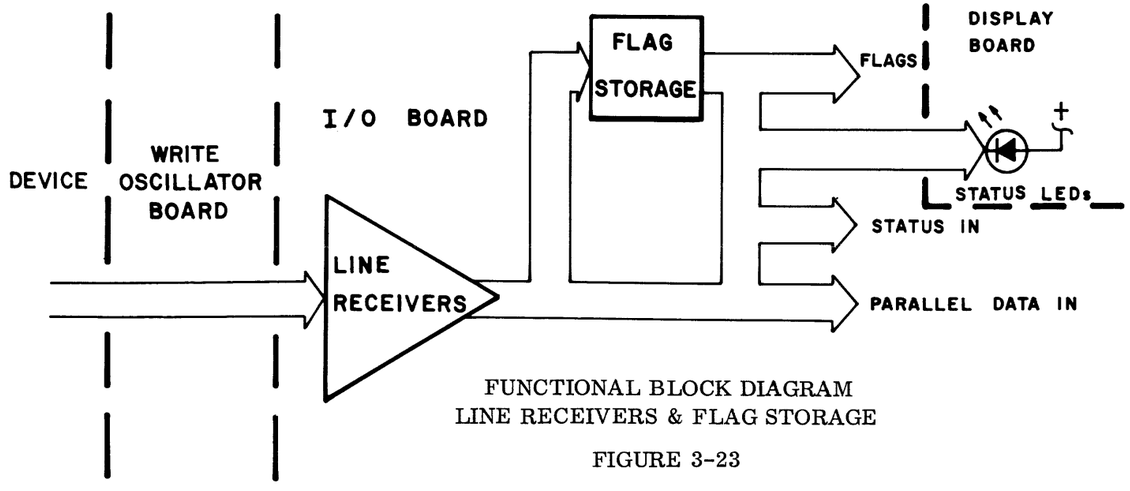
All input signals other than serial data and clock inputs are shown on this drawing. All input is via the front panel connector (P8), through the Write Oscillator board and cables P4 and P5, to the line receivers on the I/O board. Incoming signals are low-active, so all lines are terminated with 150Ω resistors to +3.5V. Since there is some signal loss in the cable and connections, the hexinverter receivers are used to restore waveforms to their original values.

Flag storage makes possible the storage of momentary status signals so they can be inspected by the microprogram as required: it eliminates the necessity of requiring the microprogram to run in full synchronism with the external momentary signals, but at the same time provides a degree of synchronism. For example, when strobing a Restore command to a connected disk drive, the RESTORE (-OUT CONTROL 2) and STROBE (-OUT CONTROL 1) signals should not be removed until ADDRESS ACKNOWLEDGE (-FLAG 9) is received from the drive. The microprogram sends OUT CONTROL 2 (RESTORE) and OUT CONTROL 1 (STROBE) and then goes into a loop testing for -FLAG 9 (ADDRESS ACKNOWLEDGE). Since this reply is momentary (as short as 2.5 μs) it may not appear at the precise moment that it is being tested, so the fact that it had occurred is stored, and the storage is tested when the microprogram "gets around to it". The other stored flags are used in similar instances.

Input lines carry different information, depending upon the device being tested. For example, the PARALLEL DATA IN lines can be used for status or other information when the tester is used with a device that does not provide parallel input data.

Some of the input and flag storage lines are connected directly to the P1 connector, which takes them to the Display board where they illuminate the status LEDs on the front panel.

The +3.5 volt power source pictured here also goes to the Read/Write logic for the serial data and clock inputs.

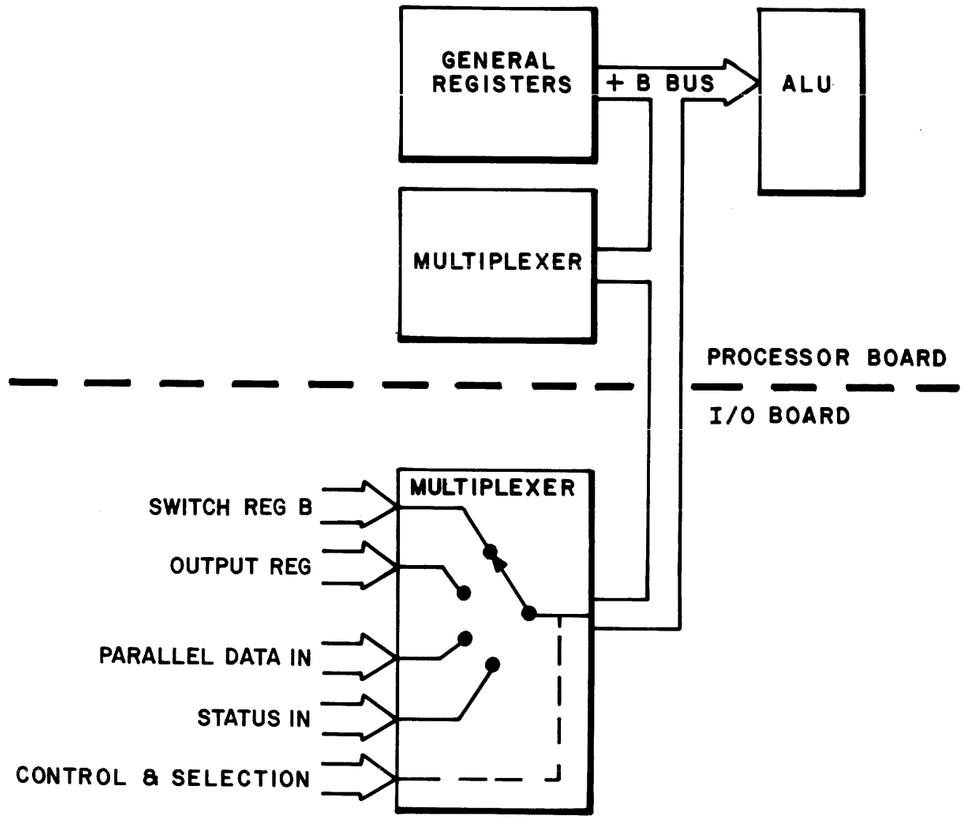


FUNCTIONAL BLOCK DIAGRAM
LINE RECEIVERS & FLAG STORAGE

FIGURE 3-23

3.7.2.5 I/O Multiplexer (Figure 3-24, I/O-SH5)

The I/O Multiplexer is identical to the multiplexer on the Processor board: it acts as a 12-pole 4-position switch, transferring 12 bits of data from any of four sources, as dictated by the A-field of the instruction, onto the +B Bus. It is comprised of six dual 4-bit tri-state multiplexer chips, each chip handling 2 bits of data from each of the four sources. All chip outputs remain in the high-impedance state until the Strobe A and Strobe B inputs go low. Then the outputs assume the levels of the two data inputs that have been enabled by the Select A and Select B inputs.



FUNCTIONAL BLOCK DIAGRAM
I/O MULTIPLEXER

FIGURE 3-24

This multiplexer is enabled by the combination of +INPUT SEL and +ADDR 4. Table 3-6 shows the relationship between different A-field bit combinations and the respective multiplexer inputs.

TABLE 3-6

I/O MULTIPLEXER INPUT SELECTION

A FIELD	ADDRESS SIGNALS AD2	AD1	AD0	INPUT SELECTED
1 0 0 0	0	0	0	OTHER MULTIPLEXER (PROCESSOR BOARD)
1 0 0 1	0	0	1	
1 0 1 0	0	1	0	
1 0 1 1	0	1	1	
1 1 0 0	1	0	0	SWITCH REG B
1 1 0 1	1	0	1	DATA OUTPUT REG
1 1 1 0	1	1	0	PARALLEL DATA IN
1 1 1 1	1	1	1	STATUS IN

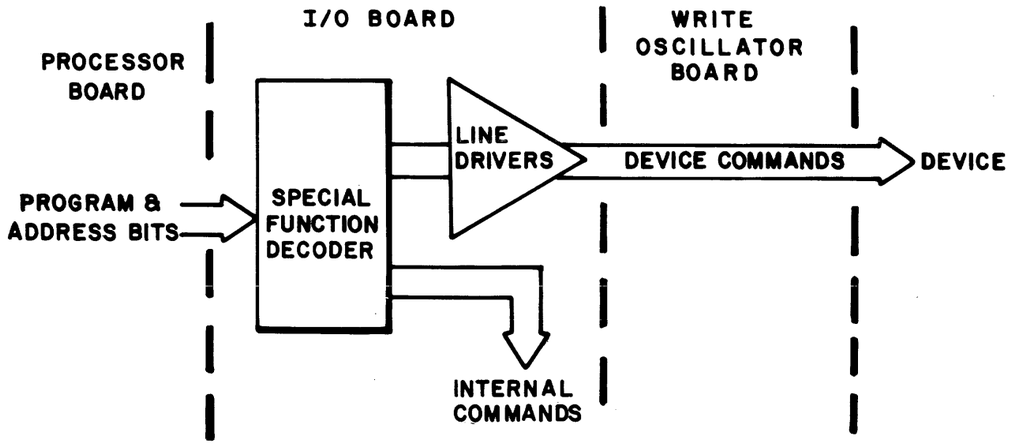
3.7.2.6 Special Function Decoder (Figure 3-25, I/O-SH6)

The Special Function Decoder breaks down Special Control Function instructions into individual lines to activate specific internal or device functions. It is composed of a dual one-of-four decoder and three 8-bit addressable latches.

One-half of the decoder is used to decode the instruction A-field (0011 is the highest A-field value used in SPC instructions) and to enable one of the addressable latch chips or the other half of the decoder. The B-field program bits are applied to the addressable latches and the second half of the decoder: the LSB is the "data" input to the latches and the other three bits address one of the eight latches in the enabled chip. This causes the selected latch to assume the state of the LSB. Once a latch is set, it remains so until it is again addressed and reset, or until -GEN CLR is developed.

The two decoder outputs remain active only as long as the inputs are applied. Since -GATED SPC INSTR is governed by A-Clock, the decoder outputs are low only for a short pulse time, approximating A-Clock time.

Further information concerning the output drivers is contained in Section 2.



FUNCTIONAL BLOCK DIAGRAM
SPECIAL FUNCTION DECODER

FIGURE 3-25

3.7.2.7 Display Register B & Output Drivers (Figure 3-26, I/O-SH7)

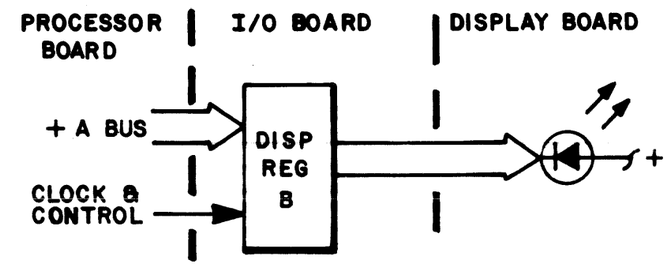
Display Register B is identical to Display Register A on the Processor board. It is composed of two hex-D latch chips, having common clock and clear.

Data from the +A Bus is set into Display Register B at the trailing edge of -B CLK after -LOAD DISP REG B has been developed by an instruction B-field of 1010. The complement of the register contents is displayed in the front panel LEDs.

The register is cleared by -GEN CLR. The LED cartridges contain current-limiting resistors.

The Parallel Data Output drivers receive data from the Data Input Register and apply it to the device adapter cable through the Write Oscillator board.

Two other signals, +SW REG A5 and +SW REG A4, pass through the I/O board simply because there are not enough connector pins in the P6 connector to run them directly from the Display board to the Processor board.



FUNCTIONAL BLOCK DIAGRAM
DISPLAY REGISTER B

FIGURE 3-26

3.7.3 Program Board

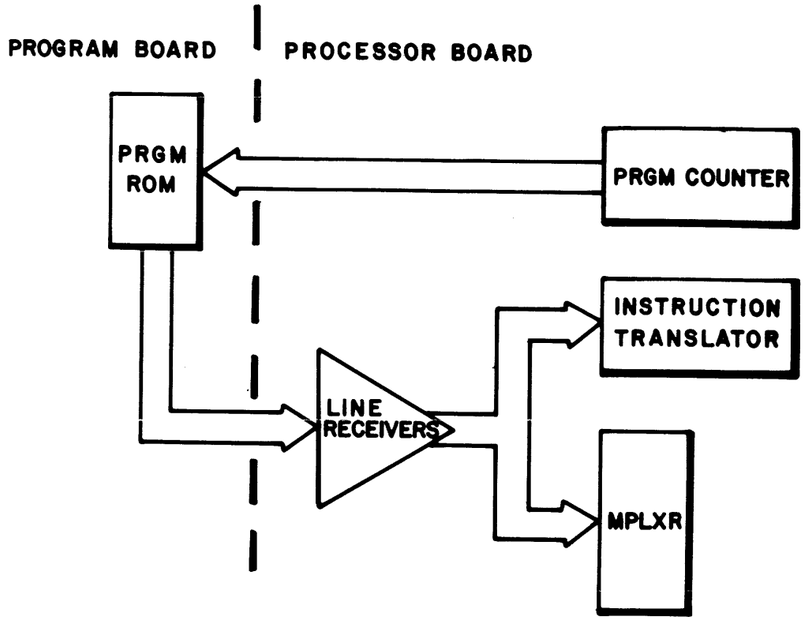
The standard Program board contains a maximum of 1024 12-bit instructions and 256 12-bit constants, all contained in ROM chips. The possibility exists that other Program boards may be released in the future, but at the time of this writing, the "standard" board is the only one available, and the following descriptions pertain to this standard board only.

3.7.3.1 Program ROM (Figure 3-27, PRGM-SH1)

The Program ROM may employ either 256 x 4-bit ROMs or 512 x 4-bit ROMs. Short programs will very likely employ the 256 x 4-bit ROM chips, and long programs will usually employ the 512 x 4-bit ROMs, "Medium-sized" programs may use either type of chip, depending upon cost and availability at the time of manufacture. Two jumper wires are soldered to the board to provide proper addressing for the type of ROMs used.

Addressing input to the ROMs is from the Program Counter on the Processor board. LEDs provide a visual indication of the Program Counter setting should the counter ever stop. Note, however, that these LEDs display the complement of the Program Counter setting.

Program ROM output is in complementary form. For example, bits 11, 10, 9 and 8 of a Branch instruction would measure LHLH, respectively. ROM output goes to the Processor board, where it is inverted to its true form and applied to the Instruction Translator, and to the multiplexer for use during Load Zero instructions.

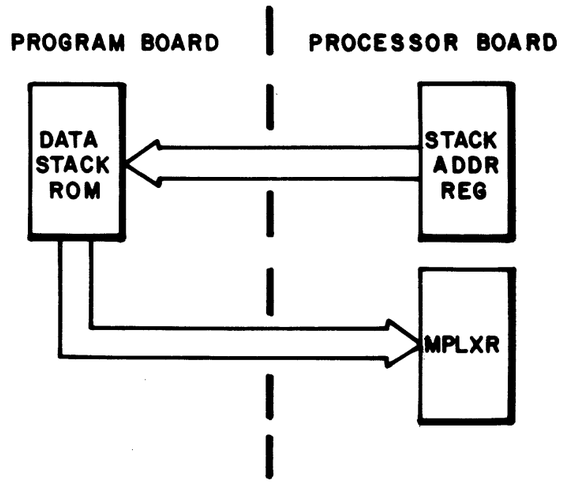


FUNCTIONAL BLOCK DIAGRAM
PROGRAM ROM

FIGURE 3-27

3.7.3.2 Data Stack ROM (Figure 3-28, PRGM-SH2)

The Data Stack ROM is comprised of three 256 x 4-bit ROM chips. Addressing input is from the Stack Address Register and output is to the multiplexer, both located on the Processor board. Maximum constant-factor data capacity is 256 12-bit words.



FUNCTIONAL BLOCK DIAGRAM
DATA STACK ROM

FIGURE 3-28

3.7.4 Write Oscillator Board (Figure 3-29, WOSC-SH1)

The Write Oscillator board performs three basic functions. First, as its name implies, it contains the oscillator that clocks the serial output circuits. Second, it contains circuitry for debouncing the General Clear and Program Reset pushbuttons. Third, it passes all interface signals between the I/O board and the device.

The Write Oscillator frequency is controlled by switching the desired crystal or external signal (from Test Point D--see note below) into the oscillator circuit via the front panel toggle switches. The Write Oscillator frequency, equal to four times the selected bit rate, is divided in two by the Half-Frequency flip-flop. Depending upon the setting of the FULL DENSITY/HALF DENSITY toggle switch, either the Full-Frequency flip-flop output or the Half-Frequency flip-flop output is gated out to become the +DISK OSC signal. This signal is twice the desired bit rate, as it must be to produce double-frequency data and clocks on alternate cycles. +DISK OSC is routed to the Write Logic on the I/O Board, where it synchronizes the data and clocks before they are sent to the disk drive under test.

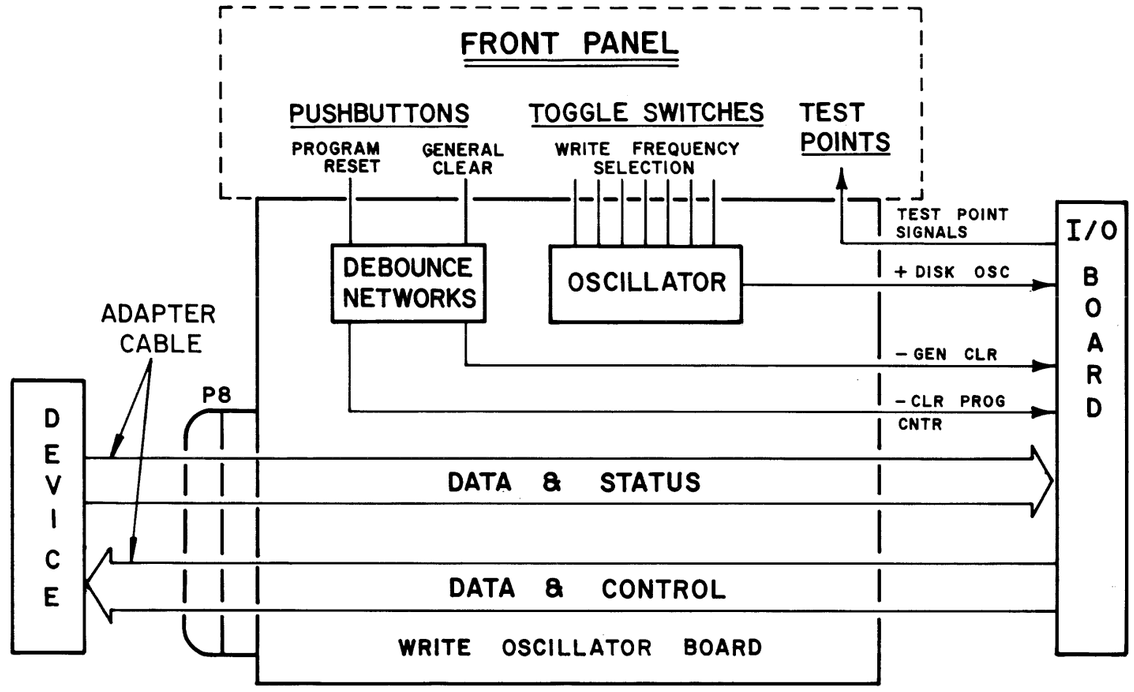
The pushbutton debouncing circuitry utilizes series resistance, relatively large capacitors, and DTL power inverters to slow down changes appearing on the pushbutton's outputs. This effectively filters out noise spikes and slivers resulting from operation of the buttons, and provides sufficient power to drive the many loads on the -GEN CLR signal.

Figure 3-29 shows that interface signals between the Programmable Tester and the device being tested pass through the Write Oscillator board and the front panel connector (P8) on their way to/from the adapter cable and the I/O board. The P8 connector is mounted directly on the Write Oscillator board, and all signals to/from P8 go directly to either the P4 or P5 connector for routing to the I/O board. The chart on sheet 1 of the Write Oscillator logic diagram lists all interface signals by name, their front panel connector pin designation, their P4 or P5 pin designation, and where they can be found entering or leaving the I/O board logic drawings.

NOTE

Externally-generated frequencies can be used to clock the Write Oscillator. The external signal is introduced via Test Point D. It is selected by turning all Write Frequency switches off. (The FULL DENSITY/HALF DENSITY switch is still functional.) The external frequency can be supplied either from a crystal or a signal generator connected across Test Points D and G. If a signal generator is used, the following output signal characteristics must be observed for proper operation:

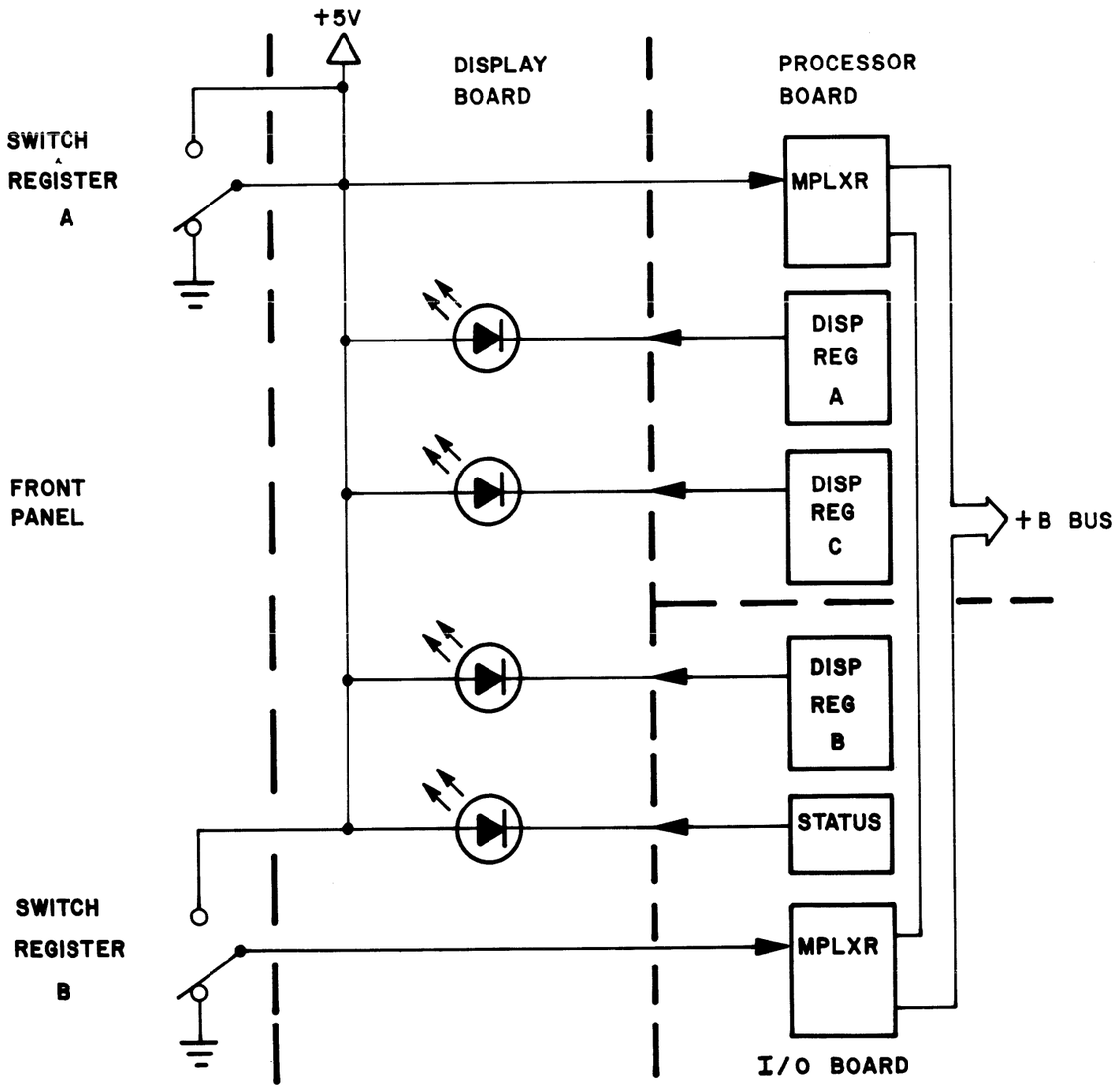
1. Wave shape--rectangular, short positive pulses.
2. Pulse width--<500ns
3. Amplitude--+4V max.
4. Frequency--to >10 MHz (4 times desired disk writing rate).



FUNCTIONAL BLOCK DIAGRAM
WRITE OSCILLATOR BOARD
FIGURE 3-29

3.7.5 Display Board (Figure 3-30)

The Display Board contains the Switch Register logic and the LEDs providing the visual display of the output of the Display Registers and some status signals.



FUNCTIONAL BLOCK DIAGRAM
DISPLAY BOARD

FIGURE 3-30

3.7.5.1 Switch Registers (DISP-SH1)

The Switch Register toggle switches are physically mounted on the front panel, in close proximity to the Display board. Short jumper wires connect each switch to the board, and most signals pass directly across the board to the P1 or P6 connector. All signals from Switch Register B pass directly through P1 to the I/O board. Most signals from Switch Register A pass directly through P6 to the Processor board. However, the two high-order switches, A11 and A10, are wired differently and are debounced on the Display board before leaving for the Processor board. This debouncing provides the ability to operate these switches while the microprogram is running, without throwing "glitches" into the sequence of program steps.

The +SW REG A5 and +SW REG A4 signals pass through the I/O board on the way to the Processor multiplexer only because there are not enough pins on the P6 plug.

3.7.5.2 Display LEDs (DISP-SH2)

The LED sockets are soldered directly to the Display board, and the LEDs are inserted from the front of the front panel and plugged into the sockets. All LEDs are returned to +5 Volts, so they are illuminated when the input to the Display board is grounded. In the case of the Display Registers, this is when the corresponding register flip-flop is reset. In the case of the Status signals, the LED lights when the corresponding status signal is ACTIVE. Each LED cartridge contains a current-limiting resistor in series with the LED + lead.

3.7.6 Power Supply

The power supply is comprised mainly of a Powertec model 2C5-6 repackaged by Diablo onto a different heatsink/bracket assembly. The model 2C5-6 is produced by the Powertec Division of Airtronics, Inc., Chatsworth, California 91311. Added to this package is Powertec's model OVP-1 overvoltage protector.

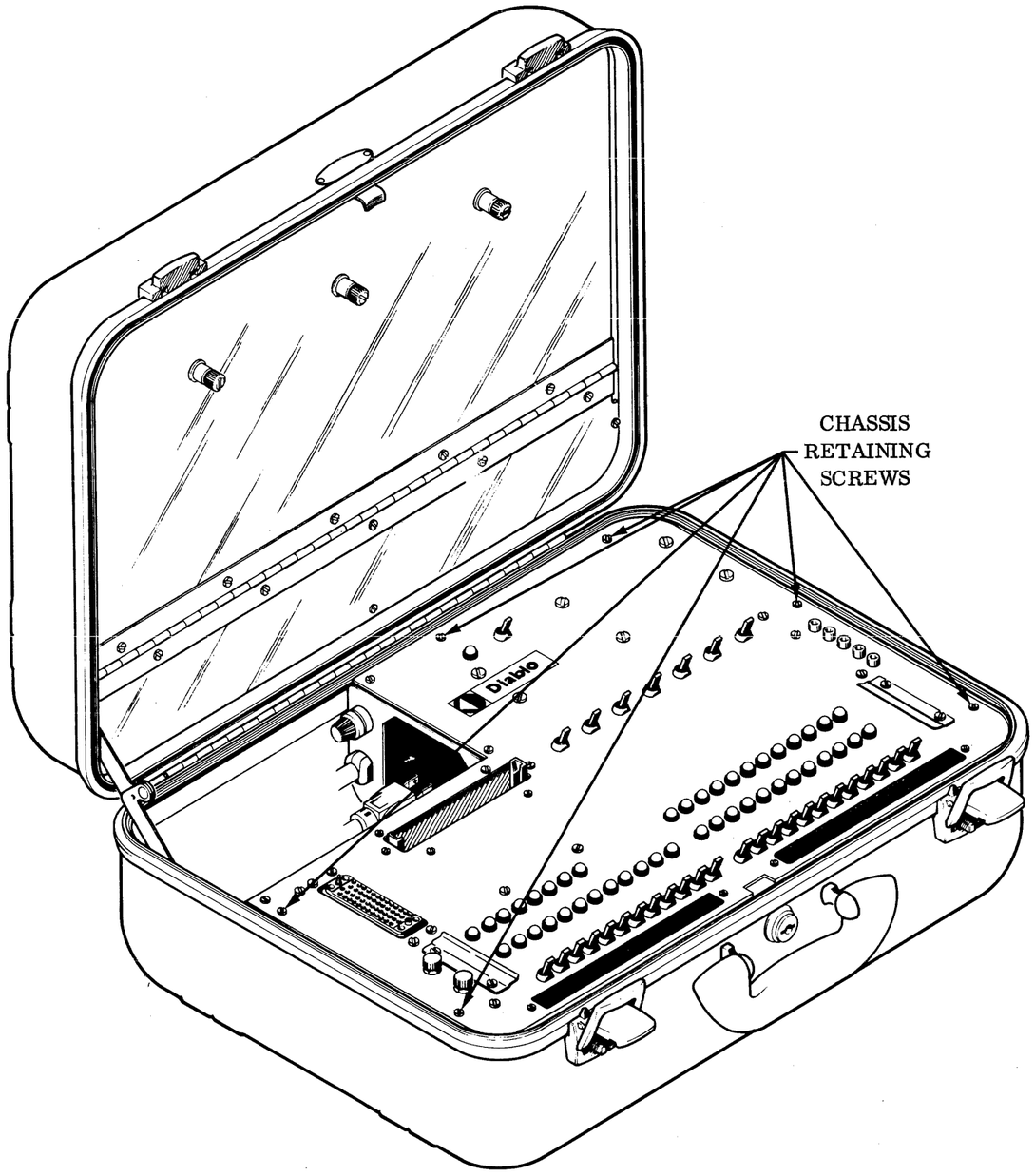
The power supply is a common series regulator with foldback current limiting. There are separate adjustment potentiometers for output voltage level and overvoltage cutoff level. Applicable specifications are as follows:

AC input:	105 to 125 Vac, 57 to 63 Hz.
DC output:	5 V at 6 amps, within expected normal operating temperatures.
Regulation:	Better than .25% within rated input and output.
Output Ripple:	1.5 millivolt RMS, 5 mV pk-pk.

Adjustment procedures, troubleshooting hints, and typical voltage readings will be found in Section 4 of this manual.

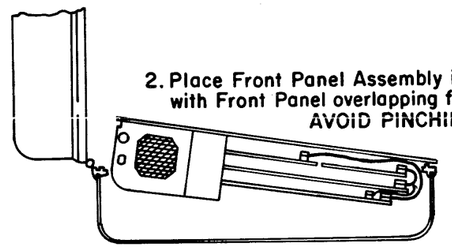
Section 4

MAINTENANCE

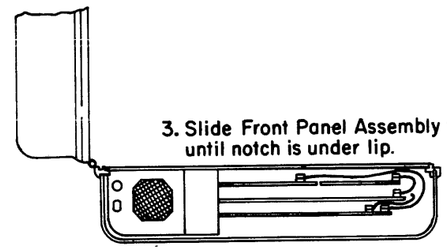


ASSEMBLY STEPS FOR INSTALLING FRONT PANEL ASSEMBLY IN SUITCASE ASSEMBLY.

1. Clean interior of suitcase thoroughly.



2. Place Front Panel Assembly in suitcase with with Front Panel overlapping front of suitcase. AVOID PINCHING CABLES.



3. Slide Front Panel Assembly to rear until notch is under lip.

4. Install the six screws, adjust Front Panel Assembly to give the latch clearance and then tighten screws.

FRONT PANEL
REMOVAL & INSTALLATION

FIGURE 4-1

Section 4

MAINTENANCE

4.1 PREVENTIVE MAINTENANCE

The Programmable Tester requires no specific periodic preventive maintenance. Only ordinary precautions should be taken, such as not impeding the flow of air through the unit when it is operating, occasionally cleaning the suitcase and front panel with a damp cloth, and other reasonable care. The plastic storage door can be cleaned with soap and water or almost any commerical glass cleaner. The suitcase is water resistant, but if it has been exposed to extreme moisture, the tester should be disassembled and dried.

4.2 LED REPLACEMENT

All LEDs but the Power-On indicator can be replaced from the front of the front panel, without disassembling the tester. All LEDs in Display Registers A, B, and C should light when the General Clear pushbutton is depressed, regardless of the program being run. If an LED status indicator is suspected of being burned out, it can be moved to one of the display registers to be tested.

To remove the LED, simply pull it straight up and out of the panel. To insert an LED, orient the pin marked "+" away from you, toward the suitcase hinge. Then, holding the LED so that the two pins are aligned as close as possible to the sockets on the DISPlay board, move the LED slightly while applying light pressure until the pins are felt to enter the sockets. The key point in "finding" the sockets is to keep the LED pins aligned on a "6 o'clock" line between the front and back of the tester--only a slight twist of the LED will prevent the pins from finding the sockets. (If the chassis is removed from the suitcase, the pins can be lined up visually.)

To replace the Power On indicator, the chassis must be removed from the suitcase. LED replacement is then a simple matter of unplugging and removing the old one, inserting the new one, and attaching the plug.

4.3 REMOVAL OF CHASSIS FROM SUITCASE

Once the tester chassis is removed from the suitcase, the suitcase is top heavy and becomes very unstable and unwieldy. Therefore, precautions should be made to support the suitcase before the chassis is removed. It is also desirable to remove all items from the storage compartment prior to chassis removal. Then perform the following steps:

1) Remove the six screws as noted in Figure 4-1.

2) Lift the front of the front panel slightly.

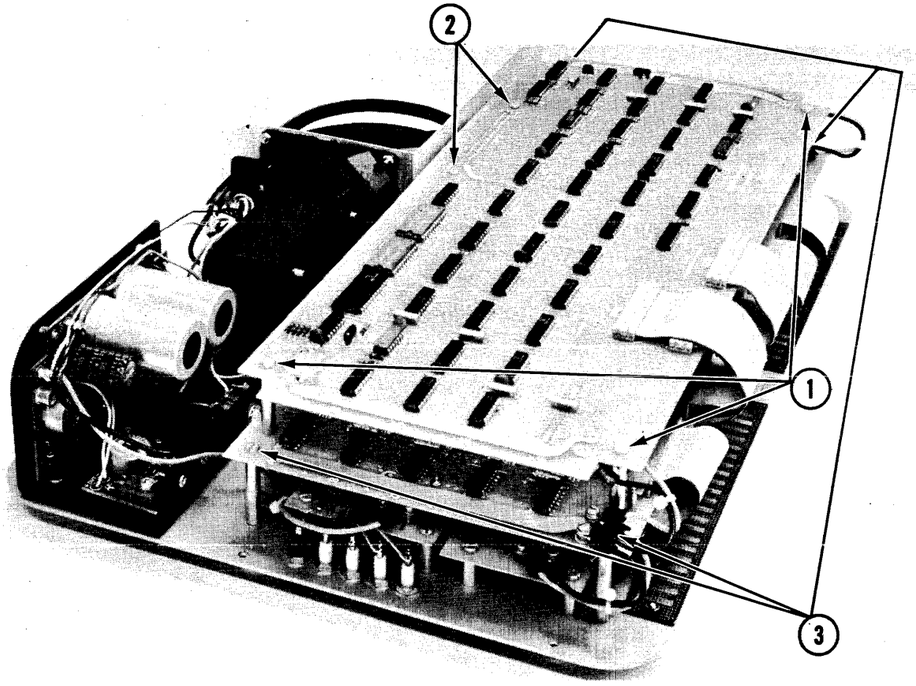
3) Slide front panel assembly toward you so that the panel overlaps the front of the suitcase.

4) Lift the rear of the front panel.

5) Slide the front panel to the rear and lift it out.

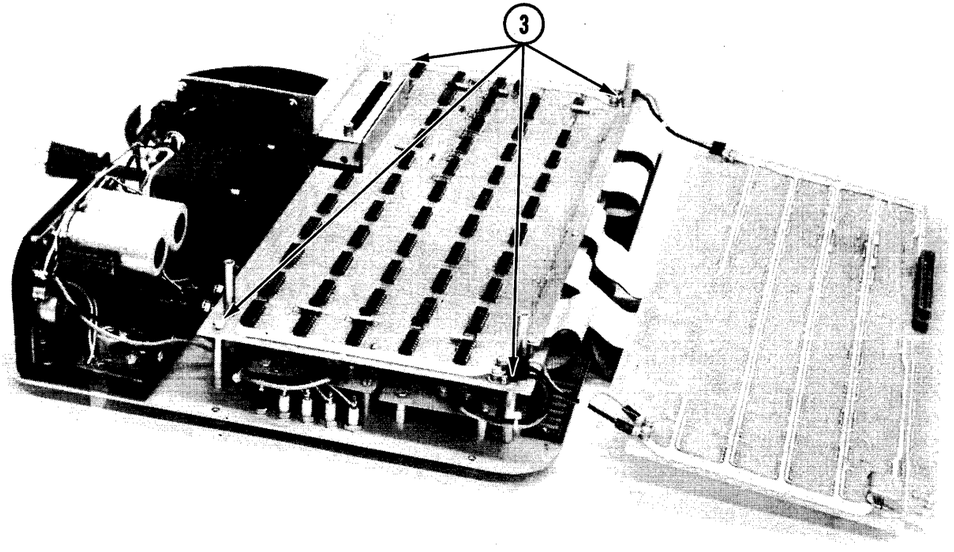
4.3.1 Replacement of Chassis

The front panel is replaced following the steps and pictures shown in Figure 4-1.



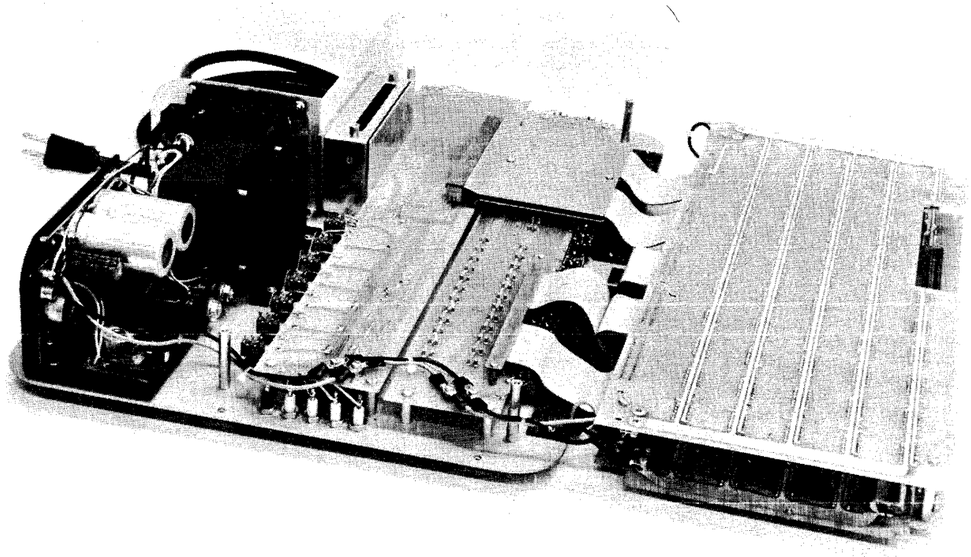
CHASSIS REMOVED FOR SERVICING

FIGURE 4-2



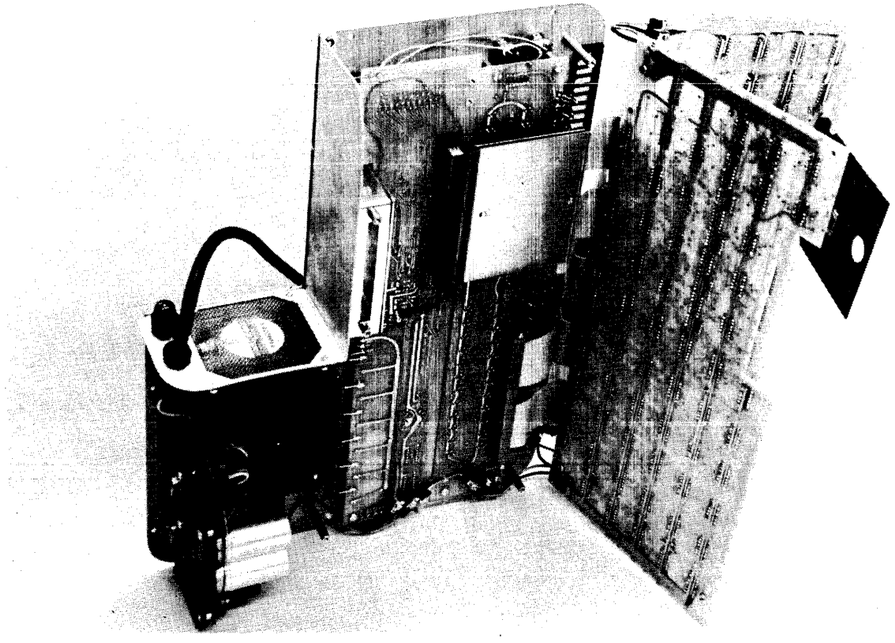
ACCESS TO I/O LOGIC BOARD

FIGURE 4-3



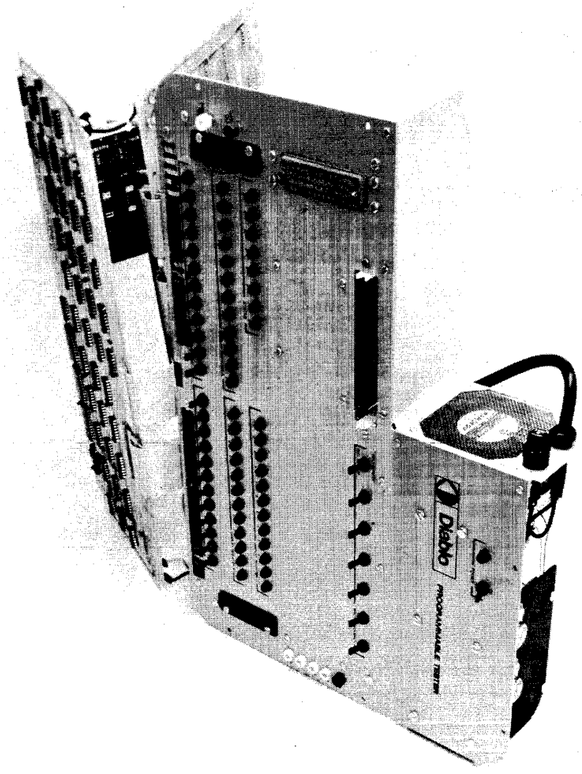
ACCESS TO DISPLAY & WRITE OSCILLATOR BOARDS

FIGURE 4-4



FULL PC BOARD ACCESS

FIGURE 4-5



TROUBLESHOOTING POSITION

FIGURE 4-6

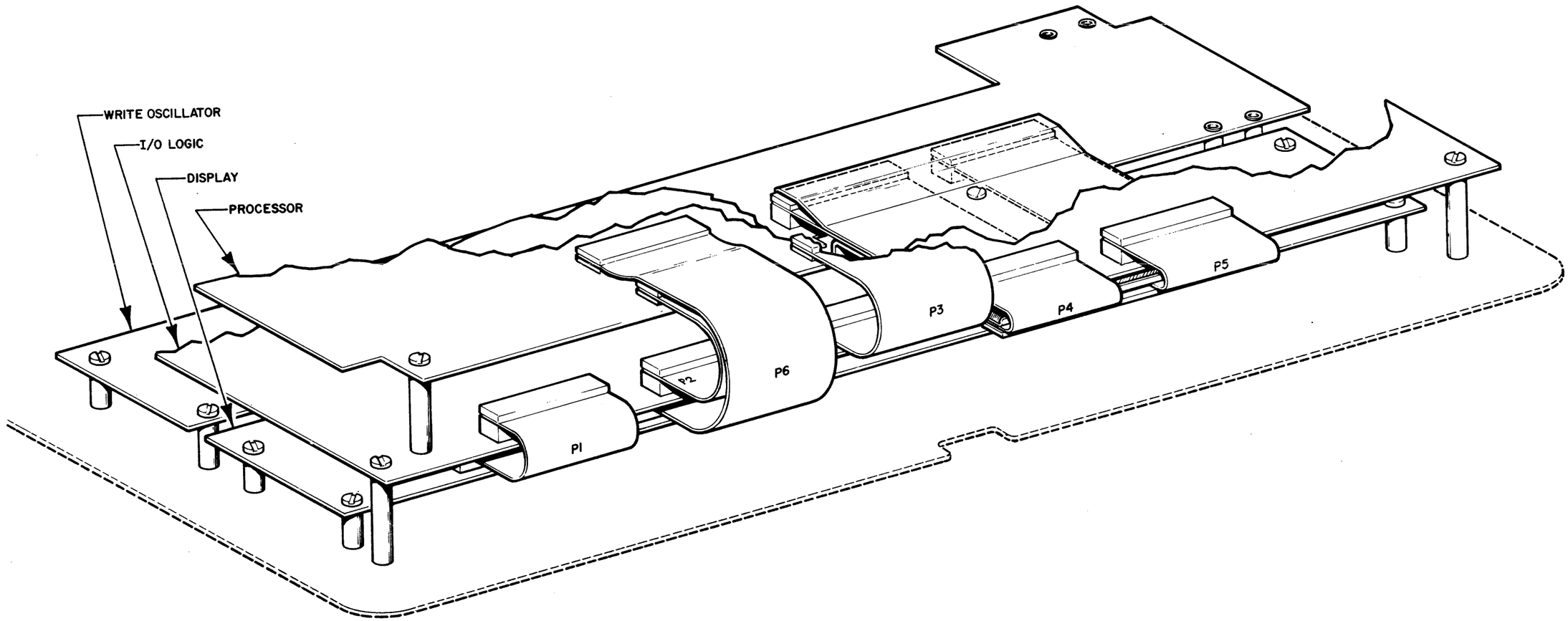
4.4 ACCESS TO LOGIC BOARDS

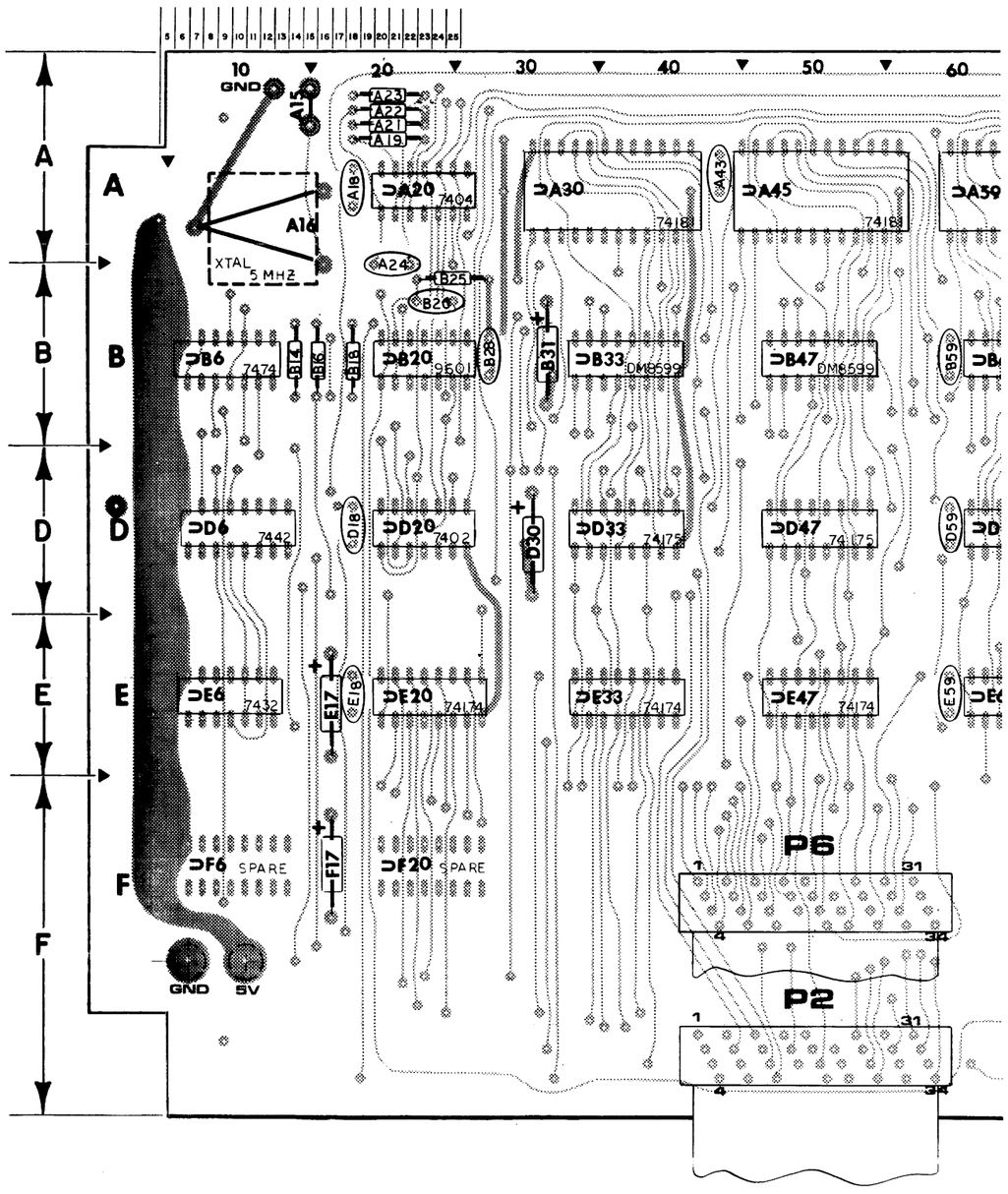
Once the front panel has been removed from the suitcase, the PROCessor logic board is accessible, as shown in Figure 4-2. By removing the five screws marked "1" and "2" in Figure 4-2, access can be gained to the I/O logic board, as shown in Figure 4-3. Or, by leaving in the "1" screws and removing the two "2" screws and four "3" screws, both the DISPlay and Write OSCillator boards can be reached, shown in Figure 4-4. By removing all "1", "2", and "3" screws, both sides of the PROCessor and I/O logic boards can be reached, but in this case the tester must be stood on its edge, as shown in Figure 4-5. This is often the best troubleshooting configuration, because in addition to providing the best access to all logic boards, the front panel is also accessible for operating the switches and observing the LEDs, shown in Figure 4-6. The PROGRAM board may be inserted and the program actually run in all positions other than that shown in Figure 4-2. However, if the adapter cable is to be used, the position shown in Figures 4-5 and 4-6 is preferable. When reassembling, note that screws "1" and "3" are the same, but the "2" screws are a different size.

Figure 4-7 (next page) is presented as an aid to proper reassembly of boards and cables in the event cables have to be unplugged for servicing.

INTERNAL CABLE CONNECTIONS

FIGURE 4-7





COORDINATE SYSTEM

FIGURE 4-8

4.5 COMPONENT LOCATION

The schematics list a letter-number coordinate (eg, D15) which can be used to locate each particular component on a board. Figure 4-8 illustrates the coordinate system used. Letters are printed in the approximate center of the area they refer to, whereas numbers appear at the beginning of their respective area. Card assembly drawings in Section 5 also illustrate the location of the various components, as well as identifying IC chips by type number. Coordinates given for IC chips are the approximate location of pin no. 1.

The DISPlay board does not use the coordinate system because there are so few components mounted on it.

Pin no. 1 of each IC is easily identified from the bottom (solder) side of the board by its square solder pad. This lessens the chance of errors in counting pin numbers.

4.6 COMPONENT REPLACEMENT

No unusual techniques need be employed for component replacement. However, sometimes when component changes are made, certain precautions or procedures should be observed. The points listed in the following paragraphs should be studied before any components are replaced on the respective circuit board.

4.6.1 Processor Logic Board

The chip in the B20 position, a 9601 one-shot, contains the CLOCK O/S, the timing of which is quite critical. Whenever this chip is replaced, the length of the one-shot's pulse should be measured and timing components should be changed in order to bring the time within the 70 ns, +0, -3 ns range. Since the resistor value is quite large in relation to the capacitor value, small changes in the pulse length are much easier to obtain by swapping out the resistor.

The short duration of this pulse makes the one-shot very sensitive to changes in its timing components' values, and even to stray capacitance in the timing circuit. Therefore, a "chip clip" should never be used directly on the one-shot when its length is being checked because the clip introduces enough capacitance to the timing circuit to materially affect the pulse length. Instead the clip should be placed on a chip that receives the one-shot's output and the pulse length checked at B6-3, D20-2, or D20-11.

4.6.2 I/O Logic Board

The I/O Logic board contains two 9600 one-shot chips, A133 and B144. If either of these ICs or any of their timing components are replaced, their pulse lengths should be checked and corrections made in the timing circuitry if necessary. Since the resistor value is quite large in relation to the capacitor value, small changes in the pulse length are much easier to obtain by swapping out the resistor.

4.6.3 Write Oscillator Board

Should any components need replacing on the Write Oscillator board, it is recommended that all wires from the Test Points (5), the Write Frequency Selection switches (7), and the pushbuttons (2) be unsoldered. This allows the board to be completely removed for servicing. Wires should be unsoldered at the circuit board.

4.6.4 Display Board

There are only four components mounted on the Display board. Should it ever become necessary to replace one of these, it should only be necessary to remove one wire--the one connecting E31 to the pushbutton switches. Then, after the necessary screws are removed and the cables unplugged, the board can be rotated on the remaining wires to provide access to the top of the board.

4.7 POWER SUPPLY ADJUSTMENTS

There are only two power supply adjustments; output voltage and overvoltage cutoff. The output voltage must be adjusted to precisely 5.0 V and the overvoltage protector must be adjusted to "short out" the +5 V supply should it ever increase to approximately 6.5 volts due to some malfunction. Since the output voltage must be varied in order to properly check the overvoltage adjustment, the overvoltage protector must be adjusted first. The overvoltage adjustment is more easily accomplished using an ordinary voltmeter, whereas the output voltage adjustment requires a digital voltmeter because of its greater accuracy. Use this procedure.

1) Disconnect wires from power supply to Display board. Unplug Power-On LED. Leave the overvoltage protector connected.

2) Connect voltmeter to the output terminals.

3) Set overvoltage protector potentiometer (see Figure 4-9) fully counter-clockwise, then back 1/8 turn clockwise.

4) Turn on power. Monitor the output voltage. Turn the voltage adjusting potentiometer (Figure 4-9) clockwise slowly to increase the output voltage until it suddenly drops to almost zero. Note the point from which it drops: it should be approximately 6.5 $\pm$ .2 V. If it is within this range, skip to step 8.

5) Turn off power. If the voltage cutoff point in the previous step was:

   too low, turn the OVP pot 1/8 turn clockwise.
   too high, turn the voltage adjustment pot 1/8 turn counter-clockwise.

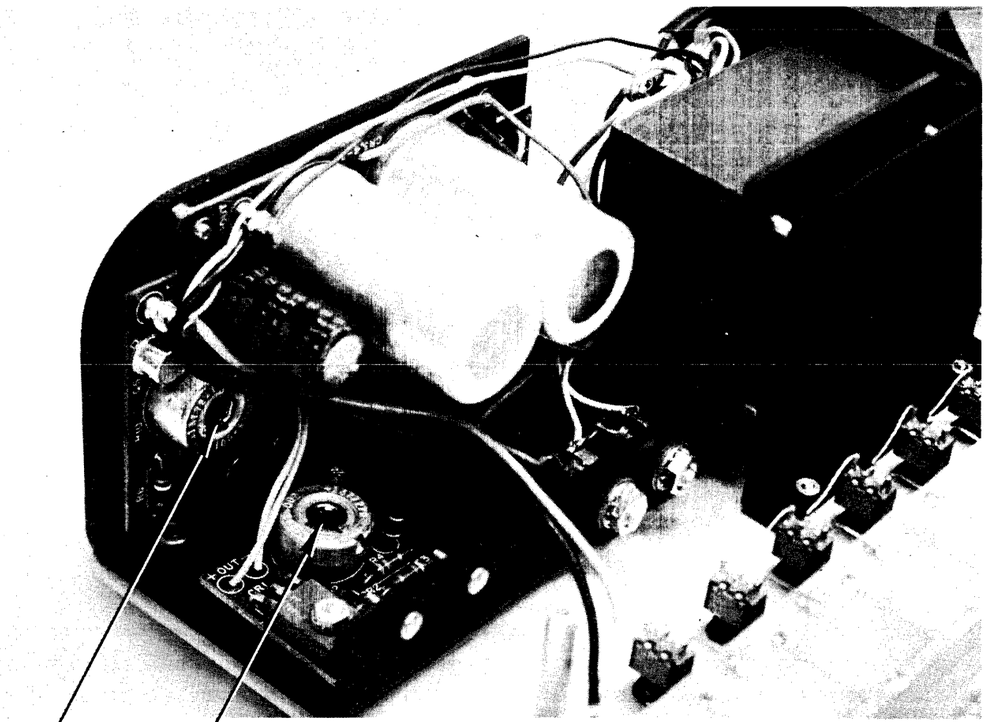
6) Turn on power. Adjust output voltage to 6.5 volts. Slowly turn the OVP pot counterclockwise until the output voltage drops. Turn off power.

7) Turn output voltage pot slightly counterclockwise (1/8 to 1/4 turn). Do not change setting of OVP pot. Turn on power. Slowly increase output voltage (turn pot clockwise) until output drops, again noting voltage at cutoff point. If the cutoff point is between 6.3 and 6.7 volts, go on to step 8. If not, return to step 5.

8) Turn off power. Connect digital voltmeter to output terminals. Turn voltage adjustment pot counterclockwise 1/4 to 1/2 turn. Turn on power. Adjust output to 5.0 volts, $\pm$.1 volt.

9) Turn off power. Reconnect wires to Display board. Plug in Power-On indicator LED.

10) Recheck output voltage and adjust if necessary.



POWER SUPPLY ADJUSTING POTS

FIGURE 4-9

4.8 POWER SUPPLY TROUBLESHOOTING

If the proper power supply adjustments cannot be obtained using the foregoing procedure, there is probably a malfunction in the power supply. Figure 4-10 is supplied by Powertec to aid in troubleshooting the power supply.

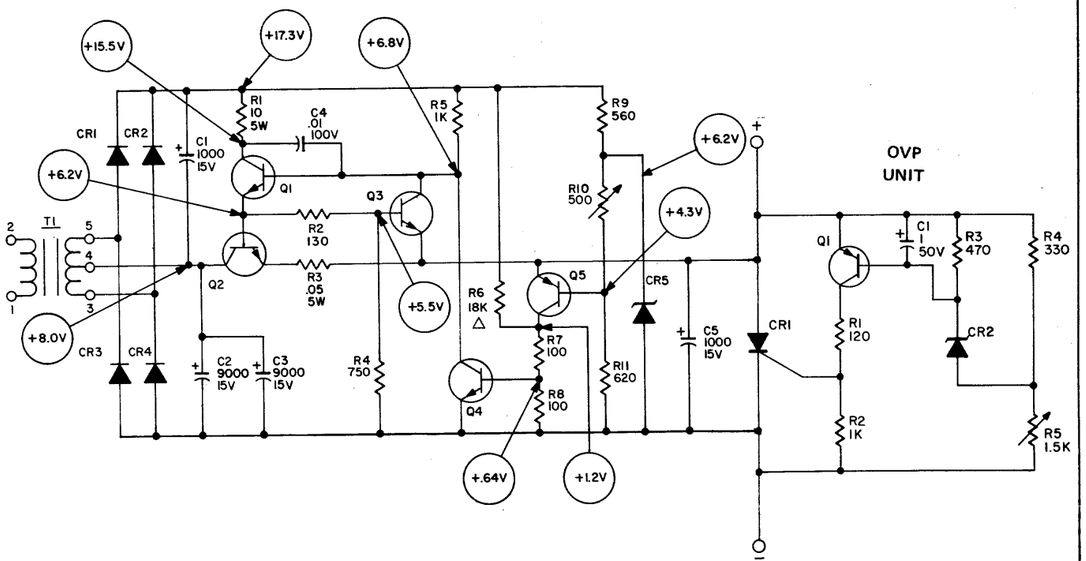
TROUBLESHOOTING GUIDE CHECK VOLTAGE TEST POINTS SHOWN ON SCHEMATIC FOR EASE OF FAILURE DETERMINATION.	
FAILURE INDICATION:	**CHECK:**
1. HIGH INPUT CURRENT, BLOWS FUSES.	C1-C3 SHORTED. CR1-CR4 SHORTED.
2. POOR REGULATION, HIGH OUTPUT RIPPLE.	C1-C3 OPEN. CR1-CR4 OPEN. Q2 SHORTED. POSSIBLE OUTPUT OVERLOAD.
3. HIGH OUTPUT VOLTAGE AND RIPPLE, POOR REGULATION.	Q1, Q2 SHORTED. Q4 OPEN.
4. LOW OUTPUT VOLTAGE WITH EXCESSIVE RIPPLE.	C5 LEAKY CR1-CR4 OPEN Q3 SHORTED POSSIBLE OUTPUT OVERLOAD.
5. EXCESSIVE UNIT HEATING.	IMPROPER INPUT FREQUENCY OR VOLTAGE. POSSIBLE OUTPUT OVERLOAD. INADEQUATE VENTILATION. IMPROPER PRIMARY – SECONDARY TRANSFORMER TAP CONNECTION. (SEE SCHEMATIC)

	OVP UNIT
FAILURE INDICATION	**CHECK**
1. UNIT REMAINS SHORTED AFTER AN OVERVOLTAGE CONDITION IS CORRECTED.	SCR1 SHORTED Q1 SHORTED CR2 SHORTED
2. UNIT REMAINS SHORTED AFTER ALL VOLTAGE IS REMOVED.	SCR1 SHORTED
3. UNIT TRIGGERS ERRATICALLY ON NOISE SPIKES OR TRANSIENTS.	C1 OPEN
4. UNIT FAILS TO TRIGGER.	SCR1 OPEN Q1 OPEN CR2 OPEN R5 OPEN C1 SHORTED

SPECIFICATIONS:
AC INPUT: 105 TO 125 VAC, 57 TO 63 HZ
DC OUTPUT: 6 A. MAXIMUM
REGULATION: LINE + 0.25%, LOAD + 0.25%
OUTPUT RIPPLE: 1.5 MILLIVOLT RMS, 5 MV. PK-PK
OVERLOAD PROTECTION: UNIT IS PROTECTED FROM OVERLOAD AND SHORT CIRCUIT USING THE CURRENT FOLDBACK METHOD.

OPERATING TEMPERATURE: SEE TABLE BELOW

PERCENT OF FULL RATED LOAD AT TEMP.			
+ 40°C	+ 50°C	+ 60°C	+ 71°C
100%	75%	50%	30%



3. TEST VOLTAGES ARE TAKEN AT FULL RATED LOAD CURRENT, 115 VAC INPUT. OUTPUT VOLTAGE ADJUSTED TO 5.0 VOLTS.
2. ALL VOLTAGES ARE REFERENCED TO NEGATIVE OUTPUT.
1. △ INDICATES NOMINAL VALUE
NOTE: UNLESS OTHERWISE SPECIFIED

CONTRACT NO.	POWERTEC DIVISION AIRTRONICS INCORPORATED 9168 DESOTO AVE., CHATSWORTH, CALIF. 91311	
APPD		
CHECK	D. WEISSE	10-22-70
DRAWN	M. PIERCE	9-8-70
APPROVED		10-22-70
APPROVED		
TITLE	OEM SERIES MODEL 2C5-6	
SIZE C	CODE IDENT NO. 24429	DRAWING NUMBER 12928 REV. D
SCALE —		SHEET 1 OF 1

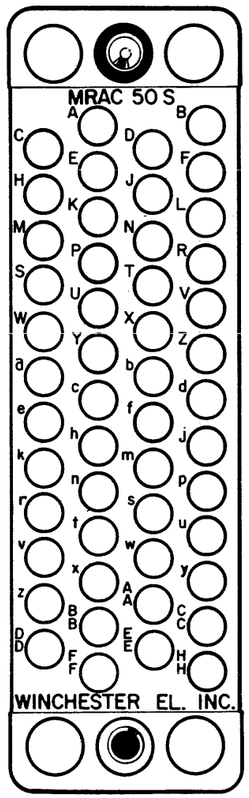
POWER SUPPLY TROUBLESHOOTING

FIGURE 4-10

4.9 FRONT PANEL CONNECTOR

Figure 4-11 is included as an aid to locating pins on the front panel connector. It can also be used to locate I/O cable points when the I/O cable is plugged into the front panel.

When checking the tester output lines, bear in mind that these open-collector outputs are pulled up to +5 volts by circuitry within the device being tested--if no device is connected, these lines will not rise to +5 V when they are disabled. If a true representation of these lines is desired (for troubleshooting purposes) with no device connected, each line should be returned to +5V (connector pin r), through a 1k to 5k resistor, as it is being tested.



I/O CONNECTOR PIN LAYOUT

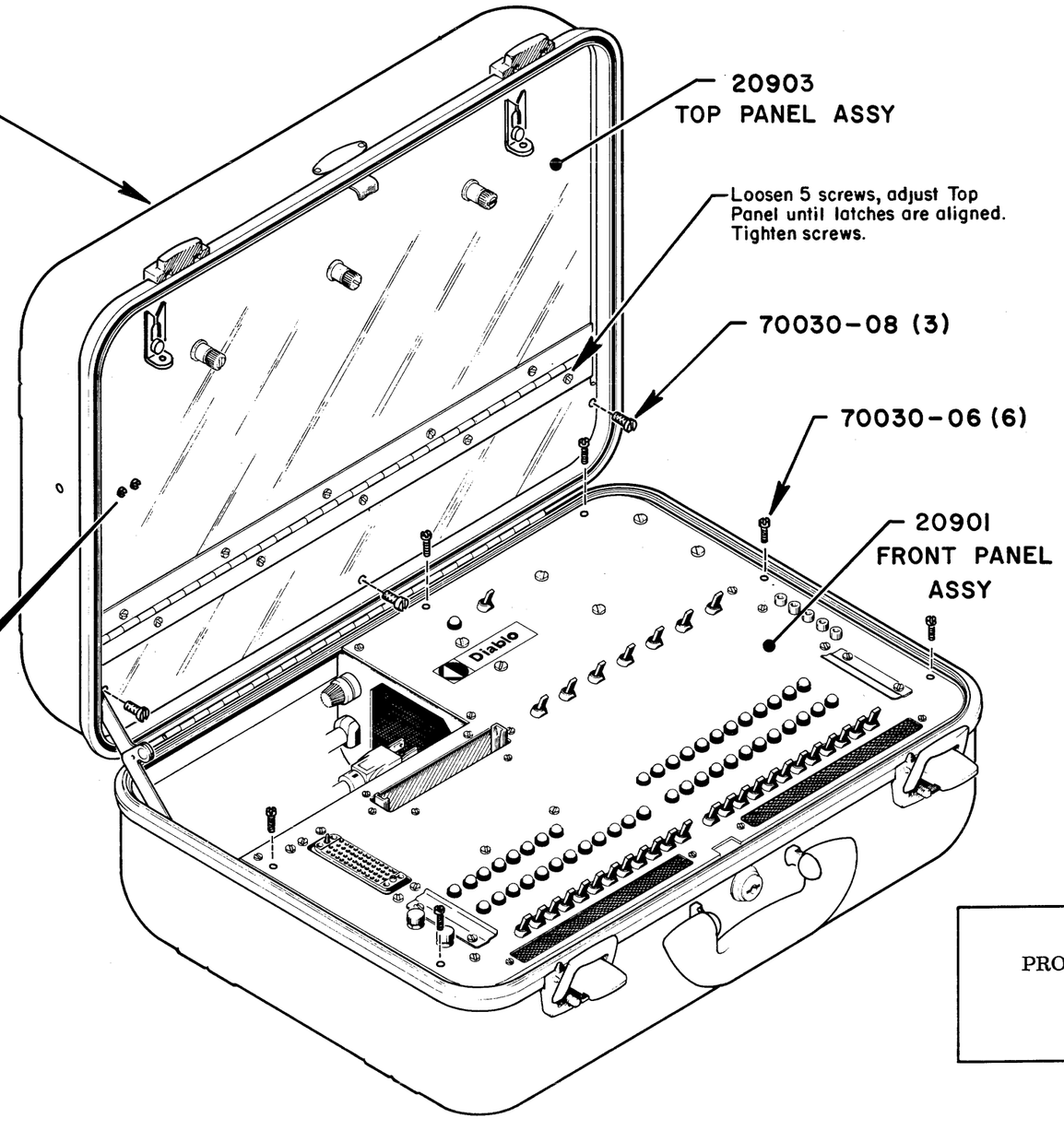
FIGURE 4-11

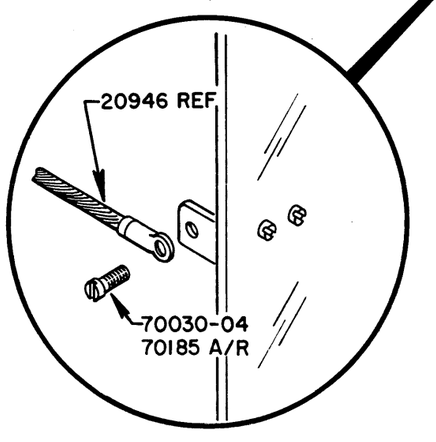
Section 5

PARTS

PRODUCT NO. 20900

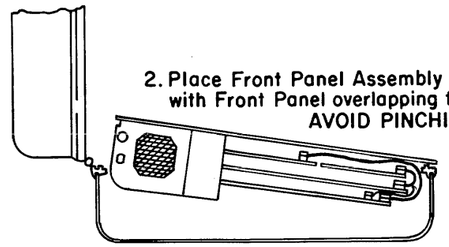
PRODUCT NO. 20900 DEVELOPMENT REV.



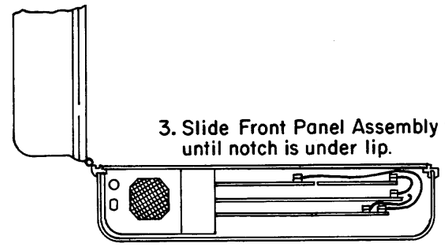


ASSEMBLY STEPS FOR INSTALLING FRONT PANEL ASSEMBLY IN SUITCASE ASSEMBLY.

1. Clean interior of suitcase thoroughly.



2. Place Front Panel Assembly in suitcase with with Front Panel overlapping front of suitcase. AVOID PINCHING CABLES.



3. Slide Front Panel Assembly to rear until notch is under lip.

4. Install the six screws, adjust Front Panel Assembly to give the latch clearance and then tighten screws.

PROGRAMMABLE TESTER ASSEMBLY

FIGURE 5-1

Diablo Systems incorporated

TITLE: PROGRAMMABLE TESTER ASSEMBLY

MODEL: 500

PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED. SYSTEM LOGIC NO.

SHEET 1 | TOTAL SHEETS 2 | SIZE D | PRODUCT NO 20900 | REV A

DRAWN C.Lowell 7-73 | CHECKED | ENG | MFG | DATE

REV J E.C.O. NO. | REV H E.C.O. NO. | REV G E.C.O. NO. | REV F E.C.O. NO. | REV E E.C.O. NO. | REV D E.C.O. NO. | REV C E.C.O. NO. | REV B E.C.O. NO. | REV A E.C.O. NO.

PRODUCT NO 20900 | REFERENCE DESIGNATORS NOT USED | REFERENCE DESIGNATORS LAST USED

DCT CTL 0020, 1-25-73

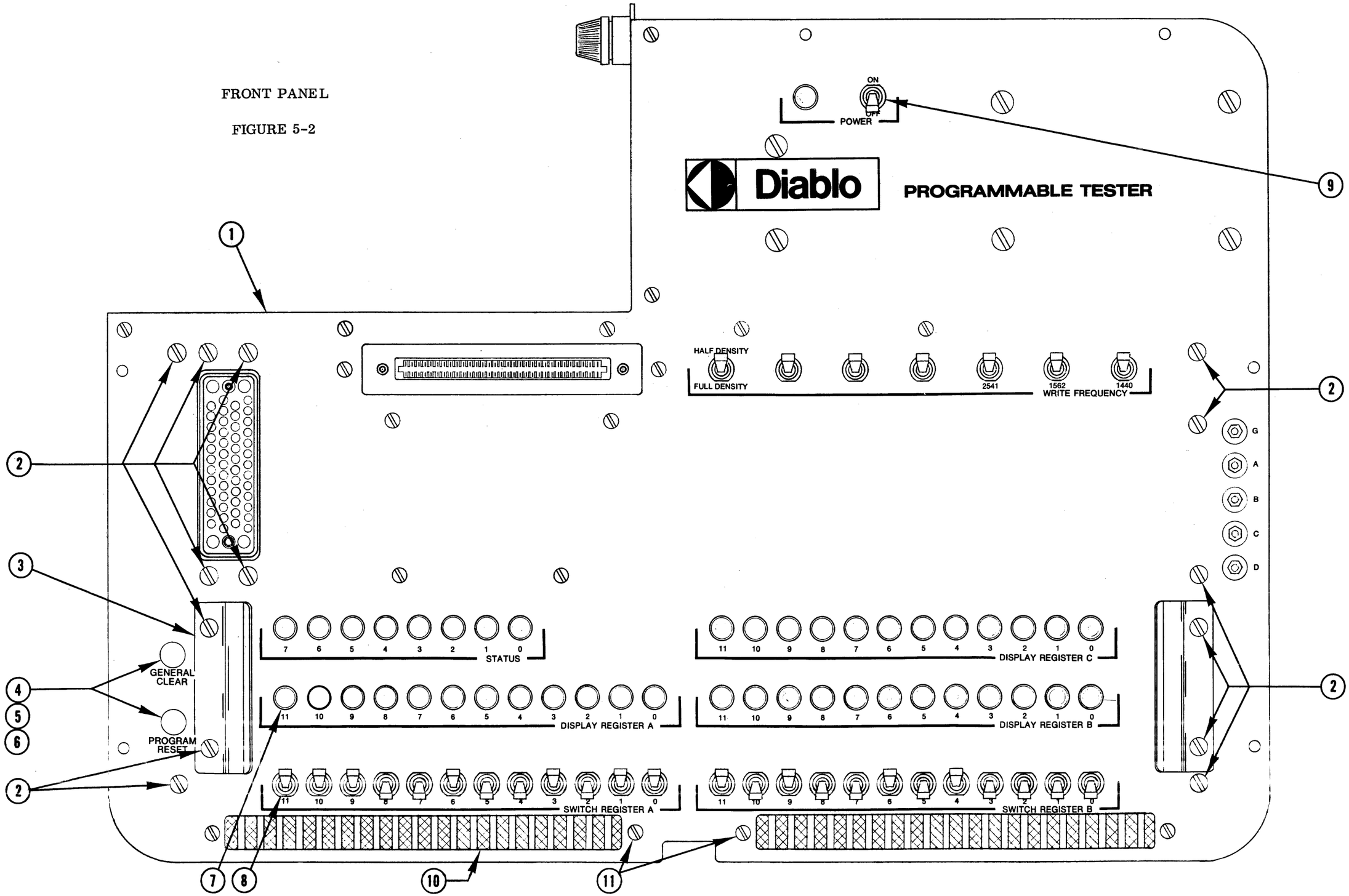
FRONT PANEL

(Figure 5-2)

ITEM	PART NUMBER	DESCRIPTION
1	20908	Plate, Front Panel, silkscreened
2	70030-04	Screw, 6-32 x 1/4, Pan hd. (14)
3	20944	Clip (2)
4	10729-01	Switch, Pushbutton, SPDT (2)
5	10734-03	Cap, Pushbutton switch, Red
6	10734-05	Cap, Pushbutton switch, Yellow
7	10732-01	Indicator LED (45)
8	10579-01	Switch, toggle, SPDT (31)
9	10763	Switch, toggle, DPDT
10	20918	Grille, air inlet (2)
11	70029-04	Screw, 4-40 x 1/4, Pan hd. (4)

FRONT PANEL

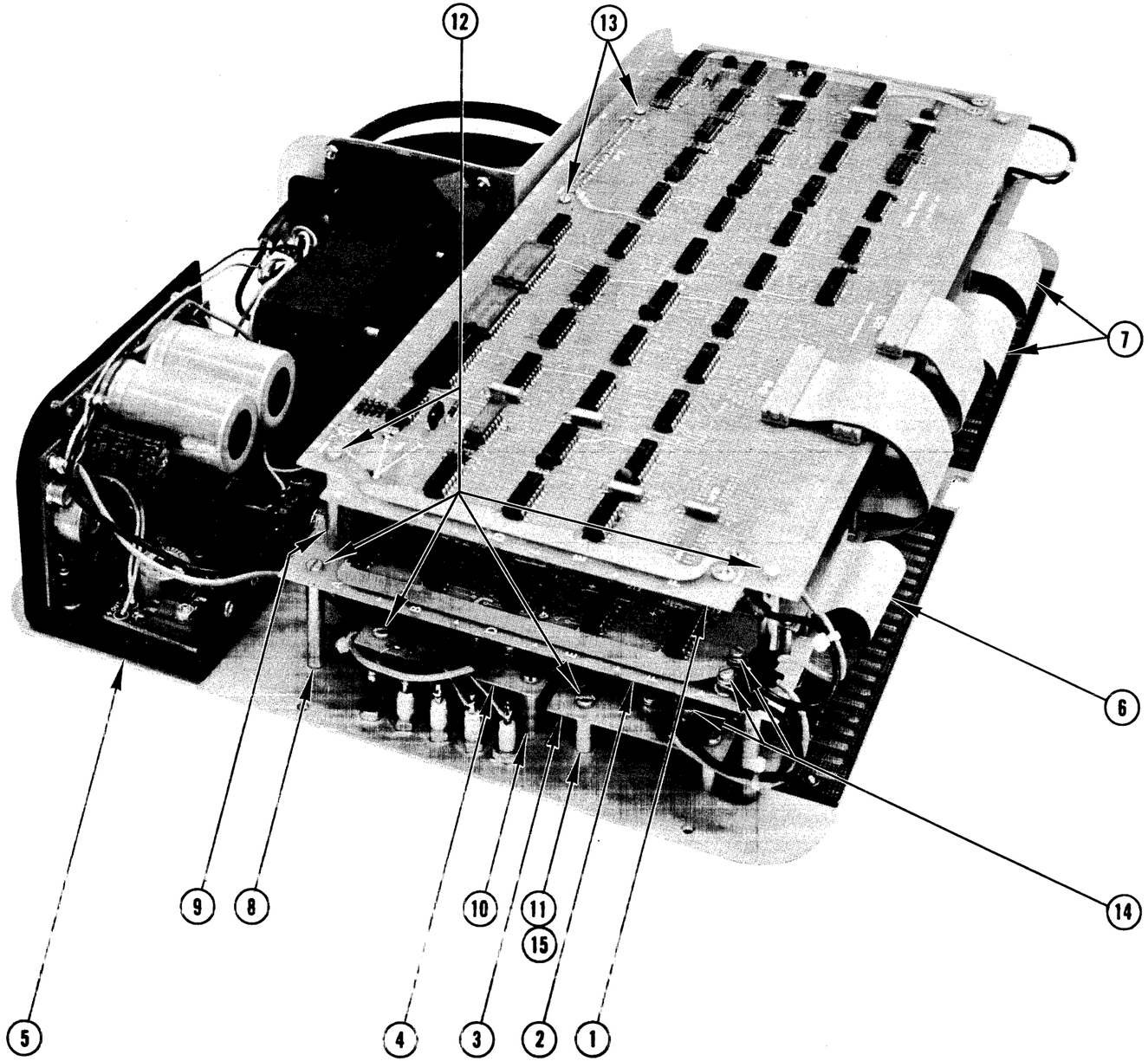
FIGURE 5-2



FIRST LEVEL HARDWARE

(Figure 5-3)

ITEM	PART NUMBER	DESCRIPTION
1	21037	PROC Logic board assy. (Figure 5-12)
2	21035	I/O Logic board assy. (Figure 5-13)
3	21033	DISP board assy. (Figure 5-15)
4	21031	WOSC board assy. (Figure 5-14)
5	20904	Power supply assy. (Figures 5-7, 5-8, 5-9)
6	21047-01	Cable, P1
7	21047-02	Cable, P4, P5
8	70409-23	Standoff, 1/4 x 1-7/16, 6-32 thd. (4)
9	70409-21	Standoff, 1/4 x 1-5/16, 6-32 thd. (3)
10	70409-12	Standoff, 1/4 x 3/4, 6-32 thd. (2)
11	70409-10	Standoff, 1/4 x 5/8, 6-32 thd. (4)
12	70030-04	Screw, 6-32 x 1/4, Pan hd. (13)
13	70029-10	Screw, 4-40 x 5/8, Pan hd. (2)
14	70029-04	Screw, 4-40, x 1/4, Pan hd. (12)
15	10553	Insulator, #6 x .003 (4). Mount between PC board and standoff on DISPlay board (early production units only).

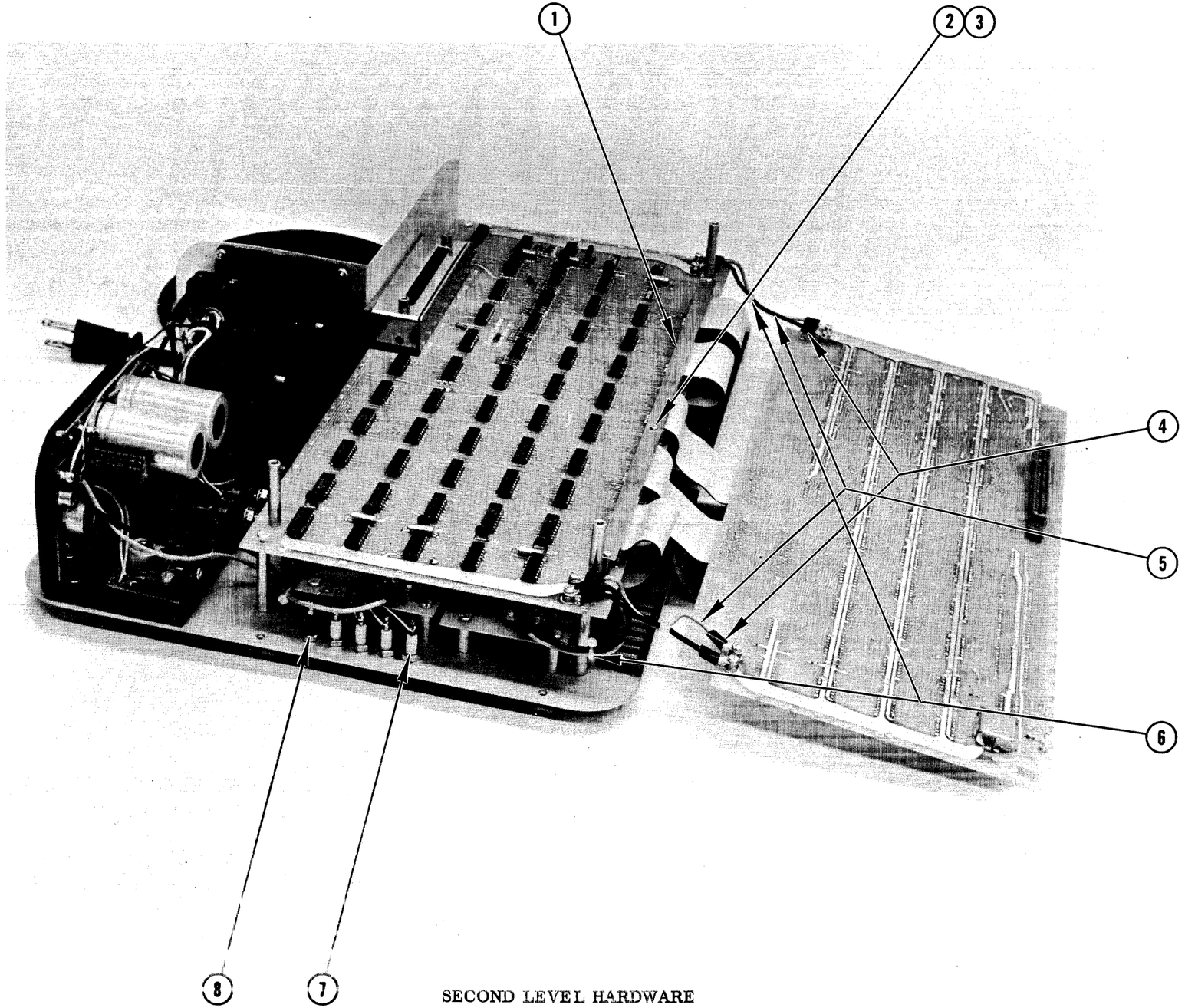


FIRST LEVEL HARDWARE
FIGURE 5-3

SECOND LEVEL HARDWARE

(Figure 5-4)

ITEM	PART NUMBER	DESCRIPTION
1	20911	Bracket, Connector Locking, (five 34-position plugs)
2	70027-03	Screw, 2-56 x 3/16 Pan hd. (3)
3	70169-02	Flat Washer, #2 (3)
4	10514-10	Ring Terminal, crimped, 14/16 AWG, for #4 stud (18 total)
5	Not available separately	Wire, #14 AWG (A/R)
6	10538-01	Wire Tie (3)
7	10730-02	Jack, yellow (4)
8	10730-01	Jack, black



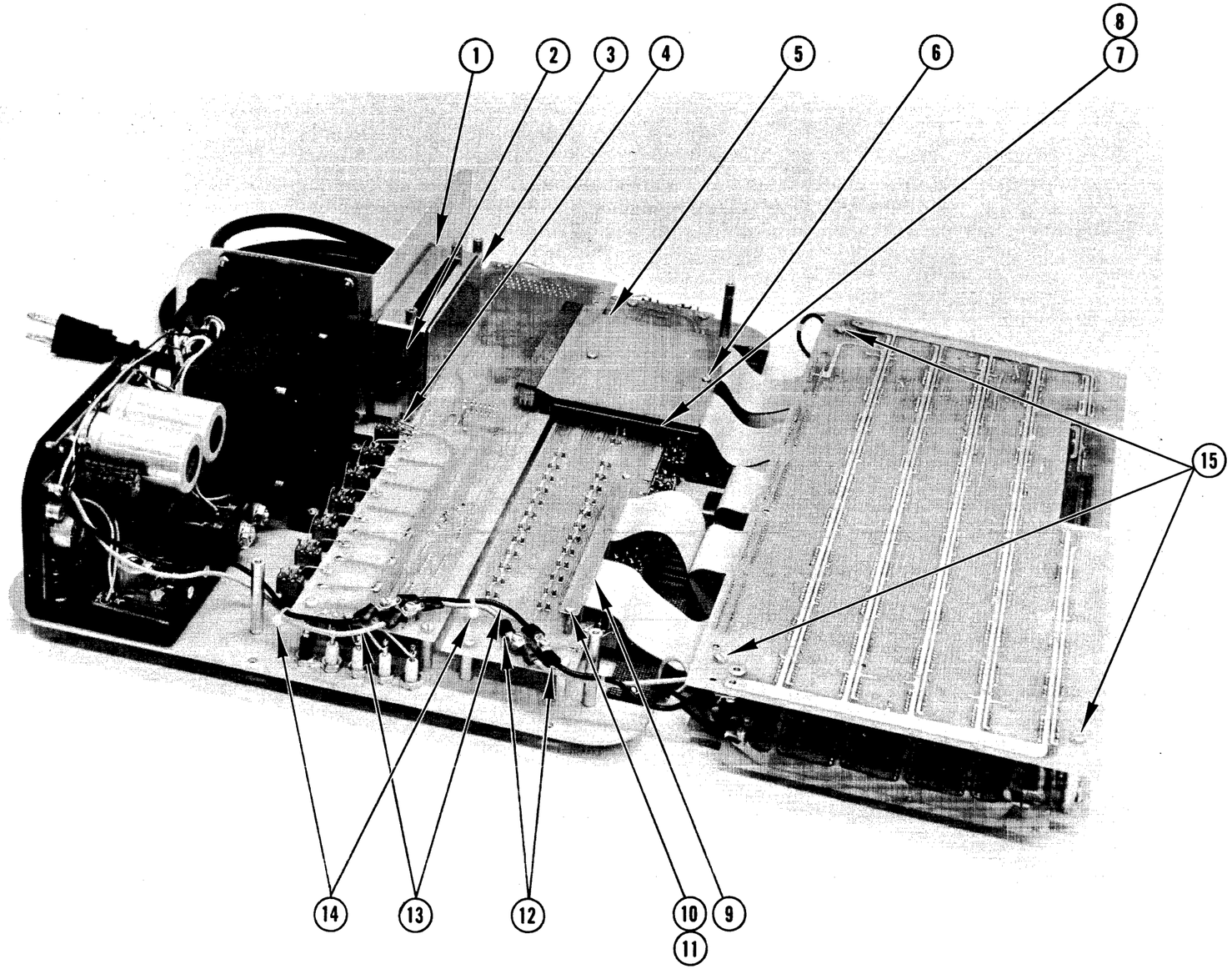
SECOND LEVEL HARDWARE

FIGURE 5-4

THIRD LEVEL HARDWARE

(Figure 5-5)

ITEM	PART NUMBER	DESCRIPTION
1	20916	Bracket, PRGM board
2	10724-01	Card Guide, Snap-in, 2-1/2" (2)
3	209	Shield, PRGM board
4	700 -04	Screw, 4-40 x 1/4 Pan hd. (4) (2 mount 20916 Bracket to front panel; 2 mount 20941 Shield to front panel.)
5	20913	Shield, flat cable
6	70029-04	Screw, 4-40 x 1/4 Pan hd. (2)
7	20912	Support, flat cable shield
8	70029-04	Screw, 4-40 x 1/4 Pan hd. (2) (To mount 20912 support to front panel.)
9	20910	Bracket, Connector locking (two 34-position plugs)
10	70027-03	Screw, 2-56 x 3/16 Pan hd. (2)
11	70169-02	Flat washer, #2 (2)
12	10514-10	Ring Terminal, crimped, 14/16 AWG, for #4 stud (18 total)
13	Not available separately	Wire, #14 AWG (A/R)
14	10538-01	Wire Tie (2)
15	70030-04	Screw, 6-32 x 1/4 Pan hd. (3)



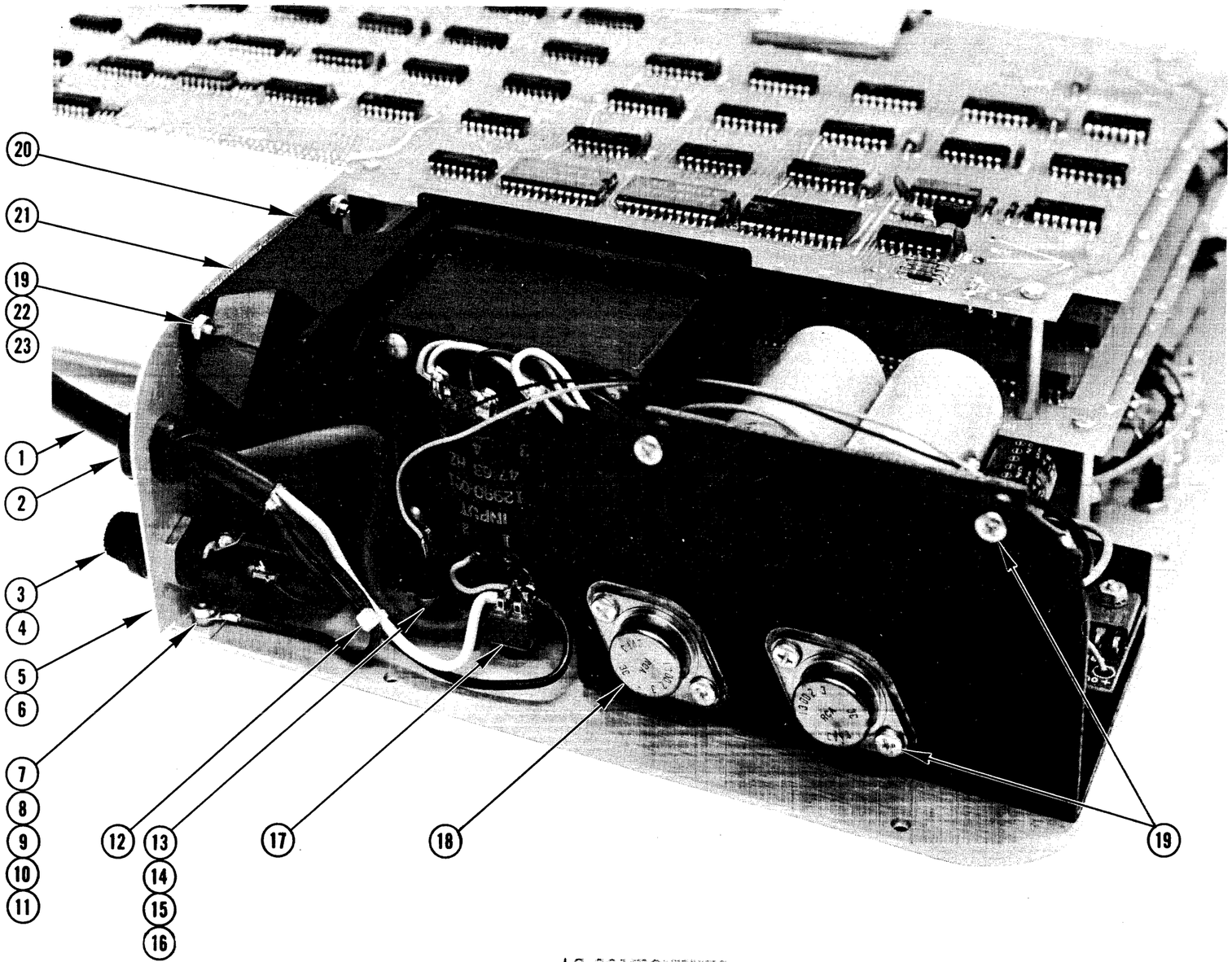
THIRD LEVEL HARDWARE

FIGURE 5-5

AC COMPONENTS

(Figure 5-6)

ITEM	PART NUMBER	DESCRIPTION
1	10638-01	Power Cord
2	10608-01	Strain Relief
3	10705	Fuse Holder
4	10745-01	Fuse, 1 amp Slo-blo, 3AG
5	20919	Bracket, Fan mounting
6	20942	Gasket, PRGM board shield, 2-1/4 x 4-3/8 x 1/8 Neoprene
7	70029-06	Screw, 4-40 x 3/8 Pan hd.
8	70425-04	Star washer, #4, int star
9	10616-04	Terminal
10	70168-04	Lockwasher, #4
11	70166-04	Hex Nut, 4-40
12	10538-01	Wire Tie
13	10732-01	Indicator LED
14	10702	Washer, Indicator
15	10700	Clip, Indicator mounting
16	10701	Socket, Indicator
17	10763	Switch, Power, DPDT
18	See Fig. 5-7	Power Transistor Q1 & Q2
19	70030-06	Screw, 6-32 x 3/8 Pan hd. (10)
20	10611-01	Fan
21	Not available separately	Screen, Fan, 29 ga. aluminum wire, #15 mesh
22	70168-06	Lockwasher, #6 (4)
23	70166-66	Nut, 6-32 x 1/4 Hex (4)



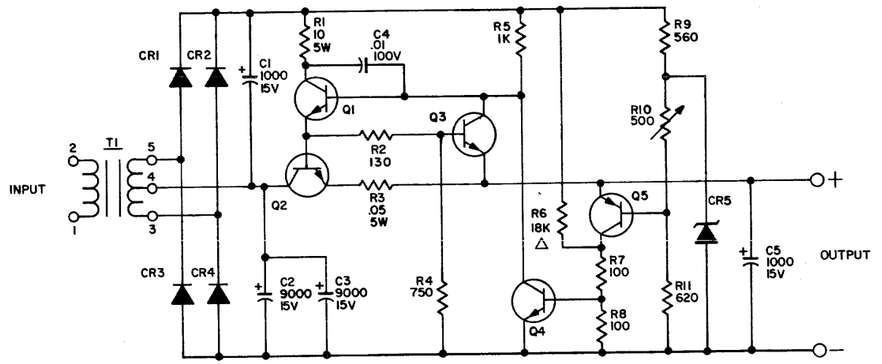
AC COMPONENTS

FIGURE 5-6

SYM	POWERTEC P/N	COM'L EQUIV	DESC
C1,5	32-13006-003	PCZ1000PN15	1000 MFD, 15V
C2,3	32-13008-001	STM23C15AA93	9,000 MFD, 15V
C4	31-13005-003	NPC-EL	.01MFD, 100V
CR1,2	11-13009-001	SI-2	——
CR3,4	11-13012-001	IN1200	——
CR5	12-13013-008	IN4735A	——
R1	22-13049-002	PW5-10Ω, 10%	10Ω, 5W, 10%
R7,8	20-13004-049	RC20GF101J	100Ω, 1/2W, 5%
R3	22-13280-001	KS500	.05Ω, 5W, 15%
R4	20-13004-070	RC20GF751J	750Ω, 1/2W, 5%
R5	20-13004-073	RC20GF102J	1K, 1/2W, 5%
R6 △	20-13004-103	RC20GF183J	18K, 1/2W, 5%
R9	20-13004-067	RC20GF561J	560Ω, 1/2W, 5%
R10	23-13016-001	CTS-111	500Ω
R11	20-13004-068	RC20GF621J	620Ω, 1/2W, 5%
Q1,2	10-13002-003	2N3055	——
Q3,4	10-13018-001	2N2219A	——
Q5	10-13021-001	2N2905A	——
CHASSIS	50-12931-001	——	——
P.C.B.	55-12891-001	——	——
T1	40-12990-001	——	——
R2	20-13004-052	RC20GF131J	130Ω, 1/2W, 5%

1. △ INDICATES NOMINAL VALUE.

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVED
A	SEE ECN 010422	4-7-71	
B	SEE ECN 010746	6-18-71	
C	SEE ECN 010998	9-29-71	
D	SEE ECN 011231	12-3-71	



QTY REQD	PART NO. OR TYPE DESIGNATION	SYM	NOMENCLATURE OR DESCRIPTION	CODE IDENT	MATERIAL, NOTES AND SPECIFICATIONS	ITEM NO.

LIST OF MATERIALS

UNLESS OTHERWISE SPECIFIED:
DIMENSIONS ARE IN INCHES
TOLERANCES ON
DECIMALS X ±.060, .XX ±.030, .XXX ±.010
ANGLES X° ±1°0', X°X' ±0°30'
DIM. AND TOL PER MIL-STD-8
MACHINED DIA'S ON COMMON CENTER CONCENTRIC WITHIN .005 T.I.R.
125 MACHINED SURFACE ROUGHNESS PER MIL-STD-10
REMOVE BURRS, BREAK EDGES .010 MAX
DO NOT SCALE DRAWING
REPORT ERRORS TO ENGINEERING DEPT
DO NOT MAKE CHANGES WITHOUT PROPER AUTHORIZATION

NEXT ASSY | FINAL ASSY
MATERIAL
FINISH

CONTRACT NO.

APPD	[illegible]	[illegible]
CHECK	D. WEISSE	10-22-70
DRAWN	M. PIERCE	9-8-70
APPROVED	SR	0-22-70
APPROVED		

POWERTEC DIVISION
AIRTRONICS INCORPORATED
9168 DESOTO AVE., CHATSWORTH, CALIF. 91311

TITLE
OEM SERIES
MODEL 2C5-6

SIZE	CODE IDENT NO.	DRAWING NUMBER	REV
C	24429	12928	D

SCALE —— SHEET 1 OF 1

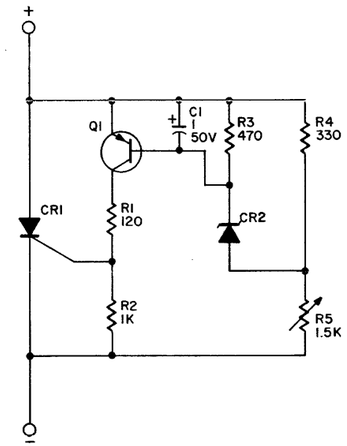
COPY 12928

POWER SUPPLY COMPONENTS

FIGURE 5-7

SYM	POWERTEC P/N	COM'L EQUIV	DESC
C1	32-13006-001	PCZ1PA50	1 MFD, 50V
CR1	13-13015-001	2N4441	——
CR2	12-13025-007	IN752A	——
R1	20-13004-051	RC20GF121J	120Ω, 1/2W, 5%
R2	20-13004-073	RC20GF102J	1K, 1/2W, 5%
R3	20-13004-065	RC20GF471J	470Ω, 1/2, 5%
R4	20-13004-061	RC20GF331J	330Ω, 1/2W, 5%
R5	23-13016-002	CTS-111	1.5K
Q1	10-13020-001	2N2907A	——
BRACKET	50-12836	——	——
P.C.B.	55-12789	——	——

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVED



QTY REQD	PART NO. OR TYPE DESIGNATION	SYM	NOMENCLATURE OR DESCRIPTION	CODE IDENT	MATERIAL, NOTES AND SPECIFICATIONS	ITEM NO.

LIST OF MATERIALS

UNLESS OTHERWISE SPECIFIED:
DIMENSIONS ARE IN INCHES
TOLERANCES ON
DECIMALS X ±.060, .XX ±.030, .XXX ±.010
ANGLES X° ±1°0', X°X' ±0°30'
DIM. AND TOL PER MIL-STD-8
MACHINED DIA'S ON COMMON CENTER CONCENTRIC WITHIN .005 T.I.R.
125 MACHINED SURFACE ROUGHNESS PER MIL-STD-10
REMOVE BURRS, BREAK EDGES .010 MAX
DO NOT SCALE DRAWING
REPORT ERRORS TO ENGINEERING DEPT
DO NOT MAKE CHANGES WITHOUT PROPER AUTHORIZATION

NEXT ASSY | FINAL ASSY
MATERIAL
FINISH

CONTRACT NO.

APPD	SR	10/29/70
CHECK	D. WEISSE	10/29/70
DRAWN	M. PIERCE	10-26-70
APPROVED	[signature]	10/29/70
APPROVED		

POWERTEC DIVISION
AIRTRONICS INCORPORATED
9168 DESOTO AVE., CHATSWORTH, CALIF. 91311

TITLE
OEM OVP
ADJ. 6.5 TO 30VDC
12 AMPS MAX.

SIZE	CODE IDENT NO.	DRAWING NUMBER	REV.
C	24429	13207	NC

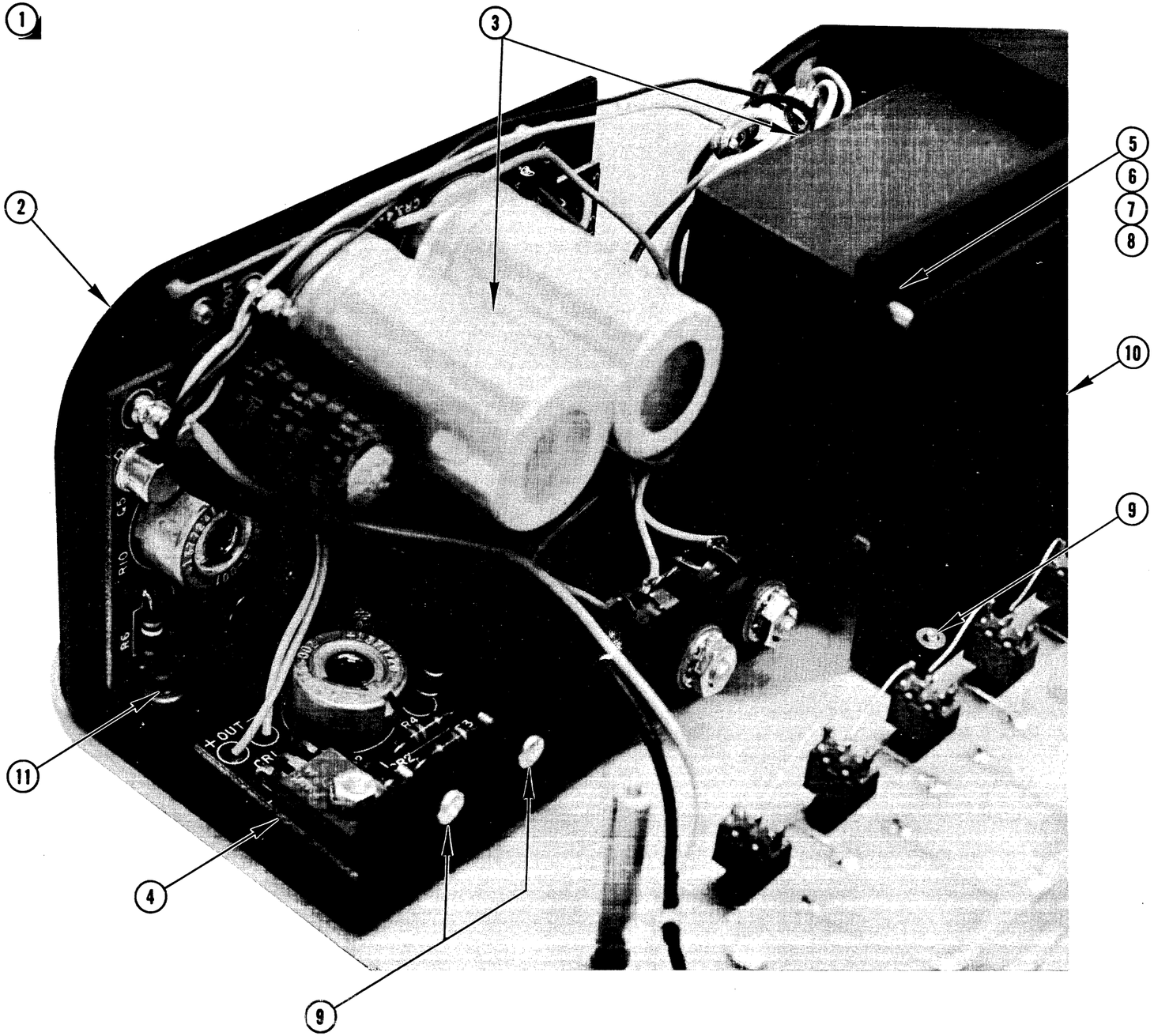
SCALE — SHEET 1 OF 1

COPY 13207 NC

OVERVOLTAGE PROTECTOR

FIGURE 5-8

ITEM	PART NUMBER	DESCRIPTION
1	20904	Heatsink/Power Supply Assy. (Includes items 2 through 9)
2	20921	Heatsink
3	70456	Power Supply, Powertec Model 2C5-6 (Includes Regulator board, Transformer, Power Transistors, and Diodes) For parts breakdown, refer to Figure 5-7.
4	70457	Overvoltage Protector, Powertec Model OVP-1 For parts breakdown, refer to Figure 5-8.
5	70031-32	Screw, 8-32 x 2 (4)
6	70169-08	Flatwasher, #8 (12)
7	70168-08	Lockwasher, #8 (4)
8	70166-08	Hex nut, 8-32 (4)
9	70029-04	Screw, 4-40 x 1/4 Pan hd. (4)
10	20922	Transformer shield
11	70031-06	Screw, 8-32 x 3/8 (6)



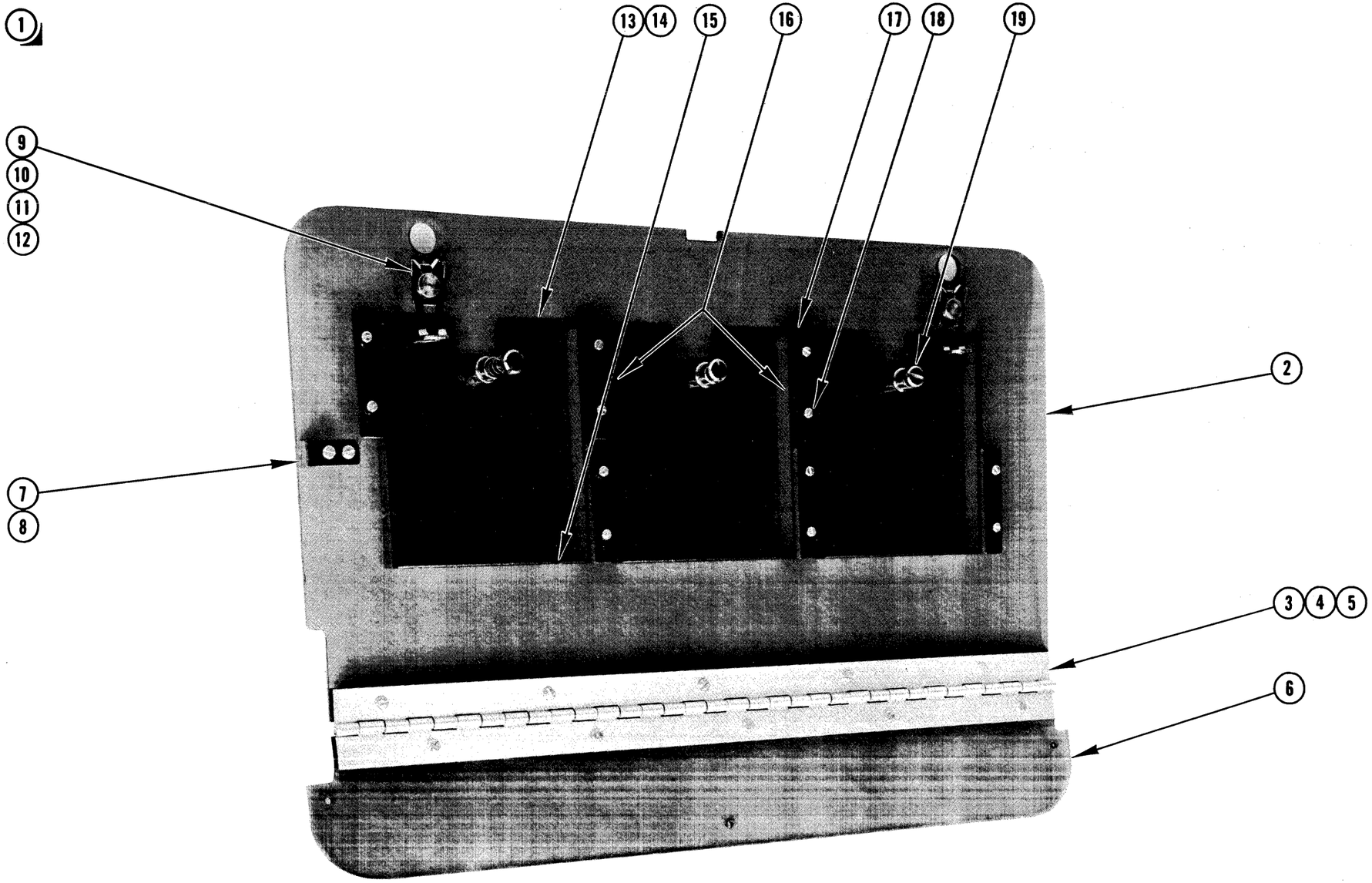
POWER SUPPLY

FIGURE 5-9

STORAGE COMPARTMENT DOOR ASSEMBLY

(Figure 5-10)

ITEM	PART NUMBER	DESCRIPTION
1	20903	Storage Compartment Cover Assy., complete
2	20928	Door, Storage Compartment
3	20927	Hinge, Storage Compartment
4	70030-06	Screw, 6-32 x 3/8, pan hd. (10)
5	20925	Nut Plate, Storage Compartment Hinge (2)
6	20929	Cover, Storage Compartment
7	20935	Bracket, Cable, Storage Compartment Door
8	70030-08	Screw, 6-32, x 1/2, pan hd. (2)
9	70450	Latch, Snapslide Fastener (2)
10	70451	Guide, Snapslide Fastener (2)
11	70452-05	Rivet, Snapslide Fastener (2)
12	70454	Spring Washer, Snapslide Fastener (2)
13	20907	Bracket Assy., PRGM Board Storage (3) (Includes items 14-17)
14	20926	Bracket, PRGM Board Storage (3)
15	20923	Insulation, PRGM Board Storage (3)
16	10724-04	Card Guide, Snap-in, 4-1/2" (6)
17	20967	Gasket, PRGM Board Bracket (6)
18	70029-05	Screw, 4-40 x 5/16, pan hd. (12)
19	70414-01	Screw Assy., Spring-Ejected (3) (Includes screw, spring, washer, and standoff.)



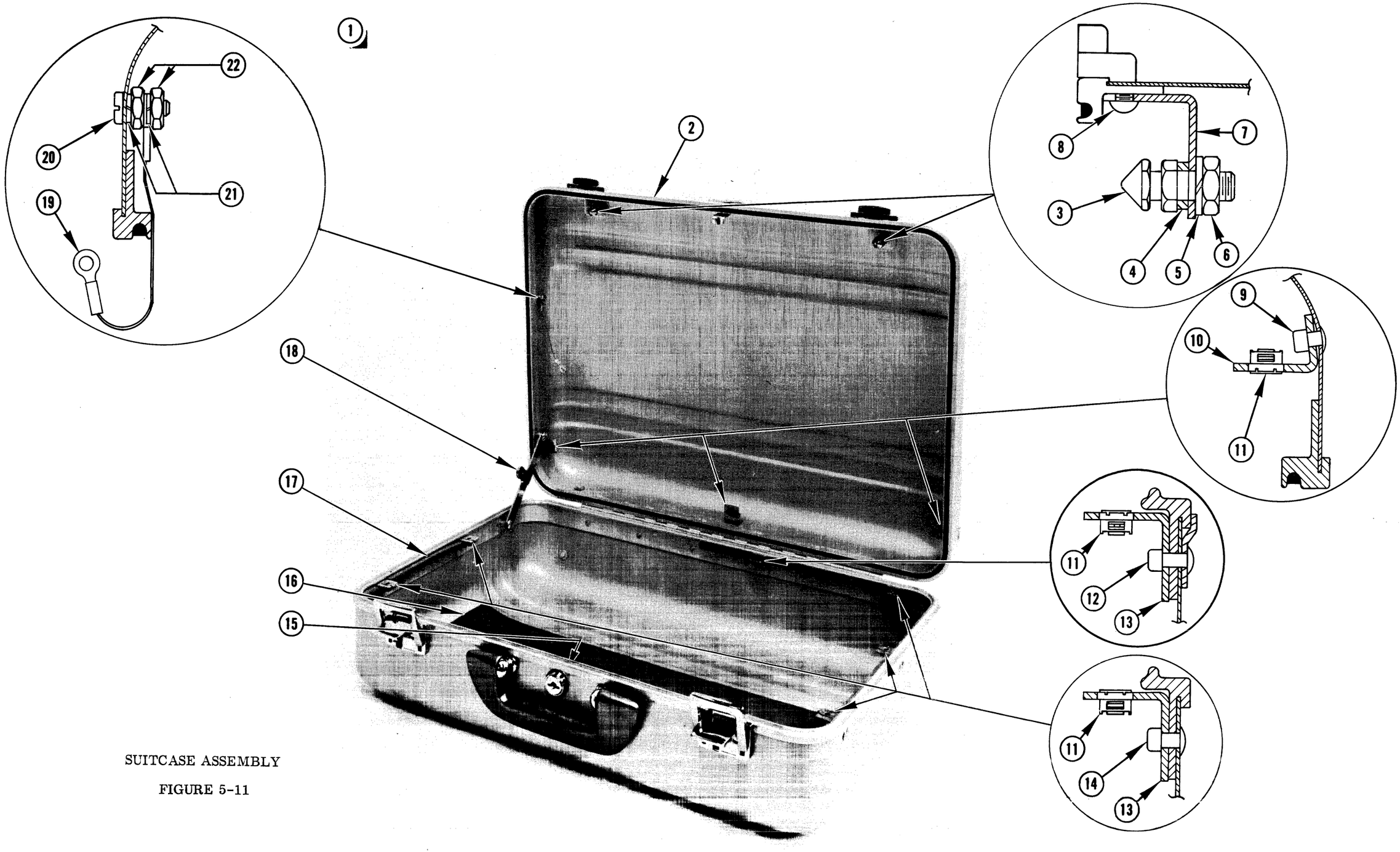
STORAGE COMPARTMENT
DOOR ASSEMBLY

FIGURE 5-10

SUITCASE ASSEMBLY

(Figure 5-11)

ITEM	PART NUMBER	DESCRIPTION
1	20902	Suitcase Assy., complete
2	20909	Suitcase
3	70453-05	Stud, Snapslide Fastener (2)
4	20937	Spacer (2)
5	70168-13	Lockwasher, 1/4" (2)
6	70455	Nut, hex, 1/4-28 (2)
7	20931	Bracket (2)
8	Not Available Separately	6-32 x 1/4 Phillips hd. screw (4) (Part of item #2.)
9	70412-02	Rivet (6)
10	20939	Bracket (3)
11	70411-01	Nut, Floating, 6-32 (9)
12	70412-04	Rivet (2)
13	20915	Bracket (6)
14	70412-03	Rivet (10)
15	20914	Bracket, Support (not visible)
16	20924	Insulation, Neoprene Sponge, 16-3/4 x 7-1/2 x .060"
17	20930-04	Gasket, Neoprene Sponge, 3/16 x 5/16 x 8-7/8" long (Cut as needed for shorter lengths.)
18	Not Available Separately	Cover Stop, (Part of item #2)
19	20946	Cable Assy.
20	70030-06	Screw, 6-32 x 3/8, Pan hd.
21	70168-06	Lockwasher, #6 (2)
22	70166-06	Nut, hex 6-32 (2)



SUITCASE ASSEMBLY

FIGURE 5-11

PROCESSOR LOGIC BOARD (PROC)

HARDWARE:

ITEM	PART NUMBER	DESCRIPTION
1	70175-09	Standoff, 1/4 dia x 1/8 high, 4-40 int thd (4)
2	70168-04	Lockwasher, #4 (4)
3	70029-04	Screw, 4-40 x 1/4 pan hd (4)
4	10757	Terminal, miniature feed-through (3)
5	10500	Terminal, miniature turret type (3)
6	10731-01	Connector, P7
7	21046-01	Cable assy, flat, 3.2" long, P2 & P3 (2)
8	21046-02	Cable assy, flat, 5.6" long, P6

INTEGRATED CIRCUITS:

LOCATION	PART NUMBER	DESCRIPTION
B144	10307	74H00 quad 2-input NAND
D20, D144	10135	7402 quad 2-input NOR
A20, E131	10136	7404 Hexinverter
A131, B131, F104	10324	74S04 Hexinverter
D131	10119	7408 quad 2-input AND
E6, E144	10302	7432 quad 2-input OR
D6	10146	7442 1-of-10 Decoder
B6, F131	10139	7474 dual D-type Flip-flop
D75, D90, E75, E90, F75, F90	10333	8214 dual 4-input Multiplexer, Tri-State
B33, B47, B61	10334	8599 64-bit RAM, Tri-state
F117	10152	9312 8-input Multiplexer
B20	10159	9601 one-shot
B104	10157	74157/9322 quad 2-input Multiplexer
B75, B90, D104	10335	74161/9316 synchronous 4-bit Counter
D117, E20, E33, E47, E61, E104, E117	10336	74174 hex D-type Flip-flop
D33, D47, D61	10337	74175 quad D-type Flip-flop
A30, A45, A59	10338	74181 ALU
A74, A143	10150	74195/9300 4-bit Shift Register
B117	21073	DMP-3 ROM

RESISTORS: (All 5%, 1/4 Watt)

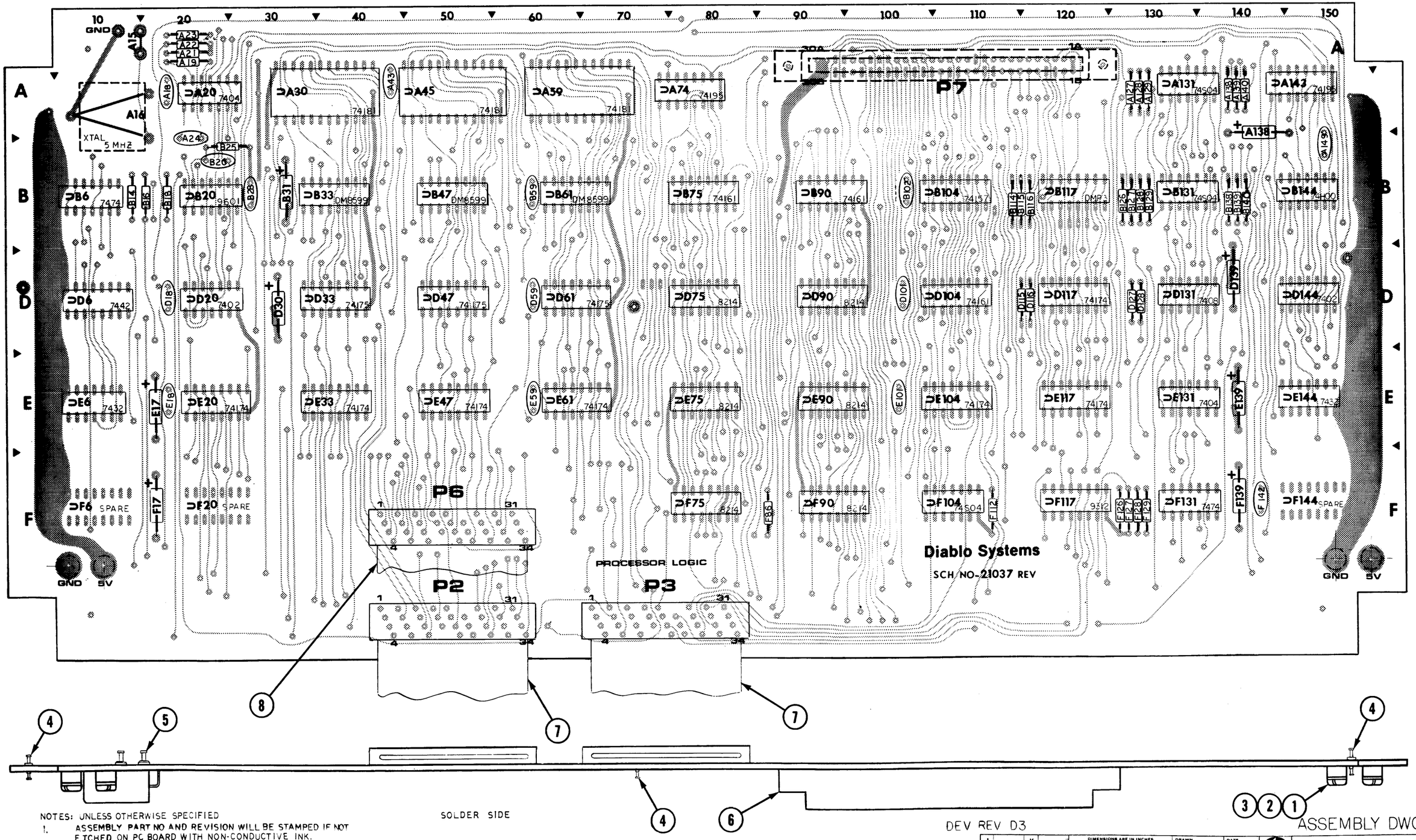
LOCATION	PART NUMBER	DESCRIPTION
A127, A128, A129, A138, A139, A140, B127, B128, B129, B138, B139, B140	10022-33	330Ω
B114, B115, B116, B126 D115, D116, D127, D128	10022-43	430Ω
F129	10022-62	620Ω
A19, A23, B14, B16, B18, F86, F112, F126, F127, F128	10023-10	1K
A21, A22	10023-18	1.8K
B25	10023-75	7.5K

CAPACITORS:

LOCATION	PART NUMBER	DESCRIPTION
B26	10061-10	10 pf, Mica, 500V
A24	10062-20	200 pf, Mica, 500V
A18, A43, A149, B28, B59, B102, D18, D59, D101, E18, E59, E101, F142	10094-10	.01μf, Ceramic, 25V
A138, B31, D30, D139, E17, E139, F17, F139	10077-39	39μf, Tantalum electrolytic, 10V

MISCELLANEOUS:

LOCATION	PART NUMBER	DESCRIPTION
A16	10449	Crystal, 5.000 MHz



NOTES: UNLESS OTHERWISE SPECIFIED

1. ASSEMBLY PART NO AND REVISION WILL BE STAMPED IF NOT ETCHED ON PC BOARD WITH NON-CONDUCTIVE INK.
2. MASTER ARTWORK AND FABRICATION PART NOS ARE 21036
3. SCHEMATIC NUMBER IS 21037

PROCESSOR LOGIC BOARD

FIGURE 5-12

DEV REV D3

ASSEMBLY DWG.

J K G H E F C D A B	DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED TOLERANCES ARE LINEAR ± ANGULAR ± MATERIAL HEAT TREAT FINISH	DRAWN BEDEL	DATE 11-18-72	Diablo Systems Incorporated Hayward, California 94545	
		CHECKED		PROCESSOR LOGIC PROGRAMMABLE TESTER	
		ENGR P Sumner		SCALE 2=1	SHEET 12 TOT SH 12
REVISIONS FIRST USED 20900		MFG		PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED	SIZE D 21037

I/O LOGIC BOARD (I/O)

HARDWARE:

ITEM	PART NUMBER	DESCRIPTION
1	70175-09	Standoff, 1/4 dia x 1/8 high, 4-40 int thd (4)
2	70168-04	Lockwasher, #4 (4)
3	70029-04	Screw, 4-40 x 1/4 pan hd (4)
4	10757	Terminal, miniature feed-through (3)
5	10641	Post Connector (170)
6	16577-02	Standoff, 7/16 high, 2-56 int thd (3)

INTEGRATED CIRCUITS:

LOCATION	PART NUMBER	DESCRIPTION
E90, E104, E117, F90, F104, F117	10132	858 DTL quad 2-input NAND
A60, A146, D6, F47	10134	7400 quad 2-input NAND
E6	10135	7402 quad 2-input NOR
B60, B144, D90, D104, D117, D131, E131	10136	7404 Hexinverter
A74	10125	7420 dual 4-input NAND
B6	10344	74S20 dual 4-input NAND
F6, F131	10302	7432 quad 2-input OR
B104, B117	10139	7474 dual D-type Flip-flop
B90	10349	74S74 dual D-type Flip-flop
B75	10138	7476 dual J-K Flip-flop
D60, D75, E60, E75, F60, F75	10333	8214 dual 4-input Multiplexer, Tri-state
B131	10153	9314 4-bit Dual Mode Latch
A6	10156	9321 dual 1-of-4 Decoder
A20, A33, A47	10339	9334 8-bit Addressable Latch
A133, D144	10340	9600 One-shot
E20, F20	10336	74174 hex D-type Flip-flop
B20, B33, B47, D20, D33, D47, E33, E47, F33	10150	74195/9300 4-bit Shift Register

RESISTORS: (All 5% 1/4 Watt unless otherwise specified)

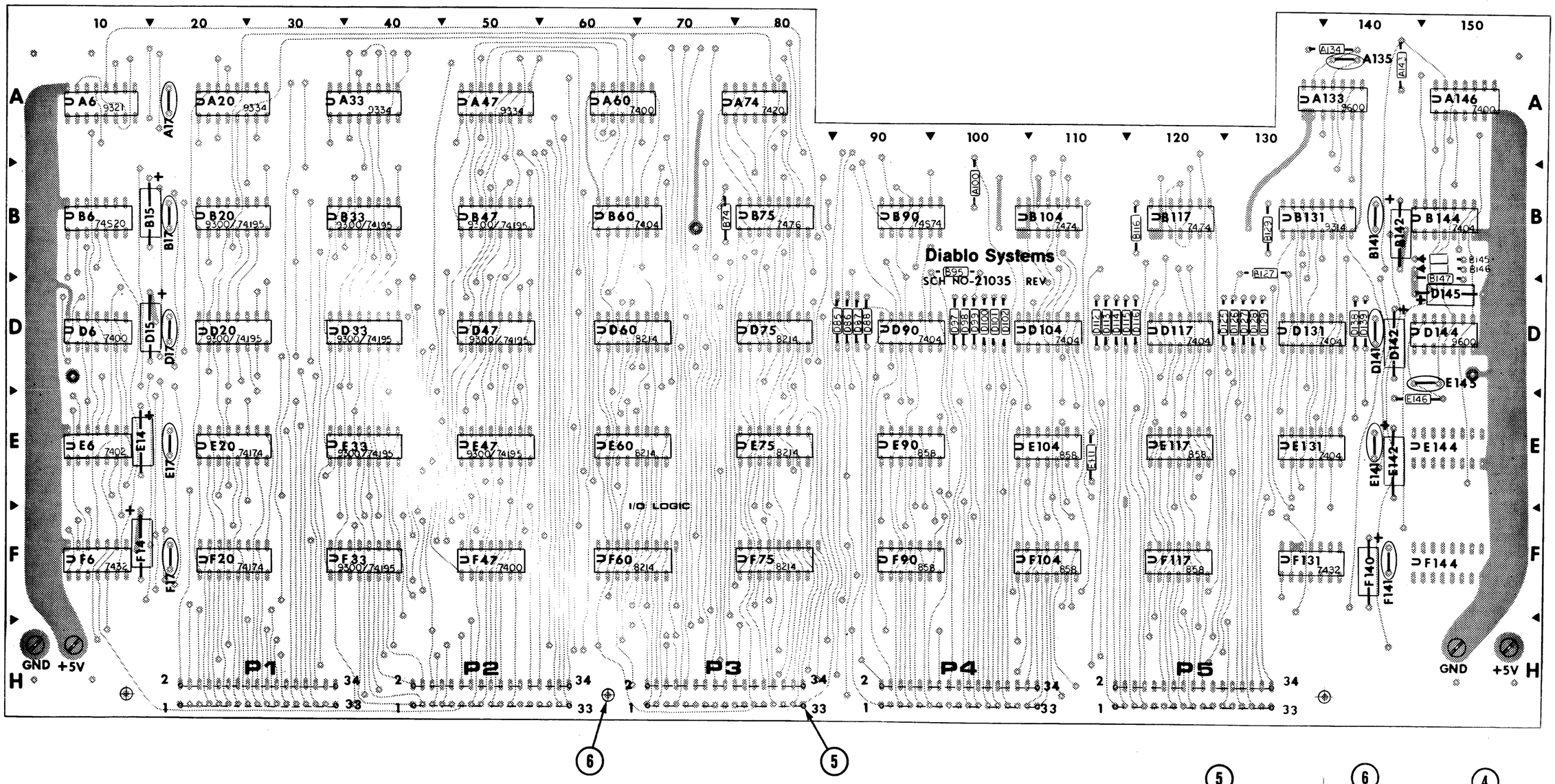
LOCATION	PART NUMBER	DESCRIPTION
D99, D129	10021-82	82 Ω
B95, B127, B147, D85-88, D97, D98, D100-102, D112-116, D125-128, D138, D139	10022-15	150 Ω
B74, B116, B129, E111	10023-10	1K
E146	10023-51	5.1K
A134	10004-23	16.9K, 1% 1/8 Watt
A100, A143	10022-51	510 Ω

CAPACITORS:

LOCATION	PART NUMBER	DESCRIPTION
E145	10061-10	10 pf, 500V
A135	10062-15	150 pf, 5%, 500V
D145	10077-10	10 μf, 20V
B15, B142, D15, D142, E14, E142, F14, F140	10077-39	39 μf, 10V
A17, B17, B141, D17, D141, E17, E141, F17, F141	10094-10	.01 μf, Ceramic, 25V

MISCELLANEOUS:

LOCATION	PART NUMBER	DESCRIPTION
B145, B146	10101	A14F Diode



I/O LOGIC BOARD

FIGURE 5-13

DEV REV D4 PROGRAMMABLE TESTER ASSEMBLY DWG.

DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED TOLERANCES ARE	DRAWN K Gustafson DATE 4-N-72
LINEAR ± ANGULAR ±	CHECKED
MATERIAL	ENGR
HEAT TREAT	MFG
REVISIONS	FINISH
FIRST USED 20900	PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED

Diablo Systems Incorporated
Hayward, California 94545

I/O LOGIC BOARD ASSEMBLY

SCALE 2 To 1 SHEET 11 TOT SH 11

SIZE D 21035

HARDWARE:

ITEM	PART NUMBER	DESCRIPTION
1	70175-09	Standoff, 1/4 dia x 1/8 high, 4-40 int thd (2)
2	70168-04	Lockwasher, #4 (2)
3	70029-04	Screw, 4-40 x 1/4 pan hd (2)
4	10641	Post Connector (68)
5	70410-11	Standoff, 1/4 dia x 11/16 high, 6-32 int thd (4)
6	20920	Bracket
7	10667-02	Connector (P8), female, Winchester MRAC 50 SJ6
8	10583-02	Socket contact (50)
9	Not Available Separately	Guide pin, connector (P8) (Part of item #7)

INTEGRATED CIRCUITS:

LOCATION	PART NUMBER	DESCRIPTION
B74	10132	858 DTL quad 2-input NAND
B142	10134	7400 quad 2-input NAND
B132	101399	7474 dual D-type flip-flop

RESISTORS: (All 5%, 1/4 Watt)

LOCATION	PART NUMBER	DESCRIPTION
A78, A82	10021-10	10Ω
B122	10022-33	330Ω
A83	10022-50	500Ω
B69, B78	10022-51	510Ω
B71, B76, B123, B128, B129, B130 A77	10023-10	1K
B117	10023-33	3.3K
B116	10025-47	470K

CAPACITORS:

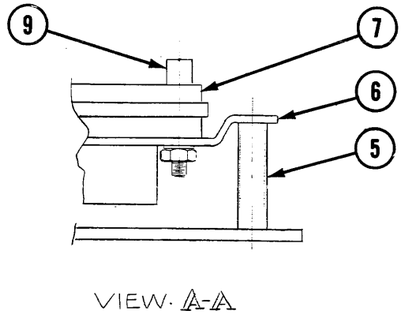
LOCATION	PART NUMBER	DESCRIPTION
B114, B112	10061-20	20pf, 500V
B124	10070-10	.001μf, 200V
B72	10094-10	.01μf, Ceramic, 25V
A79, A81, B82	10077-39	39μf, 10V

MISCELLANEOUS:

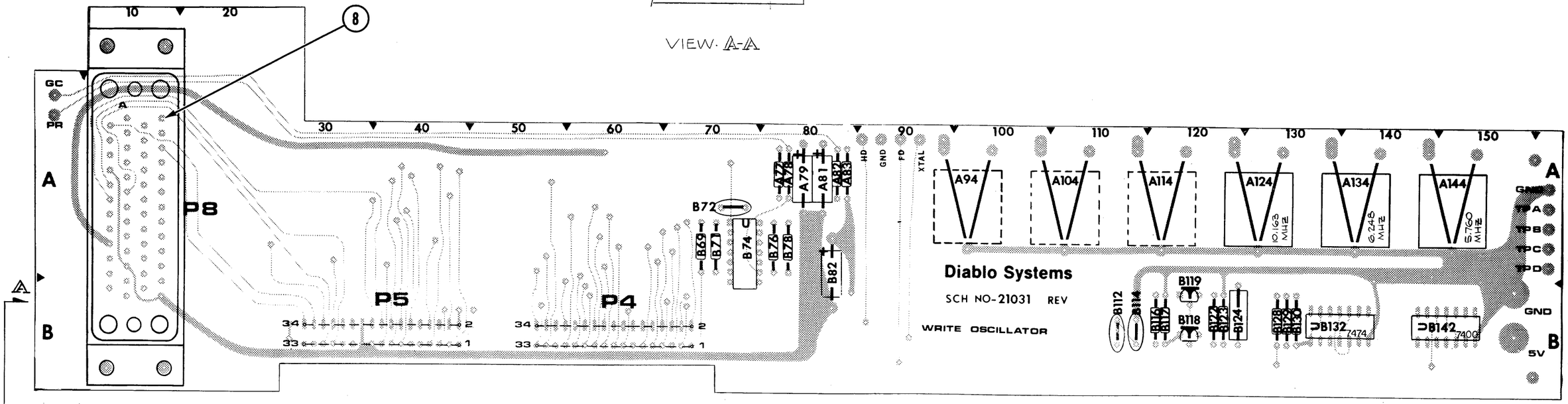
LOCATION	PART NUMBER	DESCRIPTION
B118	10327	Transistor, MPS2369
B119	10328	Transistor, MPS3640
A144	10450	Crystal, 5.760 MHz
A134	10202-06	Crystal, 6.248 MHz
A124	10451	Crystal, 10.163 MHz

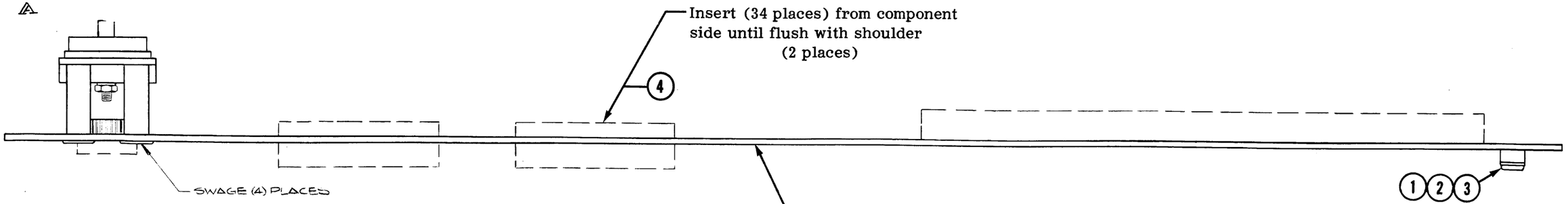
WRITE OSCILLATOR BOARD

FIGURE 5-14



VIEW A-A





NOTES:
UNLESS OTHERWISE SPECIFIED
1) ALL RESISTORS 1/4 W.
2) ALL FILTER CAP. 39 μf @ 10V.

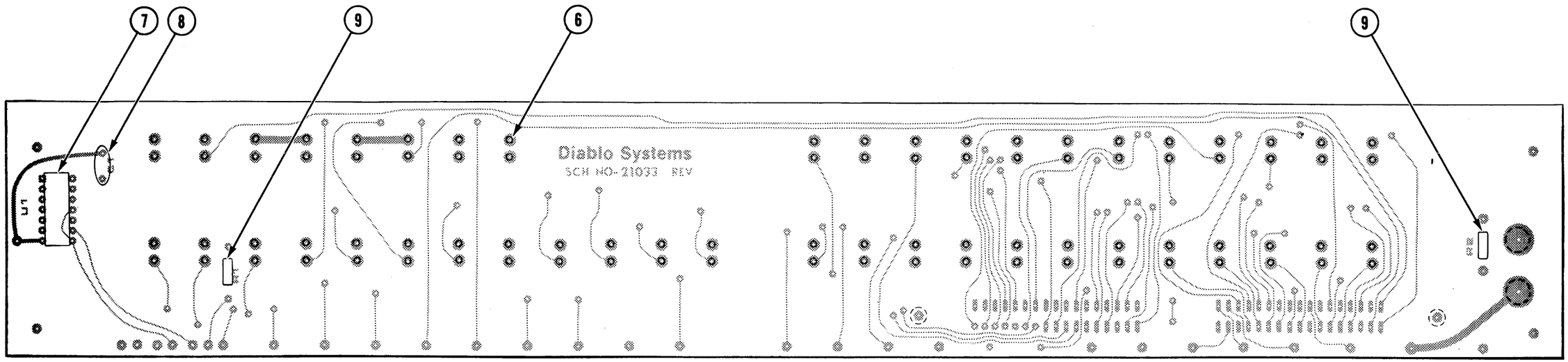
DEV REV DS PROGRAMMABLE TESTER ASSEMBLY DWG

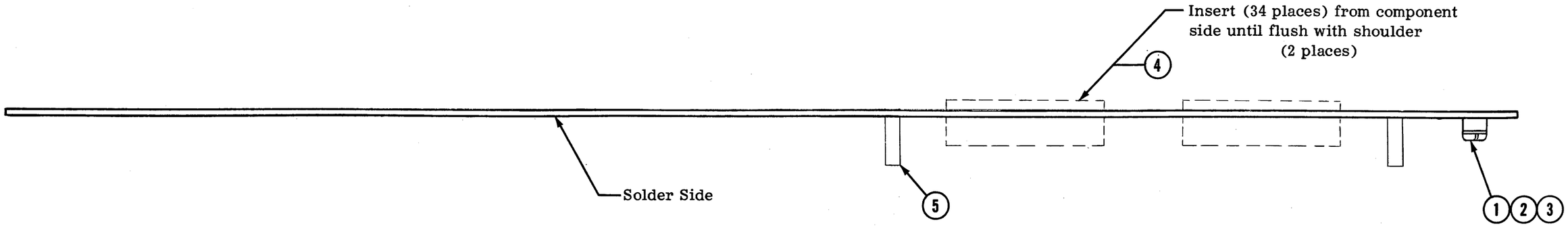
J K G H E F C D A B	DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED TOLERANCES ARE LINEAR ANGULAR	DRAWN	DATE 8 Nov. 72	Diablo Systems Incorporated Hayward, California 94545	
		CHECKED		WRITE OSCILLATOR BOARD	
	MATERIAL	ENGR R Swan	-/5/73	ASSY	
	HEAT TREAT	MFG		SCALE	SHEET 4 TOT SH 4
REVISIONS FIRST USED 20900	FINISH	PROPRIETARY INFORMATION. UNAUTHORIZED DISCLOSURE OR USE PROHIBITED		SIZE D	21031

FORM 100-5-3-70

DISPLAY BOARD (DISP)

ITEM	PART NUMBER	DESCRIPTION
1	70175-09	Standoff, 1/4 dia x 1/8 high, 4-40 int thd (2)
2	70168-04	Lockwasher, #4 (2)
3	70029-04	Screw, 4-40 x 1/4 pan hd (2)
4	10641	Post connector (68)
5	16577-02	Standoff, 7/16 high, 2-56 int thd (2)
6	10592	Jack, closed entry (88)
7	10322	Integrated circuit (U1), 836 hexinverter
8	10095-01	Capacitor (C1), .1μf, 10V
9	10023-10	Resistor (R1, R2), 1K, 5%, 1/4 Watt





DISPLAY BOARD

FIGURE 5-15

DEV REV D3 PROGRAMMABLE TESTER ASSEMBLY DWG

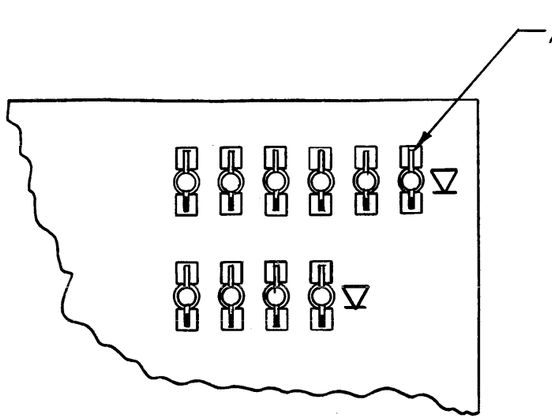
J K / G H / F F / C D / A B	DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED TOLERANCES ARE: LINEAR ± ANGULAR ± MATERIAL HEAT TREAT	DRAWN BEDEL	DATE 11-8-72	Diablo Systems Incorporated Hayward, California 94545	
		CHECKED		ASSEMBLY, DISPLAY BOARD	
		ENGR J. Smith	1/5/73		
		MFG		SCALE	SHEET 4 / REV BH 4
REVISIONS					
FIRST USED 20900	FIN. SH	PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED		SIZE D	21033

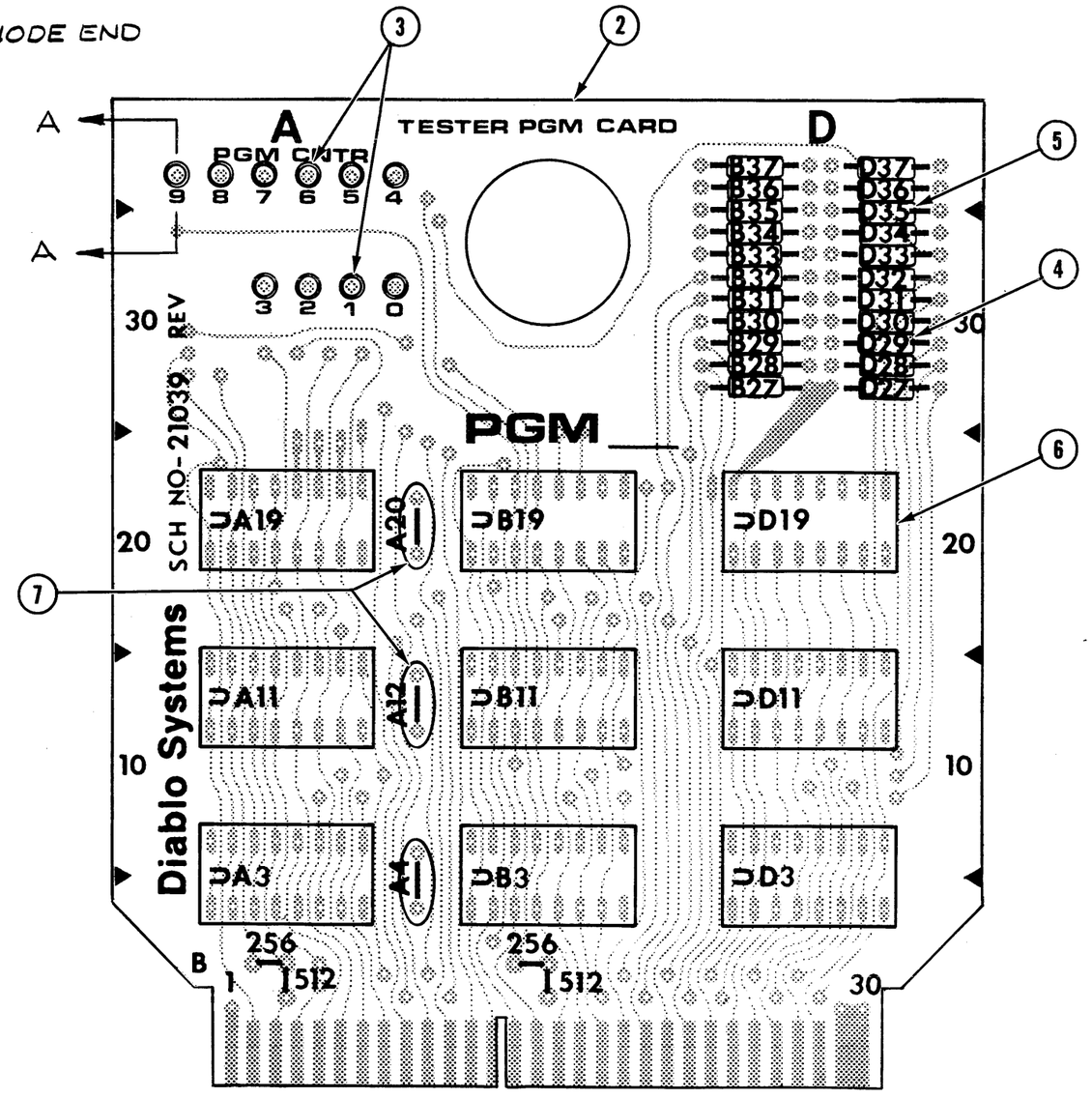
FORM 100.9.2.70

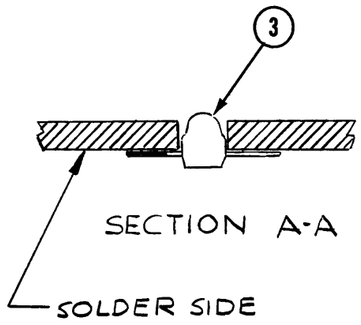
PROGRAM BOARD (PRGM)

ITEM	PART NUMBER	DESCRIPTION
1	21039	PRGM board, complete, less ROMs
2	21038	Circuit board, less components
3	10733-01	Indicator (LED), type MV-55 (10)
4	10022-51	Resistor (B27-B32, D27-D32), 510Ω, 5%, 1/4 Watt (12)
5	10023-33	Resistor (B33-B37, D33-D37), 3.3K, 5%, 1/4 Watt (10)
6	10786	IC socket (9)
7	10095-01	Capacitor (A4, A12, A20), .1μf, 10V (3)

FOR PART NUMBERS OF ROMS
SEE APPLICABLE PROGRAM MANUAL







PROGRAM BOARD

FIGURE 5-16

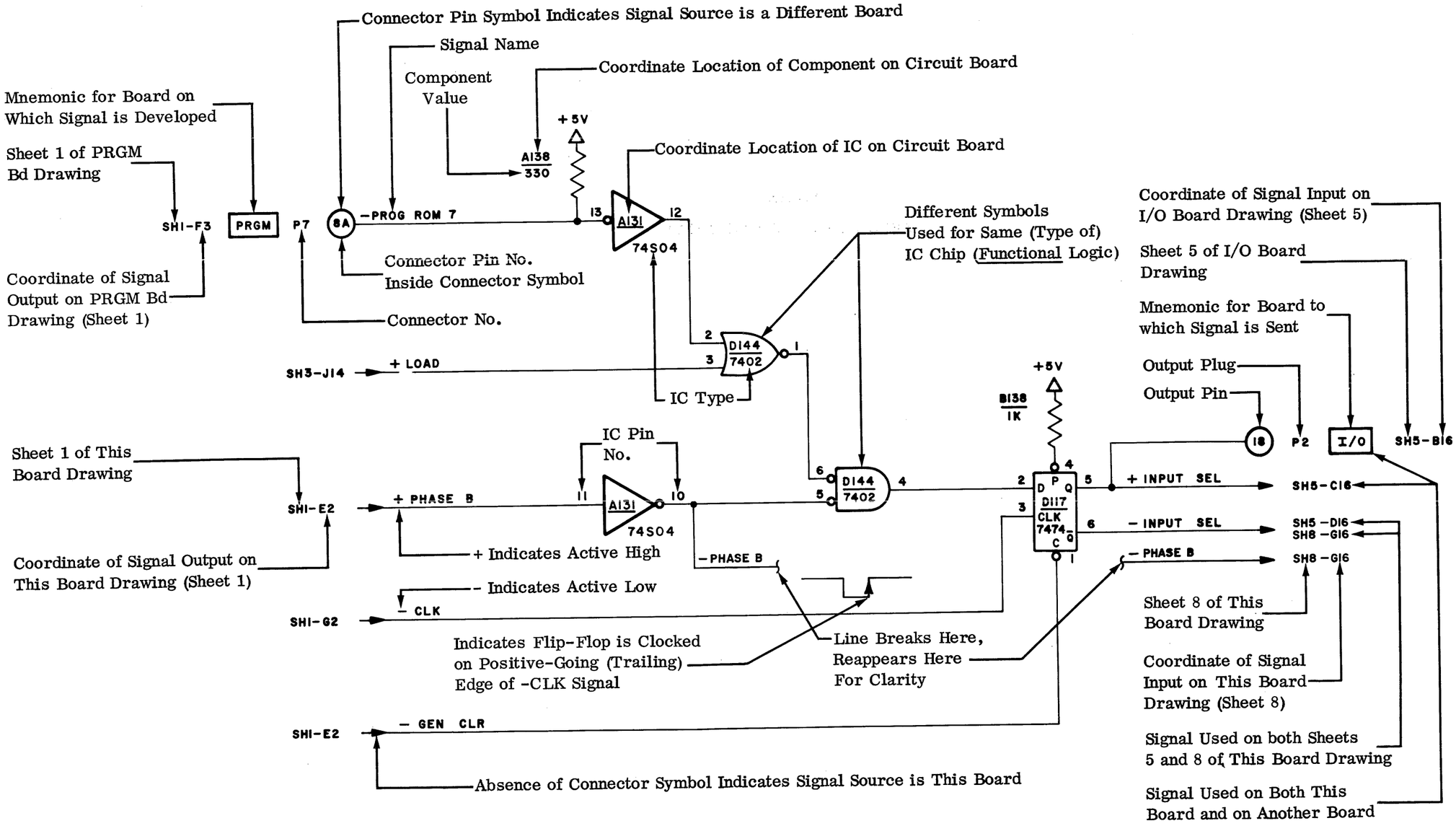
DEV REV D3 PROGRAMMABLE TESTER ASSEMBLY DWG

J		K		DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED TOLERANCES ARE	DRAWN Green	DATE 11-16-72	Diablo Systems Incorporated, Hayward, California 94545
G		H			CHECKED		ASSEMBLY
E		F		LINEAR ± ANGULAR ±	ENGR R Swenson	7/5/73	PGM BOARD
C		D		MATERIAL	MFG		SCALE 2:1 SHEET 4 TOT SH 4
A		B		HEAT TREAT	PROPRIETARY INFORMATION. UNAUTHORIZED DISCLOSURE OR USE PROHIBITED.		SIZE C 21039
REVISIONS				FINISH			
FIRST USED							

FORM 100-S 3-70

Section 6

LOGIC DIAGRAMS & SCHEMATICS



LOGIC DIAGRAM NOTATION

FIGURE 6-1

Section 6

LOGIC DIAGRAMS & SCHEMATICS

6.1 LOGIC DIAGRAM NOTATION

The various types of notation used on the logic diagrams are illustrated in Figure 6-1. All of the information contained in the logic diagrams, as well as the special diagramming techniques used, are explained in sample form.

6.2 INTEGRATED CIRCUITS

Figure 6-2 lists all of the integrated circuits used in the Model 500, along with Diablo part numbers and a "where used" list. The following twelve pages contain logic symbols, truth tables, and other information pertaining to the individual chips.

6.3 DIAGRAMS & SCHEMATICS

The logic diagrams and schematics will be found at the end of this manual, following the integrated circuit section, which ends on page 6-13. The diagrams are arranged in the following sequence.

Processor Logic board (PROC), 7 pages
I/O Logic board (I/O), 7 pages
Write Oscillator board (WOSC), 1 page
Display board (DISP), 2 pages
Program board (PRGM), 2 pages
Power Supply & DC Power Distribution, 1 page

PC board assembly drawings will be found at the end of Section 5.

TYPE	DESCRIPTION	WHERE USED			DIABLO PART NUMBER
		PROC	I/O	WOSC	
858	DTL Quad 2-input NAND Power Gate, O.C.		6	1	10132
7400	TTL Quad 2-input NAND		4	1	10134
74H00	TTL Quad 2-input NAND Hi-speed	1			10307
7402	TTL Quad 2-input NOR	2	1		10135
836	DTL Hexinverter	(1 used on DISP bd)			10322
7404	TTL Hexinverter	2	7		10136
74S04	TTL Hexinverter, Schottky	3			10324
7408	TTL Quad 2-input AND	1			10119
7420	TTL Dual 4-input NAND		1		10125
74S20	TTL Dual 4-input NAND, Schottky		1		10344
7432	TTL Quad 2-input OR	2	2		10302
7442	TTL 1-of-10 Decoder	1			10146
7474	TTL Dual D F/F	2	3	1	10139
7476	TTL Dual J-K Master-Slave F/F		1		10138
74157/ 9322	TTL Quad 2-input Multiplexer	1			10157
74161/ 9316	TTL 4-bit Synchronous Binary Counter	3			10335
74174	TTL Hex D Latch	7	2		10336
74175	TTL Quad D Latch	3			10337
74181	TTL Arithmetic/Logical Unit	3			10338
74195/ 9300	TTL 4-bit Shift Register	2	9		10150
8214	TTL Dual 4-input Multiplexer, Tri-state	6	6		10333
8599	TTL 16 x 4-bit RAM, Tri-state	3			10334
9312	TTL 8-input Multiplexer	1			10152
9314	TTL 4-bit Dual-Mode Latch		1		10153
9321	TTL Dual 1-of-4 Decoder		1		10156
9334	TTL 8-bit Addressable Latch		3		10339
9600	TTL Retriggerable O/S		2		10340
9601	TTL Retriggerable O/S	1			10159
DMP3	32 x 8-bit Read Only Memory	1			21073

PROGRAM BOARD

Typical Unprogrammed PROMs

(Refer to individual Program Manual for Diablo part numbers.)

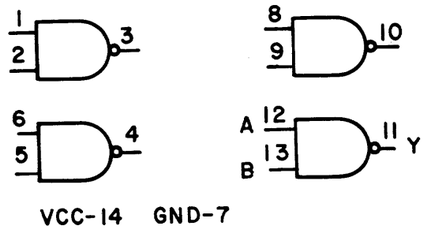
MM 6300/ HPROM-1024A	256 x 4-Bit Programmable Read Only Memory
MM 6305 HPROM-2048A	512 x 4-Bit Programmable Read Only Memory

LIST OF INTEGRATED CIRCUITS

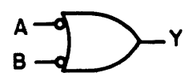
FIGURE 6-2

DTL Quad 2-input NAND Power Gate, O.C. — Part No. 10132 — Type 858

Logic Symbol



Alternate Symbol



Truth Table

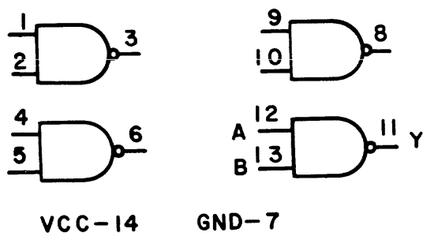
A	B	Y
L	L	H
H	L	H
L	H	H
H	H	L

TTL Quad 2-input NAND — Part No. 10134 — Type 7400

TTL Quad 2-input NAND, High Speed — Part No. 10307 — Type 74H00

The 74H00 has a slightly shorter propagation delay than the 7400, especially in the low-to-high transition of the output. It also has higher output current.

Logic Symbol



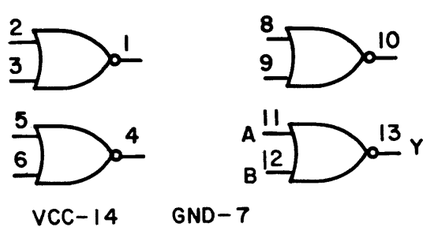
Alternate Symbol

Truth Table

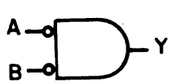
A	B	Y
L	L	H
H	L	H
L	H	H
H	H	L

TTL Quad 2-input NOR — Part No. 10135 — Type 7402

Logic Symbol



Alternate Symbol



Truth Table

A	B	Y
L	L	H
H	L	L
L	H	L
H	H	L

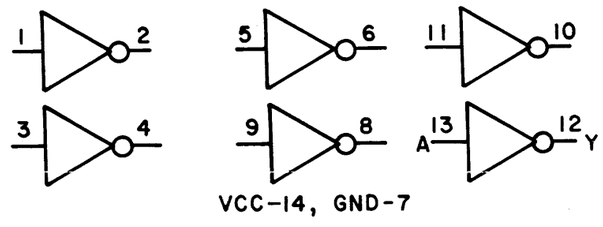
DTL Hexinverter — Part No. 10322 — Type 836

TTL Hexinverter — Part No. 10136 — Type 7404

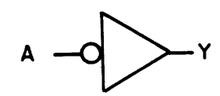
TTL Hexinverter, Schottky — Part No. 10324 — Type 74S04

The 74S04 has propagation delays of 1/2 to 1/4 that of the 7404

Logic Symbol

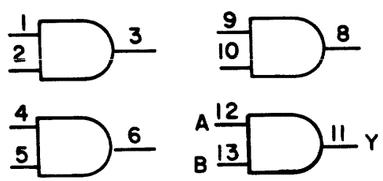


Alternate Symbol

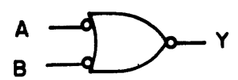


TTL QUAD 2-input AND — Part No. 10119 — Type 7408

Logic Symbol



Alternate Symbol



Truth Table

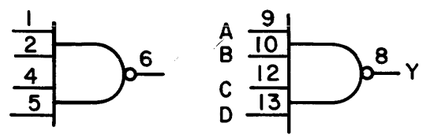
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

TTL Dual 4-input NAND — Part No. 10125 — Type 7420

TTL Dual 4-input NAND, Schottky — Part No. 10344 — Type 74S20

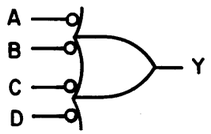
The 74S20 has a propagation delay of 1/2 to 1/4 that of the 7420. The 74S20 has a more nearly symmetrical propagation delay in both directions.

Logic Symbol



VCC-14, GND-7 Pins 3 & 11 not used

Alternate Symbol

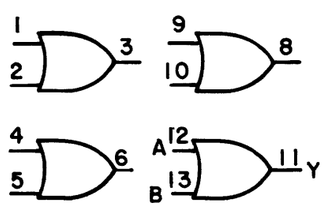


Truth Table

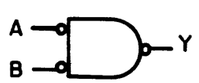
A	B	C	D	Y
L	L	L	L	H
L	L	L	H	H
L	L	H	L	H
L	L	H	H	H
L	H	L	L	H
L	H	L	H	H
L	H	H	L	H
L	H	H	H	H
H	L	L	L	H
H	L	L	H	H
H	L	H	L	H
H	L	H	H	H
H	H	L	L	H
H	H	L	H	H
H	H	H	L	H
H	H	H	H	L

TTL Quad 2-input OR — Part No. 10302 — Type 7432

Logic Symbol



Alternate Symbol

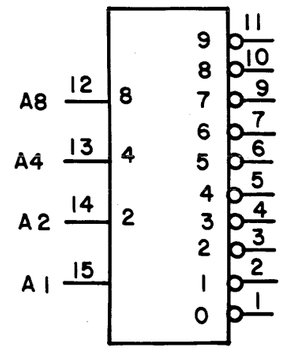


Truth Table

A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

TTL BCD-To-Decimal Decoder — Part No. 10146 — Type 7442

Logic Symbol



VCC = 16 GND = 8

A1-A8 = Binary address input
0-9 = Decimal output

Loading:

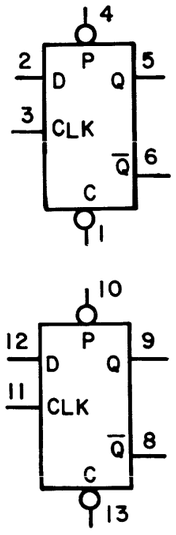
Inputs 1 Unit Load
Outputs 10 Unit Loads

Truth Table

A_8	A_4	A_2	A_1	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	1	1	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1
0	1	1	1	1	1	1	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0
1	0	1	0	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

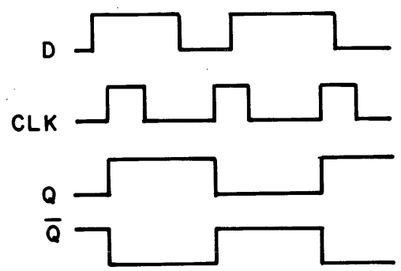
The 7474 contains two D-type edge-triggered flip-flops with direct preset and clear inputs. A low level on the preset or clear input will set or reset the flip-flop, respectively, regardless of other input conditions. When both the preset and clear are high, the logic level on D is transferred to Q on the positive-going edge of the clock.

Logic Symbol



VCC-14 GND-7

Timing Waveforms



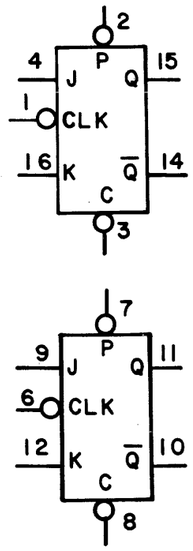
P = Preset input
D = Data input
CLK = Clock input
C = Clear input
Q, $\overline{Q}$ = Data outputs

Loading:

C, CLK	2 Unit Loads
D, P	1 Unit Load
Outputs	10 Unit Loads

Note that VCC and GND connections to this device are non-standard.

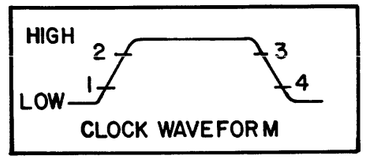
Logic Symbol



NOTE

VCC-5 GND-13

Timing Waveform



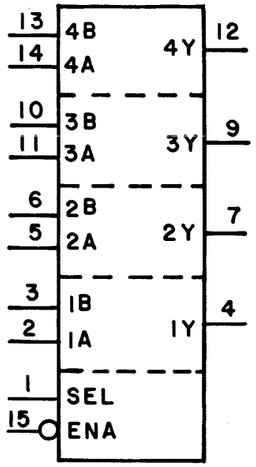
1. Isolate slave from master
2. Enable entry of data from J and K inputs to master
3. Disable entry of data from J and K inputs
4. Transfer information from master to slave

P = Preset input
J, K = Data inputs
CLK = CLock input
C = CLear inputs
Q, $\overline{Q}$ = Data outputs

Loading:

P, C, CLK	2 Unit Loads
J, K	1 Unit Load
Outputs	10 Unit Loads

Logic Symbol



VCC-16, GND-8

Loading:

Inputs	1 Unit Load
Outputs	10 Unit Loads

Truth Table

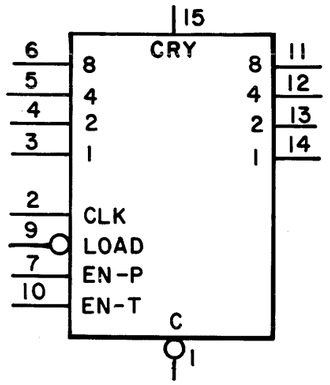
INPUTS				OUTPUT
ENA	SELECT	A	B	Y
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = high level, L = low level,
X = irrelevant

1A – 4A = No 1 data inputs
1B – 4B = No 2 data inputs
SEL = Select No. 1 or No. 2 inputs
ENA = Low active Enable inputs
1Y – 4Y = Data outputs

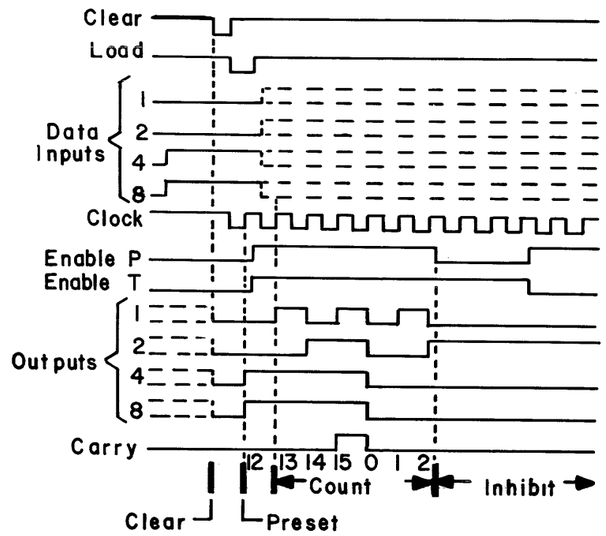
All flip-flops in this chip are clocked simultaneously, so all output changes occur simultaneously. A low on the Clear input overrides all other inputs and drives all outputs low.

Logic Symbol



VCC-16 GND-8

Timing Waveforms



1,2,4,8 = Data parallel inputs
CLK = Clock input, clocks both loading and counting.
LOAD = Low active parallel-load input
EN-P, EN-T = Load and count enable
C = Clear input
CRY = Carry output
1,2,4,8 = Parallel data outputs

1. Clear outputs to zero
2. Preset to binary twelve
3. Count to thirteen, fourteen, fifteen, zero, one, and two.
4. Inhibit

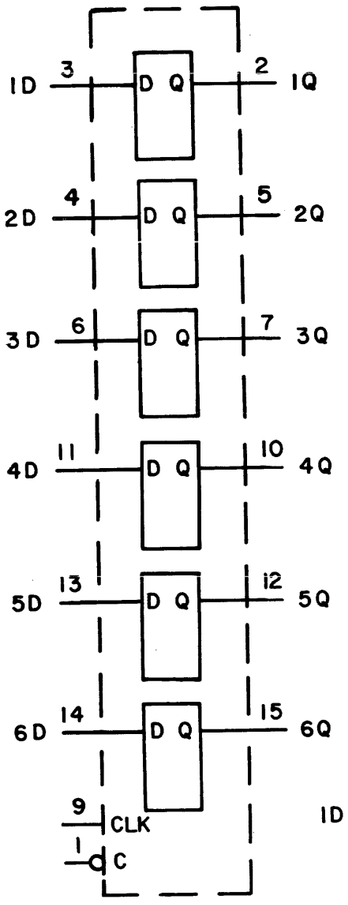
Loading:

CLK, EN-T	2 Unit Loads
All other inputs	1 Unit Load
Outputs	10 Unit Loads

TTL Hex D Latch — Part No. 10336 — Type 74174

All flip-flops in this chip are clocked or cleared simultaneously. A low on the clear input overrides all other inputs.

Logic Symbol



1D – 6D = Data inputs
CLK = Clock input
C = Clear
1Q – 6Q = Data outputs

VCC-16, GND-8

Truth Table
(Each Flip-flop)

INPUTS			OUTPUT
C	CLK	D	Q
L	X	X	H
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

H = High level
L = Low level
X = Irrelevant
↑ = Transition from low to high level
Q_0 = The level of Q before the indicated input conditions were established.

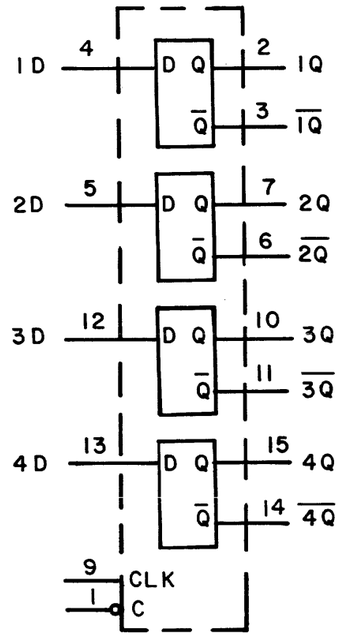
Loading:

Inputs	1 Unit Load
Outputs	10 Unit Loads

TTL Quad D Latch — Part No. 10337 — Type 74175

All flip-flops in this chip are clocked or cleared simultaneously. A low on the clear input overrides all other inputs.

Logic Symbol



1D – 4D = Data inputs
CLK = Clock input
C = Clear input
1Q – 4Q, 1Q̄ – 4Q̄ = Data outputs

VCC-16, GND-8

Truth Table
(Each Flip-flop)

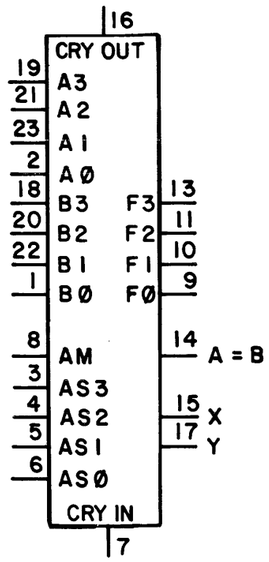
INPUTS			OUTPUTS	
C	CLK	D	Q	Q̄
L	X	X	H	L
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\bar{Q}_0$

H = High level
L = Low level
X = Irrelevant
↑ = Transition from low to high level
Q_0 = The level of Q before the indicated input conditions were established.

Loading:

Inputs	1 Unit Load
Outputs	10 Unit Loads

Logic Symbol



VCC-24, GND-12

Function Tables

SELECTION A S3	A S2	A S1	A S0	LOW = ACTIVE DATA: AM = H LOGIC FUNCTIONS	AM = L : ARITHMETIC OPERATIONS: CRY IN = 0 = L	CRY IN = 1 = H
L	L	L	L	F = $\overline{A}$	F = A MINUS 1	F = A
L	L	L	H	F = $\overline{AB}$	F = AB MINUS 1	F = AB
L	L	H	L	F = $\overline{A}$ + B	F = A$\overline{B}$ MINUS 1	F = A$\overline{B}$
L	L	H	H	F = 1	F = MINUS 1 (2's COMP)	F = ZERO
L	H	L	L	F = $\overline{A + B}$	F = A PLUS (A + $\overline{B}$)	F = A PLUS (A + $\overline{B}$) PLUS 1
L	H	L	H	F = $\overline{B}$	F = AB PLUS (A + $\overline{B}$)	F = AB PLUS (A + $\overline{B}$) PLUS 1
L	H	H	L	F = A⊕B	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	F = A + $\overline{B}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
H	L	L	L	F = $\overline{A}$B	F = A PLUS (A + B)	F = A PLUS (A + B) PLUS 1
H	L	L	H	F = A⊕B	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = A$\overline{B}$ PLUS (A + B)	F = A$\overline{B}$ PLUS (A + B) PLUS 1
H	L	H	H	F = A + B	F = A + B	F = (A + B) PLUS 1
H	H	L	L	F = 0	F = A PLUS A*	F = A PLUS A PLUS 1
H	H	L	H	F = A$\overline{B}$	F = AB PLUS A	F = AB PLUS A PLUS 1
H	H	H	L	F = AB	F = A$\overline{B}$ PLUS A	F = A$\overline{B}$ PLUS A PLUS 1
H	H	H	H	F = A	F = A	F = A PLUS 1

SELECTION A S3	A S2	A S1	A S0	HIGH = ACTIVE DATA: AM = H LOGIC FUNCTIONS	AM = L : ARITHMETIC OPERATIONS: $\overline{\text{CRY IN}}$ = 0 = H	$\overline{\text{CRY IN}}$ = 1 = L
L	L	L	L	F = $\overline{A}$	F = A	F = A PLUS 1
L	L	L	H	F = $\overline{A + B}$	F = A + B	F = (A + B) PLUS 1
L	L	H	L	F = $\overline{AB}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
L	L	H	H	F = 0	F = MINUS 1 (2's COMP)	F = ZERO
L	H	L	L	F = $\overline{AB}$	F = A PLUS A$\overline{B}$	F = A PLUS A$\overline{B}$ PLUS 1
L	H	L	H	F = $\overline{B}$	F = (A + B) PLUS A$\overline{B}$	F = (A + B) PLUS A$\overline{B}$ PLUS 1
L	H	H	L	F = A⊕B	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	F = A$\overline{B}$	F = A$\overline{B}$ MINUS 1	F = A$\overline{B}$
H	L	L	L	F = $\overline{A}$ + B	F = A PLUS AB	F = A PLUS AB PLUS 1
H	L	L	H	F = $\overline{A}$⊕$\overline{B}$	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = (A + $\overline{B}$) PLUS AB	F = (A + $\overline{B}$) PLUS AB PLUS 1
H	L	H	H	F = AB	F = AB MINUS 1	F = AB
H	H	L	L	F = 1	F = A PLUS A*	F = A PLUS A PLUS 1
H	H	L	H	F = A + $\overline{B}$	F = (A + B) PLUS A	F = (A + B) PLUS A PLUS 1
H	H	H	L	F = A + B	F = (A + $\overline{B}$) PLUS A	F = (A + $\overline{B}$) PLUS A PLUS 1
H	H	H	H	F = A	F = A MINUS 1	F = A

*Each bit is shifted to the next more significant position.

AM = ALU Mode — High = Logic; Low = Arithmetic

ASØ-AS3 = ALU Select Inputs

AØ -A3 = A-Factor Inputs

BØ -B3 = B-Factor Inputs

CRY IN = Carry Input

CRY OUT = Carry Output

FØ -F3 = Data Outputs

A = B = High If A = B; Low If A ≠ B

X & Y = Used Only In Conjunction with 74182 Look-Ahead Carry Generator

Loading:

Inputs

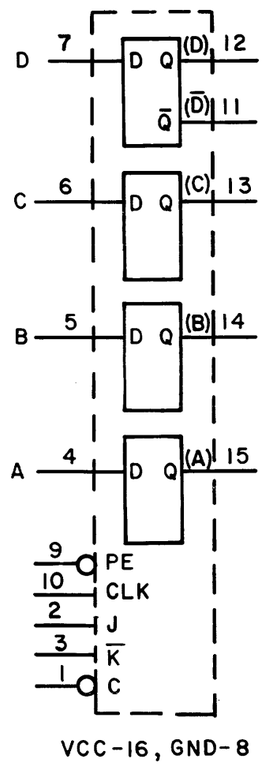
Mode	1 Unit Load
Any A or B	3 Unit Loads
Any AS	4 Unit Loads
Carry In	5 Unit Loads

Outputs

ALL	10 Unit Loads

Data can be loaded into this register either serially or in parallel. When Parallel Enable (PE) is low, parallel data is loaded into the flip-flops on every positive-going clock. When PE is high, data is shifted from the J and $\overline{K}$ inputs to flip-flop A, and from A to B, B to C, and C to D, at each positive-going clock transition. A low on the Clear (C) input overrides all other controls.

Logic Symbol



VCC-16, GND-8

Truth Table

Inputs at t_n J	K	Outputs at $t_n + 1$ QA	QB	QC	QD	$\overline{QD}$
L	H	QA_n	QA_n	QB_n	QC_n	$\overline{QC_n}$
L	L	L	QA_n	QB_n	QC_n	$\overline{QC_n}$
H	H	H	QA_n	QB_n	QC_n	$\overline{QC_n}$
H	L	$\overline{QA_n}$	QA_n	QB_n	QC_n	$\overline{QC_n}$

H = High level

L = Low level

t = Bit time before clock pulse

t_{n+1} = Bit time after clock pulse

QA_n = State of QA at t_n

Pin Names

		Active
PE	Parallel Enable	Low
A,B,C,D	Parallel inputs	High
J	First Stage J input	High
$\overline{K}$	First Stage $\overline{K}$ input	Low
CLK	Clock Pulse Input	High-going
C	Master Clear input	Low
QA,QB,QC,QD	Parallel outputs	High
$\overline{QD}$	Last Stage complementary output	Low

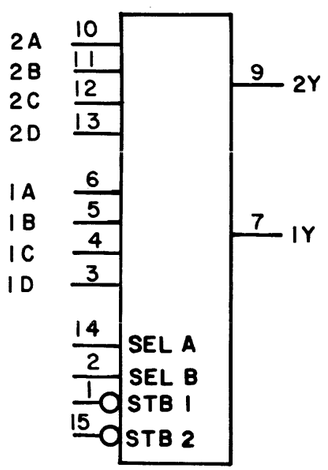
Loading:

Inputs	1 Unit Load
Outputs	10 Unit Loads

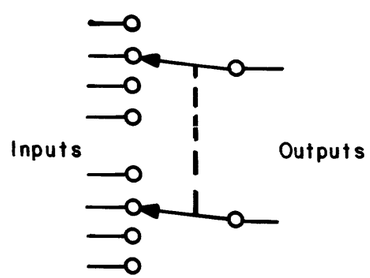
TTL Dual 4-input Multiplexer, Tri-State Part No. 10333 Type 8214

This is a Tri-State device: its outputs can neither sink nor source current when in the high-impedance (Hi-Z) state. Thus its outputs have three states: "high", "low", and "off". When enabled (both STB-1 and STB-2 low), its outputs go either high or low, depending upon the level of the selected input. When either STB-1 or STB-2 (or both) goes low, the output assumes the Hi-Z state, effectively isolating the multiplexers from the rest of the circuitry.

Logic Symbol



Analogous to DP4T Switch



2A,B,C,D = No. 2 Data inputs
1A,B,C,D = No. 1 Data inputs
SEL A, SEL B = Selection inputs
2Y, 1Y = Outputs

VCC - 16, GND - 8

All inputs 1 TTL unit load

Truth Table
(each section)

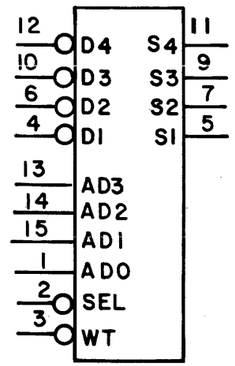
ADDRESS INPUTS		DATA INPUTS				STROBE	OUTPUT
SELB	SELA	A	B	C	D	STB	Y
X	X	X	X	X	X	H	Hi-Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address inputs SELA and SELB are common to both sections.
H = high level, L = low level, X = irrelevant.

TTL 16 x 4-bit Random Access Memory, Tri-State Part No. 10334 Type 8599

This is a Tri-State device: its outputs can neither sink nor source current when in the high-impedance (Hi-Z) state. Thus its outputs have three states; "high", "low", and "off". When enabled (SEL low) and NOT writing (WT high), it is in the "Read" mode and all memories except one are gated into the Hi-Z state while the one selected memory exhibits the normal low-impedance output characteristics of TTL. (During reading, the output is equal to the complement of the previously stored data.) When either WT goes low or SEL goes high, the outputs all assume the Hi-Z state, effectively isolating them from the rest of the circuitry. When SEL is high writing is also disabled.

Logic Symbol



Truth Table

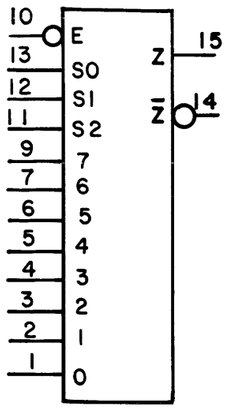
Memory Enable	Write Enable	OPERATION	Sense Outputs
SEL	WT		S1-S4
L	L	Write	Hi-Z State
L	H	Read	Complement of Data Stored in Memory
H	X	Hold	Hi-Z State

X = Irrelevant

VCC - 16, GND - 8

D1-D4 = Data inputs
AD0-AD3 = Address inputs
SEL = Select enable
WT = Write enable
S1-S4 = Data output

Logic Symbol



E = Enable input
S0-S2 = Select inputs
0 - 7 = Data inputs
Z , $\overline{Z}$ = Data outputs

VCC - 16, GND - 8

Loading:

Inputs	1 Unit Load
Outputs	10 Unit Loads

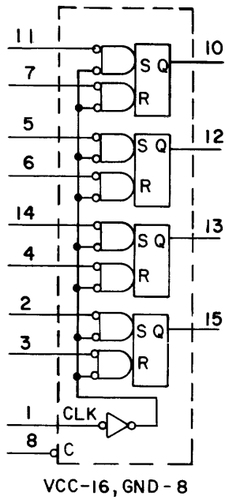
Truth Table

E	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\overline{Z}$	Z
H	X	X	X	X	X	X	X	X	X	X	X	H	L
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = HIGH voltage level
L = LOW voltage level
X = Irrelevant

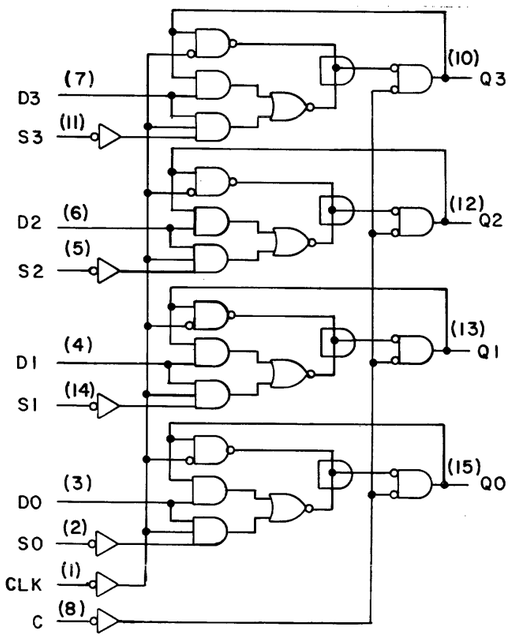
The 9314 is a multifunctional 4 bit latch. The master reset when activated overrides all other input conditions forcing all outputs LOW.
Each of the four latches can be operated in one of two modes:
D TYPE LATCH- For D type operation the S input of a latch is held LOW. While the clock is LOW the latch output follows the D input. Information present at the latch output is stored in the latch when the clock goes HIGH.
SET/RESET LATCH- During set/reset operation when the clock is LOW a latch is reset by a LOW on the D input, and can be set by a LOW on the S input if the D input is HIGH. If both S and D inputs are LOW, the D input will dominate and the latch will be reset. When the clock goes HIGH, the latch remains in the last state prior to the LOW-to-HIGH transition.

Logic Symbol



VCC-16, GND - 8

Logic Diagram



Truth Table

C	CLK	D	S	Q_n	OPERATION
H	L	L	L	L	D MODE
H	L	H	L	H	
H	H	X	X	Q_{n-1}	
H	L	L	L	L	R/S MODE
H	L	H	L	H	
H	L	L	H	L	
H	L	H	H	Q_{n-1}	
H	H	X	X	Q_{n-1}	
L	X	X	X	L	RESET

L = LOW Voltage Level
H = HIGH Voltage Level
Q_{n-1} = Previous Output State
Q_n = Present Output State
X = Irrelevant

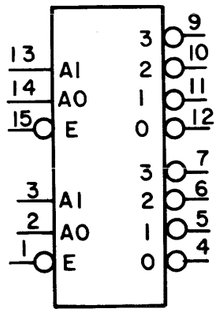
Pin Names

CLK	(Active LOW) Clock Input
D0, D1, D2, D3	Data input
S0, S1, S2, S3	Set (Active LOW) Inputs
C	Clear (Active LOW) Input
Q0, Q1, Q2, Q3	Latch Outputs (Note b)

Loading:

CLK	1.5 Unit Loads
All other inputs	1 Unit Load
Outputs	10 Unit Loads

Logic Symbol



VCC-16, GND-8

Truth Table

DECODER 1 & 2

$\overline{E}$	A_0	A_1	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L
H	X	X	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Irrelevant

Loading:

Inputs 1 Unit Load
Outputs 10 Unit Loads

9334 Truth Table

PRESENT OUTPUT STATES

C	E	D	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	MODE
L	H	X	X	X	X	L	L	L	L	L	L	L	L	CLEAR
L	L	L	L	L	L	L	L	L	L	L	L	L	L	DEMULTIPLEX
L	L	H	L	L	L	H	L	L	L	L	L	L	L	
L	L	L	H	L	L	L	L	L	L	L	L	L	L	
L	L	H	H	L	L	L	H	L	L	L	L	L	L	
.	.	.		.					.					
.	.	.		.					.					
.	.	.		.					.					
L	L	H	H	H	H	L	L	L	L	L	L	L	H	
H	H	X	X	X	X	Q_{N-1} →								MEMORY
H	L	L	L	L	L	L	Q_{N-1}	Q_{N-1}	Q_{N-1} →					ADDRESSABLE
H	L	H	L	L	L	H	Q_{N-1}	Q_{N-1} →						LATCH
H	L	L	H	L	L	Q_{N-1}	L	Q_{N-1} →						
H	L	H	H	L	L	Q_{N-1}	H	Q_{N-1} →						
.	.	.		.				.						
.	.	.		.				.						
.	.	.		.				.						
H	L	L	H	H	H	Q_{N-1} →						Q_{N-1}	L	
H	L	H	H	H	H	Q_{N-1} →						Q_{N-1}	H	

L = LOW Voltage Level
H = HIGH Voltage Level
Q_{N-1} = Previous Output State
X = Irrelevant

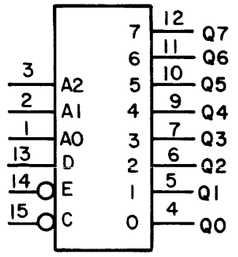
The 9334 is a multifunctional device capable of storing single line data in eight addressable latches, and being a one-of-eight decoder and demultiplexer with high-active outputs. The device also incorporates a low-active common clear for resetting all latches, as well as a low-active enable.

The 9334 has two modes of operation which are shown in the mode selection table. In the addressable latch mode, when E is LOW, data on the data line (D) is written into the addressed latch. The addressed latch will follow the data input, with all nonaddressed latches remaining in their previous states. When E is HIGH all latches remain in their previous state and are unaffected by the data or address inputs. When operating the 9334 as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while E is HIGH.

In the one-of-eight decoding or demultiplexing mode, the addressed output will follow the state of the D input, with all other outputs in the LOW state.

When E is HIGH and C is LOW all outputs are LOW and unaffected by the address and data inputs.

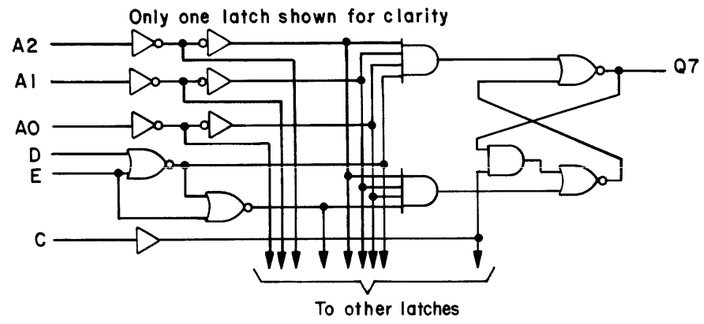
Logic Symbol



VCC-16, GND-8

AO - A2 = Address inputs
D = Data inputs
E = Enable input
C = Clear input
QO - Q7 = Data output

Logic Diagram



Mode Selection

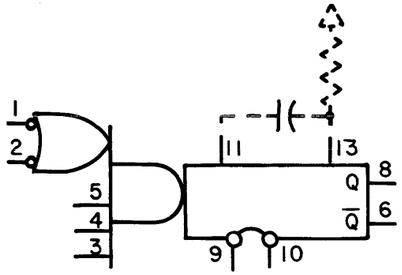
C	Mode	E	Function
H	Addressable Latch	L	Data store
		H	Memory
L	8-Channel Demultiplexer	L	Active
		H	Clear

Truth Table

Loading:

E 1.5 Unit Loads
All other inputs 1 Unit Load
Outputs 6 Unit Loads

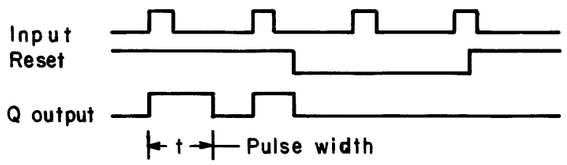
Logic Symbol



VCC-14 , GND-7

(Pin 12 not used)

Waveforms

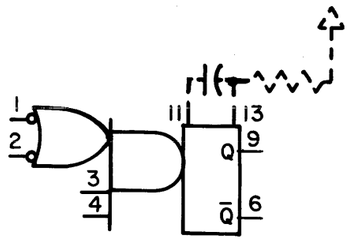


Triggering Truth Table

(PIN NO'S.) 1	2	3	4	5	9	10	OPERATION
H→L	H	H	H	H	H	H	Trigger
H	H→L	H	H	H	H	H	Trigger
L	X	L→H	H	H	H	H	Trigger
X	L	L→H	H	H	H	H	Trigger
L	X	H	L→H	H	H	H	Trigger
X	L	H	L→H	H	H	H	Trigger
L	X	H	H	L→H	H	H	Trigger
X	L	H	H	L→H	H	H	Trigger
X	X	X	X	X	L	X	Reset
X	X	X	X	X	X	L	Reset

H = HIGH Voltage Level
L = LOW Voltage Level
X = Irrelevant
H→L = Transition from HIGH to LOW Voltage Level
L→H = Transition from LOW to HIGH Voltage Level

Logic Symbol



VCC-14, GND-7

(Pins 5,9,10, and 12 not used)

Triggering Truth Table

Pin Number 1	2	3	4
H→L	H	H	H
H	H→L	H	H
L	X	L→H	H
X	L	L→H	H
L	X	H	L→H
X	L	H	L→H

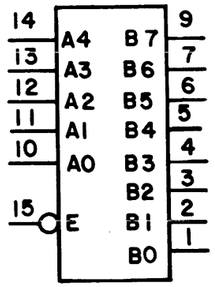
T (trigger) = (1 + 2) · 3 · 4

Change of T from FALSE to TRUE causes trigger.

H = HIGH voltage level
L = LOW voltage
L→H = transition from LOW to HIGH voltage level
H→L = transition from HIGH to LOW voltage level
X = Irrelevant

This ROM is made from a type 8256 Programmable ROM, part no. 10332. It is coded to provide the Instruction Translator function in the Model 500 Programmable Tester.

Logic Symbol



VCC-16, GND-8

A0-A4 = Address inputs
E = Enable input
B0-B7 = Data outputs

Truth Table

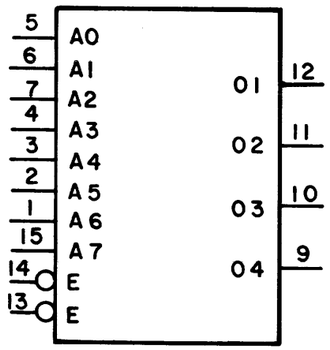
DMP3 Coding

WORD	INPUTS						OUTPUTS							
NUMBER	E	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0
X	H	X	X	X	X	X	H	H	H	H	H	H	H	H
0	L	L	L	L	L	L	H	L	H	L	H	L	L	L
1	L	L	L	L	L	H	H	L	H	L	H	L	L	L
2	L	L	L	L	H	L	H	L	H	L	H	L	L	L
3	L	L	L	L	H	H	H	L	H	L	H	L	L	L
4	L	L	L	H	L	L	H	L	H	L	H	L	L	L
5	L	L	L	H	L	H	H	L	H	L	H	L	L	L
6	L	L	L	H	H	L	H	L	H	L	H	L	L	L
7	L	L	L	H	H	H	H	L	H	L	H	L	L	L
8	L	L	H	L	L	L	H	L	H	L	H	L	L	L
9	L	L	H	L	L	H	H	L	H	L	H	L	L	L
10	L	L	H	L	H	L	H	L	H	L	H	H	L	L
11	L	L	H	L	H	H	H	L	H	L	H	L	H	H
12	L	L	H	H	L	L	H	L	H	L	H	L	L	L
13	L	L	H	H	L	H	H	L	H	L	H	L	L	L
14	L	L	H	H	H	L	H	L	H	L	H	L	L	L
15	L	L	H	H	H	H	H	L	H	L	H	L	L	L
16	L	H	L	L	L	L	L	H	L	L	H	L	L	H
17	L	H	L	L	L	H	L	L	H	H	L	L	L	L
18	L	H	L	L	H	L	L	H	L	L	H	L	L	L
19	L	H	L	L	H	H	H	H	H	L	H	L	L	L
20	L	H	L	H	L	L	H	L	H	H	H	L	L	L
21	L	H	L	H	L	H	L	L	L	L	L	L	L	L
22	L	H	L	H	H	L	L	H	H	H	H	L	L	L
23	L	H	L	H	H	H	H	H	H	H	H	L	L	L
24	L	H	H	L	L	L	H	L	L	L	L	L	L	L
25	L	H	H	L	L	H	H	L	H	H	L	L	L	L
26	L	H	H	L	H	L	H	H	H	H	H	L	L	H
27	L	H	H	L	H	H	H	H	H	H	H	L	H	H
28	L	H	H	H	L	L	H	H	H	H	H	L	L	L
29	L	H	H	H	L	H	H	H	H	H	H	L	L	L
30	L	H	H	H	H	L	H	H	H	H	H	L	L	L
31	L	H	H	H	H	H	H	H	H	H	H	L	L	L

256 x 4-bit Read Only Memory | Part No. 10341 | Type MM6300
Part No. 10345 | Type HPROM1024A

This is a Programmable Read-Only Memory chip which is normally programmed by the Vendor. No truth table appears here because each program requires a separate table. Note that the part number above is the Diablo number for the unprogrammed ROM: a new number is assigned when the ROM is programmed. Part numbers for programmed ROMs appear in the individual Program Manuals. Access time is typically 50 ns. Output is open-collector, so pull-up resistors are required. With either Enable (E) high, all outputs are high: both Enables must go low to allow the stored code to be seen at the output.

Logic Symbol



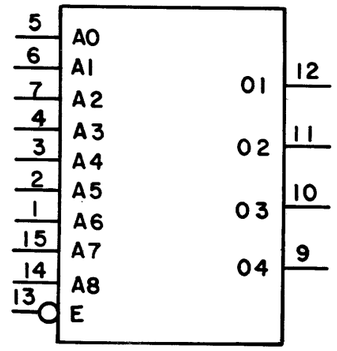
VCC-16, GND-8

A0 - A7 = Address inputs
E = Enable
01 - 04 = Data outputs

512 x 4-bit Read Only Memory | Part No. 10342 | Type MM6305
Part No. 10343 | Type HPROM2048A

These devices are Programmable Read-Only chips which are normally programmed by the Vendor. No truth table appears here because each program requires a separate table. Note that the part numbers above are the Diablo numbers for the unprogrammed ROMS: a new number is assigned when the ROM is programmed. Part numbers for programmed ROMs appear in the individual Program Manuals. Access time is typically 50 ns. Output is open-collector, so pull-up resistors are required. With Enable (E) high, all outputs are high: Enable must go low to allow the stored code to be seen at the output.

Logic Symbol



VCC-16, GND-8

A0-A8 = Address inputs
E = Enable input
01-04 = Data outputs

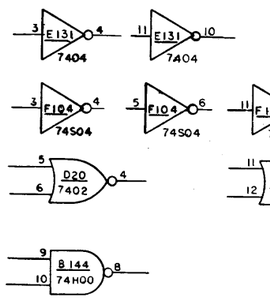
PRODUCT NO. 21037

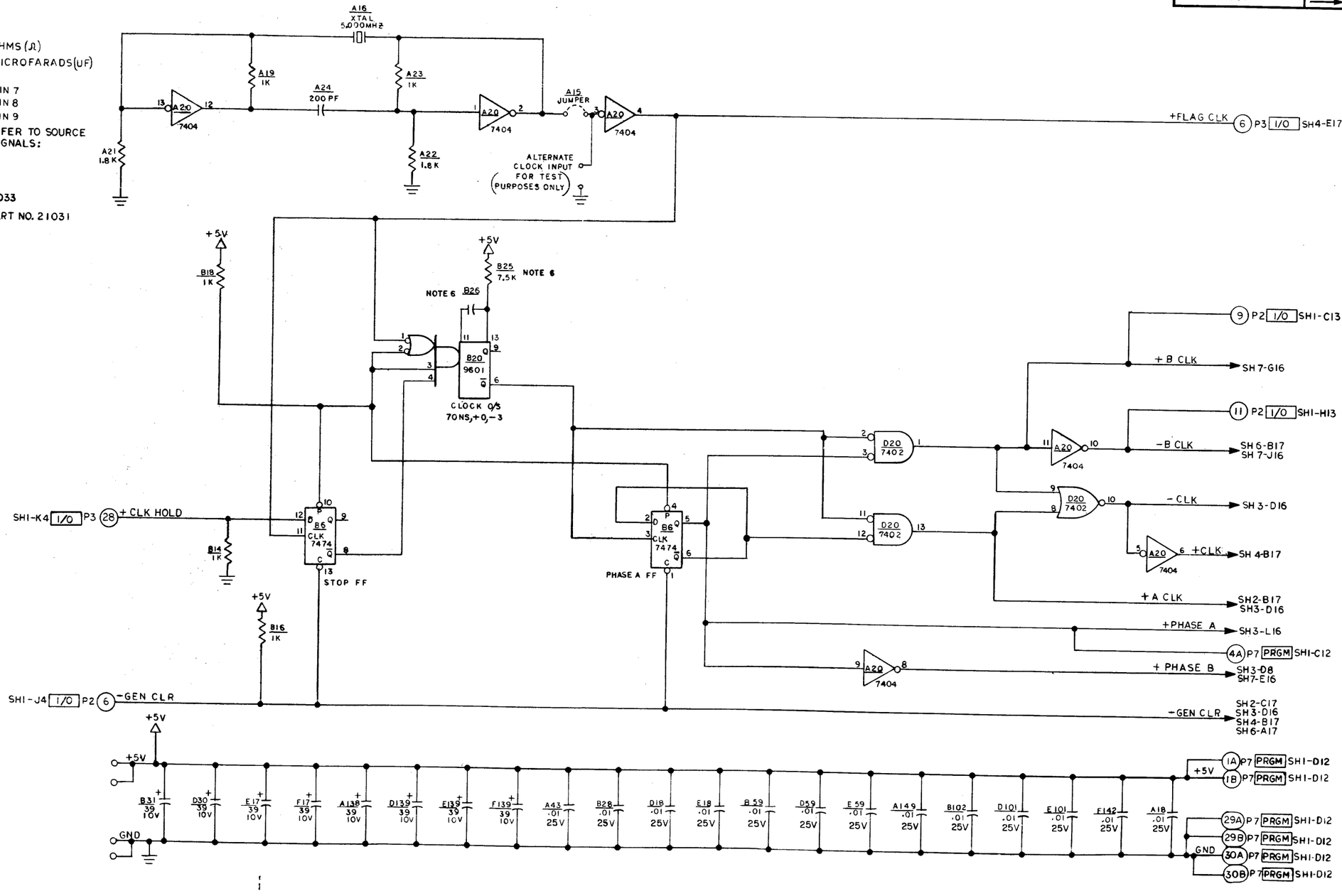
PRODUCT NO 21037 | DEVELOPMENT REV. D3

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTANCES SPECIFIED IN OHMS (Ω)
2. ALL CAPACITANCE SPECIFIED IN MICROFARADS (UF)
3. ALL RESISTORS ARE ± 5% 1/4 WATT
4. +5V TO PIN 14 OF 14 PIN IC, GND ON PIN 7
   +5V TO PIN 16 OF 16 PIN IC, GND ON PIN 8
   +5V TO PIN 24 OF 24 PIN IC, GND ON PIN 9
5. MNEMONICS IN ENCLOSED BOXES REFER TO SOURCE OR DESTINATION OF INTERBOARD SIGNALS:
   - [I/O] = I/O BOARD PART NO. 21035
   - [PRGM] = PROGRAM BOARD
   - [DISP] = DISPLAY BOARD PART NO. 21033
   - [WOSC] = WRITE OSCILLATOR BOARD PART NO. 21031
6. ADJUSTED DURING MANUFACTURE

SPARE GATES





PROC

Diablo Systems Incorporated
Hayward, California 94545

TITLE: LOGIC DIAGRAM
PROCESSOR CLOCK
PROCESSOR LOGIC BOARD

MODEL: 5CO PROGRAMMABLE TESTER

PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED.

SYSTEM LOGIC NO.

SHEET	TOTAL SHEETS	SIZE	PRODUCT NO.	REV
1	12	D	21037	A

REV	ECO NO	DATE	ENG	DATE	CHECKED	DATE	DRAWN	DATE
A	3905 4766		R Sussman	1/29/73			BRIA	3-21-73

PRODUCT NO 21037 | REFERENCE DESIGNATORS NOT USED | REFERENCE DESIGNATORS LAST USED

DCT CTL 0020, 1-23-73

PRODUCT NO. 21037 | DEVELOPMENT REV. D3

STACK ADDRESS REGISTER

SH4-K2 +A11
SH4-J2 +A10
SH4-J2 +A9
SH4-H2 +A8

SH4-G2 +A7 → A143 D Q → 15 +STACK ADDR REG 7 → 23A P7 PRGM SH2-K16

9300/74195

SH4-F2 +A6 → D Q → 13 +STACK ADDR REG 6 → 23B P7 PRGM SH2-J16

SH4-F2 +A5 → D Q → 14 +STACK ADDR REG 5 → 24A P7 PRGM SH2-J16

SH4-E2 +A4 → D Q → 12 +STACK ADDR REG 4 → 24B P7 PRGM SH2-J16

SH4-D2 +A3 → A74 D Q → 12 +STACK ADDR REG 3 → 25B P7 PRGM SH2-J16

9300/74195

SH4-C2 +A2 → D Q → 15 +STACK ADDR REG 2 → 28B P7 PRGM SH2-J16

SH4-C2 +A1 → D Q → 14 +STACK ADDR REG 1 → 27B P7 PRGM SH2-H16

SH4-C2 +AØ → D Q → 13 +STACK ADDR REG Ø → 26B P7 PRGM SH2-H16

SH7-E3 -LOAD STACK ADDR REG
SH1-E2 -GEN CLR

SH3-G3 I/O P3 29 -CLR PROG CNTR
SH1-F2 +A CLK
SH7-K3 -BRANCH

7408 (1/3 1)

F104 74SØ4

PROGRAM COUNTER

B90 74161 BIN CNTR
D104 74161 BIN CNTR
B75 74161 BIN CNTR

CRY, LOAD, EN-P, EN-T, CLK, C

+5V
F128 1K

F104 74SØ4

+PROG CNTR 11 → 17A P7 PRGM SH1-C12
+PROG CNTR 10 → 2A P7 PRGM SH1-C12
+PROG CNTR 9 → 15A P7 PRGM SH1-L12
-PROG CNTR 9 → 4B P7 PRGM SH1-L12
+PROG CNTR 8 → 3B P7 PRGM SH1-L12
-PROG CNTR 8 → 3A P7 PRGM SH1-K12
+PROG CNTR 7 → 2B P7 PRGM SH1-K12
+PROG CNTR 6 → 13B P7 PRGM SH1-K12
+PROG CNTR 5 → 14B P7 PRGM SH1-K12
+PROG CNTR 4 → 15B P7 PRGM SH1-K12
+PROG CNTR 3 → 16B P7 PRGM SH1-J12
+PROG CNTR 2 → 18A P7 PRGM SH1-J12
+PROG CNTR 1 → 18B P7 PRGM SH1-J12
+PROG CNTR Ø → 17B P7 PRGM SH1-J12

+VF128 → SH7-J16

PROG

Diablo Systems Incorporated
Hayward, California 94545

TITLE: LOGIC DIAGRAM
PROGRAM COUNTER/STACK ADDR REG.
PROCESSOR LOGIC BOARD

MODEL: 50C PROGRAMMABLE, TESTER

PROPRIETARY INFORMATION / UNAUTHORIZED DISCLOSURE OR USE PROHIBITED.

SYSTEM LOGIC NO.

SHEET	TOTAL SHEETS	SIZE	PRODUCT NO.	REV
2	12	D	21037	A

DRAWN: BRIA 3-23-73 | CHECKED | ENG: R Summers 6/19/73 | MFG | DATE

REV	J	H	G	F	E	D	C	B	A
E.C.O. NO.									3908 4762

PRODUCT NO 21037 | REFERENCE DESIGNATORS NOT USED | REFERENCE DESIGNATORS LAST USED

DCY CTL 0020, 1-23-73

PRODUCT NO. 21037

DEVELOPMENT REV. D3

SHI-E2 +PHASE A

SHI-G3 PRGM P7 (11B) -PROG ROM 11

SHI-G3 PRGM P7 (12B) -PROG ROM 10

SHI-G3 PRGM P7 (10B) -PROG ROM 9

SHI-G3 PRGM P7 (9B) -PROG ROM 8

+5V B140 330 B131 74SØ4 A3

+5V B127 330 B131 74SØ4 A2

+5V B128 330 B131 74SØ4 A1

+5V B129 330 B131 74SØ4 A0

D131 7408

B117 DMP 3

OP CODE TRANS-LATOR PROM

ALU & GR CONTROL REG

+5V D128 430 B7 E117 74174 +PROG BIT 9 SH5-H16

+5V D115 430 B6 E117 +ALU MODE SH4-C17

+5V B126 430 B5 D117 74174 +ALU SEL 3 SH 4-C17

+5V B116 430 B4 E117 +ALU SEL 2 SH 4-C17

+5V B114 430 B3 D117 +ALU SEL 1 SH4-B17

+5V B115 430 B2 D117 +ALU SEL Ø SH4-B17

+5V D127 430 B1 D117 E131 7404 -BRANCH IF SH 7-L16

+5V D116 430 BØ E117 B144 74H00 -GATED SPC INSTR (28) P2 1/0 SH6-D16

+DONT SAVE RESULTS SH7-F16

E131 7404 +CARRY IN SH 4-B17

NOTE: ALL FLIP-FLOPS NOT IN SAME IC PACKAGE.

SHI-G2 -CLK

SHI-E2 -GEN CLR

SHI-F2 +A CLK

+PROG BIT 8 SH 5-G16

OP CODE DECODER

SHI-F3 PRGM P7 (8A) -PROG ROM 7 330 +5V A138 A131 74SØ4

SHI-D3 PRGM P7 (8B) -PROG ROM 3 +5V B139 330 B131 74SØ4

SHI-F3 PRGM P7 (9A) -PROG ROM 6 +5V A139 330 A131 74SØ4

SHI-D3 PRGM P7 (7B) -PROG ROM 2 +5V A129 330 A131 74SØ4

SHI-E3 PRGM P7 (10A) -PROG ROM 5 +5V A140 330 A131 74SØ4

SHI-D3 PRGM P7 (6B) -PROG ROM 1 +5V A128 330 A131 74SØ4

SHI-E3 PRGM P7 (11A) -PROG ROM 4 +5V B138 330 B131 74SØ4

SHI-D3 PRGM P7 (5B) -PROG ROM Ø +5V A127 330 A131 74SØ4

SHI-E3 +PHASE B

SH6-G3 I/O P3 (18) +A FIELD

SH6-G3 I/O P5 (16) +B FIELD

F86 1K F112 1K

ADDRESS FIELD SELECT

B104 9322 74157

4X2-BIT MPLXR

SEL

ENA

ALU & GR CONTROL REG

D144 7402 D144 7402 D144 7402

D117 74174

-GEN REG ENA SH 4-H17

(18) P2 I/O SH5-B16 +INPUT SEL SH 5-C16

D117 +OUTPUT SEL SH 7-G16

D131 7408 E131 7404

D117 CLK

+PROG BIT 7 SH5-E16

+PROG BIT 6 SH5-E16

+PROG BIT 5 SH 5-L8

+PROG BIT 4 SH 5-K8

+PROG BIT 3 SH 5-H8

(33) P2 I/O SH6-D16 +ADDR 8 SH 4-J17

E104 74174

(20) P2 I/O SH5-B16 +ADDR 4 SH 4-J17 SH 7-E16 SH 5-B16

E104 +ADDR 2 SH4-J17 SH5-C16 SH 7-E16

E104 +ADDR 2A (23) P3 I/O SH5-C16

E104 +ADDR 1 SH4-J17 SH5-C17 SH 7-E16

E104 +ADDR 1A (26) P3 I/O SH5-C16

(32) P2 I/O SH6-D16 +PROG BIT 2 SH5-G8, SH7-L16

(31) P2 I/O SH6-D16 +PROG BIT 1 SH5-E8, SH7-L16

+PROG BIT Ø SH5 D8, SH7-L16

(34) P2 I/O SH6-C16

ADDRESS DECODER

PROG

Diablo Systems Incorporated
Hayward, California 94545

TITLE: LOGIC DIAGRAM INSTRUCTION TRANSLATOR PROCESSOR LOGIC BOARD

MODEL: 500 PROGRAMMABLE TESTER

PRODUCT NO	REFERENCE DESIGNATORS NOT USED	REFERENCE DESIGNATORS LAST USED	REV	E.C.O. NO.	DRAWN	DATE	SHEET	TOTAL SHEETS	SIZE	PRODUCT NO.	REV
21037			A	3905 4762	BRIA	4-24-73	3	12	D	21037	A

PRODUCT NO. 21037

PRODUCT NO. 21037 | DEVELOPMENT REV. D3

GENERAL REGISTERS

ARITHMETIC/LOGICAL UNIT

TEMPORARY REGISTER

NOTE: B BUS IS TRI STATE

SH5-L10
SH5-L10 I/O P3 (3) +B11
SH5-K10
SH5-K10 I/O P3 (4) +B10
SH5-H10
SH5-H10 I/O P3 (1) +B9
SH5-G10
SH5-G10 I/O P3 (2) +B8

SH3-H2 +ADDR 8
SH3-G2 +ADDR 4
SH3-F2 +ADDR 2
SH3-E2 +ADDR 1
SH3-L2 - GEN REG ENA
SH7-F3 -WRITE GEN REGS
SH5-G10

SH5-E10 I/O P3 (10) +B7
SH5-D10
SH5-D10 I/O P3 (7) +B6
SH5-L3
SH5-L3 I/O P3 (34) +B5
SH5-K3
SH5-K3 I/O P3 (30) +B4

SH5-H3
SH5-H3 I/O P3 (31) +B3
SH5-G3
SH5-G3 I/O P3 (32) +B2
SH5-E3
SH5-E3 I/O P3 (33) +B1
SH5-D3
SH5-D3 I/O P3 (12) +B0

SH3-K10 +ALU MODE
SH3-J10 +ALU SEL 3
SH3-J10 +ALU SEL 2
SH3-H10 +ALU SEL 1
SH3-G10 +ALU SEL 0
SH3-E10 +CARRY IN

SH1-F2 +CLK
SH1-E2 +GEN CLR

-A8
-A9
-A10
-A11

B33 DM 8599 RAM
B47 DM8599 RAM
B61 DM8599 RAM
AD3
AD2
AD1
AD0
SEL
WT

+B11
+B10
+B9
+B8
+B7
+B6
+B5
+B4
+B3
+B2
+B1
+B0

A3 A2 A1 A0 74181 ALU
CRY OUT
CRY IN
B3 B2 B1 B0
F3 F2 F1 F0
AM AS3 AS2 AS1 AS0

A30
A45
A59

-C11
-C10
-C9
-C8
-C7
-C6
-C5
-C4
-C3
-C2
-C1
-C0

D33
D47
D61
74175
D Q CLK C

-A4
-A5
-A6
-A7
-A0
-A1
-A2
-A3

4 P2 I/O SH1-L14 +A11 SH2-L17 SH6-K17 SH7-J16
2 P2 I/O SH1-L14 +A10 SH2-K17 SH6-K17
3 P2 I/O SH1-K14 +A9 SH2-K17 SH6-J17
1 P2 I/O SH1-K14 +A8 SH2-K17 SH6-H17
7 P2 I/O SH1-H14 +A7 SH2-J17 SH6-H17
5 P2 I/O SH1-G14 +A6 SH2-H17 SH6-G17
8 P2 I/O SH1-G14 +A5 SH2-H17 SH6-F17
10 P2 I/O SH1-F14 +A4 SH2-G17 SH6-E17
21 P2 I/O SH1-E14 +A3 SH2-E17 SH6-D17
17 P2 I/O SH1-D14 +A2 SH2-E17 SH6-C17
15 P2 I/O SH1-D14 +A1 SH2-E17 SH6-C17
13 P2 I/O SH1-C14 +A0 SH2-D17 SH6-B17

+ALU ZERO SH 7-G16

PROG

Diablo Systems Incorporated
Hayward California 94545

TITLE LOGIC DIAGRAM
ARITHMETIC/LOGIC SECTION
PROCESSOR LOGIC BOARD
MODEL SCO PROGRAMMABLE TESTER

PROPRIETARY INFORMATION
UNAUTHORIZED DISCLOSURE OR USE PROHIBITED.

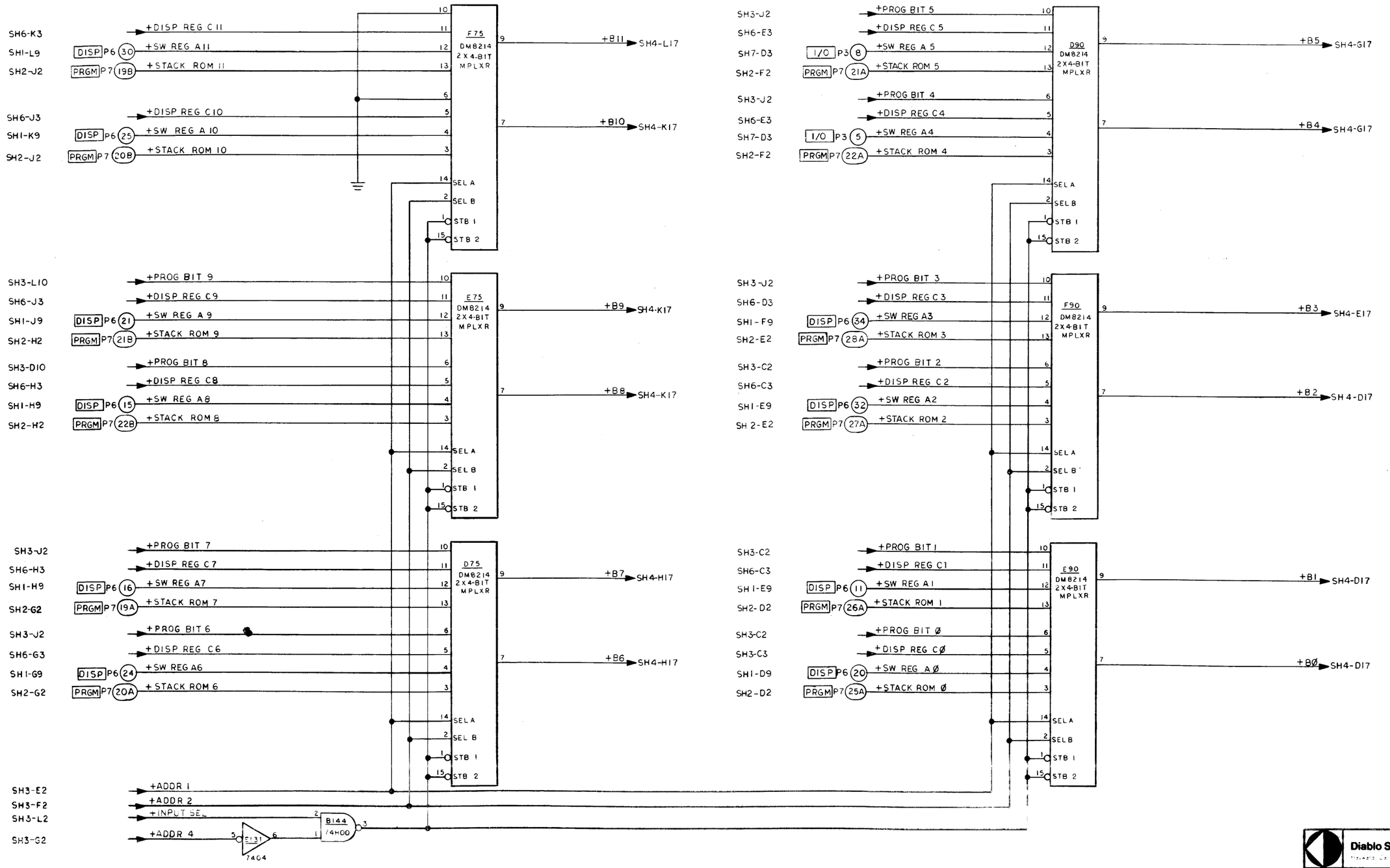
SYSTEM LOGIC NO

SHEET	TOTAL SHEETS	SIZE	PRODUCT NO.	REV
4	12	D	21037	A

PRODUCT NO 21037 | REFERENCE DESIGNATORS NOT USED | REFERENCE DESIGNATORS LAST USED

REV J	REV H	REV G	REV F	REV E	REV D	REV C	REV B	REV A
E.C.O. NO.	E.C.O. NO.	E.C.O. NO.	E.C.O. NO.	E.C.O. NO.	E.C.O. NO.	E.C.O. NO.	E.C.O. NO.	E.C.O. NO. 3905 4762

MFG | DATE | ENG | DATE R. Sweiver 6/1/73 | CHECKED | DATE | DRAWN | DATE F. BRIA 5-28-73



PROC

Diablo Systems Incorporated

TITLE: LOGIC DIAGRAM MULTIPLEXER PROCESSOR LOGIC BOARD

MODEL: 500 PROGRAMMABLE TESTER

PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED.

SYSTEM LOGIC NO.

PRODUCT NO.	SHEET	TOTAL SHEETS	SIZE	PRODUCT NO.	REV
21037	5	12	D	21037	A

REV	J	H	G	F	E	D	C	B	A
E.C.O. NO.									3905 4762

MFG	DATE	ITEMS	DATE	CHECKED	DATE	DRAWN	DATE
		DS Surman	6/19/73			BRIA	4/8-73

PRODUCT NO. 21037

REFERENCE DESIGNATORS NOT USED

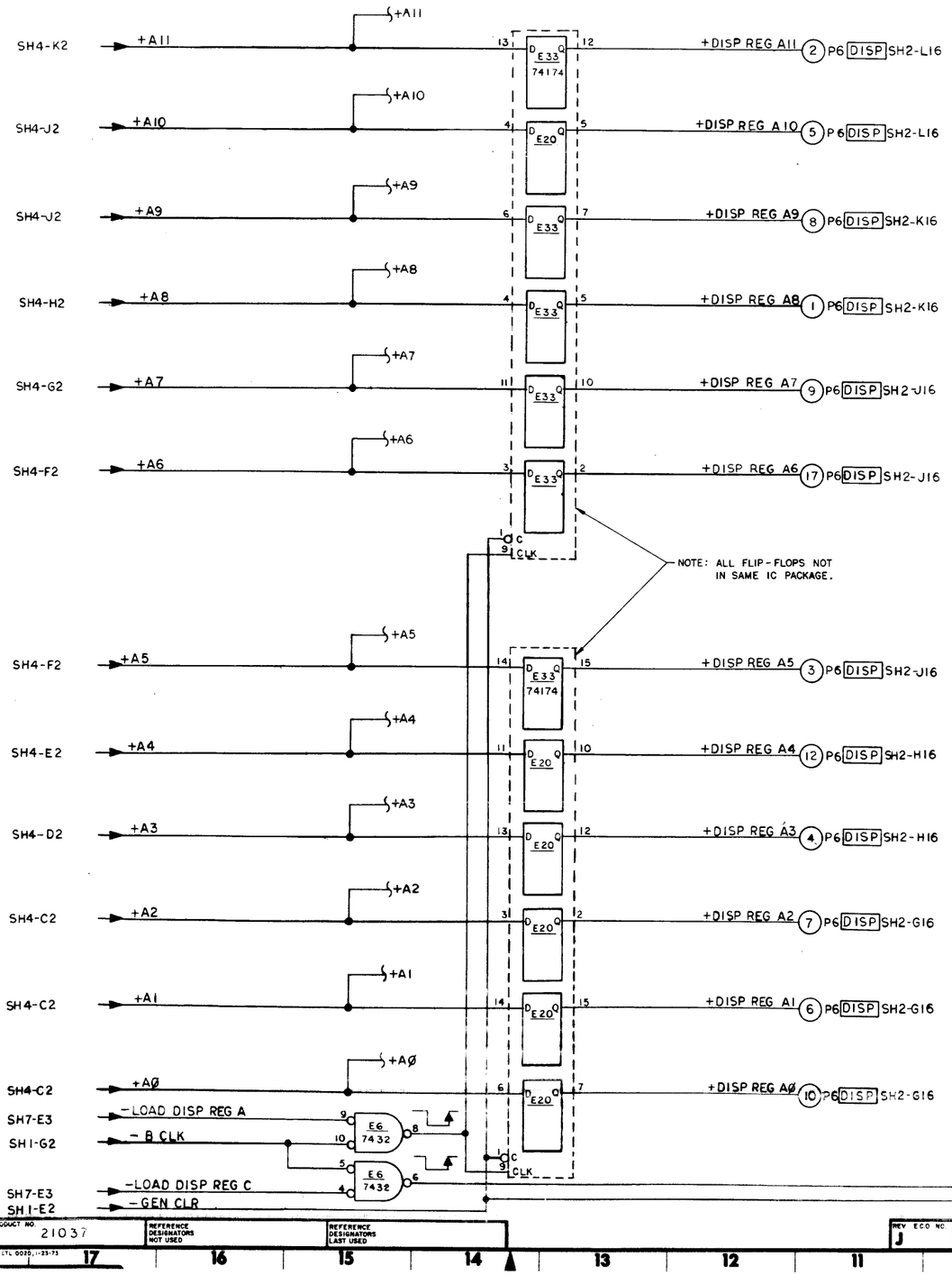
REFERENCE DESIGNATORS LAST USED

DOC. CTL. 30205 (1-23-73)

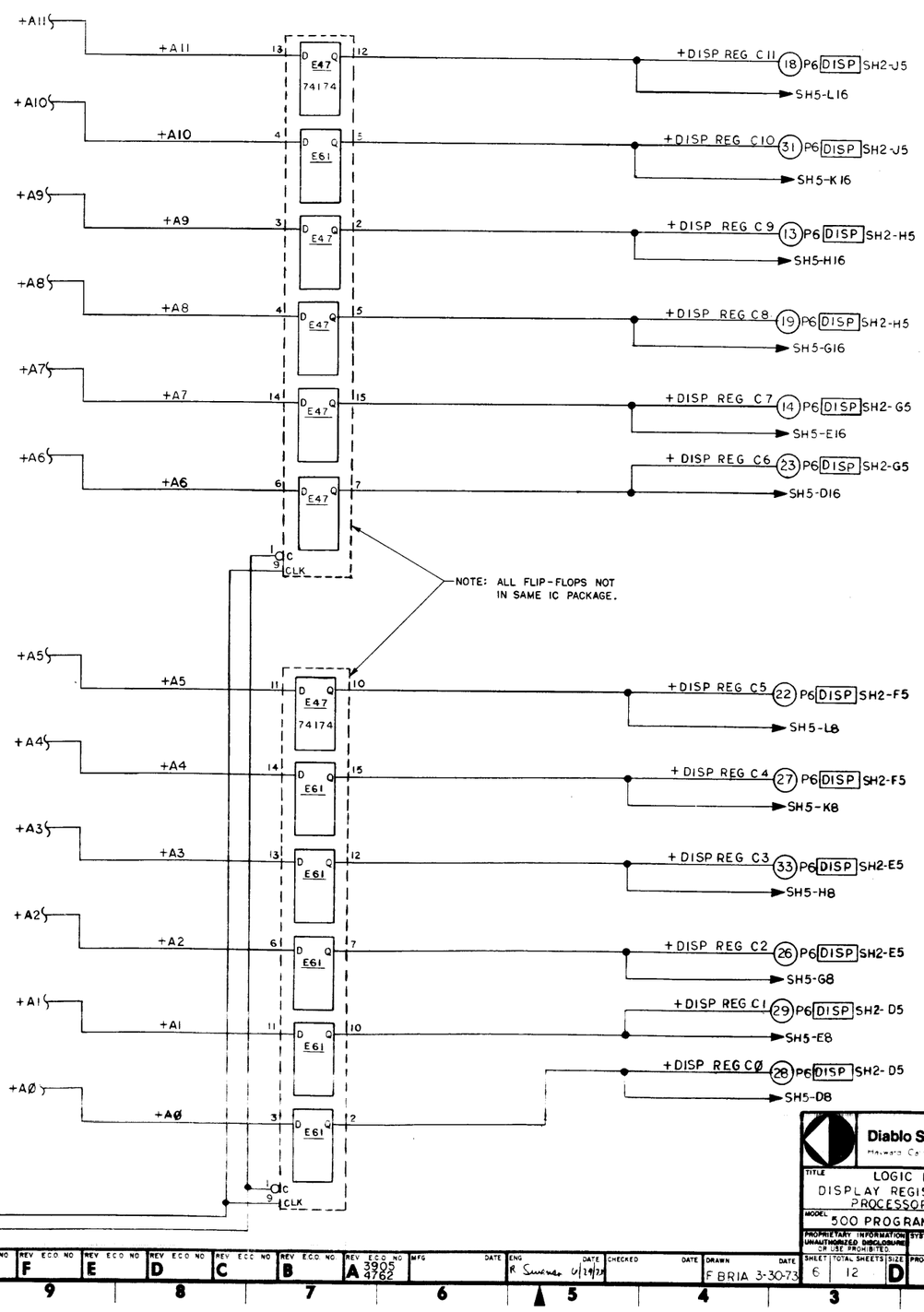
PRODUCT NO. 21037

PRODUCT NO. 21037 DEVELOPMENT REV. D3

DISPLAY REGISTER A



DISPLAY REGISTER C



PROC

Diablo Systems Incorporated
Hayward, California 94545

TITLE: LOGIC DIAGRAM
DISPLAY REGISTERS A & C
PROCESSOR LOGIC BOARD

MODEL: 500 PROGRAMMABLE TESTER

PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED.

SYSTEM LOGIC NO.

PRODUCT NO.	REV
21037	A

SHEET	TOTAL SHEETS	SIZE
6	12	D

REV	ECO NO	DATE	ENG	DATE	CHECKED	DATE	DRAWN	DATE
J								
H								
G								
F								
E								
D								
C								
B								
A	3905 4762		R Sumner	6/19/73			F BRIA	3-30-73

PRODUCT NO. 21037 | REFERENCE DESIGNATORS NOT USED | REFERENCE DESIGNATORS LAST USED

DOT LTL 0020, 1-23-73

SH3-G10 −BRANCH IF
SH3-D2 +PROG BIT 2
SH3-C2 +PROG BIT 1
SH3-C2 +PROG BIT Ø
NOT USED I/O P2 (23) +I/O BRANCH B
NOT USED I/O P2 (25) +I/O BRANCH A
SH3-D3 I/O P3 (20) − ADDR MARK DET
SH4-G10 I/O P3 (27) −STATUS IN 5

F127 1K

SH2-F2 +VF128
SH4-K2 +A11
SH4-G2 −B CLK

F131 7474 (P, D, CLK, Q, C)

+ MINUS

F129 620 +5V

SH4-C2 +ALU ZERO
SH1-H2 +B CLK

F131 7474

+ ZERO
+ NOT ZERO

F126 1K

F117 9312 MPLXR (E, S0, S1, S2, 0–7)

−BRANCH → SH2-B17

SH3-K2 +OUTPUT SEL
SH3-E10 +DONT SAVE RESULTS

E144 7432

−WRITE GEN REGS → SH4-H17

E131 7404

B144 74H00

SH1-E2 +PHASE B

D131 7408

SH3-G2 +ADDR 4
SH3-F2 +ADDR 2
SH3-E2 +ADDR 1

D6 7442 DECODER (E, 0–9)

−LOAD DATA INPUT REG (26) P2 I/O SH2-C16
−LOAD BIT RING (14) P2 I/O SH1-H14
−LOAD STACK ADDR REG → SH2-D17
−LOAD DISP REG C → SH6-B16
−LOAD DISP REG A → SH6-B17
−LOAD DISP REG B (12) P2 I/O SH7-B15
−LOAD I/O A (27) P2 I/O NOT USED

PROC

Diablo Systems Incorporated
Hayward California 94545

TITLE LOGIC DIAGRAM
BRANCH AND STORE CONTROLS
PROCESSOR LOGIC BOARD

MODEL 500 PROGRAMMABLE TESTER

PROPRIETARY INFORMATION
UNAUTHORIZED DISCLOSURE OR USE PROHIBITED

SYSTEM LOGIC NO.

PRODUCT NO. 21037 REV A

SHEET 7 TOTAL SHEETS 12 SIZE D

DRAWN F BRIA 3-30-73 CHECKED ENG R. Swenson 4/19/73 MFG

REV J ECO NO. REV H ECO NO. REV G ECO NO. REV F ECO NO. REV E ECO NO. REV D ECO NO. REV C ECO NO. REV B ECO NO. REV A ECO NO 3905 4762

PRODUCT NO 21037 REFERENCE DESIGNATORS NOT USED REFERENCE DESIGNATORS LAST USED

DOC CTL 0025, 1-23-73

PRODUCT NO. 21035

PRODUCT NO. 21035 | DEVELOPMENT REV. | D4

NOTE; UNLESS OTHERWISE SPECIFIED,

1. ALL RESISTANCES ARE SPECIFIED IN OHMS(Ω) ±5% 1/4 WATT.
2. ALL CAPACITANCE SPECIFIED IN MICROFARADS(μf).
3. +5V TO PIN 14 OF 14 PIN IC, GND TO PIN 7. +5V TO PIN 16 OF 16 PIN IC, GND TO PIN 8. EXCEPT IC 7476.(B75)
4. MNEMONICS IN ENCLOSED BOXES REFER TO SOURCE OR DESTINATION OF INTERBOARD SIGNALS.

   PROC = PROCESSOR BOARD, PART NO. 21037

   PRGM = PROGRAM BOARD

   DISP = DISPLAY BOARD PART NO. 21033

   WOSC = WRITE OSCILLATOR BOARD PART NO. 21031
5. ADJUSTED DURING MANUFACTURE

SPARES

A146 7400 — E6 7402 — E131 7404 — B6 74S20

E104 858 — E104 858

SH6-L3 → -WAIT FOR BIT RING

SH4-K3 PROC P2 (4) +A11 — SH4-K3 PROC P2 (2) +A10 — SH4-J3 PROC P2 (3) +A9 — SH4-H3 PROC P2 (1) +A8

SH6-C4 +READ, SH6-C4 +WRITE → F131 7432 → F6 7432 → +SHIFT ENA

SH3-F3 +SERIAL IN CLK O/S — SH3 C3 +READ SYNC DETECT — SH3-K3 +WRITE PHASE FF — SH3-H3 +BIT RING SHIFT SYNC → F47 7400 → B6 74S20 → B60 7404

SH3-K3 -WRITE SHIFT

SH7-F3 PROC P2 (14) -LOAD BIT RING — SH1-G2 PROC P2 (11) -B CLK → F6 7432

SH4-G3 PROC P2 (7) +A7 — SH4-F3 PROC P2 (5) +A6 — SH4-F3 PROC P2 (8) +A5 — SH4-E3 PROC P2 (10) +A4

-B CLK

SH6-J4 → +BYTE MODE → B60 7404 → D6 7400

SH4-D3 PROC P2 (21) +A3 — SH4-D3 PROC P2 (17) +A2 — SH4-C3 PROC P2 (15) +A1 — SH4-C3 PROC P2 (13) +AØ

SH1-H2 PROC P2 (9) +B CLK — NOT USED

SH1-C8 WOSC P4 (1) -GEN CLR

F33 9300 74195 — E33 9300 74195 — E47 9300 74195

+5V — B74 1K

B75 7476 CLK

A143 51Ω

+5V — A17 .01 25V — B15 39 10V — B17 .01 25V — B141 .01 25V — B142 39 10V — D15 39 10V — D17 .01 25V — D141 .01 25V — D142 39 10V — E14 39 10V — E17 .01 25V — E141 .01 25V — E142 39 10V — F14 39 10V — F17 .01 25V — F140 39 10V — F141 .01 25V — GND

+A11 → SH2-L16 SH7-L15

+BIT RING ZERO → SH2-B16

+A10 → SH2-L16 SH7-K15

+A9 → SH2-K16 SH7-J15

+A8 → SH2-K16 SH7-J15

+CLK HOLD (28) P3 PROC SH1-F14

+VB74 → SH3-J16

+A7 → SH2-H16 SH7-H15

+SKIP CLK OUT → SH3-H16

+A6 → SH2-H16 SH7-G16

+A5 → SH2-G16 SH7-F15

+A4 → SH2-G16 SH7-G15

-B CLK → SH2-C16 SH7-B17

+A3 → SH2-E16 SH7-E15

+A2 → SH2-E16 SH7-D15

+A1 → SH2-D16 SH7-C15

+AØ → SH2-D16 SH7-B15

(6) P2 PROC SH1-E14

-GEN CLR → SH2-B16 SH4-E17 SH6-C16 SH7-B15 SH3-G16

I/O

Diabo Systems Incorporated
Hayward, California 94545

TITLE: LOGIC DIAGRAM BIT RING I/O LOGIC BOARD

MODEL: 500 PROGRAMMABLE TESTER

PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED.

SYSTEM LOGIC NO.

SHEET 1 | TOTAL SHEETS 11 | SIZE D | PRODUCT NO. 21035 | REV B

PRODUCT NO	REFERENCE DESIGNATORS NOT USED	REFERENCE DESIGNATORS LAST USED
21035		

REV	E.C.O. NO.	DWN	DATE	CHECKED	DATE	DRAWN	DATE
J							
H							
G							
F							
E							
D							
C							
B	4761						
A	3905			R Swenson	6/27/73	BRIA	5-4-73

DGT CTL 0020, -23-73

PRODUCT NO. 21035

DEVELOPMENT REV. D4

DATA INPUT REGISTER

DATA OUTPUT REGISTER

SHI-L4 → +A11

SHI-L4 → +A10

SHI-K4 → +A9

SHI-K4 → +A8

SHI-H4 → +A7

SHI-H4 → +A6

SHI-G4 → +A5

SHI-G4 → +A4

SHI-E4 → +A3

SHI-E4 → +A2

SHI-D4 → +A1

SHI-D4 → +AØ

SH6-C4 → +READ

SH7-F3 PROC P2 (26) → −LOAD DATA INPUT REG

SHI-F4 → −B CLK

SH3-F3 → +SERIAL IN CLK Q/S

SH3-E3 → +BIT DETECTED

SHI-L4 → +BIT RING ZERO

SH3-G3 → −WRITE CLK PHASE

SHI-C4 → −GEN CLR

D20 / B20 — 9300 / 74195 — bits 11, 10, 9, 8

D33 / B33 — 9300 / 74195 — bits 7, 6, 5, 4

D47 / B47 — 9300 / 74195 — bits 3, 2, 1, Ø

PE, CLK, J, K, C

E6 7402 — D6 7400 — A146 7400

+DATA INPUT REG 8 → SH7-K8

+DATA INPUT REG 7 → SH7-J8

+DATA INPUT REG 6 → SH7-J8

+DATA INPUT REG 5 → SH7-H8

+DATA INPUT REG 4 → SH3-C16, SH7-H8

+DATA INPUT REG 3 → SH7-G8

+DATA INPUT REG 2 → SH7-G8

+DATA INPUT REG 1 → SH7-F8

+DATA INPUT REG Ø → SH7-F8

+DATA OUTPUT REG 11 → SH3-K16, SH5-L16

+DATA OUTPUT REG 10 → SH5-K16

+DATA OUTPUT REG 9 → SH5-H16

+DATA OUTPUT REG 8 → SH5-G16

+DATA OUTPUT REG 7 → SH5-E16

+DATA OUTPUT REG 6 → SH5-D16

+DATA OUTPUT REG 5 → SH5-L8

+DATA OUTPUT REG 4 → SH5-K8

+DATA OUTPUT REG 3 → SH5-H8

+DATA OUTPUT REG 2 → SH5-G8

+DATA OUTPUT REG 1 → SH5-E8

+DATA OUTPUT REG Ø → SH5-D8

I/O

Diablo Systems Incorporated
Hayward, California 94545

TITLE: LOGIC DIAGRAM
DATA INPUT REG/DATA OUTPUT REG
I/O LOGIC BOARD

MODEL: 500 PROGRAMMABLE TESTER

PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED.

SYSTEM LOGIC NO.

PRODUCT NO. 21035 | REV B

SHEET 2 | TOTAL SHEETS 11 | SIZE D

DRAWN BRIA 5-7-73 | CHECKED | ENG K Swenson 6/19/73 | MFG

PRODUCT NO. 21035

REFERENCE DESIGNATORS NOT USED

REFERENCE DESIGNATORS LAST USED

REV J 4761 | REV H A3905

ECT CTL DOCU. 1-23-73

PRODUCT NO. 21035

PRODUCT NO. 21035 DEVELOPMENT REV. D4

SH6-C4 → +BIT RING SHIFT CONTROL
SH6-J3 → +VE III
SH1-J4 → +VB74
SH2-L3 → + DATA OUTPUT REG 11

SH1-C2 WOSC P5 (26)
SH1-C2 WOSC P5 (24)
SH1-C2 WOSC P5 (23)
SH1-C3 WOSC P5 (22)
SH1-C3 WOSC P5 (21)
SH1-C4 WOSC P5 (19)
→ +DISK OSC

SH1-H4 → +SKIP CLK OUT
SH6-J4 → +ENA SKIP CLK OUT
SH6-C4 → +WRITE

SH1-C9 WOSC P4 (3) → -CLR PROG CNTR
SH1-C4 → -GEN CLR

A60 7400
A74 7420
E117 858
B75 CLK 7476 — WRITE PHASE F.F.
B90 CLK 74S74 — WRITE SYNC F.F.
-WRITE DATA
-WRITE CLK

-WRITE SHIFT → SH1-H13
+ WRITE PHASE FF → SH1-J13
- SERIAL DATA OUT (16) P5 WOSC SH1-E14
+ BIT RING SHIFT SYNC → SH1-J13
-WRITE CLK PHASE → SH2-B16
-CLR PROG CNTR (29) P3 PROC SH2-B17

+5V
A100 510

+SERIAL IN CLK O/S → SH1-J13, SH2-C16

SH4-L3 → +3.5V
D129 82
SH1-G14 WOSC P5 (32) → -SERIAL IN DATA
D131 7404
E131 7404
D99 82
SH1-G14 WOSC P4 (22) → -SERIAL IN CLK
D90 7404
SH4-J10 → +VB129

+5V
E145 10pf
E146 5.1 K NOTE 5
D144 9600
SERIAL IN CLK O/S 100 NS

B60 7404 ×3
B104 CLK 7474 — + BIT DETECTED → SH2-B16

+5V
B116 1K
A134 16.9K NOTE 5 1/8 W 1%
A135 150pf
A133 9600
B117 CLK 7474 — MISSED CLK F.F.
-ADDRESS MARK DETECT (20) P3 PROC SH7-K17

SH6-J4 → +MISSING CLK ENA
MISSING CLK O/S 1.00 µS ±.05

(13) P4 WOSC SH1-C17
+ READ SYNC DETECT → SH1-J13

SH2-G9 → +DATA INPUT REG 4
SH6-C4 → +READ A

1/0

Diablo Systems Incorporated
Hayward California 94545

TITLE: LOGIC DIAGRAM READ/WRITE LOGIC I/O LOGIC BOARD
MODEL: 500 PROGRAMMABLE TESTER
PROPRIETARY INFORMATION — UNAUTHORIZED DISCLOSURE ON 1ST PROHIBITED
SYSTEM LOGIC NO.

PRODUCT NO.	REFERENCE DESIGNATORS NOT USED	REFERENCE DESIGNATORS LAST USED	REV J E.C.O. NO.	REV H E.C.O. NO.	REV G E.C.O. NO.	REV F E.C.O. NO.	REV E E.C.O. NO.	REV D E.C.O. NO.	REV C E.C.O. NO.	REV B E.C.O. NO. 4761	REV A E.C.O. NO. 3905	MFG	DATE	ENG	DATE	CHECKED	DATE	DRAWN	DATE	SHEET	TOTAL SHEETS	SIZE	PRODUCT NO.	REV
21035														R Swenson	6/19/73			BRIA	4/19/73	3	11	D	21035	B

OCT CTL 0030-1-23-73

PRODUCT NO. 21035

DEVELOPMENT REV. D4

FLAG STORAGE

+5V

B145 A14F

B146 A14F

+3.5V

B147 150

D145 10µf

B129 1K

+VB129 → SH3-D16

SHI-H14 WOSC P5 (30) -FLAG 9 — D128 150 — D131 (7404) — E131 (7404) — B131 9314 S/R

SHI-H14 WOSC P5 (28) -FLAG 8 — D127 150 — D131 (7404) — E131 (7404) — B131 9314 S/R

SHI-H14 WOSC P5 (27) -FLAG 5 — D139 150 — D131 (7404) — E131 (7404) — B131 9314 S/R

SHI-H14 WOSC P5 (29) -FLAG 4 — D138 150 — D131 (7404) — E131 (7404) — B131 9314 S/R

SHI-K2 PROC P3 (6) +FLAG CLK — B144 (7404) — B144 (7404) — B144 (7404) → CLK

SHI-C4 -GEN CLR

SH6-L3 -CLR FLAG STORAGE 12 — A146 7400

B131 9314 outputs:

- Q → +STATUS IN 9 → SH5-H16
- Q → B144 (7404) → -STATUS IN 8 → (12) P1 DISP SH2-D16; +STATUS IN 8 → SH5-G16
- Q → B144 (7404) → -STATUS IN 5 → SH5-L8; -STATUS IN 5 → (27) P3 PROC SH7-K16
- Q → +STATUS IN 4 → SH5-K8
- CLR → B144 (7404) → C

SHI-H14 WOSC P4 (20) -STATUS IN 11 — D98 150 — D90 (7404)
- → -STATUS IN 11 → (26) P1 DISP SH2-E16
- → +STATUS IN 11 → SH5-K16

SHI-H14 WOSC P5 (3) -STATUS IN 10 — D125 150 — D117 (7404)
- → -STATUS IN 10 → (28) P1 DISP SH2-D16
- → +STATUS IN 10 → SH5-K16

SHI-H14 WOSC P4 (2) -STATUS IN 7 — D88 150 — D90 (7404)
- → -STATUS IN 7 → (24) P1 DISP SH2-E16
- → +STATUS IN 7 → SH5-E16

SHI-H14 WOSC P4 (27) -STATUS IN 6 — D102 150C — D104 (7404)
- → -STATUS IN 6 → (2) P1 DISP SH2-E16
- → +STATUS IN 6 → SH5-D16

+3.5 V → SH3-F16

SHI-J14 WOSC P4 (24) -PARALLEL DATA IN 9 — D86 150 — D104 (7404) → +PARALLEL DATA IN 9 → SH5-H16

SHI-J14 WOSC P4 (22) -PARALLEL DATA IN 8 — D112 150 — D104 (7404) → +PARALLEL DATA IN 8 → SH5-G16

SHI-J14 WOSC P4 (23) -PARALLEL DATA IN 7 — D100 150 — D104 (7404) → +PARALLEL DATA IN 7 → SH5-E16

SHI-J14 WOSC P4 (25) -PARALLEL DATA IN 6 — D101 150 — D104 (7404) → +PARALLEL DATA IN 6 → SH5-D16

SHI-J14 WOSC P4 (17) -PARALLEL DATA IN 5 — D126 150 — D117 (7404) → +PARALLEL DATA IN 5 → SH5-L8

SHI-J14 WOSC P5 (1) -PARALLEL DATA IN 4 — D113 150 — D117 (7404) → +PARALLEL DATA IN 4 → SH5-K8

SHI-J14 WOSC P5 (2) -PARALLEL DATA IN 3 — D114 150 — D117 (7404) → +PARALLEL DATA IN 3 → SH5-H8

SHI-J14 WOSC P5 (5) -PARALLEL DATA IN 2 — D115 150 — D117 (7404) → +PARALLEL DATA IN 2 → SH5-G8

SHI-J14 WOSC P5 (8) -PARALLEL DATA IN 1 — D116 150 — D117 (7404) → +PARALLEL DATA IN 1 → SH5-E8

SHI-H14 WOSC P4 (26) -PARALLEL DATA IN Ø — D85 150 — D104 (7404) → +PARALLEL DATA IN Ø → SH5-D8

SHI-H14 WOSC P5 (7) -STATUS IN 3 — B127 150 — D131 (7404) → +STATUS IN 3 → SH5-H8

SHI-H14 WOSC P5 (4) -STATUS IN 2 — B95 150 — D90 (7404) → +STATUS IN 2 → SH5-G8

SHI-G14 WOSC P4 (4) -STATUS IN 1 — D87 150 — D90 (7404)
- → -STATUS IN 1 → (30) P1 DISP SH2-C16
- → +STATUS IN 1 → SH5-E8

SHI-G14 WOSC P4 (16) -STATUS IN Ø — D97 150 — D90 (7404) → +STATUS IN Ø → SH5-D8

I/O

Diablo Systems Incorporated
Hayward, California 94545

TITLE: LOGIC DIAGRAM
LINE RECEIVERS & FLAG STORAGE
I/O LOGIC BOARD

MODEL: 500 PROGRAMMABLE TESTER

PROPRIETARY INFORMATION: UNAUTHORIZED DISCLOSURE OR USE PROHIBITED. SYSTEM LOGIC NO.

PRODUCT NO.	REFERENCE DESIGNATORS NOT USED	REFERENCE DESIGNATORS LAST USED	REV J E.C.O. NO.	REV H E.C.O. NO.	REV G E.C.O. NO.	REV F E.C.O. NO.	REV E E.C.O. NO.	REV D E.C.O. NO.	REV C E.C.O. NO.	REV B E.C.O. NO.	REV A E.C.O. NO.	MFG	DATE	ENG	DATE	CHECKED	DATE	DRAWN	DATE	SHEET	TOTAL SHEETS	SIZE	PRODUCT NO.	REV
21035										4761	3905			R. Swenson	6/9/73			BRIA	1-25-73	4	11	D	21035	B

DCT CTL 0020, 1-23-73

PRODUCT NO. 21035

DEVELOPMENT REV. D4

SH1-K4 DISP P1 (21) +SW REG B11
SH2-L3 +DATA OUTPUT REG 11
SH4-D10 +STATUS IN 11
SH1-J4 DISP P1 (6) +SW REG B10
SH2-L3 +DATA OUTPUT REG 10
SH4-D10 +STATUS IN 10

F60 DM8214 2X4-BIT MPLXR
10 11 12 13 6 5 4 3
14 SEL A
2 SEL B
1 STB 1
15 STB 2
9 +B11 (3) P3 PROC SH4-K17
7 +B10 (4) P3 PROC SH4-K17

SH1-J4 DISP P1 (23) +SW REG B9
SH2-K3 +DATA OUTPUT REG 9
SH4-L3 +PARALLEL DATA IN 9
SH4-H10 +STATUS IN 9
SH1-H4 DISP P1 (20) +SW REG B8
SH2-K3 +DATA OUTPUT REG 8
SH4-K3 +PARALLEL DATA IN 8
SH4-H10 +STATUS IN 8

E60 DM8214 2X4-BIT MPLXR
10 11 12 13 6 5 4 3
14 SEL A
2 SEL B
1 STB 1
15 STB 2
9 +B9 (1) P3 PROC SH4-K17
7 +B8 (2) P3 PROC SH4-J17

SH1-H4 DISP P1 (29) +SW REG B7
SH2-H3 +DATA OUTPUT REG 7
SH4-K3 +PARALLEL DATA IN 7
SH4-C10 +STATUS IN 7
SH1-G4 DISP P1 (22) +SW REG B6
SH2-H3 +DATA OUTPUT REG 6
SH4-J3 +PARALLEL DATA IN 6
SH4-B10 +STATUS IN 6

D60 DM8214 2X4-BIT MPLXR
10 11 12 13 6 5 4 3
14 SEL A
2 SEL B
1 STB 1
15 STB 2
9 +B7 (10) P3 PROC SH4-H17
7 +B6 (7) P3 PROC SH4-H17

SH3-D2 PROC P3 (26) +ADDR 1A
SH3-F2 PROC P3 (23) +ADDR 2A
SH3-G2 PROC P2 (20) +ADDR 4
SH3-L2 PROC P2 (18) +INPUT SEL

F47 7400
9 10 8
5 4 6

SH1-G4 DISP P1 (33) +SW REG B5
SH2-G3 +DATA OUTPUT REG 5
SH4-H3 +PARALLEL DATA IN 5
SH4-G10 -STATUS IN 5
SH1-F4 DISP P1 (4) +SW REG B4
SH2-G3 +DATA OUTPUT REG 4
SH4-H3 +PARALLEL DATA IN 4
SH4-F10 +STATUS IN 4

F75 DM8214 2X4-BIT MPLXR
10 11 12 13 6 5 4 3
14 SEL A
2 SEL B
1 STB 1
15 STB 2
9 +B5 (34) P3 PROC SH4-G17
+B4 (30) P3 PROC SH4-G17

SH1-F4 DISP P1 (31) +SW REG B3
SH2-E3 +DATA OUTPUT REG 3
SH4-G3 +PARALLEL DATA IN 3
SH4-E3 +STATUS IN 3
SH1-E4 DISP P1 (34) +SW REG B2
SH2-E3 +DATA OUTPUT REG 2
SH4-G3 +PARALLEL DATA IN 2
SH4-E3 +STATUS IN 2

E75 DM8214 2X4-BIT MPLXR
10 11 12 13 6 5 4 3
14 SEL A
2 SEL B
1 STB 1
15 STB 2
9 +B3 (31) P3 PROC SH4-E17
+B2 (32) P3 PROC SH4-D17

SH1-E4 DISP P1 (32) +SW REG B1
SH2-D3 +DATA OUTPUT REG 1
SH4-F3 +PARALLEL DATA IN 1
SH4-D3 +STATUS IN 1
SH1-D4 DISP P1 (16) +SW REG B0
SH2-D3 +DATA OUTPUT REG 0
SH4-F3 +PARALLEL DATA IN 0
SH4-C3 +STATUS IN 0

D75 DM8214 2X4-BIT MPLXR
10 11 12 13 6 5 4 3
14 SEL A
2 SEL B
1 STB 1
15 STB 2
9 +B1 (33) P3 PROC SH4-D17
7 +B0 (12) P3 PROC SH4-C17

+ADDR 1A SH6-G16
+ADDR 2A SH6-H16

I/O

Diablo Systems Incorporated
Hayward California 94545

TITLE LOGIC DIAGRAM
INPUT MULTIPLEXER
I/O LOGIC BOARD

MODEL 500 PROGRAMMABLE TESTER

PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED.

SYSTEM LOGIC NO.

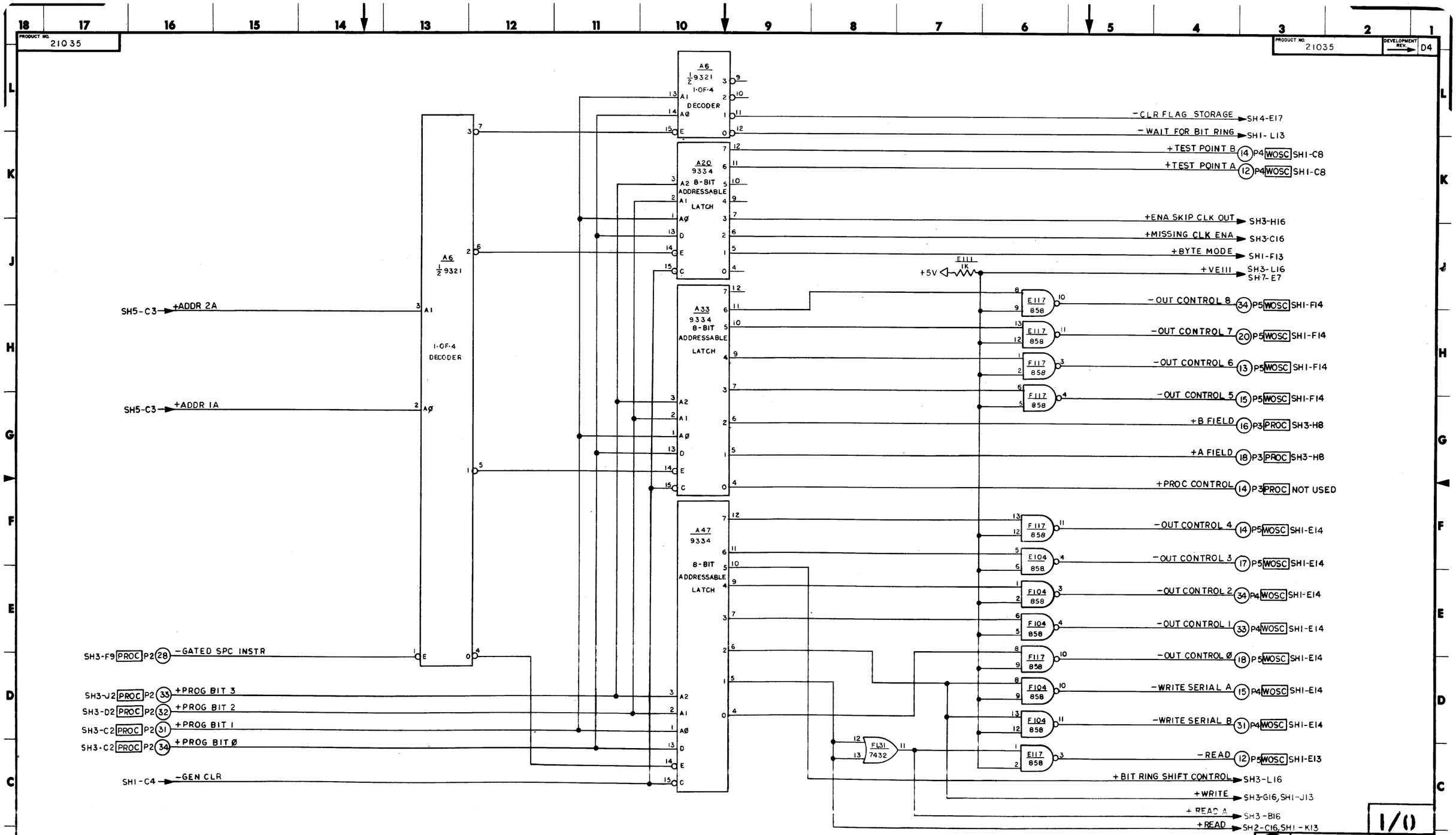
PRODUCT NO.	REFERENCE DESIGNATORS NOT USED	REFERENCE DESIGNATORS LAST USED
21035		

DCT CTL 0030, (-23-73

REV J	REV H	REV G	REV F	REV E	REV D	REV C	REV B	REV A
E.C.O. NO.	E.C.O. NO.	E.C.O. NO.	E.C.O. NO.	E.C.O. NO.	E.C.O. NO.	E.C.O. NO.	E.C.O. NO. 4761	E.C.O. NO. 3905

MFR	DATE	ENG	DATE	CHECKED	DATE	DRAWN	DATE
		R Sussman	6/19/73			BRIA	4-26-73

SHEET	TOTAL SHEETS	SIZE	PRODUCT NO.	REV.
5	11	D	21035	B



PRODUCT NO. 21035

PRODUCT NO. 21035 DEVELOPMENT REV. D4

I/O

Diablo Systems Incorporated
Hayward, California 94545

TITLE: LOGIC DIAGRAM
SPECIAL FUNCTION DECODER
I/O LOGIC BOARD

MODEL: 500 PROGRAMMABLE TESTER

PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED

SYSTEM LOGIC NO.

PRODUCT NO	REFERENCE DESIGNATORS NOT USED	REFERENCE DESIGNATORS LAST USED	REV	ECO NO	REV	ECO NO	REV	ECO NO	REV	ECO NO	REV	ECO NO	REV	ECO NO	REV	ECO NO	REV	ECO NO	MFG	DATE	ENG	DATE	CHECKED	DATE	DRAWN	DATE	SHEET	TOTAL SHEETS	SIZE	PRODUCT NO	REV
21035			J		H		G		F		E		D		C		B	4761	A	3905			R Sverna	6/29/73			BRIA	5-2-73	6	11	D	21035	B

DISPLAY REGISTER B

SH1-L4 +A11 → 14 D Q F20 74174 15 → +DISP REG B11 (7) P1 DISP SH2-J11
SH1-L4 +A10 → 13 D Q F20 12 → +DISP REG B10 (15) P1 DISP SH2-J11
SH1-K4 +A9 → 11 D Q F20 10 → +DISP REG B9 (19) P1 DISP SH2-H11
SH1-K4 +A8 → 6 D Q F20 7 → +DISP REG B8 (18) P1 DISP SH2-H11
SH1-H4 +A7 → 4 D Q F20 5 → +DISP REG B7 (14) P1 DISP SH2-G11
SH1-H4 +A6 → 3 D Q F20 2 → +DISP REG B6 (8) P1 DISP SH2-G11
SH1-G4 +A5 → 14 D Q E20 74174 15 → +DISP REG B5 (11) P1 DISP SH2-F11
SH1-G4 +A4 → 13 D Q E20 12 → +DISP REG B4 (27) P1 DISP SH2-F11
SH1-E4 +A3 → 11 D Q E20 10 → +DISP REG B3 (25) P1 DISP SH2-E11
SH1-E4 +A2 → 6 D Q E20 7 → +DISP REG B2 (17) P1 DISP SH2-E11
SH1-D4 +A1 → 4 D Q E20 5 → +DISP REG B1 (13) P1 DISP SH2-D11
SH1-D4 +AØ → 3 D Q E20 2 → DISP REG BØ (9) P1 DISP SH2-D11

1 C
9 CLK

SH1-C4 -GEN CLR
SH1-F4 -B CLK → 9, 10 E6 7432 8 → SH7-E3 PROC P2 (12) -LOAD DISP REG B

PARALLEL DATA OUTPUT DRIVERS

SH2-K9 +DATA INPUT REG 8 → 1, 2 E104 858 3 → -DATA OUT 8 (32) P4 WOSC SH1-G14
SH2-H9 +DATA INPUT REG 7 → 13, 12 F90 858 11 → -DATA OUT 7 (7) P4 WOSC SH1-G14
SH2-H9 +DATA INPUT REG 6 → 8, 9 F90 858 10 → -DATA OUT 6 (11) P4 WOSC SH1-G14
SH2-G9 +DATA INPUT REG 5 → 6, 5 F90 858 4 → -DATA OUT 5 (8) P4 WOSC SH1-G14
SH2-G9 +DATA INPUT REG 4 → 1, 2 F90 858 3 → -DATA OUT 4 (6) P4 WOSC SH1-F14
SH2-E9 +DATA INPUT REG 3 → 13, 12 F90 858 11 → -DATA OUT 3 (21) P4 WOSC SH1-F14
SH2-E9 +DATA INPUT REG 2 → 8, 9 F90 858 10 → -DATA OUT 2 (19) P4 WOSC SH1-F14
SH2-D9 +DATA INPUT REG 1 → 6, 5 F90 858 4 → -DATA OUT 1 (9) P4 WOSC SH1-F14
SH2-D9 +DATA INPUT REGØ → 1, 2 F90 858 3 → -DATA OUT Ø (5) P4 WOSC SH1-F14

SH6-J4 +VEIII

SH1-G9 DISP P1 (3) +SW REG A5 → +SW REG A5 (8) P3 PROC SH5-L8
SH1-F9 DISP P1 (1) +SW REG A4 → +SW REG A4 (5) P3 PROC SH5-K8

I/O

Diablo Systems Incorporated
Hayward California 94545

TITLE: LOGIC DIAGRAM
DISPLAY REG B & OUTPUT DRIVERS
I/O LOGIC BOARD
MODEL: 500 PROGRAMMABLE TESTER

PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED. SYSTEM LOGIC NO.

PRODUCT NO.	SHEET	TOTAL SHEETS	SIZE	PRODUCT NO.	REV
21035	7	11	D	21035	B

REV	ECO NO	DATE	ENG	DATE	CHECKED	DATE	DRAWN	DATE
J								
H								
G								
F								
E								
D								
C								
B	4761		R Swenson	6/29/73			BRIA	5-2-73
A	3905							

REFERENCE DESIGNATORS NOT USED
REFERENCE DESIGNATORS LAST USED

PRODUCT NO. 21031

PRODUCT NO. 21031 DEVELOPMENT REV. D3

NOTES; UNLESS OTHERWISE SPECIFIED.
1. ALL RESISTOR VALUES ARE IN OHMS(Ω) ±5% 1/4 WATT.
2. ALL CAPACITANCES ARE IN MICROFARADS(μF)
3. MNEMONICS IN ENCLOSED BOXES REFER TO SOURCE OR DESTINATION OF INTERBOARD SIGNALS, AS PER
   I/O = I/O LOGIC BOARD PART NO. 21035
   DISP = DISPLAY BOARD PART NO. 21033

SPARE GATES

B142 7400

DISPLAY BOARD

SH1-J9 DISP — CLR PB GND — E31

PUSHBUTTON SWITCHES

PROGRAM RESET — E2 PR

GENERAL CLEAR — E1 GC

TOGGLE SWITCHES ON FRONT PANEL

FULL DENSITY / HALF DENSITY — E4 GND, E3 HD, E5 FD

2541 1562 1440

E6 XTAL — A94 — A104 — A114 — A124 10,164MHZ — A134 6.248MHZ — A144 5,760MHZ

P8 50 PIN FRONT PANEL CONNECTOR

SIGNAL NAME	FRONT PANEL CONNECTOR PIN	WRITE OSC (AND I/O BOARD) CONNECTOR & PIN	I/O BOARD REFERENCE
PARALLEL DATA IN 9	FF	P4-24	SH4-L7
PARALLEL DATA IN 8	EE	P4-28	SH4-K7
PARALLEL DATA IN 7	DD	P4-23	SH4-K7
PARALLEL DATA IN 6	CC	P4-25	SH4-J7
PARALLEL DATA IN 5	d	P4-17	SH4-H7
PARALLEL DATA IN 4	v	P5-1	SH4-H7
PARALLEL DATA IN 3	n	P5-2	SH4-G7
PARALLEL DATA IN 2	k	P5-5	SH4-G7
PARALLEL DATA IN 1	j	P5-8	SH4-F7
PARALLEL DATA IN 0	c	P4-26	SH4-F7
STATUS IN 11	u	P4-20	SH4-D17
STATUS IN 10	P	P5-3	SH4-C17
FLAG 9	p	P5-30	SH4-H17
FLAG 8	y	P5-28	SH4-H17
STATUS IN 7	U	P4-2	SH4-C17
STATUS IN 6	F	P4-27	SH4-B17
FLAG 5	W	P5-27	SH4-G17
FLAG 4	Y	P5-29	SH4-F17
STATUS IN 3	M	P5-7	SH4-E7
STATUS IN 2	D	P5-4	SH4-E7
STATUS IN 1	z	P4-4	SH4-D7
STATUS IN 0	h	P4-16	SH4-C7
SERIAL IN CLOCK	A	P4-22	SH3-D16
SERIAL IN DATA	C	P5-32	SH3-F16
DATA OUT 8	m	P4-32	SH7-J3
DATA OUT 7	BB	P4-7	SH7-J3
DATA OUT 6	b	P4-11	SH7-H3
DATA OUT 5	T	P4-8	SH7-H3
DATA OUT 4	f	P4-6	SH7-G3
DATA OUT 3	X	P4-21	SH7-G3
DATA OUT 2	J	P4-19	SH7-F3
DATA OUT 1	s	P4-9	SH7-F3
DATA OUT 0	N	P4-5	SH7-E3
OUT CONTROL 8	L	P5-34	SH6-J3
OUT CONTROL 7	R	P5-20	SH6-H3
OUT CONTROL 6	V	P5-13	SH6-H3
OUT CONTROL 5	Z	P5-15	SH6-G6
O/T CONTROL 4	H	P5-14	SH6-F6
OUT CONTROL 3	AA	P5-17	SH6-F6
OUT CONTROL 2	w	P4-34	SH6-E6
OUT CONTROL 1	t	P4-33	SH6-E6
OUT CONTROL 0	a	P5-18	SH6-D6
WRITE SERIAL A	e	P4-15	SH6-D6
WRITE SERIAL B	K	P4-31	SH6-D6
READ	E	P5-12	SH6-C6
SERIAL DATA OUT	B	P5-16	SH3-J3
+5 Volts	r		
GND	S		
GND	x		
GND	HH		

+5V — A83 510 — A82 10 — B74 858 — A81 39 10V — B71 1K — B74 858 — B69 510

+5V — A77 2K — A78 10 — B74 858 — A79 39 10V — B76 1K — B74 858 — B78 510

-CLR PROG CNTR

-GEN CLR

FULL FREQUENCY F.F.

+5V — B130 1K — B116 470K — B122 330 — B124 .001 — B118 MPS2369 — B112 20 PF — B114 20 PF — B117 3.3 K — B119 MPS3640 — B123 1K — B132 CLK 7474

HALF FREQUENCY F.F.

+5V — B128 1K — +5V — B129 1K

B142 7400 — B142 7400 — B142 7400 — +DISK OSC

+5V — B72 .01 25V — B62 39 10V — GND

+TEST POINT A

+TEST POINT B

+READ SYNC DETECT

E17 TPD — E16 TPC — E15 TPB — E14 TPA — E13 GND

TEST POINTS ON FRONT PANEL

P5 — P4

P4 3	P4 1	P4 12	P4 14	P4 13	D	C	B	A	G	P5 19	P5 21	P5 22	P5 23	P5 24	P5 25
I/O SH3-G16	I/O SH1-B14	I/O SH6-K3	I/O SH6-K3	I/O SH3-C3						I/O SH3-J16	I/O SH3-J16	I/O SH3-J16	I/O SH3-J16	I/O SH3-J16	I/O SH3-J16

WOSC

Diablo Systems Incorporated
Hayward, California 94545

TITLE: LOGIC DIAGRAM WRITE OSCILLATOR BOARD

MODEL: 500 PROGRAMMABLE TESTER

PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED. SYSTEM LOGIC NO.

REV	E.C.O. NO.	DATE	ENG	DATE	CHECKED	DATE	DRAWN	DATE	SHEET	TOTAL SHEETS	SIZE	PRODUCT NO.	REV
J													
H													
G													
F													
E													
D													
C													
B	4760												
A	3905		R Sweeney 6/19/73				BRIA	5-9-73	1	4	D	21031	B

PRODUCT NO 21031 — REFERENCE DESIGNATORS NOT USED — REFERENCE DESIGNATORS LAST USED — DOC CTL 0020 1-29-73

PRODUCT NO. 21033

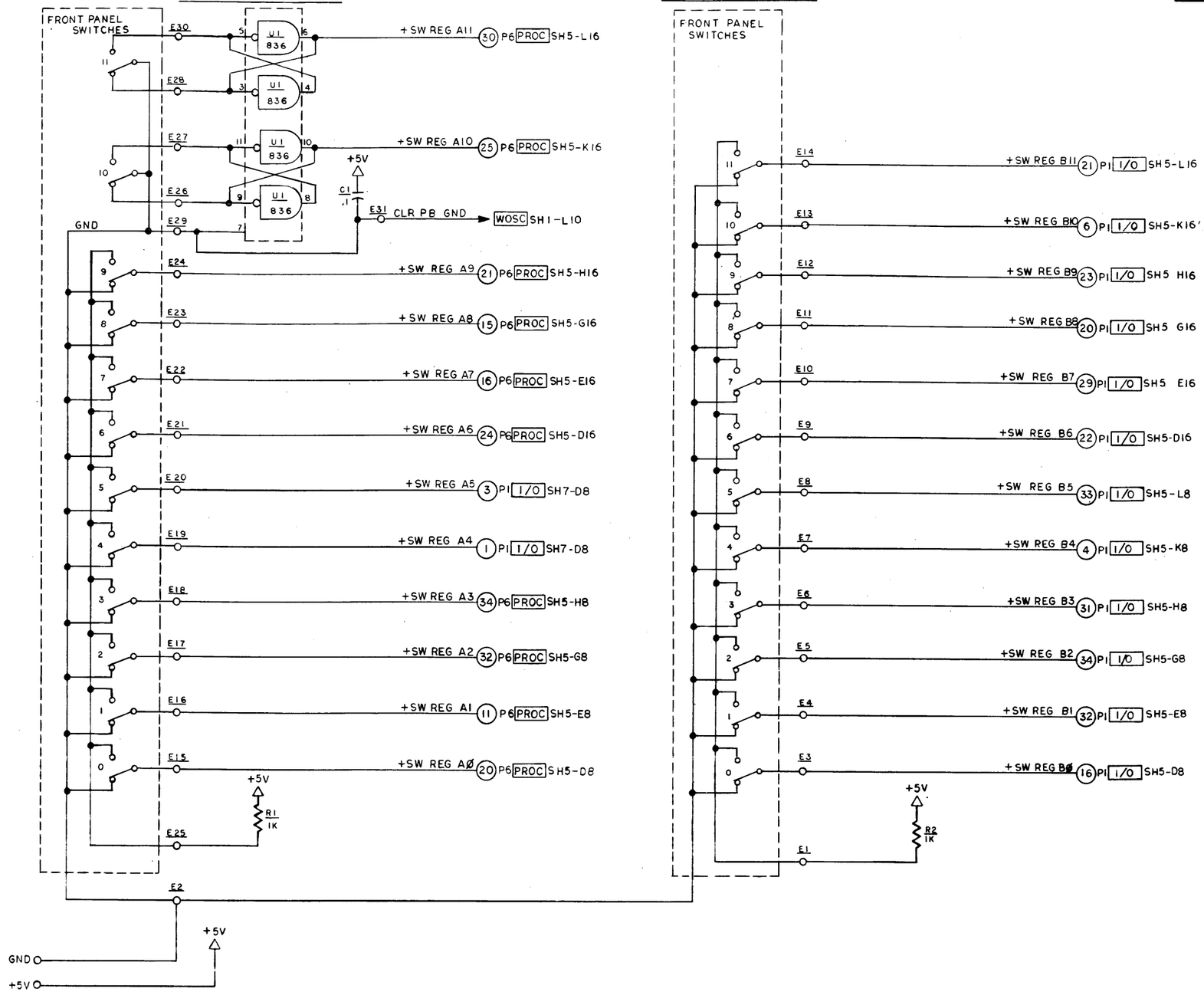
NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTOR VALUES ARE SPECIFIED IN OHMS(Ω) ±5% 1/4 WATT.
2. ALL CAPACITANCES ARE SPECIFIED IN MICROFARADS(μf)
3. MNEMONICS IN ENCLOSED BOXES REFER TO SOURCE OR DESTINATION OF INTERBOARD SIGNALS, AS PER,

PROC = PROCESSOR BOARD PART NO. 21037

I/O = I/O BOARD PART NO. 21035

WOSC = WRITE OSCILLATOR BOARD PART NO. 21031



PRODUCT NO. 21033 DEVELOPMENT REV. D3

DISP

Diablo Systems Incorporated
Hayward, California 94545

TITLE: LOGIC DIAGRAM SWITCH REGISTERS DISPLAY BOARD

MODEL: 500 PROGRAMMABLE TESTER

PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED. SYSTEM LOGIC NO.

SHEET	TOTAL SHEETS	SIZE	PRODUCT NO.	REV
1	4	D	21033	A

DRAWN	DATE	CHECKED	DATE	ENG	DATE	MFG	DATE	REV A	E.C.O. NO 3905	REV B	E.C.O. NO.	REV C	E.C.O. NO	REV D	E.C.O. NO.	REV E	E.C.O. NO.	REV F	E.C.O. NO.	REV G	E.C.O. NO	REV H	E.C.O. NO	REV J	E.C.O. NO.
BRIA	5-10-73			R. Simons	6/14/73																				

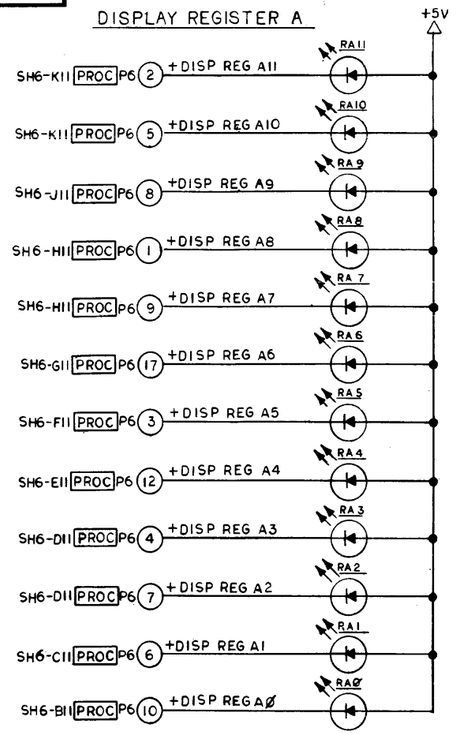
PRODUCT NO. 21033 | REFERENCE DESIGNATORS NOT USED | REFERENCE DESIGNATORS LAST USED

JCT CTL 0020, 1-23-73

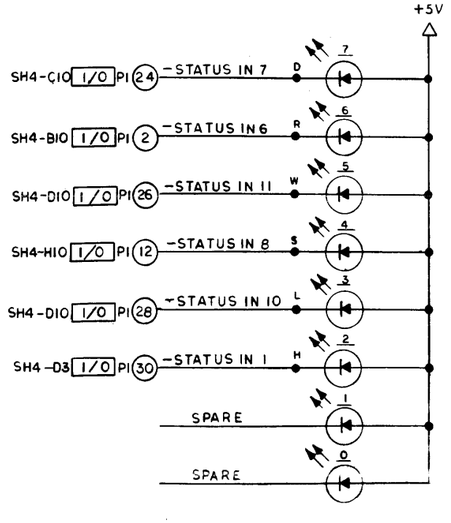
PRODUCT NO. 21033

PRODUCT NO. 21033 | DEVELOPMENT REV. D3

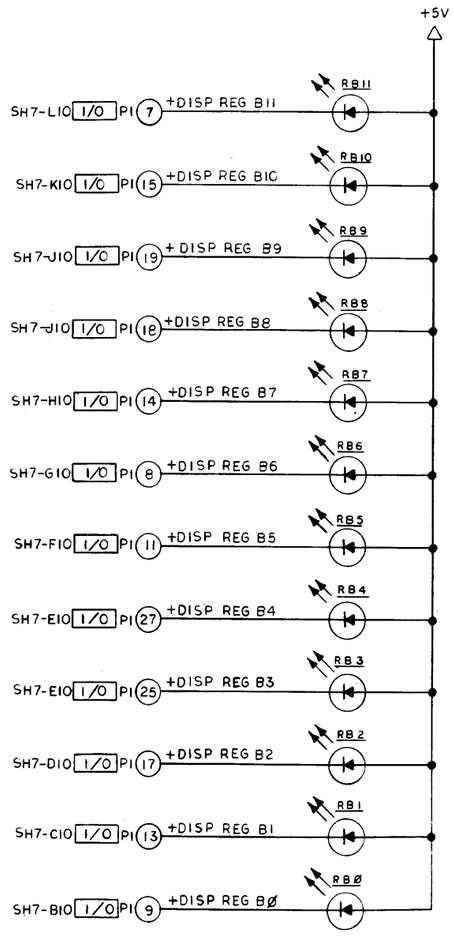
DISPLAY REGISTER A



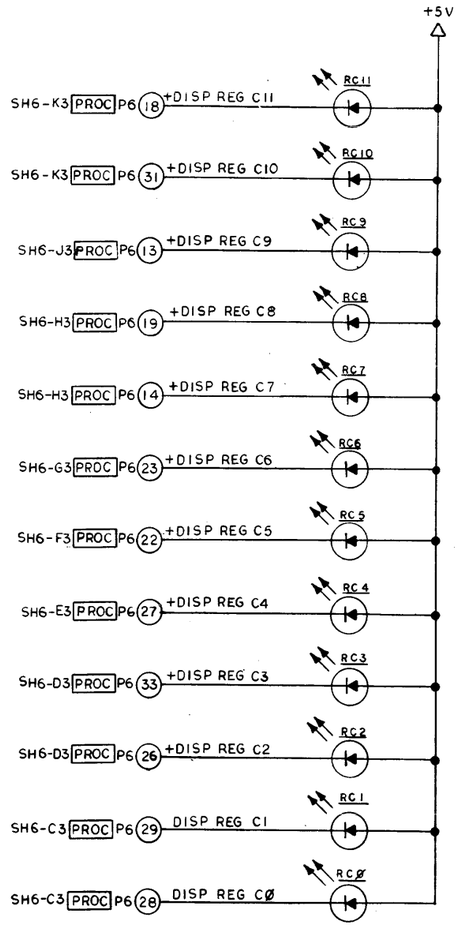
STATUS INDICATORS



DISPLAY REGISTER B



DISPLAY REGISTER C



DISP

Diablo Systems incorporated
Hayward California 94545

TITLE: LOGIC DIAGRAM
DISPLAY REGISTERS
DISPLAY BOARD

MODEL: 500 PROGAMMABLE TESTER

PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED.

SYSTEM LOGIC NO.

PRODUCT NO.	REFERENCE DESIGNATORS NOT USED	REFERENCE DESIGNATORS LAST USED	REV	ECO NO.	DATE	ENG	DATE	CHECKED	DATE	DRAWN	DATE	SHEET	TOTAL SHEETS	SIZE	PRODUCT NO.	REV
21033			A	3905		R Swenson	11-11-73			BRIA	5-11-73	2	4	D	21033	A

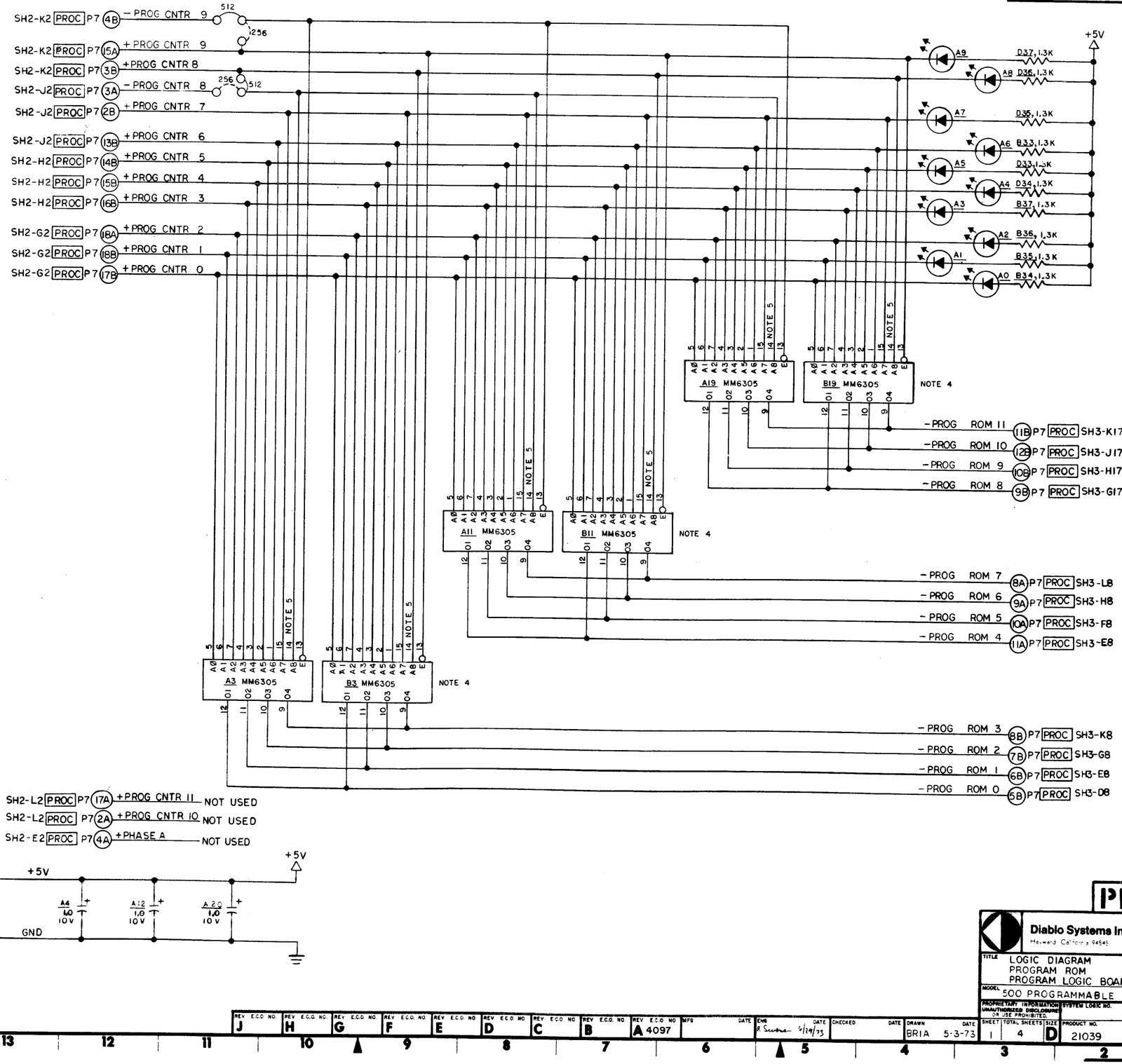
SST CTL 0089, 1-23-73

PRODUCT NO. 21039

PRODUCT NO. 21039 DEVELOPMENT REV. D3

NOTES; UNLESS OTHERWISE SPECIFIED

1. ALL RESISTOR VALUES ARE SPECIFIED IN OHMS(Ω) ±5% 1/4 WATT.
2. ALL CAPACITANCE SPECIFIED IN MICROFARADS(μf)
3. MNEMONICS IN ENCLOSED BOXES REFER TO SOURCE OR DESTINATION OF INTERBOARD SIGNALS; AS PER PROC = PROCESSOR BOARD PART NO. 21037
4. PROM TYPE NUMBERS SHOWN REFER TO TYPICAL UNPROGRAMMED PROMS. CONSULT PROGRAM MANUAL FOR DESCRIPTIONS AND PART NUMBERS OF ROMS USED BY EACH PARTICULAR PROGRAM.
5. IF 512 X 4 BIT PROMS (MM6305 OR EQUAL) ARE USED FOR PROGRAM STORAGE, INSTALL 2 JUMPERS MARKED "512". IF 256 X 4 BIT PROMS (MM6300 OR EQUAL) ARE USED, INSTALL 2 JUMPERS MARKED "256". WITH THE "256" JUMPERS INSTALLED, PIN 14 OF EACH PROM BECOMES A LOW-ACTIVE ENABLE, HAVING THE SAME CHARACTERISTICS AS PIN 13.



PRGM

Diablo Systems Incorporated
Hayward, California 94545

TITLE: LOGIC DIAGRAM
PROGRAM ROM
PROGRAM LOGIC BOARD

MODEL: 500 PROGRAMMABLE TESTER

PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED.

SYSTEM LOGIC NO.

SHEET	TOTAL SHEETS	SIZE	PRODUCT NO.	REV
1	4	D	21039	A

DRAWN BRIA 5-3-73 | CHECKED | ENG R Sievers 6/29/73

REV	ECO NO.
J	
H	
G	
F	
E	
D	
C	
B	
A	4097

MFG DATE

PRODUCT NO. 21039

REFERENCE DESIGNATORS NOT USED

REFERENCE DESIGNATORS LAST USED

SCY CTL 0080, 1-23-73

PRODUCT NO. 21039

DEVELOPMENT REV. D3

SH2-J11 PROC P7 23A +STACK ADDR REG 7
SH2-H11 PROC P7 23B +STACK ADDR REG 6
SH2-H11 PROC P7 24A +STACK ADDR REG 5
SH2-G11 PROC P7 24B +STACK ADDR REG 4
SH2-F11 PROC P7 25B +STACK ADDR REG 3
SH2-E11 PROC P7 28B +STACK ADDR REG 2
SH2-E11 PROC P7 27B +STACK ADDR REG 1
SH2-D11 PROC P7 26B +STACK ADDR REG Ø

D3 MM 6300 NOTE 4
D11 MM 6300 NOTE 4
D19 MM 6300 NOTE 4

+5V

D31 510 +STACK ROM 11 19B P7 PROC SH5-K16
B32 510 +STACK ROM 10 20B P7 PROC SH5-K16
B30 510 +STACK ROM 9 21B P7 PROC SH5-H16
B28 510 +STACK ROM 8 22B P7 PROC SH5-G16
D32 510 +STACK ROM 7 19A P7 PROC SH5-E16
B31 510 +STACK ROM 6 20A P7 PROC SH5-D16
B27 510 +STACK ROM 5 21A P7 PROC SH5-L8
B29 510 +STACK ROM 4 22A P7 PROC SH5-K8
D30 510 +STACK ROM 3 28A P7 PROC SH5-H8
D27 510 +STACK ROM 2 27A P7 PROC SH5-G8
D28 510 +STACK ROM 1 26A P7 PROC SH5-E8
D29 510 +STACK ROM Ø 25A P7 PROC SH5-D8

PRGM

Diablo Systems Incorporated
Hayward, California 94545

TITLE: LOGIC DIAGRAM
DATA STACK ROM
PROGRAM LOGIC BOARD

MODEL: 500 PROGRAMMABLE TESTER

PROPRIETARY INFORMATION
UNAUTHORIZED DISCLOSURE
OR USE PROHIBITED.

SYSTEM LOGIC NO.

PRODUCT NO 21039 | REV A

PRODUCT NO	REFERENCE DESIGNATORS NOT USED	REFERENCE DESIGNATORS LAST USED	REV J ECO NO	REV H ECO NO	REV G ECO NO	REV F ECO NO	REV E ECO NO	REV D ECO NO	REV C ECO NO	REV B ECO NO	REV A ECO NO 4097	MFG	DATE	ENG	DATE	CHECKED	DATE	DRAWN	DATE	SHEET	TOTAL SHEETS	SIZE
21039														R Swenson	6/29/73			BRIA	5-3-73	2	4	D

DOC STL 0028 1-23-73

PRODUCT NO. 21066

PRODUCT NO. 21066 DEVELOPMENT REV. D1

NOTES; UNLESS OTHERWISE SPECIFIED.

1. ALL RESISTOR VALUES ARE SPECIFIED IN OHMS (Ω) ARE ±5% 1/4 WATT
2. CAPACITANCES ARE SPECIFIED IN MICROFARADS (μf)
3. Q1, Q2, OF REGULATOR BOARD ARE MOUNTED ON HEATSINK BEHIND PC BOARD. LEADS ATTACHED TO PC BOARD.
4. LOGIC GND NOT CONNECTED TO SAFETY GND.
5. CHASSIS CONNECTED TO SAFETY GND.
6. CR3, CR4 MOUNTED ON HEATSINK.
7. CR1 POWER ON INDICATOR LED INCLUDES BUILT-IN CURRENT-LIMITING RESISTOR.

HEATSINK ASSY PART NO. 20904

POWER SUPPLY POWERTEC MODEL 2C5-6 (REPACKAGED)

REGULATOR BOARD

P1 BLK GRN WHT — S1A — S1B — F1 — NOTE 4 & 5

T1

B1 FAN

CR1 S1-2 — CR2 S1-2 — C1 1000 15V

R1 10 5W — C4 .01 100V

Q1 2N3055 — Q3 2N2219A — R2 130

R3 .05 5W — Q2 2N3055 NOTE 3

HEATSINK

TI-5 — TI-3 — TI-4

R5 1K — R9 560 — R10 500 CW

R6 18K — Q5 2N2905A — R7 100

CR5 IN4735A — C5 1000 15V — R11 620

R8 100 — Q4 2N2219A — R4 750

NOTE 6

CR3 IN1200 — CR4 IN1200 — C2 9000 15V — C3 9000 15V

CR3,4-A

OVERVOLTAGE PROTECTOR POWERTEC OVP-1

R4 330 — R3 470 — C1 1 50V

CR2 IN752A — Q1 2N2907A — R1 120 — CR1 2N4441 — R2 1K

R5 1.5K CTS 111 CW

(+) OUT — +5V ORG — +5V — +5V — +5V — +5V — +5V — +5V

NOTE 7 PWR ON — CR1 — FRONT PANEL

WOSC — DISP — I/O — PROC

GND — BLK — NOTE 4 — GND — GND — GND — GND — GND — GND

(−) OUT

Diablo Systems Incorporated
Hayward California 94545

TITLE: SCHEMATIC DIAGRAM POWER SUPPLY & DC POWER DISTRIBUTION

MODEL: 500 PROGRAMMABLE TESTER

PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED.

SYSTEM LOGIC NO.

SHEET 1 TOTAL SHEETS 1 SIZE D — PRODUCT NO 21066 — REV A

DRAWN BR1A 5-18-73 — ENG R Swenson 6/27/73 — CHECKED — DATE

REV	ECO NO	DATE
A	4097	

PRODUCT NO 21066 — REFERENCE DESIGNATORS NOT USED — REFERENCE DESIGNATORS LAST USED

DOT CTL 0020, 1-25-73