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PRELIMINARY

Diablo Systems Incorporated
A Xerox Company

HyTerm Communications Terminal

Model 1660

Maintenance Manual

400083-01 Rev. B

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PREFACE

This manual contains only Theory of Operation (Section 2) and Maintenance (Section 3) information, and schematics and logic drawings (Section 4). Refer to the Product Description manual, no. 400082, for operation instructions, specifications, functional description, interface information and installation instructions.

This is a preliminary edition. Comments and suggestions on this manual and its use are welcome. Please complete the pre-addressed comment card bound in the back of this manual. Your cooperations is appreciated.

Diablo Systems, Inc., reserves the right to make improvements to products without incurring any obligation to incorporate such improvements in units previously sold.

WARRANTY

The Diablo HyTerm Communications Terminal Model 1641 is warranted against defects in materials and workmanship for 90 days from the date of shipment. Any questions with respect to the warranty should be directed to your Diablo sales represenative. All requests for repairs should be directed to the Diablo repair depot in your area. This will assure you of the fastest possible service.

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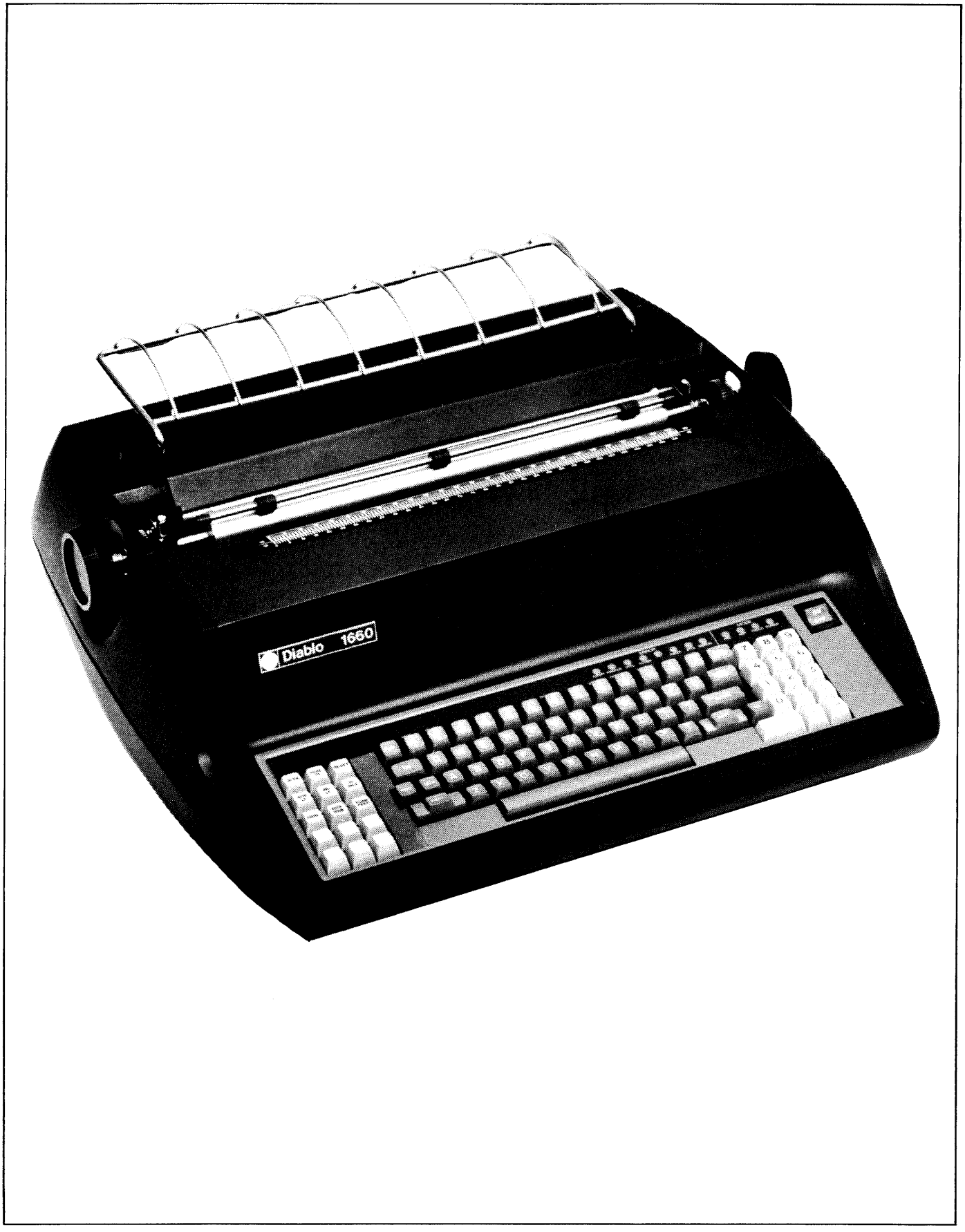


Figure 1-1. Model 1660 HyTerm Communications Terminal

Section 1
INTRODUCTION

1.1 GENERAL DESCRIPTION

The Diablo Model 1660 HyTerm Communications Terminal (see Figure 1-1) combines the field-proven Series 2300 Matrix Printer with 1) an integral power supply, 2) additional microprocessor control and Read-Only Memory/Random Access Memory (ROM/RAM), and 3) an Electronic Industries Association RS-232-C interface, to produce a fully-contained data communications terminal that is similar in size and mobility to the ordinary wide-carriage office typewriter. In the local mode of operation, the Model 1660 HyTerm will serve as a desktop document writer for correspondence and other secretarial functions. When used as a data communications terminal, the Model 1660 HyTerm transmits and receives asynchronous serial data over a communications link from a distant computer or data terminal. In this remote mode of operation, the Model 1660 HyTerm may also be used as a computer console or similar I/O device for data entry and data editing. In addition, the Model 1660 HyTerm is ideally suited for computer applications where a hard-copy printout is required on multi-copy forms.

The Model 1660 HyTerm utilizes a 9-wire print head and serial impact to construct characters in a 7 x 9 dot matrix. The matrix printer is capable of printing characters at a maximum speed of 200 characters per second (cps). The microprocessor control and ROM/RAM memory facilitate such features as motion accumulation, high speed horizontal and vertical tabbing, automatic reverse line printing, and complete local and remote control of all printer functions.

1.2 SCOPE

This manual provides information on theory of operation, maintenance, and module replacement. It also includes data covering the electronic components used and explanations of the logic symbology and drawing conventions used. It does not include operating instructions, installation procedures, or information on the functional operation of the HyTerm; these are all contained in the Product Description manual listed in the related documents.

1.3 RELATED DOCUMENTS

(1) HYTERM COMMUNICATIONS TERMINAL MODEL 1660, PRODUCT DESCRIPTION. Diablo Systems, Inc. Publication No. 400082-01.

(2) SERIES 2300 MATRIX PRINTER PARTS CATALOG. Diablo Systems, Inc. Publication No. 82414-01.

(3) INTERFACE BETWEEN DATA TERMINAL EQUIPMENT AND DATA COMMUNICATION EQUIPMENT EMPLOYING SERIAL BINARY DATA INTERCHANGE. EIA Standard RS-232-C, August, 1969. Engineering Dept., Electronic Industries Assn., 201 Eye St. N.W., Washington, D.C. 20006.

(4) AMERICAN STANDARD CODE FOR INFORMATION INTERCHANGE. USAS X3.4-1977. American National Standards Institute, 1430 Broadway, New York, N.Y. 10018.

(5) DATA SET 103A INTERFACE SPECIFICATION. February, 1967, Engineering Director, Data Communications, American Telephone and Telegraph Co. Publication 41101.

(6) DATA SET 202C and 202D INTERFACE SPECIFICATION. May, 1964, Engineering Director, Data Communications, American Telephone and Telegraph Co., Publication 41202.

(7) Data Set 212A Interface Specification. October, 1976. Director, Data and Special Services, American Telephone and Telegraph Co.

(8) C.C.I.T.T. GREEN BOOK, VOL. VIII, DATA TRANSMISSION, 1973. The International Telephone and Telegraph Consultative Committee, International Telecommunication Union, Geneva, Switzerland.

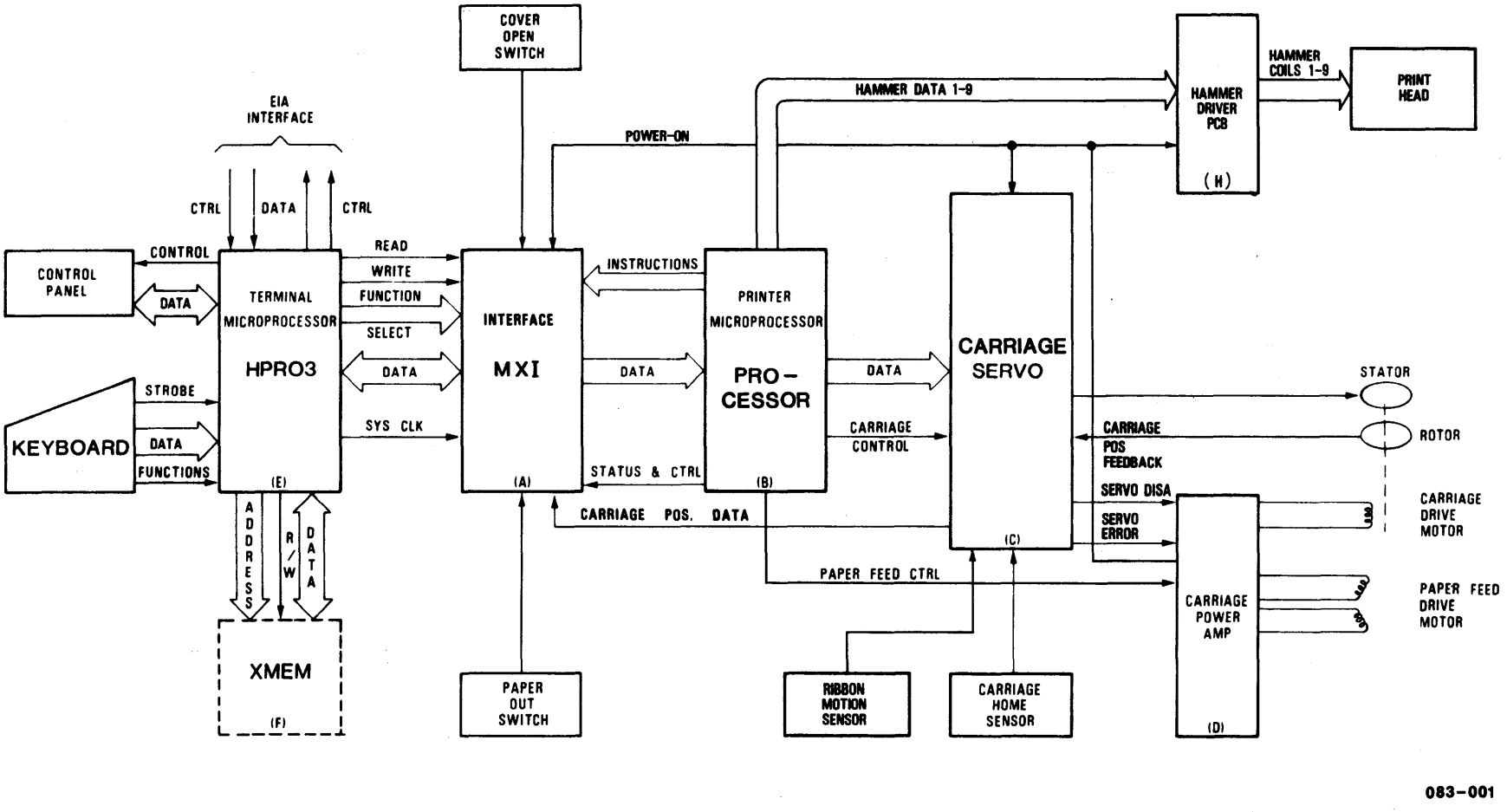


Figure 2-1. Model 1660 HyTerm System Block Diagram

Section 2
THEORY OF OPERATION

2.1 INTRODUCTION (Figure 2-1)

The 1660 employs two separate, asynchronous, processing systems. One, called the "printer microprocessor," is an integral part of all HyType printers. The other, called the "terminal microprocessor," provides the additional functions that transform a matrix printer into a 1660 communications terminal.

The terminal microprocessor, located on the HPRO3 board, controls the overall terminal functions of sending and receiving data over the EIA interface, receiving data from the keyboard, and monitoring the control panel. It also communicates with the printer microprocessor, contained on the PROCESSOR board. This second microprocessor system initiates movement of the printer carriage and paper feed drive motor, and it monitors feedback from the carriage position circuit to effect proper execution of these motion commands. It also issues hammer-fire instructions to the hammer driver board, it provides printer status information to the terminal microprocessor, and it performs other "housekeeping" functions.

The XMEM board is not part of all 1660 terminals. It is used during engineering development, in early production models, and for options when requirements exceed the memory available on the HPRO3 board.

The MATRIX INTERFACE board is located logically between the two microprocessors. It provides temporary storage for data and status information, and synchronizes the transfer of data from the terminal microprocessor to the printer microprocessor, and the transfer of status information back. It also contains some control logic for the servo feedback system.

The CARRIAGE SERVO board receives the carriage motion commands from the printer microprocessor in digital form and converts these to analog signals represenatitive of the distance and direction to be moved. These servo "error" signals are passed on to the carriage power amplifiers, which drive their respective servo motors. Feedback signals, derived from the carriage rotary transducers, are amplified and passed on to the MATRIX INTERFACE board. Here they are available to the printer microprocessor, which uses them to regulate the error signals.

The HAMMER DRIVER board provides nine identical driver circuits for driving each of the nine print head hammers and a hammer protection circuit.

The CARRIAGE POWER AMPLIFIER drives the carriage servo motor and the paper feed step motor. It also monitors the input voltages and develops the POWER ON signal to initiate the Restore operation.

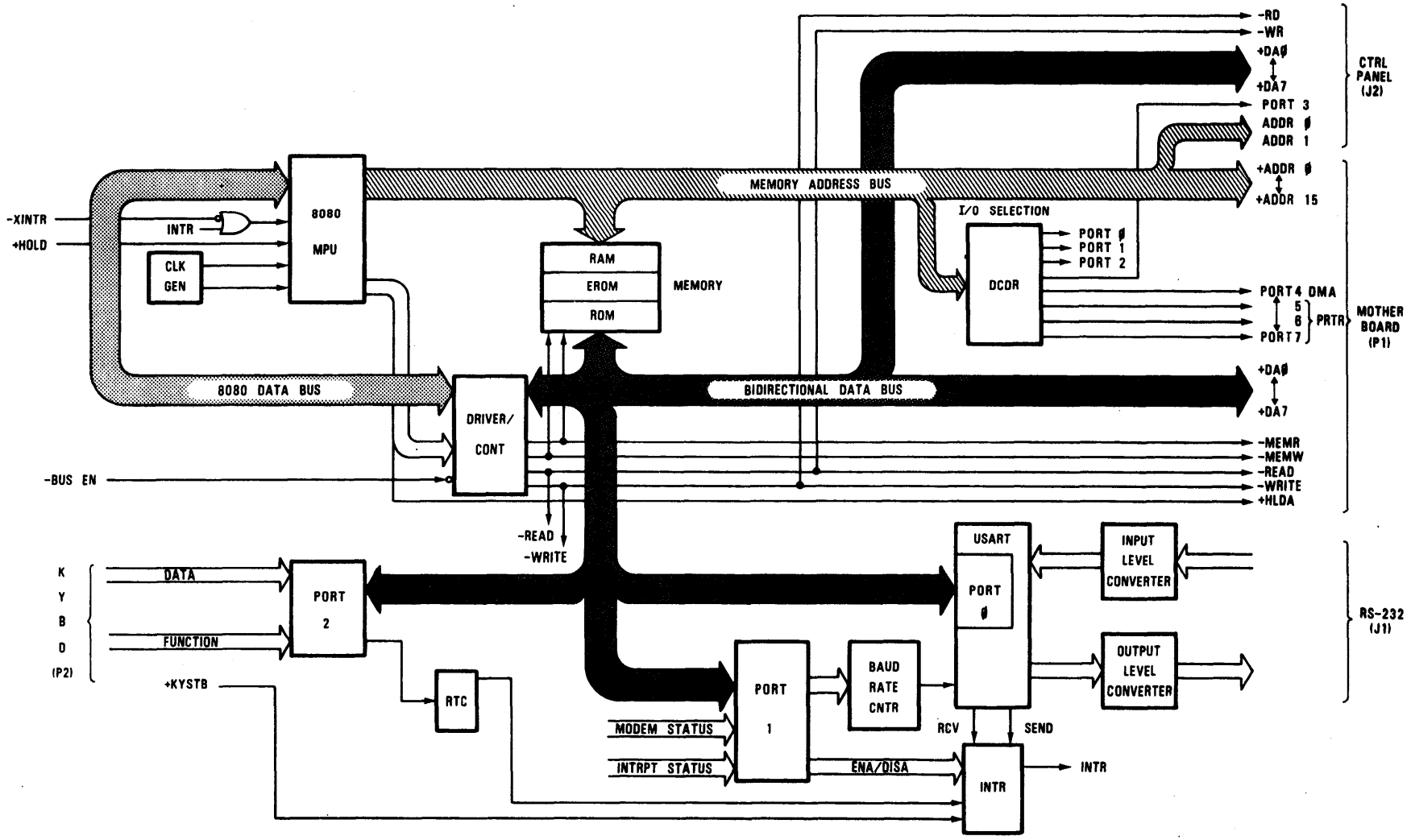


Figure 2-2. Block Diagram, HPRO3 Board

2.2 PROCESSOR (HPRO3) BOARD, PART NO. 23924-XX (Figure 2-2)

The HPRO3 board contains the terminal microprocessor system. This includes the 8080A Microprocessing Unit (MPU), Memory, several Input/Output (I/O) ports, the Universal Synchronous/Asynchronous Receiver/Transmitter (USART) and its associated RS-232 interface components, and all control electronics.

NOTE

Throughout this manual, two terms will be used extensively: terminal microprocessor refers mainly to the entire HPRO3 circuit board, whereas MPU refers to the 8080A integrated circuit.

2.2.1 General Operation

The terminal microprocessor is actually a miniature computer. It receives its instructions from Read Only Memory (ROM), either locally or located on the XMEM board. These instructions are arranged to form a "microprogram." As it executes this microprogram, the MPU receives data from the various input ports and stores it in memory, or reads data out of memory and sends it to the various output ports. Between input and output instructions, the MPU may perform other operations on the data, make logical decisions concerning the data, or "jump" to a different portion of its program.

2.2.1.1 Input/Output

Data can enter or leave the HPRO3 board via any of four channels. First, in the case of the keyboard, data enters the board over the "keyboard data bus" and is held in Port 2 until the MPU is ready for it. Then the MPU "reads" the data from Port 2, and the data is transferred to the MPU over the bidirectional data bus.

Second, data may enter (or leave) over the EIA interface, and be held temporarily in the USART (Port 0). The data is transferred between the MPU and the USART over the bidirectional data bus.

Third, data may enter or leave the board over the 8-bit bidirectional data bus through the J2 connector (normally used for the control panel). In this case, an "I/O port" or its equivalent must be located on another board cable-connected to the HPRO3 board via J2. This port is addressed as Port 3.

Fourth, data may enter or leave the board over the 8-bit bidirectional data bus through the mother board connector (P1). Again, an I/O port of some type must be located on another circuit board plugged into the printer mother board. The port must be addressed as Port 4, 5, or 6.

In this fourth case, the data transfer can be either between the MPU and the external port, or it can be directly between the memory and the external port, bypassing the MPU. If direct memory access is used, the external port or device must provide the necessary signals to delay, or "hold," the MPU while the data transfer is taking place.

Note that the MPU can also address Port 1 for either input or output. This port, however, is contained fully on the HPRO3 board, and does not transfer data onto or off the board. It is used for local control of the baud rate and interrupt enable/disable, and to monitor interrupt status.

When the XMEM board is supplied, it is addressed in the same manner as HPRO3 internal memory via address lines on the mother board. Data is also transferred via the mother board.

2.2.1.2 Interrupts

The normal microprogram instruction sequence can be interrupted when necessary to enable the transfer of data to or from an I/O device, or for other purposes. Generally, when an interrupt occurs, the MPU completes the instruction it is presently performing, and then jumps to its interrupt servicing routine, which begins at memory location 0056_{10}. This routine first determines what type of interrupt is occurring, and then performs the steps necessary to service the interrupt. If two or more interrupts occur simultaneously, the interrupt service routine in the microprogram determines which will be serviced first.

There are five types of interrupts, all of which can be individually enabled or disabled by the microprogram. The first four types can be independently enabled or disabled on the HPRO3 board, whereas the last type (external) must be disabled on the circuit board on which it is initiated (some external circuit board). The five types of interrupts are as follows:

(1) USART receive: the USART has received a character from the data link and is waiting to transfer it to the MPU.

(2) USART send: the USART has shifted a character out to the data link and is ready to accept a new character from the MPU for transmission.

(3) Keyboard: a data character has been received from the keyboard (or parallel data interface) accompanied by a strobe, and is waiting to be read by the MPU.

(4) Real-Time Clock: the Real-Time Clock has timed out, denoting that 10 ms has elapsed since it was activated.

(5) External: an interrupt can be generated by logic on a different circuit board and applied to the HPRO3 board via the -XINTR input.

2.2.1.3 Memory

Either random-access memory (RAM), read-only memory (ROM), or erasable read-only memory (EROM) ICs (or all three) may be used. Maximum capacity of the HPRO3 board is 4K bytes of ROM, 1K of EROM, and 512 bytes of RAM. Additional memory on the XMEM board can be utilized by placing the necessary address on the memory address bus; data is transferred over the bidirectional data bus.

2.2.1.4 Real-Time Clock

A 10-ms one-shot is used as a real-time clock, to allow the MPU to pole various I/O ports (eg, the control panel) at regular intervals.

2.2.1.5 Special Voltage Supplies

The HPRO3 board also contains local voltage regulators to convert the ±15V from the main power supply to ±12V and -5V needed by the EIA interface, some of the memory ICs, the MPU, and some external circuits and devices.

2.2.2 8080A Microprocessing Unit (MPU)

The 8080A is an 8-bit microprocessor contained in a single 40-pin integrated circuit (IC) package. It has an 8-bit wide bidirectional data bus used for both input and output. It has a 16-bit address bus, capable of addressing up to 65,536 memory locations. The MPU's instructions are located in memory, from where they are fetched and executed sequentially. There are over 100 separate instructions possible, although many are similar, the difference being only in the various MPU internal registers specified.

2.2.2.1 Architecture

To understand the operation of the terminal microprocessor, it is only necessary to know that the MPU contains an instruction register, a program counter, a memory address register, a stack pointer, and other registers and logic elements. The instruction register contains the 8-bit instruction op code. The program counter contains the 16-bit memory address of the next instruction to be fetched. The memory address register is made up of two 8-bit registers, referred to as the H and L register pair. It is used to address memory for memory read and memory write instructions. Other internal MPU registers can also be used to address memory. The stack pointer is generally used to "remember" the address of the next sequential main program instruction while an interrupt subroutine is being executed. Still other elements internal to the MPU perform the arithmetic and logic operations and control the input and output over the data bus.

This is admittedly a very brief description of the MPU architecture, but this background should be sufficient to allow understanding of the material to follow. Further information on the MPU can be found in the integrated circuit information presented in the Schematics/ Reference section of this manual.

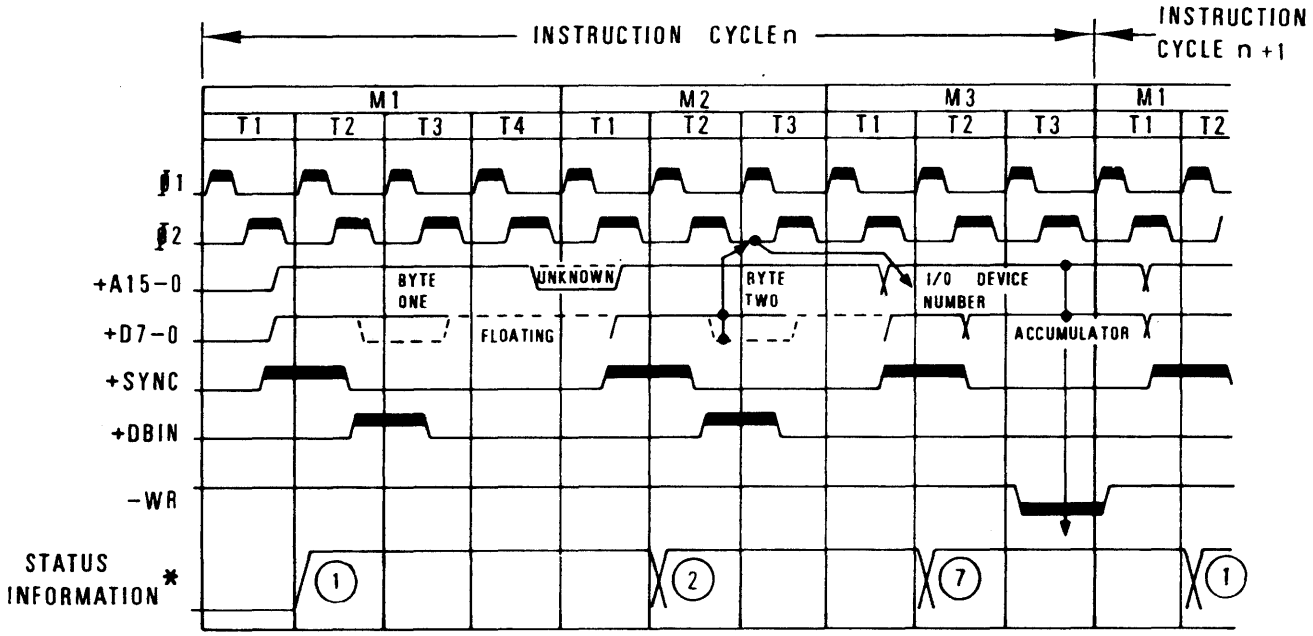
2.2.2.2 Timing

Timing is controlled by two 12V (nominal) non-overlapping clocks, Φ1 and Φ2. These clocks are provided at a frequency of 2 MHz by a Clock Generator IC.

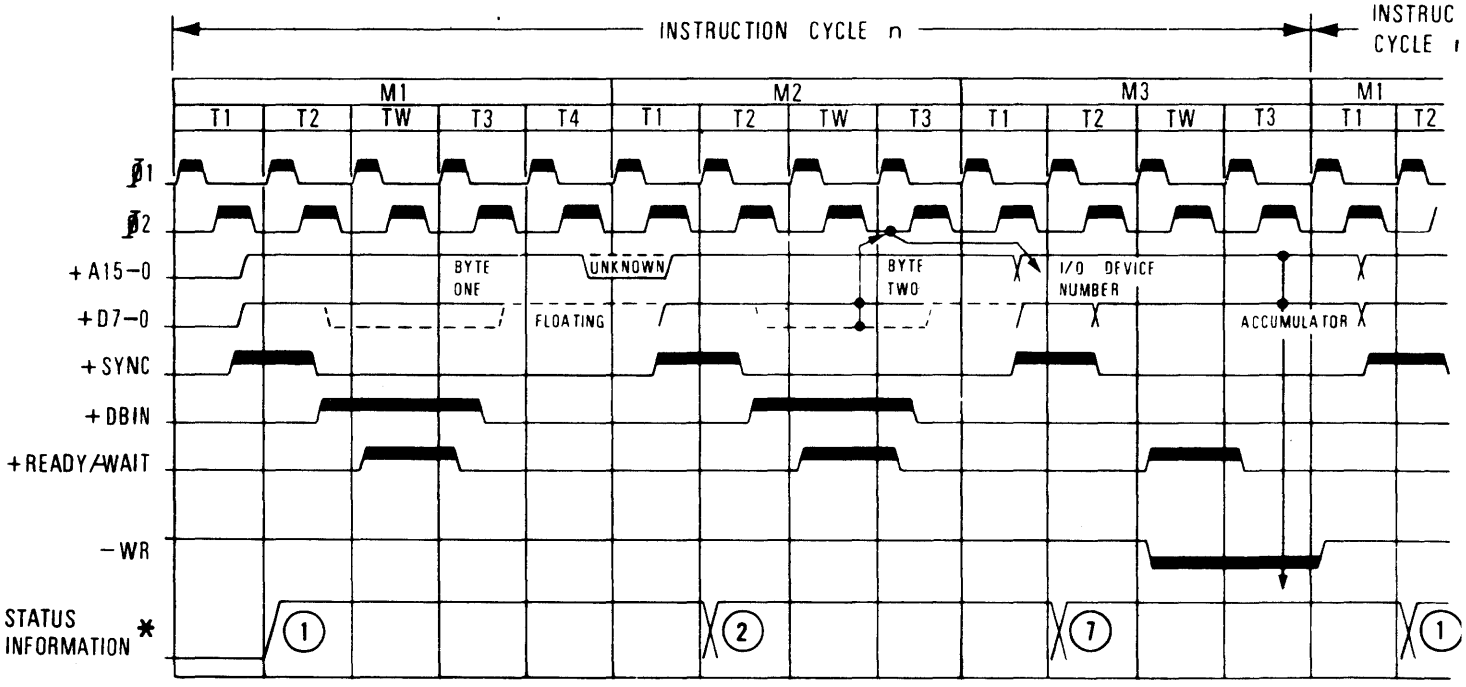
2.2.2.3 Basic Processor Operation

MPU operation is divided into time periods called "cycles" and "states." There are two types of cycles: instruction cycles and machine cycles. The material that follows is summarized in the timing chart in Figure 2-3.

A. Without WAIT State



B. With WAIT State



*Numbers in circles refer to types of machine cycles.

Figure 2-3. Typical Instruction Cycle (Output Instruction)

2.2.2.3.1 Instruction Cycle. An instruction cycle includes both the fetching of the instruction from memory and the execution of the instruction. Each instruction may contain one, two, or three 8-bit bytes. Multiple byte instructions must be stored in successive memory locations. Figure 2-4 illustrates the three instruction formats. The actual bit configuration of the op code is not important to the understanding of the terminal processor operation.

One Byte Instructions

D7	D6	D5	D4	D3	D2	D1	D0	OP CODE

Two Byte Instructions

D7	D6	D5	D4	D3	D2	D1	D0	OP CODE
D7	D6	D5	D4	D3	D2	D1	D0	DATA or ADDRESS

Three Byte Instructions

D7	D6	D5	D4	D3	D2	D1	D0	OP CODE
D7	D6	D5	D4	D3	D2	D1	D0	DATA or
D7	D6	D5	D4	D3	D2	D1	D0	ADDRESS

Figure 2-4. MPU Instruction Format

2.2.2.3.2 Machine Cycle. A machine cycle is required each time an I/O array or the memory is accessed. Each instruction cycle can contain from one to five machine cycles. There are ten different types of machine cycles possible, as follows:

(1) Instruction Fetch
(2) Memory Read
(3) Memory Write
(4) Stack Read
(5) Stack Write
(6) Input
(7) Output
(8) Interrupt Acknowledge
(9) Halt Acknowledge
(10) Interrupt Acknowledge While in Halt

2.2.2.3.3 States. A state is defined as the time interval (500 ns) from leading edge to leading edge of the Φ1 clock. There are 6 possible states, numbered T1 through T5 and TW (representing "wait"). All machine cycles include T1, T2, and T3. When the jumper wire is installed between pins 24 (WAIT) and 23 (RDY) of the 8080A, TW follows T2. This is to slow down the MPU so that slower memory ICs may be used. T4 and T5 are omitted during execution of instructions not requiring them.

2.2.2.3.3.1 T1. During state T1 either a memory address or an I/O port number is placed onto the memory address bus. Also, the MPU places eight bits of status information on the data bus which identify the type of machine cycle being performed. Following the rising edge of Φ2 the SYNC signal is produced by the MPU, which identifies the beginning of a machine cycle. See Figure 2-3.

2.2.2.3.3.2 T2. During state 2 the MPU monitors its RDY input. If it is high, the MPU goes on to state 3; if it is low, the MPU goes on to the Wait state.

During machine cycles that bring data into the MPU (Instruction Fetch, Memory Read, Stack Read, Input, and Interrupt Acknowledge), the Data Bus In signal, DBIN, is developed at Φ2 during T2. DBIN remains high through TW and into T3. This signal develops -READ and -MEMR at the proper time to provide the input data needed by the MPU. (This is covered more fully in 2.2.4.)

2.2.2.3.3.3 TW. The wait state provides the MPU delay required for proper memory access. No internal processing occurs during this state. The MPU monitors its RDY input, and if it is low, it remains in the Wait state; if it is high, the MPU goes on to state 3. If the RDY input is connected to the WAIT output, the MPU goes on to T3 after one state time (500 ns) in TW.

During machine cycles in which the MPU outputs data (Memory Write, Stack Write, Output), it develops the WR (Write) signal during TW or T3 and holds it low until after the end of T3. This signal is used by other logic on the HPRO3 board or another board to strobe the output data to memory or to the selected output port.

2.2.2.3.3.4 T3. During state T3 the data or instruction byte is actually transferred between the MPU and memory or an I/O port. The source and destination of the byte is determined by the type of machine cycle being performed. For example, during an instruction fetch cycle, the source of the data (instruction byte) is the memory location addressed during state 1; the destination is the MPU. During an Output machine cycle, the source is the MPU and the destination is the I/O port selected (addressed) in state 1.

2.2.2.3.3.5 T4 and T5. These two states are used only when required for manipulation of data within the MPU.

2.2.2.3.4 Hold. When the +HOLD signal goes high, it causes the MPU to stop operation at the end of the instruction currently being executed. This is used during direct memory access; when DMA is not used, the +HOLD line is held low by a jumper wire to GND.

2.2.3 Clock Generator (8224)

The clock generator is contained in a single integrated circuit that provides several functions. First, it provides the two non-overlapping 12V signals, Φ1 and Φ2, required by the MPU. The frequency of these signals (2 MHz) is controlled by an external quartz crystal. A TTL equivalent of the Φ2 signal, +TΦ2, is also developed for use in timing other functions.

Second, the 8224 converts the MPU's SYNC signal into the Status Strobe signal, STSTB. This signal is used to load the status information, put out by the MPU at the beginning of each machine cycle, into the Bus Driver/System Controller IC. This is covered more fully in 2.2.4.

Third, at power-on, the clock generator IC develops +CLR, which is used to reset and initialize the entire HPRO3 board.

The 8224 has other capabilities not utilized by the terminal microprocessor.

2.2.4 Bus Driver/System Controller (8228)

This module is another single IC that performs three basic functions: bidirectional bus control, system logic control, and initial interrupt request processing.

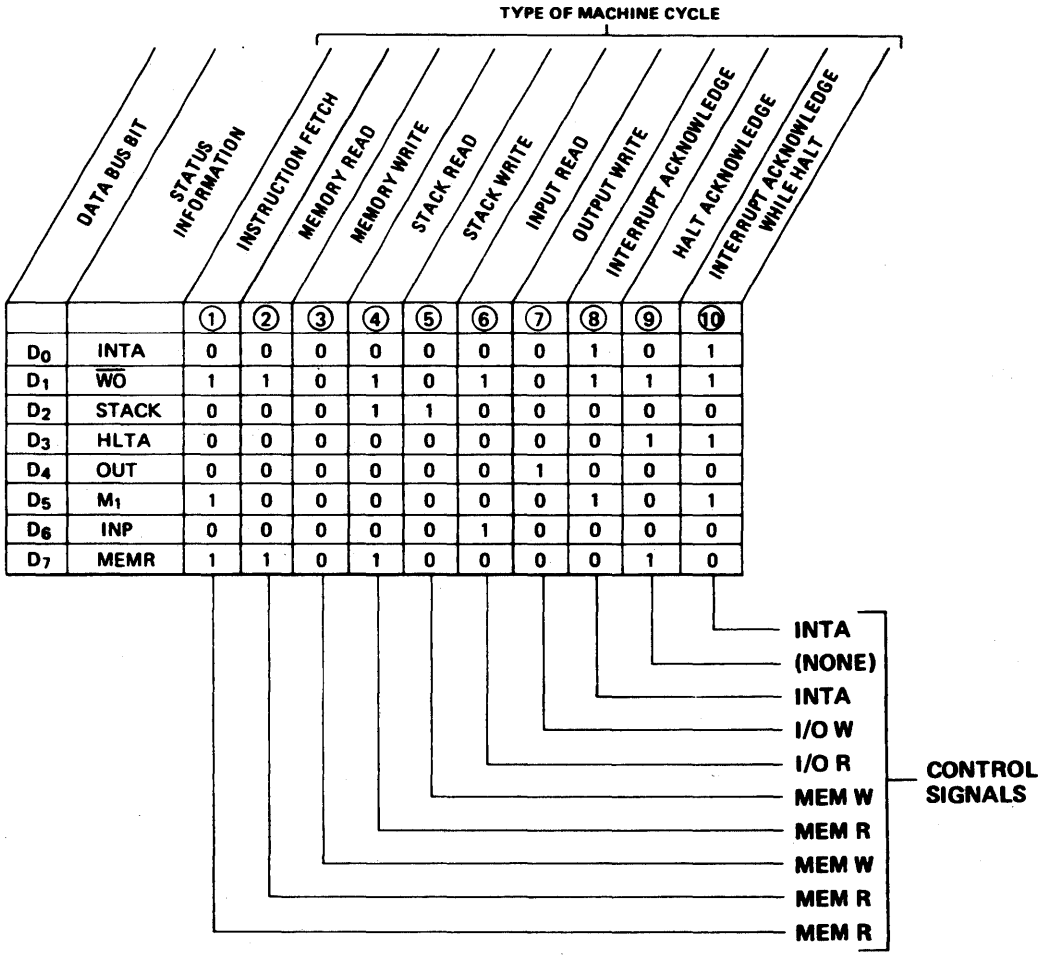


Figure 2-5. MPU Status and Resultant Control Signals

2.2.4.1 Bus Control

The 8228 provides a buffer between the MPU and the memory and I/O ports. Controlling the two 8-bit data buses on the HPRO3 board involves not only switching the data on and off in the proper direction at the right time, but also in providing the required voltage and current levels. Since the MPU is an MOS device, it requires a voltage of at least +3.3 volts for a "logic 1" or "true" indication on its data inputs. The 8228 provides a minimum of +3.6 volts on the 8080 Data Bus, which is substantially higher than can be guaranteed by standard TTL devices. For output data, the MPU can provide only 1.9 mA of current drive. With many I/O ports and the memory connected to the bidirectional data bus, this value could easily be exceeded, so the 8228 is used to provide over 10 mA to satisfy this requirement. The buses can be "turned off" (forced into the high-impedance state) when direct memory access is used. See 2.2.4.4. The direction of data flow on the buses is controlled internally by the same signals that furnish the system control function performed by this IC.

2.2.4.2 System Logic Control

At the beginning of each machine cycle, the MPU issues "status" information on the 8080 data bus that indicates the type of cycle about to be performed. At the same time, the clock generator module develops STSTB, which loads this status information into a status latch inside the 8228. This status latch output is decoded, along with DBIN, WR, and HLDA (Hold Acknowledge) from the MPU, into the system control signals MEMR (Memory Read), MEMW (Memory Write), READ (I/O READ), and WRITE (I/O WRITE). (These decoded signals also provide the internal control of the bus driver.) Note that these signals are not levels, but that they are gated by DBIN or WR from the MPU at the proper time. The status information provided by the MPU, and the system control signals developed for each of the ten types of machine cycles are shown in Figure 2-5.

2.2.4.3 Interrupt Handling

The 8228 is capable of handling interrupts in either of two different ways. Only one of these methods is used in this terminal, in which the Interrupt Acknowledge pin (23) is connected to +12V through a resistor. Connected this way, when the MPU is interrupted (by an input from the keyboard or USART, for example), it performs an INTERRUPT ACKNOWLEDGE machine cycle, and the 8228 automatically forces an RST 7 (Restart 7) instruction into the MPU. This instruction causes the MPU to fetch its next instruction from memory location 56_{10}, which begins the routine needed to service the interrupt.

2.2.4.4 Direct Memory Access

The BUS ENable input (pin 22) must be low for normal operation. When direct memory access is used, the DMA circuitry on another board drives this signal high, forcing all 8228 outputs into their high-impedance state. This allows the bidirectional data bus and the MEMR and MEMW signals to be controlled by the DMA logic. If the DMA feature is not used, -BUS EN is held low by a jumper wire to GND.

2.2.5 Memory

Maximum memory capacity of the HPRO3 board is 4K ROM, 512 bytes of RAM, and 1K of EROM. ROM memory consists or one or two 2K x 8-bit mask-programmed ROM ICs containing the terminal microprogram. RAM memory consists of two 256 x 4-bit ICs for each 256 bytes. The EROM portion can be either a 512 x 8-bit or 1K x 8-bit EROM IC. The EROM would normally contain keyboard position encoding data or similar data for terminals built in small quantities—too small to justify masked-ROM changes. When the XMEM board is supplied, the terminal microprogram can be stored there. See paragraph 2.3.

2.2.5.1 Addressing

The memory map in Figure 2-6 shows the relationship of the various memory elements to their addresses.

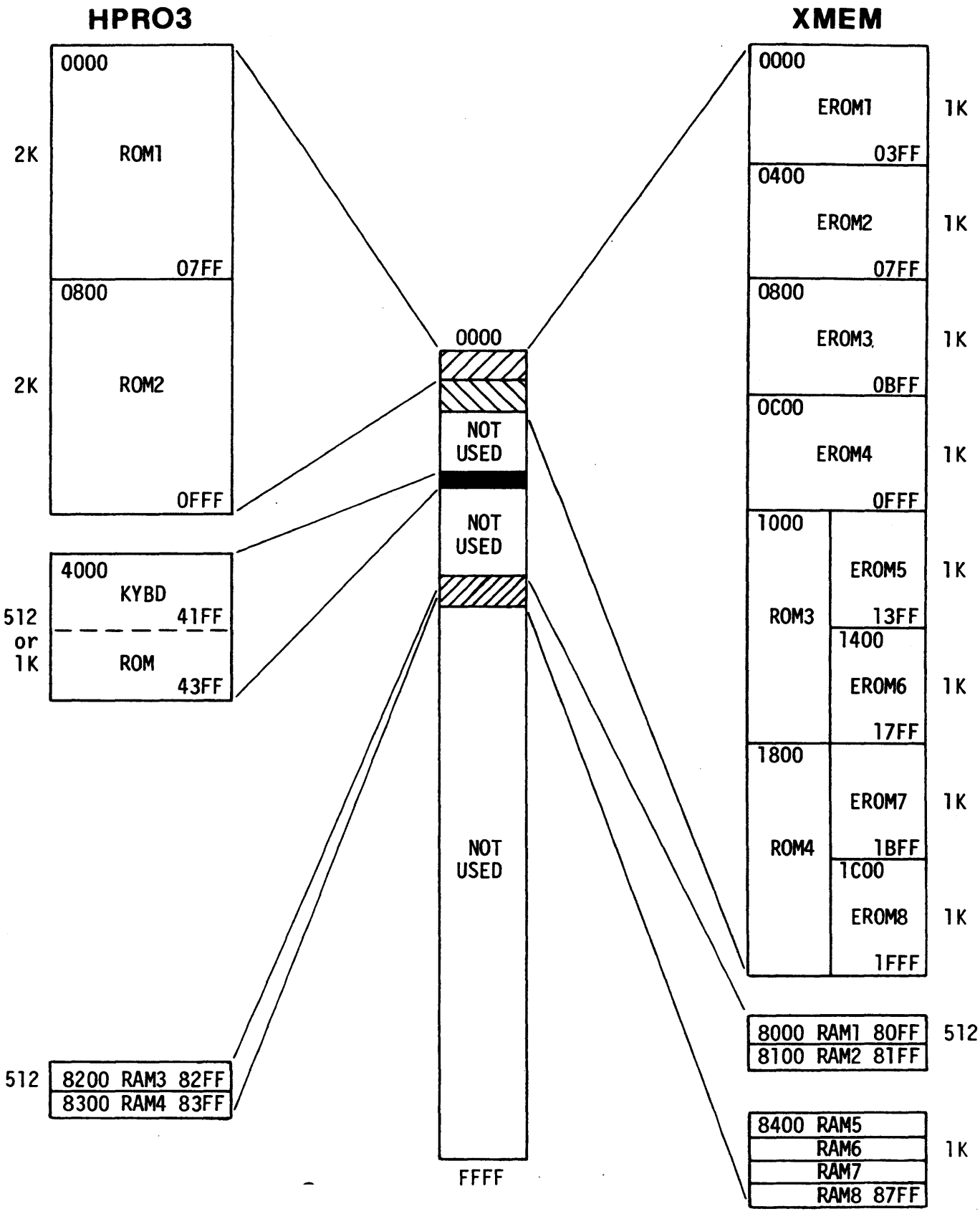
The memory ICs on the HPRO3 board are addressed by the lower-order bits of the memory address bus. The higher-order bits A9, A10, A11, A14, and A15 are used to select, through a decoder, whether RAM, ROM, or EROM will be addressed. In the case of RAM, the state of the A8 line determines which pair of ICs will be addressed. For ROM, the A11 line selects which of the two possible ICs will be used. (Note that A11 goes to both ROM ICs; the internal programming of the ICs is such that one of the ICs will be activated when A11 is low and the other when A11 is high.)

Since the memory address bus is available on the HPRO3 board outputs, external memory can assume any memory address, so the terminal designer must assure that only one memory location exists for each address. For example, during program development, the microprogram can be contained in external memory beginning at location 0000. In this case, the HPRO3 board cannot have ROMs installed. After the microprogram is perfected, it can be "burned" into masked ROMs, which can be installed on the HPRO3 board, and the external memory board can be eliminated.

The memory address bus being available on the HPRO3 board's plug also enables the entire memory to be addressed from and external source, as is the case when the DMA function is utilized.

2.2.5.2 Reading

All memory ICs are three-state devices. This means that the outputs remain in the high-impedance, or "off" state, at all times when the IC is not selected. (This allows the memory address bus to be used for addressing I/O devices; the address lines can assume any configuration, but there will be no input to or output from memory without the proper system control signals.) The MEMR signal is connected to the "output disable" input of the RAMs (pin 9). This maintains the RAM outputs in their high-impedance state at all times other than during a memory read. MEMR is also one of the inputs to the memory type decoder. This allows ROM and EROM to be selected only during a read operation.



NOTES: 1. First 4K can be either ROMs on HPRO3 or EROMs on XMEM.
2. Second 4K can be either ROMs or EROMs on XMEM.

Figure 2-6. Memory Map

2.2.5.3 Writing

When memory write is performed, the RAM output remains disabled (MEMR is high), and MEMW being low allows information on the bidirectional data bus to be written into the addressed RAM location. Note that each pair of RAMs operates in parallel, one IC servicing the low-order four bits of the bidirectional bus, and the other taking care of the high-order four bits.

2.2.5.4 Timing

Typical idealized timing waveforms are shown in Figure 2-7. Specific timing requirements for each of the memory IC types can be found in the IC information in the schematic/reference section. In all cases, the timing shown in Figure 2-7 is within the timing constraints of the individual ICs.

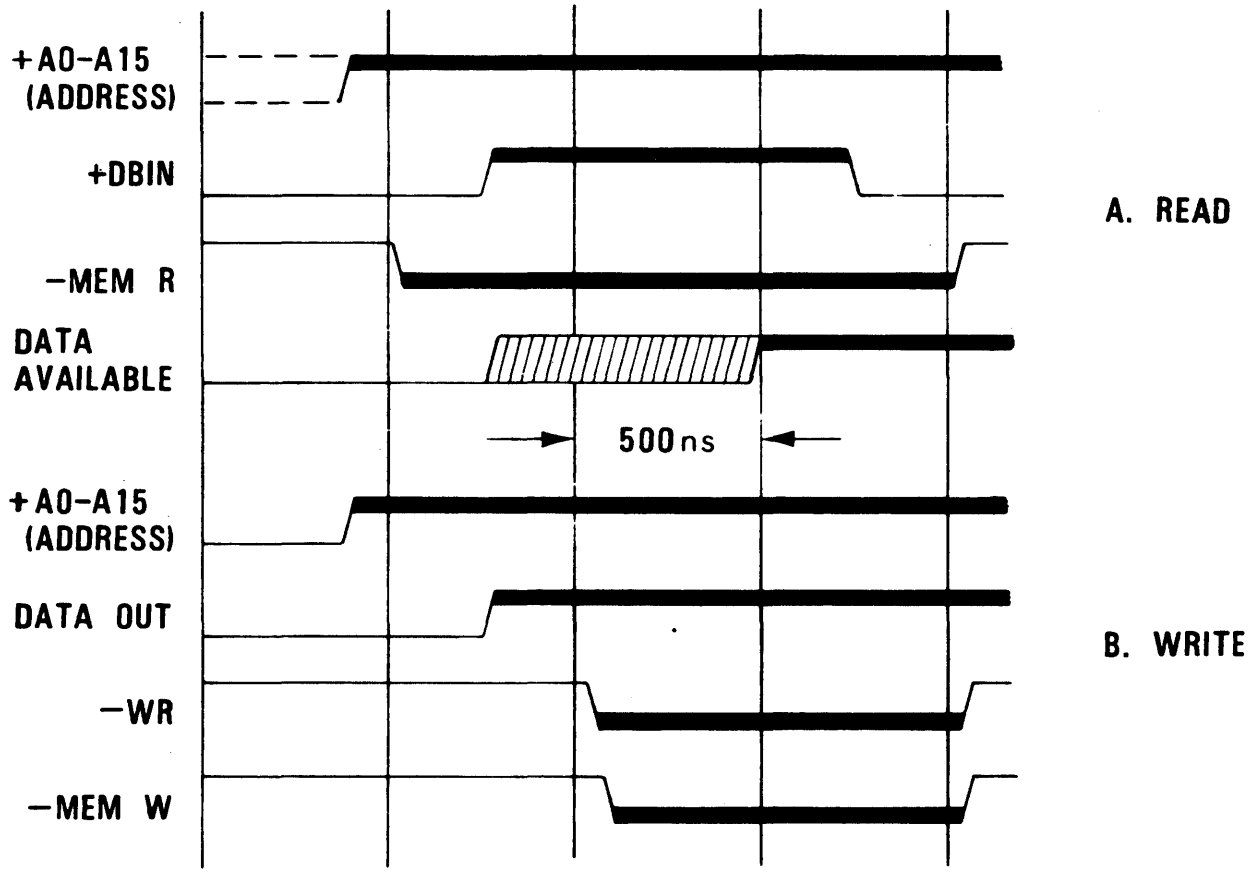


Figure 2-7. Memory Timing

2.2.5.5 Direct Memory Access

When the DMA function is utilized, it conforms to the following general sequence:

(1) DMA circuitry on another board raises the +HOLD line to the MPU.

(2) The MPU finishes the instruction it is presently performing, and then raises its HLDA (Hold Acknowledge) line. It then suspends operations, and holds all data and address lines in their high-impedance state.

(3) The DMA circuitry receives the hold acknowledgement and drives -BUSEN low. This forces the 8228 to place all of its outputs, both data and control signals, into their high-impedance state.

(4) The external DMA circuitry then places the desired address on the memory address bus, and drives either -MEMR or -MEMW low. The data is then transferred over the bidirectional data bus.

(5) When the DMA circuitry is finished, it raises -BUSEN and lowers +HOLD, and the MPU resumes processing at its next sequential instruction.

2.2.6 Input/Output

The terminal microprocessor can address up to eight I/O ports. These ports, or "devices," such as keyboard, control panel, etc., are addressed over the Memory Address Bus, and data is transferred to and from the MPU over the bidirectional data bus. An I/O channel or device is first addressed by the MPU, which then develops the -READ or -WRITE signal to transfer the data. On output, for example, the MPU first addresses a particular output device, then places the output data on the bidirectional data bus, and finally develops -WRITE. Although the data is available to all "devices" on the bus, only the one that had been addressed can accept the data. Input is similar: only the addressed device places data onto the bus. All other devices are "observers."

The five low-order bits of the memory address bus are used for I/O device selection. Bits 2, 3, and 4 are applied to a decoder, the outputs of which (-PORT Ø through -PORT 6) are used to select one of the seven possible ports. Each port can comprise up to four 8-bit bytes, and bits 0 and 1 are used to select one of the four bytes.

Three of the seven possible I/O ports are located on the HPRO3 board. The rest of the ports may or may not be used in a particular terminal or printer. The possible ports and their typical functions are as shown in Table 2-1.

2.2.6.1 USART (Port 0)

The type 8251 USART (Universal Synchronous/Asynchronous Receiver/Transmitter) IC accepts an 8-bit byte of data from the MPU in parallel format and converts it to a serial stream of data for transmission over the communications link. Similarly, it receives data characters from the link in serial format and converts them into parallel data bytes for the MPU. During transmission, the USART adds start, stop, and parity bits. During reception, it strips these bits and also checks parity, if desired. It also checks for data framing errors and overrun errors, and can monitor modem status. It has other capabilities that are not generally used (synchronous transmit/receive, character lengths down to 5 bits, etc.).

Table 2-1. I/O Ports

Port No.	Function
0	USART
1	Baud Rate, Interrupt Enable/Disable & Status
2	Keyboard
3	Control Panel
4	DMA

2.2.6.1.1 Addressing. The CS (Chip Select) input is driven low whenever the MPU addresses Port 0. No information can be transferred between the USART and the MPU until the USART is selected.

The USART also has a C/D input, which is connected to the +ADDR Ø line of the Memory Address Bus. When this line is high, control information is transferred; when it is low, data is transferred. The USART does not utilize the +ADDR 1 line.

2.2.6.1.2 Timing. Refer to the baud rate counter discussion in 2.2.6.2.1.2.

2.2.6.1.3 Information Transfer. Two inputs, RD and WR, determine the direction of information transfer. When RD is low, the USART places data or status information (determined by the C/D input) on the bidirectional data bus for input to the MPU. When WR is low, data or control information from the MPU is taken off the data bus and loaded into the USART. The RD and WR inputs are controlled by -READ and -WRITE, respectively, from the 8228 bus driver/system controller.

Note that all information transfer between the MPU and the USART is over the bidirectional data bus, through a bidirectional, 3-state buffer within the USART. Information transfer between the USART and the data link is over individual lines for Send Data, Receive Data, and each of the modem status and control lines, through a voltage level converter, to (or from) the modem. (Refer to the integrated circuit data in the Schematics/Reference section for information on the level converter ICs.)

2.2.6.1.3.1 Read Data. When the USART receives a character from the data link, it raises its RXRDY (Receiver Ready) line, which goes to the interrupt logic. If USART interrupts are enabled, +INTR is developed and sent to the MPU. In servicing this interrupt, the MPU performs a sequence of instructions, one or which is an input from Port 0. With CS low, RD low, and C/D low, the USART puts an 8-bit byte of data onto the bidirectional data bus, from where it is accepted by the MPU. The USART, having presented the data byte to the bus, resets its RXRDY line, until the next character is received and the entire sequence repeats.

As the data is received from the data link, the USART strips off the start and stop bits, checks the parity bit (if parity checking is enabled—see 2.2.6.1.3.4), and checks for framing errors (lack of a stop bit at the proper time). If an error is detected, a bit is set in the internal Status Register. The USART also checks to see that the previous character has been accepted by the MPU—if RXRDY is still high (has not been reset by the MPU having read the previous character), the overrun status bit is set.

2.2.6.1.3.2 Write Data. When the MPU wishes to send data to the USART, it addresses Port 0, places the data character on the bidirectional data bus, and develops -WRITE. This combination (CS, WR, and C/D all low) loads the character into the USART, which then adds the start, stop, and parity bits, and immediately begins to shift the character out, one bit at a time through the level converter IC to the data link.

There are two status bits pertaining to data transmission: TXE (Transmitter Empty) and TXRDY (Transmitter Ready). Both of these become reset when a character is loaded into the USART from the MPU. If a relatively long time has passed since the previous character was loaded, TXRDY sets again almost immediately. This allows a second character to be loaded, even though the first has not been fully shifted out. TXRDY again resets as the second character is loaded, but this time it remains reset until the first character is completely shifted out. Then it sets again, allowing another character to be loaded. When all data characters have been fully transmitted, TXE again sets.

2.2.6.1.3.3 Read Status. When the MPU wishes to know the status of the USART, it performs an input from Port 0 with +ADDR Ø high. This occurs after any interrupt, since the MPU needs to know if it is the USART that is interrupting, and before every data output to the USART, because the MPU must check to see that the USART is able to accept the data character.

When Port 0 is addressed, the -PORT Ø signal enables the USART by driving its CS input low, and +ADDR Ø drives the USART's C/D input high, which directs the USART to transfer control/status information. -READ again directs the USART to output information onto the bidirectional data bus, but because the C/D input is high, the USART outputs status information instead of data.

2.2.6.1.3.4 Write Control. A control write is used to program the USART for parity checking, byte length, number of stop bits, etc. When the MPU outputs control information for the USART, it addresses Port 0 while holding +ADDR Ø high. However, complete control of the USART requires more than 8 bits of information. The USART is designed to accept two different control bytes, a "Command" byte and a "Mode" byte. It accepts the Mode byte only as the first control instruction following a reset. All subsequent "control writes" are accepted as Command bytes. Each of the individual bits in the Command and Mode bytes is defined in the IC data for the 8251 in the Schematics/Reference section of this manual.

2.2.6.2 I/O Port IC (8255)

The other two I/O ports on the HPRO3 board, Ports 1 and 2, utilize an 8255 Programmable Interface IC. This type of IC may also be used for ports located on the other circuit boards. This is a 40-pin IC having eight pins connected to the bidirectional data bus and three more sets of eight pins each that can interface to various "peripheral" devices. The balance of the pins are used for power supply connections and control signals.

The 8255 contains three 8-bit registers called A, B, and C, each of which can be used for either input or output. The C register can even be split into two 4-bit registers, each individually programmable for input or output, or for control and status signals.

There are three possible modes of operation, selected by a control word issued by the MPU. This control word is a part of the firmware microprogram stored in ROM, so it can be different for each 8255, and it can even change at different points in the execution of the program. (This control word can also be used to alter individual bits in Register C, while leaving the other seven bits unchanged.) The three possible modes are as follows:

Mode 0: Simple input or output for each register
Two 8-bit and two 4-bit registers
Outputs are latched
Inputs are not latched

Mode 1: Strobed input or output for Registers A and B
Register C used as control/status for the other two registers
Inputs and outputs all latched

Mode 2: Strobed bidirectional bus (not used in HPRO3)

Each 8255 IC has the following connections to the terminal microprocessor:

DØ-D7: The bidirectional data bus, over which all data transfer occurs between the MPU and the 8255.

CS: Chip Select Input. One of the decoded "port" signals is used to select only one 8255 at a time. Only -PORT 1 and -PORT 2 select 8255s on the HPRO3 board. The other port signals may select 8255s on other circuit boards.

A0&A1: ADDRESS Ø and ADDRESS 1 Inputs. The two low-order lines of the Memory Address Bus (ADDR Ø and ADDR 1) are used to select which of the three registers is to be used, or to specify that a control word is being sent out by the MPU.

ADDR 1 (A1)	ADDR Ø (AØ)	
0	0	Register A
0	1	Register B
1	0	Register C
1	1	Control Word

RD: Read Input. When low, specifies a read (into the MPU) is occurring. This is considered "input."

WR: Write Input. When low, specifies a write (from the MPU) is occurring. This is considered "output."

Further details of the 8255 IC's operation can be found in the Schematics/Reference section.

2.2.6.2.1 Port 1. Port 1 is enabled by the -PORT 1 signal. It is generally operated in Mode 0. The control word from the MPU programs the port for input through Register A and output through Registers B and C.

2.2.6.2.1.1 Status Inputs. The six bits of Register A that are used provide status to the MPU of the following:

Bit 2	EIA option 3
Bit 3	EIA option 2
Bit 4	Carrier Detect
Bit 5	Clear to Stand
Bit 6	Keyboard Interrupt
Bit 7	Real-Time Clock Interrupt

2.2.6.2.1.2 Baud Rate Counter. This counter produces a square wave at 1, 16, or 64 times the baud rate frequency. The USART clock frequency requirements vary according to the USART programming (the "mode" instruction) and the desired baud rate. The mode instruction determines whether this clock must be 1, 16, or 64 times the baud rate. (64 is generally used for baud rates below 1200.) A factor is loaded into Register B of the 8255 by the MPU, and the counter, driven by TΦ2, is counted up until it overflows. When this happens, the same factor is reloaded and the counting resumes. The overflow also toggles a D-type flip-flop, which further divides the count by 2 and makes the output symmetrical.

The USART clock can also be supplied by an external source via board pin 4, when the correct jumper wire is installed. Furthermore, during synchronous data transmission/reception, the USART's receive clock is provided by the modem. In this case, a jumper on the HPRO3 board must be changed to separate the transmit and receive clocks.

2.2.6.2.1.3 Interrupt Enable/Disable. Each of the four types of interrupts that can be generated on the HPRO3 board can be individually enabled or disabled. A "1" loaded into the C Register enables, while a "0" disables, as follows:

Bit 4	USART receive
Bit 5	USART send
Bit 6	Keyboard
Bit 7	Real-Time Clock

2.2.6.2.2 Port 2. Port 2 is selected by the -PORT 2 signal, and is generally operated in Mode 1. The control word from the MPU programs the port for input through Registers A and B. The Register C bits are used mostly for control/status in Mode 1, but two bits, PC6 and PC7, are still available for I/O, and in this port they are used for output.

2.2.6.2.2.1 Keyboard (Parallel) Input. This data, in the form of 8-bit parallel bytes on the -DATAØ through -DATA7 lines, is continually applied to the Register A inputs. As long as the Register A strobe input, which is PC4 (pin 13) in the Mode 1 configuration, is low, this data is loaded into Register A. -KYSTB is normally high, so after it drops low and then goes high again, the KEYBOARD INTERRUPT flip-flop sets on the trailing (positive going) edge. As soon as this flop-flop sets, it latches the data into Register A; at this point the eight parallel inputs may be removed or changed without altering the data in the register.

When the KEYBOARD INTERRUPT flip-flop sets, it also presents an interrupt to the MPU (provided keyboard interrupts have been previously enabled). When the MPU recognizes the interrupt, part of its interrupt service routine is an instruction to read from Register A, to input the data to the MPU. Following this, it also performs a pair of "bit set/reset" instructions: the first to put a "low" on PC6 to clear the KEYBOARD INTERRUPT flip-flop; the second to put a "high" back on PC6 to enable the flip-flop to be set again by the next -KYSTB. The MPU also reads the function key status from Register B as part of this interrupt service routine.

Note that +BUSY is driven high when the KEYBOARD INTERRUPT flip-flop sets, and remains high until after the flip-flop is cleared and reenabled. This signal can be used by an 8-bit parallel input device as a ready/not ready indicator; when +BUSY is high, it indicates that -KYSTB signals will not be accepted. The 8-bit parallel input device should present -KYSTB only when +BUSY is low.

2.2.6.2.2.2 Function Key Status. The keyboard function key signals, as well as the status of the three options, are continually applied to Register B. In Mode 1, the Register B strobe is received on PC2 (pin 16). The +SYNC signal from the MPU thus latches the status of the function keys and jumper options into Register B.

These signals do not produce an interrupt. Instead, their status is read from Register B by the MPU each time it services an interrupt caused by -KYSTB.

2.2.6.2.2.3 Real-Time Clock One-Shot. The Real-Time Clock one-shot is controlled by the individual bit set/reset feature of the 8255. Bit 7 in the C Register (PC7, pin 10) is controlled by the MPU: when it goes high, the one-shot fires; when it goes low, the one-shot is enabled to fire again. PC7, when high, must first go low, then return to high to start the 10 ms timer.

2.2.6.3 Off-Board I/O

Input from or output to logic circuits external to the HPRO3 board can be accomplished in either of two ways: programmed I/O or direct memory access. Programmed I/O can occur either through the mother board connector (P1) or the control panel connector (J2). DMA transfer can occur only through the mother board.

2.2.6.3.1 Programmed I/O. This is accomplished in the same manner used for onboard I/O. An I/O port, #3 through #6, is addressed, and -READ or -WRITE is developed. If necessary, +ADDR Ø and +ADDR 1 may be used to further define the address (as when an 8255 IC is used). All data is transferred between the MPU and the off-board port over the bidirectional data bus.

Port 3 must be accessed through the control panel connector. (-READ and -WRITE are passed through the drivers, and become -RD and -WR.) Ports 4,5, and 6 must be accessed through the mother board. Port 4 is generally reserved for DMA, and Ports 5 and 6 are generally used for the printer.

2.2.6.3.2 Direct Memory Access. Data can be transferred directly between memory and an external device following the procedure outlined in 2.2.5.5. In this case, data is transferred directly between memory and the external device over the bidirectional data bus; the MPU stops in a "Hold" condition while the transfer takes place.

2.2.7 Miscellaneous Circuitry

2.2.7.1 3-Terminal Voltage Regulators

There are three 3-terminal voltage regulator ICs, shown on sheet 1 of the HPRO3 logic drawing, that provide the source of -5V, -12V, and +12V. These voltages are derived from the ±15V provided by the power supply, which also provides +5V.

2.2.7.2 Level Converters

The input and output voltage level converters provide the interface between the TTL inputs and outputs of the USART and the 12V (nominal) requirements of RS-232-C.

2.2.7.3 Options

There are four options on the HPRO3 board that provide variations in operation. These are covered in detail in the Product Description.

2.3 XMEM (EXTRA MEMORY) BOARD, PART NO. 23926-XX.

When the 4K bytes of ROM, 1K of EROM, and 512 bytes of RAM on the HPRO board are adequate for the programming application, the XMEM board is not supplied. When additional memory is required, the XMEM board is installed in slot F, directly behind the HPRO board; no connections other than plugging into the mother board are required. The XMEM1 board can contain up to 1.5K bytes of RAM, 4K of ROM, 8K of EROM, or a combination of memory types.

2.3.1 Applications

During program development, programs are stored on EROMs so they can be debugged, erased, and rewritten. When the program has been tested and validated, it is burned into the masked ROMs, which are installed on the HPRO board.

EROMs on the XMEM board are used to store development programs. Because of the time involved in manufacturing masked ROMs, early production terminals are often shipped with programs on EROMs on the XMEM board instead of on masked ROMs on the HPRO board. Also, when a program is larger than 4K bytes, additional memory chips, either ROMs or EROMs, are installed on the XMEM board to store part of the program. ROMs and EROMs on the XMEM board are addressed in the same manner as ROMs and EROMs located on the HPRO board. For applications requiring more than 512 bytes of working read/write memory, up to 1.5K bytes of RAM can be installed on the XMEM board.

2.3.2 Basic XMEM Board

The basic XMEM board (dwg. no. 23926-XX) contains an address buffer, address decoders, and voltage regulators. IC memory chips of the required type and number are added to suit a specific application.

2.3.3 XMEM Configurations

The XMEM can have the following numbers of memory chips installed:

12 Type 2111A-4, 256 x 4-bit RAMs
2 Type 8316A, 2K x 8bit masked ROMs
8 Type 8708, 1K x 8bit EROMs

While it is possible to have all these memories installed (physically) on the same XMEM board, is is logically impractical, because both ROMs and EROMs use the same addresses, and two EROMs must be eliminated for each ROM installed. There is no address interference between RAMs and ROMs or EROMs, so a full complement of RAMs can be installed regardless of the number of ROMs and/or EROMs installed.

2.3.4 Addressing

Figure 2-6 shows the memory addressing scheme used by the MPU to access the entire memory, both on the HPRO board and on the XMEM board. Note that HPRO ROMs #1 and #2, and XMEM ROMs #3 and #4 use the same address areas as the EROMs on the XMEM board, so the EROMs can not be used when the masked ROMs are installed. This is done intentionally, so that a program can be written electrically into EROMs, tested and corrected as often as necessary, and when approved, the program can be used to generate masked ROMs without need for address modification. When masked ROMs are in production, the EROMs can be eliminated, and, if the program is less than 4K, the two ROMs containing the program can be installed on the HPRO board. If there is no need for the additional RAM storage, the XMEM board can be eliminated. If the program is larger than 4K, two additional ROMs can be installed on the XMEM board, along with as many RAMs as are required.

ROMs and EROMs can be mixed, as long as there is no direct address conflict. For example it would be possible to use EROMs 5, 6, 7, and 8 with HPRO ROMs 1 and 2, but these EROMs could not be used with XMEM ROMs 3 and 4. Since RAMs use an entirely different address area, their use is independent of ROM/EROM configuration.

2.3.5 Additional Applications

- o EROMs can be used in terminals produced in quantities too small to justify the expense of preparing masked ROMs.
- o A mixture of ROMs and EROMs can be used in applications requiring special programs.
- o RAMs can provide additional working memory.

2.4 MATRIX INTERFACE BOARD, PART NO. 25930-XX

The MATRIX INTERFACE (MXI) board contains I/O Ports 5 and 6, which transfer data, control signals, and Status information between the terminal processor and the printer processor. Also contained on the MXI board is the logic for receiving and temporary storage of carriage position feedback signals from the CARRIAGE SERVO board enroute to the printer processor. Carriage directional commands are also produced on the MXI board from the data received from the printer processor. These signals are applied to the servo motor driver FETs on the CARRIAGE SERVO board. A block diagram of the MXI board is shown in Figure 2-8.

2.4.1 I/O Ports 5 and 6

I/O ports 5 and 6 are used to synchronize the tranfer of information between the two processors. When the terminal processor performs an output instruction to Port 5 or 6, the output information is stored on the MXI board where it is available to the printer microprocessor. The printer microprocessor periodically "reads" the MXI board to see if there is any information that it should process. Similarly, as the printer microprocessor goes though its steps of controlling the printer operations, it provides status information to the MXI board. This status information is monitored by the terminal microprocessor prior to each output command.

2.4.1.1 Transferring Information to the Printer Processor.

The prerequisites to actual transfer of data include the +POWER ON and -SELECT PRINTER signals. The +POWER ON signal energizes the 8212 ICs and is inverted to provide a -POWER ON signal. Both +POWER ON and -POWER ON are outputs to the printer processor. The -SELECT PRINTER signal will enable the transfer of information between the two processors.

*WRITE TO PORT 6: When -WRITE and -PORT 6 signals develop, the control information on the data bus is transferred to the printer microprocessor via the Port 6 latches. This data is output directly onto control lines to the printer and includes the following control signals: -DOUBLE LINE FEED, +AUTO LINE FEED, +TEST, -SET TOF ZERO, and +RESTORE (INT Ø).

*WRITE TO PORT 5: A Write to Port 5 instruction will only be performed by the terminal processor if the +READY output line from the MXI board is high. This +READY signal is developed on the MXI board when the printer processor provides a -DATA ACK to the MXI board. The -DATA ACK indicates that the printer has received and processed the previous information and it is now able to receive more data. -DATA ACK enters the MXI board and resets the Data Strobe FF (C49) which in turn raises the +READY signal. The -WRITE and -PORT 5 signals load the data on the terminal data bus (DAØ -DA7) into the Port 5 latch on the MXI board and raise the +DATA STROBE signal to inform the printer processor that data is available. This data is then clocked into the printer processor via the printer data bus (D1 - D8). The Data Strobe FF is reset when the -DATA ACK line becomes active (low) from the printer processor.

2.4.1.2 Transferring Information from the Printer Processor

Only status information is received by the terminal processor from the printer when a Read from Port 5 instruction is output to the MXI board from the terminal processor. A +SYSTEM CLOCK signal allows status information from the printer processor to be loaded into the Port 5 latch (D54) at a time that will not cause an error in the system. The -SELECT PRINTER signal must also be present to enable the transfer of data between the two processors. When -READ and -PORT 5 signals are issued from the terminal processor, the data latched at D54 is transferred to the terminal processor via the bi-directional data bus (DAØ - DA7). This status information is "read" by the terminal processor prior to each command.

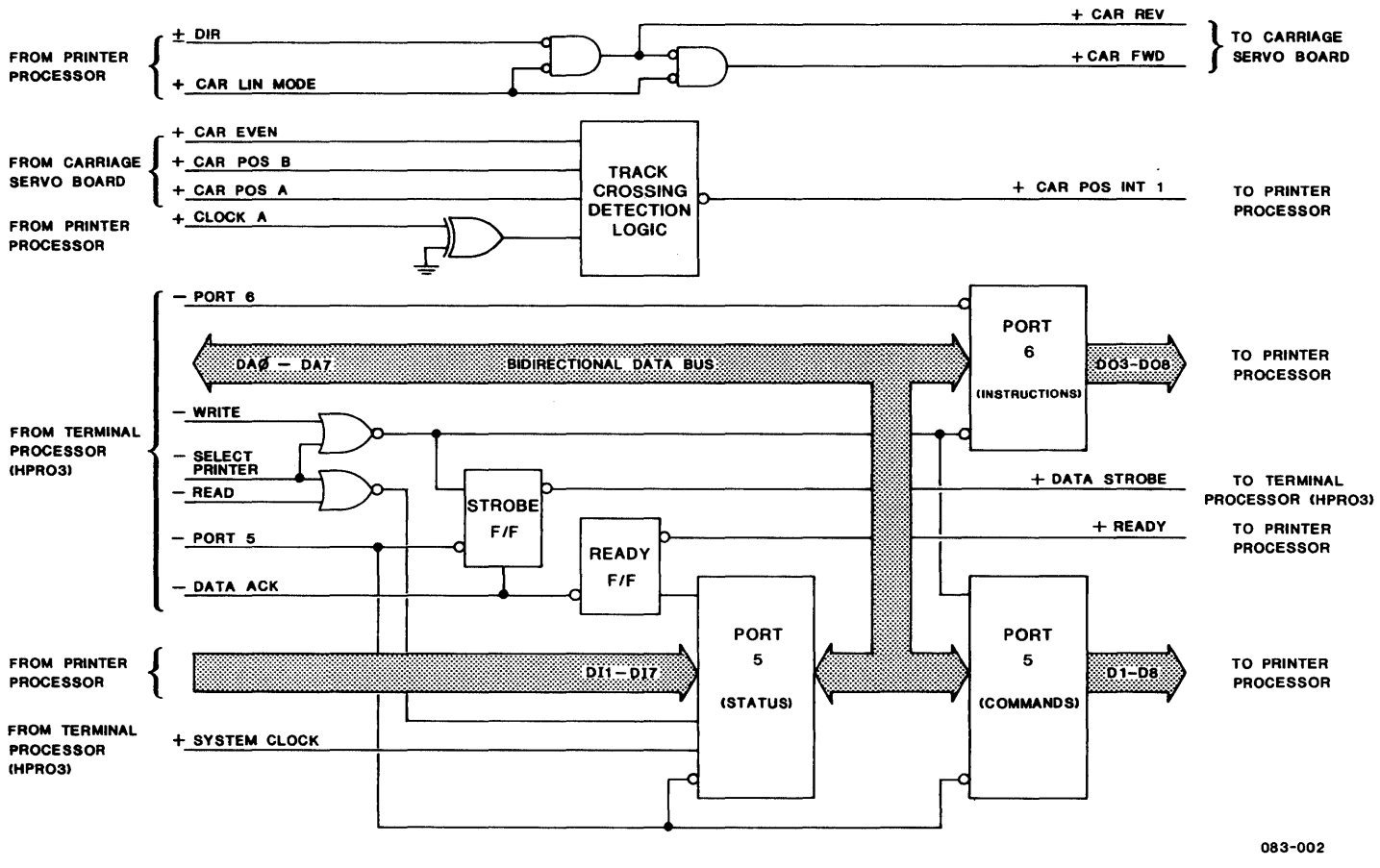


Figure 2-8. MXI Board Block Diagram

2.4.2 Carriage Position Data

The matrix printer prints characters using a dot matrix where the horizontal distance between sucessive dot positions is 1/100 inch (.254 mm). The purpose of this circuitry is to generate a 4 μs pulse when, and only when, the carriage has moved the print head 1/100 inch in either direction (left or right) from the position represented by the preceding pulse. This circuit is called the Track Crossing Detection Logic.

The printer's carriage servo motor includes a shaft position transducer that transforms a two-phase sinewave input into a composite output. The instantaneous value of the output is compared with the input and used to produce three square waves called +CAR POS A, +CAR POS B, and +CAR POS EVEN. The high and low status of these square waves changes with respect to actual carriage travel, so that (depending on the direction of carriage movement) two of them (EVEN and A or B) will be opposite polarity when the third (A or B) changes polarity. This event occurs once for each 1/100 inch of carriage movement and is called a track crossing point. The circuit output is a 4 us pulse called +CAR POS INT 1, and is supplied to the printer microprocessor as an interrupt signal, telling the microprocessor to interrupt its normal program and update carriage position data.

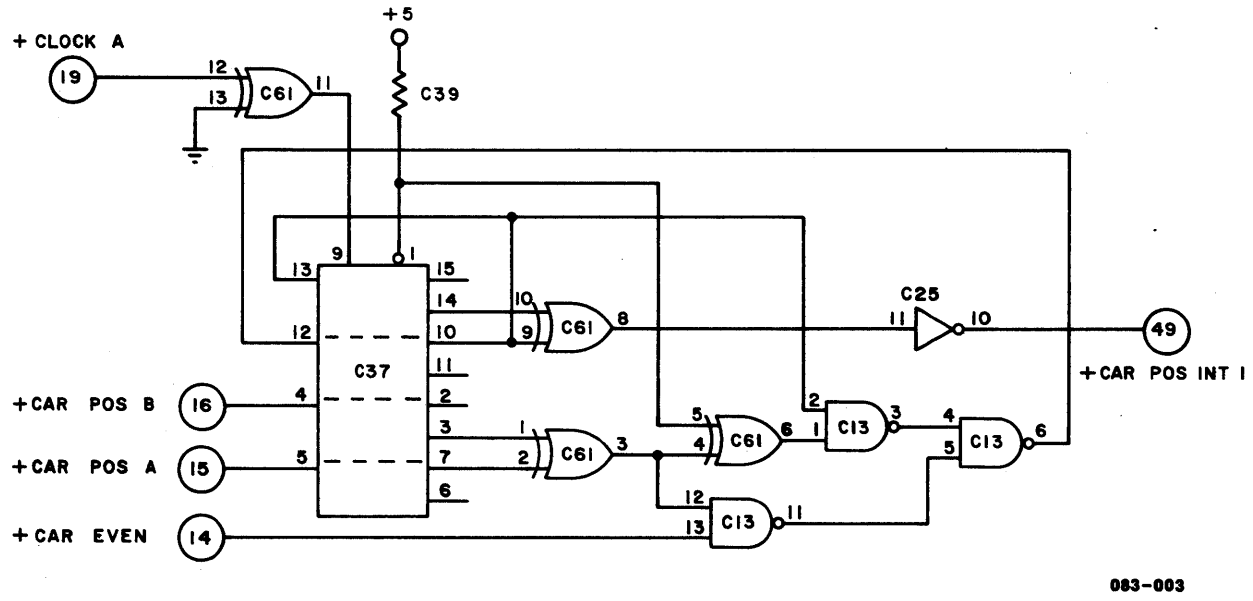


Figure 2-9. Track Crossing Detection Logic

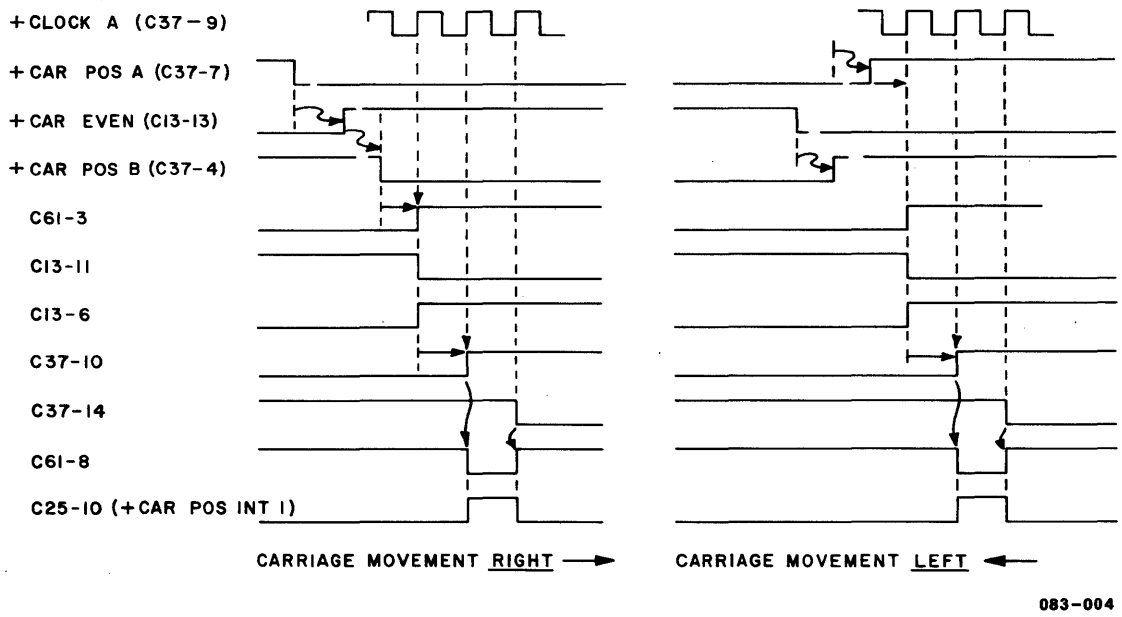


Figure 2-10. Track Crossing Detection Waveforms

Referring to Figures 2-9 and 2-10, device C37 is a series of D-type flip-flops with their Clear input tied to +5 volts. In this situation the C37 Q outputs will follow the D input with positive clock input excursions. As shown by the waveforms in Figure 2-10, generation of the +CAR POS INT 1 signal for carriage movement to the right begins with a high to low transition of +CAR POS A, followed some time later (not clock related) by +CAR EVEN going low to high. With the preconditions met, and again some time later, +CAR POS B will go low. Then, with the next positive clock transition, the output of XOR gate C61-13 will go high, NAND gate C13-11 will go low, and NAND gate C13-6 will go high. C13-6 = high is supplied to C37-12 where, with the next positive clock transition, C37-10 goes high. This high drives the output of XOR gate C61-8 low, and is supplied to C37-13. C37-13 = high drives C37-14 low with the next positive clock transition to drive the output of C61-8 high again to end the pulse. Inverter C25-10 inverts the output of C61-8 to produce the 4 μs positive pulse on +CAR POS INT 1 that is sent to the printer microprocessor.

For carriage movement to the left, Figure 2-10 shows +CAR EVEN first going low, followed by +CAR POS B going high. Then when +CAR POS A goes high, the signals proceed through the logic as outlined above to produce the 4 μs output pulse.

2.4.3 Carriage Direction Commands

The PROCESSOR board provides a directional signal ($\pm$ DIR) to the MXI board where it is gated with the +CAR LIN MODE signal from the CARRAIGE SERVO board to produce the +CAR FWD and +CAR REV carriage direction signals for the CARRIAGE SERVO board.

The +CAR LIN MODE signal is active (high) only when the carriage is in detent (or stopped). This high +CAR LIN MODE signal causes both the +CAR FWD and +CAR REV output signals to become inactive (low). When the +CAR LIN MODE signal goes inactive (low), the polarity of the $\pm$ DIR signal will determine which of the two carriage direction signals will be active. A +DIR produces an active (high) +CAR FWD signal and an inactive (low) +CAR REV signal while a -DIR signal produces an inactive (low) +CAR FWD signal and an active (high) +CAR REV signal.

2.5 PROCESSOR (PRINTER) BOARD, PART NO. 24620-XX

The matrix printer's microprocessor consists mainly of six MOS-LSI chips: two Parallel Data Control (PDC) chips, two Read Only Memory (ROM) chips, one Random Access Memory (RAM) chip, and one Central Processor Unit (CPU) chip. Auxiliary devices such as a clock generator and addressable latch modules, a voltage regulator, a power-on delay circuit, and several control switches complete the PROCESSOR board circuits.

Figure 2-11 presents the PROCESSOR board circuits in simplified block diagram form. Its use along with the full schematic diagram in Section 4 and the following paragraphs should aid the reader in understanding the operation of the microprocessor.

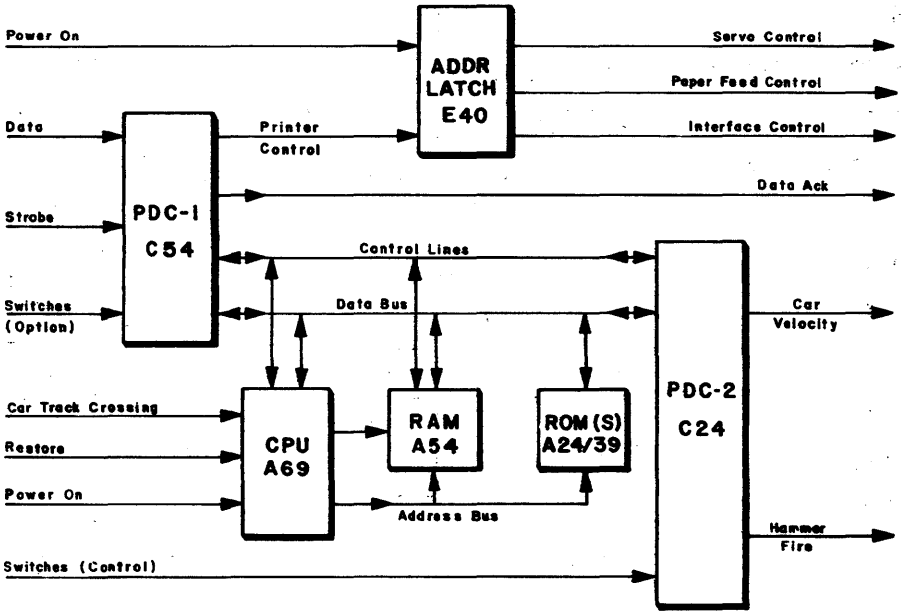


Figure 2-11. Processor Simplified Block Diagram

2.5.1 Chip Task Assignment

2.5.1.1 The PDC (Parallel Data Controller)

A PDC is a flexible parallel input/output device for interfacing the microprocessor to external circuits. It provides two independent, bidirectional 8-bit input/output channels, each of which may operate in a variety of parallel data transfer modes. The CPU is able to designate these 16 lines to operate as either inputs or outputs in blocks of 4.

PDC-1 C54 has 8 data inputs (pins 10-17) and a data strobe input all working as one channel. Latched +DATA signals are presented to these 8 inputs, along with the +DATA STROBE on pin 8, all from the MXI board. The transition of the data strobe causes the ASCII data to be sent into the PDC data buffer. The PDC will then produce a high signal at pin 9 to indicate that the PDC buffer is full. This signal is inverted to -DATA ACK=low and is sent to the MXI board to delay the output of the ACKNOWLEDGE signal to the controller until the CPU has taken the data from the PDC buffer. When this internal transfer of data has been completed, the PDC will drive its pin 9 low to produce -DATA ACK= high to the MXI board to permit the output of the ACKNOWLEDGE signal to the controller. This is referred to as the handshake mode of operation.

The second channel operates in the clocked I/O mode. The input lines (pins 30-37) are divided so that pins 34-37 are inputs and pins 30-33 are outputs, with pin 1 the input clock or strobe.

Pins 34-37 receive inputs from the option selection switches or the MXI board (pin 35 only). These inputs are read during a power on sequence or when a +DATA STROBE =high is received from the MXI board.

Pins 2 and 30-33 are outputs to Addressable Latch E40. Pins 30-32 address 1 of 8 latches in E40. Pin 33 inputs the data to be set into the addressed latch. Pin 2 controls the mode of operation of E40. When pin 2 is high, the output from pin 33 will be set into the addressed latch, and all other outputs will remain unchanged. When pin 2 is low, pins 30-33 have no effect on the outputs of E40. All 8 lines from E40 will output data previously set into the latch.

Pins 18-25 connect to the bidirectional data bus to transfer data to and from the CPU.

PDC pins 3-6 and 42 are processor activity control lines used by the several chips to communicate with each other. Pins 40 and 41 are clock signal inputs.

PDC-2 C24 operates in the static output mode. It functions as two groups of 8 latched outputs fed from the data bus. One group (pins 10-17) is designated as Hammer Data. Outputs on these lines control individual print wire firing through the HAMMER DRIVER board. The other group (pins 30-37) is designated Velocity Data. Outputs on these lines are commands used to generate carriage servo drive through the CARRIAGE SERVO board and are latched and remain static until changed by insertion of new command information. New command information occurs when the processor detects a need for a change in carriage velocity following a track crossing. Referring to the previous discussion, the MXI board generates the +CAR POS INT 1 pulse for each increment of carriage movement. Processor logic, in looking ahead at the stored data, may detect that the carriage has reached a tab position or the end of the print line. In this instance, the processor will begin to issue new carriage velocity commands to change the carriage velocity to meet the changing situation. In addition, three command line inputs (pins 1, 2, and 8) carry +TEST, +LINE FEED, and +SET TOF ZERO command signals from the MXI board instructing the processor to execute the indicated function.

2.5.1.2 The RAM (Random Access Memory)

RAM A54 is a device consisting of 2048 bits of read-write memory in a 256 x 8-bit configuration. It is used in the microprocessor as the general working register, the vertical and horizontal tab table, and as the processor's data buffer.

2.5.1.3 The ROM (Read Only Memory)

ROMs A24 and A39 are devices each consisting of 16,384 bits of read only memory in a 2048 x 8-bit configuration. They are used in the microprocessor for the storage of all microprocessor program instructions, including various constants such as the velocity table used for servo control, and the print font.

2.5.1.4 The CPU (Central Processor Unit)

CPU A69 is a device which contains all of the logic necessary to receive and decode 8-bit instruction words, and to perform all the required arithmetic and logic operations. Through a 14 line parallel (multiplexed) address bus, the CPU addresses 32,768 bits or 4096 bytes (8-bits/byte) of read only memory (ROM), and with the same 14 line bus also addresses 2048 bits or 256 bytes of random access memory (RAM). The CPU functions as an 8-bit parallel data processor, and in conjunction with the RAM, the ROMs, and the two PDCs forms the microprocessor for the matrix printer.

2.5.1.5 The Clock Generator Circuit

Clock module E8, along with 3.58 MHz crystal D8, make up the printer's basic clock generator. The clock output frequency is 256 kHz on pins 1, 4, and 10. Pins 1 and 10 are designated CLK A, and pin 4 is designated CLK $\overline{B}$. The output at pin 10 includes a driver which makes this output TTL compatible. Inverter D18-2 inverts the CLK A signal for use in the MXI board circuits.

2.5.1.6 The 12 Volt Regulator Circuit

Module E66 and its associated components form a circuit which lowers the -15 volt input to -12 volts, and regulates the output for use in the microprocessor circuits.

2.5.1.7 Summary

In overview, the matrix printer's microprocessor controls machine operation by receiving, storing and executing commands. As each command is executed, the processor signals its status to the terminal microprocessor through the MXI board, to keep the terminal microprocessor constantly updated. Only in the RESTORE activity does the printer microprocessor program digress. The microprocessor will, by itself, initiate a RESTORE sequence under the following conditions:

- o When instructed to backspace (BS) past the left margin.
- o When instructed to print (CR or SI) past column 132.
- o When instructed to tab (HT or VT) with a value greater than 127.
- o When the carriage fails to move when commanded.

NOTE

If the carriage still does not move during the restore sequence, the microprocessor will issue the +SERVO DISABLE signal to prevent circuit damage.

- o When POWER ON goes low during machine operation.

The RESTORE sequence can also be commanded by the terminal microprocessor.

2.6 CARRIAGE SERVO BOARD, PART NO. 24625-XX

Refer to the CARRIAGE SERVO board schematic diagram. Figure 2-12 is a simplified block diagram of the circuits on the CARRIAGE SERVO board.

As described earlier, the Track Crossing Detection Logic circuit on the MXI board makes use of a series of three squarewaves on the PROCESSOR board to update its carriage position file. The development of these squarewaves in sync with actual carriage movement is one of the two major functions of the CARRIAGE SERVO board. The second major function of this board is to provide an error signal to the CARRIAGE POWER AMPLIFIER board for use in developing carriage servo drive signals.

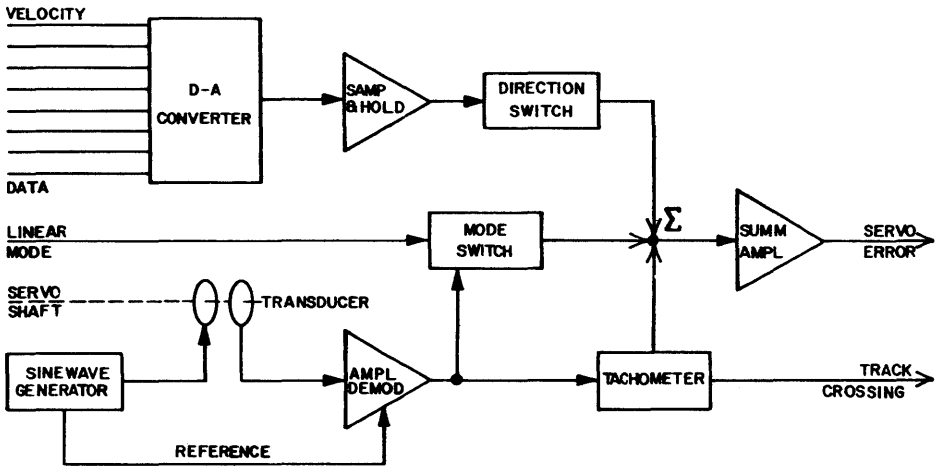


Figure 2-12. Carriage Servo Block Diagram

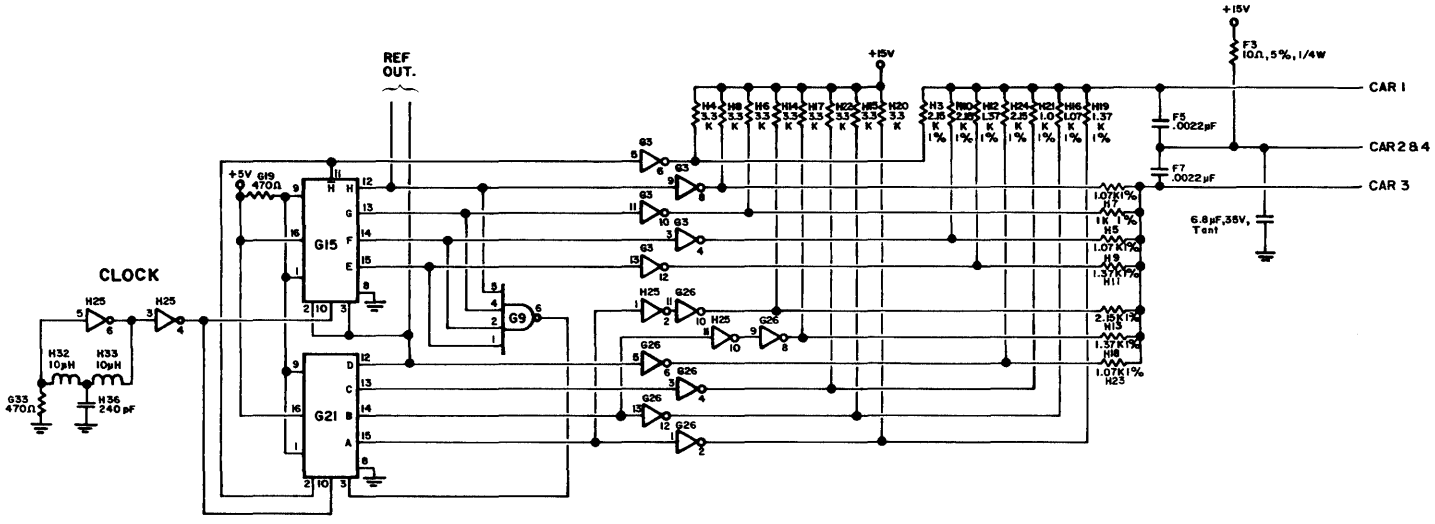
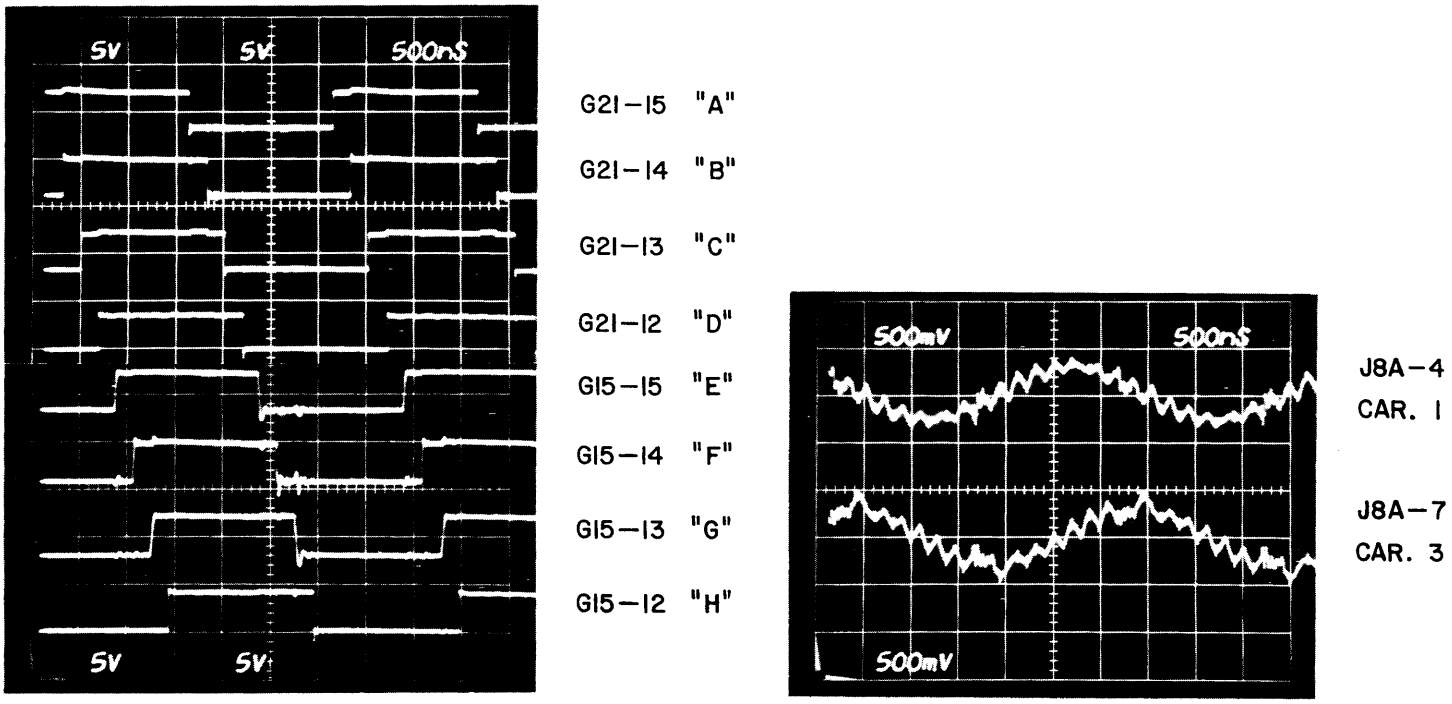


Figure 2-13. Digital Sinewave Generator

NOTE: All waveforms pictured in this section were taken with the oscilloscope synchronized to the A output of shift register G21-15 during carriage forward movement at 200 cps while printing the test line.

2.6.1 The Digital Sinewave Generator

Figure 2-13 is a partial schematic diagram showing the Digital Sinewave Generator. Figure 2-14a shows the waveforms generated by this circuit. The two modules G15 and G21 are 4-bit parallel access shift registers which are driven by a clock circuit with an output of about 5 MHz, connected to form a divide-by-16 circuit. The outputs of G15 and G21 are squarewaves as shown in Figure 2-14, where the output G21-15=high is followed one clock cycle later by G21-14=high and so forth. When G15-12 goes high, feedback through G15-11 and through NAND gate G9-6 drives the output G21-15 low. This condition then cascades through the registers again until G15-12 goes low, when G15-11 will drive G21-15 high to start the cycle again. These squarewave outputs are connected through inverters, pull-up resistors, and load resistors to two output lines. The inverters act as switches, allowing current to flow through the associated load resistor whenever the inverter output is low. Seven of the inverter outputs are selected for summation to form each of the two signals CAR 1 and CAR 3. The values of the several load resistors plus a capacitor from each of the output lines to their common return line produces the two-phased sinusoidal waveforms shown in Figure 2-14b. These signals are fed to the stator windings on the carriage servo's position transducer.



(a) (b)

Figure 2-14. Digital Sinewave Generator Waveforms

2.6.2 Servo Position Transducer

The Servo Position Transducer consists of rotor and stator members made up as flat disks with windings laminated on adjacent surfaces. The rotor is mounted on the free end of the carriage servo motor shaft, with the stator mounted over it and fastened to the motor casing. Output signals from the rotor are picked up by means of an axially mounted rotary transformer as CAR 5 and CAR 6 signals.

As shown in Figure 2-15, the stator has an eight segment winding, with alternate segments connected together to form two groups of four segments each. The four segments of one group are displaced laterally from the other group by a distance equal to one-half a winding width. This displacement is equal to a 90° phase difference. The rotor has one symmetrical winding.

The two sinusoidal waveforms shown in Figure 2-15 are introduced into the transducer's stator windings, and are coupled electromagnetically to the transducer's rotor winding. Since all windings in the device are nearly 1:1, the only transformation of the inputs is that the summed output is phase modulated by rotor movement. The phase modulated output is supplied back to a 3-stage amplifier and demodulator circuit on the CARRIAGE SERVO board.

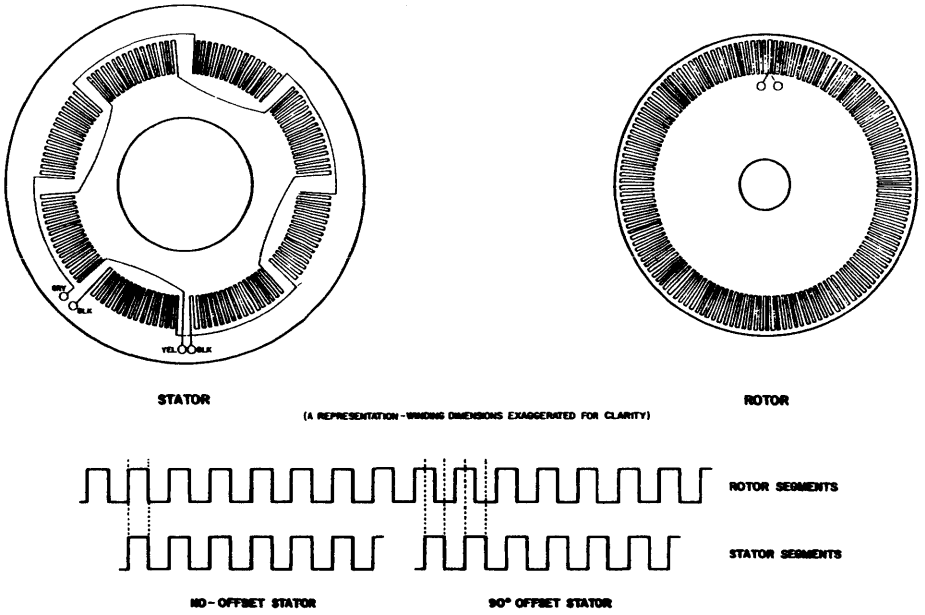


Figure 2-15. Servo Position Transducer

2.6.3 Servo Feedback Amplifier

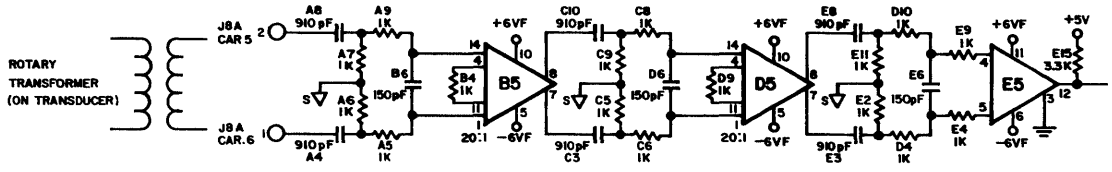
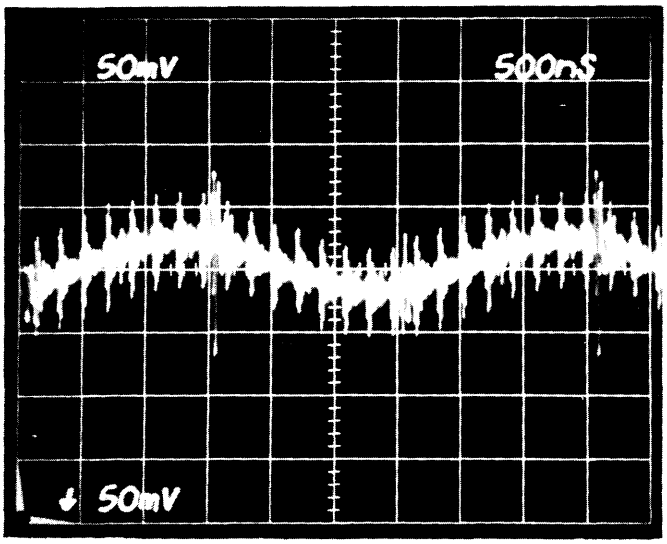


Figure 2-16. Servo Feedback Amplifier

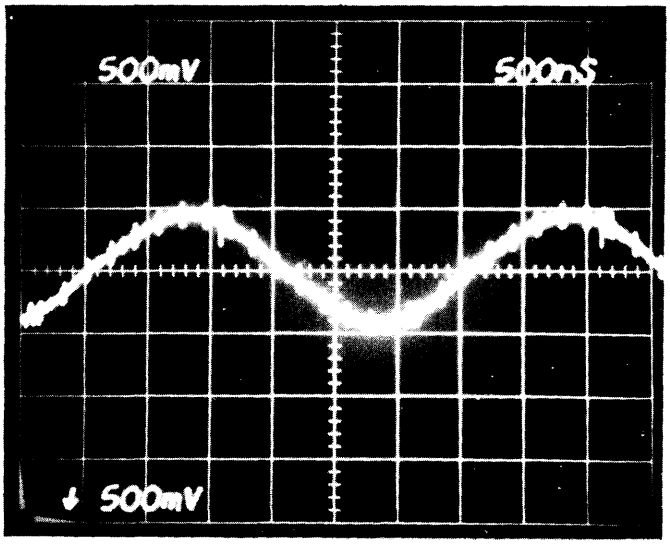
Figure 2-16 is a partial schematic diagram showing the Servo Feedback Amplifier. Figure 2-17 shows waveforms taken in this circuit. Waveform A is the phase-modulated servo transducer output, as seen at the input to the first video amplifier B5-1/-14. Amplifier B5 has an adjusted gain of ≅ 20. It amplifies and partially filters the input (B). The second video amplifier D5, also with a gain of 20, further filters the signal and generates a 10 volt p-p output waveform (C) which displays some squaring effect of saturation limiting. This output is applied to a high speed squaring comparator module E5. E5 is overdriven, and produces a squarewave output.



A

1st VIDEO AMPL. INPUT

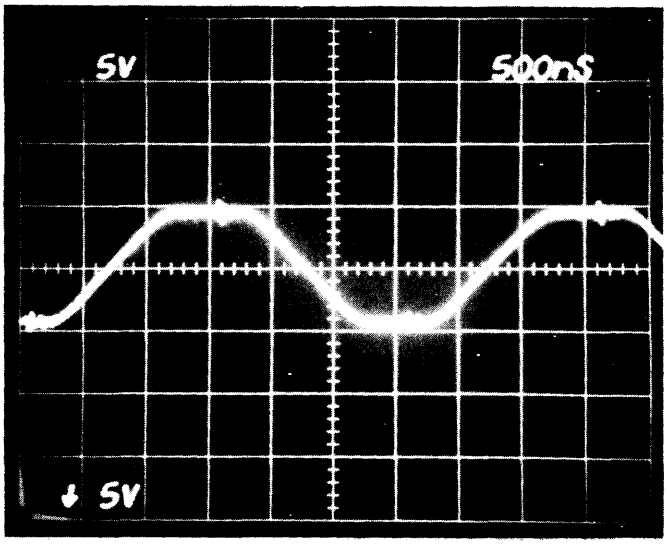
B5 — 1/14 (B5—1 INVERTED)



B

1st VIDEO AMPL. OUTPUT

B5—7/8 (B5—7 INVERTED)



C

2nd VIDEO AMPL. OUTPUT

D5 — 7/8 (D5—7 INVERTED)

Figure 2-17. Servo Feedback Amplifier Waveforms

2.6.4 Servo Feedback Demodulator/Amplifier

Figure 2-18 is a partial schematic diagram showing the Servo Feedback Demodulator/ Amplifier circuit. Figure 2-19 shows waveforms taken in this circuit.

The squarewave output of comparator E5 is inverted and applied to Exclusive OR gate D18-8 as the squared and inverted phase-modulated signal from the carriage servo transducer. This output of D18-8 is applied to Exclusive OR gates D18-3 and D18-11 along with reference squarewaves from the sinewave generator. Refer to Figure 2-19. Observe the two inputs to either D18-3 or D18-11, along with its output, on a multichannel oscilloscope which is synchronized to the sinewave generator while slowly moving the carriage by hand. The squarewave input from gate D18-8 (B) will appear to move with respect to the input on pin 1 or 12 from the sinewave generator (A). Then, the output (C) from either D18-3 or D18-11 will be a squarewave whose relative high-low status will vary as the high-low states of the two inputs vary with respect to each other. Figure 2-20 illustrates the development of the output waveform (C) from the two squarewave inputs (A and B), and further shows the sawtooth waveshape developed in the integrating circuits for input to amplifiers A18-10 and C18-12. The output of A18-10 is then supplied to amplifier A18-12. These three amplifiers produce the waveshapes called CAR POS SIG #1, CAR POS SIG #2, and CAR POS SIG #3.

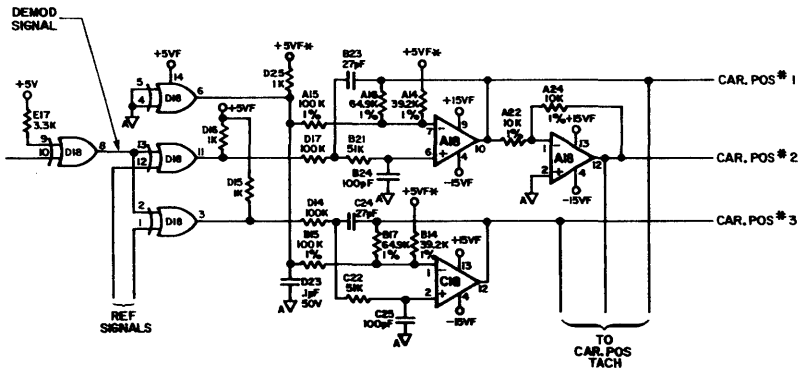


Figure 2-18. Servo Feedback Demodulator/Amplifier

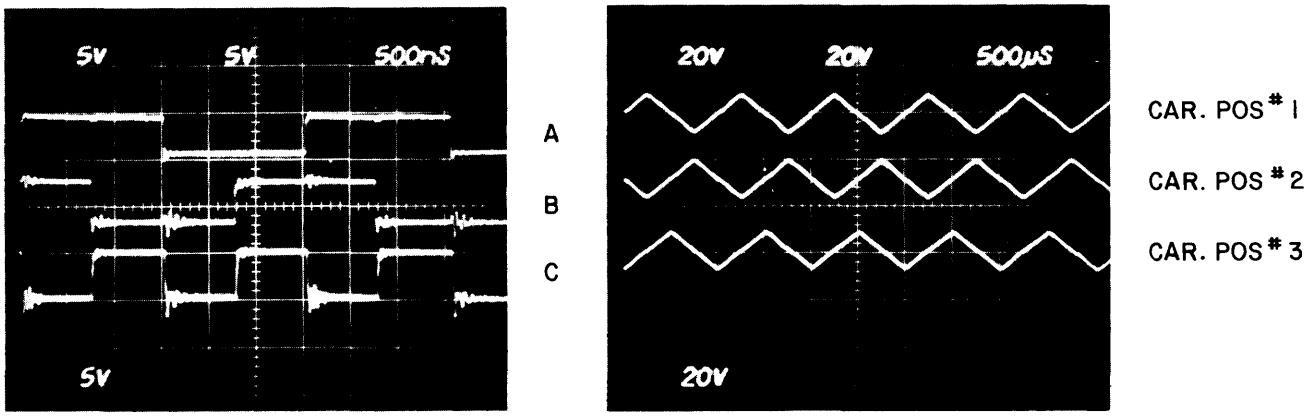


Figure 2-19. Servo Feedback Demodulator/Amplifier Waveforms

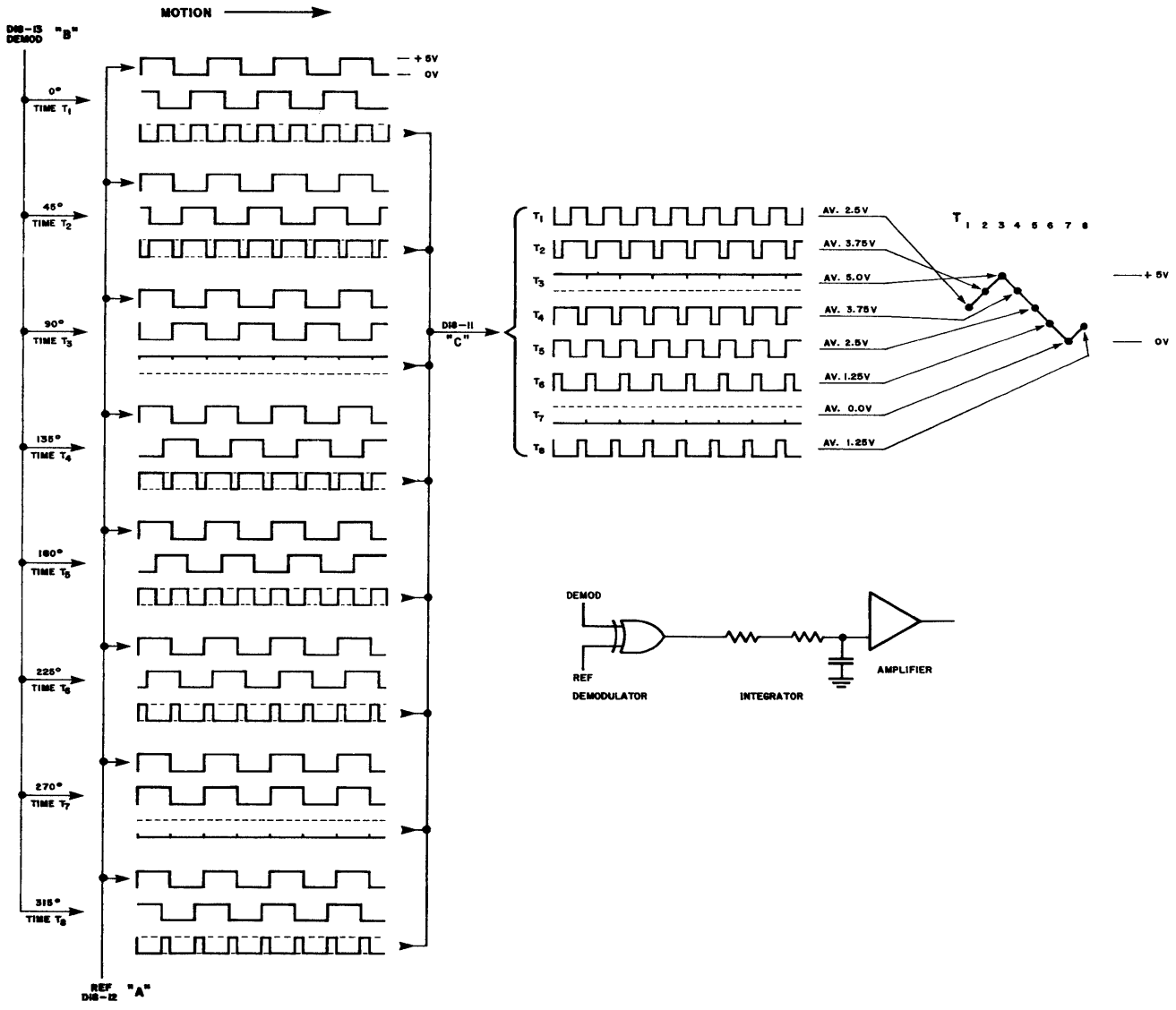


Figure 2-20. Waveform Analysis

2.6.5 Carriage Position Tachometer

Figure 2-21 is a partial schematic diagram showing the Carriage Position Tachometer and associated circuits. Figure 2-22 shows waveforms taken in these circuits.

The design of the transducer on the carriage servo motor is such that each complete cycle of the sawtooth waveform input to these circuits represents 2/100 inch (.508 mm) of carriage travel, or two "track crossing" points. Thus, while these inputs do not vary in amplitude, they do vary in frequency. This variation (or modulation) follows actual carriage speed, with the waveshape itself tracking carriage position.

Refer to Figure 2-22. Modules E39 and F39 are high speed comparators. Their inputs are the triangular CAR POS SIG waveforms A, B and C. Their actual outputs are square-waves. The duration of these squarewaves follows the frequency of the sawtooth inputs. They pass through inverters, whose outputs are waveforms E and F from comparators F39 and E39 respectively, and are sent to the MXI board as CAR POS A and CAR POS B. The CAR POS SIG #3 is also sent through inverting amplifier C18-10, comparator F39-7, and inverter E27-8 to develop the CAR EVEN signal also supplied to the MXI board.

The CAR POS A and B squarewaves are also channeled through a series of inverters and NAND gates to supply waveforms F, G, H, and I. These signals are used to control the feedback FETs C39-7, -10, -2 and -15 respectively.

The three CAR POS SIG triangular waveforms, plus CAR POS SIG #3 inverted are supplied to the control FETs through differentiating networks. Figure 2-23 shows the waveforms taken at the capacitor-resistor junction in each network. The control pulse to each FET will turn the FET on to pass either the positive or the negative part of the differentiated signal, depending on the direction of carriage movement. Since carriage velocity is seen here as frequency, the higher or lower the velocity, the higher or lower the level of the differentiated squarewave. The voltage levels of the outputs of the FETs are applied one at a time to the input (pin 1) of amplifier A39-12 representing carriage velocity. A39-12 inverts the input and presents it to the carriage velocity summation junction (pin 7) of Servo Summation Amplifier A39-10 as negative feedback.

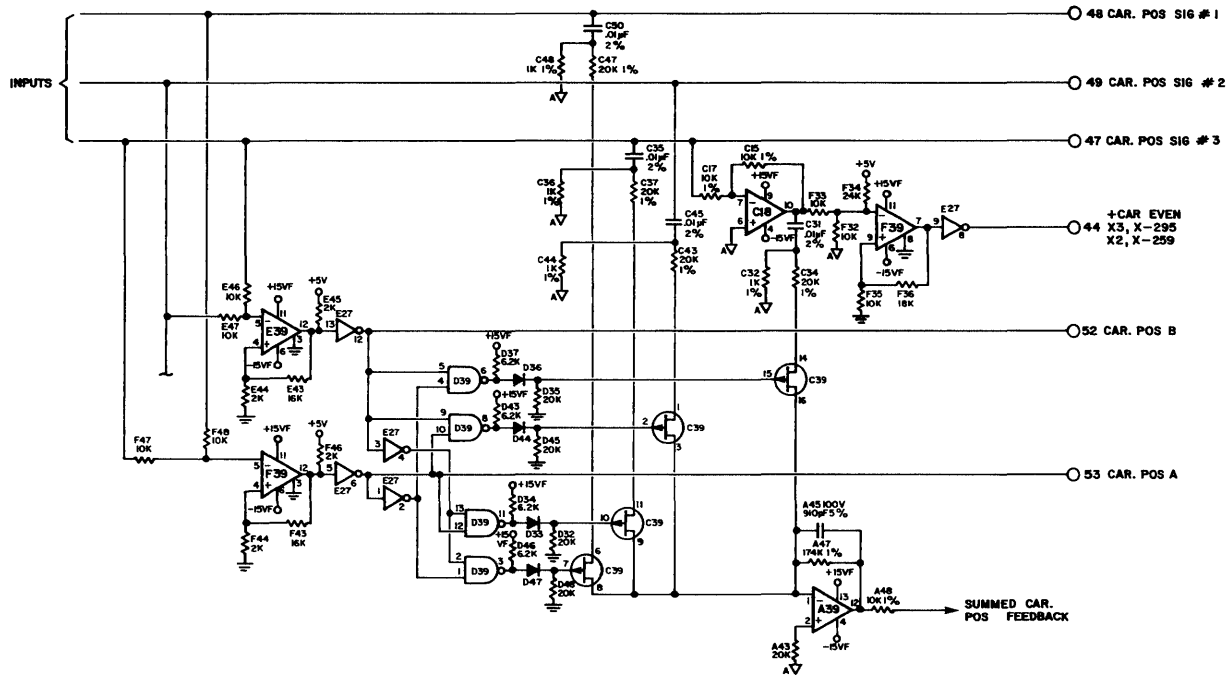
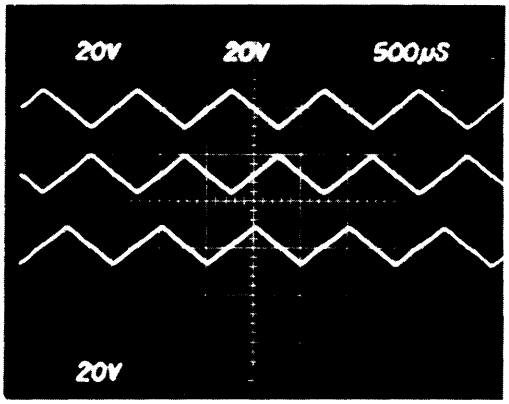
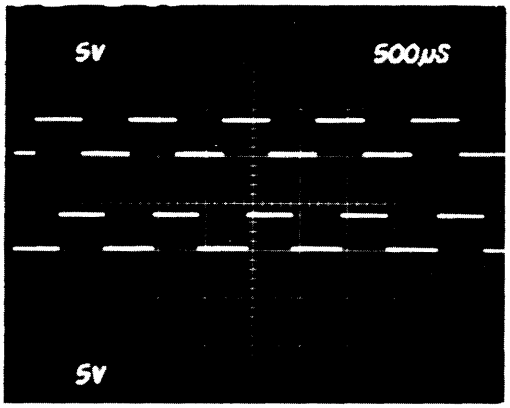


Figure 2-21. Carriage Position Tachometer





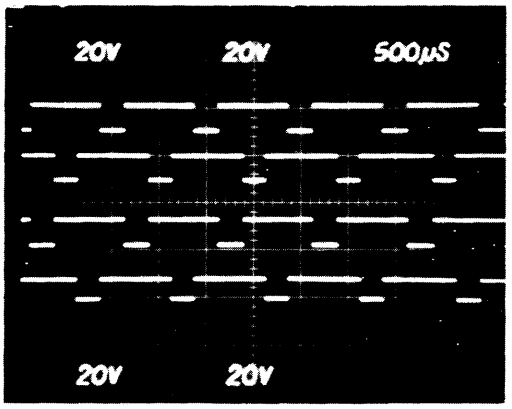


Figure 2-22. Carriage Position Tachometer Waveforms

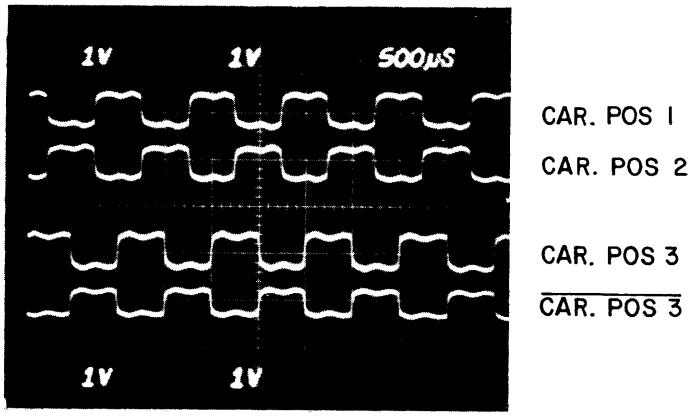


Figure 2-23. Carriage Position FET Input Waveforms

2.6.6 Carriage Velocity Command

As discussed earlier, the printer microprocessor looks ahead in its buffer, determines the carriage direction and velocity requirements for the upcoming print situation, and adjusts its commands to the CARRIAGE SERVO board accordingly. The velocity command arrives on the CARRIAGE SERVO board in digital form, and is converted to an analog form which is then used to develop a velocity command voltage level. This voltage level is then adjusted in polarity to set the direction of carriage movement, and applied to a summing junction where it is summed with a negative feedback voltage. The resultant is amplified and sent to the CARRIAGE POWER AMPLIFIER board as CAR SERVO ERROR, a signal whose level and polarity is used to generate the carriage servo motor drive to propel the carriage in the right direction at the right velocity.

2.6.6.2 The D-A Converter

Module H39, a D-A Converter, converts the binary input from the printer microprocessor to a current. The amplitude of this current represents the carriage speed command. The circuit's operating parameters are set by the value of the resistor in the +5V supply line to pin 14 such that when all digital inputs are high, the output current at pin 4 will be 99.6% of the reference current (approximately 1 mA) on pin 14. When all digital input signals are low, the output on pin 4 will be 0 mA. G39-10 is a current-to-voltage converter, with its instantaneous output voltage level stored in capacitor G34 for reference between updating inputs from the microprocessor.

2.6.6.3 Carriage Direction Switches

The output of the D-A Converter circuit at G39-10 is applied to the FWD control FET at B39-14, and to inverting amplifier G39-12. The inverted output from G39-12 is then applied to the REV control FET at B39-3. The outputs of both FETs are then tied to the carriage velocity summation junction (pin 7) of Servo Summation Amplifier A39-10.

2.6.6.4 Carriage Linear Mode

An input from the printer microprocessor, +CAR LIN MODE, is used to control FET B39-7. Whenever the carriage is stopped, this signal is issued by the printer microprocessor to turn on the FET and apply the CAR POS SIG #2 signal directly to the summation junction. This signal serves to electrically detent the carriage servo motor to lock the carriage in position.

2.6.6.5 Servo Summation Amplifier

The Servo Summation Amplifier A39-10 has four inputs; speed signal forward, speed signal reverse, carriage linear mode signal, and tachometer negative feedback signal. The first three control carriage movement. The feedback stabilizes the servo system, and causes the carriage to accelerate (or decelerate) and move at the command speed without variation due to changes in mechanical load. The output, CAR SERVO ERROR, is limited to approximately 5.6 volts peak, and is negative for forward and positive for reverse carriage movement.

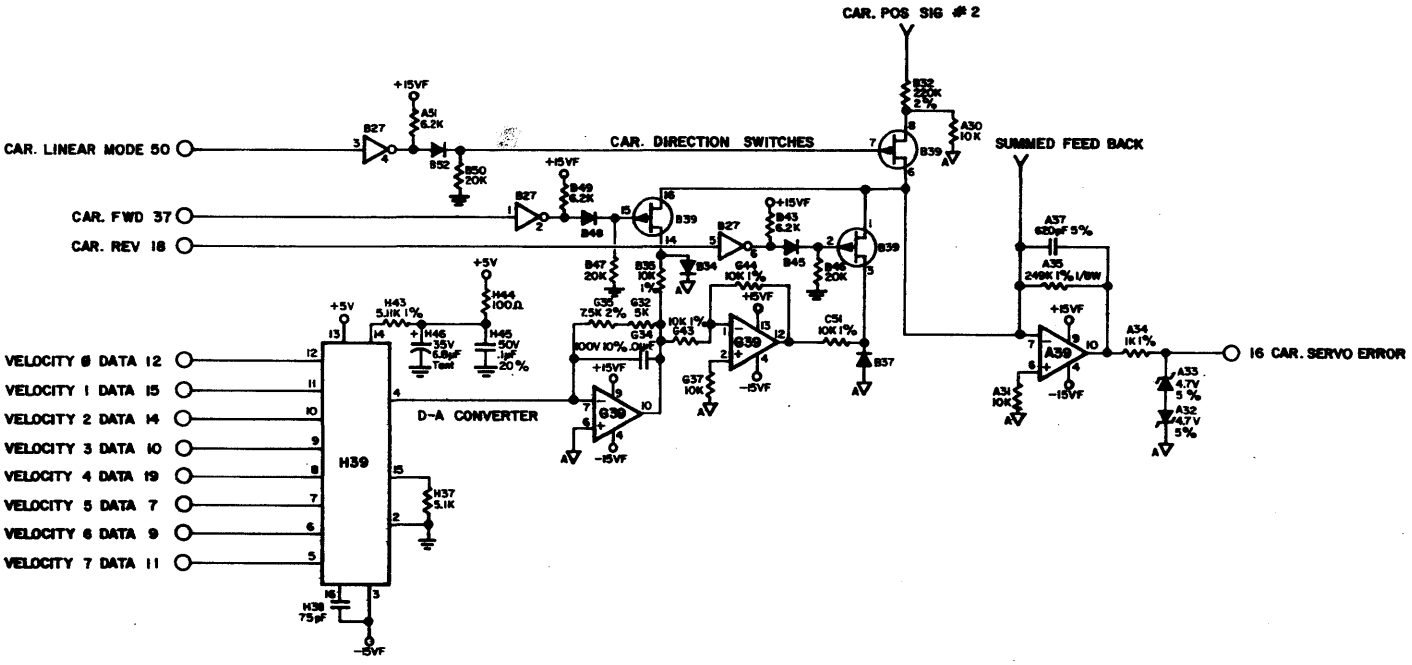


Figure 2-24. Carriage Velocity Command Circuits

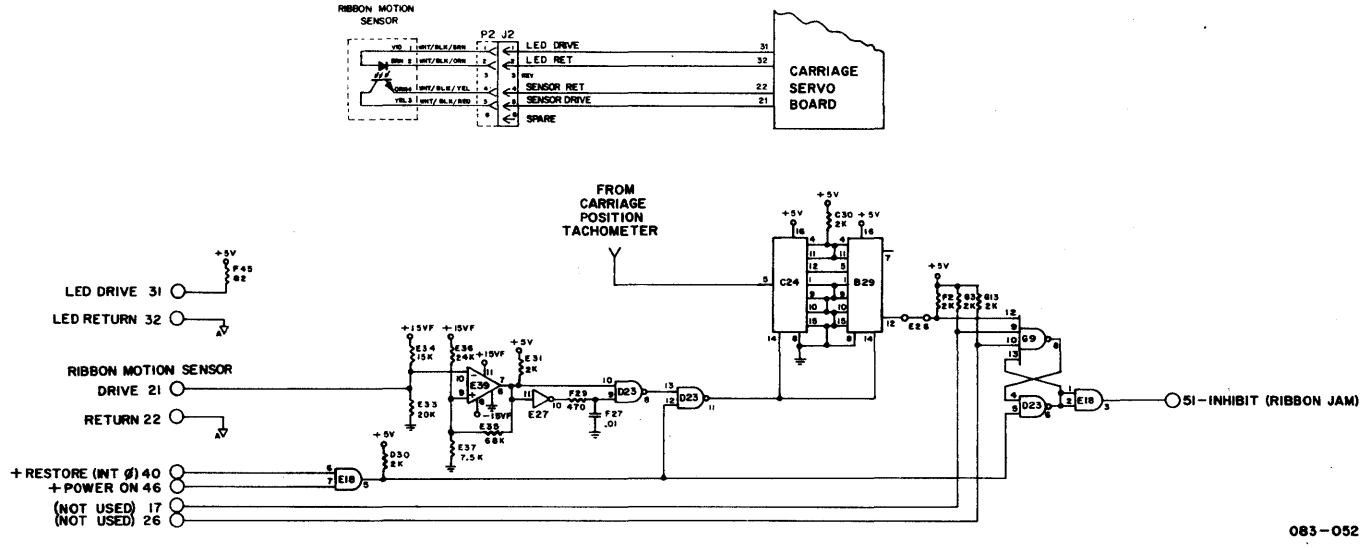


Figure 2-25. Ribbon Motion Sensor

2.6.6.6 Ribbon Motion Sensor (RMS) [See Figure 2-25]

The Ribbon Motion Sensor (RMS) circuit consists of a light sensitive phototransistor and a Light Emitting Diode (LED). This circuit works in conjunction with an idler wheel located inside all matrix ribbon cartridges. This idler wheel has reflective spokes and is driven by the physical motion of the ribbon moving through the ribbon cartridge. When the ribbon cartridge is installed correctly, an access hole in the cartridge is aligned directly over the RMS circuit to allow light from the LED to be reflected back from the idler wheel's reflective spokes to the light-sensitive transistor. The phototransistor converts these "light flashes" to electrical pulses and routes these pulses to the CARRIAGE SERVO board via the RMS DRIVE input at pin 21. On the CARRIAGE SERVO board, these ribbon motion pulses travel through comparator E39-7 and its associated circuitry to appear on pin 14 of counter modules B29 and C24. The CAR POS A pulse train from the Carriage Position Tachometer circuit is applied to input pin 5 of counter C24 whose output on pin 12 is connected to input pin 5 of counter B29. The output of these two counter modules on B29-12 is a pulse for every 256 -CAR POS A pulses at C24-5. (256 -CAR POS A pulses are the equivalent of 25 characters spaces of carriage movement.) The RMS pulses at pin 14 of the counter modules are Clear signals that reset both counters to zero. This action of continuously resetting the counters keeps the B29-12 output high.

Should the ribbon fail to move for any reason, the RMS pulses used as Clear signals to the counter modules are not produced. Any subsequent carriage movement soon accumulates the 256 counts needed to present a negative-going pulse at the output of B29-12. This negative-going pulse sets the G9/D23 latch output D23-6 low and causes the -INHIBIT signal at E18-3 to become active (low). The -INHIBIT = low signal is loaded into the Port 5 Status latch on the MXI board and read by the terminal microprocessor.

When an active (high) +RESTORE (INT Ø) signal from the MXI board is applied to AND gate E18-6, the G9/D23 latch is reset and the -INHIBIT signal becomes high (inactive) again.

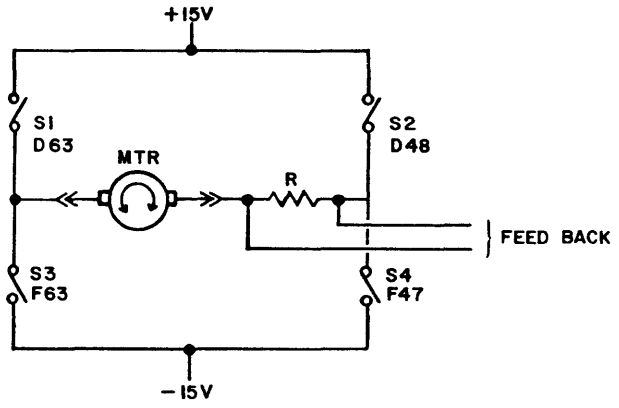


Figure 2-26a. Carriage Power Amplifier Simplified Diagram

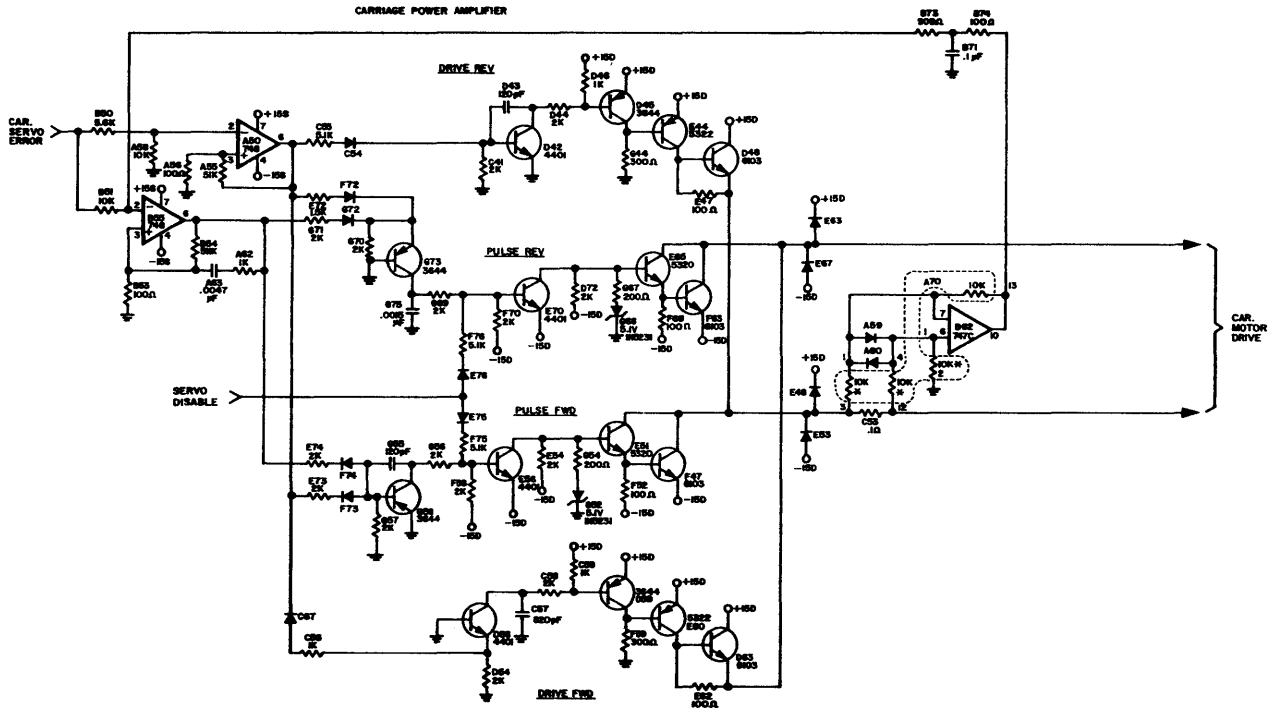


Figure 2-26b. Carriage Power Amplifier

2.7 CARRIAGE POWER AMPLIFIER BOARD, PART NO. 40525-XX

This assembly includes the Carriage Servo Power Amplifier, the Paper Feed Drivers, and the Power Monitor circuit. It is located in Slot D, and has a finned heat sink attached to it, to help cool the several drive transistors.

NOTE

Do NOT stand the terminal on its rear heat sink panels. The finned heat sinks are mounted on plug-in circuit boards which can be easily damaged by this practice.

2.7.1 Carriage Power Amplifier Circuit

This circuit supplies and controls current flow to the carriage servo drive motor. The circuit is designed as an H bridge, allowing all current to flow through the motor from supply to supply instead of through circuit ground. This feature helps to avoid circuit noise problems. Figure 2-26a illustrates the circuit in simplified form, where certain transistors (final drivers) in the actual circuit are represented as switches. It may be seen that closing switches S2 and S3 will cause electrons to flow through the motor left to right.

Refer to Figure 2-26b. Assume a CAR SERVO ERROR signal input of +1 volt for a commanded motor current of 1 ampere. The output from operational amplifier B55-6 will be low, and this will place a low potential on the base of transistor G58 to disable the Pulse Fwd circuits, and on the emitter of transistor G73, to turn G73 off. G73 being off turns transistor E70 off, which turns transistor E65 on to turn on the Pulse Rev switching transistor F63.

The error signal is also supplied to amplifier A50-6. The A50-6 output will be negative with a positive input, which will turn transistor D45 off and transistor E44 on to turn on Drive Rev switching transistor D48.

Referring again to Figure 2-25, transistor D48 is shown as switch S2, while transistor F63 is shown as switch S3. Turning these two transistors on establishes a current path from the +15 volt supply through D48, resistor C53 (R), the drive motor, and through F63 to the -15 volt supply.

Figure 2-27 is a simplified schematic diagram of the feedback circuit. This circuit includes the .1 ohm resistor C53 (R) located in one of the lines to the servo motor, across which is connected a precision balanced 10K resistor network and difference amplifier B62-10. The value of resistor C53 is such that its voltage drop to current ratio is 1 to 10. (.1 volt drop equals 1.0 ampere of motor current.) Difference amplifier B62-10 presents this voltage to the servo error input terminal 2 of amplifier B55-6. The two signals are summed at a ratio of 10 input to 1 feedback. As current through the drive motor approaches the commanded level, the output of B55-6 will diminish. When motor current matches command current, the Pulse Rev switching transistor F63 will be turned off. This removes motor current, which removes feedback voltage, and F63 is turned back on again. The circuit will oscillate in this manner to maintain motor current at the commanded level.

Should the Power Monitor circuit detect an input voltage error, it will generate a -CAR SERVO DISABLE signal. This signal will turn transistor E77 on which results in turning Pulse Fwd and Pulse Rev transistors F47 and F63 off to disable carriage servo movement.

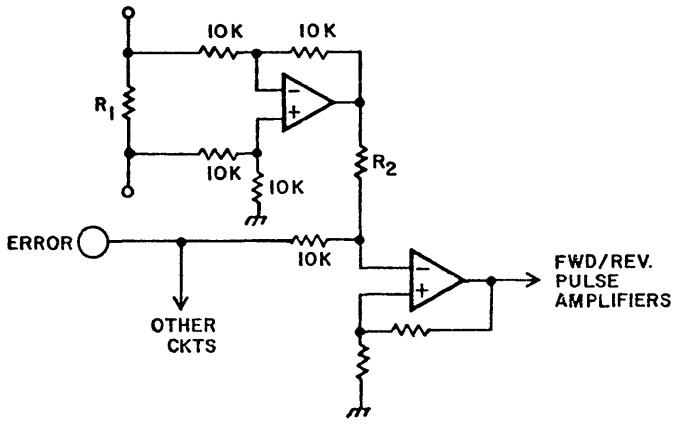


Figure 2-27. Simplified Feedback Circuit

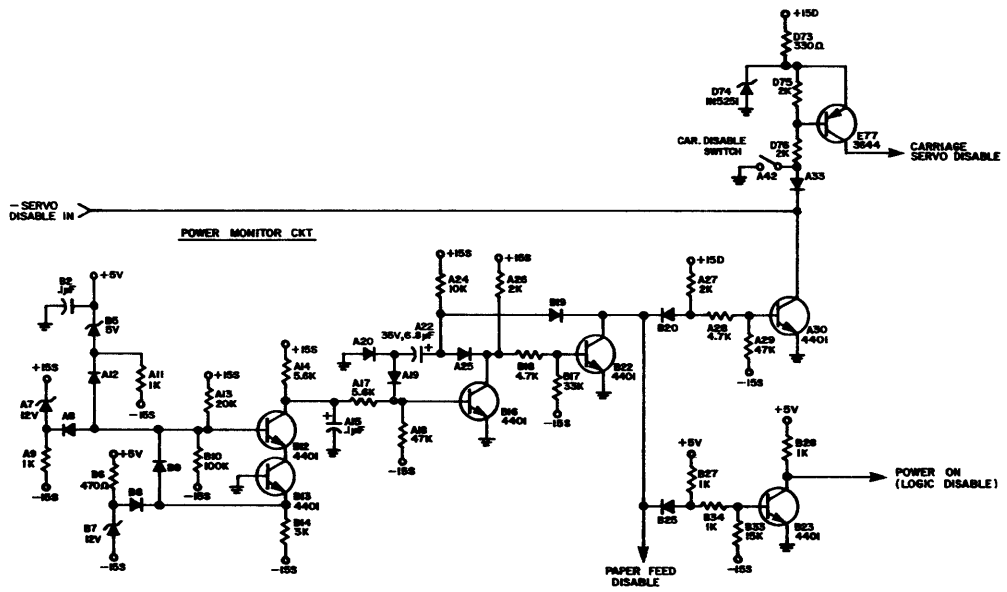


Figure 2-28. Power Monitor Circuit

2.7.2 Power Monitor Circuit

The purpose of this circuit is to inhibit all printer functions any time one or more of the three supply voltages of +5, +15, or -15 volts drops below a level where printer malfunction or component damage could occur as a result of the low voltage.

The circuit operates as follows. As power is applied, transistors B12 and B13 are off. Three divider networks begin to sample the +5, +15, and -15 volt levels being supplied: zener diode B5 and resistor A11 sample the +5 volt input; zener diode A7 and resistor A9 sample the +15 volt input; and zener diode B7 and resistor B6 sample the -15 volt input. As these voltages approach their appropriate values, diodes A12, A8, B8 and B9 (operating as an AND gate) are reverse biased, and transistors B12 and B13 turn on. Up to this time transistor B16 has been on and B22 off. When transistors B12 and B13 turn on, capacitor A22 begins to charge through resistor A24 and the emitter/base junction of B16, and transistor B22 is biased off. With transistor B22 off, transistors A30, B23, C36, and C34, are all biased on, and their outputs are all clamped low. This condition disables all printer functions as outlined. This condition will continue until capacitor A22 has charged sufficiently to turn transistor B22 on.

At the end of the delay (approximately 25 ms), transistor B22 is turned on discharging capacitor A22 and turning transistor B16 off. It will also turn off transistors A30, B23, C36 and C34, allowing all their outputs to go high. This removes the circuit disable clamps, starts the program counter in the printer microprocessor, and initiates a Restore sequence.

Any subsequent interruption in, or depreciation of, any of the three input voltages monitored, will disable the printer by action of this circuit. Complete restoration of power recycles this circuit, putting the printer back in operation with a Restore sequence.

2.7.3 Paper Feed Drive Circuit

Figure 2-29 is a partial schematic diagram of the Paper Feed Drive circuit. Figure 2-30 shows waveforms taken in the circuit. The circuit consists of two identical channels A and B, each feeding a field winding in the paper feed stepping motor. As shown in Figure 2-30, the signals in channel A lead the signals in channel B by 90°. This relationship produces clockwise rotation of the stepping motor shaft (as viewed from its shaft end) for upward paper movement only. Since the A and B channels are identical, only channel B will be discussed here.

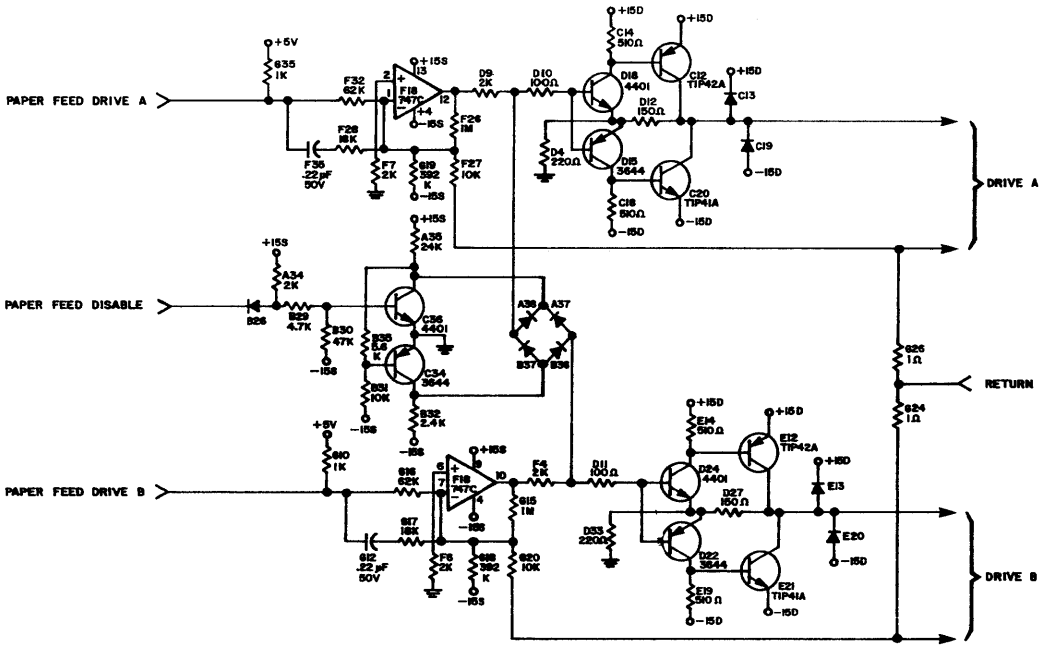


Figure 2-29. Paper Feed Drive Circuit

In operation, the squarewave PF B input on connector 10 is differentiated by a circuit consisting of capacitor G12, resistor G17, and resistor G20. This network provides a pulse to the input (pin 7) of operational amplifier F18-10 with a duration of approximately 4 to 5 ms. The op-amp F18-10 squares and amplifies the input, with the result coupled to current amplifiers D22/24-E12/21. The output drive current waveform (lower half of Figure 2-30) is applied to the B winding of the paper feed stepping motor (terminals T5 and T6).

The waveforms shown in Figure 2-30 represent one complete line feed operation. Examnation of the waveforms will disclose four level changes for each channel, or a total of eight level changes per line feed. The stepping motor shaft moves 7-1/2° per level change (A or B). Thus each line feed command produces 8 x 7.5 = 60° of shaft rotation for a line spacing of six lines per inch.

The paper feed motor is detented electrically at the end of each line feed operation. Again, discussing channel B only, a circuit consisting of resistors G18, G16 and G10 (-15 volts to +5 volts) provides enough output from amplifier F18-10 (about .4 amp motor current) to electrically detent the stepper motor.

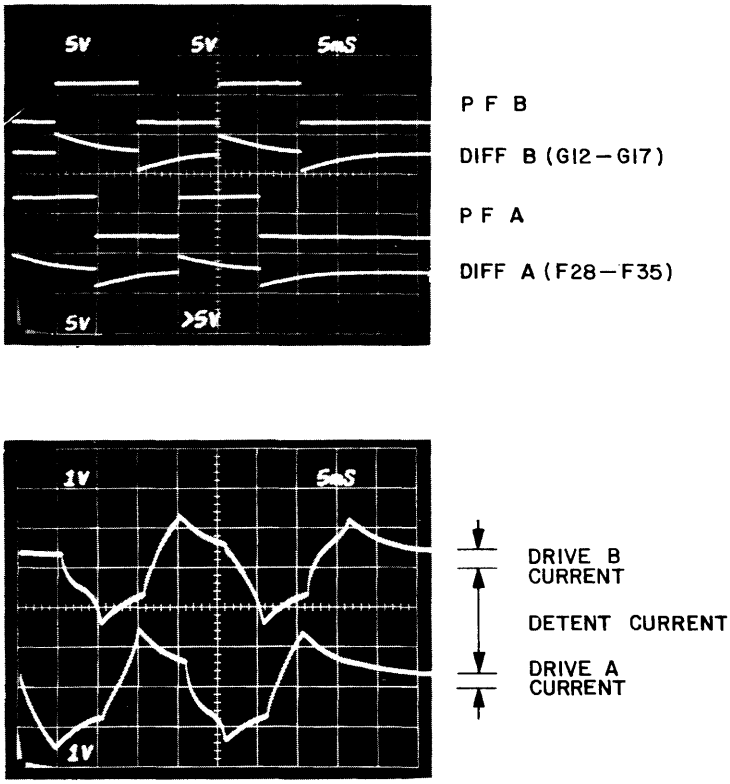


Figure 2-30. Paper Drive Waveforms

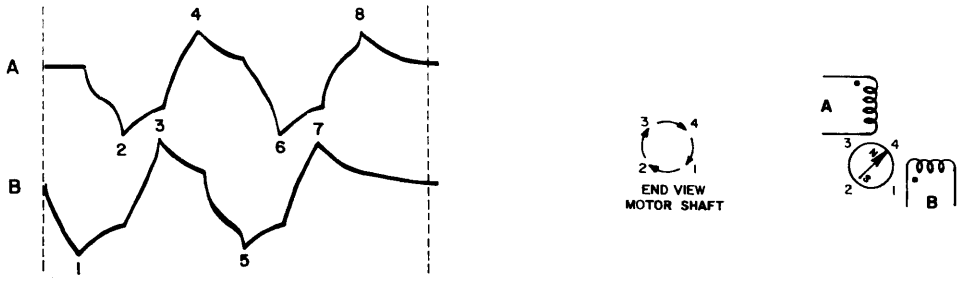


Figure 2-31. Typical Stepping Motor Rotation

Figure 2-31 illustrates the development of stepping motor rotation from two inputs 90° out of phase with each other. Actually, the paper feed stepper motor's rotor has a magnetic node each 7-1/2°. This would be difficult to illustrate. It should be noted, therefore, that for clarity the illustration depicts a stepping motor with magnetic nodes every 90° only.

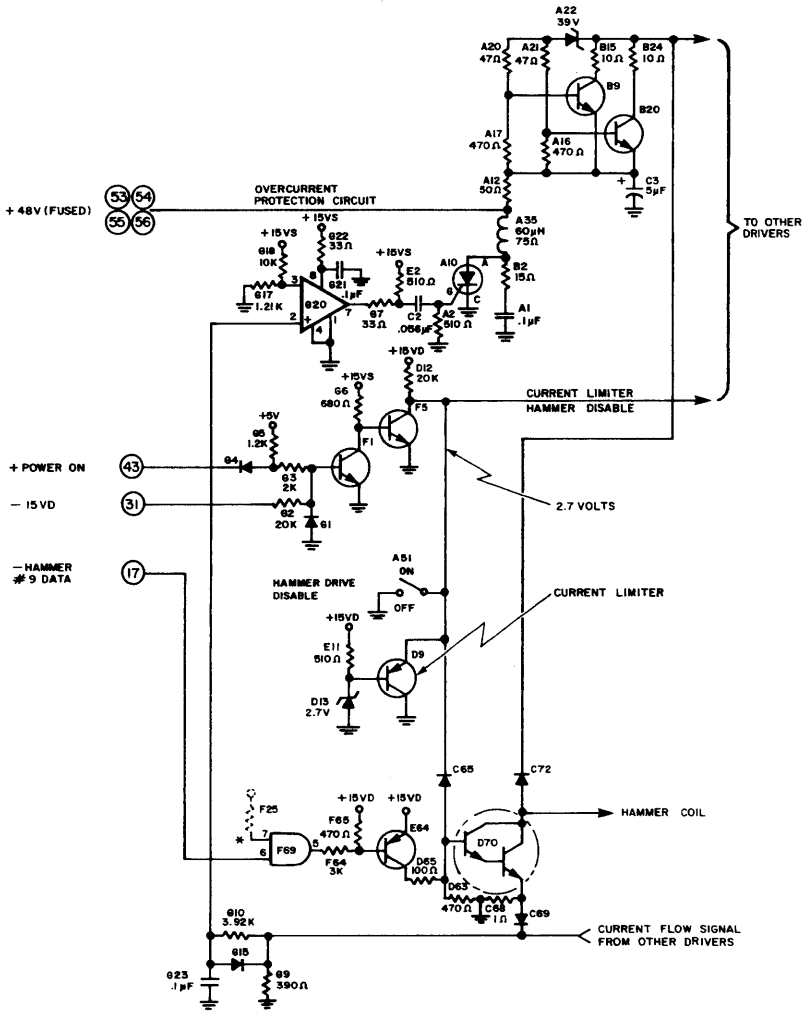


Figure 2-32. Typical Hammer Driver and Common Protection Circuits

2.8 MATRIX HAMMER DRIVER BOARD, PART NO. 24605-02

Refer to the MATRIX HAMMER DRIVER schematic diagram. This board contains nine identical Hammer Driver circuits. Figure 2-32 is a practical schematic diagram showing only one Hammer Driver circuit and its associated circuitry.

2.8.1 Hammer Driver Circuit

In operation, a -HAMMER "X" DATA=low (340ns) is applied to an AND gate to turn on a control transistor. This control transistor will turn on the hammer driver switch, a Darlington amplifier. Current then flows from ground through a 1 ohm resistor, through the driver and out through the hammer coil to +48 volts.

2.8.2 Hammer Coil Protection Circuit

As current flows through the hammer coil, it also flows through a diode and resistor G10 to begin charging capacitor G23. Should a defect occur in the hammer driver circuit, making the current through the coil too high or the drive pulse too long, capacitor G23 would be charged high enough to unbalance the inputs to comparator G20-7 in the Overcurrent Protection circuit. When this happens, G20-7 will gate SCR A10 to its on state, to short circuit the +48 volt supply to ground. This action will cause the 6400 μF capacitor C101 in the +48 volt power supply to discharge which will blow the special quick acting Type GBB-7 fuse in the +48 volt supply line and remove power before circuit or component damage can occur.

2.8.3 Surge Suppression

At the end of a hammer fire pulse, a surge is developed in the hammer coil circuit due to the collapse of the coil's magnetic field when the driver shuts off. A suppressor circuit, which includes transistors B9 and B20, acts to absorb these surges, store the energy in a capacitor, and bleed it slowly back into the +48 volt supply line.

2.8.4 Current Limiting

Transistor D9 and zener diode D13 work to limit the Darlington Amplifier outputs to about 2.7 amperes by clamping their input bases to about 2.7 volts. This action maintains hammer coil current to within necessary limits. Switch A51, when closed, grounds the Darlington Amplifier inputs preventing current flow to the hammer coils and thus disabling them.

2.8.5 Power Loss Protection

In the event of a loss of power, the Power Monitor circuit on the CARRIAGE POWER AMPLIFIER board will issue a +POWER ON=low signal to this circuit. Transistor F5 will turn on to ground the driver input in the same manner as closing the Disable Switch A51. This circuit thus works to prevent firing of the solenoids during power up or down.

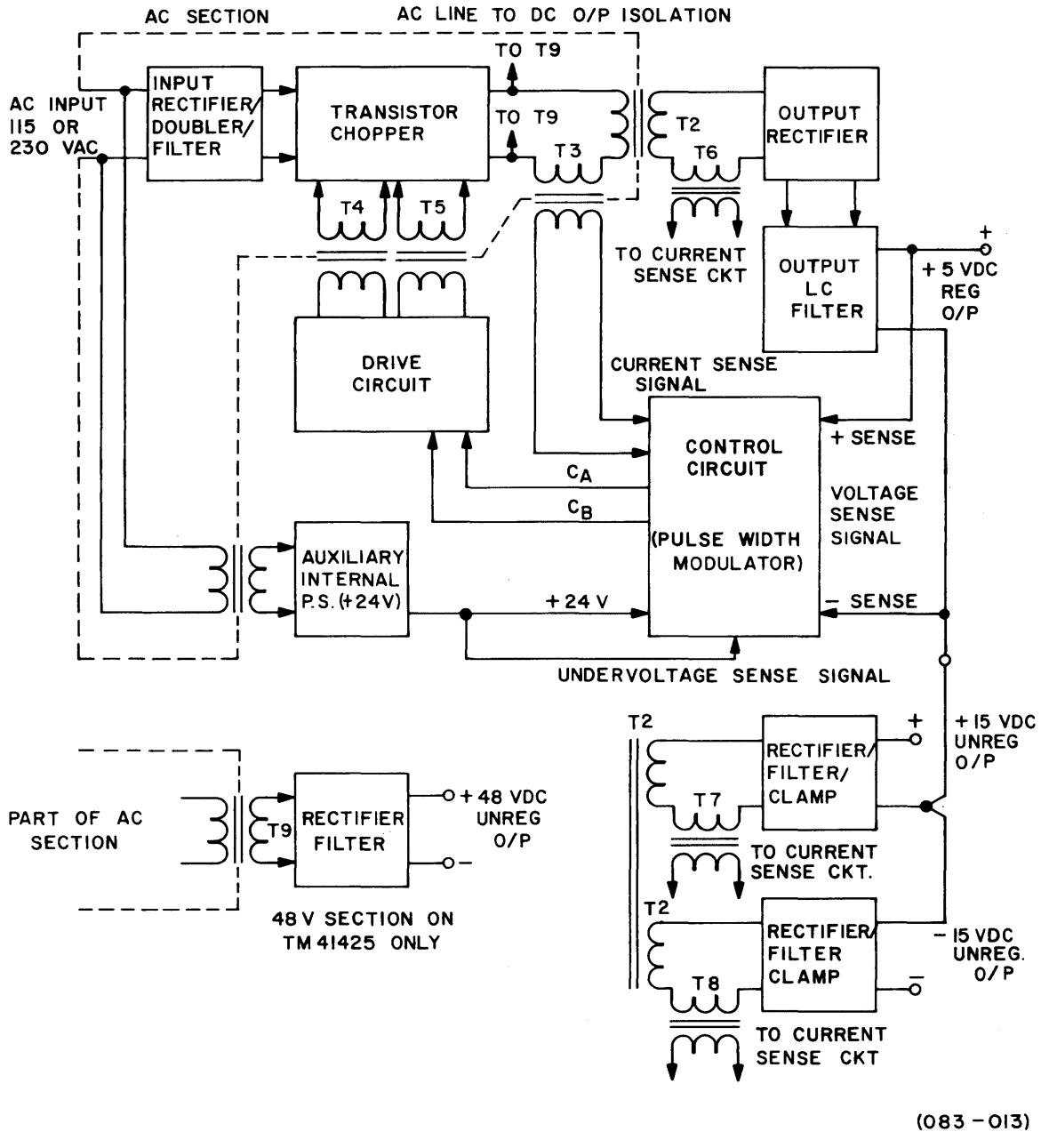


Figure 2-33. Power Supply Block Diagram

2.9 POWER SUPPLY, PART NO. 400062-01 (see Figure 2-33)

The main output of the Switching Power Supply is a pulse-width modulated chopper converter. The AC input is rectified, doubled and filtered to 300VDC and than chopped and transformed to a lower voltage by a half-bridge. This transformer secondary output (consisting of a quasi-square wave) is rectified and filtered to the final DC output value.

The output is sensed and the error signal voltage is amplified and used to control the pulse width of the chopper, thus regulating the output voltage within narrow limits under all conditions of the input line and the output load. The output and all control circuitry are isolated from the AC input line.

This power supply has input undervoltage sense, soft start control, output current limiting, output overvoltage protection and crowbar on the +5V. The unregulated ±15V outputs have current limiting circuits and overvoltage clamps.

2.9.1 Detailed Description (See Schematic 400062-XX)

2.9.1.1 Input Filter (See Figures 2-34 and 2-35)

The input filter consists of L1, C1, and C2, that form an RF noise suppression filter. R1 and R2 are thermistors with a high resistance at low temperature. The thermistors limit the input start-up current. The filter operation, including polarity and current flow is described by Figures 2-34 and 2-35. The strapping connections at T2 allow the use of the same assembly for 115 or 230VAC input. R3 and R4 are the bleeder resistors.

2.9.1.2 Chopper Section (See Figures 2-36 and 2-37)

Transistors Q1 and Q2 are alternately turned on and off at a 20 kHz rate. C7 is a balance capacitor and T3 is a current sensing transformer. R5 and C8 form a primary RC snubber to attenuate voltage overshoots. CR7 and CR8 prevent reverse conduction of Q1 and Q2 during transient conditions. The switching action of Q1 and Q2 applies a quasi-square voltage waveform of 300 volts peak-to-peak to primary of T2.

2.9.1.3 Output Rectifier and Filter. (See Figure 2-37)

The quasi-square voltage waveform is transformed down by T2. The output is rectified by BR1 and filtered by an LC filter, consisting of L2, C15, C30, and C31. Ripple and RFI are further reduced by C16 and C17. C9 and R25 form a secondary snubber network.

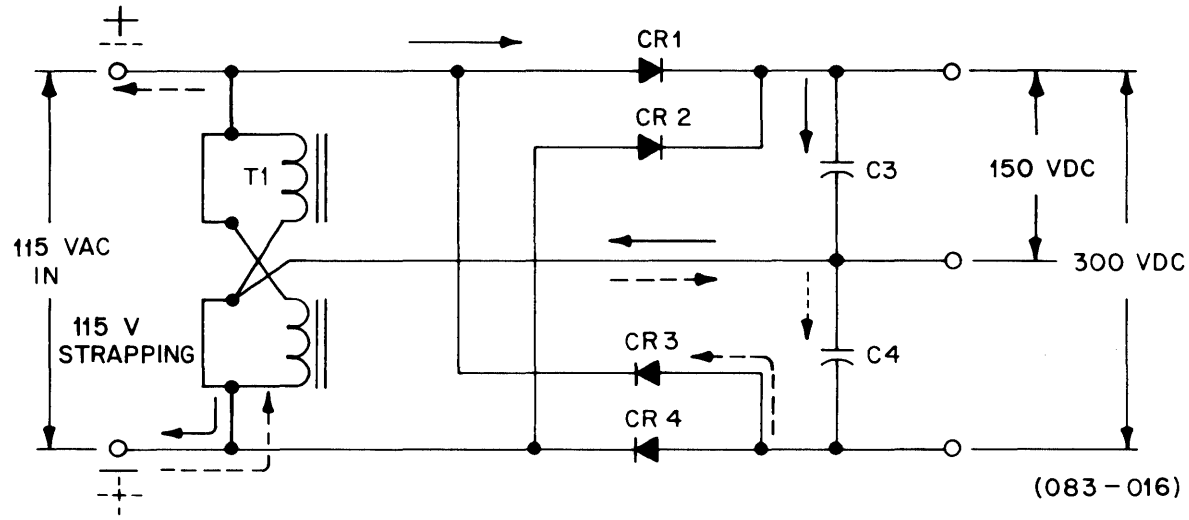


Figure 2-34. Simplified Input Rectifier/Filter/Doubler Section
(115 VAC Input Strapping)

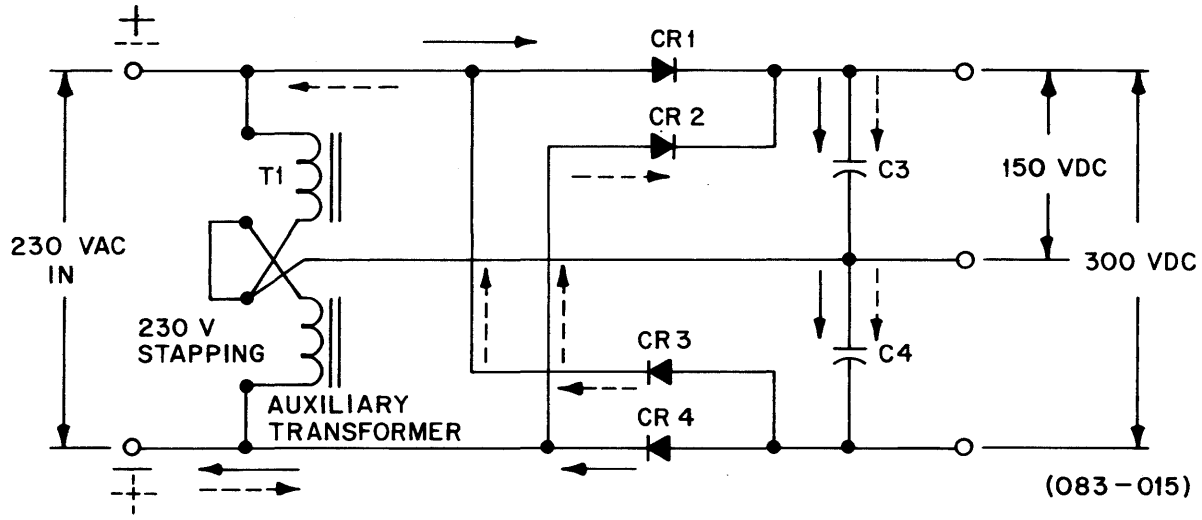


Figure 2-35. Simplified Input Rectifier/Filter/Doubler Section
(230 VAC Input Strapping)

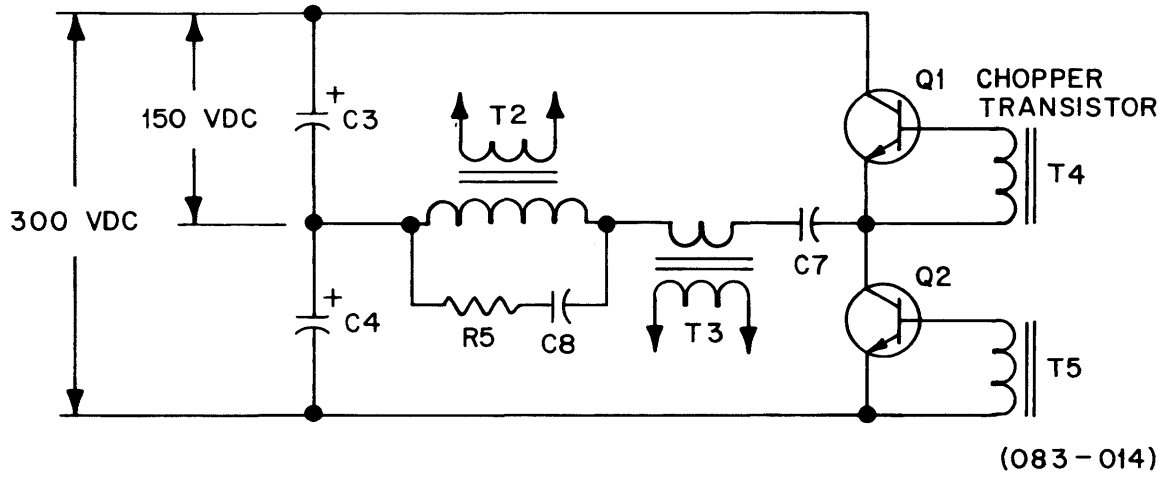


Figure 2-36. Simplified Transistor Chopper (Half-Wave)

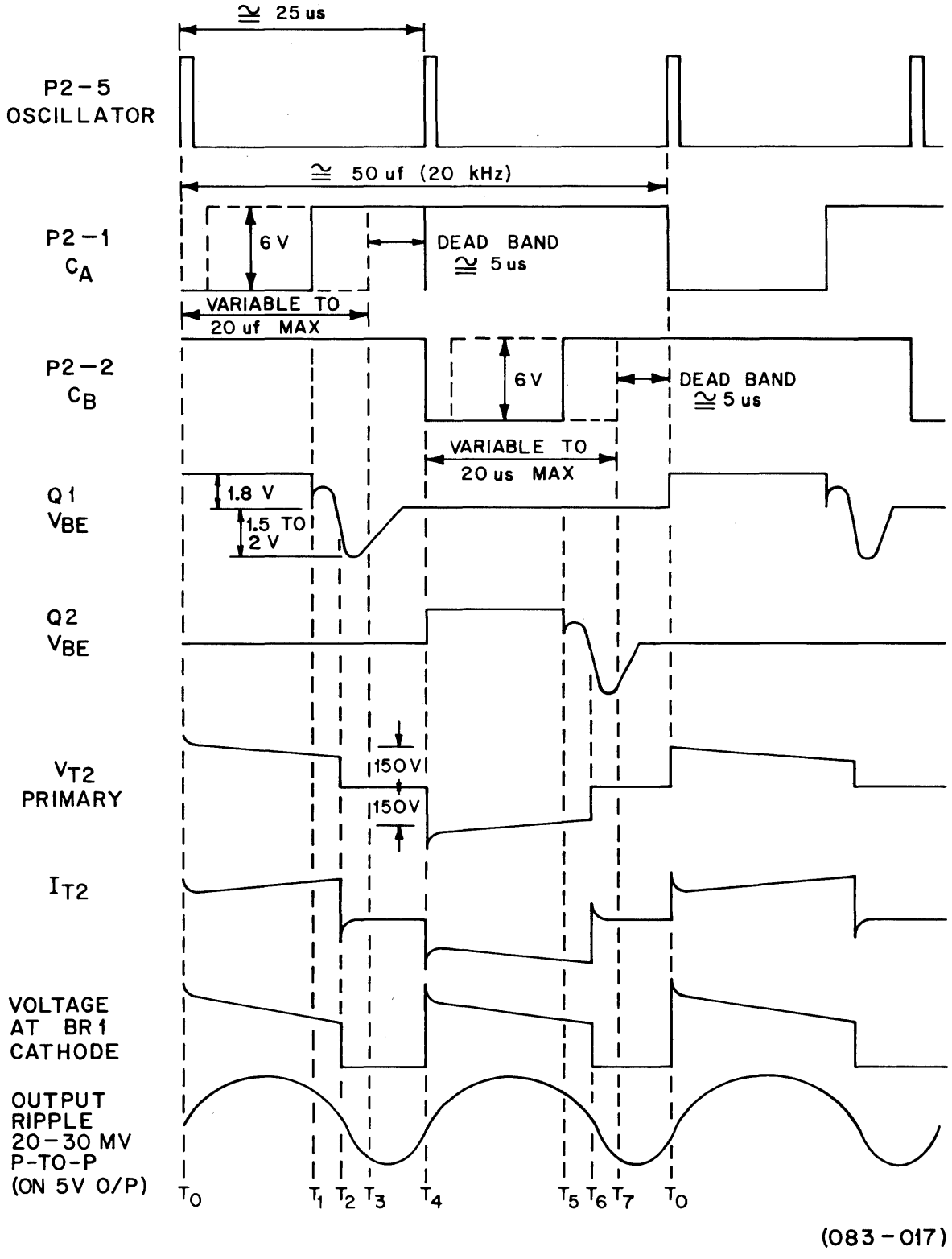


Figure 2-37. Power Supply Waveforms

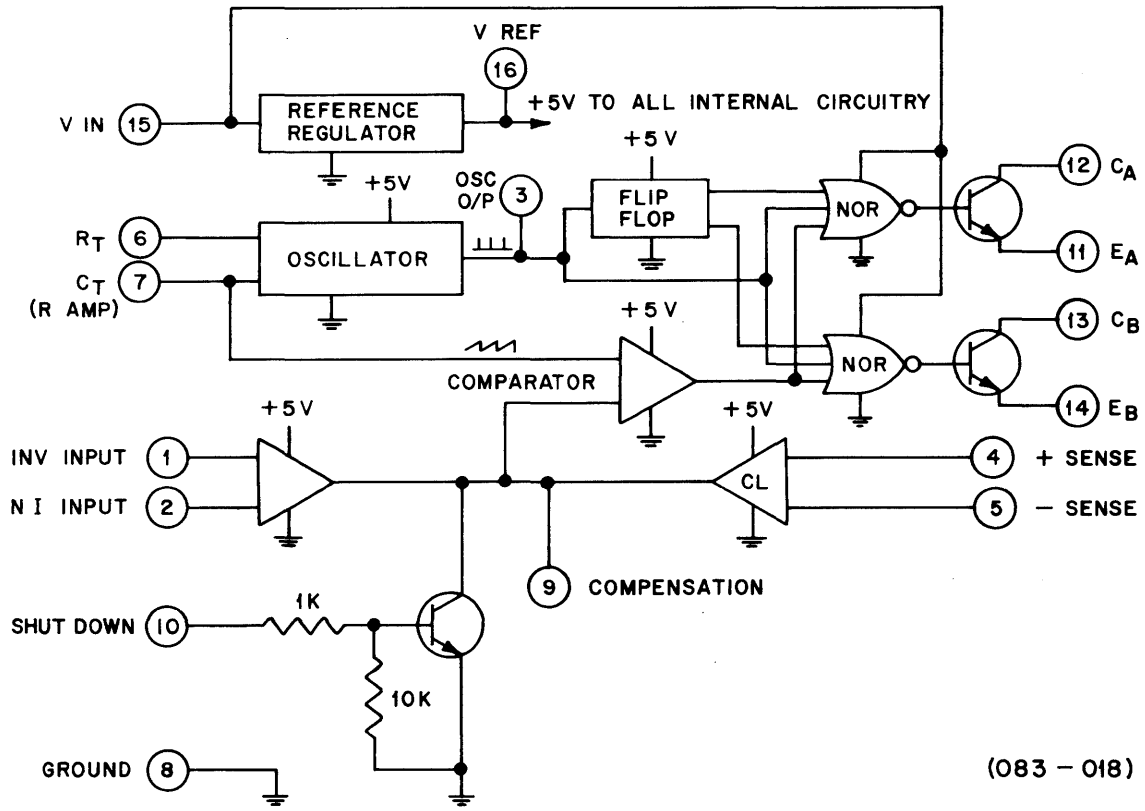


Figure 2-38. Control Module Block Diagram

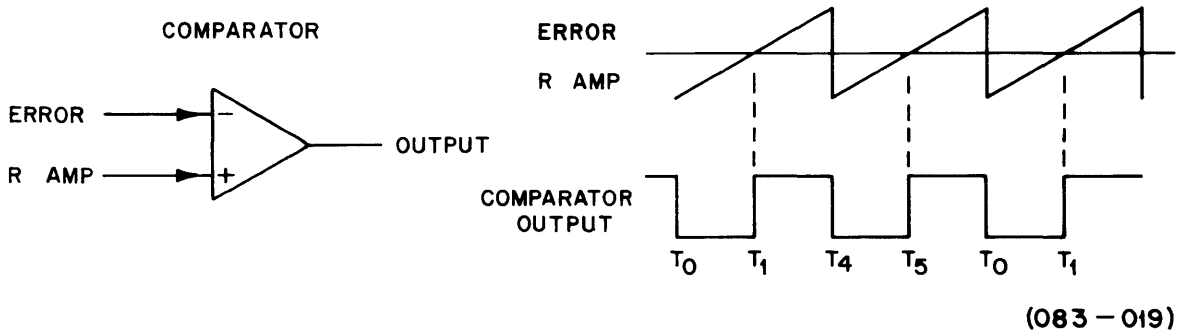


Figure 2-39. Control Module Timing Diagram (SG3524)

2.9.1.4 Internal Auxiliary Power Supply

Transformer T1 transforms the 115 or 230VAC line voltage to supply unregulated +24VDC to the control circuit. CR13, CR14, CR15, and CR16 form a full bridge rectifier and C10 filters the output.

2.9.1.5 Control Circuitry

The control module assembly contains a pulse-width-modulator, IC SG3524, (See Figures 2-38 and 2-39) and provides all the basic control functions as follows:

1. Voltage Amplifier and Reference
2. Overvoltage Protection
3. Undervoltage Protection
4. Soft Start
5. Remote On/Off
6. Power Fail
7. Current Limit

The adjustments on the control module assembly are factory set, and it should not normally be necessary to readjust the factory settings.

Table 2-2 defines the voltage/current levels at nominal line and load conditions.

Table 2-2. Voltage/Current Levels

Pin	Function	Measurement	Pin	Function	Measurement
P1-1	OVP	2.3V	P2-1	C_A	See Fig 2-37
P1-2	Current Limit	Square Wave, 1.4V Peak	P2-1	C_B	See Fig 2-37
			P3-3	Power Fail	3.5-5VDC
P1-3	Current Limit	.5-.6VDC	P2-4	-Sense	0
P1-4	Remote On/Off	1-4VDC	P2-5	OSC out	See Fig 2-37
P1-5	UVS	12-18VDC	P2-6	+Sense Divider	2.2-2.8VDC
P1-6	+24V Input	22-25VDC	P2-7	R_T	
P1-7	Current Lim Bias	.5-.7VDC	P2-8	Common	0

Note: All measurements are made with respect to pins P2-4 or P2-8.

2.9.1.6 Chopper Drivers

Drive to the bridge transistors Q1 and Q2 is provided by two pair of push-pull current source drivers Q3, Q4, Q5 and Q6. Q4 and Q5 bases are held at a 5.1V level. Q3 and Q6 are alternately turned on by C_A and C_B . C_A and C_B levels are clamped at 5.7V by CR19 and CR20 (see Figure 2-37). Transformers T4 and T5 couple drive signals to the base of Q1 and Q4. The snubbers consists of R11, C11, R16 and C13. Resistors R12 and R17 control the drive current.

2.9.1.7 The +5V Main Output Crowbar

Components CR34, R29, R28 and SCR1 form an overvoltage crowbar circuit. If the +5V regulated output goes above 6.3V, the SCR1 fires and keeps the output low. The power supply must be turned off to re-start after the overvoltage condition has been removed.

2.9.1.8 Secondary Current Limiting Circuitry

Transformer T6, R27, CR22 through CR25 are part of the secondary current limit circuit.

2.9.1.9 The ± 15V Unregulated Outputs

The +15V and the -15V unregulated circuits are identical. Only the +15V unregulated circuit will be described. The quasisquare voltage waveform is transformed down by T2, rectified by BR2 and filtered by L3 and C20. C21 is an RFI suppression capacitor. R31 and C29 form an RC snubber to suppress overshoot. T7, R30, CR26 through CR29 are part of the +15V current limit circuit.

2.9.1.10 The ± 15V Overvoltage Limit

The +15V and the -15V overvoltage limit circuits are identical. Only the +15V circuit will be described. Components R36, CR35, CR36 and R37 are a biasing network to turn on Q7, when the output voltage is greater than 17 volts. The circuit limits the no load output voltage to 17 volts.

2.9.1.11 The +48V Unregulated Output

The primary of transformer T9 is paralleled with the primary of transformer T2. The quasisquare voltage waveform is transformed down by T9, rectified by BR4 and filtered by L5 and C27. R34 preloads the output to help limit the no load voltage. The +48 volt output does not have current limit.

2.10 KEYBOARD (CORTRON UP/DOWN STROKE), SCHEMATIC NO. 400094-01

2.10.1 Keyswitch Description

The keyswitch used on the keyboard is a linear saturable ferrite core with two preformed wires snapped through it. One wire, called the drive wire, is periodically driven by a current pulse. The response to the drive pulse appears, through transformer action, on the second wire called the sense wire. This core module assembly is snapped into the switch housing together with the plunger and return spring. Into the plunger are molded a pair of magnets. In the undepressed position the magnets are saturating the core. Since the core is saturated, signals which are present on the drive wire are not coupled to the sense wire. As the plunger is depressed, the magnets clear the core, bringing it out of saturation and allowing the drive signals to be coupled to the sense wire. These sense signals are translated into digital pulses.

2.10.2 Circuit Description

2.10.2.1 Microprocessor

The 128 key non-programmable MOS/LSI microprocessor integrated circuit with external electronics is used for sequential interrogation. This microprocessor can be logically divided into the following sections:

a) timing section
b) count register section
c) data section
d) strobe section

2.10.2.1.1 Timing Section. The timing section generates a main clock signal train which drives the scanning counter and generates clock signals $\Phi 1$, $\Phi 2$, & $\Phi 3$, ($\Phi 2$ is used internally only). The scanning counter provides the address for each key and its position code. The position code is the address of the keyswitch latched into the output data latch. $\Phi 1$ is used as the interrogation enable signal. $\Phi 2$ generates the strobe and loads the data into the data latch. The strobe is updated one time per depression of a keyswitch. $\Phi 3$ is used in the external electronics. The input to the timing section (TPC) is a pulse train of 10μs square waves.

2.10.2.1.2 Count Register Section. The count register section consists of one binary counter seven bits in length. The first four bits are used to scan in the "X" direction and the last three bits are used to scan in the "Y" direction. This counter provides 128 unique position codes, each of which corresponds to a unique location of the key in the matrix.

2.10.2.1.3 Data Section. The output data consists of a seven bit data latch and a shift register. Each of the seven bits of the counter is latched into the data latch with Φ2, when the key is depressed, and with Φ1 CLK, when the key is released. A 128-bit shift register is used to provide past key history to the data latch, to the strobe section, and to the external amplifier for hysteresis.

2.10.2.1.4 Strobe Section. All keys that are detected will enter into the N-key rollover scheme. During Φ2, the input shift register is "anded" with the inverted output of the shift register to detect a down stroke of the keyswitch which is presently being interrogated, and the strobe is generated.

2.10.3 External Electronics

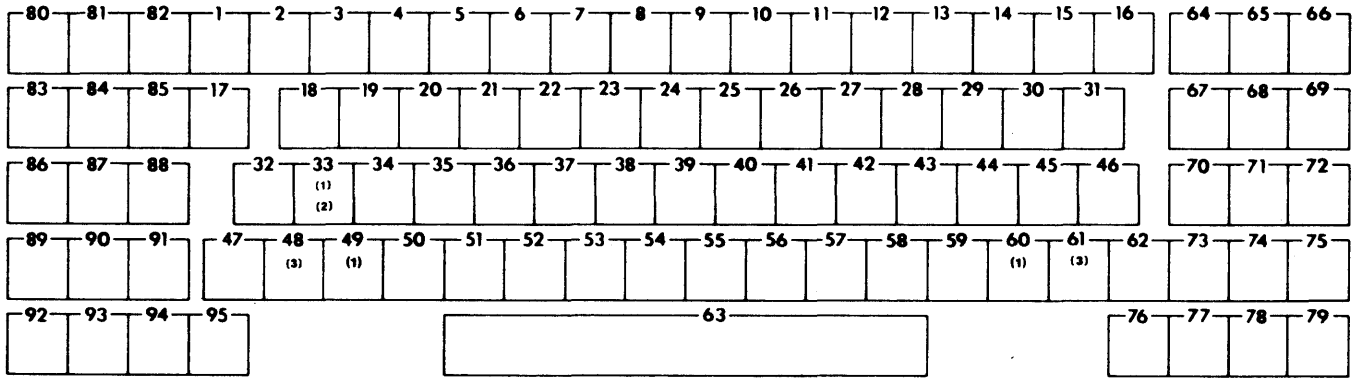
2.10.3.1 Keyswitch Array

Each keyswitch is assigned to a particular location in the matrix (see organization chart, dwg. no. 400099-01, sht. 2). The first four lines (A1 - A4) of the microprocessor are gated with Φ1, to scan in the "X" direction, and the last three lines (A5 - A7) are used to scan in the "Y" direction. If the keyswitch is depressed, a signal appears on the sense line, which is amplified and latched into the keyswitch latch. The detected signal in the keyswitch latch is called "Shift Register In" (SRIN) and represents a depressed keyswitch in the matrix location.

2.10.3.2 Output Code

The microprocessor will generate a binary code to identify the key station location in the given matrix when the key is depressed, and a modified key code when the key is released. This modified key code consists of regeneration of bits DØ through D6, and the inversion of bit D7.

This 8-bit code is a position code assigned to the physical location of a particular key on the keyboard. Figure 2-40 shows the key positions and Table 2-3 gives the position codes generated by each key position. These position codes are sent to the terminal microprocessor as part of a memory address and in turn converted to the corresponding ASCII code stored in ROM. (See Table 4-2 for the ASCII Code Chart).



NOTES:

(1) KEYS 33, 49 & 60 SHARE THE SAME POSITION CODE.

(2) KEY 33 IS A MECHANICAL SHIFT LOCK KEY.

(3) KEY POSITION 48 & 61 ARE PERMANENTLY IN THE DOWN POSITION.

083-053

Figure 2-40. Key Position Layout

Table 2-3. Cortron Key Position Numbers and Position Codes

Key Pos. No.	Position Codes		Key Pos. No.	Position Codes		Key Pos. No.	Position Codes	
	Down Stroke	Up Stroke		Down Stroke	Up Stroke		Down Stroke	Up Stroke
1	05	85	33	3F	BF	65	72	F2
2	06	86	34	3A	BA	66	73	F3
3	3D	BD	35	10	90	67	61	E1
4	3E	BE	36	12	92	68	62	E2
5	15	95	37	20	A0	69	63	E3
6	16	96	38	22	A2	70	51	D1
7	25	A5	39	30	B0	71	52	D2
8	26	A6	40	32	B2	72	53	D3
9	35	B5	41	28	A8	73	41	C1
10	36	B6	42	2A	AA	74	42	C2
11	2D	AD	43	18	98	75	43	C3
12	2E	AE	44	1A	9A	76	78	F8
13	1D	9D	45	08	88	77	79	F9
14	1E	9E	46	0A	8A	78	7A	FA
15	0D	8D	47	07	87	79	7B	FB
16	0E	8E	48	76	F6	80	77	F7
17	03	83	49	3F	BF	81	74	F4
18	3C	BC	50	39	B9	82	75	F5
19	3B	BB	51	17	97	83	67	E7
20	14	94	52	11	91	84	64	E4
21	13	93	53	27	A7	85	65	E5
22	24	A4	54	21	A1	86	57	D7
23	23	A3	55	37	B7	87	54	D4
24	34	B4	56	31	B1	88	55	D5
25	33	B3	57	2F	AF	89	47	C7
26	2C	AC	58	29	A9	90	44	C4
27	2B	AB	59	1F	9F	91	45	C5
28	1C	9C	60	3F	BF	92	7F	FF
29	1B	9B	61	09	89	93	7C	FC
30	0C	8C	62	0F	8F	94	7D	FD
31	0B	8B	63	19	99	95	7E	FE
32	38	B8	64	71	F1			

NOTES: 1. All codes are in hexadecimal form. Bit Ø is the LSB.

2. Only Down-stroke position codes are used for keyboard diagnostics.

The downstroke position code generated when the key is depressed uses the D7 bit to flag the terminal microprocessor to repeat the corresponding function or character after a delay of 1/2 second (counted by the Real-Time Clock). The upstroke position code, generated when the key is released, inverts the D7 bit of the downstroke position code which in turn causes the terminal microprocessor to remove the repeat flag for the corresponding function or character.

There are two diagnostic positions installed on the keyboard to generate only the downstroke position codes. All keyboard memories are erased when -POR is low. When -POR goes high, the diagnostic codes and the codes of any depressed keys will appear at the interface. The sequence in which these codes appear depends upon the location of the key in the matrix, and on the time of removal of -POR.

2.10.3.3 Output Strobe Logic

A strobe signal -KYSTB is generated each time a key is depressed or released. (This signal is generated by the microprocessor, gated with Φ1.) The +BUSY signal goes high after the terminal microprocessor receives the strobe signal. The strobe will go high after +BUSY returns low. As long as -KYSTB and +BUSY are both high, the scan cycle stops, and any new key depressions will be ignored.

2.11 KEYBOARD (MICRO SWITCH UP/DOWN STROKE), Schematic No. 400286-01

2.11.1 General Description

The keyboard contains an LSI Scan Encoder that is capable of encoding up to 127 keys by sequentially interrogating each key, and generating a specific code and data ready signal for each key that is operated.

2.11.2 Internal Logic Description

2.11.2.1 Keyswitch Matrix

The 127 possible keys of the keyboard are arranged in a matrix consisting of 16 row drive outputs and 8 column sense inputs. An operated key will produce a "Key Active" signal when a corresponding matrix intersection is sensed. The signals used to interrogate the key matrix are also used to address an internal ROM which is programmed with a specific code for each key.

2.11.2.2 N-Key Rollover Mode

The basic operation of the keyboard is N-Key Rollover mode. This is implemented by storing the state of each key in the prior scan in a 128-bit shift register. By comparing the input and output of the shift register, key actuation and release can be detected for each key regardless of the state of any other key. Thus, by responding to an actuated key on the down-stroke transition, a new code and strobe will be generated for every new key depression, regardless of how many keys are already depressed.

2.11.2.3 Strobe Output

Whenever new data is loaded into the output storage latches a Strobe or "data ready" signal is generated. Only one Strobe signal can be generated per scan cycle. The presence and duration of the Strobe signal is determined by the Strobe Reset input signal.

2.11.2.4 Strobe Reset

The Strobe signal is enabled only when the Strobe Reset input is in the high (not reset) state. It is cleared by the Strobe Reset signal going low (reset). The associated data will remain stable until the Strobe Reset signal returns to the high state. The Strobe Reset signal must never go low except in response to a high Strobe signal.

2.11.2.5 FIFO Buffer Operation

A two level FIFO (first-in first-out) buffer is also provided on the keyboard. Two sets of latches are loaded alternately to the output drivers in response to the Strobe Reset signal. If new data is generated when both buffers are still waiting for system response (Overrun Condition) the output drivers are forced to an all low state. A new Strobe signal is generated if not already present. When the external electronics acknowledges this Strobe signal, an internal System Reset signal is produced. Thus, any previous data will no longer be accessible, but keys found depressed at the end of the reset sequence will be treated as new key depressions.

2.11.2.6 System Reset

A System Reset signal will be required to reset all counters and logic to an initial state necessary for subsequent correct operation. After the system reset signal is removed the encoder completes the reset operation in a time lasting between one and two scan cycles. During this time, and the reset time, all key inputs are ignored. Any keys found depressed after this time are treated as new key depressions, even if they were depressed prior to system reset.

2.11.3 External Electronics

2.11.3.1 Output Codes

The Scan Encoder will generate an 8-bit binary code to identify the key station location in the given matrix when the key is depressed, and a modified key code when the key is released. This modified key code consists of regeneration of bits DØ through D6, and the inversion of bit D7. This 8-bit code is a position code assigned to the physical location of a particular key on the keyboard. Figure 2-40 shows the key positions and Table 2-3 gives the position codes generated by each key position. These position codes are inverted and sent to the terminal microprocessor as part of a memory address and, in turn, are converted to the corresponding ASCII code stored in ROM. (See Table 4-2 for the ASCII Code Chart.)

Table 2-4 Micro Switch Key Position Numbers and Position Codes.

Y	X	KEY NO.	DOWNSTROKE 76543210	UPSTROKE 76543210	Y	X	KEY NO.	DOWNSTROKE 76543210	UPSTROKE 76543210	Y	X	KEY NO.	DOWNSTROKE 76543210	UPSTROKE 76543210
4	2	80	01110111	11110111	2	5	22	00100100	10100100	6	13	70	01010001	11010001
0	2	81	01110100	11110100	2	6	23	00100011	10100011	6	14	71	01010010	11010010
0	3	82	01110101	11110101	2	7	24	00110100	10110100	6	15	72	01010011	11010011
1	0	1	00000101	10000101	2	8	25	00110011	10110011	7	0	89	01000111	11000111
1	1	2	00000110	10000110	2	9	26	00101100	10101100	7	1	90	01000100	11000100
1	2	3	00111101	10111101	2	10	27	00101011	10101011	7	2	91	01000101	11000101
1	3	4	00111110	10111110	2	11	28	00011100	10011100	3	1	49	00111111	10111111
1	4	5	00010101	10010101	2	12	27	00011011	10011011	4	3	50	00111001	10111001
1	5	6	00010110	10010110	2	13	30	00001100	10001100	4	4	51	00010111	10010111
1	6	7	00100101	10100101	2	14	31	00001011	10001011	4	5	52	00010001	10010001
1	7	8	00100110	10100110	5	13	67	01100001	11100001	4	6	53	00100111	10100111
1	8	9	00110101	10110101	5	14	68	01100010	11100010	4	7	54	00100001	10100001
1	9	10	00110110	10110110	5	15	69	01100011	11100011	4	8	55	00110111	10110111
1	10	11	00101101	10101101	6	0	86	01010111	11010111	4	9	56	00110001	10110001
1	11	12	00101110	10101110	6	1	87	01010100	11010100	4	10	57	00101111	10101111
1	12	13	00011101	10011101	6	2	88	01010101	11010101	4	11	58	00101001	10101001
1	13	14	00011110	10011110	3	0	32	00111000	10111000	4	12	59	00011111	10011111
1	14	15	00001101	10001101	3	1	33	00111111	10111111	3	1	60	00111111	10111111
1	15	16	00001110	10001110	3	2	34	00111010	10111010	4	15	62	00001111	10001111
0	13	64	01110001	11110001	3	3	35	00010000	10010000	7	13	73	01000001	11000001
0	14	65	01110010	11110010	3	4	36	00010010	10010010	7	14	74	01000010	11000010
0	15	66	01110011	11110011	3	5	37	00100000	10100000	7	15	75	01000011	11000011
5	0	83	01100111	11100111	3	6	38	00100010	10100010	0	4	92	01111111	11111111
5	1	84	01100100	11100100	3	7	39	00110000	10110000	0	5	93	01111100	11111100
5	2	85	01100101	11100101	3	8	40	00110010	10110010	0	6	94	01111101	11111101
2	0	17	00000011	10000011	3	9	41	00101000	10101000	0	7	95	01111110	11111110
2	1	18	00111100	10111100	3	10	42	00101010	10101010	0	8	63	00011001	10011001
2	2	19	00111011	10111011	3	11	43	00011000	10011000	0	10	77	01111001	11111001
2	3	20	00010100	10010100	3	12	44	00011010	10011010	0	11	78	01111010	11111010
2	4	21	00010011	10010011	3	14	46	00001010	10001010	0	12	79	01111011	11111011

The downstroke position code generated when the key is depressed uses the D7 bit to flag the terminal micrprocessor to repeat the corresponding function or character after a 1/2 second delay (counted by the Real Time Clock). The upstroke position code generated when a key is released, inverts the D7 bit of the downstroke position code which in turn causes the terminal microprocessor to remove the repeat flag for the corresponding function or character.

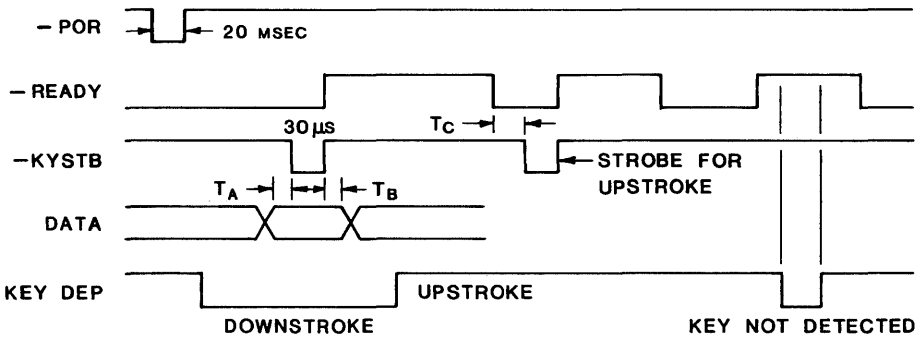
There are two key positions on the keyboard which are strapped to produce only the downstroke position code for keyboard diagnostics. These position codes are present at the interface after a power-up or system reset sequence.

2.11.3.2 Output Strobe Logic

The strobe output signal -KYSTB is generated each time a key is depressed and released. A low (active) state on the -KYSTB output informs the terminal microprocessor that data is available at the keyboard. In response, the terminal microprocessor sends a high (active) +BUSY input signal to the keyboard. The -KYSTB strobe will go high after the +BUSY input signal returns to a low (inactive) state. As long as -KYSTB and +BUSY are both high, the scan cycle stops, and any new key depressions are ignored. (See Figure 2-41)

2.11.3.3 Power-on Reset

The terminal microprocessor will provide a low -POR input signal to the keyboard when power is applied to the terminal. The low (active) state of the -POR input signal produces a System Reset signal for the encoder. When the -POR input signal returns to its normally high (inactive) state, the position codes of the two diagnostic keys and any other keys that are depressed will appear at the interface. The sequence in which these codes arrive at the interface depends upon the location of the keys in the matrix at the time when the -POR signal became high (inactive). (See Figure 2-41.)



T_A = 5µs MINIMUM: DATA BITS STABLE BEFORE STROBE IS ACTIVE.

T_B = 5µs MINIMUM: DATA BITS STABLE AFTER STROBE GOES HIGH.

T_C = 10 µs MINIMUM: READY ACTIVE LOW UNTIL NEW STROBE IS SENT.

NOTE: DATA IS TAKEN DURING 'T_B'.

083-049

Figure 2-41. Keyboard Timing Diagram

2.12 CONTROL PANEL, PART NO. 400056-01

The Control Panel (Port 3), uses the 8255 I/O interface used by other I/O ports. Refer to Figure 2-42 and Schematic Diagram No. 400056-01. The 8255 IC has a data bus buffer, three registers that can be programmed for either input or output, a control word register, and power and control signal connections. See Table 2-4. The Control Panel is located at the right side of the terminal with the indicator lamps visible just above the keyboard and the switches concealed just inside the printer under the access cover. The indicator lamps are LED (Light Emitting Diode) type.

Table 2-4. I/O Interface Connections

8255 Signals	Functions
DØ - D7 (pins 27-34)	Bidirectional data bus — all data and command words are transferred between the MPU and the control panel over these eight lines.
CS (pin 6)	Chip Select — Port 3, the control panel, is selected when this line goes low.
A1/AØ (pins 8/9)	ADDR 1/ADDR Ø — two low-order address lines of the memory address bus, used to select 8255 registers or to specify that a control word is to be transmitted from the MPU over the data bus. A1 AØ 0 0 Register A 0 1 Register B 1 0 Register C 1 1 Control Word (on Data Bus)
WR (pin 36)	WRITE — when low, specifies that a Write from the MPU to the control panel via the data bus is taking place — output from the MPU.
RD (pin 5)	READ — when low, specifies that a Read into the MPU from the control panel via the data bus is taking place — input to the MPU from the control panel.
RST (pin 35)	RESET — when high, clears all internal registers, including the control register, and sets A, B, and C to input mode. RST is driven high only at power-up.
Vcc (pin 26)	+5 volts.
GND (pin 7)	Ground.

NOTE

The RESET keyswitch located on the control section of the keyboard is used to clear (turn off) the error indicators, via the system firmware: it does not reset the 8255.

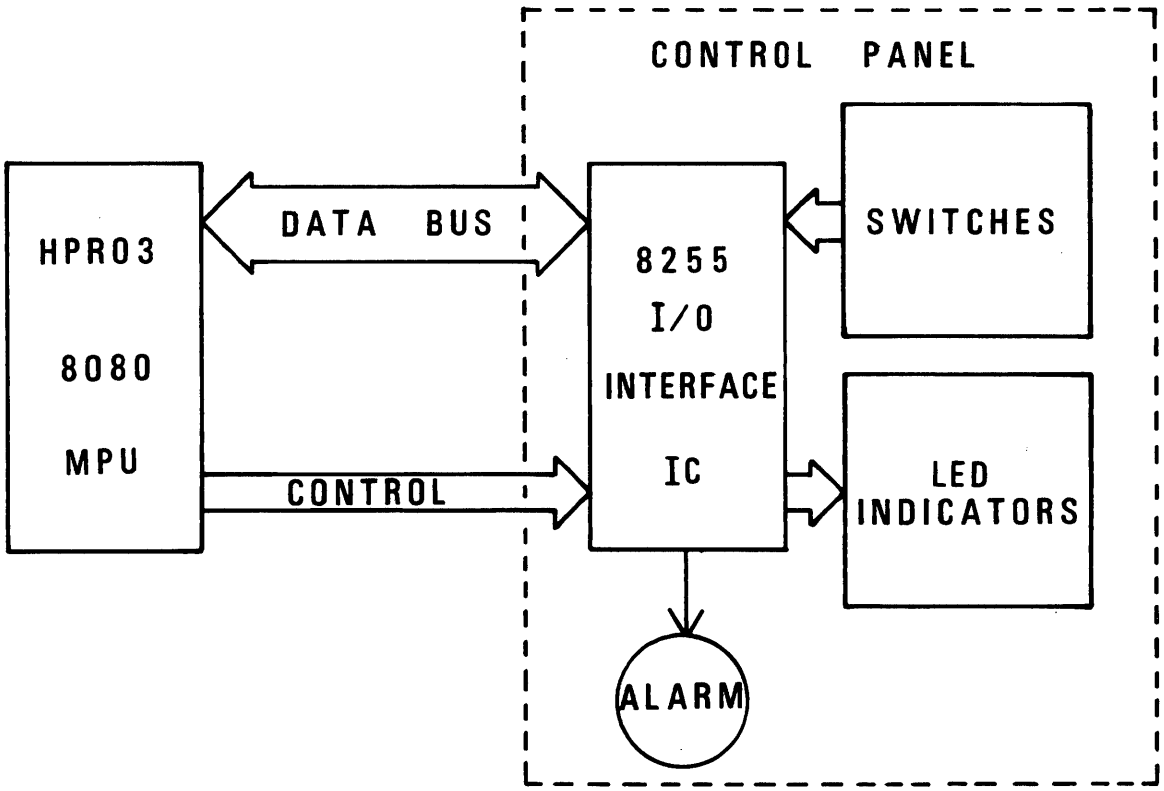


Figure 2-42. Block Diagram, Control Panel

2.12.1 Operating Mode

The 8255 IC is capable of operating in one of three modes, selected by system firmware. Only Mode 0, pure input/output, which is used by the control panel, will be described here. The three eight-bit registers of the 8255 IC are designated as A, B, and C. As part of its power-up initialization program, the firmware defines the A register (PAØ --PA7) and the four low-order bits of the C register (PCØ — PC3) as inputs, and the B register (PBØ — PB7) and the four high-order bits of the C register (PC4 — PC7) as outputs. All inputs are connected to switches. All outputs are used to control LEDs and the audible alarm.

2.12.2 Switches

Switches are all single-pole, double-throw. All switches have their moving contact grounded. With switches open, as shown in the schematic, all input lines are held high by pull-up resistors. When a switch is closed manually, the affected line goes low.

2.12.3 Reading Registers

The control panel operates under control of the MPU and the system firmware. The firmware periodically initiates a READ by driving CS and RD low, causing the contents of either the A register or the C register to be input to the MPU over the data bus lines. Firmware masks out the meaningless four high-order bits of the C register. The firmware examines each bit to determine whether it is high or low. If a bit is found to be low, the associated switch has been actuated; if the bit is high the switch is in the OFF position. Refer to the Control Panel Identification Chart in the Schematics/Reference section for functional identification of all switches and indicators.

2.12.4 Indicators and Audible Alarm

System firmware controls the LED indicators (except for the POWER ON indicator) and the audible alarm. The POWER ON indicator is hard-wired to +5 volts and lights when the POWER switch is turned on. When the firmware in the MPU detects an error condition or a change in state requiring the lighting of an LED or sounding the buzzer, the MPU initiates a WRITE (output to the control panel) by driving CS and WR low, then sending the appropriate data over the data bus. When the RESET keyswitch on the keyboard is pressed, the firmware clears (turns off) any error-indicating LEDs. All LEDs are red, except CR12, which is green.

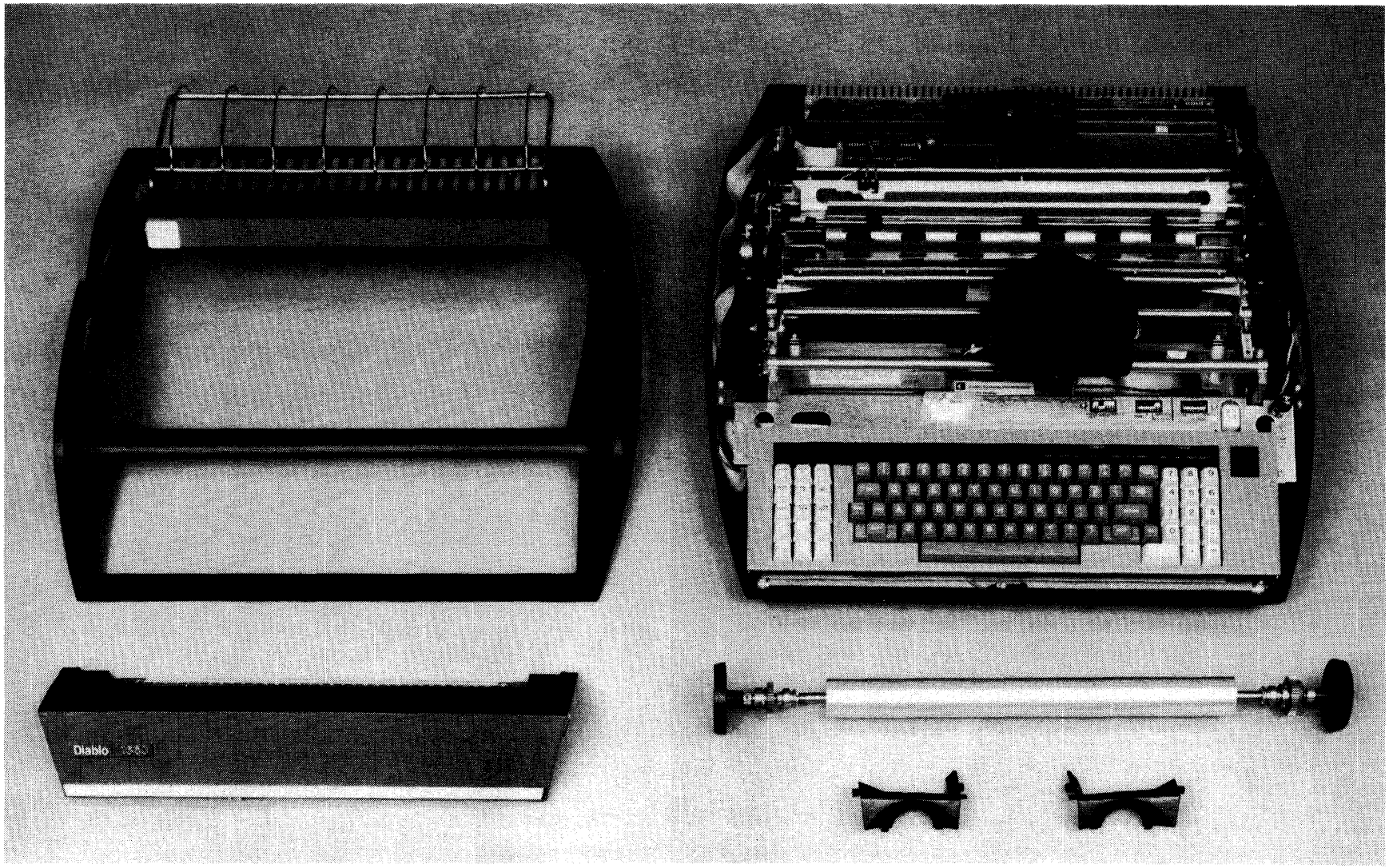


Figure 3-0. HyTerm with top cover removed

Section 3

MAINTENANCE

3.1 INTRODUCTION

Maintenance of the terminal is generally divided into two broad categories: module replacement and adjustments, and detailed troubleshooting and repair of the circuit boards. Since some troubleshooting is also involved in locating the faulty module before it can be replaced, there is no clear-cut dividing line between these categories, and overlap will occur in many areas.

This section is generally divided so that those performing module replacement will use the next three sub-headings, (3.2) PREVENTIVE MAINTENANCE, (3.3) MODULE REPLACEMENT, and (3.4) ADJUSTMENTS. The remainder of this section contains component location/identification information that will be useful in troubleshooting.

NOTE

Preventive Maintenance, when performed according to the procedures listed here, will not affect the Diablo warranty. However, any module replacement or adjustment unsuccessfully attempted that results in damage to the equipment will render the warranty null and void. All time and material required to restore the terminal to working order will be billed at the prevailing rates.

3.1.1 General Rules

There are a few general rules that should always be observed:

(1) Never remove or install any circuit boards, or connect or disconnect any plugs, while power is on.

(2) Applying power to the terminal initiates a printer Restore sequence, which includes carriage movement. Make sure the carriage is free to move to the left before applying power.

(3) Whenever the access cover is removed, be careful not to brush against the cover-open switch: operating this switch could allow the carriage to move suddenly, which could cause an injury. When operating the terminal with the access cover removed (and the cover-open switch in the "override" position), keep fingers, hair, etc., away from the printer.

(4) Never remove the top cover without first disconnecting the power cord from the wall outlet.

(5) The print head does not need cleaning under normal operating conditions. Only unusually severe operating conditions will make print head cleaning necessary, in which case the problem should be referred to your Diablo Service Represenative.

(6) Do not use alcohol to clean the paper feed rollers, or any other rubber parts. Alcohol dries out the rubber and hardens it, eventually resulting in paper feed problems. Use "Fedron Platen Cleaner" or its equivalent.

WARNING

Fedron Platen Cleaner and similar products are flammable, and have a very low flash point.

(7) Take care not to touch plastic parts with platen cleaner. These products are usually harmful to plastics. Use alcohol to clean plastic parts.

(8) When tipping the HyTerm up to gain access to its underside, first position the power cord and EIA cable to the sides so they will not be in the way. Make sure the surface behind the HyTerm is flat and free of any foreign objects. Then tip the HyTerm up approximately 70° so that it balances on the rear edge of its bottom cover. Do not allow the table surface or any objects to apply pressure to the finned heat sinks on the rear; since these heat sinks are mounted on the power amplifier boards, any pressure could damage these circuit boards or the mother board and its connectors. Also, while the HyTerm is tilted up in this manner, hold onto it with one hand to prevent it from falling.

3.1.2 Top Cover Removal/Replacement

Removal of the top cover and its accessories is a prerequisite to most HyTerm maintenance procedures.

REMOVAL

Refer to Figure 3-0.

(1) Turn the power off and unplug the cord from the ac outlet.

(2) Remove the top cover accessories: the access cover and the plastic platen skirts over the ends of the platen shaft (see Figure 3-0).

(3) Remove the platen: grasp the platen knobs in both hands, press down on the platen latches with your thumbs, and lift the platen straight up.

(4) Release the top cover by pulling forward on the two latches inside the cover at both sides, just in front of the platen. Lift the top cover straight up and free from the printer.

REPLACEMENT

(1) Remove the platen from the printer.

(2) Install the top cover and accessories by reversing the Removal procedure above.

3.1.3 Tools

A basic hand tool assortment, including regular and Phillips screwdrivers, small open-end wrenches, pliers, and Allen setscrew wrenches is needed for any maintenance. Tools such as screw starters, offset screwdrivers, etc., are not essential, but will make some jobs much easier. In addition, the following tools are needed for driving and removing the special screws used in the terminal and for performing printer adjustments.

	Description	Diablo Part No.
(1)	T15 TORX^{R} Screwdriver	70826-03
	or T15 Driver Bit	70826-01
(2)	T15 TORX Key Wrench	70826-05
(3)	Circuit Board Extender	40539-01
(4)	3M Connector Extractor Tool	70832
(5)	Molex Connector Extractor Tool	24853
(6)	Molex Connector Pin Extractor Tool	13197
(7)	Platen Adjustment Tool	24708
(8)	Tensiometer, Electromatic Equipment Co. Model DXX-1KD or equivalent, calibrated for Diablo cable.	

For detailed troubleshooting and repair of circuit boards, the usual oscilloscope, soldering iron, etc., are needed, plus the following special tools:

	Description	Diablo Part No.
(1)	Transducer Cable Extender	40666
(2)	Carriage Motor Cable Extender	40667
(3)	48V Return Cable Extender	24789

3.2 PREVENTIVE MAINTENANCE

3.2.1 Supplies

The following supplies and lubricants are necessary for proper preventive maintenance. The part numbers listed below are Diablo part numbers.

1. Fedron Platen Cleaner, or equivalent.
2. No. 99000-01 Alcohol Pads (91% Isopropyl alcohol), or equivalent.
3. Lint-free Wipes.
4. Clean, low pressure compressed air.
5. No. 70825-01 2-oz tube of Multipurpose grease.
6. No. 70364 Polyoil (light white grease).
7. No 70243 Light Oil (Shell Turbo 27).
8. Loctite

CAUTIONS:

* Do not use alcohol on any rubber parts.
* Do not use platen cleaners on plastic parts.
* Platen cleaners are flammable, and have a very low flash point.

TORX^{R} is a registered trademark of Camcar Screw & Mfg.

3.2.2 Cleaning and Inspection

It is difficult to state specific rules concerning the frequency of preventive maintenance inspections, because of differences in the hours of usage and environmental considerations from one machine to another. It is recommended, therefore, that the following preventive maintenance procedure be performed at least every 500 hours of printing time, or every six months, whichever occurs first:

(1) Remove power from the terminal. Remove the top cover (see 3.1.2). Reinstall the platen once the top cover has been removed from the HyTerm.

(2) Thoroughly inspect the printer for signs of wear and loose or broken hardware. Check carriage cable for signs of wear, and cable pulleys for loose bearings. Check platen for looseness or wobble. Check platen drive gears for looseness. Check the carriage for looseness, wobble, or accumulation of foreign material on the rails, which might cause uneven movement of the carriage.

(3) Remove the platen and the paper cradle and inspect them and the plastic paper clamp for signs of wear.

(4) Clean the printer thoroughly, using alcohol-saturated cleaning pads and wipes. Remove accumulations of paper residue, ink, dust, etc., with special attention to carriage rails and pulley grooves.

(5) Clean the paper bail tires and paper feed rollers with a good platen cleaner which is non-injurious to rubber products, such as "Fedron" Platen Cleaner. Do not use alcohol to clean these items.

*(6) Clean the rest of the terminal as required -- remove all dust and foreign material.

*(7) Inspect the entire machine for loose hardware and frayed wires or cables.

*(8) Check to be certain that the fan is operating.

*(9) Check all power supply voltages (see 3.4.3).

Items above marked with an asterisk (*) should be checked on every machine visit, not only at the P.M. inspection.

3.2.3 Lubrication

Lubricate the various parts of the cleaned and inspected printer according to the following schedule. DO NOT exceed this schedule. Too much lubricant is often worse than none at all! (To be done every six months or if printer has not been used for more than a week.)

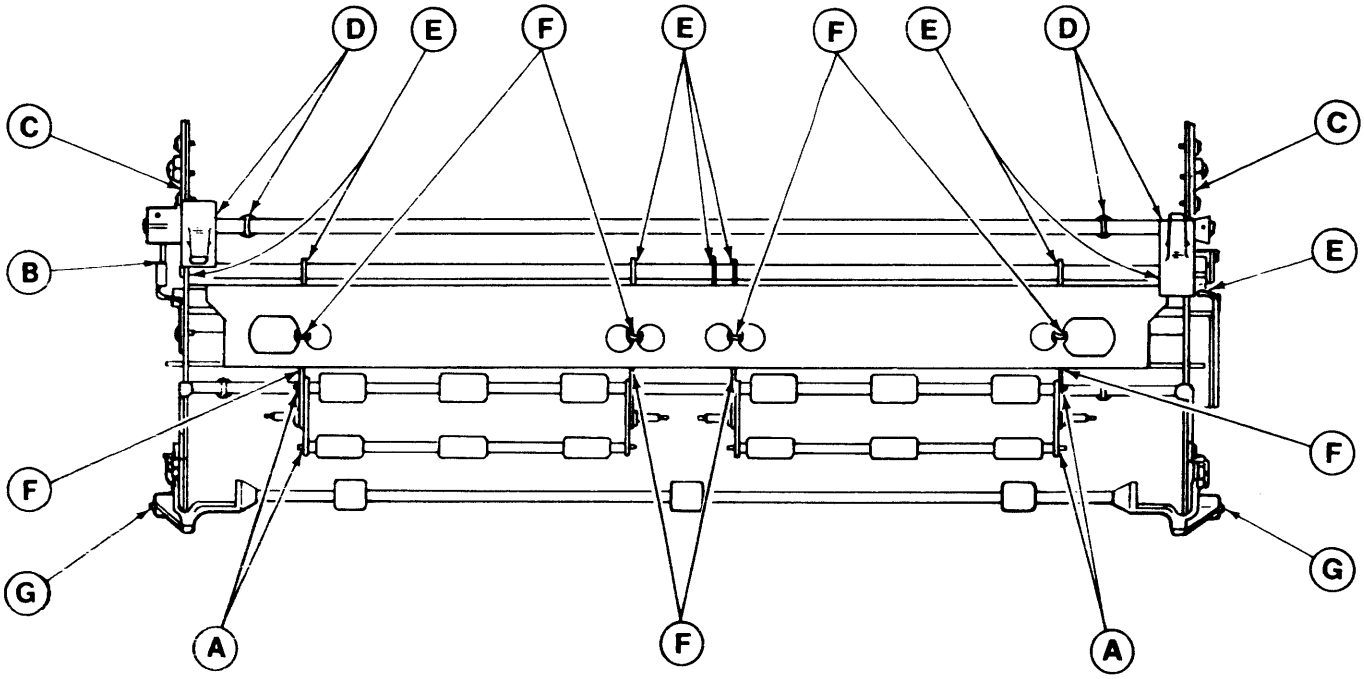


Figure 3-1. Carrier System Lubrication Points

3.2.3.1 Carrier System

Refer to Figure 3-1. Lightly grease all the points indicated in this procedure with Diablo no. 70825-01 grease.

1. Paper Feed Roller Shaft Pins (A).
2. Platen Position Lever Detent Plate (inside surface) (B).
3. Platen Position Slide Plates (carrier frame) (C), with the lever moved limit to limit. Also grease all points of the contact with pivots, eccentrics, guides, etc.
4. Platen Position Torque Shaft Ends, Bearing Surfaces, and Spring Loops (D).
5. Paper Release Lever Tab Ramp and Shaft Piviots (E).
6. Paper Release Torque Shaft Pivots and Arm Slots (F).
7. Paper Bail Pivots (G).

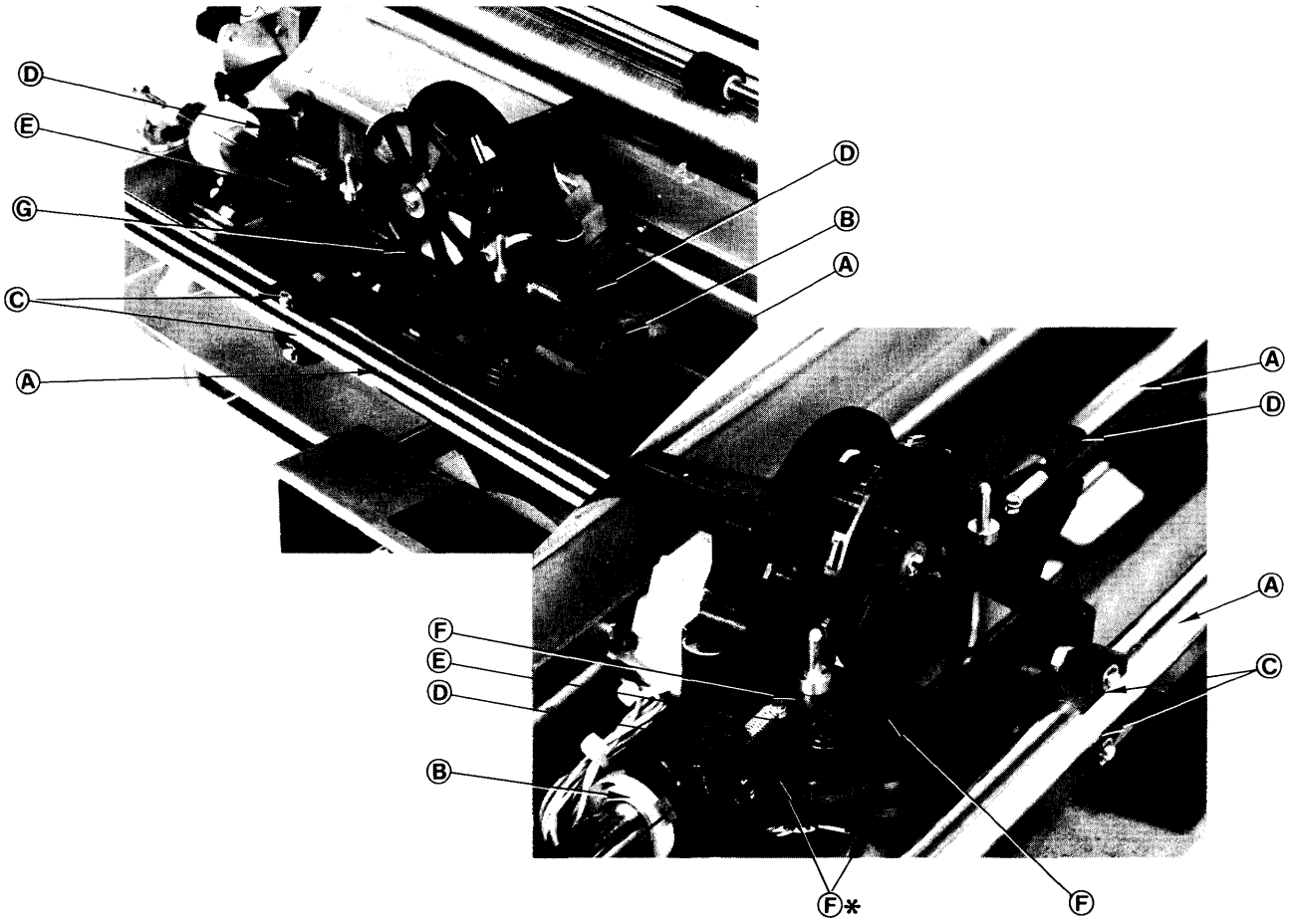


Figure 3-2. Carriage System Lubrication Points

3.2.3.2 Carriage System

Refer to Figure 3-2. While this system is to be lubricated at normal 6 month or 500 hour intervals, it may need additional attention if the printer has not been used for some time.

1. Carriage Rails (A) — Clean the rails with alcohol wipes.
2. Carriage Rear Bearings (B) — Place 4 - 5 drops of No. 70243 oil on the rail beside each bearing. Move the carriage back and forth manually to spread the oil and saturate the felt washers inside each bearing.
3. Carriage Front Bearings (C) — Swab the top and bottom rail surfaces with No. 70243 oil. Leave a thin film only - no droplets.
4. Ribbon Cartridge Latches (D) — Apply one small drop on No. 70243 oil to each latch pivot, and moisten the latch return spring ends.
5. Ribbon Drive Capstan (E) — Apply one drop of No. 70243 oil to the capstan drive blade and hub. Work the blade up and down manually a few times to spread oil to the blade shaft in the hub.
6. Ribbon Drive Clutches (F) — Apply one very small drop of No. 70243 oil to each clutch pulley shaft end. Wipe all gears with the oil. *Oil the clutch springs by spreading oil lightly across their surfaces.
7. Ribbon Drive Pulley (G) — Apply one drop of No. 70243 oil to the upper end of the pulley shaft.

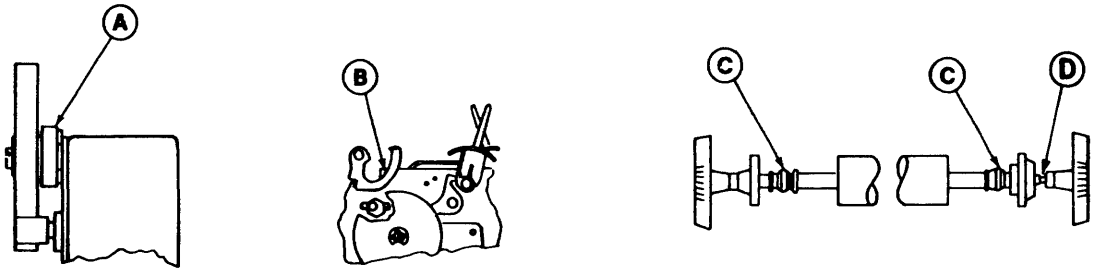


Figure 3-3. Platen System Lubrication Points

3.2.3.3 Platen System

Refer to Figure 3-3.

1. Paper Feed Idler Gear (A) — Inspect the large felt washer behind this gear. If it is becoming white in color, saturate it with 70364 Polyoil.
2. Platen Latches (B) — Lightly grease the contact area between these arms and the carrier side frames with No. 70825-01 grease.
3. Platen Hubs (C) — Apply one drop of No. 70243 oil to the shaft between the knob end and drive gear hub.

NOTE

This procedure is applicable to optional pin feed platens. The pin cam area of these platens is self-lubricating, and does not require additional lubrication for the life of the unit.

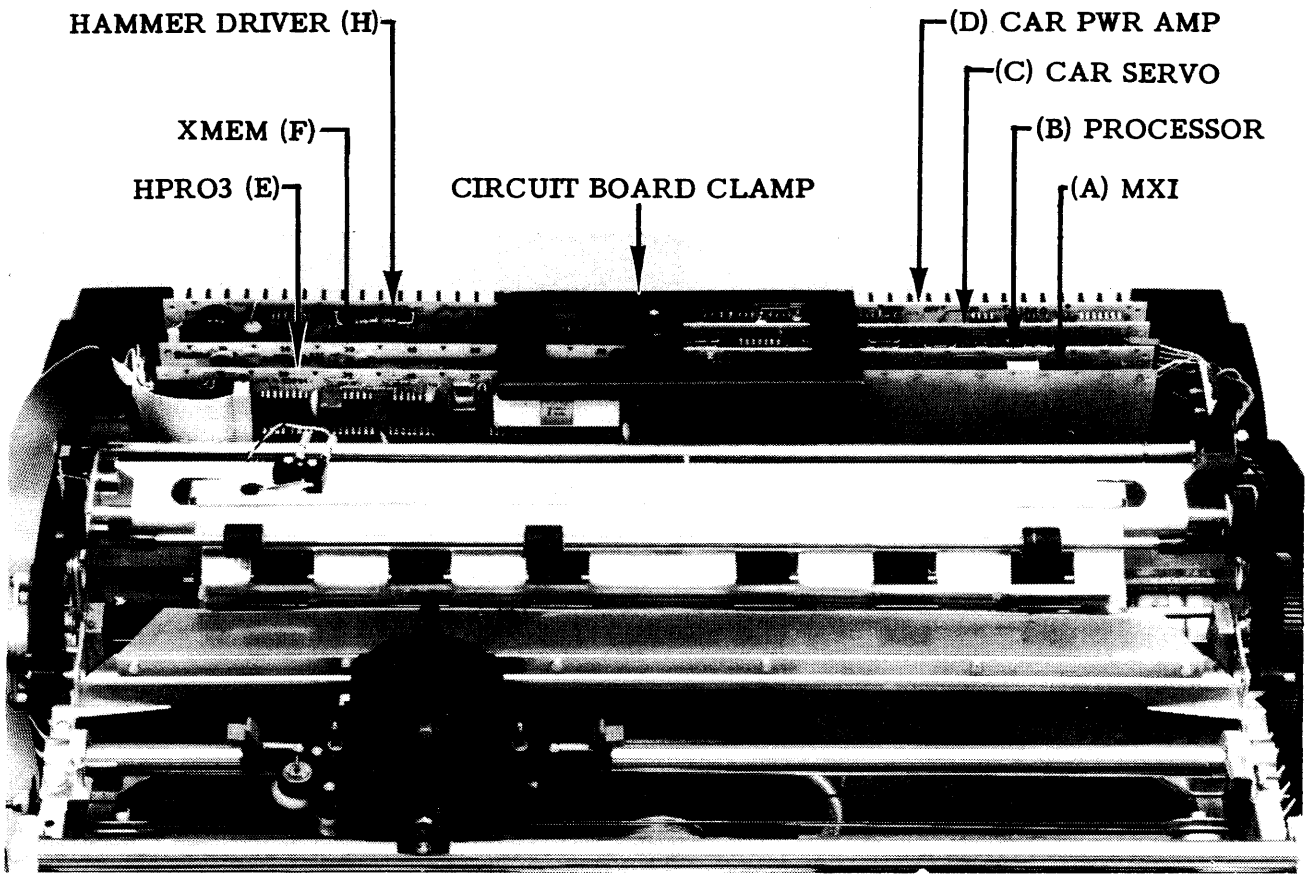


Figure 3-4. Circuit Board Locations

3.3 MODULE REMOVAL AND REPLACEMENT

Always make certain that the power cord is unplugged from the ac outlet before attempting to replace any components or modules.

All modules have been assigned "assembly numbers" according to the system adopted by the American National Standards Institute (ANSI) in their standard no. Y32.16: "Reference Designations for Electrical and Electronics Parts and Equipments." Table 3-1 lists all major assemblies, and the smaller assemblies that are normally considered replaceable as modules, along with their reference designations. These designations are used in the remainder of this section and in the schematics and wiring diagrams to identify the various assemblies.

Table 3-1. Major Assemblies and Modules

Assembly No. (Reference Designators)	Description
A1	Matrix Printer
A1A1	Matrix Interface (MXI) Board
A1A2	Processor Board
A1A3	Carriage Servo Board
A1A4	Carriage Power Amplifier Board
A1A5	HPRO3 Board
A1A6	XMEM Board
A1A8	Hammer Driver Board
A1A9	Mother Board
A2	Power Supply
A3	Keyboard
A4	Control Panel

3.3.1 Printed Circuit Boards

CAUTION

Never remove or install circuit boards or connectors while power is applied to the HyTerm.

(1) Turn the power off and unplug the cord from the ac outlet.

(2) Remove the paper or forms from the printer. Remove the forms tractor if applicable (see 1660 Product Description, paragraph 2.4.3).

(3) Remove the top cover and accessories from the printer (see 3.1.2).

(4) Remove the screw in the center of the circuit board clamp (see Figure 3-4) and remove the clamp.

(5) Locate the circuit board to be removed (see Figure 3-4).

(6) Grasp the circuit board firmly at the two upper corners and pull it straight up, taking care not to stress any existing cable connections.

(7) Disconnect all remaining cables from the circuit board.

REPLACEMENT

(1) Check all jumper positions and switch settings on the circuit board. Verify that the board is configured correctly.

(2) If the HPRO3 board is being installed, first attach the keyboard cable to the P2 connector on the circuit board.

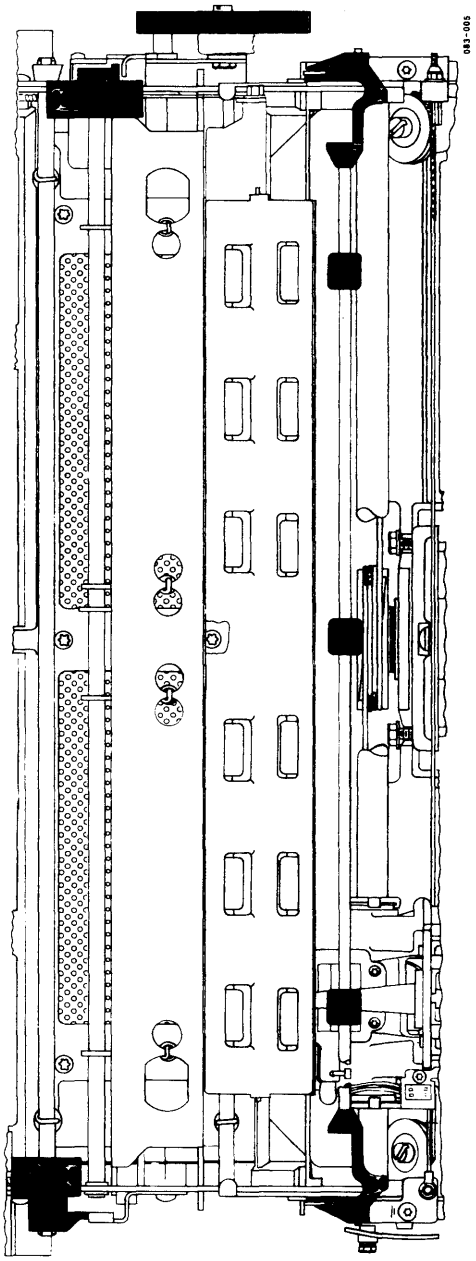


Figure 3-5. Power Supply Mounting

(3) Holding the board with the component side toward the front of the printer (toward the platen), insert the circuit board into the guides and slide it all the way down until it contacts the connector on the motherboard.

(4) Using firm, equal pressure on both upper corners of the board, push it down so that it is fully seated into the socket.

NOTE

If excessive resistance is encountered, check to make sure the proper board is being installed in the socket: all boards are keyed so they will not fit in the wrong socket (refer to Figure 3-4).

(5) Replace the platen, insert a sheet of paper, and apply power to the HyTerm. Test the HyTerm at this time.

(6) After determining that the terminal is operating properly, remove power and install the circuit board clamp. Remove the platen and install the top cover and accessories (see 3.1.2).

3.3.2 Power Supply

REMOVAL

(1) Turn the power off and unplug the power cord from the ac outlet.

(2) Move the HyTerm to a location where both the top and bottom are accessible when the HyTerm is tilted back (preferably a work bench).

(3) Remove the top cover following the procedure in 3.1.2. Remove the paper cradle (see Figure 3-5).

(4) Tilt the HyTerm up so it is resting on the rear edge of the bottom cover, and remove the screen-like bottom pan. Loosen the three rear screws and remove the three forward and two side screws; then slide the bottom pan off the HyTerm. Lay the HyTerm back on its feet.

CAUTION

When tipping the HyTerm up, be certain to use a flat surface, with no foreign objects in the way. Any small object could cause pressure to be applied to the rear heat sinks, which are mounted on the power amplifier boards. Excess pressure on these boards could damage the boards and/or the mother board.

(5) Look down into the platen area of the printer and locate the power supply, which is covered by an aluminum screen. Remove the four mounting screws from the top of the power supply (see Figure 3-5). The supply will drop slightly and rest on the work surface.

(6) Tilt the HyTerm up slightly and reach underneath to hold the power supply with your hand (to prevent it from falling). Then tilt the HyTerm all the way up so that it rests on the rear edge of the bottom cover.

(7) Slide the power supply out of the printer enough to access the terminal strip at the right side of the power supply. Disconnect the wiring from the terminal strip. Set the power supply aside and set the HyTerm down on its feet.

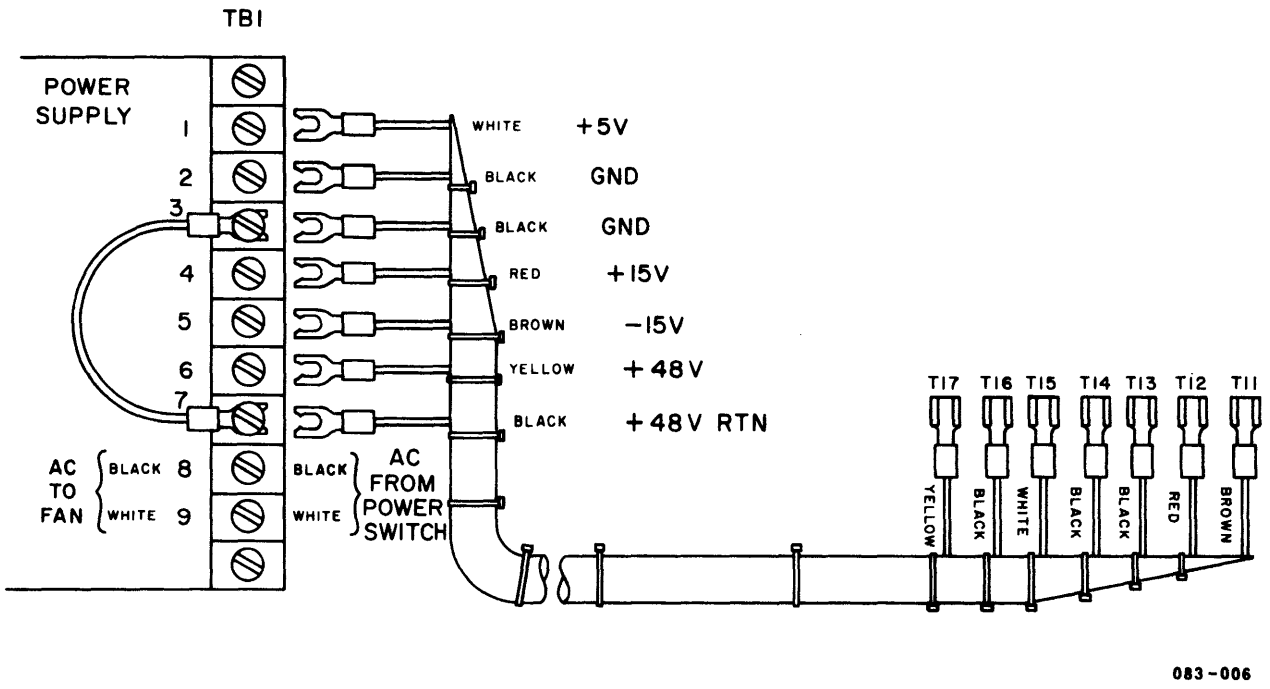


Figure 3-6. Power Supply Connections

REPLACEMENT

(1) Tilt the HyTerm up on the rear edge of the bottom cover and connect the wires to the power supply terminal strip as shown in Figure 3-6. Observe the caution about tilting the HyTerm noted in step (4) above.

(2) Swing the power supply into position inside the printer casting. Make sure all wires and cables are routed correctly and securely.

(3) Holding the power supply in position, insert the mounting screws through the cover screen and the printer casting and start them into the threads in the power supply frame. Start all four mounting screws.

(4) Set the HyTerm back down on its feet. Tighten all four power supply mounting screws securely.

(5) Locate the power connections (+48V, +15V, -15V and +5V) at the right side of the mother board between the card cage and the rear right side of the bottom cover (see Figure 3-25).

(6) Plug the HyTerm into an ac outlet and turn the POWER switch on. Verify that the HyTerm does a restore (carriage moves to left).

(7) Using a voltmeter, measure the voltages between ground and each of the four power connections on the motherboard. The voltages should read as follows when under load conditions:

+5V = +4.75 to +5.25 volts
+15V = +15 to +16 volts
-15V = -15 to -16 volts
+48V = +48.5 to +50.5 volts

If voltages do not read within the ranges above, see 3.4.3.

(8) Temporarily install the platen and a sheet of paper and test the HyTerm for proper operation by running a Self-Test routine and by entering data from the keyboard. If operation is satisfactory, turn the POWER switch off and unplug the power cord.

(9) Tilt the HyTerm up again and install the screenlike bottom pan by sliding it under the three rear screws and then installing the remaining five screws. Tighten all eight bottom pan mounting screws.

(10) Set the HyTerm down on its feet and install the paper cradle.

(11) Replace the top cover and accessories (see 3.1.2).

(12) Insert paper, apply power, and test the HyTerm thoroughly.

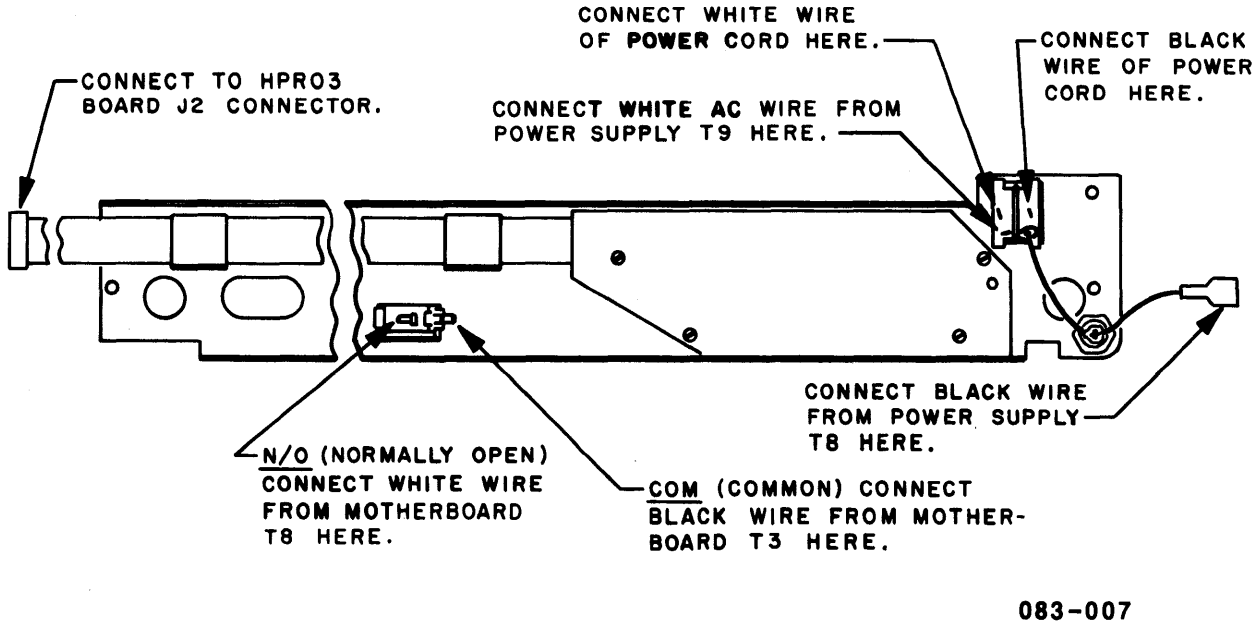


Figure 3-7. Control Panel Connections

3.3.3 Control Panel

REMOVAL

(1) Set the power switch to off and unplug the power cord from the ac outlet.

(2) Remove the top cover and accessories (see 3.1.2).

(3) Remove the keyboard mask by lifting up on the forward corners of the mask until it "pops" loose, then lift the mask from the keyboard.

(4) Remove the four control panel mounting screws (two screws on each side of the panel).

(5) Remove the HPRO3 board from slot (E) of the mother board (see Figure 3-4); disconnect the control panel cable at the J2 connector.

(6) Disconnect the remaining wiring on the rear of the control panel and lift the control panel off the HyTerm.

REPLACEMENT

(1) Connect the control panel wiring on the rear of the panel referring to Figure 3-7.

(2) Connect the control panel cable to the J2 connector on the HPRO3 board and install the HPRO3 board into slot (E) of the mother board (see Figure 3-4).

(3) Set the control panel in place and install the four mounting screws and tighten securely.

(4) Install the keyboard mask by setting it in place and applying pressure on the forward corners of the mask until its "pops" securely into place.

(5) Install the top cover and accessories (see 3.1.2).

(6) Apply power and test the HyTerm.

3.3.4 Keyboard

REMOVAL

(1) Turn the power off and unplug the power cord from the ac outlet.

(2) Remove the top cover and accessories (see 3.1.2).

(3) Remove the keyboard mask by lifting up on the forward corners of the mask until it "pops" loose, then lift the mask from the keyboard.

(4) Remove the four keyboard mounting screws (two on each side).

(5) Disconnect the keyboard cable connector which is visible through an access hole cut in the left side of the control panel.

(6) Remove the keyboard by first sliding it to the right then lifting up on the left forward corner and swinging the left side out first, then the right. Set the keyboard aside where it will not be damaged.

REPLACEMENT

(1) Set the right side of the keyboard into place and then swing the left side into place.

(2) Connect the keyboard cable to the keyboard connector.

(3) Center the keyboard on its mounting brackets and install the four mounting screws. Tighten the mounting screws down securely.

(4) Install the keyboard mask by setting it in place and applying pressure on the forward corners of the mask until its "pops" into place.

(5) Install the top cover and accessories (see 3.1.2).

(6) Apply power and test the HyTerm.

3.3.4.1 Keyswitch Removal/Replacement

Once the keyboard has been removed from the HyTerm, individual keyswitches can be replaced if necessary. The required tools for keyswitch replacement are a low-wattage soldering iron, a solder removal tool, 60/40 rosin-core solder, and a long needle-nose pliers.

CAUTION

When removing the keytops from the "Press-to-Latch/Press-to-Release" keyswitches in the control section of the keyboard, always place the keyswitch in the released (up) position to avoid damage to the module.

REMOVAL

(1) Remove the keytop from the module being replaced by lifting or prying upward with a padded tool. Remove the keytops from the modules on either side of the one being replaced. It may also be necessary to remove other adjacent keytops to provide adequate work space.

(2) Unsolder the four module terminals from the keyboard's circuit board. Use a solder removal tool to remove all solder from the pin holes in the circuit board.

(3) Grip the switch module retaining clip release tabs on two sides of the module with the needle-nose pliers. Squeeze the pliers while pulling up on the module to free the module from the circuit board.

REPLACEMENT

(1) Grip the switch module retaining clip release tabs on two sides of the switch with the needle-nose plier. Squeeze the pliers while inserting the module into place; release the pliers once the module is in place.

NOTE

Make sure the module is properly oriented and that the four pins are through the holes in the circuit board.

(2) Solder the new switch module terminals using 60/40 rosin-core solder and a low-wattage soldering iron.

CAUTION

Never hold the soldering iron to the module pins for more than four seconds.

(3) The solder joints should be cleaned on the bottom side of the circuit board with a mild solvent. Be careful not to get any solvent on the switch module or keytops.

(4) Replace all keytops making certain that they are placed on the right module and are properly oriented.

3.3.5 Printer

REMOVAL

(1) Turn the power off and unplug the power cord from the ac outlet.

(2) Remove the top cover and accessories (see 3.1.2).

(3) Disconnect the following wiring and cables:

1. The ground wire from the printer to the bottom cover at the terminal post in the front, center of the bottom cover.
2. The ac power cord ground wire connected to the printer's frame near the right carriage pulley. Disconnect the ac cord clamp at the printer's right side frame.
3. The Cover-Open switch wires from the mother board at the Cover-Open switch on the control panel.
4. The ac wires from the control panel to the mother board at the power switch and fuse.
5. The keyboard cable at the HPRO3 board J2 connector.
6. The control panel cable from the P2 edge connector on the HPRO3 board.

(4) Tilt the HyTerm up and remove the four screws that hold the bottom cover to the printer at the shock mounts.

(5) Set the HyTerm down on its feet and lift the printer straight up and out of the bottom cover.

NOTE

If any unusual resistance is felt when lifting the printer out of the bottom cover, double check all wire and cable connections to determine what is causing the resistance. Never force the printer out of the bottom cover.

REPLACEMENT

(1) Set the printer in place inside the bottom cover making sure that no wires or cables are pinched between the printer frame and the bottom cover.

(2) Tilt the HyTerm up and install the four mounting screws through the bottom cover and into the printer shock mounts. Tighten securely.

(3) Connect all the wires and cables listed in step (3) of the removal instructions above.

(4) Replace the top cover and accessories (see 3.1.2).

(5) Apply power and test the HyTerm thoroughly.

3.3.6 Print Head

REMOVAL

(1) Turn the power off and unplug the power cord from the ac outlet.

(2) Remove the access cover.

(3) Remove the two setscrews that hold the print head to the carriage assembly.

(4) Disconnect the print head connector located directly below the print head on the carriage assembly. Lift the print head off the carriage assembly.

REPLACEMENT

(1) Connect the print head connector to its mate on the carriage assembly.

(2) Set the print head in place and install the two setscrews through the mounting bracket and into the print head. Tighten securely.

(3) Replace the access cover.

(4) Apply power and test the print head for proper character representation. If the print quality is not sufficient, refer to the printer adjustment section (3.4.1).

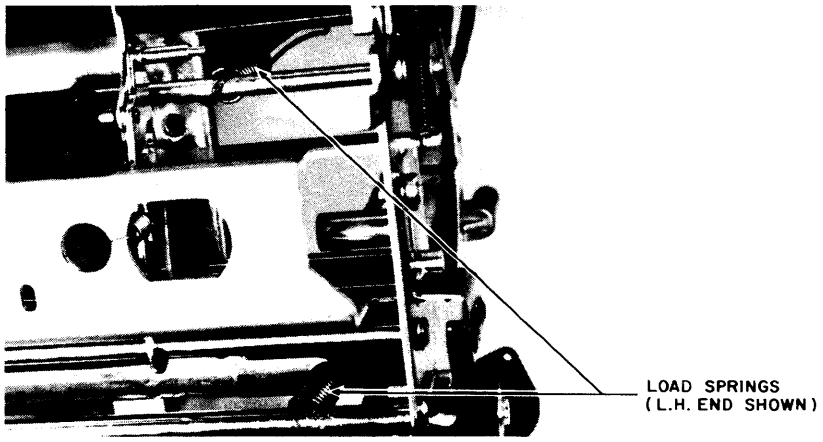


Figure 3-8. Carrier System Removal—A

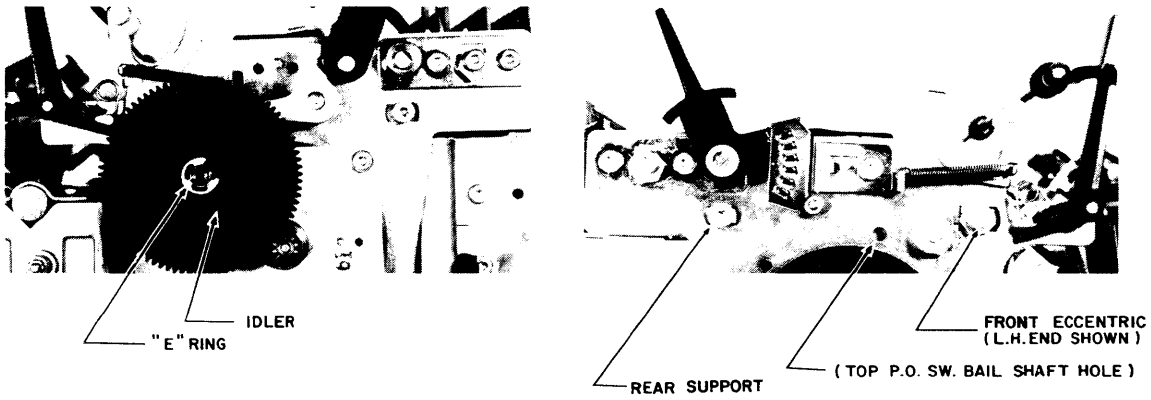


Figure 3-9. Carrier System Removal—B

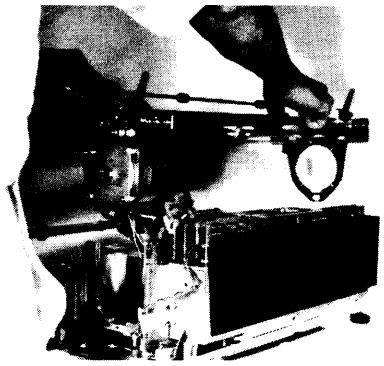


Figure 3-10. Carrier System Removal—C

3.3.7 Paper Carrier Subassembly

REMOVAL

(1) Remove the printer from the bottom cover following the procedure in 3.3.5 and place the printer on a sturdy work bench or table.

(2) Remove the ribbon cartridge and paper cradle and set them aside with the other accessories.

(3) Stand the printer up on the front end of its main frame. Use a #99009 T-Handle Spring Hook to disengage the four Carrier System load springs from the printer's main frame (two long springs in front and two short springs in the rear). See Figure 3-8.

(4) Open the wire bundle to the mother board and disconnect the four paper feed motor wires from the mother board at T4, T5, T6, and T7 (see Figure 3-19). Also disconnect the Paper-Out switch wires from the mother board at T9 and T10 and open the associated wire bundle.

(5) Return the printer to its upright position. Remove the two mounting screws and spacers from the fan on the left side of the Carrier Subassembly and lay the fan next to the printer. Move to the right side and cut the tie wraps from the wire bundle mounted to the paper feed motor.

(6) Remove the E-ring, the paper feed idler gear, and the felt washer (see Figure 3-9) to facilitate easy access to the right-hand carrier height eccentric.

(7) Using a 1/4" wrench or nut driver, remove the left- and right-side front Carrier Subassembly height adjustment eccentrics. Using a TORX T15 screwdriver, remove the left- and right-hand rear Carrier Subassembly support shoulder screws (see Figure 3-9).

(8) Carefully lift the Carrier Subassembly, including the paper feed motor, free of the printer's main frame, as shown in Figure 3-10. Be sure the motor wires and Paper-Out switch wires are free and not caught in the wire bundle.

REPLACEMENT

(1) Clean all Carrier Subassembly bearing surfaces on the printer's main frame of old grease, etc. Apply a light coating of multipurpose grease to the points shown in Figure 3-11, on both ends of the main frame.

(2) Carefully lower the Carrier Subassembly down into position on the printer's main frame. Refer to Figure 3-10.

(3) Insert the left- and right-hand rear Carrier Subassembly shoulder support screws using a TORX T15 screwdriver (see Figure 3-9). Make sure the screw shoulders pass into the slots in the Carrier side frame, and tighten the screws firmly. DO NOT over-tighten and strip the threads from the holes in the main frame casting.

(4) Insert the left- and right-hand front Carrier Subassembly height adjustment eccentrics using a 1/4" wrench or nut driver. Make sure the shoulders of the eccentrics pass into the slots in the Carrier side frames, and thread the screws in far enough to retain the eccentrics snugly in the slots, but DO NOT tighten. The eccentrics should be positioned so their lobes point toward the rear of the machine.

(5) Install the fan on the left side of the Carrier Subassembly so that the standoffs rest between the Carrier's side frame and the fan mounting bracket. Tighten the two fan mounting screws with a TORX T15 screwdriver.

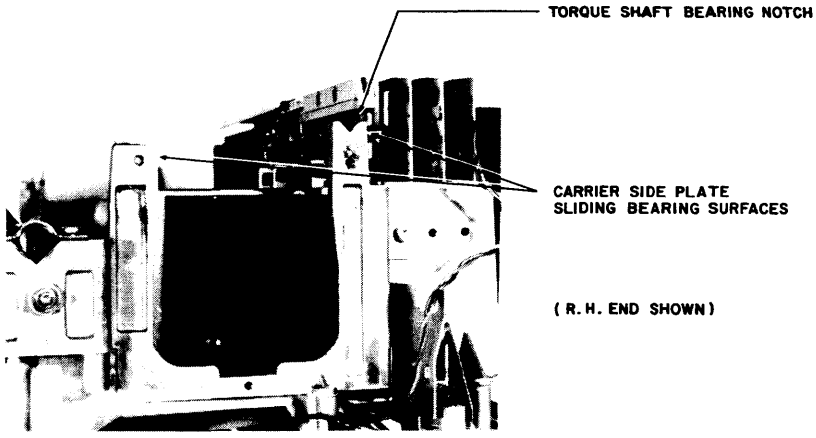


Figure 3-11. Carrier System Replacement

(6) Using a tie wrap, secure the wire bundle to the right side frame at the paper feed motor. Replace the felt wiper, the paper feed idler gear, and the E-ring.

(7) Stand the printer on the front end of its main frame. Use the #99009 T-Handle Spring Hook to connect the loose ends of the four Carrier Subassembly load springs to the main frame making use of the holes provided (see Figure 3-8).

(8) Arrange the four paper feed motor wires and the two Paper-Out switch wires into the proper wire bundles running along the edge of the mother board. Connect the wires to the mother board as follows:

Red (paper feed motor) to T4
Yellow (paper feed motor) to T5
Black (paper feed motor) to T6
Gray (paper feed motor) to T7
Yellow (Paper-Out switch) to T9
Brown (Paper-Out switch) to T10

Secure the wire bundles with tie wraps or equivalent.

(9) Reinstall the printer into the bottom cover following the procedure in 3.3.5. Install the paper cradle and ribbon cartridge.

(10) Perform the printer adjustments described in section 3.4.1.

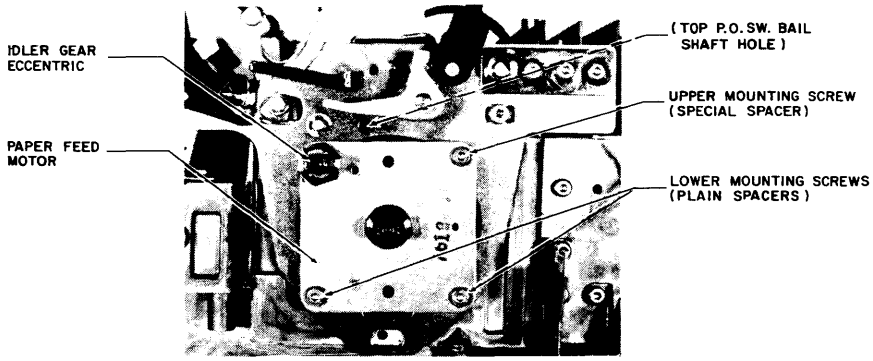


Figure 3-12. Paper Feed Motor Removal/Replacement

3.3.8 Paper Feed Motor

REMOVAL

(1) Remove the printer from the bottom cover following the procedure in 3.3.5 and place the printer on a sturdy work bench or table.

(2) Stand the printer up on the front end of its main frame. Open the wire bundle from the paper feed motor to the mother board and disconnect the four paper feed motor wires from the mother board at T4, T5, T6, and T7.

(3) Return the printer to its upright position. Remove the E-ring, paper feed idler gear, and the felt washer from the paper feed motor on the right side frame. Cut the tie wrap from the wire bundle mounted to the paper feed motor.

(4) Using a TORX T15 screwdriver, remove the three paper feed motor mounting screws and the three spacers installed between the motor flange and printer frame. Note that the upper right-hand spacer has a shoulder which fits into the motor flange hole to prevent side play.

(5) Tilt the motor down and out of the printer frame, and gently pull its connecting wires free from the wire bundle inside the printer.

(6) Using an 11/32" open end wrench and a blade screwdriver, remove the paper feed idler gear mounting stud eccentric, nut, and two washers from the paper feed motor's upper left-hand flange hole (see Figure 3-12).

REPLACEMENT

(1) Orient the (new) paper feed motor to the printer frame so that the motor shaft points outward and the motor wires point directly downward. Now insert the idler gear mounting stud through the upper left-hand motor flange hole. Install the two washers and nut from the rear of the flange. Thread the nut on finger-tight only; it will be tightened later when performing the paper drive adjustments.

(2) Carefully insert the paper feed motor wires into the opening in the right-hand printer side frame, and tilt the motor into position in the frame opening.

(3) Insert the special spacer [noted in step (4) above] behind the motor's upper right flange hole, with its shoulder extending into the flange hole. Loosely thread a motor mounting screw through the upper right flange hole, through the spacer, and into the printer side frame.

(4) Place the other two spacers behind the two lower flange holes and install (finger-tight) the remaining two motor mounting screws. Now tighten the upper right mounting screw until it is snug, but not so tight as to restrict lateral movement of the motor.

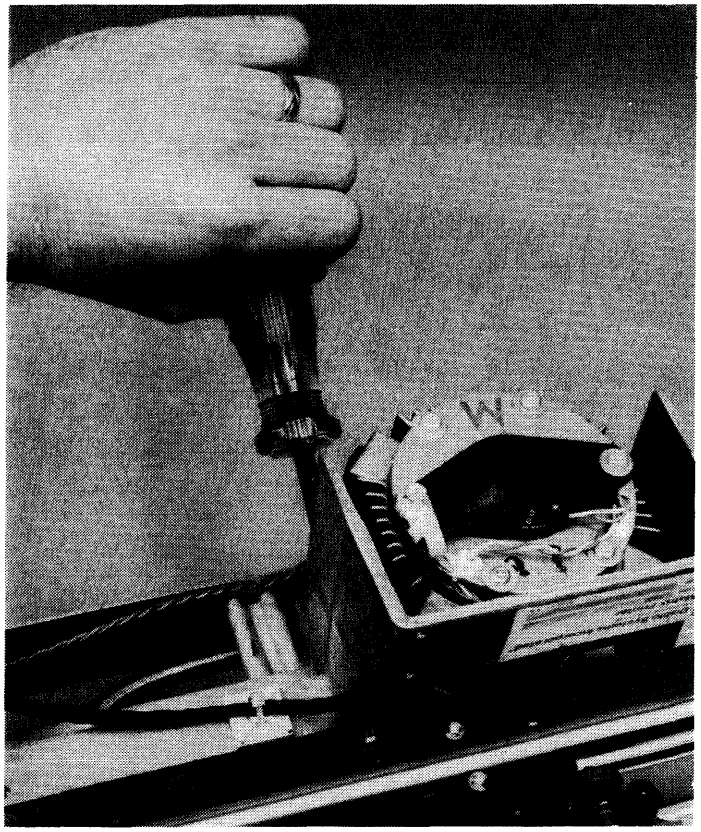
(5) Replace the felt washer, idler gear, and E-ring on the idler gear mounting stud. Also replace the tie wrap on the wire bundle previously secured to the paper feed motor with a stick-on mount. It may be necessary to replace the stick-on mount at the same time.

(6) Arrange the four paper feed motor wires into the wire bundle running along the edge of the mother board. Connect these wires to the mother board as follows: red to T4, yellow to T5, black to T6, and gray to T7. Secure the wire bundle with tie wraps.

(7) Reinstall the printer into the bottom cover following the procedure in 3.3.5.

(8) Perform the printer adjustments described in section 3.4.1.

a.



b.

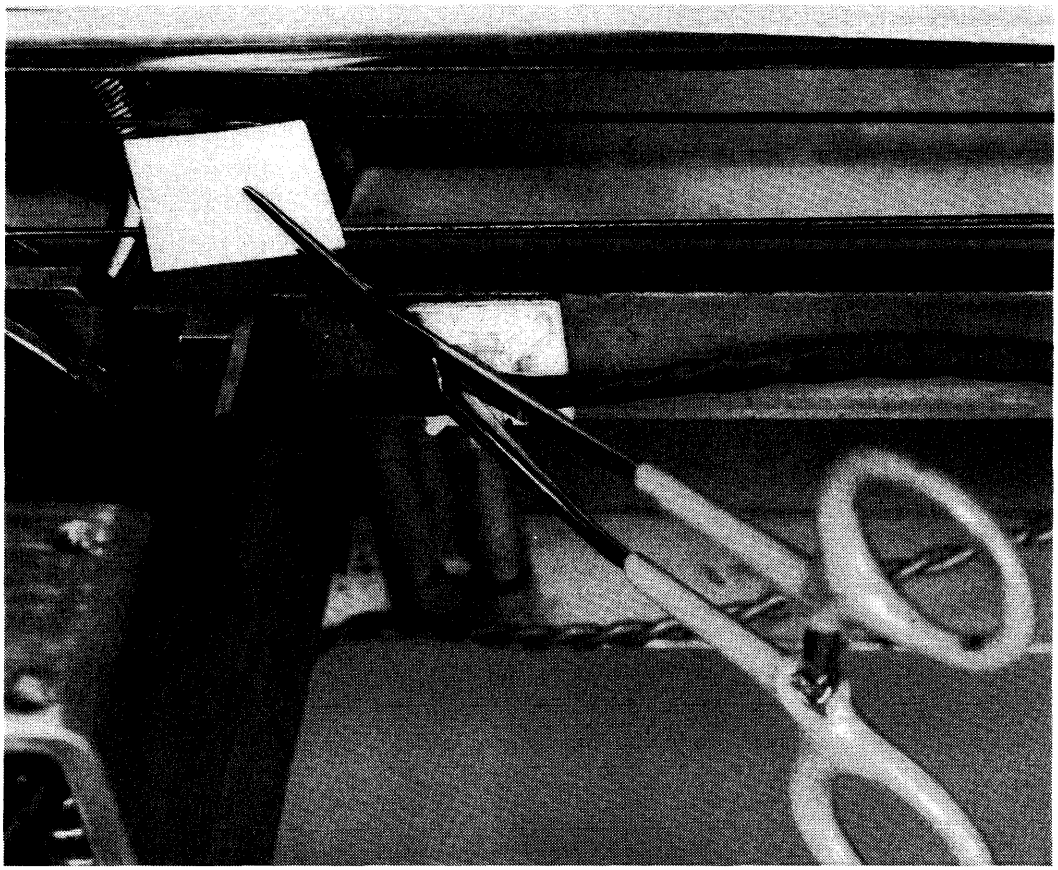


Figure 3-13. Carriage Drive Cable Pulley Removal

3.3.9 Carriage Subassembly

REMOVAL

(1) Turn the power off and unplug the power cord from the ac outlet.

(2) Remove the top cover and accessories (see 3.1.2).

(3) Remove the ribbon cartridge and store with the other accessories.

(4) Loosen the ribbon drive cable locknut at the right end of the cable, but do not remove. Remove the E-ring from the fastening post at the left end of the ribbon drive cable and slip the cable ring off the post. Remove the ribbon drive cable from around the ribbon drive pulley and lay the cable out of the way over the printer's left side frame.

(5) Position the carriage slightly to the right of center to gain access along the right side of the carriage servo motor to the mounting screw for the carriage drive cable pulley. Install a hemostat clamp on the pulley as shown in Figure 3-13a (use a piece of heavy paper between the pulley and the hemostat clamp jaws to protect the pulley flanges). This prevents the pulley from moving or flipping over and releasing the drive cables. Referring to Figure 3-13a, note that the hemostat clamp is installed to trap the upper forward right-hand cable segment between its jaws as it is clamped to the pulley. Make sure this has been done, and that the clamp is secure before proceeding.

(6) Use a TORX T15 screwdriver to reach up beside the carriage motor and remove the pulley mounting screw (see Figure 3-13b). Make sure the pulley is free from the carriage frame, and gently move the carriage to the left to clear the pulley. Retrieve the spacer from the top of the pulley, and note that the spacer has a shoulder which extends down into the center of the pulley when properly assembled. Store the spacer and pulley mounting screw. DO NOT remove the hemostat clamp from the pulley!

(7) Use a small blade screwdriver to remove the ribbon motion sensor mounting bracket from the carriage. Use a TORX T9 screwdriver to remove the Molex connector mounting bracket from the carriage subassembly. Disconnect the Molex connector and remove the spring-type cable shield from the snap-in metal clip mounted to the carriage subassembly. Lay the entire cable (with the removed mounting brackets) on the bottom of the carriage trough.

(8) Using a Torx T15 screwdriver, loosen the eight carriage rail clamp screws from the front and rear carriage rail clamps on both sides of the printer. Slide the front rail to the left until it clears the carriage rail bearings. Slide the rear carriage rail slightly to the left and remove the heavy rubber washer and metal washer from the rail. While holding the carriage in one hand, continue sliding the rear rail leftward until the rail slides out of the rear carriage bearing sleeve and is free of the carriage subassembly.

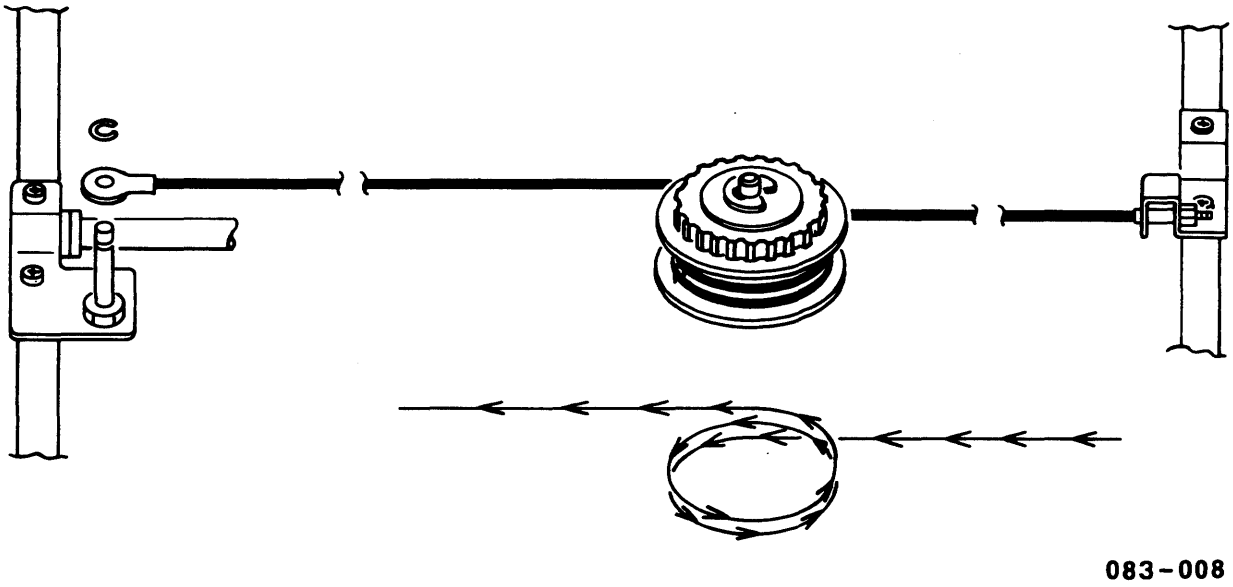


Figure 3-14. Ribbon Drive Cable Replacement

REPLACEMENT

NOTE

When installing a new carriage subassembly from the factory, it will be necessary to saturate the felt wipers provided with a light oil and install them and their white plastic snap-on covers into both ends of the rear carriage rail bearing sleeve.

(1) Using a TORX T15 screwdriver, remove the carriage drive pulley and spacer from the carriage subassembly to be installed. If carriage drive cables have been removed or if the carriage drive pulley is to be replaced, refer to 3.3.10 before proceeding.

(2) Clean both carriage rails with alcohol and check them for surface defects and for straightness. Replace any rail which has surface damage or is bent. Carefully slide both carriage rails through the right-hand rail clamps into the printer about half way.

(3) Slide one of the heavy rubber washers over the left end of the rear carriage rail. Holding the carriage subassembly in one hand, gently slide the carriage subassembly onto the carriage rails. Be careful not to stretch or break the lubricated felt wipers installed at both ends of the rear carriage bearing. Also be sure that the forward carriage rail rests between the two forward carriage slide bearings. With the carriage subassembly installed on the carriage rails, place the other heavy rubber washer, followed by the metal washer, on the left end of the rear carriage rail (a heavy rubber washer should be on both sides of the carriage subassembly's rear bearing). Slide both carriage rails into the clamps on the left printer side frame making sure that the rails come to rest in the notches provided on both sides of the printer. Using a TORX T15 screwdriver, tighten the two forward and two rear carriage rail clamps on both sides of the printer. Move the carriage back and forth along the rails to ensure smooth and even carriage movement.

(4) Place the spacer, removed in step (6) above, on top of the carriage drive pulley with the shoulder extending down into the center of the pulley. Position the carriage subassembly over the clamped carriage drive pulley, and insert the shoulder screw through the pulley and spacer, and into the mounting hole on the carriage. Using a TORX T15 screwdriver, tighten the shoulder screw and remove the hemostat clamp.

(5) Retrieve the spring-shielded cable (including the print head connector and ribbon sensor mounting bracket) from the carriage trough and snap the cable shield into the metal clamp on the bottom of the carriage. Connect the print head connector to its mate from the print head. Install the two mounting bracket screws and tighten them with a TORX T9 screwdriver. Set the ribbon sensor mounting bracket in place on the carriage and install, tightening the mounting screw.

(6) Route the ring end of the ribbon drive cable (stored at the right side frame) through the carriage behind the ribbon drive pulley. Make two CCW revolutions (looking from the top of the pulley) around the ribbon drive pulley and continue to run the cable to the left until the fastening post on the left side frame is reached (see Figure 3-14). Slip the cable ring over the fastening post and install the E-ring on the post.

(7) Perform the printer adjustments described in section 3.4.1.

(8) Replace the ribbon cartridge. Reinstall the top cover and accessories (see 3.1.2) when the HyTerm is ready to return to service.

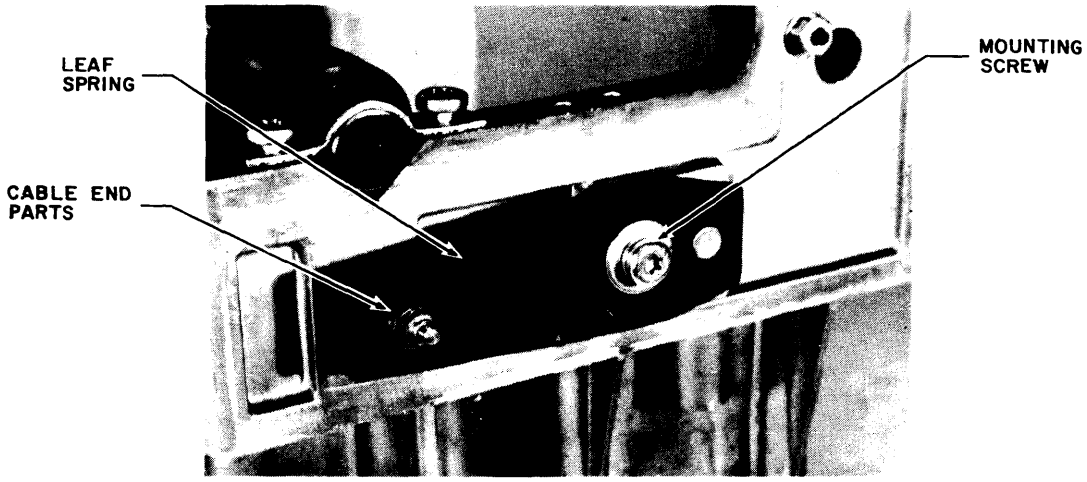


Figure 3-15. Carriage Drive Cable Tension Spring

3.3.10 Carriage Drive System

This section outlines the removal and replacement of the carriage drive system, which includes the carriage drive cables and the carriage servo motor.

REMOVAL

(1) Turn the power off and unplug the power cord from the ac outlet.

(2) Remove the top cover and accessories (see 3.1.2).

(3) Remove the printer from the bottom cover (see 3.3.5).

(4) Position the carriage slightly to the right of center to gain access along the right side of the carriage servo motor to the mounting screw for the carriage drive pulley on the lower portion of the carriage. Use a TORX T15 screwdriver, reach up beside the carriage motor, and remove the carriage pulley mounting screw. Make sure the pulley is free from the carriage subassembly, and move the carriage to the side to clear the pulley. Retrieve the spacer from the top of the pulley; note that the spacer has a shoulder which extends down into the center of the pulley for later reassembly.

(5) Referring to Figure 3-15, use a TORX T15 screwdriver to loosen the mounting screw and release the tension on the drive cable tension leaf spring, located on the left side frame. This will release the tension of the carriage drive cables.

(6) Retrieve the carriage drive pulley, and unthread the two drive cables from around the servo motor's capstan and fixed side pulleys. Note that the ball end of the left-hand cable is trapped between the servo motor's capstan and the printer frame. Rotate the capstan so that the notch is in the six o'clock position and release the ball and cable from the bottom of the printer.

If the carriage servo motor is <u>not</u> to be removed, skip to step (5) of the Replacement instructions.

(7) Stand the printer up on the front end of its frame. Using a TORX T15 screwdriver, remove the four fastening screws from the carriage trough bottom plate and move the plate out of the way.

(8) Remove the cable ties while following the servo motor's tranducer and power cables to their respective circuit board connections. Note each cable routing for later reassembly. Disconnect the transducer cable at the J8 connector on the CAR SERVO board in slot C of the mother board. Disconnect the power cable at the B75 and C75 connections on the CAR PWR AMP board in slot D of the mother board.

(9) Using a 1/4" wrench, remove the two hex head thread forming screws and flat washers holding the servo motor to the printer frame. Remove the servo motor and its attached cables, noting their orientation for later reassembly.

REPLACEMENT

(1) On the replacement carriage servo motor, lightly coat those surfaces which will contact the printer's frame with heat sink compound. With the printer still up on the front end of its frame, orient the servo motor with the capstan up, and the two-wire power cable to the left (as viewed from the bottom of the printer) and move it into position in the printer's frame.

(2) Using a 1/4" wrench, replace the two hex head thread forming screws and two flat washers to hold the motor in place. Tighten the screws securely.

(3) Arrange the two attached cables along their respective routings (as noted during removal) and secure the wire bundle with tie wraps. Plug the transducer cable into the J8 connector on the CAR SERVO board in slot C of the motherboard and plug the two power wires onto the B75 (blue wire) and C75 (red wire) connectors on the CAR PWR AMP board in slot D of the motherboard.

(4) Set the bottom plate back into position, and replace the four fastening screws using a TORX T15 screwdriver to tighten them. Set the printer back down on its feet.

(5) Study the carriage drive cable arrangement shown in Figure 3-16. Assemble an O-ring, cable hub, lockwasher, and locknut on the end of the replacement carriage drive cables. Screw the nut onto the cable shank far enough to allow two threads to show on the free side of the nut. Hold the cable shank securely with a wrench while driving the nut on, to avoid twisting the cable.

(6) Insert the ball end of this cable through the cable hole in the right side frame. Engage the cable's ball into the notch on the outside rim of the servo motor capstan.

(7) Hold a slight tension on the cable, and turn the capstan CCW (viewed from the printer's front) to wind on almost all of the cable (slightly more than four complete turns).

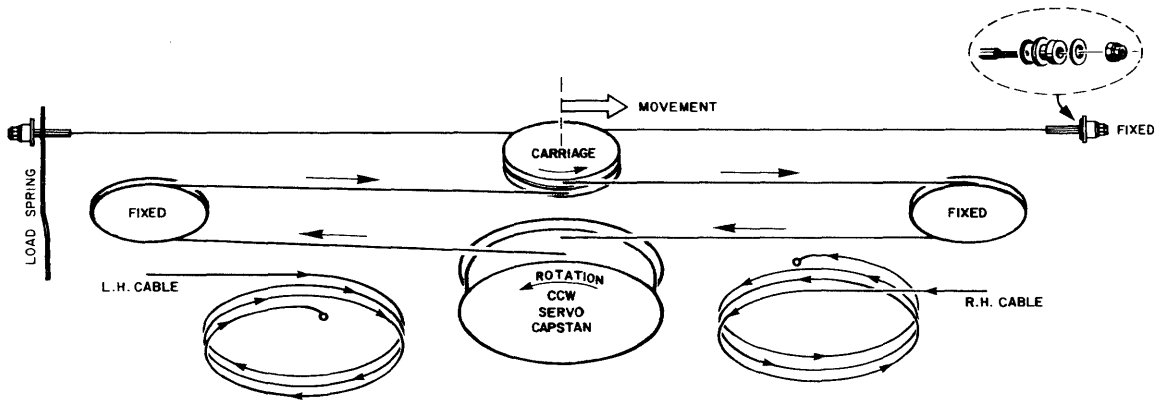


Figure 3-16. Carriage Drive Cable Routing

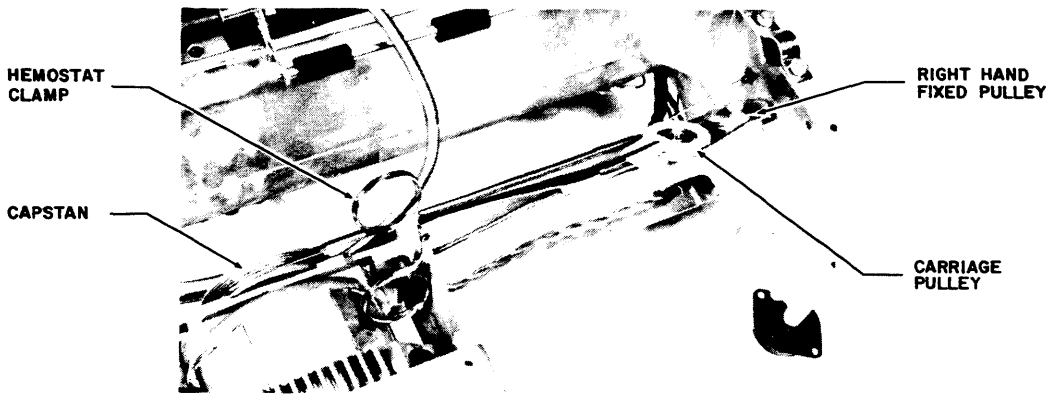


Figure 3-17. Right-Hand Carriage Drive Cable Installation

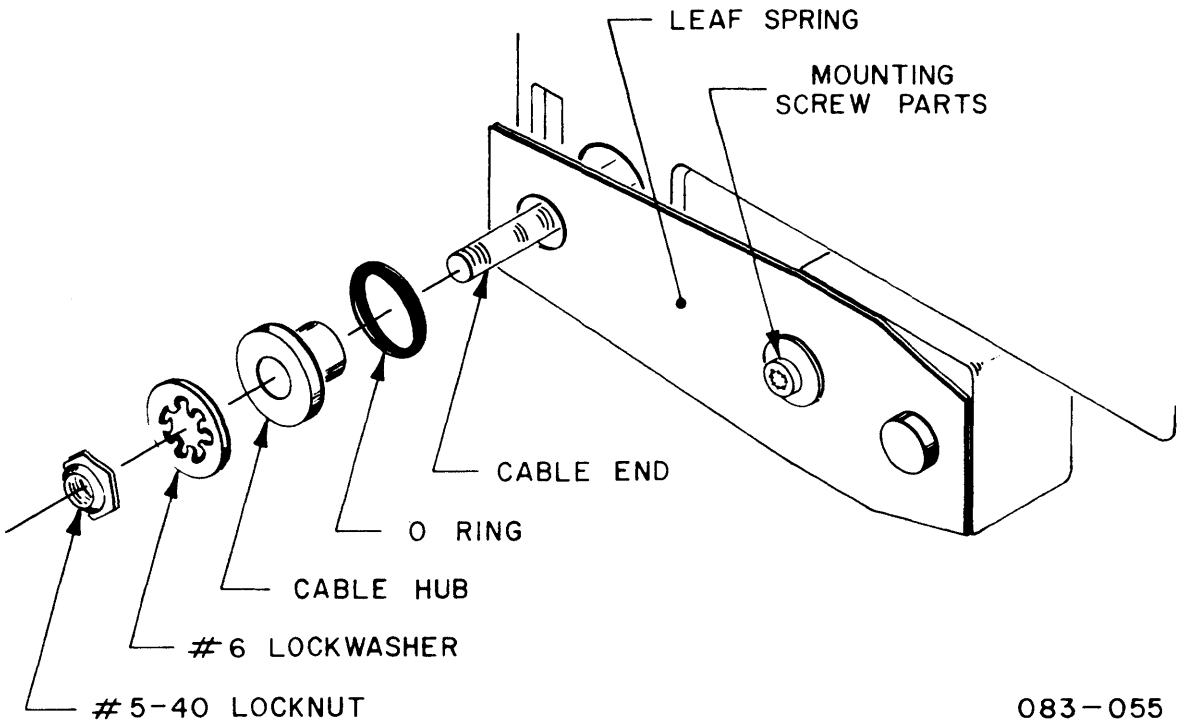


Figure 3-18. Carriage Drive Cable Tension Spring Assembly

(8) Refer to Figure 3-17. From the capstan, arrange the cable back to the right around the right side pulley CW (bottom rear to front top), and to the left and CW (front to back) around the carriage drive pulley, with the cable in the drive pulley's upper groove. It will be necessary to allow the capstan to rotate slightly.

(9) Protect the carriage drive pulley with heavy paper, and grasp it with a hemostat clamp as shown in Figure 3-17. Hook the hemostat clamp's lower finger ring over the main frame servo motor shield as shown, where the motor's magnetism will help to hold it in position. Rotate the capstan CCW to keep a slight tension on the cable, and to locate the notch on the capstan's inside rim (closest to the motor) as near the top as possible.

(10) Place the ball end of the second cable between the capstan and the main frame at the lowest point of the capstan (the ball will not fit between the capstan and the main frame at any other point). Pull the cable up until the ball can be inserted into the notch on the capstan's inside rim and insert the ball into the notch. Run the cable directly over to the left side pulley. There should be no more than 1/4 turn of this cable on the capstan.

(11) Arrange the cable around the left side pulley CCW (bottom rear to top front), and back to the right. Carefully route the cable CCW (front to back and back to left) around the carriage pulley in the lower slot of the pulley. Stretch the cable to the left, and thread its free end out through the cable hole in the left side frame.

(12) Assemble the hardware items on the free end of the cable, as it protrudes beyond the side of the frame, in the order shown in Figure 3-18. Put the locknut on finger tight only, and avoid twisting the cable.

(13) Refer to Figure 3-18. Mount the leaf spring onto the side frame with the screw, flat washer, and lockwasher. Use a TORX T15 screwdriver to tighten the screw down slightly and apply a light spring tension on the cables.

(14) Insert the small end of the TORX screwdriver down through the hub of the carriage drive pulley; this prevents the pulley from flipping over and releasing the drive cables. Carefully release the hemostat clamp. Holding the TORX screwdriver handle upright, gently rotate the drive capstan CW to move the carriage pulley left, to a position just to the right of the carriage servo motor, where the pulley hub is accessible up through the bottom alongside the motor. Install the hemostat clamp (with heavy paper protector for the pulley) as shown in Figure 3-13b, and remove the TORX screwdriver.

(15) Place the spacer [removed in step (4) above] on top of the carriage drive pulley with the shoulder extending down into the center of the pulley. Position the carriage subassembly over the clamped carriage drive pulley, and insert the shoulder screw through the pulley and spacer, and into the mounting hole on the carriage. Using a TORX T15 screwdriver, tighten down the shoulder screw and remove the hemostat clamp.

(16) Perform the printer adjustments described in section 3.4.1.

(17) Reinstall the printer into the bottom cover (see 3.3.5).

(18) Replace the top cover and accessories (see 3.1.2).

(19) Apply power and test the HyTerm carriage movement while printing.

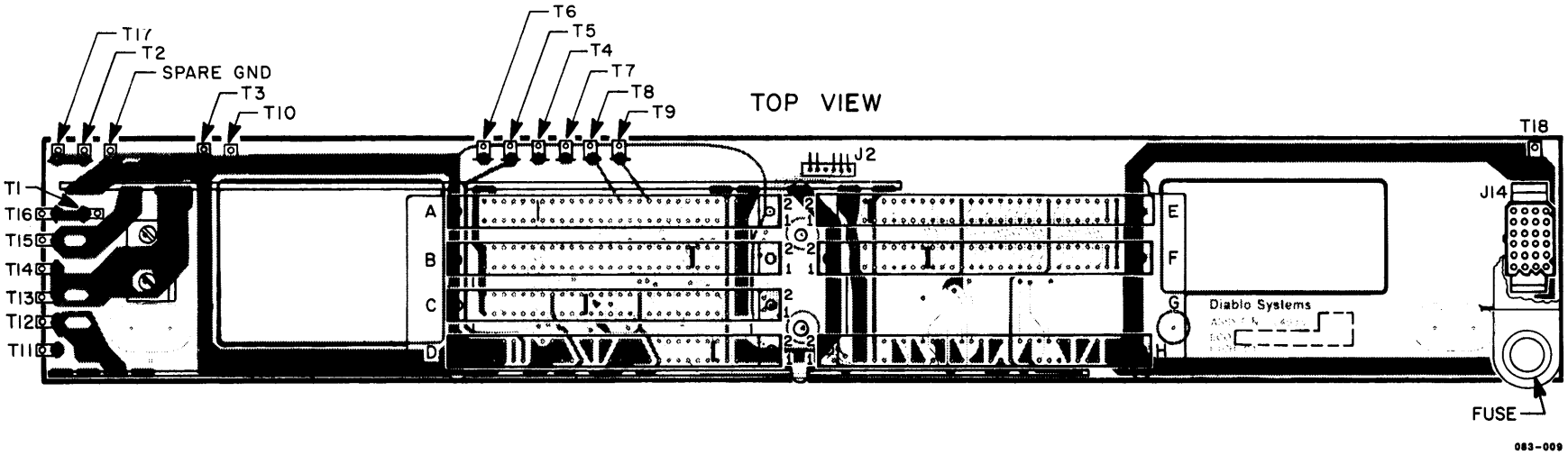


Figure 3-19. Mother Board Connections

3.3.11 Mother Board

REMOVAL

(1) Turn the power off and unplug the power cord from the ac outlet.

(2) Remove the top cover and accessories (see 3.1.2).

(3) Remove the printer from the bottom cover (see 3.3.5).

(4) Using a nut driver, remove the circuit board clamp; disconnect and remove all the circuit boards.

(5) Stand the printer up on the front of its main frame, with the bottom facing front (toward you).

(6) Disconnect the Molex plug from the mother board located at the left side frame (the right side as you view it).

(7) Using a TORX T15 screwdriver, remove the two rear shock mounts from the printer.

(8) Using a TORX T15 screwdriver, remove the two mother board mounting bracket screws from the right-side frame and three from the left-side frame. Remove the remaining six mounting screws from the bottom center of the mother board.

(9) Carefully flip the mother board over to expose the circuit board sockets and wire connections. Disconnect all the wire connections from the mother board and cut the necessary tie wraps to free the mother board.

REPLACEMENT

(1) Refer to Figure 3-19. Connect all wire and cable connections to the mother board and replace the necessary tie wraps.

(2) Set the mother board in place and check that all wires and cables clear the mother board and frame, and are arranged properly to reach their respective connections.

(3) Using a TORX T15 screwdriver, install the six bottom center mother board mounting screws, then the three left-side frame and the two right-side frame mounting bracket screws (a cable clamp is installed on one of the left-side frame mounting bracket screws). Tighten down all the mounting screws.

(4) Using a TORX T15 screwdriver, install the two rear printer shock mounts.

(5) Connect the Molex connector at the left-side frame to its mate on the mother board.

(6) Place the printer back down on its feet and install and connect all the circuit boards and their wire and cable connections.

(7) Reinstall the printer into the bottom cover (see 3.3.5).

(8) Replace the top cover and accessories (see 3.1.2).

(9) Apply power and test the HyTerm.

3.4 ADJUSTMENTS

The HyTerm seldom requires readjustment due to ordinary wear, and no adjustments should be attempted unless a malfunction indicates a specific need. But readjustment is routinely required whenever any of the following components or subassemblies are changed, or where adjustments are distributed to facilitate other maintenance:

(1)	Print Head	(6)	Ribbon Drive System
(2)	Paper Carrier Subassembly	(7)	Paper Clamp
(3)	Paper Feed Motor	(8)	Bottom Feed Paper Chute (option)
(4)	Carriage Subassembly	(9)	Cover-Open Switch
(5)	Carriage Drive System	(10)	Paper-Out Switch

Only the control panel's Alarm Volume adjustment can be performed at will, without affecting operation or other adjustments.

3.4.1 Printer Quality Testing

3.4.1.1 Print Registration

1. Column Registration: The maximum deviation between identical characters in the same column is .010 inch (.254mm) when printing in one direction; .020 inch (.508mm) when printing bidirectional.

2. Line Registration: The maximum deviation between identical characters in the same line is .010 inch (.254mm). [Does not apply to first character of a line.]

NOTE

Test methods for the above are totally related to the proper alignment and handling of the paper or form used.

3.4.1.2 Print Quality Test

The print quality test below is a method of testing the printer for possible misalignment. But print quality is not attributed to printer alignment alone. Paper thickness, number of copies, the condition of the ribbon, and the position of the Platen Adjust Lever all affect print quality as does the condition to the print head, the straightness of the carriage rails, and the roundness of the platen. Therefore, proper assessment of print quality requires that print samples for evaluation be obtained under standardized conditions. Tests should be made using a new ribbon cartridge on a good grade of bond paper with the Platen Adjust Lever in the second (from the front) detent position.

1. Prepare the printer as described above. (Install a new ribbon cartridge and one sheet of bond paper; set the Platen Adjust Lever to the second detent from the front.)

2. Power up and print a few lines of random characters to allow the ribbon cartridge to stablize.

3. Print a full (132 character) line across the page that includes several of the following characters: upper-case E, F, T, Z, and lower-case g, j, p, q, and the underscore.

4. Observe the print sample for clear character recognition and uniform character intensity across the entire print line. Observe the characters for uniform dot density (or character fill) and edge definition (see Figure 3-20) within a maximum dot edge variation of .003 inch (.076 mm).

The following conditions are indicators of possible printer misalignment:

* Characters are too light or too dark.
* Characters with flat tops (E, F, T, and Z) are faded or lighter along the top edges.
* Characters extending below the print line (g, j, q, and the underscore) are faded or lighter along the bottom edge.
* Characters are light or spotty at one end of the print line when compared to the other end.
* Characters are light or spotty over the entire length of the print line.

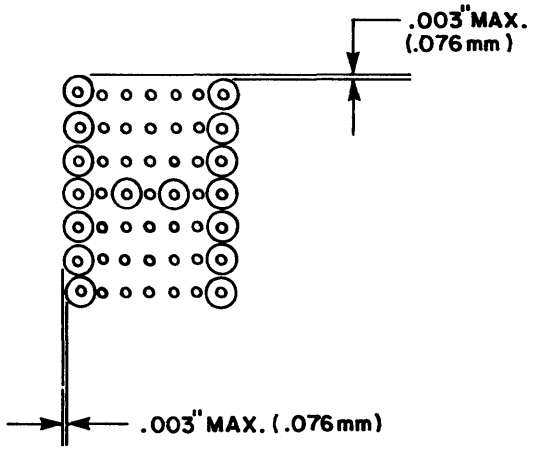


Figure 3-20. Dot Matrix Character Edge Variation

3.4.2 Printer Adjustments

Because some adjustments affect others, the printer adjustments should be performed in the sequence outlined in this section.

3.4.2.1 Carrier Assembly

1. Carrier Assembly Bias Shaft (A) : Check for axial movement of .001 inch (.025 mm) ±.0005 inch (.0127 mm). Adjust the position of the collar on the left end of the shaft as required to achieve this dimension.
2. Platen Position Torque Shaft (B) : Check that the set screws in the eccentric collars (C) at each end of this shaft are aligned vertically with each other when the Platen Adjust Lever (D) is fully forward (in first detent), and that the shaft end play is .001 inch (.025 mm) ±.0005 inch (.0127 mm). Adjust one or both eccentric end collars as required to achieve this dimension. Failure of eccentric collars to align as described indicates that the torque shaft is possibly twisted, in which case the proper lateral alignment of the platen will be impossible.
3. Move the Platen Adjust Lever (D) back and forth. A positive detenting force must be felt for each position. Adjust the detent plate (E) as required to achieve an even detenting action. The carrier assembly must move equally at both ends within .002 inch (.051 mm) in increments of .005 inch (.127 mm) ±.002 inch (.051 mm) between detent positions.

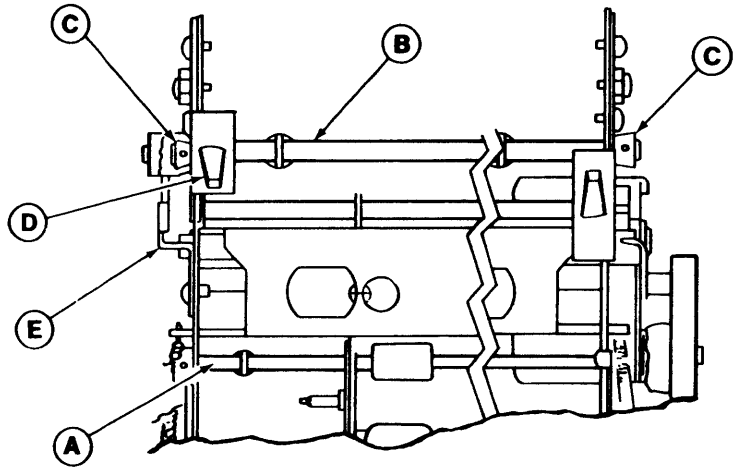


Figure 3-21. Carrier Assembly Adjustment Points

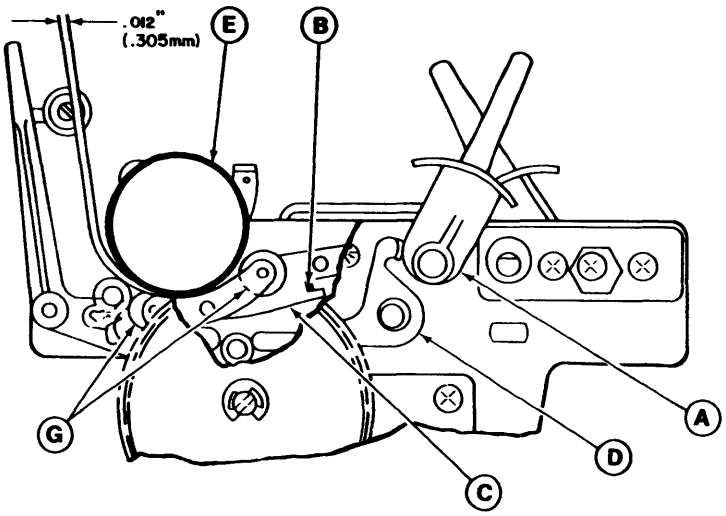


Figure 3-22. Paper Feed Adjustment Points

3.4.2.2 Paper Feed Assembly

Refer to Figure 3-22 for Paper Feed adjustment points.

With the Paper Release Lever (A) fully forward, the Paper Feed Rollers (G) must clear the Platen (E) by .08 inch (2.03 mm) minimum. The paper feed system may be adjusted as follows to achieve this and other goals:

1. Insert four sheets of standard forms paper (.012 inch or .305 mm) and move the paper release lever (A) fully rearward.
2. Ensure that the torque shaft arm tabs (B) are touching the lower edge of the feed roller support arm slots (C).
3. Ensure that the paper release actuator (D) is touching the ramp on the paper release lever (A). Loosen the actuator's set screw and adjust the actuator to achieve this condition, then retighten the set screw.
4. Remove the four sheets of paper, and insert one strip of paper 1 inch (25.4 mm) wide, or a .004 inch (.102 mm) shim, between the front paper feed rollers and the platen. Check that both platen and rollers rotate when the strip, or shim, is pulled free. Repeat for all rollers, front and rear. If no rotation occurs, the torque shaft arm Tabs B have been pushed down too low.

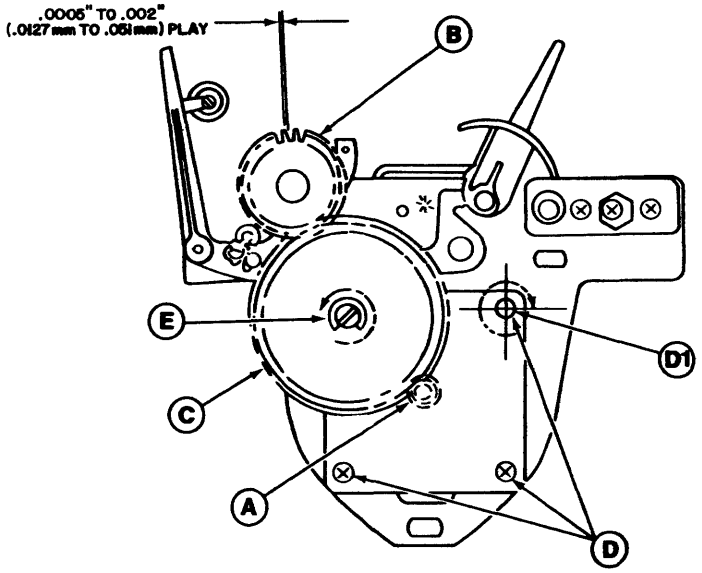


Figure 3-23. Platen Drive Adjustment Points

3.4.2.3 Platen Drive Assembly

Refer to Figure 3-23 for Platen Drive Assembly adjustments points.

With the paper feed motor drive gear (A) locked, platen drive gear (B) must have between .0005 inch (.0127 mm) minimum to .002 inch (.051 mm) maximum play, including idler gear (C).

1. Loosen the paper feed motor mounting screws (D), and remove the platen.
2. Locate the idler gear (C) and turn the eccentric (E) counterclockwise ONLY until a minimum backlash is obtained between gear (C) and motor gear (A). (Clockwise rotation of this eccentric will make proper installation of the platen impossible.)
3. Check the idler gear (C) for no binding effect for a full 360° of rotation.
4. Install the platen. Rotate the paper feed motor mounting plate around mounting screw (D1) to achieve the gear play dimenisions described above between gears (B) and (C). Tighten screws (D).

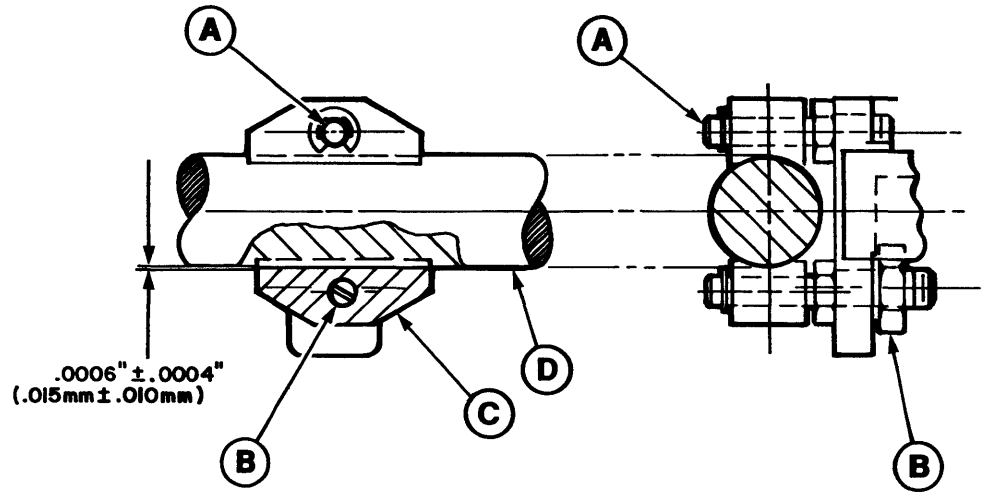


Figure 3-24. Front Guide Bearing Adjustment Points

3.4.2.4 Carriage Front Guide Bearing Assembly

Refer to Figure 3-24 for Carriage Front Guide Bearing adjustment points.

Under normal operating conditions and preventive maintenance activity, the carriage sliding bearings should not require corrective maintenance. All carriage assemblies including replacement units have their front bearings carefully adjusted at the factory, and should not require further post-installation adjustment in the field. Malfunction in this area, however, can effect carriage movement and print quality. If the carriage assembly is replaced for any reason, the front bearing should be checked for proper clearance and, if necessary, adjusted as follows:

1. Make sure the upper bearing stud (A) is firmly tightened.
2. Adjust the lower bearing eccentric (B) as required to achieve a clearance of .0006 inch (.015 mm) ±.0004 inch (.010 mm) between the lower bearing block (C) and the printer's front rail (D).
3. Test the bearing clearance at several points along the front rail to ensure that the rail has not become worn.
4. Tighten eccentric (B) and lubricate the rails (see 3.2.3.2.).

3.4.2.5 Platen-To-Print Head Adjustment

The Platen-to-Print Head adjustment is essential for optimum print quality. A special Platen-to-Print Head Adjustment Tool (Diablo No. 24708) must be used along with the following procedure:

1. Remove the print head from the carriage assembly (see 3.3.6).
2. Install the Platen-to-Print Head tool onto the carriage assembly as shown in Figure 3-25. The tool is correctly aligned for use when its two mounting thumbscrews have been threaded in smoothly, completely, and are finger tight.

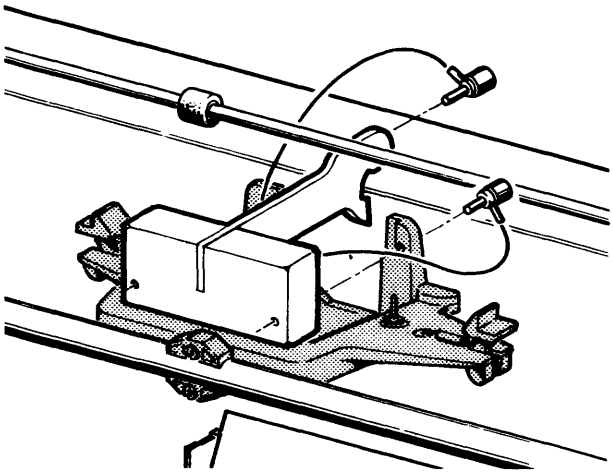


Figure 3-25. Platen-To-Print Head Adjustment Tool Installation

Refer to Figure 3-26 for Platen-to-Print Head adjustment points.

3. Loosen the front eccentric lockbolt A on each side of the printer, and orient the eccentrics as shown.

4. Loosen the two rear eccentric clamp screws on each side of the printer with a TORX T15 screwdriver, then loosen the rear eccentric clamp bolt B on each side of the printer.

5. Slide the carriage from end to end, stopping at several points to rotate the platen while checking the tool-to-platen clearances. Check for an average of .010 inch (.254 mm) ±.001 inch (.025 mm) clearance between the platen surface and the tool face 'A'.

6. Adjust <u>both</u> rear eccentrics as required to achieve this goal. Tighten the two clamp screws on each side of the printer and recheck the clearance to ensure nothing has moved out of adjustment. Tighten the eccentric lockbolts B on each side of the printer.

7. Slide the carriage from end to end, stopping at several points to rotate the platen while checking the tool-to-platen clearances. Check for an average of .010 inch (.254 mm) ±.001 inch (.025 mm) clearance between the platen surface and the tool face 'B'. Adjust <u>both</u> front eccentrics as required to achieve this goal. Hold each adjusted eccentric with a 7/16" wrench while tightening its lockbolt. Recheck the clearances to ensure nothing has moved out of adjustment.

8. Remove the tool and reinstall the print head (see 3.3.6).

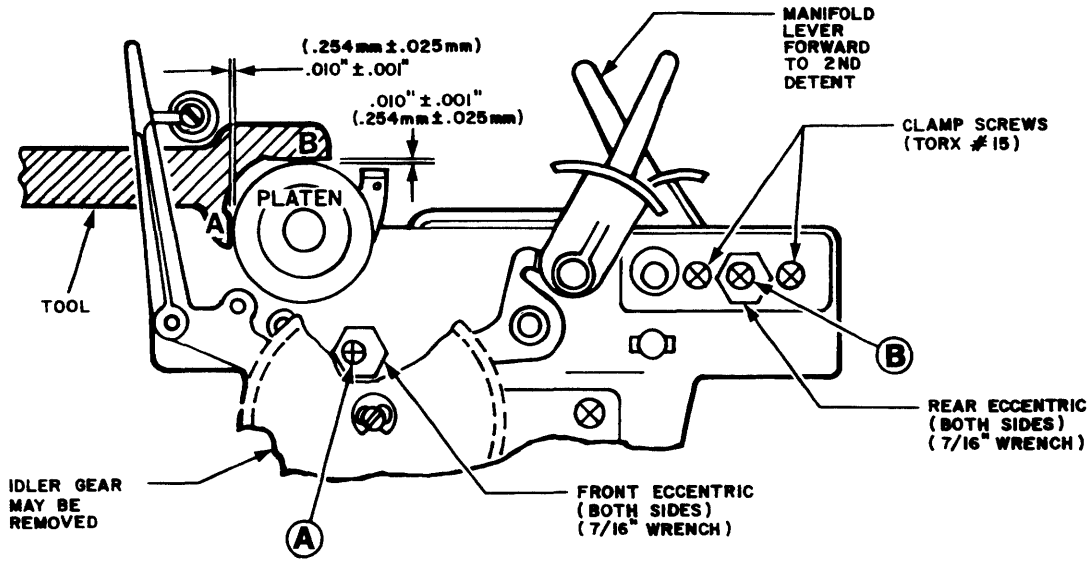


Figure 3-26. Platen-To-Print Head Adjustment Points

3.4.2.6 Variable Adjust Platen Knob's End Play Adjustment

The variable adjust (right hand) platen knob's end play must not exceed .002 inch (.051mm) maximum.

Refer to Figure 3-27 for the variable adjust platen knob's end play adjustment.

1. Loosen the set screws in the platen release gear hub (A) and adjust the hub to achieve the desired clearance.
2. Retighten the set screws in the platen release gear hub.

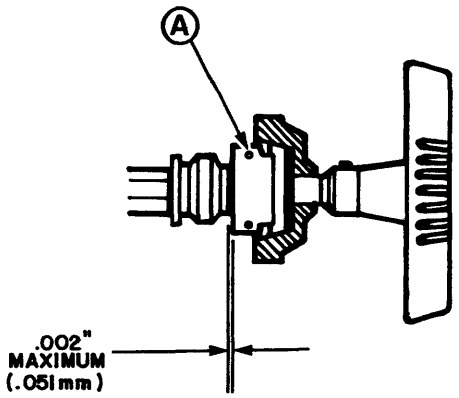


Figure 3-27. Variable Adjust Platen Knob's End Play Adjustment

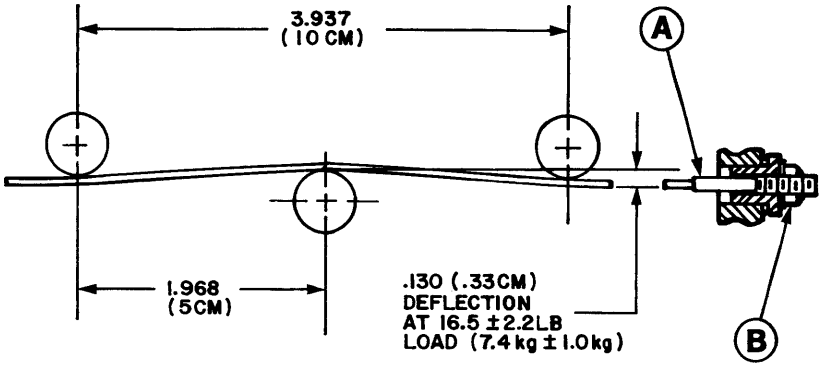


Figure 3-28. Carriage Drive Cable Adjustment

3.4.2.7 Carriage Drive Cable Adjustment

Refer to Figure 3-28 for Carriage Drive Cable adjustments.

With the carriage positioned against the right-hand stop, check the cable tension midway along the exposed cable for a force of 16.5 lbs ± 2.2 lbs (7.4 kg ± 1.0 kg) necessary to distort the cable as shown.

NOTE

If the Tensionmeter listed under tools at the front of this section is not used, the dimensions between force points shown must be carefully followed.

1. Adjust cable tension by tightening or loosening cable tension nut B while holding the square cable shank A from turning.
2. After adjusting the nut B , move the carriage back and forth several times to redistribute cable tension, and recheck. Use Loctite on nut B after adjustment has been completed.

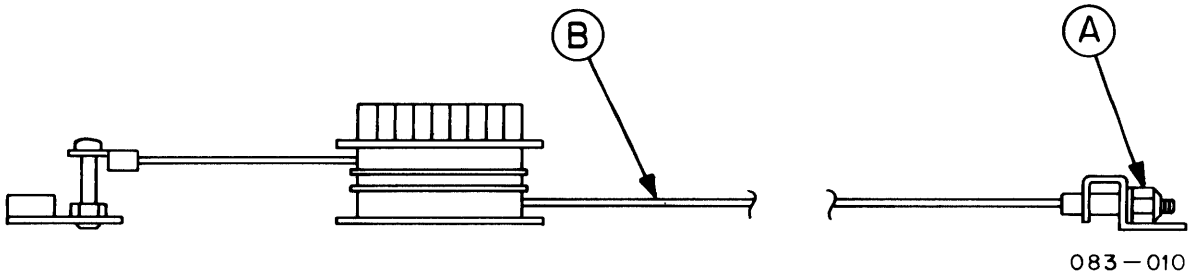


Figure 3-29. Ribbon Drive Cable Adjustment

3.4.2.8 Ribbon Drive Cable Adjustment

Refer to Figure 3-29 for Ribbon Drive Cable adjustment.

The Ribbon Drive Cable tension must be adjusted to provide adequate drive while not unduly impeding carriage motion or straining the cable. To adjust the cable, start with a properly lubricated carriage, then install a ribbon cartridge and proceed as follows:

1. Move the carriage back and forth slowly at least 6 inches (15.24 cm) each way from machine centerline while tightening the cable locknut A on the right end of cable B .
2. Tighten slowly until the ribbon drive is observed to rotate without slipping during a full carriage motion. Then add 1/2 to 3/4 turn (180° to 270°) to locknut A .

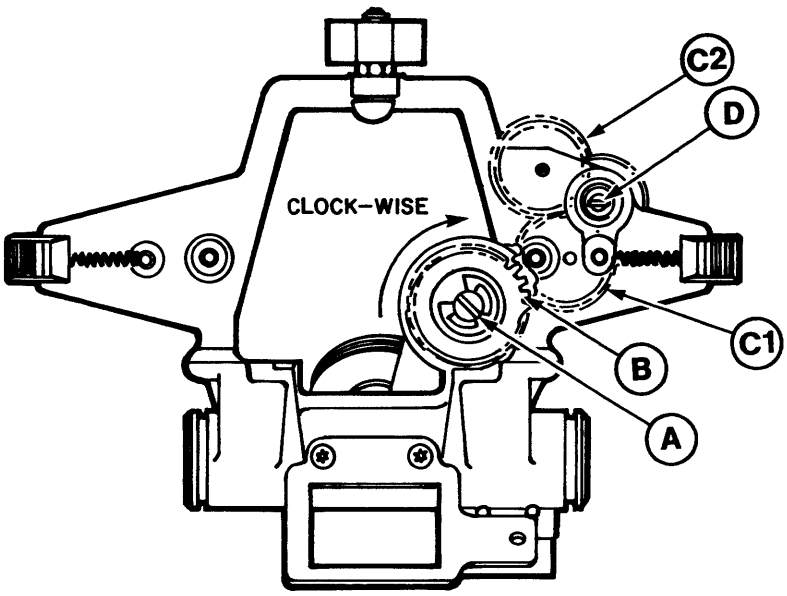


Figure 3-30. Ribbon Drive Gear Adjustment

3.4.2.9 Ribbon Drive Gear Adjustment

Refer to Figure 3-30 for Ribbon Drive Gear adjustments.

The Ribbon Drive system includes two opposing spring clutch gears ((C1) and (C2)) driving a ribbon capstain (D) , and being driven from a cable pulley gear (B) . The system backlash is adjusted as follows:

1. Hold clutch gear (C2) stationary.
2. Rotate the eccentric mounting screw (A) of cable pulley gear (B) clockwise ONLY to achieve a .003 inch (.08 mm) ±.002 inch (.05 mm) backlash between pulley (B) and clutch gear (C1) .
3. Move the carriage from side to side and check for a full 360° of clockwise rotation of ribbon capstan (D) without evidence of binding or slippage.

3.4.2.10 Paper Clamp Adjustment

Refer to Figure 3-31 for Paper Clamp adjustments.

The Paper Clamp extends the full length of the platen, and is held in place by the two rear carriage rail clamp's rear hold-down screws. The Paper Clamp assembly will seldom require adjustment, except when the rear carriage rail has been removed and replaced. To adjust, proceed as follows:

1. Loosen the two rear mounting screws (A) from the rear carriage rail clamps at each end of the carriage rail (B).
2. Push the paper clamp assembly (C) back toward the platen (D) as far as it will go and retighten the screws (A).

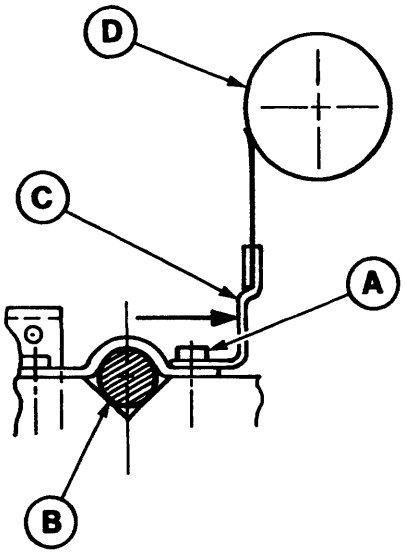


Figure 3-31. Paper Clamp Adjustment

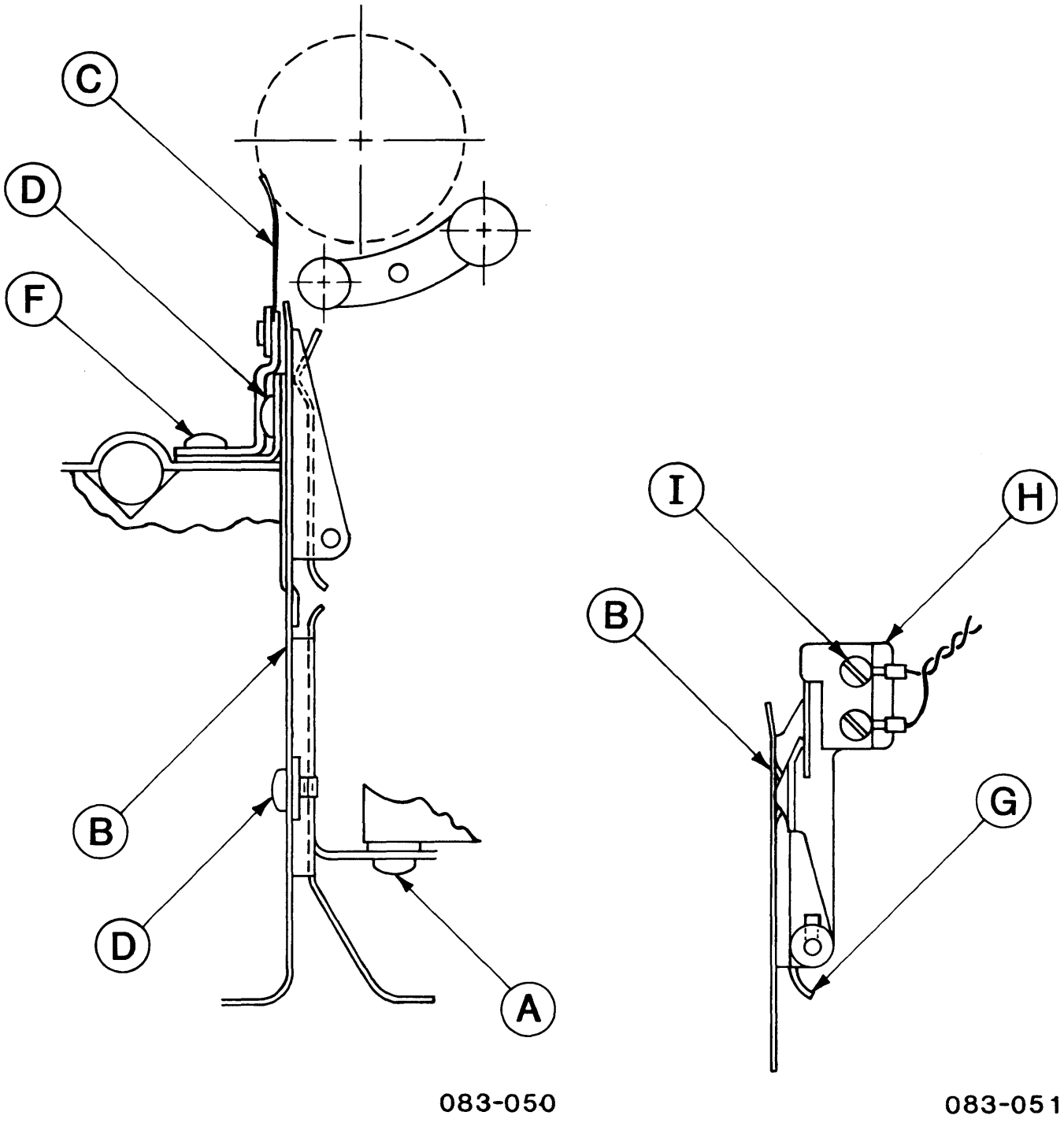


Figure 3-32. Bottom Feed Paper Chute Adjustment

3.4.2.11 Bottom Feed Paper Chute Adjustment

Refer to Figure 3-32 for Bottom Feed Paper Chute adjustments.

The Bottom Feed Paper Chute is an optional feature, not found on all HyTerms. Its use requires that a forms tractor be used along with the standard friction-feed platen. To properly adjust the paper chute, proceed as follows:

1. Make sure the following adjustments are correct before adjusting the bottom feed paper chute:
   (a) Platen-To-Print Head (see 3.4.2.5).
   (b) Paper-Feed Assembly (see 3.4.2.2).
2. Remove the Paper Clamp (C), and replace its rail clamp mounting screws (F) finger tight. Loosen all other screws except those holding the paper chute's bottom flanges (A).
3. Move the paper release and platen adjust levers fully forward.
4. Adjust the paper chute (B) down as low as possible, tighten the four forward facing screws (D). See Figure 3-32a.
5. Remove screws (F).
6. Install paper clamp (C), adjust paper clamp and paper chute back toward the platen as far as possible. Tighten screws (F). See Figure 3-32a.
7. Adjust the dimples of the paper out bail (G) to touch the front paper chute (B) at both ends. Tighten set screws located in hubs at each end of paper out bail (G). See Figure 3-32b.
8. Adjust micro switch (H) to just reset .025 - .040 inch before dimples of paper out bail (G) touch front paper chute (B). Tighten screws (I). See Figure 3-32b. Bail minimum movement should be .100 inch at tangent of dimples. If not, form switch arm and readjust the switch per step 7. Note: Bail must move freely.

3.4.3 Control Panel Alarm Volume Adjustment

Refer to Figure 3-33 for the Control Panel Volume Adjustment.

There is a potentiometer on the control panel that can be adjusted to change the Alarm buzzer volume. To adjust, proceed as follows:

1. Remove access cover to expose the switch portion tof the control panel.

2. Using a small blade screwdriver, adjust the Alarm buzzer volume control potentiometer until the desired volume is obtained. To test the alarm after each adjustment, depress the RESET keyswitch on the keyboard and then attempt to print a character (Cover-Open error will occur).

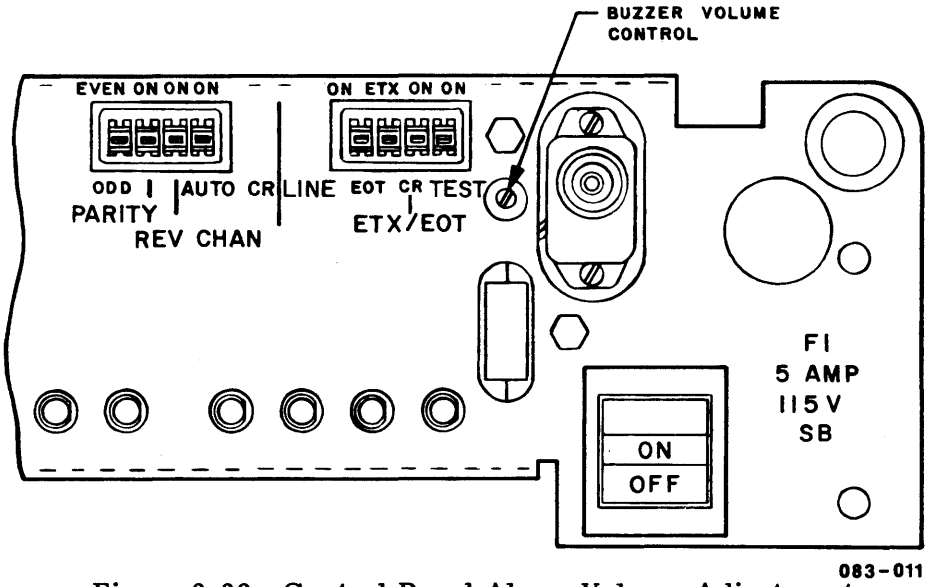


Figure 3-33. Control Panel Alarm Volume Adjustment

3.4.4 Power Supply Adjustment

Adjustment of the power supply should not normally be required unless power supply components have been replaced. Proper adjustment of the power supply requires use of a variable load, so these adjustments should not be attempted in the field. It is recommended that power supply adjustment problems be referred to the nearest Diablo service depot. The following information is provided for Diablo service depot personnel.

NOTE

For locations of the various potentiometers mentioned in the following procedures, refer to the assembly drawing following schematic no. 400062-XX in the schematics/reference section.

All output readings should be taken with a digital voltmeter.

3.4.4.1 Overvoltage Protection

Disconnect the power supply outputs from the terminal and connect a dummy load to the +5V output which draws approximately 1 amp. While monitoring the +5V output, adjust pot R22 clockwise and note the maximum voltage obtainable (after which the overvoltage circuit takes over and causes the output to drop). This should be between +5.5V and +6.3V, preferable around +6.0V. Adjust pot R23 on the control module (the small circuit board attached to the power supply's main circuit board) clockwise to trigger the overvoltage circuit at a highter point, or counterclockwise for a lower point.

NOTE

If the putput reaches +6.3V before triggering the OVP circuit, the SCR "crowbar" circuit may trigger, requiring removal of input power before the power supply can restart. If this occurs, turn off power, turn pots R23 on the control module and R22 both counterclockwise slightly, restore power, and continue the test as described.

3.4.4.2 Current Limit

This adjustment should be made with the input voltage at a nominal value--not at either of its extremes. This is, the input voltage should be as close to 115V (or 230V) as possible. This adjustment also requires that the outputs be loaded so that the power supply delivers about 320 watts of total power.

CAUTION

Maintain this power level for no longer than 30 seconds while making this adjustment.

Adjust pot R19 until the output begins to drop off at the 320 watts total power point.

3.4.4.3 Output Voltage

With the power supply connected to the terminal, adjust pot R22 to obtain +5.0V +1V, at Mother Board connector T15 (refer to Figure 3-19). Check the +15V, -15V and +48V readings at Mother Board connectors T15, T11, and T18, respectively. If these readings are not within $\pm$ 5%, some problem exists and must be corrected before proper adjustment can be made.

NOTE

The power supply must be connected to the terminal for this adjustment. Accurate adjustment cannot be make without a proper connected to the +5 output.

3.4.5 Cover-Open Switch Adjustment

Before attempting an adjustment, be sure that the top cover fits the bottom cover properly, and that the access cover fits the top cover properly, and is tight. Adjust and/or from the access cover clamp springs (replace if necessary) to tighten the access cover. If switch adjustment is still necessary, proceed as follows:

For a minor adjustment, form the small protrusion on the bracket inside the bottom center of the access cover. If further adjustment is necessary, it may be necessary to shift the entire bracket up or down slightly. Check the adjustment by making sure the switch operates each time the access cover is opened or closed.

3.4.6 Paper-Out Switch Adjustment

This switch is functional only when a forms tractor or pin-feed platen is used. When a friction-feed platen is used (without forms tractor), the switch is held in its nonoperated (paper in) position by the paper release lever's being in its rearward position. When the paper release lever is moved to its forward position, the switch operating mechanism is unlocked and allowed to sense the paper-out condition.

Before starting this adjustment, make sure that the Platen-To-Print Head adjustment (see 3.4.2.5) and the Paper Feed Assembly adjustments (see 3.4.2.2) are correct. Perform the adjustment with the platen installed and the paper release lever in its rearward position (pressure applied).

Refer to Figure 3-34 for Paper-Out switch adjustment, and proceed as follows:

(1) Using a .050 inch Allen setscrew wrench, loosen the setscrew 1 in the bell crank on the end of the paper-out bail pivot shaft 2 . The front edge of the bail should touch the platen surface squarely within .003 inch (.08 mm). A gap of .010 inch (.25 mm) maximum due to bowed paper-out bail is permissible. If necessary to adjust, loosen the setscrew 3 at either end (or both), adjust, and tighten the screw(s).

(2) Loosen the switch mounting screws 4 , and adjust the switch to transfer when the bail is .010-.020 inch (.2-.5 mm) away from the platen. Tighten the screws.

(3) Move the bail back away from the platen fully. The bail legs must bottom against the printer "comb" frame, and not against the switch. If necessary, form the switch arm to allow the switch to transfer sooner, and reposition the switch to obtain the proper adjustment as noted in step (2).

(4) Remove the platen, and move the bail rearward until its legs come within .030 inch (.76 mm) of the comb. Hold the bail in this position and rotate bellcrank 5 until its ear 6 rests against the actuator lever arm 7 . Tighten setscrew 1 . After tightening the screw, the shaft 2 should pivot freely with .005 inch (.13 mm) maximum end play. Install the platen, move the pressure release lever back and forth several times, and stop with the lever in the rearward position. There must be at least .090 inch (2.3 mm) clearance between the bail and the platen.

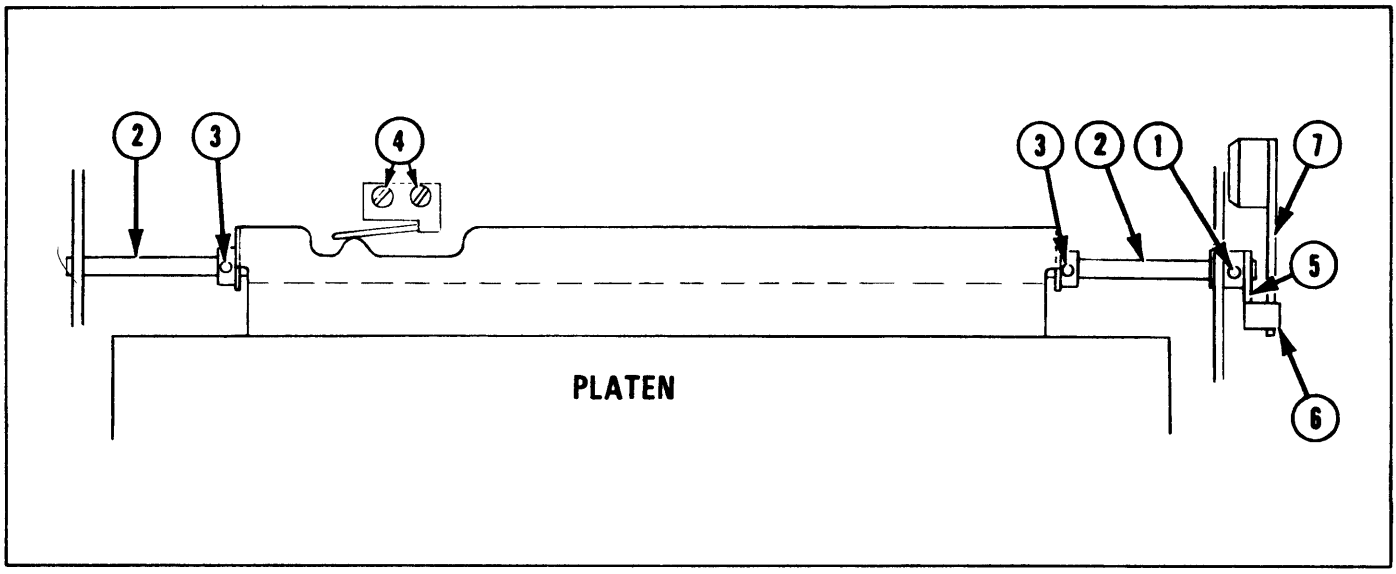


Figure 3-34. Paper-Out Switch Adjustment

3.5 COMPONENT IDENTIFICATION

There are two methods used to identify components within the terminal. The first is an extension of the reference designator system used to identify replaceable modules (Table 3-1). The second is a coordinate system used to identify components of the plug-in circuit boards. Also, closely related to component identification is the location of connectors and the numbering of connector pins.

3.5.1 Reference Designator System

The reference designator system is used to identify individual components mounted to the printer frame, as well as components on the control panel, in the power supply, and on the keyboard. Table 3-2 defines the class letters used on schematics and wiring diagrams to refer to various items. On the control panel and keyboard, the reference designators for each component are etched on the circuit board.

3.5.2 Coordinate System

Components are identified on the logic drawings as to type and location. The location information consists of a letter and a number, each representing coordinates on the circuit board. Refer to Figure 3-35. Letters are printed on the circuit board in the approximate center of the area they refer to, whereas numbers appear at the beginning of their respective area. As an example, to locate resistor E62, follow the "E" row horizontally to where it intersects the "60" column. Below the "60" and a little to the right (at "62") you will find resistor E62. Coordinates given for IC chips are the approximate location of pin no. 1. Coordinates for other "horizontally mounted" components (as in Figure 3-35) refer to the location of the leftmost lead.

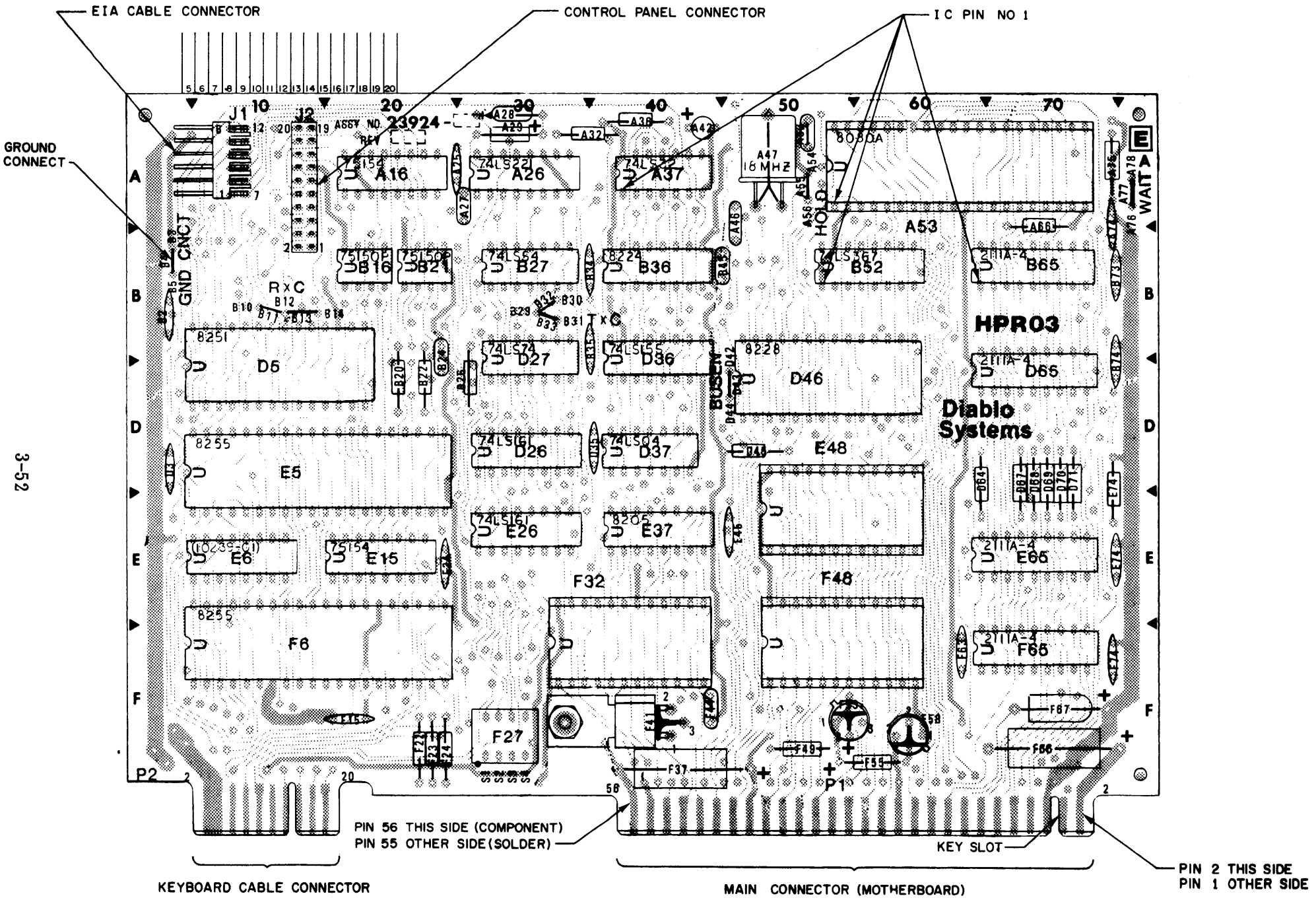


Figure 3-35. Circuit Board Component Location and Pin Numbering.

Table 3-2. Reference Designators

Designator	Description
A	Assembly
B	Fan (blower)
C	Capacitor
CR	Diode (including bridge rectifiers, LEDs)
DS	Alarm (buzzer)
E	Individual terminal
F	Fuse
FL	Filter
J	Jack (connector, stationary portion)
L	Inductor (coil)
P	Plug (connector, movable portion)
Q	Transistor
R	Resistor
RT	Resistor, temperature-sensitive (thermistor)
S	Switch
T	Transformer
TE	Terminal board
TP	Test point
U	Integrated circuit
VR	Voltage regulator (zener diode)
W	Cable
X	Circuit board socket, fuseholder

Letter coordinates for vertically mounted components that overlap usually refer to the row in which the largest portion of the component is located.

Pin no. 1 of each IC is easily identified from the bottom (solder) side of the board by its square solder pad. This lessens the chance of errors in counting pin numbers.

The mother board, the keyboard, and the control panel circuit boards do not use the coordinate system because of the small number of components involved. These boards use standard reference designators, which are silkscreened or etched onto the board, and referenced on the schematics.

3.5.3 Pin Numbering

Industry standards are followed for pin numbering of integrated circuits. Pin identification for all integrated circuits, including metal-can ICs, can be found in the Schematics/Reference Section.

3.5.3.1 Discrete Semiconductors

Pin identification for most discrete semiconductors is presented in Figure 3-36.

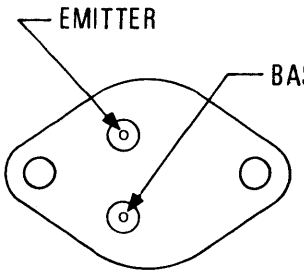
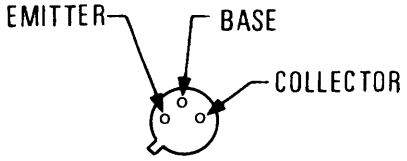
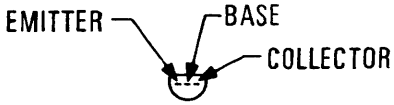
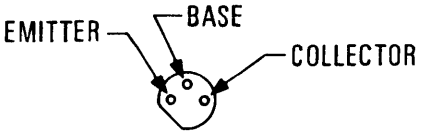
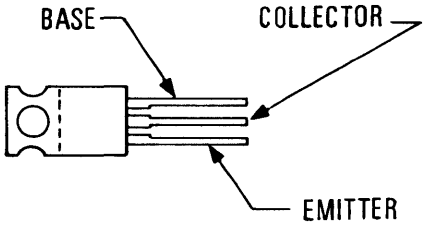
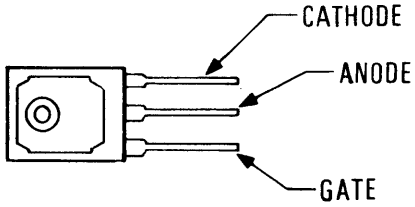
Outline (Bottom View)	Diablo Part Number	Industry Type Number
 (COLLECTOR CONNECTED TO CASE)	42190-29 42190-30 USE SJ7280 42190-71	SJ7280 SJ7280 (Matched Pair) 2N6303 (SJ7280) 2N6545
	10422-01 10443-01 10444-01	2N3725 2N5320 2N5322
	10105 42190-26 13013 42190-21 42190-28	2N3644 2N4126 2N4401 MPS-A43 MPS-A93 MPS5172 MPS6516
	10105	PN3644
	10177-02 10178-02 10445-01 13063 13064 42190-27 42190-70	TIP31A TIP32A 2N6103 TIP41A TIP42A TIP47 TIP49
 LED	42222-01 42222-02 14005-01	5082-4955 521-9203 MV5753
 SCR	42190-43	C122F (50316)

Figure 3-36. Semiconductor Lead Identification

NOTE

Components in Figure 3-36 that are listed by Diablo part number should not be replaced by standard industry types. They should be ordered by Diablo part number because in some cases there are more stringent tolerances for the Diablo parts, and restrictions as to approved manufacturers, due to reliability and functional differences.

3.5.3.2 Circuit Boards and Mother Board

Pin numbering of circuit boards that plug into the left-hand half of the terminal is shown in Figure 3-35. Circuit boards on the right side are mirror images, so pin no. 1 is on the left side; pin no. 56 on the right.

The numbering of all mother board pins is shown in Figure 3-37. Signal names for all points, including power connections are shown on schematic no. 24935-01.

3.4.3.3 Keyboard Cable

Pin numbers are shown in Figure 3-38. Pin numbers and signal names are the same at both ends. Odd-numbered pins are on the top (component side) of the keyboard and the back (solder side) of the HPRO board; even-numbered pins are on the bottom (solder side) of the keyboard and the front (component side) of the HPRO board. Signal names are listed in Table 3-3.

Table 3-3. Keyboard Signal Names

Pin No.	Signal Name
1	+5V
2	SIGNAL GND
3	+5V
4	SIGNAL GND
5	Unassigned
6	Unassigned
7	Unassigned
8	-POR
9	+BUSY (-READY)
10	Unassigned
11	-12V
12	-KYSTB
13	-DATAØ
14	-DATA7
15	-DATA6
16	-DATA1
17	-DATA5
18	-DATA2
19	-DATA4
20	-DATA3

Switch		Signal	
Designator	Name	Designator	Name
S3D	TEST	SW1	-SELF TEST
S3C	ETX/EOT (ON)	SW2	-ETX/EOT
S3B	ETX/EOT (ETX)	SW3	-ETX
S3A	LINE	SW4	-ON LINE
S2D	AUTO CR	SW5	-AUTO CR
S2C	REV. CHAN.	SW6	-REVERSE CHANNEL
S2B	PARITY (ON)	SW7	-PARITY ENABLE
S2A	PARITY (EVEN)	SW8	-EVEN PARITY
S1D	DUPLEX	SW9	-FULL DUPLEX
S1C	SPEED (120)	SW10	-1200 BAUD
S1B	SPEED (30)	SW11	-300 BAUD
S1A	PAPER OUT	SW12	-DEFEAT

Indicators	
LED 1 (CR9)	RIBBON
LED 2 (CR8)	ATTN
LED 3 (CR7)	PAPER
LED 4 (CR6)	⚠
LED 5 (CR5)	COVER
LED 6 (CR4)	OVFL
LED 7 (CR3)	PRINTER
LED 8 (CR2)	PARITY
LED 9 (CR10)	REC
LED 10 (CR11)	XMIT
LED 11 (CR12)	PROCEED

⚠ NOT DEFINED

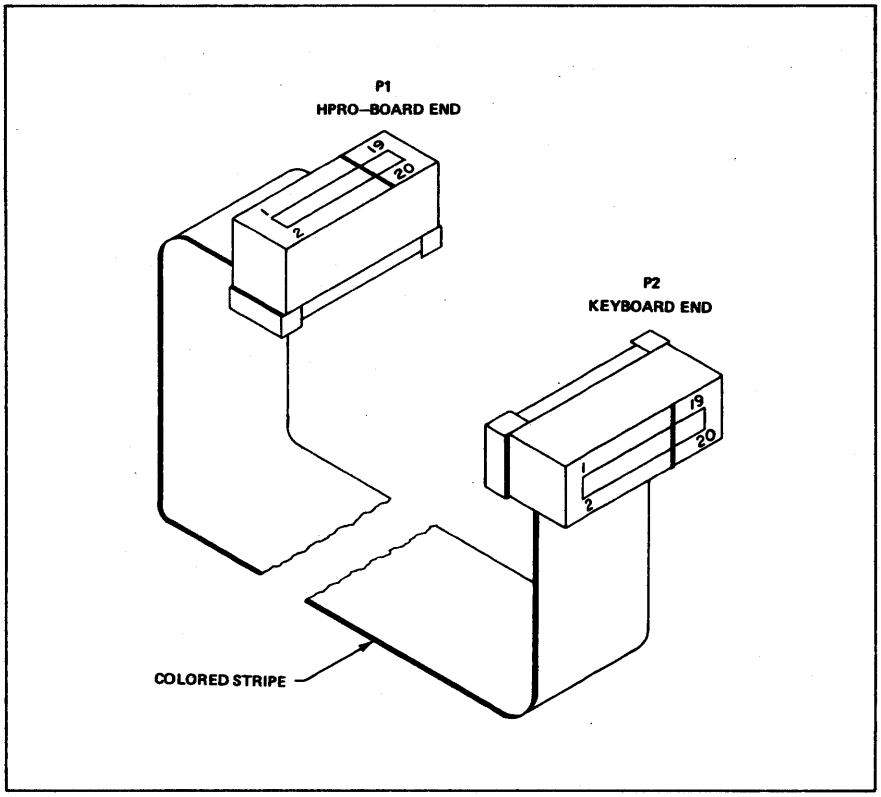


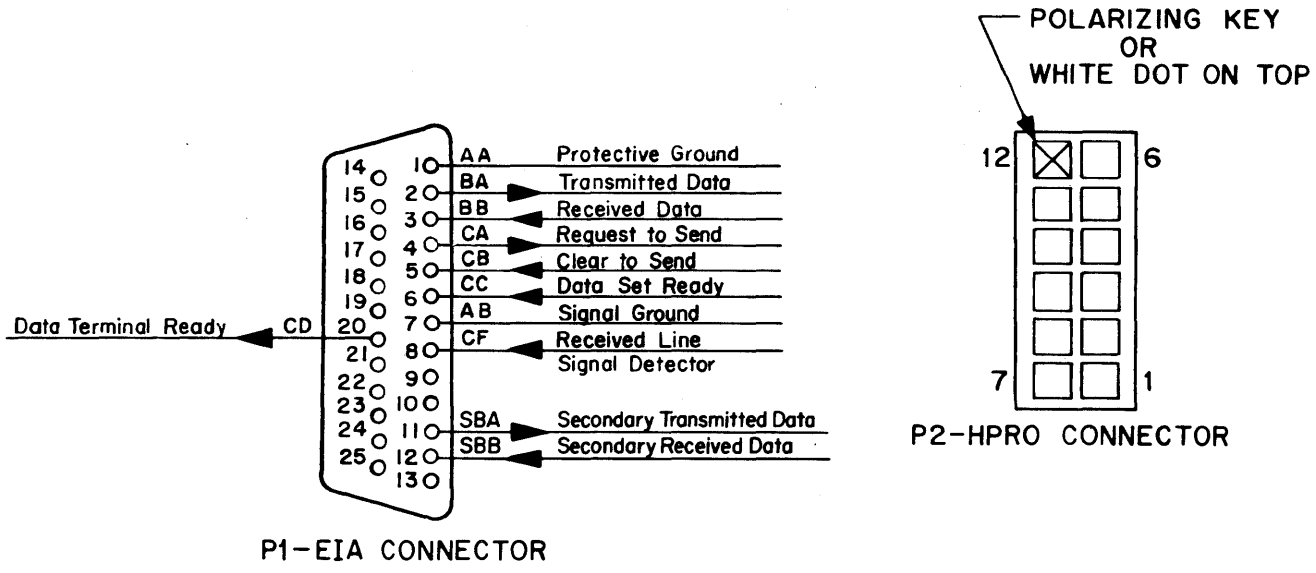
Figure 3-38. Keyboard Cable

3.5.3.4 Control Panel Cable

The control panel cable is permanently mounted to the control panel circuit board. The 20-conductor ribbon lead is terminated in a 20-pin female connector that plugs into J2 on the front surface of the HPRO board. The control panel schematic diagram (400056-01) shows witing of both the circuit board and the cable. The connector is similar in appearance to the connectors for the keyboard (Figure 3-38). Pin 1 is identified by a triangle on the connector and by the color stripe on the edge of the ribbon cable. Signal names for this cable are shown on the control panel schematic diagram and on the Signal Cable Interconnection Diagram No. 400089-01.

3.5.3.5 EIA Cable

Complete information on the wiring of the EIA cable is given in Figure 3-39. Note that the male EIA connector is shown; the female connector on the modem or acoustic coupler is a mirror image of this. Note also that the J1 connector on the HPRO board is a mirror image of the P2 connector shown.



WIRING LIST			
COLOR	P1	P2	
GREEN	1	6	
RED	2	5	
ORANGE	3	7	
YELLOW	4	4	
BROWN	5	9	
BLUE	6	8	
PURPLE	7	1	
WHITE	8	10	
BLACK	20	3	
SLATE	11	2	
PINK	12	11	
TAN	22	12	*

* NOT USED

083-054

Figure 3-39. EIA Cable Pin Identification

SECTION 4
SCHEMATICS AND REFERENCE INFORMATION

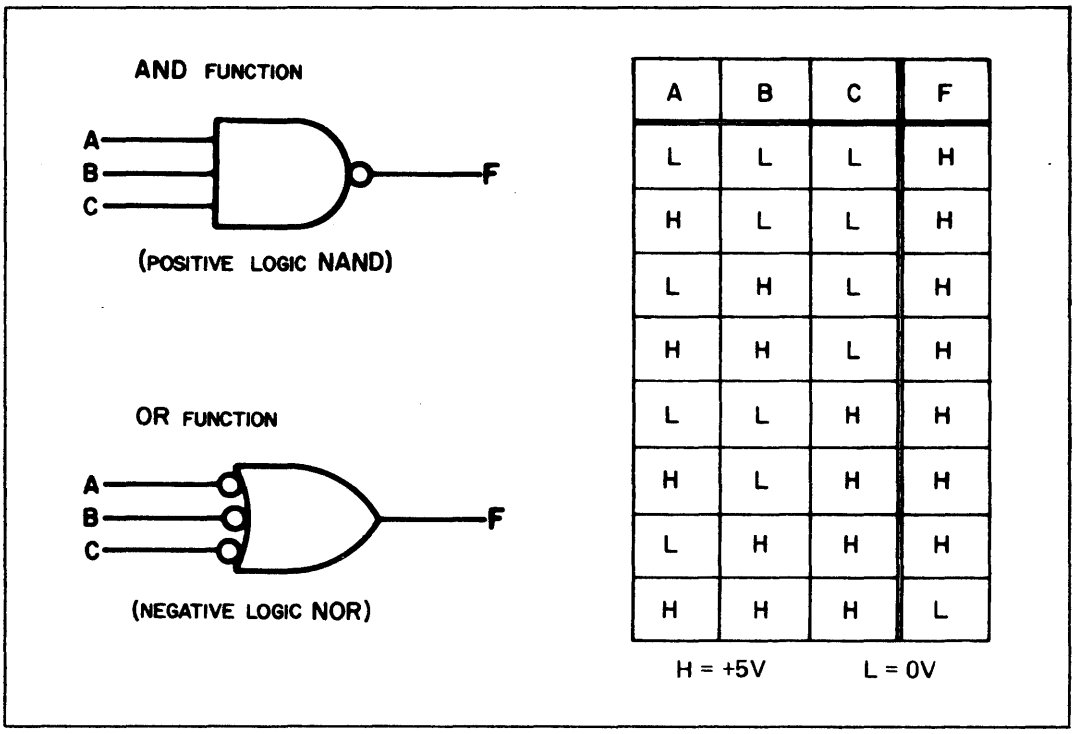
4.1 INTRODUCTION

This section contains information on logic symbology and drawing conventions used in the HyTerm schematics and logic diagrams, and information on the integrated circuits used.

4.2 FUNCTIONAL LOGIC

The HyTerm logic diagrams are troubleshooting aids for use by field service personnel. As such, the first responsibility of logic diagrams is to illustrate principles of operation. Diablo Systems logic diagrams, therefore, emphasize functions performed by logic elements, rather than the kinds of devices used to implement the functions.

For example, a NAND gate may appear on a logic diagram as either a positive AND function with the output inverted (NAND), or as a negative OR function with the inputs inverted (NOR). See Figure 4-1. This is contrary to some logic drawing standards, which require a NAND symbol for both functions. In Diablo Systems diagrams, different symbols are used to distinguish between the two functions because the functional elements are considered more relevant to design theory than symbolic representation of the devices used.



A	B	C	F
L	L	L	H
H	L	L	H
L	H	L	H
H	H	L	H
L	L	H	H
H	L	H	H
L	H	H	H
H	H	H	L

H = +5V L = 0V

Figure 4-1. Example of Functional Logic

4.3 SIGNAL NOMENCLATURE

The active level of each logic signal is assigned a descriptive name. A signal is considered active when it either causes or represents some logic event that is significant to the progress of an operation. Consequently, the name given a signal usually provides one of two kinds of functional information:

(1) Describes the effect that the signal's active level has on the logic it feeds; for example, -ENABLE INP allows data to be brought into the printer microprocessor.

(2) Represents a condition or event that develops elsewhere in the logic; for example -DBLE LINE FEED is the name of the signal that is active whenever the terminal microprocessor issues a Double Line Feed command to the printer microprocessor.

A plus sign (+) or a minus sign (-) generally precedes each signal name to identify which of the two voltage levels used in the logic system is considered to be that signal's active level. The + sign represents the relatively higher logic level and the - sign, the relatively lower level. (This means relatively higher or lower with respect to each other; the signs do not always indicate signal polarity with respect to ground.) For example, if -RESET is high (+5 volts), the Reset function is inactive. If +USART INTERRUPT is high, it means the USART has received a character from the data link and is ready to forward it to the MPU; if +USART INTERRUPT is low, it means the USART has not received any data from the data link that has not already been accepted by the MPU.

The actual voltage levels represented by the signs will depend on the logic family being used. For example, in TTL circuits, the signal identified by -RESET is active when it is at 0V (nominal) and inactive at +5V (nominal).

Sometimes a signal serves as the input to both positive logic and negative logic elements. Ordinarily in such cases, the sign preceding the signal name agrees with the active level indicated at the output of the logic element that produced the signal.

In the text, signal names are printed in capital letters to distinguish them from functions being performed. For example, '-RESET' refers to an actual signal name, whereas 'Reset' refers to the reset operation in general.

4.4 LOGIC SYMBOLOGY

The logic function symbols used in Diablo Systems logic diagrams conform closely to those set forth in MIL-STD-806. Most small scale integration (SSI) circuits are represented by function symbols. Medium scale integration (MSI) devices, such as shift registers and counters, may be represented by rectangles with functional labels.

Generally, a circle drawn at an input to a symbol indicates that the input is active when it is low (0V nominal). The absence of a circle at an input means that input is logically active when it is high (+5V nominal). The presence or absence of a circle at a symbol output has similar meanings for the active level of that output. Usually, all logic symbols are drawn with inputs on the left and outputs on the right. Symbols for all integrated circuits used are shown in the IC data contained in this section.

4.5 INTEGRATED CIRCUITS

Table 4-1 summarizes all integrated circuits used in the HyTerm. All of the ICs listed were used at some point in the HyTerm manufacturing process, but all will not be found in current production machines. Further IC data is contained in the following several pages arranged in the same order as listed in Table 4-1, which can be used as an index to data on a particular IC.

Table 4-1. Integrated Circuits

Digital:

Type	Description	Diablo Part No.
833	TTL Dual 4-Input Expander	42191-31
7400	TTL Quad 2-Input NAND Gate	10134
74LS00	Quad 2-Input NAND Gate, Low Power Schottky	13077
7402	TTL Quad 2-Input NOR Gate	10135
74LS02	NOR Gate, Low Power Schottky	42350-01
7404	TTL Hex Inverter	10136
74LS04	TTL Hex Inverter, Low Power Schottky	10209
7405	TTL Hex Inverter, Open Collector	13145
7406	TTL Hex Inverter Buffer/Driver	10460
74LS08	TTL Quad 2-Input AND Gate, Low Power Schottky	10210
7416	TTL Hex Inverter Buffer Driver	10390
7420	TTL Dual 4-Input NAND Gate	10125
7426	TTL Quad 2-Input NAND High-Voltage Interface Gate	10120
7432	TTL Quad 2-Input OR Gate	10302
74LS32	TTL Quad 2-Input OR Gate, Low Power Schottky	13082
74LS54	TTL 4-Wide AND-OR INVERT Gate, Low Power Schottky	42408-01
74LS74	TTL Dual D Flip-flop, Low Power Schottky	13085
7476	TTL Dual J-K Flip-flop, with Preset and Clear	10138
7486	TTL Quad 2-Input Exclusive OR Gate	10303
74LS123	TTL Dual Retriggerable One-Shot, Low Power Schottky	42313-01
74145	TTL BCD/Decimal Decoder/Driver	10172-29
74LS155	TTL Dual 2:4 Decoder, Low Power Schottky	13090
74LS161	TTL 4-Bit Synchronous Binary Counter, Low Power Schottky	13091
74175	TTL Quad D Flip-flop with Clear	10337
74193	TTL 4-Bit Synchronous Up/Down Counter with Dual Clock	10154
74195	TTL 4-Bit Parallel-Access Shift Register	10191
74259	TTL 8-Bit Addressable Latch	10339
74LS367	TTL Hex Bus Driver, Three-State, Low Power Schottky	13096
8080A	MOS 8-Bit Microprocessing Unit	42338
8205	TTL 3-Line to 8-Line Decoder	42335
8212	TTL 8-Bit I/O Port, Schottky	42337
8224	TTL Clock Generator/Driver, Schottky	10215
8228	TTL Bus Driver/System Controller, Schottky	42331
8251	MOS USART	42336
8255	Universal Communications Interface	42407-01
MM5873	Keyboard Decoder/Encoder	42191-33
SD 25010-K	Keyboard Decoder/Encoder	—
CPU11806	Microprocessor	13144

Interface:

Type	Description	Diablo Part No.
75150P	Dual Line Driver	10353
75154	Quad Line Receiver	10354
75451	Dual AND-Gate Peripheral Driver	10181

Table 4-1. Integrated Circuits (Continued)

Linear:

Type	Description	Diablo Part No.
LM311	Voltage Comparator	10188-01
LM319	Dual High-Speed Voltage Comparator	10168
LM320H-5	Voltage Regulator, 3-Terminal Negative 5V	42155-05
LM320H-12	Voltage Regulator, 3-Terminal Negative 12V	42155-12
LM340T-12	Voltage Regulator, 3-Terminal Positive 12V	10284-03
LM341P-5	Voltage Regulator, 3-Terminal Positive 5V	42154-05
LM341P-12	Voltage Regularor, 3-Terminal Positive 12V	42154-12
LM733C	Differential Video Amplifier	10124
72747	Dual Op Amp, General Purpose	10165
72747	Dual Op Amp, Selected	13072
72748	Op Amp	10166
MC7912 CB	Voltage Regulator, -12V	13142

Miscellaneous/Special Purpose:

Type	Description	Diablo Part No.
10706	Clock Generator	13143
CA3086	NPN Transistor Array	42191-32
8041	Quad FET	10190
10453	Parallel Data Control	13159
1408L-6	Digital-to-Analog Converter	13060
	Resistor Network, 1K (15 resistors)	10239-01
	Resistor Network, 1K (13 resistors)	10761
	Resistor Network, 10K (8 resistors)	13044
	Resistor Network, 15K (13 resistors)	13140

Memory

Type	Description	Diablo Part No.
10809	256 x 8-Bit RAM	13158
2111A-4	MOS 256 x 4-Bit RAM (450 ns)	42334-11
82S115	TTL 512 x 8-Bit pROM, Three State	10406
8316A	TTL 2K x 8-Bit masked ROM, Three State	—
8708	MOS 1K x 8-Bit EROM, Three State	42329

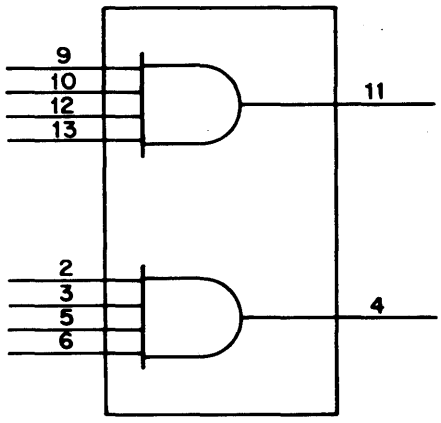
NOTE

Any Diablo part number given here is for the "raw" (unprogrammed) IC. When a pROM or EROM contains a program or data, it is assigned a new part number reflecting the program or data it contains. Masked ROMs are programmed during manufacture; each ROM with a different program carries a different part number.

TTL Dual 4-Input Expander | Part No. 42191-31 | Type 933

This device is an expander element which allows increased fan-in for buffer units.

Logic Symbol



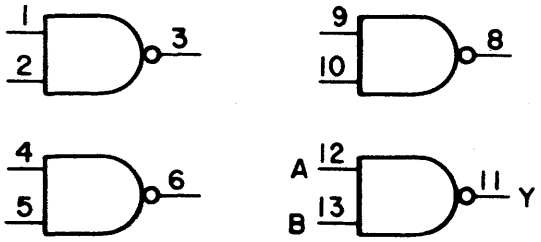
VCC – 14

GND – 7

(083-030)

TTL Quad 2-Input NAND Gate — Part No. 10134 — Type 7400
TTL Quad 2-Input NAND Gate, Low Power Schottky — Part No. 13077 — Type 74LS00

Logic Symbol



Alternate Symbol

Truth Table

A	B	Y
L	L	H
H	L	H
L	H	H
H	H	L

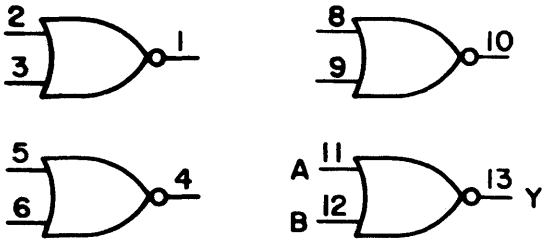
VCC-14, GND-7

Loading:

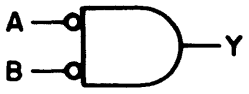
Inputs	1 Unit Load (.2 for 74LS00)
Outputs	10 Unit Loads (5 for 74LS00)

TTL Quad 2-Input NOR Gate — Part No. 10135 — Type 7402
TTL Quad 2-Input NOR Gate, Low Power Schottky — Part No. 42350-1 — Type 74LS02

Logic Symbol



Alternate Symbol



Truth Table

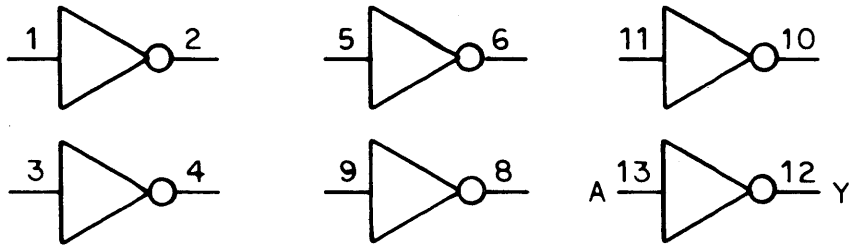
A	B	Y
L	L	H
H	L	L
L	H	L
H	H	L

VCC-14, GND-7

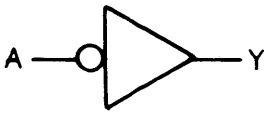
Loading:	7402	74LS02
Inputs	1 Unit Load	.2 Unit Load
Outputs	10 Unit Load	5 Unit Loads

TTL Hex Inverter	Part No. 10136	Type 7404
TTL Hex Inverter, Low Power Schottky	Part No. 10209	Type 74LS04
TTL Hex Inverter, Open Collector	Part No. 10209	Type 7405

Logic Symbol



Alternate Symbol

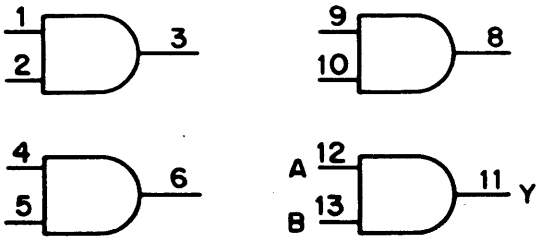


VCC-14, GND-7

Loading:	7404	74LS04	7405
Inputs	1 Unit Loads	.2 Unit Loads	1 Unit Load
Outputs	10 Unit Loads	5 Unit Loads	10 Unit Loads

TTL Quad 2-Input AND Gate — Part No. 10119 — Type 7408
TTL Quad 2-Input AND Gate, Low Power Schottky — Part No. 10210 — Type 74LS08

Logic



Symbol

Truth Table

A	B	Y
L	L	L
H	L	L
L	H	L
H	H	H

VCC-14, GND-7

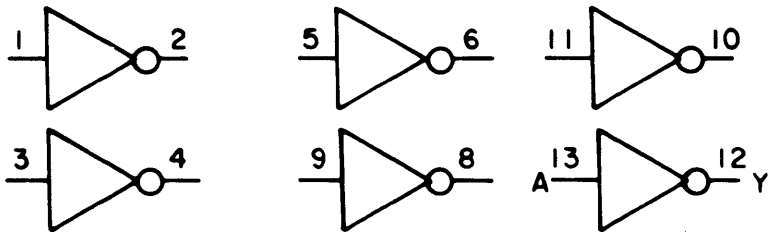
Loading:

Inputs	1 Unit Load (.2 for 74LS08)
Outputs	10 Unit Loads (5 for 74LS08)

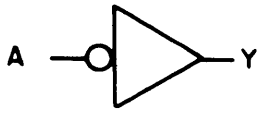
TTL Hex Inverter Buffer/Driver — Part No. 10390 — Type 7416

These drivers have high-voltage (up to 15V) open-collector outputs for interfacing with high-level circuits or for driving high current loads.

Logic Symbol



Alternate Symbol

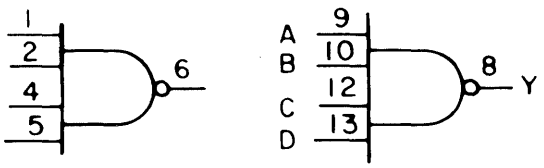


Loading:

Inputs	1 Unit Load
Outputs	25 Unit Loads

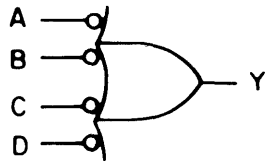
TTL Dual 4-Input NAND Gate | Part No. 10125 | Type 7420

Logic Symbol



VCC-14, GND-7. Pins 3 & 11 not used.

Alternate Symbol



Truth Table

A	B	C	D	Y
L	L	L	L	H
L	L	L	H	H
L	L	H	L	H
L	L	H	H	H
L	H	L	L	H
L	H	L	H	H
L	H	H	L	H
L	H	H	H	H
H	L	L	L	H
H	L	L	H	H
H	L	H	L	H
H	L	H	H	H
H	H	L	L	H
H	H	L	H	H
H	H	H	L	H
H	H	H	H	L

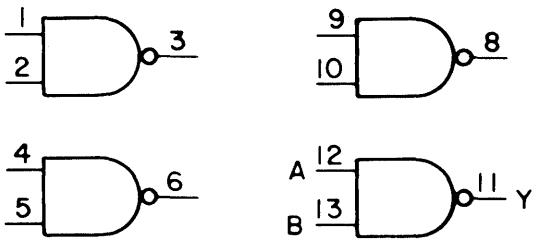
Loading:

Inputs	1 Unit Load
Outputs	10 Unit Loads

TTL Quad 2-Input NAND High-Voltage Interface Gate | Part No. 10120 | Type 7426

These gates have high-voltage (up to 15V) open-collector outputs for interfacing with high-level circuits.

Logic Symbol



VCC-14, GND-7

Alternate Symbol

Truth Table

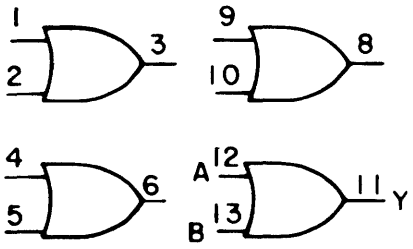
A	B	Y
L	L	H
H	L	H
L	H	H
H	H	L

Loading:

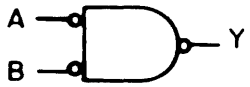
Inputs	1 Unit Load
Outputs	10 Unit Loads

TTL Quad 2-Input OR Gate — Part No. 10302 — Type 7432
TTL Quad 2-Input OR Gate, Low Power Schottky — Part No. 13082 — Type 74LS32

Logic Symbol



Alternate Symbol



Truth Table

A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

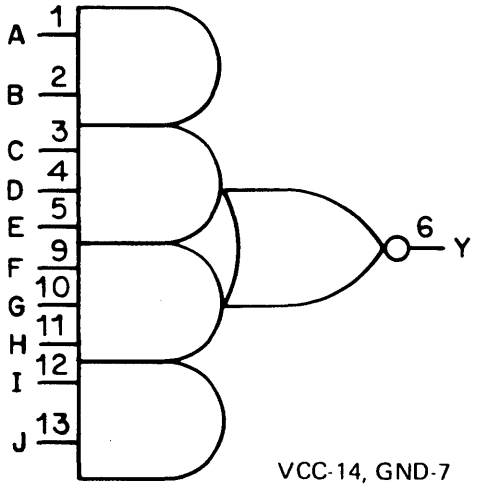
VCC-14, GND-7

Loading:

Inputs	1 Unit Load (.25 for 74LS32)
Outputs	10 Unit Loads (5 for 74LS32)

TTL 4-Wide AND-OR-INVERT Gate — Part No. 42408-01 — Type 74LS54

Logic Symbol



$$Y = \overline{AB+CDE+FGH+IJ}$$

VCC-14, GND-7

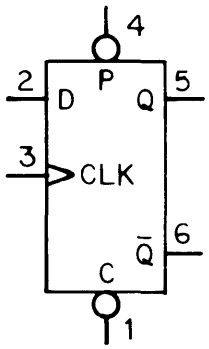
Loading:

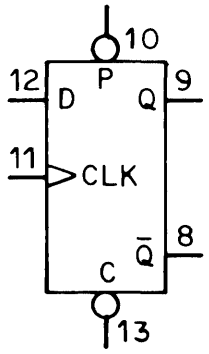
Inputs	.25 Unit Load
Outputs	5 Unit Loads

TTL Dual D Flip-flop — Part No. 10139 — Type 7474
TTL Dual D Flip-Flop, Low Power Schottky — Part No. 13085 — Type 74LS74

The 7474 contains two D-type edge-triggered flip-flops with direct preset and clear inputs. A low level on the preset or clear input will set or reset the flip-flop, respectively, regardless of other input conditions. When both the preset and clear are high, the logic level on D is transferred to Q on the positive-going edge of the clock.

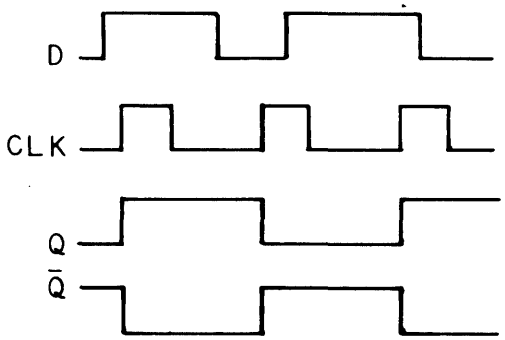
Logic Symbol





VCC-14, GND-7

Timing Waveforms



Truth Table

Function	Inputs				Outputs	
	Preset	Clear	Clock	D	Q	Q̄
Preset	L	H	X	X	H	L
Clear	H	L	X	X	L	H
Clear	L	L	X	X	H	H*
Set	H	H	↑	H	H	L
Reset	H	H	↑	L	L	H
Set Up	H	H	L	X	No Change	

P = Preset input
D = Data input
CLK = Clock input
C = Clear input
Q,Q̄ = Data outputs

*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high level).

Loading:

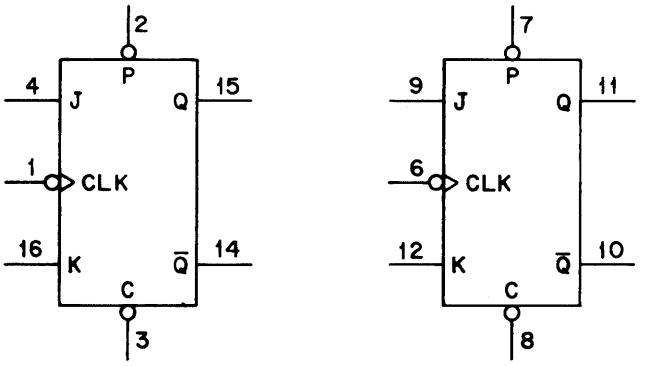
		Unit Loads	
		7474	74LS74
Inputs	CLK	2	.5
	D	1	.25
	P	1	.5
	C	2	.75
Outputs	Q,Q̄	10	5

TTL Dual J-K Flip-Flop with Preset and Clear

Part No. 10138

Type 7476

Logic Symbol



VCC – 5

GND – 8

(083 – 038)

Truth Table

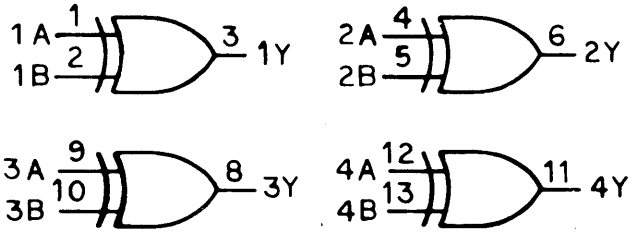
		INPUTS			OUTPUTS	
PR	CLR	CLK	J	K	Q	Q
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H	H
H	H		L	L	Q0	Q0
H	H		H	L	H	L
H	H		L	H	L	H
H	H		H	H	TOGGLE	

TTL Quad 2-Input Exclusive OR Gate

Part No. 10303

Type 7486

Logic Symbol



VCC-14, GND-7

Truth Table

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

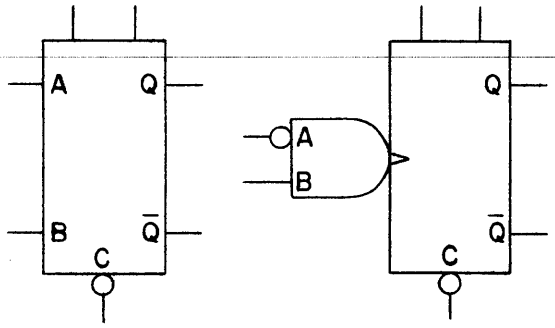
Loading:

Inputs	1 Unit Load
Outputs	10 Unit Loads

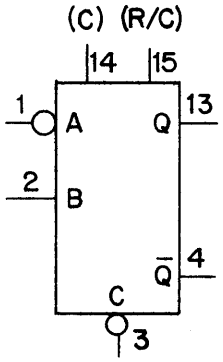
TTL Dual Retriggerable One-Shot Part No. 10145 Type 74123
TTL Dual Retriggerable One-Shot Part No. 42313-01 Type 74LS123

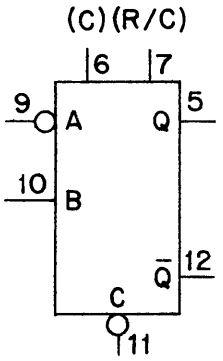
Either of the one-shots in this package can be triggered by a positive-going or a negative-going input, providing the other input is already in the proper state. At least one of the inputs must be removed and re-applied in order to retrigger the device. A low on the C input terminates the output pulse immediately. The length of the output pulse is dependent upon external timing components.

Alternate Symbols



Logic Symbol





Truth Table

INPUTS			OUTPUTS	
CLEAR	A	B	Q	Q
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L			
H		H		
	L	H		

Loading:	74123	74LS123
Clear	2 Unit Loads	.25 Unit Load
Other Inputs	1 Unit Load	.25 Unit Load
Outputs	10 Unit Loads	5 Unit Loads

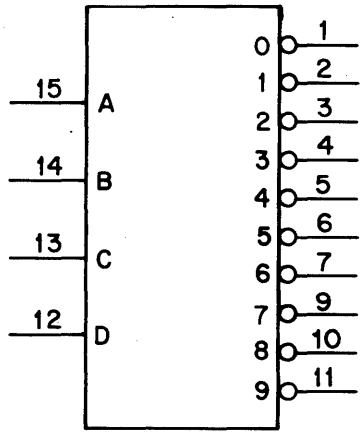
BCD/Decimal Decoder/Driver, Low Power Schottky

Part No. 10172-29

Type 74LS145

This BCD-to-decimal decoder/driver consists of eight inverters and ten 4-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of BCD input logic ensures that all outputs remain off for all invalid (10-15) binary input conditions.

Logic Symbol



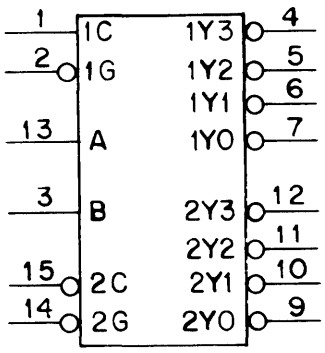
VCC – 16

GND – 8

(083-035)

TTL Dual 2:4 Decoder — Part No. 10194 — Type 74155
TTL Dual 2:4 Decoder, Low Power Schottky — Part No. 13090 — Type 74LS155

Logic Symbol



VCC-16, GND-8

Truth Table

Inputs				Outputs			
Select		Gate	Data				
B	A	1G	1C	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H
		2G	2C	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

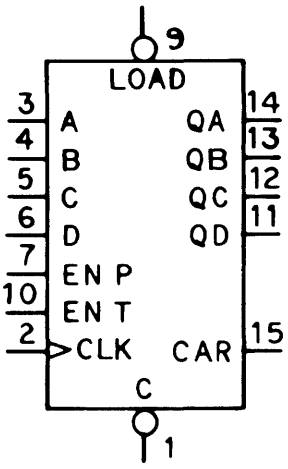
Loading:

Inputs	1 Unit Load (.25 for 74LS155)
Outputs	10 Unit Loads (5 for 74LS155)

TTL 4-Bit Synchronous Binary Counter — Part No. 10335 — Type 74161
TTL 4-Bit Synchronous Binary Counter, Low Power Schottky — Part No. 13091 — Type 74LS161

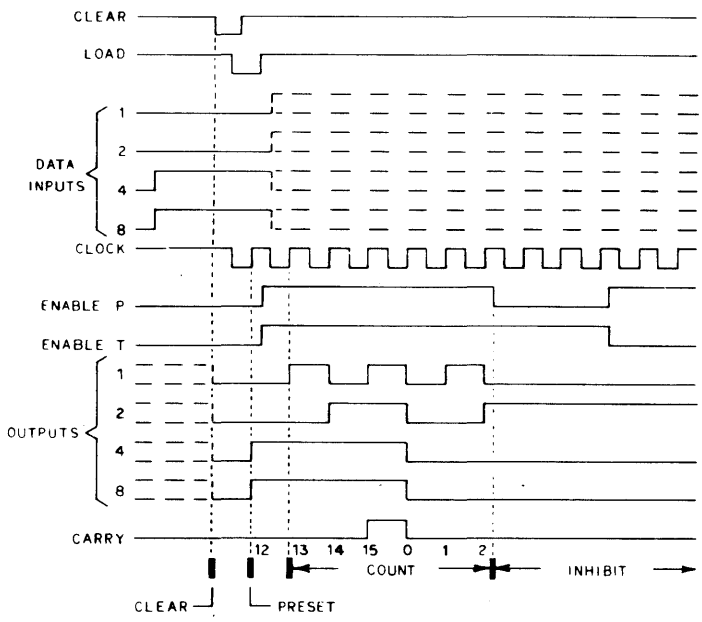
All flip-flops in this chip are clocked simultaneously, so all output changes occur simultaneously. A low on the Clear input overrides other inputs, and drives all outputs low.

Logic Symbol



VCC-16, GND-8

Timing Waveforms



1. Clear outputs to zero
2. Preset to binary twelve
3. Count to thirteen, fourteen, fifteen, zero, one, and two.
4. Inhibit

Loading:

		Unit Loads	
		74161	74LS161
Inputs	LOAD	1	.5
	CLK, EN-T	2	.5
	Other	1	.25
Outputs		10	5

Truth Table

INPUTS						
CLK	EN-P	EN-T	LOAD	C	A,B,C,D	OUTPUTS
H	X	X	X	X	X	No Change
L	X*	X*	X*	X	X	No Change
X	X	X	X	L	X	All LOW
↑	X	X	L	H	DATA	Preset to A,B,C,D, input data
↑	L	L	H	H	X	No Change
↑	H	L	H	H	X	No Change
↑	L	H	H	H	X	No Change
↑	H	H	H	H	X	Count Up

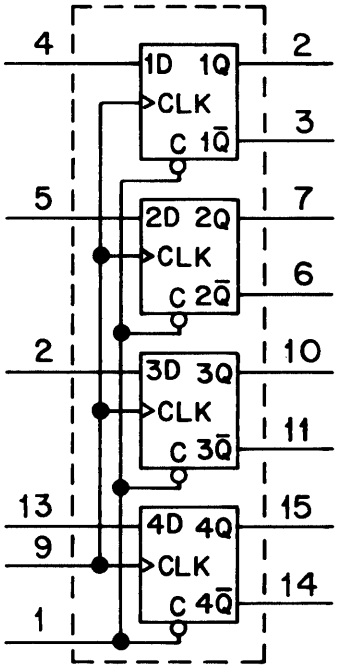
*Avoid changes to inputs while CLK is low.

TTL Quad D Flip-Flop with Clear | Part No. 10337 | Type 74175

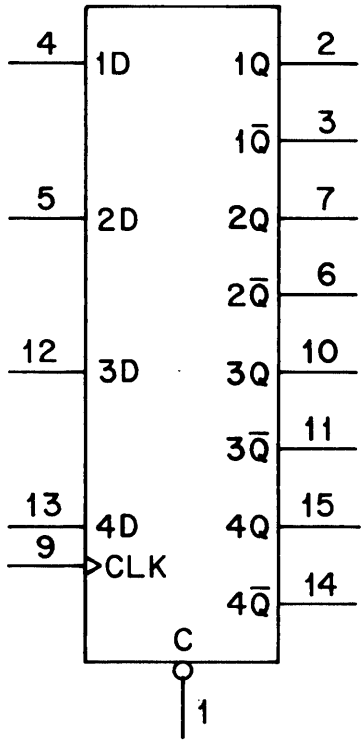
This positive-edge-triggered flip-flop utilizes TTL circuitry to implement D-type flip-flop logic, with a direct clear input and complementary outputs from each flip-flop.

Data at the D inputs meeting the set-up time requirements is transferred to the Q outputs on the positive going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock unput is at either the high or low level, the D input signal has no effect at the output.

Logic Symbol



Alternate Symbol



VCC — 16
GND — 8

(083 – 034)

Synchronous Up/Down Counter with Dual Clock | Part No. 10154 | Type 74193

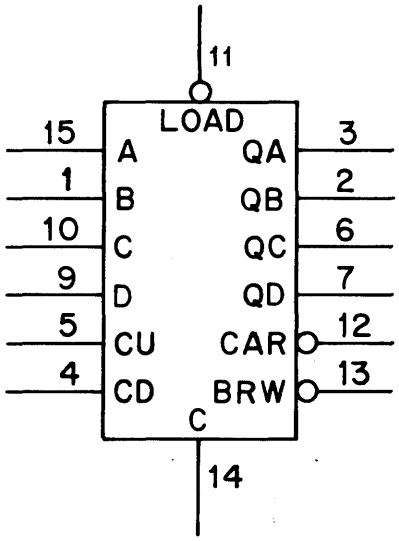
This device is a synchronous up/down 4-bit binary counter. Synchronous operation is provided by having all flip-flops clocked simultaneously, so that the outputs change together when so instructed by steering logic.

The outputs of the four master-slave flip-flops are triggered by a low-to-high transition of either count (clock) input. The direction of counting is determined by which count input is pulsed, while the other count is held high.

All four counters are fully programmable; ie, each output may be preset to either level by entering the desired data at the inputs while the load input is low. The output will change independently of the count pulses.

A clear input, when taken to a high level, forces all outputs to the low level, independent of the count and load inputs. The clear, count, and load inputs are buffered to lower the drive requirements of clock drivers, etc., required for long words.

Logic Symbol



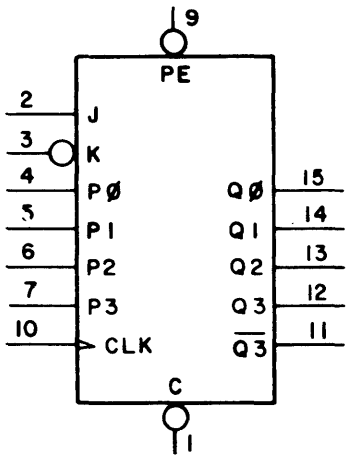
VCC – 16

GND – 8

(083-032)

Data can be loaded into this register either serially or in parallel. When Parallel Enable (PE) is low, parallel data is loaded into the flip-flops on every positive-going clock. When PE is high, data is shifted from the J and K inputs to flip-flop 0, and from 0 to 1, 1 to 2, and 2 to 3, at each positive-going clock transition. A low on the Clear (C) input overrides all other controls.

Logic Symbol



VCC-16, GND-8

Truth Table

Inputs						Outputs					
C	PE	CLK	J	K	P0-P3	Q0	Q1	Q2	Q3	$\overline{Q3}$	
L	X	X	X	X	X	L	L	L	L	H	Clear
H	L	↑	X	X	abcd	a	b	c	d	$\overline{d}$	Parallel Load
H	H	L	X	X	X	Q0n	Q1n	Q2n	Q3n	$\overline{Q3n}$	No Change
H	H	↑	L	L	X	L	Q0n	Q1n	Q2n	$\overline{Q2n}$	Shift
H	H	↑	L	H	X	$\overline{Q0n}$	Q0n	Q1n	Q2n	$\overline{Q2n}$	
H	H	↑	H	L	X	$\overline{Q0n}$	Q0n	Q1n	Q2n	$\overline{Q2n}$	
H	H	↑	H	H	X	H	Q0n	Q1n	Q2n	$\overline{Q2n}$	

H = High
L = Low
X = Irrelevant
Q0n = State of Q0 before positive transition of CLK

Loading:

Inputs	1 Unit Load
Outputs	10 Unit Loads

TTL 8-bit Addressable Latch — Part No. 10339 — Type 74259
TTL 8-bit Addressable Latch, Low Power Schottky — Part No. 13094 — Type 74LS259

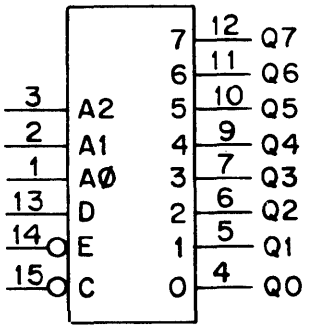
This is a multifunctional device capable of storing single line data in eight addressable latches, and being a one-of-eight decoder and demultiplexer with high-active outputs. It incorporates a low-active common clear for resetting all latches, as well as a low-active enable.

There are two modes of operation, shown in the Function Table. In the addressable latch mode, when E is LOW, data on the data line (D) is written into the addressed latch. The addressed latch will follow the data input, with all nonaddressed latches remaining in their previous states. When E is HIGH all latches remain in their previous state and are unaffected by the data or address inputs. When operating as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while E is HIGH.

In the one-of-eight decoding or demultiplexing mode, the addressed output will follow the state of the D input, with all other outputs in the LOW state.

When E is HIGH and C is LOW all outputs are LOW and unaffected by the address and data inputs.

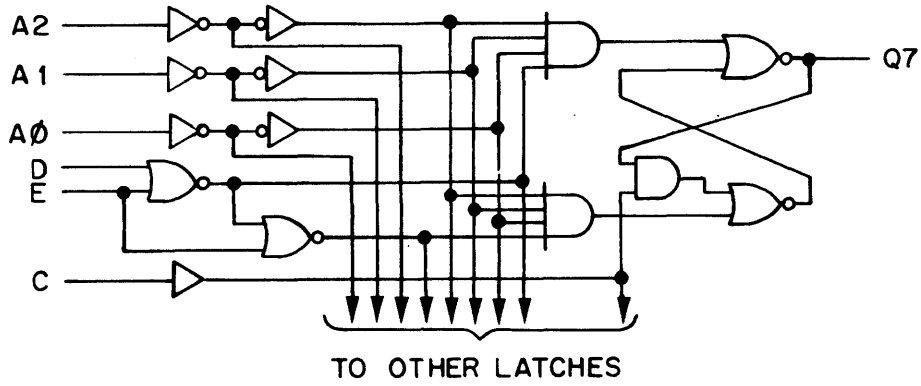
Logic Symbol



VCC-16, GND-8

Logic Diagram

ONLY ONE LATCH SHOWN FOR CLARITY



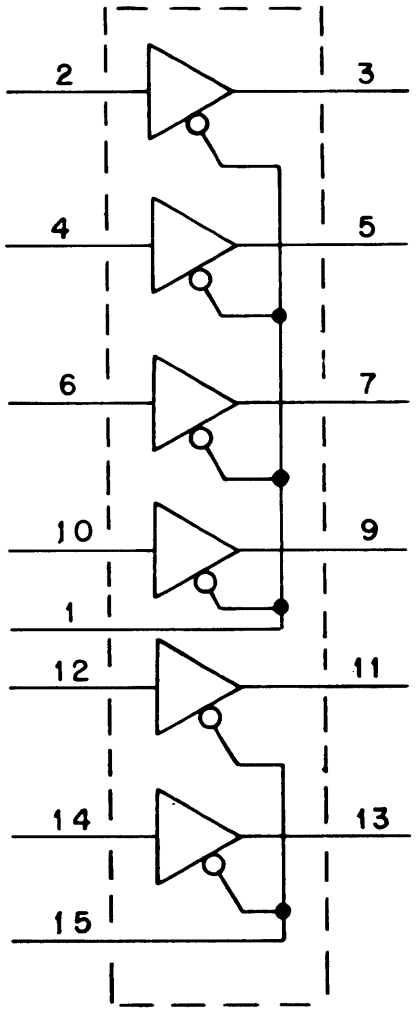
Function Table

Inputs			Outputs		
C	E	D	Addressed Latch	Others	Mode
L	L	L	L	L	Demultiplexer
L	L	H	H	L	Demultiplexer
L	H	X	L	L	Clear
H	L	L	L	No Change	Addressable Latch
H	L	H	H	No Change	Addressable Latch
H	H	X	No Change	No Change	

Loading:

		Unit Loads	
		74259	74LS259
Inputs	E	1.5	.25
	Other	1	.25
Outputs		6	5

Logic Symbol



VCC-16, GND-8

Loading:

	Unit Loads	
	74367	74LS367
Inputs (Gate enabled)	1	.25
Outputs	20	10

MOS 8-bit Microprocessing Unit

Part No. 42338

Type 8080A

This is a single chip 8-bit parallel microprocessor which forms a microcomputer system when interfaced with any type or speed of standard semiconductor memory up to 64K 8-bit words and an I/O device. The MPU inputs and outputs data over an 8-bit bi-directional three-state data bus (D0-D7). It addresses memory and I/O devices over a 16-bit three-state memory address bus (A0-A15). It is driven by two 12-volt non-overlapping clocks, ø1 and ø2. There are four input signals, INT (Interrupt), RDY (Ready), HOLD, and RST (Reset). Output signals include INTE (Interrupt Enable), DBIN (Data Bus In), WR (Write), SYNC, WAIT, and HLDA (Hold Acknowledge).

The 8080A contains a register array made up of six 16-bit registers: a Program Counter, a Stack Pointer, and four register "pairs," each made up of two 8-bit registers. One of these is the Temporary Register, called W/Z, which is used for the internal execution of instructions. The other three are working registers, called B/C, D/F, and H/L. The six general purpose registers can be used as either single 8-bit registers or 16-bit register pairs; W/Z is not program addressable.

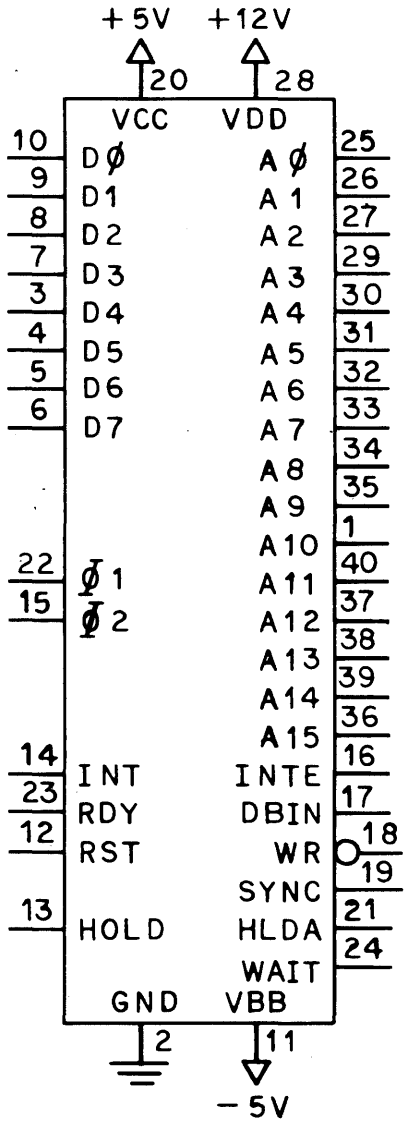
The 8080A also contains an Arithmetic and Logic Unit (ALU), containing an 8-bit accumulator (ACC), an 8-bit temporary accumulator (ACT), an 8-bit temporary register (TMP), and a 5-bit flag register. All arithmetic and logic instructions are performed in this section.

The third major part of the 8080A contains the Instruction Register, Instruction Decoder, and all timing and control logic. The last major portion is the Data Bus Buffer, a 3-state bi-directional 8-bit latch that serves to isolate the the MPU's internal data bus from the external bus.

The instruction set consists of over 100 different instructions, which provide conditional and unconditional branching, decimal and binary arithmetic, and logical, register-to-register, stack control, memory reference, and I/O instructions. Up to 256 input ports and 256 output ports can be addressed. Instructions may be either one, two, or three 8-bit bytes in length. Memory can be referenced four ways: direct, register, register indirect, and immediate. Non memory-reference instructions can be executed in 2 microseconds when a 2 MHz clock is used. The sequential program execution can be interrupted by driving the INT input high.

The 8080A uses its internal stack pointer to access external memory, allowing it to handle multiple-level priority interrupts. This also allows adequate subroutine nesting.

Logic Symbol



Loading:

Outputs 1.2 Unit Loads

Mnemonic	Description	Instruction Code[1] D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Clock[2] Cycles
$MOV_{r1,r2}$	Move register to register	0	1	D	D	D	S	S	S	5
MOV M, r	Move register to memory	0	1	1	1	0	S	S	S	7
MOV r, M	Move memory to register	0	1	D	D	D	1	1	0	7
HLT	Halt	0	1	1	1	0	1	1	0	7
MVI r	Move immediate register	0	0	D	D	D	1	1	0	7
MVI M	Move immediate memory	0	0	1	1	0	1	1	0	10
INR r	Increment register	0	0	D	D	D	1	0	0	5
DCR r	Decrement register	0	0	D	D	D	1	0	1	5
INR M	Increment memory	0	0	1	1	0	1	0	0	10
DCR M	Decrement memory	0	0	1	1	0	1	0	1	10
ADD r	Add register to A	1	0	0	0	0	S	S	S	4
ADC r	Add register to A with carry	1	0	0	0	1	S	S	S	4
SUB r	Subtract register from A	1	0	0	1	0	S	S	S	4
SBB r	Subtract register from A with borrow	1	0	0	1	1	S	S	S	4
ANA r	And register with A	1	0	1	0	0	S	S	S	4
XRA r	Exclusive Or register with A	1	0	1	0	1	S	S	S	4
ORA r	Or register with A	1	0	1	1	0	S	S	S	4
CMP r	Compare register with A	1	0	1	1	1	S	S	S	4
ADD M	Add memory to A	1	0	0	0	0	1	1	0	7
ADC M	Add memory to A with carry	1	0	0	0	1	1	1	0	7
SUB M	Subtract memory from A	1	0	0	1	0	1	1	0	7
SBB M	Subtract memory from A with borrow	1	0	0	1	1	1	1	0	7
ANA M	And memory with A	1	0	1	0	0	1	1	0	7
XRA M	Exclusive Or memory with A	1	0	1	0	1	1	1	0	7
ORA M	Or memory with A	1	0	1	1	0	1	1	0	7
CMP M	Compare memory with A	1	0	1	1	1	1	1	0	7
ADI	Add immediate to A	1	1	0	0	0	1	1	0	7
ACI	Add immediate to A with carry	1	1	0	0	1	1	1	0	7
SUI	Subtract immediate from A	1	1	0	1	0	1	1	0	7
SBI	Subtract immediate from A with borrow	1	1	0	1	1	1	1	0	7
ANI	And immediate with A	1	1	1	0	0	1	1	0	7
XRI	Exclusive Or immediate with A	1	1	1	0	1	1	1	0	7
ORI	Or immediate with A	1	1	1	1	0	1	1	0	7
CPI	Compare immediate with A	1	1	1	1	1	1	1	0	7
RLC	Rotate A left	0	0	0	0	0	1	1	1	4
RRC	Rotate A right	0	0	0	0	1	1	1	1	4
RAL	Rotate A left through carry	0	0	0	1	0	1	1	1	4
RAR	Rotate A right through carry	0	0	0	1	1	1	1	1	4
JMP	Jump unconditional	1	1	0	0	0	0	1	1	10
JC	Jump on carry	1	1	0	1	1	0	1	0	10
JNC	Jump on no carry	1	1	0	1	0	0	1	0	10
JZ	Jump on zero	1	1	0	0	1	0	1	0	10
JNZ	Jump on no zero	1	1	0	0	0	0	1	0	10
JP	Jump on positive	1	1	1	1	0	0	1	0	10
JM	Jump on minus	1	1	1	1	1	0	1	0	10
JPE	Jump on parity even	1	1	1	0	1	0	1	0	10
JPO	Jump on parity odd	1	1	1	0	0	0	1	0	10
CALL	Call unconditional	1	1	0	0	1	1	0	1	17
CC	Call on carry	1	1	0	1	1	1	0	0	11/17
CNC	Call on no carry	1	1	0	1	0	1	0	0	11/17
CZ	Call on zero	1	1	0	0	1	1	0	0	11/17
CNZ	Call on no zero	1	1	0	0	0	1	0	0	11/17
CP	Call on positive	1	1	1	1	0	1	0	0	11/17
CM	Call on minus	1	1	1	1	1	1	0	0	11/17
CPE	Call on parity even	1	1	1	0	1	1	0	0	11/17
CPO	Call on parity odd	1	1	1	0	0	1	0	0	11/17
RET	Return	1	1	0	0	1	0	0	1	10
RC	Return on carry	1	1	0	1	1	0	0	0	5/11
RNC	Return on no carry	1	1	0	1	0	0	0	0	5/11
RZ	Return on zero	1	1	0	0	1	0	0	0	5/11
RNZ	Return on no zero	1	1	0	0	0	0	0	0	5/11
RP	Return on positive	1	1	1	1	0	0	0	0	5/11
RM	Return on minus	1	1	1	1	1	0	0	0	5/11
RPE	Return on parity even	1	1	1	0	1	0	0	0	5/11
RPO	Return on parity odd	1	1	1	0	0	0	0	0	5/11
RST	Restart(3)	1	1	A	A	A	1	1	1	11
IN	Input	1	1	0	1	1	0	1	1	10
OUT	Output	1	1	0	1	0	0	1	1	10
LXI B	Load immediate register Pair B & C	0	0	0	0	0	0	0	1	10
LXI D	Load immediate register Pair D & E	0	0	0	1	0	0	0	1	10
LXI H	Load immediate register Pair H & L	0	0	1	0	0	0	0	1	10
LXI SP	Load immediate stack pointer	0	0	1	1	0	0	0	1	10
PUSH B	Push register Pair B & C on stack	1	1	0	0	0	1	0	1	11
PUSH D	Push register Pair D & E on stack	1	1	0	1	0	1	0	1	11
PUSH H	Push register Pair H & L on stack	1	1	1	0	0	1	0	1	11
PUSH PSW	Push A and Flags on stack	1	1	1	1	0	1	0	1	11
POP B	Pop register pair B & C off stack	1	1	0	0	0	0	0	1	10
POP D	Pop register pair D & E off stack	1	1	0	1	0	0	0	1	10
POP H	Pop register pair H & L off stack	1	1	1	0	0	0	0	1	10
POP PSW	Pop A and Flags off stack	1	1	1	1	0	0	0	1	10
STA	Store A direct	0	0	1	1	0	0	1	0	13
LDA	Load A direct	0	0	1	1	1	0	1	0	13
XCHG	Exchange D & E, H & L Registers	1	1	1	0	1	0	1	1	4
XTHL	Exchange top of stack, H & L	1	1	1	0	0	0	1	1	18
SPHL	H & L to stack pointer	1	1	1	1	1	0	0	1	5
PCHL	H & L to program counter	1	1	1	0	1	0	0	1	5
DAD B	Add B & C to H & L	0	0	0	0	1	0	0	1	10
DAD D	Add D & E to H & L	0	0	0	1	1	0	0	1	10
DAD H	Add H & L to H & L	0	0	1	0	1	0	0	1	10
DAD SP	Add stack pointer to H & L	0	0	1	1	1	0	0	1	10
STAX B	Store A indirect	0	0	0	0	0	0	1	0	7
STAX D	Store A indirect	0	0	0	1	0	0	1	0	7
LDAX B	Load A indirect	0	0	0	0	1	0	1	0	7
LDAX D	Load A indirect	0	0	0	1	1	0	1	0	7
INX B	Increment B & C registers	0	0	0	0	0	0	1	1	5
INX D	Increment D & E registers	0	0	0	1	0	0	1	1	5
INX H	Increment H & L registers	0	0	1	0	0	0	1	1	5
INX SP	Increment stack pointer	0	0	1	1	0	0	1	1	5
DCX B	Decrement B & C	0	0	0	0	1	0	1	1	5
DCX D	Decrement D & E	0	0	0	1	1	0	1	1	5
DCX H	Decrement H & L	0	0	1	0	1	0	1	1	5
DCX SP	Decrement stack pointer	0	0	1	1	1	0	1	1	5
CMA	Complement A	0	0	1	0	1	1	1	1	4
STC	Set carry	0	0	1	1	0	1	1	1	4
CMC	Complement carry	0	0	1	1	1	1	1	1	4
DAA	Decimal adjust A	0	0	1	0	0	1	1	1	4
SHLD	Store H & L direct	0	0	1	0	0	0	1	0	16
LHLD	Load H & L direct	0	0	1	0	1	0	1	0	16
EI	Enable Interrupts	1	1	1	1	1	0	1	1	4
DI	Disable interrupt	1	1	1	1	0	0	1	1	4
NOP	No-operation	0	0	0	0	0	0	0	0	4

Notes:

1)

	Register							
	A	B	C	D	E	H	L	Mem
DDD or SSS	111	000	001	010	011	100	101	110

2) Two possible cycle times (11/17 or 5/11) indicate instruction cycles dependent on condition flags.

3) After a Restart instruction, the next instruction is fetched from memory at the address eight times AAA.

MNEMONIC	OP CODE		M1[1]					M2		
	$D_7 D_6 D_5 D_4$	$D_3 D_2 D_1 D_0$	T1	T2[2]	T3	T4	T5	T1	T2[2]	T3
MOV r1, r2	0 1 D D	D S S S	PC OUT STATUS	PC = PC + 1	INST→TMP/IR	(SSS)→TMP	(TMP)→DDD			
MOV r, M	0 1 D D	D 1 1 0				X[3]		HL OUT STATUS[6]	DATA →	DDD
MOV M, r	0 1 1 1	0 S S S				(SSS)→TMP		HL OUT STATUS[7]	(TMP) →	DATA BUS
SPHL	1 1 1 1	1 0 0 1				(HL) →	SP			
MVI r, data	0 0 D D	D 1 1 0				X		PC OUT STATUS[6]	B2 →	DDDD
MVI M, data	0 0 1 1	0 1 1 0				X			B2 →	TMP
LXI rp, data	0 0 R P	0 0 0 1				X			PC = PC + 1 B2 →	r1
LDA addr	0 0 1 1	1 0 1 0				X			PC = PC + 1 B2 →	Z
STA addr	0 0 1 1	0 0 1 0				X			PC = PC + 1 B2 →	Z
LHLD addr	0 0 1 0	1 0 1 0				X			PC = PC + 1 B2 →	Z
SHLD addr	0 0 1 0	0 0 1 0				X		PC OUT STATUS[6]	PC = PC + 1 B2 →	Z
LDAX rp[4]	0 0 R P	1 0 1 0				X		rp OUT STATUS[6]	DATA →	A
STAX rp[4]	0 0 R P	0 0 1 0				X		rp OUT STATUS[7]	(A) →	DATA BUS
XCHG	1 1 1 0	1 0 1 1				(HL)←→(DE)				
ADD r	1 0 0 0	0 S S S				(SSS)→TMP (A)→ACT		[9]	(ACT)+(TMP)→A	
ADD M	1 0 0 0	0 1 1 0				(A)→ACT		HL OUT STATUS[6]	DATA →	TMP
ADI data	1 1 0 0	0 1 1 0				(A)→ACT		PC OUT STATUS[6]	PC = PC + 1 B2 →	TMP
ADC r	1 0 0 0	1 S S S				(SSS)→TMP (A)→ACT		[9]	(ACT)+(TMP)+CY→A	
ADC M	1 0 0 0	1 1 1 0				(A)→ACT		HL OUT STATUS[6]	DATA →	TMP
ACI data	1 1 0 0	1 1 1 0				(A)→ACT		PC OUT STATUS[6]	PC = PC + 1 B2 →	TMP
SUB r	1 0 0 1	0 S S S				(SSS)→TMP (A)→ACT		[9]	(ACT)-(TMP)→A	
SUB M	1 0 0 1	0 1 1 0				(A)→ACT		HL OUT STATUS[6]	DATA →	TMP
SUI data	1 1 0 1	0 1 1 0				(A)→ACT		PC OUT STATUS[6]	PC = PC + 1 B2 →	TMP
SBB r	1 0 0 1	1 S S S				(SSS)→TMP (A)→ACT		[9]	(ACT)-(TMP)-CY→A	
SBB M	1 0 0 1	1 1 1 0				(A)→ACT		HL OUT STATUS[6]	DATA →	TMP
SBI data	1 1 0 1	1 1 1 0				(A) →ACT		PC OUT STATUS[6]	PC = PC + 1 B2 →	TMP
INR r	0 0 D D	D 1 0 0				(DDD)→TMP (TMP) + 1→ALU	ALU→DDD			
INR M	0 0 1 1	0 1 0 0				X		HL OUT STATUS[6]	DATA → (TMP)+1 →	TMP ALU
DCR r	0 0 D D	D 1 0 1				(DDD)→TMP (TMP)+1→ALU	ALU→DDD			
DCR M	0 0 1 1	0 1 0 1				X		HL OUT STATUS[6]	DATA → (TMP)-1 →	TMP ALU
INX rp	0 0 R P	0 0 1 1				(RP) + 1 →	RP			
DCX rp	0 0 R P	1 0 1 1				(RP) - 1 →	RP			
DAD rp[8]	0 0 R P	1 0 0 1				X		(ri)→ACT	(L)→TMP (ACT)+(TMP)→ALU	ALU→L, CY
DAA	0 0 1 0	0 1 1 1				DAA→A, FLAGS[10]				
ANA r	1 0 1 0	0 S S S				(SSS)→TMP (A)→ACT		[9]	(ACT)+(TMP)→A	
ANA M	1 0 1 0	0 1 1 0	PC OUT STATUS	PC = PC + 1	INST→TMP/IR	(A)→ACT		HL OUT STATUS[6]	DATA →	TMP

M3			M4			M5				
T1	T2[2]	T3	T1	T2[2]	T3	T1	T2[2]	T3	T4	T5
HL OUT STATUS[7]	(TMP) →	DATA BUS								
PC OUT STATUS[6]	PC = PC + 1 B3 →	rh								
	PC = PC + 1 B3 →	W	WZ OUT STATUS[6]	DATA →	A					
	PC = PC + 1 B3 →	W	WZ OUT STATUS[7]	(A) →	DATA BUS					
	PC = PC + 1 B3 →	W	WZ OUT STATUS[6]	DATA → WZ = WZ + 1	L	WZ OUT STATUS[6]	DATA →	H		
PC OUT STATUS[6]	PC = PC + 1 B3 →	W	WZ OUT STATUS[7]	(L) → WZ = WZ + 1	DATA BUS	WZ OUT STATUS[7]	(H) →	DATA BUS		
[9]	(ACT)+(TMP)→A									
[9]	(ACT)+(TMP)→A									
[9]	(ACT)+(TMP)+CY→A									
[9]	(ACT)+(TMP)+CY→A									
[9]	(ACT)-(TMP)→A									
[9]	(ACT)-(TMP)→A									
[9]	(ACT)-(TMP)-CY→A									
[9]	(ACT)-(TMP)-CY→A									
HL OUT STATUS[7]	ALU →	DATA BUS								
HL OUT STATUS[7]	ALU →	DATA BUS								
(rh)→ACT	(H)→TMP (ACT)+(TMP)+CY→ALU	ALU→H, CY								
[9]	(ACT)+(TMP)→A									

MNEMONIC	OP CODE		M1[1]					M2		
	$D_7 D_6 D_5 D_4$	$D_3 D_2 D_1 D_0$	T1	T2[2]	T3	T4	T5	T1	T2[2]	T3
ANI data	1 1 1 0	0 1 1 0	PC OUT STATUS	PC = PC + 1	INST→TMP/IR	(A)→ACT		PC OUT STATUS[6]	PC = PC + 1 B2 →	→TMP
XRA r	1 0 1 0	1 S S S	↕	↕	↕	(A)→ACT (SSS)→TMP		[9]	(ACT)+(TPM)→A	
XRA M	1 0 1 0	1 1 1 0				(A)→ACT		HL OUT STATUS[6]	DATA →	→TMP
XRI data	1 1 1 0	1 1 1 0				(A)→ACT		PC OUT STATUS[6]	PC = PC + 1 B2 →	→TMP
ORA r	1 0 1 1	0 S S S				(A)→ACT (SSS)→TMP		[9]	(ACT)+(TMP)→A	
ORA M	1 0 1 1	0 1 1 0				(A)→ACT		HL OUT STATUS[6]	DATA →	→TMP
ORI data	1 1 1 1	0 1 1 0				(A)→ACT		PC OUT STATUS[6]	PC = PC + 1 B2 →	→TMP
CMP r	1 0 1 1	1 S S S				(A)→ACT (SSS)→TMP		[9]	(ACT)-(TMP), FLAGS	
CMP M	1 0 1 1	1 1 1 0				(A)→ACT		HL OUT STATUS[6]	DATA →	→TMP
CPI data	1 1 1 1	1 1 1 0				(A)→ACT		PC OUT STATUS[6]	PC = PC + 1 B2 →	→TMP
RLC	0 0 0 0	0 1 1 1				(A)→ALU ROTATE		[9]	ALU→A, CY	
RRC	0 0 0 0	1 1 1 1				(A)→ALU ROTATE		[9]	ALU→A, CY	
RAL	0 0 0 1	0 1 1 1				(A), CY→ALU ROTATE		[9]	ALU→A, CY	
RAR	0 0 0 1	1 1 1 1				(A), CY→ALU ROTATE		[9]	ALU→A, CY	
CMA	0 0 1 0	1 1 1 1				$(\bar{A})\rightarrow A$				
CMC	0 0 1 1	1 1 1 1				$\overline{CY}\rightarrow CY$				
STC	0 0 1 1	0 1 1 1				1→CY				
JMP addr	1 1 0 0	0 0 1 1				X		PC OUT STATUS[6]	PC = PC + 1 B2 →	→Z
J cond addr[17]	1 1 C C	C 0 1 0				JUDGE CONDITION		PC OUT STATUS[6]	PC = PC + 1 B2 →	→Z
CALL addr	1 1 0 0	1 1 0 1				SP = SP - 1		PC OUT STATUS[6]	PC = PC + 1 B2 →	→Z
C cond addr[17]	1 1 C C	C 1 0 0				JUDGE CONDITION IF TRUE, SP = SP - 1		PC OUT STATUS[6]	PC = PC + 1 B2 →	→Z
RET	1 1 0 0	1 0 0 1				X		SP OUT STATUS[15]	SP = SP + 1 DATA →	→Z
R cond addr[17]	1 1 C C	C 0 0 0			INST→TMP/IR	JUDGE CONDITION[14]		SP OUT STATUS[15]	SP = SP + 1 DATA →	→Z
RST n	1 1 N N	N 1 1 1			ϕ→W INST→TMP/IR	SP = SP - 1		SP OUT STATUS[16]	SP = SP - 1 (PCH) →	→DATA BUS
PCHL	1 1 1 0	1 0 0 1			INST→TMP/IR	(HL) → PC				
PUSH rp	1 1 R P	0 1 0 1			↕	SP = SP - 1		SP OUT STATUS[16]	SP = SP - 1 (rh) →	→DATA BUS
PUSH PSW	1 1 1 1	0 1 0 1				SP = SP - 1		SP OUT STATUS[16]	SP = SP - 1 (A) →	→DATA BUS
POP rp	1 1 R P	0 0 0 1				X		SP OUT STATUS[15]	SP = SP + 1 DATA →	→r1
POP PSW	1 1 1 1	0 0 0 1				X		SP OUT STATUS[15]	SP = SP + 1 DATA →	→FLAGS
XTHL	1 1 1 0	0 0 1 1				X		SP OUT STATUS[15]	SP = SP + 1 DATA →	→Z
IN port	1 1 0 1	1 0 1 1				X		PC OUT STATUS[6]	PC = PC + 1 B2 →	→Z, W
OUT port	1 1 0 1	0 0 1 1				X		PC OUT STATUS[6]	PC = PC + 1 B2 →	→Z, W
EI	1 1 1 1	1 0 1 1				SET INTE F/F				
DI	1 1 1 1	0 0 1 1				RESET INTE F/F				
HLT	0 1 1 1	0 1 1 0	↕	↕	↕	X		PC OUT STATUS	HALT MODE[20]	
NOP	0 0 0 0	0 0 0 0	PC OUT STATUS	PC = PC + 1	INST→TMP/IR	X				

M3			M4			M5						
T1	T2[2]	T3	T1	T2[2]	T3	T1	T2[2]	T3	T4	T5		
[9]	(ACT)+(TMP)→A											
[9]	(ACT)+(TMP)→A											
[9]	(ACT)+(TMP)→A											
[9]	(ACT)+(TMP)→A											
[9]	(ACT)+(TMP)→A											
[9]	(ACT)-(TMP), FLAGS											
[9]	(ACT)-(TMP), FLAGS											
PC OUT STATUS[6]	PC = PC + 1 B3	→W									WZ OUT STATUS[11]	(WZ) + 1 → PC
PC OUT STATUS[6]	PC = PC + 1 B3	→W									WZ OUT STATUS[11,12]	(WZ) + 1 → PC
PC OUT STATUS[6]	PC = PC + 1 B3	→W	SP OUT STATUS[16]	(PCH) → SP = SP - 1	→DATA BUS	SP OUT STATUS[16]	(PCL) →	DATA BUS			WZ OUT STATUS[11]	(WZ) + 1 → PC
PC OUT STATUS[6]	PC = PC + 1 B3	→W[13]	SP OUT STATUS[16]	(PCH) → SP = SP - 1	→DATA BUS	SP OUT STATUS[16]	(PCL) →	DATA BUS			WZ OUT STATUS[11,12]	(WZ) + 1 → PC
SP OUT STATUS[15]	SP = SP + 1 DATA	→W									WZ OUT STATUS[11]	(WZ) + 1 → PC
SP OUT STATUS[15]	SP = SP + 1 DATA	→W									WZ OUT STATUS[11,12]	(WZ) + 1 → PC
SP OUT STATUS[16]	(TMP = 00NNN000) → (PCL)	→Z →DATA BUS									WZ OUT STATUS[11]	(WZ) + 1 → PC
SP OUT STATUS[16]	(rl)	→DATA BUS										
SP OUT STATUS[16]	FLAGS	→DATA BUS										
SP OUT STATUS[15]	SP = SP + 1 DATA	→rh										
SP OUT STATUS[15]	SP = SP + 1 DATA	→A										
SP OUT STATUS[15]	DATA	→W	SP OUT STATUS[16]	(H)	→DATA BUS	SP OUT STATUS[16]	(L) →	DATA BUS	(WZ)	→HL		
WZ OUT STATUS[18]	DATA	→A										
WZ OUT STATUS[18]	(A)	→DATA BUS										

NOTES FOR CHART ON PRECEDING PAGES

1. The first memory cycle (M1) is always an instruction fetch; the first (or only) byte, containing the op code, is fetched during this cycle.

2. If the READY input from memory is not high during T2 of each memory cycle, the processor will enter a wait state (TW) until READY is sampled as high.

3. States T4 and T5 are present, as required, for operations which are completely internal to the CPU. The contents of the internal bus during T4 and T5 are available at the data bus; this is designed for testing purposes only. An "X" denotes that the state is present, but is only used for such internal operations as instruction decoding.

4. Only register pairs rp = B (registers B and C) or rp = D (registers D and E) may be specified.

5. These states are skipped.

6. Memory read sub-cycles; an instruction or data word will be read.

7. Memory write sub-cycle.

8. The READY signal is not required during the second and third sub-cycles (M2 and M3). The HOLD signal is accepted during M2 and M3. The SYNC signal is not generated during M2 and M3. During the execution of DAD, M2 and M3 are required for an internal register-pair add; memory is not referenced.

9. The results of these arithmetic, logical or rotate instructions are not moved into the accumulator (A) until state T2 of the next instruction cycle. That is, A is loaded while the next instruction is being fetched; this overlapping of operations allows for faster processing.

10. If the value of the least significant 4-bits of the accumulator is greater than 9 or if the auxiliary carry bit is set, 6 is added to the accumulator. If the value of the most significant 4-bits of the accumulator is now greater than 9, or if the carry bit is set, 6 is added to the most significant 4-bits of the accumulator.

11. This represents the first sub-cycle (the instruction fetch) of the next instruction cycle.

12. If the condition was met, the contents of the register pair WZ are output on the address lines ($A_{0\text{-}15}$) instead of the contents of the program counter (PC).

13. If the condition was not met, sub-cycles M4 and M5 are skipped; the processor instead proceeds immediately to the instruction fetch (M1) of the next instruction cycle.

14. If the condition was not met, sub-cycles M2 and M3 are skipped; the processor instead proceeds immediately to the instruction fetch (M1) of the next instruction cycle.

15. Stack read sub-cycle.

16. Stack write sub-cycle.

17.

CONDITION		CCC
NZ	– not zero (Z = 0)	000
Z	– zero (Z = 1)	001
NC	– no carry (CY = 0)	010
C	– carry (CY = 1)	011
PO	– parity odd (P = 0)	100
PE	– parity even (P = 1)	101
P	– plus (S = 0)	110
M	– minus (S = 1)	111

18. I/O sub-cycle: the I/O port's 8-bit select code is duplicated on address lines 0-7 ($A_{0\text{-}7}$) and 8-15 ($A_{8\text{-}15}$).

19. Output sub-cycle.

20. The processor will remain idle in the halt state until an interrupt, a reset or a hold is accepted. When a hold request is accepted, the CPU enters the hold mode; after the hold mode is terminated, the processor returns to the halt state. After a reset is accepted, the processor begins execution at memory location zero. After an interrupt is accepted, the processor executes the instruction forced onto the data bus (usually a restart instruction).

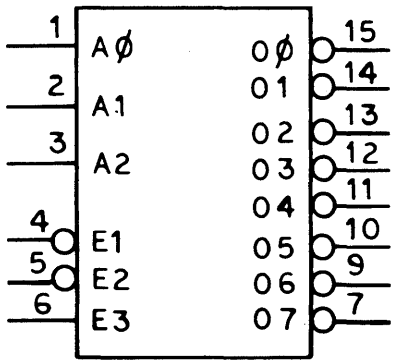
SSS or DDD	Value	rp	Value
A	111	B	00
B	000	D	01
C	001	H	10
D	010	SP	11
E	011		
H	100		
L	101		

TTL 3-Line to 8-Line Decoder

Part No. 42335-XX
Part No. 42403-XX

Type 8205
Type 25LS138

Logic Symbol



VCC-16, GND-8

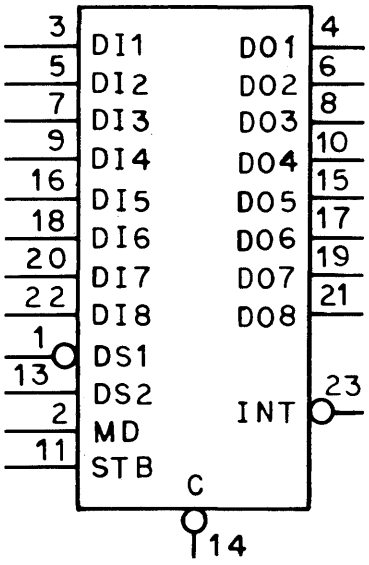
Truth Table

Inputs						Outputs							
A0	A1	A2	E1	E2	E3	0	1	2	3	4	5	6	7
L	L	L	L	L	H	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	L	H	H	H	L	H	H	H	H	H
H	H	L	L	L	H	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
H	L	H	L	L	H	H	H	H	H	H	L	H	H
L	H	H	L	L	H	H	H	H	H	H	H	L	H
H	H	H	L	L	H	H	H	H	H	H	H	H	L
X	X	X	L	L	L	H	H	H	H	H	H	H	H
X	X	X	H	L	L	H	H	H	H	H	H	H	H
X	X	X	L	H	L	H	H	H	H	H	H	H	H
X	X	X	H	H	L	H	H	H	H	H	H	H	H
X	X	X	H	L	H	H	H	H	H	H	H	H	H
X	X	X	L	H	H	H	H	H	H	H	H	H	H
X	X	X	H	H	H	H	H	H	H	H	H	H	H

Loading:	8205	25LS138
Inputs	.16 Unit Load	.25 Unit Load
Outputs	6 Unit Loads	5 Unit Loads

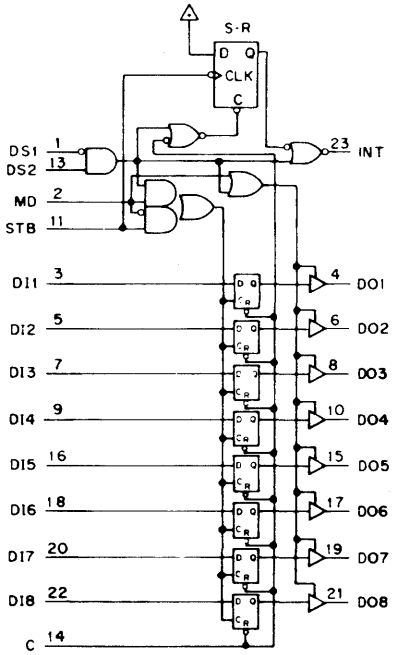
This device contains an 8-bit latch with three-state output buffers and logic to allow independent control of input and output. It also has an internal Service Request flip-flop for generating interrupts for the MPU.

Logic Symbol



VCC-24, GND-12

Logic Diagram



Function Table

Mode	Inputs MD	DS1=L DS2=H	STB	DI1-8	Outputs DO1-8	Internal Latches
Input	L	No	L	X	Hi-Z	No Change
	L	No	H	L	Hi-Z	Load L
	L	No	H	H	Hi-Z	Load H
	L	Yes	L	X	Previous H/L	No Change
	L	Yes	H	H	H	Load H
	L	Yes	H	L	L	Load L
Output	H	No	X	X	Previous H/L	Read
	H	Yes	X	H	H	Load H
	H	Yes	X	L	L	Load L

Loading:

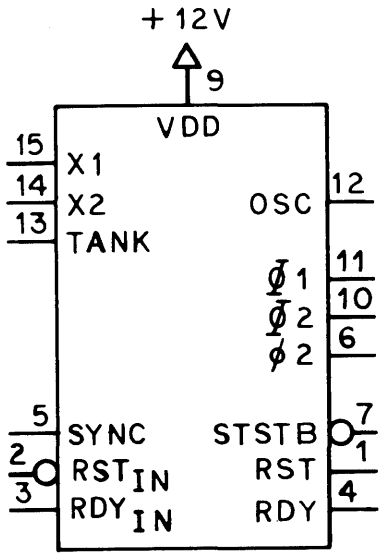
Inputs	
C, DS2, DI1-8, STB	.16 Unit Load
MD	.46 Unit Load
DS1	.62 Unit Load
Outputs	9 Unit Loads

Interrupt Generation

Inputs DS1=L DS2=H	C	STB	S-R ff	Output INT
No	L	L	L	H
No	H	L	No Change	
No	H	↓	H	L
Yes	X	X	X	L

The device provides the 12 volt, non-overlapping clocks required by the 8080 MPU. The frequency of the output signals is determined by an external crystal (crystal frequency = 9 times clock frequency). It also provides power-up Reset and Status Strobe functions.

Logic Symbol



VCC–16, GND–8

Loading:

Inputs	.16 Unit Load
Outputs	
RDY,RST,STSTB	1.5 Unit Loads
ø2,OSC	9 Unit Loads

Clock Generator

The clock generator provides the 12 volt Ø1 and Ø2 signals needed by the 8080, plus a Ø2 TTL signal for related logic.

Status Strobe

The SYNC signal from the 8080 is used to generate STSTB (low active) at the earliest possible moment that the 8080 status data is stable on the MPU data bus (at the beginning of each 8080 machine cycle). This STSTB signal is used by the 8228 System Controller IC. STSTB is also developed when RST is produced.

Reset

A pulse is developed automatically at turn-on when power reaches a minimum predetermined value. A level is produced when the RST-IN input is driven low.

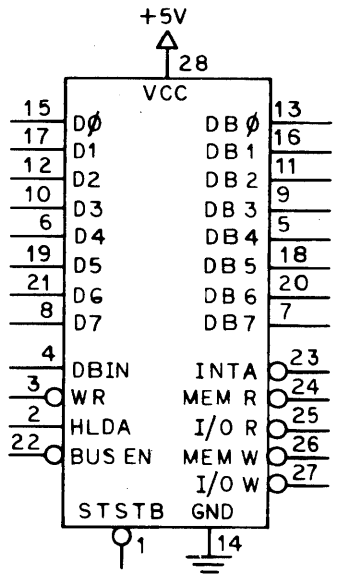
Ready

The RDY input to the 8080 must meet certain critical timing requirements. An asynchronous signal can be applied to the 8224 on the RDY-IN input, and the RDY output of the 8224 will be synchronized properly with the 8080.

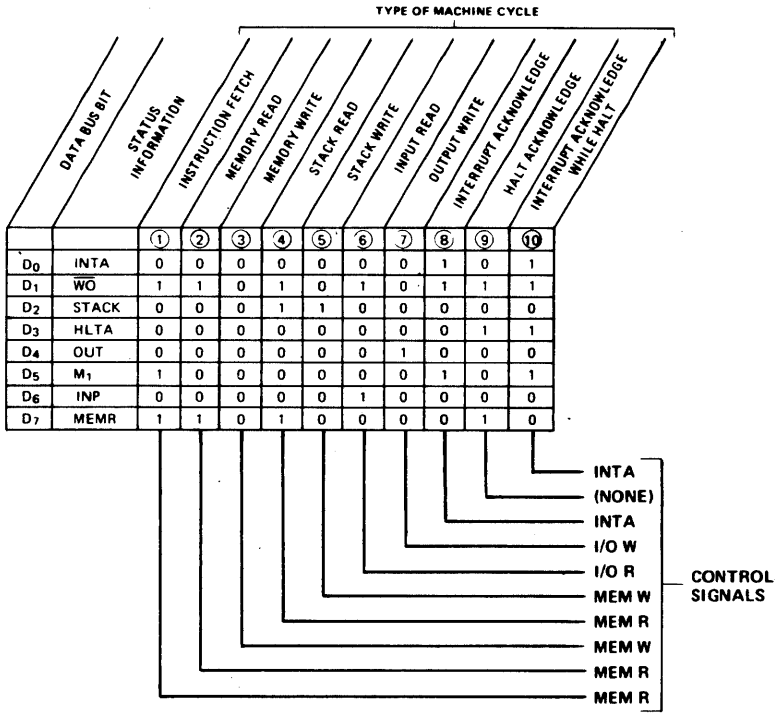
TTL Bus Driver/System Controller, Schottky | Part No. 42331 | Type 8228

This is a combination bi-directional 8-bit bus driver and system controller for use with the 8080 MPU.

Logic Symbol



Status Word Chart



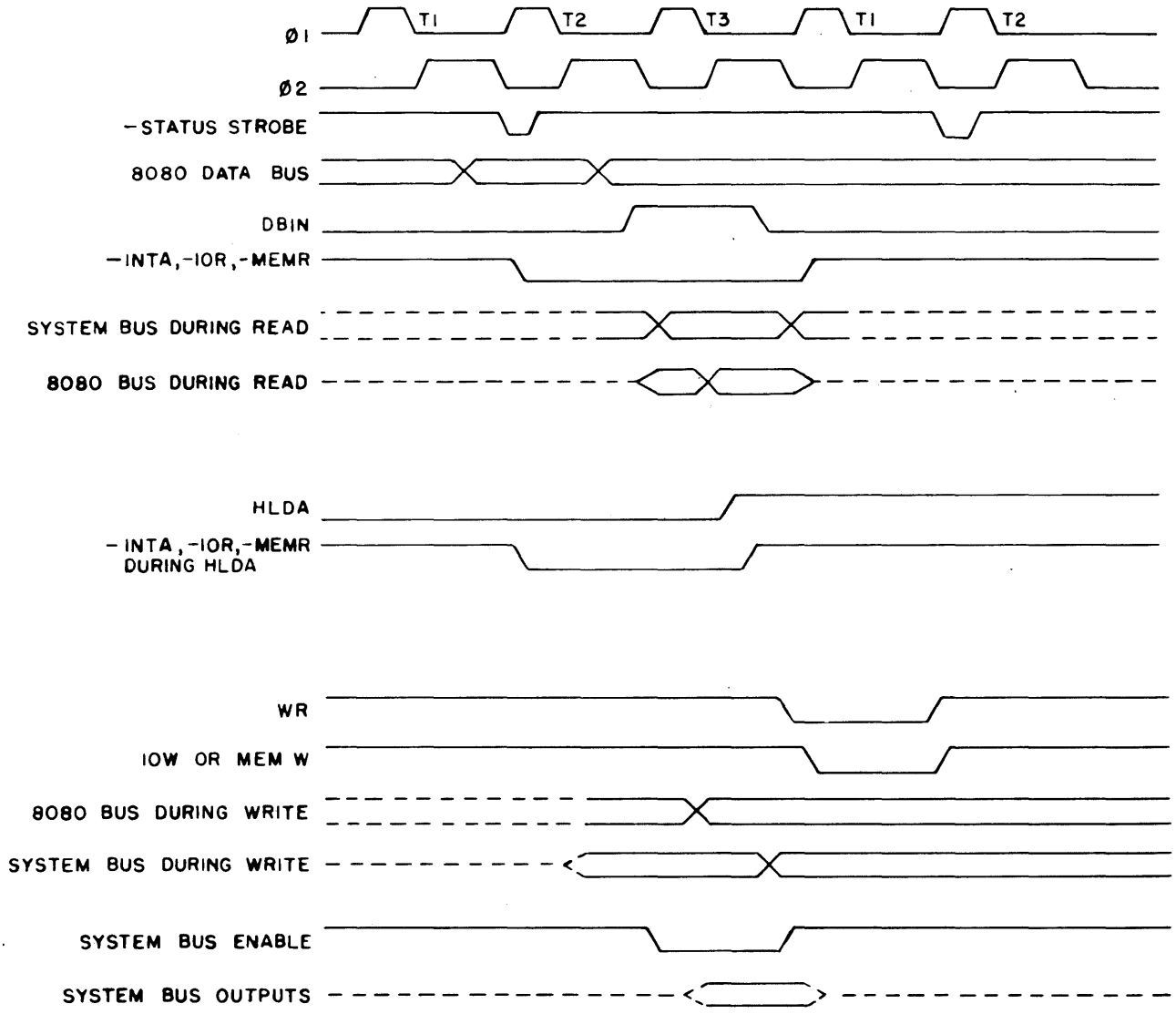
Bus Driver

When driving into the 8080 MPU, this device provides a minimum of +3.6 volts, well above the +3.3 volts required by the 8080. On 8080 output, this device provides 10 ma of drive current, as opposed to the 8080's 1.9 ma. The direction of data flow on the bus is controlled by the System Controller portion of this IC. The BUS EN input turns the bus driver on and off; when BUS EN is high, the bus outputs are in the three-state high-impedance condition.

System Controller

At the beginning of each 8080 machine cycle, the status information from the 8080 is loaded into a 6-bit latch inside the 8228. The STSTB signal from the 8224 IC strobes this latch. The outputs of this latch are then gated by the DBIN, WR, and HLDA outputs from the 8080 to produce the system control outputs MEM R, MEM W, I/O R, I/O W, and INTA. Interrupt Acknowledge (INTA) is normally used to gate instruction data from the peripheral circuitry onto the data bus after the MPU has been interrupted. A special feature of this IC allows an RST7 (Restart 7) instruction to be gated into the MPU automatically whenever the MPU is interrupted. This is accomplished by connecting the INTA output to +12 volts through a 1K resistor.

Type 8228
Timing Waveforms



Loading:

Inputs

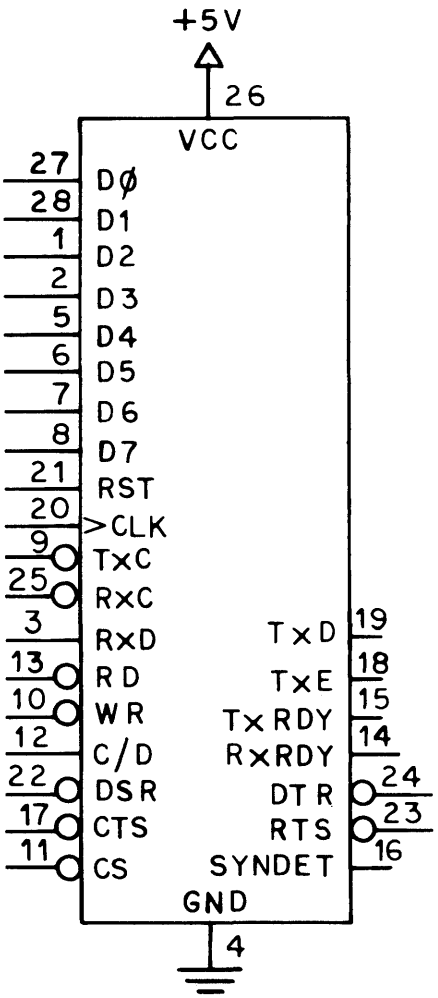
D2,D6	.46 Unit Load
STSTB	.31 Unit Load
Others	.16 Unit Load

Outputs

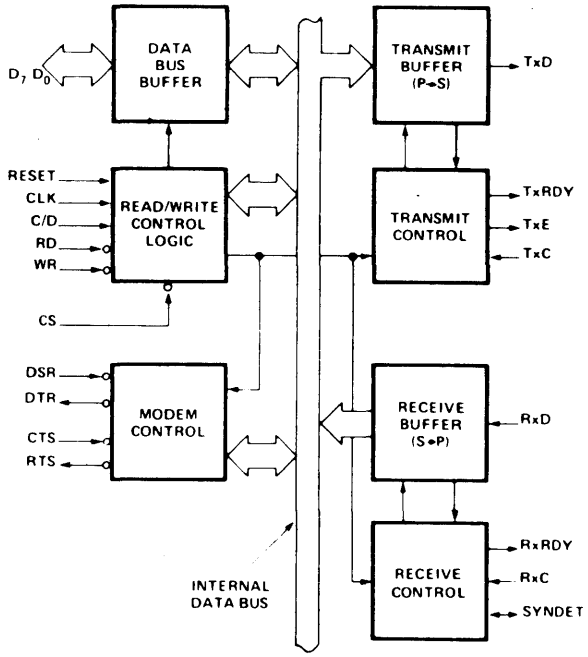
D0-D7	1.25 Unit Loads
Others	9 Unit Loads

The USART is used to interface the serial data channel of a terminal or communications device to the parallel data channel of a computer or terminal. The transmitter section converts parallel data into serial words with start bits, stop bits, and (if desired) parity bits. The receiver section converts serial data into parallel words, while stripping off the start bits and stop bits, checking word length, and, if desired, checking parity. Both the receiver and transmitter are double buffered. Parallel words can contain up to eight bits. Serial word length can be 5, 6, 7, or 8 bits. Parity can be even or odd, or parity checking and generation can be inhibited. The number of stop bits can be either one or two (or 1-1/2 when word length = 5 bits). Transmitting and receiving can occur simultaneously (full-duplex). Transmit and Receive Clocks must be supplied at 1, 16, or 64 times the desired baud rate.

Logic Symbol



Block Diagram



Loading:

Outputs 1 Unit Load

Data Bus Buffer

This is a three-state, bidirectional, 8-bit buffer used to interface the 8251 to the MPU system data bus. Data, control words, command words, and status information are transferred through this buffer.

Read/Write Control Logic

Control inputs from the MPU system are received and stored here Control/command bits stored here influence subsequent 8251 operation.

RST (Reset). A high on this input forces the 8251 into an "idle" condition, where it remains until a Mode instruction is received.

CLK (Clock). This input is normally driven by the Ø2 (TTL) output of the 8224 Clock Generator, to provide timing for internal operations. This clock must be greater than 30 times the RxC and TxC frequency for synchronous operation and 4.5 times for asynchronous operation.

WR (Write). A low on this input signals the 8251 that the MPU is writing (outputting) to the 8251.

RD (Read). A low on this input signals the 8251 that the MPU is reading (inputting) from the 8251.

C/D (Control/Data). This input, along with the WR and RD inputs, informs the 8251 whether the word on the data bus is a data, control, or status word.

C/D	WR	RD	Function
L	X	X	Data
H	H	L	Status
H	L	H	Control

CS (Chip Select). A low on this input enables the 8251. A high disables all reading and writing and drives all outputs into the high-impedance state.

Modem Control

These inputs and outputs can be used to interface to the modem, or they can be used for other functions as desired.

DSR (Data Set Ready). This input is normally used to test modem conditions such as Data Set Ready. Its condition is tested by the MPU performing a status read operation.

CTS (Clear to Send). A low on this input enables the 8251 to transmit serial data if the TxN bit in the command byte is set to a 1.

DTR (Data Terminal Ready) and RTS (Request to Send). These two outputs can be set low by programming the appropriate bits in the command instruction word. They are normally used for modem control.

Transmit Buffer

This buffer accepts parallel data from the Data Bus Buffer, converts it to a serial bit stream, inserts the appropriate characters or bits, and outputs a composite serial stream of data on the TxD pin. It consists essentially of two buffers, a transmit buffer and a holding register.

Transmit Control

This section controls the Transmit Buffer and provides the signals necessary to synchronize transmission with the MPU.

TxRDY (Transmit Ready). This output goes high to inform the MPU that the transmit holding register is ready to accept the next character. The MPU can also check this condition by performing a status read operation. This output goes low (at least momentarily) when a character is received from the MPU, and returns high when the character is transferred from the holding register to the transmit buffer.

TxE (Transmitter Empty). This output goes high when the transmitter has no more characters to transmit. It goes low when a character is received from the MPU.

TxC (Transmit Clock). The signal applied to this input controls the rate of data transmission. In synchronous transmission, the baud rate is the same as the TxC rate. In asynchronous transmission, the TxC rate can be 1, 16, or 64 times the baud rate, determined by the Mode instruction. The serial data is shifted out of the 8251 on the falling edge of TxC.

Receive Buffer

This buffer accepts serial data from the RxD input, converts it to parallel format, checks for bits or characters according to the established mode and control words, and provides this data to the MPU.

Receive Control

This section controls the Receive Buffer and provides the signals for synchronizing it with the MPU.

RxRDY (Receiver Ready). This output goes high to inform the MPU that the 8251 has a character ready to be input to the MPU. This condition can also be checked via a status read operation. The output is driven low when the character is received by the MPU (when RD is driven low).

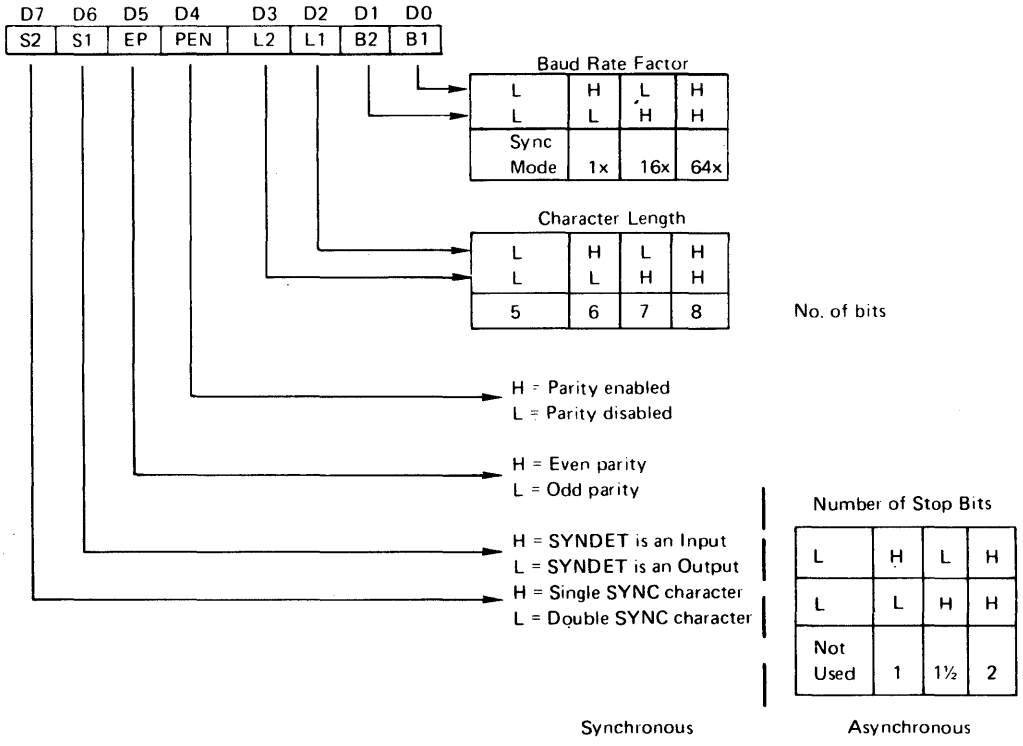
RxC (Receiver Clock). The signal applied to this input controls the rate of data reception. In synchronous mode, the RxC rate must be the same as the baud rate. In asynchronous mode, the RxC rate can be 1, 16, or 64 times the baud rate, as determined by the Mode instruction. The data on the RxD input is sampled and shifted into the 8251 on the rising edge of RxC.

SYNDET (SYNC Detect). This pin is used in synchronous mode only, and it can be used as either an input or an output, programmable through the Control word. When used as an output, it goes high to indicate that the 8251 has received a SYNC character. If the 8251 is programmed to use double SYNC characters, then SYNDET goes high in the middle of the last bit of the second SYNC character. The condition of this output is also available to the MPU via a status read operation, which automatically resets the SYNDET condition.

SYNDET may be used as an input if the check for synchronization is made by external logic. In this case, when SYNDET is driven high, the 8251 begins assembling serial input data into characters on the falling edge of the next RxC.

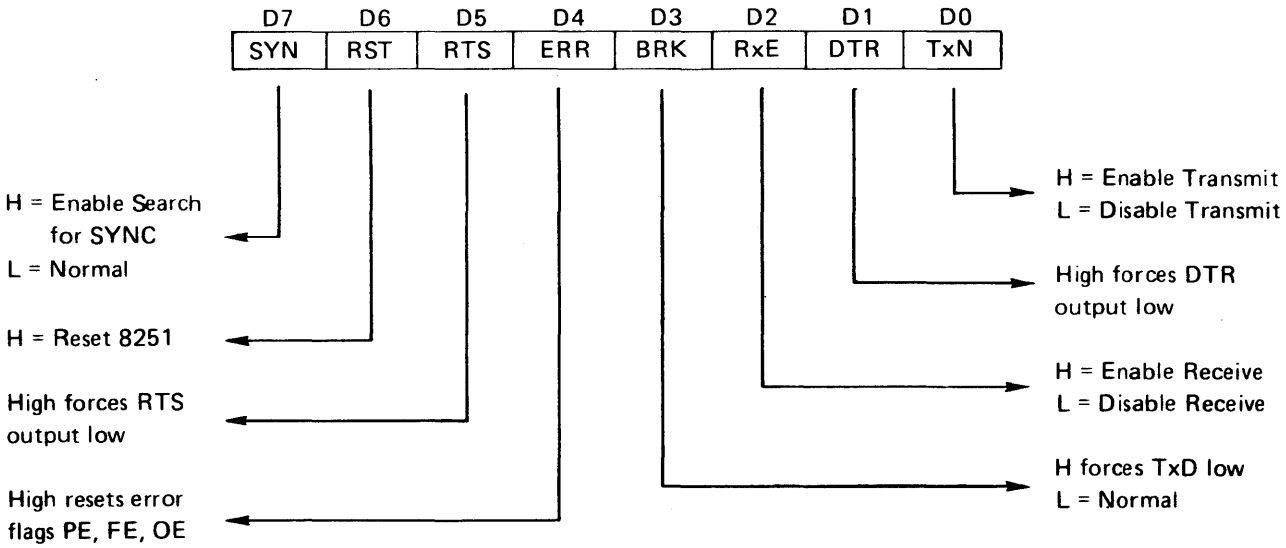
Mode Instruction

The first "control" (C/D high) write after a Reset loads the Mode instruction into the 8251. Any subsequent control writes load Command instructions. The Mode instruction format is as follows:



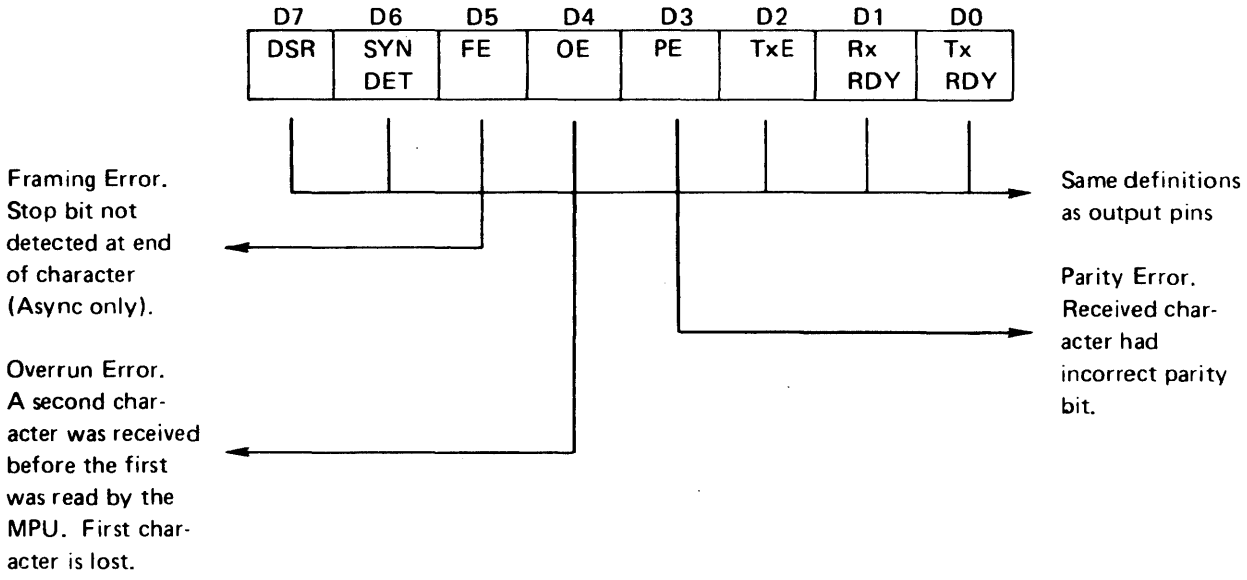
Command Instruction

After the mode instruction has been loaded, subsequent control writes load the Command instruction, as follows:

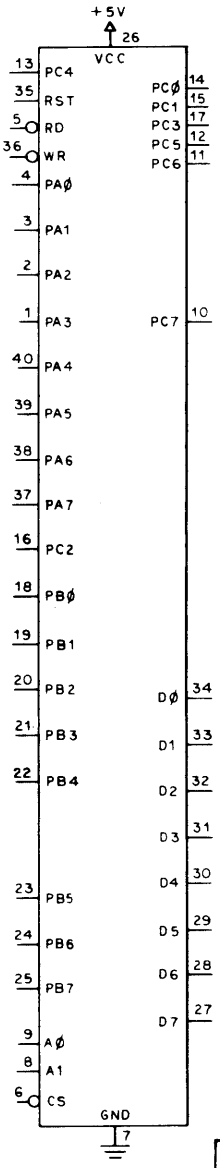


Status Read

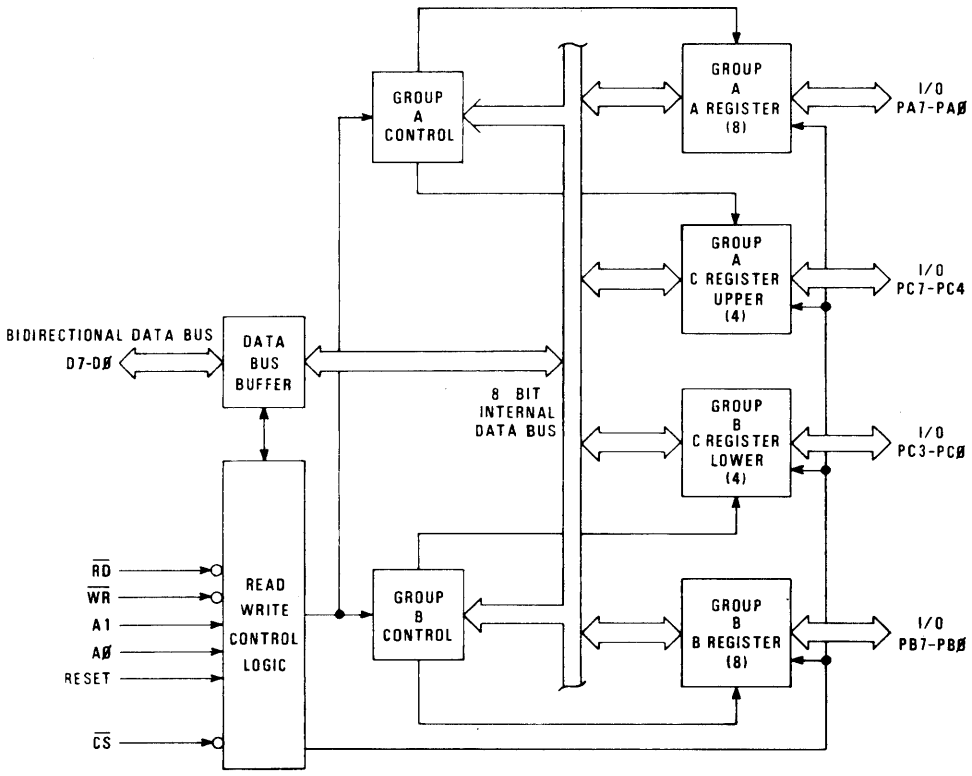
When a Read operation is performed with the C/D input high, status is provided to the MPU on the parallel data bus as follows:



Logic Symbol



Block Diagram



PIN NAMES

D7 – D0	DATA BUS (BIDIRECTIONAL)
RESET	RESET INPUT
CS	CHIP SELECT INPUT
RD	READ INPUT
WR	WRITE INPUT
A0,A1	REGISTER ADDRESS
PA7-PA0	A REGISTER (BITS)
PB7-PB0	B REGISTER (BITS)
PC7-PC0	C REGISTER (BITS)
V_{CC}	15 VOLTS
GND	0 VOLTS

The 8255 is a general purpose, programmable interface designed for use with 8080 microprocessor systems to provide communication between the 8080 and a variety of peripheral devices. An eight-bit bidirectional data bus buffer interfaces the 8080 system bus with the 8255 internal data bus. Three eight-bit registers — called A, B, and C — can be connected directly to the peripheral device. The three registers can be configured by system software or firmware to suit the input/output requirements of a specific peripheral device. The C register can be split into two four-bit registers, and can also be used for control and status signals in applications requiring them. The microprocessor can read from or write to any of the three registers via the data bus buffer.

Communication between the microprocessor and the interface is maintained over the eight bidirectional data bus lines, four control lines, and two address lines. The microprocessor selects the 8255 operating mode by sending a Control Word over the data bus lines. The Control Word is also used to define registers as being input, output, bidirectional, or control. Only the A register can be bidirectional, and only the C register can be used for control. Individual bits of the C register can be set or reset by a Control Word.

There are three operating modes. Registers are controlled in two groups of 12 bits each. Control Group A controls the eight bits of the A register and the four high-order bits of the C register (C7 — C4); Control Group B controls the eight bits of the B register and the low-order half (C3 — C0) of the C register. Since the structure of the Control Word permits separate programming of the two groups, the 8255 can operate in two modes simultaneously. Operating mode is set during system initialization, and can be changed during program execution by sending a new Control Word over the data lines.

The operating modes are as follows:

Mode 0 — Basic Input/Output. The A and B registers can be separately defined as input or output. The C register can be split into two four-bit registers, one input and the other output, or it can be used for all input or all output. Sixteen different register configurations are available. No strobes or handshaking are involved.

Mode 1 — Strobed Input/Output. The A and B registers can be individually programmed for input or output. Six bits of the C register are used as control and status bits for the A and B registers; the remaining two bits of the C register can be programmed as either input or output.

Mode 2 — Strobed Bidirectional Input/Output. The A register can be used for two-way communication with a peripheral device. Five bits of the C register are used for control and status for the A register; the remaining three bits of the C register can be used for input, output, or control, depending on the mode of the B register. When the B register is in Mode 0, the C register bits could be input or output. In mode 1, the three bits of the C register would be used for control and status of the B register.

In Mode 1 or Mode 2, when the C register is used for control and status, the peripheral device is permitted to interrupt the 8080. The 8080 program can enable/disable interrupts by setting/resetting individual C register bits.

Loading:

When a register is programmed for output, up to eight output buffers, selected randomly from the B and C registers, can furnish 1mA at 1.5 volts to drive Darlington type or similar circuits. Other outputs can drive 1 unit load.

A non-programmed MOS/LSI Scanner, in a 28-lead dual-in-line package. Used in Cortron Up/Dn stroke keyboard. Supply Voltages:
Vss = 5V at 40 ma.
Vdd = 0V at 50 ma (for TTL outputs).
Vgg = -12V at 40 ma.

The device has 12 TTL/DTL outputs which are capable of sinking 1.6 ma. These outputs are:

Pin	Pin
19. SR out	14. Strobe
12. Ø1	18. Flag (SRIN)
13. Ø3	and B1 through B7

Each of these outputs has the following specifications:

Logic "1" (high) = 2.4V min. at 100 μa
Logic "0" (low) = 0.4V max. at 1.6 ma

The device has 7 standard TTL/DTL compatible outputs, each capable of sinking 3.2 ma. These outputs are A1 through A7.

Each of these outputs has the following specifications:

Logic "1" (high) = 2.4V min. at 200 μa
Logic "0" (low) = 0.4V max. at 3.2 ma

This device has 6 logic inputs

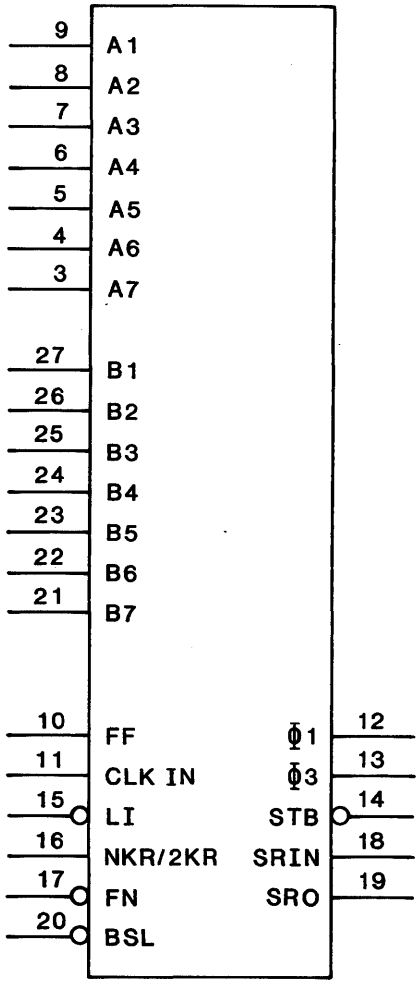
Pin	Pin
17. Function	20. Bypass shift logic
10. Data in (FF)	15. Latch Inh
11. Clock in	16. NKR/2KRO

Each input has the following specification:

Vin (Logic 1) = Vss -2V min.
= Vss +0.3V max.
Vin (Logic 0) = Vss -4.0V max.
= Vgg min.

A pull-up resistor is provided for each input on the device.

Logic Symbol



083-048

Keyboard Encoder Part No. xxxxxx Type SD25010-K

An LSI programmable circuit in a dual-in-line package. Used in the MICROSWITCH keyboard in the Model 1660.

POWER SUPPLY
+5 VDC at 1Amp, Max.

OUTPUT SPECIFICATIONS
Data Bits D0-D7 and Strobe.

1. Logic '1' (high) = 2.4V min. at 40 μa
2. Logic '0' (low) = 0.4V max. at 1.6 ma

X0-X15 will handle a full matrix of Hall effect logic scan switches.

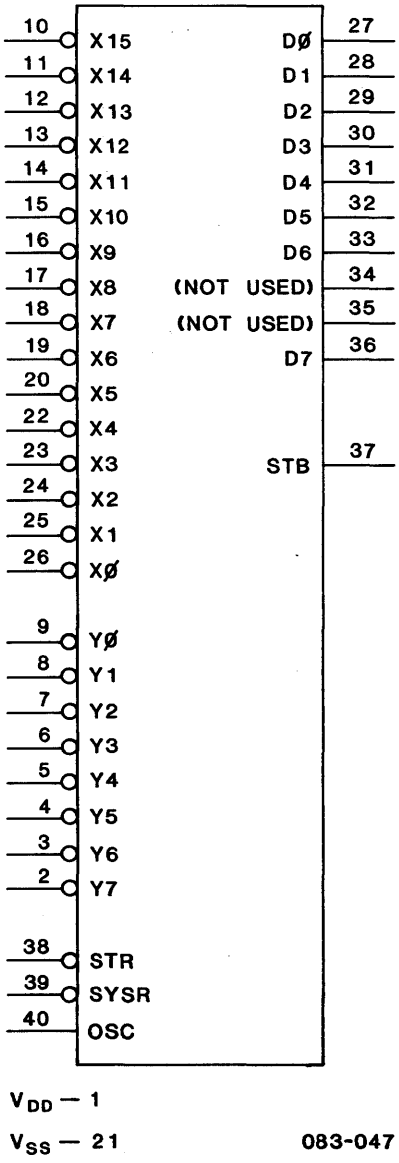
Y0-Y7 will handle a full matrix of Hall effect logic scan switches.

INPUT SPECIFICATIONS

Strobe Reset and System Reset (POR) inputs.
High level voltage = 2.0V
Low level voltage = 0.8V
High level current = 0.25 ma source
Low level current = 1.6 ma source

Clock Input - External Drive Option.
High level input voltage = Vdd -1.0V
Low level input voltage = 0.8V

Logic Symbol



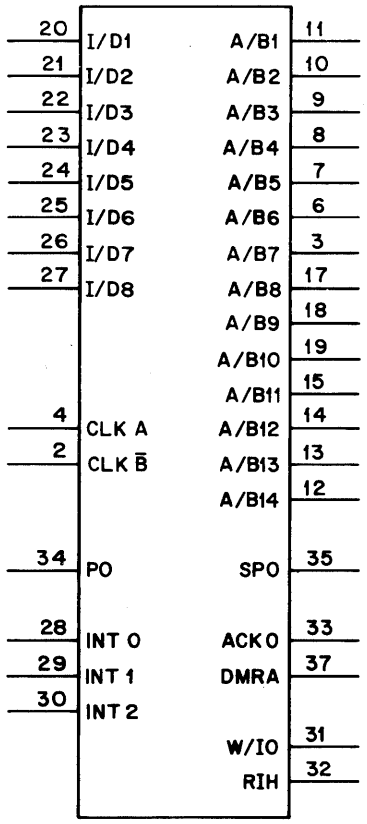
083-047

The PPS-8 Central Processor Unit, is a complete 8-bit parallel processor on a single MOS chip. The Central Processor Unit (CPU) uses four-phase dynamic logic for operation.

The CPU contains:
(a) Logic necessary to receive and decode the instructions
(b) 8-bit parallel adder-accumulator for arithmetic and logical operations
(c) 14-bit P-Register for sequencing through the ROM program
(d) 16-bit L-Register for subroutine linkage, RAM operand addressing, and ROM indirect addressing
(e) Three 8-bit registers, (X, Y and Z) for RAM operand addressing
(f) 5-bit stack pointer S for addressing a dedicated RAM area
(g) Logic for processing a priority interrupt structure
(h) Direct memory access (DMA) mode
(i) Multiplexed receivers and drivers for interfacing with the 14-bit multiplexed address bus and the 8-bit bi-directional data/instruction bus.

The CPU, through time multiplexing, utilizes an 8-bit bi-directional bus to transfer instrctions from ROM to CPU (and I/O) during 04, and to transfer data between the CPU, RAMs and I/O devices during 02.

Logic Symbol



VDD – 16
VSS – 41

(083-042)

FUNCTIONAL DESCRIPTION

Instructions for the PP-8 CPU are either one, two, or three bytes in length, and require from one to three clock cycles for execution. The CPU decodes instructions, senses interrupt and DMA requests, and controls data transfer, arithmetic, logical, and indexing operation.

The adder, with the 8-bit accumulator register (A), and associated logic circuits forms the Arithmetic and Logical Unit (ALU). The A register is the primary working register in the CPU and the central data interchange for most data operations. The adder is an 8-bit parallel binary adder with an internally connected carry flipflop (C), used for precision arithmetic operation, packed BCD (decimal) arithmetic, and hexadecimal data manipulation. Accumulator circular shifting right and left with carry linkage is also available.

P-REGISTER (14-BITS)

The P-Register contains the address of the instruction currently being executed, and automatically increments (least significant 7-bits) to fetch the next byte from instruction memory (ROM). It may be altered during the execution of Branch, Return or Skip instructions.

L-REGISTER (16-BITS)

The L-Register saves the return address after a subroutine call or an interrupt. It is also used as an address register for indirect ROM operands, as an alternate RAM address register, or as a general purpose programming register.

Z-REGISTER (8-BITS)

This register holds the 7 most significant bits of the 14-bit RAM operand address or may be used as a general purpose programming register.

X-REGISTER (8-BITS)

The X-Register holds the 7 least significant bits of the 14-bit RAM operand address. The most significant bit (8th bit) is used as an upper RAM address control bit.

Logic 1 - the Z-Register contents are output for the most significant 7 bits of the RAM address.

Logic 0 - logic zero is output for the most significant 7 bits of the RAM address.

This register may be loaded, stored, and automatically incremented or decremented under program control.

Y-REGISTER (8-BITS)

The Y-Register is used as an alternate lower RAM address register and as a "loop counter" or it may be used as a general purpose programming register.

S-REGISTER (5-BITS)

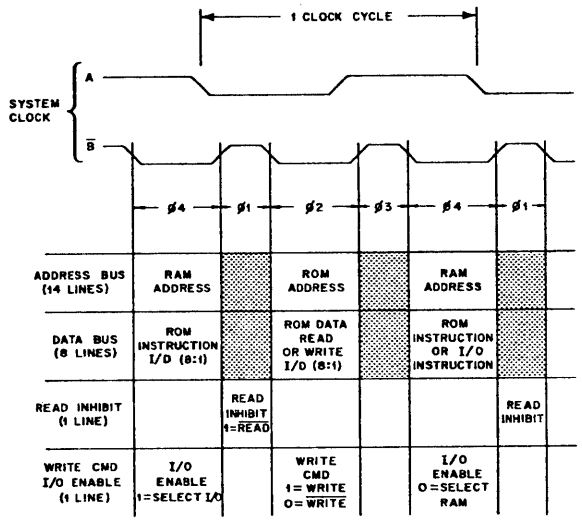
The 5-bit up-down counter S-Register is used as an address pointer to a 32 byte "stack" in RAM. This stack pointer is automatically incremented each time a byte is "pushed" into the stack and decremented each time a byte is "popped" from the stack.

W-REGISTER (8-BITS)

The W-Register serves primarily as an internal buffer register. Additionally, it is used in conjunction with the LAL and PSHL instructions.

POWER-ON RESET (PO)

The Power-On input signal is used to initialize the CPU to a known starting address and state during a power-on sequence. The Power-On (PO) signal is generated external to the CPU. The CPU receives this signal, initializes the internal logic states, and at the same time generates a Synchronized Power-On output (SPO) signal which is used to initialize other circuits of the PPS-8.



PPS-8 BUS TIMING BASIC

PPS-8 INSTRUCTIONS SET LIST

Data Transfer Group

L	Load A
LN	Load A, Increment Address
LD	Load A, Decrement Address
LNXL	Load A, Increment Address, Exchange L
LDXL	Load A, Decrement Address, Exchange L
LNCX	Load A, Increment & Compare Address, Exchange L
LDCX	Load A, Decrement & Compare Address, Exchange L
LNXY	Load A, Increment Address, Exchange Y
S	Store A
SN	Store A, Increment Address
SD	Store A, Decrement Address
SNXL	Store A, Increment Address, Exchange L
SDXL	Store A, Decrement Address, Exchange L
SNCX	Store A, Increment & Compare Address, Exchange L
SDCX	Store A, Decrement & Compare Address, Exchange L
SNXY	Store A, Increment Address, Exchange Y
X	Exchange
XN	Exchange, Increment Address
XD	Exchange, Decrement Address
XNXL	Exchange, Increment Address, Exchange L
XDXL	Exchange, Decrement Address, Exchange L
XNCX	Exchange, Increment & Compare Address, Exchange L
XDCX	Exchange, Decrement & Compare Address, Exchange L
XNXY	Exchange, Increment Address, Exchange Y

Stack Group

PSHA	Push A
PSHX	Push X
PSHY	Push Y
PSHZ	Push Z
PSHL	Push L
POPA	Pop A
POPX	Pop X
POPY	Pop Y
POPZ	Pop Z
POPL	Pop L

Arithmetic Group

A	Add
AC	Add with Carry
ASK	Add, Skip on Carry
ACSK	Add with Carry, Skip on Carry
AISK	Add Immediate, Skip on Carry
INCA	Increment A
DC	Decimal Correct (1)
DCC	Decimal Correct (2)

Logical Group

AN	Logical AND
ANI	Logical AND Immediate
OR	Logical OR
EOR	Logical Exclusive OR
COM	Complement

Increment/Decrement Group

INCX	Increment X
DECX	Decrement X
INXY	Increment X, Exchange Y
DEXY	Decrement X, Exchange Y
INCY	Increment Y
DECY	Decrement Y

Skip/Branch Group

B	Branch
BDI	Branch, Disable Interrupts
NOP	No Operation
SKC	Skip if Carry

Register Group

LX	Load X
LY	Load Y
LZ	Load Z
LAI	Load A Immediate
LXI	Load X Immediate
LYI	Load Y Immediate
LZI	Load Z Immediate
LAL	Load A through Link
LXL	Load X through Link
LYL	Load Y through Link
LZL	Load Z through Link
LXA	Load X from A
LYA	Load Y from A
LZA	Load Z from A
LLA	Load L from A
XY	Exchange Y
XL	Exchange L
XAX	Exchange A and X
XAY	Exchange A and Y
XAZ	Exchange A and Z
XAL	Exchange A and L

Subroutine Group

BL	Branch and Link
RT	Return
RSK	Return & Skip
RTI	Return, Enable Interrupts
SKNC	Skip if No Carry
SKZ	Skip if Zero
SKNZ	Skip if Non-Zero
SKP	Skip if Positive
SKN	Skip if Negative
SKE	Skif if Equal
BBT	Branch if Bit (n) True
BBF	Branch if Bit (n) False
BC	Branch if Carry
BNC	Branch if No Carry
BZ	Branch if Zero
BNZ	Branch if Non-Zero
BP	Branch if Positive
BN	Branch if Negative
BNE	Branch if Not Equal

Input/Output Group

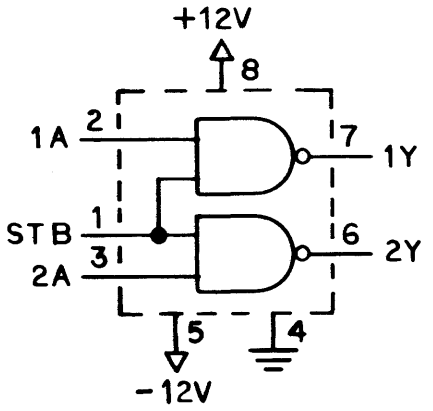
IO4	Digit I/O (C, D)
IN	Input (C, D)
OUT	Output (C,D)
RIS	Read Interrupt Status

Bit Manipulation Group

SC	Set Carry
RC	Reset Carry
RAR	Rotate A Right
RAL	Rotate A Left
MDR	Move Digit Right
MDL	Move Digit Left
SB	Set Bit (n)
RB	Reset Bit (n)

This line driver is commonly used to interface data terminal equipment to data communication equipment utilizing the EIA Standard RS-232-C. Input is TTL/DTL compatible, and output is ±12V.

Logic Symbol

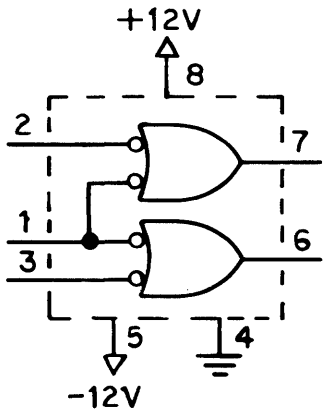


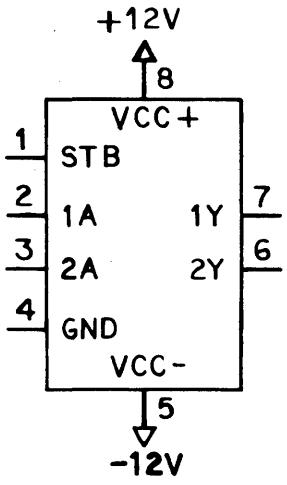
Truth Table

INPUTS		OUTPUT
STB	A	Y
L	X	+12
H	L	+12
H	H	-12

L = 0V
H = +5V
X = Irrelevant

Alternate Symbols



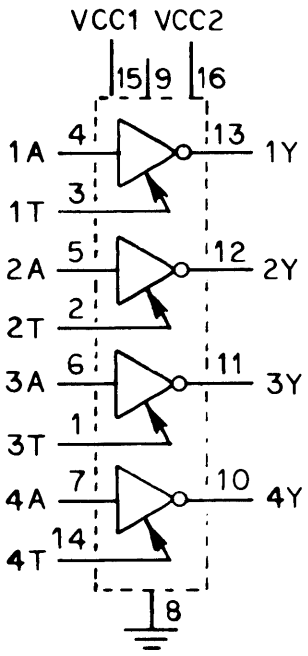


Loading:

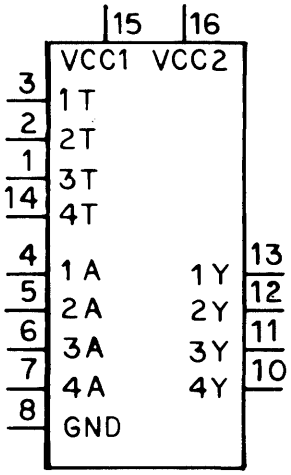
Inputs	1 Unit Load
Strobe	2 Unit Loads

This receiver satisfies the requirements of the interface between data communication equipment and data terminal equipment as defined by EIA Standard RS-232-C. Input is from +25V to -25V, and output is either 0V or +5V. For normal operation, the threshold control terminal is connected to VCC1. This provides a wide hysteresis loop which is the difference between the positive-going and negative-going threshold levels. In this mode of operation, if the input voltage goes to zero (or open-circuit), the output will remain either low (0V) or high (+5V) as determined by the previous input. For fail-safe operation, the threshold terminal is left floating. This reduces the hysteresis loop, causing the negative-going threshold to be above 0V. The positive-going threshold is unchanged. In this mode, if the input voltage goes to 0V or is open-circuited, the output goes high (+5V) regardless of the previous input condition. VCC can be either +5V or +12V. Pin 9 should not be connected externally.

Logic Symbol



Alternate Symbol

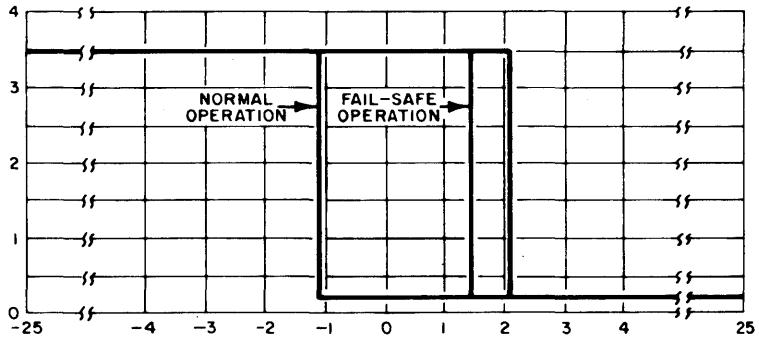


A = input
Y = output
T = threshold control
VCC1 = +5V
VCC2 = +12V

Truth Table
(each receiver)

INPUT A	OUTPUT Y
-12	H (+5)
+12	L (0)

Waveforms

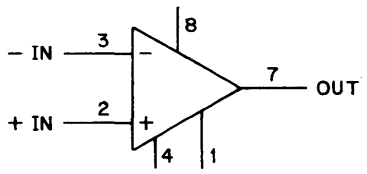


Loading:
Outputs 10 Unit Loads

Voltage Comparator | Part No. 10188 | Type LM311

This comparator can be used with power supplies providing two output voltages, up to ± 15 volts. It can be used with single output supplies up to +5 volts.

Logic Symbol

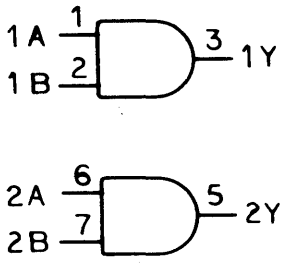


V+, PIN 8
V–, PIN 4
GND, PIN 1

(083–041)

Dual AND-Gate Peripheral Driver | Part No. 10181 | Type 75451

Logic Symbol



VCC-8, GND-4

Truth Table

A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

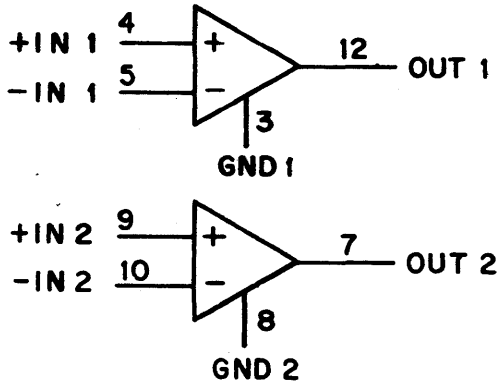
Loading:

Input	1 Unit Load
Output	300 ma

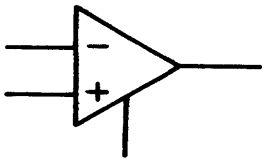
High-Speed Dual Comparator | Part No. 10168 | Type LM319

This device can operate on voltage supplies up to ±15V, but can also operate off of a single +5V supply, depending upon the application. Note the non-standard voltage connections.

Logic Symbol



Alternate Symbol

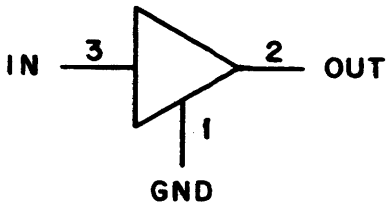


V+, pin 11
V- , pin 6

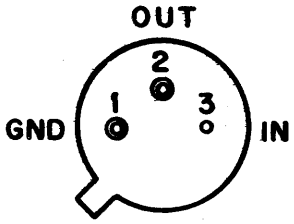
3-Terminal Negative Voltage Regulator, 5 Volt | Part No. 42155-05 | Type LM320H-5
3-Terminal Negative Voltage Regulator, 12 Volt | Part No. 42155-12 | Type LM320H-12

This series of negative regulators provides precision regulation of output currents up to .5A, while also providing current limiting and thermal overload protection.

Logic Symbol



Pinout
(Bottom View)



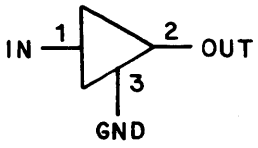
Maximum Voltages

	-05	-12
IN	-7 to -25	-14 to -35
OUT	-4.8 to -5.2	-11.6 to -12.4

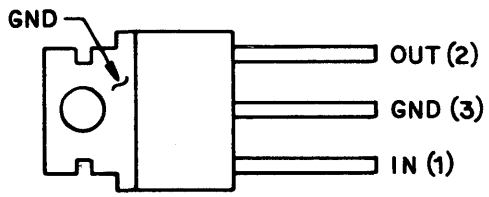
3-Terminal Positive Voltage Regulator, 12 Volt | Part No. 10284-03 | Type LM340T-12

This series of positive regulators provides precision regulation of output currents up to 1A, while providing current limiting and thermal overload protection.

Logic Symbol



Connection Diagram



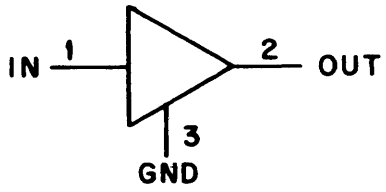
Input = +14.4 to +27.5V

Output = +11.4 to +12.6V

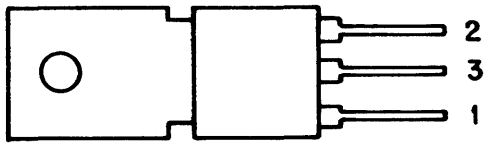
3-Terminal Positive Voltage Regulator, 5 Volt | Part No. 42154-05 | Type LM341P-5
3-Terminal Positive Voltage Regulator, 12-Volt | Part No. 42154-12 | Type LM341P-12

This series of positive regulators provides precision regulation of output currents up to .5A, while also providing current limiting and thermal overload protection.

Logic Symbol



Pinout
(Top View)

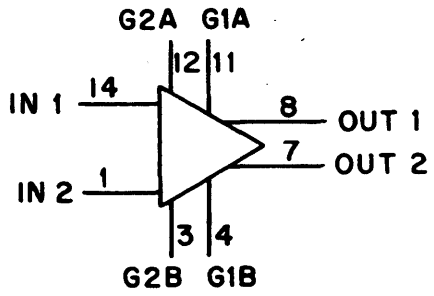


	-12	-5
Input (1)	+14.8 to +27V	+7 to +17V
Output (2)	+11.4 to +12.6V	+4.75 to +5.25V

Differential Video Amplifier | Part No. 10124 | Type LM733C

This differential-input/differential-output amplifier provides selectable gains of 10, 100, and 400.

Logic Symbol



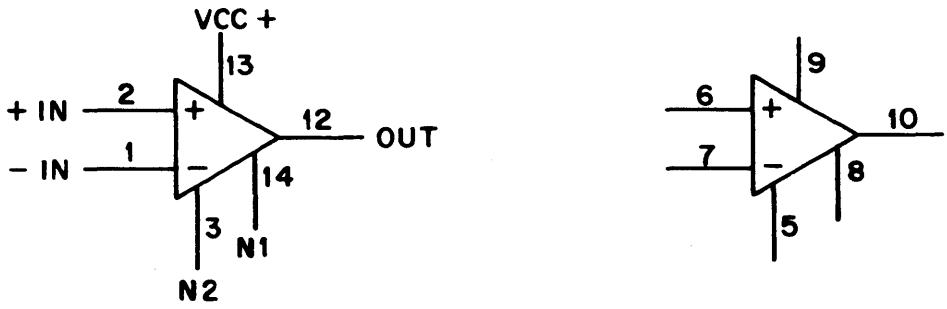
Gain Selection

Gain	Connection
10	None
100	G1A to G1B
400	G2A to G2B

V+, 10
V-, 5
(No connection to pins 2, 6, 9, and 13)

Dual Op Amp, General Purpose | Part No. 10165 | Type 72747
Dual Op Amp, Selected | Part No. 13072 | Type 72747

Logic Symbol

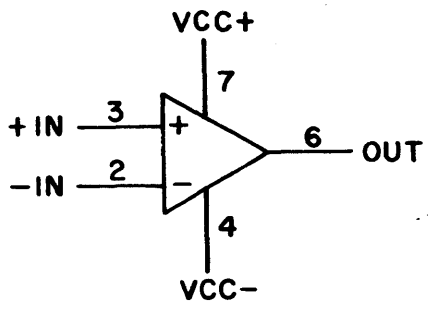


VCC-4, No Connection -11

Op Amp, General Purpose | Part No. 10166 | Type 72748

This single op amp is housed in an 8-pin DIP.

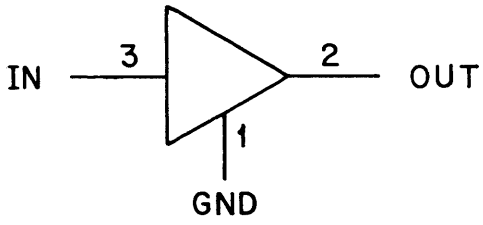
Logic Symbol



Pin 1 = Offset null/Comp
Pin 5 = Offset null (N2)
Pin 8 = Comp

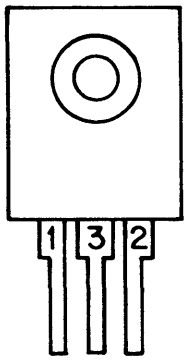
Voltage Regulator, -12V Part No. 13142 Type MC7912CB

Logic Symbol



V_{IN} = -14.5 TO -30V
V_O = -11.5 TO -12.5V

Pin Out

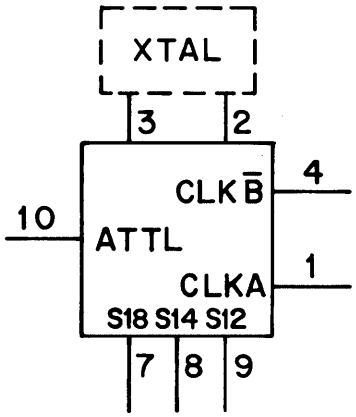


(083-039)

The Clock Generator circuit generates the "A" and "B" clock waveforms required by circuits in the PPS. The Clock Generator has an internal oscillator which is stabilized by connecting a 3.579545 MHz color TV quartz crystal to the appropriate inputs. Primary clock A output is a square wave. Clock B output is a pulse output occurring during each phase of clock A, with unique timing features required by the circuits within the PPS system. Clock A is also available, through a TTL output, for synchronizing equipment external to PPS.

The input straps provide a countdown of the oscillator frequency equal to the number associated with the strap; ie, S12 divides by 12, E14 divides by 14, and S18 divides by 18. Thus, with a crystal frequency of approximately 3.58 MHz and input S14 terminated to V_{DD}, the clock A output frequency is 256 kHz, (3.58 MHz ÷ 14 = 256 kHz).

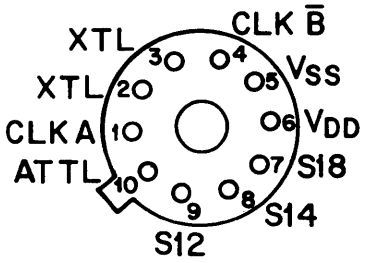
Logic Symbol



V_{DD} — PIN 6

V_{SS} — PIN 5 (GND)

Bottom View



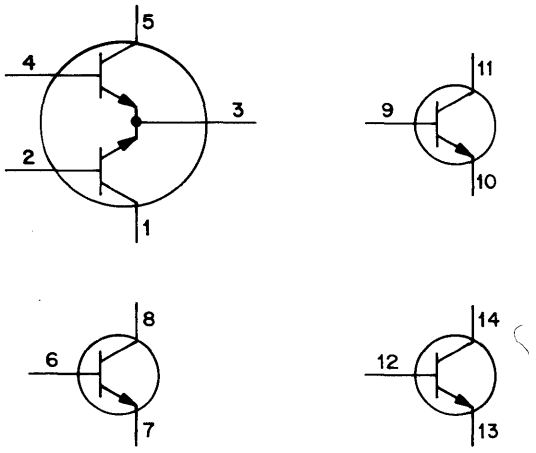
FREQUENCY SELECT STRAPS — PINS 7, 8, 9

(083-036)

NPN Transistor Array | Part No. 42191-32 | Type CA3086

This device consists of five general-purpose silicon NPN transistors on a common monolithic substrate. Two of the transistors are internally connected to form a differentially-connected pair.

Logic Symbol

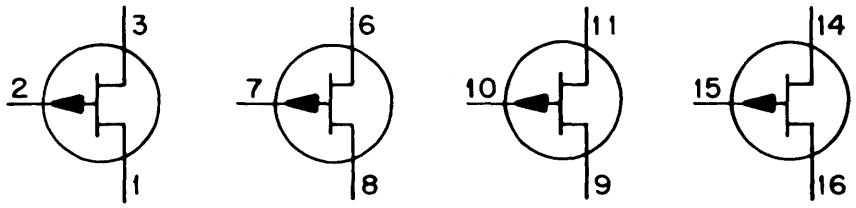


(083-040)

Quad Field Effect Transistor (FET) | Part No. 10190 | Type 8041

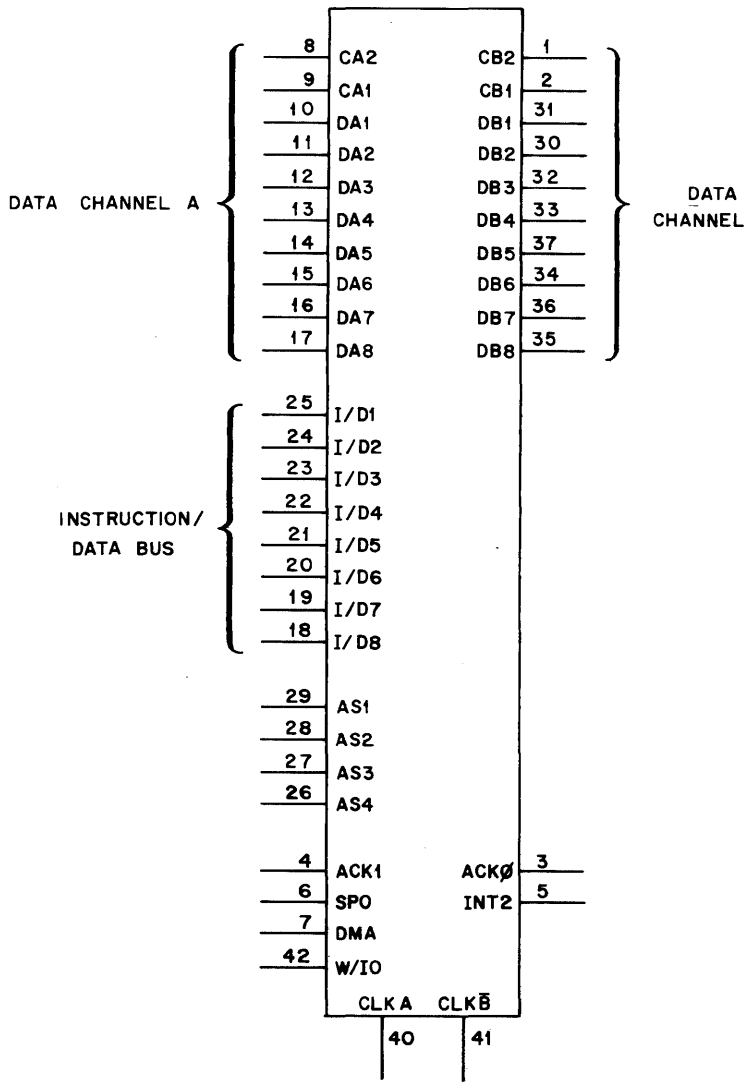
This IC contains four independent p-channel FETs.

Logic Symbol



The Parallel Data Controller (PDC), is a flexible parallel input/output device for interfacing the PPS-8 system to external devices or for interfacing between multiple PPS systems. The device provides two independent, bi-directional input/output channels, each of which operates in a variety of parallel data transfer modes. Each channel consists of ten TTL-compatible lines; eight data lines and two control lines (DA1 through DA8, CA1 and CA2; DB1 through DB8, CB1 and CB2). Each channel has its own data buffer (eight bits) and function register (eight bits); the two channels share a common device status register (5 bits) and an interrupt status register (4 bits.) The function (mode) of each channel is programmable and is selected by control data loaded into the associated function register under CPU program control. Direct addressing for up to 15 PDCs is possible by the use of four chip select address straps (AS1 through AS4) that can be user-terminated to create each device address. Address 0000 is reserved for the "all call" command, Read Interrupt Status (RIS).

Logic Symbol



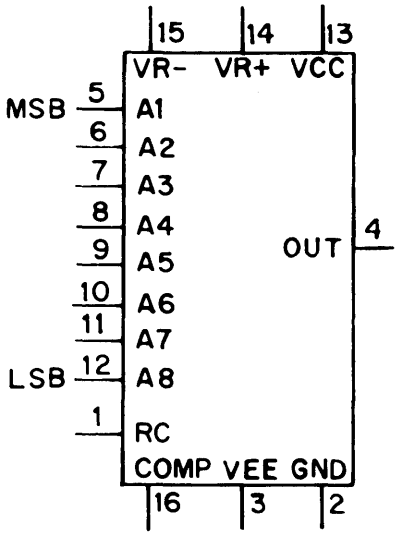
VDD – 38
VSS – 39

(083 – 044

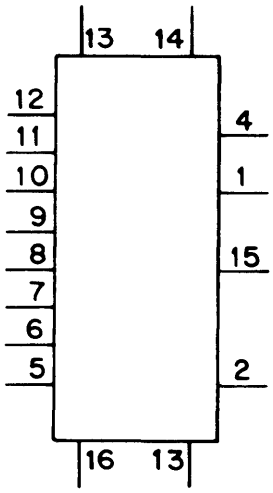
Digital-to-Analog Converter | Part No. 13060 | Type 1408L-6

This eight-bit multiplying D-to-A converter provides a current output which is the product of a digital word (applied to the A1-A8 inputs) and an analog reference voltage (applied to the VR+ and VR- inputs). Digital inputs are TTL and CMOS compatible. Output voltage swing is +0.5V to -0.6V with the Range Control (pin 1) grounded; leaving pin 1 open enables the negative voltage swing to reach -5V when maximum power supply voltages are applied. Frequency compensation capacitors are connected to pin 16. Note the non-standard VCC and GND connections.

Logic Symbol



Alternate Symbol



NOTE: VCC-13, GND-2

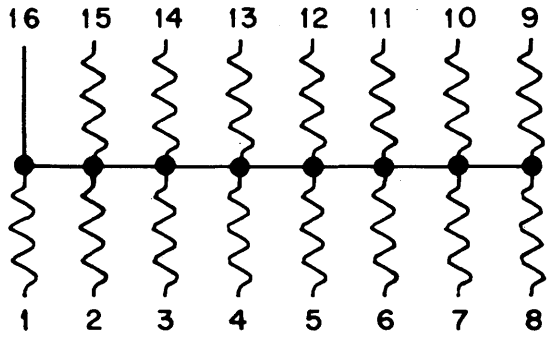
VCC = +5V
VEE = -5V to -15V (current source)
VR- = -15V (max.)
VR+ = +5V (max.)

Loading:

Inputs (digital)	1 Unit Load
Output	2.0 ma.

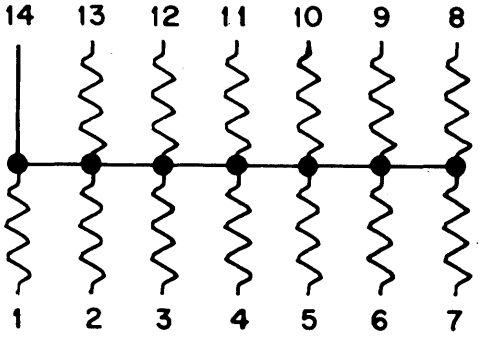
Resistor Network, 1K x 15 Part No. 10239-01

Pinout



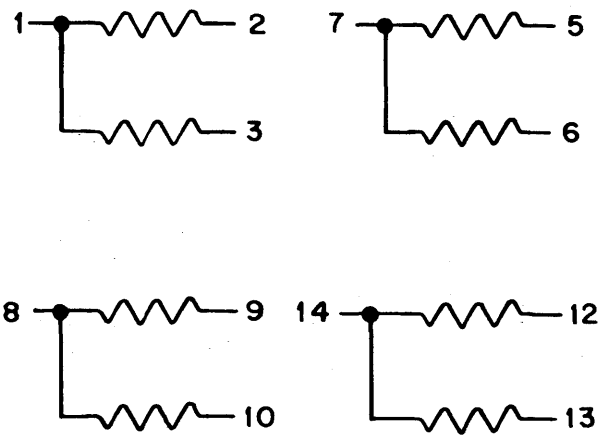
Resistor Network, 1K x 13 Part No. 10761

Pinout



Resistor Network, Quad 10K x 2 Part No. 13044

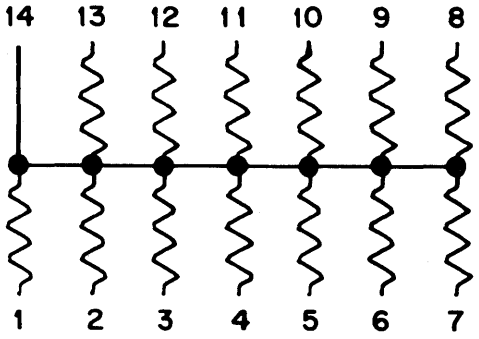
Pinout



(Pins 4 and 11, no connection)

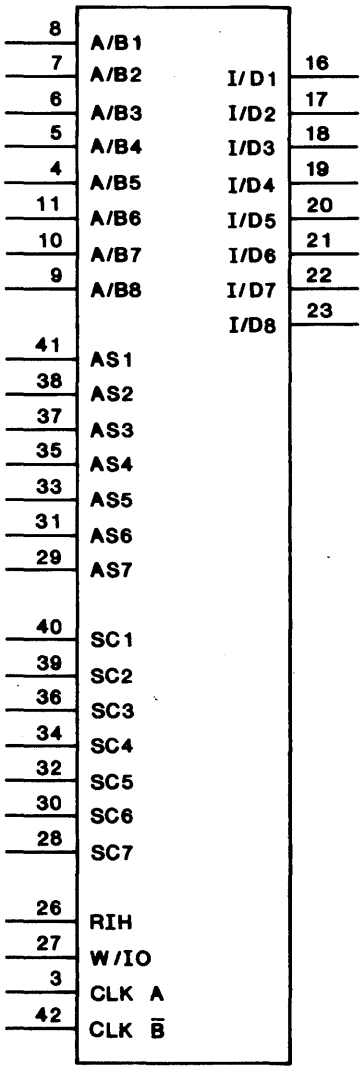
Resistor Network, 15K x 13 Part No. 13140

Pinout



The Random Access Memory (RAM) is a 2048 bit RAM organized in 256 x 8-bit configuration. It is designed for compatibility with the PPS-8 system, and the A and B system clocks. It is a dynamic memory with automatic refresh logic and a 1.8 μs access time. It is intended to be used as a read/write data storage device for the PPS-8 system.

Logic Symbol

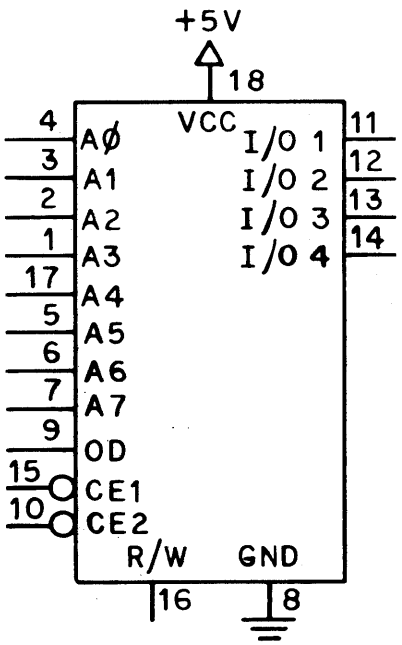


V_{DD} - 25
V_{SS} - 14

083-045

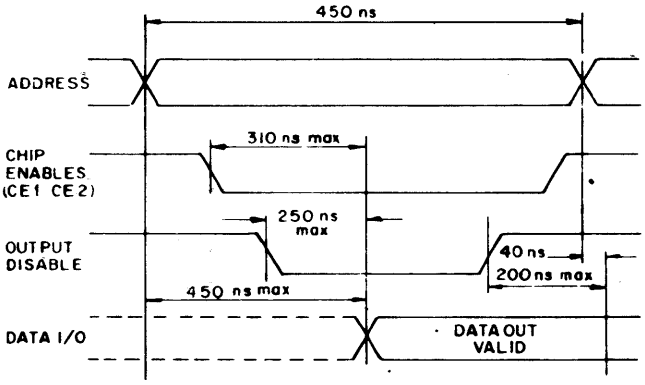
This is the 450 ns member of a family of random-access memories available in several speed ranges. The Output Disable pin (9), when high, drives the Input/Output pins to their high-impedance state.

Logic Symbol

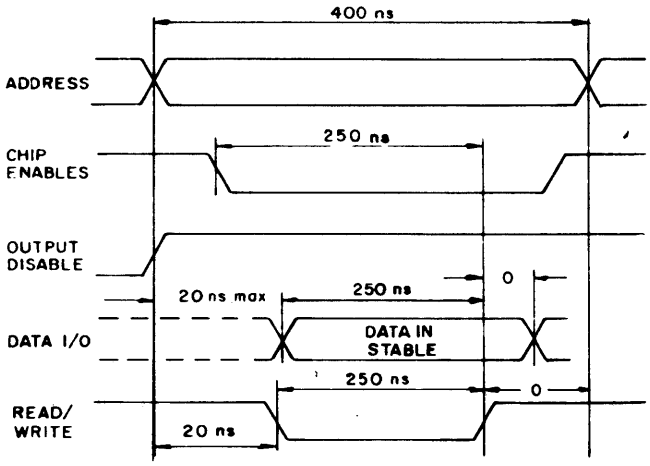


Timing Waveforms
(All times are minimum unless noted)

Read Cycle



Write Cycle



Loading:

Outputs 1.25 Unit Loads

512 x 8-Bit Programmable Read Only Memory, Three-State Part No. 10406 Type 82S115

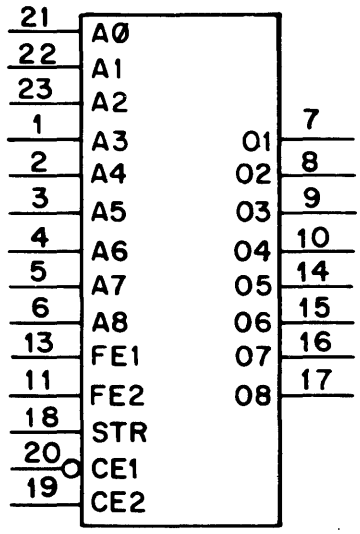
These devices are Programmable Read-Only memories which are normally programmed by the vendor. No truth table appears here because each program requires a separate table. Note that the part number above is the Diablo number for the unprogrammed pROMs: a new number is assigned when the pROM is programmed. Part numbers for programmed pROMs appear on the schematic. Access time is typically 35 ns (60 ns maximum).

There are two modes of operation. In the TRANSPARENT READ mode, stored data is addressed by applying a binary code to the address inputs while holding Strobe high. In this mode the bit drivers are controlled solely by CE1 and CE2 lines.

In the LATCHED READ mode, outputs are held in their previous state (1, 0, or Hi-Z) as long as Strobe is low, regardless of the state of address or chip enable. A positive Strobe transition causes data from the applied address to reach the outputs if the chip is enabled, and causes outputs to go to the Hi-Z state if the chip is disabled.

A negative Strobe transition causes outputs to be locked into their last Read Data condition if the chip was enabled, or causes outputs to be locked into the Hi-Z condition if the chip was disabled.

Logic Symbol



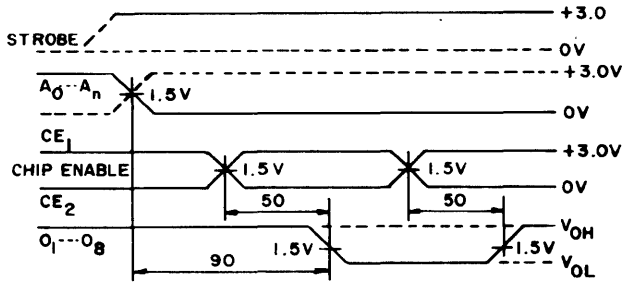
VCC-24, GND-12

AØ-A8 = Address Inputs
FE1, FE2 = Programming Inputs
STR = Strobe Input
CE1, CE2 = Chip Enable Inputs
O1-O8 = Data Outputs

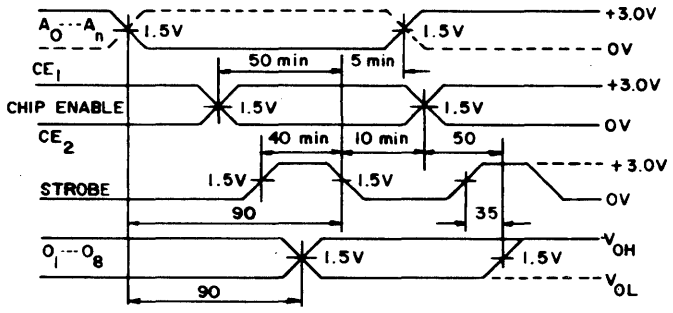
Loading:

Inputs	.1 Unit Load
Outputs	6 Unit Loads

Waveforms
(Times shown are maximum unless noted)
(Times shown are in nanoseconds)

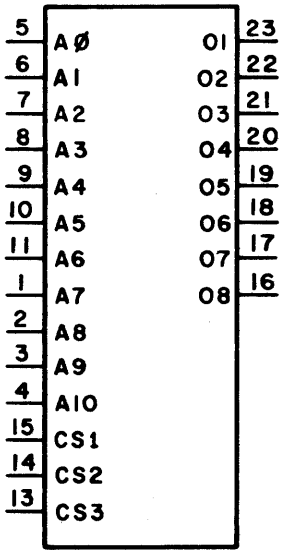


Latched Read



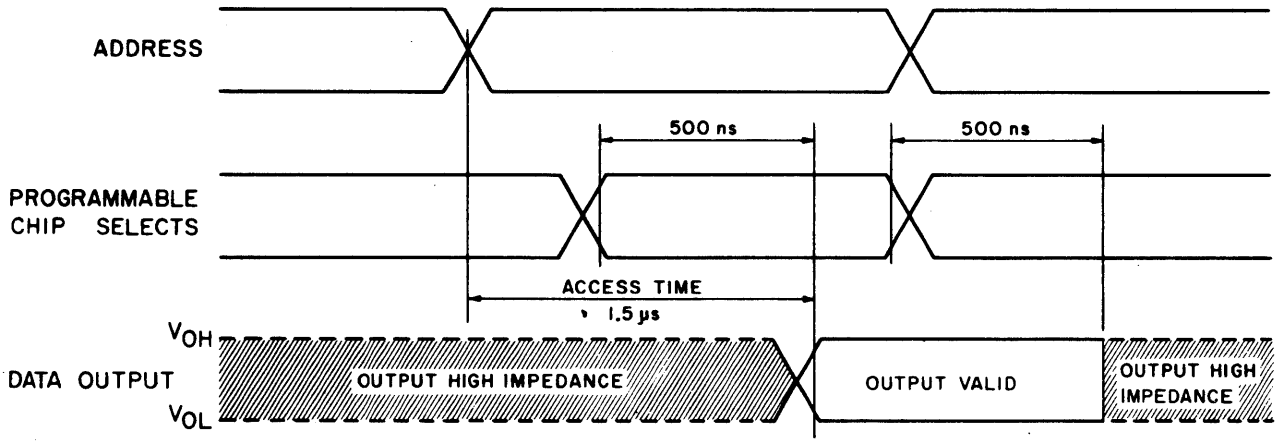
This is a Read-Only Memory that is programmed during manufacture. No part number is given because each program requires a separate part number. Part numbers are given on the schematics. Outputs are 3-state, controlled by three programmable chip-select inputs. Any combination of high- or low-active chip select inputs can be defined, and the desired chip select code is programmed into the chip during manufacture. Maximum access time is 1.5 μs. Only a single power supply voltage (+5V) is required.

Logic Symbol



VCC-24, GND-12

Waveforms
(All times shown are maximum)

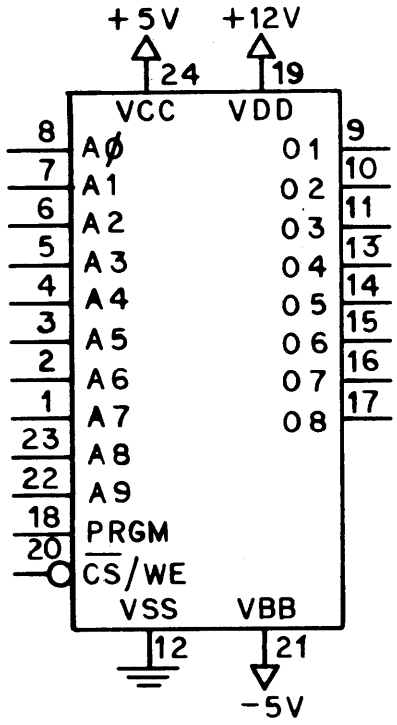


Loading:
Outputs 1.1 Unit Loads

MOS 1024 x 8-Bit Electrically-Alterable ROM | Part No. 42329 | Type 8708

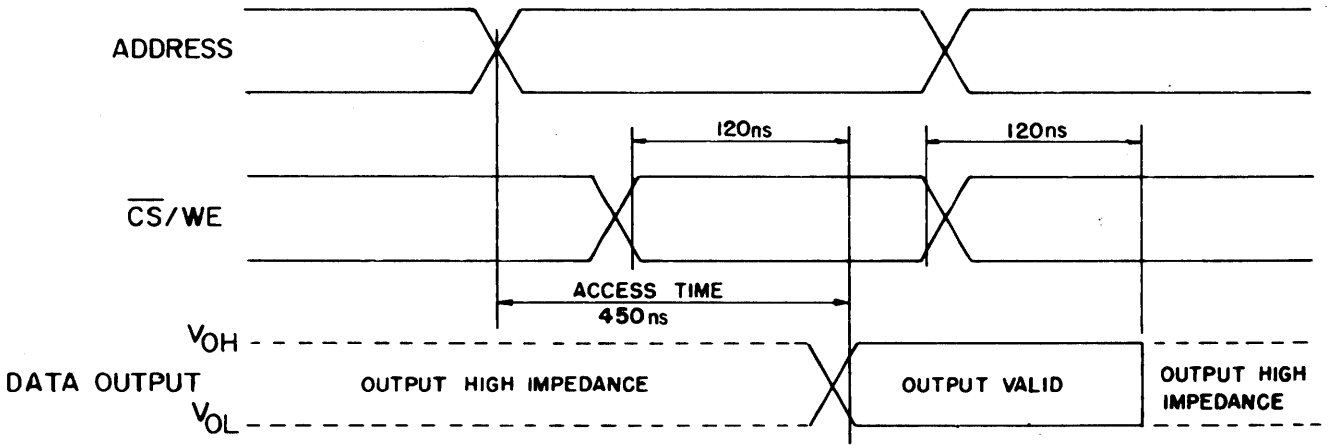
This Read-Only Memory is programmed at the Diablo factory. It has a transparent quartz lid which allows exposure to ultraviolet light to erase the bit pattern. It is electrically compatible with the type 8308 ROM. Access time is 450 ns. Outputs are 3-state, controlled by the Chip Select (CS) input.

Logic Symbol



VBB = +5V
VCC = +5V
VDD = +12V
VSS = GND

Waveforms
(All times shown are maximum)



Loading:

Outputs 1 Unit Load

4.6 ASCII CODE CHART

The ASCII code chart is reproduced in Figure 4-2.

4.7 SCHEMATICS AND LOGIC DRAWINGS

Figure 4-3 explains the meaning of the various notations contained on the logic drawings and schematics. For more information on component locations, connector pin numbers, cables, etc., see Section 3.5.

Table 4-2 lists the schematics and logic drawings provided in the remaining pages of this manual.

Table 4-2. Schematic and Logic Drawing Index

Drawing No.	Description
23924-99	HPRO3 Board (Terminal Processor)
23926-XX	XMEM1 Board
24930-01	MXI Board (Matrix Interface)
24620-XX	PROCESSOR Board (Printer)
24625-XX	CAR SERVO Board
40525-XX	CAR PWR AMP Board
24605-XX	HAMMER DRIVER Board
24935-01	Motherboard
400056-01	Control Panel
400089-01	Interconnection Diagram
400097-01	Power Distribution
400062-XX	Power Supply (115/230 Vac)
400094-01	Keyboard (Cortron)
400285-01	Keyboard (Micro Switch)
24500-XX	Interconnection Diagram, Printer Cables

BITS 7 6 5 4 3 2 1 / ROW / COLUMN					0_0	0_1	1_0	1_1	0_0	0_1	1_0	1_1
					0	1	2	3	4	5	6	7
0	0	0	0	0	NUL	DLE	SP	0	@	P	`	p
0	0	0	1	1	SOH	DC1	!	1	A	Q	a	q
0	0	1	0	2	STX	DC2	"	2	B	R	b	r
0	0	1	1	3	ETX	DC3	#	3	C	S	c	s
0	1	0	0	4	EOT	DC4	$	4	D	T	d	t
0	1	0	1	5	ENQ	NAK	%	5	E	U	e	u
0	1	1	0	6	ACK	SYN	&	6	F	V	f	v
0	1	1	1	7	BEL	ETB	'	7	G	W	g	w
1	0	0	0	8	BS	CAN	(	8	H	X	h	x
1	0	0	1	9	HT	EM	)	9	I	Y	i	y
1	0	1	0	10	LF	SUB	*	:	J	Z	j	z
1	0	1	1	11	VT	ESC	+	;	K	[	k	{
1	1	0	0	12	FF	FS	,	<	L	\	l	|
1	1	0	1	13	CR	GS	-	=	M	]	m	}
1	1	1	0	14	SO	RS	.	>	N	^	n	~
1	1	1	1	15	SI	US	/	?	O	_	o	DEL

All characters in these two columns an SP(Space) are non-printing. Del(Delete) does not print in the remote mode,but prints logical NOT symbol(¬) when entered on keyboard in local mode. (Logical NOT is also printed in place of characters received with parity or framing error.

Figure 4-2. ASCII Code Chart

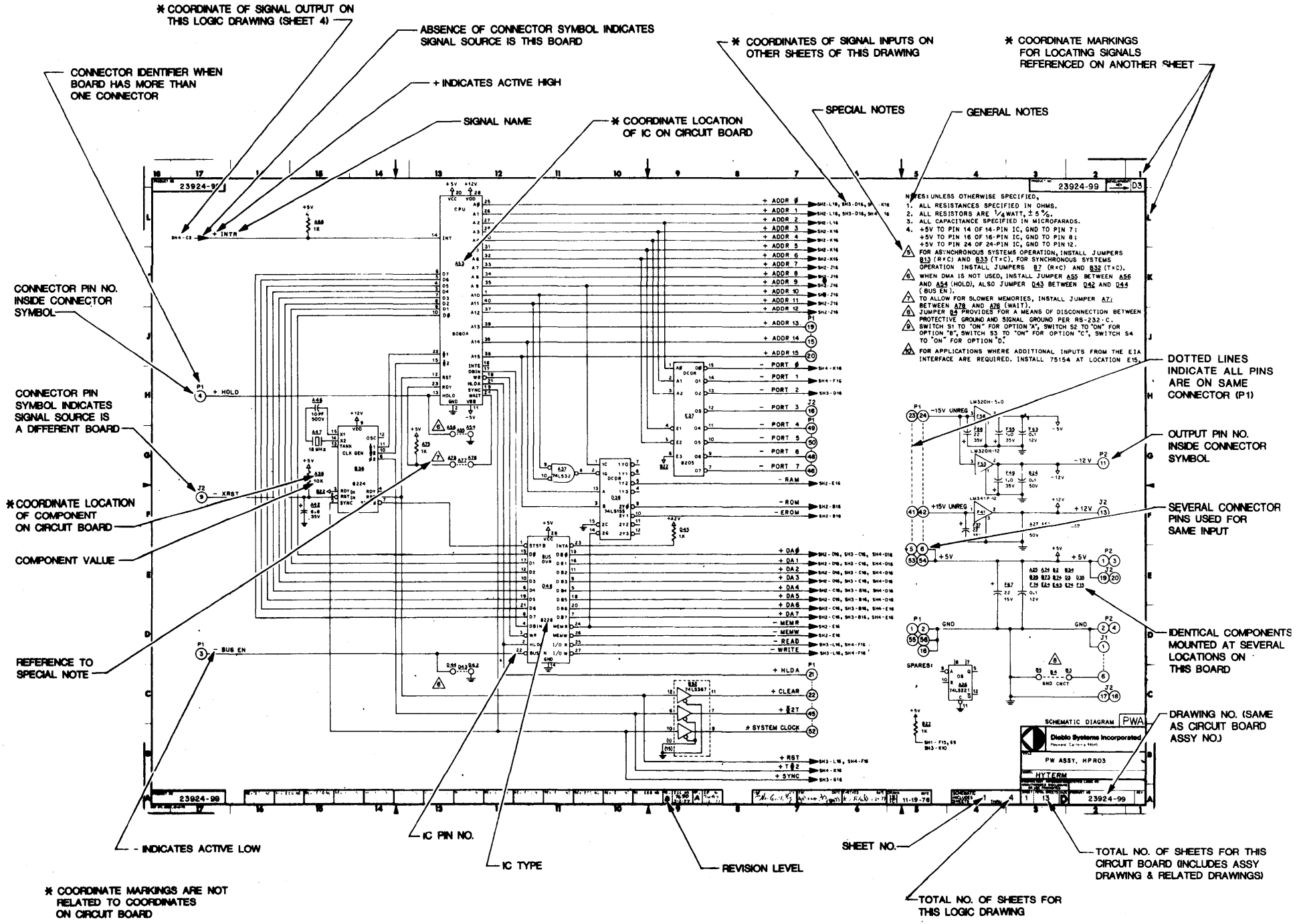


Figure 4-3 Logic Drawing Notation

PRODUCT NO 23924-99 | DEVELOPMENT REV. D3

NOTES: UNLESS OTHERWISE SPECIFIED,
1. ALL RESISTANCES SPECIFIED IN OHMS.
2. ALL RESISTORS ARE 1/4 WATT, ± 5%.
3. ALL CAPACITANCE SPECIFIED IN MICROFARADS.
4. +5V TO PIN 14 OF 14-PIN IC, GND TO PIN 7;
   +5V TO PIN 16 OF 16-PIN IC, GND TO PIN 8;
   +5V TO PIN 24 OF 24-PIN IC, GND TO PIN 12.
5. FOR ASYNCHRONOUS SYSTEMS OPERATION, INSTALL JUMPERS B13 (R×C) AND B33 (T×C). FOR SYNCHRONOUS SYSTEMS OPERATION INSTALL JUMPERS B11 (R×C) AND B32 (T×C).
6. WHEN DMA IS NOT USED, INSTALL JUMPER A55 BETWEEN A56 AND A54 (HOLD), ALSO JUMPER D43 BETWEEN D42 AND D44 (BUS EN).
7. TO ALLOW FOR SLOWER MEMORIES, INSTALL JUMPER A77 BETWEEN A78 AND A76 (WAIT).
8. JUMPER B4 PROVIDES FOR A MEANS OF DISCONNECTION BETWEEN PROTECTIVE GROUND AND SIGNAL GROUND PER RS-232-C.
9. SWITCH S1 TO "ON" FOR OPTION "A", SWITCH S2 TO "ON" FOR OPTION "B", SWITCH S3 TO "ON" FOR OPTION "C", SWITCH S4 TO "ON" FOR OPTION "D."
10. FOR APPLICATIONS WHERE ADDITIONAL INPUTS FROM THE EIA INTERFACE ARE REQUIRED. INSTALL 75154 AT LOCATION E15.

SCHEMATIC DIAGRAM PWA

Diablo Systems Incorporated
Hayward California 94545

TITLE: PW ASSY, HPRO3

MODEL: HYTERM

PROPRIETARY INFORMATION. UNAUTHORIZED DISCLOSURE OR USE PROHIBITED. SYSTEM LOGIC SH.

SHEET 1 | TOTAL SHEETS 13 | SIZE D | PRODUCT NO 23924-99

SCHEMATIC INCLUDES SHEETS 1 THRU 4

DRAWN [N] [C] 11-19-76 | CHECKED | ENG | MFG | QUAL

REV	ECO NO	DATE
E	7816	8/6/77
D	7771	5-25-77
C	7759	4-26-77
B	7690	3-2-77
A	5648	

DCT CTL DOBE 12-10-75

PRODUCT NO 23924-99 DEVELOPMENT REV. D3

SH1-L7 + ADDR Ø
SH1-L7 + ADDR 1
SH1-L7 + ADDR 2
SH1-L7 + ADDR 3
SH1-L7 + ADDR 4
SH1-K7 + ADDR 5
SH1-K7 + ADDR 6
SH1-K7 + ADDR 7
SH1-K7 + ADDR 8
SH1-K7 + ADDR 9
SH1-K7 + ADDR 10
SH1-K7 + ADDR 11
SH1-J7 + ADDR 12

P1 + ADDR Ø (35)
P1 + ADDR 1 (36)
P1 + ADDR 2 (33)
P1 + ADDR 3 (34)
P1 + ADDR 4 (29)
P1 + ADDR 5 (27)
P1 + ADDR 6 (25)
P1 + ADDR 7 (43)
P1 + ADDR 8 (44)
P1 + ADDR 9 (40)
P1 + ADDR 10 (38)
P1 + ADDR 11 (28)
P1 + ADDR 12 (26)

+5V, VCC (18), RAM, A0–A7, OD, CE1, CE2, R/W, GND (16, 8), I/O1–I/O4, 2111A-4

D65 (VCC, GND: 18, 8)
B65 (VCC, GND: 18, 8)
F65 (VCC, GND: 18, 8)
E65 (VCC, GND: 18, 8)

SH1-D7 − MEMR
SH1-D7 − MEMW
SH1-G7 − RAM
SH1-E7 + DAØ
SH1-E7 + DA1
SH1-E7 + DA2
SH1-E7 + DA3
SH1-E7 + DA4
SH1-E7 + DA5
SH1-D7 + DA6
SH1-D7 + DA7
SH1-F7 − ROM
SH1-F7 − EROM

D37 74LSØ4 (5, 6)

E48 ROm, A0–A10, CS1, CS2, CS3, 01–08, 8316

F46 ROM, A0–A10, CS1, CS2, CS3, 01–08, 8316

F32 EROM (VCC +5V: 24; VDD +12V: 19; VSS −5V: 12; VBB: 21; PRGM: 18; CS/WE: 20; A0–A9; 01–08; 2704/2708)

P1 − MEMR (7)
P1 − MEMW (17)
P1 + DAØ (9)
P1 + DA1 (12)
P1 + DA2 (11)
P1 + DA3 (13)
P1 + DA4 (8)
P1 + DA5 (10)
P1 + DA6 (14)
P1 + DA7 (16)

SCHEMATIC DIAGRAM

Diablo Systems Incorporated
Hayward, California 94545

TITLE: PW ASSY, HPR03
MODEL: HYTERM
PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED. SYSTEM LOGIC NO.
SHEET 2 TOTAL SHEETS 13 SIZE D PRODUCT NO. 23924-99

REV	E.C.N.	DATE
E	7816	
D	7771	5-25-77
C	7759	4-26-77
B	7690	3-2-77
A	7648	1-21-77

ENG. John Curtis 1/24/77 — CHECKED Woolley Olson 1-24-77 — DRAWN [illegible] 11-8-76

SCHEMATIC INCLUDES SHEETS 1 THRU 4

PRODUCT NO 23924-99

DCT CTL DOC. 12-10-73

REVISION HISTORY - #23924-XX HPRO3 Board

Rev.	A	ECO#	7648	As released.
	B		7690	Change resistor F24 from 1K to 8.2K; add resistor F25 from -OPTION D to +5V.
	C		7759	Correct error on bill of material (diode A28 omitted); add "on" indication to S1-S4 on sheet 3 of schematic; correct note 5 on sheet 1 of schematic --specified "B7," should be "B11." No changes to board.
	D		7771	Replace 74LS221 at A26 with 74LS123. Change resistor (S32) and capacitor (A29), and remove diode (A28). Provides more stable real-time clock.
	E		7816	Allow use of plastic ICs, no schematic changes.

PRODUCT NO 23924-99 | DEVELOPMENT REV D3

SH1-D7 – WRITE
SH1-D7 – READ
SH1-B7 + RST
P2 (12) + KYSTB
+5V B26 1K
+5V F24 8.2K
+5V E6 1K
(13) – DATA Ø
(16) – DATA 1
(18) – DATA 2
(20) – DATA 3
(19) – DATA 4
(17) – DATA 5
(15) – DATA 6
(14) – DATA 7
SH1-B7 + SYNC
(7) – FKY 1
(8) – FKY 2
(10) – FKY 3
(5) – FKY 4
(6) – FKY 5
F27 S4 – OPTION D, S3 – OPTION C, S2 – OPTION B, S1 – OPTION A, ON
9
SH1-L7 + ADDR Ø
SH1-L7 + ADDR 1
SH1-H7 – PORT 2
SH1-E7 + DAØ
SH1-E7 + DA1
SH1-E7 + DA2
SH1-E7 + DA3
SH1-E7 + DA4
SH1-E7 + DA5
SH1-E7 + DA6
SH1-D7 + DA7

+5V 26 VCC
GND 7
8255 I/O INTFC
PC4 13, RST 35, RD 5, WR 36, PAØ 4, PA1 3, PA2 2, PA3 1, PA4 40, PA5 39, PA6 38, PA7 37, PC2 16, PBØ 18, PB1 19, PB2 20, PB3 21, PB4 22, PB5 23, PB6 24, PB7 25, AØ 9, A1 8, CS 6
PCØ 14, PC1 17, PC3 12, PC5 11, PC6
PC7 10
F6
MODE 1
DØ 34, D1 33, D2 32, D3 31, D4 30, D5 29, D6 28, D7 27

B22 D FF (P, D, CLK, Q, C) D27 74LS74
D37 74LSØ4
A37 74LS32
D37 74LSØ4
A29 47 50V
A32 68K
A28 (JUMPER)
A26 74LS123 (B, A, OS, Q, C)
10 MS
B52 74LS367
F22 8.2K, F23 8.2K, E74 8.2K, D67 8.2K, D71 8.2K, D70 8.2K, D69 8.2K, D68 8.2K
+5V F25 1K

– WRITE P1 (39)
– READ (37)
– RST SH4 - E16
+ KYBD INTR SH4 - C16
+ BUSY P2 (9)
+ RTCLK INTR SH4 - B16
– RD J2 (11)
– WR (4)
–CLR (1)
+ DA Ø (3)
+ DA 1 (2)
+ DA 2 (7)
+ DA 3 (8)
+ DA 4 (6)
+ DA 5 (5)
+ DA 6 (10)
+ DA 7 (12)
– OPTION D SH4 - G16

SCHEMATIC DIAGRAM

Diablo Systems Incorporated
Hayward California 94545

TITLE PW ASSY, HPRO3
MODEL HYTERM

PRODUCT NO	REV ECO NO	REV ECO NO	REV ECO NO	REV ECO NO	REV ECO NO	REV ECO NO	REV ECO NO	REV ECO NO	REV ECO NO	REV ECO NO	REV ECO NO	REV ECO NO
23924-99									E 7916	D 7771 5-25-77	C 7759 4-26-77	B 7690 3-2-77

DRAWN	DATE	CHECKED	DATE	ENG	DATE	MFG	DATE
IN/CI	12-10-76	R.W.Fjell	1-24-77				

SCHEMATIC INCLUDES SHEETS 1 THRU 4 | SHEET 3 | TOTAL SHEETS 13 | SIZE D | PRODUCT NO 23924-99

DEV CTL DOC E 12-10-75

SH1 - L7 +ADDR 1
P1 (51) -XIO
SH1 - H7 -PORT Ø
SH1 - L7 +ADDRØ
SH1 - B7 +T02

J1 (7) -DATA RECEIVED
(8) +DATA SET READY
(9) +CLEAR TO SEND
(10) +CARRIER DETECT

VCC1 RI VCC2 RCVR A16 75154 GND

(11) +OPTION 2
(12) +OPTION 3

VCC1 RI VCC2 RCVR E15 75154 GND

SH3 - C3 -OPTION D

8255: RST, CS, RD, WR, PA7-PAØ, PCØ-PC7, MODEØ, I/O INTFC, VCC, GND

SH1 - B7 +RST
SH1 - H7 -PORT 1
SH1 - D7 -READ
SH1 - D7 -WRITE

SH3 - L3 -RST

SH1 - E7 +DAØ
SH1 - E7 +DA1
SH1 - E7 +DA2
SH1 - E7 +DA3
SH1 - E7 +DA4
SH1 - E7 +DA5
SH1 - D7 +DA6
SH1 - D7 +DA7

SH3 - X3 +KYBD INTR

SH3 - G3 +RTCLK INTR

P1 (47) -XINTR

E5: 74LS161 LOAD/CLK/ENP/ENT/CNTR, B22, D26, D37 74LSØ4, A37 74LS32, B24 D-FF CLK D27 74LS74, B30 B32 B29 B31 B33 B14 B13 B12 B10 B11

D5 USART: CS, C/D, CLK, RxD, DSR, CTS, DTR, TxE, SYNDET, RTS, TxD, RxC, DØ-D7, RD, WR, RST, RxRDY, TxRDY; +5V

8251

B20 1K

B16 75150P, B21 75150P: +12V / -12V

J2 (15) +ADDR 1
(14) +ADDRØ

J1 (2) +OPTION 1
(3) +DATA TERMINAL READY
(4) +REQUEST TO SEND
(5) -XMIT DATA

B27 74LS54, D64 1K

+INTR → SH1-L7

SCHEMATIC DIAGRAM

Diablo Systems Incorporated
Hayward California 94545

TITLE PW ASSY, HPR03
MODEL HYTERM
PROPRIETARY INFORMATION: UNAUTHORIZED DISCLOSURE OR USE PROHIBITED. SYSTEM LOGIC NO.
SHEET 4 TOTAL SHEETS 13 SIZE D PRODUCT NO 23924-99

SCHEMATIC INCLUDES SHEETS 1 THRU 4

REV	ECO NO	DATE
E	7816	
D	7721	5-25-77
C	7759	4-26-77
B	7690	3-2-77
A	7649	2-17-77

DRAWN (GORDIG) 11-18-76 | CHECKED R.W.F. 1-24-77 | ENG F.W.G. 1/24/77 | PROJ R.W.F. 1-24-77

PRODUCT NO 23924-99 DEV CTL DOSE 12-10-73

NOTES: UNLESS OTHERWISE SPECIFIED,
1. ALL RESISTANCES SPECIFIED IN OHMS.
2. ALL RESISTORS ARE 1/4 WATT, ± 5 %.
3. ALL CAPACITANCE SPECIFIED IN MICROFARADS.
4. + 5V TO PIN 14 OF 14-PIN IC, GND TO PIN 7;
   + 5V TO PIN 16 OF 16-PIN IC, GND TO PIN 8;
   + 5V TO PIN 24 OF 24-PIN IC, GND TO PIN 12.

ADDRESS BUFFER — E40 8212 I/O PORT

+ ADDRØ (35)
+ ADDR1 (36)
+ ADDR2 (33)
+ ADDR3 (34)
+ ADDR4 (29)
+ ADDR5 (27)
+ ADDR6 (25)
+ ADDR7 (43)

DI1 DI2 DI3 DI4 DI5 DI6 DI7 DI8 DS1 DS2 MD STB
DO1 DO2 DO3 DO4 DO5 DO6 DO7 DO8 INT
F24 C

RAM — 2111A-4 — VCC, A0–A7, I/O1–I/O4, OD, CE1, CE2, R/W, GND

D4 D10 D16
D40 D46 D52

+ A12 SH3-C17
+ A11 SH3-C17
+ A10 SH3-C17
+ A9 SH3-C17
+ A8 SH3-C17
+ A7 SH2-J16, SH3-D17
+ A6 SH2-K16, SH3-D17
+ A5 SH2-K16, SH3-D17
+ A4 SH2-K16, SH3-D17
+ A3 SH2-K16, SH3-D17
+ A2 SH2-K16, SH3-D17
+ A1 SH2-K16, SH3-D17
+ AØ SH2-K16, SH3-E17

+ DAØ SH2-H16
+ DA1 SH2-G16
+ DA2 SH2-F16
+ DA3 SH2-F16
+ DA4 SH2-F16
+ DA5 SH2-F16
+ DA6 SH2-F16
+ DA7 SH2-F16

RAM DECODER — E34 74LS32 — E22 8205 DCDR

+ ADDR8 (44)
+ ADDR9 (40)

EROM DECODER — E28 8205 DCDR

+ ADDRIØ (38)
+ ADDR11 (28)
+ ADDR12 (26)

+ ADDR14 (15)
+ ADDR15 (20)
− MEMR (7)
− MEMW (17)

− RAM5 SH2-D16
− RAM6 SH2-D16
− RAM7 SH2-C16

− S1K SH3-C17
− S2K SH3-C17
− S3K SH3-B17
− S4K SH3-H17
− S5K SH3-H17
− S6K SH3-H17
− S7K SH3-H17
− S8K SH3-H17
− ENRO SH3-H17

− MEMR SH2-C16
− MEMW SH2-C16

(5,6,53,54) +5V — F30 22 15V — F75 0.1 12V
A13 A31 A49 A67 B5 B17 B29 B41 B53 B65 E6 E15 E23 E29 E39 E49

(1,2,55,56) LM32ØT-5.0 — −15V UNREG — F64 — E64 22 35V — B69 1.0 35V — 0.1 12V — −5V
A9 A26 A44 A62

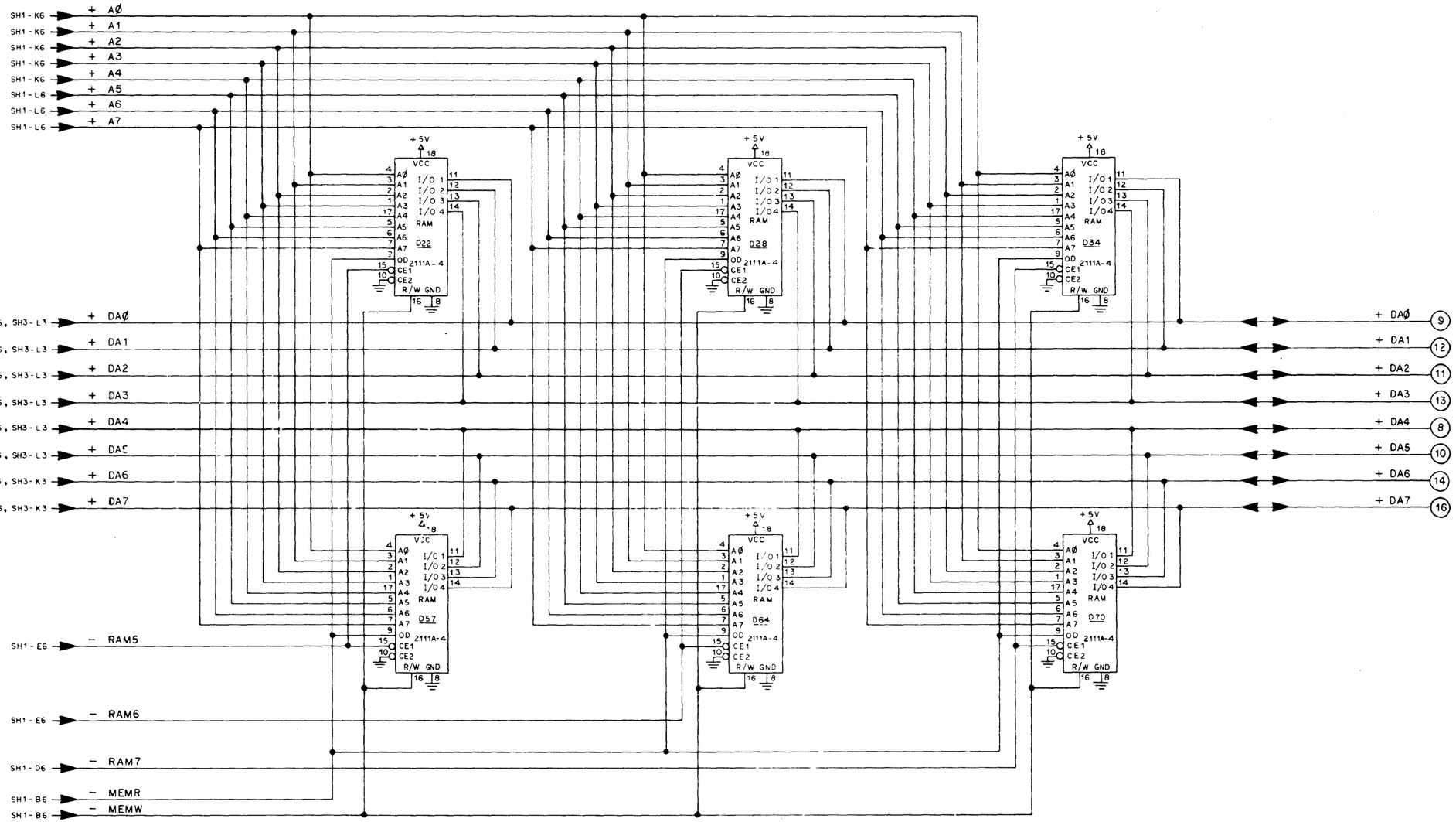
(23,24) LM34ØT-12 +12V — +15V UNREG — F51 — F49 22 35V — 0.1 50V
B12 B21 B30 B39 B48 B57 B66 B75

+5V — F24 1K — SH1-C14, H16

SCHEMATIC DIAGRAM
Diablo Systems Incorporated
PW ASSY, XMEM1
PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE IS PROHIBITED
SYSTEM LOGIC NO
SHEET 1 TOTAL SHEETS 8 SIZE D
PRODUCT NO 23926-XX
9-17-76

REVISION HISTORY -#23926-XX XMEM1 Board

Rev. A	ECO#	7646	As released.
B		7852	Add dash numbers for 1641, 1660. No schematic changes.
C		7933	PWA MEM1 bill of materials and ROM changes.
D		7953	PWA MEM1 establish -98, -99. Change bill of material to include -98 - authorize 04 etch for custom ROM.
E		A4092	Authorized Purchasing to buy other than plastic packaged IC's if there was a shortage.



SCHEMATIC DIAGRAM

Diablo Systems Incorporated
Hayward, California 94545

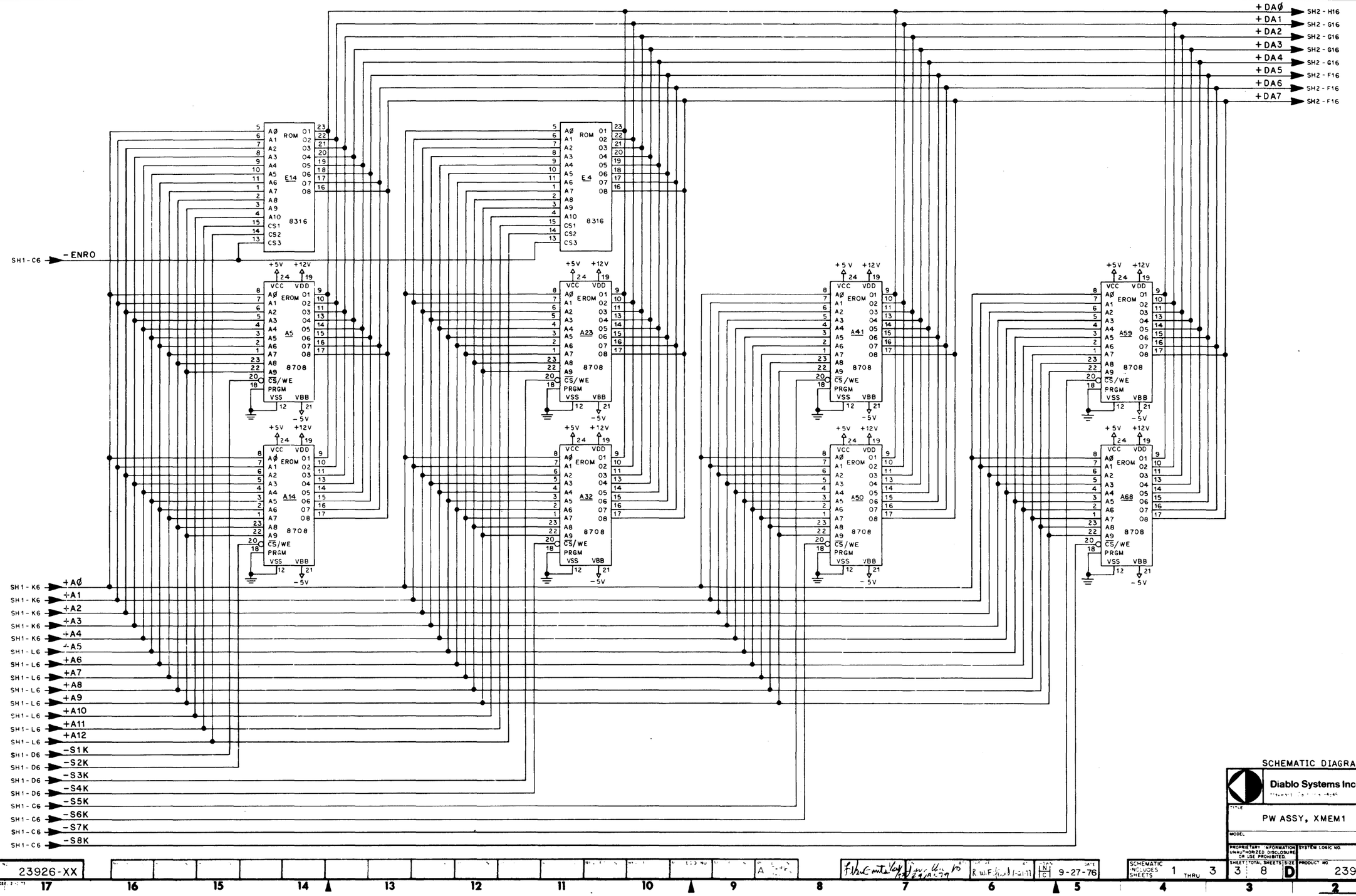
TITLE: PW ASSY, XMEM1

MODEL:

PROPRIETARY INFORMATION SYSTEM LOGIC NO.
UNAUTHORIZED DISCLOSURE OR USE PROHIBITED.

PRODUCT NO.	SCHEMATIC INCLUDES SHEETS	SHEET	TOTAL SHEETS	SIZE	PRODUCT NO.
23926-XX	1 THRU 3	2	8	D	23926-XX

REV. ECO NO.	DATE	ENG	DATE	CHECKED	DATE	DRAWN	DATE
A 7646	12-29-77					IH IC	9-23-76



SCHEMATIC DIAGRAM

Diablo Systems Incorporated

TITLE: PW ASSY, XMEM1

MODEL:

PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED.

SYSTEM LOGIC NO.

SHEET 3 TOTAL SHEETS 8 SIZE D PRODUCT NO 23926-XX

SCHEMATIC INCLUDES SHEETS 1 THRU 3

DRAWN N/C DATE 9-27-76

± DIR 42
+ CAR LIN MODE 38
+ CAR. POS A 15
+ CAR POS B 16
+ CLOCK A 19
+ CAR EVEN 14
−PORT 6 52
−WRITE 51
−SELECT PRINTER 26
+ DA Ø 9
+ DA 1 13
+ DA 2 20
+ DA 3 24
+ DA 4 8
+ DA 5 11
+ DA 6 21
+ DA 7 25
−DATA ACK 50
− PORT 5 53
−READ 47
SPARE 55
−INHIBIT (RIBBON JAM) 56
−ESC RESET (CHECK) 40
− BUSY RESET 39
− BELL (TIME OUT) 36
− COVER OPEN 28
− PAPER OUT 22
+ SYSTEM CLOCK 54
+ POWER ON 17
+5V 5,6
GND 1-4

C73 C37 C61 C13 C25 C39 1K +5V

TRACK CROSSING DETECTION LOGIC

23 + CAR REV
44 + CAR FWD
49 + CAR POS INT 1

BIDIRECTIONAL DATA BUS

STROBE FF C49 D68

READY FF

D54 OUTPUT

STATUS OUT PR/B

D36 INPUT

COMMAND PR/B INPUT

DATA PR/B INPUT

E51 1K E50 1K E65 1K E63 1K E66 .1 50V E61 .1 50V E68 1K C17 470pF E5 6.8 35V TA .1 50V

* C4, C38, C64, D3, D37, D73

43 − DOUBLE LINE FEED
45 + AUTO LINE FEED
18 + TEST
10 − SET TOF ZERO
12 − LINE FEED
48 + RESTORE (INT Ø)
37 + DATA STROBE
7 + READY
35 + D1
34 + D2
33 + D3
32 + D4
31 + D5
30 + D6
29 + D7
27 + D8
46 + POWER ON
41 − POWER ON

MATRIX INTERFACE

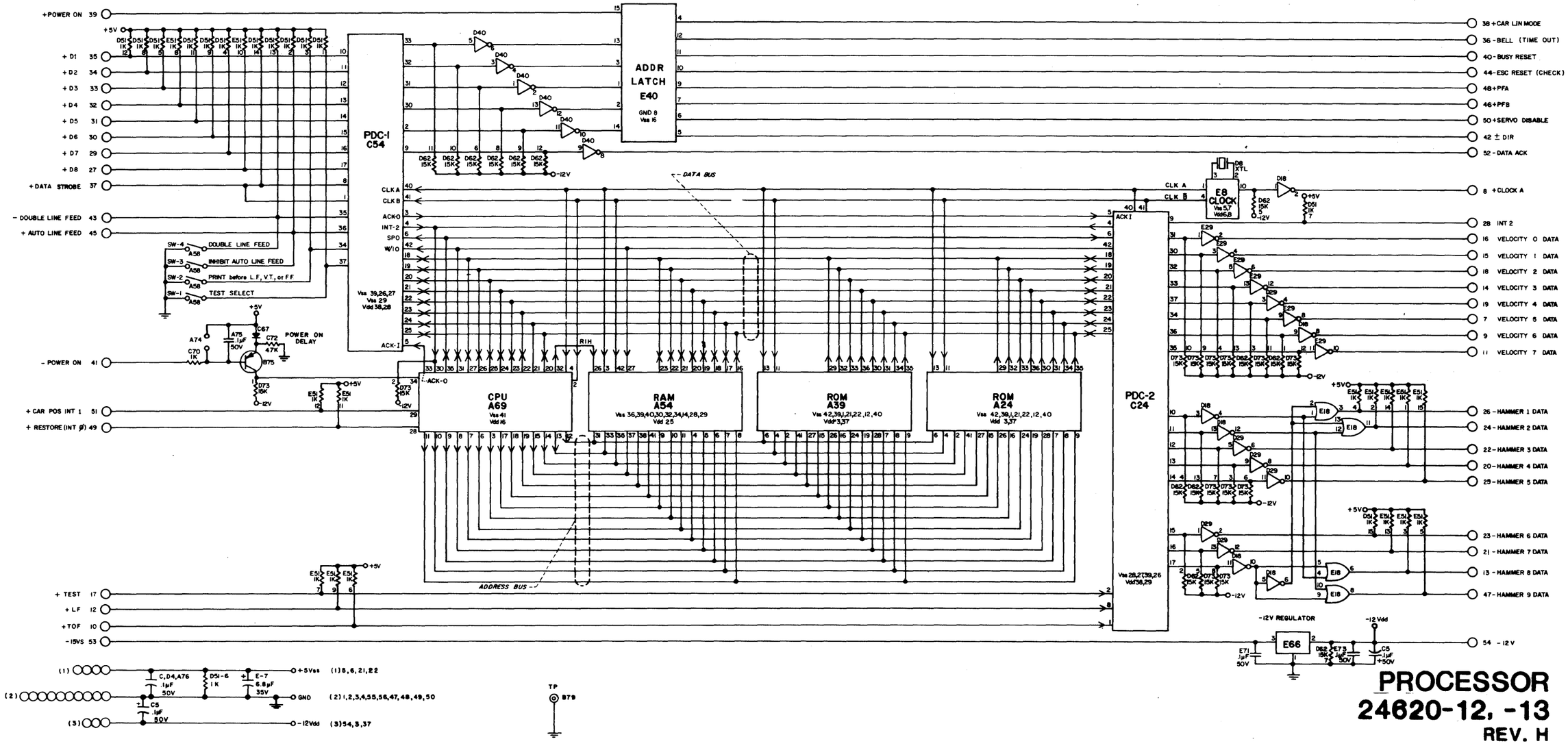
24930-01

REV. A

083-020

REVISION HISTORY - #24930-01 MATRIX INTERFACE

REV. A ECO# A1902 As released.

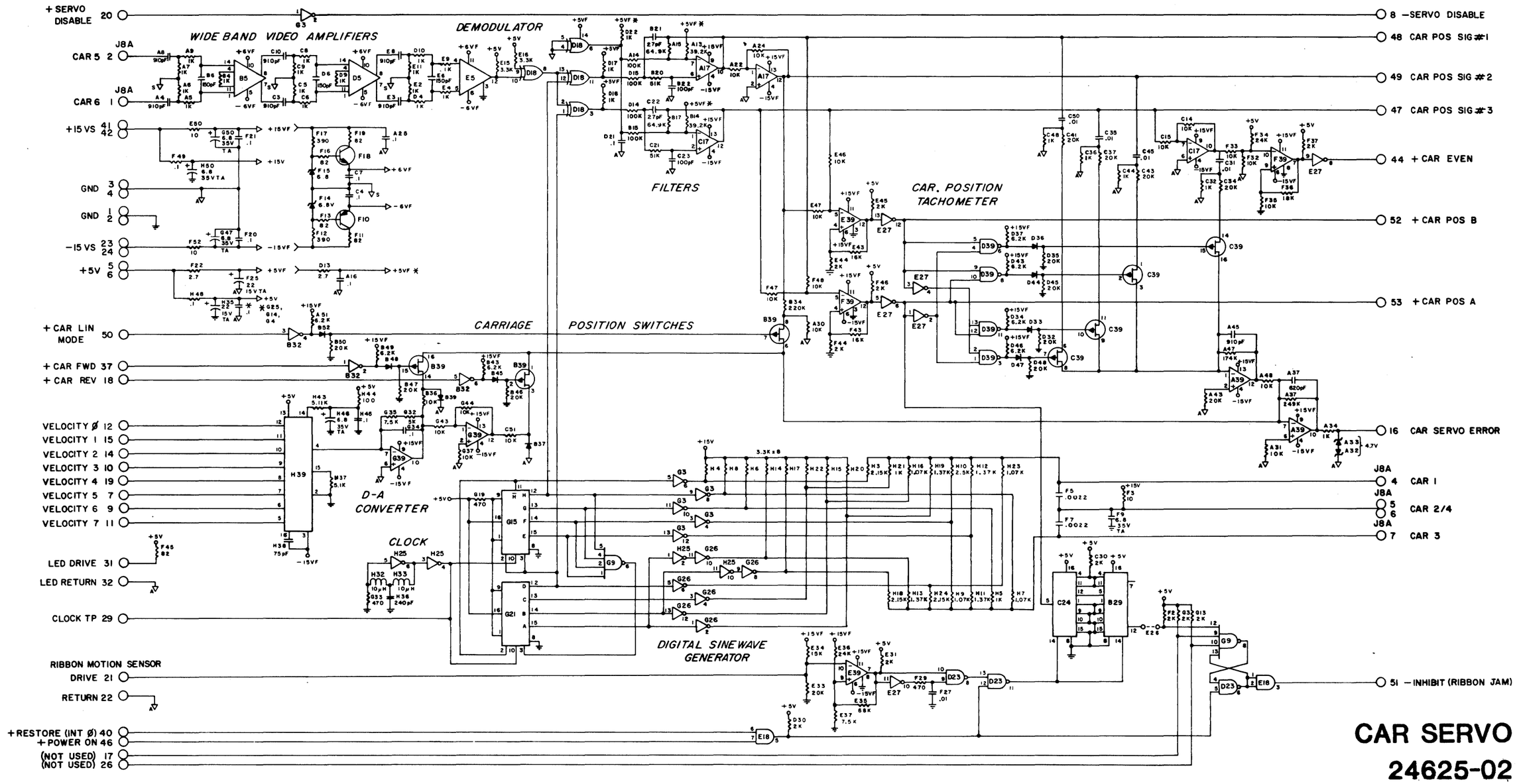


PROCESSOR
24620-12, -13
REV. H

083 - 021

REVISION HISTORY -# 24620-12, -13 PROCESSOR Board

REV.	ECO#	ETCH	CONFIGURATION
A	A1429	01	Standard -01 configuration bill of material, assembly, and schematic as released.
B	A1464	01	Documentation change only.
C	A1539	01	Eliminate PROM PCB, add ROM's to this assembly (A24=13206-01/A39=13206-12)
D	A1828	01	Add ROM descriptions (13206-01 = A52G0PA 13206-12 = A52G1PB)
E	A1902	01	Change drawing to -XX, add -11 (systems) configuration.
F	A3106	01	Documentation change only
G	A3127	02	Add -02, -05, and -12 configurations. Allow use of -02 etch. Remove switch A74 and ground terminal B70. Add -12V (Vss) to ROM pins 12 and 40. Add connector J17 in upper left hand corner for additional ROM PCB interconnect. Include ROMs with bi-directional printing program.
H	A3610	02	Add -13 configuration. Allow program change to accept multiple font option.



CAR SERVO
24625-02
REV. D

083-022

REVISION HISTORY -# 24625-02 CARRIAGE SERVO Board

REV.	ECO#	ETCH	CONFIGURATION
A	A1738	03	Release -02 configuration, and allow use of -03 etch. Include Ribbon Motion Sensor circuits.
B	A1871	03	Add low offset Op-Amp (selected 747C) at A39 to reduce speed variation in reverse carriage motion.
C	A1870	03	Change transistor F10 from type 2N5322L to type 2N5322.
D	A1891	03	Documentation changes only.

CARRIAGE POWER AMPLIFIER

DRIVE REV

PULSE REV

PULSE FWD

DRIVE FWD

POWER MONITOR CKT

PAPER FEED DRIVE A

PAPER FEED DISABLE

PAPER FEED DRIVE B

CAR SERVO ERROR (20)

-SERVO DISABLE (8)

CAR. DISABLE SWITCH

CARRIAGE DRIVE MOTOR

+PW SERVO ENABLE (18)

+POWER ON (16)

PAPER FEED #1

DRIVER RETURN

PAPER FEED #2

+PF A (44)

+PF B (10)

-15VD (21)(23)(29)

+15VD (37)(39)(46)

+5V (5)(6)

ANALOG GND (1)(4)

+15VS (35)(38)

-15VS (19)(22)

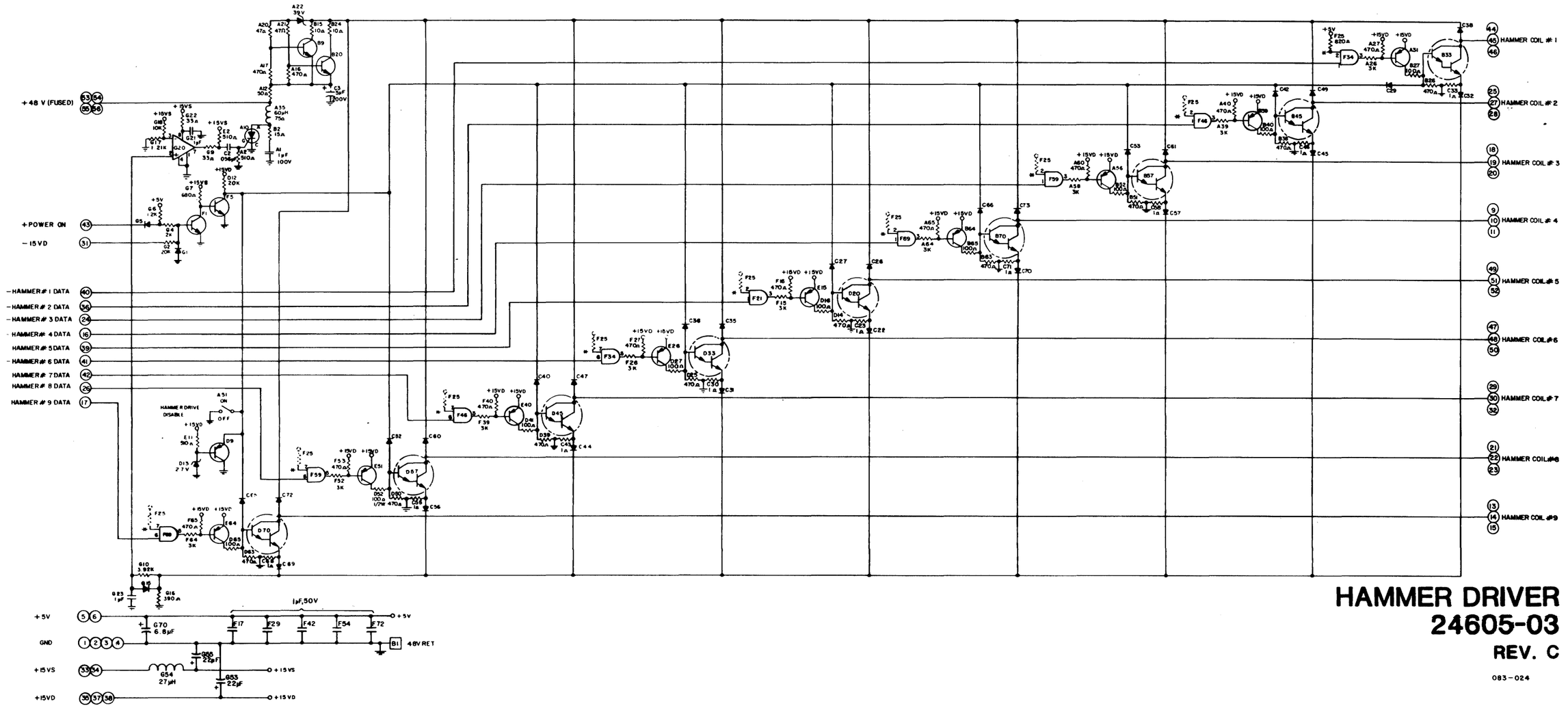
CAR PWR AMP 40525-07

REV. A

083,-023

REVISION HISTORY -#40525-07 CARRIAGE POWER AMPLIFIER Board

REV.	ECO#	ETCH	CONFIGURATION
N	A1260	05	As released for use in the Series 2300 Matrix Printer.
P	A1260A	05	Documentation error
Q	A1565	05	Documentation error.
A	A3128	06	-05 to -06 configuration. Allow use of -07 etch. PCB relayout only. Change component locator codes as follows: C57 to A44 C54 to B46 C55 to B47 C56 to B44 C54 to A45 D56 to A47
A	A3278	07	-05 to -07 configuration, -06 to -08 configuration. Reduce sensitivity to power supply variations. Remove D74. Replace D73 with a jumper. Change zener diodes A7 and B7 to 11 volt devices. Change resistor values: D75 to 5.1K and B33 to 30K.

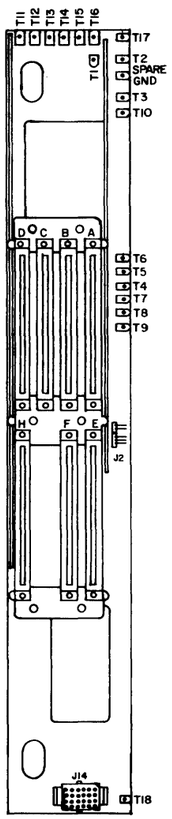


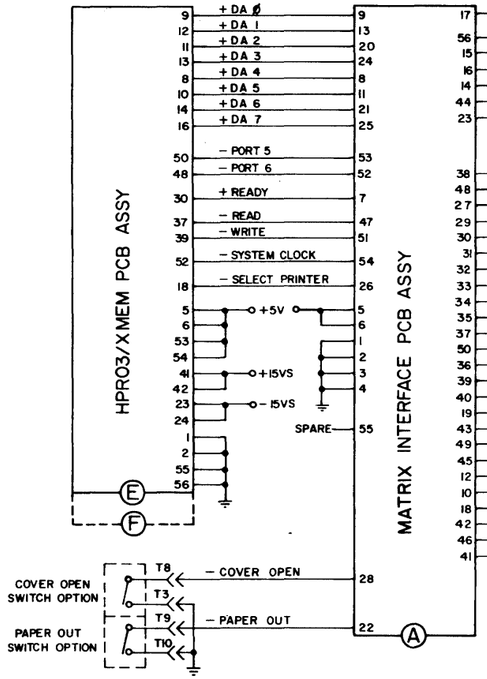
HAMMER DRIVER
24605-03
REV. C

083-024

REVISION HISTORY -# 24605-03 HAMMER DRIVER Board

REV.	ECO#	ETCH	CONFIGURATION
A	A1426	02	-02 configuration bill of material. Assembly, and schematic as released.
B	A1532	02	Documentation change only.
C	A1575	02	Parts standardization. Change transistor types: TIP32 to TIP32A, 2N3644 to PN3644.
D	A1817	02	Change types but not values of capacitors for automatic insertion.
A	A1896	04	-02 to -03 configuration. Allow use of -04 etch. New layout only, no circuit changes.
B	A1975	04	Document change only.
C	A3539	04	Hardware change only. See Parts Catalog.





MOTHER BOARD
24935-01
REV. B

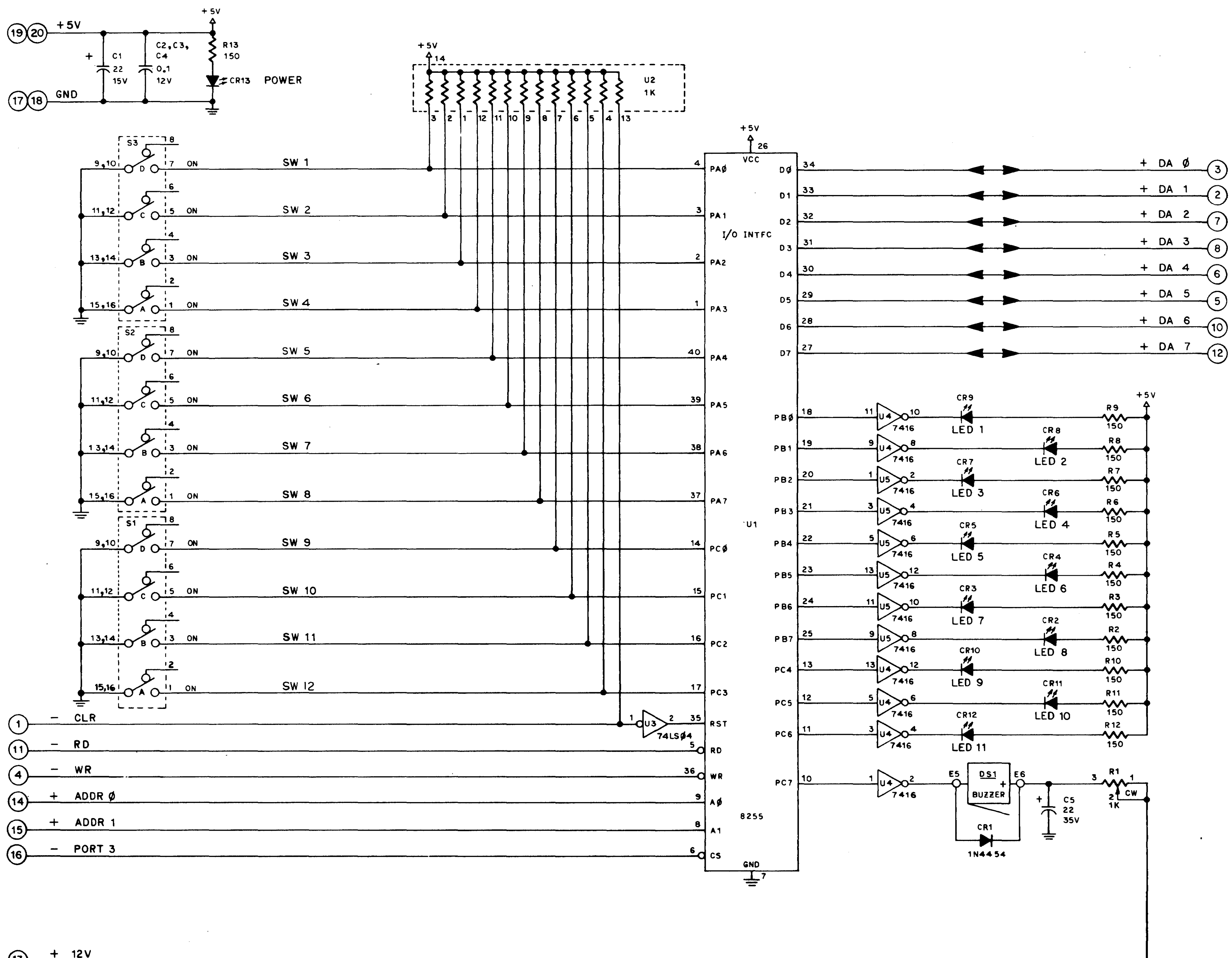
083-025

REVISION HISTORY -#24935-01 MOTHER BOARD

REV.	A	ECO#	A1902	As released
	B		A3535	Change Key Position from 20-22 to 4-6. Remove 90° form from 10 terminals.

400056-01

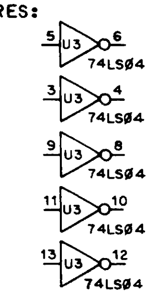
400056-01 DEVELOPMENT REV D2



NOTES: UNLESS OTHERWISE SPECIFIED,

1. ALL RESISTANCES SPECIFIED IN OHMS.
2. ALL RESISTORS ARE 1/4 WATT, ± 5 %.
3. ALL CAPACITANCE SPECIFIED IN MICROFARADS.
4. +5V TO PIN 14 OF 14-PIN IC, GND TO PIN 7; +5V TO PIN 16 OF 16-PIN IC, GND TO PIN 8.
5. ALL LIGHT EMITTING DIODES ARE MV5753 OR EQUIVALENT, EXCEPT CR13 WHICH IS A 5082-4955 OR EQUIVALENT.
6. REFERENCE SCHEMATIC PACKAGE FOR SPECIFIC ASSIGNMENTS OF LEDS AND SWITCHES.

SPARES:



SCHEMATIC DIAGRAM PE

Diablo Systems Incorporated
Hayward, California 94545

TITLE: CONTROL PANEL ASSY,

MODEL: Hy TERM

PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED

SHEET	TOTAL SHEETS	SIZE	PRODUCT NO.
1	7	D	400056-01

SCHEMATIC INCLUDES SHEETS 1 THRU 1

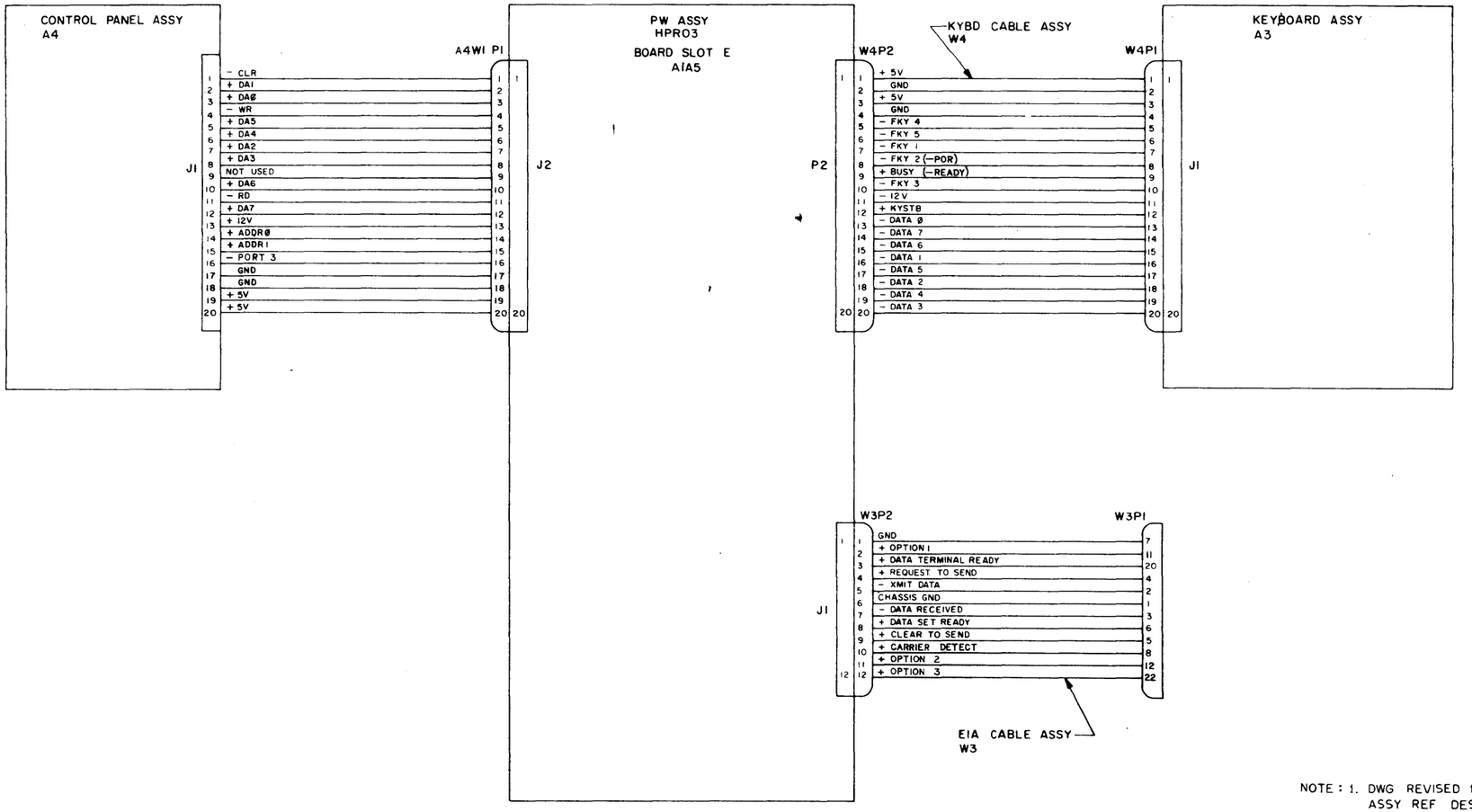
DRAWN 3-1-77

REV	ECO NO
B1	7894 10-12-77
B	7838 7-19-77
A	7788 6/3/77

400056-01

PRODUCT NO. 400089-01

DEVELOPMENT REV. D2



NOTE : 1. DWG REVISED 11-77 SHOWING CORRECTED ASSY REF DESIGNATORS. ECO PENDING.

REV	ECO NO
A	7901 10-11-77

MFG [signature] DATE 9/26/77

CHK [signature] DATE 10/25/77

CHECKED R.W.Fould DATE 4/27/77

DRAWN R.L. DATE 15 JUNE 77

SCHEMATIC INCLUDES SHEETS THRU

Diablo Systems Incorporated
Hayward, California 94545

TITLE: INTERCONNECTION DIAGRAM
SIGNAL CABLES

MODEL: 1660/1641 HYTERM

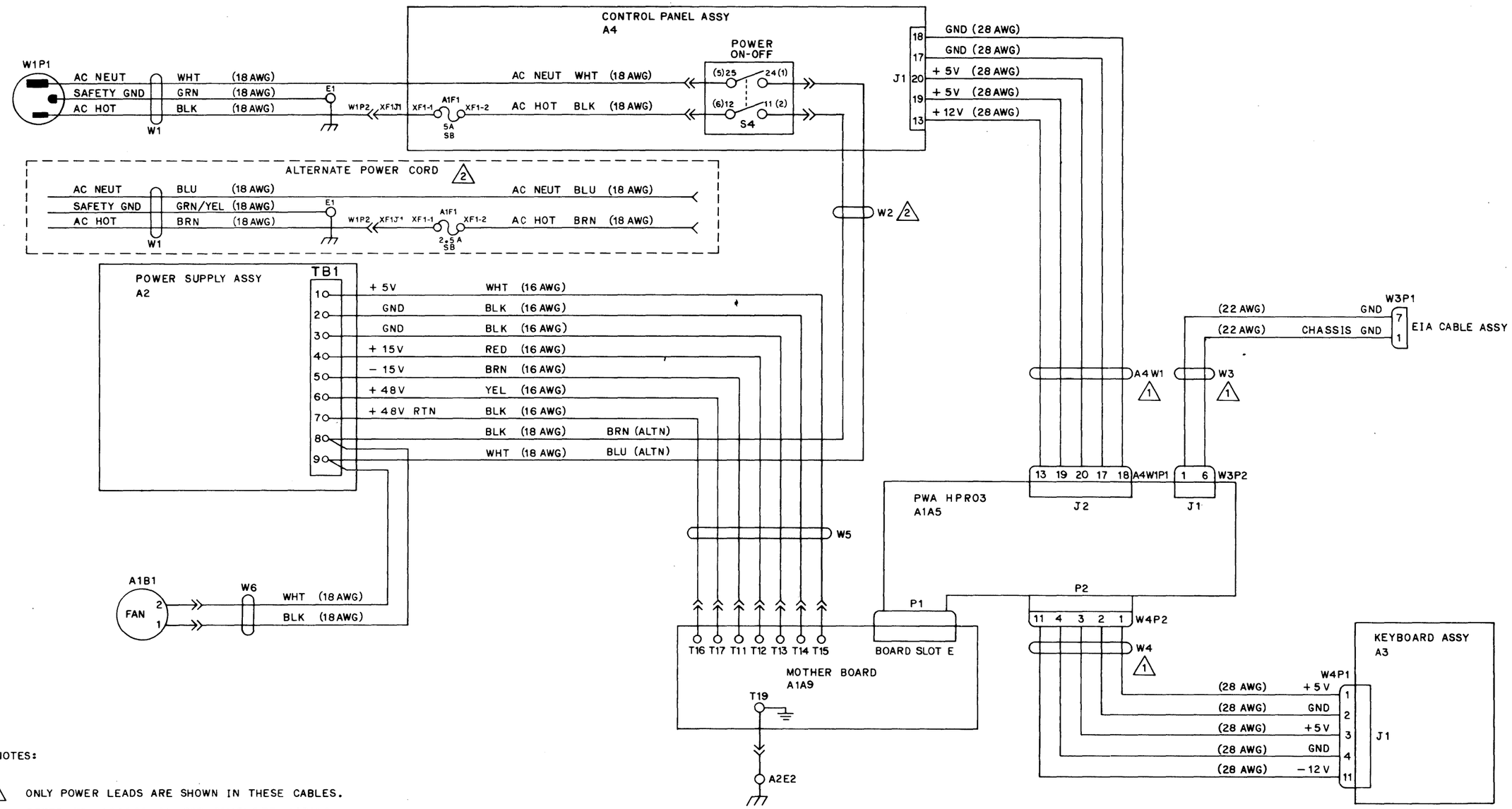
PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED.

SYSTEM LOGIC NO.

SHEET 1 TOTAL SHEETS 1 SIZE D

PRODUCT NO. 400089-01

REV RV



NOTES:

1. ONLY POWER LEADS ARE SHOWN IN THESE CABLES. REFER TO 400089-01 FOR COMPLETE WIRING.

2. ALTERNATE CABLE ASSY ARE USED FOR GREATER THAN 115VAC OPERATION.

SCHEMATIC DIAGRAM

RS

DRAWN N C	DATE 7-11-77	Diablo Systems Incorporated, Hayward, California 94545
CHECKED R.W.Fifield	DATE 7-15-77	
ENGR	DATE 7/26/77	
MFG	DATE 9/26/77	
FIRST USED (NEXT ASSY) 400073-01		SCHEMATIC: 1660 HY TERM POWER DISTRIBUTION
SHEET 1	TOT SHT 1	SIZE D — DWG NO 400097-01

REV A — E C O NO 7901 10-11-77

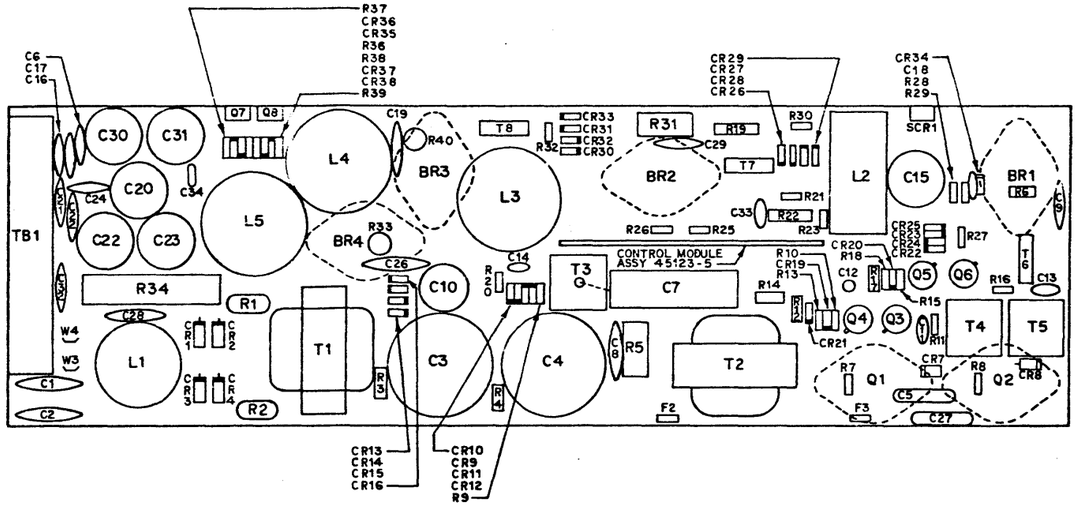
CONTROL BOARD

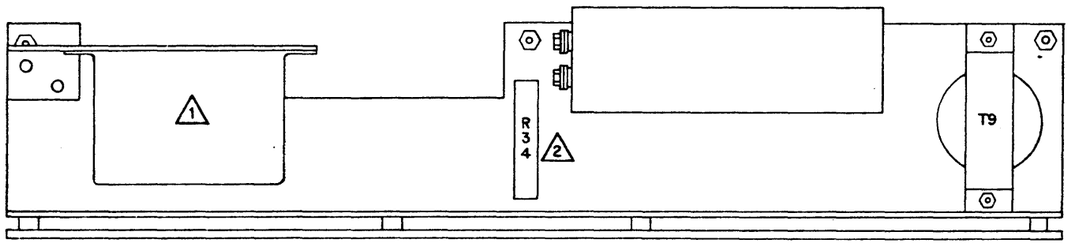
TB1
AC 8 W4
ACC 9 W3
L1 45210
C2 .01 1.4KV
C1 .01 1.4KV
CR1 CR2 CR3 CR4 IN4724 (4)
R1 THERMISTOR 2.5 SG-3
F2 3A
R3, 75K, ½W
C3 400MF 200V
F3 3A
C4 400MF 200V
R2 THERMISTOR 2.5 SG-3
R4, 75K, ½W
T1 45172 115V 230V 115V
CR7 RG1J CR5 1540B Q1
CR8 RG1J CR6 1540B Q2
C5 .005MF
R7 47
R8 47
T4 45270
T5 45270
C7 1MF 400V
T9-1
C27 .005MF
T3
R9 68
T9-2
.0015MF 3KV
C8
25Ω 5W
R5
T6 45325
T2 45246
CR22 CR24 CR23 CR25 IN4148 (4)
R27 130
C9 .01MF 1.4KV
R6 4.7 ½W
BR1 RT12X
L2 45337
W1 W2
TB1 1 +15V-6A
2 RETURN
EXTERNAL STRAP
C15 2K MF 16V
C30 2KMF 16V
C31 2KMF 16V
CR34 5.1V IN5232B
R29 10Ω
R28 51
C18 .01MF 16V
SCR1 IR122F
C16 .1MF 25V
C17 .1MF 100V
C6 .1MF 100V
C34 .1 MF 100 V
CR13 CR14 CR15 CR16 IN4002 (4)
C10 470MF 35V
R11 2.2K
C11 500PF 500V
R14 1.5K ½W
500PF 500V
C13
R16 2.2K
CR20
IN4148
R10 100
Q3 2N3725
CR19 IN4148
Q4 2N3725
R13 100
R12 150 ½W
CR21 IN5231B
R15 100
C12 33MF 10V TANT
Q5 2N3725
Q6 2N3725
R18 100
R19 150 ½W
C14 910 PF
R20 1K
R19 1K
CURRENT LIMIT ADJUST
CW
T7 45325
T2
CR26 CR28 CR27 CR29 IN4148 (4)
R30 100
R31 27Ω 2W
C29 .01MF 1.4K
BR2 RT12X
L3 22007
C20 1KMF 35V
R36 10
CR35 CR36 IN5237B
R37 47
Q7 TIP31A
C21 .1 MF 25V
4 +15V-2A
3 RETURN
(20GA EXT. JUMPER TO TB1-7)
C25 .1MF 25V
CR30 CR32 CR31 CR33 IN4148 (4)
R32 100
C22 1KMF 50V
T8 45325
T2
R40 27Ω 2W
C19 .01MF 1.4K
BR3 RT12X
L4 22007
C23 1K MF 35V
R38 10
CR37 CR38 IN5237B
R39 47
Q8 TIP31A
C24 .1MF 100V
5 -15V-2A
P2-1 P2-8 P2-2
P1-5 UVS C_A COM C_B +24V P1-6
P2-3 PWR. FAIL CURRENT LIMIT BIAS P1-7
P1-4 REMOTE ON/OFF CURRENT LIMIT P1-2
P2-7 OVP P1-1
P2-6 +SENSE DRIVER C.S. P1-3
OSC P2-5
RT P2-7
P2-4 -SENSE
CONTROL MODULE ASSY 45123-5
C33 (NOT USED)
R21 RN55C 1.30K ± 1% ⅛ W
VOLTAGE ADJUST R22 500
R23 RN55C 1.10K ± 1% ⅛ W
R25 2.7K
R26 390
45318
T9 45256
R33 220 2W
BR4 RT12X
C26 .005MF 3KV
L5 45327
C27 6300MF 75V
T9-4
R34 500 10W
C32 .1UF 100V
C28 .1MF 100V
6 +48V - 2.1A
7 RETURN
(20GA EXT JUMPER TO TB1-3)

T8	
SCR-1	
R40	R24,35
Q8	
L5	
F3	
CR39	CR5&7,8
C34	
HG4	
LAST DES. USED	DES. NOT USED

2. ALL RESISTORS ARE ¼W 5%
⚠ COMPONENTS NOT USED ON ASSY 45323-2
NOTES: UNLESS OTHERWISE SPECIFIED:

L & N RESEARCH
Diablo Systems Incorporated
POWER SUPPLY 3 + 4 OUTPUT
115/230 VAC
SHEET 3 OF 4
PROPRIETARY INFORMATION. UNAUTHORIZED REPRODUCTION OR USE PROHIBITED.
SIZE D 400062XX





NOTES:

1. EMI FILTER REQUIRED ON -03 AND -04 VERSIONS ONLY.
2. LOCATION OF R34 ON -04 VERSION.
3. COMPONENTS T9, L5, R33, R34, BR4, C26, C , C28 AND C32 ARE NOT USED ON -03 VERSION.

DRAWINGS FURNISHED BY L.H. RESEARCH INC.
FOR MAINTENANCE PURPOSES ONLY.

J G E C A	R M F D B	DRAWN N C	DATE 10-25-77	Diablo Systems Incorporated	
				POWER SUPPLY 3 AND 4 OUTPUT	
				115/230VAC	
				SCALE 1:1	SHEET 4 TOTAL SH 4
				SIZE D	400062-XX

NOTES: UNLESS OTHERWISE SPECIFIED,
1. ALL RESISTANCES SPECIFIED IN OHMS.
2. ALL RESISTORS ARE 1/4 WATT, ± 5%.
3. ALL CAPACITANCE SPECIFIED IN MICROFARADS.
4. +5V TO PIN 14 OF 14-PIN IC, GND TO PIN 7;
   +5V TO PIN 16 OF 16-PIN IC, GND TO PIN 8.

8 – POR
9 + BUSY
(– READY)

D1 1N4148
C2 4700PF
R1 220 10% +5V
C1 0.1
U2 74145 DCDR/DRVR
KEYSWITCH MATRIX
U12 833
TPA
R2 470
C5 220PF 10%
C3 0.01
C4 2200 PF
R6 4.7K
R9 4.7K
R3 2.2K
R4 120
R5 2.2K
U1 CA3086
TPB
R8 2.2K
R7 3.3K 10%
C6 0.01
-12V
U3 74LSØ2
U5 74LSØ8
U9 74LSØ8
U14 74145 DCDR/DRVR
U13 74145 DCDR/DRVR
U8 74LSØØ
U10 74LSØ4
R14 2.2K
U7 74LS74 D-FF
U5 74LSØ8
U9 74LSØ8
– KYSTB 12
R10 1.2K 10%
R11 1.5K
R12 2.2K
R13 2.2K
C7 .015 10%
U4 7405 OC
TPC
U6 MM5873 (CHIP "C") MPROC
SRIN FF FN NKR/2KR CLK IN LI STB SRO BSL VSS VDD VGG
U11 74LSØ4
– DØ 13
– D1 16
– D2 18
– D3 20
– D4 19
– D5 17
– D6 15
– D7 14
DØ TO D7
C12 22 +5V
C9 C13 C14 C15 0.1
C10 10
C8 C11 0.1
– 12V

10 μSEC
TPC
φ1
φ3
– KYSTB
BUSY
– POR
IF KEY IS DEPRESSED OR RELEASED

SCHEMATIC DIAGRAM

RS

DRAWN MC	DATE 6-30-77	Diablo Systems Incorporated, Hayward, California 94545
CHECKED R.W. Fifield	DATE 7-12-77	
ENGR J. Worthington	DATE 7/28/77	
ENG. R. Brown	DATE 9/26/77	
FIRST USED NEXT ASSY 400073-01		CORTRON UP/DN STROKE KEYBOARD
SHEET 1	TOT SHT 2	SIZE D DWG NO 400094-01

REV A ECO NO 7901 10-11-77

DEVELOPMENT REV D1

400094-01 ON DWG

NOTE:

MATRIX	OUTPUT CODE
B1	B1
B2	B2
B3	B3
B7	B4
B5	B5
B6	B6
B4	B7

BIT 7 →					0	0	0	0	1	1	1	1	SENSE ADDRESS
BIT 6 →					0	0	1	1	0	0	1	1	
BIT 5 →					0	1	0	1	0	1	0	1	
B4	B3	B2	B1		SØ	S1	S2	S3	S4	S5	S6	S7	
0	0	0	0	DØ	1	35	37	39	45	43	41	32	ALPHA / NUMERIC OUTPUT B7 = Ø
0	0	0	1	D1		52	54	56	TEST CORE D2 61	63	58	50	
0	0	1	0	D2		36	38	40	46	44	42	34	
0	0	1	1	D3	17	21	23	25	31	29	27	19	
0	1	0	0	D4		20	22	24	30	28	26	18	
0	1	0	1	D5	1	5	7	9	15	13	11	3	
0	1	1	0	D6	2	6	8	10	16	14	12	4	
0	1	1	1	D7	47	51	53	55	62	59	57	SHIFT 33 / SHIFT 49 / SHIFT LOCK 60	
1	0	0	0	D8								76	RIGHT HAND PAD OUTPUT B7 = 1 B3 = Ø
1	0	0	1	D9	73	70	67	64				77	
1	0	1	0	DA	74	71	68	65				78	
1	0	1	1	DB	75	72	69	66				79	
1	1	0	0	DC	90	87	84	81				93	LEFT HAND PAD OUTPUT B7 = 1 B3 = 1
1	1	0	1	DD	91	88	85	82				94	
1	1	1	0	DE				TEST CORE D1 48				95	
1	1	1	1	DF	89	86	83	80				92	

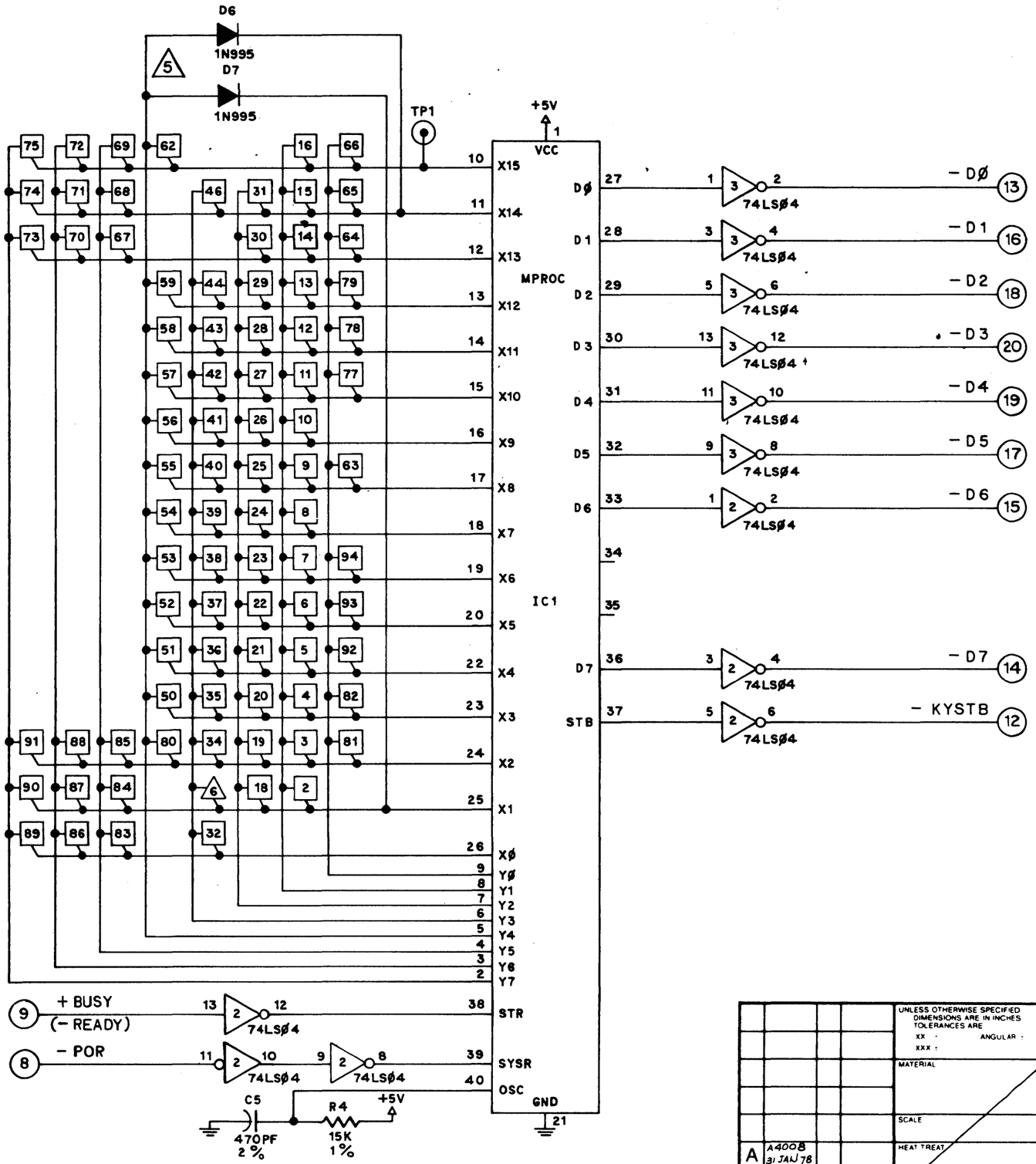
DRIVE ADDRESS

SCHEMATIC DIAGRAM

DRAWN NJC	DATE 7-1-77	Diablo Systems Incorporated Hayward, California 94545	
CHECKED R.W. Folick	DATE 7-12-77		
ENGR	DATE 7/26/77		
MFG L. Brown	DATE 9/26/77		
FIRST USED (NEXT ASSY) 400073-01		CORTRON UP/DN STROKE KEYBOARD	
SHEET 2	TOT SHT 2	SIZE D	DWG NO 400094-01

REV A E.C.O. NO. 1901 10-11-77

DEVELOPMENT REV D1



NOTES: UNLESS OTHERWISE SPECIFIED,

1. ALL RESISTANCES SPECIFIED IN OHMS.
2. ALL RESISTORS ARE 1/4 WATT, ± 5 %.
3. ALL CAPACITANCE SPECIFIED IN MICROFARADS.
4. +5V TO PIN 14 OF 14-PIN IC, GND TO PIN 7;
   +5V TO PIN 16 OF 16-PIN IC, GND TO PIN 8.

△5 DIODES 6 AND 7 ARE INSTALLED ON KEYBOARD BY THE MANUFACTURER FOR DIAGNOSTIC CODE CHECKS OF STATIONS 48 AND 61.

△6 SECRETARY SHIFT STATIONS 33, 49 AND 60 ARE LOCATED HERE.

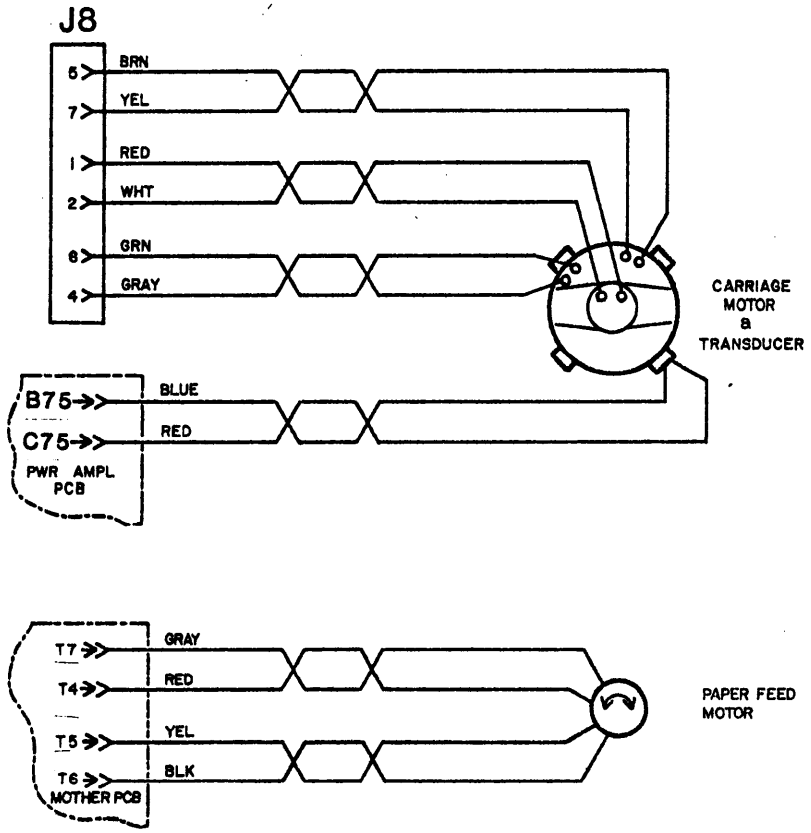
DRAWINGS FURNISHED BY MICRO SWITCH, FREEPORT, ILL., FOR MAINTENANCE PURPOSES ONLY.

BISHOF GRAPHICS/ACCUFRESS

400285-01

SCHEMATIC DIAGRAM RS

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE XX ANGULAR : XXX :	DRAWN NC	DATE 11-16-77	Diablo Systems Incorporated Hayward, California 94545
MATERIAL	CHECKED R.W. Fifield	DATE 12-21-77	
SCALE	ENGR	DATE 21 DEC 77	
HEAT TREAT	MFG L. BROWN	DATE 2/1/78	
FINISH	FIRST USED IN EXT ASSY 400000-XX		MICRO SWITCH UP/DN STROKE KEYBOARD
A A4008 31 JAN 78 REVISIONS	SHEET 1	TOT SHT 2	SIZE C / DWG NO 400285-01



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