

DataGeneral

**TECHNICAL
STATEMENT**

TEXT LISTING

068-001067-01

PROGRAM

ARRAY PROCESSOR EXERCISER-C

TEXT TAPE

097-001067-01

ABSTRACT

THIS PROGRAM IS A FUNCTIONAL TEST FOR THE ARRAY PROCESSOR (AP).
IT IS EXECUTED BY A CENTRAL PROCESSOR (OR IOP) CONTROLLING THE
AP AND TESTS SPECIFIC AP INSTRUCTIONS.

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0001 APC.T
01 ***** 09:37:54 09/19/79 *****
02 ; NAME: APC.TX PART NUMBER 097-1067
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06 ; DESCRIPTION: ARRAY PROCESSOR EXERCISER-C.
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09 ; REVISION HISTORY:
10 ;
11 ; REV. DATE
12 ; 00 03/29/78
13 ; 01 12/29/78
14 ;
15 ;
16 ; COPYRIGHT © DATA GENERAL CORPORATION, 1978
17 ; ALL RIGHTS RESERVED.
18 ; *****
19 ; *****

0002 APC.T
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03 ; PART NUMBER: 097-1067
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06 ; PROGRAM NAME
07 ; 1.0
08 ; SOURCE FILE: APC.SR
09 ; DTOS FILE: APC EXER
10 ;
11 ; REVISION HISTORY
12 ;
13 ; DATE REVISION
14 ; ----
15 ; XX/XX/78 00
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17 ; MACHINE REQUIREMENTS
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19 ; 1. ECLIPSE FAMILY CENTRAL PROCESSOR (HOST OR IOP)
20 ; WITH AT LEAST 16-K READ/WRITE MEMORY
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22 ; 2. ARRAY PROCESSOR BOARDS AP1, AP2, AP3
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24 ; 3. BASIC I/O TELETYPE INTERFACE AND CONTROL
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26 ; TEST REQUIREMENTS
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28 ; 1. SAME AS MACHINE REQUIREMENTS
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30 ; 2. I/O TESTER OR DISC
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32 ; 3. MMPU1
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34 ; SUMMARY
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36 ; THIS PROGRAM IS A FUNCTIONAL TEST FOR
37 ; THE ARRAY PROCESSOR (AP). IT IS EXECUTED BY
38 ; A CENTRAL PROCESSOR (OR IOP) CONTROLLING THE AP
39 ; AND TESTS SPECIFIC AP INSTRUCTIONS.
40 ;
41 ; RESTRICTIONS
42 ;
43 ; THE PROGRAM ASSUMES
44 ; - THE SYSTEM EXCLUDING THE AP IS ERROR FREE
45 ; - THE HOST COMPUTER AND MEMORY/MAP SYSTEMS
ARE WORKING PROPERLY.
- THE 2 AP MAINTENANCE DIAGNOSTICS USING
THE MAINTENANCE INSTRUCTION SET (MIS)
HAVE BEEN SUCCESSFULLY RUN.

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10003 APC.1

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01 PROGRAM DESCRIPTION/THEORY OF OPERATION
02 APC TEST DESCRIPTION
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?7.0 PROGRAM DESCRIPTION/THEORY OF OPERATION
APC TEST DESCRIPTION

?7.1 APC TESTS THE FOLLOWING INSTRUCTIONS:

ARA = ADD REAL ARRAYS
SRA = SUBTRACT REAL ARRAYS
CMA = COMPARE REAL ARRAYS
MCA = MULTIPLY REAL ARRAYS
SPR = SIGNED PRODUCT OF REAL ARRAYS
SPS = SIGNED PRODUCT OF SCALAR AND REAL ARRAY

TESTING OF ARA
?7.1.1 THE MAIN CONCEPT INVOLVED IN MOST OF THIS TEST
CAN BE DESCRIBED AS FOLLOWS:
GIVEN A SEQUENTIAL, FLOATING POINT ARRAY "X"
OF INDEX VALUE "I".
AND A SEQUENTIAL, FLOATING POINT ARRAY "Y" OF
INDEX VALUE "J" AND STARTING AT 0.0. THEN
[X] + [Y] = [Z]
WHERE [X] MEANS ARRAY "X"

WHERE THE ARRAY "Z" WOULD BE EQUAL TO THE ARRAY
"X" ONLY NOW INDEXED BY I + J
THIS CONCEPT ENABLES US TO EXERCISE THE INDEXING
FUNCTIONS OF ARA AT THE SAME TIME TESTING VARIATION
OF N AND OTHER PARAMETER VARIATIONS.

A) THE FIRST ARA TEST IS SIMPLE. THE AP RAM IS
DIVIDED INTO THREE SECTIONS. THE LOWER SECTION IS
LOADED WITH SEQUENTIAL FLOATING POINT DATA FROM THE
BUFFER IN MAIN MEMORY STARTING AT FDATA. THE
SECOND SECTION IS LOADED WITH 1.0'S. THESE TWO
ARRAYS ARE USED AS INPUT FOR THE ARA INSTRUCTION.
THE OUTPUT IS A SEQUENTIAL FLOATING POINT ARRAY.
THIS WILL BE STORED IN THE UPPER ONE THIRD OF THE
AP RAM. THIS ARRAY SHOULD COMPARE EQUALLY TO THE
ARRAY STARTING AT FDATA*2 IN MAIN MEMORY. AND
INDEED THIS IS CHECKED WITH THE RCOMP ROUTINE.
NUMBER OF ELEMENTS IS VARIED FROM 2 TO 1252 BY 2'S.
ALL INDEXES ARE EQUAL TO ONE.

B) THE SECOND TEST IS SIMILAR TO THE FIRST TEST.
ONCE AGAIN SEQUENTIAL FLOATING POINT NUMBERS, FROM
THE BUFFER STARTING AT FDATA, ARE LOADED TO THE
LOWER ONE THIRD OF AP RAM. TO THE 2ND ONE THIRD
OF AP RAM GOES A BUFFER LOADED WITH 1.0'S. THIS
BUFFER STARTS AT IDATA IN MAIN MEMORY. THEN A
RANDOM SLICE OF BOTH THESE SECTIONS IN RAM IS TAKEN.
THESE SLICES ARE USED AS THE INPUT ARRAYS TO THE
ARA INSTRUCTION. THE OUTPUT ARRAY IS STORED IN
ANOTHER RANDOM SLICE IN THE TOP ONE THIRD OF AP
RAM. THIS ARRAY IS COMPARED TO THE CORRESPONDING
SLICE OF THE FDATA BUFFER. THIS TEST CHECKS OUT
VARIATION OF INPUT AND OUTPUT STARTING ADDRESSES
AND VARIATION OF N.

10004 APC.1

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C) TESTS #3 AND #4 CHECK OUT THE INDEXING CAP-
ABILITIES OF THE ARA INSTRUCTION USING THE
CONCEPT DISCUSSED AT THE BEGINNING OF THIS SECTION.
IN THESE TESTS THE TWO INPUT ARRAYS ARE SEQUENTIAL
FLOATING POINT ARRAYS LOADED FROM THE FDATA BUFFER
INTO AP RAM. IN BOTH TESTS (#3 AND #4) THE INPUT
INDEXES ARE 6 AND 1. THEREFORE THE OUTPUT ARRAY
SHOULD COMPARE TO A SEQUENTIAL FLOATING POINT ARRAY
WITH AN INDEX OF 7. THIS IS CHECKED. N IS FIXED
IN ALL CASES AT 112.

D) TEST #5 CHECKS OUT THE OUTPUT INDEXING FUNCTION
OF THE ARA INSTRUCTION. THIS IS DONE WITH INPUTS
OF A SEQUENTIAL FLOATING POINT ARRAY AND AN ARRAY
OF ALL 1.0'S.
THE ARA INSTRUCTION IS THEN EXECUTED WITH AN OUTPUT
INDEX OF NON-UNITY. RESULTS ARE CHECKED BACK WITH
FDATA BUFFER.
E) TEST #6 AND #7 USE THE INDEXING CONCEPT EXPLAINED
IN THE BEGINNING OF THIS SECTION.
IN BOTH TESTS N, IJ, IK, IL ARE VARIED. IN #6
VARIATION IS SEQUENTIAL. IN #7 VARIATION IS RANDOM.
THE DATA USED IS THE SEQUENTIAL DATA LOADED FROM
THE FDATA BUFFER.

?7.1.2 THE ARA INSTRUCTION TESTS ARE ALMOST IDENTICAL TO
THE ARA TESTS. EXCEPTIONS ARE NOTED IN THE COMMENTS.

?NOTE: IN BOTH ARA AND SRA TESTS WE HAVE AVOIDED SIMULATION.
THIS ENABLES US TO DO A MUCH MORE EXHAUSTIVE TEST.

10005 APC.T

01 MRA TESTS ARE MORE STRAIGHT FORWARD. HERE WE SIM-
02 ULATE MRA INSTRUCTION.
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05 A) TEST #1 VARIES N FROM 2-1252(8). THE DATA IS
06 SEQUENTIAL FLOATING POINT DATA LOADED FROM FDATA
07 AND FDATA*26.
08 BOTH INPUT ARRAYS ARE LOADED INTO THE LOWER 2/3 OF AP
09 RAM. THE OUTPUT GOES TO THE TOP 1/3. THE INDEXES=1.
10
11 THE INSTRUCTION IS SIMULATED AND THE OUTPUT GOES TO
12 THE IDATA BUFFER. THE INSTRUCTION IS THEN EXECUTED
13 AND SIMULATED AND AP DATA ARE COMPARED.
14
15 B) IN TEST #2 WE SLICE THE TWO INPUT ARRAYS AND
16 THE OUTPUT ARRAY GOES TO A RANDOM SLICE.
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18 NOTE: IN THIS TEST THE SIMULATION OF MRA INSTRUCTION IS
19 DONE IN THE BEGINNING THE REAL VARIATION IS DONE
20 IN THE SLICING. THIS WILL CHECK VARIOUS START
21 ADDRESS AND N'S.
22
23 C) TESTS #3 AND #4 VARY N, IJ, IK, IL. OTHERWISE
24 IT IS SIMILAR TO ALL PREVIOUS TESTS OF MRA.
25 THE INPUT ARRAYS ARE LOADED TO AP RAM FROM SECTIONS
26 OF FDATA. THE INSTRUCTION IS SIMULATED AND THEN
27 EXECUTED AND RESULTS ARE COMPARED. SIMULATED
28 RESULTS ARE ATIDATA.
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30 TEST #4 IS RANDOM VARIATIONS
31 TEST #5 IS SEQUENTIAL VARIATIONS
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33 SPR TESTS ARE IDENTICAL TO MRA EXCEPT A DIFFERENT
34 SIMULATOR IS USED.
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10006 APC.T

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7.2.5 SPS TEST DESCRIPTION.
THESE TESTS USE THE SEQUENTIAL FLOATING DATA ATIDATA,
AND A SCALAR OF 2.0. ALL TESTS USE THE SIMULATOR
APPROACH.
A) TEST #1 VARIES N FROM 0-1024 BY
B) TEST #2 VARIES N AND IJ RANDOMLY
C) TEST #3 IS A RANDOM SLICE TEST.
MCA TESTS ARE THE SAME AS MRA TESTS.
THE CMA TESTS ARE AN EXHAUSTIVE SET OF TESTS.
EACH OPERATOR IS TESTED WITH THREE BASIC TESTS.
THE DATA USED IS TWO ARRAYS. ONE AT FDATA AND
ONE AT GDATA IN MM.
ONE IS A SEQUENTIAL VECTOR AND THE OTHER IS THE
INVERSE SEQUENTIAL VECTOR. THE CMA INSTRUCTION
IS SIMULATED IN ALL TESTS.
A) TEST #1 - THIS STRUCTURE VERIFIES, FOR EACH
OPERATOR THAT N CAN BE VARIED, WITH ALL OTHER
VARIABLES HELD CONSTANT. N GOES FROM 2-2000(8)
BY 2'S. SEQUENTIAL DATA FROM FDATA IS LOADED
STARTING AT RAM LOC 0. INVERSE SEQUENTIAL DATA
IS LOADED AT RAM LOC 2000. THE CMA INSTRUCTION
IS SIMULATED AND OUTPUT IS STORED IN HDATA ARRAY.
THE CMA INSTRUCTION IS DONE AND OUTPUT IS STORED
AT IDATA.
THE TWO INTEGER VECTORS ARE THEN COMPARED VIA THE
ICOMP ROUTINE.
IN THIS TESTS N VERIFIES FROM 2-2000 BY 2.
B) VTEST2 - THIS TEST STRUCTURE WILL TEST VARIOUS
INPUT ARRAY STARTING ADDRESS IN RAM AND VARIOUS
VALUES OF N. A RANDOM SLICE IS TAKEN OF EACH
INPUT ARRAY. THE TEST IS BASICALLY THE SAME AS
THE FIRST SET OF TESTS EXCEPT THAT THE INPUT
ARRAYS ARE RANDOMLY SLICED. THE INSTRUCTION IS
SIMULATED AND COMPARED TO AP RESULTS.
C) THE VTEST3 STRUCTURE.
THIS STRUCTURE VARIES THE N, IJ, IK FOR ANY CMA
OPERATOR.
THE SAME DATA IS USED AS IN PREVIOUS CMA TESTS AND
IS LOADED INTO AP RAM IN THE SAME MANNER AS IN
PREVIOUS TEST.
N VARIES FROM 1-5(8)
IJ, IK VARY FROM 1-5(8)
THE INSTRUCTION IS SIMULATED AND THEN EXECUTED.
SIMULATE RESULTS ARE STORED IN BOATA ARRAY.
AP RESULTS ARE AT IDATA.
BOATA IS THEN COMPARED TO IDATA.

10007 APC.T

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NOTE: THIS TEST IS OF A NESTED DO LOOP TYPE AND IS QUITE LONG.
D) THE FINAL TEST IS ONE WHICH VARIES N (1-77)
IJ, IK VARIES (1-77) AND OPERATOR IS VARIED ALL
RANDOMLY. IN ORDER TO VARY THE OPERATOR OF THIS
INSTRUCTION BITS 1-4 OF THE 2ND WD MUST BE
VARIED. IN ORDER TO DO THIS A CMA LT IS AS-
SEMBLED IN SCRATCH AREA. BITS 1-4 ARE VARIED
RANDOMLY AND THEN THE ENTIRE INSTRUCTION (BOTH
WDS) ARE STORED INTO THE TEST.
THIS IS DONE EACH TIME N, IJ, IK ARE CHANGED.

10008 APC.T

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S?WPD 8

SWITCH SETTINGS

LOCATION "SWREG" IS USED TO SELECT THE PROGRAM OPTIONS (NOT SYSTEM CONFIGURATION). WHILE RUNNING UNDER DTOS, THIS LOCATION WILL BE LOADED BY THE MONITOR. HOWEVER UNDER STAND ALONE AND PROGRAM LOAD MODES THIS LOCATION WILL BE SET ACCORDING TO THE ANSWERS SUPPLIED BY THE OPERATOR. IN ANY CASE THE OPTIONS CAN BE CHANGED OR VERIFIED BY USING ONE OF THE COMMANDS GIVEN IN SEC. 8.2

SWITCH OPTIONS
DIFFERENT BITS AND THEIR INTERPRETATION AT LOCATION "SWREG" IS AS FOLLOWS:

BIT	OCTAL VALUE	BINARY VALUE	INTERPRETATION
1	40000	1	LOOP ON ERROR SKIP LOOPING ON ERROR
2	20000	1	PRINT TO CONSOLE ABORT PRINT OUT TO CONSOLE
3	10000	1	DO NOT PRINT % FAILURE PRINT % FAILURE
4	04000	1	ALLOW END OF PASS PRINT OUT SUPPRESS END OF PASS PRINT OUT
5	02000	1	DO NOT PRINT ON THE LINE PRINTER PRINT ON THE LINE PRINTER
6	01000	1	DO NOT HALT ON ERROR HALT ON ERROR
7	0	0	DO NOT PRINT SUMMARY AND/OR PASSING OF EACH SUBTEST PRINT SUMMARY AND/OR PASSING OF EACH SUBTEST
8	00200	1	PRINT ONLY THE FIRST ERROR PRINT EVERY ERROR

SWITCH COMMANDS

8.2

ONCE THE PROGRAM STARTS EXECUTING THE STATE OF ANY OF THE BITS CAN BE CHANGED BY HITTING KEYS 1-9, A-F. THE PROGRAM WILL CONTINUE RUNNING AFTER UPDATING THE OPTIONS. EACH KEY WILL COMPLEMENT THE STATE OF THE BIT AFFILIATED WITH IT, THUS BIT 4 CAN BE ALTERED BY HITTING KEY 4. SETTING OF ANY BIT OF LOCATION "SWREG" WILL SET BIT 0. (DEFAULT MODE IS DEFINED AS ALL BITS OF SWREG SET TO 0) THE PROGRAM CAN BE LOCKED INTO SWITCH MODIFICATION MODE BY TYPING A 0, IN WHICH CASE MORE THAN ONE BIT CAN BE CHANGED BEFORE CONTROL IS ALLOWED TO RETURN TO THE MAIN PROGRAM.

10013 APC.T

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11.3 COMMON SUBROUTINES

A) ADSETP,SETP,LOOP - THESE ALL WORK IN CONJUNCTION TO SET UP THE TEST LOOP. ADSETP TELLS SETP WHERE THE LOOP ENDS. SETP MARKS THE START OF THE TEST LOOP. LOOP MARKS THE END OF THE TEST LOOP. THE AP INSTRUCTION IS EXECUTED AND THE RESULTS ARE CHECKED FOR ERROR WITHIN THIS TEST LOOP. IF AN ERROR OCCURS THEN THE PROGRAM CAN LOOP INDEFINITELY BETWEEN THE SETP AND THE LOOP. (SEE SECTION 6 ON VARIOUS SWITCH SETTINGS).

NORMALLY, WITH NO ERRORS, THE PROGRAM WILL GO THROUGH THIS LOOP ONCE ON THE FIRST PASS OF THE PROGRAM. ON SUBSEQUENT PASSES THE PROGRAM WILL STAY IN THE LOOP FOR 5 LOOPS. (OK 100. DEPENDING ON THE PROGRAM).

B) PARAMETER BLOCK LOADER ROUTINES - THESE CALLS ALL HAVE DIFFERENT NAMES DEPENDING ON THE INSTRUCTION. HOWEVER THEY OPERATE IN THE SAME MANNER. THE COMMENT FIELD ON THE CALL WILL ALWAYS INDICATE THAT THIS IS A PARAMETER BLOCK LOAD ROUTINE AND WILL NAME THE AP INSTRUCTION THAT THE LOAD IS COMPATIBLE WITH. THE ARGUMENTS OF THE CALL ARE THE PARAMETERS OF THE AP INSTRUCTION. THESE PARAMETERS ARE TO BE LOADED BY THESE ROUTINES INTO MAIN MEMORY AT A LOCATION POINTED TO BY AC2. AC2 MUST ALWAYS POINT TO THE PARAMETER BLOCK DURING AP INSTRUCTION EXECUTION.

10014 APC.T

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C) SLICING ROUTINES - THESE TYPES OF ROUTINES EXIST IN SEVERAL DIFFERENT FORMS. THEY ALL HAVE VERY SIMILAR NAMES. FOR EXAMPLE - SLICE, SLICC,SLICA,SLICB. THESE ARE ALL JSR'S TO SOME SLICING ROUTINE. THE SLICING ROUTINES WILL SET UP VARIOUS RANDOM SLICES IN AP RAM FOR THE VARIOUS INPUT AND OUTPUT ARRAYS USED IN THE AP INSTRUCTIONS. TO CREATE THESE SLICES, RANDOM N AND STARTING ADDRESS ARE CREATED. THE COMMENTS ON THE CALL WILL INDICATE THE DESTINATION OF THESE RANDOM PARAMETERS WITHIN THE TEST CODE. THE ROUTINES ALL SLICE DIFFERENTLY. ONE WILL DIVIDE THE RAM IN HALF AND THEN FIND A RANDOM SLICE WITHIN EACH HALF. ANOTHER MIGHT FIND A RANDOM SLICE FOR EACH THIRD OF RAM.

10015 APC.T

SEQUENCE OF TESTING

11.4

10016 APC.T

02D0D 12

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12.1

12.2

12.3.1

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IT IS IMPORTANT THAT THE PROGRAMS BE EXECUTED IN A SPECIFIC SEQUENCE:

APIS DIAG (CPU/AP ONLY)
 APP DIAG (CPU/AP ONLY)
 APB EXER
 APC EXER
 APD EXER
 APE EXER
 APF EXER
 APG EXER
 APH EXER
 API EXER
 APJ EXER
 APK EXER

THE DIAGNOSTIC IS EQUIPPED WITH A BUILT IN ODT WHICH CAN BE ACCESSED BY HITTING CONTROL 0 ("O") AT ANY TIME DURING THE EXECUTION OF THE PROGRAM (AFTER SETTING THE PARAMETERS).

ON ENTERING ODT THE ADDRESS OF THE LOCATION HAVING THE NEXT INSTRUCTION TO BE EXECUTED WILL BE TYPED-OUT.

CONVENTIONS AND SYMBOLS

THE FOLLOWING CONVENTIONS ARE USED BY THE ODT:

? PRESSING ANY ILLEGAL KEY CAUSES THE ODT TO RESPOND WITH A "?".

o ODT IS READY AND AT YOUR SERVICE.

COMMAND STRUCTURE

AN ODT COMMAND HAS THE FOLLOWING FORMAT:

[ARGUMENT] [COMMAND]

AN ARGUMENT MAY BE ONE OF THE FOLLOWING:

"EXP" AN OCTAL EXPRESSION CONSISTING OF OCTAL NUMBERS SEPARATED BY PLUS (+) OR MINUS (-) SIGNS. LEADING ZEROS NEED NOT BE TYPED.

"ADR" AN ADDRESS IS THE SAME AS AN EXPRESSION EXCEPT THAT BIT 0 IS NEGLECTED.

A COMMAND IS A SINGLE TELETYPE CHARACTER

ODT COMMANDS

THE LOCATIONS THAT CAN BE EXAMINED AND MODIFIED BY THE USER ARE CALLED CELLS. THESE CELLS ARE OF TWO TYPES: INTERNAL CPU CELLS AND MEMORY LOCATIONS.

OPENING INTERNAL CELLS

THE COMMAND TO OPEN ONE OF THE INTERNAL REGISTERS IS OF THE FORM "NA" WHERE N IS ANY OCTAL EXPRESSION BETWEEN 0 AND 7

FOR ACCUMULATORS 0-3 FOR PC OF THE NEXT INSTRUCTION TO BE EXECUTED IN THE EVENT OF A "P" COMMAND.

CPU AND TIO STATUS BIT INTERPRETATION

15 STATUS OF TIO DONE FLAG

14 STATUS OF INTERRUPTS (ION FLAG)

13 STATUS OF CARRY BIT

6 ADDRESS OF THE LOCATION HAVING THE BREAK POINT (IF ANY)

7 INSTRUCTION AT THE BREAK POINT LOCATION

OTHER COMMANDS TO OPEN CELLS ARE:

"ADR"/ OPEN THE CELL AND PRINT ITS CONTENTS

"/ OPEN THE CELL CURRENTLY POINTED TO BY THE POINTER AND PRINT ITS CONTENTS.

."ADR"/ ADD "ADR" TO THE POINTER, OPEN THE CELL AND PRINT ITS CONTENTS.

.-"ADR"/ AND SUBTRACT "ADR" FROM THE POINTER, OPEN THE CELL AND PRINT ITS CONTENTS.

"CR" THE RETURN KEY IS USED TO CLUSE THE OPEN CELL

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0017 APC.T
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02 WITH OR WITHOUT MODIFICATION.
03 LINE FEED IS USED TO CLOSE THE OPEN CELL WITH OR
04 WITHOUT MODIFICATION AND TO OPEN THE SUCCEEDING
05 CELL. THE OPEN CELL WITH OR WITHOUT MODIFICATION
06 AND OPEN THE PRECEDING CELL
07 CLOSE THE OPEN CELL WITHOUT MODIFICATION, AND
08 OPEN THE CELL POINTED TO BY ITS CONTENTS.
09 "+ADR"/ OPEN THE OPEN CELL WITHOUT MODIFICATION, AND
10 OPEN THE CELL POINTED TO BY ITS CONTENTS + "ADR".
11 "-ADR"/ CLOSE THE OPEN CELL WITHOUT MODIFICATION, AND
12 OPEN THE CELL POINTED TO BY ITS CONTENTS - "ADR".
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10018 APC.T
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SPECIAL NOTES/SPECIAL FEATURES
13.1 FOR A COMPLETE TEST ALL PROGRAMS SHOULD BE EXECUTED WITH CAT/KITTEN.
13.2 A NOTE ABOUT AP ADDRESSING
ADDRESSES IN THE AP CAN BE OF SEVERAL MODES:
1) ONE WORD MODE (IE) SAME AS STANDARD ADDRESSING
2) TWO WORD MODE (2WM) - EACH 32 BITS IS NOW ONE ADDRESS SPACE. THIS IS USED IN THE AP TO SIMPLIFY REAL NUMBER ADDRESSING.
3) FOUR WORD MODE (4WM) - EACH 64 BITS IS NOW ONE ADDRESS SPACE. THIS IS USED IN THE AP TO SIMPLIFY COMPLEX NUMBER ADDRESSING.

THE AP ACCESSES AN ADDRESS RELATIVE TO THE START OF THE AP RAM. THUS AP RAM LOC 0 WOULD BE THE FIRST LOCATION THAT IS IN THE AP. HOWEVER, AS FAR AS THE ECLIPSE CPU IS CONCERNED, AP LOC 0 IS CONTAINED AT LOCATION LABEL "RAMPT". (IN PAGE ZERU. SO, IF RAMPT CONTAINS 64000, THEN 2000 2WM (AP RAM) IS REALLY 64000+2000*2000=70000.

NOTE: "STOP ON STORE" OR "STOP ON ADDRESS" IN AP RAM SPACE WILL NOT WORK IF THE AP IS USING THE INTERNAL AP ADDRESS LINES TO ACCESS AP RAM.

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10019 APC.I      ?14.0  RUN TIME
01      ?
02      ?
03      ?      14.1  PASS 1      40 SECONDS
04      ?
05      ?      14.2  SUBSEQUENT PASSES  1 MIN. 40 SECONDS
06      ?      .TTL APC.TX
08      ?      .END
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0020 APC.T

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020TD 001551 MC 16/02
S?MPD 001075 MC  8/01
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**00000 TOTAL ERRORS, 00000 PASS 1 ERRORS