

TEXT LISTING

068-000516-01

PROGRAM

S-130 WRITABLE CONTROL
STORE DIAGNOSTIC; PART 4

TEXT TAPE

097-000516-01

ABSTRACT

THIS PROGRAM IS 1 OF 5 DESIGNED TO TEST THE FUNCTIONAL OPERATION OF THE WRITABLE CONTROL STORE OPTION (WCS). THIS PROGRAM SHOULD NOT BE RUN UNTIL ALL THE C.P. AND I/O TEST PROGRAMS HAVE BEEN SUCCESSFULLY EXECUTED. THE LAST STEP IN THE TEST PROCEDURE SHOULD BE THE EXECUTION OF ALL THE WCS TEST PROGRAMS WITH THE CAT/KITTEN RUNNING IN THE BACKGROUND.

10003 WCS

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THIS DIAGNOSTIC IS DESIGNED TO RUN IN AN
AUTO-LOAD AUTO-RUN ENVIRONMENT.

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OPERATION OF THE WRITABLE CONTROL STORE OPTION (WCS).

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EXECUTION OF ALL THE WCS TEST PROGRAMS WITH THE
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MACHINE REQUIREMENTS

2.1 ECLIPSE S-130 PROCESSOR
2.2 8K OF READ/WRITE MEMORY
2.3 TTY OR CRT
2.4 WCS OPTION IN SECTOR 2
2.5 I-O TESTER (OPTIONAL)

PLEASE NOTE THAT FOR A COMPLETE TEST, SUCH
AS IN FACTORY TEST, THE I-O TESTER
MUST BE IN THE SYSTEM.

OPERATING PROCEDURE

3.0
3.1 LOAD PROGRAM VIA THE BINARY LOADER.
3.2 START ADDRESS
SET SWITCHES TO 200 OCTAL.
THE PROGRAM STARTS OUT BY PRINTING THE
PROGRAM NAME AND REVISION NUMBER ALONG
WITH THE EXISTENCE OF THE I/O TESTER.
3.3 SWITCH SETTINGS
SWITCH 0 (0) = USE CONTENTS OF SWREG"
SWITCH 0 (1) = USE DATA SWITCHES
SWITCH 1 (1) = PROCEED FROM ERROR
SWITCH 2 (1) = INHIBIT PRINTOUT TO TTY
SWITCH 3 (1) = PRINT FAILURE RATE, ALSO THE #
OF ITERATIONS FOR CURRENT TEST.
SWITCH 4 (1) = DO NOT PRINT PASS MESSAGE AT
END OF TEST.
SWITCH 5 (1) = ENABLE PRINTOUT TO LPT

PLEASE NOTE THAT THE OPTION TO USE THE
DATA SWITCHES OR THE CONTENTS OF "SWREG"
MAY ONLY BE EXERCISED AT THE BEGINNING OF
THE PROGRAM OR FOLLOWING AN ERROR HALT.

3.4 NORMAL OPERATION
PROGRAM WILL EXECUTE ALL TESTS IN SEQUENCE
AND AUTOMATICALLY LOOP. IF SWITCH 4 IS RESET,
A PASS MESSAGE WILL BE PRINTED AT THE
END OF EACH PASS, ALONG WITH THE PASS COUNT
IN DECIMAL. IF SWITCH 4 IS SET, THE
PASS COUNT WILL BE ACCUMULATED, BUT NOT
PRINTED.

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THE FAILING SEQUENCE MAY BE SINGLE INSTRUCTED STARTING AT THE POINT PRECEDING THE XOP1 INSTRUCTION WHERE THE ACS ETC. ARE INITIALIZED UP TO BUT NOT INCLUDING THE XOP1 INSTRUCTION. AT THE XOP1 INSTRUCTION, ONE MAY MICRO INSTRUCT THROUGH THE ROM ADDRESS LIGHTS WILL EQUAL 10 WHEN ENTRY TO SECTOR 2 WCS IS MADE. THE MICRO-ROUTINE MAY THEN BE MICRO-INSTRUCTED.

5.4 MONITOR LOCATIONS

THE FOLLOWING LOCATIONS IN PAGE 0 MAY BE MONITORED/EXAMINED TO PROVIDE ADDITIONAL INFORMATION.

LOC 200 USED BY DTOS
 LOC 201 ADDRESS OF SETUP +1 OF LAST TEST ENTERED
 LOUPT LOC 202 PROGRAM STARTING ADDRESS
 ISTART LOC 203 PROGRAM PASS COUNT
 PCATR LOC 204 ITERATION COUNT
 ITRCT LOC 205 RTC SWITCH, 0=NO RTC
 RTCS LOC 206 I/O TESTER SWITCH, 0=NO

6.0 PROGRAMMING DESCRIPTION FOR WCS FEATURE

6.1 XOP1 INSTRUCTION

XOP1 ACS, ACD, ENTRY NUMBER

WHEN AN XOP1 INSTRUCTION IS LOADED INTO THE IR BY A LOIR OR NLDLR MICRO-ORDER, THE SUBSEQUENT PHANTOM MICROINSTRUCTION HAS A DECI MICRO-ORDER IN ITS STATE CHANGE FIELD, AND SPECIAL HARDWARE FORCES THE SUCCEEDING MICROINSTRUCTION TO BE READ FROM SECTOR 2, PAGE 0 (THE CONTROL STORE RAM). SINCE DECI MAY YIELD A UNIQUE ADDRESS FOR EACH OF THE SIXTEEN POTENTIAL ENTRY NUMBERS IN AN XOP1 INSTRUCTION, EACH ENTRY NUMBER MAY SELECT THE BEGINNING OF A DIFFERENT MICROROUTINE IN THE CONTROL STORE RAM.

6.2 LCSF INSTRUCTION

THE LCSF INSTRUCTION MAY BE USED TO LOAD WCS.

ACO=UNUSED

0008 WCS
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AC1=# OF MICROINSTRUCTIONS
 AC2=SOURCE LOCATION IN MAIN MEMORY
 AC3=DESTINATION LOCATION IN WCS

0013 WCS

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01 2.CIN=(DECL AND CARRY)(ALC AND IRT)
02 3.LINK MODIFIED BY LEFT AND RIGHT SHIFTS
03 4.UNLESS ALC WITH IRL2=1
04 5.ALLOWS DCH BREAK UNLESS STIR OR SCND
05 6.DO NOT ALLOW DCH BREAK
06 7.DISABLE DCH BREAK
07 8.DO NOT CODE WITH ALEGI OR ACEGD
08 9.FALSE ADDRESS IS IN CURRENT PAGE,TRUE ADDRESS
09 MAY CHANGE CURRENT PAGE
10 10.INHIBITED BY HALT/STOP(IF RBUF55=0),INTERRUPT WAITING,
11 OR REXAM
12 13.INHIBITED BY HALT/STOP (IF RBUF55=0)
13 OR REXAM
14 14.DO NOT CODE WITH STIR
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16 FOR A COMPLETE DESCRIPTION OF THE MICRO-ORDERS,
17 PLEASE CONSULT THE DATA GENERAL
18 USERS MANUAL "S-130 MICROPROGRAMMING WCS FEATURE"
19 015-69-00
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10014 WCS

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9.0 TESTER DESCRIPTION

9.1 TEST BOARD COMMANDS

IORST - CLEAR THE TESTER
NI0C 0 - CLEAR THE TESTER(NEW MODE)
INTA - READ THE DATA BUFFER (NOT NEW MODE)
DIC - READ THE PULSE DETECTORS
DIB - READ THE DATA BUFFER
DIA - READ THE DCH ADDRESS BUFFER (NEW MODE)
DOA - LOAD THE DATA BUFFER
DOB - LOAD THE FUNCTION BUFFER
DOC - LOAD THE DATA AND DCH ADDRESS BUFFERS

9.2 FUNCTION REGISTER BIT ASSIGNMENTS

BIT 0 SET DCH SYNC
BIT 1 SET DCH MODE0
BIT 2 SET DCH MODE1
BIT 3 SET PI SYNC
BIT 4 BUSY (IF NOT NEW MODE)
BIT 5 DONE (IF NOT NEW MODE)
BIT 6 NEW MODE
BITS 7-9 THE # OF ROENB PULSES BETWEEN
SUCCESSIVE DCH CYCLES.
BITS 10-15 # OF DCH CYCLES

9.3 PULSE DETECTOR BIT ASSIGNMENTS

BIT 0 IOPLS
BIT 1 INTA (INTA + DCHP)
BIT 2 MSKO
BIT 3 UCHI
BIT 4 OVFL0-NOT USED ON ECLIPSE
BIT 5 DCHO
BIT 6 DCHA
BIT 7 ROENB
BIT 8 DOA
BIT 9 DOB
BIT 10 DOC
BIT 11 DIA
BIT 12 DIB
BIT 13 DIC (NOT SET IF DEV. CODE=0)
BIT 14 STRT
BIT 15 CLR

PLEASE NOTE THAT DCH PRIORITY MUST BE WIRED TO THE SLOT IN WHICH THE I-0 TESTER IS RESIDENT. FAILURE TO DO THIS WILL CAUSE ERRORS WITH ANY TESTS WHICH ARE TESTING THE INTA PULSE DETECTOR AND/OR DATA CHANNEL.

10017 NCS

**00000 TOTAL ERRORS, 00000 PASS 1 ERRORS