DataGeneral

TECHNICAL STATEMENT

TEXT LISTING

068-000514-01

PROGRAM

S-130 WRITABLE CONTROL
STORE DIAGNOSTIC; PART 2

TEXT TAPE

097-000514-01

ABSTRACT

THIS PROGRAM IS 1 OF 5 DESIGNED TO TEST THE FUNCTIONAL OPERATION OF THE WRITABLE CONTROL STORE OPTION (WCS). THIS PROGRAM SHOULD NOT BE RUN UNTIL ALL THE C.P. AND I/O TEST PROGRAMS HAVE BEEN SUCCESSFULLY EXECUTED. THE LAST STEP IN THE TEST PROCEDURE SHOULD BE THE EXECUTION OF ALL THE WCS TEST PROGRAMS WITH THE CAT/KITTEN RUNNING IN THE BACKGROUND.

```
 0001 WCS   MACRO REV 06.20              14:20:07 11/09/77
01
02
03
04
05
06
07              ;*************************************************************
08              ;
09              ; NAME: EMLWCS8.TX                          PART NUMBER: 097-000514
10              ;
11              ;
12              ; DESCRIPTION: S-130 WRITABLE CONTROL STORE DIAGNOSTIC; PART 2
13              ;                TEXT FILE
14              ;
15              ;
16              ; REVISION HISTORY:
17              ;
18              ;       REV.            DATE
19              ;
20              ;       00              05/20/77
21              ;       01              11/11/77
22              ;
23              ; COPYRIGHT (C) DATA GENERAL CORPORATION, 1977
24              ; ALL RIGHTS RESERVED.
25              ;*************************************************************
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10002 WCS
01              ;
                        .TITLE  WCS
03              ;
04              ; ECLIPSE WRITABLE CONTROL STORE TEST
05              ;       PART    2
06
```

```
!0003 WCS
01
02                ;
03                ;EWCS
04                ;
05                ;
06                ;THIS DIAGNOSTIC IS DESIGNED TO RUN IN AN
07                ;AUTO-LOAD AUTO-RUN ENVIRONMENT.
08                ;
09                ;
10                ;1.0     ABSTRACT
11                ;
12                ;
13                ;
14                ;        THIS PROGRAM IS 1 OF 5  DESIGNED TO TEST THE FUNCTIONAL
15                ;        OPERATION OF THE WRITABLE CONTROL STORE OPTION (WCS).
16                ;
17                ;
18                ;        THIS PROGRAM SHOULD NOT BE RUN UNTIL ALL THE C.P.
19                ;        AND I/O TEST PROGRAMS HAVE BEEN SUCCESSFULLY EXECUTED.
20                ;
21                ;
22                ;        THE LAST STEP IN THE TEST PROCEDURE SHOULD BE THE
23                ;        EXECUTION OF ALL THE WCS TEST PROGRAMS WITH THE
24                ;        CAT/KITTEN RUNNING IN THE BACKGROUND.
25                ;
26                ;
27                ;
28                ;
29                ;
30                ;
```

```
!0004 WCS
01
02                ;
03                ;2.0     MACHINE REQUIREMENTS
04                ;
05                ;        2.1      ECLIPSE S-130  PROCESSOR
06                ;        2.2      8K OF READ/WRITE MEMORY
07                ;        2.3      TTY OR CRT
08                ;        2.4      WCS OPTION IN SECTOR 2
09                ;        2.5      I-O TESTER (OPTIONAL)
10                ;
11                ;                 PLEASE NOTE THAT FOR A COMPLETE TEST,SUCH
12                ;                 AS IN FACTORY TEST,THE I-O TESTER
13                ;                 MUST BE IN THE SYSTEM.
14                ;
15                ;
16                ;
17                ;3.0     OPERATING PROCEDURE
18                ;
19                ;        3.1      LOADING
20                ;                 LOAD PROGRAM VIA THE BINARY LOADER.
21                ;        3.2      START ADDRESS
22                ;                 SET SWITCHES TO 200 OCTAL.
23                ;                 PRESS START.
24                ;                 THE PROGRAM STARTS OUT BY PRINTING THE
25                ;                 PROGRAM NAME AND REVISION NUMBER ALONG
26                ;                 WITH THE EXISTENCE OF THE I/O TESTER.
27                ;        3.3      SWITCH SETTINGS
28                ;                 SWITCH 0 (0) = USE CONTENTS OF SWREG"
29                ;                 SWITCH 0 (1) = USE DATA SWITCHES
30                ;                 SWITCH 1 (1) = PROCEED FROM ERROR
31                ;                 SWITCH 2 (1) = INHIBIT PRINTOUT TO TTY
32                ;                 SWITCH 3 (1) = PRINT FAILURE RATE,ALSO THE #
33                ;                                OF ITERATIONS FOR CURRENT TEST.
34                ;                 SWITCH 4 (1) = DO NOT PRINT PASS MESSAGE AT
35                ;                                END OF TEST.
36                ;                 SWITCH 5 (1) = ENABLE PRINTOUT TO LPT
37                ;
38                ;                 PLEASE NOTE THAT THE OPTION TO USE THE
39                ;                 DATA SWITCHES OR THE CONTENTS OF "SWREG"
40                ;                 MAY ONLY BE EXERCISED AT THE BEGINNING OF
41                ;                 THE PROGRAM OR FOLLOWING AN ERROR HALT.
42                ;
43                ;        3.4      NORMAL OPERATION
44                ;                 PROGRAM WILL EXECUTE ALL TESTS IN SEQUENCE
45                ;                 AND AUTOMATICALLY LOOP.  IF SWITCH 4 IS RESET,
46                ;                 A PASS MESSAGE   WILL BE PRINTED AT THE
47                ;                 END OF EACH PASS,  ALONG WITH  THE PASS COUNT
48                ;                 IN DECIMAL.  IF SWITCH 4 IS SET, THE
49                ;                 PASS COUNT WILL BE ACCUMULATED, BUT NOT
50                ;                 PRINTED.
51                ;
52                ;
53                ;
```

```
10005 WCS
01
02              ;
03              ;4.0    ERROR DESCRIPTION
04              ;       4.1     NORMAL
05              ;               UPON THE DETECTION OF AN ERROR,THE CARRY,
06              ;               PC AND THE AC'S WILL BE PRINTED AND THEN
07              ;               THE PROGRAM WILL LOOP ON THE FAILING TEST.
08              ;               THE ADDRESS OF THE TEST FAILING IS
09              ;               CONTAINED IN LOCATION 201. CONSULT THE
10              ;               LISTING FOR A DETAILED TEST DESCRIPTION.
11              ;       4.2     ABNORMAL
12              ;               THERE ARE SEVERAL TYPES OF UNEXPECTED FAILURES
13              ;               WHICH WILL CAUSE A PROGRAM HALT.  THEY ARE AS
14              ;               FOLLOWS:
15              ;                       UNEXPECTED INTERRUPT
16              ;                       STACK OVERFLOW OR UNDERFLOW
17              ;               THE CAUSE OF ANY OF THESE FAILURES SHOULD BE
18              ;               CORRECTED BEFORE RESUMING TESTING.
19              ;
20              ;5.0    PROGRAM DESCRIPTION
21              ;       5.1 COMMON SUBROUTINE CALLS
22              ;               THE DIAGNOSTIC IS COMPRISED OF A SERIES OF
23              ;               SHORT TESTS.  BASICALLY, EACH TEST CONSISTS
24              ;               OF A SETUP PROCEDURE, ONE OR MORE EVALUATING
25              ;               CASES WITH ERROR CALLS, AND A LOOP CAPABILITY.
26              ;               EACH PARTICULAR TEST CASE IS DESCRIBED IN THE
27              ;               LISTING.  THE COMMON ROUTINES FOR SETUP (SETUP),
28              ;               ERROR CALLS (EHALT), AND LOOP (LOOP) ARE
29              ;               DESCRIBED HERE ALONG WITH OTHER COMMONLY
30              ;               USED ROUTINES.
31              ;
32              ;
33              ;               SETUP
34              ;               EACH TEST BEGINS WITH A CALL TO SETUP.  THIS
35              ;               ROUTINE  SETS  THE LOOP ADDRESS,
36              ;               RESETS CERTAIN ERROR SWITCHES AND ITERATION
37              ;               COUNTS,AND INITIALIZES THE USER STACK.
38              ;
39              ;               EHALT
40              ;               THIS ROUTINE IS CALLED WHEN AN ERROR
41              ;               IS DETECTED.INITIALLY IT WILL CAUSE
42              ;               A PROGRAM HALT.IT WILL THEN PERFORM
43              ;               SPECIFIC FUNCTIONS AS SELECTED VIA
44              ;               THE SWITCH REGISTER.
45              ;
46              ;
47              ;               LOOP
48              ;               THIS ROUTINE IS CALLED AT THE END OF EACH TEST
49              ;               SEQUENCE.  IT IS USED TO ITERATE THE SEQUENCE
50              ;               3  TIMES IF NO ERROR HAS BEEN DETECTED.
51              ;               IF AN ERROR HAS BEEN DETECTED, IT IS USED TO
52              ;               MAINTAIN THE SCOPE LOOP AND INTERROGATE THE
53              ;               SWITCHES, ETC.  THE USER STACK
54              ;               IS   ALSO INITIALIZED.
55              ;
```

```
10006 WCS
01              ;
02              ;
03              ;
04              ;       ARL
05              ;       LOAD EVERY LOCATION IN THE WCS RAM WITH THE
06              ;       MICRO-WORD THAT FOLLOWS THE CALL.
07              ;
08              ;       SRL
09              ;       LOAD ONE LOCATION IN THE WCS RAM WITH THE MICRO-WORD
10              ;       WHICH FOLLOWS THE CALL.THE LAST ENTRY IN THE
11              ;       MICRO-ORDER STRING DENOTES THE ADDRESS INTO WHICH
12              ;       THE MICRO-WORD WILL BE LOADED.
13              ;
14              ;E.G.   SRL AR PC ACS A1 F0 L N S N N N JUMP 0 10 0 4377
15              ;
16              ;       THE SPECIFIED MICRO-WORD FOLLOWING THE SRL CALL
17              ;       WOULD BE LOADED INTO LOCATION 4377 OCTAL IN  THE
18              ;       WCS RAM.
19              ;
20              ;
21              ;
22              ;
23              ;       5.2 TEST DESCRIPTION
24              ;
25              ;       EACH TEST STARTS VIA A CALL SETUP TO INITIALIZE
26              ;       THE STATE OF THE C.P.
27              ;       THE AC'S ARE SET UP TO THEIR TEST VALUES,THE DEC1
28              ;       AND DEC2 ROMS ARE PRE-LOADED  AS REQUIRED,AND A "TEST"
29              ;       MICRO-ROUTINE IS LOADED INTO THE WCS RAM.IN MOST CASES
30              ;       THIS "TEST" MICRO-ROUTINE STARTS AT LOCATION 0.AN XOP1
31              ;       IS THEN EXECUTED TO ENTER WCS.THE "TEST" MICRO-ROUTINE
32              ;       IS EXECUTED AND WCS IS EXITED.THE PROGRAM THEN CHECKS
33              ;       FOR EXPECTED RESULTS.
34              ;
35              ;       5.3 ERROR ANALYSIS
36              ;
37              ;       WCS ENTRY ERROR
38              ;
39              ;       IF A DEC1 ADDRESSING ERROR OCCURS WHILE ATTEMPTING TO
40              ;       ENTER WCS VIA AN XOP1 INSTRUCTION,THE PROGRAM WILL
41              ;       PROBABLY EXECUTE ONE MICRO-INSTRUCTION IN WCS RAM
42              ;       AND RETURN TO THE LOCATION OF THE XOP1+1.THE PROGRAM
43              ;       MUST BE MICRO-INSTRUCTED STARTING AT THE XOP1
44              ;       INSTRUCTION TO TRACE THE FAILING FLOW.
45              ;
46              ;       WCS EXIT ERROR
47              ;
48              ;       IF AN ERROR OCCURS IN AN ATTEMPT TO EXIT WCS,THE TEST
49              ;       WOULD RETURN TO THE LOCATION SPECIFIED BY THE PC.
50              ;
51              ;
52              ;
53              ;       EXPECTED RESULTS INCORRECT
54              ;
55              ;
56              ;       IF THE "TEST" MICRO-ROUTINE CAN BE EXECUTED IN WCS
57              ;       AND A SUCCESSFUL EXIT IS MADE BACK TO THE TEST PROGRAM,
58              ;       BUT THE  RESULTS ARE INCORRECT,THE "TEST"  MICRO-ROUTINE
59              ;       MUST BE CAREFULLY EXAMINED TO DETERMINE
60              ;       ITS PROPER EXECUTION.
```

```
01                ;
02                ;       THE FAILING SEQUENCE MAY BE SINGLE INSTRUCTED STARTING
03                ;       AT THE POINT PRECEEDING THE XOP1 INSTRUCTION WHERE
04                ;       THE AC'S ETC. ARE INITIALIZED UP TO BUT NOT INCLUDING
05                ;       THE XOP1 INSTRUCTION.AT THE XOP1 INSTRUCTION,ONE MAY
06                ;       MICRO INSTRUCT THROUGH THE XOP1,AND INTO WCS.NOTE THAT
07                ;       THE SECTOR BITS ON THE ROM ADDRESS LIGHTS WILL EQUAL 10
08                ;       WHEN ENTRY TO SECTOR 2 WCS IS MADE.THE  MICRO-ROUTINE
09                ;       MAY THEN BE MICRO-INSTRUCTED.
10                ;
11                ;
12                ;
13                ;       5.4 MONITOR LOCATIONS
14                ;
15                ;       THE FOLLOWING LOCATIONS IN PAGE 0
16                ;       MAY BE MONITORED/EXAMINED TO PROVIDE
17                ;       ADDITIONAL INFORMATION.
18                ;
19                ;               LOC 200     USED BY DTOS
20                ;       LOOPR   LOC 201     ADDRESS OF SETUP +1 OF
21                ;                           LAST TEST ENTERED
22                ;       ISTART  LOC 202     PROGRAM STARTING ADDRESS
23                ;       PCNTR   LOC 203     PROGRAM PASS COUNT
24                ;       ITRCT   LOC 204     ITERATION COUNT
25                ;       RTCS    LOC 205     RTC SWITCH,0=NO RTC
26                ;       IOTS    LOC 206     I/O TESTER SWITCH,0=NO
27                ;
28                ;
29                ;
30                ;
31                ;
32                ;
33                ;6.0    PROGRAMMING DESCRIPTION FOR WCS FEATURE
34                ;
35                ;
36                ;
37                ;
38                ;
39                ;
40                ;       6.1 XOP1 INSTRUCTION
41                ;
42                ;       XOP1 ACS,ACD,ENTRY NUMBER
43                ;
44                ;       WHEN AN XOP1 INSTRUCTION IS LOADED INTO THE IR BY
45                ;       A LDIR OR NILDIR MICRO-ORDER, THE SUBSEQUENT
46                ;       PHANTOM MICROINSTRUCTION HAS A DEC1 MICRO-ORDER
47                ;       IN ITS STATE CHANGE FIELD, AND SPECIAL HARDWARE
48                ;       FORCES THE SUCCEEDING MICROINSTRUCTION TO BE READ
49                ;       FROM SECTOR 2,PAGE 0 (THE CONTROL STORE RAM).  SINCE DEC1
50                ;       MAY YIELD A UNIQUE ADDRESS FOR EACH OF THE SIXTEEN
51                ;       POTENTIAL ENTRY NUMBERS IN AN XOP1 INSTRUCTION,
52                ;       EACH ENTRY NUMBER MAY SELECT THE BEGINNING OF A
53                ;       DIFFERENT MICROROUTINE IN THE CONTROL STORE RAM.
54                ;
55                ;
56                ;       6.2 LCSF INSTRUCTION
57                ;
58                ;       THE LCSF INSTRUCTION MAY BE USED TO LOAD WCS.
59                ;
60                ;       AC0=UNUSED
```



```
01                ;       AC1=# OF MICROINSTRUCTIONS
02                ;       AC2=SOURCE LOCATION IN MAIN MEMORY
03                ;       AC3=DESTINATION LOCATION IN WCS
04                ;
05                ;
```

```
10009 WCS
01
02
03
04                ;7.0    ROM CONTROL WORD
05                ;
06                ;
07                ;
08                ;
09                ;       THE 56 BIT ROM CONTROL WORD IS DIVIDED
10                ;       INTO THE FOLLOWING FIELDS.
11                ;
12                ;       DESCRIPTION             BITS
13                ;
14                ;       A INPUT                 0-3
15                ;       A REG                   4-7
16                ;       B REG                   8-11
17                ;       ALU                     12-15
18                ;       SHIFT                   16-19
19                ;       LOAD                    20
20                ;       CRY                     21-22
21                ;       MA                      23
22                ;       MBUS                    24-25
23                ;       RAND1                   26-28
24                ;       RAND2                   29-31
25                ;       STATE CHANGE            32-37
26                ;       PAGE                    38-39
27                ;       TRUE ADDR.              40-47
28                ;       FALSE ADDRS.            48-55
29                ;
30                ;
31                ;
32                ;
33                ;
34                ;
35                ;
36                ;8.0    MICRO-ORDERS
37                ;
38                ;
39                ;       THE VARIOUS MICRO-ORDERS IN EACH CONTROL FIELD ARE
40                ;       DESCRIBED HERE.
41                ;
42                ;
43                ;
44                ;
45                ;
46                ;       A INPUT FIELD OF ROM WORD
47
48        000000 .DUSR    AR=0    ;AREG<0-15> = A<0-15>
49        000001 .DUSR    IRD=1   ;IR<3-4> = A<14-15>,0'S = A<0-13>
50        000002 .DUSR    BIT=2   ;2(15-COUNT) = A<0-15>
51        000003 .DUSR    TRP=3   ;IR10 = A10,IR<5-9> = A<11-15>,0'S = A<0-9> (1)
52        000005 .DUSR    PL=5    ;PL ROM WORD ADDR. BY BREG<11-15> = A<0-15>
53        000010 .DUSR    LBY=10  ;AREG<8-15> = A<8-15>,0'S = A<0-7>
54        000011 .DUSR    IRS=11  ;IR<1-2> = A<14-15>,0'S = A<0-13>
55        000012 .DUSR    Z=12    ;0'S = A<0-15>
56        000013 .DUSR    CON=13  ;RBUF<40-47> = A<8-15>,0'S = A<0-7>
57        000014 .DUSR    SEX=14  ;AREG<8-15> = A<8-15>,IR8'S = A<0-7>
58        000016 .DUSR    CCN=16  ;RBUF<40-47> = A<8-15>,1'S = A<0-7>
59        000017 .DUSR    UBY=17  ;AREG<0-7> = A<0-7>,0'S = A<8-15>
60
```

```
0010 WCS
01                ;       A REG/B REG FIELD OF ROM WORD
02
03        000000 .DUSR    ACS=0   ;ACS
04        000001 .DUSR    AD1=1   ;SELECT AC=ACD+1
05        000002 .DUSR    ACD=2   ;ACD
06        000004 .DUSR    GRS=4   ;GR SPECIFIED BY IR BITS 1-2.
07        000005 .DUSR    GD1=5   ;GR SPECIFIED BY IR BITS 3-4,+1.
08        000006 .DUSR    GRD=6   ;GR SPECIFIED BY IR BITS 3-4.
09        000010 .DUSR    AC0=10  ;AC0
10        000011 .DUSR    AC1=11  ;AC1
11        000012 .DUSR    AC2=12  ;AC2
12        000013 .DUSR    AC3=13  ;AC3
13        000014 .DUSR    GR0=14  ;GR 0
14        000015 .DUSR    GR1=15  ;GR 1
15        000016 .DUSR    GR2=16  ;GR 2
16        000017 .DUSR    GR3=17  ;(PC) GR 3
17        000017 .DUSR    PC=17   ;(GR3)
18
19
20
21
22
23                ;       ALU FIELD OF ROM WORD (2)
24                ;
25                ;
26                ;CIN=CARRY IN
27                ;C=COMPLEMENT
28                ;
29                ;
30
31        000000 .DUSR    A=0     ;A+CIN
32        000001 .DUSR    APB=1   ;A+B+CIN
33        000002 .DUSR    A1=2    ;A+1
34        000003 .DUSR    APCB=3  ;A+CB+CIN
35        000004 .DUSR    AM1=4   ;A-1+CIN
36        000005 .DUSR    APA=5   ;A+A+CIN
37        000006 .DUSR    APA1=6  ;A+A+1
38        000007 .DUSR    APB1=7  ;A+B+1
39        000010 .DUSR    AMB=10  ;A-B
40        000011 .DUSR    CA=11   ;CA
41        000012 .DUSR    AOB=12  ;A OR B
42        000013 .DUSR    AXB=13  ;A XOR B
43        000014 .DUSR    ANB=14  ;A AND B
44        000015 .DUSR    ANCB=15 ;A AND CB
45        000016 .DUSR    CANB=16 ;CA AND B
46        000017 .DUSR    ANBC=17 ;(A AND B)C
47
48                ;       SHIFT FIELD OF ROM WORD (3)
49
50        000000 .DUSR    FO=0    ;STRAIGHT,0-SHIFT0
51        000001 .DUSR    FC=1    ;STRAIGHT,CARRY-SHIFT0
52        000002 .DUSR    FI=2    ;STRAIGHT,ION-SHIFT0
53        000003 .DUSR    FA=3    ;STRAIGHT,ALL 16 BITS
54        000004 .DUSR    L0=4    ;LEFT,0-SHIFT15
55        000005 .DUSR    LL=5    ;LEFT,LINK-SHIFT15
56        000006 .DUSR    LQ=6    ;LEFT,QBIT-SHIFT15
57        000007 .DUSR    LC=7    ;LEFT,CRY ENAB-SHIFT15
58        000010 .DUSR    RO=10   ;RIGHT,0-SHIFT0
59        000011 .DUSR    RL=11   ;RIGHT,LINK-SHIFT0
60        000012 .DUSR    RM=12   ;RIGHT,MULS CRY-SHIFT0
```

```
0011 WCS
01        000013 .DUSR    RC=13    ;RIGHT,CRY ENAB=SHIFT0
02        000014 .DUSR    SW=14    ;SWAP BYTES
03
04
05                ;       LOAD FIELD OF ROM WORD
06
07        000001 .DUSR    L=1      ;SHIFT<0-15> = AREG<0-15> (4)
08
09
10                ;       CARRY FIELD OF ROM  WORD
11
12        000000 .DUSR    N=0      ;NO EFFECT
13        000001 .DUSR    SET=1    ;1 = CARRY
14        000002 .DUSR    CLR=2    ;0 = CARRY
15        000003 .DUSR    ALC=3    ;ENABLE ALC LOGIC
16
17
18                ;       MA FIELD OF ROM WORD
19
20        000001 .DUSR    S=1      ;ALU<1-15> = LA<1-15>,START MEMORY (5)
21
22                ;       MBUS FIELD OF ROM WORD
23
24
25        000001 .DUSR    RMOD=1   ;READ,NO RELEASE (6)
26        000002 .DUSR    WRIT=2   ;WRITE AND RELEASE
27        000003 .DUSR    READ=3   ;READ AND RELEASE
28
29                ;       RAND1 FIELD OF ROM WORD
30
31
32        000001 .DUSR    DCH=1    ;ALLOW DATA CHANNEL BREAK
33        000002 .DUSR    SCND=2   ;(QBIT XOR ALU0 SAVE XOR CRY0)C = QBIT,
34                                 ;ALU0 = ALU0 SAVE (7)
35        000003 .DUSR    IOTR=3   ;IO TRANSFER (6)
36        000004 .DUSR    IOPS=4   ;I/O PULSE (6)
37        000006 .DUSR    CNDA=6   ;CONSOLE DATA SWITCHES = MEM<0-15>
38        000007 .DUSR    STIR=7   ;MEM<0-15> = IR<0-15> (7)(8)
39
40
41
42
43
44                ;       RAND2 FIELD OF ROM WORD
45
46        000001 .DUSR    BMEM=1   ;BREG<0-15> = MEM<0-15>
47        000002 .DUSR    DECL=2   ;CARRY = CIN;SHIFT<12-15> = AREG<12-15>
48        000003 .DUSR    LCNT=3   ;ALU<12-15> = COUNT<12-15>
49        000004 .DUSR    PFL=4    ;SYSRST IF PWR FF=1
50        000005 .DUSR    IOFF=5   ;0 = ION
51        000006 .DUSR    CNIN=6   ;CONSOLE FUNCTION CODE = MEM<1-4> (6)
52        000007 .DUSR    LPST=7   ;LOAD PROCESSOR STATE
53
54
55
56                ;       STATE CHANGE FIELD OF ROM  WORD (9)
57
58        000000 .DUSR    LDIR=0           ;PHANTOM;MEM=IR,17-COUNT,1=QBIT,
59                                         ;0=ALU0 SAVE,0 = ION PEND (6)(10)
60        000001 .DUSR    DEC1=1           ;DECODE 1
```

```
0012 WCS
01        000002 .DUSR    DEC2=2           ;DECODE 2
02        000005 .DUSR    JUMP=5           ;J
03        000007 .DUSR    NILDIR=7         ;PHANTOM;MEM=IR,17-COUNT,1=QBIT,
04                                         ;0=ALU0 SAVE,0=ION PEND (6)(15)
05        000010 .DUSR    ALU15=10         ;T IF ALU15=1,ELSE F
06        000011 .DUSR    ALU14=11         ;T  IF ALU14=1,ELSE F
07        000012 .DUSR    ALU12=12         ;T IF ALU12=1,ELSE FALSE
08        000013 .DUSR    ALU0=13          ;T IF ALU0=1,ELSE F
09        000014 .DUSR    CRY12B=14        ;F IF CRY12=1,ELSE T
10        000015 .DUSR    SCRY=15          ;T IF A0 XOR B0 XOR CRY0=1,ELSE F
11        000016 .DUSR    DCRY=16          ;T IF CRY12=1 OR ALU<12-15> >9,ELSE F
12        000017 .DUSR    CRY0B=17         ;F IF CRY0=1,ELSE T
13        000020 .DUSR    AUTIX=20         ;T IF 20 OCTAL < OR EQUAL ALU<1-15> OR
14                                         ;37 OCTAL < OR EQUAL,ELSE F
15        000021 .DUSR    IRSBD1=21        ;F IF IR5=1,ELSE DECODE 1
16        000022 .DUSR    A0BD1=22         ;F IF A0=1,ELSE DECODE1
17        000023 .DUSR    ACEQ1=23         ;F IF IR<1-2>=IR<3-4>,ELSE T;
18                                         ;INCREMENT IR<1-2> (14)
19        000024 .DUSR    ACEQD=24         ;F IF IR<1-2>=IR<3-4>,ELSE T;
20                                         ;DECREMENT IR<1-2> (14)
21        000025 .DUSR    CNTND=25         ;T IF COUNT NOT = 0,ELSE F;DEC. COUNT
22        000026 .DUSR    LINK=26          ;T IF LINK = 1,ELSE F
23        000027 .DUSR    NC=27            ;F
24        000030 .DUSR    INTR=30          ;T IF INTERRUPT WAITING,ELSE F
25        000031 .DUSR    IOSKPB=31        ;F IF I/O SKIP TEST TRUE,ELSE T
26        000032 .DUSR    CONRQ=32         ;T IF CONSOLE SWITCH PRESSED,ELSE F
27        000033 .DUSR    LOCKB=33         ;F IF POWER SWITCH IN LOCK POS.,ELSE T
28        000034 .DUSR    QBIT=34          ;T IF QBIT = 1,ELSE F
29        000035 .DUSR    CARRY=35         ;T IF CARRY = 1,ELSE F
30        000036 .DUSR    A0=36            ;T IF A0=1,ELSE F
31        000037 .DUSR    ALUZ=37          ;T IF ALU<0-15> = 0,ELSE F
32        000050 .DUSR    LEAP0=50         ;LEAP 0
33        000051 .DUSR    LEAP1=51         ;LEAP 1
34        000052 .DUSR    LEAP2=52         ;LEAP 2
35        000053 .DUSR    LEAP3=53         ;LEAP 3
36        000004 .DUSR    WCABUS=4         ;WCS ADDRESS
37        000055 .DUSR    WCSBUS=55        ;WCS DATA
38        000056 .DUSR    BUSMD=56         ;MD TO BUS
39        000057 .DUSR    BUSMQ=57         ;MQ TO BUS
40        000060 .DUSR    MDPAD=60         ;PAD TO MD
41        000061 .DUSR    MDBUS=61         ;BUS TO MD
42        000062 .DUSR    MQPAD=62         ;PAD TO MQ
43        000063 .DUSR    MQBUS=63         ;BUS TO MQ
44        000064 .DUSR    PDVPAD=64        ;POST DIVIDE
45        000065 .DUSR    DIVPAD=65        ;DIVIDE
46        000066 .DUSR    MULPAD=66        ;MULTIPLY
47        000067 .DUSR    PADBUS=67        ;BUS TO PAD
48        000070 .DUSR    JMPER1=70        ;JUMPER 1 TEST
49        000071 .DUSR    JMPER2=71        ;JUMPER 2 TEST
50        000072 .DUSR    BUSPAD=72        ;PAD TO BUS
51        000073 .DUSR    SLEAP=73         ;SECTOR LEAP
52        000074 .DUSR    HOP=74           ;HOP
53        000075 .DUSR    MARBUS=75        ;BUS TO MAR
54        000076 .DUSR    MARPAD=76        ;PAD TO MAR
55                ;
56                ;
57                ;
58                ;       NOTES PERTAINING TO MICRO-ORDERS ABOVE.
59                ;
60                ;       1.COUNT MUST BE > 7
```

```
 0013 WCS
01                ;       2.CIN=(DECL AND CARRY)OR(ALC AND IR7)
02                ;       3.LINK MODIFIED BY LEFT AND RIGHT SHIFTS
03                ;       4.UNLESS ALC WITH IR12=1
04                ;       5.ALLOWS DCH BREAK UNLESS STIR OR SCND
05                ;       6.DO NOT ALLOW DCH BREAK
06                ;       7.DISABLE DCH BREAK
07                ;       8.DO NOT CODE WITH ACEN1 OR ACEQD
08                ;       9.FALSE ADDRESS IS IN CURRENT PAGE,TRUE ADDRESS
09                ;         MAY CHANGE CURRENT PAGE
10                ;       10.INHIBITED BY HALT/STOP(IF RBUF55=0),INTERRUPT WAITING,
11                ;          OR REXAM
12                ;       13.INHIBITED BY HALT/STOP (IF RBUF55=0)
13                ;          OR REXAM
14                ;       14.DO NOT CODE WITH STIR
15                ;
16                ;       FOR A COMPLETE DESCRIPTION OF THE MICRO-ORDERS,
17                ;       PLEASE CONSULT THE DATA GENERAL
18                ;       USERS MANUAL "S-130 MICROPROGRAMMING WCS FEATURE"
19                ;       015-69-00
20                ;
21                ;
22
```

```
 0014 WCS
01                ;
02                ;
03                ;
04                ;9.0    I-O TESTER DESCRIPTION
05                ;
06                ;
07                ;       9.1 TEST BOARD COMMANDS
08                ;
09                ;       IORST  - CLEAR THE TESTER
10                ;       NIOC 0 - CLEAR THE TESTER(NEW MODE)
11                ;       INTA   - READ THE DATA BUFFER (NOT NEW MODE)
12                ;       DIC    - READ THE PULSE DETECTORS
13                ;       DIB    - READ THE DATA BUFFER
14                ;       DIA    - READ THE DCH ADDRESS BUFFER (NEW MODE)
15                ;       DOA    - LOAD THE DATA BUFFER
16                ;       DOB    - LOAD THE FUNCTION BUFFER
17                ;       DOC    - LOAD THE DATA AND DCH ADDRESS BUFFERS
18                ;
19                ;
20                ;       9.2 FUNCTION REGISTER BIT ASSIGNMENTS
21                ;
22                ;       BIT 0           SET DCH SYNC
23                ;       BIT 1           SET DCH MODE0
24                ;       BIT 2           SET DCH MODE1
25                ;       BIT 3           SET PI SYNC
26                ;       BIT 4           BUSY (IF NOT NEW MODE)
27                ;       BIT 5           DONE (IF NOT NEW MODE)
28                ;       BIT 6           NEW MODE
29                ;       BITS 7-9        THE # OF RQENB PULSES BETWEEN
30                ;                       SUCCESSIVE DCH CYCLES.
31                ;       BITS 10-15      # OF DCH CYCLES
32                ;
33                ;
34                ;       9.3 PULSE DETECTOR BIT ASSIGNMENTS
35                ;
36                ;
37                ;       BIT 0   IOPLS
38                ;       BIT 1   INTA (INTA + DCHP)
39                ;       BIT 2   MSKO
40                ;       BIT 3   DCH1
41                ;       BIT 4   OVFLO-NOT USED ON ECLIPSE
42                ;       BIT 5   DCH0
43                ;       BIT 6   DCHA
44                ;       BIT 7   RQENB
45                ;       BIT 8   DOA
46                ;       BIT 9   DOB
47                ;       BIT 10  DOC
48                ;       BIT 11  DIA
49                ;       BIT 12  DIB
50                ;       BIT 13  DIC (NOT SET IF DEV. CODE=0)
51                ;       BIT 14  STRI
52                ;       BIT 15  CLR
53                ;
54                ;
55                ;
56                ;       PLEASE NOTE THAT DCH PRIORITY MUST BE WIRED
57                ;       TO THE SLOT IN WHICH THE I-O TESTER IS RESIDENT.
58                ;       FAILURE TO DO THIS WILL CAUSE ERRORS WITH ANY
59                ;       TESTS WHICH ARE TESTING THE INTA PULSE DETECTOR
60                ;       AND/OR DATA CHANNEL.
```

```
0015 WCS
01              ;
02              ;
03              ;
04              ;
05              ;
06              ;
07              ;10.0   SOFTWARE DEBUGGING AIDS
08              ;
09              ;       DUE TO THE DIFFICULTY IN DYNAMICALLY CHECKING
10              ;       THE OUTPUTS OF THE RAMS,A SERIES OF SHORT
11              ;       DEBUGGING ROUTINES HAVE BEEN INCLUDED AT THE
12              ;       END OF THE TEST PROGRAM STARTING AT THE
13              ;       LOCATION TAGGED "AIDS".THESE ROUTINES MAY BE
14              ;       USED ALONG WITH THE MICRO-INSTRUCT
15              ;       CAPABILITY TO STATICALLY CHECK THE OUTPUT
16              ;       OF ANY RAM.
17              ;
18              ;
19              ;11.0   RUNNING WITH CAT/KITTEN
20              ;
21              ;       THE PROGRAM MAY BE EXECUTED WITH THE CAT/KITTEN IN THE
22              ;       BACKGROUND VIA PRECEEDING THE EDTOS COMMAND WITH THE
23              ;       LETTER "C",SUCH AS "CLOAD".
24              ;
25              ;       THE DEVICE CODE FOR WCS MAY BE ADDED TO THE EDTOS
26              ;       EQUIPMENT TABLE VIA AN  "ADD  -,1"  COMMAND.
27              ;
28              ;
29              ;
30              ;       IF THE CAT/KITTEN IS SELECTED,THE FIRST PASS WILL BE A
31              ;       NORMAL RUN,AND SUBSEQUENT PASSES WILL BE WITH THE
32              ;       CAT/KITTEN IN THE BACKGROUND.
33              ;
34              ;       IF AN ERROR OCCURS AFTER THE FIRST PASS,THE NORMAL
35              ;       ERROR INFORMATION WILL BE PRINTED,BUT NO HALT WILL
36              ;       OCCUR.THE PROGRAM WILL CONTINUE TESTING AS DIRECTED
37              ;       BY THE SETTING OF THE SWITCHES.
38              ;
39              ;       IF RESTART IS REQUIRED USE THE FOLLOWING
40              ;       SPECIAL RESTART LOCATIONS:
41              ;
42              ;       170     START WITHOUT CAT/KITTEN
43              ;       171     START WITH CAT/KITTEN
44              ;
45              ;       IN ALL CASES, A CAT/KITTEN RUN SHOULD NOT BE ATTEMPTED
46              ;       UNTIL THE PROGRAM EXECUTES SUCCESSFULLY IN
47              ;       NORMAL MODE.
48              ;
49              ;       WHEN RUNNING WITH THE  CAT/KITTEN , THE PROGRAM WILL
50              ;       PRINT IT'S NORMAL PASS MESSAGE AND THE
51              ;       CAT/KITTEN WILL PRINT THE LETTER "P" AS IT'S
52              ;       PASS MESSAGE.
53              ;
54              ;
55              ;       PLEASE NOTE THAT CERTAIN TESTS CANNOT BE EXECUTED WITH
56              ;       THE CAT/KITTEN SO THAT THESE TESTS WOULD BE EXECUTED
57              ;       DURING THE FIRST PASS AND BYPASSED DURING THE SECOND
58              ;       AND SUBSEQUENT PASSES.
59              ;
```

```
0016 WCS
01              ;
02              ;12.0   PROGRAM TEST SEQUENCE
03              ;
04              ;       THE PROGRAM TEST SEQUENCE IS AS FOLLOWS.
05              ;
06              ;       A-INPUT FIELD
07              ;       ALU FIELD
08              ;
09              ;
```

10017 WCS

**00000 TOTAL ERRORS, 00000 PASS 1 ERRORS