DataGeneral

TECHNICAL STATEMENT

TEXT LISTING

068-000268-03

PROGRAM

ECLIPSE MAP DIAGNOSTIC, PART A

TEXT TAPE

097-000268-03

ABSTRACT

THIS IS THE FIRST OF 2 PROGRAMS (EMAPA,EMAPB) DESIGNED TO VERIFY THE OPERATION OF THE MEMORY ALLOCATION AND PROTECTION (MAP) FEATURE.

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 0001 EMAPA     MACRO REV 06.30.          14:31:36 02/14/79
01
02
03
04
05
06              ;*************************************************************
07              ;
08              ; NAME: EMAPA.TX                          PART NUMBER: 097-000268
09              ;
10              ; DESCRIPTION: ECLIPSE MAP DIAGNOSTIC, PART A
11              ;
12              ; REVISION HISTORY:
13              ;
14              ;       REV.            DATE
15              ;
16              ;       00              04/11/75
17              ;       01              11/07/75
18              ;       02              08/06/76
19              ;       03              12/31/76
20              ;
21              ; COPYRIGHT (C) DATA GENERAL COPERATION, 1975, 1976
22              ; ALL RIGHT RESERVED.
23              ;*************************************************************
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!0002 EMAPA
01
                        .TITLE EMAPA
03              ;
04              ; ECLIPSE MEMORY PROTECTION AND MANAGMENT TEST
05              ;               PART 1
06                      .EJECT
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0003 EMAPA
01              ;EMAPA
02              ;MAP DIAGNOSTIC- 1 OF 2
03              ;
04              ;THIS DIAGNOSTIC IS DESIGNED TO RUN IN AN
05              ;AUTO-LOAD AUTO-RUN ENVIRONMENT.
06              ;
07              ;1.0    ABSTRACT
08              ;               THIS IS THE FIRST OF 2 PROGRAMS (EMAPA,EMAPB)
09              ;               DESINGED TO VERIFY THE OPERATION OF THE
10              ;               MEMORY ALLOCATION AND PROTECTION (MAP) FEATURE.
11              ;               THIS PROGRAM VERIFIES THE OPERATION OF MMPU.
12              ;               THE FIRST PROGRAM IS A PREREQUSITE TO THE
13              ;               SECOND AND THEY ARE BOTH PREREQUSITES TO THE
14              ;               MULTIPROGRAMMING RELIABILITY TEST PROGRAM.
15              ;
16              ;
17              ;2.0    MACHINE REQUIREMENTS
18              ;       2.1     ECLIPSE PROCESSOR WITH MAP OPTION.
19              ;       2.2     8K OF READ/WRITE MEMORY.
20              ;       2.3     TTY
21              ;       2.4     RTC (OPTIONAL)
22              ;       2.5     I/O TESTER (OPTIONAL)
23              ;
24              ;
25
26              ;3.0    OPERATING PROCEDURE
27              ;       3.1     LOADING
28              ;               LOAD PROGRAM VIA THE BINARY LOADER.
29              ;       3.2     START ADDRESS
30              ;               SET SWITCHES TO 200 OCTAL.
31              ;               PRESS START.
32              ;               THE PROGRAM STARTS BY PRINTING OUT THE
33              ;               PROGRAM NAME AND REVISION NUMBER.  IF MAP
34              ;               FEATURE MMPU DOES NOT EXIST AND THE PROGRAM
35              ;               IS RUN IN AUTO MODE IT PRINTS A MESSAGE AND
36              ;               EXITS TO DTOS. IT THEN INFORMS THE OPERATOR OF THE
37              ;               EXISTENCE I/O TESTER.THIS IS FOLLOWED BY THE
38              ;               PHY NUMBER  OF 1K MEMORY BLOCKS IN THE SYSTEM.
39              ;               IT IS QUITE POSSIBLE THAT IF THERE IS A
40              ;               FAILURE IN THE SYSTEM, THIS NUMBER WILL
41              ;               BE INCORRECT.
42              ;
43              ;       3.3     SWITCH SETTINGS
44              ;               SWITCH 0 (0) = USE CONTENTS OF "SWREG"
45              ;               SWITCH 0 (1) = USE DATA SWITCHES
46              ;               SWITCH 1 (1) = PROCEED FROM ERROR
47              ;               SWITCH 2 (1) = INHIBIT PRINTOUT TO TTO
48              ;               SWITCH 3 (1) = PRINT FAILURE RATE
49              ;               SWITCH 4 (1) = INHIBIT PRINTING OF PASS COUNT
50              ;               SWITCH 5 (1) = ENABLE PRINTOUT TO LPT
51              ;
52              ;               PLEASE NOTE THAT THE SELECTION TO USE THE DATA
53              ;               SWITCHES OR THE CONTENTS OF "SWREG" MAY BE
54              ;               MADE ONLY AT THE BEGINNING OF THE PROGRAM
55              ;               OR FOLLOWING AN ERROR HALT.
56              ;
57              ;       3.4     NORMAL OPERATION
58              ;               PROGRAM WILL EXECUTE ALL TESTS IN SEQUENCE
59              ;               AND AUTOMATICALLY LOOP.  IF SWITCH 4 IS CLEAR,
60              ;               A MESSAGE "PASS"  WILL BE PRINTED AT THE
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0004 EMAPA
01              ;               END OF EACH PASS  ALONG WITH THE
02              ;               PASS COUNT IN DECIMAL.  IF SWITCH 4 IS SET,
03              ;               THE PASS COUNT WILL BE ACCUMULATED, BUT NOT
04              ;               PRINTED.
05              ;
06              ;               IF AN I/O TESTER OR AN RTC IS NOT IN THE SYSTEM,
07              ;               THE TTY WILL ECHO RUBOUT CODES AT VARIOUS TIMES
08              ;               IN THE PROGRAM.  THIS IS NECESSARY TO PRODUCE
09              ;               INTERRUPTS.
10              ;
11
```

```
01
02              ;
03              ;4.0    ERROR DESCRIPTION
04              ;       4.1     NORMAL
05              ;               UPON THE DETECTION OF AN ERROR, THE PROGRAM
06              ;               WILL PRINT THE C/PC AND AC'S AND THEN LOOP.
07              ;               CONSULT THE LISTING FOR A TEST DESCRIPTION.
08              ;               SET THE SWITCHES TO CONTINUE.
09              ;
10              ;       4.2     ABNORMAL
11              ;               THERE ARE SEVERAL TYPES OF UNEXPECTED FAILURES
12              ;               WHICH WILL CAUSE A PROGRAM HALT.  THEY ARE AS
13              ;               FOLLOWS:
14              ;                       UNEXPECTED INTERRUPT
15              ;                       STACK OVERFLOW OR UNDERFLOW
16              ;               THE CAUSE OF ANY OF THESE FAILURES SHOULD BE
17              ;               CORRECTED BEFORE RESUMING TESTING.
18              ;
19              ;       4.3     MAP DATA
20              ;               THE CONTENTS OF THE USER AND DCH MAPS
21              ;               MAY BE PRINTED ON THE TTY/CRT FOR
22              ;               VISUAL ANALYSIS BY SETTING THE
23              ;               SWITCHES TO 206 OCTAL AND PRESSING START.
24              ;;
25              ;5.0    PROGRAM DESCRIPTION
26              ;       5.1     COMMON SUBROUTINE CALLS
27              ;               THE DIAGNOSTIC IS COMPRISED OF A SERIES OF
28              ;               SHORT TESTS.  BASICALLY, EACH TEST CONSISTS
29              ;               OF A SETUP PROCEDURE, ONE OR MORE EVALUATING
30              ;               CASES WITH ERROR CALLS, AND A LOOP CAPABILITY.
31              ;               EACH PARTICULAR TEST CASE IS DESCRIBED IN THE
32              ;               LISTING.  THE COMMON ROUTINES FOR SETUP (SETUP),
33              ;               ERROR CALLS (EHALT), AND LOOP (LOOP) ARE
34              ;               DESCRIBED HERE,ALONG WITH OTHER
35              ;               COMMONLY CALLED ROUTINES.
36              ;
37              ;               SETUP
38              ;               EACH TEST BEGINS WITH A CALL TO SETUP.  THIS
39              ;               ROUTINE ISSUES AN IORST, SETS UP THE LOOP ADDRESS,
40              ;               RESETS CERTAIN ERROR SWITCHES AND ITERATION
41              ;               COUNTS.  IT ALSO STORES AN ADDRESS OF 60 INTO
42              ;               LOCATIONS 0,1,2,3 AND 45.  LOC 60 IS SET AS A
43              ;               JMP INDIRECT TO LOC 61.  LOC 61 CONTAINS AN
44              ;               ADDRESS WITHIN THE TEST WHICH POINTS TO SETUP+1.
45              ;               THE USER STACK AND VECTOR STACKS ARE ALSO
46              ;               INITIALIZED.
47              ;
48              ;               EHALT
49              ;               THIS ROUTINE IS CALLED WHEN AN ERROR IS
50              ;               DETECTED.  SUMETIMES AN ERROR MIGHT OCCUR
51              ;               WITH USER MODE ENABLED.  FOR THIS REASON,
52              ;               UPON ENTRY INTO EHALT, AN SCL IS EXECUTED
53              ;               TO REMOVE USER MODE.  THE ROUTINE WILL THEN
54              ;               PROCEED TO HALT.  THIS ROUTINE WILL ALSO
55              ;               INTERROGATE ERROR SWITCHES AND PRINT ERROR DATA.
56              ;
57              ;              LOOP
58              ;               THIS ROUTINE IS CALLED AT THE END OF EACH TEST
59              ;               SEQUENCE.  IT IS USED TO ITERATE THE SEQUENCE
60              ;               100 TIMES IF NO ERROR HAS BEEN DETECTED.
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01              ;               IF AN ERROR HAS BEEN DETECTED, IT IS USED TO
02              ;               MAINTAIN THE SCOPE LOOP AND INTERROGATE THE
03              ;               SWITCHES, ETC.  THE USER STACK AND VECTOR STACK
04              ;               ARE ALSO INITIALIZED.
05              ;
06              ;
07              ;               LEPAB
08              ;               MAP ALL OF MEMORY TO
09              ;               LOGICAL = PHYSICAL
10              ;
11              ;               SULMP
12              ;               SET UP THE AC'S FOR A LMP INSTRUCTION
13              ;               AS PER THE WORDS FOLLOWING THE CALL.
14              ;               WORD 1 = AC0    WORD 2 = AC1
15              ;               WORD 3 = AC2    WORD 4 = AC3
16              ;
17              ;               SETDONE
18              ;               THE DONE FLOP IS SET IN ONE OF
19              ;               THE FOLLOWING DEVICES:
20              ;               RTC, I/O TESTER OR TTY/CRT.
21              ;
22              ;               SUMAP
23              ;               A BLOCK OF MEMORY IS SET UP TO  ) A BLOCK
24              ;               LOAD OF THE MAP VIA A LMP.  TH  CALL
25              ;               IS FOLLOWED BY 3 PAIRS OF TWO  ORDS.  THE
26              ;               FIRST WORD IN EACH PAIR IDENT  IES WHICH
27              ;               MAP:
28              ;               400 = DCH, 1000 = USER A, 1400 = USER B
29              ;               THE SECOND WORD IN EACH PAIR DENOTES
30              ;               HOW THAT MAP IS TO BE LOADED:
31              ;               0 = 0'S, 1 = 1'S, 2 = ADDRESS
32              ;
33              ;               RCBLK
34              ;               THIS ROUTINE IS USED FOLLOWING A BLOCK
35              ;               LOAD OF THE MAP BY A LMP TO READ
36              ;               BACK AND CHECK THE LOADED MAPS.
37              ;               AS DESCRIBED ABOVE FOR THE "SUMAP" ROUTINE,
38              ;               THE CALL IS FOLLOWED BY A USER SELECTION
39              ;               WORD AND A LOAD SPECIFIER.
40              ;
41              ;               SUIOMAP
42              ;               A BLOCK OF MEMORY IS SET UP FOR
43              ;               A LMP TO PERFORM A BLOCK LOAD
44              ;               OF DEVICE PROTECTION.  THE CALL IS
45              ;               FOLLOWED BY 2 FIVE WORD BLOCKS.
46              ;               THE FIRST WORD OF EACH 5 WORD BLOCK
47              ;               SPECIFIES THE USER: 0 = USER A, 20000 = USER B.
48              ;               THE NEXT 4 WORDS IN EACH BLOCK SPECIFY
49              ;               THE DEVICE PROTECTION WHICH IS TO BE
50              ;               LOADED FOR THE SELECTED USER.
51              ;
52              ;
53              ;               IOCHK
54              ;               THIS ROUTINE IS USED FOLLOWING A
55              ;               BLOCK LOAD OF DEVICE PROTECTION IN
56              ;               THE MAP VIA LMP.  IT CREATES
57              ;               A 4 WORD BY 16 BIT MATRIX OF
58              ;               THE DEVICE PROTECTION IN THE MAP
59              ;               AND COMPARES THIS TO THE MATRIX
60              ;               OF THE ORIGINAL LOADED DEVICE PROTECTION
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                ;               WHICH HAS BEEN PREVIOUSLY SAVED.
                ;               THE CALL IS FOLLOWED BY A ONE
                ;               WORD USER IDENTIFICATION SPECIFIER:
                ;               0 = USER A, 20000 = USER B.
                ;
                ;               TRAN
                ;               IF NO ERROR EXISTS, A NEW
                ;               RANDOM # IS RETURNED IN AC0.
                ;               IF AN ERROR EXISTS, THE OLD
                ;               # IS RE-CIRCULATED.
                ;
                ;               SPA1
                ;               SET ALL DEVICE PROTECTION BITS
                ;               FOR USER A = 1.
                ;
                ;               SPA0
                ;               SET ALL DEVICE PROTECTION BITS
                ;               FOR USER A = 0.
                ;
                ;               SPB1
                ;               SET ALL DEVICE PROTECTION BITS
                ;               FOR USER B = 1.
                ;
                ;               SPB0
                ;               SET ALL DEVICE PROTECTION BITS
                ;               FOR USER B = 0.
                ;
                ;               IOMAP
                ;               THE DEVICE PROTECTION MAP FOR A
                ;               SELECTED USER IS SET AS SPECIFIED
                ;               BY THE 5 WORD INFORMATION BLOCK
                ;               FOLLOWING THE CALL.
                ;               WORD 1 = USER, 0 = USER A, 20000 = USER B.
                ;               THE NEXT 4 WORDS SPECIFY THE CONTENTS
                ;               OF THE DEVICE PROTECTION MAP FOR THAT USER.
                ;
```



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                ;       5.2     MONITOR LOCATIONS
                ;
                ;               LOC 200         USED BY DTOS
                ;               LOC 201         CURRENT TEST ADDRESS LOCATION
                ;               LOC 202         STARTING ADDRESS FOR  PROGRAM
                ;               LOC 203         PROGRAM PASS COUNT
                ;               LOC 204         TEST ITERATION COUNT
                ;
                ;
                ;
                ;       5.3     MEMORY MAP
                ;
                ;               UNLESS OTHERWISE MENTIONED IN THE
                ;               SPECIFIC TEST,MEMORY FOR USERS A
                ;               AND B IS ALWAYS MAPPED TO ITSELF.
                ;               THAT IS LOGICAL=PHYSICAL.
                ;
                ;
                ;6.0    SEQUENCE OF TESTING
                ;
                ;               THE TESTING SEQUENCE FOR PROGRAM
                ;               MAPA IS AS FOLLOWS:
                ;
                ;               BASIC LOADING AND READING BACK OF
                ;               USER A, USER B, AND DCH MAPS.
                ;
                ;               SINGLE REFERENCE
                ;
                ;               USER SELECTION
                ;
                ;               USER ENABLE
                ;
                ;               DEFER PROTECT
                ;
                ;               VALIDITY PROTECT
                ;
                ;               WRITE PROTECT
                ;
                ;               DEVICE PROTECT
                ;
                ;               PROT. FAULT RESETS USER MODE
                ;
                ;               INTERRUPT
                ;
                ;               USER ENABLE VIA SPECIAL INSTRUCTIONS
                ;
                ;               USER ENABLE VIA @ BIT
                ;
                ;               SUPERVISOR BLOCK
                ;
                ;               PHYSICAL BLOCK 128
                ;
                ;
                ;
                ;
                ;
                ;7.0    PROGRAMMING DESCRIPTION FOR MAP FEATURE
                ;
                ;               THE INSTRUCTIONS WHICH MAY BE
                ;               USED TO SETUP AND INTERROGATE
```

0009 EMAPA

THE MAP FEATURE ARE BRIEFLY
DESCRIBED HERE.

7.1 DOA INSTRUCTION

THE DOA INSTRUCTION WITH THE FOLLOWING
FORMAT WILL DEFINE THE MAP FOR A
SINGLE 1K WORD BLOCK OF LOGICAL MEMORY.

BIT	CONTENTS
0	UNUSED
1-5	LOGICAL BLOCK NUMBER
6-7	MAP TYPE 01=DATA CHANNEL 10=USER A 11=USER B
8	WRITE PROTECT
9-15	PHYSICAL BLOCK NUMBER

THE DOA INSTRUCTION WITH THE FOLLOWING
FORMAT WILL DEFINE THE I/O DEVICES
WHICH ARE INACCESSIBLE TO THE USER.

BIT	CONTENTS
0	UNUSED
1	MUST BE 1
2	USER SELECTION 0=A, 1=B
3-5	DEVICE CLASS
6-7	MUST BE 00
8-15	DEVICE PROTECT BITS

10010 EMAPA

THE DOA INSTRUCTION WITH THE FOLLOWING
FORMAT DEFINES THE PROTECTION FEATURES
THAT ARE TO BE ENABLED FOR A USER.

BIT	CONTENTS
0	UNUSED
1	MUST BE 0
2	USER SELECTION 0=A, 1=B
3-5	UNUSED
6-7	MUST BE 00
8	UNUSED
9	LEF MODE
10	I/O PROTECT
11	WRITE PROTECT
12	INDIRECT PROTECT
13	DATA CHANNEL PROTECT
14	DATA CHANNEL MAP ENABLE
15	USER MAP ENABLE

7.2 DOB INSTRUCTION

THE DOB INSTRUCTION MAY BE USED
TO MAP SUPERVISOR BLOCK 31. BITS 9-15
OF THE SPECIFIED AC DENOTE A
PHYSICAL BLOCK NUMBER TO WHICH
LOGICAL 31 WILL BE MAPPED WHEN
IN THE SUPERVISOR MODE.

7.3 DIA INSTRUCTION

THE DIA INSTRUCTION MAY BE USED
TO READ INTO THE SPECIFIED AC
THE STATUS OF THE LAST ENABLED USER.

BIT	CONTENTS
0-1	UNUSED
2	USER 0=A, 1=B
3-8	UNUSED
9	LEF
10	IO PROTECT
11	WRITE PROTECT
12	INDIRECT PROTECT
13	DATA CHANNEL PROTECT
14	DATA CHANNEL MAP ENABLE
15	USER MODE INTERRUPT

7.4 DIC INSTRUCTION

THE DIC INSTRUCTION MAY BE USED
TO READ INTO THE SPECIFIED AC THE
CONTENTS OF THE MAP STATUS REGISTER.

BIT CONTENTS

```
;
;                       0       DATA CHANNEL PROTECT ERROR
;                       1       ERROR  DURING MAP SINGLE CYCLE
;                       2       WRITE PROTECT ERROR
;                       3       VALIDITY PROTECT ERROR
;                       4       INDIRECT PROTECT ERROR
;                       5       I/O PROTECTION ERROR
;                       6       USER LAST ENABLED, 0=A, 1=B
;                       7       PC ON  STACK IS UNDEFINED
;                       8       WRITE PROTECT
;                       9-15    PHYSICAL BLOCK # CORRESPONDING
;                               TO THE LOGICAL
;                               PAGE NUBER GIVEN IN
;                               LAST TRANSLATE BLOCK INSTRUCTION.
;
;
;
;               7.5     DOC INSTRUCTION
;
;                       THE DOC INSTRUCTION MAY BE USED TO
;                       TRANSLATE A LOGICAL BLOCK NUMBER TO
;                       ITS CORRESPONDING PHYSICAL BLOCK NUMBER.
;                       THE RESULT IS PLACED IN BITS 9-15 OF
;                       THE MAP STATUS REGISTER.
;
;                       BIT     CONTENTS
;
;                       0       UNUSED
;                       1-5     LOGICAL BLOCK NUMBER TO
;                               BE TRANSLATED
;                       6-7     00=NO TRANSLATION
;                               01=DCH MAP
;                               10=USER A
;                               11=USER B
;
;               7.6     MAP SINGLE CYCLE
;
;                       AN IO PULSE ISSUED TO THE MAP
;                       ALLOWS THE LAST USER MAP ENABLED
;                       TO BE MAPPED FOR ONE MEMORY REFERENCE.
;                       THE FIRST MEMORY REFERENCE AFTER
;                       THE NEXT LOAD OR STORE INSTRUCTION
;                       IS MAPPED.  AFTER THE MEMORY CYCLE
;                       IS MAPPED, THE USER MAP IS AGAIN
;                       DISABLED.
;
;
;
;
```



```
;
;               7.7     LEF INSTRUCTION
;
;                       IF THE LEF MODE BIT IN THE USER STATUS
;                       IS 1 FOR A USER, THEN ALL I/O
;                       INSTRUCTIONS ISSUED BY THAT USER
;                       WILL BE INTERPRETED AS LEF INSTRUCTIONS.
;                       THE LOGICAL EFFECTIVE ADDRESS IS
;                       COMPUTED FROM BITS 5-15 OF
;                       THE INSTRUCTION AND PLACED IN THE
;                       SPECIFIED AC.
;
;               7.8     LMP
;
;                       A BLOCK ADD AND MOVE  IS PERFORMED.
;                       THE RESULT IS LOADED INTO THE MAP
;                       FEATURE.  THE ACCUMULATORS ARE SET UP
;                       IN THE SAME MANNER AS THE BAM
;                       INSTRUCTION.  THE ONLY EXCEPTION IS THAT
;                       DATA IS NOT TRANSFERED TO THE
;                       DESTINATION ADDRESS AND AC3 IS
;                       UNUSED.
;
;                       ACCUMULATORS
;
;                       AC0 = ADDEND
;                       AC1 = NUMBER OF WORDS TO BE MOVED
;                       AC2 = SOURCE ADDRESS
;                       AC3 = DESTINATION ADDRESS (UNUSED)
;
;                       THE INFORMATION TO BE LOADED INTO
;                       THE MAP IS IN THREE FORMATS
;                       AS DESCRIBED IN SECTION 7.1,
;                       FOR THE DOA INSTRUCTION.
;
;
;
;
;8.0    I/O TESTER HARDWARE DESCRIPTION
;
;       8.1     TEST BOARD COMMANDS
;
;               IORST  =  CLEAR THE TESTER
;               NIOC 0 =  CLEAR THE TESTER (IF  NEW MODE)
;               INTA   =  READ THE DATA BUFFER (NOT NEW MODE)
;               DATIC  =  READ THE PULSE DETECTORS
;               DATIB  =  READ THE DATA BUFFER
;               DATIA  =  READ THE DCH ADDRESS BUFFER (NEW MODE)
;               DATOA  =  LOAD THE DATA BUFFER
;               DATOB  =  LOAD THE FUNCTION BUFFER
;               DATOC  =  LOAD THE DATA AND DCH ADDRESS BUFFERS
;
;       8.2     FUNCTION REGISTER BIT ASSIGNMENTS
;
;               BIT 0     SET DCH SYNC
;               BIT 1     SET DCH MODE0
;               BIT 2     SET DCH MODE1
;               BIT 3     SET PI SYNC
;               BIT 4     BUSY (IF NOT IN NEW MODE)
;               BIT 5     DONE (IF NOT IN NEW MODE)
```

```
 0013 EMAPA
01                ;               BIT 6     NEW MODE
02                ;               BITS 7-9  AN OCTAL # WHICH SPECIFIES THE
03                ;                         # OF RQENB PULSES BETWEEN
04                ;                         SUCCESSIVE DCH CYCLES. (NEW MODE ONLY)
05                ;                         NOTE THAT 0 SPECIFIES 1 RQENB PULSE.
06                ;               BITS 10-15  # OF DCH CYCLES TO BE RUN.
07                ;                         (NEW MODE ONLY)
08                ;                         NOTE THAT 0 SPECIFIES 1 DCH CYCLE.
09                ;
10                ;
11                ;
12                ;       8.3     PULSE DETECTOR BIT ASSIGNMENTS
13                ;
14                ;               BIT 0     IOPLS
15                ;               BIT 1     INTA (INTA AND DCHP)
16                ;               BIT 2     MSKO
17                ;               BIT 3     DCHI
18                ;               BIT 4     OVFLO
19                ;               BIT 5     DCHO
20                ;               BIT 6     DCHA
21                ;               BIT 7     RQENB (COMPLEMENTS WITH EACH PULSE)
22                ;               BIT 8     DATOA
23                ;               BIT 9     DATOB
24                ;               BIT 10    DATOC
25                ;               BIT 11    DATIA
26                ;               BIT 12    DATIB
27                ;               BIT 13    DATIC (NOT SET IF DEV CODE = 0)
28                ;               BIT 14    STRT
29                ;               BIT 15    CLR
30                ;
31                ;       8.4     TEST BOARD LOGIC
32                ;
33                ;               THE TEST BOARD CONTAINS 16 PULSE
34                ;               DETECTOR FLIP FLOPS.  THESE FF'S MAY
35                ;               BE READ BY A "DIC" WITH A DEVICE
36                ;               CODE OF 0.  THEY MAY BE CLEARED BY
37                ;               IORST OR NIOC 0 (IF IN NEW MODE).
38                ;               A PARTICULAR FF SETS WHENEVER
39                ;               A PULSE OCCURS ON THE LINE TO
40                ;               WHICH IT IS CONNECTED.
41                ;
42                ;               THE TEST BOARD ALSO CONTAINS
43                ;               A 16 BIT DATA BUFFER.  THIS
44                ;               BUFFER MAY BE LOADED/READ ETC.
45                ;               UNDER PROGRAM CONTROL.  THIS
46                ;               BUFFER IS ALSO USED FOR DCH
47                ;               OPERATIONS.  IT SHOULD BE NOTED THAT
48                ;               IN NEW MODE, ANY LOAD DATA BUFFER
49                ;               PROCEDURE, ACTUALLY LOADS THE
50                ;               EXCLUSIVE OR OF THE OUTPUT DATA
51                ;               AND THE DATA PREVIOUSLY STORED IN THE BUFFER.
52                ;
53                ;
54                ;               A 15 BIT DCH ADDRESS BUFFER
55                ;               IS USED TO DIRECT DCH REQUESTS
56                ;               TO ANY LOCATION IN/OUT OF MEMORY.
57                ;
58                ;
```

```
!0014 EMAPA
01
02                ;
03                ;       8.3     PULSE DETECTOR BIT ASSIGNMENTS
04                ;
05                ;               BIT 0     IOPLS
06                ;               BIT 1     INTA (INTA AND DCHP)
07                ;               BIT 2     MSKO
08                ;               BIT 3     DCHI
09                ;               BIT 4     OVFLO
10                ;               BIT 5     DCHO
11                ;               BIT 6     DCHA
12                ;               BIT 7     RQENB (COMPLEMENTS WITH EACH PULSE)
13                ;               BIT 8     DATOA
14                ;               BIT 9     DATOB
15                ;               BIT 10    DATOC
16                ;               BIT 11    DATIA
17                ;               BIT 12    DATIB
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41                ;               EXCLUSIVE OR OF THE OUTPUT DATA
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43                ;
44                ;
45                ;               A 15 BIT DCH ADDRESS BUFFER
46                ;               IS USED TO DIRECT DCH REQUESTS
47                ;               TO ANY LOCATION IN/OUT OF MEMORY.
48                ;
49                ;
50
51                .EOT
```

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0015 EMAPA
**00000 TOTAL ERRORS, 00000 PASS 1 ERRORS
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