digital

DV11-Ø

Engineering Drawings

Digital Equipment Corporation

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CUSTOMER PRINT SET INDEX

THIS IS PRINT SET ☐☐☐☐

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SYNCH MUX LINE CARD	D-CS-M7839-0-1
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LINE CARD 4-7 (SYNCH)	D-BS-DV11-0-11
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ASYNCH MUX LINE CARD	B-PL-M7833-0-0
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LINE CARD 8-11 (ASYNCH)	D-BS-DV11-0-17
LINE CARD 12-15 (ASYNCH)	D-BS-DV11-0-18
BUS CONTROL & MUX	D-CS-M7807-0-1
MODEM CONTROL	D-CS-M7808-0-1
INTERNAL BUS CONN. M92Ø	C-CS-M920-0-1
DV11 DIST. PANEL (C.S.)	D-CS-5411153-0-1
MODEM I/O CABLE ASSY	C-UA-BCØ8R-0-0
H325 TEST CONNECTOR	D-CS-H325-0-1
H861 TEST CONNECTOR	D-CS-H861-0-1
H8612 LINE CARD TEST CONNECTOR	C-UA-H8612-0-0
MODEM CONTROL	D-CS-M7147-0-1

SEQUENCE	MFG. PRINT SET	
DV11 MODULE TEST PROCEDURE		A-SP-DV11-0-2
DV11 TEST PROCEDURE		A-SP-DV11-0-3
ACCEPTANCE PROCEDURE		A-SP-DV11-0-4

UNIT VARIATIONS

VAR	TITLE	PRINT SET 1
DV11-AA	COMM. MUX CONTROL UNIT	X
DV11-BA	MODULE SET & DIST. PANEL (SYNCH)	X
DV11-BB	MODULE SET & DIST. PANEL (ASYNCH)	X
DV11-BC	SYNCH/ASYNCH MODULE SET & DIST. PANEL	X

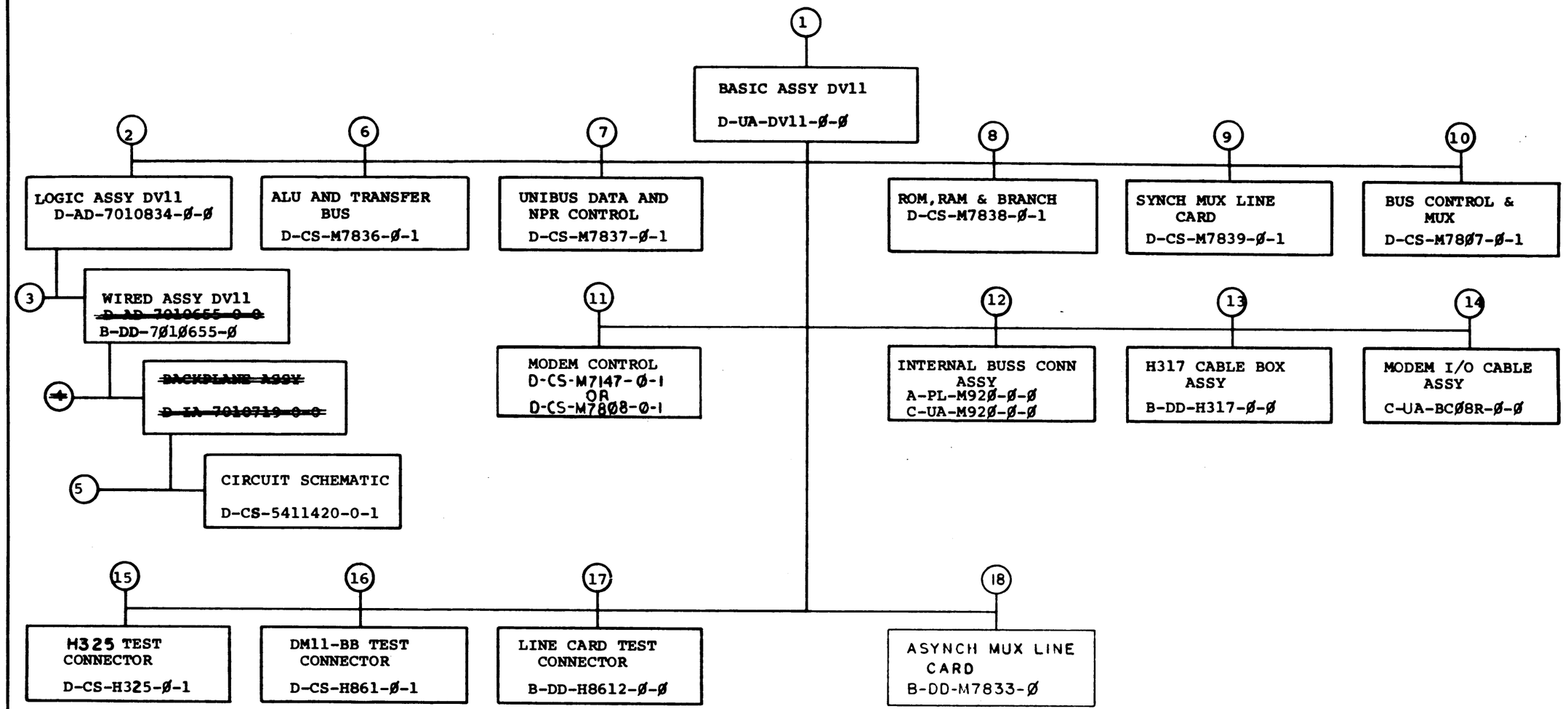
REVISIONS		
DATE	CHG. NO.	REV
5-76	DV11-4	D
REVISED & REDRAWN		E
8-76	DV11-5	F
7-77	DV11-6	H
5-78	DV11-MK7	J
10-78	DV11-MK8	K
6-82	DV11-MKØØ9	

EN-0106-2-1-8-8272-1285

DRB 106

USED ON OPTION/MODEL	
DV11	
SHEET 1 OF 5	

DRN. K. DAVIS	DATE 3-20-75	TITLE: BASIC ASSY (DV11)
CHK'D. S. ROBERTS	DATE 4-23-75	
PROJ ENG. J.E.McNAMARA	DATE 4-23-75	
PROD. R. WALL	DATE 4-23-75	SIZE B / CODE DD / NUMBER DV11-Ø / REV K
FIELD SERV. T. RITTER	DATE 4-25-75	DIST / MP-ØDV11-ØØ



TITLE		SIZE	CODE	NUMBER	REV
BASIC ASSY DV11	SHEET 2 OF 5	B	DD	DV11-Ø	K

DRB 107
DEC 16-(325)-1062-3-N871

CUSTOMER PRINT SET				MFG. SET	ELECTRICAL						CUSTOMER PRINT SET				MFG SET	ELECTRICAL					
1					FIND NO.	DRAWING NO.	REV	NO OF SHT	DESCRIPTION	OPTION NO./FILE DATE	1					FIND NO.	DRAWING NO.	REV	NO OF SHT	DESCRIPTION	OPTION NO./FILE DATE
X					1	D-UA-DV11-Ø-Ø	B	9	BASIC ASSY (DV11)		X					6	D-CS-M7836-Ø-1	#	10	ALU AND TRANSFER BUS	
X						A-SP-DV11-Ø-1	B	44	ENGINEERING SPEC								K-CO-M7836-Ø-4		1	X-Y COORDINATE HOLE LOCATION	
				X		A-SP-DV11-Ø-2	A	3	DV11 MODULE TEST PROCEDURE								D-AH-M7836-Ø-5		1	ASSY/DRILLING HOLE LAYOUT	
				X		A-SP-DV11-Ø-3	B	19	DV11 TEST PROCEDURE								B-MH-M7836-Ø-6		1	MODULE ECO HISTORY	
X				X		A-SP-DV11-Ø-4	A	3	ACCEPTANCE PROCEDURE												
X						A-PL-DV11-Ø-5		1	SHIPPING LIST												
X						A-PL-DV11-Ø-6	A	1	SOFTWARE LIST												
X						D-BD-DV11-Ø-8	A	2	DV11 MODEM CONTROL		X					7	D-CS-M7837-Ø-1	#	11	UNIBUS DATA AND NPR CONTROL	
X						C-IC-DV11-Ø-9	A	1	INTERCONNECTION DV11								K-CO-M7837-Ø-4		1	X-Y COORDINATE HOLE LOCATION	
X						D-BS-DV11-Ø-1Ø	A	8	LINE CARD Ø-3 (SYNCH)								D-AH-M7837-Ø-5		1	ASSY/DRILLING HOLE LAYOUT	
X						D-BS-DV11-Ø-11	A	8	LINE CARD 4-7 (SYNCH)								B-MH-M7837-Ø-6		1	MODULE ECO HISTORY	
X						D-BS-DV11-Ø-12	A	8	LINE CARD 8-11 (SYNCH)												
X						D-BS-DV11-Ø-13	A	8	LINE CARD 12-15 (SYNCH)												
C						K-CS-DV11-Ø-14	A	13	MICROPROGRAM LISTING												
X						D-BS-DV11-Ø-15		10	LINE CARD Ø-3 (ASYNCH)												
X						D-BS-DV11-Ø-16		10	LINE CARD 4-7 (ASYNCH)		X					8	D-CS-M7838-Ø-1	#	11	ROM, RAM & BRANCH	
X						D-BS-DV11-Ø-17		10	LINE CARD 8-11 (ASYNCH)								K-CO-M7838-Ø-4		1	X-Y COORDINATE HOLE LOCATION	
X						D-BS-DV11-Ø-18		10	LINE CARD 12-15 (ASYNCH)								D-AH-M7838-Ø-5		1	ASSY/DRILLING HOLE LAYOUT	
																	B-MH-M7838-Ø-6		1	MODULE ECO HISTORY	
																	K-CS-M7838-Ø-8		9	23-A1Ø1A2 (ROM LIST)	
																	K-CS-M7838-Ø-9		9	23-A1Ø2A2 (ROM LIST)	
X					2	D-AD-7010834-0-0	#	1	LOGIC ASSY (DV11)								K-CS-M7838-Ø-1Ø		9	23-A1Ø3A2 (ROM LIST)	
X						D-IA-7010835-0-0	#	1	POWER HARNESS (DV11)								K-CS-M7838-Ø-11		9	23-A1Ø4A2 (ROM LIST)	
																	K-CS-M7838-Ø-12		9	23-A1Ø5A2 (ROM LIST)	
																	K-CS-M7838-Ø-13		9	23-A1Ø6A2 (ROM LIST)	
																	K-CS-M7838-Ø-14		9	23-A1Ø7A2 (ROM LIST)	
~~X~~					~~3~~	~~D-AD-7010655-0-0~~	~~#~~	~~1~~	~~WIRED ASSY (DV11)~~								K-CS-M7838-Ø-15		9	23-A1Ø8A2 (ROM LIST)	
~~C~~						~~K-WL-DV11-Ø-7~~	~~A~~	~~1~~	~~WIRE LIST~~												
						~~A-WT-7010655-0~~		~~1~~	~~AWT REVISION STATUS~~												
					3	B-DD-7010655-Ø	A	1	DRAWING DIRECTORY												
											X					9	D-CS-M7839-Ø-1	#	9	SYNCH MUX LINE CARD	
																	K-CO-M7839-Ø-4		1	X-Y COORDINATE HOLE LOCATION	
																	D-AH-M7839-Ø-5		1	ASSY/DRILLING HOLE LAYOUT	
																	B-MH-M7839-Ø-6		1	MODULE ECO HISTORY	
~~X~~					~~4~~	~~D-IA-7010719-0-0~~	~~#~~	~~1~~	~~BACKPLANE ASSY~~												
X					5	D-CS-5411420-0-1	#	1	CIRCUIT SCHEMATIC												
						K-CO-5411420-0-4		1	X-Y COORDINATE HOLE LOCATION												
						D-AH-5411420-0-5		1	ASSY/DRILLING HOLE LAYOUT												
						B-MH-5411420-0-6		1	MODULE ECO HISTORY												

CUSTOMER PRINT SET CODES	X = PRINT OF DOCUMENT INCLUDED IN PRINT SET C = INCLUDES ALL PRINTS INDICATED ON DOCUMENT S = CONFIDENTIAL AUTHORIZED SIGNATURE REQUIRED	TITLE: BASIC ASSY (DV11)	SHEET 3 OF 5	SIZE: B	CODE: DD	NUMBER: DV11-Ø	REV: K

DRB 108

MK

CUSTOMER PRINT SET 1	MFG. SET	ELECTRICAL FIND NO.	DRAWING NO.	REV	NO OF SHT	DESCRIPTION	OPTION NO./FILE DATE
X		10	D-CS-M78Ø7-Ø-1	#	7	BUS CONTROL & MUX	
			K-CO-M78Ø7-Ø-4		1	X-Y COORDINATE HOLE LOCATION	
			D-AH-M78Ø7-Ø-5		1	ASSY/DRILLING HOLE LAYOUT	
			B-MH-M78Ø7-Ø-6		1	MODULE ECO HISTORY	
X		11	D-CS-M7147-Ø-1	#	7	MODEM CONTROL	
			K-CO-M7147-Ø-4		1	X-Y COORDINATE HOLE LOCATION	
			D-AH-M7147-Ø-5		1	ASSY/DRILLING HOLE LAYOUT	
			B-MH-M7147-Ø-6		1	MODULE ECO HISTORY	
		12	C-UA-M92Ø-Ø-Ø		1	INTERNAL BUS CONN. ASSY	
			A-PL-M92Ø-Ø-Ø		1	INTERNAL BUS CONN. M92Ø	
X			C-CS-M92Ø-Ø-1	**	1	INTERNAL BUS CONN. M92Ø	
			K-CO-M92Ø-Ø-4		1	X-Y COORDINATE HOLE LOCATION	
			D-AH-M92Ø-Ø-5		1	ASSY/DRILLING HOLE LAYOUT	
		13	B-DD-H317-Ø-Ø	.	3	H317 CABLE BOX ASSY	
X			D-CS-5411153-0-1	#	3	DV11 DIST. PANEL (C.S.)	
X		14	C-UA-BCØ8R-Ø-Ø	#	1	BCØ8R I/O CABLE	
X		15	D-CS-H325-Ø-1	#	1	H325 TEST CONNECTOR	
			K-CO-H325-Ø-4		1	X-Y COORDINATE HOLE LOCATION	
			C-AH-H325-Ø-5		1	ASSY/DRILLING HOLE LAYOUT	
			B-MH-H325-Ø-6		1	MODULE ECO HISTORY	

CUSTOMER PRINT SET 1	MFG SET	ELECTRICAL FIND NO.	DRAWING NO.	REV	NO OF SHT	DESCRIPTION	OPTION NO./FILE DATE
X		16	D-CS-H861-Ø-1	#	1	DM11-BB TEST CONNECTOR	
			K-CO-H861-Ø-4		1	X-Y COORDINATE HOLE LOCATION	
			D-AH-H861-Ø-5		1	ASSY/DRILLING HOLE LAYOUT	
			B-MH-H861-Ø-6		1	MODULE ECO HISTORY	
		17	B-DD-H8612-Ø		2	LINE CARD TEST CONNECTOR	
X			C-UA-H8612-Ø-Ø	#	1	LINE CARD TEST CONNECTOR	
		18	B-DD-M7833-Ø		1	ASYNCH MUX LINE CARD	
X			D-UA-M7833-Ø-Ø		3	ASYNCH MUX LINE CARD	
X			B-PL-M7833-Ø-Ø		4	ASYNCH MUX LINE CARD	
X			D-CS-M7833-Ø-1		10	ASYNCH MUX LINE CARD	
			D-MD-5Ø12Ø25-Ø-Ø		3	DRILL AND ETCH DRAWING	
			B-MH-M7833-Ø-6		1	ASYNCH MUX LINE CARD	
X		11	D-CS-M7808-Ø-1	#	7	MODEM CONTROL	
			K-CO-M7808-Ø-4		1	X-Y COORDINATE HOLE LOCATION	
			D-AH-M7808-Ø-5		1	ASSY/DRILLING HOLE LAYOUT	
			B-MH-M7808-Ø-6		1	MODULE ECO HISTORY	

CUSTOMER PRINT SET CODES

X = PRINT OF DOCUMENT INCLUDED IN PRINT SET
C = INCLUDES ALL PRINTS INDICATED ON DOCUMENT
S = CONFIDENTIAL AUTHORIZED SIGNATURE REQUIRED

TITLE		SIZE	CODE	NUMBER	REV
BASIC ASSY (DV11)	SHEET 4 OF 5	B	DD	DV11-Ø	K

DRB 108

DEC 16-(325)-1062-2B-R972

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CUSTOMER PRINT SET				MFG. SET	MECHANICAL						CUSTOMER PRINT SET				MFG SET	MECHANICAL				
1					FIND NO.	DRAWING NO.	REV	NO OF SHT	DESCRIPTION	OPTION NO./FILE DATE						FIND NO.	DRAWING NO.	REV	NO OF SHT	DESCRIPTION	OPTION NO./FILE DATE
					1	D-UA-DV11-Ø-Ø	B	9	BASIC ASSY (DV11)											
						D-MD-7408510-0-0		1	CROSS BAR CABLE BRKT											
						C-IA-7408283-0-0		1	SIDE BAR SUPPORT											
						C-IA-7411632-0-0		1	STRAIN RELIEF											
						C-IA-7411633-0-0		1	CLAMP, STRAIN RELIEF											
					2	D-AD-7010834-0-0		1	LOGIC ASSY (DV11)											
						D-IA-7010835-0-0		1	POWER HARNESS (DV11)											
					3	B-DD-7010655-0		1	DV11 WIRED ASSY											
					4	~~D-IA-7010719-0-0~~		~~1~~	~~BACKPLANE ASSY~~											
					12	C-UA-M92Ø-Ø-Ø		1	INTERNAL BUS CONN ASSY											
						A-PL-M92Ø-Ø-Ø		1	INTERNAL BUS CONN. M92Ø											
						A-DC-7407806-0-0		1	DEC UNIBUS DECAL											
					13	B-DD-H317-Ø		3	H317 CABLE BOX ASSY											
					14	C-UA-BCØ8R-Ø-Ø		1	MODEM I/O CABLE ASSY											

CUSTOMER PRINT SET CODES	TITLE	SHEET	SIZE	CODE	NUMBER	REV
X = PRINT OF DOCUMENT INCLUDED IN PRINT SET C = INCLUDES ALL PRINTS INDICATED ON DOCUMENT S = CONFIDENTIAL AUTHORIZED SIGNATURE REQUIRED	BASIC ASSY (DV11)	5 OF 5	B	DD	DV11-Ø	K

DRB 108

DEC 16-(325)-1062-2B-R972

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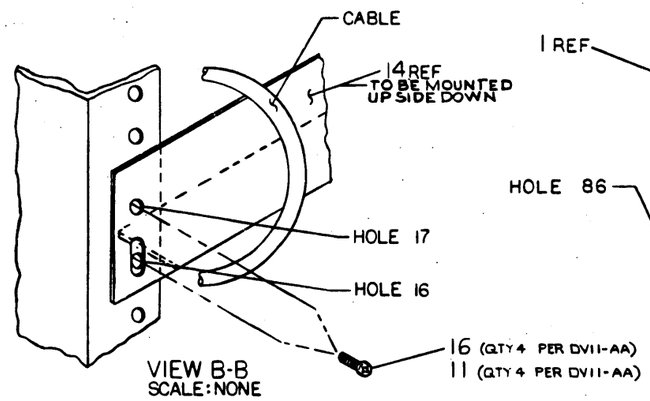
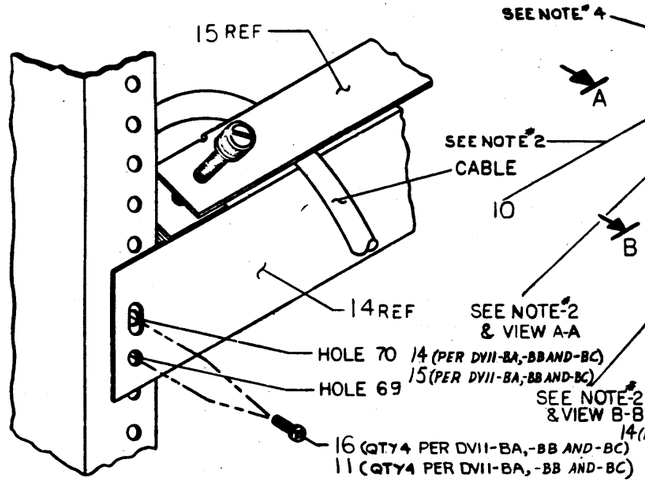
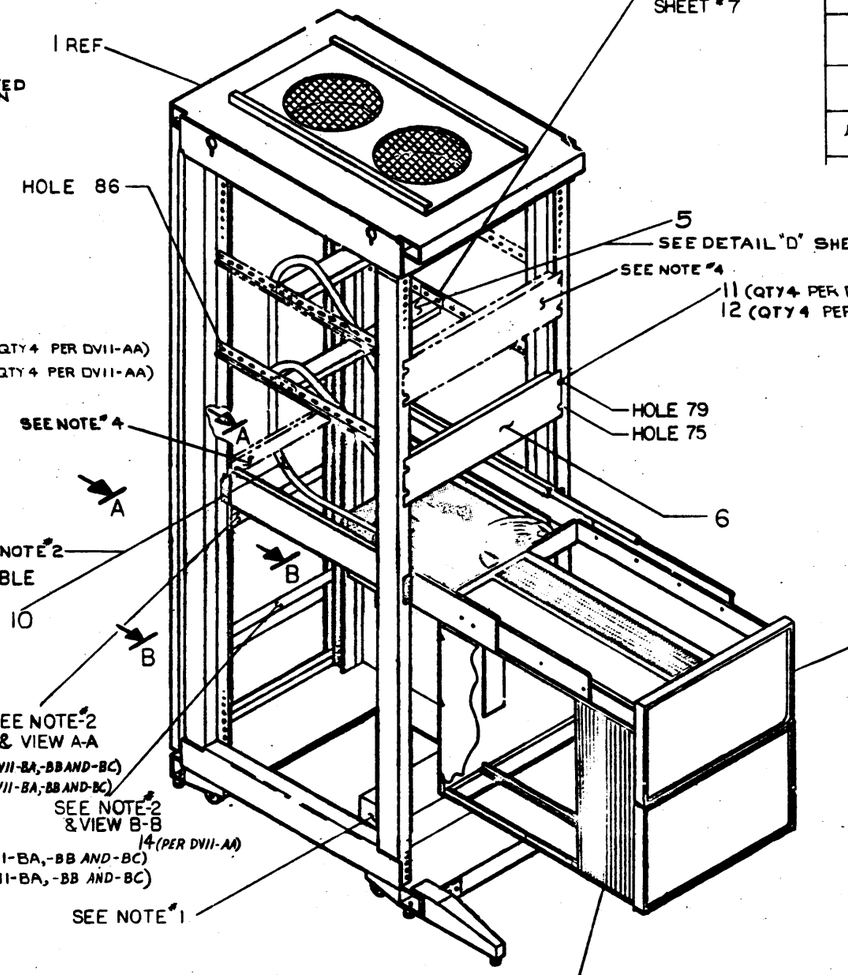


VIEW B-B
SCALE: NONE



VIEW A-A



LEGEND	
NUMBER	VARIATION
DV11-AA	COMM MUX CONTROL UNIT
DV11-BA	MODULE SET & DIST. PANEL FOR 8 SYNC LINES
DV11-BB	MODULE SET & DIST. PANEL FOR 8 ASYN LINES
DV11-BC	MODULE SET & DIST PANEL FOR 4 SYNC LINES AND 4 ASYN LINES

NOTES:

1. 861 POWER CONTROL MUST BE LOCATED AT FRONT OF CABINET TO ALLOW CABLES FROM ITEM ("6) TO SWEEP BEHIND AND UNDER ITEM "2
2. EACH H960 CONTAINING A DV11 SHALL HAVE ONE STRAIN RELIEF (ITEM 14) AND CLAMP (ITEM 15) FOR BC08R CABLES AND ONE STRAIN RELIEF AT THE LOWER REAR OF CABINET, SEE VIEWS A-A AND B-B.
3. A CABINET THAT CONTAINS AN EXPANDER BOX CANNOT HAVE MORE THAN TWO CABLE BOX ASSEMBLIES, ITEM "6) FOR SYSTEMS WITH THREE OR MORE CABLE BOX ASSEMBLIES, A SEPERATE CABINET MUST BE USED. UP TO FOUR (4) PANELS CAN BE MOUNTED INTO CABINETS WITHOUT AN EXPANDER BOX.
4. 8 LINE SYSTEM IS SHOWN: TO MAKE UP 16 LINE SYSTEM ADD THE FOLLOWING EQUIPMENT (SHOWN WITH PHANTOM LINES): ONE H317-C (ITEM "5) USING MTG HOLES "93 & 97, TWO SIDE BAR SUPPORTS (ITEM "8) USING MTG HOLE "99, ONE CROSS BAR CABLE BRKT (ITEM "5), ONE STRAIN RELIEF (ITEM "14), ONE CLAMP, STRAIN RELIEF (ITEM "15) AND NECESSARY MTG HARDWARE

DV11-BC	DV11-BB	DV11-BA	DV11-AA			
1	2	-	-	ASYNCH MUX LINE CARD	D-CS-M7833-0-1	27
1	1	1	-	H325 TEST CONNECTOR	D-CS-H325-0-1	26
-	-	-	1	H861 TEST CONNECTOR	D-CS-H861-0-1	25
2	2	2	-	LINE CARD TEST CONNECTOR	C-UA-H862-0-0	24
-	-	-	1	MODEM CONTROL	D-CS-M7147-0-1	23
1	-	2	-	SYNCH MUX LINE CARD	D-CS-M7839-0-1	22
-	-	-	1	ROM, RAM & BRANCH	D-CS-M7838-0-1	21
-	-	-	1	UNIBUS DATA AND NPR CONTROL	D-CS-M7837-0-1	20
-	-	-	1	ALU AND TRANSFER BUS	D-CS-M7836-0-1	19
-	-	-	1	BUS CONTROL & MUX	D-CS-M7867-0-1	18
-	-	-	1	INTERNAL BUS CONN M920	C-UA-M920-0-0	17
8	8	8	4	SCR PHL PAN HD 10-32 X 3/8 LG	90006071-1	16
1	1	1	-	CLAMP, STRAIN RELIEF	C-IA-7411633-00	15
1	1	1	1	STRAIN RELIEF	C-IA-7411632-00	14
-	-	-	4	SCR PHL PAN HD 8-32-1 LG	90006043-1	13
8	8	8	-	SCR PHL PAN HD 10-32-5/8 LG	9006074-1	12
8	8	8	4	NUT, TINNERMAN #10-32	9007786	11
4	4	4	-	I/O CABLE (BC08R-12.0	C-UA-BC08R-12-0	10
-	-	-	1	PRIORITY JUMPER LEVEL "5	C-IA-5408778-0-0	9
2	2	2	-	SIDE BAR SUPPORT	C-IA-7408283-00	8
-	-	-	4	WASHER, LOCK #8 EXT TOOTH	9008072	7
1	1	1	-	H317-C CABLE BOX ASS'Y	D-UA-H317-C-0	6
1	1	1	-	CROSS BAR CABLE BRKT.	D-MD-7408510-0-0	5
8	8	8	-	WASHER LOCK #10 EXT	9007651	4
-	-	-	1	LOGIC ASSY (DV11)	D-AD-10C834-00	3
REF	REF	REF	REF	MOUNTING BOX ASSY	D-UA-BA11-FC-0	2
REF	REF	REF	REF	H960 CABINET	D-UA-H960-CD-0	1
		QTY		DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

REVISIONS			
DOC.	CHANGE NO.	REV.	
23	DV11-00004	A	2 Lines Shifted 5-30-75 J. MCNAMARA
DEL	DV11-MK007	B	Del Line 1/2 7-10-75 R. HARRINGTON
24	DV11-MK008	C	R. Harrington 11-07-75 R. HARRINGTON

FIRST USED ON OPTION/MODEL	PDP11
UNLESS OTHERWISE SPECIFIED DIMENSION IS INCHES. TOLERANCES	
DECIMALS	ANGLES
.XXX = .005 .XX = .02 X = .1	±0° 30'
REMOVE BURRS AND BREAK SHARP CORNERS. SURFACE QUALITY: ✓	
MATERIAL	
FINISH	

DRN. C. Avery 11-25-74
ENGR. R. J. Blute 4-25-75
MFG. 4-23-75
QUAL. 4-27-75
NEXT HIGHER ASSY. B-DD-DV11-0

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE: BASIC ASSY DV11

SIZE D | CODE UA | NUMBER DV11-0-0 | REV. C
SCALE
SHEET 1 OF 9
DIST.

D UA DV11-0-0 B

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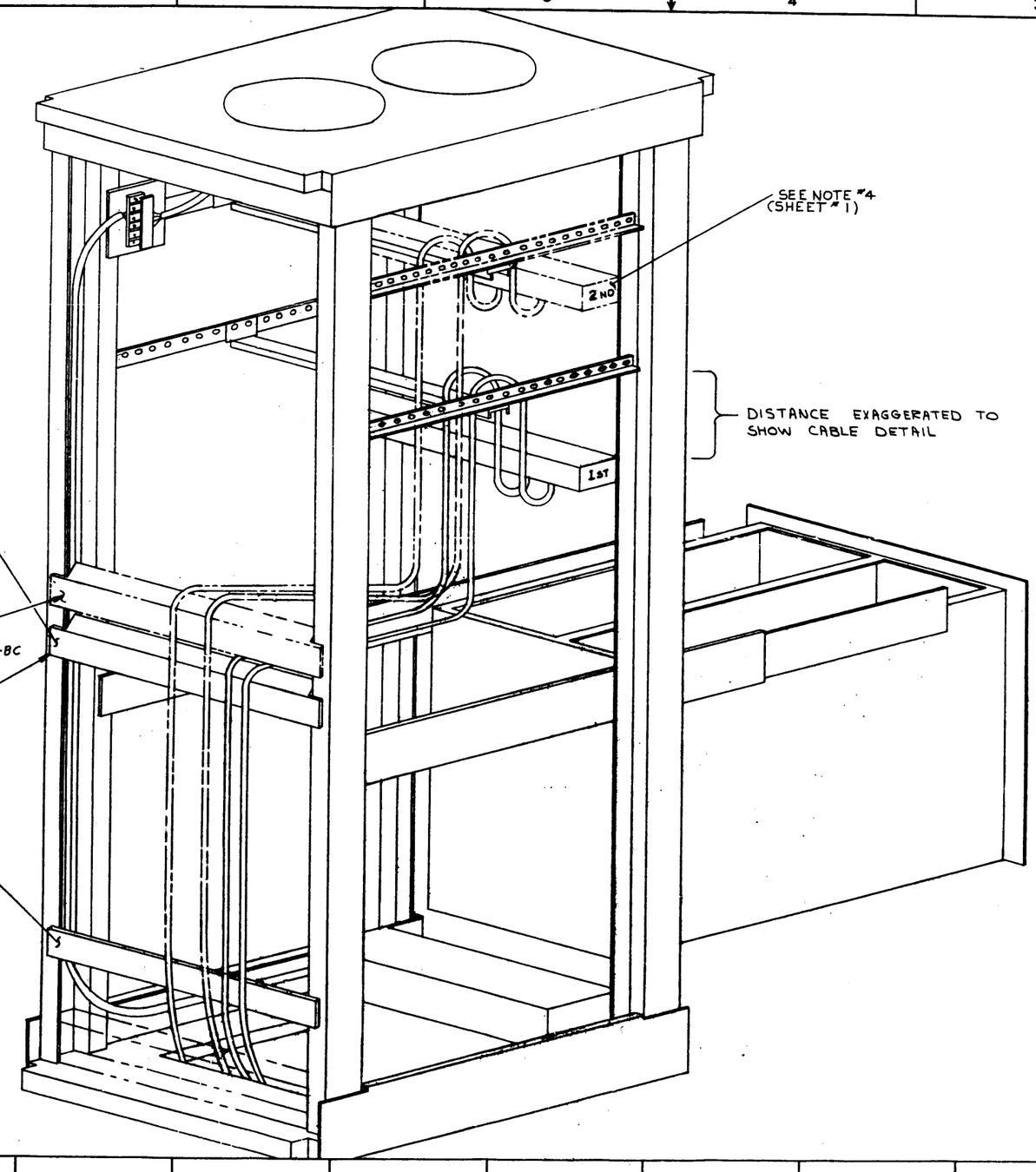

NOTE:
FOR ROUTING BC05D CABLES FROM DISTRIBUTION PANELS TO MODEMS. SEE SHEET #3 FOR ROUTING BC05R CABLES.

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	BASIC ASSY DV11			
SCALE NONE	SHEET 2 OF 9	SIZE D	CODE UA	NUMBER DV11-Ø-Ø
DIST. MK				REV. C

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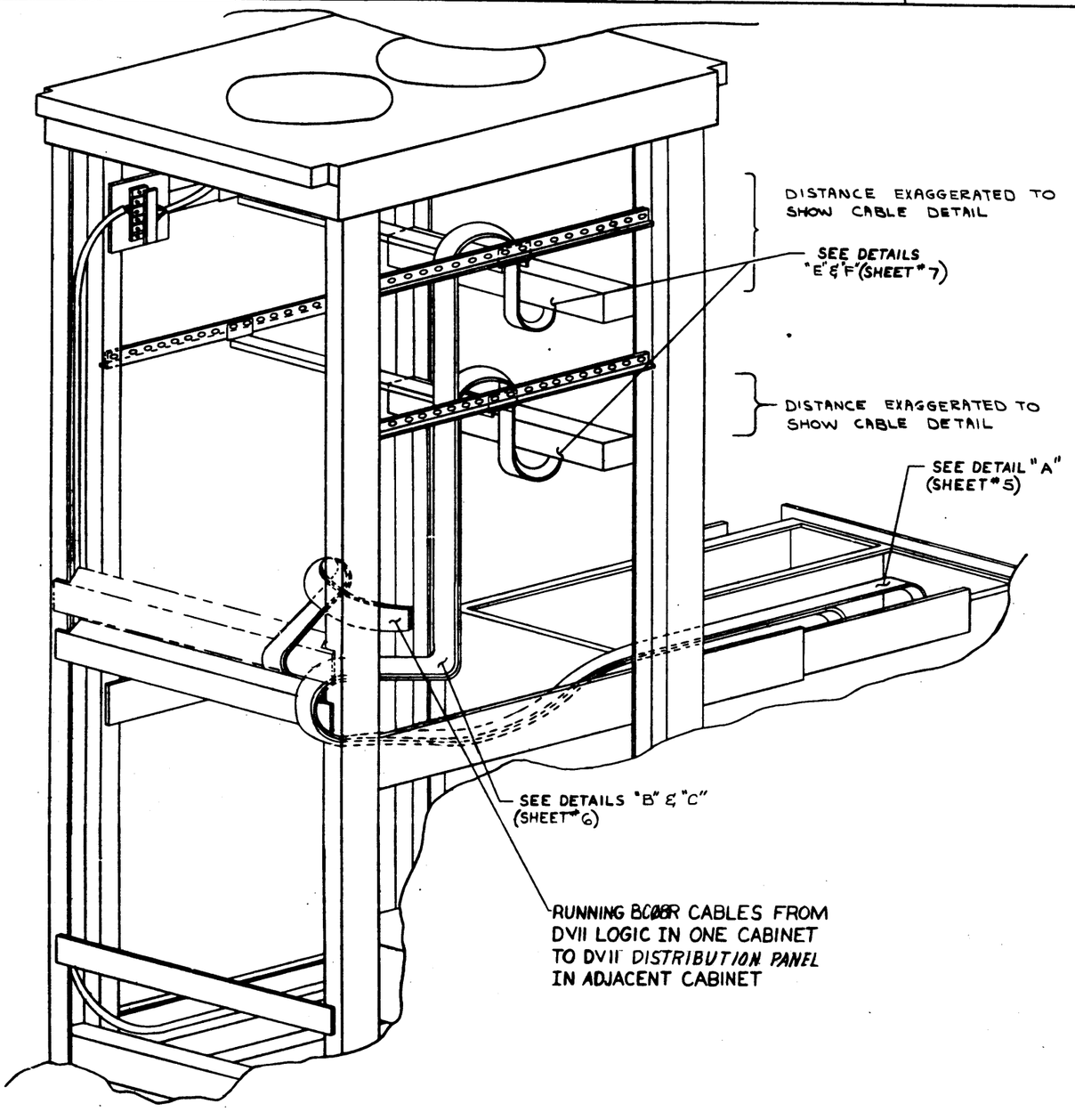

NOTE:
FOR ROUTING BC05R CABLES FROM DV11 LOGIC & EXPANDER BOX TO DISTRIBUTION PANELS IN SAME CABINET OR ADJACENT CABINET. SEE SHEET # 2 FOR BC05D CABLE ROUTING.

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	BASIC ASSY. DV11		SIZE	CODE	NUMBER / REV.
			D	UA	DV11-Ø-Ø / C
SCALE	NONE	SHEET 3 OF 9	DIST.		

MK

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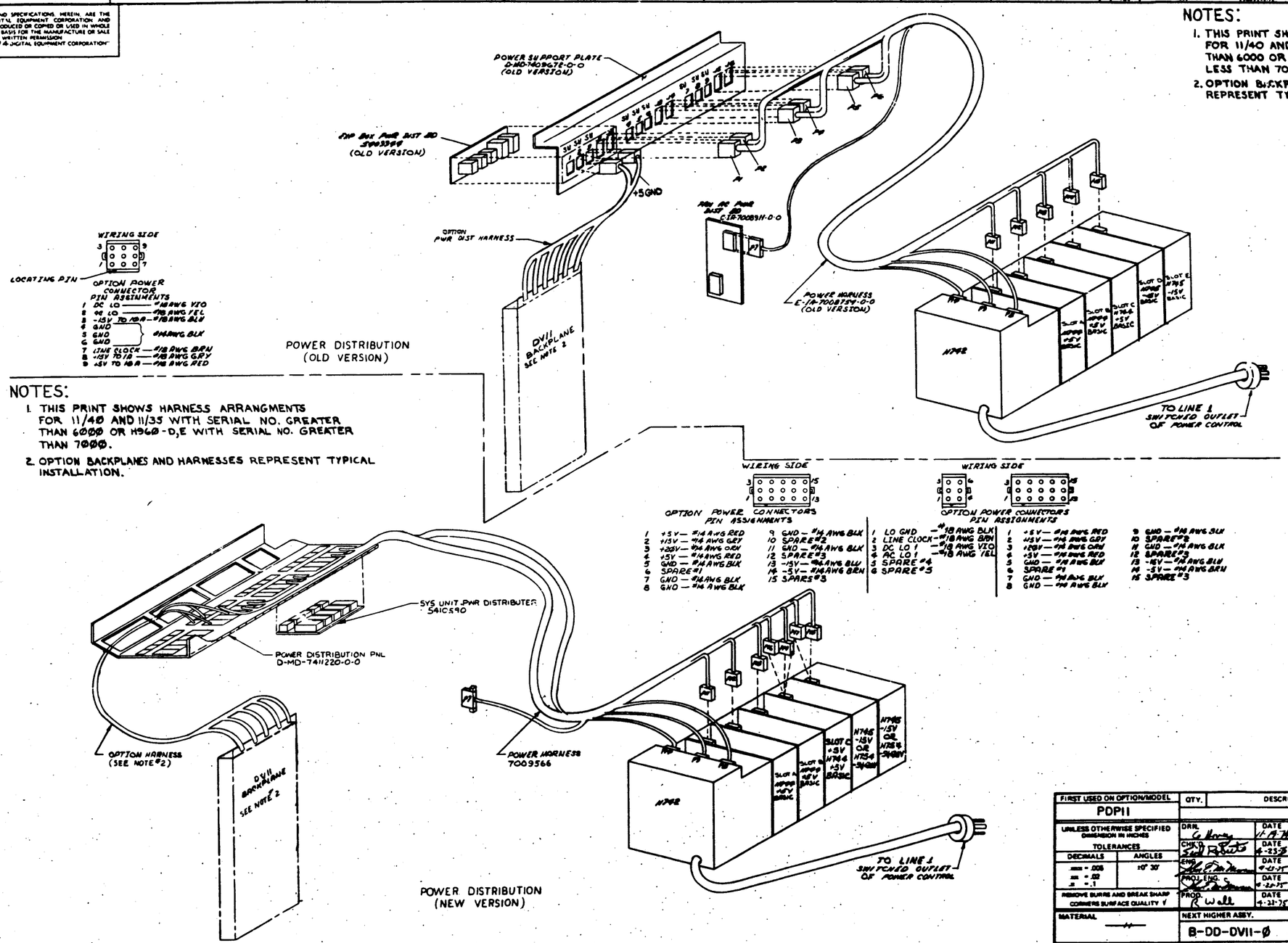
NOTES:

1. THIS PRINT SHOWS HARNESS ARRANGMENTS FOR 11/40 AND 11/35 WITH SERIAL NO. LESS THAN 6000 OR H960-D,E WITH SERIAL NO. LESS THAN 7000.
2. OPTION BACKPLANES AND HARNESSES REPRESENT TYPICAL INSTALLATION.



NOTES:

1. THIS PRINT SHOWS HARNESS ARRANGMENTS FOR 11/40 AND 11/35 WITH SERIAL NO. GREATER THAN 6000 OR H960-D,E WITH SERIAL NO. GREATER THAN 7000.
2. OPTION BACKPLANES AND HARNESSES REPRESENT TYPICAL INSTALLATION.

WIRING SIDE

OPTION POWER CONNECTORS PIN ASSIGNMENTS

1	+5V — #14 AWG RED	9	GND — #14 AWG BLK
2	+15V — #14 AWG GRY	10	SPARE #2
3	+20V — #14 AWG ORN	11	GND — #14 AWG BLK
4	+5V — #14 AWG RED	12	SPARE #3
5	GND — #14 AWG BLK	13	-15V — #14 AWG BLU
6	SPARE #1	14	-5V — #14 AWG BRN
7	GND — #14 AWG BLK	15	SPARE #3
8	GND — #14 AWG BLK		

WIRING SIDE

OPTION POWER CONNECTORS PIN ASSIGNMENTS

1	LO GND — #18 AWG BLK	1	+5V — #14 AWG RED
2	LINE CLOCK — #18 AWG BRN	2	+15V — #14 AWG GRY
3	DC LO 1 — #18 AWG VIO	3	+20V — #14 AWG ORN
4	AC LO 1 — #18 AWG YEL	4	+5V — #14 AWG RED
5	SPARE #4	5	GND — #14 AWG BLK
6	SPARE #5	6	SPARE #1
		7	GND — #14 AWG BLK
		8	GND — #14 AWG BLK
		9	GND — #14 AWG BLK
		10	SPARE #2
		11	GND — #14 AWG BLK
		12	SPARE #3
		13	-15V — #14 AWG BLU
		14	-5V — #14 AWG BRN
		15	SPARE #3

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
PDP11		PARTS LIST		

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES
TOLERANCES
DECIMALS .xxx = .005 .xx = .02 .x = .1
ANGLES ±0° 30'
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY √
MATERIAL —//—
FINISH —//—

DRN. C. Hovey DATE 11-19-74
CHK'D. Sidd Roberts DATE 4-23-75
ENG. [signature] DATE 4-23-75
PROJ. ENG. [signature] DATE 4-23-75
PROD. R. Wall DATE 4-23-75

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE BASIC ASSY DV11

NEXT HIGHER ASSY. B-DD-DV11-Ø
SCALE —//—
SHEET 4 OF 4

SIZE D CODE UA NUMBER DV11-Ø-Ø REV. C
DIST.

REVISIONS: CHK | CHANGE NO | REV

MK

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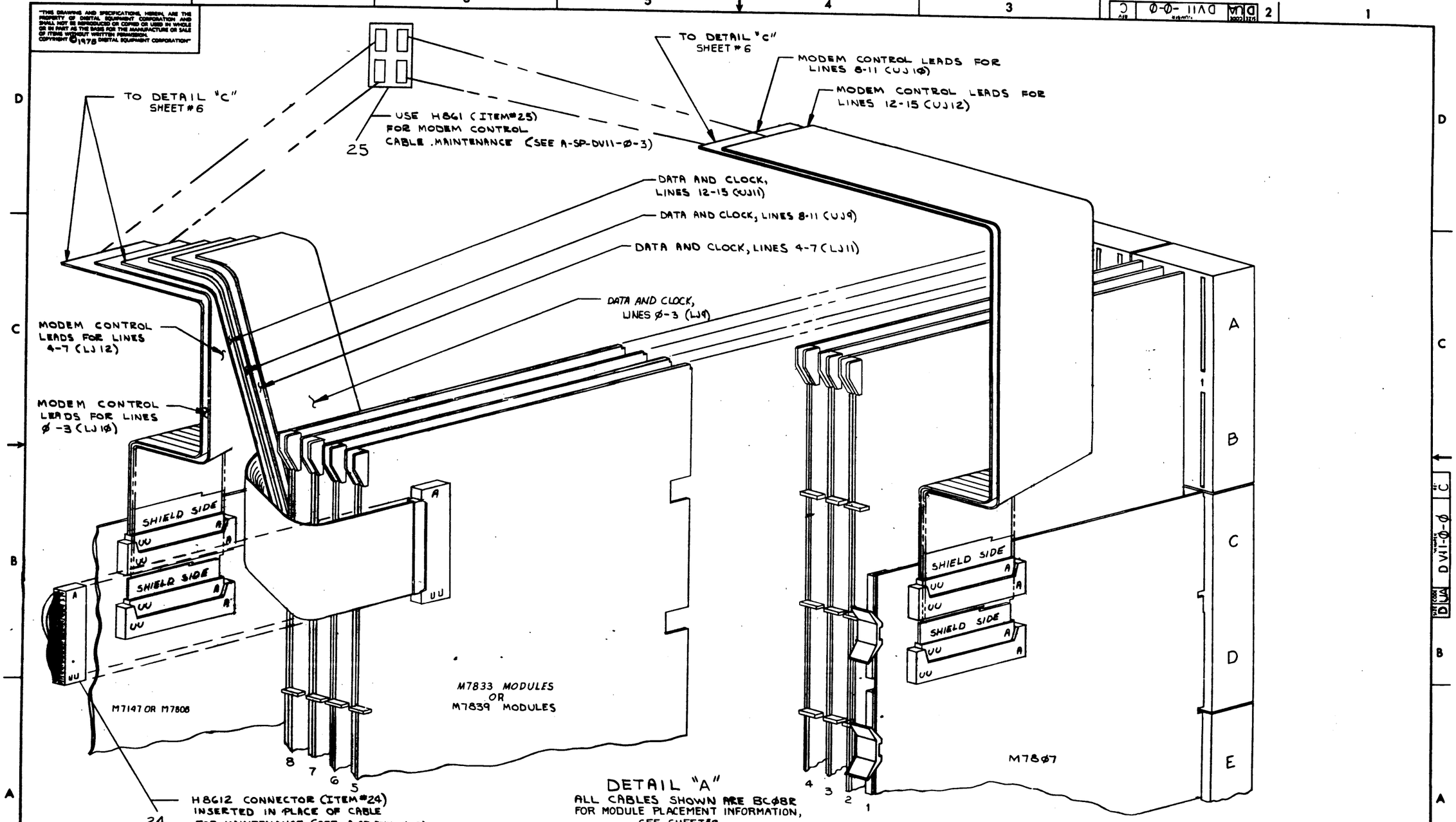

REVISIONS		
CHK	CHANGE NO.	REV.

APPLICATION: DV11-AA,BA,BB,BC

TITLE	SIZE	CODE	NUMBER	REV.
BASIC ASSY DV11	D	UA	DV11-0-0	C
SCALE NONE SHEET 5 OF 9	DIST.			

MK

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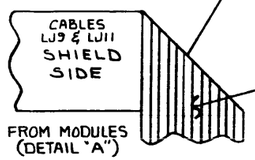
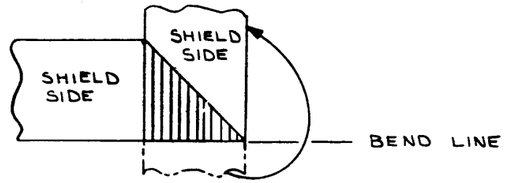
FOLD LJ9 & LJ11 TOGETHER AS ONE CABLE

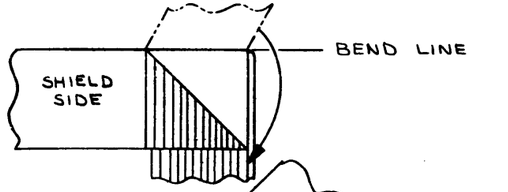
STEP #1



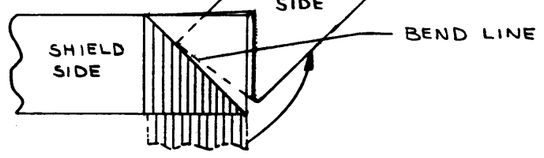
STEP #2



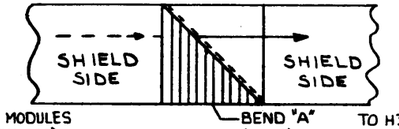
STEP #3



STEP #4

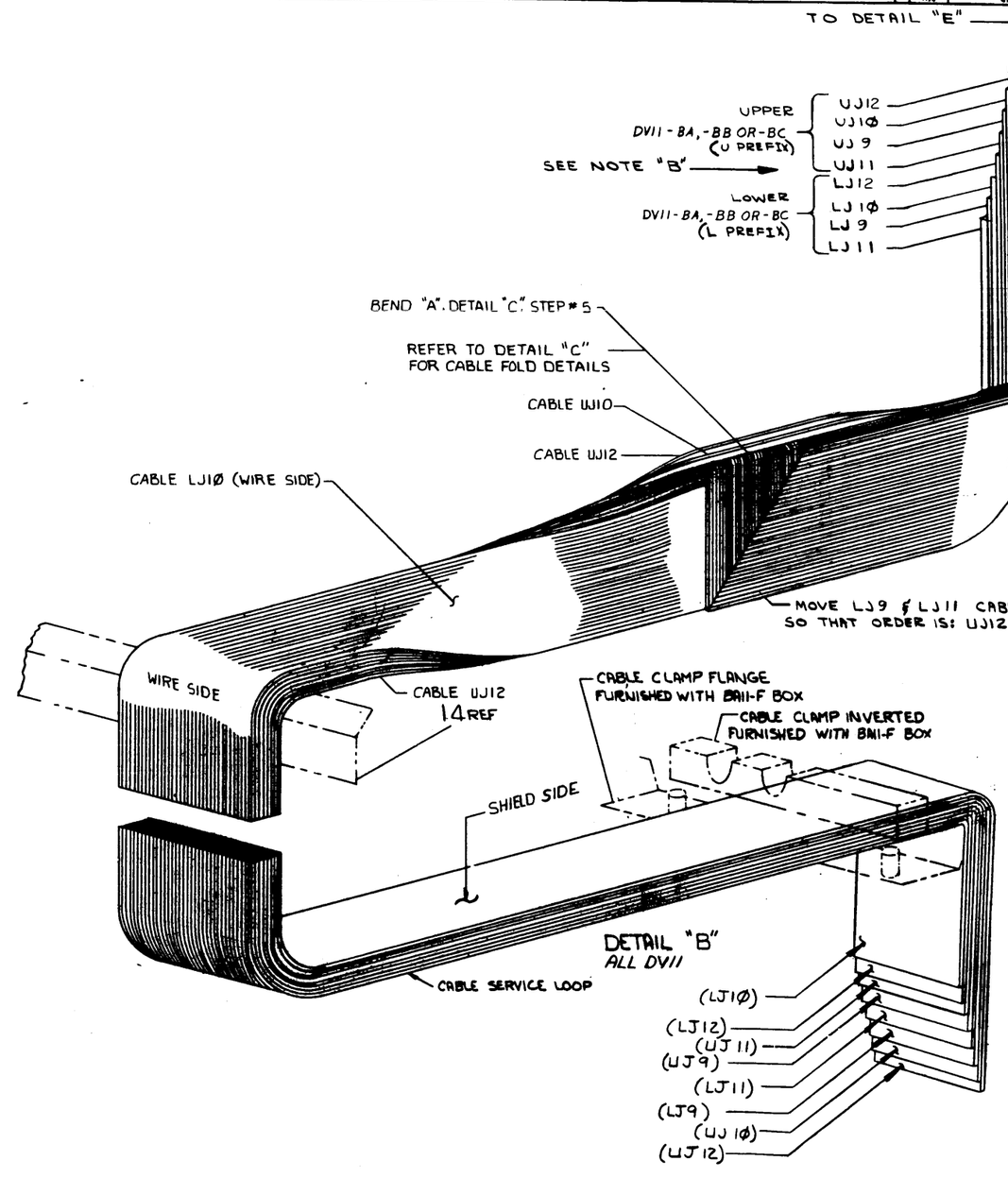


STEP #5



DETAIL "C"

NOTE THAT UJ9, UJ11, LJ12, LJ10 CABLES CAN PASS THROUGH THE FOLDED AREA AS SHOWN BY DOTTED ARROW AND SOLID ARROW. NOTE THAT FOLDED CABLE IS INSTALLED IN DETAIL "B" UPSIDE DOWN FROM VIEW SHOWN IN DETAIL "C" - REFER TO POSITION OF BEND "A".

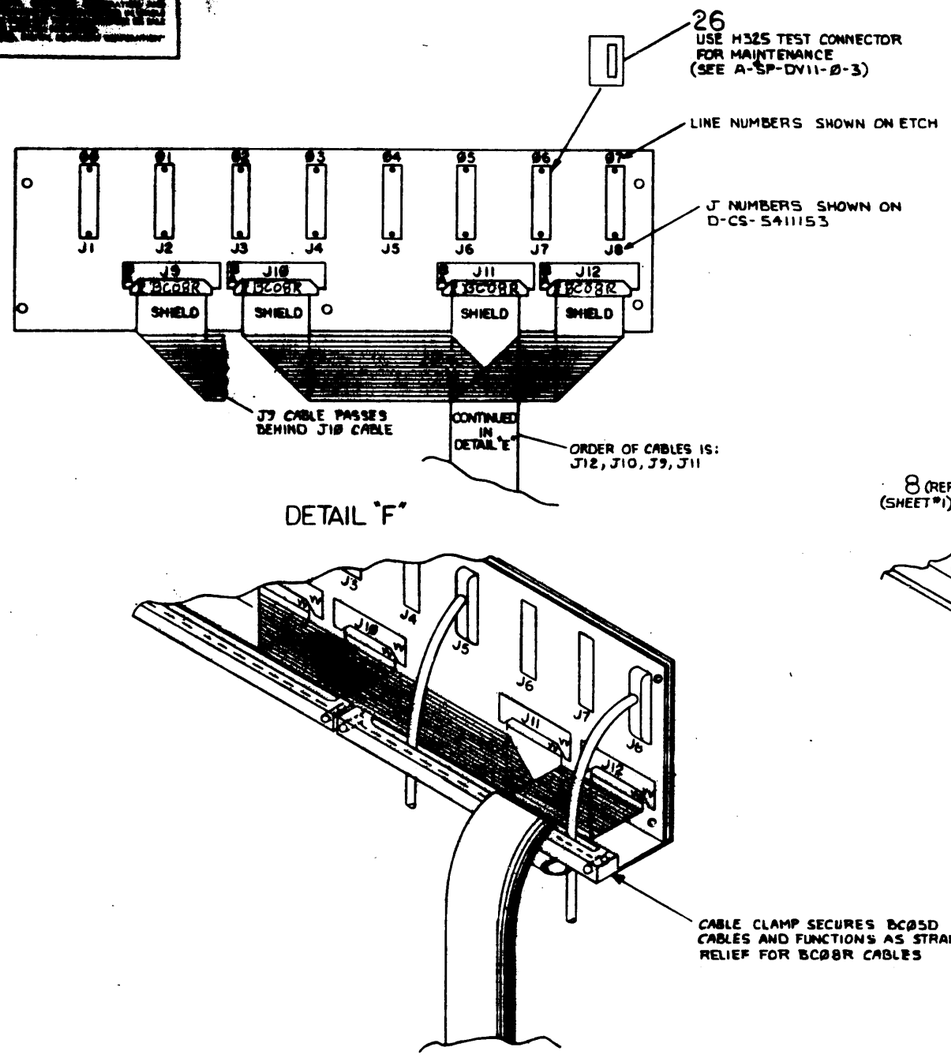


NOTES:
A. INSTALL VINYL FOAM BETWEEN UNIBUS & OTHER CABLES WHERE UNIBUS GOES THRU CABLE CLAMPS.
B. DVII DISTRIBUTION PANEL (H317C) CONTAINING D-CS-5411153) REFER TO DETAILS "E" AND "F" ON SHEET # 7.

REVISIONS		
CHK	CHANGE NO.	REV.

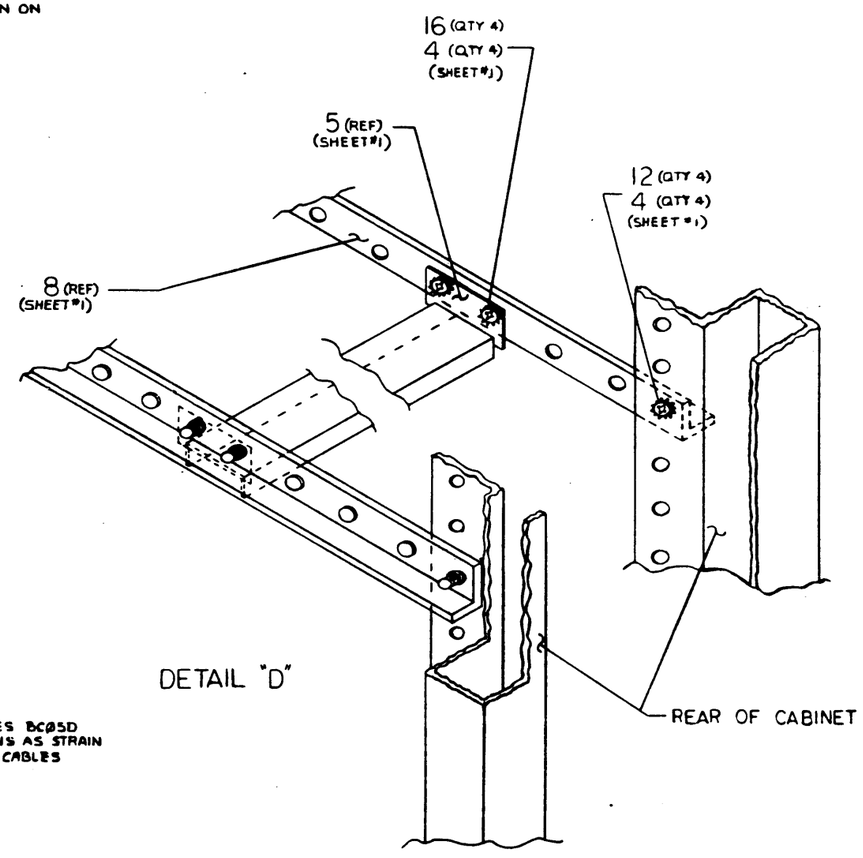
TITLE	BASIC ASSY. DVII	SIZE / CODE	NUMBER / REV.
SCALE NONE	SHEET 6 OF 9	D UA	DVII-Ø-Ø C
		DIST.	

MK



DETAIL "F"

DETAIL "E"
CONTINUED FROM DETAIL "F"



DETAIL "D"

REVISIONS		
CODE	CHANGE NO.	REV.

TITLE	BASIC ASSY DV11	SIZE / CODE	NUMBER
		D / UA	DV11-Ø-Ø
SCALE	NONE	SHEET 7 OF 9	REV. C
		DIST.	MK

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VECTORS:

OCTAL TO SWITCH POSITION CONVERSIONS FOR M7837

VECTORS

	8	7	6	5	4	3	2	
300	ON	OFF	OFF	ON	ON	ON	*	*VECTOR BIT 2 IS CONTROLLED BY DV11 LOGIC
304	ON	OFF	OFF	ON	ON	ON	*	
310	ON	OFF	OFF	ON	ON	OFF	*	
314	ON	OFF	OFF	ON	ON	OFF	*	
320	ON	OFF	OFF	ON	OFF	ON	*	
324	ON	OFF	OFF	ON	OFF	ON	*	
330	ON	OFF	OFF	ON	OFF	OFF	*	
334	ON	OFF	OFF	ON	OFF	OFF	*	
340	ON	OFF	OFF	OFF	ON	ON	*	
350	ON	OFF	OFF	OFF	ON	OFF	*	
360	ON	OFF	OFF	OFF	OFF	ON	*	
370	ON	OFF	OFF	OFF	OFF	OFF	*	
400	OFF	ON	ON	ON	ON	ON	*	
410	OFF	ON	ON	ON	ON	OFF	*	
420	OFF	ON	ON	ON	OFF	ON	*	
430	OFF	ON	ON	ON	OFF	OFF	*	

OCTAL TO JUMPER CONVERSIONS FOR M7807

VECTORS

	8	7	6	5	4	3	2
300	OUT	IN	IN	OUT	OUT	OUT	OUT
304	OUT	IN	IN	OUT	OUT	OUT	IN
310	OUT	IN	IN	OUT	OUT	IN	OUT
314	OUT	IN	IN	OUT	OUT	IN	IN
320	OUT	IN	IN	OUT	IN	OUT	OUT
324	OUT	IN	IN	OUT	IN	OUT	IN

ADDRESSES:

M7836
DV11 DATA CONTROL ADDRESS OFF-1, ON-0
BITS 9,11,12 ARE OFF
BIT 10 IS ON

		8	7	6	5	4
775	000	ON	ON	ON	ON	ON
	040	ON	ON	ON	OFF	ON
	100	ON	ON	OFF	ON	ON
	140	ON	ON	OFF	OFF	ON

M7807
DV11 MODEM CONTROL ADDRESS OUT-1, IN-0
BITS 9,11,12 ARE OUT
BIT 10 IS IN

		8	7	6	5	4	3
775	020	IN	IN	IN	IN	OUT	IN
	060	IN	IN	IN	OUT	OUT	IN
	120	IN	IN	OUT	IN	OUT	IN
	160	IN	IN	OUT	OUT	OUT	IN

PDP 11 BIT TO OCTAL DIGIT CORRESPONDENCE

BIT	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
EXAMPLE	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0
OCTAL DIGIT	6TH			5TH			4TH			3RD			2ND			1ST		
EXAMPLE	7			7			5			0			0			0		

NOTE. I/O DEVICE ADDRESS IN #11 LITERATURE ARE VARIOUSLY GIVEN AS 760 000 THRU 777 777 AND AS 160 000 THRU 177 777
THESE ARE EQUIVALENT IN MACHINES WITHOUT MEMORY MANAGEMENT, WHENEVER BITS 15,14, AND 13 ARE ALL "1" (16X XXX OR 17X XXX) THE PROCESSOR ALSO MAKES BITS 17 AND 16 "1" (76X XXX OR 77X XXX) [ON MACHINES WITH MEMORY MANAGEMENT I/O DEVICE ADDRESSES ARE IN PHYSICAL MEMORY AT 760 000 THRU 777 777. THEY ARE ONLY AVAILABLE TO A PROGRAM IF SOME VIRTUAL ADDRESS AREA IS MAPPED INTO THIS PHYSICAL AREA]

JUMPERS AND MODIFICATIONS

BR LEVEL SELECT BOARD - M7837
BR PLUG SHOULD BE 5400778 (LEVEL #5)
(AS SUPPLIED STANDARD)

REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV
BASIC ASSY DV11	D	UA	DV11-0-0	C
SCALE —	SHEET 8 OF 9	DIST.		

MK

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VIEW FROM SLOT SIDE

NOTES:

1. IF END OF BUS REPLACE M920 WITH M930.
2. IF LAST UNIT IN BASIC BOX REPLACE M920 WITH BC11A CABLE END WHEN EXPANDING TO PHERIPHERAL BOX.
3. IF FIRST UNIT IN EXPANDER BOX REPLACE M920 WITH BC11A CABLE END.
4. TWO LINE CARDS ITEM #22 OR #27 ARE LOCATED IN SLOTS 5 & 6 FOR THE FIRST LINE CARD VARIATION: FOR THE SECOND LINE CARD VARIATION LOCATE TWO MORE LINE CARDS IN SLOTS 7 & 8.
5. M7147 IS USED ON REVISION B OR LATER TO CURE FALSE REPORTING OF TRANSITIONS ON MODEM CONTROL LINES.

F	E	D	C	B	A	
M7147 OR M7808 MODEM CONTROL SCAN AND MUX (NOTE #5)				M920 UNIBUS CONNECTOR NOTE #1 & #2		9
M7833 ASYNC MUX LINE CARD OR M7839 SYNC MUX LINE CARD LINES 12-15						8
M7833 ASYNC MUX LINE CARD OR M7839 SYNC MUX LINE CARD LINES 8-11						7
M7833 ASYNC MUX LINE CARD OR M7839 SYNC MUX LINE CARD LINES 4-7						6
M7833 ASYNC MUX LINE CARD OR M7839 SYNC MUX LINE CARD LINES 0-3						5
M7838 ROM RAM AND BRANCH						4
M7837 UNIBUS DATA AND NPR CONTROL						3
M7836 ALU AND TRANSFER BUS						2
M7807 BUS CONTROL AND MUX				M920 UNIBUS CONNECTOR (NOTE #3)		1
F	E	D	C	B	A	

22,27 SEE NOTE #4 (9)
22,27 SEE NOTE #4 (8)
22,27 SEE NOTE #4 (7)
22,27 SEE NOTE #4 (6)
21 (5)
20 (4)
19 (3)
18 (C)
17 (A)

REVISIONS		
CHR.	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
BASIC ASSY DV11	D	UA	DV11-0-0	C
SCALE	SHEET 9 OF 9	DIST.	MK	

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DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

ENGINEERING SPECIFICATION

DATE May 17,1974

TITLE DV11 Communications Multiplexor

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	ECO CHANGE	00001	J.McNAMARA	5-75		5/14/75
B	ECO CHANGE	00004	W.SMITH	4-76		5/28/76

ENG	APPD	SIZE	CODE	NUMBER	REV
5-23-74	5-23-74	A	SP	DV11-0-1	B

General Description

The DV11 is a sixteen line multiplexor for the PDP-11 family of computers.

The DV11 is designed to achieve very high throughput (16 lines times 1200 characters per second times two directions equals 38,400 characters per second in DDCMP mode, 26,000 characters per second in character oriented protocols) by the use of NPR transfers on both transmission and reception. The use of control bytes stored in core tables makes the DV11 essentially a classical state machine and permits it to achieve hardware throughput capabilities without committing the hardware design to any specific protocol.

The DV11 is housed in a nine slot double system unit and includes a distribution panel for each eight line group and a complete sixteen line modem control similar to the DM11-BB modem control.

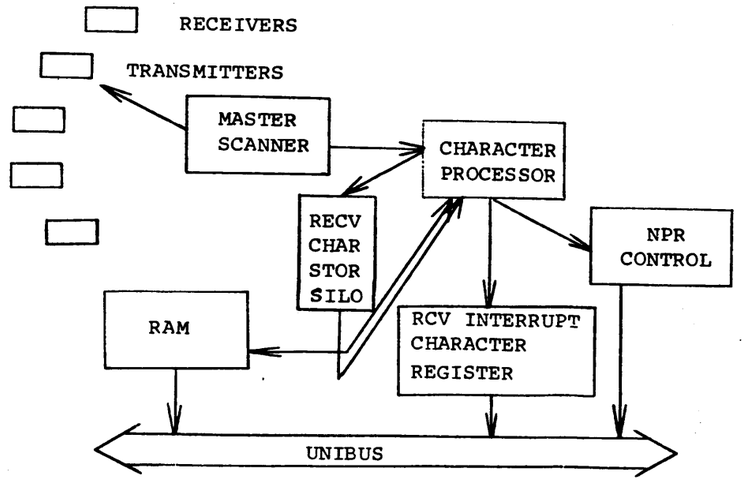


Figure 1: Block Diagram of DV11

SIZE	CODE	NUMBER	REV
A	SP	DV11-0-1	B

A DV11-AA is the option designation for the DV11 control logic and double system unit. No lines or distribution panels are implemented with this option. Three option designations are provided for ordering the line cards in eight line groups. Each group contains a distribution panel in addition to the selection type of line cards. Line cards for eight synchronous lines are designated a DV11-BA option. Line cards for eight asynchronous lines are designated a DV11-BB option. For four synchronous, four asynchronous line card mixture, DV11-BC is the option designation.

The basic elements of the DV11 are shown in figure 1.

The Receivers (16) assemble characters received from serial communications lines and assert a flag as each character is received. The Transmitters (16) disassemble characters and transmit them on serial communications lines and assert a flag whenever they can accept another character for transmission.

The Master Scanner sequentially checks the Receivers and Transmitters for each line to see if flags exist.

The Character Processor is a ROM controlled microprocessor which handles all characters received or transmitted by the DV11. It controls all non-Unibus data transfers and steps the Master Scanner. Except for those occasions where a Unibus instruction or NPR transfer involving the DV11 is taking place, the microprocessor never stops.

The Received Character Storage Silo is a first-in, first-out storage buffer. While most characters received by the DV11 will propagate through this buffer and be directly transferred to PDP-11 core by means of an NPR transfer, the occasion may arise when the attention of the PDP-11 program is required before this is done in the case of a particular character. To prevent the Receivers from experiencing data overruns during the interval that the DV11 is awaiting program attention, the microprogram will continue to load the received characters into the first-in first-out buffer, but the action of the Character Processor in withdrawing characters from the buffer will cease until the PDP-11 program responds to the interrupt caused by the special character at the bottom of the silo buffer.

The character which requires PDP-11 program attention is copied into the Next Received Character Register at the time the aforementioned interrupt is generated.

The RCV Interrupt Character Register is a Unibus addressable register used by the microprogram to show the PDP-11 program any received character, along with line number and error flags, for which the microprogram requires assistance in processing.

The NPR Control is the hardware which the microprogram uses to gain control of the Unibus in order to store received characters, obtain characters for transmission, and obtain control bytes that direct the character processing.

The RAM contains the current addresses and byte counts used in the aforementioned NPR transfers. The initial values are loaded by the PDP-11 program via the Unibus and these values are subsequently updated by the microprogram. The RAM also contains a line protocol byte for each line by which the PDP-11 program can specify what action is to be taken when the byte count reaches zero and what type of block check polynomial should be used. In addition, a line state byte is stored for each line providing a snapshot of what microprogram activity is in progress on a particular line.

Operation

The Master Scanner checks both Receivers and Transmitters for flags indicating that characters are to be read from them (receivers) or loaded into them (transmitters).

If the Master Scanner finds a receiver flag, the microprocessor performs a data transfer operation reading a character from that Receiver and loading it into the Received Character Storage Silo.

If the Master Scanner finds a transmitter flag, the microprocessor utilizes the NPR Control to obtain a character from core and to obtain a control byte from core. The control byte contains information regarding any special treatment the character is to receive during transmission.

After any such treatment, the microprocessor loads that character into that Transmitter for transmission.

In addition to servicing Receiver flags and Transmitter flags, the microprocessor also retrieves characters from the Received Character Storage Silo. As removed from the character storage silo, each character is accompanied by its line number and error flags.

If any of the error flags are set, the microprocessor places the character in the Receiver Interrupt Character Register and generates an interrupt. If there are no error flags set, the microprocessor appends "Mode bits*" to the high order end of the character and uses the resultant expanded character as an offset in a core table from which a control byte appropriate to that character and mode is retrieved. The control byte indicates whether or not an interrupt should be generated (i.e., special character), whether or not the character should be included in the block check character calculation, whether or not the character should be stored in the core message table for that line, and whether or not the "Mode bits" for that line should be changed. In those cases where the microprocessor deposits a character in the Receiver Interrupt Character Register (either because of error flags or as a result of information in the control byte), no further action** is taken by the microprocessor in retrieving characters from the Received Character Storage Silo until so directed by the setting of System Control Register bit Ø8 - Receiver Interrupt Response Complete.

The details of DV11 operation are best understood by reference to the register bit explanations which follow on sheets 6 to 36. Most bits are the same for synchronous and asynchronous applications, but where they differ, notes refer the reader to the appropriate information on sheets 37 to 44.

*Mode bits are always loaded into bits Ø8, Ø9, and 1Ø. Thus, the core tables containing the mode bytes always contain 256 bytes for each mode - i.e., all received characters are treated as 8-bit characters.
**If the program is too tardy in servicing the Receiver Interrupt Character Register, the silo will overflow - See System Control Register (address XØØ) bit 14.

System Control Register - Address XØØ

The System Control Register is a byte addressable register. The bit assignment is as follows:

Bit	Description
ØØ	Microprocessor GO This bit when set permits the DV11 to cycle the Microprocessor that controls the DV11. This is read/write, CLEARED by Initialize. System programs must set this bit for the DV11 to function.
Ø1	ROM Single Step (For Maintenance Use) This bit permits the PDP-11 program to execute one ROM cycle (only). This bit is read/write, cleared by Initialize. When the ROM cycle begins, this bit is automatically cleared.
Ø2	ROM Branch Disable (For Maintenance Use) This bit when set assures that the DV11 microcode will not branch if the ROM cycles to a branch instruction while this bit is set. This bit is read/write, cleared by Initialize.
Ø3	ROM Data Source Select (For Maintenance Use) This bit when set enables the ROM Data Register (a microprocessor register) to be loaded from the Unibus by doing a write into the Special Functions Register (address X12). This bit is read/write, cleared by Initialize.
Ø4-Ø5	Memory Extension The information stored in these bits becomes bits 16 and 17 respectively of any current address or control table base address loaded by the program into the RAM. These bits are read/write (cleared by Initialize) but when read, represent only the status of bits 4 and 5 of the System Control Register, not the status of address bits 16 and 17 of the selected line. See the Line Control Register for further information. This arrangement permits interrupt service routines to save the contents of the System Control Register accurately.

Ø6 Receiver Interrupt Enable

This bit, when set, permits the setting of bit 7 to generate an interrupt request. RW Init. clears.

Ø7 Receiver Interrupt (Vector A)

This bit, when set, indicates that the microprocessor has either (1) withdrawn a byte from a core control table indicating that an interrupt should be generated for the character presently being processed, or (2) the character presently being processed has one or more of its associated error flags set or (3) experienced a zero byte count, non-existant memory location, or memory parity error in processing this characater. The program should respond to this interrupt by setting SCRØ8. (The program might wish to alter the Control Byte Storage Register before setting SCRØ8.) This bit is read only except when SCRØ9 is set. It is cleared by Initialize.

Ø8 Receiver Interrupt Response

The setting of this bit clears SCRØ7 and allows the microprocessor to take action on the character in the RICR (according to the information stored in the Receiver Control Byte Storage Register) and to continue removing characters from the receive silo for processing.

Ø9 Bit 7 & 15 Write Enable (Maintenance)

This bit, when set, permits the program to write bits 7 and 15 of this register. This bit is read/write, cleared by Initialize. This register must be word addressed when and while this bit (SCRØ9) is set.

1Ø NPR Status Overflow Interrupt

This bit, when set, indicates that the DV11 hardware checked the NPR status register (a silo) and found that there was no room due to insufficient program attention to servicing this register. All DV11 transmitter action in performing NPR trasnfers will cease until this condition is corrected. This bit is read/write, cleared by Initialize.

11 Master Clear

This bit, when set, generates "Initialize" within the DV11 data handling sections (It does not affect the modem control.). The silos (both received character and NPR status*) are cleared. The secondary registers are not cleared. This bit is read/write and is self-clearing.

12 Storage Interrupt Enable

This bit, when set, permits the setting of bit 1Ø to generate an interrupt request. Read/write, cleared by Initialize.

13 NPR Status Interrupt Enable

This bit, when set, permits the setting of bit 15 to generate an interrupt request. This bit is read/write, cleared by Initialize.

14 Unused

15 NPR Status Interrupt (Vector B)

This bit is set whenever there is one or more entries in the NPR Status Register, which is a silo-type register. The reading of that read-once register clears this bit, but it resets again if a new entry moves down into the register to replace the previously read entry. This bit is read only except when **SCRØ9** is set, when it is read/write. This bit is cleared by Initialize

*The NPR Status Register Bit 15 ("Entry Present") is cleared by Initialize; the other bits are not.

Receiver Interrupt Character Register - Address XØ2

This register is read only, cleared by Initialize.

Bits	Description
ØØ-Ø7	Interrupting Character These bits contain the interrupting character, right justified. The least significant bit is bit ØØ. On parity-equipped characters, less than 8 bits, the parity bit will appear immediately to the left of the highest order bit in the character. See special note associated with Error Code 0101 below.
Ø8-11	Line Number The bits indicate the line number on which the interrupting character was received. Bit 8 is the least significant bit.
12-15	Error Code These bits indicate the reason that the character shown in bits ØØ-Ø7 generated an interrupt request. Refer to Chart.

Error Code Bit				Meaning
15	14	13	12	
0	0	0	0	SPECIAL CHARACTER The receipt of this character caused the seizure of a control byte which had bit ØØ (generate interrupt) set indicating that this is a special character.
0	0	0	1	PARITY ERROR This character was received with a parity sense opposite to that selected for this line by the parity sense switches on the line card.
0	0	1	0	OVERRUN The character(s) preceding this character on this line has (have) been lost due to failure of the DV11 receiver system to keep up with the incoming character rate on this line.

Error Code Bit				Meaning
15	14	13	12	
0	0	1	1	PARITY ERROR AND OVERRUN (SEE PREVIOUS LISTINGS) (FOR ASYNCHRONOUS USE, SEE SHEETS 42 & 43)
0	1	0	0	BYTE COUNT WARNING This character has been stored, but it is the last character that can be stored for this line as the byte count is now zero for reception on this line.
0	1	0	1	BLOCK CHECK COMPLETED A block of text or data and the associated block check characters have been received and the program should now check the accumulated receiver block check; the DV11 presents the OR of the high and low bytes of that register in bits ØØ-Ø7 of this register.
0	1	1	0	UNDEFINED
0	1	1	1	UNDEFINED
1	0	0	0	BYTE COUNT ZERO This character was not stored, as the byte count for reception on this line is zero and thus there is no place to store this character.
1	0	0	1	UNDEFINED
1	0	1	0	UNDEFINED
1	0	1	1	UNDEFINED
1	1	0	0	PROCESSING ERROR ØØ A nonexistant memory time-out occurred when the DV11 attempted to store this character.
1	1	0	1	PROCESSING ERROR Ø1 A nonexistent memory time-out occurred when the DV11 attempted to obtain the control byte associated with this character.
1	1	1	0	PROCESSING ERROR 1Ø A memory parity error occurred when the DV11 attempted to store this character. (NOTE: this error should never occur, as the memory parity logic gives alarms only on DATO transfers).
1	1	1	1	PROCESSING ERROR 11 A memory parity error occurred when the DV11 attempted to obtain the control byte associated with this character.

In response to a receiver interrupt (SCRØ7), the PDP-11 Program should examine this register (Receiver Interrupt Character Register), make any desired changes in the Receiver Control Byte Storage Register, and then set SCRØ8.

Note: Line Control Register bit definitions for synchronous lines are shown on sheets 11 to 15. Line Control Register bit definitions for asynchronous lines are shown on sheets 38 to 42.

Line Control Register - Address Ø4

This register controls the maintenance features associated with each line in the DV11 and provides an opportunity for the PDP-11 program to read the extended address bits for each line.

The following bits are read only and may be read only after the appropriate bits in the Secondary Register Selection Register have been conditioned to select the appropriate secondary register for the appropriate line: Ø4, Ø5, and Ø7.

The following bits are read/write, but the read is only a read of the most recently written entry into this bit of this register, not a read of the status of this bit for this line (This is referred to as "write/limited read".). A write into one of these bits does not affect the selected line unless bit 15 is also set: Ø8, Ø9, 1Ø, 11, 12, 13, and 14. An example will clarify this. The PDP-11 program can read and write LPR 13 (Receiver Enable) at any time, but reading will only tell the program whether or not LPR 13 is set, not whether or not a particular line's receiver is enabled or not. In addition, the line specified in Secondary Register Selection Register bits ØØ-Ø3 will not be placed in Receiver Enable mode merely by the writing of bit 13 of the LPR. Rather, the line will be placed in Receiver Enable mode only when bit 15 is set in addition (or subsequent to) bit 13 being set.

The line number to which the maintenance information, search sync, or extended address applies is specified by bits ØØ-Ø3 of the Secondary Register Selection Register.

The bit functional assignments are as follows:

ØØ-Ø1 Reserved for Maintenance
(Caution: Various bits may appear here during normal DV11 operation.)

Ø2-Ø3 Unused

Ø4-Ø5 Extended Address Read (Read Only)

For the line number entered in bits ØØ-Ø3 of the Secondary Register Selection Register these bits represent the status of bits 16 and 17 of the secondary register specified by bits Ø8-11 of the Secondary Register Selection Register. This permits the PDP-11 program to read the Extended Address bits of the Current Address and Control Table Base Address entries in the RAM.

Ø6 Unused

Ø7 Maintenance Bit Window (Maintenance)

When in the maintenance mode Ø1 only, this bit can be used to monitor the input to the receiver logic of the selected line. The stimulus that creates the input could be either the maintenance Data bit or the serial output of the transmitter, depending on the state of the Transmitter Disable bit. Program read only. This bit does not represent the status of the selected line.

Ø8 Maintenance Clock Pulse (Maintenance) (See Bit 15)

This bit is used to simulate the Transmitter and Receiver Clock. It is used for diagnostic purposes only. With this bit, the diagnostic has the ability to single step the interface. Setting this bit causes the transmitter to transfer a bit from the internal shift register to the output of the transmitter and causes the receiver to transfer the input of the receiver into the internal shift register.

This bit is program write only and is self-clearing. It pulses all DV11 lines that are in maintenance mode Ø1.

Ø9 Transmitter Disable (Maintenance) (See Bit 15)

This bit, when set, disables the output of this line's Synchronous Transmitter. In this way data from the Maintenance Data bit may be entered into the receiver. This bit is used only for maintenance purposes and is write/limited read.

11 & 12 Maintenance Mode Select (See Bit 15)

These bits are used to select any one of the three maintenance modes:

	BIT 12	SETTING 11
1. Internal Maintenance Mode	0	1
2. External Maintenance Mode	1	0
3. Internal Maintenance Mode for Systems Testing	1	1
4. Normal Operation	0	0

Internal Maintenance Mode (Ø1)

Internal Maintenance Mode clocking comes from the Maintenance Clock Pulse bit (bit Ø8) driven via the program. While using this mode, the following EIA level converters are disabled (This is done so that the majority of the logic can be diagnosed without disconnecting the modem cable.):

Receiver Clock
Transmitter Clock
Receiver Data
Transmitter Data

Transmitted data is looped to received data on a TTL basis.

External Maintenance Mode (1Ø)

When in the external maintenance mode, all lines connected to the data set must be removed at the data set interface. A special connector replaces the connector of the data set. The function of the special connector is to turn around specified signals after level conversion and bring them back to the DV11 as simulated inputs.

Clocking in this mode is under control of internal DV11 clocks in the same way as Internal Maintenance Mode 11.

Internal Maintenance Mode for Systems Testing (11)

With bits 12 and 11 both set to a one (mode 11), the internal maintenance mode provides internal clocking for the receiver and transmitter. The clocking rate is controlled by switches on the DV11 line cards. Mode 11 will be the same as mode Ø1 with respect to data set control leads and TTL data loopback. The only difference is that in mode 11 the receiver and transmitter clocking is derived from internal clocks.

Bits 11 and 12 are write/limited read.

NOTE: If bits 12 and 11 are zero, normal operating mode is assumed.

13 Receiver Enable (See bit 15)

When this bit is set by the program, a sync search is initiated on this line by the receiver logic. After an initialize, this bit must be set by the program before any reception can begin on this line - i.e., Receiver Active (See "Line State" secondary register) will not set unless this bit has been set.

A switch for each line determines whether the receiver searches for one sync character or for two in a row.

A successful sync search results in the setting of Receiver Active (Line State Bit ØØ) for this line.

This bit is write/limited read.

NOTE: Should it be desired to resynchronize during the course of reception, the program could accomplish this by setting "Receiver Resynchronize" (Line State Ø1). To shut down reception on a line, the program should clear Receiver Enable and then set Receiver Resynchronize.

14 Maintenance Data (Maintenance) (See Bit 15)

This bit is used only in the maintenance mode by the diagnostic program. In maintenance mode Ø1 this bit can be used to simulate data at the receiver input. When used as a simulated input to the receiver, the Transmitter Disable bit must be set to inhibit additional input from the transmitter. This bit should be cleared if it is not being used as the simulated input. If this bit were inadvertently set in maintenance mode and the transmitter Disable bit was clear, the receiver input would have two sources of input. This bit is write/limited read.

15 Maintenance Conditions Strobe (Maintenance)

The setting of this bit records the status of bits Ø8, Ø9, 1Ø, 11, 12, 13, and 14 into the status flip-flops associated with the line specified in bits ØØ-Ø3 of the Secondary Register Selection Register. This bit is self-clearing, hence write only. It may be set at the same time as the bits whose status it records, as its action is delayed until the conclusion of the instruction cycle which set it. This bit is necessary due to "Reads" in the PDP-11/20 being "read-write" cycles, and certain synchronization requirements associated with mode changes during clocking pulses.

CAUTION: After setting this bit, do not change bits ØØ-Ø3 of Secondary Register Selection Register until this bit has self cleared indicating conclusion of the strobe operation.

Secondary Register Selector - Address XØ6

The bits in this register provide a path for the program to access the various locations in the DV11 RAM. The program may read or write these locations. The various locations may be thought of as registers.

Interrupt service routines must save the contents of this register so that no changes occur between the setting of bits in this register and the reading or writing of the Secondary Register Access Register - Address X1Ø.

The bit assignments of the Secondary Register Selector Register are as follows:

Bit	Description
ØØ-Ø3	Line Selection For each type of register selected by bits Ø8-11, there are 16 registers - one per line. The setting of the Line Selection bits determines exactly which of these line registers is to be addressed.
Ø4-Ø7	Unused
Ø8-11	Register Selection These bits determine which type of register is addressed for the line number specified in bits ØØ-Ø3.

Bits

11	10	9	8	
0	0	0	0	Transmitter Primary Current Address
0	0	0	1	Transmitter Primary Byte Count
0	0	1	0	Transmitter Secondary Current Address
0	0	1	1	Transmitter Secondary Byte Count
0	1	0	0	Receiver Current Address
0	1	0	1	Receiver Byte Count
0	1	1	0	Transmitter Accumulated Block Check
0	1	1	1	Receiver Accumulated Block Check
1	0	0	0	Transmit Control Table Base Address

Bits

11	10	9	8	
1	0	0	1	Receiver Control Table Base Address
1	0	1	0	Line Protocol Parameters
1	0	1	1	Line State
1	1	0	0	Transmitter Mode Bits
1	1	0	1	Receiver Mode Bits
1	1	1	0	Line Progress
1	1	1	1	Receiver Control Byte Storage Register

Secondary Registers

These registers are selected by conditioning bits in the Secondary Register Selector Register (Address XØ6) and then reading or writing into the Secondary Register Access Register (Address X1Ø).

NOTE: The Secondary Registers are NOT cleared by Initialize.

0000 Transmitter Principal Current Address

The Transmitter Principal Current Address secondary register contains the 18-bit core memory address of the next character to be transmitted on the associated line. The extended address bits are initially loaded from SCR 04-05 to provide the 18-bit address capability. This register is incremented by one with each character transmitted on the associated line by the DV11 if the principal message table is being used (Line State secondary register bit 07 set to zero).

0001 Transmitter Principal Byte Count

The transmitter Principal Byte Count secondary register contains a 15-bit word that is the two's complement of the number of bytes (characters) remaining to be transmitted on the associated line. The 16th bit (bit 15) is used by the PDP-11 program to enable change of mode and/or BCC transmission based on reaching a zero byte count during transmisssion. When bit 15 is set to zero by the PDP-11 program, bits 13-15 of the Line Progress secondary register for this line will control the trans-

mission mode when the principal byte count reaches zero; also, the BCC will be transmitted if Line Progress bit 10 is set to one. When bit 15 is set to one by the PDP-11 program, bits 00-02 of the Transmitter Mode Bits secondary register continue to control the line transmission mode. A byte count with bit 15 set to zero (at the time the byte count is loaded by the PDP-11 program) is referred to as a "marked" byte count.

This register is incremented by one with each character transmitted on the associated line by the DV11 if the principal message table is being used (Line State 07 set to zero). When this register reaches zero, transmission continues using the transmitter alternate byte count for this line, if the Transmitter Go bit in the Line State secondary register is still set to one.

0010 Transmitter Alternate Current Address

The Transmitter Alternate Current Address register has exactly the same function as the Transmitter Principal Current Address register (0000). This register is incremented by one with each character transmitted by the DV11 on the associated line if the alternate message table is being used (line State secondary register bit 07 set to one).

0011 Transmitter Alternate Byte Count

The transmitter Alternate Byte Count secondary register contains a 15-bit word that is the two's complement of the number of bytes (characters) remaining to be transmitted on the associated line. The 16th bit (bit 15) is used by the PDP-11 program to enable change of mode and/or BCC transmission based on reaching a zero byte count during transmission in the same fashion as described for Transmitter Principal Byte Count.

This register is incremented by one with each character transmitted on the associated line by the DV11 if the alternate message table is being used (line State secondary register bit 07 set to one). When this register reaches zero, transmission continues using the

transmitter principal byte count for this line if the Transmitter Go bit in the Line State secondary register is still set to one.

0100 Receiver Current Address

The Receiver Current Address register contains the 18-bit core memory address for storage of the next character to be received on the associated line. The extended address bits are initially loaded from SCR 04-05 to provide the 18-bit address capability. This register is incremented by one with each character received on the associated line by the DV11.

0101 Receiver Byte Count

The Receiver Byte Count secondary register contains a 15-bit word that is the two's complement of the number of bytes (characters) remaining to be received on the associated line. The 16th bit (bit 15) is used by the PDP-11 program to enable change of mode and/or BCC anticipation based on reaching a zero byte count during reception. When bit 15 is set to zero by the PDP-11 program, bits 13-15 of the Line State secondary register for this line will control the reception mode when the byte count reaches zero; also, the BCC will be expected if Line State bit 10 is set to one. When bit 15 is set to one by the PDP-11 program, bits 00-02 of the Receiver Mode Bits secondary register continue to control the line reception mode. When this register reaches zero, an interrupt code is set in the Receiver Interrupt Character register and the DV11 stops transferring received characters to core memory.

0110 Transmitter Accumulated Block Check Character

The Transmitter Accumulated Block Check secondary register contains the continuously computed block check character specified by the Line Protocol Parameters secondary register to enable destination stations to check integrity of transmission on the associated line. Characters to be included in the

block check calculation are specified by bit 03 of the transmitter control bytes for each character. The contents of this register are transmitted as two sequential bytes, low-order eight bits first, except when LRC-8 is the selected block check type, in which case a single byte is transmitted. The DV11 automatically clears this register to zero after transmitting its contents.

NOTE

The DV11 computes CRC-16 and CRC-CCITT on a byte at a time basis (parallel), thus the character length must be eight bits. LRC-8 may be selected for characters of 5, 6, 7, or 8 bits.

0111 Receiver Accumulated Block Check Character

The Receiver Accumulated Block Check secondary register contains the continuously computed block check character specified by the Line Protocol Parameters secondary register for checking integrity of data received on the associated line. Characters to be included in the block check calculation are specified by bit 03 of the receiver control byte for that character. The PDP-11 program should clear this register if the accumulated block check at the end of the message is non-zero.

1000 Transmitter Control Table Base Address

The transmitter Control Table Base Address secondary register contains the 18-bit address of the transmitter control table for the associated line. The extended address bits are initially loaded from SCR 04-05 to provide the 18-bit address capability. The contents of this register are used by the microprocessor in the computation of the control byte addresses for transmitted characters.

1001 Receiver Control Table Base Address

The Receiver Control Table Base Address secondary register contains the 18-bit address of the receiver control table for the associated line. The extended address bits are initially loaded from SCR 04-05 to provide the 18-bit address capability. The contents of this register are used by the microprocessor in the computation of the control byte addresses for the received characters.

1010 Line Protocol Parameters

The Line Protocol Parameters secondary register contains the transmitter Data Link Escape (DLE) character when required by the associated line protocol, plus control bits to implement protocol requirements and handling of synch characters. The PDP-11 program writes the data in this register for reference by the microprogram. Bit assignments are described in the following table:

LINE PROTOCOL PARAMETERS SECONDARY REGISTER BIT ASSIGNMENTS

Bit(s)	Designation
00	Idle Mark if both Byte Counts Zero
01	Strip Leading Syncs
02	Unused
03-04	Block Check Type
05	DDCMP Receive
06	DDCMP Transmit
07	Unused
08-15	DLE Character

Block Check Type

03	04	BCC Type
0	0	LRC-8 (XOR)
1	0	CRC-16 ($X^{16}+X^{15}+X^{2}+1$)
0	1	Unused-16
1	1	CRC-CCITT ($X^{16}+X^{12}+X^{5}+1$)

1011 Line State

The Line State secondary register is used by the PDP-11 program and the microprocessor to control and monitor line activities in executing the selected protocol. This register is also used by the PDP-11 program to store mode change and BCC anticipation bits for reference by the microprocessor when a marked receiver byte count reaches zero.

LINE STATE SECONDARY REGISTER BIT ASSIGNMENTS

Bit(s)	Designation	Read/Write
00	Receiver Active	Read
01	Receiver Resynchronize	Write
02	Transmitter Go	Read or Write
03	Transmitter Underrun	Read or Write zero
04	Transmitter Non-existant Memory (NXM)	
05	Transmitter Memory Parity Error	
06	Sync Strip On	
07	Use Alternate Tables	
08-09	Unused	
10	Expect BCC	
11-12	Unused	
13-15	Next Receive Mode on Marked Byte Count = 0	

1100 Transmitter Mode Bits

The Transmitter Mode Bits secondary register contain the 3-bit mode selection field (in bits 00-02) which determines the transmitter control table to be used for controlling transmission on the associated line.

1101 Receiver Mode Bits

The Receiver Mode Bits secondary register contains the 3-bit mode selection field (in bits 00-02) which determines the receiver control table to be used for controlling reception on the associated line.

1110 Line Progress

The Line Progress secondary register contains bits set and referenced by the microprocessor to control and monitor activities on the associated line in executing the selected protocol (these bits are not intended for access by the PDP-11 program). This register also stores mode change and BCC transmission control bits, as set by the PDP-11 program, for use by the microprocessor when a marked transmitter byte count reaches zero.

LINE PROGRESS SECONDARY REGISTER BIT ASSIGNMENTS

Bit(s)	Designation
00	Send BCC1 Next
01	Send BCC2 Next
02	DLE Sending In Progress
03-04	Unused
05	Expect BCC1
06	Expect BCC2 Next

07	Resynchronization Flag Expected
08-09	Unused
10	Send BCC
11-12	Unused
13-15	Next Transmit Mode on Marked Byte Count = 0

1111 Receiver Control Byte Holding

The Receiver Control Byte Holding secondary register provides a location for the microprocessor to store the Receiver Control Byte in bits 00-07 during character processing. The PDP-11 program may set a control byte into this register while responding to a DV11 receiver special character interrupt. When the PDP-11 program signals the DV11 that its interrupt response is complete (SCR 08=1), the microprocessor uses the control byte in this register to control the disposition of the interrupting character in the Receiver Interrupt Character register.

The microprocessor may also use this register to write control bytes that specify character discard only, if an error condition or data block boundary condition caused the interrupt; the existing mode specified in the control byte is not altered. The PDP-11 program should not write this register except during initialization or interrupt response cycles.

Special Functions Register - Address X12

Reserved for maintenance. Various bits may appear here during normal operations. Word addressable.

NPR Status Register - Address X14

This register is a silo-type register in that it is read once, in that a new entry "falls" into the register if there are additional "entries" existing at the time that the read of this register is completed. This register is read only.

This register reports various interrupt-causing conditions associated with the transmitter NPR hardware. Interrupt conditions related to various transmitter NPR operations are stacked up in a first-in first-out storage buffer along with the line number being serviced when this condition occurred. As soon as the program has finished reading this register once, a new entry is cycled into the register in place of the former entry. The interrupt is SCR 15 (NPR Status Interrupt). This register is read only, not cleared by Initialize, except for bit 15 which is cleared by initialize.

Bits	Description
ØØ-Ø3	Line Number These bits indicate which line was being serviced when the interrupt condition developed. The format of these bits is the same as bits ØØ-Ø3 of the Secondary Register Selection Register (SRSR) so that the program can load these bits into the SRSR and read the appropriate current address of byte count.
Ø4-Ø7	Unused
Ø8-11	These bits indicate the type of interrupt condition which occurred. The hardware is designed so that simultaneous occurrences on the same line create separate entries (Example: non-existant memory and byte count zero both occur). NOTE that the condition codes are the addresses of the secondary registers which apply.

Code	Condition
ØØØØ	Transmitter Principal Current Address sent NPR hardware to a non-existant memory location (NXM).
ØØØ1	Transmitter Principal Byte Count = Ø.
ØØ1Ø	Transmitter Alternate Current Address sent NPR hardware to a non-existant memory location.
ØØ11	Transmitter Alternate Byte Count = Ø.
1ØØØ	Transmitter Control Table Base Address - fetching control byte produced NXM or a memory parity error, The program should examine the Line State secondary register for further details.
12-14	Unused
15	Entry Present When set, this bit indicates that bits ØØ-11 contain a valid entry. Reading the register or generating initialize clears this bit. It re-sets when another status report entry reaches the "bottom" of the silo and can be read in bits ØØ-11. Bits ØØ-11 are meaningless unless this bit (15) is set.

Reserved Register - Address X16

Bits	Function
ØØ-15	Reserved - word addressable

CONTROL BYTE FORMATS

The DV11 achieves its high througput and generalized operating capabilities by having both the transmitter and the receiver character handling apparatus perform NPR cycles to control byte tables in PDP-11 core to determine the next step to take with regard to the particular character being processed. The bit assignments in the control bytes are arranged such that the same control bytes may be used for both transmission and reception if the communications protocol being used progresses from

mode to mode in a symmetrical fashion on both transmit and receive and provided that the same characters would be included in the Block Check Character in both transmission and reception.

BITS	TRANSMITTER CONTROL BYTE FUNCTION	RECEIVER CONTROL BYTE FUNCTION
Ø5-Ø7	NEXT MODE Determines next transmission mode used on this line.	NEXT MODE Determines next reception mode used on this line
Ø4	RESERVED	STORE/DISCARD Determines whether this character is stored in message table or is discarded.
Ø3	INCLUDE IN BCC YES/NO Determines whether or not this character will be included in the BCC being accumulated for this line.	INCLUDE IN BCC YES/NO Determines whether or not this character will be included in the BCC being accumulated for this line.
Ø2	SEND BCC NEXT Tells Transmitter Logic to send the 16-bit BCC after the character presently being handled. (8-bit if LRC selected)	EXPECT BCC NEXT Tells receiver logic to expect the 16-bit BCC after the character presently being handled. (8-bit if LRC selected)
Ø1	SEND DATA LINK ESCAPE NEXT Tells transmitter logic to send Data Link Escape character from Secondary Register 1Ø1Ø before sending the character presently being handled. (8-bit if LRC selected).	RESERVED

ØØ	RESERVED	GENERATE AN INTERRUPT The setting of this bit causes the character presently being processed to generate an interrupt. The microprocessor moves that character to the Receiver Interrupt Character Register and generates an interrupt request.

SPECIFICATIONS

SYSTEM ADDRESSES

The DV11 uses the same address space as the DM11-A. The first DV11 in a system would be at 775ØØØ; the next at 775Ø4Ø; then 7751ØØ; and finally, 7751 4Ø. If there are DM11-A's in the system already, the first DV11 would be at 775Ø4Ø. The DV11 data handling and modem control use a total of ten registers.

INTERRUPT VECTORS

The DV11 requires three interrupt vectors - two for the data handling section and one for the modem control. The interrupt vectors are in the floating vector space that starts at 3ØØ. The DV11 modem control follows the DM11-BB which follows the DN11. The DV11 data handling section follows the DUP11 which in turn follows the DU11.

TIMING CONSIDERATIONS

The modem control timing considerations consist of scan control and CLR SCAN operations. Scan control through the CSR allows the scan to either run free (SCAN EN) or to be sequentially stepped through the line counter line by line (STEP bit of CSR). The Read/Write cycles of the modem control scan logic force the program to wait, after issuing CLR SCAN, until it has cycled through the memories. Also, the scan's Read/Write cycles prevent halting the scan and changing the line number with one machine cycle.

Programs should not spin on flags in the DV11 secondary registers using loops less than 3Ø (octal) instructions; to do so may interfere with DV11 RAM microprocessor / Unibus access interlocks.

ORDER NUMBERS

DV11-AA	Double System unit contains all DV11 logic except the line cards and distribution panels. No lines are implemented.
DV11-BA	Line cards and distribution panel for eight synchronous lines. Requires 5-1/4 inches of cabinet space. Two DV11-BA's can be used with one DV11-AA. To configure an 8 line synchronous DV11, order 1 DV11-AA and 1 DV11-BA. To configure a 16 line synchronous DV11, order 1 DV11-AA and 2 DV11-BA's.
DV11-BB	Line cards and distribution panel for eight asynchronous lines. Requires 5-1/4 inches of cabinet space. Two DV11-BB's can be used with one DV11-AA. To configure an 8 line asynchronous DV11, order 1 DV11-AA and 1 DV11-BB. To configure a 16 line asynchronous DV11, order 1 DV11-AA and 2 DV11-BB's.
DV11-BC	Line cards and distribution panel for four synchronous and four asynchronous lines. Requires 5-1/4 inches of cabinet space.

BUS LOADS

Two bus loads.

POWER CONSUMPTION

A DV11 system with 16 synchronous lines takes:

17.5 Amps @ +5 Volts
1.Ø Amps @ -15 Volts
Ø.5 Amps @ +15 Volts

A DV11 system with 16 asynchronous lines takes:

2Ø.5 Amps @ +5 Volts
1.Ø Amps @ -15 Volts
Ø.6 Amps @ +15 Volts

A DV11 with 8 synchronous and 8 asynchronous lines takes:

19.Ø Amps @ +5 Volts
1.Ø Amps @ -15 Volts
Ø.55 Amps @ +15 Volts

ENVIRONMENTAL

+10 degrees to +50 degrees C with a relative humidity of 20% to 95%.

SPACE REQUIREMENTS

DV11-AA:	Two system units (SU's).
DV11-BA:	5-1/4 inches of cabinet space (SM PAN).
DV11-BB:	5-1/4 inches of cabinet space (SM PAN).
DV11-BC:	5-1/4 inches of cabinet space (SM PAN).

CABLES

Order BCØ5D-25 modem cables.

PROGRAMMABLE MODEM CONTROL DEVICE REGISTERS

The two programmable modem control device registers and their specific bit assignments are listed in the following paragraphs.

Control Status Register (CSR) (Address: 770XX0)

Bit	Status	Description
03:00	LINE #	The LINE # bits are the binary addresses for the modem control's 16 lines (0-15) as follows:

Bit 3	2	1	0	Line #
0	0	0	0	0
0	0	0	1	1
			:	:
1	1	1	1	15

If the Scan is cleared by INITIALIZE or CLR SCAN, the Line # Register will settle in 16μs ±10%. When settled, the Line # Register will be set to Line #0(0000).

NOTE

When the Scan is enabled (or STEP) the next line to be tested will always be Line # +1. These bits are Read/Write and are cleared by INITIALIZE and by CLR SCAN.

04	BUSY	BUSY provides a program indicator that is set to 1 when the Scan is cycling. This bit is particularly useful to determine when a CLR SCAN (bit 11) has completed the task of cycling 0s into the Scanner's memory elements. In addition, this bit must be tested for 0 if SCAN ENABLE was turned off preparatory to changing the Line #. In Interrupt Mode, this procedure guarantees that detected transitions are serviced before the Line # is changed. (If functioning with interrupts OFF, then DONE should be tested after BUSY is found to be 0.)

Bit	Status	Description
05	SCAN EN	The SCAN ENABLE flip-flop allows the scan to "free run" -- testing all lines sequentially if the DONE flip-flop is cleared. When the SCAN EN flip-flop is set to 1 and DONE is 0, a ring counter is allowed to cycle in the following order (from Rest): a. Increment line counter. b. Store contents of memory (Line # Address) in the HOLD flip-flop. c. Write current modem status into memory. d. Compare HOLD and contents of memory for Interrupt conditions. The ring counter continues to cycle (a to d) if DONE remains 0 and SCAN EN is set. If the SCAN EN flip-flop is negated while the ring counter is cycling (i.e., DONE net set) the ring counter will come to rest in 1.2μs ±10% (MAX). The line #Register must not be changed until BUSY (bit 04) is found to be 0. This bit is Read/Write and cleared by INITIALIZE and CLR SCAN.
06	INTER EN	If set to 1, Interrupt Enable allows DONE to cause an interrupt on priority four (4). This bit is Read/Write and cleared by INITIALIZE and CLR SCAN.
07	DONE	The DONE flag, when set to 1, indicates that the hardware Scan has detected a transition on CARRIER, SEC RX, CS, or the RING Modem Status leads. Additionally, DONE freezes the Scan which makes available to the programmer: a. The Line # that caused the interrupt b. The state of the flags (4 bits) c. Modem status (8 bits)

This bit is Read/Write and cleared by INITIALIZE and CLR SCAN.

08 STEP

STEP, when set to 1, causes the Scan to increment the Line # and test that line for interrupts causing transitions. STEP can be used in place of SCAN EN, but care should be exercised that the Scan rate is great enough (milliseconds) so that double carrier transitions will be detected. Additionally, DONE does not inhibit STEP. A STEP requires 1.2μs $\pm$10% to execute. This bit is Write 1s only.

09 MAINT MODE

When the MAINT MODE flip-flog is set to 1, it conditions the Scan Input (RING, CLEAR TO SEND, CARRIER, and SEC RX) to a 1 or ON state. Utilizing STEP or SCAN EN with MAINT MODE exercises 100 percent of the scan logic (not the data multiplexers). This includes the interrupt circuits (M7821) and the address selector (M105).

This mode provides a diagnostic feature, as well as an on-line test facility for the modem control's interaction with the Unibus. This bit is Read/Write and cleared by INITIALIZE and CLR SCAN.

10 CLEAR MUX

CLEAR MUX clears the REQUEST TO SEND, TERMINAL READY, SEC TX, and LINE EN flip-flops for all lines, when this bit is set to 1. This bit is Write 1s only.

11 CLR SCAN

CLEAR SCAN clears all active functions (Line #, SCAN EN, etc.) and the memory logic, when this bit is set to 1. The memory logic requires 18.8 μs $\pm$10% to cycle a CLEAR through the memory locations. This function is especially useful if the programmer requires knowledge of the ON states of CARRIER, CLEAR TO SEND, RING and SEC RX. When the Scan is enabled (or STEP) following a CLR SCAN, an interrupt will occur for all ON states as they will appear (to the logic) as OFF to ON transitions.

12 DSR *

The DATA SET READY flag is 1 if an ON to OFF or an OFF to ON transition has occurred on this modem lead. This bit is not valid if the program has changed the LINE # and the Scan has not cycled for one or more lines. This bit is Read Only and presents 0 when INITIALIZED or CLR SCAN.

13 CS

The CLEAR TO SEND flag is 1 if an ON to OFF or OFF to ON transition has occurred on this modem lead. This bit is not valid if the program has changed the LINE # and the Scan has not cycled for one or more lines. This bit is Read Only and presents 0 when INITIALIZED or CLR SCAN.

14 CO

The CARRIER flag is 1 if an ON to OFF or OFF to ON transition has occurred on this modem lead. This bit is not valid if the program has changed the LINE # and the Scan has not cycled for one or more lines. This bit is Read Only and presents 0 when INITIALIZED and CLR SCAN.

15 RING

The RING flag is 1 if an OFF to ON transition has occurred on this modem lead. This bit is not valid if the program has changed the LINE # and the Scan has not cycled for one or more lines. This bit is Read Only and presents 0 when INITIALIZED and CLR SCAN.

* FOR ASYNCHRONOUS USE, REFERENCE SHEET 43.

Line Status Register (LSR) (Address: 770XX2)

Bit	Status	Description
00	LINE EN	The LINE ENABLE flip-flop, when asserted, enables RING, CO, CS, and SEC RX to be sampled (line status) by the program, and to be tested for transitions.

This bit is Read/Write and cleared by INITIALIZE and CLEAR MUX.

01 TERM RDY — Controls switching of the data communications equipment to the communication channel (via modem).

Auto-Dial and Manual Call origination: Maintains the established call.

Auto-Answer: Allows "handshaking" in response to a RING signal.

This bit is Read/Write and is cleared by INITIALIZE and CLEAR MUX.

02 RS — When REQUEST TO SEND is set to 1, it conditions the modem for transmit if the communications channel has been established (switched network). This bit is Read/Write and is cleared by INITIALIZE and CLEAR MUX.

03 NS * — The New Sync (201) flip-flop, when 1, presents a high to the New Sync lead. This bit is Read/Write and is cleared by INITIALIZE or CLEAR MUX.

04 DSR * — When the state of the modem's Data Set Ready lead is a high, this bit is a 1. The DSR bit is inhibited when the LINE EN flip-flop is 0. This bit is Read Only.

05 CS — This bit reflects the current state of the modem CLEAR TO SEND lead. An ON indicates that the modem is ready to transmit data. This lead is most often the result of the REQUEST TO SEND lead. The CS bit is inhibited when the LINE EN flip-flop is 0. This bit is Read Only.

* FOR ASYNCHRONOUS USE, REFERENCE SHEET 43.

06 CO — This bit reflects the current state of the modem carrier detect lead. An OFF indicates that the received signal is unsuitable for demodulation. The CO bit is inhibited when the LINE EN flip-flop is 0. This bit is Read Only.

07 RING — This bit reflects the current state of the modem's ring lead. The RING bit is inhibited when the LINE EN flip-flop is 0. This bit is Read Only.

NOTE

The Line Status Register bits 07:04 are inhibited when LINE EN is 0.

System Addresses

The DV11 modem control uses two address locations in the floating address area.

Interrupt Vectors

Each modem control requires one interrupt vector. The vector addresses are assigned upward from 300 to 777. The modem control falls in behind the DV11 in contiguous assignments from 300.

Timing Considerations

The modem control timing considerations consist of scan control and CLR SCAN operations. Scan control through the CSR allows the scan to either run free (SCAN EN) or to be sequentially stepped through the line counter line by line (STEP bit of CSR). The Read/Write cycles of the modem control scan logic (Paragraph 4.4) force the program to wait, after issuing CLR SCAN, until it has cycled through the memories. Also, the scan's Read/Write cycles prevent halting the scan and changing the line number with one machine cycle.

General Description

The DV11 Asynchronous Line Card provides EIA communication capability for the DV11 multiplexor. Each ALC contains four double-buffered serial communication lines (UART'S) that are serviced by the DV11 character processor.

For Asynchronous reception, the UART assembles the serial communication line's character and presents a receiver flag to the character processor. Upon servicing of that receiver flag, the ALC presents the received character and associated error conditions to the character processor's Received Character Storage Silo for future processing. During Asynchronous transmission, the character processor checks the state of the line card's transmit flag to determine the need for servicing. If conditions exist so that transmission is required on that line, the character processor will send a parallel character to the transmitter register file for serial presentation to the communication line.

Each serial communication line of the ALC can operate with with individual programmable parameters.

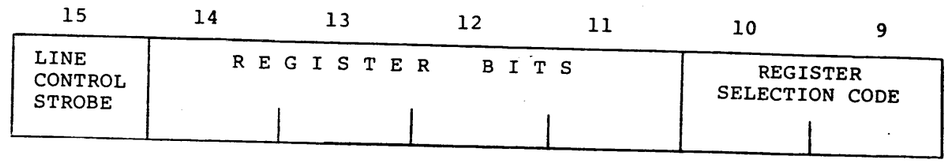
The parameters are:

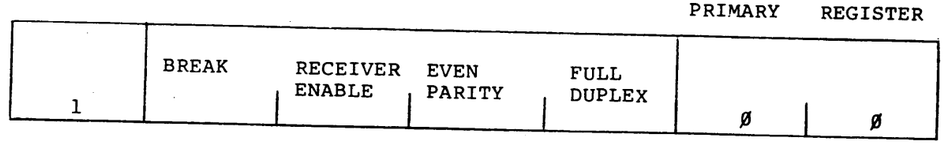
Character length:	5, 6, 7 or 8 bit.
Number of stop bits:	1 or 2 for 5, 6, 7, 8 bit characters.
Parity generation and detection:	Odd, Even or None.
Operating Mode:	Half Duplex or Full Duplex and Receiver Enable.
Transmitter/ Receiver Speed:	50, 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 7200, 9600 and 38,400.
Breaks:	Generaticn and Detection.

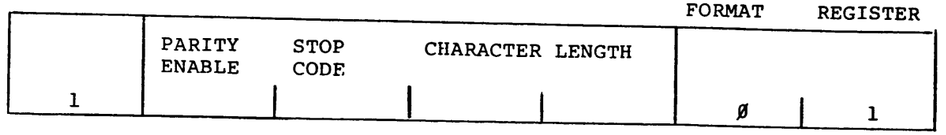
LINE CONTROL REGISTER (LCR) - ADDRESS X04

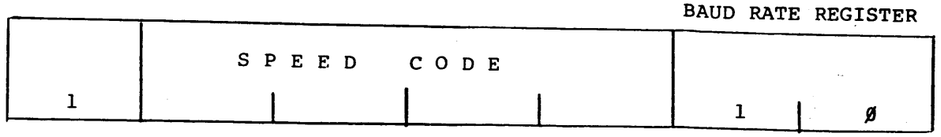
This register controls the features associated with each type of line card. The following LCR bit functions will pertain only to those lines associated with an asynchronous line card. For synchronous line card functions, refer to sheets 9 through 15 of this specification. Bits 00-03 of the Secondary Register Selection Register specify the line numbers to which the bits in the Line Control Register apply.

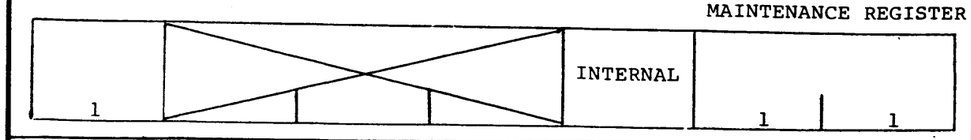
The bit assignments of the asynchronous line card are as follows:











BITS 09-10 REGISTER SELECTION CODE (See bit 15)

Each line has four associated registers that are determined by the states of these bits. These registers are four bits wide and are defined by bits 11 through 14.

Register	Bit Setting 10	9
1. Primary	0	0
2. Format	0	1
3. Baud Rate	1	0
4. Maintenance	1	1

BIT PRIMARY REGISTER

11 (Primary ØØ) Full-Duplex/Half Duplex (See bit 15)

The per line bit, when cleared, conditions the line to operate in full-duplex mode. If this bit is set, the line is conditioned to operate in half-duplex mode, where the selected receiver is blinded during transmission of a character.

12 (Primary ØØ) Even Parity (See bit 15)

This bit, when set, generates character with even parity on the line and expects received characters to have even parity. If this bit is cleared, characters of odd parity are generated on the line and received characters are expected to have odd parity.

The state of this bit is immaterial if the Parity Enable bit (Format Register - Bit 14) is not set. This bit must be conditioned prior to loading of the Format Register.

13 (Primary ØØ) Receiver Enable (See bit 15)

This bit must be set before the receiver logic can assemble characters from the serial input line. When this bit is set, Receiver Active (Line State Bit ØØ) will subsequently set. To shut down reception on a line, the program should first clear Receiver Enable and then set Receiver Resynchronize (Line State Bit Ø1). The program must wait one character interval after shutdown before restarting a line.

14 (Primary ØØ) Break (See bit 15)

This bit, when set, will force a space on that line's output causing a break condition. The break condition may be timed by sending characters during the break interval, since these characters never reach the EIA line.

All primary registers will be cleared following a Bus Initialize or DV11 Master Clear.

BIT FORMAT REGISTER

11-12 (Format Ø1) Character Length (see bit 15)

These bits are set to receive and transmit characters of the length (excluding parity) as shown below.

12	11	
0	0	5 bit
0	1	6 bit
1	0	7 bit
1	1	8 bit

13 (Format Ø1) Two Stop Bits (See bit 15)

This bit, when set, conditions the line transmitting with 5, 6, 7 or 8 bit code to transmit characters having two stop bits. One stop bit is sent when this bit is cleared.

14 (Format Ø1) Parity Enable (See bit 15)

If this bit is set, characters transmitted on the line have an appropriate parity bit affixed; and characters received on the line have their parity checked. Parity sense is determined by the state of Primary Register bit 12.

BIT BAUD RATE

11-14 (Baud Rate 1Ø) Speed Code (See bit 15)

The state of these bits determine the operating speed for the transmitter and receiver of the selected line.

14	13	12	11	Baud Rate
0	0	0	0	50
0	0	0	1	75
0	0	1	0	110
0	0	1	1	134.5
0	1	0	0	150
0	1	0	1	300
0	1	1	0	600
0	1	1	1	1200
1	0	0	0	1800
1	0	0	1	2000
1	0	1	0	2400
1	0	1	1	3600
1	1	0	0	4800
1	1	0	1	7200
1	1	1	0	9600
1	1	1	1	38,400

Refer to DV11 Busy and Data Set Busy features for 38.4K baud operation.

BIT MAINTENANCE

11 (Maintenance 11) Maintenance Internal Mode (See bit 15)

This per line bit, when set, loops the transmitter's serial output lead to the receiver's serial input lead on a TTL basis. While operating in maintenance mode, the EIA transmit data leads, EIA received data leads, and the remote Data Set Busy features are disabled. Normal operating mode is assumed when this bit is cleared. All Maintenance Registers will be cleared following a Bus Initialize or DV11 Master Clear.

12-14 (Maintenance 11) Unused

BIT 15 LINE CONTROL STROBE

The setting of this bit records the status of bits Ø9, 1Ø, 11, 12, 13 and 14 into the registers associated for the line specified in bits ØØ-Ø3 of the Secondary Register Selection Register. This bit is self-clearing, hence write only. It may be set at the same time as the bits whose status it records, as its action is delayed until the conclusion of the instruction cycle which set it.

CAUTION: Reference the CAUTION NOTE located on sheet 15.

RECEIVER INTERRUPT CHARACTER REGISTER - ADDRESS XØ2

The RICR Register is a Unibus Addressable Register used by the microprogram to show the PDP-11 program any received character, along with line number and error flags, for which the microprogram requires assistance in processing.

Three individual error flags from an asynchronous line will be presented in the RICR register in the following manner:

Error Code Bit 15	14	13	12	Meaning
0	0	0	1	Parity Error This character was received with a parity sense opposite to that which was selected for this line.
0	0	1	0	Overrun Error The character(s) preceding this character on this line has (have) been lost due to failure of the DV11 receiver system to keep up with the incoming character rate on this line.
0	0	1	1	Framing Error These bits are set if the received character did not have a stop bit present at the proper time. These bits are usually interpreted as indicating the reception of a break.

Existing error codes not shown above are the same for both the synchronous and asynchronous line cards.

A priority encoding scheme is used by an asynchronous line to present a multiple error code condition. Any error flag combination that contains an overrun error will be presented as an Overrun Error (code 0010) in the RICR register. A framing error and parity error combination will be presented as a Framing Error (code 0011) in the RICR Register. A multiple error condition that displays a Parity Error (code 0001) does not exist. This priority scheme is used only by the Asynchronous Line Card. Existing error code bits that are generated on a synchronous line are not affected by this scheme.

PROGRAMMABLE MODEM CONTROL DEVICE REGISTERS

The Asynchronous Line Card uses the existing modem control unit, but with Secondary Receive and Secondary Transmit substituted for Data Set Ready and New Sync respectively. An asynchronous line requires the following changes to the programmable modem control device registers and bit assignments:

CONTROL STATUS REGISTER (CSR) (ADDRESS: 770XX0)

Bit	Status	Description
12	SEC Rx	The Secondary Receive Flag is a ONE if an ON to OFF or an OFF to ON transition has occurred on this modem lead. This bit is not legitimate if the Program has changed the Line # and the Scan has not cycled for one or more lines. This bit is READ only and shall present a ZERO when INITIALIZED or CLEAR SCAN.

LINE STATUS REGISTER (LSR) (ADDRESS: 770XX2)

3	SEC Tx	The Secondary Transmit (202) flip flop, when a ONE, presents a MARK to the Modems Secondary Transmit lead. This bit is READ/WRITE and is cleared by INITIALIZE or CLEAR MUX.
4	SEC Rx	The state of the modem's Secondary Receive Lead, when a ONE, is a MARKING state. The Sec Rx bit is inhibited when the Line Enable Flip Flop is a ZERO. This bit is READ only.

DV11 BUSY

DV11 Busy is a response that emanates from an asynchronous receiving line to indicate that the character servicing rate for that line isn't being sustained. To insure received data integrity, external hardware must interpret and implement this response in such a fashion as to provide a restraining feature on the remote transmitter.

The "ON" condition of DV11 Busy is indicated by a negative voltage in the 3 to 15 volt range. The "OFF" condition of DV11 Busy is indicated by a positive voltage in the 3 to 15 volt range. DV11 Busy will be in the off state following a Unibus Initialized, DV11 Master Clear or Receiver Enable being cleared (LCR Primary Register bit 13). The ON duration of this lead is dependent on the servicing rate of the DV11 Character Processor. Therefore, DV11 Busy can be of any minimal period. DV11 Busy will be asserted a maximum of 10/16th of a bit time following the reception of the first stop bit. For an operating speed of 38.4K baud, external hardware must implement the DV11 Busy feature.

DATA SET BUSY

Each asynchronous transmitting line has the capability of having continual transmission remotely started and stopped. This is the complementary feature of DV11 Busy. Data Set Busy must be implemented with external supporting hardware and must be used with an operating speed of 38.4K baud. Line card modification is required for implementing Data Set Busy at a baud rate other than 38.4K baud.

The "ON" condition of Data Set Busy will be interpreted by a negative voltage in the 3 to 15 volt range. The "OFF" condition of Data Set Busy will be interpreted by a positive voltage in the 3 to 15 volt range. Data Set Busy, when on, is defined as a remote stop request.

To inhibit continual character transmission, Data Set Busy must be received prior to 15/16th of the last stop bit interval. Data Set Busy is invalid when the line is being operated in either internal maintenance mode or at an operating speed less than 38.4K baud, assuming no line card modification was performed.

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DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

ENGINEERING SPECIFICATION

DATE 22 April 75

TITLE DV11 Acceptance Procedure

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	E C O CHANGE	00004	W. SMITH	4-76	[illegible]	5-28-76

ENG	APPD	SIZE	CODE	NUMBER	REV
[illegible] 4-22-75		A	SP	DV11 - Ø - 4	A

DEC 16-(392)-1079-N971
DRA 107

ENGINEERING SPECIFICATION [redacted] CONTINUATION SHEET

TITLE DV11 Acceptance Procedure

I. Q.C. STATUS

Acceptance must ascertain that hte DV11-AA, DV11-BA, DV11-BB and DV11-BC have been through Q.C.

II. ECO STATUS

All hardware to be shipped with this option must have all current ECO's installed. Acceptance area will have on hand any and all information required to verify the ECO status of the option to be shipped.

III. Hardware Procedure

A. Requirements

1. DV11 logic tests DZDVA through DZDVF
2. PDP-11 with 8K of core and a console Teletype
3. An expander box suitable for the DV11; i.e. with space for hex modules and capable of supplying the following current requirements:

	@ +5 Volts	@ -15 Volts	@ +15 Volts
DV11-AA, 2 DV11-BA	17.5 Amps	1 Amp	Ø.5 Amps
DV11-AA, 2 DV11-BB	20.5 Amps	1 Amp	Ø.6 Amps
DV11-AA, DV11-BA, DV11-BB	19.0 Amps	1 Amp	Ø.55 Amps

B. Procedure

1. Check the module placement against sheet 9 of the Unit Assembly drawing (D-UA-DV11-Ø-Ø).
2. Place an H8612 test connector in the jack of each line card. Connect a total of four BC08R cables from each jack of the M7807 and M7809 modules to each jack (all are identical) of the H861 test connector. Connect the BC08R cables such that the smooth side is toward you and the ribbed side is toward the circuit board.
3. Load and run diagnostics DZDVA through DZDVF for four error-free passes* each. In the DZDVE diagnostic select the tests appropriate to H861. Refer to the diagnostic writeup for starting procedures. In particular, refer to the DZDVE writeup for manual input of parameters if other than standard addresses, etc. are being used.

*NOTE: RUN ALL DIAGNOSTICS WITH ITERATIONS ENABLED.

SIZE	CODE	NUMBER	REV
A	SP	DV11-Ø-4	A

DEC FORM NO DEC 16-(381)-1022-N370
DRA 108

4. Remove the H8612 and H861 test connectors and reconfigure the apparatus in accordance with Figure 1.
5. Load and run four error-free passes* of DZDVE, selecting the tests which utilize the H325 test connector. Note that the DZDVE test can be run with any number of H325's by using the introductory dialog of the DZDVE test to specify which lines are equipped with H325's and then moving the H325's until all lines have been tested.

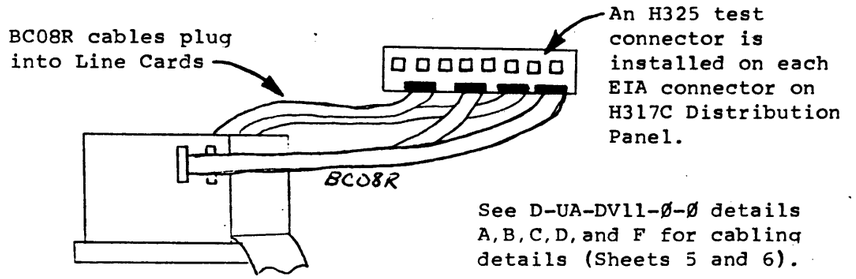

Figure 1- Test Configuration for Acceptance Procedure

Note for Figure 1: Only one H317C Distribution Panel is shown. This is sufficient to test two line cards simultaneously. If it is desired to test four at a time, a second H317C panel would be used and eight more H325 connectors.

*NOTE: RUN ALL DIAGNOSTICS WITH ITERATIONS ENABLED.

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

PARTS LIST

MADE BY John McNamara	CHECKED Ed Roberts	SECTION
DATE April 16, 1975	DATE 4-17-75	
ENG John E. McNamara	PROD R. Wall	ISSUED SECT.
DATE 4-17-75	DATE 4-17-75	

ITEM NO.	DWG NO. / PART NO.	DESCRIPTION	QUANTITY / VARIATION DV11-AA
1.	MP-DV11-Ø	DV11 Customer Print Set #1	1
2.	ZJ192-RB	DV11 Diagnostic Kit	1
3.	EK-DV11-MM	DV11 Maintenance Manual	1

TITLE	ASSY NO.	SIZE	CODE	NUMBER	REV.	ECO NO.
DV11 Shipping List	SHEET 1 OF 1	A	PL	DV11-Ø-5		
		DIST.				

DEC FORM DEC 16-(325)-1031-N870
DRA 110

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

PARTS LIST

MADE BY John McNamara	CHECKED Sid Roberts	SECTION
DATE April 16, 1975	DATE 4-17-75	
ENG John E. McNamara	PROD R. Wall	ISSUED SECT.
DATE 4-17-75	DATE 4-17-75	

ITEM NO.	DWG NO. / PART NO.	DESCRIPTION	QUANTITY / VARIATION DV11-AA
1	ZJ192-RB	DV11 Diagnostic Kit	1
		NOTE: The ZJ192-RB diagnostic kit includes,	
		but is not necessarily limited to, the	
		following diagnostics: Maindec-11-DZDVA,	
		Maindec-11-DZDVB, Maindec-11-DZDVC,	
		Maindec-11-DZDVD, MAINDEC-11-DZDVE,	
		AND MAINDEC-11-DZDVF.	

TITLE	ASSY NO.	SIZE	CODE	NUMBER	REV.	ECO NO.
DV11 Software List	-11-	A	PL	DV11-0-6	A	DV11-00004
	SHEET 1 OF 1	DIST.				

DEC FORM DEC 16-(325)-1031-N870
DRA 110

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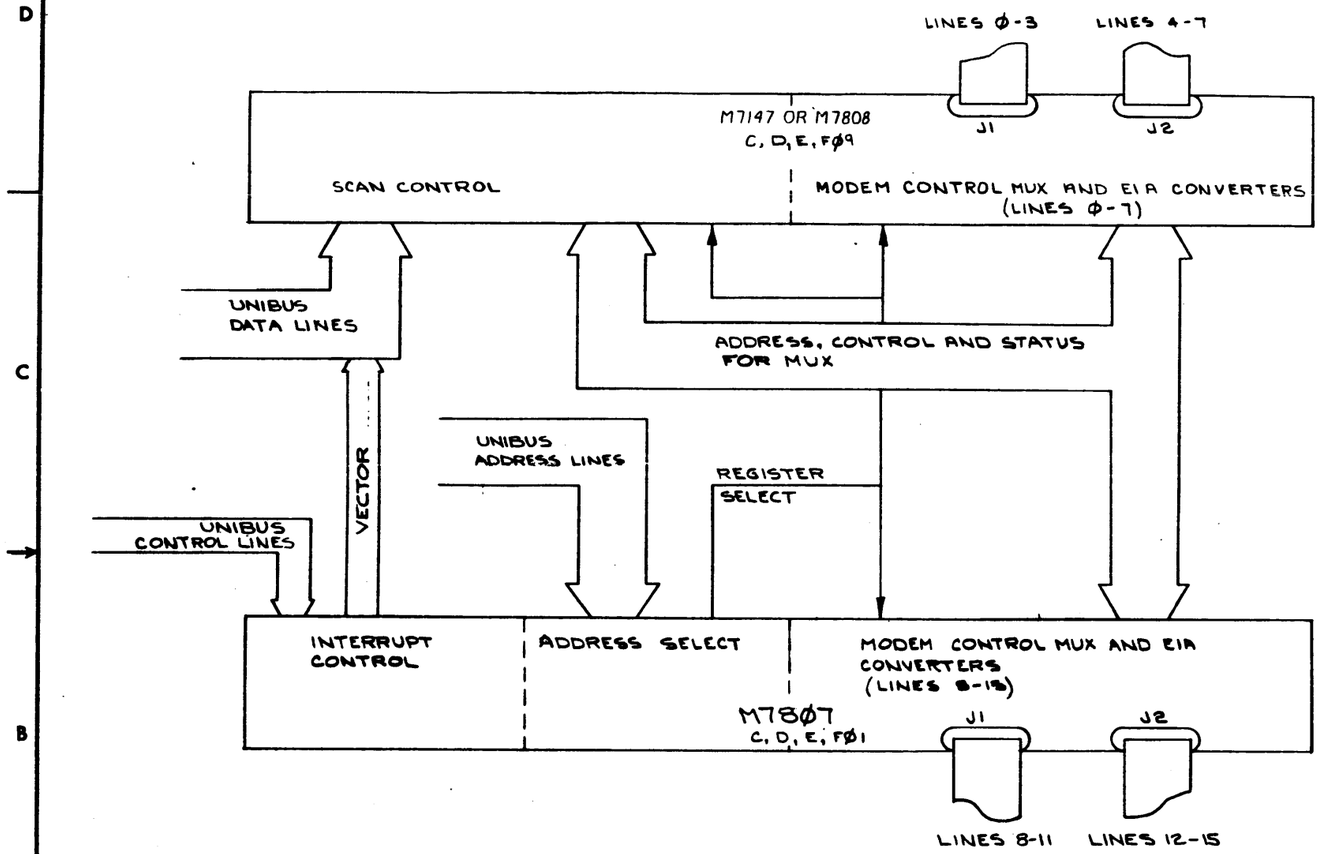


FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
DV11		PARTS LIST		

DIMENSIONAL TOLERANCE
DIMENSIONS ARE MILLIMETERS / INCHES
UNLESS OTHERWISE SPECIFIED

MILLIMETERS	INCHES	ANGLES
X.XX = ±0.10	.XXX = ±.005	±0° 30'
X.X = ±0.5	.XX = ±.02	
X = ±2.	.X = ±.1	

THIRD ANGLE PROJECTION

REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓

MATERIAL

FINISH

DRN K. Davis DATE 3-18-75
CHK'D [signature] DATE 4-17-75
ENG [signature] DATE 4-17-75
PROJ. ENG. [signature] DATE 4-17-75
PROJ. [signature] DATE 4-17-75

NEXT HIGHER ASSY.
B-DD-DV11-Ø

SCALE
SHEET 1 OF 2

digital

TITLE
DV11 MODEM CONTROL

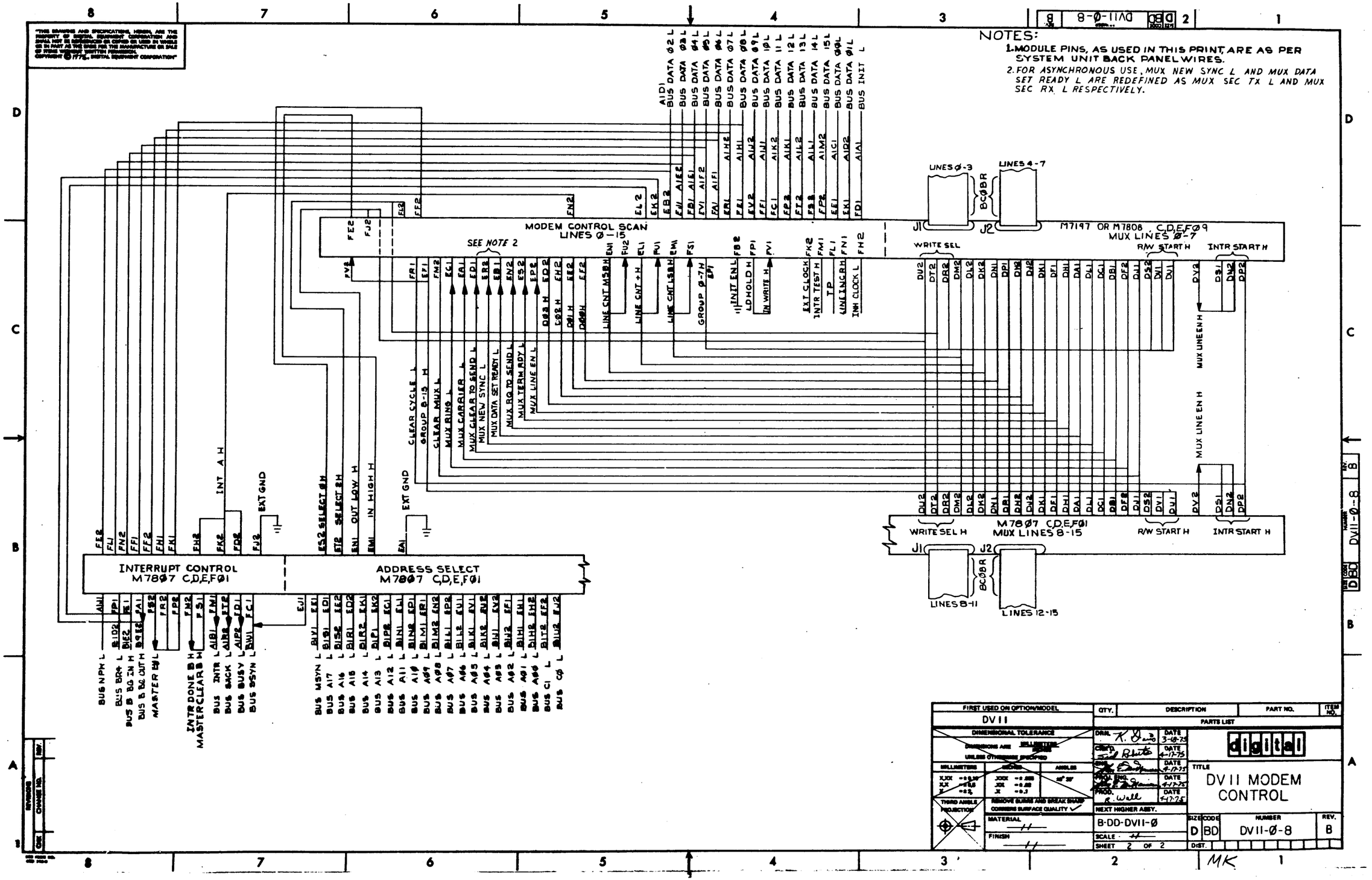
SIZE	CODE	NUMBER	REV.
D	BD	DV11-Ø-8	B

DIST.

MK

REVISIONS

CHG.	CHANGE NO.	REV.
	DV11-00004	A
	J. MCNAMARA 5-26-76	
	DV11-MK008	B
	R. HARRINGTON 23-OCT-78	


NOTES:
1. MODULE PINS, AS USED IN THIS PRINT, ARE AS PER SYSTEM UNIT BACK PANEL WIRES.
2. FOR ASYNCHRONOUS USE, MUX NEW SYNC L AND MUX DATA SET READY L ARE REDEFINED AS MUX SEC TX L AND MUX SEC RX L RESPECTIVELY.
MODEM CONTROL SCAN
LINES Ø-15
SEE NOTE 2
M7197 OR M7808 C,D,E,FØ9
MUX LINES Ø-7
LINES Ø-3
LINES 4-7
BCØBR
WRITE SEL
R/W START H
INTR START H
MUX LINE EN H
M78Ø7 C,D,E,FØ1
MUX LINES 8-15
WRITE SEL H
LINES 8-11
LINES 12-15
INTERRUPT CONTROL
M78Ø7 C,D,E,FØ1
ADDRESS SELECT
M78Ø7 C,D,E,FØ1
INT A H
EXT GND
CLEAR CYCLE L
GROUP 8-15 H
CLEAR MUX L
MUX RING L
MUX CARRIER L
MUX CLEAR TO SEND L
MUX NEW SYNC L
MUX DATA SET READY L
MUX RQ TO SEND L
MUX TERM RDY L
MUX LINE EN L
LINE CNT MSB H
LINE CNT + H
LINE CNT LSB H
GROUP Ø-7 H
INIT EN L
LD HOLD H
IN WRITE H
EXT CLOCK
INTR TEST H
TP
LINE INCR H
INH CLOCK L
BUS DATA Ø2 L
BUS DATA Ø3 L
BUS DATA Ø4 L
BUS DATA Ø5 L
BUS DATA Ø6 L
BUS DATA Ø7 L
BUS DATA Ø8 L
BUS DATA Ø9 L
BUS DATA 1Ø L
BUS DATA 11 L
BUS DATA 12 L
BUS DATA 13 L
BUS DATA 14 L
BUS DATA 15 L
BUS DATA ØØL
BUS DATA Ø1L
BUS INIT L
BUS NPR L
BUS BR4 L
BUS B BG IN H
BUS B BG OUT H
MASTER H L
INTR DONE B H
MASTER CLEAR B H
BUS INTR L
BUS SACK L
BUS BUSY L
BUS SSYN L
BUS MSYN L
BUS A17 L
BUS A16 L
BUS A15 L
BUS A14 L
BUS A13 L
BUS A12 L
BUS A11 L
BUS A1Ø L
BUS A Ø9 L
BUS A Ø8 L
BUS A Ø7 L
BUS A Ø6 L
BUS A Ø5 L
BUS A Ø4 L
BUS A Ø3 L
BUS A Ø2 L
BUS A Ø1 L
BUS A ØØ L
BUS C1 L
BUS CØ L
FIRST USED ON OPTION/MODEL
DV11
QTY.
DESCRIPTION
PART NO.
ITEM NO.
PARTS LIST
DIMENSIONAL TOLERANCE
DIMENSIONS ARE MILLIMETERS
UNLESS OTHERWISE SPECIFIED
MILLIMETERS
INCHES
ANGLES
THIRD ANGLE PROJECTION
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY
MATERIAL
FINISH
DRN.
CHK'D.
ENG.
PROJ. ENG.
PROD.
DATE 3-18-75
DATE 4-17-75
DATE 4-17-75
DATE 4-17-75
DATE 4-17-75
NEXT HIGHER ASSY.
B-DD-DV11-Ø
SCALE
SHEET 2 OF 2
digital
TITLE
DV11 MODEM CONTROL
SIZE D
CODE BD
NUMBER DV11-Ø-8
REV. B
DIST.
MK

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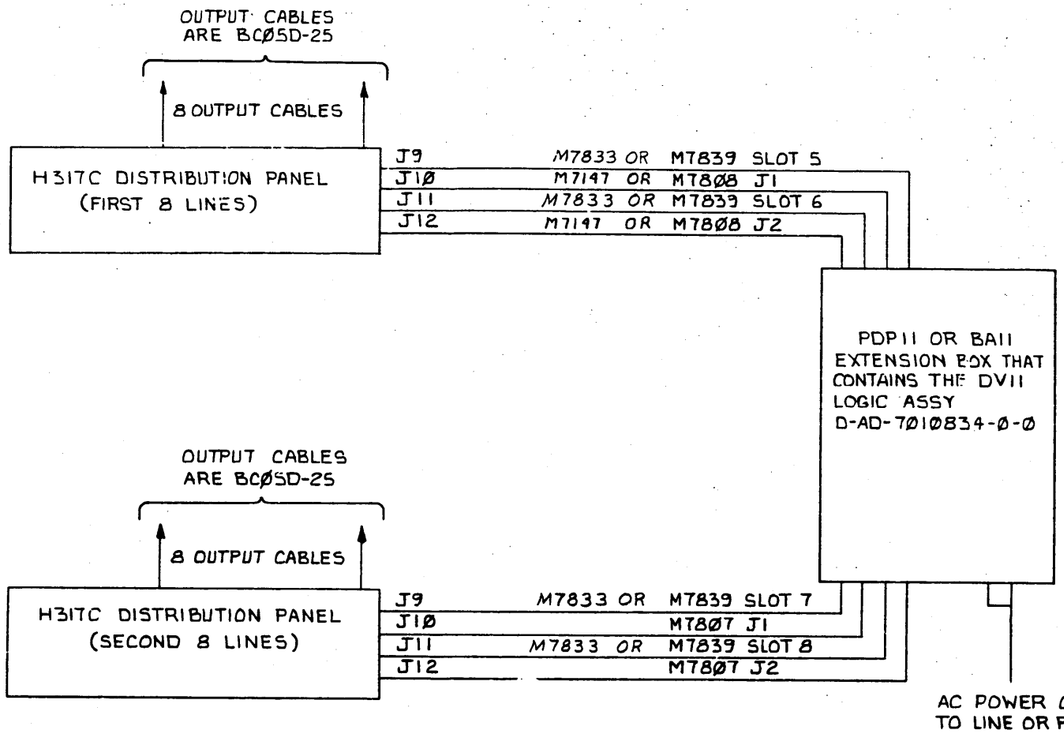
NOTES:

1. ON M78ØT & M7147 OR M7808 MODULES J1 IS THE JACK NEAREST THE EDGE OF THE BOARD.
2. ON H31TC DISTRIBUTION PANEL (D-CS-5411153) J9 IS FAR LEFT JACK; J12 IS FAR RIGHT JACK.
3. INSERT CABLES FLAT SIDE TOWARD YOU; RIBBED SIDE AGAINST CIRCUIT BOARD.



REVISIONS			
CHK	CHANGE NO.	REV.	
JCM	DV11-00004	A	J. MCNAMARA 21MAY76
[illegible]	DV11-MK008	B	R. HARRINGTON 26OCT78

DEC FORM NO. DRC 100-B

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
DV11		PARTS LIST		

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES	DRN. Robert Hopgood	DATE 3-28-75
TOLERANCES	CHK'D S. Roberts	DATE 4-17-75
DECIMALS: .xxx = .005, .xx = .02, .x = .1 — ANGLES: ±0° 30'	ENG. [illegible]	DATE 4-17-75
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY √	PROJ. ENG. [illegible]	DATE 4-17-75
MATERIAL —	PROD. R. Wall	DATE 4-17-75
FINISH —	NEXT HIGHER ASSY. B-DD-DV11-Ø	
	SCALE —	
	SHEET 1 OF 1	

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE: INTERCONNECTION DV11

SIZE	CODE	NUMBER	REV.
C	IC	DV11-Ø-9	B

DIST.

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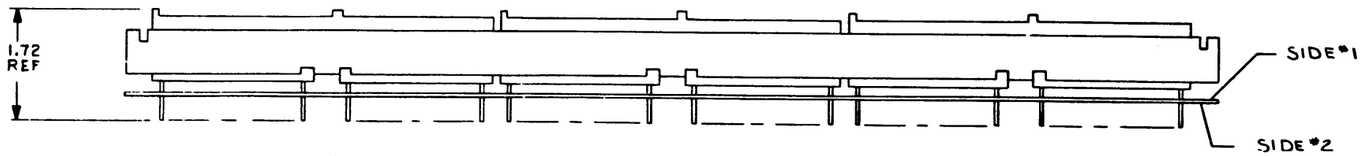
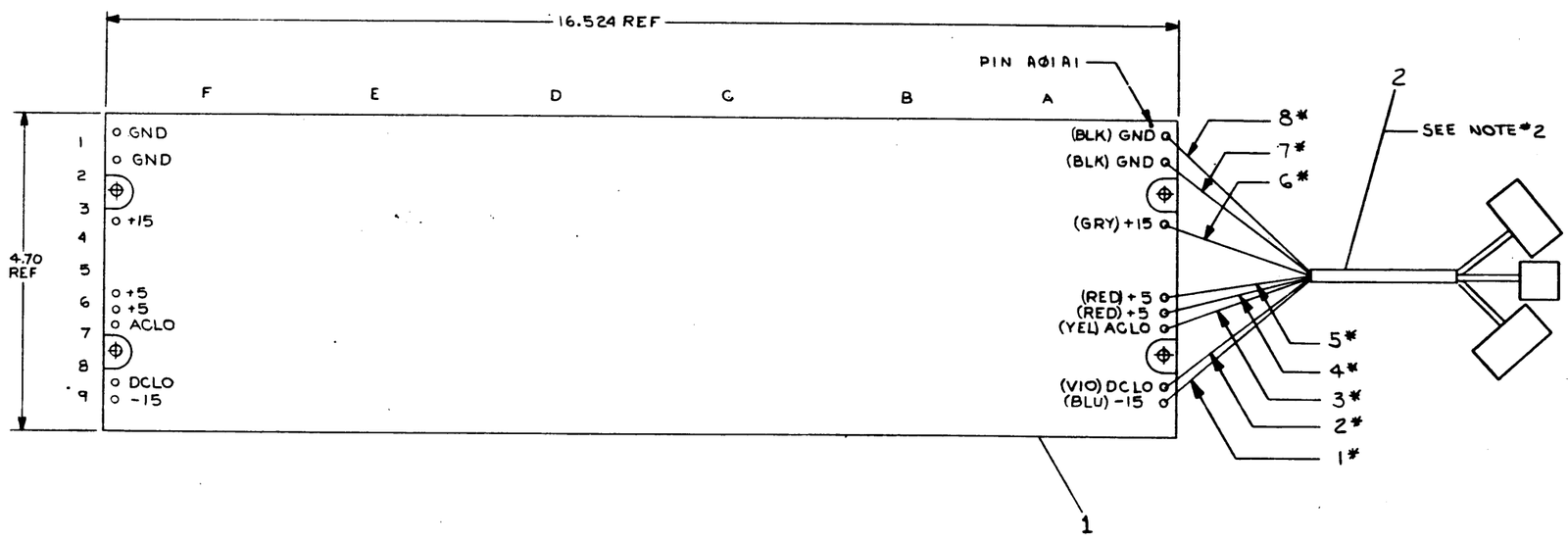
DO NOT SCALE DRAWING

NOTES:
1. * INDICATES POINT NO. ON ITEM #2 (POWER HARNESS).
2. ITEM #2 (POWER HARNESS) TO BE CONNECTED TO ITEM #1 (LOGIC ASSY) AS SHOWN USING SOLDER.





REF	AWT REVSTATUS	A-WT-7010834-0	3
1	POWER HARNESS (DV11)	D-IA-7010835-0-0	2
1	WIRED ASS'Y	D-IA-7010655-0-0	1
	DESCRIPTION	DWG./PART NO.	ITEM NO.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

ANGLES 10° 30'
SURFACE QUALITY ✓ MICROINCHES
CLASS OF ACCURACY (CHECK ONE): MEDIUM / PREFERRED
NOMINAL DIMENSION RANGE INCHES: OVER 0 TO 0.2; OVER 0.2 TO 1.2; OVER 1.2 TO 4.0; OVER 4.0 TO 12.0; OVER 12.0 TO 48.0; OVER 48.0 TO 80.0
QUANTITY & VARIATION

THIRD ANGLE PROJECTION
REMOVE BURRS AND BREAK SHARP CORNERS
DO NOT SCALE DWG
MATERIAL ++
FINISH ++

DRN. 1/17/75
CHK'D 4-9-75
ENG. 4/9/75
PROJ. ENG. 4/9/75
PROD. 4/9/75
NEXT HIGHER ASSY. D-UA-DV11-0-0
SCALE 1/1
SHEET 1 OF 1

FIRST USED ON PDP11
digital
TITLE LOGIC ASS'Y (DV11)
SIZE D CODE AD NUMBER 7010834-0-0 REV.
DIST.

REVISIONS: CHK. CHANGE NO. REV.

DEC FORM NO. DRD 160-C

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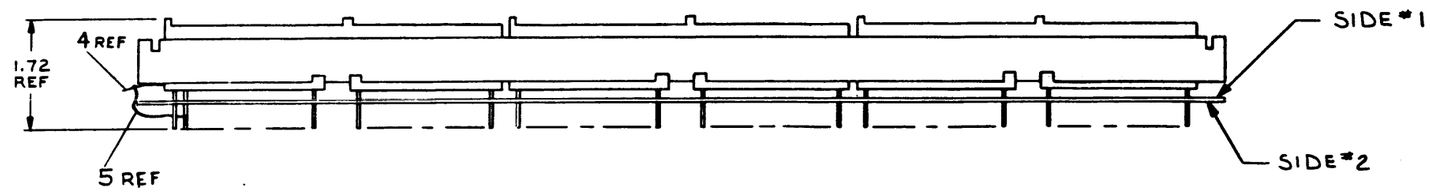
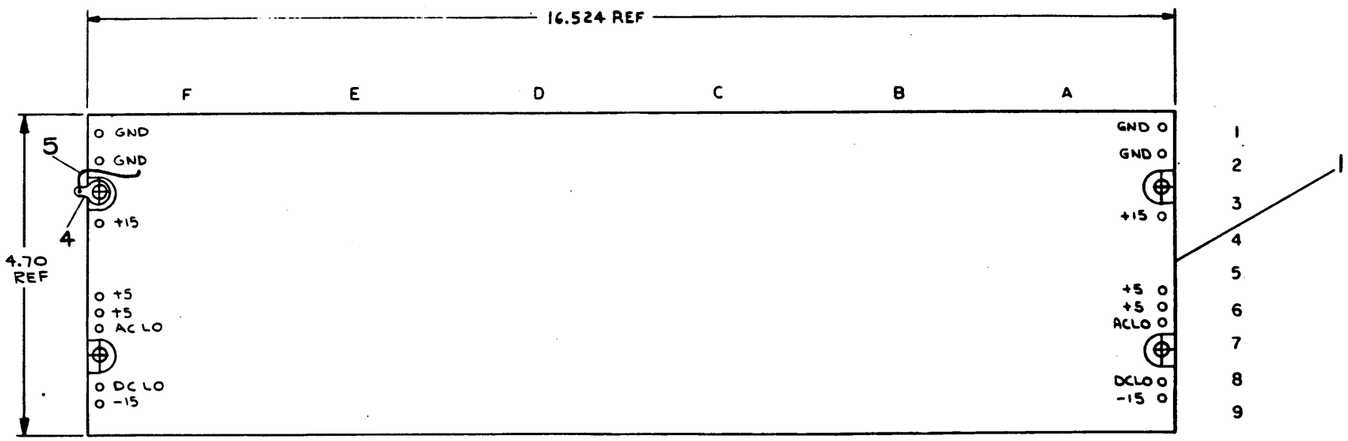
DO NOT SCALE DRAWING

NOTES:

1. WIREWRAP ONE END OF ITEM #5 TO PIN F02T1 AND SOLDER THE OTHER END TO ITEM #4 WHICH IS MOUNTED UNDER THE SYSTEM UNIT MOUNTING SCREW.





QTY.	DESCRIPTION	PART NO.	ITEM NO.
A/R	COMPRESS-O-CARTON	9905016-4	9
REF	PACKAGING INSTRUCTIONS	3700040-0-0	8
1	DECAL, LOGIC ASSY	7411881-01	7
REF	AWT REVISION STATUS	A-WT-7010655-0	6
A/R	WIRE #24 AWG SOLID BLK	9107688-00	5
1	TERMINAL LOCKING, SHAKEPROOF	9008150	4
REF	WIRE LIST	K-WL-DVII-0-7	3
A/R	WIRE #30 AWG SOLID YEL	9105740-44	2
1	BACK PLANE ASSY	D-AD-7010719-0-0	1

PARTS LIST

FIRST USED ON OPTION/MODEL: PDP 11

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES

TOLERANCES: DECIMALS .XXX ± .005, .XX ± .02, .X ± .1; ANGLES ±0° 30'

REMOVE BURRS AND BREAK SHARP CORNERS. SURFACE QUALITY ✓

MATERIAL: —/—/—

FINISH: —/—/—

DRN. C. Harvey DATE 11-26-75
CHKD. S. Roberts DATE 4-9-75
ENG. [signature] DATE 4-9-75
PROJ. ENG. [signature] DATE 4-9-75
PROD. R. Wall DATE 4-9-75

NEXT HIGHER ASSY. D-AD-7010834-0-0

SCALE —/—/—

SHEET 1 OF 1

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE: WIRED ASSY (DVII)

SIZE D | CODE AD | NUMBER 7010655-0-0 | REV. A

DIST.

REVISIONS

CHK	CHANGE NO	REV
J.C.	DVII-00003	A

J. MCNAMARA 4-28-76

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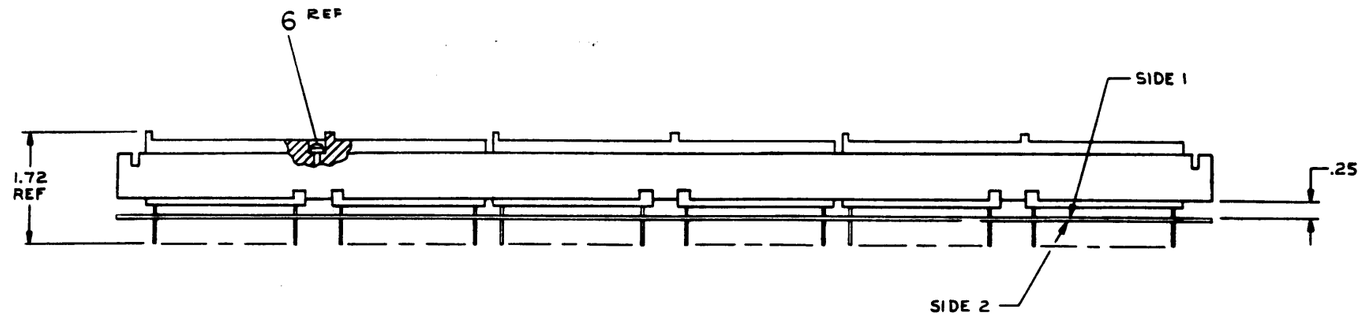
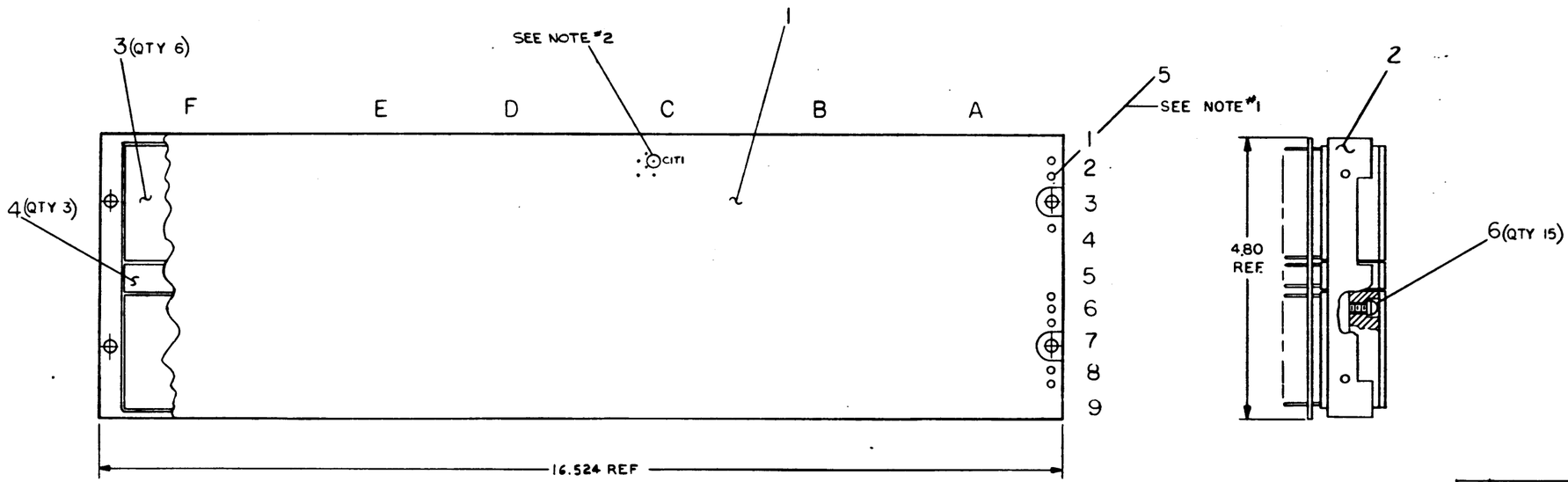
DO NOT SCALE DRAWING

NOTES:
1. INSERT EYELET (ITEM #5) FROM SIDE #2 OF ETCH BOARD.
2. REWORK ITEM #1 (ETCH BOARD), IF REV C, BY USING CIRCUIT BOARD REWORK DRILL (HOLLOW DRILL .04 ID, .125 OD) AT PIN CIT1 ALL THE WAY THROUGH. THIS WORK TO BE DONE AFTER ITEM #1 HAS BEEN INSTALLED ON ITEMS #3 & #4. NO REWORK REQUIRED IF ITEM #1 IS REV D OR LATER





QTY.	DESCRIPTION	PART NO.	ITEM NO.
REF	CIRCUIT SCHEMATIC	D-CS-5411420-0-1	7
15	SCR FILHD POSI DR 8-32 X .62	9006120-6	6
16	EYELET	9009605	5
3	72 PIN CONN. BLOCK	1211425-00	4
6	288 PIN BLOCK H863	1210258	3
1	LOGIC FRAME	1211439	2
1	ETCHED CIRCUIT BOARD	5011419	1

PARTS LIST

FIRST USED ON OPTION/MODEL: PDP 11

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES
TOLERANCES
DECIMALS: .XXX = .005, .XX = .02, .X = .1
ANGLES: ±0 30'
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY
MATERIAL
FINISH

DRN: G. Henry DATE 11-26-74
CHK'D: S. D. Roberts DATE 4-9-75
ENG: DATE 4/9/75
PROJ ENG: DATE 4/9/75
PROD: R. Wall DATE 4/9/75

NEXT HIGHER ASSY.: D-AD-7010655-0-0
SCALE 1/1
SHEET 1 OF 1

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE: BACK PLANE ASSY

SIZE D | CODE IA | NUMBER 7010719-0-0 | REV

DIST.

REVISIONS: REV. | CHANGE NO. | CHK

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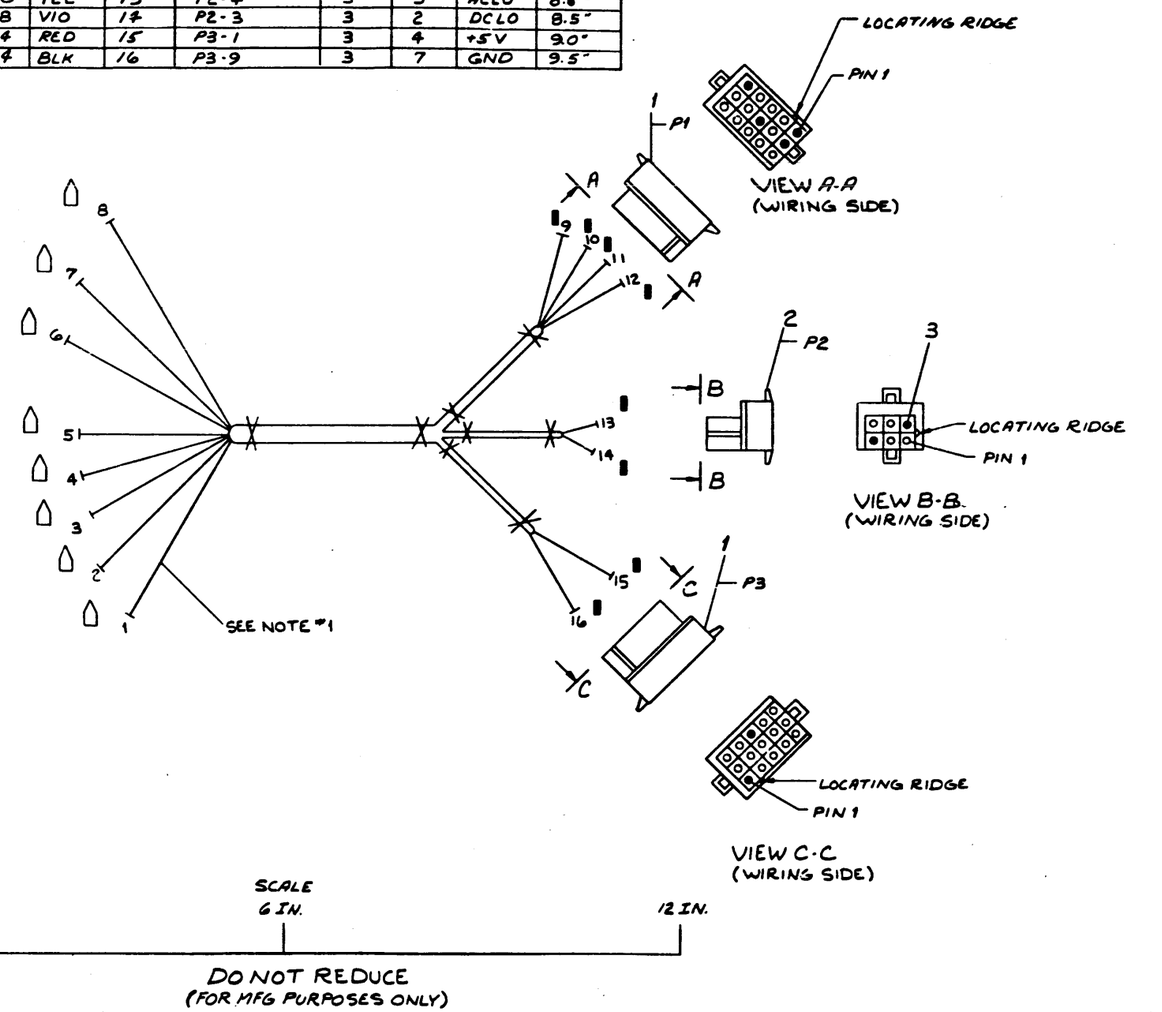
WIRE TABLE

ITEM NO	DESCRIPTION AWG	DESCRIPTION COLOR	FROM POINT	FROM CONNECTION	FROM WITH	TO POINT	SIGNAL	WIRE LENGTHS
6	14	BLU	9	P1-13	3	1	-15V	10.0"
5	14	BLK	10	P1-8	3	8	GND	10.5"
4	14	RED	11	P1-1	3	5	+5V	9.0"
9	18	GRY	12	P1-2	3	6	+15V	9.5"
8	18	YEL	13	P2-4	3	3	ACLO	8.5"
7	18	VIO	14	P2-3	3	2	DCLO	8.5"
4	14	RED	15	P3-1	3	4	+5V	9.0"
5	14	BLK	16	P3-9	3	7	GND	9.5"

NOTES

1. INSULATION AT POINT 1 THRU 8 SHOULD BE STRIPPED BACK .18 INCHS AND WIRES SOLDER TINNED.



SYM	QUANTITY & VARIATION	DESCRIPTION	DWG./PART NO.	ITEM NO.
X	8	TIE WRAP	9007031	10
∩	A/R	WIRE, #18 AWG (GRY)	9107360-88	9
∩	A/R	WIRE, #18 AWG (YEL)	9107360-44	8
∩	A/R	WIRE, #18 AWG (VIO)	9107360-77	7
∩	A/R	WIRE, #14 AWG (BLU)	9107370-66	6
∩	A/R	WIRE, #14 AWG (BLK)	9107370-00	5
∩	A/R	WIRE, #14 AWG (RED)	9107370-22	4
■	8	PIN, MALE	1209378-01	3
	1	HOUSING, CONN, 6 PIN	1209351-06	2
	2	HOUSING, CONN 15 PIN	1209351-15	1

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

ANGLES ±0° 30'

SURFACE QUALITY IN MICROINCHES

CLASS OF ACCURACY (CHECK ONE): MEDIUM ☐ PREFERRED ☐

NOMINAL DIMENSION RANGE INCHES: OVER 0 TO 0.2 | OVER 0.2 TO 1.2 | OVER 1.2 TO 4.0 | OVER 4.0 TO 12.0 | OVER 12.0 TO 48.0 | OVER 48.0 TO 80.0

MEDIUM	▭	±.004	±.008	±.012	±.016	±.024	±.01
PREFERRED	▭	±.012	±.016	±.025	±.04	±.003	±0.1

THIRD ANGLE PROJECTION

REMOVE BURRS AND BREAK SHARP CORNERS

DO NOT SCALE DWG

MATERIAL: SEE PARTS LIST

FINISH

DRN. 1-20-75
CHK. 3-31-75
ENG. 3-31-75
PROJ. ENG. 3-31-75
PROD. R. Will 3-31-75

NEXT HIGHER ASSY.: D-AD-7010834-0-0

SCALE

SHEET 1 OF 1

FIRST USED ON: DV11

digital

TITLE: POWER HARNESS (DV11)

SIZE: D | CODE: IA | NUMBER: 7010835-0-0 | REV.

DIST.

REVISIONS: CHK. | CHANGE NO. | REV.

DEC FORM NO. DRD 100-C

D IA 7010835-0-0

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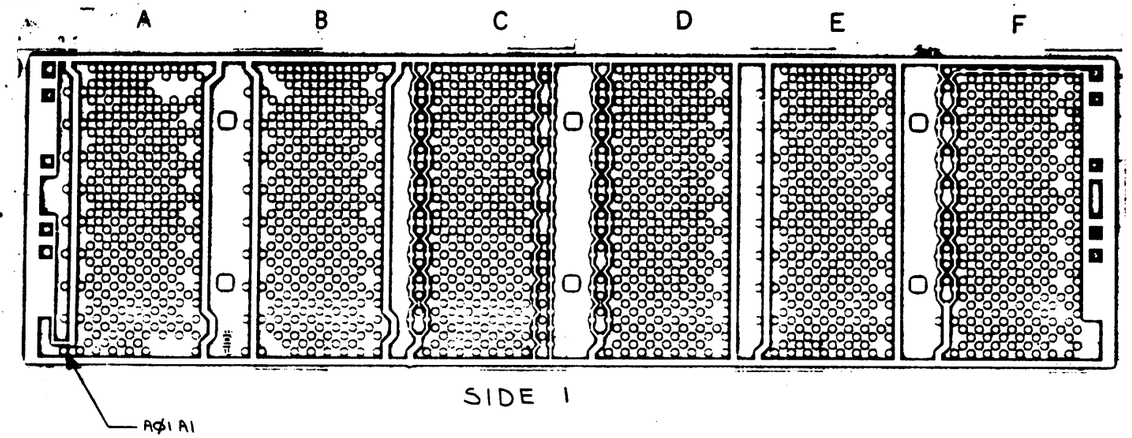
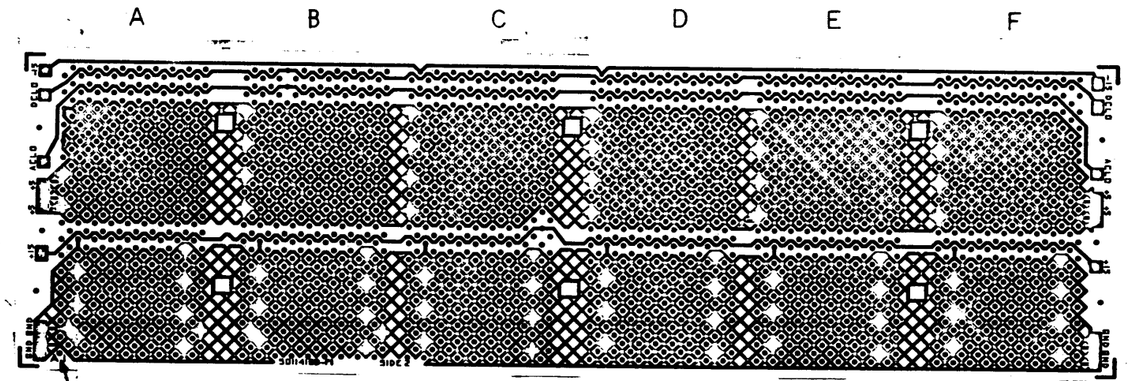
NOTES:



SIDE 1



SIDE 2

IC TYPE	GND	+ 5V

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

REF		MODULE ECO HISTORY	B-MM-5411420-0-4	4
REF		ASSY/DRILLING HOLE LAYOUT	D-MM-5411420-0-5	3
REF		X-Y COORDINATE HOLE LOCATION	K-CO-5411420-0-4	2
1		ETCHED CIRCUIT BOARD	5011419	1
QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

FIRST USED ON OPTION MODEL: PDP 11

ETCH BOARD REV: D

REVISIONS	REV	CHANGE NO.	CHK	DATE
J. McNAMARA 1-24-75	B	5411420-1	J. McNAMARA	1-24-75
J. McNAMARA 4-10-75	C	5411420-00002	J. McNAMARA	4-10-75

DEC NO.	EIA NO.	DEC NO.	EIA NO.

SEMICONDUCTOR CONVERSION CHART

		DATE
DRN	R. Davis	1-24-75
CHK'D	K. McNamara	1-24-75
ENG	K. McNamara	1-24-75
FIRST ENG	K. McNamara	1-24-75
PROJ	K. Will	1-24-75

NEXT HIGHER ASSY: D-IA-7010719-0-0

SCALE: NONE

SHEET: 1 OF 1

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE: CIRCUIT SCHEMATIC

SIZE D | CODE CS | NUMBER 5411420-0-1 | REV. C

DIST.

DCS5411420-0-1 C

B

A

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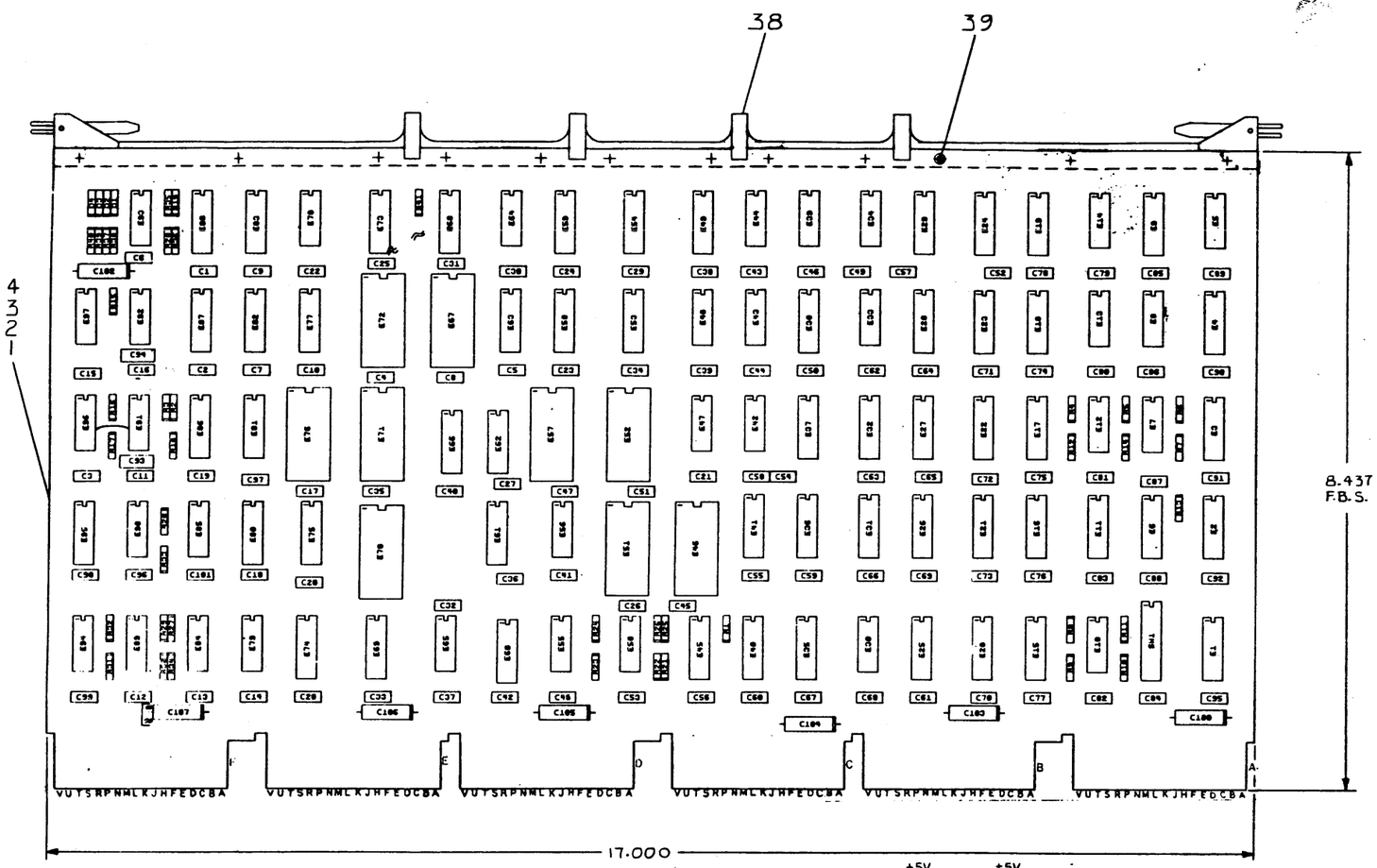
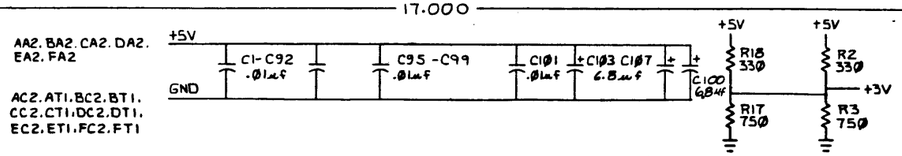
NOTES:





74155	8	16	
74151	8	16	
74153	8	16	
74181	12	24	
74150	12	24	
74175	8	16	
74174	8	16	
8640	1	8	
74157	8	16	
8838	9	16	
3341	8	16	1
IC TYPE	GND	+5V	-12V

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

REF			
REF		X-Y COORDINATE HOLE LOCATION	K-CO-M7836-0-4
REF		ASSY/DRILLING HOLE LAYOUT	D-AH-M7836-0-5
REF		MODULE ECO HISTORY	B-MH-M7836-0-6
1		ETCHED CIRCUIT BOARD	5010876
1	C83	CAP 10 PF 100V 5% DM	1000008
1	C84	CAP 100 PF 100V 5% DM	1000016
88	C1 THRU C82, C95-C99, C101	CAP .01 UF 100V 20% CER	1001810-01
7	C100. C102 THRU C107	CAP 6.8 UF 35V 10% tant	1005306
4	D1-D4	DIODE D664	1100114
2	R2, R18	RES. 330 1/4W 5%	1300295
1	R1	RES. 470 1/4W 5%	1300316
1	R15	RES. 3K 1/4W 5%	1300432
12	R4-R14, R41	RES. 1K 1/4W 5%	1300385
2	R3, R17	RES. 750 1/4W 5%	1301401
1	R16	RES. 18K 1/4W 5%	1302485
4	E5. E85. E90, E97	IC 7474	1905547
1	E55	IC 7432	19M521
1	E78	IC 7420	1905577
1	E84	IC 7402	1908004
3	E14. 30. 65	IC 7404	1909688
1	E8	IC 8881	1908705
3	E7. 10. 12	IC 8242	1909712
4	E13. 50. 89. 93	IC 8640	1911469
4	E38. 49. 53. 54	IC 74153	1909837
5	E46. 52. 57. 70. 71	IC 74181	1909862
10	E33. 34. 39. 42. 43. 44. 47. 48. 56. 64	IC 7486	1910011
2	E79. 96	IC 7437	1910091
4	E51, 67, 72, 76	IC 74158	1910153
2	E91, 92	IC 74121	1910230
7	E4, 9, 19, 28. 82, 62, 31.	IC 74175	1910651
13	E 53, 59, 60, 61, 63, 66, 18, 23, 27, 41, 45, 35. 36.	IC 74174	1910652
4	E1, 37, 40, 32	IC 74157	1910655
1	E35	IC 74155	1910656
4	E 3. 15. 20. 25	IC 8838	1911117
1	E 94	IC 7400	1910155
8	E29. 73. 81. 29. 83. 86. 88. 68	IC 3341	2111188
1	SW1	SWITCH 10 POS	1211184-06
1		HEX HANDLE ASSY	1210711 -2
12		EYELET	9006732
11	R19. 21. 23. 25. 27. 29. 31. 33. 35. 37. 39	RES. 180. 1/4W. 5%	1301322
11	R20. 22. 24. 26. 28. 30. 32. 34. 36. 38. 40	RES. 390. 1/4W. 5%	1300309
1		COVER SWITCH 10 POS	1211284-06
14	E2. 6. 11. 16. 17. 21. 22. 26. 69. 74. 75. 77. 80. 87	IC. 74151	1909936
A/R		WIRE #30 AWG INSULATED	9105740

QTY	REF DESIGNATION	DESCRIPTION	PART NO	ITEM NO.

PARTS LIST

FIRST USED ON OPTION MODEL: DV11-AA

ETCH BOARD REV B

ORIGINATED	A
CHK	

REVISIONS

DEC NO.	EIA NO.	DEC NO.	EIA NO.

SEMICONDUCTOR CONVERSION CHART

		DATE
DRN	P.L. Jr.	3/11/75
DWG		DATE
CHK		DATE 3/14/75
ENG		DATE 3/14/75
PROJ ENG		DATE 3/14/75
PROJ	R. Wall	DATE 3/14/75

NEXT HIGHER ASSY: B-DD-DV11-0

SCALE

SHEET 1 OF 10

digital EQUIPMENT CORPORATION

TITLE: ALU AND TRANSFER BUS

SIZE	CODE	NUMBER	REV.
D	CS	M7836-0-1	A

DIST.

DCS M7836-0-1 A

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SUB DI-2 ALU A=B H
DI-1 COUT L

74181 E71: DI-2 REG A Ø7 H, DI-2 REG A Ø6 H, DI-2 REG A Ø5 H, DI-2 REG A Ø4 H, DI-2 BUF ROM DATA Ø3 H, DI-2 BUF ROM DATA Ø2 H, DI-2 BUF ROM DATA Ø1 H, DI-2 BUF ROM DATA ØØ H

74181 E7Ø: DI-2 REG A Ø3 H, DI-2 REG A Ø2 H, DI-2 REG A Ø1 H, DI-2 REG A ØØ H, DI-3 BUF ROM DATA Ø4 H, DI-3 BUF ROM DATA Ø5 H

+5V
R1 47Ø

74174 E61 → DI-1 ALU RESULT Ø0 H, Ø3 H, Ø4 H, Ø5 H, Ø6 H, Ø7 H
DM2, DL2, CE1

74174 E18
DI-4 TRANSFER BUS 17 H (BA1) → DI-1 REG B 17 H
DI-4 TRANSFER BUS 16 H (AL1) → DI-1 REG B 16 H
DI-4 TRANSFER BUS 15 H (AV2) → DI-1 REG B 15 H
DI-4 TRANSFER BUS 14 H (BF1) → DI-1 REG B 14 H
DI-4 TRANSFER BUS 13 H (AS2) → DI-1 REG B 13 H
DI-4 TRANSFER BUS 12 H (AP2) → DI-1 REG B 12 H

D3-7 INIT DI L (ES2)

74174 E58
DI-4 TRANSFER BUS 11 H (BE2) → DI-1 REG B 11 H
DI-4 TRANSFER BUS 1Ø H (EV2) → DI-1 REG B 1Ø H
DI-4 TRANSFER BUS Ø9 H (ES1) → DI-1 REG BØ9 H
DI-4 TRANSFER BUS Ø8 (ER1) → DI-1 REG BØ8 H
DI-3 TRANSFER BUS Ø7 (EP1) → DI-1 REG BØ7 H
DI-3 TRANSFER BUS Ø6 (BD2) → DI-1 REG BØ6 H

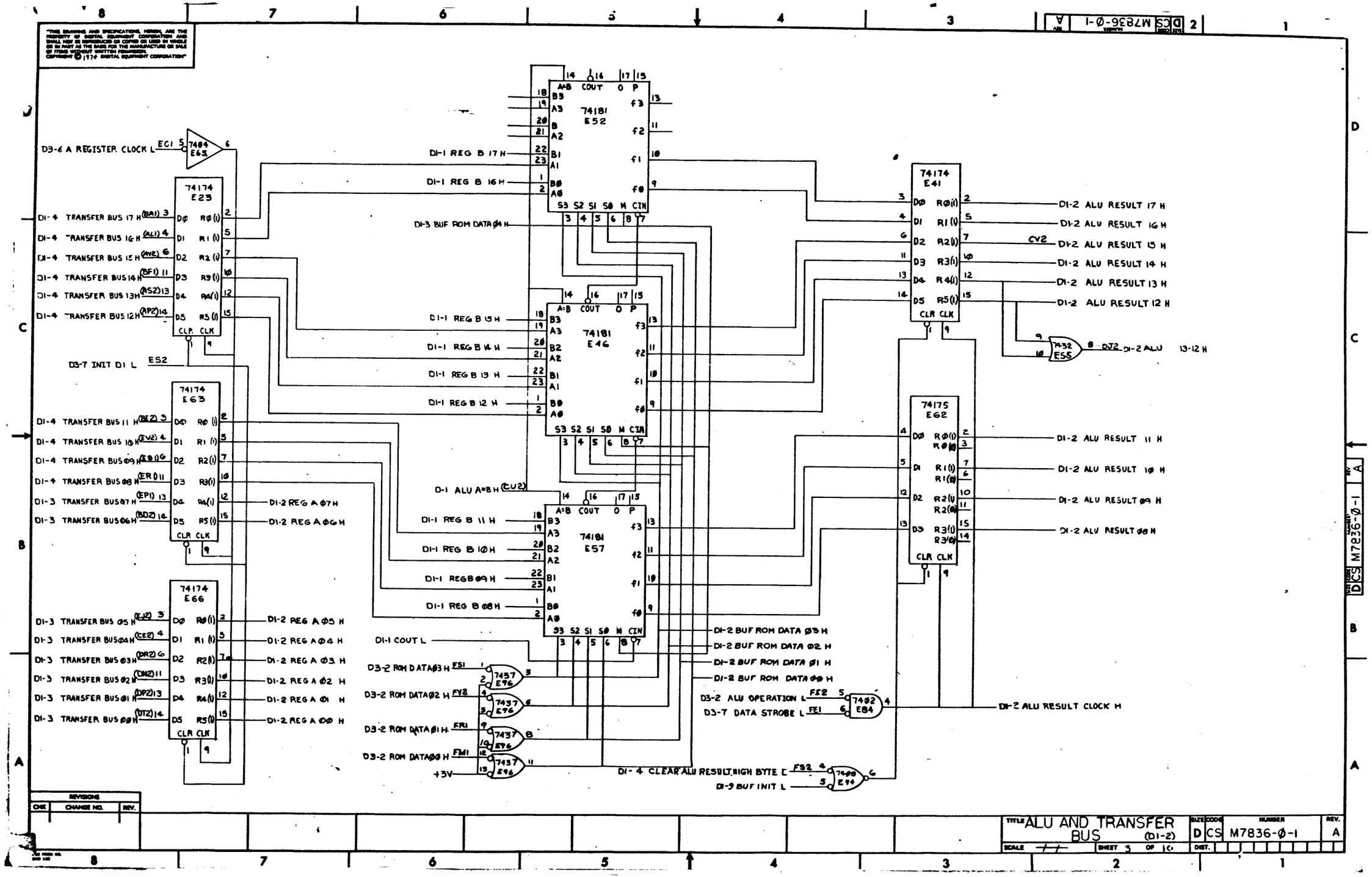
74174 EGØ
DI-3 TRANSFER BUS Ø5 H (EJ2) → DI-1 REG BØ5 H
DI-3 TRANSFER BUS Ø4 H (CE2) → DI-1 REG BØ4 H
DI-3 TRANSFER BUS Ø3 H (DR2) → DI-1 REG BØ3 H
DI-3 TRANSFER BUS Ø2 H (DN2) → DI-1 REG BØ2 H
DI-3 TRANSFER BUS Ø1 H (DP2) → DI-1 REG BØ1 H
DI-3 TRANSFER BUS ØØ H (DT2) → DI-1 REG BØØ H

D3-6B REGISTER CLOCK L DU2 → 7404 EG5

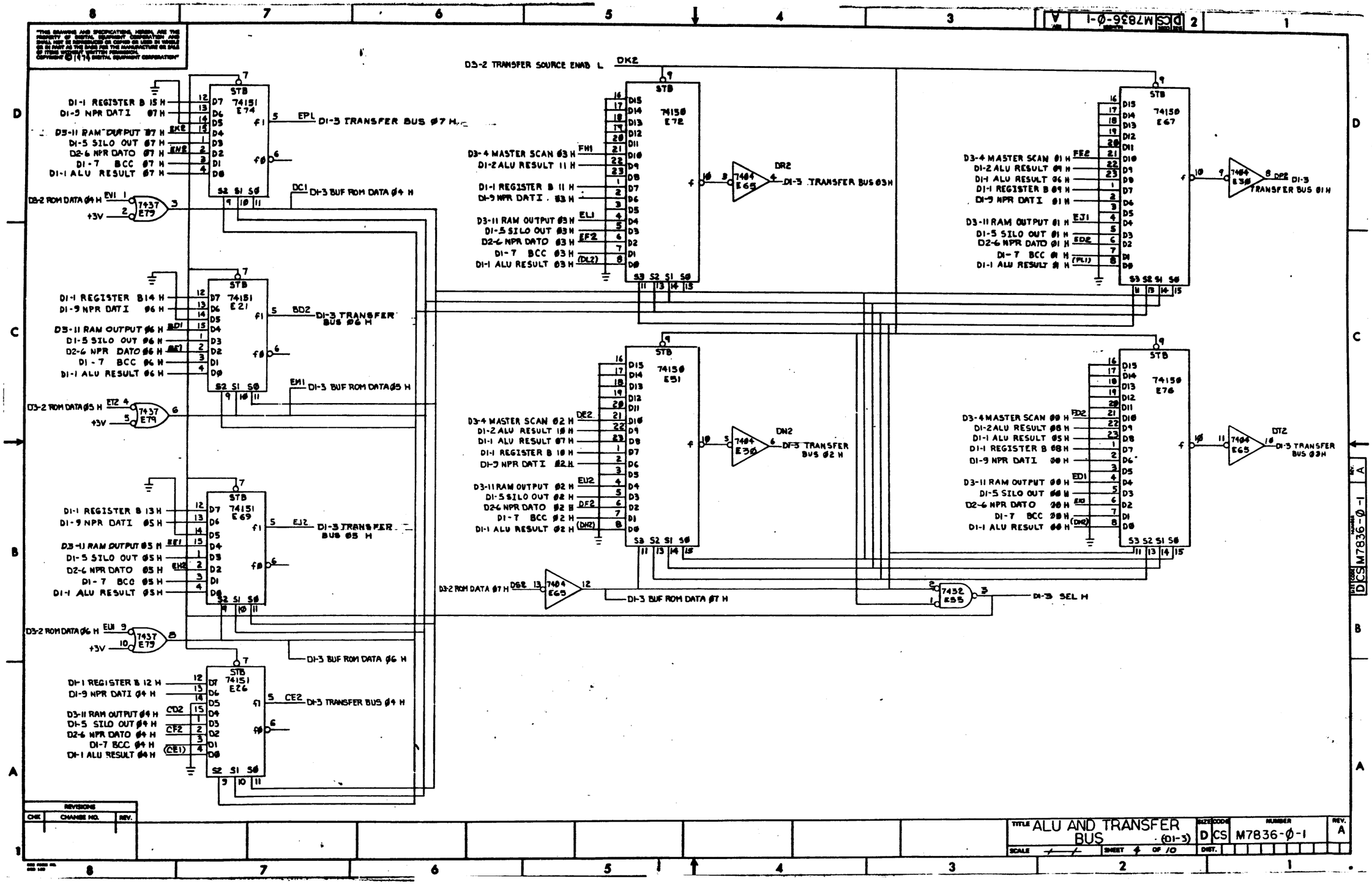
DI-4 SET ALU Ø2 L → 7474 E85 → DI-1 ALU RESULT Ø2 H (DH2)
DI-9 BUF INIT
DI-4 CLEAR ALU Ø2 L (FP1) → 7408 E94
7474 E9Ø → DI-1 ALU RESULT Ø1 H (FL1)
DI-4 CLEAR ALU Ø1 L (FT2) → 7408 E94
DI-2 ALU RESULT CLOCK H

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE ALU AND TRANSFER BUS (DI-1)
SIZE D CODE DCS NUMBER M7836-Ø-1 REV. A
SCALE — SHEET 2 OF 10 DIST.



D3-6 A REGISTER CLOCK L
EC1
7404 E65
74174 E23
D1-4 TRANSFER BUS 17 H
D1-4 TRANSFER BUS 16 H
D1-4 TRANSFER BUS 15 H
D1-4 TRANSFER BUS 14 H
D1-4 TRANSFER BUS 13 H
D1-4 TRANSFER BUS 12 H
D3-7 INIT D1 L
ES2
74174 E63
D1-4 TRANSFER BUS 11 H
D1-4 TRANSFER BUS 10 H
D1-4 TRANSFER BUS 09 H
D1-4 TRANSFER BUS 08 H
D1-3 TRANSFER BUS 07 H
D1-3 TRANSFER BUS 06 H
D1-2 REG A 07 H
D1-2 REG A 06 H
74174 E66
D1-3 TRANSFER BUS 05 H
D1-3 TRANSFER BUS 04 H
D1-3 TRANSFER BUS 03 H
D1-3 TRANSFER BUS 02 H
D1-3 TRANSFER BUS 01 H
D1-3 TRANSFER BUS 00 H
D1-2 REG A 05 H
D1-2 REG A 04 H
D1-2 REG A 03 H
D1-2 REG A 02 H
D1-2 REG A 01 H
D1-2 REG A 00 H
74181 E52
D1-1 REG B 17 H
D1-1 REG B 16 H
D1-3 BUF ROM DATA 04 H
74181 E46
D1-1 REG B 15 H
D1-1 REG B 14 H
D1-1 REG B 13 H
D1-1 REG B 12 H
D-1 ALU A=B H
CU2
74181 E57
D1-1 REG B 11 H
D1-1 REG B 10 H
D1-1 REG B 09 H
D1-1 REG B 08 H
D1-1 COUT L
D3-2 ROM DATA 03 H
D3-2 ROM DATA 02 H
D3-2 ROM DATA 01 H
D3-2 ROM DATA 00 H
+3V
7437 E96
74174 E41
D1-2 ALU RESULT 17 H
D1-2 ALU RESULT 16 H
CV2
D1-2 ALU RESULT 15 H
D1-2 ALU RESULT 14 H
D1-2 ALU RESULT 13 H
D1-2 ALU RESULT 12 H
7432 E55
DJ2
D1-2 ALU 13-12 H
74175 E62
D1-2 ALU RESULT 11 H
D1-2 ALU RESULT 10 H
D1-2 ALU RESULT 09 H
D1-2 ALU RESULT 08 H
D1-2 BUF ROM DATA 03 H
D1-2 BUF ROM DATA 02 H
D1-2 BUF ROM DATA 01 H
D1-2 BUF ROM DATA 00 H
D3-2 ALU OPERATION L
FE2
D3-7 DATA STROBE L
FE1
7402 E84
D1-2 ALU RESULT CLOCK H
D1-4 CLEAR ALU RESULT HIGH BYTE L
FS2
D1-9 BUF INIT L
7408 E94
REVISIONS
CHK
CHANGE NO.
REV.
TITLE ALU AND TRANSFER BUS (D1-2)
SIZE D
CODE CS
NUMBER M7836-0-1
REV. A
SCALE
SHEET 3 OF 10
DIST.



D3-2 TRANSFER SOURCE ENAB L
DK2
STB
74151 E74
74151 E21
74151 E69
74151 E26
74150 E72
74150 E67
74150 E51
74150 E76
7437 E79
7404 E65
7432 E55
D1-1 REGISTER B 15 H
D1-9 NPR DATI 07 H
D3-11 RAM OUTPUT 07 H
D1-5 SILO OUT 07 H
D2-6 NPR DATO 07 H
D1-7 BCC 07 H
D1-1 ALU RESULT 07 H
D1-3 TRANSFER BUS 07 H
D3-2 ROM DATA 04 H
D1-3 BUF ROM DATA 04 H
D1-1 REGISTER B 14 H
D1-9 NPR DATI 06 H
D3-11 RAM OUTPUT 06 H
D1-5 SILO OUT 06 H
D2-6 NPR DATO 06 H
D1-7 BCC 06 H
D1-1 ALU RESULT 06 H
D1-3 TRANSFER BUS 06 H
D3-2 ROM DATA 05 H
D1-3 BUF ROM DATA 05 H
D1-1 REGISTER B 13 H
D1-9 NPR DATI 05 H
D3-11 RAM OUTPUT 05 H
D1-5 SILO OUT 05 H
D2-6 NPR DATO 05 H
D1-7 BCC 05 H
D1-1 ALU RESULT 05 H
D1-3 TRANSFER BUS 05 H
D3-2 ROM DATA 06 H
D1-3 BUF ROM DATA 06 H
D1-1 REGISTER B 12 H
D1-9 NPR DATI 04 H
D3-11 RAM OUTPUT 04 H
D1-5 SILO OUT 04 H
D2-6 NPR DATO 04 H
D1-7 BCC 04 H
D1-1 ALU RESULT 04 H
D1-3 TRANSFER BUS 04 H
D3-4 MASTER SCAN 03 H
D1-2 ALU RESULT 11 H
D1-1 REGISTER B 11 H
D1-9 NPR DATI 03 H
D3-11 RAM OUTPUT 03 H
D1-5 SILO OUT 03 H
D2-6 NPR DATO 03 H
D1-7 BCC 03 H
D1-1 ALU RESULT 03 H
D1-3 TRANSFER BUS 03 H
D3-4 MASTER SCAN 01 H
D1-2 ALU RESULT 09 H
D1-1 ALU RESULT 06 H
D1-1 REGISTER B 09 H
D1-9 NPR DATI 01 H
D3-11 RAM OUTPUT 01 H
D1-5 SILO OUT 01 H
D2-6 NPR DATO 01 H
D1-7 BCC 01 H
D1-1 ALU RESULT 01 H
D1-3 TRANSFER BUS 01 H
D3-4 MASTER SCAN 02 H
D1-2 ALU RESULT 10 H
D1-1 ALU RESULT 07 H
D1-1 REGISTER B 10 H
D1-9 NPR DATI 02 H
D3-11 RAM OUTPUT 02 H
D1-5 SILO OUT 02 H
D2-6 NPR DATO 02 H
D1-7 BCC 02 H
D1-1 ALU RESULT 02 H
D1-3 TRANSFER BUS 02 H
D3-4 MASTER SCAN 00 H
D1-2 ALU RESULT 08 H
D1-1 ALU RESULT 05 H
D1-1 REGISTER B 08 H
D1-9 NPR DATI 00 H
D3-11 RAM OUTPUT 00 H
D1-5 SILO OUT 00 H
D2-6 NPR DATO 00 H
D1-7 BCC 00 H
D1-1 ALU RESULT 00 H
D1-3 TRANSFER BUS 03 H
D3-2 ROM DATA 07 H
D1-3 BUF ROM DATA 07 H
D1-3 SEL H
REVISIONS
CHK
CHANGE NO.
REV.
TITLE ALU AND TRANSFER BUS (D1-3)
SIZE D
CODE CS
NUMBER M7836-0-1
REV. A
SCALE
SHEET 4 OF 10
DIST.

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DI-2 ALU RESULT 17 H
D3-11 RAM OUTPUT 17H AT2
STB 74151 E16 — DØ D1 D2 D3 D4 D5 D6 D7 — fØ f1 — S2 S1 SØ
BAI
DI-4 TRANSFER BUS 17 H

DI-2 ALU RESULT 13H
DI-7 BCC 13H
DI-9 NPR DATO 13H
DI-5 SILO OUT 13H
D3-11 RAM OUTPUT 13H API
D2-3 RIRR Ø5H AR1
STB 74151 E11
AS2 DI-4 TRANSFER BUS 13 H

DI-3 SEL H
DI-2 ALU RESULT 10H
DI-7 BCC 10H
DI-9 NPR DATO 10H
DI-5 SILO OUT 10H
D3-11 RAM OUTPUT 10H EP2
D3-11 RAM OUTPUT Ø2 H EU2
D2-3 RIRR Ø2 H ER2
STB 74151 EBØ
EV2 DI-4 TRANSFER BUS 10 H

DI-2 ALU RESULT 16H
D3-11 RAM OUTPUT 16 H AL2
STB 74151 E2
ALI DI-4 TRANSFER BUS 16 H

DI-2 ALU RESULT 12 H
DI-7 BCC 12 H
DI-9 NPR DATO 12 H
DI-5 SILO OUT 12 H
D3-11 RAM OUTPUT 12H AN1
D2-3 RIRR Ø4 H AM2
STB 74151 E6
AP2 DI-4 TRANSFER BUS 12 H

DI-2 ALU RESULT Ø9 H
DI-7 BCC Ø9 H
DI-9 NPR DATO Ø9 H
DI-5 SILO OUT Ø9 H
D3-11 RAM OUTPUT Ø9 H EE2
D3-11 RAM OUTPUT Ø1 H EJ1
D2-3 RIRR Ø1 H EM2
STB 74151 E75
ES1 DI-4 TRANSFER BUS Ø9 H

DI-2 ALU RESULT 15 H (CY2)
DI-7 BCC 15H
DI-9 NPR DATO 15H
DI-5 SILO OUT 15 H
D3-11 RAM OUTPUT 15 H AR2
D2-3 RIRR Ø7 H AU2
STB 74151 E17
AVE DI-4 TRANSFER BUS 15 H

DI-2 ALU RESULT 11 H
DI-7 BCC 11 H
DI-9 NPR DATO 11 H
DI-5 SILO OUT 11 H
D3-11 RAM OUTPUT 11 H FV1
D2-3 RIRR Ø3 H FD1
STB 74151 E07
BE2 DI-4 TRANSFER BUS 11 H

DI-2 ALU RESULT Ø8 H
DI-7 BCC Ø8 H
DI-9 NPR DATO Ø8H
DI-5 SILO OUT Ø8H
D3-11 RAM OUTPUT Ø8H EL2
D3-11 RAM OUTPUT ØØH EDI
D2-3 RIRR ØØ H ENI
STB 74151 E77
ERI DI-4 TRANSFER BUS Ø8 H

DI-3 BUF ROM DATA Ø4 H
DI-3 BUF ROM DATA Ø5 H
DI-3 BUF ROM DATA Ø6 H

DI-2 ALU RESULT 14 H
DI-7 BCC 14 H
DI-9 NPR DATO 14 H
DI-5 SILO OUT 14 H
D3-11 RAM OUTPUT 14 H BC1
D2-3 RIRR Ø6H BB1
STB 74151 E22
BFI DI-4 TRANSFER BUS 14 H

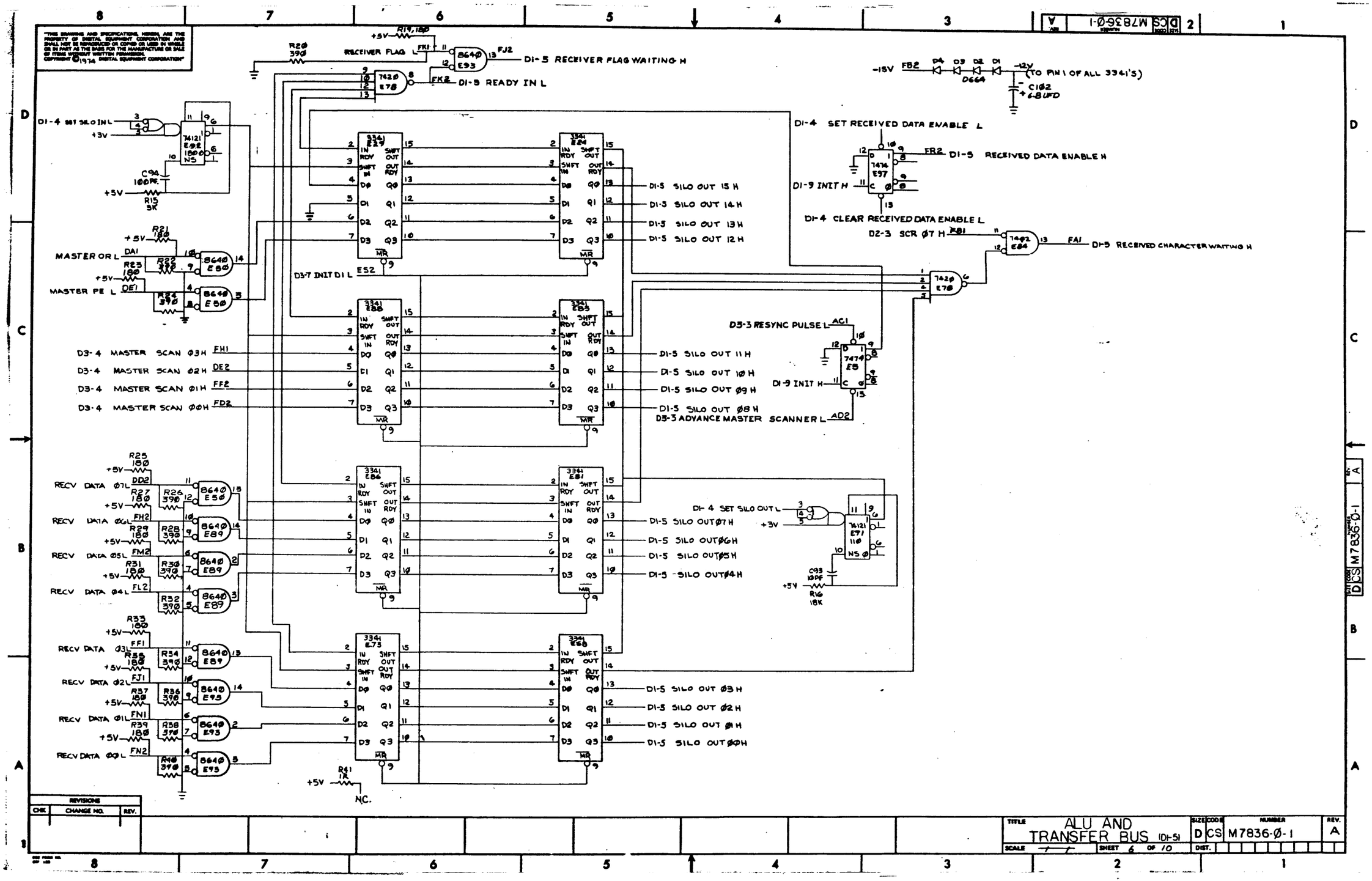
D3-2 TRANSFER SOURCE ENAB L DK2
DI-3 BUF ROM DATA Ø7 H
7432 E55

D3-3 SET/CLEAR Ø4 L FU2
DI-2 BUF ROM DATA Ø2 H
DI-2 BUF ROM DATA Ø1 H
DI-2 BUF ROM DATA ØØ H
STBB STBA 74155 E95
FB3 DI-4 SET ALU Ø2 L
FB2 FP1 DI-4 CLEAR ALU Ø2 L
FB1 FT2 DI-4 CLEAR ALU Ø1 L
FBØ FS2 DI-4 CLEAR ALU RESULT HIGH BYTE L
FA3 DI-4 SET SILO OUT L
FA2 DI-4 SET SILO IN L
FA1 DI-4 CLEAR RECEIVED DATA ENABLE L
FAØ DI-4 SET RECEIVED DATA ENABLE L

REVISIONS

CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
ALU AND TRANSFER BUS (DI-4)	D	DCS	M7836-Ø-1	A
SCALE	SHEET 5 OF 10	DIST.		



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RECEIVER FLAG L
D1-5 RECEIVER FLAG WAITING H
D1-5 READY IN L
D1-4 SET SILO IN L
MASTER OR L
MASTER PE L
D3-4 MASTER SCAN Ø3H
D3-4 MASTER SCAN Ø2H
D3-4 MASTER SCAN Ø1H
D3-4 MASTER SCAN ØØH
RECV DATA Ø7L
RECV DATA Ø6L
RECV DATA Ø5L
RECV DATA Ø4L
RECV DATA Ø3L
RECV DATA Ø2L
RECV DATA Ø1L
RECV DATA ØØL
D1-5 SILO OUT 15 H
D1-5 SILO OUT 14 H
D1-5 SILO OUT 13 H
D1-5 SILO OUT 12 H
D3-7 INIT D1 L
D1-5 SILO OUT 11 H
D1-5 SILO OUT 1Ø H
D1-5 SILO OUT Ø9 H
D1-5 SILO OUT Ø8 H
D3-3 ADVANCE MASTER SCANNER L
D1-4 SET SILO OUT L
D1-5 SILO OUT Ø7 H
D1-5 SILO OUT Ø6 H
D1-5 SILO OUT Ø5 H
D1-5 SILO OUT Ø4 H
D1-5 SILO OUT Ø3 H
D1-5 SILO OUT Ø2 H
D1-5 SILO OUT Ø1 H
D1-5 SILO OUT ØØH
D1-4 SET RECEIVED DATA ENABLE L
D1-5 RECEIVED DATA ENABLE H
D1-9 INIT H
D1-4 CLEAR RECEIVED DATA ENABLE L
D2-3 SCR Ø7 H
D1-5 RECEIVED CHARACTER WAITING H
D3-3 RESYNC PULSE L
D1-9 INIT H
-15V
-12V (TO PIN 1 OF ALL 3341'S)
C1Ø2 6.8UFD
D664
N.C.
REVISIONS
CHK
CHANGE NO.
REV.
TITLE ALU AND TRANSFER BUS (D1-5)
SIZE D
CODE CS
NUMBER M7836-Ø-1
REV. A
SCALE
SHEET 6 OF 10
DIST.

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DI-2 REG A Ø H
DI-1 REG B Ø H → 7486 E56 → DI-6 LRC ØØ H

DI-2 REG A 1 H
DI-1 REG B 1 H → 7486 E56 → DI-6 LRC Ø1 H

DI-2 REG A 2 H
DI-1 REG B 2 H → 7486 E56 → DI-6 LRC Ø2 H

DI-2 REG A 3 H
DI-1 REG B 3 H → 7486 E56 → DI-6 LRC Ø3 H

DI-2 REG A 4 H
DI-1 REG B 4 H → 7486 E64 → DI-6 LRC Ø4 H

DI-2 REG A 5 H
DI-1 REG B 5 H → 7486 E64 → DI-6 LRC Ø5 H

DI-2 REG A 6 H
DI-1 REG B 6 H → 7486 E64 → DI-6 LRC Ø6 H

DI-2 REG A 7 H
DI-1 REG B 7 H → 7486 E64 → DI-6 LRC Ø7 H

DI-1 REG B 11 H → 7486 E42 → 7486 E39 → DI-6 CRC16-Ø6 H
7486 E39 → DI-6 CRC16-Ø7 H
7486 E39 → DI-6 CRC16-Ø8 H
7486 E39 → DI-6 CRC16-Ø9 H
7486 E34 → DI-6 CRC16-1Ø H
7486 E34 → DI-6 CRC16-11 H
7486 E34 → DI-6 CRC16-12 H
7486 E34 → DI-6 CRC16-13 H
7486 E44 → DI-6 CRC-CCITT 12 H
DI-1 REG B 8 H → 7486 E44 → DI-6 CRC-CCITT 13 H
DI-1 REG B9 H → 7486 E44 → DI-6 CRC-CCITT 14 H
DI-1 REG B1Ø H → 7486 E44 → DI-6 CRC-CCITT 15 H
DI-1 REG B 14 H → 7486 E48 → DI-6 CRC-CCITT Ø6 H
DI-1 REG B13 H → 7486 E48 → DI-6 CRC-CCITT Ø5 H
DI-1 REG B12 H → 7486 E48 → DI-6 CRC-CCITT Ø4 H

7486 E42 → DI-6 CRC16-Ø7 H
7486 E47 → 7486 E47 → DI-6 CRC16-14 H
7486 E33 → 7486 E42 → DI-6 CRC16-15 H
DI-6 CRC16-13 H
7486 E47 → DI-6 CRC16-ØØ H
7486 E43 → DI-6 CRC-CCITT ØØ H
7486 E43 → DI-6 CRC-CCITT Ø1 H
7486 E43 → DI-6 CRC-CCITT Ø2 H
7486 E48 → DI-6 CRC-CCITT Ø3 H
7486 E43 → DI-6 CRC-CCITT Ø7 H
7486 E47 → DI-6 CRC-CCITT Ø8 H
7486 E33 → DI-6 CRC-CCITT Ø9 H
7486 E33 → DI-6 CRC-CCITT 1Ø H
7486 E48 → DI-6 CRC-CCITT Ø5 H
7486 E48 → DI-6 CRC-CCITT Ø4 H

REVISIONS

CHK	CHANGE NO.	REV.

TITLE: ALU AND TRANSFER BUS (DI-6)
SIZE: D | CODE: CS | NUMBER: M7836-Ø-1 | REV: A
SCALE: — | SHEET 7 OF 10 | DIST.

DCS M7836-Ø-1 A

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74153 E49 1/2 f1
DI-6 CRC-CCITT Ø1 H
DI-6 REG B Ø9 H
DI-6 LRC Ø1 H

74153 E53 1/2 f1
DI-6 CRC-CCITT Ø3 H
DI-6 REG B 11 H
DI-6 LRC Ø3 H

74153 E54 1/2 f1
DI-6 CRC-CCITT Ø5 H
DI-6 REG B 13 H
DI-6 LRC Ø5 H

74153 E38 1/2 f1
DI-6 CRC-CCITT Ø7 H
DI-6 CRC-16 Ø7 H
DI-6 LRC Ø7 H

74153 E49 1/2 fØ
DI-6 CRC-CCITT ØØ H
DI-6 CRC-16 ØØ H
DI-6 LRC ØØ H

74153 E53 1/2 fØ
DI-6 CRC-CCITT Ø2 H
DI-6 REG B 10 H
DI-6 LRC Ø2 H

74153 E54 1/2 fØ
DI-6 CRC-CCITT Ø4 H
DI-6 REG B 12 H
DI-6 LRC Ø4 H

74153 E38 1/2 fØ
DI-6 CRC-CCITT Ø6 H
DI-6 CRC-16 Ø6 H
DI-6 LRC Ø6 H

D3-11 RAM CD2 3 OUTPUT Ø4H
74Ø4 E38
+3V
7437 E79

74174 E59
DØ R0(1) — DI-7 BCC Ø5 H
D1 R1(1) — DI-7 BCC Ø4 H
D2 R2(1) — DI-7 BCC Ø3 H
D3 R3(1) — DI-7 BCC Ø2 H
D4 R4(1) — DI-7 BCC Ø1 H
D5 R5(1) — DI-7 BCC ØØ H
CLR CLK

74157 E37
DI-6 CRC-16 Ø8 H / DI-6 CRC-CCITT Ø8 H
DI-6 CRC-16 Ø9 H / DI-6 CRC-CCITT Ø9 H
DI-6 CRC-16 1Ø H / DI-6 CRC-CCITT 1Ø H
DI-6 CRC-1611 H / DI-6 LRC Ø3 H
STB SØ

D3-11 RAM OUTPUT Ø3 L — DV2 1 — 74Ø4 E65 — 2

74157 E32
DI-6 CRC 16 12 H / DI-6 CRC-CCITT 12 H
DI-6 CRC 16 13 H / DI-6 CRC-CCITT 13 H
DI-6 CRC-16 14 H / DI-6 CRC-CCITT 14 H
DI-6 CRC-16 15H / DI-6 CRC-CCITT 15 H
STB SØ

74174 E36
D5 R5(1) — DI-7 BCC Ø8 H
D4 R4(1) — DI-7 BCC Ø9 H
D3 R3(1) — DI-7 BCC 1Ø H
D2 R2(1) — DI-7 BCC 11 H
D1 R1(1) — DI-7 BCC 12 H
DØ RØ(1) — DI-7 BCC 13 H
CLR CLK

74175 E31
D3 R3(1) R3(Ø) — DI-7 BCC 14 H
D2 R2(1) R2(Ø) — DI-7 BCC 15 H
D1 R1(1) R1(Ø) — DI-7 BCC Ø6 H
DØ RØ(1) RØ(Ø) — DI-7 BCC Ø7 H
CLR CLK

D3-7 INIT DI L (ES2)
D3-7 DATA STROBE L FE1
D3-2 BCC CALCULATION L FC1
74Ø2 E84

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
ALU AND TRANSFER BUS (DI-7)	D	CS	M7836-Ø-1	A
SCALE —	SHEET 8 OF 10	DIST.		

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D3-2 ROM DATA Ø9 H
D3-2 ROM DATA Ø8 H
DI-4 TRANSFER BUS 17 H
DI-4 TRANSFER BUS 16 H
DI-9 BUF INIT L
D3-6 NPR ADDRESS REGISTER CLOCK L
DI-4 TRANSFER BUS 15 H
DI-4 TRANSFER BUS 14 H
DI-4 TRANSFER BUS 13 H
DI-4 TRANSFER BUS 12 H
DI-4 TRANSFER BUS 11 H
DI-4 TRANSFER BUS 10 H
DI-4 TRANSFER BUS Ø9 H
DI-4 TRANSFER BUS Ø8 H
DI-3 TRANSFER BUS Ø7 H
DI-3 TRANSFER BUS Ø6 H
D3-7 INIT DI L
DI-3 TRANSFER BUS Ø5 H
DI-3 TRANSFER BUS Ø4 H
DI-3 TRANSFER BUS Ø3 H
DI-3 TRANSFER BUS Ø2 H
DI-3 TRANSFER BUS Ø1 H
DI-3 TRANSFER BUS ØØ H

74175 E4
74175 E9
74174 E27
74174 E35
7404 E5Ø
8838 E3
8838 E2Ø
8838 E15
8838 E25
D2-7 ADDRESS TO BUS L
DI-8 NPR ADDRØØ H

DI-8 C1 H
DI-8 BUS C1 L
DI-8 C0 H
DI-8 BUS C0 L
DI-8 A17 H
DI-8 BUS A17 L
DI-8 BUS A12 L
DI-8 BUS A11 L
DI-8 BUS A10 L
DI-8 BUS A09 L
DI-8 BUS A08 L
DI-8 BUS A07 L
DI-8 BUS A06 L
DI-8 BUS A05 L
DI-8 BUS A04 L
DI-8 BUS A03 L
DI-8 A03 H
DI-8 BUS A02 L
DI-8 A02 H
DI-8 BUS A01 L
DI-8 A01 H
DI-8 BUS A00 L
DI-8 A00 H

DI-8 BUS A16 L
DI-8 BUS A15 L
DI-8 BUS A14 L
DI-8 BUS A13 L
DI-8 ADDRESS SELECTED H
8881 E8
8640 E13
8242 E7

S1-1 R6 1K
S1-2 R7 1K
S1-3 R8 1K
S1-4 R9 1K
S1-5 R10 1K
S1-6 R11 1K
S1-7 R12 1K
S1-8 R13 1K
S1-9 R14 1K
+5V
R4 1K

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE: ALU AND TRANSFER BUS (DI-8)
SIZE: D | CODE: DCS | NUMBER: M7836-Ø-1 | REV: A
SCALE: — | SHEET 9 OF 10 | DIST.

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BUS PB L AN2 — 8640 E13
BUS PA L AM1 — 8640 E13

74Ø8 E94 — DI-9 MEM PAR ERR H

74157 E1
D2-3 BUF DATAØØH AK2 — AØ
D2-3 BUF DATAØ8H AJ2 — BØ
D2-3 BUF DATA Ø1 H AH2 — A1
D2-3 BUF DATA Ø9H AF1 — B1
D2-3 BUF DATAØ2H AE2 — A2
D2-3 BUF DATA 1Ø H AF2 — B2
D2-3 BUF DATA Ø3 H AH1 — A3
D2-3 BUF DATA 11 H AE1 — B3
STB SØ
ØØ, Ø1, Ø2, Ø3

74175 E28
D3 R3(1) R3(Ø)
D2 R2(1) R2(Ø)
D1 R1(1) R1(Ø) — DI-9 NPR DATI Ø2 H
DØ RØ(1) RØ(Ø) — DI-9 NPR DATI Ø3 H
CLR CLK

DI-8 NPR ADDR ØØ H CH2

74157 E40
D2-3 BUF DATA Ø4 H CS2 — AØ
D2-3 BUF DATA 12 H CR2 — BØ
D2-3 BUF DATA Ø5 H CP2 — A1
D2-3 BUF DATA 13 H CN2 — B1
D2-3 BUF DATA Ø6 H CL2 — A2
D2-3 BUF DATA 14 H CK2 — B2
D2-3 BUF DATA Ø7 H CJ2 — A3
D2-3 BUF DATA 15 H CM2 — B3
STB SØ
Ø4, Ø5, Ø6, Ø7

74174 E45
D4 R4(1) — DI-9 NPR DATI ØØ H
DI R1(1) — DI-9 NPR DATI Ø1 H
D5 R5(1) — DI-9 NPR DATI Ø4 H
D3 R3(1) — DI-9 NPR DATI Ø5 H
D2 R2(1) — DI-9 NPR DATI Ø6 H
DØ RØ(1) — DI-9 NPR DATI Ø7 H
CLR CLK

D3-7 DATA STROBE H CT2

74Ø4 E14 — 74Ø2 E84 — DI-9 BUF INIT L
DI-9 INIT H

74175 E82
DI-4 TRANSFER BUS ØB H — D3 R3(1) R3(Ø) — DI-9 NPR DATO Ø8 H
DI-4 TRANSFER BUS Ø9 H — D2 R2(1) R2(Ø) — DI-9 NPR DATO Ø9 H
DI-4 TRANSFER BUS 1Ø H — D1 R1(1) R1(Ø) — DI-9 NPR DATO 1Ø H
DI-4 TRANSFER BUS 11 H — DØ RØ(1) RØ(Ø) — DI-9 NPR DATO 11 H
CLR CLK

74175 E19
DI-4 TRANSFER BUS 12 H — D3 R3(1) R3(Ø) — DI-9 NPR DATO 12 H
DI-4 TRANSFER BUS 13 H — D2 R2(1) R2(Ø) — DI-9 NPR DATO 13 H
DI-4 TRANSFER BUS 14 H — D1 R1(1) R1(Ø) — DI-9 NPR DATO 14 H
DI-4 TRANSFER BUS 15 H — DØ RØ(1) RØ(Ø) — DI-9 NPR DATO 15 H
CLR CLK

D3-7 INIT D1 L ES2

D3-6 NPR DATO REGISTER CLOCK L AU1 — 74Ø4 E15

REVISIONS
CHK | CHANGE NO. | REV.

TITLE ALU AND TRANSFER BUS (D1-9)
SIZE D | CODE CS | NUMBER M7836-Ø-1 | REV. A
SCALE — | SHEET 10 OF 10 | DIST.

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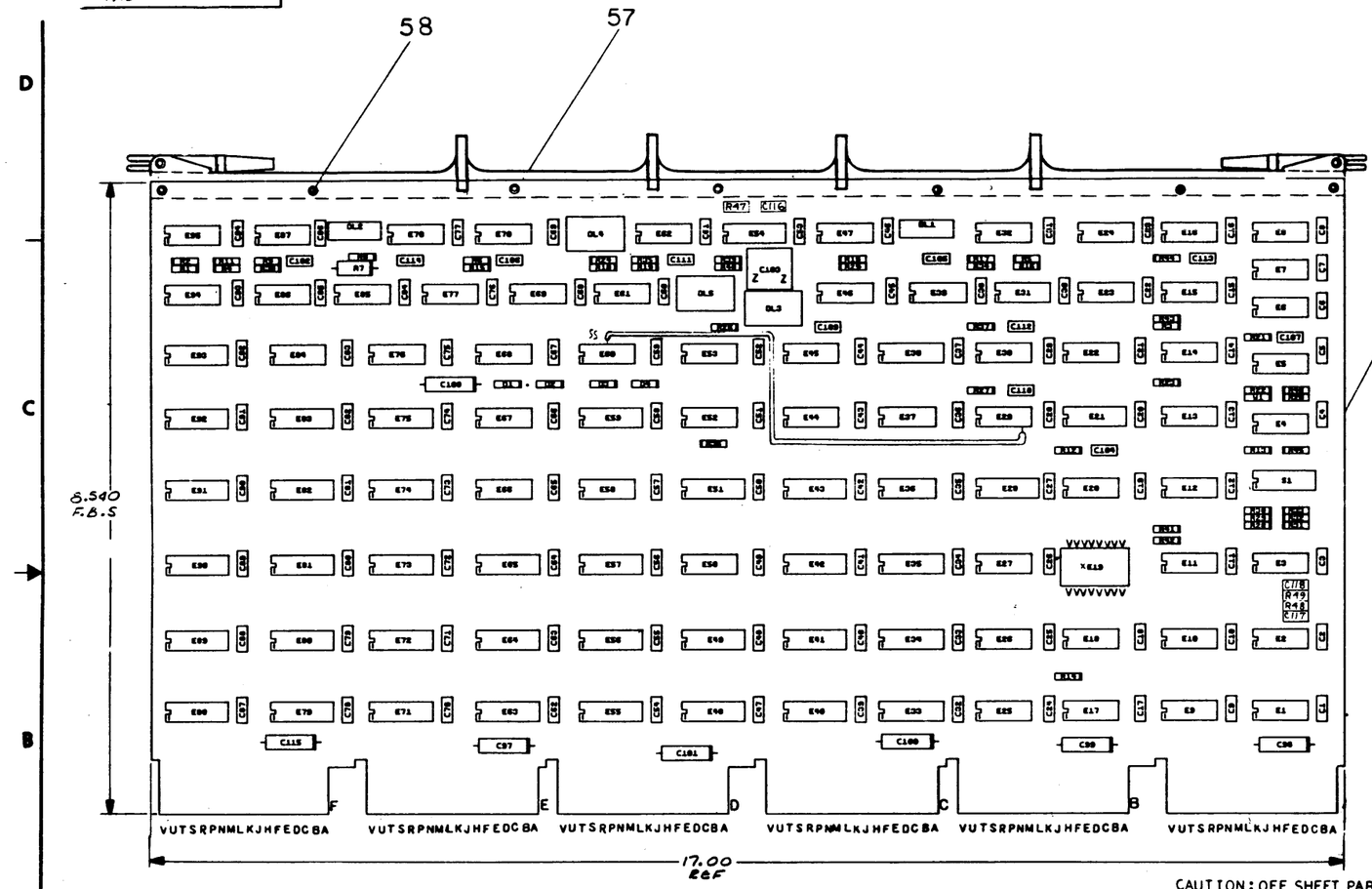
NOTES: R47, R48, R49, C116, C117, C118 ARE ECO #2 ADDITIONS.



CAUTION: OFF SHEET PARTS LIST. SEE K-PL-M7837-0-0.

REF		X-Y COORDINATE HOLE LOCATION	K-CO-M7837-04	1
REF		ASS'Y/DRILLING HOLE LAYOUT	D-AH-M7837-0-1	2
REF		MODULE ECO HISTORY	B-MH-M7837-0-1	3
1		ETCHED CIRCUIT BOARD	5010977	4
3	C104, C110, C111	CAP 10 PF 100V 5%	1000006	5
5	C109, C106, C112, C102, C107	CAP 100 PF 100V 5%	1000016	6
3	C113, C117, C118	CAP 330 PF 100V 5%	1000023	7
2	C105, C116	CAP 470 PF 100V 5%	1000024	8
1	C103	CAP 1500 PF 100V 5%	1002428	9
94	C1 – C96	CAP .01 UF 100V 20%	1001610-01	10
7	C97–C101, C108, C115	CAP 6.8 UF 35V 10%	1005306	11
4	D1–D4	DIODE DG64	1100114	12
9	E8, E12, E22, E53, E60, E66 E67, E77, E84.	I.C DEC 7474	1905547	13
3	E15, E69, E86	I.C DEC 7400	1905575	14
1	E68	I.C DEC 7410	1905576	15
6	E6, E13, E24, E31, E46, E96	I.C DEC 7402	1909004	16
1	E76	I.C DEC 74H55	1909063	17
7	E9, E7, E18, E25, E26, E27, E32	I.C DEC 8640	1911969	18
2	E61, E95	I.C DEC 74S74	1910544	19
3	E16, E44, E50	I.C DEC 7404	1909686	20
8	E1, E2, E3, E9, E10, E11 E14, E17	I.C DEC 8881	1909705	21
16	E71, E72, E73, E74, E75 E79, E80, E81, E82, E83 E88, E89, E90, E91, E92, E93	I.C DEC 74151	1909936	22
1	E38.	I.C DEC 7442	1910046	23
1	E51	I.C DEC 7015	1910087	24
2	E37, E58	I.C DEC 7437	1910091	25
4	E23, E47, E52, E85	I.C DEC 7408	1910155	26
9	E5, E20, E29, E30, E63 E62, E70, E78, E87	I.C DEC 74121	1910230	27
7	E28, E34, E40, E48, E56, E59, E	I.C DEC 74175	1910651	28
3	E33, E64, E66	I.C DEC 74174	1910652	29
4	E35, E41, E42, E43	I.C DEC 74157	1910655	30
1	E49	I.C DEC 74155	1910656	31
1	E54	I.C DEC 74123	1910836	32
14	R28, R29, R30, R31, R32, R33, R35 R11, R24, R15, R18, R19, R22, R36	RES 1K 1/4W 5%	1300363	33
1	R37	RES 3K 1/4 W 5%	1300632	34
1	R17	RES 3.3K 1/4 W 5%	1300679	35
1	R34	RES 10K 1/4 W 5%	1300879	36
QTY	REF. DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

I.C DEC 74151	8	16
I.C DEC 7442	8	16
I.C DEC 7015	8	16
I.C DEC 74175	8	16
I.C DEC 74174	8	16
I.C DEC 74157	8	16
I.C DEC 74155	8	16
I.C DEC 74123	8	16
IC TYPE	GND	+5V

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

REV	CHANGE NO.	REVISIONS	
J	M7837-NK007	15-NOV-81	W. SMITH
H	M7837-00006	10-APR-78	R. HARRINGTON
G	M7837-00005	12-SEP-77	J. MCNAMARA
F	M7837-00004	11-NOV-76	J. MCNAMARA
E	M7837-00003	6-2-76	J.M. NAMARA
D	M7837-00002	5-26-76	J MCNAMARA
C	M7837-00001	5-16-76	J. MCNAMARA
B	ORIGINATED	5-2-76	
A			

SEMICONDUCTOR CONVERSION CHART

DEC NO.	EIA NO.	DEC NO.	EIA NO.

FIRST USED ON OPTION MODEL: DV11-AA

ETCH BOARD REV. B

DRN	Diane Swift	DATE 1/24/75
CHKD		DATE 2/11/75
ENG		DATE 3-10-75
PROJ. ENG		DATE 3-10-75
PROD.		DATE 3-10-75

NEXT HIGHER ASSY: B-DD-DV11-0

SCALE: 1=1

SHEET 1 OF 11

digital

TITLE: UNIBUS DATA AND NPR CONTROL

SIZE	CODE	NUMBER	REV.
D	CS	M7837-0-1	J

OBJ.

M7837-0-1 D CS J

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5	R3,R45,R14,R46,R23	RES 180Ω 1/4 W 5%	1301322	37
3	R2,R39,R42	RES 750Ω 1/4W 5%	1301401	38
3	R43,R13,R20	RES 390Ω 1/4 W 5%	1300309	39
1	R7	RES 2.21K, 1/2W, 1% RN60	1312404	40
1	R35	RES 18K 1/4 W 5%	1302465	41
2	R6, R9	RES 2.74K 1/4 W 1% RN55	1304868	42
1	R26	RES 4.7K 1/4 W 5%	1300447	43
3	R44,R48,R49	RES 820Ω 1/4W 5%	1300271	44
1	R16	RES 100Ω 1/4W 5%	1300229	45
5	R1,R40,R41,R5,R8	RES 330Ω 1/4W 5%	1300295	46
2	R27, R12	RES 6.8K 1/4W 5%	1301423	47
2	R4, R38	RES 470Ω 1/4W 5%	1300316	48
1	R10	RES 47K 1/4 W 5%	1302177	49
1	R21	RES 1.5K 1/4 W 5%	1300391	50
1		SWITCH RKR COVER, 8 POS	1211284-04	51
1	E19	SOCKET GLASS	1209838	52
1	S1	SWITCH ROCKER DIP	1211164-04	53
2	DL1, DL2	DELAY LINE 30NS	1605528-01	54
2	DL4, DL5	DELAY LINE 50NS	1609428	55
1	DL3	DELAY LINE 100NS	1609559	56
1		HANDLE HEX	1210711-02	57
12		EYELET	9006732	58
1	W1	JUMPER INSULATED	9009185	59
1	E21	I.C DEC 74193	1910018	60
2	E55, E57	I.C DEC 3341	2111188	61
1	C114	CAP, 68PF, 100V, 5%	1000014	62
2	E35,E46	I.C. DEC 7432	1911521	63
A/R		WIRE, #30 AWG INSULATED	9105740	64
1	R47	RES 15KΩ 1/4W 5%	1300496	65

CAUTION:
OFF SHEET PARTS LIST.
SEE K-PL-M7837-Ø-2.

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE UNIBUS DATA AND NPR CONTROL

SIZE D CODE CS NUMBER M7837-Ø-1 REV. J

SCALE — SHEET 2 OF 11 DIST.

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D2-1 DATA FOR BUS ØØ H
D2-4 SCR ØØ H
D2-9 RICR ØØ H
D3-2 BRANCH A L
D3-F SRS ØØH
D3-9 RAM UNIDATAØØ H
D3-2 ROM DATA ØØH
D2-9 NPR STATUS ØØ H
D2-3 RIRR ØØ H
STB 74151 E79
DI-6 AØ3 H CU2
7437 E37
D2-1 DATA SOURCE C L

D2-1 DATA FOR BUS Ø3H
D2-4 SCR Ø3 H
D2-9 RICR Ø3 H
D3-8 SRS Ø3 H
D3-9 RAM UNIDATAØ3 H
D3-2 ROM DATA Ø3 H
D2-9 NPR STATUS Ø3 H
D2-3 RIRR Ø3 H
STB 74151 E71

D2-1 DATA FOR BUS Ø6 H
D2-4 SCR Ø6 H
D2-9 RICR Ø6 H
D3-9 RAM UNIDATA Ø6H
D3-2 ROM DATA Ø6H
D2-3 RIRR Ø6H
STB 74151 E93

D2-1 DATA FOR BUS Ø9 H
D2-4 SCR Ø9 H
D2-9 RICR Ø9 H
D2-3 LCR Ø9 H
D3-8 SRS Ø9 H
D3-10 RAM UNI DATA Ø9 H
D3-2 ROM DATA Ø9 H
D2-9 NPR STATUS Ø9 H
STB 74151 E7d

D2-1 DATA FOR BUS Ø1H
D2-4 SCR Ø1 H
D2-9 RICR Ø1 H
D3-2 BRANCH B L
D3-8 SRS Ø1 H
D3-9 RAM UNIDATA Ø1H
D3-2 ROM DATA Ø1 H
D2-9 NPR STATUS Ø1 H
D2-3 RIRR Ø1 H
STB 74151 E83
DI-8 AØ2 H CS1
7437 E37
D2-1 DATA SOURCE B L

D2-1 DATA BUS Ø4 H
D2-4 SCR Ø4H
D2-9 RICR Ø4 H
D3-10 RAM UNI DATA 16 H
D3-9 RAM UNI DATAØ4 H
D3-2 ROM DATA Ø4 H
D2-3 RIRR Ø4H
STB 74151 E80

D2-1 DATA FOR BUS Ø7 H
D2-4 SCR Ø7H
D2-9 RICR Ø7 H
D2-3 LCR Ø7 H
D3-9 RAM UNIDATA Ø7 H
D3-2 ROM DATA Ø7H
D2-3 RIRR Ø7 H
STB 74151 E92

D2-1 DATA FOR BUS Ø2 H
D2-4 SCR Ø2 H
D2-9 RICR Ø2 H
D3-8 SRS Ø2 H
D3-9 RAM UNIDATAØ2 H
D3-2 ROM DATA Ø2 H
D2-9 NPR STATUS Ø2 H
D2-3 RIRR Ø2 H
STB 74151 E72
DI-8 AØ1 H CM2
7437 E37
D2-1 DATA SOURCE A L

D2-1 DATA FOR BUS Ø5H
D2-4 SCR Ø5H
D2-9 RICR Ø5H
D3-10 RAM UNI DATA 17 H
D3-9 RAM UNIDATA Ø5 H
D3-2 ROM DATA Ø5 H
D2-3 RIRR Ø5 H
STB 74151 E94

D2-1 DATA FOR BUS Ø8 H
D2-4 SCR Ø8H
D2-9 RICR Ø8 H
D2-3 LCR Ø8H
D3-8 SRS Ø8H
D3-9 RAM UNIDATA Ø8H
D3-2 ROM DATA Ø8H
D2-9 NPR STATUS Ø8H
STB 74151 E73

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE UNIBUS DATA & NPR CONTROL (D2-1)
SIZE D CODE CS NUMBER M7837-Ø-1 REV. J
SCALE — SHEET 3 OF 11 DIST.
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DCSM7837-Ø-1 J

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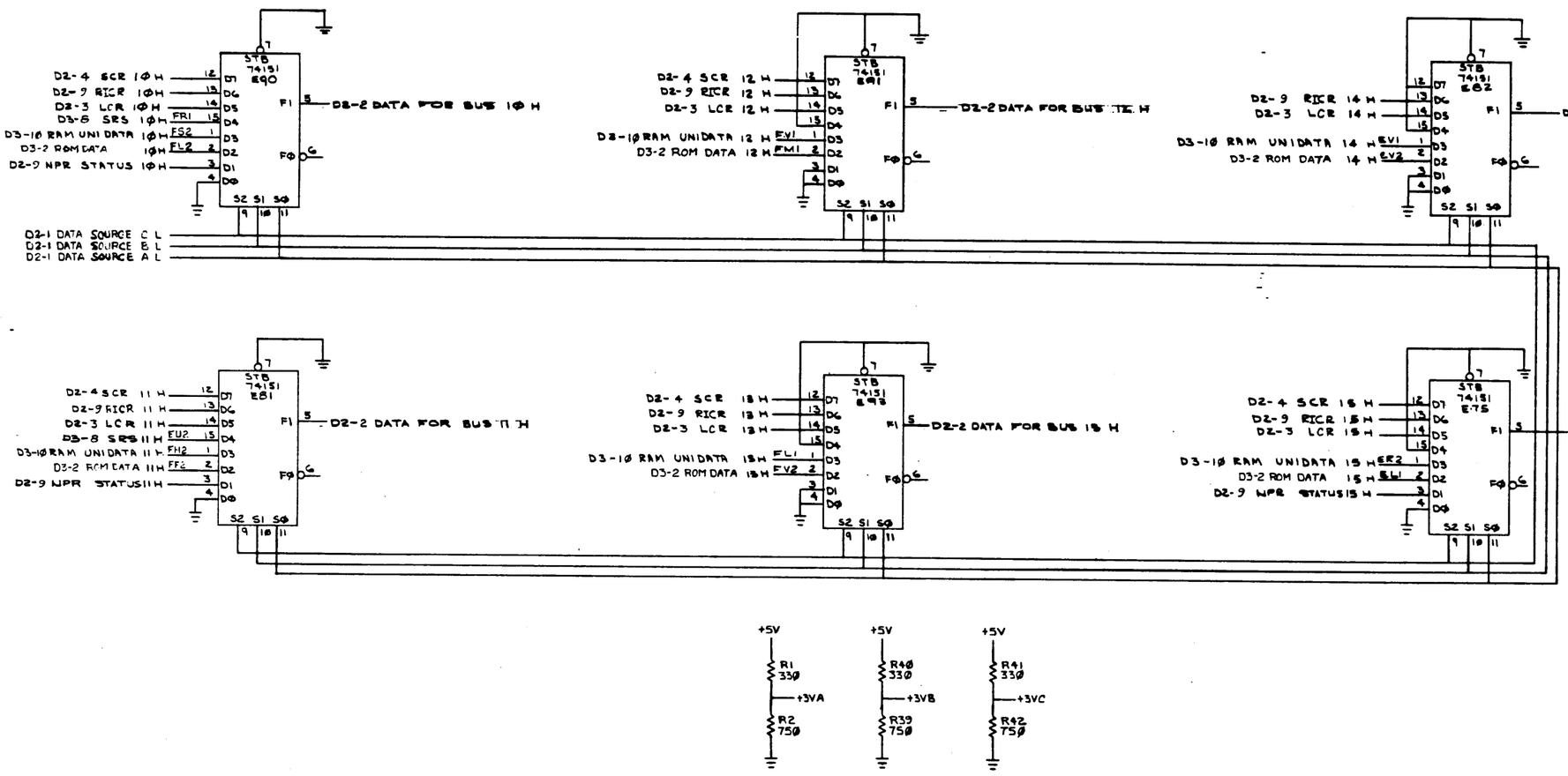

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	UNIBUS DATA & NPR CONTROL (D2-2)	SIZE/CODE	NUMBER / REV.
		D	CS M7837-Ø-1 J
SCALE	1/1 SHEET 4 OF 11	DIST.	MK

CS M7837-Ø-1 J

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D2-6 BUS D15 L
D2-5 LOAD LCR H
D2-6 BUS D14 L
D2-9A BUFFERED INIT D2 L
D2-6 BUS D13 L
D2-6 BUS D12 L
D2-6 BUS D11 L
D2-6 BUS D10 L
D2-6 BUS D09 L
D2-6 BUS D08 L
D3-5 9600 BAUD
D2-3 LCR 15 H
R26 4.7K +5V
DMI D2-3 CONTCOL STROBE H
C199 100PF
D2-3 LCR 14 H
D2-3 LCR 13 H
D2-3 LCR 12 H
D2-3 LCR 11 H
D2-3 LCR 10 H
D2-3 LCR 09 H
D2-3 LCR 08 H
D3-5 230.4 KB H
BMI
D2-3 MAINTENANCE CLK PULSE H
BR2 D2-3 BUF DATA 15 H
CF2 D2-3 BUF DATA 14 H
CE1 D2-3 BUF DATA 13 H
CB2 D2-3 BUF DATA 12 H
BR1 D2-3 BUF DATA 11 H
CD1 D2-3 BUF DATA 10 H
CF1 D2-3 BUF DATA 09 H
BS1 D2-3 BUF DATA 08 H

BIT WINDOW L AVI
D2-3 LCR 07 H
D2-6 BUS D07 L
D2-6 BUS D06 L
D2-6 BUS D05 L
D2-6 BUS D04 L
D2-6 BUS D03 L
D2-6 BUS D02 L
D2-6 BUS D01 L
D2-6 BUS D00 L
D3-2 SET CLEAR 03 L DH2
D3-2 ROM DATA 02 H
D3-2 ROM DATA 01 H
D3-2 ROM DATA 00 H
D2-5 LOAD RIRR H
ED1 D2-3 BUF DATA 04 H
BV2 D2-3 BUF DATA 05 H
BT2 D2-3 BUF DATA 06 H
3S2 D2-3 BUF DATA 07 H
EF2 D2-3 BUF DATA 00 H
EH2 D2-3 BUF DATA 01 H
BH1 D2-3 BUF DATA 02 H
BE1 D2-3 BUF DATA 03 H
D2-3 RIEE 07 H
D2-3 RIEE 06 H
D2-3 RIEE 05 H
D2-3 RIEE 04 H
D2-3 SET RECEIVER INTERRUPT L
D2-3 SET SCR 10 L
D2-3 SET RICE 14 L
D2-3 SET EICE 15 L
D2-3 CLEAR NXM L
D2-3 CLEAR SCE 08 L
D2-3 SET RICE 12 L
D2-3 SET EICE 13 L
D2-3 RIEE 03 H
D2-3 RIEE 02 H
D2-3 RIEE 01 H
D2-3 RIEE 00 H

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
UNIBUS DATA AND NPR CONTROL (D2-3)	D	CS	M7837-0-1	J
SCALE	SHEET 5 OF 11	DIST.	MK	

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D2-3 BUF DATA Ø3 H — 74175 E63 D3 — R3(1) — D2-4 SCR Ø3 H (SOURCE SELECT)
R3(0) — D2-4 SCR Ø3 L
D2-3 BUF DATA Ø2 H — D2 — R2(1) — D2-4 SCR Ø2 H (BRANCH DISABLE)
R2(0)
D2-3 BUF DATA Ø4 H — D1 — R1(1) — D2-4 SCR Ø4 H (MEMEX A16)
R1(0)
D2-3 BUF DATA ØØ H — DØ — RØ(1) — D2-4 SCR ØØ H (MICROPROCESSOR GO)
RØ(0)
CLR CLK

D2-9 B BUFFERED INIT D2 L

D2-3 BUF DATA Ø1 H — 7474 E66 — FP1 — D2-4 SCR Ø1 H (ROM SINGLE STEP)
D3-7 Ø1 L — 7400 E28
FN2 — D2-4 SCR Ø5 H (MEMEX A17)
D2-3 BUF DATA Ø5 H — 7474 E67
D2-3 BUF DATA Ø6 H — 7474 E67 — D2-4 SCR Ø6 H (RECV INTR ENAB)
D2-3 SET RECEIVER INTERRUPT L
D2-3 BUF DATA Ø7 H — 7474 E68 — DV1 — D2-4 SCR Ø7 H (RECV INTERRUPT)
D2-5 LOAD SCR LOW BYTE H
7400 E23

D2-3 BUF DATA Ø8 H — 7474 E12 — AV2 — D2-4 SCR Ø8 H (RECV INTERRUPT RESPONSE COMPLETE)
7400 E15 — R44 220Ω — C113 330 PF
7400 E47
D2-3 SET SCR 10Ø L
D2-3 BUF DATA 10 H — 7474 E66 — D2-4 SCR 10 H (NPR STATUS OVERFLOW INTR)

R47 15K — C116 470 PF — +5 — +3
D2-3 CLR SCR Ø8 L — E54 74123 3NS
+3

D2-3 BUF DATA 15 H — 7474 E12
D2-9 NPR STATUS AVAILABLE — 7400 E15 — D2-4 SCR 15 H

7410 E68 — D2-4 B REQUEST H — 7404 E16 — D2-4 B REQUEST L
7400 E69
7410 E68 — 7404 E76 — D2-4 A REQUEST H
D2-4 A REQUEST L

74175 E28
D2-3 BUF DATA 11 H — D3 — R3(1) — BP2 — D2-4 SCR 11 H (MASTER CLEAR)
D2-3 BUF DATA Ø9 H — D2 — R2(1) — D2-4 SCR Ø9 H (SCR15 WRITE ENABLE)
D2-3 BUF DATA 13 H — D1 — R1(1) — D2-4 SCR 13 H (NPR STATUS INTR EN)
D2-3 BUF DATA 12 H — DØ — RØ(1) — D2-4 SCR 12 H (STORAGE INTR EN)
CLK CLR

D2-5 LOAD SCR HIGH BYTE H — 7404 E16
7400 E25 4045 — C110 10PF — +5V — R27 6.8K

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE UNIBUS DATA & NPR CONTROL (D2-4)
SIZE D — CODE DCS — NUMBER M7837-Ø-1 — REV. J
SCALE — SHEET 6 OF 11 — DIST.
MK

DCS M7837-Ø-1 REV J

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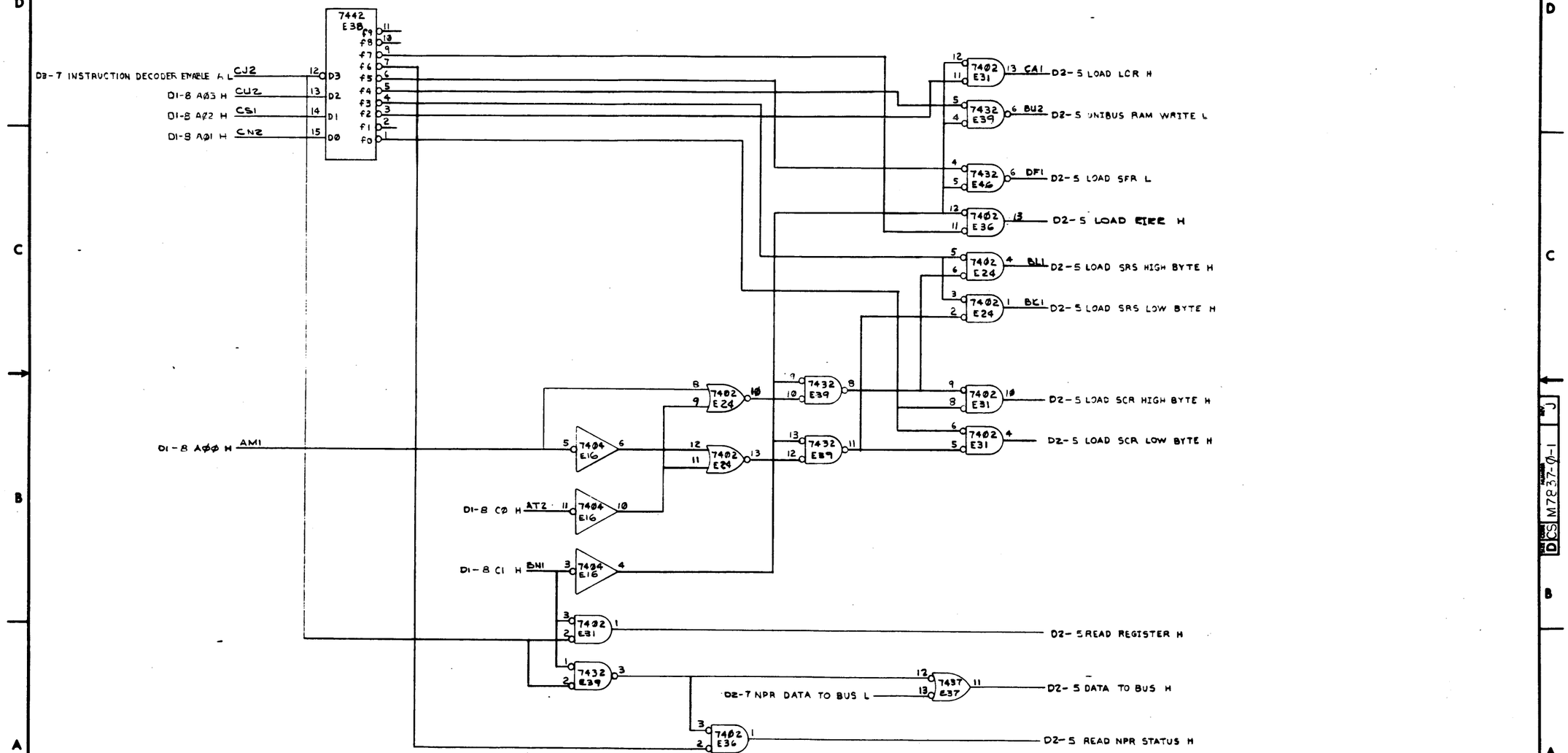

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
UNIBUS DATA AND NPR CONTROL (D2-5)	D	DCS	M7837-Ø-1	J
SCALE NONE	SHEET 7 OF 17	DIST.	MK	

M7837-Ø-1 J DCS

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DI-3 TRANSFER BUS Ø4 H CR2
DI-3 TRANSFER BUS 03 H CN1
DI-3 TRANSFER BUS Ø6 H CP1
DI-3 TRANSFER BUS Ø7 H CC2
74175 E40 — D3 D2 D1 D0 — R3(1) R3(Ø) R2(1) R2(Ø) R1(1) R1(Ø) RØ(1) RØ(Ø) — CLR CLK

CU1 D2-6 NPR DATO Ø7 H
CM1 D2-6 NPR DATO Ø6 H
CM2 D2-6 NPR DATO Ø5 H
CT2 D2-6 NPR DATO Ø4 H
CR1 D2-6 NPR DATO Ø3 H
CH1 D2-6 NPR DATO Ø2 H
CP2 D2-6 NPR DATO Ø1 H
CV1 D2-6 NPR DATO ØØ H

DI-3 TRANSFER BUS ØØ H CH2
DI-3 TRANSFER BUS Ø1 H CK2
DI-3 TRANSFER BUS Ø2 H CK1
DI-3 TRANSFER BUS Ø3 H CL1
74175 E34 — D3 D2 D1 D0 — R3(1) R3(Ø) R2(1) R2(Ø) RØ(1) RØ(Ø) — CLR CLK

D2-9 B BUFFERED INIT D 2 L

D3-6 UPE DATO REG CLK L DJ2 — 7404 E44

DE-2 DATA FOR BUS 15 H
DE-2 DATA FOR BUS 14 H
DE-2 DATA FOR BUS 13 H
DE-2 DATA FOR BUS 12 H
74157 E42 — B3 A3 B2 A2 B1 A1 BØ AØ — F3 F2 F1 FØ — STB SØ

7402 E36

D2-2 DATA FOR BUS 11 H
D2-2 DATA FOR BUS 10 H
D2-1 DATA FOR BUS Ø9 H
D2-1 DATA FOR BUS Ø8 H
74157 E35 — B3 A3 B2 A2 B1 A1 BØ AØ — F3 F2 F1 FØ — STB SØ

DE-1 DATA FOR BUS Ø7 H
DE-1 DATA FOR BUS Ø6 H
DE-1 DATA FOR BUS Ø5 H
DE-1 DATA FOR BUS Ø4 H
74157 E43 — B3 A3 B2 A2 B1 A1 BØ AØ — F3 F2 F1 FØ — STB SØ

DE-5 READ REGISTER H
7402 E36

DI-8 NPR ADDR ØØ H CC1
7404 E44

DE-1 DATA FOR BUS Ø3 H
DE-1 DATA FOR BUS Ø2 H
DE-1 DATA FOR BUS Ø1 H
DE-1 DATA FOR BUS ØØ H
74157 E41 — B3 A3 B2 A2 B1 A1 BØ AØ — F3 F2 F1 FØ — STB SØ

DE-7 NPR DATA TO BUS L

DE-5 DATA TO BUS H

8881 E10 — AM2 D2-6 BUS DI5 L
8881 E10 — AL1 D2-6 BUS DI4 L
8881 E10 — AL2 D2-6 BUS DI3 L
8881 E10 — AK1 D2-6 BUS DI2 L
8881 E9 — AK2 D2-6 BUS DI1 L
8881 E9 — AJ1 D2-6 BUS DI0 L
8881 E9 — AJ2 D2-6 BUS DØ9 L
8881 E9 — AH1 D2-6 BUS DØ8 L
8881 E11 — AH2 D2-6 BUS DØ7 L
8881 E11 — AF1 D2-6 BUS DØ6 L
8881 E2 — AF2 D2-6 BUS DØ5 L
8881 E2 — AE1 D2-6 BUS DØ4 L
8881 E3 — AE2 D2-6 BUS DØ3 L
8881 E3 — AD1 D2-6 BUS DØ2 L
8881 E1 — AD2 D2-6 BUS DØ1 L
8881 E1 — AC1 D2-6 BUS DØØ L

+5V R28 1K — 8881 E11 — S1 1 16
+5V R29 1K — 8881 E11 — S1 2 15
+5V R30 1K — 8881 E2 — S1 3 14
+5V R31 1K — 8881 E2 — S1 4 13
+5V R32 1K — 8881 E3 — S1 5 12
+5V R33 1K — 8881 E3 — S1 6 11

D2-8 VECTOR BIT Ø2 H — 8881 E1

DE-8 VECTOR TO BUS L — 7404 E44 — 8881 E1 — AB1 D2-6 BUS INTR L

REVISIONS		
ECR	CHANGE NO.	REV.

TITLE UNIBUS DATA & NPR CONTROL (D2-6)
SIZE D CODE DCS NUMBER M7837-Ø-1 REV. J
SCALE — SHEET 8 OF 11 DIST. MR

J DCS M7837-Ø-1

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+5V R5 330 DL1 30NS R4 470
8640 E32 — 7402 E94 — DE-7 NO BBSY NO SSYN H
D3-7 BUS SSYN L BUI — R16 100 — R17 3.3K — C105 470 PF — R34 10K — D2-7 SSYN H

+5V R8 330 DL2 30NS R38 470 C114 68PF R7 2.21K 1/2W 1%
D3-2 NPR OPERATION L EK1 — D3-7 Ø2 L FJ2 — 7400 E86 — 7408 E85

+3V — 7474 E96 REQ BUS — BF2 D2-7 REQUEST BUS H — 8881 E17 — AS2 D2-7 BUS NPR L

+5V R14 180 — 8881 E17 — BD1 D2-7 BUS NPG OUT H

+3V — 7474 E77 GRANT — 7400 E86 — 7400 E69

+3V — 7474 E77 SACK — 8881 E17 — AR2 D2-7/D2-8 BUS SACK L

DL4 50NS R15 1K — 7408 E86 — 7402 E13

+3V — 7474 E77 BBSY — 8881 E17 — AP2 D2-7/D2-8 BUS BSY L

7408 E85 — EH1 D2-7 ADDRESS TO BUS L

+5V R45 180 — BUS NPG IN H AU1 — R13 390 — 8640 E4 — 7404 E44 — +5V R24 1K

+5V R25 1K DL3 100NS R11 1K — +3V — 7474 E95 TIME OUT — EK1 D2-7 NXM H

D1-8 C1 H — 74H55 E76

7400 E86 — 7402 E94 — 74121 ET9 200NS C106 100 PF — R6 2.7K +5V — DE-7 NPR DATA TO BUS L

+3V — 7474 E64 MSYN — EJ1 D2-6 ASSERT MSYN H

7412L1 E78 100NS — R10 47K +5V — C103 150 PF — 74123 E54 20MS — +3V

7411 E37 MSYN WAIT 200NS — C102 100PF — R9 2.7K +5V

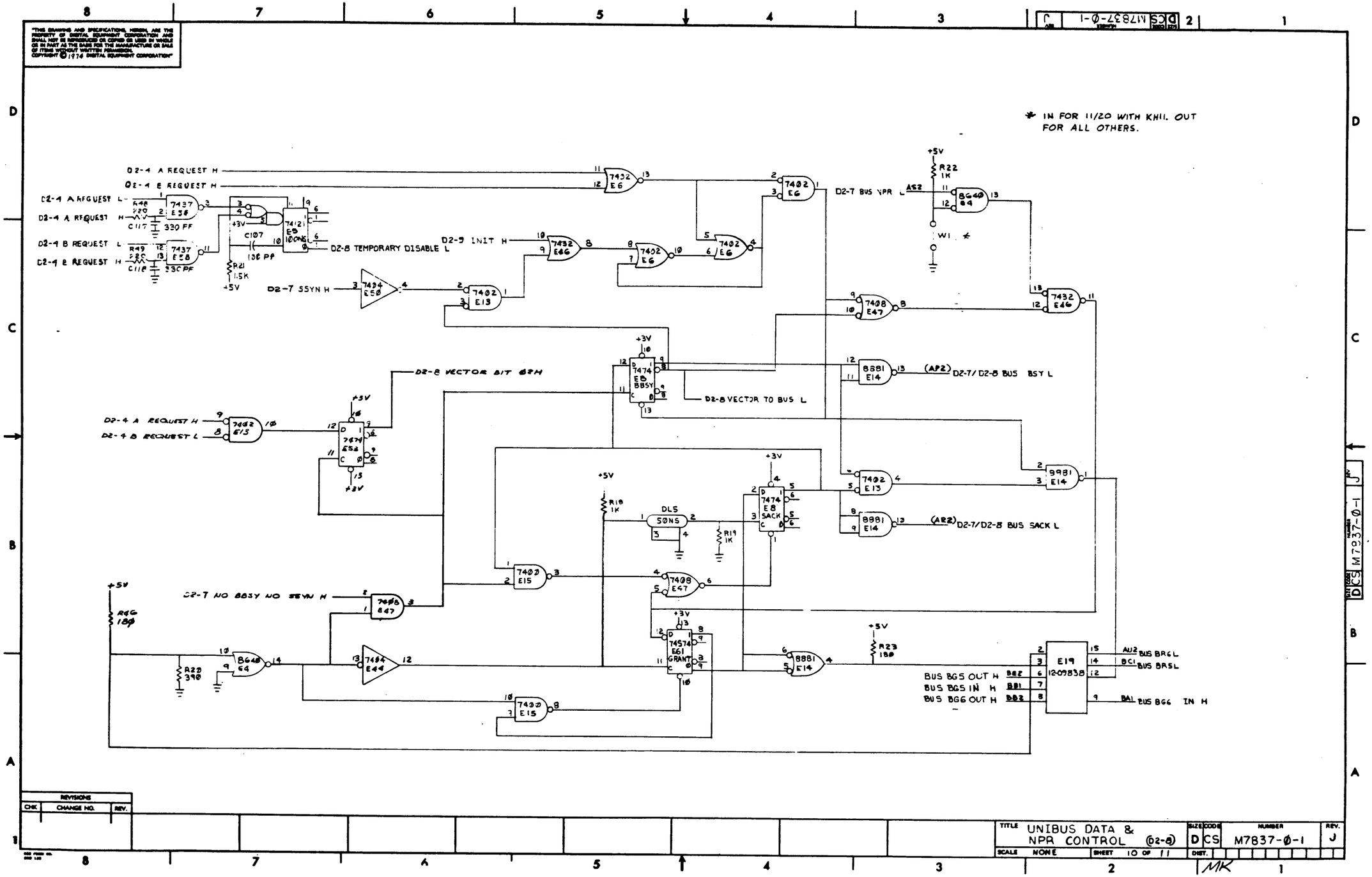
D2-9 B BUFFERED BIT D2 L — 7400 E44 — 7408 E85
D2-3 CLEAR NXM L

7474 E84 CLR — 7402 E94

7411 E28 DATA STROBE 100NS — C104 10PF — R12 2.8K +5V — BF1 D2-7 DATA STROBE H

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
UNIBUS DATA & NPR CONTROL (D2-7)	D	CS	M7837-Ø-1	J
SCALE —	SHEET 9 OF 11	DIST. MK		



TITLE	SIZE	CODE	NUMBER	REV.
UNIBUS DATA & NPR CONTROL (D2-8)	D	CS	M7837-0-1	J
SCALE NONE	SHEET 10 OF 11	DIST.		

REVISIONS

CHK	CHANGE NO.	REV.

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D1-3 TRANSFER BUS 00H (CH2)
D1-3 TRANSFER BUS 01H (CK2)
D1-3 TRANSFER BUS 02H (CK1)
D1-3 TRANSFER BUS 03H (CL1)
D1-3 TRANSFER BUS 04H (CR2)
D1-3 TRANSFER BUS 05H (CN1)
74174 E64
D5 D4 D3 D2 D1 D0 CLK CLR
E3(0) E4(0) E3(1) E2(0) E1(0) E2(1)
D2-9 EICR 00H
D2-9 EICR 01H
D2-9 EICR 02H
D2-9 EICR 03H
D2-9 EICR 04H
D2-9 EICR 05H

D1-4 TRANSFER BUS 12 H DE1
D2-3 SET EICR 12 L
TRANSFER BUS 13 H DE2
D2-3 SET EICR 13 L
TRANSFER BUS 14 H DF2
D2-3 SET EICR 14 L
D1-4 TRANSFER BUS 15H DJ1
D2-3 SET EICR 15 L
8015 E51
D3 D2 D1 D0 SET3 SET2 SET1 SET0 CLK CLR
E3(0) R2(0) E1(0) E2(0)
D2-9 EICR 12H
D2-9 EICR 13H
D2-9 EICR 14H
D2-9 EICR 15H

D3-6 NPR STATUS REPORTING REGISTER CLK L
BPI
74181 E36 180NS
C118 100pf
R37 3K
+5V

R36 1K +5V
D3-7 INIT D2 L DE2
7404 E56
7437 E58
D2-9 A BUFFERED INIT D2 L
D2-9 INIT H
D2-9 B BUFFERED INIT D2 L

D3-4 MASTER SCAN 00H DE1
D3-4 MASTER SCAN 01 H DP1
D3-4 MASTER SCAN 02 H DN1
D3-4 MASTER SCAN 03H DM1
D1-3 TRANSFER BUS 06H (CP1)
D1-3 TRANSFER BUS 07H (CC2)
D1-4 TRANSFER BUS 08H EC1
D1-4 TRANSFER BUS 09H EB2
D1-4 TRANSFER BUS 10H EB1
D1-4 TRANSFER BUS 11 H EE2
74174 E69
D5 D4 D3 D2 D1 D0 CLK CLR
E5(0) E4(1) E3(0) E2(0) E1(0) E5(0)
D2-9 EICR 06 H
D2-9 EICR 07 H
D2-9 EICR 08 H
D2-9 EICR 09 H
D2-9 EICR 10 H
D2-9 EICR 11 H
3341 E93
WR RDY SHIFT OUT SHIFT OUT RDY D0 D1 D2 D3 MR Q0 Q1 Q2 Q3
D2-9 NPR STATUS 00H
D2-9 NPR STATUS 01H
D2-9 NPR STATUS 02H
D2-9 NPR STATUS 03H

+3V
74181 E68 110NS
C111 100pf
R35 18E
+5V
D2-9 NPR STATUS 15 H
74174 E58 NPR STATUS
7404 E69
7408 E54
7408 E52

D2-5 READ NPR STATUS H
D3-2 ROM DATA 00H (DC1)
D3-2 ROM DATA 01 H (DD2)
D3-2 ROM DATA 02H (DM2)
D3-2 ROM DATA 03H (ET2)
74174 E66
D5 D1 D2 D3 CLK CLR
R5(1) R1(0) R2(0) R3(1) R3(0)
3341 E87
WR RDY SHIFT OUT SHIFT OUT RDY D0 D1 D2 D3 MR Q0 Q1 Q2 Q3
D2-9 NPR STATUS 08H
D2-9 NPR STATUS 09 H
D2-9 NPR STATUS 10H
D2-9 NPR STATUS 11 H
DLI
D3-6 RAM OUT PUT DATA CLK H
D3-6 RICR CLOCK L DD1
7404 E50
-15V
D1 D3 D5 D7 DB2 -15V
D6644
C108 6.8uf

7408 E54
D2-9 NPR STATUS AVAILABLE L
DK2
7404 E50
D2-9 NPR SILO NOT AVAILABLE H

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	UNIBUS DATA AND NPR CONTROL (D2-9)	SIZE/CODE D CS	NUMBER M7837-0-1 REV. J
SCALE		SHEET 11 OF 11	DIST. MK

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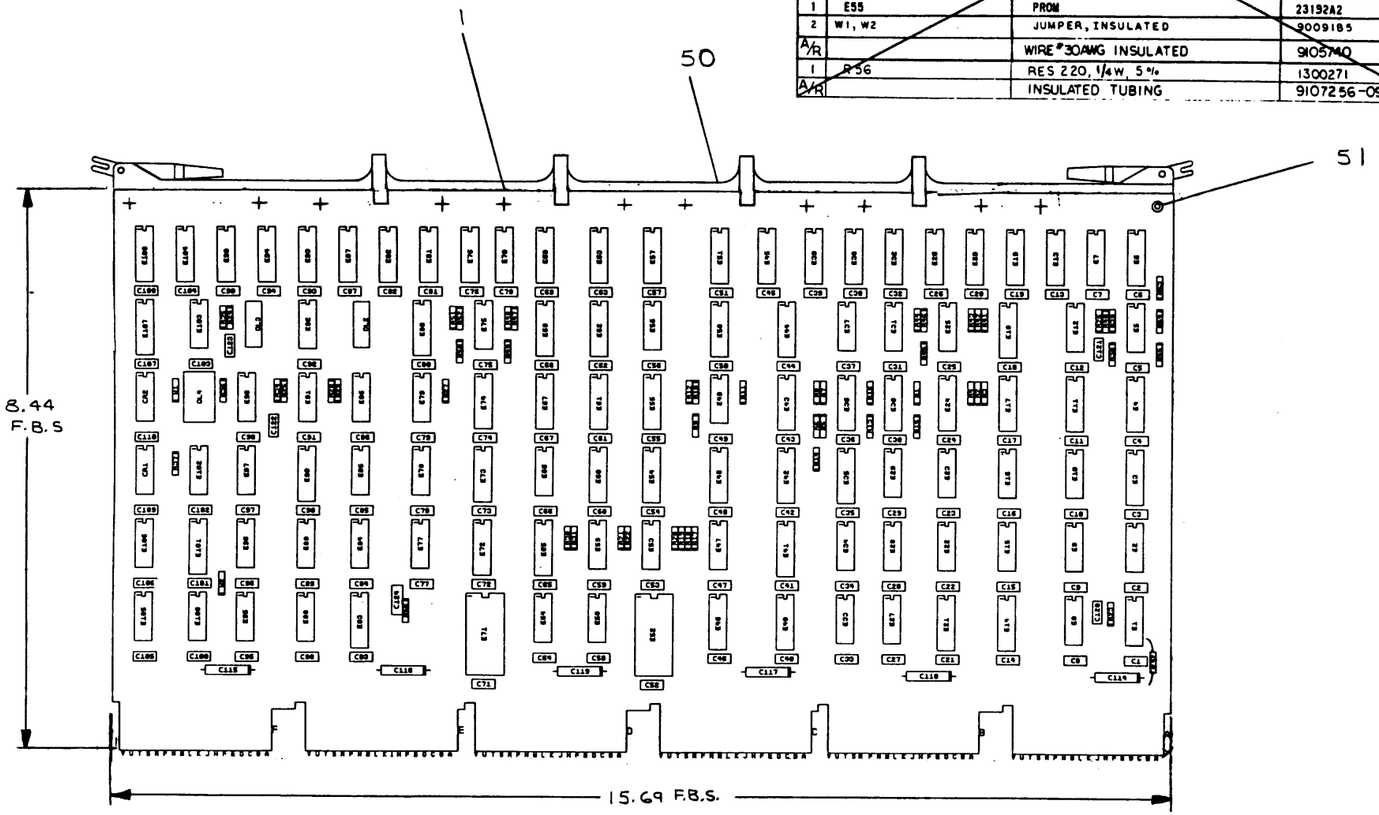
NOTES:

1. FOR USE WITH ASYNCHRONOUS LINE CARDS M7833 THIS BOARD MUST BE CS REV E OR LATER.

QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.
1	E80	I.C. DEC 74S175	1910857	52
1		HANDLE ASSY.	12L0711-2	53
12		EYELET, HANDLE	9006732	54
1	E4	PROM	23185A2	55
1	E11	PROM	23186A2	56
1	E17	PROM	23187A2	57
1	E24	PROM	23188A2	58
1	E30	PROM	23189A2	59
1	E38	PROM	23190A2	60
1	E43	PROM	23191A2	61
1	E55	PROM	23192A2	62
2	W1, W2	JUMPER, INSULATED	9009185	63
A/R		WIRE #30AWG INSULATED	9105740	64
1	R56	RES 220, 1/4W, 5%	1300271	65
A/R		INSULATED TUBING	9107256-09	66



REF		DESCRIPTION	PART NO.	ITEM NO.
REF		X-Y COORDINATE HOLE LOCATION	K-CO-M7838-0-4	1
REF		ASSY/DRILLING HOLE LAYOUT	D-AH-M7838-0-5	2
REF		MODULE ECO HISTORY	B-MH-M7838-0-6	3
1		ETCHED CIRCUIT BOARD	5010978	4
1	C131	CAP 10PF 100V,5% DM	1000008	5
2	C120,C123	CAP 100PF 100V,5% DM	1000016	6
2	C122,C124	CAP 1000PF 100V,5%	1000042	7
110	C1-C113	CAP .01UF 100V, 20%	1001610-01	8
6	C114-C119	CAP 6.8UF 35V 10% TANT	1005808	9
3	R24,29,30	RES. 330 OHM, 1/4W, 5%	1300295	10
2	R25,28	RES. 470 OHM, 1/4W, 5%	1300316	11
37	R1-18,27,38-55,36,37,	RES. 1K, 1/4W, 5%	1300365	12
1	R34	RES. 3.3K, 1/4W, 5%	1300439	13
2	R23,57	RES. 4.7K, 1/4W, 5%	1300447	14
3	R19,20,22	RES. 390 OHM, 1/4W, 5%	1300309	15
1	R26	RES. 15K, 1/4W, 5%	1300496	16
3	R17,19,21	RES. 180 OHM, 1/4W, 5%	1301322	17
1	R31	RES. 750 OHM, 1/4W, 5%	1301401	18
1	R35	RES. 5.6K, 1/4W, 5%	1301874	19
2	DL2,DL3	DELAY LINE 30NS	1605528-01	20
1	,DL4	DELAY LINE 100NS	1609559	21
1	CR1	20MHZ OSCILLATOR 14 PIN DIP	1811880-00	22
1	CR2	5.068 MHZ OSCILLATOR 14 PIN DIP	1811880-02	23
5	E58,15,22,23,28	I.C. DEC 7474	1905547	24
2	E47,78	I.C. DEC 7400	1905575	25
1	E2	I.C. DEC 7420	1905577	26
2	E97,102	I.C. DEC 7430	1905578	27
4	E31,37,49,56	I.C. DEC 7401	1905590	28
3	E85,91,1	I.C. DEC 7402	1909004	29
1	E105	I.C. DEC 7492	1909053	30
2	E100,106	I.C. DEC 7493	1909054	31
2	E59,96	I.C. DEC 74H00	1909056	32
1	E95	I.C. DEC 74H11	1909287	33
2	E33,53	I.C. DEC 8640	1911469	34
4	E84,88,89,16	I.C. DEC 74S74	1910544	35
5	E5,25,64,77,75	I.C. DEC 7404	1909686	36
1	E21	I.C. DEC 7442	1910046	37
1	E27	I.C. DEC 8881	1909705	38
3	E3,10,86	I.C. DEC 8815	1909713	39
5	E61,65,67,72,74	I.C. DEC 74193	1910018	40
1	E66	I.C. DEC 7437	1910091	41
2	E52,71	I.C. DEC 74150	1910153	42
3	E92,29,34	I.C. DEC 7408	1910155	43
4	E8,12,98,103	I.C. DEC 74121	1910230	44
1	E101	I.C. DEC 74181	1910850	45
10	E3,14,42,44,46,48,50,54,60,62	I.C. DEC 74175	1910851	46
1	E73	I.C. DEC 74174	1910852	47
9	E18,45,51,57,63,68,69,80,107	I.C. DEC 74157	1910855	48
4	E75,40,41,83	I.C. DEC 74155	1910856	49
19	E6,7,13,19,20,26,32,38,E39,70,76,81,82,87,93,94,E99,104,108	I.C. DEC 3108	1910818-02	50
1	E79	I.C. DEC 74H10	1909057	51
QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

8640	1	8
7493	10	5
7492	10	5
IC TYPE	GND	+5V

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

AA2, BA2, CA2, DA2, EA2, FA2 — +5V

AC2, AT1, BC2, BT1, CC2, CT1, DC2, DT1, EC2, ET1, FC2, FT1 — GND

C114 6.8UF, C115 6.8UF, C116 6.8UF, C117 6.8UF, C118 6.8UF, C119 6.8UF, C1 .01UF, C1 THRU C110 .01UF

REV	CHANGE NO	CHK	DATE	BY
A	ORIGINATED	RD	16-DEC-75	J. McNAMARA
B	M7838-00001	RD	7-JAN-76	J. McNAMARA
C	M7838-00002	JMcN	16-JAN-76	J. McNAMARA
D	M7838-00002	JMcN	16-JAN-76	J. McNAMARA
E	M7838-00004	JMcN	16-JAN-76	J. McNAMARA
F	M7838-00005	JMcN	16-JAN-76	J. McNAMARA
G	M7838-00006	JMcN	16-JAN-76	J. McNAMARA
H	M7838-00007	JMcN	16-JAN-76	J. McNAMARA
J	M7838-00008	JMcN	16-JAN-76	J. McNAMARA
K	M7838-00009	JMcN	16-JAN-76	J. McNAMARA

REVISIONS

DEC NO.	EIA NO.

SEMICONDUCTOR CONVERSION CHART

FIRST USED ON OPTION MODEL: DV11-AA

ETCH BOARD REV: C

		DATE
DRN.	K. Davis	1-6-75
CHK'D		1-14-75
ENG.		2-12-75
PROJ. ENG.		2-12-75
PROD.		2-12-75

NEXT HIGHER ASSY: B-DD-DV11-Ø

SCALE: NONE

SHEET 1 OF 12

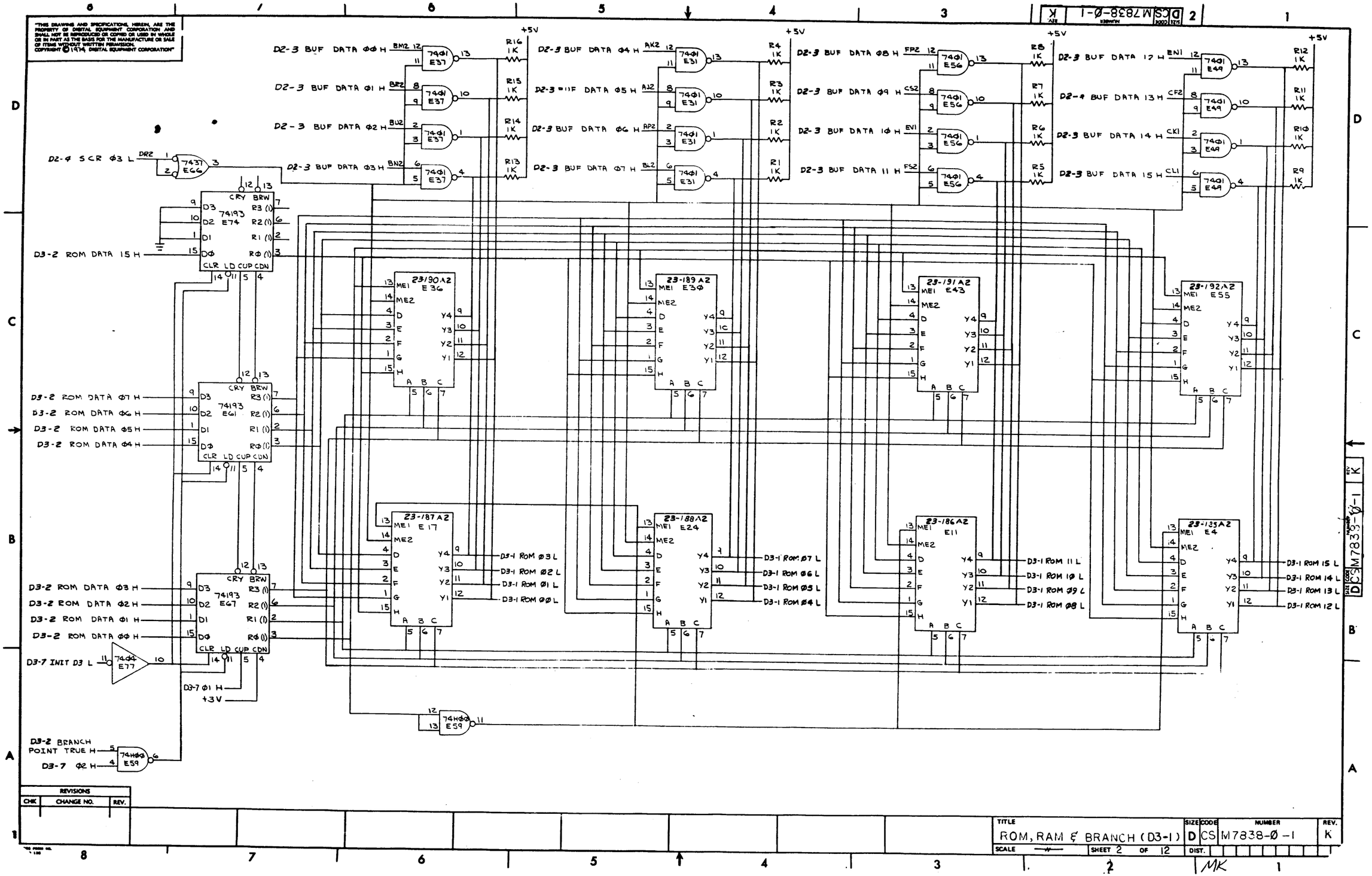
digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE: ROM, RAM AND BRANCH

SIZE D | CODE | NUMBER: DCSM7838-Ø-1 | REV. K

DIST.

DCSM7838-Ø-1 K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D2-3 BUF DATA ØØ H
D2-3 BUF DATA Ø1 H
D2-3 BUF DATA Ø2 H
D2-3 BUF DATA Ø3 H
D2-3 BUF DATA Ø4 H
D2-3 BUF DATA Ø5 H
D2-3 BUF DATA Ø6 H
D2-3 BUF DATA Ø7 H
D2-3 BUF DATA Ø8 H
D2-3 BUF DATA Ø9 H
D2-3 BUF DATA 1Ø H
D2-3 BUF DATA 11 H
D2-3 BUF DATA 12 H
D2-3 BUF DATA 13 H
D2-3 BUF DATA 14 H
D2-3 BUF DATA 15 H
D2-4 SCR Ø3 L
D3-2 ROM DATA 15 H
D3-2 ROM DATA Ø7 H
D3-2 ROM DATA Ø6 H
D3-2 ROM DATA Ø5 H
D3-2 ROM DATA Ø4 H
D3-2 ROM DATA Ø3 H
D3-2 ROM DATA Ø2 H
D3-2 ROM DATA Ø1 H
D3-2 ROM DATA ØØ H
D3-7 INIT D3 L
D3-7 Ø1 H
+3V
D3-2 BRANCH POINT TRUE H
D3-7 Ø2 H
D3-1 ROM Ø3 L
D3-1 ROM Ø2 L
D3-1 ROM Ø1 L
D3-1 ROM ØØ L
D3-1 ROM Ø7 L
D3-1 ROM Ø6 L
D3-1 ROM Ø5 L
D3-1 ROM Ø4 L
D3-1 ROM 11 L
D3-1 ROM 1Ø L
D3-1 ROM Ø9 L
D3-1 ROM Ø8 L
D3-1 ROM 15 L
D3-1 ROM 14 L
D3-1 ROM 13 L
D3-1 ROM 12 L
74Ø1 E37
74Ø1 E31
74Ø1 E56
74Ø1 E49
74Ø1 E74
74Ø1 E61
74Ø1 E67
74Ø1 E77
74HØØ E59
74HØØ E59
74Ø4 E77
74Ø4 E37
23-190A2 E36
23-189A2 E3Ø
23-191A2 E43
23-192A2 E55
23-187A2 E17
23-188A2 E24
23-186A2 E11
23-185A2 E4
+5V
REVISIONS
CHK
CHANGE NO.
REV.
TITLE
ROM, RAM & BRANCH (D3-1)
SIZE D
CODE CS
NUMBER M7838-Ø-1
REV. K
SCALE
SHEET 2 OF 12
DIST.
MK

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NOTE PIN DV2 IS ASSIGNED PIN "I-ZALU-8" BUT IS NOT USED ON THIS BOARD

D2-4 SCR Φ2 H EU1

D3-2 TRANSFER SOURCE ENAB L FB2

TRAN FLAG WAITING L CP2

+5V R17 180 R18 390

DB1 D3-2 BRANCH B L

D3-2 DATA TRANSFER L FB3

D3-2 RAM OPERATION L FB2

D3-2 ALU OPERATION L FB1 EP2

D3-2 BCC CALCULATION L EU2

D3-2 SET/CLEAR OPERATION L FA1

D3-2 NPR OPERATION L FA0 ET2

74155 E63 STBB STBA DB DA S1 S0

D2-5 WRITE INHIBIT H

D3-11 RAM OUTPUT Φ-14=Φ

D3-11 RAM OUTPUT 15 H

D1-9 MEM PRE ERR H

D2-7 REQUEST BUS H

D3-11 RAM OUTPUT Φ7 H

D3-11 RAM OUTPUT Φ6 H

D3-11 RAM OUTPUT Φ5 H

D3-11 RAM OUTPUT Φ4 H

D3-11 RAM OUTPUT Φ3 H

D3-11 RAM OUTPUT Φ2 H

D3-11 RAM OUTPUT Φ1 H

D3-11 RAM OUTPUT ΦΦ H

74150 E52 STB D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0 S3 S2 S1 S0

MATCH DETECT L CR1 R20 340 R19 180 +5V

DATA NOT AVAILABLE L CT2 R22 340 R21 180 +5V

D1-5 READY IN L DL1

D1-1 ALU RESULT Φ4 H DS1

D1-1 ALU RESULT Φ3 H DS2

D1-1 ALU RESULT Φ2 H DT2

D1-1 ALU RESULT Φ1 H DU1

D1-1 ALU RESULT Φ0 H DU2

D1-2 ALU 13-12 H EC1

D2-9 NPR SILO NOT AVAILABLE H EJ1

D2-7 NXM H EJ2

D2-6 SCR Φ0 H EK1

D1-5 RECEIVER FLAG WAITING EK2

D1-5 RECEIVED CHARACTER WAITING H EN2

+3V

D1-2 ALU RESULT 13 H EH1

74150 E71 STB D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0 S3 S2 S1 S0

74H08 E59

D3-2 BRANCH A L EH2

+3V

74S74 E68

D3-7 T SΦ H

D3-2 BRANCH POINT TRUE H

74175 E66 D3 D2 D1 D0 R3(1) R3(0) R2(1) R2(0) R1(1) R1(0) R0(1) R0(0) CLR CLK

D3-1 ROM 15 L

D3-1 ROM 14 L

D3-1 ROM 13 L

D3-1 ROM 12 L

D3-2 ROM DATA 15 H EE2

D3-2 ROM DATA 14 H ES1

D3-2 ROM DATA 13 H ES2

D3-2 ROM DATA 12 H EE1

D3-7 INIT D3 L

74175 E54

D3-1 ROM 11 L

D3-1 ROM 10 L

D3-1 ROM Φ9 L

D3-1 ROM Φ8 L

D3-2 ROM DATA 11 H DB2

D3-2 ROM DATA 10 H CU2

D3-2 ROM DATA Φ9 H EA1

D3-2 ROM DATA Φ8 L EB1

74175 E45

D3-1 ROM Φ7 L

D3-1 ROM Φ6 L

D3-1 ROM Φ5 L

D3-1 ROM Φ4 L

D3-2 ROM DATA Φ7 H CH2

D3-2 ROM DATA Φ6 H CF1

D3-2 ROM DATA Φ5 H CE1

D3-2 ROM DATA Φ4 H CE2

74175 E42

D3-1 ROM Φ3 L

D3-1 ROM Φ2 L

D3-1 ROM Φ1 L

D3-1 ROM ΦΦ L

D3-2 ROM DATA Φ3 H BL1

D3-2 ROM DATA Φ2 L

D3-2 ROM DATA Φ2 H BD2

D3-2 ROM DATA Φ1 L

D3-2 ROM DATA Φ1 H EJ1

D3-2 ROM DATA ΦΦ L

D3-2 ROM DATA ΦΦ H BC1

D3-7 Φ3 L

D2-5 LOAD SFR L DH1

74H08 E59

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
ROM, RAM & BRANCH (D3-2)	D	CS	M7838-Ø-1	K
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D3-2 ROM DATA Ø5 H — 7400 E47 pin 1
D3-2 ROM DATA Ø4 H — 7400 E47 pin 5
D3-2 ROM DATA Ø7 H — 7410 E47 pin 9
D3-2 ROM DATA Ø3 H — 7400 E47 pin 13
D3-2 ROM DATA Ø6 H — 7400 E78 pin 13
D3-7 DATA STROBE L — 7402 E85 pin 3
D3-2 SET/CLEAR OPERATION L — 7402 E85 pin 2

7400 E47 pin 3 — D3-3 SET/CLEAR Ø4 L (CN1)
7400 E47 pin 6 — D3-3 SET/CLEAR Ø3 L (CD1)
7402 E85 pin 1 — (CE1)

D3-3 ROM DATA Ø0 L
D3-2 ROM DATA Ø1 L
D3-2 ROM DATA Ø2 L

74155 E41 (STBB, STBA, SI, SØ, DB, DA)
- FB0 — D3-3 SET RAM OUTPUT Ø0 L
- FB1 — D3-3 CLEAR RAM OUTPUT Ø0 L
- FB2 — D3-3 SET RAM OUTPUT Ø1 L
- FB3 — D3-3 CLEAR RAM OUTPUT Ø1 L
- FA0 — D3-3 SET RAM OUTPUT Ø2 L
- FA1 — D3-3 CLEAR RAM OUTPUT Ø2 L
- FA2 — D3-3 SET RAM OUTPUT Ø3 L
- FA3 — D3-3 CLEAR RAM OUTPUT Ø3 L

74155 E35 (STBB, STBA, SI, SØ, DB, DA)
- FB0 — D3-3 SET RAM OUTPUT Ø4 L
- FB1 — D3-3 CLEAR RAM OUTPUT Ø4 L
- FB2 — D3-3 SET RAM OUTPUT Ø5 L
- FB3 — D3-3 CLEAR RAM OUTPUT Ø5 L
- FA0 — D3-3 SET RAM OUTPUT Ø6 L
- FA1 — D3-3 CLEAR RAM OUTPUT Ø6 L
- FA2 — D3-3 SET RAM OUTPUT Ø7 L
- FA3 — D3-3 CLEAR RAM OUTPUT Ø7 L

74155 E40 (STBB, STBA, SI, SØ, DB, DA)
- FB0 — D3-3 SET TRAN DATA Ø2 L
- FB1 — D3-3 CLEAR TRAN DATA Ø2 L
- FB2 — CD2 — D3-3 SET T MARK L
- FB3 — CA1 — D3-3 CLEAR T MARK L
- FA0 — CE2 — D3-3 RESYNC PULSE L
- FA1 — DP2 — D3-3 ADVANCE MASTER SCANNER L
- FA2
- FA3

REVISIONS

CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
ROM, RAM & BRANCH (D3-3)	D	CS	M7838-Ø-1	K
SCALE	SHEET 4 OF 12	DIST.	MK	

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D3-3 TRANSFER BUS ØØ H — CJ2 13 — 74175 E46 D3 — R3 15 CH1 — D3-4 TRAN DATA ØØ H
D3-3 TRANSFER BUS Ø1 H — CK2 12 — D2 — R2 1Ø CJ1 — D3-4 TRAN DATA Ø1 H
D3-3 TRANSFER BUS Ø2 H — CM2 5 — D1 — R1 7 CL2 — D3-4 TRAN DATA Ø2 H
D3-3 TRANSFER BUS Ø3 H — CMN 4 — DØ — RØ 2 CN2 — D3-4 TRAN DATA Ø3 H
CLR 1 CLK 9

D3-7 INIT D3 L

D3-6 TRANSMITTED DATA BUS CLOCK L — 1 — 7404 E64 — 2

D3-3 TRANSFER BUS Ø4 H — AN2 13 — 74175 E14 D3 — R3 15 AT2 — D3-4 TRAN DATA Ø4 H
D3-3 TRANSFER BUS Ø5 H — AR1 12 — D2 — R2 1Ø AS1 — D3-4 TRAN DATA Ø5 H
D3-3 TRANSFER BUS Ø6 H — AU2 5 — D1 — R1 7 AV2 — D3-4 TRAN DATA Ø6 H
D3-3 TRANSFER BUS Ø7 H — AUN 4 — DØ — RØ 2 AS2 — D3-4 TRAN DATA Ø7 H
CLR 1 CLK 9

D3-3 SET TRAN DATA Ø8 L — 4 — 74174 E58 D — Q 5 DF2 — D3-4 TRAN DATA Ø8 H
D3-5 INIT H — 3 — C
D3-3 CLEAR TRAN DATA Ø8 L — 1

+3V — 3 4 5 — 74121 E8 300Ω — 11 9 6 1 — AM2 — D3-4 TRANSMITTER STROBE H
1Ø — C12Ø 1ØØPF
R23 4.7K — +5V

5 — 7404 EG4 — 6 DP1 — D3-4 MASTER SCAN C H

74193 E72 — 12 13 CRY BRW — 9 D3 1Ø D2 1 D1 15 DØ — R3 7 NC — R2 6 NC — R1 2 NC — RØ 3 DN1 — D3-4 MASTER SCAN Ø3 H
CLR 14 LD 11 CUP 5 CDN 4 — +3V
3 — 7404 EG4 — 4 DN2 — D3-4 MASTER SCAN D H

74193 EG5 — 12 13 CRY BRW — 9 D3 1Ø D2 1 D1 15 DØ — R3 7 DM2 — D3-4 MASTER SCAN Ø2 H — R2 6 DL2 — D3-4 MASTER SCAN Ø1 H — R1 2 FT2 — D3-4 MASTER SCAN ØØ H — RØ 3 FU2 — D3-4 MASTER SCAN T/R
CLR 14 LD 11 CUP 5 CDN 4 — +3V

D3-5 INIT H
D3-3 ADVANCE MASTER SCANNER L

REVISIONS
CHK | CHANGE NO. | REV.

TITLE: ROM, RAM & BRANCH (D3-4)
SIZE D CODE CS NUMBER M7838-Ø-1 REV. K
SCALE — SHEET 5 OF 12 DIST. NK

SIZE D CODE CS NUMBER M7838-Ø-1 REV. K

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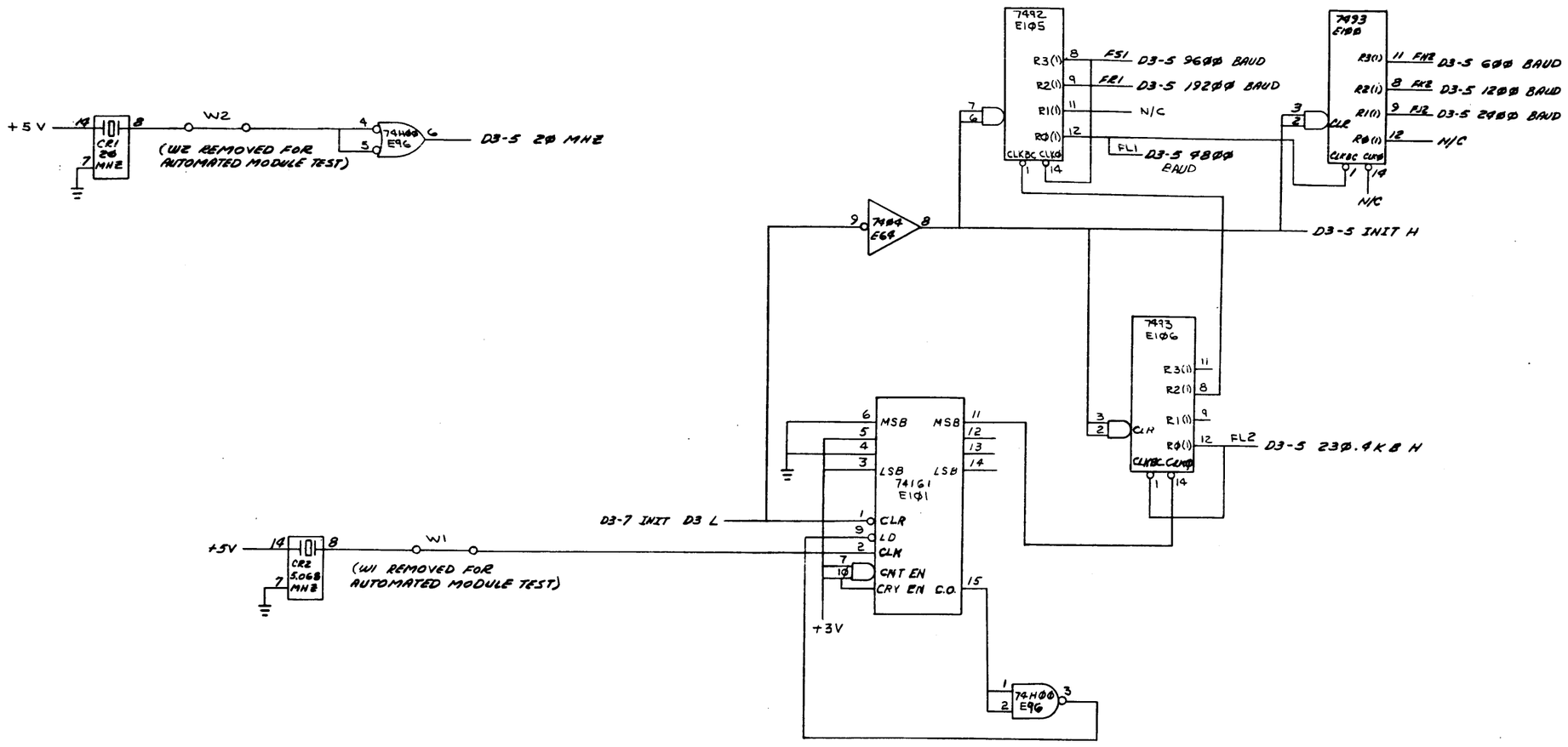

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
ROM, RAM & BRANCH (D3-5)	D	CS	M7838-Ø-1	K
SCALE	SHEET 6 OF 12	DIST.	MK	

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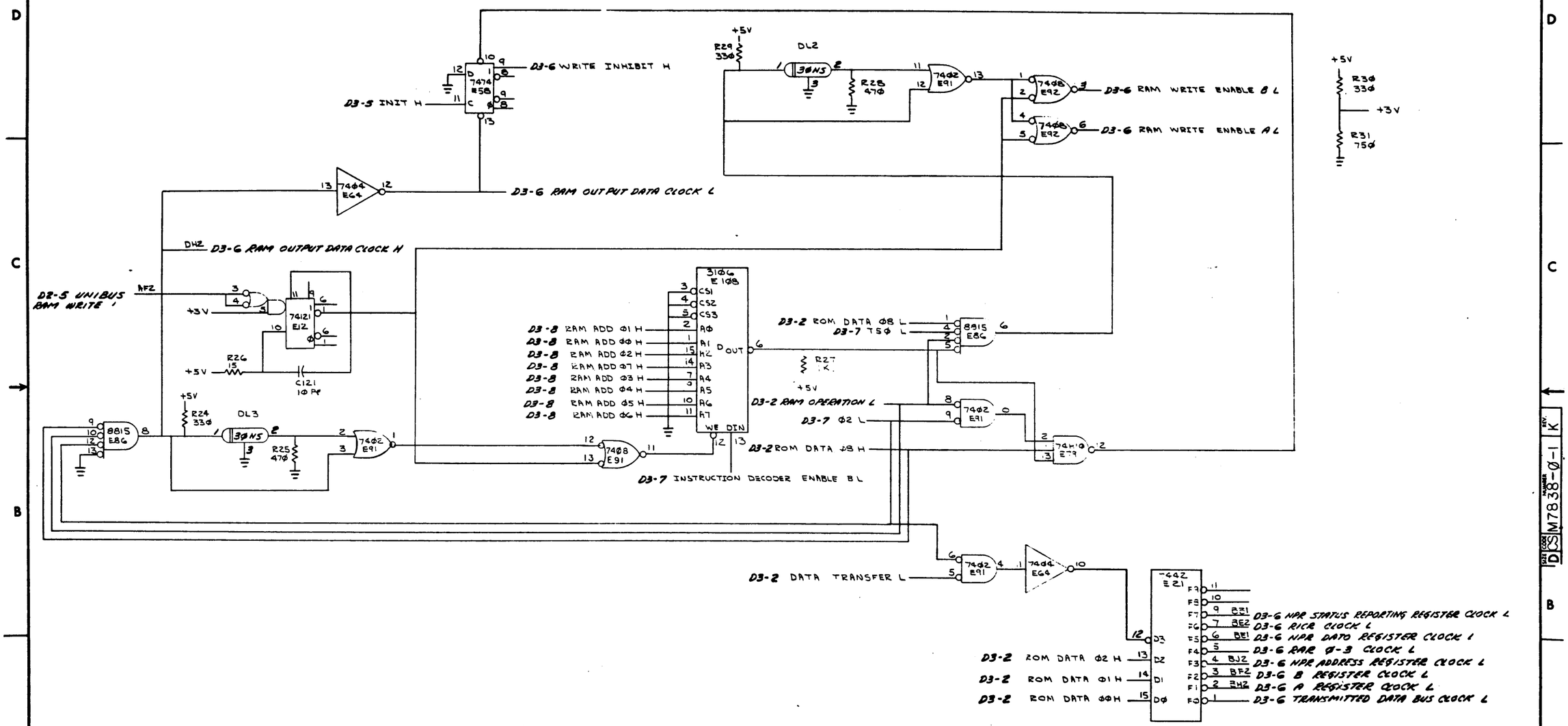

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
ROM, RAM & BRANCH (D3-6)	D	CS	M7838-0-1	K

SCALE — SHEET 7 OF 12 DIST.

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D2-4 SCR 11 H ELI — 74ØØ E78 — C122 1ØØØ PF — R34 3.3K — +5V — 74121 E98 — 2.4 USEC

8W D3-7 BUS MSYN L — D2-6 ASSERT MSYN H — BP2 — 8881 E27 — 8640 E33

D3-7 INSTRUCTION DECODER ENABLE B L — 7430 E102 — 7430 E97

DI-8 A17 H — FE1 — FE2 — DI-8 ADDRESS SELECTED H

D2-5 LOAD LCR H — FP1 — +5V — R35 5.6K — 74121 E103 30ns — C123 1ØØ PF

BUS INIT L AA1 — 8640 E33 — 7402 E85 — 7404 E77 — +3V — 7437 E66 — EB2 D3-7 INIT D1 L

7400 E78 — AV1 D3-7 INIT D2 L — 7437 E66 — D3-7 INIT D3 L

DL4 100NS — R36 1K — R37 1K — +5V

7404 E77 — D3-7 BUS INIT L

74H11 E95 — 74H00 E96 — SCR Ø1 H — FF2 — SCR ØØ H — FA1

74S74 E88 UNIBUS GO — 74S74 E89 PHASE — D3-5 20 MHZ — +3V

74S74 E84 MICRO CODE GO — ER1 D3-7 Ø1 L — D3-7 Ø1 H

7402 E85 — 13

74S175 E90 — D3 R3(1) R3(0) — FC1 D3-7 DATA STROBE L — D2 R2(1) R2(0) — D1 R1(1) R1(0) — FD2 D3-7 Ø2 L — D0 R0(1) R0(0) — D3-7 T5Ø H — D3-7 T5Ø L — CLR CLK

74S74 E89 — T25Ø — D3-7 Ø3 H — D3-7 Ø3 L

R57 4.7K — +5V — C1 H — AN1 — 7402 E1 — C0 H — BH1 — 7402 E1

74S74 DATIP E16 — +3V — 74S74 E86 MICRO INSTR. SEQUENCING CONTROL PROM

R56 220 — C124 1000PF — 8881 E27 — BUI D3-7 BUS SSYN L

FB1 D3-7 INSTRUCTION DECODER ENABLE A L

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
ROM, RAM & BRANCH (D3-7)	D	CS	M7838-Ø-1	K
SCALE	SHEET 8 OF 12	DIST.		MK

D CS M7838-Ø-1 K

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D3-7 INSTRUCTION DECODER ENABLE B L

D3-7 INSTRUCTION DECODER ENABLE A L

74157 E45: D1-3 TRANSFER BUS Ø0 H (CJ2) / D2-3 BUF DATA Ø0 H → D3-8 RAM INPUT DATA Ø0 H; D1-3 TRANSFER BUS Ø1 H (CK2) / D2-3 BUF DATA Ø1 H → D3-8 RAM INPUT DATA Ø1 H; D1-3 TRANSFER BUS Ø2 H (CM2) / D2-3 BUF DATA Ø2 H → D3-8 RAM INPUT DATA Ø2 H; D1-3 TRANSFER BUS Ø3 H (CM1) / D2-3 BUF DATA Ø3 H → D3-8 RAM INPUT DATA Ø3 H

74157 E18: D1-3 TRANSFER BUS Ø4 H (AN2) / D2-3 BUF DATA Ø4 H → D3-8 RAM INPUT DATA Ø4 H; D1-3 TRANSFER BUS Ø5 H (AR1) / D2-3 BUF DATA Ø5 H → D3-8 RAM INPUT DATA Ø5 H; D1-3 TRANSFER BUS Ø6 H (AN2) / D2-3 BUF DATA Ø6 H → D3-8 RAM INPUT DATA Ø6 H; D1-3 TRANSFER BUS Ø7 H (AN1) / BUF DATA Ø7 H → D3-8 RAM INPUT DATA Ø7 H

74157 E107: D1-3 TRANSFER BUS Ø8 H (FR2) / D2-3 BUF DATA Ø8 H → D3-8 RAM INPUT DATA Ø8 H; D1-3 TRANSFER BUS Ø9 H (FM2) / D2-3 BUF DATA Ø9 H → D3-8 RAM INPUT DATA Ø9 H; D1-3 TRANSFER BUS 1Ø H (FN2) / D2-3 BUF DATA 1Ø H → D3-8 RAM INPUT DATA 1Ø H; D1-3 TRANSFER BUS 11 H (FV1) / D2-3 BUF DATA 11 H → D3-8 RAM INPUT DATA 11 H

74157 E85: D1-3 TRANSFER BUS 12 H (EM1) / D2-3 BUF DATA 12 H → D3-8 RAM INPUT DATA 12 H; D1-3 TRANSFER BUS 13 H (EL2) / D2-3 BUF DATA 13 H → D3-8 RAM INPUT DATA 13 H; D1-3 TRANSFER BUS 14 H (EM2) / D2-3 BUF DATA 14 H → D3-8 RAM INPUT DATA 14 H; D1-3 TRANSFER BUS 15 H (EP1) / D2-3 BUF DATA 15 H → D3-8 RAM INPUT DATA 15 H

74157 E68: D1-3 TRANSFER BUS 16 H (DJ2) / D2-Ø SCR Ø4 H (DJ1) → D3-8 RAM INPUT DATA 16 H; D1-3 TRANSFER BUS 17 H (DK2) / D2-Ø SCR Ø5 H (DK1) → D3-8 RAM INPUT DATA 17 H

74157 E57: D3-8 RAR ØØ H / D3-8 SRS ØØ H (CB2) → D3-8 RAM ADD A ØØ H; D3-8 RAR Ø1 H / D3-8 SRS Ø1 H (BH1) → D3-8 RAM ADD A Ø1 H; D3-8 RAR Ø2 H / D3-8 SRS Ø2 H (BT2) → D3-8 RAM ADD A Ø2 H; D3-8 RAR Ø3 H / D3-8 SRS Ø3 H (BS2) → D3-8 RAM ADD A Ø3 H

74157 E51: D3-8 RAR ØØ H / D3-8 SRS ØØ H (CB2) → D3-8 RAM ADD B ØØ H; D3-8 RAR Ø1 H / D3-8 SRS Ø1 H (BH1) → D3-8 RAM ADD B Ø1 H; D3-8 RAR Ø2 H / D3-8 SRS Ø2 H (BT2) → D3-8 RAM ADD B Ø2 H; D3-8 RAR Ø3 H / D3-8 SRS Ø3 H (BS2) → D3-8 RAM ADD B Ø3 H

74157 E69: D3-2 ROM DATA ØØ H / D3-8 SRS Ø8 H (DE2) → D3-8 RAM ADD A Ø8 H; D3-2 ROM DATA Ø1 H / D3-8 SRS Ø9 H (DH1) → D3-8 RAM ADD A Ø5 H; D3-2 ROM DATA Ø2 H / D3-8 SRS 1Ø H (DV1) → D3-8 RAM ADD A Ø6 H; D3-2 ROM DATA Ø3 H / D3-8 SRS 11 H (DP1) → D3-8 RAM ADD A Ø7 H

74157 E63: D3-2 ROM DATA ØØ H / D3-8 SRS Ø8 H (DE2) → D3-8 RAM ADD B Ø4 H; D3-2 ROM DATA Ø1 H / D3-8 SRS Ø9 H (DH1) → D3-8 RAM ADD B Ø5 H; D3-2 ROM DATA Ø2 H / D3-8 SRS 1Ø H (DV1) → D3-8 RAM ADD B Ø6 H; D3-2 ROM DATA Ø3 H / D3-8 SRS 11 H (DP1) → D3-8 RAM ADD B Ø7 H

74175 E0Ø: D2-3 BUF DATA ØØ H → D3-8 SRS ØØ N; D2-3 BUF DATA Ø1 H → D3-8 SRS Ø1 N; D2-3 BUF DATA Ø2 H → D3-8 SRS Ø2 N / D3-8 SRS Ø2 L (CC1); D2-3 BUF DATA Ø3 H → D3-8 SRS Ø3 N / D3-8 SRS Ø3 L (BV2)

D3-7 INIT D3 L / D2-5 LOAD SRS LOW BYTE H (CB1)

74175 E62: D2-3 BUF DATA Ø8 H → D3-8 SRS Ø8 N; D2-3 BUF DATA Ø9 H → D3-8 SRS Ø9 N; D2-3 BUF DATA 1Ø H → D3-8 SRS 1Ø N; D2-3 BUF DATA 11 H → D3-8 SRS 11 N

D2-5 LOAD SRS HIGH BYTE H (DD2)

74175 E50: D1-3 TRANSFER BUS ØØ H (CJ2) → D3-8 RAR ØØ N; D1-3 TRANSFER BUS Ø1 H (CK2) → D3-8 RAR Ø1 N; D1-3 TRANSFER BUS Ø2 H (CM2) → D3-8 RAR Ø2 N; D1-3 TRANSFER BUS Ø3 H (CM1) → D3-8 RAR Ø3 N

D3-6 RAR Ø-3 CLOCK L ← 7404 E77

REVISIONS

CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
ROM, RAM & BRANCH (D3-8)	D	CS	M7838-Ø-1	K
SCALE	SHEET 9 OF 12	DIST.	MK	

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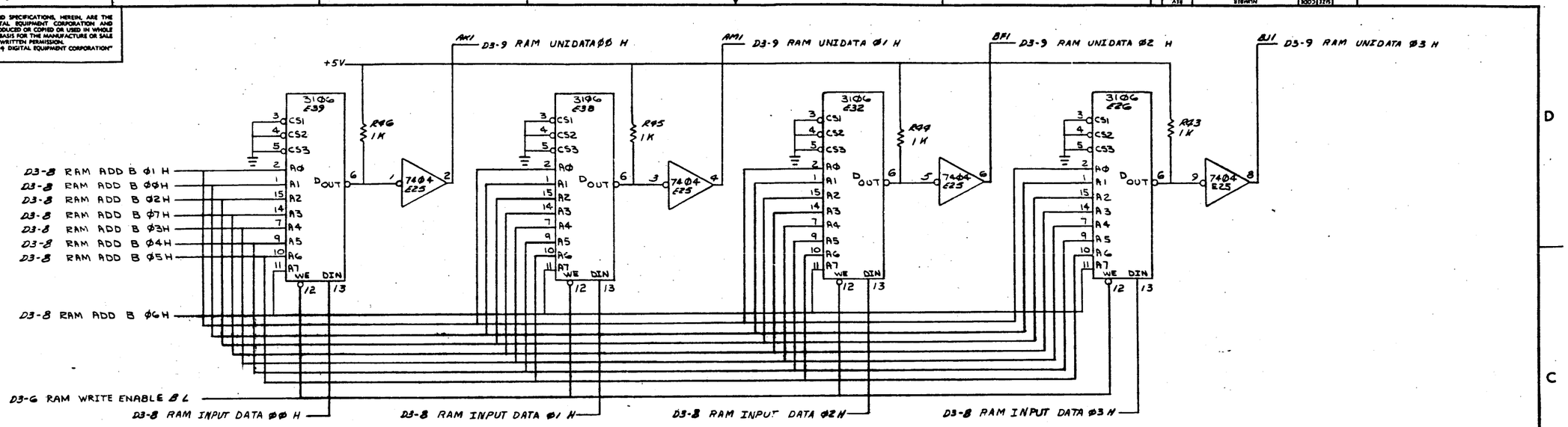
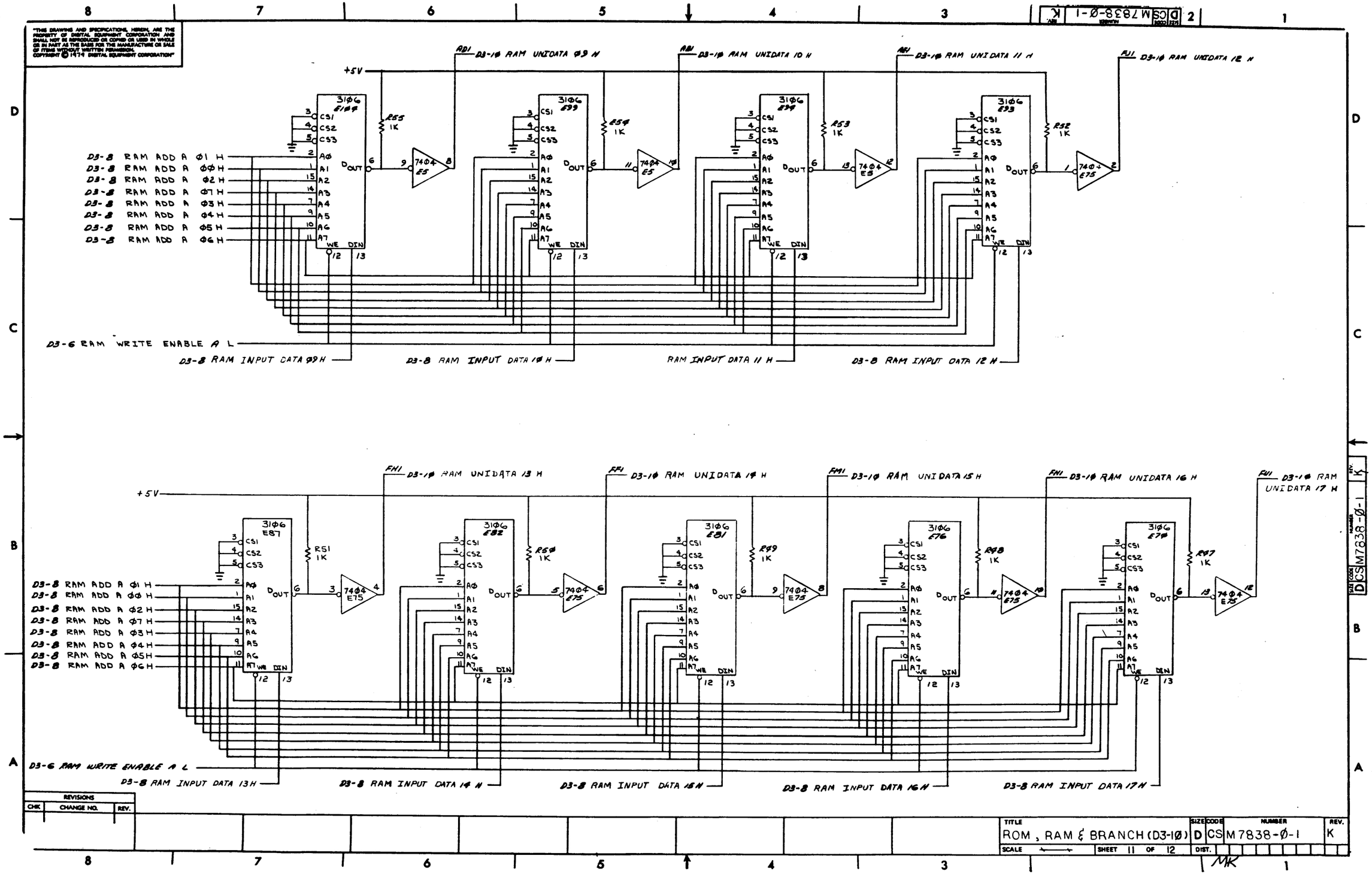


REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
ROM, RAM & BRANCH (D3-9)	D	CS	M7838-Ø-1	K
SCALE	SHEET 10 OF 12	DIST.		

MK



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D3-10 RAM UNIDATA 09 H
D3-10 RAM UNIDATA 10 H
D3-10 RAM UNIDATA 11 H
D3-10 RAM UNIDATA 12 H
+5V
3106 E104
3106 E99
3106 E94
3106 E93
R55 1K
R54 1K
R53 1K
R52 1K
7404 E5
7404 E75
D3-8 RAM ADD A 01 H
D3-8 RAM ADD A 00 H
D3-8 RAM ADD A 02 H
D3-8 RAM ADD A 07 H
D3-8 RAM ADD A 03 H
D3-8 RAM ADD A 04 H
D3-8 RAM ADD A 05 H
D3-8 RAM ADD A 06 H
D3-6 RAM WRITE ENABLE A L
D3-8 RAM INPUT DATA 09 H
D3-8 RAM INPUT DATA 10 H
RAM INPUT DATA 11 H
D3-8 RAM INPUT DATA 12 H
D3-10 RAM UNIDATA 13 H
D3-10 RAM UNIDATA 14 H
D3-10 RAM UNIDATA 15 H
D3-10 RAM UNIDATA 16 H
D3-10 RAM UNIDATA 17 H
3106 E87
3106 E82
3106 E81
3106 E76
3106 E70
R51 1K
R50 1K
R49 1K
R48 1K
R47 1K
D3-8 RAM ADD A 01 H
D3-8 RAM ADD A 00 H
D3-8 RAM ADD A 02 H
D3-8 RAM ADD A 07 H
D3-8 RAM ADD A 03 H
D3-8 RAM ADD A 04 H
D3-8 RAM ADD A 05 H
D3-8 RAM ADD A 06 H
D3-6 RAM WRITE ENABLE A L
D3-8 RAM INPUT DATA 13 H
D3-8 RAM INPUT DATA 14 H
D3-8 RAM INPUT DATA 15 H
D3-8 RAM INPUT DATA 16 H
D3-8 RAM INPUT DATA 17 H
REVISIONS
CHK
CHANGE NO.
REV.
TITLE
ROM, RAM & BRANCH (D3-10)
SIZE D
CODE CS
NUMBER M7838-0-1
REV. K
SCALE
SHEET 11 OF 12
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D3-3 SET RAM OUTPUT Ø6 L
D3-9 RAM UNIDATA Ø6 H
D3-6 RAM OUTPUT DATA CLOCK L
D3-3 CLEAR RAM OUTPUT Ø6 L
7437 E66
7408 E29
7474 E23
DA1
D3-11 RAM OUTPUT Ø6 H

D3-3 SET RAM OUTPUT Ø5 L
D3-9 RAM UNIDATA Ø5 H
D3-3 CLEAR RAM OUTPUT Ø5 L
7408 E29
7474 E23
DC1
D3-11 RAM OUTPUT Ø5 H

D3-3 SET RAM OUTPUT Ø4 L
D3-9 RAM UNIDATA Ø4 H
D3-3 CLEAR RAM OUTPUT Ø4 L
7408 E29
7474 E28
CU1
D3-11 RAM OUTPUT Ø4 H

D3-3 SET RAM OUTPUT Ø3 L
D3-9 RAM UNIDATA Ø3 H
D3-3 CLEAR RAM OUTPUT Ø3 L
7408 E29
7474 E28
CV2
BK2
D3-11 RAM OUTPUT Ø3 H
D3-11 RAM OUTPUT Ø3 L

D3-3 SET RAM OUTPUT Ø2 L
D3-9 RAM UNIDATA Ø2 H
D3-3 CLEAR RAM OUTPUT Ø2 L
7408 E34
7474 E22
CV1
D3-11 RAM OUTPUT Ø2 H

D3-3 SET RAM OUTPUT Ø1 L
D3-9 RAM UNIDATA Ø1 H
D3-3 CLEAR RAM OUTPUT Ø1 L
7408 E34
7474 E22
BA1
D3-11 RAM OUTPUT Ø1 H

D3-3 SET RAM OUTPUT ØØ L
D3-9 RAM UNIDATA ØØ H
D3-3 CLEAR RAM OUTPUT ØØ L
7408 E34
7474 E15
AH2
D3-11 RAM OUTPUT ØØ H

74174 E73
D3-10 RAM UNIDATA 12 H
D3-10 RAM UNIDATA 13 H
D3-10 RAM UNIDATA 14 H
D3-10 RAM UNIDATA 15 H
D3-10 RAM UNIDATA 16 H
D3-10 RAM UNIDATA 17 H
D5 D4 D3 D2 D1 DØ
R5(1) R4(1) R3(1) R2(1) R1(1) RØ(1)
CLR CLK
EE1 DR1 ED2 EB1 EF2 EF1
D3-11 RAM OUTPUT 12 H
D3-11 RAM OUTPUT 13 H
D3-11 RAM OUTPUT 14 H
D3-11 RAM OUTPUT 15 H
D3-11 RAM OUTPUT 16 H
D3-11 RAM OUTPUT 17 H
D3-7 INIT D3 L
8815 E10

74175 E3
D3-9 RAM UNIDATA Ø8 H
D3-10 RAM UNIDATA Ø9 H
D3-10 RAM UNIDATA 10 H
D3-10 RAM UNIDATA 11 H
D3 D2 D1 DØ
R3(1) R3(Ø) R2(1) R2(Ø) R1(1) R1(Ø) RØ(1) RØ(Ø)
CLR CLK
AE2 AR2 AD2 AC1
D3-11 RAM OUTPUT Ø8 H
D3-11 RAM OUTPUT Ø9 H
D3-11 RAM OUTPUT 10 H
D3-11 RAM OUTPUT 11 H
D3-7 INIT D3 L
8815 E10

D3-3 SET RAM OUTPUT Ø7 L
D3-9 RAM UNIDATA Ø7 H
D3-3 CLEAR RAM OUTPUT Ø7 L
7474 E15
7408 E34
8815 E9
AL2
D3-11 RAM OUTPUT Ø7 H

7420 E2
7404 E77
D3-7 BUF INIT L
D3-11 RAM OUTPUT Ø-14=Ø
D3-3 CLEAR RAM OUTPUT ØØ L
7408 E34
8815 E9

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE: ROM, RAM & BRANCH (D3-11)			SIZE: D	CODE: DCSM7838-Ø-1	REV: K
SCALE: —/—	SHEET 12 OF 12		DIST.	MK	

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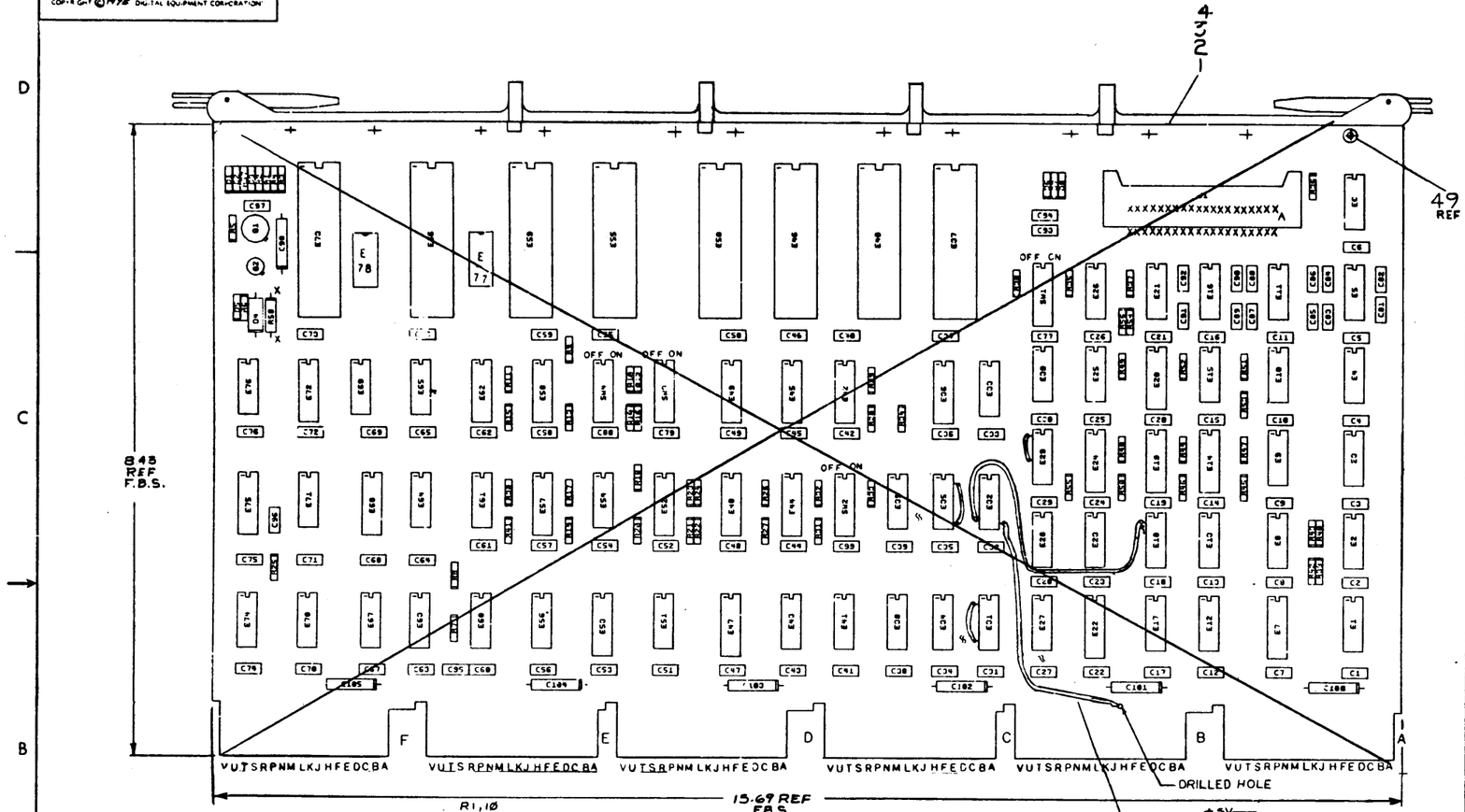
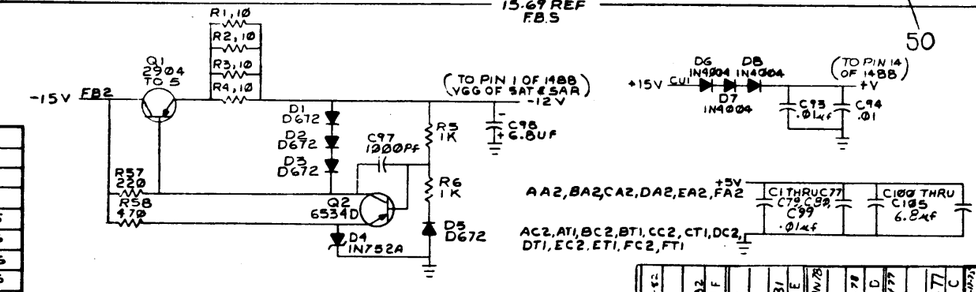
NOTES:





CAUTION:
OFF SHEET PARTS LIST
SEE K-PL-M7839-0-0

DEC 74157	8	16
DEC 74123	8	16
DEC 74155	8	16
DEC 74153	8	16
DEC 74175	8	16
PR1472B SAR	20	1
PT1482B SAT	21	1
DEC 1488	7	—
IC TYPE	GND	+5V

—	16
—	16
14	1
+V	-12

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

REV				
		X-Y COORDINATE HOLE LOCATION	K-CO-M7839-0-4	1
REF		ASSY/HOLE DRILLING LAYOUT	D-AH-M7839-0-3	2
REF		MODULE ECO HISTORY	B-MH-M7839-0-0	3
1		ETCHED CIRCUIT BOARD	5010989	4
1	C98	CAP 68 PF, 100V, 5%	1000014	5
12	C81-92	CAP 470 PF, 100V, 5%	1000024	6
1	C97	CAP 1000PF, 100V, 5%	1000047	7
83	C93,94,95,C177,89,78,80	CAP .01 UF, 100V DISC	1001810-01	8
7	C98,100-C105	CAP 6.8 UF, 35V, 10%	1006306	9
1	D4	DIODE IN752A	1102808	10
4	D1,2,3,5	DIODE D672	1105275	11
3	D6,7,8	DIODE IN4004	1105786	12
1	J1	CONN. 40 PIN.	1208941	13
4	SW1,SW2,SW3,SW4	DIPSWITCH 8-POS	1211184-04	14
4		DIPSWITCH COVER 8-POS	1211284-04	15
1	R57	RES. 220,1/4W, 5%	1300271	16
1	R7	RES. 330, 1/4W, 5%	1300335	17
1	R58	RES. 470, 1/2W, 5%	1300315	18
11	R5,8,30,38-44,26,27	RES. 1K, 1/4W, 5%	1300385	19
35	R9-THRU 25,28,29,31 THRU 34,45 THRU 56	RES. 10K,1/4W, 5%	1300479	20
4	R1 THRU R4	RES. 10, 1/4W, 5%	1301317	21
1	R8	RES. 750, 1/4W, 5%	1301401	22
4	R35 THRU 38	RES. 7.5K, 1/4W, 5%	1301422	23
1	Q1	TRANSISTOR 2904	1501742	24
1	Q2	TRANSISTOR 6534D	1503408	25
4	E21,33,17,23	DEC I.C. 7400	1905575	26
3	E64,8,9	DEC I.C. 7450	1905580	27
3	E1,12,3	DEC I.C. 7402	1909004	28
3	E39,25,34	DEC I.C. 74H11	1909267	29
10	E69,65,43,32,28,51,58,60,27,38	DEC I.C. 7474	1905547	30
3	E41,54,10	DEC I.C. 7404	1909688	31
4	E70,71,74,67	DEC I.C. 8881	1909705	32
1	E2	DEC I.C. 8242	1509712	33
3	E61,76,30	DEC I.C. 7417	1909929	34
2	E52,59	DEC I.C. 74157	1910655	35
9	E68,E36,44,48,42,62,45,49,22,	DEC I.C. 74153	1909937	36
1	E63	DEC I.C. 7437	1910091	37
5	E18,35,29,31,13	DEC I.C. 7408	1910155	38
2	E26,6	DEC I.C. 1488	1910322	39
3	E5,16,11	DEC I.C. 1489	1910323	40
5	E14,19,20,24,75	DEC I.C. 74123	1910436	41
1	E7	DEC I.C. 74175	1910651	42
4	E47,57,53,72	DEC I.C. 74155	1910656	43
2	E15,4	DEC I.C. 7432	1911521	44
4	E56,37,46,40	DEC I.C. PR1472B SAR	2111556	45
4	E66,73,59,55	DEC I.C. PT1482B SAT	2111557-01	46
1		TRAN COVER	9008351-0	47
1		HANDLE ASSY	1210711-2	48
12		EYELET	9006732	49
A/R		WIRE # 30 AWG GREEN	9105740-55	50

QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO

PARTS LIST

DEC NO.	EIA NO.
D672	IN3653
6534D	NONE
2904	2N1132

DEC NO. EIA NO.

SEMICONDUCTOR CONVERSION CHART

REV	CHANGE NO.	ORIGINATED
A	M7839-00001	J. MCNAMARA 25-July-77
B	M7839-00002	J. MCNAMARA 25-July-77
C	M7839-MK0003	R. HARRINGTON 27-DEC-78
D	M7839-MK0004	J. MCNAMARA 4-MAR-78
E	M7839-MK005	R. HARRINGTON 6-12-81
F	M7839 MK005	F. BACKES 21-JUN-82

REVISIONS

FIRST USED ON OPTION MODEL: DV11

ETCH BOARD REV: B

NEXT HIGHER ASSY: B-DD-DV11-0-0

SCALE: NONE

SHEET 1 OF 9

digital EQUIPMENT CORPORATION

TITLE: SYNC MUX LINE CARD

SIZE: D | CODE: CS | NUMBER: M7839-0-1 | REV: F

DIST

DCS M7839-0-1

MK

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BERG PINNING CHART

J1	SIGNAL
A	GROUND
B	DCE SCR ØØ
C	GROUND
D	DCE SCR Ø1
E	GROUND
F	DCE SCR Ø2
H	GROUND
J	DCE SCR Ø3
K	GROUND
L	EIA RCV DATA ØØ
M	GROUND
N	EIA RCV DATA Ø1
P	GROUND
R	EIA XMIT DATA ØØ
S	GROUND
T	EIA XMIT DATA Ø1
U	GROUND
V	DTE SCTE ØØ
W	GROUND
X	DTE SCTE Ø1
Y	DTE SCTE Ø2
Z	GROUND
A A	DTE SCTE Ø3
B B	GROUND
C C	EIA XMIT DATA Ø2
D D	GROUND
E E	EIA XMIT DATA Ø3
F F	GROUND
H H	EIA RCV DATA Ø2
J J	GROUND
K K	EIA RCV DATA Ø3
L L	GROUND
M M	DCE SCT Ø3
N N	GROUND
P P	DCE SCT Ø2
R R	GROUND
S S	DCE SCT Ø1
T T	GROUND
U U	DCE SCT ØØ
V V	GROUND

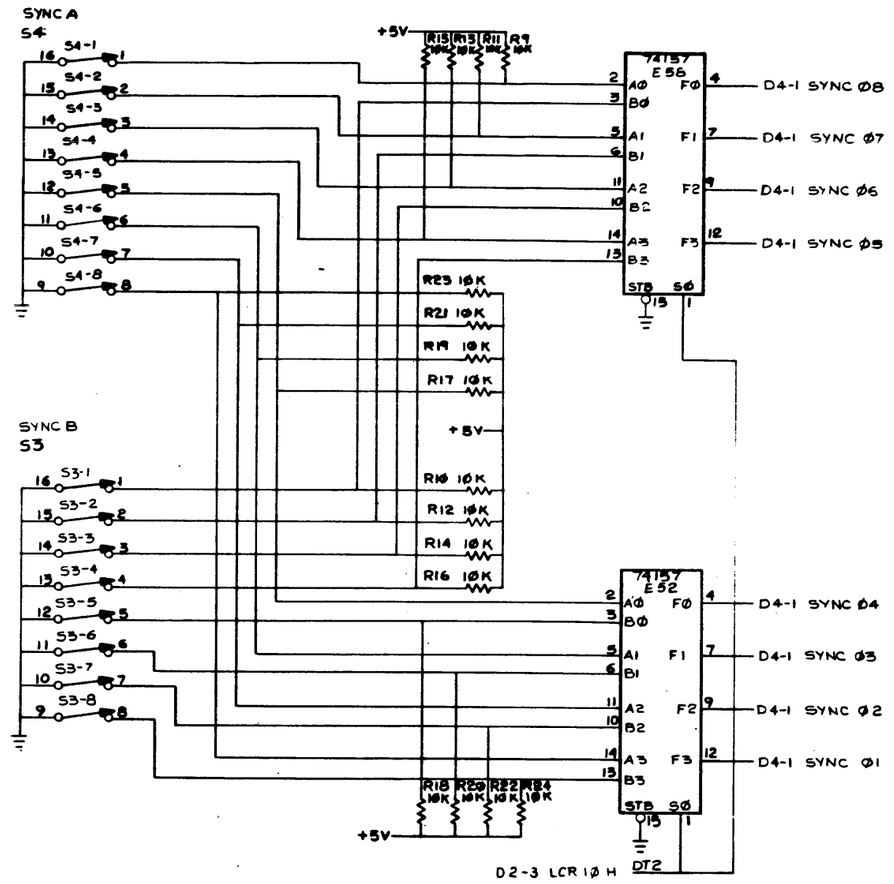
PARAMETER SWITCH SETTINGS

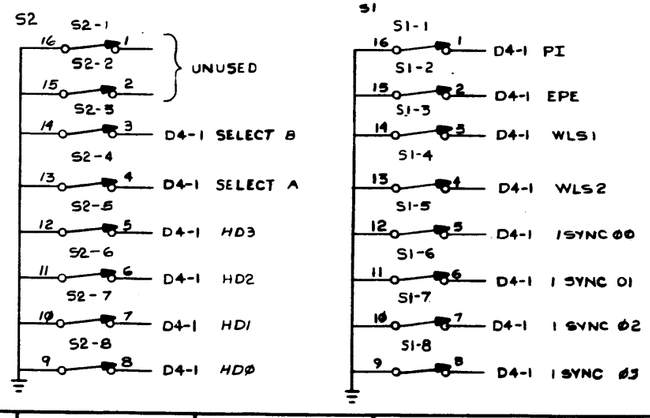
FUNCTION	SWITCH NAME	SW PACK	SW NO	PARAMETER/SETTING			
INTERNAL BAUD RATE				1200 BAUD	2400 BAUD	4800 BAUD	9600 BAUD
	SELECT B	S2	3	ON	ON	OFF	OFF
	SELECT A	S2	4	ON	OFF	ON	OFF
FULL/HALF DUPLEX				FULL DUPLEX		HALF DUPLEX	
	HD3	S2	5	ON		OFF	
	HD2	S2	6	ON		OFF	
	HD1	S2	7	ON		OFF	
	HDØ	S2	8	ON		OFF	
PARITY				NO PARITY	ODD PARITY	EVEN PARITY	
	PI	S1	1	OFF	ON	ON	
	EPE	S1	2	OFF	ON	OFF	
CHARACTER LENGTH				8 BITS/CHAR	7 BITS/CHAR	6 BITS/CHAR	5 BITS/CHAR
	WLS1	S1	3	OFF	ON	OFF	ON
	WLS2	S1	4	OFF	OFF	ON	ON
SYNC REQUIREMENT				1 SYNC REQUIREMENT		2 SYNC REQUIREMENT	
	1 SYNC ØØ	S1	5	OFF		ON	
	1 SYNC Ø1	S1	6	OFF		ON	
	1 SYNC Ø2	S1	7	OFF		ON	
	1 SYNC Ø3	S1	8	OFF		ON	
SYNC SELECT				ONE		ZERO	
LCR1Ø=Ø	SYNC A	S4	1-8	OFF		ON	
LCR1Ø=1	SYNC B	S3	1-8	OFF		ON	

PARAMETER SELECTION

FUNCTION	PARAMETER	SELECTED
TRANSMITTER CLK RATE		1X BIT RATE
	CS1	GROUND
	CS2	GROUND
TRANSMITTER MODE SEL		SYNCHRONOUS
	MS1	GROUND
	MS2	NO CONNECTION
RECEIVER MODE SEL		SYNCHRONOUS
	RMS1	NO CONNECTION
	RMS2	NO CONNECTION
	RMS3	NO CONNECTION

NOTES:
1. SWITCHES ARE MOUNTED FOR "OFF" TO THE LEFT AND "ON" TO THE RIGHT
2. FOR SYNC A OR SYNC B SELECTION S4-1 AND S3-1 RESPECTIVELY ARE THE MOST SIGNIFICANT BITS
3. PIN ER1 IS AN ASSIGNED BACKPLANE SIGNAL, "RAN DATA ØR H." NO M7839 CIRCUITRY IS CONNECTED TO IT.
4. PIN BM1 IS AN ASSIGNED BACKPLANE SIGNAL, 230.4KBH. NO M7839 CIRCUITRY IS CONNECTED TO IT.





(CHARTS, SWITCHES AND SYNC SELECTOR)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
SYNC MUX LINE CARD (D4-1)	D	CS	M7839-Ø-1	F
SCALE —	SHEET 2 OF 9	DIST.		

MK

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D4-2 CARD PARAMETER SELECT ØØ-Ø3 L DU2

D3-8 SRS Ø3 L DS2
D3-8 SRS Ø2 L BE2
7400 E23

D2-3 CONTROL STROBE H CS2 11
7404 E41
D4-2 BUF CONTROL STROBE L

D3-7 INIT DI L EN2 9
7437 EG3
D4-2 RESET H
7437 EG3
D4-2 RESET A L
7437 EG3
D4-2 RESET B L
+3V

D4-2 STROBE Ø3 L
7404 E54
D4-2 STROBE Ø3 H
D4-2 STROBE Ø2 L
7404 E54
D4-2 STROBE Ø2 H
D4-2 STROBE Ø1 L
7404 E54
D4-2 STROBE Ø1 H
D4-2 STROBE ØØ L
7404 E54
D4-2 STROBE ØØ H

D3-8 SES Ø1 H BT2
D3-8 SRS ØØ H BM2

D4-5 RCV IN Ø3 H
D4-5 RCV IN Ø2 H
D4-4 RCV IN Ø1 H
D4-4 RCV IN ØØ H
74153 E22
8881 EG7
FPI BIT WINDOW L
BE2
D4-3 INTR MAINTENANCE ØØ-Ø3 H

D3-4 TRAN DATA Ø8 H ER1 (SEE NOTE 3 ON SHEET 2 OF 9)
D3-4 TRAN DATA Ø7 H EP1 7417 EG1 D4-2 TRB H
D3-4 TRAN DATA Ø6 H EM2 7417 EG1 D4-2 TRT H
D3-4 TRAN DATA Ø5 H FR2 7417 E76 D4-2 TRA H
D3-4 TRAN DATA Ø4 H FV2 7417 E76 D4-2 TRS H
D3-4 TRAN DATA Ø3 H FS2 7417 E76 D4-2 TR4 H
D3-4 TRAN DATA Ø2 H FV1 7417 E76 D4-2 TR3 H
D3-4 TRAN DATA Ø1 H FT2 7417 E76 D4-2 TR2 H
D3-4 TRAN DATA ØØ H FU2 7417 E76 D4-2 TR1 H

D4-2 CARD FLAG SELECT ØØ-Ø3 L DM2

D3-4 MASTER SCAN D H BU2 12
D3-4 MASTER SCAN C H EN2 13
7437 EG3
7404 E41
D3-3 RESYNC PULSE L DF2

D3-3 SET TMARK L CU2 3
7404 E41

74H11 E39
D1-5 RECEIVED DATA ENABLE H CN2
FK1 D4-2 DATA ENABLE ØØ-Ø3 H

+5V
R25 10K
C96 68pf
7123 E75 RDE 300NS
FU1 RDE ØØ-Ø3 H
+5V

STBB STBA 74155 E47
D4-2 RESYNC PULSE Ø3 L
D4-2 RESYNC PULSE Ø2 L
D4-2 RESYNC PULSE Ø1 L
D4-2 RESYNC PULSE ØØ L
D4-2 SET TMARK Ø3L
D4-2 SET TMARK Ø2L
D4-2 SET TMARK Ø1L
D4-2 SET TMARK ØØL

D4-5 DA Ø3 H
D4-5 DA Ø2 H
D4-4 DA Ø1 H
D4-4 DA ØØ H
D4-7 MDET Ø3 H
D4-7 MDET Ø2 H
D4-6 MDET Ø1 H
D4-6 MDET ØØ H
74153 EG2
8881 EG7
FCI DATA NOT AVAILABLE L
FEI MATCH DETECT L

STBB STBA 74155 E57
D4-2 BUF RDE Ø3 L
D4-2 BUF RDE Ø2 L
D4-2 BUF RDE Ø1 L
D4-2 BUF RDE ØØ L
D4-2 THRL Ø3 L
D4-2 THRL Ø2 L
D4-2 THRL Ø1 L
D4-2 THRL ØØ L

D3-4 TRANSMITTER STROBE H EH2

+5V
R26 1K
D3-4 MASTER SCAN Ø1 H EM1 13
7417 EG1

+5V
R27 1K
D3-4 MASTER SCAN ØØ H EN1 5
7417 EG1

D4-5 TRAN FLAG Ø3 H
D4-5 TRAN FLAG Ø2 H
D4-4 TRAN FLAG Ø1 H
D4-4 TRAN FLAG ØØ H
D4-7 REC FLAG Ø3 H
D4-7 REC FLAG Ø2 H
D4-6 REC FLAG Ø1 H
D4-6 REC FLAG ØØ H
74153 E48
8881 E71
FLZ TRAN FLAG WAITING L
8881 E71
FM2 RECEIVER FLAG L

D4-2 BUF MASTER SCAN Ø1 H
D4-2 BUF MASTER SCAN ØØ H
D3-4 MASTER SCAN T/R CE2 13
7404 E41

REVISIONS		
ECR	CHANGE NO.	REV.

(CARD SELECTION, INIT AND TRAN DATA)

TITLE: SYNC MUX LINE CARD (D4-2)		NUMBER: DCS M7839-Ø-1	REV: F
SCALE:	SHEET 3 OF 9	DRAWN: MK	

DCS M7839-Ø-1 F

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NOTE:1) A JUMPER WIRE MAY BE SOLDERED ACROSS THE RESISTOR IF THE CUSTOMER SO REQUESTS. HOWEVER, ALL M7839 MODULES WILL BE SHIPPED WITH THE RESISTOR NOT JUMPERED TO INSURE PROPER OPERATION WITH BELL SYSTEM 201A AND 201B MODEMS.

D4-8 TMARK ØØ L — CD2 — R28 10K — +5V — D4-1 HDØ — 7400 E33

DCE SCR ØØ — J1 B — 1489 E5 — C81 470pf — 7432 E4 — 74H11 E25 — D4-3 RX CLOCK ØØ L — 7404 E41 — DS2 — D4-3 RX CLOCK ØØ H

D4-8 TMARK Ø2 L — EL2 — R33 10K — +5V — D4-1 HD2 — 7400 E38

DCE SCR Ø2 — J1 F — 1489 E5 — C83 470pf — 7432 E4 — 74H11 E39 — D4-3 RX CLOCK Ø2 L — 7404 E54 — DS2 — D4-3 RX CLOCK Ø2 H

DCE SCR Ø1 — J1 D — 1489 E5 — C82 470pf — 7432 E4 — 74H11 E25 — D4-3 RX CLOCK Ø1 L — 7404 E54 — CE2 — D4-3 RX CLOCK Ø1 H

D4-8 TMARK Ø1 L — CB2 — R29 10K — +5V — *D4-1 HD1 — 7400 E33

DCE SCR Ø3 — J1 J — 1489 E5 — C84 470pf — 7432 E4 — 74H11 E25 — D4-3 RX CLOCK Ø3 L — 7404 E41 — CP2 — D4-3 RX CLOCK Ø3 H

D4-8 TMARK Ø3 L — EE2 — R34 10K — +5V — D4-1 HD3 — 7400 E33

DCE SCT ØØ — J1 44 — 1489 E16 — C92 470 pf — 7432 E15 — 7400 E21 — D4-3 TX CLOCK ØØ H

DCE SCT Ø1 — SS — 1489 E16 — C91 470 pf — 7432 E15 — 7400 E21 — D4-3 TX CLOCK Ø1 H

DCE SCT Ø2 — PP — 1489 E16 — C90 470pf — 7432 E15 — 7400 E21 — D4-3 TX CLOCK Ø2 H

DCE SCT Ø3 — MM — 1489 E16 — C89 470pf — 7432 E15 — 7400 E21 — D4-3 TX CLOCK Ø3 H

D2-3 MAINTENANCE CLK PULSE H — ET2 — 7450 E64 — BJ1 — SOURCE CLOCK A ØØ-Ø3 L

D4-3 MUX CLOCK ØØ-Ø3 H (ES2) — D2-3 MAINTENANCE CLK PULSE H (ET2) — 7450 E64 — BN2 — SOURCE CLOCK B ØØ-Ø3 L

D4-4 MODE ØØ (1) H — 7417 E61 — D4-4 MODE Ø1 (1) H — 7408 E13 — AS2 — SYSTEM MODE ØØ-Ø3 H

R30 1K — +5V — D4-4 MODE Ø1 (Ø) H — 7408 E13 — BE2 — D4-3 INTR MAINTENANCE ØØ-Ø3 H

D3-5 9600 BAUD — FF2
D3-5 4800 BAUD — FE2
D3-5 2400 BAUD — FD2
D3-5 1200 BAUD — FD1

74LS3 E68 — STB1 STB2 — D1 C1 B1 A1 — F1 F0 — S1 S0 — ES2 — D4-3 MUX CLOCK ØØ-Ø3 H

R31 10K — +5V — R32 10K — D4-1 SELECT B — D4-1 SELECT A

BAUD RATE	TIME FOR ONE CYCLE (IN MICROSECONDS)
9600	104
4800	208
2400	417
1200	833

J1 V — R37 7.5K SEE NOTE 1 — 1488 E26 — DTE SCTE ØØ

J1 X — R36 7.5K SEE NOTE 1 — 1488 E6 — DTE SCTE Ø1

J1 Y — R35 7.5K SEE NOTE 1 — 1488 E26 — DTE SCTE Ø2

J1 AA — R38 7.5K SEE NOTE 1 — 1488 E26 — DTE SCTE Ø3

(CLOCK SOURCE AND SELECTION)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SYNC MUX LINE CARD (D4-3)
SIZE	D
CODE	CS
NUMBER	M7839-Ø-1
REV.	F
SCALE	
SHEET	4 OF 9
DIST.	

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EIA REC DATA ØØ
D2-3 LCR 14 H
D2-3 LCR 12 H
D2-3 LCR 11 H
D2-3 LCR ØØ H
D4-2 RESET A L
D4-2 CARD PARAMETER SELECT ØØ-Ø3 L
D4-2 BUF CONTROL STROBE L
D4-4 MODE ØØ (Ø) H
D4-4 MODE ØØ(1)H
D4-3 INTR MAINTENANCE ØØ-Ø3 H
D4-4 MODE Ø1(1) H
D4-4 MODE Ø1(Ø)H
D4-4 TRANS DISABLE ØØ-Ø3 H
D4-4 BUF MODE ØØ(Ø) H
D4-4 MODE ØØ(1)H
D4-4 INTR RCV DATA ØØ-Ø3 L
D4-4 RCV IN ØØ H
EIA XMIT DATA ØØ
AJ2 SERIAL OUT ØØ L
ETCH CUTS FOR YC VARIATION
D4-4 MODE ØØ (1) H
D4-8 TMARK ØØ L
D4-3 TX CLOCK ØØ H
D4-2 RESET H
D4-2 THRL ØØ L
D4-2 TR8 H
D4-2 TR7 H
D4-2 TR6 H
D4-2 TR5 H
D4-2 TR4 H
D4-2 TR3 H
D4-2 TR2 H
D4-2 TR1 H
D4-2 STROBE ØØ L
D4-1 SYNC Ø8
D4-1 SYNC Ø7
D4-1 SYNC Ø6
D4-1 SYNC Ø5
D4-1 SYNC Ø4
D4-1 SYNC Ø3
D4-1 SYNC Ø2
D4-1 SYNC Ø1
D4-1 PI
D4-1 EPE
D4-1 WLS1
D4-1 WLS2
TCO ØØ H
EOC ØØ H
D4-4 TRAN FLAG ØØ H
D4-3 TX CLOCK Ø1 H
D4-2 RESET A L
YC VARIATION
EIA REC DATA Ø1
D4-4 MODE ØØ (Ø) H
D4-4 MODE ØØ (1) H
BDI D4-4 RCV IN Ø1 H
D4-4 TRANS DISABLE ØØ-Ø3 H
SERIAL OUT Ø1 L
D4-4 BUF MODE ØØ(Ø)H
EIA XMIT DATA Ø1
D4-8 TMARK Ø1 L
D4-3 TX CLOCK Ø1 H
D4-2 RESET H
D4-2 THRL Ø1 L
D4-2 TR8 H
D4-2 TR7 H
D4-2 TR6 H
D4-2 TR5 H
D4-2 TR4 H
D4-2 TR3 H
D4-2 TR2 H
D4-2 TR1 H
D4-2 STROBE Ø1 L
D4-1 SYNC Ø8
D4-1 SYNC Ø7
D4-1 SYNC Ø6
D4-1 SYNC Ø5
D4-1 SYNC Ø4
D4-1 SYNC Ø3
D4-1 SYNC Ø2
D4-1 SYNC Ø1
D4-1 PI
D4-1 EPE
D4-1 WLS1
D4-1 WLS2
TCO Ø1 H
EOC Ø1 H
D4-4 TRAN FLAG Ø1 H
D4-3 TX CLOCK Ø1 H
D4-2 RESET A L
YC VARIATION ONLY

(MODE SELECTION, TRANSMITTERS ØØ AND Ø1).

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE: SYNC MUX LINE CARD (D4-4)	SIZE: D	CODE: CS	NUMBER: M7839-Ø-1	REV: F
SCALE:	SHEET 5 OF 9	DIST.		

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EIA REC DATA Ø2 — J1 HH — 1489 E11 — C88 470pf
D4-4 MODE ØØ (Ø) H, D4-4 MODE ØØ (1) H — 7450 E9
D4-4 TRANS DISABLE ØØ-Ø3 H (AF2) — 7402 E12
7400 E23 — BK2 — D4-5 RCV IN Ø2 H
D4-4 INTR RCV DATA ØØ-Ø3 L — BC1
D4-4 BUF MODE ØØ(Ø) H — 8242 E2 — +5V R42 1K — 1488 E6 — J1 CC — EIA XMIT DATA Ø2
D4-4 MODE ØØ (1) H — CUT ETCH: YC VAR. ONLY — 7402 E12
7404 E10 — AT2 — SERIAL OUT Ø2 L
EIA REC DATA Ø3 — J1 KK — 1489 E11 — C85 470pf
D4-4 MODE ØØ (Ø) H, D4-4 MODE ØØ (1) H — 7450 E9
7402 E3 — (AF2) D4-4 TRANS DISABLE ØØ-Ø3 H
7400 E23 — BK1 — D4-5 RCV IN Ø3 H
D4-4 BUF MODE ØØ (Ø) H — +5V R45 1K — 8242 E2 — 1488 E26 — J1 EE — EIA XMIT DATA Ø3
D4-4 MODE ØØ (1) H — 7402 E3 — ETCH CUT FOR YC VARIATION ONLY

SAT Ø2 E59 — +5 VSS, -12V VGG, 21 VDD

D4-8 TMARK Ø2 L EL2	17	CTS	
D4-3 TX CLOCK Ø2 H	5	TRC	
D4-2 RESET H	18	MR	
	10	DAR	
D4-2 THRL Ø2 L	19	THRL	
D4-2 TR8 H	38	TR8	
D4-2 TR7 H	36	TR7	
D4-2 TR6 H	34	TR6	
D4-2 TR5 H	32	TR5	
D4-2 TR4 H	30	TR4	
D4-2 TR3 H	28	TR3	
D4-2 TR2 H	26	TR2	
D4-2 TR1 H	24	TR1	
D4-2 STROBE Ø2 L	20	FHRL	
D4-1 SYNC Ø8	37	FR8	
D4-1 SYNC Ø7	35	FR7	
D4-1 SYNC Ø6	33	FR6	
D4-1 SYNC Ø5	31	FR5	
D4-1 SYNC Ø4	29	FR4	
D4-1 SYNC Ø3	27	FR3	
D4-1 SYNC Ø2	25	FR2	
D4-1 SYNC Ø1	23	FR1	
	4	CRL	
	22	CD	

TRO 15 — 7404 E10 — AH2 — SERIAL OUT Ø2 L
TCO 11 EJ2 — TCO Ø2 H
DD/EOC 13 EK2 — EOC Ø2 H
DA 12 — D4-5 DA Ø2 H
THRE 14 — D4-5 TRAN FLAG Ø2 H

+3V — E77 — D4-3 TXCLK Ø2 H, D4-2 RESET B L — 74LS74
YC VARIATION ONLY

D4-1 PI, D4-1 EPE, D4-1 WLS1, D4-1 WLS2, CS1, CS2, MS1, MS2

SAT Ø3 E55 — +5V, -12V, VSS, VGG, VDD

D4-8 TMARK Ø2L EE2	17	CTS	
D4-3 TX CLOCK Ø3 H	5	TRC	
D4-2 RESET H	18	MR	
	10	DAR	
D4-2 THRL Ø3 L	19	THRL	
D4-2 TR8 H	38	TR8	
D4-2 TR7 H	36	TR7	
D4-2 TR6 H	34	TR6	
D4-2 TR5 H	32	TR5	
D4-2 TR4 H	30	TR4	
D4-2 TR3 H	28	TR3	
D4-2 TR2 H	26	TR2	
D4-2 TR1 H	24	TR1	
D4-2 STROBE Ø3 L	20	FHRL	
D4-1 SYNC Ø8	37	FR8	
D4-1 SYNC Ø7	35	FR7	
D4-1 SYNC Ø6	33	FR6	
D4-1 SYNC Ø5	31	FR5	
D4-1 SYNC Ø4	29	FR4	
D4-1 SYNC Ø3	27	FR3	
D4-1 SYNC Ø2	25	FR2	
D4-1 SYNC Ø1	23	FR1	
	4	CRL	
	22	CD	

ETCH CUT YC VARIATION ONLY
TRO 15 — 7404 E10 — AH2 — SERIAL OUT Ø3 L
TCO 11 ED2 — TCO Ø3 H
DD/EOC 13 EF2 — EOC Ø3 H
DA 12 — D4-5 DA Ø3 H
THRE 14 — D4-5 TRAN FLAG Ø3 H

+3V — E77 — D4-3 TXCLOCK Ø3 H, D4-2 RESET B L — 74LS74
YC VARIATION ONLY

D4-1 PI, D4-1 EPE, D4-1 WLS1, D4-1 WLS2, CS1, CS2, MS1, MS2

(TRANSMITTERS Ø2 AND Ø3)

REVISIONS: CHK | CHANGE NO. | REV.

TITLE: SYNC MUX LINE CARD (D4-5)
SIZE D | CODE CS | NUMBER M7839-Ø-1 | REV. F
SCALE | SHEET 6 OF 9 | DIST. MK

DCS M7839-Ø-1 F

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+5V -12V VSS VGG VDD

D4-3 RX CLOCK ØØ H — DE2 31 — RRC
D4-4 RCV IN ØØ H — BDI 35 — RI
D4-2 RESET H — 32 — MR

SAR ØØ E50

CLR FLAG ØØ L — BV2
D4-2 BUF RDE ØØ L — 7408 E55 — 24 SFR, 25 DRR
DD2 RESYNC 2 ØØ (Ø) H — D4-2 STROBE ØØ L — 34 MHRL

D4-1 SYNC Ø8 — 40 — MHR8
D4-1 SYNC Ø7 — 4 — MHR7
D4-1 SYNC Ø6 — 38 — MHR6
D4-1 SYNC Ø5 — 3 — MHR5
D4-1 SYNC Ø4 — 36 — MHR4
D4-1 SYNC Ø3 — 17 — MHR3
D4-1 SYNC Ø2 — 22 — MHR2
D4-1 SYNC Ø1 — 18 — MHR1
33 CRL
6 CD PI EPE WLS1 WLS2 RMS3 RMS2 RMS1 SS — 19 21 5 23 2 39 37 28

D4-1 PI
D4-1 EPE
D4-1 WLS1
D4-1 WLS2

RR9 7 — D4-6 RR9 ØØ
RR8 8 — D4-6 RR8 ØØ
RR7 9 — D4-6 RR7 ØØ
RR6 10 — D4-6 RR6 ØØ
RR5 11 — D4-6 RR5 ØØ
RR4 12 — D4-6 RR4 ØØ
RR3 13 — D4-6 RR3 ØØ
RR2 14 — D4-6 RR2 ØØ
RR1 15 — D4-6 RR1 ØØ
PE 29 — D4-6 PE ØØ
OE 27 — D4-6 OE ØØ

+5V R47 10K
74123 E14 75NS — AR2 — DR ØØ H
DR 26
+3V

D4-6 MDET ØØ H — 74Ø8 E18 — 74123 E14 75NS — AV2 — MDET ØØ H
MDET 30
+5V R46 10K
D4-1 1 SYNC ØØ — R45 10K — +5V

D4-6 REC FLAG ØØ H — 74Ø8 E18
7474 E28 RCV FLAG — BV2 — CLR FLAG ØØ L

D4-6 BUF LCR 13 H
D4-2 RESYNC PULSE ØØ L — DL2
D2-3 LCR 13 H — BAI — 7417 E30
+5V R44 1K +3V
D4-2 STROBE ØØ H — 7474 E60 SEARCH SYNC
D4-3 RX CLOCK ØØ H — DE2
7408 E35 — 7474 E28 RESYNC — 7417 E30 — DD2 RESYNC 2 ØØ (Ø) H
D4-3 RX CLOCK ØØ L — CV2 — RESYNC 1 ØØ (Ø) H
74H11 E39
D4-2 RESET A L

D4-3 RX CLOCK Ø1 H — CE2 31 — RRC
D4-4 RCV IN Ø1 H — BDI 35 — RI
D4-2 RESET H — 32 — MR

SAR Ø1 E37

CLR FLAG Ø1 L — BF1
D4-2 BUF RDE Ø1 L — 7408 E18 — 24 SFR, 25 DRR
RESYNC 2 Ø1 (Ø) H — CF2 — D4-2 STROBE Ø1 L — 34 MHRL

D4-1 SYNC Ø8 — 40 — MHR8
D4-1 SYNC Ø7 — 4 — MHR7
D4-1 SYNC Ø6 — 38 — MHR6
D4-1 SYNC Ø5 — 3 — MHR5
D4-1 SYNC Ø4 — 36 — MHR4
D4-1 SYNC Ø3 — 17 — MHR3
D4-1 SYNC Ø2 — 22 — MHR2
D4-1 SYNC Ø1 — 18 — MHR1
33 CRL
6 CD PI EPE WLS1 WLS2 RMS3 RMS2 RMS1 SS — 19 21 5 23 2 39 37 28

D4-1 PI
D4-1 EPE
D4-1 WLS1
D4-1 WLS2

RR9 7 — D4-6 RR9 Ø1
RR8 8 — D4-6 RR8 Ø1
RR7 9 — D4-6 RR7 Ø1
RR6 10 — D4-6 RR6 Ø1
RR5 11 — D4-6 RR5 Ø1
RR4 12 — D4-6 RR4 Ø1
RR3 13 — D4-6 RR3 Ø1
RR2 14 — D4-6 RR2 Ø1
RR1 15 — D4-6 RR1 Ø1
PE 29 — D4-6 PE Ø1
OE 27 — D4-6 OE Ø1

+5V R48 10K
74123 E19 75NS — AU2 — DR Ø1 H
DR 26
+3V

D4-6 MDET Ø1 H — 74Ø8 E35 — 74123 E19 75NS — BH1 — MDET Ø1 H
MDET 30
+5V R49 10K
D4-1 1 SYNC Ø1 — R86 10K — +5V

74Ø8 E18 — 7474 E28B RCV FLAG — BF1 — CLR FLAG Ø1 L

D4-2 RESYNC PULSE Ø1 L — DK2
D4-6 BUF LCR 13 H
D4-2 STROBE Ø1 H — 7474 E60 SEARCH SYNC
D4-3 RX CLOCK Ø1 H — CE2
7408 E35 — 7474 E32 RESYNC — 7417 E30 — CF2 RESYNC 2 Ø1 (Ø) H
D4-3 RX CLOCK Ø1 L — BH2 — RESYNC 1 Ø1 (Ø) H
74H11 E34

(RECEIVERS ØØ AND Ø1, RESYNC)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE: SYNC MUX LINE CARD (D4-6)		SIZE/CODE: D CS	NUMBER: M7839-Ø-1
SCALE:	SHEET 7 OF 9	DIST.	REV. F

DCS M7839-Ø-1 F

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+5V -12V
VSS VGG VDD
D4-3 RX CLOCK Ø2 H DS2 31 RRC
D4-5 RCV IN Ø2 H BK2 35 RI
D4-2 RESET H 32 MR
SAR Ø2 E46
CLR FLAG Ø2 L BU2
D4-2 BUF RDE Ø2 L
7408 E29
24 SFR
25 DRR
DR2
D4-2 STROBE Ø2 L 34 MHRL
RESYNC 2 Ø2 (Ø) H
D4-1 SYNC Ø8 40 MHR8
D4-1 SYNC Ø7 4 MHR7
D4-1 SYNC Ø6 38 MHR6
D4-1 SYNC Ø5 3 MHR5
D4-1 SYNC Ø4 36 MHR4
D4-1 SYNC Ø3 17 MHR3
D4-1 SYNC Ø2 22 MHR2
D4-1 SYNC Ø1 18 MHR1
33 CRL
6 CDPI EPE WLS1 WLS2 RMS3 RMS2 RMS1 SS
19 21 5 23 2 39 37 28
D4-1 PI
D4-1 EPE
D4-1 WLS1
D4-1 WLS2
RR9 7
RR8 8 D4-7 RR8 Ø2
RR7 9 D4-7 RR7 Ø2
RR6 10 D4-7 RR6 Ø2
RR5 11 D4-7 RR5 Ø2
RR4 12 D4-7 RR4 Ø2
RR3 13 D4-7 RR3 Ø2
RR2 14 D4-7 RR2 Ø2
RR1 15 D4-7 RR1 Ø2
PE 29 D4-7 PE Ø2
OE 27 D4-7 OE Ø2
DR 26
+5V R51 10K
7408 E29
7423 E20 75NS
BB1 DR Ø2 H
+3V
7408 E29
7474 E27 RCV FLAG
BU2 CLR FLAG Ø2 L
+5V R52 10K
D4-7 MDET Ø2 H
MDET 30 12
7408 E29
74123 E20 75NS
BJ2 MDET Ø2 H
R53 10K +5V
D4-1 I SYNC Ø2
D4-2 RESYNC PULSE Ø2 L DJ2
7417 E30
DR2 RESYNC 2 Ø2 (Ø) H
D4-3 RX CLOCK Ø2 H DS2
+3V
D4-6 BUF LCR 13 H
D4-2 STROBE Ø2 H
7474 E56 RESYNC SYNC
7408 E29
7474 E51 RESYNC
7474 E51 RESYNC
D4-3 RX CLOCK Ø2 L
DN2
7411 E34
RESYNC 1 Ø2 (Ø) H
D4-2 RESET B L

+5V -12V
VSS VGG VDD
D4-3 RX CLOCK Ø3 H CP2 31 RRC
D4-5 RCV IN Ø3 H BK1 35 RI
D4-2 RESET H 32 MR
SAR Ø3 E40
CLR FLAG Ø3 L BV1
D4-2 BUF RDE Ø3 L
7408 E31
24 SFR
25 DRR
RESYNC 2 Ø3 (Ø) H CM2
D4-2 STROBE Ø3 L 34 MHRL
D4-7 REC FLAG Ø2 H
D4-1 SYNC Ø8 40 MHR8
D4-1 SYNC Ø7 4 MHR7
D4-1 SYNC Ø6 38 MHR6
D4-1 SYNC Ø5 3 MHR5
D4-1 SYNC Ø4 36 MHR4
D4-1 SYNC Ø3 17 MHR3
D4-1 SYNC Ø2 22 MHR2
D4-1 SYNC Ø1 18 MHR1
33 CRL
6 CDPI EPE WLS1 WLS2 RMS3 RMS2 RMS1 SS
19 21 5 23 2 39 37 28
D4-1 PI
D4-1 EPE
D4-1 WLS1
D4-1 WLS2
RR9 7
RR8 8 D4-7 RR8 Ø3
RR7 9 D4-7 RR7 Ø3
RR6 10 D4-7 RR6 Ø3
RR5 11 D4-7 RR5 Ø3
RR4 12 D4-7 RR4 Ø3
RR3 13 D4-7 RR3 Ø3
RR2 14 D4-7 RR2 Ø3
RR1 15 D4-7 RR1 Ø3
PE 29 D4-7 PE Ø3
OE 27 D4-7 OE Ø3
DR 26
+5V R54 10K
74123 E24 75NS
BL2 DR Ø3 H
+3V
7408 E31
7474 E27 RCV FLAG
BV1 CLR FLAG Ø3 L
+5V R55 10K
D4-7 MDET Ø3 H
MDET 30 9
7408 E31
74123 E24 75NS
BP2 MDET Ø3 H
R56 10K +5V
D4-1 I SYNC Ø3
D4-2 RESYNC PULSE Ø3 L DH2
7417 E30
CM2 RESYNC 2 Ø3 (Ø) H
D4-3 RX CLOCK Ø3 H CP2
+3V
D4-6 BUF LCR 13 H
D4-2 STROBE Ø3 H
7474 E56 RESYNC SYNC
7408 E31
7474 E38 RESYNC
7474 E38 RESYNC
D4-3 RX CLOCK Ø3 L
CK2
7411 E34
RESYNC 1 Ø3 (Ø) H

(RECEIVERS Ø2 AND Ø3, RESYNC)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
SYNC MUX LINE CARD (D4-7)	D	CS	M7839-Ø-1	F
SCALE	SHEET 8 OF 9	DIST.		

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D4-7 RR6 Ø3 — D4-7 RR6 Ø2 — D4-6 RR6 Ø1 — D4-6 RR6 ØØ — D4-7 RR5 Ø3 — D4-7 RR5 Ø2 — D4-6 RR5 Ø1 — D4-6 RR5 ØØ

74153 STBI STBØ DI E42 CI BI AI CØ CØ BØ AØ SI SØ F1 FØ

8881 E74 → 4 FRI RECV DATA Ø5 L

8881 E74 → 1 FSI RECV DATA Ø4 L

D4-7 PE Ø3 — D4-7 PE Ø2 — D4-6 PE Ø1 — D4-6 PE ØØ — D4-7 OE Ø3 — D4-7 OE Ø2 — D4-6 OE Ø1 — D4-6 OE ØØ

74155 STBI STBØ DI E44 CI BI AI DØ CØ BØ AØ SI SØ F1 FØ

8881 E70 → 1 FMI MASTER PE L

8881 E70 → 4 FLI MASTER OR L

D4-7 RR4 Ø3 — D4-7 RR4 Ø2 — D4-6 RR4 Ø1 — D4-6 RR4 ØØ — D4-7 RR3 Ø3 — D4-7 RR3 Ø2 — D4-6 RR3 Ø1 — D4-6 RR3 ØØ

74153 STBI STBØ DI E45 CI BI AI DØ CØ BØ AØ SI SØ F1 FØ

8881 E74 → 13 FNI RECV DATA Ø5 L

8881 E74 → 10 FPI RECV DATA Ø2 L

D3 3 CLEAR TMARK L FK2 15

74155 STBB STBA E72 DB DA FB3 FB2 FB1 FB0 FA3 FA2 FA1 FAØ SI SØ

D4-2 SET TMARK Ø3 L

7474 E69 T MARK Ø3 → EE2 D4-8 TMARK Ø3 L

D4-2 SET TMARK Ø2 L

7474 E69 T MARK Ø2 → EL2 D4-8 TMARK Ø2 L

D4-2 SET TMARK Ø1 L

7474 E65 T MARK Ø1 → CB2 D4-8 TMARK Ø1 L

D4-2 SET TMARK ØØ L

7474 E65 T MARK ØØ → CD2 D4-8 TMARK ØØ L

D4-2 RESET H

D4-2 CARD FLAG SELECT ØØ-Ø3 L DM2

D4-7 RR2 Ø3 — D4-7 RR2 Ø2 — D4-6 RR2 Ø1 — D4-6 RR2 ØØ — D4-7 RR1 Ø3 — D4-7 RR1 Ø2 — D4-6 RR1 Ø1 — D4-6 RR1 ØØ

74153 STBI STBØ DI E49 CI BI AI DØ CØ BØ AØ SI SØ F1 FØ

8881 E71 → 4 FN2 RECV DATA Ø1 L

8881 E71 → 1 FP2 RECV DATA ØØ L

D4-7 RR8 Ø3 — D4-7 RR8 Ø2 — D4-6 RR8 Ø1 — D4-6 RR8 ØØ — D4-7 RR7 Ø3 — D4-7 RR7 Ø2 — D4-6 RR7 Ø1 — D4-6 RR7 ØØ

74153 STBI STBØ DI E36 CI BI AI DØ CØ BØ AØ SI SØ F1 FØ

8881 E70 → 13 FHI RECV DATA Ø7 L

8881 E70 → 10 FJI RECV DATA Ø6 L

D4-2 BUF MASTER SCAN Ø1 H

L4-2 BUF MASTER SCAN ØØ H

D4-2 DATA ENABLE ØØ-Ø3 H (FK1)

REVISIONS

CHK	CHANGE NO.	REV.

(RECV DATA MUX'S AND TMARK DECODER)

TITLE	SIZE	CODE	NUMBER	REV.
SYNC MUX LINE CARD (D4-8)	D	CS	M7839-Ø-1	F

SCALE — SHEET 9 OF 9 — DIST. MK

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BERG PINNING CHART

J1	SIGNAL
A	GROUND
B	DCE SCR ØØ
C	GROUND
D	DCE SCR Ø1
E	GROUND
F	DCE SCR Ø2
H	GROUND
J	DCE SCR Ø3
K	GROUND
L	EIA RCV DATA ØØ
M	GROUND
N	EIA RCV DATA Ø1
P	GROUND
R	EIA XMIT DATA ØØ
S	GROUND
T	EIA XMIT DATA Ø1
U	GROUND
V	DTE SCTE ØØ
W	GROUND
X	DTE SCTE Ø1
Y	DTE SCTE Ø2
Z	GROUND
A A	DTE SCTE Ø3
B B	GROUND
C C	EIA XMIT DATA Ø2
D D	GROUND
E E	EIA XMIT DATA Ø3
F F	GROUND
H H	EIA RCV DATA Ø2
J J	GROUND
K K	EIA RCV DATA Ø3
L L	GROUND
M M	DCE SCT Ø3
N N	GROUND
P P	DCE SCT Ø2
R R	GROUND
S S	DCE SCT Ø1
T T	GROUND
U U	DCE SCT ØØ
V V	GROUND

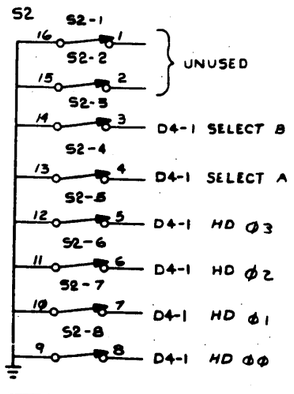
PARAMETER SWITCH SETTINGS

FUNCTION	SWITCH NAME	SW PACK	SW NO	PARAMETER/SETTING			
INTERNAL BAUD RATE				1200 BAUD	2400 BAUD	4800 BAUD	9600 BAUD
	SELECT B	S2	3	ON	ON	OFF	OFF
	SELECT A	S2	4	ON	OFF	ON	OFF
FULL/HALF DUPLEX				FULL DUPLEX		HALF DUPLEX	
	HDØ3	S2	5	ON		OFF	
	HDØ2	S2	6	ON		OFF	
	HDØ1	S2	7	ON		OFF	
	HDØØ	S2	8	ON		OFF	
PARITY				NO PARITY	ODD PARITY	EVEN PARITY	
	PI	S1	1	OFF	ON	ON	
	EPE	S1	2	OFF	ON	OFF	
CHARACTER LENGTH				8 BITS/CHAR	7 BITS/CHAR	6 BITS/CHAR	5 BITS/CHAR
	WLS1	S1	3	OFF	ON	OFF	ON
	WLS2	S1	4	OFF	OFF	ON	ON
SYNC REQUIREMENT				1 SYNC REQUIREMENT		2 SYNC REQUIREMENT	
	1 SYNC ØØ	S1	5	OFF		ON	
	1 SYNC Ø1	S1	6	OFF		ON	
	1 SYNC Ø2	S1	7	OFF		ON	
	1 SYNC Ø3	S1	8	OFF		ON	
SYNC SELECT				ONE		ZERO	
LCR10=Ø	SYNC A	S4	1↕8	OFF		ON	
LCR10=1	SYNC B	S3	1↕8	OFF		ON	

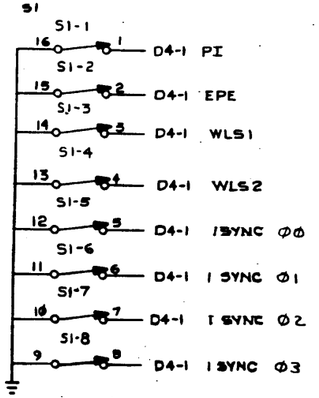
PARAMETER SELECTION

FUNCTION	PARAMETER	SELECTED
TRANSMITTER CLK RATE		1X BIT RATE
	CS1 CS2	GROUND GROUND
TRANSMITTER MODE SEL		SYNCHRONOUS
	MS1 MS2	GROUND NO CONNECTION
RECEIVER MODE SEL		SYNCHRONOUS
	RMS1 RMS2 RMS3	NO CONNECTION NO CONNECTION NO CONNECTION

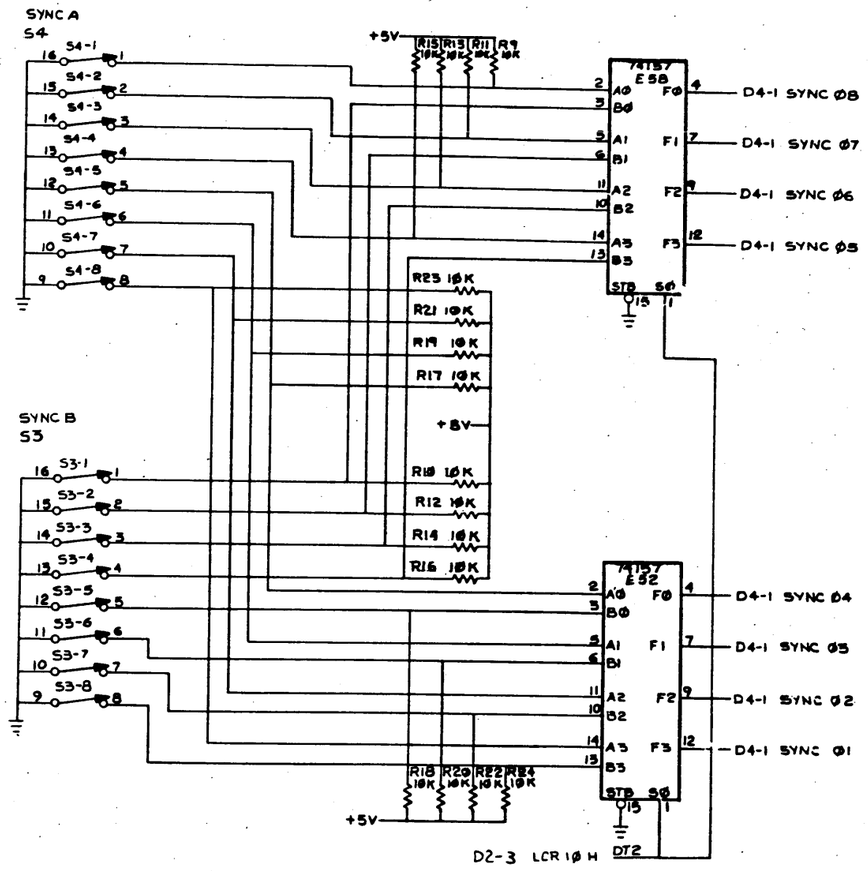
S2



S1



NOTES:
1. SWITCHES ARE MOUNTED FOR "OFF" TO THE LEFT AND "ON" TO THE RIGHT
2. FOR SYNC A OR SYNC B SELECTION S4-1 AND S3-1 RESPECTIVELY ARE THE MOST SIGNIFICANT BITS
3. PIN ER1 IS AN ASSIGNED BACKPLANE SIGNAL, TRAN DATA ØØ H. NO M7839 CIRCUITRY IS CONNECTED TO 1T.
4. PIN BM1 IS AN ASSIGNED BACKPLANE SIGNAL, 230.4KBH. NO M7839 CIRCUITRY IS CONNECTED TO 1T.



D2-3 LCR 1Ø H

D3-5 230.4 KB H BM1
(SEE NOTE 4)

(CHARTS SWITCHES AND SYNC SELECTOR)

REVISIONS		
CHK	CHANGE NO.	REV.
	DVII-00006	A
D Chiasson 20 Sept 77		
J McNAMARA 21 Dec 77		

DRN		4/8/77
CHK		4/8/77
ENG.		
PROJ. ENG.		
PROD.		
NEXT HIGHER ASSY.	B-DD-DVII-Ø	
SCALE		
SHEET 1 OF 8		

FIRST USED ON: DVII

digital

TITLE: SYNC MUX LINE CARD LINES ØØ-Ø3 (D4-1)

SIZE	CODE	NUMBER	REV.
D	BS	DVII-Ø-1Ø	A

DIST.

DVII-Ø-1Ø

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D4-2 CARD PARAMETER SELECT ØØ-Ø3 L DU2

D3-8 SRS Ø3 L BS2 — 7400 E23

D3-8 SRS Ø2 L BE2

D2-3 CONTROL STROBE H CS2 11 — 7404 E41 — D4-2 BUF CONTROL STROBE L

STBB STBA 74155 E53

D4-2 STROBE Ø3 L — 7404 E54 — D4-2 STROBE Ø3 H

D4-2 STROBE Ø2 L — 7404 E54 — D4-2 STROBE Ø2 H

D4-2 STROBE Ø1 L — 7404 E54 — D4-2 STROBE Ø1 H

D4-2 STROBE ØØ L — 7404 E54 — D4-2 STROBE ØØ H

D3-7 INIT DI L EN2 9 — 7437 E63 — D4-2 RESET H

7437 E63 — D4-2 RESET A L

7437 E63 — D4-2 RESET B L

+3V

D3-8 SRS Ø1 H BT2

D3-8 SRS ØØ H BM2

D4-5 RCV IN Ø3 H
D4-5 RCV IN Ø2 H
D4-4 RCV IN Ø1 H
D4-4 RCV IN ØØ H

STBI STBB 74153 E22 — 8881 E67 — FFI BIT WINDOW L

BE2

D4-3 INTR MAINTENANCE ØØ-Ø3 H

D3-4 TRAN DATA Ø8 H ERI (SEE NOTE 3 ON SHEET 1 OF 8)

D3-4 TRAN DATA Ø7 H EP1 — 7417 E61 — D4-2 TR8 H

D3-4 TRAN DATA Ø6 H EM2 — 7417 E61 — D4-2 TR7 H

D3-4 TRAN DATA Ø5 H FR2 — 7417 E76 — D4-2 TR6 H

D3-4 TRAN DATA Ø4 H FV2 — 7417 E76 — D4-2 TR5 H

D3-4 TRAN DATA Ø3 H FS2 — 7417 E76 — D4-2 TR4 H

D3-4 TRAN DATA Ø2 H FV1 — 7417 E76 — D4-2 TR3 H

D3-4 TRAN DATA Ø1 H FT2 — 7417 E76 — D4-2 TR2 H

D3-4 TRAN DATA ØØ H FU2 — 7417 E76 — D4-2 TR1 H

D4-2 CARD FLAG SELECT ØØ-Ø3 L DM2

D3-4 MASTER SCAN D H BU2 12
D3-4 MASTER SCAN C H EN2 13 — 7437 E63 — 7404 E41

D3-3 RESYNC PULSE L DF2

STBB STBA 74155 E47

D4-2 RESYNC PULSE Ø3 L DH2
D4-2 RESYNC PULSE Ø2 L DJ2
D4-2 RESYNC PULSE Ø1 L DK2
D4-2 RESYNC PULSE ØØ L DL2

D3-3 SET TMARK L CU2 — 7404 E41

D4-2 SET TMARK Ø3 L
D4-2 SET TMARK Ø2 L
D4-2 SET TMARK Ø1 L
D4-2 SET TMARK ØØ L

D4-5 DA Ø3 H
D4-5 DA Ø2 H
D4-4 DA Ø1 H
D4-4 DA ØØ H

D4-7 MDET Ø3 H
D4-7 MDET Ø2 H
D4-6 MDET Ø1 H
D4-6 MDET ØØ H

STBI STBA 74153 E62 — 8881 E67 — FCI DATA NOT AVAILABLE L

8881 E67 — FEI MATCH DETECT L

D1-5 RECEIVED DATA ENABLE H CN2 — 74H11 E39 — FXI D4-2 DATA ENABLE ØØ-Ø3 H

+5V — R25 10K — C96 68pf — 74123 E75 RDE 300NS — FUI RDE ØØ-Ø3 H — +3V

D3-4 TRANSMITTER STROBE H EH2

STBB STBA 74155 E57

D4-2 BUF RDE Ø3 L
D4-2 BUF RDE Ø2 L
D4-2 BUF RDE Ø1 L
D4-2 BUF RDE ØØ L

D4-2 THRL Ø3 L
D4-2 THRL Ø2 L
D4-2 THRL Ø1 L
D4-2 THRL ØØ L

D4-5 TRAN FLAG Ø3 H
D4-5 TRAN FLAG Ø2 H
D4-4 TRAN FLAG Ø1 H
D4-4 TRAN FLAG ØØ H

D4-7 REC FLAG Ø3 H
D4-7 REC FLAG Ø2 H
D4-6 REC FLAG Ø1 H
D4-6 REC FLAG ØØ H

STBI STBB 74153 E48 — 8881 E71 — FLZ TRAN FLAG WAITING L

8881 E71 — FMZ RECEIVER FLAG L

+5V — R26 1K — D3-4 MASTER SCAN Ø1 H EM1 — 7417 E61

+5V — R27 1K — D3-4 MASTER SCAN ØØ H EN1 — 7417 E61

D4-2 BUF MASTER SCAN Ø1 H

D4-2 BUF MASTER SCAN ØØ H

D3-4 MASTER SCAN T/R CR2 — 7404 E41

(CARD SELECTION, INIT AND TRAN DATA)

REVISIONS

CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
SYNC MUX LINE CARD LINES Ø0-Ø3 (D4-2)	D	BS	DV11-Ø-1Ø	A
SCALE	SHEET 2 OF 8	DIST.		

DV11-Ø-1Ø A

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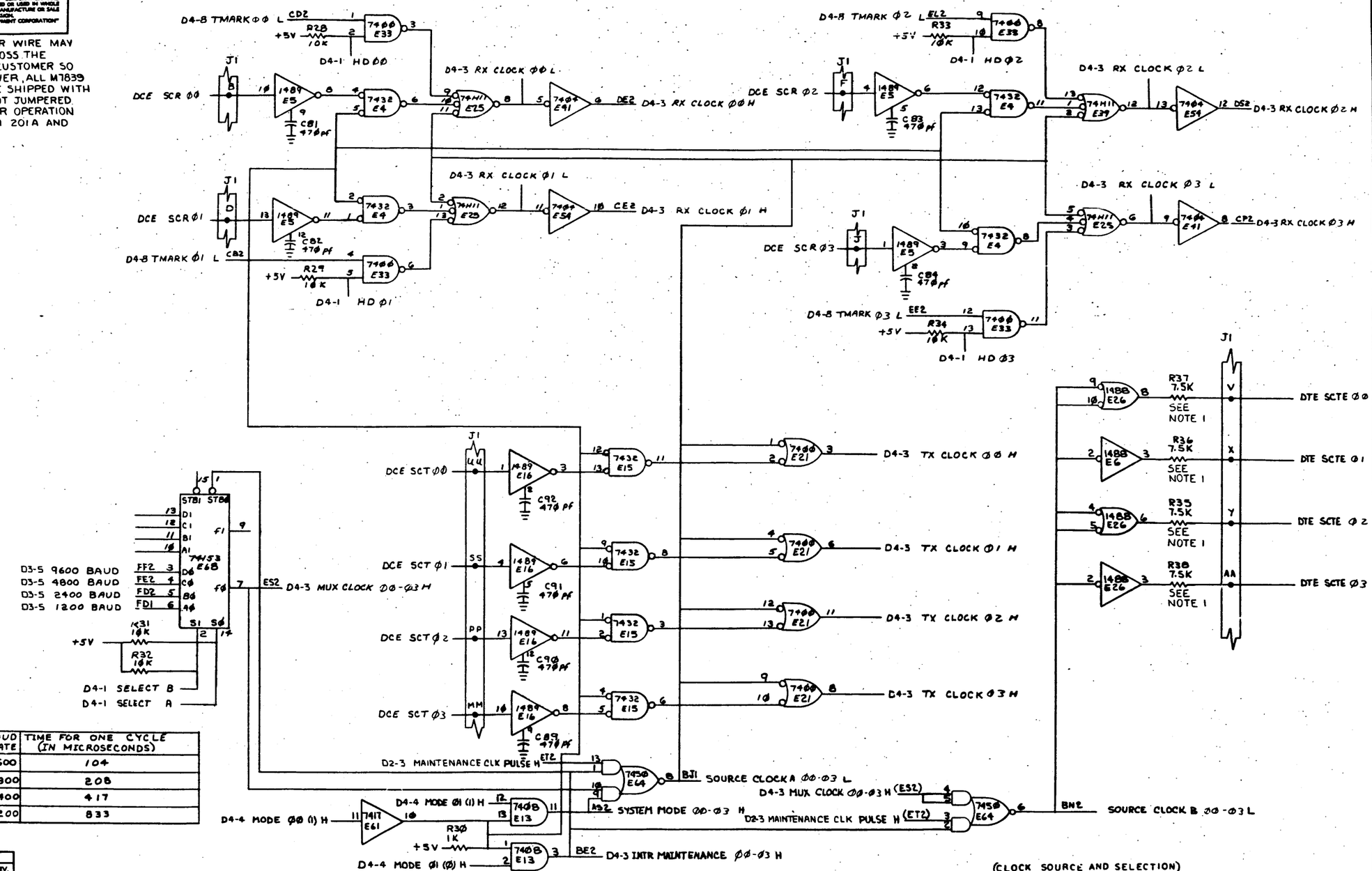
NOTE 1) A JUMPER WIRE MAY BE SOLDERED ACROSS THE RESISTOR IF THE CUSTOMER SO REQUESTS. HOWEVER, ALL M7839 MODULES WILL BE SHIPPED WITH THE RESISTOR NOT JUMPERED TO INSURE PROPER OPERATION WITH BELL SYSTEM 201A AND 201B MODEMS.



BAUD RATE	TIME FOR ONE CYCLE (IN MICROSECONDS)
9600	104
4800	208
2400	417
1200	833

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE SYNC MUX LINE CARD LINES ØØ-Ø3 (D4-3)

SIZE D | CODE BS | NUMBER DV11-Ø-1Ø | REV. A

SCALE | SHEET 3 OF 8 | DIST.

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D4-4 MODE ØØ (0) H
D4-4 MODE ØØ (1) H
D4-4 RCV IN ØØ H
D4-4 INTR RCV DATA ØØ-Ø3 L
D4-3 INTR MAINTENANCE ØØ-Ø3 H
D4-4 MODE Ø1 (0) H
D4-4 MODE Ø1 (1) H
D4-4 TRANS DISABLE ØØ-Ø3 H
D4-4 BUF MODE ØØ (0) H
D4-2 RESET A L
D4-2 CARD PARAMETER SELECT ØØ-Ø3 L
D4-2 BUF CONTROL STROBE L
SERIAL OUT ØØ L
D4-4 MODE ØØ (1) H
EIA XMIT DATA ØØ
D4-8 TMARK ØØ L
D4-3 TX CLOCK ØØ H
D4-2 RESET H
D4-2 THRL ØØ L
D4-2 TR8 H
D4-2 TR7 H
D4-2 TR6 H
D4-2 TR5 H
D4-2 TR4 H
D4-2 TR3 H
D4-2 TR2 H
D4-2 TR1 H
D4-2 STROBE ØØ L
D4-1 SYNC Ø8
D4-1 SYNC Ø7
D4-1 SYNC Ø6
D4-1 SYNC Ø5
D4-1 SYNC Ø4
D4-1 SYNC Ø3
D4-1 SYNC Ø2
D4-1 SYNC Ø1
D4-1 PI
D4-1 EPE
D4-1 WLS1
D4-1 WLS2
TCO ØØ H
EOC ØØ H
D4-4 DA ØØ H
D4-4 TRAN FLAG ØØ H
EIA REC DATA Ø1
D4-4 MODE ØØ (0) H
D4-4 MODE ØØ (1) H
D4-4 RCV IN Ø1 H
D4-4 TRANS DISABLE ØØ-Ø3 H
SERIAL OUT Ø1 L
D4-4 MODE ØØ (0) H
D4-4 BUF MODE ØØ (0) H
EIA XMIT DATA Ø1
D4-8 TMARK Ø1 L
D4-3 TX CLOCK Ø1 H
D4-2 RESET H
D4-2 THRL Ø1 L
D4-2 TR8 H
D4-2 TR7 H
D4-2 TR6 H
D4-2 TR5 H
D4-2 TR4 H
D4-2 TR3 H
D4-2 TR2 H
D4-2 TR1 H
D4-2 STROBE Ø1 L
D4-1 SYNC Ø8
D4-1 SYNC Ø7
D4-1 SYNC Ø6
D4-1 SYNC Ø5
D4-1 SYNC Ø4
D4-1 SYNC Ø3
D4-1 SYNC Ø2
D4-1 SYNC Ø1
D4-1 PI
D4-1 EPE
D4-1 WLS1
D4-1 WLS2
TCO Ø1 H
EOC Ø1 H
D4-4 DA Ø1 H
D4-4 TRAN FLAG Ø1 H

REVISIONS

CHK	CHANGE NO.	REV.

(MODE SELECTION, TRANSMITTERS ØØ AND Ø1)

TITLE	SIZE	CODE	NUMBER	REV.
SYNC MUX LINE CARD LINES ØØ-Ø3 (D4-4)	D	DBS	DV11-Ø-10	A

SCALE — SHEET 4 OF 8 — DIST.

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EIA REC DATA Ø2 — J1 HH — 1489 E11 — CBB 470pf
D4-4 MODE ØØ (Ø) H, D4-4 MODE ØØ (1) H — 7450 E9 — 7400 E23 — BK2 — D4-5 RCV IN Ø2 H
D4-4 TRANS DISABLE ØØ-Ø3 H (AF2) — 7402 E12
D4-4 INTR RCV DATA ØØ-Ø3 L — BC1
D4-4 MODE ØØ (1) H — 7402 E12 — 7404 E10 — AT2 — SERIAL OUT Ø2 L
D4-4 BUF MODE ØØ (Ø) H — 8242 E2 — +5V R42 1K — 1488 E6 — J1 CC — EIA XMIT DATA Ø2
EIA REC DATA Ø3 — J1 KK — 1489 E11 — CB5 470pf
D4-4 MODE ØØ (Ø) H, D4-4 MODE ØØ (1) H — 7450 E9 — 7400 E23 — BK1 — D4-5 RCV IN Ø3 H
D4-4 MODE ØØ (1) H — 7402 E3 — 7402 E3 — (AF2) — D4-4 TRANS DISABLE ØØ-Ø3 H
D4-4 BUF MODE ØØ (Ø) H — +5V R43 1K — 8242 E2 — 1488 E26 — J1 EE — EIA XMIT DATA Ø3

SAT Ø2 E59 — +5V -12V — VSS VGG VDD
D4-8 TMARK Ø2 L — EL2 17 CTS
D4-3 TX CLOCK Ø2 H — 5 TRC
D4-2 RESET H — 18 MR
10 DAR
D4-2 THRL Ø2 L — 19 THRL
D4-2 TR8 H — 38 TR8
D4-2 TR7 H — 36 TR7
D4-2 TR6 H — 34 TR6
D4-2 TR5 H — 32 TR5
D4-2 TR4 H — 30 TR4
D4-2 TR3 H — 28 TR3
D4-2 TR2 H — 26 TR2
D4-2 TR1 H — 24 TR1
D4-2 STROBE Ø2 L — 20 FHRL
D4-1 SYNC Ø8 — 37 FR8
D4-1 SYNC Ø7 — 35 FR7
D4-1 SYNC Ø6 — 33 FR6
D4-1 SYNC Ø5 — 31 FR5
D4-1 SYNC Ø4 — 29 FR4
D4-1 SYNC Ø3 — 27 FR3
D4-1 SYNC Ø2 — 25 FR2
D4-1 SYNC Ø1 — 23 FR1
4 CRL
22 CD
D4-1 PI — 3 PI
D4-1 EPE — 2 EPE
D4-1 WLS1 — 39 WLS1
D4-1 WLS2 — 40 WLS2
6 CS1
7 CS2
8 MS1
9 MS2
TRO — 15
TCO — 11 EJ2 — TCO Ø2 H
DD/EOC — 13 EK2 — EOC Ø2 H
DA — 12 — D4-5 DA Ø2 H
THRE — 14 — D4-5 TRAN FLAG Ø2 H

SAT Ø3 E55 — +5V -12V — VSS VGG VDD
D4-8 TMARK Ø3 L — EE2 17 CTS
D4-3 TX CLOCK Ø3 H — 5 TRC
D4-2 RESET H — 18 MR
10 DAR
D4-2 THRL Ø3 L — 19 THRL
D4-2 TR8 H — 38 TR8
D4-2 TR7 H — 36 TR7
D4-2 TR6 H — 34 TR6
D4-2 TR5 H — 32 TR5
D4-2 TR4 H — 30 TR4
D4-2 TR3 H — 28 TR3
D4-2 TR2 H — 26 TR2
D4-2 TR1 H — 24 TR1
D4-2 STROBE Ø3 L — 20 FHRL
D4-1 SYNC Ø8 — 37 FR8
D4-1 SYNC Ø7 — 35 FR7
D4-1 SYNC Ø6 — 33 FR6
D4-1 SYNC Ø5 — 31 FR5
D4-1 SYNC Ø4 — 29 FR4
D4-1 SYNC Ø3 — 27 FR3
D4-1 SYNC Ø2 — 25 FR2
D4-1 SYNC Ø1 — 23 FR1
4 CRL
22 CD
D4-1 PI — 3 PI
D4-1 EPE — 2 EPE
D4-1 WLS1 — 39 WLS1
D4-1 WLS2 — 40 WLS2
6 CS1
7 CS2
8 MS1
9 MS2
TRO — 15 — 7404 E10 — AH2. — SERIAL OUT Ø3 L
TCO — 11 EDE — TCO Ø3 H
DD/EOC — 13 EFE — EOC Ø3 H
DA — 12 — D4-5 DA Ø3 H
THRE — 14 — D4-5 TRAN FLAG Ø3 H

(TRANSMITTERS Ø2 AND Ø3)

REVISIONS
CHK | CHANGE NO. | REV.

TITLE SYNC MUX LINE CARD. LINES ØØ-Ø3 (Ø4-5)
SIZE D CODE BS NUMBER DV11-Ø-10 REV A
SCALE — SHEET 5 OF 8 DIST.

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D4-3 RX CLOCK ØØ H — DE2 31 — RRC
D4-4 RCV IN ØØ H — BFE 35 — RI
D4-2 RESET H — 32 — MR
+5V -12V — 1 VSS, 16 VGG, 28 VDD
SAR ØØ E50
CLR FLAG ØØ L — BV2
D4-2 BUF RDE ØØ L — 74Ø8 E58 — 24 SFR, 25 DRR
CV2 RESYNC 1 ØØ (Ø) H — D4-2 STROBE ØØ L — MHRL
D4-1 SYNC ØØ — 40 MHR8
D4-1 SYNC Ø7 — 4 MHR7
D4-1 SYNC Ø6 — 38 MHR6
D4-1 SYNC Ø5 — 3 MHR5
D4-1 SYNC Ø4 — 36 MHR4
D4-1 SYNC Ø3 — 17 MHR3
D4-1 SYNC Ø2 — 22 MHR2
D4-1 SYNC Ø1 — 18 MHR1
CRL — 33
CD PI EPE WLS1 WLS2 RMS3 RMS2 RMS1 SS — 19 21 5 23 2 39 37 28
D4-1 PI
D4-1 EPE
D4-1 WLS1
D4-1 WLS2

RR9 7
RR8 8 — D4-6 RR8 ØØ
RR7 9 — D4-6 RR7 ØØ
RR6 10 — D4-6 RR6 ØØ
RR5 11 — D4-6 RR5 ØØ
RR4 12 — D4-6 RR4 ØØ
RR3 13 — D4-6 RR3 ØØ
RR2 14 — D4-6 RR2 ØØ
RR1 15 — D4-6 RR1 ØØ
PE 29 — D4-6 PE ØØ
OE 27 — D4-6 OE ØØ
+5V R47 10K

74123 E14 — AR2 — DR ØØ H
DR 26
+3V
+5V R46 10K
D4-6 MDET ØØ H — MDET 30 — 7408 E18 — AV2 — MDET ØØ H
74123 E14 75NS
R45 10K
D4-1 1 SYNC ØØ — +5V

D4-6 REC FLAG ØØ H
7474 E28 REV FLAG — BV2 — CLR FLAG ØØ L

D4-3 RX CLOCK Ø1 H — DE2 31 — RRC
D4-4 RCV IN Ø1 H — BDI 35 — RI
D4-2 RESET H — 32 — MR
+5V -12V — 1 VSS, 16 VGG, 28 VDD
SAR Ø1 E37
CLR FLAG Ø1 L — BFI
D4-2 BUF RDE Ø1 L — 7408 E18 — 24 SFR, 25 DRR
RESYNC 1 Ø1 (Ø) H — BH2 — D4-2 STROBE Ø1 L — MHRL
D4-1 SYNC ØØ — 40 MHR8
D4-1 SYNC Ø7 — 4 MHR7
D4-1 SYNC Ø6 — 38 MHR6
D4-1 SYNC Ø5 — 3 MHR5
D4-1 SYNC Ø4 — 36 MHR4
D4-1 SYNC Ø3 — 17 MHR3
D4-1 SYNC Ø2 — 22 MHR2
D4-1 SYNC Ø1 — 18 MHR1
CRL — 33
CD PI EPE WLS1 WLS2 RMS3 RMS2 RMS1 SS — 19 21 5 23 2 39 37 28
D4-1 PI
D4-1 EPE
D4-1 WLS1
D4-1 WLS2

RR9 7
RR8 8 — D4-6 RR8 Ø1
RR7 9 — D4-6 RR7 Ø1
RR6 10 — D4-6 RR6 Ø1
RR5 11 — D4-6 RR5 Ø1
RR4 12 — D4-6 RR4 Ø1
RR3 13 — D4-6 RR3 Ø1
RR2 14 — D4-6 RR2 Ø1
RR1 15 — D4-6 RR1 Ø1
PE 29 — D4-6 PE Ø1
OE 27 — D4-6 OE Ø1
+5V R48 10K

74123 E19 — AU2 — DR Ø1 H
DR 26
+3V
D4-6 REC FLAG Ø1 H
+5V R49 10K
D4-6 MDET Ø1 H — MDET 30 — 7408 E35 — BH1 — MDET Ø1 H
74123 E19 75NS
R86 10K
D4-1 1 SYNC Ø1 — +5V
7474 E28 REV FLAG — BFI — CLR FLAG Ø1 L

D4-6 BUF LCR 13 H
D4-2 RESYNC PULSE ØØ L — DL2
+5V R44 1K
D2-3 LCK 13 H — BA1 — 7417 E30 — 8
+3V
7474 E60 SEARCH SYNC
D4-2 STROBE ØØ H
D4-3 RX CLOCK ØØ H — DE2
7417 E30 — DD2 RESYNC 2 ØØ (Ø) H
7408 E35
D4-3 RX CLOCK ØØ L
7474 E60 RESYNC
7474 E28 RESYNC
7411 E39
CV2 RESYNC 1 ØØ (Ø) H
D4-2 RESET A L

D4-2 RESYNC PULSE Ø1 L — DK2
D4-6 BUF LCR 13 H
D4-2 STROBE Ø1 H
7474 E60 SEARCH SYNC
D4-3 RX CLOCK Ø1 L
7474 E32 RESYNC
7417 E30 — CF2 RESYNC 2 Ø1 (Ø) H
7408 E35
7474 E38 RESYNC
7411 E34
BH2 RESYNC 1 Ø1 (Ø) H

(RECEIVERS ØØ AND Ø1, RESYNC)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
SYNC MUX LINE CARD LINES ØØ-03 (D4-6)	D	BS	DVII-Ø-10	A
SCALE —	SHEET 6 OF 8		DIST.	

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+5V -12V
VSS VGG VDD
D4-3 RX CLOCK Ø2 H DS2
D4-5 RCV IN Ø2 H BK2
D4-2 RESET H
SAR Ø2 E46
RRC RI MR SFR DRR MHRL MHR8 MHR7 MHR6 MHR5 MHR4 MHR3 MHR2 MHR1 CRL
RR9 RR8 RR7 RR6 RR5 RR4 RR3 RR2 RR1 PE OE DR
D4-7 RR8 Ø2 … D4-7 RR1 Ø2, D4-7 PE Ø2, D4-7 OE Ø2
D4-2 BUF RDE Ø2 L
CLR FLAG Ø2 L BU2
7408 E29
DN2
D4-2 STROBE Ø2 L
RESYNC 1 Ø2 (Ø) H
D4-1 SYNC Ø8 … D4-1 SYNC Ø1
CDP1 EPE WLS1 WLS2 RMS3 RMS2 RMS1 SS
D4-1 PI
D4-1 EPE
D4-1 WLS1
D4-1 WLS2
R51 10K +5V
74123 E20 75NS
BB1 DR Ø2 H
+3V
7408 E29
D4-7 MDET Ø2 H
R52 10K +5V
MDET
BJ2 MDET Ø2 H
R53 10K +5V
D4-1 1 SYNC Ø2
7474 E27 RCV FLAG
D4-7 REC FLAG Ø2 H
CLR FLAG Ø2 L
D4-2 RESYNC PULSE Ø2 L DJ2
7417 E30
DR2 RESYNC 2 Ø2 (Ø) H
D4-6 BUF LCR 13 H
7474 E56 SEARCH SYNC
D4-2 STROBE Ø2 H
D4-3 RX CLOCK Ø2 L
7474 E51 RESYNC
D4-3 RX CLOCK Ø2 H DS2
DR2
74H11 E54
DN2
RESYNC 1 Ø2 (Ø) H
D4-2 RESET B L

+5V -12V
VSS VGG VDD
D4-3 RX CLOCK Ø3 H CP2
D4-5 RCV IN Ø3 H BK1
D4-2 RESET H
SAR Ø3 E46
RRC RI MR SFR DRR MHRL MHR8 MHR7 MHR6 MHR5 MHR4 MHR3 MHR2 MHR1 CRL
RR9 RR8 RR7 RR6 RR5 RR4 RR3 RR2 RR1 PE OE DR
D4-7 RR8 Ø3 … D4-7 RR1 Ø3, D4-7 PE Ø3, D4-7 OE Ø3
CLR FLAG Ø3 L BV1
D4-2 BUF RDE Ø3 L
RESYNC 1 Ø3 (Ø) H CK2
7408 E31
D4-2 STROBE Ø3 L
D4-7 REC FLAG Ø2 H
CDP1 EPE WLS1 WLS2 RMS3 RMS2 RMS1 SS
D4-1 PI
D4-1 EPE
D4-1 WLS1
D4-1 WLS2
R54 10K +5V
74123 E24 75NS
BL2 DR Ø3 H
+3V
7408 E31
D4-7 REC FLAG Ø3 H
7474 E27 RCV FLAG
BV1
BP2 MDET Ø3 H
D4-7 MDET Ø3 H
MDET
R55 10K +5V
R56 10K +5V
CLR FLAG Ø3 L
D4-1 1 SYNC Ø3
D4-2 RESYNC PULSE Ø3 L DH2
7417 E36
D4-6 BUF LCR 13 H
7474 E56 SEARCH SYNC
D4-2 STROBE Ø3 H
D4-3 RX CLOCK Ø3 H CP2
CK2 RESYNC 2 Ø3 (Ø) H
7408 E31
7474 E58 RESYNC
D4-3 RX CLOCK Ø3 L
74H11 E34
CK2
RESYNC 1 Ø3 (Ø) H

(RECEIVERS Ø2 AND Ø3, RESYNC)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE SYNC MUX LINE CARD LINES Ø0-Ø3 (D4-7)
SIZE D CODE BS NUMBER DVII-Ø-10 REV. A
SCALE SHEET 7 OF 8 DIST.

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D4-7 RR6 Ø3
D4-7 RR6 Ø2
D4-6 RR6 Ø1
D4-6 RR6 ØØ
D4-7 RR5 Ø3
D4-7 RR5 Ø2
D4-6 RR5 Ø1
D4-6 RR5 ØØ
STBI STBØ 74153 DI E42 CI BI AI DØ CØ BØ AØ SI SØ F1 FØ
8881 E74
FR1 RECV DATA Ø5 L
FS1 RECV DATA Ø4 L

D4-7 PE Ø3
D4-7 PE Ø2
D4-6 PE Ø1
D4-6 PE ØØ
D4-7 OE Ø3
D4-7 OE Ø2
D4-6 OE Ø1
D4-6 OE ØØ
STBI STBØ 74153 DI E44 CI BI AI DØ CØ BØ AØ SI SØ F1 FØ
8881 E76
FM1 MASTER PE L
8881 E76
FL1 MASTER OR L

D4-2 SET TMARK Ø3 L
D4-2 SET TMARK Ø2 L
D4-2 SET TMARK Ø1 L
D4-2 SET TMARK ØØ L
D4-2 RESET H
7474 E68 MARK Ø3
7474 E68 MARK Ø2
7474 E68 MARK Ø1
7474 E68 MARK ØØ
EE2 D4-8 TMARK Ø3 L
EL2 D4-8 TMARK Ø2 L
CB2 D4-8 TMARK Ø1 L
CD2 D4-8 TMARK ØØ L

D4-7 RR4 Ø3
D4-7 RR4 Ø2
D4-6 RR4 Ø1
D4-6 RR4 ØØ
D4-7 RR3 Ø3
D4-7 RR3 Ø2
D4-6 RR3 Ø1
D4-6 RR3 ØØ
STBI STBØ 74153 DI E45 CI BI AI DØ CØ BØ AØ SI SØ F1 FØ
8881 E74
FN1 RECV DATA Ø3 L
FP1 RECV DATA Ø2 L

D3-3 CLEAR TMARK L FK2
STBB STBA 74153 E76 DB DA FB3 FB2 FB1 FB0 FA3 FA2 FA1 FA0 SI SØ

D4-2 CARD FLAG SELECT ØØ-Ø3 L DM2

D4-7 RR2 Ø3
D4-7 RR2 Ø2
D4-6 RR2 Ø1
D4-6 RR2 ØØ
D4-7 RR1 Ø3
D4-7 RR1 Ø2
D4-6 RR1 Ø1
D4-6 RR1 ØØ
STBI STBØ 74153 DI E49 CI BI AI DØ CØ BØ AØ SI SØ F1 FØ
8881 E71
FN2 RECV DATA Ø1 L
FP2 RECV DATA ØØ L

D4-7 RR8 Ø3
D4-7 RR8 Ø2
D4-6 RR8 Ø1
D4-6 RR8 ØØ
D4-7 RR7 Ø3
D4-7 RR7 Ø2
D4-6 RR7 Ø1
D4-6 RR7 ØØ
STBI STBØ 74153 DI E36 CI BI AI DØ CØ BØ AØ SI SØ F1 FØ
8881 E76
FH1 RECV DATA Ø7 L
8881 E76
FJ1 RECV DATA Ø6 L

D4-2 BUF MASTER SCAN Ø1 H
D4-2 BUF MASTER SCAN ØØ H
D4-2 DATA ENABLE ØØ-Ø3 H (FK1)

REVISIONS
CHK | CHANGE NO. | REV.

(RECV DATA MUX S AND TMARK DECODER)

TITLE SYNC MUX LINE CARD LINES ØØ-Ø3 (D4-8)
SIZE D CODE BS NUMBER DVII-Ø-10 REV. A
SCALE SHEET 8 OF 8 DIST.

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BERG PINNING CHART

J1	SIGNAL
A	GROUND
B	DCE SCR Ø4
C	GROUND
D	DCE SCR Ø5
E	GROUND
F	DCE SCR Ø6
H	GROUND
J	DCE SCR Ø7
K	GROUND
L	EIA RCV DATA Ø4
M	GROUND
N	EIA RCV DATA Ø5
P	GROUND
R	EIA XMIT DATA Ø4
S	GROUND
T	EIA XMIT DATA Ø5
U	GROUND
V	DTE SCTE Ø4
W	GROUND
X	DTE SCTE Ø5
Y	DTE SCTE Ø6
Z	GROUND
A A	DTE SCTE Ø7
B B	GROUND
C C	EIA XMIT DATA Ø6
D D	GROUND
E E	EIA XMIT DATA Ø7
F F	GROUND
H H	EIA RCV DATA Ø6
J J	GROUND
K K	EIA RCV DATA Ø7
L L	GROUND
M M	DCE SCT Ø7
N N	GROUND
P P	DCE SCT Ø6
R R	GROUND
S S	DCE SCT Ø5
T T	GROUND
U U	DCE SCT Ø4
V V	GROUND

PARAMETER SWITCH SETTINGS

FUNCTION	SWITCH NAME	SW PACK	SW NO	PARAMETER/SETTING			
INTERNAL BAUD RATE				1200 BAUD	2400 BAUD	4800 BAUD	9600 BAUD
	SELECT B	S2	3	ON	OFF	OFF	OFF
	SELECT A	S2	4	ON	OFF	ON	OFF
FULL / HALF DUPLEX				FULL DUPLEX		HALF DUPLEX	
	HDØ7	S2	5	ON		OFF	
	HDØ6	S2	6	ON		OFF	
	HDØ5	S2	7	ON		OFF	
	HDØ4	S2	8	ON		OFF	
PARITY				NO PARITY	ODD PARITY	EVEN PARITY	
	PI	S1	1	OFF	ON	ON	
	EPE	S1	2	OFF	ON	OFF	
CHARACTER LENGTH				8 BITS/CHAR	7 BITS/CHAR	6 BITS/CHAR	5 BITS/CHAR
	WLS1	S1	3	OFF	ON	OFF	ON
	WLS2	S1	4	OFF	OFF	ON	ON
SYNC REQUIREMENT				1 SYNC REQUIREMENT		2 SYNC REQUIREMENT	
	1 SYNC Ø4	S1	5	OFF		ON	
	1 SYNC Ø5	S1	6	OFF		ON	
	1 SYNC Ø6	S1	7	OFF		ON	
	1 SYNC Ø7	S1	8	OFF		ON	
SYNC SELECT				ONE		ZERO	
LCR10=Ø	SYNC A	S4	1↕8	OFF		ON	
LCR10=1	SYNC B	S3	1↕8	OFF		ON	

PARAMETER SELECTION

FUNCTION	PARAMETER	SELECTED
TRANSMITTER CLK RATE		1X BIT RATE
	CS1 CS2	GROUND GROUND
TRANSMITTER MODE SEL		SYNCHRONOUS
	MS1 MS2	GROUND NO CONNECTION
RECEIVER MODE SEL		SYNCHRONOUS
	RMS1 RMS2 RMS3	NO CONNECTION NO CONNECTION NO CONNECTION

S2

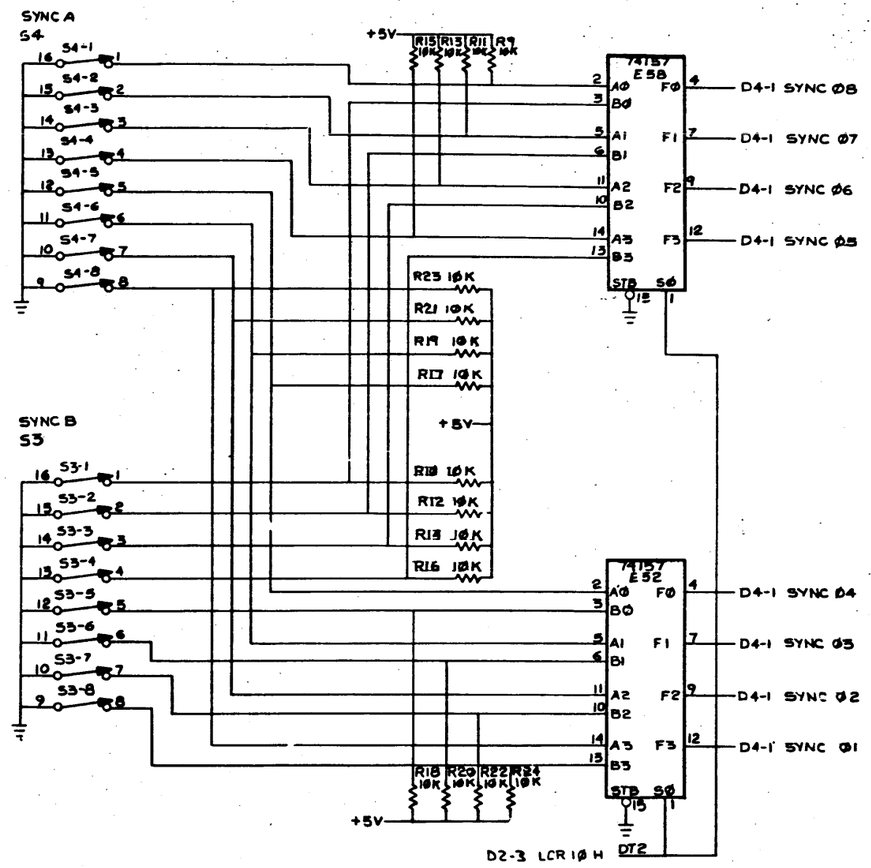
S2-1 16 — 1
S2-2 15 — 2 } UNUSED
S2-3 14 — 3 D4-1 SELECT B
S2-4 13 — 4 D4-1 SELECT A
S2-5 12 — 5 D4-1 HD Ø7
S2-6 11 — 6 D4-1 HD Ø6
S2-7 10 — 7 D4-1 HD Ø5
S2-8 9 — 8 D4-1 HD Ø4

S1

S1-1 16 — 1 D4-1 PI
S1-2 15 — 2 D4-1 EPE
S1-3 14 — 3 D4-1 WLS1
S1-4 13 — 4 D4-1 WLS2
S1-5 12 — 5 D4-1 1SYNC Ø4
S1-6 11 — 6 D4-1 1 SYNC Ø5
S1-7 10 — 7 D4-1 1 SYNC Ø6
S1-8 9 — 8 D4-1 1 SYNC Ø7

NOTES:

1. SWITCHES ARE MOUNTED FOR "OFF" TO THE LEFT AND "ON" TO THE RIGHT
2. FOR SYNC A OR SYNC B SELECTION S4-1 AND S3-1 RESPECTIVELY ARE THE MOST SIGNIFICANT BITS
3. PIN BR1 IS AN ASSIGNED BACKPLANE SIGNAL, TRAN DATA Ø8 H. NO M7839 CIRCUITRY IS CONNECTED TO IT.
4. PIN BM1 IS AN ASSIGNED BACKPLANE SIGNAL, 230.4KBH. NO M7839 CIRCUITRY IS CONNECTED TO IT.



(CHARTS SWITCHES AND SYNC SELECTOR)

REVISIONS		
CHK	CHANGE NO.	REV.
DC	DVII-00006	A
B Chisson 20 July 77		
J. MCNAMARA		

DRN	4/6/77	FIRST USED ON DVII
CHK	4/6/77	digital
ENG.		TITLE SYNC MUX LINE CARD LINES Ø4 - Ø7
PROJ. ENG.	4-17-77	
PROD.	4-17-77	
NEXT HIGHER ASSY.		(Ø4-11)
8-00-DVII-Ø		SIZE D CODE BS NUMBER DVII-Ø-11 REV. A
SCALE		
SHEET 1 OF 8		DIST.

DVII-Ø-11 A

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D4-2 CARD PARAMETER SELECT Ø4-Ø7 L DW2

D3-8 SRS Ø3 L BS2
D3-8 SRS Ø2 H BE2
7400 E23

D2-3 CONTROL STROBE H CS2
7404 E41
D4-2 BUF CONTROL STROBE L

D3-7 INIT DI L EN2
7437 E63
D4-2 RESET H
D4-2 RESET A L
D4-2 RESET B L
+3V

D4-2 STROBE Ø7 L
D4-2 STROBE Ø7 H
D4-2 STROBE Ø6 L
D4-2 STROBE Ø6 H
D4-2 STROBE Ø5 L
D4-2 STROBE Ø5 H
D4-2 STROBE Ø4 L
D4-2 STROBE Ø4 H
7404 E54

D3-8 SRS Ø1 H BT2
D3-8 SRS ØØ H BM2

D4-5 RCV IN Ø7 H
D4-5 RCV IN Ø6 H
D4-4 RCV IN Ø5 H
D4-4 RCV IN Ø4 H
74153 E22
8881 E67
FP1 BIT WINDOW L
BE2
D4-3 INTR MAINTENANCE Ø4-Ø7 H

D3-4 TRAN DATA Ø8 H ER1 (SEE NOTE 3 ON SHEET 1 OF 8)

D3-4 TRAN DATA Ø7 H EP1
D3-4 TRAN DATA Ø6 H EM2
D3-4 TRAN DATA Ø5 H FR2
D3-4 TRAN DATA Ø4 H FV2
D3-4 TRAN DATA Ø3 H FS2
D3-4 TRAN DATA Ø2 H FV1
D3-4 TRAN DATA Ø1 H FT2
D3-4 TRAN DATA ØØ H FU2
7417 E61 / E76
D4-2 TRB H
D4-2 TRT H
D4-2 TR6 H
D4-2 TR5 H
D4-2 TR4 H
D4-2 TR3 H
D4-2 TR2 H
D4-2 TR1 H

D4-2 CARD FLAG SELECT Ø4-Ø7 L DM2

D3-4 MASTER SCAN D H EU2
D3-4 MASTER SCAN Ø2 H EN2
7437 E63

D3-3 RESYNC PULSE L DF2
7404 E41

D3-3 SET TMARK L CU2
7404 E41

D4-2 RESYNC PULSE Ø7 L
D4-2 RESYNC PULSE Ø6 L
D4-2 RESYNC PULSE Ø5 L
D4-2 RESYNC PULSE Ø4 L
D4-2 SET TMARK Ø7 L
D4-2 SET TMARK Ø6 L
D4-2 SET TMARK Ø5 L
D4-2 SET TMARK Ø4 L
74155 E47

D4-5 DA Ø7 H
D4-5 DA Ø6 H
D4-4 DA Ø5 H
D4-4 DA Ø4 H
D4-7 MDET Ø7 H
D4-7 MDET Ø6 H
D4-6 MDET Ø5 H
D4-6 MDET Ø4 H
74153 E62
8881 E67
FC1 DATA NOT AVAILABLE L
FE1 MATCH DETECT L

D1-5 RECEIVED DATA ENABLE H CN2
74HTT E39
FX1 D4-2 DATA ENABLE Ø4-Ø7 H

+5V
R25 10K
C96 68pf
74123 E75
FU1 RDE Ø4-Ø7 H
300NS

D4-2 BUF RDE Ø7 L
D4-2 BUF RDE Ø6 L
D4-2 BUF RDE Ø5 L
D4-2 BUF RDE Ø4 L
D4-2 THRL Ø7 L
D4-2 THRL Ø6 L
D4-2 THRL Ø5 L
D4-2 THRL Ø4 L
74155 E57

D3-4 TRANSMITTER STROBE H EH2

D4-5 TRAN FLAG Ø7 H
D4-5 TRAN FLAG Ø6 H
D4-4 TRAN FLAG Ø5 H
D4-4 TRAN FLAG Ø4 H
D4-7 REC FLAG Ø7 H
D4-7 REC FLAG Ø6 H
D4-6 REC FLAG Ø5 H
D4-6 REC FLAG Ø4 H
74153 E48
8881 E71
FL2 TRAN FLAG WAITING L
FM2 RECEIVER FLAG L

+5V
R26 1K
D3-4 MASTER SCAN Ø1 H EM1 V3
7417 E61

+5V
R27 1K
D3-4 MASTER SCAN ØØ H EN1
7417 E61

D4-2 BUF MASTER SCAN Ø1 H
D4-2 BUF MASTER SCAN ØØ H
D3-4 MASTER SCAN T/R CE2
7404 E41

(CARD SELECTION, INIT AND TRAN DATA)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
SYNC MUX LINE CARD LINES Ø4-Ø7 (D4-2)	D	BS	DVII-Ø-11	A
SCALE	SHEET 2 OF 8	DIST.		

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NOTE 1) A JUMPER WIRE MAY BE SOLDERED ACROSS THE RESISTOR IF THE CUSTOMER SO REQUESTS. HOWEVER, ALL M7839 MODULES WILL BE SHIPPED WITH THE RESISTOR NOT JUMPERED TO INSURE PROPER OPERATION WITH BELL SYSTEM 201A AND 201B MODEMS.

D4-8 TMARK Ø4 L — CD2 — R28 10K +5V — D4-1 HD Ø4

D4-8 TMARK Ø6 L — EL2 — R33 10K +5V — D4-1 HD Ø6

DCE SCR Ø4 — J1 B — 1489 E5 — C81 470 pf — 7432 E4 — 74H11 E25 — D4-3 RX CLOCK Ø4 L — 7404 E41 — DE2 — D4-3 RX CLOCK Ø4 H

DCE SCR Ø6 — J1 F — 1489 E5 — C83 470 pf — 7432 E4 — 74H11 E39 — D4-3 RX CLOCK Ø6 L — 7404 E54 — DS2 — D4-3 RX CLOCK Ø6 H

DCE SCR Ø5 — J1 D — 1489 E5 — C82 470 pf — 7432 E4 — 74H11 E25 — D4-3 RX CLOCK Ø5 L — 7404 E54 — CE2 — D4-3 RX CLOCK Ø5 H

D4-8 TMARK Ø5 L — CB2 — R29 10K +5V — D4-1 HD Ø5

DCE SCR Ø7 — J1 J — 1489 E5 — C84 470 pf — 7432 E4 — 74H11 E25 — D4-3 RX CLOCK Ø7 L — 7404 E41 — CP2 — D4-3 RX CLOCK Ø7 H

D4-8 TMARK Ø7 L — EE2 — R34 10K +5V — D4-1 HD Ø7

DCE SCT Ø4 — J1 U — 1489 E16 — C92 470 pf — 7432 E15 — 7408 E21 — D4-3 TX CLOCK Ø4 H

DCE SCT Ø5 — SS — 1489 E16 — C91 470 pf — 7432 E15 — 7408 E21 — D4-3 TX CLOCK Ø5 H

DCE SCT Ø6 — PP — 1489 E16 — C90 470 pf — 7432 E15 — 7408 E21 — D4-3 TX CLOCK Ø6 H

DCE SCT Ø7 — MM — 1489 E16 — C89 470 pf — 7432 E15 — 7408 E21 — D4-3 TX CLOCK Ø7 H

D3-5 9600 BAUD
D3-5 4800 BAUD
D3-5 2400 BAUD
D3-5 1200 BAUD

74153 E68 — STB1 STB0 — D1 C1 B1 A1 — D0 C0 B0 A0 — S1 S0 — FF2 FE2 FD2 FD1 — F1 F0 — ES2 — D4-3 MUX CLOCK Ø4-Ø7 H

R31 10K +5V — R32 10K — D4-1 SELECT B — D4-1 SELECT A

BAUD RATE	TIME FOR ONE CYCLE (IN MICROSECONDS)
9600	104
4800	208
2400	417
1200	833

D2-3 MAINTENANCE CLK PULSE H — ET2 — 7450 E64 — BJ1 — SOURCE CLOCK A Ø4-Ø7 L

D4-3 MUX CLOCK Ø4-Ø7 H (ES2) — D2-3 MAINTENANCE CLK PULSE H (ET2) — 7450 E64 — BN2 — SOURCE CLOCK B Ø4-Ø7 L

D4-4 MODE Ø0 (1) H — 7417 E61 — D4-4 MODE Ø1 (1) H — 7408 E13 — M42 — SYSTEM MODE Ø4-Ø7 H

R30 1K +5V — D4-4 MODE Ø1 (Ø) H — 7408 E13 — BE2 — D4-3 INTK MAINTENANCE Ø4-Ø7 H

J1 — R37 7.5K — SEE NOTE 1 — 1488 E26 — V — DTE SCTE Ø4

R36 7.5K — SEE NOTE 1 — X — DTE SCTE Ø5

R35 7.5K — SEE NOTE 1 — Y — DTE SCTE Ø6

R38 7.5K — SEE NOTE 1 — AA — DTE SCTE Ø7

REVISIONS		
CHK	CHANGE NO.	REV.

(CLOCK SOURCE AND SELECTION)

TITLE	SIZE	CODE	NUMBER	REV.
SYNC MUX LINE CARD LINES Ø4-Ø7 (D4-3)	D	BS	DV11-Ø-11	A
SCALE	SHEET 3 OF 8	DIST.		

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J1 EIA REC DATA Ø4

D2-3 LCR 14 H — AL2 13
D2-3 LCR 12 H — AM2 12
D2-3 LCR 11 H — AN2 5
D2-3 LCR Ø3 H — AP2 4

74175 E7: D3 MAINT DATA R3(1) 16 / R3(0) 14; D2 MODE Ø1 R2(1) 15 / R2(0) 11; D1 R1(1) 7 / R1(0) 6; D0 TRAN DISABLE R0(1) 2 / R0(0) 3; CLR 1; CLK 9

D4-3 INTR MAINTENANCE Ø4-Ø7H — BE2
D4-4 MODE Ø1(1) H
D4-4 MODE Ø1(Ø) H
D4-4 TRANS DISABLE Ø4-Ø7 H — AF2

D4-2 RESET A L
D4-2 CARD PARAMETER SELECT Ø4-Ø7 L — DU2 5
D4-2 BUF CONTROL STROBE L — 6
7402 E12 → 4

7400 E8 → 7400 E17 → 3 BPC D4-4 RCV IN Ø4 H
7400 E8 → 7400 E17 → 6 BCI D4-4 INTR RCV DATA Ø4-Ø7 L

D4-4 MODE Ø0 (Ø) H
D4-4 MODE Ø0 (1) H
7400 E8 → 7400 E17 → 8 BDI D4-4 RCV IN Ø5 H

EIA REC DATA Ø5 — J1 N — 8T97 E11 → D4-4 MODE Ø0 (Ø) H / D4-4 MODE Ø0 (1) H; C86 470PF

7402 E1 (D4-4 TRANS DISABLE Ø4-Ø7 H AF2) → D4-4 BUF MODE Ø0 (Ø) H

7417 E61 ← +5V R41 1K

7404 E10 ← AB1 SERIAL OUT Ø5 L
D4-4 MODE Ø0 (1) H
7402 E1 → D4-4 BUF MODE Ø0 (Ø) H
8T97 E2 ← +5V R39 1K
1488 E6 → J1 T → EIA XMIT DATA Ø5

AJ2 SERIAL OUT Ø4 L
8T97 E2 ← +5V R40 1K
1488 E6 → J1 R → EIA XMIT DATA Ø4

D4-4 MODE Ø0 (1) H

+5V -12V — VSS 1, VGG 16, VDD 21

SAT Ø4 E73

D4-8 TMARK Ø4 L	CD2 17	CTS
D4-3 TX CLOCK Ø4 H	5	TRC
D4-2 RESET H	18	MR
	10	DAR
D4-2 THRL Ø4 L	19	THRL
D4-2 TR8 H	30	TR8
D4-2 TR7 H	36	TR7
D4-2 TR6 H	34	TR6
D4-2 TR5 H	32	TR5
D4-2 TR4 H	30	TR4
D4-2 TR3 H	28	TR3
D4-2 TR2 H	26	TR2
D4-2 TR1 H	24	TR1
D4-2 STROBE Ø4 L	20	FHRL
D4-1 SYNC Ø8	37	FR8
D4-1 SYNC Ø7	35	FR7
D4-1 SYNC Ø6	33	FR6
D4-1 SYNC Ø5	31	FR5
D4-1 SYNC Ø4	29	FR4
D4-1 SYNC Ø3	27	FR3
D4-1 SYNC Ø2	25	FR2
D4-1 SYNC Ø1	23	FR1
	4	CRL
	22	CD PI EPE WLS1 WLS2 CS1 CS2 MS1 MS2

TRO	15	
TCO	11	FH2 TCO Ø4 H
DD/EOC	13	FJ2 EOC Ø4 H
DA	12	D4-4 DA Ø4 H
THRE	14	D4-4 TRAN FLAG Ø4 H

D4-1 PI — 3
D4-1 EPE — 2
D4-1 WLS1 — 39
D4-1 WLS2 — 40

7404 E10 → 7402 E1 → D4-4 MODE Ø0 (1) H

+5V -12V — VSS 1, VGG 16, VDD 21

SAT Ø5 E66

D4-8 TMARK Ø5 L	CD2 17	CTS
D4-3 TX CLOCK Ø5 H	5	TRC
D4-2 RESET H	18	MR
	10	DAR
D4-2 THRL Ø5 L	19	THRL
D4-2 TR8 H	30	TR8
D4-2 TR7 H	36	TR7
D4-2 TR6 H	34	TR6
D4-2 TR5 H	32	TR5
D4-2 TR4 H	30	TR4
D4-2 TR3 H	28	TR3
D4-2 TR2 H	26	TR2
D4-2 TR1 H	24	TR1
D4-2 STROBE Ø5 L	20	FHRL
D4-1 SYNC Ø8	37	FR8
D4-1 SYNC Ø7	35	FR7
D4-1 SYNC Ø6	33	FR6
D4-1 SYNC Ø5	31	FR5
D4-1 SYNC Ø4	29	FR4
D4-1 SYNC Ø3	27	FR3
D4-1 SYNC Ø2	25	FR2
D4-1 SYNC Ø1	23	FR1
	4	CRL
	22	CD PI EPE WLS1 WLS2 CS1 CS2 MS1 MS2

TRO	15	
TCO	11	EP2 TCO Ø5 H
DD/EOC	13	ER2 EOC Ø5 H
DA	12	D4-4 DA Ø5 H
THRE	14	D4-4 TRAN FLAG Ø5 H

D4-1 PI — 3
D4-1 EPE — 2
D4-1 WLS1 — 39
D4-1 WLS2 — 40

REVISIONS

CHK	CHANGE NO.	REV.

(MODE SELECTION, TRANSMITTERS Ø4 AND Ø5)

TITLE SYNC MUX LINE CARD LINES Ø4 - Ø7 (D4-4)
SIZE D CODE BS NUMBER DV11-Ø-11 REV A
SCALE — SHEET 4 OF 8 DIST.

REV A
DBS DV11-Ø-11

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J1 HH — EIA REC DATA Ø6 — 1489 E11 — C88 47Øpf

D4-4 MODE ØØ (Ø) H
D4-4 MODE ØØ (1) H
7450 E9
7460 E23 — BK2 — D4-5 RCV IN Ø6 H

D4-4 TRANS DISABLE Ø4-Ø7 H (AF2) — 7402 E12

D4-4 INTR RCV DATA Ø4-Ø7 L — BC1

D4-4 BUF MODE ØØ (Ø) H — +5V — R42 1K — 8242 E2 — 1488 E6 — J1 CC — EIA XMIT DATA Ø6

D4-4 MODE ØØ (1) H — 7402 E12 — 7404 E10 — AT2 — SERIAL OUT Ø6 L

J1 KK — EIA REC DATA Ø7 — 1489 E11 — C85 47Øpf

D4-4 MODE ØØ (Ø) H
D4-4 MODE ØØ (1) H
7450 E9
7400 E23 — BK1 — D4-5 RCV IN Ø7 H

7402 E3 — (AF2) D4-4 TRANS DISABLE Ø4-Ø7 H

D4-4 MODE ØØ (1) H — 7402 E3

D4-4 BUF MODE ØØ (Ø) H — +5V — R43 1K — 8242 E2 — 1488 E26 — J1 EE — EIA XMIT DATA Ø7

+5V -12V — VSS VGG VDD

SAT Ø6 E59

D4-8 TMARK Ø6 L EL2 17 CTS
D4-3 TX CLOCK Ø6 H 5 TRC
D4-2 RESET H 18 MR
10 DAR
D4-2 THRL Ø6 L 19 THRL
TRO 15
TCO 11 EJ2 TCO Ø6 H
DD/EOC 13 EK2 EOC Ø6 H
DA 12 D4-5 DA Ø6 H
THRE 14 D4-5 TRAN FLAG Ø6 H
D4-2 TR8 H 38 TR8
D4-2 TR7 H 36 TR7
D4-2 TR6 H 34 TR6
D4-2 TR5 H 32 TR5
D4-2 TR4 H 30 TR4
D4-2 TR3 H 28 TR3
D4-2 TR2 H 26 TR2
D4-2 TR1 H 24 TR1
D4-2 STROBE Ø6 L 20 FHRL
D4-1 SYNC Ø8 37 FR8
D4-1 SYNC Ø7 35 FR7
D4-1 SYNC Ø6 33 FR6
D4-1 SYNC Ø5 31 FR5
D4-1 SYNC Ø4 29 FR4
D4-1 SYNC Ø3 27 FR3
D4-1 SYNC Ø2 25 FR2
D4-1 SYNC Ø1 23 FR1
4 CRL
22 CD PI EPE WLS1 WLS2 CS1 CS2 MS1 MS2 — 3 2 39 40 6 7 8 9
D4-1 PI
D4-1 EPE
D4-1 WLS1
D4-1 WLS2

+5V -12V — VSS VGG VDD

SAT Ø7 E55

D4-8 TMARK Ø7 L EE2 17 CTS
D4-3 TX CLOCK Ø7 H 5 TRC
D4-2 RESET H 18 MR
10 DAR
D4-2 THRL Ø7 L 19 THRL
TRO 15 — 7404 E10 — AH2 — SERIAL OUT Ø7 L
TCO 11 ED2 TCO Ø7 H
DD/EOC 13 EF2 EOC Ø7 H
DA 12 D4-5 DA Ø7 H
THRE 14 D4-5 TRAN FLAG Ø7 H
D4-2 TR8 H 38 TR8
D4-2 TR7 H 36 TR7
D4-2 TR6 H 34 TR6
D4-2 TR5 H 32 TR5
D4-2 TR4 H 30 TR4
D4-2 TR3 H 28 TR3
D4-2 TR2 H 26 TR2
D4-2 TR1 H 24 TR1
D4-2 STROBE Ø7 L 20 FHRL
D4-1 SYNC Ø8 37 FR8
D4-1 SYNC Ø7 35 FR7
D4-1 SYNC Ø6 33 FR6
D4-1 SYNC Ø5 31 FR5
D4-1 SYNC Ø4 29 FR4
D4-1 SYNC Ø3 27 FR3
D4-1 SYNC Ø2 25 FR2
D4-1 SYNC Ø1 23 FR1
4 CRL
22 CD PI EPE WLS1 WLS2 CS1 CS2 MS1 MS2 — 3 2 39 40 6 7 8 9
D4-1 PI
D4-1 EPE
D4-1 WLS1
D4-1 WLS2

REVISIONS | CHK | CHANGE NO. | REV.

(TRANSMITTERS Ø6 AND Ø7)

TITLE SYNC MUX LINE CARD LINES Ø4-Ø7 (D4-5)
SIZE D | CODE BS | NUMBER DVII-Ø-11 | REV. A
SCALE | SHEET 5 OF 8 | DIST.

DVII-Ø-11 A

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+5V -12V
1 VSS 16 VGG 20 VDD

D4-3 RX CLOCK Ø4 H DE2 31 RRC
D4-4 RCV IN Ø4 H BFE 35 RI
D4-2 RESET H 32 MR
SAR Ø4 E50

CLR FLAG Ø4 L BV2
D4-2 BUF RDE Ø4 L
74ØB E58
CV2 RESYNC 1 Ø: (Ø) H
D4-2 STROBE Ø4 L 34 MHRL

D4-1 SYNC Ø8 40 MHR8
D4-1 SYNC Ø7 4 MHR7
D4-1 SYNC Ø6 38 MHR6
D4-1 SYNC Ø5 3 MHR5
D4-1 SYNC Ø4 36 MHR4
D4-1 SYNC Ø3 17 MHR3
D4-1 SYNC Ø2 22 MHR2
D4-1 SYNC Ø1 18 MHR1
33 CRL
6 CD PI EPE WLS1 WLS2 RMS3 RMS2 RMS1 SS
19 21 5 23 2 39 37 28
D4-1 PI
D4-1 EPE
D4-1 WLS1
D4-1 WLS2

RR9 7
RR8 8 D4-6 RR8 Ø4
RR7 9 D4-6 RR7 Ø4
RR6 10 D4-6 RR6 Ø4
RR5 11 D4-6 RR5 Ø4
RR4 12 D4-6 RR4 Ø4
RR3 13 D4-6 RR3 Ø4
RR2 14 D4-6 RR2 Ø4
RR1 15 D4-6 RR1 Ø4
PE 29 D4-6 PE Ø4
OE 27 D4-6 OE Ø4
DR 26

+5V R47 10K
74123 E14 75NS
AR2 DR Ø4 H
+3V
74Ø8 E18
D4-6 REC FLAG Ø4 H
7474 E28 RCV FLAG
BV2 CLR FLAG Ø4 L /3

+5V R46 10K
D4-6 MDET Ø4 H
MDET 30 74Ø8 E18
74123 E19 75NS
AV2 MDET Ø4 H
R45 10K +5V
D4-1 1 SYNC Ø4

D4-6 BUF LCR 13 H
D4-2 RESYNC PULSE Ø4 L DL2
+5V R44 1K
D2-3 LCR 13 H BA1 7417 E36
+3V
D4-2 STROBE Ø4 H
7474 E60 SEARCH SYNC
D4-3 RX CLOCK Ø4 H DE2
74Ø8 E35
D4-3 RX CLOCK Ø4 L
7474 E60 RESYNC
7474 E60 RESYNC
CV2 RESYNC 1 Ø4 (Ø) H
7417 E30
DD2 RESYNC 2 Ø4 (Ø) H
74111 E39
D4-2 RESET A L

+5V -12V
1 VSS 16 VGG 20 VDD

D4-3 RX CLOCK Ø5 H CE2 31 RRC
D4-4 RCV IN Ø5 H BDI 35 RI
D4-2 RESET H 32 MR
SAR Ø5 E37

CLR FLAG Ø5 L BF1
D4-2 BUF RDE Ø5 L
74ØB E18
RESYNC 1 Ø5 (Ø) H BH2
D4-2 STROBE Ø5 L 34 MHRL

D4-1 SYNC Ø8 40 MHR8
D4-1 SYNC Ø7 4 MHR7
D4-1 SYNC Ø6 38 MHR6
D4-1 SYNC Ø5 3 MHR5
D4-1 SYNC Ø4 36 MHR4
D4-1 SYNC Ø3 17 MHR3
D4-1 SYNC Ø2 22 MHR2
D4-1 SYNC Ø1 18 MHR1
33 CRL
6 CD PI EPE WLS1 WLS2 RMS3 RMS2 RMS1 SS
19 21 5 23 2 39 37 28
D4-1 PI
D4-1 EPE
D4-1 WLS1
D4-1 WLS2

RR9 7
RR8 8 D4-6 RR8 Ø5
RR7 9 D4-6 RR7 Ø5
RR6 10 D4-6 RR6 Ø5
RR5 11 D4-6 RR5 Ø5
RR4 12 D4-6 RR4 Ø5
RR3 13 D4-6 RR3 Ø5
RR2 14 D4-6 RR2 Ø5
RR1 15 D4-6 RR1 Ø5
PE 29 D4-6 PE Ø5
OE 27 D4-6 OE Ø5
DR 26

+5V R48 10K
74123 E19 75NS
AU2 DR Ø5 H
+3V
74Ø8 E18
D4-6 REC FLAG Ø5 H
7474 E28 RCV FLAG
BF1 3 CLR FLAG Ø5 L

+5V R49 10K
D4-6 MDET Ø5 H
MDET 30 74Ø8 E35
74123 E19 75NS
BH1 MDET Ø5 H
R86 10K +5V
D4-1 1 SYNC Ø5

D4-2 RESYNC PULSE Ø5 L DK2
+3V
D4-6 BUF LCR 13 H
D4-2 STROBE Ø5 H
7474 E60 SEARCH SYNC
D4-3 RX CLOCK Ø5 H CE2
74Ø8 E35
D4-3 RX CLOCK Ø5 L
7474 E32 RESYNC
7474 E32 RESYNC
BH2 RESYNC 1 Ø5 (Ø) H
7417 E30
CF2 RESYNC 2 Ø5 (Ø) H
74H11 E34

(RECEIVERS Ø4 AND Ø5, RESYNC)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE SYNC MUX LINE CARD LINES Ø4 - Ø7 (D4-6)		SIZE D	CODE BS	NUMBER DVII-Ø-11
SCALE	SHEET 6 OF 8	DIST.		REV. A

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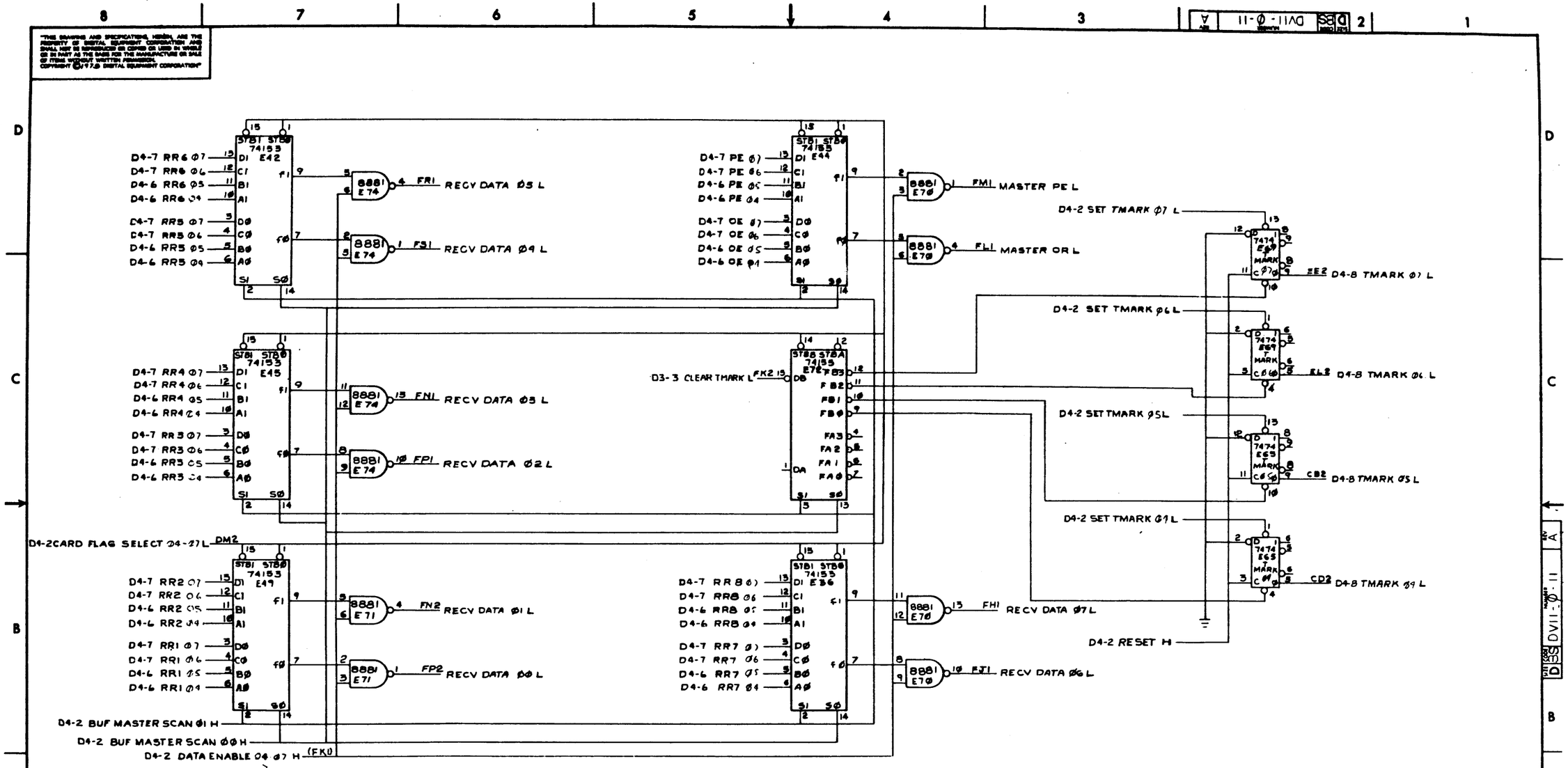

(RECV DATA MUX S AND TMARK DECODER)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
SYNC MUX LINE CARD LINES Ø4 - Ø7 D4-8	D	BS	DV11-Ø-11	A
SCALE	SHEET 8 OF 8	DIST.		

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BERG PINNING CHART

J1	SIGNAL
A	GROUND
B	DCE SCR Ø8
C	GROUND
D	DCE SCR Ø9
E	GROUND
F	DCE SCR 10
H	GROUND
J	DCE SCR 11
K	GROUND
L	EIA RCV DATA Ø8
M	GROUND
N	EIA RCV DATA Ø9
P	GROUND
R	EIA XMIT DATA Ø8
S	GROUND
T	EIA XMIT DATA Ø9
U	GROUND
V	DTE SCTE Ø8
W	GROUND
X	DTE SCTE Ø9
Y	DTE SCTE 10
Z	GROUND
A A	DTE SCTE 11
B B	GROUND
C C	EIA XMIT DATA 10
D D	GROUND
E E	EIA XMIT DATA 11
F F	GROUND
H H	EIA RCV DATA 10
J J	GROUND
K K	EIA RCV DATA 11
L L	GROUND
M M	DCE SCT 11
N N	GROUND
P P	DCE SCT 10
R R	GROUND
S S	DCE SCT Ø9
T T	GROUND
U U	DCE SCT Ø8
V V	GROUND

PARAMETER SWITCH SETTINGS

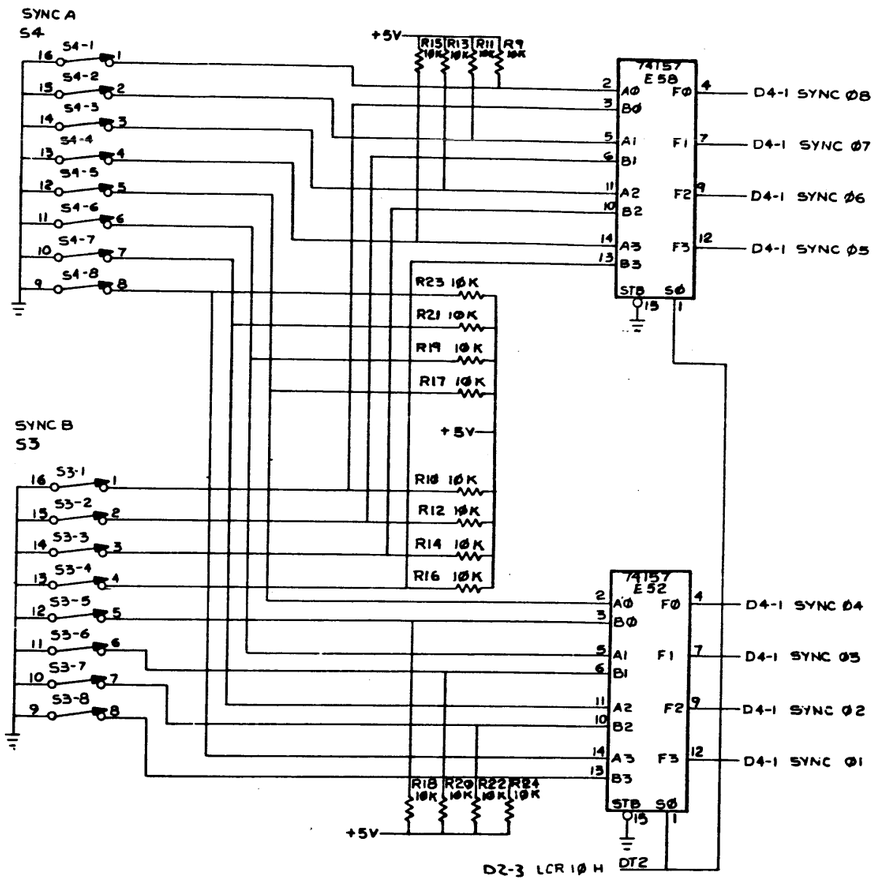
FUNCTION	SWITCH NAME	SW PACK	SW NO	PARAMETER/SETTING			
INTERNAL BAUD RATE				1200 BAUD	2400 BAUD	4800 BAUD	9600 BAUD
	SELECT B	S2	3	ON	ON	OFF	OFF
	SELECT A	S2	4	ON	OFF	ON	OFF
FULL / HALF DUPLEX				FULL DUPLEX		HALF DUPLEX	
	HDX	S2	5	ON		OFF	
	HDØ9	S2	6	ON		OFF	
	HDØ9	S2	7	ON		OFF	
	HDØ8	S2	8	ON		OFF	
PARITY				NO PARITY	ODD PARITY	EVEN PARITY	
	PI	S1	1	OFF	ON	ON	
	EPE	S1	2	OFF	ON	OFF	
CHARACTER LENGTH				8 BITS/CHAR	7 BITS/CHAR	6 BITS/CHAR	5 BITS/CHAR
	WLS1	S1	3	OFF	ON	OFF	ON
	WLS2	S1	4	OFF	OFF	ON	ON
SYNC REQUIREMENT				1 SYNC REQUIREMENT		2 SYNC REQUIREMENT	
	1 SYNC Ø8	S1	5	OFF		ON	
	1 SYNC Ø9	S1	6	OFF		ON	
	1 SYNC 10	S1	7	OFF		ON	
	1 SYNC 11	S1	8	OFF		ON	
SYNC SELECT				ONE		ZERO	
LCR10=Ø	SYNC A	S4	1↔8	OFF		ON	
LCR10=1	SYNC B	S3	1↔8	OFF		ON	

PARAMETER SELECTION

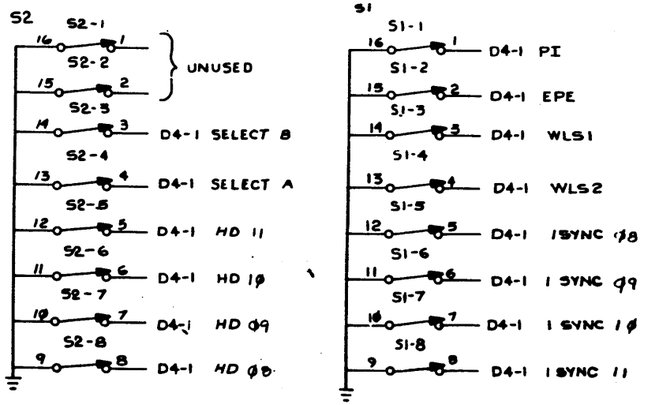
FUNCTION	PARAMETER	SELECTED
TRANSMITTER CLK RATE		1X BIT RATE
	CS1 CS2	GROUND GROUND
TRANSMITTER MODE SEL		SYNCHRONOUS
	MS1 MS2	GROUND NO CONNECTION
RECEIVER MODE SEL		SYNCHRONOUS
	RMS1 RMS2 RMS3	NO CONNECTION NO CONNECTION NO CONNECTION

NOTES:

1. SWITCHES ARE MOUNTED FOR "OFF" TO THE LEFT AND "ON" TO THE RIGHT
2. FOR SYNC A OR SYNC B SELECTION S4-1 AND S3-1 RESPECTIVELY ARE THE MOST SIGNIFICANT BITS
3. PIN ER1 IS AN ASSIGNED BACKPLANE SIGNAL, TRAN DATA Ø8 H. NO M7839 CIRCUITRY IS CONNECTED TO IT.
4. PIN BM1 IS AN ASSIGNED BACKPLANE SIGNAL, 230.4KBH. NO M7839 CIRCUITRY IS CONNECTED TO IT.



D3-5 230.4 KB H BM1
(SEE NOTE 4)



REVISIONS		
CHK	CHANGE NO.	REV.
J U	DVII-00006	A
J MCNAMARA		77

(CHARTS, SWITCHES AND SYNC SELECTOR)

DRW		FIRST USED ON: DVII
CHK		digital
ENG.		TITLE: SYNC MUX LINE CARD LINES Ø8 --11
PROJ. ENG.		
PROD.		
NEXT HIGHER ASSY.	B-DD-DVII-Ø	SIZE: D; CODE: BS; NUMBER: DVII-Ø-12; REV: A
SCALE		
SHEET 1 OF 8		DIST.

DVII-Ø-12 A

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D4-2 CARD PARAMETER SELECT Ø8-11 L DU2

D3-8 SRS Ø3 H BS2 — 7400 E23 — D3-8 SRS Ø2 L BE2

D2-3 CONTROL STROBE H CS2 11 — 7404 E41 — D4-2 BUF CONTROL STROBE L 10

D3-7 INIT DI L EN2 9 — 7437 E63 — D4-2 RESET H

7437 E63 — D4-2 RESET A L

7437 E63 — D4-2 RESET B L

+3V

STB8 STB4 74158 E53 — DB, DA, S1 S0, FB3 FB2 FB1 FB0, FA3 FA2 FA1 FA0

D4-2 STROBE 11 L — 7404 E54 — D4-2 STROBE 11 H

D4-2 STROBE 10 L — 7404 E54 — D4-2 STROBE 10 H

D4-2 STROBE Ø9 L — 7404 E54 — D4-2 STROBE Ø9 H

D4-2 STROBE Ø8 L — 7404 E54 — D4-2 STROBE Ø8 H

D3-8 SES Ø1 H BT2

D3-8 SRS ØØ H BM2

STB1 STB9 74153 E22 — D4-5 RCV IN 11 H, D4-5 RCV IN 10 H, D4-4 RCV IN Ø9 H, D4-4 RCV IN Ø8 H

8881 E67 — FF1 — BIT WINDOW L

BE2 — D4-3 INTR MAINTENANCE Ø8-11 H

D3-4 TRAN DATA Ø8 H ER1 (SEE NOTE 3 ON SHEET 1 OF 8)

D3-4 TRAN DATA Ø7 H EP1 — 7417 E61 — D4-2 TR8 H

D3-4 TRAN DATA Ø6 H EM2 — 7417 E61 — D4-2 TR7 H

D3-4 TRAN DATA Ø5 H FR2 — 7417 E76 — D4-2 TR6 H

D3-4 TRAN DATA Ø4 H FV2 — 7417 E76 — D4-2 TR5 H

D3-4 TRAN DATA Ø3 H FS2 — 7417 E76 — D4-2 TR4 H

D3-4 TRAN DATA Ø2 H FV1 — 7417 E76 — D4-2 TR3 H

D3-4 TRAN DATA Ø1 H FT2 — 7417 E76 — D4-2 TR2 H

D3-4 TRAN DATA ØØ H FU2 — 7417 E76 — D4-2 TR1 H

D4-2 CARD FLAG SELECT Ø8-11 L DM2

D3-4 MASTER SCAN Ø3 H BU2 — 7437 E63 — D3-4 MASTER SCAN C H EN2

7404 E41 — D3-3 RESYNC PULSE L DF2

STB8 STB4 74155 E47 — DB, DA, S1 S0, FB3 FB2 FB1 FB0, FA3 FA2 FA1 FA0

D4-2 RESYNC PULSE 11 L DH2
D4-2 RESYNC PULSE 10 L DJ2
D4-2 RESYNC PULSE Ø9 L DK2
D4-2 RESYNC PULSE Ø8 L DL2

D3-3 SET TMARK L CU2 — 7404 E41

D4-2 SET TMARK 11 L
D4-2 SET TMARK 10 L
D4-2 SET TMARK Ø9 L
D4-2 SET TMARK Ø8 L

STB1 STB9 74153 E62 — D4-5 DA 11 H, D4-5 DA 10 H, D4-4 DA Ø9 H, D4-4 DA Ø8 H, D4-7 MDET 11 H, D4-7 MDET 10 H, D4-6 MDET Ø9 H, D4-6 MDET Ø8 H

8881 E67 — FC1 — DATA NOT AVAILABLE L

8881 E67 — FE1 — MATCH DETECT L

D1-5 RECEIVED DATA ENABLE H CN2 — 74H11 E34 — FK1 — D4-2 DATA ENABLE Ø8-11 H

+5V, R25 10K, C96 68pf, 74123 E75 RDE 3Ø8NS — FU1 — RDE Ø8-11 H, +3V

STB8 STB4 74155 E57 — DB, DA, S1 S0, FB3 FB2 FB1 FB0, FA3 FA2 FA1 FA0

D4-2 BUF RDE 11 L
D4-2 BUF RDE 10 L
D4-2 BUF RDE Ø9 L
D4-2 BUF RDE Ø8 L

D3-4 TRANSMITTER STROBE H EH2

D4-2 THRL 11 L
D4-2 THRL 10 L
D4-2 THRL Ø9 L
D4-2 THRL Ø8 L

STB1 STB9 74153 E48 — D4-5 TRAN FLAG 11 H, D4-5 TRAN FLAG 10 H, D4-4 TRAN FLAG Ø9 H, D4-4 TRAN FLAG Ø8 H, D4-7 REC FLAG 11 H, D4-7 REC FLAG 10 H, D4-6 REC FLAG Ø9 H, D4-6 REC FLAG Ø8 H

8881 E71 — FL2 — TRAN FLAG WAITING L

8881 E71 — FM2 — RECEIVER FLAG L

+5V, R26 1K — D3-4 MASTER SCAN Ø1 H EM1 — 7417 E61

+5V, R27 1K — D3-4 MASTER SCAN ØØ H EN1 — 7417 E61

D4-2 BUF MASTER SCAN Ø1 H

D4-2 BUF MASTER SCAN ØØ H

D3-4 MASTER SCAN T/R CR2 — 7404 E41

(CARD SELECTION, INIT AND TRAN DATA)

REVISIONS

CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
SYNC MUX LINE CARD LINES Ø8-11 (D4-2)	D	BS	DV11-Ø-12	A
SCALE	SHEET 2 OF 8		DIST.	

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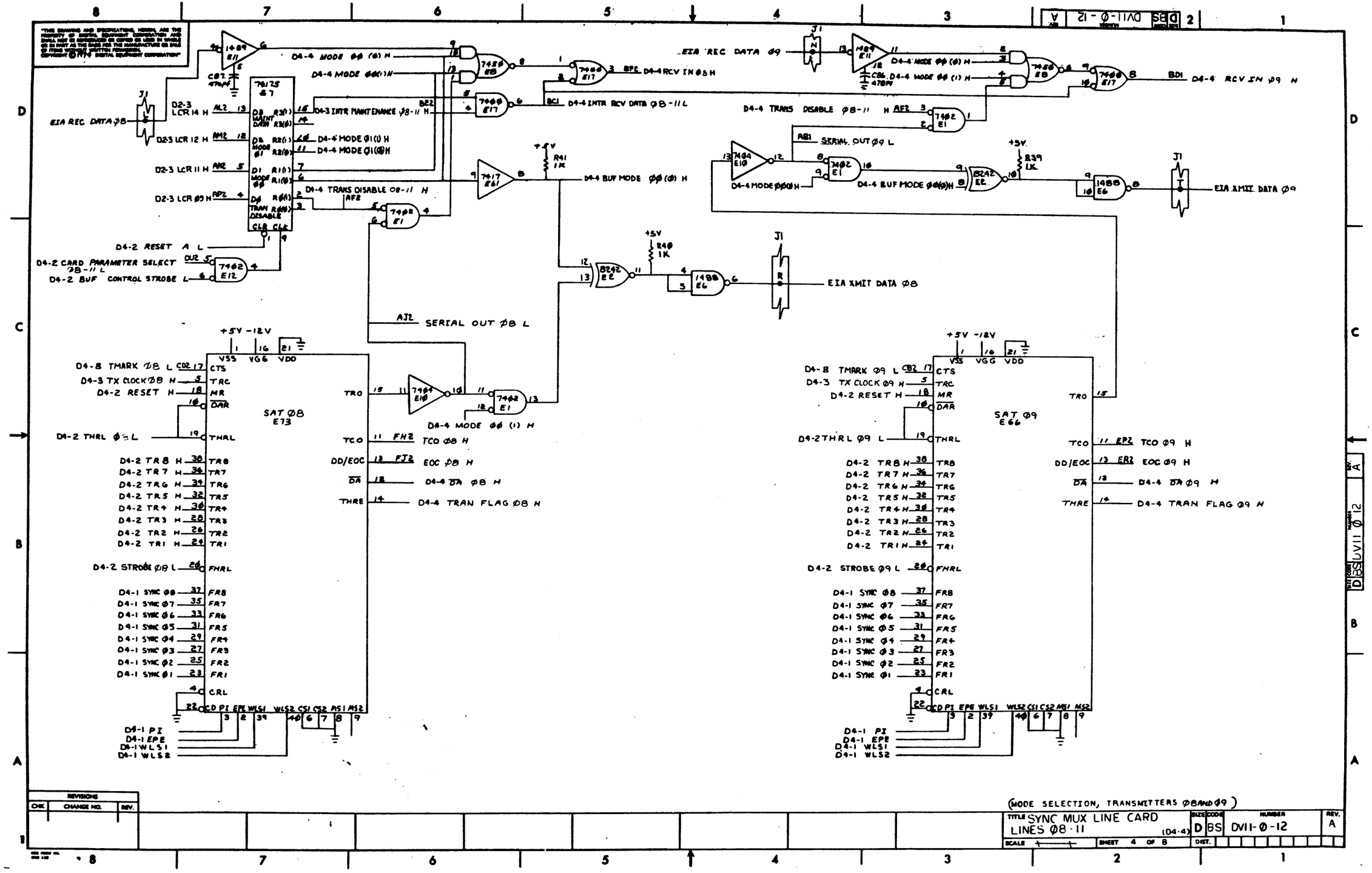
NOTE 1) A JUMPER WIRE MAY BE SOLDERED ACROSS THE RESISTOR IF THE CUSTOMER SO REQUESTS. HOWEVER, ALL M7839 MODULES WILL BE SHIPPED WITH THE RESISTOR NOT JUMPERED TO INSURE PROPER OPERATION WITH BELL SYSTEM 201A AND 201B MODEMS.

BAUD RATE	TIME FOR ONE CYCLE (IN MICROSECONDS)
9600	104
4800	208
2400	417
1200	833

REVISIONS		
CHK	CHANGE NO.	REV.

(CLOCK SOURCE AND SELECTION)

TITLE	SIZE	CODE	NUMBER	REV.
SYNC MUX LINE CARD LINES Ø8-11 (D4-3)	D	BS	DV11-Ø-12	A
SCALE	SHEET 3 OF 8	DIST.		

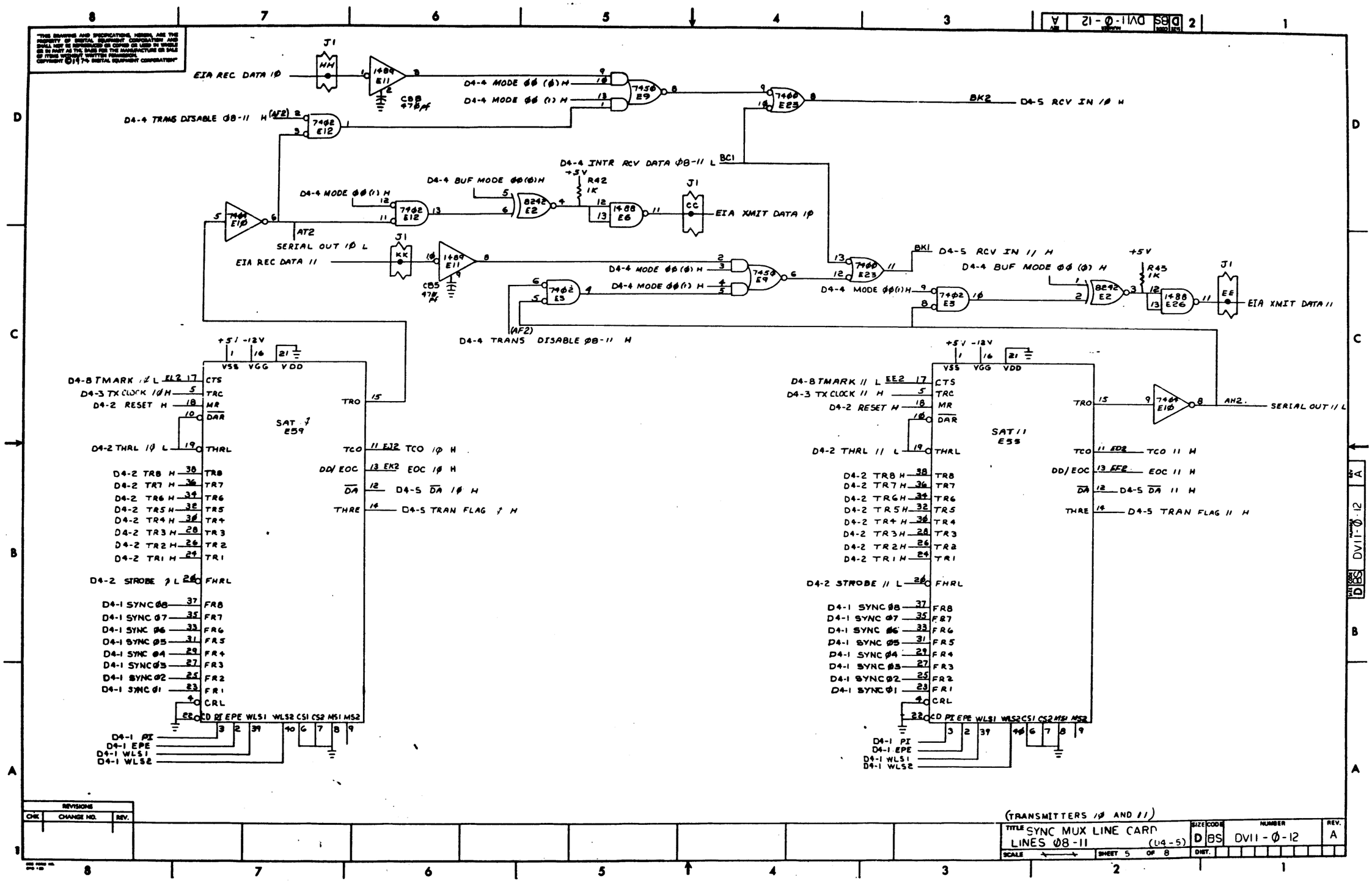


(MODE SELECTION, TRANSMITTERS Ø8 AND Ø9)

TITLE	SIZE	CODE	NUMBER	REV.
SYNC MUX LINE CARD LINES Ø8-11 (D4-4)	D	BS	DV11-Ø-12	A

SCALE — SHEET 4 OF 8 — DIST.

REVISIONS: CHK | CHANGE NO. | REV.


EIA REC DATA 10
D4-4 MODE 00 (0) H
D4-4 MODE 00 (1) H
D4-4 TRANS DISABLE 08-11 H
BK2
D4-5 RCV IN 10 H
D4-4 INTR RCV DATA 08-11 L
BC1
D4-4 BUF MODE 00(0)H
D4-4 MODE 00 (1) H
R42 1K
EIA XMIT DATA 10
AT2
SERIAL OUT 10 L
EIA REC DATA 11
BK1
D4-5 RCV IN 11 H
D4-4 BUF MODE 00 (0) H
R43 1K
EIA XMIT DATA 11
D4-4 MODE 00(1)H
D4-4 TRANS DISABLE 08-11 H
SAT 10 E59
SAT 11 E55
D4-8 TMARK 10 L
D4-3 TX CLOCK 10 H
D4-2 RESET H
D4-2 THRL 10 L
D4-2 TR8 H
D4-2 TR7 H
D4-2 TR6 H
D4-2 TR5 H
D4-2 TR4 H
D4-2 TR3 H
D4-2 TR2 H
D4-2 TR1 H
D4-2 STROBE 10 L
D4-1 SYNC 08
D4-1 SYNC 07
D4-1 SYNC 06
D4-1 SYNC 05
D4-1 SYNC 04
D4-1 SYNC 03
D4-1 SYNC 02
D4-1 SYNC 01
D4-1 PI
D4-1 EPE
D4-1 WLS1
D4-1 WLS2
TCO 10 H
EOC 10 H
D4-5 DA 10 H
D4-5 TRAN FLAG 10 H
D4-8 TMARK 11 L
D4-3 TX CLOCK 11 H
D4-2 THRL 11 L
D4-2 STROBE 11 L
TCO 11 H
EOC 11 H
D4-5 DA 11 H
D4-5 TRAN FLAG 11 H
SERIAL OUT 11 L
(TRANSMITTERS 10 AND 11)
SYNC MUX LINE CARD LINES 08-11 (U4-5)
SIZE D
CODE BS
NUMBER DV11-0-12
REV. A
SHEET 5 OF 8

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+5V -12V 2Ø
VSS VGG VDD

D4-3 RX CLOCK Ø8 H CE2 31 RRC
D4-4 RCV IN Ø8 H BF2 35 RI
D4-2 RESET H 32 MR
SAR Ø8 E5Ø
CLR FLAG Ø8 L BV2
D4-2 BUF RDE Ø8 L
74ØB E5B
SFR 24
DRR 25
CVE
D4-2 STROBE Ø2 L 34 MHRL
RESYNC 1 Ø8 (Ø) H
D4-1 SYNC Ø8 40 MHR8
D4-1 SYNC Ø7 4 MHR7
D4-1 SYNC Ø6 38 MHR6
D4-1 SYNC Ø5 3 MHR5
D4-1 SYNC Ø4 36 MHR4
D4-1 SYNC Ø3 17 MHR3
D4-1 SYNC Ø2 22 MHR2
D4-1 SYNC Ø1 18 MHR1
CRL 33
6
CD PI EPE WLS1 WLS2 RMS3 RMS2 RMS1 SS
19 21 5 23 2 39 37 28
D4-1 PI
D4-1 EPE
D4-1 WLS1
D4-1 WLS2

RR9 7
RR8 8 D4-6 RR8 Ø8
RR7 9 D4-6 RR7 Ø8
RR6 10 D4-6 RR6 Ø8
RR5 11 D4-6 RR5 Ø8
RR4 12 D4-6 RR4 Ø8
RR3 13 D4-6 RR3 Ø8
RR2 14 D4-6 RR2 Ø8
RR1 15 D4-6 RR1 Ø8
PE 29 D4-6 PE Ø8
OE 27 D4-6 OE Ø8
DR 26
+5V R47 10K
74123 E14 75NS
AR2 DR Ø8 H
+3V
MDET 30
D4-6 MDET Ø8 H
74ØB E18
+5V R46 10K
AV2 MDET Ø8 H
CLR FLAG Ø8 L
D4-1 I SYNC Ø8
R45 10K +5V
D4-6 REC FLAG Ø8 H
7474 E28 REV FLAG
BV2

D4-6 BUF LCR 13 H
D4-2 RESYNC PULSE Ø8 L DL2
+5V R44 1K
D2-3 LCR 13 H BAI
7417 E3Ø
+3V
D4-2 STROBE Ø8 H
7474 E6B SEARCH SYNC
D4-3 RX CLOCK Ø8 L
7474 E29 RESYNC
D4-3 RX CLOCK Ø8 H DE2
7411 E39
DD2 RESYNC 2 Ø8 (Ø) H
CV2
RESYNC 1 Ø8 (Ø) H
D4-2 RESET A L

D4-3 RX CLOCK Ø9 H CE2 31 RRC
D4-4 RCV IN Ø9 H BD1 35 RI
D4-2 RESET H 32 MR
SAR Ø9 E37
CLR FLAG Ø9 L BF1
D4-2 BUF RDE Ø9 L
74ØB E1B
RESYNC 1 Ø9 (Ø) H BH2
SFR 24
DRR 25
D4-2 STROBE Ø9 L 34 MHRL
D4-1 SYNC Ø8 40 MHR8
D4-1 SYNC Ø7 4 MHR7
D4-1 SYNC Ø6 38 MHR6
D4-1 SYNC Ø5 3 MHR5
D4-1 SYNC Ø4 36 MHR4
D4-1 SYNC Ø3 17 MHR3
D4-1 SYNC Ø2 22 MHR2
D4-1 SYNC Ø1 18 MHR1
CRL 33
6
CD PI EPE WLS1 WLS2 RMS3 RMS2 RMS1 SS
19 21 5 23 2 39 37 28
D4-1 PI
D4-1 EPE
D4-1 WLS1
D4-1 WLS2

RR9 7
RR8 8 D4-6 RR8 Ø9
RR7 9 D4-6 RR7 Ø9
RR6 10 D4-6 RR6 Ø9
RR5 11 D4-6 RR5 Ø9
RR4 12 D4-6 RR4 Ø9
RR3 13 D4-6 RR3 Ø9
RR2 14 D4-6 RR2 Ø9
RR1 15 D4-6 RR1 Ø9
PE 29 D4-6 PE Ø9
OE 27 D4-6 OE Ø9
DR 26
+5V R48 10K
74123 E19 75NS
AU2 DR Ø9 H
+3V
MDET 30
D4-6 MDET Ø9 H
74ØB E35
+5V R49 10K
BH1 MDET Ø9 H
CLR FLAG Ø9 L
D4-1 I SYNC Ø9
R86 10K +5V
D4-6 REC FLAG Ø9 H
7474 E88 RCV FLAG
BF1

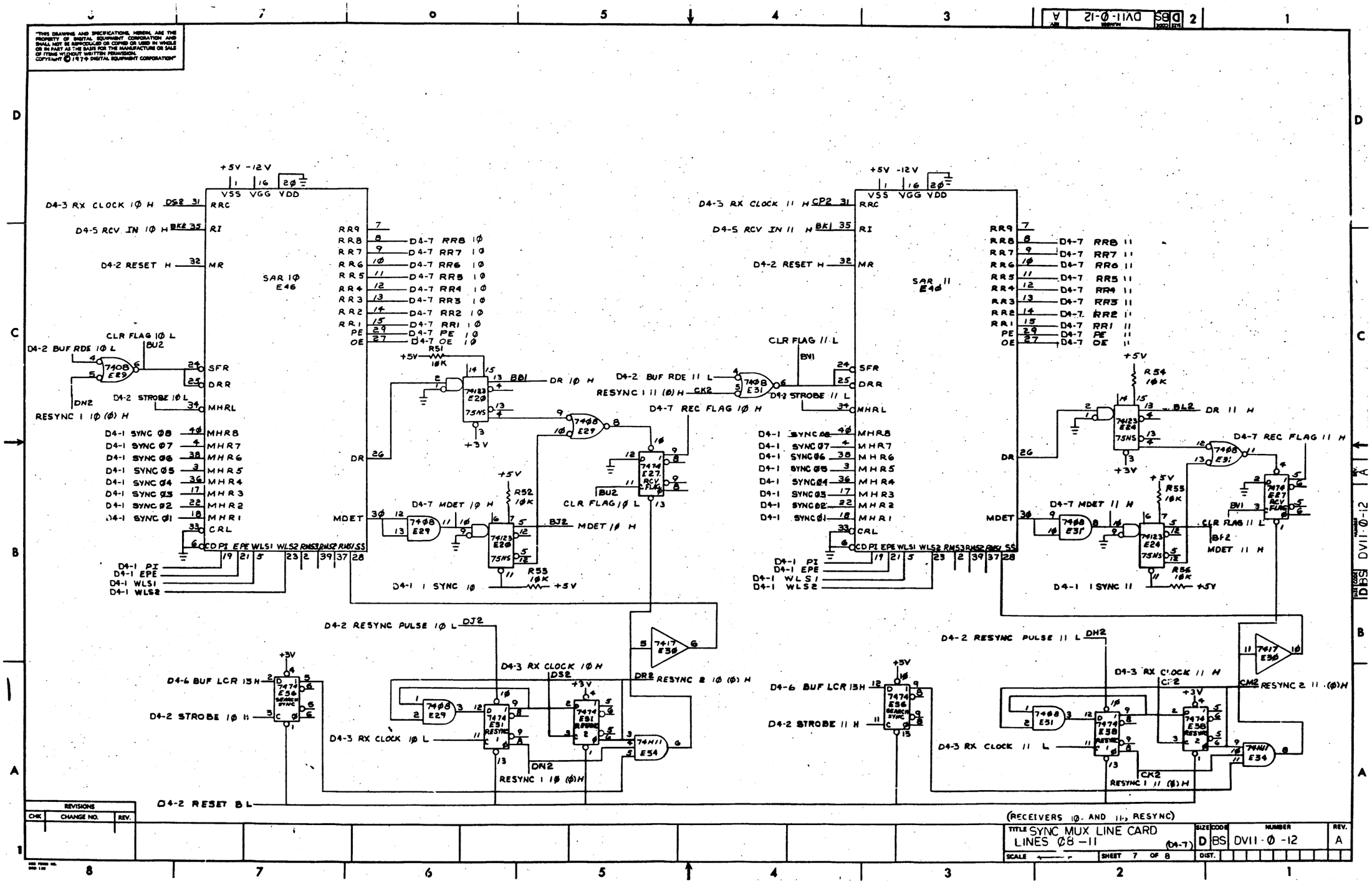
D4-6 BUF LCR 13 H
D4-2 STROBE Ø9 H
7474 E6Ø SEARCH SYNC
D4-2 RESYNC PULSE Ø9 L DK2
7417 E3Ø
CF2 RESYNC 2 Ø9 (Ø) H
D4-3 RX CLOCK Ø9 H CE2
+3V
74ØB E35
7474 E32 RESYNC
D4-3 RX CLOCK Ø9 L
7411 E34
BH2
RESYNC 1 Ø9 (Ø) H

(RECEIVERS Ø8 AND Ø9, RESYNC)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SYNC MUX LINE CARD LINES Ø8 12 (D4-6)			
SIZE	CODE	NUMBER	REV.	
D	BS	DV11-Ø-12	A	
SCALE		SHEET 6 OF 8	DWT	

A DBS DV11-Ø-12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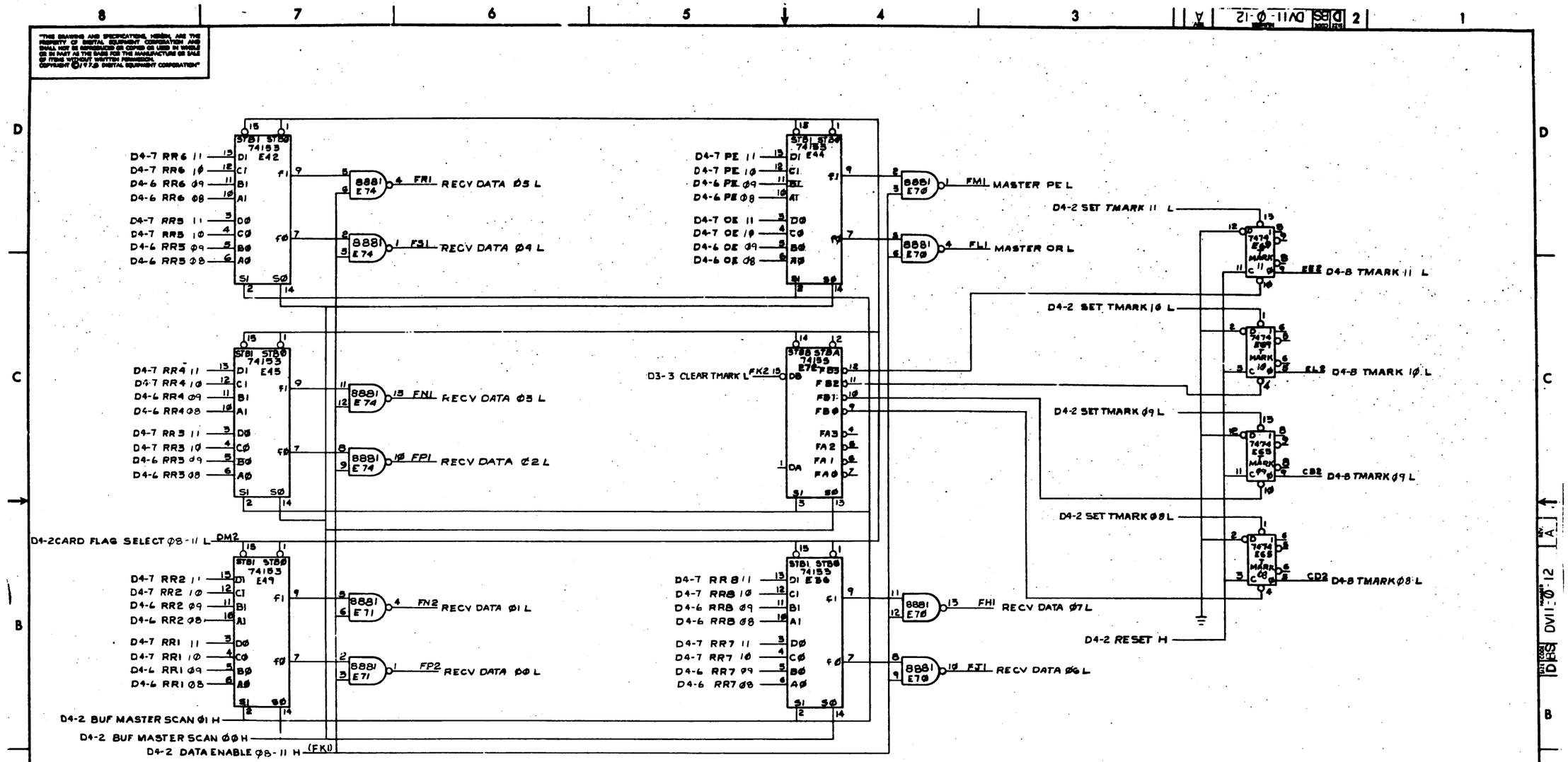
SAR 10 E46
SAR 11 E40
D4-3 RX CLOCK 10 H
D4-5 RCV IN 10 H
D4-2 RESET H
D4-2 BUF RDE 10 L
CLR FLAG 10 L
D4-2 STROBE 10 L
RESYNC 1 10 (0) H
D4-1 SYNC 08
D4-1 SYNC 07
D4-1 SYNC 06
D4-1 SYNC 05
D4-1 SYNC 04
D4-1 SYNC 03
D4-1 SYNC 02
D4-1 SYNC 01
D4-1 PI
D4-1 EPE
D4-1 WLS1
D4-1 WLS2
D4-7 RR8 10
D4-7 RR7 10
D4-7 RR6 10
D4-7 RR5 10
D4-7 RR4 10
D4-7 RR3 10
D4-7 RR2 10
D4-7 RR1 10
D4-7 PE 10
D4-7 OE 10
DR 10 H
D4-7 REC FLAG 10 H
D4-7 MDET 10 H
MDET 10 H
D4-1 1 SYNC 10
D4-2 RESYNC PULSE 10 L
D4-3 RX CLOCK 10 H
RESYNC 2 10 (0) H
D4-6 BUF LCR 13 H
D4-2 STROBE 10 H
D4-3 RX CLOCK 10 L
RESYNC 1 10 (0) H
D4-2 RESET B L
D4-3 RX CLOCK 11 H
D4-5 RCV IN 11 H
D4-2 RESET H
CLR FLAG 11 L
D4-2 BUF RDE 11 L
RESYNC 1 11 (0) H
D4-2 STROBE 11 L
D4-7 REC FLAG 11 H
D4-7 MDET 11 H
CLR FLAG 11 L
MDET 11 H
D4-1 1 SYNC 11
D4-2 RESYNC PULSE 11 L
D4-3 RX CLOCK 11 H
RESYNC 2 11 (0) H
D4-6 BUF LCR 13 H
D4-2 STROBE 11 H
D4-3 RX CLOCK 11 L
RESYNC 1 11 (0) H
(RECEIVERS 10 AND 11, RESYNC)
TITLE SYNC MUX LINE CARD LINES 08 -11 (D4-7)
SIZE D
CODE BS
NUMBER DV11-0-12
REV. A
SHEET 7 OF 8
REVISIONS
CHK
CHANGE NO.
REV.



(RECV DATA MUX S AND TMARK DECODER)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
SYNC MUX LINE CARD LINES 08-11 (D4-8)	D	BS	DV11-0-12	A
SCALE	SHEET 8 OF 8	DIST.		

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BERG PINNING CHART

J1	SIGNAL
A	GROUND
B	DCE SCR 12
C	GROUND
D	DCE SCR 13
E	GROUND
F	DCE SCR 14
H	GROUND
J	DCE SCR 15
K	GROUND
L	EIA RCV DATA 12
M	GROUND
N	EIA RCV DATA 13
P	GROUND
R	EIA XMIT DATA 12
S	GROUND
T	EIA XMIT DATA 13
U	GROUND
V	DTE SCTE 12
W	GROUND
X	DTE SCTE 13
Y	DTE SCTE 14
Z	GROUND
A A	DTE SCTE 15
B B	GROUND
C C	EIA XMIT DATA 14
D D	GROUND
E E	EIA XMIT DATA 15
F F	GROUND
H H	EIA RCV DATA 14
J J	GROUND
K K	EIA RCV DATA 15
L L	GROUND
M M	DCE SCT 15
N N	GROUND
P P	DCE SCT 14
R R	GROUND
S S	DCE SCT 13
T T	GROUND
U U	DCE SCT 12
V V	GROUND

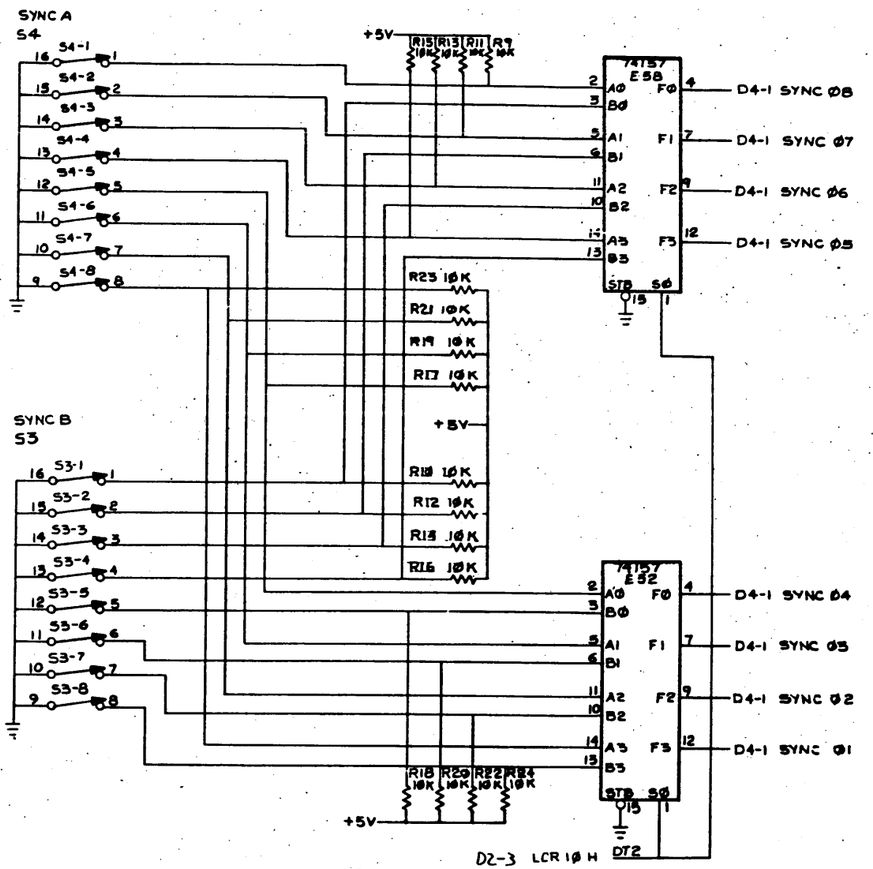
PARAMETER SWITCH SETTINGS

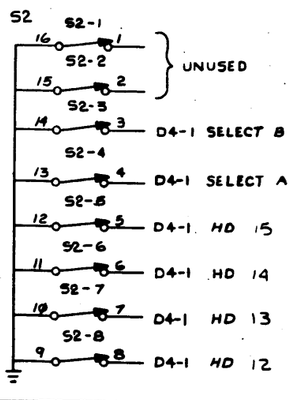
FUNCTION	SWITCH NAME	SW PACK	SW NO	PARAMETER/SETTING			
INTERNAL BAUD RATE				1200 BAUD	2400 BAUD	4800 BAUD	9600 BAUD
	SELECT B	S2	3	ON	ON	OFF	OFF
	SELECT A	S2	4	ON	OFF	ON	OFF
FULL / HALF DUPLEX				FULL DUPLEX		HALF DUPLEX	
	HD 15	S2	5	ON		OFF	
	HD 14	S2	6	ON		OFF	
	HD 13	S2	7	ON		OFF	
	HD 12	S2	8	ON		OFF	
PARITY				NO PARITY	ODD PARITY	EVEN PARITY	
	PI	S1	1	OFF	ON	ON	
	EPE	S1	2	OFF	ON	OFF	
CHARACTER LENGTH				5 BITS/CHAR	7 BITS/CHAR	6 BITS/CHAR	8 BITS/CHAR
	WLS1	S1	3	OFF	ON	OFF	ON
	WLS2	S1	4	OFF	OFF	ON	ON
SYNC REQUIREMENT				1 SYNC REQUIREMENT		2 SYNC REQUIREMENT	
	1 SYNC 12	S1	5	OFF		ON	
	1 SYNC 13	S1	6	OFF		ON	
	1 SYNC 14	S1	7	OFF		ON	
	1 SYNC 15	S1	8	OFF		ON	
SYNC SELECT				ONE		ZERO	
LCR10=0	SYNC A	S4	1 2 3 4 5 6 7 8	OFF		ON	
LCR10=1	SYNC B	S3	1 2 3 4 5 6 7 8	OFF		ON	

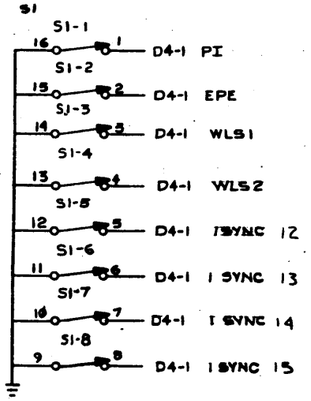
PARAMETER SELECTION

FUNCTION	PARAMETER	SELECTED
TRANSMITTER CLK RATE		1X BIT RATE
	CS1	GROUND
	CS2	GROUND
TRANSMITTER MODE SEL		SYNCHRONOUS
	MS1	GROUND
	MS2	NO CONNECTION
RECEIVER MODE SEL		SYNCHRONOUS
	RMS1	NO CONNECTION
	RMS2	NO CONNECTION
	RMS3	NO CONNECTION

NOTES:
1. SWITCHES ARE MOUNTED FOR "OFF" TO THE LEFT AND "ON" TO THE RIGHT
2. FOR SYNC A OR SYNC B SELECTION S4-1 AND S3-1 RESPECTIVELY ARE THE MOST SIGNIFICANT BITS
3. PIN ER1 IS AN ASSIGNED BACKPLANE SIGNAL, TRAN DATA 08 H. NO M7839 CIRCUITRY IS CONNECTED TO IT.
4. PIN BM1 IS AN ASSIGNED BACKPLANE SIGNAL, 230.4KBH. NO M7839 CIRCUITRY IS CONNECTED TO IT.





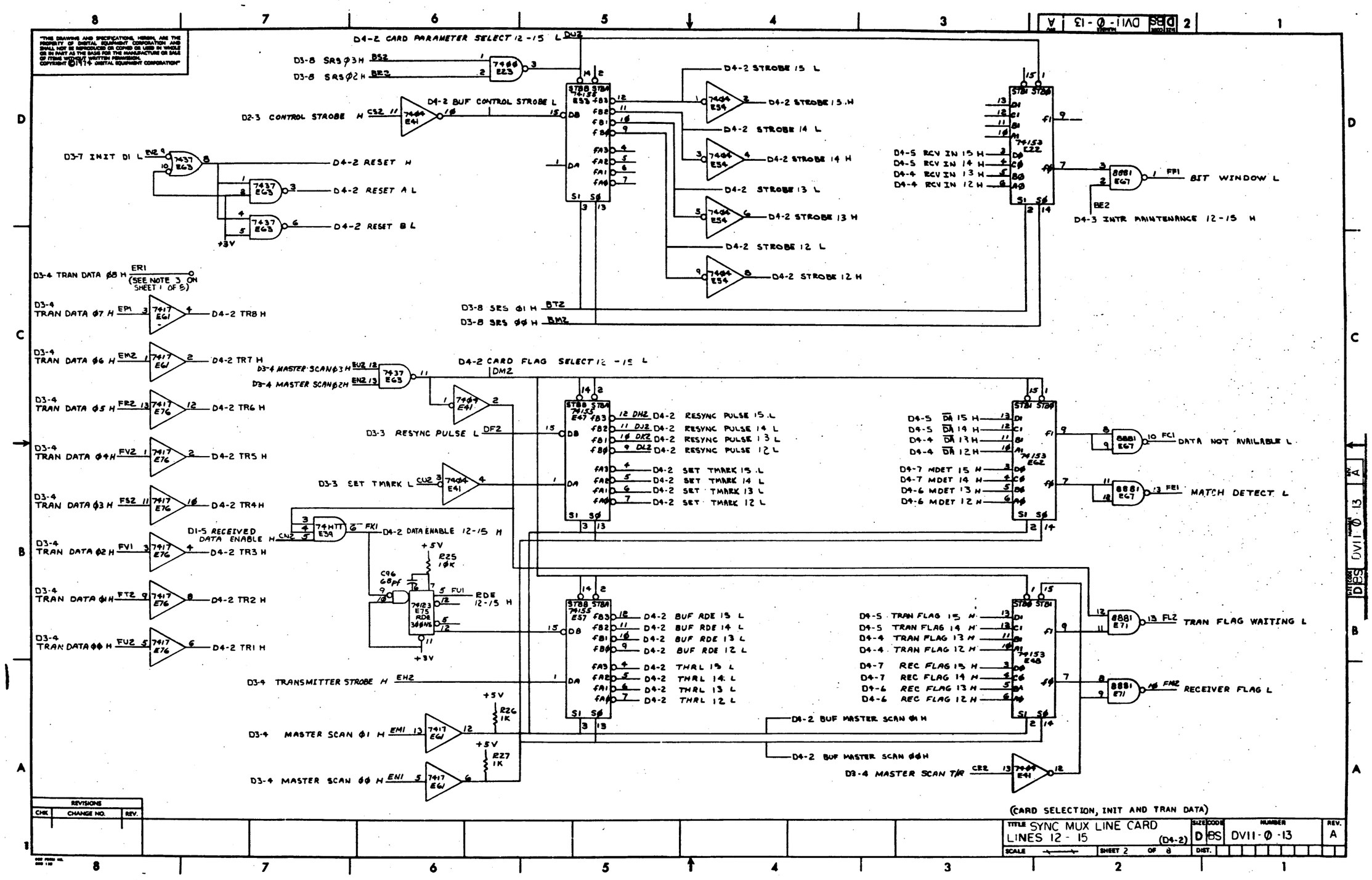


D3-5 230.4 KB H BM1
(SEE NOTE 4)

REVISIONS		
CHK	CHANGE NO.	REV.
	DV11-00006	A
J. Chauvin	20 July 77	
J. MCNAMARA		
	27 July 77	

(CHARTS, SWITCHES, AND SYNC SELECTOR)

DRN		FIRST USED ON: DV11
CHK'D		digital
ENG.		TITLE: SYNC MUX LINE CARD LINES 12 - 15
PROJ. ENG.		(D4-1)
PROD.	4-17-77	
NEXT HIGHER ASSY.		
B DD-DV11-0		SIZE D, CODE BS, NUMBER DV11-0-13, REV. A
SCALE		
SHEET 1 OF 8		DIST.



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REVISIONS		
CHK	CHANGE NO.	REV.

TITLE SYNC MUX LINE CARD LINES 12 - 15 (D4-2)

SIZE D | CODE BS | NUMBER DV11-Ø-13 | REV. A

SCALE | SHEET 2 OF 8 | DIST.

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NOTE: 1) A JUMPER WIRE MAY BE SOLDERED ACROSS THE RESISTOR IF THE CUSTOMER SO REQUESTS. HOWEVER, ALL M7839 MODULES WILL BE SHIPPED WITH THE RESISTOR NOT JUMPERED TO INSURE PROPER OPERATION WITH BELL SYSTEM 201A AND 201B MODEMS.

D4-8 TMARK 12 L — CD2 — R28 10K +5V — D4-1 HD 12
DCE SCR 12 — C81 470 pf — D4-3 RX CLOCK 12 H — DE2
D4-8 TMARK 13 L — CB2 — R29 10K +5V — D4-1 HD 13
DCE SCR 13 — C82 470 pf — D4-3 RX CLOCK 13 H — CE2
D4-8 TMARK 14 L — EL2 — R33 10K +5V — D4-1 HD 14
DCE SCR 14 — C83 470 pf — D4-3 RX CLOCK 14 H — DS2
D4-8 TMARK 15 L — EE2 — R34 10K +5V — D4-1 HD 15
DCE SCR 15 — C84 470 pf — D4-3 RX CLOCK 15 H — CP2

DCE SCT 12 — C92 470 pf — D4-3 TX CLOCK 12 H
DCE SCT 13 — C91 470 pf — D4-3 TX CLOCK 13 H
DCE SCT 14 — C90 470 pf — D4-3 TX CLOCK 14 H
DCE SCT 15 — C89 470 pf — D4-3 TX CLOCK 15 H

D2-3 MAINTENANCE CLK PULSE H — ET2
D4-4 MODE Ø1 (1) H — R30 1K +5V — D4-4 MODE Ø1 (Ø) H — BE2 — D4-3 INTR MAINTENANCE 12-15 H

D3-5 9600 BAUD
D3-5 4800 BAUD
D3-5 2400 BAUD
D3-5 1200 BAUD
74153 E68 — FF2 FE2 FD2 FD1 — F1 F0 — ES2 — D4-3 MUX CLOCK 12-15 H
R31 10K +5V — R32 10K — D4-1 SELECT B — D4-1 SELECT A

BAUD RATE	TIME FOR ONE CYCLE (IN MICROSECONDS)
9600	104
4800	208
2400	417
1200	833

D4-3 MUX CLOCK 12-15 H (ES2) — D2-3 MAINTENANCE CLK PULSE H (ET2) — BJ1 — SOURCE CLOCK A 12-15 L
M2 — SYSTEM MODE 12-15 H — BN2 — SOURCE CLOCK B 12-15 L

R37 7.5K — SEE NOTE 1 — DTE SCTE 12
R36 7.5K — SEE NOTE 1 — DTE SCTE 13
R35 7.5K — SEE NOTE 1 — DTE SCTE 14
R38 7.5K — SEE NOTE 1 — DTE SCTE 15

(CLOCK SOURCE AND SELECTION)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SYNC MUX LINE CARD LINES 12—15 (D4-3)			
SIZE	CODE	NUMBER	REV.	
D	BS	DV11-Ø-13	A	
SCALE		SHEET 3 OF 8	DIST.	

DES DV11-Ø-13 REV A

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D4-4 MODE ØØ (0) H
D4-4 MODE ØØ(1) H
D2-3 LCR 14 H
D2-3 LCR 12 H
D2-3 LCR 11 H
D2-3 LCR Ø9 H
D4-2 RESET A L
D4-2 CARD PARAMETER SELECT 2-15 L
D4-2 BUF CONTROL STROBE L
D4-3 INTR MAINTENANCE 12-15 H
D4-4 MODE Ø1(1) H
D4-4 MODE Ø1(Ø) H
D4-4 TRANS DISABLE 12-15 H
D4-4 BUF MODE ØØ (Ø) H
D4-4 RCV IN 12 H
D4-4 INTR RCV DATA 12-15 L
EIA REC DATA 12
EIA REC DATA 13
D4-4 MODE ØØ (0) H
D4-4 MODE ØØ (1) H
D4-4 TRANS DISABLE 12-15 H
SERIAL OUT 13 L
D4-4 MODE ØØØ H
D4-4 BUF MODE ØØ(Ø)H
D4-4 RCV IN 13 H
EIA XMIT DATA 13
EIA XMIT DATA 12
SERIAL OUT 12 L
D4-4 MODE ØØ (1) H

+5V -12V

D4-8 TMARK 12 L
D4-3 TX CLOCK 12 H
D4-2 RESET H
D4-2 THRL 12 L
D4-2 TR8 H
D4-2 TR7 H
D4-2 TR6 H
D4-2 TR5 H
D4-2 TR4 H
D4-2 TR3 H
D4-2 TR2 H
D4-2 TR1 H
D4-2 STROBE 12 L
D4-1 SYNC Ø8
D4-1 SYNC Ø7
D4-1 SYNC Ø6
D4-1 SYNC Ø5
D4-1 SYNC Ø4
D4-1 SYNC Ø3
D4-1 SYNC Ø2
D4-1 SYNC Ø1
D4-1 PI
D4-1 EPE
D4-1 WLS1
D4-1 WLS2

SAT 12 E73

TCO 12 H
ECC 12 H
D4-4 DA 12 H
D4-4 TRAN FLAG 12 H

SAT 13 E66

TCO 13 H
EOC 13 H
D4-4 DA 13 H
D4-4 TRAN FLAG 13 H

(MODE SELECTION, TRANSMITTERS 12 AND 13)

REVISIONS
CHK | CHANGE NO. | REV.

TITLE SYNC MUX LINE CARD
LINES 12 - 15 (D4-4)
SIZE D CODE DBS NUMBER DV11-Ø-13 REV. A
SCALE SHEET 4 OF 8 DIST.

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EIA REC DATA 14 — J1 HH — 1489 E11 — C88 470 pf

D4-4 MODE ØØ (Ø) H, D4-4 MODE ØØ (1) H — 7450 E9

D4-4 TRANS DISABLE 12-15 H (AF2) — 7402 E12

7400 E23 — BK2 — D4-5 RCV IN 14 H

D4-4 INTR RCV DATA 12-15 L BC1

D4-4 BUF MODE ØØ (Ø) H — +5V — R42 1K — 8242 E2 — 1488 E6 — J1 CC — EIA XMIT DATA 14

D4-4 MODE ØØ (1) H — 7402 E12

7404 E10 — AT2 — SERIAL OUT 14 L

EIA REC DATA 15 — J1 KK — 1489 E11 — C85 470 pf

D4-4 MODE ØØ (Ø) H, D4-4 MODE ØØ (1) H — 7450 E9

7402 E3 — D4-4 TRANS DISABLE 12-15 H (AF2)

7400 E23 — BK1 — D4-5 RCV IN 15 H

D4-4 BUF MODE ØØ (Ø) H — +5V — R43 1K — 8242 E2 — 1488 E26 — J1 EE — EIA XMIT DATA 15

D4-4 MODE ØØ (1) H — 7402 E3

+5V -12V — VSS VGG VDD

SAT 14 E59

D4-8 TMARK 14 L (EL2 17) — CTS
D4-3 TX CLOCK 14 H (5) — TRC
D4-2 RESET H (18) — MR
(10) — DAR
D4-2 THRL 14 L (19) — THRL
D4-2 TR8 H (38) — TR8
D4-2 TR7 H (36) — TR7
D4-2 TR6 H (34) — TR6
D4-2 TR5 H (32) — TR5
D4-2 TR4 H (30) — TR4
D4-2 TR3 H (28) — TR3
D4-2 TR2 H (26) — TR2
D4-2 TR1 H (24) — TR1
D4-2 STROBE 14 L (20) — FHRL
D4-1 SYNC Ø8 (37) — FR8
D4-1 SYNC Ø7 (35) — FR7
D4-1 SYNC Ø6 (33) — FR6
D4-1 SYNC Ø5 (31) — FR5
D4-1 SYNC Ø4 (29) — FR4
D4-1 SYNC Ø3 (27) — FR3
D4-1 SYNC Ø2 (25) — FR2
D4-1 SYNC Ø1 (23) — FR1
(4) — CRL
(22) — CD PI EPE WLS1 WLS2 CS1 CS2 MS1 MS2 (3 2 39 40 6 7 8 9)
D4-1 PI
D4-1 EPE
D4-1 WLS1
D4-1 WLS2

TRO (15) — 7404 E10 — AH2. — SERIAL OUT 15 L

TCO (11 EJ2) — TCO 14 H
DD/EOC (13 EK2) — EOC 14 H
DA (12) — D4-5 DA 14 H
THRE (14) — D4-5 TRAN FLAG 14 H

+5V -12V — VSS VGG VDD

SAT 15 E55

D4-8 TMARK 15 L (EE2 17) — CTS
D4-3 TX CLOCK 15 H (5) — TRC
D4-2 RESET H (18) — MR
(16) — DAR
D4-2 THRL 15 L (19) — THRL
D4-2 TR8 H (38) — TR8
D4-2 TR7 H (36) — TR7
D4-2 TR6 H (34) — TR6
D4-2 TR5 H (32) — TR5
D4-2 TR4 H (30) — TR4
D4-2 TR3 H (28) — TR3
D4-2 TR2 H (26) — TR2
D4-2 TR1 H (24) — TR1
D4-2 STROBE 15 L (20) — FHRL
D4-1 SYNC Ø8 (37) — FR8
D4-1 SYNC Ø7 (35) — FR7
D4-1 SYNC Ø6 (33) — FR6
D4-1 SYNC Ø5 (31) — FR5
D4-1 SYNC Ø4 (29) — FR4
D4-1 SYNC Ø3 (27) — FR3
D4-1 SYNC Ø2 (25) — FR2
D4-1 SYNC Ø1 (23) — FR1
(4) — CRL
(22) — CD PI EPE WLS1 WLS2 CS1 CS2 MS1 MS2 (3 2 39 40 6 7 8 9)
D4-1 PI
D4-1 EPE
D4-1 WLS1
D4-1 WLS2

TRO (15) — 7404 E10 — AH2. — SERIAL OUT 15 L

TCO (11 EJ2) — TCO 15 H
DD/EOC (13 EK2) — EOC 15 H
DA (12) — D4-5 DA 15 H
THRE (14) — D4-5 TRAN FLAG 15 H

REVISIONS		
CHK	CHANGE NO.	REV.

(TRANSMITTERS 14 AND 15)

TITLE SYNC MUX LINE CARD LINES 12 - 15 (D4-5)
SIZE D | CODE BS | NUMBER DV11-Ø-13 | REV. A
SCALE | SHEET 5 OF 8 | DIST.

DEC DWG NO. DV11-Ø-13 REV A

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+5V -12V
VSS VGG VDD
D4-3 RX CLOCK 12 H DE2 31 RRC
D4-4 RCV IN 12 H BF6 35 RI
D4-2 RESET H 32 MR
SAR 12 E50
CLR FLAG 12 L BV2
D4-2 BUF RDE 12 L
74Ø8 E5B
SFR 24
DRR 25
CV2
RESYNC 1 12 (Ø) H
D4-2 STROBE 12 L 34 MHRL
D4-1 SYNC Ø8 40 MHR8
D4-1 SYNC Ø7 4 MHR7
D4-1 SYNC Ø6 38 MHR6
D4-1 SYNC Ø5 3 MHR5
D4-1 SYNC Ø4 36 MHR4
D4-1 SYNC Ø3 17 MHR3
D4-1 SYNC Ø2 22 MHR2
D4-1 SYNC Ø1 18 MHR1
33 CRL
6 CDPI EPE WLS1 WLS2 RMS3 RMS2 RMS1 SS
19 21 5 23 2 39 37 28
D4-1 PI
D4-1 EPE
D4-1 WLS1
D4-1 WLS2
RR9 7
RR8 8 D4-6 RR8 12
RR7 9 D4-6 RR7 12
RR6 10 D4-6 RR6 12
RR5 11 D4-6 RR5 12
RR4 12 D4-6 RR4 12
RR3 13 D4-6 RR3 12
RR2 14 D4-6 RR2 12
RR1 15 D4-6 RR1 12
PE 29 D4-6 PE 12
OE 27 D4-6 OE 12
DR 26
+5V R47 10K
74123 E14 75MS
AR2 DR 12 H
+3V
74Ø8 E18
D4-6 REC FLAG 12 H
74174 E28 RCV FLAG
CLR FLAG 12 L BV2
+5V R46 10K
D4-6 MDET 12 H
MDET 30 12 13
74Ø8 E18
74123 E14 75MS
AV2 MDET 12 H
R45 10K +5V
D4-1 1 SYNC 12
D4-6 BUF LCR 13 H
D4-2 RESYNC PULSE 12 L DL2
+5V R44 1K +3V
D2-3 LCR 13 H BA1
7417 E3Ø
74174 E6Ø SEARCH SYNC
D4-2 STROBE 12 H
D4-3 RX CLOCK 12 H DE2
7408 E35
74174 E68 RESYNC 1
D4-3 RX CLOCK 12 L
+3V
74174 E68 RESYNC 2
DD2 RESYNC 2 12 (Ø) H
7417 E3Ø
74H11 E39
CV2
RESYNC 1 12 (Ø) H
D4-2 RESET A L

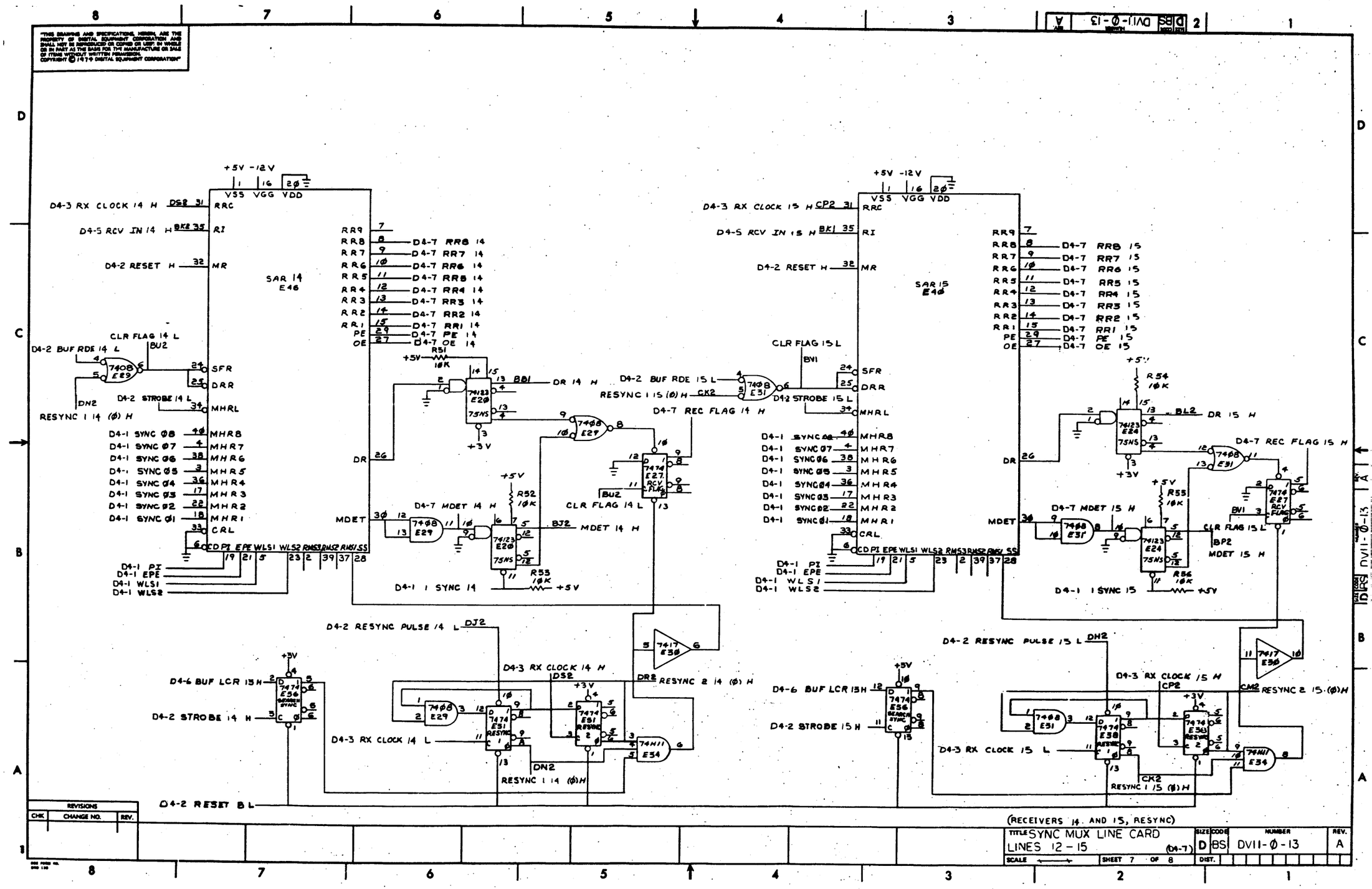
+5V -12V
VSS VGG VDD
D4-3 RX CLOCK 13 H CE2 31 RRC
D4-4 RCV IN 13 H BD1 38 RI
D4-2 RESET H 32 MR
SAR 13 E57
CLR FLAG 13 L BF1
D4-2 BUF RDE 13 L
74Ø8 E1B
SFR 24
DRR 25
RESYNC 1 13 (Ø) H BH2
D4-2 STROBE 13 L 34 MHRL
D4-1 SYNC Ø8 40 MHR8
D4-1 SYNC Ø7 4 MHR7
D4-1 SYNC Ø6 38 MHR6
D4-1 SYNC Ø5 3 MHR5
D4-1 SYNC Ø4 36 MHR4
D4-1 SYNC Ø3 17 MHR3
D4-1 SYNC Ø2 22 MHR2
D4-1 SYNC Ø1 18 MHR1
33 CRL
6 CDPI EPE WLS1 WLS2 RMS3 RMS2 RMS1 SS
19 21 5 23 2 39 37 28
D4-1 PI
D4-1 EPE
D4-1 WLS1
D4-1 WLS2
RR9 7
RR8 8 D4-6 RR8 13
RR7 9 D4-6 RR7 13
RR6 10 D4-6 RR6 13
RR5 11 D4-6 RR5 13
RR4 12 D4-6 RR4 13
RR3 13 D4-6 RR3 13
RR2 14 D4-6 RR2 13
RR1 15 D4-6 RR1 13
PE 29 D4-6 PE 13
OE 27 D4-6 OE 13
DR 26
+5V 24Ø 10K
74123 E19 75MS
AU2 DR 13 H
+3V
74Ø8 E18
D4-6 REC FLAG 13 H
74174 E68 RCV FLAG
CLR FLAG 13 L BF1
+5V R49 10K
D4-6 MDET 13 H
MDET 30 4 5
74Ø8 E35
74123 E19 75MS
BH1 MDET 13 H
R86 10K +5V
D4-1 1 SYNC 13
D4-2 RESYNC PULSE 13 L DR2
+3V
D4-6 BUF LCR 13 H
74174 E6Ø SEARCH SYNC
D4-2 STROBE 13 H
D4-3 RX CLOCK 13 H CE2
7408 E35
74174 E32 RESYNC 1
D4-3 RX CLOCK 13 L
74174 E32 RESYNC 2
CF2 RESYNC 2 13 (Ø) H
7417 E3Ø
74H11 E34
BH2 RESYNC 1 13 (Ø) H

(RECEIVERS 12 AND 13, RESYNC)

REVISIONS
CHK | CHANGE NO. | REV.

TITLE SYNC MUX LINE CARD
LINES 12 - 15 (D4-6)
SIZE D | CODE BS | NUMBER DVII-Ø-13 | REV. A
SCALE —— | SHEET 6 OF 8 | DIST.

DVII-Ø-13 A



(RECEIVERS 14 AND 15, RESYNC)

TITLE	SIZE	CODE	NUMBER	REV.
SYNC MUX LINE CARD LINES 12 - 15 (D4-7)	D	BS	DV11-Ø-13	A

SCALE — SHEET 7 OF 8 — DIST.

REVISIONS

CHK	CHANGE NO.	REV.

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D4-7 RR6 15
D4-7 RR6 14
D4-6 RR6 13
D4-6 RR6 12
D4-7 RR5 15
D4-7 RR5 14
D4-6 RR5 13
D4-6 RR5 12
74153 STB1 STB0 DI E42 C1 B1 A1 D0 C0 B0 A0 SI S0 F1 F0
8881 E74 → FRI RECV DATA Ø5 L
8881 E74 → FSI RECV DATA Ø4 L

D4-7 PE 15
D4-7 PE 14
D4-6 PE 13
D4-6 PE 12
D4-7 OE 15
D4-7 OE 14
D4-6 OE 13
D4-6 OE 12
74153 STB1 STB0 DI E44 C1 B1 A1 D0 C0 B0 A0 SI S0 F1 F0
8881 E78 → FMI MASTER PE L
8881 E78 → FLI MASTER OR L

D4-7 RR4 15
D4-7 RR4 14
D4-6 RR4 13
D4-6 RR4 12
D4-7 RR3 15
D4-7 RR3 14
D4-6 RR3 13
D4-6 RR3 12
74153 STB1 STB0 DI E45 C1 B1 A1 D0 C0 B0 A0 SI S0 F1 F0
8881 E74 → FNI RECV DATA Ø5 L
8881 E74 → FPI RECV DATA Ø2 L

D3-3 CLEAR TMARK L FK2 15
74155 STB1 STB0 E76 DB DA FB3 FB2 FB1 FB0 FA3 FA2 FA1 FA0 SI S0

D4-2 SET TMARK 15 L
D4-2 SET TMARK 14 L
D4-2 SET TMARK 13 L
D4-2 SET TMARK 12 L
D4-2 RESET H
7474 E68 MARK → EE2 D4-8 TMARK 15 L
7474 E68 MARK → EL2 D4-8 TMARK 14 L
7474 E68 MARK → CB2 D4-8 TMARK 13 L
7474 E68 MARK → CD2 D4-8 TMARK 12 L

D4-2 CARD FLAG SELECT 12-15 L DM2

D4-7 RR2 15
D4-7 RR2 14
D4-6 RR2 13
D4-6 RR2 12
D4-7 RR1 15
D4-7 RR1 14
D4-6 RR1 13
D4-6 RR1 12
74153 STB1 STB0 E49 DI C1 B1 A1 D0 C0 B0 A0 SI S0 F1 F0
8881 E71 → FN2 RECV DATA Ø1 L
8881 E71 → FP2 RECV DATA ØØ L

D4-7 RR8 15
D4-7 RR8 14
D4-6 RR8 13
D4-6 RR8 12
D4-7 RR7 15
D4-7 RR7 14
D4-6 RR7 13
D4-6 RR7 12
74153 STB1 STB0 E36 DI C1 B1 A1 D0 C0 B0 A0 SI S0 F1 F0
8881 E78 → FHI RECV DATA Ø7 L
8881 E78 → FJI RECV DATA Ø6 L

D4-2 BUF MASTER SCAN Ø1 H
D4-2 BUF MASTER SCAN ØØ H
D4-2 DATA ENABLE 12-15 H (FK1)

REVISIONS
CHK | CHANGE NO. | REV.

(RECV DATA MUXS AND TMARK DECODER)

TITLE SYNC MUX LINE CARD LINES 12 - 15 (D4-8)
SIZE D | CODE BS | NUMBER DVII-Ø-13 | REV. A
SCALE | SHEET 8 OF 8 | DIST.

DVII-Ø-13 A

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This microprogram listing lists the 9 bit binary address of each micro instructions, followed by the 16 bit micro instruction as it would appear in the ROM DATA REGISTER (D3-2), followed by an explanation of the micro instruction. Contents of the ROM DATA REGISTER are the complement of the ROM chip outputs. Odd addresses reference one set of 4 ROM chips, even addresses reference the other set of 4 ROM chips.

BITS	ADDRESSES	PART NUMBER	ROM LIST
15-12	even	23-192A2	K-CS-M7838-Ø-15
11-8	even	23-191A2	K-CS-M7838-Ø-14
7-4	even	23-189A2	K-CS-M7838-Ø-12
3-0	even	23-190A2	K-CS-M7838-Ø-13
15-12	odd	23-185A2	K-CS-M7838-Ø-8
11-8	odd	23-186A2	K-CS-M7838-Ø-9
7-4	odd	23-188A2	K-CS-M7838-Ø-11
3-0	odd	23-187A2	K-CS-M7838-Ø-1Ø

Diagnostic DZDVC Test #1 compares ROM DATA REGISTER contents with this listing. Use the above table to determine which ROM is faulty. Bit 15 is at left end of word Bit Ø at right end.

FIRST USED ON OPTION MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
DV11		PARTS LIST		

DRN. Robert Koppenal	DATE 3-31-75	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
CHK'D Ted Roberts	DATE 4-17-75	TITLE MICROPROGRAM LISTING
ENG. [illegible]	DATE 4-17-75	
PROJ. ENG. [illegible]	DATE 4-17-75	
PROD. R. Wall	DATE 4-17-75	
NEXT HIGHER ASSEMBLY B-DD-DV11-Ø		SIZE K CODE CS NUMBER DV11-Ø-14 REV. A
SCALE —		
SHEET 1 OF 13		DIST.

REVISIONS

CHK	CHANGE NO.	REV.
[illegible]	DV11-00002	A

DEC FORM NO. DRB 109

```
                                        ;IDLE LOOP

00 00000000  0101000001000010   ILOOP  S/C     6,2      ;INCREMENT SCANNER
00 00000001  0011000001010100           XFR     ,5,4     ;MOVE MASTER SCAN TO RAM ADDRESS
00 00000010  0000001011100100           BRA     2,TSERV  ;TEST FOR TRANSMIT FLAG WAITING, IF YES BRANCH TO TRANSMIT SERVICE
00 00000011  0000010000001010           BRA     4,RSERV  ;TEST FOR RECEIVER FLAG WAITING, IF YES BRANCH TO RECEIVE FLAG SERV
00 00000100  0000001101000011           BRA     3,SSERV  ;TEST FOR RECEIVED CHARACTER WAITING, IF YES BRANCH TO RECEIVED CHA
00 00000101  0010000000001011   ILOP2  RAM     0,0,13   ;OBTAIN LINE STATE
00 00000110  0111000100101110           BRB     1,RSYNC  ;TEST RAM OUTPUT 01 (RESYNC), IF YES BRANCH TO RESYNCHRONIZE
00 00000111  0111001000111010           BRB     2,TMARK  ;TEST RAM OUTPUT 02 (XMIT GO), IF YES BRANCH TO CLEAR TMARK
00 00001000  0000010100101001   ILOP5  BRA     5,ISERV  ;TEST FOR CHARACTER DISPATCH PROCEED, (SCR 08) IF YES BRANCH T
00 00001001  0000000100000000           BRA     1,ILOOP  ;TEST FOR SURE TRUE, IF YES BRANCH TO IDLE LOOP


                                        ;RECEIVE FLAG SERVICE  (LINE STATE IS IN RAM OUTPUT)

00 00001010  0010000000001011   RSERV  RAM     0,0,13   ;OBTAIN LINE STATE
00 00001011  0111000000011110           BRB     0,TESTX  ;TEST RAM OUTPUT 00 (RECEIVER ACTIVE), IF YES BRANCH TO TESTX
00 00001100  0111110100001111           BRB     15,S/ACT         ;TEST MATCH DETECT, IF YES BRANCH TO SET ACTIVE
00 00001101  0101000001000110           S/C     6,6      ;SET RESYNC PULSE,
00 00001110  0000000100000000           BRA     1,ILOOP  ;TEST FOR SURE TRUE, IF YES BRANCH TO ILOOP
00 00001111  0010000000001010   S/ACT  RAM     0,0,12   ;OBTAIN DLE/PROTOCOL
00 00010000  0111000100011000           BRB     1,SACT2  ;TEST RAM 01 (STRIP LEADING SYNC), IF YES BRANCH TO SACT2
00 00010001  0010000000001011   SACT1  RAM     0,0,13   ;OBTAIN LINE STATE
00 00010010  0101000000100111           S/C     5,7      ;SET RAM OUTPUT 00 (RECEIVER ACTIVE)
00 00010011  0010000110111011           RAM     1,13,13  ;WRITE NEW LINE STATE
00 00010100  0111111000100001           BRB     16,SACT1         ;TEST FOR WRITE INHIBIT, IF YES BRANCH TO SACT 1
00 00010101  0101000000010011   CLRRF  S/C     4,3      ;SET RECEIVE DATA ENABLE
00 00010110  0101000000010010           S/C     4,2      ;CLEAR RECEIVE DATA ENABLE AND DATA AVAILABLE (FLAG WAITING)
00 00010111  0000000100000000           BRA     1,ILOOP  ;TEST FOR SURE TRUE, IF YES BRANCH TO IDLE LOOP
00 00011000  0010000000001011   SACT2  RAM     0,0,13   ;OBTAIN LINE STATE
00 00011001  0101000000100111           S/C     5,7      ;SET RAM OUTPUT 00 (RECEIVER ACTIVE)
00 00011010  0101000010000110           S/C     7,6      ;SET RAM OUTPUT 06 (STRIP SYNC ON)
00 00011011  0010000110111011           RAM     1,13,13  ;WRITE NEW LINE STATE
00 00011100  0111111000011000           BRB     16,SACT2         ;TEST FOR WRITE INHIBIT, IF YES BRANCH TO SACT 2
00 00011101  0000000100010101           BRA     1,CLRRF  ;TEST FOR SURE TRUE, IF YES BRANCH TO CLRRF


00 00011110  0010000000001011   TESTX  RAM     0,0,13   ;OBTAIN LINE STATE
00 00011111  0111011000100001           BRB     6,TMD    ;TEST RAM OUTPUT 06 (STRIP SYNC ON), IF YES BRANCH TO TMD
00 00100000  0000000100100101           BRA     1,S/RDE  ;TEST FOR SURE TRUE, IF YES BRANCH TO S/RDE
00 00100001  0111111010001010   TMD    BRB     15,CLRRF         ;TEST MATCH DETECT, IF YES BRANCH TO CLRRF
00 00100010  0101000010000010           S/C     7,2      ;CLEAR RAM OUTPUT 06 (STRIP SYNC ON)
00 00100011  0010000110111011           RAM     1,13,13  ;WRITE NEW LINE STATE
00 00100100  0111111000000110           BRB     16,RSERV         ;TEST FOR WRITE INHIBIT, IF YES BRANCH TO RSERV
00 00100101  0101000000010011   S/RDE  S/C     4,3      ;SET RECEIVE DATA ENABLE
00 00100110  0101000000010001           S/C     4,1      ;SET SILO IN
00 00100111  0101000000010010           S/C     4,2      ;CLEAR RECEIVE DATA ENABLE AND DATA AVAILABLE (FLAG WAITING)
00 00101000  0000000100000000           BRA     1,ILOOP  ;TEST FOR SURE TRUE, IF YES BRANCH TO ILOOP

                                        ;RECEIVE INTERRUPT RESPONSE SERVICE

00 00101001  0011000011000001   ISERV  XFR     ,14,1    ;MOVE SILO OUT TO A REGISTER
00 00101010  0001000000011111           ALU     37       ;LET ALU RESULT = A REGISTER
00 00101011  0011000001100100           XFR     ,6,4     ;MOVE ALU RESULT 08-11 TO RAM ADDRESS REGISTER 00-03
00 00101100  0101000000001110           S/C     3,6      ;CLEAR SCR08
00 00101101  0000000101100010           BRA     1,CTEST  ;TEST FOR SURE TRUE, IF YES BRANCH TO CTEST
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                                        ;RESYNCHRONIZE (MASTER SCAN IS IN RAM AR; LINE STATE IS IN RAM OUTPUT)

00 0101110  0010000000001011    RSYNC  RAM     0;0,13  ;OBTAIN LINE STATE
00 0101111  0101000000100011           S/C     5;3     ;CLEAR RAM OUTPUT 00 (RECEIVER ACTIVE)
00 0110000  0101000000100001           S/C     5;1     ;CLEAR RAM OUTPUT 01 (RESYNCHRONIZE)
00 0110001  0010000110111011           RAM     1;13,13 ;WRITE NEW LINE STATE
00 0110010  0111111000101110           BRB     16,RSYNC        ;TEST FOR WRITE INHIBIT, IF YES BRANCH BACK
00 0110011  0010000000001110    PSI    RAM     0;0,16  ;OBTAIN LINE PROTOCOL
00 0110100  0101000010000100           S/C     7;4     ;SET RAM OUTPUT 07
00 0110101  0010000110111110           RAM     1;13,16 ;WRITE NEW LINE PROTOCOL
00 0110110  0111111000110011           BRB     16,PSI  ;TEST FOR WRITE INHIBIT, IF YES BRANCH BACK
00 0110111  0101000001000110           S/C     6;6     ;SET RESYNC PULSE
00 0111000  0101000000010001           S/C     4;1     ;SET SILO IN
00 0111001  0000000100000101           BRA     1;ILOP2 ;TEST FOR SURE TRUE, IF YES BRANCH TO ILOP2 (ILOOP +2)


                                        ;CLEAR TMARK

00 0111010  0101000001000001    TMARK  S/C     6;1     ;CLEAR TMARK
00 0111011  0000000100001000           BRA     1;ILOP5 ;TEST FOR SURE TRUE, IF YES BRANCH TO IDLE LOOP +5


                                        ;TEST FOR RESYNC FLAG (LINE NUMBER IN RAM AR, CHARACTER IN ALU RESULT)

00 0111100  0000000000111110    TFRF   BRA     0;CRAM7 ;TEST BIT 15 OF ALU RESULT, IF YES BRANCH TO HERE +2
00 0111101  0000000110000011           BRA     1;DISC  ;TEST FOR SURE TRUE, IF YES BRANCH TO DISCARD RECEIVED CHARACTER
00 0111110  0010000000001110    CRAM7  RAM     0;0,16  ;OBTAIN LINE PROTOCOL
00 0111111  0101000010000000           S/C     7;0     ;CLEAR RAM OUTPUT 07 (RESYNCH FLAG NOT FOUND)
01 0000000  0010000110111110           RAM     1;13,16 ;WRITE NEW LINE PROTOCOL
00 1000001  0111111000111110           BRB     16,CRAM7        ;TEST FOR WRITE INHIBIT,IF YES BRANCH BACK
00 1000010  0000000110000011           BRA     1;DISC  ;TEST FOR SURE TRUE, IF YES BRANCH TO DISCARD RECEIVED CHARACTER

                                        ;RECEIVED CHARACTER SILO SERVICE

00 1000011  0000010100010001    SSERV  BRA     5;ISERV ;TEST FOR SCR08 (COULD HAVE SET BETWEEN 7 AND 9 INST OF ILOOP)
00 1000100  0011000011000001           XFR     ,12,1   ;MOVE SILO OUT TO A REGISTER
00 1000101  0000100000011111           ALU     3       ;LET ALU RESULT = A REGISTER
00 1000110  0011000001100100           XFR     ,0,4    ;MOVE ALU RESULT 08-11 TO RAM ADDRESS REGISTER 00-03
00 1000111  0010000000001011           RAM     0;0,13  ;OBTAIN LINE STATE
00 1001000  0111000110000011           BRB     1;DISC  ;TEST RAM OUTPUT 01 (RESYNC), IF YES BRANCH TO DISCARD
00 1001001  0010000000011110           RAM     0;0,16  ;OBTAIN LINE PROTOCOL
00 1001010  0111011100111100           BRB     7;TFRF  ;TEST RAM OUTPUT 07, IF YES BRANCH TO TEST FOR RESYNC FLAG
00 1001011  1000100010110001           BRA     10,POER ;TEST BITS  13, 14 OF ALU RESULTS, IF YES BRANCH TO PARITY/OVERRUN
00 1001100  0111011010111010           BRB     6;T8C2  ;TEST RAM OUTPUT 06, IF YES BRANCH TO THIS IS BCC 2
00 1001101  0111010110100101           BRB     5;T8C1  ;TEST RAM OUTPUT 05, IF YES BRANCH TO THIS IS BCC 1
00 1001110  0010000000000101           RAM     0;0,5   ;OBTAIN RECEIVER BYTE COUNT
00 1001111  0111111010001100           BRB     14,CRBC0        ;TEST RAM OUTPUT 0-14=0, IF YES BRANCH TO CHARACTER RECEIVED WHILE
01 1010000  0010000000001010           RAM     0;0,12  ;OBTAIN TRANSMITTER DLE/LINE PROTOCOL ??
00 1010001  0111010101111110           BRB     5;DDCMR ;TEST RAM OUTPUT 05, IF YES BRANCH TO DDCMP RECV
00 1010010  0010000000001101           RAM     0;0,15  ;OBTAIN RECEIVER MODE BITS
00 1010011  0011000010100010    ZETA   XFR     ,12,2   ;MOVE RAM OUTPUT DATA TRANSLATED 0-2/8-10 TO B REGISTER
00 1010100  0101000000010111           S/C     4;7     ;CLEAR ALU RESULT UPPER BYTE
00 1010101  0011000011110001           XFR     ,17,1   ;MOVE ALU RESULT TO A REGISTER
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00 1010110  0001000000010110           ALU     20      ;LET ALU RESULTS = A PLUS B
00 1010111  0010000111100010           XFR     ,17,2   ;MOVE ALU RESULTS TO B REGISTER
00 1011000  0010000000001001           RAM     0;0,11  ;OBTAIN RECEIVER CONTROL TABLE BASE ADDRESS
00 1011001  0011000010110001           XFR     ,13,1   ;MOVE RAM OUTPUT DATA TO A REGISTER (BASE ADDRESS)
00 1011010  0001000000010110           ALU     20      ;LET ALU RESULTS = A PLUS B (EFFECTIVE ADDRESS)
00 1011011  0011000011110011           XFR     1;17,3  ;MOVE ALU RESULTS TO NPR ADDRESS REGISTER
00 1011100  0100000000000000           NPR             ;DO NPR TO GET CONTROL BYTE
00 1011101  0111100101011101    RBUS1  BRB     11,RBUS1        ;TEST REQUEST BUS, IF YES, BRANCH TO HERE
00 1011110  0000011011011010           BRA     6;RNXMC ;TEST NXM, IF YES, BRANCH TO RECEIVER NXM / CONTROL BYTE
00 1011111  0111101011010111           BRB     15,RMPEC        ;TEST MEM PAR ERR, IF YES, BRANCH TO RECEIVER MPE/CONTROL BYTE
00 1100000  0010000000001111           RAM     0;0,17  ;OBTAIN CONTROL BYTE STORAGE REGISTER (TO CLEAR INTERLOCK)
00 1100001  0010000110011111           RAM     1;11,17 ;MOVE DATI REGISTER TO RAM AND WRITE CONTROL BYTE STORAGE REGISTER


                                        ;CONTROL BYTE TESTS BEGIN (CHARACTER IS IN SILO OUT, CONTROL BYTE IS IN RAM 17)

00 1100010  0010000000001111    CTEST  RAM     0;0,17  ;OBTAIN CONTROL BYTE STORAGE REGISTER
00 1100011  0011000010110010           XFR     ,13,2   ;MOVE RAM OUTPUT TO B REGISTER
00 1100100  0001000000000101           ALU     5       ;LET ALU RESULT = B REGISTER
00 1100101  0010000101111101           RAM     1;7,15  ;MOVE ALU RESULTS TRANSLATED 5-7/0-2 TO RAM (AND WRITE NEW MODE BITS
00 1100110  1000101010101011           BRA     14,CBINT        ;TEST BIT 0 OF ALU RESULT, IF YES BRANCH TO CONTROL BYTE INTERRUPT
00 1100111  0000110010011011           BRA     14,EBCC ;TEST BIT 02 OF ALU RESULT, IF YES BRANCH TO SET EXPECT BCC 1 NEXT
00 1101000  0000011011000101    EPSIL  BRA     15,RBCC ;TEST BIT 03 OF ALU RESULT, IF YES, BRANCH TO CALCULATE RECV B


                                        ;RETURN FROM RECV BCC  (CONTROL BYTE IS STILL IN ALU RESULT)

00 1101001  0000011101000011    RRBCC  BRA     16,DISC ;TEST BIT 4 OF ALU RESULT, IF YES, BRANCH TO (BIT 4 SET = DISC
00 1101010  0010000000001100           RAM     0;0,4   ;OBTAIN RECEIVER CURRENT ADDRESS
00 1101011  0011001110110011           XFR     0;13,3  ;MOVE RAM OUTPUT TO NPR ADDRESS REGISTER
00 1101100  0011000011000101           XFR     ,14,5   ;MOVE SILO OUT TO DATO REGISTER (FOR USE IF NEXT CHARACTER WILL HAVE
00 1101101  0100000000000000           NPR             ;DO NPR TO STORE RECEIVED CHARACTER
00 1101110  0111100101101110    RBUS2  BRB     11,RBUS2        ;TEST REQUEST BUS, IF YES, BRANCH TO HERE
00 1101111  0000011011100000           BRA     6;RNXM  ;TEST NXM, IF YES, BRANCH TO RECEIVER NXM
00 1110000  0010000000001101    DRBC   RAM     0;0,5   ;OBTAIN RECEIVER BYTE COUNT
00 1110001  0011000010110001           XFR     ,13,1   ;MOVE RAM OUTPUT TO REGISTER A
00 1110010  0001000000111111           ALU     77      ;LET ALU RESULTS = A+1
00 1110011  0010000111110101           RAM     1;17,5  ;MOVE ALU RESULTS TO RAM INPUT (AND WRITE NEW BYTE COUNT)
00 1110100  0111111001110000           BRB     16,DRBC ;TEST FOR WRITE INHIBIT, IF YES BRANCH TO  HERE -4
00 1110101  0010000000001100    DRC=   RAM     0;0,4   ;OBTAIN RECEIVER CURRENT ADDRESS
00 1110110  0011000010110001           XFR     ,13,1   ;MOVE RAM OUTPUT DATA TO REGISTER A
00 1110111  0001000000111111           ALU     77      ;LET ALU RESULTS = A+1
00 1111000  0010000111110100           RAM     1;17,4  ;MOVE ALU RESULTS TO RAM INPUT (AND WRITE NEW ADDRESS)
00 1111001  0111111001110101           BRB     16,DRCA ;TEST FOR WRITE INHIBIT, IF YES BRANCH TO HERE -4
00 1111010  0010000000000101           RAM     0;0,5   ;OBTAIN RECEIVER BYTE COUNT
00 1111011  0111111001000111           BRB     14,NBC0 ;TEST RAM OUTPUT 0-14=0, IF YES, BRANCH TO NEXT CHARACTER WILL HAVE
00 1111100  0101000000010000           S/C     4;0     ;SET SILO OUT
00 1111101  0000000100000200           BRA     1;ILOOP ;TEST FOR SURE TRUE, IF YES BRANCH TO IDLE LOOP


                                        ;DDCMP RECEPTION

00 1111110  0010000000001101    DDCMR  RAM     0;0,15  ;OBTAIN RECEIVER MODE BITS
00 1111111  0111111001000001           BRB     14,DDCM2        ;TEST RAM OUTPUT 0-14=0, IF YES BRANCH TO DDCM2
01 0000000  0000000101010011           BRA     1;ZETA  ;TEST FOR SURE TRUE, IF YES BRANCH TO ZETA
01 0000001  0001000000001100    DDCM2  ALU     14      ;LET ALU RESULT = 0
01 0000010  0000000110000101           BRA     1;RBCC  ;TEST FOR SURE TRUE, IF YES BRANCH TO CALCULATE RECV BCC
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                                    ;DISCARD RECEIVED CHARACTER

0100000011  0101000000010000    DISC   S/C     4,0      ;SET SILO OUT
0100000100  0000000100000000           BRA     1,ILOOP  ;TEST FOR SURE TRUE, IF YES BRANCH TO IDLE LOOP

                                    ;CALCULATE RECV BCC (ASSUME RECEIVED CHARACTER IN SILO OUT)

0100000101  0011000011000001   RBCC   XFR     ,14,1    ;MOVE SILO OUT REGISTER TO A REGISTER
0100000110  0010000000000111           RAM     0,0,7    ;OBTAIN RECV BCC CALCULATED TO DATE
0100000111  0011000010110010           XFR     ,13,2    ;MOVE RAM OUTPUT DATA TO B REGISTER
0100001000  0010000000001010           RAM     0,0,12   ;OBTAIN TRANSMITTER DLE/LINE PROTOCOL II
0100001001  0110000000000000           BCC              ;PERFORM SPECIFIED BCC CALCULATION
0100001010  0010000111100111           RAM     1,16,7   ;MOVE BCC TO RAM INPUT AND WRITE NEW RECEIVER BCC
0100001011  0000000101101001           BRA     1,RRBCC  ;TEST FOR SURE TRUE, IF YES, BRANCH TO RETURN FROM RECV BCC

                                    ;CHARACTER RECEIVED WHILE RECV BC=0

0100001100  0011000011000110   CRBC0  XFR     ,14,6    ;MOVE SILO OUT REGISTER TO RICR
0100001101  0101000000001000           S/C     3,0      ;SET RICR 15 (TO INDICATE RECEPTION WHILE BC=0)
0100001110  1000000110110010           BRA     1,CNACB  ;TEST FOR SURE TRUE, IF YES BRANCH TO CREATE NULL ACTION CONTROL BY

                                    ;NEXT CHARACTER WILL HAVE BC=0  (SILO OUT HAS BEEN SET, RECEIVER BYTE COUNT IS 1

0100001111  0011000011010110   NBC0   XFR     ,15,6    ;MOVE NPR DATO REGISTER TO RICR
0100010000  0101000000001001           S/C     3,1      ;SET RICR 14 (TO INDICATE RECEPTION OF NEXT CHARACTER WILL BE BC=0)
0100010001  0111121110010011           BRB     15,MCBCX         ;TEST RAM OUTPUT 15, IF TRUE BRANCH TO MODE CHANGE / BCC EXPECT
0100010010  1000000110110010           BRA     1,CNACB  ;TEST FOR SURE TRUE, IF YES BRANCH TO  CREATE NULL ACTION CONTROL B

                                    ;MODE CHANGE AND BCC EXPECT

0100010011  0010000000001011   MCBCX  RAM     0,0,13   ;OBTAIN LINE STATE
0100010100  0011000010110010          XFR     ,13,2    ;MOVE RAM OUTPUT TO B REGISTER
0100010101  0011000010000010          XFR     ,10,2    ;MOVE B REGISTER 0-15 TO B REGISTER 0-7
0100010110  0001000000000101          ALU     5        ;LET ALU RESULT = B REGISTER
0100010111  0010000101111101          RAM     1,7,15   ;MOVE ALU RESULTS TRANSLATED TO RAM AND WRITE NEW  RECV MODE BITS
0100011000  0010000111111111          RAM     1,17,17  ;WRITE CONTROL BYTE STORAGE FROM ALU RESULT
0100011001  0000110010100000          BRA     14,EBCN  ;TEST ALU RESULT 02, IF YES BRANCH TO EXPECT BCC NEXT BECAUSE OF BC
0100011010  1000000110110010          BRA     1,CNACB  ;TEST FOR SURE TRUE, IF YES BRANCH TO CREATE NULL ACTION CONTROL BY

                                    ;EXPECT BCC NEXT BECAUSE OF CONTROL BYTE

0100011011  0010000000001110   EBCC   RAM     0,0,16   ;OBTAIN LINE PROTOCOL
0100011100  0101000010000101          S/C     7,5      ;SET RAM OUTPUT 05 (EXPECT BCC 1 NEXT)
0100011101  0010300110111110          RAM     1,13,16  ;WRITE LINE PROTOCOL FROM RAM OUTPUT
0100011110  0111111010011011          BRB     16,EBCC  ;TEST FOR WRITE INHIBIT, IF YES BRANCH BACK
0100011111  0000000101101000          BRA     1,EPSIL  ;TEST FOR SURE TRUE, IF YES BRANCH TO EPSIL

                                    ;EXPECT BCC NEXT BECAUSE OF BC = 0

0100100000  0010000000001110   EBCN   RAM     0,0,16   ;OBTAIN LINE PROTOCOL
0100100001  0101000010000101          S/C     7,5      ;SET RAM OUTPUT 05 (EXPECT BCC1 NEXT)
0100100010  0010000110111110          RAM     1,13,16  ;WRITE LINE PROTOCOL FROM RAM OUTPUT
0100100011  0111111010100000          BRB     16,EBCN  ;TEST FOR WRITE INHIBIT, IF YES BRANCH TO EBCN
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0100100100  0010000011000011           BRA     1,DISC   ;TEST FOR SURE TRUE, IF YES BRANCH TO DISCARD

                                    ;THIS IS BCC 1

0100100101  0010000000001110   TBC1   RAM     0,0,16   ;OBTAIN LINE PROTOCOL
0100100110  0101000010000001          S/C     7,1      ;CLEAR RAM OUTPUT 05 (EXPECT BCC 1 NEXT)
0100100111  0101000010000110          S/C     7,6      ;SET RAM OUTPUT 06 (EXPECT BCC 2 NEXT)
0100101000  0010000110111110          RAM     1,13,16  ;WRITE LINE PROTOCOL FROM RAM
0100101001  0111111010010101          BRB     16,TBC1  ;TEST FOR WRITE INHIBIT, IF YES BRANCH BACK
0100101010  0011000011000001          XFR     ,14,1    ;MOVE SILO OUT REGISTER TO A REGISTER
0100101011  0010000000000111          RAM     0,0,7    ;OBTAIN RECV BCC CALCULATED TO DATE
0100101100  0011000010110010          XFR     ,13,2    ;MOVE RAM OUTPUT DATA TO B REGISTER
0100101101  0010000000001010          RAM     0,0,12   ;OBTAIN TRANSMITTER DLE/LINE PROTOCOL II
0100101110  0110000000000000          BCC              ;PERFORM SPECIFIED BCC CALCULATION
0100101111  0010300111100111          RAM     1,16,7   ;MOVE BCC TO RAM INPUT AND WRITE NEW RECEIVER BCC
0100110000  0010000000001010          RAM     0,0,12   ;OBTAIN TRANSMITTER DLE/LINE PROTOCOL II (TO LOOK FOR LRC)
0100110001  0111021110111000          BNB     3,TBC1X  ;TEST RAM OUTPUT 03
0100110010  0111010010111000          BRB     4,TBC1X  ;TEST RAM OUTPUT 04
0100110011  0010000000001110   MRTMA  RAM     0,0,16   ;OBTAIN LINE PROTOCOL
0100110100  0101000010000010          S/C     7,2      ;CLEAR RAM OUTPUT 06 (EXPECT BCC2 NEXT)
0100110101  0010000110111110          RAM     1,13,16  ;WRITE LINE PROTOCOL
0100110110  0111111010110011          BRB     10,MRTMA         ;TEST FOR WRITE INHIBIT, IF YES BRANCH BACK
0100110111  0000000111000100          BRA     1,BCCCK  ;TEST FOR SURE TRUE, IF YES BRANCH  TO BCC CHECK COMPLETE
0100111000  0101000000010000   TBC1X  S/C     4,0      ;SET SILO OUT
0100111001  0000000100000000          BRA     1,ILOOP  ;TEST FOR SURE TRUE, IF YES BRANCH TO IDLE LOOP

                                    ;THIS IS BCC 2

0100111010  0010000000001110   TBC2   RAM     0,0,16   ;OBTAIN LINE PROTOCOL
0100111011  0101000010000010          S/C     7,2      ;CLEAR RAM OUTPUT 06
0100111100  0010000110111110          RAM     1,13,16  ;WRITE LINE PROTOCOL
0100111101  0111111010111010          BRB     16,TBC2  ;TEST FOR WRITE INHIBIT, IF YES BRANCH BACK
0100111110  0011000011000001          XFR     ,14,1    ;MOVE SILO OUT REGISTER TO A REGISTER
0100111111  0010000000000111          RAM     0,0,7    ;OBTAIN RECV BCC CALCULATED TO DATE
0101000000  0011000010110010          XFR     ,13,2    ;MOVE RAM OUTPUT DATA TO B REGISTER
0101000001  0010000000001010          RAM     0,0,12   ;OBTAIN TRANSMITTER DLE/LINE PROTOCOL II
0101000010  0110000000000000          BCC              ;PERFORM SPECIFIED BCC CALCULATION
0101000011  0010000111100111          RAM     1,16,7   ;MOVE BCC TO RAM INPUT AND WRITE NEW RECEIVER BCC
0101000100  0001000000011100   BCCCK  ALU     34       ;LET ALU RESULT = MINUS 1
0101000101  0101000000010111          S/C     4,7      ;CLEAR ALU RESULT UPPER BYTE
0101000110  0011000011100001          XFR     ,17,1    ;MOVE ALU RESULT TO A REGISTER
0101000111  0011000011000010          XFR     ,14,2    ;MOVE SILO OUT TO B REGISTER
0101001000  0001000000001101          ALU     15       ;LET ALU RESULT = AND OF A COMPLEMENT AND B
0101001001  0011000011100010          XFR     ,17,2    ;MOVE ALU RESULT TO B REGISTER
0101001010  0011000011100001          XFR     ,16,1    ;MOVE BCC TO A REGISTER
0101001011  0001000000011111          ALU     37       ;LET ALU RESULT = A
0101001100  0101000000010111          S/C     4,7      ;CLEAR ALU RESULT UPPER BYTE
0101001101  0011000011100001          XFR     ,17,1    ;MOVE ALU RESULT TO A REGISTER
0101001110  0001000000011110          ALU     36       ;LET ALU RESULT= A OR B
0101001111  0011000011100001          XFR     ,17,1    ;MOVE ALU RESULT TO A REGISTER
0101010000  0011000011000010          XFR     ,16,2    ;MOVE BCC TO B REGISTER
0101010001  0011000010000010          XFR     ,10,2    ;MOVE B REGISTER 0-15 TO B REGISTER 0-7 (UPPER BYTE OF BCC)
0101010010  0001000000011110          ALU     36       ;LET ALU RESULT = A OR B
0101010011  0011000011110110          XFR     ,17,6    ;MOVE ALU RESULT TO RICR REGISTER
0101010100  0101000000001101          S/C     3,5      ;SET RICR 12
0101010101  0101000000010001          S/C     3,1      ;SET RICR 14
0101010110  1000000110110010          BRA     1,CNACB  ;TEST FOR SURE TRUE, IF YES BRANCH TO CREATE NULL ACTION CONTROL BY.
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                                    ;RECEIVER MPE / CONTROL BYTE
0|10|10111  0011000011000110    RMPEC  XFR     ,14,6   ;MOVE SILO OUT TO RICR REGISTER
0|10|11000  0101000000001100            S/C     3,4     ;SET RICR 13
0|10|11001  0000000111011011            BRA     1,GAMMA ;TEST FOR SURE TRUE, IF YES BRANCH TO RECEIVER NXM / CONTROL BYTE +

                                    ;RECEIVER NXM / CONTROL BYTE
0|10|11010  0011000011000110    RNXMC  XFR     ,14,6   ;MOVE SILO OUT TO RICR REGISTER
0|10|11011  0101000000001101    GAMMA  S/C     3,5     ;SET RICR 12
0|10|11100  0101000000001001    BETA   S/C     3,1     ;SET RICR 14
0|10|11101  0101000000001000            S/C     3,0     ;SET RICR 15
0|10|11110  0101000000001111            S/C     3,7     ;CLEAR NXM
0|10|11111  1000000110110010            BRA     1,CNACB ;TEST FOR SURE TRUE, IF YES BRANCH TO CREATE NULL ACTION CONTROL BY

                                    ;RECEIVER NXM (WE GOT HERE FROM RECEIVED CHARACTER SILO SERVICE)
0|11|00000  0011000011000110    RNXM   XFR     ,14,6   ;MOVE SILO OUT TO RICR REGISTER
0|11|00001  0000000111011100            BRA     1,BETA  ;TEST FOR SURE TRUE, IF YES BRANCH TO RECEIVER NXM / CONTROL BYTE +

                                    ;NPR SILO OVERFLOW
0|11|00010  0101000000001010    NPRSO  S/C     3,2     ;SET SCR 10 INDICATING NPR SILO OVERFLOW
0|11|00011  0000000100000000            BRA     1,ILOOP ;TEST FOR SURE TRUE, IF YES BRANCH TO IDLE LOOP

                                    ;TRANSMIT SERVICE

                                    ;CHECK FOR BCC TRANSMISSION

0|11|00100  0010000000001110    TSERV  RAM     0,0,16  ;OBTAIN LINE PROTOCOL
0|11|00101  0011000010110001           XFR     ,13,1   ;MOVE RAM OUTPUT DATA TO A REGISTER
0|11|00110  0000100000011111           ALU     3/      ;LET ALU RESULT=A REGISTER
0|11|00111  1000101010010110           BRA     12,SBC1 ;TEST BIT 0 OF ALU RESULT, IF YES BRANCH TO SEND BCC 1
0|11|01000  1000101110100010           BRA     13,SBC2 ;TEST BIT 1 OF ALU RESULT, IF YES BRANCH TO SEND BCC 2
0|11|01001  0000011111100010           BRA     7,NPRSO ;TEST FOR NPR SILO NOT AVAILABLE, IF YES,BRANCH TO NPR SILO OVERFLO

                                    ;PRINCIPAL/ALTERNATE SELECTION

0|11|01010  0010000000001011           RAM     0,0,13  ;OBTAIN LINE STATE
0|11|01011  0111001011101101           BRB     2,SIGMA ;TEST BIT 02 OF RAM, IF YES, BRANCH TO HERE +2 (TESTING TRANSMIT GO
0|11|01100  1000000101100100           BRA     1,ITYPE ;TEST FOR SURE TRUE, IF YES BRANCH TO SELECT TYPE OF IDLING
0|11|01101  0111011111110010   SIGMA   BRB     7,USCA  ;TEST RAM OUTPUT 07, IF YES BRANCH TO USE ALTERNATE CA
0|11|01110  0010000000000001           RAM     0,0,1   ;OBTAIN PRINCIPAL BC (GE TEST)
0|11|01111  1111110001000000           BRB     14,XPBC0        ;TEST RAM OUTPUT 0-14=0, IF YES BRANCH TO XMIT PBCO
0|11|10000  0010000000000000           RAM     0,0,0   ;OBTAIN PRINCIPAL CURRENT ADDRESS
0|11|10001  0000000111110101           BRA     1,OXCB  ;TEST FOR SURE TRUE, IF YES BRANCH TO OBTAIN XMIT CONTROL BYTE

                                    ;USE ALTERNATE CA

0|11|10010  0010000000000011    USCA   RAM     0,0,3   ;OBTAIN ALTERNATE BC. (GE TEST)
0|11|10011  1111110001010000           BRB     14,XSBC0        ;TEST RAM OUTPUT 0-14=0, IF YES BRANCH TO XMIT SBCO
0|11|10100  0010000000000010           RAM     0,0,2   ;OBTAIN ALTERNATE CURRENT ADDRESS
                                    ;OBTAIN XMIT CONTROL BYTE
```



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0|11|10101  0011000010110011    OXCB   XFR     1,13,3  ;MOVE DATA FROM RAM OUTPUT TO NPR ADDRESS REGISTER
0|11|10110  0000200000000000           NPR             ;DO NPR TO GET CHARACTER
0|11|10111  0111100111110111   RBUS3  BRB     11,RBUS3        ;TEST REQUEST BUS, IF YES, BRANCH TO HERE
0|11|11000  1000011000110001           BRA     6,TNXMC ;TEST NXM, IF YES, BRANCH TO TRANSMIT NXM/CHARACTER
0|11|11001  1111101000110001           BRB     14,TMPEC        ;TEST MEM PAR ERR, IF YES, BRANCH TO TRANSMIT MPE/CHARACTER
0|11|11010  0011020010010001           XFR     ,11,1   ;MOVE DATA FROM DDC/DATI REGISTER TO A REGISTER
0|11|11011  0000100000011111           ALU     3/      ;LET ALU RESULT = A REGISTER
0|11|11100  0011000011110101           XFR     ,17,5   ;MOVE DATA FROM ALU RESULT TO DATO REGISTER (FOR BCC AND TRANSMITTER
0|11|11101  0010000000001010           RAM     0,0,12  ;OBTAIN TRANSMITTER DLE/LINE PROTOCOL II
0|11|11110  1111011010001100           BRB     6,DDCMX ;TEST RAM OUTPUT 06, IF YES BRANCH TO DDCMP XMIT (CALCULATE BCC)
0|11|11111  0010000000001102           RAM     0,0,14  ;OBTAIN MODE BITS
1|00|00000  0011000010100010   PI      XFR     ,12,2   ;MOVE RAM OUTPUT DATA TRANSLATED 0-2/8-10 TO B REGISTER
1|00|00001  0000100000010110           ALU     26      ;LET ALU RESULTS = A PLUS B
1|00|00010  0011000011110010           XFR     ,17,2   ;MOVE ALU RESULTS TO B REGISTER
1|00|00011  0210000200001040           RAM     0,0,10  ;OBTAIN CONTROL TABLE BASE ADDRESS
1|00|00100  3011000010110001           XFR     ,13,1   ;MOVE RAM OUTPUT TO A REGISTER
1|00|00101  0200100000010110           ALU     26      ;LET ALU RESULT = A PLUS B ((CHAR+MODE)+BASE ADDR)
1|00|00110  0011000011110011           XFR     1,17,3  ;MOVE ALU RESULTS TO NPR ADDRESS REGISTER
1|00|00111  0100000000000000           NPR             ;DO NPR TO GET CONTROL BYTE
1|00|01000  1111100100001000   RBUS4  BRB     11,RBUS4        ;TEST REQUEST BUS, IF YES, BRANCH TO HERE
1|00|01001  1030011000110001           BRA     6,TNXMC ;TEST NXM, IF YES, BRANCH TO TRANSMIT NXM/CONTROL BYTE
1|00|01010  1111101000111001           BRB     14,TMPEC        ;TEST MEM PAR ERR, IF YES, BRANCH TO TRANSMIT MPE/CONTROL BYTE
1|00|01011  0211000010010010           XFR     ,11,2   ;MOVE DATI REGISTER TO B REGISTER
1|00|01100  0001000000001101           ALU     5       ;LET ALU RESULT = B REGISTER
1|00|01101  1000101101110011           BRA     15,SDLE ;TEST BIT 1 OF ALU RESULT, IF YES BRANCH TO SEND DLE FIRST.
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                                    ;RETURN FROM DLE SENDING

1|00|01110  0010000101111100    RDLE   RAM     1,7,14  ;MOVE ALU RESULT TRANSLATED 5-7/0-2 TO RAM (AND WRITE NEW MODE B
1|00|01111  1000110010000010           BRA     14,SSBN ;TEST BIT 2 OF ALU RESULT, IF YES BRANCH TO SET SEND BCC NEXT

                                    ;RETURN FROM SSBCCNXT

1|00|10000  1000110110001111    RSSBN  BRA     15,XBCC ;TEST BIT 3 OF ALU RESULT, IF YES BRANCH TO CALCULATE TRANS BC

                                    ;RETURN FROM XMIT BCC

1|00|10001  1111100001101001    RXBCC  BRB     10,SIDLE        ;TEST FOR DNA FLAG, IF YES BRANCH TO SENT IDLE
1|00|10010  0011000011010000    ALPHA  XFR     ,15,0   ;MOVE DATO REGISTER TO TRANSMITTED DATA BUS
1|00|10011  0010000000001011           RAM     0,0,13  ;OBTAIN LINE STATE
1|00|10100  1111011100100011           BRB     7,USBC  ;TEST BIT 7 OF RAM OUTPUT, IF YES BRANCH TO USE ALTERNATE BC

                                    ;USE PRINCIPAL BC

1|00|10101  0010000000000001    UPBC   RAM     0,0,1   ;OBTAIN PRINCIPAL BYTE COUNT
1|00|10110  1111110001000000           BRB     14,XPBC0        ;TEST RAM 0-14=0
1|00|10111  0011000010110001           XFR     ,13,1   ;MOVE RAM OUTPUT TO A REGISTER
1|00|11000  0000100000011111           ALU     7/      ;LET ALU RESULTS = A PLUS 1
1|00|11001  0010000111110001           RAM     1,17,1  ;MOVE ALU RESULT TO RAM INPUT AND WRITE NEW PRINCIPAL BYTE COUNT
1|00|11010  1111111000010101           BRB     16,UPBC ;TEST FOR WRITE INHIBIT, IF YES BRANCH TO HERE -4
1|00|11011  0010000000000000   OPCA    RAM     0,0,2   ;OBTAIN PRINCIPAL CURRENT ADDRESS
1|00|11100  0011000010110001           XFR     ,13,1   ;MOVE RAM OUTPUT TO A REGISTER
1|00|11101  0000100000011111           ALU     77      ;LET ALU RESULT = A PLUS 1
1|00|11110  0010000111110002           RAM     1,17,0  ;MOVE ALU RESULT TO RAM INPUT AND WRITE NEW PRINCIPAL CURRENT ADDRES
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1Ø0011111  1111111000011011          BRB     1Ø,OPCA /TEST FOR WRITE INHIBIT, IF YES BRANCH TO HERE -4
1Ø0100000  0010000030000001          RAM     0,0,1   /OBTAIN PRINCIPAL BYTE COUNT
1Ø0100001  1111110001000000          BRB     14,XP8C0        /TEST RAM 0-14-0, IF YES, BRANCH TO XMIT P8C0
1Ø0100010  0000000100000000          BRA     1,ILOOP /TEST FOR SURE TRUE AND BRANCH TO IDLE LOOP

                                    /USE ALTERNATE BC

1Ø0100011  0010000000000011  USBC    RAM     0,0,3   /OBTAIN ALTERNATE BYTE COUNT
1Ø0100100  1111110001010000          BRB     14,XS8C0        /TEST RAM 0-14=0
1Ø0100101  0011000010110001          XFR     ,13,1   /MOVE RAM OUTPUT TO A REGISTER
1Ø0100110  0001000000111111          ALU     7/      /LET ALU RESULTS = A PLUS 1
1Ø0100111  0010000111110011          RAM     1,17,3  /MOVE ALU RESULT TO RAM INPUT AND WRITE NEW ALTERNATE BYTE COUNT
1Ø0101000  1111111000100011          BRB     1Ø,USBC /TEST FOR WRITE INHIBIT, IF YES BRANCH TO HERE -4
1Ø0101001  0010000000000010  OSCA    RAM     0,0,2   /OBTAIN ALTERNATE CURRENT ADDRESS
1Ø0101010  0011000010110001          XFR     ,13,1   /MOVE RAM OUTPUT TO A REGISTER
1Ø0101011  0001000000111111          ALU     7/      /LET ALU RESULT = A PLUS 1
1Ø0101100  0010000111110010          RAM     1,17,2  /MOVE ALU RESULT TO RAM INPUT AND WRITE NEW ALTERNATE CURRENT ADDRES
1Ø0101101  1111111000101001          BRB     1Ø,OSCA /TEST FOR WRITE INHIBIT, IF YES BRANCH TO HERE -4
1Ø0101110  0010000000000011          RAM     0,0,3   /OBTAIN ALTERNATE BYTE COUNT
1Ø0101111  1111110001010000          BRB     14,XS8C0        /TEST RAM 0-14-0, IF YES, BRANCH TO XMIT S8C0
1Ø0110000  0000000100000000          BRA     1,ILOOP /TEST FOR SURE TRUE, IF YES BRANCH TO IDLE LOOP

                                    /TRANSMIT NXM/CHARACTER  (CURRENT ADDRESS REGISTER ADDRESS IS IN RAM AR)

                                    /TRANSMIT NXM/CONTROL BYTE  (CONTROL TABLE BASE ADDRESS REGISTER ADDRESS IS IN R

1Ø0110001  0011000000000111  TNXMC   XFR     ,Ø,7    /MOVE  TO NPR STATUS REPORT REG.
1Ø0110010  0010000000001011  IOTA    RAM     0,0,13  /OBTAIN LINE STATE
1Ø0110011  0101000010000111          S/C     7,7     /SET RAM 04 (TRANSMITTER NXM)
1Ø0110100  0101000000001111          S/C     3,7     /CLEAR NXM
1Ø0110101  0101000000100010          S/C     5,2     /CLEAR RAM 02 (TRANSMITTER GO)
1Ø0110110  0010000110111011          RAM     1,13,13 /WRITE NEW LINE STATE
1Ø0110111  1111111000110010          BRB     1Ø,IOTA /TEST FOR WRITE INHIBIT, IF YES BRANCH TO IOTA
1Ø0111000  0000000100000000          BRA     1,ILOOP /TEST FOR SURE TRUE, IF YES BRANCH TO IDLE LOOP

                                    /TRANSMIT MPE/CHARACTER   (CURRENT ADDRESS REGISTER ADDRESS IS IN RAM AR)

                                    /TRANSMIT MPE/CONTROL BYTE  (CONTROL TABLE BASE ADDRESS REGISTER ADDRESS IS IN R

1Ø0111001  0011000000000111  TMPEC   XFR     ,Ø,7    /MOV.  TO NPR STATUS REPORT REG.
1Ø0111010  0010000000001011  OMEGA   RAM     0,0,13  /OBTAIN LINE STATE
1Ø0111011  0101000010000101          S/C     7,5     /SET RAM 05 (TRANSMIT MPE)
1Ø0111100  0101000000100010          S/C     5,2     /CLEAR RAM 02 (TRANSMITTER GO)
1Ø0111101  0010000110111011          RAM     1,13,13 /WRITE NEW LINE STATE
1Ø0111110  1111111000111010          BRB     1Ø,OMEGA        /TEST FOR WRITE INHIBIT, IF YES BRANCH TO HERE -4
1Ø0111111  0000000100000000          BRA     1,ILOOP /TEST FOR SURE TRUE, IF YES, BRANCH TO IDLE LOOP

                                    /XMIT P8C0

1Ø1000000  0010000000001011  XP8C0   RAM     0,0,13  /OBTAIN LINE STATE
1Ø1000001  0101000010000100          S/C     7,4     /SET RAM OUTPUT BIT 7 (GO TO ALTERNATE)
1Ø1000010  0010000110111011          RAM     1,13,13 /MOVE RAM OUTPUT TO RAM (AND WRITE NEW LINE STATE)
1Ø1000011  1111111001000000          BRB     1Ø,XP8C0        /TEST FOR WRITE INHIBT, IF YES BRANCH TO HERE -3
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1Ø1000100  0010000000000001          RAM     0,0,1   /OBTAIN PRINCIPAL BYTE COUNT
1Ø1000101  0[illegible]0000000111          XFR     ,Ø,7    /MAKE NPR SILO ENTRY
1Ø1000110  1[illegible]101101001000          BRB     15,RED  /TEST RAM OUTPUT BIT 15, IF YES BRANCH TO HERE +2
1Ø1000111  1000000101010111          BRA     1,C8C0  /TEST FOR SURE TRUE, IF YES BRANCH TO CHECK FOR BOTH BC=0
1Ø1001000  0010000100000001  RED     RAM     1,0,1   /ZERO PRINCIPAL BYTE COUNT
1Ø1001001  0010000000001110  OTM8    RAM     0,0,16  /OBTAIN  LINE PROTOCOL
1Ø1001010  0011000010110010          XFR     ,13,2   /MOVE RAM OUTPUT TO REGISTER 8
1Ø1001011  0011000010000010          XFR     ,10,2   /MOVE REGISTER 88-15 TO REGISTER 8 0-7
1Ø1001100  0000100000000101          ALU     5       /LET ALU RESULT = 8
1Ø1001101  0010000101111100          RAM     1,7,14  /MOVE ALU RESULTS TRANSLATED  TO RAM AND WRITE NEW MODE BITS
1Ø1001110  1000110010000111          BRA     14,8C0SB        /TEST  ALU RESULT 02, IF YES BRANCH TO 8C0 SEND 8CC
1Ø1001111  1000000101010111          BRA     1,C8C0  /TEST FOR SURE TRUE, IF YES BRANCH TO CHECK FOR BOTH BC=0

                                    /XMIT S8C0

1Ø1010000  0010000000001011  XS8C0   RAM     0,0,13  /OBTAIN LINE STATE
1Ø1010001  0101000010000000          S/C     7,0     /CLEAR RAM OUTPUT BIT 7 (GO TO PRINCIPAL)
1Ø1010010  0010000110111011          RAM     1,13,13 /MOVE RAM OUTPUT TO RAM (AND WRITE NEW LINE STATE)
1Ø1010011  1111111001010000          BRB     1Ø,XS8C0        /TEST FOR WRITE INHIBIT, IF YES BRANCH TO HERE -3
1Ø1010100  0010000000000011          RAM     0,0,3   /OBTAIN ALTERNATE BYTE COUNT
1Ø1010101  0011000000000111          XFR     ,Ø,7    /MAKE NPR SILO ENTRY
1Ø1010110  1111101101011101          BRB     15,ESS  /TEST RAM OUTPUT 15, IF YES, BRANCH TO CLEAR ALTERNATE BYTE COUNT

                                    /CHECK FOR BOTH BC=0

1Ø1011000  0010000000000001  C8C0    RAM     0,0,1   /OBTAIN PRINCIPAL BYTE COUNT
1Ø1011001  1111110001011010          BRB     14,DELTA        /TEST RAM OUTPUT 0-14-0, IF YES, BRANCH TO HERE +2
1Ø1011010  0010000000000011          BRA     1,ILOOP /TEST FOR SURE TRUE, IF YES, BRANCH TO IDLE LOOP
1Ø1011011  1111110001011111  DELTA   RAM     0,0,3   /OBTAIN ALTERNATE BYTE COUNT
1Ø1011100  0000000100000000          BRB     14,C/GO /TEST RAM OUTPUT 0-14-0, IF YES, BRANCH TO CLEAR GO
                                    BRA     1,ILOOP /TEST FOR SURE TRUE, IF YES BRANCH TO IDLE LOOP

                                    /CLEAR ALTERNATE BYTE COUNT

1Ø1011101  0010000100000011  ESS     RAM     1,0,3   /ZERO ALTERNATE BYTE COUNT
1Ø1011110  1000000101001001          BRA     1,OTM8  /TEST FOR SURE TRUE, BRANCH TO OTM8

                                    /CLEAR GO

1Ø1011111  0010000000001011  C/GO    RAM     0,0,13  /OBTAIN LINE STATE
1Ø1100000  0101000000100010          S/C     5,2     /CLEAR RAM 02 (TRANSMITTER GO)
1Ø1100001  0010000110111011          RAM     1,13,13 /WRITE NEW LINE STATE
1Ø1100010  1111111001011111          BRB     1Ø,C/GO /TEST FOR WRITE INHIBIT, IF YES BRANCH TO HERE -3
1Ø1100011  0000000100000000          BRA     1,ILOOP /TEST FOR SURE TRUE, IF YES BRANCH TO IDLE LOOP

                                    /SELECT TYPE OF IDLE

1Ø1100100  0010000000001010  ITYPE   RAM     0,0,12  /OBTAIN TRANSMITTER DLE/PROTOCOL II
1Ø1100101  1111000001100111          BRB     0,BC0CG /TEST RAM OUTPUT 00, IF YES BRANCH TO BC0CG
1Ø1100110  0000000100000000          BRA     1,ILOOP /TEST FOR SURE TRUE, IF YES BRANCH TO IDLE LOOP
1Ø1100111  0101000001000101  BC0CG   S/C     6,5     /SET TMARK
1Ø1101000  0C0000010000000Ø          BRA     1,ILOOP /TEST FOR SURE TRUE, IF YES BRANCH TO IDLE LOOP

                                    /SENT IDLE  (LINE STATE IS IN RAM OUTPUT)

1Ø1101001  0010000000001011  SIDLE   RAM     0,0,13  /OBTAIN LINE STATE
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1Ø1101010  0101000000100100          S/C     5,4      ;SET RAM 03 (TRANSMITTER UNDERRUN)
1Ø1101011  0010000110111011          RAM     1,13,13 ;MOVE RAM OUTPUT TO RAM (AND WRITE NEW LINE STATE)
1Ø1101100  1111111001101001          BRB     16,SIDLE        ;TEST FOR WRITE INHIBIT, IF YES BRANCH TO HERE -3
1Ø1101101  1000000100010010          BRA     1,ALPHA ;TEST FOR SURE TRUE, IF YES, BRANCH TO RETURN FROM XMIT BCC +3

                                     ;SENT IDLE/DLE

1Ø1101110  0010000000001011  MU     RAM     0,0,13  ;OBTAIN LINE STATE
1Ø1101111  0101000000100100          S/C     5,4     ;SET 03 (UNDERRUN)
1Ø1110000  0010000110111011          RAM     1,13,13 ;WRITE LINE STATE
1Ø1110001  1111111001101110          BRB     16,MU   ;TEST FOR INHIBIT
1Ø1110010  1000000101111011          BRA     1,NU    ;GO BACK TO SEND IDLE

                                     ;SEND DLE FIRST

                                     ;(WE GOT HERE FROM TRANSMIT SERVICE.  THE CONTROL BYTE IS
                                     ;IN ALU RESULT AND B REGISTER.  MASTER SCAN POSITION IS IN
                                     ;RAM ADDRESS REGISTER 0-5).

1Ø1110011  0010000000001110  SDLE   RAM     0,0,16  ;OBTAIN LINE PROTOCOL
1Ø1110100  1111001001111101          BRB     2,CRAM2 ;TEST RAM OUTPUT 02, IF YES BRANCH TO CLEAR RAM 02
1Ø1110101  0101000000100110          S/C     5,6     ;SET RAM 02
1Ø1110110  0010000110111110          RAM     1,13,16 ;MOVE RAM OUTPUT TO RAM INPUT AND WRITE NEW LINE PROTOCOL
1Ø1110111  1111111001110011          BRB     16,SDLE ;TEST FOR WRITE INHIBIT, IF YES BRANCH BACK
1Ø1111000  0010000000001010          RAM     0,0,12  ;OBTAIN TRANSMITTER DLE / LINE PROTOCOL II
1Ø1111001  0011000010110010          XFR     ,13,2   ;MOVE RAM OUTPUT TO REGISTER B
1Ø1111010  1111100001101110          BRB     16,MU   ;TEST FOR DNA FLAG, IF YES BRANCH TO SENT IDLE/DLE
1Ø1111011  0011000010000000  NU     XFR     ,10,0   ;MOVE REGISTER B 15-8 TRANSMITTED DATA BUS
1Ø1111100  0000000100000000          BRA     1,ILOOP ;TEST FOR SURE TRUE, IF YES BRANCH TO IDLE LOOP

                                     ;CLEAR RAM 02 (RAM 02 IS DLE SENDING IN PROGRESS)

1Ø1111101  0010000000001110  CRAM2  RAM     0,0,16  ;OBTAIN LINE PROTOCOL
1Ø1111110  0101000000100010          S/C     5,2     ;CLEAR RAM OUTPUT 02
1Ø1111111  0010000110111110          RAM     1,13,16 ;MOVE RAM OUTPUT TO RAM INPUT DATA AND WRITE NEW LINE PROTOCOL
11Ø0000000 1111111001111101          BRB     16,CRAM2        ;TEST FOR WRITE INHIBIT, IF YES BRANCH BACK
11Ø0000001 1000000100001110          BRA     1,RDLE  ;TEST FOR SURE TRUE, IF YES BRANCH TO RETURN FROM DLE SENDING

                                     ;SET SEND BCC NEXT

11Ø0000010  0010000000001110  SSBN   RAM     0,0,16  ;OBTAIN LINE PROTOCOL
11Ø0000011  0101000000100111          S/C     5,7     ;SET RAM OUTPUT BIT 0
11Ø0000100  0010000110111110          RAM     1,13,16 ;MOVE RAM OUTPUT TO RAM INPUT AND WRITE NEW LINE PROTOCOL
11Ø0000101  1111111010000010          BRB     16,SSBN ;TEST FOR WRITE INHIBIT, IF YES BRANCH BACK
11Ø0000110  1000000100010000          BRA     1,RSSBN ;TEST FOR SURE TRUE, IF YES BRANCH TO RETURN FROM SSBCCNXT-

                                     ;BC0 SEND BCC

11Ø0000111  0010000000001110  BC0SB  RAM     0,0,16  ;OBTAIN LINE PROTOCOL
11Ø0001000  0101000000100111          S/C     5,7     ;SET RAM OUTPUT BIT 0
11Ø0001001  0010000110111110          RAM     1,13,16 ;MOVE RAM OUTPUT TO RAM INPUT AND WRITE NEW LINE PROTOCOL
11Ø0001010  1111111010000111          BRB     16,BC0SB        ;TEST FOR WRITE INHIBIT, IF YES BRANCH BACK
11Ø0001011  1000000101010111          BRA     1,CBC0  ;TEST FOR SURE TRUE, IF YES BRANCH TO CBC0
```



```
                                     ;DDCMP TRANSMIT

11Ø0001100  [illegible]0000002011Ø0  DDCMX  RAM     0,0,14  ;OBTAIN TRANSMITTER MODE BITS
11Ø0001101  1111110010001111          BRB     14,XBCC ;TEST RAM 0-14=0, IF YES BRANCH TO XBCC
11Ø0001110  1000000100000003          BRA     1,PI    ;TEST FOR SURE TRUE, IF YES BRANCH TO PI

                                     ;CALCULATE TRANSMITTER BCC

11Ø0001111  2011000011010001  XBCC   XFR     ,15,1   ;MOVE DATO REGISTER TO A REGISTER
11Ø0010000  0010000200000110          RAM     0,0,6   ;OBTAIN TRANSMITTER BCC CALCULATED TO DATE
11Ø0010001  0011000010110010          XFR     ,13,2   ;MOVE RAM DATA TO REGISTER B
11Ø0010010  ~0130000000001010         RAM     0,0,12  ;OBTAIN TRANSMITTER DLE/LINE PROTOCOL II
11Ø0010011  0110000000000000          BCC             ;PERFORM SPECIFIED BCC CALCULATION
11Ø0010100  0010000111100110          RAM     1,16,6  ;MOVE BCC TO RAM INPUT AND WRITE NEW TRANSMITTER BCC
11Ø0010101  1000000100010001          BRA     1,RXBCC ;TEST FOR SURE TRUE, IF YES, BRANCH TO RETURN FROM XMIT BCC

                                     ;SEND BCC 1

                                     ;(WE GOT HERE FROM TRANSMIT SERVICE.  THE MASTER SCAN POSITION
                                     ;IS IN THE RAM ADDRESS REGISTER 0-3.  THE LINE PROTOCOL IS IN
                                     ;THE A REGISTER AND THE ALU RESULT REGISTER.)

11Ø0010110  0010000000001110  SBC1   RAM     0,0,16  ;OBTAIN LINE PROTOCOL
11Ø0010111  0011000010110001          XFR     ,13,1   ;MOVE RAM OUTPUT TO A REGISTER
11Ø0011000  0001000000111111          ALU     7/      ;LET ALU RESULT = A PLUS 1
11Ø0011001  0010000111111110          RAM     1,17,16 ;MOVE ALU RESULT TO RAM INPUT DATA AND WRITE NEW LINE PROTOCOL
11Ø0011010  1111111010010110          BRB     16,SBC1 ;TEST FOR WRITE INHIBIT, IF YES BRANCH BACK
11Ø0011011  0010000000000110          RAM     0,0,6   ;OBTAIN TRANSMITTER BCC
11Ø0011100  0011000010110000          XFR     ,13,0   ;MOVE RAM OUTPUT DATA TO TRANSMITTED DATA BUS (HIGH ORDER BITS GO INT
11Ø0011101  0010000000001010          RAM     0,0,12  ;OBTAIN TRANSMITTER DLE/LINE PROTOCOL II (TO LOOK FOR LRC)
11Ø0011110  1111001110100001          BRB     3,GOIDL ;TEST RAM OUTPUT 03, IF YES BRANCH TO HERE +4
11Ø0011111  1111010010100001          BRB     4,GOIDL ;TEST RAM OUTPUT 04, IF YES BRANCH TO HERE +3
11Ø0100000  1000000110100101          BRA     1,C/LU1 ;TEST FOR SURE TRUE, IF YES BRANCH TO SEND BCC 2 + 6
11Ø0100001  0000000100000000  GOIDL  BRA     1,ILOOP ;TEST FOR SURE TRUE, IF YES BRANCH TO IDLE LOOP

                                     ;SEND BCC2

                                     ;(WE GOT HERE FROM TRANSMIT SERVICE.  THE MASTER SCAN POSITION
                                     ;IS IN THE RAM ADDRESS REGISTER 0-3.  THE LINE PROTOCOL IS IN
                                     ;THE A REGISTER AND IN THE ALU RESULT REGISTER.)

11Ø0100010  0010000000000110  SBC2   RAM     0,0,6   ;OBTAIN TRANSMITTER BCC
11Ø0100011  0011000010110010          XFR     ,13,2   ;MOVE RAM OUTPUT DATA TO REGISTER B
11Ø0100100  0011000010000000          XFR     ,10,0   ;MOVE REGISTER B 8-15/0-7 TO TRANSMITTED DATA BUS

11Ø0100101  0010000100000110  C/LU1  RAM     1,0,6   ;MOVE ZERO TO RAM INPUT DATA AND WRITE ZERO TRANSMITTER BCC
11Ø0100110  0010000000001110          RAM     0,0,16  ;OBTAIN LINE PROTOCOL
11Ø0100111  0101000000100001          S/C     5,1     ;CLEAR RAM BIT 01 (SEND BCC 2)
11Ø0101000  0010000110111110          RAM     1,13,16 ;MOVE RAM INPUT TO RAM INPUT DATA AND WRITE NEW LINE PROTOCOL
11Ø0101001  1111111010100101          BRB     16,C/LU1        ;TEST FOR WRITE INHIBIT, IF YES BRANCH BACK
11Ø0101010  0000000100000000          BRA     1,ILOOP ;TEST FOR SURE TRUE, IF YES BRANCH TO IDLE LOOP
```

```
                                        ;RECEIVED ERRORS

                                        ;CONTROL BYTE INTERRUPT

1 1 0 1 0 1 0 1 1   0 0 1 0 0 0 0 0 0 0 0 0 0 1 1 1 1   CBINT  RAM     0,0,17  ;READ CONTROL BYTE HOLDING REGISTER
1 1 0 1 0 1 1 0 0   0 1 0 1 0 0 0 0 0 0 0 1 0 0 0 1 1           S/C     5,3     ;CLEAR RAM 00 (GENERATE INTERRUPT)
1 1 0 1 0 1 1 0 1   0 0 1 0 0 0 0 0 1 1 0 1 1 1 1 1 1           RAM     1,13,17 ;WRITE CONTROL BYTE HOLDING REGISTER
1 1 0 1 0 1 1 1 0   0 0 1 1 0 0 0 0 0 1 1 0 0 0 1 1 0           XFR     ,14,6   ;MOVE SILO OUT TO RICR REGISTER
1 1 0 1 0 1 1 1 1   0 1 0 1 0 0 0 0 0 0 0 0 1 0 1 1 1           S/C     3,3     ;SET SCR07 (RECEIVER INTERRUPT)
1 1 0 1 1 0 0 0 0   0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0           BRA     1,ILOOP ;TEST FOR SURE TRUE, IF YES BRANCH TO IDLE LOOP

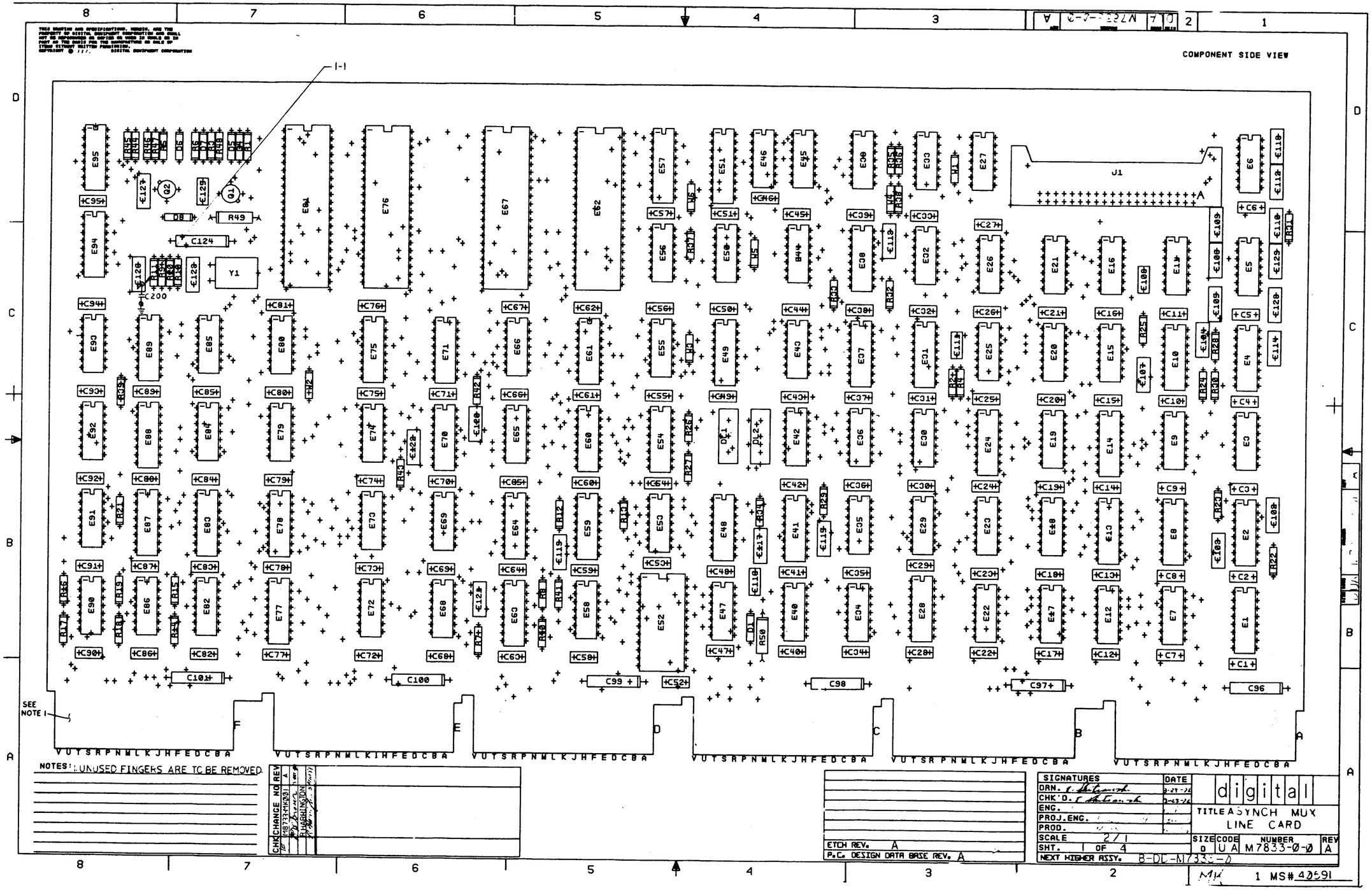
                                        ;PARITY AND OVERRUN ERRORS

1 1 0 1 1 0 0 0 1   0 0 1 1 0 0 0 0 1 1 0 0 0 1 1 1 0   POER   XFR     ,14,6   ;MOVE SILO OUT TO RICR REGISTER

                                        ;CREATE NULL ACTION CONTROL BYTE (MODE IS PRESERVED)

1 1 0 1 1 0 0 1 0   0 0 1 0 0 0 0 0 0 0 0 0 0 1 1 1 1   CNACB  RAM     0,0,17  ;READ CONTROL BYTE HOLDING REGISTER
1 1 0 1 1 0 0 1 1   0 1 0 1 0 0 0 0 0 0 0 1 0 0 0 1 1           S/C     5,3     ;CLEAR RAM 00
1 1 0 1 1 0 1 0 0   0 1 0 1 0 0 0 0 0 0 0 1 0 0 0 0 1           S/C     5,1     ;CLEAR RAM 01
1 1 0 1 1 0 1 0 1   0 1 0 1 0 0 0 0 0 0 0 1 0 0 0 1 0           S/C     5,2     ;CLEAR RAM 02
1 1 0 1 1 0 1 1 0   0 1 0 1 0 0 0 0 0 0 0 1 0 0 0 0 0           S/C     5,0     ;CLEAR RAM 03
1 1 0 1 1 0 1 1 1   0 1 0 1 0 0 0 0 0 0 0 0 0 0 1 1 1           S/C     7,7     ;SET RAM OUTPUT 04 (DISCARD)
1 1 0 1 1 1 0 0 0   0 0 1 0 0 0 0 1 1 0 1 1 1 1 1 1 1           RAM     1,13,17 ;WRITE CONTROL BYTE HOLDING REGISTER FROM RAM OUTPUT
1 1 0 1 1 1 0 0 1   0 1 0 1 0 0 0 0 0 0 0 0 0 1 0 1 1           S/C     3,3     ;SET SCR 07 (RECEIVER INTERRUPT)
1 1 0 1 1 1 0 1 0   0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0           BRA     1,ILOOP ;TEST FOR SURE TRUE, IF YES BRANCH TO IDLE LOOP

                                        ;END
```


COMPONENT SIDE VIEW
I-I
J1
SEE NOTE 1
NOTES: 1. UNUSED FINGERS ARE TO BE REMOVED.
CHK CHANGE NO REV
M8733-MK001 A
R. HARRINGTON
ETCH REV. A
P.C. DESIGN DATA BASE REV. A
SIGNATURES
DATE
DRN.
CHK'D.
ENG.
PROJ.ENG.
PROD.
SCALE 2/1
SHT. 1 OF 4
NEXT HIGHER ASSY. B-DD-M7333-0
digital
TITLE ASYNCH MUX LINE CARD
SIZE D
CODE U A
NUMBER M7833-0-0
REV A
1 MS# 40591

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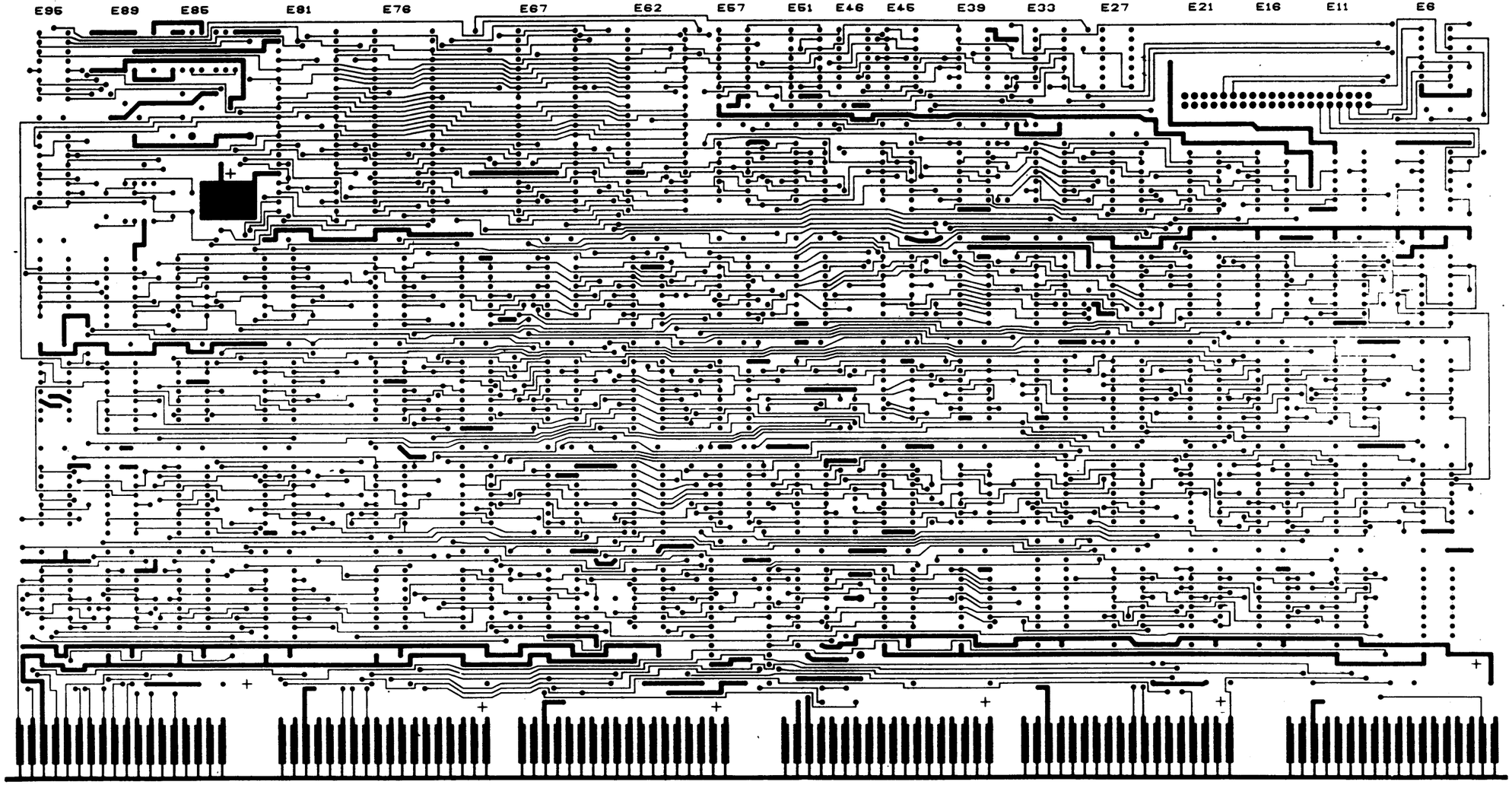
CS*ABCDEFHJKLMNPRS

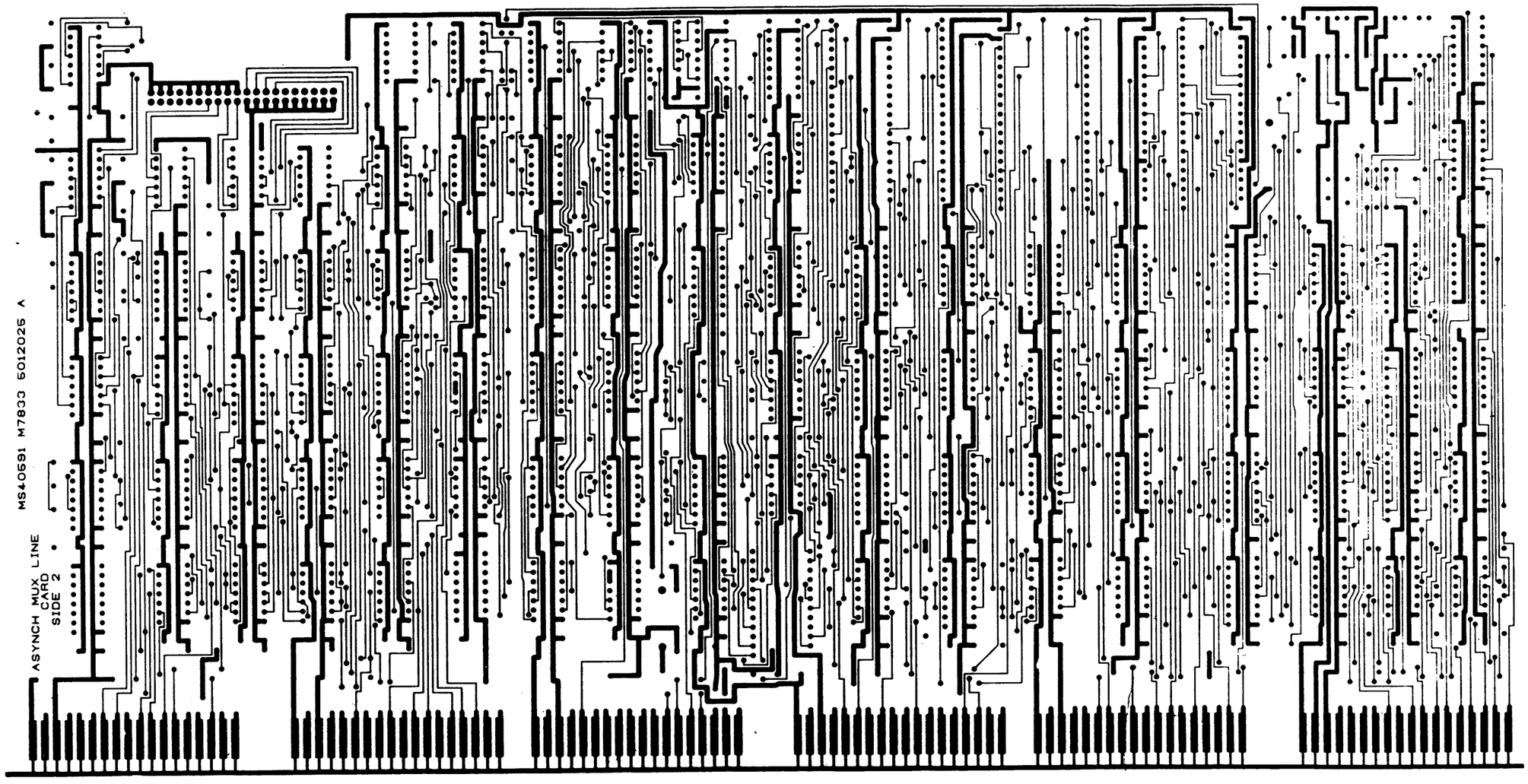
SIDE 1

digital

E96 E89 E85 E81 E76 E67 E62 E57 E51 E46 E45 E39 E33 E27 E21 E16 E11 E6



| REV | | |



REVISIONS		
CHK	CHANGE NO	REV

TITLE: ASYNCH MUX LINE CARD DUA M7833-0-0 A

SCALE 2/1 SHEET 3 OF 4

DUA M7833-0-0 A

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REWORK INSTRUCTIONS

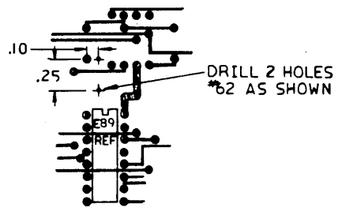

FIG 1
COMPONENT SIDE VIEW
SCALE-NONE

ECO* M7833-MK00J

1-1 DRILL TWO HOLES #62 AS SHOWN IN FIGURE 1. INSERT C200 IN HOLES. BEND AND SOLDER TOP LEAD TO ETCH CONNECTING C126 TO R11. BEND AND SOLDER BOTTOM LEAD TO GROUND ETCH FROM E89 PIN 8, AS SHOWN IN FIGURE 2.

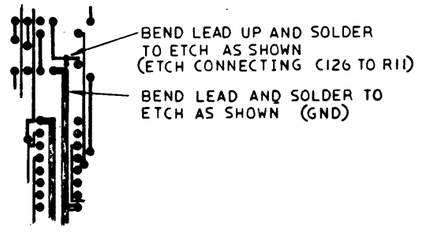

FIG. 2
SOLDER SIDE VIEW
SCALE - NONE

REVISIONS

CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
ASYNCH MUX LINE CARD	D	UA	M7833-0-0	A
SCALE NONE SHEET 4 OF 4	DIST.			

MK

AUTOMATED BY PRTLST.3P(44)

PARTS LIST

LINE	ITEM	DOCUMENT NUMBER	PART NUMBER	DESCRIPTION	QTY PER VARIATION 00	REFERENCE DESIGNATOR
1	1	D-MD-5012025-0-0	5012025-00	M7833-ETCH BD	1	
2	2		1002427-00	15.0 MMF 100V 5%200PPM MICA	2	C115,C122
3	3		1005820-00	22.0 MMF 100V 5%200PPM MICA	3	C123,C126,C200
4	4		1001739-00	27.0 MMF 100V 5%200PPM MICA	5	C102,C103,C104,C107,C121
5	5		1000012-00	56.0 MMF 100V 5%200PPM MICA	1	C120
6	6		1000006-00	10.0 MMF 100V 5%200PPM MICA	1	C114
7	7		1000019-00	150.0 MMF 100V 5%200PPM MICA	1	C113
8	8		1000020-00	180.0 MMF 100V 5%200PPM MICA	1	C117
9	9		1000024-00	470.0 MMF 100V 5%200PPM MICA	8	C105,C106,C109,C110,C112,C118,
					CONT	C128,C129
10	10		1000042-00	1000.0 MMF 100V 5%200PPM MICA	1	C127
11	11		1001610-01	.01 MFD50/100V +80-20% DISC	99	C1-C95,C111,C125,C108,C116
12	12		1005306-00	6.8MFD 35V 10% S.TANT	7	C96-C101,C124
13	13		1000016-00	100.0 MMF 100V 5%200PPM MICA	1	C119
14	14		1102808-00	1N 752A VZ= 5.6 5% .40W	1	D8
15	15		1105275-00	D 672 TR= 15NS PIV= 60V SI	4	D4-D7
16	16		1110836-00	1N 759A VZ= 12.0 5% .40W	1	D1
17	17		1209941-02	HEADER 100 40POS RT ANGLE	1	J1
18	18		1216988-02	HANDLE,MODULE,HEX TWO EJECTORS	1	
19	19		1301317-00	10.0 .25 W 5.0 % CC	4	R44-R47
20	20		1300271-00	220.0 .25 W 5.0 % CC	1	R48
21	21		1300295-00	330.0 .25 W 5.0 % CC	2	R1,R2
22	22		1300309-00	390.0 .25 W 5.0 % CC	2	R26,R39
23	23		1300316-00	470.0 .25 W 5.0 % CC	2	R27,R40
24	24		1300315-00	470.0 .50 W 5.0 % CC	1	R49
25	25		1301401-00	750.0 .25 W 5.0 % CC	2	R3,R4
26	26		1300365-00	1.0 K .25 W 5.0 % CC	18	R5,R6,R11-R21,R31,R35-R38
27	27		1300479-00	10.0 K .25 W 5.0 % CC	17	R7-R10,R22-R25,R28-R30,R32-R34,
					CONT	R41-R43
28	28		1302336-00	39.0 .50 W 5.0 % CC	1	R50

REVISION HISTORY			BASIC PART NO: M7833
ENG	ECO NUMBER	REV	SECTION A OF A
R4	M8733-MK001	A	SECTION.VARIATION INDEX [A] 00 [B] [C] [D] [E] [F] [H] [J] [K] [L] [M] [N]

DRN: B.FRASER	DATE: 15-DEC-80	D I G I T A L
CHK'D: J.FALKOWSKI	DATE: 15-DEC-80	TITLE: PARTS LIST ASYN MUX LINE CARD
DES.ENG: W.SMITH	DATE: 15-DEC-80	
RESP.ENG.: R.HARRINGTON (R. Harrington 6 MAR 81)	DATE: 15-DEC-80	DOCUMENT NUMBER
MFG.ENG.: R.WALL	DATE: 15-DEC-80	SIZE: K / CODE: PL / NUMBER: M7833-0-0 / REV: A
ASSEMBLY NUMBER: D-UA-M7833-0-0	TOP DOCUMENT NUMBER: #B-DD-M7833-0	FILE NAME: MK0296.PLS / EDIT #: 3

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AUTOMATED BY PRTLST.3P(44) — P A R T S L I S T — SHEET A2 OF A2

LINE	ITEM	DOCUMENT NUMBER	PART NUMBER	DESCRIPTION	QTY PER VARIATION 00	REFERENCE DESIGNATOR
29	29		1501742-00	DEC2904 PNP 600MW SI 40 40 P	1	Q1
30	30		1503409-00	DEC6534D PNP 310MW SI 40 90	1	Q2
31	31		1605528-00	DELAY= 30NS,0TAPS DL5184	2	DL1,DL2
32	32		1811660-02	OSCILLATOR, XTAL 5.0688 MHZ	1	E27
33	33		1812396-00	XTAL 2.4576 MHZ	1	Y1
34	34		1909701-00	74154 1 OF 16,BINA	1	E52
35	35		1910436-00	DEC 74123 ONE SHOT-DUAL,RETRIG	8	E2,E4,E10,E38,E41,E59,E63,E70
36	36		1905575-00	7400 NAND GATE-QUAD 2IN	1	E68
37	37		1909686-00	7404 INVERTER GATE-HEX 1I	7	E7,E47,E53,E58,E66,E73,E80
38	38		1910091-00	DEC 7437 AND GATE-QUAD 2IN,BU	3	E12,E40,E46
39	39		1910651-00	DEC 74175 FF-D QUAD	6	E8,E13,E14,E24,E49,E88
40	40		1905547-00	7474 FF-D DUAL,EDGE TRIGG	13	E15,E23,E25,E26,E29,E34-E36,E44,
					CONT	E45,E55,E74,E84
41	41		1909937-00	74153 MUX 1 OF 4 (DUAL)	4	E37,E71,E75,E83
42	42		1910656-00	74155 DECODER-2 OF 4(DUAL)	4	E31,E60,E61,E89
43	43		1911521-00	7432 OR GATE-QUAD 2IN, PO	3	E3,E22,E72.
44	44		1909705-00	DEC 8881 NAND GATE-QUAD 2IN O	4	E82,E86,E90,E91
45	45		2112623-00	DUAL BAUD RATE GEN/PROG DIVIDER,	2	E51,E57
46	46		1905577-00	7420 NAND GATE-DUAL 4INPU	1	E39
47	47		1910390-00	DEC 7380 NOR GATE-QUAD 2IN,FA	1	E93
48	48		1910837-00	8093 BUFFER CATE-QUAD 2IN	2	E18,E50
49	49		1912666-00	BUFFER GATE-QUAD 2IN	2	E17,E56
50	50		1909054-00	7493 COUNTER,ASYNCH UP,BI	1	E92
51	51		1910655-00	74157 MUX 2 TO 1 QUAD	1	E64
52	52		1909267-00	DEC 74H11 AND GATE-TRIPLE 3INP	2	E33,E69
53	53		1910738-00	DEC 74170 MEMORY READ/WRITE	5	E54,E77,E78,E94,E95
54	54		1910155-00	DEC 7408 AND GATE,POS.QUAD 2I	7	E9,E19,E20,E30,E32,E42,E85
55	55		1910454-00	DEC 9318 ENCODER, 8 INPUT PRI	2	E48,E87
56	56		1910322-00	DEC 1488L DRIVER,LINE,QUAD,EI	2	E11,E16
57	57		1909004-00	DEC 7402 NOR GATE-QUAD 2IN	2	E21,E43
58	58		1910323-00	DEC 1489L RECEIVER,LINE,QUAD,	2	E5,E6
59	59		1909713-00	DEC 8815 NOR GATE-DUAL 4IN	2	E65,E79
60	60		2111450-00	UART 40K BAUD VARIATION OF 19-10	4	E62,E67,E76,E81
61	61		9008351-00	CAP,TRANSISTOR .320 ID	1	
62	62		9009185-00	JUMPER, WIRE, INSULATED, BLACK B	6	W1-W6
63	63		9000024-01	EYELET, ROLLED FLANGE, .121 OD X	12	

D	I	G	I	T	A	L	TITLE	SECTION A OF A
							ASYN MUX LINE CARD	

SIZE	CODE	DOCUMENT NUMBER	REV
K	PL	M7833-0-0	A

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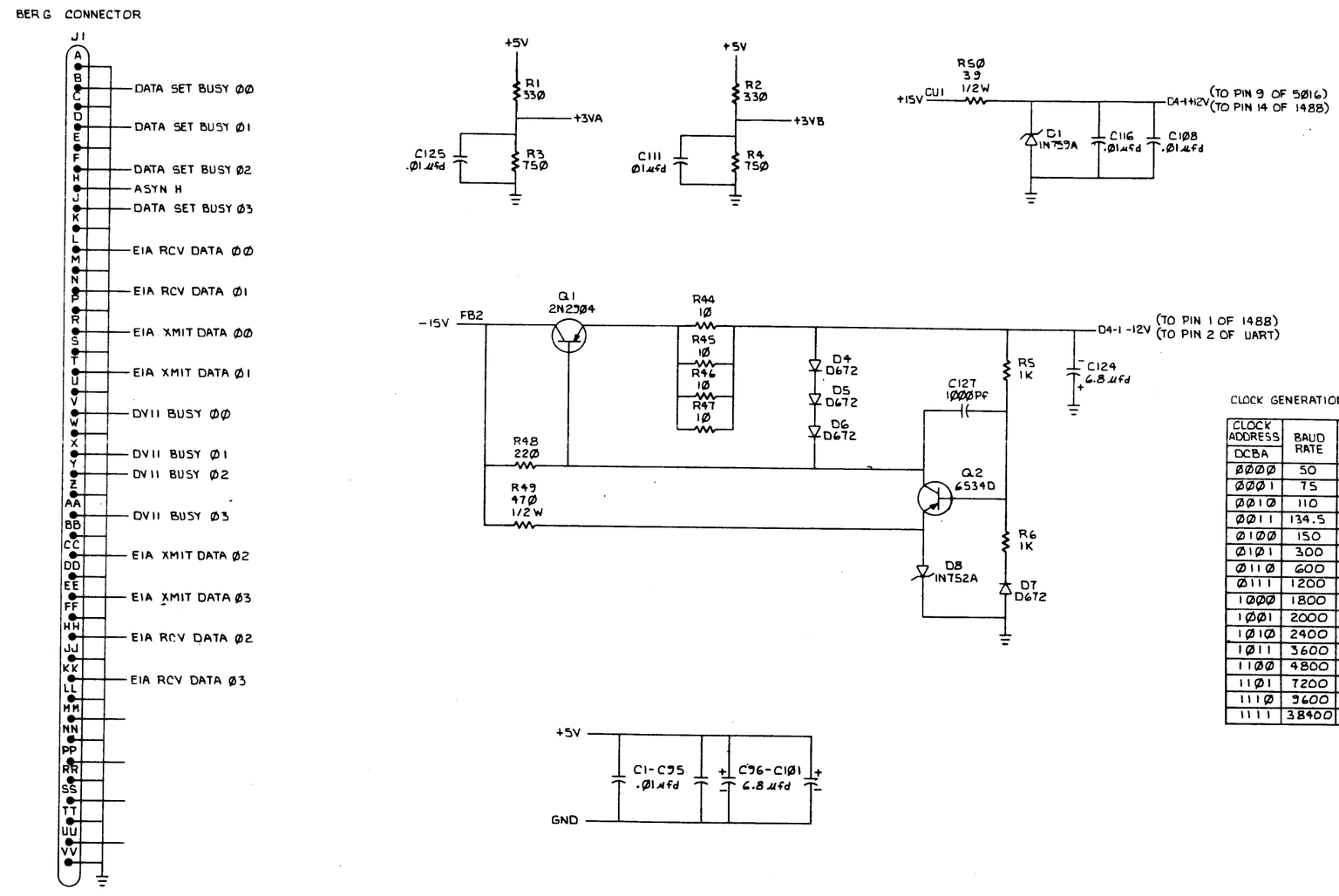


CLOCK GENERATION CHART

CLOCK ADDRESS DCBA	BAUD RATE	PERIOD (USEC)
ØØØØ	50	1250.00
ØØØ1	75	833.33
ØØ1Ø	110	568.18
ØØ11	134.5	464.68
Ø1ØØ	150	416.67
Ø1Ø1	300	208.33
Ø11Ø	600	104.17
Ø111	1200	52.08
1ØØØ	1800	34.72
1ØØ1	2000	31.25
1Ø1Ø	2400	26.04
1Ø11	3600	17.36
11ØØ	4800	13.02
11Ø1	7200	8.68
111Ø	9600	6.51
1111	38400	1.63

(CHART, REGULATORS)

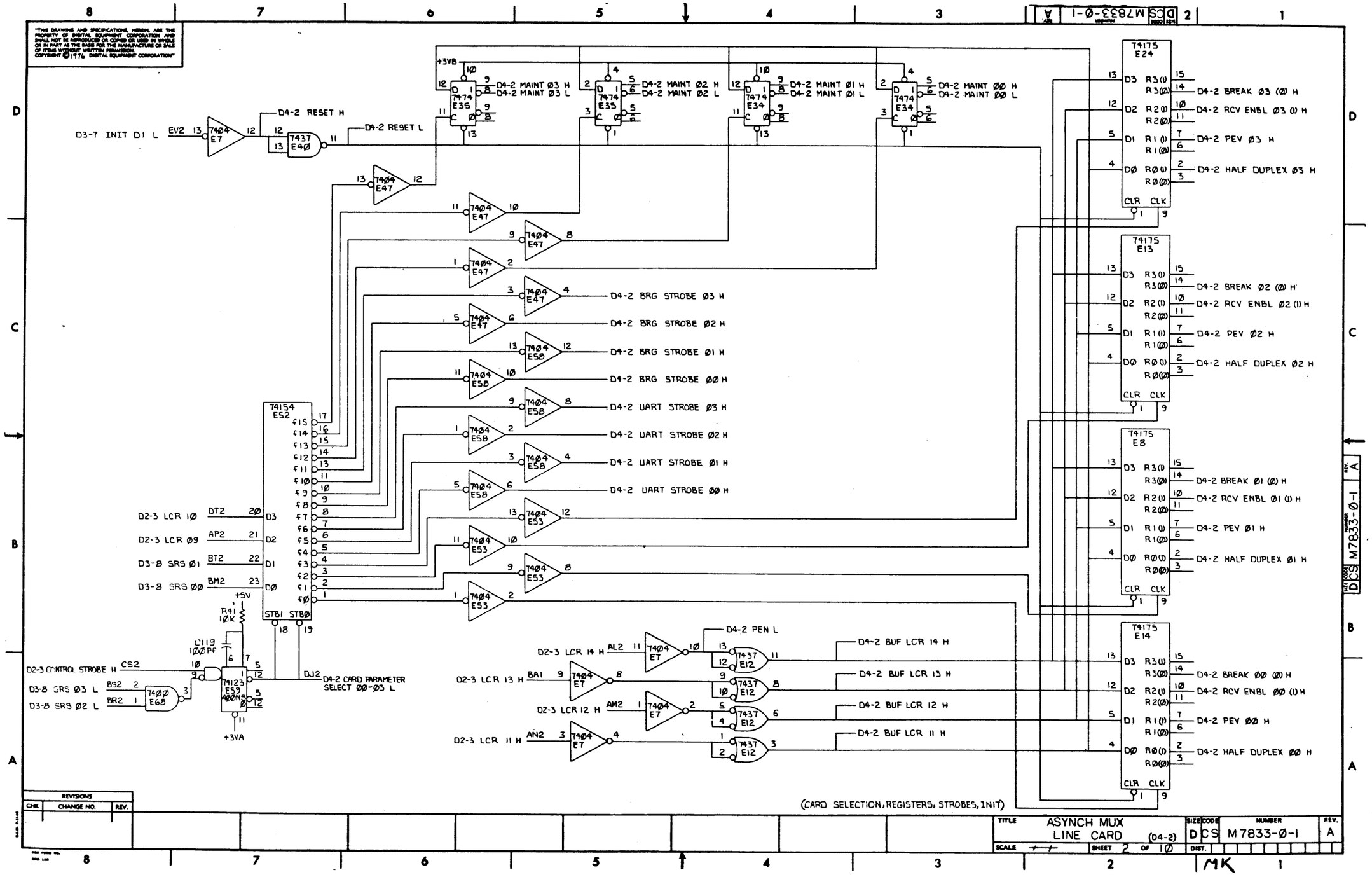
DRN R. Kopenal	1-13-76	FIRST USED ON DV11
CHK	4/6/76	digital
ENG.	April 6, 76	TITLE ASYNCH MUX LINE CARD (D4-1)
PROJ. ENG.	April 6, 76	
PROD. R. Wall	4/6/76	
NEXT HIGHER ASSY. D-UA-M7833-Ø-Ø		SIZE D CODE CS NUMBER M7833-Ø-1 REV. A
SCALE		
SHEET OF 1Ø		DIST.

REVISIONS

CHK	CHANGE NO.	REV.
	M8733-MK001	A
	15-DEC-80	
	R. HARRINGTON	

DEC FORM NO. DRD 160-0

MK



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D3-7 INIT D1 L
EV2
7404 E7
D4-2 RESET H
7437 E40
D4-2 RESET L
+3VB
7474 E35
D4-2 MAINT Ø3 H
D4-2 MAINT Ø3 L
D4-2 MAINT Ø2 H
D4-2 MAINT Ø2 L
7474 E34
D4-2 MAINT Ø1 H
D4-2 MAINT Ø1 L
D4-2 MAINT ØØ H
D4-2 MAINT ØØ L
74175 E24
D4-2 BREAK Ø3 (Ø) H
D4-2 RCV ENBL Ø3 (1) H
D4-2 PEV Ø3 H
D4-2 HALF DUPLEX Ø3 H
74175 E13
D4-2 BREAK Ø2 (Ø) H
D4-2 RCV ENBL Ø2 (1) H
D4-2 PEV Ø2 H
D4-2 HALF DUPLEX Ø2 H
74175 E8
D4-2 BREAK Ø1 (Ø) H
D4-2 RCV ENBL Ø1 (1) H
D4-2 PEV Ø1 H
D4-2 HALF DUPLEX Ø1 H
74175 E14
D4-2 BREAK ØØ (Ø) H
D4-2 RCV ENBL ØØ (1) H
D4-2 PEV ØØ H
D4-2 HALF DUPLEX ØØ H
CLR CLK
74154 E52
D4-2 BRG STROBE Ø3 H
D4-2 BRG STROBE Ø2 H
D4-2 BRG STROBE Ø1 H
D4-2 BRG STROBE ØØ H
D4-2 UART STROBE Ø3 H
D4-2 UART STROBE Ø2 H
D4-2 UART STROBE Ø1 H
D4-2 UART STROBE ØØ H
D2-3 LCR 1Ø
D2-3 LCR Ø9
D3-8 SRS Ø1
D3-8 SRS ØØ
DT2
AP2
BT2
BM2
STB1 STBØ
+5V
R41 1ØK
C119 1ØØ PF
D2-3 CONTROL STROBE H
CS2
D3-8 SRS Ø3 L
BS2
D3-8 SRS Ø2 L
BR2
7400 E68
74123 E59 4ØØNS
+3VA
DJ2
D4-2 CARD PARAMETER SELECT ØØ-Ø3 L
D4-2 PEN L
D2-3 LCR 14 H
AL2
D2-3 LCR 13 H
BA1
D2-3 LCR 12 H
AM2
D2-3 LCR 11 H
AN2
7437 E12
D4-2 BUF LCR 14 H
D4-2 BUF LCR 13 H
D4-2 BUF LCR 12 H
D4-2 BUF LCR 11 H
(CARD SELECTION, REGISTERS, STROBES, INIT)
REVISIONS
CHK
CHANGE NO.
REV.
TITLE ASYNCH MUX LINE CARD (D4-2)
SIZE D
CODE CS
NUMBER M7833-Ø-1
REV. A
SCALE
SHEET 2 OF 1Ø
DIST.
MK

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D3-4 MASTER SCAN D H
D3-4 MASTER SCAN C H
EU2
EN2
7400 E68
DM2
D4-3 CARD FLAG SELECT ØØ-Ø3 L
7404 E73
D3-3 RESYNC PULSE L
DF2
74155 E6Ø
STBB STBA
DB
DA
S1 SØ
ƒBØ D4-3 RESYNC PULSE Ø3 L
ƒB1 D4-3 RESYNC PULSE Ø2 L
ƒB2 D4-3 RESYNC PULSE Ø1 L
ƒB3 D4-3 RESYNC PULSE ØØ L
ƒAØ D4-3 TRAN FLAG CLK Ø3 L
ƒA1 D4-3 TRAN FLAG CLK Ø2 L
ƒA2 D4-3 TRAN FLAG CLK Ø1 L
ƒA3 D4-3 TRAN FLAG CLK ØØ L
D3-4 TRANSMITTER STROBE H
EH2
7400 E68
7404 E53
D4-3 TRAN FILE LOAD L
D4-3 BUF MSCAN Ø1 L
D4-3 BUF MSCAN ØØ L
D4-6 RCV FLAG Ø3 H
D4-6 RCV FLAG Ø2 H
D4-6 RCV FLAG Ø1 H
D4-6 RCV FLAG ØØ H
D4-5 MATCH Ø3 (1) H
D4-5 MATCH Ø2 (1) H
D4-5 MATCH Ø1 (1) H
D4-5 MATCH ØØ (1) H
74153 E37
STBØ STB1
AI BI CI DI
AØ BØ CØ DØ
S1 SØ
ƒ1 ƒØ
7432 ET2
8881 E82
FM2 RECEIVER FLAG L
FE1 MATCH DETECT L
+5V
RB 10K
D1-5 RECEIVED DATA ENABLE H
CN2
7400 E68
74123 E63
FU1
D4-3 RDE ØØ-Ø3
+3VB
FK1
D4-3 DATA ENABLE ØØ-Ø3 H
D4-3 MATCH H
7474 E36
7437 E4Ø
D4-2 RESET L
D4-3 CLR RCV FLAG Ø3 L
D4-3 CLR RCV FLAG Ø2 L
D4-3 CLR RCV FLAG Ø1 L
D4-3 CLR RCV FLAG ØØ L
74155 E31
D4-3 CLR MATCH Ø3 L
D4-3 CLR MATCH Ø2 L
D4-3 CLR MATCH Ø1 L
D4-3 CLR MATCH ØØ L
D3-4 MASTER SCAN Ø1 H
EM1
7404 E73
D3-4 MASTER SCAN ØØ H
EN1
D4-8 TRAN FLAG Ø3 H
D4-8 TRAN FLAG Ø2 H
D4-8 TRAN FLAG Ø1 H
D4-8 TRAN FLAG ØØ H
74153 E83
FL2 TRAN FLAG WAITING
D3-4 MASTER SCAN T/R
CR2
(SCAN SELECTION, FLAGS)

REVISIONS

CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
ASYNCH MUX LINE CARD (04-3)	D	CS	M7833-Ø-1	A
SCALE	SHEET 3 OF 10	DIST.		

M7833-Ø-1 REV A

MK

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R9 1ØK
R1Ø 1ØK
C126 22PF
C123 22PF
7380 E93
7380 E93
Y1 2.457G MHZ
R11 1K
C2ØØ 22PF
7404 E8Ø
W2 (W2 REMOVED FOR AUTOMATED MODULE TEST)
D4-2 RESET H
T493 E92
R3(1) R2(1) R1(1) RØ(1) CLR CLKØ CLKBC
BN2 D4-4 SOURCE CLOCK B ØØ-Ø3 L
D4-2 BUF LCR 14 H
D4-2 BUF LCR 13 H
D4-2 BUF LCR 12 H
D4-2 BUF LCR 11 H
COM 5Ø16 E51
TD TC TB TA STT EXT2 EXT1 RD RC RB RA STR 4T 4R
D4-1 +12V
5Ø88 MHZ E27
+5V
W1 (W1 REMOVED FOR AUTOMATED MODULE TEST)
BJ1 D4-4 SOURCE CLOCK A ØØ-Ø3 L
7437 E46
7437 E46
COM 5Ø16 E57
D4-2 BRG STROBE Ø3 H
D4-2 BRG STROBE Ø2 H
D4-2 BRG STROBE Ø1 H
D4-2 BRG STROBE ØØ H
7420 E39
+3VA
7474 E45
7474 E45
7474 E55
7474 E55
D4-4 SPEED 17Ø3 H
D4-4 SPEED 17Ø2 H
D4-4 SPEED 17Ø1 H
D4-4 SPEED 17ØØ H
D4-2 RESET L
8Ø94 E56
8Ø93 E5Ø
CP2 D4-4 CLOCK Ø3 H
DS2 D4-4 CLOCK Ø2 H
CE2 D4-4 CLOCK Ø1 H
DE2 D4-4 CLOCK ØØ H

(CRYSTAL, CLOCK GENERATION)

REVISIONS
CHK | CHANGE NO | REV.

TITLE ASYNCH MUX LINE CARD (D4-4)
SIZE D | CODE CS | NUMBER M7833-Ø-1 | REV. A
SCALE | SHEET 4 OF 1Ø | DIST.
MK

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D4-6 ENBL ERROR FLAGS L

D4-1Ø OR Ø3
D4-1Ø OR Ø2
D4-9 OR Ø1
D4-9 OR ØØ
D4-1Ø PE Ø3
D4-1Ø PE Ø2
D4-9 PE Ø1
D4-9 PE ØØ

D4-1Ø FE Ø3
D4-1Ø FE Ø2
D4-9 FE Ø1
D4-9 FE ØØ

D4-9 RD8
D4-9 RD7
D4-9 RD6
D4-9 RD5
D4-9 RD4
D4-9 RD3
D4-9 RD2
D4-9 RD1

D4-3 BUF MSCAN ØØ L
D4-3 BUF MSCAN Ø1 L
D4-3 CARD FLAG SELECT ØØ-Ø3 L
D4-6 RCV FILE LOAD L
D4-6 RCV FILE ADDRS Ø1 L
D4-6 RCV FILE ADDRS ØØ L
D4-3 DATA ENABLE ØØ-Ø3 H

MASTER OR L
MASTER PE L
RECV DATA Ø7 L
RECV DATA Ø6 L
RECV DATA Ø5 L
RECV DATA Ø4 L
RECV DATA Ø3 L
RECV DATA Ø2 L
RECV DATA Ø1 L
RECV DATA ØØ L

D4-2 RCV ENBL Ø3 (1) H
D4-3 CLR MATCH Ø3 L
D4-3 RESYNC PULSE Ø3 L
D4-5 MATCH Ø3 (1) H
D4-5 ACTIVE Ø3 H
D4-5 ACTIVE Ø3 L

D4-2 RCV ENBL Ø2 (1) H
D4-3 CLR MATCH Ø2 L
D4-3 RESYNC PULSE Ø2 L
D4-5 MATCH Ø2 (1) H
D4-5 ACTIVE Ø2 H
D4-5 ACTIVE Ø2 L

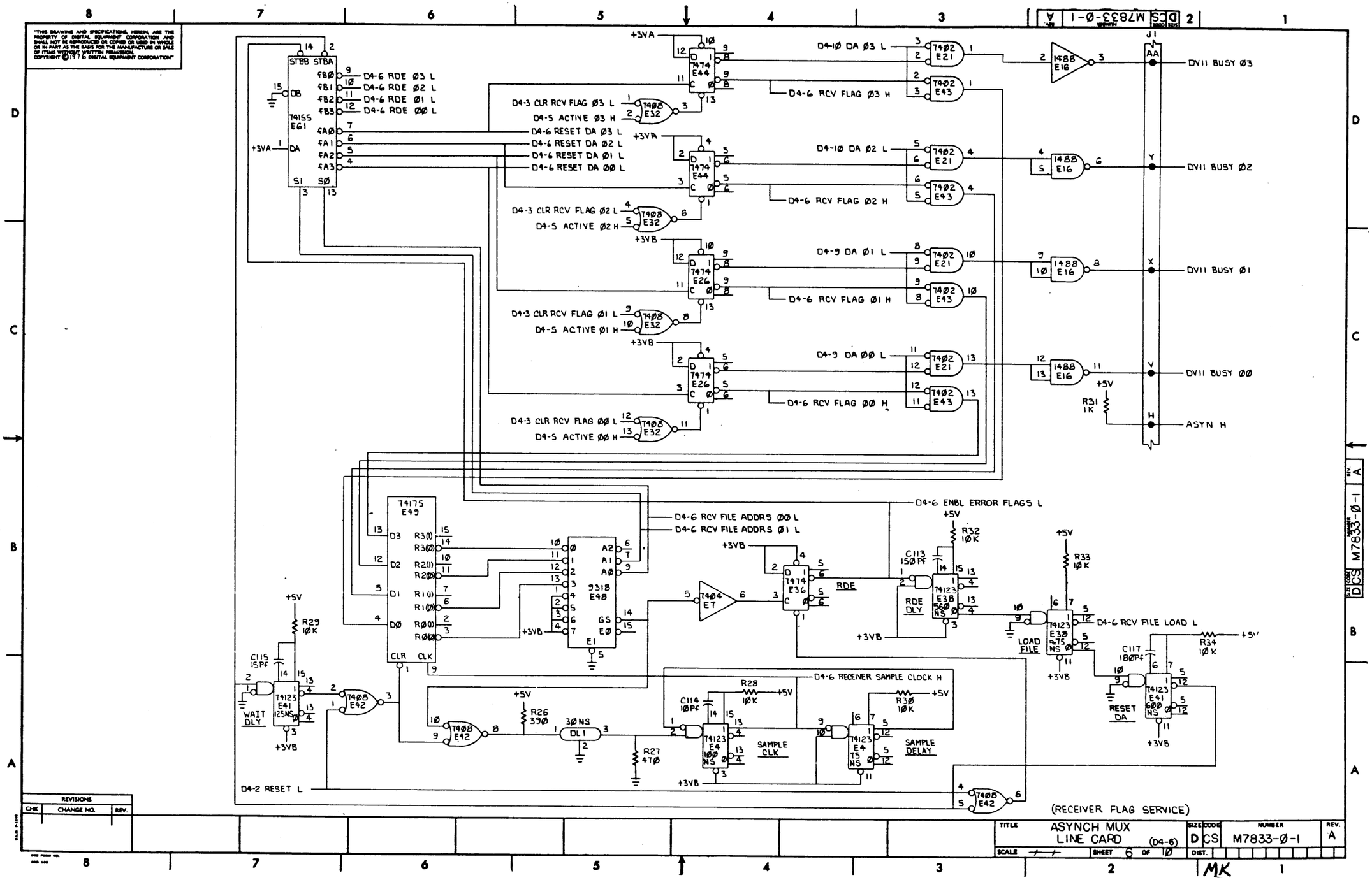
D4-2 RCV ENBL Ø1 (1) H
D4-3 CLR MATCH Ø1 L
D4-3 RESYNC PULSE Ø1 L
D4-5 MATCH Ø1 (1) H
D4-5 ACTIVE Ø1 H
D4-5 ACTIVE Ø1 L

D4-2 RCV ENBL ØØ (1) H
D4-3 CLR MATCH ØØ L
D4-3 RESYNC PULSE ØØ L
D4-5 MATCH ØØ (1) H
D4-5 ACTIVE ØØ H
D4-5 ACTIVE ØØ L

(RCV FILES, RCV DATA, MATCH LOGIC)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
ASYNCH MUX LINE CARD (D4-5)	D	DCS	M7833-Ø-1	A
SCALE	SHEET 5 OF 1Ø	DIST.	MK	



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DCS M7833-Ø-1 A
74155 E61
D4-6 RDE Ø3 L
D4-6 RDE Ø2 L
D4-6 RDE Ø1 L
D4-6 RDE ØØ L
D4-3 CLR RCV FLAG Ø3 L
D4-5 ACTIVE Ø3 H
D4-6 RESET DA Ø3 L
D4-6 RESET DA Ø2 L
D4-6 RESET DA Ø1 L
D4-6 RESET DA ØØ L
D4-3 CLR RCV FLAG Ø2 L
D4-5 ACTIVE Ø2 H
D4-3 CLR RCV FLAG Ø1 L
D4-5 ACTIVE Ø1 H
D4-3 CLR RCV FLAG ØØ L
D4-5 ACTIVE ØØ H
D4-1Ø DA Ø3 L
D4-6 RCV FLAG Ø3 H
D4-1Ø DA Ø2 L
D4-6 RCV FLAG Ø2 H
D4-9 DA Ø1 L
D4-6 RCV FLAG Ø1 H
D4-9 DA ØØ L
D4-6 RCV FLAG ØØ H
DV11 BUSY Ø3
DV11 BUSY Ø2
DV11 BUSY Ø1
DV11 BUSY ØØ
ASYN H
R31 1K
74175 E49
9318 E48
D4-6 RCV FILE ADDRS ØØ L
D4-6 RCV FILE ADDRS Ø1 L
D4-6 ENBL ERROR FLAGS L
RDE
RDE DLY
LOAD FILE
D4-6 RCV FILE LOAD L
RESET DA
WAIT DLY
D4-6 RECEIVER SAMPLE CLOCK H
SAMPLE CLK
SAMPLE DELAY
D4-2 RESET L
(RECEIVER FLAG SERVICE)
REVISIONS
CHK
CHANGE NO.
REV.
TITLE ASYNCH MUX LINE CARD (D4-6)
SIZE D
CODE CS
NUMBER M7833-Ø-1
REV. A
SCALE
SHEET 6 OF 1Ø
DIST.
MK

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D4-10 SERIAL OUT Ø3 H
D4-2 BREAK Ø3 (Ø) H
AH2
74Ø8 E9
1488 E11
J1 EE
EIA XMIT DATA Ø3
EIA RCV DATA Ø3
J1 KK
1489 E5
C1Ø6 47ØPf
D4-2 MAINT Ø3 H
8Ø94 E17
8Ø93 E18
D4-2 HALF DUPLEX Ø3 H
D4-1Ø EOC Ø3 L
(EF2)
74Ø8 E19
7432 E3
D4-5 ACTIVE Ø3 L
7432 E22
BK1
D4-7 SERIAL IN Ø3 H

D4-10 SERIAL OUT Ø2 H
D4-2 BREAK Ø2 (Ø) H
AT2
74Ø8 E9
1488 E11
J1 CC
EIA XMIT DATA Ø2
EIA RCV DATA Ø2
J1 HH
1489 E5
C1Ø5 47ØPf
D4-2 MAINT Ø2 H
8Ø94 E17
8Ø93 E18
D4-2 HALF DUPLEX Ø2 H
D4-1Ø EOC Ø2 L
(EK2)
74Ø8 E19
7432 E3
D4-5 ACTIVE Ø2 L
7432 E22
BK2
D4-7 SERIAL IN Ø2 H

D4-9 SERIAL OUT Ø1 H
D4-2 BREAK Ø1 (Ø) H
AB1
74Ø8 E9
1488 E11
J1 T
EIA XMIT DATA Ø1
EIA RCV DATA Ø1
J1 N
1489 E5
C128 47ØPf
D4-2 MAINT Ø1 H
8Ø94 E17
8Ø93 E18
D4-2 HALF DUPLEX Ø1 H
D4-9 EOC Ø1 L
(ER2)
74Ø8 E19
7432 E3
D4-5 ACTIVE Ø1 L
7432 E22
BD1
D4-7 SERIAL IN Ø1 H

D4-9 SERIAL OUT ØØ H
D4-2 BREAK ØØ (Ø) H
AJ2
74Ø8 E9
1488 E11
J1 R
EIA XMIT DATA ØØ
EIA RCV DATA ØØ
J1 L
1489 E5
C129 47Ø Pf
D4-2 MAINT ØØ H
8Ø94 E17
8Ø93 E18
D4-2 HALF DUPLEX ØØ H
D4-9 EOC ØØ L
(FJ2)
74Ø8 E19
7432 E3
D4-5 ACTIVE ØØ L
7432 E22
BF2
D4-7 SERIAL IN ØØ H

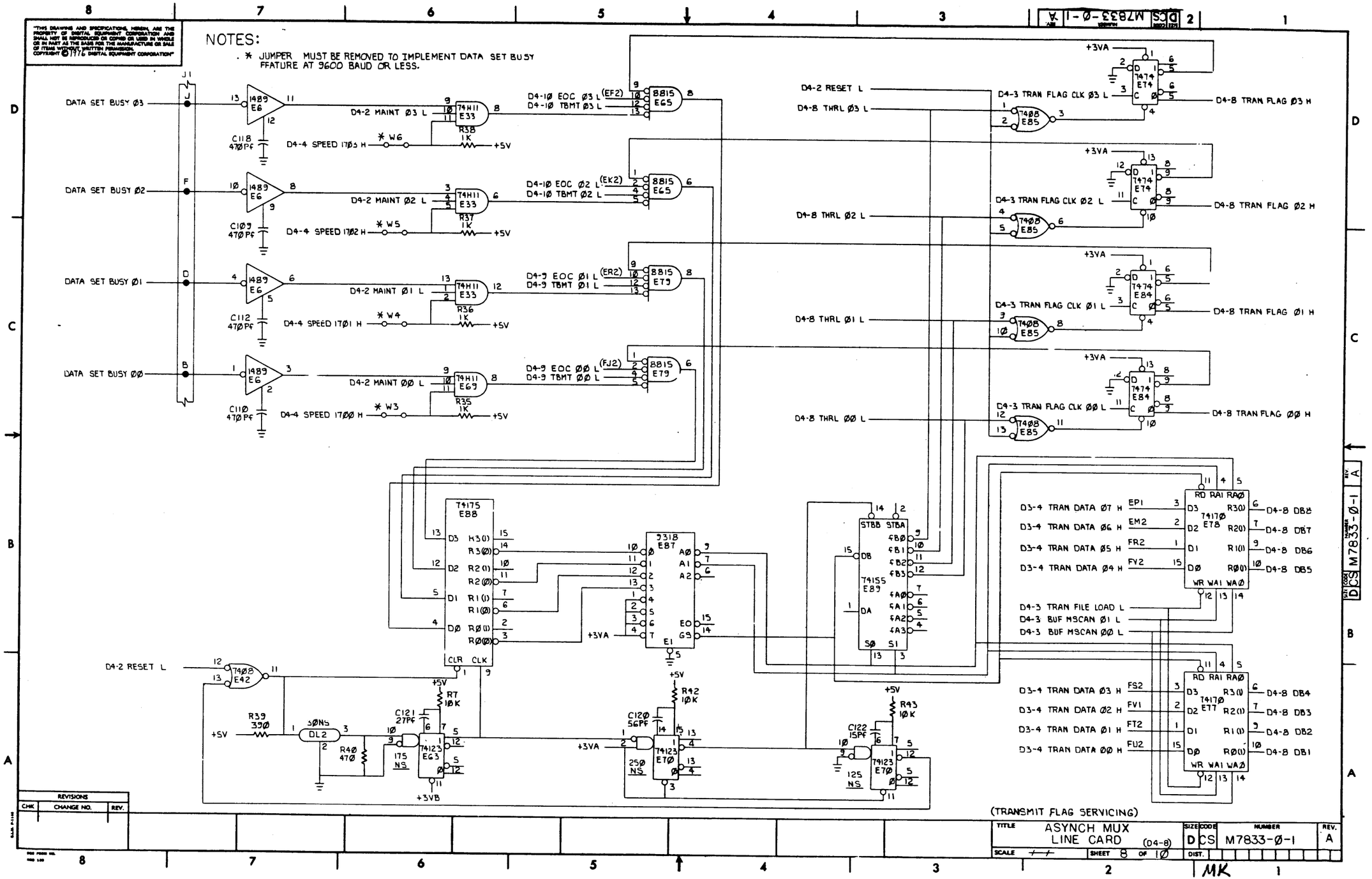
(EIA IN & OUT. HALF DUPLEX, BREAK, MAINT LOGIC)

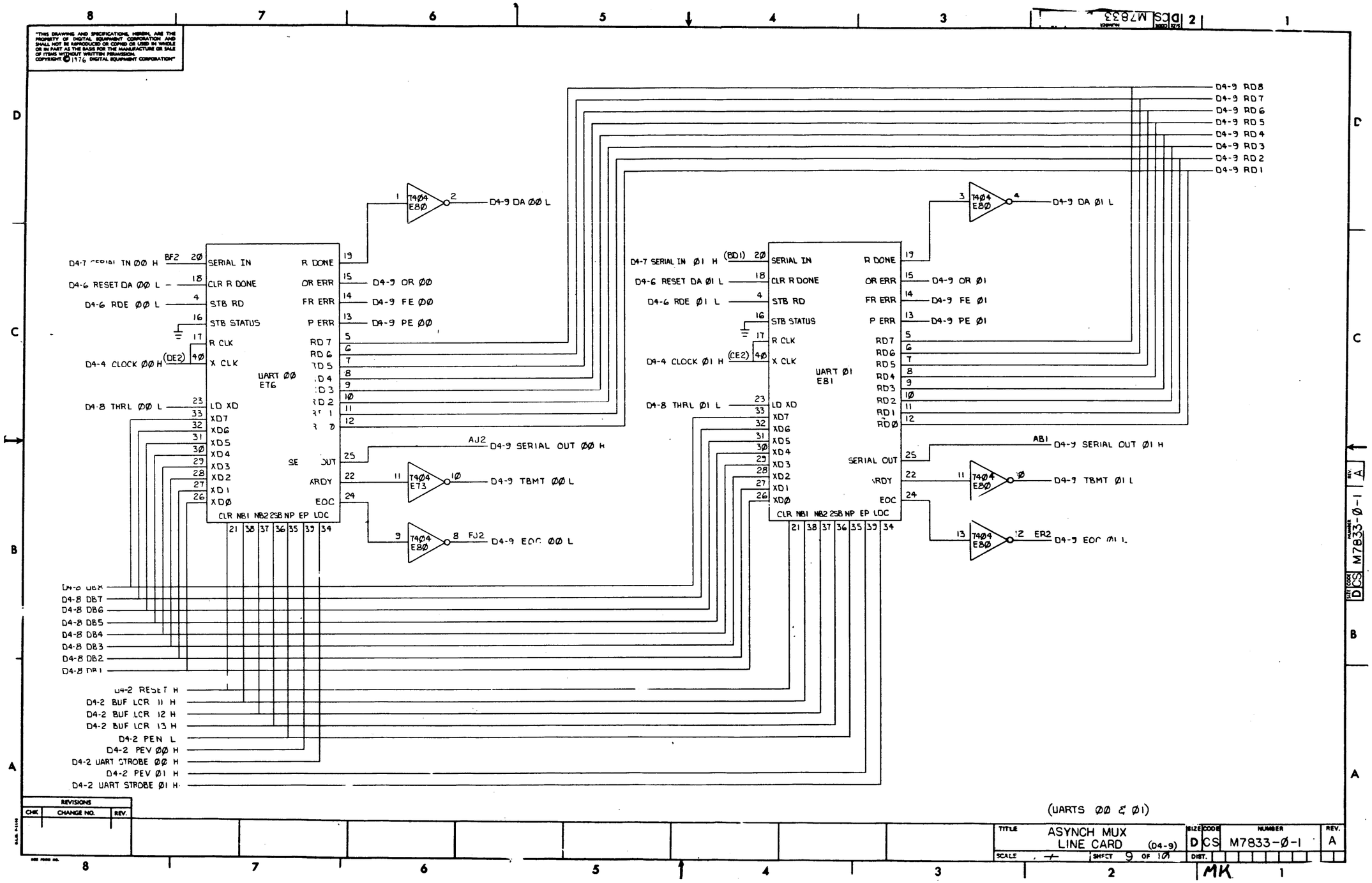
REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
ASYNCH MUX LINE CARD (D4-7)	D	CS	M7833-Ø-1	A
SCALE	SHEET 7 OF 1Ø	DIST.		

MK

M7833-Ø-1 REV A DCS 2


NOTES:
. * JUMPER MUST BE REMOVED TO IMPLEMENT DATA SET BUSY FFATURE AT 9600 BAUD OR LESS.
DATA SET BUSY Ø3
DATA SET BUSY Ø2
DATA SET BUSY Ø1
DATA SET BUSY ØØ
D4-2 MAINT Ø3 L
D4-2 MAINT Ø2 L
D4-2 MAINT Ø1 L
D4-2 MAINT ØØ L
D4-4 SPEED 17Ø3 H
D4-4 SPEED 17Ø2 H
D4-4 SPEED 17Ø1 H
D4-4 SPEED 17ØØ H
D4-1Ø EOC Ø3 L
D4-1Ø TBMT Ø3 L
D4-1Ø EOC Ø2 L
D4-1Ø TBMT Ø2 L
D4-9 EOC Ø1 L
D4-9 TBMT Ø1 L
D4-9 EOC ØØ L
D4-9 TBMT ØØ L
D4-2 RESET L
D4-8 THRL Ø3 L
D4-8 THRL Ø2 L
D4-8 THRL Ø1 L
D4-8 THRL ØØ L
D4-3 TRAN FLAG CLK Ø3 L
D4-3 TRAN FLAG CLK Ø2 L
D4-3 TRAN FLAG CLK Ø1 L
D4-3 TRAN FLAG CLK ØØ L
D4-8 TRAN FLAG Ø3 H
D4-8 TRAN FLAG Ø2 H
D4-8 TRAN FLAG Ø1 H
D4-8 TRAN FLAG ØØ H
D3-4 TRAN DATA Ø7 H
D3-4 TRAN DATA Ø6 H
D3-4 TRAN DATA Ø5 H
D3-4 TRAN DATA Ø4 H
D4-3 TRAN FILE LOAD L
D4-3 BUF MSCAN Ø1 L
D4-3 BUF MSCAN ØØ L
D3-4 TRAN DATA Ø3 H
D3-4 TRAN DATA Ø2 H
D3-4 TRAN DATA Ø1 H
D3-4 TRAN DATA ØØ H
D4-8 DB8
D4-8 DB7
D4-8 DB6
D4-8 DB5
D4-8 DB4
D4-8 DB3
D4-8 DB2
D4-8 DB1
(TRANSMIT FLAG SERVICING)
TITLE ASYNCH MUX LINE CARD (D4-8)
SIZE D CODE CS NUMBER M7833-Ø-1 REV. A
SCALE SHEET 8 OF 1Ø
DIST.
MK
REVISIONS
CHK CHANGE NO. REV.
DCS M7833-Ø-1 A



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D4-9 RD8
D4-9 RD7
D4-9 RD6
D4-9 RD5
D4-9 RD4
D4-9 RD3
D4-9 RD2
D4-9 RD1
D4-9 DA ØØ L
D4-9 DA Ø1 L
D4-7 SERIAL IN ØØ H
D4-6 RESET DA ØØ L
D4-6 RDE ØØ L
D4-4 CLOCK ØØ H
D4-8 THRL ØØ L
SERIAL IN
CLR R DONE
STB RD
STB STATUS
R CLK
X CLK
LD XD
XD7
XD6
XD5
XD4
XD3
XD2
XD1
XDØ
R DONE
OR ERR
FR ERR
P ERR
RD7
RD6
RD5
RD4
RD3
RD2
RD1
RDØ
SERIAL OUT
XRDY
EOC
CLR NB1 NB2 2SB NP EP LDC
UART ØØ
ET6
UART Ø1
E81
D4-9 OR ØØ
D4-9 FE ØØ
D4-9 PE ØØ
D4-9 OR Ø1
D4-9 FE Ø1
D4-9 PE Ø1
D4-9 SERIAL OUT ØØ H
D4-9 TBMT ØØ L
D4-9 EOC ØØ L
D4-9 SERIAL OUT Ø1 H
D4-9 TBMT Ø1 L
D4-9 EOC Ø1 L
D4-8 DB8
D4-8 DB7
D4-8 DB6
D4-8 DB5
D4-8 DB4
D4-8 DB3
D4-8 DB2
D4-8 DB1
D4-2 RESET H
D4-2 BUF LCR 11 H
D4-2 BUF LCR 12 H
D4-2 BUF LCR 13 H
D4-2 PEN L
D4-2 PEV ØØ H
D4-2 UART STROBE ØØ H
D4-2 PEV Ø1 H
D4-2 UART STROBE Ø1 H
(UARTS ØØ & Ø1)
REVISIONS
CHK
CHANGE NO.
REV.
TITLE
ASYNCH MUX
LINE CARD
(D4-9)
SIZE D
CODE CS
NUMBER M7833-Ø-1
REV. A
SCALE
SHEET 9 OF 10
DIST.
MK

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D4-9 RD8
D4-9 RD7
D4-9 RD6
D4-9 RD5
D4-9 RD4
D4-9 RD3
D4-9 RD2
D4-9 RD1

D4-8 DB8
D4-8 DB7
D4-8 DB6
D4-8 DB5
D4-8 DB4
D4-8 DB3
D4-8 DB2
D4-8 DB1

D4-2 RESET H
D4-2 BUF LCR 11 H
D4-2 BUF LCR 12 H
D4-2 BUF LCR 13 H
D4-2 PEN L
D4-2 PEV Ø2 H
D4-2 UART STROBE Ø2 H
D4-2 PEV Ø3 H
D4-2 UART STROBE Ø3 H

UART Ø2 E67

D4-7 SERIAL IN Ø2 H (BK2) 20 SERIAL IN
D4-6 RESET DA Ø2 L 18 CLR R DONE
D4-6 RDE Ø2 L 4 STB RD
16 STB STATUS
17 R CLK
D4-4 CLOCK Ø2 H (DS2) 40 X CLK
D4-8 THRL Ø2 L 23 LD XD
33 XD7
32 XD6
31 XD5
30 XD4
29 XD3
28 XD2
27 XD1
26 XDØ
21 38 37 36 35 39 34 CLR NBI NB2 2SB NP EP LDC

R DONE 19 ← 74Ø4 E66 1 → 2 D4-1Ø DA Ø2 L
OR ERR 15 → D4-1Ø OR Ø2
FR ERR 14 → D4-1Ø FE Ø2
P ERR 13 → D4-1Ø PE Ø2
RD7 5
RD6 6
RD5 7
RD4 8
RD3 9
RD2 1Ø
RD1 11
RDØ 12
SERIAL OUT 25 → AT2 D4-1Ø SERIAL OUT Ø2 H
XRDY 22 ← 74Ø4 E66 5 → 6 D4-1Ø TBMT Ø2 L
EOC 24 → 74Ø4 E66 9 → 8 EK2 D4-1Ø EOC Ø2 L

UART Ø3 E62

D4-7 SERIAL IN Ø3 H (BK1) 20 SERIAL IN
D4-6 RESET DA Ø3 L 18 CLR R DONE
D4-6 RDE Ø3 L 4 STB RD
16 STB STATUS
17 R CLK
D4-4 CLOCK Ø3 H (CP2) 40 X CLK
D4-8 THRL Ø3 L 23 LD XD
33 XD7
32 XD6
31 XD5
30 XD4
29 XD3
28 XD2
27 XD1
26 XDØ
21 38 37 36 35 39 34 CLR NBI NB2 2SB NP EP LDC

R DONE 19 ← 74Ø4 E66 3 → 4 D4-1Ø DA Ø3 L
OR ERR 15 → D4-1Ø OR Ø3
FR ERR 14 → D4-1Ø FE Ø3
P ERR 13 → D4-1Ø PE Ø3
RD7 5
RD6 6
RD5 7
RD4 8
RD3 9
RD2 1Ø
RD1 11
RDØ 12
SERIAL OUT 25 → AH2 D4-1Ø SERIAL OUT Ø3 H
XRDY 22 ← 74Ø4 E66 11 → 1Ø D4-1Ø TBMT Ø3 L
EOC 24 → 74Ø4 E66 13 → 12 EF2 D4-1Ø EOC Ø3 L

(UARTS Ø2 & Ø3)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
ASYNCH MUX LINE CARD (D4-1Ø)	D	CS	M7833-Ø-1	A
SCALE —	SHEET 1Ø OF 1Ø	DIST.		

MK

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BERG CONNECTOR

J1

A — DATA SET BUSY ØØ
B
C
D — DATA SET BUSY Ø1
E
F
H — DATA SET BUSY Ø2
J — ASYN H
K — DATA SET BUSY Ø3
L
M — EIA RCV DATA ØØ
N
P
R — EIA RCV DATA Ø1
S
T
U — EIA XMIT DATA ØØ
V — EIA XMIT DATA Ø1
W — DVII BUSY ØØ
X
Y — DVII BUSY Ø1
Z — DVII BUSY Ø2
AA
BB — DVII BUSY Ø3
CC
DD — EIA XMIT DATA Ø2
EE
FF — EIA XMIT DATA Ø3
HH — EIA RCV DATA Ø2
JJ
KK — EIA RCV DATA Ø3
LL
MM
NN
PP
RR
SS
TT
UU
VV

+5V — R1 330 — +3VA
C125 .Ø1 µfd — R3 75Ø

+5V — R2 330 — +3VB
C111 .Ø1 µfd — R4 75Ø

+15V — CU1 — R5Ø 39 1/2W — D4-1+12V (TO PIN 9 OF 5Ø16) (TO PIN 14 OF 1488)
D1 IN759A — C116 .Ø1 µfd — C1Ø8 .Ø1 µfd

-15V — FB2 — Q1 2N2Ø4
R44 1Ø — R45 1Ø — R46 1Ø — R47 1Ø
D4 D672 — D5 D672 — D6 D672
R48 2.7Ø
R49 47Ø 1/2W
C127 1ØØØPF
Q2 6534D
R5 1K — C124 6.8 µfd — D4-1 -12V (TO PIN 1 OF 1488) (TO PIN 2 OF UART)
R6 1K
D8 IN752A — D7 D672

CLOCK GENERATION CHART

CLOCK ADDRESS DCBA	BAUD RATE	PERIOD (USEC)
ØØØØ	50	1250.00
ØØØ1	75	833.33
ØØ1Ø	110	568.18
ØØ11	134.5	464.68
Ø1ØØ	150	416.67
Ø1Ø1	300	208.33
Ø11Ø	600	104.17
Ø111	1200	52.08
1ØØØ	1800	34.72
1ØØ1	2000	31.25
1Ø1Ø	2400	26.04
1Ø11	3600	17.36
11ØØ	4800	13.02
11Ø1	7200	8.68
111Ø	9600	6.51
1111	38400	1.63

+5V — C1-C95 .Ø1 µfd — C96-C1Ø1 6.8 µfd
GND

(CHART, REGULATORS)

REVISIONS: REV. | CHANGE NO. | CHK.

DRN	R Hammel	4-13-76
CHK	D Fotta	4-15-76
ENG	M P Smith	4-15-76
PROJ. ENG.	W A Hill	4-15-76
PROD.	R. Wall	4-16-76
NEXT HIGHER ASSY.	B-DD-DV11-Ø	
SCALE		
SHEET	OF 1Ø	

FIRST USED ON: DV11

TITLE: ASYNCH MUX LINE CARD LINES ØØ-Ø3 (D4-1)

SIZE D | CODE BS | NUMBER DV11-Ø-15 | REV. *

DIST.

D BS DV11-Ø-15

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D3-7 INIT D1 L
D4-2 RESET H
D4-2 RESET L
D4-2 MAINT Ø3 H
D4-2 MAINT Ø3 L
D4-2 MAINT Ø2 H
D4-2 MAINT Ø2 L
D4-2 MAINT Ø1 H
D4-2 MAINT Ø1 L
D4-2 MAINT ØØ H
D4-2 MAINT ØØ L
D4-2 BRG STROBE Ø3 H
D4-2 BRG STROBE Ø2 H
D4-2 BRG STROBE Ø1 H
D4-2 BRG STROBE ØØ H
D4-2 UART STROBE Ø3 H
D4-2 UART STROBE Ø2 H
D4-2 UART STROBE Ø1 H
D4-2 UART STROBE ØØ H
D2-3 LCR 1Ø
D2-3 LCR Ø9
D3-8 SRS Ø1
D3-8 SRS ØØ
D2-3 CONTROL STROBE H
D3-8 SRS Ø3 L
D3-8 SRS Ø2 L
D4-2 CARD PARAMETER SELECT ØØ-Ø3 L
D2-3 LCR 14 H
D2-3 LCR 13 H
D2-3 LCR 12 H
D2-3 LCR 11 H
D4-2 PEN L
D4-2 BUF LCR 14 H
D4-2 BUF LCR 13 H
D4-2 BUF LCR 12 H
D4-2 BUF LCR 11 H
D4-2 BREAK Ø3 (Ø) H
D4-2 RCV ENBL Ø3 (1) H
D4-2 PEV Ø3 H
D4-2 HALF DUPLEX Ø3 H
D4-2 BREAK Ø2 (Ø) H
D4-2 RCV ENBL Ø2 (1) H
D4-2 PEV Ø2 H
D4-2 HALF DUPLEX Ø2 H
D4-2 BREAK Ø1 (Ø) H
D4-2 RCV ENBL Ø1 (1) H
D4-2 PEV Ø1 H
D4-2 HALF DUPLEX Ø1 H
D4-2 BREAK ØØ (Ø) H
D4-2 RCV ENBL ØØ (1) H
D4-2 PEV ØØ H
D4-2 HALF DUPLEX ØØ H

(CARD SELECTION, REGISTERS, STROBES, INIT)

REVISIONS

CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
ASYNCH MUX LINE CARD LINES ØØ-Ø3 (Ø4-2)	D	BS	DV11-Ø-15	*
SCALE —	SHEET 2 OF 1Ø	DIST.		

DV11-Ø-15

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D3-4 MASTER SCAN D H
D3-4 MASTER SCAN C H
EU2
EN2
T400 E68
DM2
D4-3 CARD FLAG SELECT ØØ-Ø3 L
T404 E73
STB8 STBA
D3-3 RESYNC PULSE L
DF2
DB
T4155 E60
SA
SB
SI
SØ
FBØ
FB1
FB2
FB3
FAØ
FA1
FA2
FA3
D4-3 RESYNC PULSE Ø3 L
D4-3 RESYNC PULSE Ø2 L
D4-3 RESYNC PULSE Ø1 L
D4-3 RESYNC PULSE ØØ L
D4-3 TRAN FLAG CLK Ø3 L
D4-3 TRAN FLAG CLK Ø2 L
D4-3 TRAN FLAG CLK Ø1 L
D4-3 TRAN FLAG CLK ØØ L
D3-4 TRANSMITTER STROBE H
EH2
T400 E68
T404 E53
D4-3 TRAN FILE LOAD L
D4-3 BUF MSCAN Ø1 L
D4-3 BUF MSCAN ØØ L
STBØ STB1
D4-6 RCV FLAG Ø3 H
D4-6 RCV FLAG Ø2 H
D4-6 RCV FLAG Ø1 H
D4-6 RCV FLAG ØØ H
D4-5 MATCH Ø3 (1) H
D4-5 MATCH Ø2 (1) H
D4-5 MATCH Ø1 (1) H
D4-5 MATCH ØØ (1) H
AI
BI
CI
DI
AØ
BØ
CØ
DØ
T4153 E37
T432 E72
8881 E82
FM2
RECEIVER FLAG L
FE1
MATCH DETECT L
+5V
R8 10K
D1-5 RECEIVED DATA ENABLE H
CN2
T400 E68
FU1
D4-3 RDE ØØ-Ø3
T4123 E63
+3VB
FK1
D4-3 DATA ENABLE ØØ-Ø3 H
D4-3 MATCH H
T7474 E36
T437 E90
D4-2 RESET L
STB6 STBA
D4-3 CLR RCV FLAG Ø3 L
D4-3 CLR RCV FLAG Ø2 L
D4-3 CLR RCV FLAG Ø1 L
D4-3 CLR RCV FLAG ØØ L
D4-3 CLR MATCH Ø3 L
D4-3 CLR MATCH Ø2 L
D4-3 CLR MATCH Ø1 L
D4-3 CLR MATCH ØØ L
D3-4 MASTER SCAN Ø1 H
EM1
T404 E73
D3-4 MASTER SCAN ØØ H
EN1
T404 E73
STB1 STBØ
D4-8 TRAN FLAG Ø3 H
D4-8 TRAN FLAG Ø2 H
D4-8 TRAN FLAG Ø1 H
D4-8 TRAN FLAG ØØ H
T4153 E83
8881 E82
FL2
TRAN FLAG WAITING L
D3-4 MASTER SCAN T/R
CR2
T404 E73
(SCAN SELECTION, FLAGS)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	ASYNCH MUX LINE CARD LINES ØØ-Ø3 (D4-3)			
SIZE	CODE	NUMBER		REV.
D	BS	DV11-Ø-15		*
SCALE		SHEET 3 OF 10	DIST.	

D BS DV11-Ø-15

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R9 10K
R10 10K
C126 22PF
C123 22PF
7380 E93
7380 E93
Y1 2.4576 MHZ
C200 22PF
R11 1K
7404 E80
W2 (W2 REMOVED FOR AUTOMATED MODULE TEST)
7493 E92
D4-2 RESET H
R3(1) R2(1) R1(0) R0(0) CLR CLK0 CLKBC
BN2 D4-4 SOURCE CLOCK B Ø0-Ø3 L
D4-2 BUF LCR 14 H
D4-2 BUF LCR 13 H
D4-2 BUF LCR 12 H
D4-2 BUF LCR 11 H
COM 5016 E51
D4-1 +12V
BJ1 D4-4 SOURCE CLOCK A Ø0-Ø3 L
5068 MHZ E27
+5V
W1 (W1 REMOVED FOR AUTOMATED MODULE TEST)
7437 E46
7437 E46
COM 5016 E57
D4-1 +12V
+3VA
7474 E45
7474 E45
7474 E55
7474 E55
7420 E39
D4-2 BRG STROBE Ø3 H
D4-2 BRG STROBE Ø2 H
D4-2 BRG STROBE Ø1 H
D4-2 BRG STROBE Ø0 H
D4-2 RESET L
8094 E56
8093 E50
CP2 D4-4 CLOCK Ø3 H
DS2 D4-4 CLOCK Ø2 H
CE2 D4-4 CLOCK Ø1 H
DE2 D4-4 CLOCK Ø0 H
D4-4 SPEED 17Ø3 H
D4-4 SPEED 17Ø2 H
D4-4 SPEED 17Ø1 H
D4-4 SPEED 17ØØ H

(CRYSTAL, CLOCK GENERATION)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
ASYNCH MUX LINE CARD LINES Ø0-03 (D4-4)	D	BS	DV11-Ø-15	*
SCALE	SHEET 4 OF 10	DIST.		

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D4-6 ENBL ERROR FLAGS L

D4-1Ø OR Ø3
D4-1Ø OR Ø2
D4-9 OR Ø1
D4-9 OR ØØ
D4-1Ø PE Ø3
D4-1Ø PE Ø2
D4-9 PE Ø1
D4-9 PE ØØ

74153 E71 (STBØ STB1 AI BI CI DI AØ BØ CØ DØ SI SØ 1Y)

D4-1Ø FE Ø3
D4-1Ø FE Ø2
D4-9 FE Ø1
D4-9 FE ØØ

74153 E75 (STBØ STB1 AI BI CI DI AØ BØ CØ DØ SI SØ 1Y)

7404 E53

74H11 E69

74H11 E69

SØ	F
L	A
H	B

74157 E64 (+3VB BI AI +3VB BØ AØ B3 A3 B2 A2 SØ STB → 1Y 2Y 3Y 4Y)

D4-9 RD8
D4-9 RD7
D4-9 RD6
D4-9 RD5

74170 E35 (RD RAI RAØ D3 D2 D1 DØ WR WAI WAØ → R3(I) R2(I) R1(I) RØ(I))

D4-3 BUF MSCAN ØØ L
D4-3 BUF MSCAN Ø1 L
D4-3 CARD FLAG SELECT ØØ-Ø3 L

D4-9 RD4
D4-9 RD3
D4-9 RD2
D4-9 RD1

74170 E34 (RD RAI RAØ D3 D2 D1 DØ WR WAI WAØ → R3(I) R2(I) R1(I) RØ(I))

D4-6 RCV FILE LOAD L
D4-6 RCV FILE ADDRS Ø1 L
D4-6 RCV FILE ADDRS ØØ L
D4-3 DATA ENABLE ØØ-Ø3 H

8881 E86 → FL1 MASTER OR L (R12 1K +5V)
8881 E86 → FM1 MASTER PE L (R13 1K +5V)
8881 E86 → FH1 RECV DATA Ø7 L (R14 1K +5V)
8881 E86 → FJ1 RECV DATA Ø6 L (R15 1K +5V)
8881 E9Ø → FR1 RECV DATA Ø5 L (R16 1K +5V)
8881 E9Ø → FS1 RECV DATA Ø4 L (R17 1K +5V)
8881 E9Ø → FN1 RECV DATA Ø3 L (R18 1K +5V)
8881 E9Ø → FP1 RECV DATA Ø2 L (R19 1K +5V)
8881 E91 → FN2 RECV DATA Ø1 L (R2Ø 1K +5V)
8881 E91 → FP2 RECV DATA ØØ L (R21 1K +5V)

R22 1ØK +5V
C1Ø2 27 PF
D4-2 RCV ENBL Ø3 (1) H
+3VB
74123 E2 (1Ø 16Ø NS)
7474 E29 (D C)
D4-5 MATCH Ø3 (1) H
D4-5 ACTIVE Ø3 H
D4-5 ACTIVE Ø3 L
D4-3 CLR MATCH Ø3 L
7408 E3Ø
D4-3 RESYNC PULSE Ø3 L
D4-2 RCV ENBL Ø3 (1) H

R23 1ØK +5V
C1Ø3 27PF
D4-2 RCV ENBL Ø2 (1) H
+3VB
74123 E2 (1Ø 16Ø NS)
7474 E23 (D C)
D4-5 MATCH Ø2 (1) H
D4-5 ACTIVE Ø2 H
D4-5 ACTIVE Ø2 L
D4-3 CLR MATCH Ø2 L
7408 E3Ø
D4-3 RESYNC PULSE Ø2 L
D4-2 RCV ENBL Ø2 (1) H

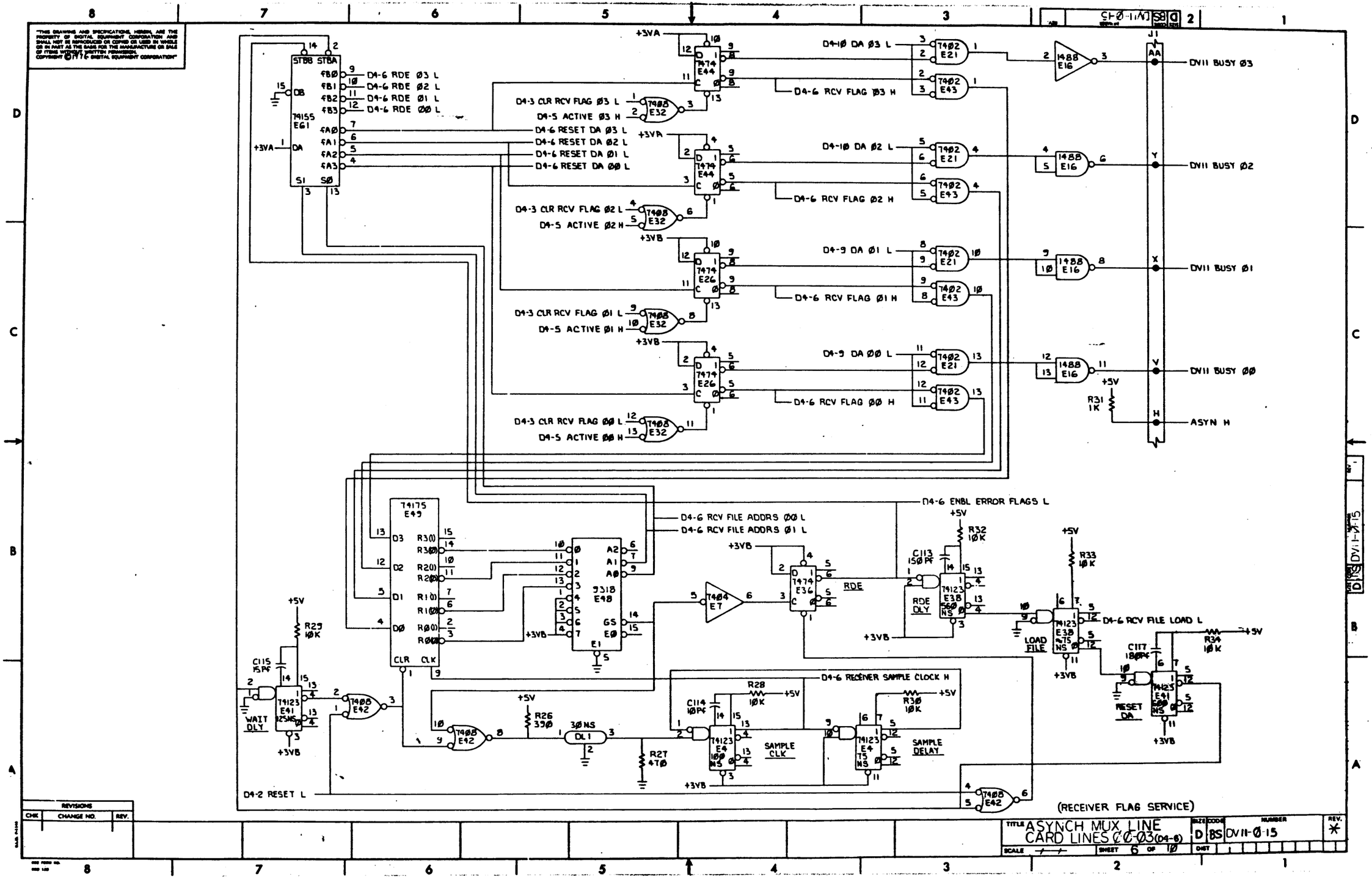
R24 1ØK +5V
C1Ø4 27 PF
D4-2 RCV ENBL Ø1 (1) H
+3VB
74123 E1Ø (1Ø 16Ø NS)
7474 E25 (D C)
D4-5 MATCH Ø1 (1) H
D4-5 ACTIVE Ø1 H
D4-5 ACTIVE Ø1 L
D4-3 CLR MATCH Ø1 L
7408 E2Ø
D4-3 RESYNC PULSE Ø1 L
D4-2 RCV ENBL Ø1 (1) H

R25 1ØK +5V
C1Ø7 27 PF
D4-2 RCV ENBL ØØ (1) H
+3VB
74123 E1Ø (1Ø 16Ø NS)
7474 E15 (D C)
D4-5 MATCH ØØ (1) H
D4-5 ACTIVE ØØ H
D4-5 ACTIVE ØØ L
D4-3 CLR MATCH ØØ L
7408 E2Ø
D4-3 RESYNC PULSE ØØ L
D4-2 RCV ENBL ØØ (1) H

(RCV FILES, RCV DATA, MATCH LOGIC)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE ASYNCH MUX LINE CARD LINES ØØ-Ø3 (Ø4-5)
SIZE D CODE BS NUMBER DV11-Ø-15 REV *
SCALE SHEET 5 OF 1Ø DIST.



D4-6 RDE Ø3 L
D4-6 RDE Ø2 L
D4-6 RDE Ø1 L
D4-6 RDE ØØ L
D4-3 CLR RCV FLAG Ø3 L
D4-5 ACTIVE Ø3 H
D4-6 RESET DA Ø3 L
D4-6 RESET DA Ø2 L
D4-6 RESET DA Ø1 L
D4-6 RESET DA ØØ L
D4-3 CLR RCV FLAG Ø2 L
D4-5 ACTIVE Ø2 H
D4-3 CLR RCV FLAG Ø1 L
D4-5 ACTIVE Ø1 H
D4-3 CLR RCV FLAG ØØ L
D4-5 ACTIVE ØØ H
D4-1Ø DA Ø3 L
D4-6 RCV FLAG Ø3 H
D4-1Ø DA Ø2 L
D4-6 RCV FLAG Ø2 H
D4-9 DA Ø1 L
D4-6 RCV FLAG Ø1 H
D4-9 DA ØØ L
D4-6 RCV FLAG ØØ H
DV11 BUSY Ø3
DV11 BUSY Ø2
DV11 BUSY Ø1
DV11 BUSY ØØ
ASYN H
D4-6 ENBL ERROR FLAGS L
D4-6 RCV FILE ADDRS ØØ L
D4-6 RCV FILE ADDRS Ø1 L
D4-6 RCV FILE LOAD L
D4-6 RECEIVER SAMPLE CLOCK H
D4-2 RESET L
RDE
RDE DLY
LOAD FILE
RESET DA
SAMPLE CLK
SAMPLE DELAY
WAIT DLY
(RECEIVER FLAG SERVICE)
TITLE ASYNCH MUX LINE CARD LINES ØØ-Ø3 (D4-6)
SIZE D
CODE BS
NUMBER DV11-Ø-15
REV. *
SHEET 6 OF 1Ø

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D4-10 SERIAL OUT Ø3 H — AH2 1 — 7408 E9 3
D4-2 BREAK Ø3 (Ø) H — 2
2 — 1488 E11 3 — J1 EE — EIA XMIT DATA Ø3
EIA RCV DATA Ø3 — J1 KK — 1 — 1489 E5 3
C1Ø6 47ØPf — 2
D4-2 MAINT Ø3 H — 2 — 8094 E17 3 — 1
D4-2 HALF DUPLEX Ø3 H — 1 — 7408 E19 3
D4-1Ø EOC Ø3 L — (EF2) 2
1 — 7432 E3 3 — 2 — 8093 E18 3 — 1
D4-5 ACTIVE Ø3 L — 1 — 7432 E22 3 — BK1 — D4-7 SERIAL IN Ø3 H
2

D4-10 SERIAL OUT Ø2 H — AT2 4 — 7408 E9 6
D4-2 BREAK Ø2 (Ø) H — 5
4 — 1488 E11 6 — J1 CC — EIA XMIT DATA Ø2
EIA RCV DATA Ø2 — J1 HH — 4 — 1489 E5 6
C1Ø5 47ØPf — 5
D4-2 MAINT Ø2 H — 5 — 8094 E17 6 — 4
D4-2 HALF DUPLEX Ø2 H — 4 — 7408 E19 6
D4-1Ø EOC Ø2 L — (EK2) 5
4 — 7432 E3 6 — 5 — 8093 E18 6 — 4
D4-5 ACTIVE Ø2 L — 4 — 7432 E22 6 — BK2 — D4-7 SERIAL IN Ø2 H
5

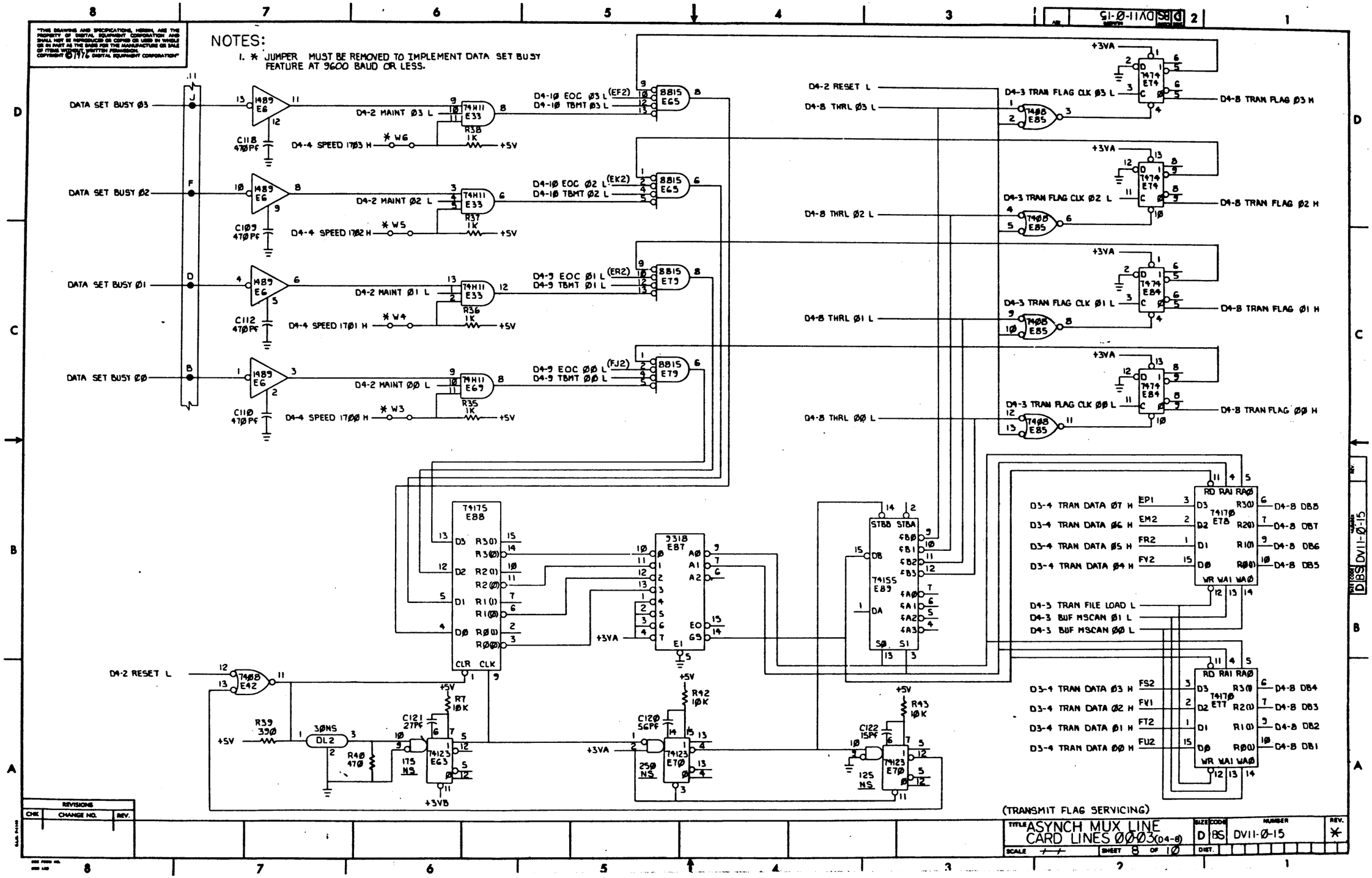
D4-9 SERIAL OUT Ø1 H — A81 9 — 7408 E9 8
D4-2 BREAK Ø1 (Ø) H — 1Ø
9 — 1488 E11 8 — J1 T — EIA XMIT DATA Ø1
EIA RCV DATA Ø1 — J1 N — 1Ø — 1489 E5 8
C128 47ØPf — 9
D4-2 MAINT Ø1 H — 9 — 8094 E17 8 — 1Ø
D4-2 HALF DUPLEX Ø1 H — 9 — 7408 E19 8
D4-9 EOC Ø1 L — (ER2) 1Ø
9 — 7432 E3 8 — 9 — 8093 E18 8 — 1Ø
D4-5 ACTIVE Ø1 L — 9 — 7432 E22 8 — BD1 — D4-7 SERIAL IN Ø1 H
1Ø

D4-9 SERIAL OUT ØØ H — AJ2 12 — 7408 E9 11
D4-2 BREAK ØØ (Ø) H — 13
12 — 1488 E11 11 — J1 R — EIA XMIT DATA ØØ
EIA RCV DATA ØØ — J1 L — 13 — 1489 E5 11
C129 47Ø PF — 12
D4-2 MAINT ØØ H — 12 — 8094 E17 11 — 13
D4-2 HALF DUPLEX ØØ H — 12 — 7408 E19 11
D4-9 EOC ØØ L — (KJ2) 13
12 — 7432 E3 11 — 12 — 8093 E18 11 — 13
D4-5 ACTIVE ØØ L — 12 — 7432 E22 11 — BF2 — D4-7 SERIAL IN ØØ H
13

(EIA IN & OUT. HALF DUPLEX. BREAK. MAINT LOGIC)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
ASYNCH MUX LINE CARD LINES ØØ-Ø3 (Ø4-7)	D	BS	DV11-Ø-15	*
SCALE —	SHEET 7 OF 1Ø	DIST.		


NOTES:
1. * JUMPER MUST BE REMOVED TO IMPLEMENT DATA SET BUSY FEATURE AT 9600 BAUD OR LESS.
DATA SET BUSY Ø3
DATA SET BUSY Ø2
DATA SET BUSY Ø1
DATA SET BUSY ØØ
D4-2 MAINT Ø3 L
D4-4 SPEED 17Ø3 H
D4-2 MAINT Ø2 L
D4-4 SPEED 17Ø2 H
D4-2 MAINT Ø1 L
D4-4 SPEED 17Ø1 H
D4-2 MAINT ØØ L
D4-4 SPEED 17ØØ H
D4-1Ø EOC Ø3 L
D4-1Ø TBMT Ø3 L
D4-1Ø EOC Ø2 L
D4-1Ø TBMT Ø2 L
D4-9 EOC Ø1 L
D4-9 TBMT Ø1 L
D4-9 EOC ØØ L
D4-9 TBMT ØØ L
D4-2 RESET L
D4-8 THRL Ø3 L
D4-8 THRL Ø2 L
D4-8 THRL Ø1 L
D4-8 THRL ØØ L
D4-3 TRAN FLAG CLK Ø3 L
D4-3 TRAN FLAG CLK Ø2 L
D4-3 TRAN FLAG CLK Ø1 L
D4-3 TRAN FLAG CLK ØØ L
D4-8 TRAN FLAG Ø3 H
D4-8 TRAN FLAG Ø2 H
D4-8 TRAN FLAG Ø1 H
D4-8 TRAN FLAG ØØ H
D3-4 TRAN DATA Ø7 H
D3-4 TRAN DATA Ø6 H
D3-4 TRAN DATA Ø5 H
D3-4 TRAN DATA Ø4 H
D4-3 TRAN FILE LOAD L
D4-3 BUF MSCAN Ø1 L
D4-3 BUF MSCAN ØØ L
D3-4 TRAN DATA Ø3 H
D3-4 TRAN DATA Ø2 H
D3-4 TRAN DATA Ø1 H
D3-4 TRAN DATA ØØ H
D4-8 DB8
D4-8 DB7
D4-8 DB6
D4-8 DB5
D4-8 DB4
D4-8 DB3
D4-8 DB2
D4-8 DB1
(TRANSMIT FLAG SERVICING)
ASYNCH MUX LINE CARD LINES ØØØ3 (D4-8)
D BS DV11-Ø-15
SHEET 8 OF 1Ø

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D4-9 RD8
D4-9 RD7
D4-9 RD6
D4-9 RD5
D4-9 RD4
D4-9 RD3
D4-9 RD2
D4-9 RD1

D4-7 SERIAL IN ØØ H — BF2 20 — SERIAL IN
D4-6 RESET DA ØØ L — 18 — CLR R DONE
D4-6 RDE ØØ L — 4 — STB RD
16 — STB STATUS
17 — R CLK
D4-4 CLOCK ØØ H — (DE2) 4Ø — X CLK
UART ØØ ET6
D4-8 THRL ØØ L — 23 — LD XD
33 — XD7
32 — XD6
31 — XD5
3Ø — XD4
29 — XD3
28 — XD2
27 — XD1
26 — XDØ
21 38 37 36 35 33 34 — CLR NB1 NB2 2SB NP EP LDC

R DONE — 19 — 1 — 74Ø4 E8Ø — 2 — D4-9 DA ØØ L
OR ERR — 15 — D4-9 OR ØØ
FR ERR — 14 — D4-9 FE ØØ
P ERR — 13 — D4-9 PE ØØ
RD 7 — 5
RD 6 — 6
RD 5 — 7
RD 4 — 8
RD 3 — 9
RD 2 — 10
RD 1 — 11
RD Ø — 12
SERIAL OUT — 25 — AJ2 — D4-9 SERIAL OUT ØØ H
XRDY — 22 — 11 — 74Ø4 ET3 — 1Ø — D4-9 TBMT ØØ L
EOC — 24 — 9 — 74Ø4 E8Ø — 8 — FJ2 — D4-9 EOC ØØ L

D4-7 SERIAL IN Ø1 H — (BD1) 2Ø — SERIAL IN
D4-6 RESET DA Ø1 L — 18 — CLR R DONE
D4-6 RDE Ø1 L — 4 — STB RD
16 — STB STATUS
17 — R CLK
D4-4 CLOCK Ø1 H — (CE2) 4Ø — X CLK
UART Ø1 E81
D4-8 THRL Ø1 L — 23 — LD XD
33 — XD7
32 — XD6
31 — XD5
3Ø — XD4
29 — XD3
28 — XD2
27 — XD1
26 — XDØ
21 38 37 36 35 33 34 — CLR NB1 NB2 2SB NP EP LDC

R DONE — 19 — 3 — 74Ø4 E8Ø — 4 — D4-9 DA Ø1 L
OR ERR — 15 — D4-9 OR Ø1
FR ERR — 14 — D4-9 FE Ø1
P ERR — 13 — D4-9 PE Ø1
RD7 — 5
RD6 — 6
RD5 — 7
RD4 — 8
RD3 — 9
RD2 — 10
RD1 — 11
RDØ — 12
SERIAL OUT — 25 — AB1 — D4-9 SERIAL OUT Ø1 H
XRDY — 22 — 11 — 74Ø4 E8Ø — 1Ø — D4-9 TBMT Ø1 L
EOC — 24 — 13 — 74Ø4 E8Ø — 12 — ER2 — D4-9 EOC Ø1 L

D4-8 DB8
D4-8 DB7
D4-8 DB6
D4-8 DB5
D4-8 DB4
D4-8 DB3
D4-8 DB2
D4-8 DB1

D4-2 RESET H
D4-2 BUF LCR 11 H
D4-2 BUF LCR 12 H
D4-2 BUF LCR 13 H
D4-2 PEN L
D4-2 PEV ØØ H
D4-2 UART STROBE ØØ H
D4-2 PEV Ø1 H
D4-2 UART STROBE Ø1 H

(UARTS ØØ & Ø1)

REVISIONS
CHK | CHANGE NO. | REV.

TITLE ASYNCH MUX LINE CARD LINESØØ-Ø3(D4-9)
SIZE D | CODE BS | NUMBER DV11-Ø-15 | REV. *
SCALE | SHEET 9 OF 1Ø | DIST.

DIRS/DV11-Ø-15

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D4-9 RDB
D4-9 RD7
D4-9 RD6
D4-9 RD5
D4-9 RD4
D4-9 RD3
D4-9 RD2
D4-9 RD1

1 7404 E66 2 D4-1Ø DA Ø2 L

D4-7 SERIAL IN Ø2 H (RK2) 2Ø
D4-6 RESET DA Ø2 L 18
D4-6 RDE Ø2 L 4
16 STB STATUS
17 R CLK
D4-4 CLOCK Ø2 H (DS2) 4Ø X CLK

UART Ø2 E67

SERIAL IN
CLR R DONE
STB RD
STB STATUS
R CLK
X CLK
LD XD
XD7
XD6
XD5
XD4
XD3
XD2
XD1
XDØ
CLR NBI NB2 2SB NP EP LDC

R DONE 19
OR ERR 15 D4-1Ø OR Ø2
FR ERR 14 D4-1Ø FE Ø2
P ERR 13 D4-1Ø PE Ø2
RD7 5
RD6 6
RD5 7
RD4 8
RD3 9
RD2 1Ø
RD1 11
RDØ 12

D4-8 THRL Ø2 L 23
SERIAL OUT 25 AT2 D4-1Ø SERIAL OUT Ø2 H
XRDY 22
EOC 24

5 7404 E66 6 D4-1Ø TBMT Ø2 L

9 7404 E66 8 EK2 D4-1Ø EOC Ø2 L

3 7404 E66 4 D4-1Ø DA Ø3 L

D4-7 SERIAL IN Ø3 H (BK1) 2Ø
D4-6 RESET DA Ø3 L 18
D4-6 RDE Ø3 L 4
16 STB STATUS
17 R CLK
D4-4 CLOCK Ø3 H (CP2) 4Ø X CLK

UART Ø3 E62

SERIAL IN
CLR R DONE
STB RD
STB STATUS
R CLK
X CLK
LD XD
XD7
XD6
XD5
XD4
XD3
XD2
XD1
XDØ
CLR NBI NB2 2SB NP EP LDC

R DONE 19
OR ERR 15 D4-1Ø OR Ø3
FR ERR 14 D4-1Ø FE Ø3
P ERR 13 D4-1Ø PE Ø3
RD7 5
RD6 6
RD5 7
RD4 8
RD3 9
RD2 1Ø
RD1 11
RDØ 12

D4-8 THRL Ø3 L 23
SERIAL OUT 25 AH2 D4-1Ø SERIAL OUT Ø3 H
XRDY 22
EOC 24

11 7404 E66 1Ø D4-1Ø TBMT Ø3 L

13 7404 E66 12 EF2 D4-1Ø EOC Ø3 L

D4-8 DB8
D4-8 DB7
D4-8 DB6
D4-8 DB5
D4-8 DB4
D4-8 DB3
D4-8 DB2
D4-8 DB1

D4-2 RESET H
D4-2 BUF LCR 11 H
D4-2 BUF LCR 12 H
D4-2 BUF LCR 13 H
D4-2 PEN L
D4-2 PEV Ø2 H
D4-2 UART STROBE Ø2 H
D4-2 PEV Ø3 H
D4-2 UART STROBE Ø3 H

(UARTS Ø2 & Ø3)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
ASYNCH MUX LINE CARD LINES ØØ-Ø3 (Ø4-1Ø)	D	BS	DV11-Ø-15	*
SCALE —	SHEET Ø OF 1Ø		DIST.	

D BS DV11-Ø-15

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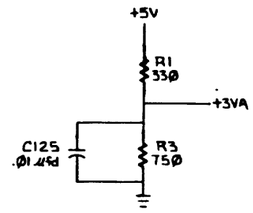
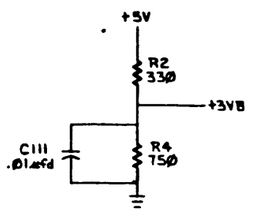
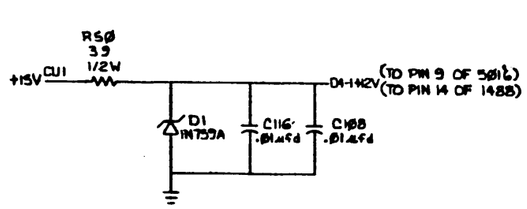
BERG CONNECTOR

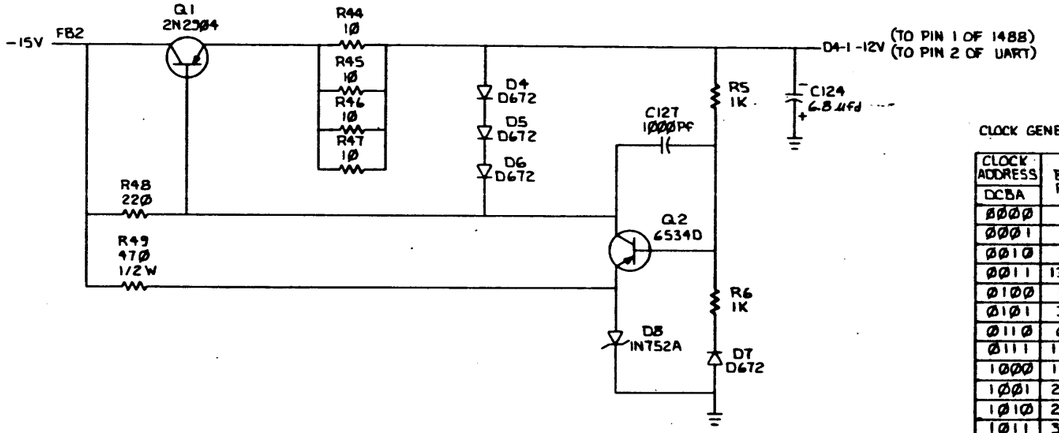
J1

DATA SET BUSY Ø4
DATA SET BUSY Ø5
DATA SET BUSY Ø6
ASYN H
DATA SET BUSY Ø7
EIA RCV DATA Ø4
EIA RCV DATA Ø5
EIA XMIT DATA Ø4
EIA XMIT DATA Ø5
DV11 BUSY Ø4
DV11 BUSY Ø5
DV11 BUSY Ø6
DV11 BUSY Ø7
EIA XMIT DATA Ø6
EIA XMIT DATA Ø7
EIA RCV DATA Ø6
EIA RCV DATA Ø7



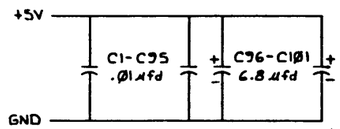






CLOCK GENERATION CHART

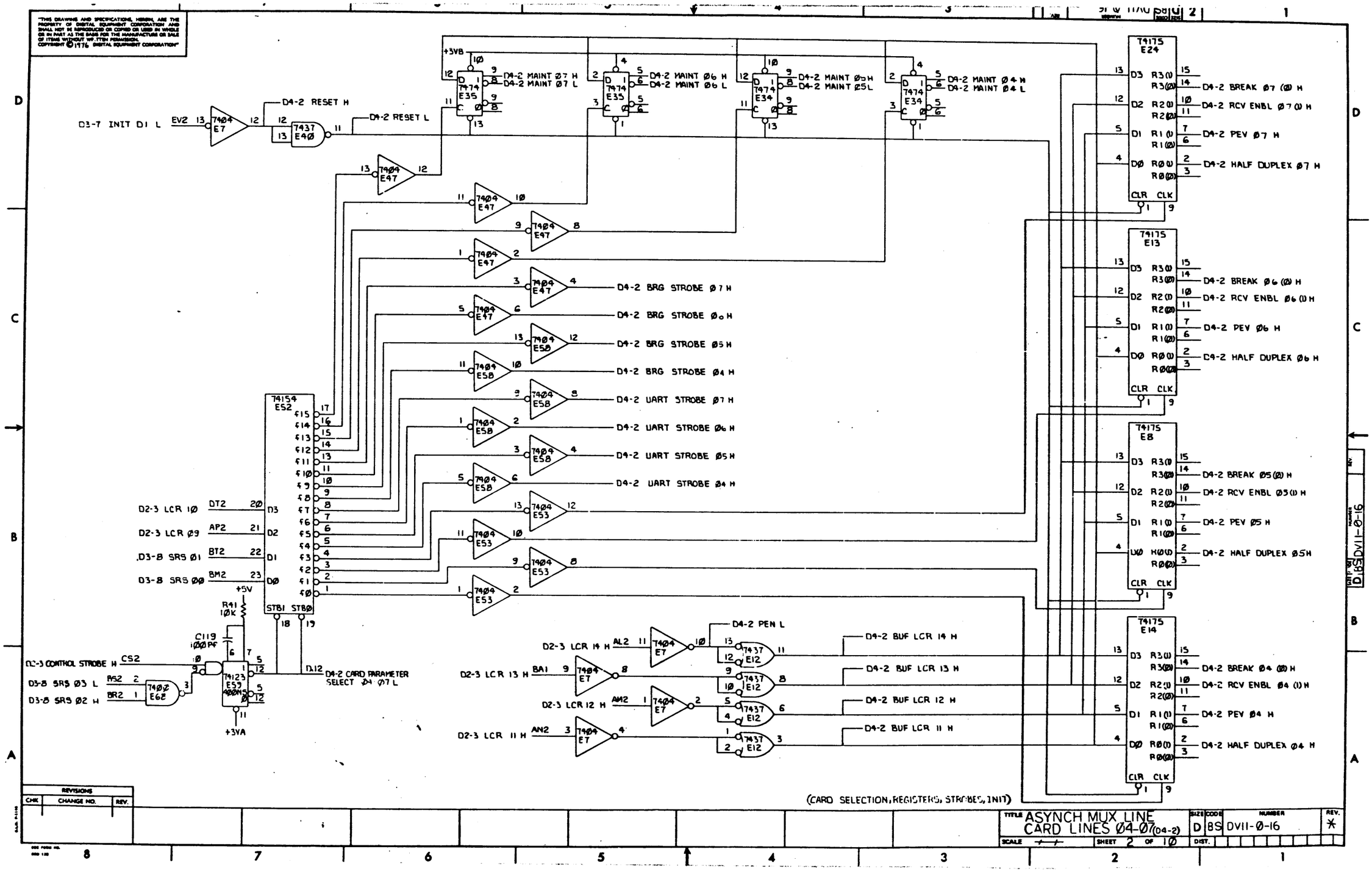
CLOCK ADDRESS DCBA	BAUD RATE	PERIOD (USEC)
ØØØØ	50	1250.00
ØØØ1	75	833.33
ØØ1Ø	110	568.18
ØØ11	134.5	464.68
Ø1ØØ	150	416.67
Ø1Ø1	300	208.33
Ø11Ø	600	104.17
Ø111	1200	52.08
1ØØØ	1800	34.72
1ØØ1	2000	31.25
1Ø1Ø	2400	26.04
1Ø11	3600	17.36
1100	4800	13.02
1101	7200	8.68
111Ø	9600	6.51
1111	38400	1.63



(CHART, REGULATORS)

DRN R Raymond	1-13-76	FIRST USED ON: DV11
CHK	1/15/76	digital
ENG.	1-15-76	TITLE: ASYNCH MUX LINE CARD LINES Ø4-Ø7 (04-1)
PROJ. ENG.	1-15-76	
PROD.	1-16-76	
NEXT HIGHER ASSY.		SIZE D · CODE BS · NUMBER DV11-Ø-16 · REV. *
B-DD-DV11-Ø		
SCALE		
SHEET	OF 10	DIST.

REVISIONS: REV. | CHANGE NO. | CHK



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REVISIONS		
CHK	CHANGE NO.	REV.

TITLE ASYNCH MUX LINE CARD LINES Ø4-Ø7 (D4-2)

SIZE D | CODE BS | NUMBER DV11-Ø-16 | REV. *

SCALE — | SHEET 2 OF 1Ø | DIST.

D BS DV11-Ø-16

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D3-4 MASTER SCAN D H
D3-4 MASTER SCAN Ø2 H
EU2
EN2
7400 E68
DM2 D4-3 CARD FLAG SELECT Ø4-Ø7 L
7404 E73
D3-3 RESYNC PULSE L
DF2
STBB STBA
DB
74155 E6Ø
SI SØ
FBØ D4-3 RESYNC PULSE Ø7 L
FB1 D4-3 RESYNC PULSE Ø6 L
FB2 D4-3 RESYNC PULSE Ø5 L
FB3 D4-3 RESYNC PULSE Ø4 L
FAØ D4-3 TRAN FLAG CLK Ø7 L
FA1 D4-3 TRAN FLAG CLK Ø6 L
FA2 D4-3 TRAN FLAG CLK Ø5 L
FA3 D4-3 TRAN FLAG CLK Ø4 L
D3-4 TRANSMITTER STROBE H
EH2
7400 E68
7404 E53
D4-3 TRAN FILE LOAD L
D4-3 BUF MSCAN Ø1 L
D4-3 BUF MSCAN ØØ L
STBØ STBI
D4-6 RCV FLAG Ø7 H
D4-6 RCV FLAG Ø6 H
D4-6 RCV FLAG Ø5 H
D4-6 RCV FLAG Ø4 H
D4-5 MATCH Ø7 (1) H
D4-5 MATCH Ø6 (1) H
D4-5 MATCH Ø5 (1) H
D4-5 MATCH Ø4 (1) H
AI BI CI DI
AØ BØ CØ DØ
SI SØ
74153 E37
7432 ET2
8881 E82
FM2 RECEIVER FLAG L
FE1 MATCH DETECT L
+5V
RB 10K
D1-5 RECEIVED DATA ENABLE H
CN2
7400 E68
74123 E63
TS NS
FJ1 D4-3 RDE Ø4-Ø7
+3VB
FK1 D4-3 DATA ENABLE Ø4-Ø7 H
7474 E36
D4-3 MATCH H
7437 E4Ø
D4-2 RESET L
STBB STBA
DB
74155 E31
SI SØ
FBØ D4-3 CLR RCV FLAG Ø7 L
FB1 D4-3 CLR RCV FLAG Ø6 L
FB2 D4-3 CLR RCV FLAG Ø5 L
FB3 D4-3 CLR RCV FLAG Ø4 L
FAØ D4-3 CLR MATCH Ø7 L
FA1 D4-3 CLR MATCH Ø6 L
FA2 D4-3 CLR MATCH Ø5 L
FA3 D4-3 CLR MATCH Ø4 L
D3-4 MASTER SCAN Ø1 H
EM1
7404 ET3
D3-4 MASTER SCAN ØØ H
EN1
7404 ET3
STBI STBØ
D4-8 TRAN FLAG Ø7 H
D4-8 TRAN FLAG Ø6 H
D4-8 TRAN FLAG Ø5 H
D4-8 TRAN FLAG Ø4 H
AI BI CI DI
AØ BØ CØ DØ
SI SØ
74153 E83
8881 E82
FL2 TRAN FLAG WAITING L
D3-4 MASTER SCAN T/R
CR2
7404 ET3

(SCAN SELECTION. FLAGS)

REVISIONS
CHK | CHANGE NO. | REV.

TITLE ASYNCH MUX LINE CARD LINES Ø4-Ø7(Ø4-3)
SIZE D | CODE BS | NUMBER DV11-Ø-16 | REV. *
SCALE | SHEET 3 OF 1Ø | DIST.

DBS DV11-Ø-16

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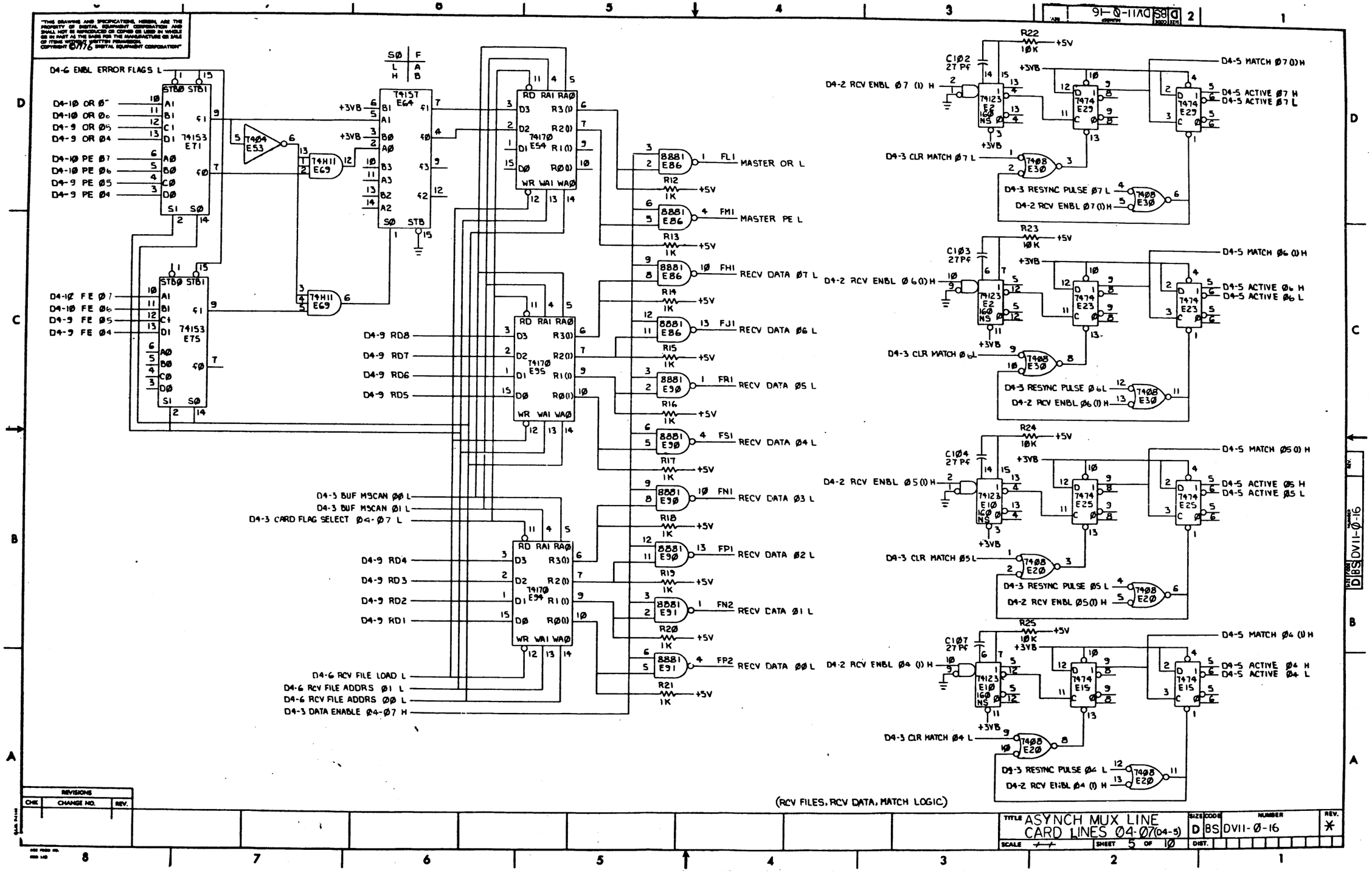
R9 10K
R10 10K
C126 22PF
C123 22PF
7380 E93
7380 E93
Y1 2.457G MHZ
R11 1K
C200 22PF
7404 E80
W2 (W2 REMOVED FOR AUTOMATED MODULE TEST)
D4-2 RESET H
7493 E92
R3(1) R2(1) R1(1) R0(1) CLR CLK0 CLKBC
BN2 D4-4 SOURCE CLOCK B Ø4-Ø7 L
D4-2 BUF LCR 14 H
D4-2 BUF LCR 13 H
D4-2 BUF LCR 12 H
D4-2 BUF LCR 11 H
COM 5016 E51
TD TC TB TA STT EXT2 EXT1 RD RC RB RA STR 4T 4R
D4-1 +12V
5Ø.ØMHZ E27
+5V
W1 (W1 REMOVED FOR AUTOMATED MODULE TEST)
BJ1 D4-4 SOURCE CLOCK A Ø4-Ø7 L
7437 E46
7437 E46
COM 5016 E51
COM 5016 E51
+3VA
7474 E45
7474 E45
7474 E55
7474 E55
D4-4 SPEED 17Ø7 H
D4-4 SPEED 17Ø6 H
D4-4 SPEED 17Ø5 H
D4-4 SPEED 17Ø4 H
7420 E39
D4-2 BRG STROBE Ø7 H
D4-2 BRG STROBE Ø6 H
D4-2 BRG STROBE Ø5H
D4-2 BRG STROBE Ø4 H
D4-2 RESET L
8034 E56
8093 E50
CP2 D4-4 CLOCK Ø7 H
DS2 D4-4 CLOCK Ø6 H
CE2 D4-4 CLOCK Ø5 H
DE2 D4-4 CLOCK Ø4 H

(CRYSTAL, CLOCK GENERATION)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
ASYNCH MUX LINE CARD LINES Ø4-Ø7(04-4)	D	BS	DV11-Ø-16	*
SCALE	SHEET 4 OF 10	DIST.		



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REVISIONS		
CHK	CHANGE NO.	REV.

TITLE ASYNCH MUX LINE CARD LINES Ø4-Ø7 (D4-5)

SIZE D | CODE BS | NUMBER DV11-Ø-16 | REV. *

SCALE — | SHEET 5 OF 10 | DIST.

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+3VA
+3VB
+5V
D4-1Ø DA Ø7 L
D4-6 RCV FLAG Ø7 H
D4-3 CLR RCV FLAG Ø7 L
D4-5 ACTIVE Ø7 H
D4-6 RESET DA Ø7 L
D4-1Ø DA Ø6 L
D4-6 RCV FLAG Ø6 H
D4-3 CLR RCV FLAG Ø6 L
D4-5 ACTIVE Ø6 H
D4-9 DA Ø5 L
D4-6 RCV FLAG Ø5 H
D4-3 CLR RCV FLAG Ø5 L
D4-5 ACTIVE Ø5 H
D4-9 DA Ø4 L
D4-6 RCV FLAG Ø4 H
D4-3 CLR RCV FLAG Ø4 L
D4-5 ACTIVE Ø4 H
D4-6 RESET DA Ø6 L
D4-6 RESET DA Ø5 L
D4-6 RESET DA Ø4 L
D4-6 RDE Ø7 L
D4-6 RDE Ø6 L
D4-6 RDE Ø5 L
D4-6 RDE Ø4 L
DV11 BUSY Ø7
DV11 BUSY Ø6
DV11 BUSY Ø5
DV11 BUSY Ø4
ASYN H
D4-6 ENBL ERROR FLAGS, L
D4-6 RCV FILE ADDRS ØØ L
D4-6 RCV FILE ADDRS Ø1 L
D4-6 RCV FILE LOAD L
D4-6 RECEIVER SAMPLE CLOCK H
D4-2 RESET L
RDE
RDE DLY
LOAD FILE
WAIT DLY
SAMPLE CLK
SAMPLE DELAY
RESET DA
(RECEIVER FLAG SERVICE)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
ASYNCH MUX LINE CARD LINES Ø4-Ø7 (04-6)	D	BS	DV11-Ø-16	*
SCALE	SHEET 6 OF 1Ø		DIST.	

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D4-10 SERIAL OUT Ø7 H — AH2 — T4Ø8 E9
D4-2 BREAK Ø7 (Ø) H
1488 E11 — EIA XMIT DATA Ø7
EIA RCV DATA Ø7 — 1489 E5 — C1Ø6 47ØPf
J1 EE / KK
D4-2 MAINT Ø 7H — 8Ø94 E17 — 8Ø93 E18
D4-2 HALF DUPLEX Ø 7 H — T4Ø8 E19 (EF2)
D4-1Ø EOC Ø7 L — T432 E3
D4-5 ACTIVE Ø7 L — T432 E22 — BK1 — D4-7 SERIAL IN Ø7 H

D4-10 SERIAL OUT Ø6 H — AT2 — T4Ø8 E9
D4-2 BREAK Ø6 (Ø) H
1488 E11 — EIA XMIT DATA Ø6
EIA RCV DATA Ø6 — 1489 E5 — C1Ø5 47ØPf
J1 CC / HH
D4-2 MAINT Ø 6H — 8Ø94 E17 — 8Ø93 E18
D4-2 HALF DUPLEX Ø6 H — T4Ø8 E19 (EK2)
D4-1Ø EOC Ø6 L — T432 E3
D4-5 ACTIVE Ø6 L — T432 E22 — BK2 — D4-7 SERIAL IN Ø6 H

D4-9 SERIAL OUT Ø5 H — AB1 — T4Ø8 E9
D4-2 BREAK Ø5(Ø)H
1488 E11 — EIA XMIT DATA Ø5
EIA RCV DATA Ø5 — 1489 E5 — C128 47ØPf
J1 T / N
D4-2 MAINT Ø5 H — 8Ø94 E17 — 8Ø93 E18
D4-2 HALF DUPLEX Ø5 H — T4Ø8 E19 (ER2)1Ø
D4-9 EOC Ø5 L — T432 E3
D4-5 ACTIVE Ø5 L — T432 E22 — BD1 — D4-7 SERIAL IN Ø5 H

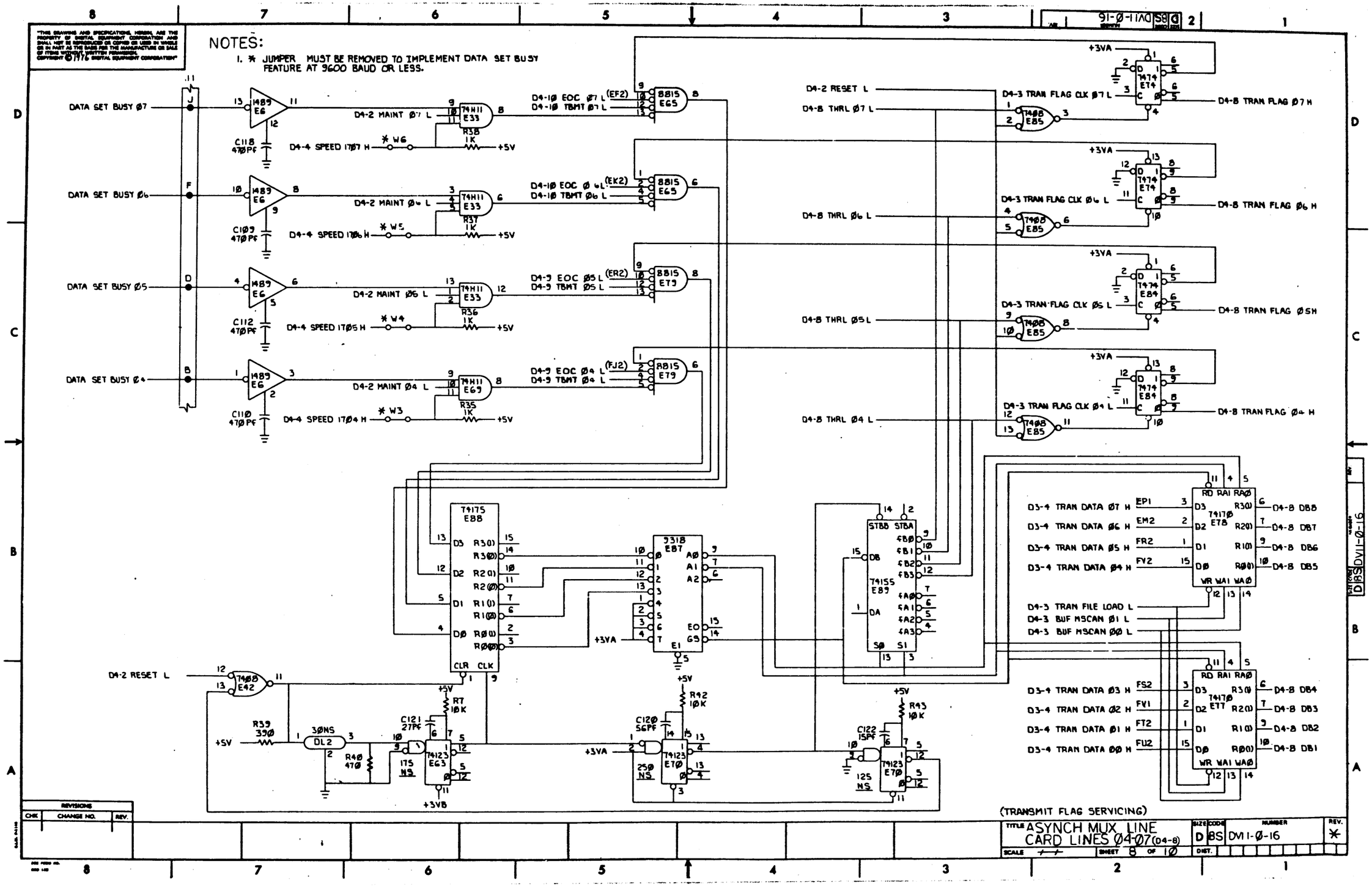
D4-9 SERIAL OUT Ø4 H — A12 — T4Ø8 E9
D4-2 BREAK Ø4 (Ø) H
1488 E11 — EIA XMIT DATA Ø4
EIA RCV DATA Ø4 — 1489 E5 — C129 47Ø PF
J1 R / L
D4-2 MAINT Ø4 H — 8Ø94 E17 — 8Ø93 E18
D4-2 HALF DUPLEX Ø4 H — T4Ø8 E19 (FJ2)
D4-9 EOC Ø4 L — T432 E3
D4-5 ACTIVE Ø4 L — T432 E22 — BF2 — D4-7 SERIAL IN Ø4 H

(EIA IN & OUT. HALF DUPLEX, BREAK, MAINT LOGIC)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
ASYNCH MUX LINE CARD LINES Ø4-Ø7 (D4-7)	D	8S	DV11-Ø-16	*
SCALE —	SHEET 7 OF 1Ø	DIST.		

D8S DV11-Ø-16


NOTES:
1. * JUMPER MUST BE REMOVED TO IMPLEMENT DATA SET BUSY FEATURE AT 9600 BAUD OR LESS.
DATA SET BUSY Ø7
DATA SET BUSY Ø6
DATA SET BUSY Ø5
DATA SET BUSY Ø4
D4-2 MAINT Ø7 L
D4-4 SPEED 17Ø7 H
D4-2 MAINT Ø6 L
D4-4 SPEED 17Ø6 H
D4-2 MAINT Ø5 L
D4-4 SPEED 17Ø5 H
D4-2 MAINT Ø4 L
D4-4 SPEED 17Ø4 H
D4-1Ø EOC Ø7 L
D4-1Ø TBMT Ø7 L
D4-1Ø EOC Ø6 L
D4-1Ø TBMT Ø6 L
D4-9 EOC Ø5 L
D4-9 TBMT Ø5 L
D4-9 EOC Ø4 L
D4-9 TBMT Ø4 L
D4-2 RESET L
D4-8 THRL Ø7 L
D4-8 THRL Ø6 L
D4-8 THRL Ø5 L
D4-8 THRL Ø4 L
D4-3 TRAN FLAG CLK Ø7 L
D4-3 TRAN FLAG CLK Ø6 L
D4-3 TRAN FLAG CLK Ø5 L
D4-3 TRAN FLAG CLK Ø4 L
D4-8 TRAN FLAG Ø7 H
D4-8 TRAN FLAG Ø6 H
D4-8 TRAN FLAG Ø5H
D4-8 TRAN FLAG Ø4 H
D3-4 TRAN DATA Ø7 H
D3-4 TRAN DATA Ø6 H
D3-4 TRAN DATA Ø5 H
D3-4 TRAN DATA Ø4 H
D4-3 TRAN FILE LOAD L
D4-3 BUF MSCAN Ø1 L
D4-3 BUF MSCAN ØØ L
D3-4 TRAN DATA Ø3 H
D3-4 TRAN DATA Ø2 H
D3-4 TRAN DATA Ø1 H
D3-4 TRAN DATA ØØ H
D4-8 DB8
D4-8 DB7
D4-8 DB6
D4-8 DB5
D4-8 DB4
D4-8 DB3
D4-8 DB2
D4-8 DB1
(TRANSMIT FLAG SERVICING)
ASYNCH MUX LINE CARD LINES Ø4-Ø7 (D4-8)
D BS DV11-Ø-16
SHEET 8 OF 1Ø

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D4-7 SERIAL IN Ø4 H (BF2) 20 SERIAL IN
D4-6 RESET DA Ø4 L 18 CLR R DONE
D4-6 RDE Ø4 L 4 STB RD
16 STB STATUS
17 R CLK
D4-4 CLOCK Ø4 H (DE2) 40 X CLK
D4-8 THRL Ø4 L 23 LD XD
33 XD7
32 XD6
31 XD5
30 XD4
29 XD3
28 XD2
27 XD1
26 XDØ
UART Ø4 E76
CLR NBI NB2 2SB NP EP LDC
21 38 37 36 35 39 34
R DONE 19
OR ERR 15 D4-9 OR Ø4
FR ERR 14 D4-9 FE Ø4
P ERR 13 D4-9 PE Ø4
RD 7 5
RD 6 6
RD 5 7
RD 4 8
RD 3 9
RD 2 10
RD 1 11
RD Ø 12
SERIAL OUT 25 A12 D4-9 SERIAL OUT Ø4 H
XRDY 22 11 T4Ø4 E73 1Ø D4-9 TBMT Ø4 L
EOC 24 9 T4Ø4 E8Ø 8 FJ2 D4-9 EOC Ø4 L
1 T4Ø4 E8Ø 2 D4-9 DA Ø4 L

D4-9 RD8
D4-9 RD7
D4-9 RD6
D4-9 RD5
D4-9 RD4
D4-9 RD3
D4-9 RD2
D4-9 RD1

D4-8 DB8
D4-8 DB7
D4-8 DB6
D4-8 DB5
D4-8 DB4
D4-8 DB3
D4-8 DB2
D4-8 DB1

D4-2 RESET H
D4-2 BUF LCR 11 H
D4-2 BUF LCR 12 H
D4-2 BUF LCR 13 H
D4-2 PEN L
D4-2 PEV Ø4 H
D4-2 UART STROBE Ø4 H
D4-2 PEV Ø5 H
D4-2 UART STROBE Ø5 H

D4-7 SERIAL IN Ø5 H (BD1) 20 SERIAL IN
D4-6 RESET DA Ø5L 18 CLR R DONE
D4-6 RDE Ø5 L 4 STB RD
16 STB STATUS
17 R CLK
D4-4 CLOCK Ø5 H (CE2) 40 X CLK
D4-8 THRL Ø5 L 23 LD XD
33 XD7
32 XD6
31 XD5
30 XD4
29 XD3
28 XD2
27 XD1
26 XDØ
UART Ø5 E81
CLR NBI NB2 2SB NP EP LDC
21 38 37 36 35 39 34
R DONE 19
OR ERR 15 D4-9 OR Ø5
FR ERR 14 D4-9 FE Ø5
P ERR 13 D4-9 PE Ø5
RD7 5
RD6 6
RD5 7
RD4 8
RD3 9
RD2 10
RD1 11
RDØ 12
SERIAL OUT 25 AB1 D4-9 SERIAL OUT Ø5H
XRDY 22 11 T4Ø4 E8Ø 1Ø D4-9 TBMT Ø5 L
EOC 24 13 T4Ø4 E8Ø 12 ER2 D4-9 EOC Ø5L
3 T4Ø4 E8Ø 2 D4-9 DA Ø5 L

(UARTS Ø4 & Ø5)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE ASYNCH MUX LINE CARD LINES Ø4-Ø7(04-9)
SIZE D CODE 8S NUMBER DV11-Ø-16 REV. *
SCALE SHEET 9 OF 1Ø DIST.

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D4-9 RDB
D4-9 RD7
D4-9 RD6
D4-9 RD5
D4-9 RD4
D4-9 RD3
D4-9 RD2
D4-9 RD1

1 7404 E66 2 D4-10 DA Ø6 L

D4-7 SERIAL IN Ø6 H (BK2) 20 SERIAL IN
D4-6 RESET DA Ø6 L 18 CLR R DONE
D4-6 RDE Ø6 L 4 STB RD
16 STB STATUS
17 R CLK
D4-4 CLOCK Ø6 H (DS2) 40 X CLK

UART Ø6 E67

D4-8 THRL Ø6 L 23 LD XD
33 XD7
32 XD6
31 XD5
30 XD4
29 XD3
28 XD2
27 XD1
26 XDØ

R DONE 19
OR ERR 15 D4-10 OR Ø6
FR ERR 14 D4-10 FE Ø6
P ERR 13 D4-10 PE Ø6
RD7 5
RD6 6
RD5 7
RD4 8
RD3 9
RD2 10
RD1 11
RDØ 12

SERIAL OUT 25 AT2 D4-10 SERIAL OUT Ø6 H
XRDY 22 5 7404 E66 6 D4-10 TBMT Ø6 L
EOC 24

CLR NB1 NB2 23B NP EP LDC
21 38 37 36 35 39 34

9 7404 E66 8 EK2 D4-10 EOC Ø6 L

3 7404 E66 4 D4-10 DA Ø7L

D4-7 SERIAL IN Ø7 H (BK1) 20 SERIAL IN
D4-6 RESET DA Ø7 L 18 CLR R DONE
D4-6 RDE Ø7 L 4 STB RD
16 STB STATUS
17 R CLK
D4-4 CLOCK Ø7 H (CP2) 40 X CLK

UART Ø7 E62

D4-8 THRL Ø7 L 23 LD XD
33 XD7
32 XD6
31 XD5
30 XD4
29 XD3
28 XD2
27 XD1
26 XDØ

R DONE 19
OR ERR 15 D4-10 OR Ø7
FR ERR 14 D4-10 FE Ø7
P ERR 13 D4-10 PE Ø7
RD7 5
RD6 6
RD5 7
RD4 8
RD3 9
RD2 10
RD1 11
RDØ 12

SERIAL OUT 25 AH2 D4-10 SERIAL OUT Ø7 H
XRDY 22 11 7404 E66 10 D4-10 TBMT Ø7 L
EOC 24

CLR NB1 NB2 23B NP EP LDC
21 38 37 36 35 39 34

13 7404 E66 12 EF2 D4-10 EOC Ø7 L

D4-8 DB8
D4-8 DB7
D4-8 DB6
D4-8 DB5
D4-8 DB4
D4-8 DB3
D4-8 DB2
D4-8 DB1

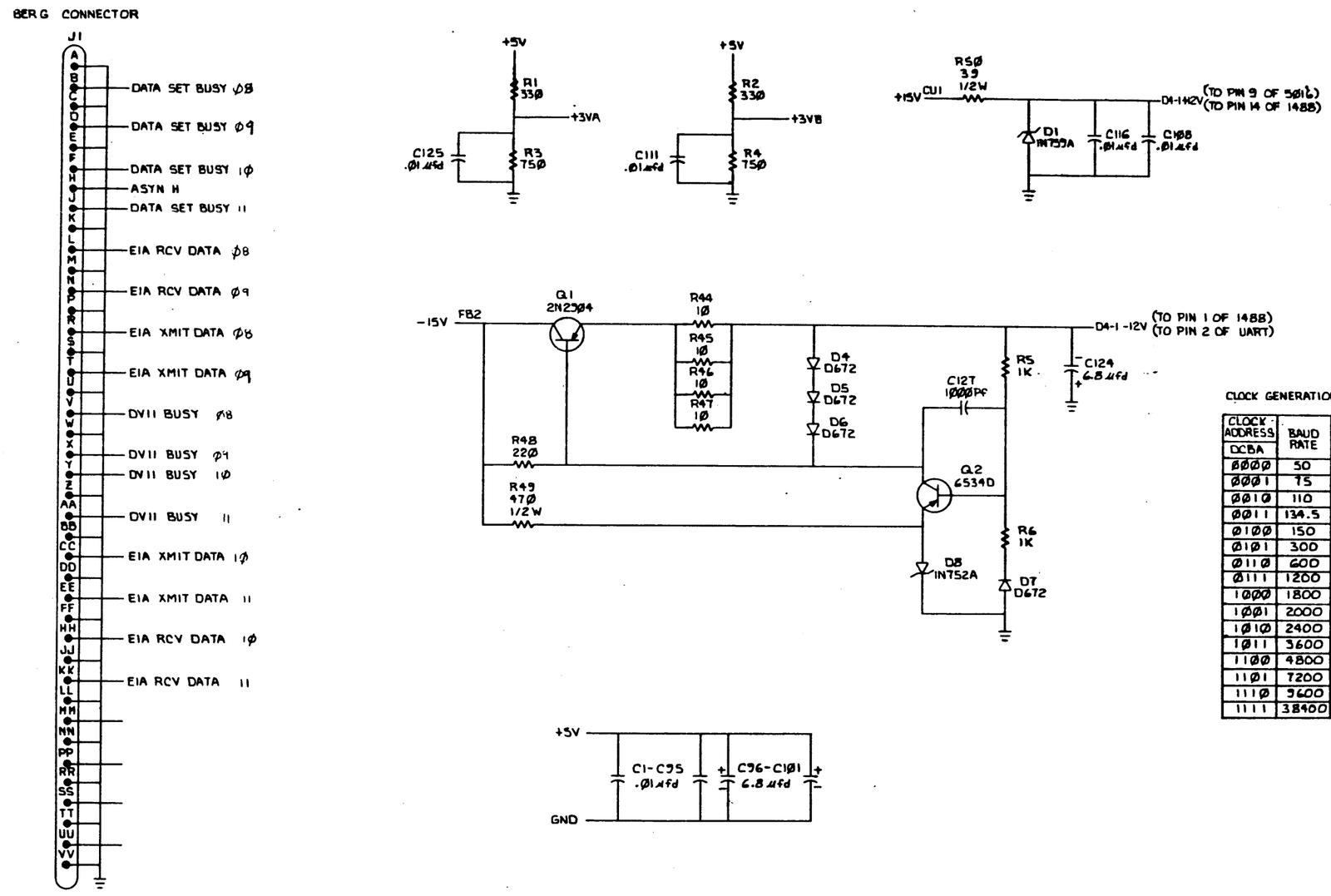
D4-2 RESET H
D4-2 BUF LCR 11 H
D4-2 BUF LCR 12 H
D4-2 BUF LCR 13 H
D4-2 PEN L
D4-2 PEV Ø6 H
D4-2 UART STROBE Ø6 H
D4-2 PEV Ø7 H
D4-2 UART STROBE Ø7 H

(UARTS Ø6 & Ø7)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
ASYNCH MUX LINE CARD LINES Ø4-07 (04-10)	D	BS	DV11-Ø-16	*
SCALE —	SHEET Ø OF 10	DIST.		

DBS DV11-Ø-16



CLOCK GENERATION CHART

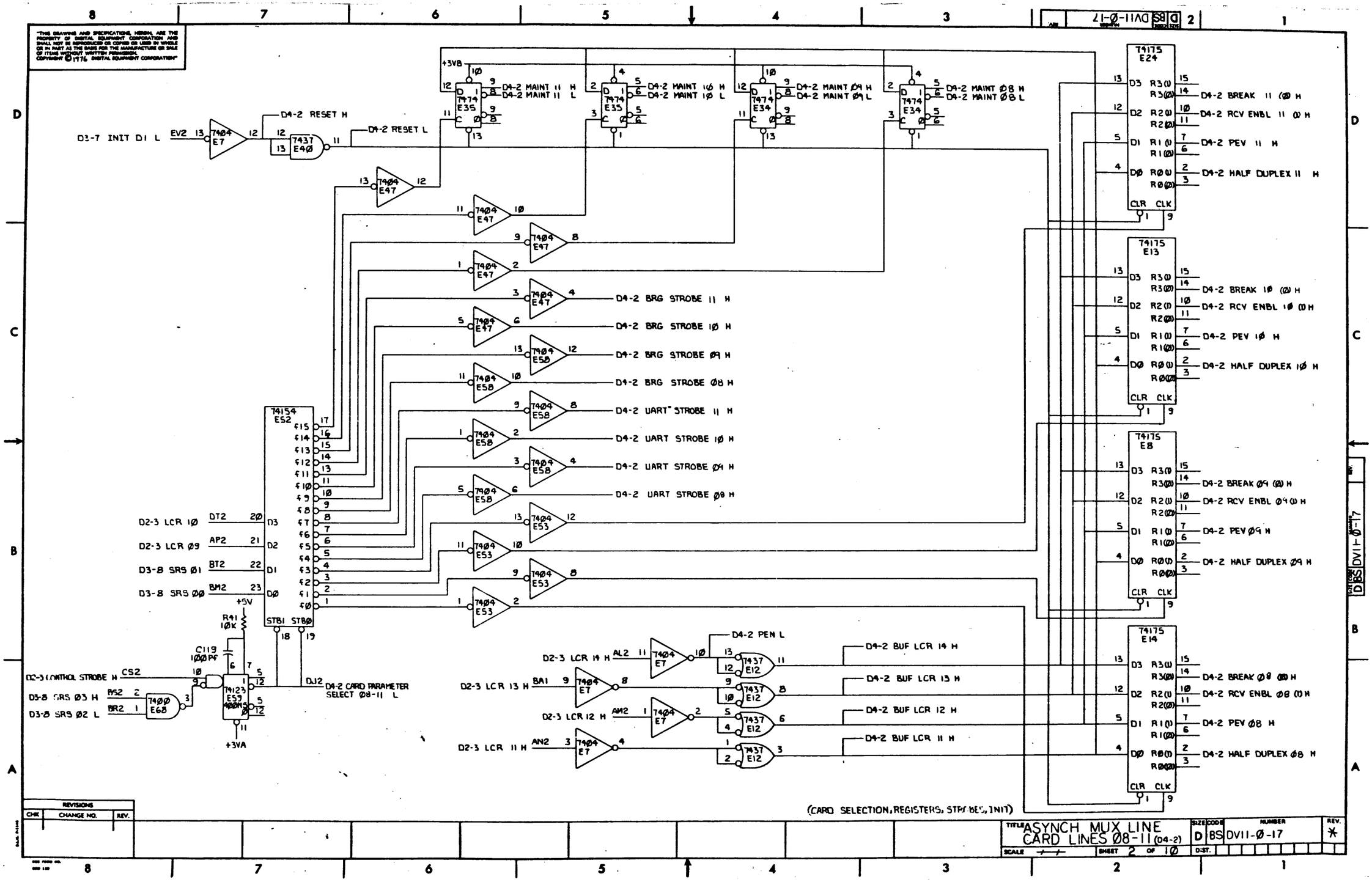
CLOCK ADDRESS DCBA	BAUD RATE	PERIOD (USEC)
ØØØØ	50	1250.00
ØØØ1	75	833.33
ØØ1Ø	110	568.18
ØØ11	134.5	464.68
Ø1ØØ	150	416.67
Ø1Ø1	300	208.33
Ø11Ø	600	104.17
Ø111	1200	52.08
1ØØØ	1800	34.72
1ØØ1	2000	31.25
1Ø1Ø	2400	26.04
1Ø11	3600	17.36
11ØØ	4800	13.02
11Ø1	7200	8.68
111Ø	9600	6.51
1111	38400	1.63

(CHART, REGULATORS)

DRN.	4-13-76	FIRST USED ON DV11
CHK.	4/15/76	digital
ENG.	4-15-76	TITLE ASYNCH MUX LINE CARD LINES Ø8-11 (D4-1)
PROJ. ENG.	4-15-76	
PROD. R. Will	4-16-76	
NEXT HIGHER ASSY.		
B-DD-DV11-Ø		SIZE D CODE BS NUMBER DV11-Ø-17 REV. *
SCALE		
SHEET	OF 1Ø	DIST.

REVISIONS CHK. CHANGE NO. REV.

DBS DV11-Ø-17



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REVISIONS		
CHK	CHANGE NO.	REV.

TITLE ASYNCH MUX LINE CARD LINES 08-11 (D4-2)

SIZE D | CODE BS | NUMBER DV11-0-17 | REV. *

SCALE | SHEET 2 OF 10 | DIST.

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D3-4 MASTER SCAN Ø3 H
D3-4 MASTER SCAN C H
EU2
EN2
7400 E68
DM2
D4-3 CARD FLAG SELECT Ø8-11 L
7404 E73
STBB STBA
D3-3 RESYNC PULSE L
DF2
DB
DA
S1 SØ
74155 E60
ƒBØ D4-3 RESYNC PULSE 11 L
ƒB1 D4-3 RESYNC PULSE 10 L
ƒB2 D4-3 RESYNC PULSE Ø9 L
ƒB3 D4-3 RESYNC PULSE Ø8 L
ƒAØ D4-3 TRAN FLAG CLK 11 L
ƒA1 D4-3 TRAN FLAG CLK 10 L
ƒA2 D4-3 TRAN FLAG CLK Ø9 L
ƒA3 D4-3 TRAN FLAG CLK Ø8 L
D4-3 BUF MSCAN Ø1 L
D4-3 BUF MSCAN ØØ L
D3-4 TRANSMITTER STROBE H
EH2
7400 E68
7404 E53
D4-3 TRAN FILE LOAD L
STBØ STB1
AI BI CI DI
AØ BØ CØ DØ
74153 E37
ƒI ƒØ
D4-6 RCV FLAG 11 H
D4-6 RCV FLAG 10 H
D4-6 RCV FLAG Ø9 H
D4-6 RCV FLAG Ø8 H
D4-5 MATCH 11 (1) H
D4-5 MATCH 10 (1) H
D4-5 MATCH Ø9 (1) H
D4-5 MATCH Ø8 (1) H
7432 ET2
8881 E82
FM2
RECEIVER FLAG L
+5V
R8 10K
D1-5 RECEIVED DATA ENABLE H
CN2
7400 E68
74123 E63
FU1
D4-3 RDE Ø8-11
+3VB
FK1
D4-3 DATA ENABLE Ø8-11 H
D4-3 MATCH H
7474 E36
7437 E40
D4-2 RESET L
8881 E82
FE1
MATCH DETECT L
STBB STBA
DB
DA
S1 SØ
74155 E31
ƒBØ D4-3 CLR RCV FLAG 11 L
ƒB1 D4-3 CLR RCV FLAG 10 L
ƒB2 D4-3 CLR RCV FLAG Ø9 L
ƒB3 D4-3 CLR RCV FLAG Ø8 L
ƒAØ D4-3 CLR MATCH 11 L
ƒA1 D4-3 CLR MATCH 10 L
ƒA2 D4-3 CLR MATCH Ø1 L
ƒA3 D4-3 CLR MATCH Ø8 L
D3-4 MASTER SCAN Ø1 H
EM1
7404 ET3
D3-4 MASTER SCAN ØØ H
EN1
7404 ET3
STBI STBØ
AI BI CI DI
AØ BØ CØ DØ
74153 E83
ƒI ƒØ
D4-8 TRAN FLAG 11 H
D4-8 TRAN FLAG 10 H
D4-8 TRAN FLAG Ø9 H
D4-8 TRAN FLAG Ø8 H
8881 E82
FL2
TRAN FLAG WAITING L
D3-4 MASTER SCAN T/R
CR2
7409 ET3
(SCAN SELECTION. FLAGS)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
ASYNCH MUX LINE CARD LINES Ø8-11 (D4-3)	D	BS	DV11-Ø-17	*
SCALE	SHEET 3 OF 10		DIST.	

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R9 10K
R10 10K
C126 22PF
C123 22PF
7380 E93
7380 E95
Y1 2.4576 MHZ
R11 1K
C200 22PF
7404 E80
W2
(W2 REMOVED FOR AUTOMATED MODULE TEST)
D4-2 RESET H
7493 E92
R3(1)
R2(1)
R1(1)
R0(1)
CLR
CLK0 CLKBC
BN2
D4-4 SOURCE CLOCK B Ø8-11 L
D4-2 BUF LCR 14 H
D4-2 BUF LCR 13 H
D4-2 BUF LCR 12 H
D4-2 BUF LCR 11 H
COM 5016 E51
TD TC TB TA STT EXT2 EXT1 RD RC RB RA STR
4T 4R
D4-1 +12V
BJ1
D4-4 SOURCE CLOCK A Ø8-11 L
5.0688 MHZ E27
+5V
W1
(W1 REMOVED FOR AUTOMATED MODULE TEST)
7437 E46
7437 E46
COM 5016 E57
D4-1 +12V
+3VA
7474 E45
7474 E45
7474 E55
7474 E55
7420 E39
D4-2 BRG STROBE 11 H
D4-2 BRG STROBE Ø H
D4-2 BRG STROBE Ø9 H
D4-2 BRG STROBE ØB H
D4-2 RESET L
8Ø74 E56
8Ø93 E50
CP2 D4-4 CLOCK 11 H
DS2 D4-4 CLOCK 1Ø H
CE2 D4-4 CLOCK Ø9 H
DE2 D4-4 CLOCK Ø8 H
D4-4 SPEED 1713 H
D4-4 SPEED 1712 H
D4-4 SPEED 1711 H
D4-4 SPEED 1710 H

REVISIONS		
CHK	CHANGE NO.	REV.

(CRYSTAL. CLOCK GENERATION)

TITLE	SIZE	CODE	NUMBER	REV.
ASYNCH MUX LINE CARD LINES Ø8-11 (D4-4)	D	BS	DV11-Ø-17	*
SCALE —	SHEET 4 OF 1Ø	DIST.		

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D4-6 ENBL ERROR FLAGS L

D4-1Ø OR 11
D4-1Ø OR 1Ø
D4-9 OR Ø9
D4-9 OR Ø8
D4-1Ø PE 11
D4-1Ø PE 1Ø
D4-9 PE Ø9
D4-9 PE Ø8

74153 E71

D4-1Ø FE 11
D4-1Ø FE 1Ø
D4-9 FE Ø9
D4-9 FE Ø8

74153 E75

74Ø4 E53
74H11 E69
74H11 E69

S Ø / L H — F / A B

74157 E64

+3VB
+3VB

D4-9 RD8
D4-9 RD7
D4-9 RD6
D4-9 RD5

D4-3 BUF MSCAN Ø Ø L
D4-3 BUF MSCAN Ø 1 L
D4-3 CARD FLAG SELECT 2 L

D4-9 RD4
D4-9 RD3
D4-9 RD2
D4-9 RD1

D4-6 RCV FILE LOAD L
D4-6 RCV FILE ADDRS Ø1 L
D4-6 RCV FILE ADDRS ØØ L
D4-3 DATA ENABLE Ø8-11 H

74170 E54
74170 E55
74170 E54

8881 E86 — FL1 MASTER OR L
8881 E86 — FM1 MASTER PE L
8881 E86 — FH1 RECV DATA Ø7 L
8881 E86 — FJ1 RECV DATA Ø6 L
8881 E9Ø — FR1 RECV DATA Ø5 L
8881 E9Ø — FS1 RECV DATA Ø4 L
8881 E9Ø — FN1 RECV DATA Ø3 L
8881 E9Ø — FP1 RECV DATA Ø2 L
8881 E91 — FN2 RECV DATA Ø1 L
8881 E91 — FP2 RECV DATA Ø Ø L

R12 1K +5V
R13 1K +5V
R14 1K +5V
R15 1K +5V
R16 1K +5V
R17 1K +5V
R18 1K +5V
R19 1K +5V
R2Ø 1K +5V
R21 1K +5V

R22 1ØK +5V — C1Ø2 27 PF
R23 1ØK +5V — C1Ø3 27PF
R24 1ØK +5V — C1Ø4 27 PF
R25 1ØK +5V — C1Ø7 27 PF

D4-2 RCV ENBL 11 (1) H
D4-3 CLR MATCH 11 L
D4-3 RESYNC PULSE 11 L
D4-2 RCV ENBL 11 (1) H
D4-5 MATCH 11 . Ø) H
D4-5 ACTIVE 11 H
D4-5 ACTIVE 11 L

D4-2 RCV ENBL 1Ø (1) H
D4-3 CLR MATCH 1Ø L
D4-3 RESYNC PULSE 1Ø L
D4-2 RCV ENBL 1Ø (1) H
D4-5 MATCH 1Ø (1) H
D4-5 ACTIVE 1Ø H
D4-5 ACTIVE 1Ø L

D4-2 RCV ENBL Ø9 (1) H
D4-3 CLR MATCH Ø9L
D4-3 RESYNC PULSE Ø9 L
D4-2 RCV ENBL Ø9 (1) H
D4-5 MATCH Ø9 (1) H
D4-5 ACTIVE Ø9 H
D4-5 ACTIVE Ø9 L

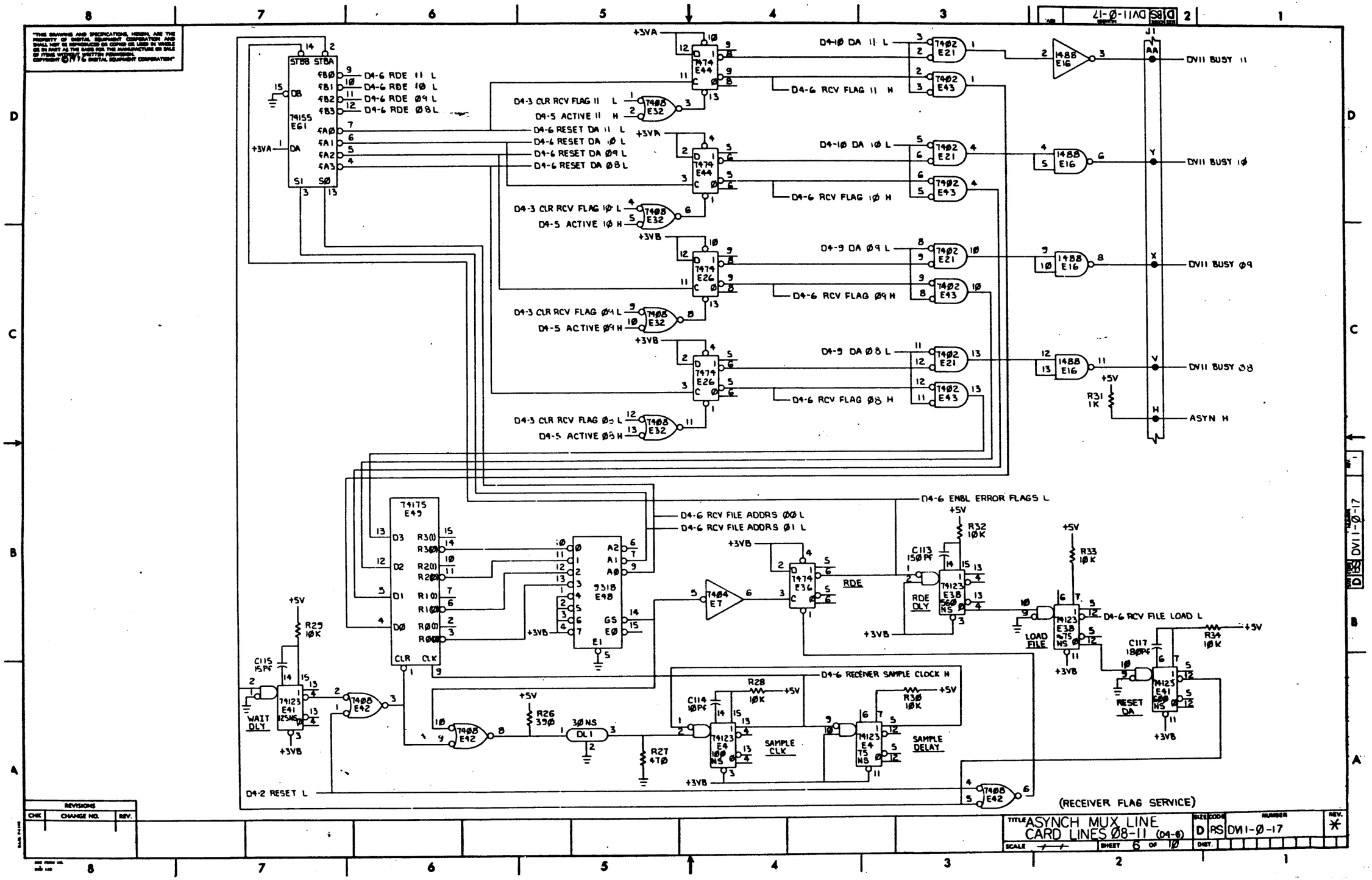
D4-2 RCV ENBL Ø8 (1) H
D4-3 CLR MATCH Ø8L
D4-3 RESYNC PULSE Ø8 L
D4-2 RCV ENBL Ø8 (1) H
D4-5 MATCH Ø8 (1) H
D4-5 ACTIVE Ø8 H
D4-5 ACTIVE Ø8 L

(RCV FILES, RCV DATA, MATCH LOGIC)

REVISIONS

CHK	CHANGE NO.	REV.

TITLE	ASYNCH MUX LINE CARD LINES Ø8-11 (D4-5)			
SIZE	CODE	NUMBER		REV.
D	BS	DV11-Ø-17		*
SCALE		SHEET 5 OF 1Ø	DIST.	



REVISIONS		
CHK	CHANGE NO.	REV.

TITLE ASYNCH MUX LINE CARD LINES 08-11 (D4-6)

SIZE D | CODE RS | NUMBER DV11-0-17 | REV. *

SCALE — | SHEET 6 OF 10 | DIST.

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D4-10 SERIAL OUT 11 H
D4-2 BREAK 11 (Ø) H
AH2
74Ø8 E9
1488 E11
EIA RCV DATA 11
J1 Ee KK
EIA XMIT DATA 11
1489 E5
C1Ø6 47ØPf
D4-2 MAINT 11 H
D4-2 HALF DUPLEX 11 H
D4-1Ø EOC 11 L
(EF2)
74Ø8 E19
8Ø94 E17
7432 E3
8Ø93 E18
D4-5 ACTIVE 11 L
7432 E22
BK1
D4-7 SERIAL IN 11 H

D4-10 SERIAL OUT 1Ø H
D4-2 BREAK 1Ø (Ø) H
AT2
74Ø8 E9
1488 E11
EIA RCV DATA 1Ø
J1 .11 CC HH
EIA XMIT DATA 1Ø
1489 E5
C1Ø5 47ØPf
D4-2 MAINT 1Ø H
D4-2 HALF DUPLEX 1Ø H
D4-1Ø EOC 1Ø L
(EK2)
74Ø8 E19
8Ø94 E17
7432 E3
8Ø93 E18
D4-5 ACTIVE 1Ø L
7432 E22
BK2
D4-7 SERIAL IN 1Ø H

D4-9 SERIAL OUT Ø9 H
D4-2 BREAK Ø9 (Ø) H
AB1
74Ø8 E9
1488 E11
EIA RCV DATA Ø9
J1 T N
EIA XMIT DATA Ø9
1489 E5
C128 47ØPf
D4-2 MAINT Ø9 H
D4-2 HALF DUPLEX Ø9 H
D4-9 EOC Ø9 L
(ER2)
74Ø8 E19
8Ø94 E17
7432 E3
8Ø93 E18
D4-5 ACTIVE Ø9 L
7432 E22
BD1
D4-7 SERIAL IN Ø9 H

D4-9 SERIAL OUT Ø8 H
D4-2 BREAK Ø8 (Ø) H
AJ12
74Ø8 E9
1488 E11
EIA RCV DATA Ø8
J1 R L
EIA XMIT DATA Ø8
1489 E5
C129 47ØPf
D4-2 MAINT Ø8 H
D4-2 HALF DUPLEX Ø8 H
D4-9 EOC Ø8 L
(FJ2)
74Ø8 E19
8Ø94 E17
7432 E3
8Ø93 E18
D4-5 ACTIVE Ø8 L
7432 E22
BF2
D4-7 SERIAL IN Ø8 H

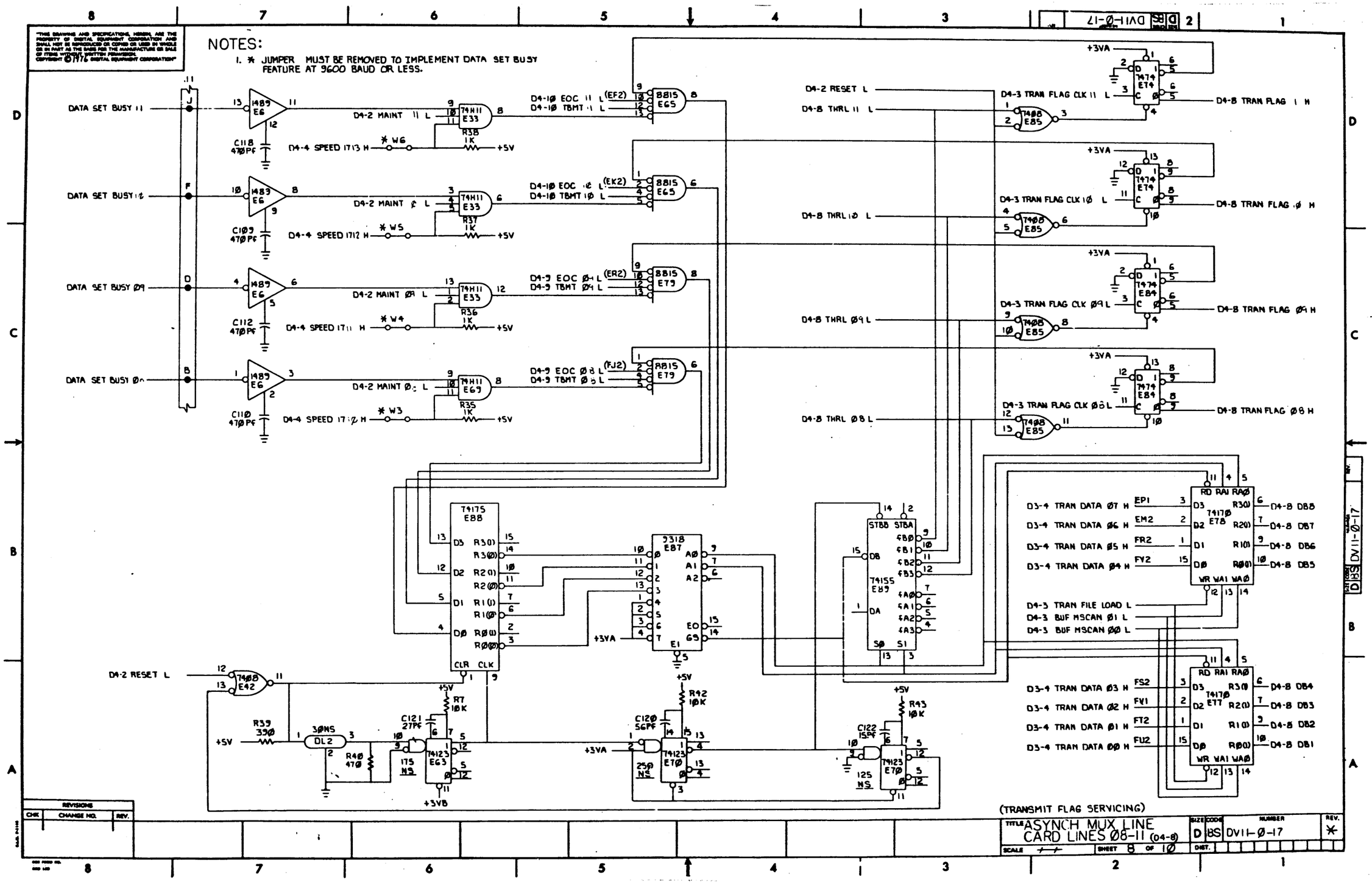
(EIA IN & OUT, HALF DUPLEX, BREAK, MAINT LOGIC)

REVISIONS
CHK | CHANGE NO. | REV.

TITLE ASYNCH MUX LINE CARD LINES Ø8-11 (D4-7)
SIZE D | CODE BS | NUMBER DVII-Ø-17 | REV. *
SCALE -/- | SHEET 7 OF 1Ø | DIST.

DEC STD 030 | DEC STD 110

DIST CODE BS | NUMBER DVII-Ø-17 | REV.


NOTES:
1. * JUMPER MUST BE REMOVED TO IMPLEMENT DATA SET BUSY FEATURE AT 9600 BAUD OR LESS.
DATA SET BUSY 11
DATA SET BUSY 10
DATA SET BUSY 09
DATA SET BUSY 08
D4-2 MAINT 11 L
D4-4 SPEED 1713 H
D4-2 MAINT 10 L
D4-4 SPEED 1712 H
D4-2 MAINT 09 L
D4-4 SPEED 1711 H
D4-2 MAINT 08 L
D4-4 SPEED 1710 H
D4-10 EOC 11 L
D4-10 TBMT 11 L
D4-10 EOC 10 L
D4-10 TBMT 10 L
D4-9 EOC 09 L
D4-9 TBMT 09 L
D4-9 EOC 08 L
D4-9 TBMT 08 L
D4-2 RESET L
D4-8 THRL 11 L
D4-8 THRL 10 L
D4-8 THRL 09 L
D4-8 THRL 08 L
D4-3 TRAN FLAG CLK 11 L
D4-3 TRAN FLAG CLK 10 L
D4-3 TRAN FLAG CLK 09 L
D4-3 TRAN FLAG CLK 08 L
D4-8 TRAN FLAG 11 H
D4-8 TRAN FLAG 10 H
D4-8 TRAN FLAG 09 H
D4-8 TRAN FLAG 08 H
D3-4 TRAN DATA 07 H
D3-4 TRAN DATA 06 H
D3-4 TRAN DATA 05 H
D3-4 TRAN DATA 04 H
D4-3 TRAN FILE LOAD L
D4-3 BUF MSCAN 01 L
D4-3 BUF MSCAN 00 L
D3-4 TRAN DATA 03 H
D3-4 TRAN DATA 02 H
D3-4 TRAN DATA 01 H
D3-4 TRAN DATA 00 H
D4-8 DB8
D4-8 DB7
D4-8 DB6
D4-8 DB5
D4-8 DB4
D4-8 DB3
D4-8 DB2
D4-8 DB1
(TRANSMIT FLAG SERVICING)
ASYNCH MUX LINE CARD LINES 08-11 (04-8)
D BS DV11-0-17
SHEET 8 OF 10

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D4-9 RD8
D4-9 RD7
D4-9 RD6
D4-9 RD5
D4-9 RD4
D4-9 RD3
D4-9 RD2
D4-9 RD1

1 7404 E8Ø 2 — D4-9 DA Ø8 L

D4-7 SERIAL IN Ø8 H (BF2) 2Ø — SERIAL IN
D4-6 RESET DA Ø8 L 18 — CLR R DONE
D4-6 RDE Ø8 L 4 — STB RD
16 — STB STATUS
17 — R CLK
D4-4 CLOCK Ø8 H (DE2) 4Ø — X CLK

UART Ø8 ET6

D4-8 THRL Ø8 L 23 — LD XD
33 — XD7
32 — XD6
31 — XD5
3Ø — XD4
29 — XD3
28 — XD2
27 — XD1
26 — XDØ

CLR NB1 NB2 2SB NP EP LDC

R DONE 19
OR ERR 15 — D4-9 OR Ø8
FR ERR 14 — D4-9 FE Ø8
P ERR 13 — D4-9 PE Ø8
RD7 5
RD6 6
RD5 7
RD4 8
RD3 9
RD2 1Ø
RD1 11
RDØ 12

AJ2 — D4-9 SERIAL OUT Ø8 H
SERIAL OUT 25
XRDY 22 — 11 7404 ET3 1Ø — D4-9 TBMT Ø8 L
EOC 24 — 9 7404 E8Ø 8 FJ2 — D4-9 EOC Ø8 L

21 38 37 36 35 39 34

3 7404 E8Ø 4 — D4-9 DA Ø9L

D4-7 SERIAL IN Ø9 H (BD1) 2Ø — SERIAL IN
D4-6 RESET DA Ø9 L 18 — CLR R DONE
D4-6 RDE Ø9 L 4 — STB RD
16 — STB STATUS
17 — R CLK
D4-4 CLOCK Ø9 H (CE2) 4Ø — X CLK

UART Ø9 E81

D4-8 THRL Ø9 L 23 — LD XD
33 — XD7
32 — XD6
31 — XD5
3Ø — XD4
29 — XD3
28 — XD2
27 — XD1
26 — XDØ

CLR NB1 NB2 2SB NP EP LDC

R DONE 19
OR ERR 15 — D4-9 OR Ø9
FR ERR 14 — D4-9 FE Ø9
P ERR 13 — D4-9 PE Ø9
RD7 5
RD6 6
RD5 7
RD4 8
RD3 9
RD2 1Ø
RD1 11
RDØ 12

AB1 — D4-9 SERIAL OUT Ø9 H
SERIAL OUT 25
XRDY 22 — 11 7404 E8Ø 1Ø — D4-9 TBMT Ø9 L
EOC 24 — 13 7404 E8Ø 12 ER2 — D4-9 EOC Ø9 L

21 38 37 36 35 39 34

D4-8 DB8
D4-8 DB7
D4-8 DB6
D4-8 DB5
D4-8 DB4
D4-8 DB3
D4-8 DB2
D4-8 DB1

D4-2 RESET H
D4-2 BUF LCR 11 H
D4-2 BUF LCR 12 H
D4-2 BUF LCR 13 H
D4-2 PEN L
D4-2 PEV Ø8 H
D4-2 UART STROBE Ø8 H
D4-2 PEV Ø9 H
D4-2 UART STROBE Ø9 H

(UARTS Ø8 & Ø9)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
ASYNCH MUX LINE CARD LINES Ø8-11 (D4-9)	D	BS	DV11-Ø-17	*
SCALE —	SHEET 9 OF 1Ø	DIST.		

DVII-Ø-17 D BS

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D4-7 SERIAL IN 1Ø H (BK2) 2Ø
D4-6 RESET DA 1Ø L 18
D4-6 RDE 1Ø L 4
16
17
D4-4 CLOCK 1Ø H (DS2) 4Ø
D4-8 THRL 1Ø L 23
33 32 31 3Ø 29 28 27 26
D4-8 DB8 D4-8 DB7 D4-8 DB6 D4-8 DB5 D4-8 DB4 D4-8 DB3 D4-8 DB2 D4-8 DB1

UART 1Ø E67

SERIAL IN
CLR R DONE
STB RD
STB STATUS
R CLK
X CLK
LD XD
XD7 XD6 XD5 XD4 XD3 XD2 XD1 XDØ
CLR NB1 NB2 2SB NP EP LDC
21 38 37 36 35 39 34

R DONE 19
OR ERR 15 D4-1Ø OR 1Ø
FR ERR 14 D4-1Ø FE 1Ø
P ERR 13 D4-1Ø PE 1Ø
RD7 5 D4-9 RDB
RD6 6 D4-9 RDT
RD5 7 D4-9 RD6
RD4 8 D4-9 RD5
RD3 9 D4-9 RD4
RD2 1Ø D4-9 RD3
RD1 11 D4-9 RD2
RDØ 12 D4-9 RD1
SERIAL OUT 25 AT2 D4-1Ø SERIAL OUT 1Ø H
XRDY 22 5 7404 E66 6 D4-1Ø TBMT 1Ø L
EOC 24 9 7404 E66 8 EK2 D4-1Ø EOC 1Ø L

1 7404 E66 2 D4-1Ø DA 1Ø L

D4-2 RESET H
D4-2 BUF LCR 11 H
D4-2 BUF LCR 12 H
D4-2 BUF LCR 13 H
D4-2 PEN L
D4-2 PEV 1Ø H
D4-2 UART STROBE 1Ø H
D4-2 PEV 11 H
D4-2 UART STROBE 11 H

D4-7 SERIAL IN 11 H (BK1) 2Ø
D4-6 RESET DA 11 L 18
D4-6 RDE 11 L 4
16
17
D4-4 CLOCK 11 H (CP2) 4Ø
D4-8 THRL 11 L 23
33 32 31 3Ø 29 28 27 26

UART 11 E62

SERIAL IN
CLR R DONE
STB RD
STB STATUS
R CLK
X CLK
LD XD
XD7 XD6 XD5 XD4 XD3 XD2 XD1 XDØ
CLR NB1 NB2 2SB NP EP LDC
21 38 37 36 35 39 34

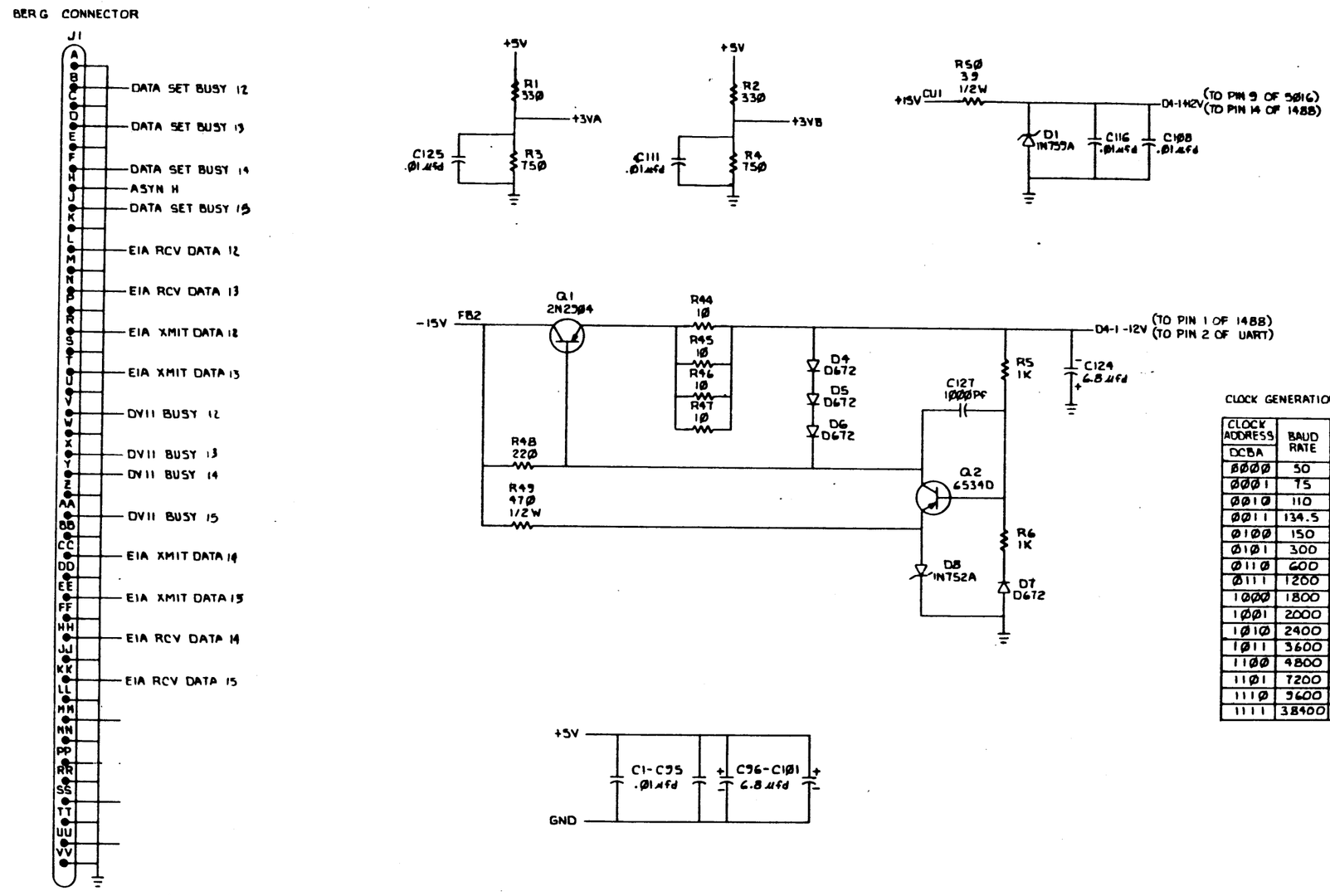
R DONE 19
OR ERR 15 D4-1Ø OR 11
FR ERR 14 D4-1Ø FE 11
P ERR 13 D4-1Ø PE 11
RD7 5
RD6 6
RD5 7
RD4 8
RD3 9
RD2 1Ø
RD1 11
RDØ 12
SERIAL OUT 25 AH2 D4-1Ø SERIAL OUT 11 H
XRDY 22 11 7404 E66 1Ø D4-1Ø TBMT 11 L
EOC 24 13 7404 E66 12 EF2 D4-1Ø EOC 11 L

3 7404 E66 4 D4-1Ø DA 11 L

(UARTS 1Ø & 11)

REVISIONS
CHK | CHANGE NO. | REV.

TITLE ASYNCH MUX LINE CARD LINES Ø8-11 (D4-1Ø)
SIZE D CODE 8S NUMBER DV11-Ø-17 REV. *
SCALE — SHEET 1Ø OF 1Ø DIST.



CLOCK GENERATION CHART

CLOCK ADDRESS DCBA	BAUD RATE	PERIOD (USEC)
0000	50	1250.00
0001	75	833.33
0010	110	568.18
0011	134.5	464.68
0100	150	416.67
0101	300	208.33
0110	600	104.17
0111	1200	52.08
1000	1800	34.72
1001	2000	31.25
1010	2400	26.04
1011	3600	17.36
1100	4800	13.02
1101	7200	8.68
1110	9600	6.51
1111	38400	1.63

(CHART, REGULATORS)

DRN	1-13-76	FIRST USED ON DV11
CHK	4/15/76	TITLE ASYNCH MUX LINE CARD LINES 12-15 (D4-1)
ENG.	4-5-76	
PROJ. ENG.	4-15-76	
PROD. R. Wall	4-16-76	
NEXT HIGHER ASSY. B-DD-DV11-0		SIZE D CODE BS NUMBER DV11-0-18 REV. *
SCALE		
SHEET	OF 10	DIST.

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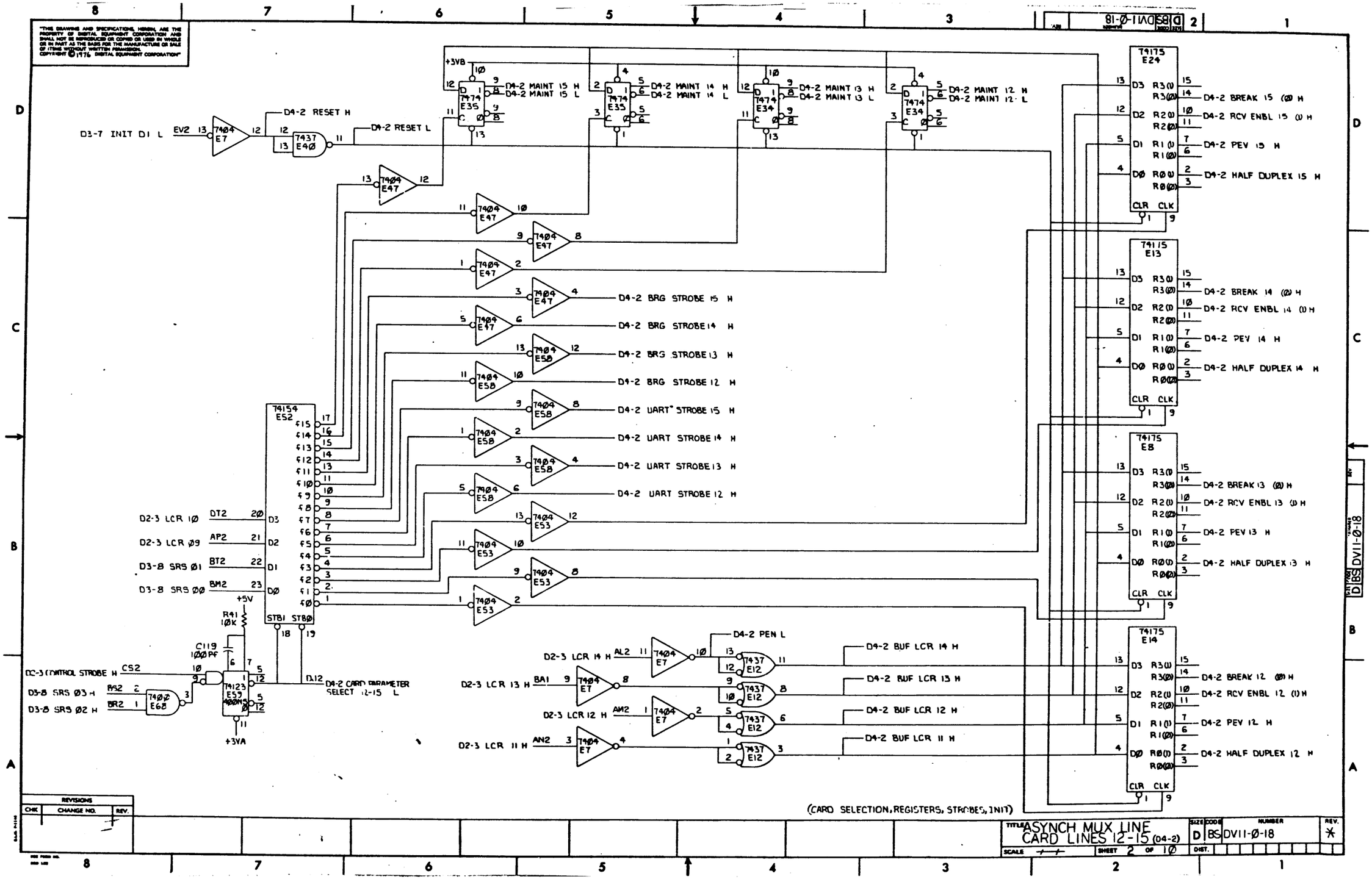

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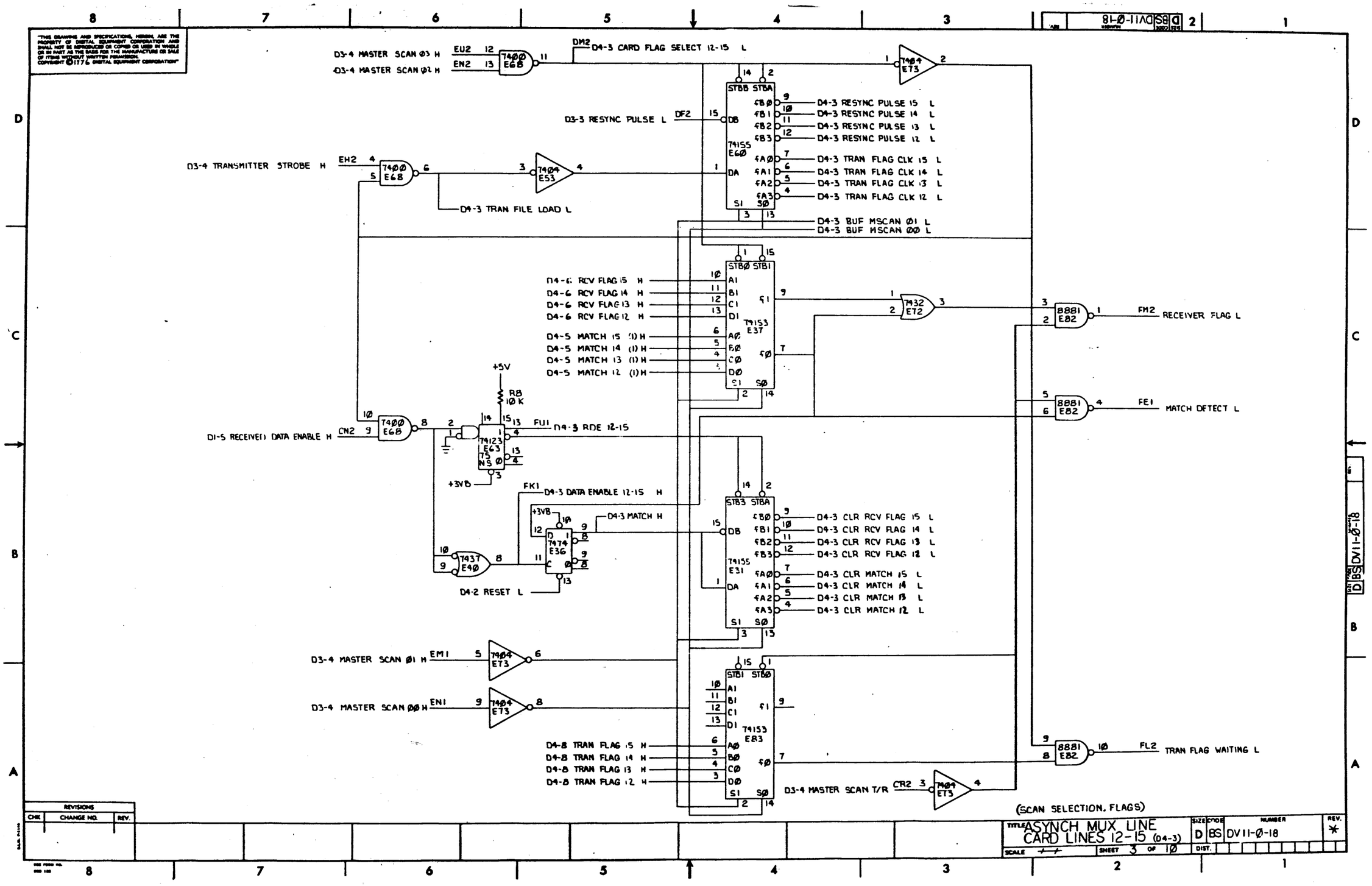
REVISIONS		
CHK	CHANGE NO.	REV.

TITLE ASYNCH MUX LINE CARD LINES 12-15 (04-2)

SIZE D | CODE BS | NUMBER DV11-0-18 | REV. *

SCALE | SHEET 2 OF 10 | DIST.

D BS DV11-0-18



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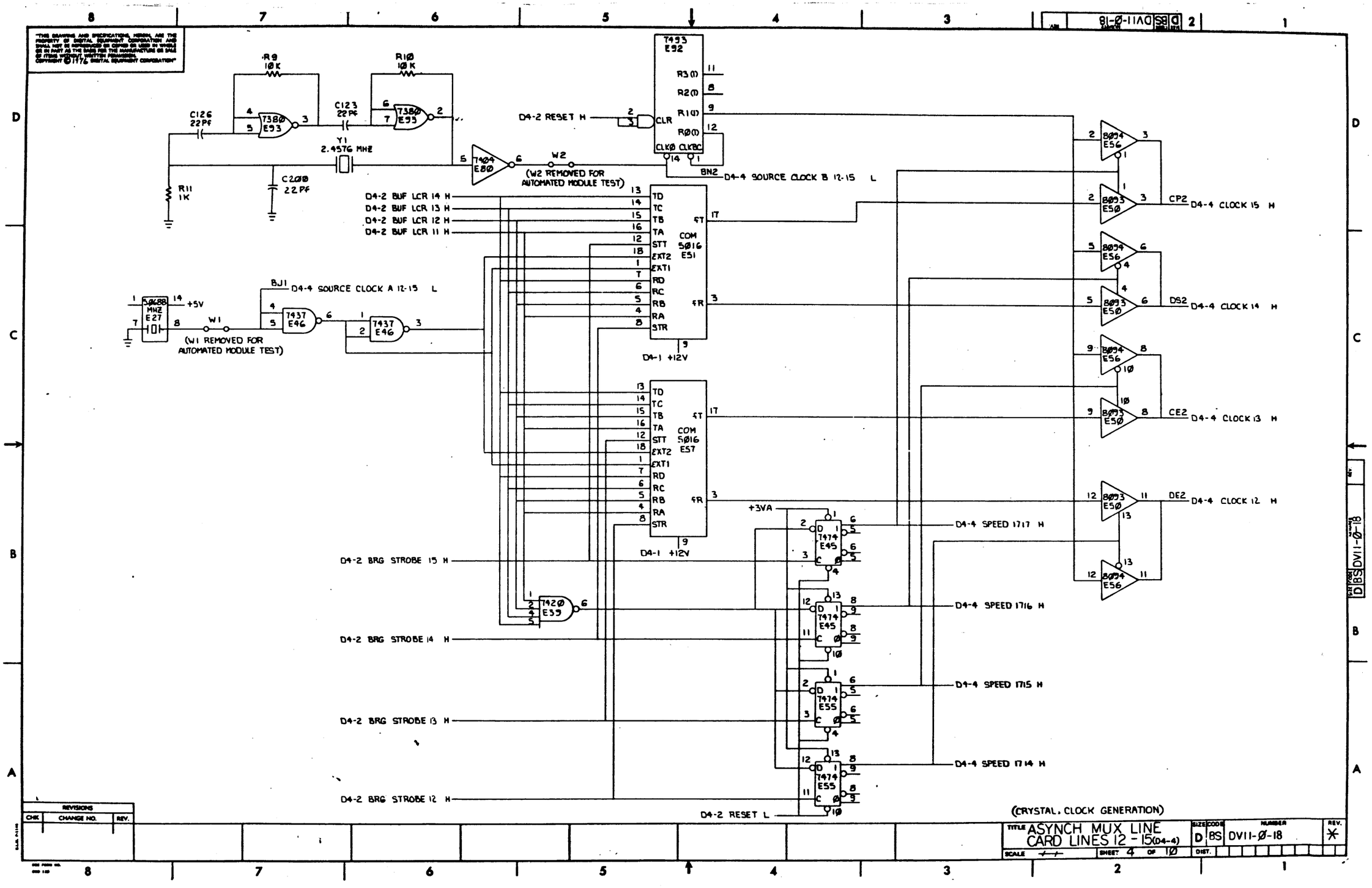
REVISIONS		
CHK	CHANGE NO.	REV.

TITLE ASYNCH MUX LINE CARD LINES 12-15 (D4-3)

SIZE D | CODE BS | NUMBER DV11-Ø-18 | REV. *

SCALE — | SHEET 3 OF 10 | DIST.

D BS DV11-Ø-18



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R9 10K
R10 10K
C126 22PF
C123 22PF
7380 E93
Y1 2.4576 MHZ
C200 22PF
R11 1K
7404 E80
W2
(W2 REMOVED FOR AUTOMATED MODULE TEST)
7493 E92
R3(1)
R2(1)
R1(1)
R0(1)
CLR
CLK0 CLKBC
BN2
D4-2 RESET H
D4-4 SOURCE CLOCK B 12-15 L
D4-2 BUF LCR 14 H
D4-2 BUF LCR 13 H
D4-2 BUF LCR 12 H
D4-2 BUF LCR 11 H
TD
TC
TB
TA
STT
EXT2
EXT1
RD
RC
RB
RA
STR
COM 5016 E51
COM 5016 E57
D4-1 +12V
BJ1
D4-4 SOURCE CLOCK A 12-15 L
50688 MHZ E27
+5V
W1
(W1 REMOVED FOR AUTOMATED MODULE TEST)
7437 E46
8094 E56
8093 E50
CP2
D4-4 CLOCK 15 H
DS2
D4-4 CLOCK 14 H
CE2
D4-4 CLOCK 13 H
DE2
D4-4 CLOCK 12 H
+3VA
7474 E45
7474 E55
D4-4 SPEED 1717 H
D4-4 SPEED 1716 H
D4-4 SPEED 1715 H
D4-4 SPEED 1714 H
D4-2 BRG STROBE 15 H
D4-2 BRG STROBE 14 H
D4-2 BRG STROBE 13 H
D4-2 BRG STROBE 12 H
7420 E39
D4-2 RESET L
(CRYSTAL, CLOCK GENERATION)
REVISIONS
CHK
CHANGE NO.
REV.
TITLE ASYNCH MUX LINE CARD LINES 12 - 15(D4-4)
SIZE D
CODE BS
NUMBER DV11-0-18
REV. *
SCALE
SHEET 4 OF 10
DIST.

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D4-6 ENBL ERROR FLAGS L

D4-10 OR 15
D4-10 OR 14
D4-9 OR 13
D4-9 OR 12
D4-10 PE 15
D4-10 PE 14
D4-9 PE 13
D4-9 PE 12

STBØ STB1 — 74153 E71 — T4Ø4 E53 — T4H11 E69

D4-10 FE 15
D4-10 FE 14
D4-9 FE 13
D4-9 FE 12

STBØ STB1 — 74153 E75

+3VB — T9157 E64 (SØ | F; L | A; H | B)

D4-9 RD8
D4-9 RD7
D4-9 RD6
D4-9 RD5

D4-3 BUF MSCAN ØØ L
D4-3 BUF MSCAN Ø1 L
D4-3 CARD FLAG SELECT 12-15 L

D4-9 RD4
D4-9 RD3
D4-9 RD2
D4-9 RD1

D4-6 RCV FILE LOAD L
D4-6 RCV FILE ADDRS Ø1 L
D4-6 RCV FILE ADDRS ØØ L
D4-3 DATA ENABLE 12-15 H

RD RAI RAØ — D3 D2 D1 DØ — R3(1) R2(1) R1(1) RØ(1) — WR WAI WAØ — 74170 E54 / E95 / E94

8881 E86 — FL1 MASTER OR L; FM1 MASTER PE L; FH1 RECV DATA Ø7 L; FJ1 RECV DATA Ø6 L
8881 E9Ø — FR1 RECV DATA Ø5 L; FS1 RECV DATA Ø4 L; FN1 RECV DATA Ø3 L; FP1 RECV DATA Ø2 L
8881 E91 — FN2 RECV DATA Ø1 L; FP2 RECV DATA ØØ L

R12 R13 R14 R15 R16 R17 R18 R19 R2Ø R21 — 1K — +5V

D4-2 RCV ENBL 15 (1) H
C1Ø2 27 PF — R22 1ØK +5V — +3VB
74123 E2 — 74174 E29 — D4-5 MATCH 15 (1) H; D4-5 ACTIVE 15 H; D4-5 ACTIVE 15 L
D4-3 CLR MATCH 15 L — 74Ø8 E3Ø
D4-3 RESYNC PULSE 15 L
D4-2 RCV ENBL 15 (1) H

D4-2 RCV ENBL 14 (1) H
C1Ø3 27PF — R23 1ØK +5V — +3VB
74123 E2 — 74174 E23 — D4-5 MATCH 14 (1) H; D4-5 ACTIVE 14 H; D4-5 ACTIVE 14 L
D4-3 CLR MATCH 14 L — 74Ø8 E3Ø
D4-3 RESYNC PULSE 14 L
D4-2 RCV ENBL 14 (1) H

D4-2 RCV ENBL 13 (1) H
C1Ø4 27 PF — R24 1ØK +5V — +3VB
74123 E1Ø — 74174 E25 — D4-5 MATCH 13 (1) H; D4-5 ACTIVE 13 H; D4-5 ACTIVE 13 L
D4-3 CLR MATCH 13 L — 74Ø8 E2Ø
D4-3 RESYNC PULSE 13 L
D4-2 RCV ENBL 13 (1) H

D4-2 RCV ENBL 12 (1) H
C1Ø7 27 PF — R25 1ØK +5V — +3VB
74123 E1Ø — 74174 E15 — D4-5 MATCH 12 (1) H; D4-5 ACTIVE 12 H; D4-5 ACTIVE 12 L
D4-3 CLR MATCH 12 L — 74Ø8 E2Ø
D4-3 RESYNC PULSE 12 L
D4-2 RCV ENBL 12 (1) H

(RCV FILES, RCV DATA, MATCH LOGIC)

REVISIONS

CHK	CHANGE NO.	REV.

TITLE	ASYNCH MUX LINE CARD LINES 12-15 (D4-5)
SIZE	D
CODE	BS
NUMBER	DV11-Ø-18
REV.	*
SCALE	
SHEET	5 OF 1Ø
DIST.	

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+3VA
+3VB
+5V
D4-6 RDE 15 L
D4-6 RDE 14 L
D4-6 RDE 13 L
D4-6 RDE 12 L
D4-6 RESET DA 15 L
D4-6 RESET DA 14 L
D4-6 RESET DA 13 L
D4-6 RESET DA 12 L
D4-3 CLR RCV FLAG 15 L
D4-5 ACTIVE 15 H
D4-3 CLR RCV FLAG 14 L
D4-5 ACTIVE 14 H
D4-3 CLR RCV FLAG 13 L
D4-5 ACTIVE 13 H
D4-3 CLR RCV FLAG 12 L
D4-5 ACTIVE 12 H
D4-10 DA 15 L
D4-6 RCV FLAG 15 H
D4-10 DA 14 L
D4-6 RCV FLAG 14 H
D4-9 DA 13 L
D4-6 RCV FLAG 13 H
D4-9 DA 12 L
D4-6 RCV FLAG 12 H
DV11 BUSY 15
DV11 BUSY 14
DV11 BUSY 13
DV11 BUSY 12
ASYN H
D4-6 ENBL ERROR FLAGS L
D4-6 RCV FILE ADDRS ØØ L
D4-6 RCV FILE ADDRS Ø1 L
D4-6 RECEIVER SAMPLE CLOCK H
D4-6 RCV FILE LOAD L
D4-2 RESET L
RDE
RDE DLY
LOAD FILE
RESET DA
WAIT DLY
SAMPLE CLK
SAMPLE DELAY
(RECEIVER FLAG SERVICE)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE ASYNCH MUX LINE CARD LINES 12-15 (D4-6)
SIZE D CODE BS NUMBER DV11-Ø-18 REV. *
SCALE — SHEET 6 OF 1Ø DIST.

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D4-10 SERIAL OUT 15 H
D4-2 BREAK 15 (Ø) H
AH2 — T4Ø8 E9 — 1488 E11 — J1 EE — EIA XMIT DATA 15.
EIA RCV DATA 15 — J1 KK — 1489 E5 — C1Ø6 47ØPf
D4-2 MAINT 15 H — 8Ø94 E17 — 8Ø93 E18
D4-2 HALF DUPLEX 15 H
D4-1Ø EOC 15 L (EF2) — T4Ø8 E13 — 7432 E3
D4-5 ACTIVE 15 L — 7432 E22 — BK1 — D4-7 SERIAL IN 15 H

D4-10 SERIAL OUT 14 H
D4-2 BREAK 14 (Ø) H
AT2 — T4Ø8 E9 — 1488 E11 — J1 CC — EIA XMIT DATA 14
EIA RCV DATA 14 — J1 HH — 1489 E5 — C1Ø5 47ØPf
D4-2 MAINT 14 H — 8Ø94 E17 — 8Ø93 E18
D4-2 HALF DUPLEX 14 H
D4-1Ø EOC 14 L (EK2) — T4Ø8 E19 — 7432 E3
D4-5 ACTIVE 14 L — 7432 E22 — BK2 — D4-7 SERIAL IN 14 H

D4-9 SERIAL OUT 13 H
D4-2 BREAK 13 (Ø) H
AB1 — T4Ø8 E9 — 1488 E11 — J1 T — EIA XMIT DATA 13
EIA RCV DATA 13 — J1 N — 1489 E5 — C128 47ØPf
D4-2 MAINT 13 H — 8Ø94 E17 — 8Ø93 E18
D4-2 HALF DUPLEX 13 H
D4-9 EOC 13 L (ER2) 1Ø — T4Ø8 E19 — 7432 E3
D4-5 ACTIVE 13 L — 7432 E22 — BD1 — D4-7 SERIAL IN 13 H

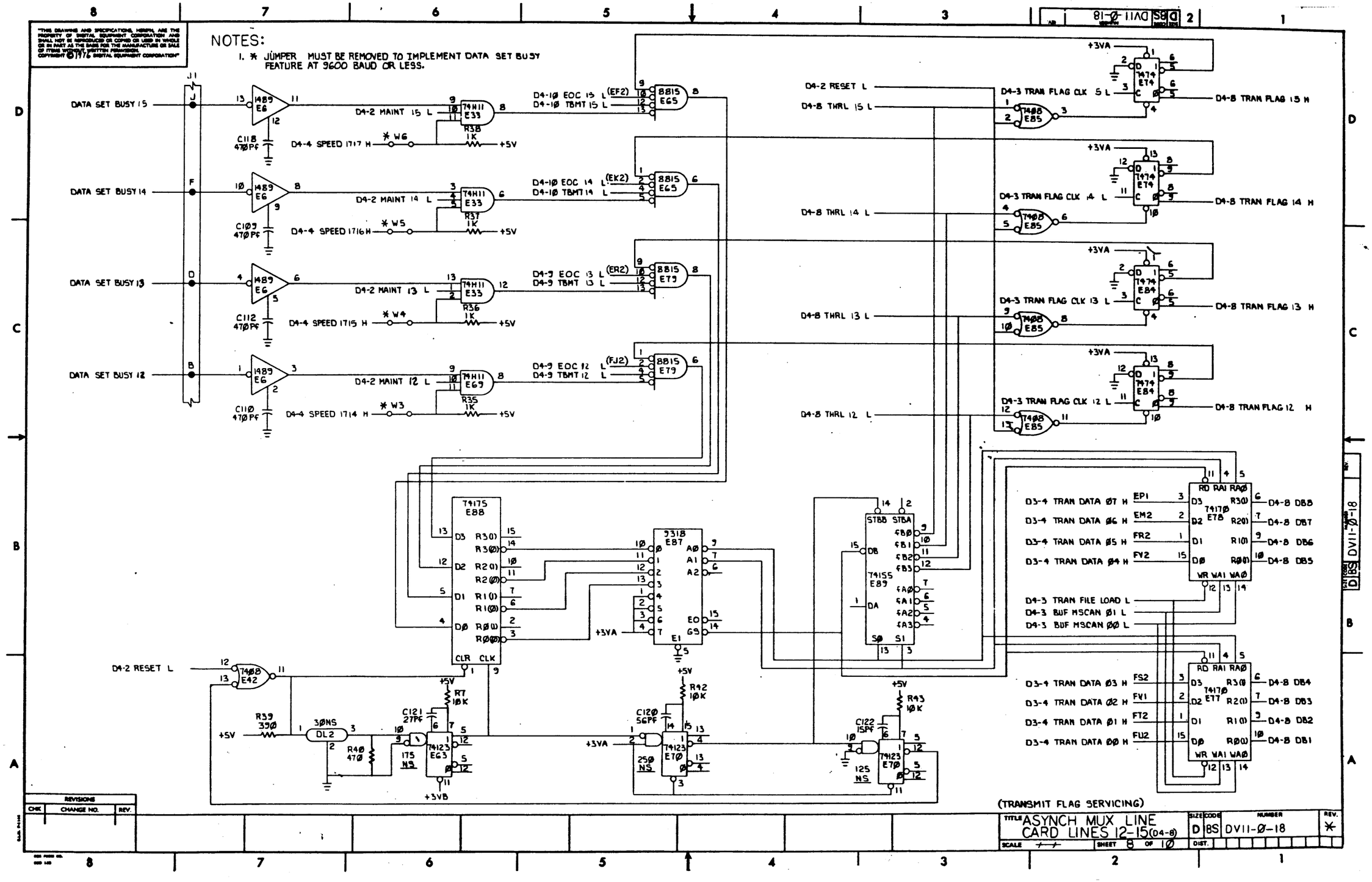
D4-9 SERIAL OUT 12 H
D4-2 BREAK 12 (Ø) H
AJ2 — T4Ø8 E9 — 1488 E11 — J1 R — EIA XMIT DATA 12
EIA RCV DATA 12 — J1 L — 1489 E5 — C129 47Ø PF
D4-2 MAINT 12 H — 8Ø94 E17 — 8Ø93 E18
D4-2 HALF DUPLEX 12 H
D4-9 EOC 12 L (NJ2) 13 — T4Ø8 E19 — 7432 E3
D4-5 ACTIVE 12 L — 7432 E22 — BF2 — D4-7 SERIAL IN 12 H

(EIA IN & OUT. HALF DUPLEX. BREAK. MAINT LOGIC)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
ASYNCH MUX LINE CARD LINES 12-15 (D4-7)	D	BS	DV11-Ø-18	*

SCALE — SHEET 7 OF 1Ø


NOTES:
1. * JUMPER MUST BE REMOVED TO IMPLEMENT DATA SET BUSY FEATURE AT 9600 BAUD OR LESS.
DATA SET BUSY 15
DATA SET BUSY 14
DATA SET BUSY 13
DATA SET BUSY 12
D4-2 MAINT 15 L
D4-4 SPEED 1717 H
D4-2 MAINT 14 L
D4-4 SPEED 1716 H
D4-2 MAINT 13 L
D4-4 SPEED 1715 H
D4-2 MAINT 12 L
D4-4 SPEED 1714 H
D4-10 EOC 15 L
D4-10 TBMT 15 L
D4-10 EOC 14 L
D4-10 TBMT 14 L
D4-9 EOC 13 L
D4-9 TBMT 13 L
D4-9 EOC 12 L
D4-9 TBMT 12 L
D4-2 RESET L
D4-8 THRL 15 L
D4-8 THRL 14 L
D4-8 THRL 13 L
D4-8 THRL 12 L
D4-3 TRAN FLAG CLK 15 L
D4-3 TRAN FLAG CLK 14 L
D4-3 TRAN FLAG CLK 13 L
D4-3 TRAN FLAG CLK 12 L
D4-8 TRAN FLAG 15 H
D4-8 TRAN FLAG 14 H
D4-8 TRAN FLAG 13 H
D4-8 TRAN FLAG 12 H
D3-4 TRAN DATA Ø7 H
D3-4 TRAN DATA Ø6 H
D3-4 TRAN DATA Ø5 H
D3-4 TRAN DATA Ø4 H
D4-3 TRAN FILE LOAD L
D4-3 BUF MSCAN Ø1 L
D4-3 BUF MSCAN ØØ L
D3-4 TRAN DATA Ø3 H
D3-4 TRAN DATA Ø2 H
D3-4 TRAN DATA Ø1 H
D3-4 TRAN DATA ØØ H
D4-8 DB8
D4-8 DB7
D4-8 DB6
D4-8 DB5
D4-8 DB4
D4-8 DB3
D4-8 DB2
D4-8 DB1
(TRANSMIT FLAG SERVICING)
ASYNCH MUX LINE CARD LINES 12-15 (D4-8)
D BS DV11-Ø-18
SHEET 8 OF 10

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D4-9 RD8
D4-9 RD7
D4-9 RD6
D4-9 RD5
D4-9 RD4
D4-9 RD3
D4-9 RD2
D4-9 RD1

D4-7 SERIAL IN 12 H — BF2 20 — SERIAL IN
D4-6 RESET DA 12 L — 18 — CLR R DONE
D4-6 RDE 12 L — 4 — STB RD
16 — STB STATUS
17 — R CLK
D4-4 CLOCK 12 H — (DE2) 40 — X CLK

UART 12 ET6

D4-8 THRL 12 L — 23 — LD XD
33 — XD7
32 — XD6
31 — XD5
30 — XD4
29 — XD3
28 — XD2
27 — XD1
26 — XDØ

CLR NB1 NB2 2SB NP EP LDC
21 38 37 36 35 39 34

R DONE 19 — 1 T4Ø4 EBØ 2 — D4-9 DA 12 L
OR ERR 15 — D4-9 OR 12
FR ERR 14 — D4-9 FE 12
P ERR 13 — D4-9 PE 12
RD7 5
RD6 6
RD5 7
RD4 8
RD3 9
RD2 10
RD1 11
RDØ 12

SERIAL OUT 25 — AJ2 — D4-9 SERIAL OUT 12 H
XRDY 22 — 11 T4Ø4 ET3 10 — D4-9 TBMT 12 L
EOC 24 — 9 T4Ø4 EBØ 8 FJ2 — D4-9 EOC 12 L

D4-7 SERIAL IN 13 H — (BD1) 20 — SERIAL IN
D4-6 RESET DA 13 L — 18 — CLR R DONE
D4-6 RDE 13 L — 4 — STB RD
16 — STB STATUS
17 — R CLK
D4-4 CLOCK 13 H — (CE2) 40 — X CLK

UART 13 EB1

D4-8 THRL 13 L — 23 — LD XD
33 — XD7
32 — XD6
31 — XD5
30 — XD4
29 — XD3
28 — XD2
27 — XD1
26 — XDØ

CLR NB1 NB2 2SB NP EP LDC
21 38 37 36 35 39 34

R DONE 19 — 3 T4Ø4 EBØ 4 — D4-9 DA 13 L
OR ERR 15 — D4-9 OR 13
FR ERR 14 — D4-9 FE 13
P ERR 13 — D4-9 PE 13
RD7 5
RD6 6
RD5 7
RD4 8
RD3 9
RD2 10
RD1 11
RDØ 12

SERIAL OUT 25 — ABI — D4-9 SERIAL OUT 13 H
XRDY 22 — 11 T4Ø4 EBØ 10 — D4-9 TBMT 13 L
EOC 24 — 13 T4Ø4 EBØ 12 ER2 — D4-9 EOC 13 L

D4-8 DB8
D4-8 DB7
D4-8 DB6
D4-8 DB5
D4-8 DB4
D4-8 DB3
D4-8 DB2
D4-8 DB1

D4-2 RESET H
D4-2 BUF LCR 11 H
D4-2 BUF LCR 12 H
D4-2 BUF LCR 13 H
D4-2 PEN L
D4-2 PEV 12 H
D4-2 UART STROBE 12 H
D4-2 PEV 13 H
D4-2 UART STROBE 13 H

(UARTS 12 & 13)

REVISIONS
CHK | CHANGE NO. | REV.

TITLE ASYNCH MUX LINE CARD LINES 12-15 (04-9)
SIZE D | CODE BS | NUMBER DV11-Ø-18 | REV. *
SCALE | SHEET 9 OF 10 | DIST.

DBS DV11-Ø-18

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D4-9 RD8
D4-9 RD7
D4-9 RD6
D4-9 RD5
D4-9 RD4
D4-9 RD3
D4-9 RD2
D4-9 RD1

D4-7 SERIAL IN 14 H (BK2) 20 — SERIAL IN
D4-6 RESET DA 14 L 18 — CLR R DONE
D4-6 RDE 14 L 4 — STB RD
16 — STB STATUS
17 — R CLK
D4-4 CLOCK 14 H (DS2) 40 — X CLK

UART 14
E67

D4-8 THRL 14 L 23 — LD XD
33 — XD7
32 — XD6
31 — XD5
30 — XD4
29 — XD3
28 — XD2
27 — XD1
26 — XD0

CLR NB1 NB2 2SB NP EP LDC

21 38 37 36 35 39 34

R DONE 19 — 7404 E66 1 → 2 — D4-10 DA 14 L
OR ERR 15 — D4-10 OR 14
FR ERR 14 — D4-10 FE 14
P ERR 13 — D4-10 PE 14
RD7 5
RD6 6
RD5 7
RD4 8
RD3 9
RD2 10
RD1 11
RD0 12
SERIAL OUT 25 — AT2 — D4-10 SERIAL OUT 14 H
XRDY 22 — 7404 E66 5 → 6 — D4-10 TBMT 14 L
EOC 24 — 7404 E66 9 → 8 — EK2 — D4-10 EOC 14 L

D4-7 SERIAL IN 15 H (BK1) 20 — SERIAL IN
D4-6 RESET DA 15 L 18 — CLR R DONE
D4-6 RDE 15 L 4 — STB RD
16 — STB STATUS
17 — R CLK
D4-4 CLOCK 15 H (CP2) 40 — X CLK

UART 15
E62

D4-8 THRL 15 L 23 — LD XD
33 — XD7
32 — XD6
31 — XD5
30 — XD4
29 — XD3
28 — XD2
27 — XD1
26 — XD0

CLR NB1 NB2 2SB NP EP LDC

21 38 37 36 35 39 34

R DONE 19 — 7404 E66 3 → 4 — D4-10 DA 15 L
OR ERR 15 — D4-10 OR 15
FR ERR 14 — D4-10 FE 15
P ERR 13 — D4-10 PE 15
RD7 5
RD6 6
RD5 7
RD4 8
RD3 9
RD2 10
RD1 11
RD0 12
SERIAL OUT 25 — AH2 — D4-10 SERIAL OUT 15 H
XRDY 22 — 7404 E66 11 → 10 — D4-10 TBMT 15 L
EOC 24 — 7404 E66 13 → 12 — EF2 — D4-10 EOC 15 L

D4-8 DB8
D4-8 DB7
D4-8 DB6
D4-8 DB5
D4-8 DB4
D4-8 DB3
D4-8 DB2
D4-8 DB1

D4-2 RESET H
D4-2 BUF LCR 11 H
D4-2 BUF LCR 12 H
D4-2 BUF LCR 13 H
D4-2 PEN L
D4-2 PEV 14 H
D4-2 UART STROBE 14 H
D4-2 PEV 15 H
D4-2 UART STROBE 15 H

(UARTS 14 & 15)

REVISIONS

CHK	CHANGE NO.	REV.

TITLE	ASYNCH MUX LINE CARD LINES 12-15 (D4-10)
SIZE	D
CODE	BS
NUMBER	DV11-Ø-18
REV.	*
SCALE	
SHEET	10 OF 10
DIST.	

DV11-Ø-18

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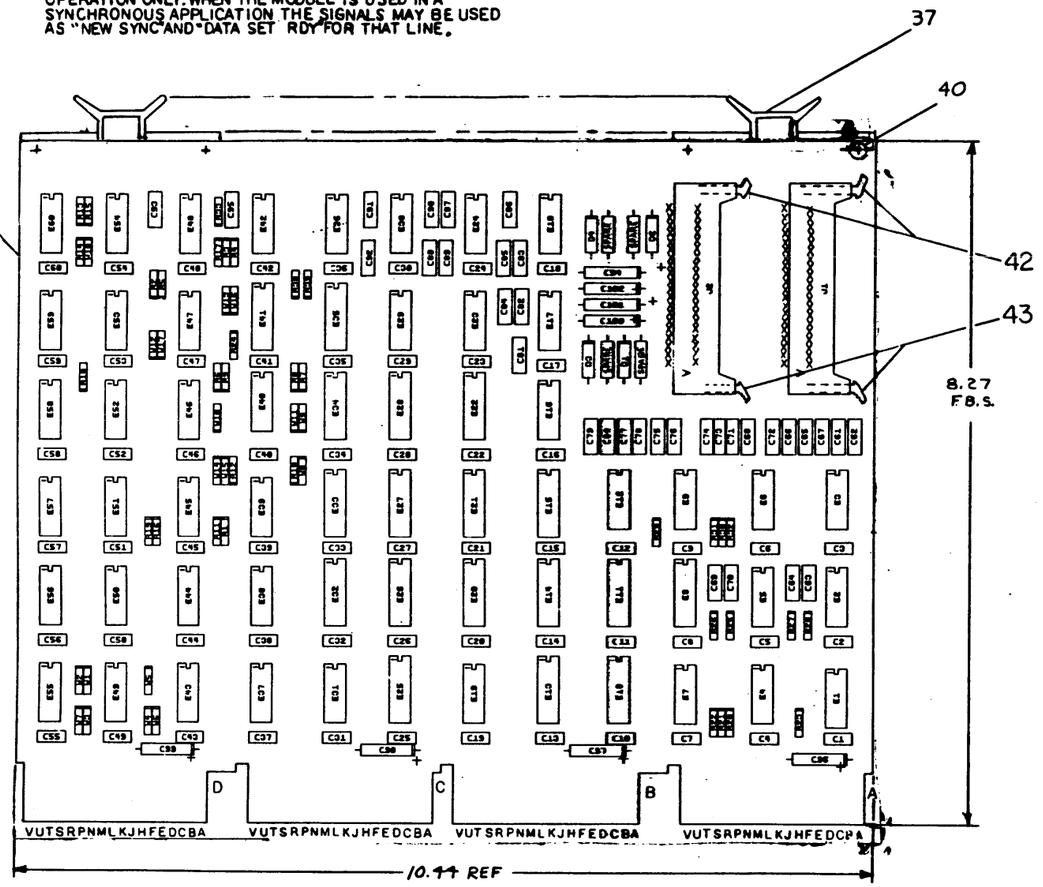
NOTES:

1. ALL UNUSED PINS ON J1, J2 GO TO GND
2. THE SIGNALS 'SEC TX' AND 'SEC RX' REFER TO ASYNCHRONOUS OPERATION ONLY. WHEN THE MODULE IS USED IN A SYNCHRONOUS APPLICATION THE SIGNALS MAY BE USED AS "NEW SYNC" AND "DATA SET RDY" FOR THAT LINE.



JUMPER TABLE	
JUMPER	BIT
W1	D00
W2	D02
W3	D03
W4	D06
W5	D07
W6	D05
W7	D04
W8	A12
W9	A09
W10	A08
W11	A10
W12	A04
W13	A05
W14	A11
W15	A03
W16	A06
W17	A07

JUMPER REMOVED INTERRUPT VECTOR = 0

JUMPER REMOVED DEVICE SELECT = 1

AA2, BA2, CA2, DA2
AC2, AT1, BC2, BT1
CC2, CT1, DC2, DT1
+5V
C1 – C60 .01 μF
C96 – C99 6.8 μF

DEC 8640	1	8
DEC IC 7442	8	16
DEC IC 74175	8	16
DEC IC 74151	8	16
IC TYPE	GND	+ 5V

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

REF		X-Y COORDINATE HOLE LOCATION	H-CO-M7807-0-4	1
REF		ASSY/DRILLING HOLE LAYOUT	D-AH-M7807-0-5	2
REF		MODULE ECO HISTORY	D-MH-M7807-0-6	3
1		ETCHED CIRCUIT BOARD	9010983	4
8	C84, C86—C102	CAP 6.8 UF 35V 10%	1905388	5
80	C1-C80	CAP .01 UF 100V 20%	1901618-04	6
33	C81—C93	CAP 470 MMF 100V 5%	1900824	7
1	C85	CAP 330 PF 100V 5%	1900823	8
4	D1, D2 D3, D4	DIODE 1N4733A	1109943	9
16	R1-R13, R15, R17, R18,	RES 1K 1/4W 5%	1300365	10
1	R14	RES 100 1/4W 5%	1300229	11
1	R33	RES 47 1/4W 5%	1300202	12
1	R19	RES 180 1/4W 5%	1301322	13
5	R20-R23, R39	RES 750 1/4W 5%	1301481	14
8	R25-R32	RES 33K 1/4W 10%	1300510	15
1	R18	RES 390 1/4W 5%	1300369	16
~~0~~	~~R24, R26—R38, R37~~	~~RES 33 OHM 1/4W 5%~~	~~1300095~~	~~17~~
1	E52	I.C. DEC 7400	1910156	18
1	E4,	I.C. DEC 7417	1909829	19
8	E16, E18, E23, E29, E36, E42	I.C. DEC 1488L	1910322	20
8	E3, 5, 6, 9, 12, 17, 24, 30	I.C. DEC 1489L	1910323	21
8	E8, 11, 14, 15, 20, 21, 22, 26	I.C. DEC 74151	1909836	22
8	E10, 13, 25, 28, 32, 33, 34, 35	I.C. DEC 74175	1910651	23
1	E19	I.C. DEC 7418	1905576	24
1	E27	I.C. DEC 7442	1910646	25
6	E7, E7, E40, E51, E55, E60	I.C. DEC 8881	1909705	26
2	E58, E59	I.C. DEC 7400	1905575	27
7	E31, E37, E43, E45, E46 E53, E54	I C DEC 8640	1911469	28
1	E50	I.C. DEC 7474	1905547	29
1	E2	I.C. DEC 74H04	1909931	30
1	E44	I.C. DEC 74H00	1908656	31
3	E39, E40, E47	I.C. DEC 8242	1908712	32
1	E41	I.C. DEC 74123	1910438	33
1	E48	I.C. DEC 74H74	1909867	34
1	E38	I.C. DEC 8815	1908713	35
2	E50 E57	I.C. DEC 7402	1909004	36
4		HANDLE FLIP CHIP	9006337-6	37
2	J1, J2	" 40 PIN HEADER	1209841	38
18	W1-W18	JUMPER (INSULATED)	9009189	39
8		EYELET HANDLE	9006732	40
1	R36	RES 33Ω 1/4W 5%	1300295	41
2		LEFT LATCH	1209941-03	42
2		RIGHT LATCH	1209941-04	43
1	R24	RES. 10K, 1/4W, 5%	1300479	44

QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

FIRST USED ON OPTION MODEL

ETCH BOARD REV D

DEC NO.	EIA NO.	DEC NO.	EIA NO.

SEMICONDUCTOR CONVERSION CHART

REV	CHANGE NO.	ORIGINATED	CHK
C	M7807-00001	3-3-75 W. FRANCK	
D	M7807-00002	4-28-75 J. McINTYRE	
E	M7807-00003	6-11-75 J. McNAMARA	
F	M7807-00004	7-8-75 R. HARRINGTON	
H			

REVISIONS

DRWN Tom Fennell 1/28/74
CHKD [illegible] 2/14/74
ENGR [illegible] 2/20/74
PROJ ENGR [illegible] 2/20/74
PROD ENGR [illegible] 2/20/74
NEXT HIGHER ASSY
SCALE
SHEET 1 OF 7

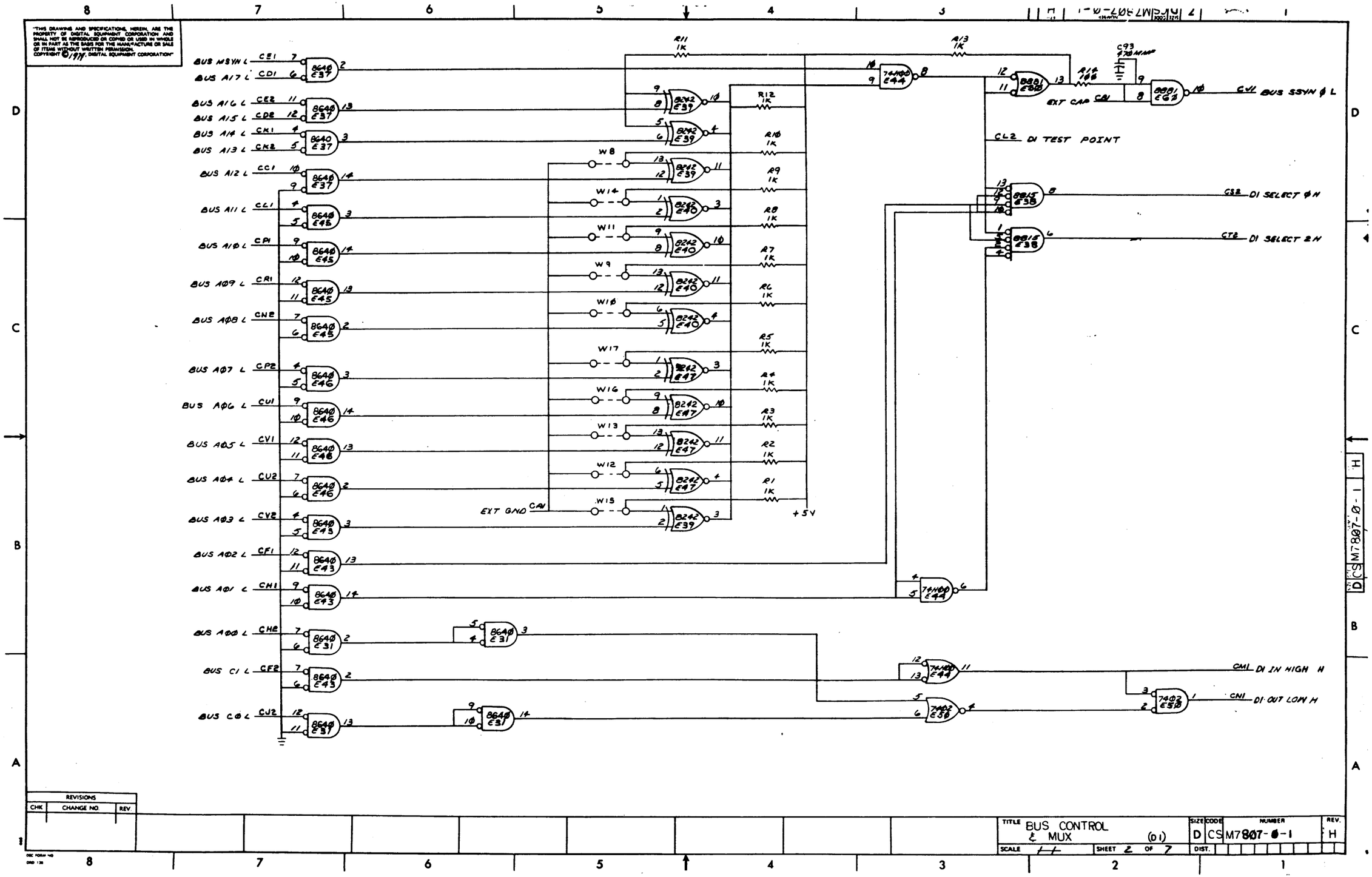
digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE BUS CONTROL & MUX

SIZE D | CODE CS | NUMBER M7807-0-1 | REV H

DIST.

DCSM7807-0-1 H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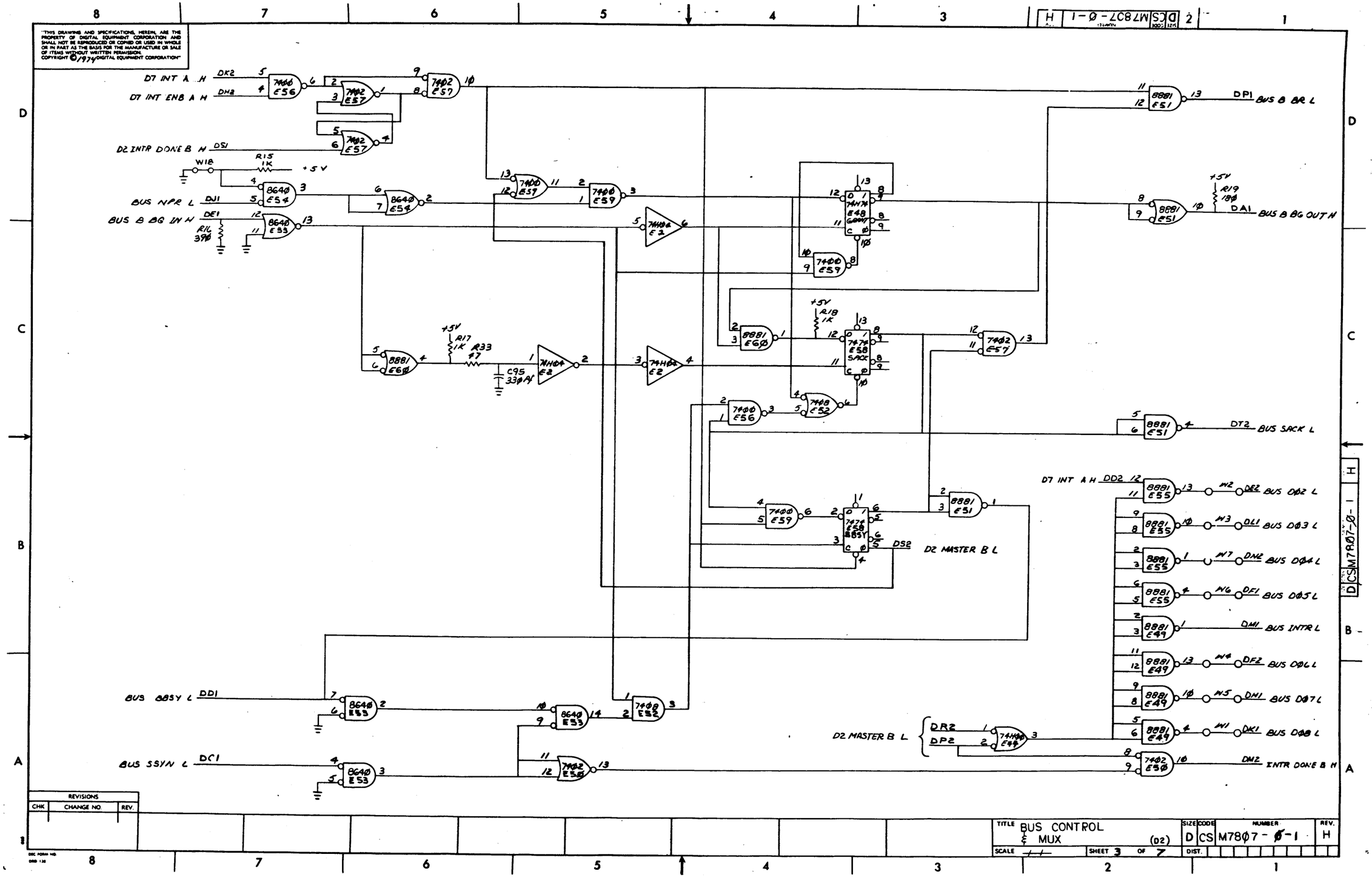
BUS MSYN L
BUS A17 L
BUS A16 L
BUS A15 L
BUS A14 L
BUS A13 L
BUS A12 L
BUS A11 L
BUS A10 L
BUS A09 L
BUS A08 L
BUS A07 L
BUS A06 L
BUS A05 L
BUS A04 L
BUS A03 L
BUS A02 L
BUS A01 L
BUS A00 L
BUS C1 L
BUS C0 L
EXT GND
+5V
EXT CAP
CL2 D1 TEST POINT
CS2 D1 SELECT 0 H
CT2 D1 SELECT 2 H
CM1 D1 IN HIGH H
CN1 D1 OUT LOW H
CV1 BUS SSYN 0 L
REVISIONS
CHK
CHANGE NO.
REV.
TITLE BUS CONTROL & MUX (D1)
SIZE D
CODE CS
NUMBER M7807-0-1
REV. H
SCALE
SHEET 2 OF 7
DIST.



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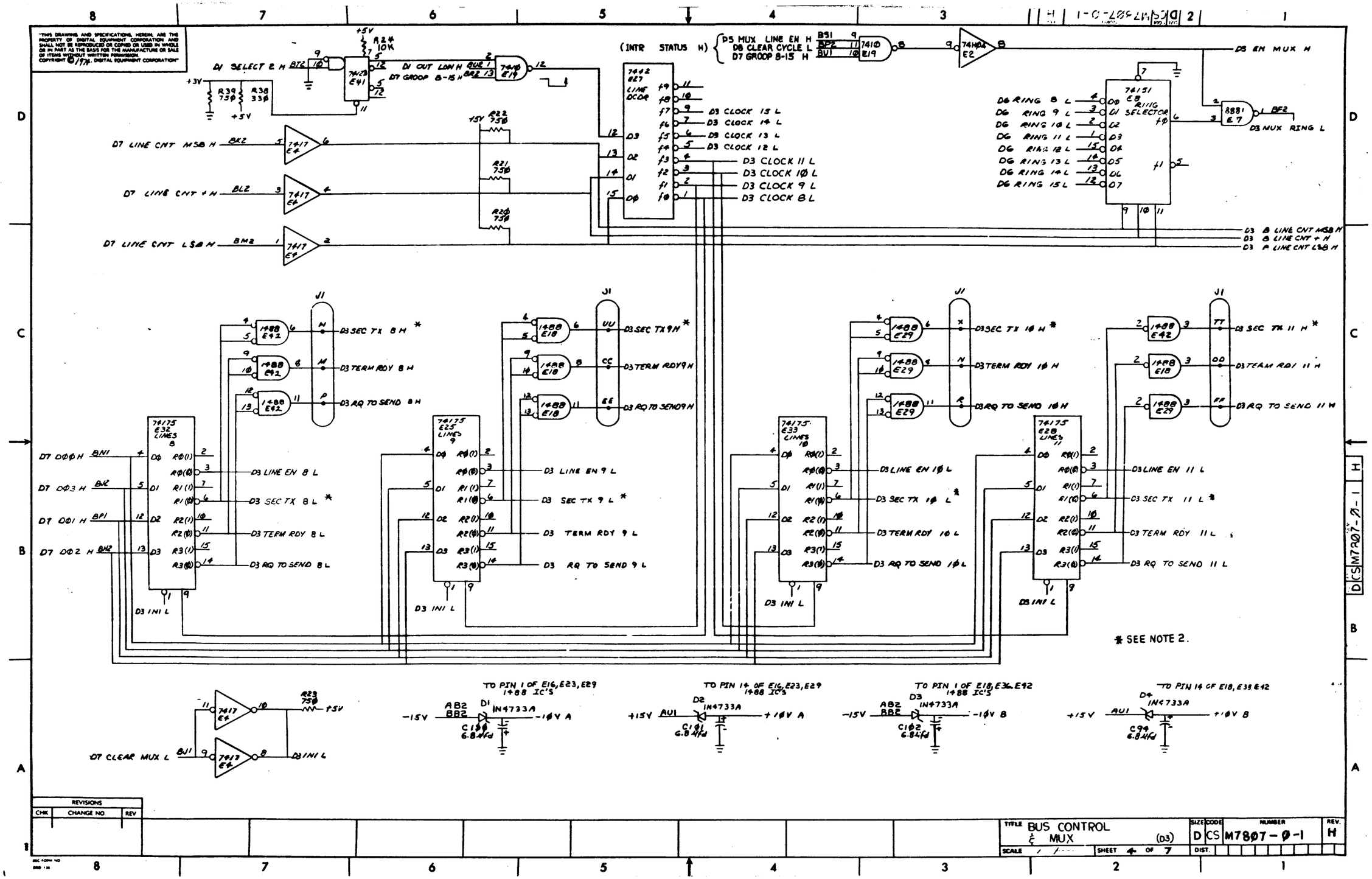
D7 INT A H
D7 INT ENB A H
D2 INTR DONE B H
BUS NPR L
BUS B BG IN H
BUS BBSY L
BUS SSYN L
D2 MASTER B L
D7 INT A H
D2 MASTER B L
DP1 BUS B BR L
DA1 BUS B BG OUT H
DT2 BUS SACK L
DE2 BUS DØ2 L
DL1 BUS DØ3 L
DN2 BUS DØ4 L
DF1 BUS DØ5 L
DM1 BUS INTR L
DF2 BUS DØ6 L
DH1 BUS DØ7 L
DK1 BUS DØ8 L
DM2 INTR DONE B H
REVISIONS
CHK
CHANGE NO.
REV.
TITLE BUS CONTROL & MUX (D2)
SIZE D
CODE CS
NUMBER M78Ø7-Ø-1
REV. H
SCALE
SHEET 3 OF 7
DIST.



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REVISIONS		
CHK	CHANGE NO.	REV

TITLE BUS CONTROL & MUX (D3)

SIZE D | CODE CS | NUMBER M7807-0-1 | REV. H

SCALE / / | SHEET 4 OF 7 | DIST.

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D3 EN MUX H

D4 MUX CARRIER L

D4 MUX CLEAR TO SEND L

D4 MUX SEC RX L

D3 B LINE CNT LSB H
D3 B LINE CNT + H
D3 B LINE CNT MSB H

D3 INI L
D3 CLOCK 12 L

D3 INI L
D3 CLOCK 13 L

D3 INI L
D3 CLOCK 14 L

D7 D00 H (BN1)
D7 D03 H (BYTE)
D7 D01 H (BP1)
D7 D02 H (SHE)

* SEE NOTE 2

REVISIONS		
CHK	CHANGE NO	REV.

TITLE	SIZE	CODE	NUMBER	REV.
BUS CONTROL & MUX (D4)	D	CS	M7807-0-1	H
SCALE 1/1 — SHEET 5 OF 7 — DIST.				

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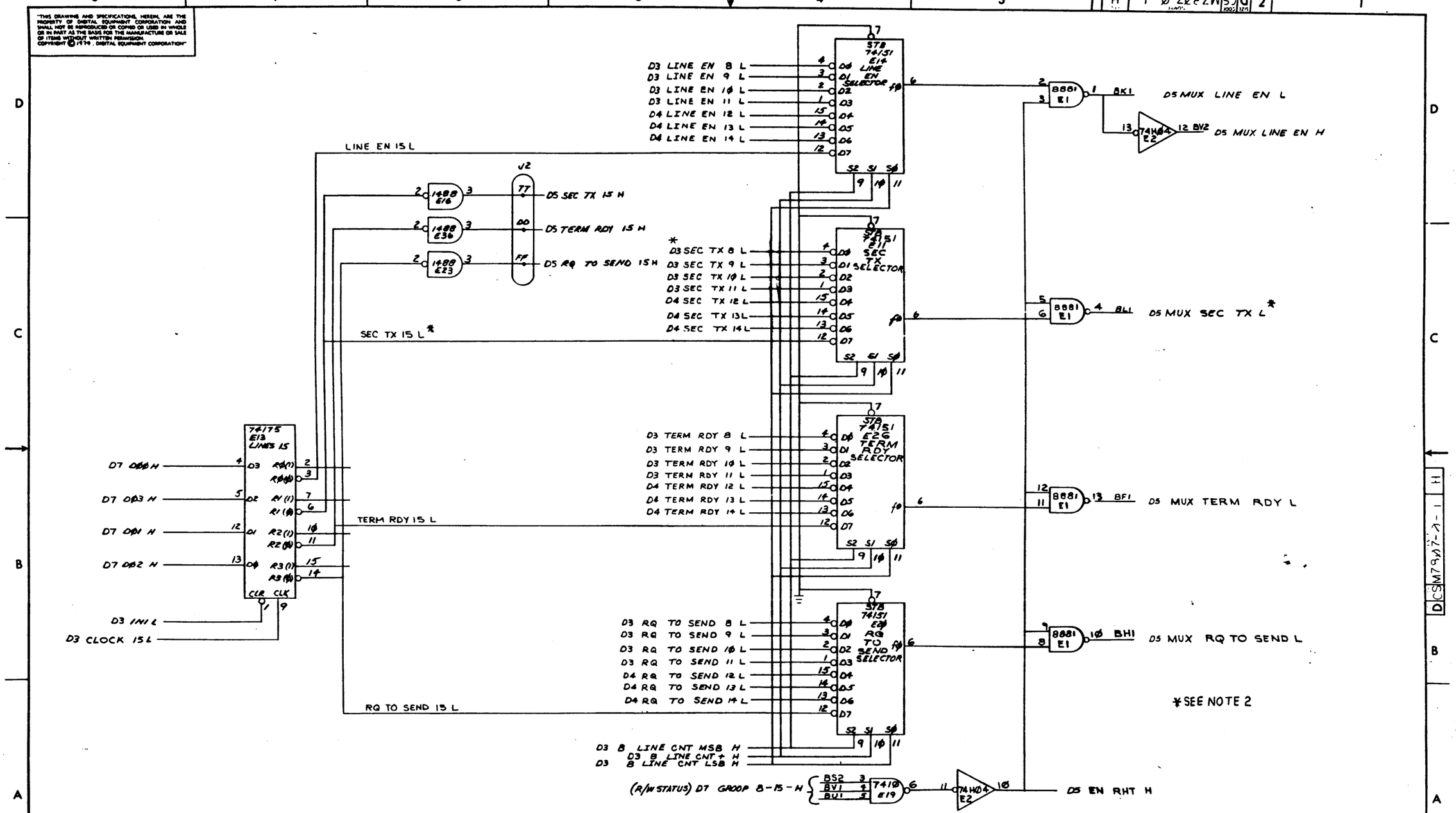

REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV.
BUS CONTROL & MUX (D5)	D	CS	M7807-0-1	H
SCALE 1-1 SHEET 6 OF 7	DIST.			

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J1 K RING 8 H → 14LS00 E3 pin 1 → pin 3 DG RING 8 L; C76 .47µf; R25 33K; -15V
J1 AA RING 9 H → 14LS00 E3 pin 4 → pin 6 DG RING 9 L; C69 .47µf; R26 33K
J1 L RING 10 H → 14LS00 E5 pin 13 → pin 11 DG RING 10 L; C64 .47µf; R27 33K
J1 BB RING 11 H → 14LS00 E5 pin 10 → pin 8 DG RING 11 L; C63 .47µf; R28 33K
J2 K RING 12 H → 14LS00 E9 pin 1 → pin 3 DG RING 12 L; C76 .47µf; R29 33K
J2 AA RING 13 H → 14LS00 E9 pin 4 → pin 6 DG RING 13 L; C75 .47µf; R30 33K
J2 L RING 14 H → 14LS00 E9 pin 13 → pin 11 DG RING 14 L; C74 .47µf; R31 33K
J2 BB RING 15 H → 14LS00 E9 pin 10 → pin 8 DG RING 15 L; C73 .47µf; R32 33K

J1 U CARRIER 8 H → 14LS00 E6 pin 1 → pin 3 DG CARRIER 8 L; C68 .47µf
J1 KK CARRIER 9 H → 14LS00 E6 pin 4 → pin 6 DG CARRIER 9 L; C71 .47µf
J1 V CARRIER 10 H → 14LS00 E6 pin 13 → pin 11 DG CARRIER 10 L; C72 .47µf
J1 LL CARRIER 11 H → 14LS00 E6 pin 10 → pin 8 DG CARRIER 11 L; C66 .47µf
J2 U CARRIER 12 H → 14LS00 E30 pin 1 → pin 3 DG CARRIER 12 L; C91 .47µf
J2 KK CARRIER 13 H → 14LS00 E30 pin 4 → pin 6 DG CARRIER 13 L; C92 .47µf
J2 V CARRIER 14 H → 14LS00 E30 pin 13 → pin 11 DG CARRIER 14 L; C90 .47µf
J2 LL CARRIER 15 H → 14LS00 E30 pin 10 → pin 8 DG CARRIER 15 L; C88 .47µf

J1 S CLEAR TO SEND 8 H → 14LS00 E12 pin 1 → pin 3 DG CLEAR TO SEND 8 L; C80 .47µf
J1 NN CLEAR TO SEND 9 H → 14LS00 E12 pin 4 → pin 6 DG CLEAR TO SEND 9 L; C79 .47µf
J1 T CLEAR TO SEND 10 H → 14LS00 E12 pin 13 → pin 11 DG CLEAR TO SEND 10 L; C77 .47µf
J1 VV CLEAR TO SEND 11 H → 14LS00 E12 pin 10 → pin 8 DG CLEAR TO SEND 11 L; C78 .47µf
J2 S CLEAR TO SEND 12 H → 14LS00 E17 pin 1 → pin 3 DG CLEAR TO SEND 12 L; C84 .47µf
J2 NN CLEAR TO SEND 13 H → 14LS00 E17 pin 4 → pin 6 DG CLEAR TO SEND 13 L; C83 .47µf
J2 T CLEAR TO SEND 14 H → 14LS00 E17 pin 13 → pin 11 DG CLEAR TO SEND 14 L; C82 .47µf
J2 VV CLEAR TO SEND 15 H → 14LS00 E17 pin 10 → pin 8 DG CLEAR TO SEND 15 L; C81 .47µf

J1 Y SEC RX 8 H * → 14LS00 E3 pin 1 → pin 3 DG SEC RX 8 L *; C67 .47µf
J1 SS SEC RX 9 H * → 14LS00 E3 pin 4 → pin 6 DG SEC RX 9 L *; C65 .47µf
J1 EE SEC RX 10 H * → 14LS00 E3 pin 13 → pin 11 DG SEC RX 10 L *; C61 .47µf
J1 VV SEC RX 11 H * → 14LS00 E3 pin 10 → pin 8 DG SEC RX 11 L *; C62 .47µf
J2 Y SEC RX 12 H * → 14LS00 E24 pin 1 → pin 3 DG SEC RX 12 L *; C87 .47µf
J2 SS SEC RX 13 H * → 14LS00 E24 pin 4 → pin 6 DG SEC RX 13 L *; C89 .47µf
J2 EE SEC RX 14 H * → 14LS00 E24 pin 13 → pin 11 DG SEC RX 14 L *; C86 .47µf
J2 VV SEC RX 15 H * → 14LS00 E24 pin 10 → pin 8 DG SEC RX 15 L *; C85 .47µf

* SEE NOTE 2.

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
BUS CONTROL & MUX (D6)	D	CS	M7807-0-1	H
SCALE —	SHEET 7 OF 7	DIST.		

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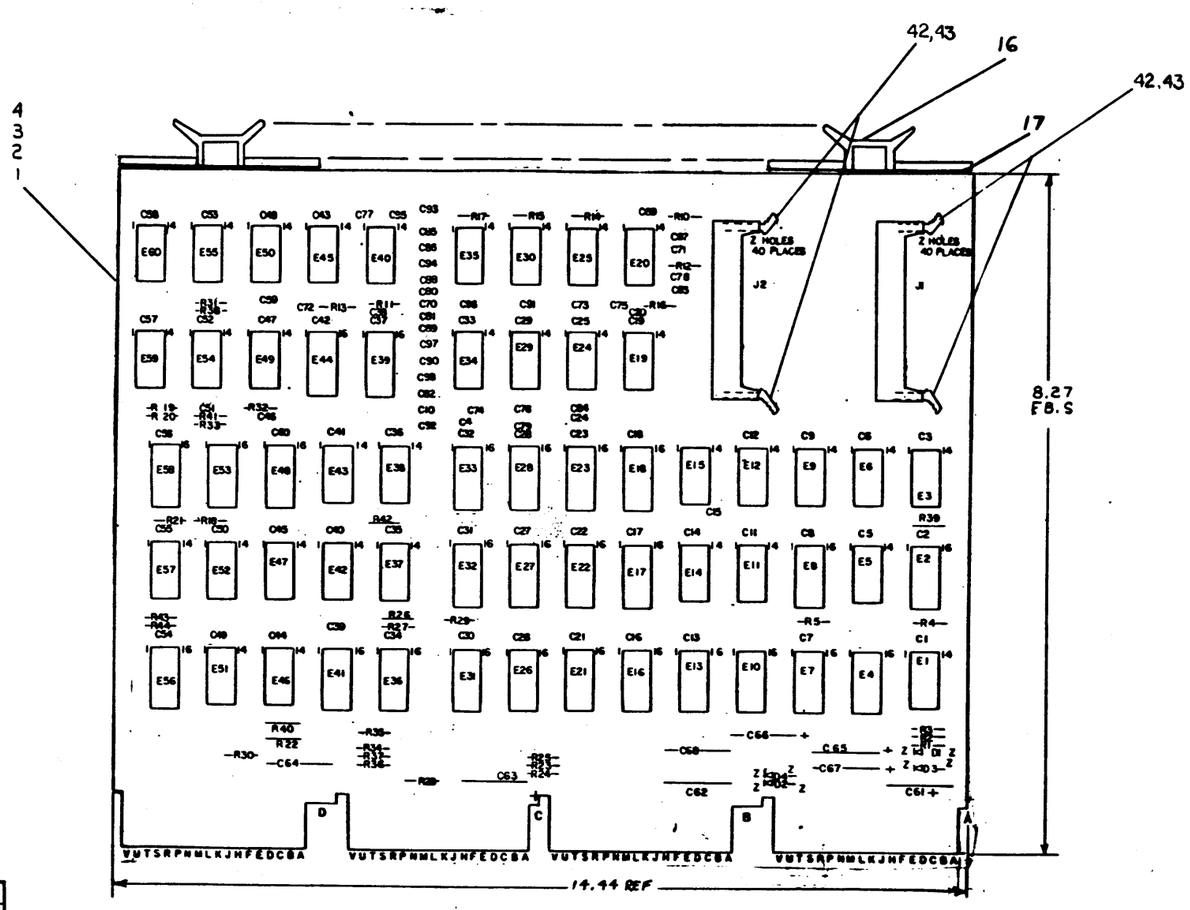
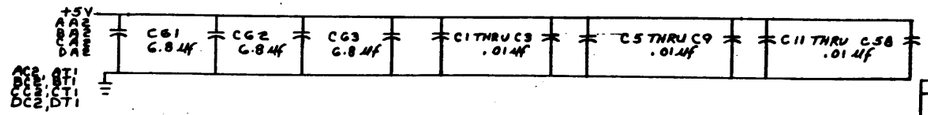
NOTES:

1. FOR −15V TO −10V AND +15V TO +10V SEE SHEET 7 OF 7
2. THE SIGNALS "SEC TX" AND "SEC Rx" REFER TO ASYNCHRONOUS OPERATION ONLY. WHEN THE MODULE IS USED IN A SYNCHRONOUS APPLICATION THE SIGNALS MAY BE USED AS "NEW SYNC" AND "DATA SET RDY" FOR THAT LINE.





DEC 4015	8	16
DEC 8271	8	16
DEC 7489	8	16
DEC 8640	1	8
DEC 8266	8	16
DEC 74123	8	16
DEC 7442	8	16
DEC 74175	8	16
DEC 74131	8	16
IC TYPE	GND	+ 5V

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

REVISIONS			
REV	CHNG NO.	ORIGINATED	DATE
J	M7808-00005	R. HARRINGTON	3-6-74
H	M7808-00004	J. MCNAMARA	2-27-74
F	M7808-00003	J. MCINTYRE	2-12-74
E	M7808-00002	W. FANDRICK	1-31-74
D	M7808-0000	ORIGINATED	1-3-74
C	ORIGINATED		

DEC NO.	EIA NO.

SEMICONDUCTOR CONVERSION CHART

FIRST USED ON OPTION MODEL

REF			
REF		X-Y COORDINATE HOLE LOCATION	H-CB-M7808-0-4
REF		ASSY/DRILL HOLE LAYOUT	D-AH-M7808-0-5
REF		MODULE ECO HISTORY	D-HH-M7808-0-6
1		ETCHED CIRCUIT BOARD	5010884
98	C1-3,5-9,11-98	CAP .01 MF, 100V, ± 20%	1001610-00
33	C4,10,58,59-98	CAP 470 PF, 100V, ± 5%	1000824
1	C99	CAP 82 PF, 100V, ± 5%	1000815
8	C61 THRU C68	CAP 6.8 MF, 35V, ± 10%	1000300
4	D1,2,3,4	DIODE 1N4733A ZENER	1100843
2	J1,J2	CONNECTOR 40 PIN	1200841
28	R1-4,10-30,32-98,40-43	RES. 750 1/4W 5%	1301401
1	R31	RES. 220 1/4W 5%	1300271
8	R10-17	RES. 33K 1/4W 10%	1300510
~~5~~	~~R5,6,7,8~~	~~RES. 330 1/4W 5%~~	~~1300295~~
1	R44	RES. 330 1/4W 5%	1300295
4		HANDLE FLIP CHIP	9000337-00
8		EYELET	9000732
1	E99	I.C. DEC 7474	1000647
8	E19,20,24,25,29,30,34,35	I.C. DEC 1489L	1010323
8	E17,18,22,23,27,28,32,33	I.C. DEC 74151	1000936
8	E4,7,10,13,18,21,26,31	I.C. DEC 74175	1010051
6	E5,6,9,11,12,15	I.C. DEC 1488	1010322
2	E14,40	I.C. DEC 7410	1000578
1	E2	I.C. DEC 7442	1010048
2	E1,42	I.C. DEC 7417	1000829
1	E8	I.C. DEC 74123	1010430
4	E3,38,54,98	I.C. DEC 8881	1000705
2	E35,53	I.C. DEC 8288	1000934
2	E41,44	I.C. DEC 8830	1011117
1	E45	I.C. DEC 8640	1011469
1	E51	I.C. DEC 7418	1000828
1	E99	I.C. DEC 7400	1010300
1	E37	I.C. DEC 74107	1010035
2	E46,47	I.C. DEC 7400	1000575
1	E52	I.C. DEC 7400	1010195
2	E55,57	I.C. DEC 8815	1000713
2	E40,43	I.C. DEC 7404	1000600
1	E48	I.C. DEC 8271	1000815
2	E39,58	I.C. DEC 4015	1010007
1	E50	I.C. DEC 7400	1010011
2	R9,39	RES. 10K,1/4W, 5%	1300479
2		LEFT LATCH	1209941-03
2		RIGHT LATCH	1209941-04
A/R		WIRE 30 AWG	9105740-55

QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO

PARTS LIST

ETCH BOARD REV D

DRWN	E. Wilson	DATE 7/3/74
CHKD	[illegible]	DATE 7/3/74
ENGR	[illegible]	DATE 7-10-74
PROJ ENGR	[illegible]	DATE 9-10-74
PROJ	[illegible]	DATE 7-23-74

NEXT HIGHER ASSY

SCALE NONE

SHEET 1 OF 7

digital EQUIPMENT CORPORATION

TITLE: MODEM CONTROL

SIZE D | CODE DCS | NUMBER M7808-0-1 | REV J

DIST.

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NOTE:

* REMOVE WIRE TO INHIBIT INTERUPTS FROM TRANSITIONS.

* SEE NOTE 2.

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
MODEM CONTROL (07)	D	CS	M7808-0-1	J
SCALE	SHEET 2 OF 7		DIST.	

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+3V

D7 LINE CNT +H
D7 LINE CNT MSB H
D7 GROOP 8-15 H
D7 LINE CUNT LSB H
8815 E57
7410 E49
7474 E50
DRI DB CLEAR CYCLE (Ø) L
D7 CLEAR SCAN L

+5V D7 LD HOLD H DVI
7404 E48

+5V
R23 750 R24 750 R25 750 R22 750
R18 750 R19 750 R20 750 R21 750

D7 MAINT MODE(1) H
7416 E51
D4,DIØ MUX CLEAR TO SEND L CDI
D4,DIØ MUX CARRIER L CAI
D3,D9 MUX RING L CCI

D4,DIØ MUX SEC RC L CBI
7489 E56
WR ENB
DØ MØ(1)
D1 M1(1)
D2 M2(1)
D3 M3(1)
A3 A2 A1 AØ

D7 GROOP 8-15 H DV2
D7 LINE CNT MBS H DU2
D7 LINE CNT +H DU1
D7 LINE CNT LSB H DSI

7486 E59
7408 E53
7404 E48
D7 RD SCAN STATUS H
8881 E60
8881 E69
8881 E69
8881 E69
8816 E55
+3V
DRZ DB BUS DATA 12 L
DIZ DB BUS DATA 13 L
DSZ DB BUS DATA 14 L
DPZ DB BUS DATA 15 L
7486 E59
DB TRANSITION DET H

4Ø15 E58
D3 R3(1)
SET 3
D2 R2(1)
SET 2
D1 R1(1)
SET 1
DØ RØ(1)
SET Ø
CLR CLK
+3V
D7 LD HOLD H DPI

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
MODEM CONTROL (D8)	D	CS	M7808-0-1	U
SCALE	SHEET 3 OF 7	DIST.		

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D1 SELECT 2H — BT2 — 74123 E8 — R5 10K +5V — D1 OUT LOW H BUS 7 — BUS 13 — 7410 E14 — 12

R44 330Ω +5V — R43 75Ø +3V — +5V — R3 75Ø — R2 75Ø — R1 75Ø

D7 LINE CNT MSB H — BK2 — 13 — 7417 E1 — 12 — D3
D7 LINE CNT + H — BL2 — 11 — 7417 E1 — 10 — D2
D7 LINE CNT LSB H — BM2 — 9 — 7417 E1 — 8 — D1

7442 E2 — D9 CLOCK 7 L, D9 CLOCK 6 L, D9 CLOCK 5 L, D9 CLOCK 4 L, D9 CLOCK 3L, D9 CLOCK 2L, D9 CLOCK 1L, D9 CLOCK ØL

3H MUX LINE EN H — BS1 — 7410 E14 — 8 — 13 — 7407 E23 — 12 — D9 EN MUX H

D12 RING Ø L, D12 RING 1 L, D12 RING 2 L, D12 RING 3 L, D12 RING 4 L, D12 RING 5 L, D12 RING 6 L, D12 RING 7 L — 74151 E18 — S2 S1 SØ — 9 10 11 — F1 — 5 — F2 — 6 — 74001 E3 — 12 — 13 BF2 — D9 MUX RING L

D9 B LINE CNT MSB H
D9 B LINE CNT + H
D9 B LINE CNT LSB H

D11 GROUP Ø-7 H — BS2 — 11

J1

1488 E6 — W — D9 SEC TX Ø H *
1488 E6 — M — D9 TERM RDY Ø H
1488 E6 — P — D9 RQ TO SEND Ø H

1488 E5 — UU — D9 SEC TX 1 H *
1488 E5 — CC — D9 TERM RDY 1 H
1488 E5 — EE — D9 RQ TO SEND 1 H

1488 E7 — X — D9 SEC TX 2 H *
1488 E7 — N — D9 TERM RDY 2 H
1488 E7 — R — D9 RQ TO SEND 2 H

1488 E6 — TT — D9 SEC TX 3 H *
1488 E5 — DD — D9 TERM RDY 3 H
1488 E7 — FF — D9 RQ TO SEND 3 H

D7 DØØ H — BN1 — 74175 E4 LINE Ø — D9 LINE EN Ø L
D7 DØ3 H — BJ2 — D9 SEC TX Ø L *
D7 DØ1 H — BP1 — D9 TERM RDY Ø L
D7 DØ2 H — BH2 — D9 RQ TO SEND Ø L
D9 INI L

74175 E7 LINE 1 — D9 LINE EN 1 L, D9 SEC TX 1 L *, D9 TERM RDY 1 L, D9 RQ TO SEND 1 L — D9 INI L

74175 E10 LINE 2 — D9 LINE EN 2 L, D9 SEC TX 2 L *, D9 TERM RDY 2 L, D9 RQ TO SEND 2 L — D9 INI L

74175 E13 LINE 3 — D9 LINE EN 3 L, D9 SEC TX 3 L *, D9 TERM RDY 3L, D9 RQ TO SEND 3 L — D9 INI L

D7 CLEAR MUX L — BJ1 — 7417 E1 — R4 75Ø +5V — D9 INI L

D1 IN4733A — (TO PIN 3 OF 3 1488 IC'S) — −15V — AB2 BB2 — C65 6.8μF — −10V

D2 IN4733A — (TO PIN 14 OF 3 1488 IC'S) — +15V — AU1 — C66 6.8μF — +10V

*SEE NOTE 2.

REVISIONS		
CHK	CHANGE NO.	REV.

(MUX)
TITLE: MODEM CONTROL (D9)
SIZE: D | CODE: CS | NUMBER: M78Ø8-Ø-1 | REV: J
SCALE | SHEET 4 OF 7 | DIST.

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D9 EN MUX H

D1Z CARRIER Ø L
D1Z CARRIER 1 L
D1Z CARRIER 2 L
D1Z CARRIER 3 L
D1Z CARRIER 4 L
D1Z CARRIER 5 L
D1Z CARRIER 6 L
D1Z CARRIER 7 L

S7B 74151 E23 CARRIER SELECTOR

8881 E3 → D1Ø BB1 MUX CARRIER L

D1Z CLEAR TO SEND Ø L
D1Z CLEAR TO SEND 1 L
D1Z CLEAR TO SEND 2 L
D1Z CLEAR TO SEND 3 L
D1Z CLEAR TO SEND 4 L
D1Z CLEAR TO SEND 5 L
D1Z CLEAR TO SEND 6 L
D1Z CLEAR TO SEND 7 L

S7B 74151 E28 CLEAR TO SEND SELECTOR

8881 E3 → 4 BC1 D1Ø MUX CLEAR TO SEND L

*D1Z SEC RX ØL
D1Z SEC RX 1 L
D1Z SEC RX 2L
D1Z SEC RX 3L
D1Z SEC RX 4 L
D1Z SEC RX 5L
D1Z SEC RX 6L
D1Z SEC RX 7L

S7B 74151 E33 SEC RX SELECTOR

8881 E3 → 16 BA1 * D1Ø MUX SEC RX L

D9 LINE CNT LSB H
D9 LINE CNT + H
D9 LINE CNT MSB H

J2

1488 E12 → D1Ø SEC TX 4 H *
1488 E12 → D1Ø TERM RDY 4 H
1488 E12 → D1Ø RQ TO SEND 4 H

74175 E16 LINE 4

LINE EN 4 L
SEC TX 4 L *
TERM RDY 4 L
RQ TO SEND 4 L

D9 INI L
D9 CLOCK 4 L

J2

1488 E11 → D1Ø SEC TX 5 H *
1488 E11 → D1Ø TERM RDY 5 H
1488 E11 → D1Ø RQ TO SEND 5 H

74175 E21 LINE 5

LINE EN 5 L
SEC TX 5 L
TERM RDY 5 L
RQ TO SEND 5 L

D9 INI L
D9 CLOCK 5 L

J2

1488 E15 → D1Ø SEC TX 6 H *
1488 E15 → D1Ø TERM RDY 6 H
1488 E15 → D1Ø RQ TO SEND 6 H

74175 E26 LINE 6

LINE EN 6 L
SEC TX 6 L *
TERM RDY 6 L
RQ TO SEND 6 L

D9 INT L
D9 CLOCK 6 L

D1Ø D0 H
D1Ø D3 H
D1Ø D1 H
D1Ø D2 H

D3 IN4733A (TO PIN 1 OF 3 1488 IC'S)
-15V → A82 B82 → C67 6.8μF → -10V

D4 IN4733A (TO PIN 14 OF 3 1488 IC'S)
+15V → AU1 → C68 6.8μF → +10V

* SEE NOTE 2.

REVISIONS		
CHK	CHANGE NO	REV

(MUX)
TITLE: MODEM CONTROL (D1Ø)
SIZE: D | CODE: CS | NUMBER: M78Ø8-Ø-1 | REV: J
SCALE | SHEET 5 OF 7 | DIST.

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D7 6P08P 6-7 H
B52

D9 LINE EN Ø L
D9 LINE EN 1 L
D9 LINE EN 2 L
D9 LINE EN 3 L
D10 LINE EN 4 L
D10 LINE EN 5 L
D10 LINE EN 6 L

74151 E17 LINE EN SELECTOR

8881 E38 → BK1 D11 MUX LINE EN L

8815 E55 → BV2 D11 MUX LINE EN H

LINE EN 7 L

J2

1488 E12 → TT → D11 SEC TX 7 H

1488 E11 → DD → D11 TERM RDY 7 H *

1488 E15 → FF → D11 RQ TO SEND 7 H

D9 SEC TX Ø L
D9 SEC TX 1 L
D9 SEC TX 2 L
D9 SEC TX 3 L
D10 SEC TX 4 L
D10 SEC TX 5 L
D10 SEC TX 6 L

74151 E22 SEC TX SELECTOR

8881 E38 → BL1 D11 * MUX SEC TX L

* SEC TX 7 L

D7, DØØ H
D7, DØ3 H
D7, DØ1 H
D7, DØ2 H
D9 INT L
D9 CLOCK 7 L

74175 E31 LINE 7

TERM RDY 7 L

D9 TERM RDYØ L
D9 TERM RDY 1 L
D9 TERM RDY 2 L
D9 TERM RDY 3 L
D10 TERM RDY 4 L
D10 TERM RDY 5 L
D10 TERM RDY 6 L

74151 E27 TERM RDY SELECTOR

8881 E38 → BF1 D11 MUX TERM RDY L

D9 RQ TO SEND Ø L
D9 RQ TO SEND 1 L
D9 RQ TO SEND 2 L
D9 RQ TO SEND 3 L
D10 RQ TO SEND 4 L
D10 RQ TO SEND 5 L
D10 RQ TO SEND 6 L

74151 E32 RQ TO SEND SELECTOR

8881 E38 → BH1 D11 MUX RQ TO SEND L

RQ TO SEND 7 L

D9 LINE CNT MSB H
D9 LINE CNT + H
D9 LINE CNT LSB H

* SEE NOTE 2.

REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV.
MODEM CONTROL (D11)	D	CS	M7808-0-1	J
SCALE	SHEET 6 OF 7	DIST.		

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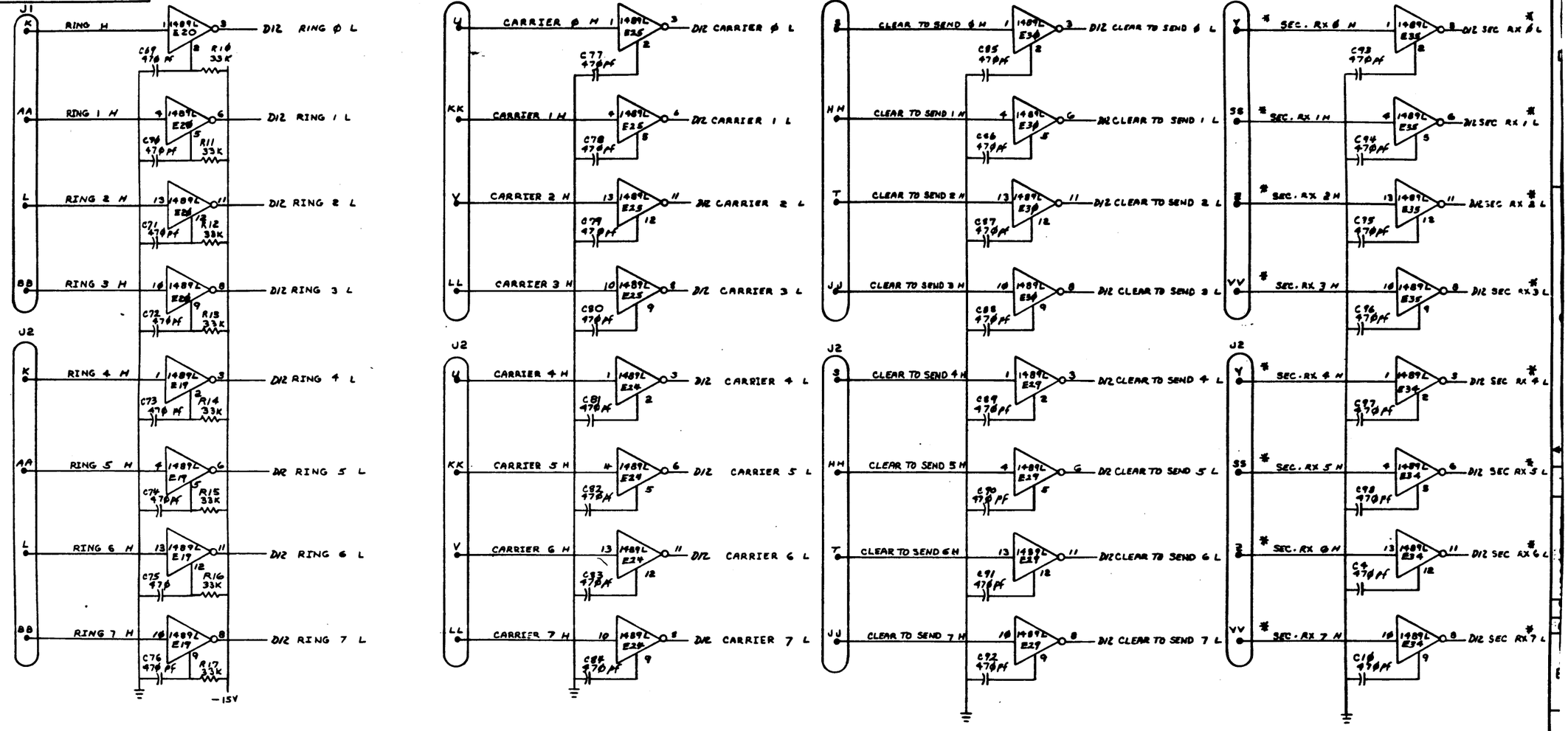

* SEE NOTE 2

REVISIONS		
CHK	CHANGE NO	REV

(EIA LEVEL CONVERTERS)

TITLE	SIZE	CODE	NUMBER	REV.
MODEM CONTROL (DI2)	D	CS	M78ØB-Ø-1	J
SCALE	SHEET 7 OF 7		DIST.	