EK-DHU11-UG-002

DHU11 Interface User's Guide

digital™

EK-DHU11-UG-002

DHU11 Interface User's Guide

Prepared by Educational Services
of
Digital Equipment Corporation

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PREFACE

This document describes the DHU11 and its installation requirements. It contains information on user-level maintenance. A substantial programming chapter and a glossary are included.

This manual was written primarily for the DHU11 user. However, information concerning such items as option installation and checkout is intended for qualified Field Service personnel.

The manual is organized into four chapters plus appendices.

Chapter 1	–	Introduction
Chapter 2	–	Installation
Chapter 3	–	Programming
Chapter 4	–	Maintenance
Appendix A	–	Glossary of Terms
Appendix B	–	Modem Control

The following is a list of related titles.

Document	**Number**
Communications Mini-Reference Guide	EK-CMINI-RM
Terminals and Communications Handbook	EB-20752-20
DHU11 Technical Manual	EK-DHU11-TM
DHU11 Maintenance Card	EK-DHU11-MC
DHU11 Field Maintenance Print Set	MP-01794-01

CHAPTER 1
INTRODUCTION

1.1 SCOPE

Chapter 1 provides general information and specifications. It describes how the module can be configured, and how it interfaces with the system bus and the serial data lines. Physical and functional descriptions are also included.

1.2 OVERVIEW

1.2.1 General Description

The DHU11 option is an asynchronous multiplexer which provides 16 full-duplex, asynchronous, serial data channels on UNIBUS systems. The option can be used in many applications. These include data concentration, terminal interfacing, and cluster controlling.

The main features of the DHU11 are as follows.

- Sixteen full-duplex asynchronous data channels
- A 256-entry first-in-first-out (FIFO) buffer for received characters, dataset status changes, and diagnostic information
- DMA or programmed transfers on transmit. Each channel has a 64-byte FIFO for output data
- Programmable delay-timer for receive interrupts
- RS-423-A/V.10/X.26 and RS-232-C/V.28 compatible
- Full-duplex point-to-point or auto-answer dial-up operation
- Programmable split speed per line
- Total module throughput of 15 000 characters per second
- Automatic flow control of transmitted and received data
- Self-test and background monitor diagnostics
- Programmable test facilities
- Single hex-height module (M3105)
- All communications functions are programmable

Enough modem control is provided on all 16 channels to allow auto-answer dial-up operation over the public switched telephone network (PSTN). The DHU11 can also be used for point-to-point operation over private lines. Modem control is implemented by software in the host.

The module provides DMA or programmed transfers from the host system to the serial lines via sixteen 64-byte FIFO buffers (one per channel). A common 256-character FIFO buffer is provided for data received **from** the serial lines.

By using microcomputers (referred to as PROC 1 and PROC 2 in this manual) the DHU11 releases the host system from many of the data-handling tasks.

One 8051 microcomputer controls DMA transmissions from the host system to the DHU11. A second 8051 controls eight DUARTs which carry out the serial/parallel and parallel/serial conversion of data.

The DHU11 carries ROM-based diagnostics which are executed independently of the host. A full range of diagnostic programs is also available for both PDP-11 and VAX-11 systems.

A green LED gives the GO/NO-GO status of the module. More detailed diagnostic information is also made available to the host system via the received-character FIFO. Loopback test connectors are supplied for use with the system-based diagnostics.

I/O addresses, interrupt vectors, and interrupt priority for the module are selected on three switchpacks. All other DHU11 functions and configurations are programmable.

To prevent loss of data at high throughput levels, the DHU11 can be programmed for automatic flow control using XON and XOFF characters.

1.2.2 Physical Description

The DHU11 consists of a module kit DHU11-M, and one of several cabkits. The DHU11-M consists of:

- A hex-height module (M3105)
- The DHU11 Interface User Guide (EK-DHU11-UG).

Figure 1-1 shows major features of the module. Its dimensions are 21.4 cm × 39.9 cm (8.4 inches × 15.7 inches). The module is connected to the backplane via connectors A to F. J1 to J4 are connected to the communications lines via BC05L cables, and distribution panels.

1.2.3 Versions of DHU11

To facilitate installation in different system packages, and to allow installation in unshielded cabinets, the DHU11 can be supplied in four upgrade-kit versions. All versions consist of the DHU11-M and cabkit.

The four cabkits are:

CK-DHU11-A1	For unshielded cabinets – (19-inch rack mount)
CK-DHU11-AD	For general-purpose expansion cabinets
CK-DHU11-AE	For VAX-11/730 and VAX-11/750 kernel systems
CK-DHU11-AF	For VAX-11/725 systems

Cabkit details are given in Chapter 2, Installation.

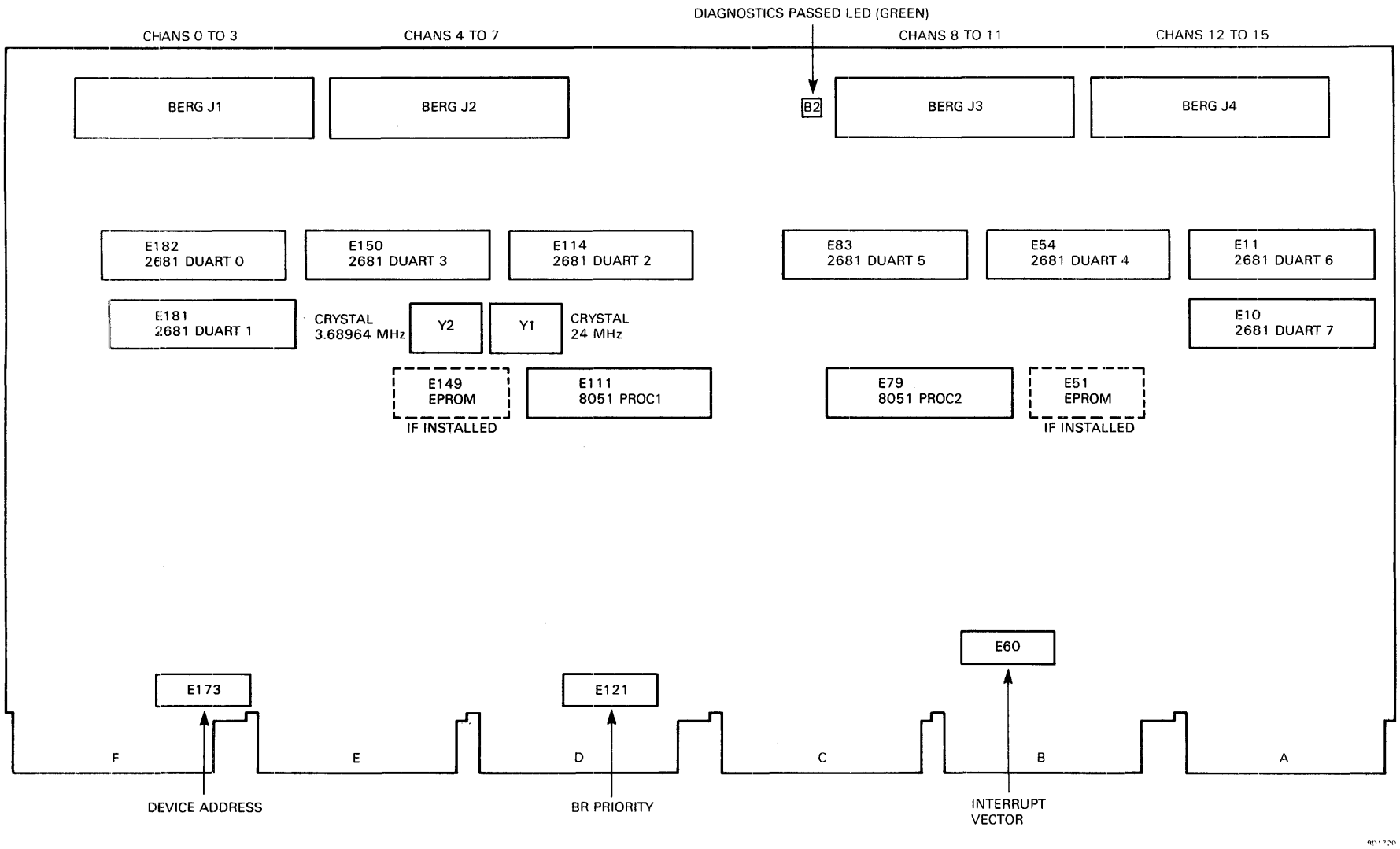


Figure 1-1 M3105 Module

1.2.4 Configurations

Figure 1-2 shows some possible DHU11 configurations. Any or all of the data channels can be connected to a terminal or to a data-communications line.

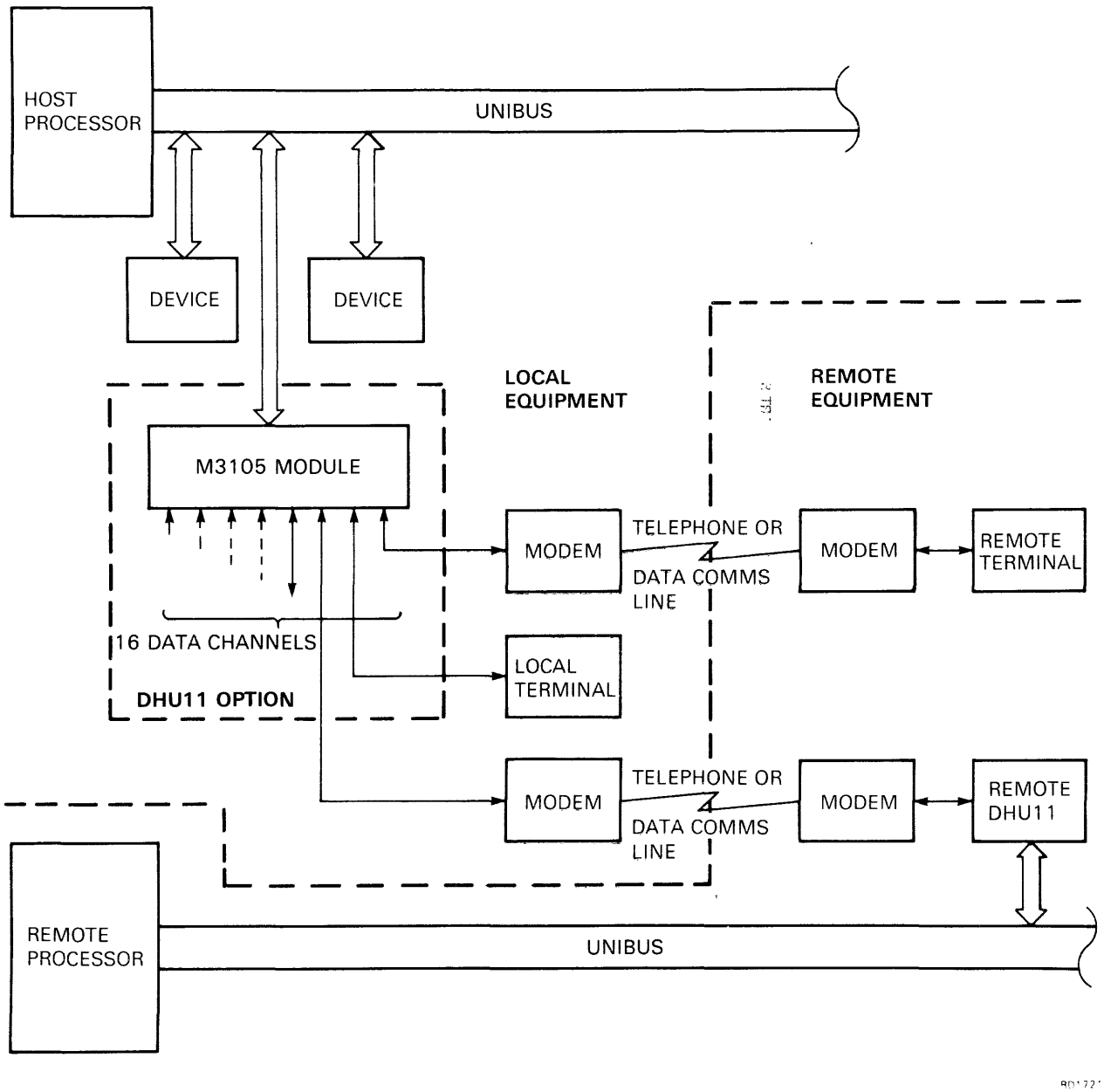


Figure 1-2 Example of DHU11 Configuration

1.2.5 Connections

Figure 1-3 shows an example of DHU11 connections. These include normal operating connections and test connections. More detail is shown in Figure 2-2 in Chapter 2, Installation.

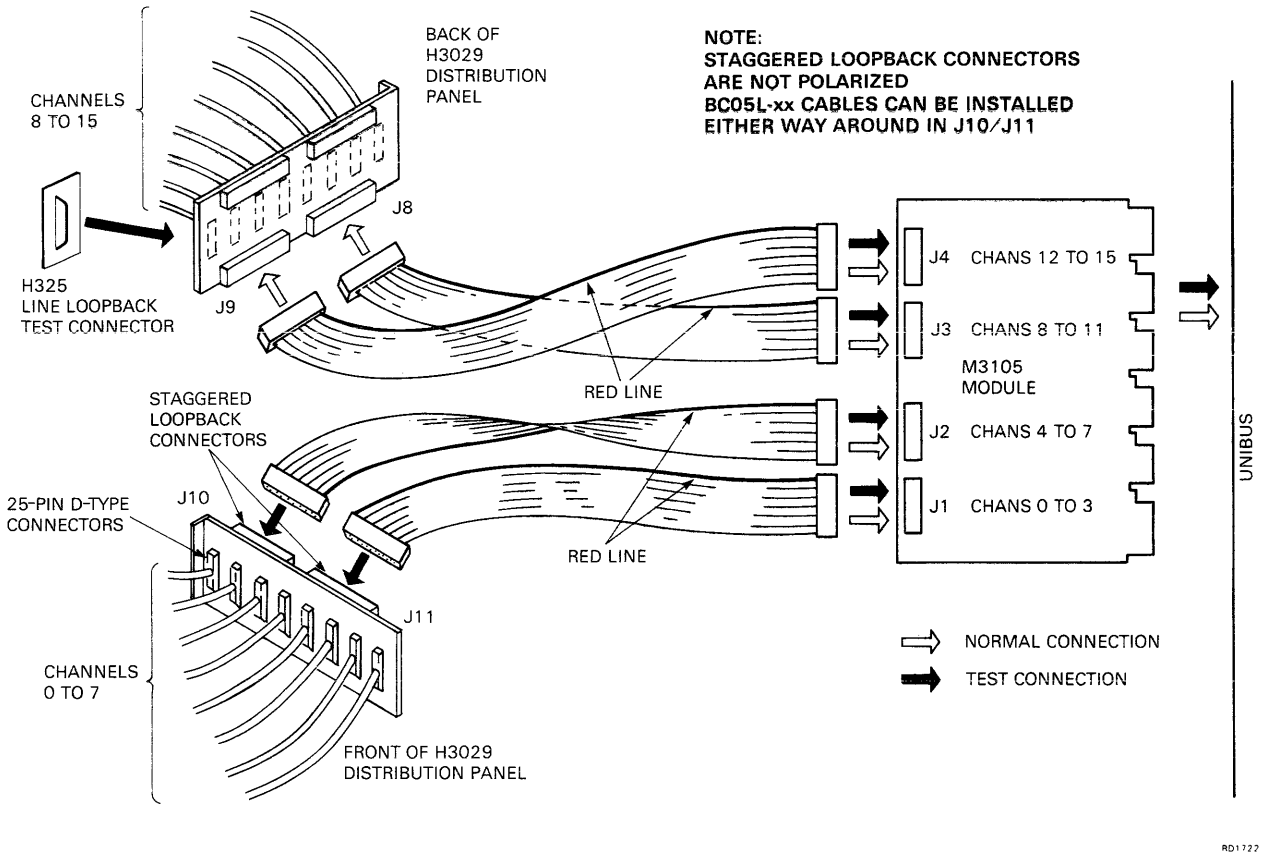


Figure 1-3 DHU11 Connections

1.3 SPECIFICATION

1.3.1 Environmental Conditions

- Storage temperature: –40°C to 66°C (–40°F to 151°F)
- Operating temperature: 5°C to 50°C (41°F to 122°F)
- Relative humidity: 10% to 95% non-condensing

1.3.2 Electrical Requirements

- +5 V dc + or – 5% at 6 A (typical)
- +15 V dc + or – 4% at 400 mA (typical)
- –15 V dc + or – 4% at 400 mA (typical)

Loads applied to the UNIBUS are as follows.

- UNIBUS ac loads – 2.2 ac loads
- UNIBUS dc loads – 1.0 dc load

1.3.3 Performance

1.3.3.1 Data Rates – Each channel can be programmed to operate at one of a number of speeds. If needed, the transmission and reception rates can be different (split speed). Table 1-1 shows the data rates which are possible.

The 16 serial channels are implemented with 8 DUARTs. Channels are paired as follows: 0/1, 2/3, 4/5, 6/7, 8/9, 10/11, 12/13, 14/15. Because of the method of data-rate generation within the DUARTs, all transmit and receive rates for a DUART channel-pair must be in the same group (A or B).

Table 1-1 DHU11 Data Rates

Speed (Bits/s)	Groups
50	A
75	B
110	A and B
134.5	A and B
150	B
300	A and B
600	A and B
1 200	A and B
1 800	B
2 000	B
2 400	A and B
4 800	A and B
7 200	A
9 600	A and B
19 200	B
38 400	A

Data-rate selection is covered in Chapter 3 (Programming).

1.3.3.2 Throughput – The approximate maximum throughput figures for DHU11 are quoted below.

- Transmit (per channel) – 1 000 chars/s
- Receive (per channel) – 4 000 chars/s *
- Total aggregate throughput – 15 000 chars/s

Several factors limit DHU11 throughput. Such factors may apply to transmission only, or to both transmission and reception.

a. The ratio between a channel's data-signaling rate and the number of bits in a character, (bits/s)/(bits/char), limits the maximum throughput in both the Transmit and Receive directions. The following example shows the relationships between two selected data rates and character formats. In each case, a start bit, a parity bit, and one stop bit are assumed.

* Seven-bit character with start bit, parity bit and one stop bit.

Data Rate (Bits/s)	5-Bit Characters (Chars/s)	7-Bit Characters (Chars/s)
38 400	4 800	3 840
4 800	600	480

b. The Transmit firmware can supply a maximum of 1 000 chars/s to any channel. Therefore, unless further limited by factor a or c, the maximum Transmit throughput per channel is 1 000 chars/s.

c. Communications firmware can handle a total of 15 000 chars/s. Unless limited by factor a, this is the maximum total throughput for the option.

NOTES

15 000 characters per second is the sum of both transmitted and received characters on all channels. This throughput could support continuous transmission *or* reception on all channels at 9 600 bits/s, or continuous transmission *and* reception on all channels at 4 800 bits/s.

9 600 bits/s is equivalent to 1 000 characters * per second. If a higher data rate is selected for a Transmit line, the duration of characters will be reduced but there will be gaps in transmission.

1.4 INTERFACES

1.4.1 System Bus Interface

The M3105 module can be connected directly to the system-unit (backplane). UNIBUS signals, together with pin details, are listed in Table 2-5 (in Chapter 2, Installation).

1.4.2 Serial Interfaces

1.4.2.1 Interface Standards – The DHU11 provides interface signals which conform to a subset of the EIA/CCITT standard RS-232-C/V.24. The electrical characteristics conform to EIA/CCITT standards RS-232-C/V.28 and RS-423-A (unbalanced interface). The interface is compatible with X.26/V.10 standards but does not comply with the slew-rate requirements.

Connections to the external equipment are via 25-pin male subminiature D-type connectors.

By means of suitable cables and connectors (not supplied or supported by DIGITAL) the channels can be made compatible with the following.

1. Subset of EIA interchange standard RS-449
2. EIA electrical standard RS-422 (balanced)

Table 1-2 shows RS-232-C/V.24/RS-449 signal relationships, and pin connections for the 25-pin male subminiature D-type connectors.

* Seven-bit character with start bit, parity bit and one stop bit.

Table 1-2 EIA/CCITT Signal Relationships

Signal Name		D-Type Pin	RS-232-C	Circuit CCITT V.24	Circuit RS-449
Protective Ground	(GND)	1	AA	–	–
Signal Ground	(SIG GND)	7	AB	102	SG
Transmit Data	(TXD)	2	BA	103	SD
Receive Data	(RXD)	3	BB	104	RD
Request to Send	(RTS)	4	CA	105	RS
Clear to Send	(CTS)	5	CB	106	CS
Data Set Ready	(DSR)	6	CC	107	DM
Data Terminal Ready	(DTR)	20	CD	108/2	TR
Ring Indicator	(RI)	22	CE	125	IC
Data Carrier Detect	(DCD)	8	CF	109	RR

NOTE

The backward channels listed below are not supported. However, by using another channel for this function, and by connecting a suitable cable (H1200 or H1201, for example), backward-channel operation is possible.

Circuit No.	Function
118	Transmitted backward-channel data
120	Transmit backward-channel line signal
119	Received backward-channel data
121	Backward channel ready
122	Backward-channel-received line-signal detector

1.4.2.2 Serial Data Format – Serial characters are made up of an encoded sequence of bits which are enclosed between a start and a stop signal. The start signal is always 1 bit long but the stop signal is programmable to 1, 1.5, or 2 bits. The duration of a bit is dependent on the selected data rate.

Character codes may be 5, 6, 7, or 8 bits long, optionally followed by a parity bit. Parity can be programmed as even, odd, or no parity.

On serial data channels controlled via the DHU11, the data line is held marking when inactive. Transfer of each character begins with a start bit (space) and ends with one or more stop bits (mark).

Figure 1-4 shows the reception of an 8-bit character with parity. The Least-Significant Bit (LSB) of the character code is transmitted first. If another character is not ready for transmission, the line will stay marking. The figure shows 1, 1.5, and 2 stop bits.

NOTE

This description applies to signals at the DUART pins. Signals measured on the interchange circuits will have the opposite polarity to those shown.

The data-rate clock, which samples the serial data, is 16 times the programmed data rate. Arrows show when the bits are tested for polarity.

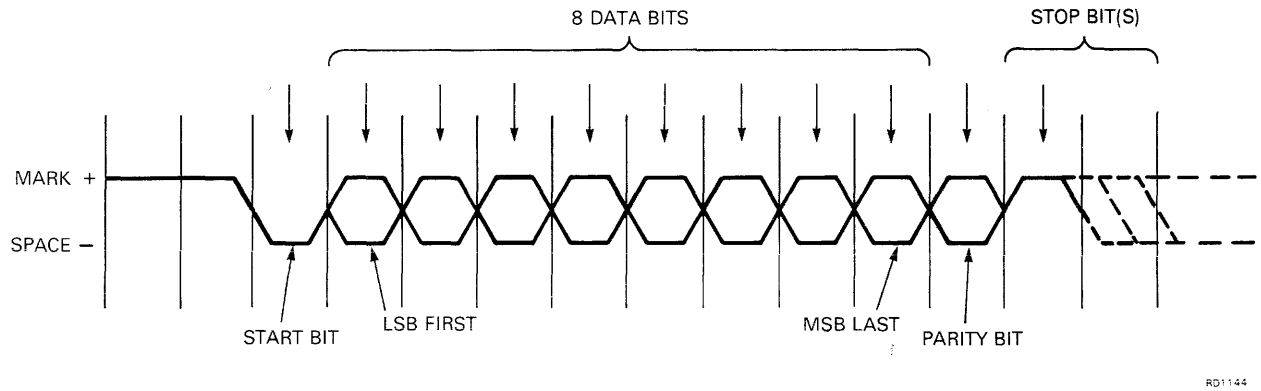


Figure 1-4 Serial Character Format

The DHU11 allows the following serial character formats.

- Characters of 5, 6, 7, or 8 bits with or without parity and with 1 stop bit
- Characters of 5 bits with or without parity and with 1.5 stop bits
- Characters of 6, 7, or 8 bits with or without parity and with 2 stop bits

1.4.2.3 Line Receivers – The serial line receivers used in this module are 9637AC or equivalent. They convert the EIA input signals to TTL levels suitable for the DUARTs.

Signals are inverted by the receivers.

1.4.2.4 Line Transmitters – The serial line transmitters used in this module are 9636AC or equivalent. They convert TTL level signals from the DUARTs to EIA levels on the data lines.

Signals are inverted by the transmitters.

1.4.2.5 Speed/Distance Considerations – The maximum data rate which can be used on a line depends upon a number of factors. These are:

1. The characteristics of the line transmitters and receivers
2. The characteristics of the serial cable
3. The length of the cable
4. Noise (interference) which affects the line.

A 'speed against distance' table for typical conditions is provided in Section 2.6.6.

1.5 FUNCTIONAL DESCRIPTION

1.5.1 Control Function

In the DHU11 module (Figure 1-5), data is transferred to and from the serial interface by three methods:

1. By DMA. Blocks of data are transferred from system memory to the serial interface. DMA data is routed via the UNIBUS data transceivers, the TX FIFO (for the addressed channel), and PROC2.

2. In the programmed transfer mode, characters are transferred from the host to the serial interface. The route for characters is via the UNIBUS data transceivers, the TX FIFO (for the addressed channel), and PROC2.

3. Received characters are transferred from the serial interface to the host via PROC2, the RX FIFO, and the UNIBUS data transceivers.

At the center of the control section is a 1K-word RAM. By writing control words or bytes to registers in the RAM, the host can configure and command the module. The host can also write data for transmission on the serial lines, to TX FIFOs (one per channel) in the RAM. TX FIFO addresses are provided by TX FIFO control.

Two microcomputers (PROC 1 and PROC 2), which have associated microprogram ROMs, scan the RAM and the FIFO logic in order to detect a new configuration, or data to be transferred. They also write status information to the RAM, which can then be read by the host.

PROC 2 configures the DUARTs, and transfers Transmit and Receive data between the FIFOs and the DUARTs. Received characters are written to the RX FIFO and transmit characters are read from the TX FIFO.

Among other functions, PROC 1 controls DMA transfers to the TX FIFO. PROC 1 keeps track of DMA addresses and character count, and reports to the host when the block has been transferred.

Both microcomputers execute background diagnostics when not busy with other tasks.

1.5.2 UNIBUS Interface

The DHU11 module is programmed by the host via a number of I/O registers. When the DHU11 recognizes a valid address, it allows the host to access the FIFOs and the registers. When TX or RX FIFOs are being accessed, FIFO controllers provide the RAM addresses.

Module address switches are connected to a comparator which monitors the address transceivers. When an I/O address from the host matches the address on the switches, the DHU11 responds to the host.

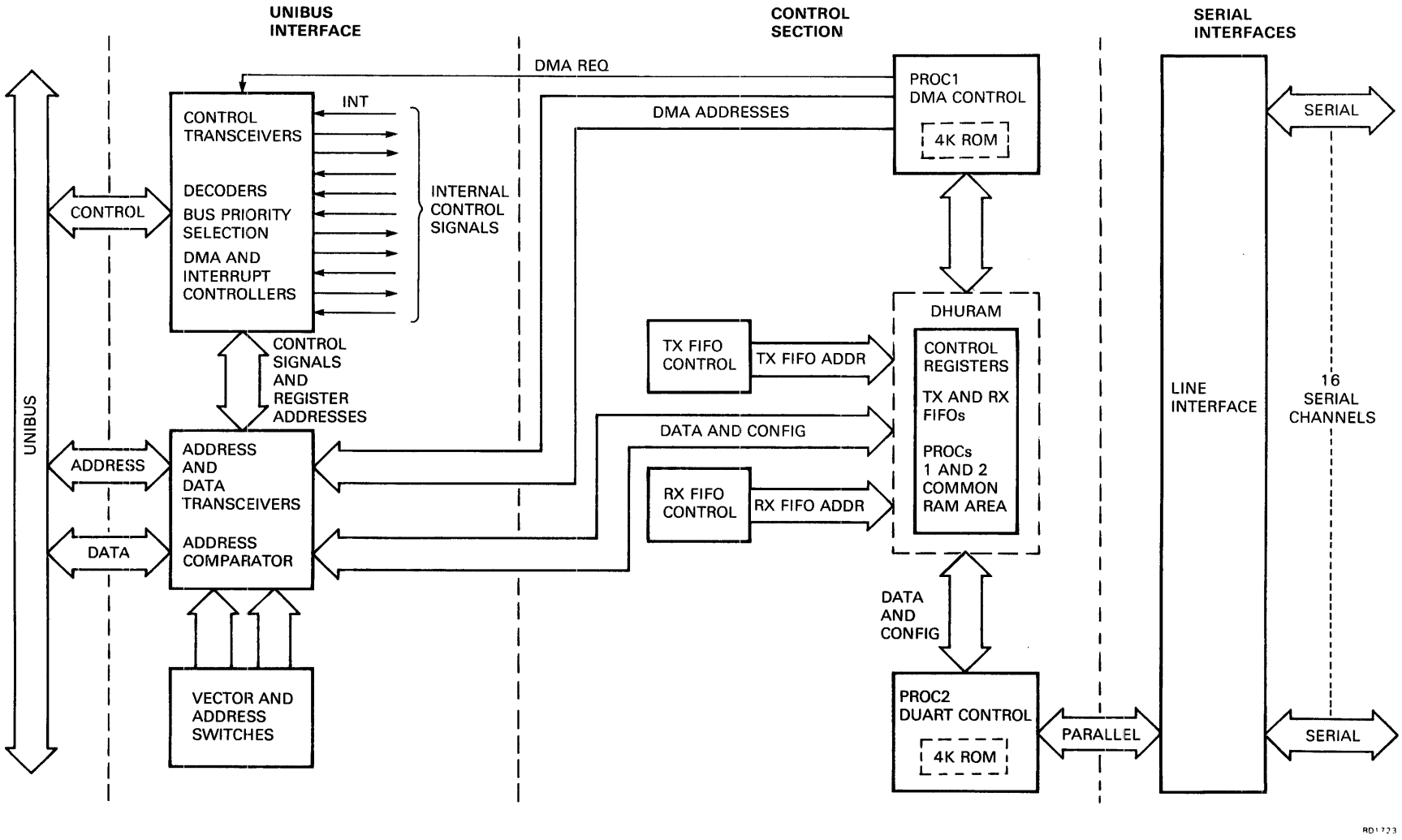


Figure 1-5 DHU11 Functional Block

Vector address switches are indirectly connected to the data transceivers. These allow the DHU11 to supply one of two interrupt vectors (transmit or receive) to the host during an interrupt acknowledge sequence.

UNIBUS control signals and register addresses are decoded to generate internal control signals. DMA and interrupt transactions are initiated by control signals from the DHU11.

1.5.3 Serial Interfaces

Sixteen full-duplex serial interfaces are provided by eight DUARTs. These ICs are configured by PROC2 as instructed by the host. They carry out the serial/parallel and parallel/serial conversion.

The status of modem control lines for each channel is polled by PROC 2. If programmed to do so, the DHU11 will report changes of modem status to the host. Such reports are made via the RX FIFO and the device registers.

CHAPTER 2
INSTALLATION

2.1 SCOPE

This chapter contains information on how to prepare and install the DHU11 option. It contains sections on the following.

- The selection of vectors and device addresses
- The selection of interrupt-priority levels
- Rules for backplane positioning
- Recommended cables
- Test connectors
- The assignment of vectors and floating addresses
- Testing after installation

2.2 DHU11-M

The DHU11-M may be installed in one of four cabinet kits.

The DHU11-M consists of:

Part Number	Description	Quantity
M3105	DHU11 module	1
EK-DHU11-UG	User Guide	1

Table 2-1 lists the parts for each cabinet kit.

Check that you have received all the items on the packing list. Examine all parts for physical damage. Report damaged or missing items to the shipper and the DIGITAL representative.

CAUTION

The M3105 module is supplied in a protective sleeve. Do not remove the sleeve until you are about to install the module. Protect the module from static during installation.

Table 2-1 Cabinet Kits for the DHU11

Cabinet Kit Number	Description				
CK-DHU11-AE	VAX-11/730 and VAX-11/750 kernel systems				
CK-DHU11-A1	Unshielded cabinet				
CK-DHU11-AD	General-purpose expansion cabinet				
CK-DHU11-AF	VAX-11/725 system				
Contains:					
H325	Single-line loopback connector	1	1	1	1
H3029	8-line 25-way distribution panel	2	2	2	2
BC05L-03	40-way ribbon cable	4			
BC05L-07	40-way ribbon cable				4
BC05L-10	40-way ribbon cable		4	4	
H9544-SJ	19-inch frame and fastenings			1	

NOTE

BC05L-xx cables are 3 ft, 7 ft, and 10 ft as indicated by xx.

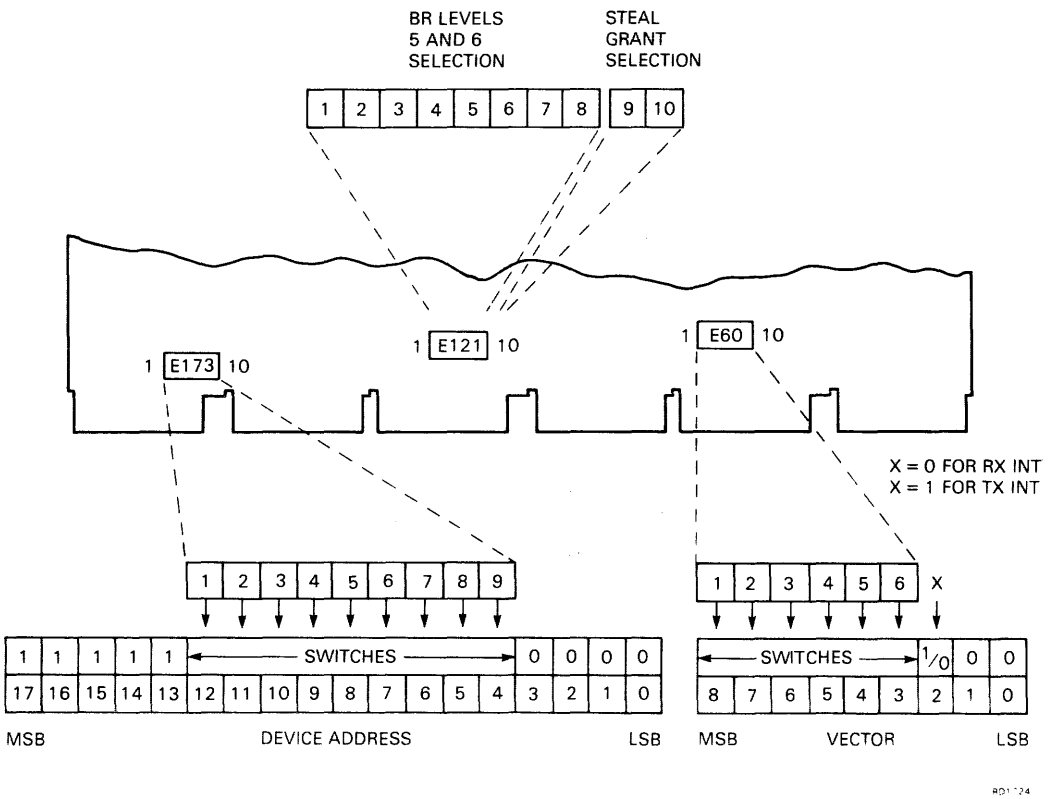


Figure 2-1 Switch Locations

2.3 MODULE CONFIGURATION

Figure 2-1 shows the location and function of switchpacks which configure device addresses, vectors, and interrupt priority. **See the previous CAUTION (in Section 2.2) before configuring the module.**

2.3.1 Address Switches

The device address for the DHU11 is set on switchpack E173. Table 2-2 explains the relationship between device addresses and switch positions.

Table 2-2 Device Address Selection Guide

MSB LSB

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	1	←			SWITCHES					→	0	0	0	0

E173 SWITCH NUMBER	1	2	3	4	5	6	7	8	9	DEVICE ADDRESS
									OFF	760020
								OFF		760040
								OFF	OFF	760060
NOTE:							OFF			760100
SWITCH E173-10						OFF				760200
MUST BE OFF						OFF	OFF			760300
					OFF					760400
					OFF		OFF			760500
					OFF	OFF				760600
					OFF	OFF	OFF			760700
				OFF						761000
			OFF							762000
			OFF	OFF						763000
		OFF								764000
	OFF									770000

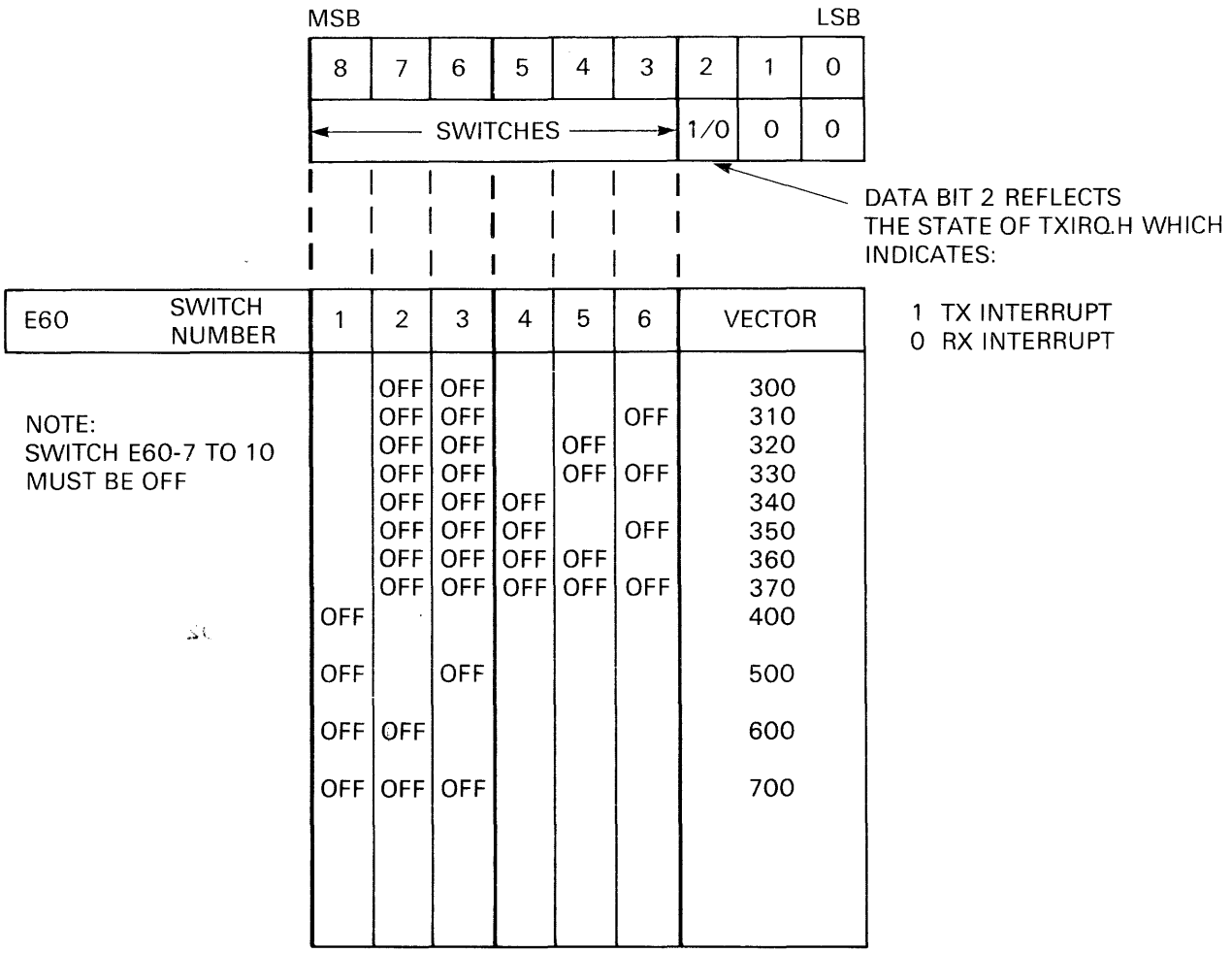
OFF = SWITCH OPEN TO RESPOND TO A LOGICAL 1

RD1744

2.3.2 Vector Switches

During an interrupt-acknowledge sequence, the DHU11 returns a 9-bit interrupt vector to the host. The six high-order bits of this vector are derived from E60-S1 to S6. Table 2-3 explains how switch positions relate to the vector.

Table 2-3 Vector Selection Guide



E60 SWITCH NUMBER	1	2	3	4	5	6	VECTOR
		OFF	OFF				300
		OFF	OFF			OFF	310
		OFF	OFF		OFF		320
		OFF	OFF		OFF	OFF	330
		OFF	OFF	OFF			340
		OFF	OFF	OFF		OFF	350
		OFF	OFF	OFF	OFF		360
		OFF	OFF	OFF	OFF	OFF	370
	OFF						400
	OFF		OFF				500
	OFF	OFF					600
	OFF	OFF	OFF				700

RD1745

2.3.3 Bus Request (BR) Interrupt-Priority Switches

The M3105 module can be switch-selected to interrupt at BR levels 5 or 6. Table 2-4 indicates how BR levels are selected.

Table 2-4 Interrupt-Priority Switches

BR Level	State of Switchpack E121-S1 to S8							
	S1	S2	S3	S4	S5	S6	S7	S8
5	OFF	OFF	OFF	OFF	ON	ON	ON	ON
6	ON	ON	ON	ON	OFF	OFF	OFF	OFF

2.3.4 Steal Grant

This facility is used to improve UNIBUS latency by 'stealing' a bus grant (BG) intended for a device further along the priority chain. If a BG is received while BNPR is asserted, passive release of the UNIBUS will occur. Thus the device which raised the NPR will not be delayed.

Steal grant is enabled/disabled by E121-S9 and S10 as follows.

S9 OFF, S10 ON = steal grant disabled (default)
S10 OFF, S9 ON = steal grant enabled

2.3.5 Backplane

2.3.5.1 Connection to the UNIBUS – The DHU11 interfaces with the system via the UNIBUS. The physical connection is made via the A, B, C, D, E, and F edge connectors on the module.

Backplane signals and pin designations are listed in Table 2-5.

Table 2-5 Backplane Connections

Signal	Pin	Signal	Pin
BUSA00.L	EH2	BPB.L	CS1
BUSA01.L	EH1		
BUSA02.L	EF1	BUSD00.L	CS2
BUSA03.L	EV2	BUSD01.L	CR2
BUSA04.L	EU2	BUSD02.L	CU2
BUSA05.L	EV1	BUSD03.L	CT2
BUSA06.L	EU1	BUSD04.L	CN2
BUSA07.L	EP2	BUSD05.L	CP2
BUSA08.L	EN2	BUSD06.L	CV2
BUSA09.L	ER1	BUSD07.L	CM2
BUSA10.L	EP1	BUSD08.L	CL2
BUSA11.L	EL1	BUSD09.L	CK2
BUSA12.L	EC1	BUSD10.L	CJ2
BUSA13.L	EK2	BUSD11.L	CH1
BUSA14.L	EK1	BUSD12.L	CH2
BUSA15.L	ED2	BUSD13.L	CF2
BUSA16.L	EE2	BUSD14.L	CE2
BUSA17.L	ED1	BUSD15.L	CD2
BBSY.L	FD1	GROUND	BT1
BDCLO.L	CN1	GROUND	CT1
BG4IN.H	DS2	GROUND	DT1
BG5IN.H	DP2	GROUND	ET1
BG6IN.H	DM2	GROUND	FT1
BG7IN.H	DK2	GROUND	AC2
BG4OUT.H	DT2	GROUND	BC2
BG5OUT.H	DR2	GROUND	CC2
BG6OUT.H	DN2	GROUND	DC2
BG7OUT.H	DL2	GROUND	EC2

Table 2-5 Backplane Connections (Cont)

Signal	Pin	Signal	Pin
BR4.L	DH2	GROUND	FC2
BR5.L	DF2	GROUND	AT1
BR6.L	DE2	NPGIN.H	CA1
BR7.L	DD2	NPGOUT.H	CB1
BUSC0.L	EJ2	+5 V	AA2
BUSC1.L	EF2	+5 V	BA2
BINIT.L	DL1	+5 V	CA2
BINTR.L	FM1	+5 V	DA2
BMSYN.L	EE1	+5 V	EA2
BNPR.L	FJ1	+5 V	FA2
BSACK.L	FT2	+15 V	CU1
BSSYN.L	EJ1	-15 V	FB2

2.3.5.2 Bus Grant Continuity Cards – Typical system-units into which the M3105 module is installed are DD11-C (four slots) and DD11-D (nine slots). For occupied slots, bus-grant continuity is provided by the installed module. However, unused slots between the first slot and the terminator must have a bus-grant card installed to extend the grant.

2.3.5.3 NPG Continuity – On unused SPC slots, NPG continuity is provided by a wire link between backplane pins CA1 and CB1.

NOTE

When installing the M3105 module in a slot, you must remove this link from the slot. If you later remove the module, replace the link. See also Section 2.3.5.2.

2.4 PRIORITY SELECTION

The DHU11 uses BR5 or BR6 to request interrupt service.

Non-processor request (NPR) priorities are determined by an option's position on the bus. The bus position may be a compromise between NPR and interrupt-priority requirements. As a general rule, NPR priorities should be considered first, and then interrupt requests.

2.4.1 Non-Processor Request

On systems with more than one DMA device there is a chance of bus-latency problems. To minimize this, a device which will lose data if its NPRs are not serviced quickly should be placed nearer to the CPU than a device which can wait longer.

DMA latency is unlikely to affect the DHU11. The worst effect would be to reduce device throughput. Transmit data will not be lost.

If there is only one DMA device on the system, there is no DMA contention.

2.4.2 Bus Request

The DHU11 is normally assigned BR level 5. Requests are made on bus-request line BR5. An arbitrator (usually in the host CPU) monitors the request lines. If the host CPU is not engaged in a higher-priority task it grants the use of the bus to the device with the highest priority.

BR contention only occurs between devices with the same BR level. Within any priority group, priority is decided by bus position. Devices with time-critical interrupts should be nearer the CPU, unless this conflicts with NPR priority.

The final configuration can be tested by the appropriate system-exerciser diagnostic. Some changes may be needed for optimum performance.

2.5 MODULE INSTALLATION

Once you have defined the backplane position of the DHU11, you can install the module and check the backplane with a testmeter.

NOTE

This checkout should be used by trained maintenance personnel only.

CAUTION

Switch off power before inserting or removing modules. Be careful not to snag module components on the card guides or adjacent modules.

The M3105 is a fine-line-etch PCB. Handle it carefully to avoid damaging the etch.

Take anti-static measures to protect the module.

1. Remove the backplane NPG link between CA1 and CB1.

2. Using Figures 2-2 and 1-3 as a guide, install the option.

   Figure 2-2 shows how to install distribution panels in the H9544-SJ frame. This frame forms part of the 19-in rack-mounting kit, CK-DHU11-A1, which is listed in Section 2.2.

3. Make sure that +5 V is present between AA2 and ground.

4. Make sure that +15 V is present between CU1 and ground.

5. Make sure that –15 V is present between FB2 and ground.

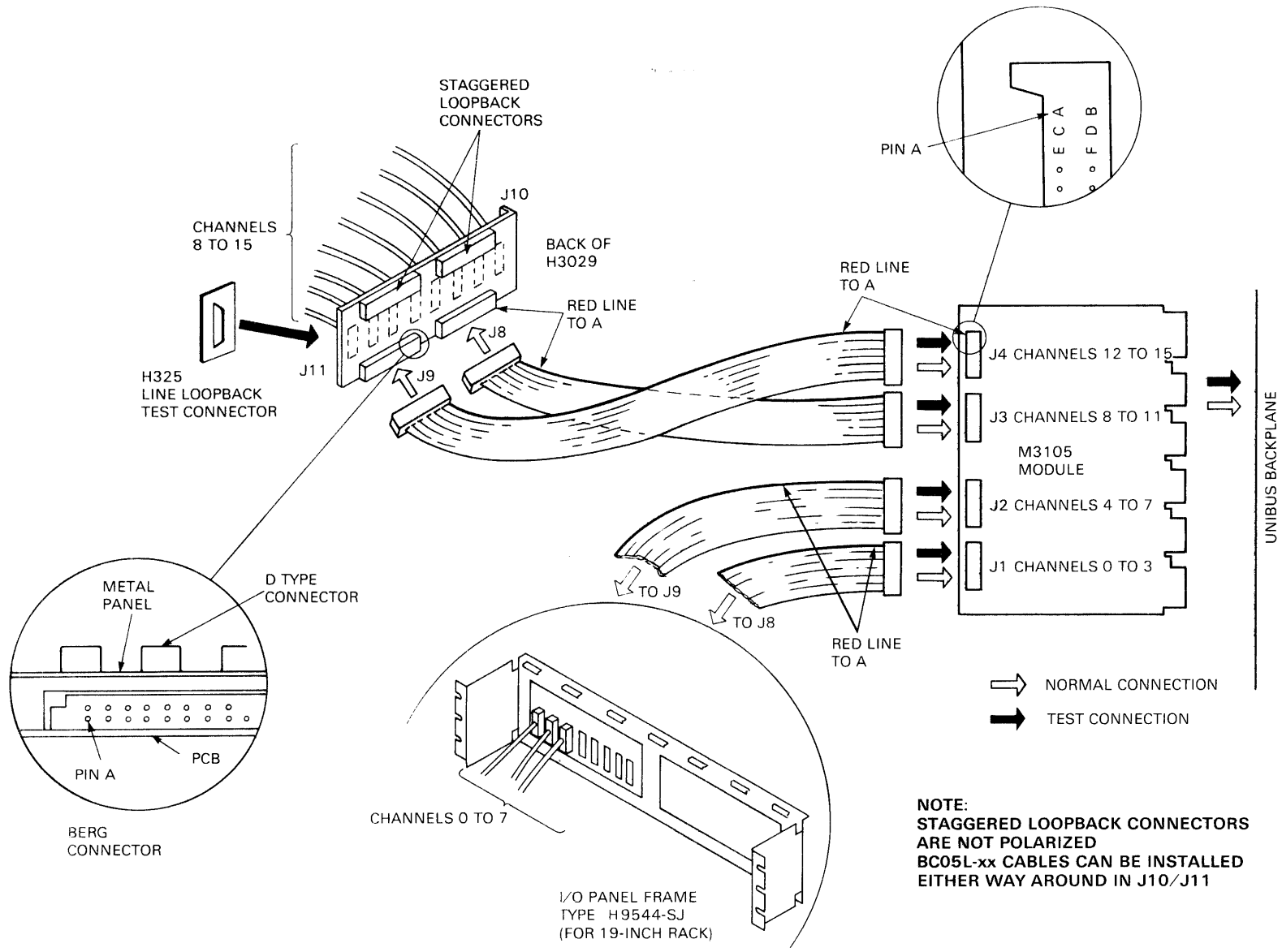


Figure 2-2 DHU11 Installation

2.6 CABLES AND CONNECTORS

2.6.1 Distribution Panel

Each H3029 distribution panel adapts two of the DHU11's Berg * connectors to eight subminiature D-type RS-232-C connectors. Noise filtering is provided on each pin of the RS-232-C connectors. This reduces electromagnetic radiation from the cables, and provides the logic with some protection against static discharge. Noise-filtering increases line capacitance by 850 pF.

Figure 2-3 shows the layout, and Figure 2-4 shows the circuit. There is no CCITT equivalent of EIA circuit AA (protective ground). To implement this circuit, a ground strap must be installed between the H3029 and the system cabinet. The 0-ohm link W1 (not installed at the factory) can then be installed to connect this circuit, and removed to disconnect it, as needed.

NOTE

Staggered-loopback connectors are incorporated in the H3029 distribution panels. The circuit, which is shown separately in Figure 2-5, is the same as the H3277 staggered-loopback connector.

Table 2-6 gives the pin/signal relationships for two distribution panels. Information in parentheses applies to channels 8 to 16.

The following is an example of the use of Table 2-6.

- Signal TXD0 is the Transmit Data line for channel 0. Its CCITT circuit number is 103. It is connected to J8 pin B on the H3029 for channels 0 to 7.

- Signal TXD8 is the Transmit Data line for channel 8. Its CCITT circuit number is 103. It is connected to J8 pin B on the H3029 for channels 8 to 15.

* Berg is a registered trademark of the Berg Corporation.

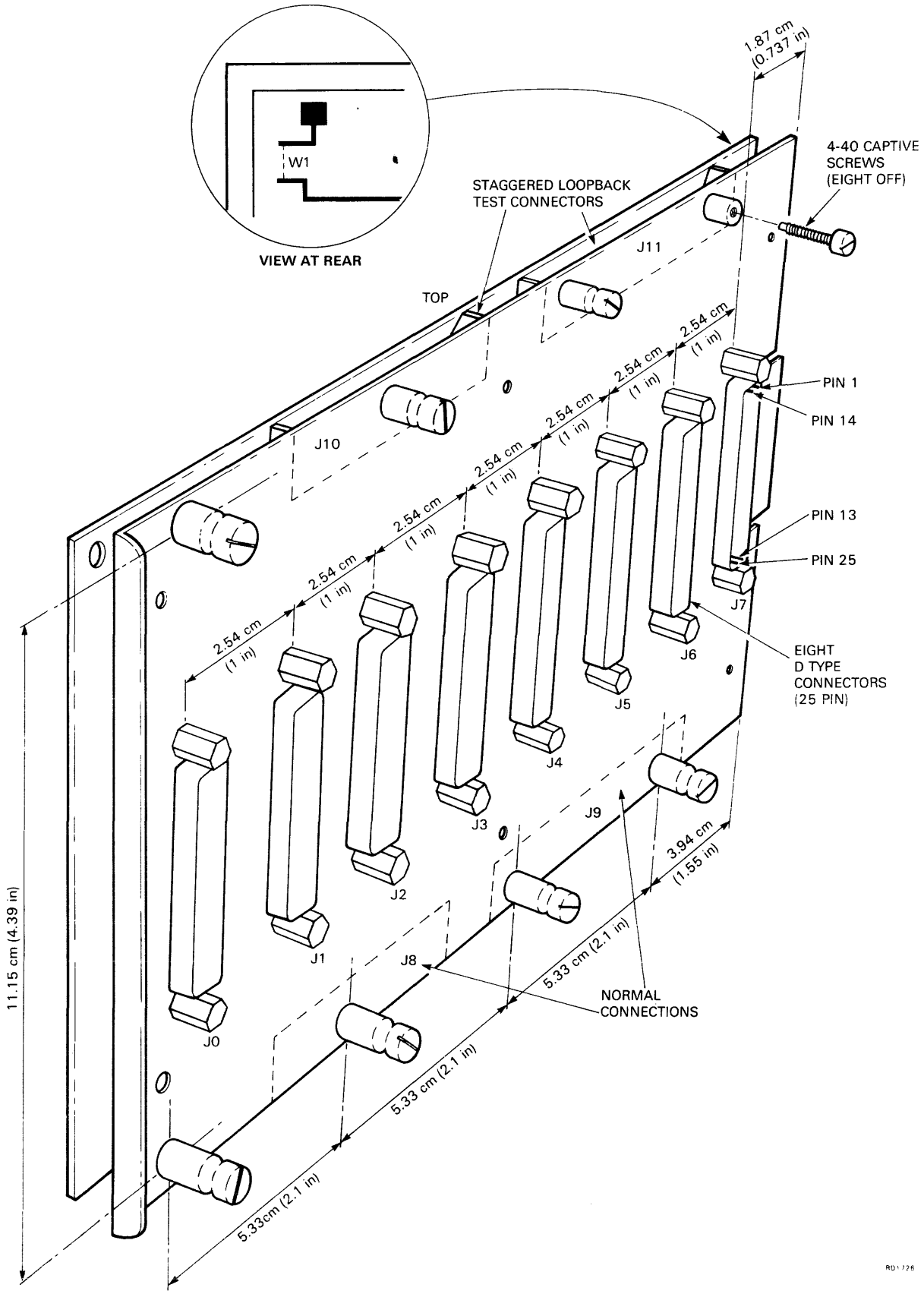


Figure 2-3 H3029 Layout

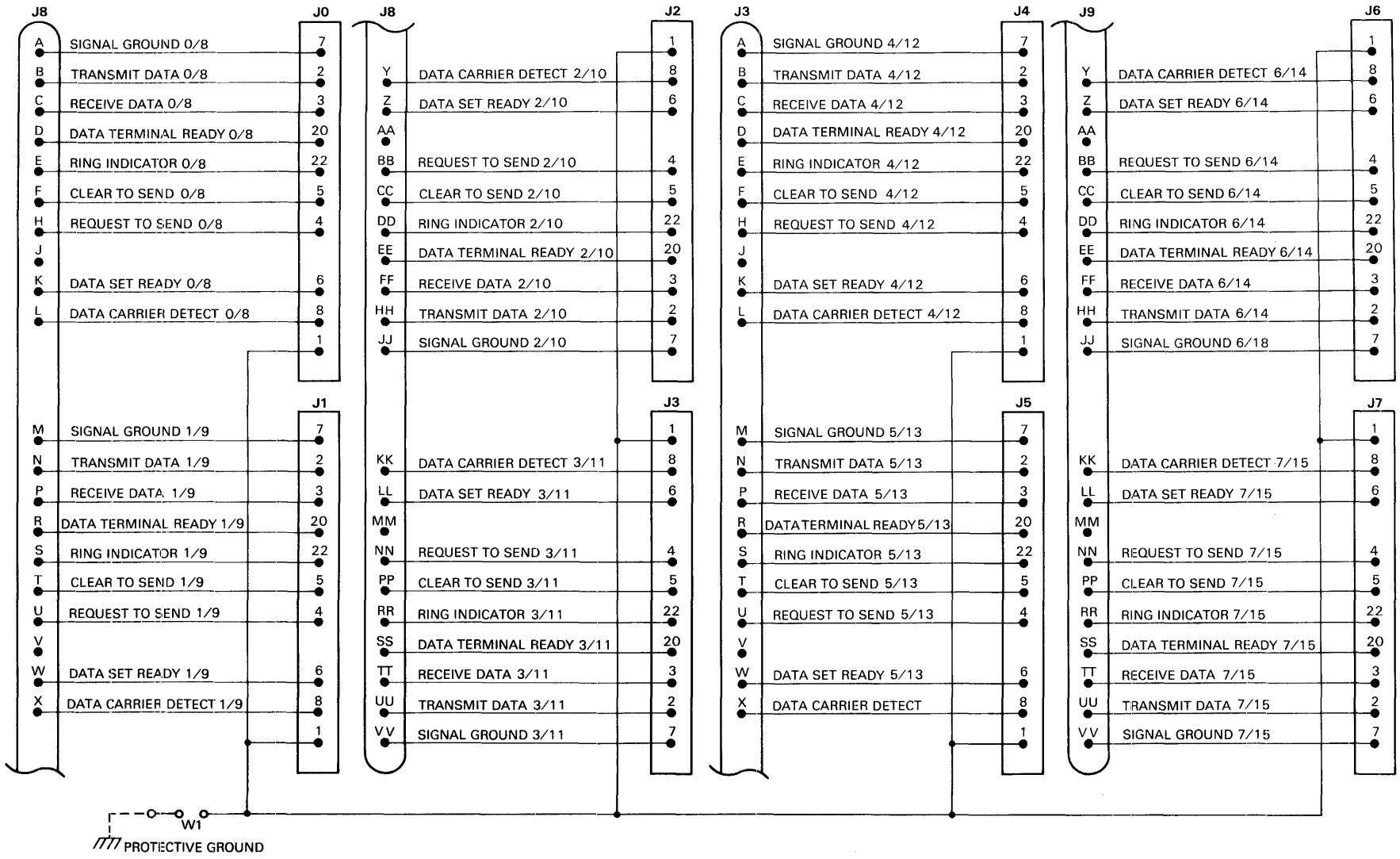


Figure 2-4 H3029 Circuit Diagram

Table 2-6 H3029 Connections

Signal	Circuit Number	J8 Pin Number	Name
SIG GND 0(8)	102	A	
TXD0(8)	103	B	Transmit Data
RXD0(8)	104	C	Receive Data
DTR0(8)	108/2	D	Data Terminal Ready
RI0(8)	125	E	Ring Indicator
CTS0(8)	106	F	Clear to Send
RTS0(8)	105	H	Request to Send
DSR0(8)	107	K	Data Set Ready
DCD0(8)	109	L	Data Carrier Detect
SIG GND 1(9)	102	M	
TXD1(9)	103	N	
RXD1(9)	104	P	
DTR1(9)	108/2	R	
RI1(9)	125	S	
CTS1(9)	106	T	
RTS1(9)	105	U	
DSR1(9)	107	W	
DCD1(9)	109	X	
DCD2(10)	109	Y	
DSR2(10)	107	Z	
RTS2(10)	105	BB	
CTS2(10)	106	CC	
RI2(10)	125	DD	
DTR2(10)	108/2	EE	
RXD2(10)	104	FF	
TXD2(10)	103	HH	
SIG GND 2(10)	102	JJ	
DCD3(11)	109	KK	
DSR3(11)	107	LL	
RTS3(11)	105	NN	
CTS3(11)	106	PP	
RI3(11)	125	RR	
DTR3(11)	108/2	SS	
RXD3(11)	104	TT	
TXD3(11)	103	UU	
SIG GND 3(11)	102	VV	

Table 2-6 H3029 Connections (Cont)

Signal	Circuit Number	J8 Pin Number	Name
SIG GND 4(12)	102	A	
TXD4(12)	103	B	Transmit Data
RXD4(12)	104	C	Receive Data
DTR4(12)	108/2	D	Data Terminal Ready
RI4(12)	125	E	Ring Indicator
CTS4(12)	106	F	Clear to Send
RTS4(12)	105	H	Request to Send
DSR4(12)	107	K	Data Set Ready
DCD4(12)	109	L	Data Carrier Detect
SIG GND 5(13)	102	M	
TXD5(13)	103	N	
RXD5(13)	104	P	
DTR5(13)	108/2	R	
RI5(13)	125	S	
CTS5(13)	106	T	
RTS5(13)	105	U	
DSR5(13)	107	W	
DCD5(13)	109	X	
DCD6(14)	109	Y	
DSR6(14)	107	Z	
RTS6(14)	105	BB	
CTS6(14)	106	CC	
RI6(14)	125	DD	
DTR6(14)	108/2	EE	
RXD6(14)	104	FF	
TXD6(14)	103	HH	
SIG GND 6(14)	102	JJ	
DCD7(15)	109	KK	
DSR7(15)	107	LL	
RTS7(15)	105	NN	
CTS7(15)	106	PP	
RI7(15)	125	RR	
DTR7(15)	108/2	SS	
RXD7(15)	104	TT	
TXD7(15)	103	UU	
SIG GND 7(15)	102	VV	

2.6.2 Staggered-Loopback Test Connector

See Figure 2-5. Two staggered-loopback test connectors are built into the H3029 distribution panel for use during diagnostic tests. Systems which do not use the H3029 will be supplied with a separate loopback connector (H3277) which implements the loopback circuits of the H3029. Using these connectors, all channels can be tested. A channel fault can be traced to one of two channels.

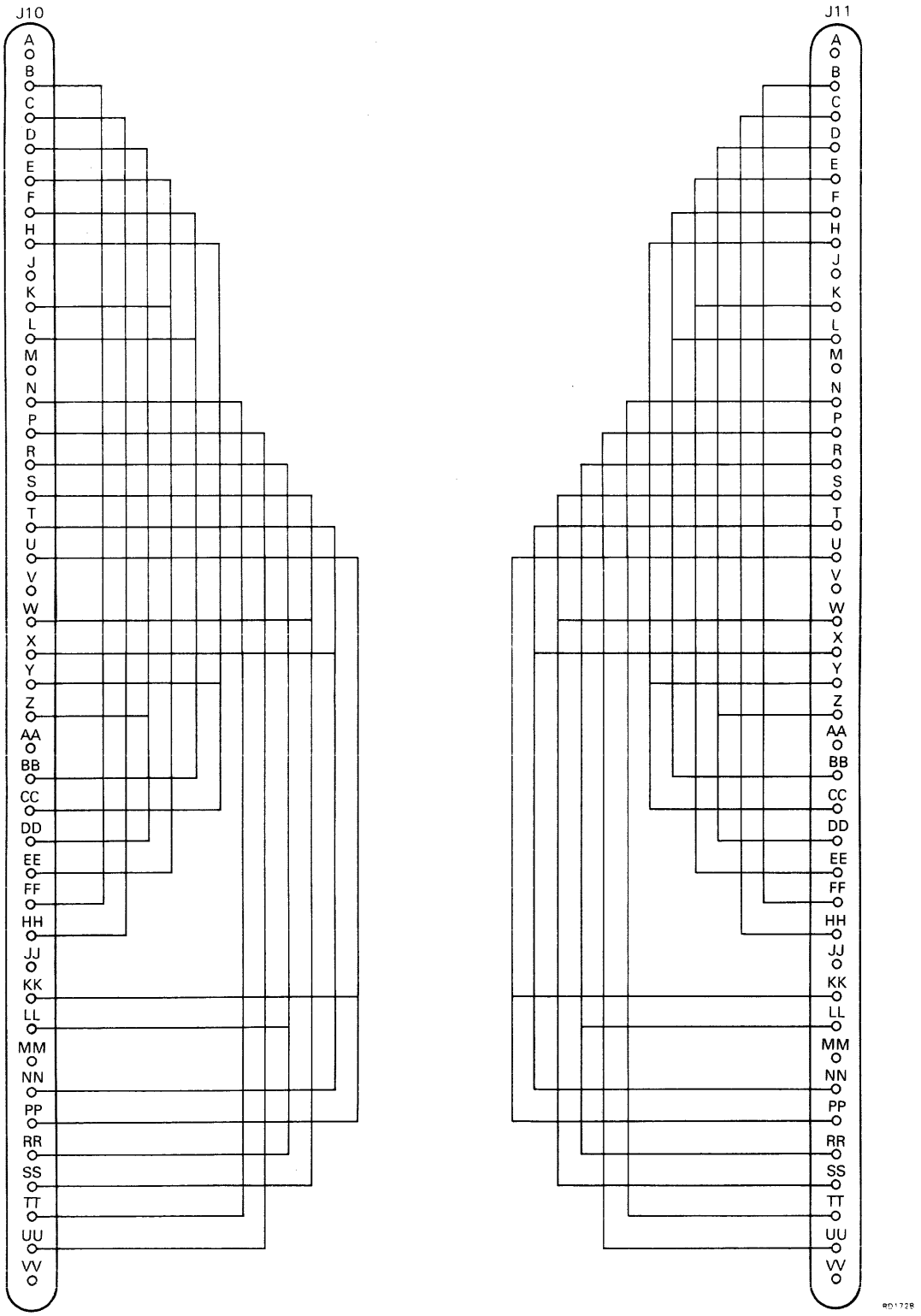


Figure 2-5 Staggered-Loopback Circuit of H3029

2.6.3 Line-Loopback Test Connector H325

This connector is shown in Figure 2-6. It can be used during diagnostic tests to trace a fault to a single channel.

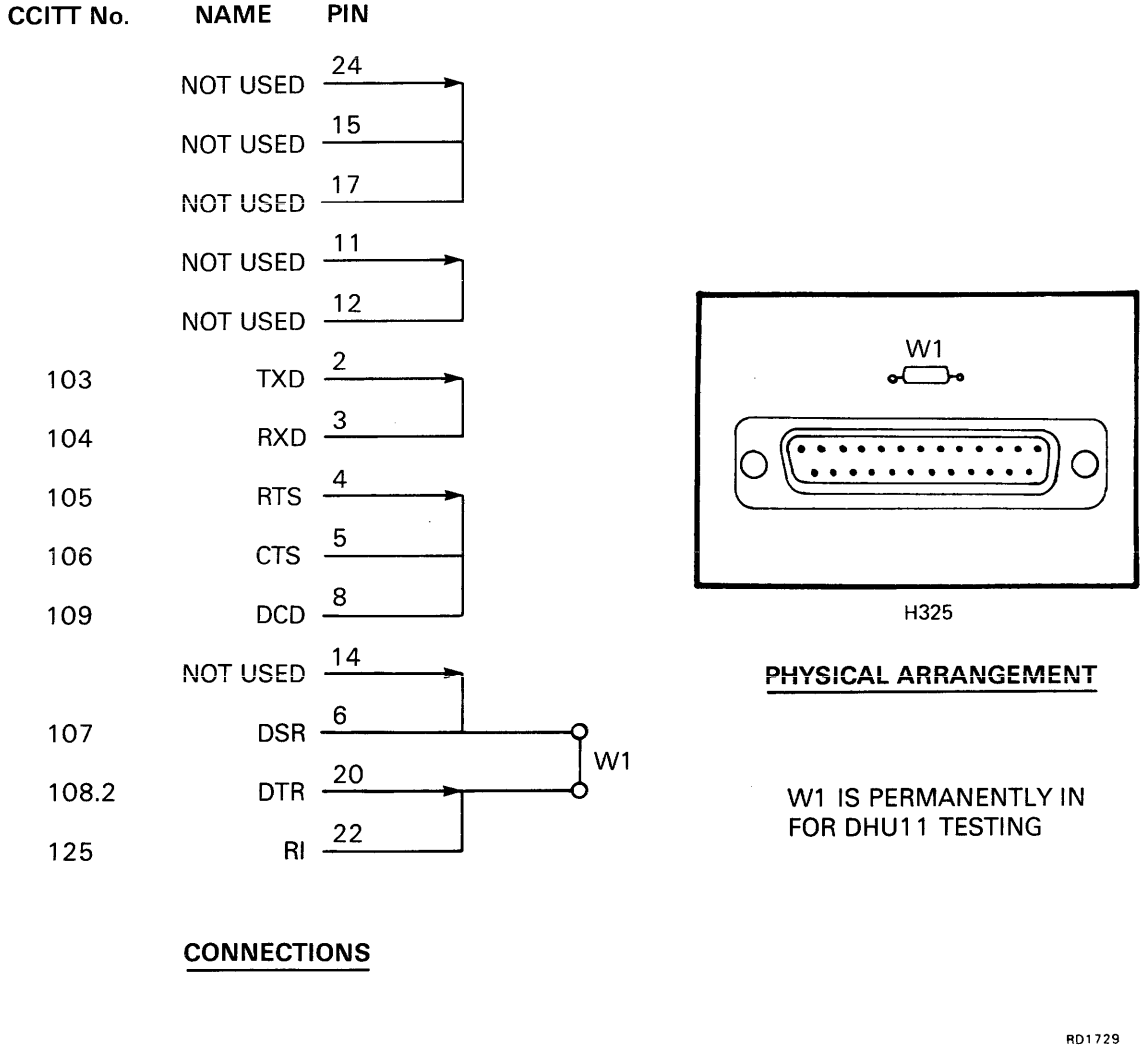


Figure 2-6 Line-Loopback Test Connector

2.6.4 Null Modem Cables

Null modem cables are used for local RS-232-C connection. Because of Federal Communications Commission (FCC) regulations, the cable specifications for the United States and Canada are different from those for non-FCC countries. Other countries may also have similar electromagnetic interference (EMI) control regulations. EMC/RFI shielded cabinets (see Appendix A, Glossary) are now available for systems which conform to FCC requirements.

Recommended null modem cables are as follows.

1. BC22D (for EMC/RFI shielded cabinets)

   - Round 6-conductor fully shielded cable to FCC specification
   - Subminiature 25-pin D-type female connector moulded on each end
   - Lengths available.

     BC22D-10 – 3.1 m (10 ft)
     BC22D-25 – 7.62 m (25 ft)
     BC22D-35 – 10.72 m (35 ft)
     BC22D-50 – 15.24 m (50 ft)
     BC22D-75 – 22.9 m (75 ft)
     BC22D-A0 – 30.48 m (100 ft)
     BC22D-B5 – 76.2 m (250 ft).

2. BC03M

   - Round 6-conductor (three twisted pairs), each pair shielded
   - Cables over 30.48 m (100 ft) have a 25-pin subminiature D-type female connector at one end. The other end is unterminated, for passing through a conduit.
   - Cables 30.48 m (100 ft) and less have a 25-pin subminiature D-type female connector at each end.
   - Lengths available.

     BC03M-25 – 7.62 m (25 ft)
     BC03M-A0 – 30.48 m (100 ft)
     BC03M-B5 – 76.2 m (250 ft)
     BC03M-E0 – 152.4 m (500 ft)
     BC03M-L0 – 304.8 m (1000 ft).

3. BC22A

   - Round 6-conductor cable
   - Subminiature 25-pin D-type female connector moulded at each end
   - Lengths available.

     BC22A-10 – 3.1 m (10 ft)
     BC22A-25 – 7.62 m (25 ft).

Cables of groups 1, 2, and 3 are all connected as in Figure 2-7. The cables are not polarized. They can be connected either way round.

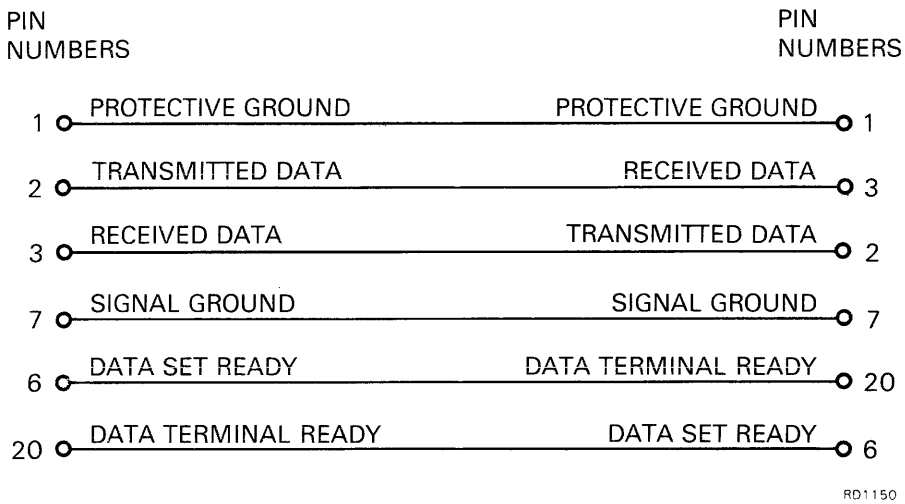


Figure 2-7 Null Modem Cable Connections

2.6.5 Modem Cables

Recommended modem cables are as follows.

1. BC22F (for EMC/RFI shielded cabinets)

   - Round 25-conductor fully shielded cable
   - Subminiature 25-pin D-type female connector on one end, male connector on the other
   - Lengths available.

     BC22F-10 – 3.1 m (10 ft)
     BC22F-25 – 7.62 m (25 ft)
     BC22F-35 – 10.72 m (35 ft)
     BC22F-50 – 15.24 m (50 ft)
     BC22F-75 – 22.9 m (75 ft).

2. BC05D

   - Round 25-conductor cable
   - Subminiature 25-pin D-type female connector on one end, male connector on the other
   - Lengths available.

     BC05D-10 – 3.1 m (10 ft)
     BC05D-25 – 7.62 m (25 ft)
     BC05D-50 – 15.24 m (50 ft)
     BC05D-60 – 18.6 m (60 ft)
     BC05D-A0 – 30.48 m (100 ft).

CAUTION

In some countries, protective hardware may be needed when connecting to certain lines. Refer to the national regulations before making a connection.

2.6.6 Data-Rate to Cable-Length Relationships

All the recommended cables have data-rate/cable-length characteristics as in Table 2-7. Cables of lengths different from those quoted in Sections 2.6.4 and 2.6.5 will have to be specially made. An acceptable non-FCC cable for this purpose is Belden type 8777.

Table 2-7 Data-Rate/Cable-Length Relationships

Data Rate (Bits/s)	Cable Length (Meters)	Cable Length (Feet)
110	914	3 000
300	914	3 000
1 200	152	500
2 400	152	500
4 800	76	250
9 600	76	250

NOTE

Cables longer than 15.24 m (50 ft), or with a total capacitance greater than 2.5 nanofarads, violate RS-232-C and V.28 specifications.

2.7 MULTIPLE COMMUNICATIONS OPTIONS

2.7.1 Floating Device-Addresses

On UNIBUS and Q-bus systems, a block of addresses in the top 4K words of address space is reserved for options with floating device-addresses. For UNIBUS systems, the floating-address range is 760010_8 to 763776_8.

Options which can be assigned floating device-addresses are listed in Table 2-8. This table gives the sequence of addresses for both UNIBUS and Q-bus options.

Having one list allows us to use one set of configuration rules and one configuration program.

Devices of the same type are given addresses in sequence, so all DZ11s have addresses higher than DU11s and lower than RL11s.

The column 'Size', in Table 2-8, shows how many words of address space are needed for each device. The column 'Modulus' is the modulus used for starting-addresses. For example, devices with an octal modulus of 10 must start at an address which is a multiple of 10_8. The same rule is used to select a gap-address (see the assignment rules) after an option, or for a nonexistent device.

Table 2-8 Floating Device Address Assignments

Rank	Device	Size (Decimal)	Modulus (Octal)	Notes
1	DJ11	4	10	
2	DH11	8	20	
3	DQ11	4	10	
4	DU11, DUV11	4	10	
5	DUP11	4	10	

Table 2-8 Floating Device Address Assignments (Cont)

Rank	Device	Size (Decimal)	Modulus (Octal)	Notes
6	LK11A	4	10	
7	DMC11/DMR11	4	10	DMC before DMR
8	DZ11/DZV11, DZS11, DZ32	4	10	A. DZ11 before DZ32
9	KMC11	4	10	
10	LPP11	4	10	
11	VMV21	4	10	
12	VMV31	8	20	
13	DWR70	4	10	
14	RL11, RLV11	4	10	B
15	LPA11-K	8	20	B
16	KW11-C	4	10	
17	Reserved	4	10	
18	RX11/RX211, RXV11/RXV21	4	10	B. RX11 before RX211
19	DR11-W	4	10	
20	DR11-B	4	10	C
21	DMP11	4	10	
22	DPV11	4	10	
23	ISB11	4	10	
24	DMV11	8	20	
25	DEUNA	4	10	B
26	UDA50/RQDX1	2	4	B
27	DMF32	16	40	
28	KMS11	6	20	
29	VS100	8	20	
30	TU81	2	4	
31	KMV11	8	20	
32	DHV11/DHU11	8	20	
33	DMZ32, CPI32 (async)	16	40	
34	Reserved	16	40	
35	Reserved	64	100	B
36	Reserved	4	10	
37	Reserved	8	20	
38	Reserved	4	10	B
39	Reserved	4	10	
40	Reserved	4	10	
41	ADV11-C	4	10	
42	AAV11-C	4	10	
43	AXV11-C	4	10	
44	KWV11-C	2	4	
45	ADV11-D	4	10	
46	AAV11-D	4	10	

NOTE
When there are no previous floating address space options in a system, the address of the first DHU11 installed is 760440_8.

A. DZ11-E and DZ11-F are treated as two DZ11s.

B. The first device of this type has a fixed address. Any extra devices have a floating address.

C. The first two devices of this type have a fixed address. Any extra devices have a floating address.

The address-assignment rules are as follows.

1. Addresses, starting at 760010_8 for UNIBUS systems, are assigned according to the sequence of Table 2-8.

2. Option- and gap-addresses are assigned according to the octal modulus as follows.

   a. Devices with an octal modulus of 4 are assigned an address on a 4_8 boundary (the two lowest-order address bits = 0).

   b. Devices with an octal modulus of 10 are assigned an address on a 10_8 boundary (the three lowest-order address bits = 0).

   c. Devices with an octal modulus of 20 are assigned an address on a 20_8 boundary (the four lowest-order address bits = 0).

   d. Devices with an octal modulus of 40 are assigned an address on a 40_8 boundary (the five lowest-order address bits = 0).

3. Address space equal to the device's modulus must be allowed for each device which is connected to the bus.

4. A 1-word gap, assigned according to rule 2, must be allowed after the last device of each type. This gap could be bigger when rule 2 is applied to the following rank.

5. A 1-word gap, assigned according to rule 2, must be allowed for each unused rank on the list if a device with a higher address is used. This gap could be bigger when rule 2 is applied to the following rank.

If extra devices are added to a system, the floating addresses may have to be reassigned in agreement with these rules.

In the following example, a brief description of UNIBUS address assignment is given. Note that the list includes floating-vector addresses. These are explained in Section 2.7.2.

Example: One DU11, one RL11, and two DHU11s

Address (Octal)		**Vector**
760010	DJ11 gap	
760020	DH11 gap	
760030	DQ11 gap	
760040	DU11	300
760050	DU11 gap	
760060	DUP11 gap	
760070	LK11A gap	
760100	DMC11 gap	
760110	DZ11 gap	
760120	KMC11 gap	

Address (Octal)		Vector
760130	LPP11 gap	
760140	VMV21 gap	
760160	VMV31 gap	
760170	DWR70 gap	
760200	RL11	310
760210	RL11 gap	
760220	LPA11-K gap	
760230	KW11-C gap	
760240	reserved gap	
760250	RX11 gap	
760260	DR11-W gap	
760270	DR11-B gap	
760300	DMP11 gap	
760310	DPV11 gap	
760320	ISB11 gap	
760340	DMV11 gap	
760350	DEUNA gap	
760354	UDA50 gap	
760400	DMF32 gap	
760420	KMS11 gap	
760440	VS100 gap	
760444	reserved gap	
760460	KMV11 gap	
760500	1st DHU11	320
760520	2nd DHU11	330
760540	DHU11 gap	

The first floating address is 760010. As the DJ11 has a modulus of 10_8, its gap can be assigned to 760010. The next available location becomes 760012.

As the DH11 has a modulus of 20_8, it cannot be assigned to 760012. The next modulo 20 boundary is 760020, so the DH11 gap is assigned to this address. The next available location is therefore 760022.

A DQ11 has a modulus of 10_8. It cannot be assigned to 760022. Its gap is therefore assigned to 760030. The next available location is 760032.

A DU11 has a modulus of 10_8. It cannot be assigned to 760032. It is therefore assigned to 760040. As the 'size' of DU11 is four words, the next available address is 760050.

There is no second DU11, so a gap must be left to indicate that there are no more DU11s. As 760050 is on a 10_8 boundary, the DU11 gap can be assigned to this address. The next available address is 760052.

And so on.

2.7.2 Floating Vectors

Addresses between 300_8 and 774_8 are designated as the floating-vector space. These addresses are assigned in sequence as in Table 2-9.

Each device needs two 16-bit locations for each vector. For example, a device with one receive and one transmit vector needs four words of vector space.

The vector assignment rules are as follows.

1. Each device occupies vector address space equal to 'Size' words. For example, the DLV11-J occupies 16 words of vector space. If its vector was 300_8, the next available vector would be at 340_8.

2. There are no gaps, except those needed to align an octal modulus.

An example of floating-vector address assignment is given in Section 2.7.1.

Table 2-9 Floating Vector Address Assignments

Rank	Device	Size (Decimal)	Modulus (Octal)	Notes
1	DC11	4	10	
1	TU58	4	10	
2	KL11	4	10	A
2	DL11-A	4	10	A
2	DL11-B	4	10	A
2	DLV11-J	16	10	
2	DLV11, DLV11-F	4	10	
3	DP11	4	10	
4	DM11-A	4	10	
5	DN11	2	4	
6	DM11-BB/BA	2	4	
7	DH11 modem control	2	4	
8	DR11-A, DRV11-B	4	10	
9	DR11-C, DRV11	4	10	
10	PA611 (reader + punch)	8	10	
11	LPD11	4	10	
12	DT07	4	10	
13	DX11	4	10	
14	DL11-C to DLV11-E	4	10	A
15	DJ11	4	10	
16	DH11	4	10	
17	VT40	8	10	
17	VSV11	8	10	
18	LPS11	12	10	
19	DQ11	4	10	
20	KW11-W, KWV11	4	10	
21	DU11, DUV11	4	10	
22	DUP11	4	10	
23	DV11 + modem control	6	10	
24	LK11-A	4	10	

Table 2-9 Floating Vector Address Assignments (Cont)

Rank	Device	Size (Decimal)	Modulus (Octal)	Notes
25	DWUN	4	10	
26	DMC11/DMR11	4	10	DMC before DMR
27	DZ11/DZS11/DZV11, DZ32	4	10	DZ11 before DZ32
28	KMC11	4	10	
29	LPP11	4	10	
30	VMV21	4	10	
31	VMV31	4	10	
32	VTV01	4	10	
33	DWR70	4	10	
34	RL11/RLV11	2	4	B
35	TS11, TU80	2	4	B
36	LPA11-K	4	10	
37	IP11/IP300	2	4	B
38	KW11-C	4	10	
39	RX11/RX211, RXV11/RXV21	2	4	B. RX11 before RX211
40	DR11-W	2	4	
41	DR11-B	2	4	B
42	DMP11	4	10	
43	DPV11	4	10	
44	ML11	2	4	C
45	ISB11	4	10	
46	DMV11	4	10	
47	DEUNA/DEQNA	12	4	B
48	UDA50/RQDX1	2	4	B
49	DMF32	16	4	
50	KMS11	6	10	
51	PCL11-B	4	10	
52	VS100	2	4	
53	TU81	2	4	
54	KMV11	4	10	
55	KCT32	4	10	
56	IEX	4	10	
57	DHV11/DHU11	4	10	
58	DMZ32, CPI32 (async)	12	4	
59	Reserved	12	4	
60	Reserved	4	1	
61	Reserved	2	4	
62	Reserved	2	4	
63	Reserved	2	4	
64	Reserved	2	4	B
65	Reserved	2	4	
66	Reserved	4	10	
67	ADV11-C	4	10	
68	AAV11-C	0	0	
69	AXV11-C	4	10	B
70	KWV11-C	4	10	
71	ADV11-D	4	10	

Table 2-9 Floating Vector Address Assignments (Cont)

Rank	Device	Size (Decimal)	Modulus (Octal)	Notes
72	AAV11-D	4	10	
73	QDSS	6	4	
74	DRV11-J	32	4	

A. A KL11 or DL11 used as the console has a fixed vector.

B. The first device of this type has a fixed vector. Any extra devices have a floating vector.

C. ML11 is a MASSBUS device which can connect to a UNIBUS via a bus adapter.

2.8 INSTALLATION TESTING

This section identifies the diagnostic tests that should be run on PDP-11 or VAX systems after the installation of a DHU11. Chapter 4, Maintenance, contains descriptions of the tests, and more detailed information on how they should be run.

DHU11 diagnostics are available for both PDP-11 and VAX systems. There are four types.

- Power-up self-test
- On-line diagnostics (VAX systems only)
- Functional verification tests
- System exercisers

The first three types provide an ascending level of confidence in the option.

As well as providing the highest level of confidence, functional verification tests also provide a means of quickly identifying a defective FRU.

System exercisers check that the options of a system will work together.

2.8.1 PDP-11 Installation Tests

The following diagnostics should be run on PDP-11 systems after installation. Note that each diagnostic name has a revision and a patch level. For example, ZDHUA1 identifies test ZDHU, revision level A and patch level 1. The symbol ? is a global indicator for revision and patch levels.

1. Self-test
2. Functional verification tests ZDHU??, ZDHV??, ZDHW??, and ZDHX??
3. DECX/11 exerciser XDHU??

XDHU?? is not directly runnable. The DECX/11 exerciser must first be configured into a run-time exerciser (see Chapter 4, Section 4.4.2). All individual device diagnostics should be run without error before DECX/11 is run.

The self-test runs automatically when the bus or DHU11 is reset. If no fault is found, the diagnostic LED will flash OFF/ON/OFF and then come ON permanently. The first OFF state is very short and may not be seen. However, if the LED goes OFF before coming ON permanently the diagnostic has found no faults. This does **not** prove that the option is serviceable.

During the self-test diagnostic operation, bytes are written to the RX FIFO. By reading these bytes, the engineer can receive more detailed information about the state of the DHU11. Diagnostic bytes and their interpretation are described in Chapter 3 of this document. The self-test can take up to 2.5 seconds.

The ZDHU??, ZDHV??, ZDHW??, and ZDHX?? diagnostics can be used:

- For testing a new installation
- For troubleshooting
- As a comprehensive confidence check.

The diagnostic listings describe these tests, and how to run them.

2.8.1.1 PDP-11 Installation Test Sequence

1. Switch on power, or reset the system. Check the diagnostic LED sequence.

2. Install staggered-loopback connectors on the BC05L cables.

3. Run all the ZDH diagnostics in sequence for one error-free pass. If there are no errors, the module is probably good.

4. Run the DECX/11 exerciser to verify that the DHU11 will run with other options of the system.

Re-cable the option for normal operation (see Figure 2-2). The DHU11 should now be ready for connection to external equipment. See Section 2.6 if necessary, for recommended modem and null-modem cables.

If any of the tests show errors, refer to Chapter 4, Maintenance, Sections 4.4 and 4.5, for diagnostic information and a troubleshooting flowchart.

2.8.2 VAX Installation Tests

In addition to the self-test, which functions as described in Section 2.8.1, the following VAX diagnostics are available.

- Standalone VAX diagnostic EVDAI
- On-line VAX diagnostic EVDAH
- User Environmental Test Program (UETP)

2.8.2.1 EVDAI Standalone Diagnostic – EVDAI is a suite of functional verification tests that can be used:

- As installation tests
- For troubleshooting
- As a more comprehensive confidence check.

The diagnostic listing ZZ-EVDAI describes the tests and how they are run.

2.8.2.2 EVDAH On-Line Diagnostic – This diagnostic provides a confidence check of DHU11s in VAX/VMS systems. Channels which have not been allocated to a process can be checked while the system is running application programs. The following tests can be selected.

1. Internal data-loopback test on selected channels in sequence.
2. Internal DMA data-loopback test on selected channels in sequence.

3. Internal data-loopback test on selected channels at the same time.
4. External loopback test (via H325) of modem control signals.
5. External data-loopback via a modem or H325. If a modem is used, it must be set up manually.

Diagnostic listing ZZ-EVDAH describes the tests and how to run them.

2.8.2.3 VAX/VMS System Exerciser UETP – This exerciser package checks that there is no unwanted interaction between the options connected to the system.

2.8.3 VAX Installation Test Sequence

The test sequence after installation is as follows.

1. Switch on power, or reset the system. Check the diagnostic LED sequence.

2. Install staggered-loopback connectors on the BC05L cables.

3. Run EVDAI for one error-free pass on all lines, in staggered-loopback mode.

4. Connect the option for normal operation.

5. Run EVDAH tests 1, 2, and 3 in internal-loopback mode for one error-free pass on all lines.

6. Run the system exerciser package UETP to verify that the DHU11 will run with other options of the system.

NOTE

Before EVDAI or EVDAH is run, the DHU11 must be 'attached' to the system (see the VAX Diagnostic System User's Guide). The form of the ATTACH command is:

DS> ATTACH DHU11 DW0 TYA xxxxxx yyy 5

where xxxxxx is the device address and yyy is the vector.

The DHU11 should now be ready for connection to external equipment. See Section 2.6 if necessary, for recommended modem and null-modem cables.

If any of the tests show errors, refer to Chapter 4, Section 4.6 for diagnostic information and a troubleshooting flowchart for the EVDAI diagnostic.

CHAPTER 3
PROGRAMMING

3.1 SCOPE

This chapter describes the control-and-status registers, and how they are used to control and monitor the DHU11. The chapter covers:

- The bit functions and format of each register
- Programming features available to the host.

Some programming examples are also included.

3.2 REGISTERS

The host controls and monitors the DHU11 module via a number of control-and-status registers.

Command words or bytes written to the registers are interpreted and processed by the firmware. Status reports and data are also transferred via the registers.

3.2.1 Register Access

DHU11 registers occupy eight words (16 bytes) of UNIBUS memory-mapped I/O space. However, by indexing, this is expanded internally to 115 words.

The position of the eight words within the I/O page is switch-selected on the DHU11. In order to access the module, bits <12:4> of an I/O address must match the address switch coding.

Table 3-1 lists the DHU11 registers and their addresses. The suffix (M) means that there are 16 of these registers, one for each channel. When an (M) register is accessed, the channel is selected by the contents of CSR<3:0>.

The term 'base' means the lowest I/O address on the module, that is to say, when the four low-order address bits = 0.

Registers are accessed by instructions which use 'base + n' as a source or destination. However, before multiple (M) registers are accessed, the channel number must be written to the CSR. The following example explains this.

To read the line-control register of channel 3, the following PDP-11 instructions are executed:

```
MOVB #CHAN,@#BASE     ;WRITE CHANNEL NUMBER (SEE BELOW) TO CSR
MOV @#BASE+10,R0      ;READ THE LINE-CONTROL REGISTER
```

In the example:

CHAN = 0er00011$_2$

Where e = the RXIE bit
and r = the MRST bit (would be 0)
and 0011$_2$ = channel number 3

NOTE

1. **Not all register bits are specified. During a write, all unspecified bits must be written as 0s. During a read, unspecified bits are undefined.**

2. **The exception to the above rule is that a bit may be written as logical 1 or 0 if it is read as logical 1. That is to say, read-modify-write instructions work correctly. Read-modify-write instructions should not be used on the base address or base + 2.**

3. **Writing to the LPR or LNCTRL registers on any line impacts the performance of every line.**

Table 3-1 DHU11 Registers

Register		Address (Octal)	Type
Control-and-Status Register	(CSR)	Base	Read/Write
Receive Buffer	(RBUF)	Base + 2	Read
Receive Timer *	(RXTIMER)	Base + 2	Write (byte)
Line Parameter Register	(LPR)	Base + 4 (M)	Read/Write
FIFO Data	(FIFODATA)	Base + 6 (M)	Write
FIFO Size	(FIFOSIZE)	Base + 6 (M)	Read (byte)
Line Status	(STAT)	Base + 7 (M)	Read (byte)
Line Control	(LNCTRL)	Base + 10 (M)	Read/Write
Transmit Buffer Address 1	(TBUFFAD1)	Base + 12 (M)	Read/Write
Transmit Buffer Address 2	(TBUFFAD2)	Base + 14 (M)	Read/Write
Transmit Buffer Count	(TBUFFCT)	Base + 16 (M)	Read/Write

* Only accessible when CSR<3:0> = 0000. See 3.2.2.1.

3.2.2 Register Bit Definitions

The register formats, which precede the definitions of the register bits, are coded as follows.

- Bits marked with an asterisk (*) may hold data-set status, or special information from the diagnostic programs. These are covered in Section 3.3.10.

- Registers which are modified by reset sequences are coded as shown in Figure 3-1.

= CLEARED BY MASTER RESET

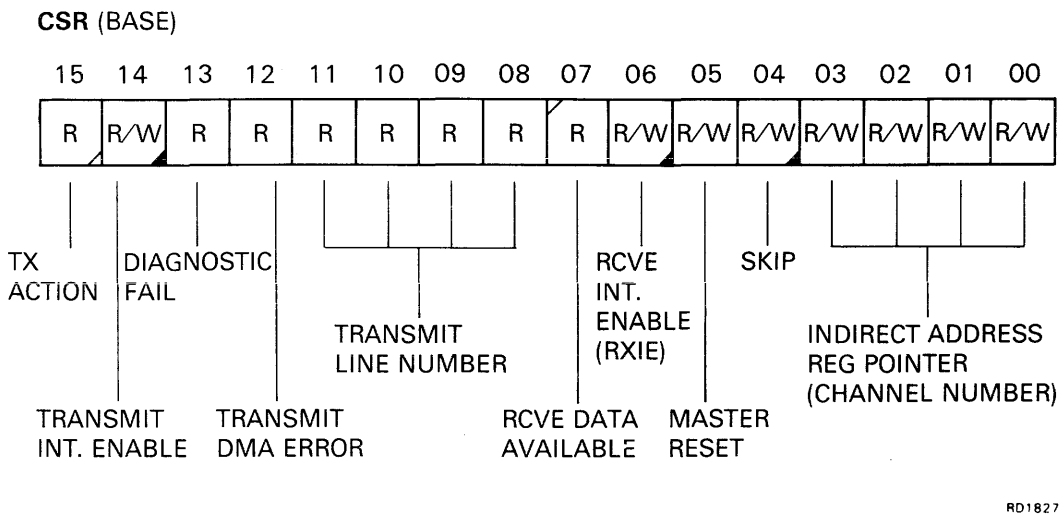
= SET BY MASTER RESET

= CLEARED BY BINIT, POWER-UP OR POWER-DOWN
BUT NOT BY MASTER RESET

RD1179

Figure 3-1 Register Coding

3.2.2.1 Base Control-and-Status Register (CSR)



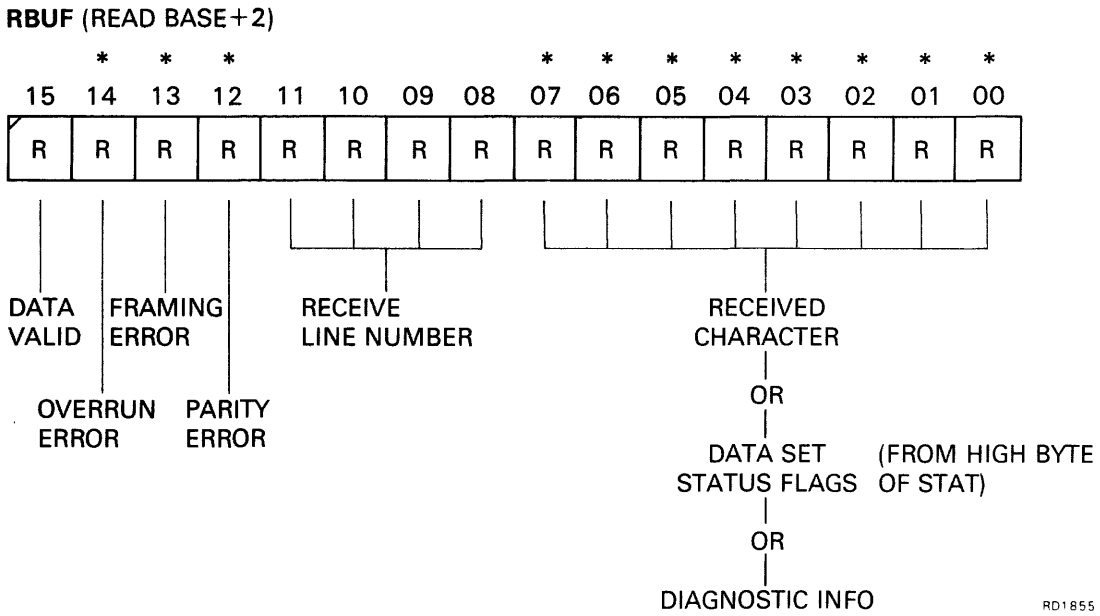
RD1827

Bit	Name	Description
<3:0>	IND.ADDR.REG (Indirect Address Register) (R/W)	These bits are used to select the channel when accessing a block of indexed (M) registers. They form the binary number of the channel which is to be accessed.
4	SKIP (Skip Self-Test) (R/W)	This bit is used to make the DHU11 skip the self-test operation. This will shorten the reset/initialization sequence to about 25 milliseconds. The bit must only be set at the same time as MASTER.RESET (write 60 to CSR). It must be cleared not less than 20 microseconds after it is set.

Bit	Name	Description
5	MASTER.RESET (Master Reset) (R/W)	Set by the host, in order to reset the DHU11 to a known state. Stays set while the DHU11 runs a self-test diagnostic and then performs an initialization sequence. The bit is then cleared to tell the host that the process is complete. This bit is set by BINIT (bus initialization signal), or by the host processor setting CSR<5>. The host must not write to any register, or read RBUF, while this bit is set, except during a 'skip self-test' operation.
6	RXIE (Receiver Interrupt Enable) (R/W)	When set, this bit allows the DHU11 to interrupt the host when RX.DATA.AVAIL is set. An interrupt is generated under the following conditions: 1. RXIE is set and a character is placed into the empty RX FIFO 2. The RX FIFO is not empty and RXIE is changed from 0 to 1. Cleared by BINIT but not by MASTER.RESET. The receive interrupt may be delayed by use of the RXTIMER register (see Section 3.2.2.3).
7	RX.DATA.AVAIL (Received Data Available) (RD)	When set, indicates that a received character is available. This bit is clear when the RX FIFO is empty. It is used to request an RX interrupt. Set after MASTER.RESET because the RX FIFO contains diagnostic information.
<11:8>	TX.LINE (Transmit Line Number) (RD)	If TX.ACTION is set, these bits hold the binary number of the channel on which one of the following has just occurred. 1. The TX FIFO has become empty. 2. A DMA transfer has been completed normally. 3. A DMA abort sequence has been completed. If TX.DMA.ERROR is also set, these bits contain the binary number of the channel which has failed during a DMA transfer.
12	TX.DMA.ERROR (Transmit DMA Error) (RD)	If set with TX.ACTION also set, means that the channel indicated by CSR<11:8> has failed to transfer DMA data within 21.3 microseconds of the bus request being acknowledged, or that there is a memory parity error. The TBUFFAD1 and TBUFFAD2 registers will contain the address of the memory location which could not be accessed. TBUFFCT will be cleared.

Bit	Name	Description
13	DIAG.FAIL (Diagnostic Fail) (RD)	When set, indicates that the DHU11 internal diagnostics have detected an error. The error may have been detected by the self-test diagnostic or by the BMP. This bit is associated with the diagnostic-passed LED. When it is set, the LED will be off. When it is cleared, the LED will be on. The bit is set by MASTER.RESET. It is cleared after the internal diagnostic programs have been run successfully. DIAG.FAIL is only valid after MASTER.RESET (CSR<5>) has been cleared.
14	TXIE (Transmit Interrupt Enable) (R/W)	When set, allows the DHU11 to interrupt the host when CSR<15> (TX.ACTION) becomes set. Cleared by BINIT but not by MASTER.RESET.
15	TX.ACTION (Transmit Action) (RD)	This bit is set by DHU11 when: 1. The last character of a DMA buffer has been transmitted 2. An abort sequence has been completed 3. A DMA transfer has been terminated by the DHU11 because nonexistent memory has been addressed, or because of a memory parity error 4. A TX FIFO becomes empty during a TX FIFO output sequence. This bit is cleared if the host reads the CSR after the TX Action FIFO has become empty. To avoid losing TX Action reports, the host must not let more than 16 reports accumulate. It is advisable to read the CSR until TX.ACTION becomes clear, otherwise a TX interrupt will not be generated when further reports are loaded. Also cleared by MASTER.RESET. NOTE **CSR contents should only be accessed by a PDP-11 MOV or MOVB instruction, or the VAX equivalent (MOVW or MOVB). Other instructions may lose the state of the TX.ACTION bit (CSR<15>).**

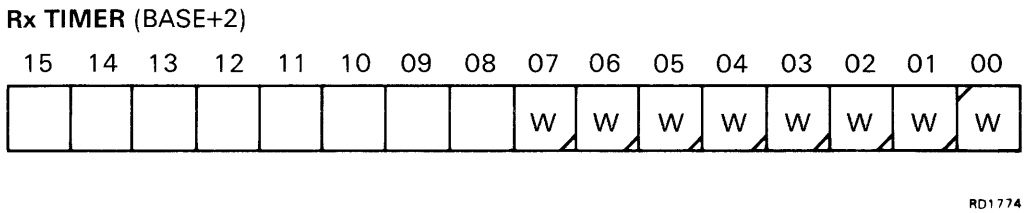
3.2.2.2 Receive Buffer (RBUF) – This is a read-only register at address Base + 2. Reading the register accesses the oldest word in the 256-word RX FIFO. The least-significant bit (LSB) of the character is in bit 0.



Bit	Name	Description
<7:0>	RX.CHAR (Received Character) (RD)	If RBUF<14:12> = 000, these eight bits contain the oldest character in the FIFO. The character is good. If RBUF<14:12> = 001, 010, or 011, these eight bits contain the oldest character in the FIFO. The character is bad. If RBUF<14:12> = 111, these eight bits contain diagnostic or modem status information. In this case, RBUF<0> has the following meanings. 0 = Modem status in RBUF<7:1> (see Section 3.2.2.7) 1 = Diagnostic information in RBUF<7:1> (see Section 3.3.10). If there is an overrun condition, the UART data buffer for that channel will be cleared. A null character with RBUF<14> set (40000_8) will be placed in the RX FIFO. The cleared data will be lost. The DHU11 does not have a break-detect bit. A line break is indicated to the program as a null character with the FRAME.ERR set (20000_8).
<11:8>	RX.LINE (Receive Line Number) (RD)	These bits hold the binary number of the channel on which the character of RBUF<7:0> was received or on which a data-set change was reported.

Bit	Name	Description
12	PARITY.ERR (Parity Error) (RD)	Set if this character has a parity error and parity is enabled for the channel indicated by bits <11:8> (also see RX.CHAR).
13	FRAME.ERR (Framing Error) (RD)	Set if the first stop bit of the received character was not detected (also see RX.CHAR).
14	OVERRUN.ERR (Overrun Error) (RD)	Set if one or more previous characters of the channel indicated by bits <11:8> were lost because of a full FIFO, or failure to service the UARTs (also see RX.CHAR). **NOTE** **The 'all 1s' code for bits <14:12> is reserved. This code indicates that modem status or diagnostic information is held in RBUF<7:0>.**
15	DATA.VALID (Data Valid) (RD)	Set if the FIFO is not empty. Cleared by MASTER.RESET or by the FIFO becoming empty. After self-test, diagnostic information is loaded into the RX FIFO. Therefore, this bit is always set after a successful master-reset sequence.

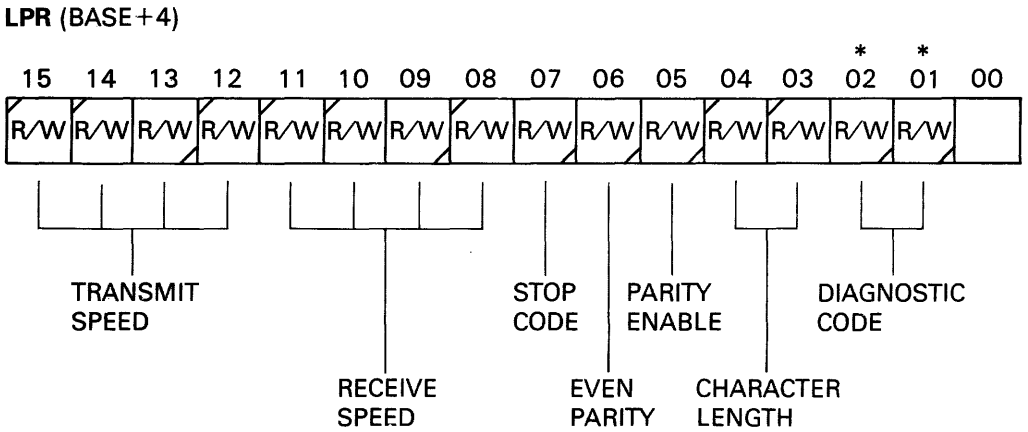
3.2.2.3 Receive Timer Register (RXTIMER) – The indirect address register (CSR<3:0>) must = 0000 in order to access the receive timer. It can be used by the host to delay the receive interrupt.



Bit	Name	Description
<7:0>	RX.TIMER (Receive Timer) (WR BYTE)	The receive interrupt is normally raised when a received character is loaded into the previously empty RX FIFO. The binary number loaded into RXTIMER modifies this procedure as follows. 0 = Infinite timeout. This timeout will be overridden by the conditions below. 1 = No timeout. The interrupt will be raised immediately. 2 to 255 = Timer delay in milliseconds

Bit	Name	Description
		The timer is overridden when the FIFO becomes three-quarters full (critical) or when a modem status change is written to the FIFO. Set to 1 by MASTER RESET.

3.2.2.4 Line Parameter Register (LPR) – This register is used to configure its associated channel. Bit function is as follows.



Bit	Name	Description
<2:1>	DIAG (Diagnostic Code) (R/W)	Diagnostic control codes. Used by the host as follows. 00 = Normal operation 01 = Causes the background monitor program (BMP) to report the DHU11 status via the RX FIFO. BMP reports are covered in Section 3.3.10. Set to 00 by MASTER.RESET.
<4:3>	CHAR.LGTH (Character Length) (R/W)	Defines the length of characters. Does not include start, stop, and parity bits. 00 = 5 bits 01 = 6 bits 10 = 7 bits 11 = 8 bits Set to 11 by MASTER.RESET.

Bit	Name	Description
5	PARITY.ENAB (Parity Enable) (R/W)	Parity enable. Causes a parity bit to be generated on transmit, and checked and stripped on receive. 1 = Parity enabled 0 = Parity disabled Cleared by MASTER.RESET.
6	EVEN.PARITY (Even Parity) (R/W)	If LPR<5> is set, this bit defines the type of parity. 1 = Even parity 0 = Odd parity Cleared by MASTER.RESET.
7	STOP.CODE (Stop code) (R/W)	Defines the length of the transmitted stop bit. 0 = 1 stop bit for 5-, 6-, 7- or 8-bit characters 1 = 2 stop bits for 6-, 7-, or 8-bit characters or 1.5 stop bits for 5-bit characters Cleared by MASTER.RESET.
<11:8>	RX.SPEED (Received Data Rate) (R/W)	Set to 1101 by MASTER.RESET. (9 600 bits/s) Defines receive data rate (Table 3-2).
<15:12>	TX.SPEED (Transmitted Data Rate) (R/W)	Set to 1101 by MASTER.RESET. (9 600 bits/s) Defines transmit data rate (Table 3-2).

Table 3-2 Data Rates

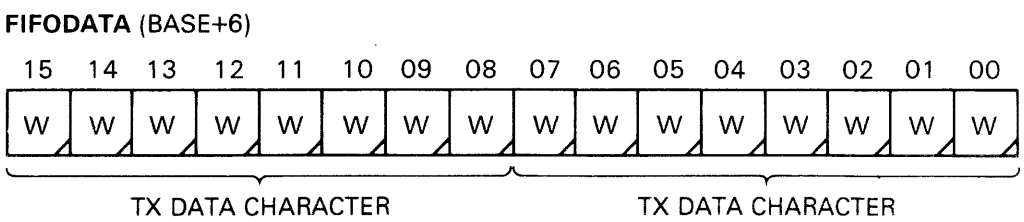
Code	Data Rate (Bits/s)	Maximum Error (%)	Groups
0000	50	0.01	A
0001	75	0.01	B
0010	110	0.08	A and B
0011	134.5	0.07	A and B
0100	150	0.01	B
0101	300	0.01	A and B
0110	600	0.01	A and B
0111	1 200	0.01	A and B
1000	1 800	0.01	B
1001	2 000	0.19	B
1010	2 400	0.01	A and B
1011	4 800	0.01	A and B
1100	7 200	0.01	A
1101	9 600	0.01	A and B
1110	19 200	0.01	B
1111	38 400	0.01	A

NOTE

The DHU11 16-channel interface uses eight dual-channel ICs. Channels 0/1, 2/3, 4/5, 6/7, 8/9, 10/11, 12/13, and 14/15 are paired. It is the responsibility of the user to select transmit and receive data rates of the same group (A or B), for any pair of channels.

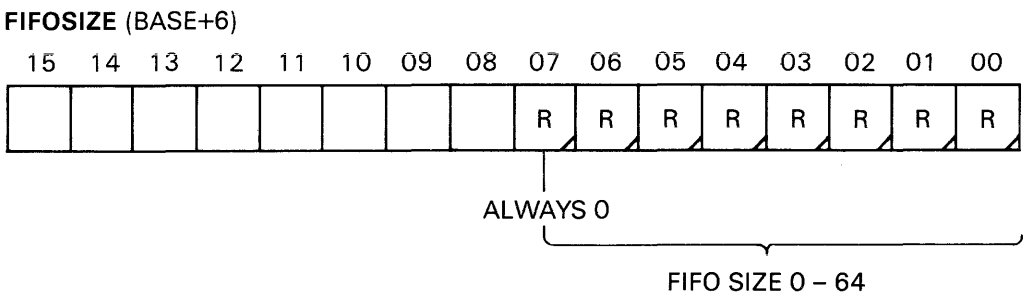
If channels within the same DUART are configured in different groups, the resulting data rates are undefined.

3.2.2.5 FIFO Data Register (FIFODATA) – A write to FIFODATA is interpreted as a write to a TX FIFO. To send a character or characters via a TX FIFO, the host writes the character(s) to the FIFO data register of the appropriate channel. To make sure that there is room in the TX FIFO, the host should first read the associated FIFO size register (See Section 3.2.2.6). If single characters are sent, they must be written to the low byte of FIFODATA.



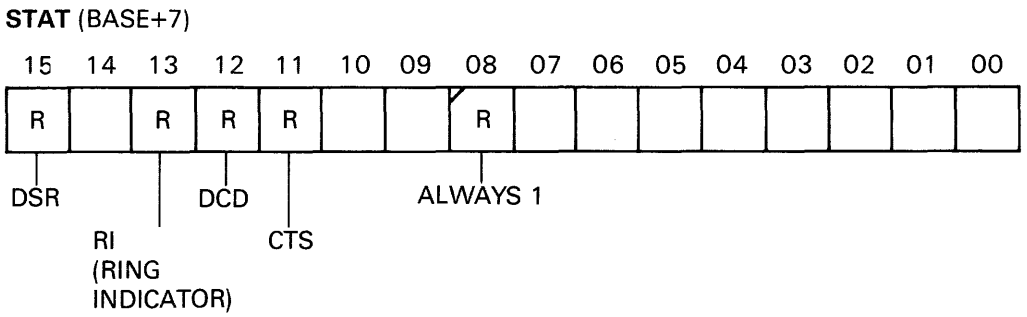
Bit	Name	Description
<7:0>	FIFODATA<7:0> (FIFO Data Byte Register) (WR BYTE)	Contains a single character for transfer via the TX FIFO. After a write-byte action to this register, FIFODATA<7:0> is transferred to the FIFO. The least-significant bit of the character is in FIFODATA bit 0. Unused bits must be cleared. Cleared by MASTER.RESET.
<15:0>	FIFODATA<15:0> (FIFO Data Register) (WR)	Contains two characters for transfer via the TX FIFO. After a write-word action to this register, FIFODATA<7:0> and then FIFODATA<15:8> are transferred to the FIFO. The least-significant bits of the characters are in FIFODATA, bits 0 and 8. Unused bits must be cleared. Cleared by MASTER.RESET.

3.2.2.6 FIFO Size Register (FIFOSIZE) – This low-byte register holds a number which indicates the space available in the TX FIFO.



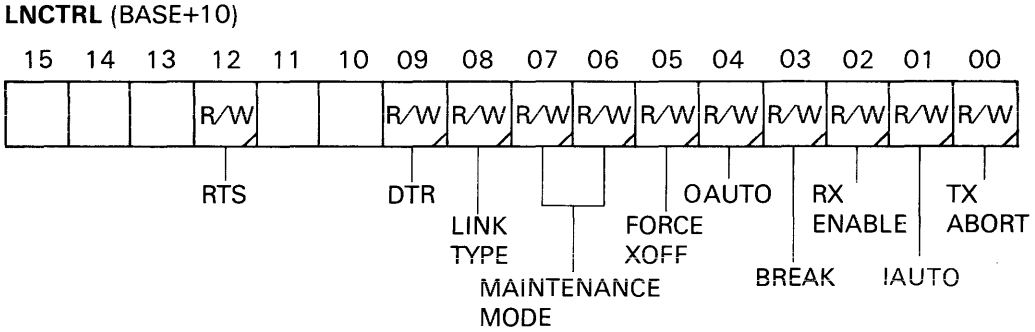
Bit	Name	Description
7:0	FIFOSIZE (FIFO Size) (RD BYTE)	Indicates the available space (in characters) in the TX FIFO. The range is 000_8 (0_{10}) to 100_8 (64_{10}). This register should be read before sending a character, or a sequence of characters, to the FIFO data register. **NOTE** **This register can be read (RD WORD) at the same time as the STAT register.** Set to 100_8 by MASTER.RESET

3.2.2.7 Line Status Register (STAT) – This high-byte register is read from base + 7. It holds modem status information.



Bit	Name	Description
8	DHUID (DHU11 Identifier) (RD)	Tells the host whether a DHU11 or a DHV11 is installed. This bit is not valid while MASTER.RESET is set. Always 1 on DHU11 (0 on DHV11).
11	CTS (Clear to Send) (RD)	Gives the present status of the Clear To Send (CTS) signal from the modem. 1 = ON 0 = OFF
12	DCD (Data Carrier Detect) (RD)	Gives the present status of the Data Carrier Detect (DCD) signal from the modem. 1 = ON 0 = OFF
13	RI (Ring Indicator) (RD)	Gives the present status of the Ring Indicator (RI) signal from the modem. 1 = ON 0 = OFF
15	DSR (Data Set Ready) (RD)	Gives the present status of the Data Set Ready (DSR) signal from the modem. 1 = ON 0 = OFF **NOTE** **In order to report a change of modem status, the DHUll writes the contents of STAT<15:9> into RBUF<7:1>. RBUF bit 0 will be clear. RBUF<14:12> = 111 to tell the host that RBUF<7:0> do not hold a received character (see Section 3.3.8, Modem Control).** **This register can be read (RD WORD) at the same time as the FIFO size register.**

3.2.2.8 Line Control Register (LNCTRL) – The main function of this register is to control the line interface.



Bit	Name	Description
0	TX.ABORT (Transmitter Abort) (R/W)	Set by the host to halt the transfer of data. If a DMA transfer was in progress, the DMA address and count registers (TBUFFAD1, TBUFFAD2, and TBUFFCT) will be updated to reflect the number of characters which have been transmitted. The transfer can be continued by clearing TX.ABORT, and then setting TX.DMA.START in TBUFFAD2. No characters will be lost. The program must make sure that TX.ABORT is clear before setting TX.DMA.START. Otherwise the transfer will be aborted before any characters are transmitted. If a programmed transfer was in progress, characters in the TX FIFO will be discarded. Because of firmware delays, it is possible to transmit a few characters before the abort is actioned. Therefore, the host cannot determine how many characters have been lost. When an abort sequence has been completed, the DHU11 will set the TX.ACTION bit in the CSR. If the transmitter interrupt is enabled, the program will be interrupted at the transmit vector. See Section 3.3.3.1, DMA Transfers, for the use of TX.ABORT. Cleared by MASTER.RESET.
1	IAUTO.FLOW (Incoming Auto Flow) (R/W)	This is the auto-flow control bit for incoming characters. If this bit is set, the DHU11 will control incoming characters by transmitting XON and XOFF codes. If the RX FIFO becomes congested, the DHU11 will send an XOFF code to channels with this bit set. An XON will be sent when the congestion is reduced. See Section 3.3.6, Auto XON and XOFF.

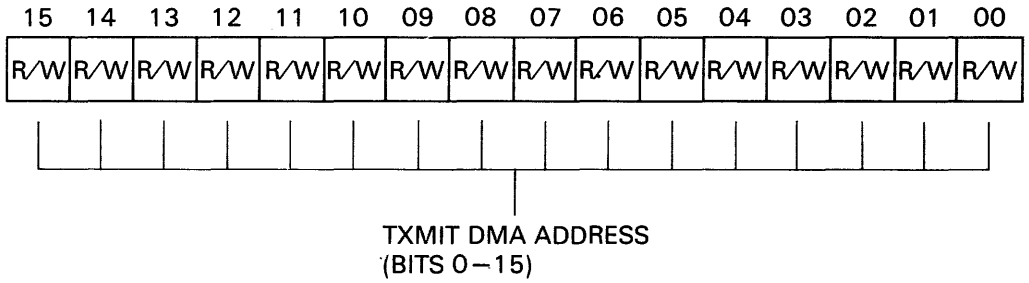
Bit	Name	Description
		Cleared by MASTER.RESET. **NOTE** **An XON code = 21_8 = DC1 = CTRL/Q.** **An XOFF code = 23_8 = DC3 = CTRL/S.** **No other codes are specified for the interface.**
2	RX.ENA (Receiver Enable) (R/W)	If this bit is set, this receiver channel is enabled. If this bit is reset when this DUART channel is assembling a character, that character may be lost. Cleared by MASTER.RESET.
3	BREAK (Break Control) (R/W)	If set, this bit forces the transmitter of this channel to the spacing state. Transmission is restarted when the bit is cleared. Cleared by MASTER.RESET. **NOTE** **There is a short delay between writing the bit and the channel changing state. The delay is dependent on the amount of DHU11 activity. Because of the normal length of a BREAK signal, this should not cause problems.**
4	OAUTO (Outgoing Auto Flow) (R/W)	This bit is the auto-flow control bit for outgoing characters. When OAUTO and RX.ENA are both set, the DHU11 will automatically respond to XON and XOFF codes received from a channel. The DHU11 uses the TX.ENA bit in TBUFFAD2 to stop and start the flow. See Section 3.3.6, Auto XON and XOFF. Cleared by MASTER.RESET.
5	FORCE.XOFF (Force XOFF) (R/W)	This bit can be set by the program to indicate that this channel is congested at the host system (for example, if the typeahead buffer is full). When it sees this bit set, the DHU11 will send an XOFF code. Until the bit is reset, XOFFs will be sent after every alternate character received on that channel. When the bit is reset, an XON will be sent unless IAUTO is set and the RX FIFO is critical. See Section 3.3.6, Auto XON and XOFF. Cleared by MASTER.RESET.

Bit	Name	Description
<7:6>	MAINT (Maintenance Mode) (R/W)	These bits can be written by the driver or test programs, in order to test the channel. The coding is as follows. 00 = Normal operation 01 = Automatic echo mode – Received data is retransmitted (regardless of the state of TX.ENA) **at the data rate selected for the receiver.** The received characters are processed normally and placed in the RX FIFO. In this mode, the DHU11 will not transmit **any** characters (this includes internally generated flow-control characters). The RX.ENA bit must be set when operating in this mode. 10 = Local loopback – The DUART channel output is internally connected to the input. Normal received data is ignored and the transmit data line is held marking. In this mode, flow-control characters will be looped back instead of being transmitted. The data rate selected for the transmitter is used for both transmission and reception. The TX.ENA bit still controls transmission in this mode. RX.ENA is ignored. 11 = Remote loopback – In this mode received data is retransmitted at a clock rate equal to the received clock rate. The data is not placed in the RX FIFO. The state of TX.ENA is ignored but RX.ENA must be set. Cleared to 00 by MASTER.RESET.
8	LINK.TYPE (Link Type) (R/W)	This bit must be set if the channel is to be connected to a modem. When the bit is set, any change in modem status will be reported via the RX FIFO as well as the STAT register. If this bit is reset, this channel becomes a 'data leads only' channel. Modem status information is loaded in the high byte of STAT but is not placed in the FIFO. Cleared by MASTER.RESET.
9	DTR (Data Terminal Ready) (R/W)	This bit controls the Data Terminal Ready (DTR) signal to the modem. 1 = ON 0 = OFF Cleared by MASTER.RESET.

Bit	Name	Description
12	RTS (Request to Send) (R/W)	This bit controls the Request To Send (RTS) signal to the modem. 1 = ON 0 = OFF Cleared by MASTER.RESET.

3.2.2.9 Transmit Buffer Address Register Number 1 (TBUFFAD1) –

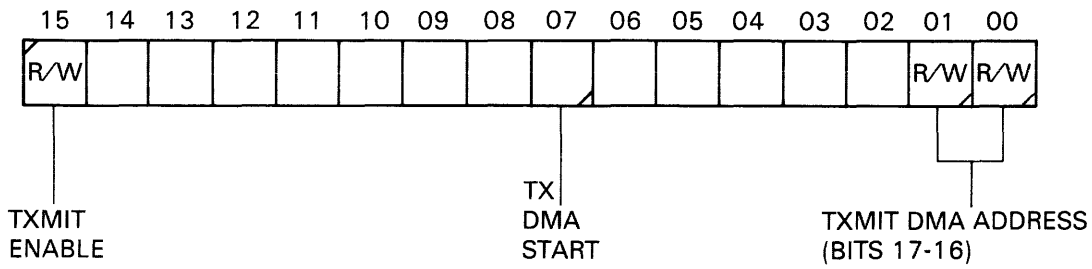
TBUFFAD1 (BASE+12)



Bit	Name	Description
<15:0>	TBUFFAD<15:0> (Transmit Buffer Address [Low]) (R/W)	Bits <15:0> of the DMA address (also see Section 3.2.2.10). Cleared by MASTER.RESET.

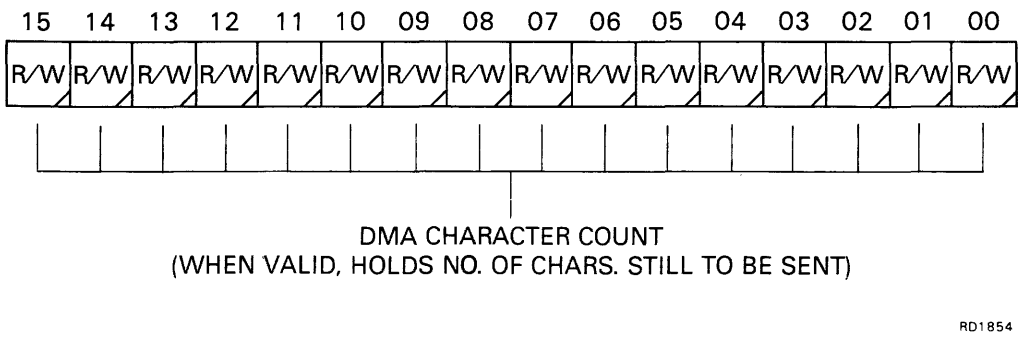
3.2.2.10 Transmit Buffer Address Register Number 2 (TBUFFAD2) –

TBUFFAD2 (BASE+14)



Bit	Name	Description
<1:0>	TBUFFAD<17:16> (Transmit Buffer Address [High]) (R/W)	Bits <17:16> of the DMA address. Before a DMA transfer, TBUFFAD1 and the low byte of TBUFFAD2 are loaded with the start address of the DMA buffer. This address is not valid during a DMA transfer. When TX.ACTION is returned, the address will be valid. Cleared by MASTER.RESET.
7	TX.DMA.START (Transmit DMA Start) (R/W)	Set by the host to start a DMA transfer. The DHU11 will reset the bit before returning TX.ACTION. Cleared by MASTER.RESET. **NOTE** **After setting this bit, the host must not write to TBUFFCT, TBUFFAD1, TBUFFAD2 <7:0>, or FIFODATA until the TX.ACTION report has been returned.**
15	TX.ENA (Transmitter Enable) (R/W)	When this bit is set, the DHU11 will transmit all characters. When this bit is cleared, the DHU11 will only transmit **internally** generated flow-control characters. In the OAUTO mode, this bit is used by the DHU11 to control outgoing characters. See Section 3.3.6, Auto XON and XOFF. Set by MASTER.RESET.

3.2.2.11 Transmit DMA Buffer Counter (TBUFFCT) –



Bit	Name	Description
<15:0>	TX.CHAR.CT (Transmit Character Count) (R/W)	Loaded with the number of characters to be transferred by DMA. The number of characters is specified as a 16-bit unsigned integer. After a DMA transfer has been aborted this location will hold the number of characters still to be transferred. See also the previous note (Section 3.2.2.10, TX.DMA.START). Cleared by MASTER.RESET.

3.3 PROGRAMMING FEATURES

3.3.1 Initialization

The DHU11 is initialized by its on-board firmware.

Initialization takes place after a bus-reset sequence, or when the host sets CSR<5> (MASTER. RESET).

Before starting initialization, the on-board diagnostics run a self-test program. The results of this test are reported by eight diagnostic bytes in the RX FIFO.

NOTE

This self-test diagnostic can be skipped on command from the program. This is covered in Section 3.3.10.3.

The DHU11 state, after a successful self-test, is as follows.

1. Eight diagnostic codes are placed in the RX FIFO
2. The diagnostic fail bit (CSR<13>) is reset
3. All channels set for:

    a. Send and receive 9 600 bits/s
    b. Eight data bits
    c. One stop bit
    d. No parity
    e. Parity odd
    f. Auto-flow off
    g. RX disabled
    h. TX enabled
    i. No break on line
    j. No loopback
    k. No modem control
    l. DTR and RTS off
    m. DMA character count zero
    n. DMA start address zero
    o. TX.DMA.START cleared
    p. TX.DMA.ABORT cleared
    q. FIFO SIZE set to 100_8

The DHU11 clears the MASTER.RESET bit (CSR<5>) when initialization and self-test are complete.

3.3.2 Configuration

After DHU11 self-initialization, the driver program can configure the module as needed. This is done via the LPR and LNCTRL registers.

By writing to the associated LPR and LNCTRL, the program can select data rate, character length, parity, and number of stop bits for each channel. Individual receivers and transmitters can be enabled and auto-flow selected.

For operation with any device which uses modem control signals, LINK.TYPE of the associated LNCTRL register should be set.

3.3.3 Transmitting

Data can be transferred to the serial interface by two methods. Blocks of characters can be transferred under DMA control, or the host can write one or two characters at a time to the FIFO data register. Such transfers are covered in the following subsections.

3.3.3.1 DMA Transfers – Before setting up the transfer of a DMA buffer, the program should make sure that TX.DMA.START is not set. TBUFFCT, TBUFFAD1, TBUFFAD2, and FIFODATA should not be written unless TX.DMA.START is clear.

Transmission will start when the program sets TX.DMA.START.

The size of the DMA buffer, and its start address, can be written to TBUFFCT, TBUFFAD1, and TBUFFAD2 in any order. However, TBUFFAD2 contains TX.ENA and TX.DMA.START, so it is simpler to write TBUFFAD2 last. By using byte operations on this register, TX.ENA and TX.DMA.START can be separated. TX.ACTION, when set, indicates the UART has finished transmitting the last character.

The DHU11 will perform the transfer, and set TX.ACTION when it is complete. If TXIE is set, the program will be interrupted at the transmit vector. Otherwise, TX.ACTION must be polled to detect the end of the DMA operation.

To abort a DMA transfer, the program must set TX.ABORT. The DHU11 will stop transmission, and update TBUFFCT, TBUFFAD1, and TBUFFAD2<7:0> to reflect the number of characters which have been transmitted. TX.DMA.START will be cleared. If the interrupt is enabled, TX.ACTION will interrupt the program at the transmit vector. If the program clears TX.ABORT and sets TX.DMA.START, the transfer can be resumed without loss of characters.

If a DMA transfer fails because of a memory error, the transmission will be terminated. TBUFFAD1 and TBUFFAD2 will point to the failing location. TBUFFCT will be cleared, and TX.DMA.ERROR and TX.ACTION will be set. If TXIE is set, the TX interrupt will be raised.

3.3.3.2 Programmed Transfers – Before writing a character or a sequence of characters to the FIFO data register (FIFODATA), the program should read the FIFO size register (FIFOSIZE) to check that there is space in the TX FIFO.

If there is space for characters, they can be written as bytes (one character) or words (two characters) to FIFODATA. After a low-byte write, FIFODATA<7:0> will be transferred to the FIFO. After a word write, FIFODATA<7:0> and then FIFODATA<15:8> will be transferred to the FIFO. High-byte writes to FIFODATA are not allowed.

The DHU11 returns TX.ACTION when the TX FIFO becomes empty. As with DMA transfers, this bit can be sensed via interrupt or by polling the CSR.

In programmed-transfer FIFO mode, TX.ACTION is returned when the DHU11 transfers the last character from the RX FIFO to the DUART, **not** when it has been transmitted. Each channel has a two-character buffer. Thus, if modem status bits or line parameters are changed immediately after the last TX.ACTION of a message, the end of the message could be lost. The program can avoid loss by adding two null characters to the end of each programmed-transfer FIFO message.

To abort a programmed transfer, the program must set TX.ABORT. The DHU11 will terminate the transfer and then set TX.ACTION. If TXIE is set, the TX interrupt will be raised. Characters in the TX FIFO will be discarded, but because of firmware delays the host cannot determine how many characters have been lost.

3.3.3.3 Methods of Control – Examples of control by polling or by the use of interrupts are given in Section 3.4, Programming Examples.

3.3.4 Receiving

Received characters, tagged with the channel number and DATA.VALID, are placed in the RX FIFO buffer (RBUF). If a character is put in an empty RBUF, the DHU11 sets RX.DATA.AVAIL. It remains set while there is valid data in there. If RXIE is set, the program will be interrupted at the receive vector. The program's interrupt routine should read RBUF until DATA.VALID is reset.

NOTE

Subject to the RX timer, a receive interrupt is generated when RX.DATA.AVAIL and RXIE both become set. If the interrupt routine does not empty the FIFO, RXIE must be toggled to raise another interrupt.

If RXIE is not set, the program must poll RBUF often enough to prevent data loss.

3.3.5 Interrupt Control

An interrupt priority level of 5 or 6 is selected by switches on the module. During an interrupt sequence, the DHU11 will provide one of two vectors.

1. A 'base' vector set on the interrupt vector switches
2. A 'base + 4' vector

Subject to the value in RXTIMER (Section 3.2.2.3), the base vector is supplied whenever data is put into an empty RX FIFO.

The 'base + 4' vector is supplied when:

1. A TX FIFO has become empty. This may be because all characters have been transmitted, or because the program has aborted the transfer.

2. A complete DMA block has been transferred.

3. A DMA transfer has been aborted, or terminated due to a memory error.

At the two vectors, the host must provide the addresses of suitable routines to deal with the above conditions.

3.3.6 Auto XON and XOFF

XON and XOFF codes are commonly used to control data flow on communications channels. To use this facility, interfaces must have suitable decoding hardware or software.

A channel which receives an XOFF stops sending characters until it receives an XON. A channel which is becoming overrun by received data, sends an XOFF. It sends an XON when the congestion is relieved.

If the DHU11 is programmed for automatic flow control (auto-flow), it can automatically regulate the flow of characters. Three bits control this function:

1. IAUTO – LNCTRL<1>
2. FORCE.XOFF – LNCTRL<5>
3. OAUTO – LNCTRL<4>

IAUTO and FORCE.XOFF both control incoming characters. IAUTO is an enable bit which allows the state of the RX FIFO counters to control the generation of XOFF and XON codes. The FORCE.XOFF bit is a direct command from the program.

1. The DHU11 hardware recognizes when the FIFO is three-quarters full and half full. The firmware uses these states for auto flow control.

   If the program sets a channel's IAUTO bit, the DHU11 will send that channel an XOFF if it receives a character after the FIFO becomes three-quarters full. If the channel does not respond to XOFF, the DHU11 will send an XOFF in reply to every alternate character received. An XON will be sent when the FIFO becomes less than half full, unless FORCE.XOFF for that channel is set. XONs are only sent to channels to which an XOFF has been sent.

   By inserting XON and XOFF characters into the data stream, the program can perform flow control directly. However, if the DHU11 is in the IAUTO or FORCE.XOFF mode, the results will be unpredictable.

   These internally generated XONs and XOFFs will be transmitted even if TX.ENA is cleared.

2. When FORCE.XOFF is set, the DHU11 sends an XOFF and then acts as if IAUTO is set and the FIFO is critical (was three-quarters full, not yet less than half full). When FORCE.XOFF is reset, an XON will be sent unless the FIFO is critical and IAUTO is set (see 1, IAUTO).

   NOTE

   If both FORCE.XOFF and IAUTO become clear after XOFF has been sent, an XON will be sent immediately.

3. If the program sets OAUTO, the DHU11 will automatically respond to XON and XOFF characters from the channel. It does this by setting and clearing the TX.ENA bit.

   The program may also control the TX.ENA bit. In this case it is important to keep track of received XON and XOFF characters.

Received XON and XOFF characters will always be reported via the FIFO. It is possible during read/modify/write operations by the program, for the DHU11 to change the TX.ENA bit between the read and the write action. For this reason, if DMA transfers are started while OAUTO is set, it is advisable to write to the low byte of TBUFFAD2 only.

NOTE

1. **The DHU11 may change the state of TX.ENA for up to 20 microseconds after OAUTO is cleared by the program.**

2. **When checking for flow-control characters, the DHU11 only checks characters which do not contain transmission errors. The parity bit is stripped and the remaining bits are checked for XON (21_8) and XOFF (23_8) codes.**

3.3.7 Error Indication

The program is informed of transmission and reception errors by means of four bits.

1. TX.DMA.ERR – CSR<12>. See Section 3.2.2.1
2. PARITY.ERR – RBUF<12>. See Section 3.2.2.2
3. FRAME.ERR – RBUF<13>. See Section 3.2.2.2
4. OVERRUN.ERR – RBUF<14>. See Section 3.2.2.2.

RBUF<14:12> are also used to identify a diagnostic or modem status code.

3.3.8 Modem Control

Each channel of the module provides modem control bits for RTS and DTR. Modem status inputs CTS, DSR, RI, and DCD are also provided on each channel. These bits can be used for modem control or as general-purpose outputs and inputs (see Section 3.2.2.7, STAT Register).

CTS, DSR and DCD are sampled by PROC2 every 10 ms, and also when a character is received while LINK.TYPE (LNCTRL<8>) is set. Therefore, to make sure that a change is detected, these bits must stay steady for at least 10 ms after a change. RI is also sampled every 10 ms, but a change is not reported unless the new state is held for three consecutive samples. There are no hardware controls between the modem control logic and the receiver and transmitter logic. Any coordination should be done under program control. Modem-status-change reports are placed in the RX FIFO at the correct position relative to the received characters.

By setting LINK.TYPE (LNCTRL<8>), a channel can be selected for modem operation. Any change of the modem status inputs will be reported to the program via the RX FIFO. Modem control bits must be driven by the program's communication routines. Control bits are written to the LNCTRL register.

Appendix B gives more detail of modem control.

By clearing LINK.TYPE the channel is selected as a 'data lines only' channel. Modem control and status bits can still be managed by the program, but status bits must be polled at the line status register. Changes of modem status will **not** be reported to the program.

NOTE

When transmitting by the programmed transfer method, up to two characters can be buffered in DHU11 hardware. If modem control bits are to be changed at the end of a transmission, two null characters should be added. When TX.ACTION is set after the second null character, the last genuine character has left the UART.

Status change reporting is done via the RX FIFO as follows.

- When OVERRUN.ERR, FRAME.ERR, and PARITY.ERR are all set, the eight low-order bits contain either status change or diagnostic information. In this case:
  - If RBUF<0> = 0, RBUF<7:1> hold STAT<15:9> (see Section 3.2.2.7).
  - If RBUF<0> = 1, RBUF<7:1> hold diagnostic information (see Section 3.3.10).

3.3.9 Maintenance Programming

As well as using on-board and external diagnostic programs, the LNCTRL register allows each channel to be configured in normal, automatic-echo, local-loopback, and remote-loopback modes (see Section 3.2.2.8, LNCTRL).

3.3.10 Diagnostic Codes

3.3.10.1 Self-Test Diagnostic Codes – After bus reset or master reset, the DHU11 executes a self-test and initialization sequence. At the end of the sequence, eight diagnostic codes are put in the RX FIFO. RX.DATA.AVAIL is set and MASTER.RESET is cleared.

After an error-free test, DIAG.FAIL will be reset. The 'diagnostic passed' LED will be on. If an error is detected, DIAG.FAIL will be set and the LED will be off.

An example program which reads and checks the diagnostic codes from RBUF is included in Section 3.4.1.

3.3.10.2 Interpretation of Self-Test Codes – All self-test codes in RBUF will have the top four bits set. Bits <11:8> indicate the sequence of the diagnostic byte. That is to say, 0 = first byte, 1 = second byte, and so on.

Figure 3-2 shows how the diagnostic code in the low byte of RBUF should be interpreted. Table 3-3 gives the meaning of each implemented diagnostic byte.

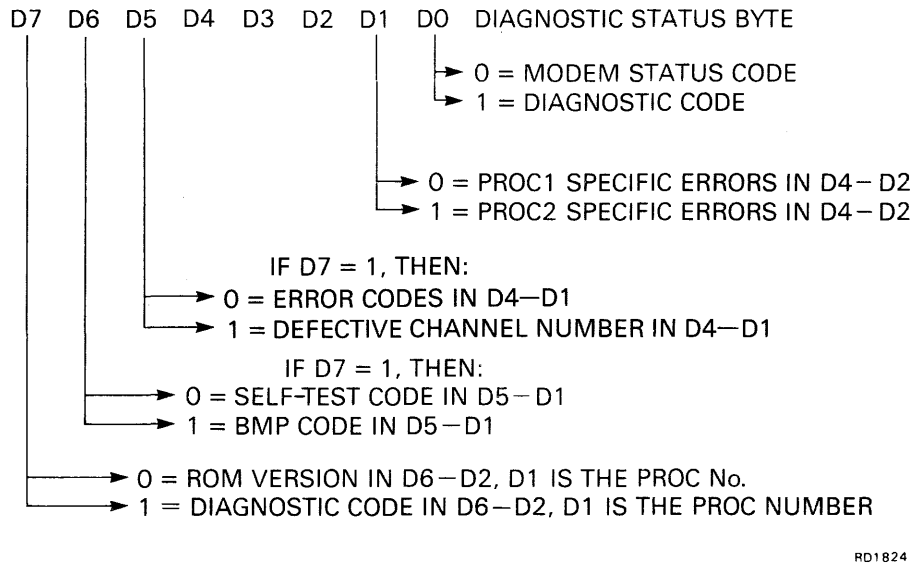


Figure 3-2 Diagnostic/Status Byte

Table 3-3 DHU11 Self Test Error Codes

Code (Octal)	Test
201	Self-test null code (used as a filler)
203	Self-test skipped
205	Interprocessor link error detected by PROC1
207	Interprocessor link error detected by PROC2
211	Basic data-path error from PROC2
213	Undefined UART error
215	Transmit-character-FIFO logic error
217	Received-character-FIFO logic error
225	PROC1 to common RAM error
227	PROC2 to common RAM error
231	PROC1 internal RAM error
233	PROC2 internal RAM error
235	PROC1 ROM CRC error
237	PROC2 ROM CRC error

The odd numbers from 241_8 to 277_8 indicate a UART access or function error on the channel indicated by D4 to D1.

If D7 = 0, the ROM version number is in D6 to D2.

D1 = PROC number (0 = PROC1, 1 = PROC2)

NOTE

Codes not shown in this table indicate undefined errors.

After self-test, the eight codes in the RX FIFO will consist of six diagnostic codes and two ROM version codes.

After an error-free test, six 201 codes and two ROM version codes will be returned.

If self-test is skipped (see next section), six 203 codes and two ROM version codes will be returned.

3.3.10.3 Skipping Self-Test – Self-test takes up to 2.5 seconds to complete. Depending on system software, this may cause a 2.5 second hang-up. The 'skip self-test' facility allows the program to bypass the self-test diagnostic.

There are two methods of skipping self-test.

- DHV11 compatible method
- DHU11 (direct) method

The DHV11 compatible method is as follows.

1. The program resets the DHU11.

2. The diagnostic firmware writes 125252_8 throughout the common RAM within eight milliseconds of reset.

3. The program waits 10 ms (+ or – 1 ms) after issuing reset. It then writes 052525_8 throughout the control registers (LPR, LNCTRL, TBUFFAD1, TBUFFAD2, and TBUFFCT) for lines 0 to 7, within the next 4 ms.

4. The diagnostic firmware waits until 16 ms after reset. It then checks for a 052525_8 code in common RAM.

   If it finds the code, self-test is skipped. The DIAG.FAIL bit is cleared and control is passed to the communications firmware which begins initialization.

   If the code is not found, self-test begins.

NOTE

The program must not write to the CSR or the control registers during the period starting 15 ms after reset and ending when the MASTER.RESET bit is cleared. This could cause a diagnostic fail condition.

The direct method is to set SKIP (CSR bit 4) and MASTER.RESET (CSR bit 5) at the same time. That is to say, write 60_8 to the base CSR. SKIP must not be cleared until at least 20 microseconds after it is set. SKIP must be cleared by the host to enable the communications firmware to complete the master reset sequence.

3.3.10.4 Background Monitor Program (BMP) – When not busy with other tasks, the DHU11's microcomputers perform background tests on the option. This is done by checking the timer-generated interrupts used by the firmware (one interrupt in PROC1 and two in PROC2). One of two codes is loaded into the RX FIFO.

- 305_8 – DHU11 running
- 307_8 – DHU11 defective

A single diagnostic word is returned via the FIFO. The low byte contains the diagnostic code. In the high byte OVERRUN.ERR, FRAME.ERR, and PARITY.ERR are all set to indicate that bits<7:0> do not hold a normal character. The line number (RBUF<11:8>) = 0.

If PROC2 stops running, PROC1 will set DIAG.FAIL and will turn off the LED. The LED will stay off, even if the fault clears. If PROC1 stops running, PROC2 will load a 307 code into the FIFO.

Normally, the BMP will only report when it finds an error. However, if the host suspects that the DHU11 is dead, it can obtain a BMP report at any time. This is done by setting DIAG (LPR <2:1>) of any channel, to 01. The line number returned is that of the LPR used to request the report.

On completion of the check, the BMP will clear the 01 code in DIAG. The host should not write to the LPR of that channel until DIAG has been cleared.

NOTE

If an error clears and then recurs, the BMP error code will be placed in the RX FIFO each time the error occurs.

3.4 PROGRAMMING EXAMPLES

This section contains programming examples. They are not presented as the only method of driving the option. These programs are not guaranteed or supported.

3.4.1 Resetting the DHU11

In the following example:

- DIAG is a routine to check the diagnostic codes. It returns with CARRY set if it detects an error code (see Section 3.3.10).
- The loop at 1$ can take up to 2.5 seconds, so the programmer could poll via a timer or poll at interrupt level zero.

```
;
; A ROUTINE TO RESET THE DHU11 AND CHECK THAT IT IS FUNCTIONING
; CORRECTLY.
;

DHURES::
        MOV     #40,@#DHUCSR            ; SET MASTER.RESET AND
                                        ; CLEAR INTERRUPT ENABLES.
1$:     BIT     #40,@#DHUCSR            ; WAIT FOR MASTER.RESET TO
        BNE     1$                      ; CLEAR.
        BIT     #20000,@#DHUCSR         ; CHECK THE DIAGNOSTICS FAIL
        BNE     DIAGER                  ; BIT.
                                        ; NOTE:TEST INSTRUCTION IS
                                        ; OK BECAUSE THERE ARE
                                        ; NO TX.ACTS PENDING.
        MOV     #8.,R5                  ; SET UP A COUNT
                                        ;
2$:     MOV     @#RBUFF,R0              ; GET NEXT DIAGNOSTIC CODE.
        JSR     PC,DIAG                 ; PROCESS IT.
        BCS     DIAGER                  ; CARRY SET - MUST HAVE BEEN
                                        ; AN ERROR.
```

```
        SOB     R5,2$                   ; GO BACK FOR NEXT CODE.

        RTS     PC                      ; RETURN - CARD IS RESET.

;
; DHU11 HAS FAILED TO RESET PROPERLY, SO HALT AND WAIT FOR
; THE FIELD SERVICE ENGINEER.
;

DIAGER: HALT
        BR      DIAGER
```

3.4.2 Configuration

This routine sets the characteristics of channel 1 as follows.

1. Transmit and receive at 300 bits/s
2. Seven data bits with even parity and one stop bit
3. Transmitters and receivers enabled
4. No modem control
5. No automatic flow control.

```
SETUP::
        MOV     #1,@#DHUCSR             ; LOAD INDEX REG
                                        ; WITH CHANNEL NO.
        MOV     #Ø52560,@#LPR           ; DATA RATE, STOP BITS,
                                        ; PARITY AND LENGTH
        MOV     #4,@#LNCTRL             ; ENABLE THE RECEIVER.
        MOVB    #2ØØ,@#TBFAD2+1         ; ENABLE THE TRANSMITTER.

        RTS     PC                      ; RETURN - CHANNEL 1 DONE.
```

3.4.3 Transmitting

3.4.3.1 Programmed Transfer – The following is a program to send a message on channel 1.

The CSR is polled for TX Action reports, but a TX.ACTION interrupt could also be used.

This program functions on a DHU11 with only this channel active. If other channels were active, this program would lose TX Action reports for them. A program to control all channels would be too big to use as an example.

```
;
; A ROUTINE TO WRITE A MESSAGE TO CHANNEL 1 USING FIFO OUTPUT
; MODE (PROGRAMMED TRANSFERS).
;

FIFOUT::
        MOV     #1,@#DHUCSR             ; POINT TO CHANNEL WE WISH
                                        ; TO TALK TO.
        MOV     #MESS,RØ                ; POINT TO MESSAGE.
        MOV     #MESIZE,R1              ; PUT COUNT IN
1$:
        TSTB    @#FIFOSIZE              ; CHECK THAT THERE IS SPACE IN
        BEQ     1$                      ; THE FIFO.
        MOVB    (RØ)+,@#FIFODATA        ; MOVE CHARACTER TO TRANSMIT FIFO
        SOB     R1,1$                   ; GO BACK FOR NEXT CHARACTER.
```

```
2$:
        MOV     @#DHUCSR,R2             ; WAIT FOR TX.ACT
        BPL     2$

        BIC     #170377,R2              ; ISOLATE CHANNEL NUMBER.
        CMP     #000400,R2
        BNE     2$                      ; IGNORE THE TX.ACT IF ITS
                                        ; NOT OURS (SHOULDN'T HAPPEN)

        RTS     PC                      ; MESSAGE SENT.

MESS:   .ASCII  /A TRANSMIT FIFO MESSAGE FOR CHANNEL 1/
MESIZE  =       .-MESS
        .EVEN
```

3.4.3.2 DMA Transfer –

```
;
; THIS PROGRAM SENDS A MESSAGE OUT ON EACH LINE OF THE DHU11 AND
; HALTS THE MACHINE WHEN ALL TRANSMISSIONS HAVE COMPLETED.
;
; THE MESSAGES ARE TRANSMITTED USING DMA MODE, AND INTERRUPTS ARE
; USED TO SIGNAL TRANSMISSION COMPLETION.
;

DMAINT::
        MOV     #TXINT,@#TXVECT         ; SET UP THE INTERRUPT VECTORS.
        MOV     #240,@#TXPSW            ; INTERRUPT PRIORITY FIVE.

        MOV     #16.,R0                 ; SIXTEEN LINES TO START.
        CLR     R1                      ; START AT LINE ZERO.
1$:
        MOVB    R1,@#DHUCSR             ; SELECT THE REGISTER BANK.
        MOV     #DMASIZ,@#TBFCNT        ; SET LENGTH OF MESSAGE.
        MOV     #DMAMES,@#TBFAD1        ; SET LOWER 16 ADDRESS BITS.
        MOV     #100200,@#TBFAD2        ; START DMA WITH TRANSMITTER
                                        ; ENABLED (ASSUME UPPER ADDRESS
                                        ; BITS ARE ZERO).
        INC     R1                      ; POINT TO NEXT CHANNEL.
        SOB     R0,1$                   ; REPEAT FOR ALL LINES.

        CLR     R5                      ; R5 IS USED BY INTERRUPT ROUTINE.
        MOVB    #100,@#DHUCSR+1         ; ENABLE TRANSMITTER INTERRUPTS.
2$:
        CMP     #16.,R5                 ; WAIT FOR ALL LINES TO FINISH.
        BNE     2$
3$:
        HALT                            ; ALL DONE, SO STOP.
        BR      3$

;
; TRANSMITTER INTERRUPT ROUTINE.
;
; R5 IS INCREMENTED AS EACH LINE COMPLETES.
;

TXINT::
        MOV     @#DHUCSR,R0     ; GET LINE NUMBER OF FINISHED LINE.
        BIT     #100000,R0      ; CHECK FOR (ANOTHER) TX.ACTION.
        BEQ     4$              ; IF NOT, GO RETURN AND WAIT.
```

```
        BIT     #Ø1ØØØØ,RØ     ; CHECK FOR DMA FAILURE.
        BNE     5$              ; GO HALT - MEMORY PROBLEM.

        INC     R5              ; FLAG THAT ANOTHER LINE HAS FINISHED.
        BR      TXINT
4$:
        RTI
5$:
        HALT                    ; MEMORY PROBLEM
        BR      5$

DMAMES: .ASCII  <15><12><7><7><7>/SYSTEM CLOSING DOWN NOW/
DMASIZ  =       .-DMAMES
        .EVEN
```

3.4.3.3 Aborting a Transmission –

```
;
; THIS ROUTINE IS CALLED TO ABORT A TRANSMISSION (EITHER DMA OR FIFO) IN
; PROGRESS ON A SPECIFIED LINE.  THIS ROUTINE MAKES THE (RATHER RASH)
; ASSUMPTION THAT THERE ARE NO OTHER TRANSFERS IN PROGRESS.
;
; ON ENTRY, RØ CONTAINS THE NUMBER OF THE LINE TO BE ABORTED.
;

TXABRT::
        MOV     RØ,@#DHUCSR     ; POINT TO THE CHANNEL TO BE ABORTED.
        BIS     #1,@#LNCTRL     ; SET THE TRANSMIT ABORT BIT.
1$:
        MOV     @#DHUCSR,R1     ; WAIT FOR THE TX.ACT
        BPL     1$
        SWAB    R1              ; CHECK ITS OUR LINE.
        BIC     #177760,R1
        CMP     RØ,R1
        BNE     1$              ; IGNORE IT IF ITS NOT (OUR
                                ; ASSUMPTION WAS WRONG!)

        BIC     #1,@#LNCTRL     ; CLEAR DOWN THE ABORT FLAG
                                ; FOR NEXT TIME.

        RTS     PC              ; BUFFER COMPLETELY ABORTED,
                                ; IF A DMA WAS IN PROGRESS, THE
                                ; DMA REGISTERS REFLECT WHERE
                                ; THE DHU11 HAD GOT TO.
```

3.4.4 Receiving

```
;
; THIS ROUTINE PROCESSES RECEIVED CHARACTERS UNDER INTERRUPT CONTROL.
; IF AN XOFF IS RECEIVED, THE TRANSMITTER FOR THAT CHANNEL IS TURNED
; OFF. IF AN XON IS RECEIVED, THE TRANSMITTER IS TURNED BACK ON.  ALL
; OTHER CHARACTERS ARE IGNORED.
;
; THIS IS JUST AN EXAMPLE, A BETTER WAY TO PERFORM FLOW CONTROL IS TO
; USE THE AUTOMATIC CAPABILITIES OF THE DHU11.
;

RXAUTO::
        MOV     #RXINT,@#RXVECT     ; SET UP THE INTERRUPT VECTORS.
        MOV     #240,@#RXPSW        ; PRIORITY LEVEL FIVE.
```

```
        MOV     #16.,R0                 ; ENABLE ALL THE RECEIVERS,
        CLR     R1                      ; STARTING AT CHANNEL ZERO,
1$:
        MOVB    R1,@#DHUCSR             ; SELECT THE LINE.
        BIS     #4,@#LNCTRL             ; ENABLE THIS RECEIVER.
        INC     R1                      ; SET POINTER TO NEXT CHANNEL.
        SOB     R0,1$

        MOVB    #0,@#DHUCSR             ; SELECT CHANNEL ZERO.
        MOV     #20.,@#RXTIMR           ; SET DELAY TO 20MS.

        MOVB    #100,@#DHUCSR           ; ENABLE THE RECEIVER INTERRUPTS.

        RTS     PC                      ; RETURN - INTERRUPTS DO THE RESET.

;
; INTERRUPT ROUTINE TO DO THE MAIN TASK.
;

RXINT::
        MOV     R0,-(SP)            ; SAVE CALLERS REGISTERS.
RXNXTC:
        MOV     @#RBUFF,R0          ; GET THE CHARACTER.
        BPL     RXIEND              ; IF NO DATA VALID, WE'VE FINISHED.
        MOV     R0,-(SP)            ; CHECK FOR ERRORS, MODEM AND
        BIC     #107777,(SP)+       ; DIAGNOSTICS CODES.
        BNE     RXNXTC              ;  - JUST IGNORE THEM (BAD PRACTICE).

        BIC     #170200,R0          ; REMOVE UNNECESSARY BITS.
        SWAB    R0                  ; POINT TO THIS CHARACTERS LINE.
        BIS     #100,R0             ; (ADD THE INTERRUPT ENABLE BIT.)
        MOVB    R0,@#DHUCSR
        SWAB    R0                  ; PUT CHARACTER BACK IN LOWER BYTE.
        CMPB    #21,R0              ; WAS IT AN "XON"?
        BNE     1$                  ; NO - GO CHECK FOR AN "XOFF"

        BISB    #200,@#TBFAD2+1     ; ENABLE THE TRANSMITTER.
        BR      RXNXTC              ; GO CHECK FOR MORE CHARACTERS.
1$:
        CMPB    #23,R0              ; WAS IT AN "XOFF"?
        BNE     RXNXTC              ; NO - GO CHECK FOR MORE CHARACTERS.

        BICB    #200,@#TBFAD2+1     ; DISABLE THE TRANSMITTER.
        BR      RXNXTC              ; GO CHECK FOR MORE CHARACTERS.

RXIEND:
        MOV     (SP)+,R0            ; RESTORE THE DESTROYED REGISTER.
        RTI
```

3.4.5 Auto XON and XOFF

```
;
; THIS PROGRAM SENDS A MESSAGE OUT ON EACH LINE OF THE DHU11 AND
; HALTS THE MACHINE WHEN ALL TRANSMISSIONS HAVE COMPLETED.
;
; THE MESSAGES ARE TRANSMITTED USING DMA MODE, AND INTERRUPTS ARE
; USED TO SIGNAL TRANSMISSION COMPLETION.
;
; AUTOMATIC FLOW CONTROL IS ENABLED ON THE OUTGOING DATA.
;
```

```
TXAUTO::
        MOV     #ATOINT,@#TXVECT        ; SET UP THE INTERRUPT VECTORS.
        MOV     #240,@#TXPSW            ; INTERRUPT PRIORITY FIVE.

        MOV     #16.,R0                 ; SIXTEEN LINES TO START.
        CLR     R1                      ; START AT LINE ZERO.
1$:
        MOVB    R1,@#DHUCSR             ; SELECT THE REGISTER BANK.
        BIS     #24,@#LNCTRL            ; ENABLE AUTOMATIC FLOW CONTROL
                                        ; ON THE TRANSMITTED DATA.
        MOV     #AUTOSZ,@#TBFCNT        ; SET LENGTH OF MESSAGE.
        MOV     #AUTOMS,@#TBFAD1        ; SET LOWER 16 ADDRESS BITS.
        MOV     #100200,@#TBFAD2        ; START DMA WITH TRANSMITTER
                                        ; ENABLED (ASSUME UPPER ADDRESS
                                        ; BITS ARE ZERO).
        INC     R1                      ; POINT TO NEXT CHANNEL.
        SOB     R0,1$                   ; REPEAT FOR ALL LINES.

        CLR     R5                      ; R5 IS USED BY INTERRUPT ROUTINE.
        MOVB    #100,@#DHUCSR+1         ; ENABLE TRANSMITTER INTERRUPTS.
2$:
        CMP     #16.,R5                 ; WAIT FOR ALL LINES TO FINISH.
        BNE     2$
3$:
        HALT                            ; ALL DONE, SO STOP.
        BR      3$

;
; TRANSMITTER INTERRUPT ROUTINE.
;
; R5 IS INCREMENTED AS EACH LINE COMPLETES.
;

ATOINT::
        MOV     @#DHUCSR,R0     ; GET LINE NUMBER OF FINISHED LINE.
        BPL     2$              ; GO RETURN IF NO MORE TX.ACTIONS.
        BIT     #10000,R0       ; CHECK FOR DMA FAILURE.
        BNE     4$              ; GO HALT - MEMORY PROBLEM.

        INC     R5              ; FLAG THAT ANOTHER LINE HAS FINISHED.
        BR ATOINT               ; CHECK FOR MORE TX.ACTIONS.
2$:
        RTI
4$:
        HALT                    ; MEMORY PROBLEM
        BR      4$

AUTOMS: .ASCII  <15><12><7><7><7>/SYSTEM CLOSING DOWN NOW/
AUTOSZ  =       .-AUTOMS
        .EVEN
```

3.4.6 Checking Diagnostic Codes

```
;
; THIS ROUTINE CHECKS THE DIAGNOSTICS CODES RETURNED FROM THE DHU11.
;
; ON ENTRY, R0 CONTAINS THE CHARACTER RECEIVED FROM THE DHU11.
;
; ON EXIT, THE CARRY BIT WILL BE CLEAR FOR SUCCESS, SET FOR FAILURE.
;
```

```
DIAG::
        MOV     R0,-(SP)                ; SAVE THE CODE FOR LATER.

        BIC     #107776,R0              ; CHECK THAT IT'S A DIAG. CODE.
        CMP     #070001,R0
        BNE     DIAGEX                  ; IF NOT, JUST EXIT NORMALLY.

        MOV     (SP),R0                 ; GET THE CODE BACK.

        BITB    #200,R0                 ; CHECK FOR ROM VERSION NUMBER.
        BEQ     DIAGEX
        CMPB    #201,R0                 ; SELF TEST NULL CODE.
        BEQ     DIAGEX
        CMPB    #203,R0                 ; SELF TEST SKIPPED CODE.
        BEQ     DIAGEX
        CMPB    #305,R0                 ; DHU RUNNING CODE.
        BEQ     DIAGEX
                                        ; ALL THE REST ARE ERROR CODES.

        SEC                             ; AN ERROR CODE WAS RECEIVED, SO
        BR      DIAGXX                  ; SET THE CARRY FLAG.

DIAGEX:
        CLC                             ; EVERYTHING OK, SO CLEAR CARRY.
DIAGXX:
        MOV     (SP)+,R0                ; RESTORE THE CHARACTER/INFO.
        RTS     PC
```

3.4.7 Modem Control

```
;
; THIS ROUTINE WILL ANSWER A MODEM CALL, PRINT OUT A MESSAGE AND
; HANG UP THE PHONE.
;
; DMA MODE IS USED.  IF FIFO OUTPUT MODE WERE USED, THEN THE
; MESSAGE WOULD NEED TO BE PADDED OUT WITH TWO NULLS DUE TO
; INTERNAL BUFFERING OF THE DHU11.
;

MODEM::
        MOV     #16.,R0                 ; SET UP ALL CHANNELS FOR MODEMS.
        CLR     R1
1$:
        MOVB    R1,@#DHUCSR             ; POINT TO CHANNEL TO BE SET UP.
        MOVB    #125,@#LPR+1            ; 300 BPS DATA RATE.
        MOV     #400,@#LNCTRL           ; SET MODEM  DISABLE RECEIVER.
        INC     R1                      ; POINT TO NEXT CHANNEL.
        SOB     R0,1$                   ; SET UP ALL CHANNELS.

        MOV     #MRXINT,@#RXVECT        ; SET UP INTERRUPT VECTORS.
        MOV     #240,@#RXPSW            ; (INTERRUPT LEVEL FIVE)
        MOV     #MTXINT,@#TXVECT
        MOV     #240,@#TXPSW
        MOV     #40100,@#DHUCSR         ; ENABLE THE INTERRUPTS.
2$:
        BR      2$                      ; LET INTERRUPT ROUTINES DO
                                          EVERYTHING

;
; TRANSMITTER INTERRUPT ROUTINE.
;
```

```
MTXINT:
        MOV     R0,-(SP)                ; SAVE THE REGISTER WE USE.
1$:
        MOV     @#DHUCSR,R0             ; GET INTERRUPTING LINE NUMBER.
        BPL     2$                      ; GO RETURN IF NO MORE TX.ACTIONS.
        SWAB    R0                      ; SELECT THIS CHANNELS REGISTERS.
        BIC     #177760,R0
        BIS     #100,R0                 ; (RETAIN INTERRUPT ENABLE)
        MOVB    R0,@#DHUCSR
        MOV     #400,@#LNCTRL           ; DROP DTR, RTS AND CLEAR ABORT.
        BR      1$                      ; CHECK FOR MORE TX.ACTIONS.
2$:
        MOV     (SP)+,R0                ; RESTORE THE REGISTER WE USED.
        RTI

;
; RECEIVER INTERRUPT ROUTINE.
;

MRXINT::
        MOV     R0,-(SP)          ; SAVE THE REGISTER WE USE.
MRXLOP:
        MOV     @#RBUFF,R0        ; GET INTERRUPTING LINE.
        BPL     MRXEND            ; EXIT IF ALL DONE.
        MOV     R0,-(SP)          ; SAVE FOR LATER USE.
        BIC     #107776,R0        ; TEST FOR MODEM INFO.
        CMP     #070000,R0
        BNE     MRXNXT            ; SKIP IF NOT.
        MOV     (SP),R0           ; SELECT REGISTERS FOR THIS LINE.
        SWAB    R0
        BIC     #177760,R0
        BIS     #100,R0           ; (RETAIN INTERRUPT ENABLE)
        MOVB    R0,@#DHUCSR

        MOV     (SP),R0           ; CHECK FOR READY FOR TRANSMISSION.
        BIC     #177547,R0
        CMP     #230,R0
        BNE     1$                ; DSR, DCD  CTS NOT SET, TRY START.
        BIC     #1,@#LNCTRL       ; CLEAR DOWN ABORT BIT (IN CASE WE
                                  ; SET IT WITHOUT A DMA IN PROGRESS).
        MOVB    #23,@#LNCTRL+1    ; ASSERT RTS IN CASE CTS AND DSR
                                  ; WERE ASSERTED AT THE SAME TIME.
        MOV     #NOSYSZ,@#TBFCNT  ; OUTPUT MESSAGE.
        MOV     #NOSYS,@#TBFAD1   ; (TRANSMITTER INTERRUPT ROUTINE
        MOV     #100200,@#TBFAD2  ;  CLEARS DOWN THE CALL.)
        BR      MRXNXT            ; GO LOOK FOR MORE.
1$:
        BIT     #200,R0           ; CHECK FOR DSR.
        BEQ     2$                ; NO - GO CHECK FOR NEW CALL.
        MOVB    #23,@#LNCTRL+1    ; ASSERT RTS.
        BR      MRXNXT            ; GO LOOK FOR MORE.
2$:
        BIT     #40,(SP)          ; CHECK FOR RING INDICATOR.
        BEQ     3$                ; NO - GO CLOSEDOWN CALL.
        MOVB    #3,@#LNCTRL+1     ; ASSERT DTR.
        BR      MRXNXT            ; GO LOOK FOR MORE.
3$:
        BISB    #1,@#LNCTRL       ; ABORT ANY CURRENT DMA TRANSFERS.
        MOVB    #1,@#LNCTRL+1     ; DROP MODEM SIGNALS.
```

```
MRXNXT:
        TST     (SP)+           ; REMOVE SIGNALS FROM THE STACK.
        BR      MRXLOP          ; GO ROUND AGAIN.
MRXEND:
        MOV     (SP)+,RØ        ; RESTORE THE REGISTER WE USED.
        RTI

NOSYS:  .ASCII  <15><12><7><7><7>/SYSTEM UNAVAILABLE, PLEASE TRY LATER/
NOSYSZ  =       .-NOSYS
        .EVEN
```

CHAPTER 4
MAINTENANCE

4.1 SCOPE

This chapter explains the maintenance strategy and how the diagnostic programs are used to find a defective field replaceable unit (FRU). The description is supplemented by troubleshooting flowcharts.

4.2 MAINTENANCE STRATEGY

4.2.1 Preventive Maintenance

No preventive maintenance is planned for this option. However, if the host system is being serviced, a visual check should be made for loose connectors and damaged cables.

4.2.2 Corrective Maintenance

The M3105 module, BC05L-xx cables, and distribution panels are all FRUs. Corrective maintenance is therefore based on finding and replacing the defective FRU. However, if the fault is not in the option, it may be possible to perform tests of external equipment. Figure 4-1 can be used as a basis for troubleshooting.

Flowcharts 4-2 and 4-4 provide recommended test sequences for PDP-11 and VAX systems respectively.

4.3 INTERNAL DIAGNOSTICS

Internal diagnostics run without intervention from the operator. There are two tests, called self-test and background monitor program.

4.3.1 Self-Test

This test starts immediately after bus or device reset. It checks the internally accessible parts of the DHU11 and gives a GO/NOGO indication via the CSR<DIAG.FAIL> bit and the 'diagnostics passed' LED. Self-test also reports error or status information to the host via the RX FIFO. This information is used by system-based diagnostics.

During a successful (no defects) self-test, the LED flashes OFF/ON/OFF before coming ON permanently. The first OFF period is very short and may not be seen. However, if the LED goes OFF and then comes ON permanently, the diagnostic has found no faults. If self-test is skipped (see Chapter 3, Section 3.3.10.3), the LED will flash OFF and then come ON permanently.

Because of the limitations of self-test, a correct sequence does not guarantee that all sections of the module are good.

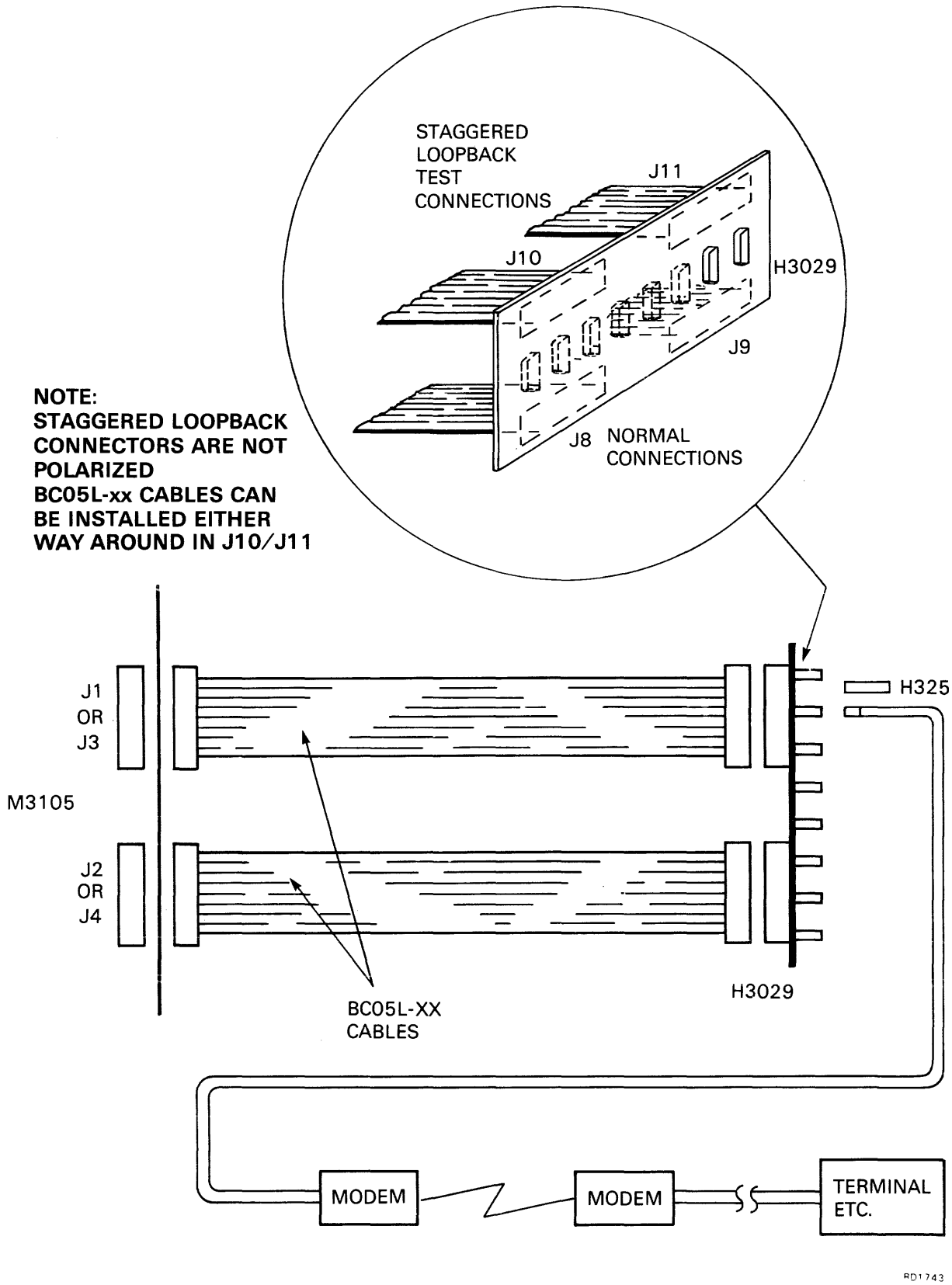


Figure 4-1 Troubleshooting Connection Diagram

4.3.2 Background Monitor Program (BMP)

The BMP performs limited tests of the DHU11 when the option is not engaged in other tasks. If it detects an error, the BMP reports to the host via the RX FIFO. It also switches off the 'diagnostics passed' LED.

By writing codes to the LPR, the host can cause the BMP to report the DHU11 status even if an error has not been detected. It is used if the host suspects that the DHU11 is defective.

NOTE

A full description of self-test and BMP diagnostic codes is provided in Chapter 3, Section 3.3.10.

4.4 XXDP+ DIAGNOSTICS

In order to run these diagnostics, the host PDP-11 system must have at least the minimum configuration specified. Loopback connectors will be needed for some of the tests. For more information, refer to the program documentation at the beginning of the ZDHU??, ZDHV??, ZDHW??, and ZDHX?? listings.

4.4.1 ZDHU??, ZDHV??, ZDHW??, and ZDHX??

These programs form a functional verification test (FVT) which runs on UNIBUS members of the PDP-11 processor family. The test runs under the PDP-11 Diagnostic Supervisor.

The minimum system requirements are:

- UNIBUS CPU
- 32K bytes memory
- Console terminal
- XXDP+ load device with Diagnostic Runtime Services
- DHU11 option.

In order to test the full DMA address capability of the DHU11, the diagnostic uses the following address patterns. If the high address lines are to be tested, the host must have memory at the following locations as well as the 32K bytes defined in the previous paragraph.

Address bits	17	16	15	14	13	...	...
Memory address (High bank)	1	0	1	x	x	x	x
Memory address (Low bank)	0	1	0	x	x	x	x

If memory is not available at these locations, some high DMA address bits will not be tested. This will not be considered as an error. The operator, by answering a prompt, can display information specifying the bits which were tested.

The ZDHU?? diagnostic has no loopback mode. ZDHV??, ZDHW??, and ZDHX?? function in the following modes.

1. Internal loopback
2. Staggered loopback
3. External (H325) loopback

In addition to the above, ZDHX?? has two extra modes.

4. Modem loopback
5. Keyboard echo

In modem-loopback mode the modem must be set up manually. The diagnostic will test to where the line is looped back.

In keyboard-echo mode, received data is retransmitted. This allows the input from a terminal keyboard to be displayed on a terminal. Modem control signals are permanently set so that modem links can also be tested.

Each mode can be selected by answering a prompt from the diagnostic program. Example printouts, together with a summary of the use of the diagnostic supervisor, are provided in Section 4.5.

A troubleshooting flowchart is provided in Figure 4-2.

4.4.1.1 Functions of ZDHU?? – This program checks the reset, skip self-test, and the register-access functions. It checks the TX-enable function, bus requests, and interrupts. CSR and RXFIFO reports from the self-test and BMP are also checked. Loopback connectors are not needed for this test.

4.4.1.2 Functions of ZDHV?? – This program checks the operation of the RX-interrupt timer and the register bits which control the flow of data and the operation of the FIFOs. A staggered loopback connector is needed for some of these tests.

4.4.1.3 Functions of ZDHW?? – This program verifies the correct operation of the modem control-and-status lines, and checks that there is no unwanted interaction between them. The tests will only run if one of the external loopback modes is selected.

4.4.1.4 Functions of ZDHX?? – This program checks DMA transfers and addressing, split-speed operation, and the reporting of data errors. Modem loopback and keyboard echo tests can be selected. ZDHX?? performs extensive data-transfer checks. One of the external loopback modes should be selected.

NOTE

Each of these diagnostics verifies that the handshake between the DHU11 and the host is operating correctly.

4.4.2 DECX/11 Exerciser

When a DHU11 or other option is installed or replaced, it is necessary to run the DECX/11 exerciser XDHU??. The exerciser must first be configured to match the host system. For more information, refer to the DECX/11 User Manual (AC-FO35B-MC) and DECX/11 Cross-Reference (AC-FO55C-MC).

DECX/11 should not be run until all modules have passed their own diagnostic tests. Therefore, before running the exerciser, the DHU11 must pass all phases of the FVT.

4.5 PDP-11 DIAGNOSTIC SERVICES SUMMARY

The FVT diagnostics have been written for use with the Diagnostic Runtime Services. DRS provides the interface between the operator and the diagnostic programs. By answering parameter questions when prompted, the operator can define the following.

1. The hardware configuration of the DHU11s being tested
2. The type of test information to be reported
3. The conditions under which the test should be terminated or continued.

4.5.1 Loading the Diagnostic

The diagnostic program may be loaded and started in the normal way, using any of the supported load systems. For example, using XXDP+, the program ZDHV??.BIN is loaded and started by typing R ZDHV??.

The diagnostic and the DRS will be loaded and the program started. The program types the following message.

```
DRS LOADED
DIAG.RUN-TIME SERVICES
CZDHV-B-0
DHU11 FUNCTIONAL VERIFICATION TEST
UNIT IS DHU11
RESTART ADDRESS xxxxxx
DR>
```

DR> is the prompt from the DRS. At this point a DRS command must be entered (supervisor commands are listed in Section 4.5.3).

B0 on the end of CZDHV indicates the revision level (B) and the patch level (0).

4.5.2 Four Steps to Run a DRS Diagnostic

1. Enter the start command.

   When the prompt DR> is issued, type:

   ```
   STA/PASS:1/FLAGS:HOE (RET)
   ```

   The switches and flags are optional.

2. Answer the hardware parameter questions.

   The program prompts with:

   ```
   CHANGE HW?
   ```

   You must answer Y to this query if you want to change the hardware parameter tables. The program will then ask a number of hardware parameter questions in sequence. For example, the first question is:

   ```
   # UNITS?
   ```

At this point, enter the number of units to be tested.

NOTE

Some versions of the DRS do not ask the CHANGE HW? question at the first start command. Instead they go straight into the hardware parameter question sequence.

The answers to the questions are used to build hardware parameter tables (P-tables) in memory. A series of questions is posed for each device to be tested. A hardware P-table is built for each device.

3. Answer the software parameter questions.

   When all the hardware P-tables are built the program responds with:

   CHANGE SW?

   If other than default parameters are wanted for the software, type Y. If the default parameters are wanted, type N.

   If you type Y, a series of software questions will be asked and the answers to these will be entered into the software P-table in memory. The software questions will be asked only once, regardless of the number of units to be tested.

4. Diagnostic execution

   After the software questions have been answered, the diagnostic starts to run.

   What happens next is determined by the switch options selected with the start command, or errors occurring during execution of the diagnostic.

4.5.3 DRS Commands

The DRS commands that may be issued in response to the DR> prompt are as follows.

- START — Starts a diagnostic program.
- RESTART — When a diagnostic has stopped and control is given back to DRS, this command restarts the program from the beginning.
- CONTINUE — Allows a diagnostic to continue running from where it was stopped.
- PROCEED — Causes the diagnostic to resume with the next test after the one in which it halted.
- EXIT — Transfers control to the XXDP+ monitor.
- DROP — Drops units specified until an ADD or START command is given.
- ADD — Adds units specified. These units must have previously been dropped.
- DISPLAY — Displays P-Tables.

- FLAGS Used to change flags.
- ZFLAGS Clears flags.

All of the DRS commands except EXIT, DISPLAY, FLAGS, and ZFLAGS can be used with switch options.

4.5.3.1 Command Switches – Switch options may be used with most DRS commands. The available switches and their functions are as follows.

- /TESTS: Used to specify the tests to be run (the default is all tests). An example of the tests switch used with the start command to run tests 1 to 5, 19, and 34 to 38 would be:

  DR> START/TESTS:1-5:19:34-38 RET

- /PASS: Used to specify the number of passes for the diagnostic to run. For example:

  DR> START/PASS:1 RET

  In this example, the diagnostic would complete one pass and give control back to the DRS.

- /EOP: Used to specify how many passes of the diagnostic will occur before the end-of-pass message is printed (the default is one).

- /UNITS: Used to specify the units to be run. This switch is valid only if N was entered in response to the CHANGE HW? question.

- /FLAGS: Used to check for conditions and modify program execution accordingly. The conditions checked for are as follows.

  :HOE Halt on error (transfers control back to the supervisor)

  :LOE Loop on error

  :IER Inhibit error reports

  :IBE Inhibit basic error information

  :IXE Inhibit extended error information

  :PRI Print errors on line printer

  :PNT Print the number of the test being executed before execution

  :BOE Ring bell on error

  :UAM Run in unattended mode, bypass manual intervention tests

  :ISR Inhibit statistical reports

  :IOU Inhibit dropping of units by program.

4.5.4 Control Characters Supported

The keyboard functions supported by DRS are as follows.

- CTRL/C (^C) Returns control to the DRS. The DR> prompt would be typed in response to CTRL/C. This function can be typed at any time.
- CTRL/Z (^Z) Used during hardware or software dialogue to terminate the dialogue and select default values.
- CTRL/O (^O) Disables all printouts. This is valid only during a printout.
- CTRL/S (^S) Used during a printout to temporarily freeze the printout.
- CTRL/Q (^Q) Resumes a printout after a CTRL/S.

4.5.5 Example Printouts

Three examples of diagnostic printouts follow. The first is error-free. In the second test, the device address is incorrect but extended error reporting is not selected. In the third test, extended error reporting is selected.

If the answer to the software question 'EXTENDED ERROR REPORTING ?' is 'N' (or default), error reports will be 'TEST FAILED' only. For example:

'DMA-START BIT TEST FAILED' or 'RXTIMER TEST FAILED'

For more detailed reporting, the answer must be 'Y'.

Note that the question:

'NUMBER OF INDIVIDUAL ERRORS TO BE REPORTED ON A LINE ?'

will not be asked unless the previous answer was 'Y'.

Entries by the operator are underlined. An underline without an entry shows that the operator has pressed the RETURN key to select the default parameter.

1. Error-free pass

```
.R ZDHVBØ
ZDHVBØ.BIC

DRSDØ
CZDHV-B-Ø
DHU-11 FUNCT TEST PART2
UNIT IS DHU-11
RESTART ADDR: 147670

DR>STA/PAS:1

CHANGE HW (L) ? Y

# UNITS (D) ? 1

UNIT Ø
```

```
CSR ADDRESS: (Ø) 160460 ?_
INTERRUPT VECTOR ADDRESS: (Ø) 310 ?_
ACTIVE LINE BIT MAP: (Ø) 177777?_

TYPE OF LOOPBACK (1=INTERNAL, 2=H3Ø29 OR H3277): (Ø) 2 ?_

CHANGE SW (L) ? Y

REPORT UNIT NUMBER AS EACH UNIT IS TESTED: (L) Y ?_
EXTENDED ERROR REPORTING:  (L) N ?_

CZDHV EOP 1
    Ø TOTAL ERRORS

DR>
```

2. Test with wrong device address selected

```
DR>STA/PAS:1

CHANGE HW (L) ? Y

# UNITS (D) ? 1

UNIT Ø
CSR ADDRESS: (Ø) 160460 ? 160500
INTERRUPT VECTOR ADDRESS: (Ø) 310 ?_
ACTIVE LINE BIT MAP: (Ø) 177777 ?_
TYPE OF LOOPBACK (1=INTERNAL, 2S=H3Ø29 OR H3277): (Ø) 2 ?_

CHANGE SW (L) ? Y

REPORT UNIT NUMBER AS EACH UNIT IS TESTED: (L) Y ?_
EXTENDED ERROR REPORTING:  (L) N ?_

CZDHV DVC FTL ERROR ØØ1Ø1 ON UNIT ØØ TST ØØ1 SUB ØØØ PC: Ø21252
DEVICE REGISTER ACCESS ERRORS
 UNIT    Ø DROPPED FROM FURTHER TESTING

PASS ABRTD THS UNIT
CZDHV EOP  1
    1 TOTAL ERRORS

DR>
```

3. Wrong device address selected and extended error reporting enabled.

```
DR>STA/PAS:1

CHANGE HW (L)  ? Y

# UNITS (D)  ? 1

UNIT Ø
CSR ADDRESS:  (Ø)  160460 ? 160500
INTERRUPT VECTOR ADDRESS:  (Ø)  310 ?_
ACTIVE LINE BIT MAP:  (Ø)  177777 ? 10000
TYPE OF LOOPBACK (1=INTERNAL, 2=H3Ø29 OR H3277): (Ø)  2 ?_

CHANGE SW (L)  ? Y
```

```
REPORT UNIT NUMBER AS EACH UNIT IS TESTED:  (L) Y ?__
EXTENDED ERROR REPORTING:  (L) N ? Y
NUMBER OF INDIVIDUAL DATA ERRORS TO REPORT ON A LINE:  (D)  Ø ?__

CZDHV DVC FTL ERR  ØØ1Ø1 ON UNIT ØØ TST ØØ1 SUB ØØØ PC: Ø21252
DEVICE REGISTER ACCESS ERRORS
BUS TIME-OUT TRAP CAUSED BY READ ATTEMPT
BUS TIME-OUT TRAP CAUSED BY WRITE ATTEMPT
DHU MAY BE AT THE WRONG UNIBUS ADDRESS

 UNIT    Ø DROPPED FROM FURTHER TESTING

PASS ABRTD THS UNIT
CZDHV EOP   1
    1 TOTAL ERRS

DR>EXIT
```

4.6 VAX DIAGNOSTICS

VAX diagnostics for the DHU11 are:

EVDAI	–	Standalone diagnostic (level 3)
EVDAH	–	On-line diagnostic (level 2R)
UETP	–	User environmental test package (exerciser).

4.6.1 EVDAI Standalone Diagnostic

EVDAI is a comprehensive suite of functional verification tests. The tests run standalone under the VAX Diagnostic Supervisor (VDS) V6.13 or later. The diagnostic may be used:

- For installation tests
- For troubleshooting
- As a more comprehensive confidence check.

EVDAI has five modes of operation.

1. Internal loopback
2. External (H325) loopback
3. Staggered loopback
4. Modem loopback
5. Terminal echo

Modes 1, 2, and 3 are used to test the DHU11, whereas modes 4 and 5 are generally used to resolve line/modem/terminal faults or compatibility problems.

The format of the START command (Section 4.6.2.2) determines which tests are to be performed. A complete test in modes 1, 2, 3, or 4 takes about five minutes. Terminal echo runs until it is deselected.

The EVDAI diagnostic is supported by the off-line help facility EVDAI.HLP.

4.6.2 Running the EVDAI Standalone Diagnostic

The minimum hardware requirements for EVDAI are:

- Any VAX system with a UNIBUS
- A console terminal
- One to eight DHU11s.

An extra terminal would be needed to run the terminal echo test.

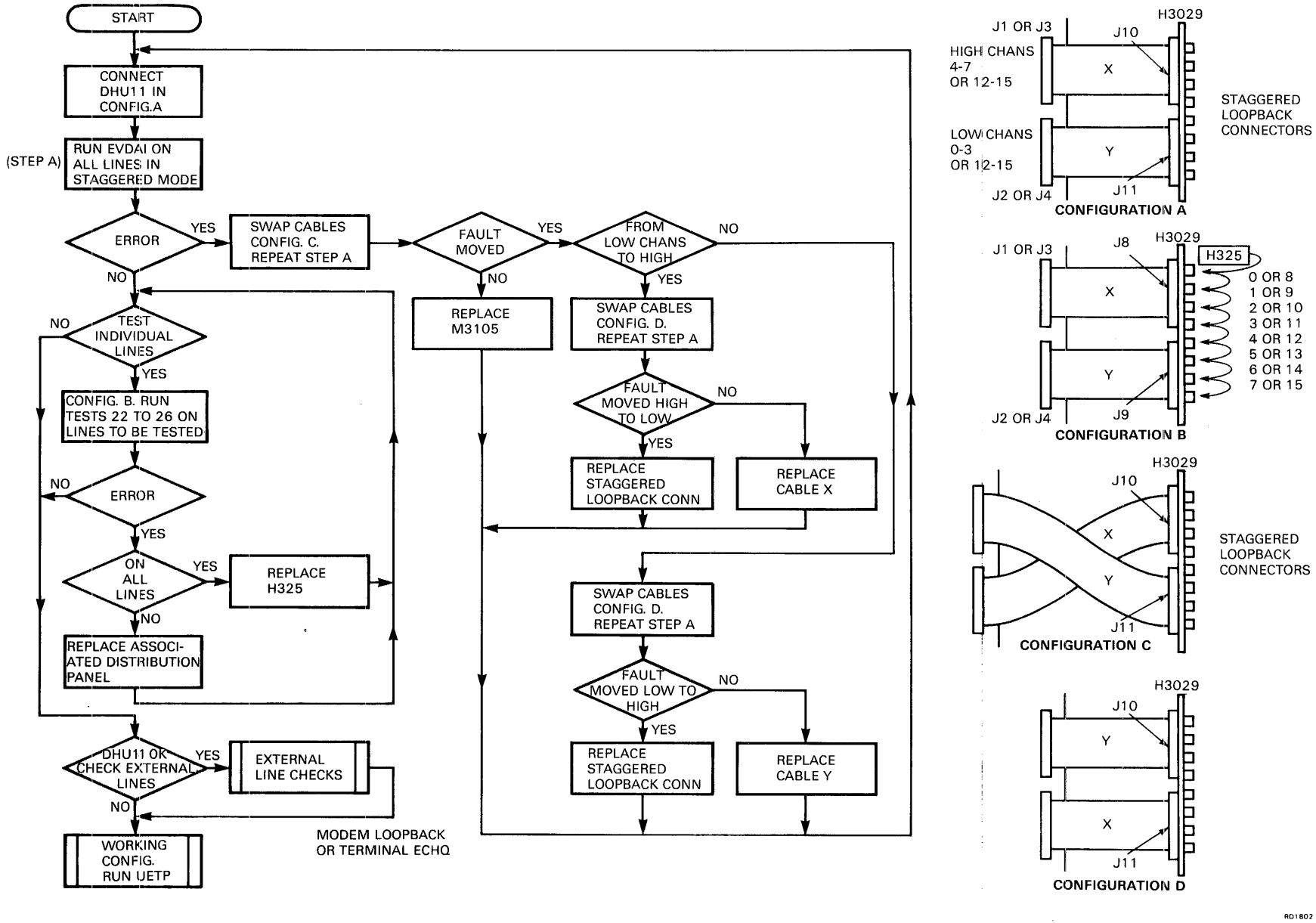


Figure 4-2 Troubleshooting Flowchart for XXDP+ Diagnostics

The VAX Diagnostic System User's Guide (EK-DS780-UG) provides instructions on how to load and run programs under the diagnostic supervisor. For details of the standalone tests, refer to the diagnostic listing ZZ-EVDAI.

4.6.2.1 Starting Up – Before EVDAI can be run, the diagnostic supervisor must be booted. The operator must then:

- Load EVDAI
- Attach the DHU11(s)
- Select the device(s) to be tested
- Start the diagnostic.

An example of how to attach the DHU11, and to load and run EVDAI follows. In the example, TRACE is set to cause all tests to be reported.

```
DIAGNOSTIC SUPERVISOR.  ZZ-ENSAA-Y6. 13-51Ø  8-FEB-1983 1Ø:47:Ø3

DS> LOAD EVDAI                    ; load the program

DS> SET TR,H                      ; set trace and halt on error

DS> ATTACH DHU11 DWØ TXA 76Ø46Ø 31Ø 5
```

- 5 — BR interrupt level (range 4 to 7)
- 31Ø — Vector address (range 000 to 770)
- 76Ø46Ø — The CSR address
- TXA — Name unit
- DWØ — The option is linked to UBA
- DHU11 — Device to be attached
- ATTACH — ATTACH command

```
DS> SEL TXA                       ; select the device for test
DS> ST                            ; start the diagnostic
```

4.6.2.2 Options – Once the program starts, the user will be asked to select a number of options.

a. Lines to be tested
b. Line speed
c. Type of loopback

In the following example, default values ALL and 4800 are selected for a and b. Staggered loopback mode is selected for c. The test starts to run when the type of loopback has been selected.

```
..  Program:  DHU11 - VAX Functional Verification Test,  revision
    1.Ø, 28 tests, at 1Ø:55:11.3Ø.
Testing: _TXA
lines to test [(ALL) or 1,2,...14,15]
Line Speed [(48ØØ),  5Ø,  75,  11Ø,   134.5,   15Ø,   3ØØ,   6ØØ,
  12ØØ,  18ØØ, 2ØØØ, 24ØØ, 7 2ØØ, 96ØØ, 192ØØ, 384ØØ]
loop type [(INTERNAL), EXTERNAL, STAGGERED, MODEM] STAGGERED

Test 1: Device Register Address Test
Test 2: Master Reset Selftest Test
Test 3: Master Reset Skip Selftest Test
Test 4: Diag Field (BMP) Test
Test 5: Selftest Forced Failure Test
Test 6: ROM Version Printout Test
Micro Processor number 1 ROM version is 1
```

```
Micro Processor number 2 ROM version is 1

Test 7: Register Address Test
Test 8: Id Bit Test
Test 9: Tx Enable Action
Test 10: Rx Data Available/Rx Data Valid/Rx Enable
Test 11: Maintenance Mode Test
Test 12: Rx FIFO Test
Test 13: Interrupts Test
Test 14: Byte Swapper Test
Test 15: RX Interrupt Holdoff Timer Test
Test 16: DMA Start/DMA Abort Test
Test 17: Byte Count Register Test
Test 19: Speed Test
Test 20: XON/XOFF Recognition Test
Test 21: Data Format Test
Test 22: Modem Signal Test
Test 23: Framing Error/Break Bit Test
Test 24: Parity Generation/Detection Test
Test 25: Overrun Detection Test
Test 26: Exerciser Test
.. End of run, 0 errors detected, pass count is 1,
   time is  8-FEB-1983 10:58:50.63
```

The default selection of tests to be run is 1 to 26. A sequence of tests, and the number of passes, can be selected via the start command.

For example:

```
DS> START/PASS:3/TEST:7          ; 3 passes, tests 7 to 26

DS> START/PASS:0/TEST:7:10       ;  loop on test,  tests 7 to 10

DS> START/TEST:5:5               ; 1 pass, test 5 only
```

4.6.2.3 Event Flags – Event flag 1 can be set to disable the ROM version number message.

```
DS> SET EVENT 1
```

4.6.2.4 Sections – Section is part of the start command. If the section is not specified, tests from 1 to 26 will be run. By specifying the section, modem loopback tests or terminal echo tests can be selected.

For example:

```
DS> ST/SE:MODEM

..  Program:  DHU11 - VAX Functional Verification Test, revision
    1.0, 28 tests, at 11:22:10.11.
Testing: _TXA
lines to test [(ALL) or 1,2,...14,15]  13
Line  Speed  [(4800),   50,   75,  110,  134.5,  150,  300,  600,
1200,  1800, 2000, 2400, 7 200, 9600, 19200, 38400] 2400
Put all modems into loopback mode,  type RETURN  keys  when  done
[(No), Yes]  Y

Test 27: Modem Loop Test
.. End of run, 0 errors detected, pass count is 1,
   time is  8-FEB-1983 11:22:31.48
DS>
```

```
DS> ST/SEC:ECHO

..  Program:  DHU11 - VAX Functional Verification Test,  revision
   1.Ø, 28 tests, at 11:25:26.34.
Testing: _TXA
lines to test [(ALL) or 1,2,....14,15]  14
Line Speed [(48ØØ), 5Ø, 75, 11Ø, 134.5, 15Ø, 3ØØ, 6ØØ, 12ØØ, 18ØØ,
2ØØØ, 24ØØ, 7, 2ØØ, 96ØØ, 192ØØ, 384ØØ] 96ØØ
```

The test will run until either an error or Control Y is detected.

By pressing the break key when the terminal echo test is running, communication between terminal and DHU11 can be proven. 'Break' causes a framing error which generates an error message.

break key on terminal pressed

```
Test 28: Terminal Echo Test
********  DHU11 - VAX Functional Verification Test - 1.Ø  ********
 Pass 1, test 28, subtest 1, error 3,  8-FEB-1983 11:26:27.7Ø
 Hard error while testing TXA: Terminal Echo Test failed

********  End of Hard error number 3 ********

.. Halt on error at PC ØØØØ6F7F(X)
DS>
```

4.6.2.5 Error Messages – An error message may indicate that the option is defective or that an illegal parameter has been selected. Error numbers are interpreted in the diagnostic listing ZZ-EVDAI. See the previous section (4.6.2.4) for an example of an error message.

4.6.3 EVDAH On-Line Diagnostic

This diagnostic runs in the on-line mode under VMS V4.0 or later versions. The operator interface is via the VAX diagnostic supervisor (VDS), V6.13 or later. EVDAH provides a confidence check of DHU11s in VAX/VMS systems. It consists of five tests.

1. Internal data-loopback test on selected channels in sequence
2. Internal DMA data-loopback test on selected channels in sequence
3. Internal data-loopback test on selected channels at the same time
4. External loopback test (via H325) of modem control signals
5. External data loopback via a modem or H325. If a modem is used, it must be set up manually.

NOTE

Tests 4 and 5 run only when "/section=manual" is selected at run time.

Before running EVDAH, the user should be aware of the following points.

1. The tests are on-line, therefore it is essential to define the channels to be tested. The test will not run if a channel which is allocated to a process is selected for testing. Channel allocations can be checked by a Show Device command such as SH DEV/FULL TXA. In the typical response which follows, channels 0 and 1 are free and channel 2 is allocated to job control.

```
Device  TXA0:           3-FEB-1984 17:Ø2: 14.Ø4

      on line

  Error count           Ø    Owner process id          ØØØØØØØØ
  Operations completed  3    Owner process name
  Reference count       Ø    Default buffer size            8Ø

Device  TXA1:           3-FEB-1984 17:Ø2: 14.Ø8

      on line

  Error count           Ø    Owner process id          ØØØØØØØØ
  Operations completed  3    Owner process name
  Reference count       Ø    Default buffer size            8Ø

Device  TXA2:           3-FEB-1984 17:Ø2: 14.15

      on line
      Spooled
      Allocated

  Error count           Ø    Owner process id          ØØØ1ØØ74
  Operations completed  9    Owner process name        JOB_CONTROL
  Reference count       1    Default buffer size            132
```

2. If test 4 is to be run, an H325 loopback connector must be installed on the selected channel. By setting event flag 20, the operator can cause the program to halt between channel tests. This allows the H325 to be moved to the next channel to be tested. Another event flag (21) causes the program to halt after each DHU11 has been tested.

3. If test 5 is to be run, a modem or an H325 must be installed on the selected channel. The event flags also function in this test.

4. If tests 4 or 5 are run without some form of loopback installed, error messages will be generated.

5. In the DHU11 hardware, adjacent channels are paired (refer to Chapter 1, Section 1.3.3.1). Any attempt to change a baud rate that will change the group of an allocated channel will generate error messages. The baud rate will not be changed.

The EVDAH diagnostic is supported by the on-line help facility EVDAH.HLP.

4.6.4 Running the EVDAH On-Line Diagnostic

The minimum hardware requirements for EVDAH are:

- Any VAX system with a UNIBUS
- A console terminal
- One to eight DHU11s.

The VAX Diagnostic System User's Guide (EK-DS780-UG) provides instructions on how to load and run programs under the diagnostic supervisor. For details of on-line tests, refer to the diagnostic listing ZZ-EVDAH.

4.6.4.1 Starting Up – Before EVDAH can be run, VMS must be booted. The operator must then:

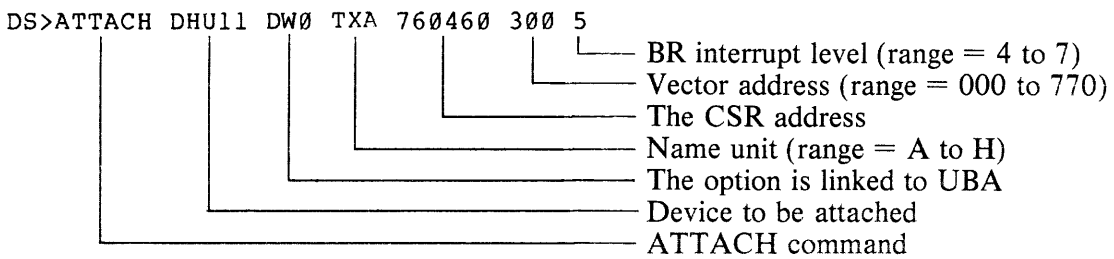
- Log into the system maintenance account
- Allocate the lines to be tested
- Load the diagnostic supervisor
- Attach the DHU11(s)
- Select the device(s) for test
- Start the diagnostic.

An example of how to attach the DHU11 and to load and run EVDAH follows. Where appropriate, commands for different systems are included.

```
$ ALL TXA0                          ; Allocate lines to be tested
$ ALL TXA1                          ;
$ ALL TXA2                          ;
$ RUN ESSAA                         ; For (11/780), Supervisor
      or
$ RUN ECSAA                         ; For (11/750)
      or
$ RUN ENSAA                         ; For (11/730)

DIAGNOSTIC SUPERVISOR  ZZ-ENSAA-Y6. 13-510  27-JAN-1984 12:00: 00.00
DS> ATT DW780 SBI DW0 3 4           ; For 11/780 Attach the UBA on the SBI
      or
DS> ATT DW750 HUB DW0               ; For 11/750
      or
DS> ATT DW730 HUB DW0               ; For 11/730

DS> LOAD EVDAH                      ; Load the DHU11 diagnostic
DS> ATT DHU11                       ; Attach the DHU11
DEVICE LINK? DW0                    ; The option is linked to the UBA
DEVICE NAME? TXA                    ; The option named unit:
                                    ; (range=A-F)
CSR? 760460                         ; The CSR address:
                                    ; (range=760000-777776)
VECTOR? 300                         ; Vector address: (range=000-770)
BR? 5                               ; BR Interrupt Level: (range=4-7)

DS> SEL TXA:                        ; Select Unit Under Test
DS> START                           ; Start diagnostic execution
```

The program should now be running

If preferred, the Attach command and parameters can be input as one statement. The following is an example of such a single-line entry.



4.6.4.2 Options – Once the program starts, the user is asked to select a number of options.

1. Lines which are to be tested
2. Baud rate
3. Type of loopback

1. Lines which are to be tested

The following question will be displayed.

Lines to test [(ALL),REV,EVE,ODD,0,1,2,3,4,5,6,7,8,9,10,11,12, 13,14,15]

Various responses can be given.

ALL – Test all lines (0 to 15) in ascending order. This is the default (press the RETURN key only).

REV – Test all lines (15 to 0) in descending order.

EVE – Test lines 0, 2, 4, 6, 8, 10, 12, and 14.

ODD – Test lines 1, 3, 5, 7, 9, 11, 13, and 15.

n – Test line n (where n can be any line number).

n,m – Test lines n,m (where n,m can be any combination of line numbers; for example, 0,15,3,7,1). The lines will be tested in the sequence entered.

Any invalid entry will display an error message:

?? Invalid response

followed by a reprompt of the input request.

2. Baud rate

The following question will be displayed.

Baud Rate [(9600),50,75,110,134,150,300,600,1200,1800,2000,2400,4800,7200,19200, 38400]

One of two responses can be given.

n – A specific value

RET – The default rate (9 600 bits/s)

Any invalid entry will display an error message:

?? Invalid response

followed by a reprompt of the input request.

3. Type of loopback

The following question will be displayed:

Loop Type [(INTERNAL), MODEM, H325]

Various responses can be given.

INTERNAL	–	Internal loopback will be used in the test. This is the default response (press the RETURN key only.
MODEM	–	A modem preset to loopback.
H325	–	External loopback connector is to be used.

Any invalid entry will display an error message:

?? Invalid response

followed by a reprompt of the input request.

4.6.4.3 Event Flags – Event flags are used to control multichannel or multi-DHU11 tests. Flags are set by the Set Event command. For example:

```
DS> SET EVENT 20
```

Event flag 20	–	Functions in tests 4 and 5 only. When flag 20 is set, the program is suspended after each channel is tested. A supervisor message will invite the operator to transfer the H325 or modem to the next channel to be tested.
Event flag 21	–	Functions in all tests. It is useful when more than one DHU11 is being tested. Event flag 21 has different functions in internal and external loopback tests.

Test	Flag 21	Function
1 to 3	0	Only the first DHU11 selected is tested.
1 to 3	1	All DHU11s are tested in the selected order. Console messages indicate the module under test. For example: INTERNAL LOOPBACK ON UNIT 000 INTERNAL LOOPBACK ON UNIT 001 INTERNAL LOOPBACK ON UNIT 002 INTERNAL LOOPBACK ON UNIT 003
4 and 5	0	Only the first DHU11 selected is tested.
4 and 5	1	The program is suspended before each module is tested. Console messages warn the user to transfer the H325 or modem.

4.6.4.4 Sections – Section is part of the start command. If the section is not specified, the default is tests 1, 2, and 3. If the section is specified as MANUAL, tests 4 and 5 are selected. For example:

```
DS> START                          ; runs tests 1, 2, and 3
DS> START/SEC=MANUAL               ; runs tests 4 and 5
```

4.6.4.5 Error Messages – If an error is detected during test, the program will output an error message. This may indicate that the option is defective or that an illegal parameter has been selected. Error numbers are interpreted in the diagnostic listing ZZ-EVDAH. The error messages below were generated by running tests 4 and 5 with the incorrect loopback mode selected.

```
Test 4: Test 4 - Modem Signal Loopback
********  DHU11 16 LINE ASYNC MUX TEST - 1.Ø  ********
 Pass 1, test 4, subtest Ø, error 2,  3-FEB-1984 15:5Ø:21.44
 System fatal error while testing TXA: INVALID LOOPBACK SELECTED

********  End of System fatal error number 2 ********

 [aborted]
Test 5: Test 5 - External Data Loopback
********  DHU11 16 LINE ASYNC MUX TEST - 1.Ø  ********
 Pass 1, test 5, subtest Ø, error 2,  3-FEB-1984 15:5Ø:22.71
 System fatal error while testing TXA: INVALID LOOPBACK SELECTED

******** End of System fatal error number 2 ********

 [aborted]
.. End of run, Ø errors detected, pass count is 1,
   time is  3-FEB-1984 15:5Ø:23.89
DS>
```

4.6.5 VAX Test Sequence

The precise sequence of diagnostic tests will depend on the state of the system and the fault which has been reported. If the system is on-line, it might be easier to run EVDAH before EVDAI. However, if it is off-line, EVDAI would probably be run immediately.

4.6.5.1 EVDAH Test Sequence – Figure 4-3 gives an example of H3029 distribution panels connected to a DHU11. A Show Device command would be used to check for 'owners' of channels 0, 1, and 2.

With the allocation shown:

a. Run tests 1, 2, and 3 on lines 3 to 15
b. Run test 4 on lines 3 to 15
c. Put the modem in loopback mode. Run test 5 on channels 1, and 3 to 15.

NOTE

The event-flag facility would be useful for b and c.

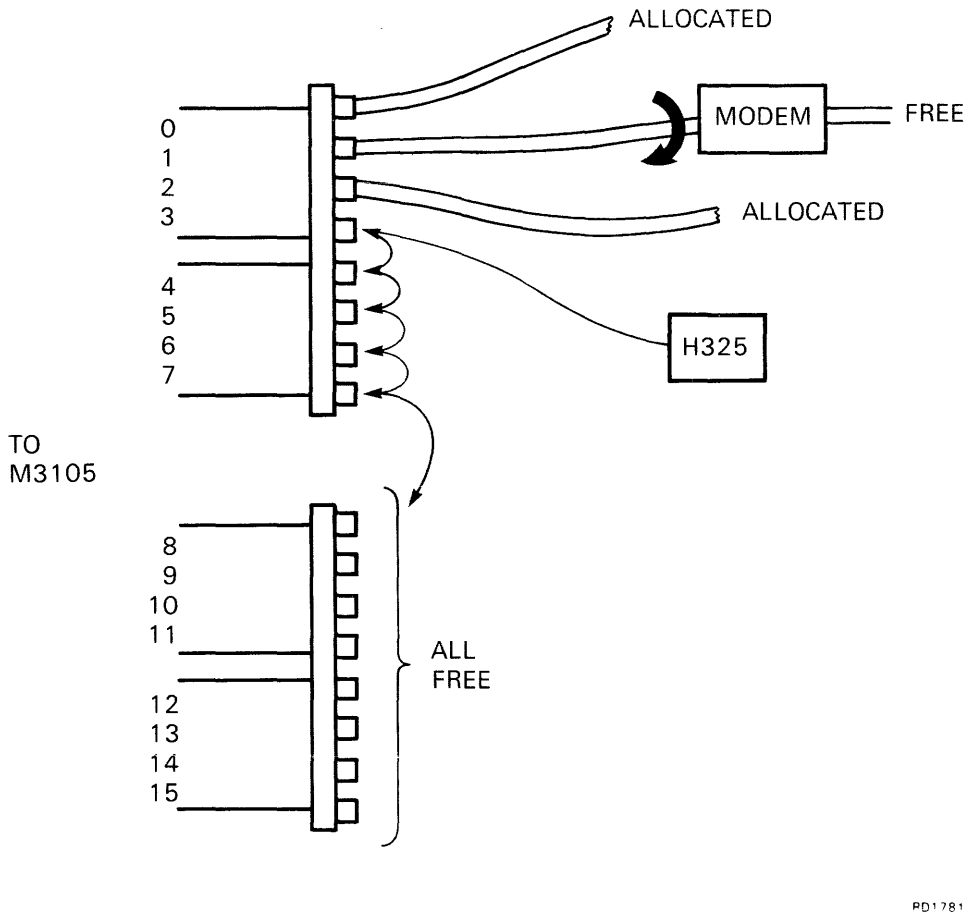


Figure 4-3 Example of Channel Allocation

4.6.5.2 EVDAI Test Sequence – Most of the EVDAI diagnostic will run in staggered loopback mode. Therefore, unless individual channel problems are indicated, tests should start with this mode.

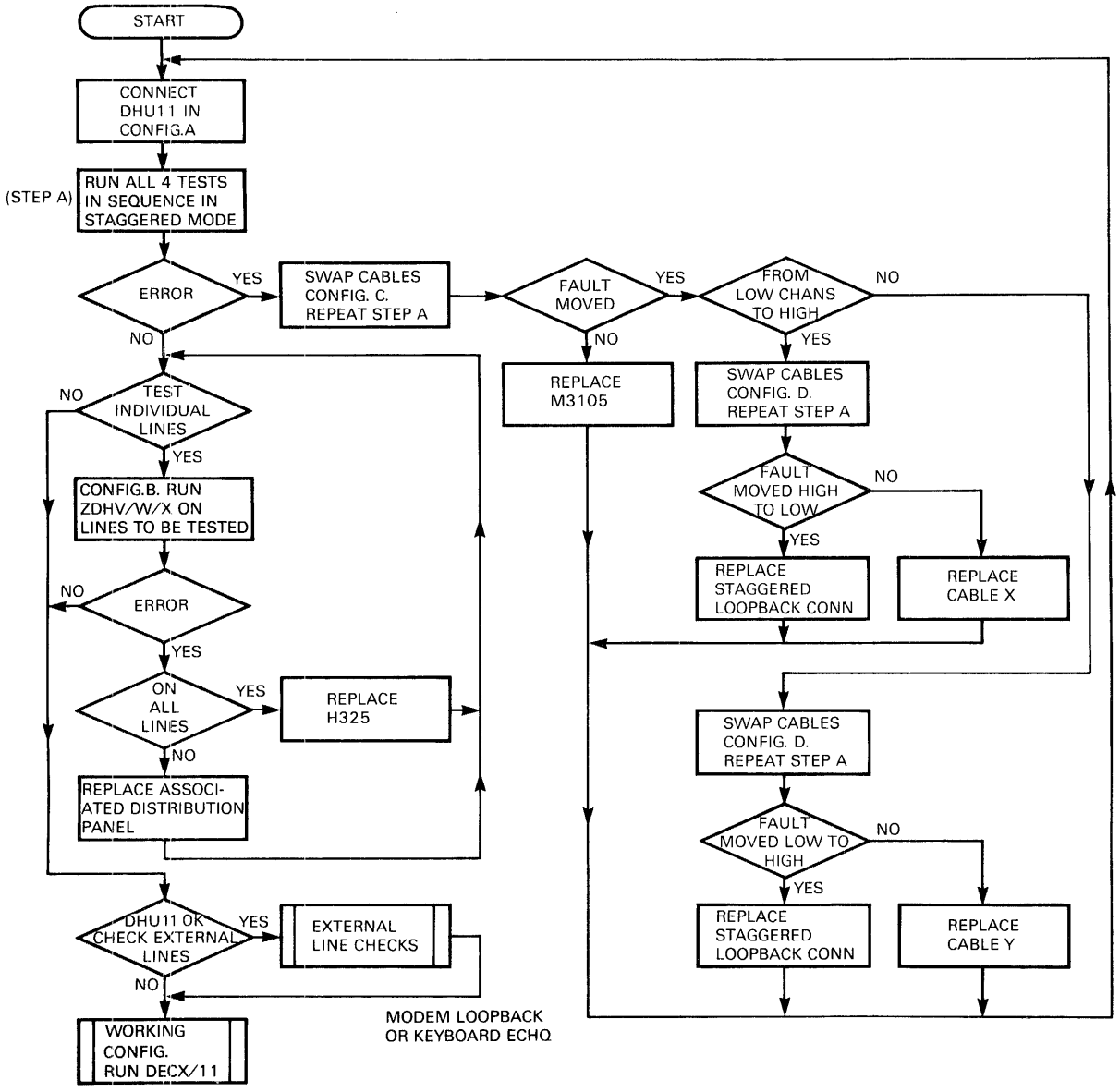
A troubleshooting diagram and a flowchart are provided by Figures 4-1 and 4-4. The flowchart shows a complete sequence that also checks the distribution panel and loopback connectors. However, if the initial test of all lines in staggered mode is error-free, the option is probably good.

4.7 FIELD REPLACEABLE UNITS (FRUs)

The FRUs are:

Reference No.	Item
M3105	Hex-height module
BC05L-xx	Flat cable, 40-conductor
H3029	Distribution panel (includes staggered loopback connector)
H325	Line loopback connector
H3277	Staggered loopback connector (if supplied).

Depending on local maintenance strategy, modems and/or external cables may also be FRUs. See Figure 4-1.



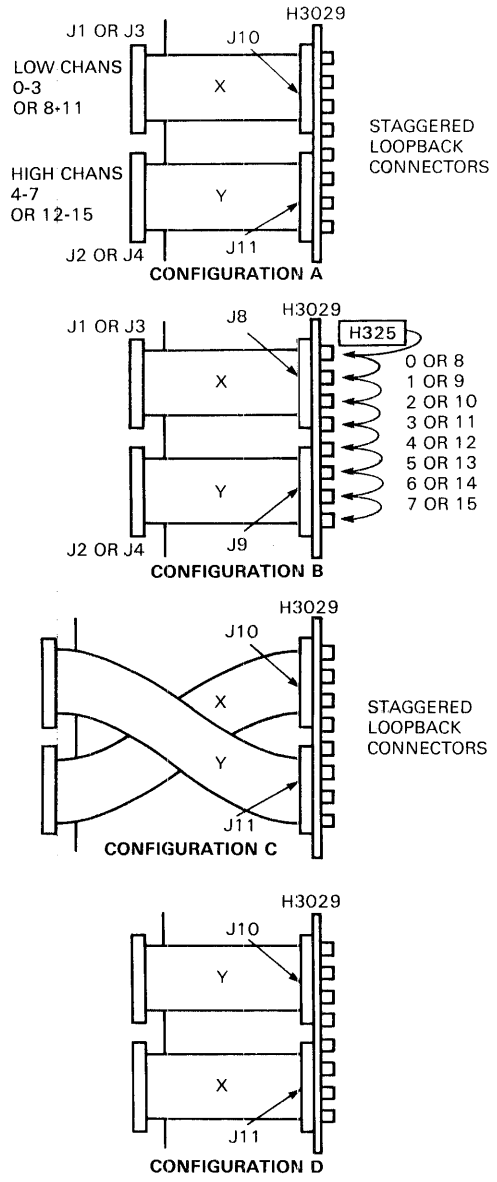


Figure 4-4 EVDAI Troubleshooting Flowchart

APPENDIX A
GLOSSARY OF TERMS

A.1 SCOPE

This appendix contains a glossary of terms used in this manual. The terms are in alphabetical order for easy reference.

A.2 GLOSSARY

asynchronous A method of serial transmission in which data is preceded by a start bit and followed by a stop bit. The receiver provides the intermediate timing to identify the data bits.

auto-answer A facility of a modem or terminal to automatically answer a call.

auto-flow Automatic flow control. A method by which the DHU11 controls the flow of data by means of special characters within the data stream.

backward channel A channel which transmits in the opposite direction to the usual data flow. Normally used for supervisory or control signals.

base address The address of the CSR.

BMP Background Monitor Program.

CCITT Comite Consultatif International de Telephonie et de Telegraphie. An international standards committee for telephone, telegraph, and data communications networks.

dataset See **modem.**

DIL Dual-In-Line. The term describes ICs and components with two parallel rows of pins.

DMA Direct Memory Access. A method which allows a bus master to transfer data to and from system memory without using the host CPU.

DUART Dual Universal Asynchronous Receiver Transmitter. An IC used for transmission and reception of serial asynchronous data on two channels.

duplex A method of transmitting and receiving on the same channel at the same time.

EIA Electrical Industries of America. An American organization with the same function as the CCITT.

EMC Electro-Magnetic Compatibility. The term denotes compliance with field-strength, susceptibility, and static discharge standards.

FCC Federal Communications Commission. An American organization which regulates and licenses communications equipment.

FIFO First In First Out. The term describes a register or memory from which the oldest data is removed first.

floating address A CSR address assigned to an option which does not have a fixed address allocated. The address is dependent on other floating address devices connected to the bus.

floating vector An interrupt vector assigned to an option which does not have a fixed vector allocated. The vector is dependent on other floating vector devices connected to the bus.

FRU Field Replaceable Unit.

GO/NOGO A test or indicator which defines only an 'error' or 'no error' condition.

IC Integrated Circuit.

I/O Input/Output.

LSB Least Significant Bit.

LSI-11 bus Another name for the Q-bus.

microcomputer An IC which contains a microprocessor and peripheral circuitry such as memory, I/O ports, timers, and UARTs.

modem The word is a contraction of MOdulator DEModulator. A modem interfaces a terminal to a transmission line. A modem is sometimes called a dataset.

MSB Most Significant Bit.

multiplexer A circuit which connects a number of lines to one line.

NPR Non-Processor Request. Requests for control of the UNIBUS for DMA transactions.

null modem A cable which allows two terminals which use modem control signals to be connected together directly. Only possible over short distances.

PCB Printed Circuit Board.

protocol A set of rules which define the control and flow of data in a communications system.

PSTN Public Switched Telephone Network.

Q-bus A global term for a specific DIGITAL bus on which the address and data are multiplexed.

RAM Random Access Memory.

RFI Radio Frequency Interference.

ROM Read Only Memory.

SPC Small Peripheral Controller.

split-speed A facility of a data communications channel which can transmit and receive at different data rates at the same time.

UART Universal Asynchronous Receiver Transmitter. An IC used for transmission and reception of serial asynchronous data on a channel.

UNIBUS A DIGITAL bus, common to a number of PDP-11 and VAX systems.

XOFF A control code (23_8) used to disable a transmitter. Special hardware or software is needed for this function.

XON A control code (21_8) used to enable a transmitter which has been disabled by an XOFF code.

APPENDIX B
MODEM CONTROL

B.1 SCOPE

This appendix contains information useful to both the programmer and the engineer. It defines control signals, describes typical modem control methods, and warns against likely network faults. A detailed example of auto-answer operation is included.

B.2 MODEM CONTROL

The DHU11 supports sufficient modem control to permit full-duplex operation over the public switched telephone network (PSTN) and over private telephone lines. Table B-1 lists the control leads supported by the DHU11, together with an explanation of their use and purpose. In this appendix, the terms MODEM and DATASET have the same meaning. They refer to the device which is used to modulate and demodulate the signals transmitted over the communications circuits.

The DHU11 modem control interface can be used in many applications. These include control of serial line printers, terminal cluster controllers, and industrial I/O equipment, in addition to the more usual applications in telephone networks. Use of the control leads described in Table B-1 is therefore completely application dependent, although there are international standards which telephone network applications should obey. There are no hardware interlocks between the modem control logic and the transmitter and receiver logic. Program control manages these actions as necessary.

A subset of the leads listed in Table B-1 could be used to establish a communications link using modems connected to the switched telephone network. Ring Indicator (RI), Data Terminal Ready (DTR), and Data Carrier Detected (DCD) are the absolute minimum requirements. In some countries Dataset Ready (DSR) is also needed. It is usually desirable, however, to implement modem control protocols which will operate over most telephone systems in the world. Also, some protection should be included to guard against network faults, particularly in applications such as dial-up time-sharing systems. Such faults include:

- Making a channel permanently busy (hung) because of a misdialed connection from a non-data station
- Connecting a new incoming call on an in-use channel. This fault might occur, for example, after a temporary carrier loss, if the host system assumed that the carrier was reasserted by the original caller.

Modem control with some protection against common faults, and which is compatible with the telephone networks in most geographic areas, can be implemented by using all the signals listed in Table B-1, in the way described by the CCITT V.24 recommendations. Section B.2.1 describes a method of implementing a full-duplex auto-answer communications link via modems over the PSTN. It is provided here only to show the operation and interaction of DHU11 modem control leads in a typical application.

Table B-1 Modem Control Leads

Name	RS-232-C	V.24	25-Pin	Definition
GND	AA	–	1	Protective ground. This provides a path between the modem and DHU11 for discharge of potentials such as static electricity.
GND	AB	102	7	Signal Ground. This is a reference level for the data and control signals used at the EIA interface.
TXD	BA	103	2	From DHU11 to modem. This signal contains the serial bit stream to be transmitted to the remote station.
RXD	BB	104	3	From modem to DHU11. This signal is the serial bit stream received by the modem from the remote station.
RTS	CA	105	4	From DHU11 to modem. Causes the modem's carrier to be placed on the line.
CTS	CB	106	5	From modem to DHU11. Indicates that the modem has successfully placed its carrier on the line and that data presented on circuit BA will be transmitted to the communication channel.
DSR	CC	107	6	From modem to DHU11. Indicates that the modem has completed all call establishment functions and is successfully connected to a communications channel.
DTR	CD	108/2	20	From DHU11 to modem. Indicates to the modem that the DHU11 is powered up and ready to answer an incoming call.
DCD	CF	109	8	From modem to DHU11. Indicates to the DHU11 that the remote station's carrier signal has been detected and is within appropriate limits.
RI	CE	125	22	From modem to DHU11. Indicates that a new incoming call is being received by the modem.

B.2.1 Example of Auto-Answer Modem Control for the PSTN

The system operator determines which DHU11 channels should be configured for either local or remote operation. Local operation implies control of data-leads only, while remote operation implies that modem control will be supported. The host software will assert DTR and RTS together with the Link Type bit in the LNCTRL register for all DHU11 channels configured for remote operation. DTR informs the modem that the DHU11 is powered up and ready to acknowledge control signals from the modem. RTS is asserted for the full-duplex mode of operation and causes the modem to place its carrier on the telephone line when the modem answers a call. Link Type (LNCTRL<8>) enables modem status information to be placed in the receive character FIFO where it will be handled by an interrupt service routine. Modem status changes are always reported in the STAT register regardless of the state of LNCTRL<8>. The modem is now prepared to auto-answer an incoming call.

Dialing the modem's number causes RI to be asserted at the EIA interface. This informs the DHU11 that a new call is being received. RI has to be in a stable state for at least 30 ms or else the change will not be reported by the DHU11. Since DTR is already asserted, the modem will auto-answer the incoming call and start its handshaking sequence with the calling station. The time needed to complete the handshaking sequence can be in the order of tens of seconds if fallback-mode speed selection and satellite links are involved. The modem will assert DSR to indicate to the DHU11 that the call has been successfully answered and a connection established.

NOTE

On some older types of modem used on the PSTN, the opposite effect is also true. The RI signal may be very short, or it may not even occur if DTR is previously asserted. When this type of modem answers an incoming call it asserts DSR almost immediately and deasserts RI at the EIA interface. Programs must therefore expect RI or DSR or DCD as the first dataset status change received from the modem when establishing a connection.

As RTS was previously asserted, the modem's carrier will be placed on the line when DSR is asserted. When the modem has successfully placed its carrier on the line it will assert CTS which indicates to the DHU11 that it may start to transmit data. Should the incoming call be the result of a misdialed number then it is possible that a carrier signal would never be received. To guard against this, the host starts a timer when it detects RI or DSR. This is usually in the range of 15 to 40 seconds, within which time the carrier must be detected. When the modem detects the remote modem's carrier signal on the line, it will assert DCD which indicates to the DHU11 that data is valid on the RXD line.

The modem may now exchange data between the DHU11 and the calling station for as long as DCD, DSR, and CTS stay asserted. If any of these three signals disappear, or if RI should be detected during normal transmission, it would indicate a fault condition. A change of state of any of these signals would cause an interrupt via the receive FIFO.

The handling of the fault conditions now becomes country-specific as some telephone systems tolerate a transient carrier loss while others do not. In the USA it is usual to proceed with a call if carrier resumes within two seconds. In non-USA areas it is possible for telephone supervisory signals, such as dial-tone, to be misinterpreted by the modem as a resumption of carrier. In this case the host program would assume that the connection had been reestablished to the original caller and would cause a 'hung' channel. To prevent this, DTR should be deasserted immediately after the loss of DCD, CTS, or DSR to abort the connection. DTR should stay deasserted for at least two seconds, after which time a new call could be answered.

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