pdp11

DX11B–PDP-11 TO IBM 360/370 CHANNEL INTERFACE

digital

Interfaces to most models of the IBM 360 or 370 on the selector, multiplexer or block multiplexer channels
Recognizes up to 128 IBM device addresses over the full range of 256 addresses.
Operates in the byte multiplexed or burst mode
NPR (DMA) operations to present status to 360, store 360 commands in the PDP-11, and transfer data
Hardware recognition and presentation of the 360 device address plus hardware presentation of initial status
Software interpretation and response to 360 commands
Can be programmed to emulate a 2848, 2703 or 3705 control unit
In off-line or powered-down mode, the DX11B is transparent to the S/360 and presents no load to the channel data and tag lines
Built-in maintenance and protection features
250,000 byte/second data transfer rate (depending upon IBM model)

The DX11B is a programmable interface between a PDP-11 UNIBUS™ and a S/360 or S/370 multiplexer or selector channel. The DX11B hardware handles the detection and response to all channel generated control signals. The DX11B hardware handles the Initial Selection Sequence operation without program intervention. It recognizes a wired (strapped) set of addresses, presents address, fetches a unique status (determined by the 360/370 command and device address) from a table in memory and stores an entry in a 128 entry tumble table. The status and tumble operations are by NPR (DMA). The tumble table entry contains status, IBM command and IBM address. Software interprets the command and responds to it. The commands recognized and the manner of response will depend upon the 360/370 control unit being emulated.

As soon as the hardware has stored the tumble table entry, it is ready to service another request from the 360/370. If both the PDP-11 and the 360/370 channel contend for the DX11B, the 360/370 channel wins and the PDP-11 is locked out. This protection feature makes sure the 360/370 channel is always master. It can cancel a previous request at any time.

The PDP-11 program loads DX11B registers to cause data transfers. Data transfer is by NPR. The length in bytes can be short (multiplex mode) or long (burst mode). Software determines which mode will be used. Burst mode is on selector channel or selector subchannel only.

The DX11B can be taken off-line or powered down. In either case, a relay closes to by-pass the SELECT-OUT line. The drivers and receivers on the 360/370 control and data lines present no bus loads when the DX11B is powered down. Thus, the DX11B is logically disengaged from the channel in the power-down or off-line mode. The DX11B contains power failure and timeout features. The power failure protection hardware interrupts the DX11 when an AC-low is detected. When in burst mode, timeout hardware interrupts the DX11 if the PDP-11 fails to respond in 5 seconds. In either case, the DX11B hardware stops all data transfers, presents UNIT CHECK status to the 360/370 and goes off-line. The programmer can disable the timeout feature during program debugging. The timeout will occur only while one of the DX11B-recognized devices is active (OPERATIONAL-IN is high).

The DX11B has a built-in channel simulator which is used by off-line diagnostics to verify the PDP-11 configuration up to and including the IBM cables. The latter can be checked by plugging one end into the DX11B and the other into the simulator.

Because NPR is used for data transfers, the DX11B is capable of data transfer rates in excess of 250,000 bytes/second. It is limited by the PDP-11 configuration and the rated capacity of the 360/370 channel to which it is attached.

Programming Interfaces

The DX11B has the following set of programmable registers:

Address	Description
176200	Device Status (DXDS)
176202	Command and Address (DXCA)
176204	Control Unit Status (DXCS)
176206	Offset and Status (DXOS)
176210	Bus Address for NPR (DXBA)
176212	Byte Count for NPR (DXBC)
176214	Maintenance-Out (DXMO)
176216	Maintenance-In (DXMI)
176220	Control Bits (DXCB)
176222	NPR Data (DXND)
176224	Extra Signals (DXES1)
176226	Maintenance-Out Buffered (DXMOB)
176230	Extra Signals (DXES2)

DXDS

DEVICE STATUS
This register contains all of the interrupt producing conditions along with various non-interrupt producing device status flags. This register is read only and is stored as the first tumble table entry before being reset.

BITS

Error Indicators

15   PARER   Parity Error
This bit is set if the DX11B detects an even-parity condition on the BUSOUT when either command or data information is sent by the channel (CH) to the DX11B. PARER will be set if bad Command-Out parity is detected during an ISS or if bad (BUSO) Data-Out parity is detected. PARER is not set on bad Address-Out parity during an ISS. In this case the DX11B will not recognize the Address from the CH.

14   NXM   PDP-11 Bus Timeout
This bit will set should the PDP-11 take longer than $20\mu s$ to complete any one Non-Processor Request Transaction (NPR). Such an occurrence might be the result of addressing a non-existent (memory) location. If set during a data transfer, this will terminate the sequence by setting CUDEND. Bus timeout is taken as equivalent to bus completion elsewhere so that a sequence may proceed to its normal ending point.

IBM Reset Indicators

13   SELRST   Selective Reset
This bit will be set by the channel execution of a Selective Reset Sequence as described in the *Channel (CH) to Control Unit (CU) OEM interface manual* published by IBM. This sequence is usually a response to a malfunction CU/device. When set, this bit causes a Program Interrupt (PI).

12   SYSRST   System Reset
This bit will be set by the channel execution of a System Reset sequence as described in the IBM document *Channel to Control Unit OEM Interface Manual*. When set this bit will cause a Program Interrupt.

11   INFDSC   Interface Disconnect
This bit is set when the channel performs a disconnect operation with the Control Unit.

Channel Status Flags

10   UCHKS   Unit Check Sent
Unit Check was included in status sent to the channel.

09   CHENDS   Channel End Sent
This bit is used to notify the emulator that CHEND status was sent in a status response.

08   BSYS   BSY Sent
BSY status bit was sent to the channel.

Channel Initiated End Indicator

07   CHIS   Channel Initiated (CHI) Selection Sequence End
This bit is set when a channel initiated sequence has been completed with the control unit. This bit becomes a zero when the DXDS is reset after the DXDS is entered in the tumble table.

Control Unit Initiated (CUI) End Indicators (PDP-11/DX11B)

06	ESEND	Ending Sequence End

This bit will set when a status byte is presented to the channel by a DX11 initialized sequence and/or when a stacked status is finally accepted.

This bit is most commonly associated with the Ending Status presentation type of sequence which normally follows a Data Transfer Sequence.

It may under some circumstances occur that the CHIS bit is set as a result of a CUI-ISS contention situation where the device address requested matched with the device address selected from the channel and the CU was requesting present status.

05	CHDEND	Channel Data End

This bit is set during a Data Transfer Sequence when the channel byte count overflows (Command-Out is sent in response to Service-In). This bit in its true state causes the CU to terminate the Data Transfer Sequence. This bit is also set when the CH terminates a Data Transfer Sequence by interface disconnect (INFDSC=1).

04	CUDEND	Control Unit Data End

This bit is set during a Data Transfer Sequence when the DXBC (byte count) register goes to its all zero state. When set, this bit causes a PI and also causes the DONE bit to assert. When this bit asserts, it causes the CU to terminate the Data Transfer Sequence.

Special Indicators

03	ISSREJ	Initial Selection Sequence Rejected

This bit is set when a channel-initiated selection sequence addressed to the CU was answered by the CU with a Control Unit Busy status indication and a short Control Unit Busy sequence. This can only occur if the CUBSY bit in the DXCS was set when the CH tried to initiate an ISS and the CU was in its idle phase.

02	CMDCHN	Command Chaining

This bit sets if the channel has indicated that another operation will probably follow for the CU/Device currently connected when the DX11B presents Device End status to the channel. Command chaining occurs when the current 360 Channel Command Word (CCW) has its command chaining bit set. The channel informs the DX11 of this by raising Suppress-Out at the same time as Service-Out.

01	STKSTB	Stack Status Copy

This bit is set when the Channel (CH) informs the DX11 that the status byte being presented on the BUS-IN cannot currently be accepted by the CH. This occurs when the CH responds to Status-In with Command-Out.
STKSTA may be set by the program if the DX11 is not active with the CH (LOCK=0). This is useful when initiating a DX11 request for status presentation. If Suppress-Out and STKSTA are both true, the DX11 drops its Request-In since the status contained is suppressible (once status has been stacked the CH also defines that status as suppressible). Since this bit is a copy of STKSTA, it is read only and is not reset with the rest of DXDS.

00	CMDREJ	Command Rejected

A Channel Initiated Selection Sequence command was ignored due to bad parity, a busy device, a pending status, or an illegal command for the device.

DXCA		COMMAND AND ADDRESS

DXCA contains the control unit command register, CUCR, and the control unit address register, CUAR. These two bytes are the address and command as transmitted from the channel during an initial selection sequence. This register is stored as the second tumble table entry upon completion of a CH-CU interaction.

15-08	CUCR	The odd byte of the DXCA register contains the Control Unit Command Register (CUCR). The CUCR cannot be loaded by the program. This byte contains the last command sent by the channel (even if it was rejected by the DX11).
07-00	CUAR	The even byte contains the Control Unit Address Register (CUAR). The CUAR is loaded with the device address from Bus-Out during an initial selection sequence. The CUAR is also loaded and cleared via PDP program control if LOCKO is a (0). The CUAR need not be loaded with some device address that is to be supported by the DX11 prior to going ON-LINE.
DXCS		**CONTROL UNIT STATUS** This register contains the primary control command information bits and primary status indications for the DX11. The DXCS may not be modified by the PDP program when LOCKO equals one (except for DONE and INTEN).

BITS

15	PARSTP	Stop on Parity Error Enable If this bit is set to a one and a parity error occurs on Bus-Out during a Data Transfer Sequence, then the sequence is terminated and CUDEND will be set. If this bit is not set, PARER may still become set but the sequence will end normally.
14	CUFBM	Control Unit Forced Burst Mode Enable This bit can be set by the program when CU Forced Burst mode is desired. This condition causes the CU to hold OPL-IN up from initial selection through the presentation of Channel End (except for TIO and IIIO).
13	ENDEN	Control Unit End Enable This bit is set and cleared only by the PDP-11 program. The purpose of setting this bit is to assert the control unit end bit (CUEND) in the device status presented to the channel during a control unit busy sequence; i.e., where the CUBSY bit is already set.
12		Reserved
11	BSYEN	CUBSY Enable This bit enables the setting of CUBSY immediately upon responding to an ISS (either CUI or CHI). This bit is set to a one by the program for emulating any single thread (shared) control unit such as 2848, 2803 and 2821. It is set to zero for multiple-thread control units such as 2703.
10		Reserved This bit is reserved for future use.

09	ONLINA	On-Line Request Enable

09   ONLINA   **On-Line Request Enable**
This bit is writable (except when LOCKO is set) by the PDP program to either the one or the zero state. ONLINA indicates that the control unit has made or is making a request to go on-line to the 360 channel. It is a two-stage operation. This is the lower stage of going on- or off-line operation and is the stage loaded or cleared by program command (ONLINA: DXCS(09)). The upper stage is the operating on-line bit ONLINB (DXCB(02)). ONLINB follows the changes of ONLINA at a time when, as specified in the OEM channel manual (IBM), it is proper to make changes from on-line to off-line or from off-line to on-line. (The CH is considered on-line itself whenever Operational-Out is set.)

08   CUBSY   **Control Unit Busy Enable**
Setting this bit will cause a channel initiated sequence to be answered by the DX11 with a Control Unit Busy Sequence. This bit causes the BSY bit to assert to the BUS-IN during the subsequent status presentation from the DX11. This bit is set and cleared by program and by the DX11 hardware if so enabled by BSYEN.

07   DONE   **Sequence Done**
The DONE bit is the normal interrupt producing condition which the DX11 uses for its primary interrupt control (c.f., INTEN). If both DONE and INTEN are set an interrupt will be requested.

Clearing DONE is required (of the program) only before making an attempt to change registers. With DONE reset, the DX11 will reset LOCKO if the DX11 is in either phase 0 or phase 7. Loading DONE is allowed only in phases 0 or 7.

06   INTEN   **Interrupt Enable**
This bit is always writable. It is recommended that this bit always be set before setting ONLINA and that ONLINB (via ONLINA) be cleared prior to clearing this bit. This bit may be cleared or set by program control only.

05   STKSTA   **Stack Status**
If set, STKSTA indicates that status was stacked. When cleared, it indicates that status was accepted. It may also be set voluntarily by a program that is presenting a suppressible (or low priority) status. It is also set automatically by the DX11 when the CH requires a status to be stacked and the DX11 will attempt to present it again.

04, 03   XBA   **Extended Bus Address Bits**
These bits are the two extended most significant bits of the memory address register during data input/output. They are loaded and cleared under program control and may be caused to complement should the DXBA overflow from a DXBA increment of +2 during a data transfer. They are used only during a data sequence.

02, 01   FCTN   **Function**
These two bits make up the DX11 function register. It is used by the program to select the CU operations desired:

FCTN=0—reset the DX
FCTN=1—input data transfer (from 360/370)
FCTN=2—output data transfer (to 360/370)
FCTN=3—present asynchronous status (to 360/370)

00   GO   When the GO bit is set, the function requested is performed. If FCTN=0 the reset operation is done on the DX11 and the DONE bit is left cleared.

If FCTN is not zero, then Request-In (REQI) will be raised as the start of a Control Unit Initiated (CUI) sequence.

DXOS   **OFFSET AND STATUS**
This is a two-byte register. The odd byte (CUOR) contains the offset address of the Status Pointer Word (SPW) table located in PDP-11 memory. The even byte (CUSR) contains the status byte that will be presented to the 360/370.

BITS			
15-08	CUOR		Control Unit Offset Register The CUOR contains the high order six bits of the SPW table and of the tumble table. It is program-loaded while in the off-line mode.
07-00	CUSR		Control Unit Status Register The CUSR contains the standard IBM status information bits which are transmitted to the channel.
07	ATTEN		Attention
06	STAMOD		Status Modifier
05	CUEND		Control Unit End
04	BSY		Busy The program should not directly set this bit. This bit is set only by a CU Busy Sequence or by being loaded as the status portion of the Status Pointer Word.
03	CHEND		Channel End
02	DEVEND		Device End
01	UCHECK		Unit Check
00	UEXCEP		Unit Exception

DXBA

BUS ADDRESS REGISTER

The bus address register is a 16-bit register which can be cleared and loaded under program control if LOCKO is not set (0). It is used during data transfers to point to the PDP-11 core location to/from which data will be transferred 16-bit words at a time. The DXBA register is also used during channel initiated sequences to fetch both the Status Pointer Word and the device status byte from PDP-11 core. During a data transfer the DXBA is preset by program to point to the first byte location where data is sent or stored. The DXBA register is incremented by two each time a PDP data word is fetched or stored in core during the data transfer process. Should the DXBA register overflow, the extended memory address bits (XBA) in the DXCS register will be caused to complement their states appropriately. The DXBA is also used to address the tumble table when information is to be stored there.

DXBA(00)

The low order bit of the DXBA is normally set to zero by program load. When this bit is placed on the UNIBUS address lines (ABUS), it is always represented as zero. This bit is also used to initiate the BALF flop when control is transferred to phases 5 or 6 to select the odd or even first byte of the first data word.

DXBC

BYTE COUNT

This register is used only during data transfers. It is loaded and cleared under program control and is set up prior to the data transfer involved. The DXBC is set to the negative of the number of bytes to be transferred. As each byte is actually transferred to/from the DX11, the DXBC register is incremented by one until all bytes are transferred, whereupon the DXBC equals zero. When the DXBC contents go to zero during a Data Transfer Sequence, the CUDEND bit of the DXDS will set, thereby terminating the data transfer sequence with the channel.

DXMO		MAINTENANCE-OUT

This register is used for holding the 360 Channel Bus-Out Data and Tags. This register is always directly readable by a PDP-11 program.

When the DX11 is On-line, the bits in this register are usually the same as what appears on the Bus-Out lines (hardwired cables to the Bus-Out Plug).

When the DX11 is Off-line, these bits may be written directly by a PDP programmed request. The programmed bits are held buffered in the DXMOB. When the DX11 is On-line but cabled to the Bus-Out Test Plug, these bits are also writable by PDP-11 programs. The on-line cabled mode is used to isolate the cables and Bus-Out receivers as an error source.

BITS

15-08	CONO	Control Out-Lines Register

This byte contains the following signals as strobed from either the Bus-Out lines or from CONOB:

Selection Control Lines

15	OPLO	Operational-Out

This line indicates that the channel is in operation.

Note: refer to IBM manual A22-6843 for detailed description of each line of the 360 bus.

14	HLDO	Hold-Out

13	SELO	Select-Out

This bit is set only if both hold-out and select-out are set. When set or cleared by a PDP-11 program, only the simulated select-out signal is affected (see DXMOB).

12	SUPO	Suppress-Out

Tag Lines

11	ADRO	Address-Out

10	CMDO	Command-Out

09	SRVO	Service-Out

Parity Line

08	PARO	Parity-Out

This bit does double duty when written by a PDP program while the DX11 is in on-line cabled mode. At such times the state of the bit will be translated directly into the state of the Simulated Clock-Out line (of the Bus-Out Test Plug) and into the Parity-Out line. Clock-Out's primary purpose is to synchronize the control units to make changes in their ON/OFF-LINE state.

Another function of the bit is to allow the program generation of either normal (odd) Parity-Out or "bad" (even) Parity-Out. This feature is necessary in order to permit checking the parity generator within the main DX11 logic.

Data Lines			
07-00	BUSO		IBM Bus-Out Register

Bus-Out data bits 0 to 7, as seen either directly from the Bus-Out Cables or from BUSOB, if off-line.

When written by the PDP-11 program, this byte is buffered in BUSOB.

DXMI   MAINTENANCE-IN

This register is used for reading the Bus-In Tags and data originating mainly from the main DX11 logic. In this way the register represents the channel's view of the Bus-In. The output of these flops is enabled to the Bus-In lines either whenever OPLI=1 or whenever a fast CU-Busy is in progress.

The register is normally read only, but for maintenance purposes programmed modification is permitted except for CLKO and PARI.

When the DX11 is off-line, the data read by PDP-11 programmed references come directly from DXMI. When the DX11 is on-line, the data read by the PDP-11 program comes from the Test-In plug. Correct data will be seen then only if the plugs are cabled together.

BITS

15-08	CONI	Buffered Control Lines in Register

This byte contains the following signals:

Selection Control Lines

15	OPLI	Operational-In
14	SELI	Select-In (not direct cleared)
13	REQI	Request-In

Tag Lines

12	ADRI	Address-In
11	STAI	Status-In
10	SRVI	Service-In

Test Lines

09	CLKO	Clock-Out signal from Bus-Out

This line always comes from the cables, even when the DX is off-line.

08	PARI	Bus Parity-In (not a flip-flop—output of parity generation for BUSI)

Data Lines

07-00	BUSI	Buffered Bus-In Data Register

This byte contains the data that is enabled to the Bus-In lines for transmission back to the IBM 360 channel. The output of this byte also is always input to a parity generator that produces the signal PARI.

DXCB   CONTROL BITS

This is a 16-bit register containing control bits such as LOCKO, phase flip-flops and time state. It is a read only register used by the diagnostics to determine the condition of the DX11B.

DXND   NON-PROCESSOR REQUEST (NPR) DATA

This is a 16-bit register to/from which NPR data moves. It is readable for diagnostic purposes.

DXES1		EXTRA SIGNALS

DXES1 — EXTRA SIGNALS
This is a two-byte register containing the tumble table index and some miscellaneous signals. The odd byte contains the Tumble Table Index (TTNDX). It indicates the word-pair address for the next tumble table entry to be made by the DX11B. The even byte (MISC) contains miscellaneous control signals for DX11B maintenance diagnostic purposes.

15-08 TTNDX Tumble table index byte
This byte is the low order address of the tumble table entry to be used next. It is shifted left before being copied into the DXBA.

07-00 MISC Miscellaneous control signals byte

07 Reserved

06 ODD Copy of DXBA(00) (for future use)

05 NPRTO NPR latency error. Bus grant not received within timeout interval.

04 DXTO Program response latency error. While OPL-IN was up, the program did not interact for a 5-second period.

03 TIMDIS Set to disable DXTO during program debugging.

02 SOSIEN Fast NPR test enable. Cause simulated SRVO to follow SRVI.

01 MCLKEN Maintenance clock enable
When this bit is set the DX does not change time states until MCLKP is set:

00 MCLKP Mainenance clock pulse
If MCLKEN is set, setting this bit causes the DX to enable the next time state.

One normal clock pulse will be issued with each setting of MNCLKF, the Clock pulse thus generated will reset the MNCLKF. The UNIBUS interface continues to run at normal speed at all times. Maintenance clock mode cannot be entered when on-line.

DXMOB MAINTENANCE-OUT BUFFERED
This is a 16-bit register containing the buffered setting of the Control-Out and Bus-Out lines. It is read only. It consists of the flip-flops that are set when the program writes to DXMO. When the DX11B is cabled back to itself and on-line, a comparison of the contents of DXMOB and DXMO is an indication of the operational condition of the DX11B drivers and receivers and of the IBM cables.

DXES2 EXTRA SIGNALS
Contains interval signals for DX11B maintenance diagnostics.

15-02 Reserved

01 DSCRSP Disconnect response
Hardware controlled latch that enables 'Fast CU busy' and 'Propagate Select Out' during Phases 4 and 7. Immediately after an Interface Disconnect. This allows Operational-In to be dropped in Phases 4 on an Interface Disconnect to meet the 6 μsec timeout requirement.

00 IRS IBM reset conditions stored
Hardware controlled latch to cause an IBM reset condition (Interface Disconnect, System Reset, Selective Reset) to be stored in the tumble table when that condition was recognized during Phase 4 or 7.

The Status Pointer Word (SPW) is accessed by the DX11B during an Initial Selection Sequence (ISS) to determine the status of the 360/370 device selected. During the ISS, the DX11B must present status for the command issued by the 360/370 for the device indicated by the DX11B when it presented Address-In. The SPW is used to perform that function.

The SPW is a word table indexed by the Control Unit Offset Register (CUOR). A 256-word memory area is reserved for the SPW. Word 0 of the SPW contains the SPW entry for device 0, word 1 for device 1, . . . , word 255 for device 255. The SPW is always on a 512 word PDP-11 memory boundary.

The SPW is a two-byte entry. The even byte contains channel status information. When an access is made to the SPW, the even byte is loaded into the Control Unit Status Register (CUSR). The odd byte contains either 0 or an offset value. If=0, the content of CUSR is the status response to all commands for this device. No further NPR operations are required for status. If the odd byte contains an offset value and the even byte is zero, the odd byte is used as the pointer to a 256-byte Device Status Table (DST). The 360/370 command is used as an index into this table to retrieve a unique status for that command. The DST status is retrieved if the SPW even byte is zero and the odd byte is other than zero. If the status byte is retrieved, it is loaded into the CUSR to become the status byte that will be presented to the 360/370. Each device can have the same, a unique, or no DST, as determined by the requirements of the control unit and devices being emulated. For each DST specified, 128 words must be reserved. The meaning of each status bit is 360/370 device-dependent. The DST is always located on a 128 word PDP-11 memory boundary.

This is the name given the circular buffer in which the DX11 stores an entry at the end of each interface activity. The interface activity can be channel (360/370) or Control Unit (PDP-11 emulation) initiated.

A 256-word area is reserved for the TT: Each entry consists of two words. The content of the two words will be the value of DXDS and DXCA, respectively, at the time the channel activity occurred. The entry is guaranteed to be other than zero. TTNDX is the index to the next TT entry to be used by the DX11B. The program must zero the slot after using it. Each entry made by the DX11B causes an interrupt and sets the DONE bit. The program can service all table entries on each interrupt. The program must keep its own TT pointer. The TT is physically located in the next 256 words above the 256 word PSW table.

Because the DX11B must respond to Initial Selection Sequences every 32 microseconds, a tumble table is used to indicate when one occurred. An interrupt is generated when the entry is made. If the program permits an interrupt on each entry, it will be impossible to service an interrupt in 32 microseconds. Besides, a subsequent table entry may supersede an operation specified by a previous entry. Therefore, it is desirable to service all tumble table entries when an interrupt occurs. The recommended interrupt procedure is:
Clear DONE bit.

　　Service all tumble table entries until a zero entry occurs, clearing the TT entries as they are processed.

　　Build a queue of operations to be performed.

　　Load the registers (DXCS, DXOS, DXBA and DXBC) with the required data to perform the first operation: set the GO bit.

As the queue of operations is built, a subsequent TT entry may cancel one of the operations in the queue. It is important to be able to delete an operation from this queue.

It must be remembered that the 360/370 channel is always master and the control unit cannot perform a function the channel has told it to terminate.

NOTE: Under no circumstances should the Interrupt Enable bit of the DX11B or any other PDP-11 peripheral be cleared while the DX11B is on-line. Otherwise a NO-SACK timeout may occur which in turn can cause DX11B NPRTO error.

NPR operations are used for data transfers, Burst mode is defined as any data transfer longer than 32 microseconds. When byte multiplexed mode is desired, the program must break up a block of data into 4-byte segments and initiate a Control Unit Initiated (CUI) operation for each segment. CUI is initiated by raising the REQUEST-IN control line. DXBC should never be loaded with a value greater than minus 4 if multiplexed mode is desired.

Programming is used to detect Tumble Table Overflow. The TT can hold 128 entries. This will normally be more than enough. However, it is possible for an overflow to occur.

Overflow is defined as follows:

The program has a pointer to the tumble table entry it serviced last. When it uses the contents, it zeros the entry. When it is ready to service another entry, overflow has occurred if the previous entry (still indicated by program pointer) is other than zero.

Overflow is an irrecoverable error. The program should present UNIT CHECK status for each active device and go off-line.

This paragraph contains a discussion of some of the general programming considerations that pertain to the DX11-B.

Because of a contention situation that can arise when both the channel and the control unit (through software request) attempt to use the interface, an interlock mechanism is necessary to protect information used by both parts of the system. The control unit can appear busy to channel activity when the control unit software must use the facilities. After system reset, while table initialization is in progress, the CUBSY flip-flop is set.

The general solution is simply to let CH requests always override CU requests. This is done by the LOCKO flip-flop which prevents further changes to the DX11-B registers once a selection sequence has begun. The program can later examine the interrupt conditions to determine if the program requests must be repeated. LOCKO gets DXCS, DXCA, DXOS, and DXBA. Only DXBC remains program-writable.

  a. The SPW, TT firmware is 512 words long and must begin on a 2000_8 address boundary
  b. All DSTs are 256 bytes long and must begin on a 400_8 address boundary.
  c. All data transfers should begin on an even boundary. On input operations, the following will occur for odd BA and odd BC, respectively:
      1. When starting an input on an odd address, the *previous* even address byte is clobbered.
      2. When ending an input on an even address, the *following* odd address byte is clobbered.
  d. On output operations, as many as two words *following* the end of the data buffer can be pre-fetched. Therefore, buffers should not be assigned at the *end* of core. This prevents spurious NXMs.

When the DX11-B requires either a program interrupt or tumble table service, it sets the DONE bit, leaving LOCKO set. When the program is ready to try a CUI, it must clear DONE; then, if no new selection is in progress, the DX11-B will clear LOCKO.

The following rules should be followed:
  a. The TT entry should be zeroed after being serviced.
  b. On an INT, *all* nonzero TT entries should be serviced before dismissing INT (RTI).
  c. Software should keep a pointer to current TT entry. This should follow the hardware pointer in relieving the entries the hardware places (hardware will guarantee a nonzero TT entry).

d. No software requests for data transfer or status should be made until all TT entries are serviced.

e. *Before* each TT entry is serviced, DONE should be cleared with a

    BIC # DONE, DXCS

thus, the general INT service procedure is:

1. Clear DONE.

2. Service current TT entry. Update action to be performed for device whose address is in TT entry. Do not request data transfer or status at this time. (Note that this may *cancel* a previously queued request for this device.)

3. Clear TT entry.

4. Bump software pointer to next TT entry.

5. When a zero TT entry is encountered, initiate *last* action pending for each device.

6. Dismiss interrupt (RTI).

Data transfer sequences (DT) are always initiated by the DX11-B program. It is a software responsibility to ensure that a DT is valid at the point requested. Information supplied to the hardware includes Buffer Start Address (DXBA), byte Count (DXBC), Device Address (CUAR), and I/O direction (FCTN—input or output). The hardware will get control of the I/O interface and transfer the data in a single burst, after which it will generate a Data End interrupt. The last bit set is the GO bit. If LOCKOUT is set at this time, the effect is a NO OP and the result is no data transfer.

Several other events can happen as follows:

a. A bus out parity error can occur, setting PARER. This will terminate data transfer with PARSTP.

b. A timeout reference can occur, setting NXM.

c. The channel can indicate I/O stop, setting CHDEND.

d. An Interface Disconnect can occur.

If a CUI is used, it could be overridden by an ISS, in which case an interrupt would occur; but different bits would be set in the DXDS and copied into the tumble table.

There are several cases in which presentation must be initiated by the program as follows:

a. When stack status is indicated by the channel. In this case, the DX11-B will automatically request presentation of the status again, until it is subsequently relieved or overridden via an ISS (only if BSYEN=1).

b. When ending status is initially available for the device (DEVEND, etc.).

c. When asynchronous status becomes available for the device (DEVEND or ATTEN).

d. When a device that had previously been interrogated while busy becomes free (CUEND or DEVEND).

e. At the termination of a data transfer (CHEND or CHEND+DEVEND).

The program loads the status and device address and requests status presentation (FCTN=3). If the status is accepted, the device status, device address and command (if any) are loaded into the tumble table and an interrupt is generated.

The ONLINA flip-flop is written by the program to request a change of on-line status. The ONLINB flip-flop, in DXCB, can be read to verify that the transition occurred. The program clears the ONLINA flip-flop to attempt to put the DX11-B off-line. The ONLINB flip-flop will not clear if any channel activity is in progress.

An on-line/off-line request can be made at any time. If channel activity occurs at the time ONLINA is cleared, it will not clear. This allows the program a chance to reconsider the off-line request in view of the new CHIS.

DEC No.	Description	Prerequisite
DX11-BA	360/370 channel interface w/115V 60Hz power supply and an H950 standard PDP-11 cabinet	PDP-11 (PDP-11/20 or PDP-11/15 w/ KH11-A Option & Comtex Software)
DX11-BB	360/370 channel interface w/230V 50Hz power supply and an H950 standard PDP-11 cabinet	same

The DX11B can be used for any application where it is desirable to have a PDP-11 as a pre- or post-processor to either a S/360 or S/370. With its ability to emulate a 2848 display or a 2703 or 3705 communications controller, it is compatible with OS/GAM, BTAM, QTAM and TCAM and DOS/BTAM and QTAM. It can be used in systems designed for the following applications:

1. Front-end processors
2. Message switching
3. Store and forward
4. On-line inquiry
5. Data entry
6. Remote batch
7. Display cluster control
8. On-line data enscribers

DIGITAL EQUIPMENT CORPORATION, Corporate Headquarters: Maynard, Massachusetts 01754, Telephone: (617) 897-5111
SALES AND SERVICE OFFICES

DOMESTIC — ARIZONA, Phoenix and Tucson • CALIFORNIA, Los Angeles, Monrovia, Oakland, Ridgecrest, San Diego, San Francisco (Mountain View), Santa Ana, Sunnyvale and Woodland Hills • COLORADO, Englewood • CONNECTICUT, Fairfield and Meriden • DISTRICT OF COLUMBIA, Washington (Latham, Md.) • FLORIDA, Orlando • GEORGIA, Atlanta • ILLINOIS, Chicago (Rolling Meadows) • INDIANA, Indianapolis • IOWA, Bettendorf • KENTUCKY, Louisville • LOUISIANA, Metairie (New Orleans) • MASSACHUSETTS, Marlborough and Waltham • MICHIGAN, Detroit (Farmington Hills) • MINNESOTA, Minneapolis • MISSOURI, Kansas City and St. Louis • NEW HAMPSHIRE, Manchester • NEW JERSEY, Fairfield, Metuchen and Princeton • NEW MEXICO, Albuquerque • NEW YORK, Albany, Huntington Station, Manhattan, Rochester and Syracuse • NORTH CAROLINA, Durham/Chapel Hill • OHIO, Cleveland, Columbus and Dayton • OKLAHOMA, Tulsa • OREGON, Portland • PENNSYLVANIA, Philadelphia (Bluebell) and Pittsburgh • TENNESSEE, Knoxville • TEXAS, Austin, Dallas and Houston • UTAH, Salt Lake City • WASHINGTON, Bellevue • WISCONSIN, Milwaukee (Brookfield) • INTERNATIONAL — ARGENTINA, Buenos Aires • AUSTRALIA, Adelaide, Brisbane, Canberra, Melbourne, Perth and Sydney • AUSTRIA, Vienna • BELGIUM, Brussels • BOLIVIA, La Paz • BRAZIL, Puerto Alegre, Rio de Janeiro and São Paulo • CANADA, Calgary, Halifax, Montreal, Ottawa, Toronto and Vancouver • CHILE, Santiago • DENMARK, Copenhagen • FINLAND, Helsinki • FRANCE, Grenoble and Paris • GERMANY, Berlin, Cologne, Hannover, Hamburg, Frankfurt, Munich and Stuttgart • HONG KONG • INDIA, Bombay • INDONESIA, Djakarta • ISRAEL, Tel Aviv • ITALY, Milan and Turin • JAPAN, Osaka and Tokyo • MALAYSIA, Kuala Lumpur • MEXICO, Mexico City • NETHERLANDS, Utrecht • NEW ZEALAND, Auckland • NORWAY, Oslo • PHILIPPINES, Manila • PUERTO RICO, Santurce • SINGAPORE • SPAIN, Barcelona and Madrid • SWEDEN, Gothenburg and Stockholm • SWITZERLAND, Geneva and Zurich • TAIWAN, Taipei and Taoyuan • UNITED KINGDOM, Birmingham, Bristol, Dublin, Edinburgh, Leeds, London, Manchester and Reading • VENEZUELA, Caracas • YUGOSLAVIA, Ljubljana •