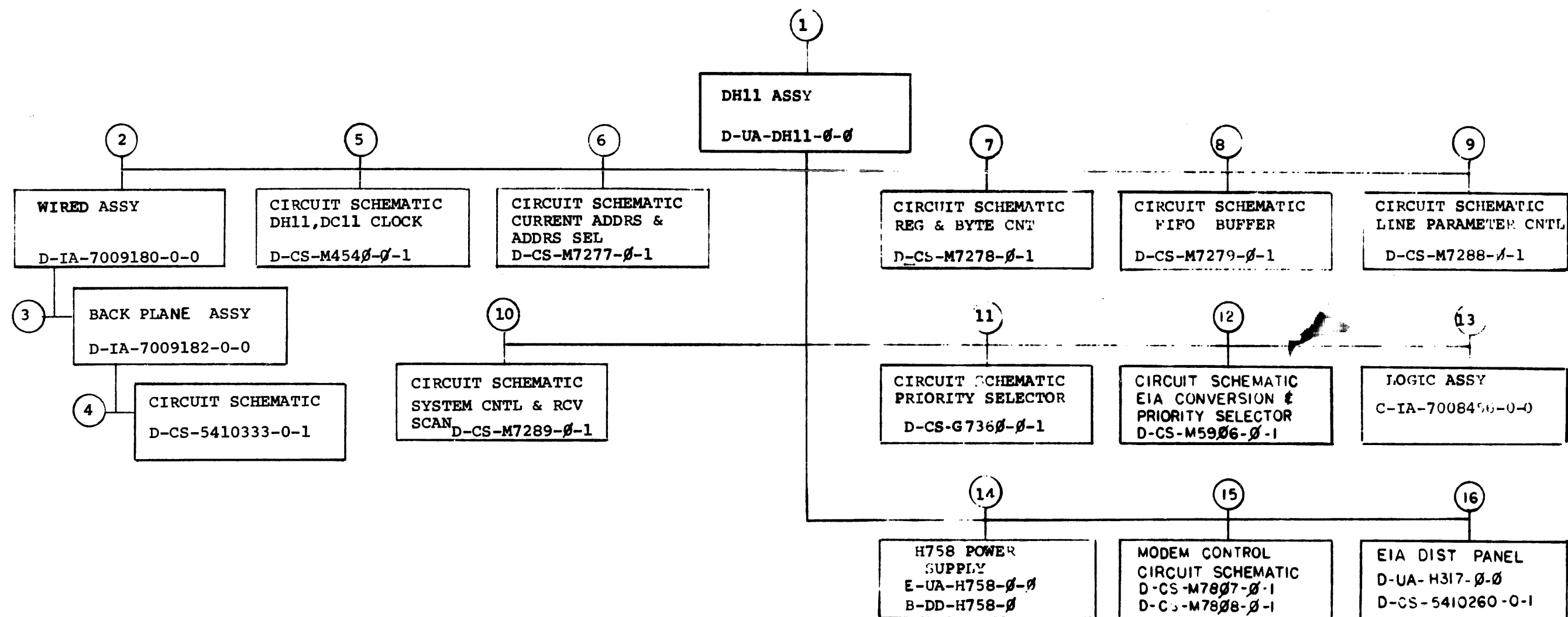




TITLE	SIZE	CODE	NUMBER	REV
16 LINE MUX DIST PANEL & 115V PS PROG LINE SPEEDS	5	B DD	DH11-0	N

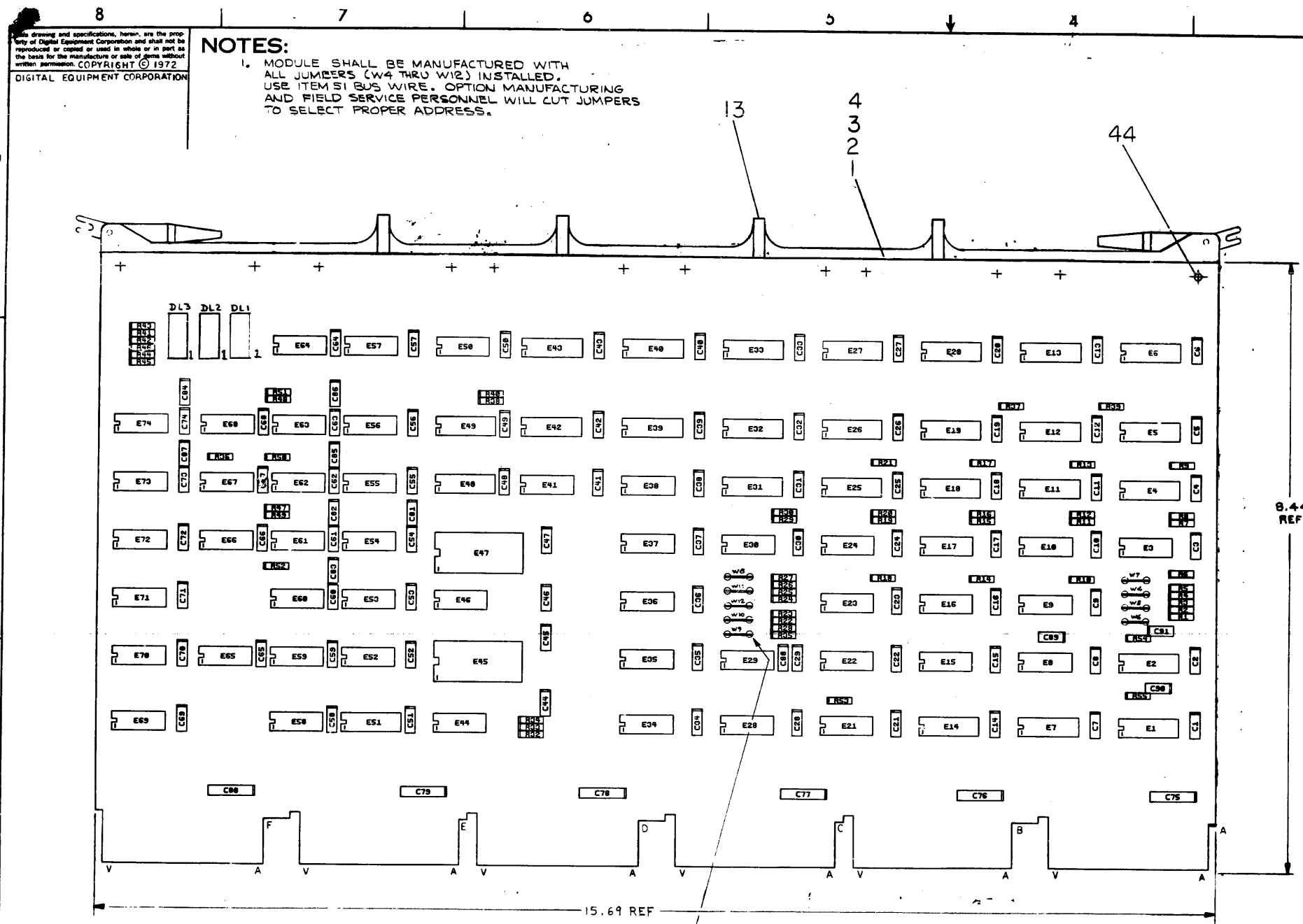
CUSTOMER PRINT SET				ELECTRICAL							CUSTOMER PRINT SET				ELECTRICAL							
A	B			MFG. SET	FIND NO.	DRAWING NO.	REV	NO OF SHT	DESCRIPTION	OPTION NO./FILE DATE	A	B			MFG. SET	FIND NO.	DRAWING NO.	REV	NO OF SHT	DESCRIPTION	OPTION NO./FILE DATE	
X	X				1	D-UA-DH11-0-0	E	14	UNIT ASSY (DH11)								3	D-IA-7009182-0-0		1	BACK PLANE ASSY	
	X					D-BD-DH11-0-16	*	2	MODEM CONTROL BLOCK DIAGRAM													
X	X					D-MU-DH11-0-3	D	1	MODULE UTILAZATION													
X	X					A-PL-DH11-0-3	D	1	MODULE UTILIZATION (PL)													
X						D-BD-DH11-0-4	*	1	DM11-BB BLOCK DIAGRAM													
X	X					A-SP-DH11-0-5	B	25	ENGINEERING SPEC		X	X				4	D-CS-5410333-0-1	#	1	CIRCUIT SCHEMATIC (BACK PNL)		
X	X					A-AL-DH11-0-6	D	1	ACCESSORY LIST								K-CO-5410333-0-4		1	X-Y COORDINATE HOLE LOCATION		
X	X					A-SL-DH11-0-7	A	2	SOFTWARE LIST								D-AH-5410333-0-5		1	ASSY DRILLING HOLE LOCATION		
X	X					D-BS-DH11-0-8	A	5	MULTIPLE UART CARD LINE 0-7								B-MH-5410333-0-6		1	MODULE ECO HISTORY		
X	X					D-BS-DH11-0-9	A	5	MULTIPLE UART CARD LINE 8-15													
X						D-MU-DM11-A-3	#	1	MODULE UTILIZATION (DIST PNL)													
X						C-IC-DM11-A-4	#	1	INTERCONNECTION (DM11)													
C						K-WL-DM11-5	#	1	WIRE LIST (DIST PNL)													
X						D-BS-DM11-A-6	#	2	DM11-DB TRANSMIT & RECEIVE													
X						D-IC DM11-A-9	#	2	DM11-DA CONNECTOR CARDS		X	X				6	D-CS-M7277-0-1	#	6	CIRCUIT SCHEMATIC (CURRENT ADDRS)		
X	X					C-IA-BC08S-0-0	#	1	I/O CABLE ASSY								K-CO-M7277-0-4		1	X-Y COORDINATE HOLE LOCATION		
X						D-IA-7008493-0-0	#	1	POWER HARNESS								D-AH-M7277-0-5		1	ASSY DRILLING HOLE LOCATION		
	X					C-IA-BC08R-0-0	#	1	MODEM I/O CABLE ASSY.								B-MH-M7277-0-6		1	MODULE ECO HISTORY		
X	X					B-CS-M401-0-1	#	1	VARIABLE CLOCK (M401)													
X						C-CS-W404-0-1	#	1	DTR JUMPER													
X	X					B-CS-M405-0-1	#	1	CRYSTAL CLOCK (M405)													
X						C-CS-M594-0-1	#	1	EIA LEVEL CONVERTER													
X						D-CS-M596-0-1	#	2	TTY 20 MA CONVERTER		X	X				7	D-CS-M7278-0-1	#	8	CIRCUIT SCHEMATIC (REG&BYTE CNT)		
X	X					D-CS-M7821-0-1	#	1	INTERRUPT CONTROL								K-CO-M7278-0-4		1	X-Y COORDINATE HOLE LOCATION		
X	X					D-CS-M796-0-1	#	1	UNIVUS MASTER CONTROL (M796)								D-AH-M7278-0-5		1	ASSY DRILLING HOLE LOCATION		
X	X					C-CS-M920-0-1	#	1	INTERNAL BUS CONN (M920)								B-MH-M7278-0-6		1	MODULE ECO HISTORY		
X						D-CS-M971-0-1	#	1	CABLE INTERFACE													
X						C-CS-M973-0-1	#	1	TTY CABLE CONNECTOR													
X						B-CS-M974-0-1	#	1	DM11 MAINTENANCE JUMPER													
	X					D-CS-H861-0-1	#	1	H861 TEST CONNECTOR													
		X				A-SP-DH11-0-10	B	40	DH11 TEST PROCEDURE													
X	X					A-SI-DH11-0-11	A	28	DH11 MODULE TEST PROCEDURE		X	X				8	D-CS-M7279-0-1	#	3	CIRCUIT SCHEMATIC (FIFO BUFFER)		
X	X					D-BD-DH11-0-12	C	3	DH11 UNIBUS INTERFACE								K-CO-M7279-0-4		1	X-Y COORDINATE HOLE LOCATION		
X	X					C-IC-DH11-0-13	B	2	INTERCONNECTION DH11								D-AH-M7279-0-5		1	ASSY DRILLING HOLE LOCATION		
X						D-UA-EC01R-0-0	#	1	CABLE CARD ASSY								B-MH-M7279-0-6		1	MODULE ECO HISTORY		
X	X					D-CS-G727-0-1	#	1	GRANT CONTINUITY CARD													
		X				A-AP-DH11-0-14	B	7	ACCEPTANCE PROCEDURE													
X	X					D-BS-DH11-0-15	*	2	FIFO BUFFER (M7279)													
X	X					D-IA-7009561-0-0	#	1	DH11 PWR HARNESS													
	X					D-CS-H315-0-1	#	1	H315 MODEM TEST CONNECTOR													
	X					C-AU-H8611	#	1	M5906 TEST CONNECTOR													
X	X				2	D-IA-7009180-0-0	#	1	WIRED ASSY (DH11)													
C	C					K-WL-DH11-0-2	C	1	WIRE LIST													
						A-WT-7009180-0	#	1	AWT REVISION STATUS													
CUSTOMER PRINT SET CODES				X = PRINT OF DOCUMENT INCLUDED IN PRINT SET C = INCLUDES ALL PRINTS INDICATED ON DOCUMENT S = CONFIDENTIAL AUTHORIZED SIGNATURE REQUIRED							TITLE 16 LINE MUX DIST PANEL & 115V PS PROG LINE SPEEDS				SHEET 3 OF 5		SIZE B	CODE DD	NUMBER DH11-0		REV N	

PAGE REVISION CONTROL SHEET

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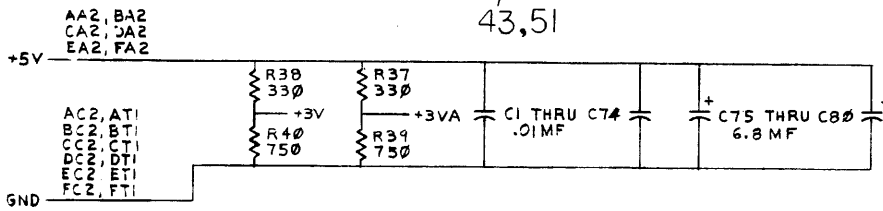
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DRN	12-7-72	DATE
CHK'D	12-7-72	DATE
ENG	12-7-72	DATE
PROJ. ENG.	12-7-72	DATE
PRG'D	12-7-72	DATE
NEXT HIGHER ASSY.		
B-DD-DH11-Ø		
SCALE	1	OF
SHEET	1	OF
TITLE		
CURRENT ADDRESS & ADDRESS SELECT		
SIZE	CODE	NUMBER
B	CS	M7277-Ø-1
DIST.		REV.
		M



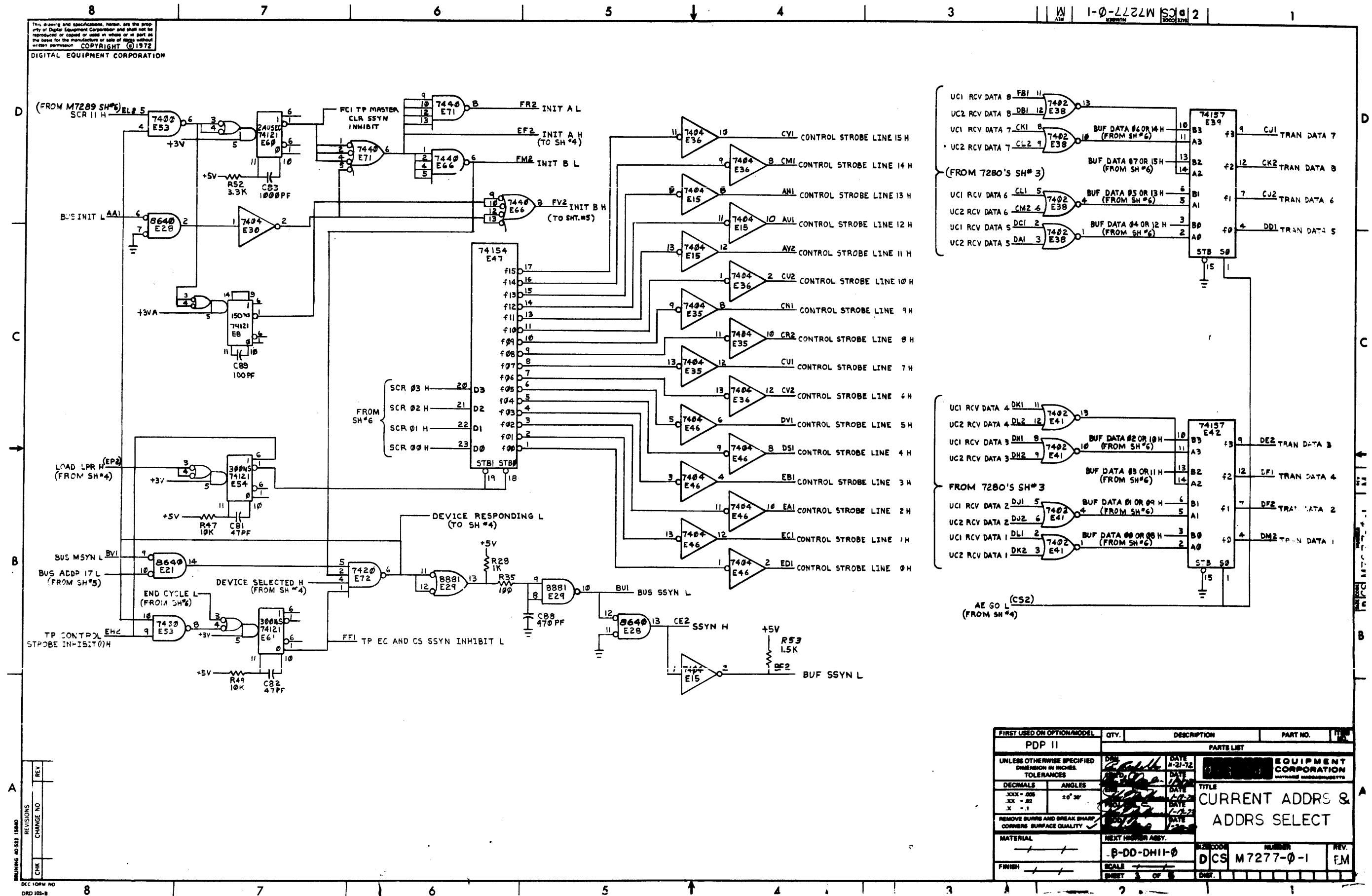
NOTES:
1. MODULE SHALL BE MANUFACTURED WITH ALL JUMPERS (W4 THRU W12) INSTALLED. USE ITEM 51 BUS WIRE. OPTION MANUFACTURING AND FIELD SERVICE PERSONNEL WILL CUT JUMPERS TO SELECT PROPER ADDRESS.

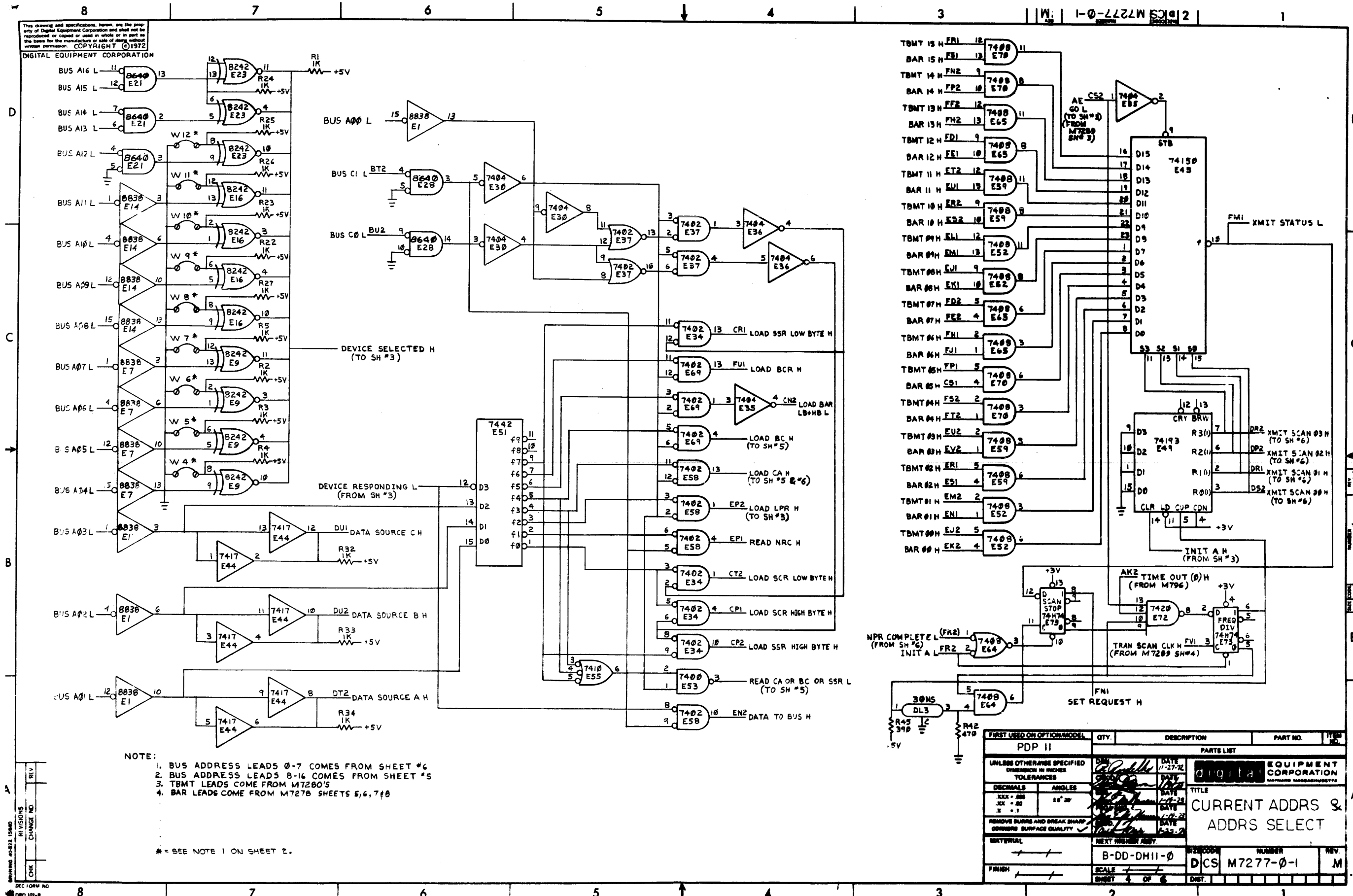
DEC 74157	8	16
DEC 7489	8	16
DEC 74150	12	24
DEC 7442	8	16
DEC 74193	8	16
DEC 74154	12	24
DEC 864	1	8
IC TYPE	GND	+5V
GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY. EXCEPTIONS ARE STATED ABOVE.		
IC PIN LOCATIONS		



W: 1-0-222W SC 2		1
	X-Y COORDINATE HOLE LOCATION	K-C0-M7277-P-4
	ASSY/DRILLING HOLE LAYOUT	D-AH-M7277-P-5
	ECO MODULE HISTORY	B-WH-M7277-P-6
1	ETCHED CIRCUIT BOARD	5010246
4	C84, C86, C90, C91	CAP 10.0 MMF 100V 5%
1	C85	CAP 15.0 MMF 100V 5%
2	C81, C82	CAP 47.0 MMF 100V 5%
2	C83, C 89	CAP 100.0 MMF 100V 5%
1	C86	CAP 470.0 MMF 100V 5%
1	C83	CAP 1000.0 MMF 100V 5%
74	C1 THRU C74	CAP .01 MF 100V 20% DISC
8	E75 THRU C80	CAP 8.8 MF 35V 10% S.TANT
1		HANDLE MODULE
1	R35	RES 100 OHMS 1/4W 5%
2	R37, R38	RES 330 OHMS 1/4W 5%
3	R44, R45, R46	RES 390 OHMS 1/4W 5%
3	R41, R42, R43	RES 470 OHMS 1/4W 5%
33	R1 THRU R38, R32, R33, R34	RES 1K OHMS 1/4W 5%
1	R36	RES 3K OHMS 1/4W 5%
1	R52	RES 3.3K OHMS 1/4W 5%
5	R47 THRU R51	RES 10K OHMS 1/4W 5%
2	R39, R40	RES 750 OHMS 1/4W 5%
3	DL1, DL2, DL3	DELAY LINE 30NS
1	E53	I.C. DEC 7400
1	E55	I.C. DEC 7410
1	E72	I.C. DEC 7420
2	E68, E71	I.C. DEC 7440
8	E34, E37, E38, E41, E50, E57, E58, E59	I.C. DEC 7402
2	E31, E70	I.C. DEC 8640
2	E56, E73	I.C. DEC 74H74
10	E3, E10, E17, E24, E30, E35, E36, E48, E74, E15	I.C. DEC 7404
1	E47	I.C. DEC 74154
2	E28, E29	I.C. DEC 8881
3	E9, E16, E23	I.C. DEC 8242
1	E44	I.C. DEC 7417
8	E5, E12, E18, E26, E32, E48	I.C. DEC 74183
1	E51	I.C. DEC 7442
1	E45	I.C. DEC 74150
5	E52, E59, E84, E85, E70	I.C. DEC 7408
8	E54, E80, E81, E82, E83, E87, E86, E8	I.C. DEC 74121
5	E4, E11, E18, E25, E31	I.C. DEC 7488
10	E8, E13, E20, E27, E33, E39, E40, E42, E43, E48	I.C. DEC 74157
18		SPLIT LUG
12		EYELET (MS-4-7)
3	E1, E7, E14	I.C. DEC 8838
1	R53	RES. 1.5K 1/4W 5%
A/R		TUBING, THINWALL WHT TFE
1	E2	IC, DEC 96C2
A/R		WIRE, 30 AWG INSULATED
2	R54, R55	RES 7.5K OHMS 1/4W 5%
A/R	W4 THRU W12	WIRE 22 AWG BUS

FIRST USED ON OPTION MODEL		PDP 11	
ETCH BOARD REV		E	
PARTS LIST		TITLE	
CURRENT ADDR & ADDR SELECT		DCE M7277-0-1	
NEXT HIGHER ASSY		B-DD-DH11-0	
SCALE		NONE	
SHEET		2 OF 3	
SEMICONDUCTOR CONVERSION CHART			
DEC NO.	EIA NO.	DEC NO.	EIA NO.





NOTE:
1. BUS ADDRESS LEADS 0-7 COMES FROM SHEET #6
2. BUS ADDRESS LEADS 8-16 COMES FROM SHEET #5
3. TBMT LEADS COMES FROM M7280'S
4. BAR LEADS COMES FROM M7276 SHEETS 5,6,7 & 8

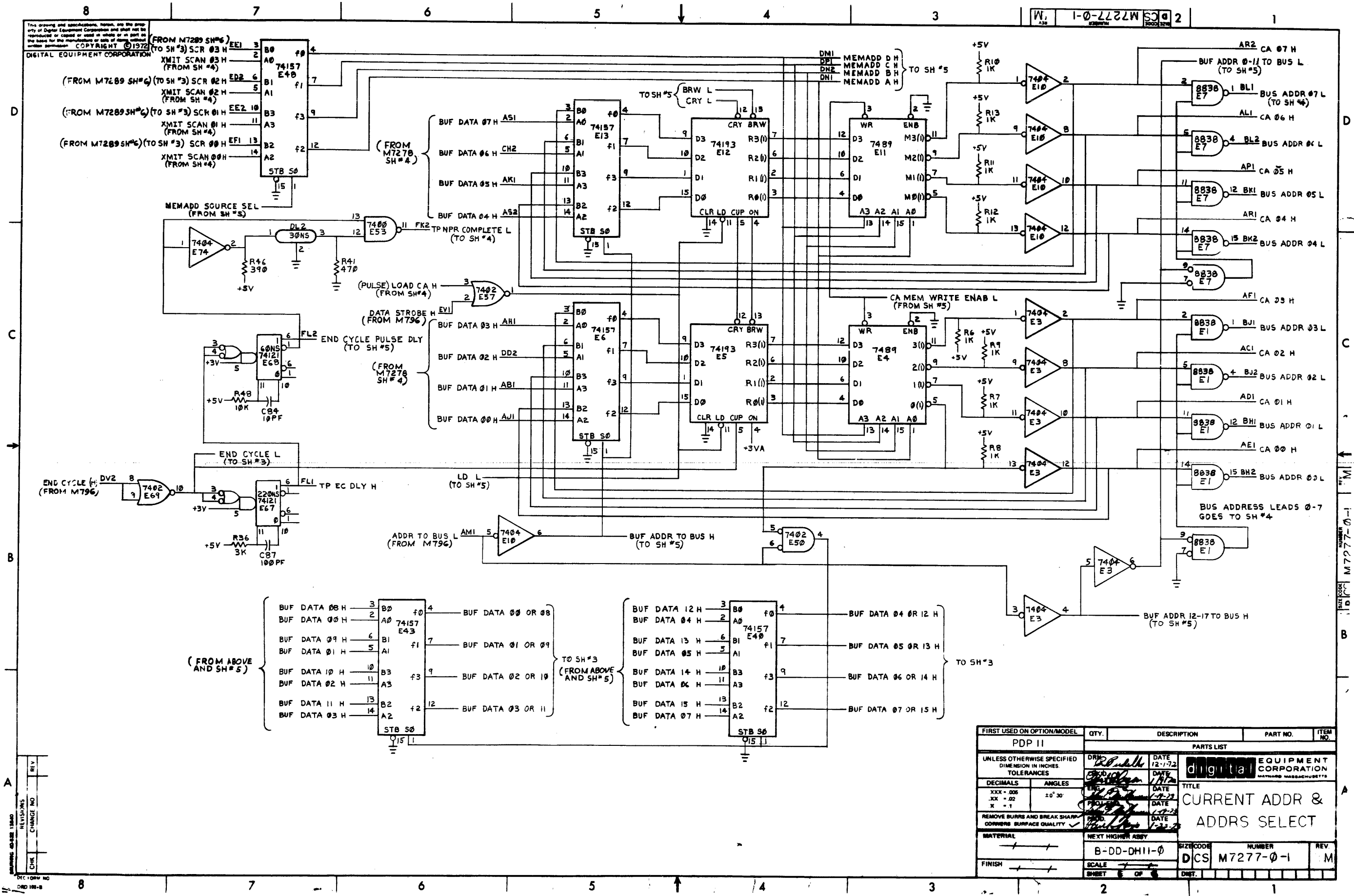
* = SEE NOTE 1 ON SHEET 2.

FIRST USED ON OPTION MODEL		QTY.	DESCRIPTION	PART NO.	ITEM NO.
PDP 11					
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES		DATE 11-27-72	DATE 11-27-72	EQUIPMENT CORPORATION BAYVIEW MAGNACHUYETTE	
DECIMALS	ANGLES	DATE 11-27-72	DATE 11-27-72	TITLE	
.XXX - .000 .XX - .00 .X - .1	5° 30'	DATE 11-27-72	DATE 11-27-72	CURRENT ADDR & ADDR SELECT	
REMOVE BURRS AND BREAK SHARP EDGES SURFACE QUALITY		DATE 11-27-72	DATE 11-27-72		
MATERIAL	NEXT HIGHER REV.	DATE 11-27-72	DATE 11-27-72		
FINISH	B-DD-DH11-0	DATE 11-27-72	DATE 11-27-72		
SCALE		DATE 11-27-72	DATE 11-27-72		
SHEET 4 OF 6		DATE 11-27-72	DATE 11-27-72		
		DATE 11-27-72	DATE 11-27-72		

DIGITAL EQUIPMENT CORPORATION



A



FIRST USED ON OPTION/MODEL		QTY.	DESCRIPTION	PART NO.	ITEM NO.
PDP 11					
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES		DATE	PARTS LIST		
DECIMALS	ANGLES	12-17-72	digital EQUIPMENT CORPORATION MILFORD, MASSACHUSETTS		
XXX - .005	±0°30'	DATE			
.XX - .02		17-72			
X - .1		DATE			
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY		DATE	TITLE CURRENT ADDR & ADDRS SELECT		
		DATE			
MATERIAL		NEXT HIGHER ASSY		SIZE CODE	NUMBER
				B-DD-DH11-0	DCS M7277-0-1
FINISH		SCALE	REV.		
		SHEET 5 OF 5	M		

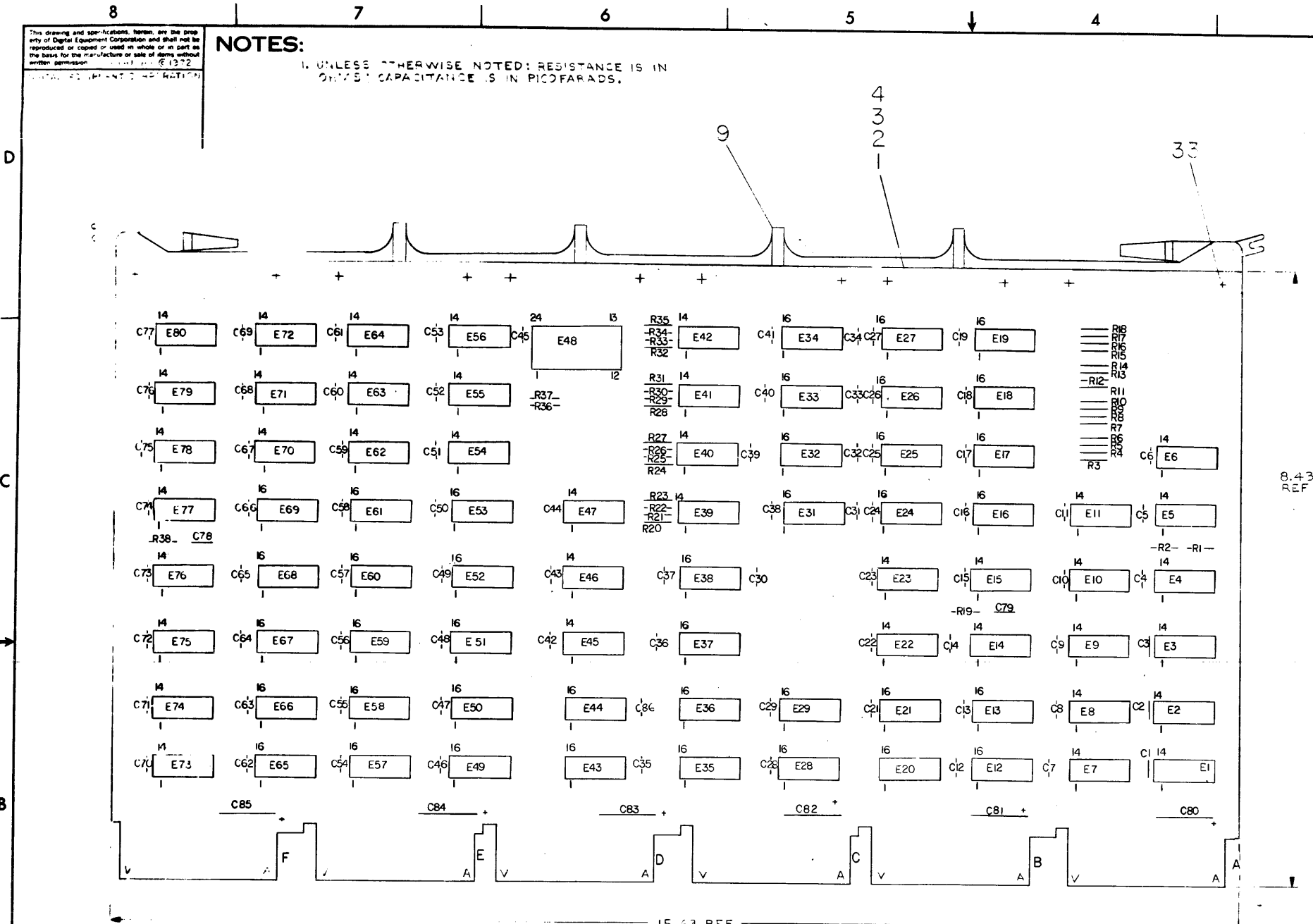
PAGE REVISION CONTROL SHEET

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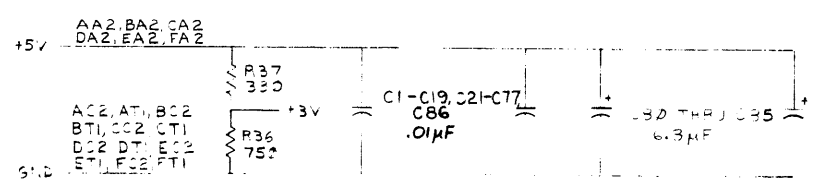
DRN.	DATE
CHKD.	12-15-72
ENG.	DATE
PROJ. ENG.	DATE
PROD.	DATE
1-22-73	DATE
1-22-73	DATE
NEXT HIGHER ASSY.	
B-DD-DH11-Ø	
SCALE	NONE
SHEET	1 OF 8
DIST.	
SIZE	
B	CS
NUMBER	
M7278-Ø-1	
REV.	
D	
TITLE	
REG & BYTE CNT	
digital	
EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS	



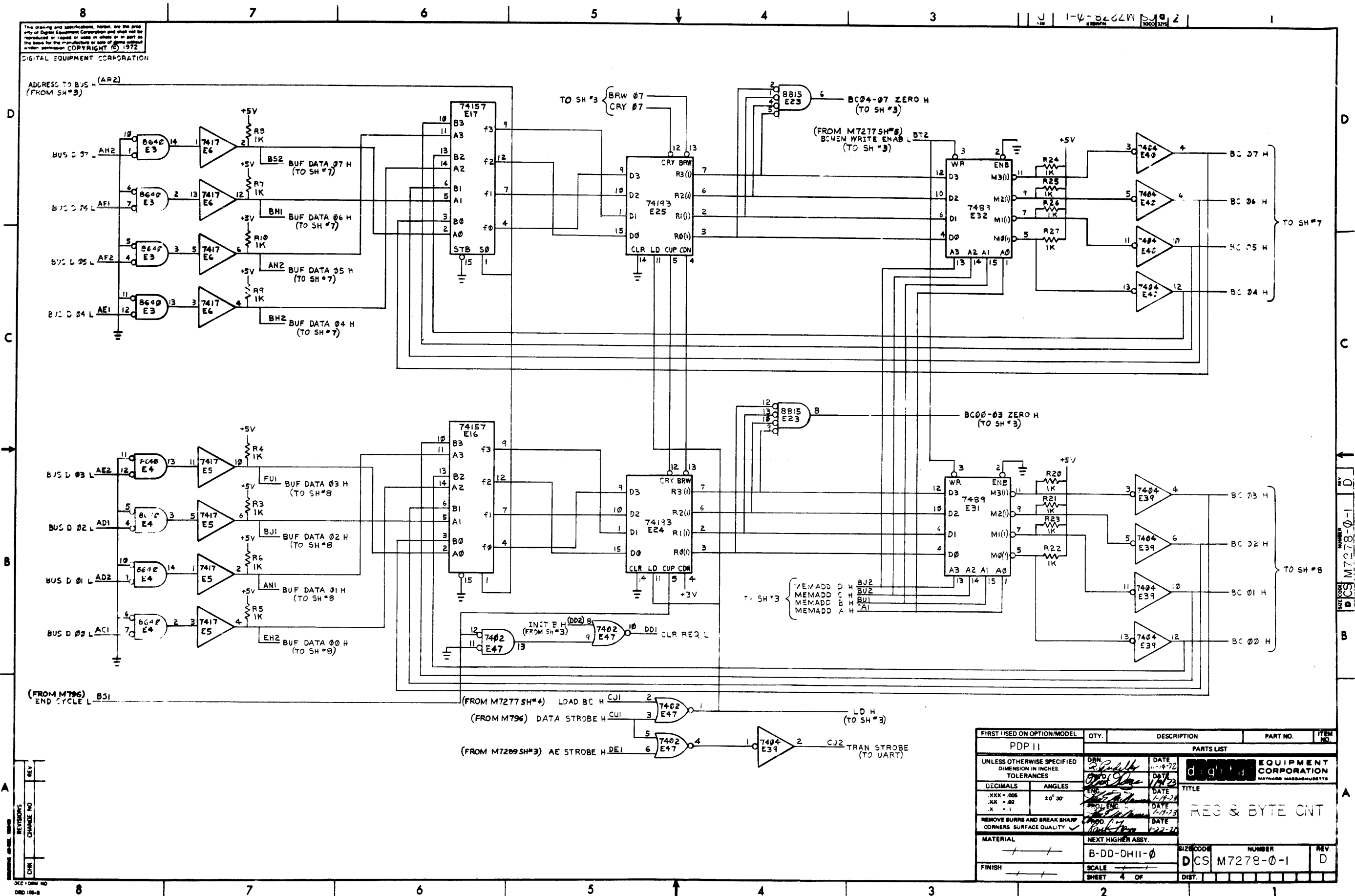
NOTES:
1. UNLESS OTHERWISE NOTED: RESISTANCE IS IN OHMS; CAPACITANCE IS IN PICOFARADS.

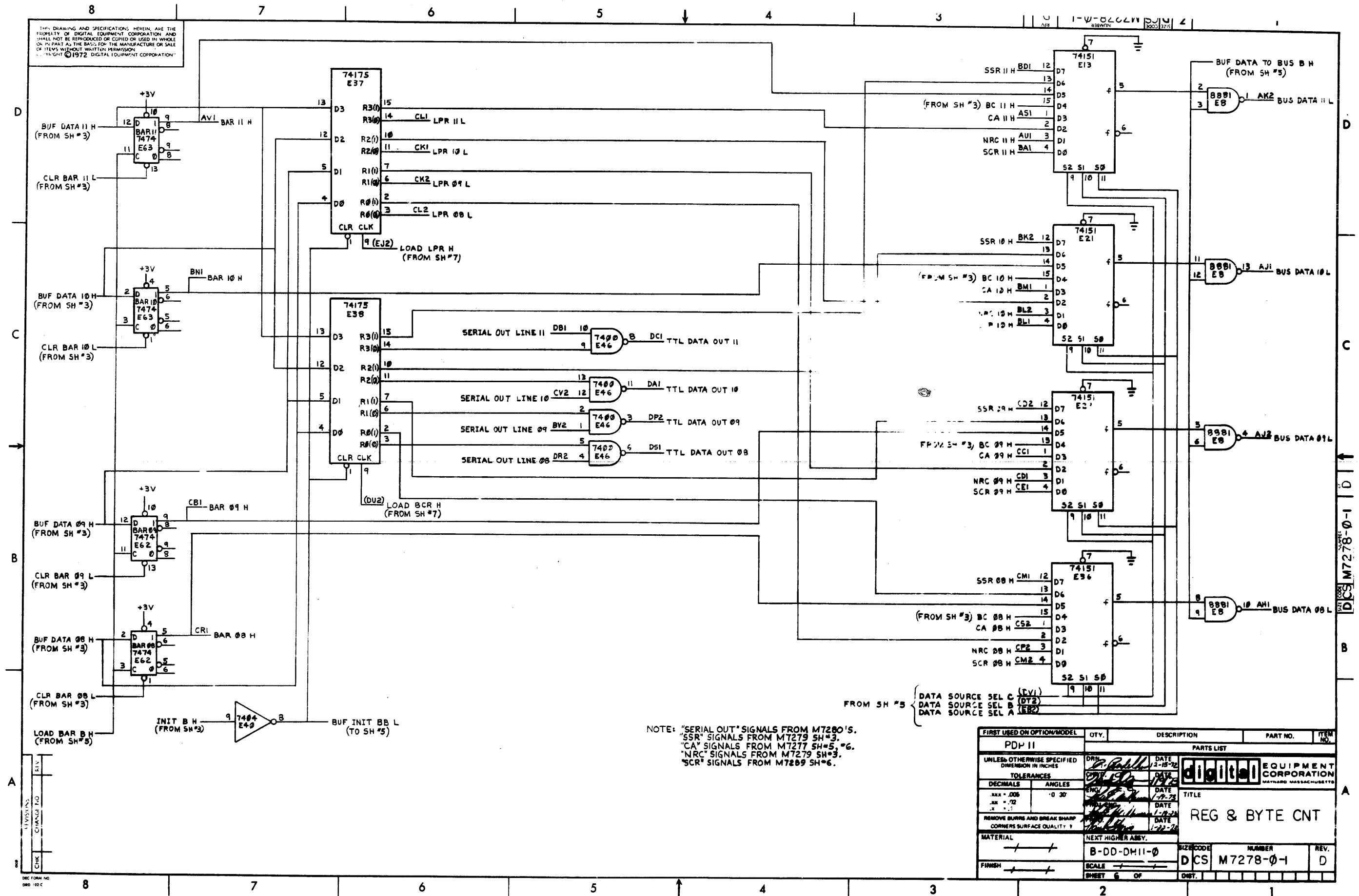
REF	REF	X-Y COORDINATE HOLE LOCATION	K-C0-M7278-B-4	1
REF	REF	ASSY/DRILLING HOLE LAYOUT	D-AH-M7278-P-5	2
1		MODULE ECO HISTORY	B-MH-M7278-B-6	3
1		ETCHED CIRCUIT BOARD	5010247	4
1	C78	CAP 1000 PF 100V ± 5% D.M.	1000042	5
77	C1-C19, C21-C77, C86	CAP .01 MF 100V ± 20% DISC	1001610	6
1	C79	CAP 27 PF 100V ± 5% D.M.	1001739	7
6	C80 THRU C85	CAP 6.8 MF 35V ± 10% S. TANT	1005308	8
1		HANDLE MODULE	1210711-2	9
1	R37	RES 330 1/4W ± 5%	1300295	10
34	R1 THRU R18, R20 THRU R35	RES 1K 1/4W ± 5%	1300365	11
1	R38	RES 1.5K 1/4W ± 5%	1300391	12
1	R19	RES 2.2K 1/4W ± 5%	1300417	13
1	R36	RES 750 1/4W ± 5%	1301401	14
8	E54, E55, E82, E83, E70, E71, E78, E79	I.C. DEC 7474	1905547	15
4	E45, E48, E75, E76	I.C. DEC 7400	1905575	16
1	E15	I.C. DEC 7420	1905577	17
1	E47	I.C. DEC 7402	1909004	18
4	E3, E4, E9, E10	I.C. DEC 7404	1911469	19
4	E39 THRU E42	I.C. DEC 7404	1909686	20
1	E48	I.C. DEC 74154	1909701	21
4	E1, E2, E7, E8	I.C. DEC 8881	1909705	22
2	E22, E23	I.C. DEC 8815	1909713	23
3	E5, E6, E11	I.C. DEC 7417	1909929	24
16	E12, E13, E20, E21, E28, E29, E35, E36, E43, E44, E49, E50, E57, E58, E65, E66	I.C. DEC 74151	1909936	25
4	E24 THRU E27	I.C. DEC 74193	1910018	26
2	E73, E74	I.C. DEC 7437	1910091	27
4	E56, E64, E72, E80	I.C. DEC 7408	1910155	28
2	E14, E77	I.C. DEC 74121	1910230	29
4	E31 THRU E34	I.C. DEC 7489	1910396	30
11	E37, E38, E51, E52, E53, E59, E60, E61, E67, E68, E69	I.C. DEC 74175	1910651	31
4	E16 THRU E19	I.C. DEC 74157	1910655	32
12		EYELET (55-4-7)	9006732	33

DEC 7451	2	24
DEC 7454	2	24
DEC 7457	2	16
DEC 7475	2	2
DEC 7478	2	2
DEC 7481	2	6
IC TYPE	GND	+5V
GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY. EXCEPTIONS ARE STATED ABOVE		
IC PIN LOCATIONS		



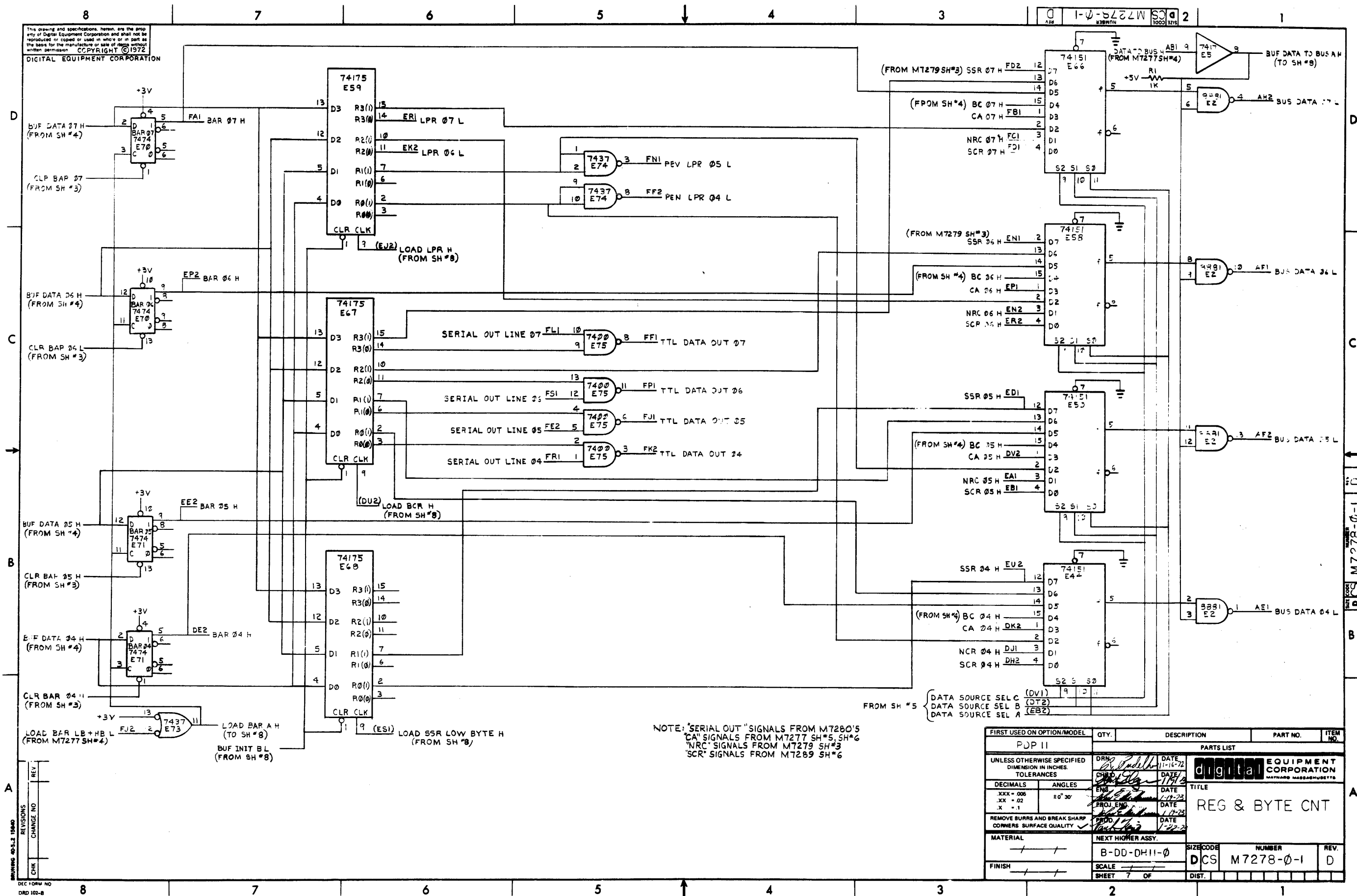
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PARTS LIST					
ETCH BOARD REV C					
FIRST USED ON OPTION MODEL PDP II					
CHK	CHANGE NO.	REV	DATE	TITLE	
				REG & BYTE CNT	
NEXT HIGHER ASSY B-DD-DH11-0					
SEMICONDUCTOR CONVERSION CHART					
DEC NO.		EIA NO.		REV.	
				D	
SHEET 2 OF 2					

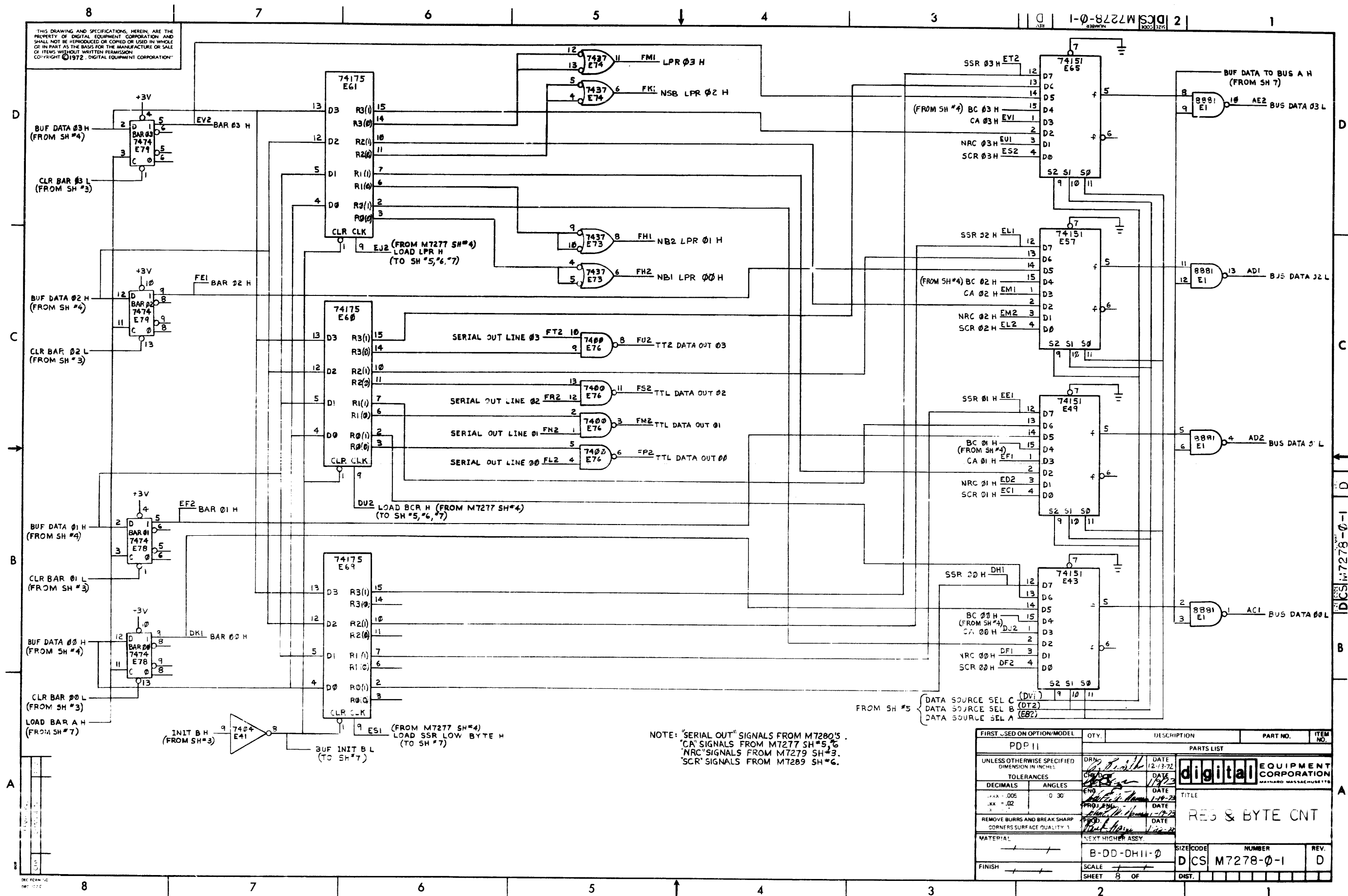


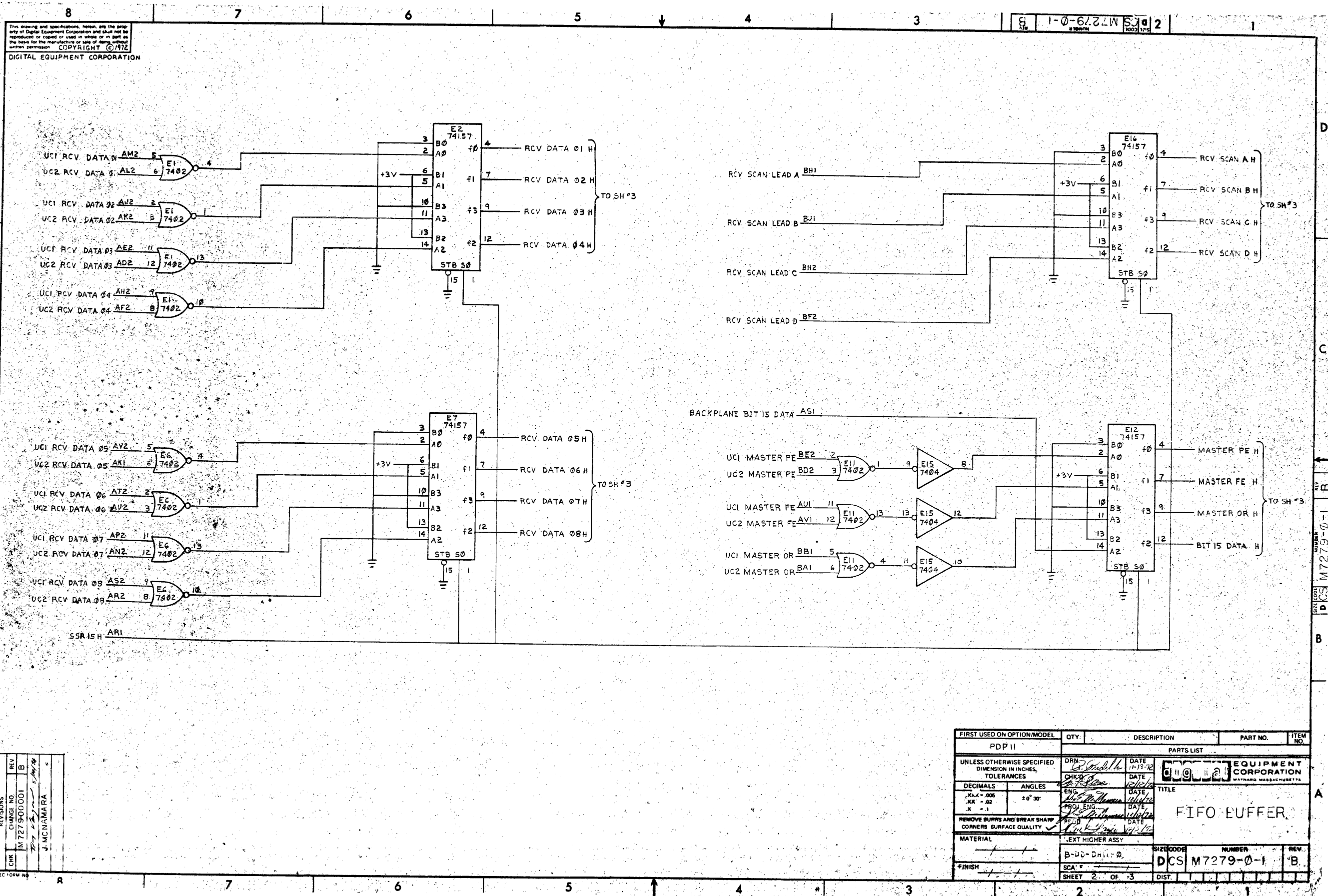


FIRST USED ON OPTION/MODEL		QTY.	DESCRIPTION	PART NO.	ITEM NO.
PDP 11					
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES		DATE 12-15-72			
TOLERANCES		DATE 1-17-73			
DECIMALS	ANGLES	DATE 1-17-73			
XXX + .005	.0 30'	DATE 1-17-73			
XX + .02		DATE 1-17-73			
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY 1		DATE 1-17-73			
MATERIAL		NEXT HIGHER ASSY.			
FINISH		B-DD-DM11-0			
SCALE		DCS M7278-0-1			
SHEET 6 OF		REV. D			

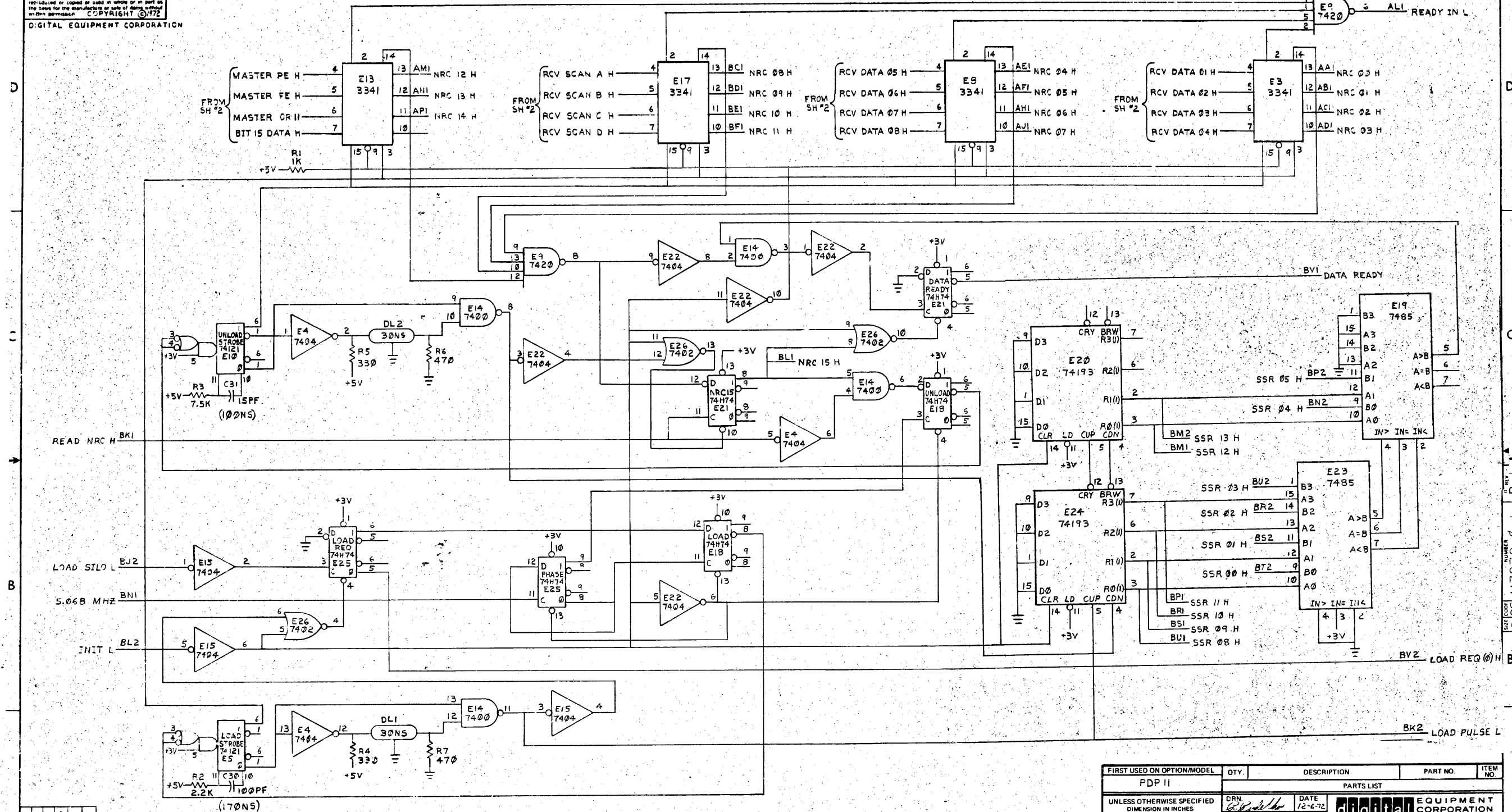
DIGITAL EQUIPMENT CORPORATION
 MAYNARD, MASSACHUSETTS







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REV	CHG	NO	DATE
1		1	12-6-72
2		2	12-6-72
3		3	12-6-72
4		4	12-6-72
5		5	12-6-72
6		6	12-6-72
7		7	12-6-72
8		8	12-6-72
9		9	12-6-72
10		10	12-6-72

DEC FORM NO. 102-B

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
PDP 11				
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES	DRN	DATE	PARTS LIST	
DECIMALS	CHK'D	DATE		
ANGLES	ENG	DATE	TITLE	
XXX - .005	PROJ. ENG.	DATE		
XX - .02	PROD. ENG.	DATE	FIFO BUFFER	
X - .1	PROD. MGR.	DATE		
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY	PROD. MGR.	DATE	SIZE CODE	
MATERIAL	NEXT HIGH: R ASSY.		NUMBER	
FINISH	B-DD-DH11-0		REV	
	SCALE		DIST.	
	SHEET			

PAGE REVISION CONTROL SHEET

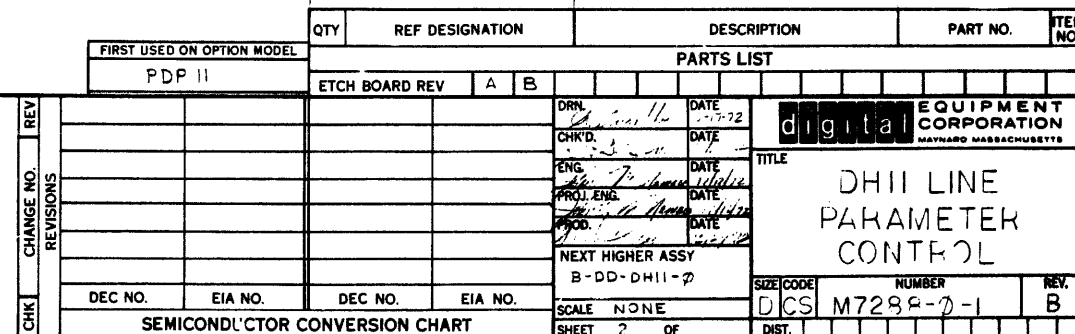
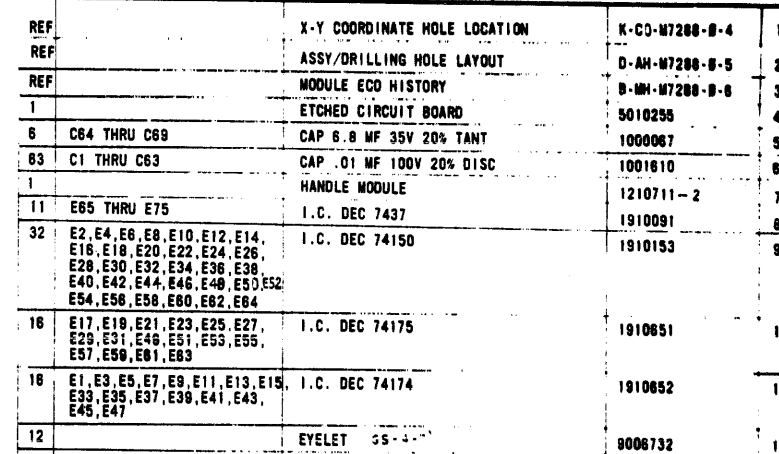
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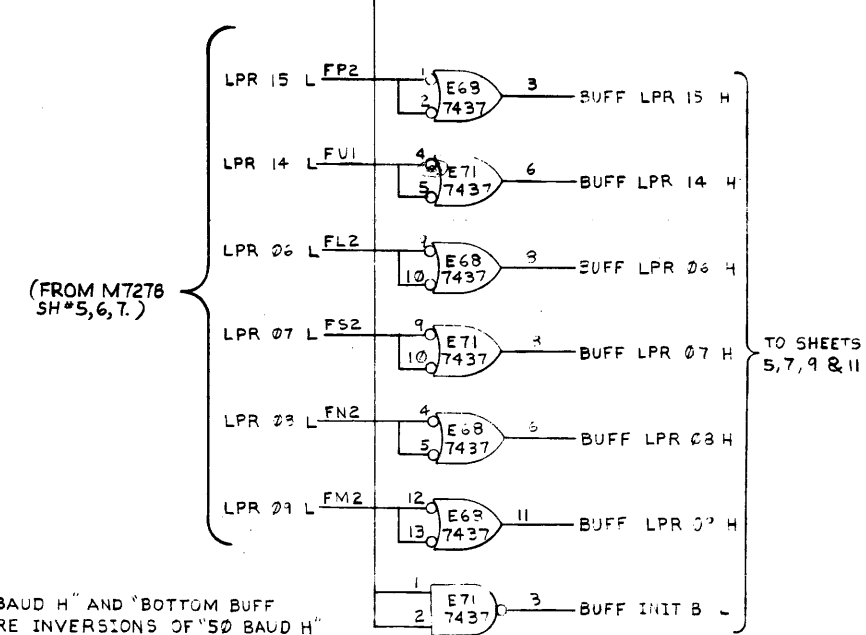
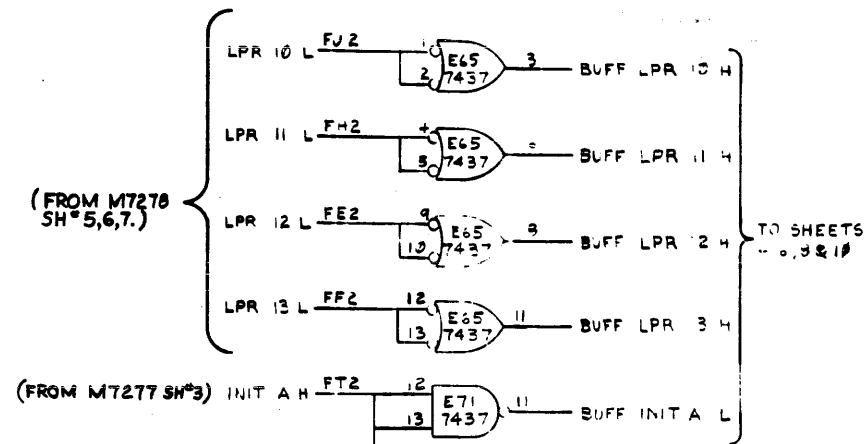
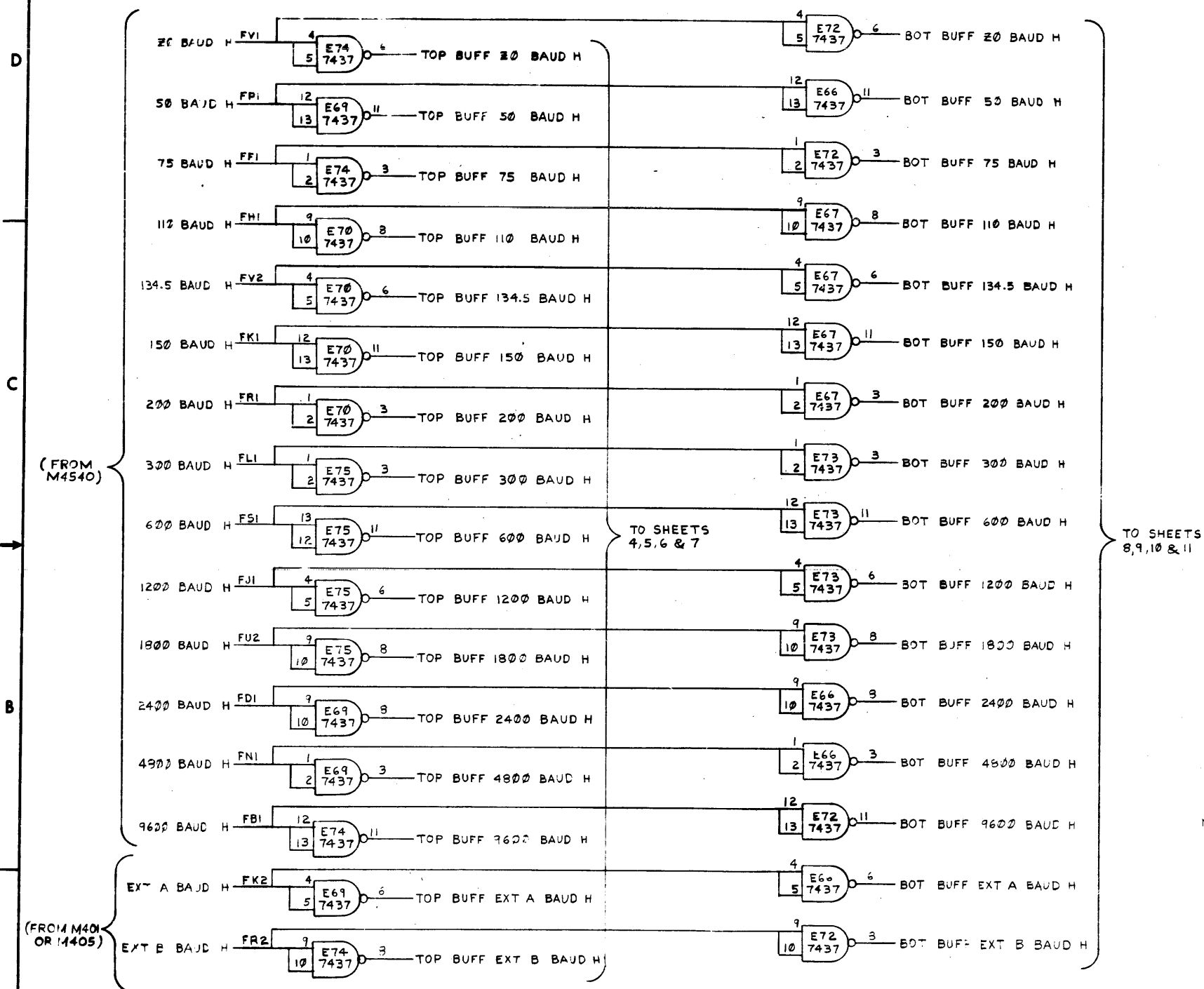
COPYRIGHT © 1972 DIGITAL EQUIPMENT CORPORATION"

DRN.	DATE	digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS
CHK'D	12-6-72	
ENG.	DATE	
PROJ. ENG.	DATE	
PROD.	DATE	
NEXT HIGHER ASSY.		TITLE DH11 LINE PARAMETER CONTROL
B-DD-DH11-Ø	SIZE	
SCALE	CODE	
SHEET 1 OF 11	DIST.	
	REV.	

NOTES:



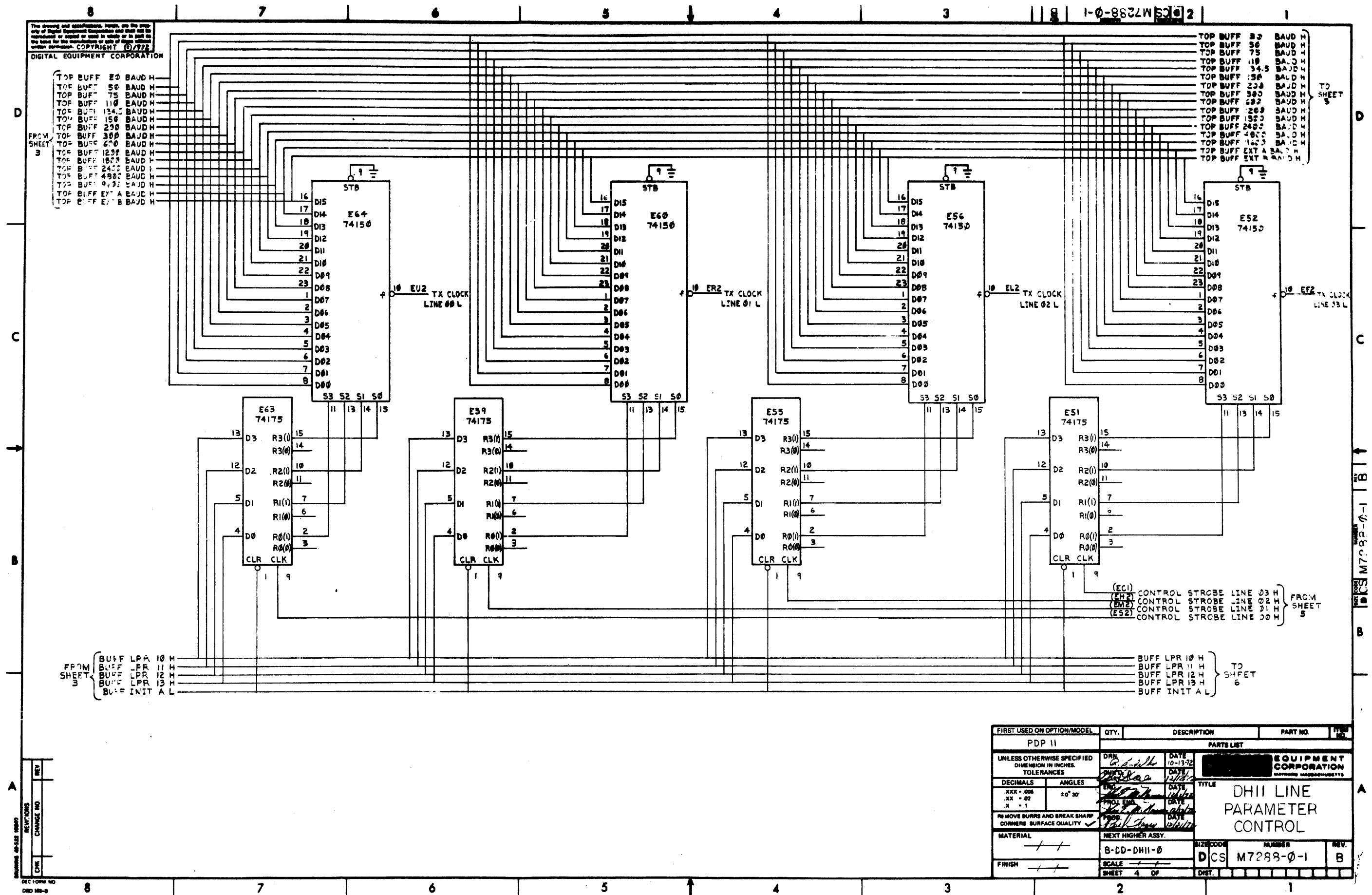
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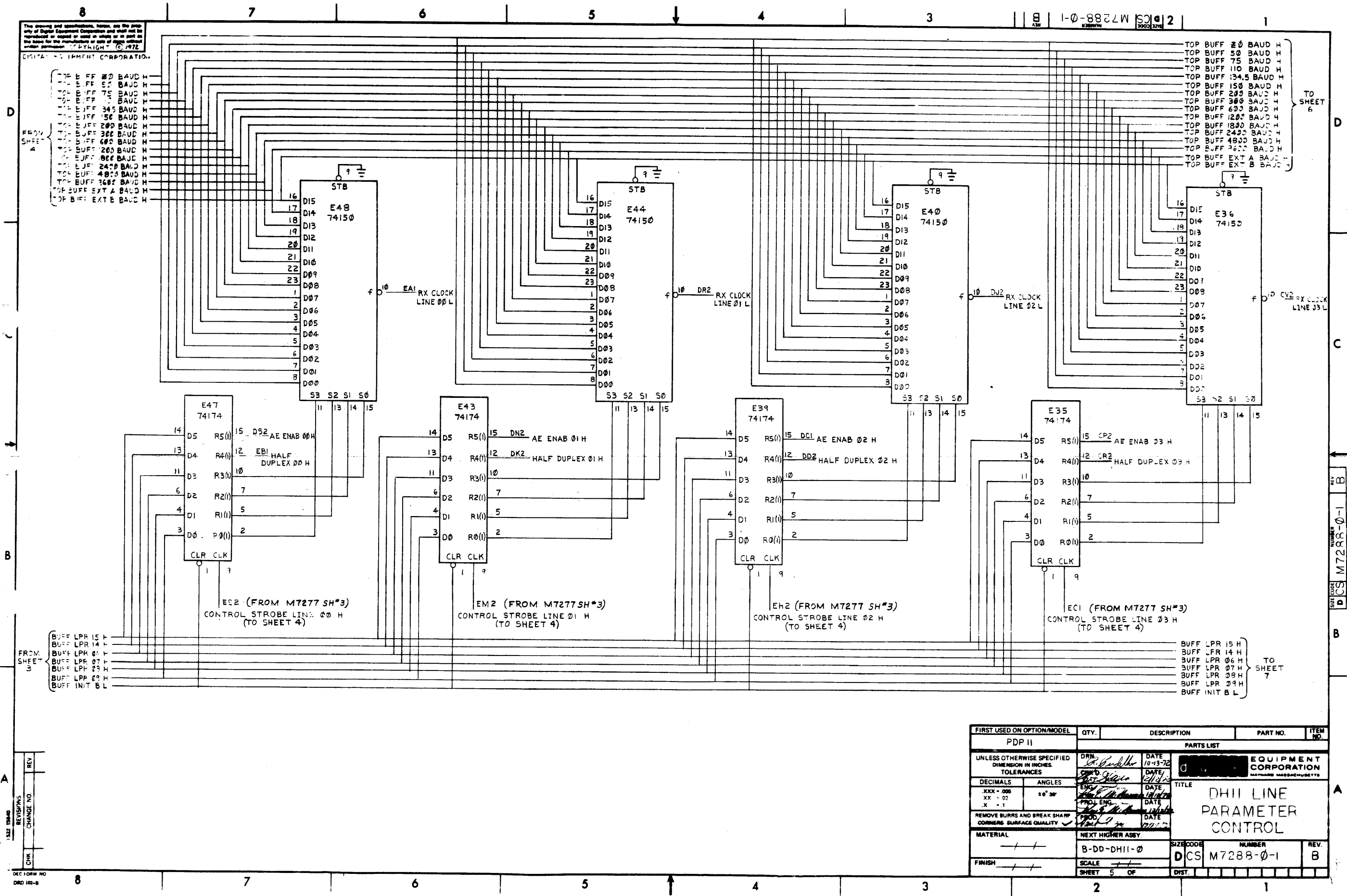
NOTE:
"TOP BUFF 50 BAUD H" AND "BOTTOM BUFF 50 BAUD H" ARE INVERSIONS OF "50 BAUD H"

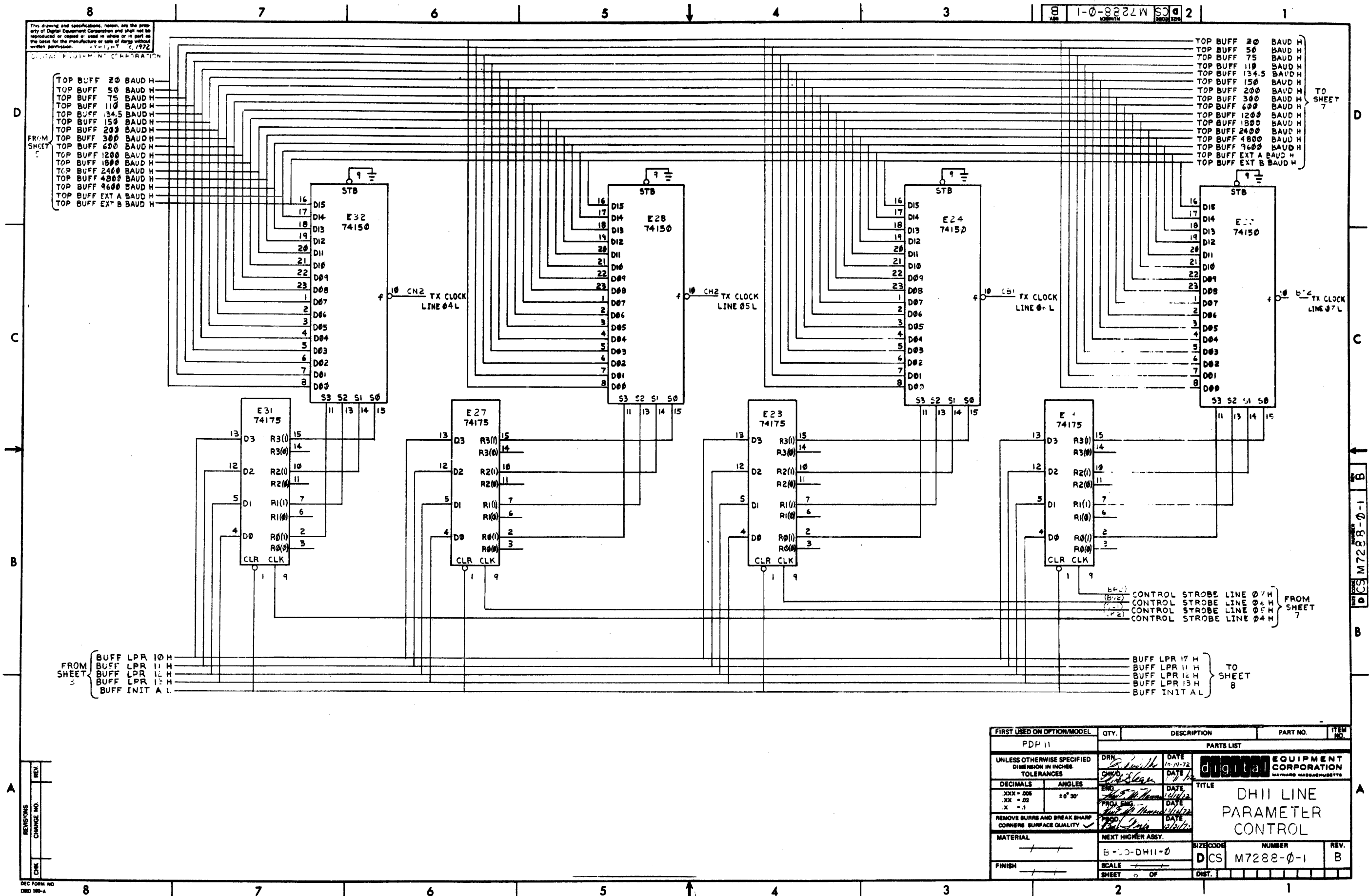
REV	CHG	NO
1	1	1

FIRST USED ON OPTION/MODEL		QTY.	DESCRIPTION	PART NO.	ITEM NO.
PDP 11					
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES		DRN	DATE	EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS	
DECIMALS	ANGLES	CHK'D	DATE	TITLE	
.XXX - .005	10° 30'	ENG	DATE	DH11 LINE PARAMETER CONTROL	
.XX - .02		PRD	DATE	SIZE CODE	
X - .1		PROD	DATE	NUMBER	
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY		NEXT HIGHER ASSY.		REV.	
MATERIAL		B-DD-DH11-0		D CS	
FINISH		SCALE		M7288-0-1	
		SHEET 3 OF		DIST.	



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TOP BUFF 50 BAUD H
TOP BUFF 50 BAUD H
TOP BUFF 75 BAUD H
TOP BUFF 110 BAUD H
TOP BUFF 134.5 BAUD H
TOP BUFF 150 BAUD H
TOP BUFF 200 BAUD H
TOP BUFF 300 BAUD H
TOP BUFF 600 BAUD H
TOP BUFF 1200 BAUD H
TOP BUFF 1800 BAUD H
TOP BUFF 2400 BAUD H
TOP BUFF 4000 BAUD H
TOP BUFF 9600 BAUD H
TOP BUFF EXT A BAUD H
TOP BUFF EXT B BAUD H

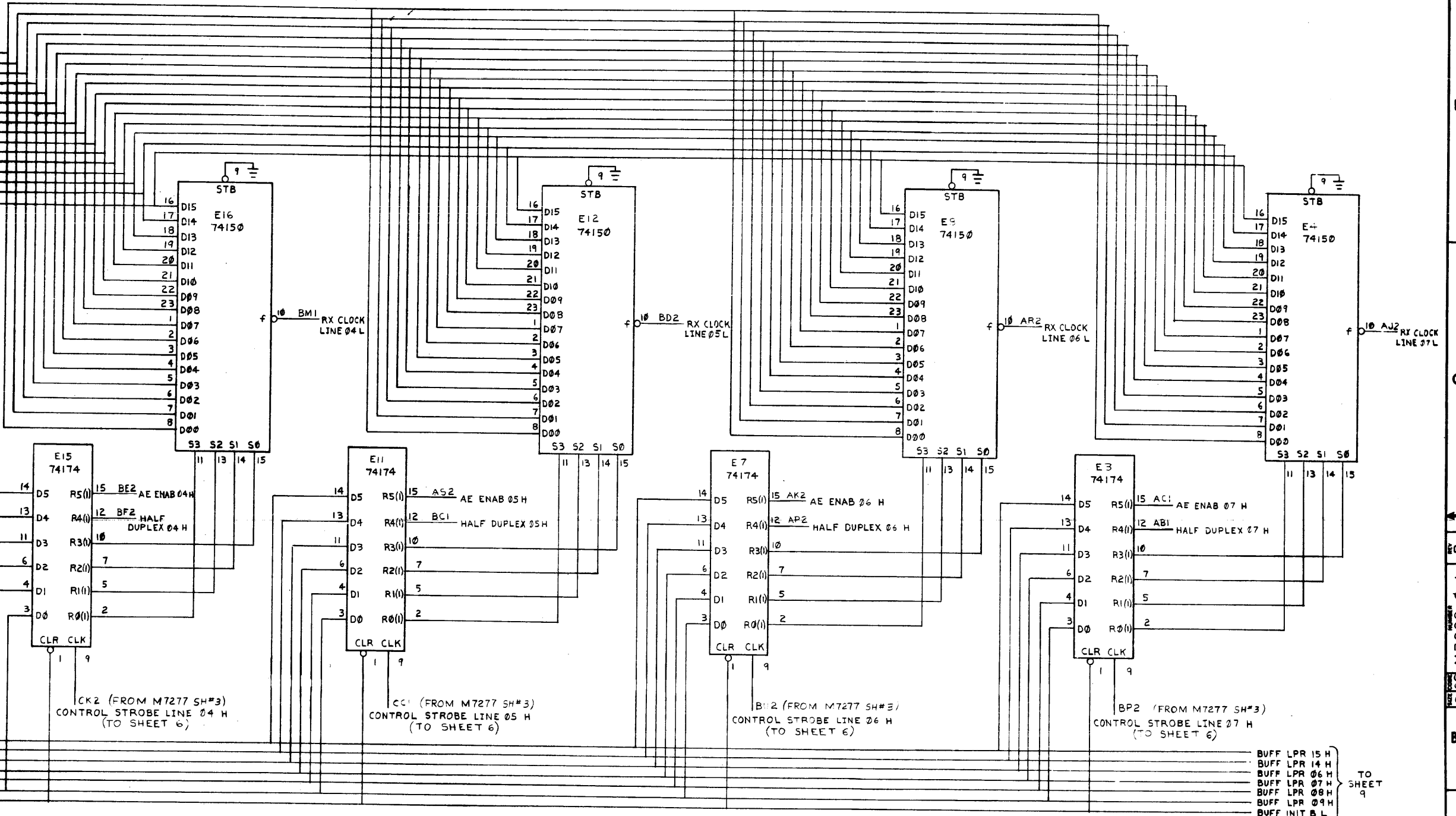
FROM SHEET 6

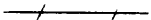
FROM SHEET 3

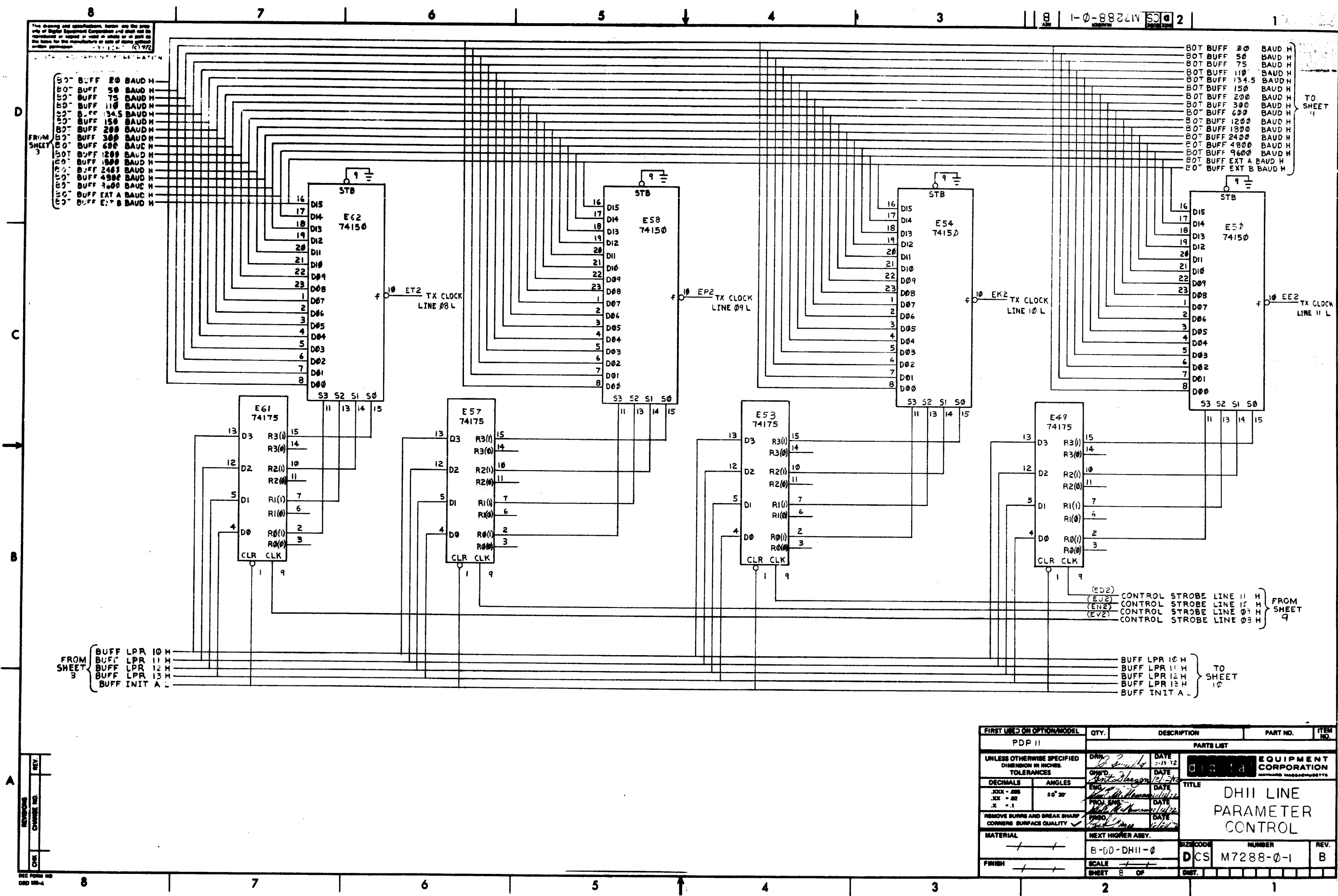
FROM SHEET 3

FROM SHEET 3

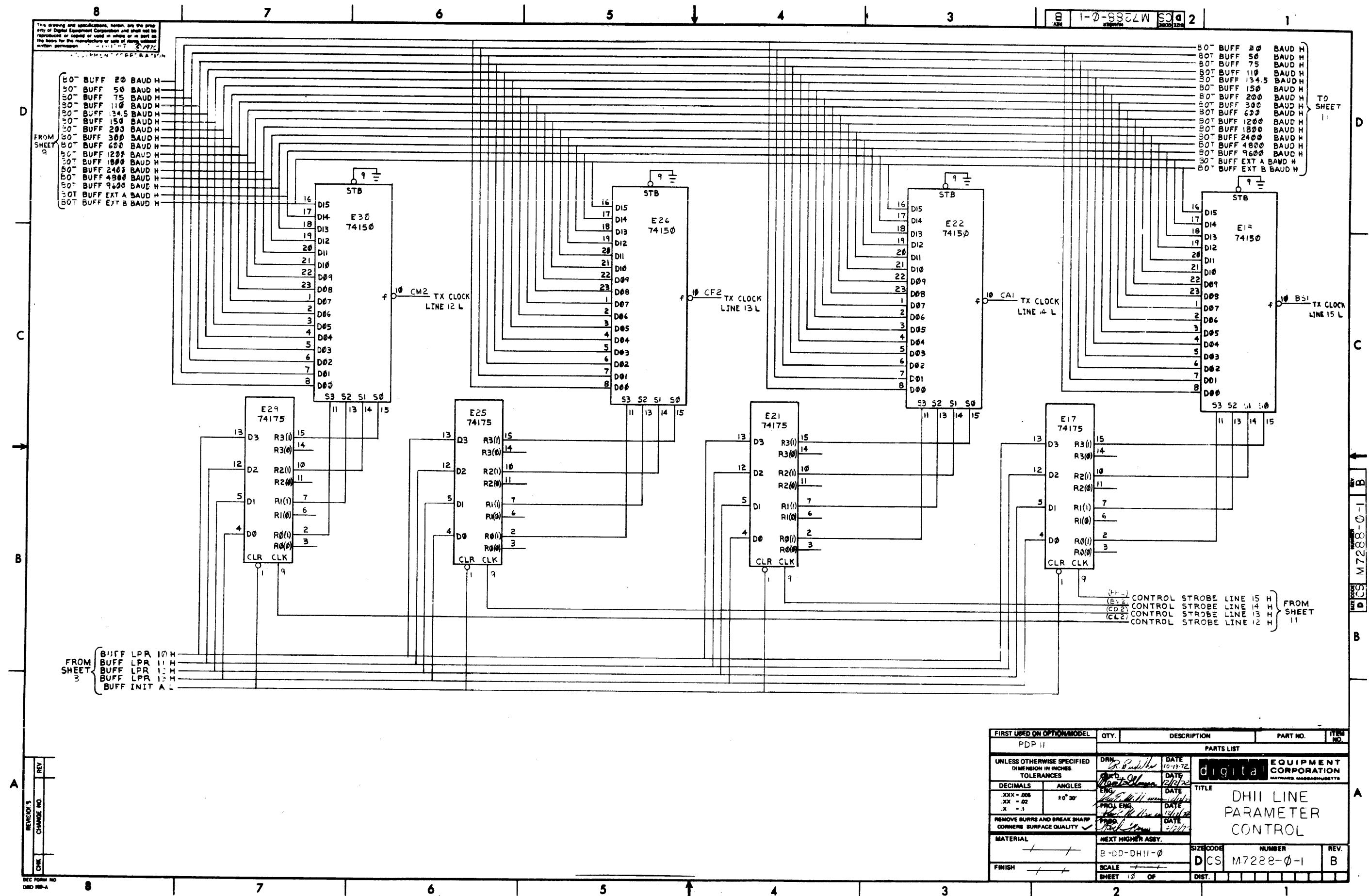
FROM SHEET 3

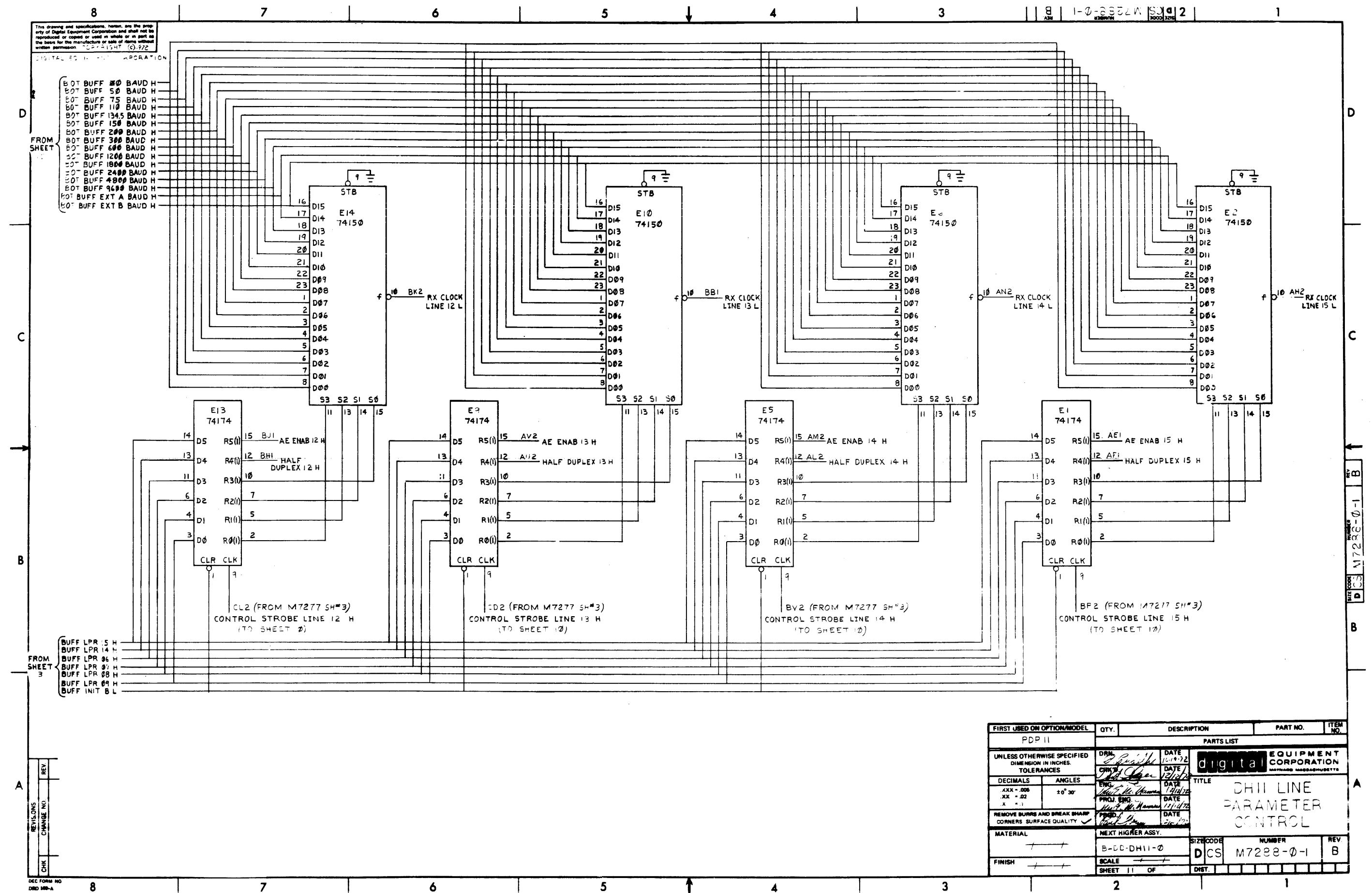


FIRST USED ON OPTION/MODEL		QTY.	DESCRIPTION	PART NO.	ITEM NO.
PDP 11		PARTS LIST			
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES		DRN	DATE	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS	
		CHK'D	DATE		
DECIMALS	ANGLES	ENG.	DATE	TITLE DH11 LINE PARAMETER CONTROL	
.XXX - .006	±0° 30'	PROF. ENG.	DATE		
XX - .02		PROD. ENG.	DATE		
X - .1			DATE		
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓					
MATERIAL		NEXT HIGHER ASSY.			
		S - 00 - DH11 - 0			
FINISH		SCALE		SIZE CODE	
		SHEET 7 OF		NUMBER	
		DST.		REV.	
				B	



FIRST USED ON OPTION/MODEL		QTY.	DESCRIPTION	PART NO.	ITEM NO.
PDP 11					
UNLESS OTHERWISE SPECIFIED DIMENSIONS IN INCHES. TOLERANCES:		DATE	DATE	EQUIPMENT CORPORATION	
DECIMALS	ANGLES	DATE	DATE	TITLE	
.XXX - .005	±0° 30'	DATE	DATE	DHII LINE	
.XX - .002		DATE	DATE	PARAMETER	
.X - .001		DATE	DATE	CONTROL	
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY		DATE	DATE	REV.	
MATERIAL		DATE	DATE	B	
NEXT HIGHER ASSY.		DATE	DATE	DCS M7288-0-1	
FINISH		DATE	DATE	SHEET 8 OF 8	





PAGE REVISION CONTROL SHEET

[illegible]

digital EQUIPMENT CORPORATION
MAYNARD MASSACHUSETTS

TITLE

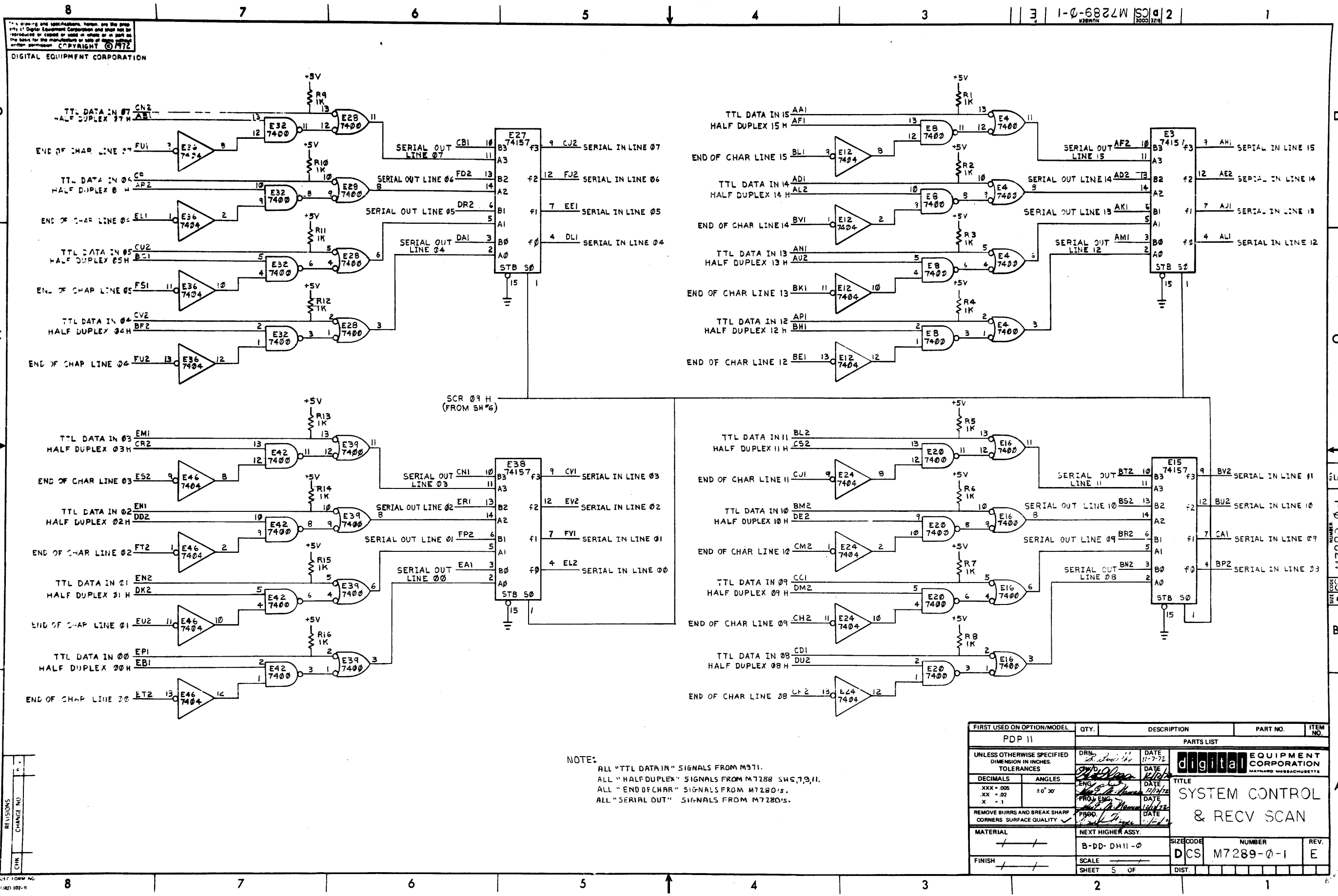
SYSTEM CONTROL
& RECV SCAN

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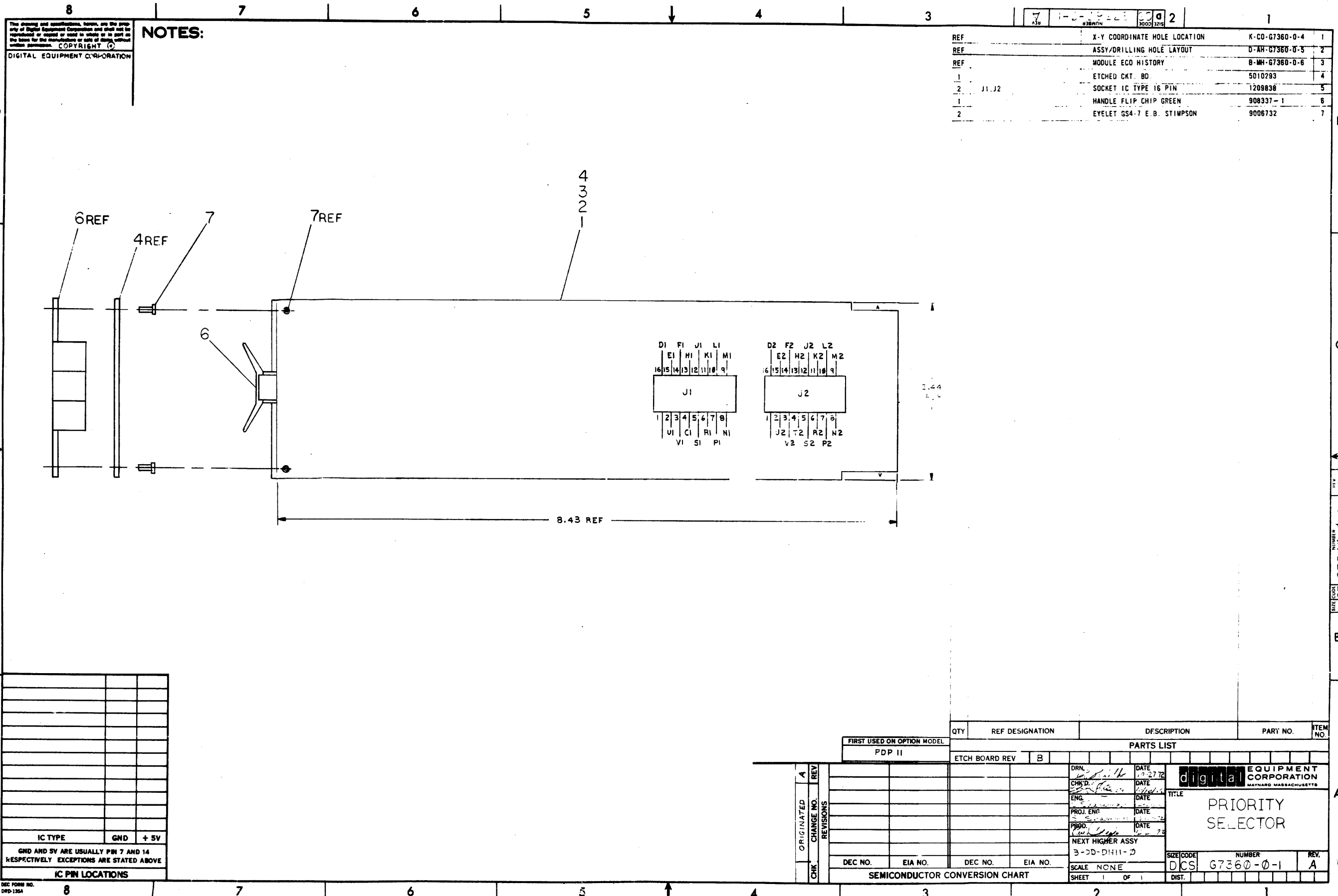
DRAWN	DATE
CHK'D.	DATE
ENG.	DATE
PROL. ENG.	DATE
PROD.	DATE
NEXT HIGHER ASSY.	
B-DD-DH11-Ø	
SCALE	

SIZE		CODE	NUMBER	REV.
B		CS	M7289- ϕ -1	E
DIST.				

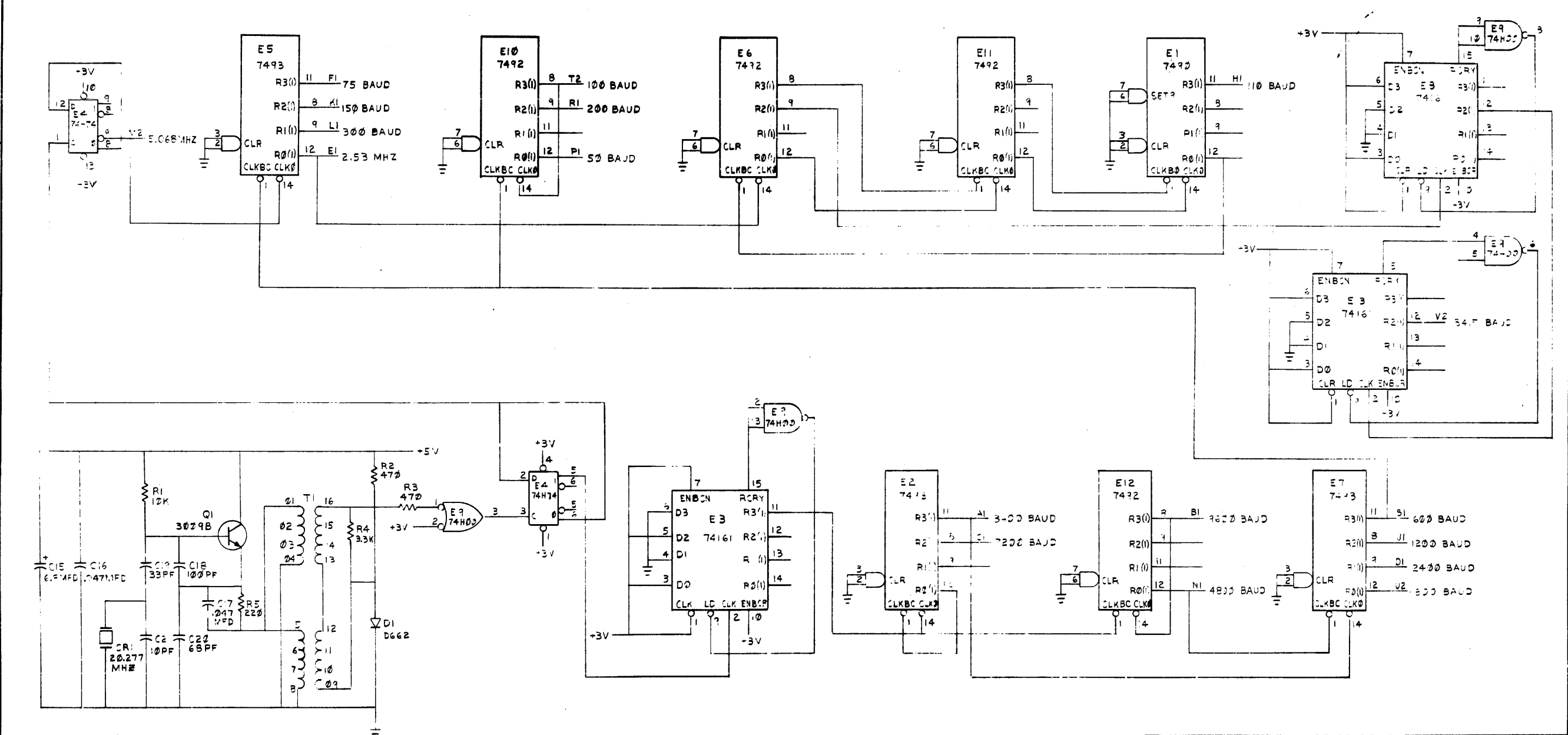


NOTE:
ALL "TTL DATA IN" SIGNALS FROM M371.
ALL "HALF DUPLEX" SIGNALS FROM M7288 SW5,7,9,11.
ALL "END OF CHAR" SIGNALS FROM M7280's.
ALL "SERIAL OUT" SIGNALS FROM M7280's.

FIRST USED ON OPTION/MODEL		QTY.	DESCRIPTION	PART NO.	ITEM NO.
PDP 11		PARTS LIST			
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES		DRN	DATE	digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS	
		ENG	DATE		
		PROJ. ENG.	DATE		
		PROD.	DATE		
			DATE		
DECIMALS		ANGLES		TITLE SYSTEM CONTROL & RECV SCAN	
.XXX = .005		± 0° 30'			
.XX = .02					
X = .1					
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓					
MATERIAL		NEXT HIGHER ASSY.		SIZE CODE DCS	
FINISH		B-DD- DH11 - 0			
		SCALE			
		SHEET 5 OF			
		DIST.			
				NUMBER M7289-0-1	
				REV. E	



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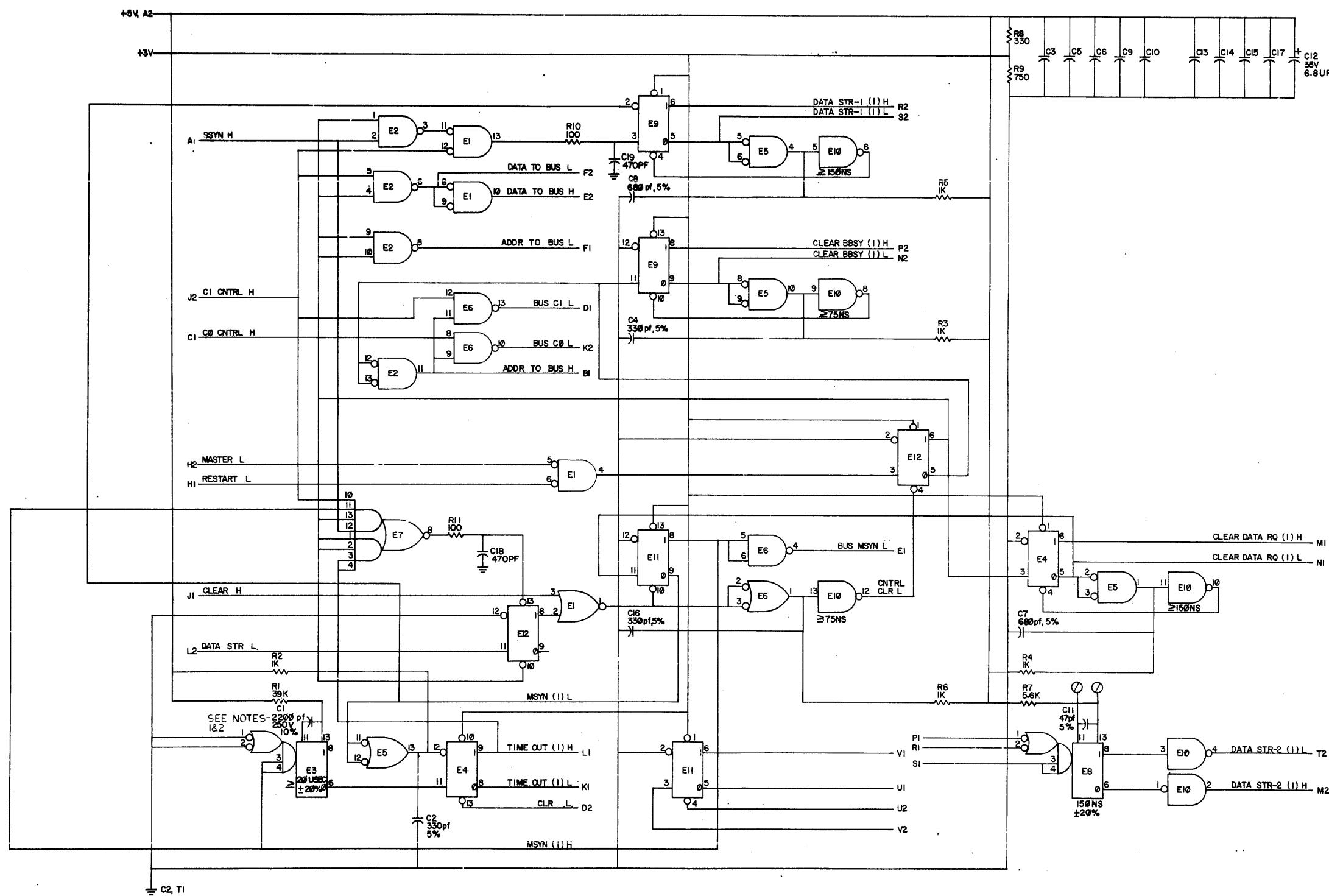


FIRST USED ON OPTION/MODEL		QTY.	DESCRIPTION	PART NO.	ITEM NO.
PDP 11					
UNLESS OTHERWISE SPECIFIED DIMENSIONS IN INCHES TOLERANCES		DATE	PARTS LIST		
DECIMALS	ANGLES	DATE	EQUIPMENT CORPORATION MILWAUKEE, WISCONSIN 53180		
.XXX - .000	± 0° 30'	DATE			
.XX - .00		DATE			
.X - .1		DATE			
REMOVE BURRS AND BREAK SHARP CORNERS. SURFACE QUALITY		DATE	TITLE		
MATERIAL		DATE	DH11-DC11 CLOCK		
FINISH		DATE	NEXT HIGHER ASSY.		
		DATE	E-DD-DH11-0		
		DATE	SCALE NONE		
		DATE	SHEET 2 OF 2		
		DATE	DIST.		
		DATE	REV.		
		DATE	DCS M4540-0-1		
		DATE	A		

DEC 10 PM NO
DRO 100-B

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1-0-5621W SD 1 0 100/1/1/1



NOTE: 1. C1 IS CHANGED TO 5000PF $\pm 20\%$ (1001765) FOR A DELAY OF 37US MINIMUM WHEN USED WITH A DL10.
2. FOR M796-YA CHANGE C1 TO 68uf 35V (P/N4000067)

UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W, 5%
CAPACITORS ARE .01uf, 150V, 20%
E1 IS DEC7482
E2 IS DEC7488
E3, E8 ARE DEC9801
E4, E9, E11, E12 ARE DEC7474
E5 IS DEC7481
E6 IS DEC9801
E7 IS DEC74H55
E10 IS DE7484
⊙ = SPLIT LUGS

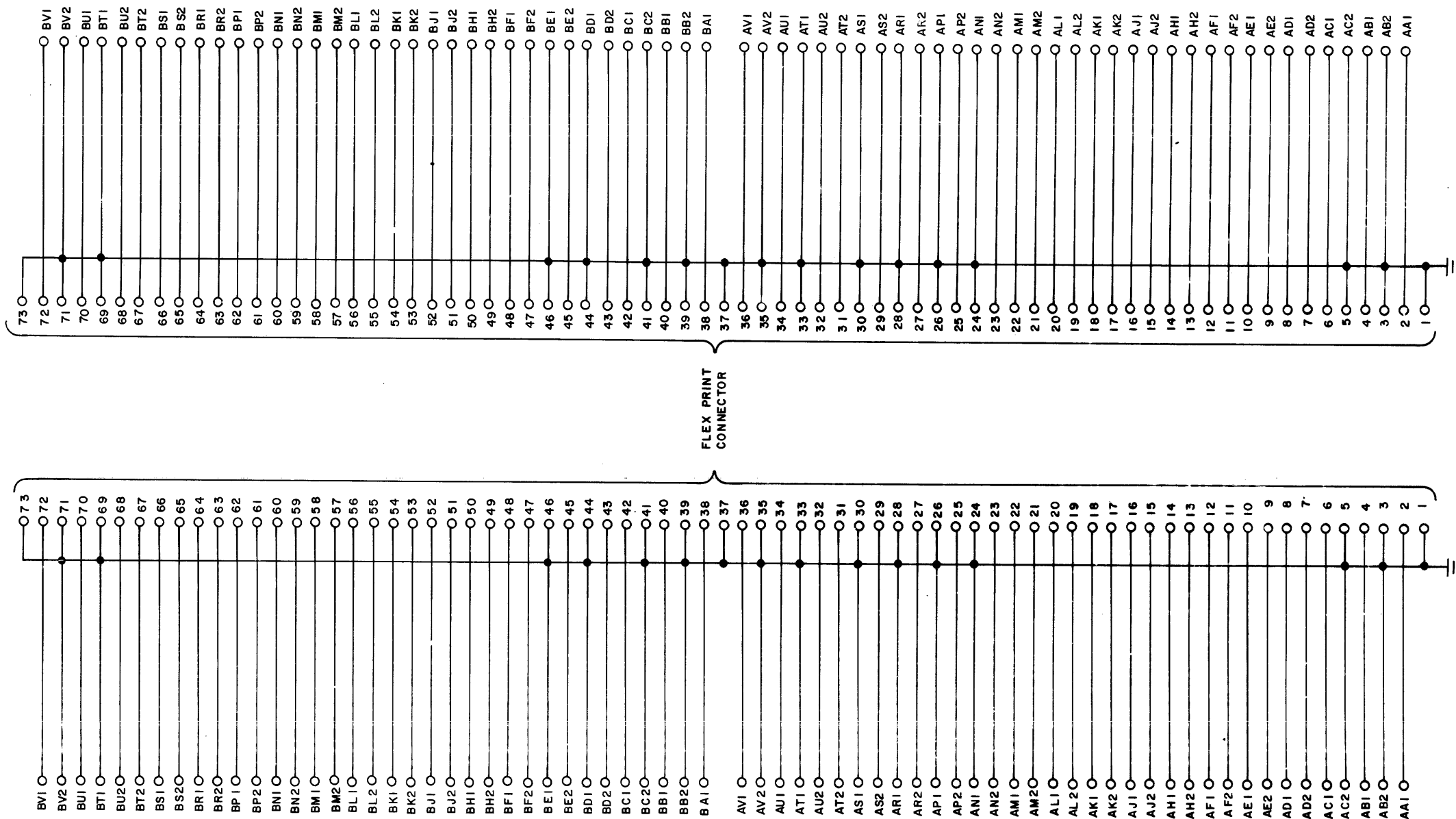
REVISIONS	DATE	BY	CHKD	APPD
1	10/24/70	W. K. G. /		
2	12/15/70	W. K. G. /		
3	12/15/70	W. K. G. /		
4	12/15/70	W. K. G. /		
5	12/15/70	W. K. G. /		
6	12/15/70	W. K. G. /		
7	12/15/70	W. K. G. /		
8	12/15/70	W. K. G. /		
9	12/15/70	W. K. G. /		
10	12/15/70	W. K. G. /		

DATE	BY	CHKD	APPD
10/24/70	W. K. G. /		
12/15/70	W. K. G. /		
12/15/70	W. K. G. /		
12/15/70	W. K. G. /		

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EA	DEC	EA

EQUIPMENT CORPORATION		TITLE	
M796 - 0-1		UNIBUS MASTER CONTROL M796	
REV. C		REV. C	
PRINTED CIRCUIT REV. C		PRINTED CIRCUIT REV. C	

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REVISIONS	
CHK	CHG NO. REV
1	00001 A
2	00002 B
3	00004 C

DEC FORM NO. DRG 102

DRN	DATE
CHK'D	DATE
ENG	DATE
PROF.	DATE

TRANSISTOR & DIODE CONVERSION CHART			
DEC		EIA	

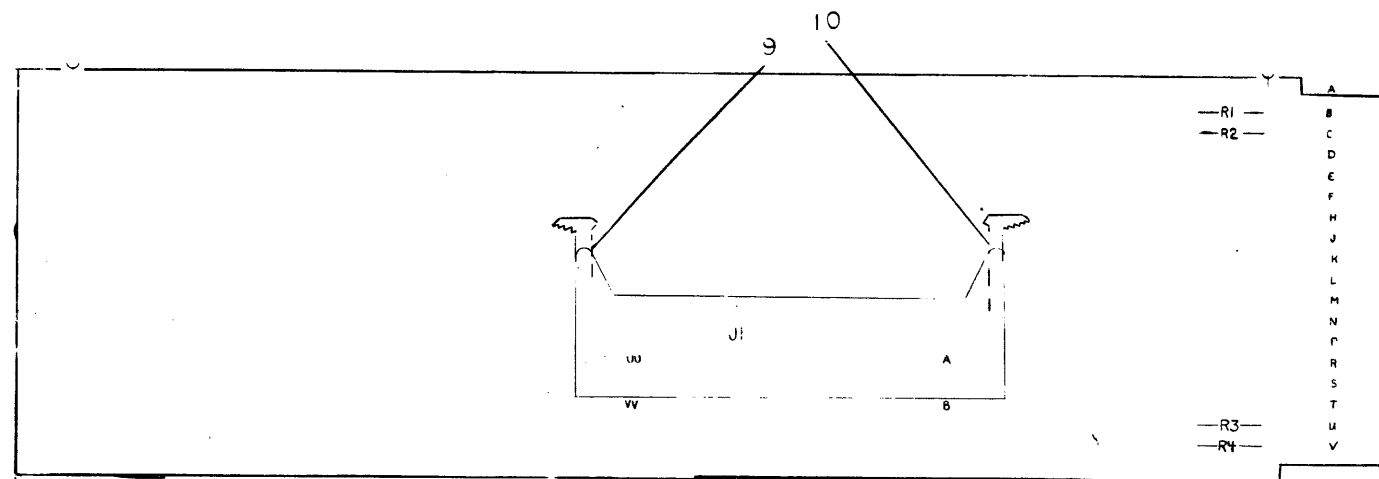
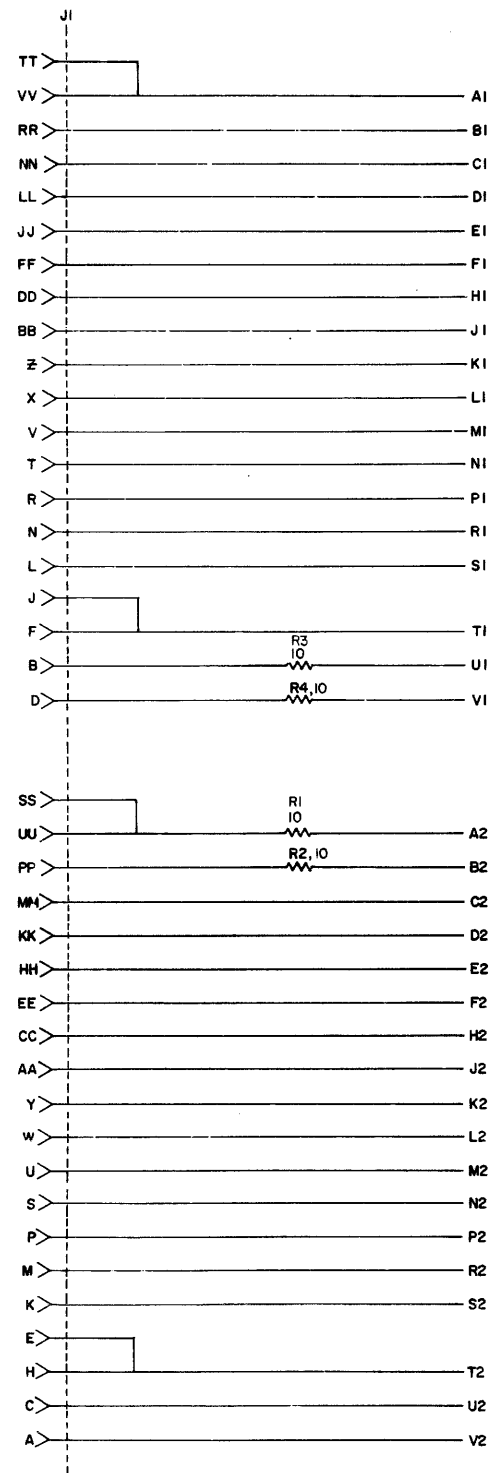
EQUIPMENT CORPORATION	
MAYNARD, MASSACHUSETTS	

TITLE			
INTERNAL BUS CONNECTOR M920			
SIZE	CODE	NUMBER	REV.
C	CS	M920-0-1	C
PRINTED CIRCUIT REV.			

3 324,434,435 PINK

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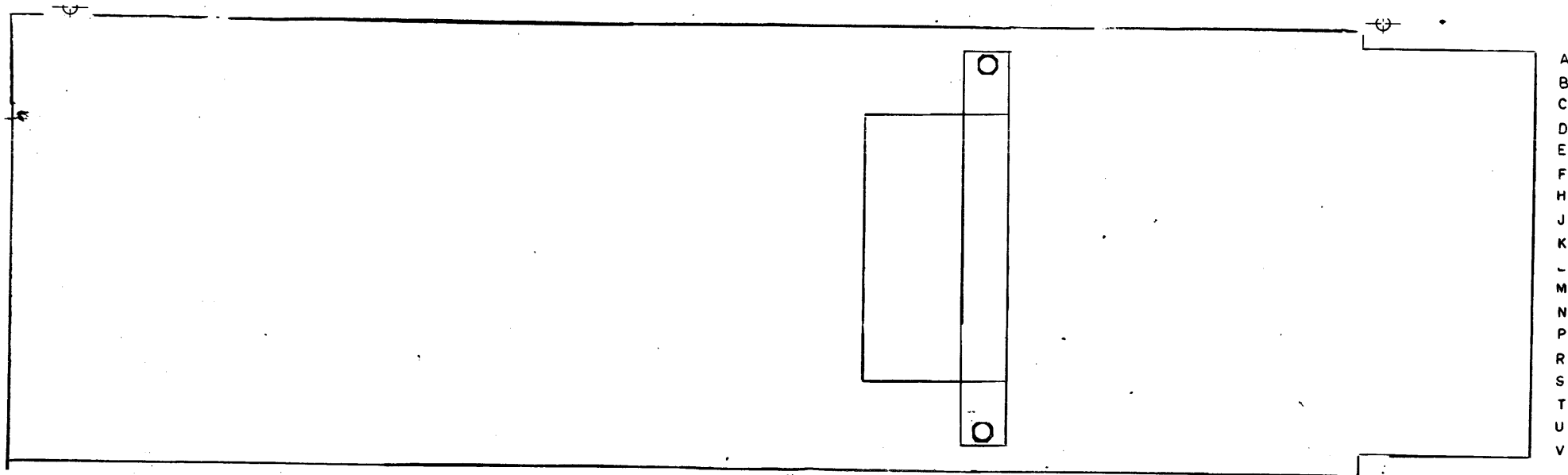
REV. 8
NUMBER 1209941-0-1
D CS 2002 105



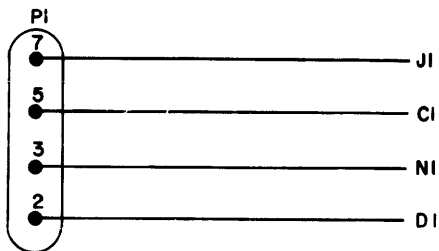
1	LEFT LATCH	1209941-03	10
1	RIGHT LATCH	1209941-04	9
1	HANDLE, FLIP CHIP - MAGENTA	9008337-06	8
2	EYELET	9006732	7
4	RES. 10 $\frac{1}{4}$ W 10%	1300170	6
1	BERG HEADER	1209941	5
1	ETCHED CIRCUIT BOARD	5009754	4
1	MODULE ECO HISTORY	B-MH-M971-0-6	3
	ASSY/DRILLING HOLE LAYOUT	D-AH-M971-0-5	2
	X-Y COORDINATE HOLE LOCATION	K-GO-M971-0-4	1
QTY.	REF. DESIGNATION	DESCRIPTION	DEC PART NO.

DESIGNED BY B. J. Nails	DATE 7/2/71	TRANSISTOR & DIODE CONVERSION CHART	TITLE CABLE INTERFACE BOARD #2
CHECKED BY M. H. Hobb	DATE 8-1-71	DEC	EIA
ENGR S. J. Lutz	DATE 8-2-71	DEC	EIA
PROD	DATE	DEC	EIA
EQUIPMENT CORPORATION		SIZE D CS	NUMBER M971-0-1
RAYMOND, MASSACHUSETTS		PRINTED CIRCUIT REV.	8

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A
B
C
D
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F
H
J
K
L
M
N
P
R
S
T
U
V



2	RIVETS	9007266	13
4	FEED THRU EYELET	9006693	12
2	WASHER	9006693	11
2	WASHER	9006655	10
2	WASHER 1/4" X 3/8"	9006011	9
1	handle FLIP CHIP - MAGENTA	9008337-06	8
2	eyelet	9006732	7
4	PINS	1209456-01	6
1	PIN HOUSING	1209340-0-0	5
1	ETCHED CIRCUIT BOARD	5009587	4
	MODULE ECO HISTORY	B-11-1973-0-6	3
	ASSY/DRILLING HOLE LAYOUT	B-AH-1973-0-5	2
	X-Y COORDINATE HOLE LOCATION	K-CC-1973-0-4	1
QTY.	REF DESIGNATION	DESCRIPTION	DEC PART NO.
		PARTS LIST	

REVISIONS	CHK	CHG	NO.	REV
1	2/24/0001	A		
2	1/6/0002	B		
3	1/12/0003	C		

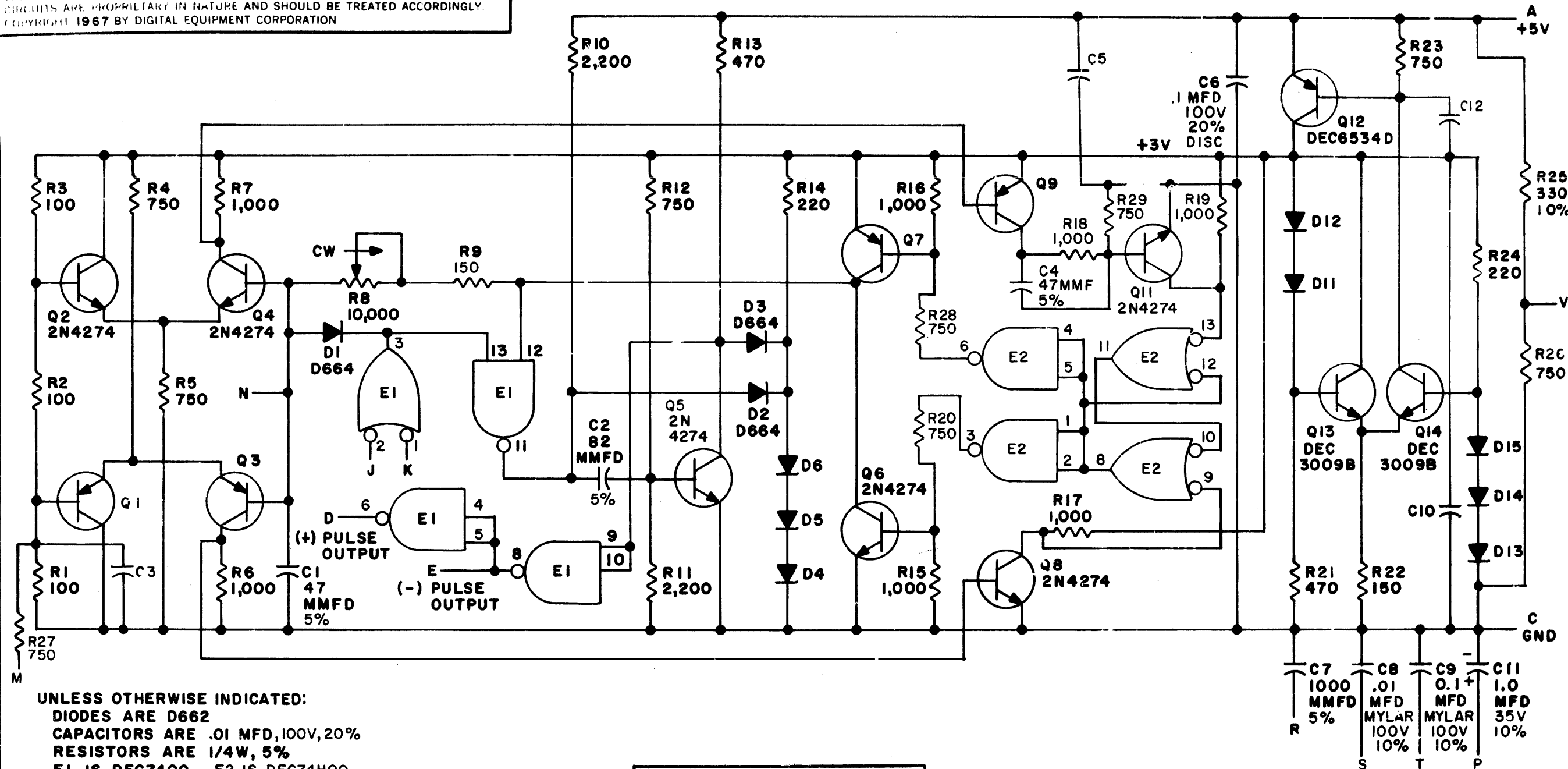
DRN	B. J. Haile	DATE	5/11/71
CHK'D	N. J. Haile	DATE	5/12/71
ENG	S. Shamma	DATE	5/21/71
PROD.		DATE	

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA

EQUIPMENT CORPORATION	
MAYNARD, MASSACHUSETTS	

TITLE		TTY CABLE CONNECTOR	
SIZE	CODE	NUMBER	REV
C	CS	M973-0-1	B
PRINTED CIRCUIT REV.		A	

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UNLESS OTHERWISE INDICATED:
 DIODES ARE D662
 CAPACITORS ARE .01 MFD, 100V, 20%
 RESISTORS ARE 1/4W, 5%
 E1 IS DEC7400, E2 IS DEC74H00
 PIN 7 ON IC = GND
 PIN 14 ON IC = +5V
 TRANSISTORS ARE DEC4258
 R8 IS A HELITRIM POT 10%-78PR

PARTS LIST A-PL-M401-0-0

REV	CHK	NO.	REV.	A	B	C	D	E	F	G	H	I	J	K	L	M
1	6769															
2	6844															
3	00001															
4	00002															
5	00003															
6	00004															
7	00005															
8	00006															
9	00007															
10	00008															

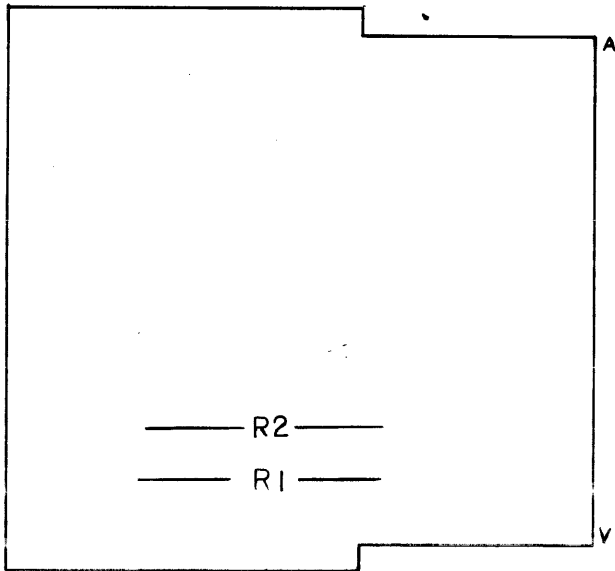
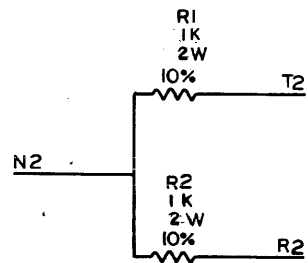
DRN.	DATE
7m. Waller	9-11-67
CHK'D	DATE
	11/13/67
ENG.	DATE
P. White	9/13/67
PROD.	DATE

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
DEC3009B	2N3009	D662	IN645
DEC4258	2N4258	D664	IN3606
2N4274	SAME		
DEC6534D	MPS6534		

digital
 EQUIPMENT CORPORATION
 MAYNARD, MASSACHUSETTS

TITLE				VARIABLE CLOCK M401			
SIZE	CODE	NUMBER	REV				
B	CS	M401-0-1	M				
PRINTED CIRCUIT REV.							

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2	R1,R2	RES. 1K, 2W, 10%	1300369	5
1		ETCHED CIRCUIT BOARD	5009588	4
		MODULE ECO HISTORY	D-AM-W404-0-6	3
		ASSY/DRILLING HOLE LAYOUT	D-AM-W404-0-5	2
		X-Y COORDINATE HOLE LOCATION	K-CO-W404-0-4	1
QTY.	REF DESIGNATION	DESCRIPTION	DEC PART NO.	ITEM NO.
		PARTS LIST		

REVISIONS
CHK CHG NO. REV.
50001 B
5/21/71
S. SHAMMAS

DEC FORM NO.

DRN	DATE
5/21/71	5/21/71
CHK'D	DATE
5/21/71	5/21/71
ENG	DATE
5/21/71	5/21/71
PROD	DATE
5/21/71	5/21/71

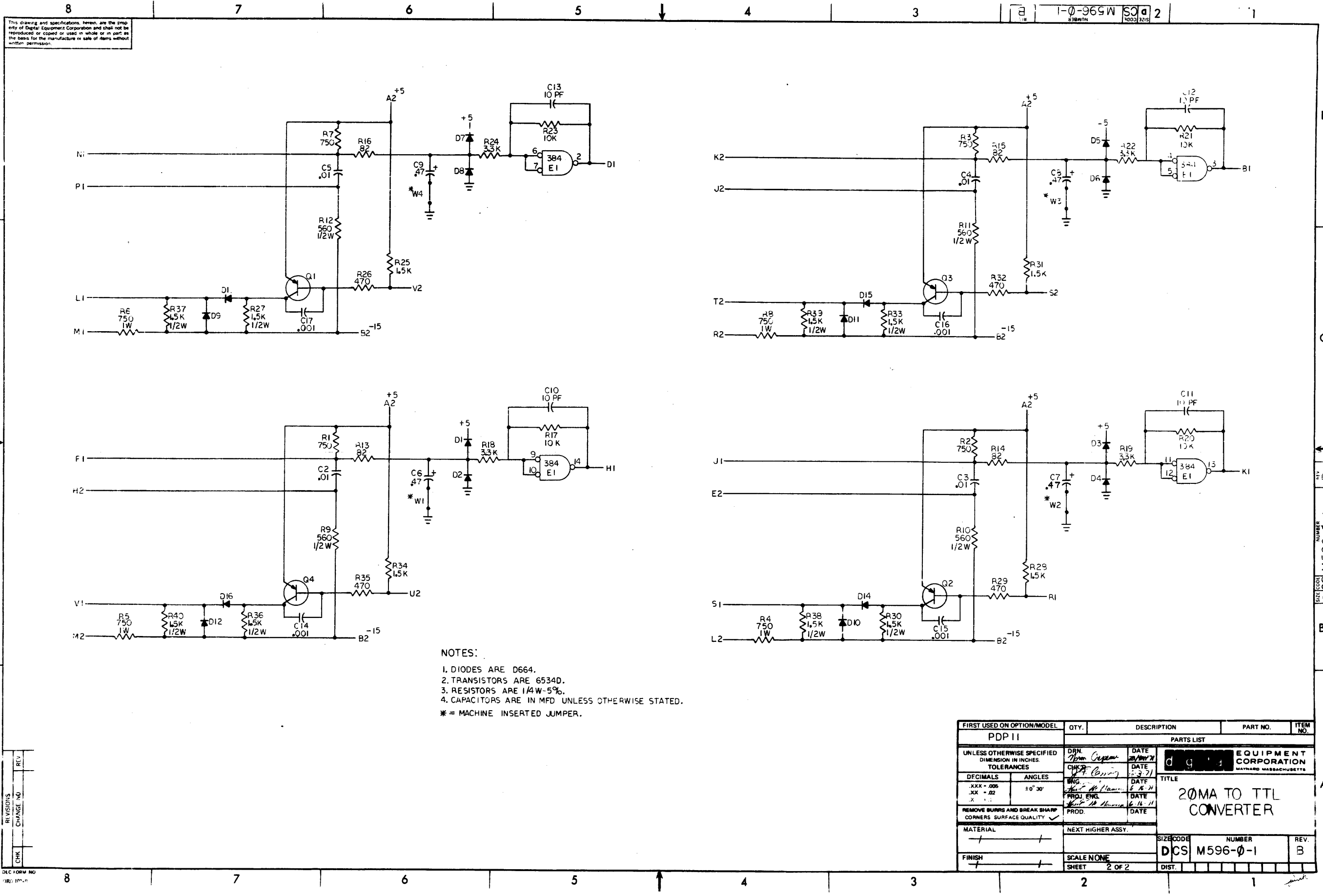
TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA

EQUIPMENT CORPORATION
MAYFIELD, MASSACHUSETTS

TITLE			
DTR JUMPER			
SIZE	CODE	NUMBER	REV
C	CS	W404-0-1	B
PRINTED CIRCUIT REV.			
C			

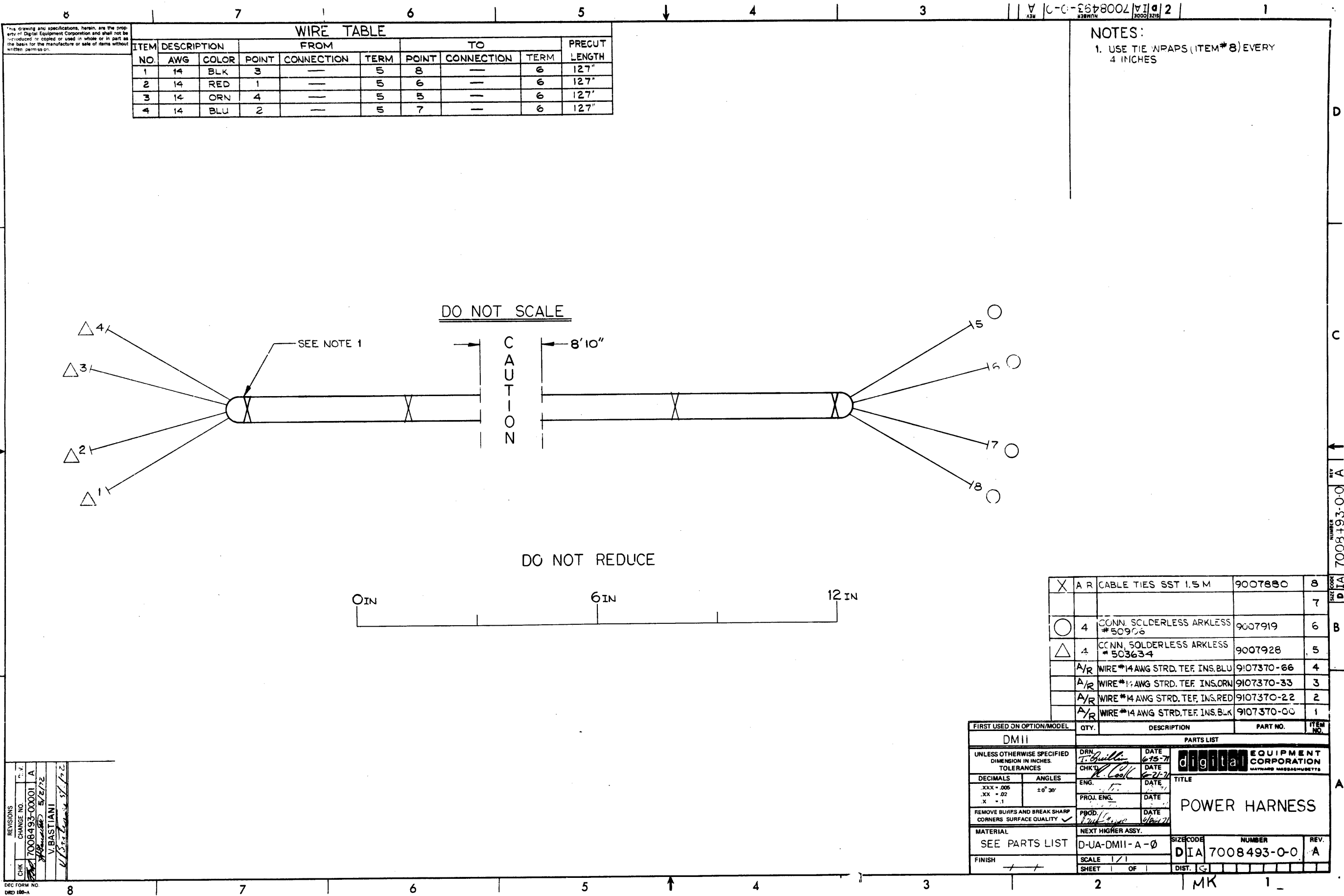
DISY. 3 24, 4 34, 4 35 2

SIZE CODE C CS
NUMBER W404-0-1
REV B



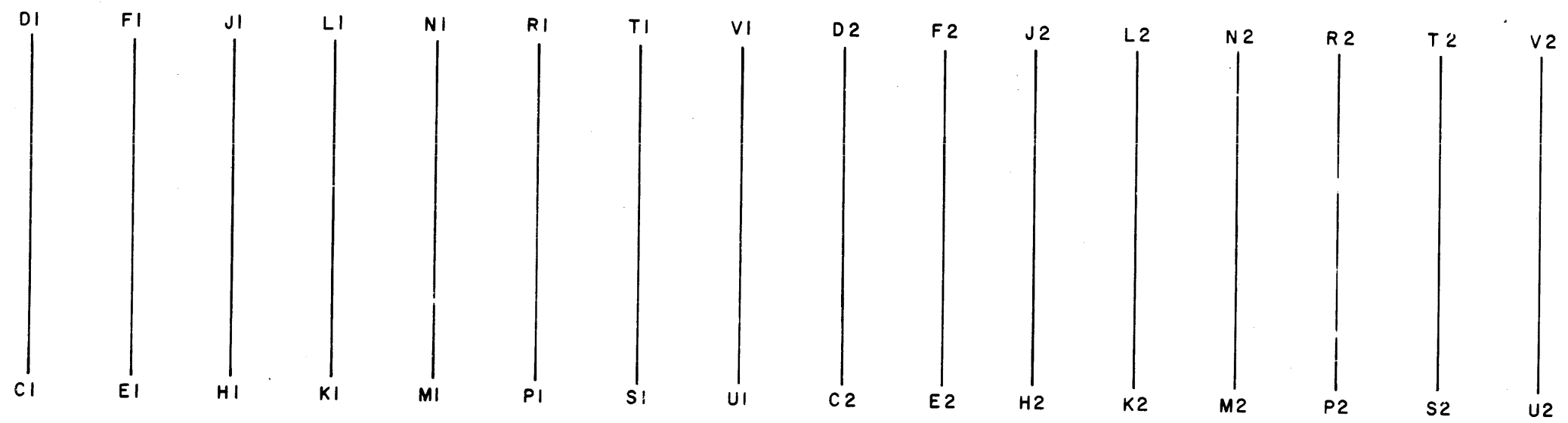
- NOTES:
- 1. DIODES ARE D664.
 - 2. TRANSISTORS ARE 6534D.
 - 3. RESISTORS ARE 1/4W-5%.
 - 4. CAPACITORS ARE IN MFD UNLESS OTHERWISE STATED.
- * = MACHINE INSERTED JUMPER.

FIRST USED ON OPTION/MODEL		QTY.	DESCRIPTION	PART NO.	ITEM NO.
PDP 11					
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES		DATE 2/10/71	EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS		
DECIMALS .XXX - .005 .XX - .02 .X - .1	ANGLES ±0° 30'	DATE 2-2-71	TITLE 20MA TO TTL CONVERTER		
REMOVE BURRS AND BREAK SHARP CORNERS. SURFACE QUALITY		DATE 6-16-71	REV. B		
MATERIAL		NEXT HIGHER ASSY.	SIZE CODE DCS		
FINISH		SCALE NONE	NUMBER M596-0-1		
SHEET 2 OF 2		DIST.			



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REV. NUMBER SIZE CODE

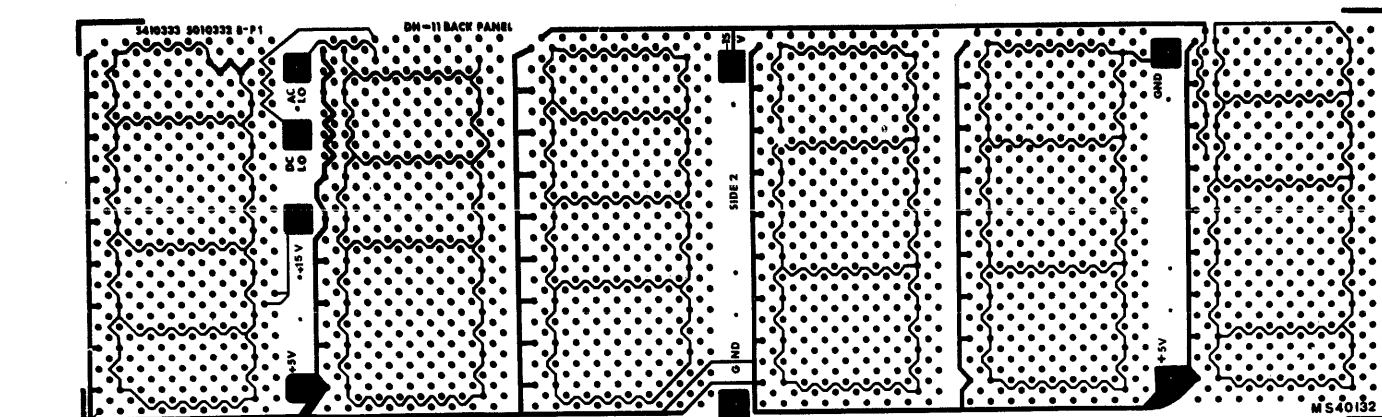


1	HANDLE, FLIP CHIP - MAGENTA	9008337-06	5
2	EYELET	9006732	4
1	ETCHED CIRCUIT BOARD	5009605	3
	MODULE ECC HISTORY	E-MH-M974-0-6	2
	ASSY/DRILLING HOLE LOCATION	D-AH-M974-0-5	1
QTY.	DESCRIPTION	DEC PART NO.	ITEM NO.
	PARTS LIST		

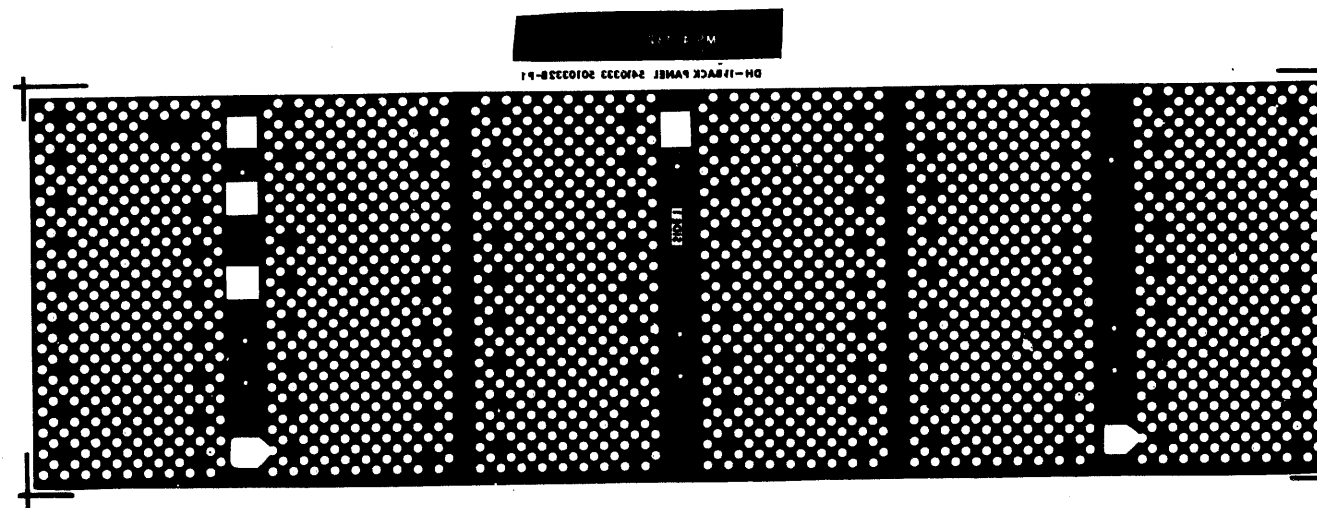
REVISIONS CHK'D NO REV	DRN. S. COPPER		DATE 5-13-71	TRANSISTOR & DIODE CONVERSION CHART				digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS	TITLE DM 11 MAINTENANCE JUMPER			
	CHK'D R. A. C. MOORE		DATE 5-14-71	DEC	EIA	DEC	EIA		SIZE B	CODE CS	NUMBER M974-0-1	REV
	ENG E. SHAMMAS		DATE 6-16-71									
	PROD.		DATE									



NOTES:



SOLDER SIDE (SIDE 2)



REF		X-Y COORDINATE HOLE LOCATION	K-CO-5410333-0-4	4
REF		ASSY/DRILLING HOLE LAYOUT	D-AH-5410333-0-5	3
REF		MODULE ECO HISTORY	B-MH-5410333-0-6	2
I		ETCHED CIRCUIT BOARD	5010332	1
QTY	REF DESIGNATION	DESCRIPTION	PART NO.	STE NO

	PARTS LIST									
ETCH BOARD REV	E									

DRN	DATE	digital EQUIPMENT CORPORATION
1-31-73		

DATE	2/22/73	TITLE	
ENG		DATE	

PROJECT NO.	DATE	CIRCUIT
2-22-78	2-22-78	CONCATENATION

PROD.	DATE	SCHEMATIC
2-23-73	2-23-73	
NEXT HIGHER ASSY		

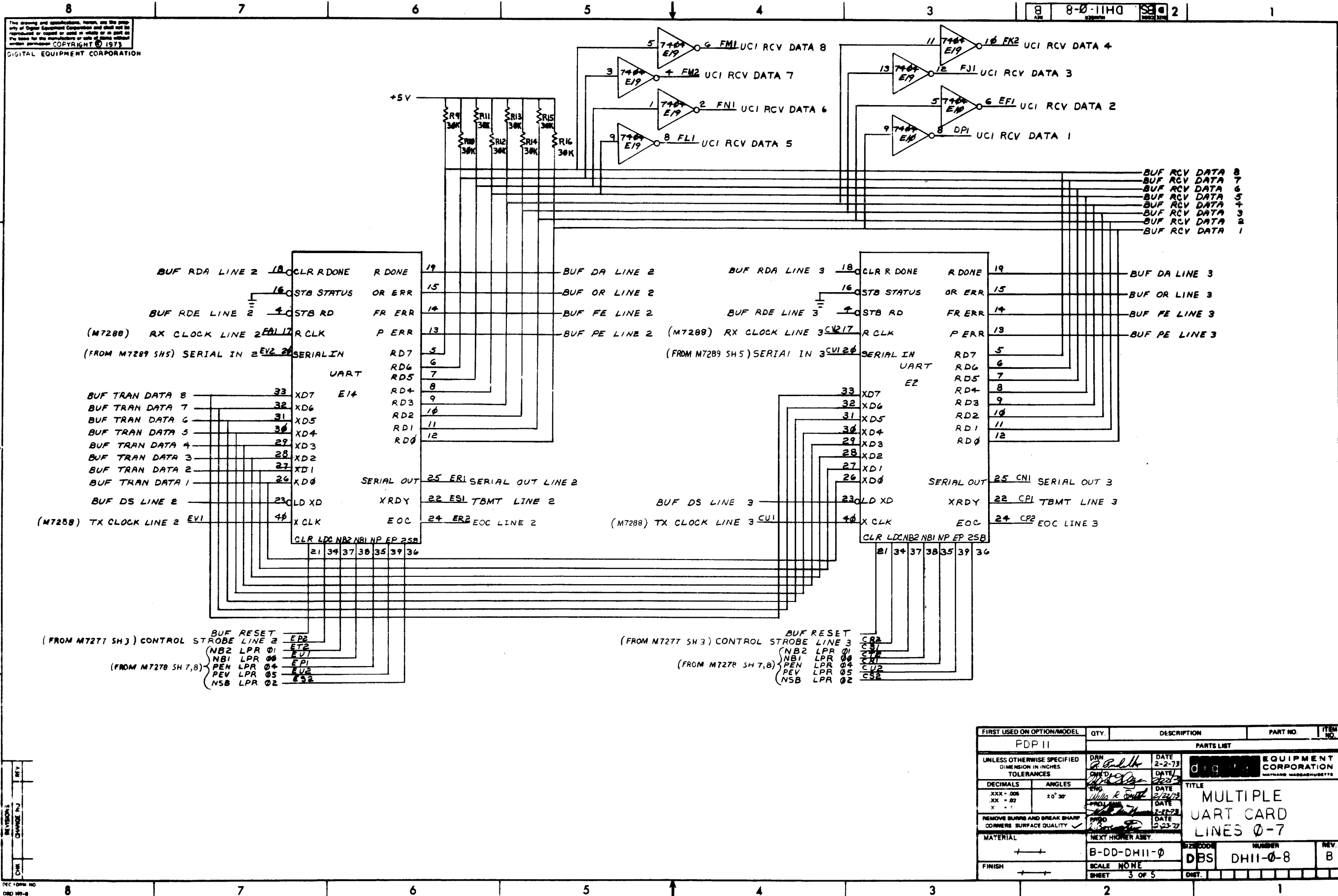
			D-AD-7009182-0-0	SIZE	CODE	NUMBER	REV.
	DEC NO	FIA NO		D	CS	5410333-0-1	A

DEC NO.		EXP NO.		SCALE		NONE		D		CS		3410333		04		11	
R CONVERSION CHART				SHEET		1		OF		1		DIST.					

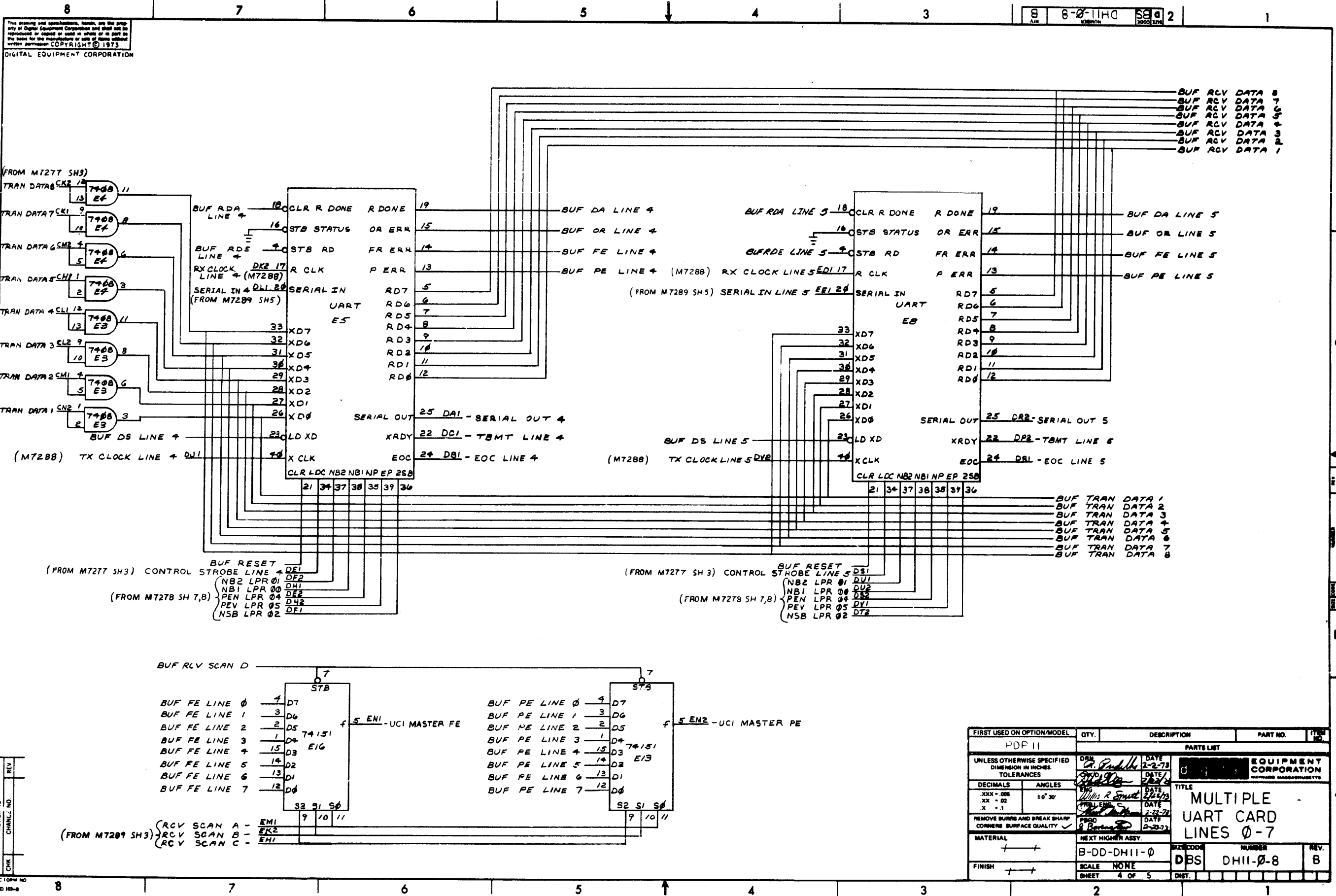
	2	1
--	---	---

GND AND 5V ARE USUALLY PIN 7 AND 14
RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS



FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
PDP 11				
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES	DRN DATE 2-2-73	DATE 2-2-73	EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS	
DECIMALS	ANGLES	DATE 2-2-73	TITLE MULTIPLE UART CARD LINES 0-7	
.XXX - .006 .XX - .02 X - .1	±0° 30'	DATE 2-2-73		
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY	DATE 2-2-73	DATE 2-2-73	SIZE CODE NUMBER DH11-0-8	
MATERIAL	DATE 2-2-73	DATE 2-2-73	REV. B	
FINISH	DATE 2-2-73	DATE 2-2-73	SHEET 3 OF 5	

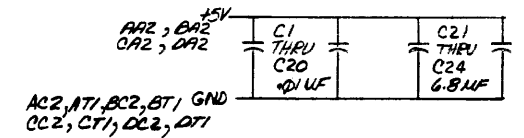


FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
PDP 11				
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES				
DECIMALS	ANGLES	DATE 2-2-79		
.XXX - .008	±0° 30'	DATE 2-2-79		
.XX - .02		DATE 2-2-79		
.X - .1		DATE 2-2-79		
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY				
MATERIAL				
NEXT HIGHER ASSY.				
FINISH				
SCALE NONE				
SHEET 4 OF 5				
DST.				
TITLE				
EQUIPMENT CORPORATION				
MULTIPLE UART CARD LINES 0-7				
REV.				
B				

NOTES:

NOTES:

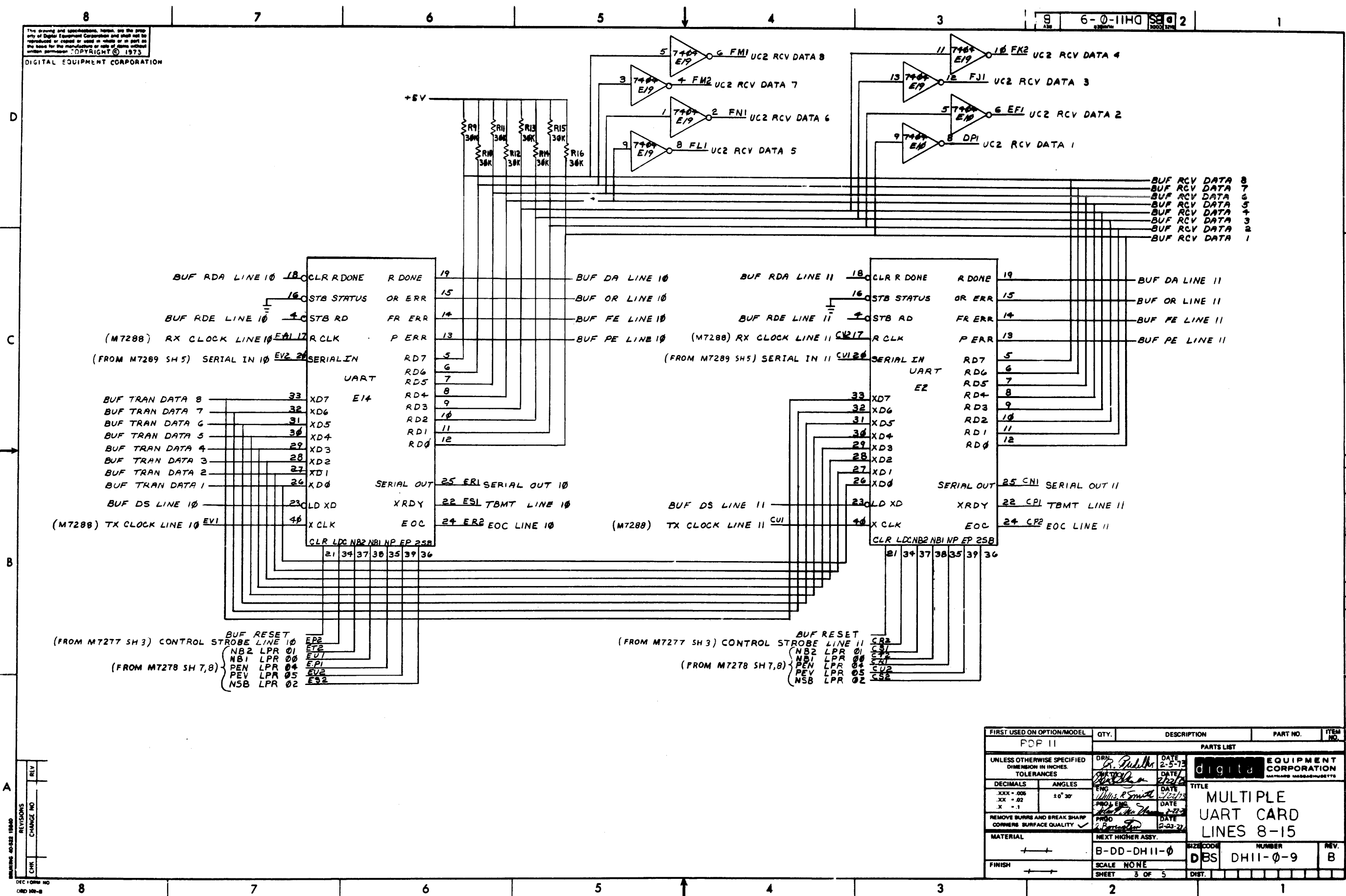
1. ALL 19-10459 UART PINS ARE -12VOLTS.
2. ALL SIGNALS THAT BEGIN WITH TAG 'BUF' ARE INTERNAL TO THE BOARD AND DO NOT GO TO EXTERNAL PINGERS.



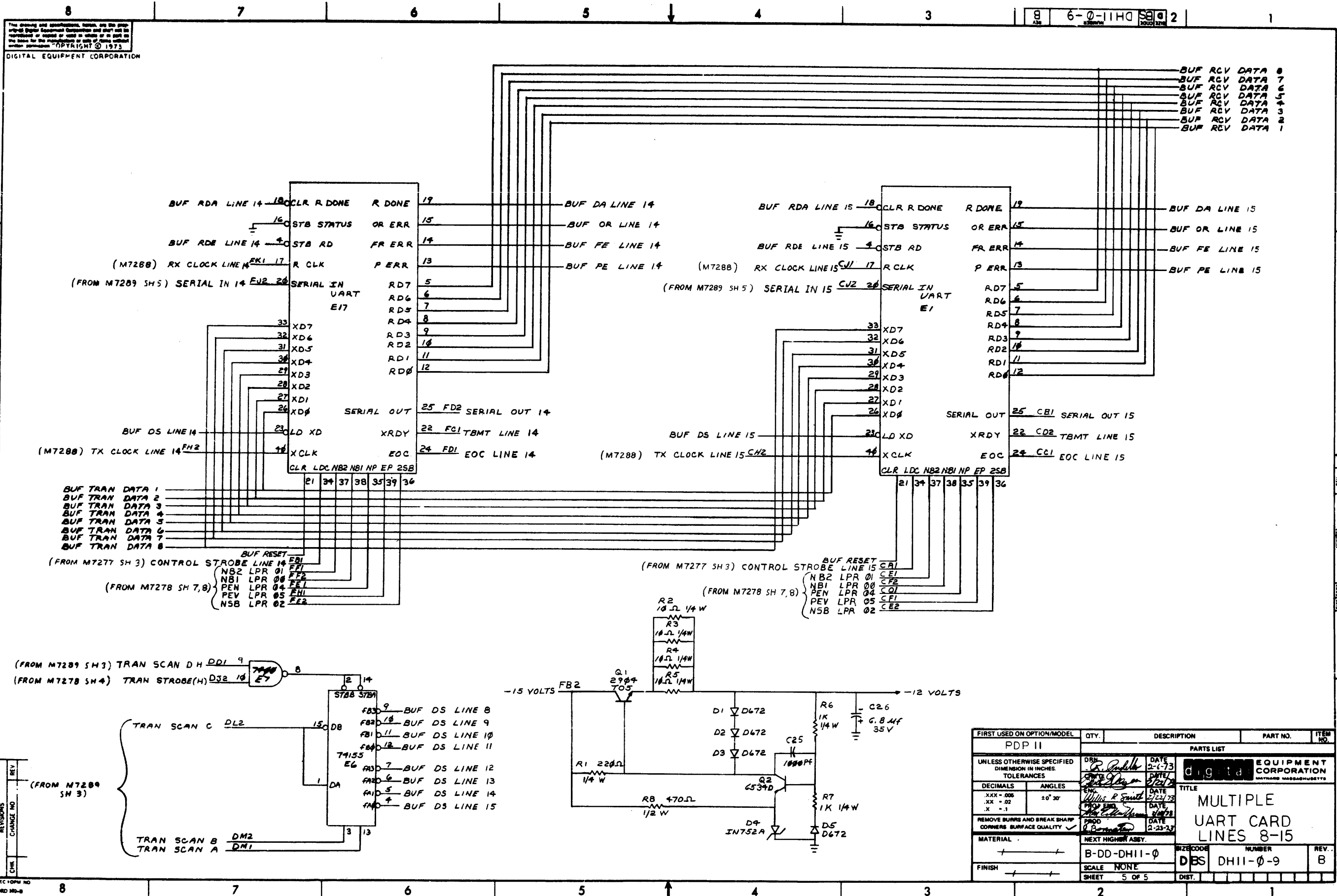
A					
	IC DEC 74153	8	/6		
	IC UART	3	1		
	IC DEC 74151	8	/6		
	IC TYPE	GND	+5V		
	GND AND +5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE				
	IC PIN LOCATIONS				

[illegible]

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DIGITAL EQUIPMENT CORPORATION



FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
PDP 11				
PARTS LIST				
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES	DRN R. P. P. 11/11/73	DATE 2-5-73	digit EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS	
DECIMALS .XXX ±.005	ENG W. R. Smith	DATE 2/22/73	TITLE MULTIPLE UART CARD LINES 8-15	
ANGLES .XX ±.02	PROL ENG W. R. Smith	DATE 2-22-73	SIZE CODE B-DD-DH11-0	
.X ±.1	PROD W. R. Smith	DATE 2-23-73	NUMBER DBS DH11-0-9	
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY	FINISH W. R. Smith	DATE 2-23-73	REV. B	
MATERIAL	NEXT HIGHER ASSY.	SCALE NONE	SHEET 3 OF 5	
FINISH			DIST.	



FIRST USED ON OPTION/MODEL		QTY.	DESCRIPTION	PART NO.	ITEM NO.
PDP 11					
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES		DATE	2-1-73	PARTS LIST	
DECIMALS	ANGLES	DATE	2-1-73	TITLE	
.XXX - .005	20° 30'	DATE	2-1-73	MULTIPLE	
.XX - .02		DATE	2-1-73	UART CARD	
.X - .1		DATE	2-1-73	LINES 8-15	
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY		DATE	2-23-73	REV. B	
MATERIAL		NEXT HIGHER ASSY.		B-DD-DH11-0	
FINISH		SCALE		NONE	
		SHEET		5 OF 5	

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DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS						
ENGINEERING SPECIFICATION				DATE February 5 1973		
TITLE DH11 Multiplexor						
REVISIONS						
REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	CHANGE PER ECO	DH11-00002	MCNAMARA	6/73	J.M. Hamman	6-6-73
B	CHANGE PER ECO	DH11-00007	MCNAMARA	10/74	J.M. Hamman	11-5-74
ENG 2-6-73 APPD 2-8-73 SIZE A CODE SP NUMBER DH11-0-5 REV B						
DEC FORM NO. DRA 107 SHEET 1 OF 25						

ENGINEERING SPECIFICATION				CONTINUATION SHEET	
TITLE DH11 Multiplexor					
General Description					
The DH11 Multiplexor connects the PDP-11 with 16 asynchronous serial communications lines operating with individually programmable parameters. These parameters are:					
Character length: 5,6,7, or 8 bit Number of Stop Bits: 1 or 2 for 6,7,8 bit characters 1 or 1.5 for 5 bit characters Parity generation and detection: Odd, Even, or None Operating Mode: Half Duplex or Full Duplex Transmitter Speed: 0,50,75,110,134.5,150,200,300,600, 1200, 1800,2400,4800,9600, Ext A, Ext B. Receiver Speed: 0,50,75,110,134.5,150,200,300,600, 1200, 1800,2400,4800,9600, Ext A, Ext B.					
Breaks may be detected or generated on each line.					
The DH11 multiplexor uses 16 double-buffered MOS/LSI receivers to assemble the incoming characters. An automatic scanner takes each received character and the line number and deposits that information in a first-in, first-out buffer memory referred to as the "silo". The bottom of the "silo" is a register which is addressable from the Unibus.					
The transmitter in the DH11 also uses double-buffered MOS/LSI units. They are loaded directly from message tables in the PDP-11 memory by means of single cycle direct memory transfers (NPR). The current addresses and byte counts for each line's message table are stored in semiconductor memories located in the DH11. This reduces the Unibus time taken for the NPR transfers to one NPR cycle per character transmitted. The NPR cycle used is lengthened slightly.					
As many as 16 DH11's may be placed on a single PDP-11 processor, creating a total capacity of 256 lines.					
SIZE A CODE SP NUMBER DH11-0-5 REV B					
DEC FORM NO DEC 16-(381)-1022-N370 DRA 108 SHEET 2 OF 25					

ENGINEERING SPECIFICATION				CONTINUATION SHEET	
TITLE DH11 Multiplexor					
II. Multiplexor Control Section					
2.1 The DH11 multiplexor control is located in a prewired double system unit. It contains NPR interface logic, interrupt logic, a clock card, transmitter and receiver scanners, etc.					
2.2 The DH11 will operate under the following conditions:					
Temperature: plus 50 to plus 110 degrees F. Humidity: zero to 95% non condensing					
2.3 The power consumption of the DH11-AA,AB and AC logic (excluding the level conversion modules, which run off the level conversion/distribution panel power supply) is:					
Plus 5: 8.4 amperes (DH11 alone)* 11.2 amperes (DH11 plus DM11-BB Modem Control)* Plus 15: None Minus 15: 240 milliamperes					
2.4 The power consumption of the DH11-AD and AE logic.					
DH11-AD					
Plus 5: 10.8 amperes* Plus 15: 400 milliamperes Minus 15: 645 milliamperes					
DH11-AE					
Plus 5: 8.6 amperes* Plus 15: 100 milliamperes Minus 15: 340 milliamperes					
2.5 The DH11 receiver units provide serial to parallel conversion of 5,6,7, or 8 bit code with one start bit and at least one stop bit. An extra data bit is added when parity operation is selected. The allowable input distortion is 43.75%, assuming no speed distortion. The maximum allowable speed distortion is 4.8% for 8 bit characters.					
2.6 The DH11 transmitters provide parallel to serial conversion of 5,6,7 or 8 bit code with one start bit and one, one and a half (5 bit only), or two (6,7, or 8 bit only) stop units. An extra data bit is added if parity operation is selected. The number of bits per character, the number of stop marks, and parity mode are selectable on a per-line basis, but must be the same as the					
* Add .2 amperes if this is the last option on the Unibus. (The Unibus terminator consumes .2 amperes.)					
SIZE A CODE SP NUMBER DH11-0-5 REV B					
DEC FORM NO DEC 16-(381)-1022-N370 DRA 108 SHEET 4 OF 25					

ENGINEERING SPECIFICATION				CONTINUATION SHEET	
TITLE DH11 Multiplexor					
1.0 Variations					
1.1 The DH11 Multiplexor is available in five variations:					
The DH11-AA consists of a double system unit, all modules necessary to implement a 16 line asynchronous multiplexor, a 5-1/4 inch level conversion and distribution panel with its own power supply,* and a data cable between the logic in the double system unit and the level conversion/distribution panel. The modules for level conversion are not included, so that the type and quantity of lines may be customized to the customer's requirements.					
The DH11-AB is the same as the DH11-AA, but does not include the level conversion/distribution panel or its associated power supply. Instead of a data cable to a distribution panel, a data cable to the DC08CS telegraph converter panel is supplied.					
The DH11-AC is the same as the DH11-AA, except that the power supply on the level conversion/distribution panel is arranged for 240 volt, 50 Hertz operation. (there is no need for a 50 Hertz version of the DH11-AB because it is a processor-powered option).					
The DH11-AA, -AB, and -AC include pre-wired slots in the double system unit for the insertion of the DM11-BB modem control.					
The DH11-AD consists of a double system unit, all modules necessary to implement a 16 line asynchronous multiplexor, EIA level conversion for the data lines, modem control with EIA level conversion, and a 16 line EIA distribution panel.					
The DH11-AE is the same as the DH11-AD except that the modem control modules are not included.					
CAUTION: THE DH11 USES HEX MODULES AND THUS CANNOT BE MOUNTED IN A BALL EXPANDER BOX. THE 11/35, 11/45 TYPE BOXES MUST BE USED.					
*The power supply for the distribution panel is also 5-1/4" high. Generally, it can be mounted on the rear of the rack in a position opposite the distribution panel which is usually mounted on the front of the rack.					
SIZE A CODE SP NUMBER DH11-0-5 REV B					
DEC FORM NO DEC 16-(381)-1022-N370 DRA 108 SHEET 3 OF 25					

ENGINEERING SPECIFICATION		CONTINUATION SHEET	
TITLE DH11 Multiplexor			
2.6 Continued corresponding receiver. The serial data rate is determined by a crystal clock and is program controllable on a per-line basis. The transmitter speeds may be program controlled independently of the receiver speeds. Output distortion is less than 2%. 2.7 Interface to and from the control section: Outputs: There are 16 data lines at TTL levels using negative logic (mark=0). Inputs: There are 16 data lines at TTL levels using negative logic (mark=0). The input leads from the level conversion/distribution panel are equipped with pull up resistors which place lines not equipped with level conversion in a permanently SPACING condition. Logic in the DH11 receivers prevents this condition from assembling null characters on a continuous basis, however. For the DH11-AD and AE options, EIA level conversion is provided for the 16 input and output TTL data lines. 2.8 Bus Load: The DH11 presents two bus loads to the Unibus. If a DM11-BB modem control is added, that will be an additional bus load. The DH11-AD is three bus loads. 2.9 Interrupts 2.9.1. There are two kinds of receiver interrupts; both are enabled by bit 6 of the System Control Register. 2.9.1.1 Receiver Interrupt (System Control Register, bit 7) This interrupt, when enabled, occurs whenever the number of entries in the silo exceeds the "silo status alarm level" that the program has stored in the low byte of the Silo Status Register. (The program can examine that actual silo fill at any time by examining the high byte of the Silo Status Register.)			
SIZE	CODE	NUMBER	REV
A	SP	DH11-0-5	B
DEC FORM NO DEC 16-(381)-1022-N370 DRA 108			
SHEET 5 OF 25			

ENGINEERING SPECIFICATION		CONTINUATION SHEET	
TITLE DH11 Multiplexor			
2.9.1.2 Storage Overflow Interrupt (System Control, bit 14) This interrupt, when enabled, occurs whenever the character storage silo is full and the DH11 hardware has a need to store an additional character there. Should this situation occur, this does not necessarily mean that data has been lost. The reader is referred to Section 5.9. "Programming-Discussion" 2.9.2 There are two kinds of transmitter interrupt; both are enable by bit 13 of the System Control Register. 2.9.2.1 Transmitter Interrupt (System Control, bit 15) This interrupt, if enabled, occurs whenever one or more lines have finished the transmission of a complete string of characters. Specifically, it occurs after the NPR cycle that loaded the last character to be transmitted (and hence incremented the byte count to zero). 2.9.2.2 Non-Existant Memory Interrupt (System Control, Bit 16) This interrupt, when enabled, occurs whenever the DH11 addresses non-existant memory. Specifically, this interrupt occurs if the DH11 enters an NPR cycle, places an address on the Unibus and fails to receive a slave sync response for the location addressed within 20 microseconds. 3.0 Description of the Hardware 3.1 Receiver Hardware Reception on each line is by means of Universal Asynchronous Receiver/Transmitters (UARTS). These are 40 pin MOS/LSI chips which perform all the necessary functions for double buffered asynchronous character assembly. The receiver section of the UART samples the line at 16 times the bit rate of the signals to be received on that line. Upon detection of a MARK to SPACE transition, the UART counts 8 clock pulses and checks the state of the line again. This sampling will occur in the center of a normal start bit.			
SIZE	CODE	NUMBER	REV
A	SP	DH11-0-5	B
DEC FORM NO DEC 16-(381)-1022-N370 DRA 108			
SHEET 6 OF 25			

ENGINEERING SPECIFICATION		CONTINUATION SHEET	
TITLE DH11 Multiplexor			
3.2 The Silo The silo is an MOS/LSI digital storage buffer that is 16 bits wide and 64 words deep. A 16 bit word is entered at the "top", from which it automatically bubbles down to the "lowest" location that does not already contain an entry. The "bottom" of the silo is the Next Received Character Register. There are three "registers" associated with the silo. One of these is the Next Received Character Register. The Next Received Character Register is a read-once register because it is, in fact, the bottom of the silo and reading it extracts that character from the silo and causes all other entries to bubble down one more position. The other two registers are byte-size registers and are contained within the Silo Status Register. One of them, the high byte, is read-only and contains the status of an up-down counter giving the actual fill level of the silo. The second register, in the low byte, is read/write and is used by the program to specify that silo fill level beyond which the program wishes to receive interrupt notification. The details of these registers are explored some more in Section 5.9 (Programming - Discussion) under the heading "Silo". 3.3 Received Character Distortion Received characters may contain up to 43.75% distortion on any bit, due to the 16 times clock rate sampling. However, the overall bit rate must be accurate. Specifically, errors in bit rate are cumulative such that when the receiver samples the stop bit to see if it is there (if not, it's a "framing error") the error accumulated by that time must not exceed 43.75% of a bit time. The accumulated error (called "gross start-stop distortion") is calculated as (clock error x (number of data bits plus one) plus bias distortion of the final character). Assuming the reception of eight data bits, or seven data bits plus parity, 4.8% speed distortion would be permissible. Speed distortion (clock error, bit rate error) of any amount poses severe problems in an echo situation, however. Specifically, if a terminal sends to the DH11 at a slightly fast rate and the DH11 sends the exact same characters back to the terminal at the correct rate, the DH11 silo will eventually fill with un-echoed characters. This problem would not occur with keyboard terminals, but high speed tape senders should have their transmission speeds carefully checked before use with the DH11 or any other asynchronous communications interface made by any			
SIZE	CODE	NUMBER	REV
A	SP	DH11-0-5	B
DEC FORM NO DEC 16-(381)-1022-N370 DRA 108			
SHEET 8 OF 25			

ENGINEERING SPECIFICATION		CONTINUATION SHEET	
TITLE DH11 Multiplexor			
3.1 Receiver Hardware (Continued) If that sample is a MARK, the receiver returns to its idling state, ready to detect another MARK to SPACE transition. If the sample was a SPACE, the receiver enters the data entry condition and samples the state of the line at subsequent sample points spaced 16 clock ticks from the center of the start bit. The number of samples taken is determined by the "character length" information entered into the UART via the Line Parameter Register. If parity checking has been enabled for this line, the receiver computes the parity of the character just received and compares it with the parity sense specified for reception on that line. If the parity sense differs, the parity error bit will be set. The character length, parity sense, number of stop bits, etc. that will be used by the UART to perform the above operations are stored within each UART in a control bits holding register. The control bits holding registers of each UART are addressable, on a write only basis, from the Unibus, by first setting the "Line selection bits" of the System Control Register and then loading the desired line parameters into the Line Parameter Register, from which they will automatically be transferred to the control bits holding register of the designated UART. It is important that no interrupt handling routine intervene and change the contents of the System Control Register during the above operation.			
SIZE	CODE	NUMBER	REV
A	SP	DH11-0-5	B
DEC FORM NO DEC 16-(381)-1022-N370 DRA 108			
SHEET 7 OF 25			

ENGINEERING SPECIFICATION		CONTINUATION SHEET	
TITLE DH11 Multiplexor			
3.3 Continued- company. In computing speeds, one may assume the DH11 receiver clock to be accurate within at least .05%. 3.4 Transmitter Hardware Transmission on each line is by means of Universal Asynchronous Receiver/Transmitters (UARTs). These are 40 pin MOS/LSI chips which perform all the necessary functions for double buffered asynchronous character transmission. The transmitter section of the UART holds the serial output line at a MARKING state when idle. When the transmitter loading leads have been conditioned with the character to be transmitted and the data strobe lead has been brought high (these functions are performed by the NPR control), the UART will commence generation of a start space within one sixteenth of a bit time. The start space and all subsequent data bits are a full bit time each. The start space is followed by M data bits, where M is 5,6,7, or 8 as determined by the control bits holding register. (See the description of the receiver hardware for a description of the UART control bits holding registers and how they are loaded from the Line Parameter Register). The data bits are presented to the line least significant bit first. The parity bit, if parity generation is enabled, is calculated by the transmitter and affixed after the last data bit, but before the stop marks. The stop bit or bits depend in quantity upon the setting of the control word. If the transmission of 6,7, or 8 bits has been selected, the program may select either one or two stop bits. If the transmission of 5 bit code has been selected, the program may select either one or one and a half stop bits. If the transmitter's holding register has been loaded while a character was being transmitted, that second character will have its start bit commence immediately at the end of the preceding character's stop bit(s). 3.5 The Auto-Echo Feature The DH11 contains provision for the hardware to echo received characters without software intervention. The feature may be enabled on any line by conditioning the line selection bits in the System Control Register and then setting the appropriate bits in the Line Parameter Register, including bit 15, Auto Echo Enable.			
SIZE	CODE	NUMBER	REV
A	SP	DH11-0-5	B
DEC FORM NO DEC 16-(381)-1022-N370 DRA 108			
SHEET 9 OF 25			

ENGINEERING SPECIFICATION		CONTINUATION SHEET	
TITLE DH11 Multiplexor			
3.5 Continued- The auto-echo hardware is part of the receiver scanner and operates as follows: 1) If the receiver scanner finds a received character for a line upon which auto-echo is NOT enabled, it simply dumps that character into the silo and resumes scanning. 2) If the receiver scanner finds a received character for a line upon which auto-echo IS enabled, it examines the error flags associated with that character- a) If a framing error is detected, this means that the remote terminal is trying to gain the attention of the processor by sending a "break". In this case, the auto-echo hardware dumps the received character and associated flag into the silo so that the system software will be alerted. The break is nofechoed to the remote terminal. b) If an overrun error is detected, this means that the remote terminal is trying to gain the attention of the processor by typing characters. This case is treated identically to 2a, above. 3) If the receiver scanner finds a received character for a line (actually I should say "from a line") upon which auto-echo is enabled and there are no error flags of the type mentioned above, the receiver scanner and auto-echo logic will attempt to echo the character. First, however, certain tests of internal logic conditions must be made. a) The UART transmitters are all loaded from a common internal data bus. Therefore, the auto-echo hardware must first check to see that no NPR cycles are in progress loading a UART transmitter from that bus. If a conflict is indicated, the receiver scanner is restarted and the process will be tried again on the scanner's next rotation. b) If the above test indicates no problem, the one remaining check is to see if the transmitter holding register for the line upon which the character was received is available. If it is not, the scanner is restarted. If it is available, auto-echo commences. One should note that it is not advisable to try to transmit messages on a line and auto-echo characters received on that line simultaneously. This is not unreasonable, as you plainly			
SIZE	CODE	NUMBER	REV
A	SP	DH11-0-5	B
DEC FORM NO DEC 16-(381)-1022-N370 DRA 108			
SHEET 10 OF 25			

ENGINEERING SPECIFICATION		CONTINUATION SHEET	
TITLE DH11 Multiplexor			
4.0 Multiplexor Distribution Panel and Power Supply 4.1 The DH11 provides a panel for level converters and cables for the individual lines. The panel uses a standard H911 style rack, but only 6 connector blocks are used. A Layout of the distribution panel and the various slot assignments is shown in the option bulletin and in the manual. Note that the slot assignments follow the DF11 (Standard level conversion and cable slot for PDP-11 Communications Products) format. Slots A06 through A21 are used for level conversion modules. Slots B06 through B21 are used for cable termination. Other slots provide inputs or special purpose outputs. The distribution panel mounts on a standard 19 inch cabinet and connects to the DH11 logic by means of a BC08-S data cable. 4.2 Power for the distribution panel is provided by the H758* power supply mounted on the rear of the cabinet. The H758 provides the voltages listed below: +15 volts @ 2 amperes -15 volts @ 2 amperes + 5 volts @ 4 amperes Power drain of the distribution panel depends upon the type of level conversion used. The maximum draw on the +15 and -15 occurs when DF11-BB modems are used, at which time the full rated output of 2 amperes is used. The maximum +5 draw occurs when all lines are arranged for full modem control (4 DM11-DC options) - the current used is then 1.7 amperes. Note that the level conversion types can be mixed on a 4 line basis, by using different converters on slots A4, A5, B4, and B5. Also level converters can be mixed on a single line basis by using slot A6 through A21 for level conversion on a single line basis. Consult the module utilization diagram for the distribution panel for specific details. 4.3 The DH11-AD and AE options use a 16 line EIA distribution panel. This panel requires no power of its own. It mounts on a standard 19 inch cabinet and connects to the DH11 logic by means of two BC08S data cables and four BC08R modem control cables. *Some units in the field may be observed with H739 or H751 supplies. These are generally equivalent to an H758 supply.			
SIZE	CODE	NUMBER	REV
A	SP	DH11-0-5	B
DEC FORM NO DEC 16-(381)-1022-N370 DRA 108			
SHEET 12 OF 25			

ENGINEERING SPECIFICATION		CONTINUATION SHEET	
TITLE DH11 Multiplexor			
3.5 Continued- cannot receive characters on a line at 30 characters per second, echo them back by auto-echo at 30 characters per second, and transmit an independent message at 30 characters per second, all on the same line. The auto-echo hardware will interlock these functions to some degree, but if more than two characters are received on a line while the scanner is waiting for the transmitter holding buffer to become available (see 3b above), a data overrun will occur and characters will be lost. In short, auto-echo and software-driven transmission should not be attempted on the same line simultaneously if input from that line is expected.			
SIZE	CODE	NUMBER	REV
A	SP	DH11-0-5	B
DEC FORM NO DEC 16-(381)-1022-N370 DRA 108			
SHEET 11 OF 25			

ENGINEERING SPECIFICATION		CONTINUATION SHEET	
TITLE DH11 Multiplexor			
5.0 Programming 5.1 The System Control Register - 000 The System Control Register is a byte-adressable register. The bit assignment is as follows: 000, 001, 002, 003 Line Selection Each of the 16 lines served by the DH11 has its own storage for line parameter information, current address, and byte count. These storage locations are loaded by the program via the Line Parameter Register, Current Address Register, and Byte Count Register, but the hardware must first be told which line is to have its line parameters, current address, or byte count changed. This routing is accomplished by setting the Line Selection bits. These bits are read/write. 004, 005 Memory Extension The information stored in these bits becomes bits 16 and 17 respectively of any current address loaded by the program into the Current Address Register. These bits are read/write, but when read represent only the status of bits 4 and 5 of the System Control Register, NOT the status of the 16th and 17th address bits of the selected line. See the Silo Status Register for further information. The reason for this arrangement is to permit interrupt service routines to save the contents of the System Control Register accurately. 006 Receiver Interrupt Enable This bit, when set, enables receiver interrupts (bit 7). 007 Receiver Interrupt This bit, when set, indicates that the number of characters stored in the silo exceeds the "alarm level" specified by the low byte of the Silo Status Register. This bit is read only, except in Maintenance Mode, when it is read/write. The setting of this bit will generate an interrupt if bit 006 (above) is also set.			
SIZE	CODE	NUMBER	REV
A	SP	DH11-0-5	B
DEC FORM NO DEC 16-(381)-1022-N370 DRA 108			
SHEET 13 OF 25			

ENGINEERING SPECIFICATION		CONTINUATION SHEET	
TITLE DH11 Multiplexor			
5.1 Continued- 008 Clear Non-Existant Memory Interrupt This bit, when set, clears the non-existent memory interrupt flip-flop (bit 10) and clears itself. This bit is read/write. 009 Maintenance (Read/Write) This bit, when set, places the DH11 in Maintenance mode. Maintenance mode is described in Section 5.11. 10 Non-existent Memory This bit is set whenever the NPR hardware within the DH11 addresses a memory location from which no slave sync is received within 20 microseconds. This indicates that the addressed location or device does not exist. This bit causes an interrupt if set while bit 13 (see below) is set. This bit is read only, unless in maintenance mode, at which time it is read/write. 11 Master Clear This bit, when set, generates "Initialize" within the DH11, clearing the silo, the UARTs, and the registers. The exact bits cleared are discussed in Section 5.10 Initialize. This bit is read/write. 12 Storage Interrupt Enable This bit, when set, permits the setting of bit 14 to generate an interrupt. This bit is read/write. 13 Transmit and Non-Ex-Mem Interrupt Enable This bit, when set, permits the setting of bit 10 or 15 to generate an interrupt. This bit is read/write. 14 Storage Interrupt This bit is set whenever the receiver scanner has found a receiver holding buffer with a character in it and desires to store that character in the silo but cannot do so at this time			
SIZE	CODE	NUMBER	REV
A	SP	DH11-0-5	B
DEC FORM NO DEC 16-(381)-1022-N370 DRA 108			
SHEET 14 OF 25			

ENGINEERING SPECIFICATION		CONTINUATION SHEET															
TITLE DH11 Multiplexor																	
5.2 Continued- reader is referred to Section 5.9 for further details on double-buffered reception. 15 Valid Data Present This bit indicates that the data presented in bits 14-000 is valid. This bit permits the use of a character handling program that takes characters from the silo until there are no more available. This is done by reading this register and checking bit 15 until one obtains a word for which bit 15 is zero. The entire Next Received Character Register is read-only and is addressable only on a word basis. 5.3 Line Parameter Register 004 This register should be loaded only after the System Control Register has had its line selection bits arranged to select the line to which these line parameters are to apply. This register is write-only. 000 - 001 Character Length These bits should be set as shown to receive and transmit characters of the length (excluding parity) shown: <table><tr><td>001</td><td>000</td></tr><tr><td>0</td><td>0</td><td>5 bit</td></tr><tr><td>0</td><td>1</td><td>6 bit</td></tr><tr><td>1</td><td>0</td><td>7 bit</td></tr><tr><td>1</td><td>1</td><td>8 bit</td></tr></table> 002 Two Stop Bits This bit, when set, conditions a line transmitting with 6,7, or 8 bit code to transmit characters having two stop marks. If the line is transmitting 5 bit code, assertion of this bit causes the characters to be transmitted with 1.5 stop marks. If this bit is not asserted, 1 stop mark is sent.				001	000	0	0	5 bit	0	1	6 bit	1	0	7 bit	1	1	8 bit
001	000																
0	0	5 bit															
0	1	6 bit															
1	0	7 bit															
1	1	8 bit															
SIZE	CODE	NUMBER	REV														
A	SP	DH11-0-5	B														
DEC FORM NO DEC 16-(381)-1022-N370 DRA 108																	
SHEET 16 OF 25																	

ENGINEERING SPECIFICATION		CONTINUATION SHEET	
TITLE DH11 Multiplexor			
5.1 Continued- because of a lack of space. This bit when set will cause an interrupt if bit 12 is set. This bit is read only, except in Maintenance Mode, at which time it is read/write. 15 Transmitter Interrupt This bit is set whenever the DH11 concludes an NPR cycle that incremented a byte count to zero, indicating the loading of the last character in a message buffer into a UART transmitter holding register. This bit when set will cause an interrupt if bit 13 is set. This bit is read/write. (It is set during an NPR cycle) 5.2 Next Received Character Register 002 000 - 007 These bits contain the next received character, right justified. The least significant bit is in bit 000. Unused bits are 0. The parity bit is not shown. 008 - 11 These bits contain the line number upon which the aforementioned character was received. Bit 8 is the least significant. 12 Parity Error This bit is set if the sense of the parity of the received character does not agree with that designated for that line. 13 Framing Error This bit is set if the received character did not have a stop bit present at the proper time. This bit is usually interpreted as indicating the reception of a "break". 14 Data Overrun This bit is set if the received character was preceded by a character that was lost due to the inability of the receiver scanner to service the UART receiver holding buffer. The			
SIZE	CODE	NUMBER	REV
A	SP	DH11-0-5	B
DEC FORM NO DEC 16-(381)-1022-N370 DRA 108			
SHEET 15 OF 25			

ENGINEERING SPECIFICATION		CONTINUATION SHEET			
TITLE DH11 Multiplexor					
5.3 Continued-					
03	Reserved (Not used)				
04	Parity Enabled				
If this bit is set, characters transmitted on this line will have an appropriate parity bit affixed and characters received on this line will be have their parity checked.					
05	Even Parity				
If this bit is set and bit 4 is set, characters of even parity will be generated on this line and incoming characters will be expected to have even parity. If this bit is not set, but bit 4 is set, characters of odd parity will be generated on this line and incoming characters will be expected to have odd parity. If bit 4 is not set, the setting of this bit is immaterial.					
06 - 09	Receiver Speed				
The state of these bits determines the operating speed for this line's receiver. The speed table below is applicable.					
10 - 13	Transmitter Speed				
The state of these bits determines the operating speed for this line's transmitter. The speed table below is applicable.					
Speed Table for Receiver and Transmitter Speeds:					
Bit	9	8	7	6	
	13	12	11	10	
	0	0	0	0	Zero Baud (See 5.9)
	0	0	0	1	50 baud
	0	0	1	0	75 baud
	0	0	1	1	110 baud
	0	1	0	0	134.5 baud
	0	1	0	1	150 baud
	0	1	1	0	200 baud
	0	1	1	1	300 baud
					SIZE A
					CODE SP
					NUMBER DH11-0-5
					REV B

DEC FORM NO DEC 16-(381)-1022-N370
DRA 108

SHEET 17 OF 25

ENGINEERING SPECIFICATION		CONTINUATION SHEET			
TITLE DH11 Multiplexor					
5.3 Continued-					
Speed Table for Receiver and Transmitter Speeds (Continued):					
Bit	9	8	7	6	
	13	12	11	10	
	1	0	0	0	600 baud
	1	0	0	1	1200 baud
	1	0	1	0	1800 baud
	1	0	1	1	2400 baud
	1	1	0	0	4800 baud
	1	1	0	1	9600 baud
	1	1	1	0	External Input A
	1	1	1	1	External Input B
14					Half-Duplex/Full-Duplex
					If this bit is set, this line is conditioned to operate in half-duplex mode. If this bit is clear, this line is conditioned to operate in full-duplex mode.
					In this application "half-duplex" means that the DH11 receiver is blinded during transmission of a character.
15					Auto-Echo Enable
					When this bit is set, characters received on this line will be hardware echoed. See Section 3.5 for further details.
				5.4 Current Address Register 06	
					This register should be loaded only after the System Control Register has had the appropriate bits set to select the line number to which this current address is to apply. When this register is loaded, address bits 00-15 are transferred into semiconductor memories in the DH11 from bits 00-15 respectively of this register. Address bits 16-17 are transferred into semiconductor memories in the DH11 from bits 4-5 of the System Control Register.
					When this register is read, it will indicate the current address of the line selected by the System Control Register. Bits 16 and 17 will appear in the Silo Status Register.
					SIZE A
					CODE SP
					NUMBER DH11-0-5
					REV B

DEC FORM NO DEC 16-(381)-1022-N370
DRA 108

SHEET 18 OF 25

ENGINEERING SPECIFICATION		CONTINUATION SHEET			
TITLE DH11 Multiplexor					
5.8 Silo Status Register 16					
This register is actually two byte-sized registers. The bit assignments are:					
00 - 05	Silo Alarm Level				
The program writes a number 0,1,2,4,8,16, or 32 into this location. When the number of characters stored in the silo exceeds that number, an interrupt (System Control Register bit 7) is generated, if enabled (System Control Register bit 6 is 1). These bits are read/write.					
06 - 07	Read Extended Memory				
These bits are read only and contain the A16 and A17 bits of the current address for the line to which the line selection bits of the System Control Register are pointing.					
08 - 13	Silo Fill Level				
These bits represent an up-down counter that indicates the actual number of characters in the silo. It should be noted that there are six binary digits; hence numbers between 0 and 63 ₁₀ can be represented. A full silo has 64 ₁₀ entries and appears as 000000, but one may easily tell the difference between an empty silo (000000) and a full silo (000000) by checking the Storage Overflow bit (bit 14 of System Control). These bits are read-only.					
14	Reserved (Not used; this bit is read/write).				
15	Silo Maintenance (See Section 5.11)				
					SIZE A
					CODE SP
					NUMBER DH11-0-5
					REV B

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DRA 108

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ENGINEERING SPECIFICATION		CONTINUATION SHEET			
TITLE DH11 Multiplexor					
5.5 Byte Count Register 10					
In the same fashion as the Line Parameter and Current Address registers, this register should not be loaded or read without first selecting a line number by means of the lower-order four bits of the System Control Register. This register should be loaded with the two's complement*of the number of characters (bytes) to be transmitted on that line. The byte count register is read/write.					
5.6 Buffer Active Register 12					
This register contains one bit for each line. The bits are to be individually set using BIS instructions. Setting a bit initiates transmission on the associated line. The bit is cleared by the hardware when the last character to be transmitted on that line is loaded into the transmitter data holding register of the UART for that line. It should be noted that while the clearing of a BAR bit does indicate that a new message may be sent, it does not indicate that the last characters from the preceding message have been completely sent. Specifically, two more characters will be sent after the BAR bit clears. These are the last two characters of the message; one of them was just starting when the BAR was cleared and one was that final character that was loaded into the holding register, thus clearing the BAR bit. This effect is a normal consequence of double-buffered transmission and is mentioned here for the benefit of programmers who want to write programs that control such modem leads as Request to Send. Clearly, Request to Send should not be dropped until at least two character times after the BAR bit for a given line clears.					
Clearing a BAR bit should not be used to abort transmission on a line. Rather, the byte count for that line should be set to zero. The Buffer Active Register (BAR) bits are read/write.					
5.7 Break Control Register 14					
This register contains one bit for each line. Setting a bit in this register will immediately generate a break condition on the line corresponding to that bit number. Clearing the bit will terminate the break condition. The break condition may be timed by sending characters during the break interval, since these characters will never actually reach the line. Further comments concerning the transmission of break signals may be found in Section 5.9					
*To determine the two's complement, write the number out in binary, complement each bit to obtain the "complement" and then add 1 to get "two's complement".					
					SIZE A
					CODE SP
					NUMBER DH11-0-5
					REV B

DEC FORM NO DEC 16-(381)-1022-N370
DRA 108

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ENGINEERING SPECIFICATION		CONTINUATION SHEET	
TITLE DH11 Multiplexor			
5.9 Programming - Discussion <u>Double Buffered Receivers</u> - General "Double-buffered" receivers contain two registers, one of which is a shift register into which the character being received from the communications line is shifted a bit at a time. The second register is a holding register; when the shift register has assembled a complete character, that character is transferred in a parallel fashion into the holding register. At that time a flag is set and the hardware or software of the system using the double-buffered receiver can access the holding register and remove/copy the data stored there. When the shift register has assembled another character, that character will be transferred into the holding register, obliterating the character previously stored there. If this action takes place before the data in the holding register has been accessed by the aforementioned hardware/software, a "data overrun" flag will be set, indicating that data was lost. <u>Double Buffered Receivers</u> - DH11 The Universal Asynchronous Receiver Transmitters (UARTs) used in the DH11 are MOS/LSI units that each contain a double buffered receiver and a double buffered transmitter. The double buffered receivers found in DH11 UARTs function exactly as described above. In the DH11, the flags indicating presence of data in the holding registers of the double-buffered UART receivers are scanned by an automatic hardware scanner which copies data from holding registers into the "silo" if and only if storage space is available in the silo. If that space is not available, and the scanner finds a flag indicating a holding register with data in it, the "Storage Overflow" bit (System Control Register, bit 14) is set, and an interrupt is generated, if enabled. As indicated in Section 2.9.1.2, the setting of this bit does not necessarily mean that data has been lost. Rather, it indicates that data will be lost if the hardware scanner is unable to service (i.e. dump into the silo) the data in one or more holding registers before additional characters arrive on those lines. Actual data loss will become evident to the program when characters are received with the "Data Overrun" bit set. (See the description of the "Next Received Character Register".)			
SIZE A	CODE SP	NUMBER DH11-0-5	REV B
DEC FORM NO DEC 16-(381)-1022-N370 DRA 108			
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ENGINEERING SPECIFICATION		CONTINUATION SHEET	
TITLE DH11 Multiplexor			
5.9 Continued- <u>Silo</u> The silo, actually more similar in design to a grainery, is a first-in first-out buffer store. A parallel - loaded 16 bit word (see Next Received Character Register for the format) automatically propagates "downward" into the first location not already containing a word. In the case where the silo is empty, this means that the word would propagate directly into the Next Received Character Register. The propagation time from the top of the silo to the bottom may be as much as 32 microseconds. For this reason, the hardware is arranged such that the Receiver Interrupt is not generated until the number of characters in the silo exceeds the "silo alarm level" AND there is at least one character in the bottom of the silo. This arrangement is necessary because the up-down counter that indicates the number of characters in the silo indicates exactly that, the number of characters in the silo, both those resting in the bottom and those propagating downward. While the hardware arrangement protects the case where the silo is empty and the alarm level is zero (if the "AND there is at least one character in the bottom of the silo" was not made a condition in the interrupt generation, the program would receive an interrupt while the single character in the silo was propagating downward), the fact still remains that the number of characters in the silo and the number actually available to be serviced may differ due to the propagation time. For this reason, character handling programs should not assume there are some particular number of characters in the silo when servicing begins. Rather, the program should extract a character, check the "valid data present" bit (bit 15) and handle the character; then the program should extract the next character and repeat the process until bit 15 no longer tests as "1". At that time, the silo may be assumed to be empty (although there may be another character propagating downward) and the character handling routine may be terminated until another Receiver Interrupt is received. On very fast processors, such as the PDP-11/45, the program should avoid reading the Next Received Character Register more often than once per microsecond, as it takes one microsecond for characters in the silo to shift downward one position. Since the typical program will be checking bit 15 and moving the character to some location, it is anticipated that this speed requirement will not pose a problem.			
SIZE A	CODE SP	NUMBER DH11-0-5	REV B
DEC FORM NO DEC 16-(381)-1022-N370 DRA 108			
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ENGINEERING SPECIFICATION		CONTINUATION SHEET	
TITLE DH11 Multiplexor			
5.10 Addresses and Vectors The DH11 uses floating addresses and is located after DJ11's in the floating address space that begins at location 160010. Because the DH11 has eight registers, it must be assigned an address that is a multiple of 20 (octal). All DH11's in a system should have consecutive addresses. <u>Example #1:</u> A system with no DJ11's, but two DH11's: 160010 Cannot use for DH11's because not multiple of 20. 160020 First DH11 160040 Second DH11 160060 DH11 Gap (Indicates that there are no more DH11's). <u>Example #2:</u> A system with one DJ11, two DH11's: 160010 First DJ11 160020 DJ11 Gap (Indicates that there are no more DJ11's). 160030 Cannot use for DH11's because not multiple of 20. 160040 First DH11 160060 Second DH11 160100 DH11 Gap (Indicates that there are no more DH11's). The DH11 vectors (2) follow those of the DJ11 in the floating vector space that starts at address 000. The vectors starting at 300 are used in the following order: DC11; KL11/DL11-A,B; DP11; DM11-A; DN11; DM11-BB; DR11-A; DR11-C; PA011 Readers; PA011 Punches; DT11; DX11; DL11-C,D,E; DJ11; DH11. Of the two DH11 vectors, the receiver vector is the lower numbered vector. The priority of the receiver and transmitter interrupts are individually selectable by means of two standard PDP11 priority jumper plugs. INITIALIZE The Initialize signal clears the Silo, the UARTs, and all registers except the Current Addresses and Byte Counts. All scanners are forced to line 00 but continue operation from there.			
SIZE A	CODE SP	NUMBER DH11-0-5	REV B
DEC FORM NO DEC 16-(381)-1022-N370 DRA 108			
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ENGINEERING SPECIFICATION		CONTINUATION SHEET	
TITLE DH11 Multiplexor			
5.9 Continued- <u>Zero Baud</u> A speed selection of "zero baud" is provided so that the program may turn off any line. This would be useful should excessive circuit noise on an unused line cause the receipt of annoying quantities of bogus characters. <u>BREAK Signals</u> When the Break Control Register has been conditioned to transmit a break signal on a particular line, DH11 logic immediately forces the output on that line to the SPACE (0) condition. As indicated in Section 5.6, the generation of a Transmitter Interrupt occurs when the last character of a message has been loaded into a UART transmitter from a message table in PDP-11 core. It is thus appropriate at that time for the program to set up a new message in core and to load the appropriate current address and byte count so that the new message can begin when the old one is finished. It is important to note that the former message is not "finished" when the Transmitter Interrupt is given. Rather, the use of the core table is finished. In terms of the actual serial communications line, there are two more characters left to go. One of these characters is in the UART transmitter's shift register; the other is in the UART transmitter's holding register. The consequence of the above is that to send a break signal, one should load two nulls and wait for a transmitter interrupt before setting the appropriate bit in the Break Control Register. In this way, generation of a break will not interrupt the transmission of any printing characters. In like manner, when using characters to time the transmission of a break signal, nulls should be used so that when the break condition is terminated by clearing the bit in the Break Control Register, no printing characters will be produced from the UART shift and holding registers.			
SIZE A	CODE SP	NUMBER DH11-0-5	REV B
DEC FORM NO DEC 16-(381)-1022-N370 DRA 108			
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ENGINEERING SPECIFICATION		CONTINUATION SHEET	
TITLE DH11 Multiplexor			
5.10 Maintenance Bits and Their Function Setting of SCR 09 (Maintenance) does the following: 1) It enables the ability of the program to write SCR 07 (Receiver Interrupt), SCR 10 (Non-Existant Memory Interrupt), and SCR 14 (Storage Overflow Interrupt) bits. This write capability is normally not enabled as it can produce hardware/software synchronization problems unless carefully done. 2) It loops the transmitted data leads (serial out line 00-15) to the received data leads (serial in line 00-15). Setting of SSR 15 (Silo Maintenance) causes the inputs of the silo to be set to a 10101010101010 bit pattern, and a single 16-bit character made up of this pattern to be loaded into the silo. Successive clears and sets of SSR 15 will repeat this procedure. All receiver speeds should be set to zero baud and the silo emptied before this is done, so that no data from the incoming serial lines will be placed in the silo while it is under test.			
		SIZE A	CODE SP
		NUMBER DH11-0-5	REV B

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DIGITAL EQUIPMENT CORPORATION

FIRST USED ON OPTION MODEL		QTY.	DESCRIPTION	PART NO.	ITEM NO.	
PDP 11			PARTS LIST			
DRN.	DATE	 DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS TITLE WIRE LIST				
CHK'D	DATE					
ENG.	DATE					
PROJ. ENG.	DATE					
PROD.	DATE					
NEXT HIGHER ASSEMBLY						
D-1A-7009180-0-0						
SCALE	SHEET		SIZE	CODE	NUMBER	REV.
1	OF	1	K	WL	DH11-0-2	C

DH11.C RUN NAME	A/P	WRP200.V34(62)-1		31-JUL-75		DRAW	RV	RG	Y	X	Z	REMARKS	12-JUL-76	16136	PAGE 1	RUN NUMBER	
		PIN NAME	ORDER PIN	BAY - ORDER	Q								NC	LENGTH	EXCEPTIONS		
+5V 1	H	A07B1		1-A1 *	1						1			N	3-1/R		1
+5V 1	H	A03V2		1-A2 *							2			N	6-7/B		1
+5V 1	H	C01U1		1-A3 *													1
+5V 1	H			1											10-0/B		1
+5V 2	H	C02U1		1-A1 *	1						1			N	6-3/B		2
+5V 2	H	A03U2		1-A2 *													2
+5V 2	H			1											6-3/B		2
-5V 1	L	A07B2		1-A1 *	1						1			N	6-5/B		3
-5V 1	L	C09B2		1-A2 *							2			N	4		3
-5V 1	L	C02B2		1-A3 *							1			N	1		3
-5V 1	L	C01B2		1-A4 *													3
-5V 1	L			1											11-5/B		3
-5V 2	L	D01B2		1-A1 *	2						2			N	1		4
-5V 2	L	D02B2		1-A2 *							1			N	4		4
-5V 2	L	D09B2		1-A3 *													4
-5V 2	L			1											5-0/B		4
100 BAUD	H	F09T2				D06									1-PIN RUN		5
110 BAUD	H	F00H1		1-A1 *		D05- 3					1			N	1		6
110 BAUD	H	F09H1		1-A2 *		D06											6
110 BAUD	H			1											1-2/B		6
1200 BAUD	H	F00J1		1-A1 *		D05- 3					1			N	1		7
1200 BAUD	H	F09J1		1-A2 *		D06											7
1200 BAUD	H			1											1-4/B		7
134.5 BAUD	H	F00V2		1-A1 *		D05- 3					1			N	1		8
134.5 BAUD	H	F09V2		1-A2 *		D06											8
134.5 BAUD	H			1											1-0/R		8
150 BAUD	H	F00K1		1-A1 *		D05- 3					1			N	1		9
150 BAUD	H	F09K1		1-A2 *		D06											9
150 BAUD	H			1											1-2/R		9
1800 BAUD	H	F00U2		1-A1 *		D05- 3					1			N	1		10
1800 BAUD	H	F09U2		1-A2 *		D06											10
1800 BAUD	H			1											1-2/B		10
2.53 MHZ	H	F05E1		1-A1 *		D11- 1					1			N	2-4/B		11
2.53 MHZ	H	F09E1		1-A2 *		D06											11
2.53 MHZ	H			1											2-4/B		11
200 BAUD	H	F00R1		1-A1 *		D05- 3					1			N	1		12
200 BAUD	H	F09R1		1-A2 *		D06											12
200 BAUD	H			1											1-2/R		12
2400 BAUD	H	F00D1		1-A1 *		D05- 3					1			N	1		13
2400 BAUD	H	F09D1		1-A2 *		D06											13
2400 BAUD	H			1											1-2/B		13

DH11.C RUN NAME	A/P	WRP280.V34(62)-1 PIN NAME	ORDER PIN	31-JUL-75 RAY - ORDER	Q	DRAW RV RG Y X Z OPT	12-JUL-76 REMARKS	16136 NC LENGTH EXCEPTIONS FLAG	PAGE 2 RUN NUMBER
300 BAUD	H	F08L1		1-01 *		D05- 3		N 1	14
300 BAUD	H	F09L1		1-02 *		D06			14
300 BAUD	H			1				1-0/8	14
3600 BAUD	H	F09A1				D06		1-PIN RUN	15
4000 BAUD	H	F08N1		1-01 *		D05- 3		N 1	16
4000 BAUD	H	F09N1		1-02 *		D06			16
4000 BAUD	H			1				1-0/8	16
5.060 MHZ	H	D09N1		1-01 *		D01- 2		N 5-5/8	17
5.060 MHZ	H	F09M2		1-02 *		D06			17
5.060 MHZ	H			1				5-5/8	17
90 BAUD	H	F08P1		1-01 *		D05- 3		N 1	18
90 BAUD	H	F09P1		1-02 *		D06			18
90 BAUD	H			1				1-0/8	18
600 BAUD	H	F08S1		1-01 *		D05- 3		N 1	19
600 BAUD	H	F09S1		1-02 *		D06			19
600 BAUD	H			1				1-0/8	19
7200 BAUD	H	F09C1				D06		1-PIN RUN	20
75 BAUD	H	F08F1		1-01 *		D05- 3		N 1	21
75 BAUD	H	F09F1		1-02 *		D06			21
75 BAUD	H			1				1-0/8	21
9600 BAUD	H	F08B1		1-01 *		D05- 3		N 1	22
9600 BAUD	H	F09B1		1-02 *		D06			22
9600 BAUD	H			1				1-0/8	22
A INTR DONE	H	A06L2		1-01 *		D07		N 1	23
A INTR DONE	H	A06R1		1-02 *		D07			23
A INTR DONE	H			1				1-0/8	23
A START INTR	L	A06D2		1-01 *		D07		N 1-6/8	24
A START INTR	L	A06R2		1-02 *		D07		N 0-4/8	24
A START INTR	L	A06N1		1-03 *		D07			24
A START INTR	L			1				2-2/8	24
ADDRS TO BUS	H	A03R2		1-01 *		D12- 1		N 2-2/8	25
ADDRS TO BUS	H	B02R1		1-02 *		D07			25
ADDRS TO BUS	H			1				2-2/8	25
ADDRS TO BUS	L	A04M1		1-01 *		D13- 2		N 3-3/8	26
ADDRS TO BUS	L	B02F1		1-02 *		D07			26
ADDRS TO BUS	L			1				3-3/8	26
AE ENAB 00	H	D05S2		1-01 *		D11- 1		N 2	27
AE ENAB 00	H	D05S2		1-02 *		D05- 1			27
AE ENAB 00	H			1				2-0/8	27
AE ENAB 01	H	D05V2		1-01 *		D11- 1		N 2	28
AE ENAB 01	H	D05V2		1-02 *		D05- 1			28
AE ENAB 01	H			1				2-0/8	28

DH11.C RUN NAME	WRP288.V34(62)-1 31-JUL-75										12-JUL-76		16136 PAGE 4		RUN NUMBER
	A/P	PIN NAME	ORDER PIN	BAY - ORDER	Q	DRAW OPT	RV	RG	Y	X	Z	REMARKS	NC FLAG	LENGTH EXCEPTIONS	
AE GO	L	C0482		1-01 *		D13- 1					1		N	5-1/8	43
AE GO	L	E05K1		1-02 *		D11- 1									43
AE GO	L			1										5-1/8	43
AE STROBE	H	A05N2		1-01 *		D11- 1					1		N	8-7/8	44
AE STROBE	H	D03E1		1-02 *		D12- 1									44
AE STROBE	H			1										8-7/8	44
B INTR DONE	H	A06M2		1-01 *		D07					1		N	1	45
B INTR DONE	H	A06S1		1-02 *		D07									45
B INTR DONE	H			1										1-0/8	45
B START INTR	L	A06P2		1-01 *		D07					1		N	0-4/8	46
B START INTR	L	A06S2		1-02 *		D07									46
B START INTR	L			1										0-4/8	46
BAR 00	H	D03K1		1-01 *		D12- 2					1		N	3-5/8	47
BAR 00	H	E04K2		1-02 *		D13- 1									47
BAR 00	H			1										3-5/8	47
BAR 01	H	E03F2		1-01 *		D12- 2					1		N	1-3/8	48
BAR 01	H	E04N1		1-02 *		D13- 1									48
BAR 01	H			1										1-3/8	48
BAR 02	H	E04S1		1-01 *		D13- 1					1		N	2-3/8	49
BAR 02	H	F03E1		1-02 *		D17- 2									49
BAR 02	H			1										2-3/8	49
BAR 03	H	E03V2		1-01 *		D12- 2					1		N	1	50
BAR 03	H	E04V2		1-02 *		D13- 1									50
BAR 03	H			1										1-0/8	50
BAR 04	H	D03E2		1-01 *		D12- 2					1		N	7-5/8	51
BAR 04	H	F04T2		1-02 *		D13- 1									51
BAR 04	H			1										7-5/8	51
BAR 05	H	C04S1		1-01 *		D13- 1					1		N	4-5/8	52
BAR 05	H	E03E2		1-02 *		D12- 2									52
BAR 05	H			1										4-5/8	52
BAR 06	H	E03P2		1-01 *		D12- 2					1		N	2-7/8	53
BAR 06	H	F04J1		1-02 *		D13- 1									53
BAR 06	H			1										2-7/8	53
BAR 07	H	F03A1		1-01 *		D12- 2					1		N	1-3/8	54
BAR 07	H	F04E2		1-02 *		D13- 1									54
BAR 07	H			1										1-3/8	54
BAR 08	H	C03R1		1-01 *		D12- 3					1		N	5-3/8	55
BAR 08	H	E04K1		1-02 *		D13- 1									55
BAR 08	H			1										5-3/8	55
BAR 09	H	C03R1		1-01 *		D12- 3					1		N	7-1/8	56
BAR 09	H	E04M1		1-02 *		D13- 1									56
BAR 09	H			1										7-1/8	56

DH11.C		WRP288.V34(62)-1 31-JUL-75										12-JUL-76		16136		PAGE 5		RUN NUMBER
RUN NAME		A/P	PIN NAME	OPDEP PIN	PAY - ORDER	Q	DRAW OPT	RV	PG	Y	X	Z	REMARKS	NC FLAG	LENGTH	EXCEPTIONS		
BAR 10		H	B03N1		1-01 *		D12- 3					1		N	9-1/8		57	
BAR 10		H	E04S2		1-02 *		D13- 1										57	
BAR 10		H			1										9-1/8		57	
BAR 11		H	A03V1		1-01 *		D12- 3					1		N	11-1/8		58	
BAR 11		H	E04U1		1-02 *		D13- 1										58	
BAR 11		H			1										11-1/8		58	
BAR 12		H	B03E1		1-01 *		D12- 3					1		N	11-3/8		59	
BAR 12		H	F04E1		1-02 *		D13- 1										59	
BAR 12		H			1										11-3/8		59	
BAR 13		H	B03R1		1-01 *		D12- 3					1		N	10-5/8		60	
BAR 13		H	F04H2		1-02 *		D13- 1										60	
BAR 13		H			1										10-5/8		60	
BAR 14		H	C03H1		1-01 *		D12- 3					1		N	9-7/8		61	
BAR 14		H	F04P2		1-02 *		D13- 1										61	
BAR 14		H			1										9-7/8		61	
BAR 15		H	C03S1		1-01 *		D12- 3					1		N	8-7/8		62	
BAR 15		H	F04S1		1-02 *		D13- 1										62	
BAR 15		H			1										8-7/8		62	
BC MEM WRITE ENAB		L	B03T2		1-01 *		D12- 1					1		N	7-1/8		63	
BC MEM WRITE ENAB		L	E04H1		1-02 *		D13- 2										63	
BC MEM WRITE ENAB		L			1										7-1/8		63	
BG 4 AB		H	A07S1		1-01 *		D08					1		N	0-5/8		64	
BG 4 AB		H	A07T2		1-02 *		D08										64	
BG 4 AB		H			1										0-5/8		64	
BG 4 BC		H	A07C1		1-01 *		D08					1		N	13-7/8		65	
BG 4 BC		H	E02L2		1-02 *		D09					2		N	3-3/8		65	
BG 4 BC		H	F01E1		1-03 *		D08										65	
BG 4 BC		H			1										17-2/8		65	
BG 4 IN A		H	A07S2		1-01 *		D08					1		N	4-7/8		66	
BG 4 IN A		H	B01E2		1-02 *		D08										66	
BG 4 IN A		H			1										4-7/8		66	
BG 4 OUT C		H	B09E2		1-01 *		D08					1		N	12-1/8		67	
BG 4 OUT C		H	E02K2		1-02 *		D09					2		N	2-7/8		67	
BG 4 OUT C		H	F01A1		1-03 *		D08										67	
BG 4 OUT C		H			1										15-0/8		67	
BG 5 AB		H	A07P1		1-01 *		D08					1		N	0-5/8		68	
BG 5 AB		H	A07R2		1-02 *		D08										68	
BG 5 AB		H			1										0-5/8		68	
BG 5 IN A		H	A07P2		1-01 *		D08					1		N	4-7/8		69	
BG 5 IN A		H	B01B1		1-02 *		D08										69	
BG 5 IN A		H			1										4-7/8		69	

QH11.C		WRP200.V34(62)-1 31-JUL-75										12-JUL-76		16136 PAGE 10		RUN NUMBER
RUN NAME		A/P	PIN NAME	ORDER PIN	BAY - ORDER	Q	DRAW OPT	RV	RG	Y	X	Z	REMARKS	NC FLAG	LENGTH EXCEPTIONS	
BUS	A11	L	B09N1		1-01 *		D10					1		N	3	112
BUS	A11	L	B04N1		1-02 *		D13- 2					2		N	2	112
BUS	A11	L	B01N1		1-03 *		D09					1		N	8	112
BUS	A11	L	E01L1		1-04 *		D09									112
BUS	A11	L			1										13-0/8	112
BUS	A12	L	B09P2		1-01 *		D10					1		N	3	113
BUS	A12	L	B04P2		1-02 *		D13- 2					2		N	2	113
BUS	A12	L	B01P2		1-03 *		D09					1		N	7-1/8	113
BUS	A12	L	E01C1		1-04 *		D09									113
BUS	A12	L			1										12-1/8	113
BUS	A13	L	B09P1		1-01 *		D10					1		N	3	114
BUS	A13	L	B04P1		1-02 *		D13- 2					2		N	2	114
BUS	A13	L	B01P1		1-03 *		D09					1		N	7-7/8	114
BUS	A13	L	E01K2		1-04 *		D09									114
BUS	A13	L			1										12-7/8	114
BUS	A14	L	B09R2		1-01 *		D10					1		N	3	115
BUS	A14	L	B04R2		1-02 *		D13- 2					2		N	2	115
BUS	A14	L	B01R2		1-03 *		D09					1		N	7-7/8	115
BUS	A14	L	E01K1		1-04 *		D09									115
BUS	A14	L			1										12-7/8	115
BUS	A15	L	B09R1		1-01 *		D10					1		N	3	116
BUS	A15	L	B04R1		1-02 *		D13- 2					2		N	2	116
BUS	A15	L	B01R1		1-03 *		D09					1		N	7-1/8	116
BUS	A15	L	E01D2		1-04 *		D09									116
BUS	A15	L			1										12-1/8	116
BUS	A16	L	B09S2		1-01 *		D10					1		N	3	117
BUS	A16	L	B04S2		1-02 *		D13- 2					2		N	2	117
BUS	A16	L	B01S2		1-03 *		D09					1		N	7	117
BUS	A16	L	E01E2		1-04 *		D09									117
BUS	A16	L			1										12-0/8	117
BUS	A17	L	B09S1		1-01 *		D10					1		N	3	118
BUS	A17	L	B04S1		1-02 *		D13- 2					2		N	2	118
BUS	A17	L	B01S1		1-03 *		D09					1		N	6-7/8	118
BUS	A17	L	E01D1		1-04 *		D09									118
BUS	A17	L			1										11-7/8	118
BUS	AC LO	L	B01F1		1-01 *		D10					1		N	4-4/8	119
BUS	AC LO	L	B09F1		1-02 *		D10									119
BUS	AC LO	L			1										4-4/8	119
BUS	BBSY	L	A09P2		1-01 *		D10					2		N	2-6/8	120
BUS	BBSY	L	A06D1		1-02 *		D07					1		N	2-4/8	120
BUS	BBSY	L	A02D1		1-03 *		D07					2		N	1-7/8	120
BUS	BBSY	L	A01P2		1-04 *		D09					1		N	12-5/8	120
BUS	BBSY	L	F01D1		1-05 *		D09									120
BUS	BBSY	L			1										19-6/8	120

DH11.C		WRP200.V34(62)-1 31-JUL-75										12-JUL-76		16136 PAGE 11		RUN NUMBER
RUN NAME		A/P	PIN NAME	ORDEP PIN	RAY - ORDER	Q	DRAW OPT	RV	RG	Y	X	Z	REMARKS	NC FLAG	LENGTH EXCEPTIONS	
BUS C0	L		B09U2		1-01 *		D10					2		N	3	121
BUS C0	L		B04U2		1-02 *		D13-	1				1		N	1-7/8	121
BUS C0	L		B02K7		1-03 *		D07					2		N	1-7/8	121
BUS C0	L		B01U2		1-04 *		D09					1		N	7-1/8	121
BUS C0	L		E01J2		1-05 *		D09									121
BUS C0	L				1										13-7/8	121
BUS C1	L		B09T2		1-01 *		D10					2		N	3	122
BUS C1	L		B04T2		1-02 *		D13-	1				1		N	2-4/8	122
BUS C1	L		B02D1		1-03 *		D07					2		N	2-1/8	122
BUS C1	L		B01T2		1-04 *		D09					1		N	7	122
BUS C1	L		E01F2		1-05 *		D09									122
BUS C1	L				1										14-5/8	122
BUS DATA 00	L		A09C1		1-01 *		D10					1		N	3-4/8	123
BUS DATA 00	L		A03C1		1-02 *		D12-	2				2		N	1-4/8	123
BUS DATA 00	L		A01C1		1-03 *		D09					1		N	11-5/8	123
BUS DATA 00	L		E02F1		1-04 *		D09									123
BUS DATA 00	L				1										16-5/8	123
BUS DATA 01	L		A09D2		1-01 *		D10					1		N	3-4/8	124
BUS DATA 01	L		A03D2		1-02 *		D12-	1				2		N	1-4/8	124
BUS DATA 01	L		A01D2		1-03 *		D09					1		N	11-5/8	124
BUS DATA 01	L		E02K1		1-04 *		D09									124
BUS DATA 01	L				1										16-5/8	124
BUS DATA 02	L		A09D1		1-01 *		D10					2		N	1-7/8	125
BUS DATA 02	L		A06E2		1-02 *		D07					1		N	2-1/8	125
BUS DATA 02	L		A03D1		1-03 *		D12-	1				2		N	1-4/8	125
BUS DATA 02	L		A01D1		1-04 *		D09					1		N	11-3/8	125
BUS DATA 02	L		E02R2		1-05 *		D09					2		N	4-1/8	125
BUS DATA 02	L		F01E2		1-06 *		D09									125
BUS DATA 02	L				1										21-0/8	125
BUS DATA 03	L		A09E2		1-01 *		D10					2		N	2-5/8	126
BUS DATA 03	L		A06L1		1-02 *		D07					1		N	2-3/8	126
BUS DATA 03	L		A03E2		1-03 *		D12-	2				2		N	1-4/8	126
BUS DATA 03	L		A01E2		1-04 *		D09					1		N	11-5/8	126
BUS DATA 03	L		E02J1		1-05 *		D09					2		N	3-7/8	126
BUS DATA 03	L		F01L1		1-06 *		D09									126
BUS DATA 03	L				1										22-0/8	126
BUS DATA 04	L		A09E1		1-01 *		D10					2		N	1-7/8	127
BUS DATA 04	L		A06N2		1-02 *		D07					1		N	3-1/8	127
BUS DATA 04	L		A03E1		1-03 *		D12-	1				2		N	1-4/8	127
BUS DATA 04	L		A01E1		1-04 *		D09					1		N	13-7/8	127
BUS DATA 04	L		F02B1		1-05 *		D09					2		N	1-7/8	127
BUS DATA 04	L		F01N2		1-06 *		D09									127
BUS DATA 04	L				1										22-2/8	127

DH11.C RUN NAME	A/P	WRP288.V34(62)-1		31-JUL-75		DRAW OPT	RV	RG	Y	X	Z	REMARKS	12-JUL-76	16136 NC FLAG	PAGE 14		RUN NUMBER
		DIN NAME	ORDER PIN	BAY - ORDER	Q										LENGTH	EXCEPTIONS	
BUS PA	L	A01M1		1-01 *		D10					1			N	4-4/8		146
BUS PA	L	A09M1		1-02 *		D10											146
BUS PA	L			1											4-4/8		146
BUS PB	L	A01N2		1-01 *		D10					1			N	4-4/8		147
BUS PB	L	A09N2		1-02 *		D10											147
BUS PB	L			1											4-4/8		147
BUS REQ A	L	A06U2		1-01 *		D08					1			N	2		148
BUS REQ A	L	A07J2		1-02 *		D08											148
BUS REQ A	L			1											2-0/8		148
BUS REQ B	L	A06P1		1-01 *		D07					1			N	1-3/8		149
BUS REQ B	L	A07J1		1-02 *		D08											149
BUS REQ B	L			1											1-3/8		149
BUS SACK	L	A09R2		1-01 *		D10					2			N	2-1/8		150
BUS SACK	L	A06T2		1-02 *		D07					1			N	2-4/8		150
BUS SACK	L	A02T2		1-03 *		D07								N	1		150
BUS SACK	L	A01R2		1-04 *		D09					1			N	14		150
BUS SACK	L	F01T2		1-05 *		D09											150
BUS SACK	L			1											19-5/8		150
BUS SSYN	L	A02C1		1-01 *		D07					1			N	2-4/8		151
BUS SSYN	L	A06C1		1-02 *		D07					2			N	6-3/8		151
BUS SSYN	L	B09U1		1-03 *		D10					1			N	3		151
BUS SSYN	L	B04U1		1-04 *		D13- 1					2			N	2		151
BUS SSYN	L	B01U1		1-05 *		D09					1			N	7-1/8		151
BUS SSYN	L	E01J1		1-06 *		D09					2			N	2-5/8		151
BUS SSYN	L	F01C1		1-07 *		D09											151
BUS SSYN	L			1											23-5/8		151
CA 00	H	A04E1		1-01 *		D13- 2					1			N	8-7/8		152
CA 00	H	D03J2		1-02 *		D12- 2											152
CA 00	H			1											8-7/8		152
CA 01	H	A04D1		1-01 *		D13- 2					1			N	11-5/8		153
CA 01	H	E03F1		1-02 *		D12- 2											153
CA 01	H			1											11-5/8		153
CA 02	H	A04C1		1-01 *		D13- 2					1			N	12-3/8		154
CA 02	H	E03M1		1-02 *		D12- 2											154
CA 02	H			1											12-3/8		154
CA 03	H	A04F1		1-01 *		D13- 2					1			N	12-7/8		155
CA 03	H	E03V1		1-02 *		D12- 2											155
CA 03	H			1											12-7/8		155
CA 04	H	A04R1		1-01 *		D13- 2					1			N	8-1/8		156
CA 04	H	D03K2		1-02 *		D12- 2											156
CA 04	H			1											8-1/8		156
CA 05	H	A04P1		1-01 *		D13- 2					1			N	9-1/8		157
CA 05	H	D03V2		1-02 *		D12- 2											157
CA 05	H			1											9-1/8		157

DH11.C RUN NAME	A/P	WRP288.V34(62)-1		31-JUL-75		DRAW OPT	RV	RG	Y	X	Z	REMARKS	12-JUL-76	16136 NC FLAG	PAGE 15		RUN NUMBER
		DIN NAME	ORDER PIN	BAY - ORDER	Q										LENGTH	EXCEPTIONS	
CA 06	H	A04L1		1-01 *		D13- 2					1			N	11-7/8		158
CA 06	H	E03P1		1-02 *		D12- 2											158
CA 06	H			1											11-7/8		158
CA 07	H	A04R2		1-01 *		D13- 2					1			N	12-7/8		159
CA 07	H	F03R1		1-02 *		D12- 2											159
CA 07	H			1											12-7/8		159
CA 08	H	B04A1		1-01 *		D13- 2					1			N	4-7/8		160
CA 08	H	C03S2		1-02 *		D12- 3											160
CA 08	H			1											4-7/8		160
CA 09	H	A04V1		1-01 *		D13- 2					1			N	4-3/8		161
CA 09	H	C03C1		1-02 *		D12- 3											161
CA 09	H			1											4-3/8		161
CA 10	H	A04U2		1-01 *		D13- 2					1			N	3-1/8		162
CA 10	H	B03M1		1-02 *		D12- 3											162
CA 10	H			1											3-1/8		162
CA 11	H	A03B1		1-01 *		D12- 3					1			N	2		163
CA 11	H	B04B1		1-02 *		D13- 2											163
CA 11	H			1											2-0/8		163
CA 12	H	B03E2		1-01 *		D12- 3					1			N	2-5/8		164
CA 12	H	C04A1		1-02 *		D13- 2											164
CA 12	H			1											2-5/8		164
CA 13	H	B03P1		1-01 *		D12- 3					1			N	1-5/8		165
CA 13	H	B04V2		1-02 *		D13- 2											165
CA 13	H			1											1-5/8		165
CA 14	H	B04F1		1-01 *		D13- 2					1			N	3-3/8		166
CA 14	H	C03H2		1-02 *		D12- 3											166
CA 14	H			1											3-3/8		166
CA 15	H	C03R2		1-01 *		D12- 3					1			N	2-1/8		167
CA 15	H	C04B1		1-02 *		D13- 2											167
CA 15	H			1											2-1/8		167
CLEAR CYCLE	L	D01P2		1-01 *		D09					2			N	1		168
CLEAR CYCLE	L	D02P2		1-02 *		D09					1			N	5-7/8		168
CLEAR CYCLE	L	F02R1		1-03 *		D09											168
CLEAR CYCLE	L			1											6-7/8		168
CLEAR NUX	L	D01J1		1-01 *		D09					2			N	1		169
CLEAR NUX	L	D02J1		1-02 *		D09					1			N	6-1/8		169
CLEAR NUX	L	F02M2		1-03 *		D09											169
CLEAR NUX	L			1											7-1/8		169
CLR REQ	L	B02D2		1-01 *		D07					2			N	2-1/8		170
CLR REQ	L	B02U2		1-02 *		D07					1			N	4-3/8		170
CLR REQ	L	D03D1		1-03 *		D12- 1											170
CLR REQ	L			1											6-4/8		170

DH11.C		WRP288.V34(62)-1		31-JUL-75		12-JUL-76		16136		PAGE 20		RUN	
RUN NAME		A/P	PIN	ORDER	RAY - Q	DRAW	RV RG Y	X Z	REMARKS	NC	LENGTH	EXCEPTIONS	RUN NUMBER
			NAME	PIN	ORDER								
GND 01			A01B2		1-01 *	D10		2		N	0-1/0		217
GND 01			A01C2		1-02 *	D10		1		N	1-5/0		217
GND 01			A01N1		1-03 *	D10		2		N	0-1/0		217
GND 01			A01P1		1-04 *	D10		1		N	0-1/0		217
GND 01			A01R1		1-05 *	D10		2		N	0-1/0		217
GND 01			A01S1		1-06 *	D10		1		N	0-1/0		217
GND 01			A01T1		1-07 *	D10		2		N	1-5/0		217
GND 01			B01B2		1-08 *	D10		1		N	0-1/0		217
GND 01			B01C2		1-09 *	D10		2		N	0-1/0		217
GND 01			B01D1		1-10 *	D10		1		N	0-1/0		217
GND 01			B01E1		1-11 *	D10		2		N	1-7/0		217
GND 01			B01T1		1-12 *	D10		1		N	0-4/0		217
GND 01			B01V2		1-13 *	D10		2		N	1-1/0		217
GND 01			C01C2		1-14 *			1		N	2-1/0		217
GND 01			C01T1		1-15 *			2		N	1-5/0		217
GND 01			D01C2		1-16 *			1		N	2-1/0		217
GND 01			D01T1		1-17 *			2		N	1-1/0		217
GND 01			E01A1		1-18 *	D09		1		N	0-4/0		217
GND 01			E01C2		1-19 *			2		N	2-1/0		217
GND 01			E01T1		1-20 *			1		N	1-5/0		217
GND 01			F01C2		1-21 *			2		N	1-1/0		217
GND 01			F01J2		1-22 *	D09		1		N	1-5/0		217
GND 01			F01T1		1-23 *								217
GND 01					1						21-6/0		217
GND 02			A02H2		1-01 *	2		2		N	1		218
GND 02			A02C2		1-02 *			1		N	1-1/0		218
GND 02			A02J2		1-03 *	D07		2		N	1-3/0		218
GND 02			A02R1		1-04 *	D07		1		N	0-4/0		218
GND 02			A02T1		1-05 *			2		N	1-5/0		218
GND 02			B02C2		1-06 *			1		N	0-4/0		218
GND 02			B02C1		1-07 *	D07		2		N	1-2/0		218
GND 02			B02J2		1-08 *	D07		1		N	1-2/0		218
GND 02			B02P1		1-09 *	D07		2		N	0-1/0		218
GND 02			B02R1		1-10 *	D07		1		N	0-4/0		218
GND 02			B02T1		1-11 *			2		N	1-3/0		218
GND 02			C02C2		1-12 *			1		N	2-1/0		218
GND 02			C02T1		1-13 *			2		N	1-5/0		218
GND 02			D02C2		1-14 *			1		N	2-1/0		218
GND 02			D02T1		1-15 *			2		N	1-3/0		218
GND 02			E02C2		1-16 *			1		N	2-1/0		218
GND 02			E02T1		1-17 *			2		N	1-5/0		218
GND 02			F02B2		1-18 *	D09		1		N	0-1/0		218
GND 02			F02C2		1-19 *			2		N	2-1/0		218
GND 02			F02T1		1-20 *								218
GND 02					1						23-7/0		218

DH11.C		WRP288.V34(67)-1		31-JUL-75		12-JUL-76		16136		PAGE 21		RUN						
RUN NAME		A/P	PIN	ORDER	RAY -	Q	DRAW	RV	RG	Y	X	Z	REMARKS	NC	LENGTH	EXCEPTIONS	RUN	
			NAME	PIN	ORDER		OPT								FLAG			NUMBER
GND	03		A02E1		1-01 *	2						2		N	1-3/0			219
GND	03		A03C2		1-02 *							1		N	2-1/0			219
GND	03		A03T1		1-03 *							2		N	1-5/0			219
GND	03		B03C2		1-04 *							1		N	2-1/0			219
GND	03		B03T1		1-05 *							2		N	1-3/0			219
GND	03		C03C2		1-06 *							1		N	2-1/0			219
GND	03		C03T1		1-07 *							2		N	1-5/0			219
GND	03		D03C2		1-08 *							1		N	2-1/0			219
GND	03		D03T1		1-09 *							2		N	1-3/0			219
GND	03		E03C2		1-10 *							1		N	2-1/0			219
GND	03		F03T1		1-11 *							2		N	1-5/0			219
GND	03		F03C2		1-12 *							1		N	2-1/0			219
GND	03		F03T1		1-13 *													219
GND	03				1										21-6/0			219
GND	04		A04C2		1-01 *							1		N	2-1/0			220
GND	04		A04T1		1-02 *							2		N	1-5/0			220
GND	04		B04C2		1-03 *							1		N	2-1/0			220
GND	04		B04T1		1-04 *							2		N	1-3/0			220
GND	04		C04C2		1-05 *							1		N	2-1/0			220
GND	04		C04T1		1-06 *							2		N	1-5/0			220
GND	04		D04C2		1-07 *							1		N	2-1/0			220
GND	04		D04T1		1-08 *							2		N	1-3/0			220
GND	04		E04C2		1-09 *							1		N	2-1/0			220
GND	04		E04T1		1-10 *							2		N	1-5/0			220
GND	04		F04C2		1-11 *							1		N	2-1/0			220
GND	04		F04T1		1-12 *													220
GND	04				1										20-3/0			220
GND	05		A05C2		1-01 *							1		N	2-1/0			221
GND	05		A05T1		1-02 *							2		N	1-5/0			221
GND	05		B05C2		1-03 *							1		N	2-1/0			221
GND	05		B05T1		1-04 *							2		N	1-3/0			221
GND	05		C05C2		1-05 *							1		N	2-1/0			221
GND	05		C05T1		1-06 *							2		N	1-5/0			221
GND	05		D05C2		1-07 *							1		N	2-1/0			221
GND	05		D05T1		1-08 *							2		N	1-3/0			221
GND	05		E05C2		1-09 *							1		N	2-1/0			221
GND	05		E05T1		1-10 *							2		N	1-5/0			221
GND	05		F05C2		1-11 *							1		N	2-1/0			221
GND	05		F05T1		1-12 *													221
GND	05				1										20-3/0			221

DN11.C	WRP200,V34(62)-1	31-JUL-75	12-JUL-76	16136	PAGE 22		
RUN NAME	A/P PIN NAME	ORDER PIN	BAY - ORDER	Q DRAW RV RG Y X Z	REMARKS	NC LENGTH EXCEPTIONS	RUN NUMBER
				OPT		FLAG	
GND 06	A06C2	1-01 *				N 1-1/8	222
GND 06	A06J2	1-02 *		D07		N 1-5/8	222
GND 06	A06T1	1-03 *				N 1-5/8	222
GND 06	B06C2	1-04 *				N 2-1/8	222
GND 06	B06T1	1-05 *				N 1-3/8	222
GND 06	C06C2	1-06 *				N 2-1/8	222
GND 06	C06T1	1-07 *				N 1-5/8	222
GND 06	D06C2	1-08 *				N 2-1/8	222
GND 06	D06T1	1-09 *				N 1-3/8	222
GND 06	E06C2	1-10 *				N 2-1/8	222
GND 06	E06T1	1-11 *				N 1-5/8	222
GND 06	F06C2	1-12 *				N 2-1/8	222
GND 06	F06T1	1-13 *					222
GND 06		1				21-0/8	222
GND 07	A07C2	1-01 *				N 2-1/8	223
GND 07	A07T1	1-02 *				N 1-3/8	223
GND 07	B07A1	1-03 *		D02		N 0-1/8	223
GND 07	B07B1	1-04 *		D02		N 3-1/8	223
GND 07	C07C2	1-05 *				N 2-1/8	223
GND 07	C07T1	1-06 *				N 1-5/8	223
GND 07	D07C2	1-07 *				N 2-1/8	223
GND 07	D07T1	1-08 *				N 1-3/8	223
GND 07	E07C2	1-09 *				N 2-1/8	223
GND 07	E07T1	1-10 *				N 1-5/8	223
GND 07	F07C2	1-11 *				N 2-1/8	223
GND 07	F07T1	1-12 *					223
GND 07		1				19-7/8	223
GND 08	A08C2	1-01 *				N 2-1/8	224
GND 08	A08T1	1-02 *				N 1-5/8	224
GND 08	B08C2	1-03 *				N 2-1/8	224
GND 08	B08T1	1-04 *				N 1-3/8	224
GND 08	C08C2	1-05 *				N 2-1/8	224
GND 08	C08T1	1-06 *				N 1-5/8	224
GND 08	D08C2	1-07 *				N 2-1/8	224
GND 08	D08T1	1-08 *				N 1-3/8	224
GND 08	E08C2	1-09 *				N 2-1/8	224
GND 08	E08T1	1-10 *				N 1-5/8	224
GND 08	F08C2	1-11 *				N 1-2/8	224
GND 08	F08K2	1-12 *		D05- 3	EXT A BAUD	N 1-1/8	224
GND 08	F08R2	1-13 *		D05- 3	EXT B BAUD	N 0-4/8	224
GND 08	F08T1	1-14 *				N 0-4/8	224
GND 08	F08V1	1-15 *		D05- 3	Z0 BAUD		224
GND 08		1				21-5/8	224

DH11.C RUN NAME	A/P	WRP200.V34(62)-1 PIN NAME	ORDER PIN	31-JUL-75 RAY - ORDER	Q	DRAW OPT	RV RG Y	X	Z	REMARKS	16136 NC FLAG	PAGE 23 LENGTH EXCEPTIONS	RUN NUMBER
GND 09		A09B2		1-01 *		D10			1		N	0-1/8	225
GND 09		A09C2		1-02 *		D10			2		N	1-5/8	225
GND 09		A09N1		1-03 *		D10			1		N	0-1/8	225
GND 09		A09P1		1-04 *		D10			2		N	0-1/8	225
GND 09		A09R1		1-05 *		D10			1		N	0-1/8	225
GND 09		A09S1		1-06 *		D10			2		N	0-1/8	225
GND 09		A09T1		1-07 *					1		N	0-4/8	225
GND 09		A09V2		1-08 *		D10			2		N	1-2/8	225
GND 09		B09B2		1-09 *		D10			1		N	0-1/8	225
GND 09		B09C2		1-10 *		D10			2		N	0-1/8	225
GND 09		B09D1		1-11 *		D10			1		N	0-1/8	225
GND 09		B09E1		1-12 *		D10			2		N	1-7/8	225
GND 09		B09T1		1-13 *		D10			1		N	0-4/8	225
GND 09		B09V2		1-14 *		D10			2		N	1-1/8	225
GND 09		C09C2		1-15 *					1		N	2-1/8	225
GND 09		C09S1		1-16 *		D01- 1			2	BP BIT IS DATA	N	1-5/8	225
GND 09		C09T1		1-17 *					1		N	1-5/8	225
GND 09		D09C2		1-18 *					2		N	2-1/8	225
GND 09		D09T1		1-19 *					1		N	1-3/8	225
GND 09		E09C2		1-20 *					2		N	2-1/8	225
GND 09		E09T1		1-21 *					1		N	1-5/8	225
GND 09		F09C2		1-22 *					2		N	2-1/8	225
GND 09		F09T1		1-23 *									225
GND 09				1								295-5/8	225
GROUP 0-7	H	D02R2		1-01 *		D09			1		N	0-1/8	226
GROUP 0-7	H	D02S2		1-02 *		D09			2		N	0-4/8	226
GROUP 0-7	H	D02U1		1-03 *		D09			1		N	0-1/8	226
GROUP 0-7	H	D02V1		1-04 *		D09			2		N	2-3/8	226
GROUP 0-7	H	E02P1		1-05 *		D09							226
GROUP 0-7	H			1								3-1/8	226
GROUP 0-15	H	D01R2		1-01 *		D09			1		N	0-1/8	227
GROUP 0-15	H	D01S2		1-02 *		D09			2		N	0-4/8	227
GROUP 0-15	H	D01U1		1-03 *		D09			1		N	0-1/8	227
GROUP 0-15	H	D01V1		1-04 *		D09			2		N	1-7/8	227
GROUP 0-15	H	E02F1		1-05 *		D09			1		N	4-7/8	227
GROUP 0-15	H	F02V2		1-06 *		D09							227
GROUP 0-15	H			1								7-4/8	227
HALF DUPLEX 00	H	E05B1		1-01 *		D11- 4			1		N	2	228
HALF DUPLEX 00	H	E05B1		1-02 *		D05- 1							228
HALF DUPLEX 00	H			1								2-0/8	228
HALF DUPLEX 01	H	D05K2		1-01 *		D11- 4			1		N	2	229
HALF DUPLEX 01	H	D05K2		1-02 *		D05- 1							229
HALF DUPLEX 01	H			1								2-0/8	229
HALF DUPLEX 02	H	D05D2		1-01 *		D11- 4			1		N	2	230
HALF DUPLEX 02	H	D05D2		1-02 *		D05- 1							230
HALF DUPLEX 02	H			1								2-0/8	230
HALF DUPLEX 03	H	C05R2		1-01 *		D11- 4			1		N	2	231
HALF DUPLEX 03	H	C05R2		1-02 *		D05- 1							231
HALF DUPLEX 03	H			1								2-0/8	231

DH11.C	WRP200.V34(62)-1 31-Jul-75										12-Jul-76	16136	PAGE 28	RUN	
RUN NAME	A/P	PIN NAME	ORDER PIN	RAY - ORDER	Q	DRAW OPT	RV	RG	Y	X	Z	REMARKS	NC LENGTH EXCEPTIONS	FLAG	NUMBER
MUX CARRIER	L	D01B1		1-01 *		D09					2		N	1	286
MUX CARRIER	L	D02B1		1-02 *		D09					1		N	2-7/8	286
MUX CARRIER	L	E02A1		1-03 *		D09									286
MUX CARRIER	L			1										3-7/8	286
MUX CLEAR TO SEND	L	D01C1		1-01 *		D09					2		N	1	287
MUX CLEAR TO SEND	L	D02C1		1-02 *		D09					1		N	3-1/8	287
MUX CLEAR TO SEND	L	E02D1		1-03 *		D09									287
MUX CLEAR TO SEND	L			1										4-1/8	287
MUX LINE EN	L	D01K1		1-01 *		D09					2		N	1	288
MUX LINE EN	L	D02K1		1-02 *		D09					1		N	3-5/8	288
MUX LINE EN	L	E02P2		1-03 *		D09									288
MUX LINE EN	L			1										4-5/8	288
MUX LINE EN 1	H	D01N2		1-01 *		D09					2		N	0-5/8	289
MUX LINE EN 1	H	D01S1		1-02 *		D09					1		N	0-5/8	289
MUX LINE EN 1	H	D01V2		1-03 *		D09									289
MUX LINE EN 1	H			1										1-2/8	289
MUX LINE EN 2	H	D02N2		1-01 *		D09					2		N	0-5/8	290
MUX LINE EN 2	H	D02S1		1-02 *		D09					1		N	0-5/8	290
MUX LINE EN 2	H	D02V2		1-03 *		D09									290
MUX LINE EN 2	H			1										1-2/8	290
MUX RING	L	D02F2		1-01 *		D09					2		N	1	291
MUX RING	L	D01F2		1-02 *		D09					1		N	2-5/8	291
MUX RING	L	E02C1		1-03 *		D09									291
MUX RING	L			1										3-5/8	291
MUX RG TO SEND	L	D01H1		1-01 *		D09					2		N	1	292
MUX RG TO SEND	L	D02H1		1-02 *		D09					1		N	3-7/8	292
MUX RG TO SEND	L	E02N2		1-03 *		D09									292
MUX RG TO SEND	L			1										4-7/8	292
MUX SEC RX	L	D01A1		1-01 *		D09					2		N	1	293
MUX SEC RX	L	D02A1		1-02 *		D09					1		N	3-1/8	293
MUX SEC RX	L	E02B1		1-03 *		D09									293
MUX SEC RX	L			1										4-1/8	293
MUX SEC TX	L	D01L1		1-01 *		D09					2		N	1	294
MUX SEC TX	L	D02L1		1-02 *		D09					1		N	3-5/8	294
MUX SEC TX	L	E02R2		1-03 *		D09									294
MUX SEC TX	L			1										4-5/8	294
MUX TERM RDY	L	D01F1		1-01 *		D09					2		N	1	295
MUX TERM RDY	L	D02F1		1-02 *		D09					1		N	4-1/8	295
MUX TERM RDY	L	E02S2		1-03 *		D09									295
MUX TERM RDY	L			1										5-1/8	295

DH11.C		WRP200.V34(62)-1 31-Jul-75										12-Jul-76		16136 PAGE 29		RUN	
RUN	NAMP	A/P	PIN NAME	ORDER PIN	RAY - ORDER	Q	DRAW OPT	RV	RG	Y	X	Z	REMARKS	NC FLAG	LENGTH EXCEPTIONS	NUMBER	
NB1	LPR 00	H	C06F2		1-01 *		D03- 5					2		N	1	296	
NB1	LPR 00	H	C07F2		1-02 *		D04- 5					1		N	1-6/8	296	
NB1	LPR 00	H	C07T2		1-03 *		D04- 3					2		N	1	296	
NB1	LPR 00	H	C06T2		1-04 *		D03- 3					1		N	2-1/8	296	
NB1	LPR 00	H	D07H1		1-05 *		D04- 4					2		N	1	296	
NB1	LPR 00	H	D06H1		1-06 *		D03- 4					1		N	1-7/8	296	
NB1	LPR 00	H	D06U2		1-07 *		D03- 4					2		N	1	296	
NB1	LPR 00	H	D07U2		1-08 *		D04- 4					1		N	1-7/8	296	
NB1	LPR 00	H	E07J1		1-09 *		D04- 2					2		N	1	296	
NB1	LPR 00	H	F06J1		1-10 *		D03- 2					1		N	1-5/8	296	
NB1	LPR 00	H	E06U1		1-11 *		D03- 3					2		N	1	296	
NB1	LPR 00	H	F07U1		1-12 *		D04- 3					1		N	1-7/8	296	
NB1	LPR 00	H	F06F2		1-13 *		D03- 5					2		N	1	296	
NB1	LPR 00	H	F07F2		1-14 *		D04- 5					1		N	1-6/8	296	
NB1	LPR 00	H	F07T2		1-15 *		D04- 2					2		N	1	296	
NB1	LPR 00	H	F06T2		1-16 *		D03- 2					1		N	2-6/8	296	
NB1	LPR 00	H	F03H2		1-17 *		D12- 2									296	
NB1	LPR 00	H			1										23-5/8	296	
NB2	LPR 01	H	C07E1		1-01 *		D04- 5					2		N	1	297	
NB2	LPR 01	H	C06E1		1-02 *		D03- 5					1		N	1-6/8	297	
NB2	LPR 01	H	C06S1		1-03 *		D03- 3					2		N	1	297	
NB2	LPR 01	H	C07S1		1-04 *		D04- 3					1		N	2-1/8	297	
NB2	LPR 01	H	D06F2		1-05 *		D03- 4					2		N	1	297	
NB2	LPR 01	H	D07F2		1-06 *		D04- 4					1		N	2-1/8	297	
NB2	LPR 01	H	D07U1		1-07 *		D04- 4					2		N	1	297	
NB2	LPR 01	H	D06U1		1-08 *		D03- 4					1		N	1-7/8	297	
NB2	LPR 01	H	E06H2		1-09 *		D03- 2					2		N	1	297	
NB2	LPR 01	H	E07H2		1-10 *		D04- 2					1		N	1-5/8	297	
NB2	LPR 01	H	E07T2		1-11 *		D04- 3					2		N	1	297	
NB2	LPR 01	H	E06T2		1-12 *		D03- 3					1		N	2-1/8	297	
NB2	LPR 01	H	F07F1		1-13 *		D04- 5					2		N	1-5/8	297	
NB2	LPR 01	H	F07S2		1-14 *		D04- 2					1		N	1	297	
NB2	LPR 01	H	F06S2		1-15 *		D03- 2					2		N	1-5/8	297	
NB2	LPR 01	H	F06F1		1-16 *		D03- 5					1		N	2-1/8	297	
NB2	LPR 01	H	F03H1		1-17 *		D12- 2									297	
NB2	LPR 01	H			1										24-0/8	297	
NRC	00	H	C09A1		1-01 *		D01- 2					1		N	5-2/8	298	
NRC	00	H	D03F1		1-02 *		D12- 2									298	
NRC	00	H			1										5-2/8	298	
NRC	01	H	C09B1		1-01 *		D01- 2					1		N	8-5/8	299	
NRC	01	H	E03D2		1-02 *		D12- 2									299	
NRC	01	H			1										8-5/8	299	
NRC	02	H	C09C1		1-01 *		D01- 2					1		N	9-3/8	300	
NRC	02	H	E03H2		1-02 *		D12- 2									300	
NRC	02	H			1										9-3/8	300	
NRC	03	H	C09D1		1-01 *		D01- 2					1		N	10-3/8	301	
NRC	03	H	E03U1		1-02 *		D12- 2									301	
NRC	03	H			1										10-3/8	301	

DN11.C RUN NAME	A/P	WRP200.V34(62)-1 PIN NAME	ORDER PIN	31-JUL-75 BAY - ORDER	Q	DRAW OPT	RV RG Y	X	Z	12-JUL-76 REMARKS	16:36 NC LENGTH EXCEPTIONS FLAG	PAGE 32	RUN NUMBER
DEV LPR 05	L	C06F1		1-01 *		D03- 5			2		N 1		317
DEV LPR 05	L	C07F1		1-02 *		D04- 5			1		N 1-7/8		317
DEV LPR 05	L	C07U2		1-03 *		D04- 3			2		N 1		317
DEV LPR 05	L	C06U2		1-04 *		D03- 3			1		N 2		317
DEV LPR 05	L	D06H2		1-05 *		D03- 4			2		N 1		317
DEV LPR 05	L	D07H2		1-06 *		D04- 4			1		N 1-7/8		317
DEV LPR 05	L	D07V1		1-07 *		D04- 4			2		N 1		317
DEV LPR 05	L	D06V1		1-08 *		D03- 4			1		N 1-7/8		317
DEV LPR 05	L	E06J2		1-09 *		D03- 2			2		N 1		317
DEV LPR 05	L	E07J2		1-10 *		D04- 2			1		N 1-5/8		317
DEV LPR 05	L	E07U2		1-11 *		D04- 3			2		N 1		317
DEV LPR 05	L	E06U2		1-12 *		D03- 3			1		N 2-1/8		317
DEV LPR 05	L	F07H1		1-13 *		D04- 5			2		N 1		317
DEV LPR 05	L	F06H1		1-14 *		D03- 5			1		N 1-6/8		317
DEV LPR 05	L	F06U1		1-15 *		D03- 2			2		N 1		317
DEV LPR 05	L	F07U1		1-16 *		D04- 2			1		N 2-7/8		317
DEV LPR 05	L	F03N1		1-17 *		D12- 2							317
DEV LPR 05	L			1							24-0/8		317
RCV DATA ENABLE	H	D05E1		1-01 *		D11- 3			1		N 1-3/8		318
RCV DATA ENABLE	H	D06D2		1-02 *		D03- 2			2		N 1		318
RCV DATA ENABLE	H	D07D2		1-03 *		D04- 2							318
RCV DATA ENABLE	H			1							2-3/8		318
RCV INTR REQ	H	A06U1		1-01 *		D07			1		N 0-1/8		319
RCV INTR REQ	H	A06V1		1-02 *		D07			2		N 0-3/8		319
RCV INTR REQ	H	D05P1		1-03 *		D11- 2							319
RCV INTR REQ	H			1							0-4/8		319
RCV SCAN A	H	D09H1		1-01 *		D01- 1			2		N 2-7/8		320
RCV SCAN A	H	D05P2		1-02 *		D11- 1			1		N 2-7/8		320
RCV SCAN A	H	E06M1		1-03 *		D03- 4			2		N 1		320
RCV SCAN A	H	E07H1		1-04 *		D04- 4							320
RCV SCAN A	H			1							6-6/8		320
RCV SCAN B	H	D09J1		1-01 *		D01- 1			2		N 3-1/8		321
RCV SCAN B	H	D05P1		1-02 *		D11- 1			1		N 2-7/8		321
RCV SCAN B	H	E06K2		1-03 *		D03- 4			2		N 1		321
RCV SCAN B	H	E07K2		1-04 *		D04- 4							321
RCV SCAN B	H			1							7-0/8		321
RCV SCAN C	H	D09H2		1-01 *		D01- 1			1		N 4-1/8		322
RCV SCAN C	H	E07H1		1-02 *		D04- 2			2		N 1		322
RCV SCAN C	H	E06H1		1-03 *		D03- 4			1		N 0-4/8		322
RCV SCAN C	H	E05K2		1-04 *		D11- 1							322
RCV SCAN C	H			1							5-5/8		322
RCV SCAN D	H	D09F2		1-01 *		D01- 1			2		N 2-2/8		323
RCV SCAN D	H	D07N1		1-02 *		D04- 2			1		N 3-3/8		323
RCV SCAN D	H	E05H1		1-03 *		D11- 1							323
RCV SCAN D	H			1							5-5/8		323
RCV SCAN D	L	D06N1		1-01 *		D03- 2			1		N 2-3/8		324
RCV SCAN D	L	E05F2		1-02 *		D11- 1							324
RCV SCAN D	L			1							2-3/8		324

DN11.C RUN NAME	A/P	WRP200.V34(62)-1 PIN NAME	ORDER PIN	31-JUL-75 BAY - ORDER	Q	DRAW OPT	RV RG Y	X	Z	12-JUL-76 REMARKS	16:36 NC LENGTH EXCEPTIONS FLAG	PAGE 33	RUN NUMBER
READ NRC	H	D09K1		1-01 *		D01- 2			1		N 4-6/8		325
READ NRC	H	E04P1		1-02 *		D13- 1							325
READ NRC	H			1							4-6/8		325
READY IN	L	C09L1		1-01 *		D01- 2			1		N 6-7/8		326
READY IN	L	E05D1		1-02 *		D11- 1							326
READY IN	L			1							6-7/8		326
REQUEST BUS (1)	H	A02U1		1-01 *		D07			1		N 0-1/8		327
REQUEST BUS (1)	H	A02V1		1-02 *		D07			2		N 3-2/8		327
REQUEST BUS (1)	H	B02V1		1-03 *		D07			1		N 2-3/8		327
REQUEST BUS (1)	H	B09R1		1-04 *		D11- 1							327
REQUEST BUS (1)	H			1							5-6/8		327
RESET DA	H	A03H2		1-01 *		D11- 1			1		N 0-7/8		328
RESET DA	H	D06K1		1-02 *		D03- 2			2		N 1		328
RESET DA	H	D07K1		1-03 *		D04- 2							328
RESET DA	H			1							9-7/8		328
RX CLOCK LINE 00	L	E06L1		1-01 *		D03- 2			1		N 1-7/8		329
RX CLOCK LINE 00	L	E08A1		1-02 *		D05- 1							329
RX CLOCK LINE 00	L			1							1-7/8		329
RX CLOCK LINE 01	L	D08R2		1-01 *		D05- 1			1		N 7-1/8		330
RX CLOCK LINE 01	L	F06V2		1-02 *		D03- 2							330
RX CLOCK LINE 01	L			1							7-1/8		330
RX CLOCK LINE 02	L	D08J2		1-01 *		D05- 1			1		N 6-1/8		331
RX CLOCK LINE 02	L	F06A1		1-02 *		D03- 3							331
RX CLOCK LINE 02	L			1							6-1/8		331
RX CLOCK LINE 03	L	C06V2		1-01 *		D03- 3			1		N 1-4/8		332
RX CLOCK LINE 03	L	C08V2		1-02 *		D05- 1							332
RX CLOCK LINE 03	L			1							1-4/8		332
RX CLOCK LINE 04	L	B08M1		1-01 *		D05- 2			1		N 6-1/8		333
RX CLOCK LINE 04	L	D06K2		1-02 *		D03- 4							333
RX CLOCK LINE 04	L			1							6-1/8		333
RX CLOCK LINE 05	L	B08D2		1-01 *		D05- 2			1		N 9-3/8		334
RX CLOCK LINE 05	L	E06D1		1-02 *		D03- 4							334
RX CLOCK LINE 05	L			1							9-3/8		334
RX CLOCK LINE 06	L	A08R2		1-01 *		D05- 2			1		N 14-3/8		335
RX CLOCK LINE 06	L	F06K1		1-02 *		D03- 5							335
RX CLOCK LINE 06	L			1							14-3/8		335
RX CLOCK LINE 07	L	A08J2		1-01 *		D05- 2			1		N 6-7/8		336
RX CLOCK LINE 07	L	C06J1		1-02 *		D03- 5							336
RX CLOCK LINE 07	L			1							6-7/8		336
RX CLOCK LINE 08	L	D08V2		1-01 *		D05- 3			1		N 2-5/8		337
RX CLOCK LINE 08	L	E07L1		1-02 *		D04- 2							337
RX CLOCK LINE 08	L			1							2-5/8		337

DH11.C RUN NAME	A/P	WRP208.V34(62)-1 PIN NAME	31-JUL-75 ORDER PIN	BAY - ORDER	Q	DRAW OPT	R V R G Y X Z	REMARKS	16136 NC LENGTH EXCEPTIONS FLAG	PAGE 34 RUN NUMBER
RX CLOCK LINE 09	L	D08P2		1-01 *		D05- 3			N 6-5/8	338
RX CLOCK LINE 09	L	F07V2		1-02 *		D04- 2				338
RX CLOCK LINE 09	L			1					6-5/8	338
RX CLOCK LINE 10	L	D08H2		1-01 *		D05- 3			N 5-5/8	339
RX CLOCK LINE 10	L	F07A1		1-02 *		D04- 3				339
RX CLOCK LINE 10	L			1					5-5/8	339
RX CLOCK LINE 11	L	C07V2		1-01 *		D04- 3			N 0-5/8	340
RX CLOCK LINE 11	L	C08U2		1-02 *		D05- 3				340
RX CLOCK LINE 11	L			1					0-5/8	340
RX CLOCK LINE 12	L	B08K2		1-01 *		D05- 4			N 6-1/8	341
RX CLOCK LINE 12	L	D07K2		1-02 *		D04- 4				341
RX CLOCK LINE 12	L			1					6-1/8	341
RX CLOCK LINE 13	L	B08B1		1-01 *		D05- 4			N 8-7/8	342
RX CLOCK LINE 13	L	E07D1		1-02 *		D04- 4				342
RX CLOCK LINE 13	L			1					8-7/8	342
RX CLOCK LINE 14	L	A08N2		1-01 *		D05- 4			N 14-1/8	343
RX CLOCK LINE 14	L	F07K1		1-02 *		D04- 5				343
RX CLOCK LINE 14	L			1					14-1/8	343
RX CLOCK LINE 15	L	A08H2		1-01 *		D05- 4			N 6-3/8	344
RX CLOCK LINE 15	L	C07J1		1-02 *		D04- 5				344
RX CLOCK LINE 15	L			1					6-3/8	344
SCR 00	H	B08D1		1-01 *		D11- 2			N 6-5/8	345
SCR 00	H	D03F2		1-02 *		D12- 2			N 3-1/8	345
SCR 00	H	E04F1		1-03 *		D13- 2				345
SCR 00	H			1					9-6/8	345
SCR 01	H	B08A1		1-01 *		D11- 2			N 8-7/8	346
SCR 01	H	E04E2		1-02 *		D13- 2			N 1-3/8	346
SCR 01	H	E03C1		1-03 *		D12- 2				346
SCR 01	H			1					10-2/8	346
SCR 02	H	A08V1		1-01 *		D11- 2			N 9-3/8	347
SCR 02	H	E04D2		1-02 *		D13- 2			N 1-3/8	347
SCR 02	H	E03L2		1-03 *		D12- 2				347
SCR 02	H			1					10-6/8	347
SCR 03	H	A08R1		1-01 *		D11- 2			N 10-3/8	348
SCR 03	H	E04E1		1-02 *		D13- 2			N 1-7/8	348
SCR 03	H	E0382		1-03 *		D12- 2				348
SCR 03	H			1					12-2/8	348
SCR 04	H	B08P1		1-01 *		D11- 2			N 2-3/8	349
SCR 04	H	C04E1		1-02 *		D13- 2			N 3-5/8	349
SCR 04	H	D03H2		1-03 *		D12- 2				349
SCR 04	H			1					6-0/8	349

DN11.C RUN NAME	A/P	WPP200,V34(62)-1 PIN NAME	31-JUL-75 ORDER PIN	PAY - ORDER	Q	DRAW OPT	RV	RG	Y	X	Z	REMARKS	12-JUL-76	16136 NC LENGTH FLAG	PAGE 35 EXCEPTIONS	RUN NUMBER
SCR 05	H	D0581		1-01 *		D11- 2					2			N	1-5/8	350
SCR 05	H	C0402		1-02 *		D13- 2					1			N	6-1/8	350
SCR 05	H	E03B1		1-03 *		D12- 2										350
SCR 05	H			1											7-6/8	350
SCR 06	H	C05F1		1-01 *		D11- 2					1			N	7-3/8	351
SCR 06	H	E03R2		1-02 *		D12- 2										351
SCR 06	H			1											7-3/8	351
SCR 07	H	D05R1		1-01 *		D11- 2					1			N	6-7/8	352
SCR 07	H	F03D1		1-02 *		D12/ 2										352
SCR 07	H			1											6-7/8	352
SCR 08	H	C03-2		1-01 *		D12- 3					1			N	7-1/8	353
SCR 08	H	E05U1		1-02 *		D11- 2										353
SCR 08	H			1											7-1/8	353
SCR 09	H	C03E1		1-01 *		D12- 3					1			N	10-5/8	354
SCR 09	H	F05N2		1-02 *		D11- 2										354
SCR 09	H			1											10-5/8	354
SCR 10	H	B03L1		1-01 *		D12- 3					1			N	11-7/8	355
SCR 10	H	F05L1		1-02 *		D11- 2										355
SCR 10	H			1											11-7/8	355
SCR 11	H	B03A1		1-01 *		D12- 3					1			N	10-1/8	356
SCR 11	H	E04L2		1-02 *		D13- 1					2			N	3-3/8	356
SCR 11	H	F05K2		1-03 *		D11- 2										356
SCR 11	H			1											13-4/8	356
SCR 12	H	B03B1		1-01 *		D12- 3					1			N	12-3/8	357
SCR 12	H	F05H1		1-02 *		D11- 2										357
SCR 12	H			1											12-3/8	357
SCR 13	H	B03M2		1-01 *		D12- 3					1			N	11-3/8	358
SCR 13	H	F05H2		1-02 *		D11- 2										358
SCR 13	H			1											11-3/8	358
SCR 14	H	C03E2		1-01 *		D12- 3					1			N	5-1/8	359
SCR 14	H	D05S1		1-02 *		D11- 2										359
SCR 14	H			1											5-1/8	359
SCR 15	H	C03N1		1-01 *		D12- 3					1			N	9-7/8	360
SCR 15	H	F05R2		1-02 *		D11- 2										360
SCR 15	H			1											9-7/8	360
SELECT 00	H	E01S2		1-01 *		D09					1			N	2-5/8	361
SELECT 00	H	F02F2		1-02 *		D09										361
SELECT 00	H			1											2-5/8	361
SELECT 02	H	D02T2		1-01 *		D09					2			N	1	362
SELECT 02	H	D01T2		1-02 *		D09					1			N	3	362
SELECT 02	H	E01T2		1-03 *		D09					2			N	2-7/8	362
SELECT 02	H	F02L2		1-04 *		D09										362
SELECT 02	H			1											6-7/8	362

DN11.C RUN NAME	A/P	WRP280.V34(62)-1 PIN NAME	31-JUL-75 ORDER PIN	BAY - ORDER	Q	DRAW OPT	RV RG Y	X	Z	REMARKS	12-JUL-76	16136 NC LENGTH EXCEPTIONS FLAG	PAGE 36	RUN NUMBER
SERIAL IN 00	H	EP5L2		1-01 *		D11- 4			1			N 1		363
SERIAL IN 00	H	EP6L2		1-02 *		D03- 2								363
SERIAL IN 00	H			1								1-0/0		363
SERIAL IN 01	H	F05V1		1-01 *		D11- 4			1			N 1		364
SERIAL IN 01	H	F06V1		1-02 *		D03- 2								364
SERIAL IN 01	H			1								1-0/0		364
SERIAL IN 02	H	E05V2		1-01 *		D11- 4			1			N 1		365
SERIAL IN 02	H	E06V2		1-02 *		D03- 3								365
SERIAL IN 02	H			1								1-0/0		365
SERIAL IN 03	H	C05V1		1-01 *		D11- 4			1			N 1		366
SERIAL IN 03	H	C06V1		1-02 *		D03- 3								366
SERIAL IN 03	H			1								1-0/0		366
SERIAL IN 04	H	D05L1		1-01 *		D11- 4			1			N 1		367
SERIAL IN 04	H	D06L1		1-02 *		D03- 4								367
SERIAL IN 04	H			1								1-0/0		367
SERIAL IN 05	H	E05E1		1-01 *		D11- 4			1			N 1		368
SERIAL IN 05	H	E06E1		1-02 *		D03- 4								368
SERIAL IN 05	H			1								1-0/0		368
SERIAL IN 06	H	F05J2		1-01 *		D11- 4			1			N 1		369
SERIAL IN 06	H	F06J2		1-02 *		D03- 5								369
SERIAL IN 06	H			1								1-0/0		369
SERIAL IN 07	H	C05J2		1-01 *		D11- 4			1			N 1		370
SERIAL IN 07	H	C06J2		1-02 *		D03- 5								370
SERIAL IN 07	H			1								1-0/0		370
SERIAL IN 08	H	B05P2		1-01 *		D11- 4			1			N 8-7/0		371
SERIAL IN 08	H	E07L2		1-02 *		D04- 2								371
SERIAL IN 08	H			1								8-7/0		371
SERIAL IN 09	H	C05A1		1-01 *		D11- 4			1			N 11-5/0		372
SERIAL IN 09	H	F07V1		1-02 *		D04- 2								372
SERIAL IN 09	H			1								11-5/0		372
SERIAL IN 10	H	B05U2		1-01 *		D11- 4			1			N 9-3/0		373
SERIAL IN 10	H	E07V2		1-02 *		D04- 3								373
SERIAL IN 10	H			1								9-3/0		373
SERIAL IN 11	H	B05V2		1-01 *		D11- 4			1			N 3-5/0		374
SERIAL IN 11	H	C07V1		1-02 *		D04- 3								374
SERIAL IN 11	H			1								3-5/0		374
SERIAL IN 12	H	A05L1		1-01 *		D11- 4			1			N 9-3/0		375
SERIAL IN 12	H	D07L1		1-02 *		D04- 4								375
SERIAL IN 12	H			1								9-3/0		375
SERIAL IN 13	H	A05J1		1-01 *		D11- 4			1			N 11-3/0		376
SERIAL IN 13	H	E07E1		1-02 *		D04- 4								376
SERIAL IN 13	H			1								11-3/0		376

DN11.C RUN NAME	A/P	WRP280.V34(62)-1 PIN NAME	31-JUL-75 ORDER PIN	BAY - ORDER	Q	DRAW OPT	RV RG Y	X	Z	REMARKS	12-JUL-76	16136 NC LENGTH EXCEPTIONS FLAG	PAGE 37	RUN NUMBER
SERIAL IN 14	H	A05E2		1-01 *		D11- 4			1			N 15-1/0		377
SERIAL IN 14	H	F07J2		1-02 *		D04- 5								377
SERIAL IN 14	H			1								15-1/0		377
SERIAL IN 15	H	A05H1		1-01 *		D11- 4			1			N 7-1/0		378
SERIAL IN 15	H	C07J2		1-02 *		D04- 5								378
SERIAL IN 15	H			1								7-1/0		378
SERIAL OUT 00	H	E06A1		1-01 *		D03- 2			2			N 1		379
SERIAL OUT 00	H	E05A1		1-02 *		D11- 4			1			N 4-7/0		379
SERIAL OUT 00	H	F03L2		1-03 *		D12- 2								379
SERIAL OUT 00	H			1								5-7/0		379
SERIAL OUT 01	H	F03J2		1-01 *		D12- 2			1			N 1-3/0		380
SERIAL OUT 01	H	F05P2		1-02 *		D11- 4			2			N 1		380
SERIAL OUT 01	H	F06P2		1-03 *		D03- 2								380
SERIAL OUT 01	H			1								2-3/0		380
SERIAL OUT 02	H	E06R1		1-01 *		D03- 3			2			N 1		381
SERIAL OUT 02	H	E05R1		1-02 *		D11- 4			1			N 3-7/0		381
SERIAL OUT 02	H	F03R2		1-03 *		D12- 2								381
SERIAL OUT 02	H			1								4-7/0		381
SERIAL OUT 03	H	C06N1		1-01 *		D03- 3			2			N 1		382
SERIAL OUT 03	H	C05N1		1-02 *		D11- 4			1			N 9-5/0		382
SERIAL OUT 03	H	F03T2		1-03 *		D12- 2								382
SERIAL OUT 03	H			1								10-5/0		382
SERIAL OUT 04	H	D06A1		1-01 *		D03- 4			2			N 1		383
SERIAL OUT 04	H	D05A1		1-02 *		D11- 4			1			N 8-1/0		383
SERIAL OUT 04	H	F03R1		1-03 *		D12- 2								383
SERIAL OUT 04	H			1								9-1/0		383
SERIAL OUT 05	H	D06R2		1-01 *		D03- 4			2			N 1		384
SERIAL OUT 05	H	D05R2		1-02 *		D11- 4			1			N 5-5/0		384
SERIAL OUT 05	H	F03E2		1-03 *		D12- 2								384
SERIAL OUT 05	H			1								6-5/0		384
SERIAL OUT 06	H	F03S1		1-01 *		D12- 2			1			N 2-3/0		385
SERIAL OUT 06	H	F05D2		1-02 *		D11- 4			2			N 1		385
SERIAL OUT 06	H	F06D2		1-03 *		D03- 5								385
SERIAL OUT 06	H			1								3-3/0		385
SERIAL OUT 07	H	C06B1		1-01 *		D03- 5			2			N 1		386
SERIAL OUT 07	H	C05B1		1-02 *		D11- 4			1			N 10-3/0		386
SERIAL OUT 07	H	F03L1		1-03 *		D12- 2								386
SERIAL OUT 07	H			1								11-3/0		386
SERIAL OUT 08	H	B05N2		1-01 *		D11- 4			1			N 6-7/0		387
SERIAL OUT 08	H	D03R2		1-02 *		D12- 3			2			N 2-7/0		387
SERIAL OUT 08	H	E07A1		1-03 *		D04- 2								387
SERIAL OUT 08	H			1								9-6/0		387

DN11.C RUN NAME	A/P	PIN NAME	ORDER PIN	31-JUL-75 PAY - ORDER	Q	DRAW OPT	RV	RG	Y	X	Z	12-JUL-76 REMARKS	16136 NC LENGTH FLAG	PAGE 38 EXCEPTIONS	RUN NUMBER
SERIAL OUT 09	H	B03V2		1-01 *		D12- 3					2		N	1-7/8	388
SERIAL OUT 09	H	B08R2		1-02 *		D11- 4					1		N	11-5/8	388
SERIAL OUT 09	H	F07P2		1-03 *		D04- 2									388
SERIAL OUT 09	H			1										13-4/8	388
SERIAL OUT 10	H	B0582		1-01 *		D11- 4					2		N	4-1/8	389
SERIAL OUT 10	H	C03V2		1-02 *		D12- 3					1		N	6-7/8	389
SERIAL OUT 10	H	E07R1		1-03 *		D04- 3									389
SERIAL OUT 10	H			1										11-0/8	389
SERIAL OUT 11	H	B05T2		1-01 *		D11- 4					2		N	3-1/8	390
SERIAL OUT 11	H	C07N1		1-02 *		D04- 3					1		N	3-2/8	390
SERIAL OUT 11	H	D03B1		1-03 *		D12- 3									390
SERIAL OUT 11	H			1										6-3/8	390
SERIAL OUT 12	H	A05M1		1-01 *		D11- 4					1		N	8-1/8	391
SERIAL OUT 12	H	D07A1		1-02 *		D04- 4					2		N	3	391
SERIAL OUT 12	H	D03R1		1-03 *		D12- 3									391
SERIAL OUT 12	H			1										11-1/8	391
SERIAL OUT 13	H	A05K1		1-01 *		D11- 4					1		N	9-5/8	392
SERIAL OUT 13	H	D03N1		1-02 *		D12- 3					2		N	2-7/8	392
SERIAL OUT 13	H	D07R2		1-03 *		D04- 4									392
SERIAL OUT 13	H			1										12-4/8	392
SERIAL OUT 14	H	A05D2		1-01 *		D11- 4					1		N	10-7/8	393
SERIAL OUT 14	H	D03P1		1-02 *		D12- 3					2		N	6-7/8	393
SERIAL OUT 14	H	F07D2		1-03 *		D04- 5									393
SERIAL OUT 14	H			1										17-6/8	393
SERIAL OUT 15	H	A05F2		1-01 *		D11- 4					2		N	5-7/8	394
SERIAL OUT 15	H	C07B1		1-02 *		D04- 5					1		N	6-3/8	394
SERIAL OUT 15	H	D03M1		1-03 *		D12- 3									394
SERIAL OUT 15	H			1										12-2/8	394
SET REQUEST	H	B02V2		1-01 *		D07					1		N	10-7/8	395
SET REQUEST	H	F04N1		1-02 *		D13- 1									395
SET REQUEST	H			1										10-7/8	395
SILO MAINT PULSE	L	F03V2		1-01 *		D12- 3					1		N	2-5/8	396
SILO MAINT PULSE	L	F05F1		1-02 *		D11- 1									396
SILO MAINT PULSE	L			1										2-5/8	396
SSR 00	H	D03H1		1-01 *		D12- 2					1		N	4-7/8	397
SSR 00	H	D09T2		1-02 *		D01- 2									397
SSR 00	H			1										4-7/8	397
SSR 01	H	D0982		1-01 *		D01- 2					1		N	4-7/8	398
SSR 01	H	E03E1		1-02 *		D12- 2									398
SSR 01	H			1										4-7/8	398
SSR 02	H	D09R2		1-01 *		D01- 2					1		N	5-5/8	399
SSR 02	H	E03L1		1-02 *		D12- 2									399
SSR 02	H			1										5-5/8	399

DH11.C RUN NAME	A/P	WRP288.V34(62)-1		31-JUL-75 BAY - ORDER	Q	DRAW OPT	RV RG Y	X	Z	REMARKS	12-JUL-76		16136 NC LENGTH FLAG		PAGE 40 EXCEPTIONS		RUN NUMBER
		PIN NAME	ORDER PIN														
TBMT LINE 00	H	D05H2		1-01 *		D11- 1			1				N	2-5/8			414
TBMT LINE 00	H	E06C1		1-02 *		D03- 2			2				N	1-3/8			414
TBMT LINE 00	H	E04J2		1-03 *		D13- 1								4-0/8			414
TBMT LINE 00	H			1													414
TBMT LINE 01	H	D05J2		1-01 *		D11- 1			2				N	3-7/8			415
TBMT LINE 01	H	E04M2		1-02 *		D13- 1			1				N	4-3/8			415
TBMT LINE 01	H	F06N2		1-03 *		D03- 2								8-2/8			415
TBMT LINE 01	H			1													415
TBMT LINE 02	H	D05F1		1-01 *		D11- 1			1				N	4-3/8			416
TBMT LINE 02	H	E06S1		1-02 *		D03- 3			2				N	1-3/8			416
TBMT LINE 02	H	E04R1		1-03 *		D13- 1								5-6/8			416
TBMT LINE 02	H			1													416
TBMT LINE 03	H	C06P1		1-01 *		D03- 3			2				N	2-7/8			417
TBMT LINE 03	H	D05H1		1-02 *		D11- 1			1				N	4-3/8			417
TBMT LINE 03	H	E04U2		1-03 *		D13- 1								7-2/8			417
TBMT LINE 03	H			1													417
TBMT LINE 04	H	D06C1		1-01 *		D03- 4			2				N	1-2/8			418
TBMT LINE 04	H	D05J1		1-02 *		D11- 1			1				N	6-7/8			418
TBMT LINE 04	H	F04S2		1-03 *		D13- 1								8-1/8			418
TBMT LINE 04	H			1													418
TBMT LINE 05	H	D06P2		1-01 *		D03- 4			2				N	1-3/8			419
TBMT LINE 05	H	D05K1		1-02 *		D11- 1			1				N	6-5/8			419
TBMT LINE 05	H	F04P1		1-03 *		D13- 1								9-0/8			419
TBMT LINE 05	H			1													419
TBMT LINE 06	H	D05M1		1-01 *		D11- 1			1				N	5-1/8			420
TBMT LINE 06	H	F06C1		1-02 *		D03- 5			2				N	1-7/8			420
TBMT LINE 06	H	F04H1		1-03 *		D13- 1								7-0/8			420
TBMT LINE 06	H			1													420
TBMT LINE 07	H	C06D2		1-01 *		D03- 5			2				N	4-7/8			421
TBMT LINE 07	H	D05N1		1-02 *		D11- 1			1				N	4-7/8			421
TBMT LINE 07	H	F04D2		1-03 *		D13- 1								9-6/8			421
TBMT LINE 07	H			1													421
TBMT LINE 08	H	C05M1		1-01 *		D11- 1			1				N	5-5/8			422
TBMT LINE 08	H	E07C1		1-02 *		D04- 2			2				N	2-3/8			422
TBMT LINE 08	H	E04J1		1-03 *		D13- 1								8-0/8			422
TBMT LINE 08	H			1													422
TBMT LINE 09	H	C05L1		1-01 *		D11- 1			1				N	6-1/8			423
TBMT LINE 09	H	E04L1		1-02 *		D13- 1			2				N	5-1/8			423
TBMT LINE 09	H	F07N2		1-03 *		D04- 2								11-2/8			423
TBMT LINE 09	H			1													423
TBMT LINE 10	H	C05K1		1-01 *		D11- 1			1				N	6-3/8			424
TBMT LINE 10	H	E04P2		1-02 *		D13- 1			2				N	1-5/8			424
TBMT LINE 10	H	E07S1		1-03 *		D04- 3								8-0/8			424
TBMT LINE 10	H			1													424

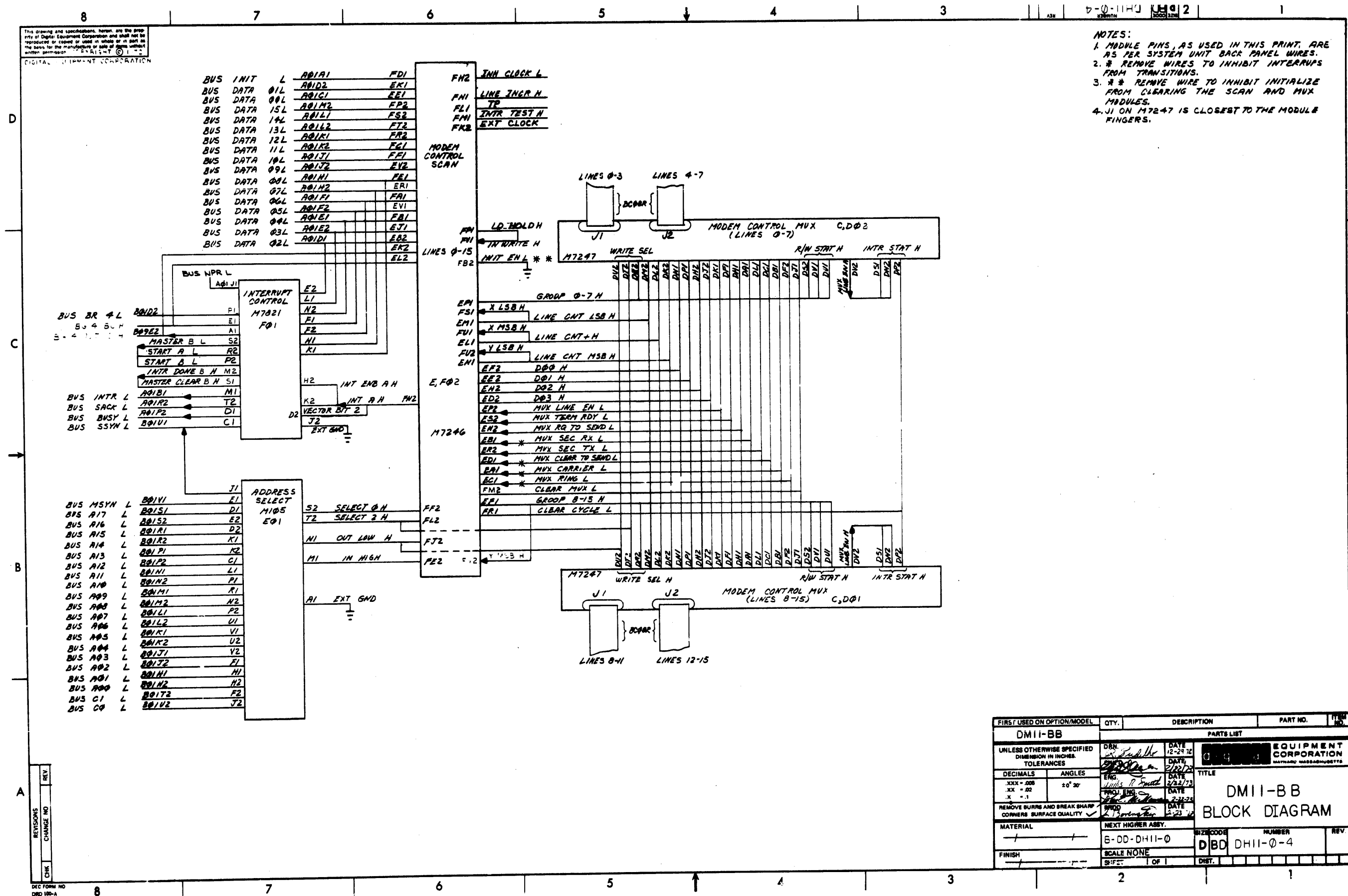
DH11.C RUN NAME	A/P	WRP288.V34(62)-1		31-JUL-75		DRAW	PV	RG	Y	X	Z	REMARKS	12-JUL-76		16136		PAGE 41		RUN NUMBER
		PIN NAME	ORDER PIN	RAY - ORDER	Q								NC	LENGTH	EXCEPTIONS	FLAG			
TBMT LINE 11	H	C07P1		1-P1 *		D04- 3					2		N	1-2/8					425
TBMT LINE 11	H	C05L2		1-P2 *		D11- 1					1		N	6-7/8					425
TBMT LINE 11	H	E04T2		1-P3 *		D13- 1									8-1/8				425
TBMT LINE 11	H			1															425
TBMT LINE 12	H	C05K2		1-P1 *		D11- 1					2		N	3-1/8					426
TBMT LINE 12	H	D07C1		1-P2 *		D04- 4					1		N	7-1/8					426
TBMT LINE 12	H	F04D1		1-P3 *		D13- 1									10-2/8				426
TBMT LINE 12	H			1															426
TBMT LINE 13	H	C05U1		1-P1 *		D11- 1					2		N	3-7/8					427
TBMT LINE 13	H	D07P2		1-P2 *		D04- 4					1		N	6-1/8					427
TBMT LINE 13	H	F04F2		1-P3 *		D13- 1									10-0/8				427
TBMT LINE 13	H			1															427
TBMT LINE 14	H	C05S1		1-P1 *		D11- 1					1		N	7-7/8					428
TBMT LINE 14	H	F07C1		1-P2 *		D04- 5					2		N	2					428
TBMT LINE 14	H	F04V2		1-P3 *		D13- 1									9-7/8				428
TBMT LINE 14	H			1															428
TBMT LINE 15	H	C07D2		1-P1 *		D04- 5					2		N	2-2/8					429
TBMT LINE 15	H	C05R1		1-P2 *		D11- 1					1		N	8-7/8					429
TBMT LINE 15	H	F04R1		1-P3 *		D13- 1									11-1/8				429
TBMT LINE 15	H			1															429
TIME OUT (0)	H	A04K2		1-P1 *		D13- 1					1		N	1-3/8					430
TIME OUT (0)	H	A03S2		1-P2 *		D12- 1					2		N	3-1/8					430
TIME OUT (0)	H	B02K1		1-P3 *		D07					1		N	10-5/8					430
TIME OUT (0)	H	E05R2		1-P4 *		D11- 2									15-1/8				430
TIME OUT (0)	H			1															430
TIME OUT (1)	H	B02L1				D07									1-PIN RUN				431
TP	H	F02L1				D09									1-PIN RUN				432
TP CLR WRITE	H	F04K1				D13- 2									1-PIN RUN				433
TP CONT STROBE INT (1)	H	E04H2				D13- 1									1-PIN RUN				434
TP EC DLY	H	F04L1				D13- 2									1-PIN RUN				435
TP EC PLS	H	F04L2				D13- 2									1-PIN RUN				436
TP EC+ES SSYN INHIBIT	H	F04F1				D13- 1									1-PIN RUN				437
TP MASTER CL SSYN		F04C1				D13- 1									1-PIN RUN				438
TP NBR COMP	L	F04K2				D13- 2									1-PIN RUN				439
TP SCR 00 CLEAR	H	F05K1				D11- 2									1-PIN RUN				440
TP SCR 00 LOAD	H	C05H1				D11- 2									1-PIN RUN				441
TP SCR HIGH BYTE LOAD	H	E05P2				D11- 2									1-PIN RUN				442

DN11.C RUN NAME	A/P	WRP288.V34(62)-1 PIN NAME	31-Jul-75 ORDER PIN	BAY - ORDER	Q	DRAW OPT	RV RG Y	X	Z	REMARKS	16136 NC LENGTH EXCEPTIONS FLAG	PAGE 42 RUN NUMBER
TP SET UP DLY	H	F04A1				D13- 2					1-PIN RUN	443
TP WRITE	L	F04J2				D13- 2					1-PIN RUN	444
TRAN DATA 01	H	C07N2		1-01 *		D04- 4			2		N 1	445
TRAN DATA 01	H	C06N2		1-02 *		D03- 4			1		N 4-1/8	445
TRAN DATA 01	H	D04M2		1-03 *		D13- 1					5-1/8	445
TRAN DATA 01	H			1								445
TRAN DATA 02	H	C07M1		1-01 *		D04- 4			2		N 1	446
TRAN DATA 02	H	C06M1		1-02 *		D03- 4			1		N 3-1/8	446
TRAN DATA 02	H	D04F2		1-03 *		D13- 1					4-1/8	446
TRAN DATA 02	H			1								446
TRAN DATA 03	H	C06L2		1-01 *		D03- 4			2		N 1	447
TRAN DATA 03	H	C07L2		1-02 *		D04- 4			1		N 3-4/8	447
TRAN DATA 03	H	D04E2		1-03 *		D13- 1					4-4/8	447
TRAN DATA 03	H			1								447
TRAN DATA 04	H	C07L1		1-01 *		D04- 4			2		N 1	448
TRAN DATA 04	H	C06L1		1-02 *		D03- 4			1		N 3-5/8	448
TRAN DATA 04	H	D04F1		1-03 *		D13- 1					4-5/8	448
TRAN DATA 04	H			1								448
TRAN DATA 05	H	C07H1		1-01 *		D04- 4			2		N 1	449
TRAN DATA 05	H	C06H1		1-02 *		D03- 4			1		N 3-5/8	449
TRAN DATA 05	H	D04D1		1-03 *		D13- 1					4-5/8	449
TRAN DATA 05	H			1								449
TRAN DATA 06	H	C04J2		1-01 *		D13- 1			1		N 1-5/8	450
TRAN DATA 06	H	C06M2		1-02 *		D03- 4			2		N 1	450
TRAN DATA 06	H	C07M2		1-03 *		D04- 4					2-5/8	450
TRAN DATA 06	H			1								450
TRAN DATA 07	H	C04J1		1-01 *		D13- 1			1		N 1-3/8	451
TRAN DATA 07	H	C06K1		1-02 *		D03- 4			2		N 1	451
TRAN DATA 07	H	C07K1		1-03 *		D04- 4					2-3/8	451
TRAN DATA 07	H			1								451
TRAN DATA 08	H	C04K2		1-01 *		D13- 1			1		N 1-4/8	452
TRAN DATA 08	H	C06K2		1-02 *		D03- 4			2		N 1	452
TRAN DATA 08	H	C07K2		1-03 *		D04- 4					2-4/8	452
TRAN DATA 08	H			1								452
TRAN SCAN CLK	H	E05M2		1-01 *		D11- 1			1		N 4-5/8	453
TRAN SCAN CLK	H	F04V1		1-02 *		D13- 1					4-5/8	453
TRAN SCAN CLK	H			1								453
TRAN STROBE	H	C03J2		1-01 *		D12- 1			1		N 4-5/8	454
TRAN STROBE	H	D07J2		1-02 *		D04- 5			2		N 1	454
TRAN STROBE	H	D06J2		1-03 *		D03- 5					5-5/8	454
TRAN STROBE	H			1								454

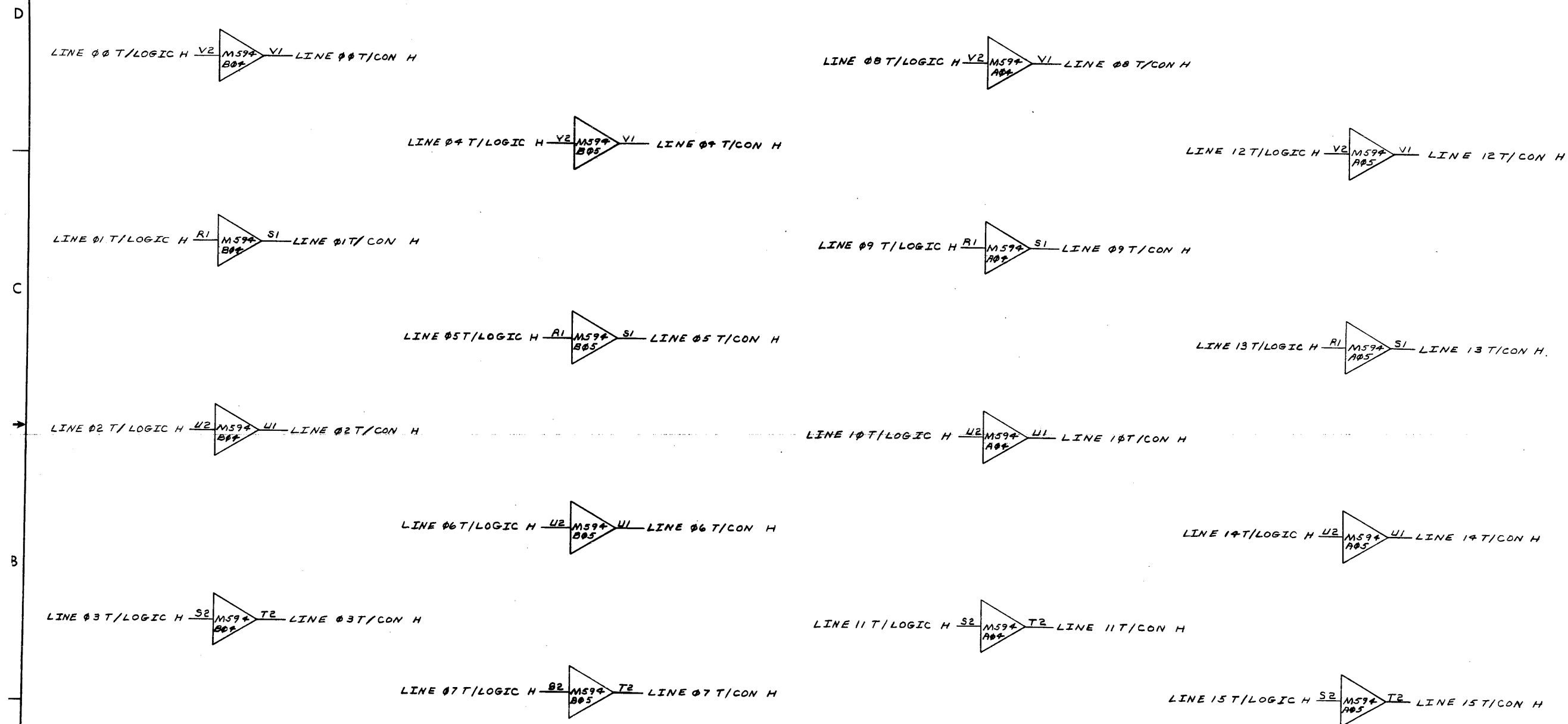
[illegible]

DH11.C		WRP288.V34(62)-1 31-Jul-75										12-Jul-76		16:36 PAGE 44		RUN	
RUN	NAME	A/P	PIN NAME	ORDER PIN	BAY - ORDER	Q	DRAW OPT	RV	RG	Y	X	Z	REMARKS	NC FLAG	LENGTH	EXCEPTIONS	NUMBER
TTL DATA IN 00		L	B07C2		1-01 *		D02					1		N	4-1/8		468
TTL DATA IN 00		L	C05D1		1-02 *		D11- 4										468
TTL DATA IN 00		L			1										4-1/8		468
TTL DATA IN 09		L	B07E2		1-01 *		D02					1		N	3-7/8		469
TTL DATA IN 09		L	C05C1		1-02 *		D11- 4										469
TTL DATA IN 09		L			1										3-7/8		469
TTL DATA IN 10		L	B05M2		1-01 *		D11- 4					1		N	1-7/8		470
TTL DATA IN 10		L	B07H2		1-02 *		D02										470
TTL DATA IN 10		L			1										1-7/8		470
TTL DATA IN 11		L	B05L2		1-01 *		D11- 4					1		N	1-3/8		471
TTL DATA IN 11		L	B07K2		1-02 *		D02										471
TTL DATA IN 11		L			1										1-3/8		471
TTL DATA IN 12		L	A05P1		1-01 *		D11- 4					1		N	4-1/8		472
TTL DATA IN 12		L	B07M2		1-02 *		D02										472
TTL DATA IN 12		L			1										4-1/8		472
TTL DATA IN 13		L	A05N1		1-01 *		D11- 4					1		N	4-3/8		473
TTL DATA IN 13		L	B07P2		1-02 *		D02										473
TTL DATA IN 13		L			1										4-3/8		473
TTL DATA IN 14		L	A05D1		1-01 *		D11- 4					1		N	5-5/8		474
TTL DATA IN 14		L	B07S2		1-02 *		D02										474
TTL DATA IN 14		L			1										5-5/8		474
TTL DATA IN 15		L	A05A1		1-01 *		D11- 4					1		N	6-3/8		475
TTL DATA IN 15		L	B07U2		1-02 *		D02										475
TTL DATA IN 15		L			1										6-3/8		475
TTL DATA OUT 00		L	B07D1		1-01 *		D02					1		N	13-7/8		476
TTL DATA OUT 00		L	F03P2		1-02 *		D12- 2										476
TTL DATA OUT 00		L			1										13-7/8		476
TTL DATA OUT 01		L	B07F1		1-01 *		D02					1		N	13-3/8		477
TTL DATA OUT 01		L	F03M2		1-02 *		D12- 2										477
TTL DATA OUT 01		L			1										13-3/8		477
TTL DATA OUT 02		L	B07J1		1-01 *		D02					1		N	13-5/8		478
TTL DATA OUT 02		L	F03S2		1-02 *		D12- 2										478
TTL DATA OUT 02		L			1										13-5/8		478
TTL DATA OUT 03		L	B07L1		1-01 *		D02					1		N	13-5/8		479
TTL DATA OUT 03		L	F03U2		1-02 *		D12- 2										479
TTL DATA OUT 03		L			1										13-5/8		479
TTL DATA OUT 04		L	B07N1		1-01 *		D02					1		N	12-3/8		480
TTL DATA OUT 04		L	F03K2		1-02 *		D12- 2										480
TTL DATA OUT 04		L			1										12-3/8		480
TTL DATA OUT 05		L	B07R1		1-01 *		D02					1		N	12-1/8		481
TTL DATA OUT 05		L	F03J1		1-02 *		D12- 2										481
TTL DATA OUT 05		L			1										12-1/8		481

DH11.C		WRP288.V34(62)-1 31-Jul-75										12-Jul-76		16136		PAGE 45		RUN NUMBER
RUN NAME		A/P	PIN NAME	ORDER PIN	BAY - ORDER	Q	DRAW OPT	RV	RG	Y	X	Z	REMARKS	NC FLAG	LENGTH	EXCEPTIONS		
TTL DATA OUT 06	L	B07T1		1-01 *	D02							1		N	12-5/8		482	
TTL DATA OUT 06	L	F03P1		1-02 *	D12- 2												482	
TTL DATA OUT 06	L			1											12-5/8		482	
TTL DATA OUT 07	L	B07V1		1-01 *	D02							1		N	11-3/8		483	
TTL DATA OUT 07	L	F03F1		1-02 *	D12- 2												483	
TTL DATA OUT 07	L			1											11-3/8		483	
TTL DATA OUT 08	L	B07D2		1-01 *	D02							1		N	9-3/8		484	
TTL DATA OUT 08	L	D03S1		1-02 *	D12- 3												484	
TTL DATA OUT 08	L			1											9-3/8		484	
TTL DATA OUT 09	L	B07F2		1-01 *	D02							1		N	8-5/8		485	
TTL DATA OUT 09	L	U03P2		1-02 *	D12- 3												485	
TTL DATA OUT 09	L			1											8-5/8		485	
TTL DATA OUT 10	L	B07J2		1-01 *	D02							1		N	7-1/8		486	
TTL DATA OUT 10	L	D03A1		1-02 *	D12- 3												486	
TTL DATA OUT 10	L			1											7-1/8		486	
TTL DATA OUT 11	L	B07L2		1-01 *	D02							1		N	7-1/8		487	
TTL DATA OUT 11	L	D03C1		1-02 *	D12- 3												487	
TTL DATA OUT 11	L			1											7-1/8		487	
TTL DATA OUT 12	L	B07N2		1-01 *	D02							1		N	7-3/8		488	
TTL DATA OUT 12	L	D03L2		1-02 *	D12- 3												488	
TTL DATA OUT 12	L			1											7-3/8		488	
TTL DATA OUT 13	L	B07R2		1-01 *	D02							1		N	7-3/8		489	
TTL DATA OUT 13	L	D03M2		1-02 *	D12- 3												489	
TTL DATA OUT 13	L			1											7-3/8		489	
TTL DATA OUT 14	L	B07T2		1-01 *	D02							1		N	7-1/8		490	
TTL DATA OUT 14	L	D03N2		1-02 *	D12- 3												490	
TTL DATA OUT 14	L			1											7-1/8		490	
TTL DATA OUT 15	L	B07V2		1-01 *	D02							1		N	6-7/8		491	
TTL DATA OUT 15	L	D03L1		1-02 *	D12- 3												491	
TTL DATA OUT 15	L			1											6-7/8		491	
TX CLOCK LINE 00	L	E06K1		1-01 *	D03- 2							1		N	2-1/8		492	
TX CLOCK LINE 00	L	E08U2		1-02 *	D05- 1												492	
TX CLOCK LINE 00	L			1											2-1/8		492	
TX CLOCK LINE 01	L	E08R2		1-01 *	D05- 1							1		N	4-5/8		493	
TX CLOCK LINE 01	L	F06U2		1-02 *	D03- 2												493	
TX CLOCK LINE 01	L			1											4-5/8		493	
TX CLOCK LINE 02	L	E06V1		1-01 *	D03- 3							1		N	2-1/8		494	
TX CLOCK LINE 02	L	E08L2		1-02 *	D05- 1												494	
TX CLOCK LINE 02	L			1											2-1/8		494	
TX CLOCK LINE 03	L	C06U1		1-01 *	D03- 3							1		N	5-5/8		495	
TX CLOCK LINE 03	L	E08F2		1-02 *	D05- 1												495	
TX CLOCK LINE 03	L			1											5-5/8		495	



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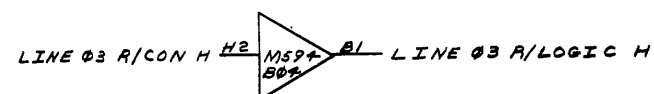
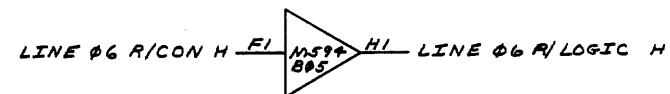
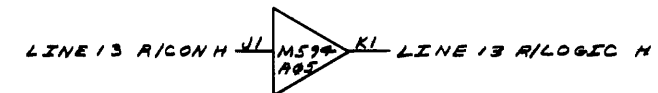
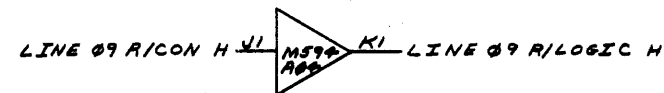
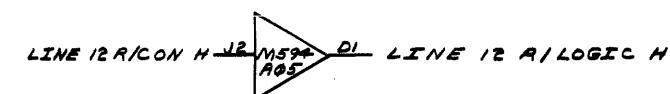
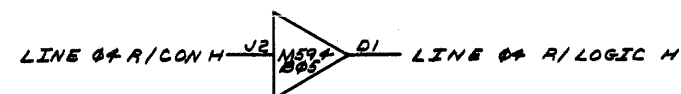
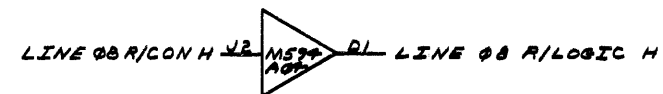


REV
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DEC FORM NO 8

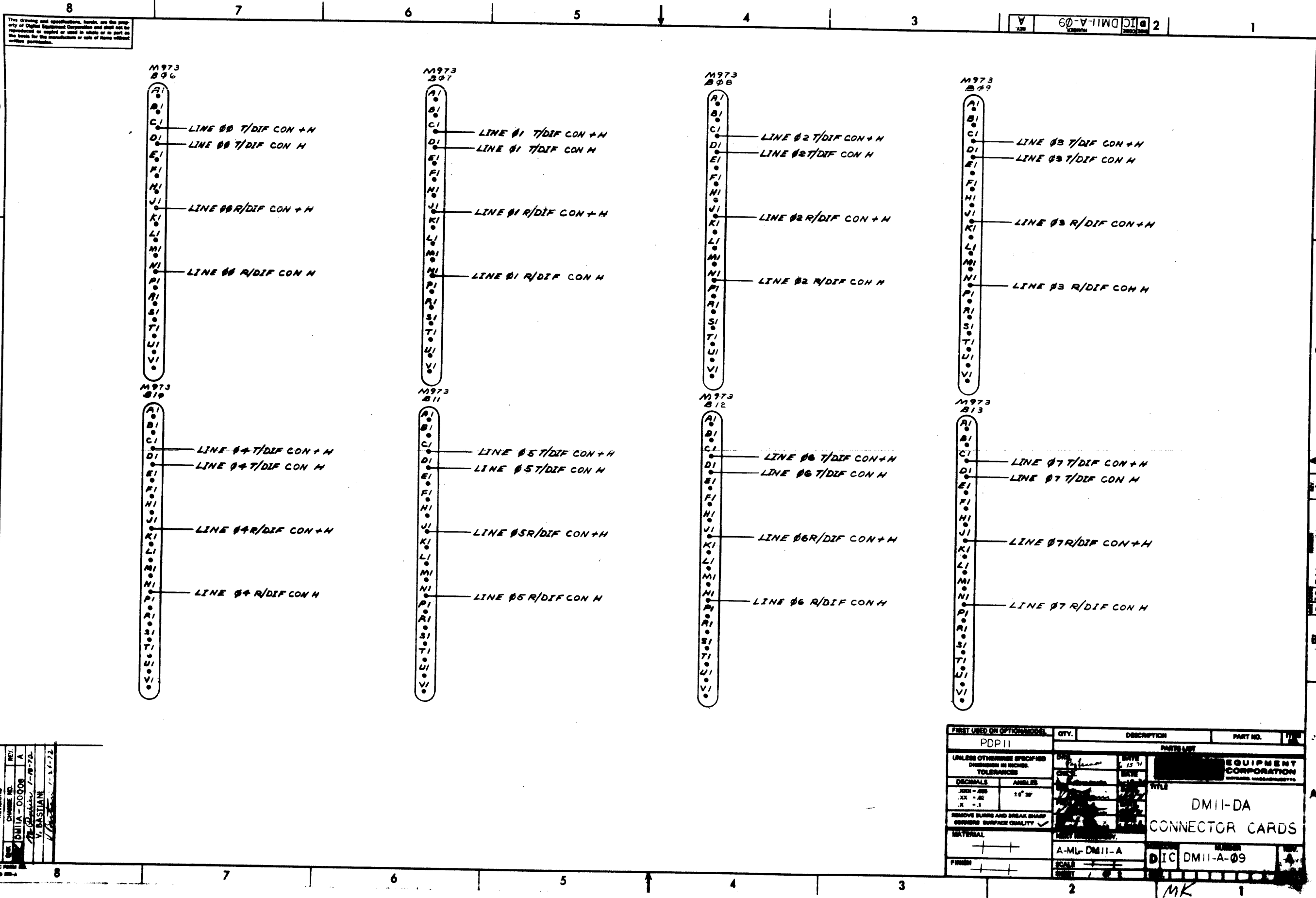
FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
PDP 11				
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES	DRN. P. J. K.	DATE 6-3-71	EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS	
DECIMALS	CHK'D.	DATE 6-5-71	TITLE	
ANGLES	ENG. A. F. R.	DATE 6-5-71	DMII-DB	
XXX + .005	PROL. ENG.	DATE 6-5-71	TRANSMIT & RECEIVE	
XX + .02	PROD. ENG.	DATE 6-5-71		
X + .1	PROD. ENG.	DATE 6-5-71		
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY	MATERIAL	NEXT HIGHER ASSY.	SIZE CODE	NUMBER
	FINISH	A-ML-DMII-A	DBS	DMII-A-08
		SCALE		REV.
		SHEET	OF 2	
		DIST.		

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FIRST USED ON OPTION/MODEL		QTY.	DESCRIPTION	PART NO.	FIG.
PDP 11		PARTS LIST			
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES		DRN. <i>Ray Lamm</i>	DATE <i>6-3-71</i>	 EQUIPMENT CORPORATION MAYFARL, MASSACHUSETTS	
DECIMALS	ANGLES	CHK'D. <i>A. E. Raymond</i>	DATE <i>6-3-71</i>	TITLE DM11-DR TRANSMIT & RECEIVE	
.XXX = .008	± 0° 30'	ENG. <i>J. Harrison</i>	DATE <i>6/16/71</i>		
.XX = .02		PROL ENG. <i>J. Harrison</i>	DATE <i>6/22/71</i>		
.X = .1		PROD. <i>Bob Harris</i>	DATE <i>6/22/71</i>		
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓		NEXT HIGHER ASSY.			
MATERIAL ++		A-ML-DM11-A		INZ CODE NUMBER DBS DM11-A-08	
FINISH ++		SCALE SHEET 2 of 2		DIST.	

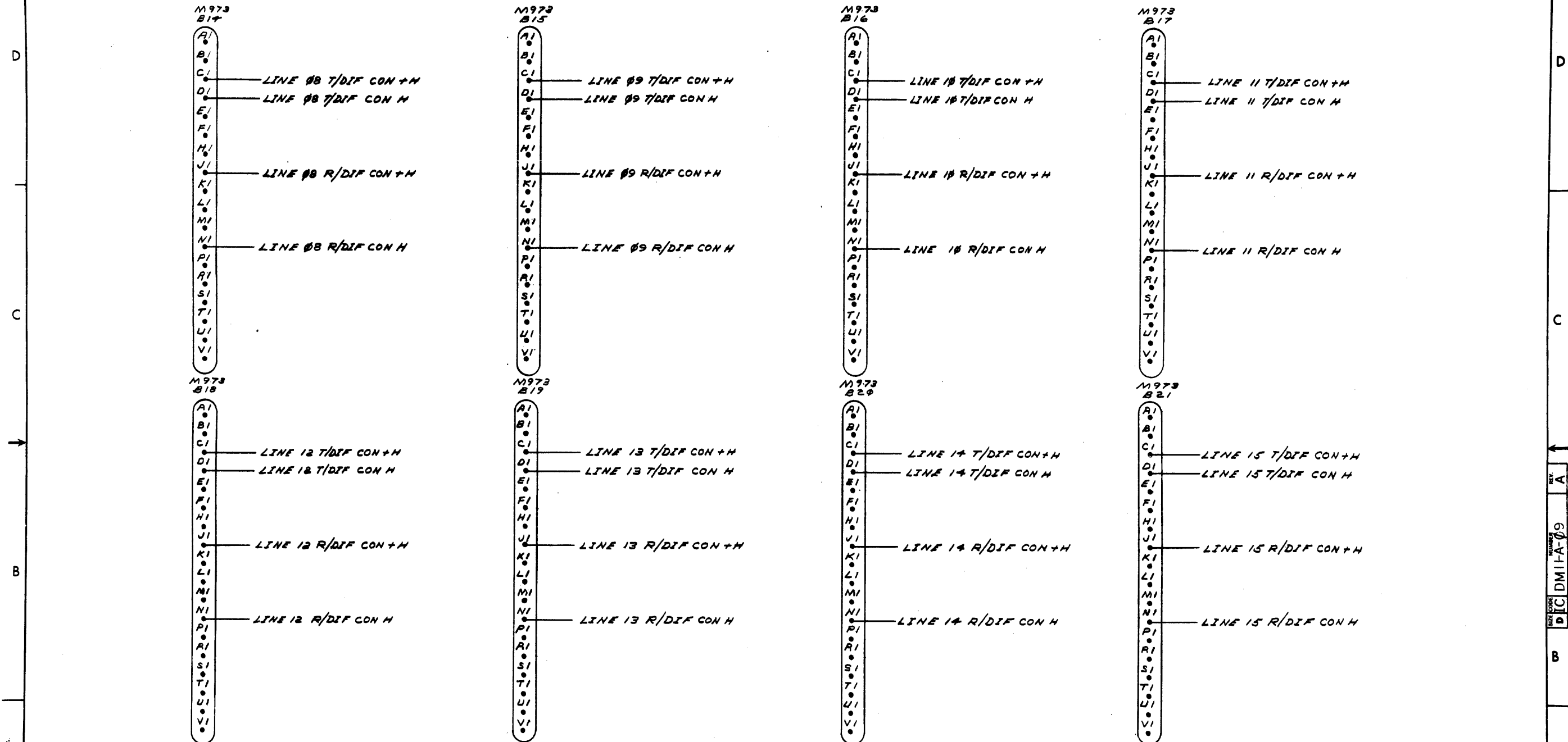
DEC FORM NO
DRD 100-4



REVISIONS	CHANGE NO.	REV.	DATE
1	1	A	1-10-72
2	2	B	1-11-72
3	3	C	1-12-72

FIRST USED ON OPTIONAL	QTY.	DESCRIPTION	PART NO.
PDP11			
UNLESS OTHERWISE SPECIFIED DIMENSIONS IN INCHES TOLERANCES	DATE	DATE	DATE
DECIMALS	ANGLES	TITLE	
.XXX - .000	10° 30'	DMII-DA CONNECTOR CARDS	
.XX - .01		EQUIPMENT CORPORATION	
.X - .1		REMOVED BURRS AND BREAK SHARP EDGES SURFACE QUALITY	
MATERIAL	DATE	DATE	
FINISH	DATE	DATE	
		A-MU-DMII-A	
		DMII-A-09	

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FIRST USED ON OPTION/MODEL		QTY.	DESCRIPTION	PART NO.	ITEM NO.
PDP11					
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES		DRN. <i>Pay</i>	DATE <i>6-15-71</i>	PARTS LIST	
		CHK'D. <i>D. Raymond</i>	DATE <i>6-18-71</i>	digital EQUIPMENT CORPORATION MAYFIELD, MASSACHUSETTS	
DECIMALS	ANGLES	ENG. <i>W. B. Smith</i>	DATE <i>6/17/71</i>	TITLE	
.XXX = .008	±0° 30'	PROJ. ENG. <i>W. B. Smith</i>	DATE <i>6/17/71</i>	DM11-DA	
.XX = .02		PROD. <i>W. B. Smith</i>	DATE <i>6/17/71</i>	CONNECTOR CARDS	
.X = .1					
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY		NEXT HIGHER ASSY.		SIZE CODE	NUMBER
		A-ML-DM11-A		DIC	DM11-A-09
MATERIAL		SCALE		REV.	
FINISH		SHEET 2 OF 2			

DRWG NO	REV LTR
K-WL-DMII-A-5	E

REVISIONS			
REV LTR	ECO NO	DATE	ENG
A	DMIIA-9-3-71	9-3-71	VJ
B	DMIIA-2-24-72	2-24-72	VJ
C	DMIIA-3-1-74	3-1-74	VJ
D	DMIIA-8-73	8-73	VJ
E	DMIIA-9-1-74	9-1-74	VJ

DRAWN <i>Cl. Hinds</i>	DATE 5/25/71	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS	TITLE WIRE LIST DISTRIBUTION PNL	
CHECKED <i>J. Hinds</i>	DATE 6-1-71		FOR TAPE # FILE #	
ENG <i>V. Portier</i>	DATE 6/1/71		SIZE CODE DWG NO	
PROJ ENG <i>V. Portier</i>	DATE 6/1/71		REV LTR	
PROD <i>Paul Hinds</i>	DATE 6/3/71	ASSY NO D-AD-7008443-0-0	K WL DMII-A-5	E
SCALE — # —		SHEET 1 OF 1		DIST.

MM11DP.E (RUN NAME)	HND28A.V23(23) 05/24/74	A/P	PIN NAME	ORDER PIN	BAY - ORDER	Q	DRAW	RV	P.G.	Y	X	Z	REMARKS	24-SEP-74 LENGTH	0152 EXCEPTIONS	PAGE 3 RIN NUMBER
01DTR/LOGIC			A01N1		1-01 *							1				21
01DTR/LOGIC			A07P2		1-02 *											21
01DTR/LOGIC					1									5-4/8		21
01REQ TO SEND/CON			A07T2		1-01 *							2				22
01REQ TO SEND/CON			B07L2		1-02 *									4-2/8		22
01REQ TO SEND/CON					1											22
01REQ TO SEND/LOGIC			A01M1		1-01 *							1				23
01REQ TO SEND/LOGIC			A07S2		1-02 *											23
01REQ TO SEND/LOGIC					1									5-6/8		23
01RING/CON			A07K2		1-01 *							1				24
01RING/CON			B07M2		1-02 *											24
01RING/CON					1									5-2/8		24
01RING/LOGIC			A01M1		1-01 *							1				25
01RING/LOGIC			A07C1		1-02 *											25
01RING/LOGIC					1									5-6/8		25
01SEC RX/LOGIC			A01V1		1-01 *							1				26
01SEC RX/LOGIC			A07E1		1-02 *											26
01SEC RX/LOGIC					1									6-0/8		26
01SEC TX/LOGIC			A01U1		1-01 *							1				27
01SEC TX/LOGIC			A07U2		1-02 *											27
01SEC TX/LOGIC					1									5-4/8		27
01SUP REC/CON			A07L2		1-01 *							1				28
01SUP REC/CON			B07F1		1-02 *											28
01SUP REC/CON					1									4-6/8		28
01SUP TRAN/CON			A07U1		1-01 *							1				29
01SUP TRAN/CON			B07E1		1-02 *											29
01SUP TRAN/CON					1									3-4/8		29
02CARRIER/CON			A08H2		1-01 *							1				30
02CARRIER/CON			B08P2		1-02 *											30
02CARRIER/CON					1									5-6/8		30
02CARRIER/LOGIC			A01J2		1-01 *							1				31
02CARRIER/LOGIC			A08B1		1-02 *											31
02CARRIER/LOGIC					1									6-0/8		31
02CLEAR TO SEND/CON			A08M2		1-01 *							1				32
02CLEAR TO SEND/CON			B08K2		1-02 *											

DM11DP.E	HND288.V23(23)	05/24/74										24-SEP-74	0152	PAGE 4	
RUN NAME	A/P	PIN NAME	ORDER PIN	BAY - ORDER	Q	DRAW	RV	PG	Y	X	Z	REMARKS	LENGTH	EXCEPTIONS	RUN NUMBER
02CLEAR TO SEND/LOGIC		A01H2		1-01 *							1				33
02CLEAR TO SEND/LOGIC		A08F2		1-02 *											33
02CLEAR TO SEND/LOGIC				1									b-u/a		33
02DTR/CON		A08R2		1-01 *							1				34
02DTR/CON		B08R2		1-02 *											34
02DTR/CON				1									5-0/a		34
02DTR/LOGIC		A01E2		1-01 *							1				35
02DTR/LOGIC		A08P2		1-02 *											35
02DTR/LOGIC				1									b-e/a		35
02REQ TO SEND/CON		A08T2		1-01 *							2				36
02REQ TO SEND/CON		B08L2		1-02 *											36
02REQ TO SEND/CON				1									4-e/a		36
02REQ TO SEND/LOGIC		A01F2		1-01 *							1				37
02REQ TO SEND/LOGIC		A0AS2		1-02 *											37
02REQ TO SEND/LOGIC				1									b-e/a		37
02RING/CON		A08K2		1-01 *							1				38
02RING/CON		B08M2		1-02 *											38
02RING/CON				1									5-e/a		38
02RING/LOGIC		A01D2		1-01 *							1				39
02RING/LOGIC		A08C1		1-02 *											39
02RING/LOGIC				1									5-4/a		39
02SEC RX LOGIC		A01L2		1-01 *							1				40
02SEC RX LOGIC		A0AE1		1-02 *											40
02SEC RX LOGIC				1									5-b/a		40
02SEC TX LOGIC		A01K2		1-01 *							1				41
02SEC TX LOGIC		A08U2		1-02 *											41
02SEC TX LOGIC				1									b-e/a		41
02SUP REC/CON		A0AL2		1-01 *							1				42
02SUP REC/CON		B08F1		1-02 *											42
02SUP REC/CON				1									4-b/a		42
02SUP TRAN/CON		A08U1		1-01 *							1				43
02SUP TRAN/CON		B08E1		1-02 *											43
02SUP TRAN/CON				1									3-4/a		43
03CARRIER/CON		A04H2		1-01 *							1				44
03CARRIER/CON		B09P2		1-02 *											44
03CARRIER/CON				1									5-b/a		44

DM11DP.E RUN NAME	HND288.V23(23) A/P PIN NAME	05/24/74 ORDER PIN	HAY - ORDER	0	DRAW	RV	PG	Y	X	Z	REMARKS	24-SEP-74 LENGTH	0152 EXCEPTIONS	PAGE 5 RUN NUMBER
03CARRIER/LOGIC	A01S2		1-01 *							1				45
03CARRIER/LOGIC	A04B1		1-02 *											45
03CARRIER/LOGIC			1									7-0/8		45
03CLEAR TO SEND/CON	A04M2		1-01 *							1				46
03CLEAR TO SEND/CON	B04K2		1-02 *											46
03CLEAR TO SEND/CON			1									4-6/8		46
03CLEAR TO SEND/LOGIC	A01K2		1-01 *							1				47
03CLEAR TO SEND/LOGIC	A04F2		1-02 *											47
03CLEAR TO SEND/LOGIC			1									6-6/8		47
03DTR/CON	A09R2		1-01 *							1				48
03DTR/CON	B09R2		1-02 *											48
03DTR/CON			1									5-0/8		48
03DTR/LOGIC	A01N2		1-01 *							1				49
03DTR/LOGIC	A09P2		1-02 *											49
03DTR/LOGIC			1									6-2/8		49
03REQ TO SEND/CON	A04T2		1-01 *							2				50
03REQ TO SEND/CON	B09L2		1-02 *											50
03REQ TO SEND/CON			1									4-2/8		50
03REQ TO SEND/LOGIC	A01P2		1-01 *							1				51
03REQ TO SEND/LOGIC	A09S2		1-02 *											51
03REQ TO SEND/LOGIC			1									6-4/8		51
03RING/CON	A04K2		1-01 *							1				52
03RING/CON	B09M2		1-02 *											52
03RING/CON			1									5-2/8		52
03RING/LOGIC	A01M2		1-01 *							1				53
03RING/LOGIC	A04C1		1-02 *											53
03RING/LOGIC			1									6-4/8		53
03SEC RX/LOGIC	A01V2		1-01 *							1				54
03SEC RX/LOGIC	A09E1		1-02 *											54
03SEC RX/LOGIC			1									6-6/8		54
03SEC TX/LOGIC	A01U2		1-01 *							1				55
03SEC TX/LOGIC	A09U2		1-02 *											55
03SEC TX/LOGIC			1									6-2/8		55
03SUP REC/CON	A09L2		1-01 *							1				56
03SUP REC/CON	B09F1		1-02 *											56
03SUP REC/CON			1									4-6/8		56

DM11DP.E RUN NAME	HND288.V23(23) 05/24/74 A/P PIN NAME	ORDER PIN	BAY - ORDER	Q	DRAW	RV	PG	Y	X	Z	REMARKS	24-SEP-74 LENGTH	0152 EXCEPTIONS	PAGE 6 RUN NUMBER
03SUP TRAN/CON	A0901		1-01 *							1				57
03SUP TRAN/CON	804E1		1-02 *											57
03SUP TRAN/CON			1									3-4/8		57
04CARRIER/CON	A10H2		1-01 *							1				58
04CARRIER/CON	B10P2		1-02 *											58
04CARRIER/CON			1									5-6/8		58
04CARRIER/LOGIC	A02J1		1-01 *							1				59
04CARRIER/LOGIC	A10B1		1-02 *											59
04CARRIER/LOGIC			1									6-6/8		59
04CLEAR TO SEND/CON	A10M2		1-01 *							1				60
04CLEAR TO SEND/CON	B10K2		1-02 *											60
04CLEAR TO SEND/CON			1									4-6/8		60
04CLEAR TO SEND/LOGIC	A02H1		1-01 *							1				61
04CLEAR TO SEND/LOGIC	A10F2		1-02 *											61
04CLEAR TO SEND/LOGIC			1									6-6/8		61
04DTR/CON	A10R2		1-01 *							1				62
04DTR/CON	B10R2		1-02 *											62
04DTR/CON			1									5-0/8		62
04DTR/LOGIC	A02E1		1-01 *							1				63
04DTR/LOGIC	A10P2		1-02 *											63
04DTR/LOGIC			1									7-0/8		63
04REQ TO SEND/CON	A10T2		1-01 *							2				64
04REQ TO SEND/CON	B10L2		1-02 *											64
04REQ TO SEND/CON			1									4-2/8		64
04REQ TO SEND/LOGIC	A02F1		1-01 *							1				65
04REQ TO SEND/LOGIC	A10S2		1-02 *											65
04REQ TO SEND/LOGIC			1									7-0/8		65
04RING/CON	A10K2		1-01 *							1				66
04RING/CON	B10M2		1-02 *											66
04RING/CON			1									5-2/8		66
04RING/LOGIC	A02D1		1-01 *							1				67
04RING/LOGIC	A10C1		1-02 *											67
04RING/LOGIC			1									6-2/8		67
04SEC RX/LOGIC	A02L1		1-01 *							1				68
04SEC RX/LOGIC	A10E1		1-02 *											68
04SEC RX/LOGIC			1									6-4/8		68

DM11DP.1 RUN NAME	HND28A.V23(P3) A/P PIN ORDER NAME PIN	05/24/74 HAY - ORDER	Q	DRAW	RV	PG	Y	X	Z	REMARKS	P4-SFP-74 LENGTH	0152 EXCEPTIONS	PAGE 4 RUN NUMBER
06REQ TO SEND/LOGIC	A02F2	1-01 *							1				93
06REQ TO SEND/LOGIC	A12S2	1-02 *											93
06REQ TO SEND/LOGIC		1									7-6/8		93
06RING/CON	A12K2	1-01 *							1				94
06RING/CON	B12M2	1-02 *											94
06RING/CON		1									5-2/8		94
06RING/LOGIC	A02D2	1-01 *							1				95
06RING/LOGIC	A12C1	1-02 *											95
06RING/LOGIC		1									7-0/8		95
06SEC RX/LOGIC	A02L2	1-01 *							1				96
06SEC RX/LOGIC	A12E1	1-02 *											96
06SEC RX/LOGIC		1									7-2/8		96
06SEC TX/LOGIC	A02K2	1-01 *							1				97
06SEC TX/LOGIC	A12U2	1-02 *											97
06SEC TX/LOGIC		1									7-6/8		97
06SUP REC/CON	A12L2	1-01 *							1				98
06SUP REC/CON	B12F1	1-02 *											98
06SUP REC/CON		1									4-6/8		98
06SUP TRAN/CON	A12U1	1-01 *							1				99
06SUP TRAN/CON	B12E1	1-02 *											99
06SUP TRAN/CON		1									3-4/8		99
07CARRIER/CON	A13H2	1-01 *							1				100
07CARRIER/CON	B13P2	1-02 *											100
07CARRIER/CON		1									5-6/8		100
07CARRIER/LOGIC	A02S2	1-01 *							1				101
07CARRIER/LOGIC	A13B1	1-02 *											101
07CARRIER/LOGIC		1									8-4/8		101
07CLEAR TO SEND/CON	A13M2	1-01 *							1				102
07CLEAR TO SEND/CON	B13K2	1-02 *											102
07CLEAR TO SEND/CON		1									4-6/8		102
07CLEAR TO SEND/LOGIC	A02R2	1-01 *							1				103
07CLEAR TO SEND/LOGIC	A13F2	1-02 *											103
07CLEAR TO SEND/LOGIC		1									8-2/8		103
07DTR/CON	A13R2	1-01 *							1				104
07DTR/CON	B13K2	1-02 *											104
07DTR/CON		1									5-0/8		104

DM11DP.1 RUN NAME	HND288.V23(23) 05/24/74 A/P PIN ORDER BAY - NAME PIN ORDER	Q DRAW RV PG Y X Z	REMARKS	24-SEP-74 LENGTH	U152 EXCEPTIONS	PAGE 10 RUN NUMBER
07DTR/LOGIC	A02N2	1-01 *				105
07DTR/LOGIC	A13P2	1-02 *				105
07DTR/LOGIC		L			7-6/8	105
07REQ TO SEND/CON	A13TP	1-01 *				106
07REQ TO SEND/CON	B13LP	1-02 *				106
07REQ TO SEND/CON		L			4-2/8	106
07REQ TO SEND/LOGIC	A02P2	1-01 *				107
07REQ TO SEND/LOGIC	A13S2	1-02 *				107
07REQ TO SEND/LOGIC		L			8-0/8	107
07RING/CON	A13K2	1-01 *				108
07RING/CON	B13M2	1-02 *				108
07RING/CON		L			5-2/8	108
07RING/LOGIC	A02M2	1-01 *				109
07RING/LOGIC	A13CL	1-02 *				109
07RING/LOGIC		L			8-0/8	109
07SEC RX/LOGIC	A02V2	1-01 *				110
07SEC RX/LOGIC	A13EL	1-02 *				110
07SEC RX/LOGIC		L			8-2/8	110
07SEC TX/LOGIC	A02U2	1-01 *				111
07SEC TX/LOGIC	A13UP	1-02 *				111
07SEC TX/LOGIC		L			7-6/8	111
07SUP REC/CON	A13LP	1-01 *				112
07SUP REC/CON	B13PL	1-02 *				112
07SUP REC/CON		L			4-6/8	112
07SUP TRAN/CON	A13UL	1-01 *				113
07SUP TRAN/CON	B13EL	1-02 *				113
07SUP TRAN/CON		L			3-4/8	113
08CARRIER/CON	A14M2	1-01 *				114
08CARRIER/CON	B14P2	1-02 *				114
08CARRIER/CON		L			5-6/8	114
08CARRIER/LOGIC	A03JL	1-01 *				115
08CARRIER/LOGIC	A14BL	1-02 *				115
08CARRIER/LOGIC		L			8-2/8	115
08CLEAR TO SEND/CON	A14M2	1-01 *				116
08CLEAR TO SEND/CON	B14KP	1-02 *				116
08CLEAR TO SEND/CON		L			4-6/8	116

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DM11DP.E RUN NAME	HND288.V23(23) A/P PIN NAME	05/24/74 ORDER PIN	BAY - ORDER	Q	DRAW	KV	PG	Y	X	Z	REMARKS	24-SEP-74 LENGTH	0152 EXCEPTIONS	PAGE 12 RUN NUMBER
09CARRIER/LOGIC	A03S1		1-01 *							1				129
09CARRIER/LOGIC	A15B1		1-02 *											129
09CARRIER/LOGIC			1									9-2/8		129
09CLEAR TO SEND/CON	A15M2		1-01 *							1				130
09CLEAR TO SFND/CON	B15K2		1-02 *											130
09CLEAR TO SEND/CON			1									4-6/8		130
09CLEAR TO SEND/LOGIC	A03R1		1-01 *							1				131
09CLEAR TO SFND/LOGIC	A15F2		1-02 *											131
09CLEAR TO SEND/LOGIC			1									9-0/8		131
09DTR/CON	A15K2		1-01 *							1				132
09DTR/CON	B15K2		1-02 *											132
09DTR/CON			1									5-0/8		132
09DTR/LOGIC	A03N1		1-01 *							1				133
09DTR/LOGIC	A15P2		1-02 *											133
09DTR/LOGIC			1									8-4/8		133
09REQ TO SEND/CON	A15T2		1-01 *							2				134
09REQ TO SEND/CON	B15L2		1-02 *											134
09REQ TO SEND/CON			1									4-2/8		134
09REQ TO SEND/LOGIC	A03P1		1-01 *							1				135
09REQ TO SEND/LOGIC	A15S2		1-02 *											135
09REQ TO SEND/LOGIC			1									8-6/8		135
09RING/CON	A15K2		1-01 *							1				136
09RING/CON	B15M2		1-02 *											136
09RING/CON			1									5-2/8		136
09RING/LOGIC	A03M1		1-01 *							1				137
09RING/LOGIC	A15C1		1-02 *											137
09RING/LOGIC			1									8-6/8		137
09SEC RX/LOGIC	A03V1		1-01 *							1				138
09SEC RX/LOGIC	A15E1		1-02 *											138
09SEC RX/LOGIC			1									9-0/8		138
09SEC TX/LOGIC	A03O1		1-01 *							1				139
09SEC TX/LOGIC	A15O2		1-02 *											139
09SEC TX/LOGIC			1									8-4/8		139
09SUP REC/CON	A15L2		1-01 *							1				140
09SUP REC/CON	A15F1		1-02 *											140
09SUP REC/CON			1									4-6/8		140

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DH1DDP.E RUN NAME	HND286.V23(P3) A/P PIN NAME	05/24/74 ORDER PIN ORDER	BAY - Q DRAW RV PG Y X Z	REMARKS	24-SEP-74 LENGTH	U152 EXCEPTIONS	PAGE 1. RUN NUMBER
09SUP TRAN/CON	A15U1	1-01 *					141
09SUP TRAN/CON	B15E1	1-02 *					141
09SUP TRAN/CON		1			3-4/8		141
10ACP	A1OT1	1-01 *					142
10ACP	A1OC2	1-02 *					142
10ACP	AOPC1	1-03 *					142
10ACP		1			10-4/8		142
10BC2	B1OC2	1-01 *					143
10BC2	B1OT1	1-02 *					143
10BC2		1			4-0/8		143
10CARRIER/CON	A16M2	1-01 *					144
10CARRIER/CON	B16P2	1-02 *					144
10CARRIER/CON		1			5-6/8		144
10CARRIER/LOGIC	A03J2	1-01 *					145
10CARRIER/LOGIC	A16B1	1-02 *					145
10CARRIER/LOGIC		1			9-0/8		145
10CLEAR TO SEND/CON	A16M2	1-01 *					146
10CLEAR TO SEND/CON	B16K2	1-02 *					146
10CLEAR TO SEND/CON		1			4-6/8		146
10CLEAR TO SEND/LOGIC	A03H2	1-01 *					147
10CLEAR TO SEND/LOGIC	A16F2	1-02 *					147
10CLEAR TO SEND/LOGIC		1			7-0/8		147
10DTR/CON	A16K2	1-01 *					148
10DTR/CON	B16R2	1-02 *					148
10DTR/CON		1			5-0/8		148
10DTR/LOGIC	A03E2	1-01 *					149
10DTR/LOGIC	A16P2	1-02 *					149
10DTR/LOGIC		1			9-2/8		149
10REQ TO SEND/CON	A16T2	1-01 *					150
10REQ TO SEND/CON	B16L2	1-02 *					150
10REQ TO SEND/CON		1			4-2/8		150
10REQ TO SFND/LOGIC	A03F2	1-01 *					151
10REQ TO SEND/LOGIC	A16S2	1-02 *					151
10REQ TO SEND/LOGIC		1			9-2/8		151

BN11DP.1 RUN NAME	MND288.V23(23) A/P PIN NAME	05/24/74 ORDER PIN ORDER	HAY - ORDER	Q	DRAW	KV	PG	Y	X	Z	REMARKS	24-SEP-74 LENGTH	0152 EXCEPTIONS	PAGE 14 RUN NUMBER
10RING/CON	A16K2	1-01 *								1				152
10RING/CON	B16M2	1-02 *												152
10RING/CON		1										5-2/8		152
10RING/LOGIC	A03D2	1-01 *								1				153
10RING/LOGIC	A16C1	1-02 *												153
10RING/LOGIC		1										8-4/8		153
10SEC RX/LOGIC	A03L2	1-01 *								1				154
10SEC RX/LOGIC	A16E1	1-02 *												154
10SEC RX/LOGIC		1										8-6/8		154
10SEC TX/LOGIC	A03K2	1-01 *								1				155
10SEC TX/LOGIC	A16U2	1-02 *												155
10SEC TX/LOGIC		1										9-2/8		155
10SUP REC/CON	A16L2	1-01 *								1				156
10SUP REC/CON	B16F1	1-02 *												156
10SUP REC/CON		1										4-6/8		156
10SUP TRAN/CON	A16U1	1-01 *								1				157
10SUP TRAN/CON	B16E1	1-02 *												157
10SUP TRAN/CON		1										3-4/8		157
11AC2	A11C2	1-01 *								2				158
11AC2	A11T1	1-02 *								1				158
11AC2	A02T1	1-03 *												158
11AC2		1										10-6/8		158
11BC2	B11C2	1-01 *								1				159
11BC2	B11T1	1-02 *												159
11BC2		1										4-0/8		159
11CARRIER/CON	A17M2	1-01 *								1				160
11CARRIER/CON	B17P2	1-02 *												160
11CARRIER/CON		1										5-6/8		160
11CARRIER/LOGIC	A03S2	1-01 *								1				161
11CARRIER/LOGIC	A17B1	1-02 *												161
11CARRIER/LOGIC		1										10-0/8		161
11CLEAR TO SEND/CON	A17M2	1-01 *								1				162
11CLEAR TO SEND/CON	B17K2	1-02 *												162
11CLEAR TO SEND/CON		1										4-6/8		162

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DM11DP.E RUN NAME	HND288.V23(23) 05/24/74 A/P PIN ORDER BAY - NAME PIN ORDER	Q	DRAW	RV	PG	Y	X	Z	REMARKS	24-SEP-74 LENGTH	0152 EXCEPTIONS	PAGE 17 RUN NUMBER
12RING/LOGIC	A18C1							1				185
12RING/LOGIC	B02D1											185
12RING/LOGIC										11-4/8		185
12SEC RX/LOGIC	A18E1							1				186
12SEC RX/LOGIC	B02L1											186
12SEC RX/LOGIC										11-6/8		186
12SEC TX/LOGIC	A18U2							1				187
12SEC TX/LOGIC	B02K1											187
12SEC TX/LOGIC										11-2/8		187
12SUP REC/CON	A18L2							1				188
12SUP REC/CON	B18F1											188
12SUP REC/CON										4-6/8		188
12SUP TRAN/CON	A18U1							1				189
12SUP TRAN/CON	B18E1											189
12SUP TRAN/CON										3-4/8		189
13ACP	A13C2							2				190
13ACP	A13T1							1				190
13ACP	A02T2											190
13ACP										11-4/8		190
13BCP	B13C2							1				191
13BCP	B13T1											191
13BCP										4-0/8		191
13CARRIER/CON	A19H2							1				192
13CARRIER/CON	B19P2											192
13CARRIER/CON										5-6/8		192
13CARRIER/LOGIC	A19H1							1				193
13CARRIER/LOGIC	B02S1											193
13CARRIER/LOGIC										12-6/8		193
13CLEAR TO SEND/CON	A19M2							1				194
13CLEAR TO SEND/CON	B19K2											194
13CLEAR TO SEND/CON										4-6/8		194
13CLEAR TO SEND/LOGIC	A19F2							1				195
13CLEAR TO SEND/LOGIC	B02R1											195
13CLEAR TO SEND/LOGIC										12-6/8		195

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DM11DP.E RUN NAME	HND288.V23(23) 05/24/74 A/P PIN ORDER BAY - NAME PIN ORDER	Q	DRAW	RV	PG	Y	X	Z	REMARKS	24-SEP-74 LENGTH	0152 EXCEPTIONS	PAGE 18 RUN NUMBER
13DTR/CON	A19R2							1				196
13DTR/CON	B19R2											196
13DTR/CON										5-0/8		196
13DTR/LOGIC	A19P2							1				197
13DTR/LOGIC	B02N1											197
13DTR/LOGIC										12-0/8		197
13REQ TO SEND/CON	A19T2							2				198
13REQ TO SEND/CON	B19L2											198
13REQ TO SEND/CON										4-2/8		198
13REQ TO SEND/LOGIC	A19S2							1				199
13REQ TO SEND/LOGIC	B02P1											199
13REQ TO SEND/LOGIC										12-2/8		199
13RING/CON	A19K2							1				200
13RING/CON	B19M2											200
13RING/CON										5-2/8		200
13RING/LOGIC	A19C1							1				201
13RING/LOGIC	B02M1											201
13RING/LOGIC										12-4/8		201
13SEC RX/LOGIC	A19E1							1				202
13SEC RX/LOGIC	B02V1											202
13SEC RX/LOGIC										12-4/8		202
13SEC TX/LOGIC	A19U2							1				203
13SEC TX/LOGIC	B02U1											203
13SEC TX/LOGIC										12-2/8		203
13SUP REC/CON	A19L2							1				204
13SUP REC/CON	B19F1											204
13SUP REC/CON										4-6/8		204
13SUP TRAN/CON	A19U1							1				205
13SUP TRAN/CON	B19E1											205
13SUP TRAN/CON										3-4/8		205
14ACP	A19T1							2				206
14ACP	A19C2							1				206
14ACP	A03C1											206
14ACP										12-0/8		206

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DI 11DP.E RUN NAME	HND288.V23(23) 05/24/74 A/P PIN ORDER PIN BAY - ORDER	W DRAW RV PG Y X Z	REMARKS	24-SEP-74 LENGTH	0152 EXCEPTIONS	PAGE 21 RUN NUMBER
15REL0 TO SEND/CON	A21T2	1-01 *				230
15REL0 TO SEND/CON	B21L2	1-02 *				230
15REL0 TO SEND/CON		1			4-2/8	230
15REL0 TO SEND/LOGIC	A21S2	1-01 *				231
15REL0 TO SEND/LOGIC	B02P2	1-02 *				231
15REL0 TO SEND/LOGIC		1			13-0/8	231
15RING/CON	A21K2	1-01 *				232
15RING/CON	B21M2	1-02 *				232
15RING/CON		1			5-2/8	232
15RING/LOGIC	A21C1	1-01 *				233
15RING/LOGIC	B02M2	1-02 *				233
15RING/LOGIC		1			13-2/8	233
15SUP REC/CON	A21LP	1-01 *				234
15SUP REC/CON	B21F1	1-02 *				234
15SUP REC/CON		1			4-6/8	234
15SUP REC/LOGIC	A21E1	1-01 *				235
15SUP REC/LOGIC	B02V2	1-02 *				235
15SUP REC/LOGIC		1			13-2/8	235
15SUP TRAN/CON	A21U1	1-01 *				236
15SUP TRAN/CON	B21E1	1-02 *				236
15SUP TRAN/CON		1			3-4/8	236
15SUP TRAN/LOGIC	A21U2	1-01 *				237
15SUP TRAN/LOGIC	B02U2	1-02 *				237
15SUP TRAN/LOGIC		1			13-0/8	237
16AC2	A16T1	1-01 *				238
16AC2	A16C2	1-02 *				238
16AC2	A03C2	1-03 *				238
16AC2		1			12-6/8	238
16BC2	B16C2	1-01 *				239
16BC2	B16T1	1-02 *				239
16BC2		1			4-0/8	239
17AC2	A17C2	1-01 *				240
17AC2	A17T1	1-02 *				240
17AC2	A03T2	1-03 *				240
17AC2		1			13-0/8	240

DN11DP.L RUN NAME	HND288.V23(23) 05/24/74 A/P PIN ORDER BAY - NAME PIN ORDER	Q	DRAW	RV	PG	Y	X	Z	REMARKS	24-SEP-74 LENGTH	0152 EXCEPTIONS	PAGE 22 RUN NUMBER
178C2	B17C2	1-01 *						1				241
178C2	B17T1	1-02 *										241
178C2		1								4-0/8		241
18AC2	A18C2	1-01 *						2				242
18AC2	A18T1	1-02 *						1				242
18AC2	B02C1	1-03 *										242
18AC2		1								15-0/8		242
188C2	B18C2	1-01 *						1				243
188C2	B18T1	1-02 *										243
188C2		1								4-0/8		243
19AC2	A19C2	1-01 *						2				244
19AC2	A19T1	1-02 *						1				244
19AC2	B02T1	1-03 *										244
19AC2		1								16-0/8		244
198C2	B19C2	1-01 *						1				245
198C2	B19T1	1-02 *										245
198C2		1								4-0/8		245
20AC2	A20C2	1-01 *						2				246
20AC2	A20T1	1-02 *						1				246
20AC2	B02C2	1-03 *										246
20AC2		1								15-6/8		246
208C2	B20C2	1-01 *						1				247
208C2	B20T1	1-02 *										247
208C2		1								4-0/8		247
21AC2	A21C2	1-01 *						2				248
21AC2	A21T1	1-02 *						1				248
21AC2	B02T2	1-03 *										248
21AC2		1								16-6/8		248
218C2	B21C2	1-01 *						1				249
218C2	B21T1	1-02 *										249
218C2		1								4-0/8		249
4AC2	A04C2	1-01 *						1				250
4AC2	A04T1	1-02 *										250
4AC2		1								4-0/8		250

DM11DP.L RUN NAME	HND288.V23(23) A/P PIN NAME	05/24/74 ORDER PIN	BAY - ORDER	Q	DRAW	RV	PG	Y	X	Z	REMARKS	24-SEP-74 LENGTH	0152 EXCEPTIONS	PAGE 25 RUN NUMBER
LINEOUT/DIFCON	A06M1		1-01 *							2				271
LINEOUT/DIFCON	B06D1		1-02 *							1				271
LINEOUT/DIFCON	B22M1		1-03 *											271
LINEOUT/DIFCON			1									14-6/8		271
LINEOUT/DIFCON+	A06L1		1-01 *							2				272
LINEOUT/DIFCON+	B06C1		1-02 *							1				272
LINEOUT/DIFCON+	B22L1		1-03 *											272
LINEOUT/DIFCON+			1									15-0/8		272
LINEOUT/LOGIC	A06V2		1-01 *							2				273
LINEOUT/LOGIC	B03D1		1-02 *							1				273
LINEOUT/LOGIC	B01D1		1-03 *							2				273
LINEOUT/LOGIC	B04V2		1-04 *							1				273
LINEOUT/LOGIC	B22V2		1-05 *											273
LINEOUT/LOGIC			1									23-6/8		273
LINEO1R/CON	A07J2		1-01 *							2				274
LINEO1R/CON	B07F2		1-02 *							1				274
LINEO1R/CON	B04J1		1-03 *											274
LINEO1R/CON			1									9-0/8		274
LINEO1R/DIFCON	A07P1		1-01 *							2				275
LINEO1R/DIFCON	B07N1		1-02 *							1				275
LINEO1R/DIFCON	B22E2		1-03 *											275
LINEO1R/DIFCON			1									15-2/8		275
LINEO1R/DIFCON+	A07N1		1-01 *							2				276
LINEO1R/DIFCON+	B07J1		1-02 *							1				276
LINEO1R/DIFCON+	B22J1		1-03 *											276
LINEO1R/DIFCON+			1									14-2/8		276
LINEO1R/LOGIC	A07D1		1-01 *							2				277
LINEO1R/LOGIC	B01E1		1-02 *							1				277
LINEO1R/LOGIC	B03E1		1-03 *							2				277
LINEO1R/LOGIC	B04K1		1-04 *							1				277
LINEO1R/LOGIC	B22K1		1-05 *											277
LINEO1R/LOGIC			1									24-2/8		277
LINEO1T/CON	A07V1		1-01 *							2				278
LINEO1T/CON	B07E2		1-02 *							1				278
LINEO1T/CON	B04S1		1-03 *											278
LINEO1T/CON			1									8-2/8		278

DM11DP.1 RUN NAME	HND286.V23(23) 05/24/74 A/P PIN ORDER PIN HAY - ORDER	Q DRAW KV PG Y X Z	REMARKS	24-SEP-74 LENGTH	0152 EXCEPTIONS	PAGE 26 RUN NUMBER
LINE01T/DIFCON	A07M1	1-01 *	2			279
LINE01T/DIFCON	B07D1	1-02 *	1			279
LINE01T/DIFCON	B22L2	1-03 *				279
LINE01T/DIFCON		1		14-b/8		279
LINE01T/DIFCON+	A07L1	1-01 *	2			280
LINE01T/DIFCON+	B07C1	1-02 *	1			280
LINE01T/DIFCON+	B22S1	1-03 *				280
LINE01T/DIFCON+		1		14-b/8		280
LINE01T/LOGIC	A07V2	1-01 *	2			281
LINE01T/LOGIC	B03F1	1-02 *	1			281
LINE01T/LOGIC	B01F1	1-03 *	2			281
LINE01T/LOGIC	B04K1	1-04 *	1			281
LINE01T/LOGIC	B22R1	1-05 *				281
LINE01T/LOGIC		1		24-0/8		281
LINE02R/CON	A08J2	1-01 *	2			282
LINE02R/CON	B08F2	1-02 *	1			282
LINE02R/CON	B04F1	1-03 *				282
LINE02R/CON		1		9-2/8		282
LINE02R/DIFCON	A0AP1	1-01 *	2			283
LINE02R/DIFCON	B08N1	1-02 *	1			283
LINE02R/DIFCON	B22H2	1-03 *				283
LINE02R/DIFCON		1		14-b/8		283
LINE02R/DIFCON+	A08N1	1-01 *	2			284
LINE02R/DIFCON+	B08J1	1-02 *	1			284
LINE02R/DIFCON+	B22F1	1-03 *				284
LINE02R/DIFCON+		1		14-0/8		284
LINE02R/LOGIC	B01H1	1-01 *	2			285
LINE02R/LOGIC	B03H1	1-02 *	1			285
LINE02R/LOGIC	B04H1	1-03 *	2			285
LINE02R/LOGIC	A0AD1	1-04 *	1			285
LINE02R/LOGIC	B22H1	1-05 *				285
LINE02R/LOGIC		1		23-0/8		285
LINE02T/CON	A0AV1	1-01 *	2			286
LINE02T/CON	B08E2	1-02 *	1			286
LINE02T/CON	B04U1	1-03 *				286
LINE02T/CON		1		8-b/8		286

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DM11DP.L RUN NAME	HND28A.V23(23) 05/24/74										REMARKS	24-SEP-74 LENGTH	U152 EXCEPTIONS	PAGE 24 RUN NUMBER
	A/P	PIN NAME	ORDER PIN	BAY - ORDER	Q	DRAW	RV	PG	Y	X	Z			
LINE04T/DIFCON		A10M1		1-01 *							2			303
LINE04T/DIFCON		B10D1		1-02 *							1			303
LINE04T/DIFCON		B23M1		1-03 *										303
LINE04T/DIFCON				1								13-2/8		303
LINE04T/DIFCON+		A10L1		1-01 *							2			304
LINE04T/DIFCON+		B10C1		1-02 *							1			304
LINE04T/DIFCON+		B23L1		1-03 *										304
LINE04T/DIFCON+				1								13-4/8		304
LINE04T/LOGIC		B01N1		1-01 *							2			305
LINE04T/LOGIC		B03N1		1-02 *							1			305
LINE04T/LOGIC		B05V2		1-03 *							2			305
LINE04T/LOGIC		A10V2		1-04 *							1			305
LINE04T/LOGIC		B23V2		1-05 *										305
LINE04T/LOGIC				1								23-4/8		305
LINE05R/CON		A11J2		1-01 *							2			306
LINE05R/CON		B11F2		1-02 *							1			306
LINE05R/CON		B05J1		1-03 *										306
LINE05R/CON				1								10-4/8		306
LINE05R/DIFCON		A11P1		1-01 *							2			307
LINE05R/DIFCON		B11N1		1-02 *							1			307
LINE05R/DIFCON		B23E2		1-03 *										307
LINE05R/DIFCON				1								13-6/8		307
LINE05R/DIFCON+		A11N1		1-01 *							2			308
LINE05R/DIFCON+		B11J1		1-02 *							1			308
LINE05R/DIFCON+		B23J1		1-03 *										308
LINE05R/DIFCON+				1								12-6/8		308
LINE05R/LOGIC		B01P1		1-01 *							2			309
LINE05R/LOGIC		B03P1		1-02 *							1			309
LINE05R/LOGIC		B05K1		1-03 *							2			309
LINE05R/LOGIC		A11D1		1-04 *							1			309
LINE05R/LOGIC		B23K1		1-05 *										309
LINE05R/LOGIC				1								23-4/8		309
LINE05T/CON		A11V1		1-01 *							2			310
LINE05T/CON		B11E2		1-02 *							1			310
LINE05T/CON		B05S1		1-03 *										310
LINE05T/CON				1								9-6/8		310

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DM11DP.L RUN NAME	HND28A.V23(23) 05/24/74										REMARKS	24-SEP-74 LENGTH	U152 EXCEPTIONS	PAGE 30 RUN NUMBER
	A/P	PIN NAME	ORDER PIN	BAY - ORDER	Q	DRAW	RV	PG	Y	X	Z			
LINE05T/DIFCON		A11M1		1-01 *							2			311
LINE05T/DIFCON		B11D1		1-02 *							1			311
LINE05T/DIFCON		B23L2		1-03 *										311
LINE05T/DIFCON				1								13-2/8		311
LINE05T/DIFCON+		A11L1		1-01 *							2			312
LINE05T/DIFCON+		B11C1		1-02 *							1			312
LINE05T/DIFCON+		B23S1		1-03 *										312
LINE05T/DIFCON+				1								13-2/8		312
LINE05T/LOGIC		B01R1		1-01 *							2			313
LINE05T/LOGIC		B03R1		1-02 *							1			313
LINE05T/LOGIC		B05R1		1-03 *							2			313
LINE05T/LOGIC		A11V2		1-04 *							1			313
LINE05T/LOGIC		B23R1		1-05 *										313
LINE05T/LOGIC				1								22-0/8		313
LINE06R/CON		A12J2		1-01 *							2			314
LINE06R/CON		B12F2		1-02 *							1			314
LINE06R/CON		B05F1		1-03 *										314
LINE06R/CON				1								10-6/8		314
LINE06R/DC		A12P1		1-01 *							2			315
LINE06R/DC		B12N1		1-02 *							1			315
LINE06R/DC		B23H2		1-03 *										315
LINE06R/DC				1								13-2/8		315
LINE06R/DIFCON+		A12N1		1-01 *							2			316
LINE06R/DIFCON+		B12J1		1-02 *							1			316
LINE06R/DIFCON+		B23F1		1-03 *										316
LINE06R/DIFCON+				1								12-4/8		316
LINE06R/LOGIC		B01S1		1-01 *							2			317
LINE06R/LOGIC		B03S1		1-02 *							1			317
LINE06R/LOGIC		B05H1		1-03 *							2			317
LINE06R/LOGIC		A12D1		1-04 *							1			317
LINE06R/LOGIC		B23H1		1-05 *										317
LINE06R/LOGIC				1								23-2/8		317
LINE06T/CON		A12V1		1-01 *							2			318
LINE06T/CON		B12E2		1-02 *							1			318
LINE06T/CON		B05U1		1-03 *										318
LINE06T/CON				1								10-2/8		318

DM11DP.E RUN NAME	HND288.V23(23) 05/24/74				Q	DRAW	RV	PG	Y	X	Z	REMARKS	24-SEP-74 LENGTH	0152 EXCEPTIONS	PAGE 31 RUN NUMBER
A/P	PIN NAME	ORDER PIN	HAY - ORDER												
LINE06T/DIFCON	A12M1		1-01 *								2				319
LINE06T/DIFCON	B12D1		1-02 *								1				319
LINE06T/DIFCON	B23M2		1-03 *												319
LINE06T/DIFCON			1										12-4/8		319
LINE06T/DIFCON+	A12L1		1-01 *								2				320
LINE06T/DIFCON+	B12C1		1-02 *								1				320
LINE06T/DIFCON+	B23V1		1-03 *												320
LINE06T/DIFCON+			1										13-0/8		320
LINE06T/LOGIC	B01T1		1-01 *								2				321
LINE06T/LOGIC	B03T1		1-02 *								1				321
LINE06T/LOGIC	B05U2		1-03 *								2				321
LINE06T/LOGIC	A12V2		1-04 *								1				321
LINE06T/LOGIC	B23U2		1-05 *												321
LINE06T/LOGIC			1										22-4/8		321
LINE07R/CON	A13J2		1-01 *								2				322
LINE07R/CON	B13F2		1-02 *								1				322
LINE07R/CON	B05H2		1-03 *												322
LINE07R/CON			1										11-2/8		322
LINE07R/DIFCON	A13P1		1-01 *								2				323
LINE07R/DIFCON	B13N1		1-02 *								1				323
LINE07R/DIFCON	B23J2		1-03 *												323
LINE07R/DIFCON			1										12-6/8		323
LINE07R/DIFCON+	A13N1		1-01 *								2				324
LINE07R/DIFCON+	B13J1		1-02 *								1				324
LINE07R/DIFCON+	B23K2		1-03 *												324
LINE07R/DIFCON+			1										12-0/8		324
LINE07R/LOGIC	B03U1		1-01 *								2				325
LINE07R/LOGIC	B01U1		1-02 *								1				325
LINE07R/LOGIC	B05B1		1-03 *								2				325
LINE07R/LOGIC	A13D1		1-04 *								1				325
LINE07R/LOGIC	B23B1		1-05 *												325
LINE07R/LOGIC			1										24-4/8		325
LINE07T/CON	A13V1		1-01 *								2				326
LINE07T/CON	B13E2		1-02 *								1				326
LINE07T/CON	B05T2		1-03 *												326
LINE07T/CON			1										10-2/8		326

DM11DP.E RUN NAME	HND288.V23(23) 05/24/74				Q	DRAW	RV	PG	Y	X	Z	REMARKS	24-SEP-74 LENGTH	0152 EXCEPTIONS	PAGE 32 RUN NUMBER
A/P	PIN NAME	ORDER PIN	HAY - ORDER												
LINE07T/DIFCON	A13M1		1-01 *								2				327
LINE07T/DIFCON	B13D1		1-02 *								1				327
LINE07T/DIFCON	B23R2		1-03 *												327
LINE07T/DIFCON			1										12-4/8		327
LINE07T/DIFCON+	A13L1		1-01 *								2				328
LINE07T/DIFCON+	B13C1		1-02 *								1				328
LINE07T/DIFCON+	B23T2		1-03 *												328
LINE07T/DIFCON+			1										12-6/8		328
LINE07T/LOGIC	B01V1		1-01 *								2				329
LINE07T/LOGIC	B03V1		1-02 *								1				329
LINE07T/LOGIC	B05S2		1-03 *								2				329
LINE07T/LOGIC	A13V2		1-04 *								1				329
LINE07T/LOGIC	B23S2		1-05 *												329
LINE07T/LOGIC			1										22-6/8		329
LINE08R/CON	A04J2		1-01 *								1				330
LINE08R/CON	A14J2		1-02 *								2				330
LINE08R/CON	B14F2		1-03 *												330
LINE08R/CON			1										12-0/8		330
LINE08R/DIFCON	A22P1		1-01 *								1				331
LINE08R/DIFCON	A14P1		1-02 *								2				331
LINE08R/DIFCON	B14N1		1-03 *												331
LINE08R/DIFCON			1										11-2/8		331
LINE08R/DIFCON+	A22N1		1-01 *								1				332
LINE08R/DIFCON+	A14N1		1-02 *								2				332
LINE08R/DIFCON+	B14J1		1-03 *												332
LINE08R/DIFCON+			1										10-6/8		332
LINE08R/LOGIC	A22D1		1-01 *								1				333
LINE08R/LOGIC	A14D1		1-02 *								2				333
LINE08R/LOGIC	A04D1		1-03 *								1				333
LINE08R/LOGIC	B03C2		1-04 *								2				333
LINE08R/LOGIC	B01C2		1-05 *												333
LINE08R/LOGIC			1										22-0/8		333
LINE08T/CON	A04V1		1-01 *								1				334
LINE08T/CON	A14V1		1-02 *								2				334
LINE08T/CON	B14E2		1-03 *												334
LINE08T/CON			1										10-6/8		334

PAGE 33
RUN
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PAGE 34
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TEST EQUIPMENT

[illegible]

DM11DP.E RUN NAME	HND288.V23(23) A/P PIN NAME	05/24/74 ORDER PIN	BAY - ORDER	Q	DRAW	RV	PG	Y	X	Z	REMARKS	24-SEP-74 LENGTH	0152 EXCEPTIONS	PAGE 36 RUN NUMBER
LINE11T/DIFCON	A22R2		1-01 *							1				354
LINE11T/DIFCON	A17M1		1-02 *							2				354
LINE11T/DIFCON	B17D1		1-03 *											354
LINE11T/DIFCON			1									9-6/8		354
LINE11T/DIFCON+	A22T2		1-01 *							1				360
LINE11T/DIFCON+	A17L1		1-02 *							2				360
LINE11T/DIFCON+	B17C1		1-03 *											360
LINE11T/DIFCON+			1									9-6/8		360
LINE11T/LOGIC	A22S2		1-01 *							2				361
LINE11T/LOGIC	A17V2		1-02 *							1				361
LINE11T/LOGIC	A04S2		1-03 *							2				361
LINE11T/LOGIC	B03L2		1-04 *							1				361
LINE11T/LOGIC	B01L2		1-05 *											361
LINE11T/LOGIC			1									22-2/8		361
LINE12R/CON	A05J2		1-01 *							1				362
LINE12R/CON	A18J2		1-02 *							2				362
LINE12R/CON	B18F2		1-03 *											362
LINE12R/CON			1									13-4/8		362
LINE12R/DIFCON	A23P1		1-01 *							1				363
LINE12R/DIFCON	A1AP1		1-02 *							2				363
LINE12R/DIFCON	B1AN1		1-03 *											363
LINE12R/DIFCON			1									9-6/8		363
LINE12R/DIFCON+	A23N1		1-01 *							1				364
LINE12R/DIFCON+	A1AN1		1-02 *							2				364
LINE12R/DIFCON+	B1AJ1		1-03 *											364
LINE12R/DIFCON+			1									9-2/8		364
LINE12R/LOGIC	A23D1		1-01 *							2				365
LINE12R/LOGIC	A18D1		1-02 *							1				365
LINE12R/LOGIC	A05D1		1-03 *							2				365
LINE12R/LOGIC	B03M2		1-04 *							1				365
LINE12R/LOGIC	B01M2		1-05 *											365
LINE12R/LOGIC			1									23-0/8		365
LINE12T/CON	A05V1		1-01 *							1				366
LINE12T/CON	A1AV1		1-02 *							2				366
LINE12T/CON	B18F2		1-03 *											366
LINE12T/CON			1									12-2/8		366

DM11DP.E RUN NAME	HND288.V23(23) 05/24/74				Q	DRAW	RV	PG	Y	X	Z	REMARKS	24-SEP-74 LENGTH	0152 EXCEPTIONS	PAGE 3 RUN NUMBER
	A/P	PIN NAME	ORDER PIN	BAY - ORDER											
LINE14T/DIFCON		A23M2		1-01 *							1				383
LINE14T/DIFCON		A20M1		1-02 *							2				383
LINE14T/DIFCON		B20D1		1-03 *											383
LINE14T/DIFCON				1									8-2/8		383
LINE14T/DIFCON+		A20L1		1-01 *							2				384
LINE14T/DIFCON+		B20C1		1-02 *							1				384
LINE14T/DIFCON+		A23V1		1-03 *											384
LINE14T/DIFCON+				1									8-4/8		384
LINE14T/LOGIC		A23U2		1-01 *							2				385
LINE14T/LOGIC		A20V2		1-02 *							1				385
LINE14T/LOGIC		A05U2		1-03 *							2				385
LINE14T/LOGIC		B03T2		1-04 *							1				385
LINE14T/LOGIC		B01T2		1-05 *											385
LINE14T/LOGIC				1									22-2/8		385
LINE15R/CON		A05H2		1-01 *							1				386
LINE15R/CON		A21J2		1-02 *							2				386
LINE15R/CON		B21F2		1-03 *											386
LINE15R/CON				1									15-2/8		386
LINE15R/DIFCON		A23J2		1-01 *							2				387
LINE15R/DIFCON		A21P1		1-02 *							1				387
LINE15R/DIFCON		B21N1		1-03 *											387
LINE15R/DIFCON				1									9-0/8		387
LINE15R/DIFCON+		A23K2		1-01 *							2				388
LINE15R/DIFCON+		A21N1		1-02 *							1				388
LINE15R/DIFCON+		B21J1		1-03 *											388
LINE15R/DIFCON+				1									8-2/8		388
LINE15R/LOGIC		A23B1		1-01 *							2				389
LINE15R/LOGIC		A21D1		1-02 *							1				389
LINE15R/LOGIC		A05B1		1-03 *							2				389
LINE15R/LOGIC		B03U2		1-04 *							1				389
LINE15R/LOGIC		B01U2		1-05 *											389
LINE15R/LOGIC				1									24-4/8		389
LINE15T/CON		A05T2		1-01 *							1				390
LINE15T/CON		A21V1		1-02 *							2				390
LINE15T/CON		B21E2		1-03 *											390
LINE15T/CON				1									13-6/8		390

DM11DP.E RUN NAME	HND288.V23(23) 05/24/74				Q	DRAW	RV	PG	Y	X	Z	REMARKS	24-SEP-74 LENGTH	0152 EXCEPTIONS	PAGE 40 RUN NUMBER
	A/P	PIN NAME	ORDER PIN	BAY - ORDER											
LINE15T/DIFCON		A23R2		1-01 *							1				391
LINE15T/DIFCON		A21M1		1-02 *							2				391
LINE15T/DIFCON		B21D1		1-03 *											391
LINE15T/DIFCON				1									8-2/8		391
LINE15T/DIFCON+		A23T2		1-01 *							1				392
LINE15T/DIFCON+		A21L1		1-02 *							2				392
LINE15T/DIFCON+		B21C1		1-03 *											392
LINE15T/DIFCON+				1									8-2/8		392
LINE15T/LOGIC		A23S2		1-01 *							2				393
LINE15T/LOGIC		A21V2		1-02 *							1				393
LINE15T/LOGIC		A05S2		1-03 *							2				393
LINE15T/LOGIC		B03V2		1-04 *							1				393
LINE15T/LOGIC		B01V2		1-05 *											393
LINE15T/LOGIC				1									23-2/8		393

DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS			LEGEND		QUANTITY / VARIATION															
ACCESSORY LIST			D DOCUMENT DN DOCUMENT CHANGE NOTICE PA PAPER TAPE ASCII PB PAPER TAPE BINARY PM PAPER TAPE READ-IN-MODE																	
MADE BY J. MCNAMARA DATE 2-21-73		CHECKED D. GLEZEN DATE 2-22-72		SECTION																
ENG J. MCNAMARA DATE 2-21-73		PROD S. BORENSTEIN DATE 2-23-73		ISSUED SECT.																
ITEM NO.	DWG NO. / PART NO.	DESCRIPTION				DH11-AA	DH11-AB	DH11-AC	DH11-AD	DH11-AE				KIT CHECK	BY	DATE	INSTALLATION CHECK	BY	DATE	
1.	DEC-11-HDHAA-B-D	DH11 Asynchronous 16-line Programmable Mux Manual				1	1	1	1	1										
2.	ZJ-114 -RP	Software (Libkit contains items listed on A-SL-																		
		DH11-O-7)				1	1	1	-	1										
3.	DH11 print set A	Customer Print Set (DH11 -AA,AB,AC.)				1	1	1	-	-										
4.	DH11 print set B	Customer Print Set (DH11-AD,AE)				-	-	-	1	1										
5.	ZJ179-RP	DH11-AD Software Kit (contains items																		
		Listed On A-SL-DH11-O-7)				-	-	-	1	-										
6.	F8611	M5906 Test Connector				-	-	-	2	2										
7.	F861	Modem Control Test Connector				-	-	-	1	-										
8.	F815	Distribution Panel Output Test Connector				-	-	-	1	1										
TITLE		DH11-A Acessory List		ASSY. NO. / /		SIZE CODE		A AL		NUMBER		DH11-0-6		REV.		D		ECO NO		
				SHEET 1 OF 1		DIST.														

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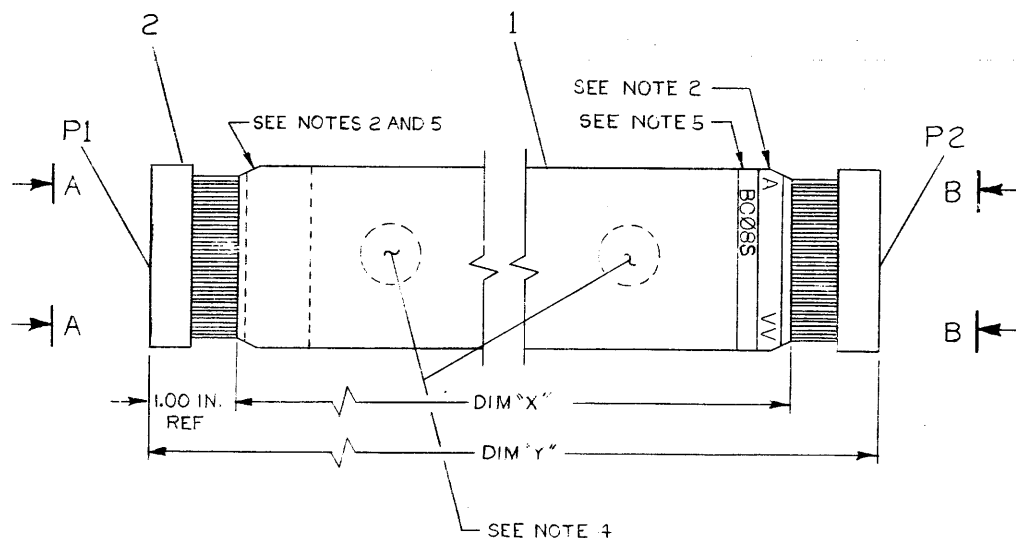
LEGEND

NUMBER	DIM "X" VAR	DIM "Y" REF
BC08S-1	10.00 IN. ± 1.00 IN.	1.00 FT. ± 1.00 IN.
BC08S-1B	14.00 IN. ± 1.00 IN.	16.00 IN. ± 1.00 IN.
BC08S-1K	2.00 FT. 9.00 IN. ± 1.00 IN.	2.00 FT. 11.00 IN. ± 1.00 IN.
BC08S-5L	70.00 IN. ± 1.50 IN.	72.00 IN. ± 1.50 IN.
BC08S-7	7.00 FT. ± 2.00 IN.	70.00 FT. 2.00 IN. ± 2.00 IN.
BC08S-8	8.00 FT. ± 2.00 IN.	80.00 FT. 2.00 IN. ± 2.00 IN.
BC08S-9	9.00 FT. ± 2.00 IN.	90.00 FT. 2.00 IN. ± 2.00 IN.
BC08S-10	10.00 FT. ± 2.00 IN.	10.00 FT. 2.00 IN. ± 2.00 IN.
BC08S-11	11.00 FT. ± 3.00 IN.	11.00 FT. 2.00 IN. ± 3.00 IN.
BC08S-12	12.00 FT. ± 3.00 IN.	12.00 FT. 2.00 IN. ± 3.00 IN.
BC08S-13	13.00 FT. ± 3.00 IN.	13.00 FT. 2.00 IN. ± 3.00 IN.
BC08S-14	14.00 FT. ± 3.00 IN.	14.00 FT. 2.00 IN. ± 3.00 IN.
BC08S-15	15.00 FT. ± 5.00 IN. - 0.00 IN.	15.00 FT. 2.00 IN. ± 5.00 IN.
BC08S-16	16.00 FT. ± 3.00 IN.	16.00 FT. 2.00 IN. ± 3.00 IN.
BC08S-17	17.00 FT. ± 3.00 IN.	17.00 FT. 2.00 IN. ± 3.00 IN.
BC08S-18	18.00 FT. ± 3.00 IN.	18.00 FT. 2.00 IN. ± 3.00 IN.
BC08S-19	19.00 FT. ± 3.00 IN.	19.00 FT. 2.00 IN. ± 3.00 IN.
BC08S-20	20.00 FT. ± 3.00 IN.	20.00 FT. 2.00 IN. ± 3.00 IN.
BC08S-25	25.00 FT. ± 3.00 FT.	25.00 FT. 2.00 IN. ± 3.00 IN.
BC08S-30	30.00 FT. ± 0.400 FT.	30.00 FT. 2.00 IN. ± 0.400 FT.
BC08S-35	35.00 FT. ± 0.700 FT.	35.00 FT. 2.00 IN. ± 0.700 FT.
BC08S-50	50.00 FT. ± 1.000 FT.	50.00 FT. 2.00 IN. ± 1.000 FT.
BC08S-Z	2.00 FT. ± 1.00 IN.	2.00 FT. 2.00 IN. ± 1.00 IN.

NOTES:

- CONNECTORS P1 AND P2, ARE TO BE WIRED POINT TO POINT.
- CONNECTOR LEGEND IDENTIFICATION TO BE PLACED ON SHIELD SIDE OF CABLE AT ONE END, AND WIRE SIDE OF CABLE ON THE OTHER END.
- MUST BE ASSEMBLED TO PROCESS SPECIFICATION 7606485-0-0.
- INSPECTION AND TEST STAMPS TO BE PLACED AT EACH END OF THE CABLE ASSEMBLY.
- THE NUMBER BC08S MUST BE ON THE CABLE IN CONJUNCTION WITH CONNECTOR LEGEND IDENTIFICATION.

VIEW A-A
CONN. LEGEND REF



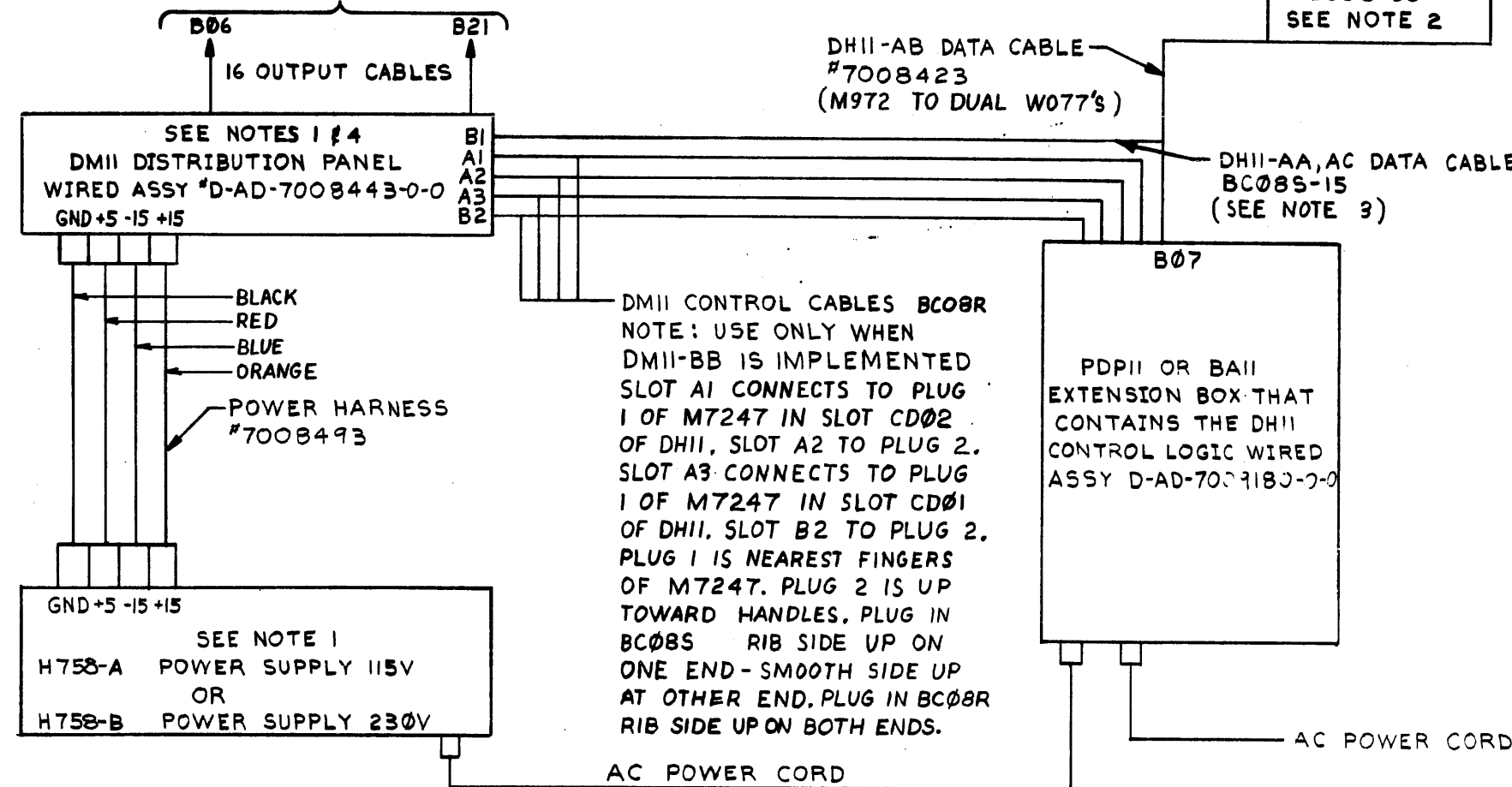
VIEW B-B
CONN. LEGEND REF

REV.	CHANGE NO.	BY	DATE
1	1	BL/COBS	00011 N
2	2	BL/COBS	00011 N
3	3	BL/COBS	00011 N
4	4	BL/COBS	00011 N
5	5	BL/COBS	00011 N
6	6	BL/COBS	00011 N
7	7	BL/COBS	00011 N
8	8	BL/COBS	00011 N
9	9	BL/COBS	00011 N
10	10	BL/COBS	00011 N
11	11	BL/COBS	00011 N
12	12	BL/COBS	00011 N
13	13	BL/COBS	00011 N
14	14	BL/COBS	00011 N
15	15	BL/COBS	00011 N
16	16	BL/COBS	00011 N
17	17	BL/COBS	00011 N
18	18	BL/COBS	00011 N
19	19	BL/COBS	00011 N
20	20	BL/COBS	00011 N
21	21	BL/COBS	00011 N
22	22	BL/COBS	00011 N
23	23	BL/COBS	00011 N
24	24	BL/COBS	00011 N
25	25	BL/COBS	00011 N
26	26	BL/COBS	00011 N
27	27	BL/COBS	00011 N
28	28	BL/COBS	00011 N
29	29	BL/COBS	00011 N
30	30	BL/COBS	00011 N
31	31	BL/COBS	00011 N
32	32	BL/COBS	00011 N
33	33	BL/COBS	00011 N
34	34	BL/COBS	00011 N
35	35	BL/COBS	00011 N
36	36	BL/COBS	00011 N
37	37	BL/COBS	00011 N
38	38	BL/COBS	00011 N
39	39	BL/COBS	00011 N
40	40	BL/COBS	00011 N
41	41	BL/COBS	00011 N
42	42	BL/COBS	00011 N
43	43	BL/COBS	00011 N
44	44	BL/COBS	00011 N
45	45	BL/COBS	00011 N
46	46	BL/COBS	00011 N
47	47	BL/COBS	00011 N
48	48	BL/COBS	00011 N
49	49	BL/COBS	00011 N
50	50	BL/COBS	00011 N

2	CONNECTOR, 40 SOCKET	1211206	2
1	CABLE, FLAT 40 COND	1700064	1
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES			
ANGLES 45° OR 90°			
SURFACE QUALITY IN			
FINISH			
QUANTITY & VARIATION			
THIRD ANGLE PROJECTION			
REMOVE BURRS AND BREAK SHARP CORNERS			
DO NOT SCALE DIMS			
MATERIAL			
FINISH			
DRAWN J. FERRELL 5-12-71			
CHK'D D.K. CRABBE 5-13-71			
ENG'D D.K. CRABBE 5-13-71			
PROD. P. FAZIO 5-21-71			
NEXT HIGHER ASSY.			
A-PL-DR8-EA-0			
SCALE NONE			
SHEET 1 OF 1			
DATE 5-21-71			
TITLE I/O CABLE ASS'Y (DIAG. JUMPER)			
SIZE CODE NUMBER			
D 1A BC08S-0-0 N			

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OUTPUT CABLES ARE EITHER BC01R-25 IF EIA OR M973 MATE-N-LOCK CONNECTOR CARD FOR PDP-11 TTY
NOTE: NEITHER ITEM SUPPLIED WITH DH11-AA

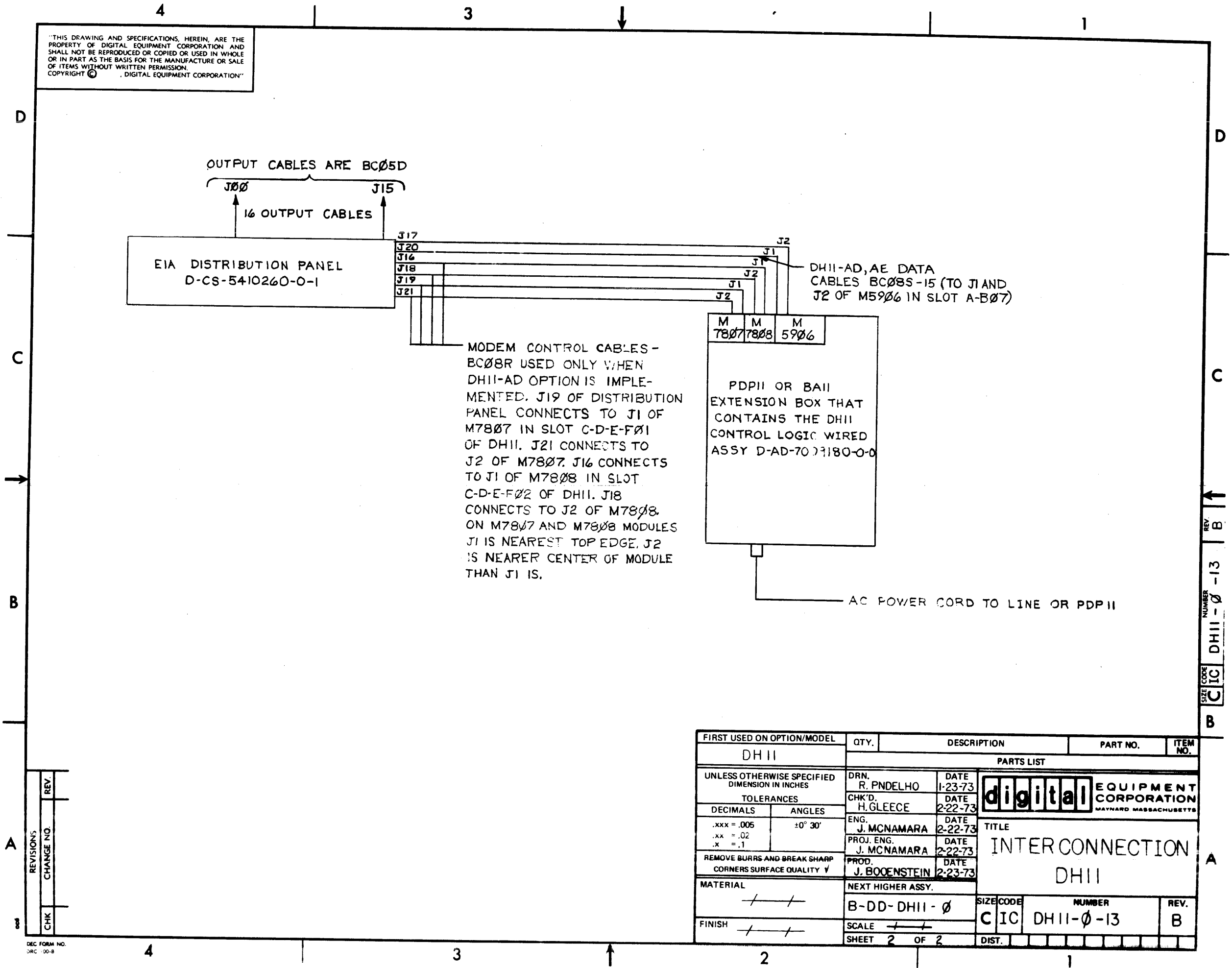


- NOTES:
1. DISTRIBUTION PANEL 7008443 AND POWER SUPPLY H758 SUPPLIED ONLY WITH DH11-AA, DH11-AC
 2. DC08 CS MUST BE ORDERED SEPARATELY DH11-AB DATA CABLE PLUGS INTO SLOTS A31, A32 OF DC08 CS FOR LINES 00 TO LINE 15 OF DC08 CS. A SECOND DH11-AB PLUGS INTO THE DC08 CS AT SLOTS B31, B32 FOR LINES 16 TO 31. THE W077 CONNECTED TO SIDE 1 OF M972 GOES TO A31 (B31). W077 CONNECTED TO SIDE 2 OF M972 GOES TO A32 (B32).
 3. A BC08S IS WIRED STRAIGHT POINT TO POINT. A BC08R IS WIRED MIRROR IMAGE: PIN A AT ONE END IS PIN VV AT OTHER END.
 4. WIRED ASSY 7008443 PLUS POWER WIRING, END PANELS & HOLD DOWN BAR ADDED ON PRODUCTION FLOOR IS 7008456 LOGIC ASSY.
 5. FOR DH11-AD, -AE OPTIONS, SEE SHEET 2.

REV.	CHANGE NO.	DATE	BY	CHK
A	00002	1-12-73	J. MCNAMARA	
B	00007	8-6-73	J. MCNAMARA	
C	00010	10-31-74	J. MCNAMARA	
D	00011	11-5-74	J. MCNAMARA	

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
DH11				
PARTS LIST				
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES	DRN	DATE	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS	
TOLERANCES	CHK'D	DATE	TITLE	
DECIMALS	ENG	DATE	INTERCONNECTION	
ANGLES	PROJ. ENG.	DATE	DH11	
.xxx = .005	PROD.	DATE	SIZE CODE	
.xx = .02			NUMBER	
.x = .1			REV.	
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY 1			B	
MATERIAL	NEXT HIGHER ASSY.		DIST.	
FINISH				
	B-DD-DH11-0			
	SCALE			
	SHEET 1 OF 2			

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OUTPUT CABLES ARE BC05D
J00 J15
16 OUTPUT CABLES

EIA DISTRIBUTION PANEL
D-CS-5410260-0-1

J17
J20
J16
J18
J19
J21

MODEM CONTROL CABLES -
BC08R USED ONLY WHEN
DH11-AD OPTION IS IMPE-
MENTED. J19 OF DISTRIBUTION
PANEL CONNECTS TO J1 OF
M7807 IN SLOT C-D-E-F01
OF DH11. J21 CONNECTS TO
J2 OF M7807. J16 CONNECTS
TO J1 OF M7808 IN SLOT
C-D-E-F02 OF DH11. J18
CONNECTS TO J2 OF M7808.
ON M7807 AND M7808 MODULES
J1 IS NEAREST TOP EDGE, J2
IS NEARER CENTER OF MODULE
THAN J1 IS.

J2
J1
J2
J1

DH11-AD, AE DATA
CABLES BC08S-15 (TO J1 AND
J2 OF M5906 IN SLOT A-B07)

M M M
7807 7808 5906
PDP11 OR BAI
EXTENSION BOX THAT
CONTAINS THE DH11
CONTROL LOGIC WIRED
ASSY D-AD-7007180-0-0

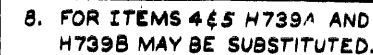
AC POWER CORD TO LINE OR PDP11

REV.	CHANGE NO.	CHK

FIRST USED ON OPTION/MODEL		QTY.	DESCRIPTION	PART NO.	ITEM NO.
DH11					
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES					
TOLERANCES					
DECIMALS	ANGLES				
.xxx = .005	±0° 30'				
.xx = .02					
.x = .1					
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY V					
MATERIAL		NEXT HIGHER ASSY.			
FINISH		SCALE			
		SHEET 2 OF 2			
		B-DD-DH11-0		SIZE CODE CIC	NUMBER DH11-0-13
				REV. B	

DRN. R. PNDELHO	DATE 1-23-73	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
CHK'D. H. GLEECE	DATE 2-22-73	
ENG. J. MCNAMARA	DATE 2-22-73	
PROJ. ENG. J. MCNAMARA	DATE 2-22-73	
PROD. J. BOONSTEIN	DATE 2-23-73	
TITLE INTER CONNECTION DH11		

DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS					QUANTITY / VARIATION														
PARTS LIST																			
MADE BY John McNamara			CHECKED K. GLEZEN		SECTION														
DATE 2-22-73			DATE 2-22-73																
ENG John McNamara			PROD B. DIGREGORIO		ISSUED SECT.														
DATE 2-22-73			DATE 2-22-73																
ITEM NO.	DWG NO. / PART NO.	DESCRIPTION			DH11-AA	DH11-AB	DH11-AC	DH11-AD	DH11-AE										
1.	M7277	Current Address and Address Select			1	1	1	1	1										
2.	M7278	Registers and Byte Count			1	1	1	1	1										
3.	M7279	FIFO Buffer			1	1	1	1	1										
4.	M7280	Multiple UARTs			2	2	2	2	2										
5.	M7288	Line Parameter Control			1	1	1	1	1										
6.	M7289	System Control and Receiver Scan			1	1	1	1	1										
7.	G7360	Priority Selector			1	1	1	-	-										
8.	5408778	Priority Jumper Plug-Level #5			2	2	2	2	2										
9.	M4540	DH11 DC11 Clock			1	1	1	1	1										
10.	M7821	Interrupt Control			2	2	2	2	2										
11.	M796	Unibus Master Control			1	1	1	1	1										
12.	M920	Internal Bus Connector			1	1	1	1	1										
13.	M971	Cable Interface			2	-	2	-	-										
14.	M974	DM11 Maintenance Jumper			1	1	1	-	-										
15.	G727	Grant Continuity Card			1	1	1	1	1										
16.	M5906	EIA CONVERSION AND PRIORITY SELECTION			-	-	-	1	1										
17.	M7807	BUS CONTROL+MUX (MODEM CONTROL)			-	-	-	1	-										
18.	M7808	MODEM CONTROL			-	-	-	1	-										
TITLE DH11 Module Utilization (PL)			ASSY NO. B-DD-DH11-ø		SIZE A	CODE PL	NUMBER DH11-ø-3				REV. D	ECO NO. DH11-00007							
			SHEET 1 OF 1		DIST.														



1. B61 POWER CONTROL MUST BF LOCATED AT FRONT OF CABINET TO ALLOW CABLES FROM ITEM 6OR19 TO SWEEP BEHIND AND UNDER ITEM 2.
2. ITEM #10 IS USED WHEN A DM11-BB IS INSTALLED,OR WITH A DH11-AD.
3. INSTALL THIS POWER SUPPLY FOR FIRST DH11, HOLES 75,79.
4. INSTALL THIS POWER SUPPLY FOR SECOND DH11, HOLES 93,97.
5. EACH H960 CONTAINING A DH11 SHALL HAVE ONE STRAIN RELIEF (ITEM 14) AND CLAMP (ITEM 15) FOR BC08R+S CABLES AND ONE STRAIN RELIEF AT THE LOWER REAR OF CABINET, SEE VIEW "A-A" AND "B-B". RETURN EXTRA ITEMS 14+15 TO STOCKROOM.
6. A CABINET THAT CONTAINS AN EXPANDER BOX CANNOT HAVE MORE THAN TWO DISTRIBUTION PANELS (ITEMS 6 OR 19). FOR DH11 SYSTEMS WITH THREE OR MORE DISTRIBUTION PANELS, A SEPARATE CABINET MUST BE USED. UP TO FOUR PANELS CAN BE MOUNTED INTO CABINETS WITHOUT AN EXPANDER BOX.
7. FOR 11/35-11/40 CPU WITH SERIAL NO. LESS THAN 6000 OR H960-D/E WITH SERIAL NO. LESS THAN 7000 USE POWER HARNESS 7009466.

DHII-AE	DHII-AD	DHII-AB	DHII-AC	DHII-AA	
					LESS THAN 6000 OR H960-D/E WITH SERIAL NO. LESS THAN 7000 USE POWER HARNESS 7009466.
4	4	4	4	4	SCR. PHIL PAN HD 8-32x3/8 9006037-1 24
1	1	1	1	1	SUPPORT HARNESS 7010167 23
4	4	-	4	4	WASHER, LOCK #10 EXT. 9007651 22
1	1	-	1	1	CROSS BAR CABLE BKT. D-MD-740851000 21
2	2	-	2	2	SIDE BAR SUPPORT C-IA-M08283-0-0 20
1	1	-	-	-	H317-B CABLE BOX ASSY D-UA-H317-0-0 19
8	8	8	8	8	WASHER, LOCK #BEXT TOOTH 9008072 18
-	-	1	-	-	M972 TO DUAL W077 CABLE D-IA-700842300 17
4	4	-	4	4	SCR. PHL PAN HD 10-32 x 3/8 LG 9006071 16
1	1	-	1	1	CLAMP, STRAIN RELIEF C-IA-741163300 15
1	1	-	1	1	STRAIN RELIEF C-IA-741163300 14
4	4	4	4	4	SCR PHL PAN HD #8-32-1 LG 9006043-1 13
8	8	-	12	12	SCR PHL PAN HD #10-32-5/8 LG 9006074-1 12
8	8	-	12	12	NUT, TINNEMAN #10-32 9007786 11
-	4	-	REF REF	REF	I/O CABLE (BC08R)(NOTE 2) C-VA-BC08R-0-0 10
2	2	-	1	1	I/O CABLE ASSY (BC08S) C-IA-BC08S-15-0 9
-	-	-	1	1	POWER HARNESS D-IA-7008493-1-0 8
1	1	1	1	1	DHII OPTION HARNESS D-IA-7008561-0-0 7
-	-	-	1	1	GLASS ASSY C-IA-7008456-0-0 6
-	-	-	1	-	POWER SUPPLY (NOTE 8) D-UA-H758-B-0 5
-	-	-	1	-	POWER SUPPLY (NOTE 8) D-UA-H758-A-0 4
1	1	1	1	1	WIRED ASSY (DHII) D-AD-7009180-0-0 3
REF REF	REF REF	REF REF	REF REF	REF REF	MOUNTING BOX ASSY D-UA-B411-FC 2
REF REF	REF REF	REF REF	REF REF	REF REF	H960 CABINET D-UA-H960-CD-0 1

FIRST USED ON OPTOMAG MODEL		QTY.	DESCRIPTION	PART NO.	ITEM NO.
PDP II		PARTS LIST			
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES		DATE 2-12-73	EQUIPMENT CORPORATION SARASOTA, FLORIDA 34237		
DECIMALS	ANGLES	DATE 2-12-73	TITLE BASIC ASSY DH11 IN H960		
.XXX = .005	± 0° 30'	DATE 2-8-73			
.XX = .02		DATE 2-22-73			
.X = .1		DATE 2-23-73			
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY					
MATERIAL		NEXT HIGHER ASSY.		SIZE CODE	NUMBER
B-DD-DH11-φ		B-DD-DH11-φ		DUA	DH11-φ-φ
FINISH		SCALE		REV.	
		SHEET OF 14		F	
		DIST.			

8

7

6

5

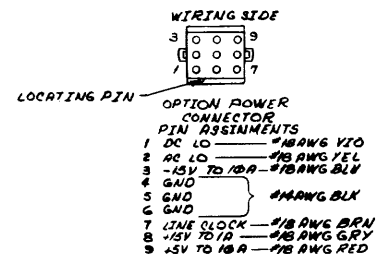
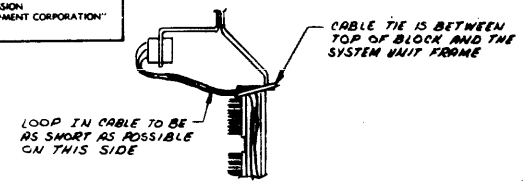
4

3

2

1

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POWER DISTRIBUTION (OLD VERSION)

NOTES:

1. THIS PRINT SHOWS HARNESS ARRANGMENTS FOR 11/40 AND 11/35 WITH SERIAL NO. GREATER THAN 6000 OR H960-D,E WITH SERIAL NO. GREATER THAN 7000.
2. OPTION BACKPLANES AND HARNESSES REPRESENT TYPICAL INSTALLATION. DHII USES PWR DIST HARNESS D-IA-7009561 WHEN USED IN THESE BOXES (SEE NOTE 1).
3. WHEN FOUR TERMINALS APPEAR IN TOP ROW, ORDER IS +5, +15, DC LO, AC LO. USE 7009561 REV B (WITH +15 GRN WIRE).

POWER SUPPORT PLATE D-MD-7403678-0-0 (OLD VERSION)

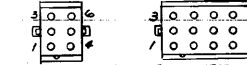
TOP ROW PWR DIST HD D-IA-7009561 (OLD VERSION)

OPTION PWR DIST HARNESS (SEE NOTE 2)

NOTE 3

POWER HARNESS E-IA-7008759-0-0 (OLD VERSION)

WIRING SIDE

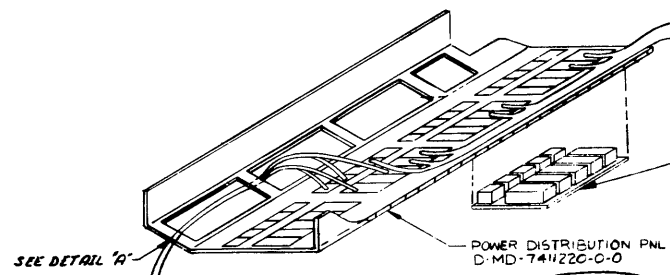


OPTION POWER CONNECTORS PIN ASSIGNMENTS

- | | | |
|----------------------------|----------------------|-----------------------|
| 1 LO GND - #18 AWG BLK | 1 +5V - #18 AWG RED | 9 GND - #18 AWG BLK |
| 2 LINE CLOCK - #18 AWG BRN | 2 +15V - #18 AWG GRN | 10 SPARE #2 |
| 3 DC LO 1 - #18 AWG VIO | 3 +5V - #18 AWG GRN | 11 GND - #18 AWG BLK |
| 4 AC LO 1 - #18 AWG YEL | 4 +5V - #18 AWG RED | 12 SPARE #3 |
| 5 SPARE #4 | 5 GND - #18 AWG BLK | 13 -15V - #18 AWG BLU |
| 6 SPARE #5 | 6 SPARE #1 | 14 -5V - #18 AWG BRN |
| | 7 GND - #18 AWG BLK | 15 SPARE #3 |
| | 8 GND - #18 AWG BLK | |

ADHESIVE TIE MOUNTS & CABLE TIES

ROUTE CABLE BETWEEN OPTION BACKPLANES AS CLOSE TO CHASSIS AS POSSIBLE.



POWER DISTRIBUTION PNL D-MD-7411226-0-0

NOTE 3

POWER HARNESS 7009566

POWER DISTRIBUTION (NEW VERSION)

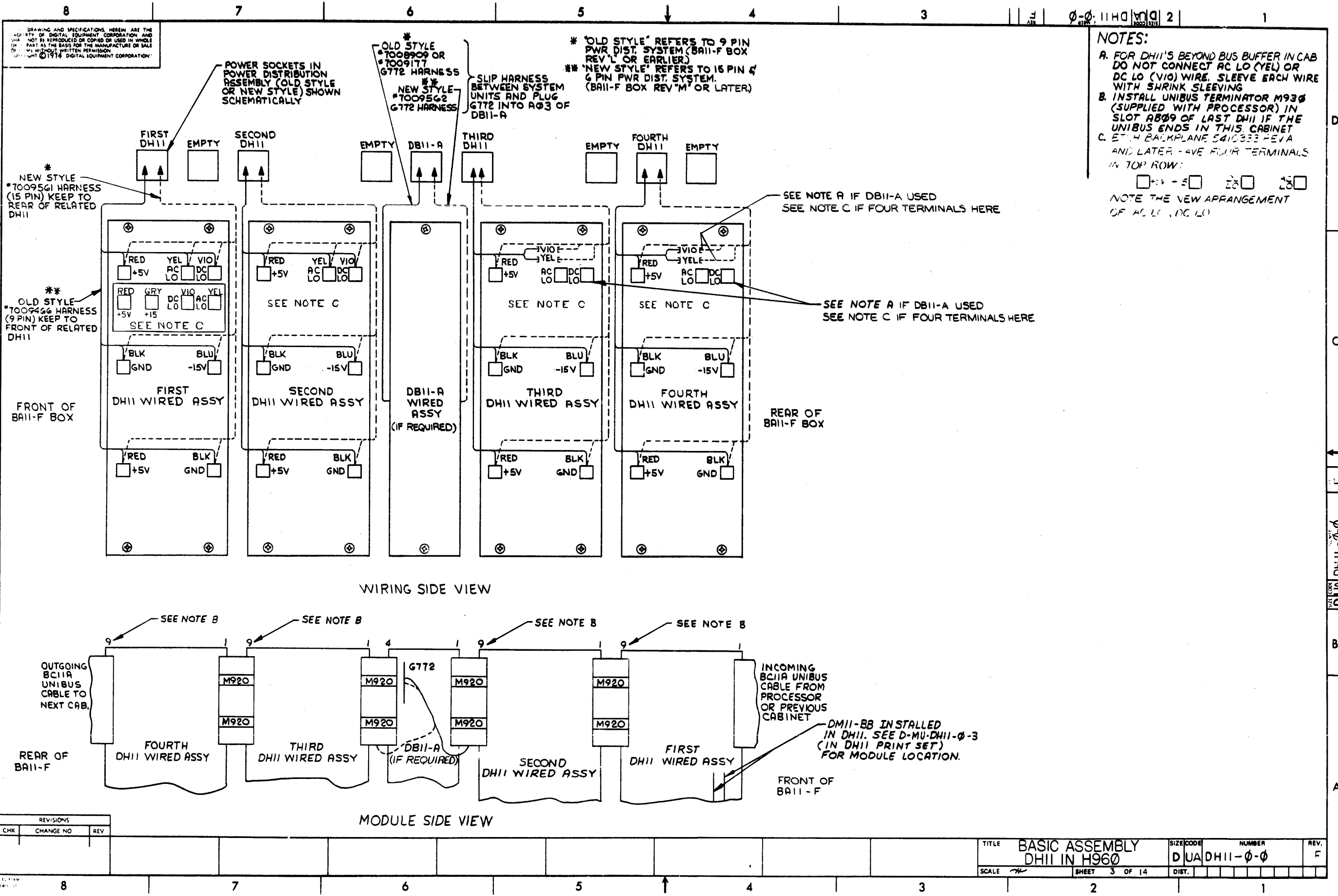
TO LINE 1 SWITCHED OUTLET OF POWER CONTROL

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
PDPII				
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES	DRN. R. PUDELKO 2-12-73	DATE 2-12-73	PARTS LIST	
TOLERANCES	CHK'D. K. GLEZEN 2-22-73	DATE 2-22-73	digital EQUIPMENT CORPORATION MAYFIELD MASSACHUSETTS	
DECIMALS ANGLES	ENG. J. MCNAMARA 2-22-73	DATE 2-22-73	TITLE BASIC ASSY	
.XXX = .005 .XX = .02 .X = .1	PROJ. ENG. J. MCNAMARA 2-22-73	DATE 2-22-73	DHII IN H960	
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY 1	PROD. J. BORENSTEIN 2-23-73	DATE 2-23-73	NEXT HIGHER ASSY.	
MATERIAL			B-DD-DHII-0	
FINISH			SCALE	
			SHEET 2 OF 14	
			DST.	

DATE CODE DUA DHII-0-0

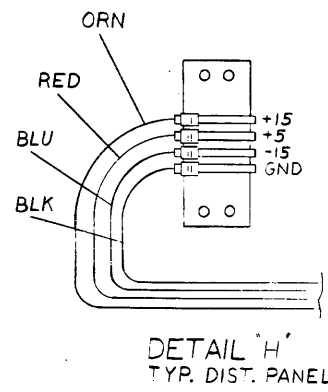
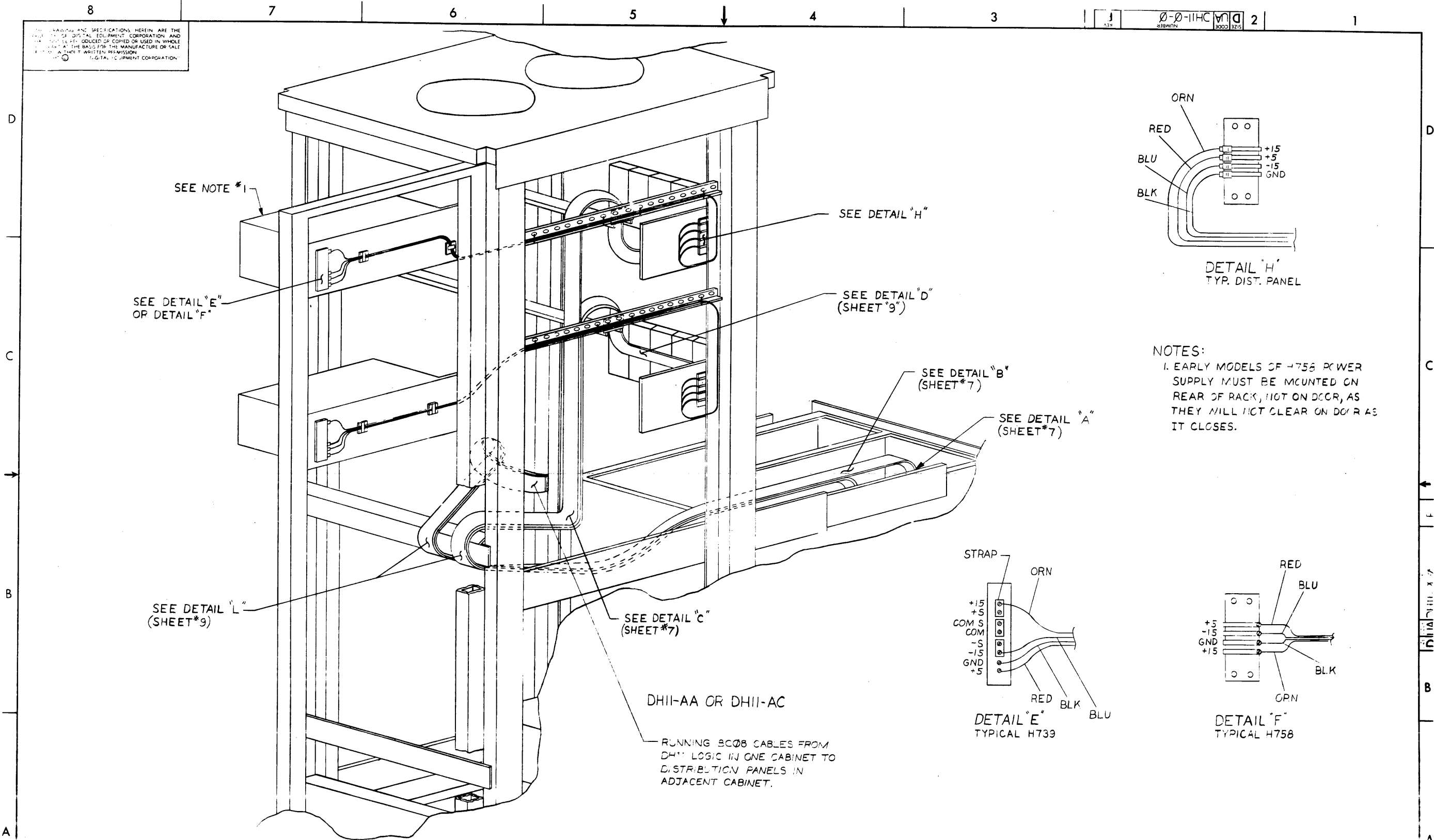
B

A

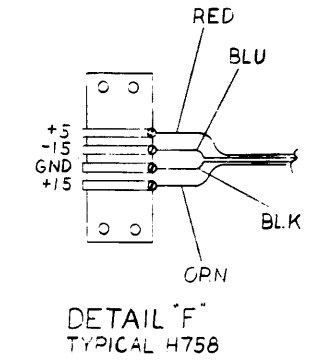
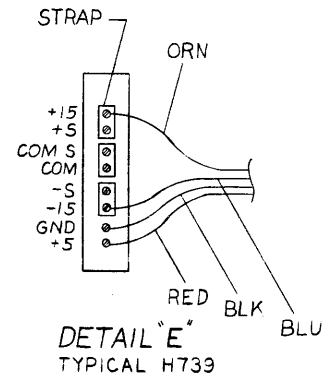


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Ø-Ø-11HC 2



NOTES:
1. EARLY MODELS OF H758 POWER SUPPLY MUST BE MOUNTED ON REAR OF RACK, NOT ON DOOR, AS THEY WILL NOT CLEAR ON DOOR AS IT CLOSSES.



REVISIONS		
CHK	CHANGE NO	REV

CONNECTION OF POWER SUPPLIES

DETAILS: E, F, H

APPLICATION: DH11-AA, -AC

TITLE BASIC ASSEMBLY
DH11 IN H960

SIZE CODE NUMBER
DUA DH11-Ø-Ø

REV.
F

SCALE NCNE

SHEET 4 OF 14

DIST.

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NOTES:

1. EARLY MODELS OF H758 POWER SUPPLY MUST BE MOUNTED ON REAR OF RACK, NOT ON DOOR, AS THEY WILL NOT CLEAR ON DOOR AS IT CLOSURES.

MODULE
RETAINING
BAR

NOTE: CABLES
CAN NOT BE
TIED TO OR
HANG IN THIS
AREA OF THE
LEFT REAR
SIDE MOUNTING
RAIL. (THEY
WILL BE
PINCHED BY
THE H758
POWER SUPPLY)

H758 P.S. CONN.

H739 P.S. CONN.
(MUST BE INSULATED)

NOTE 1

2ND

2ND

1ST

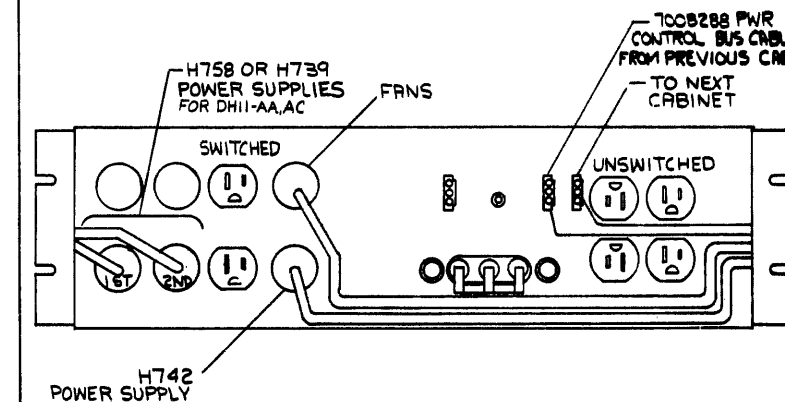
1ST

H742
P.S.

GROMMET
THIS
EDGE

M

M



VIEW M-M

POWER MAINS CONNECTIONS

DETAILS: NONE

APPLICATION: DH11-AA, AC

TITLE BASIC ASSEMBLY
DH11 IN H960

SIZE/CODE
DUA

NUMBER
DH11-0-0

REV.
F

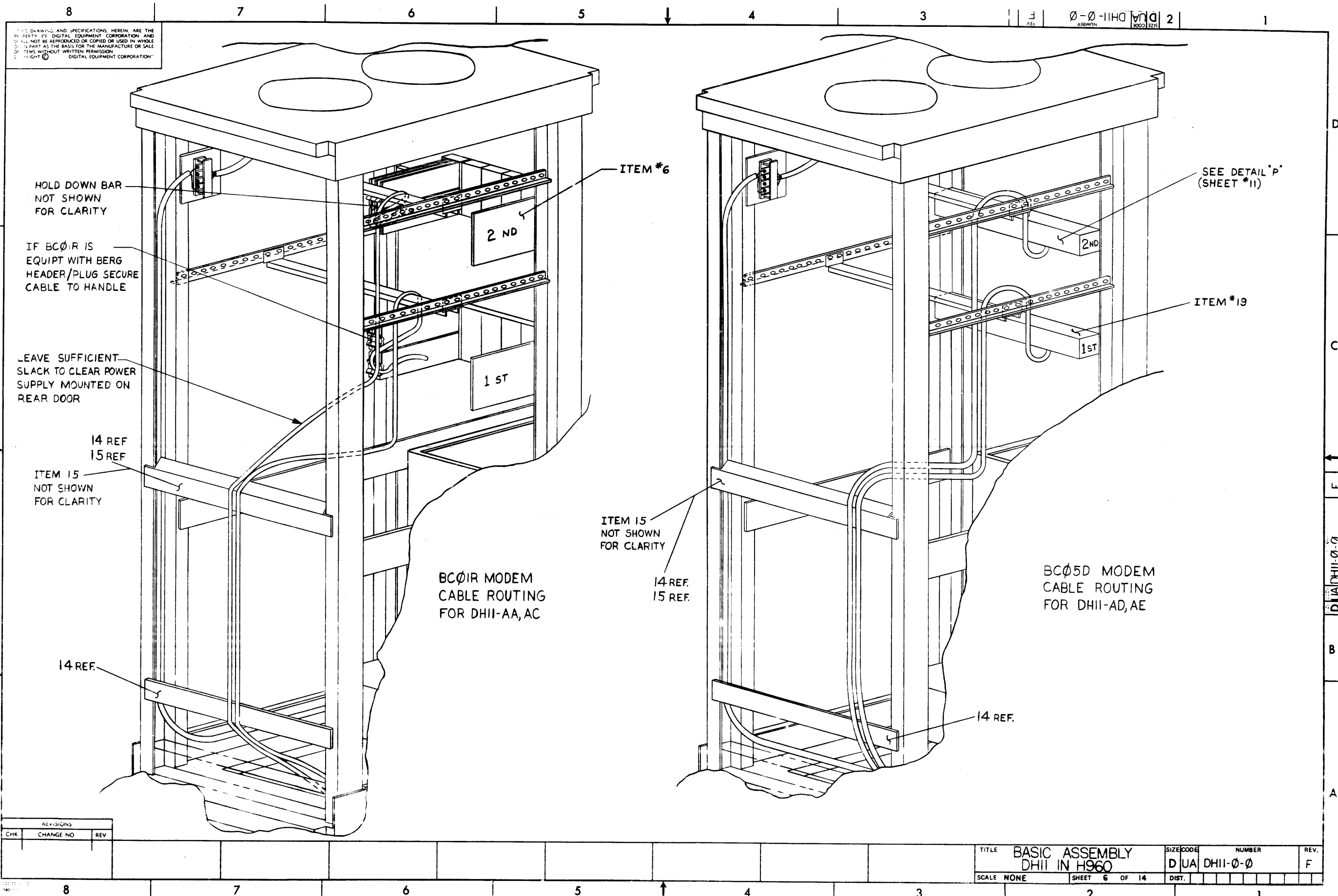
SCALE NONE

SHEET 5 OF 14

DIST.

REVISIONS		
CHK	CHANGE NO.	REV.

DEC 1978 NO
DHD 137

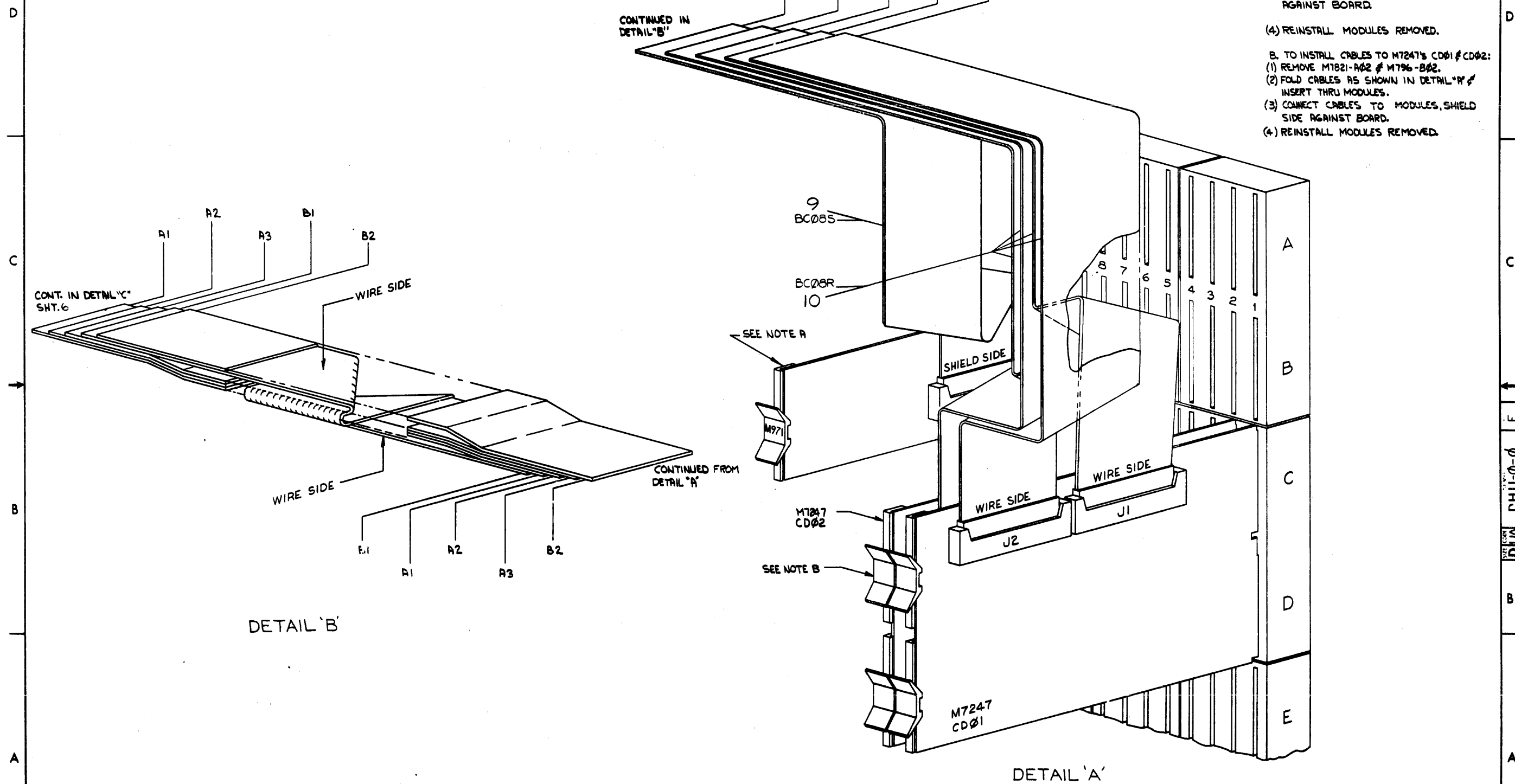


A. TO INSTALL CABLE TO M971-B07:

- (1) REMOVE G7360-A07 AND M7821-A06.
- (2) FOLD CABLE AS SHOWN IN DETAIL "A" & INSERT DOWN THRU MODULES.
- (3) CONNECT CABLE TO MODULE WIRE SIDE AGAINST BOARD.

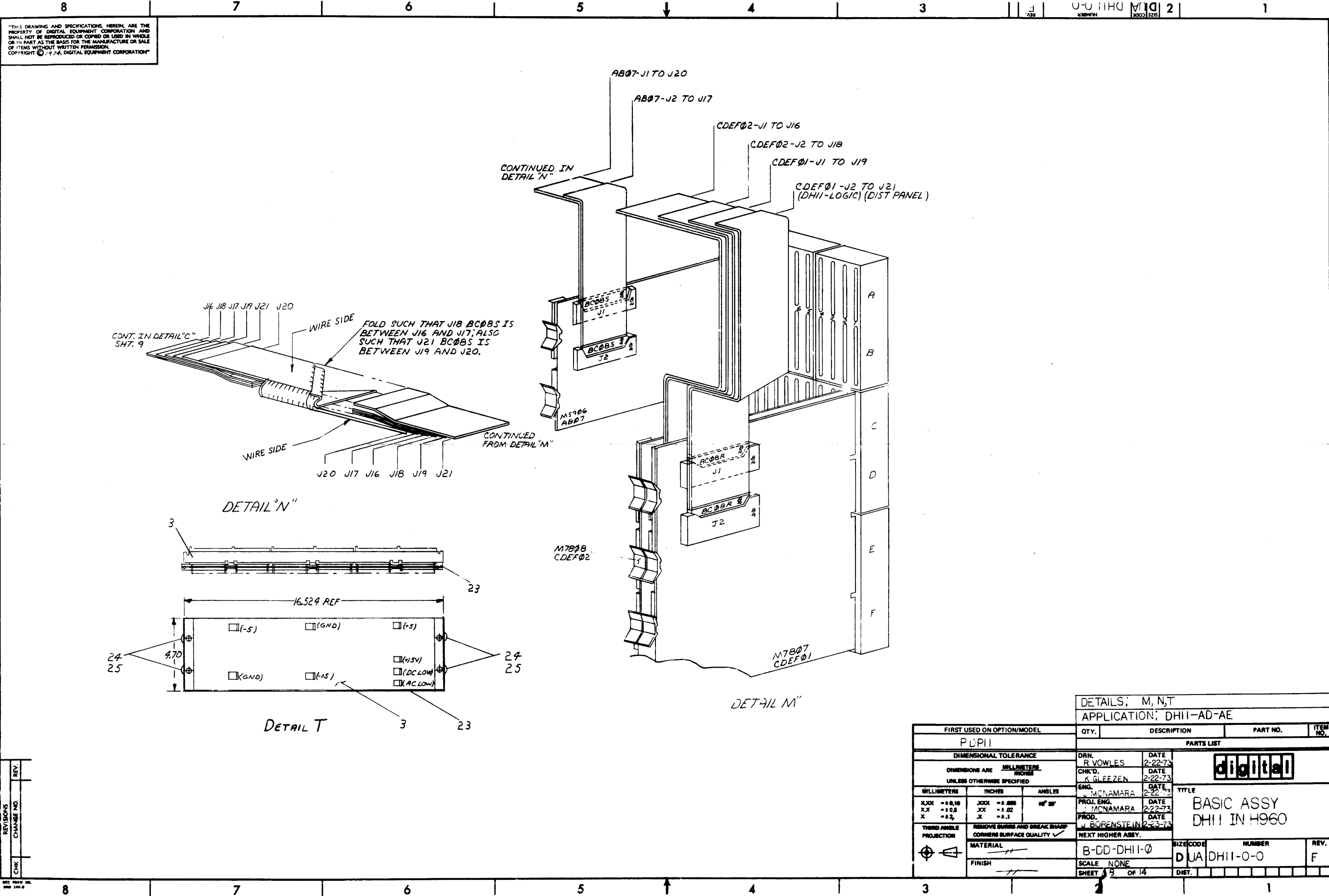
(4) REINSTALL MODULES REMOVED.

- (1) REMOVE M1821-A02 & M1796-B02.
- (2) FOLD CABLES AS SHOWN IN DETAIL "A" & INSERT THRU MODULES.
- (3) CONNECT CABLES TO MODULES, SHIELD SIDE AGAINST BOARD.
- (4) REINSTALL MODULES REMOVED.



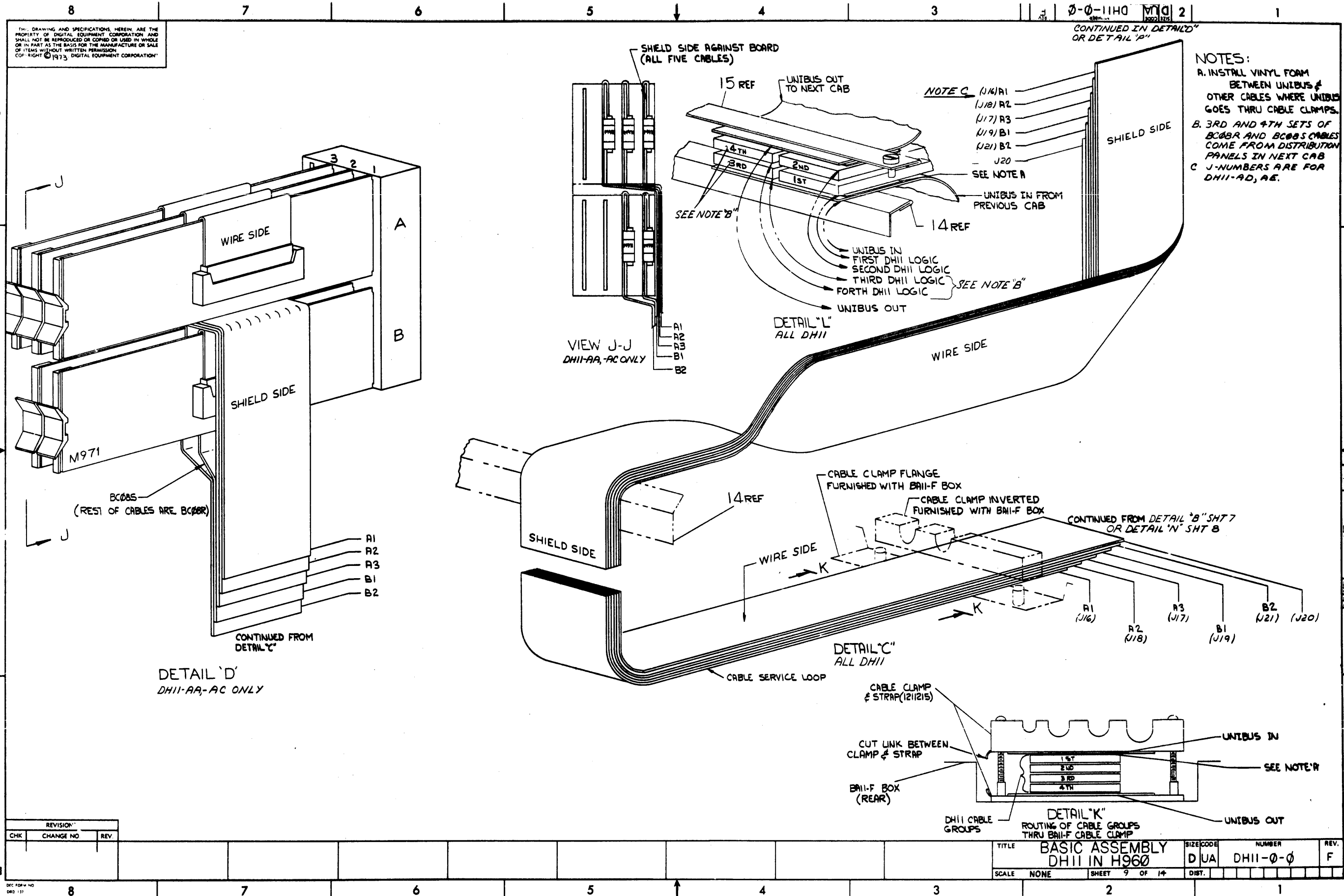
REVISIONS		
CHK	CHANGE NO.	REV.

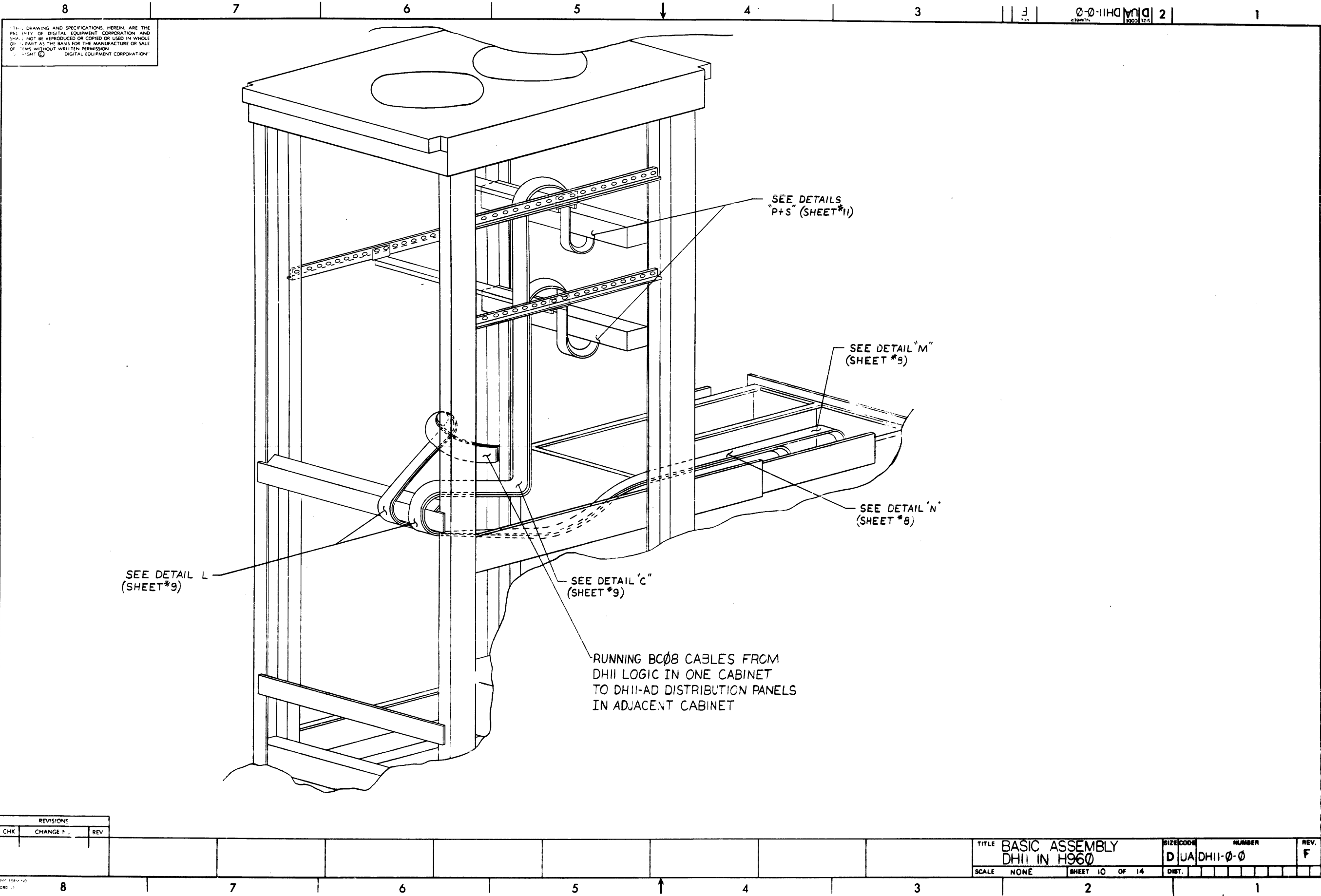
DETAILS: A, B												
APPLICATION: DH11-AA, AC												
TITLE		BASIC ASSEMBLY DH11 IN H960				SIZE CODE		NUMBER		REF		
		DUA				DH11-0-0					F	
SCALE		NONE		SHEET		7 OF 14		DWT.				



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DETAILS: M, N, T			
APPLICATION: DH11-AD-AE			
QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
FIRST USED ON OPTION/MODEL			
PUPII			
DIMENSIONAL TOLERANCE			
DIMENSIONS ARE MILLIMETERS UNLESS OTHERWISE SPECIFIED			
MILLIMETERS	INCHES	ANGLES	
XXX ±0.10	XXX ±0.005	90° 30'	
XX ±0.5	XX ±0.02		
X ±0.2	X ±0.1		
THIRD ANGLE PROJECTION			
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY			
MATERIAL			
FINISH			
NEXT HIGHER ASSY.			
B-DD-DH11-0			
SCALE NONE			
SHEET 9 OF 14			
DIST.			
REV.			
F			





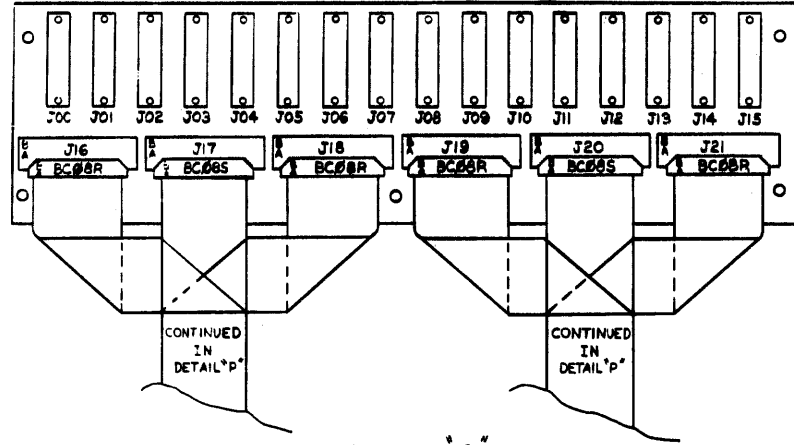
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0-0-11H0M1D 2

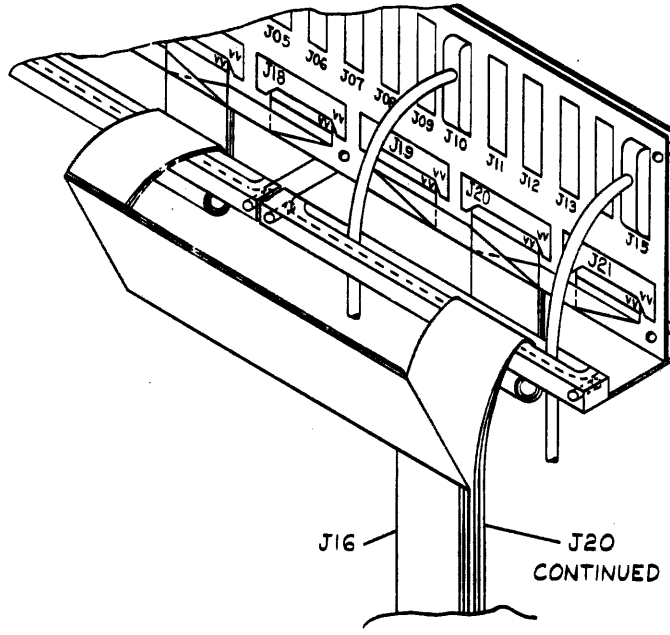
REVISIONS		
CHK	CHANGE	REV

TITLE		SIZE CODE		NUMBER		REV.
BASIC ASSEMBLY DHII IN H960		DUA		DHII-0-0		F
SCALE	NONE	SHEET 10 OF 14		DIST.		

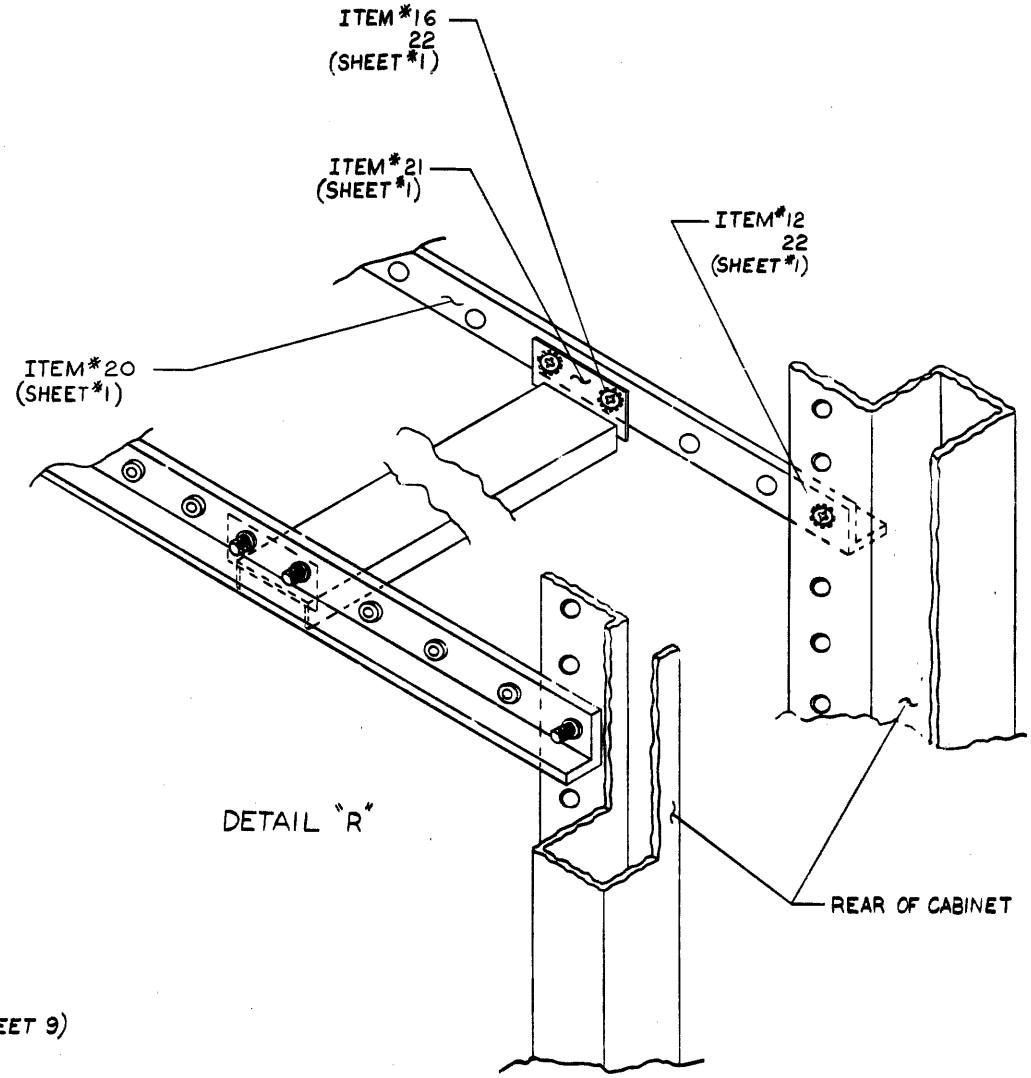
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DETAIL 'S'



DETAIL 'P'



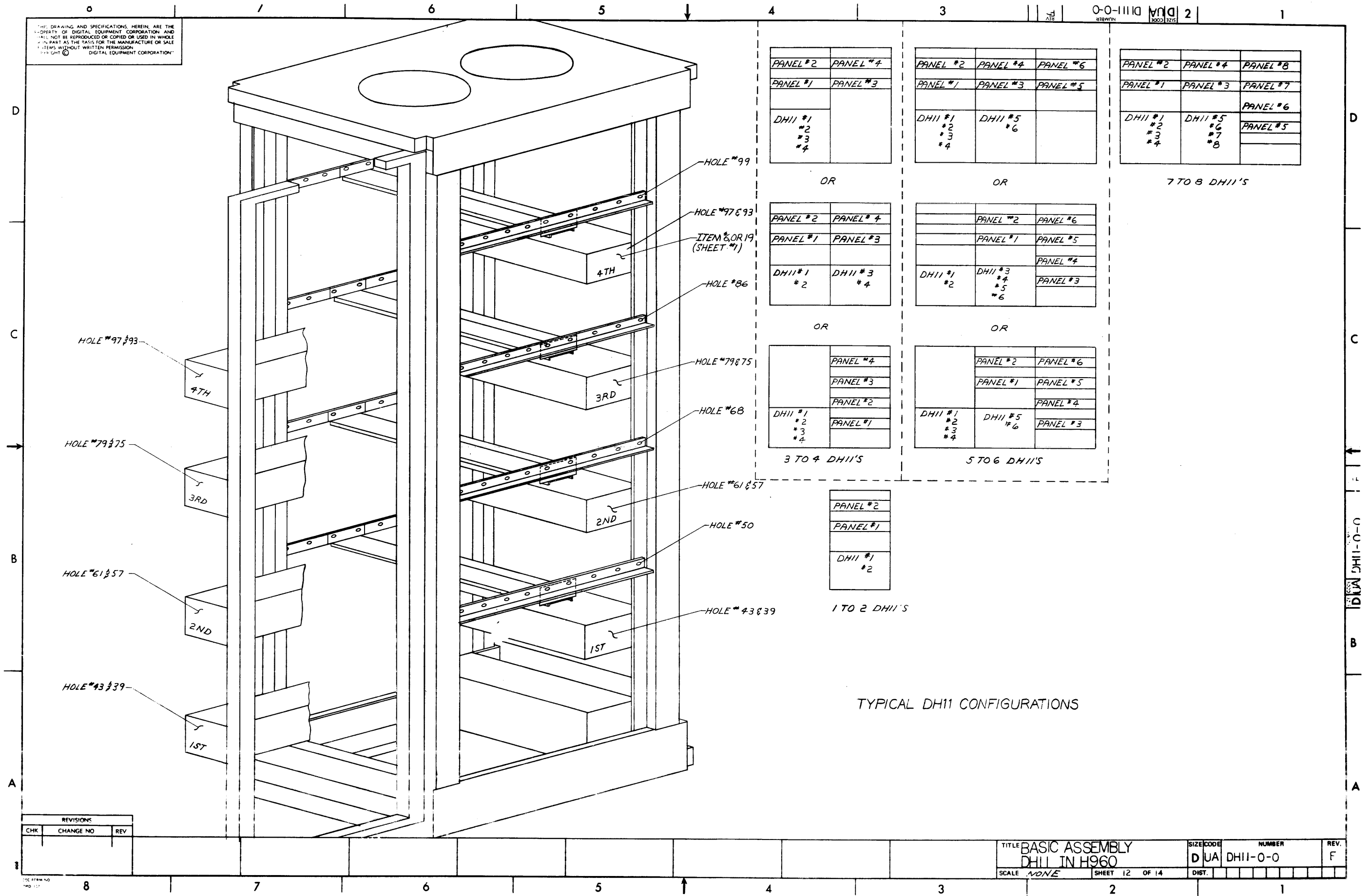
DETAIL 'R'

FIRST USED ON OPTION/MODEL		QTY.	DESCRIPTION	PART NO.
PDPII				
PARTS LIST				
DIMENSIONAL TOLERANCE		DRN.	DATE	digital
DIMENSIONS ARE		R. VOWLES	2-22-73	
UNLESS OTHERWISE SPECIFIED		CHK'D.	DATE	
		K. GLEZEN	2-22-73	
		ENG.	DATE	BASIC ASSEMBLY DH11 IN H960
		J. MCNAMARA	2-22-73	
		PROJ. ENG.	DATE	
		J. MCNAMARA	2-22-73	
		PROD.	DATE	NEXT HIGHER ASSY.
		J. BORENSTEIN	2-23-73	
THIRD ANGLE PROJECTION		REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY		
MATERIAL		B-DD-DH11-0		
FINISH		SCALE NONE		
		SHEET 11 OF 14		

REV.	CHANGE NO.
1	1

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 DIGITAL EQUIPMENT CORPORATION

0-0-11110 2
 3000 1215



PANEL #2	PANEL #4
PANEL #1	PANEL #3
DH11 #1 #2 #3 #4	

OR

PANEL #2	PANEL #4
PANEL #1	PANEL #3
DH11 #1 #2	DH11 #3 #4

OR

	PANEL #4
	PANEL #3
	PANEL #2
DH11 #1 #2 #3 #4	PANEL #1

3 TO 4 DH11'S

PANEL #2	PANEL #4	PANEL #6
PANEL #1	PANEL #3	PANEL #5
DH11 #1 #2 #3 #4	DH11 #5 #6	

OR

	PANEL #2	PANEL #6
	PANEL #1	PANEL #5
		PANEL #4
DH11 #1 #2	DH11 #3 #4 #5 #6	PANEL #3

OR

	PANEL #2	PANEL #6
	PANEL #1	PANEL #5
		PANEL #4
DH11 #1 #2 #3 #4	DH11 #5 #6	PANEL #3

5 TO 6 DH11'S

PANEL #2	PANEL #4	PANEL #8
PANEL #1	PANEL #3	PANEL #7
DH11 #1 #2 #3 #4	DH11 #5 #6 #7 #8	PANEL #6 PANEL #5

7 TO 8 DH11'S

PANEL #2
PANEL #1
DH11 #1 #2

1 TO 2 DH11'S

TYPICAL DH11 CONFIGURATIONS

REVISIONS		
CHK	CHANGE NO	REV

TITLE		SIZE CODE	NUMBER	REV.
BASIC ASSEMBLY		DUA	DH11-0-0	F
DH11 IN H960				
SCALE		SHEET	OF	
NONE		12	14	
		DIST.		

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	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
	M971	M971	M971	M594	M594																	M594	M594	
	CABLE DATA SET CNTRL LINES ΦΦ THRU Φ3	CABLE DATA SET CNTRL LINES ΦΦ THRU Φ7	CABLE DATA SET CNTRL LINES ΦΦ THRU Φ11	** LINE 8 THRU 11 "X" SLOT	** LINE 12 THRU 15 "X" SLOT	LINE 0 'A' SLOT	LINE 1 'A' SLOT	LINE 2 'A' SLOT	LINE 3 'A' SLOT	LINE 4 'A' SLOT	LINE 5 'A' SLOT	LINE 6 'A' SLOT	LINE 7 'A' SLOT	LINE 8 'A' SLOT	LINE 9 'A' SLOT	LINE 10 'A' SLOT	LINE 11 'A' SLOT	LINE 12 'A' SLOT	LINE 13 'A' SLOT	LINE 14 'A' SLOT	LINE 15 'A' SLOT	*** LINE 8 THRU 11 "Y" SLOT	*** LINE 12 THRU 15 "Y" SLOT	
	M971	M971	M974	M594	M594																	M594	M594	
	•• CABLE DATA LINES ΦΦ THRU 15	CABLE DATA SET CNTRL LINES ΦΦ THRU 15	△△ LOOP BACK TEST LINES Φ THRU 15	** LINE 0 THRU 3 "X" SLOT	** LINE 4 THRU 7 "X" SLOT	LINE 0 'B' SLOT	LINE 1 'B' SLOT	LINE 2 'B' SLOT	LINE 3 'B' SLOT	LINE 4 'B' SLOT	LINE 5 'B' SLOT	LINE 6 'B' SLOT	LINE 7 'B' SLOT	LINE 8 'B' SLOT	LINE 9 'B' SLOT	LINE 10 'B' SLOT	LINE 11 'B' SLOT	LINE 12 'B' SLOT	LINE 13 'B' SLOT	LINE 14 'B' SLOT	LINE 15 'B' SLOT	*** LINE 0 THRU 3 "Y" SLOT	*** LINE 4 THRU 7 "Y" SLOT	

WIRING SIDE VIEW OF DISTRIBUTION PANEL (MODULE UTILIZATION)

- USED WHEN DM11-BB IS IMPLEMENTED
- DATA CABLE FROM DM11-A LOGIC
- ▲▲ LOOP BACK TEST CARD FOR DIAGNOSTICS
REMOVE FOR NORMAL OPERATION
- ** EIA LEVEL CONVERSION FOR DATA LEADS ONLY (SEE CHART)
- *** ACTIVE 20mA LEVEL CONVERSION (SEE CHART)

USAGE OF LINE		'11 OPTION	"A" SLOT	"B" SLOT	"X" SLOT	"Y" SLOT
Ø	LOOP BACK TEST	_____	EMPTY	DONT CARE	EMPTY	EMPTY
1	20mA ACTIVE LOCAL	_____	DM11-DA	M973	EMPTY	M596C or M596
2	EIA LOCAL (DATA ONLY)	_____	DM11-DB	W404	BC01R	M594
3	EIA FULL CONTROL	_____	DF11-A, DM11-DC	M594	BC01R	EMPTY
4	IN GRAL MODEM (ANS ONLY)	_____	DF11-BB	M587	M587	EMPTY
5	FLOATING 20mA LOCAL	_____	DF11-K	M598	M973	EMPTY
6	GENERAL (ASYNC) DF11 SLOT	_____	NONE	DF11 LEVEL CONVERTER	DF11 CABLE	EMPTY

NOTES:

M974 IN B03. ALL LINES (Ø THRU 15) AFFECTED.

ALL 4 SLOTS IN EACH GROUP (0-3, 4-7, 8-11, 12-15) MUST BE IN THIS MODE, IF ANY ARE.

ALL 4 SLOTS IN EACH GROUP (0-3, 4-7, 8-11, 12-15) MUST BE IN THIS MODE, IF ANY ARE.

DMII-DC = 4-M594, 4-BCØIR. DFII-A =
1-M594, 1-BCØIR

M587 IS DOUBLE HEIGHT CARD.

REVISIONS		
CHK	CHANGE NO	REV

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OCTAL TO JUMPER CONVERSIONS

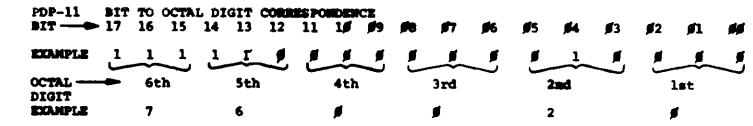
M7821									
VECTORS					IN=1 OUT=0				
18	7	6	5	4	3	2	1	0	
30#	OUT	IN	IN	OUT	OUT	OUT	OUT		
30#	OUT	IN	IN	OUT	OUT	OUT	IN		
31#	OUT	IN	IN	OUT	OUT	IN	OUT		
31#	OUT	IN	IN	OUT	OUT	IN	IN		
32#	OUT	IN	IN	OUT	IN	OUT	OUT		
32#	OUT	IN	IN	OUT	IN	OUT	IN		
33#	OUT	IN	IN	OUT	IN	IN	OUT		
33#	OUT	IN	IN	OUT	IN	IN	IN		
34#	OUT	IN	IN	IN	OUT	OUT	*		
35#	OUT	IN	IN	IN	OUT	IN	*		
36#	OUT	IN	IN	IN	IN	OUT	*		
37#	OUT	IN	IN	IN	IN	IN	*		
40#	IN	OUT	OUT	OUT	OUT	IN	*		
41#	IN	OUT	OUT	OUT	OUT	IN	*		
42#	IN	OUT	OUT	OUT	IN	OUT	*		
43#	IN	OUT	OUT	OUT	IN	IN	*		

* ALWAYS IN FOR M7821 IN LOCATION A#6

M7277									
DH11-A ADDRESS OUT=1 IN=0					M195				
BITS 8,9,10,11,12 ARE ALL IN					BITS 6,8, & 12 ARE ALL OUT				
					BITS 7,9,10, & 11 ARE ALL IN				
76#	8#	7	6	5	77#	50#	5	4	3
IN	IN	IN	OUT		IN	IN	IN	IN	OUT
IN	IN	IN	OUT		51#	IN	IN	IN	OUT
IN	IN	OUT	OUT		52#	IN	OUT	IN	
IN	OUT	IN	IN		53#	IN	OUT	OUT	
IN	OUT	IN	OUT		54#	OUT	IN	IN	
IN	OUT	IN	IN		55#	OUT	IN	OUT	
IN	OUT	OUT	OUT		56#	OUT	OUT	IN	
OUT	IN	IN	IN		57#	OUT	OUT	OUT	

M596 OR M5960									
JUMPER FOR MECHANICAL CONTACT NOISE FILTERING REMOVE FOR SPEEDS GREATER THAN 150 BAUD. (CAN ALSO BE REMOVED AT LOWER SPEEDS IF NOISE IS NOT A PROBLEM)									
LINES	8,4,8,12*	M596	M5960						
1,5,9,13	W2	W4	W2	{ IN FOR FILTERING OUT FOR HIGH SPEEDS					
2,6,10,14	W1	W3	W1						
3,7,11,15	W3	W1	W3						

*OR WHEN USED DP11-F



NOTE: I/O DEVICE ADDRESS IN 11 LITERATURE ARE VARIOUSLY GIVEN AS 76# THRU 77# 777 AND AS 16# THRU 177 777. THESE ARE EQUIVALENT IN MACHINES WITHOUT MEMORY MANAGEMENT. WHEN EVER BITS 15,14 AND 13 ARE ALL "1" (16x xxx OR 17x xxx) THE PROCESSOR ALSO MAKES BITS 17 AND 16 "1" (76x xxx OR 77x xxx). [ON MACHINES WITH MEMORY MANAGEMENT (NOT STANDARD DEC) I/O DEVICE ADDRESSES ARE IN PHYSICAL MEMORY AT 76# THRU 777 777. THEY ARE ONLY AVAILABLE TO A PROGRAM IF SOME VIRTUAL ADDRESS AREA IS MAPPED INTO THIS PHYSICAL AREA.]

DH11 JUMPERS AND MODIFICATIONS.

G736# LOCATION A#7 OR M5906 LOCATION AB07 (DH11 AD,AE) OPTIONS BR LEVEL SELECT BOARD BOTH BR PLUGS SHOULD BE 54#8778 (LEVEL #5) (AS SUPPLIED STANDARD)

M7821 LOCATION A#6 VECTOR LOCATION W2 BIT 2 IN (ALWAYS) W3 BIT 3 IN FOR "1" W4 BIT 4 IN FOR "1" W5 BIT 5 OUT FOR "0" W6 BIT 6 SEE TABLE W7 BIT 7 OF DH11 VECTORS W8 BIT 8 W9 MPR SPEED UP: IN EXCEPT WHEN 11/15 (K11) OR 11/2# (K11) PROCESSOR WITHOUT K11 OPTION IS USED. THEN OUT.

M7821 LOCATION A#2 MPR CONTROL ALL JUMPERS ARE "DON'T CARE" ON THIS MODULE

DH11-AD MODEM CONTROL ADDRESS AND VECTORS

M7807 LOCATION C,D,E,F#H VECTOR LOCATION W2 BIT 2 IN FOR "1" W3 BIT 3 OUT FOR "0" W4 BIT 4 SEE TABLE W5 BIT 5 OF DH11-BB VECTORS W6 BIT 6 W7 BIT 7 W8 BIT 8 W9 BIT 9 W10 BIT 10 W11 BIT 11 W12 BIT 12

ADDRESS LOCATION W15 BIT 3 W16 BIT 4 W17 BIT 5 W18 BIT 6 W19 BIT 7 W20 BIT 8 W21 BIT 9 W22 BIT 10 W23 BIT 11 W24 BIT 12

M7277 LOCATION ABCDEF#4 REGISTER ADDRESSES

"4" BIT 4
"5" BIT 5
"6" BIT 6
"7" BIT 7
"8" BIT 8
"9" BIT 9
"10" BIT 10
"11" BIT 11
"12" BIT 12

OUT FOR "1" IN FOR "0" SEE TABLE OF DH11 ADDRESSES

M796 LOCATION B#2 UNIBUS MASTER CONTROL DATA STROBE LENGTH 40ns NOMINAL ADD 10# pF 5% MICA CAPACITOR DEC P.N. 10#16 ACROSS SPLIT LUGS NEAR FRONT OF BOARD

TAG MODULE WITH TAG WHICH SAYS "MODIFIED MODULE 10#pF ADDED FOR 40ns STROBE.

DH11-BB DATA SET-CONTROL (OR M7807 IN DH11-AD) LOCATED IN DH11-A

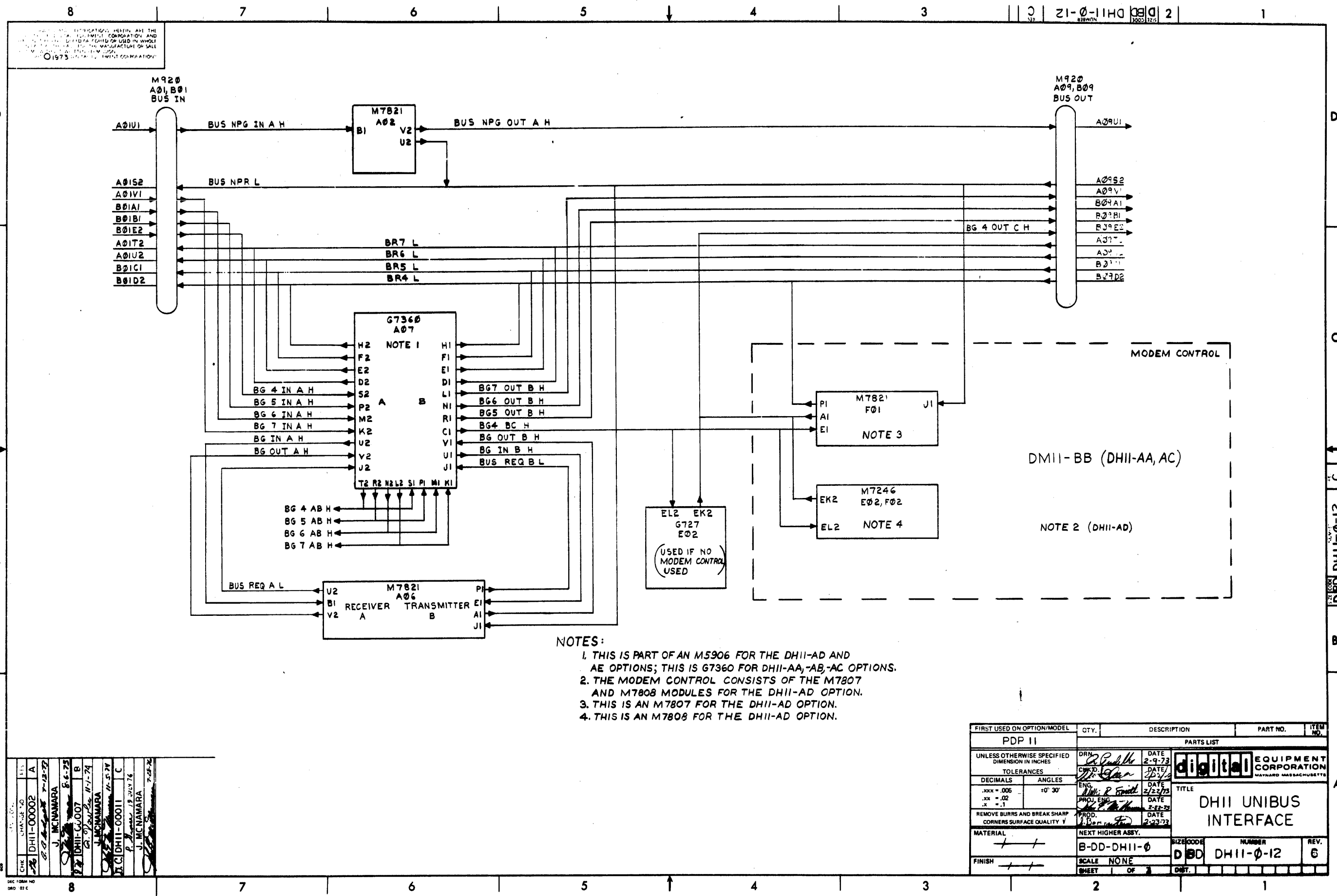
M195 LOCATION B#1

"3" BIT 3 IN FOR "0" OUT FOR "1" SEE TABLE OF DH11-BB ADDRESSES

"4" BIT 4
"5" BIT 5
"6" BIT 6 OUT
"7" BIT 7 IN
"8" BIT 8 OUT
"9" BIT 9 IN
"10" BIT 10 IN
"11" BIT 11 IN
"12" BIT 12 OUT

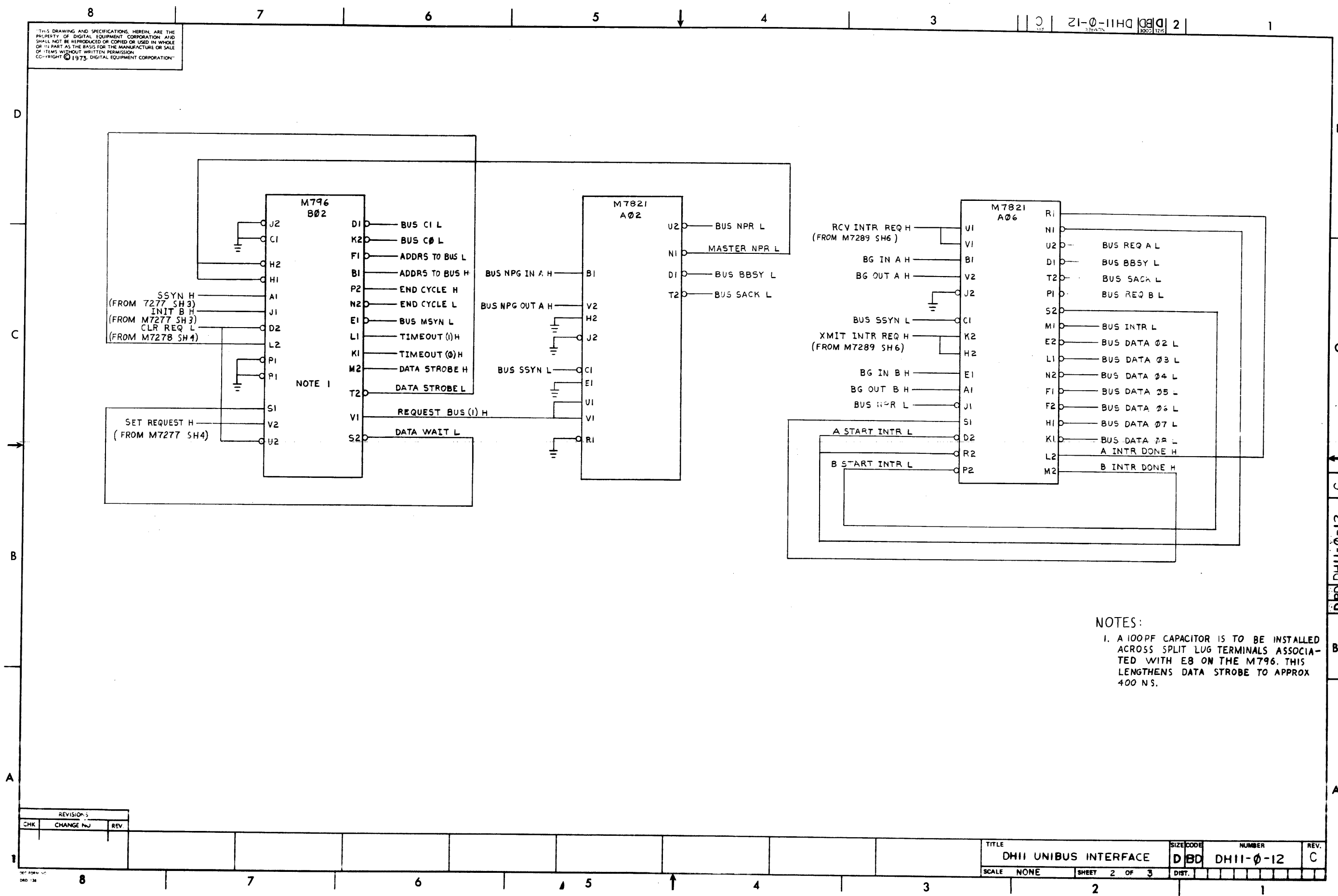
M7821 LOCATION F#1 VECTOR LOCATION W2 BIT 2 IN FOR "1" W3 BIT 3 OUT FOR "0" W4 BIT 4 SEE TABLE OF DH11-BB VECTORS W5 BIT 5 OUT W6 BIT 6 IN W7 BIT 7 IN W8 BIT 8 OUT W9 MPR SPEEDUP: IN EXCEPT WHEN 11/15 (K11) OR 11/2# (K11) PROCESSOR WITHOUT K11 OPTION IS USED. THEN OUT.

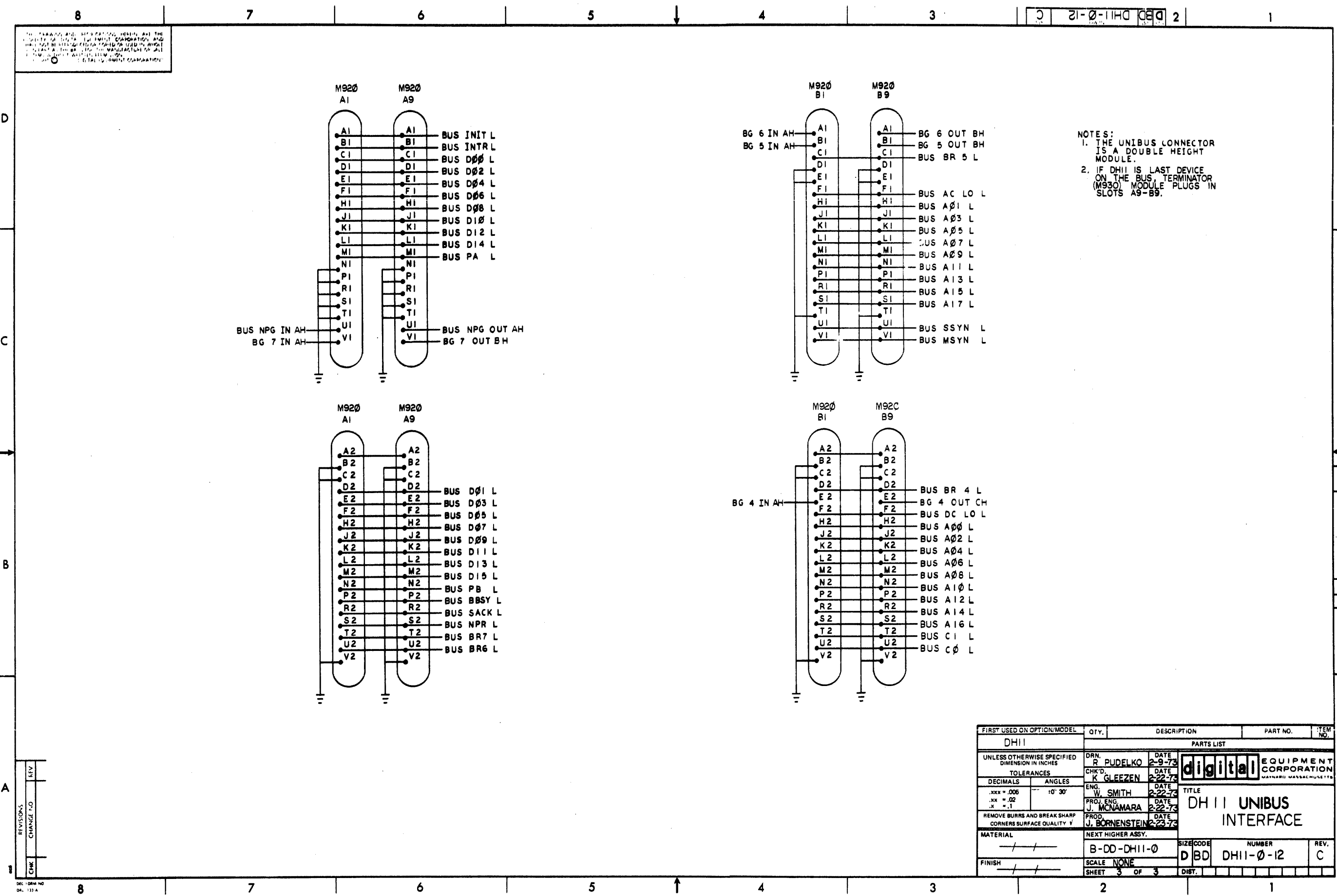
FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	REV. NO.
DP11				
PARTS LIST				
DIMENSIONAL TOLERANCE		DATE	2-12-73	
DIMENSIONS ARE MILLIMETERS UNLESS OTHERWISE SPECIFIED		CHK'D	K. GLEESON	
		DATE	2-22-73	
		ENG.	J. MCNAMARA	
		DATE	2-22-73	
		PROJ. ENG.	J. MCNAMARA	
		DATE	2-22-73	
		PROD.	J. BORENSTEIN	
		DATE	2-23-73	
		NEXT HIGHER ASBY.		
THIRD ANGLE PROJECTION	REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY	MATERIAL	B-DD-DH11-0	SCALE
		FINISH		14 OF 14
		SHEET	DIST.	



CHK	CHG	DATE	BY
1	1	1-12-77	J. MCNAMARA
2	1	2-6-75	J. MCNAMARA
3	1	2-12-77	J. MCNAMARA
4	1	2-12-77	J. MCNAMARA
5	1	2-12-77	J. MCNAMARA
6	1	2-12-77	J. MCNAMARA
7	1	2-12-77	J. MCNAMARA
8	1	2-12-77	J. MCNAMARA

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
PDP II				
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES	DRN	DATE	PARTS LIST	
TOLERANCES	CHK'D	DATE	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS	
DECIMALS	ENG	DATE	TITLE	
ANGLES	PROD. ENG.	DATE	DHII UNIBUS INTERFACE	
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY V	PROD.	DATE	SIZE CODE NUMBER REV.	
MATERIAL			B-DD-DHII-0 DDD DHII-0-12 6	
FINISH			SCALE NONE SHEET OF 3	





NOTES:
1. THE UNIBUS CONNECTOR IS A DOUBLE HEIGHT MODULE.
2. IF DH11 IS LAST DEVICE ON THE BUS, TERMINATOR (M930) MODULE PLUGS IN SLOTS A9-B9.

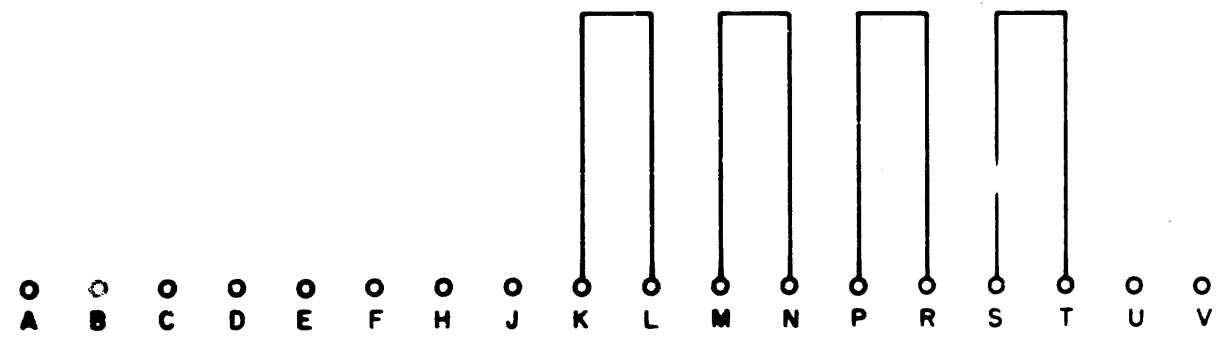
FIRST USED ON OPTION/MODEL		QTY.	DESCRIPTION	PART NO.	ITEM NO.
DH11					
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES		DRN. R. PUDELKO	DATE 2-9-73	 EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS	
TOLERANCES		CHK'D. K. GLEZEN	DATE 2-22-73		
DECIMALS	ANGLES	ENG. W. SMITH	DATE 2-22-73		
.XXX = .006	10° 30'	PROJ. ENG. J. MCNAMARA	DATE 2-22-73		
.XX = .02		PROD. J. BORNENSTEIN	DATE 2-23-73		
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY V				TITLE DH11 UNIBUS INTERFACE	
MATERIAL		NEXT HIGHER ASSY.			
/ /		B-DD-DH11-0			
FINISH		SCALE NONE			
/ /		SHEET 3 OF 3			
		DIST.		SIZE CODE D BD	
				NUMBER DH11-0-12	
				REV. C	

REV.	CHANGE NO.
1	

DEC 1081 NO
DAL 133 A



FOR TEST AND MAINTENANCE PURPOSES THE
NATURE AND SHOULD BE TREATED ACCORDINGLY
CORPORATION



REVISIONS	CHG	NO	REV		DRN	DATE	TRANSISTOR & DIODE CONVERSION CHART				digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS	TITLE GRANT CONTINUITY G727			
	CHG	NO	REV		CHK'D	DATE	DEC	EIA	DEC	EIA		SIZE	CODE	NUMBER	REV
	CHG	NO	REV		CHK'D	DATE						B	CS	G727-0-1	
	CHG	NO	REV		CHK'D	DATE									
				PROD.	DATE						PRINTED CIRCUIT REV A				

DEC FORM NO



5 PINK DIST. 324,434,435 3

DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS						
ENGINEERING SPECIFICATION					DATE 2-2-73	
TITLE DH11 Module Test Procedure						
REVISIONS						
REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	CHANGE PER ECO	DH11-00007	MCN/M/RAT	10/74	9th 7/10/74	11-5-74

ENG. <i>[Signature]</i>	2-5-73	APPD <i>[Signature]</i>	2-5-73	SIZE A	CODE SP	NUMBER DH11-0-11	REV <i>[Signature]</i>
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ENGINEERING SPECIFICATION		CONTINUATION SHEET	
TITLE DH11 Module Test Procedure			
I. Equipment Required A. A known good DH11 B. An oscilloscope - Techtronix 454 or better C. Diagnostics DZDHA-A-D through DZDHI-A-D D. PDP-11 E. Diagnostic DZDHK, H861 test connector, and 4 BC08R-12 cables. Note: Users of this procedure in the field should run all of the diagnostics, starting with DZDHA. If that fails, refer to the section of this procedure entitled "DZDHA Failures". After making any repairs necessary to get DZDHA to run, run diagnostic DZDHB. If it fails, refer to "DZDHB Failures" etc. II. Procedure A. Find the module to be tested in the list given in Section III below. Run the diagnostics as indicated, following the directions in the diagnostics for diagnostic start-up and switch settings. See "Note" on next page before starting. III. Modules of the DH11 and Their Functions A. M7277 Address Selection, Initialize, Control Strobe Generation, Instruction Generation, Data Source Selection, Current Address. Run DZDHA[*],B[*],C,D,E,G[*],H,I without iterations B. M7278 Byte Count Storage, Clear Buffer Active Register Logic, Transmitter Strobe, Buffer Active Register, Line Parameter Register, Break Control, Silo Status Register, All Gating to the Unibus, Silo Maintenance System. Run DZDHA[*],B[*],C,D,E,G[*],H,I without iterations C. M7279 First-In First-Out Buffer Memory (Silo), Silo Maintenance, Silo Fill Level, Receiver Interrupt. Run DZDHA,C[*],E,G[*],H,I WITH iterations D. M7280 Multiple UARTS Run DZDHA,B,C,D,E,G[*],H,I WITH iterations E. M7288 Speed Selection, Half-Duplex, Auto-Echo Run DZDHA,C,D[*],E,G[*],H,I without iterations			
SIZE CODE		NUMBER REV	
A		SP DH11-0-11 A	

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ENGINEERING SPECIFICATION		CONTINUATION SHEET			
TITLE	DH11 Module Test Procedure				
F. M7289 Auto-Echo System, Receiver Scanner, System Control Register, Half-D.plex Run DZDHA*,B,C,D,E,G,H,I without iterations G. M5906 EIA to TTL and TTL to EIA conversion for the 16 input and output data lines. The priority jumper plugs are also on this module. This module is hand tested on the 9305931 (M5906 tester) and needs no further checking. H. M7807 & M7808 These two modules are the modem control for the DH11-AD option 1. Connect four BC08R-12 cables to J1 & J2 on the M7807 and M7808 modules. Insert the other end of these cables into the H861 test connector. 2. Run DZDHK* with iterations. Run test group 0 and if any errors occur refer to the M7807 and M7808 circuit schematics. Also refer to the wire locator table at the end of this procedure. Run two passes without error. Note: The pages which follow outline the action of the various diagnostics and suggest signals to look for in the case of errors. The following pages are exact copies of the DH11 Option Test Procedure, Parts 4 & 5 and are labelled as such. Note: Tests marked with an asterisk (*), if run successfully, are a sufficient test of the module under test. The other diagnostics listed are convenient debugging aids should the module fail one of the * tests. Note: Each diagnostic should run at least one pass with iterations without error.					
		SIZE A	CODE SP	NUMBER DH11-0-11	REV A

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ENGINEERING SPECIFICATION		CONTINUATION SHEET																			
TITLE	DH11 TEST PROCEDURE																				
E. Summary of the Diagnostics 1. DZDHA DH11 Static Logic Test Running time: 1 sec. without iterations 35 sec with iterations Switch settings: <table border="1" style="width: 100%; border-collapse: collapse; margin-top: 10px;"> <thead> <tr> <th style="width: 20%; padding: 5px;"><u>Switch</u></th> <th style="padding: 5px;"><u>Action if set to one</u></th> </tr> </thead> <tbody> <tr><td style="text-align: center; padding: 5px;">15</td><td style="padding: 5px;">Halt on error</td></tr> <tr><td style="text-align: center; padding: 5px;">14</td><td style="padding: 5px;">Loop in the current test</td></tr> <tr><td style="text-align: center; padding: 5px;">13</td><td style="padding: 5px;">Inhibit error timeout</td></tr> <tr><td style="text-align: center; padding: 5px;">11</td><td style="padding: 5px;">Inhibit iterations</td></tr> <tr><td style="text-align: center; padding: 5px;">10</td><td style="padding: 5px;">Escape to next test on error</td></tr> <tr><td style="text-align: center; padding: 5px;">09</td><td style="padding: 5px;">Loop with current data</td></tr> <tr><td style="text-align: center; padding: 5px;">02</td><td style="padding: 5px;">Restart program at selected test</td></tr> <tr><td style="text-align: center; padding: 5px;">01</td><td style="padding: 5px;">Reselect vector and control register address after program restart</td></tr> </tbody> </table> Tests 01 through 10 (octal) test each register of the DH11 for response. Tests 11 through 14 test to make sure that the SCR, LPR, BCR, and SSR register can be cleared. Tests 15 through 27 test the ability to set and clear bits 0, 1, 2, 3, 4, 5, 6, 9, 12, 13, and 15 (decimal) of the SCR. Tests 30 through 34 test the ability in <u>Maintenance Mode</u> to set and clear bits 7, 8, 10, 11, and 14 (decimal) of the SCR. Tests 35 through 37 test to make sure that bits 7, 10, 14 can only be cleared while in maintenance mode. Tests 40 through 56 test the ability to set and clear bits of the Line Parameter Register one at a time. Tests 57 through 76 test the ability to set and clear the bits of the Break Control Register one at a time. Tests 77 through 105 test the ability to set and clear bits 0, 1, 2, 3, 4, 5, 15, of the Silo Status Register one at a time.				<u>Switch</u>	<u>Action if set to one</u>	15	Halt on error	14	Loop in the current test	13	Inhibit error timeout	11	Inhibit iterations	10	Escape to next test on error	09	Loop with current data	02	Restart program at selected test	01	Reselect vector and control register address after program restart
<u>Switch</u>	<u>Action if set to one</u>																				
15	Halt on error																				
14	Loop in the current test																				
13	Inhibit error timeout																				
11	Inhibit iterations																				
10	Escape to next test on error																				
09	Loop with current data																				
02	Restart program at selected test																				
01	Reselect vector and control register address after program restart																				
		SIZE A	CODE SP	NUMBER DH11-0-11	REV A																

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ENGINEERING SPECIFICATION		CONTINUATION SHEET	
TITLE DH11 TEST PROCEDURE			
Tests 106 through 124 set the Line Parameter Register to all ones and clear the bits one at a time. Tests 124 through 144 do the same for the Break Control Register. Tests 144 through 153 do the same for the Silo Status Register bits 0, 1, 2, 3, 4, 5, 15. If a failure occurs, go to the section of this procedure marked "DZDHA Failures". 2. DZDHE DH11 Memory Test Running time: 2 sec. without iterations, 25 sec. with iter. Switch Settings: Same as DZDHA Test 1 is the bus address memory addressing test. It loads each location in the bus address memory with the address of that location. The address is repeated every four bits. The test verifies that each location in the bus address memory was addressed. Test 2 does the same thing to the byte memories as test 1 did to the current address memories. Tests 3 through 22 set a 177777 address in bus address memory location 0, verify it, clear it, verify that it is clear, then repeat for location 1, etc. Tests 23 through 42 do the same for the byte count memory locations. Test 43 is similar to tests 3 through 22 except that in addition to verifying that the selected location was set to 177777, a check is made to make sure that no data has appeared in any of the other bus address memory locations (they should all be clear except the one set to 177777). Test 44 is the same as test 43 but uses 125252 as the test word. Test 45 is the same as test 44 but uses 52525 as the test word. Tests 46, 47, 50 are the same as tests 43, 44, 45 but are applied to the byte count memories.			
SIZE	CODE	NUMBER	REV
A	SP	DH11-0-11	A
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ENGINEERING SPECIFICATION		CONTINUATION SHEET	
TITLE DH11 TEST PROCEDURE			
Tests 51 and 52 set all locations for the bus address memories (51) or byte count memories (52) to 177777 and then set selected location to 0. No other location should change. Tests 53, 54, and 55 test the ability to set and clear the memory extension bits. In case of failure, consult the section of this procedure entitled "DZDHB Failures". 3. DZDHC DH11 Transmitter and Receiver Basic Logic Test Running time: 23 sec. without iterations, 32 sec. with iter. Switch settings: Same as DZDHA Test 1 Set character available interrupt enable and verify that no interrupts occur. Test 2 Same as test 1, but silo overflow interrupt enable. Test 3 Same as test 2, but transmitter done interrupt enable. Test 4 Set character available interrupt enable and then (in maintenance mode) set character available and then verify that an interrupt occurs. Test 5 Same as 4, but silo overflow Test 6 Same as 4, but transmitter interrupt enable/non-existent memory. Test 7 Same as 4, but transmitter interrupt enable/transmitter done. Tests 10 through 27 set byte count for line 0, set BAR bit for line 0, verify BAR bit for line 0 clears, verify transmitter done set. This is done for line 0, then 1, then 2, etc. Tests 30 through 47 set byte count for all lines to 1, then set BAR bit for line 0, verify that byte count for line 0 goes to 0, that bus address for line 1 is incremented, and that all other byte counts and bus addresses are unchanged. This is done for line 0, then line 1, line 2, etc. Test 50 tests the silo maintenance mode by forcing a 10101010101010 into the silo and verifies that the character available bit is set, that a character available interrupt occurs, that NRC bit 15 is set and that the 10101010101010 pattern appears correctly in the Next Received Character (NRC) register. Test 51 verifies that the silo up counter counts up correctly.			
SIZE	CODE	NUMBER	REV
A	SP	DH11-0-11	A
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ENGINEERING SPECIFICATION		CONTINUATION SHEET	
TITLE DH11 TEST PROCEDURE			
Test 52 verifies that the silo down counter counts down correctly. Test 53 tests the silo alarm level alarm for 0, 1, 2, 4, 8, 16, and 32 characters to see that the alarm goes off (i.e., an interrupt occurs) at the proper fill level. If a failure occurs, go to the section of this procedure marked "DZDHC Failures". 4. DZDHD DH11 Speed Selection Logic Test Running time: 15 sec. without iterations, 1 min.55 sec. with iteration Switch settings: Same as DZDHA Test 1 tests to see that there is a clock for speed 1. It then sends three characters at a selected speed on line 0. It verifies that transmitter done occurs at that selected speed and that the amount of time taken is less at this speed than at the previously selected speed. This is done for 15 (octal), 13 (decimal) speeds at increasing speeds. Tests 2 through 15 are the same as test 1, but for lines 1, 2, 3, etc., up through line 14 (octal) Tests 16 through 32 are similar to tests 1 through 15, but for one character, and receiver done is checked and timed rather than transmitter done. If a failure occurs, consult the section of this procedure entitled "DZDHD Failures". 5. DZDHE DH11 Character Length and Basic Data Test Running time: 1 sec without iterations, 20 sec. with iterations Switch settings: Same as DZDHA Tests 1 through 100 transmit an all ones character at 9600 baud, changing first the character length (5 bit, 6 bit, 7 bit, 8 bit) on line 0, then doing the same on line 1, etc. If a failure occurs, consult "DZDHE Failures" 6. DZDHF DH11 Single Line Data Test Running time: 50 min. 50 sec. without iter., 52 min.25 sec. with iterations Switch settings: Same as DZDHA			
SIZE	CODE	NUMBER	REV
A	SP	DH11-0-11	A
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ENGINEERING SPECIFICATION		CONTINUATION SHEET	
TITLE DH11 TEST PROCEDURE			
Tests 1 through 20 transmit all 8 bit characters one at a time on line 0, 1, 2, etc. Tests 21 through 40 transmit a block of 400 (octal) characters on line 0, character length is 8 bits. Line speeds start at 50 baud and are incremented to 9600 baud. A block of 400 characters is transmitted at each speed. This process is repeated for lines 0 through 17 (octal). Tests 41 through 60 transmit a block of 400 (octal) characters on line 0; speed is 9600 baud; character length is 5 bits for the first 400 characters and is then changed to 6 bits, 7 bits, and 8 bits for future blocks of 400 characters. This process is repeated for lines 0 through 17 (octal). If a failure occurs, consult "DZDHF Failures". 7. DZDHG DH11 Multi-Line Data Test Running time: 4 sec. without iterations, 5 min.33 sec. with iterations Switch settings: Same as DZDHA Test 1 - In this test the silo alarm level is set to 0. The receiver is to be serviced on a per character basis in interrupt mode. Transmitter interrupts are disabled. A binary count pattern of 400 (octal) characters is sent on all lines. Character length is 8 bits for all lines. Test 2 - Same as test 1, but all lines are run at 9600 baud. Silo alarm level is set as high as possible. No receiver interrupt servicing, but rather characters are read from the silo as quickly as possible, testing the valid data bit of the Next Received Character register. If a failure occurs, consult "DZDHG Failures". 8. DZDHH DH11 Auto-Echo Test Running time: 10 sec. without iterations, 2 min. 40 sec. with iterations Switch settings: Same as DZDHA Tests 1 through 20 enable Auto-Echo on line 0, transmit an 8 bit character on that line at 9600 baud, receive and verify that character. This continues until 64 characters have been received. Then disable auto-echo. Exactly one more character should be received. This is done for all 16 lines.			
SIZE	CODE	NUMBER	REV
A	SP	DH11-0-11	A
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TITLE DH11 TEST PROCEDURE											
Tests 21 through 40 are similar to tests 1 through 20, but the data checked is a binary count pattern on all lines except that for which the auto-echo is being run. Lines are auto-echoed one line at a time while other transmissions take place. Test 41 transmits one character on each line with auto-echo enabled. 64 characters are received on each line. If a failure occurs, consult "DZDHH Failures". 9. DZDHI DH11 Break and Half-Duplex Test Running time: 10 sec. without iter., 3 min. 25 sec. with iter. Switch Settings: Same as DZDHA Tests 1 through 20 test the break facility by first flushing the UART transmitter for a line by transmitting two nulls and setting the break bit for that line. A binary count pattern is transmitted. Only one character should be received and that should be a break character. This is done for each line sequentially. Tests 21 through 40 set half-duplex on a line. A binary count pattern is transmitted. No characters should be received. This is done for each line sequentially. If a failure occurs, consult "DZDHI Failures". 10. DZDHJ-DH11 echo test This diagnostic contains a test which verifies that all characters (#-377 octal) will echo on each line (#-17 octal) with standard DH11 terminal attachments--TTY 33, 35 or VT05 etc.-- using ASCII asynchronous code (110 baud with two stop bits and 300, 600, or 1200 baud with one stop bit only). The starting address is 000200 octal. Operational switch settings are: <table><tr><td>SW15=1</td><td>Halt on error</td></tr><tr><td>SW13=1</td><td>Suppress error timeout</td></tr><tr><td>SW02=1</td><td>Reselect line number and baud rate</td></tr><tr><td>SW00=1</td><td>Change parameters at program restart</td></tr></table> 11. DZDHK-DH11 modem control test This program is a test of the modem control multiplexer used with the DH11-AD option. The program is divided into functional test groups as follows: Group 0: All line scanner and line multiplexer functions are tested using the H861 test connector.				SW15=1	Halt on error	SW13=1	Suppress error timeout	SW02=1	Reselect line number and baud rate	SW00=1	Change parameters at program restart
SW15=1	Halt on error										
SW13=1	Suppress error timeout										
SW02=1	Reselect line number and baud rate										
SW00=1	Change parameters at program restart										
SIZE	CODE	NUMBER	REV								
A	SP	DH11-0-11									

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Group 1: A single line is tested using the modem cable and a H315 test connector. Group 2: Connect-disconnect tests for 103A modems. Group 3: Connect-disconnect tests for 202C modems. The starting address is 000200 octal. Operational switch settings are: <table><tr><td>SW15=1</td><td>Halt on error</td></tr><tr><td>SW14=1</td><td>Loop current test</td></tr><tr><td>SW13=1</td><td>Suppress error timeout</td></tr><tr><td>SW11=1</td><td>Suppress iterations</td></tr><tr><td>SW10=1</td><td>Escape to next test on error</td></tr><tr><td>SW09=1</td><td>Freeze data</td></tr></table>				SW15=1	Halt on error	SW14=1	Loop current test	SW13=1	Suppress error timeout	SW11=1	Suppress iterations	SW10=1	Escape to next test on error	SW09=1	Freeze data
SW15=1	Halt on error														
SW14=1	Loop current test														
SW13=1	Suppress error timeout														
SW11=1	Suppress iterations														
SW10=1	Escape to next test on error														
SW09=1	Freeze data														
SIZE	CODE	NUMBER	REV												
A	SP	DH11-0-11	A												

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ENGINEERING SPECIFICATION		CONTINUATION SHEET																																			
TITLE DH11 Test Procedure																																					
F. Failures 1. DZDHA Failures a. If the following message is received- ##1346 REGISTER DID NOT RESPOND ADDRESS 76##2# this indicates that the PDP-11 processor did not receive a slave sync response from the DH11. The following checks should be made: 1.) Was the address entered correctly when you responded to the questions asked in the opening dialogue of diagnostic DZDHA? The N7277 module (located in slot 04) is normally supplied with all nine address jumpers in place, making the DH11 address 160000. The following jumper out table may be of use in verifying that the address cut into the N7277 matches the address you typed into the diagnostic. <table><tr><td>Jumpers OUT</td><td>Address</td></tr><tr><td>None</td><td>160000</td></tr><tr><td>4</td><td>160020</td></tr><tr><td>5</td><td>160040</td></tr><tr><td>5-4</td><td>160060</td></tr><tr><td>6</td><td>160100</td></tr><tr><td>6-4</td><td>160120</td></tr><tr><td>6-5</td><td>160140</td></tr><tr><td>6-5-4</td><td>160160</td></tr><tr><td>7</td><td>160200</td></tr><tr><td>7-4</td><td>160220</td></tr><tr><td>7-5</td><td>160240</td></tr><tr><td>7-5-4</td><td>160260</td></tr><tr><td>7-6</td><td>160300</td></tr><tr><td>7-6-4</td><td>160320</td></tr><tr><td>7-6-5</td><td>160340</td></tr><tr><td>7-6-5-4</td><td>160360</td></tr></table> Etc. The numbers identifying the jumpers are located on the N7277 etch right underneath the jumpers. In the set of five jumpers located near the center of the board, the order top to bottom is: 8-11-12-10-9. In the set of four jumpers located				Jumpers OUT	Address	None	160000	4	160020	5	160040	5-4	160060	6	160100	6-4	160120	6-5	160140	6-5-4	160160	7	160200	7-4	160220	7-5	160240	7-5-4	160260	7-6	160300	7-6-4	160320	7-6-5	160340	7-6-5-4	160360
Jumpers OUT	Address																																				
None	160000																																				
4	160020																																				
5	160040																																				
5-4	160060																																				
6	160100																																				
6-4	160120																																				
6-5	160140																																				
6-5-4	160160																																				
7	160200																																				
7-4	160220																																				
7-5	160240																																				
7-5-4	160260																																				
7-6	160300																																				
7-6-4	160320																																				
7-6-5	160340																																				
7-6-5-4	160360																																				
SIZE	CODE	NUMBER	REV																																		
A	SP	DH11-0-11	A																																		

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near the edge of the board, the order top to bottom is: 7-4-5-6. 2.) If the address that you entered in the opening dialogue of the diagnostic agrees with the jumpered-in address, reload the diagnostic making sure that there is no check sum error (i.e. that the Bus Data lights on the computer console are all out when the tape loading finishes.) Now try the diagnostic again. 3.) If the problem still exists, look at N7277 E72 pin 4. You should see a positive pulse about one-half microsecond long and occurring every five microseconds or so, when you run the following toggled-in program (See Note A, Page 26) <table><tr><td>5000/ 12706</td><td>Set up stack</td><td>5014/ 340</td><td>Set up</td></tr><tr><td>5002/ 1000</td><td></td><td>5016/ 6</td><td>for trap</td></tr><tr><td>5004/ 12737</td><td></td><td>5020/ 5737</td><td>Test</td></tr><tr><td>5006/ 5030</td><td>Set up for</td><td>5022/1600xx</td><td>DI register (Note 1)</td></tr><tr><td>5010/ 4</td><td>trap</td><td>5024/ 137</td><td>Jump</td></tr><tr><td>5012/ 12737</td><td></td><td>5026/ 5020</td><td>to 5020</td></tr><tr><td></td><td></td><td>5030/ 2</td><td>RTI</td></tr></table> 4.) If the pulse mentioned above occurs, use it as a trigger source while you look with a second scope channel at E72 pins 1, 2, and 5. At each of these there should be a high during the time that pin 4 is high. If these conditions are met, a negative pulse that is the complement of the positive pulse on pin 4 should appear as the output (pin 6). A shorter negative pulse should appear at E29 pin 10 along with some other pulses. Please note that if you look at E29 pin 10 without using a trigger source such as E72 pin 4 you will get useless information, as you will be seeing all of the slave syncs on the Unibus. What you are looking for is the slave sync that corresponds to the positive pulse (but is shorter) on E72 pin 4. b. If the following message is received- ##2312 MASTER CLEAR ERROR EXP REC ADDRESS ##771377 76##2# this indicates that master clear was unable to clear the register named. Note 1: The number used in location 5022 of the toggle-in program should be the address cited in the error message (see I.F.1.a on preceding page.)				5000/ 12706	Set up stack	5014/ 340	Set up	5002/ 1000		5016/ 6	for trap	5004/ 12737		5020/ 5737	Test	5006/ 5030	Set up for	5022/1600xx	DI register (Note 1)	5010/ 4	trap	5024/ 137	Jump	5012/ 12737		5026/ 5020	to 5020			5030/ 2	RTI
5000/ 12706	Set up stack	5014/ 340	Set up																												
5002/ 1000		5016/ 6	for trap																												
5004/ 12737		5020/ 5737	Test																												
5006/ 5030	Set up for	5022/1600xx	DI register (Note 1)																												
5010/ 4	trap	5024/ 137	Jump																												
5012/ 12737		5026/ 5020	to 5020																												
		5030/ 2	RTI																												
SIZE	CODE	NUMBER	REV																												
A	SP	DH11-0-11	A																												

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1.) The failure of master clear to clear a register is the result of one of several things. It could be that master clear is not being generated. It could be that the register is not being cleared despite the receipt of an initialize signal. It could be that the register is actually being cleared, but that the output of the register is not being properly presented back to the Unibus. The following procedures attempt to ascertain which of these effects is occurring. Begin by toggling in the following program which will generate a programmed Unibus Initialize: <table><tr><td>5000/</td><td>5 Reset</td></tr><tr><td>5002/</td><td>137 Jump</td></tr><tr><td>5004/</td><td>5000 to 5000</td></tr></table> 2.) Look at M7277 pins EP2 and FV 2 for Initialize High, a pulse about 20 milliseconds long and occurring every 60 milliseconds or so. Also look at pins FR2 and FM2 for an Initialize Low pulse. If none of these pulses can be found, look at pin A41 to see if Initialize is being generated on the Unibus. If all of these points show the proper signals, generate DH11 Initialize by toggling in the following program: <table><tr><td>5000/</td><td>5 Reset</td><td>5006/</td><td>160020 the SCR</td></tr><tr><td>5002/</td><td>52737 BIS</td><td>5010/</td><td>137 Jump</td></tr><tr><td>5004/</td><td>4000 bit 11 in</td><td>5012/</td><td>5002 to 5002</td></tr></table> 3.) Look at the pins mentioned above for the signals mentioned above (but slightly longer - about 2.4 microseconds). If these pulses are not seen at any of the above points, check pin FC1 for negative pulses of 2.4 microsecond duration. Check EL2 for positive pulses. 4.) If M7277 pins EP2, FV2, FR2, and FM2 do show the proper signals, check the following logic: If it is the SCR that is not being cleared, check M7289 E7, E11, E19, E41, E47, and E50.								5000/	5 Reset	5002/	137 Jump	5004/	5000 to 5000	5000/	5 Reset	5006/	160020 the SCR	5002/	52737 BIS	5010/	137 Jump	5004/	4000 bit 11 in	5012/	5002 to 5002
5000/	5 Reset																								
5002/	137 Jump																								
5004/	5000 to 5000																								
5000/	5 Reset	5006/	160020 the SCR																						
5002/	52737 BIS	5010/	137 Jump																						
5004/	4000 bit 11 in	5012/	5002 to 5002																						
SIZE	CODE	NUMBER	REV																						
A	SP	DH11-0-11	A																						
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TITLE DH11 Test Procedure													
If it is the Line Parameter Register (LPR) that is not being cleared, check the M7278 E37, E52, E59, and E61. If it is the Break Control Register (BCR) that is not being cleared, check the M7278 E38, E51, E60, E67. If it is the Silo Status Register (SSR) that is not being cleared, check the M7278 E53, E68, and E69. 5.) For the IC's cited above, make sure that the initialize signal arrives (run the toggle program from section "2.") above and produces the proper clearing action. 6.) Run the diagnostic looping on the current test when you get to the error-producing test. Re-do step 5.) above. If the bits cited by the diagnostic as being not cleared are in fact being cleared at the IC's mentioned above, the problem must be in the 74151 multiplexors in the M7278, the 8881's associated with those multiplexors, or in the Data Sources Selection leads. On the M7278 print there is a signal called Data to Bus High (pin AB1). Use that as a trigger source while looking at the 8881 inputs for the bit that the diagnostic claims is not being cleared. c. The remainder of the DZDHA test sets and clears the bits of the aforementioned registers one at a time. The following error message is typical: 002610 SYSTEM CONTROL REGISTER ERROR <table><tr><td>EXP</td><td>REC</td><td>ADDRESS</td></tr><tr><td>0000001</td><td>0000000</td><td>760020</td></tr></table> 1.) In the case of such a message referring to the System Control Register (SCR), check the M7277 pins CP1 and CT2 for positive pulses while running the diagnostic on a loop of the failing test. These pins should have positive pulses somewhat shorter than one half microsecond. If these pulses are observed, check M7289 IF7, E11, E19, E41, E47, E50 for proper clocking, proper input data, and proper operation. The input data comes from the "buffered data" buffers on the M7278.								EXP	REC	ADDRESS	0000001	0000000	760020
EXP	REC	ADDRESS											
0000001	0000000	760020											
SIZE	CODE	NUMBER	REV										
A	SP	A-SP-DH11-0-11	A										
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2.) In the case of the Line Parameter Register (LPR), check pin EP2 of the M7277 for positive pulses of less than one-half microsecond duration, while looping on the current failing test. Also check EH2 for a 300 nanosecond pulse. Also check ED1, EC1, EA1, etc. for the appropriate "Control Strobe" signal for the line in question. You may have to use the pulse at EH2 as a trigger source. If the appropriate pulses are found, check M7278 E37, E52, E59, and E61 for proper clocking, proper input data, and proper operation. To check input data, use control strobe as trigger.* 3.) In the case of the Break Control Register (BCR), check M7277 pin FU1 for positive pulses, and check M7278 E38, E51, E60, and E67 for proper clocking, input data, and operation. 4.) In the case of the Silo Status Register, check M7277 pins CP2 and CR1 for positive pulses, and M7278 E53, E68, and E69 for proper clocking, input data, and operation. 5.) If proper results are obtained in following the procedures outlined above, check the 74151 multiplexors and 8881's as described in section "b.6.)" above. *NOTES: ALL PROBLEMS ENCOUNTERED IN RUNNING DZDHA MUST BE SOLVED BEFORE RUNNING ANY OTHER DIAGNOSTICS. ETCH SHORTS, PADS THAT TOUCH, ETC. ARE FAR MORE COMMON THAN BAD ICs. TO CHECK INPUT DATA AT A FLIP-FLOP USE THE CLOCK LEAD TO THAT FLIP-FLOP AS A TRIGGER (ONCE YOU KNOW THAT THERE IS A SIGNAL ON THAT CLOCK LEAD). OTHERWISE YOU WILL SEE ALL OF THE BUFFERED DATA SIGNALS FROM THE UNIBUS..							
SIZE	CODE	NUMBER	REV				
A	SP	DH11-0-11	A				
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TITLE DH11 Test Procedure																																																												
2. DZDHB Failures a. It is assumed that diagnostic DZDHA has been run successfully. b. If the following message is received- 001376 BUS ADDRESS MEMORY ERROR <table><tr><td>EXP</td><td>REC</td><td>ADDRESS</td></tr><tr><td>010421</td><td>010420</td><td>01</td></tr></table> this indicates failure to properly read or write the current address memories. If the following message is received- 001514 BYTE COUNT MEMORY ERROR <table><tr><td>EXP</td><td>REC</td><td>ADDRESS</td></tr><tr><td>010421</td><td>010420</td><td>01</td></tr></table> this indicates failure to properly read or write the byte count memories. c. It is often useful to arrange the FDP-11 console switches to escape to the next test on error by setting switch 10 to the 1 state. After accumulating several error messages and writing down the received and expected data in binary instead of octal, conclusions can be drawn. Example: <table><tr><th colspan="2">Diagnostic Output (Octal)</th><th colspan="2">Binary Representation</th></tr><tr><th>Expected</th><th>Received</th><th>Expected</th><th>Received</th></tr><tr><td>004376</td><td>004356</td><td>0000010011111110</td><td>0000010011101110</td></tr><tr><td>Expected</td><td>Received</td><td>Expected</td><td>Received</td></tr><tr><td>006233</td><td>006213</td><td>0000110010011011</td><td>0000110010001011</td></tr></table> Notice that bit 04 is being dropped. If the problem is this simple or involves a few adjacent bits, go to paragraph "1" below. d. If the "received" data is consistently all zeroes, it would be wise to look at M7277 pin EN2 "Data to Bus High" while running the following program that reads the current address: <table><tr><td>5000/</td><td>52737 BIS</td><td>5016/160026 of CA to R0</td></tr><tr><td>5002/</td><td>4000 Bit #11 in</td><td>5020/ 137 Jump</td></tr><tr><td>5004/160020 the SCR</td><td></td><td>5022/ 5000 to 5000</td></tr><tr><td>5006/ 13737 Mov contents</td><td></td><td></td></tr><tr><td>5010/177570 of SR to</td><td></td><td></td></tr><tr><td>5012/160026 the CA</td><td></td><td></td></tr><tr><td>5014/ 13700 Mov contents</td><td></td><td></td></tr></table>								EXP	REC	ADDRESS	010421	010420	01	EXP	REC	ADDRESS	010421	010420	01	Diagnostic Output (Octal)		Binary Representation		Expected	Received	Expected	Received	004376	004356	0000010011111110	0000010011101110	Expected	Received	Expected	Received	006233	006213	0000110010011011	0000110010001011	5000/	52737 BIS	5016/160026 of CA to R0	5002/	4000 Bit #11 in	5020/ 137 Jump	5004/160020 the SCR		5022/ 5000 to 5000	5006/ 13737 Mov contents			5010/177570 of SR to			5012/160026 the CA			5014/ 13700 Mov contents		
EXP	REC	ADDRESS																																																										
010421	010420	01																																																										
EXP	REC	ADDRESS																																																										
010421	010420	01																																																										
Diagnostic Output (Octal)		Binary Representation																																																										
Expected	Received	Expected	Received																																																									
004376	004356	0000010011111110	0000010011101110																																																									
Expected	Received	Expected	Received																																																									
006233	006213	0000110010011011	0000110010001011																																																									
5000/	52737 BIS	5016/160026 of CA to R0																																																										
5002/	4000 Bit #11 in	5020/ 137 Jump																																																										
5004/160020 the SCR		5022/ 5000 to 5000																																																										
5006/ 13737 Mov contents																																																												
5010/177570 of SR to																																																												
5012/160026 the CA																																																												
5014/ 13700 Mov contents																																																												
SIZE	CODE	NUMBER	REV																																																									
A	SP	DH11-0-11	A																																																									
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TITLE DH11 Test Procedure															
If the aforementioned pin does have a signal (several hundred nanosecond positive pulse every few microseconds), run the diagnostic in a loop on the current (failing) test and look at E12. The signal should still be there, but not occurring so often. Using this signal as a trigger source, examine the 74151 multiplexors and the 8881 Unibus drivers; both of these on the M7278. If the "received" data is not all zeroes but appears to bear little if any relationship to the expected data, follow the procedures outlined in steps e-f-g-h below. e. For current address memory failures, run the toggled-in program from section d above. Look at the M7277 E48 pin 1. There should be positive pulses here, each several hundred nanoseconds long and occurring every few microseconds. f. For byte count memory failures, do the same as step e above, but use the following toggled-in program- <table><tr><td>5000/ 52737</td><td>5010/177570</td><td>5020/ 137</td></tr><tr><td>5002/ 4000</td><td>5012/160030</td><td>5022/ 5000</td></tr><tr><td>5004/160020</td><td>5014/ 13700</td><td></td></tr><tr><td>5006/ 13737</td><td>5016/160030</td><td></td></tr></table> and look for pulses again at M7277 E48 pin 1. This test and that above make sure that the current address and byte count memories are getting their selection information from the proper point. It is also important to loop the program on the failing test and make sure that the bits SCR 00, 01, 02, 03 progress properly from the System Control Register (M7289) to the inputs and outputs of M7277 E48. g. For current address errors, run the following program which loads one current address register: Use the toggle-in program from "d" above. Look at E57 pin 1 for positive pulses of several hundred nanosecond duration. If the pulses are there, use them as a trigger to look at E50 pin 1 for a 60 nanosecond pulse that begins 90 nanoseconds after the E57 pin 1 pulse begins. This 60 nanosecond pulse is the write enable pulse to the current address memories. h. For byte count errors, run the following toggle-in program which loads the byte count registers: Use the toggle-in program from "f" above.				5000/ 52737	5010/177570	5020/ 137	5002/ 4000	5012/160030	5022/ 5000	5004/160020	5014/ 13700		5006/ 13737	5016/160030	
5000/ 52737	5010/177570	5020/ 137													
5002/ 4000	5012/160030	5022/ 5000													
5004/160020	5014/ 13700														
5006/ 13737	5016/160030														
SIZE	CODE	NUMBER	REV												
A	SP	DH11-0-11	A												
DEC FORM NO DEC 10-(2011)-1002-N1370 DRA 100															
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TITLE DH11 Test Procedure			
Look at M7278 pin GJ1 for positive pulses and at M7278 pin BT2 for 60 nanosecond pulses occurring 90 nanoseconds after the GJ1 pulses begin. These are the write enable pulses for the byte count memories. When performing either test g or h, it is important to look at M7277 pin FK1 where 30 nanosecond positive pulses should occur at the conclusion of current address memory write enable pulses and byte count memory write enable pulse. Those 30 nanosecond pulses clear the "write current address" and "write byte count" flip-flops. 1. If, as explained in c above, a particular bit is incorrect, examine the logic associated with that bit. If the faulty bit is in a current address, examine the M7277. If it is in a byte count, examine the M7278. Run either the toggle program from g for current addresses or the toggle program from h for byte counts and check to see that load pulses are reaching the 74193 being used by the bit in question. Also make sure that a write enable pulse is reaching the 7489 involved. Run the diagnostic, looping on the failing test, while examining the data paths for proper operation. Use the load pulse terminal (pin 11) of the 74193 as a trigger source while looking at data inputs to the 74157 (also be sure that 74157 pin 1 is high) and at the data inputs to the 74193.			
SIZE	CODE	NUMBER	REV
A	SP	DH11-0-11	A
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3. DEDNG Failures a. If any of the following messages occur- ##1446 UNEXPECTED INTERRUPT CONTROL REGISTER CONTENTS ##23## a failure in the character available, silo overflow, and transmitter done interrupt circuitry is indicated. This logic is located on the M7289. Loop on the failing test and observe pin DD1, which should be high. E19 pin 6 should also be high. E50 pin 9 and pin 5 should be low. If DD1 was low, examine the logic of the M7279 Silo Buffer. Likewise, the M7279 should also be examined if the signal at E50 pin 10 was not a constant high. Signals on E50 pin 4 come from the M7278 E14, and should be constantly high at this point in the testing. On the M7278 make sure that pin FV2 does not pulse while looking on the failing test. b. If any of the following messages occur- ##22#2 NO INTERRUPT a failure in the interrupt generation circuitry is indicated. Loop on the failing test. If it is test 4, look at E31 pin 8 on the M7289. If the failing test is test 5, look at M7289 E31 pin 3. If the failing test is test 6, look at M7289 E48 pin 8. If the failing test is test 7, look at M7289 E48 pin 3. In each of the above cases, negative pulses (signal normally high, occasionally going down to zero) should be observed. The signal must not be either always high nor always low, as transitions are necessary for successful operation of the M7821 Interrupt Control module. If the negative pulses are found, look at pins DP1 and FM1 for positive pulses. If those pulses are found, try a new M7821 after examining the inputs to the M7821 for proper inputs and PROPER VECTOR JUMPING. Remember that for the M7821 jumpers are left in to assert ones on the bus and removed to assert zeroes. For failures in the character available and silo overflow interrupts, be sure that there are positive transitions on M7821 pins G1 and G1. For transmitter done and non-exist memory interrupts, be sure that there are positive transitions on M7821 pins M3 and M2. The M7821 referred to is that located in slot A46.			
SIZE	CODE	NUMBER	REV
A	SP	DH11-0-11	A
DEC FORM NO DEC 10-(2011)-1002-N1370 DRA 100			
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TITLE DH11 Test Procedure																																			
c. If a failure message such as that below occurs- ##315# NO INTERRUPT ##316# TRANSMITTER DONE NOT SET determine the line number and then verify that the BAR (Buffer Active Register) bit for that line actually gets set. This may be done by looping on the failing test and examining the BAR register on the M7278. Check for the generation of the transmitter finished pulse by running the following toggled-in program which sets the byte count for line zero to all ones and then to all zeroes. <table><tr><td>5000/ 52737</td><td>BIS</td><td>5020/ 160030</td><td>to BC</td></tr><tr><td>5002/ 4000</td><td>bit #11</td><td>5022/ 137</td><td>Jump</td></tr><tr><td>5004/ 160020</td><td>in SCR</td><td>5024/ 5000</td><td>to 5000</td></tr><tr><td>5006/ 12737</td><td>Move</td><td></td><td></td></tr><tr><td>5010/ 777777</td><td>all ones</td><td></td><td></td></tr><tr><td>5012/ 160030</td><td>to BC</td><td></td><td></td></tr><tr><td>5014/ 12737</td><td>Move</td><td></td><td></td></tr><tr><td>5016/ 000000</td><td>all zeroes</td><td></td><td></td></tr></table> See Note B, Page 26 Note that a permanent low on M7278 pin AS2 would cause the E14 one-shot to not fire. Pin AS2 should be always high. Look for transmitter finished pulses on pin ARI. Also look at the "Clear BAR Bit" signal appropriate to the line that the diagnostic reports is erring. Verify that the signal from pin ARI causes pin FR 2 of the M7289 to go high and/or stay high. d. If the following failure message occurs- ##12# BYTE COUNT ERROR EXP REC 777777 loop on the current test and examine the BAR bit (M7278) appropriate to the line for which the error is reported. This BAR bit should change back and forth between 1 and 0 during the test looping. e. In the case of the following message- ##133# SILO DATA ERROR EXP REC 725252				5000/ 52737	BIS	5020/ 160030	to BC	5002/ 4000	bit #11	5022/ 137	Jump	5004/ 160020	in SCR	5024/ 5000	to 5000	5006/ 12737	Move			5010/ 777777	all ones			5012/ 160030	to BC			5014/ 12737	Move			5016/ 000000	all zeroes		
5000/ 52737	BIS	5020/ 160030	to BC																																
5002/ 4000	bit #11	5022/ 137	Jump																																
5004/ 160020	in SCR	5024/ 5000	to 5000																																
5006/ 12737	Move																																		
5010/ 777777	all ones																																		
5012/ 160030	to BC																																		
5014/ 12737	Move																																		
5016/ 000000	all zeroes																																		
SIZE	CODE	NUMBER	REV																																
A	SP	DH11-0-11	A																																
DEC FORM NO DEC 10-(2011)-1002-N1370 DRA 100																																			
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the silo test pattern was not properly received. Loop on the failing test and look at M7278 pin CN2 which should have positive pulses. Observe pin FV2 for one microsecond negative pulses that occur as the result of the CN2 pulses. Look at M7279 pin AR1 for the same pulses that you observed on M7278 pin CN2. Using those pulses as a trigger, look at pins 4 and 9 of the following ICs on the M7279: E2, E7, E12, and E16. These points should be low for at least the duration of the pulses on AR1. Look at pins 7 and 12 of these same ICs for highs occurring for at least as long as the AR1 pulses. These checks confirm that the proper test pattern is being prepared for entry into the silo, that the silo maintenance bit is being set, and that the silo maintenance pulse is being generated. f. The silo maintenance pulse is used in the DH11 receiver logic to simulate the finding of a data available flag, thus causing the silo logic to be cycled. Observe pin FF1 on the M7289 for the same one microsecond negative pulses that you previously observed on pin FV2 of the M7278. Using these pulses as a trigger source, observe pin AJ2 (Load Silo L) where negative pulses should occur about 2 microseconds after the FF1 pulse. There will be a varying time between the FF1 pulse and the AJ2 pulse because the receiver scanner/receiver logic has to wait for a tick of the 2.54 MHz clock before commencing operation (make sure that there is such a clock signal arriving at the M7289) and this clock is in no way related to the instruction that set the silo maintenance bit and thus generated the silo maintenance pulse that appears on FF1. Notice that the function of the FF1 pulse is to set Scanner Stop and thus cause the receiver sequencer (M7289 E21) to generate Load Silo L. g. Confirm the existence of Load Silo L pulses at pin BJ2 of the M7279. h. Be sure that there is a 5.068 MHz (period=200 nanoseconds) clock signal at pin BN1 of the M7279. i. Be sure that there is -15 VDC at pin AB2 of the M7279. j. Check pin BV2 of the M7279 to make sure that the Load Request flip-flop is being set and cleared. It gets set by the Load Silo L pulses (see G above).			
SIZE	CODE	NUMBER	REV
A	SP	DH11-0-11	A

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k. Check BK2 for 30 nanosecond negative pulses occurring about 170 to 370 ns after load request sets. (You may wish to use the 5.068 signal as a trigger and turn up the intensity). Since these pulses clear Load Request, the negative transition of BV2 might also be a good trigger source. l. Look at pin BN1 for positive pulses about a half microsecond wide. These are the program reading the NRC register and hence (hopefully) cycling a character out of the silo. m. Observe pin AL1 for negative pulses, occurring throughout the looping on the failing test. If these pulses only occur when you first start the program, the silo is probably being filled up, perhaps indicating failure in the "Unload" circuitry. n. Observe BL1 for positive pulses. These rely upon E9 pin 8 being low at times. o. Observe BV1 for negative pulses. Trace the effects of these pulses through the M7289 logic.			
SIZE	CODE	NUMBER	REV
A	SP	DH11-0-11	A

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4. DZDHD Failures a. Be sure that the lead entitled "Z# Baud" is ground and hence that the "TOP BUFF Z# BAUD H" and "BOT BUFF Z# BAUD H" signals are permanently high. Refer to the M7288 Circuit Schematic. b. Check all "TOP BUFF" and "BOT BUFF" signals at M7288 E66, E67, E69, E70, E73, E74, E75. Use the table on the first page of the M4540 Circuit Schematic to determine the proper periods for the various baud rates. Using an oscilloscope you will only be able to make an approximate measurement, but you will be able to determine which clock signal is which and that no two are crossed or interchanged. c. Make sure that the aforementioned signals make it through to E4 and E2 at the appropriate pins. d. Looping on the failing tests, make sure that the proper "BUFF LPR" signals exist at the inputs, that the Control Strobe signal occurs (300ns), that there is no noise on the control strobe signal, and that the outputs of the 74174 and 74175 of the failing line are being properly set. e. Beware of the fact that the diagnostic detects problems by comparing the time it takes to transmit at one speed with the time it took at a previous speed. When an error is reported, it may be the speed tested prior to the present speed that was in fact in error. Example: Assume the speeds should be 110, 134.5, 150 and that they are actually 110, 300, 150. The diagnostic will determine that things happened faster at speed 2 than at speed 1 (300 compared to 110), but when it gets to speed 3 (150) it will report an error. The actual problem is speed 2 where one finds 300 instead of 134.5. 5. DZDHE Failures a. While looping on the failing test, look at CD2 of both UART cards for a 300 ns Control Strobe signal. Check the CH2, CJ1, CF2, CJ2, CF2 pins for proper parameter data. b. Refer to DZDHC Failures for further tests.			
SIZE	CODE	NUMBER	REV
A	SP	DH11-0-11	A

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6. DZDHF Failures a. In most cases it should be possible to create failures at a faster rate using the DZDHC diagnostic. Try that. If fewer or no failures occur running the DZDHC for a time equal to that which you ran the DZDHF, the problem most likely concerns the loading of Line Parameters, since the DZDHF changes the line parameters whereas the DZDHC does not. b. It will generally be beneficial to try the same procedures for troubleshooting DZDHF as DZDHC so it is recommended to follow the procedures below, even if you are running DZDHF. 7. DZDHC Failures a. If difficulties occur with one line only, swap M7280 UART cards and see if the problem follows - i.e. that the problem moves from line 1 (Octal) to line 11 (Octal), etc. b. Be sure that the transmit strobe signal to the UARTs is long enough. It must be 250 nanoseconds or more. Note that this requires an added capacitor on the M796 to generate a wider "Data Strobe". (This capacitor is 100 pf). c. If difficulties occur on several lines, but only on one bit, check the buffered data leads, tran data leads, silo inputs, silo outputs, M7278 multiplexors, and M7278 Unibus drivers. Also check the auto-echo switch (M7277 E29 and E42), and the byte switch (M7277 E40 and E43). d. Receipt of a character that is one lower than that expected may be a failure of the current address up-counter system to function properly or a failure of the byte switch (see above). e. Receipt of a character one higher than expected might be a silo unloading problem; perhaps caused by noise on the Read NRC line or perhaps by improper one-shot times. f. Check ALL oneshots for accuracy. They should be no more than 20% longer or 10% shorter than their nominal values. This is particularly true if they are on the short side and the unit is running in high temperatures. g. Be sure that there is no crosstalk on the "Control Strobe" leads. (No noise pulses greater than 0.8 volts)			
SIZE	CODE	NUMBER	REV
A	SP	DH11-0-11	A

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8. DSDMH Failures

- c. Make sure that the above signal makes it to the E22 74154 multiplexor on the N7289. The following toggle-in program sets auto-echo enable on one line and allows the receiver scanner to run continuously.

5000/ 52737 EIS 5022/ 137 Jump
5002/ 4900 bit #11 5024/ 5006 to 5006
5004/160020 in SCR
5006/ 13737 Nov contents
5010/177570 of SR
5012/160020 to SCR
5014/ 52737 EIS
5016/ 10000 bit 15 (AE ENAD)
5020/160020 in LFR

Look at pin 10 of E22 on the M7289 for negative pulses (i.e. the signal is almost always high, but has occasional excursions down to nominal 0 volts).

- d. Again operate the diagnostic, looping on the failing test. Look at W289 E18 pins 2 & 6 and E10 pins 3 & 4 for highs. Look at E18 pins 10 & 14 for high. Some of these may be alternately high and low, but what is important now is that they are high at least sometimes.

- a. Look at W728: E14 pin 3 for low pulses, E2 pin 3 for high pulses, E2 pin 6 for low pulses, and E1 pin 4 for high pulses. If you are O.K. at E2 pin 3, but for some reason, check E2 pin 5 for being high at the same time as pin 4 (this should occur). Check E1 pin 5 for being low at the same time as pin 6 (this should occur). If the proper signals cannot be found on E2 pin 3 or E1 pin 5, examine the receiver sequencer - E21.

M7289 E21 Waveforms:

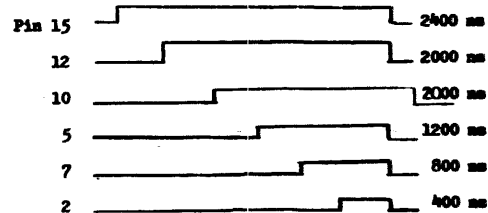
SIZE A	CODE SP	NUMBER DH11-0-11	REV A
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M7289 E21 Waveforms:



The above waveforms can only be observed if the scanner stop flip-flop E44 pin 5 is setting and clearing (i.e. the receiver scanner mechanism is servicing characters).

- f. Trace the AE GO L lead and make sure that it causes W7209 E34 to switch the UART transmitter scan leads and that it causes W7277 E39 and E42 to switch the data source leads for the UART transmitters.

- g. If the problem occurs with one line only, try swapping the W7280 UART cards to see if the problem follows - i.e. see if the problem that used to reported on line 7 (octal) is now found on line 17 (octal).

9. DZDHI Failures

- a. If the following message is received-
- | | | | |
|--------|--------------------------------|--------|--------------------|
| 001504 | MORE THAN 1 CHARACTER RECEIVED | 001524 | BREAK DATA MISSING |
| EXP | REC | EXP | REC |
| 000400 | 000000 | 720000 | 700000 |
- it indicates that the break circuitry did not function properly.

- b. Check the M278 E38, E51, E60, and E67 to make sure that the break is not being set for the failing line. Do this while looping on the failing test. Check M278 E45, E46, E75, E76 to see if the setting of the break bit produces the appropriate high on the "TTL DATA OUT" lines. The 7400 gates E45, E46, E75, E76 are normally kept qualified by the high state of the Q outputs from the 74175's that comprise the Break Control Register. Setting of a bit in

SIZE A	CODE SP	NUMBER DH11-0-11	REV A
-----------	------------	---------------------	----------

DEC FORM NO DEC 16-(501)-1002-N370
DRA 100

SHEET 26 OF 28

CONTINUATION SHEET

the Break Control Register brings the appropriate $\bar{Q}$ output to the low state, disabling the 7400 gate and placing a permanent high on the TTL DATA OUT line. The logic convention of the TTL DATA OUT lines is such that a high - space = 0 - BREAK.

- c. If the following message is received-

~~#6244~~ RECEIVER NOT BLINDED

it indicates that the half-duplex logic did not function correctly.

- d. While looping on the failing test, check the W7288 to make sure that the "Half-Duplex" bit for the failing line is being set.

- g. Check the M7289 to make sure that End of Character is being received from the UART that serves the failing line. If in doubt, swap the M7280 UART cards and see if the diagnostic now reports the error on line 11 instead of 1, 12 instead of 2, etc. (The diagnostic reports line numbers in Octal). Also check the M7289 E6, E20, E32, E42 to make sure that the half-duplex enable and end of character signals are disabling the E4, E16, E28, E39 gating appropriate to the erring line. End of Character is low while the UART is transmitting a character and comes high very briefly between characters. Loop on a test of a working line if you desire to see what it should look like.

Make all of the above examinations while looping on the failing test, unless otherwise instructed.

Note A: If the DMI1 is not decoding the address being sent by the diagnostic, E72 pin 4 will have no pulses. If the DMI1 is decoding the address but not sending Slave Sync back to the processor, the pulse will be about 25 microseconds long and occur every 45 microseconds or so. If proper response is occurred, times will be as indicated in F.1.a.3) on page 11.

Note B: As indicated in the description of this test, this program tests only the effect of zeroing the byte count on line 00. To test other lines, replace the first three instructions of the program given with:

```

5000      13737  Move contents of
5002      177570 The switch register to
5004      160020 The SCR
Toggle the desired line number into the switch register.

```

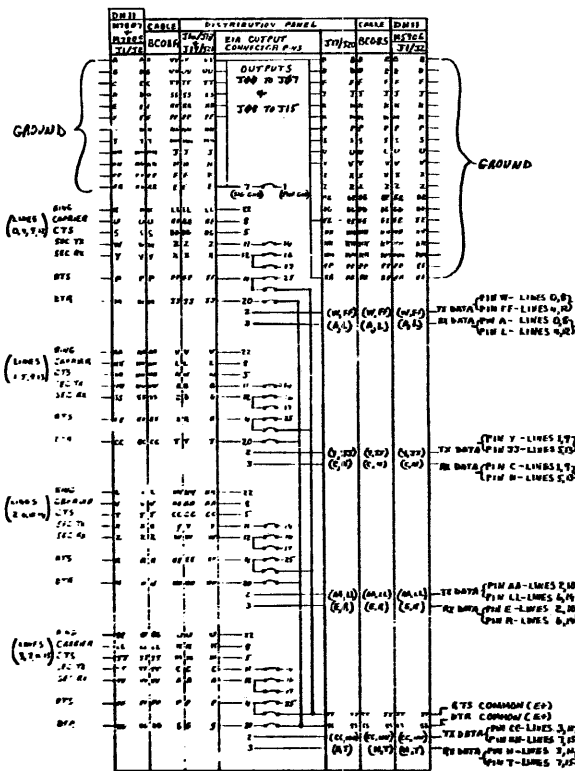
SIZE A	CODE SP	NUMBER DH11-0-11	REV A
-----------	------------	---------------------	----------

DEC FORM NO DEC 16 (201) 1002-11370
DEA 100

SHEET 27 OF 28

CONTINUATION SHEET

TABLE I
WIRE LOCATOR



NOTES: ① M107-LINES 0 TO 5 ② DISTRIBUTION PANEL (IN LOOPS)
31-0703; 32-0707 31-0703 32-0707 CONTAINS
③ M107-LINES 0 TO 7 311-0707 32-0707 DATA
31-0703; 32-0707 ④ M106 (IN DATA LOOPS)
31-0703; 32-0707

SIZE	CODE	NUMBER	REV
A		011-0-11	A

DEC FORM NO DEC 16-(381)-1022-N370
ORA 108

SHEET 28 OF 28

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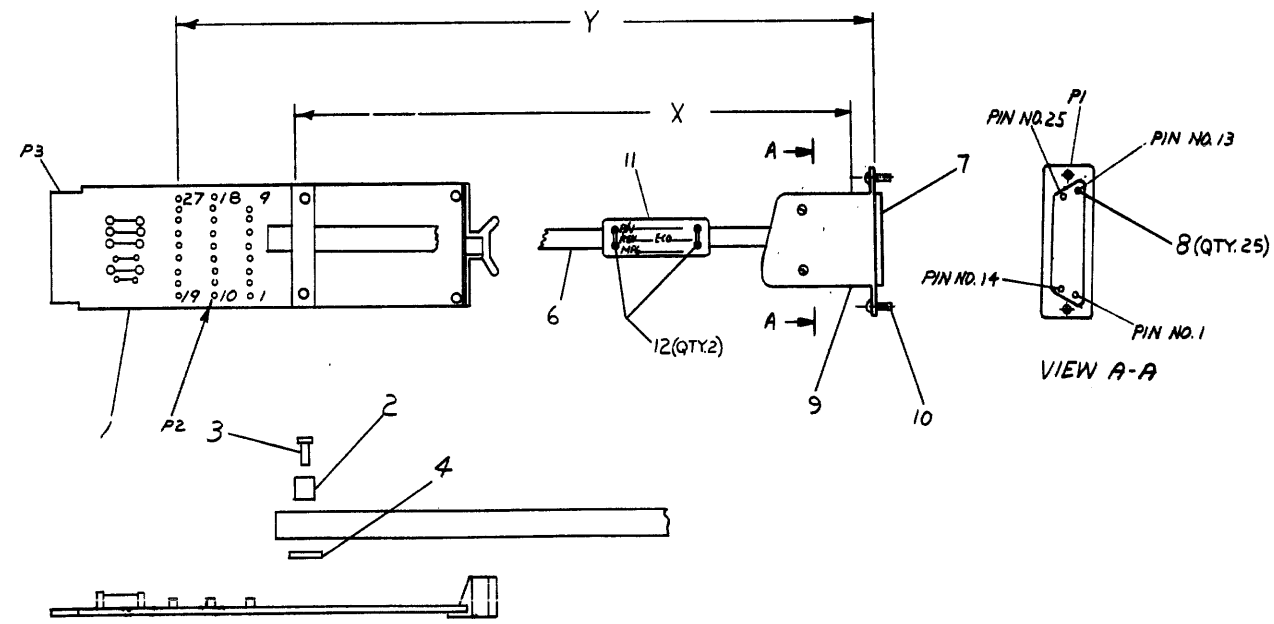
M9700 JUMPER FUNCTIONS

FUNCTIONS OF MODERN JUMPERS WHEN (INSTALLED)
A. EIA SECONDARY TRANSMIT AND RECEIVE DATA LINES TO EIA PINS 14 AND 16
B. 202 SECONDARY TRANSMIT AND RECEIVE DATA LINES TO EIA PINS 11-12
C. BELL 103B RESTRAINT FUNCTION IS MONITORED BY SECONDARY RECEIVE
D. BUSY-BELL 103B FORCE BUSY FUNCTION DRIVEN BY REQUEST TO SEND

LEGEND		
NUMBER	VARIATION	
	DIM - X	DIM - Y
BC01R-25	25' ± 3"	25' ± 3"
BC01A-50	50' ± 2 1/2"	50' ± 3"

BC01R WIRE TABLE			
NUMBER	COLOR	PI-PIN	P2-LUG
BLU - WHT	1	6	GROUND
WHT - BLU	2	1	TRANSMITTED DATA
ORN - WHT	3	2	RECEIVED DATA
WHT - ORN	4	24	REQUEST TO SEND
GRN - WHT	5	14	CLEAR TO SEND
WHT - GRN	6	26	DATA SET READY
BRN - WHT	7	7	GROUND
WHT - BRN	8	18	CARRIER
SLA - WHT	9	15	+POWER (NOT USED)
WHT - SLA	10	16	-POWER (NOT USED)
BLU - RED	11	19	BELL 202 SEC. TRANS. DATA
RED - BLU	12	21	BELL 202 SEC. RECV. DATA
ORN - RED	13	11	SEC. CLEAR TO SEND
SLA - RED	14	20	EIA SECONDARY TRANS. DATA
SLA - GRN	15	3	SERIAL CLOCK TRANS.
RED - BRN	16	23	EIA SECONDARY RECV. DATA
SLA -	17	22	SERIAL CLOCK RECV.
RED - SLA	18	17	UNASSIGNED NOT USED
BLU - BLK	19	12	SECONDARY REQUEST TO SEND
BLK - BLU	20	9	DATA TERMINAL READY
ORN - BLK	21	13	SIGNAL QUALITY DETECT
BLK - ORN	22	25	RING
GRN - BLK	23	8	SIGNAL RATE SELECT
BRN - RED	24	10	EXTERNAL CLOCK
RED - ORN	25	27	FORCE BUSY
SPECIAL			
SHIELD A	CUT	4	SHIELD A (GROUND)
SHIELD B	CUT	5	SHIELD B (GROUND)

NOTES:
1. IF USED FOR FOLLOWING OPTIONS CUT ALL JUMPER EXCEPT (DC11, DP11, DM11-DB, DS10, DQ11 AND DS11)
(2) 202 JUMPERS
REF. NOTE #6
DN11 - (2) EIA JUMPERS
DM11-DC/DM11-BB(2) 202 AND (1) B11 JUMPERS. FOR OTHER APPLICATIONS REFER TO CHART ON LEFT FOR M9700 JUMPER FUNCTIONS.
2. CIRCLED LETTERS ON RIGHT OF WIRE TABLE INDICATE THOSE PINS WHICH ARE DEPENDENT ON M9700 JUMPER FUNCTIONS AT LEFT.
3. B11 JUMPER CONNECTS J2 TO F1
SOLDER #6 (CABLE) TO #1 (CONNCARD), APPLY #4 (TAPE) AROUND #6 (CABLE), ASSEMBLE #2 (CABLE CLAMP) AND #3 (EYELETS) TO #1 (CONNC. CARD) AFTER SOLDERING
4. EACH SOLDERED CONNECTION ON PI SHALL BE INSULATED WITH A #4 ENCH. PIECE OF TIE-WRAP #5 (TUBING)
5. PI-15 AND PI-17 ARE SHIELDED LEADS
6. OLDER REV. BC01R CABLES HAD "301" JUMPERS (M9700+BC05C-25). NEW REV. CABLES (M9700) HAVE THESE CONNECTIONS IN THE ETCH. DO NOT REMOVE 301 JUMPERS ON OLD REV. CABLES.



2	TIE WRAP	9007031	12
1	CABLE LABEL	9009332	11
1	SCREW, RETAINER (2/KIT)	1210493-51	10
1	HOOD WITH STRAIN RELIEF	1210493-50	9
25	PINS, 24 TO 28 AWG.	1210493-43	8
1	CONN. PLUG	1210493-31	7
1	CONN. PLUG #BB25-P	1205886	6
1	HOOD, SHIELD #DB51226-1	1205885	5
1	AIR CABLE 25 CONDUCTOR	9107736	4
1	AIR SHrinkable TUBING	9107255	3
2	EYELET A-94	9006741	2
1	CLAMP CABLE	1202790-01	1
1	M9700 CABLE CONNECTOR	M9700	1

FIRST USED ON OPTION/MODEL		QTY.	DESCRIPTION	PART NO.	ITEM NO.
PDP 11					
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES		DATE 10-12-73			
TOLERANCES		CHK'D. DATE 10-16-70			
DECIMALS	ANGLES	ENG. DATE 10-16-73			
.XXX = .005	±0° 30'	PROJ. ENG. DATE 10-16-70			
.XX = .02		V. BASTIANI DATE 10-16-70			
.X = .1		PROD. DATE 10-16-70			
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY 1		D. CULL DATE 10-16-70			
MATERIAL		NEXT HIGHER ASSY.			
FINISH		A-PL-DC11-DA-0			
SCALE		1/1			
SHEET		1 OF 1			

PARTS LIST		TITLE	
digital EQUIPMENT CORPORATION		CABLE CARD ASSY (BC01R)	
SIZE CODE	NUMBER	REV.	
DUA	BC01R-0-0	H	
DIST.			

REVISIONS		
CHK	CHANGE NO	REV
24	BC01R-00003	U
REVISED SREDRAW		
24	24	24
SHAMMAS		
24	SHAMMAS 8-13-79	
24	BC01R-00004	E
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SHAMMAS		
24		
SHAMMAS		
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BC01R 00005		
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OUTPUT CABLES ARE EITHER BCØIR-25 IF EIA OR M973 MATE-N-LOCK CONNECTER CARD FOR PDP-11 TTY
NOTE: NEITHER ITEM SUPPLIED WITH DM11-AA

The diagram illustrates the interconnection of the DM11 system. At the top left, a box labeled 'DM11 DISTRIBUTION PANEL WIRED ASSY #D-AD-7008443-0-0' is connected to '16 OUTPUT CABLES' which lead to connectors BØ6 and B21. Below the panel is a 'POWER HARNESS #7008493' connected to a power supply unit. The power supply unit is labeled 'H758-A POWER SUPPLY 115V OR H758-B POWER SUPPLY 230V'. A 'DM11 CONTROL CABLE' is shown, with a note: 'NOTE: USED ONLY WHEN DM11-BB IS IMPLEMENTED'. This cable connects to a 'PDP11 OR BAI1 EXTENSION BOX THAT CONTAINS THE DM11 CONTROL LOGIC WIRED ASSY D-AD-7008444-0-0'. The extension box is connected to an 'AC POWER CORD TO LINE OR PDP11 IF ABOVE IS BAI1'. A 'DCØ8 CS' is also shown, with a note: 'SEE NOTE 2'. The DCØ8 CS is connected to the extension box and the DM11 Distribution Panel. The DM11 Distribution Panel is also connected to a 'DM11-AA, AC DATA CABLE BCØ8S-15'.

NOTES:
1. DISTRIBUTION PANEL 7008443 AND POWER SUPPLY H758 SUPPLIED ONLY WITH DM11AA, DM11-AC
2. DCØ8 CS MUST BE ORDERED SEPARATELY DM11-AB DATA CABLE PLUGS INTO SLOTS A31, A32 OF DCØ8 CS FOR LINES ØØ TO LINE 15 OF DCØ8 CS. A SECOND DM11-AB PLUGS INTO THE DCØ8 CS AT SLOTS B31, B32 FOR LINES 16 TO 31.

REVISIONS	CHANGE NO.	REV.
1	DM11A-00009	A
2	DM11A-00010	B
3	DM11A-00011	C
4	DM11A-00012	D
5	DM11A-00013	E
6	DM11A-00014	F
7	DM11A-00015	G
8	DM11A-00016	H
9	DM11A-00017	I
10	DM11A-00018	J
11	DM11A-00019	K
12	DM11A-00020	L
13	DM11A-00021	M
14	DM11A-00022	N
15	DM11A-00023	O
16	DM11A-00024	P
17	DM11A-00025	Q
18	DM11A-00026	R
19	DM11A-00027	S
20	DM11A-00028	T
21	DM11A-00029	U
22	DM11A-00030	V
23	DM11A-00031	W
24	DM11A-00032	X
25	DM11A-00033	Y
26	DM11A-00034	Z

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.	
DM11					
PARTS LIST					
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES		DRN. <i>J. H. H. H.</i>	DATE <i>5/18/71</i>	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS	
DECIMALS		CHK'D <i>R. Cook</i>	DATE <i>6-18-71</i>		
ANGLES		ENG. <i>J. H. H. H.</i>	DATE <i>6-18-71</i>		
.XXX = .005 .XX = .02 .X = .1		PROJ. ENG. <i>J. H. H. H.</i>	DATE <i>6-18-71</i>		
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ☒		PROD. <i>J. H. H. H.</i>	DATE <i>6-18-71</i>		
MATERIAL		NEXT HIGHER ASSY.		TITLE INTERCONNECTION DM11	
FINISH		A-ML-DM11-A			
SCALE		C IC			
SHEET 1 OF 1		DIST. G			
		NUMBER		REV. C	

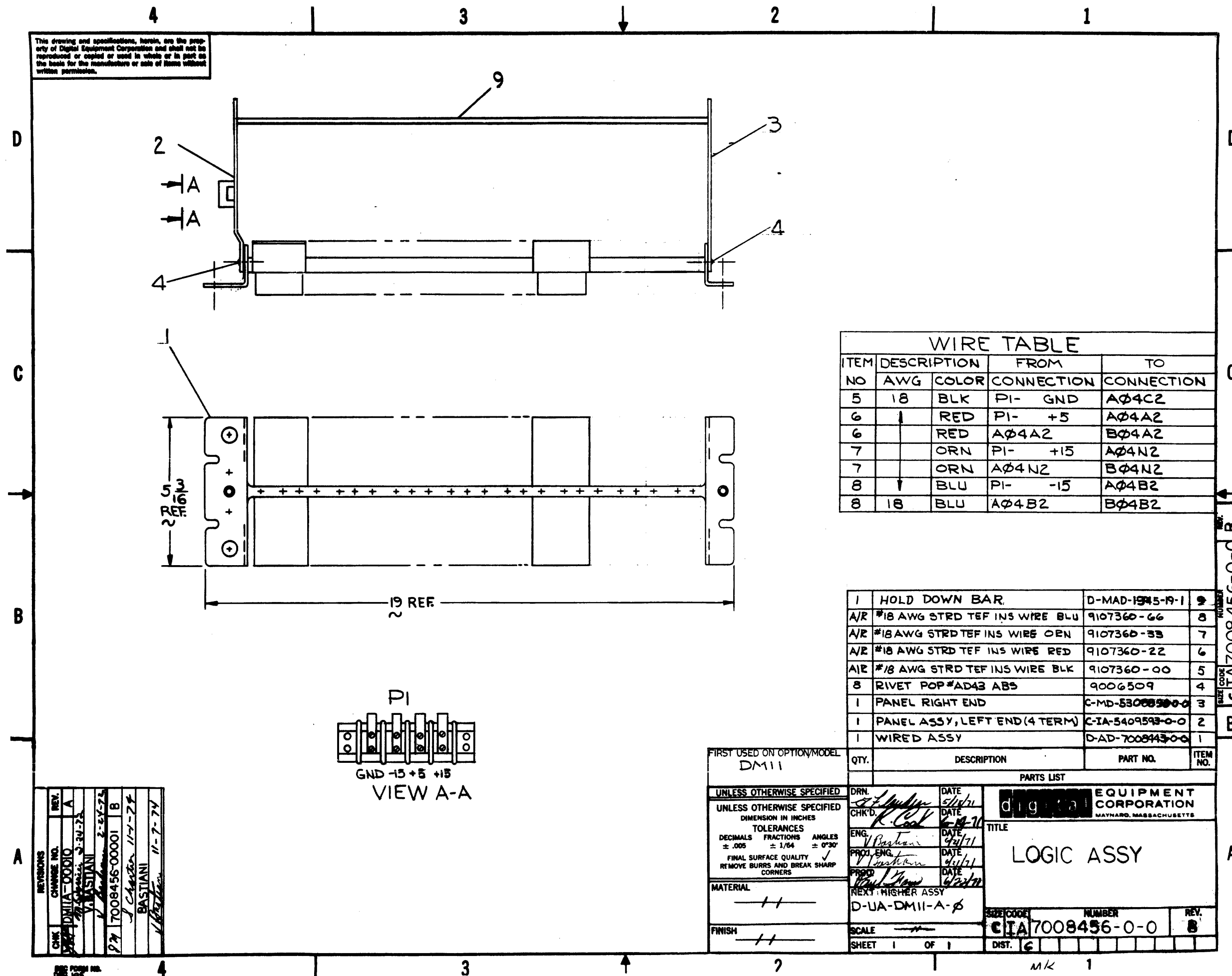
1. DISTRIBUTION PANEL
7008443 AND POWER
SUPPLY H758 SUPPLIED
ONLY WITH DM11AA,
DM11-AC

2. DCØ8 CS MUST BE
ORDERED SEPARATELY
DM11-AB DATA CABLE
PLUGS INTO SLOTS
A31,A32 OF DCØ8 CS
FOR LINES ØØ TO
LINE 15 OF DCØ8 CS.
A SECOND DM11-AB
PLUGS INTO THE
DCØ8 CS AT SLOTS
B31,B32 FOR LINES
16 TO 31.

REVISIONS		CHG	CHANGE NO.	REV.
			DM11A - 00009	A
Bastiani, et al 2-1-72				
BASTIANI				
V Bastiani 2-11-72				
			DM11A - 00013	B
Bastiani 5-17-72				
BASTIANI				
Bastiani 5-17-72				
			DM11A - 00016	C
Bastiani 8-22-73				
V. BASTIANI				
V Bastiani 9/9/73				

FIRST USED ON OPTION/MODEL		QTY.		DESCRIPTION		PART NO.		ITEM NO.	
DM11									
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES		DRN. <i>J. Hayden</i>		DATE 5/18/71		digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS			
		CHK'D <i>R. Cook</i>		DATE 6-18-71					
DECIMALS		ANGLES		ENG. <i>J. Hayden</i>		DATE 5/18/71		INTERCONNECTION DM11	
.XXX = .005 .XX = .02 .X = .1		± 0° 30'		PROJ. ENG. <i>J. Hayden</i>		DATE 5/18/71			
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ☒				PROD. <i>R. Hayden</i>		DATE 5/18/71			
MATERIAL <i>— / —</i>		NEXT HIGHER ASSY.							
FINISH <i>— / —</i>		A-ML-DM11-A		SIZE CODE C		NUMBER DM11-A-4		REV. C	
		SCALE <i>— / —</i>		DIST. ☒					
		SHEET 1 OF 1							

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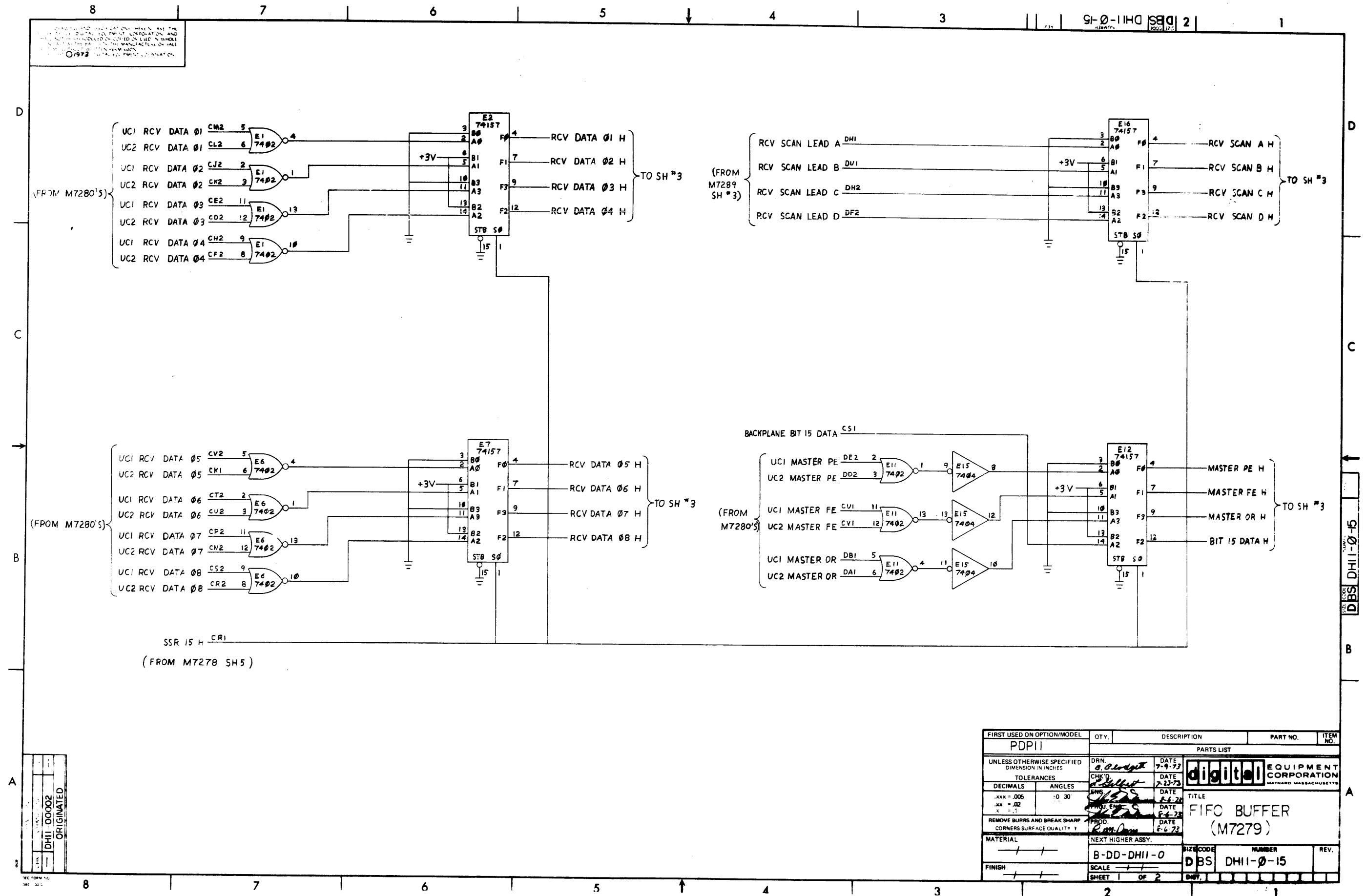


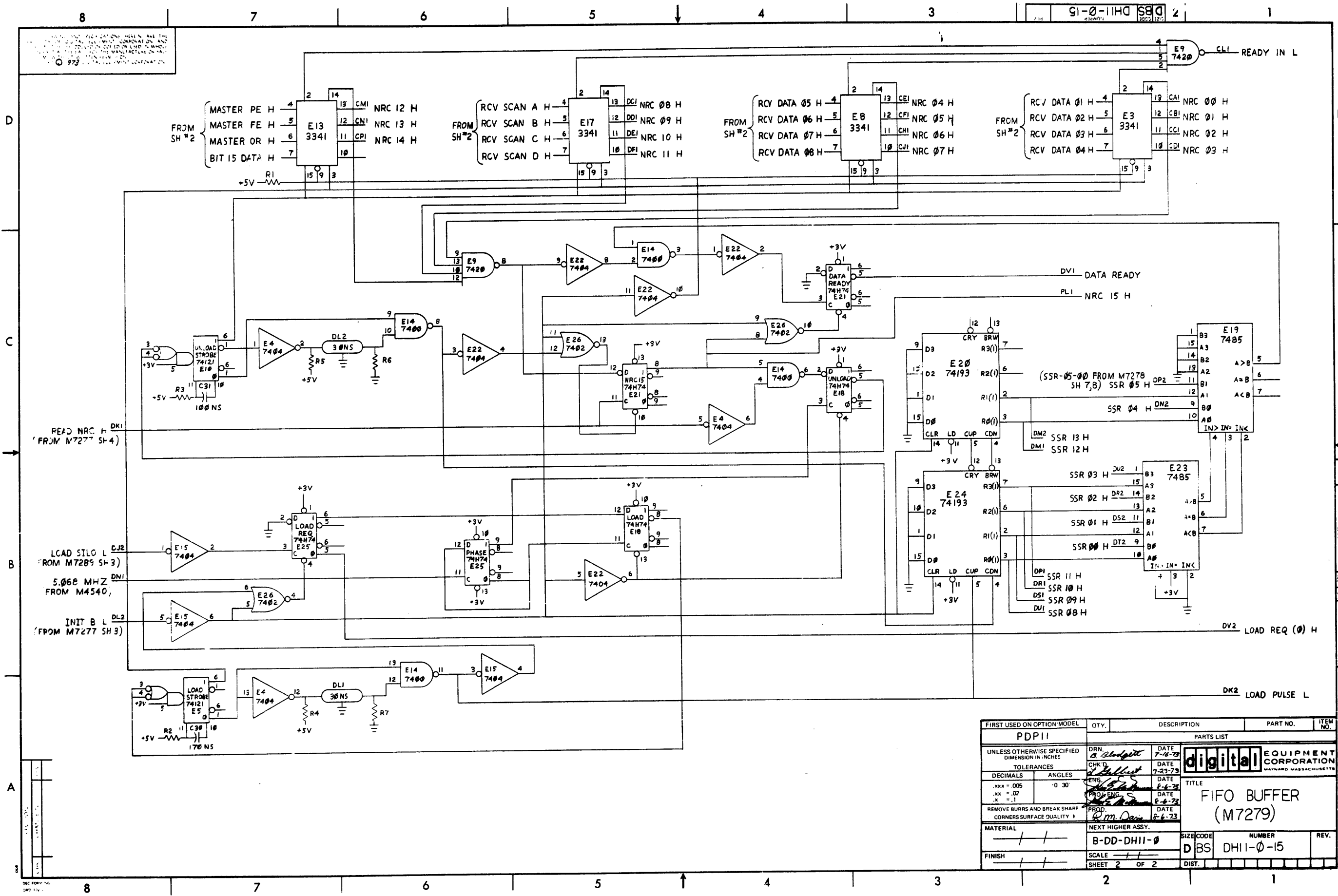
WIRE TABLE				
ITEM NO	DESCRIPTION	FROM	TO	
	AWG	COLOR	CONNECTION	CONNECTION
5	18	BLK	PI- GND	AØ4C2
6	↓	RED	PI- +5	AØ4A2
6	↓	RED	AØ4A2	BØ4A2
7	↓	ORN	PI- +15	AØ4N2
7	↓	ORN	AØ4N2	BØ4N2
8	↓	BLU	PI- -15	AØ4B2
8	18	BLU	AØ4B2	BØ4B2

1	HOLD DOWN BAR.	D-MAD-1945-19-1	2
A/R	#18 AWG STRD TEF INS WIRE BLU	9107360-66	8
A/R	#18 AWG STRD TEF INS WIRE ORN	9107360-33	7
A/R	#18 AWG STRD TEF INS WIRE RED	9107360-22	6
A/R	#18 AWG STRD TEF INS WIRE BLK	9107360-00	5
8	RIVET POP #AD43 ABS	9006509	4
1	PANEL RIGHT END	C-MD-5300830-0	3
1	PANEL ASSY, LEFT END (4 TERM)	C-IA-5409593-0-0	2
1	WIRED ASSY	D-AD-7008443-0-0	1

FIRST USED ON OPTION/MODEL DM11	QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST				
UNLESS OTHERWISE SPECIFIED	DRN.	DATE	EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS	
UNLESS OTHERWISE SPECIFIED	CHK'D.	DATE	TITLE LOGIC ASSY	
DIMENSION IN INCHES	ENG.	DATE	REV. 8	
TOLERANCES	PROJ. ENG.	DATE	CITA7008456-0-0	
DECIMALS FRACTIONS ANGLES	PROD.	DATE	SCALE 1 OF 1	
± .005 ± 1/64 ± 0°30'	REXT. HIGHER ASSY	DATE	DIST. 6	
FINAL SURFACE QUALITY	D-UA-DM11-A-Ø	DATE	MK 1	
REMOVE BURRS AND BREAK SHARP CORNERS		DATE		
MATERIAL				
FINISH				

REV.	CHANGE NO.	DATE	BY	APP.
1	1	11-24-72	V. Bastiani	
2	2	11-24-72	V. Bastiani	
3	3	11-24-72	V. Bastiani	
4	4	11-24-72	V. Bastiani	





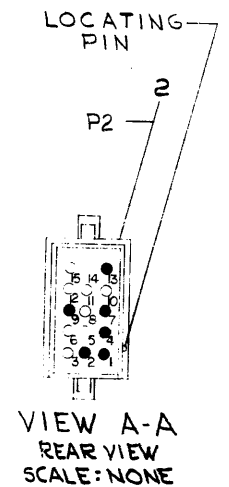
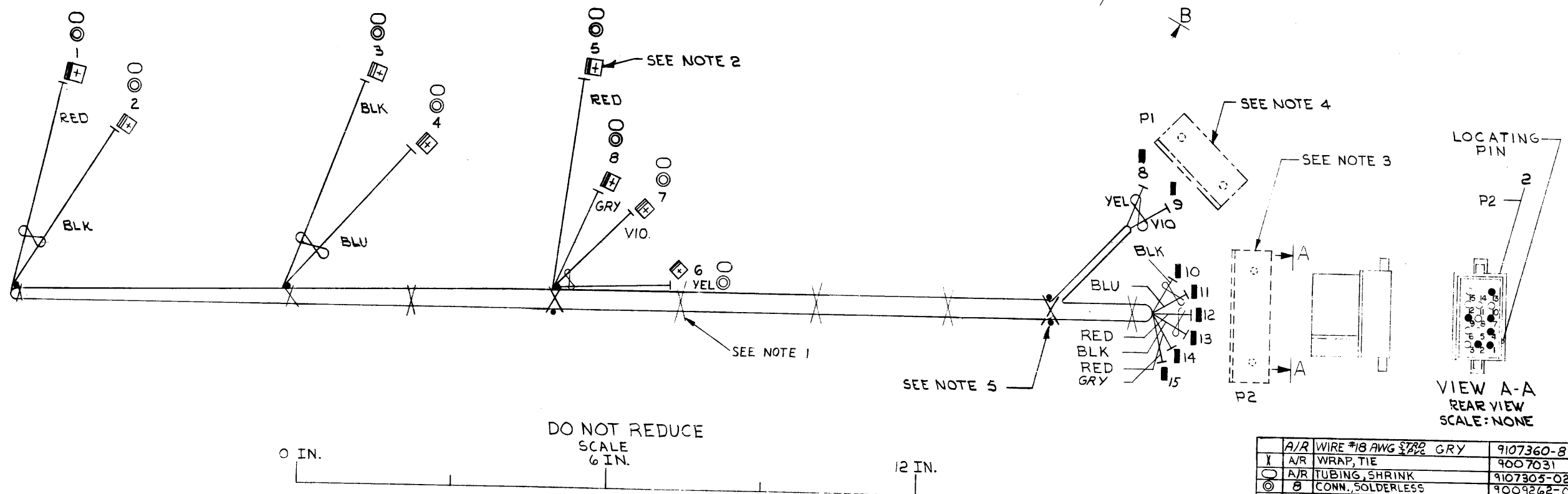
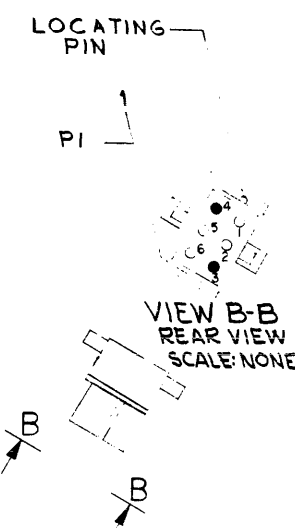
FIRST USED ON OPTION MODEL		QTY.	DESCRIPTION	PART NO.	ITEM NO.
PDPII					
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES		DRN	DATE	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS	
TOLERANCES		CHK'D	DATE		
DECIMALS	ANGLES	ENG.	DATE	TITLE	
.xxx = .005	.0 30'	PROV. ENG.	DATE		
.xx = .02		PROD.	DATE	FIFO BUFFER (M7279)	
.x = .1		PROV. ENG.	DATE		
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY 1		PROV. ENG.	DATE	REV.	
MATERIAL		NEXT HIGHER ASSY.	DATE		
FINISH		B-DD-DH11-0	DATE	DIBS DH11-0-15	
		SCALE	DATE		
		SHEET 2 OF 2	DATE	DIST.	
			DATE		

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WIRE LIST									
ITEM NO	AWG	COLOR	FROM		TO		WITH	SIGNAL	
			POINT	CONNECTION	POINT	CONNECTION			
5	14	RED	1	---	8,9	12	P2-4	3	+5V
	TWP	BLK	2	---	8,9	13	P2-7	3	GND
6	14	BLK	3	---	8,9	10	P2-9	3	GND
	TWP	BLU	4	---	8,9	11	P2-13	3	-15V
4	14	RED	5	---	8,9	14	P2-1	3	+5V
7	18	YEL	6	---	8,9	8	P1-4	3	AC LO
	TWP	VIO	7	---	8,9	9	P1-3	3	DC LO
11	18	GRY	8	---	8,9	15	P2-2	3	+15V

0-0-1996002 V11D 2

- NOTES:
- USE TIE WRAPS(X) ITEM 10 APPROXIMATELY EVERY THREE(3) INCHES WHEN NECESSARY, AND AT EVERY BREAK-OUT POINT.
 - ATTACH MALE FASTON DEC * 9008219-0 WITH WOOD SCREWS (8 PLACES).
 - USE CONN. BRKT C-MD-9305761-H15-0. MOUNT WITH WOOD SCREWS. USE MATING CONN. 1209350-15
 - USE CONN. BRKT C-MD-9305761-H6-0. MOUNT WITH WOOD SCREWS. USE MATING CONN. 1209350-06
 - DOT (•) INDICATES NAIL LOCATIONS FOR ASSEMBLY USE ONLY. COVER NAILS WITH SHRINK TUBING TO PREVENT CUTTING HARNESS.

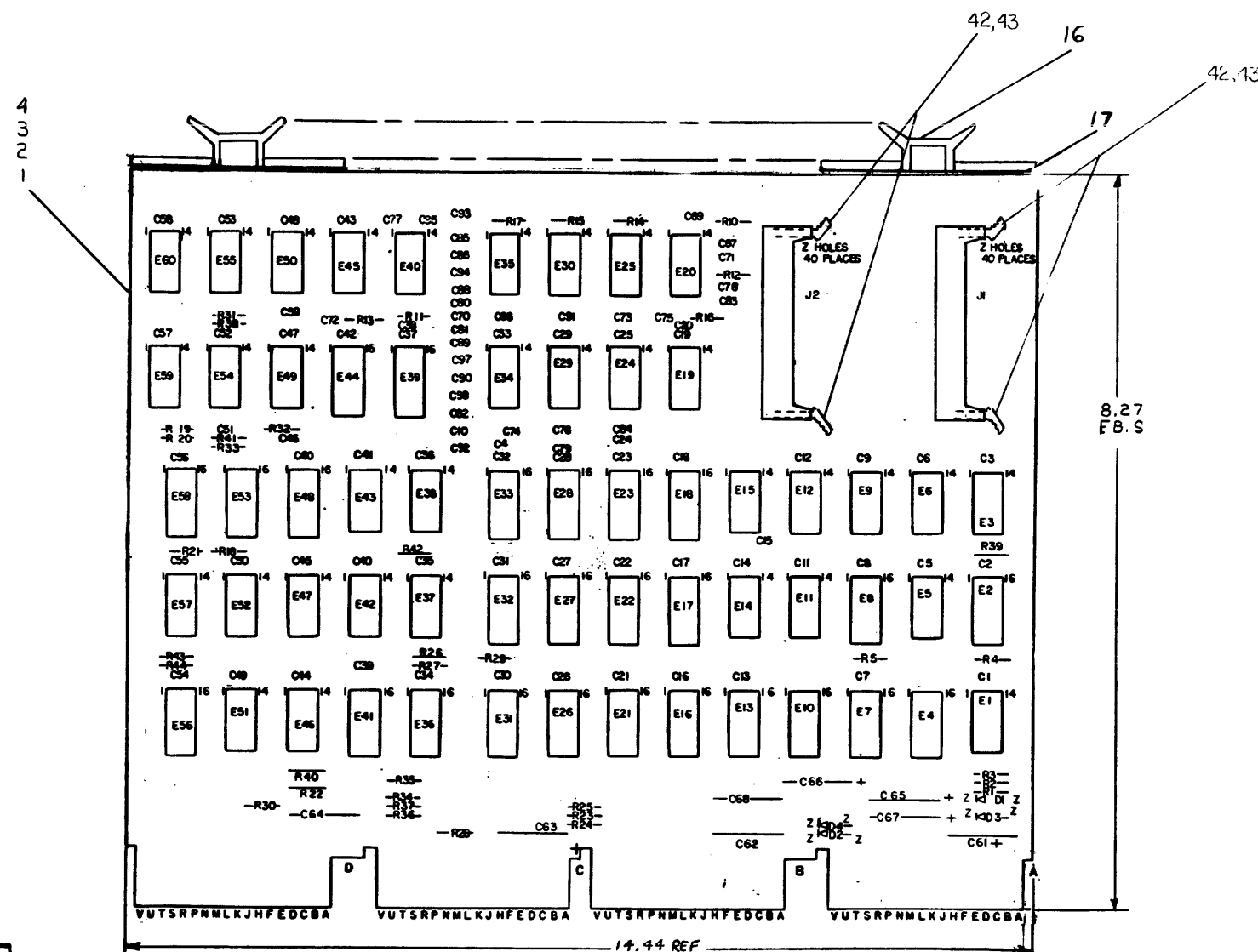


A/R	WIRE #18 AWG 2720 GRY	9107360-88	11
Y	A/R WRAP, TIE	9007031	10
○	A/R TUBING, SHRINK	9107305-02	9
⊙	CONN. SOLDERLESS	9009262-0	8
	A/R WIRE #18 TWP YEL/VIO	9107430-47	7
	A/R WIRE #14 TWP BLK/BLU	9107440-06	6
	A/R WIRE #14 TWP BLK/RED	9107440-02	5
	A/R WIRE #14 AWG RED	9107370-22	4
	8 PIN, MALE	1209378-00	3
	1 HOUSING, CONN. 15 PIN	1209351-13	2
	1 HOUSING, CONN. 6 PIN	1209351-06	1

FIRST USED ON OPTION/MODEL		QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST					
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES		DRN. <i>Amade</i>	DATE <i>7/23/75</i>	digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS	
TOLERANCES		ENG. <i>V. B. B.</i>	DATE <i>11/25/75</i>	TITLE OPTION HARNESS DH11	
DECIMALS	ANGLES	PROJ. ENG. <i>W. B. B.</i>	DATE <i>11/25/75</i>	SIZE CODE DIA	
.xxx = .005	±0° 30'	PROD. <i>W. B. B.</i>	DATE <i>10/23/75</i>	NUMBLR 7009561-0-0	
.xx = .02				REV. C	
.x = .1				SHEET 1 OF 1	
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY 1		NEXT HIGHER ASSY.		DIST.	
MATERIAL SEE PARTS LIST		SCALE 1/1			
FINISH					

REV	CHANGE NO	DATE	BY	CHK
1	7009561-00001	A	V. BOLEN	
2	7009561-00002	C	H. KWAN	
3	7009561-00003	H		
4	7009561-00004			
5	7009561-00005			
6	7009561-00006			
7	7009561-00007			
8	7009561-00008			

1. FOR $-15V$ TO $-10V$ AND $+15V$ TO $+10V$
SEE SHEET 7 OF 7
2. THE SIGNALS "SEC TX" AND "SEC RX" REFER TO ASYNCHRONOUS OPERATION ONLY.
WHEN THE MODULE IS USED IN A SYNCHRONOUS APPLICATION THE SIGNALS MAY
BE USED AS "NEW SYNC" AND "DATA SET RDY" FOR THAT LINE.



REF		X-Y COORDINATE HOLE LOCATION	K-CO-87000-B-4	1
REF		ASSY/DRILL HOLE LAYOUT	D-AH-W7000-B-5	2
REF		MODULE ECO HISTORY	B-MH-W7000-B-6	3
1		ETCHED CIRCUIT BOARD	5010004	4
56	C1-3,5,9,11-58	CAP .01 UF, 100V, $\pm 20\%$	1001610-00	5
33	C4,10,59,89-98	CAP 470 PF, 100V, $\pm 5\%$	1000024	6
1	C80	CAP 82 PF, 100V, $\pm 5\%$	1000015	7
8	C61 THRU C80	CAP 6.8 UF, 35V, $\pm 10\%$	1005306	8
4	D1,2,3,4	DIODE 1N4733A ZENER	1109943	9
2	J1,J2	CONNECTOR 40 PIN	1209941	10
28	R1-4,18-30,32-38,40-43	RES. 750 1/4W 5%	1301401	11
1	R31	RES. 220 1/4W 5%	1300271	12
8	R10-17	RES. 33K 1/4W 10%	1300510	13
4	R6,7,8,9	RES. 330 1/2W 5%	1300280	14
1	R44	RES. 330 1/4W 5%	1300295	15
4		HANDLE FLIP CHIP	9008337-08	16
8		EYELET	9006732	17
1	E50	I.C. DEC 7474	1905547	18
8	E19,20,24,25,29,30,34,35	I.C. DEC 1489L	1910323	19
8	E17,18,22,23,27,28,32,33	I.C. DEC 74151	1909936	20
8	E4,7,10,13,16,21,26,31	I.C. DEC 74175	1910851	21
6	E5,6,9,11,12,15	I.C. DEC 1488	1910322	22
2	E14,49	I.C. DEC 7410	1905576	23
1	E2	I.C. DEC 7442	1910046	24
2	E1,42	I.C. DEC 7417	1909829	25
1	E8	I.C. DEC 74123	1910436	26
4	E3,38,54,60	I.C. DEC 8081	1909705	27
2	E36,53	I.C. DEC 8266	1909934	28
2	E41,44	I.C. DEC 8838	1911117	29
1	E46	I.C. DEC 8640	1911469	30
1	E51	I.C. DEC 7416	1909928	31
1	E56	I.C. DEC 7489	1910396	32
1	E37	I.C. DEC 74197	1910035	33
2	E45,47	I.C. DEC 7400	1905575	34
1	E52	I.C. DEC 7408	1910155	35
2	E55,57	I.C. DEC 8815	1908713	36
2	E40,43	I.C. DEC 7404	1909686	37
1	E48	I.C. DEC 8271	1909615	38
2	E39,58	I.C. DEC 4015	1910087	39
1	E59	I.C. DEC 7486	1910011	40
2	R5,39	RES. 10K,1/4W, 5%	1209941-05	41
2		LEFT LATCH	1209941-05	42
2		RIGHT LATCH	1209941-05	43
A/R		WIRE 30 AWG	9105740-55	44

QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITE NO.
-----	-----------------	-------------	----------	---------

	PARTS LIST
--	------------

[illegible]

DEC NO.	EIA NO.	SCALE	NONE	SIZE	CODE	NUMBER	REV.
CONVERSION CHART		SHEET	OF 7	D	C	17808-0-1	J
				DIST.			

DEC	4015	8	16
DEC	8271	8	16
DEC	7489	8	16
DEC	8640	1	8
DEC	8266	8	16
DEC	74123	8	16
DEC	7442	8	16
DEC	74175	8	16
DEC	74151	8	16
IC TYPE		GND	+ 5V
GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE			
IC PIN LOCATIONS			

1	AMMINGTON, JOTAN 78	H	572	MT8008-000004					
	R. HARRINGTON			J. Mc NAMARA					
	P. Jones JAN 18			H. Dymally 6-7-76					
2	MT8008-000005 J	F	580	MT8008-000003					
	6-7-76			J. McINTYRE					
	6-7-76			H. Dymally 4-9-76					
3	MT8008-000006 E		462	MT8008-000002					
	6-7-76			W. FANAZICK					
	6-7-76			(19) 1-31-75					
4	MT8008-000007 D	C	19	MT8008-000001					
	ORIGINATED	REV							
CHK	CHANGE NO.	REV							
		REVISIONS							

DEC NO.	EIA NO.	DEC NO.	EIA NO.
SEMICONDUCTOR CONVERSION CHART			

DRN.	<i>E. Wilson</i>	DATE	<i>7/15/74</i>	digital EQUIPMENT CORPORATION NAYNARD MASSACHUSETTS
CH'D	<i>W. Wilson</i>	DATE	<i>7-15-74</i>	
ENG.	<i>W. Wilson</i>	DATE	<i>7-15-74</i>	
PROJ. ENG.	<i>W. Wilson</i>	DATE	<i>7-15-74</i>	
PROD.	<i>W. Wilson</i>	DATE	<i>8-30-74</i>	
NEXT HIGHER ASSY				
SCALE NONE				
SHEET OF 7		SIZE CODE	NUMBER	REV. J
		DIST.		

NOTE:

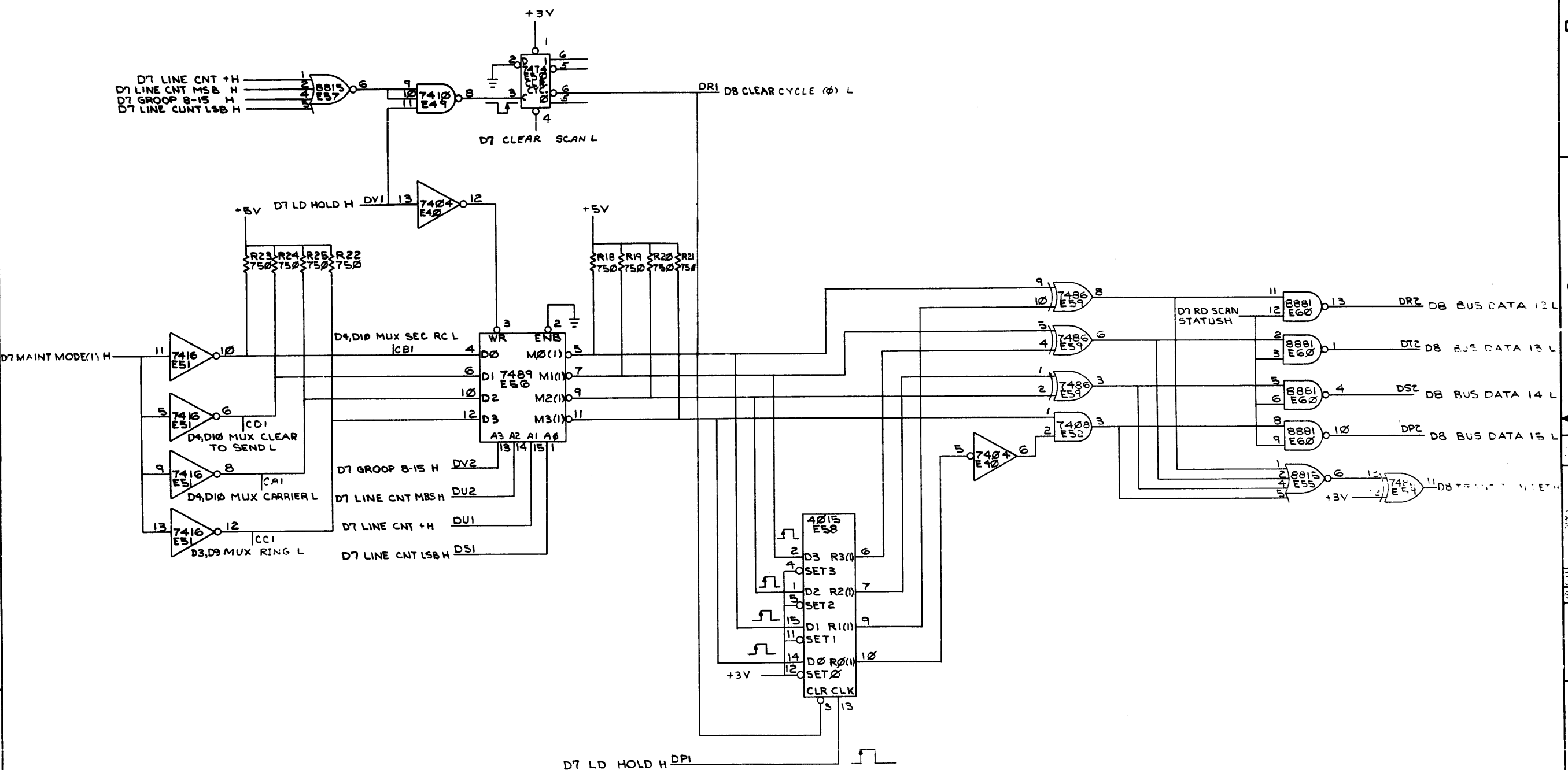
The diagram illustrates a complex digital circuit with multiple functional blocks and signal paths:

- Inputs and Outputs:** The circuit features numerous pins labeled with names like "MUX SEC TX L", "MUX RQ TO SEND L", "MUX TERM RDY L", "MUX LINE EN L", "SELECT 2 H", "IN HIGH H", "OUT LOW H", "SCAN EN(1) H", "MUX CLEAR TO SEND L", "MUX RING L", "MUX CARRIER L", "MUX SEC RX L", "D7 RD SCAN STATUS H", "DI OUT LOW H", "BUS DATA 04 L", "BUS DATA 11 L", "BUS DATA 10 L", "BUS INITIALIZE L", "INT EN L", "DN2", "D7 INT A H", "INTR EN(1) H", "DONE(1) H", "LINE INCR H(DN)", "DT MAINT MODE(1) H", "DT CLEAR SCAN L", "DB CLR CYCLE(0) L", "INH CLK L", "EXT CLOCK L", "D7 LD HOLD H", "DPH", "LINE INCR H DPH", "OUT WRITE H IDL", "INTR TEST H IDMI", "DB TRANS DET H", and "DII MUX LINE EN L".
- Internal Logic:** The circuit includes several logic gates (AND, OR, NOT), multiplexers (8266, 8271), shift registers (SHF), counters (8271), and comparators (8815). It also contains several 7410 (hex inverters), 7416 (monostable multivibrators), and 7417 (Schmitt triggers).
- Buses and Data Paths:** Multiple data buses are shown, including "BUS DATA 03 L", "BUS DATA 02 L", "BUS DATA 01 L", "BUS DATA 00 L", "BUS DATA 04 L", "BUS DATA 11 L", "BUS DATA 10 L", "BUS DATA 05 L", "BUS DATA 06 L", "BUS DATA 07 L", and "BUS DATA 09 L".
- Power and Timing:** The circuit is powered by +5V and +3V sources. Timing components include resistors (R37, R36, R35, R34, R42, R41, R38, R40, R33, R31) and capacitors (C59, C60, C58, C57, C56, C55, C54, C53, C52, C51, C50, C49, C48, C47, C46, C45, C44, C43, C42, C41, C40, C39, C38, C37, C36, C35, C34, C33, C32, C31, C30, C29, C28, C27, C26, C25, C24, C23, C22, C21, C20, C19, C18, C17, C16, C15, C14, C13, C12, C11, C10, C9, C8, C7, C6, C5, C4, C3, C2, C1, C0).
- Notes and Revisions:** The diagram includes a note "* SEE NOTE 2." and a section for "REVISIONS" at the bottom left.

REVISIONS		
CHK	CHANGE NO.	REV.

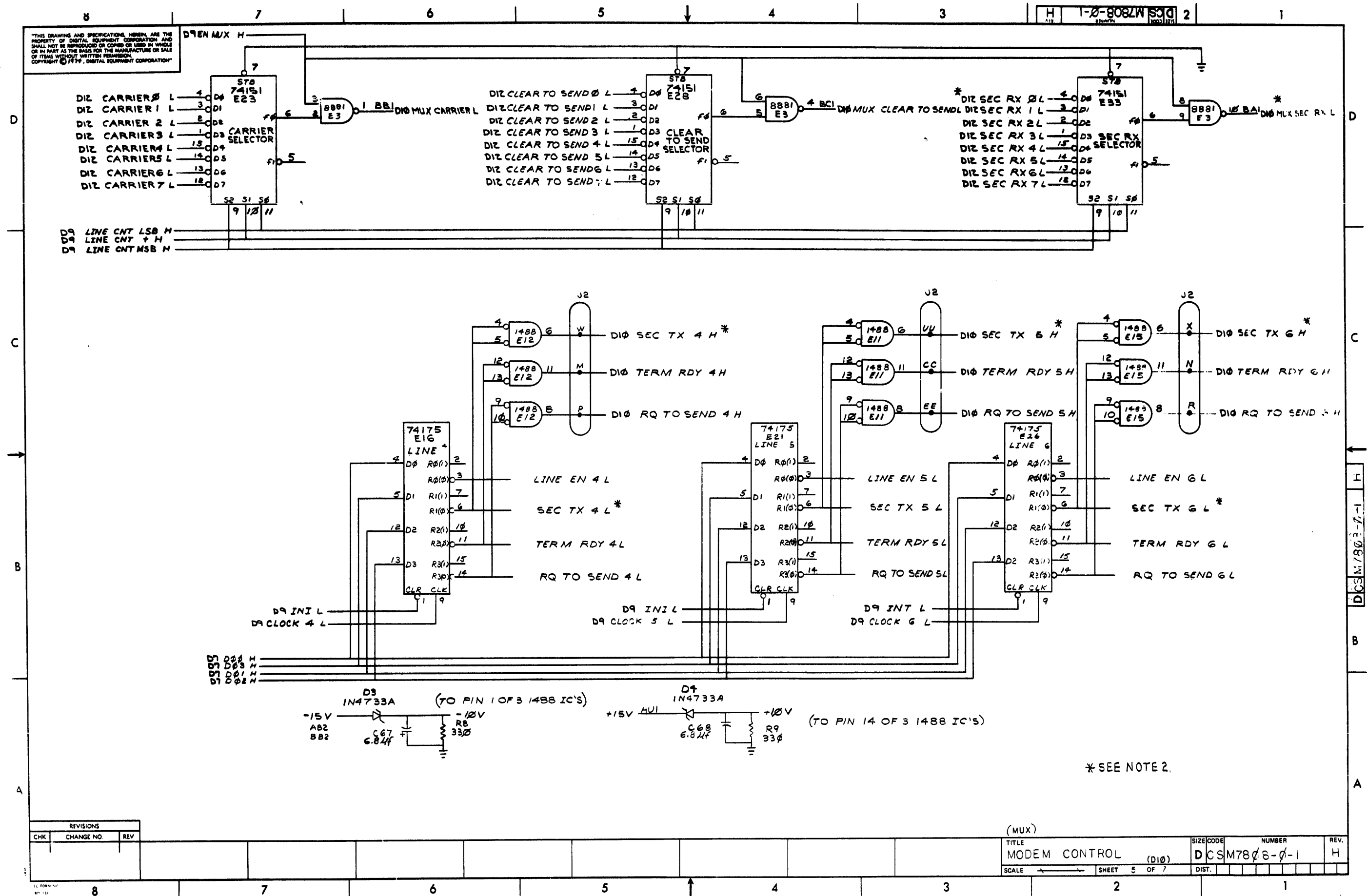
TITLE MODEM CONTROL (07)		SIZE D	CODE CS	NUMBER M7808-0-1		REV. J
SCALE 1/1	SHEET 2	OF 7		DIST.		

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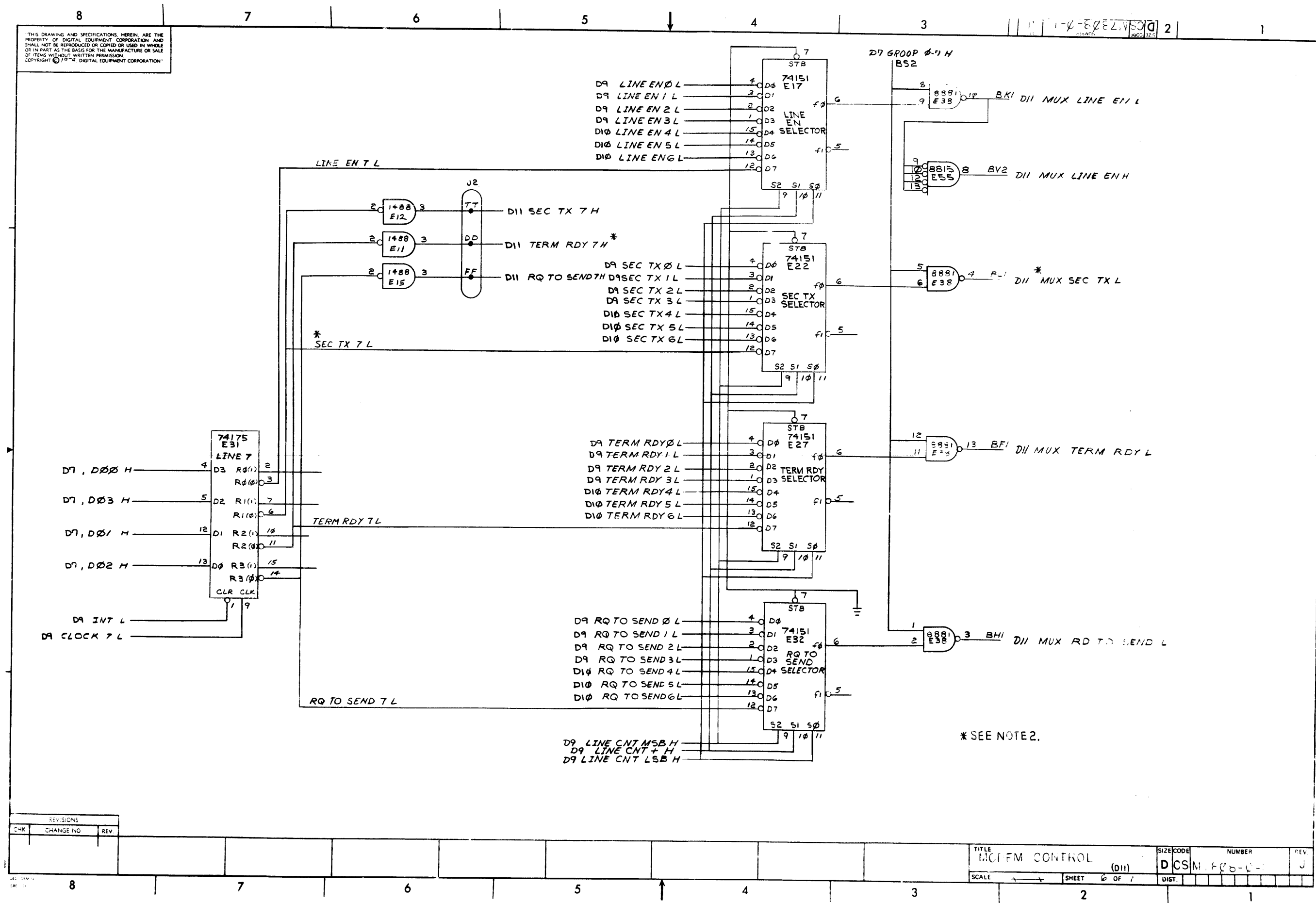


REVISIONS		
CHK	CHANGE NO.	REV.

TITLE		MODEM CONTROL (DB)	SIZE CODE		D CS	NUMBER		M7808-0-1	REV.		
SCALE			SHEET		3	OF		7	DIST.		



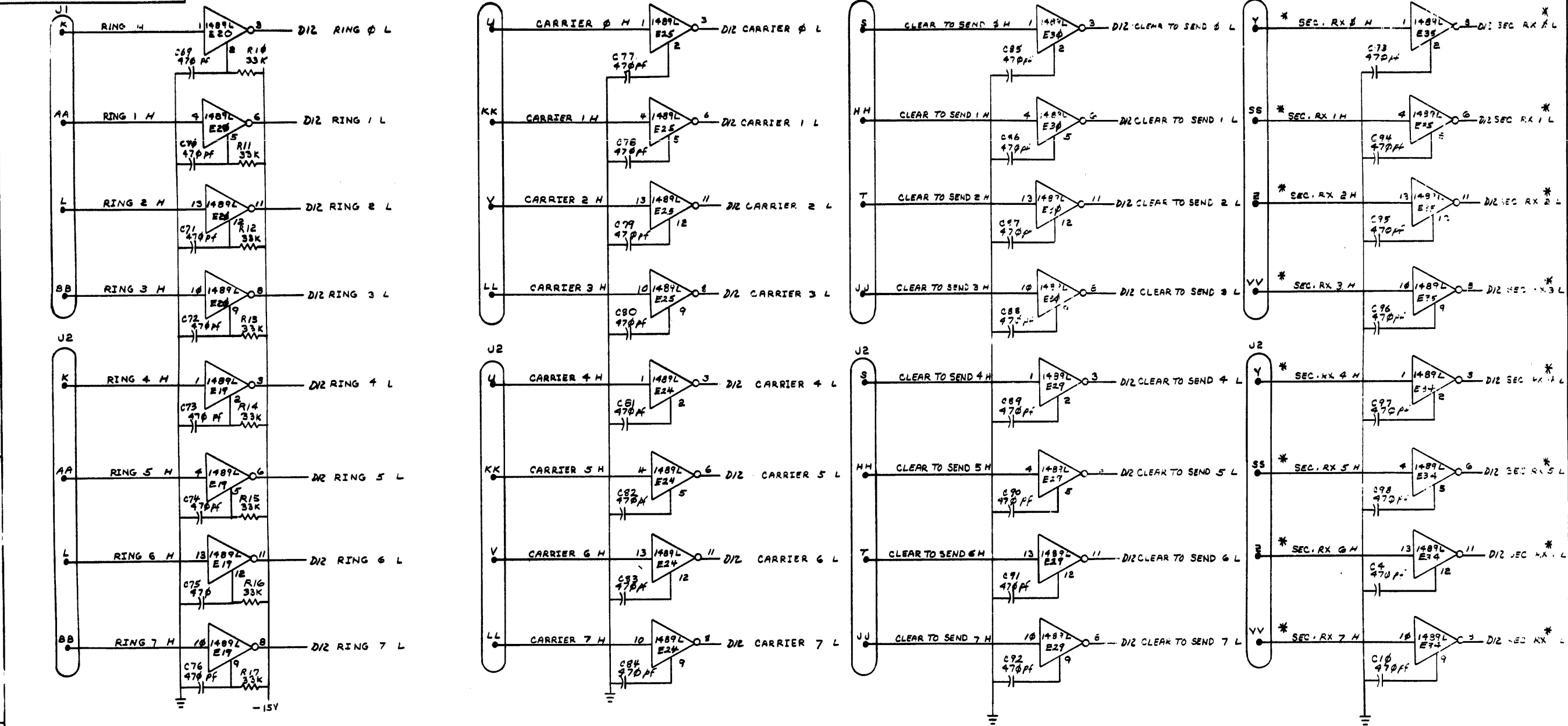
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REVISIONS		
CHK	CHANGE NO	REV.

TITLE MICEM CONTROL (D11)		SIZE CODE DCS	NUMBER PCB-0-1	REV. J
SCALE	SHEET 6 OF 7	DIST.		

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REVISIONS												
CHK	CHANGE NO	REV.										

(EIA LEVEL CONVERTERS)

TITLE	MODEM CONTROL (D12)	SIZE/CODE	D	CSM7808-4-1	NUMBER		REV.	
SCALE		SHEET	7	OF 7	DIST.			

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NOTES:

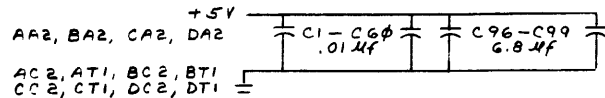
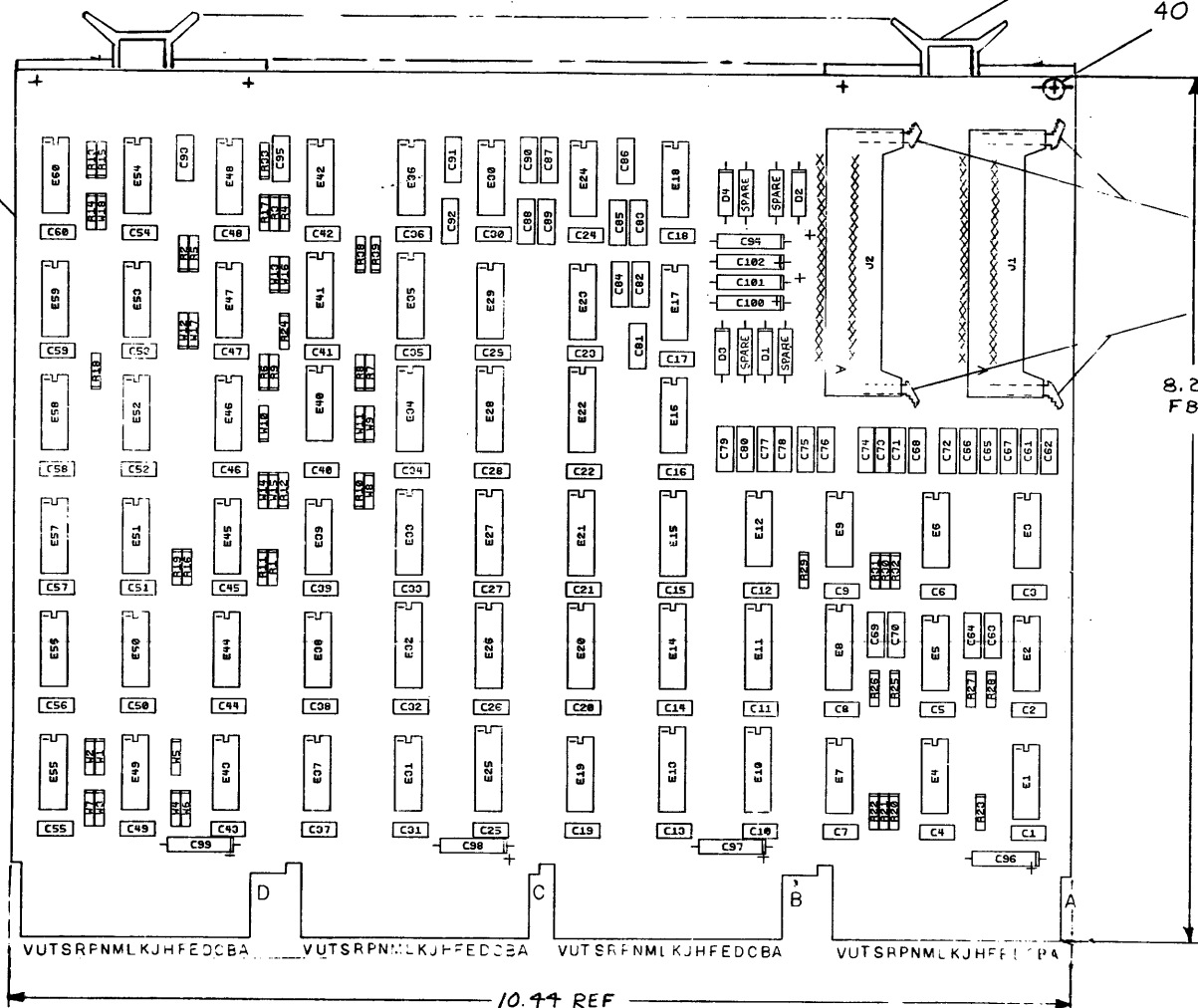
- ALL UNUSED PINS ON J1, J2 GO TO GND
- THE SIGNALS SEC TX AND SEC RX REFER TO ASYNCHRONOUS OPERATION ONLY. WHEN THE MODULE IS USED IN A SYNCHRONOUS APPLICATION THE SIGNALS MAY BE USED AS "NEW SYNC" AND "DATA SET RDY" FOR THAT LINE.

JUMPER TABLE

JUMPER	BIT
W1	D08
W2	D02
W3	D03
W4	D06
W5	D07
W6	D05
W7	D04
W8	A12
W9	A09
W10	A08
W11	A10
W12	A04
W13	A05
W14	A11
W15	A03
W16	A06
W17	A07

JUMPER REMOVED
INTERRUPT
VECTOR = 0

JUMPER REMOVED
DEVICE
SELECT = 1



REF	X-Y COORDINATE HOLE LOCATION	K-CO-M7807-B-4	1
REF	ASSY/DRILLING HOLE LAYOUT	D-AH-M7807-B-5	2
REF	MODULE ECO HISTORY	B-WH-M7807-B-6	3
1	ETCHED CIRCUIT BOARD	5010803	4
8	C84, C86-C102	CAP 6.8 UF 35V 10%	5
60	C1-C60	CAP .01 UF 100V 20%	6
33	C61-C93	CAP 470 MMF 100V 5%	7
1	C95	CAP 330 PF 100V 5%	8
4	D1, D2, D3, D4	DIODE 1N4733A	9
16	R1-R13, R15, R17, R18	RES 1K 1/4W 5%	10
1	R14	RES 100 1/4W 5%	11
1	R33	RES 47 1/4W 5%	12
1	R19	RES 100 1/4W 5%	13
5	R20-R23, R39	RES 750 1/4W 5%	14
8	R25-R32	RES 33K 1/4W 10%	15
1	R16	RES 300 1/4W 5%	16
4	R34, R36, R38, R39	RES 330 1/4W 5%	17
1	E52	I.C. DEC 7400	18
1	E4	I.C. DEC 7417	19
8	E14, E18, E23, E25, E36, E42	I.C. DEC 1488L	20
8	E3, 5, 6, 9, 12, 17, 24, 30	I.C. DEC 1488L	21
8	E8, 11, 14, 15, 20, 21, 22, 26	I.C. DEC 74151	22
8	E10, 13, 25, 28, 32, 33, 34, 35	I.C. DEC 74175	23
1	E19	I.C. DEC 7410	24
1	E27	I.C. DEC 7442	25
6	E1, E7, E48, E51, E55, E60	I.C. DEC 8001	26
2	E56, E59	I.C. DEC 7400	27
7	E31, E37, E43, E45, E46, E53, E54	I.C. DEC 8640	28
1	E58	I.C. DEC 7474	29
1	E2	I.C. DEC 74H04	30
1	E44	I.C. DEC 74H00	31
3	E39, E40, E47	I.C. DEC 8242	32
1	E41	I.C. DEC 74123	33
1	E48	I.C. DEC 74H74	34
1	E38	I.C. DEC 8815	35
2	E50, E57	I.C. DEC 7402	36
4		HANDLE FLIP CHIP	37
2	J1, J2	40 PIN HEADER	38
18	W1-W18	JUMPER (INSULATED)	39
6		EYELET HANDLE	40
1	R38	RES 330 1/4W 5%	41
2		LEFT LATCH	42
2		RIGHT LATCH	43
1	R24	RES. 10K, 1/4W, 5%	44

QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST				
ETCH BOARD REV D				
DRN DATE 11/27/74				
CHD DATE 8/14/74				
ENG DATE 7-30-74				
PROJ ENG DATE 6-20-74				
PROD DATE 5-30-74				
NEXT HIGHER ASSY				
TITLE				
BUS CONTROL & MUX				
SIZE CODE NUMBER REV				
D CSM7807-B-1 H				
SCALE 1 OF 7				
SHEET 1 OF 7				
DIST.				

FIRST USED ON OPTION MODEL

ETCH BOARD REV D

DRN DATE 11/27/74

CHD DATE 8/14/74

ENG DATE 7-30-74

PROJ ENG DATE 6-20-74

PROD DATE 5-30-74

NEXT HIGHER ASSY

TITLE

BUS CONTROL & MUX

SIZE CODE NUMBER REV

D CSM7807-B-1 H

SCALE 1 OF 7

SHEET 1 OF 7

DIST.

DEC. NO. EIA NO. DEC. NO. EIA NO.

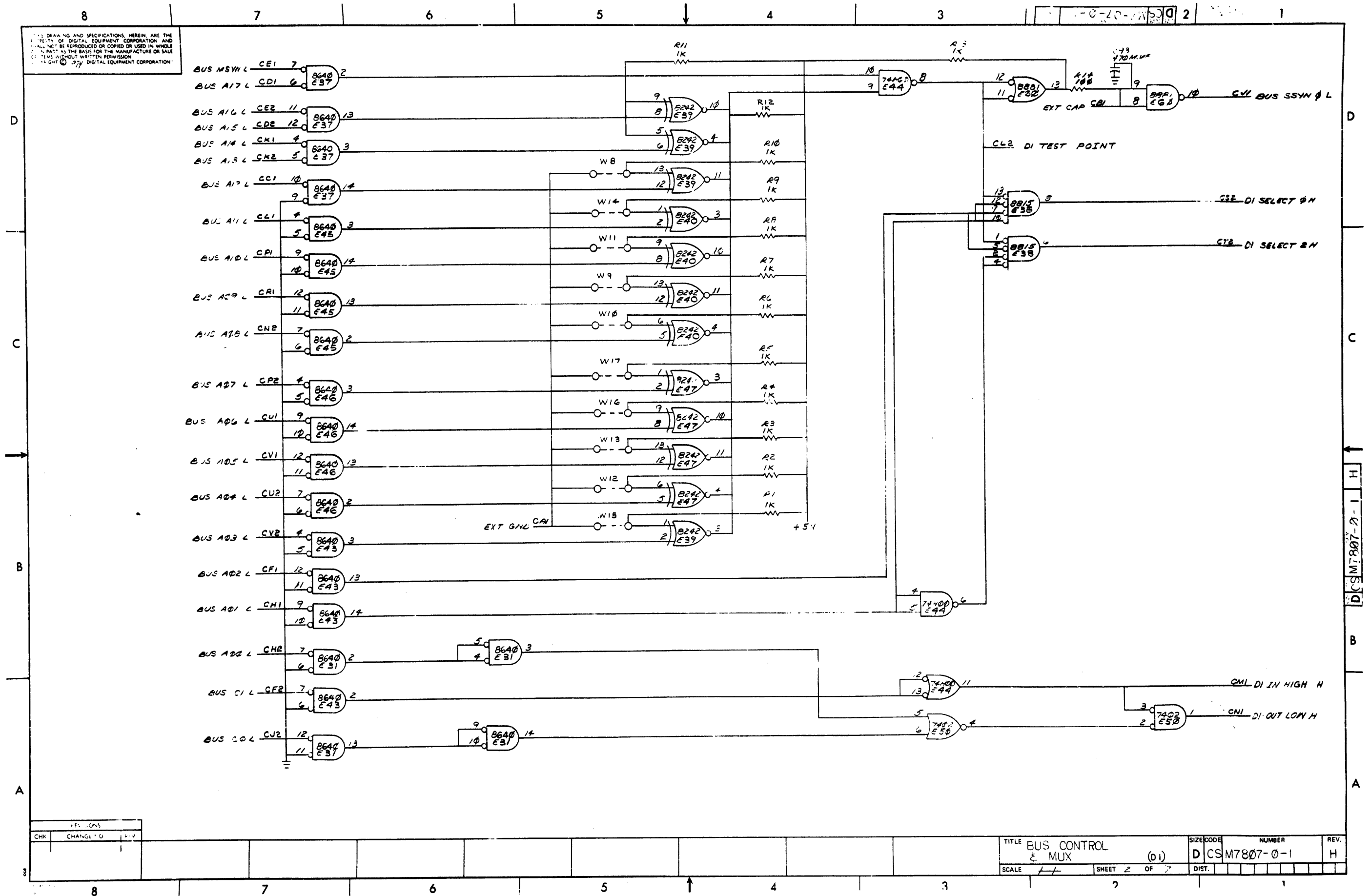
SEMICONDUCTOR CONVERSION CHART

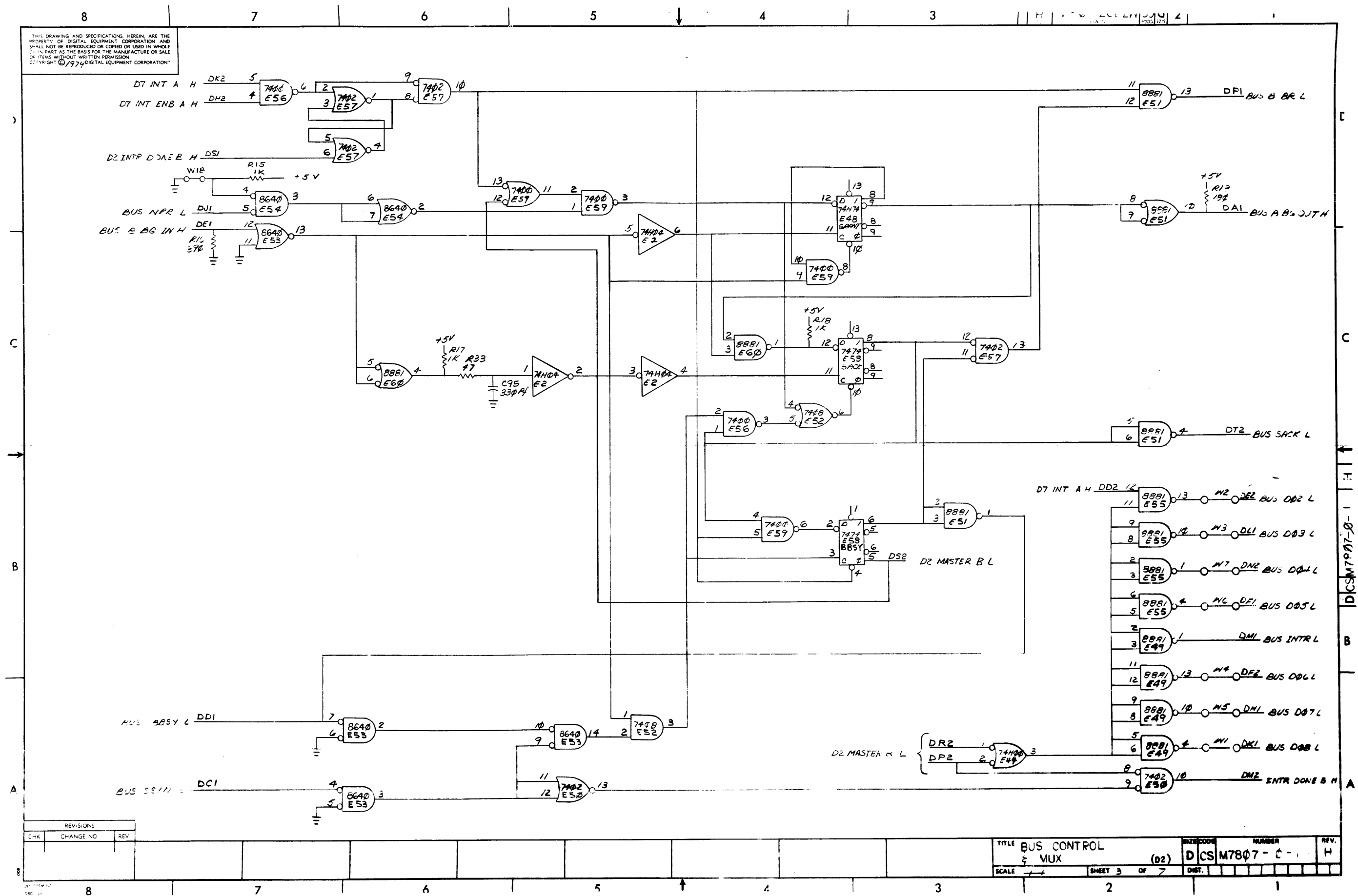
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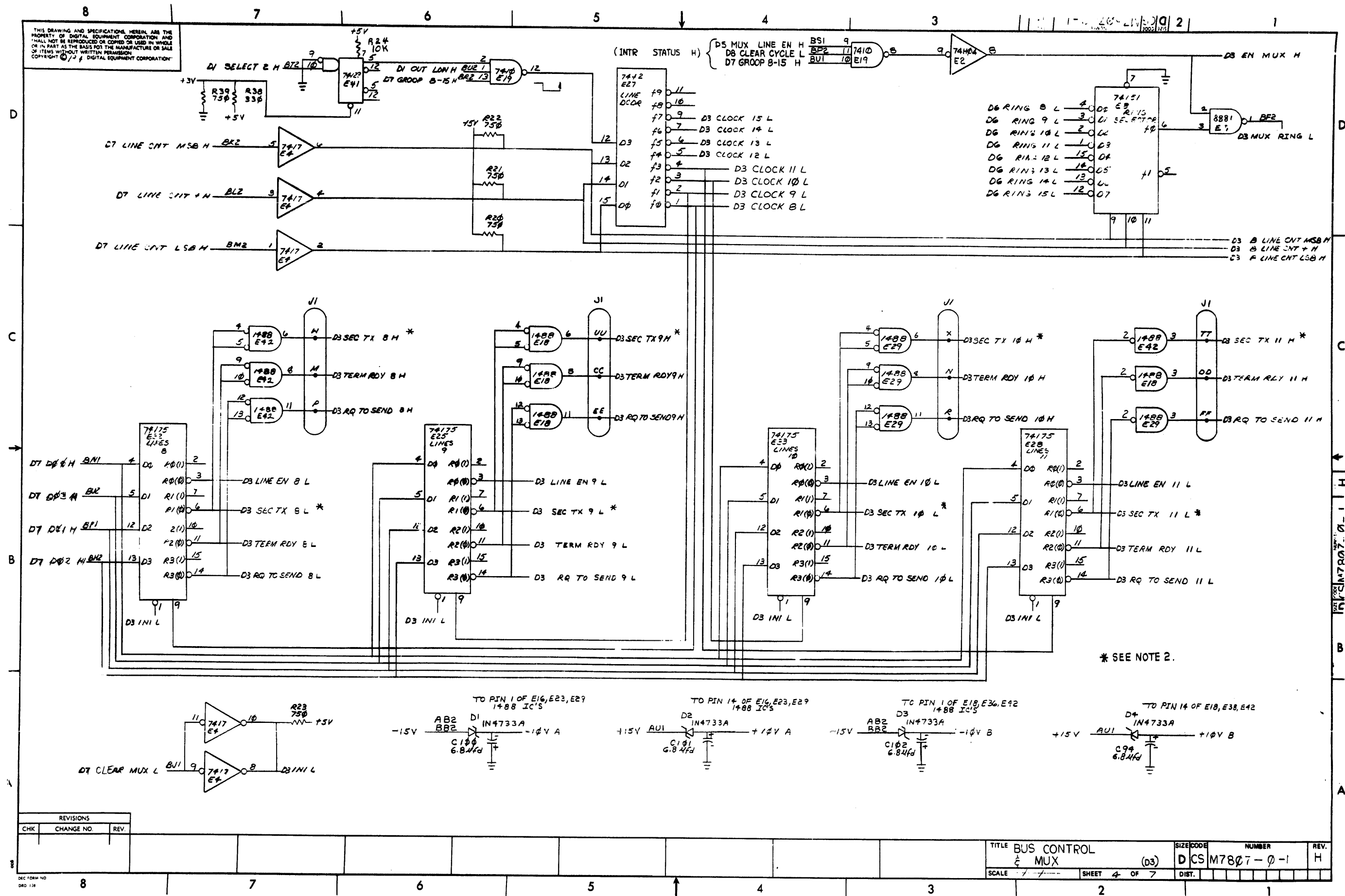
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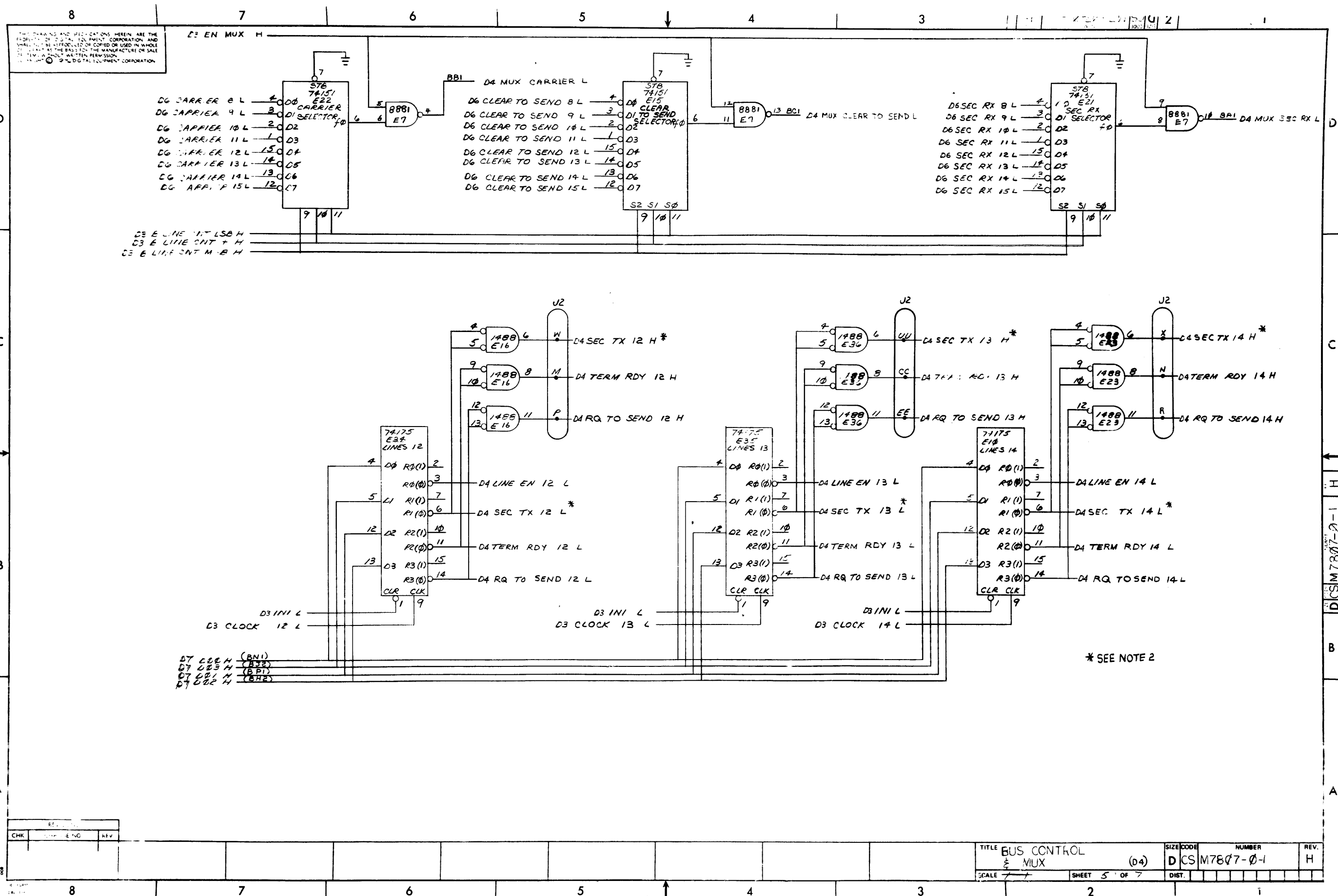
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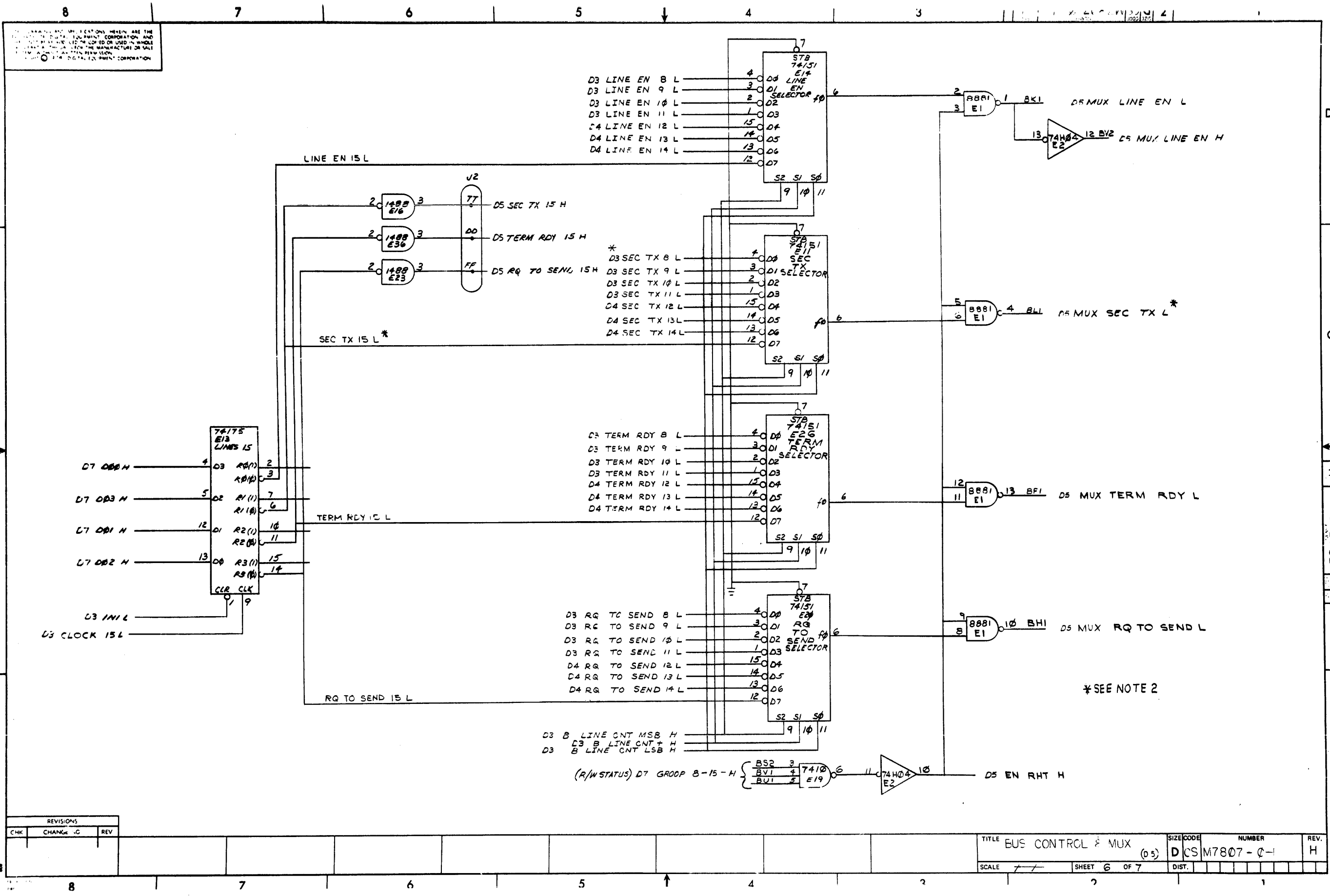
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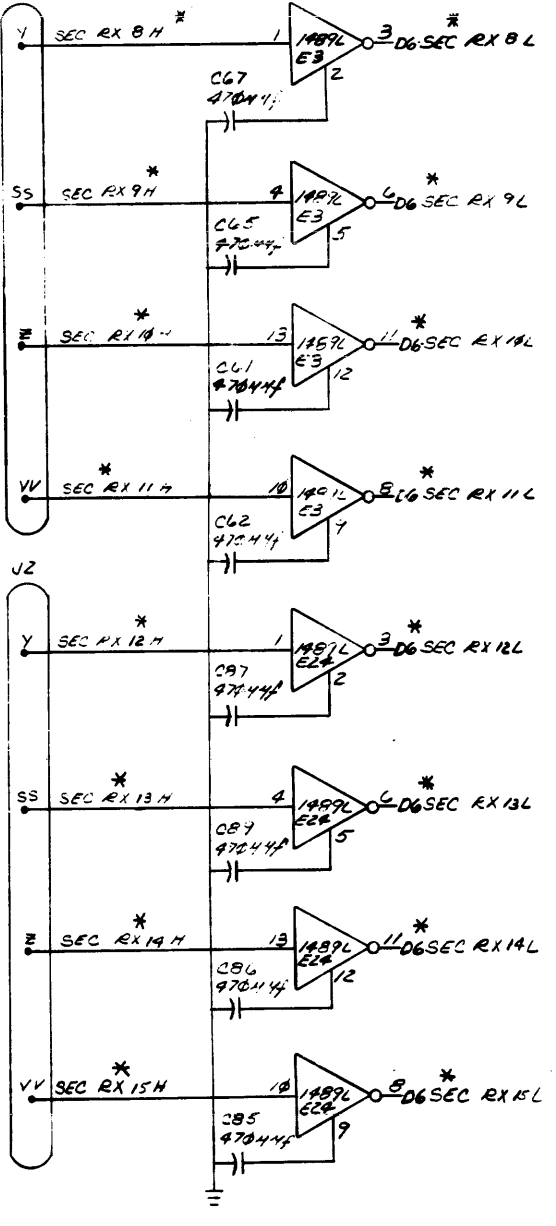
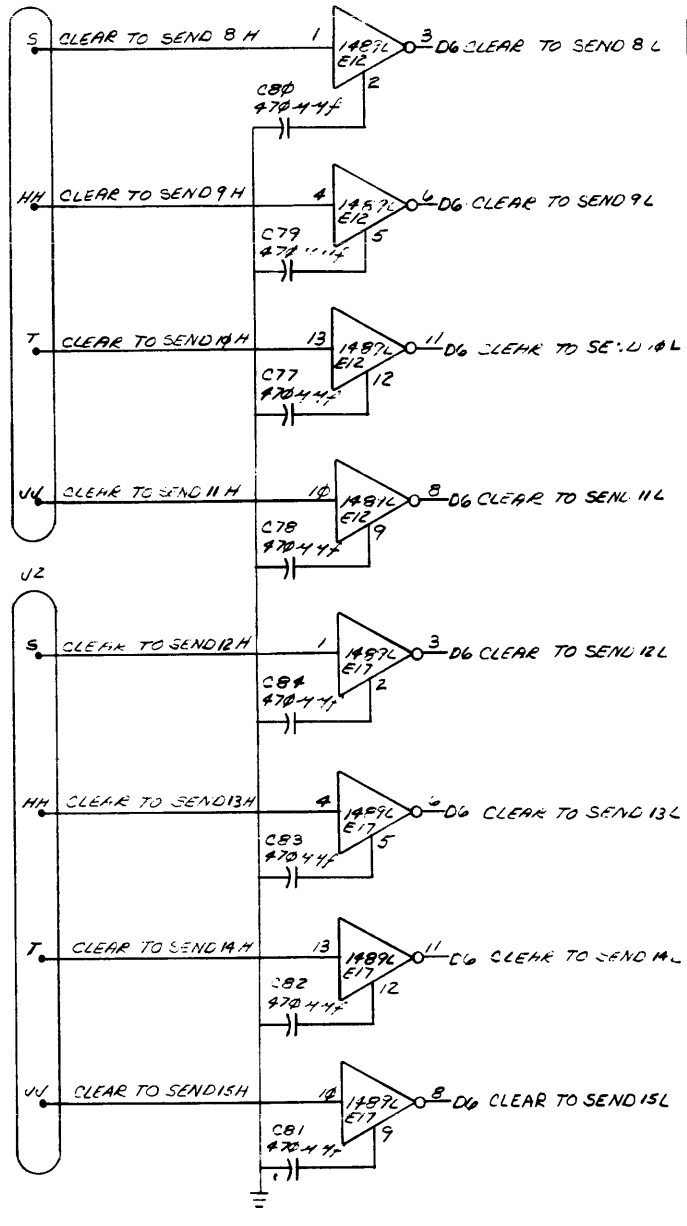
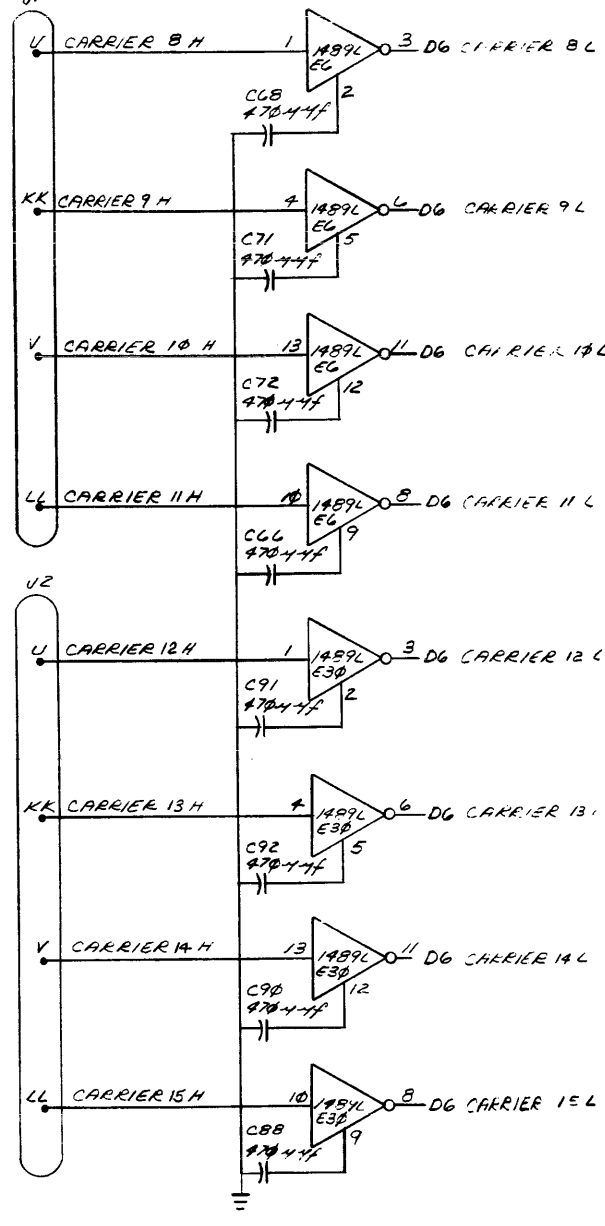
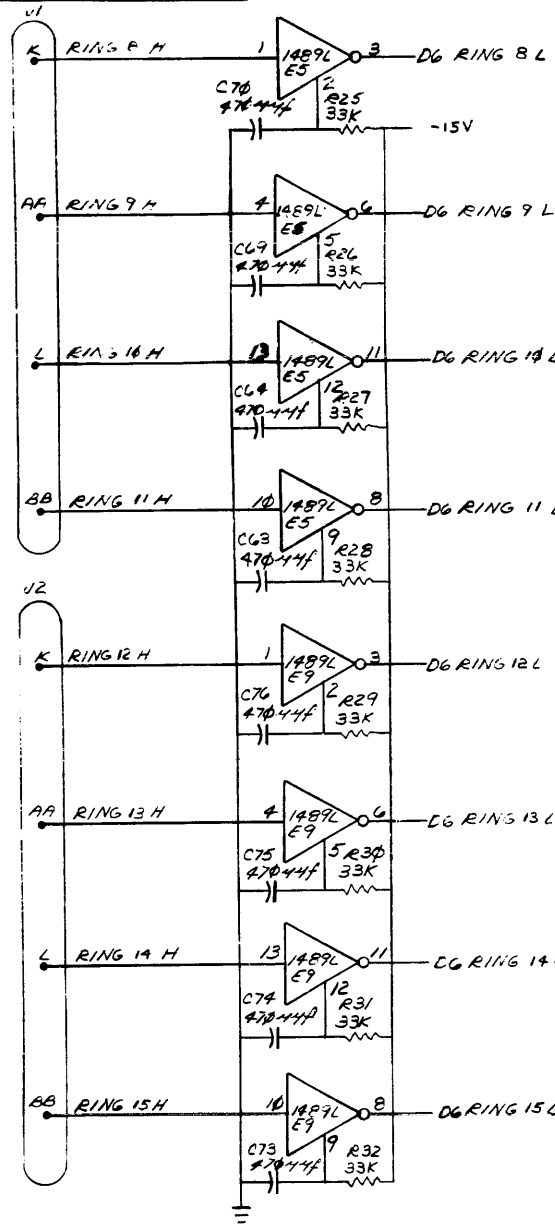




REVISIONS		
CHK	CHANGE	REV

TITLE			SIZE		CODE		NUMBER			REV.			
BUS CONTROL & MUX			(05)		D		CS		M7807-Q-1			H	
SCALE			SHEET		OF		DIST.						
7-7			6		7								

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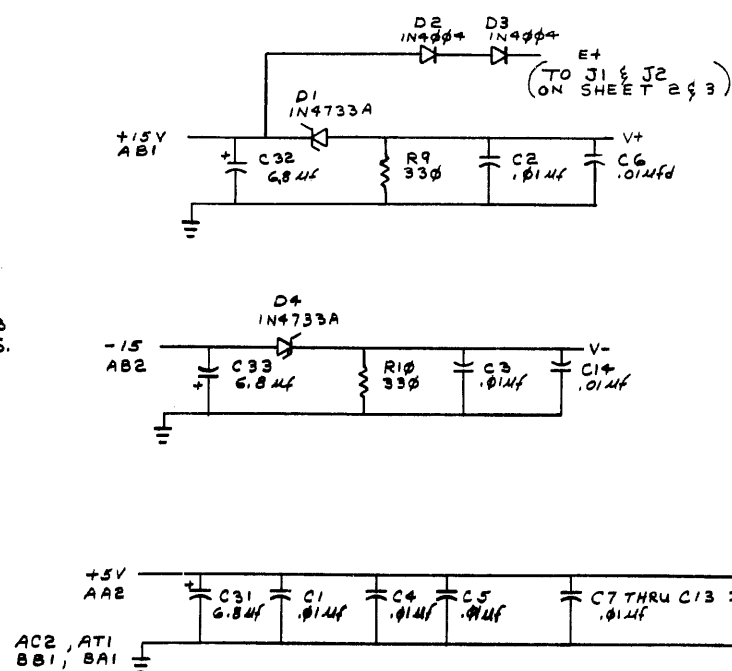


* SEE NOTE 2.

REVISIONS		
CHK	CHANGE TO	REV

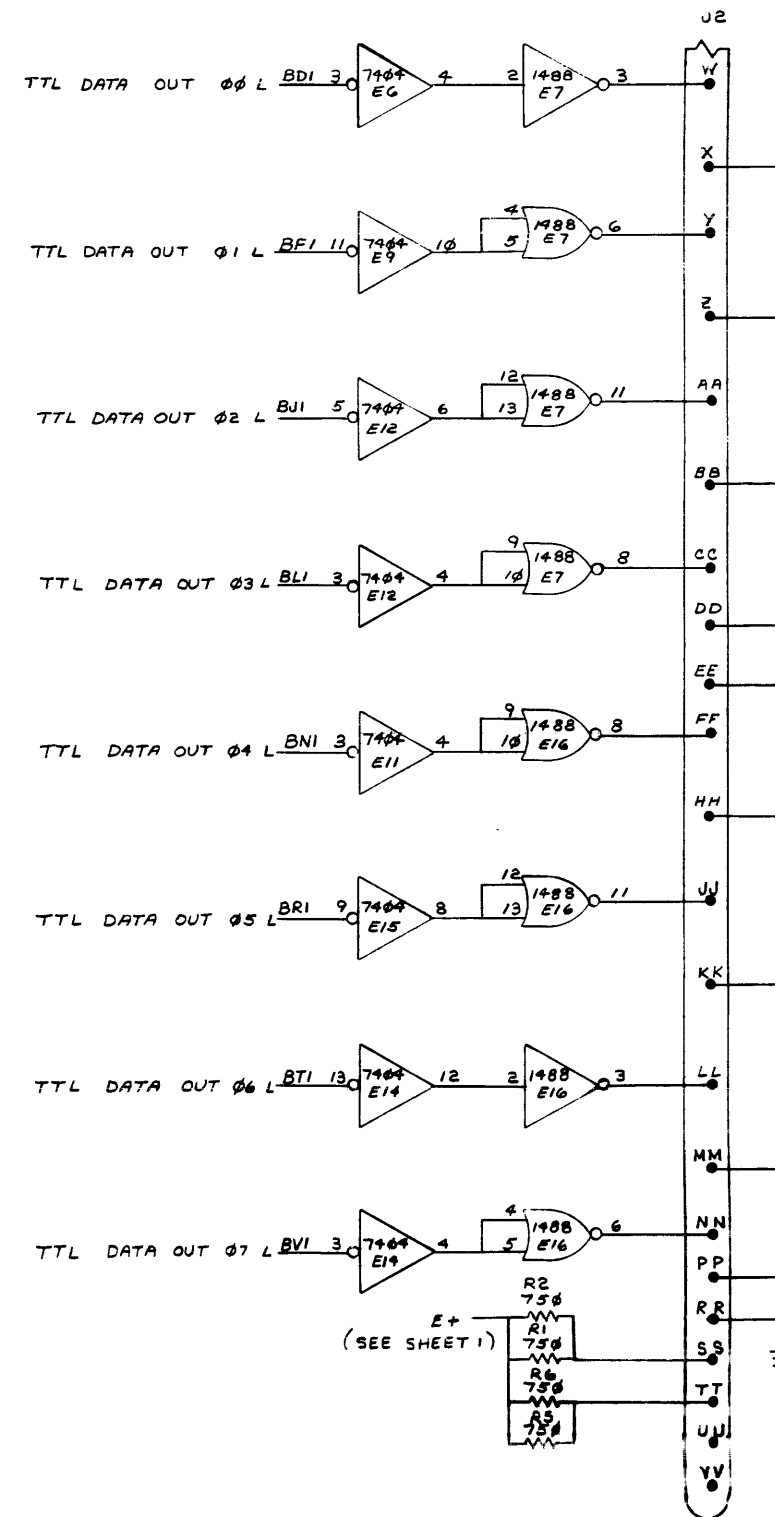
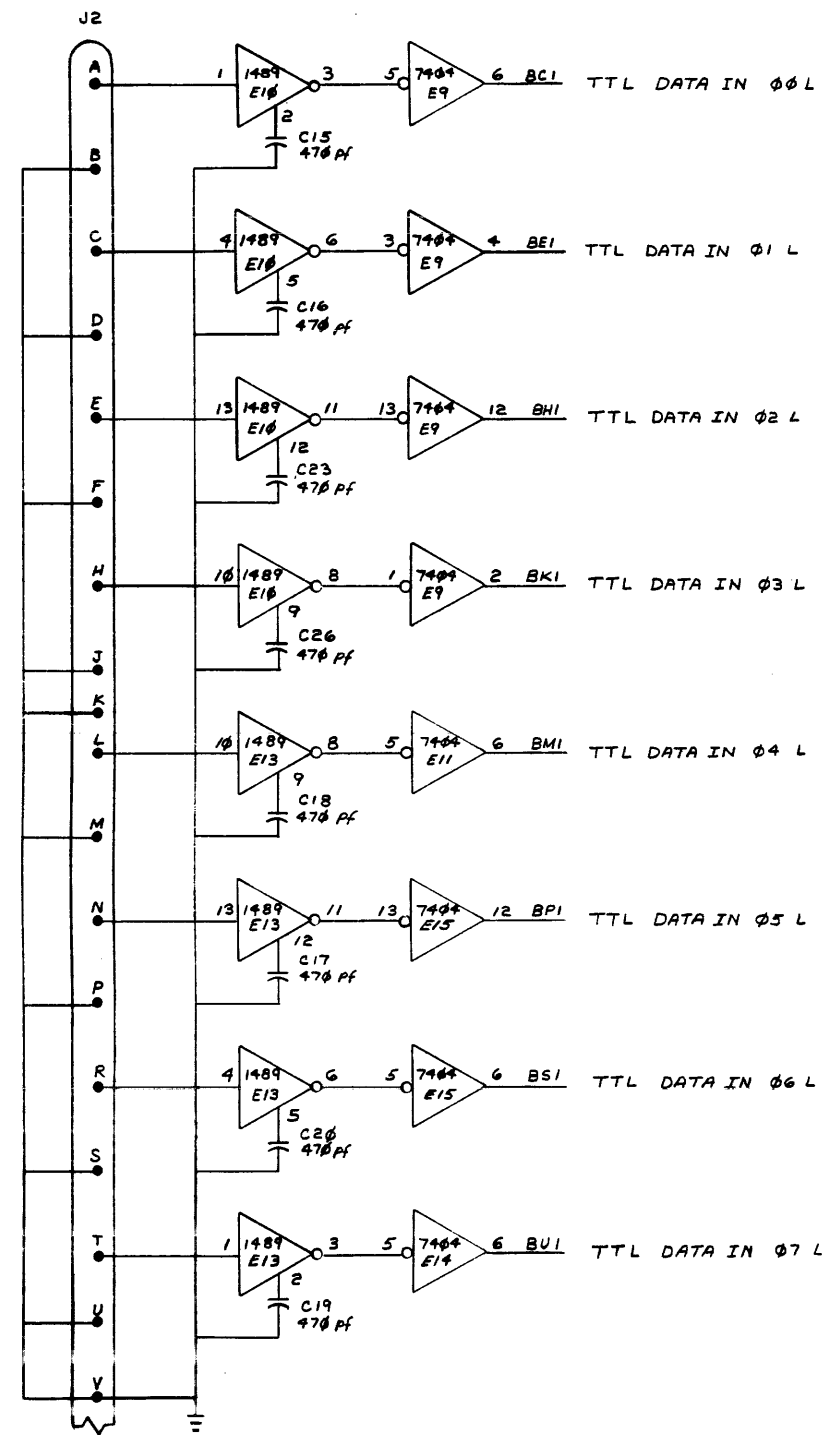
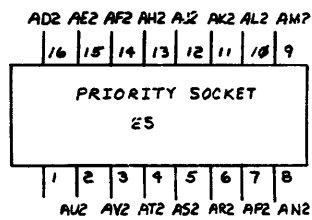
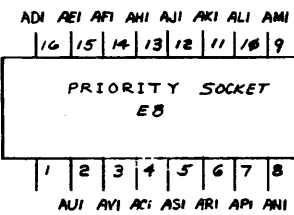
TITLE		BUS CONTROL & MUX	(D6)
SCALE	SHEET	7 OF 7	DIST.
SIZE CODE		D CSM7807-0-1	NUMBER
REV.		H	

NOTES:
1. THIS WIRE TO BE ADDED ON M5906-YA ONLY.

[illegible]

FIRST USED ON OPTION MODEL				QTY	REF DESIGNATION	DESCRIPTION				PART NO.			
DHII				ETCH BOARD REV				B	PARTS LIST				
R. Harrington J.E. KITTLE 23 MAR 78	M5906-0001 ORIGINATED A	B	A	REV	DRN <i>Quilora</i> DATE <i>3/13/78</i> <i>[Signature]</i> DATE <i>3/13/78</i> <i>[Signature]</i> DATE <i>3/13/78</i> <i>[Signature]</i> DATE <i>3/13/78</i> <i>[Signature]</i> DATE <i>3/13/78</i> NEXT HIGHER ASSY B-DD-DHII - Ø				 digital EQUIPMENT CORPORATION NATYARD MASSACHUSETTS TITLE EIA CONVERTER AND PRIORITY				
CHK	CHANGE NO.	REVISIONS			DEC NO.	EIA NO.	DEC NO.	EIA NO.	SCALE NONE	SHEET 1 OF 3	DIST.	REVISION NUMBER DCS M5906-Ø-I	REV. B
SEMICONDUCTOR CONVERSION CHART													

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REVISIONS		
CHK	CHANGE NO	REV

DEC FORM NO
DHD 138

TITLE EIA CONVERTER
AND PRIORITY

SIZE CODE NUMBER
DCSM5906-0-1

REV.
B

SCALE SHEET 2 OF 3

DIST.

11

1

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6

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4

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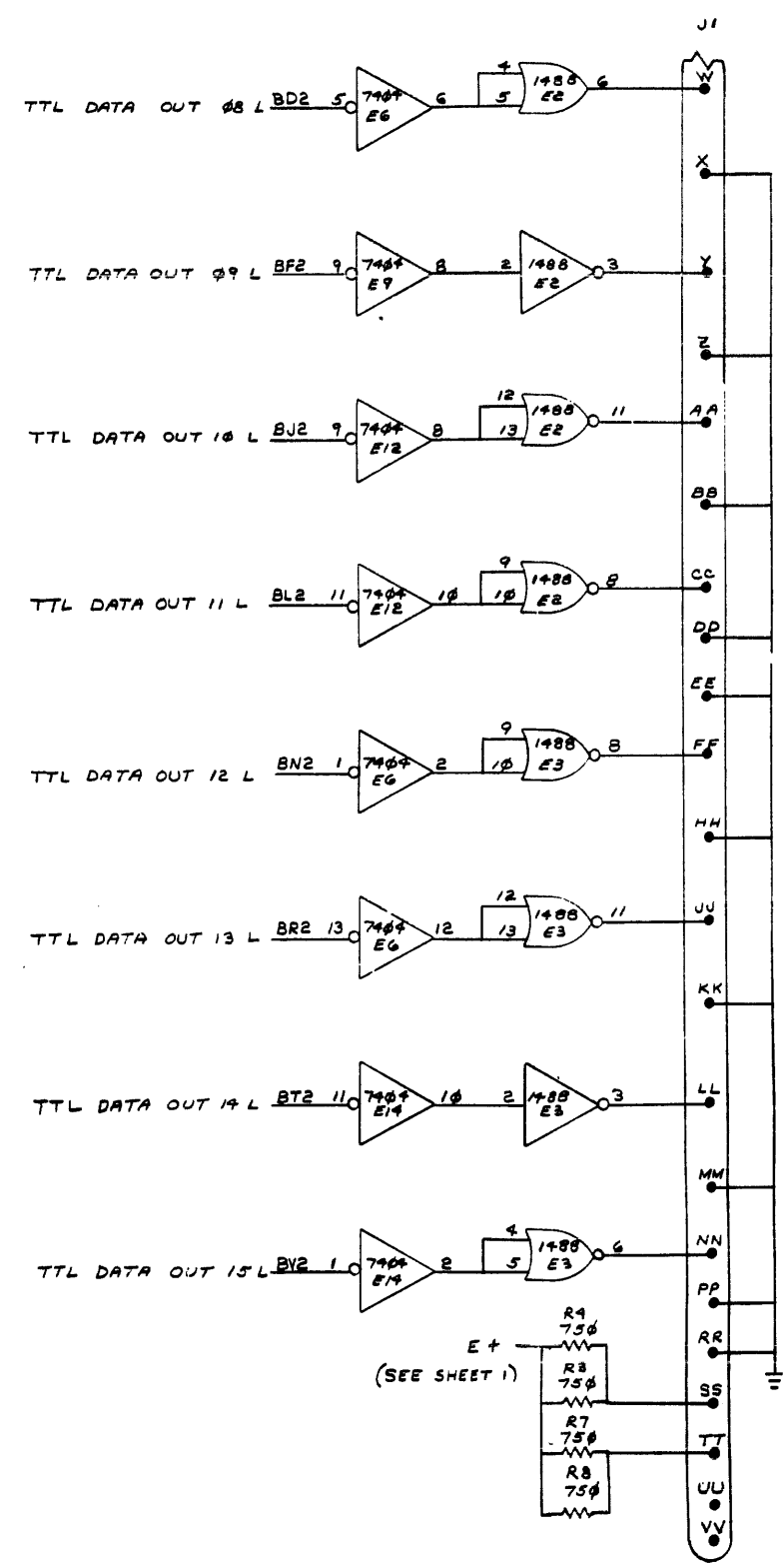
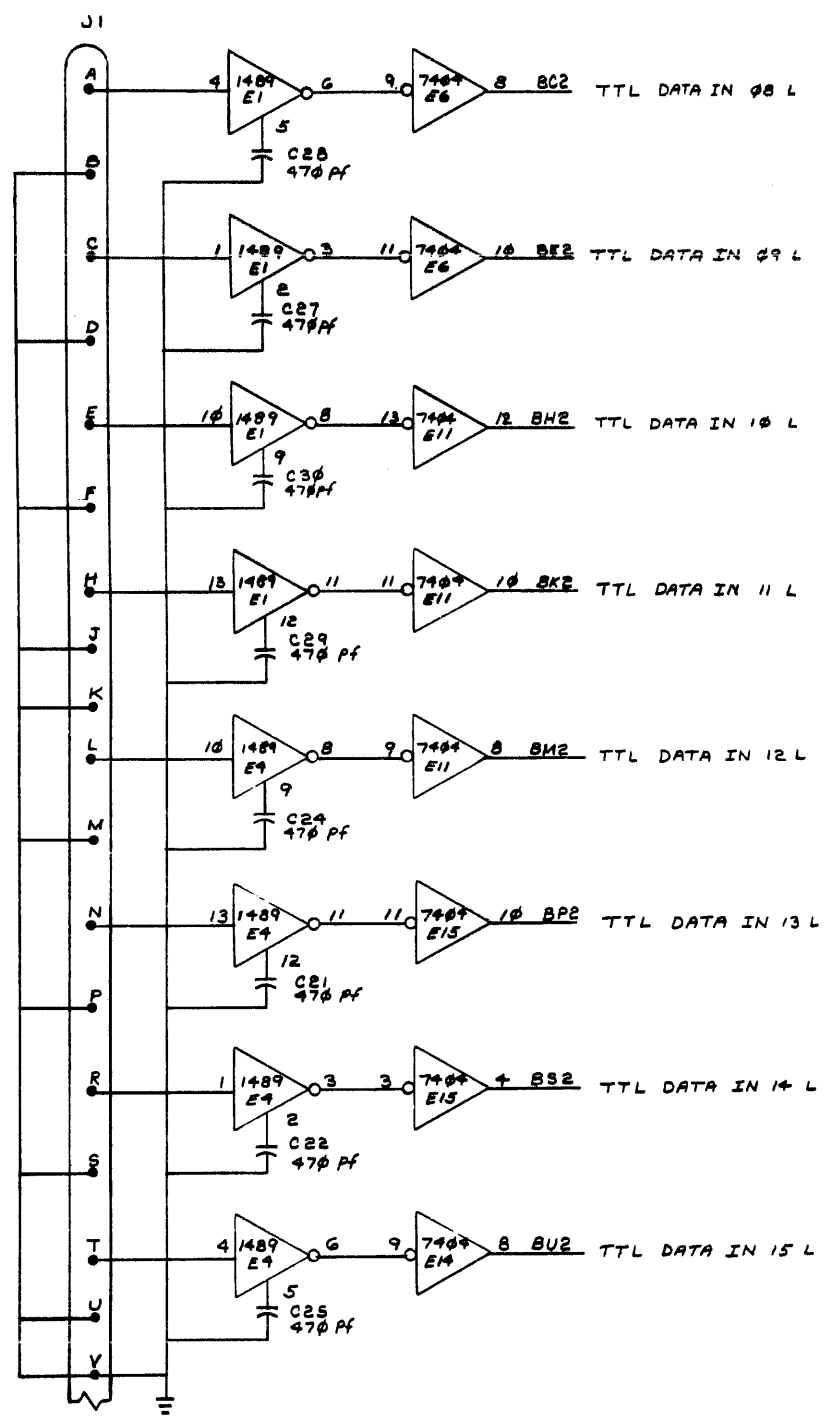
2

1-0-906SW

2

1

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REVISIONS		
CHK	CHANGE NO.	REV.

DEC FORM NO
000 132

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7

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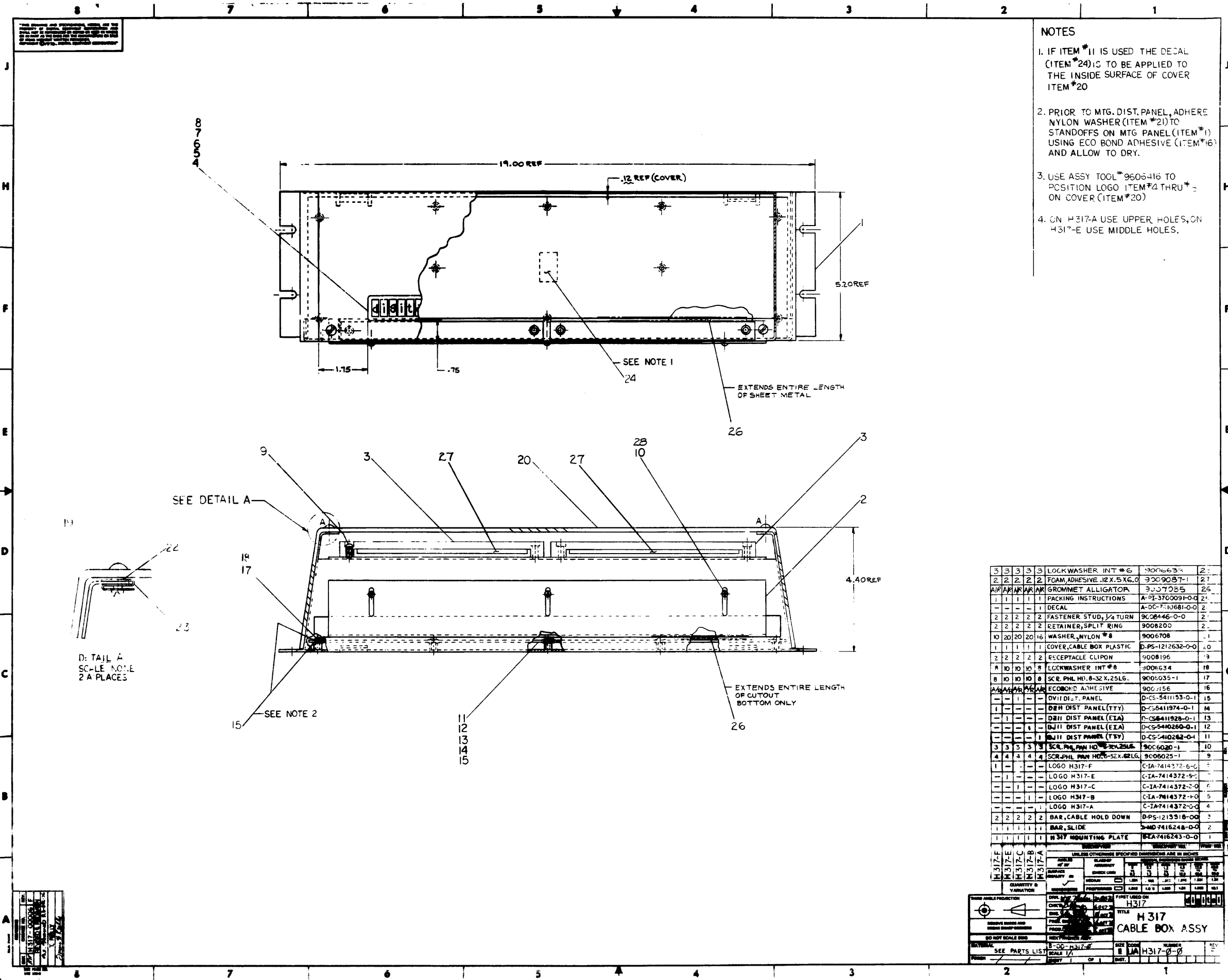
TITLE EIA CONVERTER
AND PRIORITY

SIZE CODE NUMBER
D CSM5906-0-1

REV. B

SCALE SHEET 3 OF 3

MR



- NOTES
1. IF ITEM #11 IS USED THE DECAL (ITEM #24) IS TO BE APPLIED TO THE INSIDE SURFACE OF COVER ITEM #20
 2. PRIOR TO MTG. DIST. PANEL, ADHERE NYLON WASHER (ITEM #21) TO STANDOFFS ON MTG. PANEL (ITEM #1) USING ECO BOND ADHESIVE (ITEM #6) AND ALLOW TO DRY.
 3. USE ASSY TOOL #9606416 TO POSITION LOGO ITEM #4 THRU #5 ON COVER (ITEM #20)
 4. ON H317-A USE UPPER HOLES, ON H317-E USE MIDDLE HOLES.

3	3	3	3	3	LOCK WASHER INT #6	9006634	2
2	2	2	2	2	FOAM ADHESIVE .12X.5X6.0	9009087-1	27
1	1	1	1	1	GROMMET ALLIGATOR	3007035	26
1	1	1	1	1	PACKING INSTRUCTIONS	A-PS-3700091-0-0	24
1	1	1	1	1	DECAL	A-DC-710681-0-0	2
2	2	2	2	2	FASTENER STUD, 1/4 TURN	9008446-0-0	27
2	2	2	2	2	RETAINER, SPLIT RING	9008200	28
10	20	20	16	16	WASHER, NYLON #8	9006708	21
1	1	1	1	1	COVER, CABLE BOX PLASTIC	D-PS-1212632-0-0	20
2	2	2	2	2	RECEPTACLE CLIP ON	9008196	19
8	10	10	8	8	LOCK WASHER INT #8	9006634	18
8	10	10	8	8	SCR. PHL. HD. 8-32X.25LG.	9006035-1	17
1	1	1	1	1	ECOBOND ADHESIVE	9001156	16
1	1	1	1	1	DIST. PANEL	D-CS-5411153-0-1	15
1	1	1	1	1	DIST. PANEL (TTY)	D-CS-54111974-0-1	14
1	1	1	1	1	DIST. PANEL (EIA)	D-CS-54111928-0-1	13
1	1	1	1	1	DIST. PANEL (EIA)	D-CS-5410260-0-1	12
1	1	1	1	1	DIST. PANEL (TTY)	D-CS-5410262-0-1	11
3	3	3	3	3	SCR. PHL. HD. 8-32X.25LG.	9006035-1	10
4	4	4	4	4	SCR. PHL. HD. 8-32X.25LG.	9006025-1	9
1	1	1	1	1	LOGO H317-F	C-IA-7414372-6-0	7
1	1	1	1	1	LOGO H317-E	C-IA-7414372-5-0	6
1	1	1	1	1	LOGO H317-C	C-IA-7414372-2-0	5
1	1	1	1	1	LOGO H317-B	C-IA-7414372-1-0	4
1	1	1	1	1	LOGO H317-A	C-IA-7414372-0-0	3
2	2	2	2	2	BAR, CABLE HOLD DOWN	D-PS-1213316-0-0	2
1	1	1	1	1	BAR, SLIDE	D-MD-7416248-0-0	1
1	1	1	1	1	H317 MOUNTING PLATE	E-IA-7416243-0-0	1

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

QUANTITY & VARIATION	DESCRIPTION	REVISION	DATE
1	H317	1	10-0000

THIRD ANGLE PROJECTION

REVISIONS

DATE

BY

CHKD

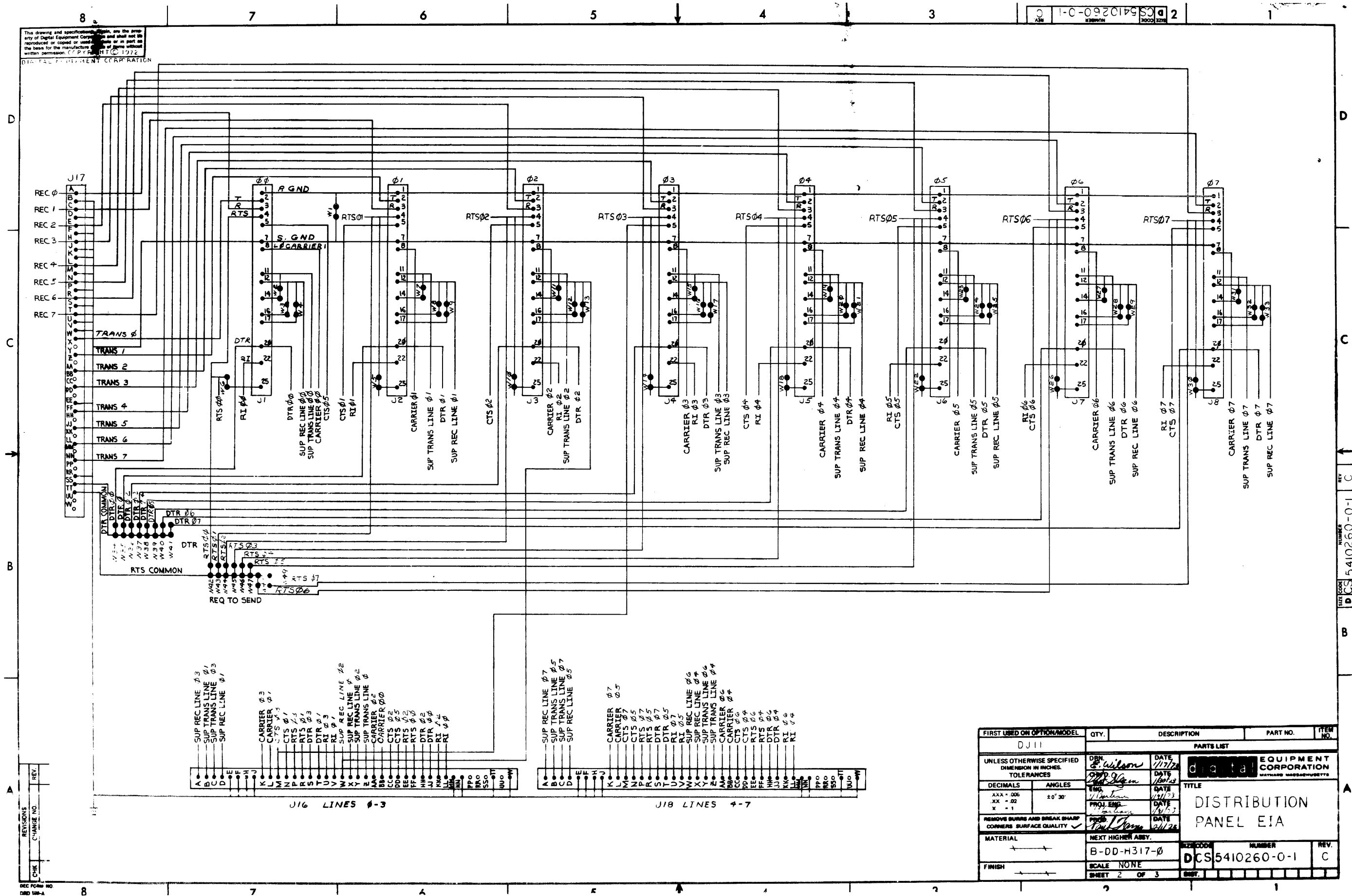
APP'D

SCALE

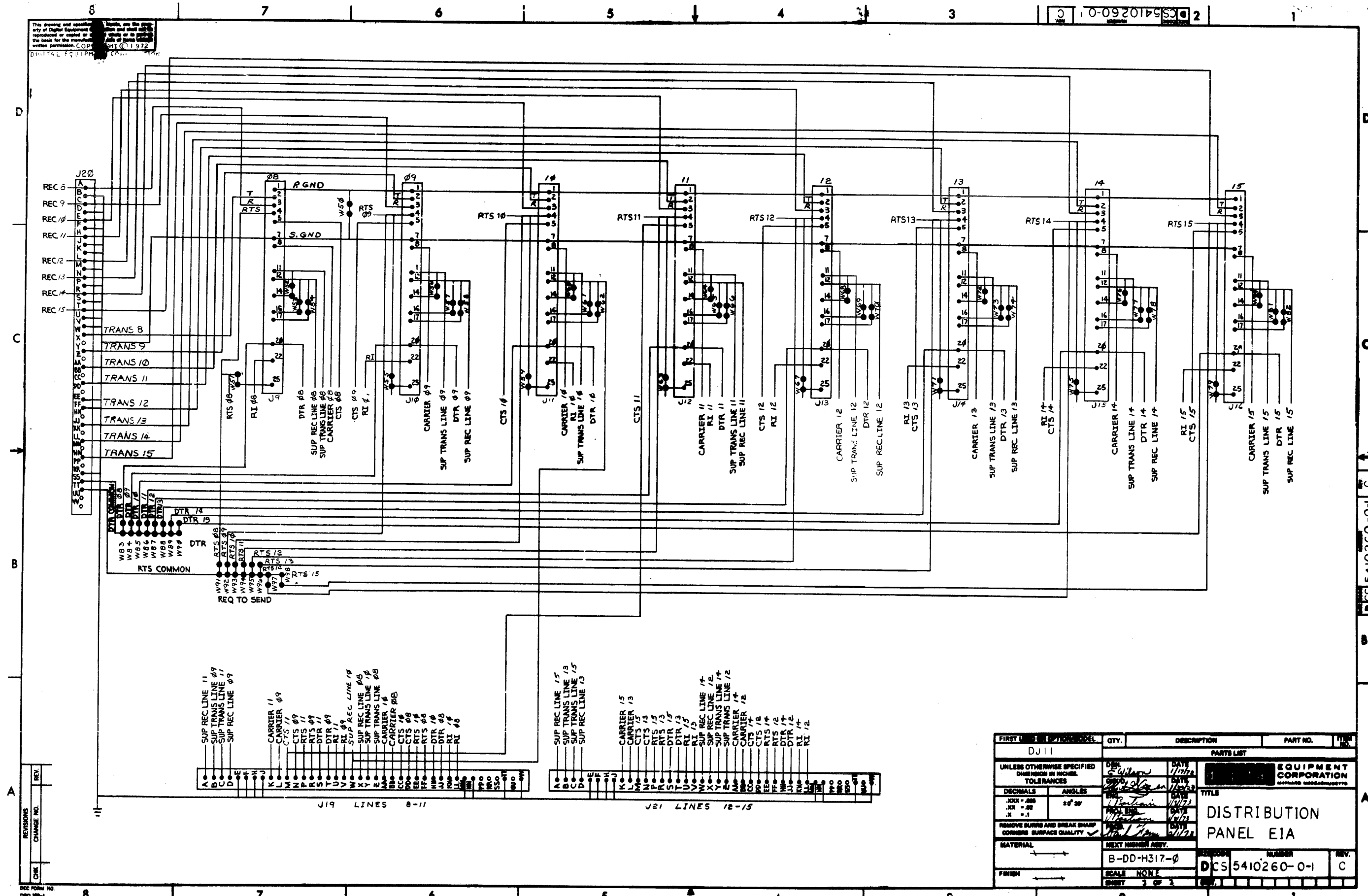
1/4"

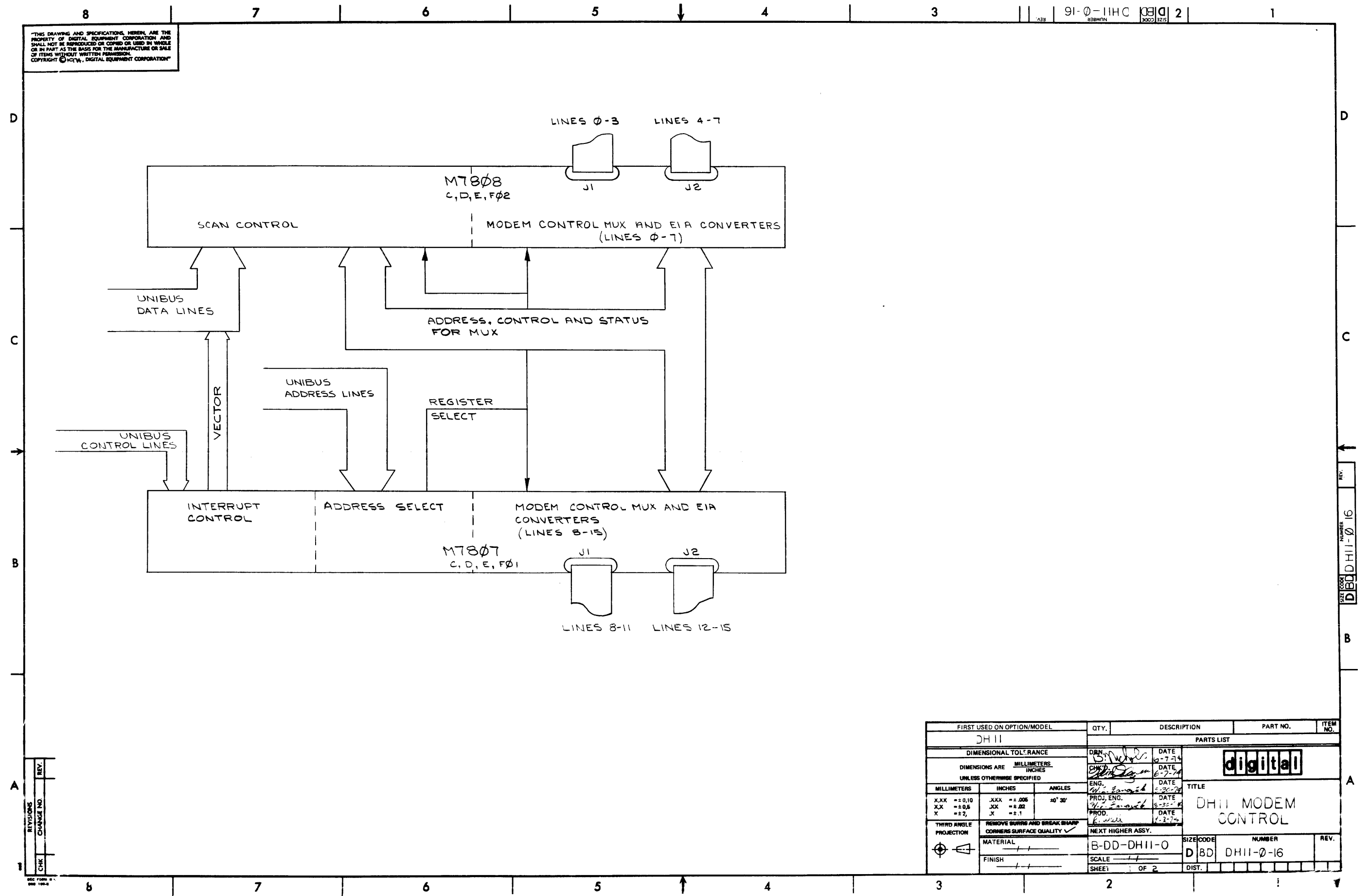
SEE PARTS LIST

1



FIRST USED ON OPTION/MODEL		QTY.	DESCRIPTION	PART NO.	ITEM NO.
DJ11			PARTS LIST		
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES.		DRN. <i>D. Wilson</i>	DATE <i>11/17/73</i>	 EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS	
TOLERANCES		<i>Paul Logan</i>	DATE <i>1/20/73</i>		
DECIMALS	ANGLES	ENG. <i>1/1/73</i>	DATE <i>1/1/73</i>		
XXX - .006 XX - .02 X - .1	±0° 30'	PROJ. ENG. <i>1/1/73</i>	DATE <i>1/1/73</i>		
REMOVE BURNS AND BREAK SHARP CORNERS SURFACE QUALITY ✓		PRICE <i>Paul Logan</i>	DATE <i>2/1/73</i>	TITLE DISTRIBUTION PANEL EIA	
MATERIAL		NEXT HIGHER ASSY.			
		B-DD-H317-Ø		MFG CODE NUMBER REV. DCS 5410260-0-1 C	
FINISH		SCALE NONE			
		SHEET 2 OF 3		MFG.	

[illegible]



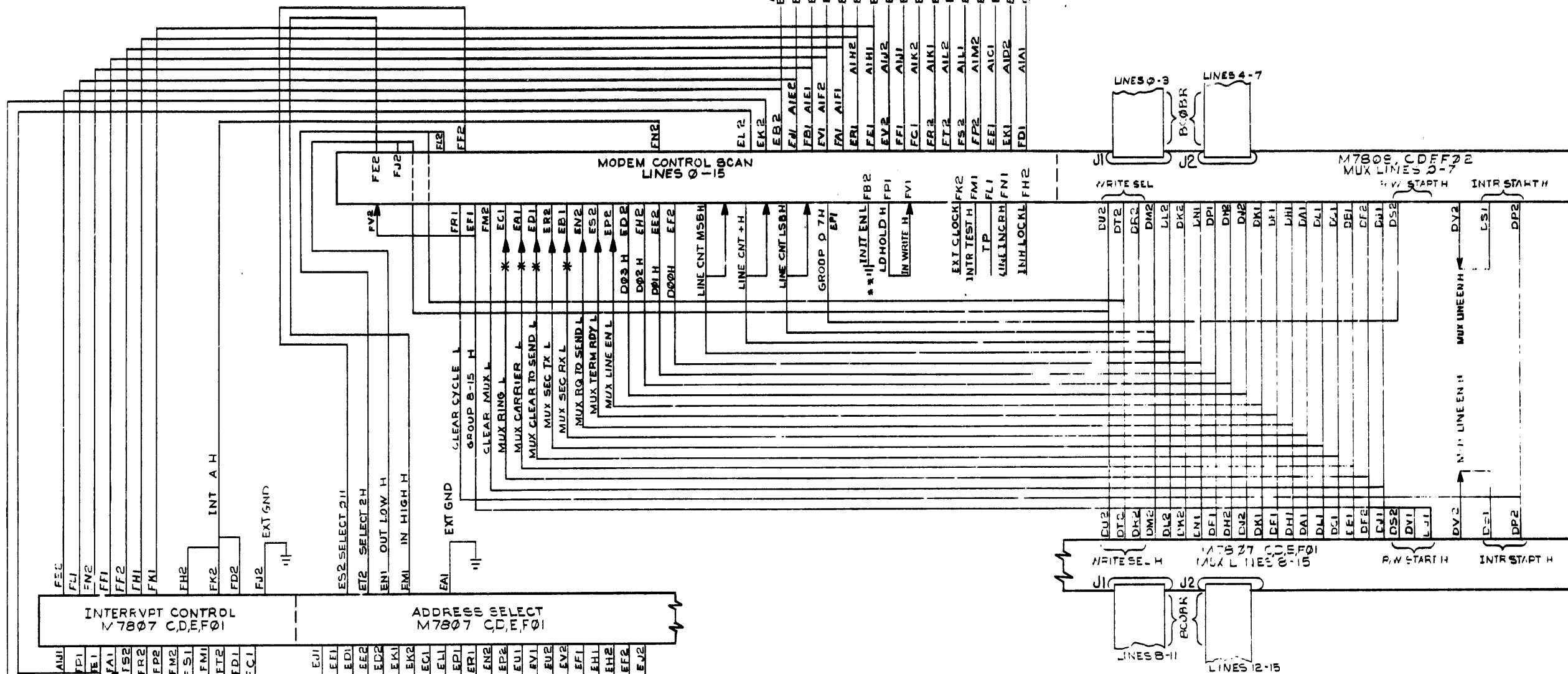
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NOTES:

- 1 MODULE PINS, AS USED IN THIS PRINT, ARE AS PER SYSTEM UNIT BACK PANEL WIRES.
- 2 * REMOVE WIRES TO INHIBIT INTERRUPTS FROM TRANSACTIONS.
- 3 *** REMOVE WIRE TO INHIBIT INITIALIZE FROM CLEARING THE SCAN AND MUX MODULES

REV.	CHANGE NO.	DESCRIPTION
1	1	INITIAL RELEASE
2	1	REWORK FOR M7807
3	1	REWORK FOR M7807
4	1	REWORK FOR M7807
5	1	REWORK FOR M7807
6	1	REWORK FOR M7807
7	1	REWORK FOR M7807
8	1	REWORK FOR M7807
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98	1	REWORK FOR M7807
99	1	REWORK FOR M7807

- 1 MODULE PINS, AS USED IN THIS PRINT, ARE AS PER SYSTEM UNIT BACK PANEL WIRES.
- 2 * REMOVE WIRES TO INHIBIT INTERRUPTS FROM TRANSITIONS.
- 3 ** REMOVE WIRE TO INHIBIT INITIALIZE FROM CLEARING THE SCAN AND MLX MODULES



FIRST USED ON JCTION/MODEL		QTY.	DESCRIPTION	PART NO.	ITEM NO.
DH11-O		PARTS LIST			
DIMENSIONAL TOLERANCE DIMENSIONS ARE <u>MILLIMETERS</u> UNLESS OTHERWISE SPECIFIED		DRN. <i>W.D.</i> <i>Baron</i> C/P D. of <i>Baron</i> ENG. <i>W.D. Baron</i> PROJ. ENG. <i>W.D. Baron</i> PROD. <i>R. Wolf</i>	DATE <i>8/6/74</i> DATE <i>8/16/74</i> DATE <i>8-30-74</i> DATE <i>8-30-74</i> DATE <i>9-3-74</i>		
MILLIMETERS HIGHS ANGLES X.XX = ±0.18 JOX = ±.008 30° 30' X.X = ±0.5 JOX = ±.02 X = ±.25 X = ±.1		TITLE		DH11 MODEM CONTROL	
THIRD ANGLE PROJECTION 		REMOVE BURRS AND BREAK SHARP CORNERS SURF. AC QUALITY ✓ MATERIAL <u>11</u> FINISH <u>11</u>		NEXT HIGHER ASSY. B-DD-DH11-O SCALE <u>11</u> SHEET 2 OF 2	
		SIZE CODE		NUMBER	REV.
		D BD		DH11-Ø-16	

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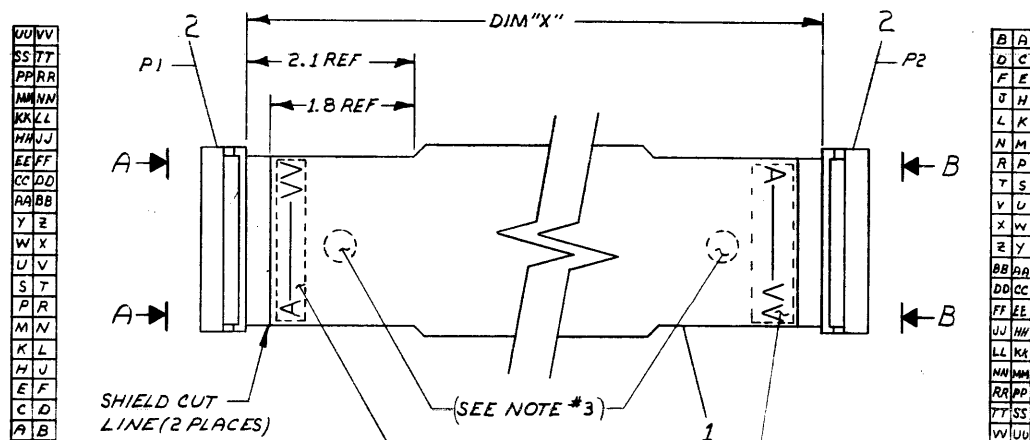
WIRE TABLE

FROM	TO	FROM	TO
P1-A	P2-VV	P1-Y	P2-X
P1-B	P2-UU	P1-Z	P2-W
P1-C	P2-TT	P1-AA	P2-V
P1-D	P2-SS	P1-BB	P2-U
P1-E	P2-RR	P1-CC	P2-T
P1-F	P2-PP	P1-DD	P2-S
P1-H	P2-NN	P1-EE	P2-R
P1-J	P2-MM	P1-FF	P2-P
P1-K	P2-LL	P1-HH	P2-N
P1-L	P2-KK	P1-JJ	P2-M
P1-M	P2-JJ	P1-KK	P2-L
P1-N	P2-HH	P1-LL	P2-K
P1-P	P2-FF	P1-MM	P2-J
P1-R	P2-EE	P1-NN	P2-H
P1-S	P2-DD	P1-PP	P2-F
P1-T	P2-CC	P1-RR	P2-E
P1-U	P2-BB	P1-SS	P2-D
P1-V	P2-AA	P1-TT	P2-C
P1-W	P2-Z	P1-UU	P2-B
P1-X	P2-Y	P1-VV	P2-A

LEGEND

NUMBER	DIM "X"	PRECUT LENGTH
BC08R-01	1.00 FT.	1.00 FT. 1.5 IN ± 1.00 IN
BC08R-02	2.00 FT.	2.00 FT. 1.5 IN ± 1.00 IN
BC08R-03	3.00 FT.	3.00 FT. 1.5 IN ± 1.00 IN
BC08R-04	4.00 FT.	4.00 FT. 1.5 IN ± 1.00 IN
BC08R-05	5.00 FT.	5.00 FT. 1.5 IN ± 1.00 IN
BC08R-06	6.00 FT.	6.00 FT. 1.5 IN ± 2.00 IN
BC08R-07	7.00 FT.	7.00 FT. 1.5 IN ± 2.00 IN
BC08R-08	8.00 FT.	8.00 FT. 1.5 IN ± 2.00 IN
BC08R-09	9.00 FT.	9.00 FT. 1.5 IN ± 2.00 IN
BC08R-10	10.00 FT.	10.00 FT. 1.5 IN ± 2.00 IN
BC08R-11	11.00 FT.	11.00 FT. 1.5 IN ± 3.00 IN
BC08R-12	12.00 FT.	12.00 FT. 1.5 IN ± 3.00 IN
BC08R-13	13.00 FT.	13.00 FT. 1.5 IN ± 3.00 IN
BC08R-14	14.00 FT.	14.00 FT. 1.5 IN ± 3.00 IN
BC08R-15	15.00 FT.	15.00 FT. 1.5 IN ± 3.00 IN
BC08R-16	16.00 FT.	16.00 FT. 1.5 IN ± 3.00 IN
BC08R-17	17.00 FT.	17.00 FT. 1.5 IN ± 3.00 IN
BC08R-18	18.00 FT.	18.00 FT. 1.5 IN ± 3.00 IN
BC08R-19	19.00 FT.	19.00 FT. 1.5 IN ± 3.00 IN
BC08R-20	20.00 FT.	20.00 FT. 1.5 IN ± 3.00 IN
BC08R-25	25.00 FT.	25.00 FT. 1.5 IN ± 3.00 IN
BC08R-30	30.00 FT.	30.00 FT. 1.5 IN ± 3.00 FT
BC08R-35	35.00 FT.	35.00 FT. 1.5 IN ± 3.00 FT
BC08R-50	50.00 FT.	50.00 FT. 1.5 IN ± 1.00 FT
BC08R-60	60.00 FT.	60.00 FT. 1.5 IN ± 1.20 FT
BC08R-75	75.00 FT.	75.00 FT. 1.5 IN ± 1.50 FT
BC08R-100	100.00 FT.	100.00 FT. 1.5 IN ± 2.00 FT
BC08R-A3	130.00 FT.	130.00 FT. 1.5 IN ± 2.00 FT
BC08R-A6	160.00 FT.	160.00 FT. 1.5 IN ± 2.00 FT

1. ASSEMBLE THIS CABLE PER PROCESS SPEC #7606485-0-0.
2. CONNECTOR LEGEND IDENTIFICATION TO BE PLACED ON SHIELD SIDE OF CABLE IN THIS AREA AS SHOWN.
3. INSPECTION & TEST STAMPS TO BE PLACED AT EACH END OF THE CABLE ASSY.
4. STRIP LENGTH SHOULD BE .62 ± 4/32.



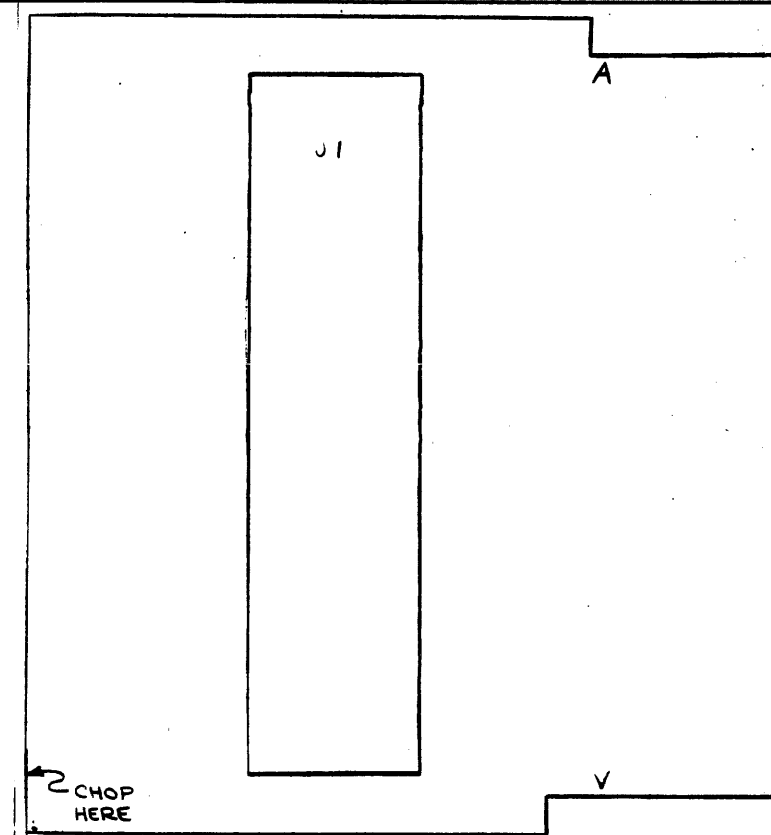
VIEW A-A
CONN LEGEND REF

VIEW B-B
CONN LEGEND REF

2	CONNECTOR, 40 SOCKET	1211206	2
1	AIR CABLE, 40 COND. FLAT W/SHIELD	1700004	1
DESCRIPTION		DWG./PART NO.	ITEM NO.
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES			
ANGLES 30° 30'	CLASS OF ACCURACY (CHECK ONE)	NORMAL DIMENSION RANGE INCHES	
SURFACE QUALITY IN	MEDIUM	OVER 0 TO 0.2	OVER 0.2 TO 1.2
	PREFERRED	OVER 1.2 TO 4.0	OVER 4.0 TO 12.0
QUANTITY & VARIATION	MICRONCHES	±.004	±.008 ±.012 ±.016 ±.024 ±.04
THIRD ANGLE PROJECTION		FIRST USED ON	
REMOVE BURRS AND BREAK SHARP CORNERS		20-00-01	
DO NOT SCALE DWG		NEXT HIGHER ASSY.	
MATERIAL		SCALE	
FINISH		SHEET OF	
DRNO. FONTAINE 8-28-70		CHIKOJ. FLEMING 8-28-70	
ENGP. GARDNER 9-3-70		PROJ. ENG. GARDNER 9-3-70	
PROD. DONALD 9-4-70		TITLE	
		BC08R IO CABLE	
SIZE CODE		NUMBER	
D UA		BC08R-0-0	
REV.		M	

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- | | | | |
|----|----|----|-------------------------|
| H1 | J1 | 24 | EXTERNAL CLOCK |
| H2 | | 15 | TRANSMIT CLOCK |
| J2 | | 17 | RECEIVER CLOCK |
| E2 | | 2 | TRANSMIT DATA |
| F2 | | 3 | RECEIVE DATA |
| N2 | | 6 | DATA SET READY |
| E1 | | 11 | SECONDARY TRANSMIT DATA |
| F1 | | 12 | SECONDARY RECEIVE DATA |
| R2 | | 20 | DATA TERMINAL READY |
| P2 | | 8 | CARRIER DETECT |
| K2 | | 7 | CLEAR TO SEND |
| L2 | | 4 | REQUEST TO SEND |
| S1 | | 25 | FORCE BUSY |
| M2 | | 22 | RING |



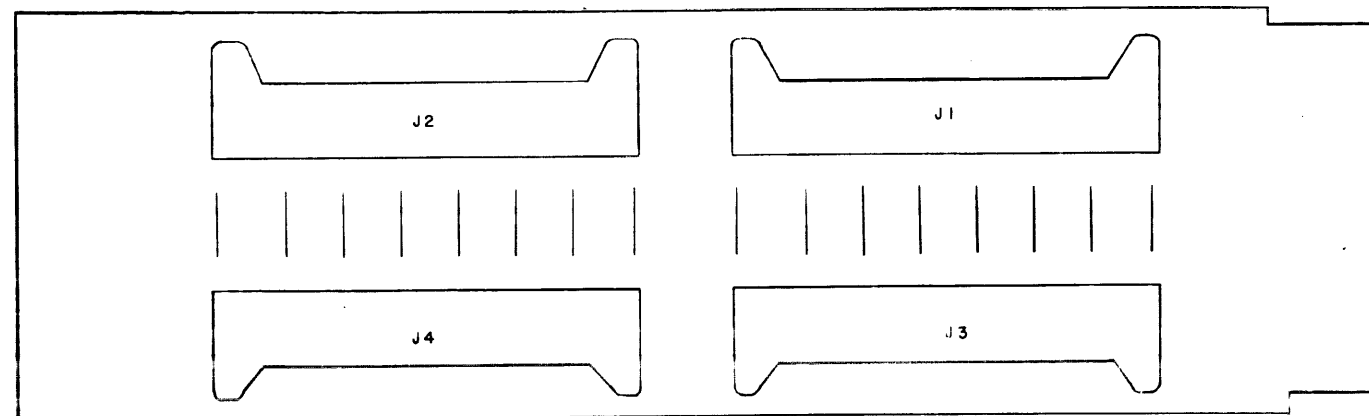
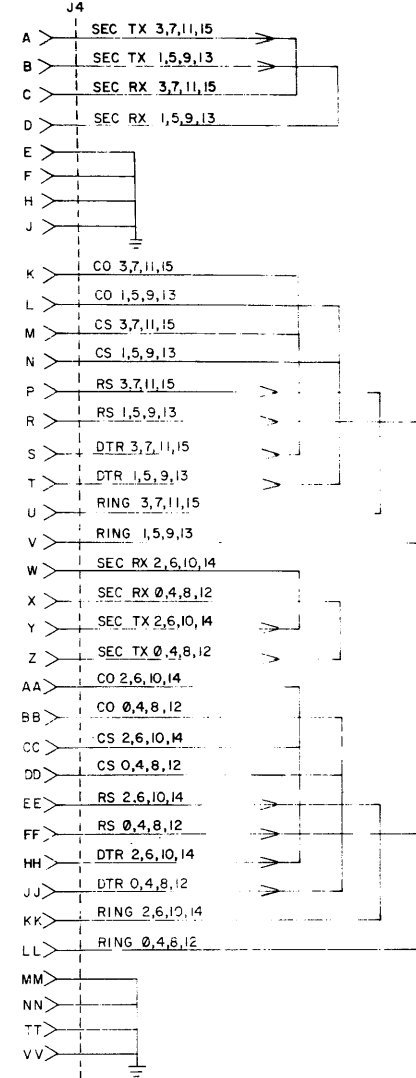
1	J1	CONN. CINCIN DB-255-	1210247	5
1		ETCHED CIRCUIT	501002C	4
		MODULE ECO HISTO...	B-MH-H315-0-6	3
		ASSY/DRILLING HOLE	C-MH-H315-0-5	2
		X-Y COORDINATE HOLE LOCATION	K-CO-H315-0-4	1

QTY	REF. DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.
-----	------------------	-------------	----------	----------

PARTS LIST

ETCH BOARD REV	A	B
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DRN <i>Rover</i>	DATE 3-5-74	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
CHD. <i>Donnell</i>	DATE 3-7-74	
APP. <i>[Signature]</i>	DATE 3-7-74	
PROD. <i>[Signature]</i>	DATE 3-7-74	
NEXT HIGHER ASSY		
DEC NO. EIA NO. DEC NO. EIA NO.		TITLE MODEM TEST CONNECTOR
SEMICONDUCTOR CONVERSION CHART		
SCALE		SIZE CODE DCS
SHEET 1 OF 1		NUMBER H315-0-1
		REV. A



4	- COMM. GND. AT END OF BOARD		1269901	5
	STANDARD CIRCUIT BOARD		5009746	4
	MODULE BCU HISTORY		B-BB-H861-0-0-6	3
	ASSY/DRILLING HOLE LAYOUT		J-AH-H861-0-0-5	2
	X-Y COORDINATE HOLE LOCATION		K-CO-H861-0-0-1	1
	DESCRIPTION		DBC PART NO.	0
REF.	DESCRIPTION			
PARTS LIST				

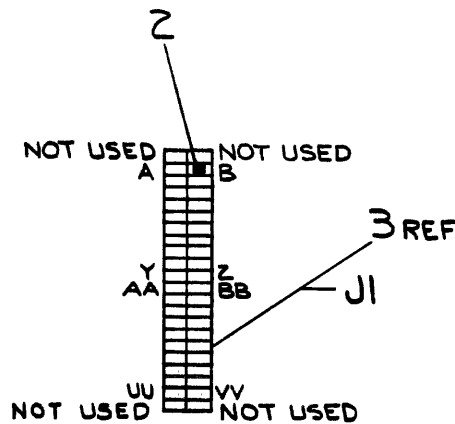
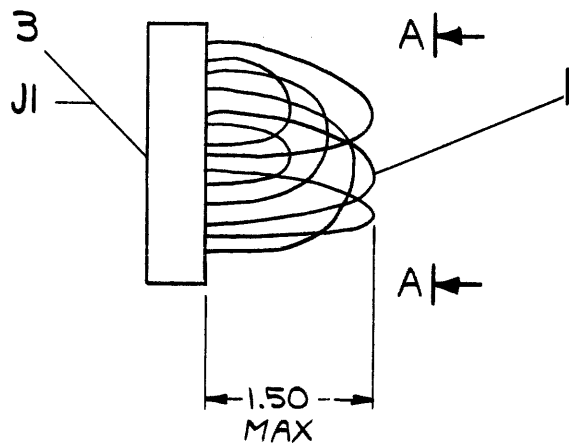
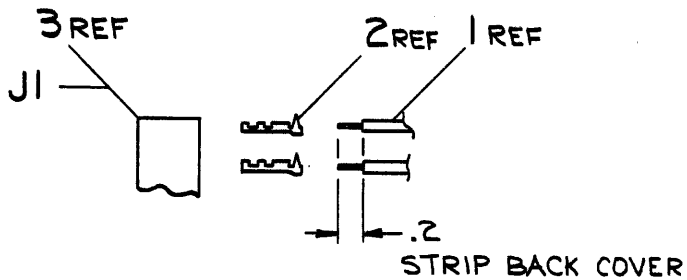
DATE 1/25/74	TRANSISTOR & DIODE CONVERSION CHART				TITLE DM 11-BB TEST CONNECTOR	
DATE 4-1-74	DEC	EIA	DEC	EIA	USE CS	CODE H861-0-1
DATE 11-26-74					NUMBER C	REV B
DATE 12-23-74					PRINTED CIRCUIT REV	

EQUIPMENT CORPORATION		MAYNARD, MASSACHUSETTS	
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DO NOT SCALE DRAWING
WIRE TABLE

ITEM NO	DESCRIPTION		FROM		TO	
	AWG	COLOR	CONN	WITH	CONN	WITH
1	22	BLK	J1 - A	Z	J1 - W	Z
			J1 - C		J1 - Y	
			J1 - E		J1 - AA	
			J1 - H		J1 - CC	
			J1 - L		J1 - FF	
			J1 - N		J1 - JJ	
			J1 - R		J1 - LL	
1	22	BLK	J1 - T	Z	J1 - NN	Z



VIEW A-A
SCALE: NONE

1	HOUSING, SOCKET	1210918-15	3
16	SOCKET, CRIMP	1210089-06	2
A/R	WIRE #22 AWG (BLK)	9107350-00	1

FIRST USED ON OPTION/MODEL M5906		QTY.	DESCRIPTION	PART NO.	ITEM NO.
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES		PARTS LIST			
TOLERANCES		digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS			
DECIMALS	ANGLES	TITLE CONN, DATA TURN AROUND			
.xxx = .005	±0° 30'	SIZE CODE C UA			
.xx = .02		NUMBER H8611-0-0			
.x = .1		REV.			
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY V		SCALE			
MATERIAL		SHEET 1 OF 1			
SEE PARTS LIST		DIST.			
FINISH					

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DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS						
ENGINEERING SPECIFICATION				DATE Aug. 6, 1975		
TITLE Installation of Additional DH11 Clocks						
REVISIONS						
REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
—	ORIGINATED	DH11-00010	J. MONAMARA	22 OCT 75	—	—
ENG	APPD	SIZE	CODE	NUMBER	REV	
<i>John E. P. P. P.</i>	<i>John E. P. P. P.</i>	A	SP	DH11-8-17	—	

DEC 16-1382-1075-41971
DRA 107

Sheet 1 of 3

ENGINEERING SPECIFICATION				CONTINUATION SHEET			
TITLE Installation of Additional DH11 Clocks							
I. Scope:							
This procedure outlines the correct method for installation of clocks appropriate to baud rates not normally supplied by the M4540 clock in the DH11. These additional clocks are referred to as "external clocks". Up to two external clocks, designated as "External A" and "External B" may be installed in a DH11. Clock pulse width must exceed 3 usec.							
II. Procedure:							
Install the appropriate module in the appropriate slot in accordance with the table below:							
Baud rate for External A is 40-110 baud: Place M401-YA in B#9. Baud rate for External A is 312-8000 baud: Place M4050-YA in B#9.							
Baud rate for External B is 40-110 baud: Place M401-YA in B#6. Baud rate for External B is 312-8000 baud: Place M4050-YA in B#6.							
Remove grounds at F08K2 and F08R2 by doing the following:							
Delete F08T1 - F08C2 (level 2) F08K2 - F08R2 (level 2) F08T1 - F08V1 (level 2) F08C2 - F08K2 (level 1) F08R2 - F08T1 (level 1)							
Add F08C2 - F08T1 (level 1) F08T1 - F08C2 (level 2) F08T1 - F08V1 (level 2)							
Install a backplane wire from B#9E2 to F#9K2. (Ext A Baud H) Install a backplane wire from B#6E2 to F#6R2. (Ext B Baud H)							
If the module that has been installed in a slot is an M401-YA, install a backplane wire from J2 to K2 and from K2 to T1. This provides the necessary enable. In addition, install a backplane wire from N2 to P2. This selects the timing range.							
III. Adjustments:							
The M4050-YA is crystal controlled, with the crystal selected to operate at a frequency 16 times the desired baud rate. Referring to the M4050-YA or M4050 schematic cut the W jumpers as indicated. No further adjustments are necessary.							
The M401-YA is an RC controlled oscillator, with the operating frequency selected to be 16 times the desired baud rate. Adjust R8 potentiometer to obtain the desired frequency.							
				SIZE	CODE	NUMBER	REV
				A	SP	DH11-8-17	—

DEC FORM NO DEC 16-1381-1022-41370
DRA 108

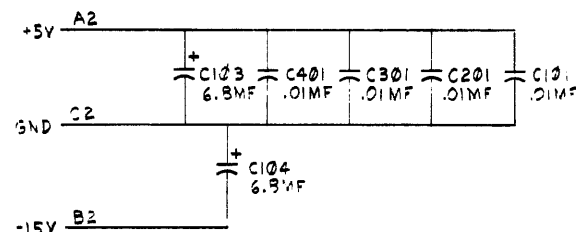
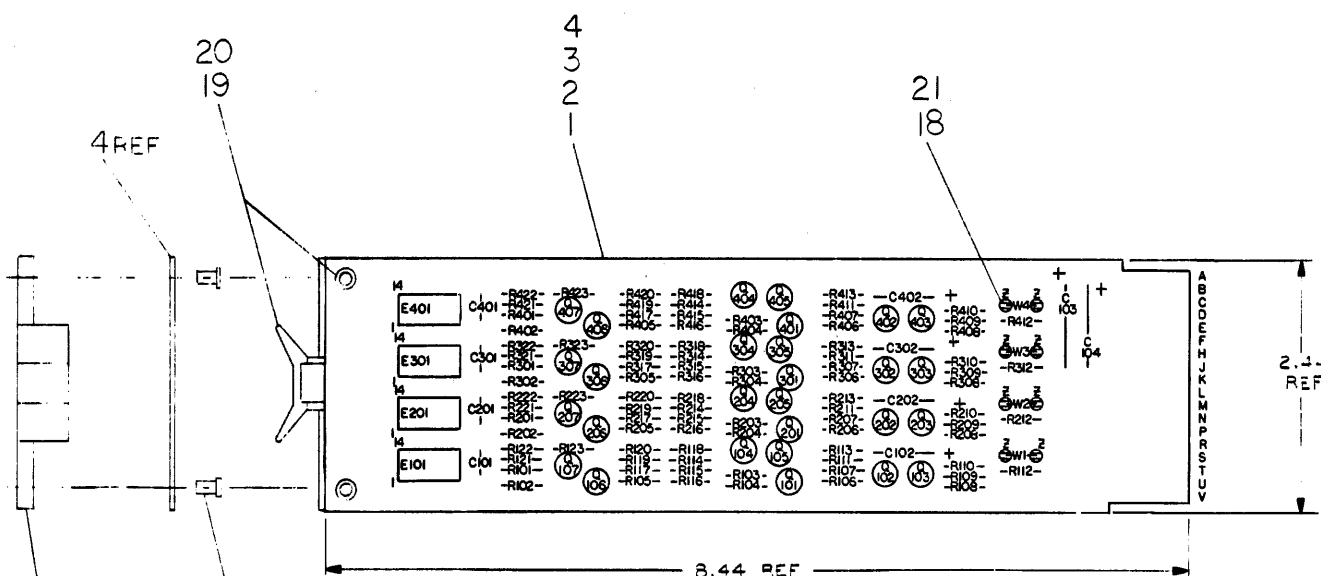
SHEET 2 OF 3

ENGINEERING SPECIFICATION				CONTINUATION SHEET			
TITLE Installation of Additional DH11 Clocks							
IV. Parts Substitutions:							
An M401-YA may be created from an M401 by replacing 82 mmf capacitor C2 with a 0.01 mf disc ceramic (10-01610-01), and tagging the module appropriately.							
An M4050-YA may be created from an M4050 by replacing C6, a 39 pf capacitor with a 470 pf capacitor and replacing R6, a 3K resistor with a 12K resistor. The new parts are 10-00024 and 13-00488 respectively. Tag the handle to indicate that this module has been altered to M4050-YA.							
An M405 may be used in place of an M4050-YA by installing a capacitor IN THE BACKPLANE between K2 and H2. Alternatively, the M405 could be converted to an M405-YA by replacing C6 (120 mmf) with another capacitor. In both the backplane capacitor and the C6 replacement case, a 0.01 mf disc ceramic (10-01610-01) will produce the appropriate pulse width (3 to 5 microseconds). If the substitution for C6 is made, tag the module to indicate this substitution.							
V. Baud Rate, Frequency & Period							
M401-YA (Pulse width approximately 4.4 microseconds)							
40 Baud	640 Hz	1.6 millisecond period					
110 Baud	1760 Hz	568 microsecond period					
M4050-YA (Pulse width approximately 4 microseconds)							
312 Baud	5000 Hz	200 microsecond period					
8000 Baud	128K Hz	7.4 microsecond period					
				SIZE	CODE	NUMBER	REV
				A	SP	DH11-8-17	—

DEC FORM NO DEC 16-1381-1022-41370
DRA 108

SHEET 3 OF 3

1. UNLESS OTHERWISE STATED RESISTANCE IS IN OHMS.
2. WHEN THE M5960 IS USED IN APPLICATIONS OVER 110 BAUD JUMPERS
W1-OUTPUT B1
W2-OUTPUT D1
W3-OUTPUT H1
W4-OUTPUT K1
MUST BE CUT OUT FOR THAT LINE.



REF		X-Y COORDINATE HOLE LOCATION	K-C-MS000-B-4
REF		ASSY.DRILL'NG HOLE LOCATION	D-AH-MS000-B-5
REF		MODULE ECO HISTORY	B-MH-MS000-B-6
1		ETCHED CIRCUIT BOARD	5010027
4	C101,C201,C301,C401	CAP .01 MF 100V 20% DISC	1001810-01
4	C102,C202,C302,C402	CAP 2.2 MF 35V 10% TANT	1002431
2	C103,C104	CAP 6.8 MF 35V 10% TANT	1005306
24	R108-R113,R208-R213,R308-R313,R408-R413	RES 47 OHMS 1/4W 5%	1300202
8	R117,R118,R217,R218,R317-R318,R417,R418	RES 68 OHMS 1/4W 5%	1300219
8	R106,R107,R206,R207,R306,R307,R406,R407	RES 150 OHMS 1/4W 5%	1300250
28	R102,R103,R105,R114,R116,R119,R120,R202,R203,R205,R214,R118,R219,R220,R302,R303,R305,R314,R318,R319,R320,R402,R403,R405,R414,R416,R419,R420	RES 1K OHMS 1/4W 5%	1300385
8	R101,R104,R201,R204,R301,R304,R401,R404	RES 3K OHMS 1/4W 5%	1300432
4	R123,R223,R323,R423	RES 15K OHMS 1/4W 5%	1300496
12	R115,R121,R122,R215,R221,R222,R215,R321,R322,R415,R421,R422	RES 5.6K OHMS 1/4W 5%	1301074
12	Q103,Q105,Q107,Q203,Q205,Q207,Q303,Q305,Q307,Q403,Q405,Q407	TRANS MPSA05	1510705
16	Q101,Q102,Q104,Q106,Q201,Q202,Q204,Q206,Q301,Q302,Q304,Q306,Q401,Q402,Q404,Q406	TRANS MPSA55	1510706
4	E101,E201,E301,E401	I.C. DEC 11380	1811113
8		SPLIT LUG	9008735
2		HYELET	9008732
1		EMULE FLIF CHIP (MAGENTA)	9008337-6
4	W1,W2,W3,W4	BUSS WIRE #22 AWG	9107500-01

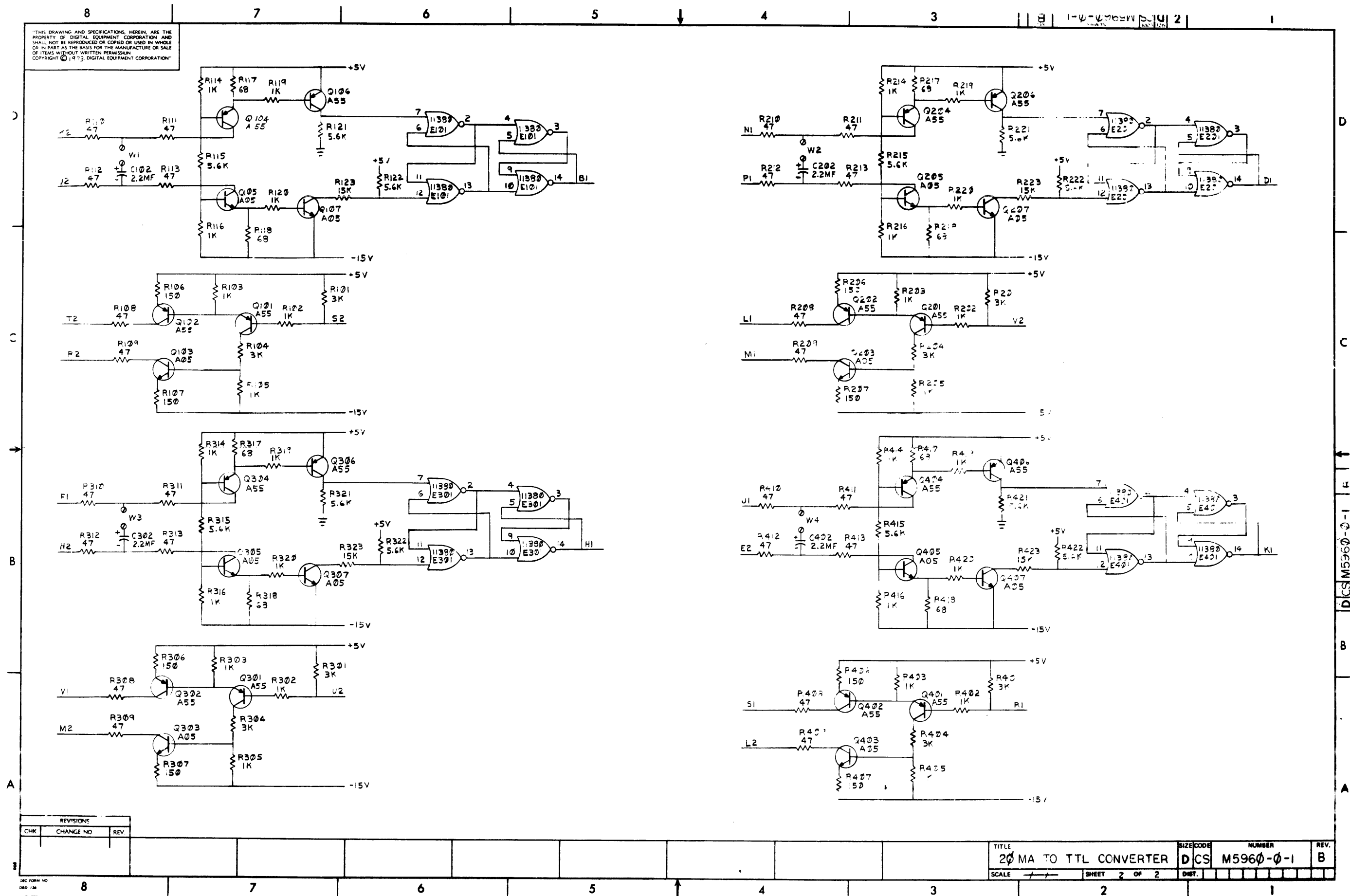
QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM
PARTS LIST				
ETCH BOARD REV	B			
		DRN <i>R. Zupke</i> DATE <i>10-2-73</i> CHG <i>Pat. Zupke</i> DATE <i>10-10-73</i> DRN <i>R. Zupke</i> DATE <i>10-17-73</i> PROBLEM <i>R. Zupke</i> DATE <i>11-12-73</i> PROD. <i>R. Wolf</i> DATE <i>12-2-73</i>	EQUIPMENT CORPORATION MAYBRAD, MASSACHUSETTS	
			TITLE 20 MA TO TTL CONVERTER	
MPS A05	NA	NEXT HIGHER ASSY		
MPS A55	NA			
DEC NO.	EIA NO.	SCALE NONE	DICS M5960-0-1	B
CONVERSION CHART		SHEET OF 2 FIRST		

DEC 11380	1	8
IC TYPE	GND	+5V

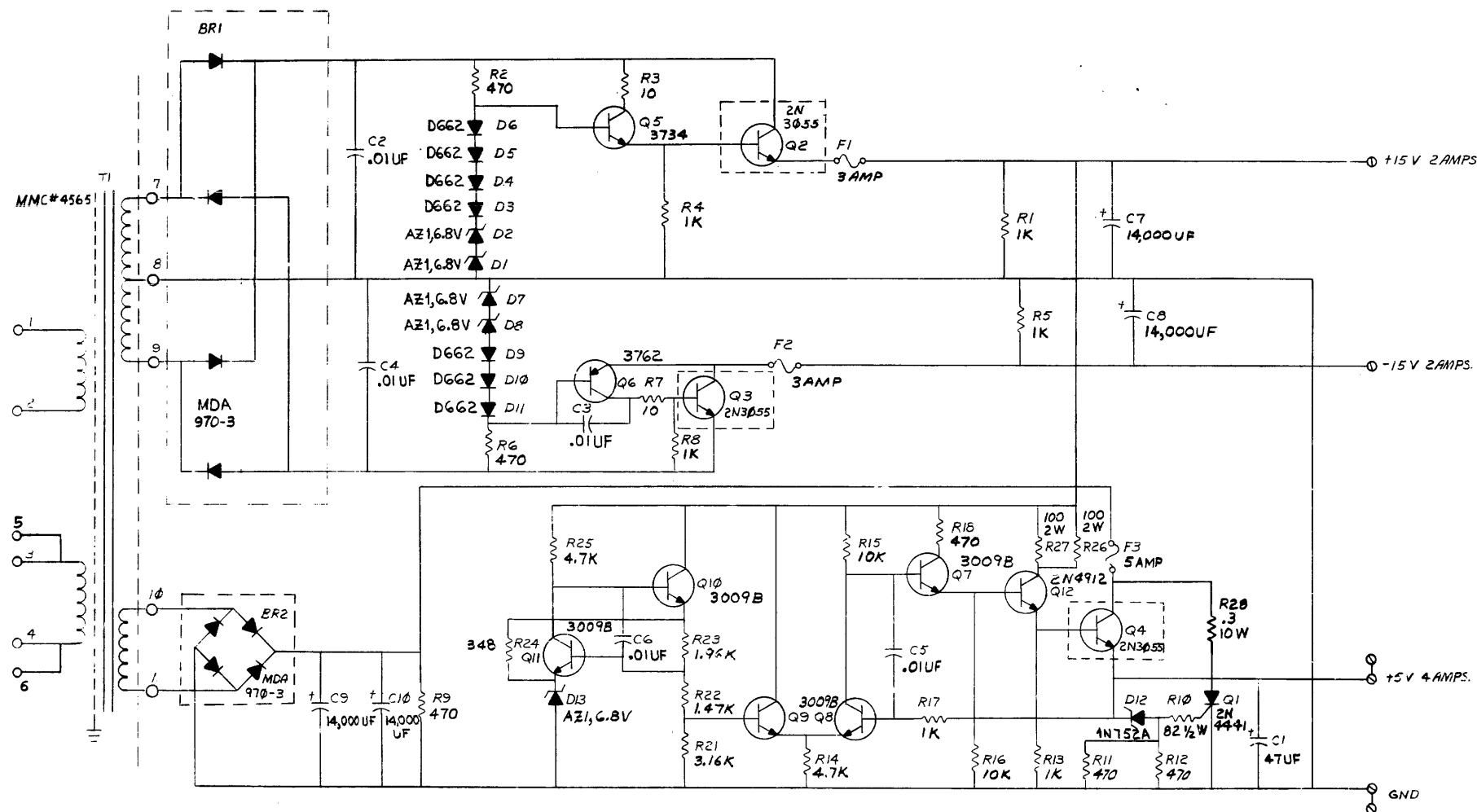
GND AND 5V ARE USUALLY PIN 7 AND 14
RESPECTIVELY. EXCEPTIONS ARE STATED ABOVE.

IC PIN LOCATIONS

DEC FORM NO
DRO-135A



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O INDICATES HOLES FOR DIODE BRIDGE
Q2, Q3, Q4, BR2 & T1 ARE MOUNTED ON
CHASSIS/HEAT SINK

QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST				
ETCH BOARD REV	C			
REV				
CHANGE NO.				
REVISIONS				
CHK				
DEC NO.	EIA NO.	DEC NO.	EIA NO.	
SEMICONDUCTOR CONVERSION CHART				
SCALE				
SHEET	2 OF 2			
EQUIPMENT CORPORATION BARTON, MASSACHUSETTS				
CASSETTE POWER SUPPLY				
DCS 5410131-0-1				