# AD11-K
## analog to digital converter
## user manual

See Note's IN BACK

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## CONTENTS

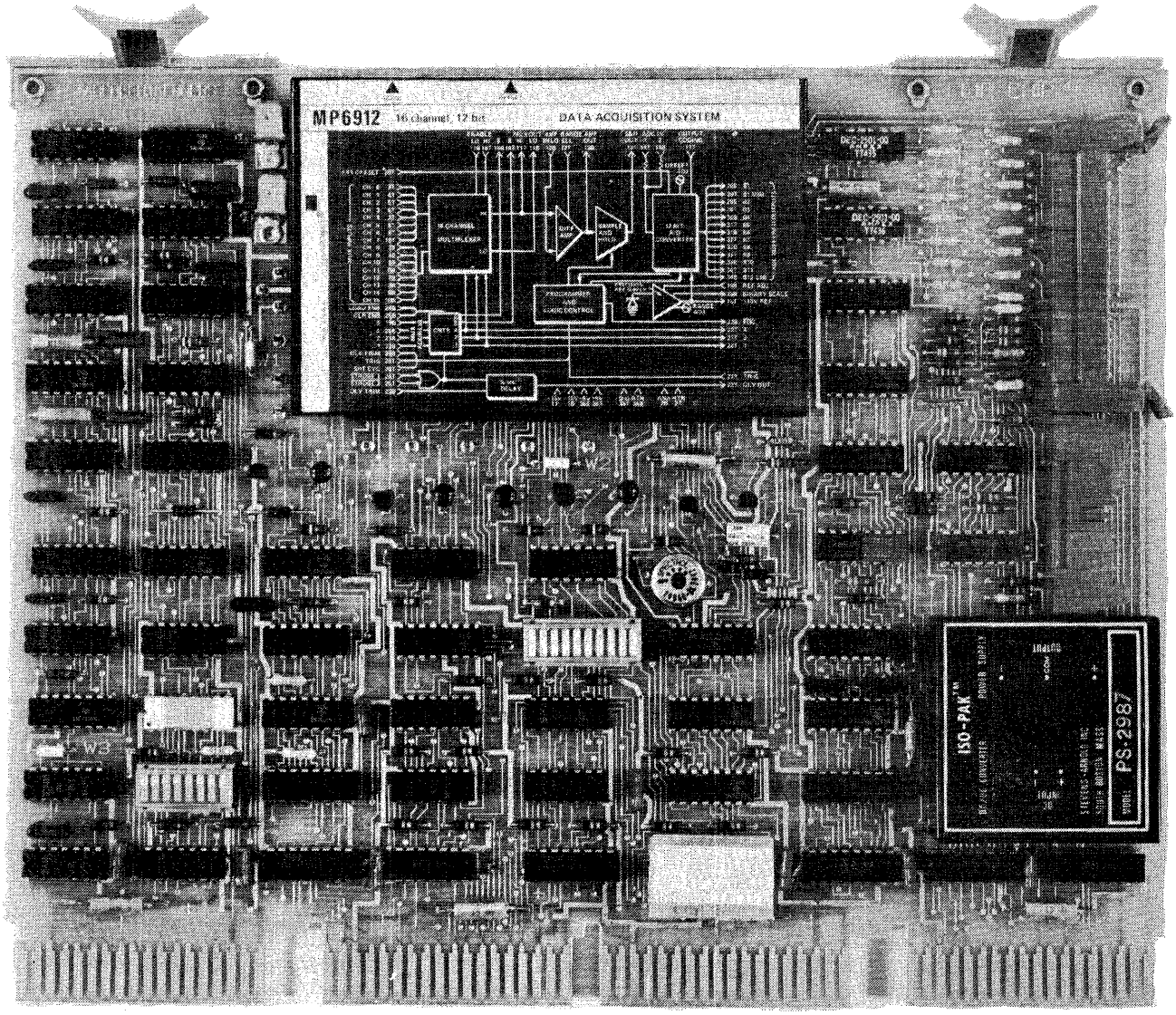


## ILLUSTRATIONS

## ILLUSTRATIONS (Cont)



## TABLES




AD11-K Module

# CHAPTER 1
# DESCRIPTION

## 1.1 GENERAL DESCRIPTION

The AD11-K, Analog-to-Digital (A/D) Converter, enables the user to sample analog data at specified rates and to store the equivalent digital value for subsequent processing. The basic subsystem consists of an input multiplexer (switch-selectable between 16-channel single-ended or 8-channel differential), sample-and-hold circuitry, and a 12-bit A/D converter. By changing jumpers, the analog inputs can be made bipolar or unipolar. The inputs over all ranges are over-voltage protected. The AD11-K has built-in self test circuitry when used in conjunction with the G5036 wrap-around module. A ±8 V ramp circuit and ±2 V 8-bit D/A converter are used to test the A/D converter and are also available for user use. A block diagram of the AD11-K is shown in Figure 1-1.

## 1.2 FUNCTIONAL DESCRIPTION

The AD11-K is a 12-bit successive approximation converter where the data is right-justified in offset binary. It is controlled by the A/D Status Register.

An A/D conversion may be initiated in any of three ways: Under program control, on overflow from a real-time clock, or on an external input. These methods give the system the flexibility to serve in most applications requiring data acquisition.

The user can switch-select operation in single-ended or differential mode. In single-ended mode, up to 16 single-ended (Figure 1-2) or pseudo-differential (Figure 1-3) channels of analog input can be selected. In true differential mode, up to eight differential channels of analog input can be selected (Figure 1-4). The input channel is selected by the status register. Input voltage range can be changed from the standard setup of ±5 V to ±5.12 V, ±10 V, ±10.24 V, 0 to 10 V or 0 to 10.24 V by configuring jumpers on the module.

When a conversion is complete, a flag is set and, if the A/D interrupt is enabled, the processor will interrupt (vector) to the proper subroutine for data manipulation. The user can run in the interrupt mode or wait to see the A/D done flag.

The multichannel throughput rate is 50 kHz using a PDP-11/10 computer (start conversion to memory). Since the converted value is held in a buffer register, a second conversion can be started before the results of the first conversion are read, thus achieving high throughput.

The digital-to-analog converter (DAC) has no control logic, so software must provide the proper settling delay (approximately 30 μsec). The DAC is an 8-bit converter with an 8-bit buffer register. The D/A output range is ±2 V. Normally, the DAC is used for maintenance to test the A/D converter via the G5036 wrap-around module; however, the output is made available for the user.

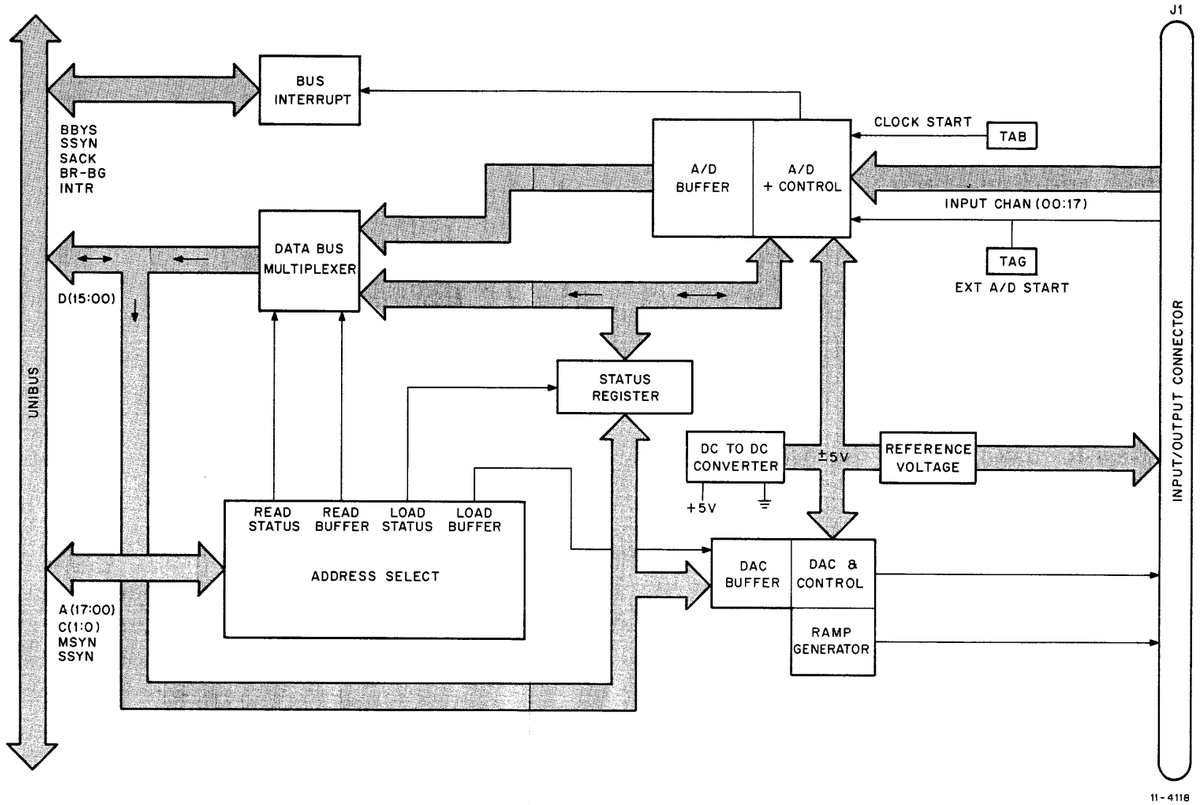



Figure 1-1 AD11-K Block Diagram

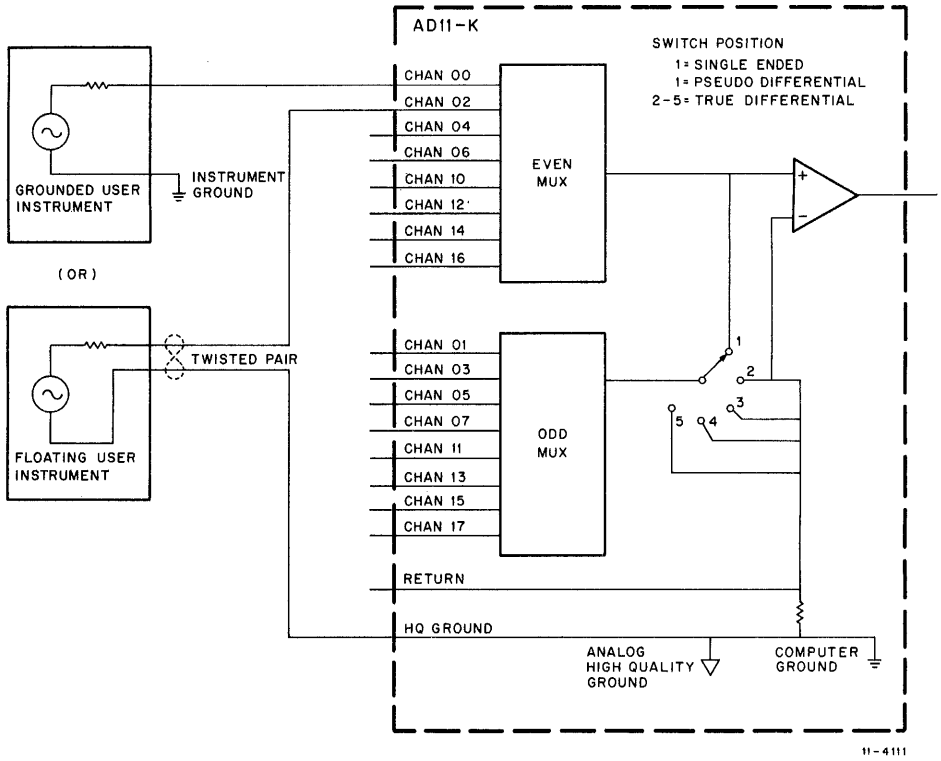



Figure 1-2 Single-Ended Input

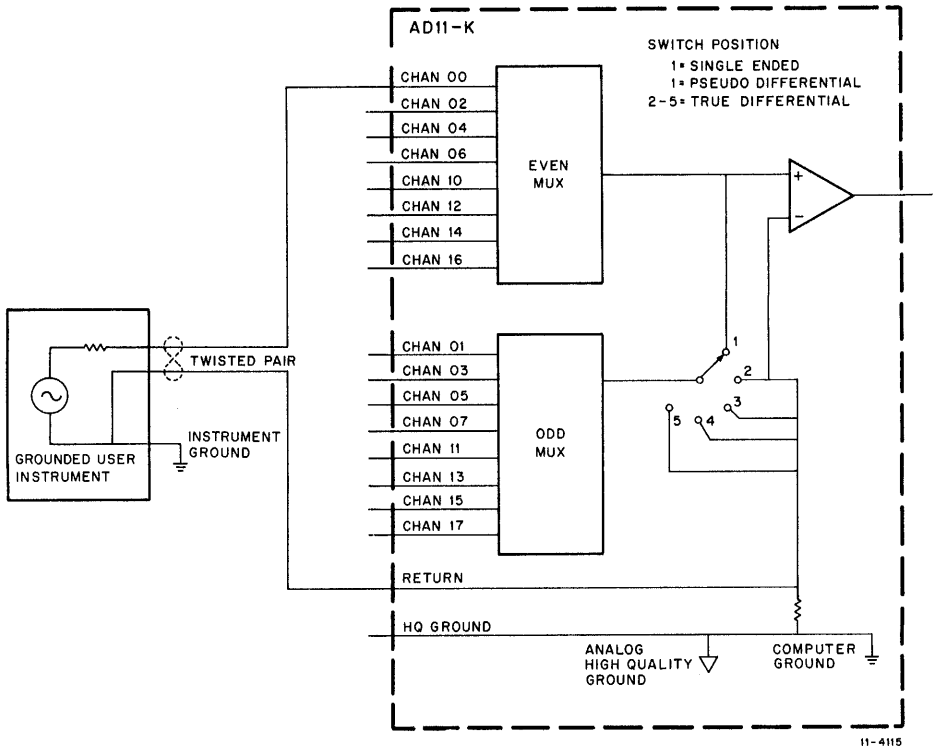



Figure 1-3 Pseudo-Differential Input

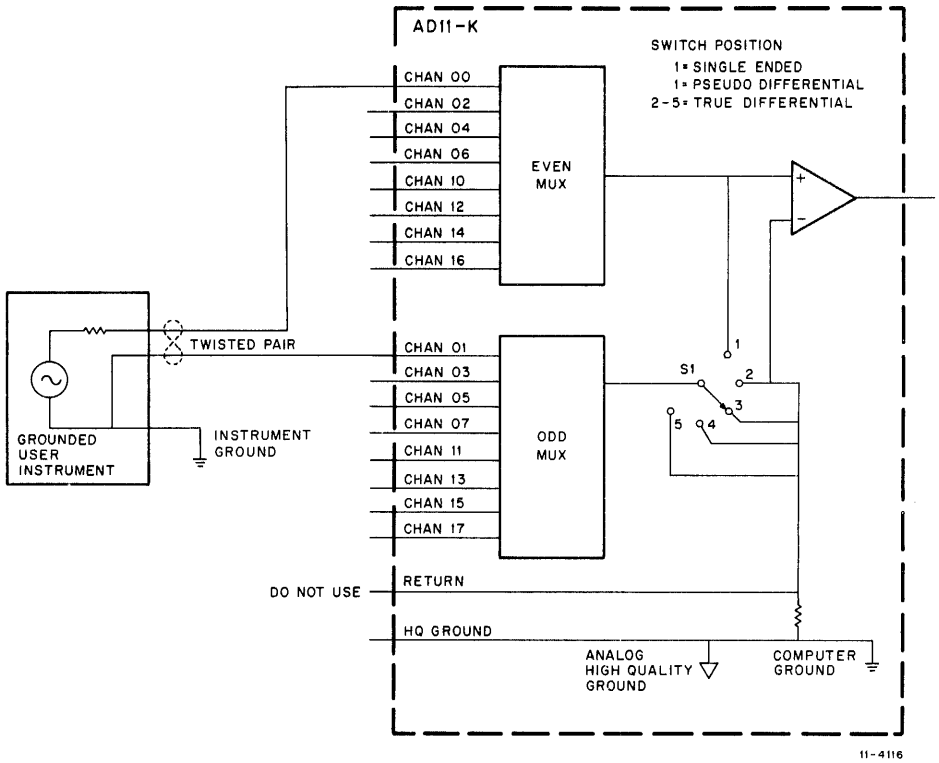



Figure 1-4 True Differential Input

## 1.3 A/D CONVERTER SPECIFICATIONS

**General**

| | |
|---|---|
| 12-bit A/D converter with sample-and-hold | |
| Accuracy at 25° C | 0.025% of full scale |
| Number of channels | 16 (single-ended or pseudo-differential)<br>8-true differential |
| SPC - Quad module | |
| Program - Compatible with LPS11 | |
| Pin - Compatible with AR11 at Berg connector (H854) | Uses H322 panel<br>Uses same wrap-around module |
| Expansion capabilities | 64 (single-ended or pseudo-differential)<br>32 (true differential) |
| Control | Controlled by programmed instructions, clock counter overflow, or external input |
| Output Format | Parallel, 12-bit, right justified, offset binary, double buffered |
| Warm-up time | Five minutes |
| Power | +5 Vdc at 3.5 A (max) |

**Accuracy**

| | |
|---|---|
| Relative accuracy (linearity) | 0.025% full scale |
| Differential linearity guaranteed | No shipped states, no states wider than 2 LSB<br>99% of states ± 1/2 LSB |

| | |
|---|---|
| **Stability** | |
| Gain temperature coefficient | 12 ppm/° C, 20° C/LSB at full scale |
| Linearity temperature coefficient | 3 ppm of F.S./° C, 81° C/LSB |
| Offset temperature coefficient | 10 ppm of F.S./° C, 24° C/LSB |
| Recommended calibration interval (two adjustments) | 6 months |
| **Repeatability** | |
| Rms Noise ($\delta$) | 1/2 LSB (max) |
| **Inputs** | |
| Bias current | 10 na (max) |
| Input impedance | 10 megohms (min)<br>10 pF (max) OFF channel<br>100 pF (max) ON channel |
| Input Voltage Range | Standard setup: ±5 V<br>Optional Setup: ±5.12 V, ±10 V, ±10.24 V, 0 to 10 V or 0 to 10.24 V |
| Resolution | 12 bits (1 part in 4096) |
| **Signal Dynamics** | |
| Throughput time | 22 $\mu$sec (includes interchannel settling and A/D conversion) |
| Inter-channel settling error | 1 LSB (max) |
| Crosstalk | 80 dB down at 1 kHz<br>(15 OFF channels into one ON channel) |
| Differential CMRR | 70 dB (dc to 1 kHz) |
| Small signal bandwidth | 500 kHz typical |
| Slew rate limit | 7 V/$\mu$sec |
| Sample-and-hold aperture | 200 nsec typ, delay from external start<br>165nsec typ, delay from clock overflow<br>20 nsec max, delay uncertainty |

## 1.4 PACKAGING

The AD11-K is a single quad-size module (A009) which mounts in a PDP-11 SPC slot. The RFI shields included with this option should be mounted on each side of the A009 module. These shields do not require a Unibus slot. To minimize computer noise within the analog circuitry, it is recommended that the AD11-K be mounted so that at least one slot adjacent to each side of the A009 module is left empty, or so that the A009 module is the last module on the bus assembly with adjacent slots left empty.

## 1.5 POWER REQUIREMENTS

The AD11-K module (A009) only uses +5 Vdc at 3.5 A max. A dc to dc converter package, powered by the +5 Vdc, is used to supply ±15 Vdc to the analog portions of the module.

## 1.6 UNIBUS LOADING

All Unibus lines are one unit load, except data lines 03 through 08, which are two unit loads.

# CHAPTER 2
# USER INTERFACING

## 2.1 CONNECTION

Input signals are interfaced to the AD11-K by a 40-pin I/O connector (H854) located in the upper right corner of the A009 module. The 40-pin I/O connector can take a standard BC08R cable or a user-made cable terminated with an H856 40-pin I/O connector. The pin assignments are shown below:

| Signal | Pin |
|---|---|
| Channel 0 | VV |
| Channel 1 | TT |
| Channel 2 | RR |
| Channel 3 | NN |
| Channel 4 | LL |
| Channel 5 | JJ |
| Channel 6 | FF |
| Channel 7 | DD |
| Channel 10 | BB |
| Channel 11 | Z |
| Channel 12 | X |
| Channel 13 | V |
| Channel 14 | T |
| Channel 15 | R |
| Channel 16 | N |
| Channel 17 | L |
| External A/D Start | U |
| DAC Output | F |
| H.Q. Ground | KK, EE, AA, W |
| Return | Y, CC, HH, MM |
| Computer Ground | P, S |
| Ramp Output | J |

## 2.2 H322 DISTRIBUTION PANEL

Figure 2-1 shows an H322 distribution panel. A decal set for the AD11-K identifies each terminal of the H322 to be connected to the A009 module. Persons who want to use the H322 distribution panel can order these options together under the AD11-KT option designation, which consists of an H322, AD11-K, and one BC08R cable eight feet (243.84 cm) long.

## 2.3 SINGLE-ENDED AND PSEUDO-DIFFERENTIAL INPUTTING

Setting switch S1 to the 1 position will allow the AD11-K to operate in either single-ended or pseudo-differential input (Figures 1-2 and 1-3). The only difference between single-ended and pseudo-differential is that in single-ended the analog input is referenced to ground (Paragraphs 2.4.1 and 2.4.2), and in pseudo-differential the analog input is referenced to a common return (Figure 1-3). This permits advantages of differential input in situations where all the signals share a single ground line. The channel selection is shown in Table 2-1.

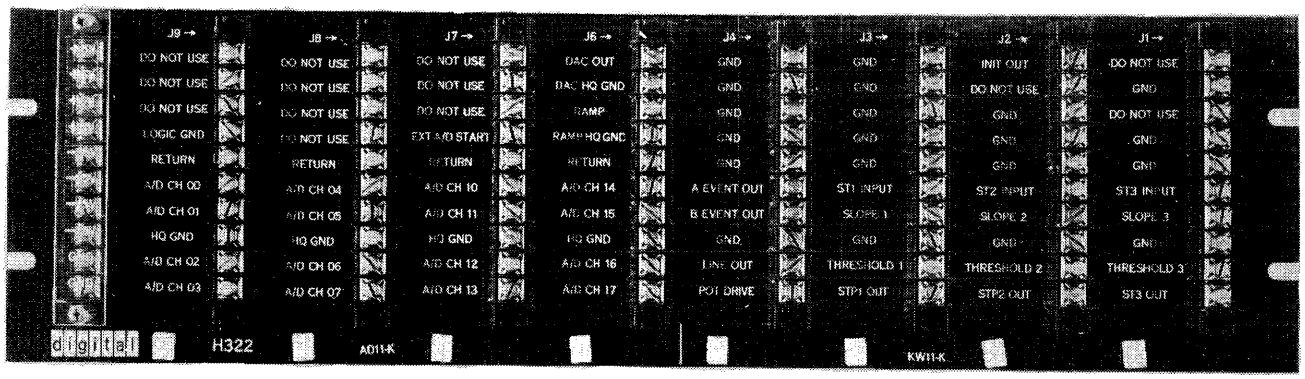



Figure 2-1 H322 Distribution Panel

Table 2-1
Channel Selection

| Status Register Mux Selection | | | | | | Input Channel Code | Pin Connection |
|---|---|---|---|---|---|---|---|
| 13 | 12 | 11 | 10 | 09 | 08 | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 00 | VV |
| 0 | 0 | 0 | 0 | 0 | 1 | 01 | TT |
| 0 | 0 | 0 | 0 | 1 | 0 | 02 | RR |
| 0 | 0 | 0 | 0 | 1 | 1 | 03 | NN |
| 0 | 0 | 0 | 1 | 0 | 0 | 04 | LL |
| 0 | 0 | 0 | 1 | 0 | 1 | 05 | JJ |
| 0 | 0 | 0 | 1 | 1 | 0 | 06 | FF |
| 0 | 0 | 0 | 1 | 1 | 1 | 07 | DD |
| 0 | 0 | 1 | 0 | 0 | 0 | 10 | BB |
| 0 | 0 | 1 | 0 | 0 | 1 | 11 | Z |
| 0 | 0 | 1 | 0 | 1 | 0 | 12 | X |
| 0 | 0 | 1 | 0 | 1 | 1 | 13 | V |
| 0 | 0 | 1 | 1 | 0 | 0 | 14 | T |
| 0 | 0 | 1 | 1 | 0 | 1 | 15 | R |
| 0 | 0 | 1 | 1 | 1 | 0 | 16 | N |
| 0 | 0 | 1 | 1 | 1 | 1 | 17 | L |

## 2.4 SINGLE-ENDED ANALOG INPUTS

### 2.4.1 Grounded Inputs

Two types of analog signals may be used as AD11-K inputs - grounded and floating. A grounded signal level is referenced to the ground of the instrument that is producing the signal (Figure 2-2). Since the instrument may be located some distance from the computer, there may be some voltage difference between the instrument ground and the computer ground. The voltage seen by the AD11-K single-ended input is the sum of this unwanted ground difference voltage and the desired signal voltage.

In cases where the input voltage is referenced to the user's ground, a wire should *not* be run from the user's ground to the AD11-K analog ground; this could cause undesirable ground loop currents which affect results not only on the input channel in question, but also on other channels. The ground difference should be minimized by plugging the instrument into an ac socket as close to the computer as possible.

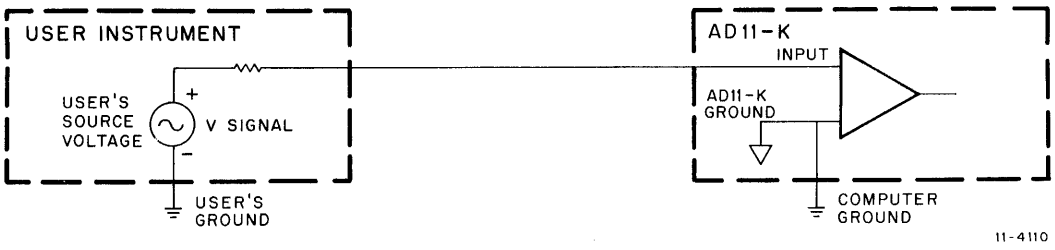



Figure 2-2 AD11-K Input Referenced to User's Ground

### 2.4.2 Floating Inputs

A floating signal voltage is measured with respect to a point that is not connected to ground. Examples of this type of analog input are shown in Figure 2-3.

The return line of a floating signal must be connected to one of the AD11-K analog input grounds (Paragraph 2.1). Although there are only four analog input grounds for the 16 analog channels, these grounds may be shared among channels. The identifying characteristic of a floating source is that connecting the signal return to the AD11-K ground does not result in a current path between the AD11-K ground and the instrument ground.

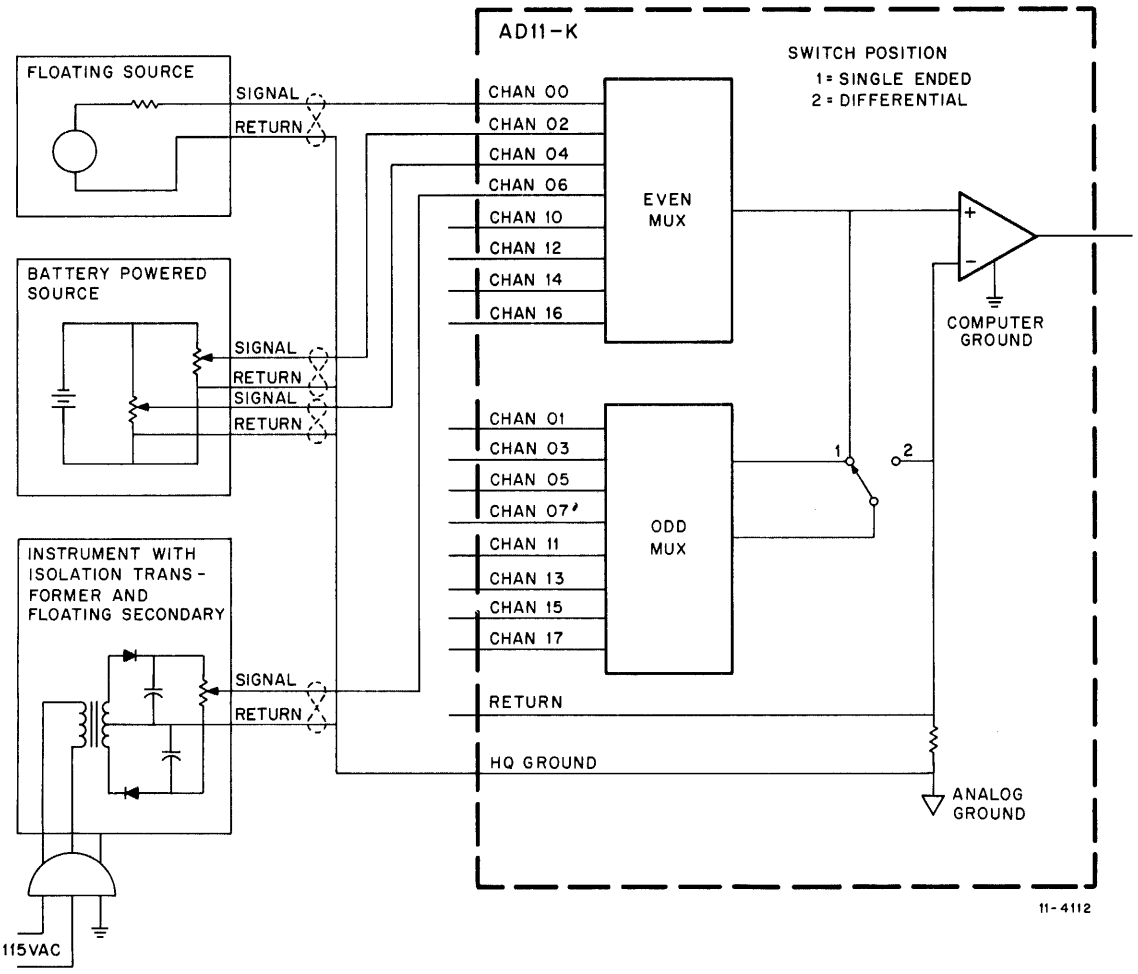



Figure 2-3 Floating AD11-K Input Signals

## 2.5 TRUE DIFFERENTIAL INPUTTING

Setting switch S1 to position 2, 3, 4 or 5 will electrically pair input lines for true differential input operation (Figure 1-3). The least significant bit of the channel selection (Status register bit 08) is ignored. The channel pair selection is shown in Table 2-2.

Table 2-2
Channel Pair Selection

| Status Register Mux Selection | | | | | | New Channel Code | Input Channel Pair | | Pin Connection | |
|---|---|---|---|---|---|---|---|---|---|---|
| 13 | 12 | 11 | 10 | 09 | 08 | | + | - | + | - |
| 0 | 0 | 0 | 0 | 0 | X | 00 | 00 | 01 | VV | TT |
| 0 | 0 | 0 | 0 | 1 | X | 02 | 02 | 03 | RR | NN |
| 0 | 0 | 0 | 1 | 0 | X | 04 | 04 | 05 | LL | JJ |
| 0 | 0 | 0 | 1 | 1 | X | 06 | 06 | 07 | FF | DD |
| 0 | 0 | 1 | 0 | 0 | X | 10 | 08 | 09 | BB | Z |
| 0 | 0 | 1 | 0 | 1 | X | 12 | 10 | 11 | X | V |
| 0 | 0 | 1 | 1 | 0 | X | 14 | 12 | 13 | T | R |
| 0 | 0 | 1 | 1 | 1 | X | 16 | 14 | 15 | N | L |

## 2.6 TWISTED PAIR INPUT

The affects of magnetic coupling on the input signals may be reduced for floating or differential inputs by twisting the signal and return lines in the input cable. If the inductive pickup voltages of the two leads match, the net effect seen at the AD11-K input is zero. Twisted pairs have no affect with a single-ended, non-floating signal (referenced to ground at the instrument end).

## 2.7 SHIELDED INPUT

The affects of electrostatic coupling on the input signals may be reduced by shielding the signal wires. This is especially important if the instrument or transducer has high source impedance. The shield should be connected to ground at one end of the cable only so that it does not carry any current.

## 2.8 INPUT SETTLING WITH HIGH SOURCE IMPEDANCE

All solid-state multiplexers have the unavoidable side affect of injecting a small amount of charge into their input lines when changing channels, causing a transient error voltage which is discharged by the input signal's source impedance.

When starting a conversion, a 10 $\mu$sec interval is allowed for the AD11-K multiplexer and sample-and-hold to settle to the correct value of the newly-selected channel before the conversion begins. Normally, this is sufficient time for the input transient to settle out; however, more time may be needed when switching into an input channel with high source impedance. It may be necessary to either reduce the signal's source impedance or preset the multiplexer channel and provide a software delay before starting the conversion.

## 2.9 EXTERNAL STARTS

The external start signal line, pin U of the 40-pin I/O connector (H854) or TAB2, is a TTL-compatible input which sees two TTL unit loads (3.2 mA). Conversions start on the high-to-low transition of this signal.

In most cases, the source of the external start signal is a grounded (non-floating) signal generator or logic circuitry located in a grounded instrument. Like the analog input signal, the return path for the External Start signal is through the grounds, and a separate return wire should not be run. The ground difference between the signal source and the computer should be minimized to prevent spurious start pulses due to ground noise.

In the case of a floating pulse generator only, the pulse generator's logic ground should be connected to the AD11-K's logic ground pins of the I/O connector.

When the AD11-K is used with the KW11-K programmable real-time clock, the output of Schmitt trigger one of the KW11-K is available at a FAST-ON TAB (also possessed by the AD11-K). By using a DEC 7010771 type jumper (Figure 2-4), the KW11-K's Schmitt trigger one output can be jumpered to the AD11-K's External Start input within the central processor cabinet.

## 2.10 JUMPERS

The AD11-K is equipped with solder jumpers (Figure 2-5) which may be changed by the user. The jumper functions and identifications are listed in Table 2-3. The jumper configuration must be set up for ±5 V or ±5.12 V input range when testing with the wrap-around module. Input range jumper setup is as shown in Table 2-4.

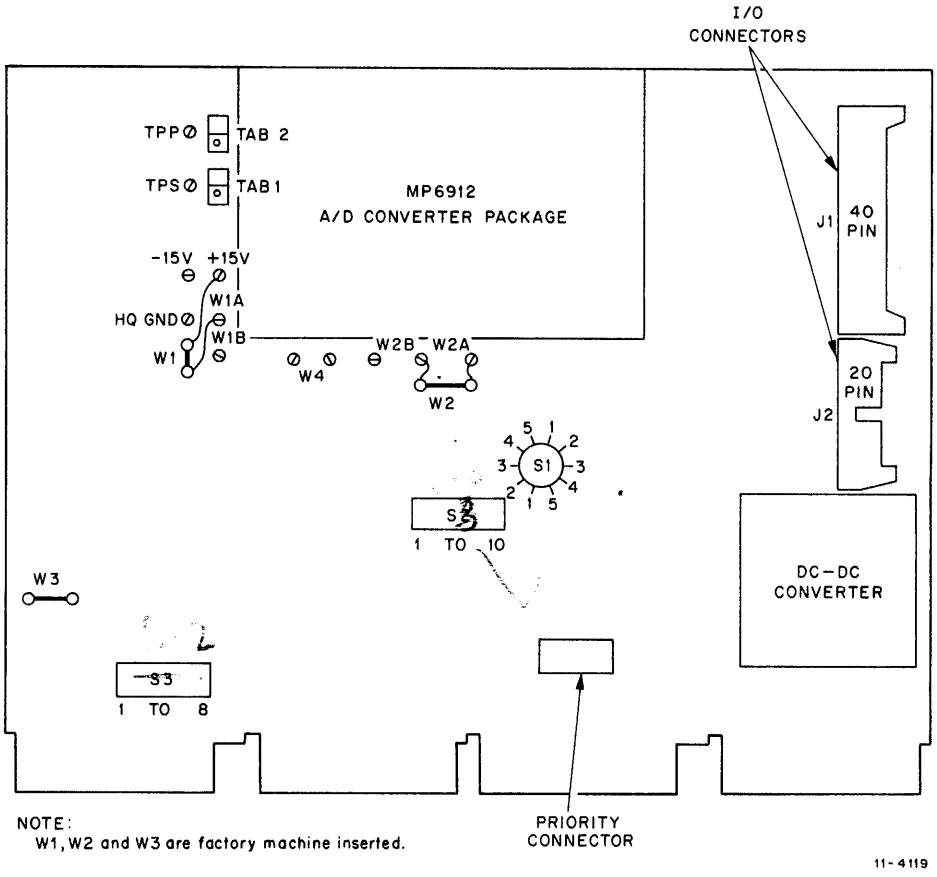



Figure 2-4 A009 Module

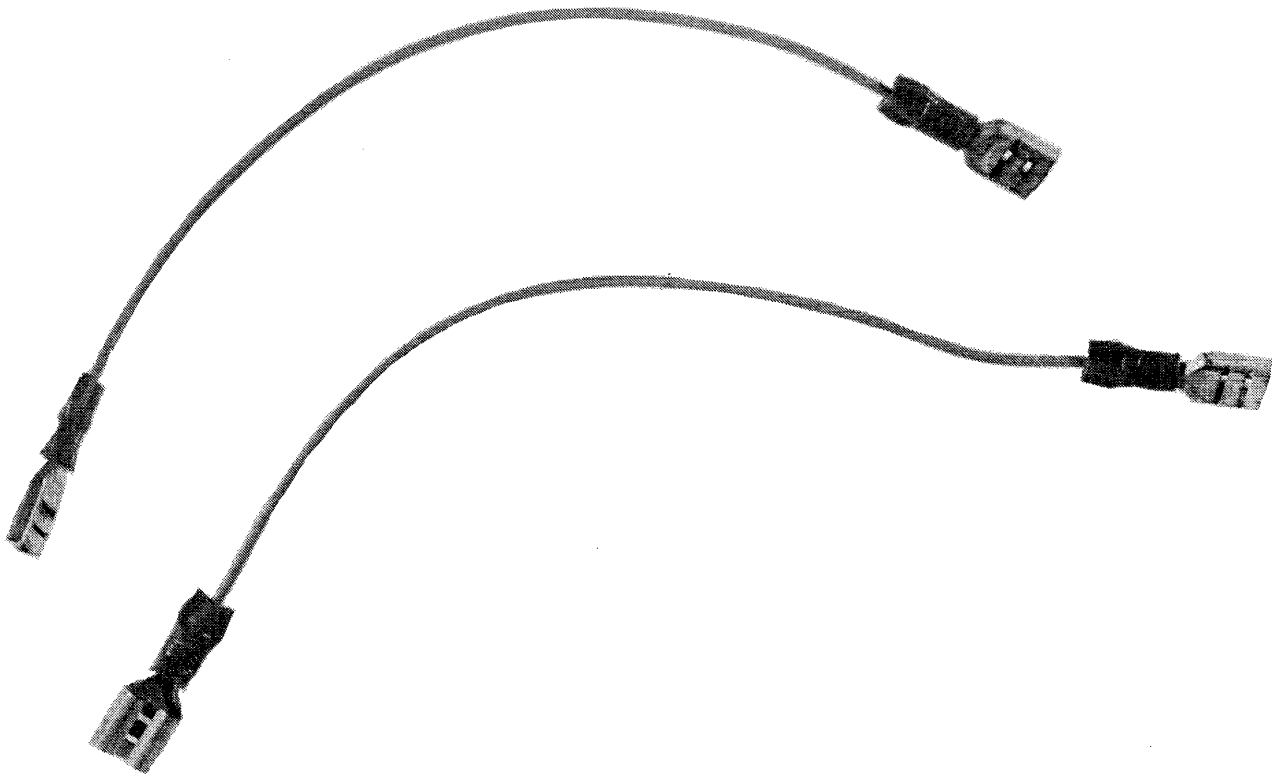


Figure 2-5 Module Jumpers

Table 2-3
A009 Jumper Descriptions

| Jumper ID (See Figure 2-4) | Description |
|---|---|
| W1 – Factory Installed<br>W1A – User Installed | Bipolar Input |
| W1B – User Installed | Unipolar Input |
| W2 – Factory Installed<br>W2A – User Installed | 5 V Input |
| W2B – User Installed | 10 V Input |
| W3 – Factory Installed | NPR – Removed only if PDP-11/20 or 11/15 without a KH11 option |
| W4 – User Installed | ±5.12 V, ±10.24 V, or 0 → +10.24 V Input |

Table 2-4
A009 Input Range Jumpers

| Jumper | Input Range | | | | | |
|---|---|---|---|---|---|---|
| | ±5 V Standard | ±10 V | 0 to +10 V | ±5.12 V | ±10.24 V | 0 to +10.24 V |
| W1* | In | In | Out | In | In | Out |
| W1A | In | In | Out | In | In | Out |
| W1B | Out | Out | In | Out | Out | In |
| W2* | In | Out | Out | In | Out | Out |
| W2A | In | Out | Out | In | Out | Out |
| W2B | Out | In | In | Out | In | In |
| W4 | Out | Out | Out | In | In | In |

*Once W1 and W2 are removed, they are not to be re-installed. These jumpers are paralleled by jumpers W1A and W2A respectively.

## 2.11 SWITCHES

A double pole switch (Figure 2-4) is provided for switching between single-ended and differential input configurations. When S1 is in position 2, 3, 4 or 5, the AD11-K is in true differential configuration and when S1 is in position 1, the AD11-K is in single-ended or pseudo-differential configuration. Single pole/single throw switches in switch packs are used to change the register and vector addressing (Paragraph 3.1) of the AD11-K. The switch identification for the address lines and vector lines is shown in Tables 2-5 and 2-6, respectively. Register address lines are switched on for a logical 0; vector address lines are switched on for a logical 1.

Table 2-5
Address Line Selection

| Switch | Address Line |
|---|---|
| Not Selectable | A15 |
| Not Selectable | A14 |
| Not Selectable | A13 |
| S2-10 | A12 |
| S2-9 | A11 |
| S2-8 | A10 |
| S2-7 | A09 |
| S2-6 | A08 |
| S2-5 | A07 |
| S2-4 | A06 |
| S2-3 | A05 |
| S2-2 | A04 |
| S2-1 | A03 |
| S3-8 | A02 |
| Not Selectable | A01 |
| Not Selectable | A00 |

Table 2-6
Vector Line Selection

| Switch | Vector Line |
|---|---|
| S3-1 | D3 |
| S3-2 | D4 |
| S3-3 | D5 |
| S3-4 | D6 |
| S3-5 | D7 |
| S3-6 | D8 |

## 2.12 OVERFLOW OR EXTERNAL START CONNECTION

Two FAST-ON TABS are available on the A009 for inputting signals from the KW11-K programmable real-time clock option. The KW11-K (M7025) also has two FAST-ON TABS (Figure 2-6) for outputting two signals - A Overflow and Schmitt trigger one. These signals can be jumpered between the A009 and M7025 models by using DEC 7010771 type jumpers (included with the AD11-K). This allows for signal connection within the processor cabinet and does not interfere with the regular I/O connector on each module. TAB 1 of the KW11-K is A Overflow and is re-named A Event Out. This can be jumpered to TAB 1 of the AD11-K, which is called KW Overflow.

TAB 2 of the KW11-K is Schmitt Trigger one. This can be jumpered to TAB 2 of the AD11-K, which is called External Start.

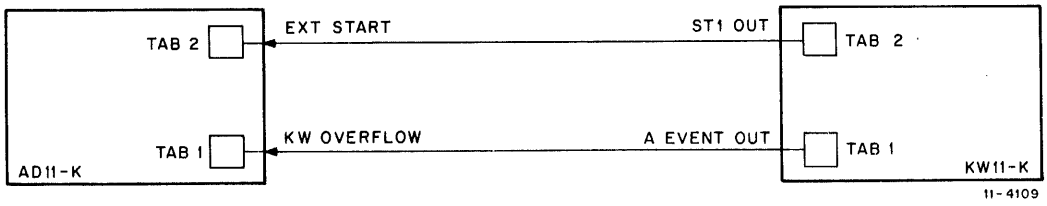



Figure 2-6 Tab Connections

# CHAPTER 3
# PROGRAMMING

## 3.1 REGISTER AND VECTOR ADDRESSING

Register and vector addresses are configured prior to shipment in standard configurations, but may be changed by means of switches on the A009 module. Paragraph 2.11 describes the procedure for changing the register and vector addresses.

The AD11-K has a floating address to allow the use of more than one AD11-K in a system, or to avoid any device address conflict with other options. The register address is selected by switches on the A009 module representing address lines A12 through A02. The standard register addresses selected for the AD11-K are:

170400 R/W – Status register

170402 Write – Loads DAC buffer register

Read – Reads A/D buffer register

The vector address is selected by switches on the A009 module representing vector lines (Unibus "D" Lines) D08 through D03. The standard vector address selected for the AD11-K is $340_8$.

## 3.2 PRIORITY LEVEL

The A009 is normally shipped with a priority level configuration of BR6; this level may be changed by replacing the priority connector for another level.

## 3.3 REGISTERS

### 3.3.1 Status Register

The A/D Status register is illustrated in Figure 3-1 and described in Table 3-1.

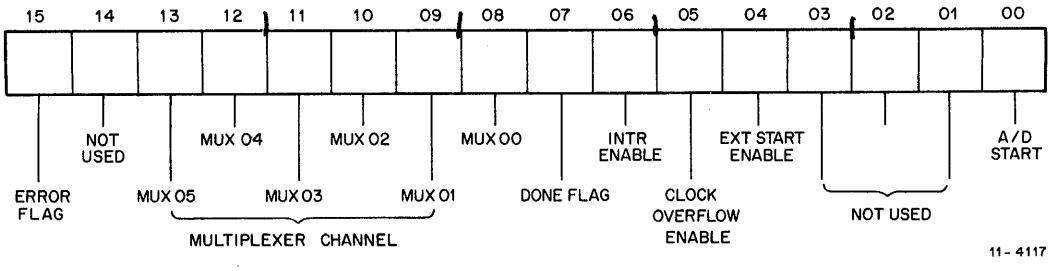



Figure 3-1 A/D Status Register Format

Table 3-1
AD11-K Status Register Bit Descriptions

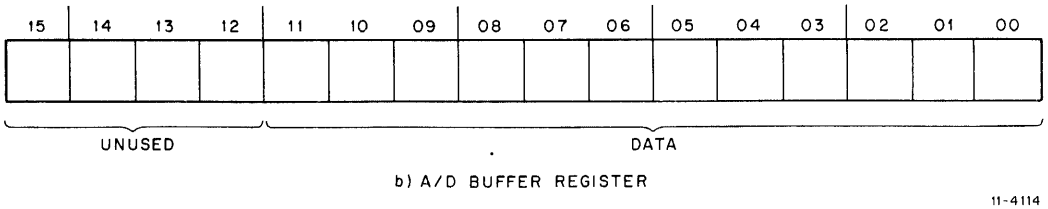
| Bit | Name | Description |
|---|---|---|
| 15 | ERROR FLAG (R/W) | This bit sets when:<br>1. A second A/D conversion ends before data from the previous A/D conversion is read.<br>2. A second A/D start is initiated before the first conversion is complete. |
| 13–8 | Mux Channel (R/W) | Defines which A/D input channel of the multiplexer is to be sampled. |
| 7 | DONE FLAG (R) | Sets upon completion of an A/D conversion. Cleared by hardware when the A/D interrupt bus cycle is completed or when the buffer register is read. |
| 6 | INTERRUPT ENABLE (R/W) | When a conversion is completed, the done flag will cause an interrupt if this bit is set. |
| 5 | OVERFLOW ENABLE (R/W) | Permits overflow from KW11-K Real-Time Clock to cause an A/D start. This allows channel sampling at precisely timed intervals independent of software. Data may then be read by testing the A/D done flag or by enabling the interrupt. |
| 4 | EXTERNAL START ENABLE (R/W) | Permits an external event to initiate an A/D conversion. |
| 0 | A/D Start (R/W) | Starts an A/D conversion. Cleared at end of conversion. |

### 3.3.2 A/D Buffer Register

The A/D Buffer register is a read only register. It furnishes the 12-bit converted value, formatted in 12-bit right-justified offset binary after an A/D conversion is complted (Figure 3-2).

| 12-BIT RESULTS (OCTAL) | INPUT VOLTAGE RANGE | | | | | |
|---|---|---|---|---|---|---|
| | ±5V | ±5.12V | ±10V | ±10.24V | 0-10V | 0-10.24V |
| 007777 | +4.9976V | +5.1175V | +9.9951V | +10.235V | +9.9976V | +10.2375V |
| 004000 | 0V | 0V | 0V | 0V | +5.0V | +5.12V |
| 000000 | -5.0V | -5.120V | -10.0V | -10.240V | 0V | 0V |
| RESOLUTION | 2.44MV | 2.5MV | 4.88MV | 5.0MV | 2.44MV | 2.5MV |

a) A/D RANGE CHART




b) A/D BUFFER REGISTER

11-4114

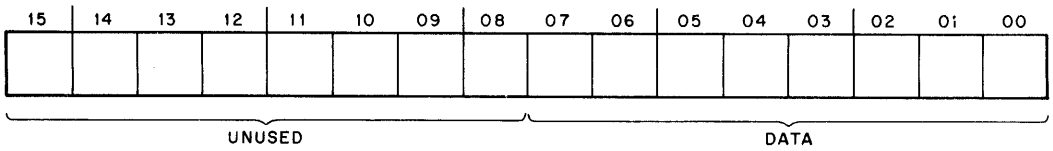
Figure 3-2 A/D Buffer Register Format

### 3.3.3 DAC Buffer

The DAC Buffer is a write only register. It is a 8-bit register which holds the digital value to be converted to an analog signal (Figure 3-3).

| 8-BIT INPUT (OCTAL) | OUTPUT RANGE |
|---|---|
| 000377<br>000200<br>000000 | +1.860V<br>0V<br>-1.875V |
| RESOLUTION | 14.64mV |

a) DAC RANGE CHART




NOTE:
ONE LSB = 19.4 mV

b) DAC REGISTER

11-4113

Figure 3-3 DAC Buffer Register Format

## 3.4 PROGRAMMING EXAMPLE

Read $64_{10}$ ($100_8$) A/D conversions from channel 0 into locations $4000_8$ - $4176_8$ and halt.

```
            R0=%0

START:      CLR     @ADSR       ;CLEAR A/D STATUS REGISTER
            MOV     #4000,R0    ;SET UP FIRST ADDRESS
            INC     @ADSR       ;START A/D CONVERSION ON CHANNEL 0

LOOP:       TSTB    @ADSR       ;CHECK DONE FLAG
            BPL     LOOP        ;WAIT UNTIL FLAG SET
            INC     @ADSR       ;START NEXT CONVERSION
            MOV     @ADBR,(R0)+ ;PLACE CONVERTED VALUE FROM A/D
                                ;BUFFER INTO CORE LOCATION AND SET UP
                                ;NEXT CORE LOCATION FOR TRANSFER
            CMP     R0,#4200    ;CHECK IF 64. CONVERSIONS HAVE BEEN
                                ;DONE
            BNE     LOOP        ;NO, GET NEXT CONVERSION
            HALT                ;DONE

ADSR:       170400              ;A/D STATUS REGISTER ADDRESS
ADBR:       170402              ;A/D BUFFER REGISTER ADDRESS

            .END    START
```

# GLOSSARY OF A/D TERMS

*Absolute Accuracy*
The analog error, expressed as a percentage of full scale, referenced to the National Bureau of Standards volt.

*Acquisition Time*
The time duration between the giving of the sample command and the point when the output remains within a specified error band around the input value.

*Aperture Delay Time*
The time elapsed between the hold command and the point at which the sampling switch is completely open.

*Aperture Uncertainty*
The variation in aperture delay time for a particular sample-and-hold.

*Common Mode Rejection (CMR)*
The ability of a differential amplifier to reject noise common to both inputs. Common mode rejection is expressed as a ratio, the Common Mode Rejection Ratio (CMRR). A differential amplifier with a CMRR of 80 dB (10,000:1) would have an output voltage of 0.5 mV if both inputs were 5 V (5 V/80 dB).

*Crosstalk*
The amount of signal coupled to the output as a percentage of input signal applied to all off channels.

*Differential Inputs (True)*
Two external signals applied to the input circuitry of an A/D system whereby the first is subtracted from the second. The difference is applied to the A/D system. This is generally used with twisted pair wiring to reduce noise pickup.

Example

$$V_O = (V+) - (V-)$$

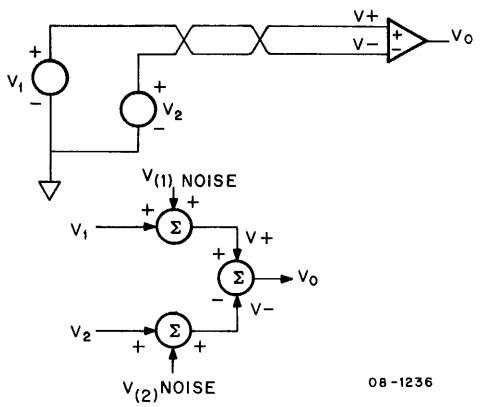
$$= [V_1 + V(_1)\text{ noise}] - [V_2 + V(_2)\text{ noise}]$$

$$= [V_1 - V_2] + [V(_1)\text{ noise} - V(_2)\text{ noise}]$$

For twisted pair wiring:

$$V(_1)\text{ noise} \doteq V(_2)\text{ noise}$$

$$\therefore V_O \doteq V_1 - V_2$$



*Differential Inputs (Psuedo)*
This method of inputting is similar to true differential inputting except that the negative input to the A/D system is common to the other inputs.

*Differential Linearity*
The maximum deviation of an actual stated width from its theoretical value for any code over the full range of the converter. A differential linearity of ±1/2 LSB means that the width of each code over the range of the converter is 1 LSB ± 1/2 LSB. Missing codes in an A/D converter occur when the output code skips a digit. This happens when the differential linearity is worse than ±1 LSB.

*Drift*
Drift is a function of the temperature coefficients of the components. It is the major contributor to gain and offset error.

*Gain Error*
The error, expressed as a percentage, by which the actual full scale range differs from the theoretical full scale range. This error is adjustable to zero.

*Gain Temperature Coefficient*
This is the amount of gain that changes with a change in temperature. This may be expressed in ppm/° C or ° C/LSB at full scale. If an A/D has a gain temperature coefficient of 20° C/LSB at F.S., the A/D converted value will be off by 1 LSB at full scale if the temperature rises 20° C above 25° C.

*Input Bias Current*
The amount of current that flows into the selected A/D channel from the source.

*Input Impedance (dc)*
The resistance seen at the input to an A/D system.

*Linearity*
Linearity is defined as the maximum deviation from a straight line drawn between the end points of the converter transfer function. Linearity may be expressed as a percentage of full scale or as a fraction of an LSB.

*Multiplexer*
The multiplexer is a set of switches that permits analog data from different sources (channels) to be supplied to the sample-and-hold (or A/D converter) individually.

*Multiplexer Settling Time*
The maximum time required to reach a specified error band around the input value when switching channels.

*Offset Error*
The error by which the transfer function fails to pass through the origin. This is usually adjustable to zero.

*Quantization Error*
Quantization error is defined as the basic uncertainty associated with digitizing an analog signal, due to the finite resolution of an A/D converter. An ideal converter has a maximum quantization error of ±1/2 LSB.

*Relative Accuracy*
This is defined as the input to output error as a fraction of full scale with gain and offset errors adjusted to zero. Relative accuracy is dependent on linearity.

*Resolution*
The resolution of an A/D converter is defined as the smallest analog change that can be distinguished. Resolution is the analog value of the least significant bit.

$$\text{Resolution} = \frac{\text{Full scale}}{\text{Least significant bit}}$$

For example, if a system requires a weight measurement range of 2540 lb, measured to the nearest 3 lb,

$$\text{Resolution} = \frac{2540}{3} = 847 \text{ code combinations}$$

The closest standard A/D converter resolution available is 10-bits binary. A binary resolution of 10-bits selected. The new resolution for this channel is recalculated for 10 bits.

$$1 \text{ LSB (least significant bit)} = \frac{\text{Full scale range}}{2^n} = \frac{2540}{1024} = 2.5 \text{ lb}$$

*Sample-and-Hold*
In order to ensure that input voltage does not change during a conversion, a sample-and-hold is required. If the change during a conversion cycle is less than 1/2 LSB, then a sample-and-hold circuit is not required.

Example

Conversion Speed = 20 $\mu$s
Full Scale Input Range (FSR) = 10.24 V
Converter Resolution = 10 bits
LSB Value = .01 V/bit
1/2 LSB = 0.005 V

Maximum slew = 0.005 V/20 $\mu$sec = 250 $\mu$V/$\mu$sec = 250 V/sec
(Rate required for no sample-and-hold)

for $e_{in} = 1/2$ (FSR) sin $\omega$ t $\qquad\qquad$ $\omega_{max} = 2$ TP (BW)

then $de/dt = (1/2)\omega$ (FSR) cos $\omega$ t

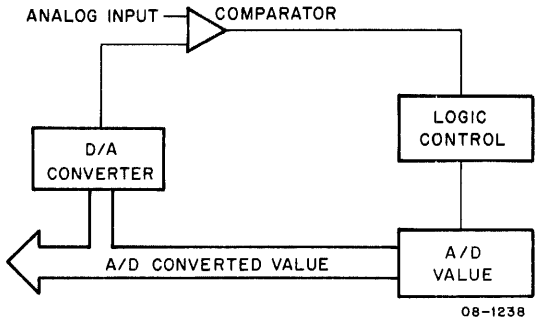
$\therefore |de/dt|_{max} = (1/2)\omega_{max}$ (FSR) = (BW) (FSR)

or 250 V/sec = $\pi$ (BW) (FSR)

BW = 250 V/sec /$\pi$ (10.24 V) $\doteq$ 7.77 Hz

*Slew Rate*
The capability of the output of an analog circuit to change its voltage in a given period of time. If the slew rate is 7 V/$\mu$sec, the analog circuit output will change seven volts in one $\mu$sec.

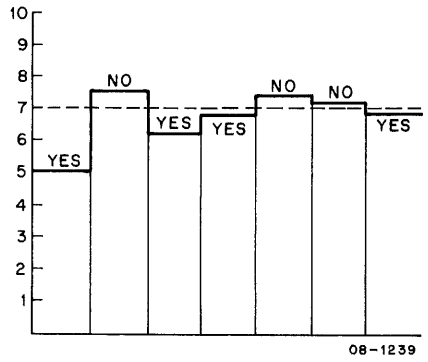
*Successive Approximation*
A method that is used to transform the analog signal to a digital number.




An analog signal is compared to a logic generated signal. The logic always supplies a half range signal initially. For example, the full scale input to an A/D converter system is 10 V and the input to the system is 7 V.

| Try* | New Logic Voltage | Is the Input Greater Than New Voltage | A/D Buffer Bits | Decision | A/D Register Value |
|---|---|---|---|---|---|
| 5 V | 5 V | Yes | 6 | Add +5 = +5 | 1000000 |
| 2.5 V | 5 + 2.5 V | No | 5 | Do nothing | 1000000 |
| 1.25 V | 5 + 1.25 V | Yes | 4 | Add 1.25 = 6.25 | 1010000 |
| .625 V | 6.25 + .625 V | Yes | 3 | Add .625 = 6.875 | 1011000 |
| .3125 V | 6.875 + .3125 V | No | 2 | Do nothing | 1011000 |
| .15625 V | 6.875 + .1562 V | No | 1 | Do nothing | 1011000 |
| .078125 V | 6.875 + .078125 V | Yes | 0 | Add .078175 | 1011001 |

*This is a 7-bit A/D
1011001 ≈ 7 V in 10 V full scale range.



*Throughput Speed*

The Nyquist sampling theorem states that a minimum of two samples per cycle are required to completely recover continuous signals in a noiseless environment. In typical instrumentation systems noise does exist and from 5–10 samples per cycle are required.

For applications with dc and very low frequency signals, sample rate is usually a sub-multiple of the powerline frequency to provide essentially infinite rejection of these frequencies.

The minimum sampling speed required is the number of samples per cycle multiplied by the highest frequency component of the data. For time multiplexed systems, the speed requirement of the A/D converter is dependent on system throughput speed. System conversion speed is determined from data bandwidth, the number of channels, and the sampling factor by:

System throughput = (N) (n) (B.W.) samples/second
n = number of channels

where N = number of samples/cycle (sampling factor)
B.W. = largest bandwidth of any channel

Example

Channel 1 bandwidth 100 Hz
Channel 2 bandwidth 200 Hz
Channel 3 bandwidth 250 Hz

throughput = $10 \times 3$ (250) = 7500 sample/second

N = 10
n = 3
BW = 250 Hz

The A/D throughput is comprised of the following:

Multiplexer settling time
Sample & Hold settling time
A/D conversion speed
A/D recovery time
Computer acquisition time (Software)

| LOCATION | CONTENTS | |
|---|---|---|
| 0 | 5077 | |
| 2 | 40 | |
| 4 | 12700 | |
| 6 | 4000 | |
| 10 | 5277 | |
| 12 | 30 | |
| 14 | 105777 | |
| 16 | 24 | |
| 20 | 100375 | |
| 22 | 5277 | |
| 24 | 16 | |
| 26 | 17720 | |
| 30 | 14 | |
| 32 | 20027 | |
| 34 | 4200 | |
| 36 | 1366 | |
| 40 | 0137 | |
| 42 | 0 | |
| 44 | 170400 | AD 52 |
| 46 | 170402 | AD BR |
| 50 | 0 | |

See pg # 3-3

# Reader's Comments

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