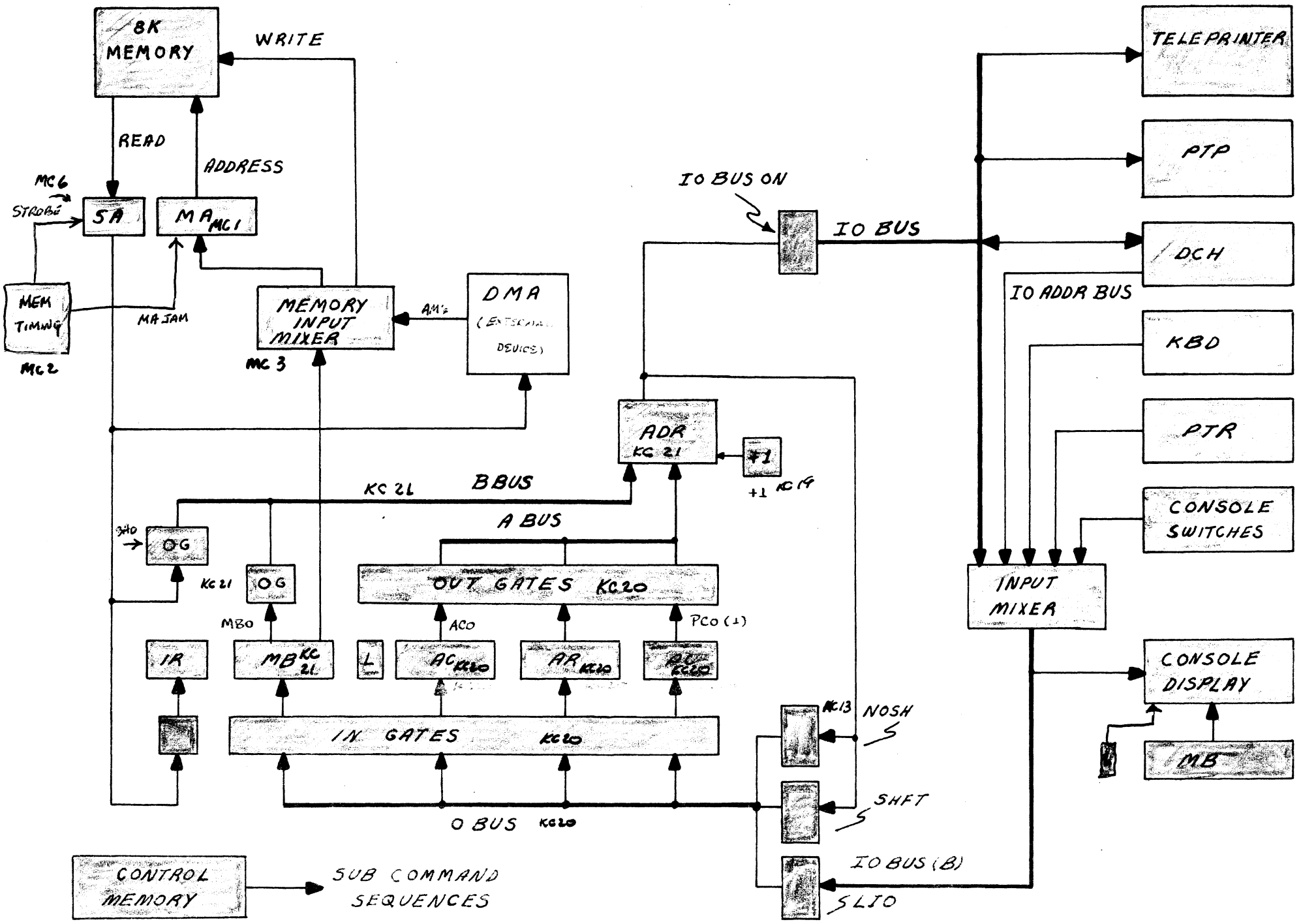
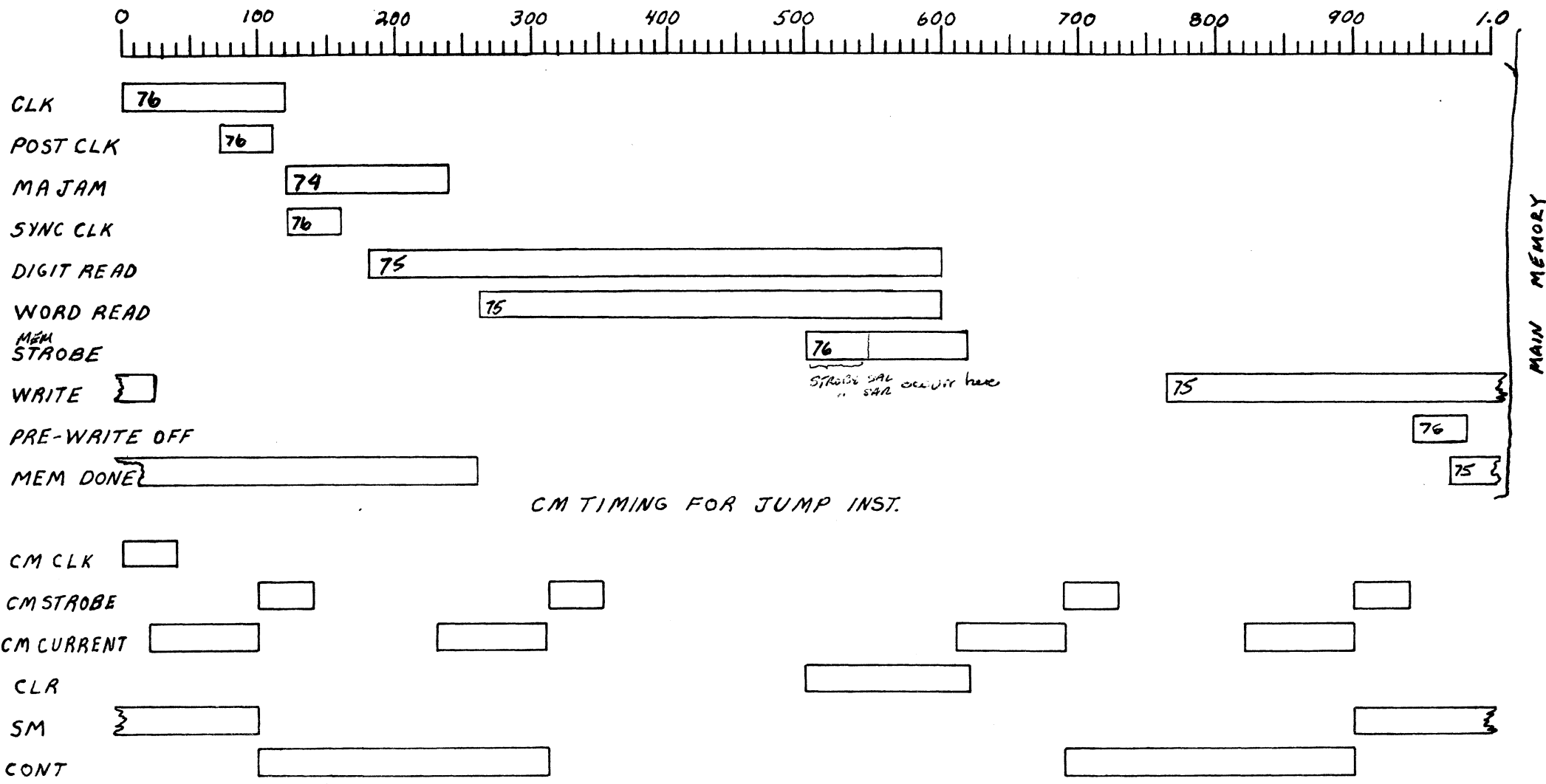
PDP-9 BASIC BLOCK



Programming running
DEC TAPE READING

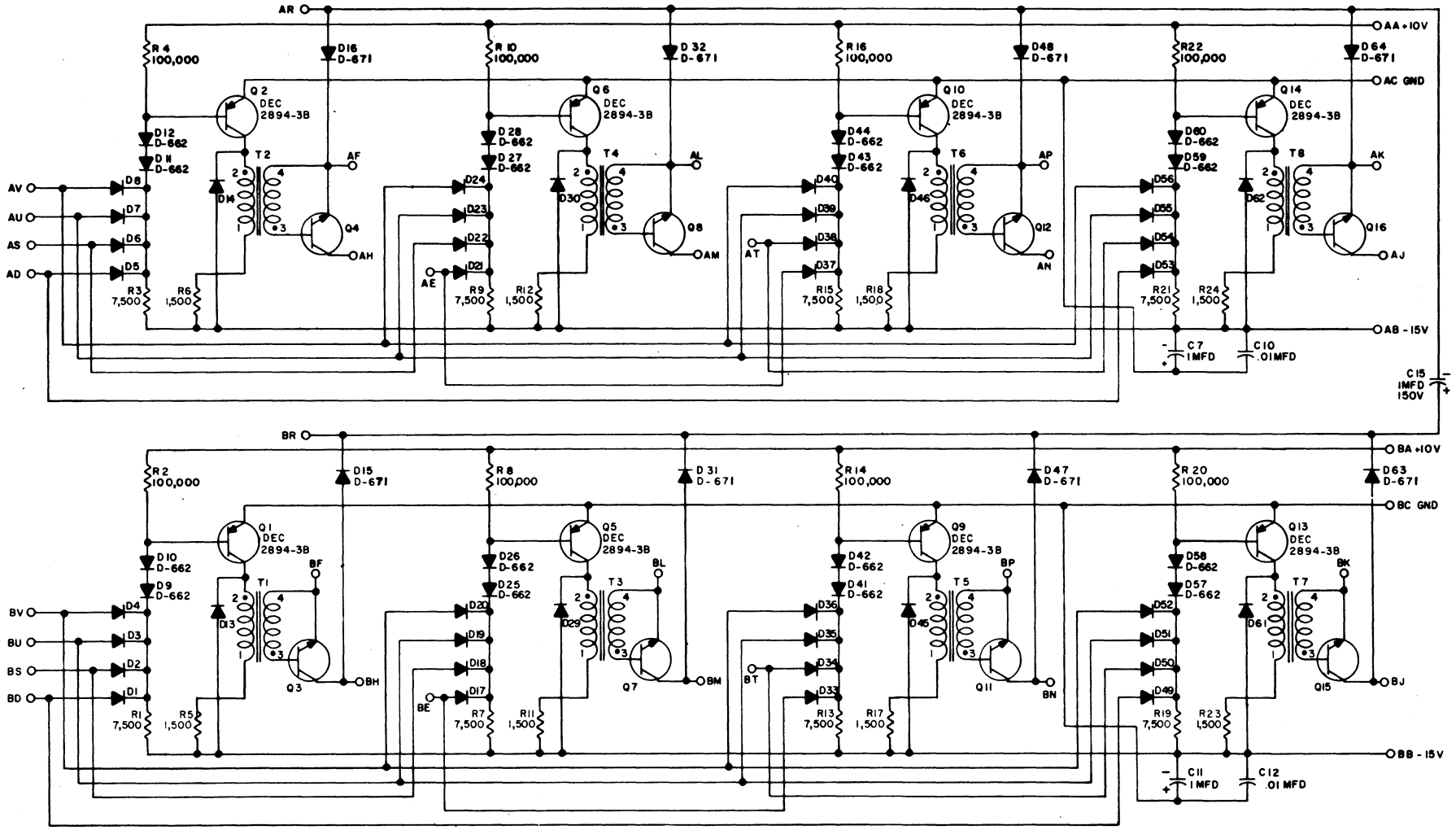
		CMA	MB	MA	PC	L	AC	AR	IR
START → 207	TAD 103	ASSUME	000207	XXXXX	00207	0	013204	XXXXXX	XXXXX
BK7 210	ISZ 703	21		207	210				
103	777 777	12						013204	00000
		CLR	340103						01111
30	777401	24							
31	000 ~~477~~ 500	30		103					
500	DATA	CLR	777777						
		67					013203		
		11	000030	@CLK		1			00000
		34		30				31	
		CLR	777401	@STROBE					
		14	000031	@CLK					
		37		31					
		CLR	000500						
		13						DATA	
		16							
		36		00500					
		CLR	DATA						
		17							
		10	0[illegible]210	@clock					

3 cycle DCH break (read)



CM TIMING FOR JUMP INST.

KIP, IO RESTART, RESTART NODE — 188 NS TO NEXT CM STROBE



UNLESS OTHERWISE INDICATED
TRANSFORMERS ARE T-2017
TRANSISTORS ARE DEC 3009A

RESISTORS ARE 1/4 W; 5 %
DIODES ARE D-664

REVISIONS			
SYM	CHG NO	DATE	BY
	5944	8	

DRN		DATE
CHK'D		DATE 11/66
ENG		DATE
PROD		DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA
DEC3009A	2N3009		
DEC2894-3B	NONE		
D662	IN645		
D664	IN3606		
D671	IN3653		

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE CONTROL MEMORY DRIVER G210

SIZE	CODE	NUMBER	REV
C	CS	G210-0-1	B

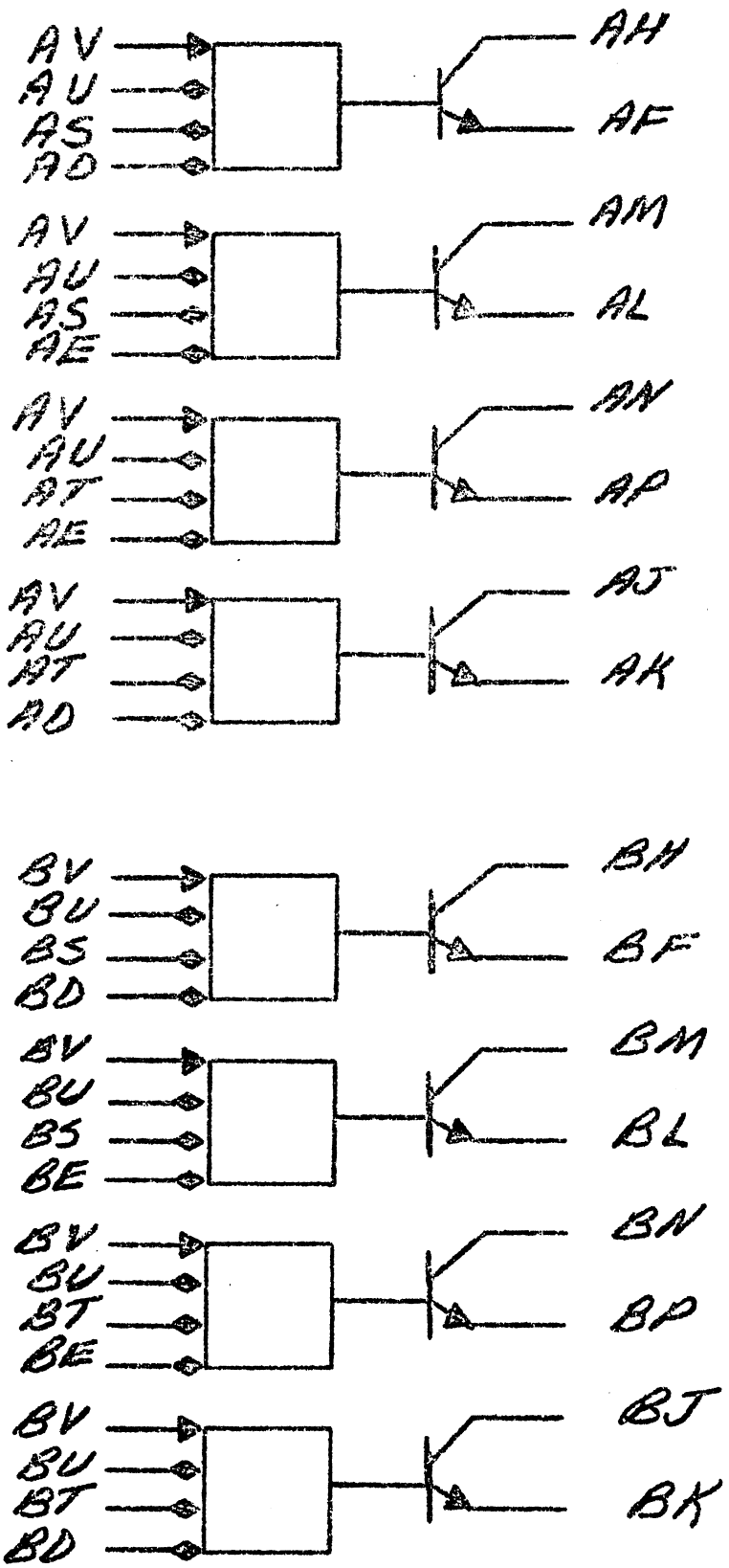
PRINTED CIRCUIT REV A

REV	NUMBER	CODE	SIZE
B	G210-0-1	CS	C

DEC FORM NO
DRC 107

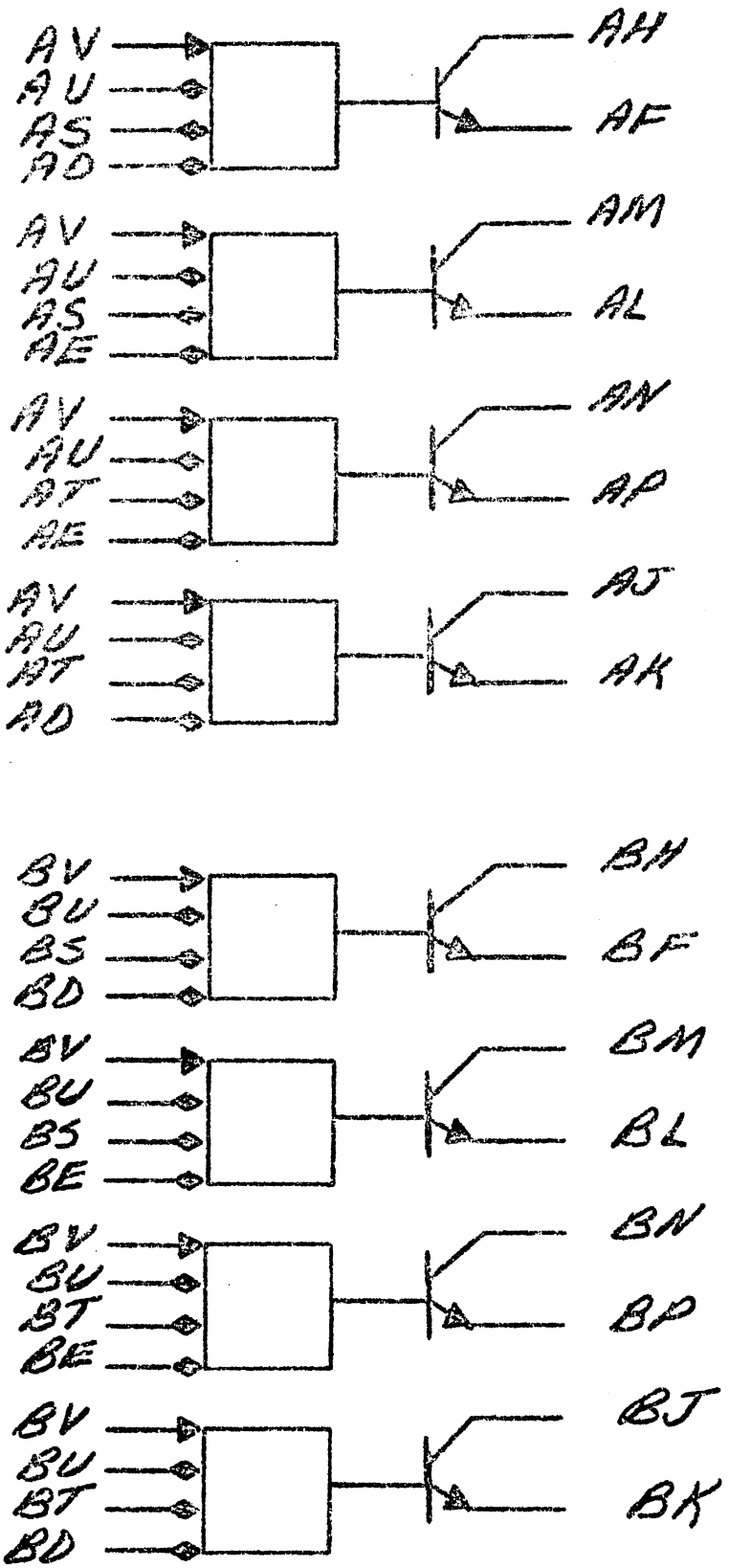
SIMPLIFIED

G210 OR G219



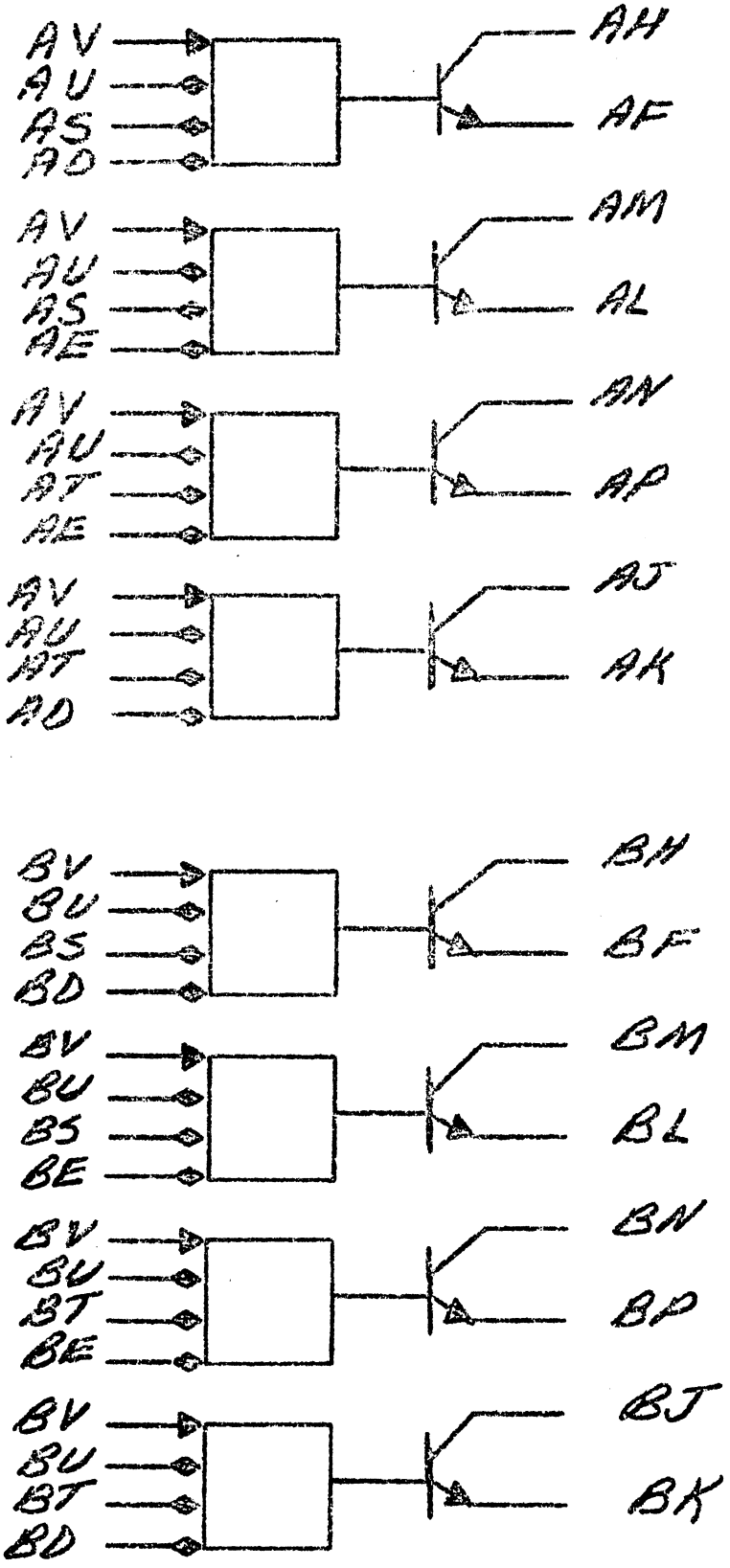
SIMPLIFIED

G210 OR G219



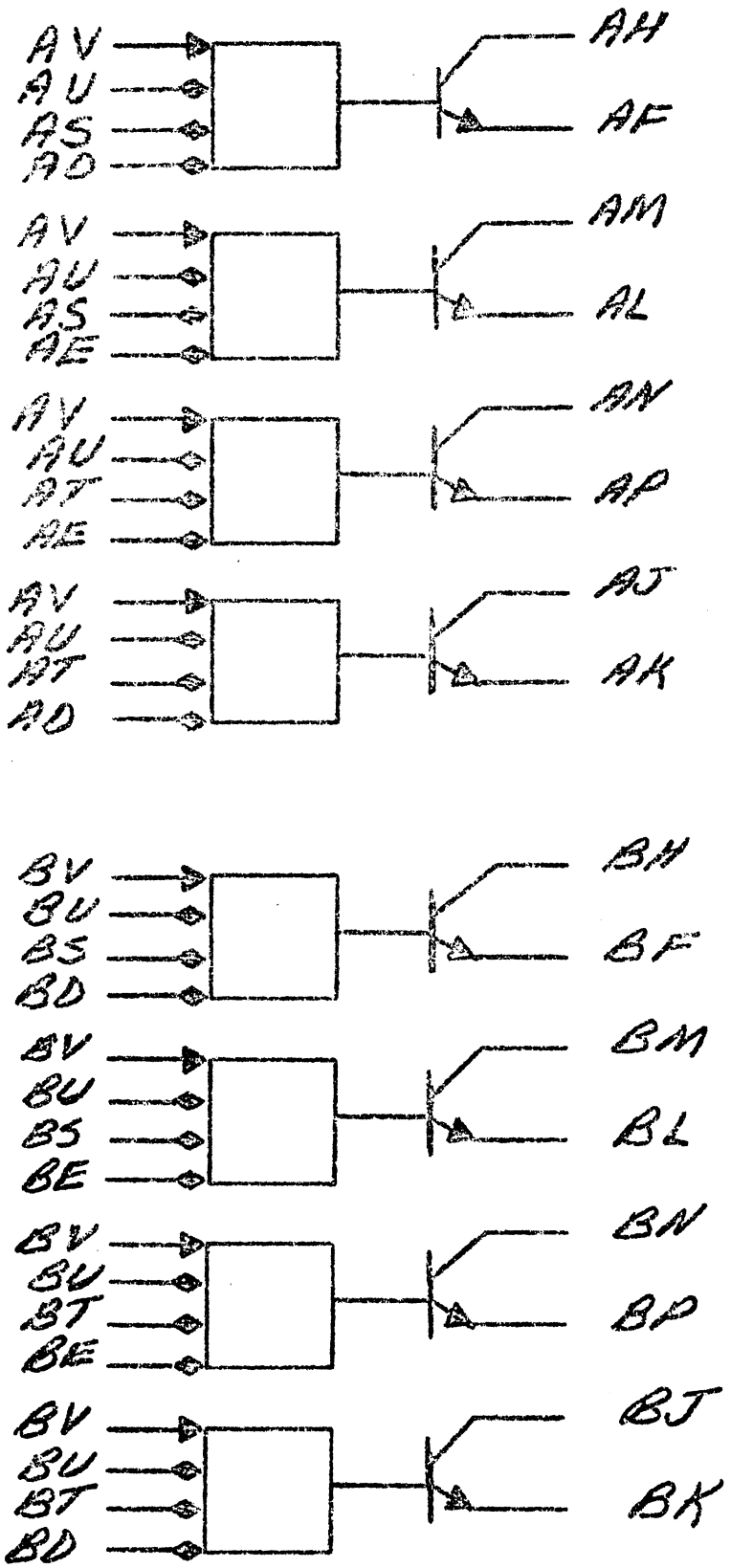
SIMPLIFIED

G210 OR G219



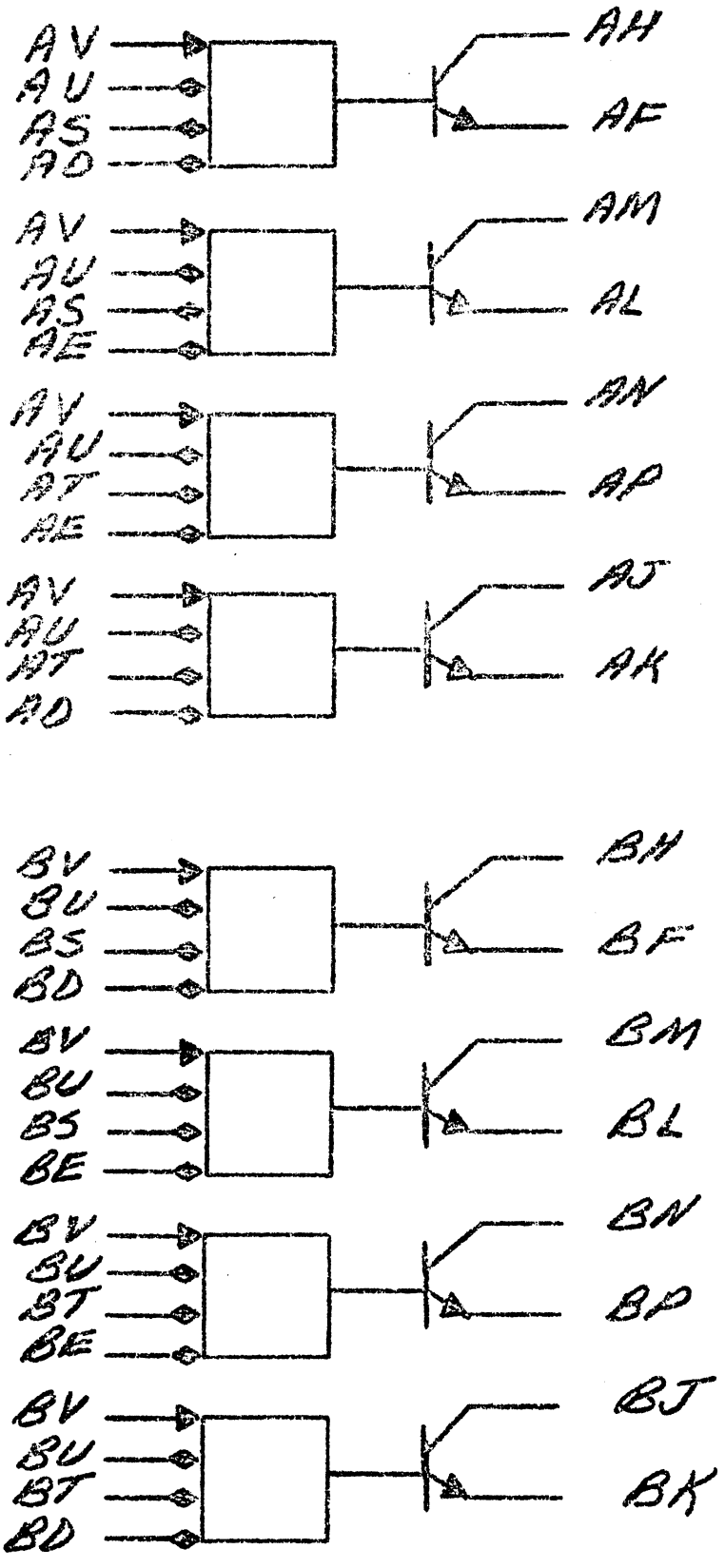
SIMPLIFIED

G210 OR G219



SIMPLIFIED

G210 OR G219

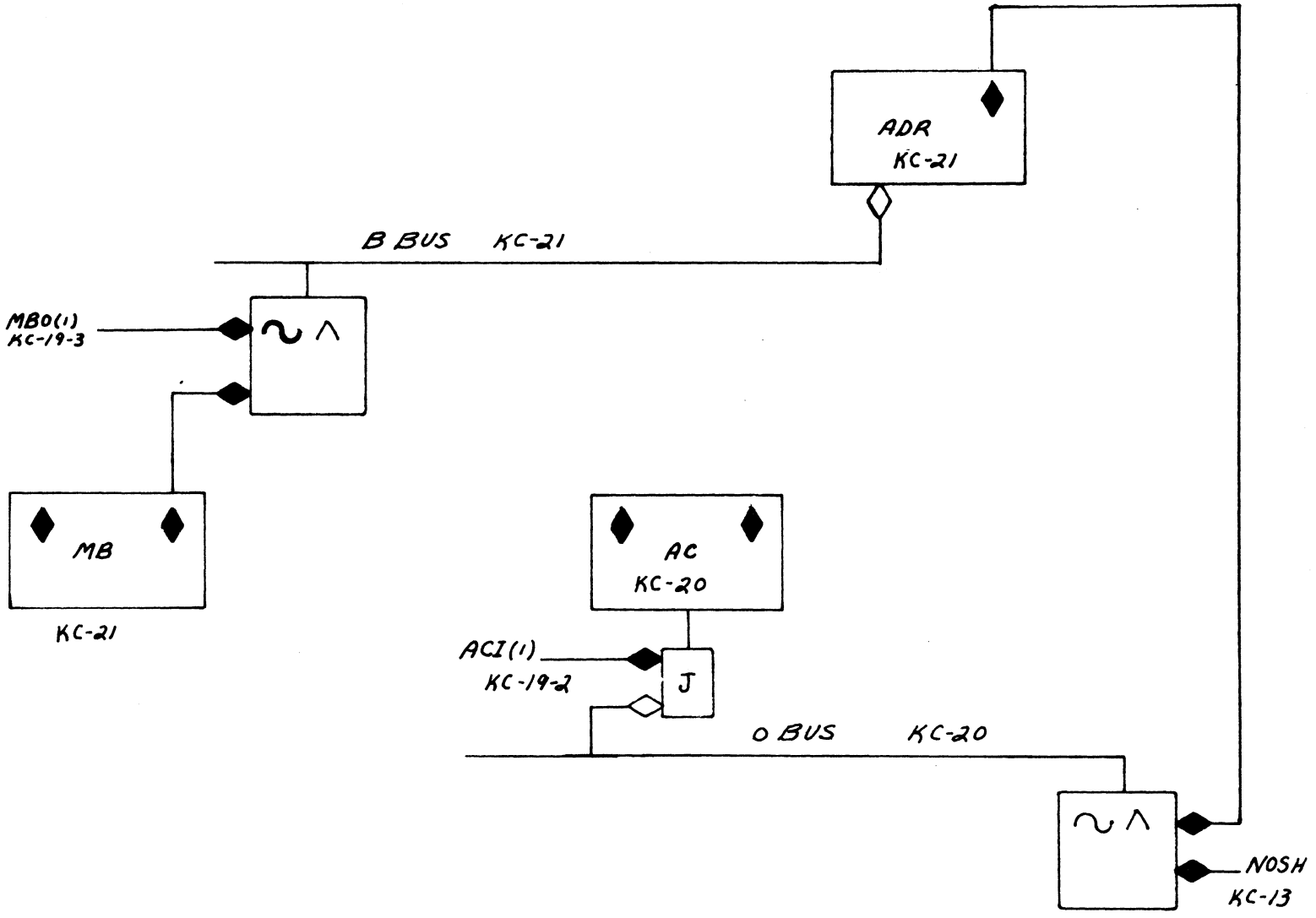


PDP-9 Memory Reference Instruction Demonstration Program

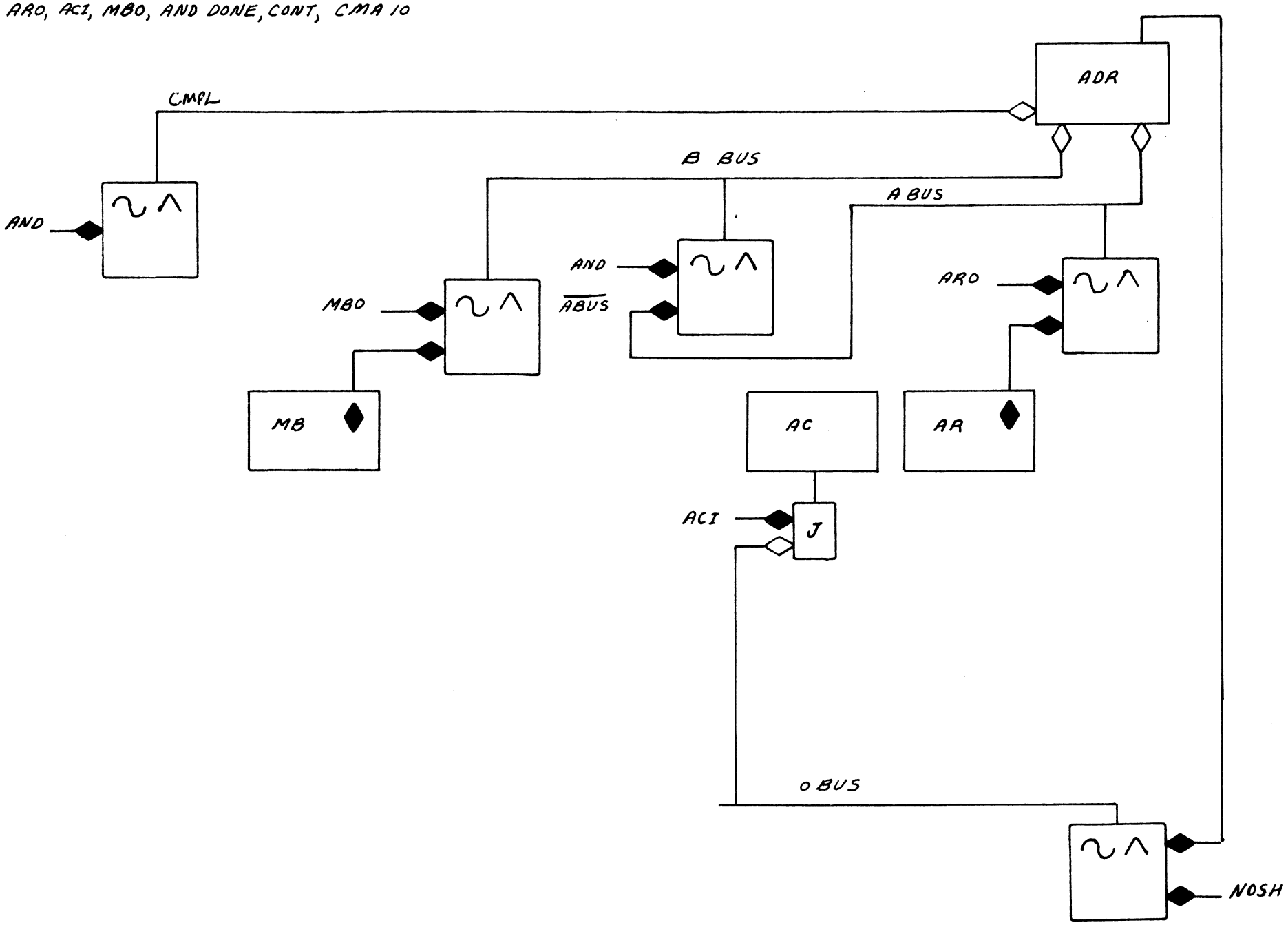
Objective: I/O result / then Stop

	MNEMONIC	ENCODED
→	*1000/ LAC 500	200500
	1001/ AND 501	500501
	1002/ SAD 502	540502
	1003/ DZM 1011	141011
	1004/ ADD 503	300503
	1005/ JMS 510	100510
	1006/ ISZ 505	440505
	1007/ JMP 1001	601001
	1010/ TAD I 13	360013
	13/ 000477	000477
	20/ 000000	000000
	21/ HLT	740040
	500/ 465432	465432
	501/ 777000	777000
	502/ 123456	123456
	503/ 677777	677776
	504/ 413000	413000
	505/ 000000	000000
	510/ 000000	000000
	511/ XCT 1003	401003
	512/ XOR 504	240504
	513/ DAC 505	040505
	514/ JMP I 510	620510

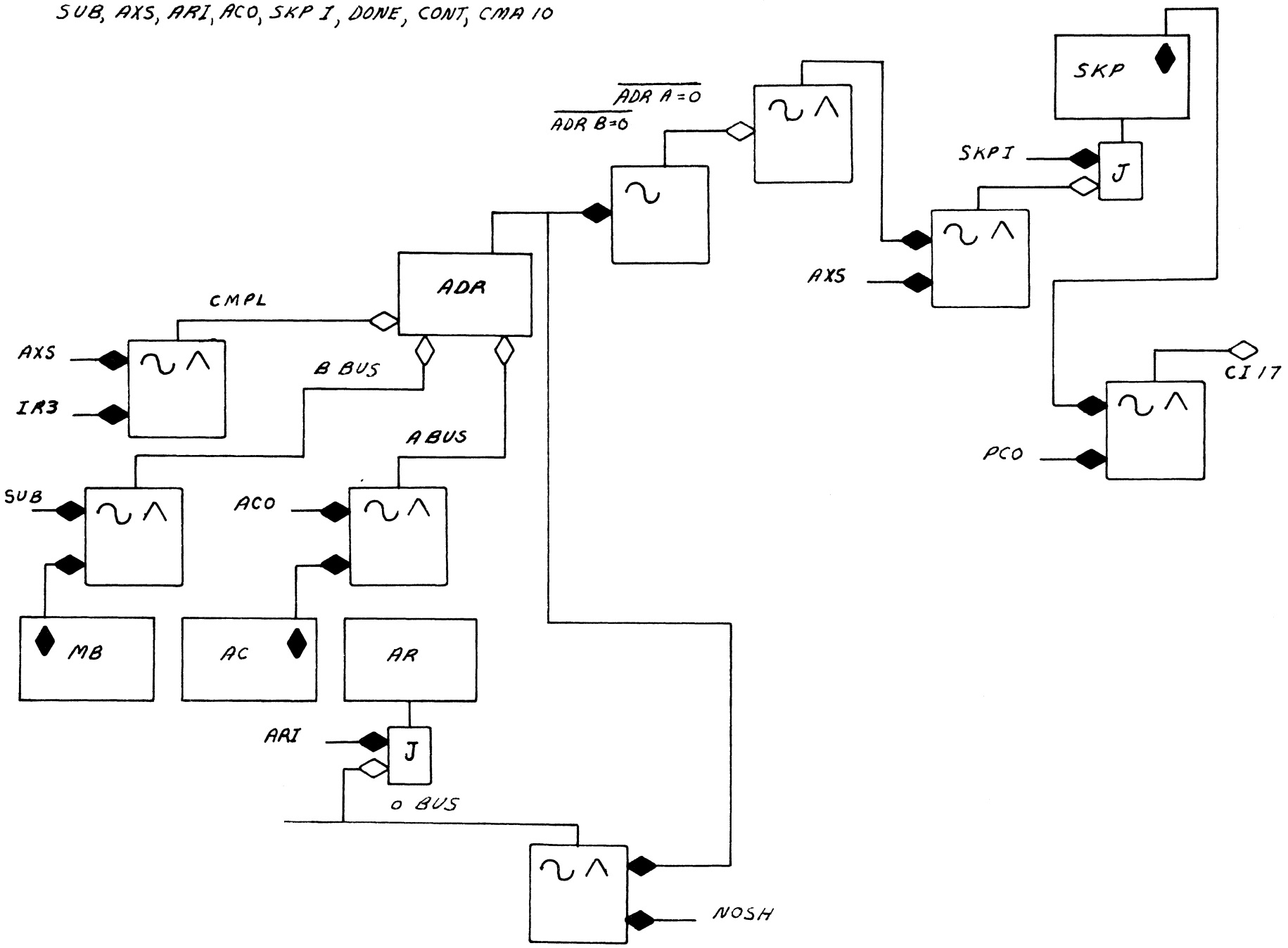
LAC INSTRUCTION LOGIC FOR CML 64:
MBO, ACI, DONE, CONT, CMA 10



AND INSTRUCTION FOR CML 72
ARO, ACI, MBO, AND DONE, CONT, CMA 10

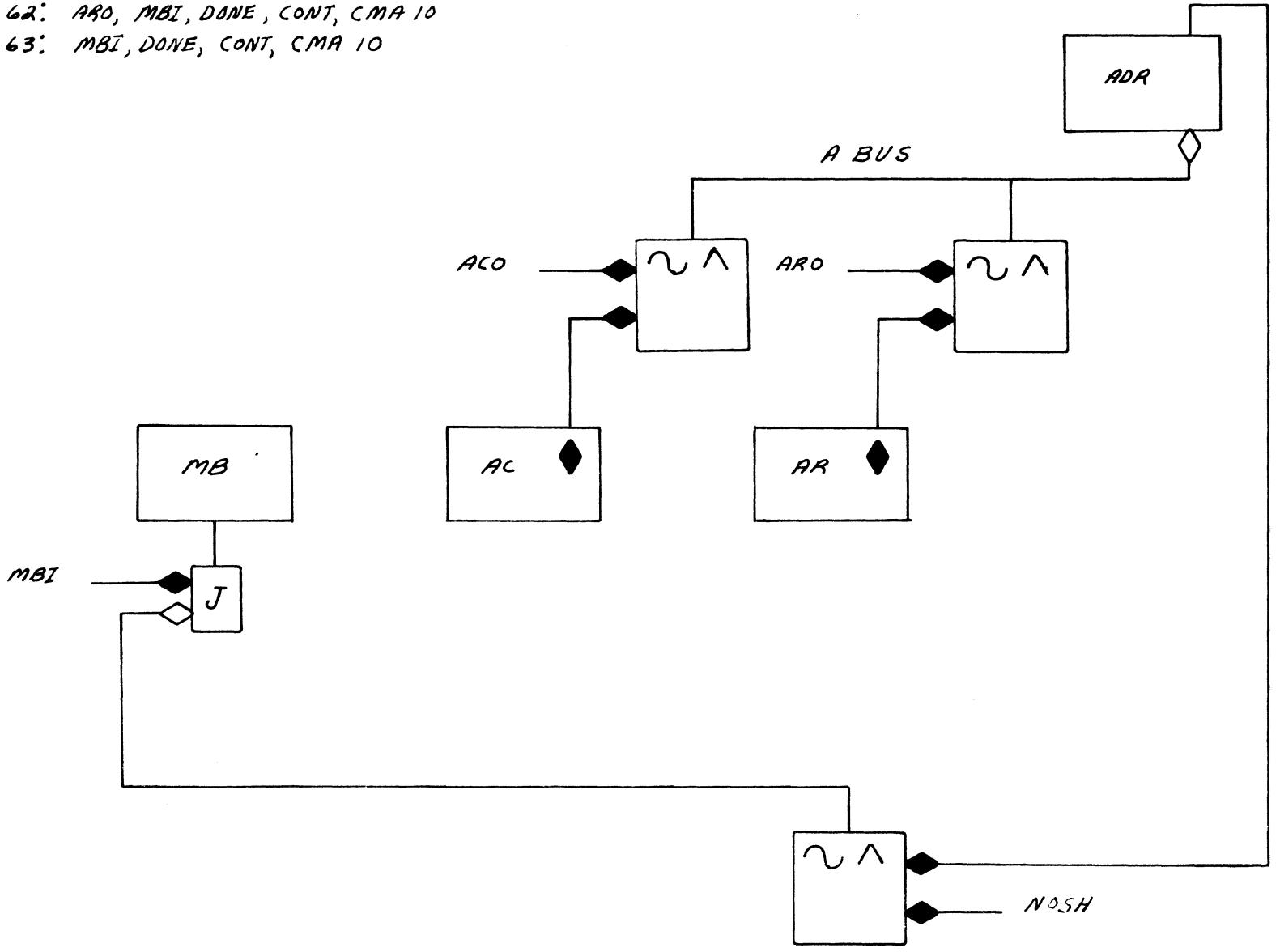


SAD INSTRUCTION LOGIC FOR CML 73
SUB, AXS, ARI, ACO, SKP I, DONE, CONT, CMA 10



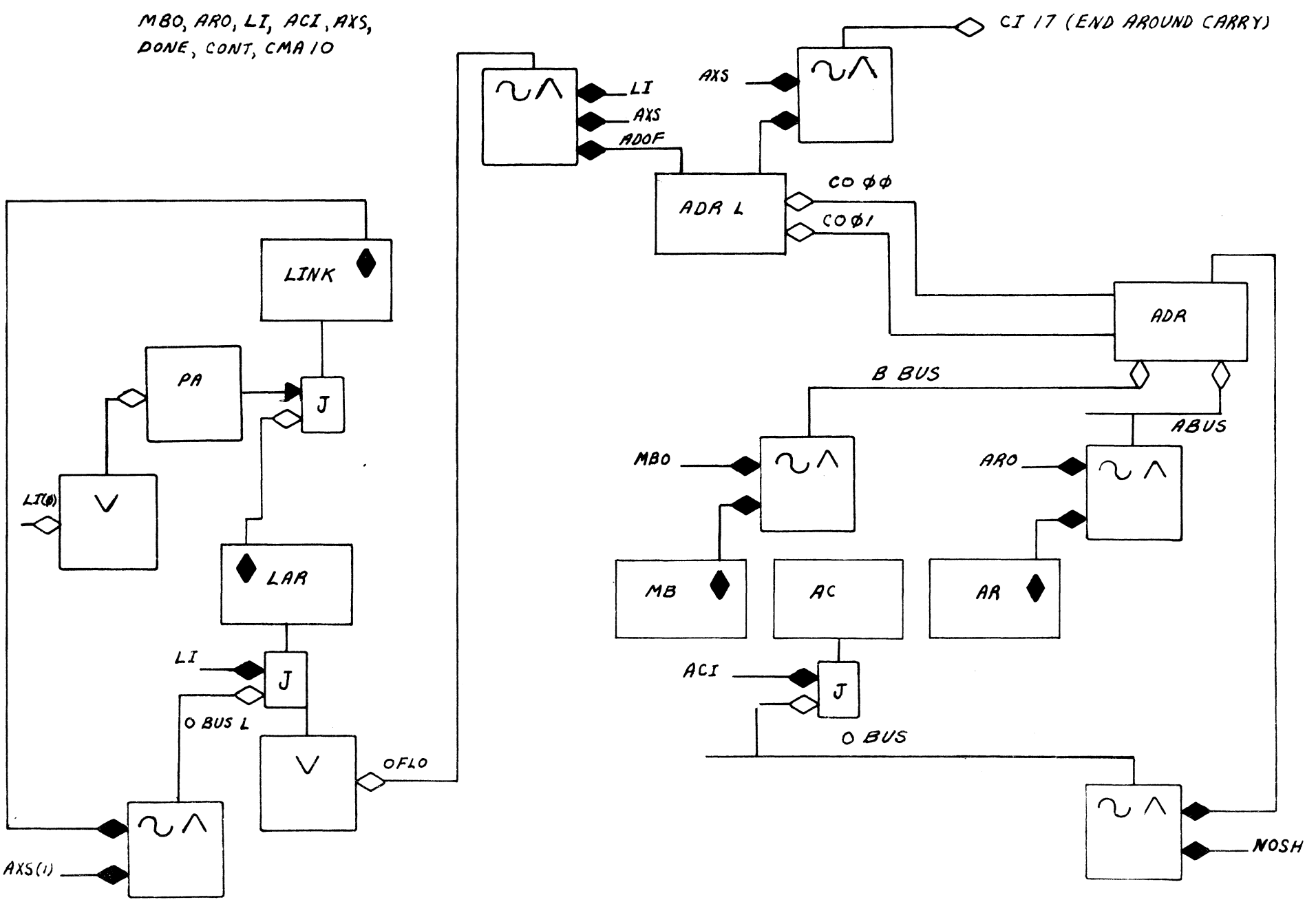
IAO INSTRUCTION LOGIC FOR:

DAC	CML 61:	ACO, MBI, DONE, CONT, CMA 10
CAL	CML 60:	ARO, MBI, DONE, CONT, CMA 10
JMS	CML 62:	ARO, MBI, DONE, CONT, CMA 10
DZM	CML 63:	MBI, DONE, CONT, CMA 10

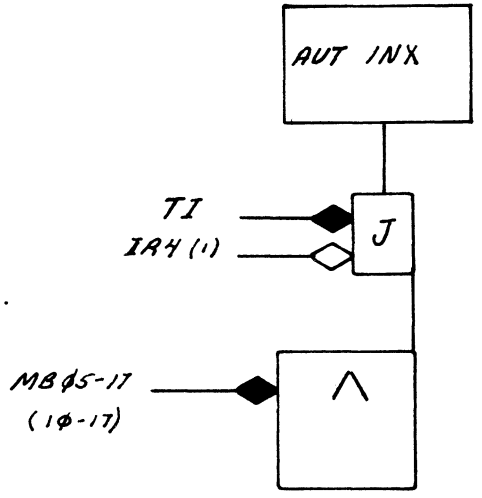


ADD INSTRUCTION LOGIC FOR CML 66

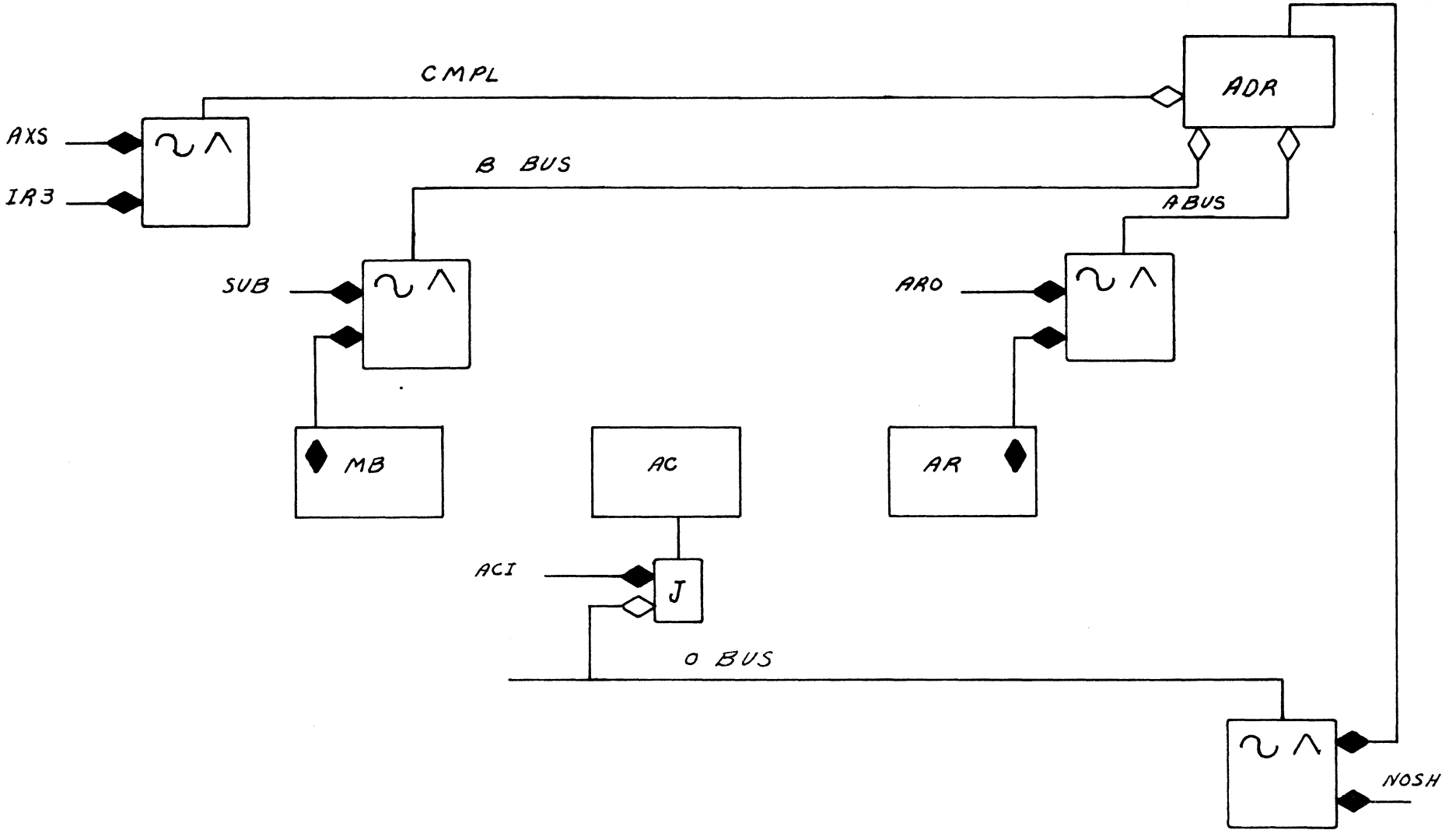
MBO, ARO, LI, ACI, AXS,
DONE, CONT, CMA IO



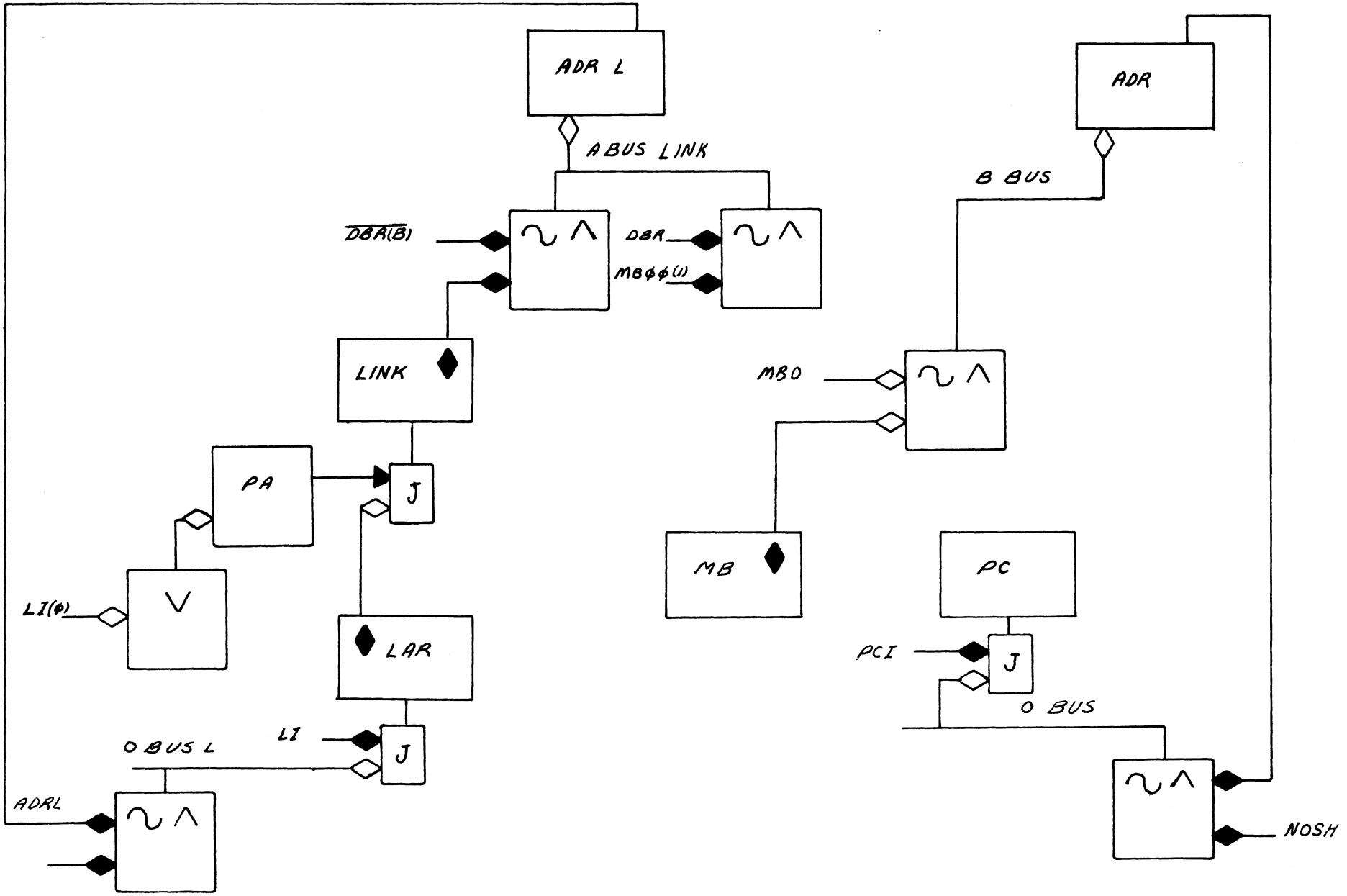
XCT INSTRUCTION LOGIC FOR CML 70
TI, SM, CMA 33 0 → AUTO INDEX



XOR INSTRUCTION LOGIC FOR CML 65
SUB, AXS, ARO, ACI, DONE, CONT, CMA 10

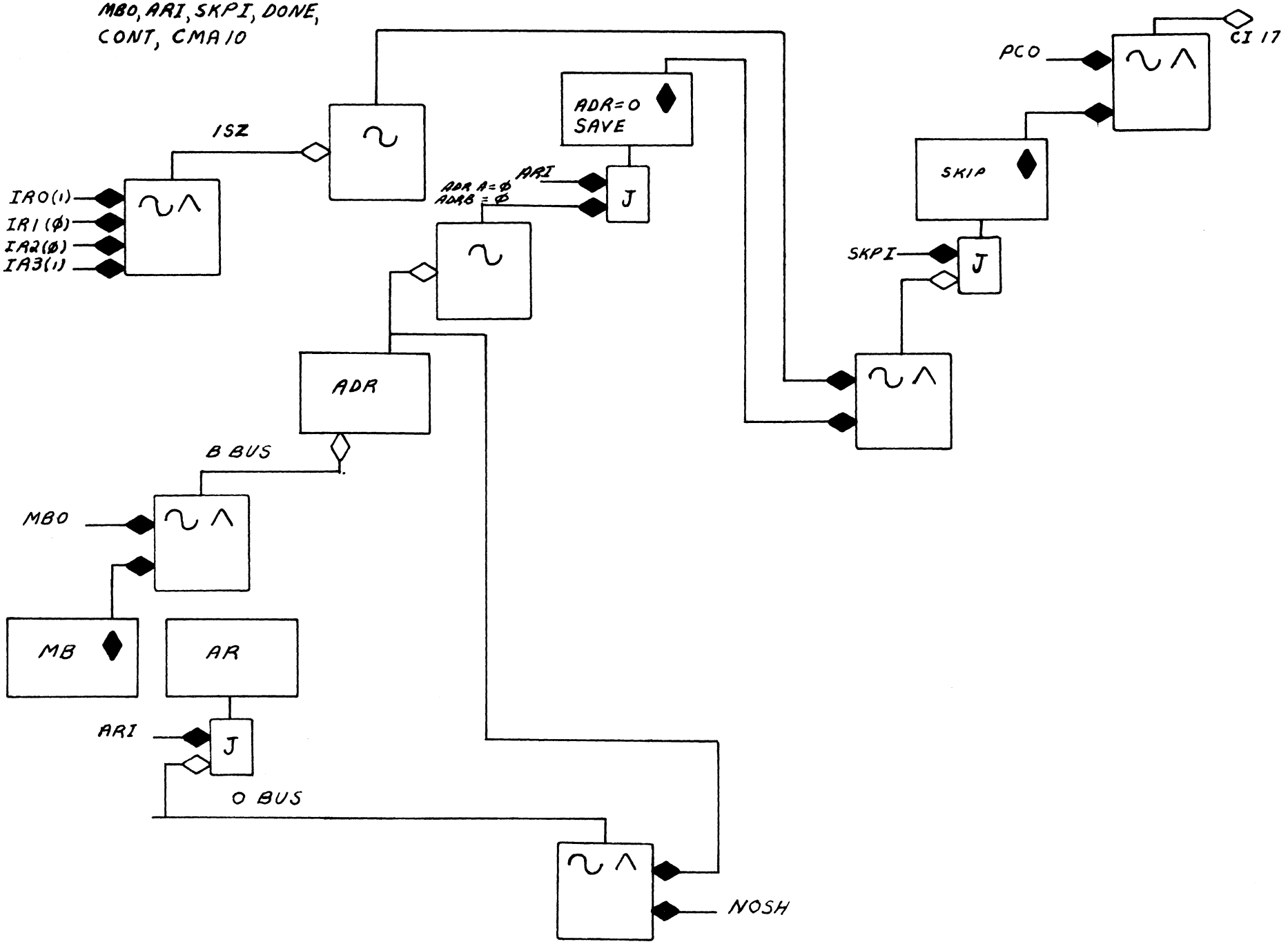


JMP INSTRUCTION LOGIC FOR CML 74
MBO, PCI, LI, DONE, CONT, CMA 10

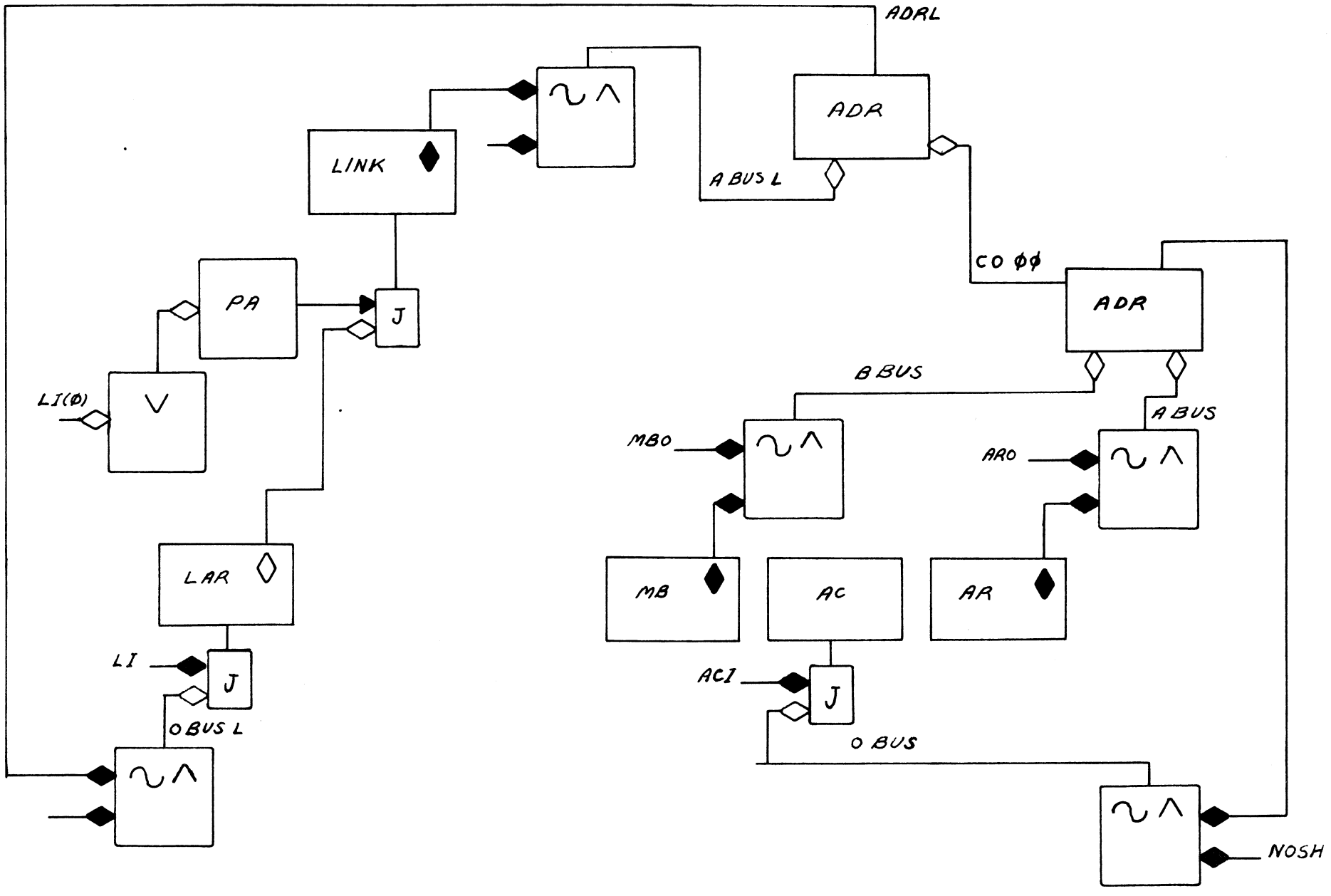


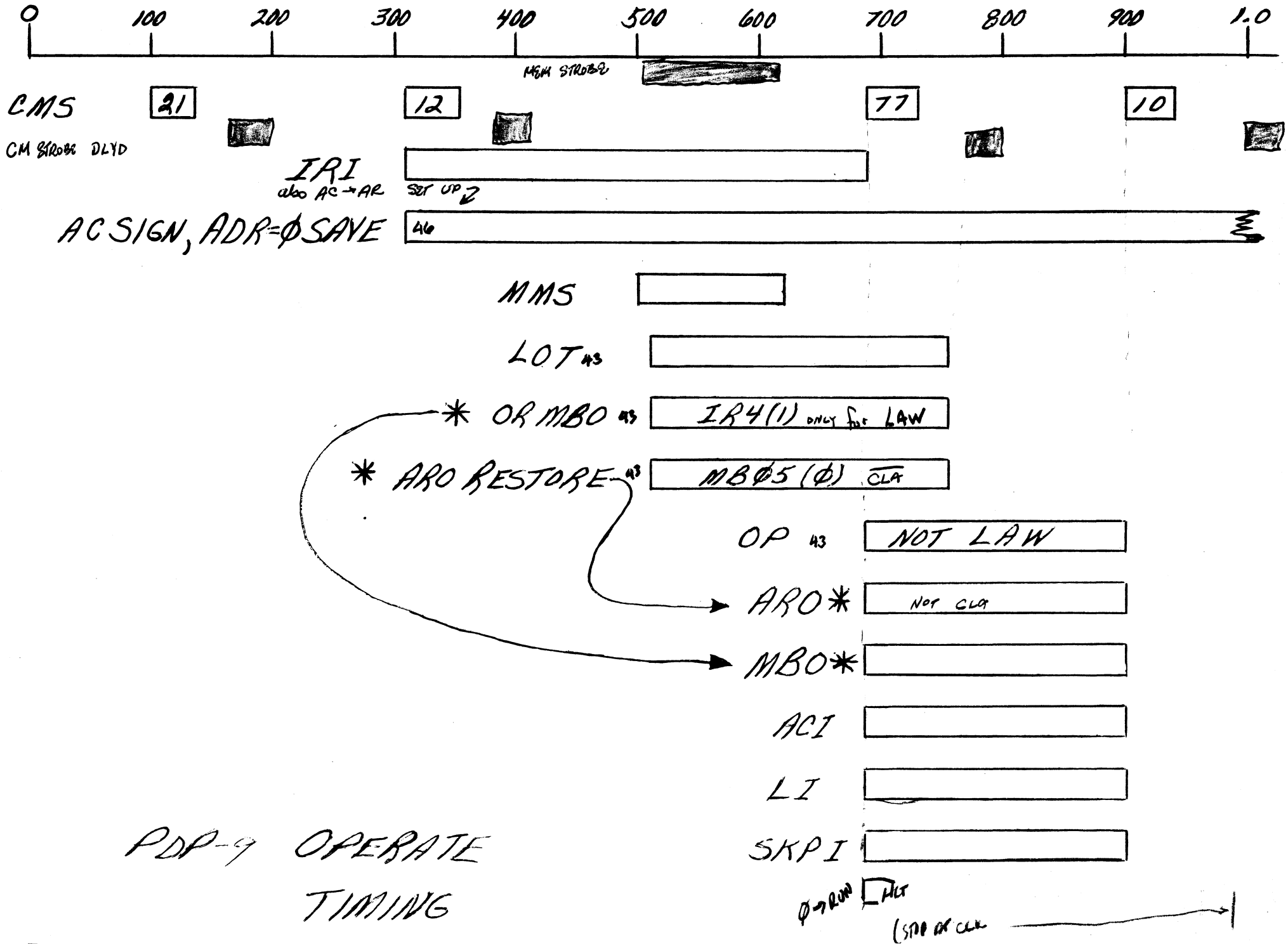
ISZ INSTRUCTION LOGIC FOR CML 71

MB0, ARI, SKPI, DONE,
CONT, CMA 10

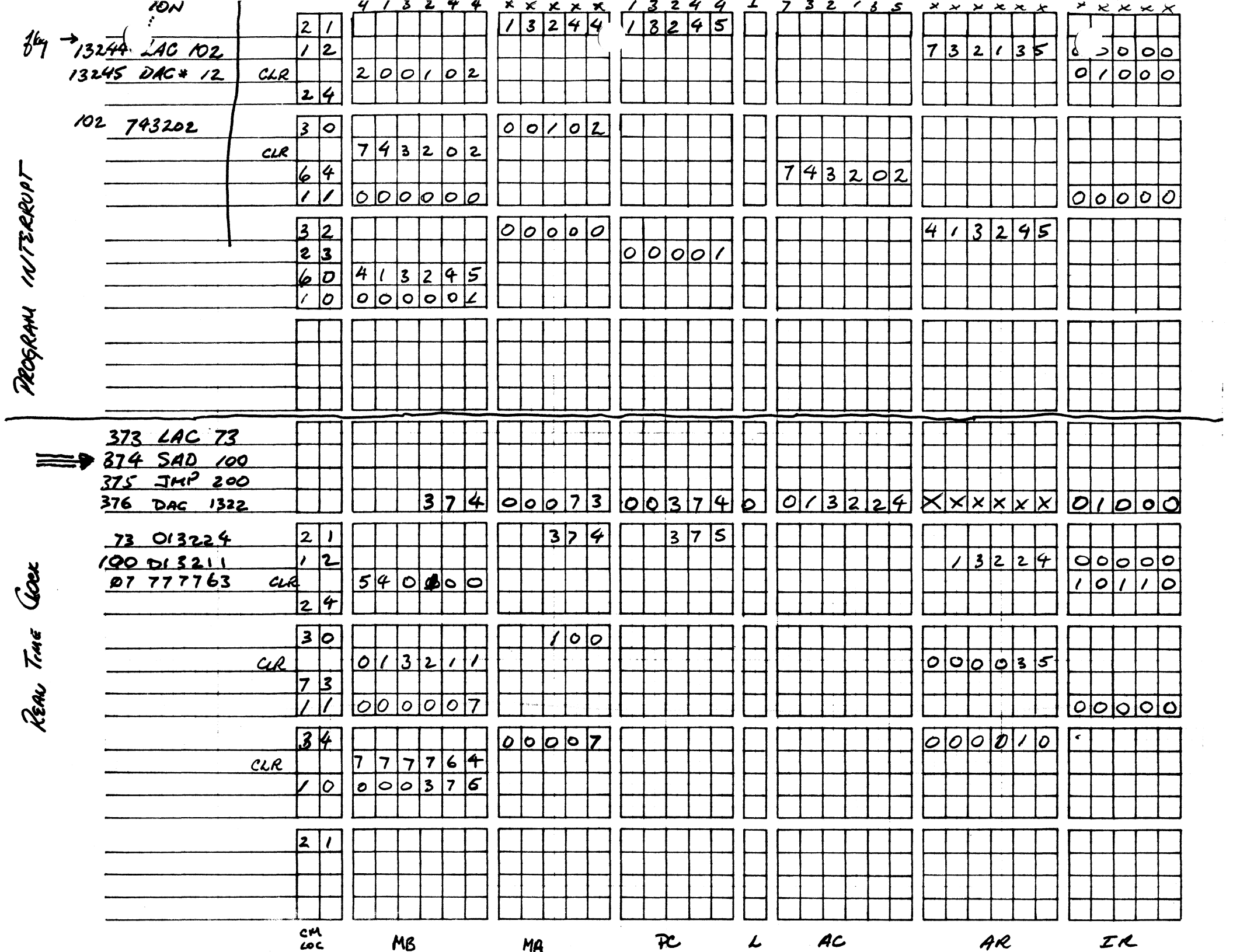


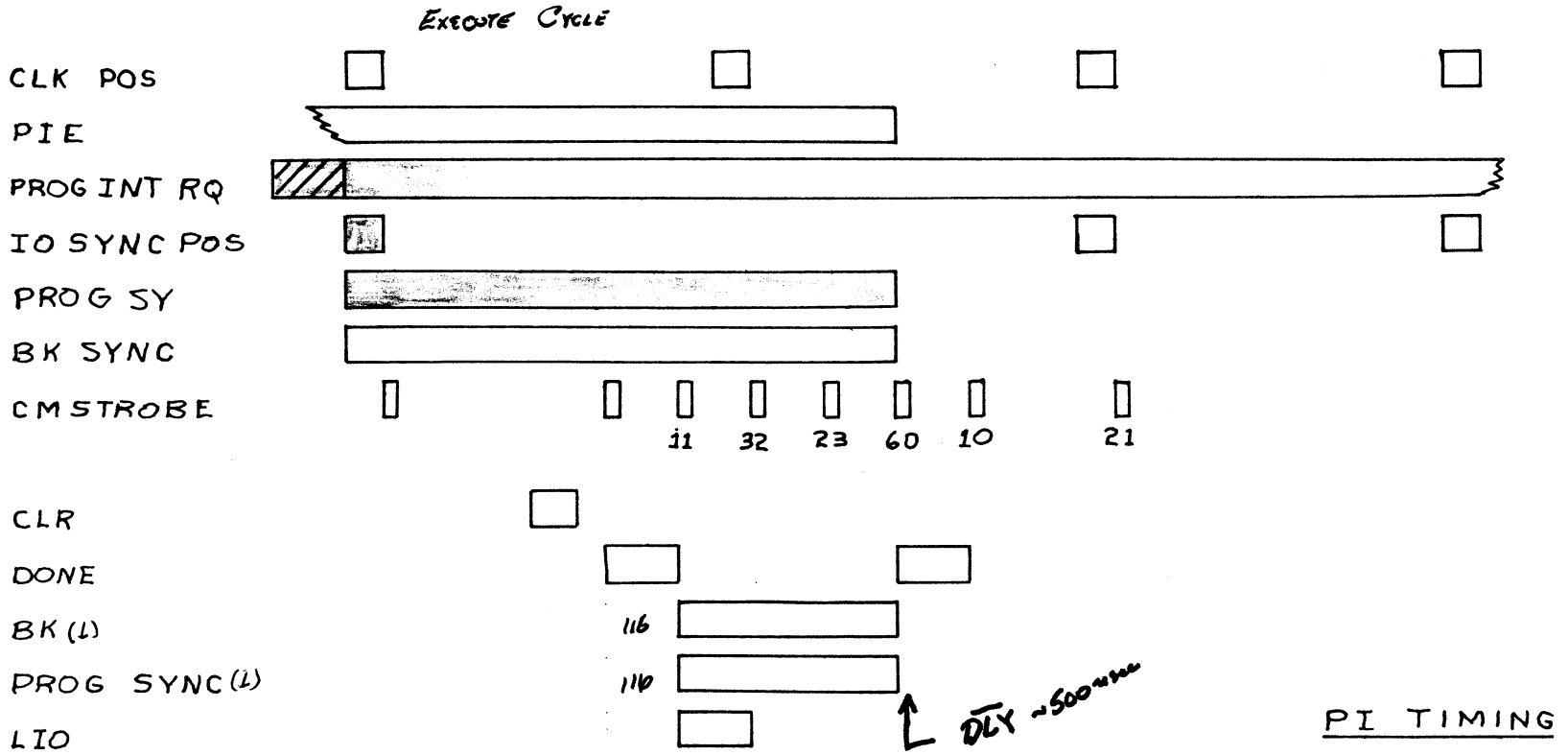
TAD INSTRUCTION LOGIC FOR CML 67
MBO, ARO, ACI, LI, DONE, CONT, CMA IO



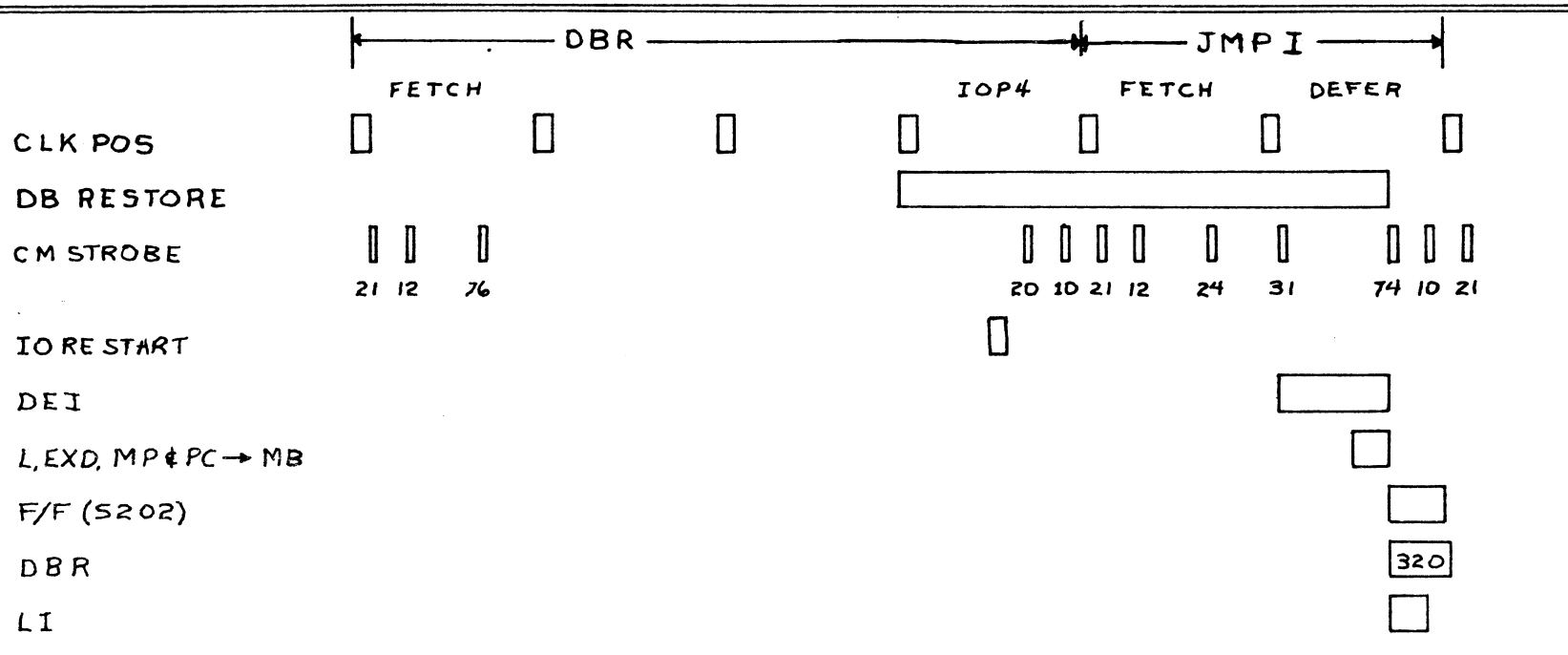


PDP-4 OPERATE TIMING

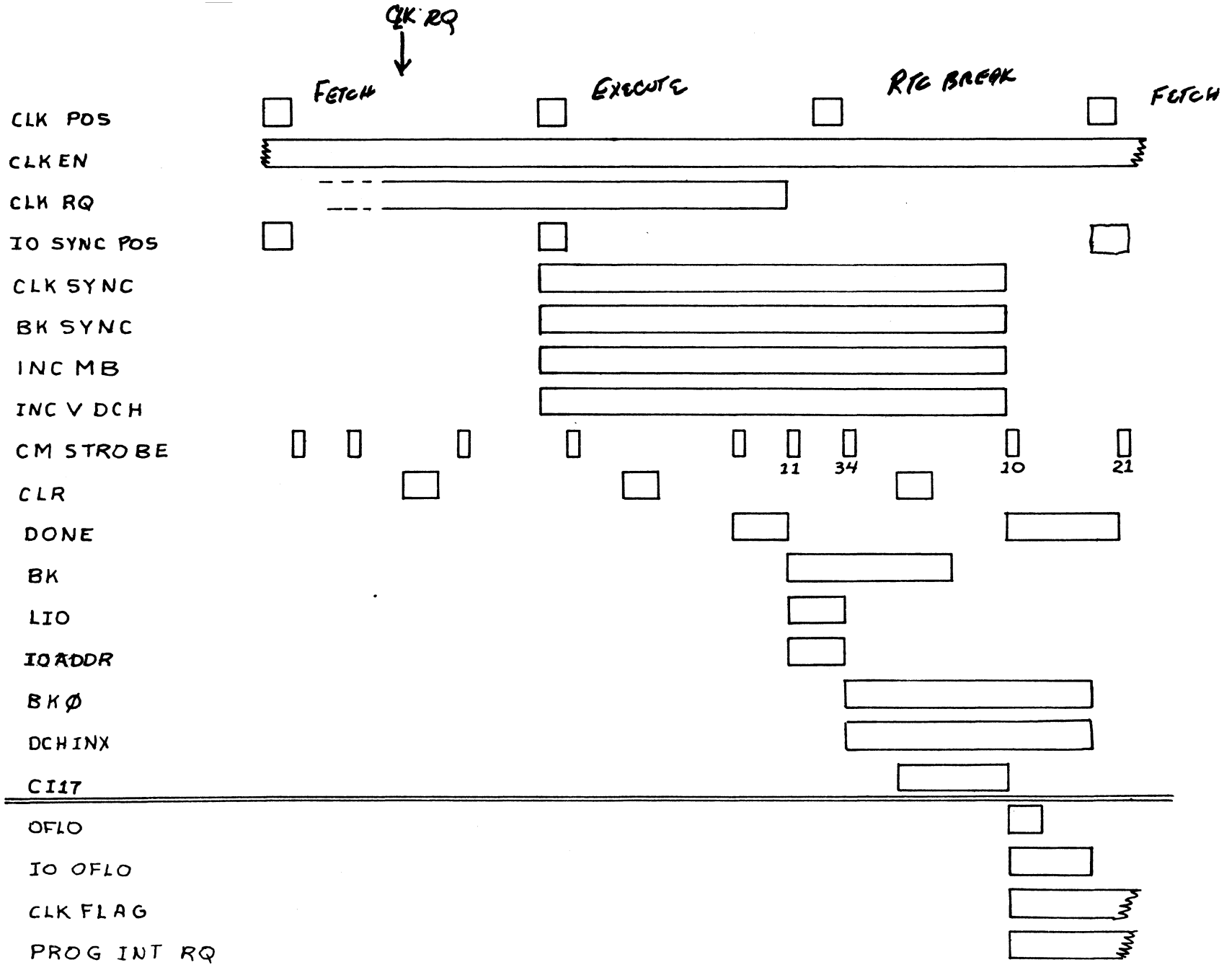

ION
PROGRAM INTERRUPT
REAL TIME CLOCK
13244 LAC 102
13245 DAC* 12
102 743202
373 LAC 73
374 SAD 100
375 JMP 200
376 DAC 1322
73 013224
100 013211
CLR
CM LOC
MB
MA
PC
L
AC
AR
IR



PI TIMING



DBR TIMING


CLK RQ
FETCH
EXECUTE
RTC BREAK
FETCH
CLK POS
CLK EN
CLK RQ
IO SYNC POS
CLK SYNC
BK SYNC
INC MB
INC V DCH
CM STROBE
11
34
10
21
CLR
DONE
BK
LIO
IOADDR
BKØ
DCH INX
CI17
OFLO
IO OFLO
CLK FLAG
PROG INT RQ

RTC TIMING

Starting at B.O.T. (In Reverse End Zone)
Tape Traveling in Forward Direction

Initial Conditions	W 1	W 2	W 3	W 4	W 5	W 6	W 7	W 8	W 9	
	0	0	0	0	0	0	0	0	0	ST IDLE (1)
55	0	0	0	0	0	0	0	0	1	Assume up to speed
	0	0	0	0	0	0	0	1	0	Mark Track is now
Rev. End	0	0	0	0	0	0	1	0	1	entering window
Mark	0	0	0	0	0	1	0	1	1	
	0	0	0	0	1	0	1	1	0	
	0	0	0	1	0	1	1	0	1	
55	0	0	1	0	1	1	0	1	1	
	0	1	0	1	1	0	1	1	0	
Rev. End	1	0	1	1	0	1	1	0	1	
Mark	1	1	1	0	1	1	0	1	1	
	1	1	0	1	1	0	1	1	0	
	1	0	1	1	0	1	1	0	1	
25	1	1	1	0	1	1	0	1	0	Counter Advances at TP Ø
	1	1	0	1	1	0	1	0	1	
	1	0	1	1	0	1	0	1	0	
Interblock	1	1	1	0	1	0	1	0	1	= C-Sync
Sync	1	1	0	1	0	1	0	1	0	100
Mark	1	0	1	0	1	0	1	0	1	101 = C-Sync
										100
25	1	1	0	1	0	1	0	1	0	
	1	0	1	0	1	0	1	0	1	101 = C-Sync
	1	1	0	1	0	1	0	1	0	100
Interblock	1	0	1	0	1	0	1	0	1	101 = C-Sync
Sync	1	1	0	1	0	1	0	1	0	100
Mark	1	0	1	0	1	0	1	0	1	101 = C-Sync
										100
	$198_{(10)}$ More Interblock Marks To Go Assume Block Mark Next									

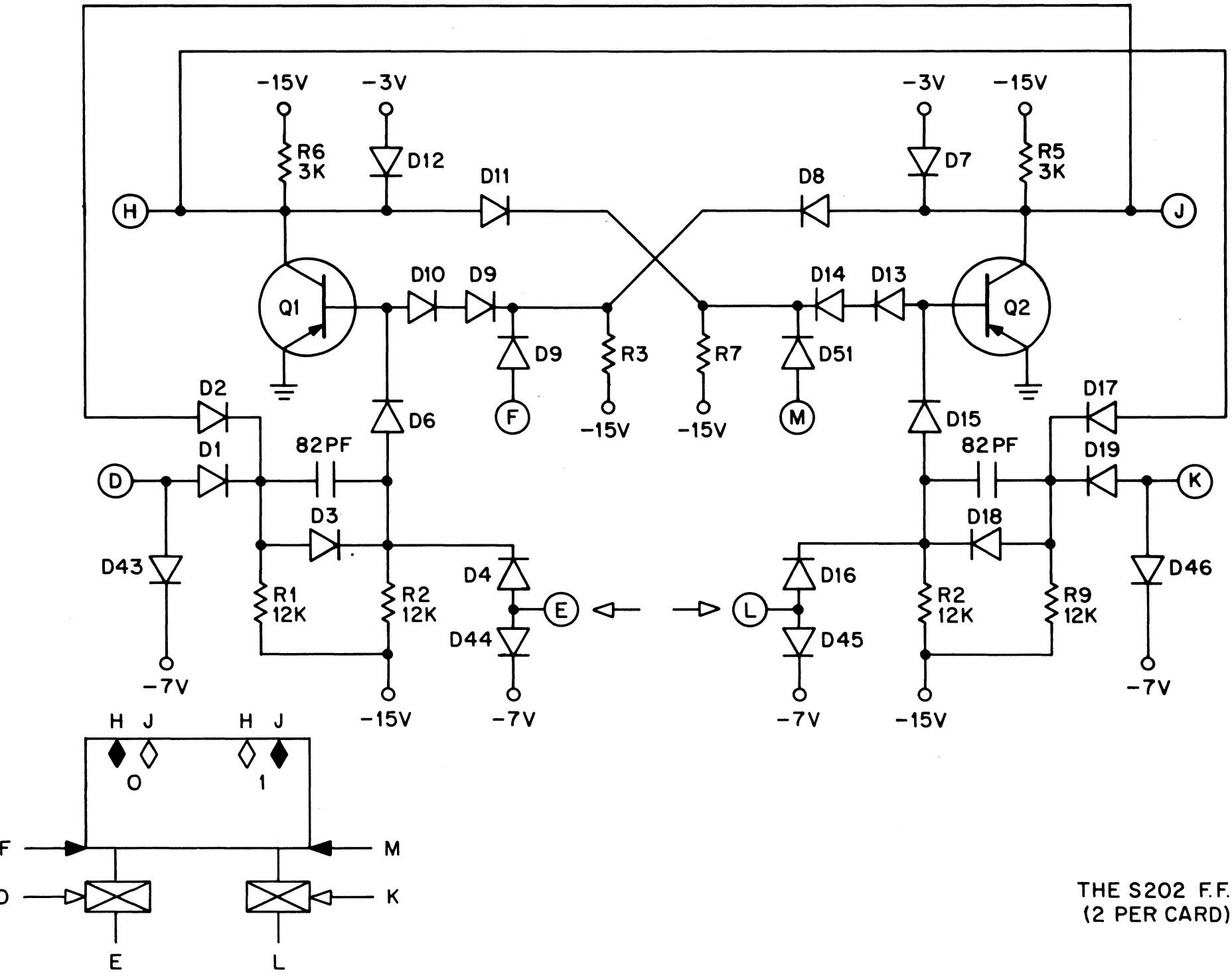
	W 1	W 2	W 3	W 4	W 5	W 6	W 7	W 8	W 9		
26 Forward Block Mark	1	1	0	1	0	1	0	1	0		100
	1	0	1	0	1	0	1	0	1	= C-Sync	101
	1	1	0	1	0	1	0	1	0		100
	1	0	1	0	1	0	1	0	1	= C-Sync (COUNTER NOW IN SYNC)	101
	1	1	0	1	0	1	0	1	1		100
	1	0	1	0	1	0	1	1	0	= Mk Blk Mk Reset ST IDLE Set ST Blk Mk	101
32 Reverse Guard Mark	1	1	0	1	0	1	1	0	0		000
	1	0	1	0	1	1	0	0	1		001
	1	1	0	1	1	0	0	1	1		010
	1	0	1	1	0	0	1	1	0		011
	1	1	1	0	0	1	1	0	1		100
	1	1	0	0	1	1	0	1	0		101
10 Lock Mark	1	0	0	1	1	0	1	0	0		000
	1	0	1	1	0	1	0	0	0		001
	1	1	1	0	1	0	0	0	1		010
	1	1	0	1	0	0	0	1	0		011
	1	0	1	0	0	0	1	0	0		100
	1	1	0	0	0	1	0	0	0	= Mk Blk Start Reset ST Blk Mk Set ST Rev CK	101
10 Reverse PCC Mark	1	0	0	0	1	0	0	0	0		0 0
	1	0	0	1	0	0	0	0	0		001
	1	0	1	0	0	0	0	0	1		010
	1	1	0	0	0	0	0	1	0		011
	1	0	0	0	0	0	1	0	0		100
	1	0	0	0	0	1	0	0	0	= Mk Blk Start Reset ST Rev Ck Set Data	101
											000

	W 1	W 2	W 3	W 4	W 5	W 6	W 7	W 8	W 9		
1Ø Reverse Final Mark	1	0	0	0	1	0	0	0	0		001
	1	0	0	1	0	0	0	0	0		010
	1	0	1	0	0	0	0	0	1	(1st Data)	011
	1	1	0	0	0	0	0	1	0	(Word Here)	100
	1	0	0	0	0	0	1	0	0		101
	1	0	0	0	0	1	0	0	0	= Mk Blk Start	000
1Ø Reverse Pre-Final	1	0	0	0	1	0	0	0	0		001
	1	0	0	1	0	0	0	0	0	(2nd Data)	010
	1	0	1	0	0	0	0	0	1	(Word Here)	011
	1	1	0	0	0	0	0	1	0		100
	1	0	0	0	0	0	1	0	0		101
	1	0	0	0	0	1	0	0	0	= Mk Blk Start	000
7Ø Data Mark	1	0	0	0	1	0	0	0	1		001
	1	0	0	1	0	0	0	1	1		010
	1	0	1	0	0	0	1	1	1	(3rd Data)	011
	1	1	0	0	0	1	1	1	0	(Word Here)	100
	1	0	0	0	1	1	1	0	0		101
	1	0	0	1	1	1	0	0	0		000
7Ø Data Mark	1	0	1	1	1	0	0	0	1		001
	1	1	1	1	0	0	0	1	1		010
	1	1	1	0	0	0	1	1	1		011
	1	1	0	0	0	1	1	1	0		100
	1	0	0	0	1	1	1	0	0		101
	1	0	0	1	1	1	0	0	0		000

	W 1	W 2	W 3	W 4	W 5	W 6	W 7	W 8	W 9		
7Ø Data Mark	1	0	1	1	1	0	0	0	1		000
	1	1	1	1	0	0	0	1	1		001
	1	1	1	0	0	0	1	1	1		010
	1	1	0	0	0	1	1	1	0		011
	1	0	0	0	1	1	1	0	0		100
	1	0	0	1	1	1	0	0	0		101
											000
	Enough Data - Now Proceeding To Block End, And Entering Next Block!										000
73 Pre-Final Mark	1	0	1	1	1	0	0	0	1		001
	1	1	1	1	0	0	0	1	1	(Next to last)	010
	1	1	1	0	0	0	1	1	1	(Data Word)	011
	1	1	0	0	0	1	1	1	0		100
	1	0	0	0	1	1	1	0	1		101
	1	0	0	1	1	1	0	1	1	= Mk Blk End Reset Data Set ST Final	000
73 Final Mark	1	0	1	1	1	0	1	1	1		001
	1	1	1	1	0	1	1	1	1		010
	1	1	1	0	1	1	1	1	1	(Last Data Word)	011
	1	1	0	1	1	1	1	1	0		100
	1	0	1	1	1	1	1	0	1		101
	1	1	1	1	1	1	0	1	1	= Mk Blk End Reset ST Final Set ST CK	000
73 PCC Mark	1	1	1	1	1	0	1	1	1		001
	1	1	1	1	0	1	1	1	1	Reset ST CK Set ST IDLE	010
	1	1	1	0	1	1	1	1	1		011
	1	1	0	1	1	1	1	1	0		100
	1	0	1	1	1	1	1	0	1		101
	1	1	1	1	1	1	0	1	1	= Mk Blk End	000

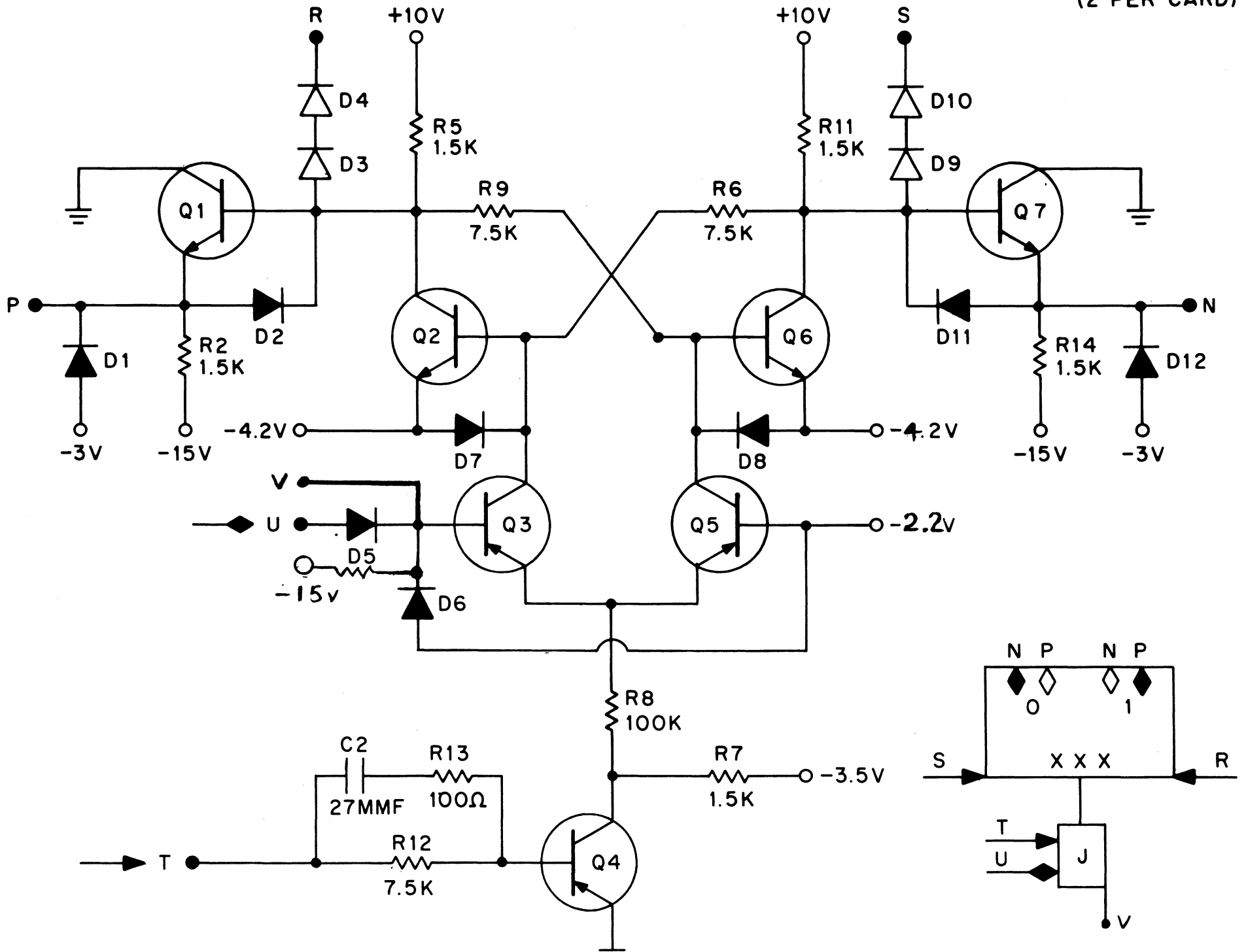
	W 1	W 2	W 3	W 4	W 5	W 6	W 7	W 8	W 9		
73 Reverse Lock Mark	1	1	1	1	1	0	1	1	1		000
	1	1	1	1	0	1	1	1	1		001
	1	1	1	0	1	1	1	1	1		010
	1	1	0	1	1	1	1	1	0		011
	1	0	1	1	1	1	1	0	1		100
	1	1	1	1	1	1	0	1	1	= Mk Blk End	101
											000
51 Guard Mark	1	1	1	1	1	0	1	1	1		001
	1	1	1	1	0	1	1	1	0		010
	1	1	1	0	1	1	1	0	1		011
	1	1	0	1	1	1	0	1	0		100
	1	0	1	1	1	0	1	0	0		101
	1	1	1	1	0	1	0	0	1		000
45 Reverse Block Mark	1	1	1	0	1	0	0	1	1		001
	1	1	0	1	0	0	1	1	0		010
	1	0	1	0	0	1	1	0	0		011
	1	1	0	0	1	1	0	0	1		100
	1	0	0	1	1	0	0	1	0		101
	1	0	1	1	0	0	1	0	1		000
25 Interblock Sync Mark	1	1	1	0	0	1	0	1	0		001
	1	1	0	0	1	0	1	0	1		010
	1	0	0	1	0	1	0	1	0		011
	1	0	1	0	1	0	1	0	1	= C-Sync	100
	1	1	0	1	0	1	0	1	0		101
	1	0	1	0	1	0	1	0	1	= C-Sync	000

	W 1	W 2	W 3	W 4	W 5	W 6	W 7	W 8	W 9		
25 Interblock Sync Mark	1	1	0	1	0	1	0	1	0		000
	1	0	1	0	1	0	1	0	1	= C-Sync	001
	1	1	0	1	0	1	0	1	0		010
	1	0	1	0	1	0	1	0	1	= C-Sync	011
	1	1	0	1	0	1	0	1	0		100
	1	0	1	0	1	0	1	0	1	= Mk Blk Mk	101
										Reset ST IDLE Set ST Blk Mk	000
	$575_{(10)}$ More Blocks To Go. (Assume EOT Next, 198 More Interblock Syncs).										
	Entering FWD End Zones										
22	W 1	W 2	W 3	W 4	W 5	W 6	W 7	W 8	W 9		
FWD End Mark	1	1	0	1	0	1	0	1	0		001
	1	0	1	0	1	0	1	0	1		010
	1	1	0	1	0	1	0	1	0		011
	1	0	1	0	1	0	1	0	0		100
	1	1	0	1	0	1	0	0	1		101
	1	0	1	0	1	0	0	1	0		000
22	1	1	0	1	0	0	1	0	0		001
	1	0	1	0	0	1	0	0	1		010
FWD End MK	1	1	0	0	1	0	0	1	0		011
	1	0	0	1	0	0	1	0	0		100
	1	0	1	0	0	1	0	0	1		101
	1	1	0	0	1	0	0	1	0	= Mk End	000

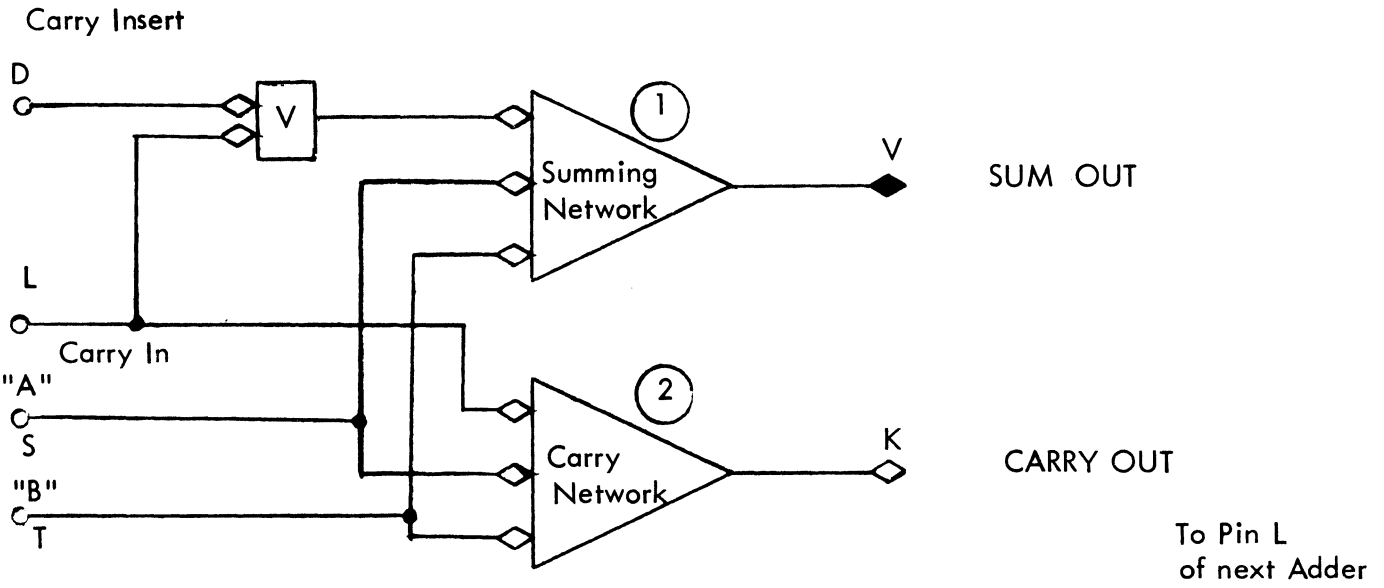


THE S202 F.F.
(2 PER CARD)

THE B213 F.F.
(2 PER CARD)



B-131 ADDER



1. An odd number of inputs true produce a sum out.

2. Two or more inputs true produce a carry out.

SUMMING NETWORK: If an odd number of inputs to the summing network is true, the sum output will be true.

The inputs to the summing network are A (Pin S), B (Pin T), Carry In (Pin L) and Carry Insert (Pin D). Transistors Q1, Q3, Q7, Q9, Q10, Q11, Q2, Q4, Q5, Q6 and Q8 affect the sum output.

The output (Pin V) directly reflects the state of Q4 through Emitter Follower Q8. A -3 Level equals a "One" output, a ground equals a "Zero" output. Thus, if Q4 is off, a "One" output will be reflected through Q8 and conversely, if Q4 is on, a "Zero" output will be felt at Pin V. Q4's state of conduction is controlled by the voltage potential felt on the bases of Q2 and Q5. The potential is developed across resistor R4, thus, the potential is directly controlled by the amount of current allowed to flow through R4. The amount of current that flows through R4 is directly proportional to the number of inputs that are true. If no input is true, minimum current is flowing and if all inputs are true, maximum current will flow. Investigating this current flow further, note that transistors Q1, Q3 and Q9 are all in this current path, therefore, the conduction of these transistors will affect the amount of current that flows through R4. When the transistors are all off, minimum current will flow and when the transistors are all on, maximum current flows. For the sake of discussion, let us assume that when all transistors (Q1, Q3 and Q9) are off, Ø units of current are flowing through R4. When 1 transistor turns on, 1 unit of current flows, 2 transistors on will cause 2 units of current to flow and 3 transistors on will cause 3 units of current to flow. Q1 will turn on when "A" is true. Q3 will turn on when "B" is true. Q9 will turn on if Carry Insert is true or if Carry In is true. Investigating Q9 further you will note that its emitter potential (thus its state of conduction) is controlled by transistor Q7 or Q11. If Carry Insert is true, Q7 turns on, which causes Q9 to turn on. If Carry In is true, the left hand sides of Q10 and Q11 turn on, causing Q9 to turn on. Thus, Carry Insert and Carry In are OR'ed together at transistor Q9. Summing up, there are four units of current possible which flow through R4. These units of current reflect how many inputs are true. It has been stated that there will be a sum output whenever an odd number of inputs is true, therefore, it is possible to conclude that since the number of inputs true will be directly reflected by the units of current present through R4, there will be a sum output whenever odd units of current flow through R4.

When there are no inputs true, Ø units of current flow through R4. The potential developed across R4 is such that it will cause Q5 to turn on. Q5 turning on causes Q6 to turn off. The potential on the base of Q4 is controlled by the conduction state of Q6. Q4 attempts to cut off. However, the base potential on Q2 is more positive than Q4's base potential, which forces Q4 into the on state and Q2 off. Thus, Q4 is conducting, producing a "0" sum out through Q8 to Pin V.

When one input is true, 1 unit of current flows through R4. With the increased current flow the voltage felt on the bases of Q2 and Q5 goes more negative. The change of voltage is not enough to change the conduction state of Q5, therefore, Q5 will remain on and Q6 off. The base of Q2, however, is now more negative than the base of Q4. This causes Q2 to turn on and subsequently Q4 to turn off. Q4 turning off produces a negative level to Pin V through Q8. The sum is now a "1".

When two inputs are true 2 units of current flow through R4, causing the voltage at the base of Q2 and Q5 to go even more negative. It would seem that this would cause Q2 to conduct harder causing Q4 to be cutoff "Harder" than before, still causing a "One" output. However, remember that Q6 was also controling the conduction factor of Q4. The base potential on Q6 is now more positive than that of Q5, causing these transistors to change states. Q5 is now off and Q6 is now on. Q6 turning on causes the base of Q4 to go sharply negative. In fact the base of Q4 is once again more negative than the base of Q2. This causes Q2 to cut off and Q4 to turn on, producing a "0" output for the sum at Pin V.

When three inputs are true, 3 units of current flow through R4, causing the most negative voltage possible to be felt by the bases of Q2 and Q5. Needless to say, a more negative potential on the base of Q5 reaffirms that Q5 is off and Q6 is on. You guessed it! Once again the voltage on the base of Q2 is more negative than the voltage of Q4's base, causing Q2 to turn on and Q4 to turn off, subsequently producing a "1" on the sum output Pin V.

A	B	CI v C Insert	R4 Current Unit	Q2	Q4	Q5	Q6	SUM
0	0	0	0	off	on	on	off	0
0	0	1	1	on	off	on	off	1
0	1	0	1	on	off	on	off	1
0	1	1	2	off	on	off	on	0
1	0	0	1	on	off	on	off	1
1	0	1	2	off	on	off	on	0
1	1	0	2	off	on	off	on	0
1	1	1	3	on	off	off	on	1

SUMMING NETWORK

CARRY NETWORK: If two or more of the three inputs to the Carry Network are true, the Carry Output will be true. The three inputs are "A" (Pin S), "B" (Pin T) and Carry In (Pin L).

The Pin K (Carry Out) voltage is a direct analog representation of the inputs to the carry circuit. There are four distinct states at which the inputs can exist. They are: all off (i.e. not true), one true, two true and all three true. It is possible to conclude that since the inputs can be in four possible conditions, the voltage measured at Pin K (Carry Out) will be indicative of the number of inputs that are true at any given time. There are four possible voltage levels at Pin K. When two or more inputs are true the voltage level at Pin K is an assertive value.

Pin K is connected to the next most significant Adder Stage (Pin L) Carry Input through a 100 ohm resistor, thus the assertive level of a carry out, becomes an assertive carry in level for the next most significant Adder stage.

Briefly, this is how the carry circuit operates. First of all, transistors Q1, Q3, Q12, Q11 (L) and Q11 (R), Q10 (L) and Q10 (R) are associated with the Carry Network. Once again, there are four possible voltages at Pin K. With no inputs true, the voltage at Pin K will be at its most negative level, and with all inputs true, the voltage at Pin K will be most positive. The Pin K voltage is directly dependent on the base voltage of Emitter Follower Q11 (R). The base voltage of Q11 (R) is dependent on the amount of current flowing through R-36 and the voltage at the emitter of Emitter Follower Q12. The current flow through R36 is controlled by the state of conduction of Current Switch Q10 (L) and Q10 (R). The state of Q10 (L) and Q10 (R) is dependent on the Carry Input Level at Pin L. The voltage at the emitter of Emitter Follower Q12 is dependent on the voltage at the base of Q12. This base potential is controlled by the conduction states of Q1 and Q3, which are monitoring the "A" and "B" Inputs at Pins S and T.

There are three possible voltages developed at the base of Q12. The most negative potential will be present when both A and B are not true. The most positive potential will be present when both A and B are true. A middle voltage potential (Halfway between most negative and most positive) will be present when either one of the inputs (A or B) is true. Thus Emitter Follower Q12 is capable of supplying three different voltage potentials to the base of Q11 (R). However, there has to be four voltage potentials at the base of Q11 (R). Q12 supplies three of them. Let us investigate how the fourth voltage is supplied. The fourth potential is supplied via the voltage drop across R36. Needless to say, current must flow through R36. It will be shown that if Carry In is not true, current will flow through R36 developing a voltage. Thus, with no inputs true, the voltage supplied by Q12 will be at its most negative level, delivering 3 negative voltage units to the Q11 (R) stage, and current is flowing through R36, delivering 1 negative voltage unit to the Q11 (R) stage. This causes Pin K (Carry Out) to be at its most negative potential.

Carry In (Pin L) controls Q10 (L) and Q10 (R) in this manner. When Carry In is not true, the base of Q10 (R) will be more positive than the base of Q10 (L). The more positive base level of Q10 (R) is felt on the emitter of Q10 (L). These voltages cause Q10 (R) to turn on and Q10 (L) to turn off. When Q10 (R) turns on current will flow through R 36, which causes one negative voltage unit to be felt on the base of Q11 (R). This signifies that Carry In is not true. When the Carry In voltage (Pin L) reaches an assertive level, the base of Q10 (L) will be more positive than the base of Q10 (R). The more positive level at the base of Q10 (L) is felt on the emitter of Q10 (R). These voltages cause Q10 (L) to turn on and Q10 (R) to cut off. Current ceases to flow through R36. Since current is not flowing through R36 one less, negative voltage unit will be felt on the base of Q11 (R). (i.e. The base voltage of Q11 (R) will raise 1 unit positive.) This signifies Carry In is true.

"A" and "B" (Pins S and T) control the base potential of Q12 in this manner. When "A" and "B" are not true Q1 and Q3 are cut off. This causes D2 and D3 to forward bias. D2 and D3, when forward biased, cause a negative voltage to be fed to the base circuit of Q12, causing the base of Q12 to go negative. The base of Q12 is most negative when both D2 and D3 are forward biased, signifying that both "A" and "B" are not true. Of course this most negative voltage is fed to the base of Q11 (R) conveying the condition of "A" and "B". When either "A" is true or "B" is true (but not both), one of the diodes (D2 and D3) will be forward biased and the other will be reverse biased. This causes the negative voltage on the base of Q12 to be cut in half, which now conveys the fact to Q11 (R) that one of the inputs (either "A" or "B") is true. When both "A" and "B" are true, Q1 and Q3 are turned on, causing diodes D2 and D3 to be reverse biased. This action causes the base of Q12 to go to its least negative voltage, signifying to Q11 (R) that both inputs ("A" and "B") are true.

The Carry Out voltage (Pin K) will be assertive for four combinations of Inputs. Remember if two or more inputs are true, a Carry Out will be generated. Also, remember there is a maximum of four negative voltage units at the base of Q11 (R). Three units are developed at Q12 and one unit is developed at R36. When four or three negative units are present at Q11 (R) Carry Out (Pin K) will be negated. When two or one negative units are present at Q11 (R) the Carry Out (Pin K) will be assertive.

When "A" and "B" are both true, both diodes D2 and D3 are reverse biased, causing the base of Q12 to go to the least negative potential. This causes the base of Q11 (R) to go two units positive producing a Carry Out.

When "A" and Carry In are true, D2 is reverse biased and current does not flow through R36. This causes the base of Q11 (R) to go two units positive producing a Carry Out.

When "B" and Carry In are true, D3 is reverse biased and current does not flow through R36. This causes the base of Q11 (R) to go two units positive producing a Carry Out.

When "A" and "B" and Carry In are true, D2 and D3 are reverse biased and current does not flow through R36. This causes the base of Q11 (R) to go three units positive producing a Carry Out.

The four above conditions are the only combination of inputs that will cause a Carry Out. All other conditions would not cause the voltage on the base of Q11 (R) to go positive enough to produce a Carry Out.

A	B	CI	** Q12 Voltage Potent.	Q10 L	Q10 R	Q11(R) *** Voltage Potent.	* Carry Out
0	0	0	0	Off	On	0	0
0	0	1	0	On	Off	1	0
0	1	0	1	Off	On	1	0
0	1	1	1	On	Off	2	1
1	0	0	1	Off	On	1	0
1	0	1	1	On	Off	2	1
1	1	0	2	Off	On	2	1
1	1	1	2	On	Off	3	1

* A one equals a Carry Out, however, it is an analog voltage and does not represent normal DEC logic levels.

** 0 = Most Negative.
2 = Least Negative.

*** 0 = Least Positive.
3 = Most Positive.

A	B	CI v Cry Insert	R 4 Current	Q2 B_E	Q5 B_E	Q6 B_E	Q4 B_E	Sum Out
0	0	0	1.37 ma	+5.643	+4.893	+2.1	+4.885	0
0	0	1	8.97 ma	+3.659	+2.909	+2.1	+4.885	1
0	1	0	8.97 ma	+3.659	+2.909	+2.1	+4.885	1
0	1	1	15.2 ma	+2.033	+1.283	+2.1	+1.46	0
1	0	0	8.97 ma	+3.659	+2.909	+2.1	+4.885	1
1	0	1	15.2 ma	+2.033	+1.283	+2.1	+1.46	0
1	1	0	15.2 ma	+2.033	+1.283	+2.1	+1.46	0
1	1	1	22 ma	+ .258	− .492	+2.1	+1.46	1

A	B	CI	CO	Q11 (R) E_E	Next Stage Q10 (L) B_E
0	0	0	0	−5.0	−6.7
0	0	1	0	−3.7	−5.7
0	1	0	0	−3.7	−5.7
0	1	1	1	−2.4	−4.6
1	0	0	0	−3.7	−5.7
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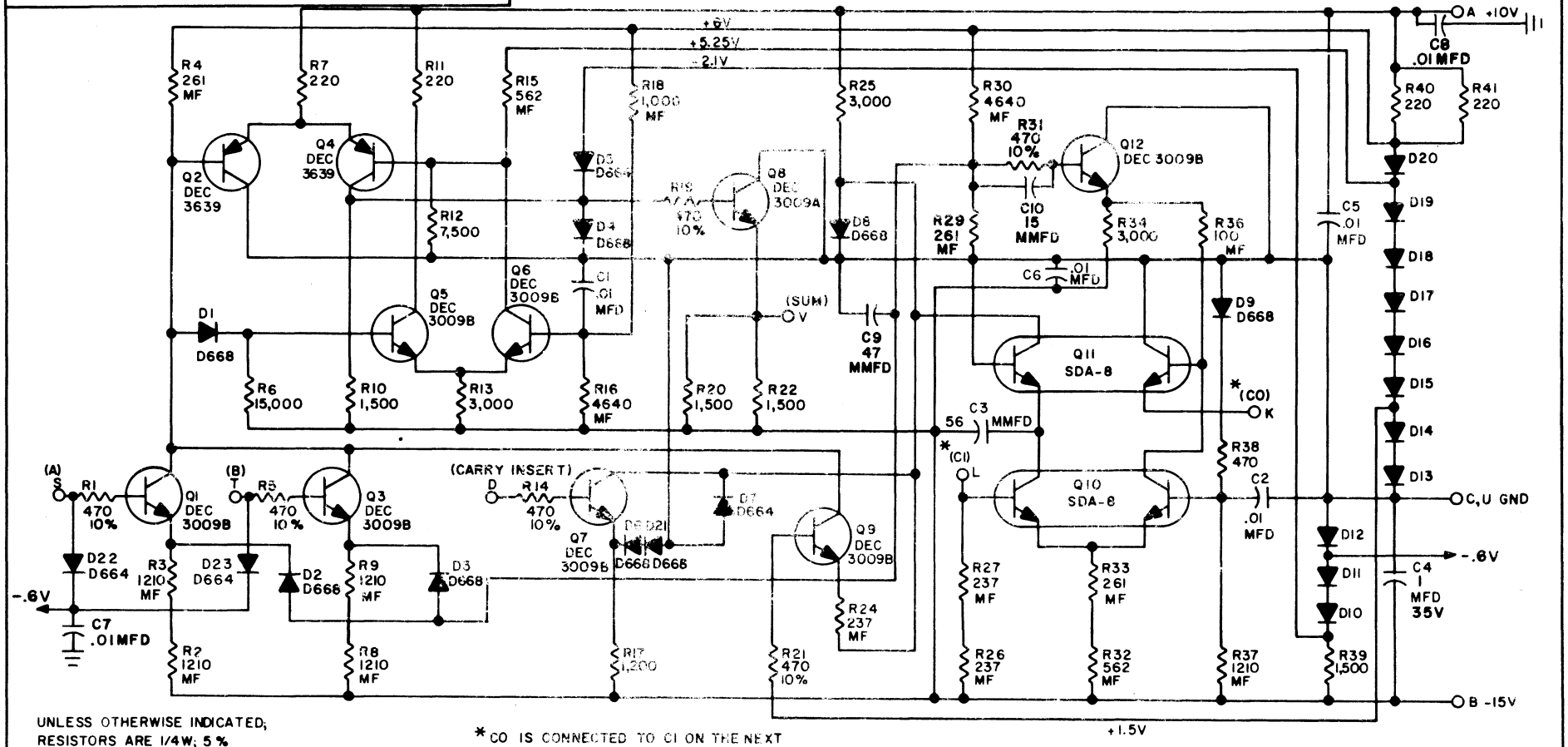
1	1	0	1	−2.4	−4.6
1	1	1	1	−1.1	−3.5



UNLESS OTHERWISE INDICATED;
RESISTORS ARE 1/4W; 5 %
MF RESISTORS ARE METAL FILM 1/8W 1% 100PPM
DIODES ARE D662
D668 2(TWO)IN3606 IN SERIES

*CO IS CONNECTED TO CI ON THE NEXT MODULE BY A 100 Ω 1/4W; 5%, CARBON RESISTOR FROM PIN K TO PIN L

REVISIONS				
CHK	CHG NO	REV		B
DAW	5250	I		C
REV.	BREDR.		5451	D
			5585	E
			5903	
			6496	

DRN	OUELLETTE	DATE 2-7-66
CHK'D	R. SILVERMAN	DATE 2-9-66
ENG	R. SOGGE	DATE 2-9-66
PROD		DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA
DEC3009B	2N3009	D668	SEE NOTE
DEC3639	2N3639		
SDA-8	NONE		
D662	IN645		
D664	IN3606		

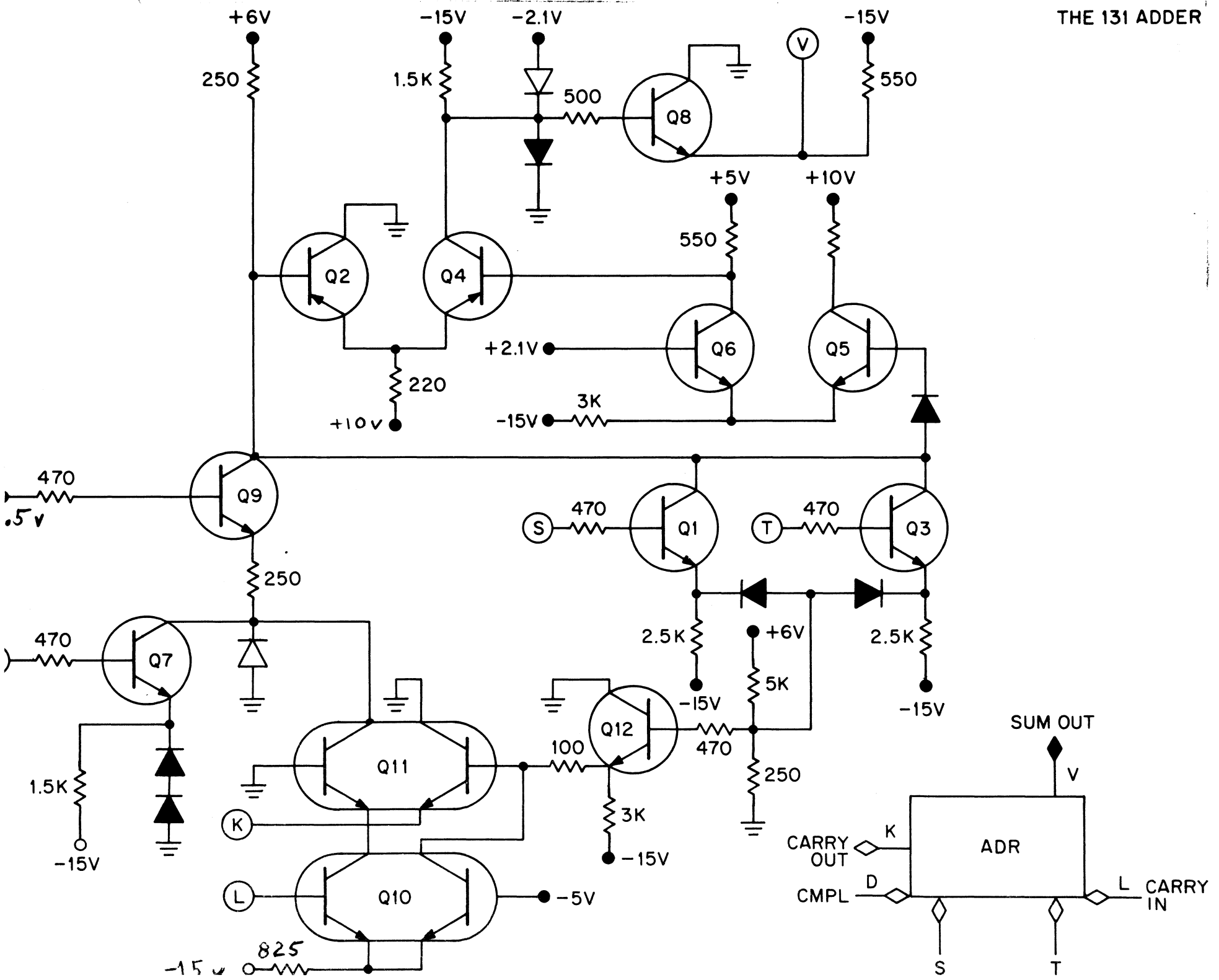
digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE: ADDER B131

SIZE	CODE	NUMBER	REV
B	CS	B131-0-1	E

PRINTED CIRCUIT REV F

DEC FORM NO DRB 102


+6V
−15V
−2.1V
−15V
V
250
1.5K
500
550
Q8
+5V
+10V
550
Q2
Q4
Q6
Q5
+2.1V
220
+10V
3K
−15V
470
.5V
Q9
S
470
Q1
T
470
Q3
250
470
Q7
2.5K
+6V
2.5K
5K
−15V
−15V
Q12
100
470
250
Q11
1.5K
3K
K
−15V
L
Q10
−5V
825
−15V
SUM OUT
V
CARRY OUT
K
ADR
D
CMPL
L
CARRY IN
S
T