IDENTIFICATION

Product Code:	MAINDEC 9A-D1AA-D
Product Name:	PDP-9 Basic Memory Checkerboard Test
Date Created:	December 16, 1966
Maintainer:	Diagnostic Group
Author:	J. W. Richardson

1 ABSTRACT

The PDP-9 Basic Memory Checkerboard Test examines and verifies the operational status of core memory by testing the ability of core memory to detect a 1 or 0 under maximum half-select noise conditions. The program is intended to be used as a means of quick checking an 8K memory field, when the need arises. The test may be performed on a PDP-9 with 8,192 to 32,768 words of core memory. The program tests only the 8K (K=1024) memory bank in which it is located.

For the reasons cited above, it is suggested that the PDP-9 Extended Memory Test be used for a more thorough test on a PDP-9 equipped with or without the extended memory option.

2 REQUIREMENTS

2.1 Equipment

A standard PDP-9 with no less than 8,192 words of core memory.

2.2 Storage

The program occupies $350_{(8)}$ words of core memory, starting at location $21_{(8)}$ up to and including location $370_{(8)}$ when loaded in the lower 4K of an 8K bank. When it occupies the higher 4K of an 8K bank, it occupies locations $17421_{(8)}$ to $17770_{(8)}$.

2.3 Programs

None required except the Basic Memory Checkerboard Test, HRI mode binary tape.

3 LOADING PROCEDURE

The binary tape is punched in the HRI mode and may be read into the lower 4K of any 8K bank of core memory by setting the ADDRESS switches as follows:

BANK	ADDRESS SWITCHES
0	$00021_{(8)}$
1	$20021_{(8)}$
2	$40021_{(8)}$
3	$60021_{(8)}$

After placing the correct value in the ADDRESS switches, set the AC switches to $000000_{(8)}$ and place the binary tape in the reader. Press READ-IN. The program self-starts at the completion of the program load.

4 STARTING PROCEDURE

The program will automatically start at location 00021 of the current memory field immediately after loading and will continue to run until an error is found, or until manually stopped by the operator. Recovery from error halts is discussed in section 6.2.

4.1 Control Switch Settings

Not applicable

4.2 Starting Addresses

Should it be desired to restart the program after a manual stop, there are four addresses available. These are 00021, 00023, 17421, and 17423. The first two addresses are for restarting when the program is located in the lower 4K (00021 to 00370) of an 8K bank, and the last two when the program is located in the upper 4K (17421 to 17770). By observing PC bits 2 through 6, the location of the program at any time may be seen. The restarting addresses are, of course, relative to the memory bank in which the program is located.

4.2.1 Restarting Addresses - 00021 or 17421 with AC switches set to $000000_{(8)}$: Program restores all constants and control words, and runs in its normal fashion.

00023 or 17423 with AC switches set to $XXXXXX_{(8)}$: Program runs in its normal fashion but continues to suppress testing those bits selected by the AC switches as described in section 5.1.

The above addresses are relative to the bank in which the program is located.

4.3 Program Action

The program is first located in memory addresses 00021 to 00375. The portion of core memory from address 10000 to 17777 is tested first. The program then relocates itself, tests from address 00000 to 077777, and relocates back to the lower 4K area and repeats the testing cycle. Before relocating, the area of memory to be occupied is first cleared to 0s.

5 OPERATING PROCEDURE

5.1 Operational Switch Settings

a. ADDRESS switches for loading:

0021. ADDRESS switches 1 and 2 set to the desired memory bank.

b. AC switches:

Any switch in the up position causes the program to suppress the testing of the corresponding bit position in all memory locations. The position of these switches is meaningful only after the occurrence of an error halt. When any switch is in the down position, the corresponding bit is included in the checkerboard patterns and tested for error. (See section 6.1).

5.2 Sub-routine Abstracts

5.2.1 Pattern Generation - The PDP-9 memory checkerboard pattern, when loaded into an 8K memory bank, will consist of words equal to all 1s and 0s. The "half-select" noise presented to the

memory sense amplifiers will be maximum when $20_{(8)}$ memory locations contain the following pattern, complemented every $200_{(8)}$ memory locations throughout the 8K memory bank. Assume the first location to be location 0: four words, each equal to $000000_{(8)}$; eight words, each equal to $777777_{(8)}$ and four more, each equal to $000000_{(8)}$.

In order to place the checkerboard pattern in memory as rapidly as possible, a pattern control word is used. Bits 0-15 of this control word are tested, and if any bit is equal to 0, a word of all 0s is written. Likewise, a word of all 1s is written if the tested bit equals 1. Loading the checkerboard pattern, as described above, requires a control word equal to $037700_{(8)}$. Reading and testing subroutines use this same method.

The memory checkerboard program generates four patterns. The load, read, and test sequence is performed on a 8K memory bank with each pattern. The four control words for the patterns equal 037700; 740076; 037701; and 740077. The first control word generates the pattern previously described; the second generates the complement pattern. In addition, another pattern and its complement are generated using 037701. The pattern generated is similar to the one described previously, but complements every $400_{(8)}$ memory locations instead of every $200_{(8)}$ locations. The complement pattern of this is generated by using 740077. Bit 17 is used to signify whether to complement every $200_{(8)}$ locations or $400_{(8)}$. If the operator were to examine the contents of memory after any one of the patterns had been loaded, each memory location would be observed as equaling that shown in tables 1, 2, or 3, or 4.

Using control word 037700 and complementing every $200_{(8)}$ locations throughout the 8K memory bank:

TABLE 1 PATTERN GENERATED BY CONTROL WORD 037700 COMPLEMENTED EVERY $200_{(8)}$ LOCATIONS

Memory Locations$_{(8)}$	Contents of MB$_{(8)}$
0 through 3	000000
4 through 7	777777
10 through 13	777777
14 through 17	000000
20 through 23	000000
24 through 27	777777
30 through 33	777777
34 through 37	000000
etc.	
200 through 203	777777
204 through 207	000000
210 through 213	000000
214 through 217	777777

Using control word 740076 and complementing every $200_{(8)}$ locations throughout the 8K memory bank:

TABLE 2 PATTERN GENERATED BY CONTROL WORD 740076 COMPLEMENTED EVERY $200_{(8)}$ LOCATIONS

Memory Locations$_{(8)}$	Contents of MB$_{(8)}$
0 through 3	777777
4 through 7	000000
10 through 13	000000
14 through 17	777777
20 through 23	777777
24 through 27	000000
30 through 33	000000
34 through 37	777777
etc.	
200 through 203	000000
204 through 207	777777
210 through 213	777777
214 through 217	000000

Using control word 037701 and complementing every $400_{(8)}$ locations:

TABLE 3 PATTERN GENERATED BY CONTROL WORD 037701 COMPLEMENTED EVERY $400_{(8)}$ Locations

Memory Locations$_{(8)}$	Contents of MB$_{(8)}$
0 through 3	000000
4 through 7	777777
10 through 13	777777
14 through 17	000000
20 through 23	000000
24 through 27	777777
30 through 33	777777
34 through 37	000000
etc.	
360 through 363	000000
364 through 367	777777
370 through 373	777777
374 through 377	000000
400 through 403	777777
404 through 407	000000
410 through 413	000000
414 through 417	777777

Using control word 740077 and complementing every $400_{(8)}$ locations:

TABLE 4 PATTERN GENERATED BY CONTROL WORD 740077 COMPLEMENTED EVERY $400_{(8)}$ LOCATIONS

Memory Locations$_{(8)}$	Contents of MB$_{(8)}$
0 through 3	777777
4 through 7	000000
10 through 13	000000
14 through 17	777777
20 through 23	777777
24 through 27	000000
30 through 33	000000
34 through 37	777777
etc.	
360 through 363	777777
364 through 367	000000
370 through 373	000000
374 through 377	777777
400 through 403	000000
404 through 407	777777
410 through 413	777777
414 through 417	000000

5.2.2 Loading and Testing Routines - One pattern at a time is generated, loaded into memory, and then tested for failure. After a pattern has been loaded into memory, each location under test is read, complemented, and loaded back into its memory location. This sequence is repeated 4 times for each location, and then the location is read once more and tested for failure. In the event of a failure, a program halt occurs at location 000223, or 17623 (Section 6.1)

5.3.3 Relocating the Program - After completing all four memory test patterns, the program will relocate to the opposite end of the memory bank. The "end of the memory bank" being defined as the low or high order 4K portion of an 8K bank. All memory reference instructions used by the program are adjusted accordingly.

The program may be "locked" in one 4K area by manually changing the contents of one memory location. This procedure is described in section 9.1.1.

6 ERRORS

6.1 Error Halts and Description

Upon detecting an error, the program will halt at either location 00223, or 17623. Error identification is accomplished by using the procedure outlined below.

HALT

C(PC) = 00223 or 17623 - C(AC) = Memory address where error occurred.

Press CONTINUE

C(PC) = 00225 or 17625 - C(AC) = Correct data word.

Press CONTINUE

C(PC) = 00227 or 17627 - C(AC) = Incorrect data word.

Press CONTINUE

C(PC) = 00234 or 17634 - C(AC) = Pattern control word.
The correct data word will always equal $000000_{(8)}$ or $777777_{(8)}$.

The incorrect data word will contain at least one bit which will be the complement of the corresponding bit in the correct data word. The complemented bits are the bits which failed.

After the halt at location 00227 or 17627, the AC switches may be set to prevent further testing of the failed bit (s). Place the corresponding AC switch up to prevent further testing of the failed bit (s). After the selection has been made, press CONTINUE (down). The bit (s) selected will not be tested again for failure.

To enable the program to again test all bits, press STOP, and restart program at address 00021 or 17421.

6.2 Error Recovery

To resume normal operation after a program halt at location 00223 or 17623:

a. Press CONTINUE

b. Press CONTINUE

c. Press CONTINUE

d. Press CONTINUE

The program will run until another error is detected.

7 RESTRICTIONS

7.1 Starting Restrictions

Start at memory address 00021 or 17421 to restore all constants and control words, and test all bits for failure.

Start at memory address 00023 or 17423 to suppress testing of bits previously selected with the AC switches.

7.2 Operating Restrictions

The PDP-9 Memory Address Test must have been run successfully before attempting to run this test.

8 MISCELLANEOUS

8.1 Execution Time

One successful pass (i.e., to test memory locations 10000 to 17777, relocate, test memory locations 00000 to 07777, and relocate to the original occupied area) requires approximately 8 seconds, or approximately 4 sec./4K.

9 PROGRAM DESCRIPTION

The PDP-9 Basic Memory Checkerboard Test is designed to be used as a means for a quick check of core memory, and provides a worst case test of any 8K memory bank using four different checkerboard patterns.

An HRI binary tape is supplied as an aid to loading the program. At the completion of program load, the program is loaded from starting address 00021 to 00375 and tests core memory from addresses 10000 to 17777. The program then relocates and occupies memory addresses 17421 to 17775. Core memory addresses 00000 to 07777 are then tested. All four memory checkerboard patterns are generated and tested from each area of memory occupied by the program.

9.1 Program Modifications

9.1.1 Inhibiting Program Relocation - If this situation arises, wait until the program has located itself in the desired area. (Indicated by PC bits 2, 3, 4, 5, and 6.

a. Press STOP.
b. Place 00202 or 17602 in the ADDRESS switches.
c. Press EXAMINE (up). The AC should contain 600235 or 617635.
d. Set the AC switches to either 600023 for the lower 4K, or 617423 for the higher 4K.
e. Press DEPOSIT (up).
f. Set the AC switches to 00021, 17421, 00023, or 17423,
g. Press START.

9.1.2 To Confine Testing to a Selected Area -

a. Do steps 1 through 5 of section 9.1.1. This will inhibit program relocation.

b. Set the ADDRESS switches to 00154 or 17554.

c. Press EXAMINE (up). The AC will contain 200154 or 217554.

d. Place 600170 or 617570 in the AC switches and press DEPOSIT (up).

e. Now set the ADDRESS switches to 00335 or 17735 and press EXAMINE (up). The AC will contain 000000.

f. Place the desired lower limit address in the AC switches. Either XXXX for the lower 4K field, or 1XXXX for the upper 4K field.

g. Press DEPOSIT (up).

n. Set the ADDRESS switches to 00354 or 17754, and press EXAMINE (up). The AC will contain 007777.

i. Place the desired upper limit address in the AC switches.

j. Press DEPOSIT (up).

k. The program may now be restarted at 0021, 00023, 17421, or 17423.

9.1.3 Using Patterns Other than Worst Case Checkerboard - The operator may load memory with any pattern other than the checkerboard pattern by manually changing the four memory locations which contain the pattern control words. All four locations must be changed, if one pattern is desired. Since the pattern is complemented every $200_{(8)}$ or $400_{(8)}$ locations, a NOP instruction may be placed in the load and read subroutines to prevent complementing. Use the following procedure:

a. Press STOP.

b. Place 00337 or 17737 in the ADDRESS switches.

c. Place the desired pattern in the AC switches.

d. Press DEPOSIT NEXT four times. This will place the new control word in locations 00340 to 00343, or 17740 to 17743. Ordinarily, the four locations contain, in order, 037700; 740076;037701; and 740077.

e. Now set the ADDRESS switches to 00072 or 17472.

f. Place 740000 (NOP) in the AC and press DEPOSIT (up).

g. Set the ADDRESS switches to 00150 or 17550. Press DEPOSIT (up). Steps f and g prevent the pattern from complementing. The two memory locations ordinarily contain a CMA instruction.

h. Set the ADDRESS switches to 00021, 00023, 17421, or 17423.

i. Press START.

9.1.4 Summary of Significant Memory Addresses Within the Program -

Program Location		Operator Action	Program Action
Lower 4K	Higher 4K		
00021	17421	Press START	Restores all constants and tests all bits for failure.
00023	17423	Press START	Continues to suppress testing of selected bits.
00223	17623	Observe AC; Press CONTINUE	Error halt. Displays memory location where error occurred.
00225	17625	Press CONTINUE	Error halt. Displays correct data word.
00227	17627	Observe AC; Set ACS to suppress further testing failed bits.	Error halt. Displays data word in error.
		Press CONTINUE	
00234	17634	Press CONTINUE to resume testing.	Displays pattern control word.
00202	17602	Stop. Deposit a JMP to 23 or 17423.	Prevents program relocation.
00154	17554	Stop. Deposit a JMP to 170 or to 17570.	
00335	17735	Examine. Deposit the new lower test limit address.	Changes lower and upper test limits.
00354	17754	Examine. Deposit the new upper test limit address.	
00340 to 00343	17740 to 17743	Contains control words for pattern generator.	Modifies pattern generator. One pattern is written if all four locations contain the same control word.
00072 and 00150	17472 and 17550	Deposit a NOP instruction in place of CMA.	Prevents the pattern from re-complementing.

10. LISTINGS

```
                                .TITLE CKBD8K
                        /PDP-9 BASIC CHECKERBOARD FOR 8K MEMORY
                        /
                                .FULL
00021                           .LOC 21
00021   777777          BEGIN   LAW -1
00022   040361                  DAC BITSUP
00023   200025                  LAC .+2
00024   040204                  DAC NEXPAT
00025   200340                  LAC KPAT
00026   040344                  DAC MPAT
00027   140347                  DZM TEMP
00030   707704                  LEM
00031   700004                  CLOF
                        /
                        /LOAD CHECKERBOARD
                        /
00032   100153                  JMS ADJUST
00033   200344          LOAD    LAC MPAT
00034   040346                  DAC PATWD
00035   777776                  LAW -2
00036   040362                  DAC WC256
00037   777770          CNTA    LAW -10
00040   040325                  DAC WC128
00041   777760          CNTB    LAW -20                 /-16 DECIMAL
00042   040324                  DAC WC16
00043   200346                  LAC PATWD
00044   040345                  DAC PATR
00045   200345          WCLOOP  LAC PATR
00046   744010                  RCL
00047   040345                  DAC PATR
00050   751400                  SZL!CLA                 /TEST FOR A 1 OR 0
00051   740001                  CMA
00052   060334                  DAC* LLREG                      /STORE WORD
00053   200334                  LAC LLREG
00054   540333                  SAD ULREG               /DONE LOADING?
00055   600075                  JMP READ                /YES
00056   440334                  ISZ LLREG               /INCR. ADR
00057   440324                  ISZ WC16                /16 WORDS?
00060   600045                  JMP WCLOOP              /NO
00061   440325                  ISZ WC128
00062   600041                  JMP CNTB
00063   200344                  LAC MPAT
00064   744020                  RCR
00065   740400                  SNL
00066   600071                  JMP .+3
00067   440362                  ISZ WC256
00070   600037                  JMP CNTA
00071   200346                  LAC PATWD
00072   740001                  CMA
00073   040346                  DAC PATWD
00074   600035                  JMP LOAD+2
```

```
                        /READ CHECKERBOARD
00075   200344  READ    LAC MPAT
00076   040351          DAC TEMP+2          /RESTORE PATTERN GEN
00077   100153          JMS ADJUST
00100   777776  RCNTA   LAW -2
00101   040362          DAC WC256
00102   777770          LAW -10
00103   040325          DAC WC128
00104   200351  RCNTB   LAC TEMP+2
00105   040345          DAC PATR
00106   777760          LAW -20             /-26 DECIMAL
00107   040324          DAC WC16
00110   777774  RCLOOP  LAW -4
00111   040337          DAC CLNTH
00112   200345          LAC PATR
00113   744010          RCL
00114   040345          DAC PATR
00115   751400          SZL!CLA
00116   740001          CMA
00117   040346          DAC PATWD           /SAVE FOR COMPARE
00120   220334          LAC* LLREG
00121   740001          CMA
00122   060334          DAC* LLREG
00123   440337          ISZ CLNTH
00124   600120          JMP .-4
00125   220334          LAC* LLREG
00126   540346          SAD PATWD           /COMPARE
00127   741000          SKP                 /OK
00130   600212          JMP ERROR
00131   200334  RDRTN   LAC LLREG
00132   540333          SAD ULREG           /DONE READING?
00133   600177          JMP NXTST           /YES
00134   440334          ISZ LLREG           /INCR. ADR
00135   440324          ISZ WC16            /16 WORDS?
00136   600110          JMP RCLOOP          /NO.
00137   440325          ISZ WC128
00140   600104          JMP RCNTB
00141   200344          LAC MPAT
00142   744020          RCR
00143   740400          SNL
00144   600147          JMP .+3
00145   440362          ISZ WC256
00146   600102          JMP RCNTA+2
00147   200351          LAC TEMP+2
00150   740001          CMA
00151   040351          DAC TEMP+2
00152   600100          JMP RCNTA
```

```
00153   000000          ADJUST  0
00154   200154                  LAC .
00155   500353                  AND LIMIT
00156   740200                  SZA
00157   600170                  JMP ULADJ
00160   200335                  LAC LLTAB
00161   240353                  XOR LIMIT
00162   040334                  DAC LLREG
00163   200332                  LAC ULTAB
00164   040333                  DAC ULREG
00165   200354                  LAC LIMITB
00166   040350                  DAC TEMP+1
00167   620153                  JMP* ADJUST
00170   200335          ULADJ   LAC LLTAB
00171   040334                  DAC LLREG
00172   200354                  LAC LIMITB
00173   040333                  DAC ULREG
00174   200365                  LAC (11
00175   040350                  DAC TEMP+1
00176   620153                  JMP* ADJUST
                        /
00177   200347          NXTST   LAC TEMP
00200   240366                  XOR (600000
00201   741200                  SNA
00202   600235                  JMP ENTST
00203   440204                  ISZ .+1
00204   200340          NEXPAT  LAC KPAT
00205   040344                  DAC MPAT
00206   200347                  LAC TEMP
00207   340367                  TAD (200000
00210   040347                  DAC TEMP
00211   600032                  JMP LOAD-1
                        /
00212   040352          ERROR   DAC TEMP+3
00213   500361                  AND BITSUP
00214   740200                  SZA
00215   740001                  CMA
00216   500361                  AND BITSUP
00217   741200                  SNA
00220   600131                  JMP RDRTN
00221   200334                  LAC LLREG               /DISPLAY ADDRESS
00222   740040          ERADR   HLT
00223   200346                  LAC PATWD               /GOOD DATA
00224   740040          GDATA   HLT
00225   200352                  LAC TEMP+3              /BAD DATA
00226   740040          BDATA   HLT
00227   750004                  LAS                     /SUPPRESS HERE
00230   740001                  CMA
00231   040361                  DAC BITSUP
00232   200351                  LAC TEMP+2              /PATTERN CONTROL WORD
00233   740040          PATT    HLT
00234   600131                  JMP RDRTN
```

```
00235   770000      ENTST   LAW -10000
00236   040357              DAC WDCNT
00237   200237              LAC .
00240   500353              AND LIMIT
00241   740200              SZA                 /IN LOWER 4K NOW?
00242   600316              JMP MVBK            /NO
00243   740001              CMA
00244   040351              DAC TEMP+2          /SOURCE ADR
00245   200336              LAC ADJUL           /U.L. START ADR
00246   040352              DAC TEMP+3          /DEST'N
00247   200351      MOVE    LAC TEMP+2
00250   040363              DAC MOVES
00251   200350              LAC TEMP+1
00252   040364              DAC MOVED
00253   440364              ISZ MOVED
00254   160364              DZM* MOVED              /CLEAR DEST'N TO 0'S
00255   440357              ISZ WDCNT           /-4K
00256   600253              JMP .-3
00257   200352              LAC TEMP+3
00260   040364              DAC MOVED           /RESTORE DEST'N S.A.
00261   440363      RFROM   ISZ MOVES
00262   220363              LAC* MOVES                  /FROM
00263   040350              DAC TEMP+1
00264   500370              AND (700000         /MASK OP CODE
00265   240370              XOR (700000
00266   740200              SZA                 /OPR. INSTRUCTION?
00267   600313              JMP MRINS           /NO. MEMORY REF
00270   200350              LAC TEMP+1
00271   440364      MVRTN   ISZ MOVED
00272   060364              DAC* MOVED
00273   540323              SAD LIMITA
00274   741000              SKP                 /YES
00275   600261              JMP RFROM
00276   777727      MVCST   LAW -51
00277   040337              DAC CLNTH
00300   440363              ISZ MOVES
00301   220363              LAC* MOVES                  /MOVE CONSTANTS
00302   440364              ISZ MOVED
00303   060364              DAC* MOVED
00304   440337              ISZ CLNTH
00305   600300              JMP .-5
00306   200306              LAC .
00307   500353              AND LIMIT
00310   741200              SNA                 /IN UPPER 4K NOW?
00311   620355              JMP* ULSA           /NO
00312   620331              JMP* KJMP           /BEGIN
                    /
00313   200350      MRINS   LAC TEMP+1
00314   240356              XOR ULMVA
00315   600271              JMP MVRTN
```

```
00316   200365          MVBK    LAC (11
00317   040352                  DAC TEMP+3
00320   200360                  LAC MVUP
00321   040351                  DAC TEMP+2
00322   600247                  JMP MOVE
                        /
                        /
                        /CONSTANTS
                        /
00323   752525          LIMITA  752525    /DELIMITER
00324   000000          WC16    0         /16 WORD COUNTER
00325   000000          WC128   0         /128 WORD COUNTER
00326   000000          MRJP    0         /USED FOR INDIRECTS
00327   000033          LRJP    LOAD      /RETURN JUMP
00330   000100          RRJP    RCNTA     /DITTO
00331   000023          KJMP    BEGIN+2   /L. L. PROGRAM S.A.
00332   017777          ULTAB   017777    /UPPER LIMIT ADDRESS
00333   000000          ULREG   0         /STORAGE FOR U.L.
00334   000000          LLREG   0         /STORAGE FOR L.L.
00335   000000          LLTAB   0         /L.L. ADDRESS
00336   017377          ADJUL   017377    /USED FOR PROGRAM MOV
00337   000000          CLNTH   0         /STORAGE FOR CONSTANT TABLE LENGTH
00340   037700          KPAT    037700    /PATTERN GENERATED
00341   740076                  740076
00342   037701                  037701
00343   740077                  740077
00344   037700          MPAT    037700    /DITTO
00345   000000          PATR    0         /STORAGE FOR ABOVE
00346   000000          PATWD   0         /DITTO
00347   000000          TEMP    0         /THESE FOUR FOR TEMP STORAGE
00350   000000                  0
00351   000000                  0
00352   000000                  0
                        /
00353   010000          LIMIT   010000
00354   007777          LIMITB  007777
00355   017423          ULSA    017423    /U.L. PROGRAM S.A.
00356   017400          ULMVA   017400    /USED TO ADJUST MCS REF. INST
00357   770000          WDCNT   770000    /-4K
00360   017411          MVUP    017411
00361   777777          BITSUP  777777    /FOR BIT SUPPRESSION
00362   777776          WC256   777776
00363   000000          MOVES   0         /SOURCE ADDRESS FOR RELOCATION
00364   000000          MOVED   0         /DEST'N ADDRESS FOR RELOCATION
        000021                  .END BEGIN
00365   000011      *LIT
00366   600000      *LIT
00367   200000      *LIT
00370   700000      *LIT
```